# OPTOELECTRONIC MONOLITHIC INTEGRATION OF METAL-GERMANIUM-METAL PHOTODETECTOR AND GE CMOSFETS ON SI WAFER

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**NATIONAL UNIVERSITY OF SINGAPORE**

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**ZANG HUI**
**(M. SCI., National University of Singapore)**

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# Table of contents

## Chapter 2 Germanium Epi-growth on Si Substrate



## Chapter 3 Application of dopant segregation to metal-germanium-metal photodetector and its dark current suppression mechanism

## Chapter 4 High-Speed Surface-illuminated Metal-Germanium-Metal Photodetector



## Chapter 5 High-Speed Metal-Germanium-Metal Photodetector Integration with SOI Waveguide

## Chapter 6 Germanium CMOSFET integration on Silicon Substrate



## Chapter 7 Conclusion

## Appendix

# Summary

Silicon-based optoelectronic device is a promising candidate to replace the III–V compound semiconductor devices due to its low cost, ease of process, and CMOS integration compatibility. Heteroepitaxial Ge on Si provides an alternative solution for near-infrared photodetection since surface-smooth Ge epitaxial layer can be realized on Si wafer using two-step Ge growth method. Metal-germanium-metal (MGM) photodetector attracts much research interest due to its ease of fabrication, low detector capacitance, and large device bandwidth as its main advantages. This thesis mainly presents the development of surface-illuminated and waveguided MGM photodetectors integrated on Si substrate and their potential integration with Ge CMOSFETs.

First, a novel technique of Ge epi-growth on Si substrate for photodetectors fabrication was developed. Low defect density and surface-smooth epi-Ge layer on Si substrate provides an excellent platform for Ge photodetectors and Ge CMOSFETs fabrication. Secondly, surface-illuminated MGM photodetectors on Si substrate were demonstrated with very low dark current and large bandwidth using the developed epi-growth method. Meanwhile, for the first time, dopant segregation technique was applied in MGM photodetectors for dark current suppression. The optimal dopant segregation scheme in NiGe barrier preferably modulates the effective Schottky barrier height (SBH) in NiGe/Ge contact and significantly suppressed the dark current without photocurrent degradation. For optoelectronic integration, we designed and fabricated MGM photodetectors integrated with SOI waveguide. The integration of photodetector with waveguide overcomes the trade-off between the detection efficiency and bandwidth in surface-illuminated photodetectors. Therefore, the waveguide-integrated MGM photodetectors with scaled contact spacing achieved

much higher detection efficiency and bandwidth than the surface-illuminated counterpart with the same Ge thickness. Furthermore, conventional MGM photodetectors can only work under photoconductive condition, thus making the high standby power unavoidable. By applying dopant segregation technique in MGM photodetector, the device achieves a very high bandwidth in photovoltaic condition (i.e., 0-V bias). Finally, Ge CMOSFETs based on the previously developed epi-growth technique were demonstrated on Si substrate for the first time and characterized for investigating the feasibility of the MGM photodetectors integration with Ge CMOSFETs instead of Si CMOSFETs. The Ge CMOSFETs on Si substrate with high-κ dielectric and metal gate shows very low gate leakage current and favorable mobility enhancement.

This study has set up a research framework for development of Ge photodetectors from surface-illumination to integration with waveguide and the potential integration with Ge CMOSFETs, indicating that monolithic integration of MGM photodetectors and Ge CMOSFETs is very promising for optoelectronic integrated circuits.

# List of Tables

# List of Figures

as compared to Si universal mobility

# LIST OF SYMBOLS

| | |
|---|---|
| $\hbar$ | Planck's constant |
| $C_{ox}$ | Gate dielectric capacitance |
| $E_g$ | Bandgap |
| $\varepsilon$ | Permittivity |
| $\kappa$ | Dielectric constant |
| $\mu_e$ | Mobility of electron |
| $\mu_h$ | Mobility of hole |
| $\mu_{eff}$ | Effective mobility |
| $\Phi_{be}$ | Electron Schottky barrier height |
| $\Phi_{eh}$ | Hole Schottky barrier height |
| $I_p$ | Photocurrent |
| $\eta$ | Quantum efficiency |
| GHz | Gigahertz |
| n | Reflection index |
| $g_m$ | Transconductance |
| $V_{th}$ | Threshold voltage |
| $I_{dark}$ | Dark current |
| R | Responsivity |
| $V_D$ | Drain voltage |
| $J_g$ | Gate leakage current density |

# LIST OF ABBREVIATION

| | |
|---|---|
| AFM | Atomic force microscopy |
| BARC | Bottom anti-reflective coatings |
| CMOSFET | Complementary metal oxide semiconductor field effect transistors |
| CMP | Chemical mechanical polishing |
| CV, C-V | Capacitance versus Voltage |
| DI | De-ionized |
| DWDM | Dense wavelength division multiplexing |
| EOT | Equivalent oxide thickness |
| $E_{buid\text{-}in}$ | Build-in electric field |
| FWHM | Full width at half maximum |
| GIDL | Gate induce drain leakage |
| HP | High-performance |
| HF | Hydrofluoric acid |
| HR-TEM | High resolution transmission electron microscopy |
| IC | Integrated circuit |
| ITRS | International technology roadmap of semiconductor |
| I-V | Current versus voltage |
| MBE | Molecular beam epitaxy |
| MSM | Metal-semiconductor-metal |
| MGM | Metal-germanium-metal |
| MBE | Molecular beam epitaxy |
| OEIC | Optoelectronic integrated circuit |
| PDA | Post-deposition annealing |

| | |
|---|---|
| PECVD | Plasma enhanced chemical vapor deposition |
| PR | Photo resist |
| RMS | Root mean square |
| RTA | Rapid thermal annealing |
| RTP | Rapid thermal processor |
| RIE | Reactive ion etching |
| RC delay | Resistance-capacitance delay |
| SEM | Scanning electron microscopy |
| SB | Schottky barrier |
| SBH | Schottky barrier height |
| SOI | Si on isolator |
| SIMS | Secondary ion mass spectrometry |
| TEM | Transmission electron microscopy |
| TCE | Thermal coefficient of expansion |
| ULSI | Ultra-large scale integrated circuits. |
| UHV-CVD | Ultra-high vacuum chemical vapor deposition |
| $V_{buid\text{-}in}$ | Build-in voltage |

# Chapter 1:

# Introduction

## 1.1 Optoelectronics Integrated Circuit

The rapid development of silicon-based microelectronics significantly changed the life of human beings in the past four decades. In modern communication technology, tens of millions of complementary metal oxide semiconductor field effect transistors (CMOSFET) were fabricated on Si chip for information processing [1.1]. However, with the improvement of process technology, the circuit based on CMOSFET is approaching some fundamental limits. First, with the scaling of device feature and the increase in device number per unit area, the resistance-capacitance (RC) delay induced by the scaling of metal interconnects spacing becomes more and more severe and slows down the processing speed of chip. Secondly, metal interconnect intrinsically suffers from heat dissipation problem. Therefore, metal interconnect becomes the bottleneck for ultra-high speed data transmission and hinders the performance enhancement of microprocessors. Silicon-based optoelectronic integrated circuit (OEIC) had been proven to be a promising solution to overcome the bottleneck of massive interconnects [1.2], since OEIC involves optical waveguide as device interconnect instead of metallic wire. The waveguide, as signal transmission line, overcomes the RC delay issue induced by metal interconnect. Besides, waveguide is free of heat dissipation since there is no heat generation during the optical signal propagation in waveguide.

Fig. 1.1 shows the schematic diagram of a photonics circuit for dense wavelength division multiplexing (DWDM). The optical signals with different wavelengths from optical fiber are coupled into optical waveguide. The ring resonator

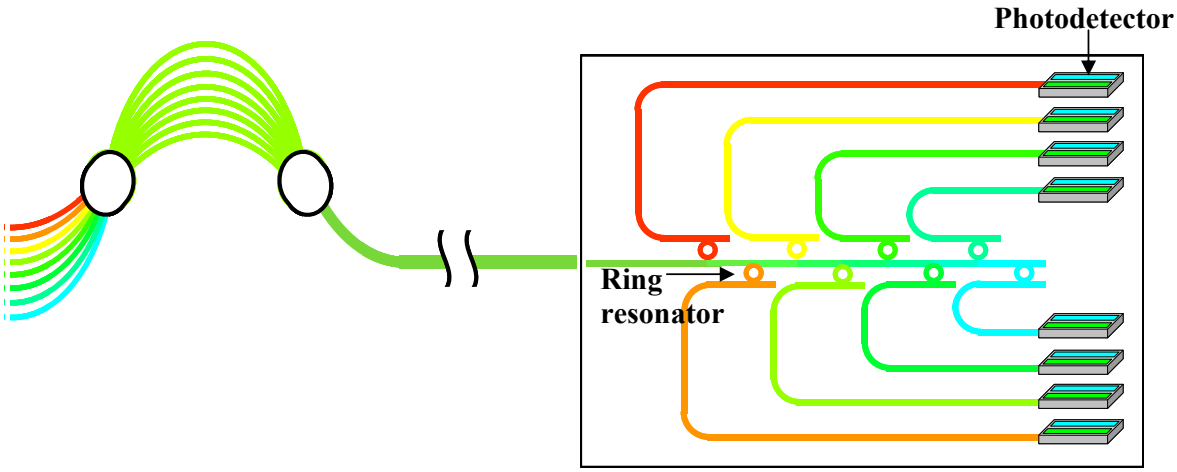


**Fig. 1.1 Schematic diagram of a photonic circuit for dense wavelength division multiplexing (DWDM).**

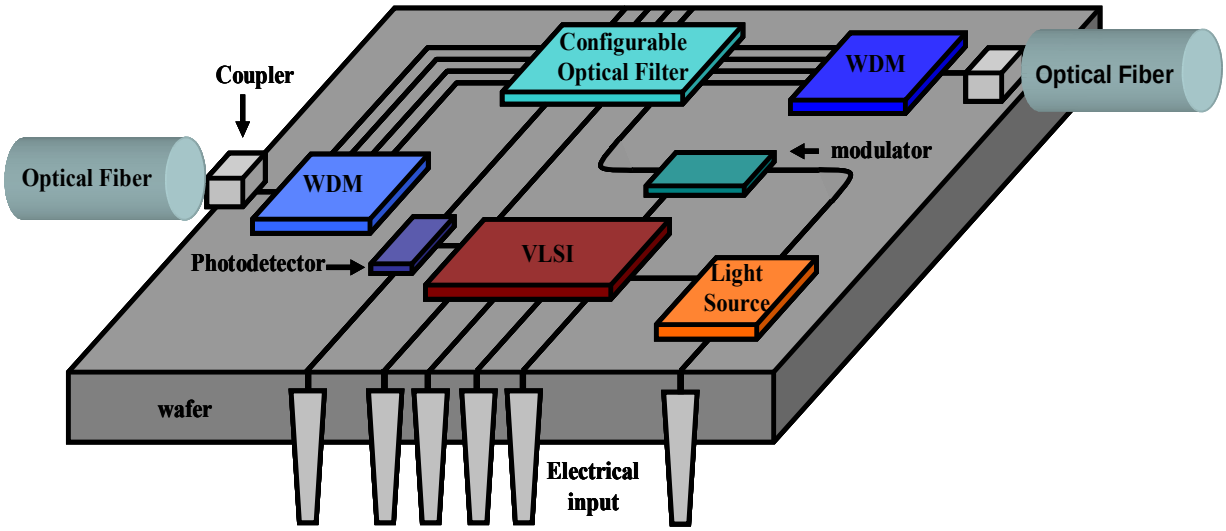


**Fig. 1.2 Schematic diagram of an optoelectronics integrated circuit (OEIC).**

selects the optical signals according to their respective wavelengths. The filtered signals will propagate to the photodetectors and be converted into electrical signals. In this way, the electrical circuit can receive optical signals from optical fibers. As shown in Fig. 1.2, OEIC needs several photonics devices to be integrated on Si chip: 1) Light sources for optical signal generation, 2) modulators to generating optical 0 and 1 signal by applying voltage, 3) photodetectors for signal detection and 4) optical waveguides for signal transmission between devices. Integrating photonics device and microelectronics device on the same chip can significantly improve circuit performance. Therefore, the fabrication processes for all the photonics devices in OEIC are required to be CMOS compatible.

## 1.2 Photodetector Fundamentals

Photodetector, as the optical signal detection device, is one of the important building blocks for OEIC. In concept, photodetector is an optoelectronic device that absorbs optical energy and converts it to either current or voltage. The converted electrical signal is subsequently amplified and further processed. The most frequently used photodetectors in communication are semiconductor-based photodetectors. Its work mechanism is that, when a photon of sufficient energy is incident to a detector active region, it excites a mobile electron and hole. These carriers are swept from the active region to electrodes by the built-in field in the depletion region or electrical field induced by applied bias, and then a photocurrent is produced. There are several kinds of semiconductor-based photodetectors in terms of configuration such as PN photodetector, PIN photodetector and metal-semiconductor-metal (MSM) photodetector. Photodetector must satisfy some requirements such as high sensitivity at the operating wavelength, high response speed, and low dark current. In addition,

photodetectors should be compact in size and reliable in operation.

For photodetectors, there are two working modes which are called photovoltaic mode and photoconductive mode. Photovoltaic mode photodetector can work at a zero bias. In the case of a zero bias, the flow of photocurrent is induced by build-in electric field. Photovoltaic mode is very desirable in integrated circuits since the stand-by power due to leakage current is significantly reduced. However, in most cases, device can only work in biased conditions, and the device which operates under applied bias is called photoconductive mode photodetector. For instance, conventional MSM photodetector is in photoconductive mode and can only work under applied bias. In PN and PIN photodiode, although there is a build-in electric field in depletion region, detectors still work under a reverse bias in most conditions for high speed operation. The applied bias increases the width of depletion layer, which decreases the junction's capacitance, resulting in faster response time.

There are three main parameters to evaluate photodetector performance including responsivity, dark current and bandwidth. First, responsivity is a parameter which indicates device efficiency. In formula, responsivity is the ratio of generated photocurrent ($I_p$) to incident light power (P). Typically it is expressed as:

$$R=I_p/P=e\eta/h\nu \qquad (1.1)$$

The responsivity can also be expressed using quantum efficiency ($\eta$), where $\eta$ is the ratio of the number of photogenerated carriers to that of incident photons, h is the Planck's constant and $h\nu$ is photon energy.

For photoconductive mode devices, dark current is the standby leakage current when no light is incident on the photodetector. Dark current is an important parameter to evaluate the standby power consumption of devices, and it is also a source of device noise. Therefore, dark current should be suppressed to be as low as possible.

The operation speed of a photodetector is important, especially for optical-fiber communications system. The response of a photodetector is required to be fast enough compared to the digital transmission data rate. Bandwidth is used to represent how fast a device can work, and it is normally measured in the unit of gigahertz (GHz). There are two factors which affect the bandwidth of photodetectors:

1) The drift time of carriers through the depletion region.

The transit time ($t_c$) represents the maximum time carriers taken to cross over the device depletion region. It is device configuration and size dependent and can be expressed as $t_c$ = w/v, where w is the depletion width and v is the carrier saturation velocity.

2) RC time constant of equivalent circuit.

The time taken to discharge the parasitic capacitance ($C_{pd}$) through load resistance $R_L$ is another factor related to device response time and can be expressed as $t_{RC}=2.2R_LC_{pd}$. Low device capacitance is always desirable for high bandwidth operation [1.3].

## 1.3 Material Candidates for Photodetector

Material selection for photodetector fabrication needs serious consideration. In OEIC, the semiconductor material used in photodetector must fulfill two basic requirements. First, in current DWDM technology, the signal wavelengths used are C-band (1528–1560 nm) and L-band (1561–1620 nm), which means the absorption range of semiconductor material is required to cover C- and L-band [1.4]. Direct band-to-band absorption in semiconductor occurs when bounded carriers interact with a photon whose energy is greater than its band gap energy. Absorption is generally expressed in absorption coefficient. The absorption coefficients for some photodetector material candidates as a function of wavelength are shown in Fig. 1.3

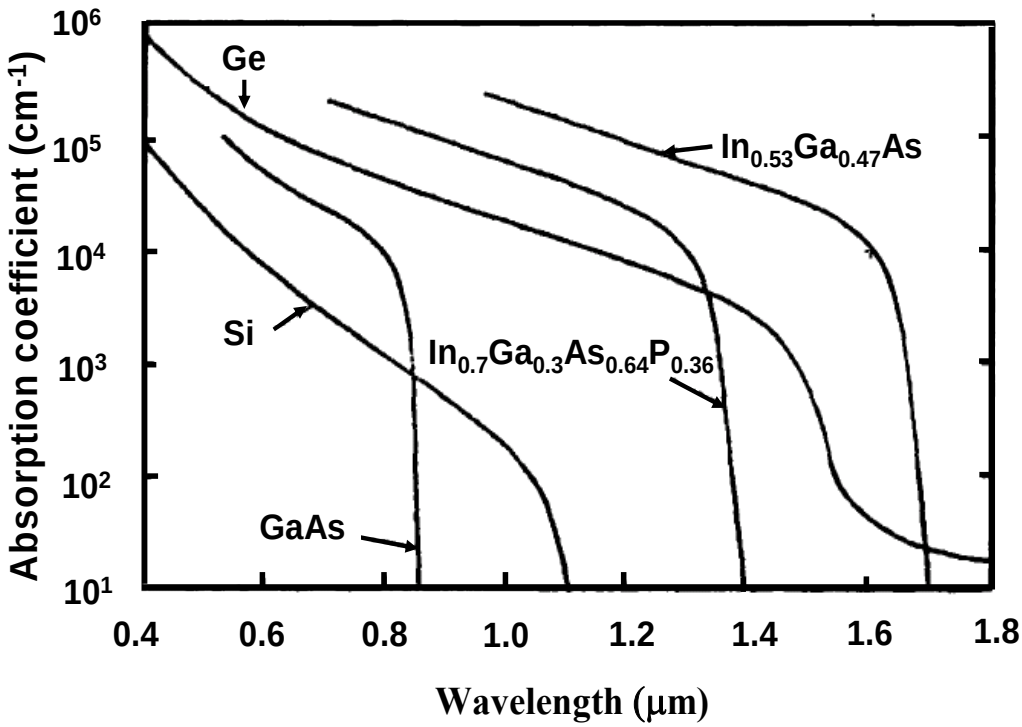


**Fig. 1.3 Optical absorption coefficients for various photodetector material candidates [1.5].**

[1.5]. The sharp decline in absorption near the direct band gap is clearly visible.

Among all the known materials, InGaAs is an ideal material for near-infrared photodiodes fabrication due to its large absorption range. InGaAs photodetectors exhibit the best device performances with regards to detection responsivity, dark current and bandwidth [1.6] [1.7] [1.8] [1.9] [1.10]. Current commercial photodetector material is $In_{0.53}Ga_{0.47}As$ which is fabricated on InP substrate. However, InGaAs photodetector integration on Si based integrated circuit (IC) induces many serious issues and challenges. The first challenge is InGaAs epitaxy growth on Si substrate. The main issue is the 8 % lattice mismatch between $In_{0.53}Ga_{0.47}As$ and Si (Si lattice constant: 5.43 Å; $In_{0.53}Ga_{0.47}As$ lattice constant: 5.87 Å) which leads to high density of threading dislocations and misfits dislocations in epitaxy thin film. High density of

threading dislocations significantly degrades detector performance. An alternative approach to integrate InGaAs photodetectors on Si wafer is to utilize wafer bonding technique [1.11] [1.12] [1.13]. However, this technique cannot be applied in designated small area in IC, which hinders large scale integration. Another issue for introducing InGaAs to IC is that InGaAs easily induces serious cross-contamination into Si based circuit since every element in InGaAs is dopant to Si wafer. Besides, the poor thermal stability of InGaAs makes itself not CMOS process compatible. For instance, in temperature range of 700-900$^{o}$C, InGaAs significantly loses As element [1.14][1.15].

With the development of strain engineering in CMOS technology, SiGe and SiGeC were successfully introduced into Si MOSFET by epitaxy growth for device performance enhancement. However, SiGe cannot be used for photodetector fabrication since the band gap of SiGe is not narrow enough to cover the wavelength of 1550 nm. Ge is considered to be a promising candidate material for CMOS compatible near-infrared photodetectors fabrication since it offers some desirable properties. First, Ge does not induce contamination to Si-based IC. Secondly, Ge has an indirect band gap of 0.66 eV which covers the absorption wavelength up to1867 nm as shown in Fig. 1.4. However, without phonon assist, photon alone is not enough for carrier pair generation. Nevertheless, Ge has a direct band gap of 0.8 eV which corresponds to 1550 nm. J. F. Liu in MIT demonstrated a Ge photodetector with tensile strain on Si and extended the absorption wavelength up to 1600 nm [1.16][1.17], which indicates that Ge is very promising for near-infrared photodetectors application in OEIC. Besides, Ge offers 2.8 times electron-mobility (3900 cm$^2$/V.s) and 4 times hole-mobility (1900 cm$^2$/V.s) over Si. High carrier mobility is very desirable for high speed operation in low bias condition. On the other

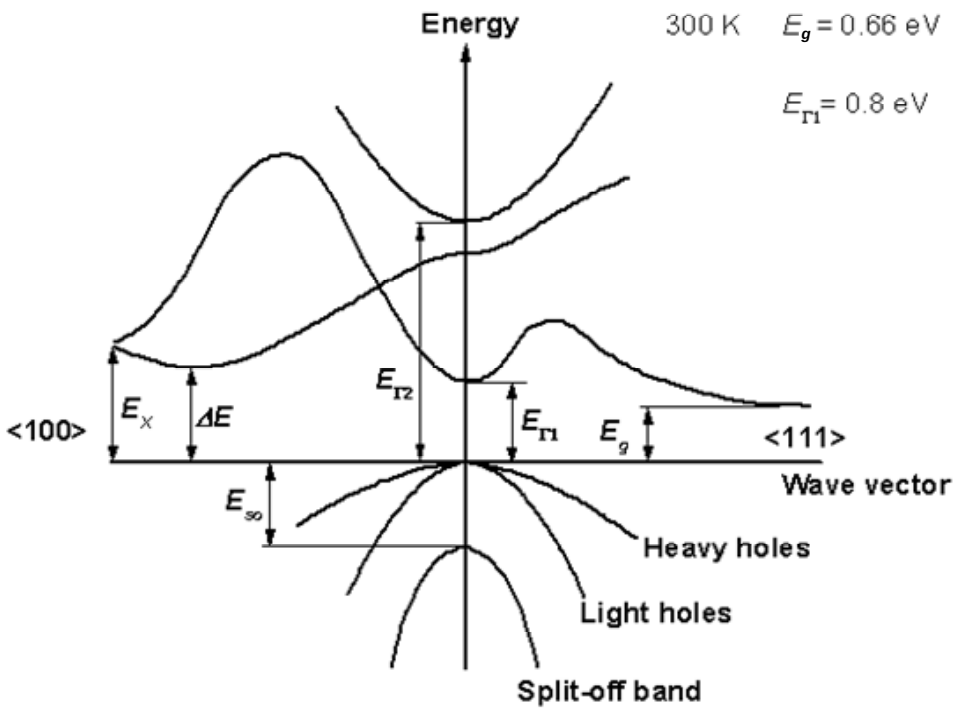


**Fig.1.4 Band diagram of Germanium at 300K. [1.15]**

hand, Ge MOSFET is also considered to be a promising candidate to replace Si MOSFET and was successfully demonstrated with mobility enhancement [1.18][1.19][1.20].

Many researchers have switched their research interest to Ge near-infrared photodetector. First, much research was addressed in Ge epitaxy growth on Si substrate for Ge photodetector fabrication [1.21][1.22][1.23]. Even though there is 4% lattice mismatch between Ge and Si (Si lattice constant: 5.43 Å; Ge lattice constant: 5.65 Å), high-quality Ge with low threading dislocation density ($10^6$-$10^{-7}$ $cm^{-2}$) was successfully achieved on Si substrate by ultra-high vacuum chemical vapor deposition (UHV-CVD) and molecular beam epitaxy (MBE) using novel epi-growth technique [1.23][1.24]. Subsequently, Ge detectors on Si substrate with high detection efficiency

and high bandwidth were also demonstrated [1.24][1.25][1.26]. The Ge epitaxy growth on Si will be reviewed and discussed in Chapter 2.

## 1.4 Metal-Germanium-Metal Photodetector

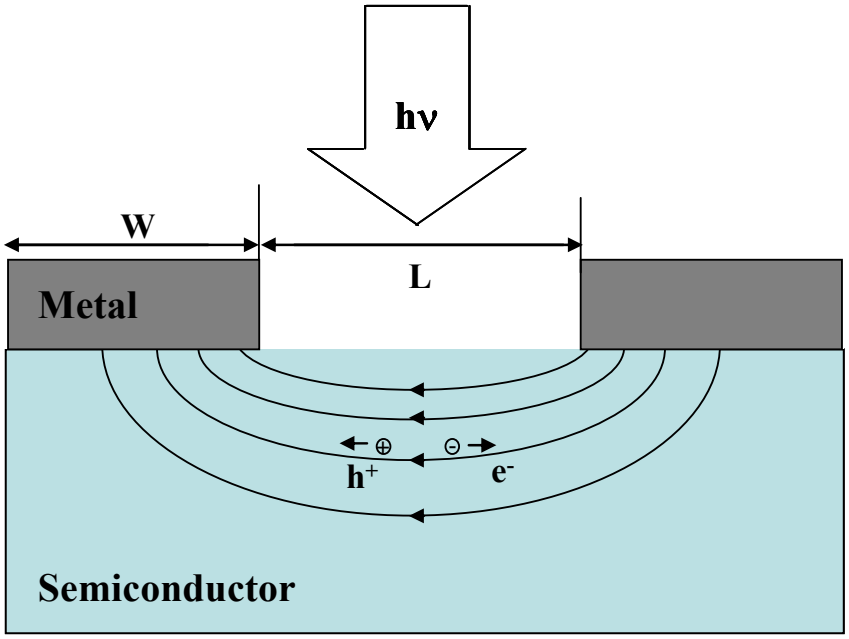


**Fig. 1.5 Schematic of MSM photodetector under bias and illumination.**

Metal-semiconductor-metal (MSM) photodetector is an attractive device structure due to its ease of process, low capacitance and large bandwidth. Fig. 1.5 shows a schematic of typical surface-illuminated MSM photodetector under biased condition. MSM photodetector is a planar structure device with two metal contacts on the semiconductor active region. The two Schottky contacts can be designed to be single pads or interdigitated for preference. The simple configuration minimizes the process steps needed and makes the device fabrication easier. Ge-based MSM photodetector is usually called metal-germanium-metal (MGM) photodetector.

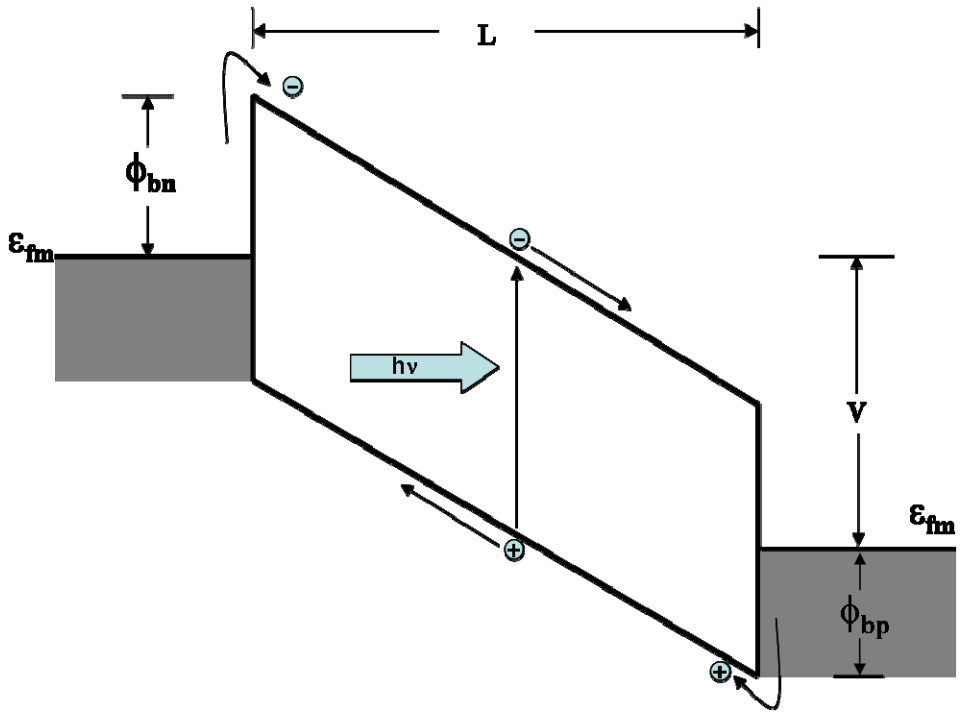


**Fig. 1.6 Energy band diagram of an MSM photodetector under bias.**

The energy band diagram of MSM photodetector with an applied bias is shown in Fig. 1.6. When incident photons are absorbed by semiconductor, the generated carrier pairs will drift under electric field and be collected by the metal electrodes. In no-photon condition, the major component of dark current is the carrier emission over Schottky barrier (SB). Therefore, the dark current density under this condition is given by:

$$J = A_n^{**} T^2 e^{-q(\phi_{bn} - \Delta\phi_{bn})/k_B T} + A_p^{**} T^2 e^{-q(\phi_{bp} - \Delta\phi_{bp})/k_B T} \tag{1.2}$$

where $A^{**}$ is the respective Richardson constants and ΔΦ's are the respective barrier height lowering due to the image force effect [1.3]. In the formula, it is obivious that Schottky barrier height (SBH) plays a crucial role in device dark current. To achieve low dark current, relatively high SBH for both electron and hole ($\Phi_{bn}$ and $\Phi_{bp}$) are needed. The summation of $\Phi_{bn}$ and $\Phi_{bp}$ equals the band gap energy of the

semiconductor. Therefore, when metal work function is pinned to the middle of the band gap, the lowest dark current can be achieved. However, most of metal-semiconductor junction has a small hole SBH or a small electron SBH. In the case of MGM photodetectors, device suffers from high dark current due to the small hole SBH (0.1 eV) in metal/Ge junction [1.27]. The Fermi level pinning between metal and Ge is always near the valence band. In Chapter 3 and 4 of this thesis, a novel technique for MGM photodetector dark current suppression will be discussed.

As discussed in the paragraph above, low capacitance is highly preferred for high bandwidth consideration. The MSM photodetector capacitance was shown to be less than half that of a PIN photodiode [1.3][1.5]. Therefore, the bandwidth of MSM photodetector is always dominated by the drift time of carriers through active region other than detector RC time constant. In other words, the bandwidth of MSM photodetector can be easily enhanced by scaling the metal contact spacing which is the carrier drift distance.

Fig. 1.5 and 1.6 also indicate that conventional MSM photodetectors can only work in photoconductive mode because bias provides the electrical field needed for carrier drift. The applied bias makes the standby power consumption of MSM photodetectors unavoidable. Therefore, minimizing the required bias is necessary for MSM detector application. In Chapter 5 of this thesis, photovoltaic mode large bandwidth MGM photodetectors will be demonstrated using proposed novel technique.

## 1.5 Germanium MOSFET

### 1.5.1 Approaches to improve MOSFET performance

MOSFET is the majority component in modern Si-based IC. Therefore,

MOSFET performance is a crucial factor to the whole circuit. In the past four decades, intensive researches had been carried out for MOSFET performance enhancement. MOSFET is a switch device which is controlled by its gate terminal (Fig. 1.7). The carriers flow from source to drain forms a current when device is on ($I_{on}$). The current in off status is called $I_{off}$ which should be as low as possible. Table 1.1 shows some performance parameters for high performance (HP) logic which are targeted in the International Technology Roadmap of Semiconductor (ITRS) 2007 [1.28]. It can be observed that the drive current ($I_{on}$) is required to be increased continuously every year. MOSFET drive current in saturation region can be expressed by a simple equation:

$$I_{d,sat} = \frac{W}{2L}\mu_{\text{eff}} C_{inv}(V_G - V_{th})^2 \tag{1.3}$$

where W is the channel width, L is the channel length, $\mu_{eff}$ is channel carrier mobility and $C_{inv}$ is the gate capacitance density when the channel is in the inversion condition. One effective approach to increase $I_{on}$ is to scale down transistor gate length. This

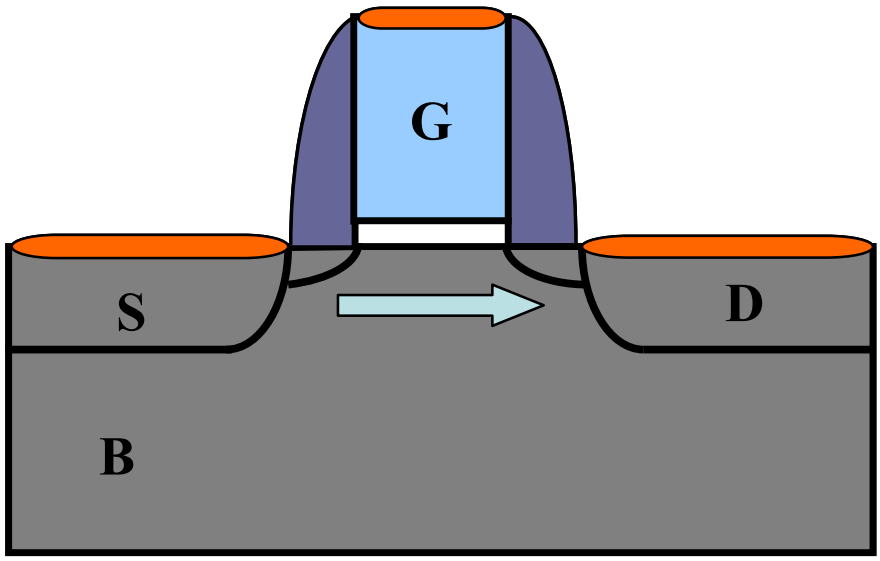


**Fig. 1.7 Schematic of a typical MOSFET structure in the modern VLSI circuits. The current between source (S) and drain (D) through channel is controlled by the gate voltage applied.**

**Table 1.1 Long-term years requirement of High-performance Logic Technology in ITRS [1.28].**

| | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 |
|---|---|---|---|---|---|---|
| ***Physical Gate length (nm)*** | ***25*** | ***22*** | ***20*** | ***18*** | ***16*** | ***14*** |
| ***Electrical Equivalent Oxide Thickness* (Å)** | **18.4** | **12.1** | **10.4** | **9.3** | **8.2** | **7.6** |
| ***Maximum gate leakage current density* (A/cm2)** | **8.00E+2** | **9.09E+2** | **1.00E+3** | **1.11E+3** | **1.25E+3** | **1.43E+3** |
| ***Off-State Leakage Current* (μ A/μ m)** | **0.34** | **0.71** | **0.70** | **0.64** | **0.74** | **0.68** |
| ***NMOS Drive Current* (μ A/μ m)** | **1211** | **1513** | **1639** | **1807** | **1824** | **1762** |
| ***Mobility enhancement factor*** | **1.8** | **1.8** | **1.8** | **1.8** | **1.8** | **1.8** |

approach has been adopted by industry for many years. Table 1.1 also indicates that the MOSFET gate length needs to be further scaled down in the future. However, the continuous scaling down of MOSFET will lead to the undesirable short channel effect. Enhancing channel carrier mobility is another effective approach to increase the $I_{on}$ directly. According to the roadmap, channel mobility needs a 1.8 times enhancement. Although strain engineering effectively enhances the mobility [1.29], the improvement is still lower than roadmap requirement. Since carrier mobility is a material property, applying an alternative high mobility channel material other than silicon is a direct approach to achieve high channel mobility. Germanium is one of the promising candidates for replacing silicon as channel material because it offers 2.8 times electron-mobility and 4 times hole-mobility over Si. Therefore, recently Ge MOSFET attracts more and more research attention.

## 1.5.2 Ge MOSFET with high-κ gate dielectrics

Historically, Ge was widely studied as the first semiconductor material. It is interesting that the first MOSFET in the world is made of Ge rather than Si. The development of Ge MOSFET was hindered by the lack of stable native oxide compared to Si [1.30]. The outstanding properties of $SiO_2$ have enabled the vertical scaling of Si based MOSFET for several decades. However, when $SiO_2$ thickness is less than 2 nm, the direct tunneling current through thin $SiO_2$ becomes significant and rises exponentially [1.31]. According to Table 1.1, $SiO_2$ needs to be scaled down to 6-7 Å to meet the ITRS requirement of HP application. This has become one of major issues for MOSFET performance enhancement. Using high dielectric constant (κ) dielectrics to replace $SiO_2$ would be a solution to enable the further scaling of the gate stack in MOSFET. The advantage of high-κ gate dielectrics over $SiO_2$ is to provide a larger physical thickness for leakage current reduction while improving the gate capacitance due to its higher permittivity. An appropriate high-κ material for MOSFET dielectric application should meet some essential requirements. For all the high-κ materials, the first requirement is good thermal stability during CMOS processing. The interface between high-κ dielectric and substrate plays a dominant role in determining overall electrical performance. Most high-κ materials have an unstable interface with Si and react with Si during high temperature process. The reaction will form an undesirable interfacial layer such as $SiO_2$ which degrades the dielectric equivalent oxide thickness (EOT) and reduces the benefit of high-κ material.

High dielectric constant, as its major advantage, is an essential criterion for high-κ material selection. High dielectric constant value will provide lower EOT and higher capacitance with the same physical thickness. With the scaling of dielectric physical thickness, direct tunneling becomes the dominant mechanism of gate

leakage current. The leakage current from gate to substrate can be expressed as:

$$J = \frac{C}{t_{ox}^{2}} \exp[-2t_{ox}\sqrt{\frac{2m^{*}q}{\hbar^{2}}(\phi_{B} - \frac{V_{ox}}{2})}] \quad (1.4)$$

where C is a constant, $t_{ox}$ is gate oxide physical thickness, m* is the electron effective mass and $\Phi_B$ is electron barrier height from gate work function to oxide layer. The tunneling current will increase exponentially if the physical thickness $t_{ox}$ and barrier height $\Phi_B$ is reduced. Therefore, except for physical thickness, $\Phi_B$ is also a crucial factor for gate leakage current control. Fig.1.8 shows the conduction and valence band offset comparison for some high-κ dielectric candidates which were proposed by Yeo et al [1.32]. It was concluded that $HfO_2$ is the most promising high-k dielectric material among the materials listed.

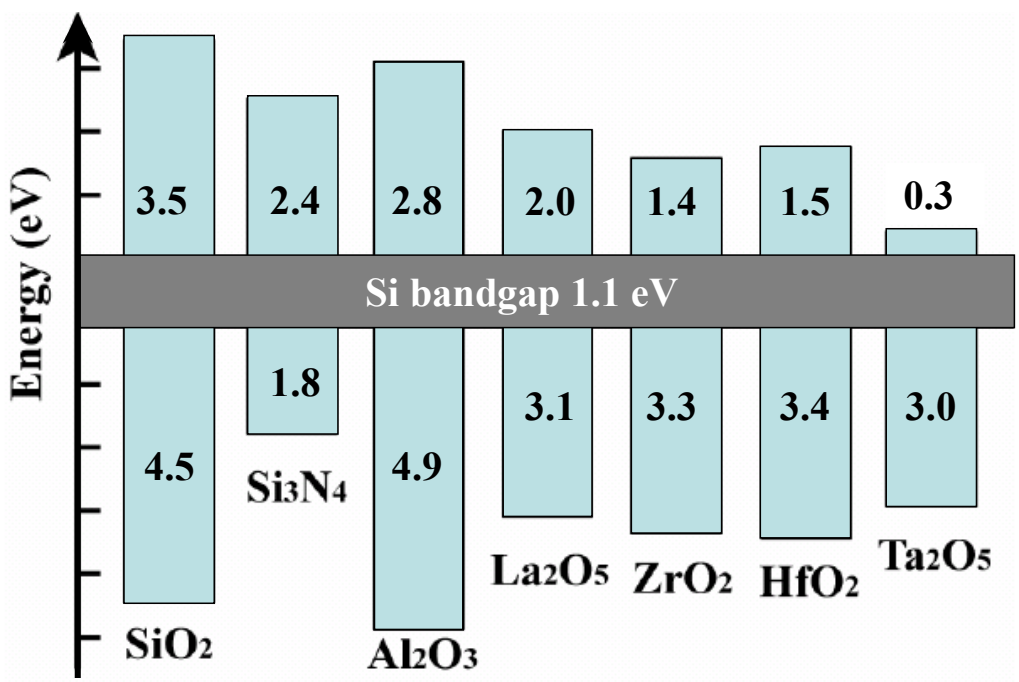


**Figure 1.8 Conduction band offset and valence band offset with respect to Si band gap of selected high-κ dielectrics compared to that of silicon oxide ($SiO_2$) [1.32].**

## 1.6 Integration of Ge Photodetector and Ge MOSFET

High-κ dielectric technology made a breakthrough for Ge MOSFET since high-κ material can replace germanium native oxide as dielectric layer. Ge channel MOSFET incorporating high-κ gate dielectrics is a very promising solution to meet the ITRS requirements since it offers both high carrier mobility and improved gate capacitance without gate leakage degradation. Ge MOSFETs with high-κ dielectric and metal gate were successfully demonstrated by many research groups [1.20][1.21][1.33][1.34].

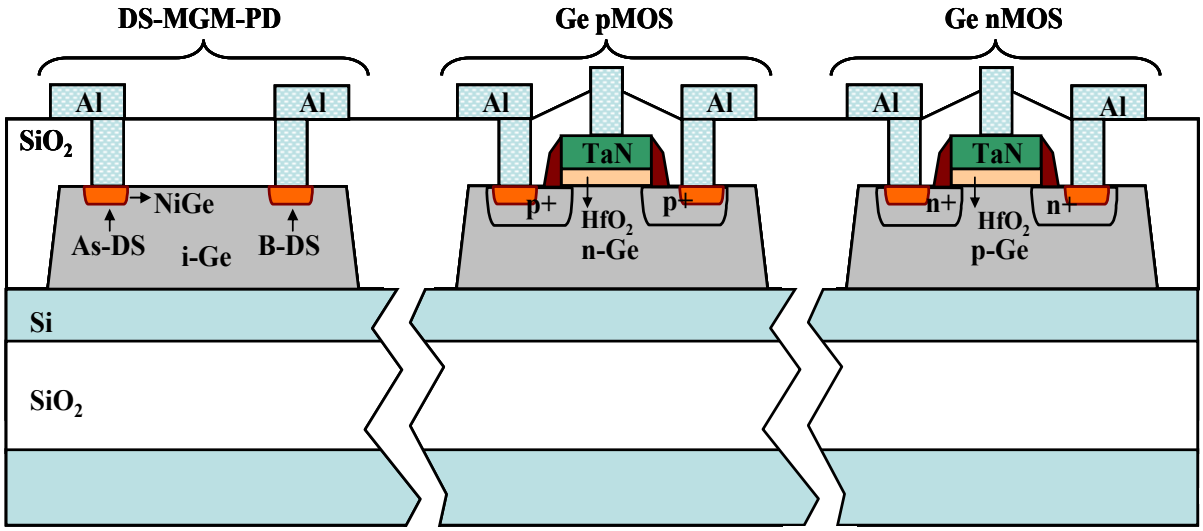


**Fig. 1.9 Integration scheme of Ge photodetector and Ge CMOSFET.**

While previous Ge-channel transistors were predominantly on Ge bulk wafers, integration of Ge transistor into Si substrate is highly desirable for future VLSI. In addition, as discussed previously, Ge is a promising material candidate for near infrared photodetector. It will be very interesting to integrate Ge MOSFET on Si substrate using the same epi-growth technique as Ge photodetector fabrication. Fig. 1.9 shows the schematic of proposed Ge MOSFET integration with Ge photodetector.

The Ge platform for both MOSFET and photodetectors can be achieved by selective Ge epi-growth in patterned window. The proposed integration scheme shows many advantages. First, the IC based on MOSFET performance was improved. Secondly, the high thermal budget process of Si MOSFET is a serious issue for integration of Ge photodetectors and Si MOSFETs. Ge MOSFET integration on Si substrate provides a solution for this issue and simplifies the integration of Ge photodetectors and MOSFET logic.

## 1.7 Thesis Outline

This thesis mainly presents the development of MGM-PDs integration on Si substrate in configuration of surface-illumination (SI) and waveguide and its CMOS compatibility. In Chapter 2, Ge epi-growth on Si substrate using UHV-CVD was investigated to provide the platform for Ge PDs integration. In Chapter 3, a novel dark current suppression method for MGM-PD was proposed and studied. In Chapter 4, high-speed SI-MGM-PD was fabricated and fully characterized. In Chapter 5, MGM-PD with scaled contact spacing integrated with SOI waveguide was demonstrated to achieve large bandwidth and high responsivity simultaneously. In Chapter 6, we will demonstrate Ge CMOSFET integration on Si substrate for future OEIC application.

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# Chapter 2
# Germanium Epi-growth on Si Substrate

## 2.1 Literature review

As discussed in Chapter 1, high-quality Ge growth on Si substrate is one of the challenges to realize Ge photodetector integration on Si. Ge layer quality is directly related to photodetector performances such as quantum efficiency and dark current. The major challenge in Ge epi-growth on Si substrate is the 4 % lattice mismatch between Ge and Si substrate. The lattice mismatch causes two issues: 1) high surface roughness due to island growth and 2) high density of misfit-dislocations and threading dislocations in the epi-layer.

First, due to the large lattice mismatch, the critical thickness of Ge on Si substrate is about 2 nm. During Ge growth, the accumulated deformation energy during heteroepitaxial growth can be partially relieved by forming three-dimensional islands because the energy reduction associated with elastic relaxation exceeds the increase in surface energy [2.1]. Therefore, Ge islands rather than continuous film are formed. Island formation seriously hinders the Ge photodetectors integration on Si substrate. Besides, misfit dislocations appear to relax the lattice stress between Ge layer and Si substrate by introducing extra half planes of atoms. Misfit dislocations are mainly confined between the interface of Ge epi-layer and Si substrate. Threading dislocations are the by-products of misfit dislocations. Threading dislocations in Ge layer cannot end in crystal and have to form a loop or terminate at a free surface. The

epi-layer surface is the nearest free surface to Ge/Si interface. Therefore, threading dislocations normally spread from Ge/Si interface to the Ge surface [2.2]. Since photodetectors are typically fabricated on the top region of epi-Ge layer, high density threading dislocations significantly degrade detection efficiency, dark current and reliability. Therefore, high-quality Ge layer on Si substrate becomes the first bottleneck for Ge photodetectors integration on Si substrate.

To overcome the Ge growth issues, extensive research activities were carried out. Colace et al. found that poly-Ge on Si substrate is a solution for the limited critical thickness issue of epi-Ge on Si [2.3][2.4][2.5]. Poly-Ge/Si hetero-junction photodiodes were fabricated with near-infrared range detection. However, the presence of high-density defects and the small active region (depletion width plus diffusion length) of poly-Ge layer severely limit its detection efficiency [2.3][2.4][2.5]. Samavedam et al. integrated Ge photodetectors on Si substrate by UHV-VCD [2.6][2.7]. To avoid island growth, a thick (10 μm) SiGe graded buffer-layer was grown before Ge growth. The Ge concentration in graded SiGe buffer ranges from 50 % to 92 %. To optimize the SiGe graded buffer layer, an intermediate chemical mechanical polishing (CMP) was carried out right after 50 % Ge layer followed by high Ge concentration re-growth. High quality Ge epi-layer was achieved on Si substrate with a threading dislocation density of $2\times10^{6}$ $cm^{-2}$. The photodetectors fabricated based on this epi-growth technique show a quantum efficiency of 12.6 % at wavelength of 1300 nm and a dark current density of 0.22 $mA/cm^{2}$ at -1 V. In this work, the 10 μm graded SiGe buffer is the key point to realize

Ge diodes on Si substrate. If the Ge epi-layer can be grown directly on Si without the thick buffer layer, the fabrication process can be much simplified, and also the process cost can be reduced. Colace et al. proposed and demonstrated a novel Ge epi-growth method called two-step CVD process [2.8] [2.9] [2.10]. First, a low- temperature (350 °C) Ge buffer layer of 50 nm is grown to prevent the island growth. The low temperature growth was followed by a high temperature (600 °C) Ge growth to reduce the threading dislocation density and increase the growth rate. However, the two-step Ge epi-layer suffers a high threading dislocation density on the order of $10^9$ $cm^{-2}$. The following research of Luan indicates that the threading dislocation density in two-step Ge layer can be significantly reduced by cyclic thermal annealing. The optimized annealing condition (900 °C/10 min, 780 °C/10 min, cycle number: 10) can reduce the threading dislocation density to $2.3\times10^7$ $cm^{-2}$ [2.11][2.12]. Ge photodetectors based on this process were successfully demonstrated with improved performance [2.11] [2.13]. The disadvantage of the cyclic annealing process is the increase of the thermal budge needed in device fabrication. The high thermal budget is undesirable for photodetectors integration with conventional MOSFET. The Ge epi-growth technique with lower thermal budget is needed for OEIC. In this chapter, we introduce an UHV-CVD growth of high quality Ge on Si substrate using two-step Ge growth method combining with an intermediate thin SiGe buffer layer. The SiGe buffer is grown at low temperature of 350-400 °C and its thickness is about 30 nm. This technique offers the advantage of not needing a thick SiGe graded layer or high thermal budget cyclic annealing step. In addition, selective Ge growth on patterned Si

wafer was also achieved using this technique. It provides a promising solution for large scale integration of Ge photodetectors on Si-based IC.

## 2.2 Experiment

The substrates used are 8 inch p-type Si (001) wafers with resistivity of 6-9 Ωcm. The epi-growth was done on both blanket wafers and patterned wafers with oxide window for selective Ge growth. For $SiO_2$/Si window formation, $SiO_2$ of 120 nm was deposited by plasma enhanced chemical vapor deposition (PECVD) first. After lithography process, plasma etching process is carried out for Ge window opening. The depth of plasma etching is about 110 nm. The remained 10 nm $SiO_2$ was removed by Hydro fluoric (HF) acid (1:100) wet etching to avoid Si surface damage induced by plasma etching.

A single-wafer cold wall ultra-high-vacuum chemical-vapor-deposition epi-reactor (UHV-CVD) was used for Ge heteroepitaxy on Si substrate. The base pressure of the UHV-CVD chamber is $7\times10^{-9}$ Torr. Before epitaxy growth, the wafers were cleaned in [$NH_4OH$: $H_2O_2$: de-ionized (DI) water = 1: 2: 10] for 10 min and HF acid (1:200) for 2 min for native oxide removal, and followed by an ultrasonic drying before loading into growth chamber. After wafer loading, the epi-growth started with an in-situ cleaning at 750 °C to remove residual oxide, and then a Si epi-growth as buffer layer was done at temperature of 570-600 °C. Next, the chamber was cooled down to 350 °C. A growth of thin $Si_{0.75}Ge_{0.25}$ buffer layer with a target thickness of 30 nm was done at low temperature (350-400 °C). While maintaining at constant

temperature, a low temperature Ge seed layer of 30 nm was grown. The gas flow of $GeH_4$ is 10 sccm. Subsequently, a high temperature epitaxy Ge layer was grown at 550-600 °C. The $GeH_4$ gas flow is also 10 sccm. Finally, a Si cap layer of 3 nm was grown on Ge layer at the same temperature. The process pressure during the epitaxial growth is between $10^{-6}$ and $10^{-3}$ Torr. High resolution transmission electron microscopy (HR-TEM) was used to observe the thickness and the quality of the epitaxial layers. The Ge surface morphology was analyzed by atomic force microscopy (AFM) and scanning electron microscopy (SEM).

## 2.3 Result and Discussion

To evaluate the two-step Ge growth method, a Ge layer without low-temperature Ge layer was directly grown at the temperature of 550-600 °C as a reference sample. Fig 2.1 and 2.2 show the SEM and HR-TEM image of the Ge epi-layer without a low-temperature Ge layer. It can be seen that not continuous Ge film but Ge islands were formed. Theoretically, due to the 4% lattice mismatch, the critical thickness of pure Ge on Si substrate is less than 2 nm [2.14]. The elastic energy caused by lattice mismatch between epi-Ge layer and Si substrate are the driving forces for the Ge islands growth [2.1][2.6]. It can be observed that the size of the Ge islands is about 100-300 nm. To make a device on Ge layer, a continuous film is required. The Ge island growth by conventional epi-growth method seriously hindered photodetectors integration on Si substrate. Fig. 2.3 and 2.4 show the HR-TEM image of Ge epi-layer on Si substrate using the proposed growth technique.

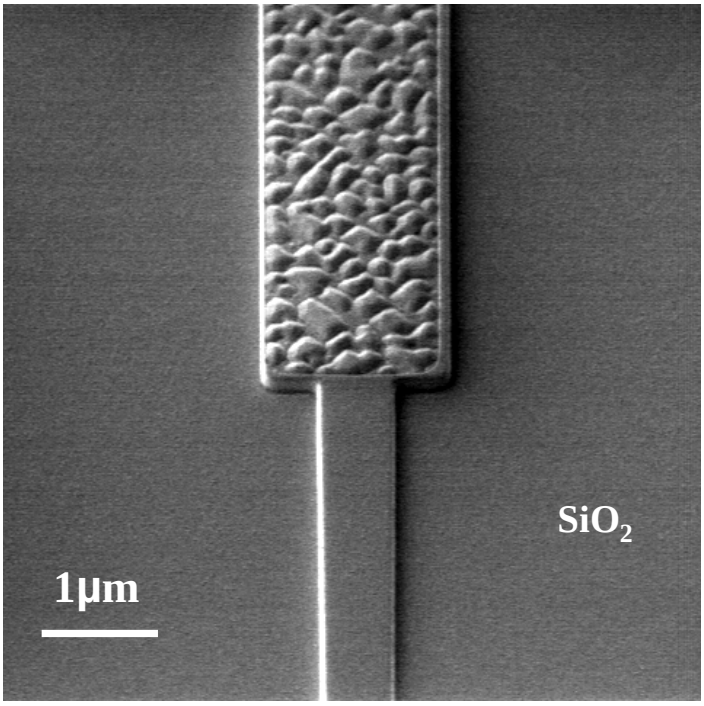


**Fig. 2.1 SEM image of Ge island growth on patterned Si wafer without low temperature buffer layer.**

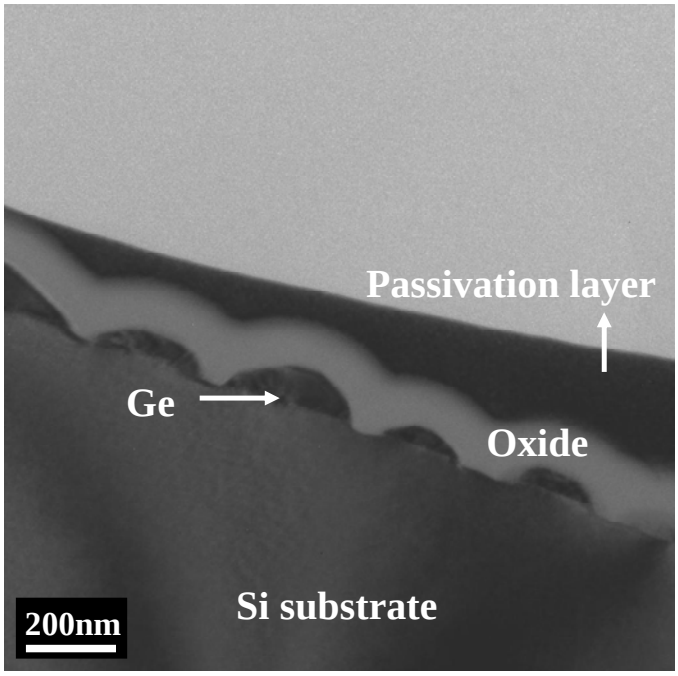


**Fig. 2.2 TEM image of Ge island growth on Si substrate without low temperature buffer layer.**

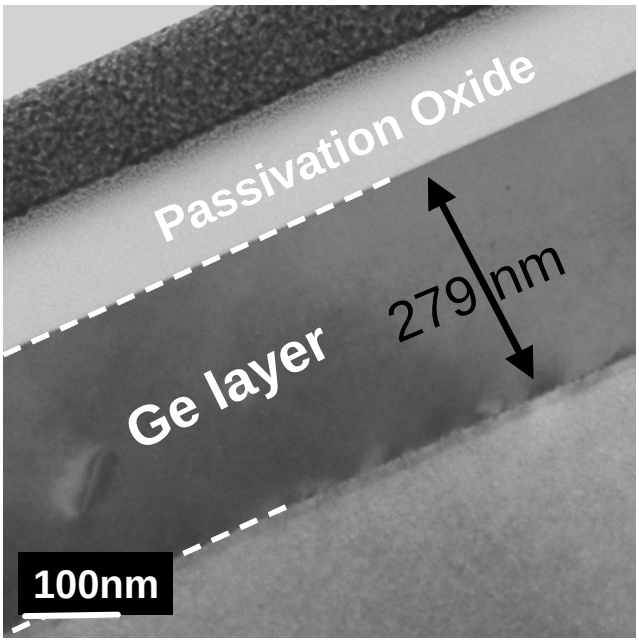


**Fig. 2.3 HR-TEM image of epitaxial Ge layer using two-step Ge growth method combining with an intermediate SiGe buffer layer.**

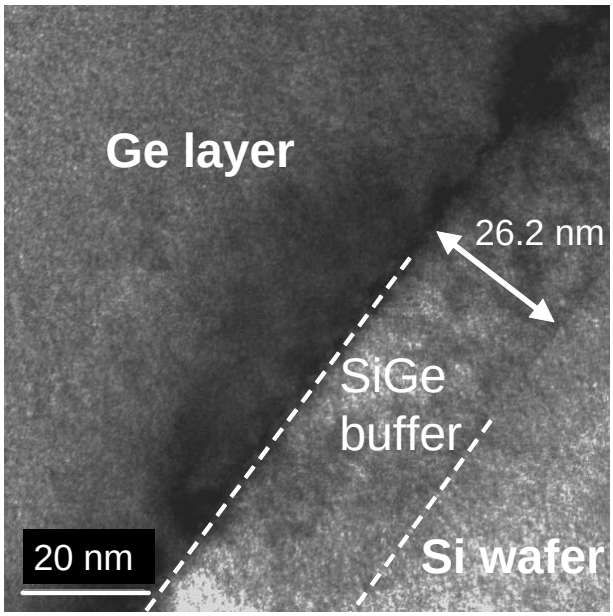


**Fig. 2.4 HR-TEM image of the heterostructure epitaxial layers of Si/ $Si_{0.75}Ge_{0.25}$ /Ge.**

Fig. 2.3 shows the HR-TEM image of Ge epi-layer grown using two-step Ge growth method combining with an intermediate SiGe buffer layer. The image shows that the total thickness of the epitaxial layers is approximately 279 nm. In addition, there was no misfit dislocation propagated through Ge epi-layer. Compared to the Ge island growth process, the key point of this epi-growth process is the low temperature (350-400 °C) Ge seed layer. Due to the surfactant effect of hydrogen at the temperature range of 350-400 °C, the surface of SiGe layer was terminated with H atoms. The nucleation of three-dimensional Ge islands was inhibited and the strain in epi-layer was released through the insertion of misfit dislocations [2.8][2.9][2.10]. When the elastic energy is fully relaxed, Ge growth becomes the homoepitaxial case. In this step, the process temperature was increased up to 550-600 °C. The high temperature growth decreases threading dislocation density and increases Ge growth rate. As a result, all the misfit dislocations were confined in the SiGe/Ge interface and the low temperature Ge seed, and the high temperature Ge above the low temperature seed layer shows very low density of dislocations. The etch pit density experiment was carried out to characterize the threading dislocation density. The Ge epi-layer shows a threading dislocation density of $6\times10^{6}$ $cm^{-2}$ which can be benchmarked with previously published results [2.11][2.12]. Fig. 2.4 shows the HR-TEM image of the heterostructure epitaxial layers of Si/SiGe/Ge. The Ge concentration in the SiGe layer is approximately 25%. The SiGe buffer layer is a buffer layer with point defect. By growing a thin epi-layer below the standard CVD growth temperatures, point defects can be generated in the low temperature layer. The point defects facilitate strain

relaxation by interacting with misfit dislocations [2.15][2.16][2.17]. All the misfit dislocations were confined near the interface of the low temperature Ge seed and the SiGe buffer layer.

The Ge epi-layer is developed for both photodetectors and MOSFETs fabrication. For MOSFETs, the surface roughness of Ge epi-layer is very important since the surface acts as the interface between channel and dielectric layer and affects the MOSFET performance directly. Fig. 2.5 shows an AFM image of grown Ge surface on an area of 10 μm × 10 μm. The AFM image indicates that the roughness root mean square (RMS) of the surface is only 4 Å. In addition, no cross-hatch pattern was observed. From the TEM and AFM images, it can be concluded that a high-quality Ge layer with smooth surface and a low threading dislocation density can be achieved using the two-step growth method combining with a low temperature SiGe buffer layer by UHV-VCD.

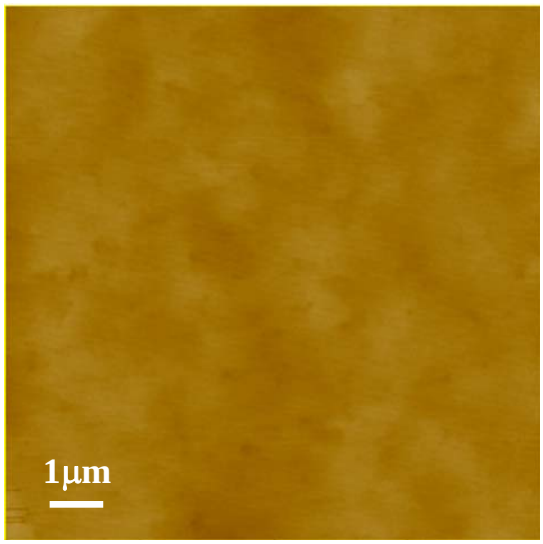


**Fig. 2.5 AFM image of grown Ge surface on 10 μm × 10 μm pad. Ge surface shows a roughness RMS of 4Å.**

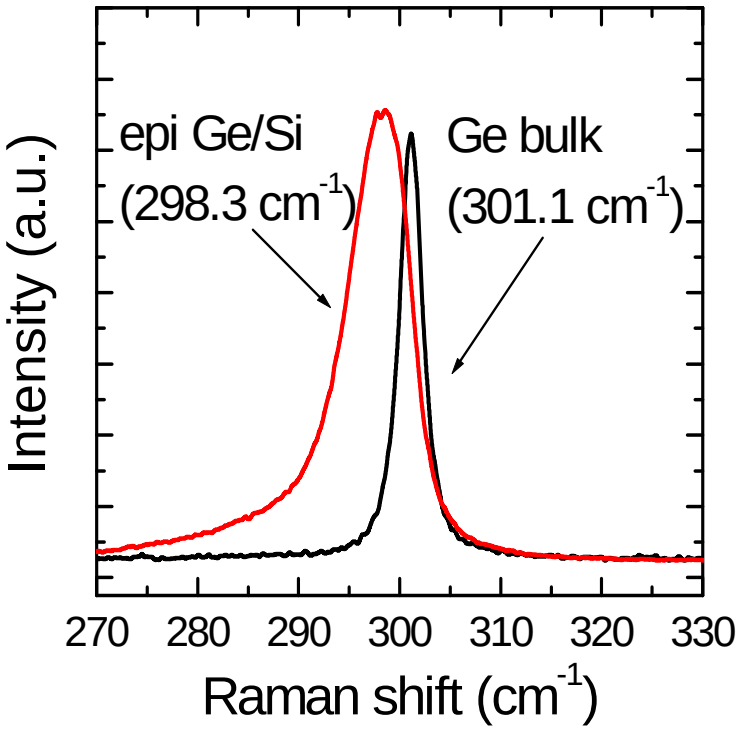


**Fig. 2.6 Raman spectra for epi-Ge on Si wafer and Ge bulk wafer.**

Fig. 2.6 shows the Raman spectra from the Ge epi-layer and a bulk Ge wafer. The 2.8 $cm^{-1}$ shift of the epi-Ge peak relative to the Ge bulk peak indicates that the epi-Ge layer experiences a tensile strain. The in-plane tensile strain $\varepsilon$ can be calculated from the strain versus phonon peak shift relationship $\Delta\omega=b\varepsilon$. By using parameters b=−415 $cm^{-1}$ from [2.18], a tensile strain of 0.67% is obtained. The tensile strain in the Ge layer is due to its higher thermal coefficient of expansion (TCE) as compared to Si. During cooling down after the high-temperature Ge growth, Ge lattice shrinkage was suppressed by the Si substrate, resulting in a tensile strain in the Ge layer. Similar tensile-strained Ge grown by MBE due to TCE mismatch mechanism had been previously reported [2.19][2.20].

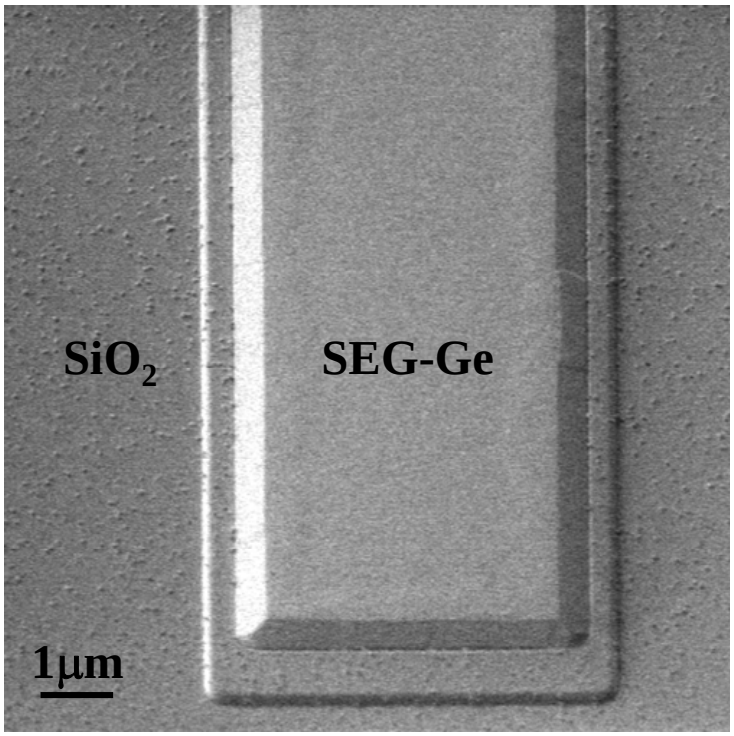


**Fig. 2.7 SEM image of the selective Ge epitaxial layer on Si wafer.**

Selective Ge growth on patterned $SiO_2$/Si wafer was also achieved by the same epi-growth method. Fig.2.7 shows the SEM image of selective grown epitaxial Ge layer on a patterned wafer. It can be seen that the Ge layer shows a smooth surface. It also can be observed that Ge layer was only grown on the patterned Si window region, and there is no Ge growth on the $SiO_2$ region. The main reason of this selective Ge growth is that the reaction between $GeH_4$ and $SiO_2$ growth forms volatile GeO and retards the nucleation of poly Ge on $SiO_2$. Fig. 2.8 shows the HR-TEM image of selective Ge epitaxial layer on SOI wafer. Similarly, selective-growth Ge layer shows a good quality and no misfit dislocation propagates through Ge layer. Meanwhile, the facets can be seen clearly on the edge of Ge mesas. The three kinds of facets on the edge are identified to be (311), (111) and (113) [2.19]. The facets play the role

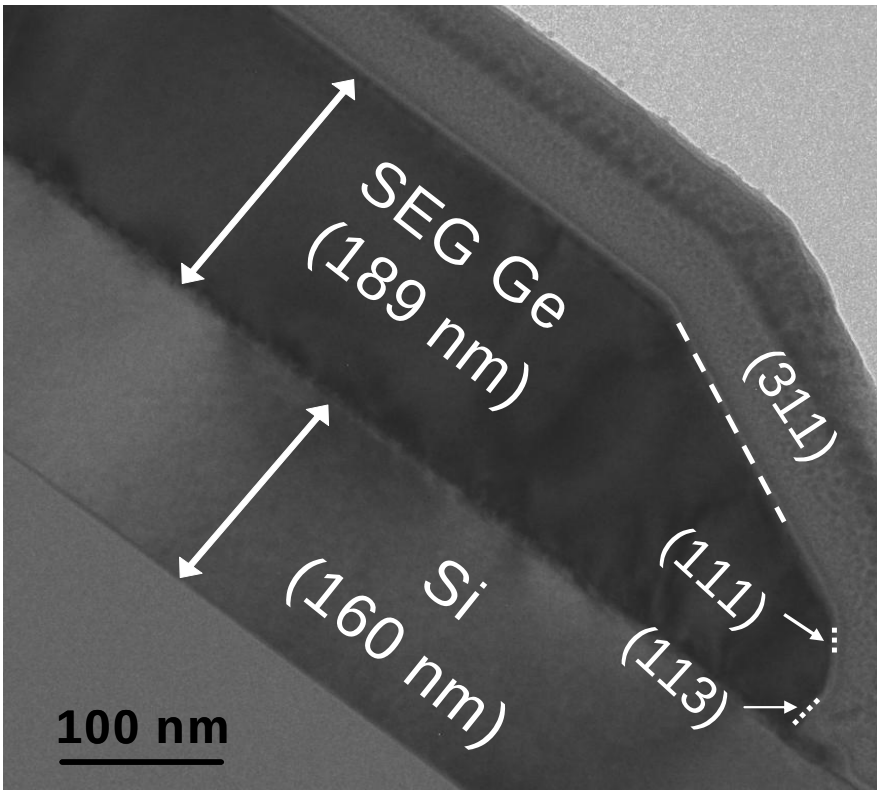


**Fig. 2.8 HR-TEM image of the selective Ge epitaxial layer on SOI wafer.**

of strain relaxation during selective Ge growth. With the demonstration of selective Ge growth, the platform for Ge photodetectors and Ge MOSFETs is well prepared. In the following chapters, devices based on this Ge growth technique will be demonstrated and studied.

## 2.4 Conclusions

High-quality thick Ge layer on Si substrate was successfully demonstrated using two-step Ge growth method combining with a low temperature ultrathin SiGe buffer layer prior to Ge epitaxy growth by UHV-CVD. Ge epi-layer grown shows a low

threading dislocation density of $6\times10^{6}$ $cm^{-2}$ and a low roughness RMS value of 0.4 nm. Selective Ge growth on patterned $SiO_2$/Si wafer was also demonstrated which provided a high-quality platform for large scale Ge photodetectors integration on Si substrate.

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# Chapter 3
# Application of dopant segregation to metal-germanium-metal photodetector and its dark current suppression mechanism

## 3.1 Literature Review

As one of the attractive photodetector configurations, MGM photodetector offers the advantages of ease of fabrication process, low capacitance and high bandwidth. With the success of epitaxy growth of high quality thick Ge layer on Si substrate, several MGM photodetectors had been already demonstrated [3.1][3.2][3.3]. However, the high dark current of MGM photodetector poses additional standby power dissipation as an increasingly serious issue especially in today's ultra-large scale integrated chip. Due to the symmetrical structure of MGM photodetector, it can only work in photoconductive mode for large bandwidth and high responsivity operation, which makes the high dark current issue unavoidable.

There are two major components of the dark current in MGM photodetectors: 1) the current over the Schottky barrier, 2) and the current associated with the thermally generated electron-hole pairs. In MGM photodetectors, SBH scaling due to the narrow band gap and the strong Femi-level pinning of metal/Ge interface at valence band is the major reason of its high dark current [3.4][3.5]. Regarding this issue, different techniques were proposed for dark current suppression. Okyay investigated the effect of varying electrode area asymmetry on the leakage behavior of MSM photodetectors

[3.6]. With the identical total electrode area and spacing, but varying the contact area asymmetry through minimizing the area of high leakage current electrode and increasing the area of low leakage current electrode, 50% reduction in dark current was obtained in MSM photodetector. In addition, choice of metal for electrodes is another factor affecting dark current. Okyay also found out that MGM photodetectors using Cr or Ti as electrodes materials show ~50% lower dark current compared to the one with Ni electrodes [3.3]. The result indicates that using a metal with work function close to Ge mid-gap as electrode material is another approach to decrease the dark current of MGM photodetector. Similar result was reported in [3.7]. However, by varying electrode material and applying asymmetric area electrodes, the dark current suppression is still less than one order of magnitude, which is far from the requirement of modern low-power circuit. Oh proposed and demonstrated a MGM photodetector with amorphous Ge layers below metal electrode for dark current suppression [3.8]. The inserted amorphous Ge layer was used to increase the SBH between epi-Ge layer and metal electrode, resulting in a dark current reduction up to more than two orders of magnitude. The exciting report indicates that SBH modulation is a promising solution for dark current suppression in MGM photodetector.

Dopant segregation proposed by Thornton is a technique for SBH modulation between metal and semiconductor material [3.9]. The concept of dopant segregation technique in the case of Si as semiconductor material is schematically explained in Fig.3.1. Before metal deposition, a low energy implantation is carried out.

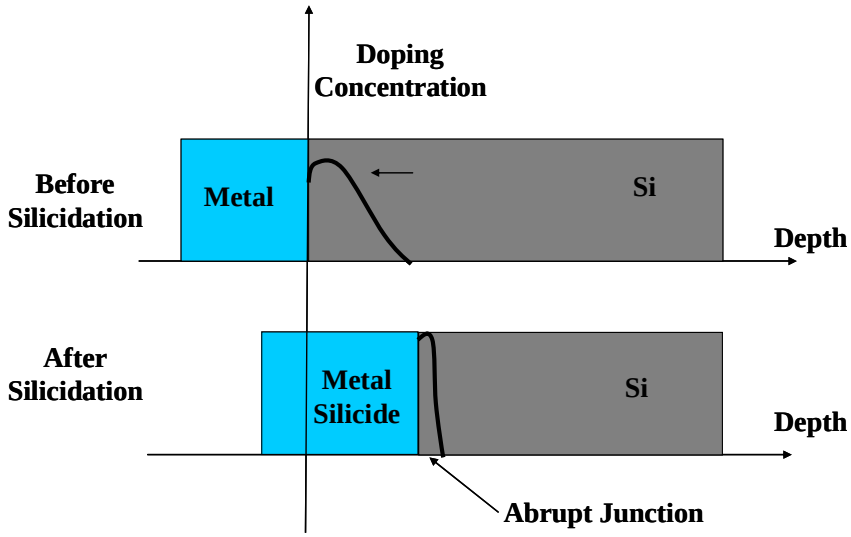



**Fig. 3.1 Schematic of dopant segregation technique on Si substrate.**

After activation, a shallow doping region is formed. Next, metal such as Ni or Co was deposited on Si. During rapid thermal annealing (RTA), the doped region is fully consumed by silicidation. Due to dopant redistribution, the dopant is piled up at the metal silicide interface. The piled-up dopant profile near metal silicide interface is steeper with a higher peak concentration than the dopant profile before silicidation. Therefore, a metal-semiconductor junction with high doping concentration of sharp profile is formed. The SBH between metal and silicon is modulated to be larger or smaller depending on the type of dopant applied. Recently, dopant segregation was applied in MOSFET gate stack engineering to adjust the work function of NiSi gates. NiSi effective work-function control over 0.3eV was achieved with P, As, and Sb used as gate impurities [3.10]. Meanwhile, dopant segregation during silicidation technique had been successfully introduced into SB-MOSFETs by Kitashino, with demonstration of a significant improvement in drivability and short channel effect

immunity [3.11]. Dopant segregation SB-MOSFET was also investigated by Zhang [3.12]. In [3.11][3.12][3.13], dopant segregation technique is used to reduce effective SBH between metal source and channel, resulting in drivability enhancement. Fig. 3.2 shows the schematic band diagram in SB-MOSFET device with dopant segregation [3.12]. The black and grey lines stand for the band diagrams with and without gate bias respectively. The n-type dopant (As) is used in n-FET (Fig. 3.2 a), and the As segregated near the NiSi interface induces a band diagram downward bending. The band bending reduces the effective electron SBH from source to channel and facilities the electron tunneling. Simultaneously, the effective hole SBH from drain to channel is enhanced and the off-state leakage current is suppressed. In p-FET (Fig. 3.2 b), the upward band bending induced by B segregation facilities the hole tunneling from source to channel and decreases the electron injection in drain side.

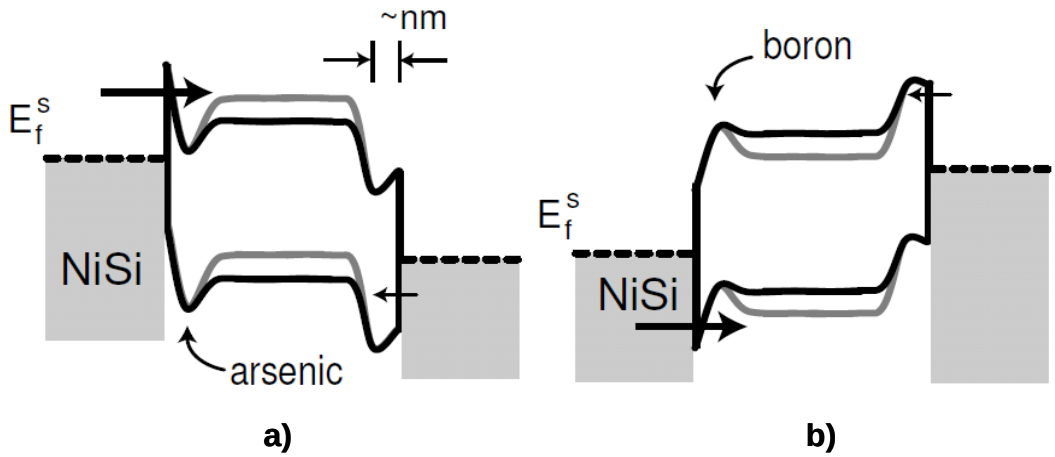


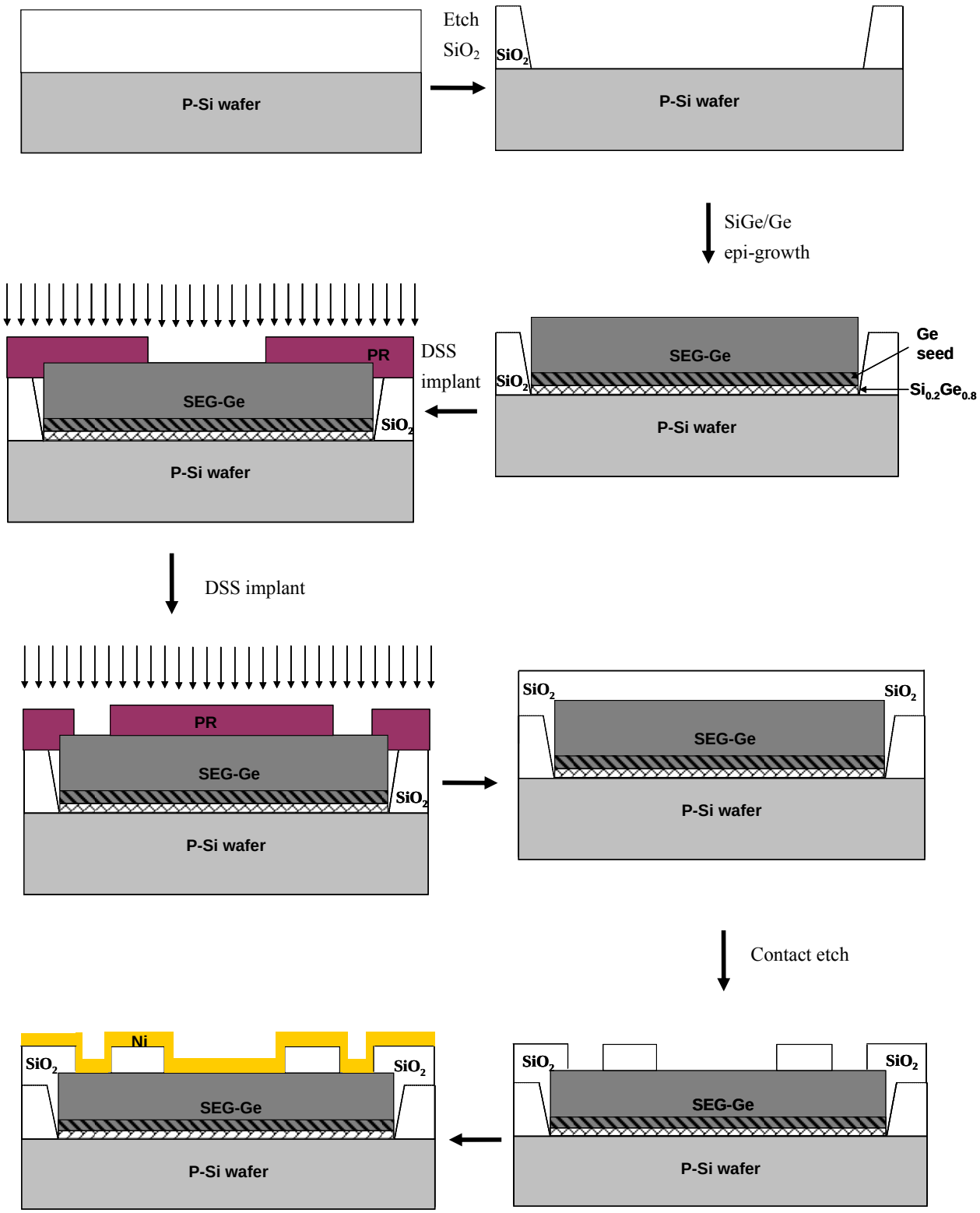

**Fig. 3.2 Schematic conduction and valence band profile in SB-MOSFET devices with dopant segregation at two different gate voltages. (a) shows the n-type device with arsenic segregation. (b) shows the p-type device with boron segregation [3.12].**

In this chapter, we propose and investigate the application of dopant segregation technique in MGM photodetectors for dark current suppression. Along with the

discussion on the dark current suppression mechanism, the effects of different dopant segregation strategies on the electrical and optical behaviors of photodetectors are investigated.

## 3.2 Experiment

Devices were fabricated on 8" p-type Si (100) wafers. Fig. 3.3 shows the device fabrication flow. First, $SiO_2$ of 120 nm was deposited by PECVD, and then detector region was defined by lithography. For opening Ge growth windows, $SiO_2$ in window regions was partially etched using reactive ion etching (RIE) process. The remaining oxide was removed by HF acid (1: 100) to avoid Si surface damage induced by RIE process. After a standard cleaning, a high-quality Ge epi-layer of ~300 nm was grown by the two-step growth method combining with an intermediate ultrathin SiGe buffer (30 nm) in UHV-CVD. The process was described in details in Chapter 2. For dopant segregated metal contact formation, the epi-Ge was patterned to define ion implantation area. The designed photodetector is a ring structure with two metal contacts which are named as inner electrode and outer electrode respectively. Devices were patterned and implanted for inner electrodes region first. After photo resist (PR) strip and wafers cleaning, another cycle of lithography and implantation was done in the outer electrodes region. To obtain the optimal dopant segregation scheme for MGM photodetector, four splits were designed and fabricated. The splits details are listed in Table 3.1. The splits are named with abbreviation for discussion convenience. For the np-DS configuration, the outer electrode was implanted with B,


P-Si wafer
Etch
SiO2
SiO2
P-Si wafer
SiGe/Ge
epi-growth
SEG-Ge
Ge
seed
SiO2
Si0.2Ge0.8
P-Si wafer
PR
DSS
implant
SEG-Ge
SiO2
P-Si wafer
DSS implant
PR
SEG-Ge
SiO2
P-Si wafer
SiO2
SiO2
SEG-Ge
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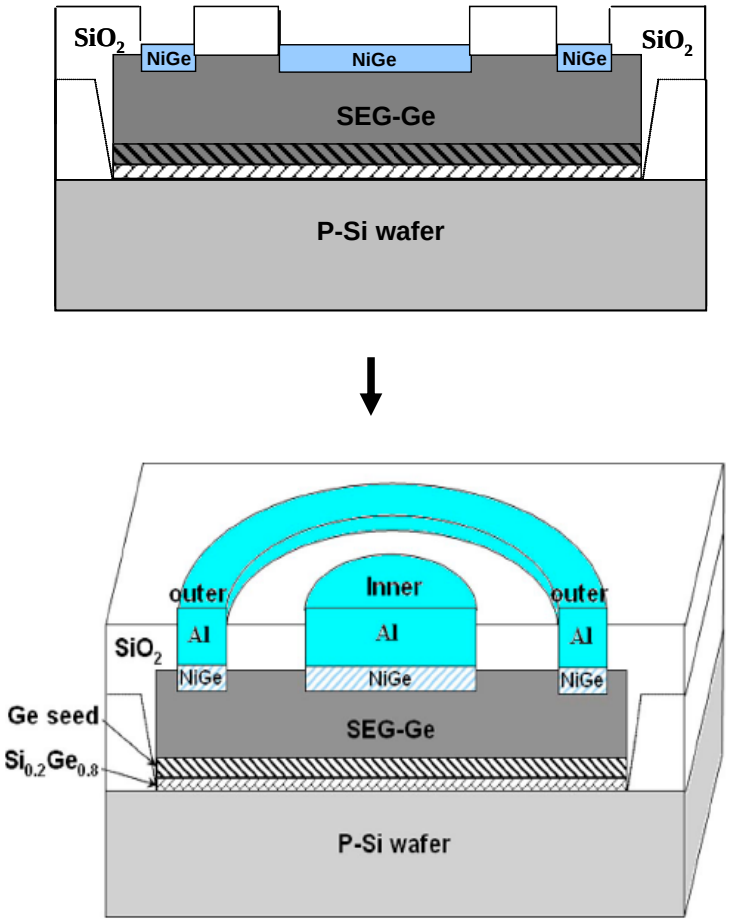



**Fig. 3.3 Schematic of MGM photodetector fabrication process flow.**

**Table 3.1. The splits of dopant segregation scheme in MGM photodetectors.**

| Structure | Inner electrode | Outer electrode | Abbreviation |
|---|---|---|---|
| NiGe-Ge-NiGe | No DS | No DS | without DS |
| NiGe-Ge-NiGe | boron DS | boron DS | pp-DS |
| NiGe-Ge-NiGe | arsenic DS | boron DS | np-DS |
| NiGe-Ge-NiGe | arsenic DS | arsenic DS | nn-DS |

while the inner electrode was implanted with As. For n-type dopant, the Arsenic dose is $1\times10^{15}$ $cm^{-2}$ and the implantation energy is 12 keV. For p-type dopant, $BF_2$ was used as implant species for shallow doping depth. The implanted dose is $1\times10^{15}$ $cm^{-2}$ and the energy is 12 keV. The four segregation schemes for MGM photodetectors were designed and fabricated on the same wafer for fair comparison. After implantation, PR was striped and wafers were cleaned for polymer removal. After $SiO_2$ (320 nm) deposition by PECVD, the wafers were patterned again for contact holes formation. Contact holes etching was done by RIE process first followed by wet etching. It should be noted that dry and wet etching are both necessary for this step. For MOSFET contact hole $SiO_2$ etching, RIE is used and controlled by end point mode with about 10 nm Si loss. However, the photodetector contact holes in this work were opened to form dopant segregation NiGe contacts. A shallow implantation at low energy was done in contact regions. Over-etching can induce dopants loss in Ge surface region. Therefore, wet etching is necessary after partial dry etching (280 nm). In addition, if skipping RIE process, a longer time wet etching for contact opening will lead to the contact hole size widening due to the isotropic properties of wet etching. The contact widening to non-implanted region will lead to a failure of dopant segregation contact formation and lose the benefit of dopant segregation contact. Therefore, partial RIE followed by wet etching is the optimal process for contact holes formation. Next, 25 nm Ni was deposited by sputtering for DS-NiGe electrodes formation. Germanidation was carried out by rapid thermal annealing (RTA) at 350 ˚C for 30 sec. The un-reacted Ni was removed by Nitric acid (15 %). The etching time is about 2 min. After wafer cleaning

and drying, TaN (20 nm) / Al (600 nm) contact stack was deposited by sputtering. Finally, the wafer was patterned again and etched for metallization.

## 3.3 Results and Discussion

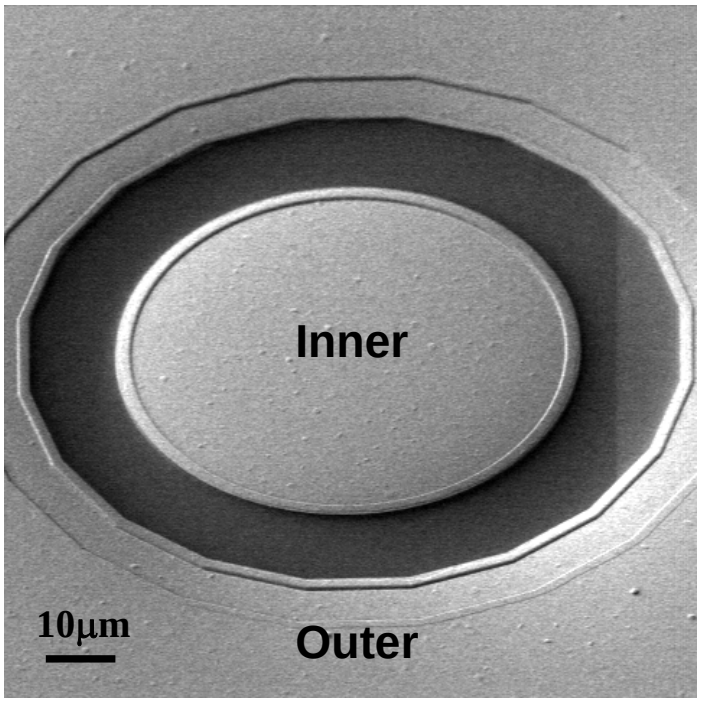



**Fig. 3.4 SEM image of a fabricated MGM photodetector**

Fig. 3.4 shows the SEM image of a fabricated MGM photodetector. The detectors were designed to be round shape with two metal contacts. The spacing between two electrodes is 17 μm. The width of the inner and the outer electrodes is 205 μm and 315 μm respectively. The inner and outer electrodes are both big enough for direct probing. It should be noted that the photodetectors fabricated in this chapter are only for dark current suppression mechanism study. The device size is too big for high

speed operation. The scaled device with new structure for responsivity and bandwidth extraction will be demonstrated and characterized in next chapter.

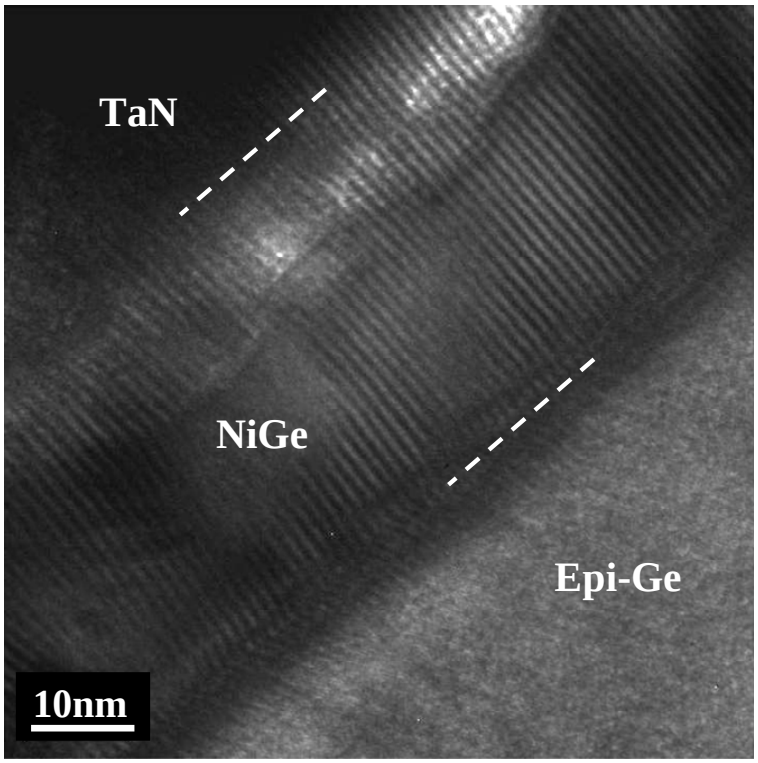
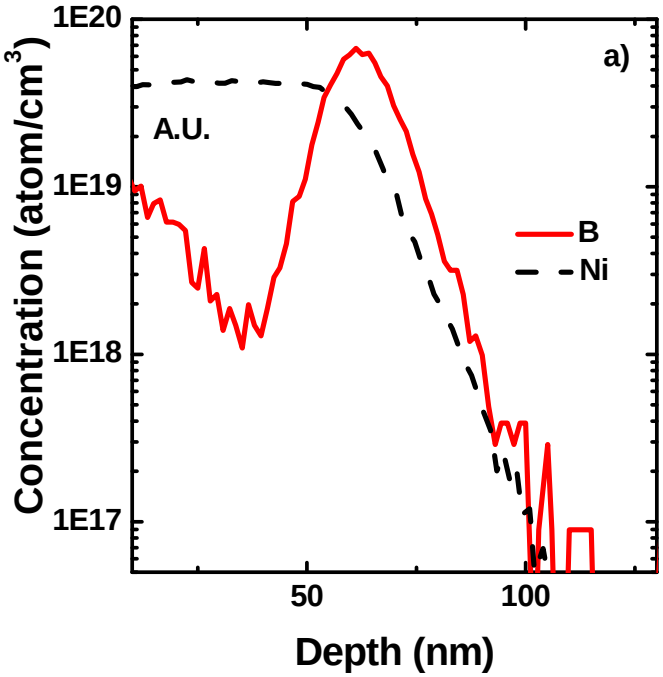



**Fig. 3.5 HR-TEM image of the layers of NiGe/epi-Ge.**

Fig. 3.5 shows a HR-TEM image of the Ni-Germanide layer formed on epi-Ge layer. Energy dispersive X-ray spectroscopy (EDX) analysis on the Ni-germanide shows formation of mono-nickel germanide (NiGe) which has been reported to show low resistivity of 15 μΩcm [3.14]. It is observed that the NiGe forms a sharp and smooth interface and exhibits epitaxial growth. The epitaxial growth is due to the low lattice mismatch between NiGe and Ge [3.15]. In the HR-TEM image, it can be seen that low-resistance NiGe contact was well formed on epi-Ge layer.



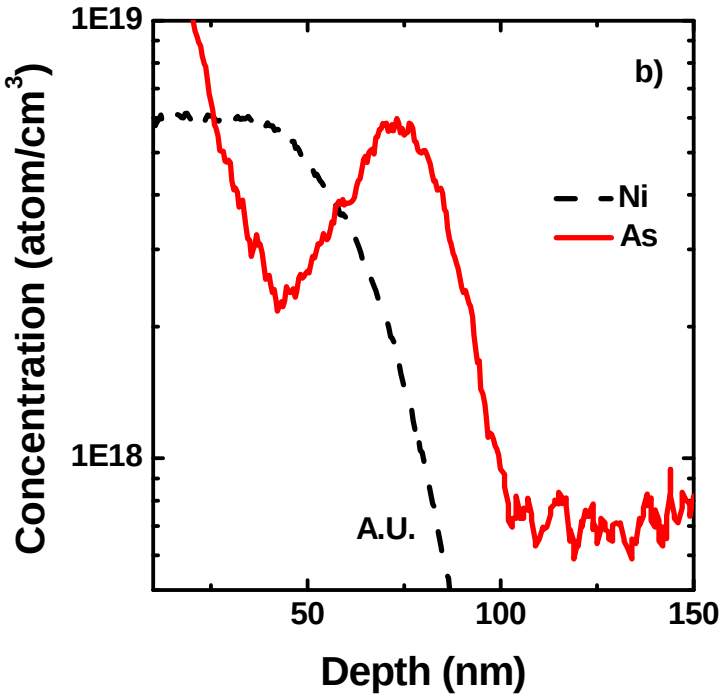




**Fig. 3.6 (a) SIMS profiles of B in NiGe/Ge Schottky diode. (b) SIMS profiles of As in NiGe/Ge Schottky diode. Ni is in arbitrary unit (A.U.).**

Most of previous reports about dopant segregation application were demonstrated on Si substrate [3.11][3.12][3.13]. To examine the dopant segregation effect in germanium, secondary ion mass spectrometry (SIMS) was employed to evaluate the dopant segregation effect in germanium substrate. From the SIMS depth profiles of As and B in NiGe/Ge interfaces (Fig. 3.6), it was observed that both As and B atoms were segregated around the interfaces of NiGe/Ge. The doping peak concentration is ~ 6 x $10^{18}$ $cm^{-3}$ for As and ~7 x $10^{19}$ $cm^{-3}$ for B. The implanted region was fully consumed by NiGe during germanidation, so the profiles of dopant atoms near the interface were determined only by the segregation effect [3.11]. The junction depth can be well controlled by the germanidation process. From the SIMS result, it is considered that dopant segregation Schottky junction had been successfully formed.

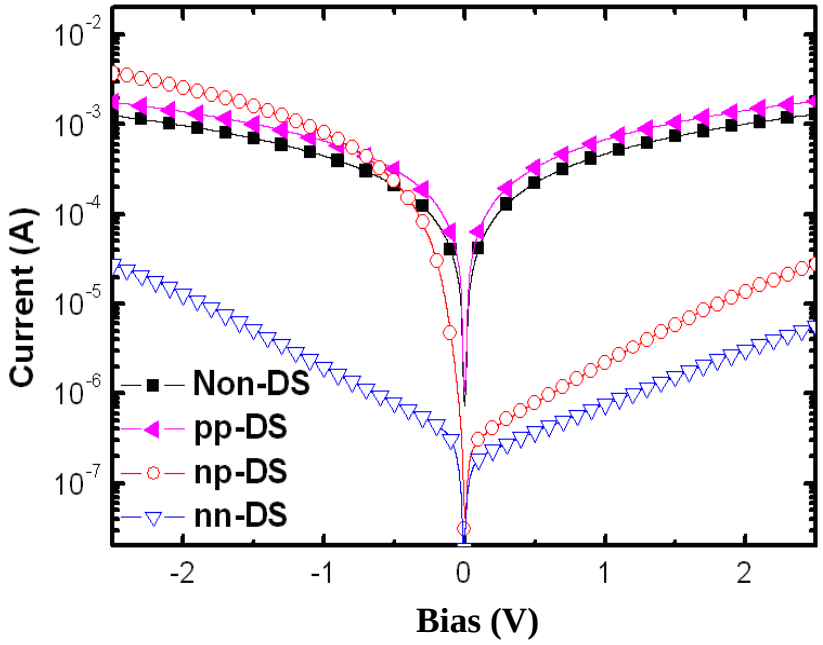



**Fig. 3.7 Dark current comparison between MGM photodetectors with different dopant segregation strategies.**

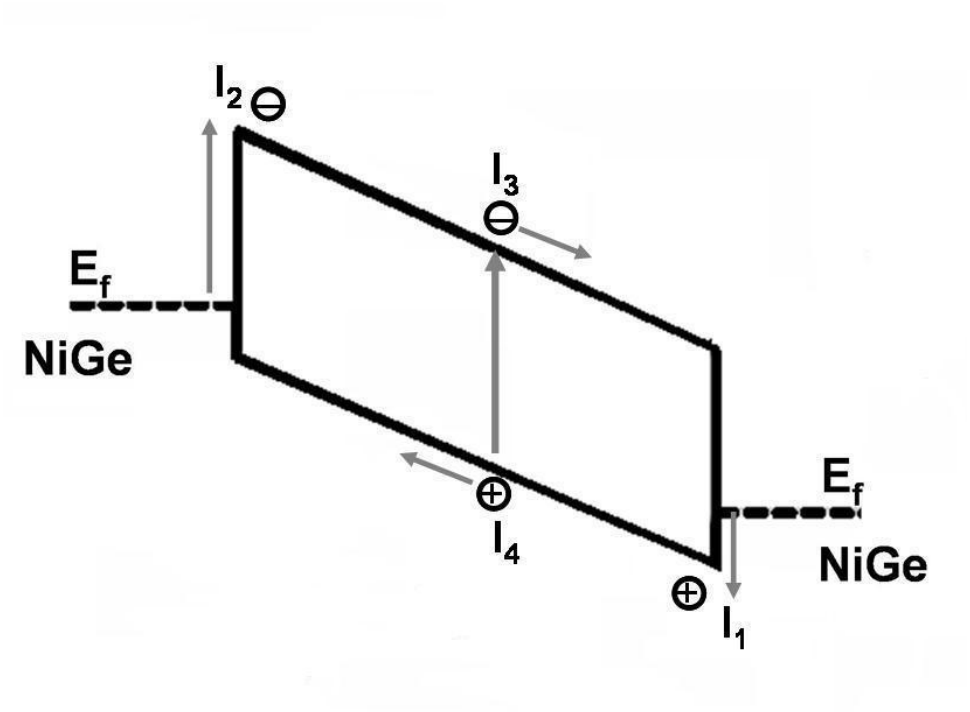



**Fig 3.8 Schematic conduction and valence band profile in MGM photodetector without DS in two NiGe electrodes at biased condition.**

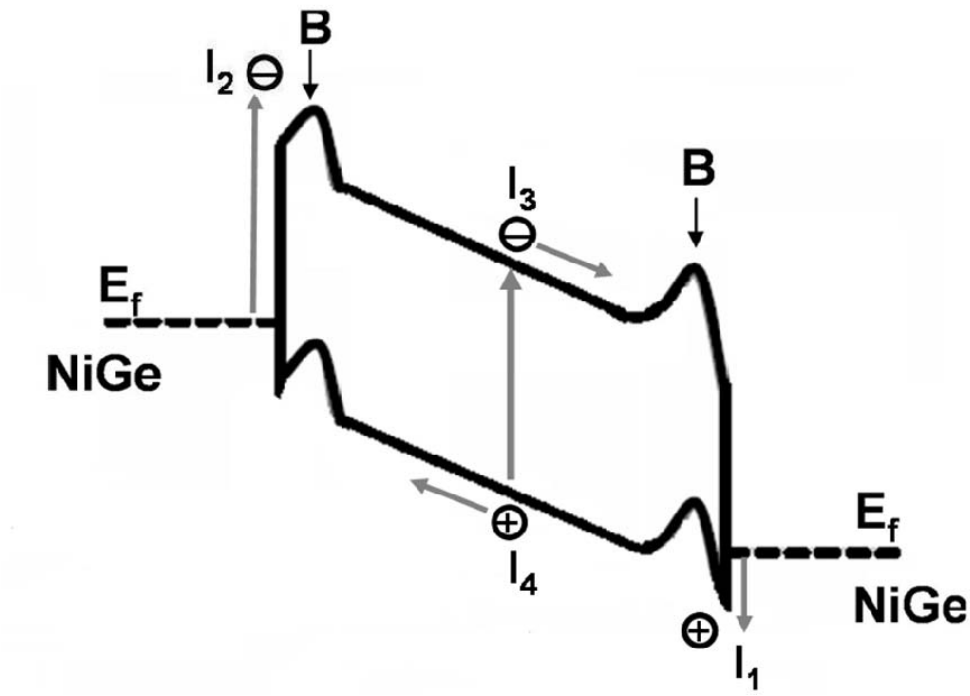



**Fig 3.9 Schematic conduction and valence band profile in MGM photodetector with pp-DS at biased condition.**

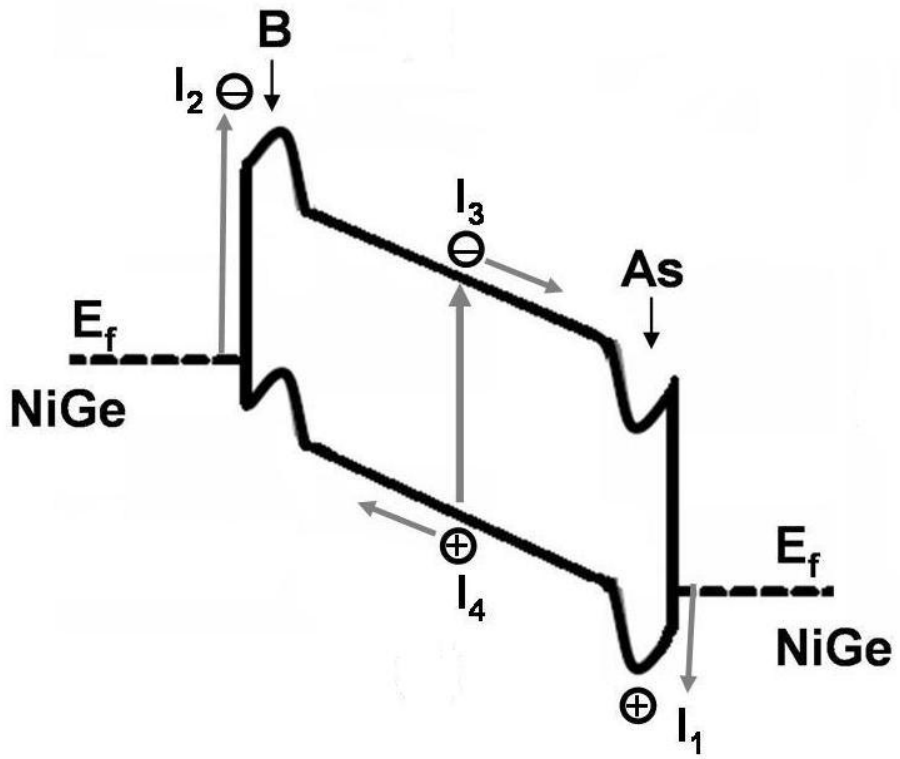



**Fig 3.10 Schematic conduction and valence band profile in MGM photodetector with np-DS at biased condition.**

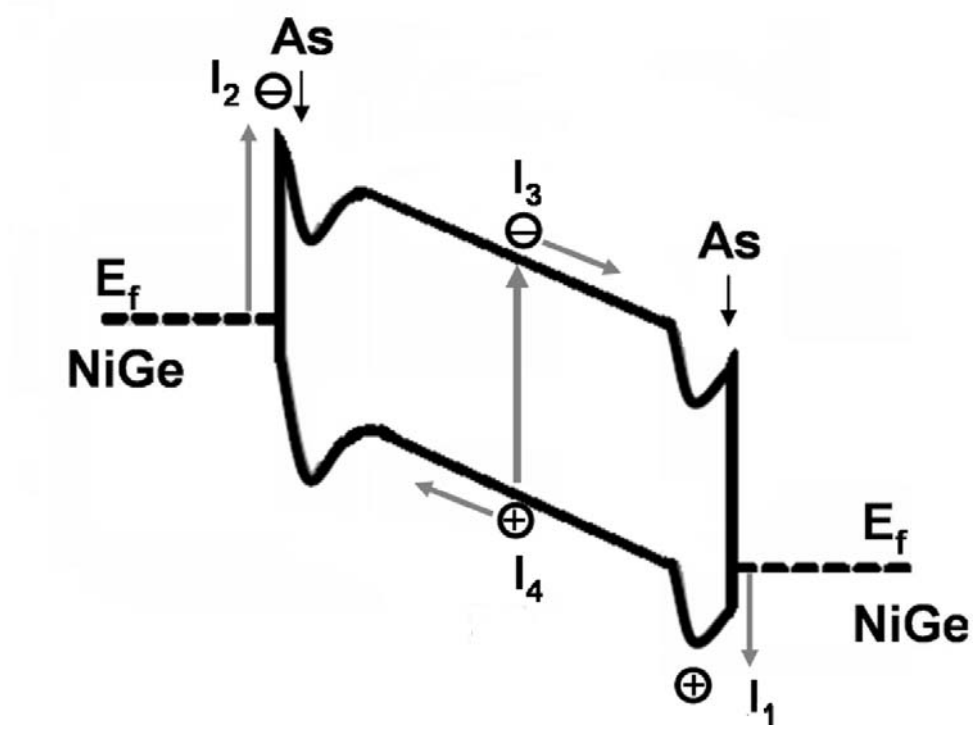



**Fig 3.11 Schematic conduction and valence band profile in MGM photodetector with nn-DS at biased condition.**

In the previous reports of dopant segregation application in SB-MOSFET for enhanced drivability [3.11] [3.12][3.13], p-type dopant was used for p-MOSFET and n-type dopant was used in n-MOSFET. The dark current of MGM photodetector involves both electron and hole current. Detectors with different dopant segregation schemes were designed and tested for comparison. Fig. 3.7 shows the dark current performances of the MGM photodetectors with different dopant segregation structures in the NiGe contact electrodes. For all the electrical characterization, the outer electrodes were grounded, while a bias was applied to the inner electrodes. Fig. 3.8-3.11 show the schematic of the conduction and valence band profile in MGM photodetectors with/without dopant segregation in two NiGe electrodes at biased condition. In MGM photodetector (Fig 3.8), the two major components of dark current are carriers injection over the SB ($I_1$ and $I_2$) and current associated with the thermally generated electron-hole pairs ($I_3$ and $I_4$). In MGM photodetector without dopant segregation technique as shown in Fig. 3.8, due to the Fermi-level pinning effect between NiGe and Ge, the hole SBH is about 0.07-0.1 eV in NiGe/p-Ge and the electron SBH is about 0.6 eV in NiGe/ n-Ge [3.4][3.5]. Ge SB-MOSFET was studied previously for low junction resistance, and Ge SB-p-MOSFET had been demonstrated by many groups [3.16][3.17][3.18]. However, due to the Fermi-level pinning effect, no Ge SB-n-MOSFET was demonstrated since the large electron SBH seriously degrades the MOSFET drivability. Therefore, the major component of the dark current is the hole injection over the SB ($I_1$), and electron current ($I_2$) is very minor.

The MGM photodetector without DS shows a high dark current of $4\times10^{-4}$ A at 1 V (Fig. 3.7).

In pp-DS-MGM photodetector (Fig. 3.9), B segregated in NiGe/Ge interface causes an abrupt band bending upwards, resulting in the reduction of effective hole SBH and thus facilitating hole tunneling probability. Simultaneously, the electron current ($I_2$) decreases due to the modulation of effective electron SBH. Since electron current $I_2$ is just a minor portion of dark current and $I_1$ is the dominant part in the dark current, the photodetector with pp-DS shows an even higher dark current than the photodetector without DS. The MGM photodetector with np-DS shows a dark current of $10^{-6}$ A at –1 V, which is 2-3 orders of magnitude lower than that of the MGM-PD without DS. It is reported that the NiGe/Ge with As ($1\times10^{15}$ $cm^{-2}$) segregation can lower the effective electron barrier height up to 0.1 eV [3.5]. Meanwhile, the downwards band bending induced by As DS increases the effective hole SBH [3.12][3.13], and thus suppressing the major component of dark current in MGM photodetector. Higher As concentration segregated near NiGe contact can further lower the dark current. At -1V bias, the current increases because the segregated As lowers the electron SBH and segregated B lowers the hole SBH.

Among all the structures, the MGM photodetector with nn-DS shows lowest dark current. The asymmetry in I-V curves under forward and reverse bias can be attributed to the electrodes width asymmetry [3.6]. Fig. 3.11 shows the band diagram of MGM photodetector with nn-DS which is similar to the one for dopant segregated Schottky n-MOSFET [3.12, 3.13]. The hole current was suppressed due to the

increase of effective hole SBH. In addition, the SB in low potential electrode blocks the thermally generated hole current ($I_4$). The dark current comparison of DS-MGM photodetectors confirmed that hole injection over SB is the major contribution to the dark current and As-segregation leads to a crucial role in dark current suppression.

To accurately extract the effective hole SBH of the NiGe/Ge contact with As segregation, the *I–V* curves of detector with np-DS (As, Boron segregated separately) were measured at different temperature ranging from 25 to 75 $^{o}$C. The barrier height was extracted using thermionic-emission theory [3.19].

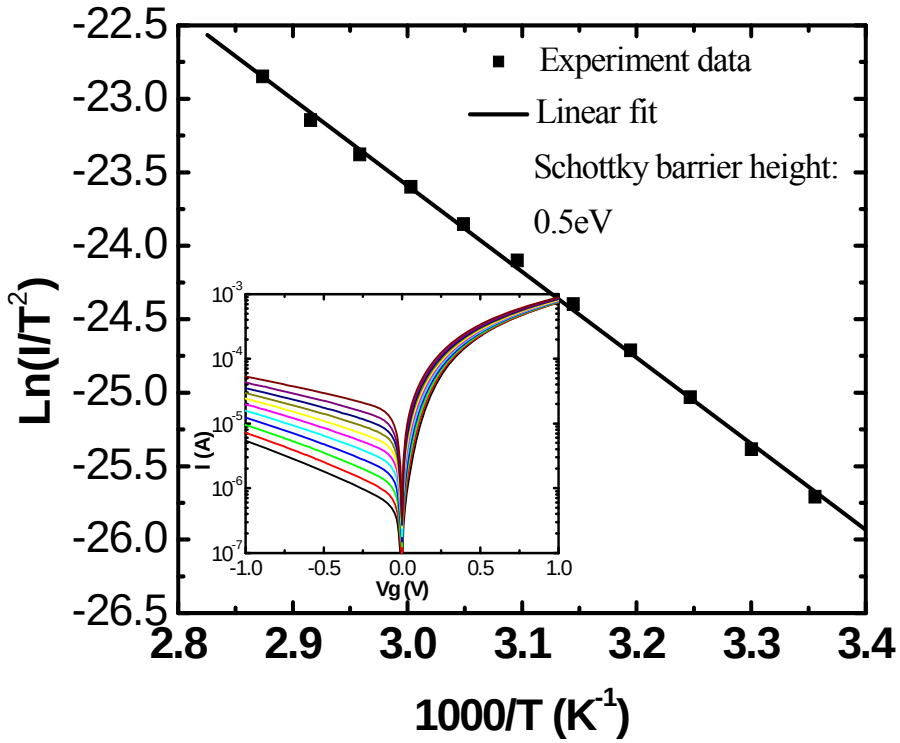



**Fig. 3.12 Richardson plot of current of NiGe/Ge (100) MGM Schottky junction at V=-0.1 V; the inset is the temperature dependent *I–V* curves.**

As discussed before, the major component of the dark current is hole injection over SBH. The thermionic current-voltage relation of a Schottky barrier diode, neglecting the series resistance, is given by

$$I_s = AA^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \tag{3.1}$$

where A is the diode area, A* is the Richardson's constant and $\phi_B$ is the effective barrier height. Equation 3.1 can be written as:

$$\ln\left(I/T^2\right) = \ln(AA^*) - \frac{q(\phi_B)}{kT} \tag{3.2}$$

The plot of $\ln\left(I/T^2\right)$ versus $1/T$ at a constant bias voltage $V_1$ is called a Richardson plot. From the slope of the Richardson plot in Fig. 3.12, an effective hole barrier height extracted is 0.5 eV which is higher than the reported barrier height without As segregation (0.1 eV) [3.4][3.5].

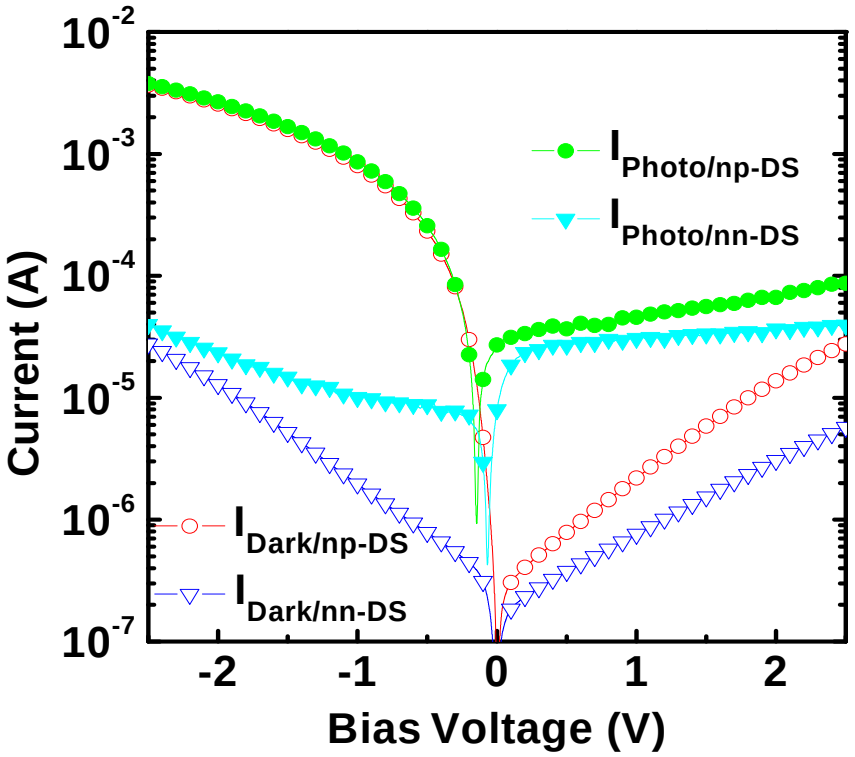



**Fig. 3.13 Measured photocurrent at wavelength of 1.55 μm for MGM photodetectors with nn-DS and np-DS.**

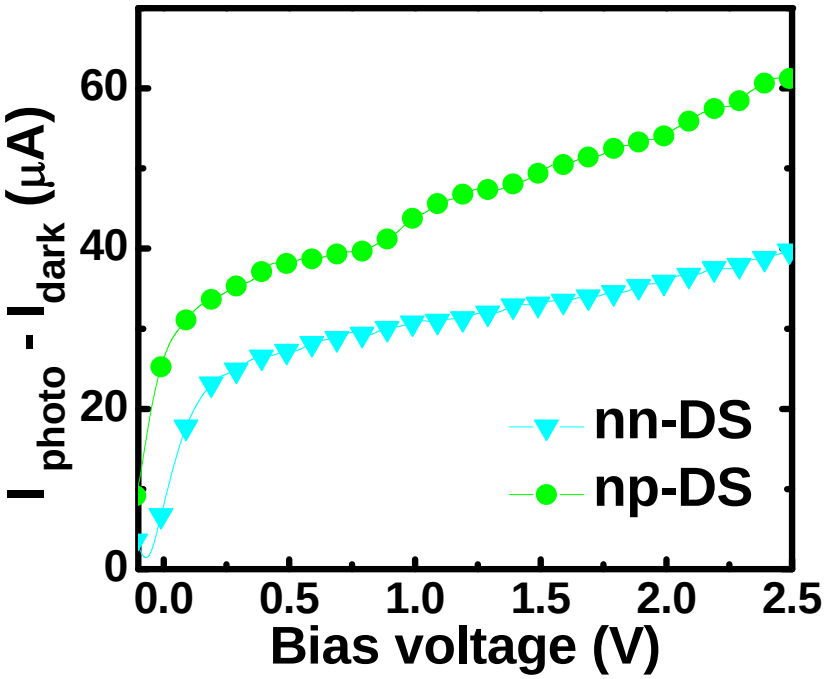


**Fig. 3.14 Photocurrent excluding dark current for MGM photodetectors with nn-DS and np-DS.**

From the dark current comparison, it can be seen that np-DS and nn-DS structures are effective in dark current suppression. To study the effect of dopant segregation on photodetector detection efficiency, the photocurrent of the MGM photodetectors at a wavelength of 1.55 μm was measured. The measurement setup will be discussed in next chapter. Fig. 3.13 shows the photocurrent and the dark current of the MGM photodetectors with nn-DS and np-DS. In Fig. 3.13, the detector with np-DS shows a higher photocurrent compared to the one with nn-DS. However, the dark current of the np-DS structure is also higher. To exclude the dark current factor, Fig. 3.14 shows the comparison of photon generated current (photocurrent minus dark current) between the two DS strategies. The MGM photodetector with np-DS shows 50 % higher photocurrent than that of the MGM photodetector with nn-DS. The lower photocurrent in nn-DS can be explained by its band diagram (Fig. 3.11). In Fig. 3.7, the MGM photodetector with nn-DS shows the lowest dark current. The hole SB in low potential side not only decreases the thermally generated hole current ($I_4$), but also blocks the photon generated hole current**.** It is interesting to observe that the photodetector with nn-DS shows a low dark current and a high photocurrent when the inner electrode is positively biased. When the inner electrode is negative-biased, the photodetector shows a higher dark current but a lower photocurrent. Under light illumination, the photo-generated hole carriers in the photodetector with nn-DS encounter an effective hole barrier created by the dopant segregation of As, as shown in Fig. 3.11. With a positive bias, the photo-generated hole is limited by the hole

barrier at outer electrode (larger width) and the dark current is limited by inner electrode (smaller width). Therefore, in positive bias, the detector shows a higher photocurrent and a lower dark current. A comparison of the photocurrents under positive and negative bias shows that the photodetector structure asymmetry may alleviate the Schottky barrier photocurrent blocking effect. However, even at positive-biased condition, the MGM photodetector with nn-DS still shows 35 % degradation in photocurrent as compared to the MGM photodetector with np-DS. The dopant segregation modulated SB at the low potential side causes the degradation of the MSM photodetectors photocurrent and must be avoided in device design.

## 3.4 Conclusion

In summary, we demonstrated MGM photodetectors on Si substrate with suppressed dark current using dopant segregation technique. In MGM photodetectors, the major component of the dark current is the hole current injection over SB. The As-segregation in electrode plays a crucial role in dark current suppression. The effective hole SBH in the As-segregated NiGe/Ge contact is extracted to be 0.5 eV. After the comparison among the four structures, the detector with nn-DS structure shows the lowest dark current and photocurrent degradation. The degradation can be alleviated by asymmetric electrodes width. The MGM photodetector with n- and p-type dopant segregated respectively in two electrodes is the optimal structure for dark current suppression and photocurrent detection.

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# Chapter 4
# High-Speed Surface-illuminated Metal-Germanium-Metal Photodetector

## 4.1 Introduction

In Chapter 3, surface-illuminated MGM photodetectors were fabricated to investigate the application of dopant segregation technique in photodetectors. Since the fabricated device is for dark current suppression mechanism study, the device size (contact spacing: 17 μm) is not optimized for large bandwidth operation. In this chapter, we demonstrate scaled MGM photodetectors (contact spacing: 2.5 μm) with np-DS for large bandwidth operation. The SBH modulation effect of dopant segregation will be further studied. The responsivity and bandwidth measurement of the photodetectors will be discussed in details. The detector performance will be benchmarked with previous publication.

## 4.2 Experiment

### 4.2.1 Device Fabrication

Starting with (100) p-type Si (~8-15 Ωcm), PECVD $SiO_2$ of 150 nm was deposited, patterned and dry/wet etched to open circular windows (20 μm in diameter) for subsequent Ge selective deposition. Before epitaxy growth, the wafers were cleaned in SC1 ($NH_4OH$:$H_2O_2$: DI ~1:2:10] and diluted HF (1:200). Subsequently, ~10nm Si and 25 nm thick $Si_{0.8}Ge_{0.2}$ buffer layer were grown at 350-400˚C and Ge

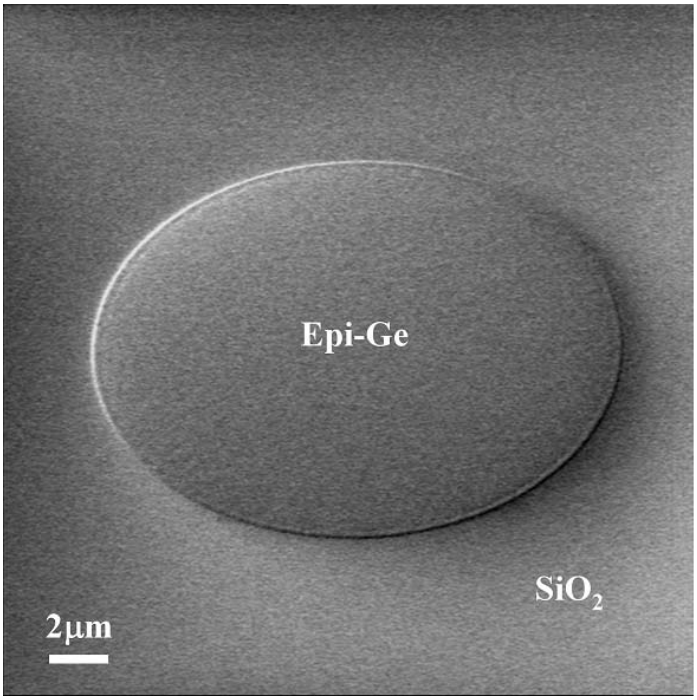


**Fig. 4.1 SEM image of selective epi-Ge growth through $SiO_2$/Si window.**

was deposited using the developed Ge growth method in an UHV-CVD. Fig. 4.1 shows the SEM image of selective Ge growth in the round $SiO_2$/Si window region. From the discussion of Chapter 3, we drew the conclusion that np-DS is the optimal scheme for both dark current suppression and detection efficiency. Therefore, we adopt the np-DS structure in this experiment. The Ge region was patterned and then implanted with As ($1\times10^{15}$ $cm^{-2}$/12 keV) in inner electrode region. After PR strip and wet cleaning, the wafer was patterned again and implanted with $BF_2$ ($1\times10^{15}$ $cm^{-2}$/12 keV) in outer electrode region. One part of the wafer is not implanted for non-DS-MGM photodetectors fabrication. After PR strip, $SiO_2$ deposition of 300 nm was deposited by PECVD. Beside isolation, $SiO_2$ acts as an anti-reflection layer for surface-illuminated photodetectors. After patterning, RIE process was done to partially etch the $SiO_2$. The remaining $SiO_2$ was removed by HF acid (1: 100) wet

etching to expose Ge contact region. Next, 20 nm Ni was deposited by sputtering for NiGe electrodes formation. Germanidation process was carried out by RTA at 350˚C. Un-reacted Ni was removed by nitric acid. Finally, Al deposition, patterning and etching were performed for metallization formation. Fig. 4.2 is the SEM image of a MGM photodetector with 2.5 μm spacing between two electrodes. The small width inner metal contact is As-segregated for lower dark current as discussed in Chapter 3, and the outer electrode is segregated with B.

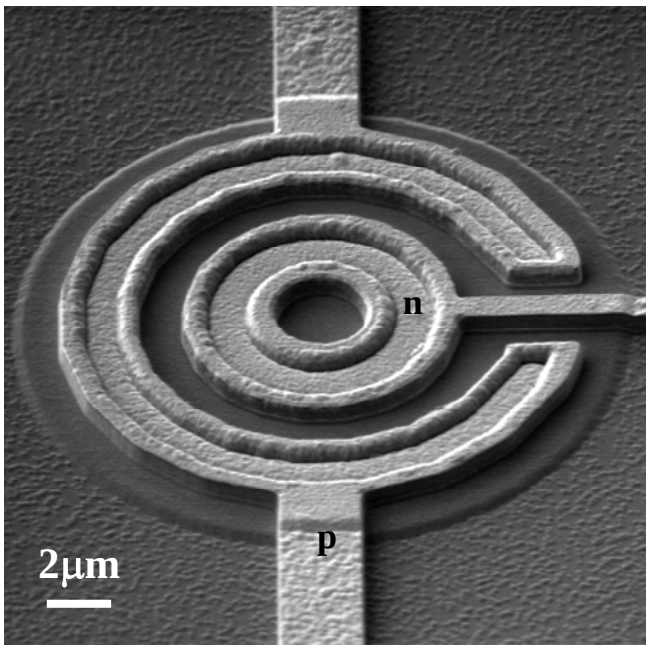


**Fig. 4.2 SEM image of a fabricated MGM photodetector with np-DS, the contact spacing between As segregated contact and B segregated contact is 2.5 μm.**

## 4.2.2 Responsivity Measurement

As introduced in Chapter 1, responsivity is a parameter which evaluates the detection efficiency of photodetectors and can be expressed by the following formula:

$$R = \frac{I_p}{P} = \frac{e\eta}{h\nu} \tag{4.1}$$

The photocurrent measurement was done using a probe station, analyzer and a laser source in the wavelength range of 1500-1650 nm. The laser was directed at a normal incidence from the top of the photodetector through a single mode optical fiber. The incident laser power was measured by an optical power meter. The device was measured under laser incidence and dark condition for comparison. There are two measurement modes carried out. First, the photocurrent at the wavelength of 1550nm was characterized in bias from -2 V to 2 V. Meanwhile, the photocurrent at the wavelength ranging from 1520 to 1620nm was also measured at a constant bias.

## 4.2.3 Bandwidth Measurement

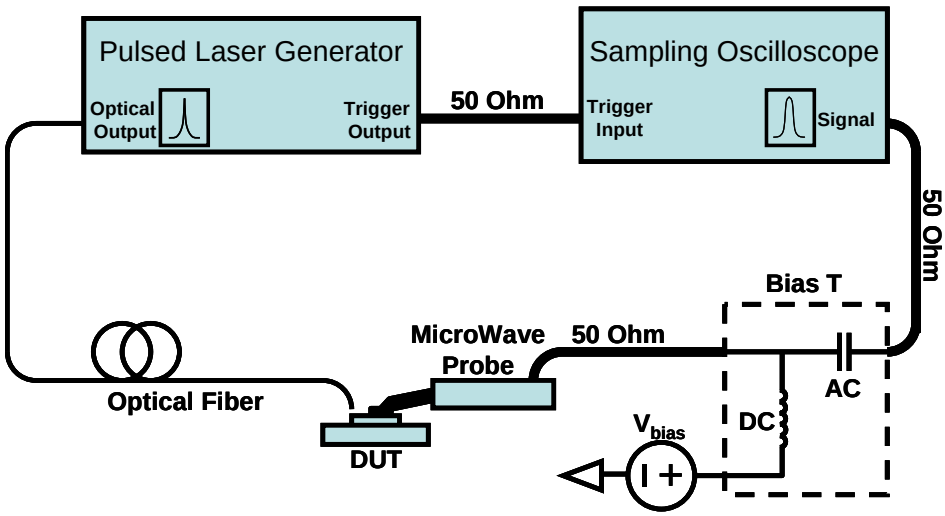


**Fig. 4.3 Schematic of temporal response measurement setup.**

Temporal response measurement was used for bandwidth extraction. By applying a very short excitation pulse, temporal response of device in time domain was directly obtained. The excitation pulse is provided by a laser with duration in sub-ps region

which corresponds to a frequency in hundreds of GHz. Detectors under measurement are expected to have a bandwidth in tens of GHz at most. A schematic of the temporal response measurement setup for photodetectors is shown in Fig 4.3. The electrical pulse from photodetector was measured by a digital oscilloscope with 60 GHz bandwidth. To obtain the temporal response of the photodetectors under different biased condition, a DC arm was connected to the system through a bias-T. The photodetector was measured using a pulsed laser with the optical pulse width of 80 fs at the wavelength of 1550 nm. The laser beam was coupled into photodetectors through a single mode fiber. The photodetector was probed with high-speed (150GHz) microwave probes in measurement.

## 4.3 Results and Discussion

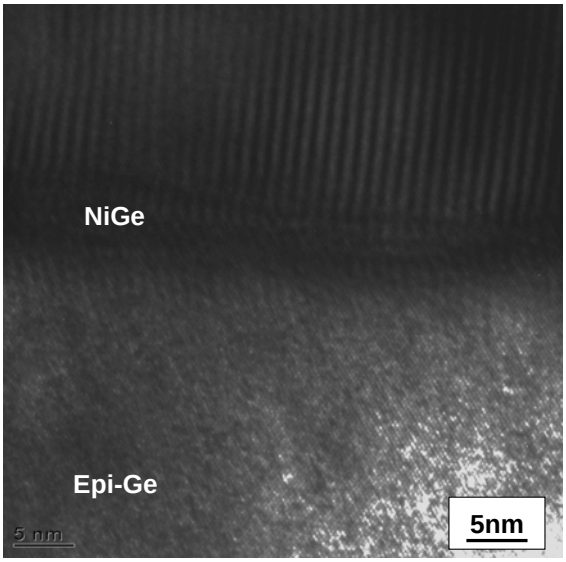


**Fig. 4.4 HR-TEM image of the layers of NiGe/Ge.**

To check the contact formation in submicron contact holes, device was

characterized by HR-TEM. Fig. 4.4 shows the HR-TEM image of the Ni Germanide layer formed on epi-Ge. Energy dispersive X-ray spectroscopy analysis on the Ni Germanide shows the formation of low resistivity mono-nickel germanide. Similar to the result in Chapter 2, the NiGe forms sharp and smooth interface and exhibits epitaxial growth.

Fig. 4.5 compares the dark current performances between the MGM photodetectors with and without dopant segregation in the NiGe contact electrodes. As mentioned in the process fabrication part, the MGM photodetectors with and without np-DS were fabricated on the same wafer with the identical process for fair comparison. In measurement, the inner electrodes were grounded, while a bias was applied to the outer electrodes. I-V curve for the MGM photodetector without dopant segregation shows a back-to-back diode behavior. The dark current at -1V bias is about $3 \times 10^{-4}$ A. Due to the Fermi-level pinning effect between NiGe and Ge, the hole SBH is 0.07~0.1 eV for NiGe/ p-Ge [4.1][4.2]. The major component of the high dark current is the hole current injection over the SB. The MGM photodetector with np-DS NiGe contact shows a dark current of $10^{-7}$A at -1V which is ~3 to 4 orders of magnitude lower than that of the MGM photodetector without DS. At positive bias, the current increases because the segregated As lowers the electron SBH and segregated B lowers the hole SBH. The comparison result is consistent to the one in Chapter 3, which confirms the dark current suppression effect of dopant segregation technique. It should be noted that the dark current suppression effect in Fig. 4.5 is more significant than the device in Chapter 3 (Fig.3.7). Dark current suppression up to

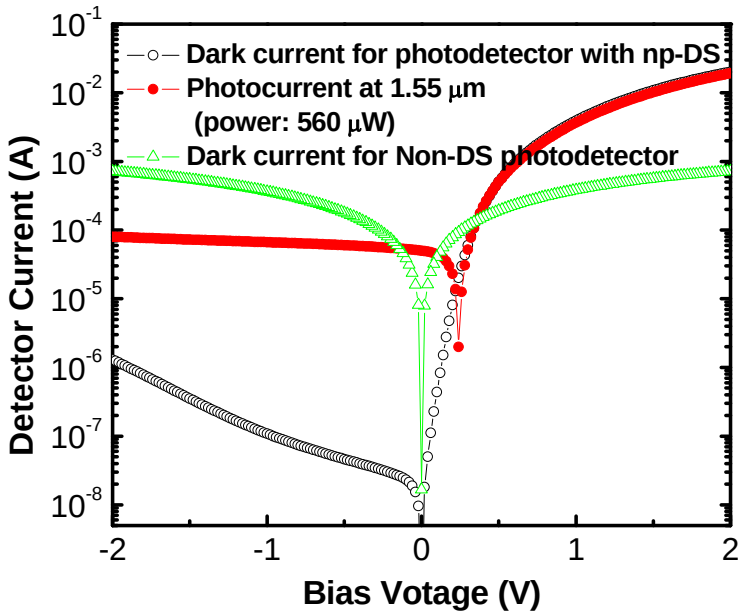


**Fig.4.5 Dark current comparison between MGM photodetectors with and without np-DS and measured photocurrent at wavelength of 1.55 μm for np-DS-MGM photodetector.**

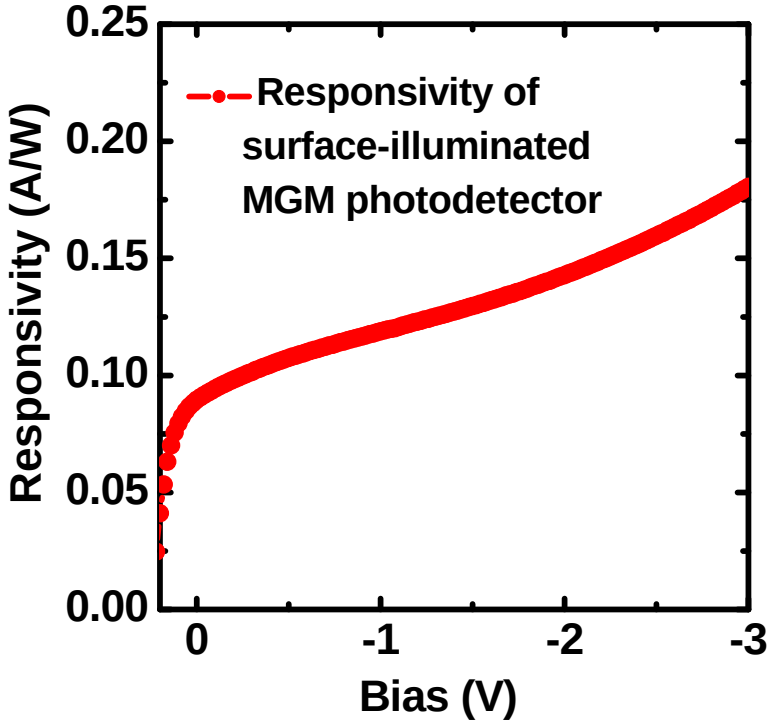


**Fig.4.6 Responsivity of surface-illuminated MGM photodetector with np-DS.**

2 orders of magnitude was achieved in Fig. 3.7. Besides SBH, another factor affecting dark current density is device contact spacing which affects the series resistance in Ge region. The scaling of detector contacts spacing reduces the series resistance, making the dark current suppression by SBH modulation more obvious. Fig. 4.5 also shows the photocurrent of the detector with np-DS at the wavelength of 1.55 μm. The laser input power is 0.55 mW at 1.55 μm. The measured photocurrent of the detector at -1 V bias is 67 μA which is 3 orders of magnitude higher than its dark current at the same bias. It should be noticed that, at 0-V bias, the detector shows a photocurrent of 50 μA. The photocurrent of the MGM photodetector with np-DS is lower than the dark current of the detector without DS. The MGM photodetector without dopant segregation can not be used for low power circuit due to its large dark current. Its photocurrent measurement needs a laser with a higher power. Therefore, the dopant segregation technique not only reduces the standby power consumption of photodetector, but also enhances its detection sensitivity. Fig. 4.6 shows that the responsivity of the photodetector with np-DS is 0.088 A/W at 0 V, 0.13 A/W at -1 V and 0.14 A/W at -2 V. The ability of the device to operate at photovoltaic status (0 voltage bias) provides high signal to noise ratio. Meanwhile, there are several reasons for the relatively low responsivity. First, the responsivity is mainly limited by the thickness of the Ge epi-layer (300 nm) which is the absorption length of the photodetector. In the work by Oh et al. [4.2], higher responsivity was achieved with a Ge thickness of 1μm. In our device structure, we can further increase the thickness, e.g., to 4000 Å or 5000 Å, especially with the selective epi-growth scheme to further

increase the responsivity. However, it should be noted that increasing Ge thickness will lead to bandwidth degradation.

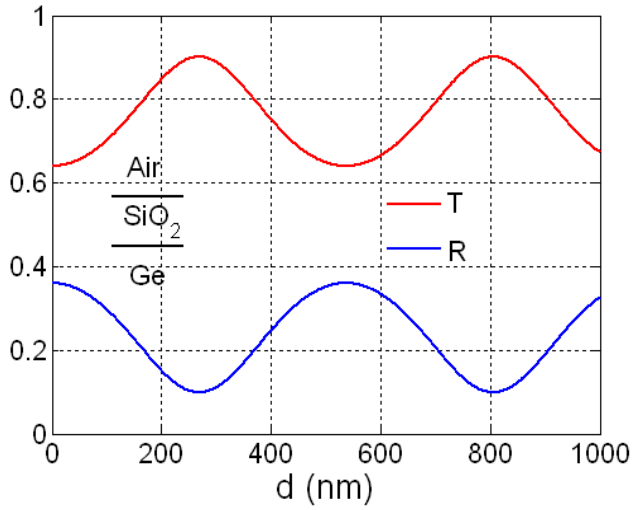


**Fig. 4.7 The simulated reflection and transmission coefficients of $SiO_2$ on Ge at wavelength of 1.55 µm using MATLAB (transmission: T, Reflection: R)**

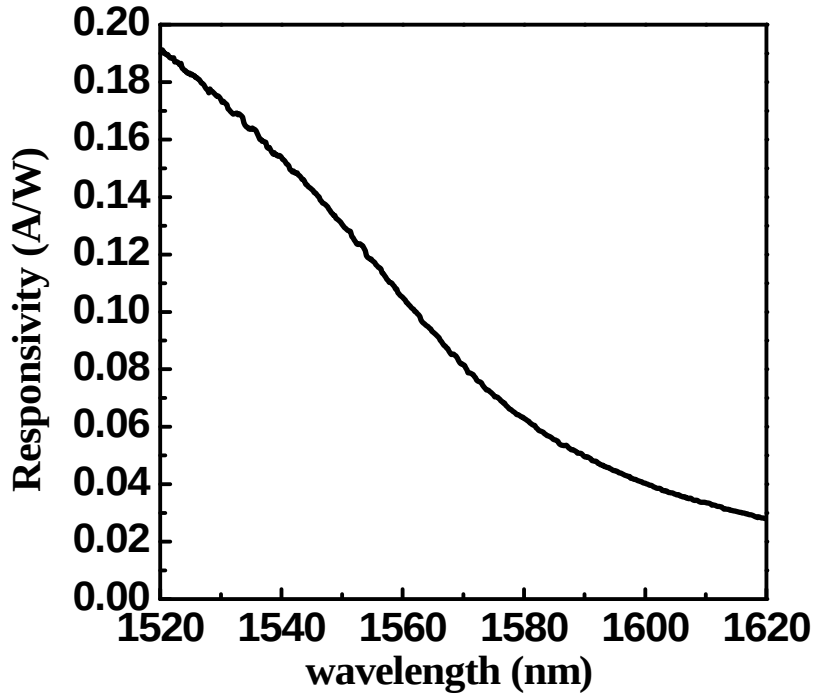


**Fig. 4.8 Measured spectral responsivity of the photodetector versus wavelength at -1 V.**

Another reason of the low responsivity is the photon absorption by the metal electrodes on the top of photodetectors. The metal electrodes have a strong absorption of photon energy with no photo current contribution. One approach to enhance the responsivity is to increase the contact spacing, resulting in a larger detection active region compared to electrodes region. However, increasing the contact spacing will directly degrade the bandwidth of photodetector since the bandwidth is strongly contact spacing dependent. Therefore, for surface-illuminated configured photodetector, there is always a tradeoff between detection responsivity and bandwidth. In addition, although the device was designed and fabricated with a $SiO_2$ anti-reflection layer, there is still a part of photon energy being reflected on the surface of the photodetector. Fig. 4.7 shows the simulated reflection and transmission efficiency of $SiO_2$ on Ge at the wavelength of 1.55 μm using MATLAB. With 300nm $SiO_2$ on Ge, the reflection coefficient is about 0.1 which is smaller than that in the condition of no anti-reflection layer (R: 0.36). Wavelength dependent responsivity was also measured to characterize the operation wavelength range of the detector. The wavelength in measurement is from 1520 to 1620 nm. A constant bias of -1 V was applied on the detector during the measurement. The responsivity of the photodetector gradually decreases with the increase of wavelength, and the responsivity at the wavelength of 1550 nm is about 1.3 A/W (Fig. 4.8).

Fig. 4.9 shows the temporal response of the MGM photodetector with np-DS at different bias which was measured using a 1.55 μm pulsed fiber laser with an optical pulse width of 80 fs. The full width at half maximum (FWHM) of the response pulse

is 69 ps at -0.1 V, 56 ps at - 1V and 56 ps at -2 V. It is observed that, after -1 V bias, the FWHM of temporal response does not decrease by further biasing. In addition, there are several secondary peaks after the main pulse. The secondary peaks are electrical reflections resulting from the impedance mismatch between the detector and the measurement system [4.3]. Fig. 4.10 shows the 3 dB bandwidth of the DS-MGM photodetector extracted from the time domain pulse response measurement as a function of reverse bias. The 3 dB bandwidth of the MGM photodetector is close to 6 GHz at -1 V. The full bandwidth can be achieved at very low bias of -1V. This is mainly due to the low sheet- and contact-resistances of the NiGe electrodes. Under reverse bias, the electric potential is dropped mainly across the Ge active region

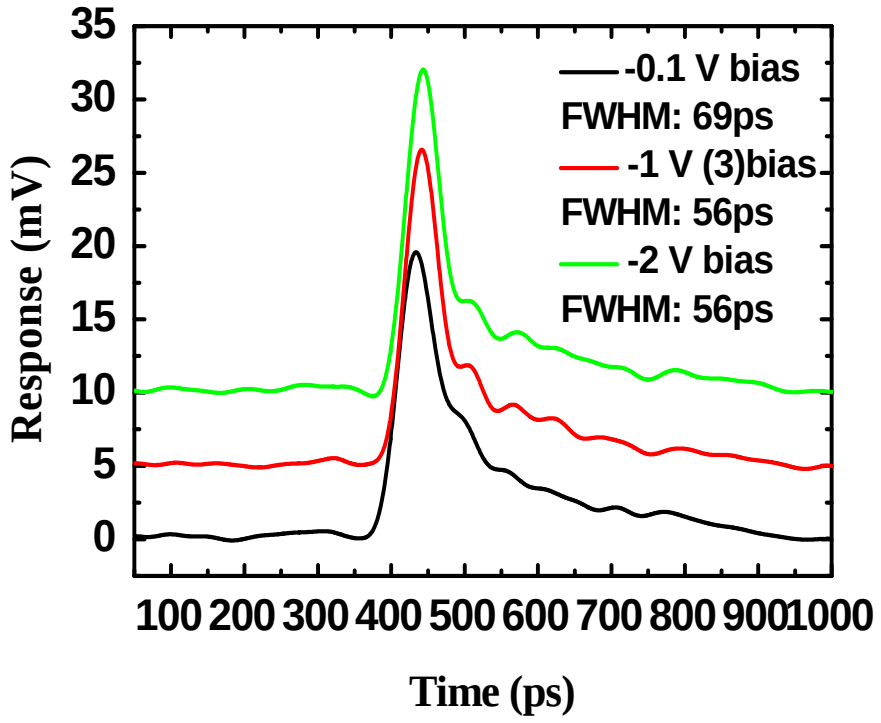


**Fig. 4.9 Temporal response of the MGM photodetector with np-DS at different bias to an 80 fs laser pulse at wavelength of 1.55 μm. The FWHM is 56 ps at -1V bias.**

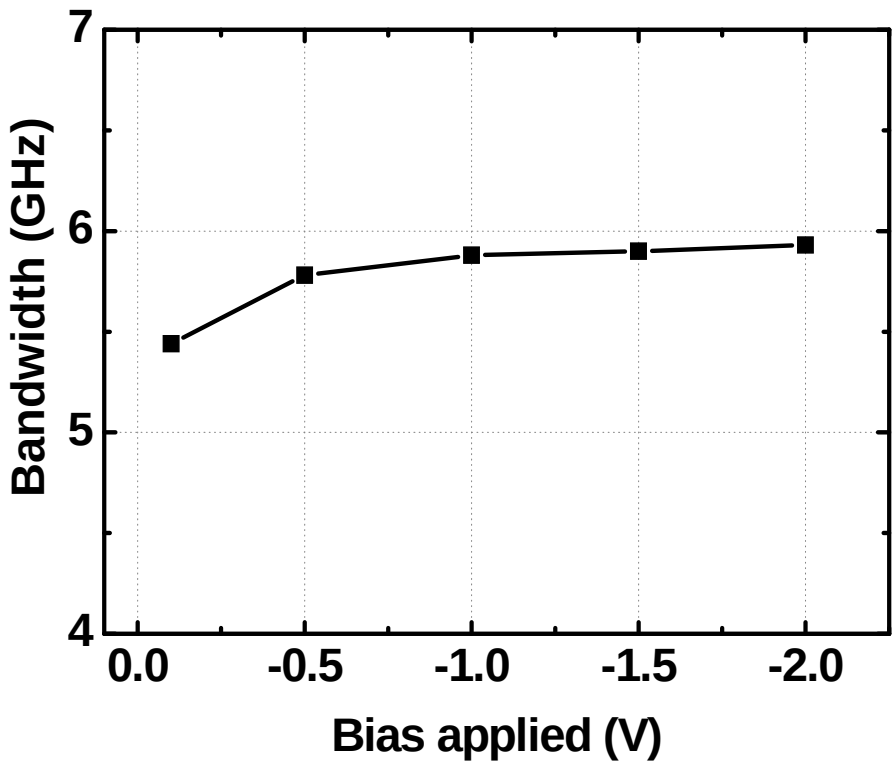


**Fig. 4.10 3dB bandwidth of MGM photodetector with np-DS as a function of reverse bias.**

due to the low sheet resistance of nickel mono-germanide. Full bandwidth at a low reverse bias is very desirable for low voltage operation in OEIC.

Table 4.1 compares the performances of the DS-MGM photodetector in this work with the other published MSM and lateral p-i-n photodetectors. Since the responsivity of surface-illuminated detector is highly Ge thickness dependent, the responsivity comparison is not listed. The comparison is mainly focused on the dark current and the bandwidth. In [4.4], MGM photodetector with Ni or Ti as electrodes shows a dark current of ~$10^{-5}$A at 1V bias, and the detector with Ti electrodes shows a lower dark current ($10^{-5}$A) due to its lower work function compared to Ni [4.4].

**Table 4.1 Summary of the performances of previously published MSM and lateral p-i-n photodetectors.**

| PDs structure | Dark current at -1 V | Dark current/ width | Width /Spacing | FWHM | 3dB Bandwidth |
|---|---|---|---|---|---|
| Ge MSM on Si [4.4] | Ti-Ge-Ti: $10^{-5}$ A | N.A | --/5 μm | 350 ps | -- |
| | Ni-Ge-Ni: $1.7 \times 10^{-5}$ A | N.A | | | |
| Ti-Si-Ti on Si [4.5] | $2\times10^{-5}$A | $6.4\times10^{-8}$A/μm | 314 μm/ 1 μm | N.A | -- |
| Ag-Ge-Ag [4.8] | -- | N.A | --/10 μm | 0.4-1.8 ns | 0.5GHz |
| A-Ge-Ag with α-Ge [4.2] | MGM w α-Ge: $10^{-6}$ A | N.A | --/2.5 μm | N.A | 2.8GHz at -2V |
| | MGM: $3\times10^{-4}$ A | N.A | | | 4.3GHz at -4V |
| Lateral Ge p-i-n [4.6] | $2\times10^{-6}$ A | $8.7\times10^{-9}$ A/μm | 230 μm /2.5 μm | | 2.2 GHz at -1V, 3.5 GHz at -3 V, 3.8 GHz at -5 V |
| Germanium Lateral p-i-n on SOI [4.7] | $10^{-8}$ ~$10^{-7}$ A | N.A | --/0.4-1.0μm | 14.9 ps | 29 GHz (0.4 μm spacing), 15 GHz (1μm spacing) both at -1 V |
| **NiGe-Ge-NiGe with Dopant segregation (This work)** | **$10^{-7}$A (with DS) $4*10^{-4}$A (without DS)** | **$3.3\times10^{-9}$ A/μm (with DS)** | **30μm/2.5μm** | **56 ps** | **6 GHz at -1 V** |

In [4.2], with an amorphous Ge layer between Ge and metal contact as Schottky barrier enhancement layer, a MGM photodetector was demonstrated with a dark current of ~$10^{-6}$ A at 1 V. MGM photodetector with np-DS in this work shows the lowest dark current among all the reported MGM photodetectors and comparable dark current to the reported lateral Ge p-i-n photodetectors [4.6][4.7]. The dark current normalized with device width is listed in the following column if the electrode width is provided in reference paper. In [4.4] and [4.8], the bandwidths of the devices are relatively lower due to their larger contact spacing. The MGM photodetector with an amorphous Ge layer shows a bandwidth of 2.8 GHz at 2 V and 4.3 at 4 V [4.2]. The bandwidth of lateral p-i-n photodetector is also highly bias dependent. A bias up to 5 V is need for 3.8 GHz operation [4.6]. Compared to the Ge photodetectors with the same contact spacing (2.5μm) in [4.2][4.6], the MGM photodetector with np-DS in this work shows a larger bandwidth up to 6 GHz at -1 V, and its bandwidth is less bias dependent. This is due to the lower resistance of NiGe [4.9] compared to Ge n- and p-junction. The MGM photodetector in this work shows a high bandwidth at low reverse bias, which is desirable for low power consumption and high signal-to-noise ratio. Besides the low resistance of NiGe contact, another reason for low voltage operation is the build-in electrical field ($E_{build\text{-}in}$) induced by dopant segregation technique, which we will discuss in details in next chapter. The lateral Ge p-i-n photodetector in [4.7] shows a very high bandwidth up to 19 GHz due to its small electrodes spacing. The bandwidth of MGM photodetector can be further improved by scaling electrodes spacing. However, for surface-illuminated configured detectors, the

scaling of the contact spacing will result in a significant degradation in responsivity. In next chapter, photodetectors with scaled contact spacing integrated with waveguide will be demonstrated and characterized.

## 4.4 Conclusion

Surface-illuminated MGM photodetector was demonstrated on Si substrate with suppressed dark current using dopant segregation method. The MGM photodetector with np-DS shows a fast temporal response up to ~56 ps and a low dark current of $10^{-7}$ A at -1 V bias, indicating that dopant segregation is a promising technique for future Ge photodetector application in OEIC.

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# Chapter 5

# High-Speed Metal-Germanium-Metal Photodetector Integration with SOI Waveguide

In this Chapter, we demonstrate a photovoltaic mode (i.e., 0-V operation) high-speed MGM configured photodetector integration with Si on insulator (SOI) waveguide. The metal contacts are engineered by an asymmetrical dopant-segregation scheme (np-DS) on Schottky contacts to suppress the dark current, and are with scaled spacing (0.8 μm) for high bandwidth operation.

## 5.1 Waveguided Photodetector

As introduced in Chapter 1, optical waveguide, as interconnect of optical signal, is one of the basic components of OEIC. The function of waveguide is to confine and transmit optical signals over tens or hundreds of micrometers between optical devices. Photodetector, as one of components in OEIC, needs to be integrated with waveguide, and photodetectors integrated with waveguide are called waveguided photodetectors.

The most frequently used optical waveguide is dielectric optical waveguide. Its structure consists of a longitudinally extended high-index optical medium, called core, which is transversely surrounded by low-index media, called cladding [5.1]. The guided optical signal propagates in the longitude direction of waveguide. It should be noted that materials for waveguide fabrication must be essentially transparent at the wavelength of propagated signal.

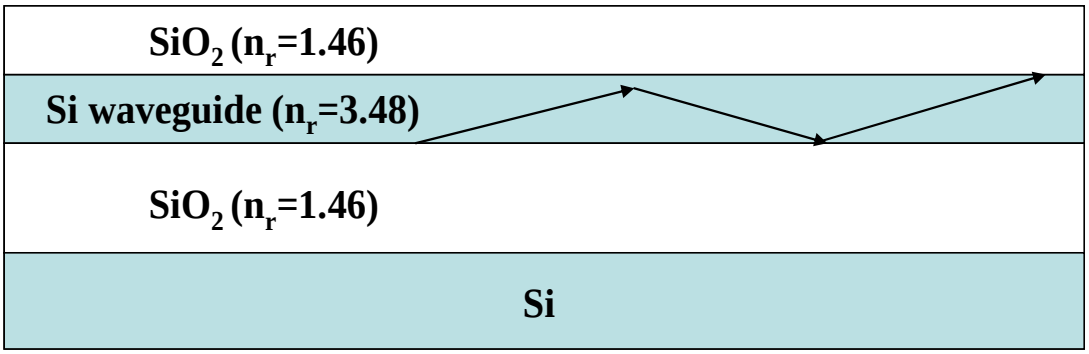


**Fig. 5.1 Schematic of light propagation in SOI waveguide.**

For waveguide in OEIC, Si, as the basic material of VLSI, is an ideal material for waveguide fabrication since it is transparent at wavelengths of 1330 nm and 1550 nm. Meanwhile, SOI waveguide is a very promising structure due to its ease of process and low propagation loss. Fig. 5.1 shows the schematic of light propagation in SOI waveguide. Vertical confinement is achieved through different refractive index. The refractive index of Si and $SiO_2$ are 3.48 and 1.46 respectively. Similar to optical fiber, waveguide directs optical signal by total internal reflection. Waveguide index contrast is expressed as:

$$Indexcontrast = \frac{n_1^2 - n_2^2}{2n_1^2} \qquad (n_1 > n_2) \qquad (5.1)$$

High index contrast generally leads to a better light confinement in waveguide. In some cases, the $SiO_2$ on top of Si can be removed since air also can be a good cladding. During light propagation in waveguide, there is a propagation loss which is normally expressed in the unit of dB/cm. There are three propagation loss

mechanisms including material absorption, scattering and leakage. As mentioned, waveguide material must be transparent at the optical signal wavelength. However, photons absorption still exists due to band edge absorption and free carrier absorption [5.1]. Waveguide scattering is induced by the roughness of waveguide surface. In SOI waveguide case, the scattering mainly depends on the roughness of etched sidewall.

The photodetectors discussed in previous chapters are surface-illuminated photodetectors. In surface-illuminated photodetectors, optical signal propagates in a direction which is perpendicular to device junction interface. This condition leads to an undesirable trade-off between detection efficiency and bandwidth. Besides, another drawback of surface-illuminated photodetectors is the trade-off between bandwidth and its saturation power. A high bandwidth photodetector requires a small absorption volume, which leads to a high carrier concentration at a given light power level. The space charge effect in detector absorption region caused by the high carrier concentration sets a limit on the saturation power of the photodetectors [5.1]. Detector saturation power can only be improved by increasing the photodetector absorption volume, resulting in a degradation of its bandwidth.

Photodetector integrated with waveguide provides a solution to these trade-off limitations. In waveguided photodetectors, the guided optical signal propagates in the direction which is perpendicular to the drift of photo-generated carriers and is parallel to the detector junction interface. This detection geometry decouples the absorption length from the carrier drift length. Therefore, a well designed waveguided photodetector is capable of achieving high absorption efficiency and high bandwidth simultaneously. In addition, the effective absorption length of waveguided photodetector is not restricted to the thickness of detector semiconductor thin film. The absorption region of waveguided photodetector becomes the detector length

along the waveguide direction. The absorption volume can be easily increased without degradation in detector bandwidth by increasing detector length. Therefore, the bandwidth of waveguide photodetector can be improved without sacrificing its detection efficiency and saturation power.

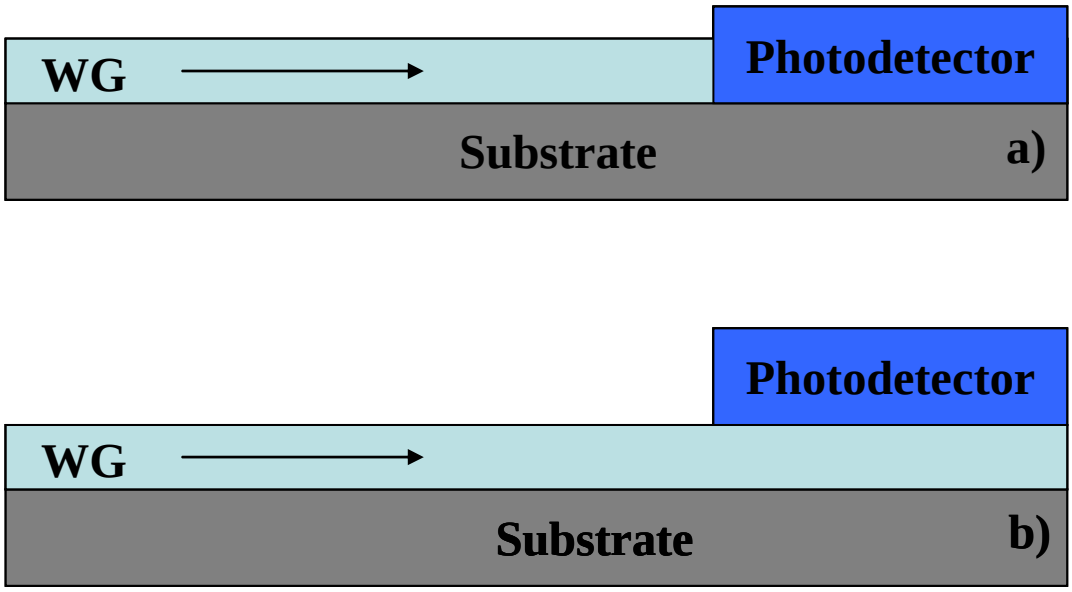


**Fig. 5.2 Schematic of waveguide coupling to photodetector, a) butt coupling mode, b) vertical coupling mode.**

There are two major approaches for optical signal coupling from waveguide into photodetectors: 1) butt coupling mode and 2) vertical coupling mode as shown in Fig. 5.2. For butt coupling approach, light wave in waveguide propagates to photodetector directly. This mode offers the merit of high coupling efficiency. The major disadvantage of butt coupling is the complexity of process integration. In vertical coupling mode structure, optical signal is coupled into photodetector evanescently as shown. Compared to butt coupling, vertical coupling mode has a lower coupling efficiency. Therefore, the photodetector in vertical coupling is normally designed to

be longer to increase the detection efficiency. The obvious advantage of vertical coupling approach is the ease of fabrication process. In the case of Ge photodetectors integration with SOI waveguide, Ge layer can be achieved by selective epitaxy growth on Si waveguide. In this chapter, we adopt the vertical coupling approach for MGM photodetectors integration with SOI waveguide.

## 5.2 Experiment

### 5.2.1 Device Fabrication

Fig. 5.3 shows the schematic process flow of MGM photodetector integration with SOI waveguide. Process started with (100) SOI wafer with 400 nm-thick p-type Si (~8-15 Ωcm) and 1μm-thick buried $SiO_2$. The waveguide is designed to be 200 nm in height, so the Si layer needs to be thinned down. We used cycled oxidation and wet etching method to reduce the Si thickness. First, the SOI wafer was oxidized in furnace. The target thickness of thermal $SiO_2$ is 150 nm, so about 70 nm Si was consumed during oxidation. After oxidation, HF acid (1:100) wet etching was done to remove the $SiO_2$ on Si layer. After this two-step process, 70 nm Si was removed. Another two more cycles of this process roughly reduced the Si layer to 200 nm. After thinning down process, detector and waveguide regions were defined by lithography. The waveguide is designed to be 600 nm in width and 200 nm in height. At the end of waveguide, there is a waveguide tip which the optical signal was coupled into. Near the tip coupler, the waveguide width becomes narrow gradually. The width of tip is about 200 nm. The tip coupler is designed to be a fiber-to-waveguide coupler. Due to the small defined dimension, besides PR, a bottom anti-reflective coatings (BARC) layer was utilized to suppress standing wave effect

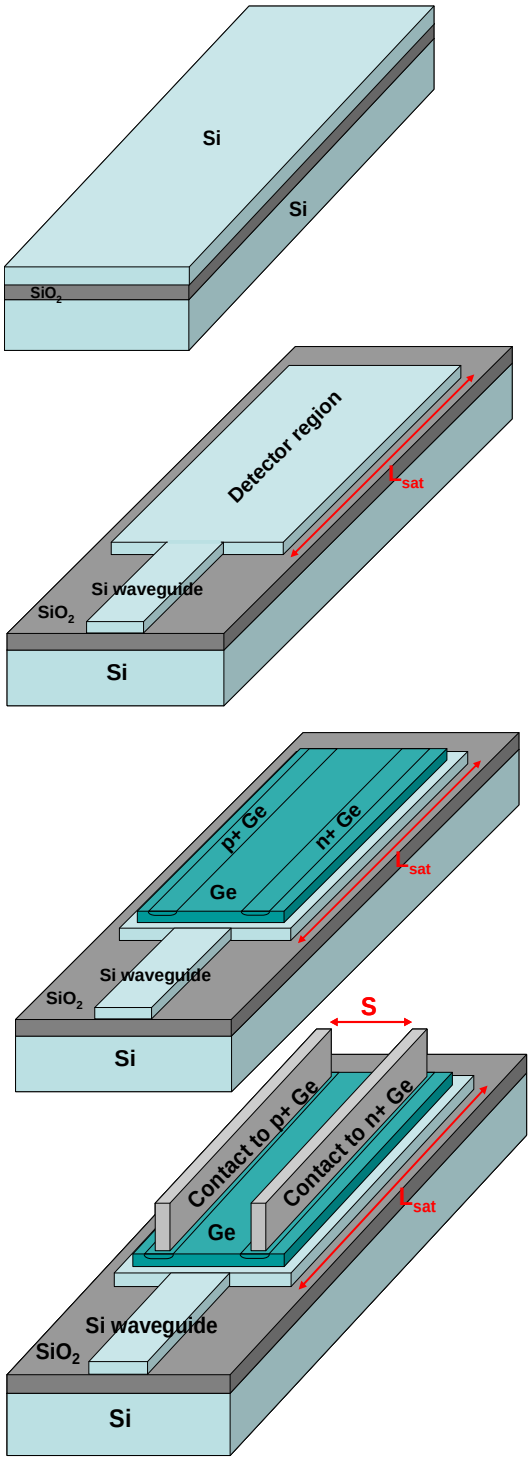


**Fig. 5.3 Schematic of waveguided MGM photodetector fabrication process flow.**

during lithography. After BARC layer etching, waveguide RIE process was carried out. The etch process was controlled by end-point mode and stopped at the $SiO_2$ box layer with a 10% over-etch. After the RIE process, the etched sidewall of waveguide is not very smooth. The roughness of the waveguide sidewalls can increase the waveguide scattering and induce high propagation loss. To overcome this issue, thermal oxidation of 3 nm and oxide wet etching by HF acid were carried out for waveguide sidewall smoothing. This method was reported previously to be effective in reducing the propagation loss [5.2]. Fig. 5.4 shows the SEM image of a fabricated waveguide tip after smoothing process. The tip width is ~200 nm, and waveguide height is also 200 nm. It can be seen that the waveguide etching profile is almost vertical, and the sidewalls are fairly smooth. After waveguide formation, $SiO_2$ (~120 nm) was deposited by PECVD and patterned for selective Ge growth window. For window open process, dry etch followed by wet etch was adopted to preserve a good interface for Ge epi-growth. The wafers were cleaned in SC1, diluted HF acid (1:200) and immediately loaded in an UHV-CVD. After pre-bake, a Si seed layer (~10 nm, 500 °C), $Si_{0.8}Ge_{0.2}$ (~25 nm, 350-400 ˚C) buffer layer, low-temperature Ge seed (~30 nm, 400 ˚C), and high-temperature Ge (~270 nm, 600 ˚C) were sequentially deposited in the previously patterned windows selectively. In Fig. 5.3, it can be seen that the coupling approach is vertical coupling mode. The Ge regions were patterned and implanted with As/$1\times10^{15}$ $cm^{-2}$/12 keV in the n-type electrode area and $BF_2$/$1\times10^{15}$ $cm^{-2}$/12 keV in the p-type electrode area. Then PR was striped, and wafer was cleaned for residual removal. After oxide deposition (~320 nm) by PECVD, patterning and contact etching, ~20 nm Ni was deposited by sputtering for NiGe electrodes formation. Wafer was annealed at 350 ˚C for 40 sec by RTP for germanidation. Un-reacted Ni was removed by nitric acid (15 %). The metallization process was done by Al deposition, patterning and dry etching. After

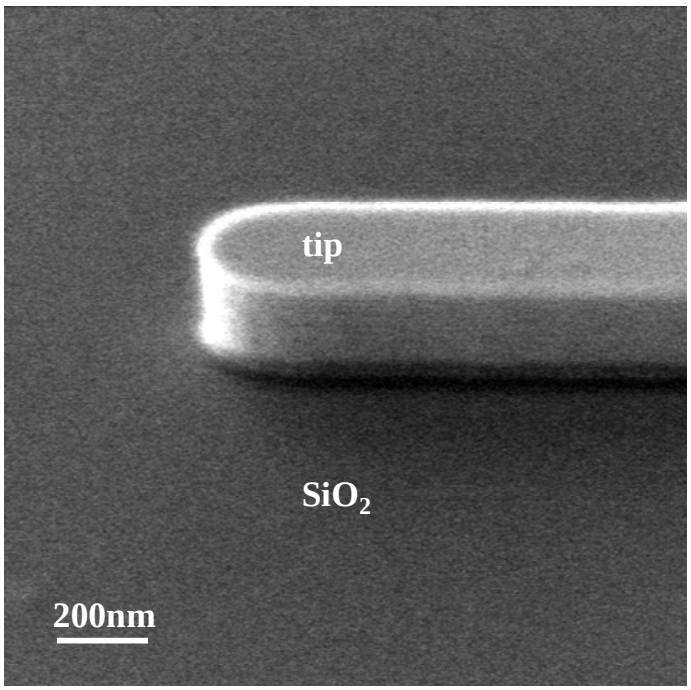


**Fig. 5.4 SEM image of a SOI waveguide tip.**

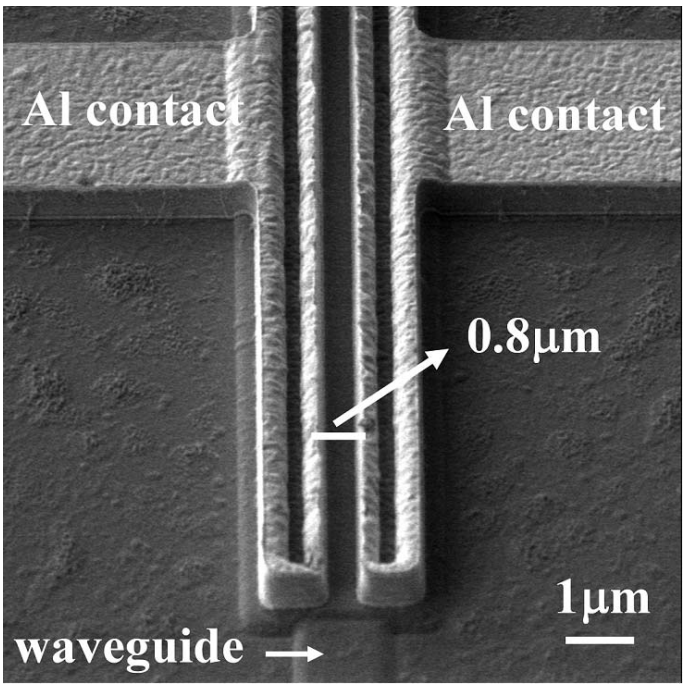


**Fig. 5.5 SEM image of a waveguided photodetector with contact spacing of 0.8 μm.**

Al etching, the device was passivated with $SiO_2$ of 1 μm to prevent waveguide light leakage. Finally, wafer was patterned and etched for metal pad opening. Fig. 5.5 shows the SEM image of a waveguided MGM photodetector before $SiO_2$ passivation. The spacing between metal contacts is 0.8 μm, detector length is 20 μm and the waveguide width is 600 nm.

## 5.2.2 Sample Preparation

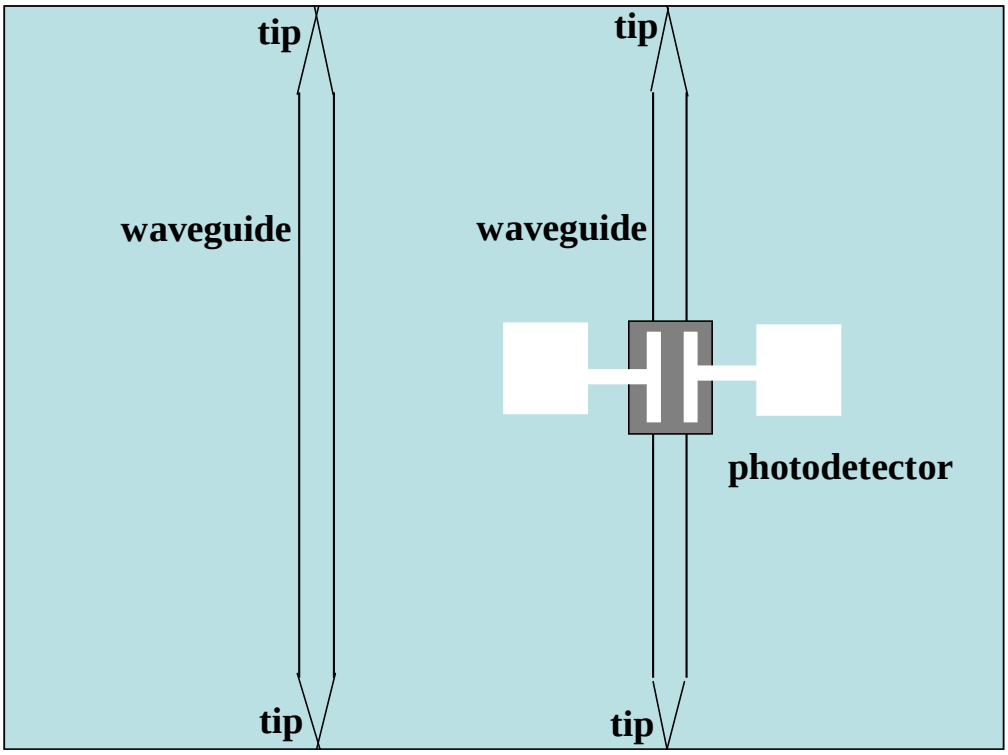


**Fig. 5.6 Schematic of polished device wafer.**

For surface-illuminated photodetectors, device characterization can be carried out immediately after device fabrication. Compared to surface-illuminated detector,

waveguided photodetector characterization is more complex. First, a device preparation procedure is needed. In waveguide photodetectors, optical signals from fiber are coupled into waveguides through side-illumination. Therefore, device wafer needs to be cut at the edge of waveguide. Fig. 5.7 shows the schematic of a prepared devices wafer. First, wafer was cut using dicing machine with the cutting edge near the waveguide coupling tip. A distance of several microns from cutting line to waveguide tip was set aside to prevent waveguide coupler broken. Each waveguide has two tip couplers. Therefore, device wafer was cut into a square with two sides near the couplers. After dicing, the wafer side wall is very rough and needs polishing. The side wall polishing was done on a rotating polishing machine. The polishing process was monitored using a microscope and controlled manually. The polished edge should be as near as possible to the waveguide coupler.

## 5.2.3 Measurement Setup

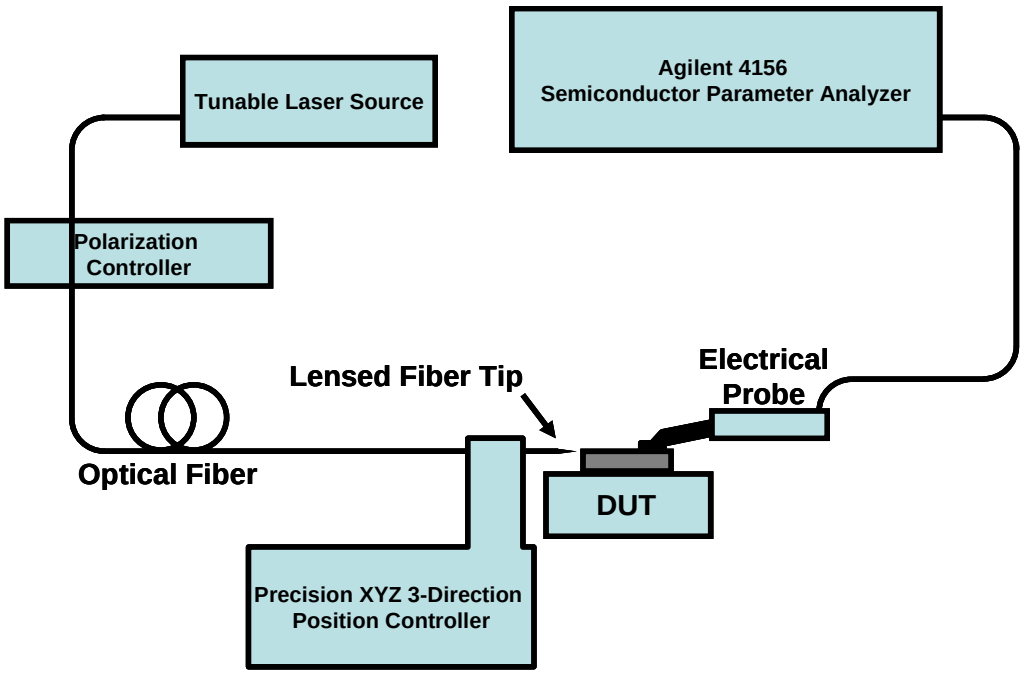


**Fig. 5.7 Schematic of waveguided photodetector measurement setup.**

The waveguided photodetector measurement is mainly done on an optical bench (Fig. 5.7). The prepared device was placed on a sample holder with backside vacuum. The device was probed by electrical probe tips and signal feedbacks to an Agilent 4156 parameter analyzer. Tunable laser source with polarization controller provides the laser of wavelength of 1550 nm. The laser was coupled into on-wafer waveguide through an optical fiber. Before measurement, the device position was adjusted to make sure that the direction of waveguide is parallel to the optical fiber. As mentioned previously, the device was diced and polished near the waveguide coupler. The laser will be coupled from optical fiber to waveguide through the tip coupler. The optical fiber was controlled by a 3-direction position controller. During optical fiber adjustment, the photocurrent of the photodetector at a constant bias was monitored by parameter analyzer. The photocurrent varies during optical fiber position adjustment since the coupled laser energy varies with position. The fiber position is optimized when the photocurrent reaches maximized value. After fiber adjustment, the photocurrent of photodetector at bias was measured.

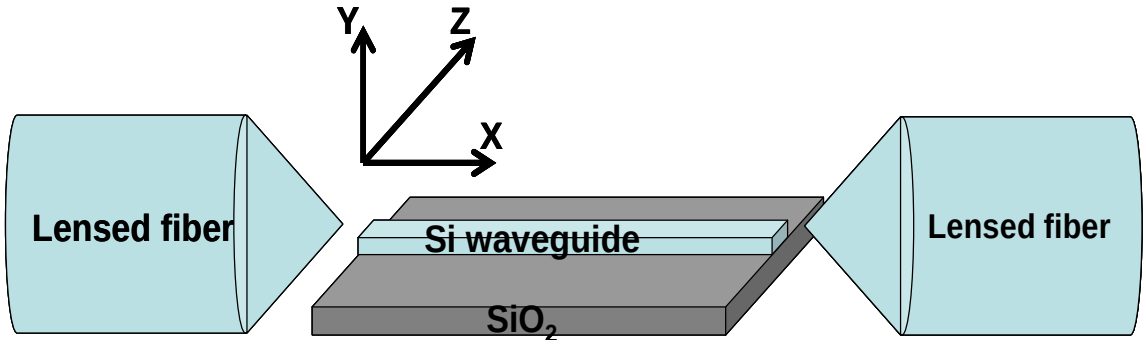


**Fig. 5.8 Schematic of waveguide measurement setup.**

For responsivity measurement of surface-illuminated photodetectors, laser power can be directly measured by an optical power meter. For waveguide photodetectors, the power measurement is more complex. Before optical signals reach the photodetectors, the laser experiences an optical energy loss. There are two major components for the energy losses in measurement. The first part is the coupling loss during the laser coupling from fiber to waveguide through tip coupler. The other part is the propagation loss during laser propagation in waveguide. The total waveguide loss is measured in units of dB. Fig. 5.8 shows the schematic waveguide loss measurement setup. In Fig. 5.6, it can be seen that a waveguide with the same dimension was designed beside the waveguided photodetector for waveguide loss characterization. Before waveguide measurement, the laser energy ($P_{in}$) was measured by optical meter. In waveguide measurement, two optical fibers were used for laser coupling in and out. There is an optical power meter connected to the coupling-out fiber to monitor the laser energy. After optical fibers position adjustment, the laser energy in the coupling-out fiber ($P_{out}$) is measured. Therefore, the combination of coupling loss and propagation was calculated by the formula:

$$Loss=10log_{10}(P_{out}/P_{in}) \quad (5.2)$$

## 5.3 Results and Discussion

Fig. 5.9 compares the dark current between the MGM photodetectors with and without np-DS in the NiGe contact electrodes. The detector length is 20 μm. The MGM photodetector without np-DS shows a rather high dark current. The MGM photodetector with DS-NiGe shows a dark current of $4.4 \times 10^{-5}$ A at -1 V, which is about ~3 orders of magnitude lower than that of the corresponding non-DS-MGM photodetector. The result is consistent to those in previous chapters. Fig. 5.9 also

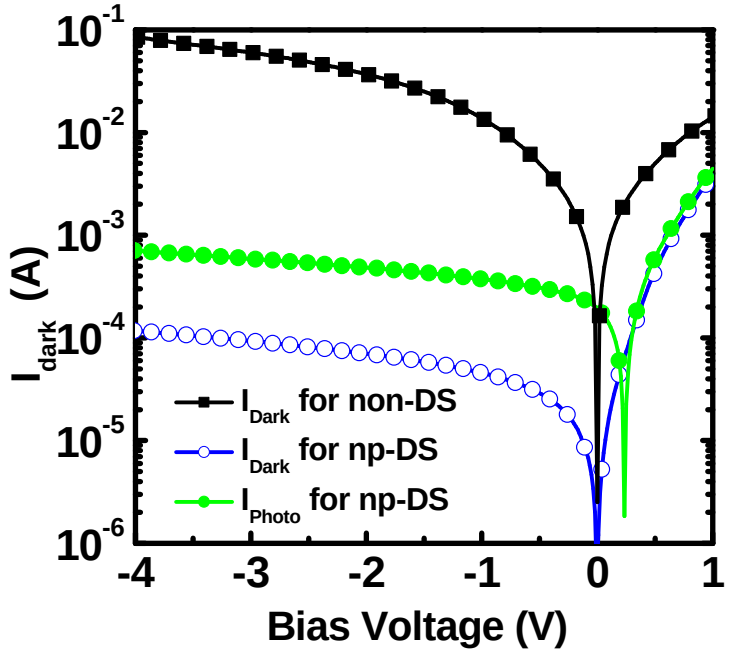


**Fig. 5.9 Dark current comparison between MGM photodetectors with and without np-DS and measured photocurrent at wavelength of 1.55 μm for MGM photodetectors with np-DS.**

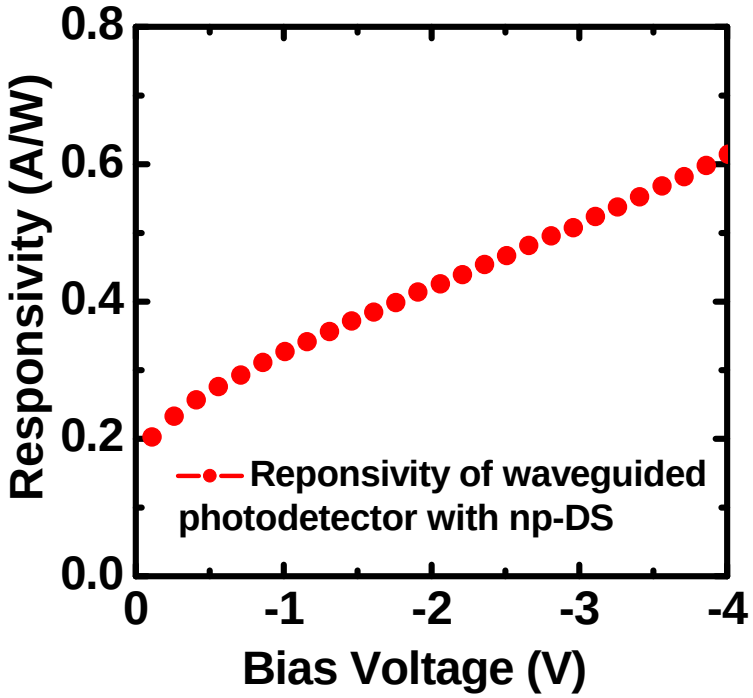


**Fig. 5.10 Responsivity of waveguided np-DS-MGM photodetector versus applied bias.**

shows the photocurrent of MGM photodetector with np-DS at wavelength of 1.55 μm. The laser is coupled into the detector from the waveguide in vertical coupling mode. The fiber-waveguide coupling loss and waveguide propagation loss at 1.55 μm were characterized to be -4.8 dB on the reference waveguides with identical size in the same die (Fig. 5.6). The power which reaches the detector region is extracted to be ~115 μW. The responsivity of the MGM photodetector is 0.17 A/W at 0 V, 0.33 A/W at –1 V and 0.6 A/W at -4 V. It should be noted that conventional MSM photodetectors without dopant segregation can only work at non-0-V biased conditions since the two metal electrodes possess the same work function, thus there is no electric field in Ge active region under 0-V biased condition. The n- and p-dopants segregated in two NiGe electrodes created a built-in electrical field around the detector active region. Compared to the responsivity of the surface-illuminated photodetector with the same Ge thickness in Chapter 4, the responsivity of waveguided photodetector is much higher. Waveguided photodetectors are intrinsically superior to surface-illuminated photodetectors in detection efficiency. The first reason of the high responsivity is that the responsivity of waveguided photodetector is not highly thickness dependent. Due to the side-illuminated configuration of waveguided photodetector, the effective absorption length of guided optical signal is the length of photodetector (20 μm) rather than the thickness of Ge layer (300 nm). Secondly, the photo energy loss due to the metal contact absorption in waveguided photodetector is much less than that in surface-illuminated photodetector. Therefore, the responsivity of the waveguided photodetector is much higher than that of the surface-illuminated photodetector with the same Ge thickness.

Fig. 5.11 shows the temporal response of the photodetector with 0.8 μm contact spacing. The obtained FWHM of the temporal response is 18 ps at 0 V and 17 ps at

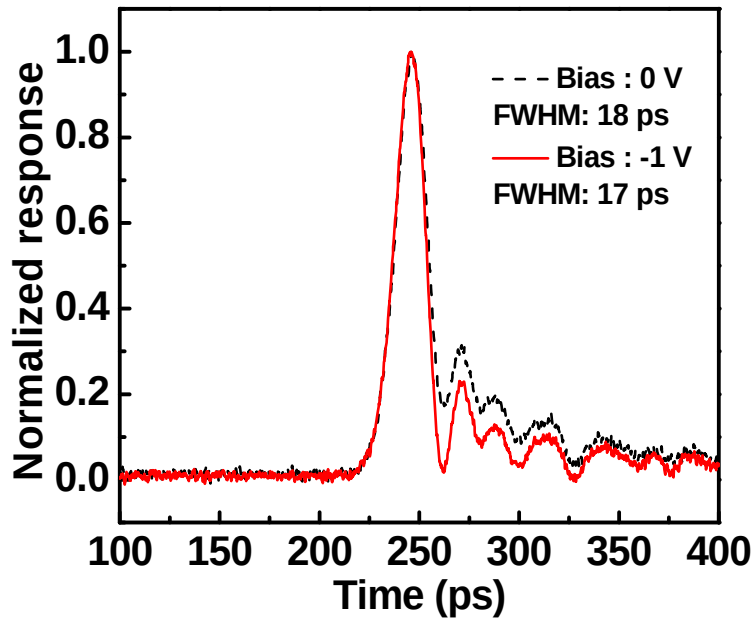


**Fig. 5.11 Temporal response of MGM photodetector with np-DS at 0 V and –1 V bias to an 80 fs laser pulse at wavelength of 1.55 μm.**

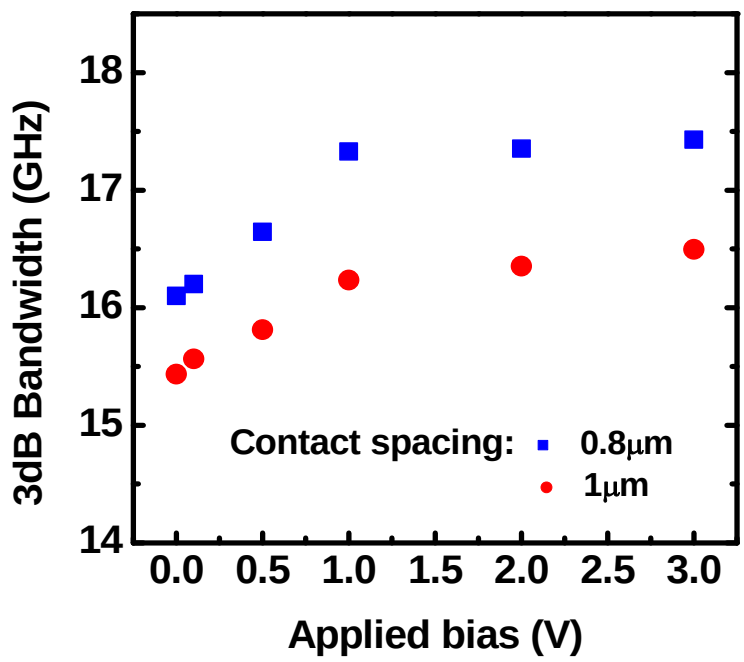


**Fig. 5.12 3dB bandwidth of waveguided MGM photodetector with np-DS as a function of reverse bias.**

at -1 V. It can be observed that there are several secondary peaks after the main temporal response peak. The secondary peaks are electrical reflections resulting from impedance mismatching between the detector and the measurement system [5.3]. The electrical reflection peak will degrade the bandwidth extracted by fast Fourier transform. Since the peaks were induced by the measurement system, the reflections peaks were neglected in bandwidth extraction. Fig. 5.12 shows the extracted 3 dB bandwidth of np-DS-MGM photodetectors with different contact spacing versus device bias. The photodetector with small contact (0.8 μm) spacing shows higher bandwidth due to the smaller carrier drift length. The photodetector with contact spacing of 0.8 μm shows a bandwidth up to 17.5 GHz at -1 V bias. It can be seen that, compared to the surface-illuminated photodetector, the waveguided photodetector achieved significant enhancements in both bandwidth and responsivity simultaneously.

In addition, the MGM photodetector with np-DS exhibits a fast pulse response of 18ps at 0V. The capability of high-speed operation in photovoltaic condition is very desirable for low power consumption and also with high signal-to-noise ratio. As mentioned, conventional MGM detector can not work in 0-V biased condition. The reason why MGM photodetector with np-DS can operate fast under 0-V bias is the $E_{build\text{-}in}$ induced by dopant segregation in NiGe contact. The build-in voltage and average built-in electrical field can be expressed as:

$$V_{build-in} = \frac{kT}{q} \ln \frac{N_n N_p}{N_i^2} \tag{5.3}$$

$$E_{build-in} = \frac{V_{build-in}}{d} \tag{5.4}$$

where k is the Boltzmann constant, q is the unit charge, d is the contact spacing (0.8 μm) and $N_i$ is Ge intrinsic carrier concentration ($2 \times 10^{13}$ $cm^{-3}$). In Fig. 3.5, the SIMS profile shows the concentrations of segregated As and B in NiGe/Ge interface were about $6 \times 10^{18}$ $cm^{-3}$ and $7 \times 10^{19}$ $cm^{-3}$. By 5.1 and 5.2, the calculated average $E_{build\text{-}in}$ near the DS-NiGe junction is ~8.9 kV/cm. Fig. 5.13 shows the carrier velocity versus different electric field. The corresponding drift velocity of electrons and holes in Ge are $6\times10^6$ cm/s and $5\times10^6$ cm/s [5.4], respectively. Therefore, the drift transit time of electrons and holes in Ge region (0.8 μm) are as short as 13 and 16 ps. It can be seen that there is a saturation velocity ($6\times10^6$ cm/s) for holes and electrons. When the carrier velocity saturates, the bandwidth of photodetector saturates and does not increase with further biasing. In Fig. 5.12, the saturation bandwidth of photodetectors with contact spacing of 0.8 μm and 1 μm is 17.5 GHz and 16.2 GHz respectively. To achieve high-speed operation in 0-V bias, two factors are necessary: 1) high dopant concentration in n- and p- electrodes region for high built-in potential, and 2) the scaling of electrode spacing which affects both built-in electrical field and carrier transit distance. Therefore, there are two approaches to achieve fast response in 0-V bias. The first approach is to increase the dopant concentration, and the other approach is to scale the device contact spacing. Dopant segregation technique is a good technique to create high doping concentration junction, indicating that this technique is very promising for photodetectors for low stand-by power and high bandwidth applications. Besides, it is attractive that the bandwidth of photodetectors with np-DS is in 0-V bias was enhanced by the scaling of contact spacing. We believe that higher bandwidth can be achieved at 0-V bias through further scaling of contact spacing. In addition, the saturated bandwidth can be achieved at 0-V bias since the $E_{build\text{-}in}$ can be increased through further contact spacing scaling.

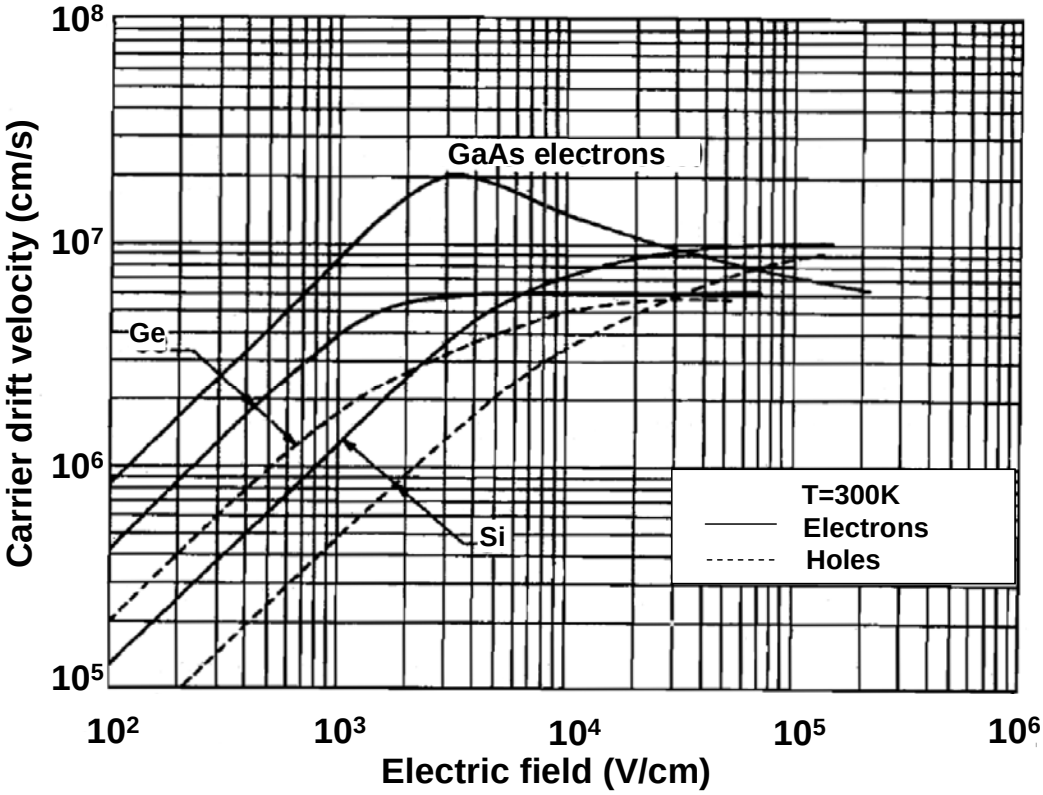


**Fig. 5.13 Carrier velocity versus electric field at room temperature [5.4].**

Table 5.1 compares the device performance of this work with the other published results. From the comparison of device performance in [5.6][5.7][5.8][5.10], it can be seen that MGM detector bandwidth increases with the scaling of electrodes spacing and also conventional MSM detector can only operate in non-0-V biased condition. The p-i-n detectors can work at 0-V biased condition due to the built-in electrical field [5.5][5.11]. With high doping concentration using np-DS technique and the scaled electrodes spacing (0.8μm), the MGM photodetector achieves a bandwidth up to 16 GHz at 0-V bias. Meanwhile, Ge detector still can not be as good as InGaAs photodetector [5.13] and needs further improvement.

**Table 5.1 Partial summary of published photodetectors performance. (SI: surface-illuminated, WG: waveguided)**

| | Structure | Dark current @-1V(A) | Width /Spacing (μm) | Responsivity @λ=1.55μm (A/W) | Power 3dB Bandwidth (GHz) |
|---|---|---|---|---|---|
| [5.7], 1998 | SI- MGM | -- | --/10 | 0.24 (@1.3 μm) | 0.5 |
| [5.8], 2006 | SI -MGM | $1.7 \times 10^{-5}$ | --/5 | 0.5A at -0.1V<br>0.75 at -1V | 1 at -2 V |
| [5.6], 2004 | SI-MGM w α-Ge | $10^{-6}$ | --/2.5 | 0.15 (@1.3 μm) | 2.8 at -2 V;<br>4.3 at -4 V |
| [5.9], 2003 | SI-MGM,SI-M-Si-M | $\sim 10^{-7}$ | 5/5 | 0.3 (@1.48μm ) | -- |
| [5.12], 2002 | SI-Ge p-i-n ( Lateral) | $2 \times 10^{-6}$ | 230 /2.5 | 0.24 at 0 V | 2.2 at -1 V;<br>3.5 at -3 V;<br>3.8 at -5 V |
| [5.5], 2005 | SI-Ge p-i-n (Vertical) | $2 \times 10^{-6}$ | N/A | 0.56 at 0 V | 3 at 0V;<br>8 at -1V |
| [5.11], 2007 | WG-Ge p-i-n (Vertical) | $0.9 \times 10^{-7}$ | N/A | 0.87 | 6.5 at 0 V;<br>7.2 at -1 V |
| [5.10], 2007 | WG MGM | $3 \times 10^{-4}$ | 10/1 | 1 at -6 V | 8.5 at -0.5V;<br>15 at -2V;<br>25 at -6V |
| [5.13] 2005 | WG InGaAs pin (Vertical) | $2\times 10^{-9}$ at-2 V | --/0.3 | 0.5 | 120 at -2.5 V |
| **This work** | **WG-DS-MGM** | **$4.4 \times 10^{-5}$** | **20/0.8** | **~0.17 at 0 V;<br>~0.33 at -1 V;<br>~0.6 at -4V** | **16 at 0 V;<br>17.5 at -1 V;<br>17.5 at -4 V;** |

## 5.4 Conclusion

In conclusion, we demonstrated waveguided np-DS-MGM photodetectors with scaled contacts spacing (0.8 μm) on SOI substrate. Significant enhancements over surface-illuminated photodetector in both detection efficiency and bandwidth were achieved due to the superior configuration of waveguided photodetector. By applying dopant segregation technique, the MGM photodetector shows a fast photo response up to ~18 ps. The device also shows a responsivity of 0.13 A/W under 0-V biased conditions and 0.6 A/W at -4 V bias. In addition, the device contact spacing scaling significantly enhances the detector performance.

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# Chapter 6
# Germanium CMOSFET integration on Silicon Substrate

## 6.1 Introduction

Ge is a promising candidate material to replace Si for MOSFET fabrication because it offers 2.8 times electron mobility and 4 times hole mobility over Si. With the development of high-κ dielectric, Ge MOSFETs with high-κ/metal gate using different passivation methods had been successfully demonstrated with excellent performance [6.1][6.2][6.3]. While previous Ge-channel transistors were dominant on Ge bulk wafers [6.1][6.2][6.3], integration of high performance Ge MOSFET on Si substrate is necessary for the application in Si-based VLSI. On the other hand, integration of Ge photodetectors on Si-based VLSI suffers from the thermal budget incompatibility problem. Si MOSFET fabrication requires high temperature processes up to 900~1000 $^{o}$C such as gate oxidation and source/drain activation. However, Ge photodetector fabrication process is not compatible with such high temperature processes due to the issues of Ge melting and dopant diffusion. If Si MOSFETs in VLSI can be replaced by Ge MOSFETs with high-κ dielectric, the process thermal budget required can be significantly reduced, and the processes for the integration of MOSFETs and photodetectors can be considerably simplified. In this chapter, we investigate and demonstrate Ge n- and p- MOSFETs with $HfO_2$/TaN gate stack integrated on Si substrate. The Ge platform was achieved by the epi-growth method

used for Ge photodetectors fabrication. This work shows a promising solution for future integration of Ge photodetectors and Ge CMOSFETs in OEIC.

## 6.2 Device Fabrication

Devices were fabricated using standard CMOS process flow on 8" p-type Si (100). After SC1 and HF acid (1:200) cleaning, 25 nm-thick $Si_{0.8}Ge_{0.2}$ buffer and Ge of 280 nm was sequentially deposited in a UHV-CVD. After Ge layer growth, the Ge epi-layer was capped with a strained Si layer as gate passivation layer in the same chamber. After epi-growth, the wafer was patterned for transistors wells formation. The wafer was patterned and implanted with B and P respectively for p- and n-well formation. The well activation was done by annealing at 600 ˚C for 10 sec in RTP. After HF acid (1:100) cleaning for native oxide removal, 6 nm $HfO_2$ was deposited by sputtering and annealed at 500 ˚C in an $O_2$ ambient for post-deposition annealing (PDA). Next, TaN of 100 nm was deposited on $HfO_2$ as metal gate material. After TaN deposition, wafer was patterned and etched for transistor gate formation. The gate etching stopped on the $HfO_2$ layer. After gate etching, the $HfO_2$ on source/ drain region needs to be removed. After PDA, $HfO_2$ was crystallized and can not be directly removed by HF acid. A nitrogen ion bombardment was carried out to make the $HfO_2$ layer amorphous, followed by HF acid (1:100) wet etching. After gate stack formation, the wafer was patterned again and implanted with B and P respectively for source/drain formation. After PR strip and wafer cleaning, source/drain activation was

carried out in RTP at 500 ˚C. Transistors with gate length of $L_g$ = 0.5 to 10 μm were fabricated. Fig. 6.1 shows the schematic of the fabricated devices.

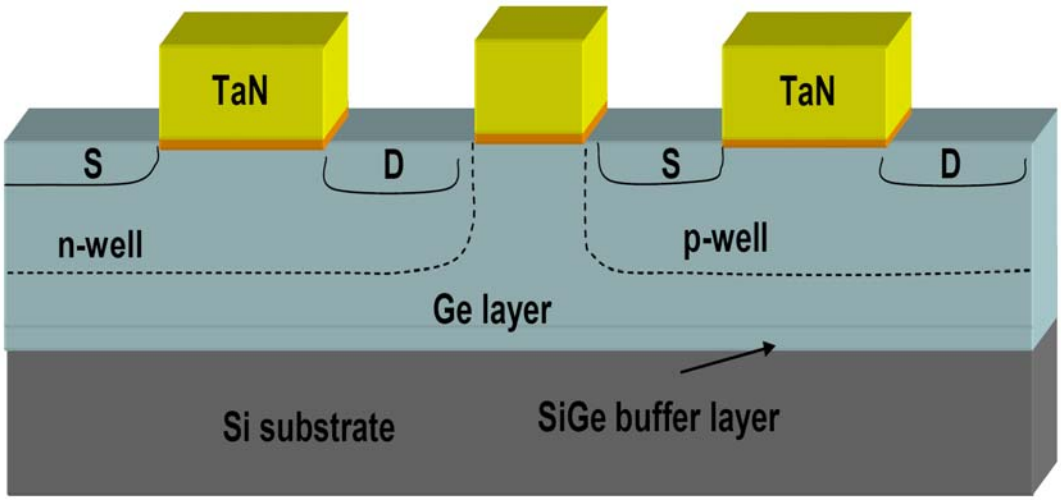


**Fig. 6.1 Schematic of Ge n- and p-MOSFET on Si substrate.**

## 6.3 Results and Discussion

To examine the gate stack and extract the EOT of the $HfO_2$, C-V measurement on the fabricated transistor was done. Fig. 6.2 shows the C-V characteristics of the Ge p-MOSFET. The device was swept from accumulation to inversion. From the C-V curve of Ge p-MOSFET, the EOT extracted by fitting the data to a simulation model is 1.4 nm, indicating a good κ value of the deposited $HfO_2$. Besides, it can be observed that the capacitance of inversion side is lower than that of accumulation side at low voltage. Fig. 6.3 shows a schematic of the band diagram of Ge p-MOSFET. The Si cap and the strong valence band offset of the strained Si/Ge heterostructure are responsible for the capacitance loss in p-MOSFET inversion region [6.4]. When $|V_g|$

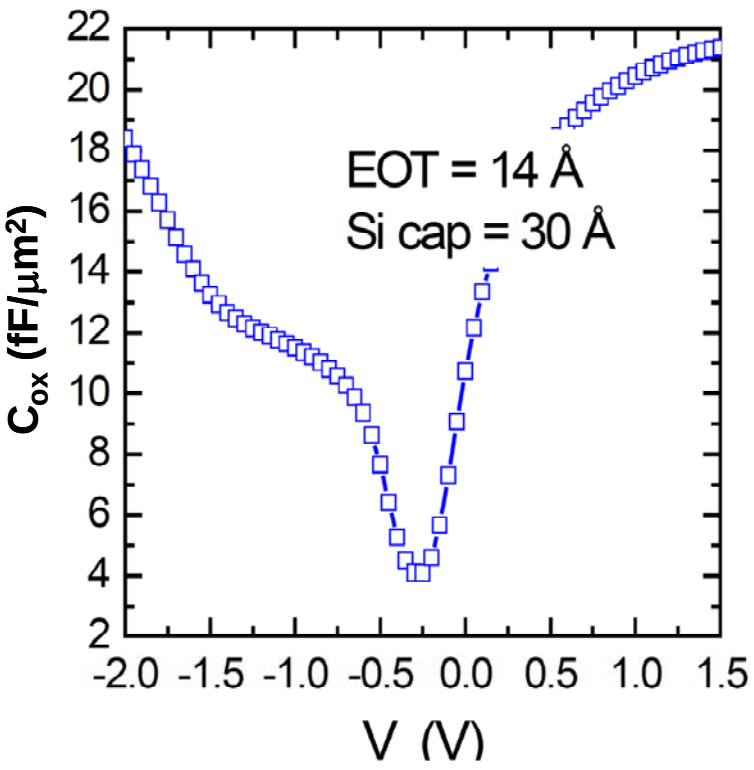


**Fig. 6.2 C-V characteristics for Ge p-MOSFET. $HfO_2$ (6nm) /TaN on Si/Ge shows accumulation EOT of 14 Å.**

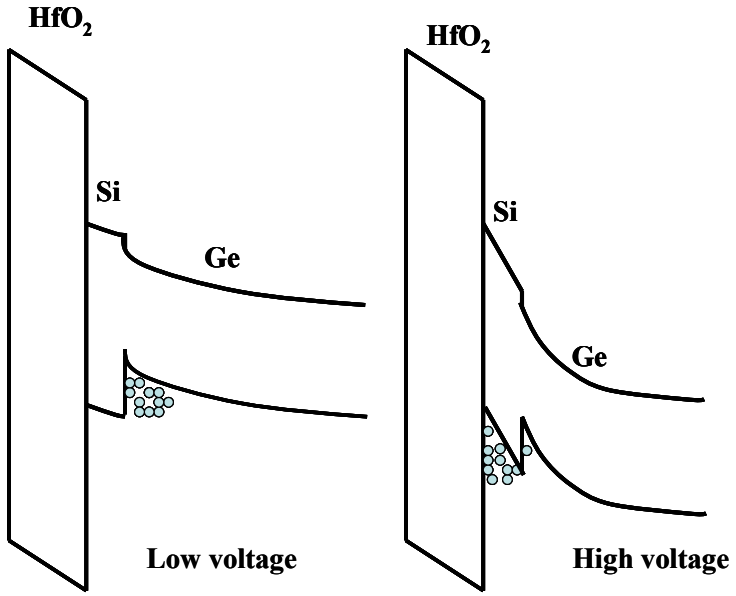


**Fig 6.3 Schematic band diagram of fabricated Ge p-MOSFET in inversion condition.**

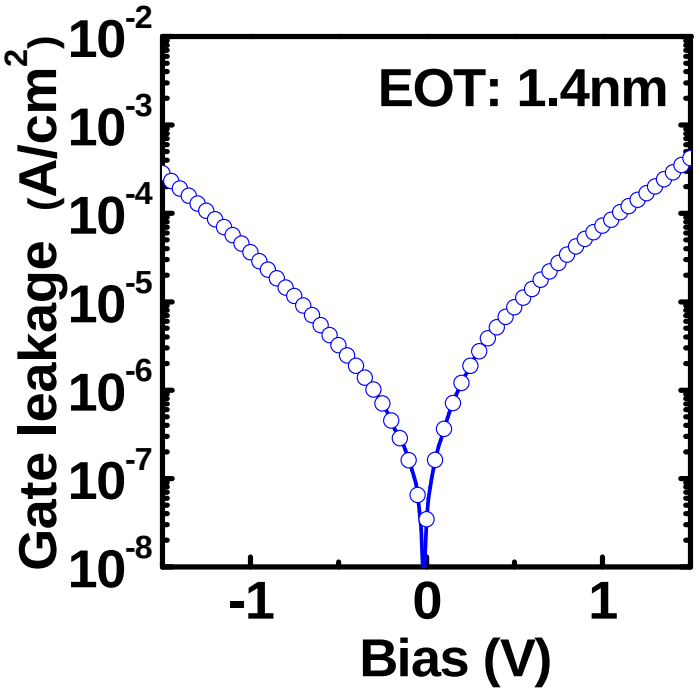


**Fig. 6.4 Gate leakage current density versus applied bias.**

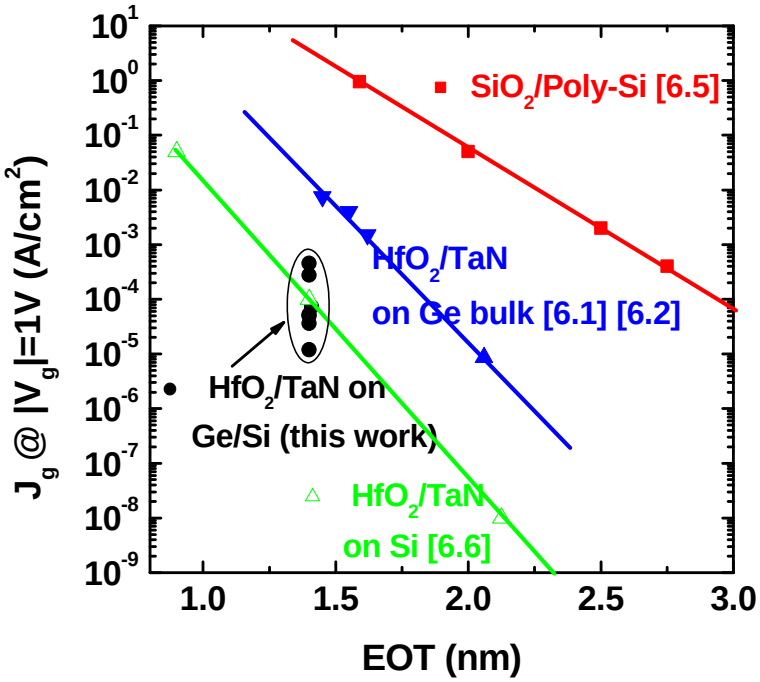


**Fig. 6.5 High-κ gate dielectric leakage current@ $|V_g|$ = 1V as function of EOT.**

($V_g$ > -1.5 V) is low, the inversion holes are confined in Ge by the valence band Offset. When $|V_g|$ is high ($V_g$ < -1.5 V), the holes which are confined in the Ge layer, repopulate in the strained-Si layer, resulting in capacitance recovery. Fig. 6.4 shows the gate leakage current density of Ge MOSFETs. It can be seen that the gate leakage current density is about $2\times10^{-5}$ A/cm$^2$ at -1 V when the EOT of $HfO_2$ is 1.4 nm. Fig. 6.5 shows the leakage current of the $HfO_2$ dielectric on the above mentioned structure, with a benchmarked data from literatures for a comparison. The previously reported gate leakage current of $HfO_2$ on Ge [6.1][6.2] is about 2 orders of magnitude higher than that of $HfO_2$ on Si [6.6]. Si passivation was reported to be one of the best interface passivation methods for $HfO_2$ on Ge [6.1][6.2][6.3]. In this work, due to the in-situ epi-Si passivation on Ge, the leakage current of the $HfO_2$ (EOT: 1.4 nm) is $10^{-4}$ ~ $10^{-5}$ A/cm$^2$ at $|V_g|$ = 1 V, which is comparable with the published $HfO_2$ on Si results [6.6]. Fig. 6.6-6.9 illustrate the DC characteristics of the Ge p- and n-MOSFETs fabricated on Si/SiGe/Ge substrate. Fig. 6.6 is the $I_d$-$V_d$ characteristic of the Ge p-MOSFET with a gate length of 5μm. The $I_d$-$V_d$ curves of the Ge p-MOSFET show an excellent performance as expected. The extracted threshold voltage ($V_{th}$) is -0.35 V for p-MOSFET. The driving current is ~20 μA/μm where gate over drive $|V_g - V_{th}|$ is -1.2 V. For n-MOSFET, the $V_{th}$ is extracted to be 0.25 V. The driving current for the n-MOSFET with of 5μm gate length is ~10 μA/μm at $|V_g - V_{th}|$=1.2 V which is only half of that in the p-MOSFET with the identical device dimension. There are several reasons which are responsible for the relatively lower drive current for the n-MOSFET. For the p-MOSFET, the channel region is in Ge layer due to the strong

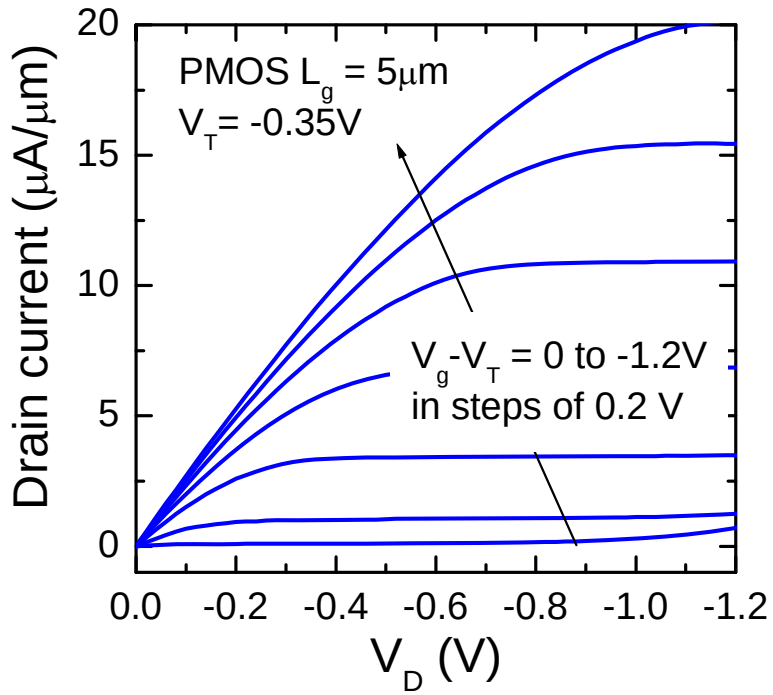


**Fig. 6.6 $I_d$-$V_d$ characteristics for fabricated Ge p-MOSFET on Si substrate.**

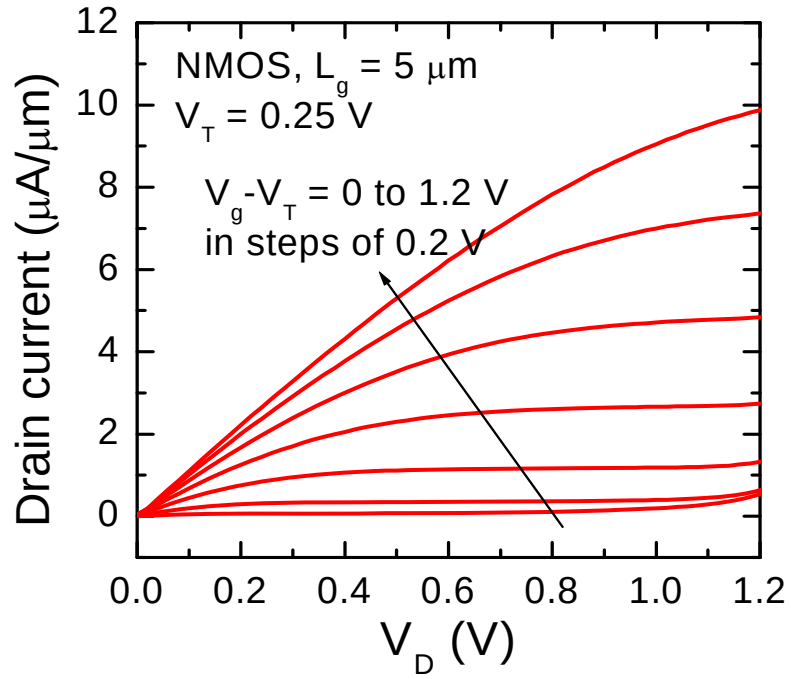


**Fig. 6.7 $I_d$-$V_d$ characteristics for fabricated Ge n-MOSFET on Si substrate.**

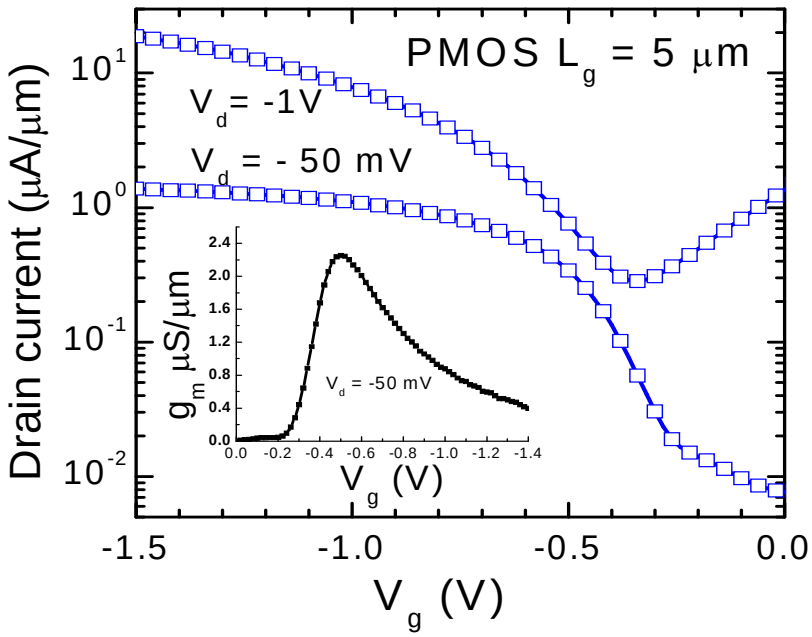


**Fig. 6.8 $I_d$-$V_g$ characteristics for Ge p-MOSFET on Si substrate. The insert shows corresponding $g_m$ for $V_{DS}$ = - 50 mV.**

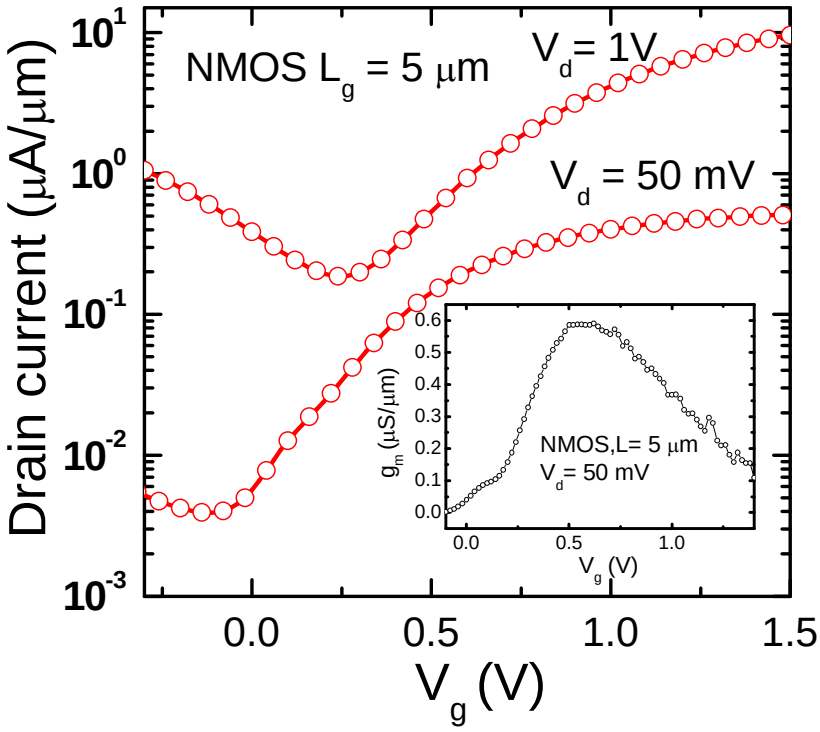


**Fig. 6.9 $I_d$-$V_g$ characteristics for Ge n-MOSFET on Si substrate. The insert shows the $g_m$ for $V_{DS}$ = 50 mV.**

valence band offset of s-Si/Ge heterostructure as shown in Fig. 6.3. However, in s-Si/Ge heterostructure, the conduction band for Ge and Si is almost aligned, which means that there is no offset in conduction band. Therefore, the channel for the n-MOSFET is in s-Si rather than Ge, which is partially responsible for the lower driving current. The Si capping layer should be optimized for the tradeoff between gate leakage current and drivability. In addition, the $I_d$-$V_d$ curve of the n-MOSFET shows a dampening in the linear region compared to that of Ge p-MOSFET. This suggests a considerable series resistance in the n-MOSFETs source and drain region. This is mainly due to the low activation temperature (500˚C) for n-MOSFETs. The high diffusivity and low solubility of n-type dopant in Ge make low resistant source/drain formation very challenging [6.3]. Therefore, the high series resistance due to in-sufficient source/drain activation is another reason for the low driving current of n-MOSFET. However, higher activation temperature can degrade the gate stack. In addition, high temperature annealing will induce P fast diffusion, resulting in low doping concentration in source/drain region. Lastly, it is discussed that the Fermi-level pinning between metal and Ge is always near to the valence band rather than conduction band. Therefore, the contact resistance between probe tip and source/drain in n-MOSFET is always higher than that in p-MOSFET.

Fig. 6.8 and 6.9 shows the $I_d$-$V_g$ plots of the Ge p- and n-MOSFETs. The insets are the transconductance ($g_m$) when drain voltage is -0.05 V or 0.05 V. The off-state leakage current at $|V_d|$=0.05 V is in the order of $10^{-2}$ μA/μm for p- MOSFETs. The $I_{on}/I_{off}$ ratio is about 2 orders of magnitude. The poor $I_{on}/I_{off}$ ratio is mainly attributed

to the threading dislocations in the Ge epi-layer. The threading dislocations lead to a high junction leakage. Therefore, the threading dislocations density in Ge epi-layer needs to be further reduced to improve the $I_{on}/I_{off}$ ratio. Fig. 6.9 shows the $I_d$-$V_g$ plots for the Ge n-MOSFET. For the n-MOSFET, the off-state leakage current at $|V_d|$=0.05 V is in the order of $10^{-3}$ μA/μm. The $I_{on}/I_{off}$ ratio is also about 2 orders of magnitude. For both n- and p-MOSFET, gate induced drain leakage current (GIDL) under high drain bias is significant due to the narrow Ge band gap, resulting in higher carrier band-to-band tunneling [6.9].

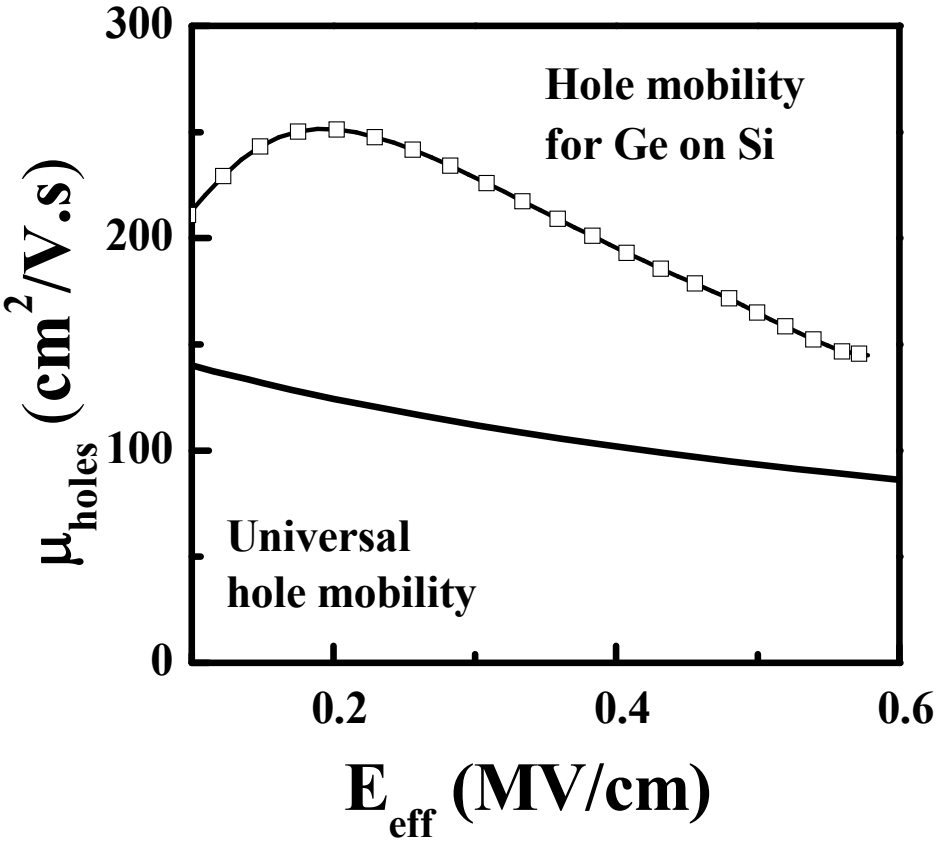


**Fig. 6.10 Extracted hole mobility for Ge p-MOSFET measured using split CV method. 2 times hole mobility is achieved as compared to Si universal mobility.**

Lastly, hole mobility is extracted using split C-V method. The hole mobility is calculated by $\mu_{hole} = \frac{I_d L}{Q_{inv} V_{ds} W}$, where $Q_B$ and $Q_{inv}$ are the deletion charge and the inversion charge respectively. Channel vertical electrical field was calculated by $E_{eff} = \frac{Q_B + \frac{1}{3} Q_{inver}}{\kappa_{Ge} \varepsilon_o}$, where $\kappa_{Ge}$ is the Ge dielectric constant, and $\varepsilon_o$ is the permittivity of vacuum. Ge channel shows higher hole mobility up to 100% enhancement compared to Si universal hole mobility. The epi-Ge on Si shows a better hole mobility compared to previously published Ge bulk results [6.1][6.2]. The high hole mobility is partially attributed to the in-situ Si passivation. Similar hole mobility (2 times) is obtained using 1.6nm $SiO_2$ as passivation layer [6.10], but the $SiO_2$

**Table 6.1 Summary of Ge p-MOSFETs performances with different hetero-structures and bulk substrate.**

| Transistor structure | $L_g$ (μm) | EOT (Å) | $J_g$@ Vg=1V (A/cm$^2$ ) | $\mu_{hole}$ (cm$^2$/V.s) |
|---|---|---|---|---|
| Ge bulk p-MOS with HfON dielectric [6.3] | 20 | 20.6 | $10^{-5}$-$10^{-6}$ | 130 |
| Ge on Si p-MOS with GeON/$SiO_2$ [6.8] | 6 | 140 | N.A. | 95 |
| s-Ge on r-SiGe buffer with $HfO_2$ [6.4] | ≤ 0.2 | 14 | $10^{-3}$ | ≥ 490 |
| Bulk Ge / s-Ge on Si with $HfO_2$ [6.7] | 3 | 16 | $10^{-7}$-$10^{-6}$ | 135/160 |
| **s-Ge on Si p-MOS with $HfO_2$ (This work)** | **0.5** | **14** | **$10^{-4}$-$10^{-5}$** | **250** |

significantly increases EOT, thus degrades the current drivability.

Table 6.1 shows a summary of device performances for Ge p-MOSFETs on Ge bulk and on Si. The epi-Ge on Si in this work shows better hole mobility compared to Ge bulk but is inferior to the ultra-thin Ge on Si superlattice [6.4]. This is however mitigated by the improved leakage and simple integration of dual channel n-and p-MOSFETs on Si/SiGe/Ge hetero-structure.

## 6.4. Conclusion

Ge CMOSFETs with high-κ dielectric/metal gate were successfully demonstrated based on the epi-growth technique used for photodetectors fabrication. Due to the high-quality Ge growth and the in-situ Si passivation on Ge surface, a very low EOT of 1.4 nm was achieved, and the gate leakage current density of $HfO_2$ (EOT: 1.4 nm) is $10^{-4}$ ~$10^{-5}$ A/cm$^2$ at $|V_g|$ = 1 V, which is 2 orders of magnitude lower than that of previously reported results of $HfO_2$ on Ge. In addition, Ge p-MOSFET shows 100 % hole mobility enhancement over Si universal mobility.

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# Chapter 7
# Conclusion

This thesis focuses on the research of integration of Ge photodetectors and Ge MOSFETs on Si platform for OEIC. For Ge photodetector, we investigated and optimized MGM photodetector and integrated it with SOI waveguide.

In Chapter 2, the research started with the development of the epi-growth technique for high-quality thick Ge layer on Si substrate using UHV-CVD, which provided the platform for Ge photodetectors and Ge MOSFETs fabrication. We proposed and demonstrated a new epi-growth method by combining two-step Ge growth method with a thin (30 nm) SiGe buffer layer. The Ge epi-layer was characterized using AFM, TEM, SEM and Micro-Raman Spectroscopy. In Ge epi-layer, most misfit dislocations were confined in the interface of Ge/SiGe and low temperature Ge layer. The Ge layer above the low temperature Ge shows a good quality. The threading dislocation density in the Ge epi-layer was characterized to be $6\times10^{6}$ $cm^{-2}$. The roughness RMS of Ge surface is measured to be 0.4 nm by AFM. Raman spectral indicates that the Ge epi-layer on non-patterned wafer experienced a tensile strain up to 0.67 % due to TCE. In addition, selective Ge growth was also achieved on patterned Si wafer which provided a platform for large scale Ge photodetectors integration on Si substrate.

In Chapter 3, to overcome the high dark current issue in MGM photodetectors, we applied dopant segregation technique in MGM photodetectors for dark current

suppression. Four device splits including non-DS, pp-DS, np-DS and nn-DS were designed and fabricated on Si wafer for comparison. The devices were characterized and the results were explained using band diagram. From the results, it can be concluded that hole current injection over SB is the major component of dark current and the segregated As in NiGe/Ge interface which increases the effective hole SBH up to 0.5 eV plays a crucial role in dark current suppression. The np-DS and nn-DS schemes achieved a significant dark current suppression up to 3 orders of magnitude. Although the MGM photodetector with nn-DS shows lowest dark current among the four structures, it shows photocurrent degradation due to the modulated barrier in the low potential contact. Therefore, the MGM photodetector with n and p type dopant segregated in two electrodes respectively is the optimal structure for dark current suppression and photocurrent detection.

In Chapter 4, high-speed surface-illuminated MGM photodetectors with np-DS were fabricated and fully characterized. The MGM photodetector with np-DS shows a dark current of $10^{-7}$ A at -1 V, which is ~3 to 4 orders of magnitude lower than that of the MGM photodetector without DS. It is attractive that the dark current suppression effect of dopant segregation technique is more significant in scaled device. The photocurrent was also measured, and the normal incidence responsivity of the photodetector at wavelength of 1.55 μm is extracted to be 0.088 A/W at 0V, 0.12 A/W at -1 V and 0.14 A/W at -2 V. The desirable ability of the device to operate at photovoltaic status was achieved due to the build-in electrical field in detector active region induced by dopant segregation technique. In addition, the device shows a

bandwidth up to 6 GHz at -1V.

In Chapter 5, we demonstrated a MGM photodetector with scaled contacts spacing (0.8μm) integrated with SOI waveguide. The fabricated SOI waveguided photodetector was characterized using fiber side-illumination method. The waveguided photodetectors overcome the trade-off between responsivity and bandwidth in surface-illuminated photodetectors and show a fast photo response up to ~17 ps (~17.5 GHz) and a responsivity of 0.6 A/W. In addition, the MGM photodetector with np-DS exhibits a fast pulse response of 18ps at 0 V due to the high $E_{build\text{-}in}$ induced by dopant segregation technique. There are two factors which lead to the high-speed operation in 0-V bias: 1) high dopant concentration in n- and p-electrodes region for high built-in potential, and 2) the scaling of electrodes spacing which affects both built-in electrical field $E_{build\text{-}in}$ and carrier transit distance. With the high doping concentration induced by dopant segregation technique and the scaled contact spacing of 0.8 μm, an $E_{build\text{-}in}$ of 8.9 kV/cm in Ge active region was achieved, which leads to a high-speed operation in 0-V bias. Therefore, dopant segregation is a very promising technique for large bandwidth and low stand-by power consumption photodetectors application.

In Chapter 6, Ge n- and p-MOSFETs with $HfO_2$/TaN gate stack integration on Si substrate were demonstrated using the Ge growth method which was used for the Ge photodetectors fabrication. An in-situ Si passivation on Ge surface was also introduced in transistor fabrication. Due to the in-situ epi-Si passivation on Ge, a low EOT of 1.4 nm was achieved, and the leakage current density of $HfO_2$ (EOT: 1.4 nm)

is $10^{-4}$ ~$10^{-5}$ A/cm$^2$ at $|V_g|$ = 1 V, which is 2 orders of magnitude lower than that of previously reported $HfO_2$ on Ge results. In addition, the Ge p-MOSFET shows a good drivability, and the hole mobility extracted using split CV method is 100 % higher than Si universal mobility. The driving current of the n-MOSFET is lower compared to the p-MOSFET due to higher source/drain resistance and contact resistance.

There are several aspects which we should study in future work. First, although Ge CMOSFETs were demonstrated on Si substrate, it is obvious that the drivability of Ge n-MOSFET is still lower than that of its Si counterpart. Further study of Ge n-MOSFETs should be addressed in future work. Secondly, the Ge epi-layer quality needs to be further improved for enhancing the channel mobility and $I_{on}/I_{off}$ ratio. Lastly, the Ge MOSFETs in this thesis are all long-channel transistors, and Ge CMOSFETs with channel lengths under 100nm should be studied and investigated in future work.

## LIST OF PUBLICATIONS


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