DESIGN OF LOW POWER CMOS UWB TRANSCEIVER ICS

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Abstract

Two non-coherent UWB transceivers for wireless sensor networks are proposed in this thesis, namely the low power burst mode transceiver and the burst mode super regenerative transceiver. Both transceivers have simple architecture and low power consumption. Power consumption can be significantly reduced with gating circuitries to switch on/off the transceiver.

The transceiver blocks were implemented in 0.18-µm CMOS technology. A low noise amplifier was designed for high gain of over 40 dB to compensate the squarer loss. A squarer with 40 dB conversion gain was designed to capture signal energy. In the limiting amplifier, a cascade of 5 stages with offset cancellation was employed to achieve 60 dB gain with a bandpass characteristic of 288 kHz to 1 GHz. A new super regenerative UWB detector was designed to achieve large gain with minimum circuit blocks through positive feedback. It can achieve rail-to-rail amplification for UWB input of 26 mV peak-to-peak.

Keywords: Ultra-Wideband (UWB), low power, transceiver, low noise amplifier, super regenerative, burst mode.

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g_m	Transconductance of MOS transistor
I_D	Drain Current of MOS transistor
μ	Carrier mobility of MOS transistor
C_{ox}	Gate oxide capacitance per unit area
W	Width of MOS transistor
L	Length of MOS transistor
V_{GS}	Gate-source voltage of MOS transistor
V_{th}	Threshold voltage of MOS transistor
ω_T	Unity gain frequency
AC	Alternating Current
ASK	Amplitude Shift Keying
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BPM	Bi-Phase Modulation
CMOS	Complementary Metal-Oxide Semiconductor
CDR	Clock and Data Recovery
DA	Driver Amplifier
DC	Direct Current
DS-UWB	Direct Sequence Ultra-Wideband
FCC	Federal Communications Commission
FSK	Frequency Shift Keying

IF	Intermediate Frequency
IME	Institute of Microelectronics
LA	Limiting Amplifier
Mbps	Mega bits per second
MOS	Metal-Oxide Semiconductor
NMOS	Negative Channel Metal-Oxide Semiconductor
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off Keying
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PMOS	Positive Channel Metal-Oxide Semiconductor
PPM	Pulse Position Modulation
PSK	Phase Shift Keying
QFN	Quad Flat No-lead
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RX	Receiver
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
TIA	Trans-Impedance Amplifier
TX	Transmitter
UWB	Ultra-WideBand
VCO	Voltage-Controlled Oscillator

VGA	Variable Gain Amplifier
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

Chapter 1

Introduction

1.1 Background on UWB System

Ever since the release of unlicensed use of UWB by the Federal Communications Commission (FCC) in 2002, the fields of wireless communications, imaging and vehicular radar systems as an example, have seen great and increasing research interest in harnessing UWB technology [1]. One of the most promising applications is in the area of Wireless Personal Area Network (WPAN) systems, ranging from low (IEEE 802.15.4a [2]) to high data rates (up to 480 Mbps at a 4-m distance) (IEEE 802.15.3a [3]) communications. According to FCC regulation [4], UWB transmission for such communication devices is permitted within the frequency spectrum of 3.1-10.6 GHz. A UWB spectral mask for indoor and handheld devices is as shown in Fig. 1.1. In addition, a UWB signal must have a fractional bandwidth of at least 0.2 or bandwidth of at least 500 MHz (regardless of fractional bandwidth).

The main reasons for the popularity of UWB lie in its ability of data transmission over a large bandwidth at very low power (below -41 dBm/MHz), thus causing minimal interference to other coexisting wireless standards such as the IEEE 802.11 Wireless Local Area Networks (WLAN). According to Shannon's channel capacity formula,

$$\text{Capacity} = \text{BW} \log_2 (1+\text{SNR}) \qquad (1.1)$$

Data transmission over an increased bandwidth will result in a larger channel capacity as compared to the same increase in Signal-to-Noise Ratio (SNR). Hence, UWB has the

ability to achieve a higher capacity than other available communications standards. In addition, UWB technology has excellent time domain resolution due to its short (sub nanosecond) pulses, making it less susceptible to jamming signals.

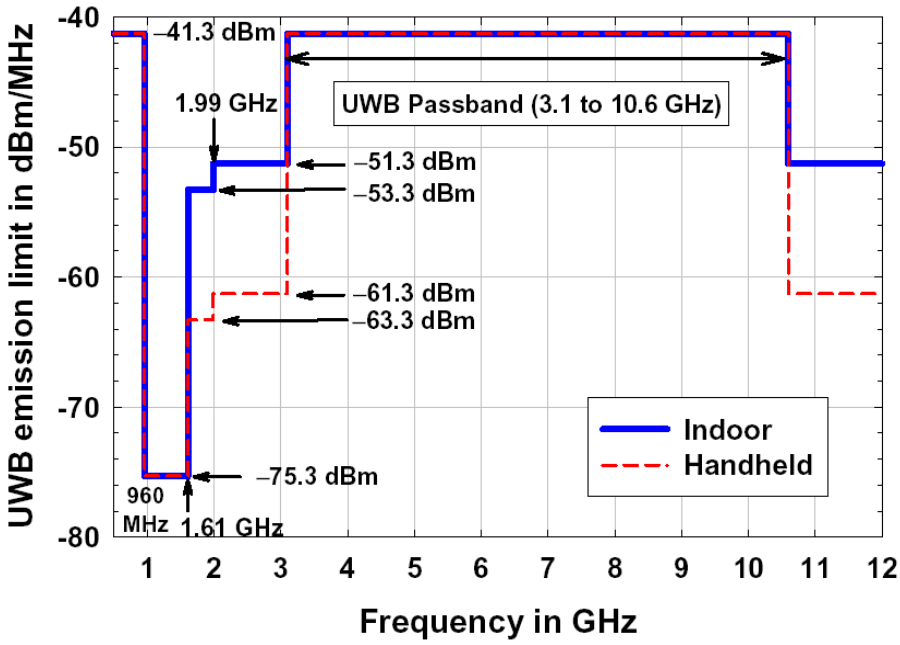


Fig. 1.1: FCC General UWB Emission Limits

There are two main methods to implement the design of UWB radio systems, namely the Orthogonal Frequency Division Multiplexing (OFDM) approach [5]-[7] and Direct Sequence Ultra-wideband (DS-UWB) approach [8]-[10]. The OFDM approach divides the UWB spectrum into many sub-bands, with each occupying 528 MHz of bandwidth. It employs conventional carrier based radio techniques for signal modulation/demodulation and thus resembles a narrowband radio when it is operating in a single sub-band. DS-UWB is a carrier-less approach whereby the system transmits non-sinusoidal wavelets that can either occupy the low-band, high-band or both bands within the UWB spectrum. Examples of wavelets and their corresponding spectrums are as shown in Fig. 1.2 [11].

Under this approach, the spectrum can be efficiently utilised as different users are able to share the entire UWB spectrum simultaneously using the direct-sequence code division multiple access (DS-CDMA) scheme.

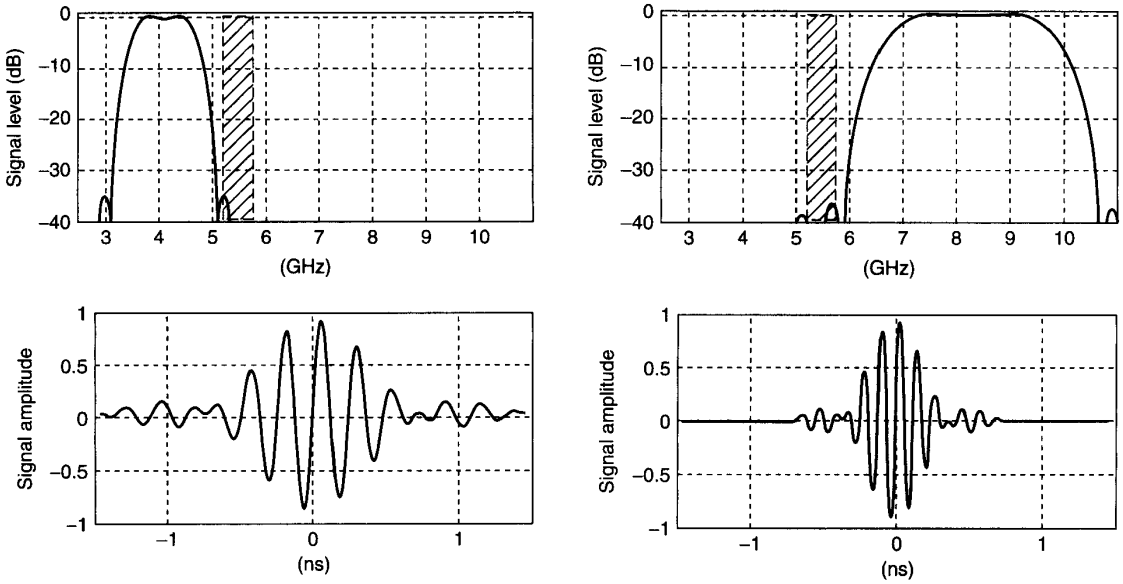


Fig. 1.2: UWB wavelets in the frequency and time domain
(a) 3.1-5 GHz, (b) 6-10.6 GHz [11].

1.2 Motivation

Recently, impulse radio UWB has been a popular choice of technology for low data rate low power applications such as wireless sensor networks [12]-[13] based on IEEE 802.15.4a standard for reasons such as low cost, low power and low complexity. Wireless sensor networks usually consist of many thousands of sensor nodes which transmit data through relays and some of these sensors may be positioned in large remote areas for surveillance and tracking purposes. It is thus imperative to use power and cost efficient transceivers in sensor nodes as it would be impractical and uneconomical to have to replace batteries for the numerous nodes frequently. The choice of impulse radio UWB

technique in low data rate applications presents a potential for even greater power saving as periods of inactivity (no pulse transmission or reception) are very much longer than the nanoseconds width of UWB pulses. In addition, the use of impulse radio approach eliminates the need for up/down conversion of data before transmission since it is essentially carrier-less, thus simplifying the system architecture. The short width of a UWB pulse will also allow its usage for precise localization and ranging purposes in sensor networks.

However, there exist several challenges in the circuit design of a UWB system. Firstly, a wideband RF front end is needed to process the incoming signal. Secondly, the generation of UWB pulses for transmission and limitation of its power level to the FCC regulation are also non-trivial issues. These certainly mean that conventional narrowband circuit blocks cannot be directly applied in wideband architectures, thus new circuit topologies have to be designed and implemented.

In this thesis, the objective is to design a low power CMOS impulse radio UWB receiver (3-5 GHz) that can be implemented in a complete UWB transceiver for low data rate WPAN applications such as in wireless sensor networks. For completeness, the results of the transmitter portion which has been designed by other team members will be summarised in Chapter 4. CMOS is chosen over other technology such as bipolar and SiGe as it is relatively cheaper and more power efficient. In addition, it allows for better system integration with future digital baseband processing blocks, which are commonly implemented using CMOS technology. Various building blocks in the transceiver such as the Low Noise Amplifier (LNA), squarer, limiting amplifier and the super regenerative detector will be investigated and designed.

1.3 Organization

The thesis is organized as follows.

In Chapter 2, conventional transceiver architectures for both narrowband and UWB applications will be presented. The common modulation/demodulation schemes will also be presented here.

In Chapter 3, a discussion on the receiver circuit building blocks will be presented. The building blocks include the low noise amplifier (LNA), squarer, limiting amplifier and super regenerative UWB detector. Simulation results for the building blocks will be shown here as well.

In Chapter 4, the two proposed non-coherent transceiver architectures and measurement results will be presented, namely the low power burst mode UWB transceiver and the burst mode super regenerative UWB transceiver.

In Chapter 5, the thesis will be concluded and a short discussion on the possible future works for the transceivers will be presented.

Chapter 2

Conventional UWB Transceiver Architectures

An insight into different modulation schemes and architectures for conventional narrowband transceivers will first be presented here before we study the conventional architecture of UWB systems in the subsequent section. This not only serves as a platform for understanding the UWB system architecture better, but also helps us to recognise the differences and challenges involved in the design of conventional narrowband transceivers and UWB transceivers. Some of the techniques used in narrowband transceivers are employed in UWB systems as well.

2.1 Overview of Narrowband Transceivers

The choice of radio architecture and the modulation scheme is heavily dependent on the required system performance such as its complexity, cost, power and extent of integration. In this section, we will present the different architectures and modulation schemes for narrowband transceivers and investigate their effects on the overall system performance.

2.1.1 Common modulation schemes

In communications, a data stream is usually modulated with a carrier before it can be transmitted. One of the motivations for modulation is to achieve antennas of reasonable gain and acceptable dimensions for mobile devices since the gain is related to the matching between the antenna dimensions and transmission frequency (wavelength). Another reason might be the rules and regulations regarding the allocation of different frequency bands for different signal transmission. In conventional narrowband radio

architectures, the commonly used modulation schemes can be categorised under amplitude modulation, phase modulation and frequency modulation. The modulated time domain waveforms of a binary baseband signal under the different modulation schemes are as shown in Fig. 2.1 [14].

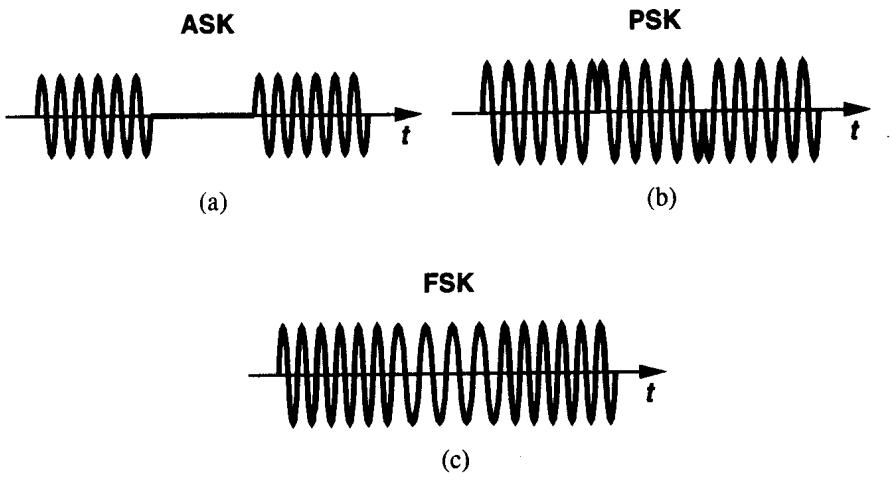


Fig. 2.1: Waveforms of a binary baseband signal under different modulation schemes (a) Amplitude Modulation, (b) Phase Modulation, (c) Frequency Modulation [14].

2.1.1.1 Amplitude Modulation

Amplitude modulated binary signal (Amplitude Shift Keying or ASK) can be defined by the following equation [14]:

$$x_{AM}(t) = A_c\left[1 + mx_{BB}(t)\right]\cos(\omega_c t) \tag{2.1}$$

where A_c is the amplitude of the carrier signal, m is the modulation index, $x_{BB}(t)$ is the binary baseband signal, ω_c is the carrier frequency and t is the time.

Straightforward ASK finds rare usage in today's RF communications systems primarily due to its high susceptibility to noise. In addition, a highly linear power amplifier will be

required in the transmitter [14]. ASK signals can be demodulated using a simple envelope detector.

2.1.1.2 Phase Modulation

Phase modulation (Phase Shift Keying or PSK) and frequency modulation (Frequency Shift Keying or FSK) in digital communications are more commonly used in RF systems since they do not rely on amplitude variations for demodulation and are therefore more robust to noise than amplitude modulation. For a phase modulated signal, the excess phase has to be linearly proportional to the baseband signal. Phase modulation can thus be expressed as follows [14]:

$$x_{PM}(t) = A_c \cos\left[\omega_c t + m x_{BB}(t)\right] \tag{2.2}$$

where the variables used here represent the same as in (2.1). PSK, such as quadrature PSK (QPSK) is usually employed in systems where there is a need to achieve higher data rates in band-limited channels as each symbol can effectively be represented by two bits (four different states).

2.1.1.3 Frequency Modulation

Frequency Shift Keying (FSK), on the other hand, is mainly used for applications that require a lower data rate. Frequency modulated signals can be expressed as follows [14]:

$$x_{FM}(t) = A_c \cos\left[\omega_c t + m \int_{-\infty}^{t} x_{BB}(t) dt\right] \tag{2.3}$$

where the variables used here represent the same as in (2.1). In this case, the excess frequency has to be linearly proportional to the baseband signal.

2.2 Common Narrowband Radio Architectures

2.2.1 Heterodyne Architecture

In heterodyne receivers, a downward frequency translation of the input signal from radio frequency (RF) to a non-zero intermediate frequency (IF) is involved. Frequency translation in the receiver is usually achieved by means of mixing the RF signal with a local oscillator (LO) frequency through the use of a frequency mixer. The useful signal may have to undergo further frequency down-conversions before retrieving it as shown in Fig. 2.2 [14].

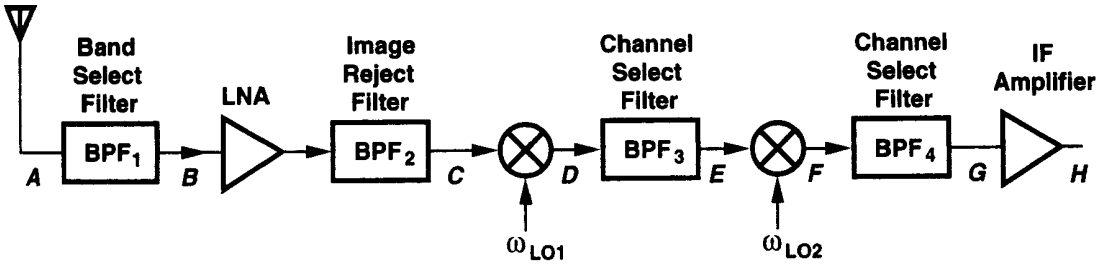


Fig. 2.2: Dual down-conversion heterodyne receiver [14]

In the transmitter, the signal is translated from the IF into the RF through the use of mixers as well. The transmitter in a heterodyne architecture can come in the form of a two-step transmitter [14] where the baseband signal is translated into RF ($\omega_1+\omega_2$) through two frequency up-conversions as shown in Fig. 2.3.

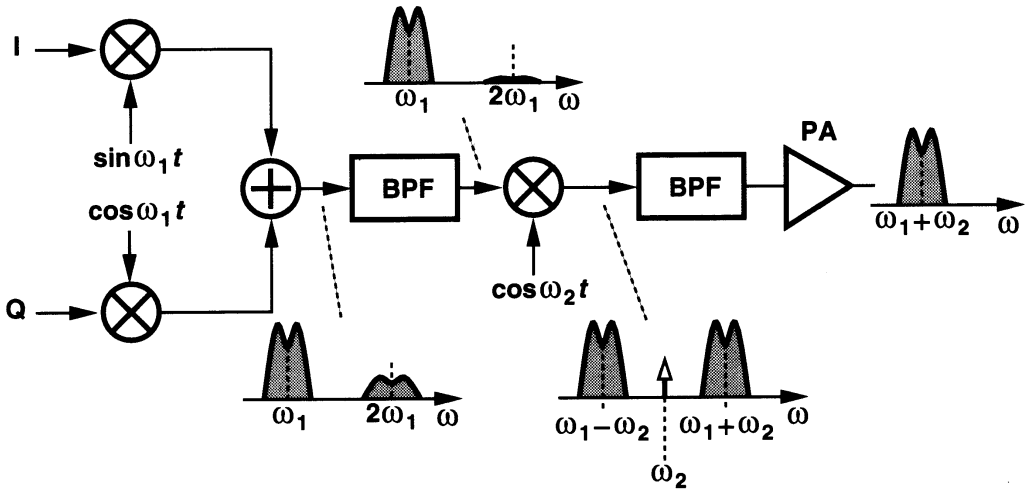


Fig. 2.3: Two-step transmitter [14]

This is the most commonly used architecture in communications devices mainly due to its high performance and selectivity even in the presence of strong interferers. However, one disadvantage of this architecture is the problem of the image frequency. As shown in Fig. 2.4, any unwanted signal (image) which exists at frequency ω_{IM} ($\omega_{LO}+\omega_{IF}$) will be down-converted to the same IF as the useful signal.

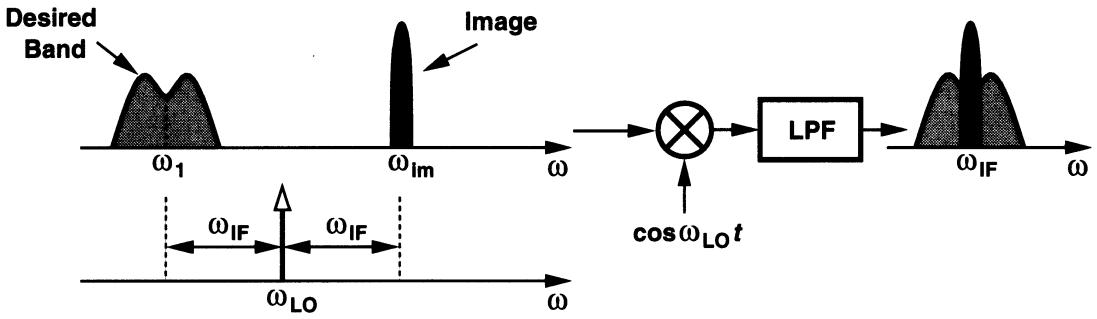


Fig. 2.4: Problem of image frequency in the receiver [14]

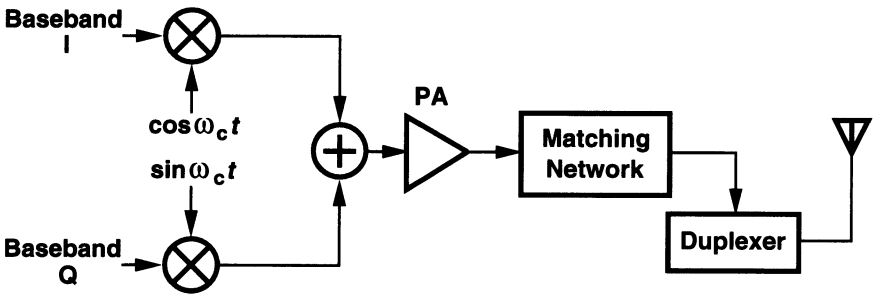
An image-reject filter (with low in-band loss and high attenuation at the image frequency) can be used before the mixer (in Fig. 2.2) to overcome this problem. However, if the IF is

too low (usually IF is low enough to allow the use of a low-Q IF or channel select filter), an external image-reject filter would have to be used to achieve high-Q, resulting in full chip integration issues.

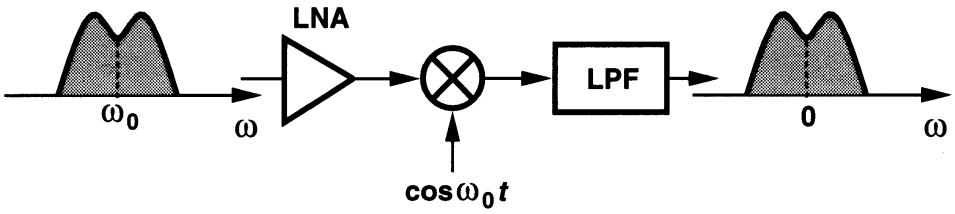
2.2.2 Homodyne Architecture

The homodyne architecture is much simpler than the heterodyne architecture as the baseband data is modulated and up-converted simultaneously into RF signal as shown in Fig. 2.5(a). The signal then gets amplified by a power amplifier (PA) and shaped by the matching network to provide maximum power transfer to the antenna. However, this transmitter architecture suffers from "injection locking" where the PA output leaks and corrupts the voltage-controlled oscillator (VCO) in the transmitter.

In the receiver, the RF signal is directly converted into baseband during the first down-conversion in the receiver, as shown in Fig. 2.5(b). In this case, the RF and LO frequencies have to be the same to achieve zero IF. The output is then taken from the low pass filter (LPF).



(a)



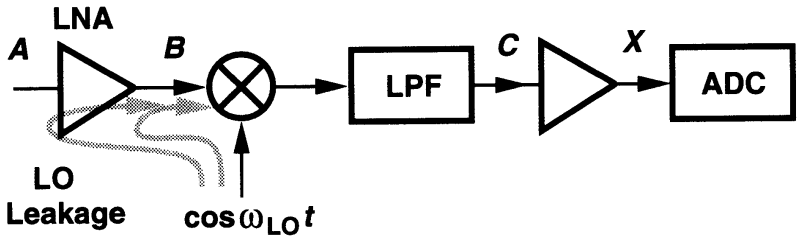
(b)

Fig. 2.5: Homodyne transceiver (a) Transmitter, (b) Receiver [14].

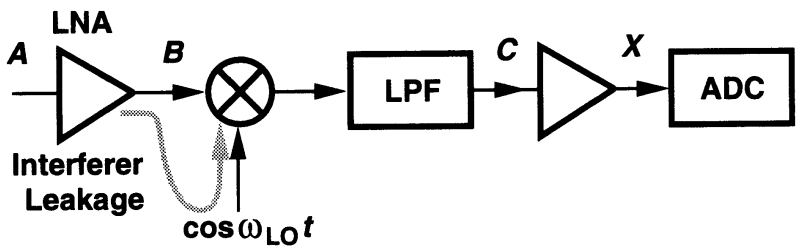
Unlike the heterodyne architecture, this receiver architecture does not suffer from image problem and is thus an easier option for full chip integration. However, the homodyne receiver architecture has several major design issues that have to be resolved.

DC Offsets

As shown in Fig. 2.6(a), LO signal can leak, for example, through the substrate to the LNA and mixer inputs [14]. The LO leakage self-mixes with the actual LO signal in the mixer and hence introduces DC offsets that might saturate the later gain stages in the receiver chain. The same problem can also happen when a strong interferer leaks from the mixer inputs to the LO port as shown in Fig. 2.6(b). Furthermore, LO leakage to the antenna will also acts as interferers to other radio systems utilizing the same wireless standard.



(a)



(b)

Fig. 2.6: Self-mixing of (a) LO signal, (b) large interferer in homodyne receivers [14].

Flicker Noise

Flicker noise (or 1/f noise) in a homodyne architecture can potentially corrupt the useful signal, which appears in the same baseband frequency. Furthermore, front end circuits (LNA and mixer) generally provide limited amount of gain (~30 dB), corresponding to tens of microvolts of output [14], which can be easily corrupted especially in the case of CMOS circuits as compared to SiGe and bipolar devices [15].

Even-order distortion

As shown in Fig. 2.7, when two strong interferers that lie close to the RF channel experience even-order nonlinearity in the LNA, low frequency components can be generated at the LNA output. Owing to asymmetry or poor isolation between the RF port and mixer output in the mixer, these low frequency components, which lie within the same band as useful demodulated signals, appear at the mixer output and degrade the SNR. This problem can be solved by employing differential architectures for the LNA and mixer, but at the expense of higher power consumption.

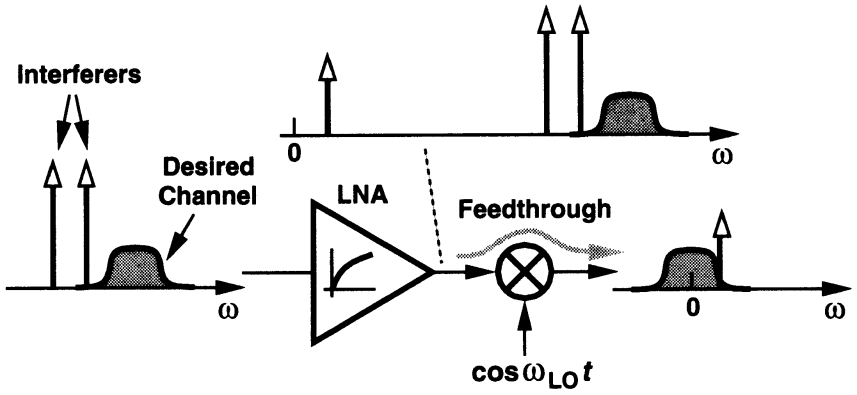


Fig. 2.7: Even-order distortion in the homodyne receiver [14]

2.3 Overview of UWB Transceivers

2.3.1 Common modulation schemes

The modulation schemes that are commonly used in UWB transceiver systems are pulse position modulation (PPM), pulse amplitude modulation (PAM), on-off keying (OOK), and bi-phase modulation (BPM) as shown in Fig. 2.8 [16].

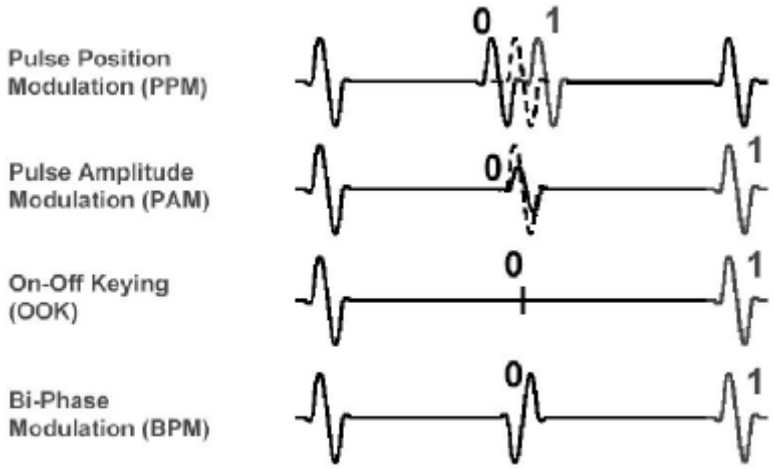


Fig. 2.8: Common modulation schemes in UWB systems [16]

Of the modulation schemes in Fig. 2.8, the OOK approach will result in the simplest transceiver architecture at the expense of a poorer sensitivity for a given Bit Error Rate (BER) as compared to the BPM approach [16].

2.3.2 UWB Transceiver Architectures

Conventional impulse radio based UWB transceiver architectures can be categorised into two main types: coherent and non-coherent.

Coherent UWB transceivers can generally be implemented in the form of a correlation receiver as shown in Fig. 2.9 [17], which includes a channel estimation block, template generator block, multiplier, integrator and finally a decision block. In this structure, the received signal *r(t)* is multiplied with a locally generated template waveform *v(t)* for correlation. The Rake receiver consisting of multiple fingers or sub-receivers is an example of such coherent architecture. Rake receivers are particularly useful for wireless communications in dense multipath environments.

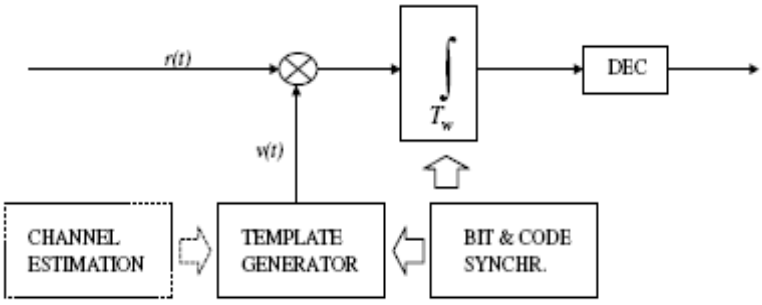


Fig. 2.9: General structure of a UWB correlation receiver [17]

Coherent transceivers, which are capable of achieving high data rates of hundreds of Mbps and good noise and interference performance, have been widely implemented for IEEE802.15.3a WPAN systems [18]-[20]. However, the need for channel estimation and

template generation usually results in complex and costly system architecture, especially so for the Rake architecture since a large number of fingers is usually required to get a good gain performance.

Non-coherent UWB receiver or transceiver architecture [21]-[23], on the other hand, is not required to generate and synchronise a template waveform and is thus simpler and consumes less power as compared to the coherent ones. It is thus more suitable for wireless sensor networks applications. Through the transmitted reference (TR) architecture (shown in Fig. 2.10 [11]), the received signal is also used as the reference waveform for automatic correlation in the mixer block. The energy of multipath signals can also be fully captured with a sufficiently long window for the integrator. In the transmitter, the data is encoded based on the pulse polarity and then the UWB impulses are transmitted. Even though this architecture does not require a local oscillator and fast sampling circuits for synchronisation and channel estimation, it suffers in terms of its noise performance since both the received signal and the reference waveform contain noise.

Another possible implementation of the non-coherent architecture is based on the energy detection approach as shown in Fig. 2.11 [23]. The non-coherent receiver architecture in Fig. 2.11 [23] uses OOK modulation scheme for its simplicity. An energy detector (usually a squarer or multiplier) is employed after the Low Noise Amplifier (LNA) in the receiver chain. It is then followed by the low pass filter, Variable Gain Amplifier (VGA) and Analog-to-Digital Converter (ADC). The transceiver architectures that will be proposed in this thesis are based on the OOK modulated energy detection architecture as in Fig. 2.11.

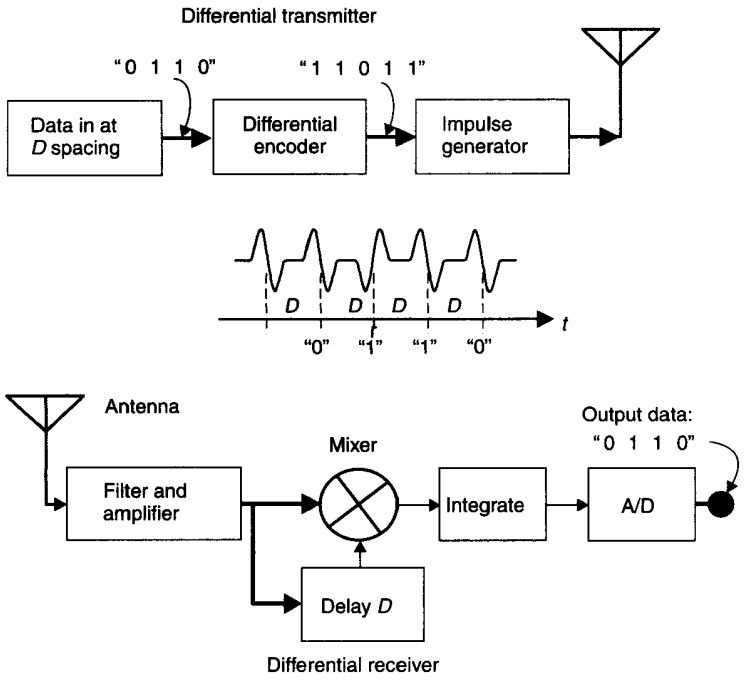


Fig. 2.10: Transmitted reference (TR) UWB transceiver [11]

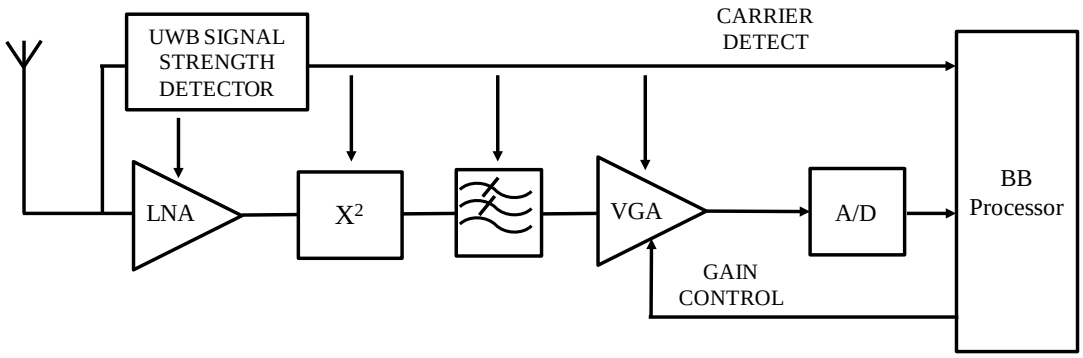


Fig. 2.11: Non-coherent receiver architecture [23]

Chapter 3

Receiver Building Block Design

This chapter will discuss the circuit blocks that have been designed by the author for the UWB receivers in this thesis, namely the low noise amplifier (LNA), squarer, super regenerative UWB detector and limiting amplifier. All designs and simulations were done using Agilent Advanced Design System (ADS) software with 0.18-µm CMOS technology provided by Chartered Semiconductor Manufacturing (CSM).

3.1 Low Noise Amplifier

3.1.1 General Considerations

Since the focus of this thesis is on the receiver, the low noise amplifier (LNA) will be presented first. The LNA is usually the first receiver block after the antenna and is one of the most important blocks in the receiver chain. Some important parameters in the design of a LNA are gain, noise figure, input impedance matching, linearity and power consumption.

The main purpose of the LNA is to provide a high enough gain while introducing minimal noise into the system since the LNA noise directly impacts the overall noise factor of the entire receiver system. This can be understood by the Friis equation [14]:

$$nf_{tot} = 1 + (nf_1 - 1) + \frac{nf_2 - 1}{A_{p1}} + \cdots + \frac{nf_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{3.1}$$

where nf_{tot} is the overall noise factor, nf_m is the noise factor of the *m*-th stage with respect to the source impedance driving that stage and A_{pm} is the numerical power gain of the *m*-

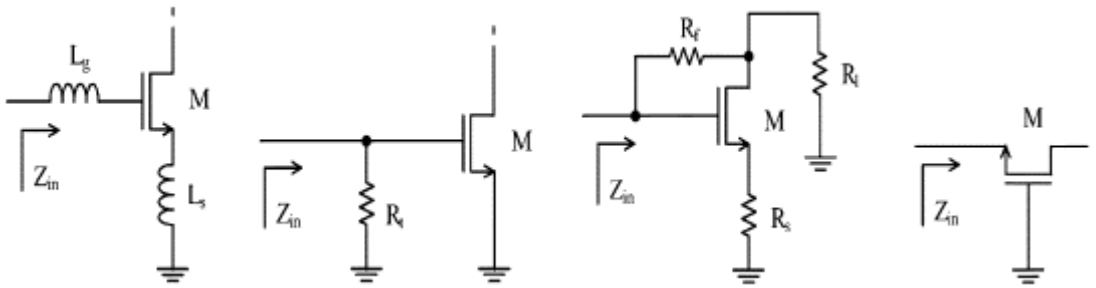
th stage. The Friis equation implies that as we move down the receiver chain, the effective noise contribution of each block decreases provided that its noise factor is not too large and the gain product of the preceding stages is large. Being the first stage in the receiver chain, the LNA therefore has to provide a low noise figure (nf_1) and high power gain (A_{p1}). In addition, the noise figure of the LNA will also present a lower limit on the receiver sensitivity. Linearity is also important as large interferers may co-exist with UWB signals and can potentially desensitize the LNA. The LNA thus has to be able to handle the useful UWB signals as well as large interferers without being desensitized.

Input impedance matching is another important consideration in the LNA design. The impedances of the antenna and LNA have to be conjugate matched (typically 50 Ω) to ensure maximum transfer of power from the antenna into the LNA in order to achieve an efficient system performance. Typically, input matching is considered to be good when the input return loss (S11) is less than -10 dB.

Lastly, the power consumption of the LNA is especially important in low data rate wireless sensor network applications to prolong the battery life of the numerous sensor nodes in possibly large remote areas so that the hassle of frequent battery replacement can be avoided. A compromise thus has to be achieved between the ideal targets of designing a high gain, highly linear, low noise and power efficient LNA.

3.1.2 LNAs in the literature

Several input impedance matching techniques have been presented in recent wideband LNA works [24]-[30] and they are as shown in Fig. 3.1.



(a) (b) (c) (d)

Fig. 3.1: Input impedance matching techniques (a) Inductive source degeneration, (b) Resistive termination, (c) Shunt-series feedback, (d) Common gate amplifier [24].

All the techniques in Fig. 3.1 except for (a), are capable of providing broadband matching to a 50 Ω antenna. Inductive source degeneration (Fig. 3.1(a)) can provide good matching at its resonant frequency and is commonly used for narrowband LNAs. Its input impedance can be derived to be as follows:

$$Z_{in} = \frac{1}{sC_{gs}} + s\left(L_s + L_g\right) + \omega_T L_s \tag{3.2}$$

where $\omega_T = \frac{g_m}{C_{gs}}$, C_{gs} is the gate-source capacitance and g_m is the transconductance of the transistor. Recent works [28]-[29] have shown that the inductive source degeneration matching technique can be extended to UWB applications. The incorporation of a Chebyshev filter network in [28] allows the reactive part of the input impedance to resonate over a wider frequency band while the introduction of a shunt feedback network in [29] widens both the bandwidth and input matching range. Even though the inductive source degeneration matching technique can achieve a better noise performance than the other techniques in Fig. 3.1, it has its disadvantage in wideband implementation as the

implementation in [28] requires large number of inductors and the filter network is not lossless. In [29], fewer inductors are used but the shunt feedback resistor would contribute thermal noise to the LNA.

Resistive termination (Fig. 3.1(b)) is the simplest technique for broadband impedance matching. However, besides introducing unacceptable levels of thermal noise into the circuit, it also reduces the received signal by half [26]. The noise figure of this matching network is

$$NF \geq 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R_t} \tag{3.3}$$

where γ is the body-effect coefficient and $\alpha = \frac{g_m}{g_{d0}}$. The noise figure of this matching technique will increase when the gate current noise is taken into account at high frequencies. Thus this technique is rarely used in practical amplifiers.

The shunt-series feedback matching technique in Fig. 3.1(c) not only provides broadband matching to the antenna, but also a flatter gain response. The input impedance is as follows [26]:

$$Z_{in} = \frac{R_f}{1 - A_V} \approx \frac{R_f}{1 + \frac{R_l}{R_s}} \tag{3.4}$$

where A_V is the voltage gain from the gate to drain terminal. However, in this technique, the resistor in the feedback path not only affects the input matching, but it also injects thermal noise into the circuit. It has been shown in [30] that the relationship between input matching and noise figure can be decoupled. However, the circuit achieves a low noise

figure at the expense of a higher power and large loop gain, which would cause stability issues in multi-stage LNA.

The common-gate amplifier in Fig. 3.1(d) can provide a good broadband matching to the antenna with a suitably chosen transistor size and bias current. The input impedance can be expressed as follows:

$$Z_{in} = \frac{1}{g_m + g_{mb}} \tag{3.5}$$

The noise figure of the common-gate amplifier is as follows [26]:

$$NF \geq 1 + \frac{\gamma}{\alpha} \tag{3.6}$$

Similarly, this equation does not take into account the gate current noise which is important in high frequency operations. The idea of further reducing the noise of the common-gate amplifier has been investigated in [27], which also allows the input matching and noise figure requirement to be decoupled. In addition, this method also reduces the noise contribution of the load by a factor of 4 in the common-gate amplifier.

3.1.3 Proposed LNA circuits

Two new LNA circuits will be proposed in this section for use in 3-5 GHz UWB systems. In both LNA circuits, common-gate has been chosen as the input matching technique as it can provide satisfactory noise performance and additional gain. A high gain is particularly needed in the LNA so as to compensate the loss of the latter stage, which is the squarer in this case.

The first LNA circuit is proposed and implemented as a four-stage wideband LNA to achieve sufficient gain as shown in Fig. 3.2.

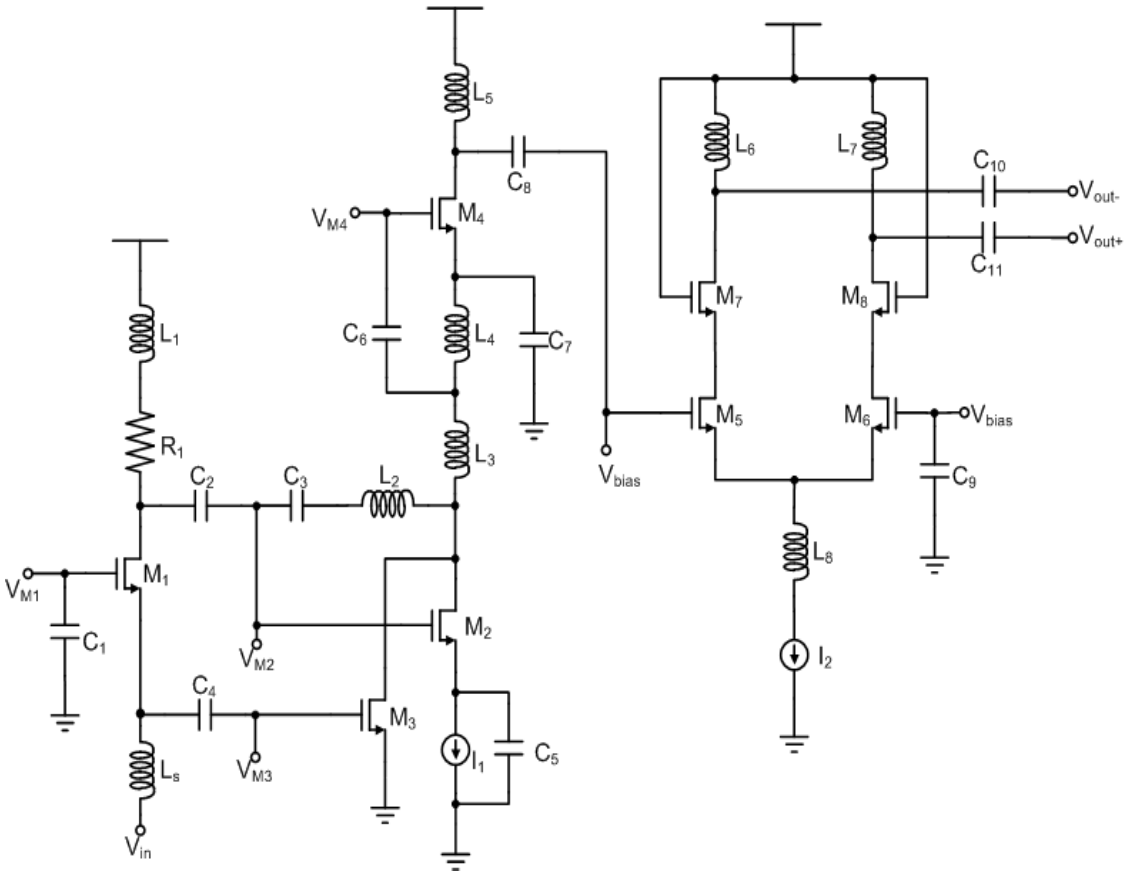
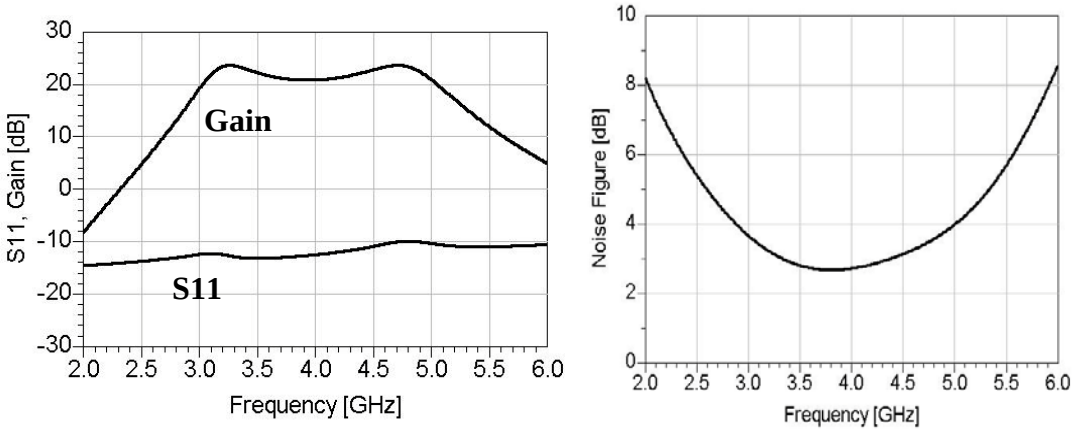


Fig. 3.2: Current reuse LNA with noise cancelling and single-ended-to-differential conversion

It combines the techniques of noise cancelling and current reuse. The noise cancelling LNA in [27] is directly adopted here to reduce the LNA noise figure as transistor M_3 cancels the noise contribution from transistor M_1. In this thesis, work has been done to enhance the bandwidth of the LNA in [27] through the use of the shunt feedback network, L_2 and C_3. This is followed by the current reuse second (M_2, L_3-L_4) and third (M_4, L_5) stage common-source amplifiers through the AC coupling capacitor C_6 to reduce the

power consumption. The differential amplifier is then proposed for the final stage to achieve both gain and single-ended to differential conversion. The LNA achieves a minimum power gain of 20.2 dB, a maximum noise figure of 4.2 dB, and S11 less than -10 dB across the desired 3-5 GHz band while consuming a total current of 9.4 mA as shown in Fig. 3.3.



(a) (b)

Fig. 3.3: Performance of noise cancelling LNA (a) Gain and S11, (b) Noise Figure.

The second LNA circuit is as shown in Fig. 3.4. The basic architecture is the same as Fig. 3.2, consisting of a common-gate input matching, 3 current reuse stages and a single-ended-to-differential amplifier. More current reuse stages have been used here for higher gain. The amplifiers in the current reuse stages are of common-source configuration for achieving high gain performance. Decoupling capacitors C_2, C_3, C_6, C_7 and C_{10} are used to achieve good AC ground. Noise cancelling functionality has been removed from this LNA circuit as additional power is needed to cancel the noise. This power can be better saved to prolong the battery life of sensor nodes instead while not sacrificing too much in terms of noise performance and this could be achieved by optimization of the circuit in Fig. 3.4. The performance of this LNA is summarized in Fig. 3.5. A minimum in-band

voltage gain of 49dB, minimum noise figure of 3 dB and good in-band input matching is achieved with a current consumption of 10.2 mA.

To reduce the power consumption, the tail current sources of the LNA can be powered on/off via the circuit implementation shown in Fig. 3.6. During power on mode, SW_1 is switched on while SW_2 is off and thus the circuit behaves as a conventional current mirror. In the power off mode, the opposite occurs (SW_1 is off and SW_2 is on) and thus no current is generated for the LNA circuit.

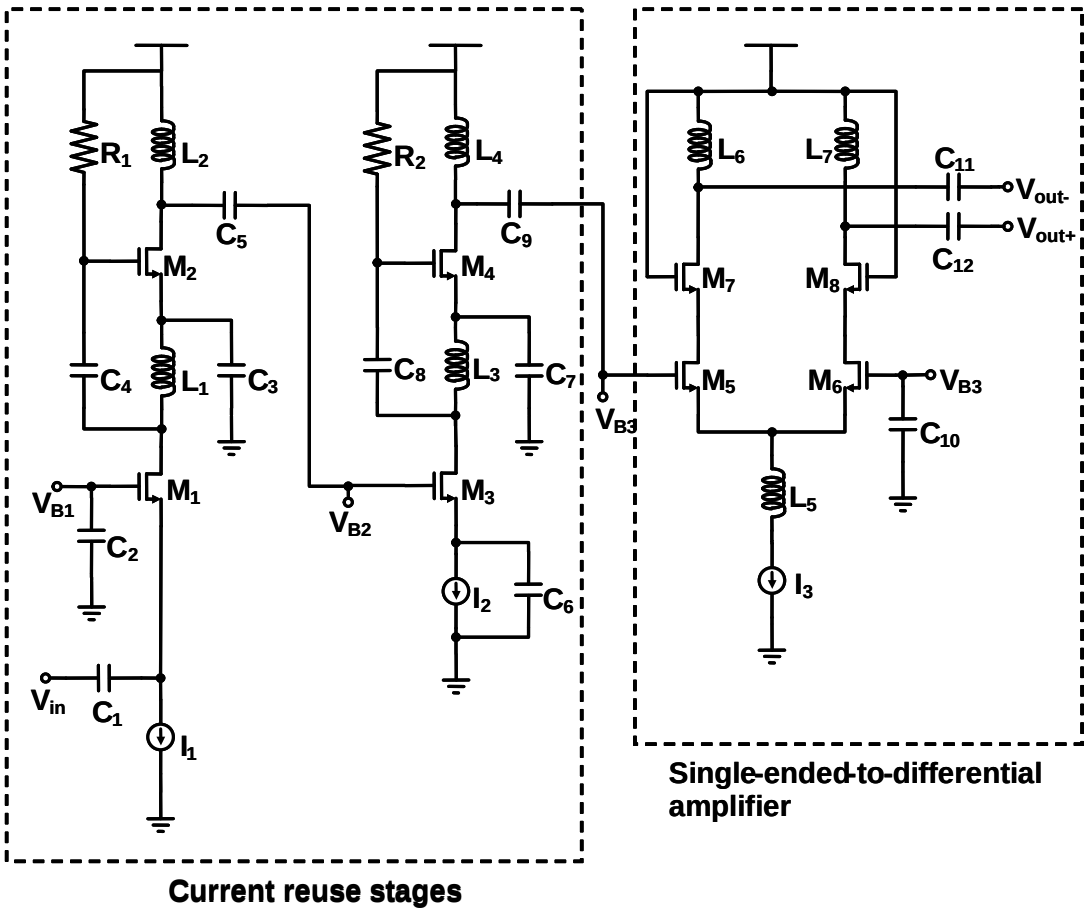


Fig. 3.4: Current reuse LNA with single-ended-to-differential conversion

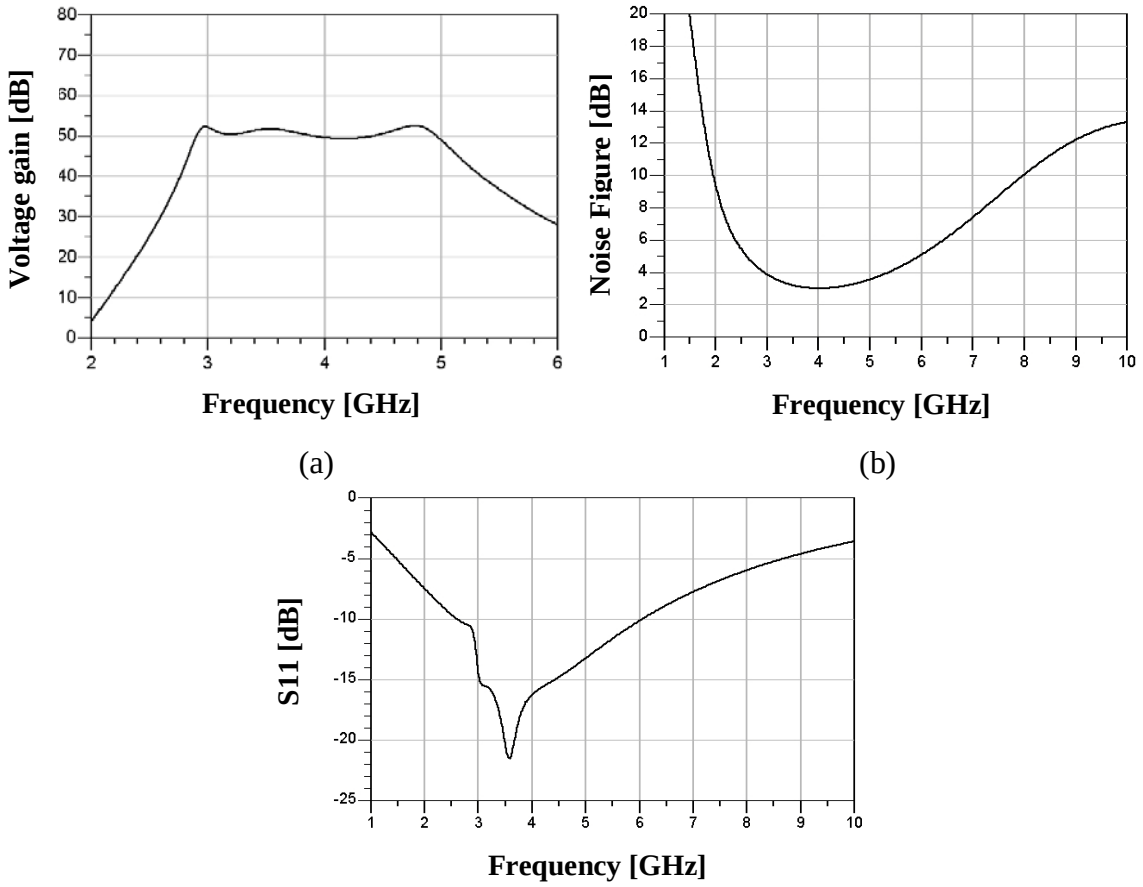


Fig. 3.5: Performance of LNA (a) Voltage gain, (b) Noise Figure, (c) S11.

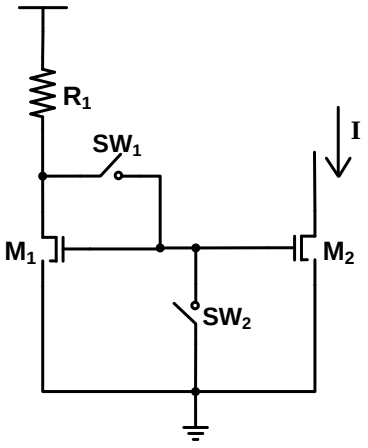


Fig. 3.6: Implementation of tail current source

3.2 Squarer

3.2.1 General Considerations

In this thesis, the squarer is the next circuit block in the receiver after the LNA. One of the main design challenges in this squarer is the wide input bandwidth (3-5 GHz) since its input comes directly from the UWB LNA. In addition, sufficient conversion gain has to be allocated to this block to improve the output SNR. The squarer gain equation can be expressed as follows:

$$y = k \cdot x^2 \tag{3.7}$$

where y is the squarer output, k is the squarer conversion gain and x is the input. The output bandwidth of the squarer is also an important consideration. Since its input is an amplified UWB (3-5 GHz) signal, the output spectrum will mostly contain energies in the regions from zero frequency to few hundreds MHz and higher frequency bands (twice the input frequency). It will be tedious and power inefficient to capture the whole useful signal. Hence, the output bandwidth has to be appropriately chosen through extensive simulations in order to capture most of the demodulated energies for better system performance. Other than the parameters mentioned above, power is also important for reasons similar to the LNA.

3.2.2 Squarers in the literature

The squaring circuit in a non-coherent system can be implemented using analogue multipliers [23] [31] or simply squarers [32]-[33]. Implementation of the multipliers, however, is more complex and requires higher power as compared to the latter since

squarers can be used as the basic block for four-quadrant multiplier circuits as shown in Fig. 3.7 [34]. Furthermore, the multiplier approach to implement squaring circuits can limit the input bandwidth [32], which is an important consideration for the squarer design here.

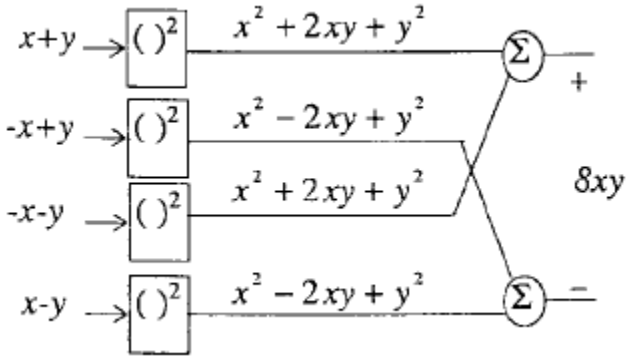


Fig. 3.7: A four-quadrant multiplier architecture employing squarer as basic block [34]

Squarers can be designed using MOS transistors working in the saturation [33] [35], linear (triode) [32] or even subthreshold conduction region [36]. Squarers in [33] and [35] make use of the following square-law characteristic exhibited by MOS transistors operating in the saturation region (neglecting channel length modulation effects):

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{th}|\right)^2 \tag{3.8}$$

where I_D represents the transistor drain current, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W is the transistor width, L is transistor length, V_{GS} is the gate-source voltage and V_{th} is the threshold voltage.

In the linear region, the drain current of MOS transistor can be expressed by the following Taylor series [32]:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\sum_{i=1}^{+\infty} a_i\left(V_D^i - V_S^i\right) \tag{3.9}$$

where the a_i coefficients are functions of the transistor parameters, gate bias and substrate bias, V_D and V_S are the drain and source voltages respectively. Even though it is relatively simpler than the other squarer ideas, its gain is not as high as those operating in saturation region and thus, an external voltage is needed to adjust the gain via the transistor's body terminal [32].

MOS transistors that operate in the subthreshold conduction region can also be used in squarers based on the following characteristic [36] whereby I_D exhibits an exponential relationship with the gate-source voltage for very low drain currents:

$$I_D = I_{ON}\exp\left(\frac{|V_{GS}| - |V_{th}| + \eta V_T}{\eta V_T}\right) \tag{3.10}$$

where I_{ON} is the transistor's drain current when it is operating at the boundary between strong and weak inversion, V_T=kT/q is the thermal voltage (26 mV at room temperature) and η is the subthreshold slope parameter. However, for the MOS transistor to operate in subthreshold conduction, a very large transistor width is usually required, thus introducing large parasitic capacitance that would limit the input bandwidth. Furthermore, the low current will also limit the speed of such circuits.

3.2.3 Proposed Squarer Circuit

The proposed squarer circuit is shown in Fig. 3.8. The basic cell of the proposed squaring circuit is directly adopted from [35] [37], which is based on the multitail technique where

the source terminals of NMOS input transistors M_1-M_4 are coupled together into a current sink I_1. In this thesis, additional circuitries have been added in to improve the performance of the basic cell. Firstly, the proposed squarer is now resistively terminated for gain and conversion of the output currents into voltages and secondly, cascode transistors are added for better gain and isolation performance.

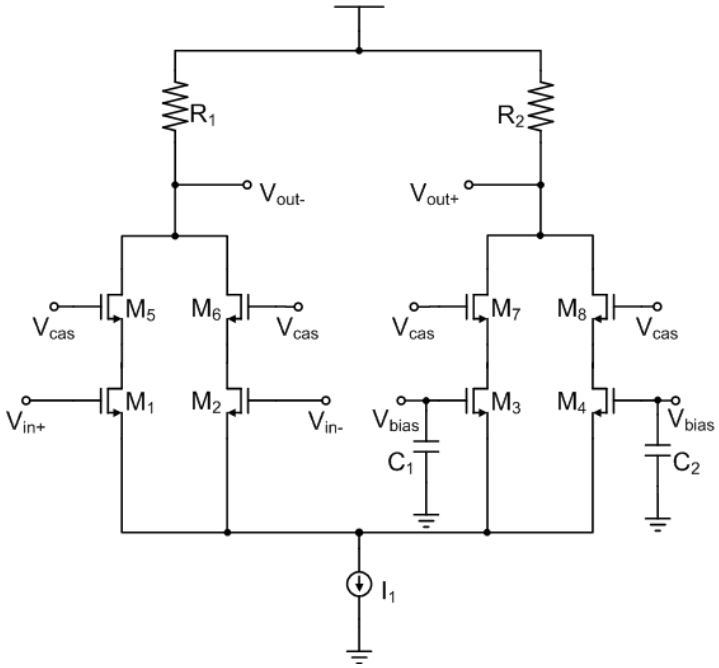


Fig. 3.8: Proposed squarer circuit

The squarer core consists of 4 NMOS input transistors M_1-M_4 with cascode transistors M_5-M_8 and resistive loads R_1, R_2 in a differential configuration where the two half circuits are of a similar structure. It makes use of MOS transistors operating in the saturation region to achieve higher gain and speed performance. Neglecting second order effects, the drain currents of transistor M_1-M_4 can be expressed as follows based on the square-law characteristic:

$$I_{D1} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(V_{bias} + V_{in}\right) - V_S - V_{th}\right]^2 \tag{3.11}$$

$$I_{D2} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[\left(V_{bias} - V_{in}\right) - V_S - V_{th}\right]^2 \tag{3.12}$$

$$I_{D3} = I_{D4} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{bias} - V_S - V_{th}\right)^2 \tag{3.13}$$

where I_{Dn} represents the drain current of transistor M_n, V_{bias} is the transistor's gate voltage bias and V_{in} is the input amplitude at each input terminal.

$$I_{D1} + I_{D2} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(2V_{OD}^2 + 2V_{in}^2\right) \tag{3.14}$$

$$I_{D3} + I_{D4} = \mu C_{ox}\frac{W}{L}V_{OD}^2 \tag{3.15}$$

where $V_{OD} = V_{bias} - V_S - V_{th}$ is the overdrive voltage. From (3.14) and (3.15), it is evident that the left transistor pair M_1-M_2 generate both a squared term (V_{in}^2) and a DC term (V_{OD}) while the right transistor pair M_3-M_4 will produce an identical DC term. Taking the difference at the outputs, we have

$$V_{out} = \left[V_{DD} - \left(I_{D3} + I_{D4}\right)R_L\right] - \left[V_{DD} - \left(I_{D1} + I_{D2}\right)R_L\right]$$

$$V_{out} = \left(\mu C_{ox}\frac{W}{L}R_L\right)V_{in}^2 \tag{3.16}$$

where R_L represents the load resistor (in this case, R_1 and R_2).

Conversion gain of the squarer can be defined as follows:

$$ConversionGain = \mu C_{ox} \frac{W}{L} R_L \tag{3.17}$$

The current consumption of the squarer is 2.06 mA. The input-output transfer characteristic of the squarer is shown in Fig. 3.9. Fig. 3.10 shows the derivative or gradient of the input-output transfer characteristic (Fig. 3.9), which represents the input voltage range of proper squaring operation as indicated by the straight line region. The proposed squarer is able to ensure proper squaring function for input voltage amplitudes of up to 50 mV at each input terminal and a conversion gain of 40 dB (Fig. 3.11). For power savings, the same current source implementation (Fig. 3.6) is used here to provide the tail current for the squarer circuit.

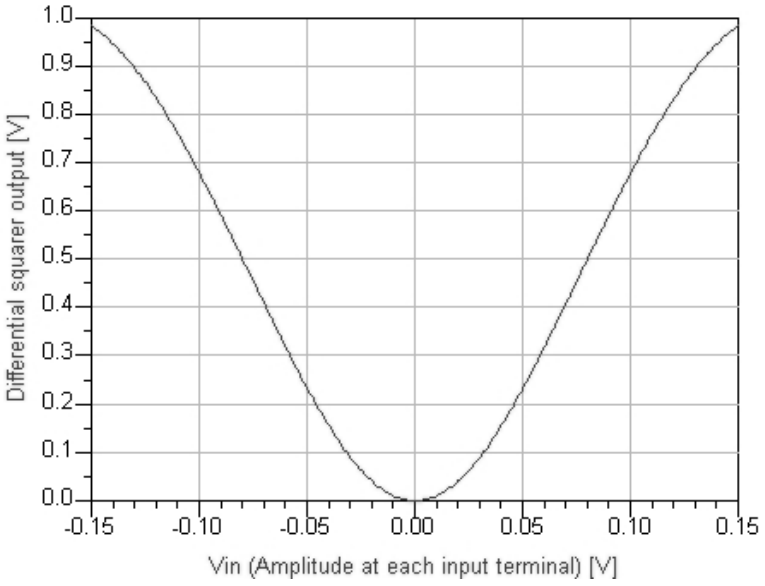


Fig. 3.9: Input-output transfer characteristic of squarer

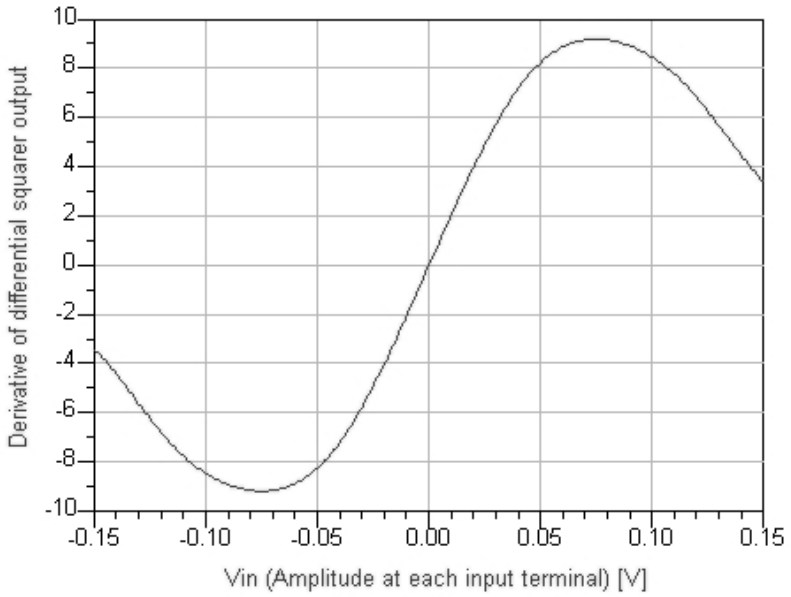


Fig. 3.10: Derivative of transfer characteristic

(Input voltage range of proper squaring operation is represented by straight line region from -50 mV to 50 mV)

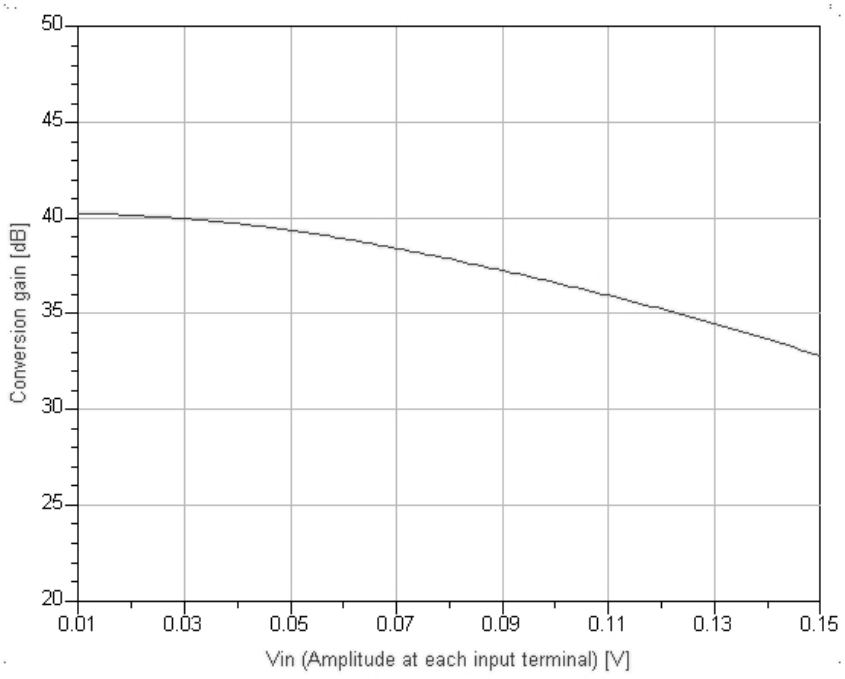


Fig. 3.11: Conversion gain of squarer

3.3 Limiting Amplifier

3.3.1 General Considerations

The limiting amplifier (LA), as its name suggests, is the circuit block that will amplify the input signal until its "limiting state" or saturation. Therefore, a limiting amplifier is usually implemented as a cascade of gain stages so as to achieve the required gain (usually at least 30 dB). A general architecture of the limiting amplifier is shown in Fig. 3.12 [38]. Since the limiting amplifier is usually employed in optical communications system, a matching network and buffer has been included in the figure for input matching to the preceding external Trans-Impedance Amplifier (TIA) and driving the capacitive load of the subsequent clock and data recovery (CDR) circuit. Some important parameters in the design of a LA are gain, bandwidth, offset cancellation and power consumption.

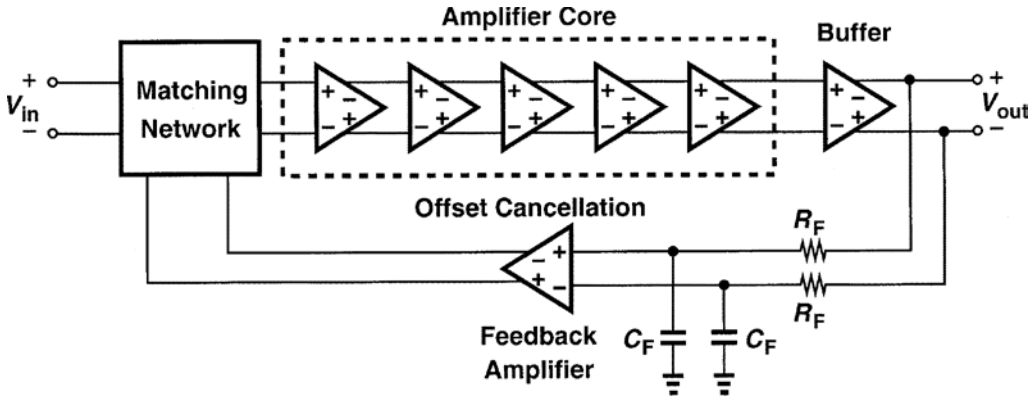


Fig. 3.12: General architecture of limiting amplifier [38]

The first two parameters are perhaps the most important ones of the list as they directly impact the most basic function of the LA circuit. Furthermore, they are usually used as the starting point in the design of the LA circuit. Knowledge of the overall gain and bandwidth requirements can enable us to calculate the optimum number of cascaded

stages as well as the gain and bandwidth distributions based on the following equations [38] for a first-order gain stage:

$$A_s = A_t^{\left(\frac{1}{N}\right)} \tag{3.18}$$

$$f_s = \frac{f_t}{\sqrt{2^{\left(\frac{1}{N}\right)} - 1}} \tag{3.19}$$

where A_t and f_t are the overall small signal gain and bandwidth, A_s and f_s are the gain and bandwidth of each gain stage, and N is the number of gain stages.

A cascade of high-gain amplifier stages can amplify mismatches (due to process, voltage and temperature variations) and cause the DC level of the differential output to increase, possibly saturating the amplifier in the absence of useful signals. To prevent this, an offset-cancellation circuit is usually implemented together with a limiting amplifier. The offset-cancellation circuit is basically a low pass filter designed to have a low cut-off frequency (in the order of tens of kilo Hertz) for reasonably fast settling times and minimizing the output "droop" in time domain as shown in Fig. 3.13 [38]. The circuit extracts the inherent DC offset, which is then fed forward or back into the limiting amplifier for elimination.

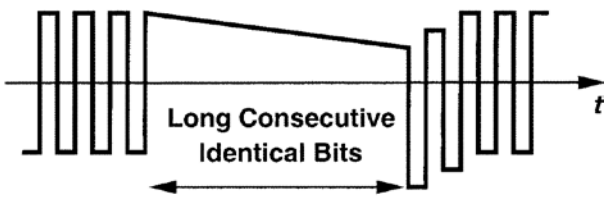


Fig. 3.13: "Drooping" of the output after long runs [38]

For low power applications, a compromise between gain, bandwidth and power consumption has to be balanced. The limiting amplifier has to be able to achieve high gain and wide bandwidth while consuming sufficiently small currents.

3.3.2 Limiting amplifiers in the literature

A basic gain stage in the limiting amplifier can be simply implemented by a NMOS differential input pair with active PMOS loads for high gain as shown in Fig. 3.14 [39].

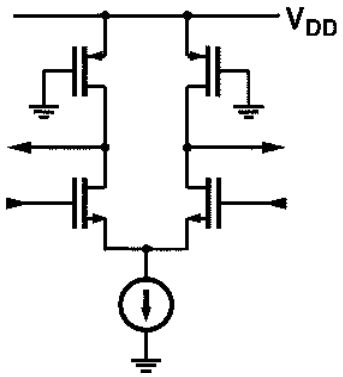


Fig. 3.14: Typical gain stage in limiting amplifier [39]

Since a cascade of gain stages introduces more poles and reduces the overall bandwidth, it is desirable to have a wide bandwidth for each gain stage. Several techniques of bandwidth enhancement in limiting amplifiers have been proposed. First technique involves the use of inverse scaling of the gain stages [39]. The gain-bandwidth product of each gain stage can be expressed as:

$$GBW = \frac{g_m}{C_{tot}} \tag{3.20}$$

where g_m and C_{tot} represent the transconductance and total load capacitance of the gain stage. Since the total load capacitance C_{tot} consists of both the output capacitance within the gain stage as well as the next stage input capacitance, it is clear that a reduction in the next stage input capacitance will result in a bandwidth increase. A larger scale factor will produce a larger bandwidth. However, the use of this technique is dependent on the maximum allowable input capacitance and the load capacitance to be driven by the limiting amplifier.

Shunt peaking is the second technique commonly used for bandwidth enhancement in limiting amplifiers. In this technique, passive or active inductors are used to introduce an additional zero into the circuit to cancel the dominant pole. Passive inductors such as spiral inductors can be used in each gain stage to provide high Q-factor, low noise and low voltage drop across it. However, they consume huge areas especially in limiting amplifiers due to the use of cascaded gain stages. On the other hand, active inductors do not take up as much die area but they require large voltage drop and introduce more noise. To overcome the problem of large voltage drop, a higher voltage may be used to bias the transistor gate of an active inductor [39] but this will require a more complex circuit if a fully integrated solution is to be implemented. Folded active inductors [40]-[41] have been proposed as an alternative solution to this problem.

In recent limiting amplifier papers, several offset cancellation circuits have been proposed. The most conventional one is the simple RC low pass filter network [38] [41] [42] [43]. However, to achieve a sufficiently low cut-off frequency (large resistor and capacitor), part of the filter network is usually implemented using off-chip discrete components. More complex techniques have been proposed to cancel the DC offset, including the use of a top-detection feedback circuit [40], peak detector and integrator [44], peak-hold

circuit and automatic offset canceling feedback amplifier [45]. However, all these techniques require a constant biasing circuitry which will increase the power consumption of the limiting amplifier circuit.

3.3.3 Proposed limiting amplifier circuit

A new limiting amplifier is proposed in this thesis, which consists of a cascade of five gain stages and each gain stage (shown in Fig. 3.15) is designed to achieve a gain of 12 dB and bandwidth of more than 1 GHz.

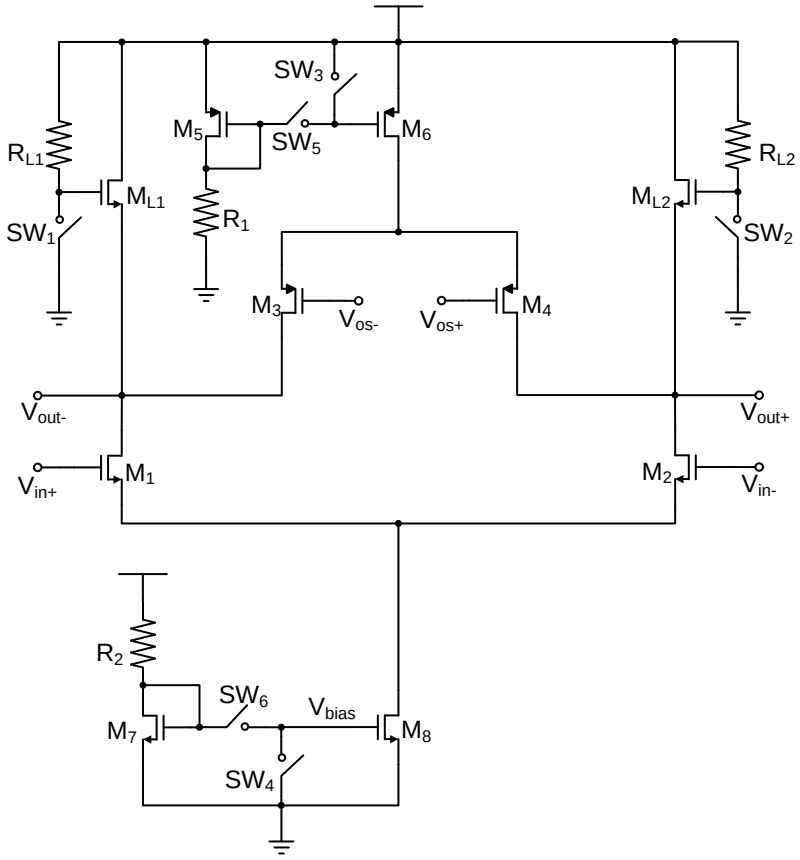


Fig. 3.15: Proposed limiting amplifier gain stage

The gain stage is made up of a differential NMOS amplifier with active inductor load (M_{L1}, R_{L1} and M_{L2}, R_{L2}) for bandwidth enhancement, where the value of the inductor is defined to be as follows [39]:

$$L = \frac{R_g}{\omega_T} \tag{3.21}$$

where R_g and ω_T represent the resistor at the transistor's gate and the unity-gain frequency. Due to the high gain in the limiting amplifier, DC offset compensation is performed at each amplifier stage. The outputs of each stage are connected to an offset extractor circuit to extract the DC offset, which is then fed back to the amplifier circuit in negative feedback configuration via M_3-M_6 and R_1 in Fig. 3.15. The implemented offset extraction circuit is directly adopted from [46] as shown in Fig. 3.16.

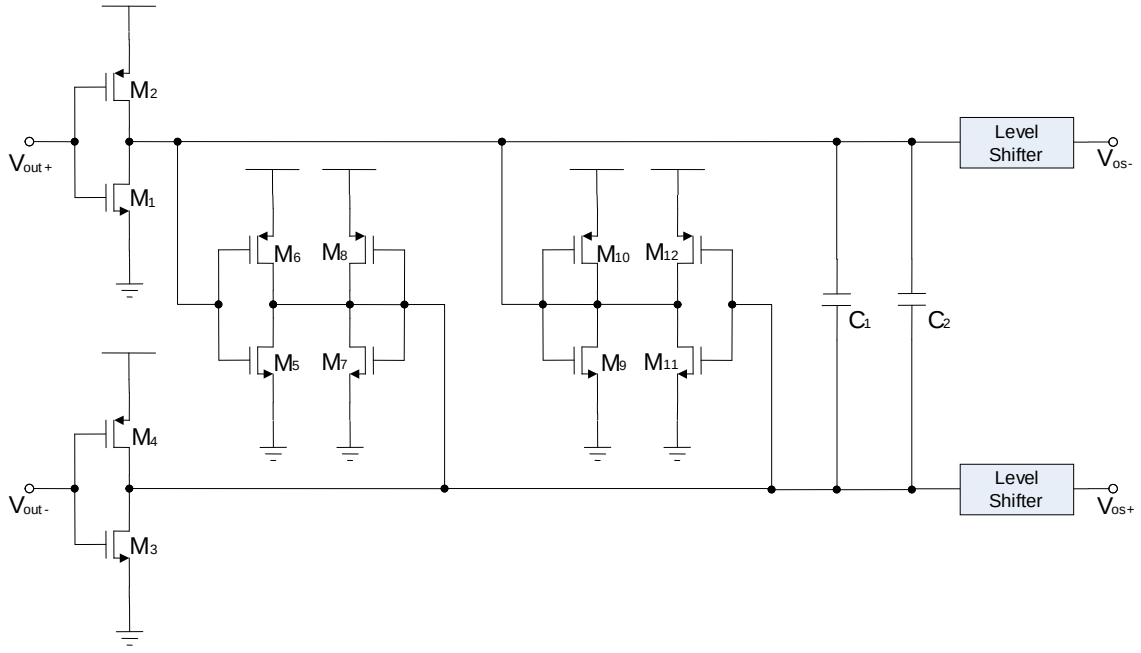


Fig. 3.16: Implemented offset extraction circuit

The output DC offset is sensed and filtered by a gm-C lossy integrator (M_1-M_{12}) employing the Nauta's differential transconductor [46]. The differential pair is made up of M_3-M_8 in one branch and M_1-M_2, M_9-M_{12} in the other branch. Inverters formed by M_1-M_2 and M_3-M_4 are used to generate the transconductance while M_5-M_{12} are employed to ensure common mode stability and achieve the desired high output impedance. In addition to the adopted offset extraction circuit, a simple source follower level shifter (shown in Fig. 3.17) is used to apply shift the voltage bias so that it can be applied onto the gate of the PMOS transistors, M_3-M_4 in Fig. 3.15. SW_1 is used to bias the output to high so that no current is consumed when the limiting amplifier is powered off.

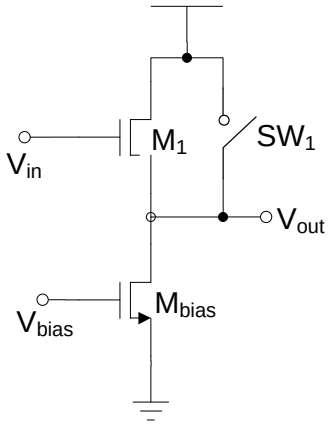


Fig. 3.17: Level shifter circuit

To obtain a low DC offset canceling pole, the output impedance of the transconductor is designed to be very large by choosing the g_m of M_5, M_6 slightly larger than M_7, M_8, so that reasonable integrated capacitance (C_1 and C_2) can be obtained.

The output single-ended impedance of the transconductor is defined as [46]:

$$R_{DM} = \frac{1}{g_{d1/2} + g_{d9/10} + g_{d11/12} + g_{m9/10} - g_{m11/12}} \tag{3.22}$$

where g_d and g_m represent the parasitic output conductance and transconductance respectively of the NMOS and PMOS transistors in each inverter.

The limiting amplifier provides an overall small signal gain of 60 dB with a bandpass characteristic of 288 kHz to 1 GHz (Fig. 3.18). A total of five gain stages are cascaded to provide sufficient gain for the weakest incoming pulse. To reduce the power consumption for stronger incoming pulses, each gain stage in the cascading chain can be powered down and bypassed independently by controlling the switches SW_1-SW_6 in Fig. 3.15. During power on mode, SW_1-SW_4 are in the off-state while SW_5-SW_6 are switched on and the limiting amplifier amplifies the input signal. When it is powered off (SW_1-SW_4 are switched on while SW_5-SW_6 are off), transistors M_{L1}-M_{L2}, M_6 and M_8 are turned off, thus eliminating static current consumption in the circuit.

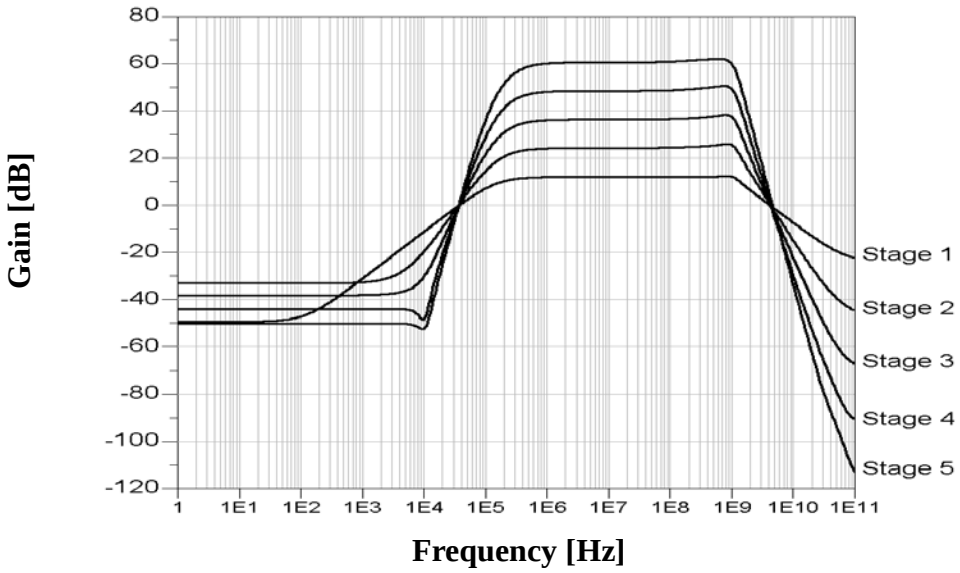


Fig. 3.18: Frequency response of LA

3.4 Super Regenerative UWB detector

3.4.1 General Considerations

For applications such as wireless sensor networks, the design of power and cost effective transceivers are important for reasons mentioned in Section 1.2. One of the most obvious methods to achieve low power and small transceiver size is to employ the super-regenerative architecture for low distance and low data rate communications. Through this architecture, the circuit blocks can be reused since they are connected in a positive feedback loop and large signal amplifications can be achieved using minimal current.

However, for these architectures, one of the most important considerations is its stability since the circuit blocks are potentially unstable within the region of large non-linear amplification. Thus, additional circuitries have to be designed to ensure its stability. Other considerations for the detector include ensuring low power consumption and an open loop gain of larger than unity so that the signal will continue increasing within the loop.

3.4.2 Super Regenerative Works in the literature

Super regeneration has been successfully employed in RF front-end for narrowband system [47]-[49]. However, to date, most super regenerative amplifiers are based on oscillator-type circuit which depends on an additional quench signal to toggle the circuit function between bandpass filter and high gain amplifier. High Q resonator is also required to improve the signal selectivity which mandates either additional tuning circuitry for Q-enhancement or external high-Q passive components.

Conventional oscillator-type based super regenerative architecture can be modeled as shown in Fig. 3.19.

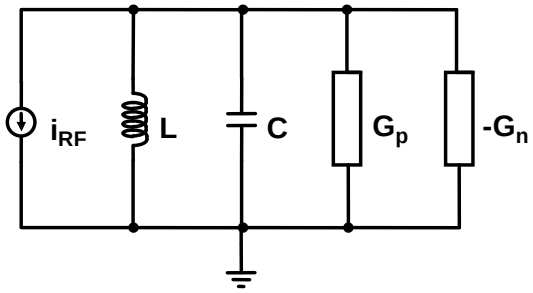


Fig. 3.19: Simplified equivalent model of conventional super regenerative architecture

The current source and LC network represent the input RF signal and the resonator respectively. The resulting tank loss can be modeled by a positive passive conductance, G_p. Additional negative conductance (G_n) is introduced through an active element to cancel this tank loss, and the effective conductance ($G=G_p+G_n$) can be varied by the quench signal. When the tank loss is not fully cancelled ($G>0$), the resonant network behaves like a simple lossy filter network and the oscillation cannot be sustained. When G becomes negative, the resonator oscillates and the output can be represented by the following equation [47]:

$$V = e^{-\alpha t}\left(k_1 e^{j\omega_d t} + k_2 e^{j\omega_d t}\right) + \frac{A\cdot\sin(\omega t+\phi)}{\sqrt{G^2+\left(\omega C-\frac{1}{\omega L}\right)^2}}, \qquad (3.23)$$

where $\alpha = \frac{G}{2C}$ is the dampling factor and $\omega_d = \sqrt{\frac{1}{LC}-\left(\frac{G}{2C}\right)^2}$ is the damping frequency.

Recently, oscillator-type based super regenerative receiver has also been successfully demonstrated for UWB technology [50]. For narrowband super regenerative amplifier,

signal selectivity is very important so that only desired signal get amplified, and thus external high-Q element or additional Q-enhancement circuitry is usually required [47]-[48]. Unlike the narrowband system where the signal selectivity is important, the UWB super regenerative receiver relies on the incoming UWB signal to determine the start-up envelope of the oscillator and thus achieve signal detection and amplification. A quench signal is still required in [50] for the proper operation of the receiver and its waveform will affect the actual performance of the receiver.

For UWB super regeneration receiver, the amplifier is initially reset to lossy filter tank using the quench signal. At the onset of incoming signal, quench signal is varied so that the amplifier is now set to the oscillation mode. The presence of an incoming signal will act as an additional excitation and speed up the oscillation start-up to produce a larger envelope. This results in the super regenerative amplification of the incoming signal. In the absence of the incoming signal, only thermal noise will cause the oscillation start-up and thus generate a smaller envelope. Quench signal has to be used to alternate the receiver between two different operating modes for proper operation. It has been observed that different types of quench waveforms such as sawtooth, triangular, etc. will affect the sensitivity and selectivity performances of the receiver [49]. In addition, the generation of this quench signal is also non-trivial [47].

3.4.3 Proposed Super Regenerative UWB Detector

A novel super regenerative detector for UWB applications will be proposed in this section. The proposed super regenerative UWB detector steers away from the conventional oscillator-type based super regenerative architecture and employs the technique of positive feedback for super regeneration. As a result, it does not require external high-Q resonator

or quench signal to start or decay the oscillations. The architecture of the proposed super regenerative UWB detector is shown in Fig. 3.20.

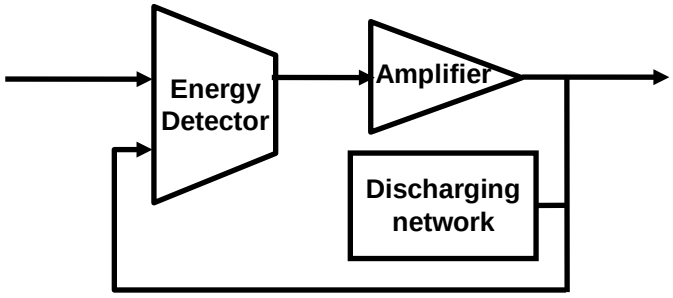


Fig. 3.20: Proposed super regenerative UWB detector

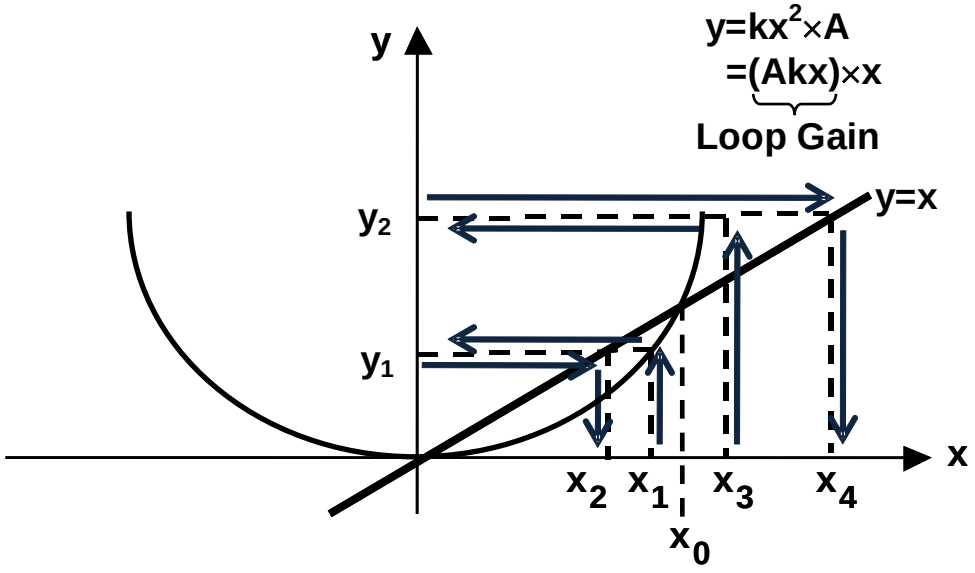


Fig. 3.21: Transfer characteristic of the super regenerative UWB detector

An energy detector (dual input squarer) and an amplifier are connected in positive feedback configuration as shown in Fig. 3.20. As the squarer gain is signal dependent, rail-to-rail amplification is only achieved for loop gain larger than unity. Using this unique characteristic of signal dependent loop gain, the detector can be designed such that the input noise will experience loop gain less than unity and be attenuated whereas the desired

signal will produce loop gain larger than unity and achieve rail-to-rail amplification. An intuitive understanding of the proposed super regeneration principle is shown in Fig. 3.21. The two curves represent the transfer characteristics of the total loop gain ($y=kx^2 \times A=Akx \times x$) and the unity gain ($y=x$). The unity gain line represents the feedback action where the output becomes the input. An input threshold (x_0) can be determined when the loop gain is equal to unity and this value can be set according to the squarer and amplifier gain. Below this input threshold, the input signal will experience attenuation. This attenuated signal, after feedback, would be reduced further, and finally dies down to zero. This is indicated by the route x_1-y_1-x_2 in Fig. 3.21. On the other hand, above this threshold, the input signal will be amplified. This amplification would be reinforced by the feedback path and eventually result in super regenerative amplification, as illustrated by the route x_3-y_2-x_4. After signal detection, the detector output will start to decay from rail-to-rail voltage at a rate determined by the squarer circuit. The schematic of the energy detector with discharging network employed in Fig. 3.20 is illustrated in Fig. 3.22 and 3.23.

The UWB energy detector (Fig. 3.22) is formed using two identical differential squarer circuits (M_1-M_4 and M_5-M_8) sharing a common active load with common mode feedback. As discussed in Section 3.2.3, for each differential squarer, the left transistor pair M_1-M_2 (or M_5-M_6) will generate both a squared term and a DC term (Equation 3.14) while the right transistor pair M_3-M_4 (or M_7-M_8) will produce an identical DC term (Equation 3.15). The first squarer (M_1-M_4) would process the output from the LNA (v_x), whereas the second squarer (M_5-M_8) would take the amplifier output (v_y) and form a positive feedback loop. Taking the differential output will eliminate the DC term for both

squarers and result in the desired squared terms of the input v_x and the feedback signal v_y as shown:

$$V_{out} = V_{out+} - V_{out-} = Z_L\left(2\beta_A v_x^2 + 2\beta_B v_y^2\right) \tag{3.24}$$

where Z_L is the output load impedance, $\beta_A = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_A$ is the transistor device parameter for M_1-M_4, $\beta_B = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_B$ is the transistor device parameter for M_5-M_8, v_x is the LNA output and v_y is the amplifier output.

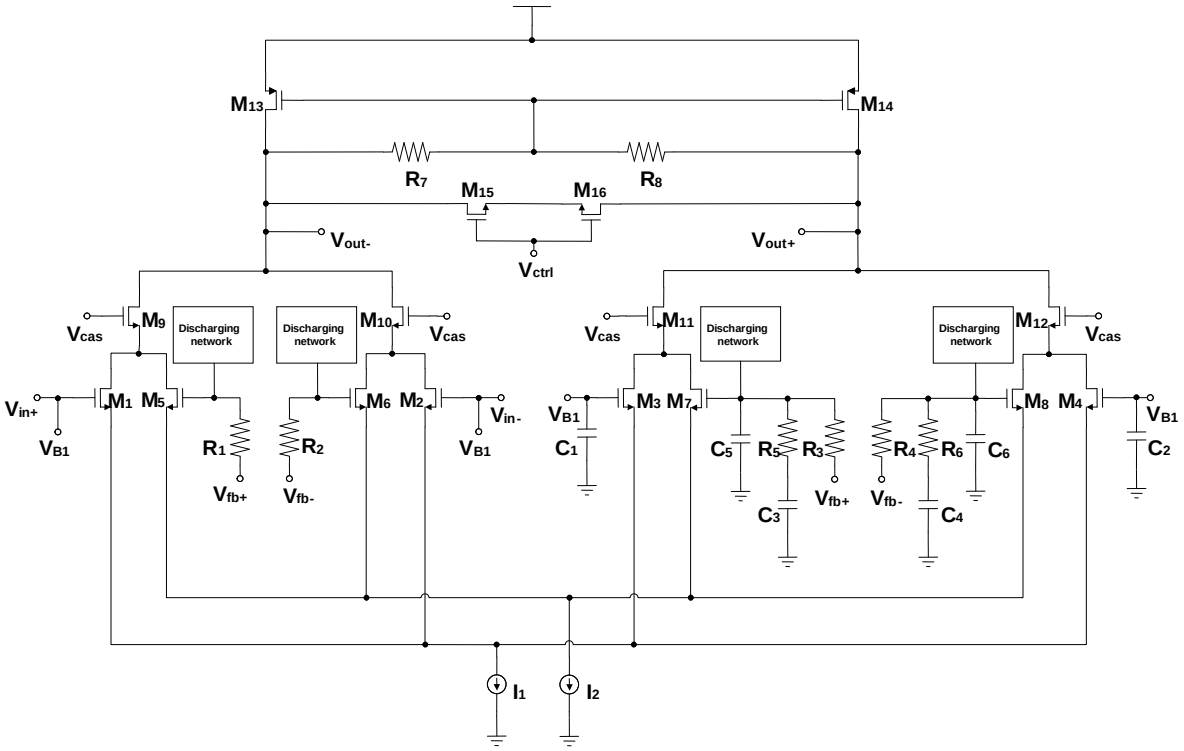


Fig. 3.22: Proposed UWB energy detector

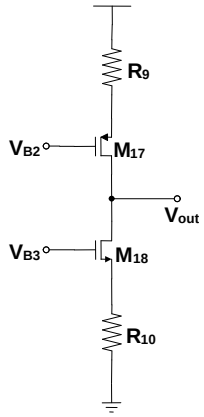


Fig. 3.23: Proposed discharging network

It should be noted that unlike the first squarer, the DC bias for the second squarer is extracted from the detector output through a simple RC filter (R_3-R_6 and C_3-C_6). This will provide the necessary decay after the signal detection. The cut-off frequency of this RC filter not only determines the decay rate but also the stability of the proposed positive feedback loop. A larger cut-off frequency generates smaller amount of positive feedback, which results in faster decay rate and a more stable system with reduced overall detector gain. To further speed up the decay of rail-to-rail output, a discharging network shown in Fig. 3.23 is used. It consists of two high output impedance current source and sink with limited voltage operating range. For small detector output, both the current source and sink match and have very little effect on the squarer circuit. For rail-to-rail detector output, either the current source or sink will remain functional, thus causing the capacitor to quickly charge or discharge back to its initial state.

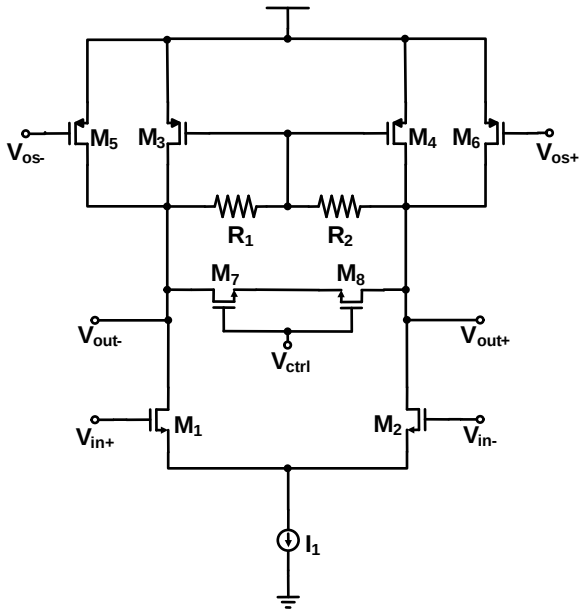


Fig. 3.24: Proposed differential amplifier

A simple differential amplifier employing active load is proposed here by the author as the amplifier in the super regenerative detector as shown in Fig. 3.24. Its input is DC coupled from the output of the energy detector to maximize the regenerative gain of the detector and avoid long settling time during switching. Offset cancellation circuit is also employed here and it has been presented in Fig. 3.16.

In order to achieve greater power savings in impulse radio based UWB systems, the transceiver blocks can be switched off when there is no input signal. Since the UWB pulses are only of nano-seconds pulse width, there is a great potential for enhanced power savings in low data rate systems. However, due to the high super regenerative gain, the switching glitches resulting from the burst mode operation can easily get amplified and saturate the output. Therefore, two pairs of reset switches (M_{15}, M_{16} for the energy detector and M_7, M_8 for the amplifier) are used to reset the output to zero during the power up of the various transceiver blocks. In addition, the current source implementation

in Fig. 3.6 is also used here to provide the tail currents for both the energy detector and differential amplifier to achieve power savings.

The simulation result is shown in Fig. 3.25. The resulting super regenerative UWB detector is able to achieve rail-to-rail amplification for input signal as small as 26 mV peak-to-peak and consumes a combined current of 8 mA.

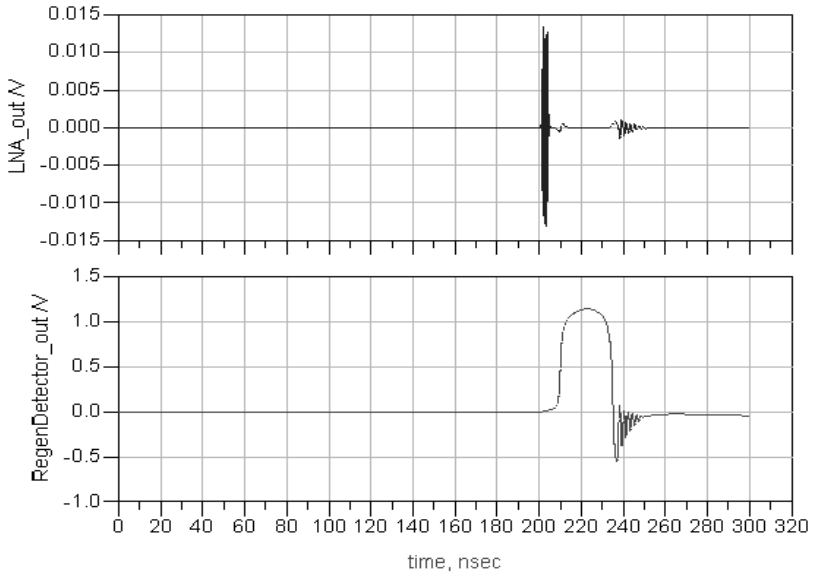


Fig. 3.25: Transient simulation result for super regenerative UWB detector

Chapter 4

Proposed UWB Transceiver Design

This chapter presents the proposed design of two UWB transceivers that are suitable for use in low power applications such as the wireless sensor networks. The architecture of each transceiver will be presented and discussed, followed by its simulation or measurement results. The focus of this thesis is on the design of the receiver portion. However, for completeness, the transmitter portion, which is done by other members of the UWB team, will be briefly described in this section.

4.1 A CMOS Low Power Burst Mode UWB Transceiver

The low power burst mode 3-5 GHz UWB transceiver is a non-coherent based architecture as shown in Fig. 4.1.

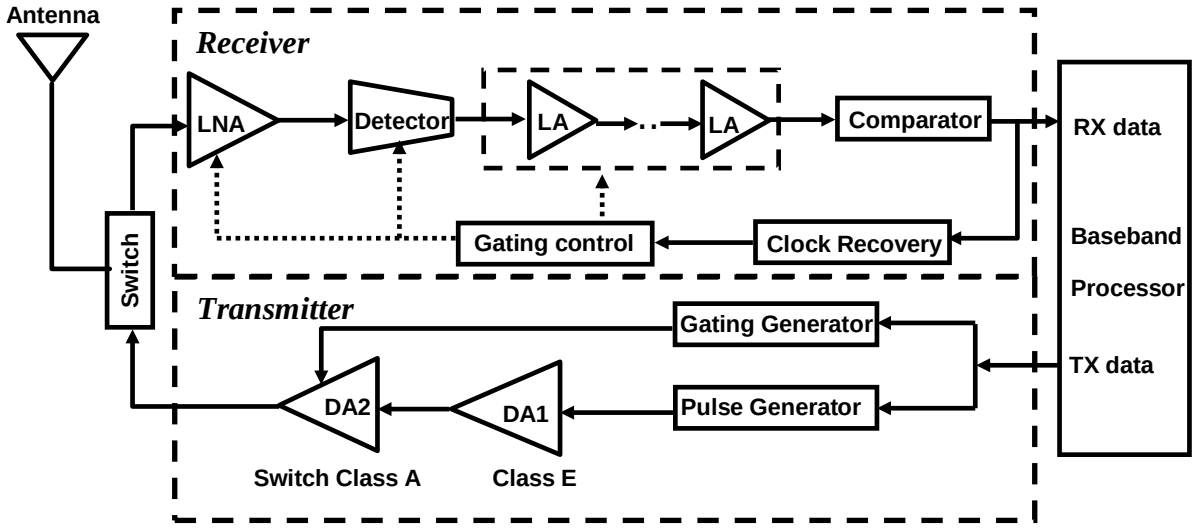


Fig. 4.1: Low power burst mode UWB transceiver architecture

Fig. 4.2: Measured result for low power burst mode UWB transceiver

The UWB transmitter in Fig. 4.1 has been published in [51], which consists of a pulse generator as well as a class E and a switch class A driver amplifier. The transmitter generates on-off keying (OOK) UWB pulses, which are amplified and emitted through the UWB antenna. In the receiver, the received signals are first amplified by the LNA (Fig. 3.2) and then demodulated through a squarer (Fig. 3.8), a cascade of five limiting amplifiers with offset extraction circuits (Fig. 3.15 and 3.16), and a comparator. In Fig. 4.1, a clock recovery circuit and gating control, which will not be discussed in this thesis, can be implemented in the receiver for burst mode operation to switch on/off the transceiver blocks and thus enable greater power saving for low data rate applications.

The measured receiver performance is shown in Fig. 4.2 using a pseudo-random sequence of 25 Mbps (Mega bits per second) pulses from the transmitter. The data recovered from

the comparator output is correctly demodulated as shown. The peak power dissipation of the receiver is 44.6 mW.

The transceiver chipset is fabricated using Chartered Semiconductor Manufacturing (CSM) 0.18-µm CMOS technology. The chip is directly mounted on a Quad Flat No-lead (QFN) package and soldered onto Printed Circuit Boards (PCB) to minimize the package parasitics. The transceiver performance is summarised in Table 4.1. The die occupies an area of 2.5mm×3mm and is shown in Fig. 4.3.

Table 4.1: Summary of low power burst mode UWB transceiver performance

Performance	
Supply voltage	1.8 V
Technology	0.18-µm CMOS
Die size	2.5mm x 3mm
Transmitter	
Pulse width	0.5 ns
Bandwidth (-10dB)	1.9 GHz
Output peak-peak swing	0.6 V
Average power dissipation	522 µW @ 20 Mbps
Data rate	1-100 Mbps
Receiver	
IIP3	-13.2 dBm @ 4 GHz
Sensitivity	-82 to -78 dBm
LA gain	0-60 dB
Average power dissipation for LNA	1.44 mW @ 20 Mbps
Peak power dissipation	44.6 mW

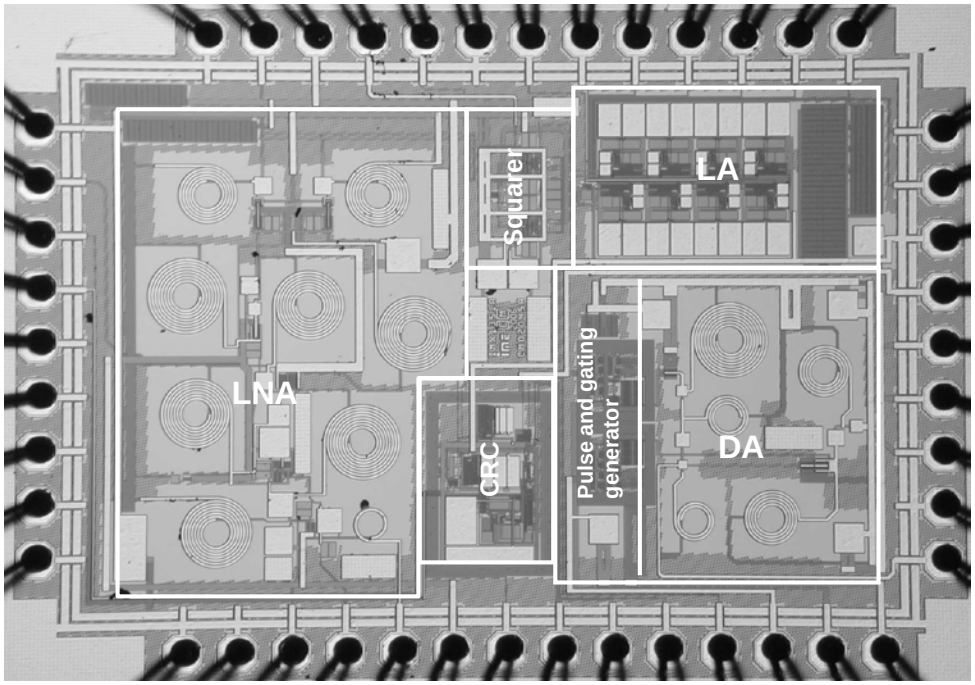


Fig. 4.3: Chip microphotograph of low power burst mode UWB transceiver

4.2 A Burst Mode Super Regenerative UWB Transceiver

Fig. 4.4 shows the proposed 3-5 GHz super regenerative UWB transceiver architecture. Non-coherent on-off keying (OOK) signaling scheme is chosen due to its simplicity and low power consumption as compared to the coherent approach, which would require additional timing synchronization and channel estimation circuitries.

The transmitter consists of a pulse generator using time gated LC voltage controlled oscillator (VCO). It is capable of achieving high output swing of 2V suitable for long range communications with low power consumption. The buffer and balun convert the differential input signal into the single-ended output and provide the desired 50 Ω output impedance matching to the antenna.

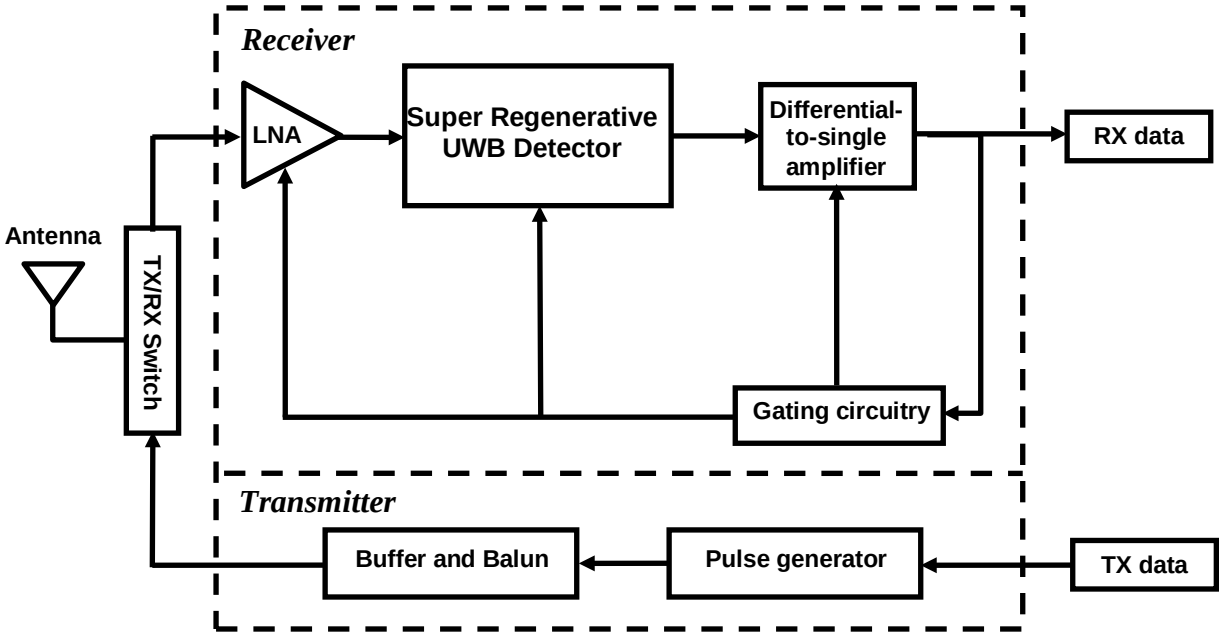


Fig. 4.4: Burst mode super regenerative UWB transceiver architecture

For the receiver, incoming signal received by the antenna is first amplified by the high gain LNA (Fig. 3.4). High gain is necessary in the LNA to compensate for the significant signal loss for small signals due to the squarer ($y=kx^2$) and thus improve the overall sensitivity. The signal is then processed by the super regenerative UWB detector (Fig. 3.20). Due to the rail-to-rail amplification, a simple differential-to-single-ended amplifier can be used as a slicer to recover the digital data. A gating circuitry will utilize this final output to synchronize the power up/down control signal (assuming data rate is known) with the incoming signals so as to turn on the receiver only for a short period at the correct instant. Based on the received data, the gating circuitry generates the EN signals to switch on/off tail current sources of the LNA, detector and amplifier, and the V_{ctrl} signal for the detector (Fig. 3.22) and amplifier (Fig 3.24) to avoid false data detection caused by the switching glitches resulting from the powering up of the transceiver blocks. The gating

circuitry operating cycle can be made programmable through a programmable counter based on the given data rate. Initially, the whole transceiver is powered up and searching for the received signal with the counter free running. Once the received data is detected, the counter would be reset to mark the beginning of the data cycle. The desired control signals, EN and V_{ctrl}, would then be generated according to the counter value. As shown in Fig. 4.5, the onset of received data resets the counter and a periodic EN and V_{ctrl} are generated thereafter. Once all the blocks are successfully powered up, V_{ctrl} signal would go low to enable normal operation. In the simulation, EN signals of pulse width of 160ns and V_{ctrl} of 90ns are used for a given data rate of 5Mbps. The settling times of the various circuit blocks has been taken into consideration in generating the control signals.

The die of the proposed transceiver is fabricated in 0.18-μm CSM CMOS technology and occupies 2.2mm×2mm (excluding pads) as shown in Fig. 4.6. The recovered data for different transmitted pulse widths at 100kbps, 1Mbps and 5Mbps is shown in Fig. 4.7. The peak power consumption for the receiver is 34.4mW, with almost 95% of it belonging to the LNA and super regenerative UWB detector. Using the gating circuitry for burst mode operation at a data rate of 1 Mbps with a power on duration of 100ns, the average power consumption is 334μW, corresponding to an energy efficiency of 3.34nJ/bit. By exploiting the duty cycle in burst mode operation, the gating circuitry helps to achieve larger power saving at low data rate compared to the conventional transceivers with continuous operation, and is suitable for wireless sensor networks application. The transceiver chip is packaged using QFN technology and mounted onto a Rogers PCB. The transceiver performance is summarized in Table 4.2.

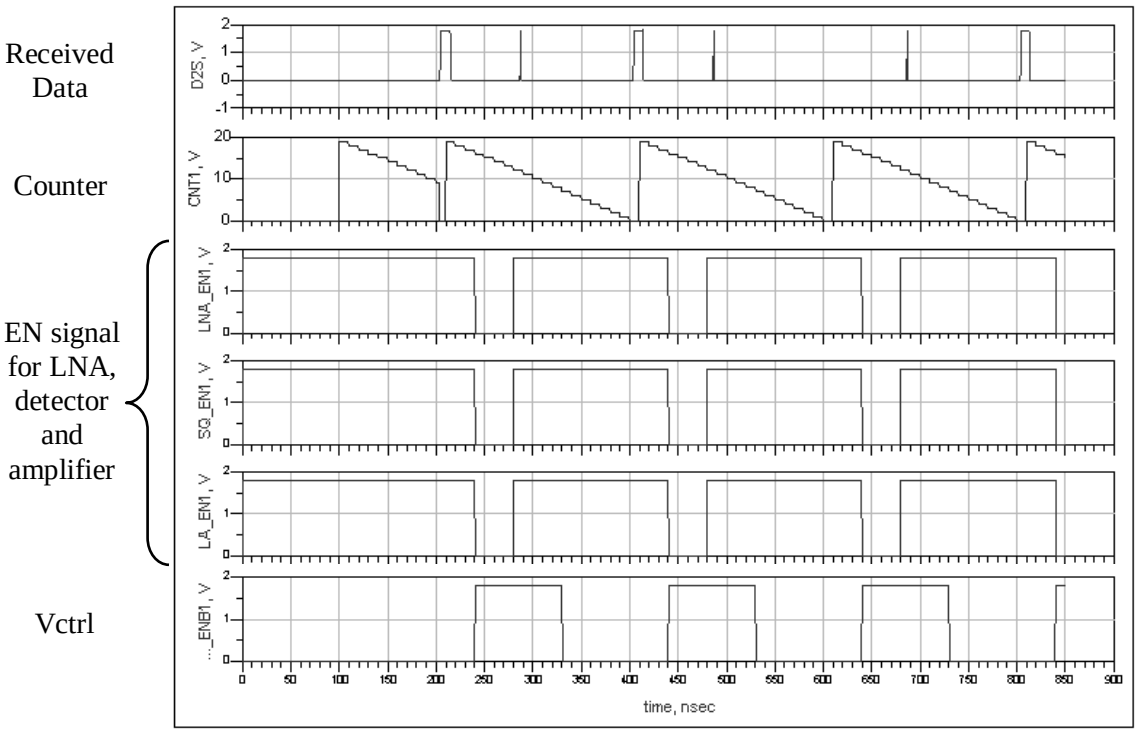


Fig. 4.5: Simulation of the gating circuitry at 5Mbps

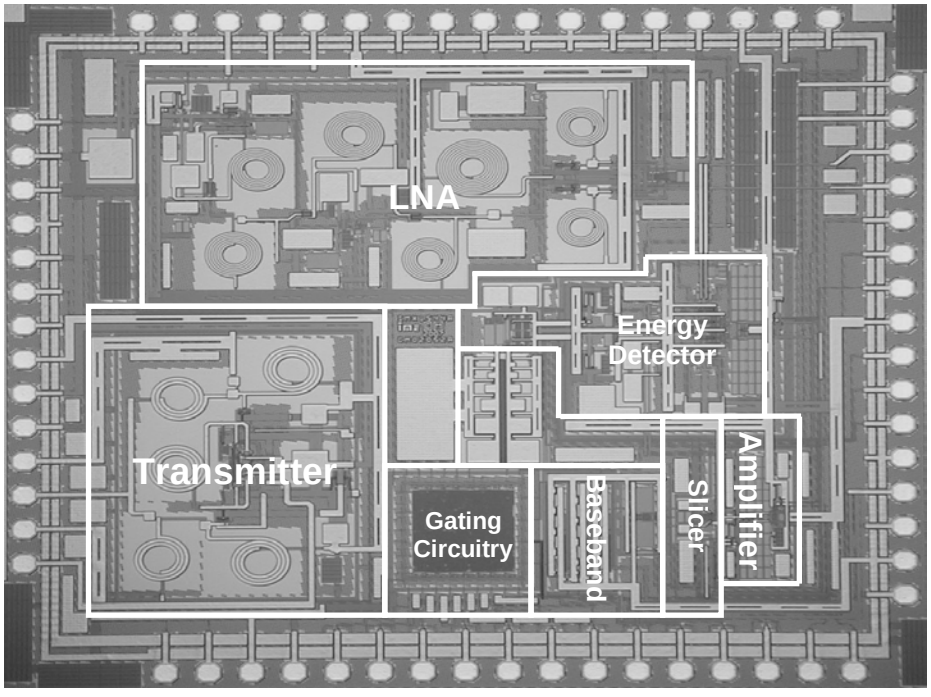


Fig. 4.6: Chip microphotograph of super regenerative UWB transceiver

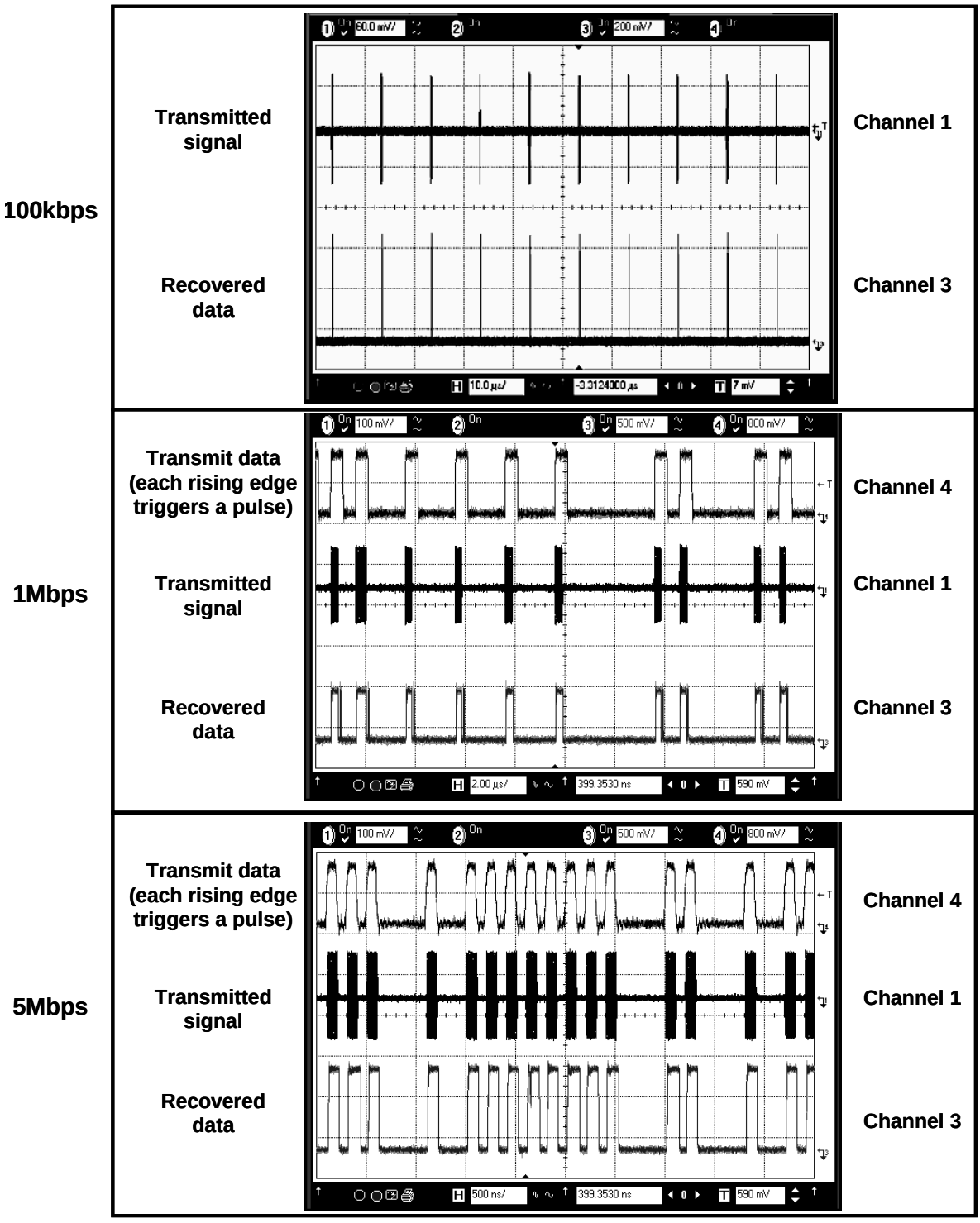


Fig. 4.7: Measured performance of super regenerative UWB transceiver

Table 4.2: Summary of super regenerative UWB transceiver performance

Performance	
Technology	0.18-µm CMOS
Die size	2.2mm x 2mm
Data rate	10kbps to 8Mbps
Transmitter	
Supply voltage	3.3 V
Peak power dissipation	129 mW @ 20Mbps
Energy efficiency	0.671 nJ/bit
Output peak-peak swing	2 V
Receiver	
Supply voltage	1.8 V
Sensitivity	-61 dBm
Peak power dissipation	34.4 mW
Average power dissipation	334 µW @ 1Mbps
Energy efficiency	3.34 nJ/bit

A performance comparison of the two proposed transceivers is shown in Table 4.3. Both transceivers employ the same 0.18-µm CMOS technology for cost and integration considerations. With the proposed super regenerative transceiver, the die area is reduced by 41% as compared to the low power burst mode transceiver. However, the transmitter portion in the super regenerative transceiver consumes more power than the other proposed transmitter so as to achieve a higher voltage swing at its output. A comparison of the two proposed receivers shows a 23% reduction in power consumption by employing the super regenerative architecture. However, the super regenerative transceiver achieves a poorer sensitivity due to the following reasons. Firstly, the use of positive feedback in the super regenerative architecture would suffer more from circuit and channel noise if it is not carefully optimised, thus degrading the SNR and sensitivity. Secondly, inaccurate

parasitics modelling and insufficient post layout simulations would also cause gain, bandwidth and thus sensitivity degradation in the designed circuit blocks as compared to that predicted in simulations.

Table 4.3: Performance comparison of proposed UWB transceivers

Performance	**Low Power Burst Mode Transceiver**	**Super Regenerative Transceiver**
Supply voltage	1.8 V	1.8 V (RX) 3.3 V (TX)
Technology	0.18-µm CMOS	
Die size	2.5mm x 3mm	2.2mm x 2mm
Transmitter		
Pulse width	0.5 ns	5.2 ns
Bandwidth (-10dB)	1.90 GHz	1.36 GHz
Output peak-peak swing	0.6 V	2.0 V
Average power dissipation	522 µW @ 20 Mbps	13.4 mW @ 20Mbps
Receiver		
Sensitivity	-78 to -82 dBm	-61 dBm
Peak power dissipation	44.6 mW	34.4 mW

Table 4.4 shows the performance comparison of the low power burst mode transceiver (presented in Section 4.1) with recent published UWB receivers/transceivers operating within the 3-5 GHz spectrum. It should be noted here that only [23] and [52] are UWB receivers while all the other are UWB transceivers. It can be observed here that the use of non-coherent impulse radio approach is able to achieve lower power consumption than the coherent approach as coherent demodulation requires synchronization and power hungry blocks such as the frequency synthesizer for LO generation. Furthermore, with duty-

cycling, the proposed transceiver is able to achieve lower average power consumption. The achieved sensitivity is better than all works in Table 4.4 except [22], which employs 90nm CMOS technology.

Table 4.4: Performance comparison of proposed low power burst mode transceiver with recent works

References	[18]	[22]	[23]	[52]	This Work
Technology	0.18-µm CMOS	90nm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.18-µm CMOS
Die Area [mm^2]	4.42	0.08 (TX) 2.20 (RX)	4.00	4.16	7.50
Frequency [GHz]	3.1 – 5	3.1 – 5	3.1 – 5	3 – 5	3.1 – 5
Approach	Coherent Impulse Radio	Non-Coherent Impulse Radio	Non-Coherent Impulse Radio	Coherent Impulse Radio & OFDM	Non-Coherent Impulse Radio
Power Consumption [mW]	76 (TX) 81 (RX)	0.718 (TX average)	31	80	0.522 (TX average) 44.6 (RX)
Energy Efficiency [nJ/bit]	–	0.043 (TX) 2.5 (RX)	–	–	–
Power Supply [V]	1.80	0.65	1.80	1.20	1.80
Sensitivity [dBm]	-80 – -72	-99	-70	-70	-82 – -78

Table 4.5 shows the performance comparison of the proposed super regenerative UWB transceiver (presented in Section 4.2) with recent published super regenerative receivers/transceivers. The operating frequency of the proposed transceiver is the widest compared to all recent super regenerative works, covering the lower band (3-5GHz) of the UWB spectrum. Its performance is comparable to the super regenerative receiver in [53]

but [53] requires an external quench signal since its super regeneration is based on conventional oscillator technique. The lower sensitivity achieved can be attributed to the inaccurate models employed in simulations and the larger noise bandwidth in the receiver since it is catered for UWB operations as compared to the other works. Furthermore, the circuit can be optimized more thoroughly to achieve better performance.

Table 4.5: Performance comparison of proposed super regenerative UWB transceiver with recent works

References	[47]	[48]	[49]	[53]	This Work
Technology	0.13-µm CMOS	CMOS	0.8-µm BiCMOS	0.13-µm CMOS	0.18-µm CMOS
Frequency [GHz]	2.4	1.9	0.3 – 1.5	3.0 – 4.0	3.0 – 5.0
Approach	Narrowband Super Regenerative	Narrowband Super Regenerative	Narrowband Super Regenerative	UWB Super Regenerative	UWB Super Regenerative with time gating
Modulation	OOK	OOK	OOK	PPM	OOK
Power Consumption [mW]	2.8	0.4 (RX) 1.6 (TX)	1.2	11.2	34.4 (RX) 129.0 (TX)
Power Supply [V]	1.2	1.0	2.0	1.2	1.8 (RX) 3.3 (TX)
Energy Efficiency [nJ/bit]	5.60	80 (RX)	–	1.12	3.34 (RX) 0.671 (TX)
Sensitivity [dBm]	-90.0	-100.5	-98.0	-99.0	-61.0
Quench signal	Internal digital	External	Internal	External	–

4.3 Layout Considerations

To ensure that the fabricated transceivers perform as in simulations and minimize non-ideal effects such as mismatch, a lot of thought and effort have been devoted to the layout stage. Some of the major considerations in the process of drawing the layouts include:

- Common centroid structure is used for differential circuits such as the squarer and super-regenerative detector to minimize the layout mismatch.
- In other differential circuits where common centroid is not practical or critical, geometrically symmetric structure is used instead.
- RF signal lines have been routed using top metal layers to minimize chances of coupling from the substrate.
- For the high-gain LNA, all the ground terminals for the different stages have been separated to eliminate any feedback paths, which might result in instability.
- For every supply voltages, wide multi-layer metals are used to reduce the resistance and large decoupling capacitors have been implemented on-chip.
- Guard rings with taps have been used for isolating the noisy digital circuits from the rest of the RF and analogue blocks.
- Electrostatic Discharge (ESD) protection circuits are used for all pads.
- Careful floor planning is done to ensure that the inter-connections between the transceiver blocks are as short as possible, especially the connection between the input (output) pads and the LNA RF input transistor (transmitter RF output transistor).
- Dummy poly layers are used on both ends of poly resistors.

Chapter 5

Conclusion and Future Directions

5.1 Conclusion

Two transceiver architectures for wireless sensor network applications have been presented in this thesis, namely the low power burst mode UWB transceiver and the burst mode super regenerative UWB transceiver. Both transceivers are based on the non-coherent architecture and are thus of low system complexity and low power consumption. For low data rate applications, the power consumption of the transceivers can be significantly reduced with the help of gating circuitries to switch on/off the transceiver building blocks.

In the proposed UWB transceivers, building blocks such as the LNA, squarer, limiting amplifier, super regenerative UWB detector were designed and implemented by the author in CSM 0.18-µm CMOS technology. A LNA was designed for high gain of more than 40 dB to compensate the squarer loss in the non-coherent approach. A simple squarer with a current consumption of 2 mA and conversion gain of 40 dB was designed to capture the signal energy. In the limiting amplifier design, a cascade of 5 gain stages with offset cancellation circuits was employed to achieve a total gain of 60 dB with a bandpass characteristic of 288 kHz to 1 GHz. A new super regenerative UWB detector was also designed to achieve large gain with minimum circuit blocks through the positive feedback technique. It is able to achieve rail-to-rail amplification with a UWB input signal of 26 mV peak-to-peak.

All design and simulations of the circuits were done with the Agilent Advanced Design System software using 0.18-µm CMOS technology models from Chartered Semiconductor Manufacturing. All the layouts were drawn using Cadence Virtuoso software.

5.2 Future Directions

The following points can be taken into consideration for future directions:

- The die area for the LNA can be significantly reduced by replacing some or all of the big passive inductors with active ones. In addition, the possibility of reducing the number of stages can be looked into as well.
- For the burst mode super regenerative UWB transceiver, the proposed discharging network in Fig. 3.19 consumes 2.2 mA for the differential signals. It can be better designed and optimized to consume even lesser current for a lower average power and higher energy efficiency.
- The burst mode super regenerative UWB transceiver has to be tested in noisy environments to verify that useful signals above the threshold can be amplified in the positive feedback loop without degradation in the output SNR.
- The sensitivity of the super regenerative UWB transceiver can be further improved upon through more accurate parasitics modelling and extensive post-layout simulations.

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Appendix A

Publication List

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