# SPACE VECTOR PULSEWIDTH MODULATION FOR MULTILEVEL INVERTERS AND SOLUTIONS TO MODULATION DEPENDENT PROBLEMS

AMIT KUMAR GUPTA
(B. ENG. IIT-ROORKEE, INDIA)

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# Contents

# Summary

The Space vector PWM (SVPWM) is a prominent modulation technique for multilevel inverters similar to two-level inverters. However, due to complex geometry of the space vector diagram and a large number of switching states, the implementation of SVPWM for multilevel inverters is considered complex. The complexity is due to the difficulty in determining the location of reference vector, the calculation of on-times and the determination and selection of switching states.

In linear range, maximum obtainable voltage is 90.7% of six-step. It can be increased further by properly utilizing the DC link capacity through overmodulation. However, the aforementioned complexity of SVPWM implementation increases further in the overmodulation range due to the nonlinearities of this region.

To deal with these problems, a general SVPWM algorithm is proposed for multilevel inverters. The proposed algorithm is based on standard two-level SVPWM which greatly simplifies the modulation process. In the proposed algorithm, irrespective of the level $n$, the computations remain same. The implementation of the proposed algorithm is experimentally shown for two widely used topologies of multilevel inverter, namely neutral point clamped (NPC) and cascaded H-bridge.

Similar to two-level inverter, multilevel inverters produce common mode voltage. This results in bearing currents that can lead to bearing failure. Schemes have been reported for multilevel inverters to reduce the common mode voltage. However, most of the schemes result in reduced modulation depth, high switching losses and high harmonic distortion. In this thesis, a scheme to reduce common mode voltage for cascaded inverters is proposed which is based on the proposed general SVPWM algorithm. This scheme can increase the voltage range of operation by about 17% and can produce lower THD than the previously proposed schemes.

The use of asynchronous PWM technique for the inverter produces subharmonics and interharmonics. These harmonics lead to several undesired effects on grid connected applications. This necessitates the need for synchronous PWM. The close loop control of synchronous PWM is complex especially during dynamics. The PWM for multilevel inverter is fairly complicated as compared to two-level inverter. Hence, aforementioned problem is more severe when multilevel inverter is used as a voltage source inverter. To deal with these problems a scheme is proposed for the close loop flux control of a grid connected cascaded multilevel inverter.

The 3-level NPC inverter is widely used topology. However, it is known to have neutral point fluctuation problem. At low modulation index, the fluctuations can be compensated using redundant switching states. But at higher modulation index and in overmodulation region, the neutral point fluctuation deteriorates the performance of the inverter. A simple SVPWM scheme is proposed for operating a three-level NPC inverter at higher modulation indices including overmodulation range while maintaining the neutral point balance.

# List of Tables

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# List of symbols

| | |
|---|---|
| $\alpha$-$\beta$ | Coordinate system of the reference vector |
| $\alpha_o$-$\beta_o$ | Coordinate system for the small vector |
| $\boldsymbol{v}^*$ | The reference vector |
| $(v_\alpha, v_\beta)$ | Coordinates of the reference vector |
| $\boldsymbol{v}^s$ | The small vector |
| $(v^s_{\alpha o}, v^s_{\beta o})$ | Coordinates of the small vector |
| $V_{dc}$ | DC-link voltage of the inverter |
| $V_{C1}$, $V_{C2}$ | Voltages across DC link capacitors |
| $n$ | Level of Inverter |
| $h$ | Height of a triangle |
| $m_i$ | Modulation Index |
| $S_i$ | Sector Number |
| $\triangle_j$ | Triangle Number |
| $\theta$ | Angle with respect to $\alpha$ axis |
| $\gamma$ | Angle with respect to $\alpha$ axis within first sector |

| | |
|---|---|
| $f_s$ | Switching frequency |
| $t_a, t_b, t_o$ | On-times of the switching vectors |
| $d_a, d_b, d_o$ | Duty ratios of the switching vectors |
| $t_{am}, t_{bm}, t_{om}$ | Modified on-times |
| $d_{am}, d_{bm}, d_{om}$ | Modified duty ratios |
| $m_{max2}$ | Boundary value of overmodulation-I and II |
| $\lambda$ | Factor used in overmodulation I |
| $\alpha_c$ | Angle with respect to $\alpha$ axis within first sector |
| $\alpha_h$ | hold angle |
| $V_{UV}, V_{VW}, V_{WU}$ | Line Voltages |
| $I_U, I_V, I_W$ | Line Currents |
| $V_{WTHD}$ | Weighted total harmonic distorsion |
| $npf$ | Percentage neutral point fluctuation |
| $npf_{max}$ | Maximum percentage neutral point fluctuation |
| $V_0$ | Medium vectors of a three-level NPC inverter |
| $V_{Si}$ | Short vectors of a three-level NPC inverter i=1→6 |
| $V_{Mi}$ | Medium vectors of a three-level NPC inverter i=1→6 |
| $V_{Li}$ | Large vectors of a three-level NPC inverter i=1→6 |
| $d_{S1}, d_{S2}$ | Duty ratios of small vectors |
| $d_{L1}, d_{L2}$ | Duty ratios of large vectors |
| $d_{S1m}, d_{S2m}$ | Modified duty ratios of small vectors |
| $d_{L1m}, d_{L2m}$ | Modified duty ratios of large vectors |

| | |
|---|---|
| $V_{dc(HB)}$ | DC-link voltage for cascaded H-bridge inverter |
| $V_{NG}$ | Common mode voltage |
| $i_{NG}$ | Common mode current |
| $f_h$ | Frequency of $h^{th}$ harmonic |
| $E_h$ | EMF generated due to $h^{th}$ harmonic |
| $\psi_h$ | flux due to $h^{th}$ harmonic |
| $\psi_g$ | Grid flux vector |
| $\psi_c$ | Inverter flux vector |
| $\psi_c(k)$ | Inverter flux vector in $k^{th}$ cycle |
| $\psi_c^*$ | Reference inverter flux vector |
| $\Delta\psi_c$ | Inverter flux error vector |
| $\psi_s$ | Flux linkage associated with synchronous reactance |
| $\boldsymbol{x}_s$ | Synchronous reactance |
| $\boldsymbol{i}_s$ | Current through synchronous reactance |
| $\boldsymbol{v}_g$ | Grid voltage vector |
| $\boldsymbol{v}_c$ | Inverter voltage vector |
| $\boldsymbol{v}_s$ | Voltage across synchronous reactance |
| $\chi$ | Tuning parameter for the flux estimation |
| $p$ | Active p.u. power |
| $q$ | Reactive p.u. power |
| $\delta$ | The angle between the fluxes $\psi_g$ and $\psi_c$ |
| $\phi$ | Power factor angle |

# List of Abbreviations

| | |
|---|---|
| DSP | Digital Signal Processor |
| PWM | Pulse Width Modulation |
| SPWM | Sin Triangle Pulse Width Modulation |
| SVPWM | Space Vector Pulse Width Modulation |
| CMV | Common Mode Voltage |
| NPC | Neutral Point Clamped |
| NV | Nearest Vectors Scheme |
| SV | Selected Vectors Scheme |
| THD | Total Harmonic Distorsion |
| FFT | Fast Fourier Transform |
| BVR | Bearing Voltage Ratio |

# Chapter 1

# Introduction

This chapter presents an introduction to the work done in this thesis. The chapter starts with a concise survey of various applications, features and topologies of multilevel inverters. Subsequently, the motivation and contribution of the work done is emphasized, following which the relevant literature survey is presented. Finally, the broad outline of the thesis is given.

## 1.1 Multilevel Inverters

There is an increasing interest in industry towards power conversion at medium voltage level for high power applications [1]. Multilevel power converters [2]-[10] are being increasingly adopted [1][7] for such applications.

### 1.1.1 Applications of Multilevel Inverters

The main applications can be divided into two areas,

1. Large Motor Drives: These cover a wide range of high-power loads [1] e.g. pumps in the petrochemical industry, fans in cement industry, traction in transportation industry [11][12], steel rolling mills in cement industry[13], blowers, compressors and conveyors, downhill conveyor system [14] etc.

2. Power Systems Applications: The typical applications are STATCOM [15] [16], UPFC [17], power quality, power conditioners [18], reactive power compensators [19]-[21], grid connected systems [22]-[26] etc.

Apart from these applications some other reported applications are rectifier [27], DC/DC Converter [28], fuel cell utilization [29], arc furnace [30] etc.

### 1.1.2 Main Features and Drawbacks

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages that reach high voltage at the output. The most attractive features [8] of multilevel inverters as compared to two-level inverter are,

1. Lower voltage stress on each switching device.

2. Output voltages with lower harmonic distortion.

3. Lower $dv/dt$ in the output voltage.

4. Lower common mode voltage at the application neutral.

5. Lesser distortion in input current.

6. Operate at lower switching frequency.

7. Lower electromagnetic interference problems.

Some of these features will be explained in this thesis. The typical drawbacks of multilevel inverters are a large number of power semiconductor switches, capacitors, DC source(s), DC-link balancing problems and complexity of control.

### 1.1.3 Functional Diagram of the Multilevel Inverters

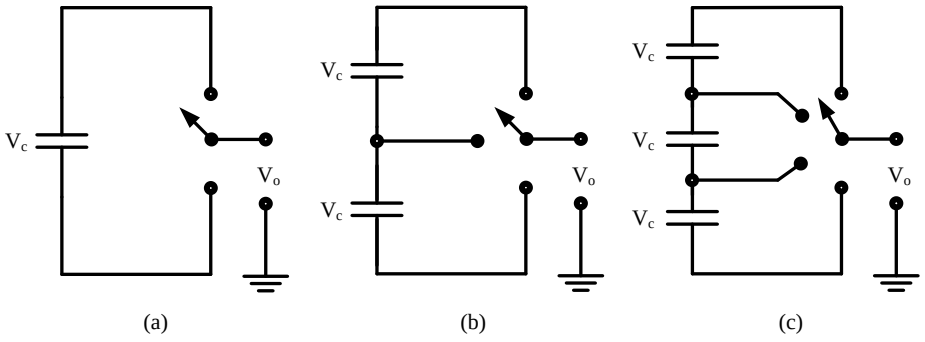



Figure 1.1: The Functional Diagram of Multilevel Inverters

Fig.1.1 explains the functional diagram of multilevel inverters. In Fig.1.1(a) the output $V_o$ can take two possible values i.e. 0 and $V_c$. In Fig.1.1(b) the output

$V_o$ can take three possible values i.e. 0, $V_c$ and $2V_c$. In Fig.1.1(c) the output $V_o$ can take four possible values i.e. 0, $V_c$, $2V_c$ and $3V_c$. It can be extended further. The number of possible outputs represents the level of the inverter. In this thesis, at several places the term '$n$-level' is used in place of 'multilevel'. The values of $n$ in Fig.1.1(a), Fig.1.1(b) and Fig.1.1(c) are 2, 3 and 4 respectively. Here, $n = 2$ represents conventional two-level inverter whereas $n > 2$ represent multilevel inverters. With the increase in $n$ the output has more number of steps leading to sinusoidal waveform. This is the basic idea behind various topologies of multilevel inverters.

## 1.2 Topologies of Multilevel Inverters

There are three main topologies of multilevel inverters.

1. Neutral Point Clamped (Diode Clamped) [31]
2. Cascaded H-Bridge [18][32]
3. Capacitor Clamped (Flying Capacitors) [9][33]

Lai et al. [3] describe the operation of these three topologies and show their detailed comparison. A brief overview of these topologies is given below.

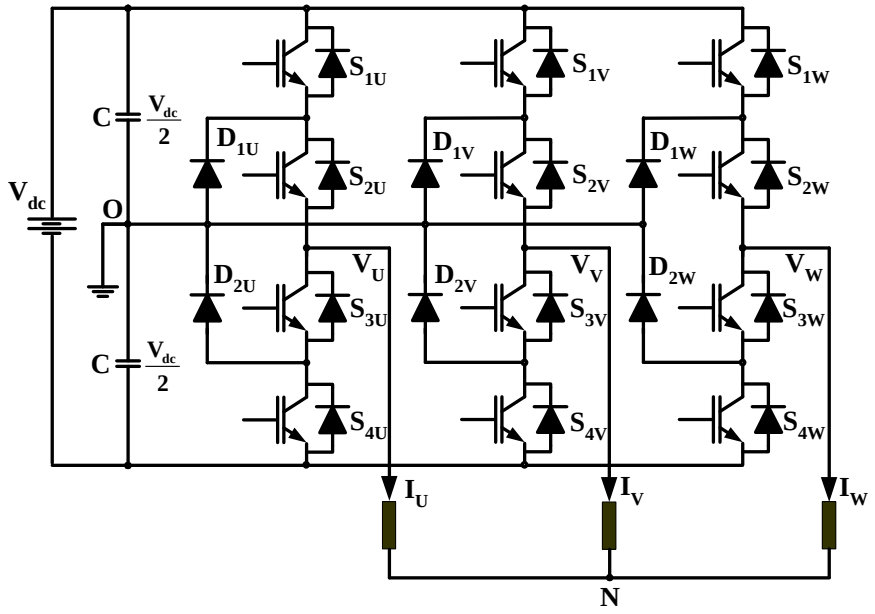



Figure 1.2: Three-level Neutral Point Clamped topology

### 1.2.1 Neutral Point Clamped (NPC) Topology

The neutral point clamped (NPC) topology is also known as diode clamped topology. Theoretically, for a NPC inverter $n$ can take any integer value. The main advantage of the NPC topology is that it requires only one DC source similar to two-level inverter, and gives better performance as mentioned in 1.1.2. However, the number of power components are more than two-level inverter. Fig. 1.2 shows 3-level NPC inverter topology. It consists of two DC-link capacitors, twelve controllable power semiconductor switches with free wheeling diodes and six clamping diodes. The minimum number of components for other levels of NPC topology are given in table 1.1. In this table, the term 'Capacitor' signifies the capacitors in DC-link, the term 'Switches' signifies controllable power semiconductor switches with free wheeling diodes and the term 'Diodes' signifies the clamping diodes.

| Level | Capacitor | Switches | Diodes |
|---|---|---|---|
| 3 | 2 | 12 | 6 |
| 4 | 3 | 18 | 9 |
| 5 | 4 | 24 | 12 |
| . | . | . | . |
| . | . | . | . |
| n | (n-1) | 6(n-1) | 3(n-1) |

Table 1.1: The number of components in NPC topology

When $n$>3, different diodes have to support different voltage levels, from 1/($n$-1) to ($n$-2)/($n$-1) times the $V_{dc}$. The other main disadvantage of this topology is the voltage fluctuation of its DC-link capacitors. For example, ideally the voltage across the two DC-link capacitors should be $V_{dc}/2$ as shown in Fig.1.2. However, in practice due to current flowing through the point O in Fig.1.2, the voltage across two capacitors are not the same leading to some undesirable effects. This problem is commonly known as 'neutral point fluctuation' or 'DC-link unbalancing' problem.

To summarize, with the increase in level $n$, not only the number of clamping diodes increase but also the problem of ensuring the DC-link balance becomes more severe. Due to these reasons, the NPC topology is mainly used for 3-level inverter.

### 1.2.2 Cascaded H-bridge Topology

In this topology the H-bridges are cascaded in every phase. With the increase in H-bridges in a phase, the output voltage waveform tends to be more sinusoidal. Fig. 1.3 shows its 5-level topology. It consists of two identical H-bridges in each phase. In $n$-level topology, ($n$-1)/2 identical H-Bridges are used in every phase.

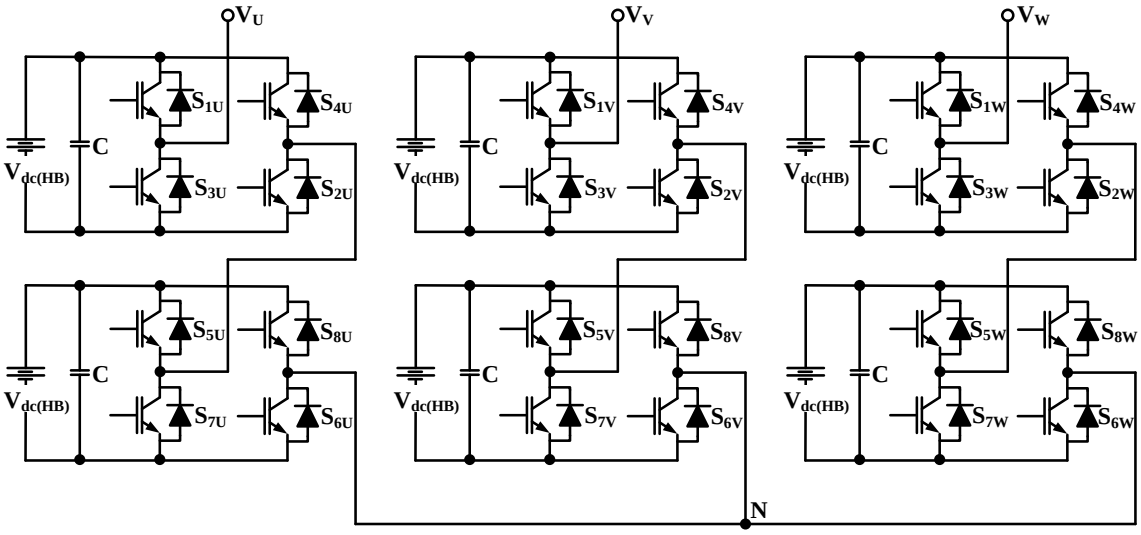



Figure 1.3: The 5-level Cascaded H-Bridge Topology

Identical H-bridges lead to reduction of manufacturing cost which is considered an attractive feature of this topology. However, voltage level at which each bridge operates is different.

There must be a separate DC source for the DC bus of every individual H-bridge, Fig. 1.3. Hence, this topology is useful for collecting energy from renewable energy resources e.g. solar panels and fuel cell. Due to the isolated DC-links, this topology does not have the DC-link unbalancing problem due to neutral point current as in NPC topology explained in 1.2.1.

### 1.2.3 Capacitor Clamped Topologies

It is also known as flying capacitor topology. For this topology $n$ can take any integer value similar to NPC topology. The voltage clamping is done by using

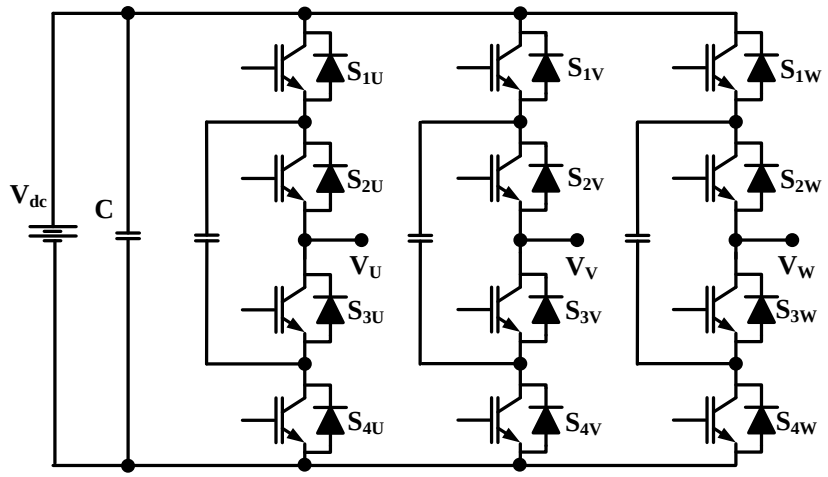



Figure 1.4: The 3-level Capacitor Clamped topology

capacitors floating with respect to the earth potential. Fig. 1.4 shows its 3-level topology. For this topology, the voltage synthesis is more flexible than the NPC topology. However, this topology also exhibits the capacitor voltage unbalancing problem. Since this topology offers more redundancy as compared to NPC topology, the capacitor voltage unbalancing can be reduced by utilizing these redundancies. The main disadvantage of this topology is that it needs a large number of bulky capacitors e.g. a $n$-level capacitor clamped inverter needs a minimum of $3n$-5 independent capacitors. The use of large number of bulky capacitors, most of which need pre-charge circuit, along with the voltage balancing problem of its capacitors inhibit the industrial use of this topology.

Apart from these three main topologies other reported topologies [34]-[36] are essentially different variations of the above three topologies e.g. hybrid topology in [34], generalized topology in [35], combined topology in [36]. Rodriguez et al. [8] briefly describe such topologies.

## 1.3 Motivation - Problem Description

The pulse width modulation (PWM) is a preferred mean of modulating power through the inverter. The typical desired features of a PWM technique are low THD, low switching losses, better DC-link utilization, less computation and simple implementation. However, in practice the PWM techniques for industrial power converters are found to produce some undesired effects. Two such effects are, (i) Common Mode Voltage in motor drives, and (ii) Asynchronous PWM Harmonics in grid connected systems. These are discussed below.

### 1.3.1 Common Mode Voltage

The common mode voltage generated by an inverter is defined as the voltage between apparatus neutral and its ground e.g. in case of an AC drive it is the stator neutral and the system ground. The common mode voltage is the sum of the three phase voltages of the inverter with respect to ground. In any PWM technique the output of every phase is in the form of pulses. Due to this, the common mode voltage also consists of high frequency voltage pulses of certain magnitude which appears between the application neutral and the ground. The common mode voltage leads to common mode current in the system.

According to Julian *et al.*[41] the common mode currents can lead to a number of problems in electrical systems such as malfunctioning of sensitive electronics

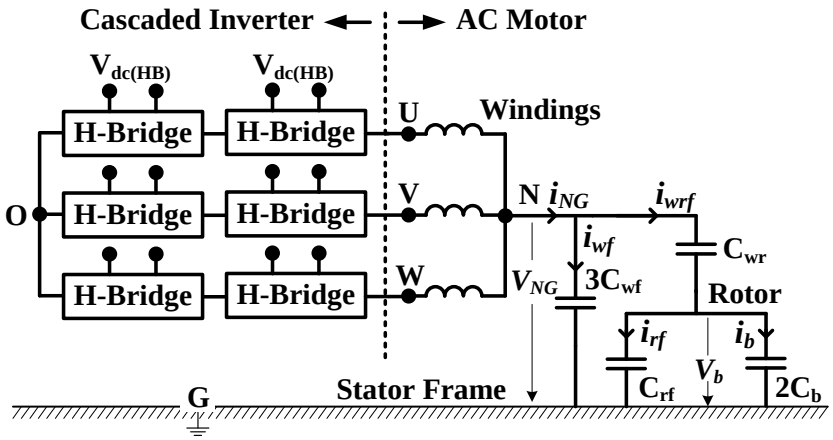



Figure 1.5: Circuit layout of inverter and motor system

and control systems. In electrical network, the common mode currents can cause problems such as false tripping of the ground fault relays.

Recently, it was found [42]-[52] that the common mode voltage leads to bearing currents in electric machines. Wang [53] showed that multilevel PWM voltage source inverter drives can cause motor bearing currents as explained for a two-level drives. The bearing currents cause damage to the motor bearing which lead physical damage of the motor over a period of time. Since, upon damage, the replacement of large motors is expensive and time consuming, the common mode voltage problem is one of the major concerns in medium voltage drives [1].

Fig.1.5 shows a 5-level cascaded H-Bridge inverter and the motor equivalent circuit [52]. This figure uses a simplified form of the 5-level cascaded H-Bridge inverter shown in Fig.1.3. The common mode voltage in Fig.1.5 is $V_{NG} = (V_{UG} + V_{VG} + V_{WG})/3$. This voltage is responsible for bearing currents.

The voltage $V_b$ in Fig.1.5 is the bearing voltage and it depends on $V_{NG}$. The relation between the two voltage is called 'bearing voltage ratio ($BVR$)' described by Busse et al. [45] and is given by Muetze et al. [52] as,

$$BVR = \frac{V_b}{V_{NG}} = \frac{C_{wr}}{C_{wr} + C_{rf} + 2C_b} \tag{1.1}$$

In (4.1) $w$, $r$, $f$ and $b$ stand for winding, rotor, stator frame and bearing respectively. In (4.1) $C_{wr}$ is the capacitance between machine winding to the rotor, $C_{rf}$ is the capacitance between rotor to the frame and $C_b$ is the bearing capacitance.

Muetze [54] explains the cause of various types of bearing currents. For a conventional motor with ungrounded rotor there are three main types of bearing currents,

1. Electrostatic Discharge Machining (EDM) Current: this current is caused when bearing voltage $V_b$ exceeds a threshold voltage $V_{b,th}$ ($\approx 5 \cdots 30$ at bearing temperature of 20$^o$C). When $V_b > V_{b,th}$, the lubrication film between balls and the running surface breaks down leading to a EDM current pulse.

2. Capacitive Bearing Current ($i_b$): this current can be expressed as,

$$i_b = C_b.dV_b/dt = BVR.C_b \cdot dV_{NG}/dt. \tag{1.2}$$

3. Circulating Bearing Current: this current is caused by high $dV_{NG}/dt$ through the stator winding to frame capacitance $C_{wf}$.

Hence, it can be concluded that to reduce the bearing currents, we need

- low magnitude of $V_{NG}$ to avoid discharge currents,
- low value of $dV_{NG}/dt$ to reduce capacitive and circulating currents and
- low frequency of $dV_{NG}/dt$ occurrences.

Multilevel inverter generates stepped output waveform. Hence, it naturally reduces $dV_{NG}/dt$ [55]. However, low magnitude of $V_{NG}$ and low frequency of $dV_{NG}/dt$ occurrences are also desired to reduce the bearing currents.

### 1.3.2 Asynchronous PWM Harmonics

The ratio of switching frequency $f_{sw}$ and fundamental frequency $f_1$ is called 'pulse number'. The ratio $f_{sw}/f_1$ is an integer for synchronous PWM, and non-integer for asynchronous PWM. Asynchronous PWM leads to harmonics which are non-integer multiples of fundamental frequency. The harmonics less than fundamental frequency are known as subharmonics and those more than fundamental frequency are known as interharmonics [56]-[59].

To explain further, let $f_h$ be the $h^{th}$ harmonics in the spectra of output voltage. The $h = 1$ corresponds to fundamental component. The integer value of $h$ correspond to typically referred harmonics. Whereas, non-integer values of $h$ correspond to subharmonics and interharmonics. Thus, depending on $h$ they are described as,

1. Harmonics: $h$ is positive integer, and $h \neq 1$

2. Subharmonics: $h$ is non-integer, and $0 < h < 1$

3. Interharmonics: $h$ is non-integer, and $h > 1$

These harmonics are observed during the experiment as shown in Fig.1.6. These results correspond to conventional asynchronous SVPWM. Fig.1.6(b) and Fig.1.6(c) show typical subharmonics and interharmonics respectively. The experiment is performed on a 5-level cascaded H-bridge inverter shown in Fig.1.3. The experimental conditions are, DC-link voltage $V_{dc} = 165V$, modulation index $m_i = 0.9$, fundamental frequency $f = 50Hz$ and sampling period $T_s = 550\mu s$.

Large motor drives are one of the main applications of multilevel inverters (section 1.1.1). According to Holtz [57][60], in a motor drives system the subharmonics produce low-frequency torque harmonics that leads to high mechanical stress and entails fatigue problems.

Recent research [61]-[73] has shown that these harmonics have severe consequences in power systems. One of such consequence of these harmonics is flux distortion. This can be explained using the following equation which is derived from Faraday's law [56][74].

$$E_h = 4.44 N f_h \psi_h \tag{1.3}$$

In this equation, $E_h$ is the EMF generated, $N$ is the number of turns, and $\psi_h$ is the flux due to $h^{th}$ harmonics.

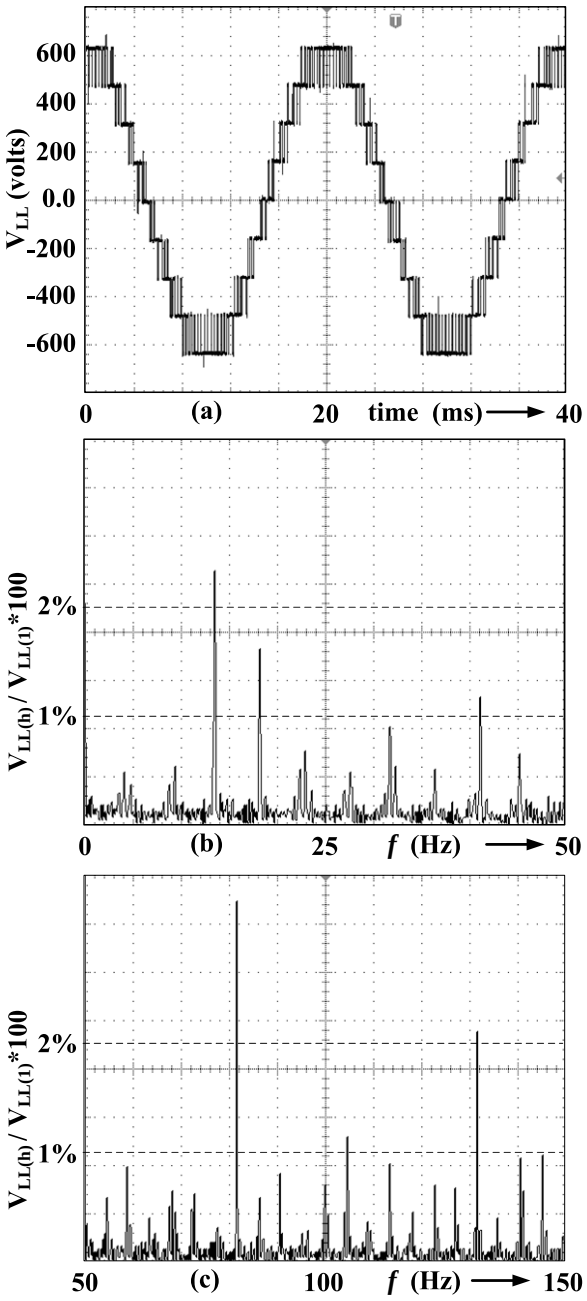



Figure 1.6: Experimental Results (a) Inverter line voltage, (b) FFT for 0→50Hz to show subharmonics, (c) FFT for 50Hz→150Hz to show interharmonics for conventional SVPWM at $V_{dc(HB)}$=160V, $m_i$=0.9, $T_s$=550$\mu$s

Since, $4.44N$ $(= E_1/f_1)$ is constant, the (1.3) can be rewritten as,

$$\psi_h = \frac{E_h}{4.44Nf_h} = \frac{f_1}{E_1}\frac{E_h}{f_h} \propto \frac{E_h}{f_h} \tag{1.4}$$

The implications of (1.4) are explained with following example. In Fig.1.6 the magnitude of 1Hz component is approximately 0.24% of the fundamental component, the corresponding $\psi_h$ is approximately 12% of $\psi_1$. The magnitude of 4Hz component is approximately 0.45% of the fundamental component, the corresponding $\psi_h$ is approximately 5.6% of $\psi_1$. The magnitude of 13.4Hz component is approximately 2.35% of the fundamental component, the corresponding $\psi_h$ is approximately 8.75% of $\psi_1$. Similarly, $\psi_h$ can be calculated for all other components in Fig.1.6. These components of flux are superimposed on fundamental flux $\psi_1$ leading to significant distortion of the flux. Testa et. al. [74] have explained this phenomenon through detailed experiments.

Some of the consequences [74] of voltage harmonics, even for very small amplitudes, superimposed to the fundamental are, (i) torque oscillations in turbogenerators [75], (ii) AC motor aging [76], (iii) malfunctions of remote control systems [77], (iv) erroneous firing of thyristor apparatus [77], (v) lighting system flicker or display and monitor image fluctuations [78], (vi) erroneous behavior of instrumentation based on phase locked loop (PLL) [74].

Apart from removal of non-integer harmonics, the symmetry in the output waveform improves the inverter performance. The typically required symmetries are three-phase symmetry and half-wave symmetry. The three-phase symmetry ensures that the harmonics and the fundamental of three phases are balanced [79]. Hence, the triplen harmonics are cancelled from the line voltage. The half wave

symmetry ensures the elimination of even harmonics from the output voltage [79].

Thus, for a close loop control of grid connected multilevel inverter, a suitable PWM technique is required where the problems described above can be eliminated. Moreover, the chosen PWM technique should also be suitable for obtaining fast dynamic response of the close loop system.

### 1.3.3 Required Features in a PWM Technique

The problems described in previous two sections are significantly dependent on the modulation technique. Hence, their mitigation or reduction is also dependent on using a suitable modulation technique. In a modulation technique, it can be assumed that in every switching cycle a switching sequence consisting of some discrete switching states is applied for the pre-determined on-times. The cause of common mode voltage and asynchronous PWM harmonics due to a modulation technique is briefly explained below.

1. It is possible to reduce common mode voltage i.e. $V_{NG}$ through careful selection of switching states. To fulfill this objective, low magnitude of $V_{NG}$ and low frequency of $dV_{NG}/dt$ occurrences are required as explained before. The magnitude of $V_{NG}$ and frequency of $dV_{NG}/dt$ occurrences depends on; (i) the switching states used in a switching sequence, (ii) the number of switching states used per switching sequence, (iii) additional switching transitions while moving from one switching sequence to another.

2. Asynchronous PWM harmonics are produced when the ratio of switching frequency and the fundamental frequency i.e. the pulse number is not an integer. Proper selection of switching frequency and suitable arrangement of switching states is required to obtain the waveform symmetries. Fast dynamic response is related to simplicity of implementation. Moreover, the switching losses can be reduced by reducing the number of switching states per switching cycle.

Hence, in an algorithm which addresses these problems, the proper selection of switching states and their sequence are important as these problems are mainly dependent on the PWM technique used. The space vector PWM (SVPWM) is a potential PWM technique which can fulfill these objectives. This is because; (i) the SVPWM offers a number of redundant switching states. For an $n$-level inverter there are $n^3$ switching states in its space vector diagram. Among them $(n-1)^3$ are redundant switching states. For example, for a 5-level inverter there are 125 switching states and among them 64 are redundant switching states, (ii) the SVPWM directly deals with the switching states and their sequence. Various optimized switching sequences can be formed using the redundant switching states.

Apart from this, other useful merits of SVPWM are; (i) it directly uses the control variable given by the control system and identifies each switching vector as a point in complex $(\alpha, \beta)$ space, (ii) it is suitable for DSP implementation. (iii) it offers improved DC-link utilization. However, the implementation of SVPWM for

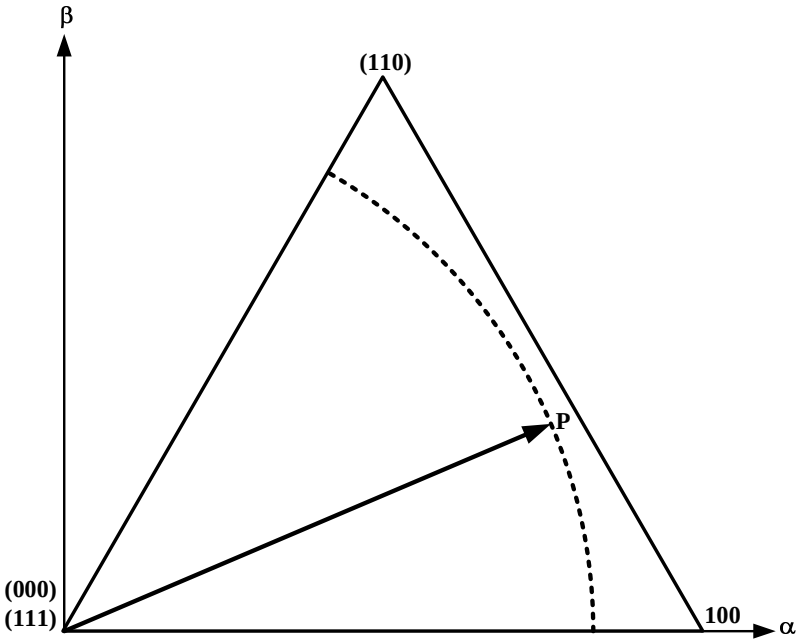



Figure 1.7: The Space Vector Diagram of a two-level Inverter

a multilevel inverter is considered complex [80]. This problem is described in next section.

### 1.3.4 Multilevel Space Vector PWM (SVPWM)

An $n$-level inverter consists of $6(n-1)$ controllable power semiconductor switches as compared to 6 switches for a two-level inverter. The space vector diagram (SVD) of a three-phase voltage source inverter consists of six sectors. Fig. 1.7 and Fig. 1.8 show the first sector of SVD for a two-level inverter and 5-level inverter respectively. Let us compare these two diagrams to understand the problems in implementing SVPWM for multilevel inverters.

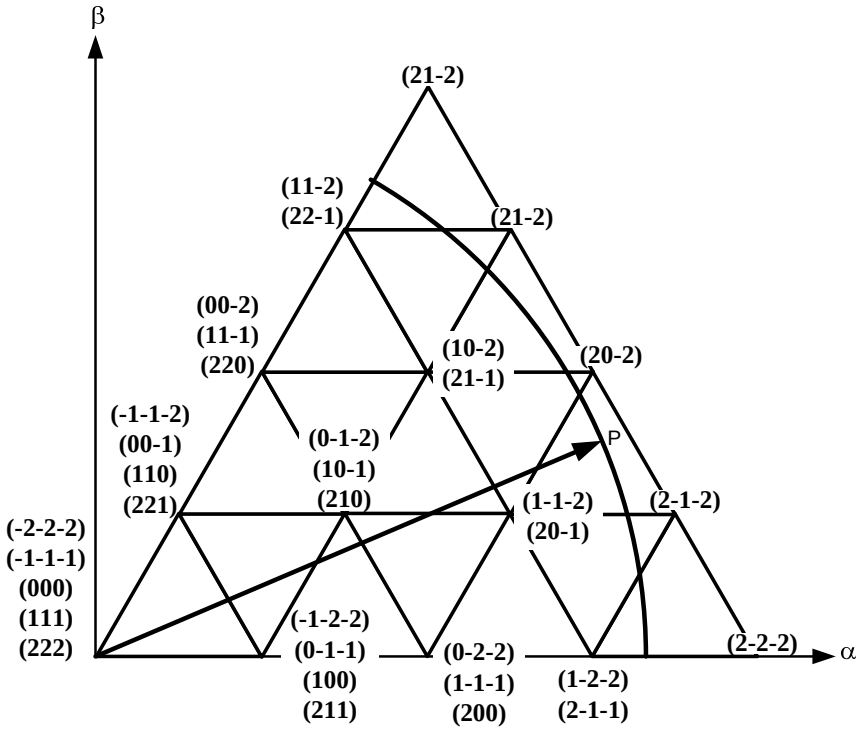



Figure 1.8: The Space Vector Diagram of a 5-level Inverter

1. Compared to two-level SVD (Fig. 1.7), the sector is divided into sixteen smaller equilateral triangles for a 5-level SVD (Fig. 1.8). These triangles are identified using the symbol $\Delta_j$, where $j$=0→15. In SVPWM, nearest three vectors are selected to keep the THD and switching losses low. Hence, it is necessary to know the triangle $\Delta_j$ where the tip of the reference vector is located. Such a problem does not exist for two-level SVD as shown in Fig. 1.7. There are $(n-1)^2$ triangles in a sector for $n$-level inverter. Hence, the complexity of determining the triangle $\Delta_j$ increases with $n$ i.e. the level of inverter.

2. For a two-level inverter in Fig. 1.7, the on-times of the three vertices are calculated using a set of three equations [81]. These equations remain same

for any location of the reference vector. Hence, in two-level SVPWM the on-time calculation is straight forward. Small triangles in the space vector diagram of 5-level inverter in Fig. 1.8 do not exactly imitate the geometry of a sector of two-level inverter in Fig. 1.7. Hence, the on-time calculation in various triangles of 5-level inverter is complicated as compared to two-level inverter.

3. For a two-level inverter there are four switching states associated with a sector as shown in Fig. 1.7 and 8 ($2^3$) switching states for the complete space vector diagram. However, for a 5-level ($n$-level) inverter there are 125 ($n^3$) switching states in its space vector diagram. Fig. 1.8 shows the switching states for the first sector of a 5-level inverter. In SVPWM, in every switching cycle a switching sequence is applied on the inverter. In case of two-level inverter the formation of switching sequence is very straight forward as there are only four switching states per sector. However, for multilevel inverter it is complicated since every triangle has numerous switching states e.g. the inner most triangle in Fig. 1.8 associates with 13 switchings states. The selection and utilization of these switching states is complicated. As mentioned before, the solution to the problem of common mode voltage (section 1.3.1), and those associated with the asynchronous PWM harmonics and symmetries (section 1.3.2) lies in proper selection and sequencing of the switching states. Thus redundant switching states in multilevel SVPWM can be used to address these problems.

In SVPWM, the normalized output voltage of the inverter can be described by modulation index ($m_i$), the $m_i$ ranges $0 \leq m_i \leq 1$ [81]. The range $0 \leq m_i \leq 0.907$ is linear modulation range. The above described problems in implementing SVPWM are essentially for linear modulation range. The $0.907 < m_i \leq 1.0$ is overmodulation range. In linear range the maximum obtainable voltage is 90.7% of the six-step value. It can be increased further by properly utilizing the DC link capacity through overmodulation [81]-[83] but at the cost of some lower order harmonics. The problems in implementing overmodulation for a multilevel inverter are described following section.

### 1.3.5 Overmodulation for Multilevel Inverters

There are two main problems in implementing overmodulation for multilevel inverters;

1. Overmodulation range is nonlinear in nature. To deal with the nonlinearity, the magnitude and angle of the reference vector has been modified in [81][82] to obtain the required fundamental vector for a two-level inverter. This process needs a preprocessor which makes the implementation complex and costly. Due to complex geometry of the space vector diagram this problem is more severe for a multilevel inverter.

2. In overmodulation range the reference vector follows a combination of circular and hexagonal trajectory unlike linear range where it is only circular. The

problem of implementing SVPWM for circular trajectory i.e. linear range is described above (section 1.3.4). Due to combined operation of circular as well as hexagonal trajectory in overmodulation range, the implementation of SVPWM for overmodulation region is even more complex as compared to linear region.

The problem of implementing SVPWM in linear and overmodulation region described above are generic in nature and independent of the topology of the inverter. Neutral point clamped topology discussed in section 1.2.1 is widely used topology. However, when a conventional SVPWM is applied to 3-level NPC inverter, it leads to neutral point fluctuation problem [84]. This problem is discussed in next section.

### 1.3.6 Neutral Point Fluctuation Problem in NPC Inverter

The DC-link of the 3-level NPC inverter shown in Fig. 1.2 consists of two capacitors. In ideal condition, these two capacitors equally share the DC-link voltage i.e. $V_{dc}/2$. However, in reality the voltages across these capacitors are not same, leading to degradation of the output voltage waveform and unequal voltage stress on the power semiconductor devices [84]. This problem is known as DC-link fluctuation problem in NPC inverter.

The main cause of the neutral point imbalance is the current at the neutral point O, Fig. 1.2. The other causes of neutral point potential drift as described by

Yamanaka et.al. [85] can be nonuniform switching and non-ideal DC-link capacitors. According to this study, such imbalances can lead to slow but continuous drift of the neutral point potential. Dynamic operating conditions such as acceleration or deceleration of load drives can also result in neutral point potential drift. Under such conditions, these fluctuation can be rapid and significant. To summarize, the neutral point fluctuation can be caused by both the modulation technique and the operating conditions of the inverter. The variation in neutral point voltage depends on the modulation technique used. However, as the output voltage and load current magnitudes increase and power factor (PF) approaches zero, the neutral point potential fluctuation increases. Under such operating conditions, the performance of the 3-level NPC inverter degrades. For a reliable operation of this topology, the neutral point balance should be ensured. This problem becomes more severe at high modulation index especially in overmodulation region.

Celanovic et.al.[84] provide a detailed insight into this problem. The neutral point fluctuation is directly related to the switching state vectors. For 3-level space vector diagram, the switching vectors can be divided into four types of vectors; zero vector $V_0$, short vectors $V_{Si}$, medium vectors $V_{Mi}$ and large vectors $V_{Li}$, where $i$ = 1→6. The zero vector and large vector do not affect the neutral point balance but the short and medium vectors affect the neutral point. Neutral point balancing techniques normally require appropriate selection of switching states and utilization of their on-times. Since, the SVPWM directly deals with switching states and their on-times, it can be used for neutral point balancing problem.

### 1.3.7 Summary

Due to the advantages described in section 1.1.2, multilevel inverters are used in large motor drives and power system applications (section 1.6). The voltage source inverters are operated using PWM that produce some undesired effects. In motor drives, the common mode voltage is one such effect (section 1.3.1). In grid connected systems, the asynchronous PWM harmonics is another such effect (section 1.3.2). These problems are significantly dependent on PWM technique used.

The space vector PWM is a suitable technique to deal with these problems. However, the implementation of SVPWM for multilevel inverter is considered complex (section 1.3.4). Hence, a simple method of implementing SVPWM is required. Furthermore, in linear range the maximum obtainable voltage is 90.7% of the six-step value. It can be increased further by properly utilizing the DC link capacity through overmodulation. However, due to the non-linearity of the overmodulation range the implementation is not easy (section 1.3.5).

The conventional PWM technique when applied to NPC topology may lead to neutral point fluctuation (section 1.3.6). Since, the SVPWM technique directly deals with redundant switching states and their on-times, this technique is suitable for obtaining the neutral point balance. Nevertheless, a simple SVPWM scheme needs to be developed to ensure neutral point balance for 3-level NPC topology.

The problems described above are motivation of the work in this thesis. It is clear from the previous discussion that implementation of SVPWM in linear and overmodulation range is a generic problem. Hence, these problems are dealt first in this thesis. Having obtained their solution, the problems related to common mode voltage are addressed first, followed by a solution to the problems related to asynchronous PWM harmonics. Finally, a simple SVPWM scheme is given for the problem of neutral point fluctuation. This sequence of dealing with problems is followed in rest of the thesis. In next section a literature survey of the work done on these problems is discussed.

## 1.4 Background Work - Literature Survey

Let us start with the literature survey on the problems in implementing multilevel SVPWM as discussed in section 1.3.4.

### 1.4.1 Multilevel Space Vector PWM

There are three main requirements to implement SVPWM for multilevel inverters, (i) sector $S_i$ and triangle $\Delta_j$, (ii) on-times of the three nearest vectors, (iii) switching sequence for the given switching cycle. The switching states in the sequence are applied for the calculated on-times to generate switching signals.

There are two common approaches to obtain the on-times. The first approach

is to determine the triangle and solve three simultaneous equations for this triangle to obtain the on-times as shown by Ishida [86]. The second approach is to determine the triangle and use particular on-time equations stored in a lookup table for this triangle, as shown by Mondal [87]. However as the number of level increases, both of these approaches become computationally intensive.

Recently general algorithms [88] and [89] are proposed to obtain on-times for SVPWM in linear modulation range [81]. An euclidean vector system based SVPWM algorithm is presented by Celanovic [88], it is quite involved due to the use of several matrix transformations. Furthermore, [88] does not provide a systematic approach for determining the switching states nor does it provide a realtime implementation. Wei [89] proposed an algorithm which is a different representation of the algorithm in [88]. This algorithm uses a coordinate system where the axes are $60^o$ apart to calculate on-times and determine switching states. Since most control schemes provide a voltage reference in orthogonal coordinate system, the $60^o$ transformation adds to complexity.

In this thesis, a simple algorithm to perform space vector modulation for a multilevel inverter is proposed. The algorithm is based on standard two-level SVPWM, and can be implemented for any level using one counter. Some researchers [90]-[92] have proposed multilevel SVPWM using two-level concept. However, there are some drawbacks in these methods which are alleviated in this thesis.

Among the schemes based on two-level simplification, Zhang [90] introduces

a method for on-time calculation where the 3-level space vector diagram is divided into six two-level space vector diagrams. The location of the centers of six virtual hexagons is found by segregation of the 3-level space vector diagram. The origin is virtually shifted to one of the six centers, and axes are rotated by $60^o$ to use two-level on-time calculation. This method works well for 3-level as the segregation is required only for 3-level. However, can this method be extended to higher levels? The work [90] does not include on-times calculation for level $n$>3.

Seo [91] also proposes a scheme for a 3-level inverter. Similar to Zhang [90], the 3-level space vector diagram is divided into six two-level space vector diagrams. A 2-phase to 3-phase conversion is needed to calculate the point to shift the origin of virtual two-level inverter. Subsequent to the shift of origin and $60^o$ coordinate transformation, on-times are calculated using two-level equations. This scheme cannot be directly applied to a $n$-level inverter. For example, in order to get the on-times for a 5-level inverter, the 5-level space vector diagram has to be divided into six 4-level space vector diagrams, then each 4-level space vector diagram has to be divided into six 3-level space vector diagrams, and finally each 3-level space vector diagram has to be divided into six two-level space vector diagrams. Therefore, it implies that as level ($n$>3) increases, complexity and computation both increase.

Loh et.al. [92] also uses the idea of two-level space vector modulation for a $n$-level inverter. Authors divide the space vector diagram of $n$-level into all possible two-level space vector diagrams and propose to use the transformations as proposed

by Celanovic et.al. [88] to find the center of a two-level hexagon in $n$-level space vector diagram. However, the transformations in [88] are not used just to find the center of a two-level hexagon in the $n$-level space vector diagram, but they directly calculate the on-times using a set of matrix transformations. Hence, the method proposed by Loh et.al. [92] using transformations proposed by [88] with two-level on-time calculation will result in total computations higher than [88]. Thus, these algorithms may use two-level simplification but they cannot be extended to multilevel without substantial computational overload.

In addition to the calculation of on-times, selection of switching states proposed in these methods is not clear. Since, the performance of multilevel inverter is significantly dependent on the selection of the switching states, the optimization of switching sequence is required. The optimization cannot be easily achieved by previous algorithms.

The literature survey given above provide us an overview of the work done on multilevel SVPWM in linear range. However, it essentially does not include overmodulation range. The problems in implementing overmodulation were discussed in section 1.3.5. The literature survey on this problem is given in the next section.

### 1.4.2 Overmodulation for Multilevel Inverters

In the recent literature [93]-[95] overmodulation for multilevel inverters has been reported. McGrath [93] explains the behavior of the key multilevel carrier

based PWM methods for diode clamped, cascaded and flying capacitors topologies in overmodulation region. Mondal [94] performs SVPWM based overmodulation on a 3-level NPC inverter. The on-time calculation equations differ for every triangle which lead to additional computational complexity. Thus, it is cumbersome to extend this scheme to a $n$-level inverter ($n$>3). Saeedifard [95] uses classification algorithm for SVPWM based overmodulation of 3-level NPC inverter. However, it is not clear how it can be extended to a $n$-level inverter ($n$>3).

These studies focus only on the implementation of SVPWM in linear as well as in overmodulation range. However, the problem of common mode voltage discussed in section 1.3.1 is more specific in nature and requires additional insight beyond general SVPWM implementation. The literature survey on this problem is given in the next section.

### 1.4.3 Common Mode Voltage Reduction

The redundant switching states have been used to address the common mode voltage problem for multilevel inverters. These approaches are divided in two types, (i) Complete Elimination (ii) Partial Elimination of common mode voltage.

The complete elimination was first proposed by Ratnayake et.al. [96] for a 3-level NPC inverter. They proposed a carrier based scheme to eliminate the voltage between stator winding neutral N and mid point O of DC-link. In this scheme only those switching states were used for which $V_{NO} = 0$. This idea was also used

by Haoran et.al. [90] for a 3-level NPC inverter where it was implemented using both carrier based and SVPWM techniques, along with their extensive comparison. Authors [90] apply their work to solve the DC-link unbalancing problem of 3-level NPC inverter in [97]. Similar to [90], the idea of making $V_{NO} = 0$ was also used in [98] for a 3-level NPC inverter where it is implemented using synchronous PWM providing smooth pulse-ratio change and a quarter-wave symmetry of the voltage waveform. This approach was applied to cascaded H-bridge inverter in [99] using carrier based schemes. Authors in [99] also try to eliminate the voltage $V_{NO}$ between stator winding neutral N and stator neutral O (Fig.1.5). Redunsara et.al. [100] proposed a scheme whereby the zero sequence voltage for each level is made zero. Rodriguez et.al. [101] also focus on making $V_{NO}$=0 through space vector modulation. This scheme is proposed for low switching frequency and ($n \geq 7$) levels. Let us address schemes which make $V_{NO} = 0$ as 'zero-$V_{NO}$ scheme' e.g. for 3-level NPC inverter [96][90], and for cascaded inverter [99][101].

Fig.1.9 shows the experimental results for the implementation of conventional SVPWM scheme while Fig.1.10 shows the experimental result for the SVPWM implementation of zero-$V_{NO}$ scheme similar to [99][101]. These schemes are applied on a 5-level cascaded H-bridge inverter with $V_{dc(HB)}$=108V, fundamental frequency $f$=50Hz and sampling frequency $f_s$=5kHz.

It can be seen from the $V_{NO}$ trace in Fig.1.9 and Fig.1.10 that though the zero-$V_{NO}$ scheme try to achieve a zero common mode voltage, in practice a large

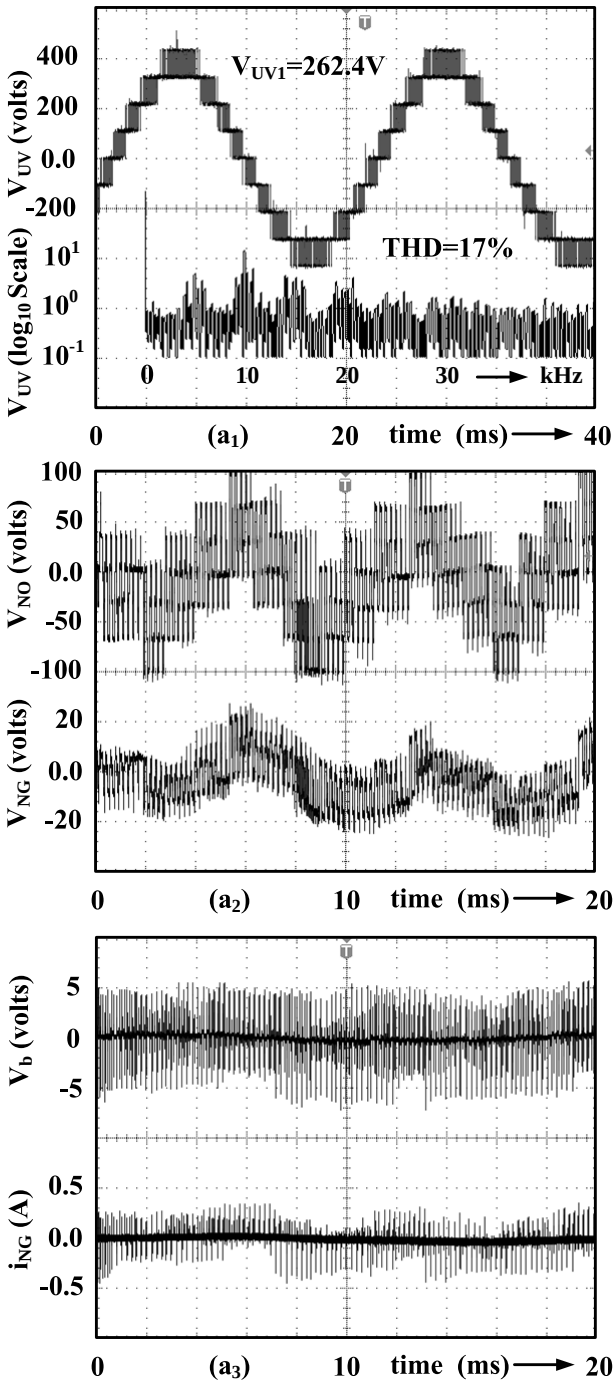



Figure 1.9: Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, voltage $V_{NO}$, voltage $V_{NG}$, voltage $V_b$ and current $i_{NG}$ at $m_i$=0.78 for conventional SVPWM scheme.

occurrences of $dV_{NO}/dt$ are found. This happens due to the switching delays in the practical inverters. The zero-$V_{NO}$ scheme, in its goal to achieve $V_{NO} = 0$, ends

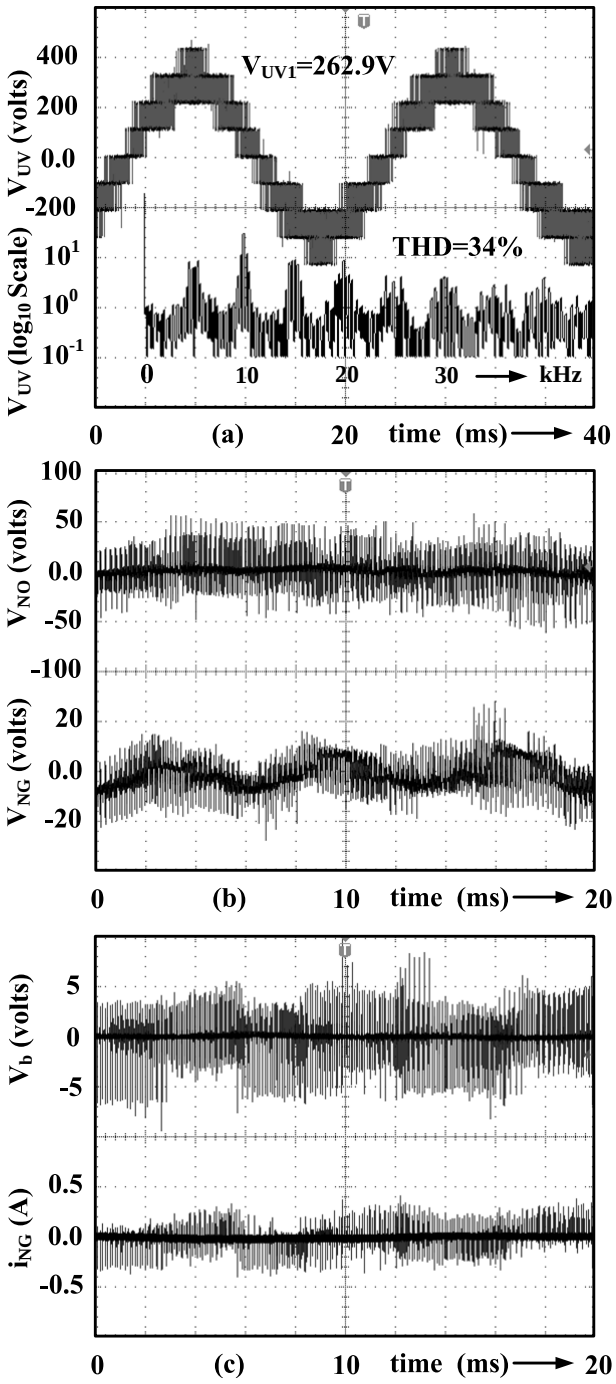



Figure 1.10: Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, voltage $V_{NO}$, voltage $V_{NG}$, voltage $V_b$ and current $i_{NG}$ at $m_i$=0.78 for zero-$V_{NO}$ scheme.

up switching a sequence that does not have minimum number of commutations.

During the transitions, interlock delay of the inverter leg produces a zero sequence

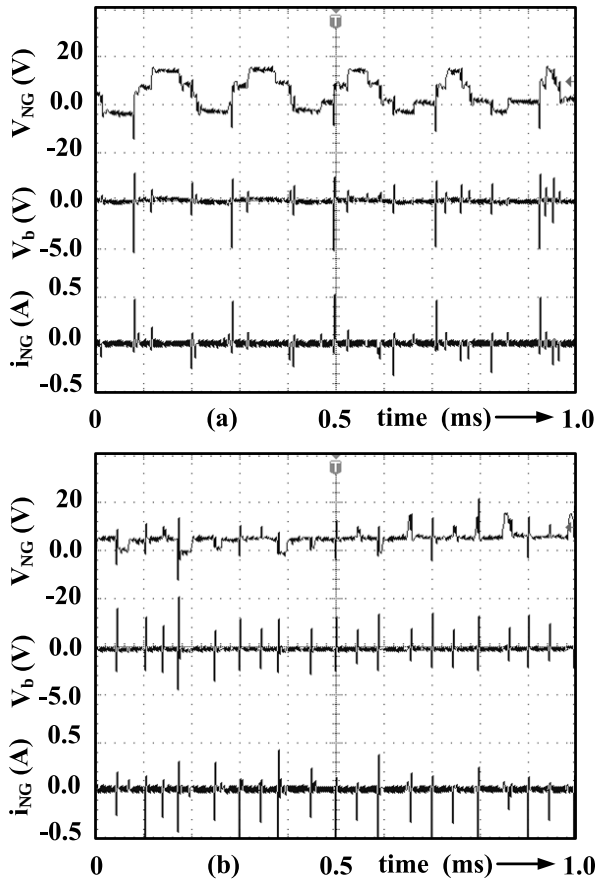



Figure 1.11: Voltage $V_{NG}$, voltage $V_b$ and current $i_{NG}$ at $m_i$=0.78 for (a) conventional SVPWM scheme (b) zero-$V_{NO}$ scheme.

voltage pulse of short duration. Since $V_{NG}$ depends on $V_{NO}$, the voltage spikes occur in $V_{NG}$ also. Consequently, the bearing voltage $V_b$ and common mode current $i_{NG}$ are not equal to zero. With every $dV_{NO}/dt$ occurrence, a spike occurs in $V_b$ and $i_{NG}$. This is verified by experiments as shown in Fig.1.11. The results in Fig.1.11 are for the conventional SVPWM and zero-$V_{NO}$ scheme at the same experimental conditions mentioned above. This is also true for 3-level NPC inverter, as seen in experimental results of Zhang [90] i.e. $dV_{NO}/dt \neq 0$. Thus, the zero-$V_{NO}$ scheme has several disadvantages which are experimentally verified as shown in Fig.1.10-Fig.1.11. Firstly, it does not eliminate common mode voltage but produces high

frequency of $dV_{NG}/dt$s, see trace $V_{NG}$ in Fig.1.10. Secondly, due to the modified switching sequence that have non-minimum commutations, the THD and switching losses increase. It can be easily observed by comparing Fig.1.9 and Fig.1.10 that the number of switchings and THD both are high in zero-$V_{NO}$ scheme. Thirdly, the choice of switching state vector restricts the maximum output voltage e.g. for a 5-level inverter it is only 78.54% of the maximum possible output voltage.

Let us briefly look into the Partial elimination method. It was proposed by Kim et. al. [55] for a 3-level NPC inverter. This carrier based scheme minimizes the voltage $V_{NO}$ by using only those switching states for which $|V_{NO}| \leq V_{DC}/6$, where $V_{DC}$ is the DC-link voltage of the 3-level NPC inverter. In this scheme the four triangles of the sector are not symmetrical. Due to use of non nearest vectors for two triangles, the THD produced by this scheme is higher than conventional method. Moreover, because of asymmetrical triangles the extension of this scheme to higher levels is difficult. Loh et.al. [99] also use the same goal as [55] of achieving a minimum $|V_{NO}|$ for each switching vector but for a cascaded inverter and proposes a carrier based scheme to extend it for higher levels. Two drawbacks are identified for the method in [99], (i) for $m_i \leq 0.7854$ this method generates $|V_{NO}| \leq V_{dc(HB)}/3$ which is minimum possible magnitude as explained by [55] however for $m_i > 0.7854$ this scheme also produces $|V_{NO}| = 2V_{dc(HB)}/3$, (ii) The choice of switching sequence proposed for partial elimination does not produce a minimum number of commutations in each triangle of the switching state diagram. Moreover, when the reference vector moves from one triangle to another, one extra commutation

along with a change in $|V_{NO}|$ might occur.

Hence, the zero-$V_{NO}$ schemes end up producing high frequency of $dV_{NG}/dt$. According to Muetze [54], bearing currents are caused not only due to the magnitude of $V_b$ and hence $V_{NO}$, they also depend on $dV_{NG}/dt$. Hence zero-$V_{NO}$ schemes would require additional $dV/dt$ filters, insulated bearings in the motor or some additional control technique [102] which lead to additional costs. Moreover, the magnitude of $V_{NG}$ and hence $V_b$ is not zero. Hence the question is can we achieve low enough magnitude of $V_{NG}$ with lower frequency of $dV_{NG}/dt$ occurrence without increasing THD and limiting the maximum output voltage to 78.54% of the maximum?

The literature discussed above describes the existing problems in the reduction of common mode voltage. Literature survey on the problems associated with asynchronous PWM harmonics (section 1.3.2) is given in the next section.

### 1.4.4 Asynchronous PWM Harmonics

The asynchronous PWM harmonics have been briefly described in section 1.3.2. They can be eliminated by using synchronous PWM [56][57]. For motor drives a number of solutions [103]-[116] have been proposed on synchronous PWM. However, grid connected multilevel inverter and its close loop operation has not received much attention in this context. Hence, a simple synchronous SVPWM based scheme need to be developed for grid connected multilevel inverter and its

close loop operation. Let us first briefly review the key ideas in implementing synchronous PWM in [103]-[116].

Holtz *et al.* [103]-[105] proposed synchronous optimal PWM for drives where the optimal pulse pattern are pre-calculated and stored i.e. determined offline. The optimization of the pulse sequences is under the assumption that steady-state conditions exist. Minimizing the total harmonic distortion of machine currents is a preferred objective. Satisfying an objective function, a set of switching angles per fundamental period is determined for every steady-state operating point. The scheme proposed in [103][104] are based on current trajectory tracking, while scheme in [105] is based on flux trajectory tracking.

Oleschuk *et al.* [106]-[111] proposed direct synchronous PWM methods. The methods are based on representation of the pulse patterns as a function of the fundamental and switching frequencies of the drive system. It provides smooth pulse-ratio changing and quarter-wave symmetry of the voltage waveforms during the whole control range including overmodulation. Both one stage and two-stage variants of synchronous PWM were considered. Continuous, discontinuous and direct schemes of synchronous PWM with both algebraic and trigonometric control functions have been presented. The schemes have been mainly applied for open loop control of motor drives.

Synchronized SVPWM techniques are proposed by Narananan *et al.* [112]-[115]. Their main contribution is bus-clamping techniques to reduce switching

losses besides achieving the three-phase, half-wave and quarter-wave symmetries in the output waveform for a two-level inverter [112]-[115]. Beig *et al.* [79] applied synchronous SVPWM for 3-level inverter along with waveform symmetries. Subsequently, Beig *et al.* [116] propose a relatively simpler bus-clamping technique for a 3-level inverter. In [112]-[116], these schemes are experimentally verified for open loop $V/f$ control of motor drives.

Yazdani et.al. [24] explain the importance of multilevel inverter in grid connected system. A space vector PWM scheme is proposed in [25] to interface a renewable energy source to the grid using a 3-level inverter. The main emphasize of this scheme is to obtain DC-link balance grid connected 3-level NPC inverter. A space vector PWM scheme is proposed in [26] to control a variable-speed type wind turbine using 3-level NPC inverter.

The above given literature does not address several questions associated with close loop control of a grid connected multilevel inverter. Few such questions are, (i) Is there a suitable synchronous PWM algorithm which can be applied for such close loop control? Can the simplicity in the implementation of synchronous PWM be ensured? (ii) Can a fast dynamic response be obtained? (iii) Can the waveform symmetries and low switching losses be obtained?

The last problem addressed in the thesis is the neutral point fluctuation in NPC inverter (section 1.3.6). The literature survey on this problem is given next.

### 1.4.5 Neutral Point Fluctuation Reduction in NPC Inverter

Several schemes [85]-[97] have been proposed to address the problem of neutral point fluctuation. Broadly, they can be categorized into space vector PWM (SVPWM) schemes [85]-[119] and carrier based PWM schemes [120]-[121].

Space Vector PWM (SVPWM) is an attractive modulation scheme for NPC topology as mentioned before. Generally, the SVPWM methods select nearest three vectors to perform modulation. This approach is known as Nearest Three Vector (NTV) scheme [85] where the duty ratios of the switching vectors and their order are manipulated to compensate the neutral point fluctuation problem, as in [91]. However, such solutions work well at lower modulation index $m_i$ or at power factor near unity. The neutral point balance is easily obtained in the range $0.0<m_i\leq 0.6$ with conventional SVPWM using NTV scheme. The method of neutral point compensation for $m_i>0.6$ including overmodulation is addressed in the thesis.

Sergio et.al. [119] propose a virtual vector based scheme for the linear modulation range. It uses nearest four or five vectors to perform modulation due to the virtual vector. This leads to higher switching losses and harmonic distortion. It selects the switching states such that for a switching period, the summation of three-phase output currents equals zero. This results in a fixed duty ratio for each switching state [119]. Moreover, its operation in overmodulation is not validated.

It is desirable to operate a 3-level inverter in overmodulation region as well.

Overmodulation utilizes the installed DC-link capacity. Schemes for a 3-level inverter in overmodulation range have been proposed in [94][95]. However, the effect of overmodulation on the neutral point unbalancing is not discussed. The methods [85][91] do not discuss the operation in overmodulation as well.

## 1.5 Contribution of the Thesis

The contribution of the thesis can be summarized as follows,

1. A simple SVPWM algorithm is proposed for multilevel inverters in this thesis. The proposed algorithm is independent of the topology of the inverter. It is based on conventional Cartesian Coordinate system and does not require coordinate transformation. It uses conventional two-level SVPWM for the on-time calculation in any triangle. To simplify the SVPWM implementation every triangle is given a unique identity called as 'triangle number $\Delta_j$'. The proposed algorithm takes the same number of computations to determine the sector number, triangle number and calculation of on-times. A simple mapping process is proposed to optimize the switching sequences. This mapping process is general in nature and can be used to solve complex problems such as common mode voltage (section 1.3.1) and asynchronous PWM harmonics (section 1.3.2). The algorithm is explained for a 3-level inverter and extended further for 5-level inverter to show that the number of steps and computations are the same as in 3-level. Then, it is generalized for any $n$-level

inverter. The proposed algorithm can be easily implemented using a commercially available motion control DSP or micro-controller which normally supports only two-level modulation. The main advantage of the proposed scheme over earlier schemes is that it can be used with an existing torque or speed control scheme implemented with two-level geometry. Since such schemes provide voltage reference in $\alpha$-$\beta$ coordinates, the proposed scheme uses most of the two-level calculation and adapts to any $n$-level inverter. The experimental results are shown for 3-level NPC inverter and 5-level cascaded H-bridge inverter.

2. An algorithm to operate a multilevel inverter in overmodulation range is proposed and a simple method to calculate on-times is given. The determination of triangle number is the same as described for the linear range. The proposed algorithm takes the same number of computation to determine the sector number, triangle number and calculation of on-times. Any of the two-level overmodulation algorithm can be easily adapted to the proposed overmodulation algorithm for multilevel inverters. The mapping process described for the linear range is extended for overmodulation range. The proposed algorithm is explained for a 5-level inverter. Then, it is generalized for any $n$-level inverter. The experimental results are shown for 3-level NPC inverter, 5-level and 7-level cascaded H-bridge inverter.

3. The phenomenon of common mode voltage generation, their cause and effects are elaborated. The problems in existing common mode voltage reduction

schemes for multilevel inverters have been brought out. A simple space vector PWM based scheme to reduce common mode voltage for cascaded inverters is proposed. In the proposed scheme, in every triangle only three switching states are used to form a switching sequence. This scheme can increase the voltage range of operation by about 17% and can produce lower THD than the previously proposed schemes. The scheme is explained with the help of a 5-level inverter. The implementation of the scheme is explained. Finally it is extended for a $n$-level inverter. The experimental results are shown for a 5-level cascaded inverter and a 3-phase induction motor. The reduction in common mode voltage and common mode currents are shown.

4. A scheme for close loop flux control of a grid connected multilevel inverter is proposed. The proposed close loop scheme is based on synchronous SVPWM. The mitigation of asynchronous PWM harmonics is shown. Synchronous SVPWM for multilevel inverter is implemented using flux error [122]. The flux error is the difference of predicted flux and estimated flux [122]. Due to the use of predicted flux, there is no delay in compensating flux error. The principle of operation, and its implementation for cascaded H-bridge inverter is clearly explained with necessary details and supported with experimental results. The flux error is significantly large in the dynamic condition. A fast dynamic performance is ensured by applying the maximum possible DC-link voltage during the dynamic condition. It is explained analytically and experimentally that the volt-sec balance is maintained even in dynamic condition.

In the proposed scheme, bus-clamping technique is applied for synchronous SVPWM of multilevel inverter. The synchronous SVPWM is applied for 3-level NPC inverter in [79] but it does not include bus-clamping. Whereas, the bus clamping in [116] is proposed for a 3-level inverter. It can not be easily extended to higher levels. These problems are addressed in this thesis. In the proposed close loop scheme, for the given flux error, the sector $S_i$, triangle $\Delta_j$ and on-times are calculated on-line in every sampling period. Hence, their pre-storage is not required. The switching sequence is mapped into a simple lookup table with respect to $S_i$ and $\Delta_j$. Hence, the switching sequence can be retrieved from this table using $S_i$ and $\Delta_j$. Due to the simple structure of the scheme, it can be easily implemented on a commercial DSP.

5. A scheme to operate a 3-level neutral point clamped inverter at high modulation index inclusive of overmodulation range is proposed. The proposed scheme maintains neutral point balance within the permissible limit at high modulation index and other unfavorable conditions. The neutral point fluctuation is within the permissible limit in overmodulation range as well. Hence, large capacitors are not required for the DC-link. Neutral point voltage fluctuation is the only parameter required as feedback to obtain good overall performance, no other input is required. This is advantageous as many other schemes need phase currents and load power factor to obtain neutral point balancing. The volt-secs balance is maintained throughout the scheme. The scheme is computationally simple so can be easily implemented.

## 1.6 Organization of the Thesis

The remaining thesis is organized as follows

- In chapter 2, a space vector PWM algorithm for the multilevel inverters is proposed based on two-level space vector PWM.
- Chapter 3 proposes space vector PWM algorithm for operation in overmodulation range for multilevel inverters.
- Chapter 4 proposes a scheme for common mode voltage reduction for the multilevel inverters.
- Chapter 5 proposes a synchronous space vector PWM based close loop flux control scheme for a grid connected cascaded multilevel inverter.
- Chapter 6 proposes a scheme to solve the neutral point balancing problem for the 3-level NPC inverter.
- Chapter 7 describes the software platform and hardware setup for the experiments in the thesis.
- Chapter 8 summarizes the salient features of the work done in this thesis and explains some future work.

# Chapter 2

# Space Vector PWM Algorithm for Multilevel Inverters based on Two-level Space Vector PWM

Implementation of space vector modulation for multilevel inverters is complex and computationally intensive due to difficulty in determining the location of reference vector, calculation of on-times and determination of switching states. This chapter proposes a simple space vector PWM algorithm for a multilevel inverter based on standard two-level space vector PWM.

## 2.1 Introduction

In section 1.3.4, problems in implementing SVPWM for multilevel inverters were described and section 1.4.1 reviewed the literature on related works. This

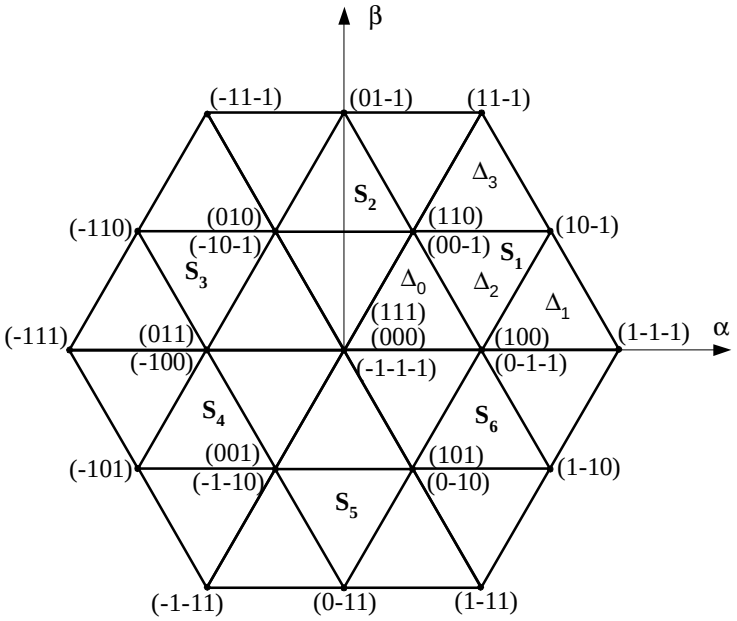



Figure 2.1: Space Vector Diagram of a 3-level Inverter

chapter proposes a simple space vector PWM algorithm for a multilevel inverter. The algorithm is based on standard two-level SVPWM, and can be implemented for any level using one counter. Some researchers [90]-[92] have proposed multilevel SVPWM using two-level concept. However, there are a few drawbacks in these methods as described in 1.4.1 of chapter 1 which are alleviated in the proposed scheme. This chapter presents a significantly different approach from prior arts and provides a general solution.

The salient features of the proposed algorithm are as follows,

• On-time calculation is simple due to use of two-level space vector PWM. On-time calculation equations do not change with the position of reference vector like the traditional approach in [87], so there is no need for any look-up tables.

• In the space vector diagram of a $n$-level inverter, the triangle where the reference vector is located, is identified as integer $\triangle_j$ using a simple algebraic expression. Let us call $\triangle_j$ as triangle number, it implies the $j^{th}$ triangle among $(n-1)^2$ triangles in a sector. Any switching sequence can be executed with respect to triangle $\triangle_j$, leading to a simplicity and flexibility of optimizing the sequence.

• The proposed scheme can be used for any $n$-level ($n \geq 3$) inverter without any significant increase in computations.

• It is based on conventional cartesian coordinate system, and hence can be easily implemented with existing outer control loops for speed or torque.

• The proposed method can be easily implemented using a commercially available motion control DSP or micro-controller which normally supports only two-level modulation.

Since the proposed multilevel space vector modulation method uses the basic two-level modulation to calculate the on-times, computation process for $n$-level inverter becomes simpler and easier. The main advantage of the proposed methodology is that it uses a simple mapping process to achieve the multilevel space vector modulation. The proposed algorithm in this chapter is explained using 3-level and 5-level inverters. The algorithm is then extended to a $n$-level inverter to generalize. The effectiveness of the algorithm has been verified by experiments, on a 3-level NPC inverter and 5-level cascaded H-Bridge inverter.

## 2.2 Proposed Algorithm of On-time Calculation

The basic idea of space vector modulation is to compensate the required volt-seconds using discrete switching states and their on-times. Traditionally, in order to determine the on-times for a triangle of a $n$-level inverter three simultaneous equations are solved. However, a classical two-level space vector geometry can be used for on-time calculation for a multilevel SVPWM. Let us first understand the on-time calculation in two-level SVPWM.

### 2.2.1 The On-time Calculation for two-level SVPWM

Fig. 2.2 shows the space vector diagram of a two-level inverter. Every sector is an equilateral triangle of unity side and $h(=\sqrt{3}/2)$ is the height of a sector. On-time calculation for any of the six sectors $S_i$, $i = 1, 2, .., 6$ is same, so let us consider the operation in sector 1.

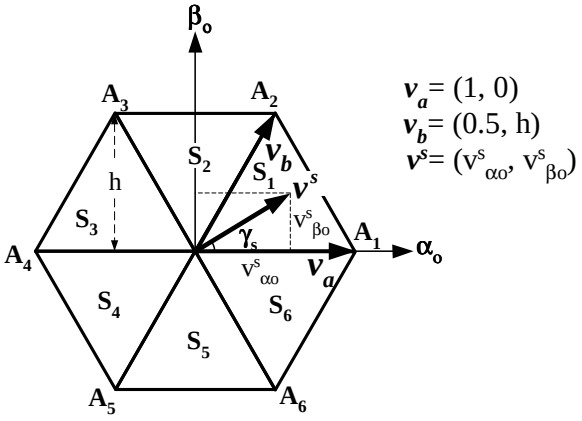



Figure 2.2: Space Vector Diagram for two-level inverter

On-time calculation is based on the location of the reference vector within a sector. For the sector 1 in Fig. 2.2, the volt-second balance is given by,

$$v^s T_s = v_a t_a + v_b t_b \tag{2.1}$$

Time balance is given by,

$$T_s = t_a + t_b + t_o \tag{2.2}$$

Resolving (2.1) along $\alpha_o$-$\beta_o$ axis, we obtain,

$$v^s_{\alpha o} T_s = t_a + 0.5 t_b \tag{2.3}$$

$$v^s_{\beta o} T_s = h t_b \tag{2.4}$$

Solving (2.2)-(2.4), we obtain (2.5)-(2.7) for the calculation of the on-times.

$$t_a = T_s[v^s_{\alpha o} - \frac{v^s_{\beta o}}{2h}] \tag{2.5}$$

$$t_b = T_s[\frac{v^s_{\beta o}}{h}] \tag{2.6}$$

$$t_o = T_s - t_a - t_b \tag{2.7}$$

### 2.2.2 The On-time Calculation for 3-level SVPWM

Fig. 2.3 illustrates, the proposed method of on-times calculation for a 3-level inverter. Each sector of a 3-level inverter can be split into 4 triangles $\triangle_j$, where $j = 0, 1, 2, 3$. To simplify on-time calculation, these triangles can be categorized into two types; type 1 and type 2. The triangle of type 1 has its base side at the bottom, as shown in Fig. 2.3(b). Triangles $\triangle_0$, $\triangle_1$ and $\triangle_3$ are of type 1. The

triangle of type 2 has its base side at the top, as shown in Fig. 2.3(d). Triangle $\triangle_2$ is of type 2.

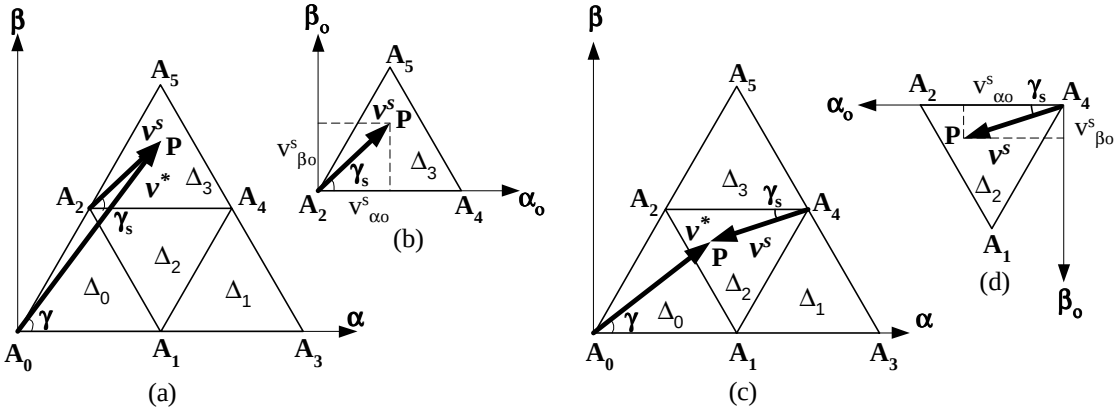



Figure 2.3: Space Vector Diagram - Virtual two-level from 3-level

Let us assume that the side of a triangle is 1(unity) and $h(=\sqrt{3}/2)$ is the height of the triangle. In Fig. 2.3(a), $\boldsymbol{v^*}$ is the reference vector of magnitude $|\boldsymbol{v^*}|$ at an angle of $\gamma$ with the $\alpha$ axis. Let us define a small vector $\boldsymbol{v^s}$, which describes the same point in shifted system ($\alpha_o$, $\beta_o$), see Fig. 2.3(b) and (d). It makes $\gamma_s$ angle with the $\alpha_o$ axis. The volt-seconds required to approximate the small vector $\boldsymbol{v^s}$ in the shifted system ($\alpha_o$, $\beta_o$) should be equal to those required for the actual vector $\boldsymbol{v^*}$ in the original system ($\alpha$, $\beta$). Hence, the on-times for any reference vector can be obtained by finding the on-times of the respective small vector $\boldsymbol{v^s}$.

To achieve the volt-seconds for any reference vector in a sector of a 3-level inverter, we have to identify the triangle in which the required reference is located and then find ($v^s_{\alpha o}$, $v^s_{\beta o}$). The on-time calculations can be performed using the geometry shown in Fig. 2.3(b) or (d), which would result in the same on-time equations as those for a classical two-level SVPWM (2.5)→(2.7).

A triangle of type 1 is similar to a sector 1 of a virtual two-level inverter. For example; In Fig. 2.3(a), triangle $\triangle_3$ can be assumed similar to sector 1 of a two-level inverter if $A_2$ is taken as zero vector of the virtual two-level sector as shown in Fig. 2.3(b). Vector $A_2P$ defines the small vector $\boldsymbol{v^s}(v^s_{\alpha o}, v^s_{\beta o})$. On-times $t_a$ ($t_{A_4}$), $t_b$ ($t_{A_5}$) and $t_o$ ($t_{A_2}$) are calculated by using (2.5)→(2.7), where the multiplication operations are required only for (2.5) and (2.6).

A triangle of type 2 is similar to a sector 4 of a virtual two-level inverter. For example; In Fig. 2.3(c), triangle $\triangle_2$ can be considered similar to sector 4 of a two-level inverter if $A_4$ is assumed to be zero vector see Fig. 2.3(d). In this example, $A_4P$ represents small vector $\boldsymbol{v^s}(v^s_{\alpha o}, v^s_{\beta o})$. On-times $t_a$ ($t_{A_2}$), $t_b$ ($t_{A_1}$) and $t_o$ ($t_{A_4}$) are calculated by using (2.5)→(2.7).

### 2.2.3 The On-time Calculation for 5-level SVPWM

Fig. 2.4(a) illustrates the proposed method of on-times calculation for a 5-level inverter. Each sector can be split into 16 triangles $\triangle_j$, where $j$=0→15. Any triangle, in the geometry in Fig. 2.4(a) can be assumed to be equivalent to a sector of a virtual two-level inverter. For example; if $A_7$ is taken as zero vector then triangle $\triangle_{11}$ can be assumed similar to sector 1 ($S_1$) of a two-level inverter, as per Fig. 2.2 and Fig. 2.4(b). The on-time calculations can be performed by using the geometry shown in Fig. 2.4(b), which would result in the same on-time equations as those for a classical two-level SVPWM (2.5)→(2.7).

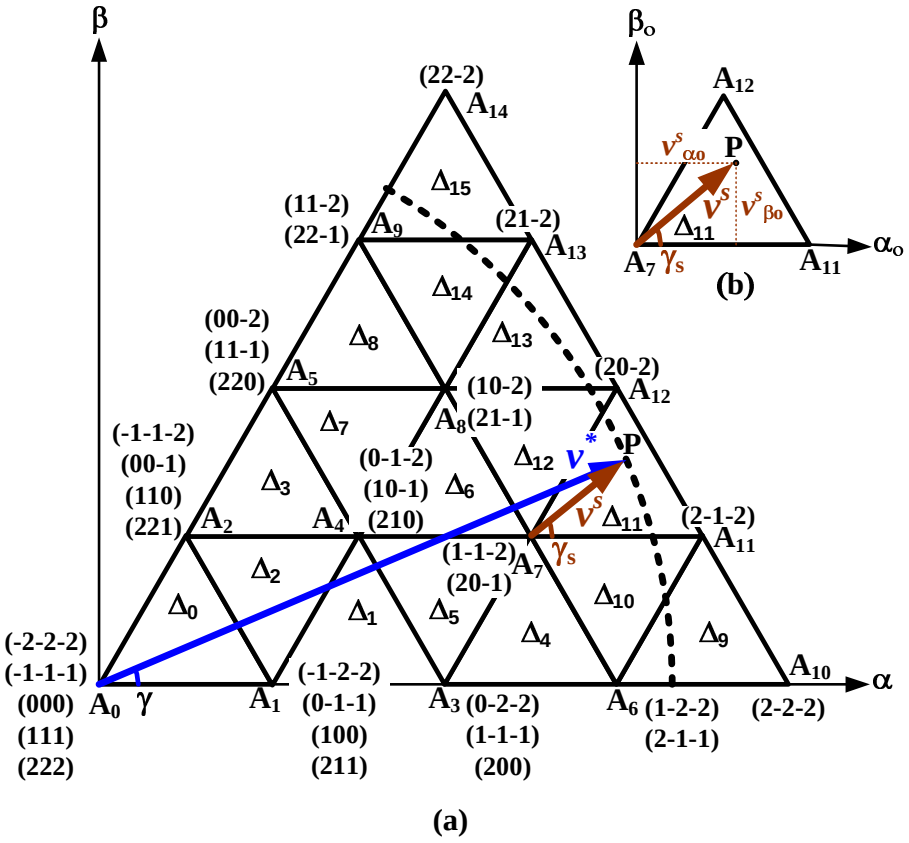



Figure 2.4: Space Vector Diagram - Virtual two-level from 5-level

Since the triangles within any sector of a $n$-level inverter are analogous to a sector of two level inverter, the idea can be extended to any level. Thus, multilevel on-time calculation problem is converted to a two-level on-time calculation problem.

## 2.3 Simplified Structure of the Proposed Scheme

Block diagram in Fig. 2.5 gives an overview of the proposed method. It consists of two basic units, namely processing unit and mapping unit respectively. Processing unit consists of a base scheme or algorithm and a counter.

The processing unit is basically a DSP or micro-controller. The base scheme in processing unit does three main tasks: (a) determination of the sector number $S_i$, (b) determination of small vector $\boldsymbol{v^s}$ coordinates ($v^s_{\alpha o}$, $v^s_{\beta o}$) and triangle $\triangle_j$, (c) On-time $t_o$, $t_a$ and $t_b$ calculation for the triangle using small vector $\boldsymbol{v^s}$ coordinates ($v^s_{\alpha o}$, $v^s_{\beta o}$) and two-level space vector PWM equations (2.5)→(2.7)

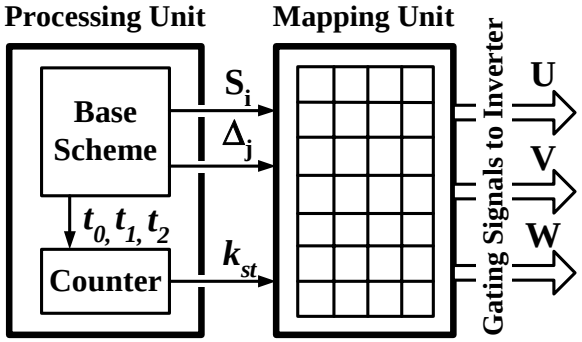



Figure 2.5: Block Diagram of the Proposed Scheme

The mapping unit uses memory. It fires the pre-stored switching sequence for the 3-phase inverter based on sector $S_i$, triangle $\triangle_j$ for the on-times obtained from the processing unit. For a multilevel inverter, a vertex of any triangle can have multiple redundancies (two or more possible switching states). For a triangle, a switching sequence is formed using a combination of the most suitable switching states from all possible switching states at the vertices. The resulting switching sequence is mapped with respect to the triangle and sector number. The switching sequence is then fired for the on-times obtained from the processing unit. In the proposed method, a triangle is considered as the basic unit, and the mapping takes care of the redundancies. Hence, any suitable vertex can be chosen as zero vector. While doing so redundancies at other vertices are also made use of. The sequence,

in which the on-times $t_a$, $t_b$ and $t_o$ have to be used, will be dependent on the order of selecting the switching states. Thus the proposed algorithm is able to make use of any redundancies for any vertex of the triangle. As opposed to this, if the two-level hexagon is used to mimic the two-level modulation, only two redundancies of zero vector are considered. Hence for higher level, where middle vectors have higher redundancies, such approach will not be able to make use of all redundancies.

Generally, a continuous PWM sequence has four stages, and a discontinuous PWM sequences have three stages [123]. The counter in processing unit generates stage number $k_{st}$ using the on-times $t_a$, $t_b$ and $t_o$. Here, $k_{st}$=0→3 for continuous SVM and $k_{st}$=0→2 for discontinuous SVM.

First, let us understand the implementation of this scheme using a 3-level and 5-level space vector diagram, then it is generalized for a $n$-level inverter. It will be thus demonstrated that unlike earlier methods the proposed scheme is easily extendable to any $n$-level inverter.

## 2.4 Implementation of the Proposed Scheme

### 2.4.1 Processing Unit

It is mentioned before that the main role of the processing unit is to determine sector, triangle, and calculate on-times. The determination of these parameters is explained using the space vector diagram of 3-level and 5-level inverter.

#### 2.4.1.1 Determination of Sector

Irrespective of the level $n$, for any given location of the reference vector, the sector of operation $S_i$ and its angle $\gamma$ within the sector are determined as,

$$S_i = \text{int}(\frac{\theta}{60}) + 1 \tag{2.8}$$

$$\gamma = rem(\frac{\theta}{60}) \tag{2.9}$$

where $\theta$ is the angle of the reference vector with respect to $\alpha$ axis, $int$ and $rem$ represent standard functions integer and remainder respectively.

#### 2.4.1.2 Determination of Small Vector $\boldsymbol{v^s}$ and Triangle Number $\triangle_j$

The determination of small vector $\boldsymbol{v^s}$ is required to determine the triangle number and to calculate the on-times. There are $(n\text{-}1)^2$ triangles in a sector of a $n$-level space vector diagram. The determination of small vector $\boldsymbol{v^s}$ is dependent on level $n$. A simple algorithm is described in this section which determines the small vector $\boldsymbol{v^s}$ for any $n$ using the same number of computations. Let us first understand this algorithm for a 3-level and 5-level space vector diagram.

Referring to the space vector diagram of a 3-level in Fig.2.3, the tip P of the reference vector $\boldsymbol{v^*}$ can be located in any of the four triangles; $\triangle_0$, $\triangle_1$, $\triangle_2$ or $\triangle_3$. As per section 2.2, a triangle in Fig.2.3 can be treated as a sector of a two-level inverter. So the first objective here is to identify the triangle of small vector

The search of the triangle of the small vector (or point P) can be narrowed

down by using two integers $k_1$ and $k_2$. They are defined by the coordinate $(v_\alpha, v_\beta)$ of point P as

$$k_1 = \text{int}(v_\alpha + v_\beta/\sqrt{3}),\ k_2 = \text{int}(v_\beta/h) \tag{2.10}$$

In (2.10), $k_1$ represents the part of the sector between the two lines joining the vertices, separated by distance $h$ and inclined at $120^o$ with respect to $\alpha$ axis, see Fig. 2.6. $k_1$=0 signifies that the point P is below line $A_1A_2$. $k_1$=1 signifies that point P is between line $A_1A_2$ and line $A_3A_5$. $k_2$ represents the part of the sector between the two lines joining the vertices, separated by distance $h$ and parallel to $\alpha$ axis. $k_2$=0 signifies that the point P is between line $A_0A_3$ and line $A_2A_4$. $k_2$=1 signifies that the point P is above line $A_2A_4$. Geometrically, the values of $k_1$ and $k_2$, is intersection of two rectangular regions which is either a triangle or rhombus. In other words the point P lies in (a) triangle $\triangle_0$ if $k_1$=0 and $k_2$=0, (b) rhombus $A_1A_3A_4A_2$ (shaded) if $k_1$=1 and $k_2$=0, (c) triangle $\triangle_3$ if $k_1$=1 and $k_2$=1. The same analogy can be used for any level.

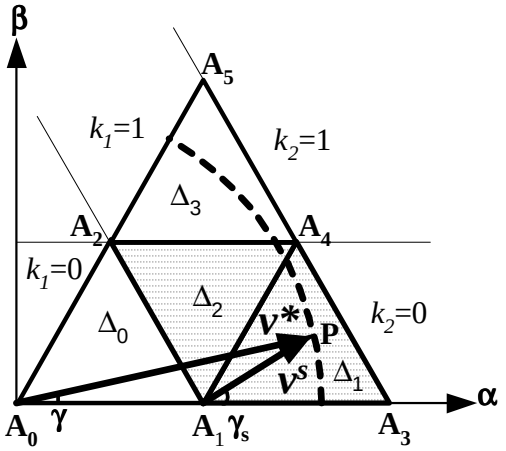



Figure 2.6: Space Vector Diagram - Sector 1 of a 3-level Inverter

In Fig. 2.6, the reference vector is located in rhombus $A_1A_3A_4A_2$. This rhombus is made of two triangles $\triangle_1$ and $\triangle_2$. The point P can be located in any of the two. Let ($v_{\alpha i}$, $v_{\beta i}$) be the coordinates of the point P with respect to the point $A_1$, obtained as,

$$v_{\alpha i} = v_\alpha - k_1 + 0.5k_2,\ v_{\beta i} = v_\beta - k_2 h \tag{2.11}$$

The slope of $\overrightarrow{A_1P}$ is $v_{\beta i}/v_{\alpha i}$ and the slope of diagonal $A_1A_4$ is $\sqrt{3}$. The triangle where point P is located can be determined by comparing the slope of $\overrightarrow{A_1P}$ with the slope of $A_1A_4$. Slope comparison is done by evaluating the inequality $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$, leading to following two results on small vector $\boldsymbol{v^s}$ and triangle number $\triangle_j$.

1. $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$: The point P is within the triangle $\triangle_1$ and the small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_1P}$ ($v_{\alpha i}$, $v_{\beta i}$). The triangle number $\triangle_j$ is obtained as

$$\Delta_j = k_1^2 + 2k_2 \tag{2.12}$$

2. $v_{\beta i} > \sqrt{3} v_{\alpha i}$: The point P is within the triangle $\triangle_2$ and the small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_4P}$ (0.5-$v_{\alpha i}$, h-$v_{\beta i}$). The triangle number $\triangle_j$ is obtained as

$$\Delta_j = k_1^2 + 2k_2 + 1 \tag{2.13}$$

These two results can be generalized to triangles of type 1 and type 2 respectively. For example; When the point P is in triangle $\triangle_3$, the inequality $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$ will be true because triangle $\triangle_3$ is a triangle of type 1. The small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_2P}$ ($v_{\alpha i}$, $v_{\beta i}$). Thus, we determine the small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$), for any given reference vector.

In (2.12) and (2.13), '△' symbolizes a triangle and 'j' the triangle number. Hence, $\triangle_j$ is an integer and signifies $j^{th}$ triangle in the sector. The triangle in a sector is identified as an integer $\triangle_j$ using a simple algebraic expression (2.12) or (2.13). It is a byproduct of the small vector determination process, so no other computation is required. It greatly simplifies the PWM process as switching states can be easily mapped with respect to the triangle number $\triangle_j$. The triangle number $\triangle_j$ is formulated to provide a simple way of arranging the triangles, leading to ease of identification and extension to any level.

The determination of small vector ($v^s_{\alpha o}$, $v^s_{\beta o}$) explained for 3-level inverter can be extended to any other level. Let us see it for 5-level inverter. Referring to the space vector diagram of 5-level inverter in Fig. 2.7, the tip P of the reference vector $\boldsymbol{v^*}$ can be located in any of the 16 triangles; $\triangle_0$-$\triangle_{15}$. As mentioned before, a triangle in Fig. 2.7 can be treated as a sector of a two-level inverter.

The integer parameters $k_1$ and $k_2$ are defined earlier in (2.10). In Fig. 2.7, $k_1$=0 signifies that the point P is below $A_1A_2$, $k_1$=1 signifies that point P is between $A_1A_2$ and $A_3A_5$, $k_1$=2 signifies that point P is between $A_3A_5$ and $A_6A_9$ and so on. In Fig. 2.7, $k_2$=0 signifies that the point P is between $OA_{10}$ and $A_2A_{11}$, $k_2$=1 signifies that the point P is between $A_2A_{11}$ and $A_5A_{12}$ and so on.

For the reference vector in Fig. 2.7, $k_1$=2 and $k_2$=1 i.e. the intersection is rhombus $A_4A_7A_8A_5$ where the tip P of reference vector is situated. This rhombus is made of two triangles $\triangle_6$ and $\triangle_7$. Let ($v_{\alpha i}$, $v_{\beta i}$) be the coordinates of the point

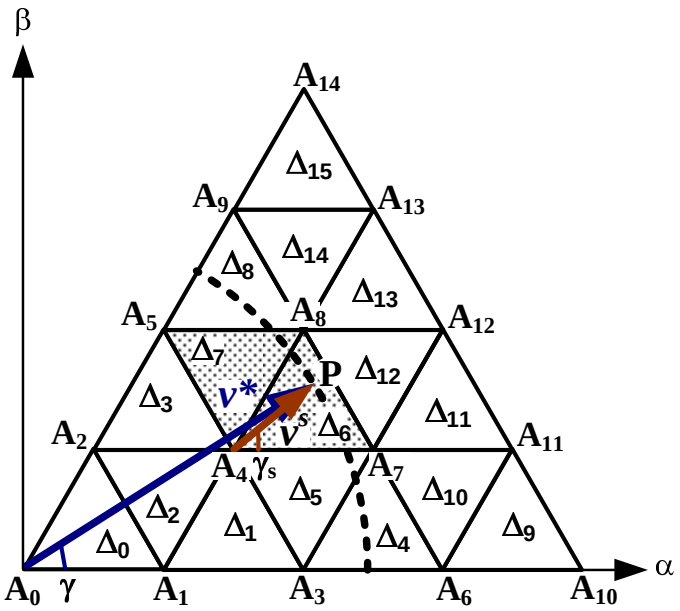



Figure 2.7: Space Vector Diagram - Sector 1 of a 5-level Inverter

P with respect to the point $A_4$, obtained using (2.11).

The slope of $\overrightarrow{A_4P}$ is $v_{\beta i}/v_{\alpha i}$ and the slope of diagonal $\overrightarrow{A_4A_8}$ is $\sqrt{3}$. The triangle where point P is located can be determined by comparing the slope of $\overrightarrow{A_4P}$ with $\overrightarrow{A_4A_8}$. As discussed before, the slope comparison is done by evaluating the inequality $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$.

The same two results described in (2.12) and (2.13) are equally applicable here also. If $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$ is true, then the point P is within the triangle $\triangle_6$, otherwise it is within the triangle $\triangle_7$. If point P is within triangle $\triangle_6$, the small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_4P}$ ($v_{\alpha i}$, $v_{\beta i}$) otherwise point P is within triangle $\triangle_7$, and small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_8P}$ (0.5-$v_{\alpha i}$, h-$v_{\beta i}$). Another example is; the period during which the point P is in triangle $\triangle_8$, inequality $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$ will

be true because triangle $\triangle_8$ is a triangle of type 1. The small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) is represented by $\overrightarrow{A_5P}$ ($v_{\alpha i}$, $v_{\beta i}$). Thus, we can determine the small vector $\boldsymbol{v^s}$ ($v^s_{\alpha o}$, $v^s_{\beta o}$) for any given reference vector.

#### 2.4.1.3 Calculation of On-times

Having determined the coordinates ($v^s_{\alpha o}$, $v^s_{\beta o}$) of small vector $\boldsymbol{v^s}$, the on-times calculation for a multilevel inverter is done by using two-level on-time calculation equations (2.5)→(2.7). Since one of the vertex is treated as zero vector, multiplication is required only for (2.5) and (2.6).

The flowchart in Fig. 2.8 summarizes the proposed algorithm of determination of sector number $S_i$, triangle number $\triangle_j$ and on-times calculation for linear modulation range of multilevel inverter.

### 2.4.2 Mapping Unit

The job of mapping unit is to generate gating signals using the sector $S_i$, triangle $\triangle_j$, on-times $t_a$, $t_b$ and $t_o$. These parameters are obtained from the processing unit for every switching period. Mapping unit uses memory. A switching state is defined as $[s_u, s_v, s_w]$ where $s_u$, $s_v$ and $s_w$ can take a value -1, 0 or 1. As shown in Fig. 2.1, there are 27 switching states for 3-level, inclusive of 19 distinct and 8 redundant states. These states are stored in a table. Depending on the position of reference vector, normally four of them are used by the switching sequence in

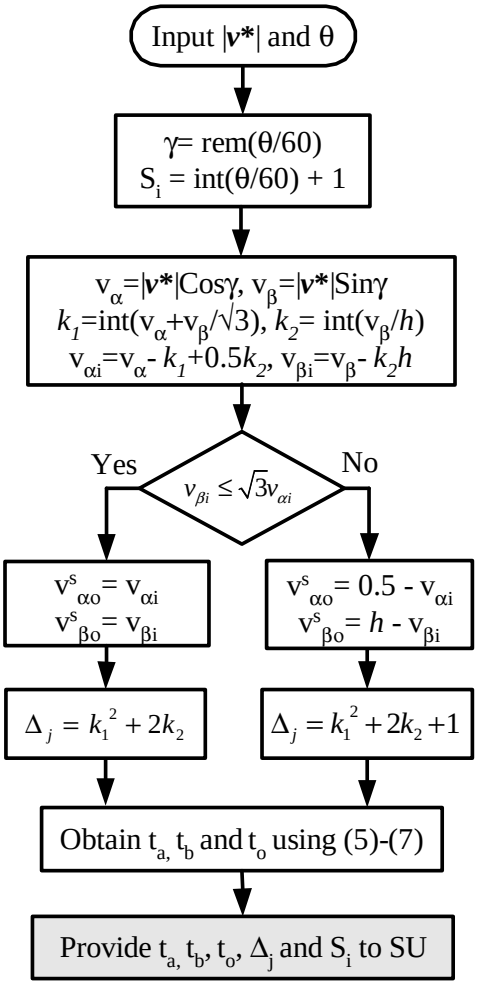



Figure 2.8: Flow chart for the proposed scheme

every switching period.

A switching sequence for a triangle is made of the switching states, corresponding to the vertices of the triangle. For example, Table 2.1 shows the switching sequence for the triangle $\triangle_3$ of the sector 1 of a 3-level inverter using minimum commutation criteria. Here, $t_{o+}$ and $t_{o-}$ play an important role in DC link balancing [91] and $t_{o+} + t_{o-} = t_o$. Jae et al. [91] adjust the on-times $t_{o+}$ and $t_{o-}$ to obtain the neutral point balance. This sequence is applied, for the time duration of

$2T_s$, when the reference vector $\boldsymbol{v}^*$ is in triangle $\triangle_3$. Similarly, any other switching sequence for any other triangle can be applied due to the generality of the unit.

| $\Delta_j$ | $\Delta_2$ | | | | $\Delta_3$ | | | | $\Delta_4$ | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| d.r. | $d_{A1-}$ | $d_{A3}$ | $d_{A4}$ | $d_{A1+}$ | $d_{A1-}$ | $d_{A2}$ | $d_{A4}$ | $d_{A1+}$ | $d_{A2-}$ | $d_{A4}$ | $d_{A5}$ | $d_{A2+}$ |
| $s_u$ | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| $s_v$ | -1 | -1 | 0 | 0 | -1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| $s_w$ | -1 | -1 | -1 | 0 | -1 | -1 | -1 | 0 | -1 | -1 | -1 | 0 |

Table 2.1: Switching Sequence for $\triangle_2, \triangle_3$ and $\triangle_4$ of sector 1 of 3-level Inverter

A switching sequence is also dependent on the switching scheme used e.g. Common-mode Voltage Elimination [90] and Flux Modulation [92]. Hence, there could be many switching sequences for any triangle. However, only one such sequence can be implemented at a time. The switching sequence can be treated as a function of the sector and triangle of the reference vector. For a 3-level inverter, the memory required for the storage of switching states is approximately 27B.

### 2.4.3 Experimental results

The proposed scheme can be used for both NPC and cascaded H-bridge topologies of multilevel inverter, as for a given level both have same space vector diagram. For both of them, the computations required by the processing unit are same. However, for a given level the actual gating signals are different for the two topologies. They are generated by simple multiplexing operation without need for additional hardware.

For implementation the algorithm has been developed on dSPACE DS1104. DS1104 was used due to its availability but no floating point operations are used. Thus, the algorithm can be implemented on a fixed point DSP as well. A laboratory prototype of 3-level NPC inverter and 5-level cascaded H-bridge inverter is used.

#### 2.4.3.1 Experimental Results for 3-level NPC Inverter

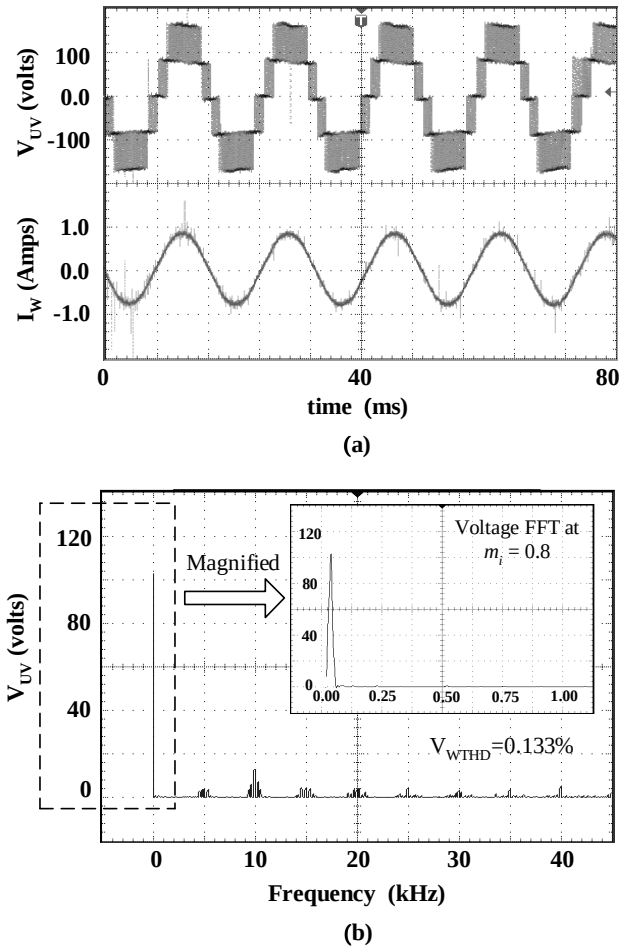



Figure 2.9: Experimental results for 3-level NPC inverter (a) Line voltage and current waveforms (b) FFT of the line voltage

Fig. 2.9(a) shows line voltage and current waveforms with the proposed method. The DC link voltage is 170 V, modulation index $m_i$=0.8, PWM frequency 5 kHz,

fundamental frequency 50 Hz, load inductance per phase 0.47 H and load resistance per phase 48.4 Ω. Neutral point balancing is obtained using [91] by adjusting the on-times $t_{o+}$ and $t_{o-}$ as described before.

Fig. 2.9(b) shows the FFT of line voltage $V_{VW}$ for $0<f_s\leq 45$ kHz inclusive of a magnified FFT view in the inset for $0<f_s\leq 1$ kHz, to better show the low order harmonics. The $x$-scale of inset is frequency in kHz. The fundamental component of line voltage increases with modulation index.

Weighted harmonic distortion $V_{WTHD}$ is used here, which represents harmonic losses. It is equivalent to $I_{THD}$. $V_{WTHD}$ (%) is obtained [37] as

$$V_{WTHD} = \frac{\sqrt{\sum_{n\neq 1}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} * 100 \tag{2.14}$$

where $V_1$ and $V_n$ are the rms values of the fundamental and the $n^{th}$ harmonic components of the line voltage waveform.

There are other forms of $V_{WTHD}$ as in [124], [125], [126]. Using 2.14, for Fig. 2.9(b) the weighted harmonic distortion $V_{WTHD}$ obtained is 0.133 %.

#### 2.4.3.2 Experimental Results for 5-level Cascaded H-Bridge Inverter

Fig. 2.10 shows experimental waveforms $V_{UV}$ and $I_W$ with the proposed method. The switching states are selected based on minimum commutation criteria. The

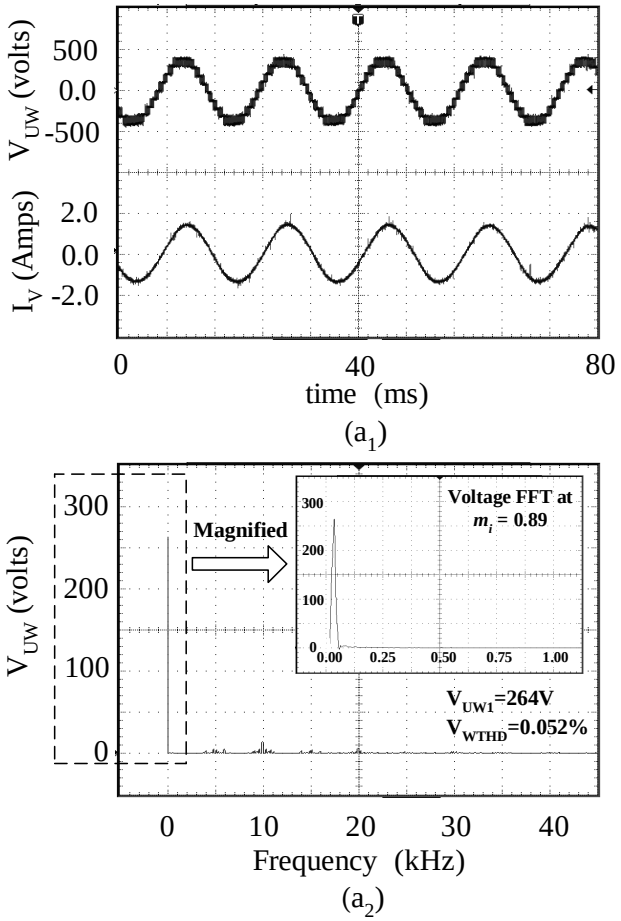



Figure 2.10: Experimental results for a 5-level inverter (a1) Voltage $V_{UW}$ and current $I_V$ at $m_i$=0.89 (a2) FFT of voltage $V_{UW}$ at $m_i$=0.89

test was performed on a 0.75 kW induction motor at $m_i$=0.8 and $V_{dc(HB)}$=100V, fundamental frequency $f = 50$Hz and sampling frequency $f_s = 5$kHz. Here, $V_{dc(HB)}$ is voltage applied on each H-bridge module per Fig. 1.8.

## 2.5 Extension of Scheme for a $n$-level Inverter

The proposed scheme is explained using 3-level and 5-level space vector diagram, it illustrated the simplicity of the approach. The proposed scheme can be

easily applied to a $n$-level inverter as well. Similar to 3-level and 5-level, we require sector number, triangle number, on-times and relevant switching states to implement the scheme for a $n$-level inverter. To understand this implementation for a $n$-level inverter, let us consider same two units as explained before i.e. processing unit and Mapping unit.

### 2.5.1 Processing Unit for $n$-level

For a given $\boldsymbol{v}^*$, the processing unit calculates sector number, triangle number and on-times. They are provided to mapping unit in every switching period. The flowchart in Fig. 2.8 describes the job of a processing unit. In this flowchart, for a given $\boldsymbol{v}^*$, all the arithmetic and logical operations required by main routine are independent of level $n$. Therefore, the number of computations remain same for any $n$-level SVPWM.

Table 2.2 shows the steps required to obtain sector number $\mathrm{S}_i$, triangle number $\triangle_j$ and on-times at a given modulation index $m_i$=0.87 and angle $\theta$=78$^o$ for a 3-level, 5-level and 7-level inverter at PWM frequency $f_s$=5 kHz.

It can be seen from table 2.2 that same number of steps are required for all the three cases. For a given $|\boldsymbol{v}^*|$ and $\theta$, the algorithm requires nearly 10 multiplications, 10 additions/subtractions and 1 branch instructions to calculate sector number, triangle number and on-times. They remain same for any level. The following points are concluded for the processing unit of a $n$-level inverter,

| Steps | 3-level | 5-level | 7-level |
|---|---|---|---|
| $\lvert\boldsymbol{v}^*\rvert$ | 1.91 | 3.82 | 5.73 |
| $S_i$ | 2 | 2 | 2 |
| $\gamma$ | $18^o$ | $18^o$ | $18^o$ |
| $(v_\alpha, v_\beta)$ | (1.5788, 0.5130) | (3.1575, 1.0259) | (4.7363, 1.5389) |
| $k_1, k_2$ | 1, 0 | 3, 1 | 5, 1 |
| $(v_{\alpha i}, v_{\beta i})$ | (0.5788, 0.5130) | (0.6575, 0.1599) | (0.2363, 0.6729) |
| $v_{\beta i} \leq \sqrt{3} v_{\alpha i}$ ? | Yes | Yes | No |
| $(v^s_{\alpha o}, v^s_{\beta o})$ | (0.5788, 0.5130) | (0.6575, 0.1599) | (0.2637, 0.1931) |
| $\triangle_j$ | 1 | 11 | 28 |
| $t_a$ | 28.26 $\mu$s | 56.52 $\mu$s | 15.22 $\mu$s |
| $t_b$ | 59.24 $\mu$s | 18.47 $\mu$s | 22.30 $\mu$s |
| $t_o$ | 12.50 $\mu$s | 25.01 $\mu$s | 62.48 $\mu$s |

Table 2.2: Steps Required for SVPWM of 3-level, 5-level and 7-level

• In the proposed scheme, the computations do not change with the level. The processing unit remains same for any level.

• On-time calculation equations do not change with triangle like the traditional approach as in [87], it saves storage space.

• The computations required by the processing unit are significantly lesser than the methods similar to proposed in [87] and comparatively lesser than the methods similar to proposed in [88].

• Triangle number $\triangle_j$ is easily identified as an integer using (2.12) or (2.13) for any level. Triangle number $\triangle_j$ leads to a flexibility and simplicity in switching sequence mapping process.

• The scheme is based on a two-level SVPWM. Therefore, an existing two-level SVPWM module can be easily adapted to multilevel inverters. It can be used with an existing torque or speed control scheme implemented with two-level geometry. This would save re-engineering cost. Commercially available motion control DSP, normally support only two-level modulation. However, the proposed architecture in Fig.2.5 can be easily implemented on it.

Apart from the above another merit of the proposed algorithm is that it can be implemented with a single counter. Some multilevel carrier PWM can be implemented using single counter. [127] uses a single counter to generate a time base for the modulation. However, in order to get phase shifted carrier and generate PWM signal an elaborate peripheral circuit has to be engineered. The complexity of the peripheral circuit and its engineering will increase with the number of levels. On the other hand [128] uses a FPGA based scheme. They argue that a conventional single counter microprocessor is almost useless for multilevel PWM as it cannot achieve double-edge modulation or phase shifting so easily. Hence they propose a FPGA based system for the implementation of carrier based scheme for 5-level cascaded H-bridge inverter. The paper describes the method for only a single phase system. One up-down counter is used for every H-bridge along with compare-match-register. Thus the scheme uses two counters for a 5-level single phase inverter. [129] proposes a very cumbersome scheme. This work developed a carrier-based PWM scheme for 5-level cascaded H-bridge inverter. As we know there will be 6 H-bridge modules for a 5-level cascaded H-bridge inverter. This

scheme uses one MiniDSP controller for every H-bridge module apart from one master DSP controller and a PC controller. The MiniDSP controller obtains the control parameter from the master controller and calculates the actual timing of the pulses to be fired and generates the gating signals. Though a single counter is used for an H-bridge, a combination of several DSPs, their synchronization and interrupt management makes this scheme very complex especially for a medium voltage drives.

On the other hand, the proposed scheme can make use of existing two-level SVPWM platform with minor modifications. Especially, when used for drives applications, one can use the existing control loops for speed, torque and current that will give the voltage space vector as the control variable. With a minor modification to the existing two-level SVPWM, the system can be easily re-engineered for any multilevel inverter. The scheme has been implemented for 3-level NPC, 5-level cascaded and 7-level cascaded inverters using the same processing unit, and can be extended to any level.

### 2.5.2 Mapping Unit for $n$-level

As level increases, the number of switching states also increase. The mapping unit can be designed to map the switching sequence for any triangle of a $n$-level inverter. As mentioned before, a switching sequence for a triangle is made of the switching states, corresponding to the vertices of the triangle.

For a $n$-level inverter, a switching state is defined as $[s_u, s_v, s_w]$, where $s_u$, $s_v$ or $s_w$ can take a value from -(n-1)/2 to (n-1)/2. There are $n^3$ switching states for a $n$-level inverter. A vertex in the space vector diagram of a $n$-level inverter can have 1 to n switching states. For example; in Fig. 2.1, there are 27 switching states in the space vector diagram of a 3-level inverter, and a vertex has 1 to 3 switching states. A simple tabulation is provided using which, the switching states associated with any vertex in the space vector diagram of a $n$-level inverter can be obtained. This is an off-line process.

The switching states associated with a vertex can be determined by using its $(\alpha, \beta)$ coordinates. Let us represent the $(\alpha, \beta)$ coordinates of a vertex as $(v_\alpha, v_\beta)$ for the determination of its switching states. To this end, five integer variables are defined as follows

$$m_1 = [v_\alpha + \frac{v_\beta}{\sqrt{3}}],\ m_2 = [n - m_1],\ m_3 = [\frac{n-1}{2}],\ m_4 = [m_1 - m_3],\ m_5 = [\frac{v_\beta}{h} - m_3] \tag{2.15}$$

where $m_1$ is vertex index, whose value depends on the location of the vertex in $\alpha$-$\beta$ plane. When subtracted from $n$, the total number of switching states $m_2$ at this vertex are obtained. -$m_3$ provides the state of phase $w$, $m_4$ provides the state of phase $u$ and $m_5$ provides the state of phase $v$.

Table 2.3 determines all the switching state(s) $[s_u, s_v, s_w]$, at a vertex $(v_\alpha, v_\beta)$ in sector 1 of a $n$-level inverter. For a three phase inverter, it is a $m_2$x3 table, where $1 \leq m_2 \leq n$.

| Switching State | $s_u$ | $s_v$ | $s_w$ |
|---|---|---|---|
| 1 | $m_4$ | $m_5$ | - $m_3$ |
| 2 | $m_4$ +1 | $m_5$ +1 | - $m_3$ +1 |
| .... | ..... | ..... | ..... |
| .... | ..... | ..... | ..... |
| $m_2$ | $m_4$ + $m_2$ -1 | $m_5$ +$m_2$ -1 | - $m_3$ +$m_2$ -1 |

Table 2.3: Switching States for a vertex of a $n$-level Inverter in sector I

| Sector | Phase U | Phase V | Phase W |
|---|---|---|---|
| $S_1$ | $s_u$ | $s_v$ | $s_w$ |
| $S_2$ | -$s_v$ | -$s_w$ | -$s_u$ |
| $S_3$ | $s_w$ | $s_u$ | $s_v$ |
| $S_4$ | -$s_u$ | -$s_v$ | -$s_w$ |
| $S_5$ | $s_v$ | $s_w$ | $s_u$ |
| $S_6$ | -$s_w$ | -$s_u$ | -$s_v$ |

Table 2.4: Switching States Mapping Between Sector 1 and Other Sectors

For example, for a 3-level inverter corresponding to vertex (0.5, $h$), the values of $m_1$, $m_2$, $m_3$, $m_4$ and $m_5$ are 1, 2, 1, 0 and 0 respectively. Therefore the switching states are [0,0,-1] and [1,1,0]. Similarly, for a 5-level inverter corresponding to vertex (0.5, $h$) the values of $m_1$, $m_2$, $m_3$, $m_4$ and $m_5$ are 1, 4, 2, -1 and -1 respectively. Therefore the switching states are [-1,-1,-2], [0,0,-1], [1,1,0] and [2,2,1].

For other sectors, the switching states are determined by mapping between the Tables 2.3 and 2.4. Tables 2.4 is of 6x3 dimension for any $n$-level inverter. Columns represent the three phases and rows represent the six sectors. For example, if in sector 1 a switching state at some particular vertex is $[1, 1, 0]$ then in sectors 2, 3, 4,

5 and 6 the switching state corresponding to the similar vertex will be $[-1, 0, -1]$, $[0, 1, 1]$, $[-1, -1, 0]$, $[1, 0, 1]$ and $[0, -1, -1]$ respectively.

The memory required to store the switching states for a $n$-level inverter is $3n^3(n-1)/8$B. For example, 188B for 5-level, 772B for a 7-level and 2187B for a 9-level.

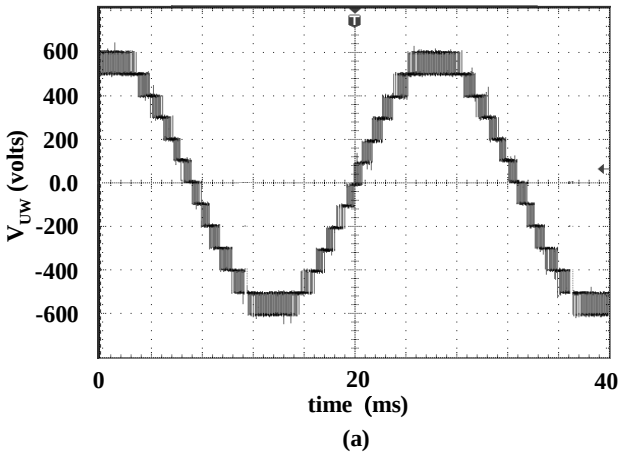



Figure 2.11: Line voltage for 7-level cascaded H-bridge inverter at $m_i$=0.89

Fig. 2.11 shows the line voltage $V_{UW}$ for 7-level cascaded H-bridge inverter at a modulation index of 0.89. The test was performed at $V_{dc}$=100V, fundamental frequency $f = 50$Hz and sampling frequency $f_s = 5$kHz. There are 13 levels in line voltage as expected. Using (2.14), the $V_{WTHD} \simeq 0.033\,\%$ for the waveform in Fig. 2.11.

## 2.6 Summary

A simple Space Vector PWM algorithm for a multilevel inverter based on standard two-level inverter has been proposed. The computations do not increase with level. The proposed method can be easily implemented using a commercially available motion control DSP or micro-controller, which normally supports only two-level modulation. The main advantage of the proposed scheme over earlier schemes is that, it can be used with an existing torque or speed control scheme implemented with two-level geometry. Since such schemes provide voltage reference in $\alpha$-$\beta$ coordinates, the proposed scheme uses most of the two-level calculation and adapts to any $n$-level inverter. The scheme can be used for both neutral point clamped and cascaded H-bridge inverter topologies. The scheme can be easily extended to include overmodulation range.

# Chapter 3

# Space Vector PWM Algorithm for Multilevel Inverters for Operation in Overmodulation Range

This chapter proposes a simple space vector PWM algorithm for a multilevel inverter for operation in overmodulation range. The proposed algorithm easily determines the location of reference vector and calculates on-times. It uses a simple mapping to generate gating signals for the inverter. A 5-level cascaded inverter is used to explain the algorithm. The algorithm can be easily extended to a $n$-level inverter. It is applicable to neutral point clamped topology as well. Experimental results are provided for 5-level, 7-level cascaded inverters and 3-level NPC inverter.

## 3.1 Introduction

The problems in implementing overmodulation for multilevel inverters are described in section 1.3.5 and the related literature survey in section 1.4.2. To address this problem, a simple algorithm is proposed in this chapter which extends the SVPWM algorithm proposed for linear mode in chapter 2 to overmodulation mode. The salient features of the proposed algorithm are given below.

• Simple on-time calculation due to the use of a two-level geometry. The overmodulation is modelled with simple mathematical expressions without any lookup tables. The on-time calculation equations do not change with the position of reference vector like the traditional approach in Mondal [87].

• An important merit of the proposed algorithm is that it can be used for any $n$-level ($n \geq 3$) inverter without any significant increase in computations.

• Fast method of determining the reference vector in the space vector diagram.

The chapter is organized in seven sections. Section 3.2 gives an overview of the modulation index and modes of modulation. Section 3.3 explains the proposed Space vector PWM algorithm in overmodulation mode for a 5-level inverter. Section 3.4 explains the implementation of the proposed algorithm for 5-level inverter. Section 3.5 shows the experimental results for 5-level. Section 3.6 explains the extension of the proposed scheme to any $n$-level inverter. The experimental result for

a 7-level cascaded inverter is shown. Section 3.7 summarizes the chapter.

## 3.2 Modulation Index and Modes of Modulation

For a 3-phase inverter, the modulation index $m_i$ [81] is defined as

$$m_i = \frac{v_1}{v_{1six-step}} \tag{3.1}$$

where $v_1$ is the peak value of fundamental voltage generated by the modulator and $v_{1six-step}$ is the peak value of fundamental voltage at six-step operation. For a $n$-level NPC topology [31] $v_{1six-step}=(2/\pi)V_{dc}$, which is same as for two-level inverter [81]. For a $n$-level cascaded topology $v_{1six-step}=(2/\pi)(n\text{-}1)V_{dc(HB)}$, where $V_{dc(HB)}$ is the DC link voltage on each H-bridge as shown in Fig. 1.3.

Based on the value of the modulation index $m_i$ ($0 \leq m_i \leq 1$), there are three modes of operation [81], namely sinusoidal mode or linear mode ($0 \leq m_i < 0.907$), overmodulation mode I ($0.907 \leq m_i < m_{max2}$) and overmodulation mode II ($m_{max2} \leq m_i < 1$). The value of $m_{max2}$ marks the boundary of overmodulation I and II.

The scheme proposed by Holtz [81] modifies the magnitude and phase of the reference voltage, to achieve the voltage control in overmodulation range. In [81] a value of 0.952 is used for $m_{max2}$. Methods such as [82][94] also use $m_{max2}=0.952$. Tripathi [83] obtains a higher value of $m_{max2}$ as 0.9535 through angular velocity balance of the flux displacement vector. In this chapter, the value of $m_{max2}$ is

taken to be 0.9535 and a strategy similar to [83] is used. The two-level based overmodulation schemes such as [82][130] can also be easily extended to a multilevel inverter using the implementation proposed in this chapter. The proposed SVPWM algorithm for overmodulation mode is described in the next section.

## 3.3 Operation in Overmodulation Mode

The space vector diagram of a 3-phase voltage source inverter is a hexagon, consisting of six sectors. Here, the operation is explained for the first sector, the same is applicable for other sectors too.

### 3.3.1 Overmodulation Mode I ($0.907 \leq m_i < 0.9535$)

In Fig. 3.1, the thick dotted circle shows the desired trajectory of the reference vector $\boldsymbol{v}^*$. Traditionally, depending on the value of $m_i$, the trajectory is modified and tip P of the actual vector $\boldsymbol{v_p^*}$ moves on trajectory $TSA_{12}RQ$ shown in thick solid lines. i.e. first it moves along the circular track $TS$, then along the linear track $SA_{12}R$ on the side $A_{10}A_{14}$ of the sector $OA_{10}A_{14}$ and finally along the circular track $RQ$. This modification in trajectory is intended to compensate for the loss in volt-secs. The linear movement along $A_{10}A_{14}$ is called 'hexagonal trajectory' in this chapter.

An approach similar to [83] is followed to compensate for the loss in volt-secs

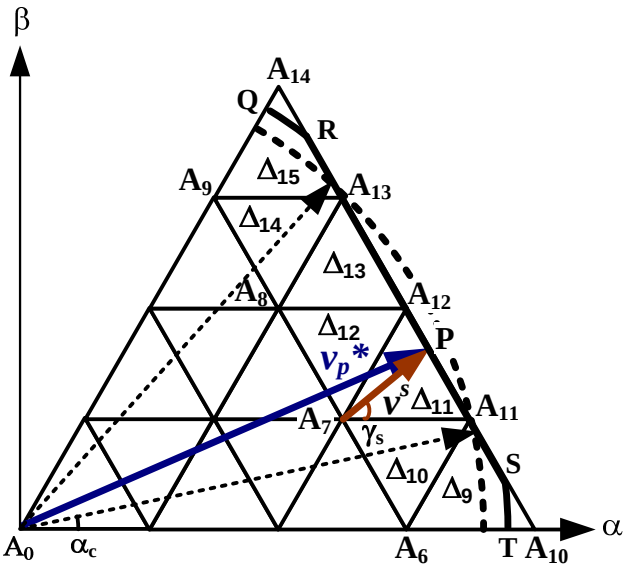



Figure 3.1: Space Vector Diagram of the first sector of a 5-level inverter showing Overmodulation Mode I, $0.907 \leq m_i < 0.9535$

by directly modifying the on-times of the switching vectors on circular track rather than modifying the reference vector.

Let $\alpha_c$ be the angle where the reference vector crosses the hexagon track, shown by the dotted arrow in Fig. 3.1. For $\alpha_c \leq \gamma < \pi/3\text{-}\alpha_c$ the vector moves on hexagonal track and for remaining part of the sector it moves on circular track. Using cartesian geometry, angle $\alpha_c$ is obtained as

$$\alpha_c = \frac{\pi}{6} - \cos^{-1}\left(\frac{\pi}{2m_i\sqrt{3}}\right) = 0.524 - \cos^{-1}\left(\frac{0.907}{m_i}\right) \tag{3.2}$$

For a given $m_i$, $\alpha_c$ is a fixed number and thus it need not be calculated in every switching period.

#### 3.3.1.1 Hexagonal Portion ($\alpha_c \leq \gamma < \pi/3\text{-}\alpha_c$)

For hexagonal track, using cartesian geometry, the coordinates of the tip P of vector $\boldsymbol{v_p^*}$ are given in terms of angle $\gamma$ and level of inverter $n$, as

$$(v_\alpha,\, v_\beta) = \left( \frac{\sqrt{3}(n-1)}{\sqrt{3}+\tan\gamma},\, \frac{\sqrt{3}(n-1)\tan\gamma}{\sqrt{3}+\tan\gamma} \right) \tag{3.3}$$

Knowing the coordinates $(v_\alpha,\, v_\beta)$ of $\boldsymbol{v_p^*}$ from (3.3), the on-times and triangle number can be obtained similar to linear mode, as explained below.

Two integers $k_1$ and $k_2$ are defined in (2.10) to find the triangle in which point P lies. Using the same definition of $k_1$ and $k_2$, these two integers are now given as,

$$k_1 = n-2,\ k_2 = \text{int}(v_\beta/h) \tag{3.4}$$

The tip of the vector $\boldsymbol{v_p^*}$ resides on one of the four triangles $\triangle_9$, $\triangle_{11}$, $\triangle_{13}$ and $\triangle_{15}$. These triangles are of type 1. Using this fact, the small vector $(v_{\alpha o}^s,\, v_{\beta o}^s)$ can be directly obtained from $(v_\alpha,\, v_\beta)$, without performing slope comparison. It is given as,

$$v_{\alpha o}^s = v_\alpha - k_1 + 0.5k_2,\ v_{\beta o}^s = v_\beta - k_2 h \tag{3.5}$$

Knowing $(v_{\alpha o}^s,\, v_{\beta o}^s)$, (2.5) is used to determine the on-time $t_a$. Similar to two-level, on-time $t_o$ is zero for hexagonal track, therefore $t_b$=$T_s$-$t_a$. Triangle number $\triangle_j$ is calculated using (2.12).

Flowchart in Fig. 3.3(c) shows the on-times and triangle number $\triangle_j$ calcula-

tion. Number of computations required for hexagonal track in Fig. 3.3(c) are less than that for circular track in Fig. 3.3(b).

#### 3.3.1.2 Circular Portion ($0 \leq \gamma < \alpha_c$ and $\pi/3 - \alpha_c \leq \gamma < \pi/3$)

Here, on-times are obtained using (2.5)-(2.7) as described before for the linear mode. However, on-times are modified to compensate for the loss of volt-secs during the linear trajectory as described below.

In the overmodulation mode I, at a modulation index $m_i$, the loss in volt-seconds over a sector is proportional to ($m_i$-0.907) [83]. Maximum possible value of $m_i$ is 0.9535. Therefore, maximum possible loss in volt-seconds over a sector is proportional to (0.9535-0.907). Let us define a compensation factor $\lambda$ as the ratio of actual loss in volt-secs and maximum loss in volt-secs. It is given as,

$$\lambda = \frac{(m_i - 0.907)}{(0.9535 - 0.907)} = \frac{(m_i - 0.907)}{0.0465} \tag{3.6}$$

Compensation factor $\lambda$ is used for modification of on-times for the volt-secs compensation. The $\lambda$ varies between 0 and 1, for $m_i$ between 0.907 and 0.9535. For a given $m_i$, $\lambda$ is a fixed number, and hence need not be calculated in every modulation cycle. Further details on $\lambda$ can be referred in [83].

In Fig. 3.1, for the circular portion, the point P can be within any of the triangles $\triangle_9 \rightarrow \triangle_{15}$. Type 1 triangles $\triangle_9$, $\triangle_{11}$, $\triangle_{13}$ and $\triangle_{15}$ have their two vertices on the side $A_{10}A_{14}$ of sector. Type 2 triangles $\triangle_{10}$, $\triangle_{12}$ and $\triangle_{14}$ have their one

vertex on the side $A_{10}A_{14}$ of sector. Let the on-times of the three vertices be $t_a$, $t_b$ and $t_o$ obtained from (2.5)-(2.7) through linear mode of modulation. For the two type of triangles, these on-times are modified differently as explained below.

- Modifications for Type 1 triangle:

  Let the on-times of the two vertices which are on the side of hexagon be $t_a$ and $t_b$, then the modified on-times are given as

$$\begin{aligned} t_a &= t_a + 0.5\lambda^2 t_o \\ t_b &= t_b + 0.5\lambda^2 t_o \\ t_o &= T_s - t_a - t_b \end{aligned} \tag{3.7}$$

  The modifications of on-times in (3.7) effectively reduce the on-times of the inner vector using $\lambda$ and increase the on-times of the outer vectors. It is explained in [83] that such scheme is suitable for fast close loop operation. Similarly, the on-times for the type 2 triangle are modified.

- Modifications for Type 2 triangle:

  Let the on-times of the two vertices that are not on the side of hexagon be $t_a$ and $t_b$, then the modified on-times are obtained as

$$\begin{aligned} t_a &= t_a - 0.5\lambda^2 t_a \\ t_b &= t_b - 0.5\lambda^2 t_b \\ t_o &= T_s - t_a - t_b \end{aligned} \tag{3.8}$$

  The modifications of on-times in (3.8) effectively reduce the on-times of the inner vectors and increase the on-times of the outer vector using $\lambda$.

In (3.7) or (3.8), there is no compensation at $m_i$=0.907 as $\lambda$=0. At $m_i$=0.9535, the compensation is maximum as $\lambda$=1 and $t_o$=0, which corresponds to complete movement along the hexagonal track.

For a given $m_i$, (3.6) and (3.7) or (3.8) are only modifications required to modify the on-times. No other lookup table or solution to complicated equations is required. Therefore, complexity of implementing overmodulation reduces. It also shows the low cost of implementing overmodulation on a microcontroller.

Above 0.9535, the circular part of the trajectory vanishes and the on-time $t_o$ obtained from (3.7) or (3.8) is negative which is meaningless. Above 0.9535, another mode is used called overmodulation II.

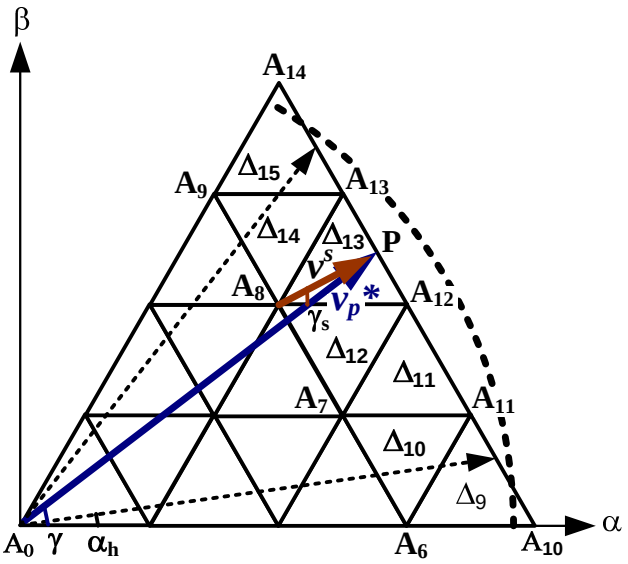



Figure 3.2: Space Vector Diagram of the first sector of a 5-level inverter showing Overmodulation Mode II, 0.9535≤$m_i$<1

### 3.3.2 Overmodulation Mode II (0.9535≤$m_i$<1)

Switching in overmodulation II is characterized by a hold angle $\alpha_h$, shown by the dotted arrow in Fig. 3.2. For $\alpha_h \leq \gamma < \pi/3\text{-}\alpha_h$, the tip P of the vector $\boldsymbol{v_p^*}$ moves on hexagonal track. In Fig. 3.2, let vectors at vertices $A_{10}$ and $A_{14}$ be addressed as large vectors. There are a total of six large vectors for the complete space vector diagram. For $0 \leq \gamma < \alpha_h$ and $\pi/3\text{-}\alpha_h \leq \gamma < \pi/3$, the vector $\boldsymbol{v_p^*}$ is held at one of the large vectors.

Normally, $\alpha_h$ is a nonlinear function of modulation index and obtained by a lookup table. In this chapter, the hold angle $\alpha_h$ is obtained using a strategy similar to [83] where $\alpha_h$ is calculated by obtaining the same average normalized angular velocity over a sector as the angular velocity of the reference vector. For the drives application if V/f is maintained, the angular velocity is proportional to modulation index $m_i$. Hence, at a given $m_i$, the time to traverse an angle $\delta$ is equal to $k\delta/m_i$ where $k$ is a constant. Similarly, time (i) to cover the linear portion is equal to $k(\pi/3\text{-}2\alpha_h)/0.9535$, (ii) to hold the vector $\boldsymbol{v_p^*}$ at the large vectors of a sector is $k(2\alpha_h)/1.0$, (iii) to cover whole sector is $k(\pi/3)/m_i$. A time balance equation can be written as,

$$\frac{\pi/3}{m_i} = \frac{2\alpha_h}{1.0} + \frac{\pi/3 - 2\alpha_h}{0.9535} \tag{3.9}$$

Simplification of (3.9) leads to the following expression for holding angle $\alpha_h$

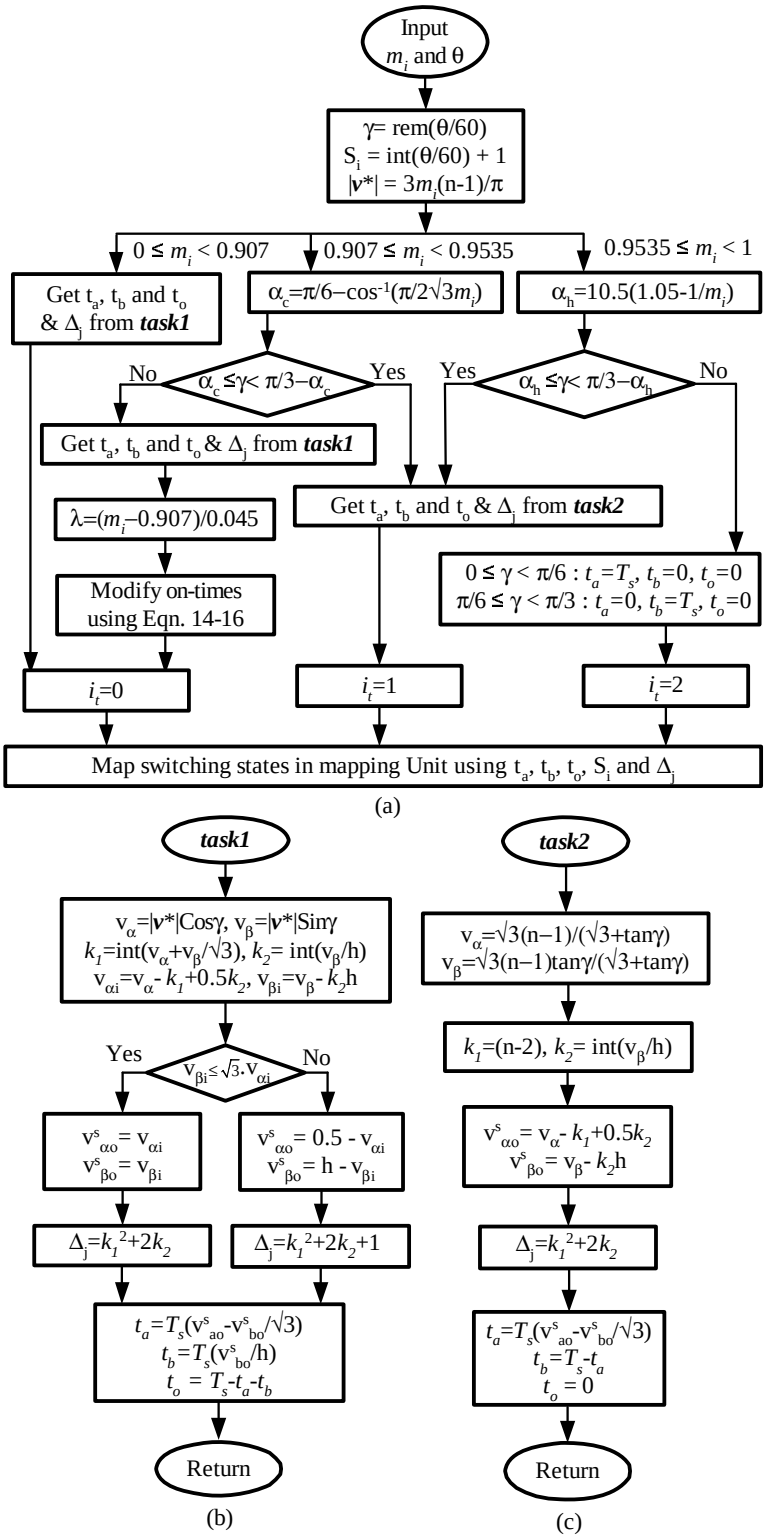



Figure 3.3: Flowchart (a) Main routine: overall modulation process (b) task 1: Subroutine to calculate on-times and triangle number for circular track (c) task 2: Subroutine to calculate on-times and triangle number for hexagonal track

as,

$$\alpha_h = 11.26 - 10.74/m_i \tag{3.10}$$

In (3.10), for a given $m_i$ only two arithmetic operations i.e. one division and one subtraction are required to obtain the hold angle $\alpha_h$. It shows the simplicity of implementing SVPWM in overmodulation mode II.

For $\alpha_h \leq \gamma < \pi/3\text{-}\alpha_h$, the on-time calculation is same as that during the hexagonal trajectory in overmodulation mode I. For $0 \leq \gamma < \alpha_h$ and $\pi/3\text{-}\alpha_h \leq \gamma < \pi/3$, the vector is held at one of the six large vectors. At $m_i$=1.0, hexagonal track vanishes and vector $\boldsymbol{v_p^*}$ is only held at the six large vectors sequentially. This is six-step operation similar to two-level inverter. Therefore, a multilevel inverter when operated at $m_i$=1.0, looses its multilevel characteristics.

## 3.4 Implementation for a 5-level inverter

The implementation for a 5-level inverter can be understood with the help of following block diagram. This is same as described in chapter 2 i.e. it has two basic units namely a processing unit and a mapping unit. It has been shown here to elaborate the effect of overmodulation.

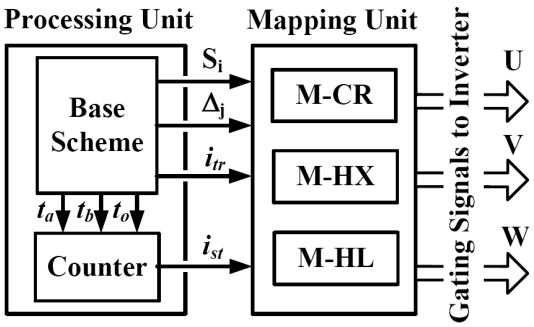



Figure 3.4: Simplified block diagram of the proposed algorithm

### 3.4.1 Processing Unit

Processing unit is same as explained in chapter 1. The base scheme for processing unit is explained in previous section, and summarized in flowchart in Fig. 3.3. It determines parameters such as sector, triangle, and calculates on-times. These details are subsequently used by mapping unit to generate gating signals.

### 3.4.2 Mapping Unit

The mapping unit stores switching sequences. A switching sequence is a set of switching states to be applied in a switching period. The structure of a switching sequence depends on the trajectory of the vector. There are three possible trajectories, (i) circular track: for linear modulation mode and some part of overmodulation I, (ii) hexagonal track: for some part in overmodulation I and overmodulation II, (iii) hold mode: in overmodulation II. Due to the difference in structures of switching sequence among the trajectories, three separate memory units M-CR, M-HX and M-HL are used in mapping unit, where CR, HX and HL stand for circular,

hexagonal and hold respectively. Flowchart in Fig. 3.3(a) introduces an integer parameter $i_{tr}$, called as track index. It is used for realtime implementation. It helps in identifying the memory unit with respect to track using three values as, (i) $i_{tr}$=0 for circular track, (ii) $i_{tr}$=1 for the hexagonal track, (iii) $i_{tr}$=2 for the hold mode. The $i_{tr}$ is independent of the level of inverter.

There exist 125 (=$5^3$) switching states $(s_u, s_v, s_w)$ for 5-level inverter, where $s_u, s_v, s_w \ \epsilon$ [-2, -1, 0, 1, 2]. In Fig. 2.4, the switching states for first sector in the space vector diagram are shown. A phase-leg state $s_x$ (x=u, v, w) describe the 'ON' or 'OFF' conditions of the switches in the respective phase. In Fig. 1.3, $S_{1X}$=$\overline{S_{3X}}$, $S_{2X}$=$\overline{S_{4X}}$, $S_{5X}$=$\overline{S_{7X}}$ and $S_{6X}$=$\overline{S_{8X}}$, where X=U, V, W. Hence, essentially four signals are required to control the eight switches of a phase-leg. Equivalently, each $s_x$ (x=u, v, w) requires four bits to store the state of the respective phase-leg. To this end, a twelve bit of memory in Fig. 3.5 stores a switching state at a memory location in M-CR, M-HX and M-HL units. Due to the difference in the switching sequences in these units, the order in which switching states are organized in memory units differ from one another.

| **Phase U** | | | | **Phase V** | | | | **Phase W** | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **$S_{1U}$** | **$S_{2U}$** | **$S_{5U}$** | **$S_{6U}$** | **$S_{1V}$** | **$S_{2V}$** | **$S_{5V}$** | **$S_{6V}$** | **$S_{1W}$** | **$S_{2W}$** | **$S_{5W}$** | **$S_{6W}$** |

Figure 3.5: Switching state at a memory location - ON/OFF signals for switches

#### 3.4.2.1 Memory unit for Circular Track (M-CR)

On circular track, tip P of the reference vector is positioned within a triangle $\triangle_0 \rightarrow \triangle_{15}$. There are redundant switching states at the vertices of the triangles. Due to redundant states, there could be several switching sequences for a triangle. For example, for the range $0.5236 \leq m_i < 0.7854$, at a switching period, the tip of the reference vector can be situated in triangle $\triangle_8$. For this triangle, following four sequences can be formed with minimum switching losses.

Seq. 1:

$(0,0,-2)_0 \Rightarrow (1,0,-2)_1 \Rightarrow (1,1,-2)_2 \Rightarrow (1,1,-1)_3 \Rightarrow (1,1,-1)_3 \Rightarrow (1,1,-2)_2 \Rightarrow (1,0,-2)_1 \Rightarrow (0,0,-2)_0$

Seq. 2:

$(1,1,-1)_0 \Rightarrow (2,1,-1)_1 \Rightarrow (2,2,-1)_2 \Rightarrow (2,2,0)_3 \Rightarrow (2,2,0)_3 \Rightarrow (2,2,-1)_2 \Rightarrow (2,1,-1)_1 \Rightarrow (1,1,-1)_0$

Seq. 3:

$(1,0,-2)_0 \Rightarrow (1,1,-2)_1 \Rightarrow (1,1,-1)_2 \Rightarrow (2,1,-1)_3 \Rightarrow (2,1,-1)_3 \Rightarrow (1,1,-1)_2 \Rightarrow (1,1,-2)_1 \Rightarrow (1,0,-2)_0$

Seq. 4:

$(1,1,-2)_0 \Rightarrow (1,1,-1)_1 \Rightarrow (2,1,-1)_2 \Rightarrow (2,2,-1)_3 \Rightarrow (2,2,-1)_3 \Rightarrow (2,1,-1)_2 \Rightarrow (1,1,-1)_1 \Rightarrow (1,1,-2)_0$

The subscript on a switching state is stage of the sequence. Stages $0 \rightarrow 3$ and $3 \rightarrow 0$ are the set and reset part of the sequence. Similarity to a two-level SVPWM can be seen here. Subscripts '0' and '3' represent the same vertex, and correspond to virtual zero vector of the two-level space vector diagram.

Generally, a continuous PWM sequence has four stages as shown above, and

a discontinuous PWM sequences have three stages [123]. The counter in processing unit generates stage number $i_{st}$ using the on-times $t_a$, $t_b$ and $t_o$. Here, $i_{st}$=0→3 for continuous SVM and $i_{st}$=0→2 for discontinuous SVM.

Among the various switching sequences for a triangle, only one can be applied at a switching period. Following examples explain the selection of a switching sequence using triangle $\triangle_8$.

- Example 1: Common Mode Voltage Reduction - In [99] a common mode voltage reduction scheme is given. The 5-level ($n$-level) space vector diagram is converted to equivalent 3-level ($n$-1-level) space vector diagram by retaining the switching states which generate zero common mode voltage. Due to the absence of redundancies, only one switching sequence exists for every triangle.

- Example 2: Intertriangle Switching Losses Minimization - There are two possible transitions of the reference vector for triangle $\triangle_8$. The transition depends on $m_i$, (i) for the range $0.5236 \leq m_i < 0.6614$, the transition is $\triangle_5 \hookrightarrow \triangle_8$, and Seq. 1 (or 2) is selected, (ii) for the range $0.6614 \leq m_i < 0.7854$, the transition is $\triangle_{14} \hookrightarrow \triangle_8$, and Seq. 3 (or 4) is selected. Here '$\hookrightarrow$' signifies transition between triangles.

- Example 3: DC-link Balancing in NPC topology - DC-link balancing is a key issue [84][131] for NPC topology. To have a better control authority over DC-link balance, a sequence is selected whose virtual zero vector has highest duty ratio among the three duty ratios i.e. $d_{A_5}$, $d_{A_8}$ and $d_{A_9}$ for triangle $\triangle_8$.

Therefore, in triangle $\triangle_8$, Seq. 1 (or 2) is selected if $d_{A_5}$ is maximum, Seq. 3 is selected if $d_{A_8}$ is maximum and Seq. 4 is selected if $d_{A_9}$ is maximum. This technique is well known for 3-level inverter.

These examples show that the selection of a switching sequence is dependent on the modulation scheme. For a given scheme, a set of relevant switching sequences can be identified for every triangle and stored in memory unit in contiguous locations. This is an off-line process.

To this end, a 11 bit address is given in Fig. 3.6. This address identifies a memory location in M-CR unit. It is divided into four parts, (i) 'Sector': 3 bits $SC_0 \rightarrow SC_2$, as for sector number $S_i$, i=1→6 (ii) 'Triangle': 4 bits $TR_0 \rightarrow TR_3$, as for triangle number $\triangle_j$, j=0→15 (iii) 'Sequence': 2 bits $SQ_0 \rightarrow SQ_1$, considering a retention of maximum four sequences per triangle (iv) 'Stage': 2 bits $ST_0 \rightarrow ST_1$, considering three or four stages per sequence with respect to continuous or discontinuous SVM respectively.

| $SC_2$ | $SC_1$ | $SC_0$ | $TR_3$ | $TR_2$ | $TR_1$ | $TR_0$ | $SQ_1$ | $SQ_0$ | $ST_1$ | $ST_0$ |
|---|---|---|---|---|---|---|---|---|---|---|

Figure 3.6: Memory address for circular track

For a given modulation scheme, at any switching period, the processing unit calculates these parameters. Using these parameters, a memory location (switching state) is identified. Since the contents of a memory location represent 'ON' or 'OFF' condition for the switches of the inverter, they can be directly applied for generating gating signals. The proposed mapping concept can be used to implement a variety

of schemes as explained above. It shows the generality of the proposed mapping concept.

#### 3.4.2.2 Memory unit for Hexagonal Track (M-HX)

On hexagonal track in Fig. 3.1 and Fig. 3.2, the tip P of the vector moves along $\overrightarrow{A_{10}A_{14}}$ on a side of one of the triangles $\triangle_9$, $\triangle_{11}$, $\triangle_{13}$ and $\triangle_{15}$. There is one switching state at a vertex on hexagonal track. The switching states at the nearest two vectors are utilized to form a switching sequence. For example; for triangle $\triangle_9$, the switching sequence is $(2,\text{-}2,\text{-}2)_0 \Rightarrow (2,\text{-}1,\text{-}2)_1 \Rightarrow (2,\text{-}1,\text{-}2)_1 \Rightarrow (2,\text{-}2,\text{-}2)_0$. Conclusively, a switching sequence on hexagonal track has only two stages. The counter in processing unit generates stage number $i_{st}$ using on-times $t_a$ and $t_b$.

To this end, a 8 bit address is given in Fig. 3.7. This address identifies a memory location in M-HX unit. It is divided into three parts, (i) 'Sector': 3 bits $SC_0 \rightarrow SC_2$ (ii) 'Triangle': 4 bits $TR_0 \rightarrow TR_3$ (iii) 'Stage': 1 bit $ST_0$, as only two stages exist. Due to the absence of redundant switching states, only one switching sequence exists for a triangle on hexagonal track.

| $SC_2$ | $SC_1$ | $SC_0$ | $TR_3$ | $TR_2$ | $TR_1$ | $TR_0$ | $ST_0$ |
|---|---|---|---|---|---|---|---|

Figure 3.7: Memory address for hexagonal track

#### 3.4.2.3 Memory unit for Hold Mode (M-HL)

In hold mode, the vector $\boldsymbol{v}_{\boldsymbol{p}}^{*}$ is held at a large vector. The switching state at this vertex e.g. (2,-2,-2) is applied for full switching period. Unlike other two tracks, the switching sequence contains only one stage in hold mode. To this end, a 3 bit address is given in Fig. 3.7, to identify a memory location in M-HL unit. The 'Triangle', 'Sequence' and 'Stage' are not required here.


Figure 3.8: Memory address for hold mode

This implementation is advantageous as compared to implementation of carrier based schemes for a multilevel inverter. In carrier based schemes, a separate controller might be required for every H-bridge [99] as every phase-leg is controlled separately. In such implementation, the synchronization of the controllers might lead to implementation complexity. On the other hand, using the proposed scheme a single controller unit generates the gating signals for all the switches of the inverter.

The proposed scheme is applicable to both NPC and cascaded inverter. For a given level, the two topologies have same space vector diagram and equal number of power switches, so the cost of peripherals does not change. The processing unit is same for both the topologies. For a given level, there are equal number of controllable switches in these topologies but their arrangement is different. Hence,

for a given switching state, the gating signals or the set of bits at a memory location in Fig. 3.5 differ for the two topologies. Hence, the mapping unit should be redesigned while changing from one topology to the other. The implementation of the proposed scheme for a 3-level NPC inverter is shown in Fig. 3.12 and Fig. 3.13.

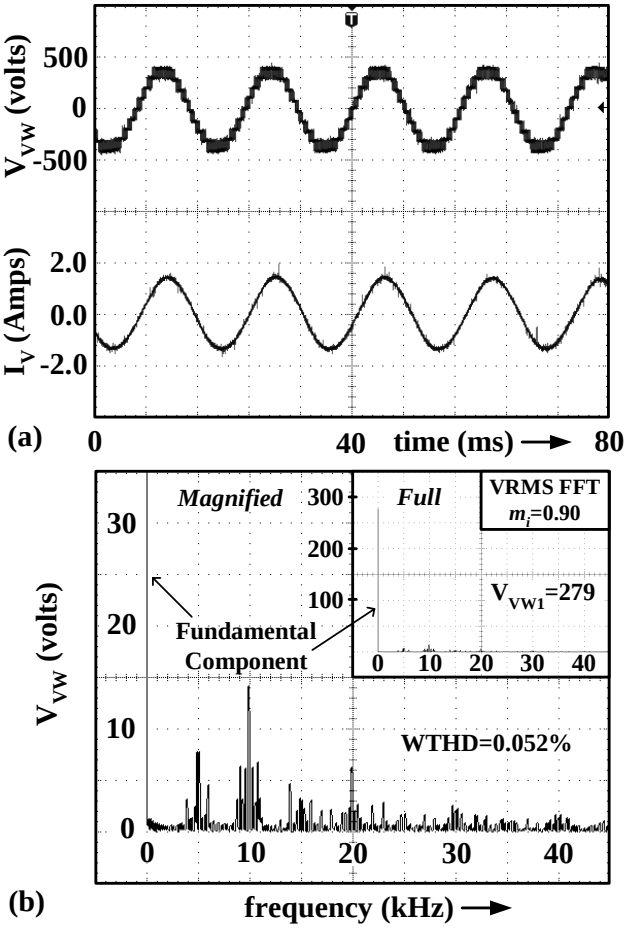



Figure 3.9: Voltage $V_{VW}$, current $I_V$ and FFT of voltage $V_{VW}$ at $m_i$=0.90

## 3.5 Experimental Results

The algorithm is implemented using a dSPACE DS1104 card, due to its availability. Owing to the simplicity of the algorithm it can be easily implemented on

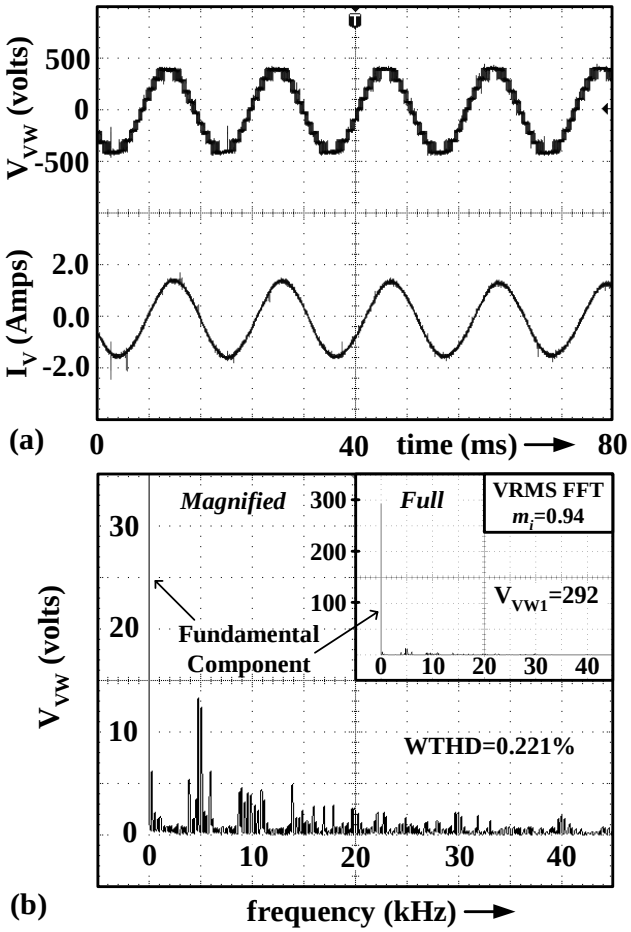



Figure 3.10: Voltage $V_{VW}$, current $I_V$ and FFT of voltage $V_{VW}$ at $m_i$=0.94

a fixed point DSP as well.

Fig. 3.9-Fig. 3.11 shows the experimental results for a laboratory prototype of a 5-level cascaded inverter. The test was performed on a 0.75 kW induction motor at $V_{dc(HB)}$=100V, fundamental frequency $f = 50$Hz and sampling frequency $f_s = 5$kHz. Here, $V_{dc(HB)}$ is voltage applied on each H-bridge module per Fig. 1.3.

Fig. 3.9 (a), Fig. 3.10 (a) and Fig. 3.11 (a) show the line voltage $V_{VW}$ and current $I_V$ at a modulation index of 0.90, 0.94 and 0.98 corresponding to linear mode,

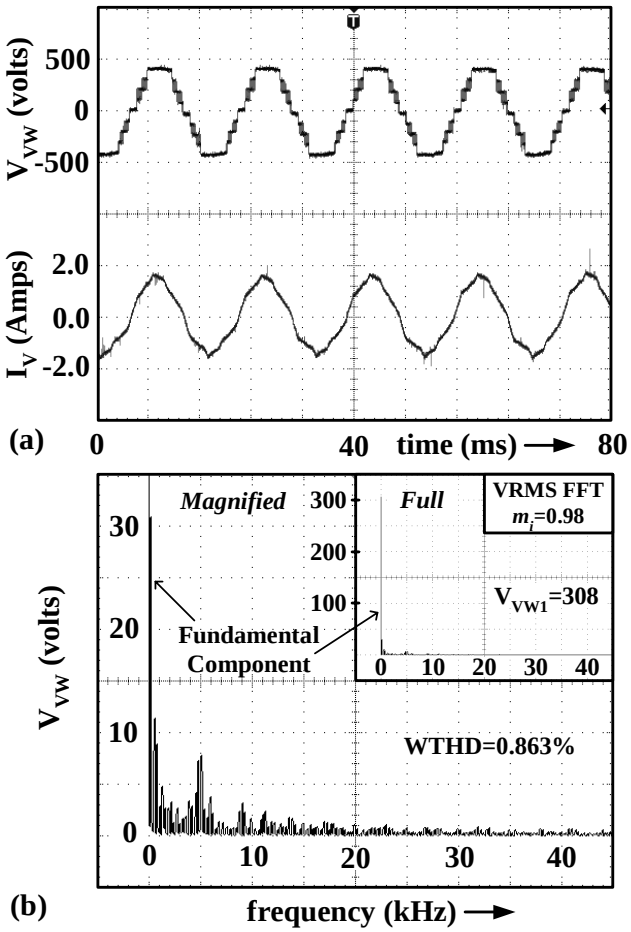



Figure 3.11: Voltage $V_{VW}$, current $I_V$ and FFT of voltage $V_{VW}$ at $m_i$=0.98

overmodulation mode I and overmodulation mode II respectively.

Fig. 3.9 (b), Fig. 3.10 (b) and Fig. 3.11 (b) show the linear RMS FFT of line voltage $V_{VW}$ at a modulation index of 0.90, 0.94 and 0.98 corresponding to the linear mode, overmodulation mode I and mode II respectively. In Fig. 3.9 (b), Fig. 3.10 (b) and Fig. 3.11 (b) and ($c_2$), the top right quarter is complete FFT. This FFT is 10 times vertically magnified to study various harmonics which occupies the remaining three quarters. The $V_{VW1}$ is RMS value of fundamental component of the line voltage. For a cascaded inverter, theoretical RMS value of $V_{VW1}$ is given

as $\sqrt{6}/\pi.m_i.(n\text{-}1).\mathrm{V}_{dc(HB)}$. The error between experimental and theoretical value is less than 1% for the three cases. The error between simulation and theoretical value is less than 0.4% for at any $m_i$.

Fig. 3.12 and Fig. 3.13 show line voltage waveform, current waveform and FFT of the voltage for a 3-level NPC inverter. The DC-link voltage is 170 V, modulation index $m_i$=0.8, switching frequency 5 kHz, fundamental frequency 50 Hz, load inductance per phase 0.47 H and load resistance per phase 48.4 Ω. Inset in Fig. 3.12($\mathrm{b}_2$) and Fig. 3.13($\mathrm{c}_2$) show the absence of lower order harmonics. For the inset, the horizontal axis is frequency in kHz.

## 3.6 Extension of the algorithm to $n$-level inverter

The block diagram in Fig. 3.4 describe the proposed scheme and its implementation for a 5-level inverter. Some changes can be expected when it is applied to a $n$-level inverter. The processing unit with respect to the computational load, and mapping unit with respect to memory requirement is discussed next.

### 3.6.1 Processing Unit

The processing unit calculates on-times and basic parameters to apply a switching state. The base scheme in Fig. 3.4 is essentially the flowchart in Fig. 3.3. This flowchart is given for a $n$-level inverter. The main routine in Fig. 3.3(a) and

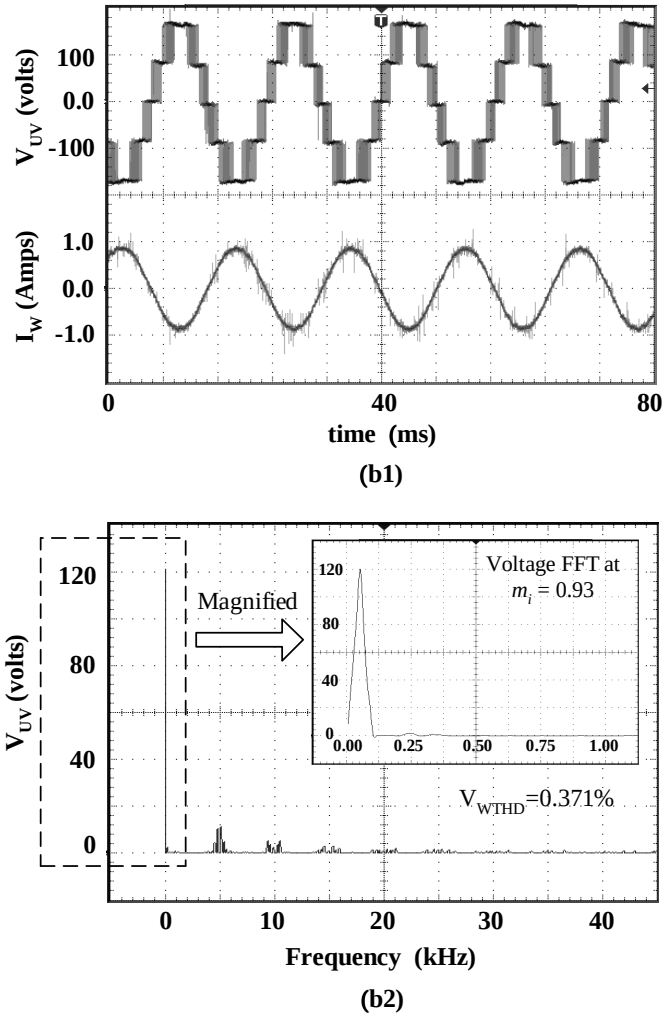



Figure 3.12: Voltage $V_{VW}$, current $I_V$ and FFT of voltage $V_{VW}$ at $m_i$=0.93

sub-routine *task*2 in Fig. 3.3(c) use $n$ as a linear constant, showing that number of computations are same for any value of $n$. Whereas *task*1 in Fig. 3.3(b) is independent of $n$. Therefore, the number of computations for the base scheme in processing unit remain same for any value of $n$. Conclusively, same processing unit can be used for any level $n$ without any change.

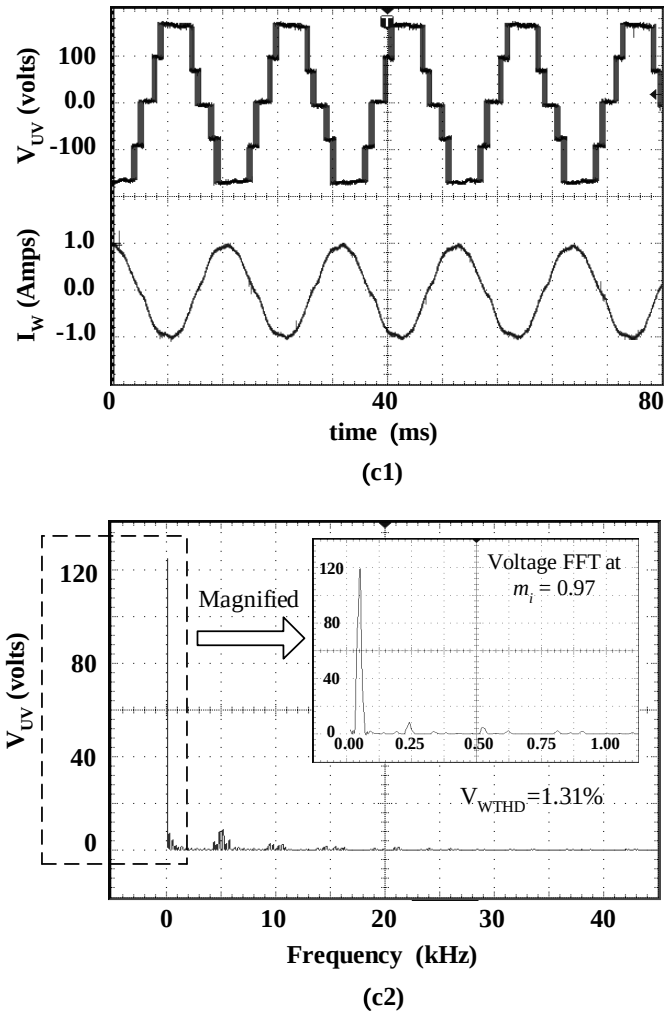



Figure 3.13: Voltage $V_{VW}$, current $I_V$ and FFT of voltage $V_{VW}$ at $m_i$=0.97

### 3.6.2 Mapping unit

Conceptually, the mapping unit for $n$-level is same as shown in Fig. 3.4. However, there are following two structural changes in the number of bits at a memory location in Fig. 3.5 and its address in Fig. 3.6-3.7.

1. In Fig. 3.5, for $n$-level, 3.($n$-1) bits are required to store a switching state at a memory location.

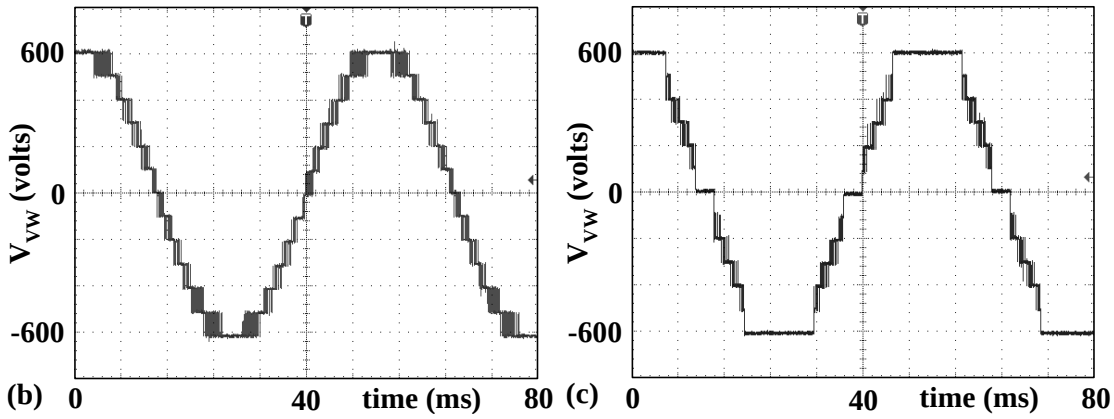



Figure 3.14: Line voltage for 7-level inverter at (b) $m_i$=0.93 (c) $m_i$=0.97

2. The bits required for 'Triangle' in Fig. 3.6-3.7 change, as there are $(n\text{-}1)^2$ triangles per sector. For example, 7 bits are required for 'Triangle' part for a 11-level inverter as there are 100 triangles per sector. Except 'Triangle', other parts in Fig. 3.6-3.7 remain unaffected by the change in $n$.

Commercially available EPROM chips of 1 k-bytes, 4 k-bytes, 16 k-bytes, 32 k-bytes and 64 k-bytes sizes fulfill the memory requirement of mapping unit, to implement the proposed scheme for 3-level, 5-level, 7-level, 9-level and 11-level inverter respectively. This estimation is based on the memory structure shown in Fig. 3.5-3.8 where the bits at memory location are directly used for generating gating signals. This estimation may change with modulation scheme. The memory requirement increases with $n$, as switching states $\alpha$ $n^3$.

Fig. 3.14(b) and (c) show the line voltage $V_{VW}$ for 7-level cascaded inverter at a modulation index of 0.93 and 0.97. For this implementation, same processing unit is used as for 5-level without any change. The mapping unit is modified per

the requirements of 7-level inverter. The test was performed at $V_{dc(HB)}$=100V, fundamental frequency $f = 50$Hz and sampling frequency $f_s = 5$kHz.

## 3.7 Summary

This chapter proposes a SVPWM based scheme to perform overmodulation for a multilevel inverter, and its implementation. The position of the vector is identified using an integer parameter, called as triangle number. The switching sequences are mapped with respect to triangle number. The on-times calculation is based on on-time calculation for two-level SVPWM. The on-time calculation equations do not change with triangle. A simple method of calculating on-times in the overmodulation range is used, hence a solution to complex equations and lookup tables are not required. This leads to ease of implementation. There are no significant change in computation with the increase in level. The proposed implementation is general in nature and can be applied to a variety of modulation schemes. The implementation is shown for a 5-level and 7-level cascaded inverter. The experimental results are provided. The proposed method can be easily implemented using a commercially available motion control DSP or micro-controller, which normally supports only two-level modulation.

# Chapter 4

# Space Vector PWM Scheme to Reduce Common Mode Voltage for Cascaded Multilevel Inverters

Multilevel inverters also produce the common mode voltage. As discussed in section 1.3.1, schemes have been reported for multilevel inverters that reduce the common mode voltage. However, most of the schemes result in reduced modulation depth, high switching losses and high harmonic distortion. This chapter proposes a space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters. The proposed scheme can increase the voltage range of operation by about 17% and can produce lower THD than the previously proposed schemes. The scheme is explained for 5-level inverter and then extended to a $n$-level cascaded inverter. Both experimental and simulation results are provided.

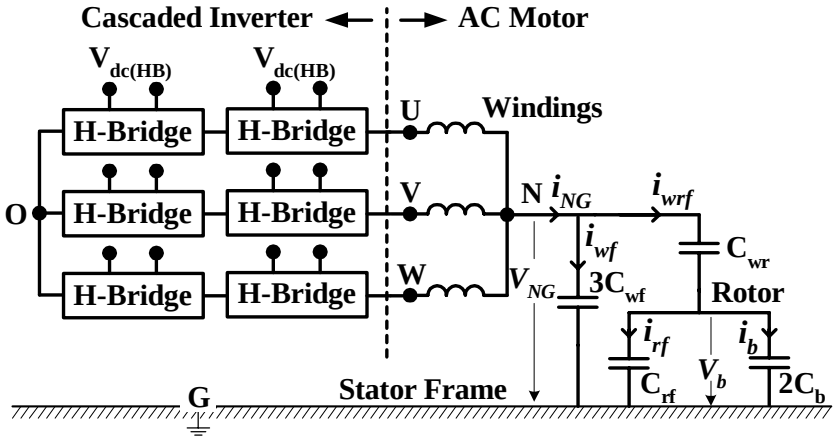



Figure 4.1: Circuit layout of inverter and motor system

## 4.1 Introduction

The cause and effects of common mode voltage are well described in section 1.3.1 and the related literature survey in section 1.4.3. Nevertheless, for simplicity some of the useful terms and definitions discussed in section 1.3.1 are given below.

Fig.4.1 shows a 5-level cascaded H-Bridge inverter [8] and the motor equivalent circuit [52]. The output of the H-Bridges are connected in series to produce the cascaded multilevel waveform. The common mode voltage in Fig.4.1 is $V_{NG} = (V_{UG} + V_{VG} + V_{WG})/3$. This voltage is responsible for bearing currents.

The voltage $V_b$ in Fig.4.1 is the bearing voltage and it depends on $V_{NG}$. The relation between the two voltage is called bearing voltage ratio ($BVR$) [45] and is defined as [52],

$$BVR = \frac{V_b}{V_{NG}} = \frac{C_{wr}}{C_{wr} + C_{rf} + 2C_b} \tag{4.1}$$

In section 1.3.1 the problems due to common mode voltage are described. In section 1.4.3, the problems in complete (zero-$V_{NO}$) and partial elimination methods are discussed. This chapter proposes a new scheme for a $n$-level ($n \geq 5$) cascaded inverter to address some of the problems mentioned in section 1.4.3. In the proposed scheme, a simple method of forming switching sequence is adduced that leads to minimum change in $V_{NO}$ as compared to other schemes. The proposed scheme suggests a modification in the space vector diagram by which a higher voltage can be attained while $|V_{NO}| \leq V_{dc(HB)}/3$. The salient features of the scheme are listed below.

- For any state transition maximum change in $V_{NO}$ is $V_{dc(HB)}/3$. This is an advantage over partial elimination scheme implemented using conventional SVPWM where for some state transitions, change in $V_{NO}$ is $2V_{dc(HB)}/3$.

- It has overall reduced number of changes in $V_{NO}$ which leads to reduced number of $dV_{NG}/dt$ occurrences. This is an advantage over many schemes described in section 1.4.3.

- For a 5-level inverter, the scheme can be operated till $m_i = 0.9163$ while maintaining $|V_{NO}| \leq V_{dc(HB)}/3$. This modulation limit is nearly 17% higher than schemes such as [99][101]. This is an advantage over both partial and complete elimination schemes.

- It uses nearest vectors leading to THD close to conventional scheme but significantly smaller than zero-$V_{NO}$ scheme. This is an advantage over complete

elimination schemes.

- It can be extended to higher level and can be easily implemented.

The chapter is divided into six sections. In section 4.2, the methodology is explained for a 5-level cascaded inverter. Section 4.3 explains the implementation of the proposed scheme. Section 4.4 discusses the experimental results. Section 4.5 explains the proposed scheme at higher levels. Section 4.6 concludes the chapter.

## 4.2 Proposed Scheme

The voltage $V_{NO}$ in Fig. 4.1 is given as,

$$V_{NO} = \frac{V_{UO} + V_{VO} + V_{WO}}{3} \tag{4.2}$$

Fig. 4.2 shows the first sector $S_1$ of the space vector diagram of a 3-phase 5-level inverter. It consists of sixteen equilateral triangles $\Delta_0$-$\Delta_{15}$ as shown in Fig. 4.2. The vertices of the triangle are made up of switching state vectors, they can be represented by one or more switching states. The switching state is determined by the set $(s_u, s_v, s_w)$, where $s_u \in \{-2, -1, 0, 1, 2\}$. The switching states not only determine the phase voltages but also the common mode voltage. The voltage $V_{NO}$ given by (4.2) can be rewritten as,

$$V_{NO} = \frac{V_{dc(HB)}(s_u + s_v + s_w)}{3} \tag{4.3}$$

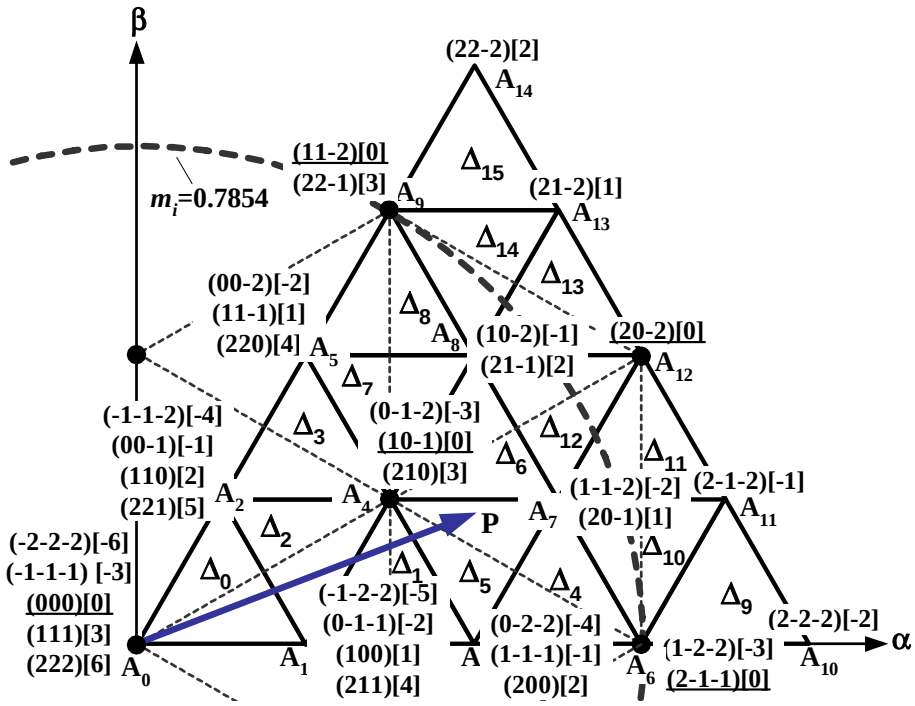



Figure 4.2: First sector of a 5-level inverter showing all the switching states

For simplification, the voltage $V_{NO}$ in (4.3) can be normalized with respect to $V_{dc(HB)}/3$ as,

$$v_{NO} = \frac{V_{NO}}{V_{dc(HB)}/3} = s_u + s_v + s_w \tag{4.4}$$

The normalized voltage $v_{NO}$ is independent of the DC-link voltage $V_{dc(HB)}$ and level of inverter $n$. It is only dependent on the switching state $(\mathrm{s}_u, \mathrm{s}_v, \mathrm{s}_w)$. In Fig. 4.2, $v_{NO}$ associated with every switching state is shown in a square bracket next to it. It varies between -6 and 6.

In order to minimize common mode voltage, only those switching states are considered that produce $|v_{NO}| \leq 1$. In so doing, a reduced set of switching states for a sector is obtained as shown in Fig. 4.3. However, large vectors given by $\mathrm{A}_{10}$ and

$A_{14}$ have a single switching state that produces $|v_{NO}|$=2. Hence, we have no choice but to avoid them. This results in drop in volt-sec at higher modulation index. In order to compensate for the lost volt-sec, a voltage vector with appropriate real and imaginary components is needed. For example if the reference vector is in triangle $\triangle_9$, $A_{10}$ is not switched. To compensate the drop in volt-sec, vector $F_{13}$ from adjacent sector is selected. It produces $v_{NO}$=-1 and has a real part greater than $A_6$. However, due to negative imaginary part, the resultant switching sequence produces a higher distortion. The same logic applies to triangle $\triangle_{15}$, the vector $B_{11}$ from adjacent sector is selected to avoid switching $A_{14}$. This idea is then extended to all sectors. The modified space vector diagram in Fig. 4.3 consists of 14 equilateral triangles $\triangle_0 \rightarrow \triangle_8$ & $\triangle_{10} \rightarrow \triangle_{14}$, and two isosceles triangles $\triangle_{9a}$ & $\triangle_{15a}$.

For the 5-level inverter, the proposed scheme can be operated with $v_{NO} \leq 1$ until $m_i$=0.9163. The range of operation is shown with the dotted circle in Fig.4.3. On the other hand, in Fig.4.2 the dotted circle represents the maximum modulation index, $m_i$=0.7854, for zero-$V_{NO}$ scheme. This includes only a part of the entire linear modulation range. As opposed to that, for the proposed scheme, $m_i = 0.9163$ encompasses the entire linear modulation range as well as a part of the overmodulation range. Though the partial elimination scheme [99] achieves $m_i$>0.7854 , it results in $v_{NO}$>1 for the higher modulation index.

For any triangle in Fig.4.3, two parameters are required to perform space

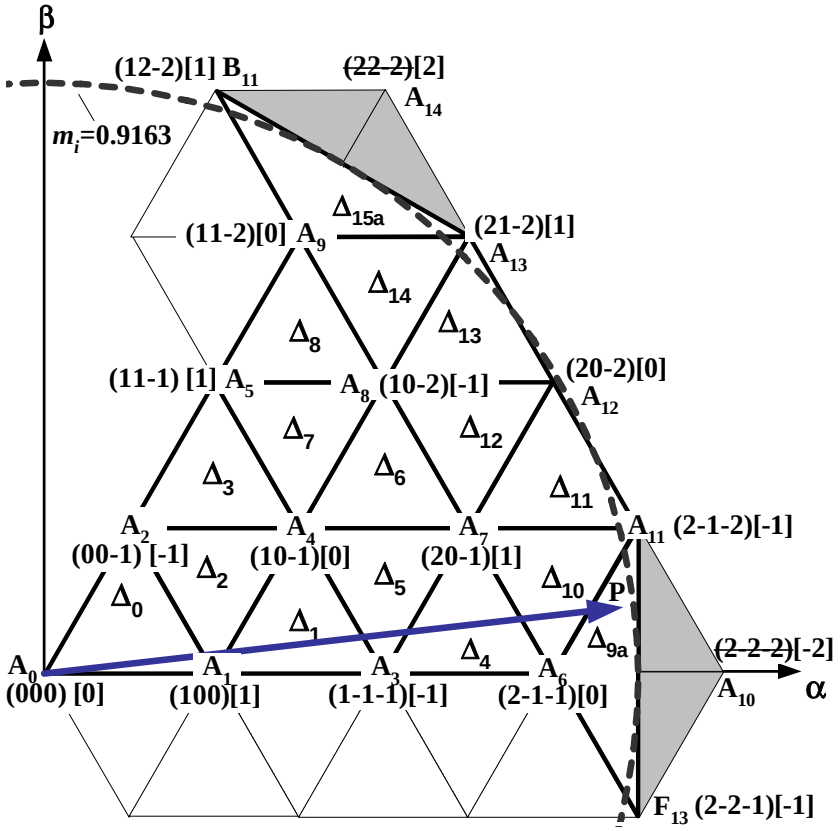



Figure 4.3: First sector of 5-level inverter showing selected switching states

vector modulation with reduced common mode voltage, (i) duty-ratio of the three vectors, (ii) switching sequence for the triangle that produces lowest value of $V_{NO}$ and has minimum number of commutations. Due to the difference in shapes, the modulation for equilateral and isosceles triangle is different as described next.

### 4.2.1 Equilateral Triangle

Procedure for the determination of duty-ratios and switching sequence for the equilateral triangles is described below.

#### 4.2.1.1 Duty-ratios

The SVPWM algorithm proposed in chapter 2 calculates the duty-ratio for conventional multilevel space vector diagram where each triangle is equilateral as shown in Fig. 4.2. The same scheme can be applied for calculating the duty-ratio $d_o$, $d_a$, $d_b$ for equilateral triangles in Fig. 4.3.

#### 4.2.1.2 Switching Sequence

The switching sequences are generated to meet two objectives,

- $v_{NO}$ changes by 1 for any state change in a leg.
- There is no additional change in $v_{NO}$ when reference vector moves from a triangle to its adjacent triangle.

The switching states at the vertices of any equilateral triangle in Fig. 4.3 produce three different $v_{NO}$: -1, 0 and 1. Considering two objectives mentioned above, a switching sequence is proposed that causes $v_{NO}$ to change as [-1]→[0]→[1]→[0]→[-1]. The switching sequences inside an equilateral triangle for half of the switching cycle ($T_s$) are shown in table 4.1. For remaining half of the switching cycle, the sequence reverses.

Only four commutations occur in one complete switching cycle ($2T_s$), leading to only four changes in $v_{NO}$ per switching cycle. The maximum change in line voltage at motor terminals is $V_{dc(HB)}$ similar to conventional SVPWM scheme.

| Triangle | $\downarrow \mathrm{SS}_0 \rightarrow$ | $\rightarrow \mathrm{SS}_1 \rightarrow$ | $\rightarrow \mathrm{SS}_2 \uparrow$ |
|---|---|---|---|
| $\triangle_0$ | (0,0,-1) [-1] | (0,0,0) [0] | (1,0,0) [1] |
| $\triangle_1$ | (1,-1,-1) [-1] | (1,0,-1) [0] | (1,0,0) [1] |
| $\triangle_2$ | (0,0,-1) [-1] | (1,0,-1) [0] | (1,0,0) [1] |
| $\triangle_3$ | (0,0,-1) [-1] | (1,0,-1) [0] | (1,1,-1) [1] |
| $\triangle_4$ | (1,-1,-1) [-1] | (2,-1,-1) [0] | (2,0,-1) [1] |
| $\triangle_5$ | (1,-1,-1) [-1] | (1,0,-1) [0] | (2,0,-1) [1] |
| $\triangle_6$ | (1,0,-2) [-1] | (1,0,-1) [0] | (2,0,-1) [1] |
| $\triangle_7$ | (1,0,-2) [-1] | (1,0,-1) [0] | (1,1,-1) [1] |
| $\triangle_8$ | (1,0,-2) [-1] | (1,1,-2) [0] | (1,1,-1) [1] |
| $\triangle_{10}$ | (2,-1,-2) [-1] | (2,-1,-1) [0] | (2,0,-1) [1] |
| $\triangle_{11}$ | (2,-1,-2) [-1] | (2,0,-2) [0] | (2,0,-1) [1] |
| $\triangle_{12}$ | (1,0,-2) [-1] | (2,0,-2) [0] | (2,0,-1) [1] |
| $\triangle_{13}$ | (1,0,-2) [-1] | (2,0,-2) [0] | (2,1,-2) [1] |
| $\triangle_{14}$ | (1,0,-2) [-1] | (1,1,-2) [0] | (2,1,-2) [1] |

Table 4.1: Switching sequence for the equilateral triangles

### 4.2.2 Isosceles Triangle

A different method is used to calculate duty-ratios and determine the switching sequence for isosceles triangles.

#### 4.2.2.1 Duty-ratios

Duty-ratios for isosceles triangles are calculated by applying volt-sec balance to the switching states in these triangles. Fig. 4.4 shows a part of Fig. 4.3 to emphasize the case where reference vector $\boldsymbol{v}^*(\overrightarrow{A_0P})$ lies in triangle $\triangle_{9a}$.

The volt-sec and duty-ratio balance for $\triangle_{9a}$ is given as,

$$d_{A_6}.\overrightarrow{A_0A_6} + d_{A_{11}}.\overrightarrow{A_0A_{11}} + d_{F_{13}}.\overrightarrow{A_0F_{13}} = \overrightarrow{A_0P} \tag{4.5}$$

$$d_{A_6} + d_{A_{11}} + d_{F_{13}} = 1 \tag{4.6}$$

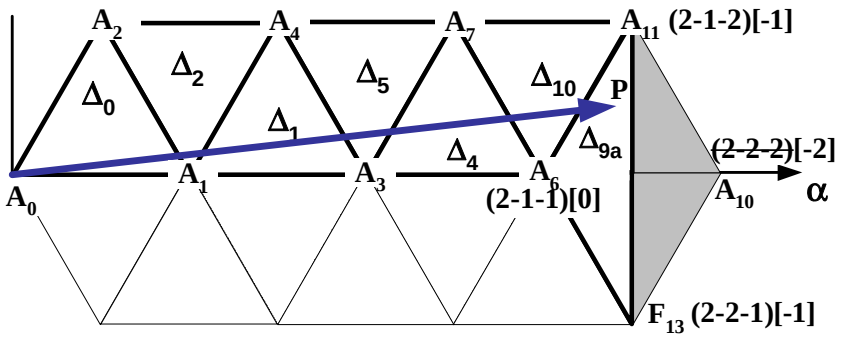



Figure 4.4: Part of the first sector to emphasize operation in triangle $\triangle_{9a}$

Where $|A_6F_{13}|$=1. Resolving (4.5) in $\alpha$-$\beta$ components and solving with (4.6), the following equations are obtained to calculate duty-ratios,

$$\begin{aligned} d_a &= d_{F_{13}} = -3 + v_\alpha + v_\beta/1.732 \\ d_b &= d_{A_{11}} = -3 + v_\alpha - v_\beta/1.732 \\ d_o &= d_{A_6} = 1 - d_a - d_b \end{aligned} \tag{4.7}$$

Similarly, referring to Fig. 4.3, following equations are obtained to calculate duty-ratios for triangle $\triangle_{15a}$,

$$\begin{aligned} d_a &= d_{A_{13}} = -3 + v_\beta/0.866 \\ d_b &= d_{B_{11}} = -3 + v_\alpha + v_\beta/1.732 \\ d_o &= d_{A_9} = 1 - d_a - d_b \end{aligned} \tag{4.8}$$

#### 4.2.2.2 Switching Sequence

The switching states at the vertices of an isosceles triangle in Fig. 4.3 produce two different sets of $v_{NO}$ [-1, 0] for $\triangle_{9a}$ and [0, 1] for $\triangle_{15a}$. Like equilateral triangles, a switching sequence in the increasing order of their $v_{NO}$ is proposed. The switching sequences for these two isosceles triangles are shown in table 4.2.

As mentioned before, THD is relatively higher for isosceles triangles. Apart

| Triangle | $\downarrow \mathrm{SS}_0 \rightarrow$ | $\rightarrow \mathrm{SS}_1 \rightarrow$ | $\rightarrow \mathrm{SS}_2 \uparrow$ |
|---|---|---|---|
| $\triangle_{9a}$<br>$\triangle_{15a}$ | (2,-1,-2) [-1]<br>(1,1,-2) [0] | (2,-2,-1) [-1]<br>(2,1,-2) [1] | (2,-1,-1) [0]<br>(1,2,-2) [1] |

Table 4.2: Switching sequence for the isosceles triangles

from this, there is only one disadvantage i.e. six commutations per switching cycle as compared to four for an equilateral triangle.

However, since the equilateral triangles dominate most of the space vector diagram, the output performance and common mode voltage are governed mainly by equilateral triangles.

## 4.3 Implementation for a 5-level inverter

To implement a SVPWM scheme, we need to identify the sector $\mathrm{S}_i$ and then triangle $\triangle_j$ where the tip of the reference vector is located. From table 4.1 and 4.2, the switching sequence is $\mathrm{SS}_0 \rightarrow \mathrm{SS}_1 \rightarrow \mathrm{SS}_2 \rightarrow \mathrm{SS}_1 \rightarrow \mathrm{SS}_0$. The subscript on SS is stage $k_{st}$ of the sequence and is useful for real time implementation. Stage $k_{st}=0 \rightarrow 2$ for set cycle and $k_{st}=2 \rightarrow 0$ for reset cycle of the complete switching cycle. Let us assume that states $\mathrm{SS}_0$, $\mathrm{SS}_1$ and $\mathrm{SS}_2$ are executed for on-times of $t_0$, $t_1$ and $t_2$. However, since the switching sequence varies from one triangle to another, we need an arrangement for every triangle to order the calculated on-times $t_o$, $t_a$ and $t_b$ in desired sequence of $t_0 \rightarrow t_1 \rightarrow t_2$. There are 6 possible orders as shown in table 4.3.

| Duty-ratio | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $d_1$<br>$d_2$<br>$d_o$ | $d_a$<br>$d_b$<br>$d_o$ | $d_a$<br>$d_o$<br>$d_b$ | $d_b$<br>$d_a$<br>$d_o$ | $d_o$<br>$d_a$<br>$d_b$ | $d_b$<br>$d_o$<br>$d_a$ | $d_o$<br>$d_b$<br>$d_a$ |

Table 4.3: Possible duty-ratio orders

For each triangle in Fig. 4.3 an order is identified using tables 4.1-4.3. It is found that a triangle in odd sectors $S_1$, $S_3$, $S_5$ has same order of duty-ratios. Similarly, a triangle in even sectors $S_2$, $S_4$, $S_6$ has same order of duty-ratios. The table 4.4 summarizes the order of duty-ratios for all six sectors.

| Sector | $\triangle_0$ | $\triangle_1$ | $\triangle_2$ | $\triangle_3$ | $\triangle_4$ | $\triangle_5$ | $\triangle_6$ | $\triangle_7$ |
|---|---|---|---|---|---|---|---|---|
| $S_{1,3,5}$<br>$S_{2,4,6}$ | 4<br>6 | 5<br>3 | 6<br>4 | 1<br>2 | 1<br>2 | 2<br>1 | 4<br>6 | 3<br>5 |
| Sector | $\triangle_8$ | $\triangle_9$ | $\triangle_{10}$ | $\triangle_{11}$ | $\triangle_{12}$ | $\triangle_{13}$ | $\triangle_{14}$ | $\triangle_{15}$ |
| $S_{1,3,5}$<br>$S_{2,4,6}$ | 5<br>3 | 2<br>3 | 3<br>5 | 5<br>3 | 6<br>4 | 1<br>2 | 2<br>1 | 1<br>5 |

Table 4.4: Identified order for the complete space vector diagram

Having determined sector $S_i$, triangle $\triangle_j$ and on-times $t_0$, $t_1$, $t_2$, the implementation can be understood with the block diagram in Fig. 3.4. It has two basic units namely a processing unit and a mapping unit.

The input data to the processing unit is the magnitude and angle of the reference vector $\overrightarrow{A_0P}$. In every switching cycle, according to the proposed scheme, the processing unit determines sector number $S_i$, triangle number $\triangle_i$ and on-times $t_0$, $t_1$, $t_2$ using the magnitude and angle of the reference vector.

The memory unit has similar structure as described in chapter 3. Since, the redundant switching states have been removed from the space vector diagram by choosing only those switching state for which $|v_{NO}| \leq 1$, there is only one switching sequence for every triangle as shown in table 4.1 and 4.2. Each switching sequence essentially uses three switching states as in table 4.1 and 4.2. Therefore, a sub-block contains three switching states $SS_0$, $SS_1$ and $SS_2$. Assuming that there is one switching state at every memory location, three consecutive memory locations are required to store a switching sequence.

To this end, a 9 bit memory address is given in Fig. 4.5 to identify a memory location. It is divided into three parts, (i) 'Sector': 3 bits $SC_0 \rightarrow SC_2$, as for $S_i$, i=1$\rightarrow$6 (ii) 'Triangle': 4 bits $TR_0 \rightarrow TR_3$, as for $\triangle_j$, j=0$\rightarrow$15 (iii) 'Stage': 2 bits $ST_0 \rightarrow ST_1$, as for $k_{st}$=0$\rightarrow$2.

| $SC_2$ | $SC_1$ | $SC_0$ | $TR_3$ | $TR_2$ | $TR_1$ | $TR_0$ | $ST_1$ | $ST_0$ |
|---|---|---|---|---|---|---|---|---|

Figure 4.5: Memory address to access a memory location (switching state)

The sector number $S_i$ and triangle number $\triangle_i$ identify the correct switching sequence which is stored in the mapping unit. This switching sequence is executed for the on-times $t_0$, $t_1$, $t_2$ using corresponding switching states. The contents of a memory location are 'ON'/'OFF' condition of the power switches of the inverter which generate gating signals. For every gating signal, the interlock delay is generated using shift register. The memory required to store all the switching sequences for 5-level inverter is 768B.

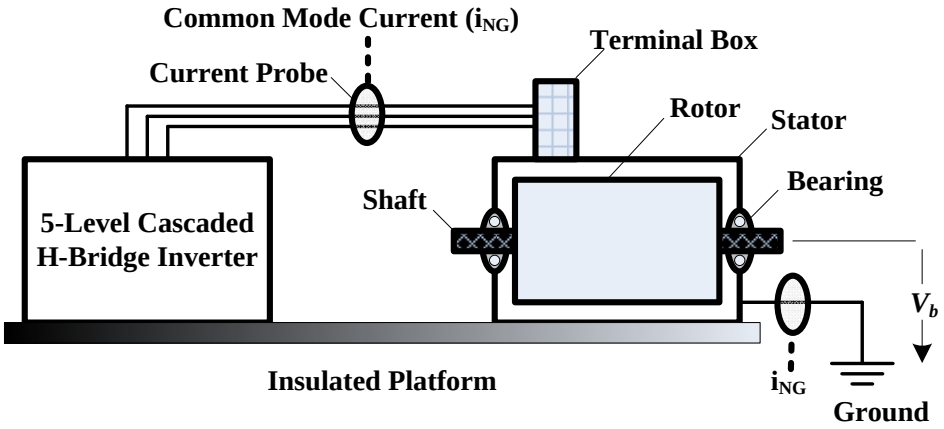



Figure 4.6: Common Mode Current ($i_{NG}$) Measurement

## 4.4 Experimental Results for 5-level Inverter

The proposed scheme can be easily implemented on a DSP microcontroller. However, for laboratory experiments an existing dSPACE DS1104 system was used. The algorithm was implemented in C.

A laboratory setup per Fig. 4.1 and Fig. 4.6 is used. A laboratory prototype of 5-level cascaded inverter is used whose each DC-link is supplied by a uncontrolled rectifier. The details of the hardware can be found in section 7.4.2. A normal (without insulated bearings) 4-pole induction motor of rating 400V and 750W under no load condition is used. The setup is placed on a insulated platform as shown in Fig. 4.6. The DC-link voltage $V_{dc(HB)}$=108V, fundamental frequency $f$=50Hz and sampling frequency $f_s$=5kHz. An interlock delay of 2$\mu$s is used and produced by the shift registers.

The experimental results include waveforms for $V_{UV}$, $V_{NO}$, voltage $V_{NG}$, volt-

age $V_b$ and current $i_{NG}$ as shown in Fig. 4.1. The stator of the motor is grounded i.e. connected to the system ground as shown in Fig. 4.6. The $V_{NO}$ is the voltage between the inverter common point $O$ and motor neutral $N$ shown in Fig. 4.1. Referring to Fig.4.1, common mode voltage $V_{NG}$ is the voltage between motor neutral and stator frame. Referring to Fig.4.1 and Fig.4.6, bearing voltage $V_b$ is measured by a voltage probe between an end of the motor shaft and the stator frame using a differential probe. The common mode current $i_{NG}$ is the sum of the motor winding currents $i_U$, $i_V$ and $i_W$, measured by putting a current probe surrounding the cable going from the inverter to the motor as shown in Fig.4.6. Since, the motor is placed on a insulated platform, the current from the motor to the ground is same as $i_{NG}$.

| Features | zero-$V_{NO}$ | Proposed |
|---|---|---|
| THD | 34% | 17.7% |
| $V_{NO}$ | 0 to 36 | 0 or 36 |
| Occurrences of $i_{NG}$ | 2173 | 1457 |
| Switching transitions | 8 or 12 | 4 or 6 |

Table 4.5: Comparison of key features in Fig. 4.7 and Fig. 4.8

The $m_i$=0.7854 is the maximum modulation index for the zero-$V_{NO}$ scheme. The experimental result for the proposed scheme is shown at $m_i$ =0.78 in Fig. 4.8 for $m_i$<0.7854 i.e. the operation in equilateral triangles. The experimental results for zero-$V_{NO}$ scheme are shown in Fig. 4.7 at $m_i$=0.78 with same experimental conditions. Table 4.5 compares the key features in these two figures. It can be observed that the line voltage waveform in the proposed method is nearly same as

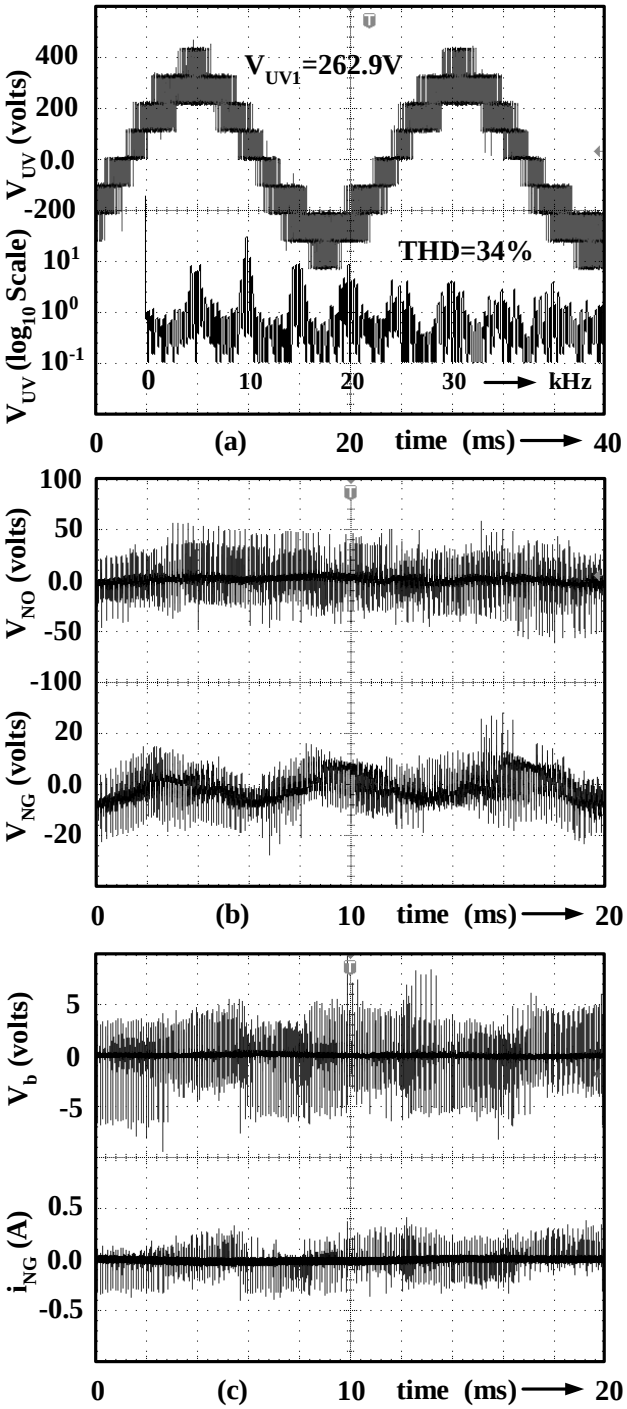



Figure 4.7: (a) Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, (b) voltage $V_{NO}$, voltage $V_{NG}$, voltage (c) $V_b$ and current $i_{NG}$ at $m_i$=0.78 for zero-$V_{NO}$ scheme.

conventional method. The measured THD for the conventional SVPWM method

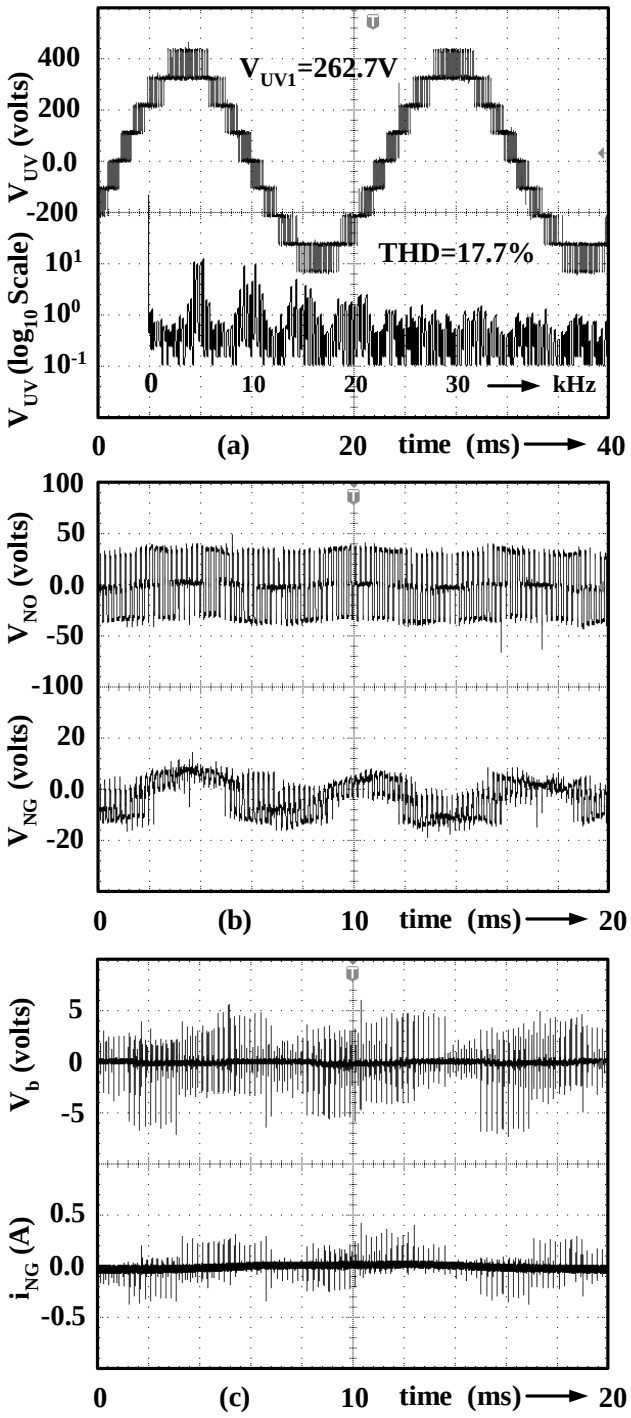



Figure 4.8: (a) Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, (b) voltage $V_{NO}$, voltage $V_{NG}$, voltage (c) $V_b$ and current $i_{NG}$ at $m_i$=0.78 for proposed scheme

is approximately 17%. The THD for the proposed scheme is approximately 17.7%,

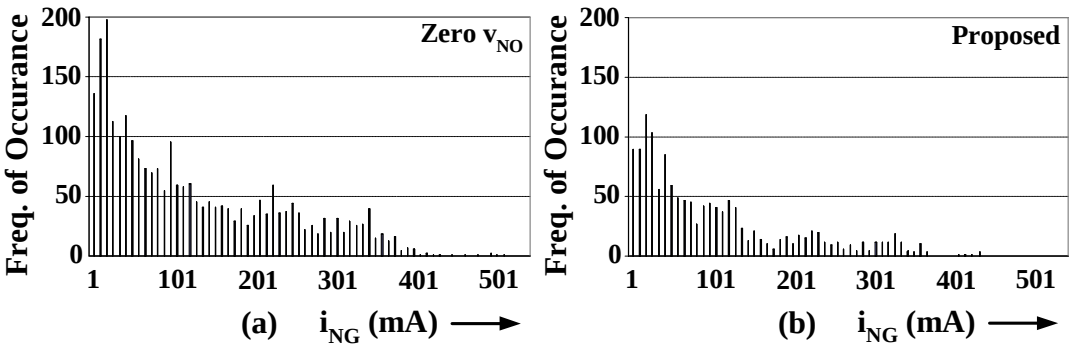



Figure 4.9: Frequency of occurrence versus current $i_{NG}$ (a) Zero $V_{NO}$ Method (b) Proposed Method at $m_i$=0.78

see Fig. 4.8(a), which is slightly higher than the conventional method. Whereas THD for the zero-$V_{NO}$ scheme is approximately 34%, see Fig. 4.7(a), which is nearly twice the conventional method. It is observed from Fig. 4.7 and Fig. 4.8 that (i) the magnitude of $V_{NO} \approx 0$ or 36V for the proposed scheme as expected, see Fig. 4.8(b) whereas the magnitude of $V_{NO} \approx 0$ to 36V for the zero-$V_{NO}$ scheme, see Fig. 4.7(b). (ii) The occurrences of $V_b$ and $i_{NG}$ spikes for proposed scheme in Fig. 4.8(c) are smaller than the zero-$V_{NO}$ scheme in Fig. 4.7(c). Fig.4.9 shows the comparison of occurrences of $i_{NG}$ for the two methods. It can be seen that the proposed scheme produces lesser number of $dV_{NG}/dt$ and hence has lesser frequency of $i_{NG}$ occurrence as compared to the zero-$V_{NO}$ scheme. The table 4.5 compares the number of occurrences of $i_{NG} > 40mA$ in Fig.4.9 counted for $50ms$. Thus, the proposed scheme reduces occurrences of $dV_b/dt$ and $i_{NG}$ without a significant increase in THD. Moreover, as mentioned in section IV, there are only four switchings for equilateral triangle and six switchings for isosceles triangle per switching cycle ($2T_s$) in the proposed method. These are nearly 50% of the switchings per switching cycle in zero-$V_{NO}$ scheme as shown in table 4.5.

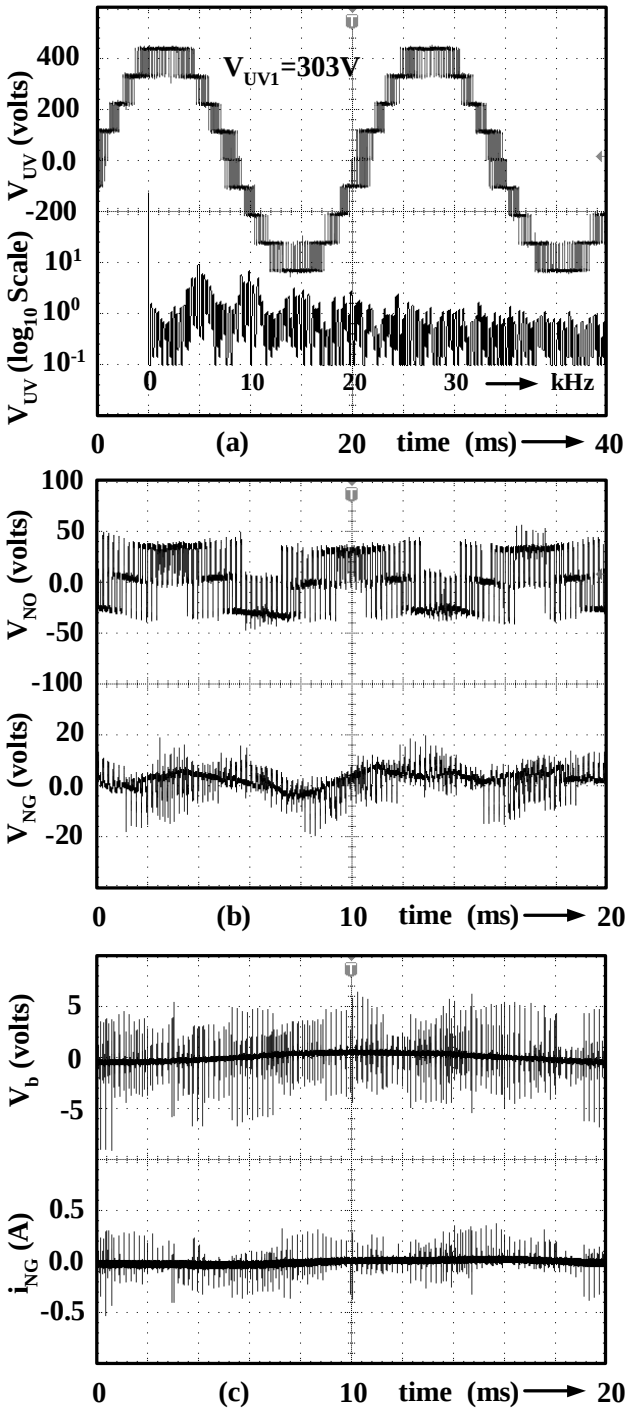



Figure 4.10: (a) Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, (b) voltage $V_{NO}$, voltage $V_{NG}$, (c) voltage $V_b$ and current $i_{NG}$ at $m_i$=0.9 for proposed scheme

For the proposed scheme, the range 0.7854 $\leq m_i <$0.907 corresponds to op-

eration in equilateral as well as in isosceles triangles. Fig. 4.10 shows results for proposed scheme at $m_i = 0.9$. It can be seen from table 4.2 that for operation in isosceles triangles $\triangle_{9a}$ and $\triangle_{15a}$, the change in $V_{NO}$ is unipolar i.e. the transitions are either only positive or only negative. In isosceles triangle for every half of the switching cycle, one of the transitions is to a non-nearest switching state e.g. in triangle $\triangle_{9a}$ the transition between $F_{13}$ (2-2-1)[-1] and $A_{11}$ (2-1-2)[-1]. Theoretically the $v_{NO}$ generated in this transition is -1. However, as explained for zero-$V_{NO}$ method, during this transition the interlock delay of the inverter leg might produce a voltage pulse of short duration which appears in the form of spike, see Fig. 4.10(b). Nevertheless, the maximum number of $dV_b/dt$ per switching cycle obtained for an isosceles triangle are less than or equal to those obtained for the equilateral triangle.

For the proposed scheme, the range $0.907 \leq m_i < 0.9163$ includes operation in overmodulation [83] region as well. Fig. 4.11 shows results for the proposed scheme at $m_i = 0.915$. In overmodulation, on the linear track $A_{11}A_{13}$, there are only two changes in $V_{NO}$ and only two state transitions per switching cycle. This leads to a further reduction in unipolar changes in $V_{NO}$. Consequently, there are reduced number of occurrences of $V_b$ and $i_{NG}$ spikes in Fig. 4.11(c) as compared to Fig. 4.10(c).

It is assumed that DC-link voltage on each H-bridge in Fig.4.1 is constant and is equal to $V_{dc(HB)}$ as shown in Fig.1.3. However, in practice all the six DC-link

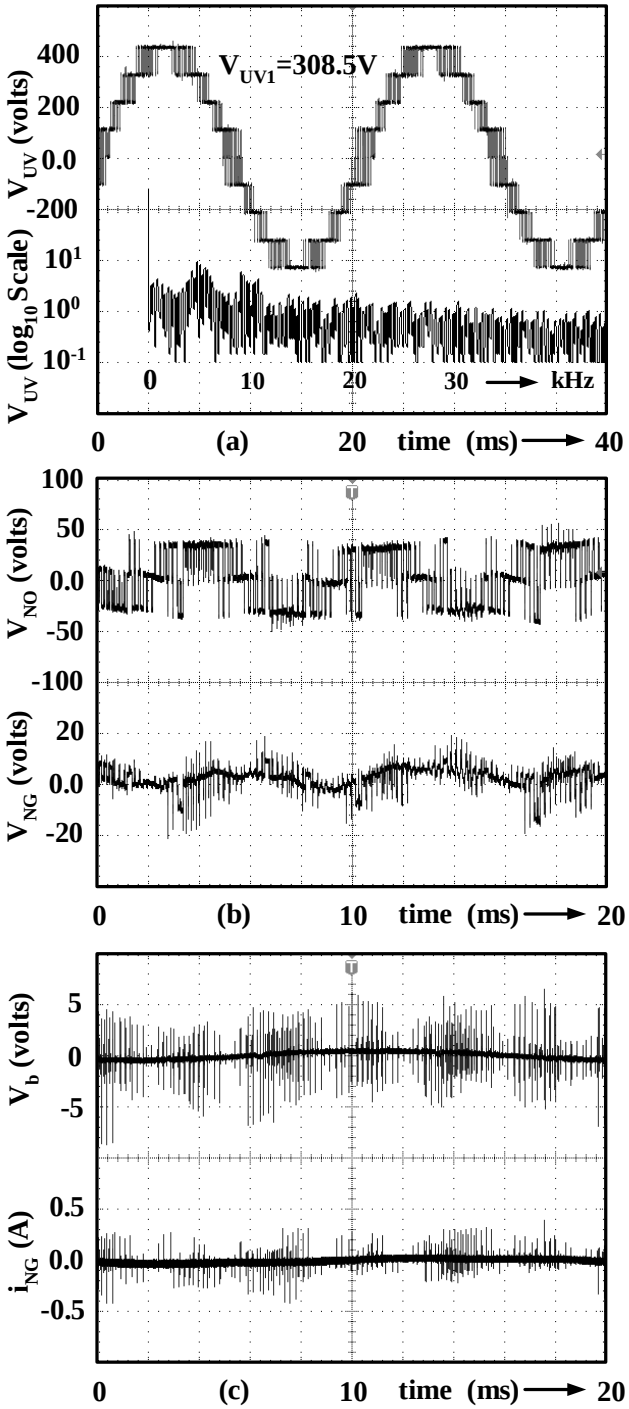



Figure 4.11: (a) Line voltage $V_{UV}$, Semi-logarithmic FFT of line voltage $V_{UV}$, (b) voltage $V_{NO}$, voltage $V_{NG}$, (c) voltage $V_b$ and current $i_{NG}$ at $m_i$=0.915 for proposed scheme

voltages are not same. Hence, the effect of difference in DC-link voltages will be

briefly discussed on common mode voltage generated in the proposed scheme. Let us assume that for the 5-level cascaded inverter in Fig. 4.1, there is an equal change of ±p% in $V_{dc(HB)}$ of all the six H-bridges. Referring to Fig. 4.3, $V_{NO}$ can vary from -$\frac{5p}{3}$%→$\frac{5p}{3}$ %. In the experiment, the maximum value of p ≈ 3%. Hence, in the proposed method, a change in $V_{NO}$ equal to 0→5 % of $V_{dc(HB)}/3$ can be expected due to difference in DC-link voltages.

## 4.5 The scheme at higher level

Let us take a 7-level cascaded inverter to explain the proposed scheme at higher level. Fig. 4.12 shows the modified space vector diagram for a 7-level with the switching states that produce $v_{NO}$= 0, ±1. The modification in the sector is carried out to exclude all corner switching states that produce $|v_{NO}| > 1$. This logic is used for other levels.

The block diagram in Fig. 3.4 in section 4.3 explains the implementation of the proposed scheme for a 5-level inverter. This block diagram can also be used to explain the implementation for 7-level ($n$-level). For 7-level ($n$-level), the requirements on the processing unit with respect to computational load and the mapping unit with respect to memory requirement are discussed below.

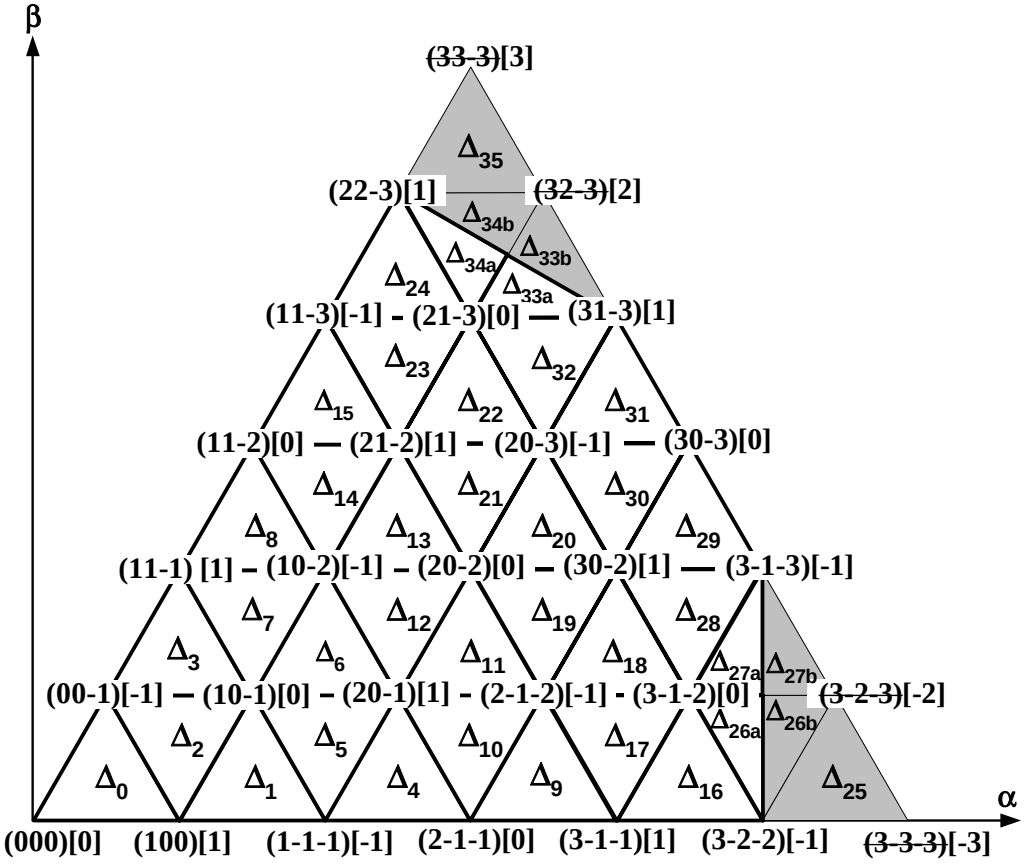



Figure 4.12: Space vector diagram of 7-level inverter with selected states

#### 4.5.0.3 Processing Unit

The processing unit determines the sector number $S_i$, triangle number $\triangle_j$ and on-times $t_0$, $t_1$, $t_2$. In chapter 2, a SVPWM scheme for multilevel inverters is proposed that is applicable to conventional space vector diagram as in Fig. 4.2, where each triangle is equilateral. Irrespective of the level $n$, the scheme in chapter 2 calculates the sector number $S_i$, triangle number $\triangle_j$ and on-times $t_0$, $t_1$, $t_2$ using the same number of computations. The same scheme is applied to the space vector diagram in Fig. 4.12 for the determination of sector & triangle, and calculation of

on-times for the equilateral triangles. However, some of the triangles are isosceles triangles e.g. in Fig. 4.12 triangles $\triangle_{26}$, $\triangle_{27}$, $\triangle_{33}$ & $\triangle_{34}$. The on-times for isosceles triangles are calculated using the set of three equations similar to (4.7) or (4.8) which are obtained through the volt-sec balance explained in section 4.3. The set of equations in (4.7) or (4.8) need only two extra $+/-$ operations as compared to set of equations (2.5)-(2.7) given in chapter 2 for equilateral triangles. Thus the computational load is almost the same as for 5-level inverter.

#### 4.5.0.4 Mapping Unit

The switching sequence for the 7-level ($n$-level) are formed similar to 5-level as shown in table I and II. With respect to block, sub-blocks and three switching states in a sub-block, the structure of mapping unit for 7-level ($n$-level) remains the same as explained in 3.4.2 for 5-level. Hence, the same explanation of mapping can be used for 7-level ($n$-level). However, the number of sub-blocks in a block are not same as in 5-level e.g. since there are 36 triangles in a sector of 7-level, there are 36 sub-blocks in every block for 7-level. Similarly, there are $(n-1)^2$ sub-blocks in a block for $n$-level. It leads to increase in the size of mapping unit. The memory required to store the switching sequences for 7, 9, 11 and 13-level is approximately 4.608kB, 6.144kB, 15.360kB and 36.864kB respectively.

Fig. 4.13 shows the simulation results for the 7-level cascaded inverter using proposed scheme at $m_i$=0.78. The $V_{dc(HB)}$ is 102V, sampling frequency is 5 kHz and

fundamental frequency is 50 Hz. The line voltage waveform Fig. 4.13(a) is similar to conventional scheme i.e. 13 levels. As expected, the $V_{NO}$ in Fig. 4.13(b) takes only three values 0, ±34V. This verifies the proposed concept. The same is used for other levels too.

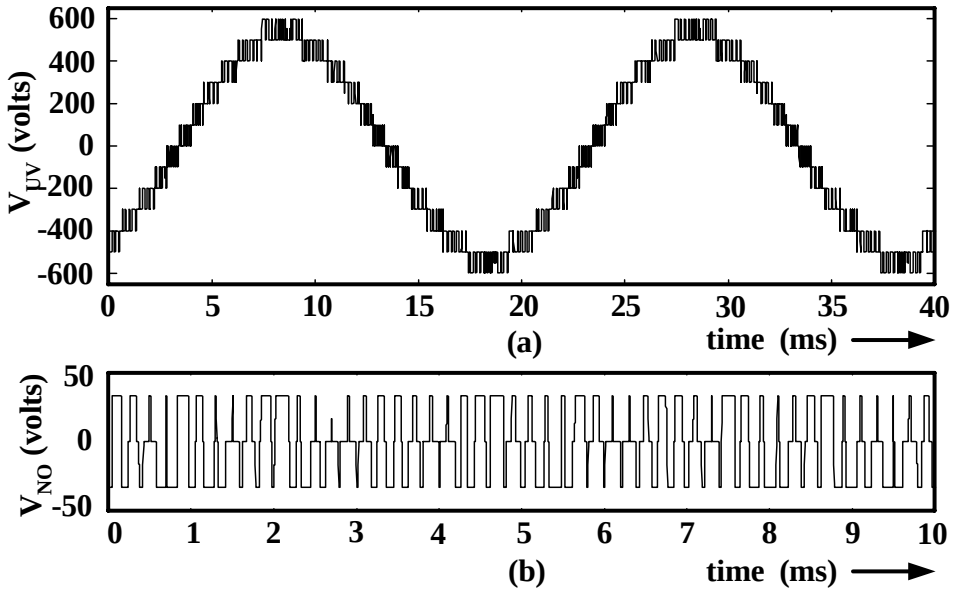



Figure 4.13: Line voltage and $V_{NO}$ for 7-level cascaded inverter at $m_i$=0.78

### 4.5.1 Normalization with respect to two-level inverter

Let us assume that the DC link voltage for a two-level inverter is $V_{dc}$. It produces a maximum fundamental voltage equal to $(2/\pi)V_{dc}$. To produce the same voltage with $n$-level cascaded H-bridge inverter, the DC link of each bridge has to be $V_{dc(HB)}$=$V_{dc}/(n-1)$. In the proposed scheme $(V_{NO(max)})_n$ is $V_{dc(HB)}/3$. Hence in terms of two-level DC link voltage $(V_{NO(max)})_n$=$V_{dc}/3(n-1)$. Whereas for two-level

inverter $(V_{NO(max)})_2 = V_{dc}/2$. Hence

$$\frac{(V_{NO(max)})_n}{(V_{NO(max)})_2} = \frac{2}{3.(n-1)} \tag{4.9}$$

For 5 and 7-level inverter, this ratio is equal to 0.167 and 0.111 respectively. Thus by increasing the number of levels $V_{NO}$ can be reduced as compared to that produced by a two-level inverter.

## 4.6 Summary

This chapter proposes a Space Vector Modulation scheme to reduce common mode voltage for cascaded multilevel inverters. Irrespective of the level $n$, the magnitude of generated $|V_{NO,\,n}|$ for that level is 0 or $V_{dc(HB,\,n)}/3$. The proposed scheme has lesser number of changes in $dV_{NG}/dt$, leading to a reduction in the number of $V_b$ and $i_{NG}$ occurrences. The scheme achieves higher modulation index as compared to other schemes while maintaining $|V_{NO,\,n}| = 0$ or $V_{dc(HB,\,n)}/3$. Due to the use of nearest three vector, the harmonic distortion is close to conventional SVPWM scheme. The number of switch commutations is lesser than conventional SVPWM for equilateral triangles and equal to conventional SVPWM scheme for isosceles triangles. The proposed scheme can be easily extended to higher levels. Since the proposed scheme is based on SVPWM, it can directly use the control variable given by the control system as mentioned in chapter 2. A commercially available DSP can implement the scheme.

# Chapter 5

# Synchronous Space Vector Modulation Based Close Loop Flux Control of a Grid Connected Cascaded Multilevel Inverter

Grid connected voltage source inverter is operated using a PWM technique. Asynchronous PWM technique for the inverter produces subharmonics and interharmonics. These harmonics can lead to the distortion of the grid voltage. Some of the consequences [74] of voltage harmonics, even for very small amplitudes, superimposed on the fundamental are; (i) torque oscillations in turbogenerators [75], (ii) AC motor aging [76], (iii) malfunctions of remote control systems [77], (iv) erroneous firing of thyristor apparatus [77], (v) lighting system flicker or display and monitor image fluctuations [78], (vi) erroneous behavior of instrumentation based on phase locked loop (PLL) [74]. Synchronous PWM can avoid the injection of sub

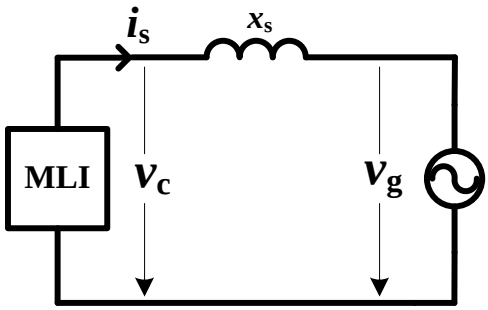



Figure 5.1: Multilevel inverter (MLI) and grid connection

and interharmonics to the grid.

Fig. 5.1 shows the simplified diagram of grid connected multilevel inverter (MLI). Main aim of this chapter is to develop a synchronous space vector PWM (SVPWM) based simple close loop flux control scheme for a grid connected cascaded H-bridge inverter. Various objective of this chapter are given below.

- Implementation of synchronous SVPWM for cascaded inverter.
- Implementation of a simple flux error based close loop scheme for a grid connected cascaded inverter. The scheme uses synchronous SVPWM.
- Propose a simple method of (a) achieving fast dynamic response, (b) ensuring synchronism during dynamic condition for the scheme mentioned above.
- Along with implementing synchronous SVPWM, exploit the redundant switching states of cascaded inverter to (a) reduce switching losses, (b) obtain waveform symmetries to improve inverter performance. Compared to other algorithms [116][132], the key focus of proposed synchronous SVPWM implemen-

tation is to use redundant switching states to improve inverter performance.

## 5.1 Introduction

It is advantageous to operate a grid connected inverter at low switching frequency to reduce the switching losses. At lower switching frequencies synchronous SVPWM can be used to avoid subharmonics and interharmonics. The close loop control using synchronous SVPWM is complex. The complexity is mainly due to implementation of synchronous SVPWM for the close loop and dynamic operation. During the dynamic condition, at low switching frequencies loss of synchronism could lead to over current. To overcome these problems, a simple scheme for the close loop flux control of a grid connected cascaded multilevel inverter is proposed in this chapter. Main features of proposed scheme are described below.

1. As mentioned before, proposed scheme is based on synchronous SVPWM. Synchronous SVPWM for cascaded H-bridge inverter is implemented using flux error [122]. The flux error is the difference of predicted flux and estimated flux [122]. Due to the use of predicted flux, there is no delay in compensating flux error. The principle of operation for the proposed scheme and its implementation for cascaded H-bridge inverter is clearly explained with necessary details and supported with experimental results.

2. In dynamic condition flux error could be significantly large. Hence, a method of obtaining fast dynamic performance is required. Moreover, as mentioned

before, during the dynamic condition, at low switching frequencies loss of synchronism could lead to problem of over current. A fast dynamic performance is ensured by applying the maximum possible DC-link voltage during the dynamic condition. A simple method is proposed to ensure synchronism in dynamic condition as well. It is explained analytically and experimentally that the volt-sec balance is maintained even in dynamic condition.

3. The redundant switching states of the multilevel inverter can be used to improve performance of the inverter. In the proposed scheme, the redundant switching states are used to reduce the switching losses and improve the harmonic performance for the inverter. Reduction of switching losses is achieved by the bus-clamping technique which is also known as discontinuous PWM. Recently, Dalessandro et.al. [132] applied discontinuous SVPWM for three-level PWM rectifiers, and discussed the importance of discontinuous SVPWM, especially the lower switching losses for the development of high power density rectifiers. In the proposed scheme, harmonic performance is improved by obtaining waveform symmetries (half wave and three phase symmetries) over a full period. Using the redundant switching states, the switching sequences are formed to obtain waveform symmetries. Hence, the proposed method of implementing synchronous SVPWM for cascaded H-bridge inverter includes both bus-clamping and waveform symmetries. It will be explained that bus-clamping and waveform symmetries are related to the formation of switching sequences, and easily achieved due to redundant

switching states. The synchronous SVPWM is applied for 3-level NPC inverter in [79] but it does not include bus-clamping. The bus clamping for a 3-level inverter has been proposed in [116]. As compared to these approaches, the proposed implementation uses redundant switching states to form switching sequences in such a way that along with obtaining waveform symmetries, there are minimal switchings while transiting from one triangle to the other. The proposed idea can be easily extended to higher level.

4. The proposed close loop scheme uses space vector PWM algorithm discussed in chapter 2 and 3. Flux error is equal to volt-secs. The switching frequency is constant in the proposed method. Hence, for a given flux error, sector $S_i$, triangle $\Delta_j$ and on-times are calculated on-line in every sampling period using the algorithm proposed in chapter 2 and 3. Switching sequence is mapped into a simple lookup table with respect to $S_i$ and $\Delta_j$. Hence, the switching sequence can be retrieved from this table using $S_i$ and $\Delta_j$. This shows that in proposed close loop scheme, SVPWM is implemented with the same simplicity as discussed in chapter 2 and 3. Due to the simple structure of the scheme, it can be easily implemented on a commercial DSP.

The usefulness of the scheme is discussed and demonstrated through analysis and experiments. Experimental results are shown for a laboratory prototype of cascaded 5-level inverter, see Fig. 1.3.

Next section briefly explains principle of flux error based SVPWM. In section 5.3, the proposed close loop scheme is discussed. Section 5.4 explains the technique used to obtain fast dynamic performance of the close loop scheme. Section 5.5 explains the implementation of synchronous SVPWM for multilevel inverter using bus-clamping technique and waveform symmetries. In section 5.6, the experimental results are discussed and analyzed. Section 5.7 summarizes the chapter.

## 5.2 Principle of Flux Error Based SVPWM

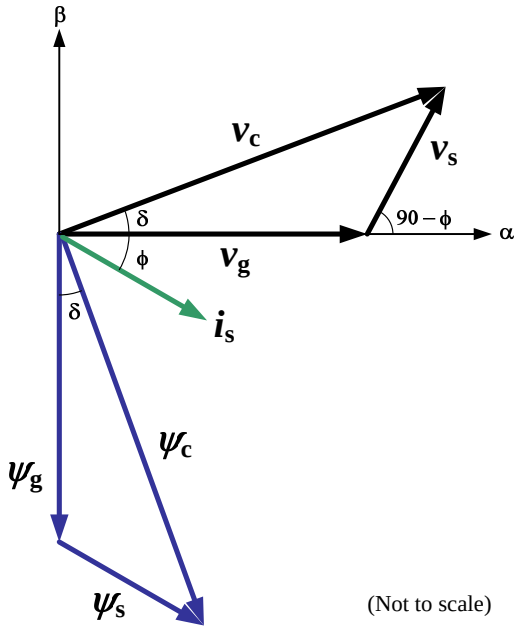



Figure 5.2: The phasor diagram for grid connected multilevel inverter in Fig. 5.1

The phasor diagram in Fig. 5.2 is drawn for the grid connected multilevel inverter shown in Fig. 5.1. In Fig. 5.2, subscript 'g' stand for grid, 'c' stands for multilevel inverter and 's' stands for synchronous reactance. In steady state, the

relationship between the voltage vectors $\boldsymbol{v_c}$, $\boldsymbol{v_g}$ and $\boldsymbol{v_s}$ can be written as,

$$\boldsymbol{v_c} = \boldsymbol{v_g} + \boldsymbol{v_s} = \boldsymbol{v_g} + \boldsymbol{i_s} x_s \tag{5.1}$$

In the phasor diagram in Fig. 5.2, the grid voltage $\boldsymbol{v_g}$ is along the $\alpha$-axis. The fundamental component of output voltage $\boldsymbol{v_c}$ produced by multilevel inverter makes angle $\delta$ with the $\alpha$-axis. The current $\boldsymbol{i_s}$ through the synchronous reactance $x_s$ is at a lagging angle $\phi$. The voltage across $x_s$ is $\boldsymbol{v_s}$ and given as $\boldsymbol{i_s} x_s$.

From (5.1), $\boldsymbol{v_c}$ depends on $\boldsymbol{v_g}$ and $\boldsymbol{v_s}$. For a grid connected system, $\boldsymbol{v_g}$ can be obtained through grid voltage measurement but $\boldsymbol{v_s}$ will change with a change in current $\boldsymbol{i_s}$ passing through $x_s$, see Fig. 5.1. Nevertheless, for any change in $\boldsymbol{v_s}$, $\boldsymbol{v_c}$ changes its magnitude $|\boldsymbol{v_c}|$ and angle $\delta$ to ensure relationship in (5.1). Multilevel inverter produces the required $\boldsymbol{v_c}$. With this the principle of flux error based SVPWM can be explained as follows.

The faraday's law states that $\boldsymbol{v}=d\boldsymbol{\psi}/dt$, in the discrete time, the expression $\boldsymbol{v}=d\boldsymbol{\psi}/dt$ can be written as $\Delta\boldsymbol{\psi}=\boldsymbol{v}\Delta t$ i.e. the flux change $\Delta\boldsymbol{\psi}$ in flux $\boldsymbol{\psi}$ can be achieved by holding the voltage vector $\boldsymbol{v}$ for the small time period $\Delta t$ which is equivalent to switching period $\tau_s$. For flux based SVPWM implementation $\Delta\boldsymbol{\psi_c}$ can taken as flux error because it is the difference of reference and estimated flux [122]. In terms of inverter flux error $\Delta\boldsymbol{\psi_c}$, voltage vector $\boldsymbol{v_c}$ and switching period $\tau_s$, the volt-sec balance can be written as,

$$\Delta\boldsymbol{\psi_c} = \boldsymbol{v_c}\tau_s = \boldsymbol{v}_{A_o}.t_{A_o} + \boldsymbol{v}_{A_a}.t_{A_a} + \boldsymbol{v}_{A_b}.t_{A_b} \tag{5.2}$$

In (5.2), (i) $\boldsymbol{v}_{A_o}$, $\boldsymbol{v}_{A_a}$ and $\boldsymbol{v}_{A_b}$ are voltage vectors corresponding to three vertices of the triangle in the space vector diagram where the tip of the $\boldsymbol{v_c}$ is located, (ii) $t_{A_o}$, $t_{A_a}$ and $t_{A_b}$ are respective on-times where $t_{A_o}+t_{A_a}+t_{A_b}=\tau_s$.

Equation (5.2) essentially describes the principle of flux error based space vector PWM i.e. the flux error $\Delta\boldsymbol{\psi_c}(k)$ is compensated by applying voltage vector $\boldsymbol{v_c}(k)$ for $\tau_s$ time. Using this principle the proposed close loop scheme is explained below.

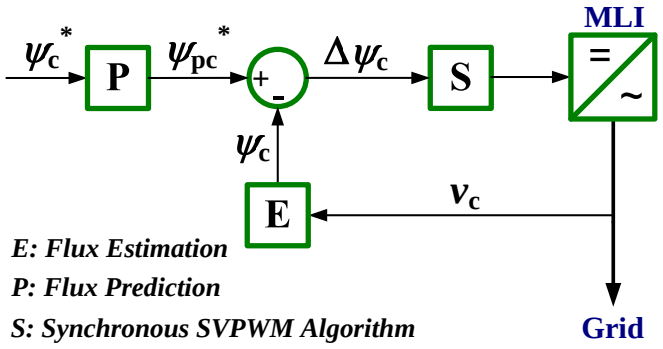



Figure 5.3: The block diagram for predictive flux vector based close loop scheme

## 5.3 Proposed Close Loop Scheme

In the proposed scheme, flux error $\Delta\boldsymbol{\psi_c}$ is used to implement space vector PWM. The flux error $\Delta\boldsymbol{\psi_c}$ is the difference of reference flux $\boldsymbol{\psi}_c^*$ and actual (estimated) flux $\boldsymbol{\psi}_c$ i.e. $\Delta\boldsymbol{\psi_c}=\boldsymbol{\psi}_c^*-\boldsymbol{\psi}_c$. Fig. 5.3 shows the basic structure of the proposed close loop scheme which essentially forms the innermost loop for the grid inverter control scheme. The 'MLI' stands for Multilevel Inverter which is 5-level cascaded H-bridge inverter shown in Fig. 1.3. Blocks 'S', 'E' and 'P' in Fig. 5.3 are described

below.

### 5.3.1 Block 'S': Synchronous SVPWM

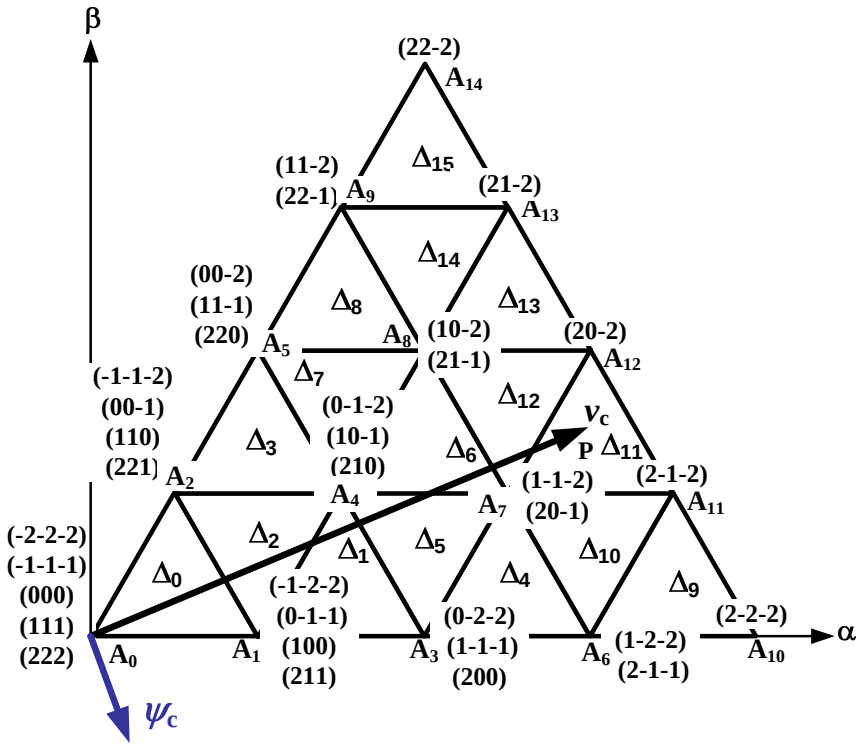



Figure 5.4: The first sector of the space vector diagram

The (5.2) at $k^{th}$ instant can be written as,

$$\Delta\boldsymbol{\psi_c}(k) = \boldsymbol{v_c}(k)\tau_s = \boldsymbol{v}_{A_o}(k).t_{A_o}(k) + \boldsymbol{v}_{A_a}(k).t_{A_a}(k) + \boldsymbol{v}_{A_b}(k).t_{A_b}(k) \tag{5.3}$$

Flux error $\Delta\boldsymbol{\psi_c}(k)$ is compensated by applying three nearest vectors $\boldsymbol{v}_{A_o}(k)$, $\boldsymbol{v}_{A_a}(k)$ and $\boldsymbol{v}_{A_b}(k)$ for their respective on-times $t_{A_o}(k)$, $t_{A_a}(k)$ and $t_{A_b}(k)$. For example, for the voltage vector $\boldsymbol{v_c}$ shown in space vector diagram in Fig. 5.4, the tip P of the voltage $\boldsymbol{v_c}$ is located in triangle $\Delta_{11}$. The volt-second balance equation

for this triangle can be written as,

$$\boldsymbol{v_c}\tau_s = \boldsymbol{v}_{A_7}.t_{A_7} + \boldsymbol{v}_{A_{11}}.t_{A_{11}} + \boldsymbol{v}_{A_{12}}.t_{A_{12}} \tag{5.4}$$

Flux error $\Delta\boldsymbol{\psi_c}(k)$ is equivalent to volt-sec balance $\boldsymbol{v_c}(k)\tau_s$ given by (5.4). Chapter 2 and 3 explain the algorithm to obtain sector, triangle and on-times for a given voltage vector $\boldsymbol{v_c}(k)$ at a switching period $\tau_s$ to implement SVPWM.

For a given flux error $\Delta\boldsymbol{\psi_c}(k)$, block 'S' in Fig. 5.3 implements synchronous SVPWM using the algorithms explained in chapter 2 (linear range) and 3 (over-modulation range). The input to the block 'S' is flux error $\Delta\boldsymbol{\psi_c}(k)$, and output is the PWM signals for the power switches of the inverter. Using $\Delta\boldsymbol{\psi_c}(k)$, the sector number, triangle number and on-times are determined. Subsequently, by identifying the appropriate switching sequence and applying its switching states, the PWM signals for the power switches of the multilevel inverter are generated.

Since, the flux error $\Delta\boldsymbol{\psi_c}(k)$ at a given instant is the difference of reference flux and actual flux, and the actual flux is estimated from the measured output voltage, it will be useful to discuss the method used for flux estimation.

### 5.3.2 Block 'E': Estimation of Flux $\boldsymbol{\psi}_c$

Mathematically, the flux estimation can be given as $\boldsymbol{\psi} = \int \boldsymbol{v}dt$ i.e. obtained by integrating the measured voltage. However, in practical situations pure integrator cannot be used due to dc offset in measured voltage which leads to problem

of integrator saturation [133]. To address this problem, a simple flux estimation model is used in this work which is given by Luomi [134]. Luomi [134] cascades a first order low pass filter with a first order high pass filter to deal with this problem. For power application, this model can be written as,

$$\boldsymbol{\psi} = \int \{(1 - j\chi\omega_s)\boldsymbol{v} - \chi\omega_s\boldsymbol{\psi}\}dt \tag{5.5}$$

This can be considered as a simple model as only one tuning parameter $\chi$ is required. The model behaves as pure integrator when $\chi$=0.0 which is the ideal situation. In practical situations, $\chi$ should be in the range of 0.1 to 0.5. However, $\chi$ should be as small as possible to have a better dynamic response [134].

In the absence of block 'P' in Fig. 5.3, the flux error $\Delta\boldsymbol{\psi_c}$ is the difference of reference flux $\boldsymbol{\psi_c}^*$ and actual flux $\boldsymbol{\psi_c}$ i.e. $\Delta\boldsymbol{\psi_c}$=$\boldsymbol{\psi_c}^*$-$\boldsymbol{\psi_c}$. In $k^{th}$ switching cycle, the flux error $\Delta\boldsymbol{\psi_c}(k)$ is given as $\Delta\boldsymbol{\psi_c}(k)$=$\boldsymbol{\psi_c}^*(k)$-$\boldsymbol{\psi_c}(k)$. This essentially means that the flux error $\Delta\boldsymbol{\psi_c}(k)$ or the volt-sec computed in $k^{th}$ cycle can only be compensated in $(k+1)^{th}$ cycle. As a result the actual flux in $k^{th}$ cycle will be,

$$\boldsymbol{\psi_c}(k) = \boldsymbol{\psi_c^*}(k-1) \tag{5.6}$$

Fig. 5.5 shows the instants where reference flux vector $\boldsymbol{\psi_c}^*$ is sampled for one fundamental cycle. For this figure, (a) fundamental period is 20ms corresponding to fundamental frequency of 50Hz (b) sampling period $\tau_s$=555.55$\mu$s corresponding to sampling frequency of 1.8kHz. To obtain synchronism, $\boldsymbol{\psi_c}^*$ is sampled at the instants 1→36 shown in the figure in every fundamental cycle. The thick arrow

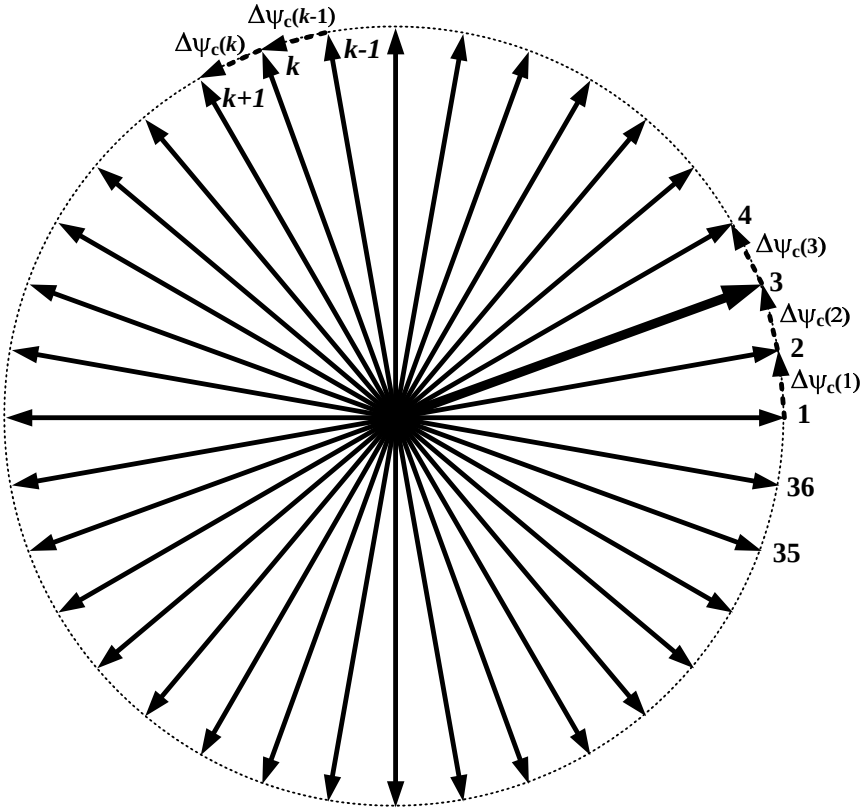



Figure 5.5: Sampling instants for non-predictive flux scheme at $\tau_s$=555.55$\mu$s

in Fig. 5.5 shows reference flux for current switching cycle i.e. $\boldsymbol{\psi}_c{}^*(3)$. Flux error $\Delta\boldsymbol{\psi_c}(3)$ computed in the $3^{rd}$ switching cycle is shown by small dotted arrow in the figure and is given as $\Delta\boldsymbol{\psi_c}(3)$=$\boldsymbol{\psi}_c{}^*(3)$-$\boldsymbol{\psi}_c(3)$. This flux error $\Delta\boldsymbol{\psi_c}(3)$ can only be compensated in $4^{th}$ cycle. The same is true for any other cycle.

Hence, as shown in Fig. 5.5, in non-predictive flux scheme the actual flux $\boldsymbol{\psi_c}(k)$ lags behind the reference flux $\boldsymbol{\psi_c^*}(k)$ by one switching cycle. To mitigate this error, the technique of flux prediction used by [122] is explained below.

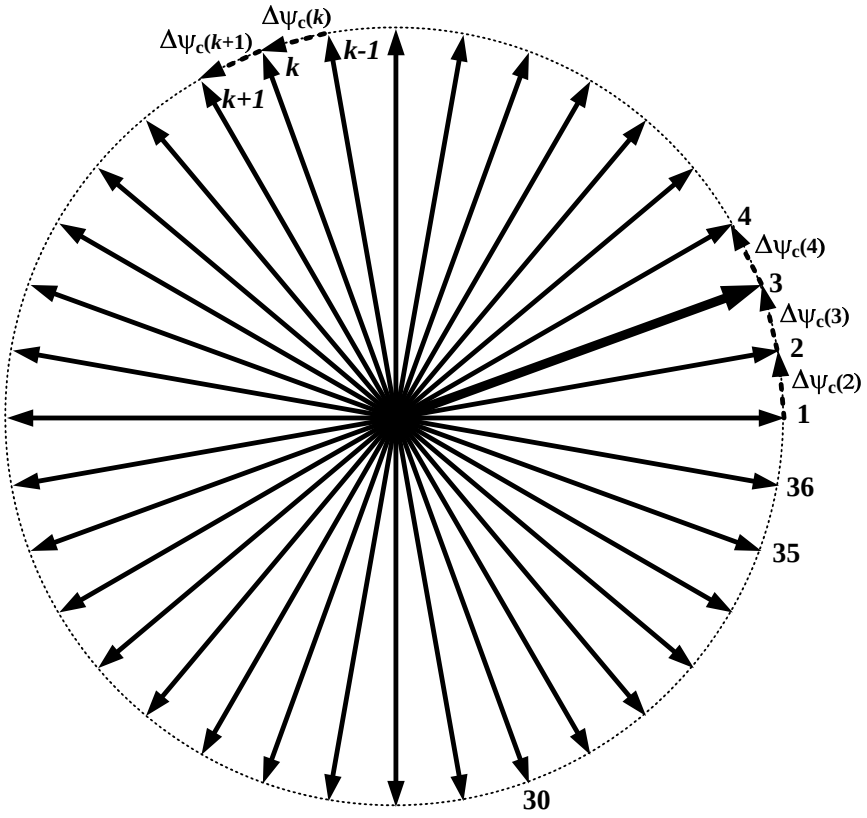



Figure 5.6: Sampling instants for predictive flux scheme at $\tau_s$=555.55$\mu$s

### 5.3.3 Block 'P': Prediction of Flux $\psi_{pc}{}^*$

In polar form, the reference flux $\boldsymbol{\psi_c^*}(k)$ can be written as

$$\boldsymbol{\psi_c^*}(k) = |\boldsymbol{\psi_c^*}(k)|e^{j\theta^*(k)} \tag{5.7}$$

In (5.7), $|\boldsymbol{\psi_c^*}(k)|$ is the magnitude and $\theta^*(k)$ is the angle of $\boldsymbol{\psi_c^*}(k)$. Due to constant angular velocity, in steady state, $\theta^*(k)$ changes by $\omega_s\tau_s$ from cycle to cycle but $|\boldsymbol{\psi_c^*}(k)|$ remains constant e.g. in Fig. 5.6, the magnitude of $\Delta\boldsymbol{\psi_c}(k)$ is the same for any switching cycle in steady state but the angle changes by $\omega_s\tau_s$ (=$10^o$) in subsequent switching cycle. Based on this fact, in the $k^{th}$ cycle, the magnitude and

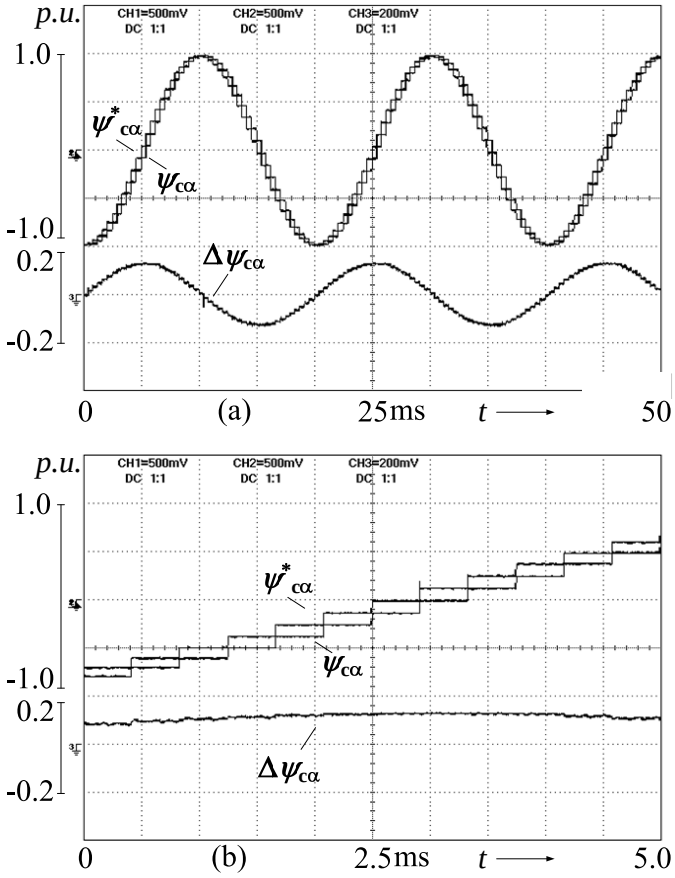



Figure 5.7: The $\alpha$ component of predicted converter flux $\boldsymbol{\psi^*_{c\alpha}}$, actual converter flux $\boldsymbol{\psi_{c\alpha}}$ and flux error $\Delta\boldsymbol{\psi_{c\alpha}}$ at $\boldsymbol{\psi_c} = 1.0\,p.u.$ and $\delta = 45^o$

angle of the predicted flux $\boldsymbol{\psi^*_{pc}}(k)$ for the next cycle will be $|\boldsymbol{\psi^*_c}(k)|$ and $\theta^*(k)+\omega_s\tau_s$ respectively. Therefore in polar form, the $\boldsymbol{\psi^*_{pc}}(k)$ will be,

$$\boldsymbol{\psi^*_{pc}}(k) = |\boldsymbol{\psi^*_c}(k)|e^{j(\theta^*(k)+\omega_s\tau_s)} = \boldsymbol{\psi^*_c}(k)e^{j\omega_s\tau_s} = \boldsymbol{\psi^*_c}(k+1) \tag{5.8}$$

Since at a given instant both $\omega_s$ and $\tau_s$ are constant, the $e^{j\omega_s\tau_s}$ is also a constant. This leads to a simplicity in prediction of flux for the next switching cycle. The block 'P' in Fig. 5.3 carries out the flux prediction given by (5.8). The flux error $\Delta\boldsymbol{\psi_c}(k)$ computed in $k^{th}$ sampling cycle is given as,

$$\Delta\boldsymbol{\psi_c}(k) = \boldsymbol{\psi^*_{pc}}(k) - \boldsymbol{\psi_c}(k) = \boldsymbol{\psi^*_c}(k+1) - \boldsymbol{\psi_c}(k) \tag{5.9}$$

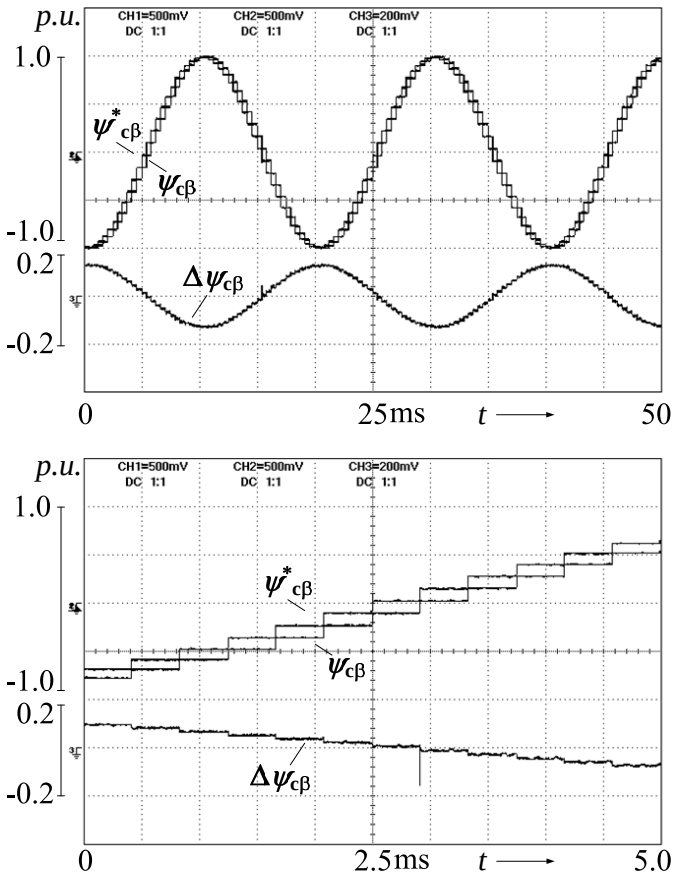



Figure 5.8: The $\beta$ component of predicted converter flux, actual converter flux and their difference at $v_c$=1.0 p.u. and $\delta$=45$^o$

The (5.9) shows that the flux error to be compensated in $(k+1)^{th}$ cycle is calculated in $k^{th}$ cycle e.g. flux error to be compensated in $4^{th}$ cycle is calculated in $3^{rd}$ cycle. This leads to removal of phase lag error of one cycle as discussed earlier.

Fig. 5.7 shows the $\alpha$ component of the predicted converter flux $\boldsymbol{\psi^*_{c\alpha}}$, actual converter flux $\boldsymbol{\psi_{c\alpha}}$ and flux error $\boldsymbol{\Delta\psi_{c\alpha}}$ at $\boldsymbol{\psi_c} = 1.0\,p.u.$ and $\delta = 45^o$. The central part of Fig. 5.7(a) is ten times horizontally magnified in Fig. 5.7(b). Note that in Fig. 5.7(b) the $\boldsymbol{\psi^*_{c\alpha}}$ is one cycle ahead of $\boldsymbol{\psi_{c\alpha}}$.

Fig. 5.8 shows the $\beta$ component of the predicted converter flux $\boldsymbol{\psi^*_{c\beta}}$, actual

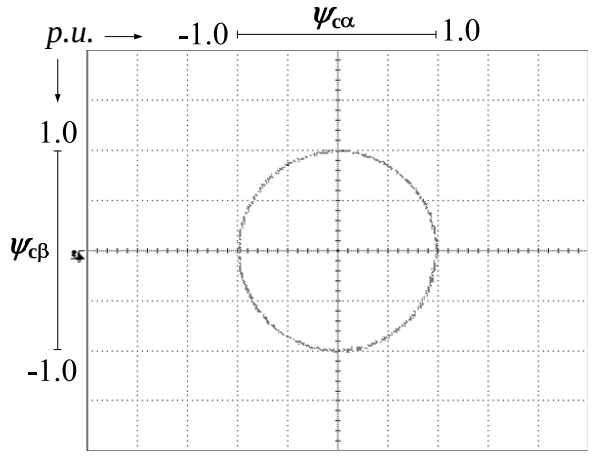



Figure 5.9: The $\psi_{c\alpha}$ vs. $\psi_{c\beta}$ at $v_c$=1.0 p.u. and $\delta$=45$^o$

converter flux $\boldsymbol{\psi_{c\beta}}$ and flux error $\Delta\boldsymbol{\psi_{c\beta}}$ at $\boldsymbol{\psi_c} = 1.0p.u.$ and $\delta = 45^o$. Fig. 5.8 can be explained similar to Fig. 5.7. In Fig. 5.9, the $\boldsymbol{\psi_{c\beta}}$ is plotted against $\boldsymbol{\psi_{c\alpha}}$ on cartesian plane, it is circle of unity radii as expected.

## 5.4 Control of Flux Error for the Large Error

In the steady state while applying the PWM signals for the present switching cycles the duty ratio for the next switching cycles are calculated using the flux error. The flux prediction helps to avoid one cycle delay in this process. In steady state it can be assumed that there is no change in the flux reference vector i.e. the magnitude of $\boldsymbol{\psi_c^*}$ is constant, and the angle of $\boldsymbol{\psi_c^*}$ is increased by $\omega_s\tau_s$ every sampling period to implement space vector PWM.

The flux reference vector $\boldsymbol{\psi_c^*}$ can suddenly change due to, (1) sudden change in active/reactive power demand from the grid, (2) sudden change in the grid voltage.

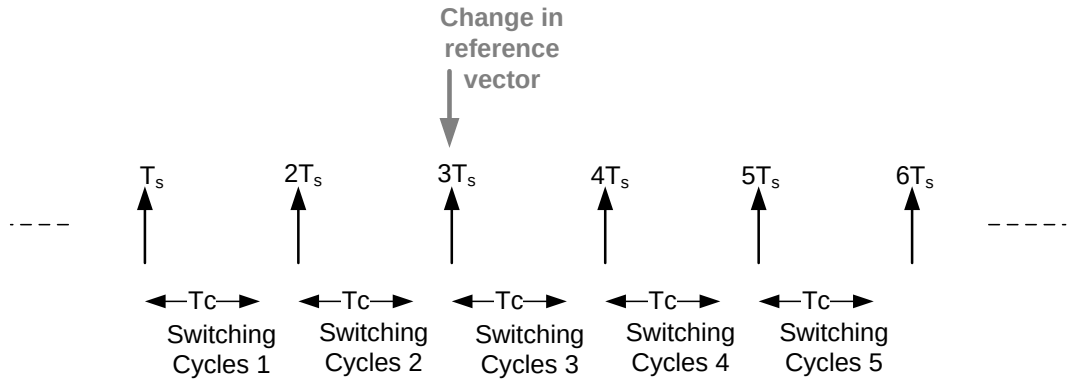



Figure 5.10: Change in reference vector at one of the sampling instant

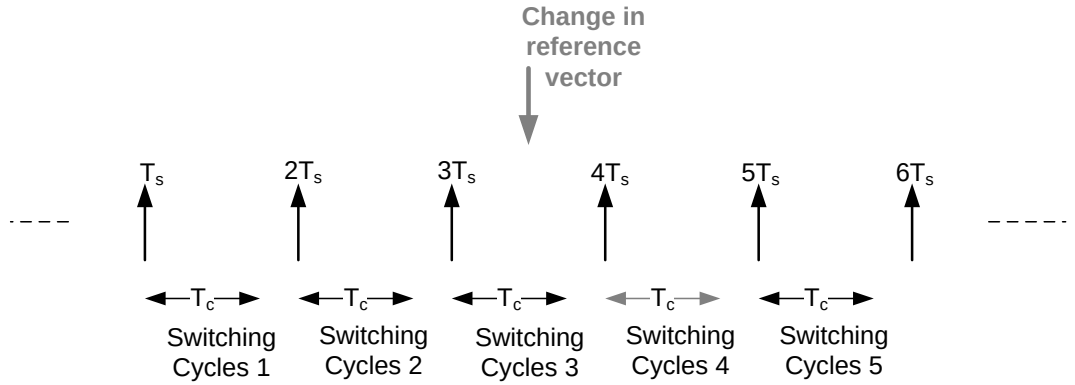



Figure 5.11: Change in reference vector in between two sampling instants

This condition is known as dynamic condition. The dynamic condition can happen anytime i.e. at the sampling instant, see Fig.5.10 or in between two sampling instants while applying the PWM pulses, see Fig.5.11. Fig.5.10 and Fig.5.11 are used to explain the effect of change in reference vector at a given instant. In these figures, $T_s$ is the sampling period and $T_c$ is the computation time to implement the algorithm and obtain the duty ratios for the next switching period. These figures show only 5 switching cycles and for the sake of simplicity it is assumed that these switching cycles start at $T_s$, $2T_s$, $3T_s$, $4T_s$ and $5T_s$ respectively.

In Fig.5.10, the change in flux reference vector takes place at $3T_s$. The computations in switching cycle 3 are done according to the changed flux reference vector. Hence, the duty ratio calculated in switching cycle 3 are also according to changed flux reference vector. In Fig.5.11, the change in flux reference vector takes place between $3T_s$ and $4T_s$ while operating in switching cycle 3. The computation done in switching cycle 3 will not be able to capture this change. This is true for any sampled data system. The computations done in switching cycle 4 will capture change in flux reference vector and the duty ratios calculated in switching cycle 4 are according to the changed reference vector. Hence, if the reference vector changes in between a switching cycle between two switching instants there will be a delay in capturing this change. This delay is inherent to the sampled data systems. Though this delay is less than $T_s$ but if $T_s$ is large, it is possible that the current error can also be large. However, this problem is less severe for a multilevel inverter as compared to two-level inverter as explained below.

For a $n$-level inverter, the switching frequency is $1/(n-1)$ times the switching frequency of a two-level inverter [8]. For a two-level inverter switching at $f_{sw}$ frequency, the sampling has to be done at $f_{sw}$. However, for a 5-level inverter switching at $f_{sw}$, the sampling can be done at $4f_{sw}$ frequency and for a $n$-level inverter the sampling can be done at $(n-1)f_{sw}$ frequency. Hence, compared to two-level inverter for a multilevel inverter switching at very low switching frequency the effective $T_s$ is significantly low as $T_s$=$1/(n-1)f_{sw}$. Hence, applying the proposed technique on a multilevel inverter significantly reduces the chances of over

current. This benefit can be further enhanced with the use of bus-clamping as with the bus clamping technique the switching frequency is reduced by 1/3. Using the bus-clamping technique for a 5-level inverter, a power semiconductor device switching at 450Hz, the sampling can be done at 2700Hz. To generalize, if the bus-clamping is applied on a $n$-level inverter the effective sampling period can be given as $T_s$=$1/1.5(n-1)f_{sw}$. Which shows that by applying the proposed technique on multilevel inverters with bus-clamping technique the chances of over current can be significantly reduced. Considering these advantages, still the design challenge is proper selection of switching frequency of power devices and sampling frequency for a given multilevel inverter so that current limit is not hit under any dynamic condition.

Take note that, (1) the flux error calculation and remaining calculation is same whether the reference flux changes at the switching instant or in between the switching instants. (2) it is flux error rather than the flux vector that is used for the generation of synchronous PWM. After a change in reference vector the flux error is computed (in the same or next switching cycle) and applied to produce appropriate dynamic response and contribute towards restoring synchronism. (3) the duty ratio computed in one switching cycle can only be applied in next switching cycle as PWM signal for the converter. The PWM signals can not change until the switching cycle is over.

For the dynamic condition illustrated in Fig. 5.12(a), the reference vector

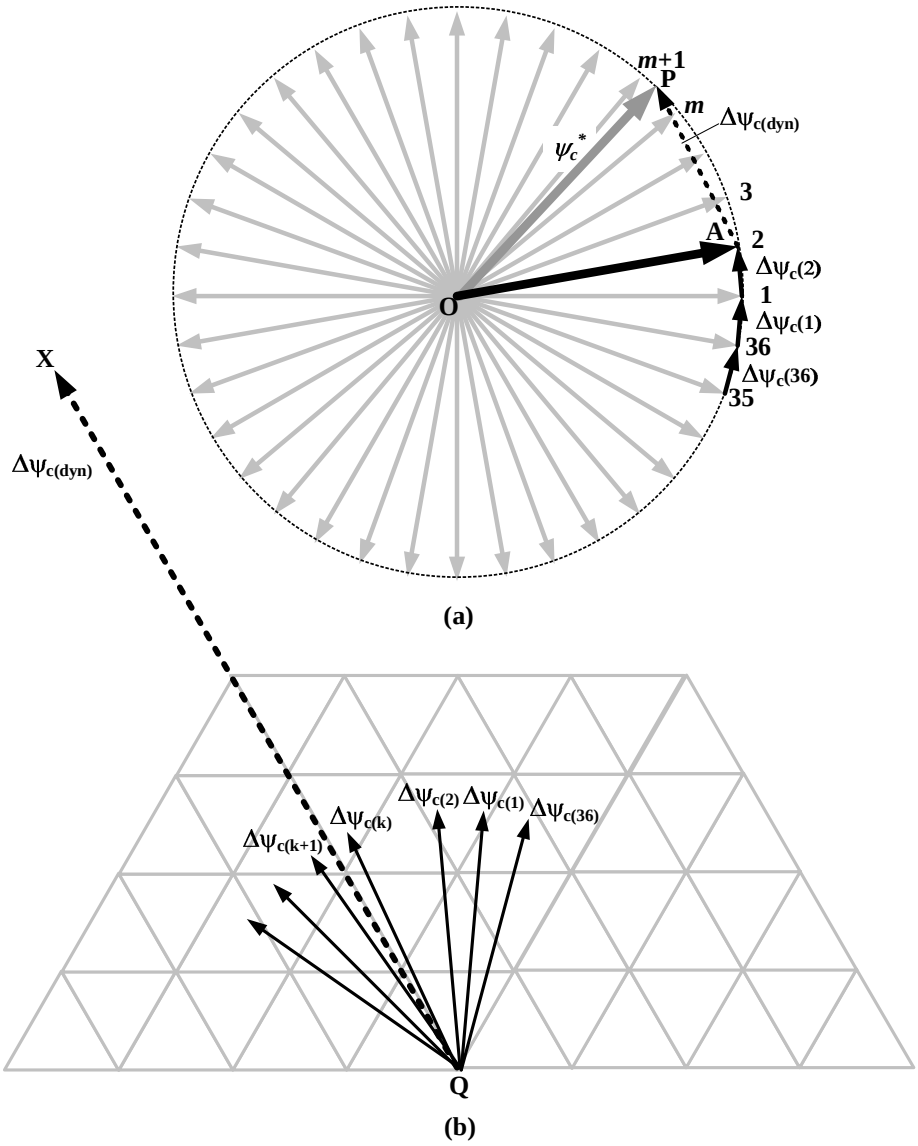



Figure 5.12: Dynamics for the proposed scheme at $\tau_s$=555.55$\mu$s

$\boldsymbol{\psi_c^*}$ is moving at angular speed $\omega_s$ and is being sampled at sampling period $\tau_s$ which means $\boldsymbol{\psi_c^*}$ is sampled after every $\omega_s\tau_s$ angular displacement corresponding to sampling instants 1→36 shown by the gray arrows which are essentially the switching angles at which the flux error is compensated. In Fig. 5.12(a), in steady state, due to flux prediction, $\Delta\boldsymbol{\psi_{c(2)}}$ is calculated while $\Delta\boldsymbol{\psi_{c(1)}}$ is applied, the

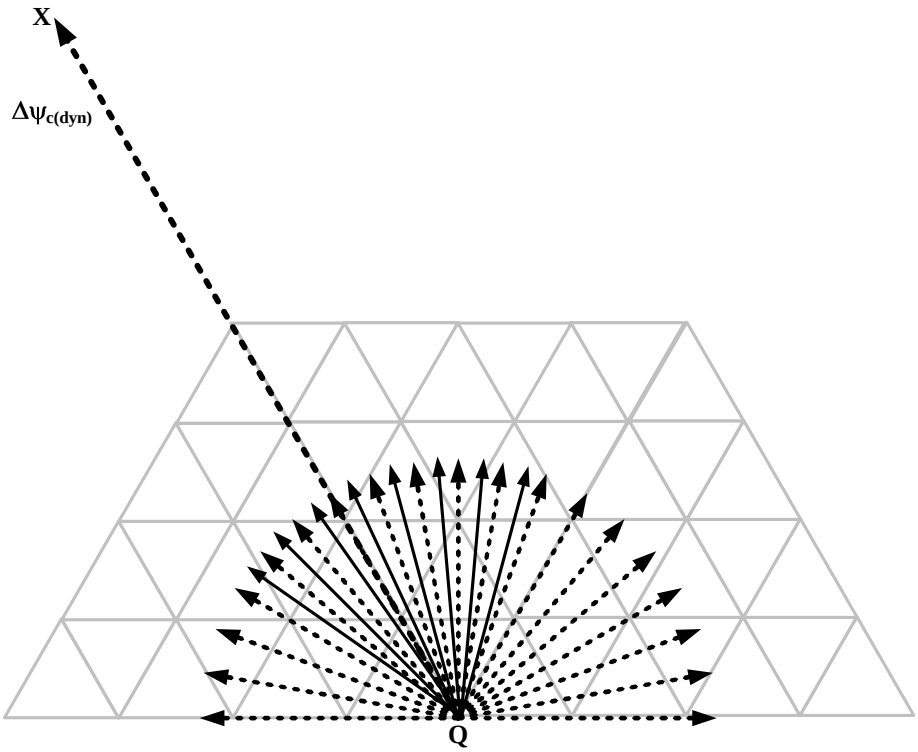



Figure 5.13: New discrete instants for the proposed scheme at $\tau_s$=555.55$\mu$s

reference vector is represented by $\overrightarrow{OA}$. In Fig. 5.12(a), while applying $\Delta\boldsymbol{\psi_{c(1)}}$ there is a dynamic condition due to change in $\boldsymbol{\psi_c^*}$. The new reference vector is shown by solid gray arrow $\overrightarrow{OP}$. Due to change in $\boldsymbol{\psi_c^*}$, the actual flux error is represented by $\Delta\boldsymbol{\psi_{c(dyn)}}$ rather than predicted flux error $\Delta\boldsymbol{\psi_{c(2)}}$, see Fig. 5.12(a). Depending on the instant of changing the reference vector, the changed reference vector will be used in the calculation of flux error and duty ratio in the same or next switching cycle as described before. The flux error $\Delta\boldsymbol{\psi_{c(dyn)}}$ is calculated using converter reference flux and observed converter flux. Actual flux error $\Delta\boldsymbol{\psi_{c(dyn)}}$ is shown by dotted arrow in Fig. 5.12(a). The flux error in dynamic condition $\Delta\boldsymbol{\psi_{c(dyn)}}$ is significantly larger than predicted $\Delta\boldsymbol{\psi_{c(2)}}$ in steady state condition and can

not be compensated in one switching cycle. Fig. 5.12(b) shows the space vector diagram where the flux error is compensated along the switching vectors shown by the solid arrows in the steady state i.e. before the dynamics. Take note that in steady state the flux error is compensated along these switching vectors in every fundamental cycle which is characteristics of synchronous PWM. However, as seen from Fig. 5.12(b) that the flux error $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ is not only significantly large but also it does not coincide with any switching vectors/solid arrows. An effort to align the flux error in dynamic condition $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ to one of the previous synchronous switching vectors will lead to significant volt-sec error. Moreover, uncertainty in providing appropriate flux error compensation for this large $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ leads to the problem of over current especially at low switching frequencies. We propose to compensate flux error along $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$. By so doing we will not only avoid error in volt-sec compensation but also naturally work towards achieving synchronism. Additionally, a strategy is adopted in this thesis where to obtain fast dynamic response maximum flux error $\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}$ (representing modulation index of 1) is compensated along the flux error in dynamic condition $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$.

With these features, the proposed method of operating in dynamic condition is explained as follows using Fig. 5.13. The solid arrows in Fig. 5.13 show the synchronous switching angles where flux error is compensated in steady state before the change in $\boldsymbol{\psi}_{\boldsymbol{c}}^{*}$. In the proposed method, the flux error compensation in dynamic condition starts with maximum possible flux error compensation along the vector $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ given by $\overrightarrow{QP}$. Maximum possible flux error compensation along the

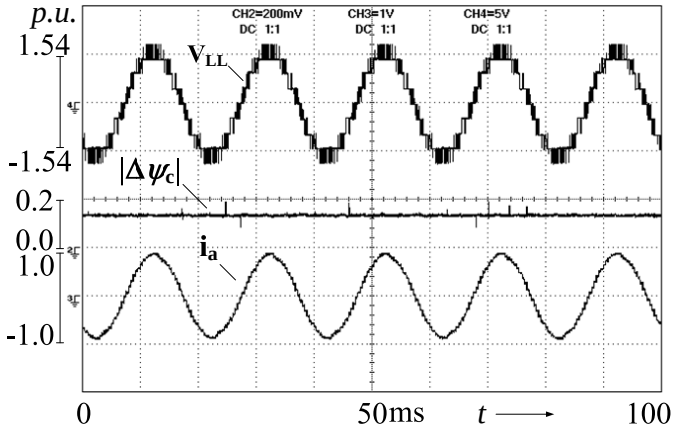



Figure 5.14: Output voltage, $\Delta\psi_c$ and $i_a$ for $v_c$=1.0 p.u. and $\delta$=45$^o$

vector $\Delta\boldsymbol{\psi_{c(dyn)}}$ not only helps to obtain good dynamic response but also helps to start the synchronization process right from the next sampling period. The dynamic response using such a strategy is shown in Fig. 5.14.

Since, we are applying maximum possible flux error, the converter is operating in six step operation during the dynamic condition. In the six-step operation one phase leg of the inverter has duty ratio/ pulse of '1' and other two phase legs are have duty ratio/ pulse of '0'. Since, the line frequency and switching frequency are fixed it is easier to ensure synchronism. For the synchronous PWM there should be a equal number of pulses in every fundamental line period. For the dynamic condition described above, there are equal numbers of pulses over a fundamental line period before and after the change in the reference vector. That shows that synchronism is not disturbed due to the change in reference vector. Eventually, switching angles for flux error compensation are shown by dotted arrows in Fig. 5.13. Since, $\omega_s$ and $\tau_s$ both are constant, angle $\omega_s\tau_s$ between any two

consecutive dotted arrows and between any two solid arrows in Fig. 5.13 are the same. Essentially, before and after dynamics there are the same number of flux error compensation instants at equal interval on time scale which also indicates restoration of synchronism.

Fig. 5.15 shows the dynamic condition takes place at $5.0ms$ and finishes at $7.5ms$. Due to six step operation the pulse width during dynamic condition are not same as during the steady state condition at the same position. In other words, desired pulses appear only after the dynamics is over because during dynamics we are applying the duty ratio of '1' to get a fast dynamic response. By applying maximum possible flux error the actual flux tries to catch up with reference flux. Depending on the initial flux error in the dynamic condition, in a number of cycles the flux error reduces are eventually is equal to steady state value.

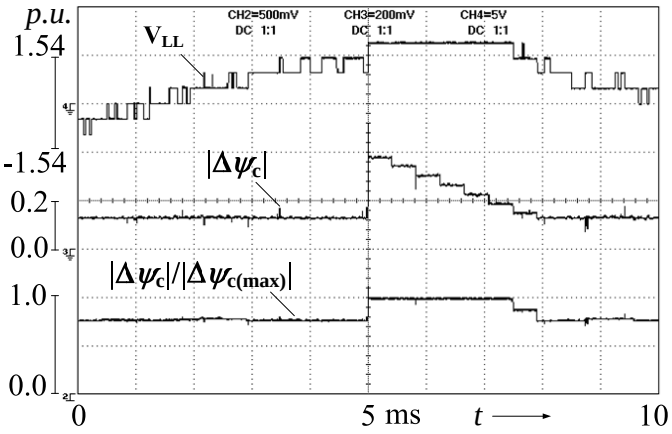



Figure 5.15: Inverter line voltage $\boldsymbol{v_{cl}}$, $|\Delta\psi_c|$ and $|\Delta\psi_c|/|\Delta\psi_{c(max)}|$ at $\psi_c$=1.0 p.u. and $\delta$=$45^o \rightarrow 59.5^o$

Take note that the process described above is valid irrespective of the instant of change in reference vector i.e. the flux error is computed at the same or next

switching cycle and the flux error compensation starts with maximum possible flux error compensation along the vector $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$. Now, let us elaborate the method used for the fast compensation of the large flux error $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ in dynamic condition. Referring to Fig. 5.13, flux error $\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}$ cannot be compensated in one switching cycle. The actual flux $\boldsymbol{\psi}_{\boldsymbol{c}}$ cannot change so fast with the sudden change in $\boldsymbol{\psi}_{\boldsymbol{c}}^{*}$. This is because maximum flux error $\boldsymbol{\Delta\psi}_{\boldsymbol{c(max)}}$ that can be compensated in a sampling period is limited by the capacity of DC-link. The maximum value of flux error $\boldsymbol{\Delta\psi}_{\boldsymbol{c(max)}}$ is obtained when $v_c$ is maximum. The maximum absolute value of $v_c$ is $(2/3)(n-1)V_{dc(HB)}$ which corresponds to a large vector in space vector diagram. The large vectors are the switching vectors which are at the vertices of the hexagon e.g. in Fig. 5.4 there are two large vectors i.e. $(2,-2,-2)$ and $(2,2,-2)$. The base value of $v_c$ is $(2/\pi)(n-1)V_{dc(HB)}$. Hence, $\boldsymbol{\Delta\psi}_{\boldsymbol{c(max)}}$ can be given as

$$\boldsymbol{\Delta\psi}_{\boldsymbol{c(max)}} = \frac{\pi}{3}\tau_s \tag{5.10}$$

If $|\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}|>|\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}|$ then the nearest large vector can be applied for full switching cycle to obtain fastest dynamic response [122]. The nearest large vector can be continuously held till $|\Delta\boldsymbol{\psi}_{\boldsymbol{c(dyn)}}|\leq|\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}|$.

Flowchart in Fig. 5.16 summarize the overall scheme in steady state as well as in dynamic condition. In the proposed scheme, $\Delta\boldsymbol{\psi}_{\boldsymbol{c}}$ is calculated in every switching cycle as explained in previous section.

When the magnitude of $\Delta\boldsymbol{\psi}_{\boldsymbol{c}}$ is more than $\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}$ then it shows the dy-

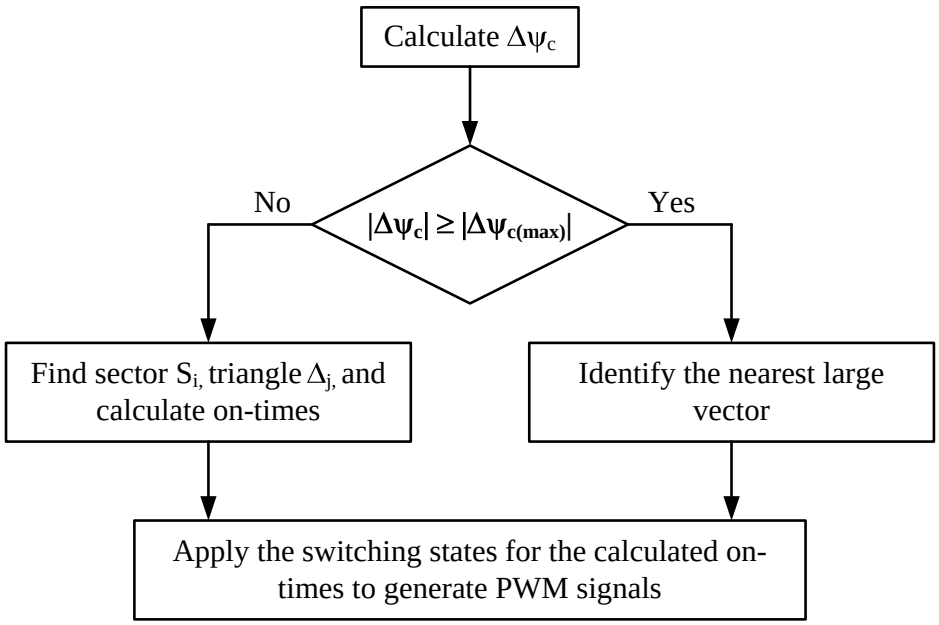



Figure 5.16: Simplified flowchart of the scheme

namic condition. In dynamic condition, to obtain fastest dynamic response the nearest large vector is switched by applying $|\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}|$. The large vectors are applied till the magnitude of $\Delta\boldsymbol{\psi}_{\boldsymbol{c}}$ becomes lesser than $\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}$. The algorithm proposed in chapter 3 is used to implement SVPWM in this condition.

When the magnitude of $\Delta\boldsymbol{\psi}_{\boldsymbol{c}}$ is less than $\Delta\boldsymbol{\psi}_{\boldsymbol{c(max)}}$ then based on the magnitude of $\Delta\boldsymbol{\psi}_{\boldsymbol{c}}$ it is determined whether the operation is in linear mode or overmodulation mode. In linear mode algorithm proposed in chapter 2 is used whereas in overmodulation mode algorithm proposed in chapter 3 is used. The detailed implementation is explained in next section.

To better explain dynamic operation a simple example is given here. Let us assume that at a given instant, angle $\delta$ changes from $\delta_1 \rightarrow \delta_2$ ($\delta_1 < \delta_2$) while keeping

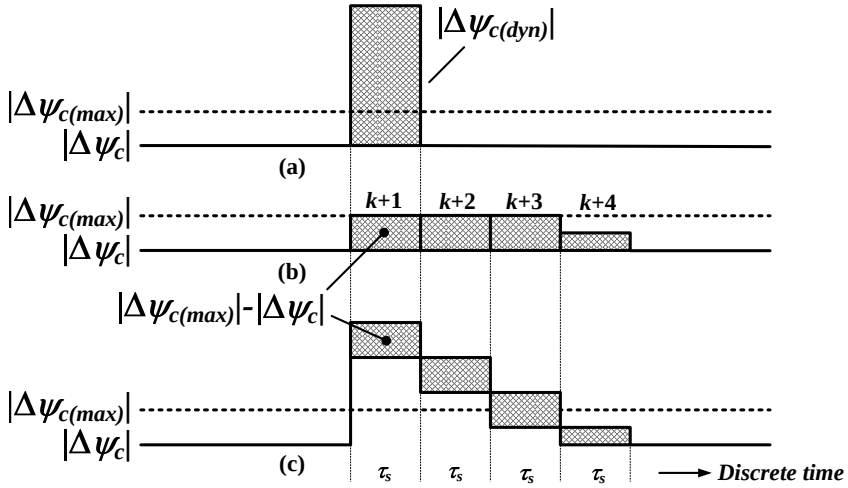



Figure 5.17: Fast flux error compensation in dynamic condition

the steady state flux $|\boldsymbol{\psi_c}|$ constant. It leads to a large flux error $|\boldsymbol{\Delta\psi_{c(dyn)}}|$ shown by gray rectangle in Fig. 5.17(a). This large flux error $|\boldsymbol{\Delta\psi_{c(dyn)}}|$ is shown by long dotted arrow in Fig. 5.13. The dotted line in Fig. 5.17 shows $|\boldsymbol{\Delta\psi_{c(max)}}|$.

For the fast compensation of large $|\boldsymbol{\Delta\psi_{c(dyn)}}|$, $|\boldsymbol{\Delta\psi_{c(max)}}|$ is applied in every switching cycle till $|\boldsymbol{\Delta\psi_{c(dyn)}}| < |\boldsymbol{\Delta\psi_{c(max)}}|$. For example in Fig. 5.17(b), $|\boldsymbol{\Delta\psi_{c(max)}}|$ is applied for three switching cycles i.e. $k$+1, $k$+2 and $k$+3. The $|\boldsymbol{\Delta\psi_{c(max)}}|$ can be written as $(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)+|\boldsymbol{\Delta\psi_c}|$. Hence, it can be assumed that apart from $|\boldsymbol{\Delta\psi_c}|$ additional $(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$ is applied for these three switching cycles shown by three shaded rectangles in Fig. 5.17(b). For $(k+4)^{th}$ switching cycle, $|\boldsymbol{\Delta\psi_{c(dyn)}}| < |\boldsymbol{\Delta\psi_{c(max)}}|$ but $|\boldsymbol{\Delta\psi_{c(dyn)}}| > |\boldsymbol{\Delta\psi_c}|$. Hence, in $(k+4)^{th}$ switching cycle additional compensation $(|\boldsymbol{\Delta\psi_{c(dyn)}}| - |\boldsymbol{\Delta\psi_c}|)$ is required which is lesser than $(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$. This required compensation is shown by a smaller gray rectangle in Fig. 5.17(b) which can be assumed a fraction of

($|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|$) compensated in previous three cycles. If this fraction is represented as $\rho_f$ ($0 \leq \rho_f < 1.0$) then for $(k{+}4)^{th}$ switching cycle in Fig. 5.17(b), $(|\boldsymbol{\Delta\psi_{c(dyn)}}| - |\boldsymbol{\Delta\psi_c}|) = \rho_f\ (|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$. Assuming this, total additional flux error compensation in dynamic condition $|\boldsymbol{\Delta\psi_{c(dyna)}}|$ can be expressed in terms of ($|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|$) as,

$$|\boldsymbol{\Delta\psi_{c(dyna)}}| = \rho_i(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|) + \rho_f(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|) \qquad (5.11)$$

In (5.11), $\rho_i$ is an integer ($\rho_i = 1, 2, ...$) e.g. for Fig. 5.17(b) $\rho_i$=3. In general (5.11) shows that for $\rho_i$ switching cycles $|\boldsymbol{\Delta\psi_{c(max)}}|$ is applied and for one switching cycle $|\Delta\boldsymbol{\psi_c}|{+}\rho_f(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$ is applied. It should also be noted that with compensation $|\boldsymbol{\Delta\psi_{c(dyn)}}|$ slowly reduces. For the large $|\boldsymbol{\Delta\psi_{c(dyn)}}|$ shown in Fig. 5.17(a), due to $|\boldsymbol{\Delta\psi_{c(max)}}|$ compensation in every switching cycle resultant gradual decrease in $|\boldsymbol{\Delta\psi_{c(dyn)}}|$ is shown in Fig. 5.17(c).

Total shaded area in Fig. 5.17(a), (b) and (c) represent additional volt-sec during the dynamic condition. The areas in Fig. 5.17(a), (b) and (c) are equal. Hence, this method not only achieves fast dynamics, but the volt-sec balance is also maintained in the dynamic condition. Experimental results are shown next.

Fig. 5.18 shows the effect of angle change $\delta$=45$^o$→59.5$^o$ on $\alpha$ and $\beta$ component of predicted converter flux, actual flux and their difference at $v_c$=1.0 p.u. The $\boldsymbol{\psi_c^*}$ changes immediately, and $\boldsymbol{\psi_c}$ follows it. The $\Delta\boldsymbol{\psi_c}$ waveform shows this effect.

Fig. 5.19 shows the dynamic condition where the angle change $\delta$=45$^o$→59.5$^o$

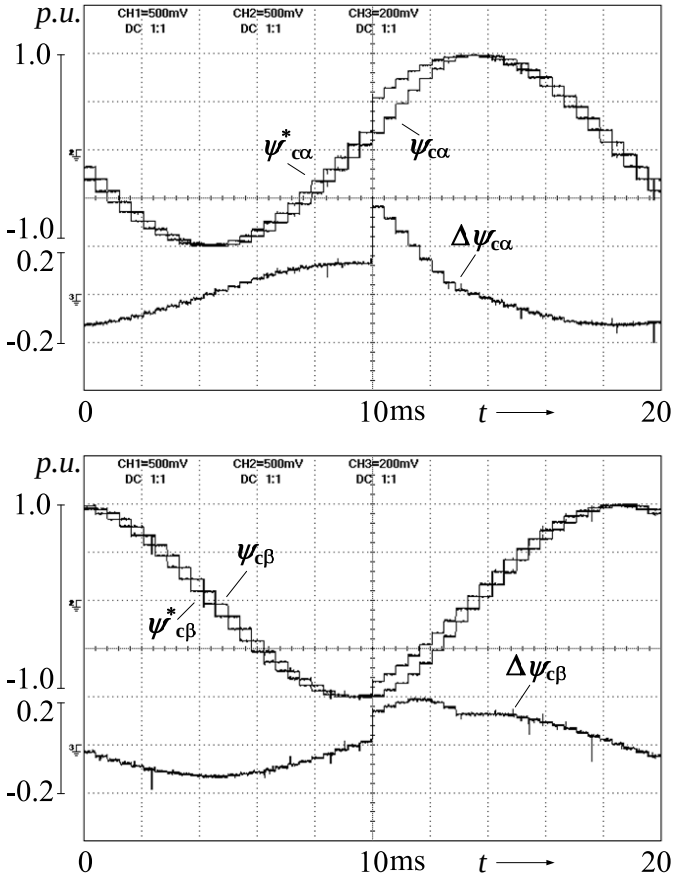



Figure 5.18: The $\alpha$ and $\beta$ component of predicted converter flux, actual converter flux and their difference at $v_c$=1.0 p.u. and $\delta$=45$^o$→59.5$^o$

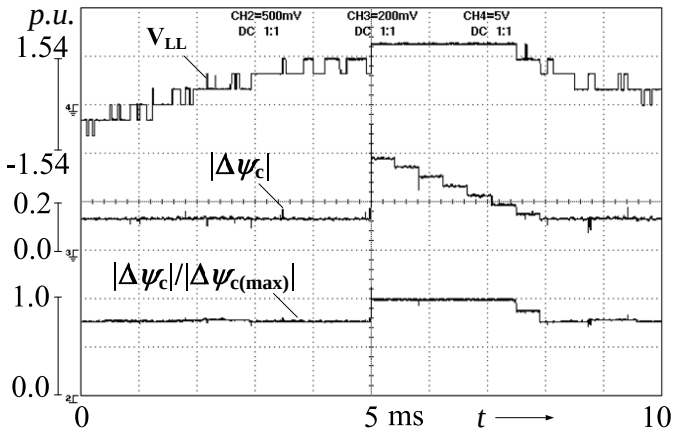



Figure 5.19: Inverter line voltage $\boldsymbol{v_{cl}}$, $|\Delta\psi_c|$ and $|\Delta\psi_c|/|\Delta\psi_{c(max)}|$ at $\psi_c$=1.0 p.u. and $\delta$=45$^o$→59.5$^o$

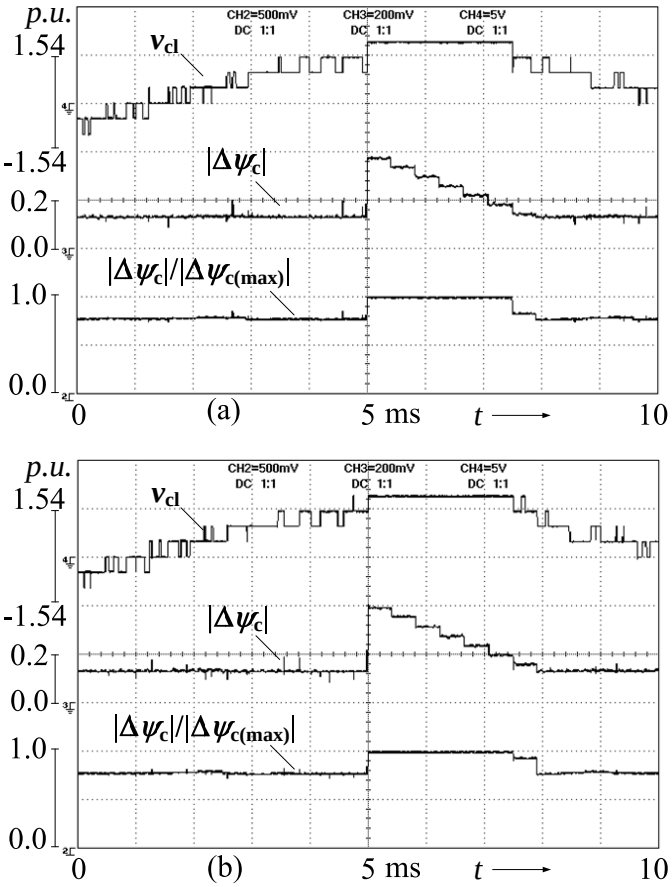



Figure 5.20: Inverter line voltage $\boldsymbol{v_{cl}}$, $|\Delta\psi_c|$ and $|\Delta\psi_c|/|\Delta\psi_{c(max)}|$ at $\psi_c$=1.0 p.u. for the change (a) $\delta$=45$^o$→59$^o$, (b) $\delta$=45$^o$→60$^o$

takes place at $t = 5\,ms$. In this figure, the inverter line voltage $\boldsymbol{v_{cl}}$, flux $|\boldsymbol{\psi_c}|$ and ratio $|\Delta\boldsymbol{\psi_c}|/|\Delta\boldsymbol{\psi_{c(max)}}|$ are plotted to show the effect of this change. Referring to (5.11) in previous section and Fig. 5.17, here $\rho_i = 6$ and $\rho_f \approx 0.5$ for the Fig. 5.19. The $\rho_i = 6$ implies that $|\boldsymbol{\psi_{c(max)}}|$ is applied for six cycles. For which the voltage waveform $\boldsymbol{v_{cl}}$ shows the six step characteristics and $|\Delta\boldsymbol{\psi_c}|/|\Delta\boldsymbol{\psi_{c(max)}}|$ is unity. The $\rho_f \approx 0.5$ implies that $|\Delta\boldsymbol{\psi_c}|$+0.5($|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|$) is applied for one cycle, as shown in Fig. 5.19.

For a different change in angle $\delta$, the value of $\rho_i$ and $\rho_f$ will be different e.g.

1. In Fig. 5.20(a), the angle change $\delta$=45$^o$→59$^o$ takes place at $t = 5ms$. Here, $\rho_i = 6$ and $\rho_f \approx 0.3$ i.e. for six cycles $|\Delta\boldsymbol{\psi_{c(max)}}|$ is applied and for one cycle $|\Delta\boldsymbol{\psi_c}|$+0.3($|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|$) is applied. Since, $\rho_f$ has lower value compared to previous case, the $|\Delta\boldsymbol{\psi_c}|+\rho_f(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$ is also lower as compared to Fig. 5.19 and can be seen in Fig. 5.20(a).

2. In Fig. 5.20(b), the angle change $\delta$=45$^o$→60$^o$ takes place at $t = 5ms$. Here, $\rho_i = 6$ and $\rho_f \approx 0.7$ i.e. for six cycles $|\Delta\boldsymbol{\psi_{c(max)}}|$ is applied and for one cycle $|\Delta\boldsymbol{\psi_c}|$+0.7($|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|$) is applied. Since, $\rho_f$ has higher value compared to previous case, the $|\Delta\boldsymbol{\psi_c}|+\rho_f(|\boldsymbol{\Delta\psi_{c(max)}}| - |\boldsymbol{\Delta\psi_c}|)$ is also higher as compared to Fig. 5.19 and can be seen in Fig. 5.20(b).

## 5.5 Implementation of the Proposed Scheme

The proposed close loop scheme is implemented in the same manner as done in previous chapters i.e. using a processing unit and mapping unit shown in Fig. 3.4. The block 'S' in Fig. 5.3 essentially consists of these two units.

### 5.5.1 Processing Unit

Referring to Fig. 3.4 and Fig. 5.3, input to the processing unit is flux error $\Delta\boldsymbol{\psi_c}$. The flux error is used to determine the sector number, triangle number and on-times $t_o$, $t_a$ and $t_b$ as explained in chapter 2 and 3. These are subsequently

provided to mapping unit to find the appropriate switching sequence.

### 5.5.2 Mapping Unit

The mapping unit has similar structure as described in previous chapter, Fig. 3.4. However, the switching sequences are different. It is mentioned in section 1.3.2 that the output performance can be further improved when waveform symmetries (half wave and three phase symmetries) and bus-clamping techniques are incorporated in synchronous SVPWM. These techniques were proposed for two-level inverters in [112]-[115] and then applied to 3-level NPC inverter in [79][116].

Fig. 5.21 shows the complete space vector diagram of a 5-level inverter. The switching sequence for any triangle is formed using the switching states at vertices. The typical switching sequence involves three switchings per switching cycle i.e. one switching per phase. However, in the bus-clamping techniques [112]-[115] there are typically two switching per switching cycle i.e. one of the phases is not switched. This directly results in reduction of switching losses by a factor of 1/3.

Beig *et al.* [79][116] applied synchronous SVPWM for three-level neutral point clamped inverter. The synchronous SVPWM in [79] explains the advantages of waveform symmetries for a three-level inverter, however does not include bus-clamping. The synchronous SVPWM in [116] shows a simple implementation of the bus-clamping technique for three-level inverter. For the easy extension to higher levels the switching sequence for any triangle must be independent of the reference

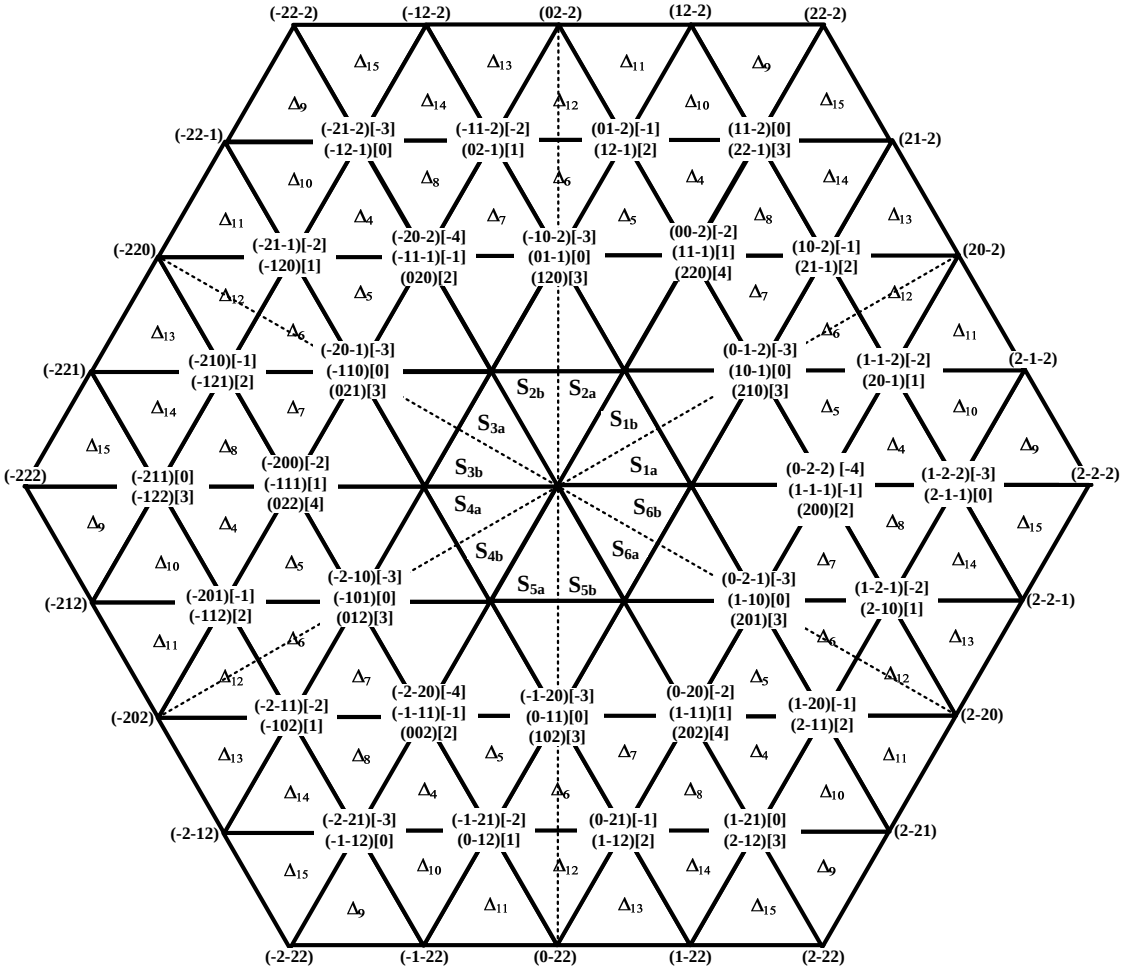



Figure 5.21: Space Vector Diagram for 5-level Inverter - Conventional

| Clamped Phase | Positive Region | Negative Region |
|---|---|---|
| u | $S_{1a}$, $S_{6b}$ | $S_{3b}$, $S_{4a}$ |
| v | $S_{2b}$, $S_{3a}$ | $S_{5b}$, $S_{6a}$ |
| w | $S_{4b}$, $S_{5a}$ | $S_{1b}$, $S_{2a}$ |

Table 5.1: Clamped phases for $60^o$ clamping technique

vector at any instant which is not obvious in [116]. Moreover, the on-time calculation method used in [116] cannot be easily extended to higher levels. To avoid these problems, a simple implementation is proposed and explained below.

| Clamped Phase | Positive Region | Negative Region |
|---|---|---|
| u<br>v<br>w | $S_{6a}$, $S_{1b}$<br>$S_{2a}$, $S_{3b}$<br>$S_{4a}$, $S_{5b}$ | $S_{3a}$, $S_{4b}$<br>$S_{5a}$, $S_{6b}$<br>$S_{1a}$, $S_{2b}$ |

Table 5.2: Clamped phases for $30^o$ clamping technique

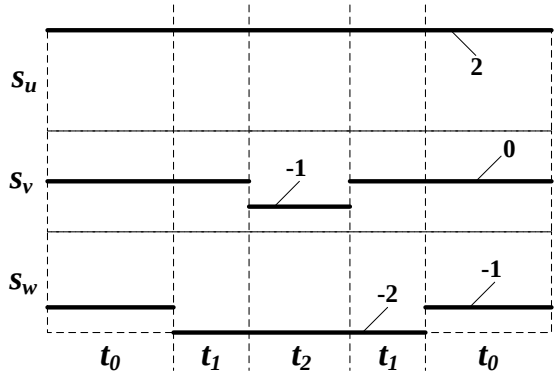



Figure 5.22: The transitions in $\triangle_{11}$ for $60^o$ clamping technique

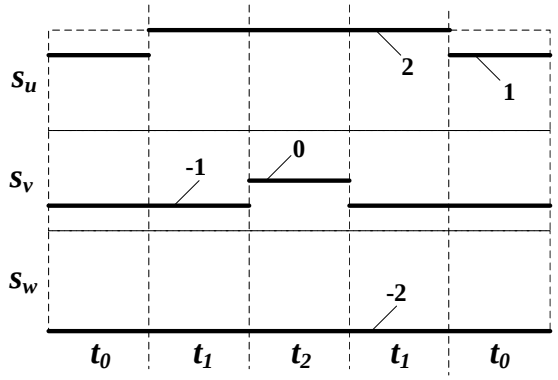



Figure 5.23: The transitions in $\triangle_{11}$ for $30^o$ clamping technique

Two of the three phases can be clamped in any sector. For example, in Fig. 5.4 at any vertex in sector 1, the phase $u$ can be clamped to $2V_{dc(HB)}$ represented as $u^+$, or the phase $w$ can be clamped to -$2V_{dc(HB)}$ represented as $w^-$. To obtain the symmetries, the bus-clamping leads to two main techniques known

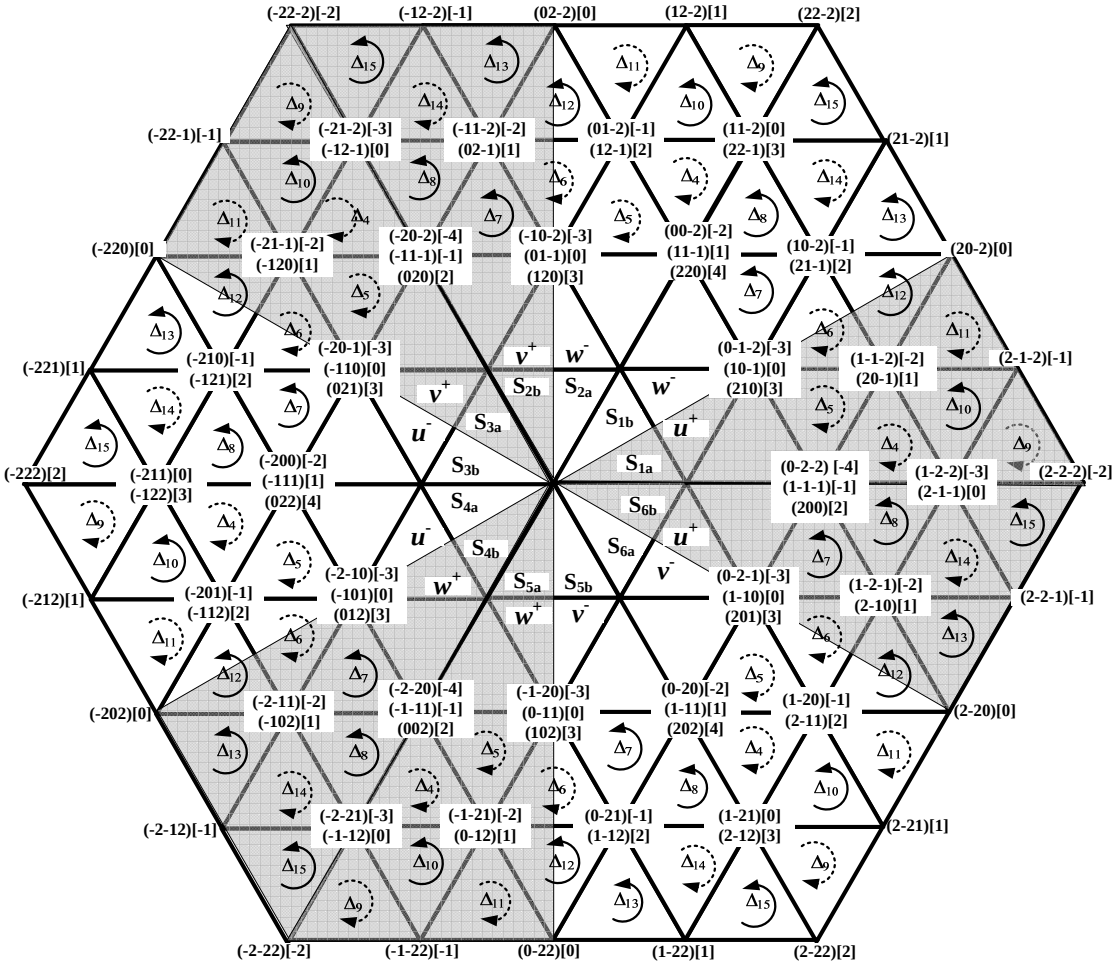



Figure 5.24: Space Vector Diagram - Emphasizing $60^o$ clamping technique

as '$60^o$' and '$30^o$' clamping techniques respectively [113]. The main difference in these two techniques is that the two parts $S_{1a}$ and $S_{1b}$ of the sector are clamped to exactly opposite phases. Tables 5.1 and 5.2 summarize the clamped phases in the two parts of the sector $S_{ia}$ and $S_{ib}$ for the $60^o$ and $30^o$ clamping techniques respectively. Fig. 5.22 shows the state transitions for $\triangle_{11}$ in sector 1 for $60^o$ clamping technique. Fig. 5.23 shows the state transitions for $\triangle_{11}$ in sector 1 for $30^o$ clamping technique. Though Fig. 5.22 and Fig. 5.23 have the same number of transitions but the switching pattern and clamped phase differs i.e. phase $u$ in Fig. 5.22 and phase

$w$ in Fig. 5.23.

The clamped phases for $60^o$ clamping technique are shown with gray color in Fig. 5.24. The implementation of $60^o$ clamping technique is explained below for a 5-level cascaded inverter and can be easily extended to higher levels using the same methodology. The $30^o$ clamping technique has been implemented in a similar manner with equal ease and verified experimentally.

Two additional requirements while forming the switching sequence are, (i) within a triangle for a given switching sequence there is only one switching for one switching state to another state transition, (ii) the switchings are minimal while changing the switching sequence between the triangles.

In Fig. 5.24, due to the phase clamping, only three switching states are available for every triangle e.g. in $\triangle_6$ the available switching states are (2,0,-1), (2,0,0) and (2,1,0). The same is true for other triangles. Let these three switching states be $SS_0$, $SS_1$ and $SS_2$ which are executed for the total on-times of $t_0$, $t_1$ and $t_2$, where $t_0+t_1+t_2=\tau_s$. The typical switching sequence for a triangle is $SS_0[t_0/2]\rightarrow SS_1[t_1/2]\rightarrow SS_2[t_2]\rightarrow SS_1[t_1/2]\rightarrow SS_0[t_0/2]$. The square bracket next to switching state shows the on-time for which it is executed. The subscript on SS is stage $k_{st}$ of the sequence and is useful for real time implementation. Stage $k_{st}=0\rightarrow 2$ for set cycle and $k_{st}=2\rightarrow 0$ for reset cycle of the complete switching cycle. The circular arrow in Fig. 5.24 indicates the order in which the switching states $SS_0$, $SS_1$ and $SS_2$ are ordered. The switching sequence for first two sectors are shown in table

| Sector | Triangle | $SS_0 \rightarrow$ | $\rightarrow SS_1 \rightarrow$ | $\rightarrow SS_2 \rightarrow$ | $\rightarrow SS_1 \rightarrow$ | $\rightarrow SS_0$ |
|---|---|---|---|---|---|---|
| 1 | $\triangle_4$ | (2,0,0) | (2,0,-1) | (2,-1,-1) | (2,0,-1) | (2,0,0) |
| | $\triangle_5$ | (2,0,-1) | (2,0,0) | (2,1,0) | (2,0,0) | (2,0,-1) |
| | $\triangle_7$ | (1,0,-2) | (0,0,-2) | (0,-1,-2) | (0,0,-2) | (1,0,-2) |
| | $\triangle_8$ | (0,0,-2) | (1,0,-2) | (1,1,-2) | (1,0,-2) | (0,0,-2) |
| | $\triangle_9$ | (2,-1,-1) | (2,-1,-2) | (2,-2,-2) | (2,-1,-2) | (2,-1,-1) |
| | $\triangle_{10}$ | (2,0,-1) | (2,-1,-1) | (2,-1,-2) | (2,-1,-1) | (2,0,-1) |
| | $\triangle_{11}$ | (2,0,-1) | (2,0,-2) | (2,-1,-2) | (2,0,-2) | (2,0,-1) |
| | $\triangle_{13}$ | (1,0,-2) | (2,0,-2) | (2,1,-2) | (2,0,-2) | (1,0,-2) |
| | $\triangle_{14}$ | (1,0,-2) | (1,1,-2) | (2,1,-2) | (1,1,-2) | (1,0,-2) |
| | $\triangle_{15}$ | (1,1,-2) | (2,1,-2) | (2,2,-2) | (2,1,-2) | (1,1,-2) |
| 2 | $\triangle_4$ | (0,0,-2) | (0,1,-2) | (1,1,-2) | (0,1,-2) | (0,0,-2) |
| | $\triangle_5$ | (0,1,-2) | (0,0,-2) | (-1,0,-2) | (0,0,-2) | (0,1,-2) |
| | $\triangle_7$ | (0,2,-1) | (0,2,0) | (1,2,0) | (0,2,0) | (0,2,-1) |
| | $\triangle_8$ | (0,2,0) | (0,2,-1) | (-1,2,-1) | (0,2,-1) | (0,2,0) |
| | $\triangle_9$ | (1,1,-2) | (1,2,-2) | (2,2,-2) | (1,2,-2) | (1,1,-2) |
| | $\triangle_{10}$ | (0,1,-2) | (1,1,-2) | (1,2,-2) | (1,1,-2) | (0,1,-2) |
| | $\triangle_{11}$ | (0,1,-2) | (0,2,-2) | (1,2,-2) | (0,2,-2) | (0,1,-2) |
| | $\triangle_{13}$ | (0,2,-1) | (0,2,-2) | (-1,2,-2) | (0,2,-2) | (0,2,-1) |
| | $\triangle_{14}$ | (0,2,-1) | (-1,2,-1) | (-1,2,-2) | (-1,2,-1) | (0,2,-1) |
| | $\triangle_{15}$ | (-1,2,-1) | (-1,2,-2) | (-2,2,-2) | (-1,2,-2) | (-1,2,-1) |

Table 5.3: Switching sequence for the triangles

| Sector | Triangle | $SS_0 \rightarrow$ | $\rightarrow SS_1 \rightarrow$ | $\rightarrow SS_2$ |
|---|---|---|---|---|
| 1 | $\triangle_6$ | (2,0,-1) | (1,0,-1) | (1,0,-2) |
| | $\triangle_{12}$ | (2,0,-1) | (2,0,-2) | (1,0,-2) |
| 2 | $\triangle_6$ | (0,1,-2) | (0,1,-1) | (0,2,-1) |
| | $\triangle_{12}$ | (0,1,-2) | (0,2,-2) | (0,2,-1) |

Table 5.4: Switching sequence for the triangles $\triangle_6$ and $\triangle_{12}$

5.3. Note that, (i) within a triangle there is only one switching for any switching state transition, (ii) since any switching sequence starts and ends with $SS_0$, there is only one switching or no switching while moving from one triangle to another.

The triangles $\triangle_6$ and $\triangle_{12}$ are located at the boundary of two clamping re-

| Triangle | $\triangle_4$ | $\triangle_5$ | $\triangle_6$ | $\triangle_7$ | $\triangle_8$ | $\triangle_9$ | $\triangle_{10}$ | $\triangle_{11}$ | $\triangle_{12}$ | $\triangle_{13}$ | $\triangle_{14}$ | $\triangle_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Order | 3 | 3 | 6 | 1 | 1 | 3 | 4 | 3 | 5 | 1 | 2 | 1 |

Table 5.5: Identified order for the $60^o$ phase clamping method

gions. Hence, the switching sequence for them is not the same as for other triangles. The switching sequence for triangles $\triangle_6$ and $\triangle_{12}$ are shown in table 5.4. For these two triangles the switching sequence is $SS_0 \rightarrow SS_1 \rightarrow SS_2$ i.e. it is not reversed. Such a sequence allows smooth transition from one clamped region to another. Let us take an example using triangle $\triangle_{11}$, $\triangle_{12}$ and $\triangle_{13}$ in $S_1$. To minimize the commutation losses, (i) the starting state for the switching sequence in $\triangle_{12}$ should be the same as end state for the switching sequence in $\triangle_{11}$ which is (2,0,-1), (ii) the end state for the switching sequence in $\triangle_{12}$ should be the same as starting state for the switching sequence in $\triangle_{13}$ which is (1,0,-2). Thus, if the switching sequence for the triangle $\triangle_{12}$ is (2,0,-1)$\rightarrow$(1,0,-1)$\rightarrow$(1,0,-2) there will be minimum commutation losses when reference vector moves from one triangle to another.

The duty ratios obtained using (2.5)$\rightarrow$(2.7) are in a generic form $t_o$, $t_a$ and $t_b$. Since the switching sequence varies from one triangle to another, an arrangement is required to order the calculated on-times $t_o$, $t_a$ and $t_b$ in the desired sequence of $t_0 \rightarrow t_1 \rightarrow t_2$. There are 6 possible orders as shown in table 4.3. For each triangle in Fig. 5.24 an order is identified using tables 4.3, 5.3, 5.4. A triangle in any sector has the same order of duty-ratios. The table 5.5 summarizes the order of duty-ratios.

## 5.6 Experimental Results, and Their Analysis

The proposed scheme can be easily implemented on a DSP microcontroller. However, for laboratory experiments an existing dSPACE DS1104 system was used. The algorithm was implemented in C language. A laboratory prototype of 5-level cascaded inverter is used for the experiments, see Fig. 1.3.

Fig. 5.27 shows experimental results for the synchronous SVPWM with $60^o$ bus clamping technique. Experimental results in Fig. 5.25 and Fig. 5.26 are for conventional SVPWM. For theses experiments, DC-link voltage $V_{dc(HB)}$=160V and fundamental frequency $f$=50Hz. Compared to Fig. 5.25(b) and Fig. 5.26(b), in Fig. 5.27(b) synchronous SVPWM lead to significant reduction of subharmonics. Similarly, compared to Fig. 5.25(c) and Fig. 5.26(c), in Fig. 5.27(c) synchronous SVPWM lead to significant reduction of interharmonics. Along with this, number of switchings are lesser in Fig. 5.27(a) as compared to Fig. 5.25(a) and Fig. 5.26(a).

Using the algorithm proposed in chapter 3, the proposed synchronous SVPWM can be easily extended to overmodulation range ($0.907<m_i<1.0$). Fig. 5.28 shows the experimental waveforms for the $60^o$ bus clamping technique at $m_i$=0.93. The experimental conditions are the same as described above. The effect of overmodulation can be seen in Fig. 5.28(a). Fig. 5.28(b) and (c) demonstrate the reduction of subharmonics and interharmonics as explained before.

The Fig. 5.29 shows the symmetry available in the waveform at $m_i$=0.9 at

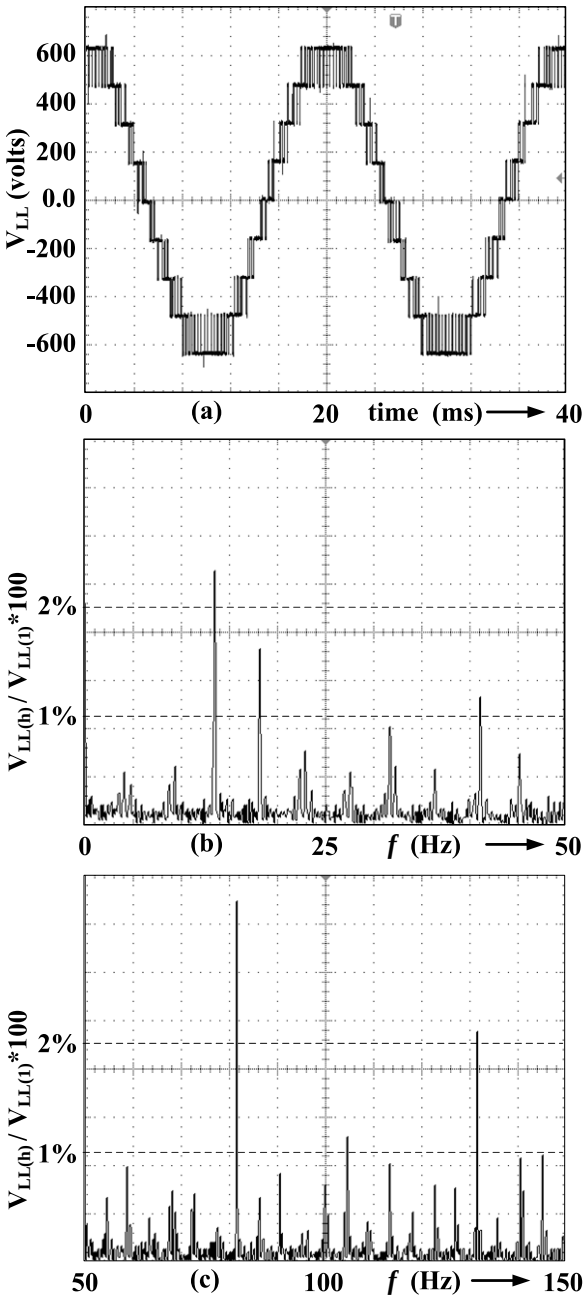



Figure 5.25: (a) Inverter line voltage, (b) FFT for 0→50Hz to show subharmonics, (c) FFT for 50Hz→150Hz to show interharmonics for conventional SVPWM at $V_{dc(HB)}$=160V, $m_i$=0.9, $\tau_s$=550$\mu$s

two sampling frequencies $f_s$=0.9kHz and 1.8kHz. The experimental conditions are the same as described for the Fig. 5.27.

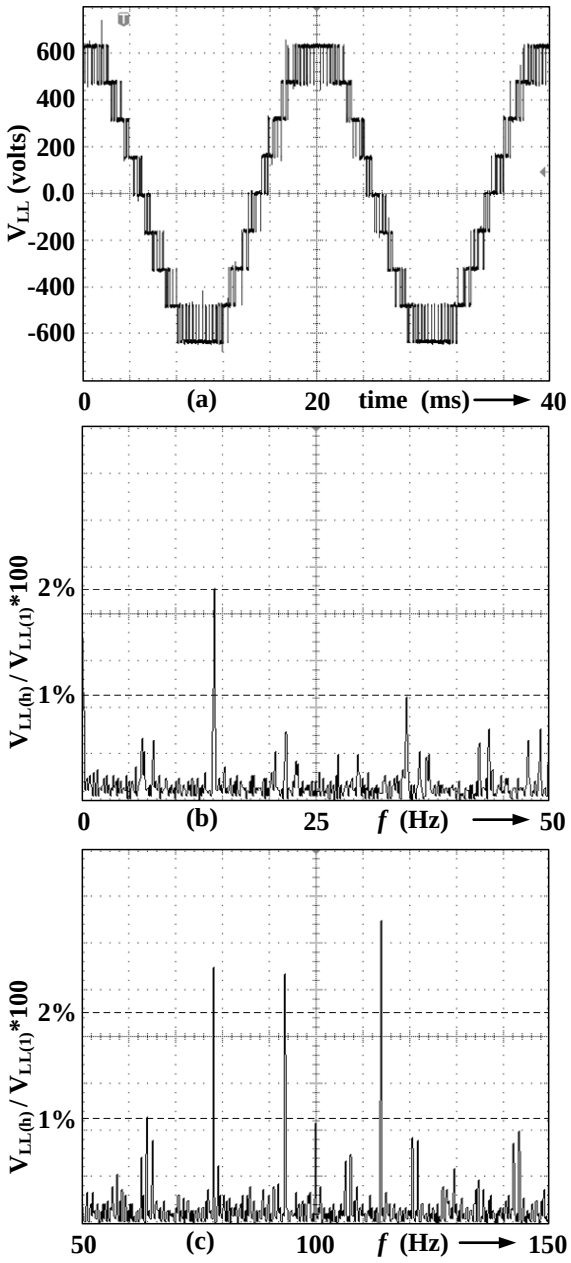



Figure 5.26: (a) Inverter line voltage, (b) FFT for 0→50Hz to show subharmonics, (c) FFT for 50Hz→150Hz to show interharmonics for conventional SVPWM at $V_{dc(HB)}$=160V, $m_i$=0.9, $\tau_s$=560$\mu$s

Fig. 5.30 shows the experimental results for the synchronous SVPWM with $30^o$ bus clamping technique. The experimental conditions are the same as described before. Compared to Fig. 5.25(b) and Fig. 5.26(b), note that in Fig. 5.30(b)

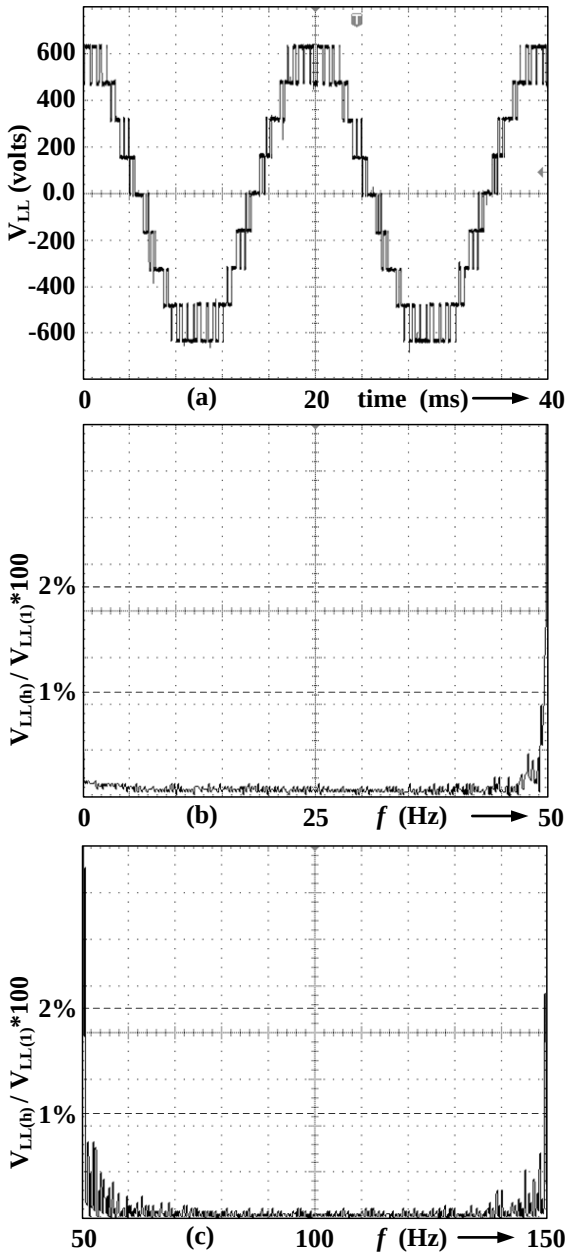



Figure 5.27: (a) Inverter line voltage, (b) FFT for 0→50Hz to show subharmonics, (c) FFT for 50Hz→150Hz to show interharmonics for proposed $60^o$ clamped SVM at $V_{dc}$=160V, $m_i$=0.9, $\tau_s$=555.55$\mu$s

synchronous SVPWM lead to significant reduction of subharmonics. Similarly, compared to Fig. 5.25(c) and Fig. 5.26(c), note that in Fig. 5.30(c) synchronous SVPWM lead to significant reduction of interharmonics. Along with this the

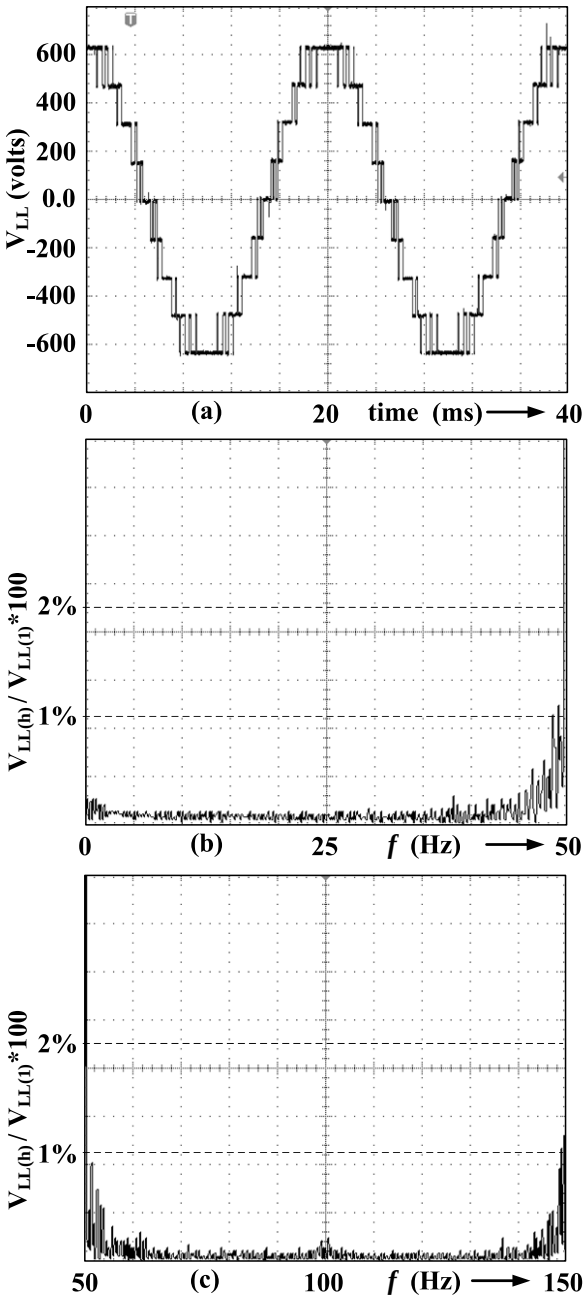



Figure 5.28: (a) Inverter line voltage, (b) FFT for 0→50Hz to show subharmonics, (c) FFT for 50Hz→150Hz to show interharmonics for proposed $60^o$ clamped SVM at $V_{dc}$=160V, $m_i$=0.93, $\tau_s$=555.55$\mu$s

number of switching are lesser in Fig. 5.30(a) as compared to Fig. 5.25(a) and Fig. 5.26(a).

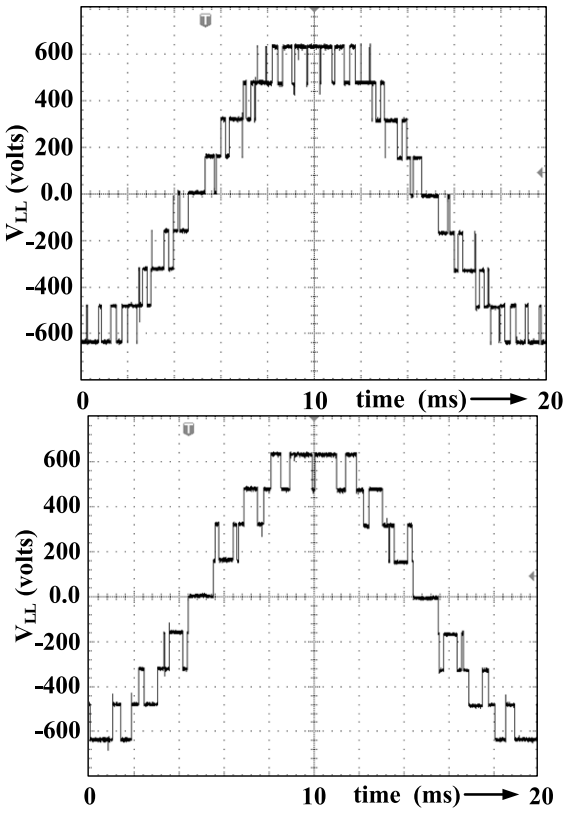



Figure 5.29: Converter output voltage showing symmetry at $V_{dc}$=160V, $m_i$=0.9 for $f_s$=1.8kHz and $f_s$=0.9kHz

For the close loop experiments, a small three-phase synchronous generator available in laboratory is used to simulate the power grid, Fig. 5.1. This synchronous generator is rated for line voltage of $400V$ and phase current of $0.5A$. The synchronous reactance $x_s$ for the experimental setup is approximately 0.2p.u. Experimental conditions; DC-link voltage $V_{dc(HB)}$=$125V$, fundamental frequency $f_1 = 50$Hz, and sampling period $\tau_s = 555.55\mu s$.

In Fig. 5.31 inverter line voltage $\boldsymbol{v_{cl}}$, $\Delta\boldsymbol{\psi_{c\alpha}}$, $\Delta\boldsymbol{\psi_{c\beta}}$ and $|\boldsymbol{\psi_c}|$ are plotted at $\boldsymbol{\psi_c} = 1.0p.u.$ and $\delta = 45^o$. In Fig. 5.32 inverter line voltage $\boldsymbol{v_{cl}}$, $|\boldsymbol{\psi_c}|$ and phase current $\boldsymbol{i_s}$ are plotted at $\boldsymbol{\psi_c} = 1.0p.u.$ and $\delta = 45^o$.

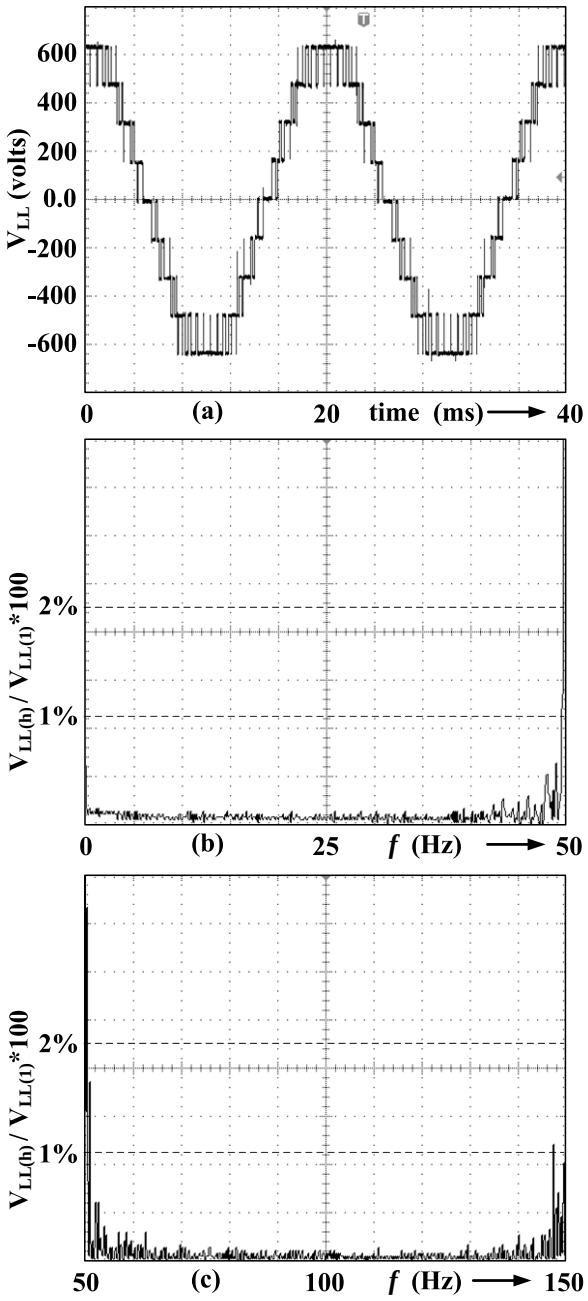



Figure 5.30: Converter output voltage, FFT for 0→50Hz to show subharmonics and FFT for 50Hz→150Hz to show interharmonics for proposed $30^o$ clamped SVM at $V_{dc}$=160V, $m_i$=0.9, $\tau_s$=555.55$\mu$s

In Fig. 5.33, inverter line voltage $v_{cl}$, grid line voltage $v_{gl}$, flux error $|\Delta\boldsymbol{\psi_c}|$ and $|\Delta\boldsymbol{\psi_c}|/|\Delta\boldsymbol{\psi_{c(max)}}|$ are plotted for the change $\delta$=$45^o$→$60^o$ at $\psi_c$=1.0. The objective here is to show the change in phase difference between $v_{cl}$ and $v_{gl}$ waveforms

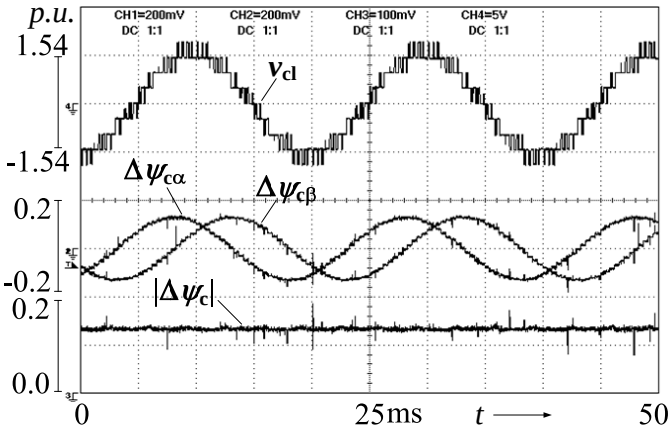



Figure 5.31: Output voltage, $\Delta\psi_{c\alpha}$, $\Delta\psi_{c\beta}$ and $|\Delta\psi_c|$ at $v_c$=1.0 p.u. and $\delta$=45$^o$

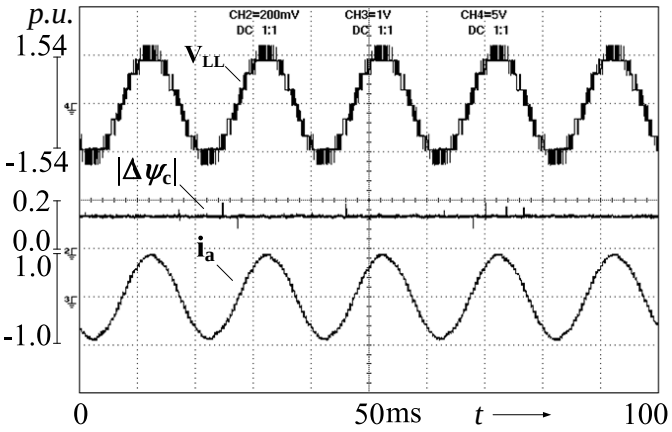



Figure 5.32: Output voltage, $\Delta\psi_c$ and $i_a$ for $v_c$=1.0 p.u. and $\delta$=45$^o$

before and after the change whereas the magnitude $|\Delta\boldsymbol{\psi_c}|$ is the same. The phase difference between these two waveforms is shown by two vertical dotted lines.

The $v_{cl}$, $|\Delta\boldsymbol{\psi_c}|$, $p$ and $q$ are plotted in Fig. 5.34 for the change $\delta = 45^o \rightarrow 60^o$ at $\boldsymbol{\psi_c}$=1.0. The effect on $v_{cl}$ and $|\Delta\boldsymbol{\psi_c}|$ is the same as explained before.

Inverter line voltage $v_{cl}$, $|\Delta\boldsymbol{\psi_c}|$ and current $i_u$ are plotted in Fig. 5.35 for the change $\delta = 45^o \rightarrow 60^o$ at $\boldsymbol{\psi_c}$=1.0. The time required for the current to settle down

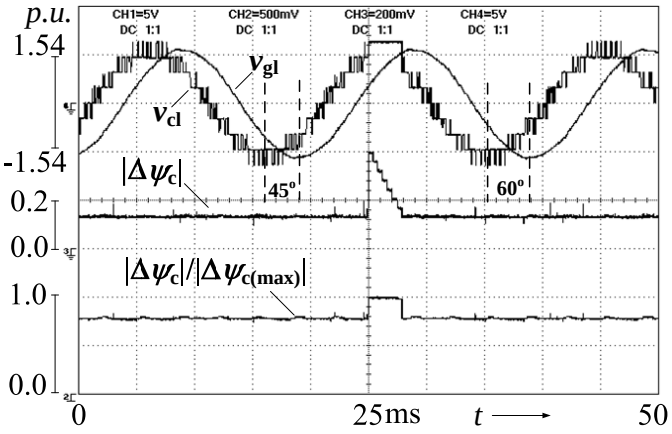



Figure 5.33: Inverter line voltage $\boldsymbol{v_{cl}}$, grid voltage $\boldsymbol{v_{gl}}$, $|\Delta\psi_c|$ and $|\Delta\psi_c|/|\Delta\psi_{c(max)}|$ for $\delta$=45$^o$→60$^o$ at $\psi_c$=1.0

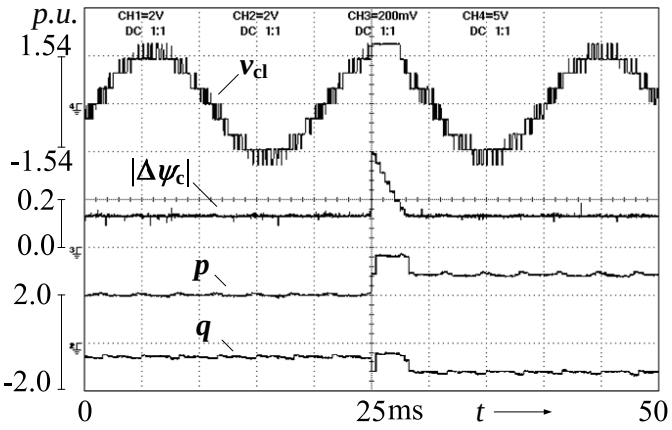



Figure 5.34: Inverter line voltage $\boldsymbol{v_{cl}}$, $|\Delta\psi_c|$, $p$ and $q$ for $\delta$=45$^o$→60$^o$ at $\psi_c$=1.0

is nearly 40% of the fundamental period.

## 5.7 Summary

Various problems due to subharmonics and interharmonics for a grid connected voltage source inverter were briefly elaborated in chapter 1. Synchronous space vector PWM for a cascaded H-bridge inverter is implemented, and imple-

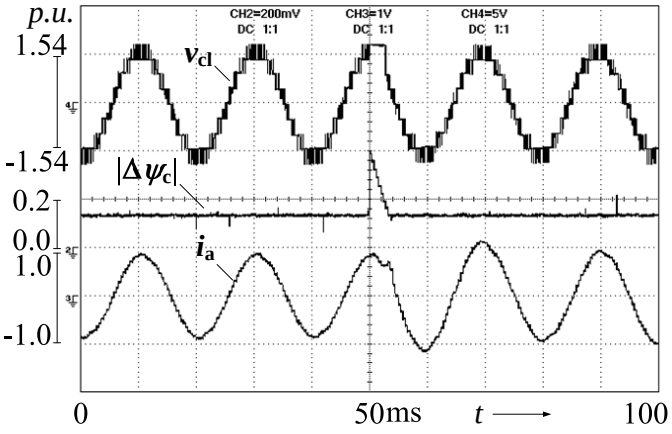



Figure 5.35: Inverter line voltage $\boldsymbol{v_{cl}}$, $|\Delta\psi_c|$, $i_a$ for $\delta$=45$^o$→60$^o$ at $\psi_c$=1.0

mentation is explained in section 5.5 of this chapter. Fig. 5.25 - Fig. 5.27 show successful elimination of subharmonics and interharmonics. The proposed scheme can be easily extended in overmodulation region as shown in Fig. 5.28 using the algorithm proposed in chapter 3. Main contribution of this chapter is a simple scheme for close loop flux control of a grid connected cascaded multilevel inverter. The working principle is explained in section 5.5. Flux estimation is done using a simple method discussed in section 5.3.2. Flux prediction is used to eliminate the phase lag error. Flux prediction is explained in section 5.3.3 and associated results are shown in Fig. 5.7-Fig. 5.9. Along with steady state, the dynamic operation is explained in detail, see section 5.4. During dynamics, the flux error is compensated fast by fully utilizing the maximum DC-link. A simple method is used to ensure synchronism in dynamic condition. The volt-sec balance is maintained even during dynamics. All computations inclusive of on-times computations are done online i.e. no off-line computation is required. Along with implementing synchronous

SVPWM, the redundant switching states of cascaded inverter are utilized to (i) reduce switching losses, (ii) obtain waveform symmetries to improve inverter performance. The implementation of proposed scheme is explained for $60^o$ technique. The scheme is constant switching frequency scheme. The experimental results are shown for a laboratory prototype of 5-level cascaded inverter.

# Chapter 6

# A Space Vector PWM Scheme to Operate a 3-level NPC Inverter at High Modulation Index Including Over-modulation Range, with Neutral Point Balancing

The DC-link of the 3-level NPC inverter shown in Fig. 1.2 consists of two capacitors. In ideal condition, these two capacitors equally share the DC-link voltage i.e. $V_{dc}/2$. However, in reality the voltages across these capacitors are not same, leading to degradation of the output voltage waveform and unequal voltage stress on the power semiconductor devices [84]. This problem is known as DC-link fluctuation problem in NPC inverter.

The main cause of the neutral point imbalance is the current at the neutral

point O, Fig. 1.2. The other causes of neutral point potential drift as described by Yamanaka et.al. [85] can be nonuniform switching and non-ideal DC-link capacitors. According to this study, such imbalances can lead to slow but continuous drift of the neutral point potential. Dynamic operating conditions such as acceleration or deceleration of load drives can also result in neutral point potential drift. Under such conditions, these fluctuation can be rapid and significant. To summarize, the neutral point fluctuation can be caused by both the modulation technique and the operating conditions of the inverter. The variation in neutral point voltage depends on the modulation technique used. However, as the output voltage and load current magnitudes increase and power factor (PF) approaches zero, the neutral point potential fluctuation increases. Under such operating conditions, the performance of the 3-level NPC inverter degrades. For a reliable operation of this topology, the neutral point balance should be ensured.

The neutral point fluctuation is directly related to the switching state vectors. For 3-level space vector diagram, the switching vectors can be divided into four types of vectors; zero vector $V_0$, short vectors $V_{Si}$, medium vectors $V_{Mi}$ and large vectors $V_{Li}$, where $i = 1 \rightarrow 6$. The zero vector and large vector do not affect the neutral point balance but the short and medium vectors affect the neutral point. Neutral point balancing techniques normally require appropriate selection of switching states and utilization of their on-times. Since, the SVPWM directly deals with switching states and their on-times, it can be used for neutral point balancing problem.

At higher modulation index, particularly in over-modulation region, the neutral point fluctuation deteriorates the performance of the inverter. Furthermore, operating the inverter at lower modulation index implies that it is operated at lower voltages only, and the installed DC link capacity is not fully utilized. This chapter proposes a simple space vector PWM scheme for operating a 3-level NPC inverter at higher modulation indices including over-modulation range, with neutral point balancing. Experimental and simulation results are provided.

## 6.1 Introduction

In section 1.3.6, the problem of neutral point fluctuation is described and section 1.4.5 reviews the literature on related works. This chapter studies the effect of increasing modulation index on neutral point balance. A simple neutral point balancing scheme is proposed to operate a 3-level NPC inverter at high modulation index including overmodulation range. The scheme is designed to work with Nearest Vector (NV) method when the neutral point fluctuation is within a set tolerance. In case it goes beyond this set tolerance, the proposed Selected Vector (SV) method is used. The salient features of the proposed scheme are as follows,

- The scheme is able to maintain neutral point balance within a specified tolerance, at any modulation index and for wide load variation. Hence, large DC-link capacitors are not required.

- Neutral point voltage fluctuation is the only feedback parameter required to obtain overall good performance, no additional input is required. This is advantageous as many other schemes need phase currents and load power factor to obtain neutral point balancing.
- The volt-sec balance is maintained throughout the scheme.
- The scheme uses simple overmodulation method proposed in chapter 3.
- The scheme is computationally simple and hence can be easily implemented.

The chapter is organized in nine sections. In section 6.2, neutral point fluctuation problem is discussed. Section 6.3 briefly discusses the proposed scheme. Sections 6.4, 6.5, and 6.6 explain the proposed space vector PWM algorithm for linear mode, overmodulation mode-I and overmodulation mode-II respectively. Section 6.7 explains the structure of the scheme. Section 6.8 shows the experimental and simulation results. Section 6.9 concludes the chapter.

## 6.2 Neutral Point Fluctuation Problem

In ideal condition, $V_{C_1}$=$V_{C_2}$=$V_{dc}$/2 (Fig.6.1). However, in reality the voltages $V_{C_1}$ and $V_{C_2}$ can fluctuate significantly. It was mentioned in sections 1.3.6 and 1.4.5 that switching states shown in Fig.6.2 and operating conditions of the inverter such as load PF affect the neutral point balance. This is explained in following sections.

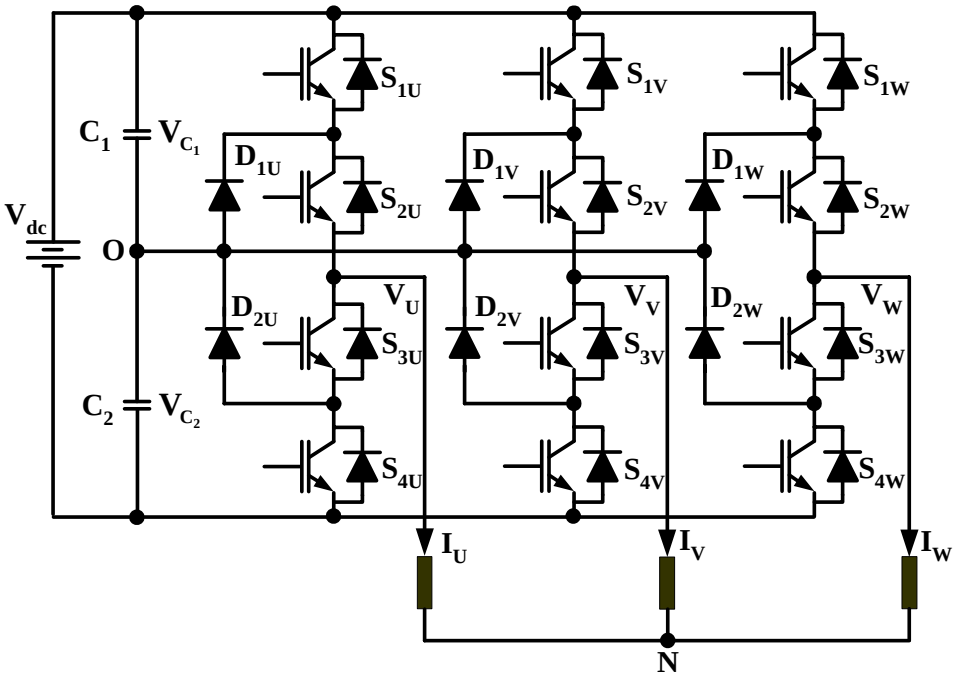



Figure 6.1: Neutral Point Clamped 3-level Inverter

### 6.2.1 Switching Vectors Vs. Neutral Point Fluctuation

The space vector diagram in Fig. 6.2 [119] of a 3-level inverter is made up of 19 switching vectors and 27 switching states. As discussed in section 1.4.5, the switching vectors in Fig. 6.2 can be divided into four type of vectors; zero vector $V_0$, short vectors $V_{Si}$, medium vectors $V_{Mi}$ and large vectors $V_{Li}$, where i = 1→6. This figure also shows the effect of each switching state on the neutral point current. The zero vector and large vector do not affect it. However, short and medium vectors affect the neutral point balance. Any short vector has two switching states. One state increases $V_{C2}$ see Fig.6.1, while the other decreases it as described in [84], [85]. Therefore, by adjusting the duty ratios of these two states, the neutral point fluctuation can be minimized. A medium vector has only one switching

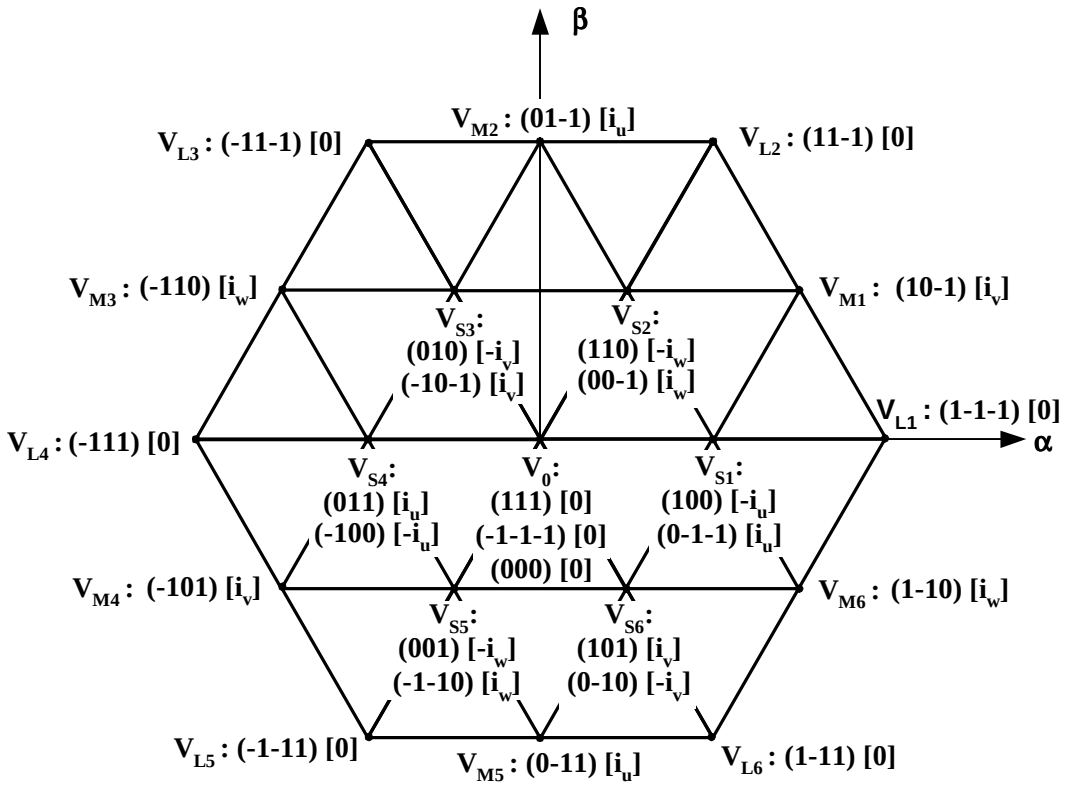



Figure 6.2: Space Vector Diagram of a 3-level Inverter

state. Therefore, unlike short vectors, medium vector does not have neutral point balancing capability.

As only short and medium vectors affect the neutral point fluctuation, it is important to see the variation of their duty ratio with angle. Fig. 6.3 show this variation at different modulation indices for the first sector. Their variation is same for other sectors too. The duty ratios have been calculated based on nearest vector scheme (chapter 2). As modulation index $m_i$ increases, the duty ratio $d_M$ of medium vector keeps on increasing, whereas the duty ratios $d_{S1}$ and $d_{S2}$ of two short vectors keep on reducing, shown in Fig. 6.3(a), (b) and (c). Fig. 6.3(a) and (b) represent linear modulation mode, Fig. 6.3(c) represents overmodulation mode-

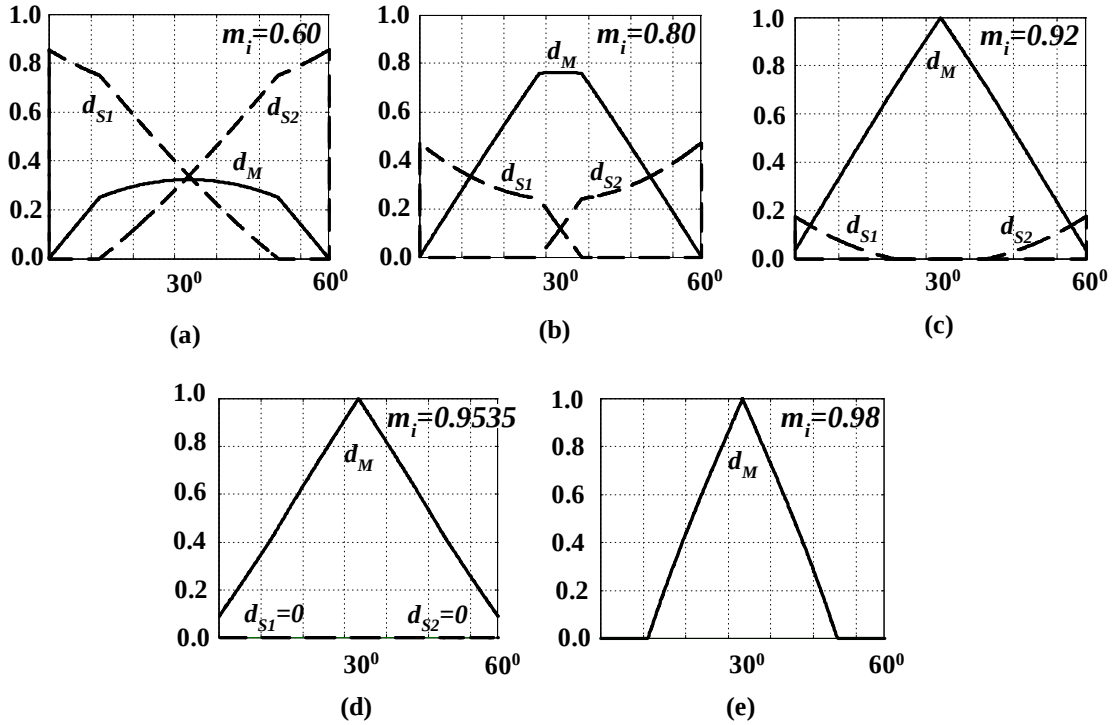



Figure 6.3: Variation of $d_M$, $d_{S1}$ and $d_{S2}$ with angle at (a) $m_i = 0.6$ (b) $m_i = 0.8$ (c) $m_i = 0.92$ (d) $m_i = 0.9535$ (e) $m_i = 0.98$

I, Fig. 6.3(d) represents boundary of overmodulation mode-I and overmodulation mode-II and Fig. 6.3(e) represents the overmodulation mode-II. At $m_i$=0.9535, the duty ratio of short vectors is zero while the effect of medium vector is maximum, therefore neutral point control is poor near $m_i$=0.9535. As $m_i$ increases above 0.9535, medium vector is not switched for certain part of the sector, so the overall effect of large vectors increase and medium vector reduces. Since only medium vector mainly influences neutral point fluctuation in overmodulation-II, the neutral point fluctuation reduces with increase in modulation index. At $m_i$=1.0 only large vectors are effective, hence ideally there is no fluctuation. However, a multilevel inverter when operated at $m_i$=1.0, looses its multilevel characteristics.

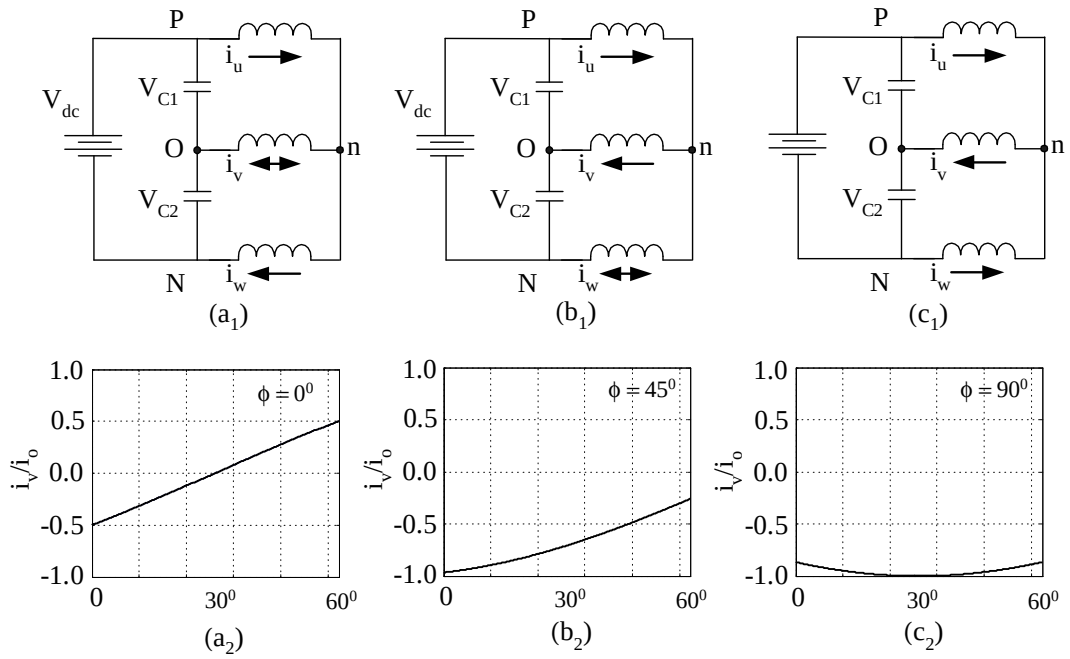



Figure 6.4: The analysis of the effect of medium vector (1,0,-1) $(a_1)(b_1)(c_1)$ Actual circuit connections and current directions at $\phi$=$0^o$, $45^o$ and $90^o$ respectively $(a_2)(b_2)(c_2)$ Neutral point current at $\phi$=$0^o$, $45^o$ and $90^o$ respectively

### 6.2.2 Effect of Varying PF on the Neutral Point Current

To study the effect of PF on neutral point current, let us take the medium vector $V_M$ in the first sector, Fig. 6.2. The corresponding switching state is (1,0,-1). The switching state (1,0,-1) signifies that phase $U$, $V$ and $W$ of the load are connected to positive bus, neutral point 'O' and negative bus respectively. The Fig. 6.4 $(a_1)(b_1)(c_1)$ shows the actual connections with respect to Fig. 6.1.

Assuming sinusoidal nature, the currents $i_u$, $i_v$ and $i_w$ can be given as,

$$\begin{aligned} i_u &= i_o e^{j(\pi/6-\phi)} \\ i_v &= i_o e^{j(\pi/6-\phi-2\pi/3)} \\ i_w &= i_o e^{j(\pi/6-\phi-4\pi/3)} \end{aligned} \tag{6.1}$$

In (6.1), $\phi$ is power factor angle and $i_o$ is load current. The current $i_o$ will depend on the actual DC-link voltage, modulation index and type of load. Current $i_v$ will be the neutral point current for the switching state (1,0,-1). Current $i_v$ can be normalized with respect to $i_o$ to study the variation of normalized $i_v$ with respect to $\phi$. Fig. 6.4($a_2$)($b_2$)($c_2$) show the variation of $i_v/i_o$ with respect to $\phi$.

Fig. 6.4($a_2$) shows that average neutral point current per sector is zero at $\phi$=$0^o$. Therefore for $\phi$=$0^o$, neutral point fluctuation will not be affected much even at high modulation index. However, as $\phi$ increases, the average neutral point current per sector also increases as seen in Fig. 6.4($b_2$). The maximum average current is at $\phi$=$90^o$, Fig. 6.4($c_2$). This is the most unfavorable condition for neutral point balancing. The same can be explained when $\phi$ changes from 0 to -$90^o$ but the average current will be positive in this case.

## 6.3 Proposed Scheme

The fluctuation of the neutral point is defined with a parameter *npf* as,

$$npf = abs\left(\frac{V_{dc}/2 - V_{C2}}{V_{dc}/2}\right) * 100 = abs\left(1 - \frac{2 * V_{C2}}{V_{dc}}\right) * 100 \qquad (6.2)$$

In (6.2) *abs* stands for the absolute value i.e. only the magnitude of fluctuation is considered. The *npf* is the percentage fluctuation of the neutral point with respect to half of the DC-link voltage. It is a dimensionless quantity and indepen-

dent of the magnitude of DC-link voltage $V_{dc}$. Its maximum permissible value can be represented as $npf_{max}$ which is fixed by desired performance. It is the key input parameter to the balancing scheme.

As discussed before, neutral point balance depends on the switching states. The switching states in a given switching cycle depend on the modulation index or the trajectory of the vector. Hence, let us restate some useful characteristics for the trajectory of the reference vector in linear and overmodulation modes. In linear mode, the control vector moves on a circular trajectory. In overmodulation I, the control vector moves on a circular trajectory for some part of the sector. For remaining part of the sector, it moves on a side of the 3-level hexagon i.e. $\mathrm{V}_{L1}\mathrm{V}_{L2}$ in Fig. 6.2 called hexagonal trajectory. In overmodulation II, for central part of the sector, control vector moves on a hexagonal trajectory while for the remaining part it is held at one of the six vertices of hexagon. Hence, there are three possible trajectories of the control vector; circular, hexagonal or discrete.

The movement of the control vector along the circular and hexagonal trajectories affect the neutral point balance. Let us briefly discuss the effect of traditional space vector PWM on neutral point balance for circular and hexagonal trajectories. For the circular trajectory, nearest three vector (N3V) scheme is used as discussed in chapter 2. In N3V, the switching states corresponding to the three vertices of a triangle [94] are switched in every switching period. For the hexagonal trajectory, nearest two vectors [94] are switched in every switching period, called N2V

scheme, discussed in chapter 3. Combination of N3V and N2V schemes is called as nearest vector (NV) scheme in this thesis. In chapter 2 and 3, a detailed SVPWM implementation of NV scheme is shown for 3-level NPC inverter.

At high modulation index and poor PF condition, the NV scheme can lead to large neutral point fluctuation. In such condition, a different scheme is proposed for neutral point balancing. In the proposed scheme, the medium vector is not switched under unbalanced neutral condition. This scheme is called as 'selected vector (SV) scheme'. Similar to NV scheme, in SV scheme also, a Selected Three Vector (S3V) scheme is used for the circular trajectory while a selected two Vector (S2V) scheme used for the hexagonal trajectory. In S3V scheme, three suitable vectors are selected and in S2V scheme two suitable vectors are selected per switching period. The selected vectors should be able to compensate for the neutral point fluctuation.

A combination of NV and SV schemes can provide an overall better performance. The NV and SV schemes for the three modulation modes are described in the following sections. The scheme is explained only for the first sector and it is valid for other sectors too. The explanation will focus the range $0.6 \leq m_i < 1.0$ where the neutral point fluctuation is a concern .

## 6.4 Linear Modulation Mode ($m_i$<0.907)

In this mode, the control vector $\boldsymbol{v}^*$ moves on a circular trajectory as shown in Fig. 6.5. In Fig. 6.5 control vector $\boldsymbol{v}^*$ ($V_0P$) makes an angle $\gamma$ with the $\alpha$ axis. Here, $\gamma$ ($0 \leq \gamma \leq 60^o$) is angle within the sector. The N3V and S3V schemes for this mode are discussed below.

### 6.4.1 N3V Scheme

The algorithm described in chapter 2 is essentially the N3V scheme. For $0.6 \leq m_i < 0.907$, the control vector will be located within one of the triangles i.e. $\triangle_1$ ($V_{S1}V_{L1}V_{M1}$), $\triangle_2$ ($V_{S1}V_{M1}V_{S2}$) or $\triangle_3$ ($V_{S2}V_{M1}V_{L2}$) shown in Fig. 6.5(a). The determination of on-times and triangle number $\triangle_j$ can be referred in chapter 2.

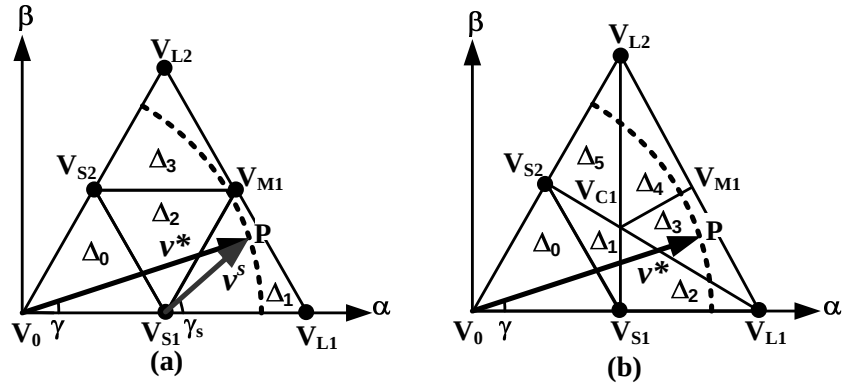



Figure 6.5: Space Vector Diagram of the first sector of a 3-level inverter to show linear mode for (a) N3V Scheme (b) S3V Scheme

In Fig. 6.5(a), $\triangle_1$: $V_{S1}V_{L1}V_{M1}$ signifies that when the control vector lies within triangle $\triangle_1$ the switching vectors $V_{S1}$,$V_{L1}$ and $V_{M1}$ are switched. The

possible switching sequence include (0,-1,-1), (1,-1,-1), (1,0,-1) and (1,0,0) with the corresponding duty ratios of $d_{S1+}$, $d_{L1}$, $d_{M1}$ and $d_{S1-}$. Here, $d_{S1+}+d_{S1-}=d_{S1}$. Therefore, by adjusting the magnitude of $d_{S1+}$ and $d_{S1-}$, the neutral point fluctuation can be controlled [91]. The same can be explained for other triangles.

### 6.4.2 S3V Scheme

The region $V_{S1}V_{L1}V_{M1}V_{L2}V_{S2}V_{S1}$ in Fig. 6.5(b) is divided into five triangles $\triangle_1 (V_{C1}V_{S2}V_{S1})$, $\triangle_2 (V_{C1}V_{S1}V_{L1})$, $\triangle_3 (V_{C1}V_{L1}V_{M1})$, $\triangle_4 (V_{C1}V_{M1}V_{L2})$ and $\triangle_5 (V_{C1}V_{L2}V_{S2})$. Point $V_{C1}$ in Fig. 6.5(b) is centroid of the sector, and it does not represent any switching vector. For $0.6 \leq m_i < 0.907$, the control vector will be located in either of the four triangles $\triangle_2 \rightarrow \triangle_5$.

In Fig. 6.5(b), $\triangle_3 : V_{S1}V_{L1}V_{L2}$ signifies that when the control vector lies in triangle $\triangle_3$, switching vectors $V_{S1}$, $V_{L1}$ and $V_{L2}$ are switched. Such a selection will help in obtaining the neutral point balance. The possible switching sequence includes (0,-1,-1), (1,-1,-1), (1,1,-1) and (1,0,0) with the corresponding duty ratios of $d_{S1+}$, $d_{L1}$, $d_{L2}$ and $d_{S1-}$. Here, $d_{S1+}+d_{S1-}=d_{S1}$. Therefore by adjusting the magnitude of $d_{S1+}$ and $d_{S1-}$, the neutral point fluctuation can be controlled.

In Fig. 6.5(b), line segments $V_{G1}V_{L1}$, $V_{G1}V_{M1}$ and $V_{G1}V_{L2}$ are boundaries between the triangles $\triangle_2 \rightarrow \triangle_5$. Line segments $V_{G1}V_{L1}$, $V_{G1}V_{M1}$ and $V_{G1}V_{L2}$ can be given as $v_\alpha + \sqrt{3}v_\beta = 2$, $\gamma = 30^o$ and $v_\alpha = 1$ respectively. The triangle number $\triangle_j$ and duty ratios can be easily determined using these three line segments and the

| $\Delta_j$ | $\Delta_2$ | | | | | $\Delta_3$ | | | | $\Delta_4$ | | | | $\Delta_5$ | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| d.r. | $d_{S2-}$ | $d_{S1-}$ | $d_{L1}$ | $d_{S1+}$ | $d_{S2+}$ | $d_{S1-}$ | $d_{L1}$ | $d_{L2}$ | $d_{S1+}$ | $d_{S2-}$ | $d_{L1}$ | $d_{L2}$ | $d_{S2+}$ | $d_{S1-}$ | $d_{S2-}$ | $d_{L2}$ | $d_{S2+}$ | $d_{S1+}$ |
| $s_u$ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| $s_v$ | 0 | -1 | -1 | 0 | 1 | -1 | -1 | 1 | 0 | 0 | -1 | 1 | 1 | -1 | 0 | 1 | 1 | 0 |
| $s_w$ | -1 | -1 | -1 | 0 | 0 | -1 | -1 | -1 | 0 | -1 | -1 | -1 | 0 | -1 | -1 | -1 | 0 | 0 |

Table 6.1: Implementation of S3V scheme for the first sector

tip $(v_\alpha, v_\beta)$ of $V_0P$ as explained below.

If the inequalities $\gamma \leq 30^o$ and $v_\alpha + \sqrt{3}v_\beta \leq 2$ are true, then the point P is in triangle $\triangle_2$ and duty ratios are obtained using

$$\begin{aligned} d_{V_{S_1}} &= 2 - v_\alpha - \sqrt{3}v_\beta \\ d_{V_{S_2}} &= v_\beta / h \\ d_{V_{L_1}} &= 1 - d_{V_{S_1}} - d_{V_{S_2}} \end{aligned} \tag{6.3}$$

Or if the inequalities $\gamma \leq 30^o$ and $v_\alpha + \sqrt{3}v_\beta > 2$ are true, then the point P is in triangle $\triangle_3$ and duty ratios are obtained using

$$\begin{aligned} d_{V_{L_1}} &= -1 + v_\alpha \\ d_{V_{L_2}} &= v_\beta / \sqrt{3} \\ d_{V_{S_1}} &= 1 - d_{V_{L_1}} - d_{V_{L_2}} \end{aligned} \tag{6.4}$$

If the inequalities $\gamma > 30^o$ and $v_\alpha \geq 1$ are true, then the point P is in triangle $\triangle_4$ and duty ratios are obtained using

$$\begin{aligned} d_{V_{S_2}} &= 2 - v_\alpha - v_\beta / \sqrt{3} \\ d_{V_{L_1}} &= 0.5(v_\alpha - v_\beta / \sqrt{3}) \\ d_{V_{L_2}} &= 1 - d_{V_{S_2}} - d_{V_{L_1}} \end{aligned} \tag{6.5}$$

Or if the inequalities $\gamma > 30^o$ and $v_\alpha < 1$ are true, then the point P is in triangle

$\triangle_5$ and duty ratios are obtained using

$$\begin{aligned} d_{V_{S_1}} &= v_\alpha - v_\beta/\sqrt{3} \\ d_{V_{S_2}} &= 2 - 2v_\alpha \\ d_{V_{L_2}} &= 1 - d_{V_{S_1}} - d_{V_{S_2}} \end{aligned} \tag{6.6}$$

Section 4.2.2.1 shows duty ratio calculation for a non-equilateral triangle using volt-sec balance equations. The same approach is followed to obtain the duty ratios for triangles $\triangle_2 \rightarrow \triangle_5$. The resulting expressions are shown in (6.3)$\rightarrow$(6.6). For a given control vector, only one of the four equations is used. These equations remain valid for other five sectors too. For a given control vector, approximately two logical operations, two multiplications and six addition or subtraction operations are required to determine the triangle number $\triangle_j$ and duty ratios. These computations show the computational simplicity of the S3V scheme.

The scheme proposed by [119] uses point $V_{C1}$ as a virtual vector. The virtual vector $V_{C1}$ is used with equal duty ratios of vectors $V_{S1}$, $V_{S2}$ and $V_{M1}$, in order to keep the neutral point current zero. Referring to Fig. 6.5(b), for triangles $\triangle_2$ and $\triangle_5$, scheme [119] works as a nearest four vector scheme, and for the triangles $\triangle_3$ and $\triangle_4$, it works as a nearest five vector scheme, leading to higher distortion. Ideally there should not be any imbalance using [119]. However, in practical situations, there could be some unbalance due to problems mentioned in section 6.1. Such unbalance is difficult to eliminate using [119]. However, in the proposed scheme, the duty ratios of the short vectors $V_{S1}$ and $V_{S2}$ can be adjusted unlike [119]. Therefore, the neutral point fluctuation can be fully controlled.

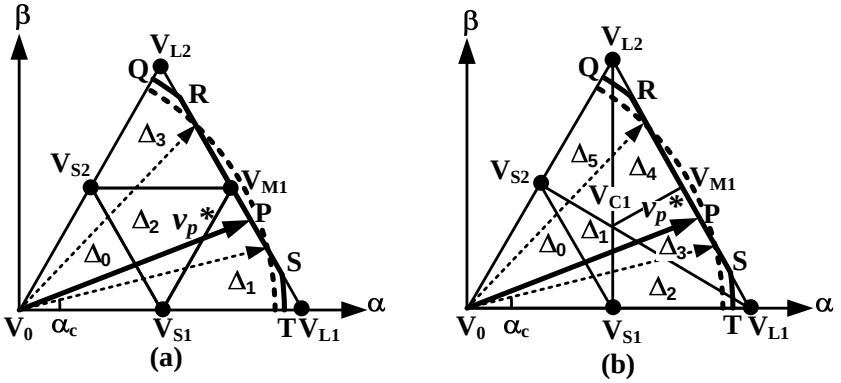
For triangles $\triangle_2$ and $\triangle_5$, the switching losses in the proposed S3V scheme are 4/3 times the switching losses for N3V scheme. Where as for the triangles $\triangle_3$ and $\triangle_4$, the switching losses in the proposed S3V scheme are 5/3 times the switching losses for N3V scheme.

Hence, in order to control the neutral point fluctuation, the distortion and switching losses are higher, when the S3V scheme is used for the circular track. This is normal for any similar scheme [119]. However, it will be shown that using a combination of N3V and S3V schemes the total distortion can be reduced. This scheme is extended to overmodulation range in next two sections.

## 6.5 Overmodulation Mode - I ($0.907 \leq m_i < 0.9535$)

In Fig. 6.6, the dashed circle shows the desired trajectory of the control vector. Traditionally, depending on the modulation index, the trajectory is modified and tip P of the actual vector moves on trajectory $TSV_{M1}RQ$ shown in thick solid lines. First, it moves along the circular track $TS$, then along the linear track $SV_{M1}R$ on the side $V_{L1}V_{L2}$ of the sector $V_0V_{L1}V_{L2}$ and finally along the circular track $RQ$. The actual control vector i.e. modified control vector is represented as $\boldsymbol{v_p^*}$.

The overmodulation technique described in chapter 3 is used here i.e. the loss in volt-secs is compensated by directly modifying the duty ratios of the switching vectors. If $\alpha_c$ is the angle where the control vector intersects the hexagon shown




**Circular Trajectory**

$\Delta_1$: $V_{S1}$,$V_{L1}$,$V_{M1}$ $\Delta_3$: $V_{S2}$,$V_{M1}$,$V_{L2}$

**Linear Trajectory**

$\Delta_1$: $V_{L1}$,$V_{M1}$ $\Delta_3$: $V_{M1}$,$V_{L2}$

**Circular Trajectory**

$\Delta_2$: $V_{S1}$,$V_{L1}$,$V_{S2}$ $\Delta_3$ : $V_{S1}$,$V_{L1}$,$V_{L2}$

$\Delta_4$: $V_{S2}$,$V_{L1}$,$V_{L2}$ $\Delta_5$ : $V_{S1}$,$V_{S2}$,$V_{L2}$

**Linear Trajectory**

$\Delta_3$: $V_{L1}$,$V_{L2}$ $\Delta_4$ : $V_{L1}$,$V_{L2}$

Figure 6.6: Space Vector Diagram of the first sector of a 3-level inverter to show overmodulation mode-I for (a) N3V + N2V Scheme (b) S3V+S2V Scheme

by the dotted arrow in Fig. 6.6, then during $\alpha_c \leq \gamma < \pi/3\text{-}\alpha_c$ the vector moves on the hexagonal trajectory and for remaining part of the sector on a circular trajectory. Angle $\alpha_c$ is obtained using (3.2).

Calculation of duty ratios for the circular and hexagonal portions of the trajectory requires different approaches. They are described below.

### 6.5.1 Circular Portion ($0 \leq \gamma < \alpha_c$ and $\pi/3\text{-}\alpha_c \leq \gamma < \pi/3$)

During the circular portion, N3V or S3V scheme can be followed depending on the neutral point fluctuation, see Fig. 6.6. The volt-secs are lost during the hexagonal portion, and have to be compensated during the circular portion. In order to do so, the duty ratios are modified during the circular portion.

#### 6.5.1.1 N3V Scheme

The tip of the control vector can be within triangle $\triangle_1$ or $\triangle_3$ see Fig. 6.6(a). The duty ratios $d_a$, $d_b$ and $d_o$ of the three associated switching vectors are calculated using (2.5)→(2.7). Here $d_a$ and $d_b$ are the duty ratios of the two vertices which are on the side of the hexagon i.e. $V_{L1}V_{L2}$. They are modified as

$$\begin{aligned} d_{am} &= d_a + 0.5\lambda d_o \\ d_{bm} &= d_b + 0.5\lambda d_o \\ d_{om} &= 1 - d_{am} - d_{bm} \end{aligned} \tag{6.7}$$

Where $d_{am}$, $d_{bm}$ and $d_{om}$ are modified duty ratios. The parameter $\lambda$ is compensation factor and obtained using (3.6).

Fig. 6.6(a) shows the selection of switching vectors for the circular trajectory in overmodulation-I for N3V scheme. This is same as that in circular trajectory in linear mode, shown in Fig. 6.5(a).

#### 6.5.1.2 S3V Scheme

The tip of the vector can be within triangles $\triangle_2$→$\triangle_5$ see Fig. 6.6(b). The duty ratios of the three associated switching vectors are calculated using (6.3)→(6.6). The aforementioned modification in duty ratios is carried out as follows.

For triangle $\triangle_2$, the modifications are obtained as

$$\begin{aligned} d_{V_{S_1m}} &= d_{V_{S_1}} - 0.5\lambda d_{V_{S_1}} \\ d_{V_{S_2m}} &= d_{V_{S_2}} - 0.5\lambda d_{V_{S_2}} \\ d_{V_{L_1m}} &= 1 - d_{V_{S_1m}} - d_{V_{S_2m}} \end{aligned} \tag{6.8}$$

The similar modification is done for triangle $\triangle_5$ as well.

For triangle $\triangle_3$, the modifications are obtained as

$$\begin{aligned} d_{V_{L_1m}} &= d_{V_{L_1}} + 0.5\lambda d_{V_{S_1}} \\ d_{V_{L_2m}} &= d_{V_{L_2}} + 0.5\lambda d_{V_{S_1}} \\ d_{V_{S_1m}} &= 1 - d_{V_{L_1m}} - d_{V_{L_2m}} \end{aligned} \tag{6.9}$$

The similar modification is done for triangle $\triangle_4$ as well.

For (6.8) and (6.9), $\lambda$ is defined by (3.6) and $m$ stands for modified.

Hence, similar to linear mode, in overmodulation mode-I also the duty ratios of the small vectors can be adjusted to obtain the neutral point balance.

Fig. 6.6(b) also shows the selection of switching vectors for the circular trajectory in overmodulation-I for S3V scheme which is same as that in circular trajectory in linear mode, as in Fig. 6.5(b).

### 6.5.2 Hexagonal Portion ($\alpha_c \leq \gamma < \pi/3\text{-}\alpha_c$)

During linear portion, two switching states are executed in a switching period. Depending on the neutral point fluctuation, two different methods of selecting

the switching vectors are proposed to use, namely nearest two vectors (N2V) and selected two vectors (S2V) schemes.

#### 6.5.2.1 N2V Scheme

For N2V scheme as shown below Fig. 6.6(a), the switching vectors $V_{L1}$ (1,-1,-1) and $V_{M1}$ (1,0,-1) are selected for triangle $\triangle_1$, and switching vectors $V_{M1}$ (1,0,-1) and $V_{L2}$ (1,1,-1) are selected for triangle $\triangle_3$.

The duty ratios and triangle $\triangle_j$ can be determined using angle $\gamma$.

In Fig. 6.6(a) if $\gamma \leq 30^o$ is true, then point P is on triangle $\triangle_1$ and the duty ratios are obtained as

$$\begin{aligned} d_{V_{L_1}} &= \left(\sqrt{3} - 3\tan\gamma\right) \Big/ \left(\sqrt{3} + \tan\gamma\right) \\ d_{V_{M_1}} &= 1 - d_{V_{L_1}} \end{aligned} \tag{6.10}$$

In Fig. 6.6(a) if $\gamma > 30^o$ is true, then point P is on triangle $\triangle_3$ and the duty ratios are obtained as

$$\begin{aligned} d_{V_{M_1}} &= 2\left(\sqrt{3} - \tan\gamma\right) \Big/ \left(\sqrt{3} + \tan\gamma\right) \\ d_{V_{L_2}} &= 1 - d_{V_{M_1}} \end{aligned} \tag{6.11}$$

#### 6.5.2.2 S2V Scheme

For the S2V scheme as shown below Fig. 6.6(b), irrespective of the location of point P, switching vectors $V_{L1}$ and $V_{L2}$ are selected. Therefore, the determination of triangle number is not required. The duty ratios of these two vectors are

determined using angle $\gamma$ as follows

$$\begin{aligned} d_{V_{L_1}} &= \left(\sqrt{3} - \tan\gamma\right) \Big/ \left(\sqrt{3} + \tan\gamma\right) \\ d_{V_{L_2}} &= 1 - d_{V_{L_1}} \end{aligned} \tag{6.12}$$

Equations (6.10)→(6.12) are obtained using volt-secs balance. They remain valid for others sectors too.

## 6.6 Overmodulation Mode II ($0.9535 \leq m_i$)

When modulation index increases above 0.9535, the circular part of the trajectory vanishes. Switching in overmodulation II is characterized by a hold angle $\alpha_h$, shown by the dotted arrow in Fig. 6.7. Normally, $\alpha_h$ is a nonlinear function of modulation index and obtained by a lookup table. In this chapter, the hold angle $\alpha_h$ is obtained using (3.10).

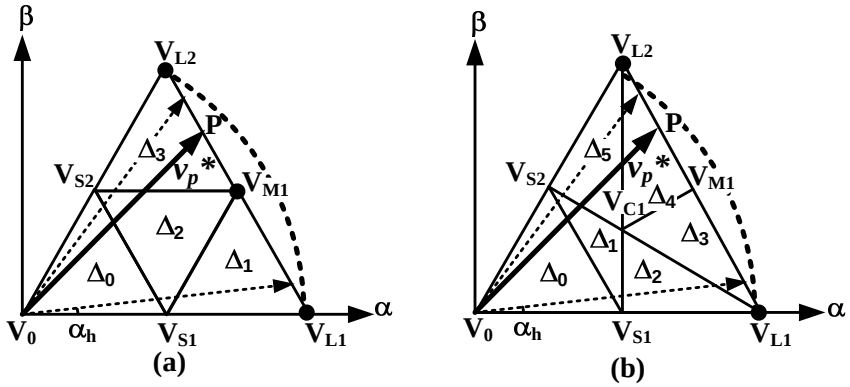



Figure 6.7: Space Vector Diagram of the first sector of a 3-level inverter to show overmodulation mode-II for (a) N2V Scheme + Discrete Movement (b) S2V Scheme + Discrete Movement

During $\alpha_h \leq \gamma < \pi/3\text{-}\alpha_h$, the tip P of the vector $\boldsymbol{v}_{\boldsymbol{p}}^{*}$ moves on a linear track i.e. side $V_{L1}V_{L2}$ of the sector. For hexagonal trajectory, N2V or S2V scheme is followed depending on the value of $npf$. The on-time calculation is same as that during the hexagonal trajectory in overmodulation-I for full switching period.

During $0 \leq \gamma < \alpha_h$ and $\pi/3\text{-}\alpha_h \leq \gamma < \pi/3$, the control vector is held at one of the six vertices of the hexagon for full switching period. It is called discrete movement.

During the linear track in overmodulation-II see Fig. 6.7, the switching vectors are selected similar to that for linear track in overmodulation-I as shown in Fig. 6.6.

## 6.7 Structure of the Scheme

The operation of NV and SV schemes is explained in sections 6.4→6.6. Depending on the fluctuation one of the two schemes can be used as shown in flowchart in Fig. 6.8 and block diagram in Fig. 6.9. Let the actual neutral point fluctuation be $npf$ given by (6.2) and its maximum permissible value be $npf_{max}$. If $npf \leq npf_{max}$ then NV scheme is used otherwise SV scheme is used.

In Fig. 6.9, the $V_{C2}$ and $V_{dc}$ are measured from the DC link and $npf$ is calculated using (6.2). In Fig. 6.9, d.r. stands for duty ratios. The block diagram in Fig. 6.9 consists of two main units namely control unit and mapping unit which is same as described in chapter 2 and 3. Control unit determines the sector number

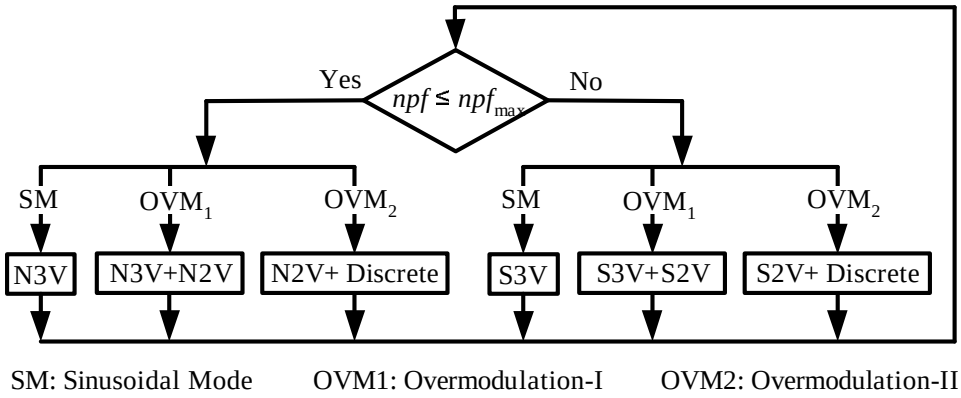



Figure 6.8: Flowchart of the balancing scheme

$S_i$, triangle number $\triangle_j$ and duty ratios for NV and SV schemes. These parameters are given to mapping unit for every switching period. Mapping unit maps to actual switching sequence based on the parameters from control unit. Switching sequence outputs the relevant switching states and thus the gate pulses for the inverter are generated.

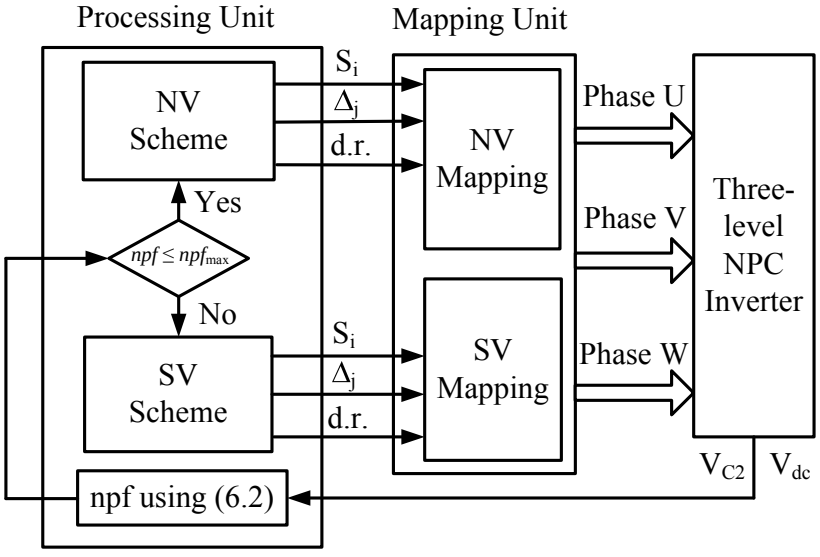



Figure 6.9: Block diagram of the balancing scheme

## 6.8 Experimental and Simulation Results

The algorithm is implemented on a dSPACE DS1104 card with fixed point calculation. Owing to the simplicity of the algorithm, it can be easily implemented on a fixed point DSP. The algorithm is tested on a laboratory prototype of 3-level NPC inverter. The test was performed on a star connected RL load of load inductance per phase 0.46H and load resistance per phase 48.4 Ω at $V_{dc}$=170V, fundamental frequency $f$=50Hz and sampling frequency $f_s$=5kHz.

The weighted total harmonic distortion $V_{WTHD}$ [124] for the NV and SV schemes is compared in Fig. 6.10. This figure shows variation of percentage $V_{WTHD}$ with the modulation index $m_i$. Here, percentage $V_{WTHD}$ for the range $0.0 \leq m_i < 0.6$ is not included, as the balance in this range can be easily achieved [84] using the conventional N3V scheme.

As expected from Fig. 6.5(b)-6.7(b) and obtained in Fig. 6.10, the SV scheme will have higher harmonic distortion compared to NV scheme. However, using a combination of the NV and SV scheme, the harmonic distortion obtained is between that obtained with NV and SV schemes, shown by the 'x' data points in Fig. 6.10.

Fig. 6.11 shows experimental results at $m_i$=0.87 corresponding to the linear mode at the aforementioned experimental conditions. Fig. 6.11 ($a_1$) shows $V_{UV}$ and $I_W$ with respect to NV scheme. Fig. 6.11 ($a_2$) shows corresponding neutral point

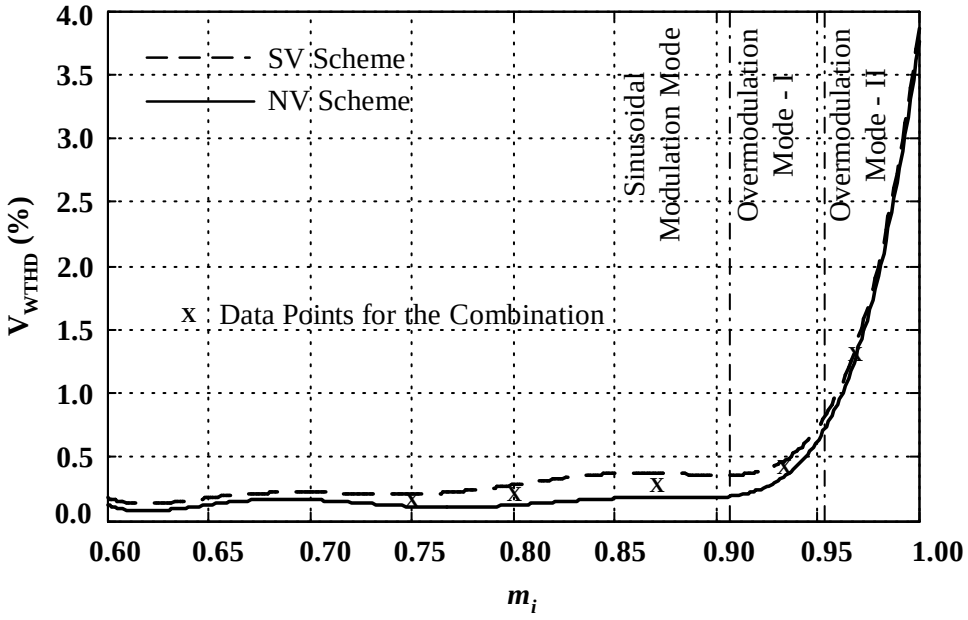



Figure 6.10: Modulation index $m_i$ versus percentage $V_{WTHD}$

fluctuation $npf$ and FFT of $V_{UV}$ corresponding to Fig. 6.11 ($a_1$). At the experimental conditions, the $V_{C2}$ is about 88.3 V. Hence, the $npf$ obtained is 4% using (6.2). The weighted total harmonic distortion $V_{WTHD}$ for this spectrum is 0.135 %. $V_{UV1}$ is fundamental component of line voltage. Fig. 6.11 ($b_1$), ($b_2$) shows the result of purely SV scheme, $V_{C2}$ is about 85.2V and $npf$ =0.25 % using (6.2). Using the SV scheme, for the loads with poor pf also, precise control of neutral point is obtained by adjusting the duty ratios of short vectors. The $V_{WTHD}$ for this spectrum is 0.323 %. Fig. 6.11 ($c_1$), ($c_2$) shows the results for the combination of NV and SV with $npf_{max}$ = 2.5%. The voltage waveform obtained for Fig. 6.11 ($c_1$) appears similar to Fig. 6.11 ($b_1$). However, the lower $V_{WTHD}$ with respect to Fig. 6.11 ($b_2$) and lower fluctuation with respect to Fig. 6.11 ($a_2$) shows the superior results using combination of the NV and SV schemes.

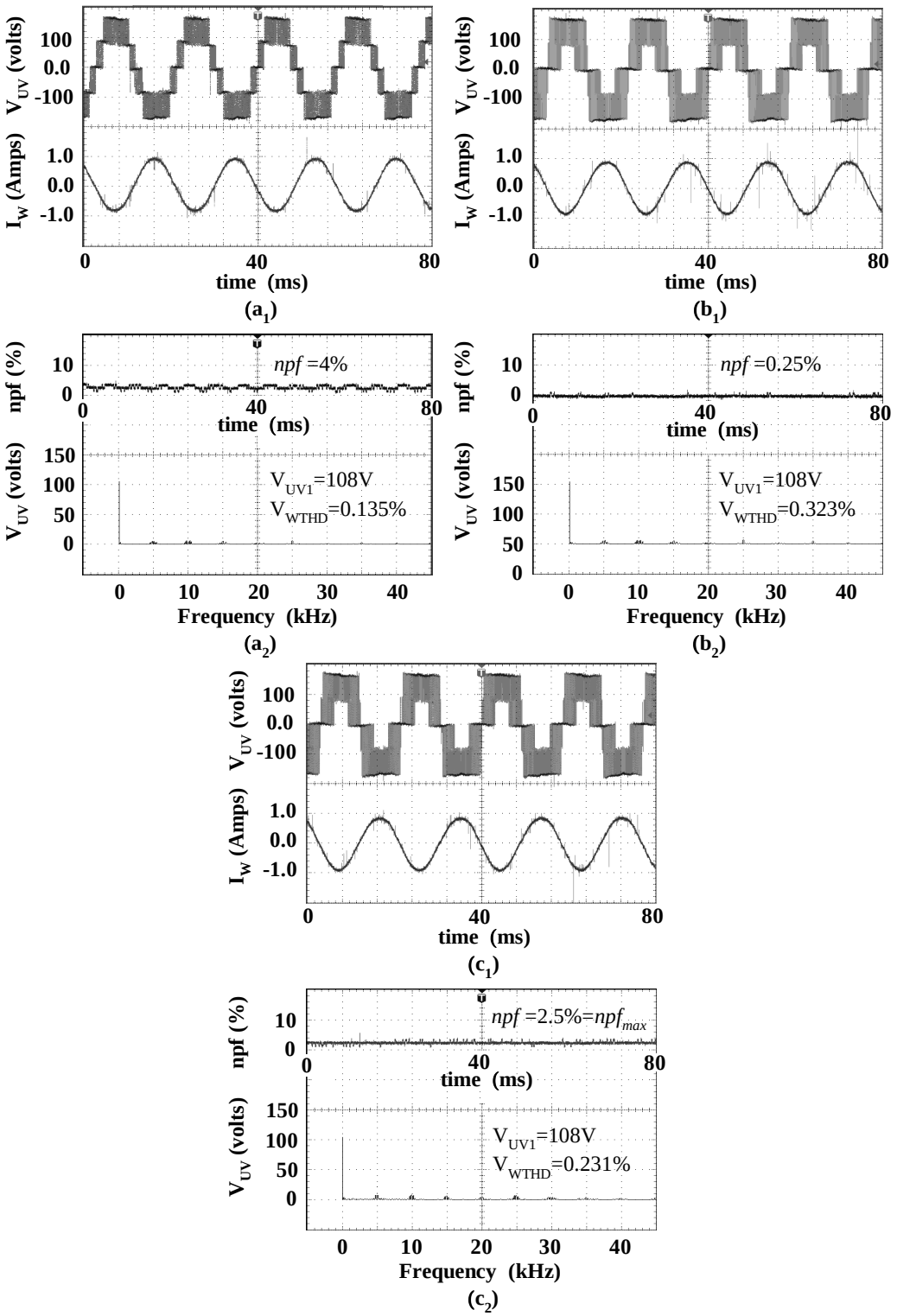



Figure 6.11: At $m_i$=0.87 ($a_1$) $V_{UV}$ and $I_W$ for NV scheme ($a_2$) $npf$ and FFT for NV scheme ($b_1$) $V_{UV}$ and $I_W$ for SV scheme ($b_2$) $npf$ and FFT for SV scheme ($c_1$) $V_{UV}$ and $I_W$ for NV + SV scheme ($c_2$) $npf$ and FFT for NV + SV scheme

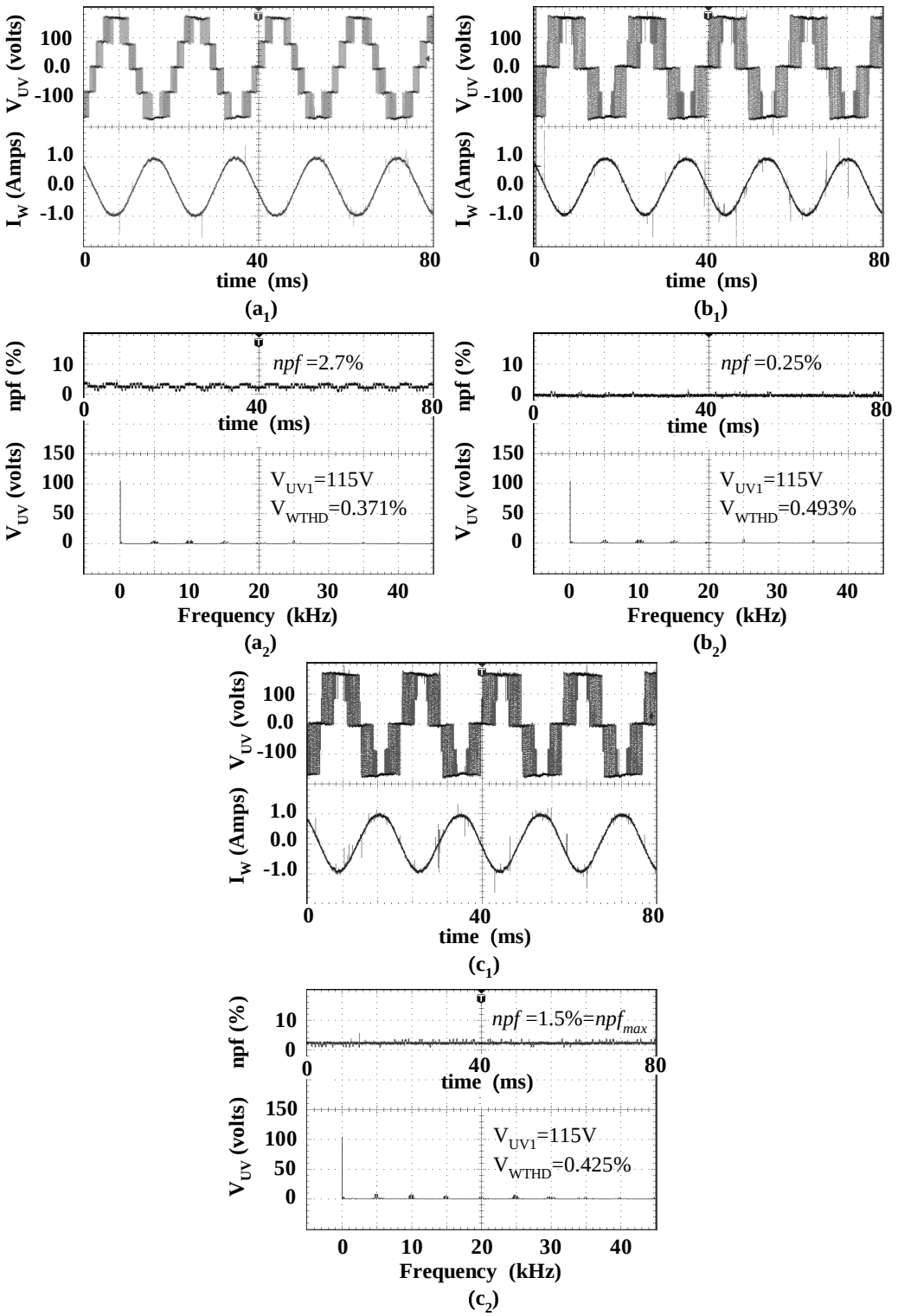



Figure 6.12: At $m_i$=0.93 ($a_1$) $V_{UV}$ and $I_W$ for NV scheme ($a_2$) $npf$ and FFT for NV scheme ($b_1$) $V_{UV}$ and $I_W$ for SV scheme ($b_2$) $npf$ and FFT for SV scheme ($c_1$) $V_{UV}$ and $I_W$ for NV + SV scheme ($c_2$) $npf$ and FFT for NV + SV scheme

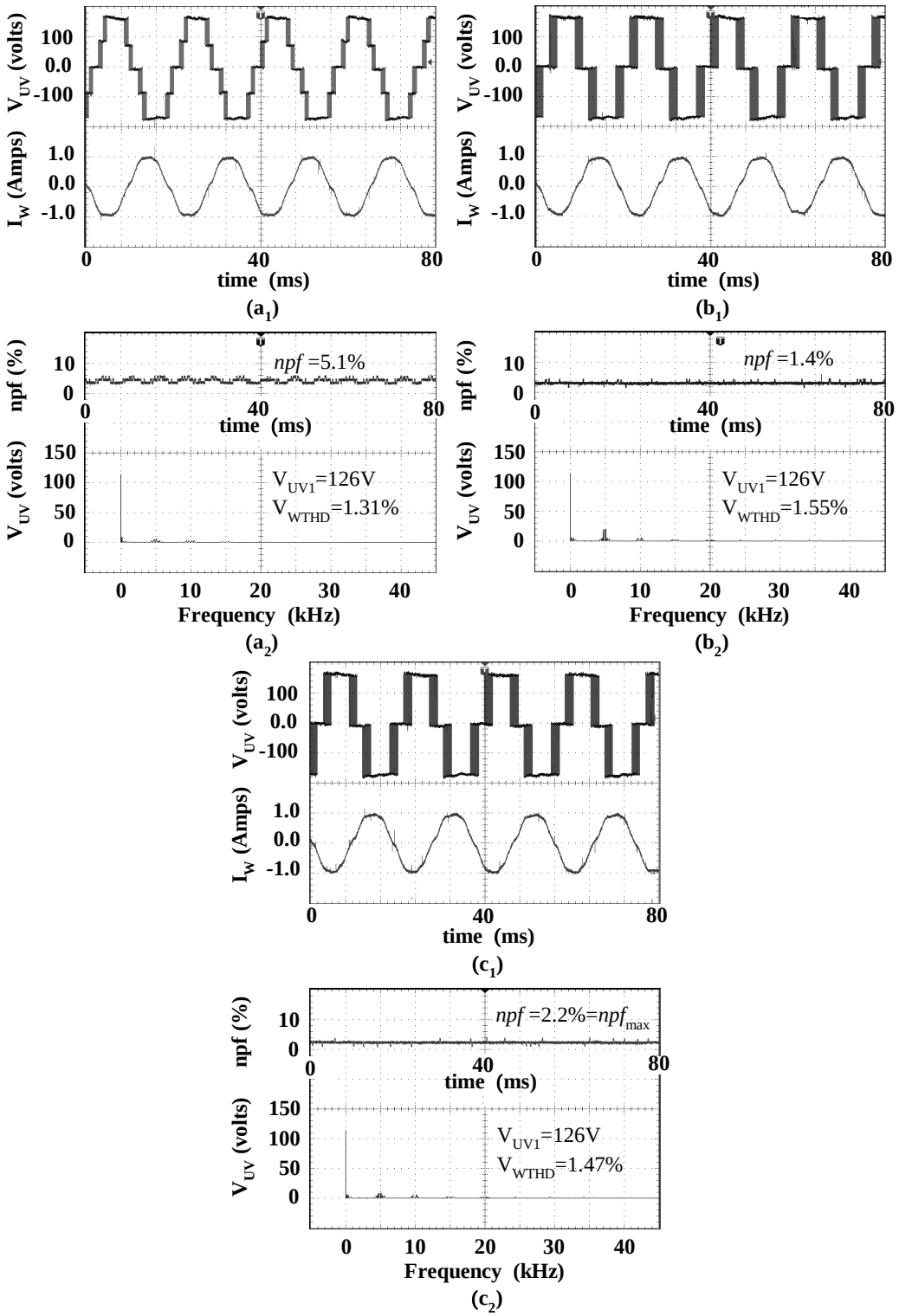



Figure 6.13: At $m_i$=0.97 ($a_1$) $V_{UV}$ and $I_W$ for NV scheme ($a_2$) $npf$ and FFT for NV scheme ($b_1$) $V_{UV}$ and $I_W$ for SV scheme ($b_2$) $npf$ and FFT for SV scheme ($c_1$) $V_{UV}$ and $I_W$ for NV + SV scheme ($c_2$) $npf$ and FFT for NV + SV scheme

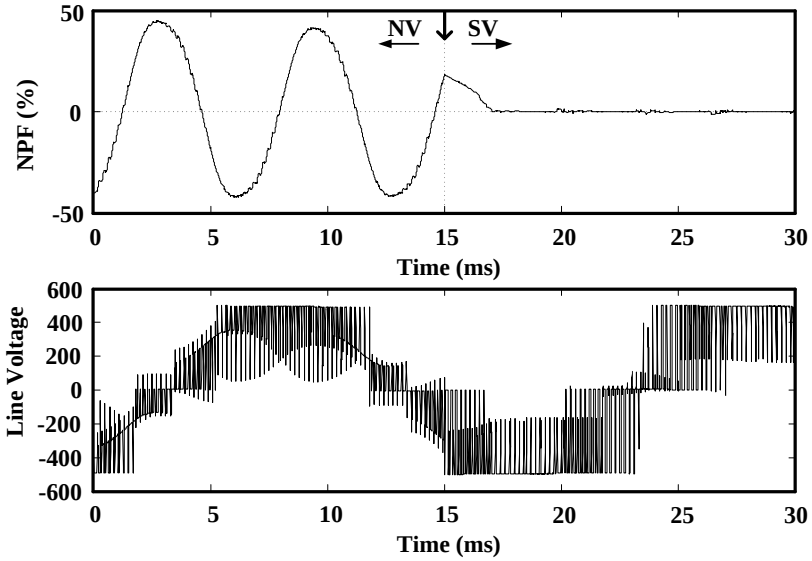



Figure 6.14: At $m_i$=0.9 transition from NV→SV scheme at t=15ms

Fig. 6.12 shows the results at $m_i$=0.93 corresponding to the overmodulation mode-I. Other explanation for Fig. 6.11 remains valid here as well.

Fig. 6.13 shows the results at $m_i$=0.97 corresponding to the overmodulation mode-II. Explanation for Fig. 6.11 remain valid here as well. In overmodulation-II, the duty ratios of small vectors are zero. For the experimental setup, the $npf$ obtained for NV scheme is about 5.1% and for the SV scheme is about 1.4%. In Fig. 6.13 $(c_1), (c_2)$, the $npf_{max}$ is set to 2.2%.

In Fig. 6.12 and 6.13, the $V_{WTHD}$ is higher due to the dominance of lower order harmonics.

Fig.6.14-Fig.6.19 show simulation results for dynamic condition using Matlab & Simulink. The simulation results are at $f$=50Hz, $f_s$=5kHz, $C_1$=$C_2$=400$\mu$F for

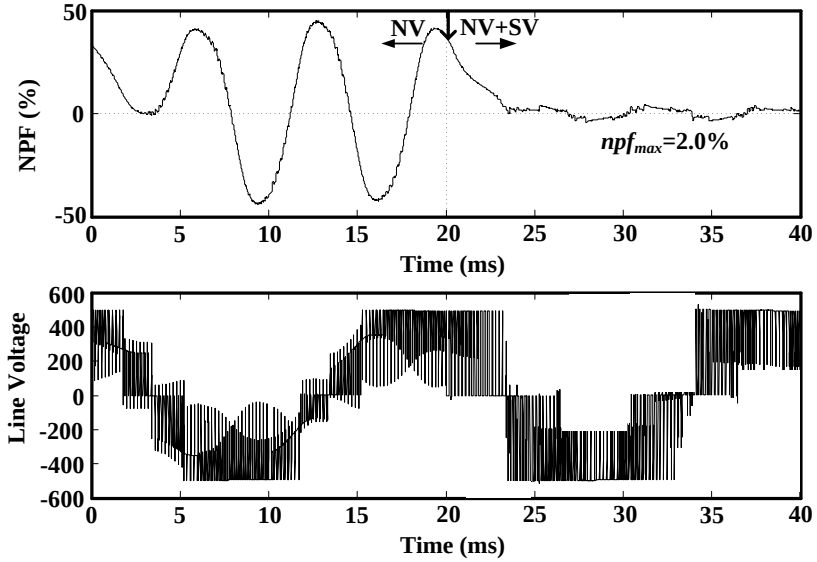



Figure 6.15: At $m_i$=0.9 transition from NV→NV+SV scheme at t=20ms

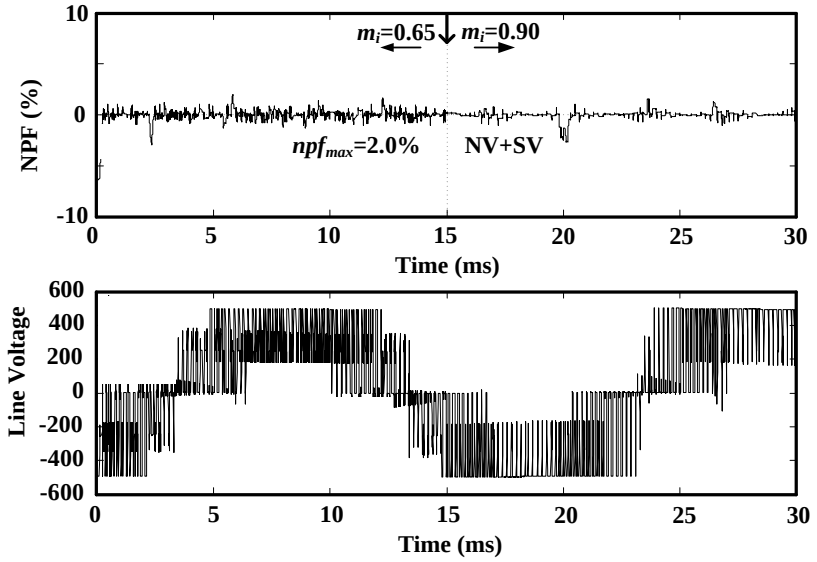



Figure 6.16: NV+SV scheme at $npf_{max}$=1% for $m_i$=0.65→$m_i$=0.90 t=15ms

a star connected RL load. Fig.6.14 shows a large neutral point fluctuation condition at $m_i$=0.9 with NV scheme. The effect of large fluctuation i.e. low order harmonics can be seen on line voltage. At $t$=15ms, SV scheme is applied and as a result neutral point fluctuation is eliminated. Similarly in Fig.6.15, NV+SV

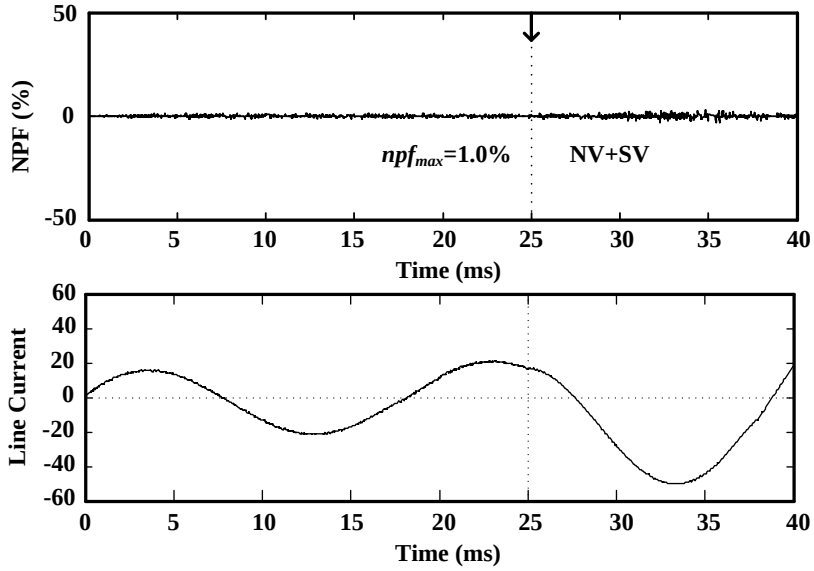



Figure 6.17: NV+SV scheme at $npf_{max}$=1% for 150% increase in load at t=25ms

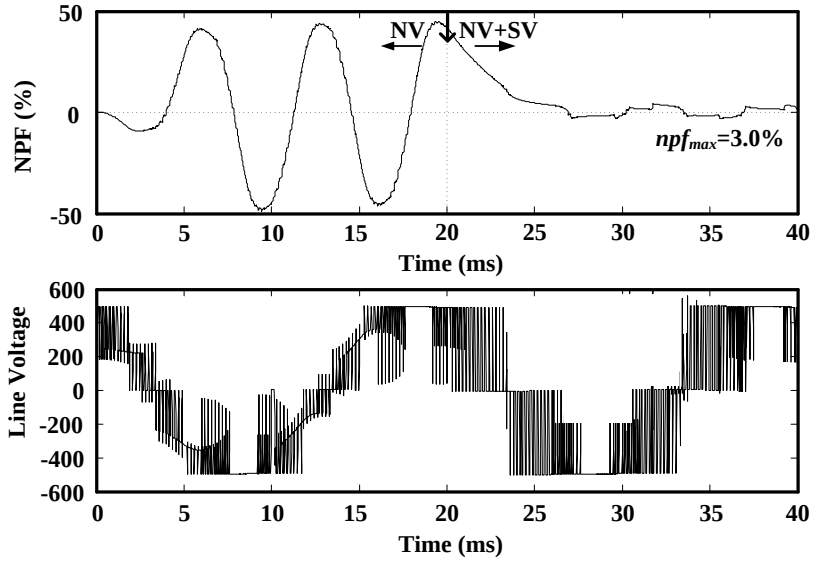



Figure 6.18: At $m_i$=0.94 transition from NV→NV+SV scheme at t=20ms

scheme with $npf_{max}$=2% is applied at $t$=20ms. After $t$=20ms, Fig.6.14 shows no neutral point fluctuation due to the use of SV scheme but Fig.6.15 shows small fluctuation corresponding to $npf_{max}$=2%. Fig.6.16 shows dynamic simulation results for NV+SV scheme with $npf_{max}$=2%. In Fig.6.16, $m_i$ is changed from 0.65 to 0.90

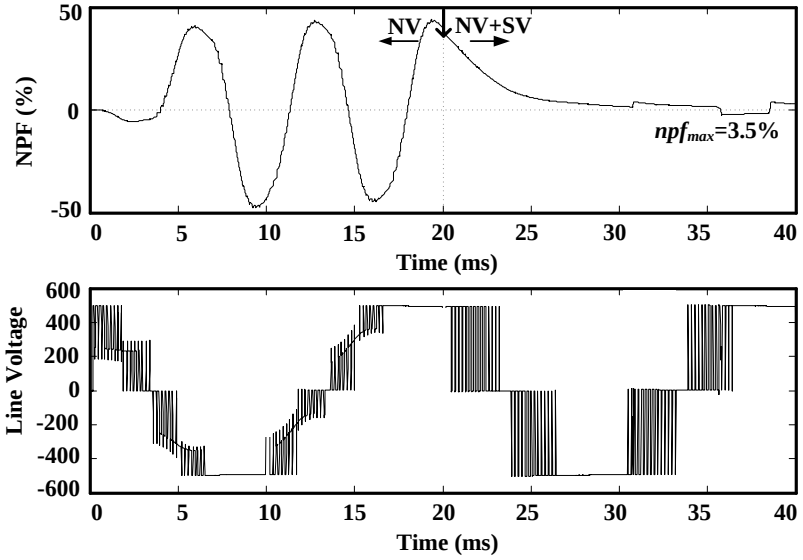



Figure 6.19: At $m_i$=0.96 transition from NV→NV+SV scheme at t=20ms

at $t$=15ms. Fig.6.17 shows dynamic simulation results for NV+SV scheme with $npf_{max}$=1% at $m_i$=0.9. In Fig.6.16, load is increased by 150% at $t$=25ms. Fig.6.16 and Fig.6.17 show that NV+SV scheme ensures neutral point balance for a sudden change in modulation index or load. Fig.6.18 shows dynamic condition at $m_i$=0.94 i.e. at $t$=15ms NV+SV scheme with $npf_{max}$=3.0% is applied. Fig.6.19 shows dynamic condition at $m_i$=0.96 i.e. at $t$=15ms NV+SV scheme with $npf_{max}$=3.5% is applied. Due to use of small vectors neutral point balance is obtained faster in Fig.6.18 as compared to Fig.6.19.

## 6.9 Summary

A scheme to operate a 3-level NPC inverter at high modulation index inclusive of overmodulation range is presented. The proposed scheme maintains neutral

point balance within a specified tolerance $npf_{max}$. The size of DC-link capacitors can be reduced as the neutral point fluctuation is restricted within a specified tolerance $npf_{max}$. Moreover, load parameters are not required. The proposed scheme uses only neutral point fluctuation $npf$ as feedback parameter to obtain an overall good performance, no other input is required. Using the combination of NV and SV scheme and maximum allowable neutral point fluctuation $npf_{max}$, the harmonic distortion and switching losses can be varied. The overmodulation is implemented using simple equations. The volt-secs balance is maintained throughout the scheme. The scheme is computationally simple, so it can be implemented using a commercially available DSP micro-controller.

# Chapter 7

# Description of Experimental Platform, Software and Hardware

This chapter describes the experimental platform, the software used and the hardware prototype developed to implement the proposed schemes.

## 7.1 Overview of the Experimental Platform

The schemes have been developed on dSPACE DS1104 Controller board. The algorithms are developed using $C$ programming language.

The block diagram in Fig. 7.1 shows the experimental setup. The experimental set-up comprises of following units,

- A pentium PC for rapid-prototyping and real-time control
- A dSPACE DS1104 board for running control programs, generating control

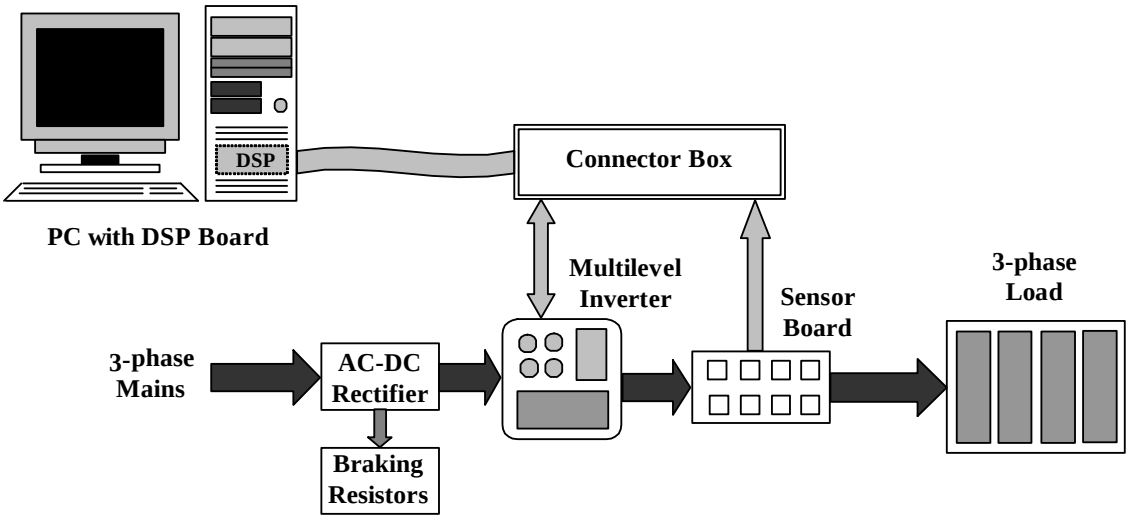



Figure 7.1: Platform used for hardware implementation

signals, sampling feedback signals and communicating with the computer

- Interface and gate drive boards for logic operations, buffering, isolations etc.
- Prototype of a three-phase 3-level NPC voltage source inverter (VSI)
- Prototype of three-phase 5-level cascaded H-bridge VSI
- The current sensors, voltage sensors and multimeters
- An induction motor or a star connected RL load
- A three-phase synchronous generator to simulate power grid
- A separate DC supply for the rotating field of synchronous generator
- A racking system that essentially is a hardware interfacing system. It comprises a 19" sub-racking system with several other cards such as Digital I/O Card, Control-PWM Card and Analog-signal Cards

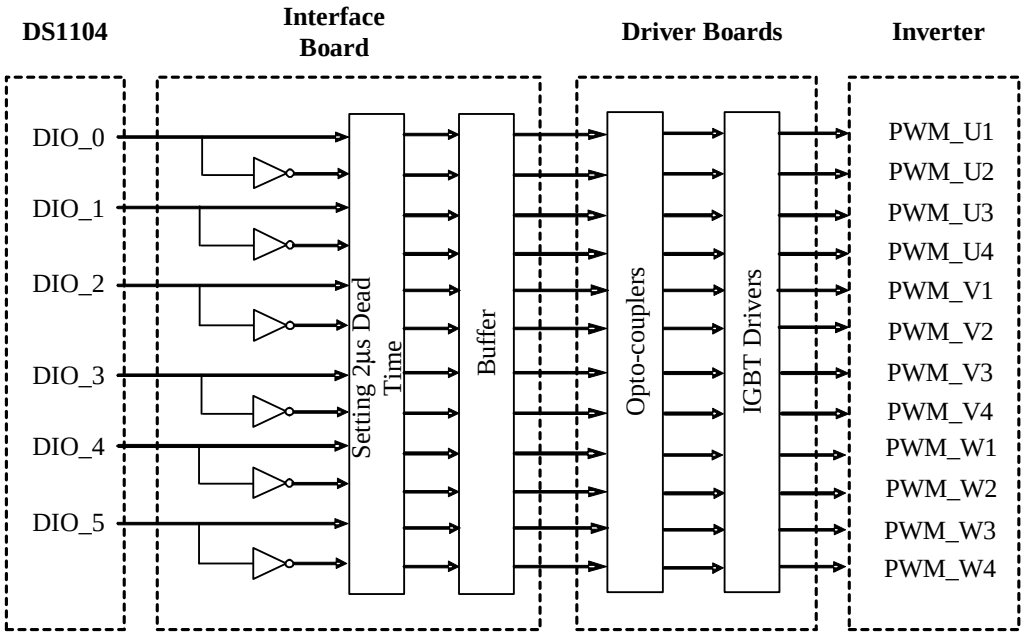



Figure 7.2: Interfacing the controller board with inverter

Among various units mentioned above, the DS1104 board, peripheral circuit interface board and inverter prototypes are described in this chapter.

## 7.2 dSPACE DS1104 R&D Controller board

The DS1104 board is specifically designed for the development of high-speed multivariable digital controllers and real time simulations in various fields [135]-[137]. It is a complete real-time control system based on a 603 PowerPC floating point processor running at 250MHz. For advanced I/O purposes, the board includes a slave-DSP subsystem based on the TMS320F240 DSP microcontroller. There are A/D and D/A converters as well to deal with analogue feedback signals. Depending on the communication between the PC and the DSP, users can debug the program

as well as tune parameters and trace execution results in real-time.

## 7.3 The Peripheral Interface Circuit

To transfer the digital signals from the DS1104 to the multilevel inverter peripheral circuits are needed. Fig. 7.2 shows the flow diagram for interfacing between DS1104 and 3-level inverter. Similar flow diagram is applicable to 5-level inverter but the number of PWM signals will be 24 and for three-phase $n$-level there will be 6($n$-1) PWM signals. There are two main boards, (i) interface board and (ii) gate drive board. They perform the following functions,

- Generating mid symmetric PWM signals to control the power switches
- Incorporating dead-time in the PWM signals
- Providing isolation between control and power circuits.
- Setting over-current/voltage protections and reset/stop functions.

### 7.3.1 Interfacing Board

Fig. 7.3 shows the interfacing board for the 3-level inverter. The 3-level inverter requires twelve PWM signals. They can be divided into two groups of six PWM signals. One group is complement of the other. Therefore essentially six signals are required from the DS1104 R&D controller board. The remaining six

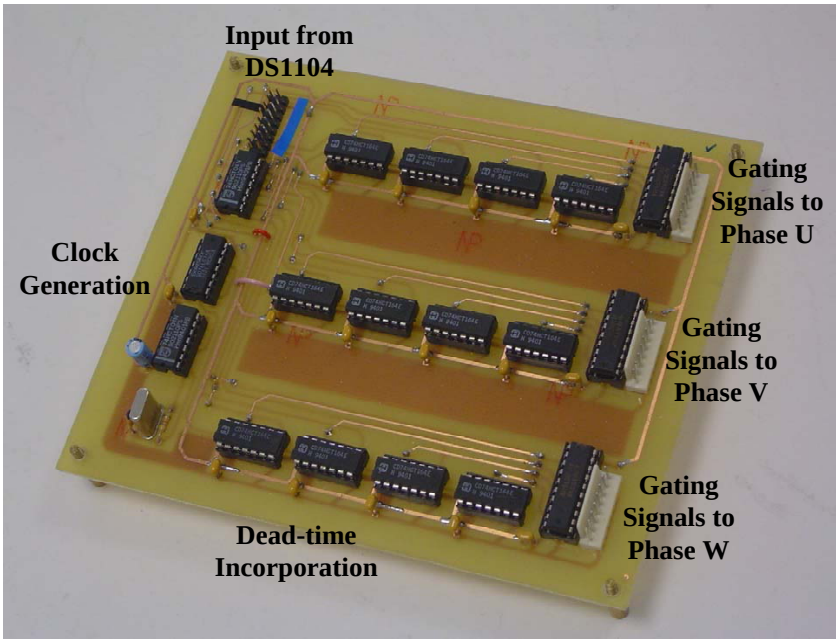



Figure 7.3: Interface board - between DS1104 board and gate drive circuit

signals are obtained by inverting them as shown for interface board in Fig. 7.3. Proper 'dead time' is then incorporated in these twelve PWM signals to avoid 'mutual-ON' of the upper and lower switches on the same phase of the inverter. For a 5-level inverter two such boards can be used to generate the PWM signals.

### 7.3.2 Gate Drive Circuit

The gate drive circuit provides isolation between the control and power circuits. Every IGBT of the power circuit has its own gate drive circuit consisting of isolated DC supplies, opto-couplers and gate drivers. Fig. 7.4 shows a typical gate drive circuit [56] to drive an IGBT.

The opto-couplers 'Agilant-HCPL4503' transfer the PWM signal and isolate

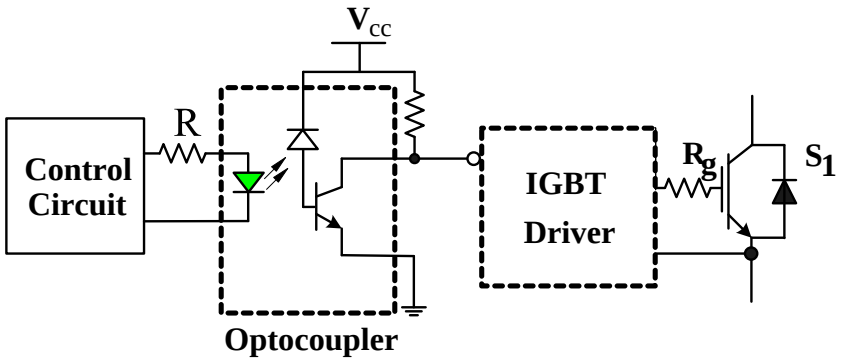



Figure 7.4: A typical circuit to drive an IGBT

the control circuit from the power circuit. The signal is then fed to IGBT driver 'Motorola-MC33153'. This driver has many important features such as protection against short-circuit, user programmable fault blanking capability, under-voltage lockout (UVLO), direct pin interface to opto-couplers etc.

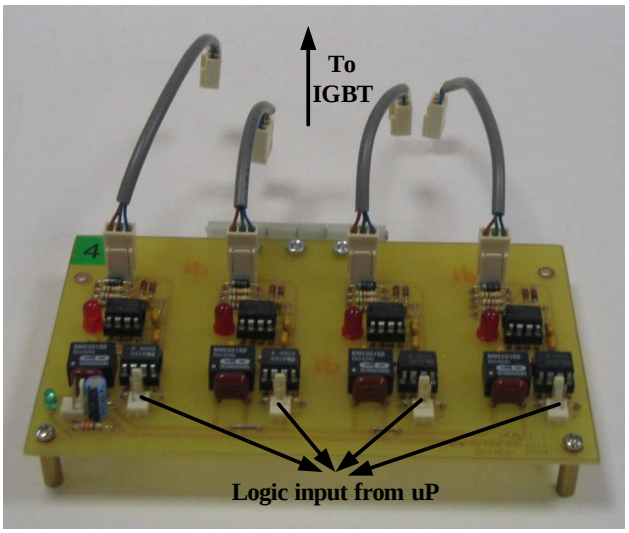



Figure 7.5: Gate drive unit for the four IGBT's which can be used for a phase 3-level NPC inverter or a H-bridge module of cascaded inverter

Fig. 7.5 shows the gate drive board for a phase of a 3-level inverter. It consists of four IGBT driving circuits as shown in Fig. 7.4. Three such boards are used for

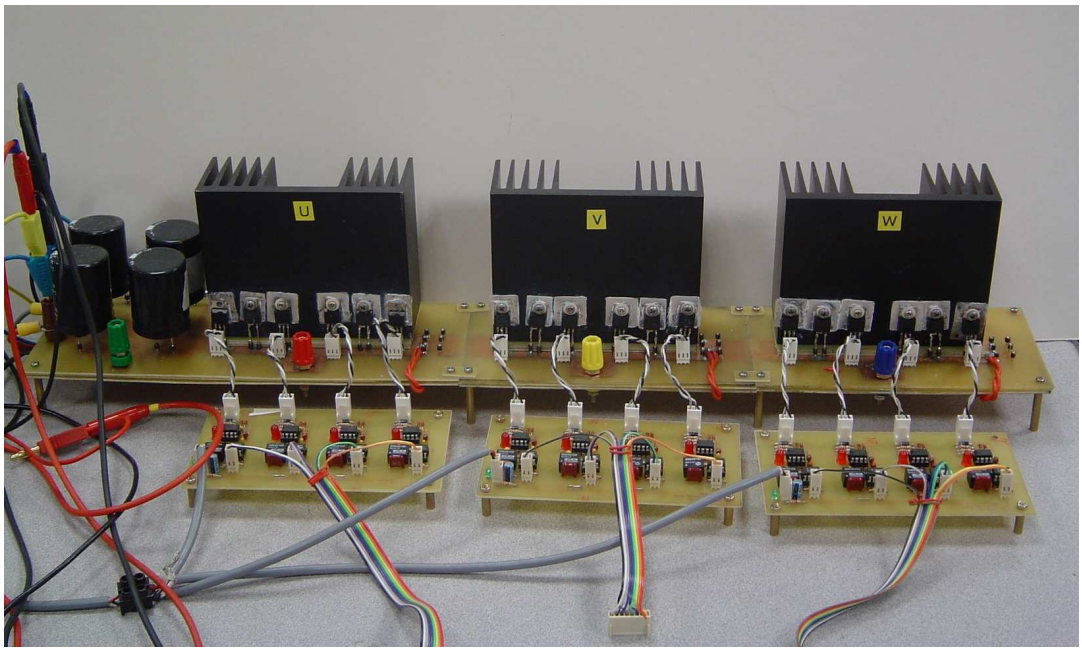



Figure 7.6: The hardware for the 3-level NPC inverter

the three-phase 3-level inverter. The similar board is developed for every H-bridge of cascaded H-bridge topology. However, the values of gate resistors [138] $R_{G(ON)}$ and $R_{G(OFF)}$, and blanking capacitor $C_{blank}$ is different from 3-level board to match the IGBT characteristics.

## 7.4 Multilevel Inverter Hardware

Prototype of a three-phase 3-level NPC inverter and a three-phase 5-level cascaded H-bridge inverters have been built for the experimental purpose.

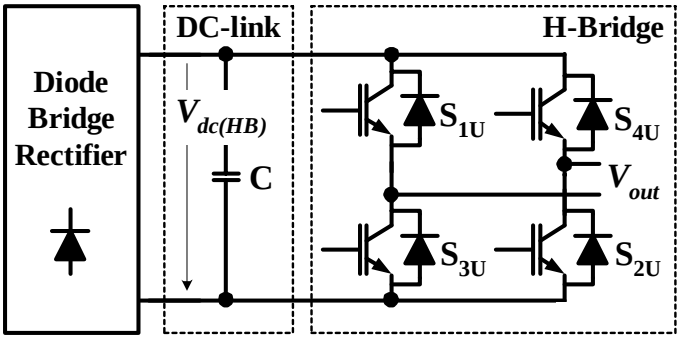



Figure 7.7: Block Diagram of a power module for the 5-level cascaded inverter

### 7.4.1 3-level Neutral Point Clamped Inverter

A three-phase 3-level NPC inverter consists of twelve power switches with reverse diodes, six clamping diodes, a DC source, Fig. 1.2. Discrete IGBT 'IR-G4BC30UD' is selected as main power switches. It has voltage rating of 600V and a maximum continuous current rating of 20A. The selected clamping diode is 'IR-20ETF10'. It has a forward current rating of 20A and a blocking voltage of 1000V. A three-phase 25A bridge rectifier 'IR-26MT160' is used for the DC link. Fig. 7.6 shows the hardware for the 3-level inverter along with respective gate drive.

### 7.4.2 5-level Cascaded H-Bridge Inverter

A three-phase 5-level cascaded H-bridge inverter requires six H-bridges Fig. 1.3 and a separate DC source for each H-bridge. A power module is developed to cater this need. The block diagram for this power module is shown in Fig.7.7. The prototype for this power module is shown in Fig.7.8. The power module mainly

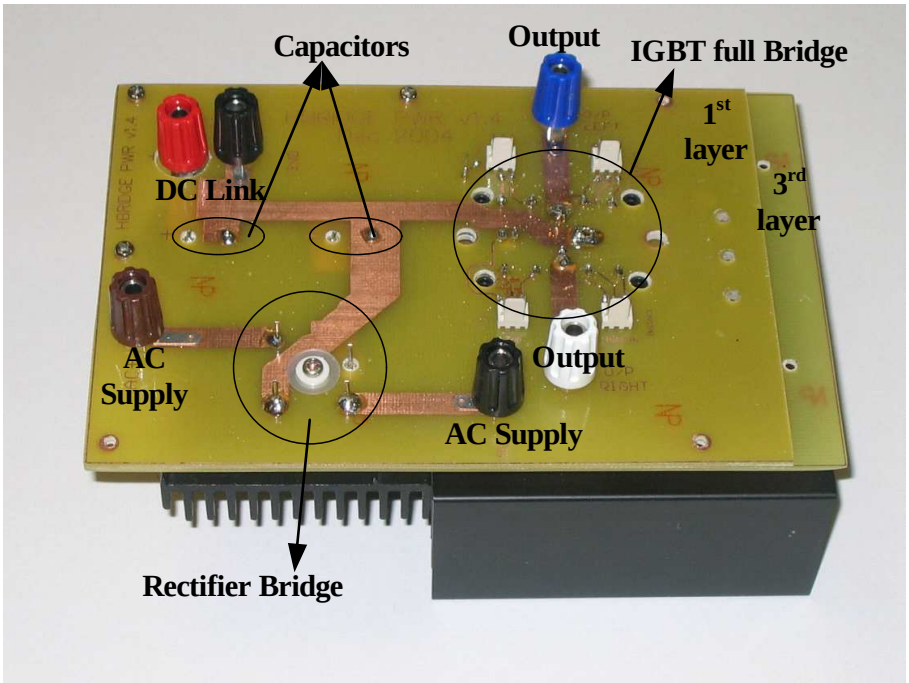



Figure 7.8: Prototype of a power module for the 5-level cascaded H-bridge Inverter

includes a single phase rectifier 'IR-GBPC2512W', DC-link capacitor and a single phase full bridge 'IR-20MT120UF'. The IGBT bridge has a maximum blocking voltage of 1200V and forward continuous current of 20A. Fig. 7.8 shows one of the six modules of 5-level cascaded H-bridge inverter. Every module can operate till $V_{dc}$=1000V and I=20A. Since every power module needs a isolated single phase AC supply. A three-phase transformer with six isolated windings is used to cater this need.

Fig.7.9 shows the laboratory setup showing 5-level inverter and some of the units mentioned in section 7.1 e.g. gate drive, dSPACE board, 3-phase transformer.

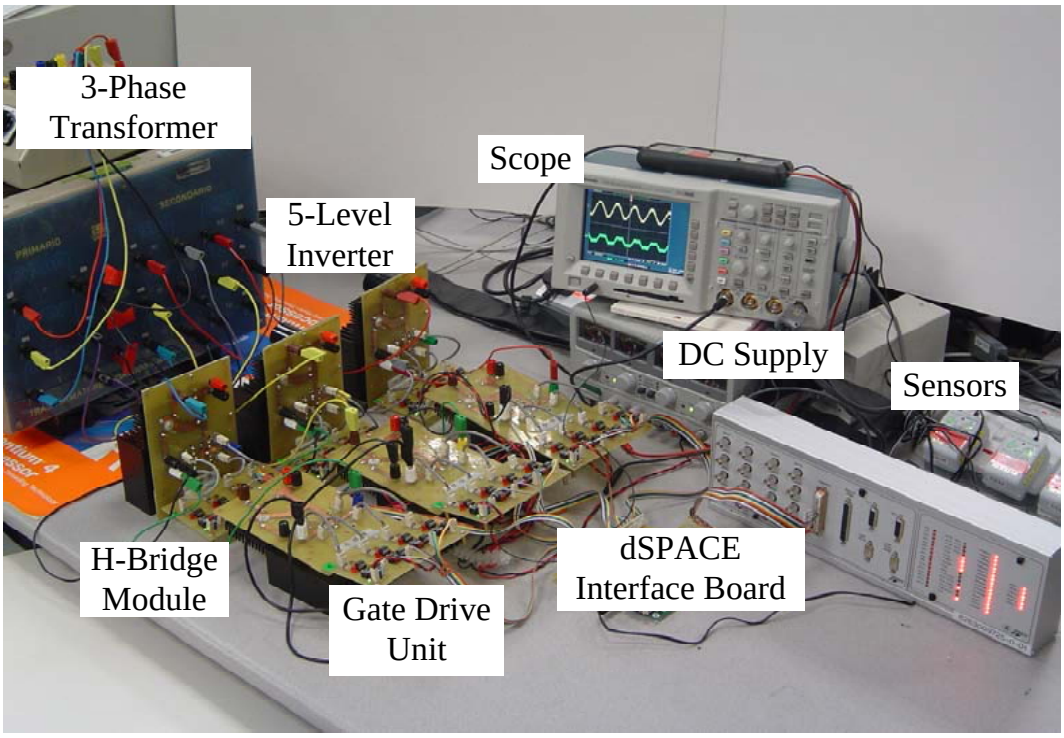



Figure 7.9: The hardware setup showing some of the units including 5-level inverter

# Chapter 8

# Conclusions and Future Work

This chapter concludes the thesis. Section 8.1 provides conclusion on the work done in this thesis. Section 8.2 briefly describes possible future work.

## 8.1 Conclusions

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. It makes multilevel inverters suitable for high voltage high power applications.

Some of the problems in the applications where multilevel inverter is being used are dependent on PWM technique. Some such problems are common mode voltage for motor drives, asynchronous PWM harmonics for grid connected VSI and neutral point fluctuation for NPC inverter. A suitable PWM technique is required to address these modulation dependent problems.

Space vector PWM is a potential PWM technique which can help in addressing these problems. However, implementation of space vector PWM for multilevel inverters is complex. Its extension to overmodulation is even more difficult due to nonlinearity of overmodulation range.

These problems are the main motivation for the work in this thesis. First, the problem of implementing space vector PWM for multilevel inverter is dealt.

Main problems in implementing space vector PWM for multilevel inverter are determination of exact location of reference vector, calculation of on-times and formation of appropriate switching sequence. In chapter 2, a simple Space Vector PWM algorithm for a multilevel inverter based on standard two-level Space Vector PWM has been proposed. The key advantages of the algorithm are, (i) it can be applied to any level without increasing the computations, in this thesis this algorithm is applied for 3-level, 5-level and 7-level using the same number of computations, (ii) it has flexibility of optimizing the switching pattern which leads to a solution to other problems, in this thesis depending on the problem various optimized switching patterns are used in Chapter 4, 5 and 6, (iii) it is independent of the topology of the inverter, in this thesis algorithm is applied for cascaded H-Bridge and NPC topology. (iv) it is simple to implement due to the use of two-level SVPWM concept, (v) it can be easily extended to overmodulation range.

In linear range the maximum obtainable voltage is 90.7% of the six-step value. It can be increased further by properly utilizing the DC link capacity through over-

modulation. Main problems in implementing SVPWM in overmodulation range is on-time calculation and formation of switching sequence due to non-linearity of this region. In chapter 3, the multilevel SVPWM algorithm proposed in chapter 2 is extended to overmodulation range. Apart from the advantages given above other merits of the proposed algorithm are, (i) use of two-level on-time calculations leading to simple calculation, (ii) simple method of calculating on-times in the overmodulation range thus avoiding use of complex equations and lookup tables.

General algorithm described above is independent of level and topology of the multilevel inverter. The algorithm is implemented using a processing unit and a mapping unit. This algorithm is applied and extended to address the modulation dependent problems mentioned above. While addressing these problems processing unit is not much affected. Whereas, since mapping unit stores switching sequences, the structure of mapping unit changes depending on level of inverter and problem into consideration as described in previous chapters.

The common mode voltage problem leads to bearing failure. This problem can be reduced by reducing the magnitude of $V_{NG}$ and frequency of $dV_{NG}/dt$. In chapter 4, a SVPWM scheme to reduce common mode voltage for a cascaded multilevel inverter is proposed. In the proposed scheme switching sequence are formed and stored in mapping unit to reduce magnitude of $V_{NG}$ and frequency of $dV_{NG}/dt$. The advantages of the scheme are, (i) Irrespective of the level $n$, the magnitude of generated $|V_{NO,\ n}|$ for that level is 0 or $V_{dc(HB,\ n)}/3$. (ii) Lesser

number of changes in $dV_{NG}/dt$, leading to a reduction in the number of $V_b$ and $i_{NG}$ occurrences. (iii) Higher modulation index as compared to other schemes while maintaining $|V_{NO,\,n}| = 0$ or $V_{dc(HB,\,n)}/3$. (iv) Harmonic distortion close to conventional SVPWM scheme due to the use of nearest three vectors. (v) The number of switch commutations lesser than conventional SVPWM for equilateral triangles and equal to conventional SVPWM scheme for isosceles triangles. (vi) Easily extendable to higher levels.

For a grid connected inverter the quality of output waveform is important. Two-level Voltage source inverter are known to produce subharmonics and interharmonics with asynchronous PWM. It is shown in this thesis that for a multilevel inverter as well subharmonics and interharmonics are generated with asynchronous PWM. In this thesis, various problems due to subharmonics and interharmonics are highlighted. Significant reduction of subharmonics and interharmonics is shown for a multilevel inverter with synchronous PWM. Waveform symmetries are incorporated to further improve the quality of the waveform. A simple scheme for close loop flux control of a grid connected cascaded multilevel inverter is proposed. The proposed scheme is based on synchronous SVPWM. The steady state and dynamic operation are clearly explained. In the proposed scheme, (i) Due to the flux prediction, the phase lag error does not exist, (ii) During dynamics, the flux error is compensated fast. The volt-sec balance is maintained even during dynamics.

The NPC topology is an attractive topology but neutral point fluctuation is

a problem with this topology. The main cause of this problem is current flowing through the neutral point in the DC-link. The key to solve this problem depends on the choice of switching states and their on-times. In chapter 6, the problem of neutral point balance at high modulation index is explained. A scheme to operate a 3-level NPC inverter at high modulation index inclusive of overmodulation range is presented. The main features of the scheme are, (i) It maintains neutral point balance within a specified tolerance $npf_{max}$ using a combination of conventional NV and proposed SV schemes. (ii) It uses only neutral point fluctuation $npf$ as feedback parameter to obtain an overall good performance and no other input is required e.g. the load parameters are not required. (iii) The size of DC-link capacitors can be reduced as the neutral point fluctuation is restricted within a specified tolerance $npf_{max}$. (iv) The volt-secs balance is maintained throughout the scheme. (v) The scheme is computationally simple and hence can be easily implemented.

In all, this thesis provides a simple algorithm to implement SVPWM for multi-level inverters. This algorithm is applied and extended to address three modulation dependent problems namely common mode voltage for motor drives, asynchronous PWM harmonics for grid connected VSI and neutral point fluctuation for NPC inverter. Proposed schemes and algorithms in this thesis have been theoretically explained and verified through experiments. Chapter 7 describes software platform, hardware developed and setup used for the experiments.

## 8.2 Future Work

With respect to the work done in this thesis, two potential directions are suggested for the future research, (i) Common mode voltage reduction in power systems, (ii) Bidirectional power transfer control using synchronous SVPWM, which will be an extension to the scheme proposed in chapter 5.

### 8.2.1 Common Mode Voltage Reduction

A space vector PWM based scheme is proposed in this thesis to reduce common mode voltage for multilevel inverters. In chapter 4, this scheme is applied to an induction motor and reduction in common mode voltage and so the common mode current is shown. It will be interesting to have a detailed study and analysis of the effect of DC-link fluctuations on common mode voltage and current.

Multilevel inverters are also used in power systems (section 1.1.1). The common mode voltage problem exists in power systems as well. Julian et al. [41] reported that the common mode currents can lead to a number of problems in power systems e.g. malfunctioning of sensitive electronics and control systems. This problem has not been addressed much in recent research. Hence, it will be interesting to study the effects of common mode voltage in power systems. Based on this study and depending on the needs of the electrical system under investigation, a suitable common mode reduction technique can be developed and applied to the electrical

system under investigation similar to chapter 4.

### 8.2.2 Bidirectional Power Control

A synchronous SVPWM scheme for close loop flux control of a grid connected cascaded multilevel inverter is proposed in this thesis. Chapter 5 shows a simple implementation of this scheme. However, in a more practical setup, it will be desired to have capability of bidirectional power transfer control through the multilevel inverter while controlling the active and reactive power [139]-[142]. The extension of the scheme proposed in chapter 5 for bidirectional power control will be timely and useful application for the grid connected system.

For the cascaded inverter setup in this thesis, the DC-link of each H-bridge inverter is supplied by an uncontrolled rectifier as shown in Fig.7.7. Such setup is sufficient to show the functionality of various algorithms/schemes proposed in this thesis. However, bidirectional power transfer control requires a proper DC-link control strategy for the inverter as part of close loop control.

# Bibliography

[1] W. Bin, *High-power converters and AC drives*. New Jersey: John Wiley & Sons, first ed., 2006.

[2] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power ac drives: a review," *IEEE International Symposium on Industrial Electronics, 1993. Conference Proceedings, ISIE'93 - Budapest*, pp. 38 – 43, June 1993.

[3] J. S. Lai and F. Z. Peng, "Multilevel converters - a new breed of power converters," *IEEE Trans. Ind. Application*, vol. 32, pp. 509 – 517, May/June 1996.

[4] M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," *IEEE-PESC Conference Record*, vol. 2, pp. 1013 – 1018, 1996.

[5] C. Newton and M. Summer, "Neutral point control for multi-level inverters: Theory, design and operation limitations," *in IEEE Ind. Applicat. Soc. Conf. Rec.*, pp. 1336 – 1343, 1997.

[6] B. S. Suh, G. Sinha, M. D. Majrekar, and T. A. Lipo, "Multilevel power conversion - an overview of topologies and modulation strategies," *Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipments, 1998. OPTIM '98*, vol. 2, pp. AD–11 – AD–24, May 1998.

[7] R. Teodorescu, F. Blaabjerg, Pedersen, E. J. Cengelci, S. U. Sulitjio, B. Woo, and P. Enjeti, "Multilevel converters - a survey," *Proceedings of EPE*, 1999.

[8] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 724 – 738, Aug. 2002.

[9] T. A. Meynard and H. Foch, "Multilevel conversion: High voltage chopper and voltage-source inverters," *in Proc. IEEE PESC 1992*, pp. 397 – 403, 1992.

[10] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. on Industry Applications*, vol. 35, pp. 36 – 44, Jan./Feb. 1999.

[11] J. Steinke, "Control strategy for a three phase ac traction drive with three-level gto pwm inverter," *19th Annual IEEE Power Electronics Specialists Conference, 1988. PESC '88 Record.*, vol. 1, pp. 431 – 438, April 1988.

[12] L. Tolbert, F. Peng, and T. Habetler, "Multilevel inverters for electric vehicle

applications," *Power Electronics in Transportation, 1998*, pp. 79 – 84, oct. 1998.

[13] H. Okayama, R. Uchida, M. Koyama, S. Mizoguchi, S. Tamai, H. Ogawa, T. Fujii, and Y. Shimomura, "Large capacity high performance 3-level gto inverter system for steel main rolling mill drives," *Industry Applications Society Conference, IAS-1996*, vol. 1, pp. 174 – 179, Oct. 1996.

[14] J. Rodriguez, J. Pontt, G. Alzarnora, N. Becker, O. Einenkel, and A. Weinstein, "Novel 20-mw downhill conveyor system using three-level converters," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 1093 – 1100, Oct. 2002.

[15] W. Min, J. Min, and J. Choi, "Control of statcom using cascade multilevel inverter for high power application," *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems, 1999. PEDS '99.*, vol. 2, pp. 871 – 876, July 1999.

[16] C. Lee, J. Leung, S. Hui, and H.-H. Chung, "Circuit-level comparison of statcom technologies," *IEEE Transactions on Power Electronics*, vol. 18, pp. 1084 – 1092, July 2003.

[17] J. Wang and F. Peng, "Unified power flow controller using the cascade multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1077 – 1084, July 2004.

[18] F. Z. Peng, J. McKeever, and D. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," *IEEE Transactions on Industry Applications*, vol. 34, pp. 1293 – 1298, Nov.-Dec. 1998.

[19] B.-R. Lin and T.-L. Hung, "Analysis and implementation of a single-phase multilevel inverter for power quality improvement," *Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, 2002. ISIE 2002.*, vol. 4, pp. 1235 – 1240, July 2002.

[20] B. R. Lin and T. C. Wei, "A novel npc inverter for harmonics elimination and reactive power compensation," *IEEE Transactions on Power Delivery*, vol. 19, pp. 1449 – 1456, July 2004.

[21] J. Ekanayake and M. Jenkins, "A three-level advanced static var compensator," *IEEE Transactions on Power Delivery*, vol. 11, pp. 540 – 545, Jan. 1996.

[22] L. Tolbert and F. Peng, "Multilevel converters as a utility interface for renewable energy systems," *IEEE Power Engineering Society Summer Meeting, 2000*, vol. 2, pp. 1271 – 1274, July 2000.

[23] S. Alepuz, A. Gilabert, E. Arguelles, J. Bordonau, and J. Peracaula, "A new approach for the connection of a three-level inverter to the power grid for applications in solar energy conversion," *28th Annual Conference of the Industrial Electronics Society, IECON 02*, vol. 4, pp. 3285 – 3290, Nov. 2002.

[24] A. Yazdani and R. Iravani, "A neutral-point clamped converter system for direct-drive variable-speed wind power unit," *Energy Conversion, IEEE Transactions on*, vol. 21, pp. 596 – 607, June 2006.

[25] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzlez, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1504 – 1511, Oct. 2006.

[26] M. Malinowski, W. Kolomyjski, Kazmierkowski, M. P., and S. Stynski, "Control of variable-speed type wind turbines using direct power control space vector modulated 3-level pwm converter," *IEEE International Conference on Industrial Technology - ICIT*, vol. 21, pp. 1516 – 1521, Dec. 2006.

[27] J. Kolar, H. Sree, U. Drofenik, N. Mohan, and F. Zach, "A novel three-phase three-switch three-level high power factor sepic-type ac-to-dc converter," *IEEE Applied Power Electronics Conference and Exposition, APEC-1997*, vol. 2, pp. 657 – 665, Feb. 1997.

[28] F. Canales, P. Barbosa, and F. Lee, "A zero-voltage and zero-current switching three-level dc/dc converter," *Power Electronics, IEEE Transactions on*, vol. 17, pp. 898 – 904, Nov. 2002.

[29] B. Ozpineci, L. Tolbert, and Z. Du, "Optimum fuel cell utilization with multilevel inverters," *IEEE 35th Annual Power Electronics Specialists Conference, 2004. PESC 04*, vol. 6, pp. 4798 – 4802, June 2004.

[30] Z. Zhang and N. Fahmi, "Modelling and analysis of a cascade 11-level inverters-based svg with control strategies for electric arc furnace (eaf) application," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 150, pp. 217 – 223, March 2003.

[31] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped pwm inverter," *IEEE Trans. Ind. Application*, vol. IA-17, p. 518523, Sept.-Oct. 1981.

[32] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Ind. Applicat.*, vol. 33, p. 202 208, Jan./Feb. 1997.

[33] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," *IEEE Conf.Ind. Application*, p. 921 928, Oct. 1994.

[34] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Trans. Ind. Applicat.*, vol. 36, pp. 834 – 841, May/June 2000.

[35] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Application*, vol. 37, pp. 611 – 618, Mar./Apr. 2001.

[36] A. Chen, L. Hu, and X. He, "A novel type of combined multilevel converter topologies," *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004.*, vol. 3, pp. 2290 – 2294, Nov. 2004.

[37] G. Narayanan, *Synchronized Pulsewidth Modulation Strategies based on Space Vector Approach for Induction Motor Drives*. PhD thesis, Indian Institute of Science, Bangalore, 1999.

[38] N. Celanovic, *Space Vector Modulation and Control of Multilevel Converters*. PhD thesis, Virginia Polytechnic Institute and State University, 2000.

[39] J. P. i Fèlix, *Modulation and Control of Three-Phase PWM Multilevel Converters*. PhD thesis, Universitat Politècnica de Catalunya, 2002.

[40] A. Tripathi, *Stator Flux Vector Based Modulation and Constant Switching Frequency Direct Torque Control of AC Machines*. PhD thesis, National University of Singapore, 2004.

[41] A. Julian, G. Oriti, and T. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *Power Electronics, IEEE Transactions on*, vol. 14, pp. 982 – 989, Sept. 1999.

[42] S. Chen, T. Lipo, and D. Fitzgerald, "Source of induction motor bearing currents caused by pwm inverters," *Energy Conversion, IEEE Transactions on*, vol. 11, pp. 25 – 32, March 1996.

[43] J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Effect of pwm inverters on ac motor bearing currents and shaft voltages," *Industry Applications, IEEE Transactions on*, vol. 32, pp. 250 – 259, March-April 1996.

[44] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leak-

age currents in pwm inverter-fed ac motor drive systems," *Industry Applications, IEEE Transactions on*, vol. 32, pp. 1105 – 1114, Sept.-Oct. 1996.

[45] D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Bearing currents and their relationship to pwm drives," *Power Electronics, IEEE Transactions on*, vol. 12, pp. 243 – 252, March 1997.

[46] D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "System electrical parameters and their effects on bearing currents," *Industry Applications, IEEE Transactions on*, vol. 33, pp. 577 – 584, Mar.-Apr. 1997.

[47] S. Chen and T. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *Industry Applications, IEEE Transactions on*, vol. 34, pp. 1042 – 1048, Sept.-Oct. 1998.

[48] Y.-S. Lai;, "Investigations into the effects of pwm techniques on common mode voltage for inverter-controlled induction motor drives," *Power Engineering Society 1999 Winter Meeting, IEEE*, vol. 1, pp. 35 – 40, Jan.-Feb. 1999.

[49] H.-D. Lee and S.-K. Sul, "Common-mode voltage reduction method modifying the distribution of zero-voltage vector in pwm converter/inverter system," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 1732 – 1738, Nov.-Dec. 2001.

[50] J. Rodriguez, L. Moran, J. Pontt, R. Osorio, and S. Kouro, "Modeling and analysis of common-mode voltages generated in medium voltage pwm-csi

drives," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 873 – 879, May 2003.

[51] A. Muetze and A. Binder, "Calculation of the influence of insulated bearings and insulated inner bearing seats on circulating bearing currents in machines of inverter-based drive systems," *International Electric Machines and Drives Conference - IEMDC*, pp. 1068 – 1074, May 2005.

[52] A. Muetze and A. Binder, "Calculation of motor capacitances for prediction of discharge bearing currents in machines of inverter-based drive systems," *International Electric Machines and Drives Conference - IEMDC*, pp. 264 – 270, May 2005.

[53] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage pwm voltage-source-inverter drive applications," *Industry Applications, IEEE Transactions on*, vol. 36, pp. 1336 – 1341, Sept.-Oct. 2000.

[54] A. Muetze and A. Binder, "Influence of motor size on the nature of bearing currents - investigations at 11 kw and 110 kw inverter-fed induction motors," *45th International Conference on Power Electronics and Intelligent Motion Power Quality (PCIM)*, no. IM 3.1, 2002.

[55] H.-J. Kim, H.-D. Lee, and S.-K. Sul;, "A new pwm strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed ac motor drives," *In-*

*dustry Applications, IEEE Transactions on*, vol. 37, pp. 1840 – 1845, Nov.-Dec. 2001.

[56] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics : converters, applications, and design*. Hoboken, NJ: John Wiley and Sons, third ed., 2003.

[57] J. Holtz, "Pulsewidth modulation-a survey," *Industrial Electronics, IEEE Transactions on*, vol. 39, pp. 410 – 420, Oct. 1992.

[58] C. Saniter, D. Schulz, and R. Hanitsch, "Causes of harmonics and interharmonics in wind energy converters," *RIO 5 - World Climate & Energy Event, Rio de Janeiro, Brazil*, pp. 169 – 176, Feb. 2005.

[59] F. Wang, "Reduce beat and harmonics in grid-connected three-level voltage-source converters with low switching frequencies," *Industry Applications, IEEE Transactions on*, vol. 43, pp. 1349 – 1359, Sep.-Oct. 2007.

[60] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE*, vol. 82, pp. 1194 – 1214, Aug. 1994.

[61] J. Deane and D. Hamill, "Instability, subharmonics, and chaos in power electronic systems," *Power Electronics, IEEE Transactions on*, vol. 5, pp. 260 – 268, July 1990.

[62] L. Hu and R. Yacamini, "Calculation of harmonics and interharmonics in hvdc schemes with low dc side impedance," *Generation, Transmission and*

*Distribution [see also IEE Proceedings-Generation, Transmission and Distribution], IEE Proceedings Conference*, vol. 140, pp. 469 – 476, Nov. 1993.

[63] R. Yacamini, "Power system harmonics. iv. interharmonics," *Power Engineering Journal [see also Power Engineer]*, vol. 10, pp. 185 – 193, Aug. 1996.

[64] I. Zhezhelenko and Y. Sayenko, "Analysis methods of interharmonics investigations in power supply systems," *Harmonics and Quality of Power, 2000. Proceedings. Ninth International Conference on*, vol. 1, pp. 61–63, Oct. 2000.

[65] E. Gunther, "Interharmonics in power systems," *Power Engineering Society Summer Meeting, 2001. IEEE*, vol. 2, pp. 813 – 817, July 2001.

[66] J. Barros, E. Prez, A. Pigazo, and R. Diego, "Power system management and control, 2002. fifth international conference on (conf. publ. no. 488)," *Electric Ship Technologies Symposium, 2005 IEEE*, pp. 100 – 105, Apr. 2002.

[67] T. Keaochantranond and C. Boonseng, "Harmonics and interharmonics estimation using wavelet transform," *Transmission and Distribution Conference and Exhibition 2002: Asia Pacific. IEEE/PES*, vol. 2, pp. 775 – 779, Oct. 2002.

[68] G. Chang and S. Chen, "Characterizing harmonic and interharmonic currents generated by the vsi-fed adjustable speed drives," *Power System Technology, 2004. PowerCon 2004. 2004 International Conference on*, vol. 1, pp. 475 – 480, Nov. 2004.

[69] T. Tayjasanant, W. Wang, C. Li, and W. Xu, "Interharmonic-flicker curves," *Power Delivery, IEEE Transactions on*, vol. 20, pp. 1017 – 1024, Apr. 2005.

[70] A. Testa and R. Langella, "Interharmonics from a probabilistic perspective," *Power Engineering Society General Meeting, 2005. IEEE*, vol. 3, pp. 2410 – 2415, June 2005.

[71] T. Kim, E. Powers, W. Grady, and A. Arapostathis, "Real and reactive power analysis for interharmonics," *Electric Ship Technologies Symposium, 2005 IEEE*, pp. 244 – 247, July 2005.

[72] S. Amrei, D. Xu, and Y. Lang, "Harmonics and interharmonics in general vsi/csi inverters: analysis, modeling and simulation," *Industrial Technology, 2005. ICIT 2005. IEEE International Conference on*, pp. 75 – 80, Dec. 2005.

[73] P. Petrovic and M. Stevanovic, "Measuring active power of synchronously sampled ac signals in presence of interharmonics and subharmonics," *Electric Power Applications, IEE Proceedings-*, vol. 153, pp. 227 – 235, Mar. 2006.

[74] A. Testa and R. Langella, "Power system subharmonics," *Power Engineering Society General Meeting, 2005. IEEE*, vol. 3, pp. 2237 – 2242, June 2005.

[75] P. Pourbeik, C. Bowler, and V. Crocker, "Model validation testing for the purpose of determining generation equipment dynamic performance and torsional mechanical response," *Power Engineering Society General Meeting, 2004. IEEE*, vol. 2, pp. 1510 – 1514, June 2004.

[76] J. De Abreu and A. Emanuel, "The need to limit subharmonics injection," *Harmonics and Quality of Power, 2000. Proceedings. Ninth International Conference on*, vol. 1, pp. 251 – 253, Oct. 2000.

[77] M. Karimi-Ghartemani and M. Iravani, "Measurement of harmonics/inter-harmonics of time-varying frequencies," *Power Delivery, IEEE Transactions on*, vol. 20, pp. 23 – 31, Jan. 2005.

[78] T. Keppler, N. Watson, J. Arrillaga, and S. Chen, "Theoretical assessment of light flicker caused by sub- and interharmonic frequencies," *Power Delivery, IEEE Transactions on*, vol. 18, pp. 329 – 333, Jan. 2003.

[79] A. Beig, G. Narayanan, and V. Ranganathan, "Space vector based synchronized pwm algorithm for three level voltage source inverters: principles and application to v/f drives," *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]*, vol. 2, pp. 1249 – 1254, Nov. 2002.

[80] R. Kanchan, M. Baiju, K. Mohapatra, P. Ouseph, and K. Gopakumar, "Space vector pwm signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEE Proc.-Electr. Power Appl.*, vol. 152, pp. 297 – 309, Mar. 2005.

[81] J. Holtz, W. Lotzkat, and A. M. Khambadkone, "On continuous control of pwm inverters in overmodulation range including six-step," *IEEE Transaction on Power Electronics*, vol. 8, pp. 546–553, 1993.

[82] D.-C. Lee and G.-M. Lee, "A novel overmodulation technique for space-vector pwm inverters," *IEEE Trans. on Power Electronics*, vol. 13, no. 6, pp. 1144–1151, 1998.

[83] A. Tripathi, A. Khambadkone, and S. Panda, "Direct method of overmodulation with integrated closed loop stator flux vector control," *IEEE Transactions on Power Electronics*, vol. 20, pp. 1161–1168, Sept. 2005.

[84] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral point voltage balancing problem in three level neutral point clamped voltage source pwm inverters," *Power Electronics, IEEE Transactions on*, vol. 15, pp. 242 – 249, March 2000.

[85] K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector," *IEEE Transactions on Ind. Applications*, vol. 38, no. 6, pp. 1572–1580, 2002.

[86] T. Ishida, T. Miyamoto, T. Oota, K. Matsuse, K. Sasagawa, and L. Huang, "A control strategy for a five-level double converter with adjustable dc link voltage," *Industry Applications Conference*, vol. 1, pp. 530 – 536, Oct. 2002.

[87] S. K. Mondal, J. O. P. Pinto, and B. K. Bose, "A neural-network-based space-vector pwm controller for a three-level voltage-fed inverter induction motor drive," *IEEE Transaction on Power Electronics*, vol. 38, May-June 2002.

[88] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, p. 637641, March/April 2001.

[89] S. Wei, B. Wu, F. Li, and C. Liu, "A general space vector pwm control algorithm for multilevel inverters," *Applied Power Electronics Conference and Exposition, APEC '03, Eighteenth Annual IEEE*, vol. 1, pp. 562 – 568, 9-13 Feb. 2003.

[90] H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Application*, vol. 36, pp. 1645 – 1653, Nov.-Dec. 2000.

[91] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector pwm method for three-level inverters," *IEEE Transactions on Power Electronics*, vol. 16, July 2001.

[92] P. C. Loh and D. G. Holmes, "Flux modulation for multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 38, pp. 1389–1399, Sep/Oct. 2002.

[93] B. McGrath and D. Holmes, "Sinusoidal pwm of multilevel inverters in the overmodulation region," *IEEE 33rd Annual Power Electronics Specialists Conference (PESC)*, vol. 2, pp. 485 – 490, June 2002.

[94] S. K. Mondal, B. K. Bose, V. Oleschuk, and J. O. P. Pinto, "Space vector pulse width modulation of three-level inverter extending operation into over-

modulation region," *IEEE Transaction on Power Electronics*, vol. 18, pp. 604 – 611, March 2003.

[95] M. Saeedifard, A. R. Bakhshai, G. Joos, and P. Jain, "Extending the operating range of the neuro-computing vector classification space vector modulation algorithm of three-level inverters into overmodulation region," *Industry Appl. Conf.*, vol. 1, pp. 672 – 677, October 2003.

[96] K. Ratnayake and Y. Murai, "A novel pwm scheme to eliminate common-mode voltage in three-level voltage source inverter," *Power Electronics Specialists Conference - PESC Record. 29th Annual IEEE*, vol. 1, pp. 269 – 274, May 1998.

[97] A. Von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing dc-link balancing, ride-through enhancement, and common-mode voltage elimination," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 739 – 745, August 2002.

[98] V. Oleschuk and F. Blaabjerg, "Three-level inverters with common-mode voltage cancellation based on synchronous pulsewidth modulation," *IEEE Power Electronics Specialists Conference, 2002*, vol. 2, pp. 863 – 868, June 2002.

[99] P. C. Loh, D. Holmes, Y. Fukuta, and T. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *Industry Applications, IEEE Transactions on*, vol. 39, pp. 1386 – 1395, Sept.-Oct. 2003.

[100] D. Rendusara, E. Cengelci, P. Enjeti, V. Stefanovic, and J. Gray, "Analysis of common mode voltage-"neutral shift" in medium voltage pwm adjustable speed drive (mv-asd) systems," *Power Electronics, IEEE Transactions on*, vol. 15, pp. 1124 – 1133, Nov. 2000.

[101] J. Rodriguez, J. Pontt, P. Correa, P. Cortes, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *Industrial Electronics, IEEE Transactions on*, vol. 51, pp. 834 – 839, Aug. 2004.

[102] P. C. Loh, D. Holmes, Y. Fukuta, and T. Lipo, "A reduced common mode hysteresis current regulation strategy for multilevel inverters," *Power Electronics, IEEE Transactions on*, vol. 19, pp. 192 – 200, Jan. 2004.

[103] J. Holtz and B. Beyer, "Optimal synchronous pulsewidth modulation with a trajectory-tracking scheme for high-dynamic performance," *Industry Applications, IEEE Transactions on*, vol. 29, pp. 1098 – 1105, Nov.-Dec. 1993.

[104] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulsewidth modulation," *Industry Applications, IEEE Transactions on*, vol. 31, pp. 1110 – 1120, Sept.-Oct. 1995.

[105] J. Holtz and N. Oikonomou, "Synchronous optimal pulsewidth modulation and stator flux trajectory control for medium-voltage drives," *Industry Applications, IEEE Transactions on*, vol. 43, pp. 600 – 608, March-April 2007.

[106] V. Oleschuk, F. Blaabjerg, and B. Bose, "Analysis and comparison of algebraic and trigonometric methods of synchronous pwm for inverter drives,"

*Power Electronics Specialists Conference, IEEE 33rd Annual*, vol. 3, pp. 1439 – 1444, June 2002.

[107] V. Oleschuk and F. Blaabjerg, "Synchronized scheme of continuous space-vector pwm with the real-time control algorithms," *Power Electronics Specialists Conference, IEEE 35th Annual*, vol. 2, pp. 1207 – 1213, June 2004.

[108] V. Oleschuk, V. Ermuratski, F. Profumo, A. Tenconi, R. Bojoi, and A. Stankovic, "Novel schemes of synchronous pwm for dual inverter-fed drives with cancellation of the zero sequence currents," *Power Electronics, Electrical Drives, Automation and Motion, International Symposium on*, pp. 451 – 456, May 2006.

[109] V. Oleschuk, A. Sizov, F. Profumo, A. Tenconi, and A. Stankovic, "Multi-level dual inverter-fed drives with algorithms of synchronized pwm," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1 – 7, June 2006.

[110] V. Oleschuk, F. Profumo, A. Tenconi, R. Bojoi, and A. Stankovic, "Cascaded three-level inverters with synchronized space-vector modulation," *The IEEE Industry Applications Conference Forty-First IAS Annual Meeting, Conference Record of*, vol. 2, pp. 595 – 602, Oct. 2006.

[111] V. Oleschuk, F. Profumo, A. Tenconi, R. Bojoi, and A. Stankovic, "Synchronization of voltage waveforms in basic topologies of dual inverter-fed motor

drives," *Power Electronics and Motion Control Conference, CES/IEEE 5th International*, vol. 3, pp. 1 – 6, Aug. 2006.

[112] G. Narayanan and V. T. Ranganathan, "Synchronised bus-clamping pwm strategies based on space vector approach for modulation up to six-step mode," *Power Electronic Drives and Energy Systems for Industrial Growth, 1998. Proceedings. 1998 International Conference on*, vol. 2, pp. 996 – 1001, Dec. 1998.

[113] G. Narayanan and V. T. Ranganathan, "Synchronised pwm strategies based on space vector approach. i. principles of waveform generation," *Electric Power Applications, IEE Proceedings-*, vol. 146, pp. 267 – 275, May 1999.

[114] G. Narayanan and V. T. Ranganathan, "Synchronised pwm strategies based on space vector approach. ii. performance assessment and application to v/f drives," *Electric Power Applications, IEE Proceedings-*, vol. 146, pp. 276 – 281, May 1999.

[115] G. Narayanan and V. T. Ranganathan, "Two novel synchronized bus-clamping pwm strategies based on space vector approach for high power drives," *Power Electronics, IEEE Transactions on*, vol. 17, pp. 84 – 93, Jan. 2002.

[116] A. Beig and V. Ranganathan, "Space vector based bus clamped pwm algorithms for three level inverters: implementation, performance analysis and application considerations," *Applied Power Electronics Conference and Ex-*

*position, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 1, pp. 569 – 575, Feb. 2003.

[117] J. Steinke, "Switching frequency optimal pwm control of a three-level inverter," *IEEE Trans. Power Electron.*, vol. 7, July 1992.

[118] L. Helle, S. Munk-Nielsen, and P. Enjeti, "Generalized discontinuous dc-link balancing modulation strategy for three-level inverters," *Power Conversion Conference, 2002*, vol. 2, pp. 359 – 366, April 2002.

[119] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector pwm - a modulation for the comprehensive neutral-point balancing in the three-level npc inverter," *IEEE Letters on Power Electro.*, vol. 2, pp. 11–15, March 2004.

[120] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source pwm inverters," *in Proc. IEEE Ind. Applicat. Soc. Conf. Rec.*, p. 965970, 1993.

[121] B. P. McGrath, D. G. Holmes, and T. A. Lipo, "Optimized space vector switching sequences for multilevel inverters," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 1293 – 1301, Nov. 2003.

[122] A. Tripathi, A. M. Khambadkone, and S. K. Panda, "Stator flux based space-vector modulation and closed loop control of the stator flux vector in overmodulation into six-step mode," *IEEE Transaction on Power Electronics*, vol. 19, pp. 775–782, May 2004.

[123] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters : principles and practice*. Piscataway, NJ: IEEE Press, first ed., 2003.

[124] T. Bruckner and D. G. Holmes, "Optimal pulse-width modulation for three-level inverters," *Power Electronics, IEEE Transactions on*, vol. 1, pp. 82 – 89, January 2005.

[125] S. Fukuda, K. Suzuki, and Y. Iwaji, "Harmonic evaluation of an npc pwm inverter employing the harmonic distortion determining factor," *in Proc. IEEE Industrial Applications Soc. Annu. Meeting, Orlando, FL*, pp. 2417 – 2421, 1995.

[126] H. W. V. D. Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," *IEEE Transaction on Industry Applications*, vol. 24, pp. 142 – 150, Jan./Feb. 1988.

[127] Z. Zhang, J. Kuang, X. Wang, and B. Ooi, "Force commutated hvdc and svc based on phase-shifted multi-converter modules," *IEEE Transactions on Power Delivery*, vol. 8, pp. 712 – 718, April 1993.

[128] C. Cecati, A. Dell'Aquila, A. Lecci, M. Liserre, and V. Monopoli, "A discontinuous carrier-based multilevel modulation for multilevel converters," *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, vol. 1, pp. 280 – 285, Nov. 2004.

[129] P. C. Loh, D. G. Holmes, and T. A. Lipo, "Implementation and control of distributed pwm cascaded multilevel inverters with minimal harmonic distor-

tion and common-mode voltage," *IEEE Transactions on Power Electronics*, vol. 20, pp. 90 – 99, Jan. 2005.

[130] S. Bolognani and M. Zigliotto, "Novel digital continuous control of svm inverters in the overmodulation range," *IEEE Trans. on Industrial Applications*, vol. 33, no. 2, pp. 525–530, 1997.

[131] T.Ishida, K. Matsuse, K. Sugita, L. Huang, and K.Sasagawa, "Dc voltage control strategy for a five-level converter," *IEEE Trans. on Power Electronics*, vol. 15, pp. 508–515, May 2000.

[132] L. Dalessandro, S. D. Round, U. Drofenik, and J. W. Kolar, "Discontinuous space-vector modulation for three-level pwm rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, pp. 530 – 542, March 2008.

[133] M. P. Kazmierkowski and H. Tunia, *Automatic Control of Converter-Fed Drives*. Amsterdam: Elsevier science publishers, 1994.

[134] M. Hinkkanen and J. Luomi, "Modified integrator for voltage model flux estimation of induction motors," in *Industrial Electronics Society, IECON '01. The 27th Annual Conference of the IEEE*, vol. 2, pp. 1339 –1343, sept.-oct. 2001.

[135] dSPACE 1104, "Ds1104 r&d controller board, installation and configuration," vol. 4.0, 2003.

[136] dSPACE 1104, "Ds1104 r&d controller board, controldesk experiment guide," vol. 4.0, 2003.

[137] dSPACE 1104, "Ds1104 r&d controller board, rti and rti-mp implementation guide," vol. 4.0, 2003.

[138] R. S. Chokhawala, J. Catt, and B. R. Pelly, "Gate drive considerations for igbt modules," *IEEE Transactions on Industry Applications*, vol. 33, pp. 603 – 611, May/June 1995.

[139] F. Peng and J. Lai, "Generalized instantaneous reactive power theory for three-phase power systems," *Instrumentation and Measurements, IEEE Transactions on*, vol. 45, pp. 293 – 297, Feb. 1996.

[140] H. Kim, F. Blaabjerg, B. Bak-Jensen, and J. Choi, "Instantaneous power compensation in three-phase systems by using p-q-r theory," *Power Electronics, IEEE Transactions on*, vol. 17, pp. 701 – 710, Sept. 2002.

[141] M. Depenbrock, V. Staudt, and H. Wrede, "A theoretical investigation of original and modified instantaneous power theory applied to four-wire systems," *Industry Applications, IEEE Transactions on*, vol. 39, pp. 1160 – 1167, July-Aug. 2003.

[142] L. S. Czarnecki, "Instantaneous reactive power p-q theory and power properties of three-phase systems," *Power Delivery, IEEE Transactions on*, vol. 21, pp. 362 – 367, Jan. 2006.

# List of Publications

## Journals

1. A. K. Gupta and A. M. Khambadkone, "A Space Vector PWM Algorithm for Multilevel Inverters based on Two-level Space Vector PWM", *Industrial Electronics, IEEE Transactions on, Volume 53, Issue 5 Oct. 2006 Page(s):1631 - 1639.*

2. A. K. Gupta and A. M. Khambadkone, "A General Space Vector PWM Algorithm for a Multilevel Inverter Including Operation in Overmodulation Range", *Power Electronics, IEEE Transactions on, Volume 22, Issue 2, March 2007 Page(s):517 - 526.*

3. A. K. Gupta and A. M. Khambadkone, "A Simple Space Vector PWM Scheme to Operate a Three-level NPC Inverter at High Modulation Index Including Over-modulation Region, with Neutral Point Balancing", *Industry Applications, IEEE Transactions on, Volume 43, Issue 3, May-June 2007 Page(s):751 - 760.*

4. A. K. Gupta and A. M. Khambadkone, "A Space Vector Modulation Scheme to Reduce Common Mode Voltage for Cascaded Multilevel Inverters", *Power Electronics, IEEE Transactions on Volume 22, Issue 5, Sept. 2007 Page(s):1672 - 1681.*

## Conferences

1. A. K. Gupta, A. M. Khambadkone and K. M. Tan, "A two-level inverter base SVPWM algorithm for a multilevel inverter", *30th Annual Conference of the IEEE Industrial Electronics Society - IECON*, November 2004, vol. 2, pp. 1823 - 1828.

2. A. K. Gupta and A. M. Khambadkone, "A General Space Vector PWM Algorithm for a Multilevel Inverter Including Operation in Overmodulation Range", *IEEE International Electrical Machines and Drives Conference - IEMDC* , May 2005, pp. 1437 - 1444.

3. A. K. Gupta and A. M. Khambadkone, "A General Space Vector PWM Algorithm for Multilevel Inverters Including Operation in Overmodulation Range, with a detailed modulation analysis for a 3-level NPC inverter", *IEEE Power Electronics Specialists Conference - PESC*, June 2005, pp. 2527 - 2533.

4. A. K. Gupta and A. M. Khambadkone, "A Simple Space Vector PWM Scheme to Operate a Three-level NPC Inverter at High Modulation Index Including Over-modulation Region, with Neutral Point Balancing", *IEEE Industry Ap-*

*plications Society Annual Conference*, Fortieth IAS Annual Meeting. Conference Record of the 2005 Volume 3, 2-6 Oct. 2005, Hong Kong, Page(s):1657 - 1664.

5. A. K. Gupta and A. M. Khambadkone, "A Space Vector PWM Scheme to Reduce Common Mode Voltage for a Cascaded Multilevel Inverter", *Power Electronics Specialists*, IEEE 36th Conference, Jeju, Korea on 18-22 June 2005 Page(s):1797 - 1803.

6. A. K. Gupta and A. M. Khambadkone, "Synchronous Space Vector Pulsewidth Modulation Based Close Loop Flux Control of a Grid Connected Cascaded Multilevel Inverter", *Power Electronics Specialists*, IEEE 39th Conference, Rhodes, Greece on 15-19 June 2008 Page(s):1358 - 1364.