BOTTOM-UP 1-D NANOWIRES

AND THEIR APPLICATIONS

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Abstract

One-dimensional semiconductor and metallic nanowires are of great interest for study due to their fascinating properties and size when compared to their bulk counterparts. This thesis focuses on the study of bottom-up synthesis of single-crystalline NiSi nanowires and $Si_{1-x}Ge_x$ nanowires via a bottom-up approach using a chemical vapor deposition (CVD) process. This approach may lead to many potential applications in using nano-scaled interconnections and thermoelectric devices.

Firstly, the growth mechanism of NiSi nanowire was systematically investigated and a detailed growth model was proposed based on experimental results. The nickel oxides on the surface play an important role in triggering the initial growth of NiSi nanowire due to the low melting point and the agglomeration of forming nano-droplets after heating. This leads to a vapor-liquid-solid growth with the aid of fast Ni diffusion before a vapor-solid growth to elongate the nanowire. In addition, it also provides a clean Ni surface for this initial epitaxial growth. The synthesis temperature was found to control the diameters of NiSi nanowires with an activation energy of ~1.72 eV, hence offering a predictable process window.

Secondly, long and uniform $Si_{1-x}Ge_x$ nanowires with a high concentration of Ge and various diameters were obtained using Au-catalyzed growth. It was found that the composition of Si and Ge varies along the individual stems of the nanowires in a slightly tapered profile and the concentration of Si gradually increases as the nanowire grows. The composition of Si and Ge also depends on the diameter of the nanowire.

Nanowires with diameters less than 30 nm exhibit an acute increase of concentration of Si. It was also found that Au compound at more than 1 atomic percentage are present in the upper part of bent stems, while the Au in the straight portions of stems was below the detection limit of energy-dispersive X-ray spectroscopy (EDS). The influence of temperature at the catalyst tip and the heat transfer along a nanowire stem were discussed, and these results indicate that thermal conductivity plays an important role during the synthesis of nanowires.

Keywords: Nanowire, NiSi nanowire, $Si_{1-x}Ge_x$ nanowire, Synthesis, Activation energy, Nanowire temperature, Nano-technology, Nano applications.

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Chapter 1

Introduction

1.1 Overview of Nanowire Materials and Applications

Nanostructures are defined as systems with sizes in the range of 1 to 100 nm in at least one dimension. A nanowire is an example of a one-dimensional (1D) nanostructure in which the sizes of two dimensions of a bulk material are reduced to such a range [1-3]. As compared to conventional bulk structure, a nanowire offers a high surface-to-volume aspect ratio and exhibits a quantum confinement effect, leading to fascinating properties and providing a large number of opportunities for intrinsic property studies and unique applications in a wide range of technologies.

A variety of nanowires, in the forms of single elements, oxides, nitrides, chalcogenide, silicides, and other compounds, have been reported and studied over the last few decades [1-7]. Semiconductor nanowires, which include a wide range of binary or ternary compounds and several metal oxides, have emerged as a type of nanowire suitable for extensive application in electronic devices, photonics, chemical sensors, photovoltaic cells, thermoelectricity, and other applications [1,6,8-26]. Due to the dominant application of silicon in the commercial semiconductor industry, and dramatically motivated by the scaling down of complementary metal-oxide-silicon (CMOS) field effect transistor (FET), single crystal silicon nanowires (SiNWs), in particular, have been comprehensively studied in the aspect of either fundamental properties or novel technological concepts.

A wide range of SiNW devices, including diodes, transistors, inverters, LED arrays, logic gates, chemical sensors and even bio-molecule analyzers, have been

developed and demonstrated, showing unique features and superior properties [16,27-37]. Furthermore, large-scale and multilayer assembly technologies have also been demonstrated [38-39]. However, the integration of SiNWs into mainstream ultra-large-scale integration (ULSI) technology has encountered challenges, such as the lack of a predictable approach to SiNW alignment and the precise control of SiNW synthesis. In addition, the efficiency of nanowire solar cells is far below their theoretical potential or even that of thin film solar cells due to the lack of high quality and well-aligned SiNW arrays, even though the diameters of SiNWs could be much larger than that for CMOS FET [40-45]. A better understanding and the development of effective techniques for the precisely controlled synthesis of nanowires is required for this technology to meet its potential.

Recently, the excellent thermoelectric properties of SiNWs were discovered, which prompted the investigation of the thermoelectric properties of nanowires as promising thermoelectric materials for potential applications in cooling and power generation [26,46-49]. In fact, the history of nanowire runs parallel with that of SiNWs, benefitting the study of nanowires of other materials for their possible applications.

1.2 Novel Properties of Nanowires

1.2.1 Mechanical Properties of Nanowires

As the grain size (d) of a polycrystalline solid decreases from a micrometer scale to a characteristic critical value (typically of the order of nm), the harness and stress yield change from hardening to softening proportionally to $d^{-1/2}$, mainly caused by the atomic sliding events at grains boundaries [50]. In contrast, as a result of the small lateral dimension in a single-crystalline 1D nanowire, the harness and yield stress are significantly stronger with the cause attributed to a lower defect density per unit length [3,51]. However, it is worthy to note that the surface or volume defects generated during fabrication or synthesis of nanowires may significantly degrade the

Young's modulus of SiNWs, such that it is much lower than that of a bulk wire [52].

1.2.2 Electrical Properties of Nanowires

1.2.2.1 Quantum Confinement

One-dimensional SiNWs exhibit noticeably different electrical properties from bulk structures due to the quantum confinement of electrical carriers. The electrical carriers are confined in the plane perpendicular to the nanowire, as the diameter of a nanowire is comparable to the Fermi wavelength (typically tens of nm for a semiconductor, and less one nm for metals). This restricts the motion of the carriers and thus results in a direct-gap-like energy band structure along the wire direction and the non-linear enhancement of the up-shift of band gap as the diameter of wire decreases [53-57]. This quantum confinement effect has been directly demonstrated by the size dependence of photoluminescence characteristics, and the scanning-tunneling spectroscopy measurement, which evaluates the band gap energy of SiNWs, shows that it increases with deceasing diameters from 1.1 eV for 7 nm to 3.5 eV for 1.3 nm (1.12 eV in the bulk Si) [56-57].

The conventional effective-mass theory (EMT), based on bulk-silicon parameters, and first-principles pseudo-potential methods were introduced to investigate the band gap and carrier properties [53-54,58-59]. The latter method, which most distinctive signature is the $1/d^n$ (where d is the diameter and $1 \leq n \leq 2$) size dependence, delivers calculation results in good agreement with the experimental results of nanowires in diameters of upon ~2 nm [19,54,56,58-59]. **Figure 1.1** compares the size-dependent band-edge shift effects between both methods, in which the EMT result is considerably matched with that of fist-principles pseudo-potential methods for these thicknesses not less than ~5 nm [58-59]. This suggests that the EMT method is still feasible for most of the applied engineering applications.

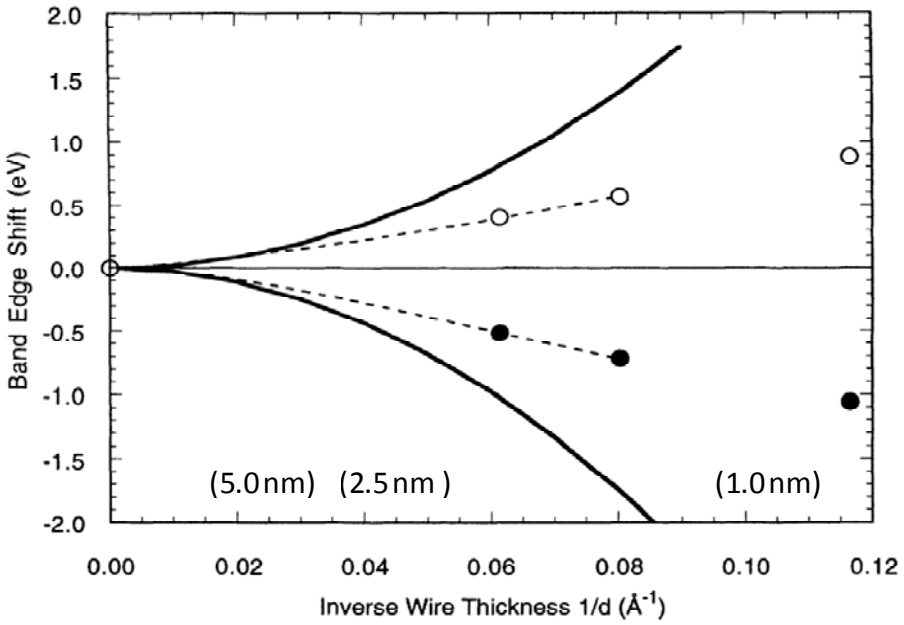

Fig. 1.1: The band-gap opening effect plotted against the inverse of the square silicon wire thickness. The band edge shifts of valence-band (filled circuit with dashed curve) and conduction-band (open circles with dashed curve) are calculated according to a first-principles pseudo-potential method, and EMT calculation results are presented in solid line [Adopted from Ref 58].

1.2.2.2 Electrical Conductivity Properties

1.2.2.2.1 Transition of Electrical Properties

Quantum confinement effect also occurs in nanowires of other materials and causes single-crystalline bismuth nanowires to undergo a transition from metal to semiconductor properties once the diameter drops below a transition diameter of ~52 nm. At this point, the conduction and valence sub-bands shift in opposite directions and eventually cause a change from narrow-band overlap to a positive band gap energy (E_g) of ~10 meV [60-62]. The intrinsic carrier density is generated by the thermal activation and increases exponentially with the temperature. The semiconductor-like temperature dependence makes the electrical conductivity (σ) of bismuth nanowires increase at higher temperature as described in **Equation 1-1:**

$$\sigma = \sigma_o \exp(-\frac{E_g}{2kT}) \quad \textbf{(1-1)}$$

where σ_o is a pre-exponential constant, k is Boltzamnn constant, and T is the absolute temperature [62]. This increase in the electrical conductivity is important for the special interest of bismuth nanowires in possible thermoelectric applications [61, 62].

1.2.2.2.2 Impurity Effect on Electrical Conductivity

Although the non-linear increase of E_g impacts the intrinsic carrier concentration and electrical conductivity of the SiNWs as the diameter decreases, the doping of impurities in the SiNWs has a profound impact on the carrier density and electrical conductivity. It is documented that the I-V measurement of SiNWs with diameters of ~15 nm, which was synthesized through Au and Zn catalyzed mechanism, possesses insulator-like characteristics, and the ionization and diffusion of the nucleating metal into the nanowires during further thermal anneal increase the conductance of SiNWs by as much as 4 orders of magnitude[63]. It was also reported that another set of SiNWs with diameters of ~20 nm shows a wide spread of resistivity which varies from > 10^5 Ω.cm to ~10^{-3} Ω.cm (2.3 x 10^5 Ω.cm in intrinsic bulk) [64]. Meanwhile, these doping impurities act as additional scattering centers or possible localization defects which may degrade the carrier mobility in SiNWs, and it is a great concern in the application of a FET [58,63-64].

1.2.2.3 Electrical Properties of Metallic Nanowires

The electric conductivity of metallic wire is reduced as the diameter of the wire is decreased to a range comparable or smaller than the mean free path of the electrons due to electron-surface, grain boundary, and surface roughness-induced scatterings [65- 66]. Compared to Cu, a single-crystal NiSi nanowire has significantly shorter electron mean free path (Ni: ~5 nm, Cu: ~39 nm), less grain boundaries, and has remarkably high failure current density (> 10^8 A.cm^{-2}) regardless of the diameters of

nanowires [65-69]. Hence, NiSi nanowires can maintain low resistivity similar to the value of bulk structure (~10 μΩ.cm) and minimize the electro-migration related failures due to the down-scaling interconnect, and also have another possible application in field emitters [67-70].

NiSi are intensively used for gate and source/drain material in current CMOS devices, indicating that the NiSi nanowire is a promising candidate for nanoscale interconnects in integrated circuits. This opens up the possibility of replacing tiny Cu wires in CMOS devices to enhance the electron-migration related reliability [70-74]. Thus, a controller synthesis of NiSi nanowires is an important step towards feasible engineering applications. Furthermore, abruptly elevated resistivity of NiSi nanowires fabricated by forming NiSi on patterned silicon rods is reported in the range of 13.0 to 22.7 μΩ.cm due to the existing grain boundary, suggesting that self-synthesis of a single-crystal NiSi nanowire is an important aspect [75-77].

1.2.3 Thermoelectric Properties

1.2.3.1 Thermal Stability of Nanowires

Zero-dimensional nano-particles have high surface-to-volume ratios and a melting temperature inversely proportional to their effective radius. This is caused by the surface atoms having fewer nearest neighbors, resulting in less constraint on their thermal motions [78-79]. The existence of an extensive surface also alters the thermal stability of a 1D nanowire with a significant depression of the melting point against the inverse of the diameter of nanowire. A transmission electron microscope (TEM) observation shows a Ge nanowire with the diameter of 55 nm starts to melt from two ends of the wire, in which the curvature is the highest, at a temperature of ~650 °C (the melting point for bulk Ge: 930 °C) [80]. This interface-driven instability also causes melting initiated from the tip and extends further to the stem of a SiNW without an exact temperature measurement reported [46].

1.2.3.2 Thermal Conductivity of Nanowires

Phonons, which in physics are a quantum mechanical version of vibrational motion according to the principle of wave-particle duality, play a major role in the thermal and electrical conductivities of a material. As the diameter of a nanowire is reduced to the range of a phonon mean free path (~300 nm in silicon at room temperature), the frequency-dependent phonon-boundary scattering is greatly increased and hence reduces the phonon mean free path and phonon group velocities along the long axis of a wire, thus leading to a further reduction in the thermal conductivity as the result of boundary scattering and phonon confinement [19,47-48,81-83].

1.2.3.3 Thermoelectric Properties of Silicon Nanowires

The concept that the thermoelectric properties of a 1D conductor depends strongly on the diameter of the wire was first proposed by Hicks and Dresselhaus in 1993 [84]. This is due to the reduction in the lattice thermal conductivity as the electrons are confined to move in a single dimension and the phonons scatterings are increased from the surface of wire [84]. SiNWs, a semiconductor material in which the thermal conductivity is dominated by phonon contribution instead of electron contribution in metal, have been experimentally confirmed that their thermal conductivities strongly depend on the diameters of the SiNWs, and it has been demonstrated that there is an up to 100-fold improvement of the SiNWs ZT (~0.6 at room temperature or ~1 at 200 K) over bulk silicon (~0.01 at 300 K) [47-49,82,85]. This remarkable improvement shows that SiNWs in small diameters can be an efficient thermoelectric material.

The heat transport of a thermoelectric material is characterized by a figure of merit ZT, which is dimension-less and is expressed as **Equation 1-2:**

$$ZT = \frac{S^2 T \sigma}{k} \qquad \textbf{(1-2)}$$

where S, σ, k, and T are the Seebeck coefficient (the thermoelectric power, measured in V/K), electrical conductivity (measured in S/m), thermal conductivity (measured in W/mK) and absolute temperature (measured in K), respectively [26,47-48]. The difficulty in improving ZT to a desirable value of > 3 at room temperature lies in that S, σ, and k are inter-dependent and often adversely affect each other [26,49,84]. For example, a lower density of carriers leads to a higher value of S and a lower value of σ, and possibly little impact on the value of k [49]. From engineering optimization, such as tuning the doping, the nanowire size, and surface roughness, it can be expected that these changes will enhance the thermoelectric performance of SiNWs [47-49].

1.2.3.4 Thermoelectric Properties of $Si_{1-x}Ge_x$ Nanowires

In an intrinsic SiNW, the long-wavelength acoustic phonon scattering by the nanowire boundary is the dominant factor in thermal reduction [47,86]. With the introduction of impurities, for example, a block-by-block Si/SiGe superlattice nanowire, the scattering of phonons in the Si-Ge segments is the dominant mechanism contributing to the thermal conductivity reduction. This is attributed to that the short-wavelength acoustic phonons are effectively scattered by the heavier atom-scale point imperfections in addition to the nanowire boundary scattering [87-88].

A molecular dynamics (MD) simulation also shows that the doping of heavier isotopic atoms reduces the thermal conductivity of SiNWs, and a small ratio of such random impurities in SiNWs results in a large scale decrease of thermal conductivity [89]. This suggests that $Si_{1-x}Ge_x$ nanowires, which could be assumed as Ge-doped SiNWs, may obtain more promising thermal conductivity properties than those of SiNWs. Furthermore, Majumdar reports that using heavier atoms in semiconductor materials to cause alloy scattering of the short-wavelength acoustic phonons is the

only way is to reduce k without substantially affecting S and σ, which results in the increase of ZT [26]. Thus, it is of interest to investigate the thermoelectric properties of $Si_{1-x}Ge_x$ nanowire with different diameters and composition.

1.3 Synthesis of Nanowires

1.3.1 Top-down Approach

Nanowires have been prepared by patterning and etching techniques in diverse ways, in which the obtained nanowires inherit the properties of the substrates [47,90-96]. This top-down approach provides a feasible way to create large-area nanowire array. However, the removal of nanowires from the substrate may cause damage to the nanowires. Furthermore, the geometries of Si nanowires are usually uniform with diameters in the range of micrometers, and it requires a precise patterning technique in order to obtain nanowires of small diameters.

1.3.2 Bottom-up Approach

1.3.2.1 Background of Bottom-up Approach

In contrast, the bottom-up approach is a direct growth of high quality nanowire in a variety of materials onto a substrate, providing a suitable approach for fundamental properties study and hierarchical assembly of nanowires as functioning devices [10,14,20-21,29-30,34,38-39,68,97-100]. Several methods have been successfully developed to synthesize bottom-up SiNWs. These methods include several specific strategies and different mechanisms.

1.3.2.2 Supercritical Fluid-Solid-Solid Approach

A supercritical fluid-solid-solid (SFSS) solution-phase growth produces bulk quantities of nanowires. However, this process requires high pressure and a high temperature above the critical point of the solvent, which may result in solvent

contamination in nanowires [101-103].

1.3.2.3 Solid-Liquid-Solid Approach

A solid-liquid-solid (SLS) solid-phase growth is a process in which a metal catalyst on the Si substrate is thermally heated up to around the eutectic point to form metal-Si alloy, then followed by rapid cooling to synthesize dense SiNWs [104-108]. However, SLS growth produces nanowires with diameters as large as tens of micrometers. Furthermore, the nanowires have non-straight stems and a rough surface. It is important to note that they are often described as amorphous structures.

1.3.2.4 Laser-assisted Catalyzed and Oxide-assisted Approach

A laser-assisted catalyzed growth (LCG) and an oxide-assisted thermal evaporation growth use laser ablation or thermal heating of a solid target to generate catalyst-contained silicon source gases which further condense at relatively cooler area to produce nanowires via a vapor-liquid-solid (VLS) mechanism [46,109-113]. This is done with the presence of a metal or SiO_x catalyst. LCG produces nanowires in large quantities, but the nanowires are generally sponge-like and disorderly. The oxide-assisted method is unique in that it is able to synthesize metal-free nanowires; however, to date results are limited on obtaining well controlled synthesis of nanowires using this method.

1.3.2.5 Vapor-Phase Approach

1.3.2.5.1 Synthesis Mechanism

Vapor-phase catalyzed methods are a promising technique to achieve precisely controlled nanowires in various materials. They are done with the use of a metal catalyst, in which the vapor-solid-solid (VSS) method grows nanowires at a temperature much lower than the eutectic point and vapor-liquid-solid (VLS) method requires a temperature around or above the eutectic point [1-3,6,19,21]. Taking the Al

catalyst as an example, the VSS growth occurs at the reduced temperature and silicon-less region as illustrated in phase diagram **Fig. 1.2**, while the VLS growth occurs at the elevated temperature and silicon-rich region [114-115]. In particular, the VLS approach allows unique material combinations and seems to be the most versatile in terms of feasibility, partially because Au owns the Au-Si eutectic point as low as 363 °C among the series of metal catalysts [114].

Figure 1.2 and **Figure 1.3** illustrate the VLS growth mechanism: gaseous silicon absorbs at the catalyst surface and forms alloy at a temperature around or above the eutectic point. This acts as an energetically favored site for vapor-phase reactant adsorption; more silicon dissolves in the droplet and leads to a supersaturation. Thus, at Si-rich region, Si in the droplet diffuses to and precipitates at the liquid-solid interface and nucleates for crystallization. This crystallization of Si at the liquid-solid interface leads to the formation of a nanowire stem right below the alloy droplet, and results in the alloy droplet forming a semispherical cap at the tip of the nanowire. Hence, this alloy cap functions as the catalyst and enables the further elongation of the stem of the nanowire [1-2,135,138]. VSS also takes part in the gas-solid interface and may generate cone-shape nanowires; hence, in-situ surface passivation is widely applied to limit the lateral growth besides the optimization of other process parameters.

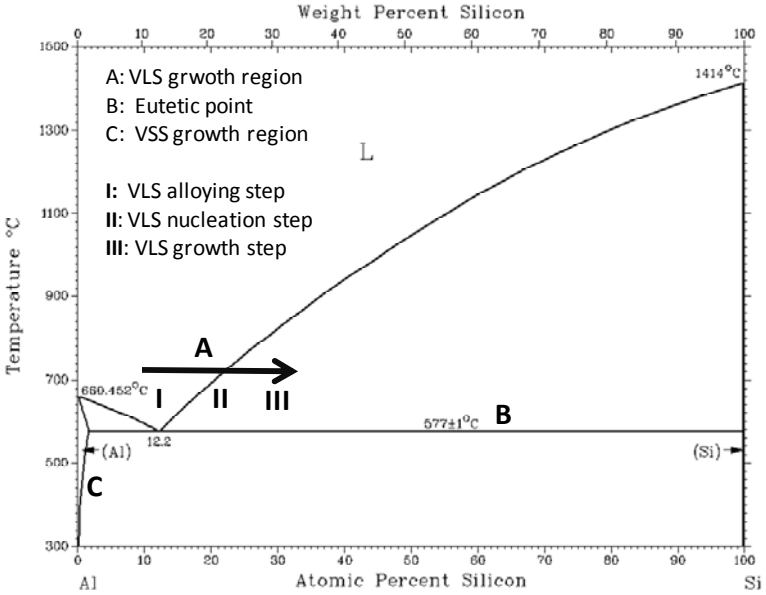

Fig. 1.2: The Al-Si binary alloy phase diagram illustrates the temperature and silicon regions for VLS and VSS growth [Adopted from Ref 114-115].

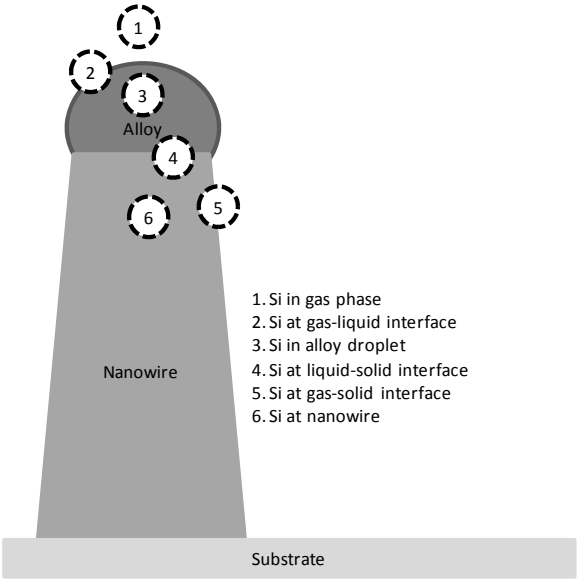

Fig. 1.3: Illustration of the VLS growth mechanism

1.3.2.5.2 Diameters of Nanowires

VSS is capable of producing long and straight nanowires, but these nanowires are generally in cone shapes [115-117]. On the other hand, nanowires in uniform diameters along the stems can be synthesized via VLS, while they are usually in

disorder.

In VLS growth, the diameter of nanowires is mainly determined by the size of the nano-particle, and an elevated temperature also increases the diameter of nanowire due to the formation of a larger size metal-Si droplet and Ostward ripening of Au [111,118-124]. Using of SiH_4 gas instead of $SiCl_4$ allows the application of a lower temperature and hence, synthesizing of smaller diameter nanowires; while SiNWs in the diameters of < 20 nm are extremely flexible, and low temperature might cause more growth defects in them [125-128]. SiNWs with diameter as small as ~3 nm corresponding to the theoretical limit of 2-3 nm via VLS growth have been achieved [120,127,129]. In contrast, well-aligned Si array may require less defect nanowires in the diameters of above 50 nm, usually produced by $SiCl_4$ at a high temperature (800-1050°C) [121,126,130-133].

Depending on the partial pressure of the silicon source gas, a reduced diameter of SiNW has two types of impact on the growth velocity: 1) to decrease growth velocity at higher partial pressure corresponding to the rate-determining gas-liquid interface decomposition [121,127,134]; 2) to increase growth velocity at the conditions of low partial pressure and relatively lower temperature [98,135]. After considering another rate-determining crystallization step at the liquid-solid interface and the diameter dependence of the solubility of Si in the metal-Si alloy which is related to supersaturation in the alloy, Schemidt *et al.* have elaborated the correlation between pressure dependence and diameter dependence of the growth velocity, as well as the temperature dependent growth [136-138]. Whereas, the diameter dependence of composition effect for Si compound nanowires is limited.

The consuming of Au in the alloy droplet leads to a reduction in diameter in the most upper part of nanowire and eventually terminates the VLS growth. The reason attributed to this result is that the Au droplet wets the nanowire surface and therefore it consumes Au in the alloy [124]. However, there might be another possibility that the reduced thermal conductivity along the nanowire causes lower temperature at the

tip of nanowire and thus less silicon can diffuse into the droplet as the temperature continues to decease. It is also observed that the growth velocity is gradually saturated as SiNW grows. The author attributes this phenomenon to the possibility of the decrease in temperature of a nano-catalyst [127]. Thus, understanding of the thermal conductivity of nanowires may result in better synthesis of nanowires.

1.3.2.5.3 Oriented Growth of Nanowires

An electric-field-directed growth induces large dipole moments and leads to large aligning torques in growing carbon nanobutes (CNTs), forcing the CNT to grow parallel to the electric field and thus obtaining oriented growth of CNTs [139-142]. Furthermore, a plasma enhanced chemical vapor deposition (PECVD) method provides a capability to synthesize vertically aligned CNTs on a large scale level [132,143-144]. A single vertically aligned tungsten nanowire probe was synthesized through filed-emission induced growth, in which the sufficiently high field ionizes the precursor gas near the tip and attracts these ionized particles to the tip of nanowire [145-146]. On the contrary, these methods have limited effects to synthesize a uniform array of aligned SiNWs [125,143,147]. Thus, template-directed growth methods are widely applied in order to obtain aligned SiNWs and arrays [134,148-149]. However, the diameters and the surface morphology of SiNWs are greatly limited by the templates, and the nanowires may be damaged during the post-synthesis removal of the templates.

An epitaxial crystal growth on a single-crystal substrate is particularly powerful to achieve selective growth in the preferential direction and possibly the precise orientation control of nanowire arrays [1,8,17,21,150]. A VLS epitaxial synthesis of SiNWs on a Si(111) substrate is applied to obtain vertically aligned SiNW arrays, while the critical growth conditions of the combination of an increased temperature and a reduced pressure lead to diameters usually in the range of μm [48,98,121,125-126,130-131,133,151]. In contrast, a VSS epitaxial growth results in well-aligned SiNW array with diameters as small as ~35 nm at a reduced temperature

in an ultra high vacuum [115]. This indicates a promising method towards precisely controllable synthesis of oriented nanowire with a small diameter.

1.4 Objective of the Research

The objective of this thesis is to address 1D bottom-up nanowire synthesis and the potential applications of nanowires. The new materials of metallic NiSi nanowires and semiconductor $Si_{1-x}Ge_x$ nanowires will be investigated.

1.5 Outline of the Thesis

The unique material features and current applications of nanowires have been briefly introduced in **this chapter**. Background information has been provided for electrical conductivity and thermoelectric properties of nanowires, as well as their possible applications and the challenges ahead. Recent technology development to address the precisely controllable synthesis of nanowires is also presented in this chapter.

Chapter 2 explores the feasibility of synthesis of single-crystalline NiSi nanowire via the chemical-vapor-deposition method. The role of surface oxide is investigated, and the growth mechanism is studied, in which the Ni_2O_3 with the coexistence of NiO phase agglomerates after heating and triggers the initial growth of the NiSi nanowire. It is also found that the diameter of the NiSi nanowire is mainly controlled by the synthesis temperature with an activation energy of ~1.72 eV.

In **Chapter 3**, Au-catalyzed VLS growths are applied to synthesize single-crystalline $Si_{1-x}Ge_x$ nanowires. Various synthesis conditions and preparation of substrates are studied in order to obtain uniform and long nanowires with difference diameters and in different compound ratio for the thermoelectric properties study. It is found that the Ge atomic percentage gradually decreases as the nanowire grows, and the compound ratio in $Si_{1-x}Ge_x$ nanowire is diameter-dependent. It is also found that

Au compound exists in the upper part of few nanowire stems. This suggests the thermal conductivity along the nanowire stem plays an important role in the synthesis of nanowire.

Chapter 4 gives an overall conclusion of this study and suggests possible further work.

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Chapter 2

Synthesis of Nickel Mono-Silicide Nanowire by Chemical Vapor Deposition on Nickel Film

2.1 Introduction

As discussed in **Chapter 1.2.2.3,** nickel mono-silicide nanowire (NiSi-NW) is attractive for potential applications in down-scaling interconnections and field emitters. NiSi-NW has been successfully synthesized by Ni-catalyzed growth with different kinds of silicon source [1-5]. Ni-catalyzed growths are also able to synthesize Si nanowires via the solid-liquid-solid (SLS) or vapor-liquid-solid (VLS) mechanism at 900 to 1100 °C in a chemical vapor deposition (CVD) or a furnace tube, at which point the temperature is near the eutectic temperature of Ni-Si (~964 °C) [6-12]. However, the synthesis mechanism of NiSi-NW has not yet been comprehensively understood.

In the work of Kim *et al.,* a metal-induced growth (MIG) mechanism which is a solid-state reaction was attributed to the growth mechanism of NiSi-NW by sputtering Si particles on a Ni layer at 550 to 600 °C, which includes the stages of Ni groove formation, agglomeration, clustering, and NiSi-NW growth [1-3]. Lee *et al.* used a Ni catalyst, obtained from treating $Ni(NO_3)_2 \cdot 6H_2O$ for 5 minutes at 700 °C in H_2 ambient, to grow carbon-coated NiSi-NWs with SiH_4/H_2 gases at 700 °C in a radio-frequency-induction heating CVD reactor. The study concluded that the nucleation site for the NiSi-NW growth is provided by the Ni catalyst with a claim that the growth mechanism is not well understood [4]. In another work growing single-crystalline NiSi-NWs on a Ni surface with silane gas at 370 to 420 °C, Decker *et al.* proposed a three-step directed growth model based on a vapor-solid mechanism:

Si decomposition from SiH_4 on Ni surface, Ni diffusion into silicon, and nanowire formation; while other phases like Ni_2Si, and Ni_3Si_2 were detected depending on unpublished growth conditions [5]. Such metal-assisted vapor-solid mechanisms are popularly proposed for metallic silicide nanowire synthesis because the relatively low degree of supersaturation in vapor-phase favors one-dimensional morphologies due to limited nucleation [13-18]. Nevertheless, it is emphasized that a certain amount of surface oxides [NiO_x, $Ni(NO_3)_2$, SiO_2] is crucial to form nanowires in large amounts [13,15,17]. Furthermore, a possible VLS-like mechanism is suggested for the growth of FeSi nanowires by Schmitt *et al.*, who found that the thin surface oxide is the key to the success of growing FeSi nanowires on a Si substrate [19]. These studies reveal that the Ni catalyst provides a nucleation site for the NiSi-NWs growth and acts as a fast diffuser towards the tip of NiSi-NW during growth, and indicate that the NiSi-NW formation is initiated by agglomerated triggers. However, there is not yet comprehensive understanding of the triggers of NiSi-NW growth. In addition, there is limited study of the dominant factor controlling the diameter of the Ni-catalyzed NiSi-NWs.

In this study, NiSi-NWs have been synthesized on Ni films with SiH_4/H_2 gases in a CVD system, and NiSi-NW growth from different substrate structures and surface treatments applied on Ni film have been investigated. The possible involvement of VLS in the early stage of nanowire growth has been studied, suggesting that surface nickel sesquioxide (Ni_2O_3) triggers initial growth of NiSi-NWs. It also shows that the diameter of NiSi-NWs is controlled by the synthesis temperature with an activation energy of ~1.72 eV. A detailed growth model is established with the estimation of minimum synthesis temperature, enabling the prediction and tuning of the diameters of NiSi-NWs.

2.2 Experiments

As illustrated in **Fig 2.1**, p-type Si (100) wafers were first cleaned by diluted

hydrofluoric acid (DHF), following which they were split for the deposition of ~400-nm-thick SiO_2 and ~200-nm-thick sputtered TaN in order to promote the adhesion of nickel film and to block nickel diffusion to the silicon substrate. Following this, electron-beam-evaporation was used to coat a thin layer of Ni films (~20 nm) before nanowires were synthesized in a CVD chamber at 550 °C. The synthesis consists of 3 consecutive steps: heating for 3 min; treatment in the flow of 1000 sccm H_2 at 25 Torr for 1 min; and growth with SiH_4/H_2 gases in the flow rate of 200/200 sccm at 25 Torr for 10 min.

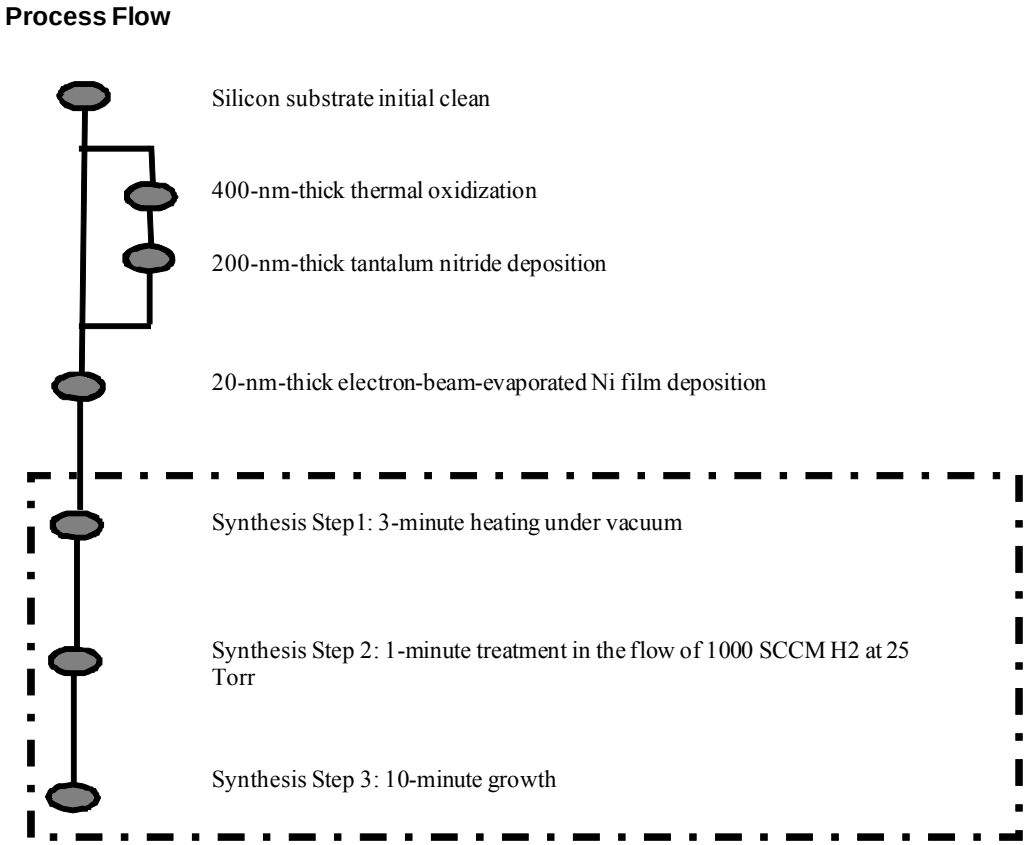


Fig. 2.1: The process flow for NiSi-NWs synthesis: the three steps of synthesis were sequentially executed in a thermal-heated CVD chamber at 550 °C, in which the SiH_4/H_2 gases had a flow rate of 200:200 SCCM at 25 Torr and provided the silicon source for nanowire growth. Oxygen plasma treated Ni film, various growth parameters, and different thickness of Ni film were also employed in this experiment.

To investigate the effects of process conditions on the growth of NiSi-NWs,

various parameters were adjusted, including synthesis temperature, surface treatments, synthesis pressures, diluted gases, and the thickness of nickel film. The growth temperature was chosen in such a range to provide sufficient thermal energy for NiSi formation, while not forming any Ni_2Si in the presence of excess Ni, also not further transiting NiSi to $NiSi_2$ in the presence of a temperature above 700 °C and excess silicon [12,20-22]. These physical and chemical properties of films or nanowires were characterized by various analysis techniques, including X-ray photoelectron spectroscopy (XPS), scanning electron microscopy (SEM), high resolution transmission electron microscope (HRTEM) and energy-dispersive X-ray spectroscopy (EDS).

2.3 Results and Discussion

2.3.1 Surface Oxides on Nickel Film

Figure 2.2 shows the XPS results of the as-deposited Ni film on a Si substrate (Ni/Si system), and the XPS binding energies for possible Ni-Si-O compounds are listed in **Table 2.1** [23-25]. The Ni spectra and their curve fittings show that there are other compounds besides Ni on the surface of the film. The main peak at 852.5 eV is traced to the Ni-Ni bond, and the strong secondary peak at 855.0 eV corresponds to Ni-O bonds, reflecting a thin layer of surface oxides on the Ni film. Similar surface oxidation also occurs on inert metals: oxygen molecules can be chemisorbed on Au nano-particles with a typical binding energy at 0.5-1.5 eV without breaking Au-Au bonds; platinum can also be covered by atomic oxygen up to 2.9 monolayers [26-27]. Furthermore, relative to the 100% normalization intensity of the main peak in Ni 2p spectra, high intensity of O 1s spectra reveals that there is more than one type of oxide compounds existing on the surface of the Ni film. The observed peaks at 531.3 and 529.2 eV in O 1s spectra indicate the compounds of Ni_2O_3 and NiO, respectively.

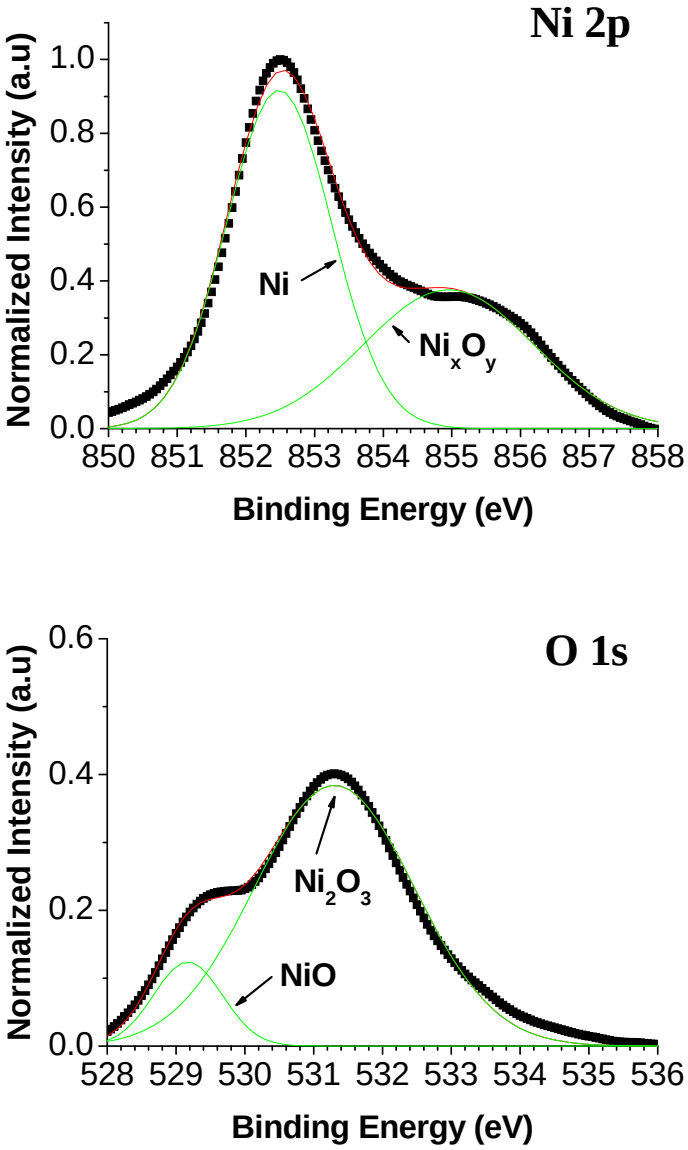


Fig. 2.2: XPS results and the curve fittings of Ni 2p and O 1s spectra of Ni film deposited on silicon substrate.

Table 2.1: Binding energy (BE) and melting point for possible Ni-Si-O compounds

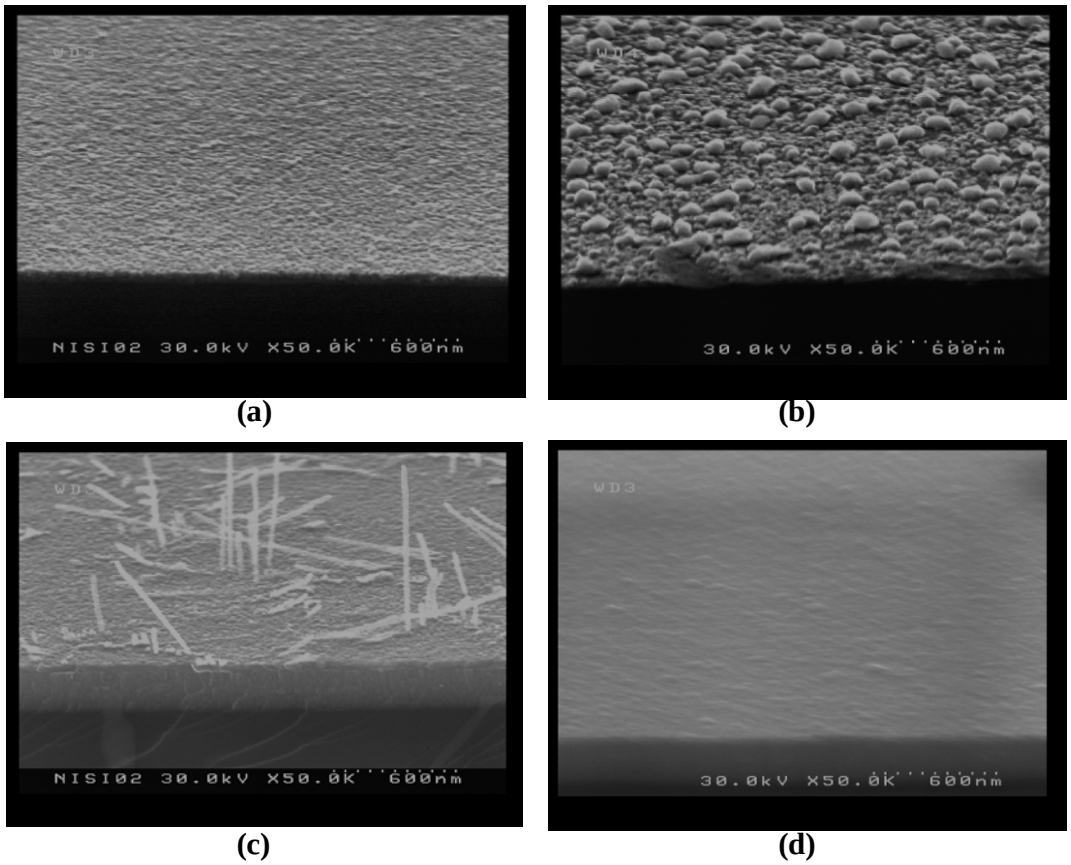
Compound	BE for Ni (eV)	BE for O (eV)	BE for Si (eV)	Melting temperature (ºC)	Reference
Ni	852.7			1455	23, 24, 25
NiO	854.7	529.6		1957	23, 24, 25
Ni_2O_3	855.9	531.6		~600	23, 24, 25
Si			99.4	1414	23, 24, 25
SiO			101.7		23
SiO_2		532.9	103.5	1713	23, 24, 25
NiSi	853.5		99.1		23, 24
Ni_2Si	853.0		99.0	1255	23, 24, 25
$NiSiO_3$	856.5	532.3	103.3		23, 24
Ni_2SiO_4	856.1	531.9	102.9		23, 24

In the VLS mechanism, a catalyst-contained alloy in liquid phase plays an important role in reducing the activation energy at both vapor-liquid and liquid-solid interfaces and triggers the growth of nanowires [28-30]. Nickel sesquioxide Ni_2O_3 owns a much lower melting temperature at ~600 °C than those of Ni and NiO at above 1000 °C, and Ni-Si eutectic temperature at 964 °C or NiSi melting temperature at 992 °C [11-12]. This melting temperature, which is close to the optimum NiSi-NW growth temperature at 550 to 600 °C, implies that Ni_2O_3 may be involved in the NiSi-NW synthesis because it melts and grooves to droplet, thus enhancing Si diffusion and triggering nanowire growth via the VLS mechanism. On the contrary, the surface oxide of Al_2O_3 with a high melting temperature blocks Si diffusion into Al and limits Al-catalyzed Si nanowire growth via the VLS mechanism [31]. Recent studies also discovered the impact of oxygen on the function of the Au catalyst in VLS growth of Si nanowire. These studies show that the exposure of the Au catalyst to oxygen can prolong the droplet volume, whereas a thin layer of silicon oxide on top of Au restrains nucleation and nanowire growth [32-33].

2.3.2 NiSi Nanowire Synthesis

2.3.2.1 NiSi Nanowire Synthesis on Nickel Film

Figure 2.3(a) and **Figure 2.4** show SEM images and the XPS results of the Ni/Si system after synthesis with SiH_4/H_2 gases. A single layer of grains with uniform diameters of ~40 nm is observed laying on the silicon substrate in the cross section, while none of the nanowires were found. This increase in film thickness, together with the reduction of sheet resistance from 11.54 to 6.04 Ω/square after synthesis, indicates the formation of nickel silicide. The XPS results reveal that NiSi is the main surface compound without Ni traced, and certain compounds of $NiSi_xO_y$ (corresponding to Ni_2SiO_4 and $NiSiO_3$) are traced [**Fig.2.4**]. Nickel is a fast diffuser during annealing with silicon, and forms NiSi at a temperature of 400 to 600 °C by diffusion control with activation energy of 1.6 eV and nucleation energy of 0.93 eV, and also further forms grains due to the agglomeration of NiSi at around 600 °C with a higher activation energy of 2.9 eV [12,22]. Another silicon source from SiH_4 gas simultaneously deposits on to the top of Ni film to form NiSi and creates a relatively smooth surface with a small amount of $NiSi_xO_y$ coexisting on the surface. Furthermore, none of peaks of NiO/Ni_2O_3, Si, and SiO_2 can be observed in XPS traces, suggesting that SiH_4 dissolves into heated nickel oxides on the surface of the film and forms $NiSi_xO_y$.



(a) **(b)**

(c) **(d)**

Fig. 2.3: SEM images of Ni film on silicon after a synthesis process with (a) SiH_4 and H_2 gases, and (b) H_2 gas only, and Ni film deposited on $TaN/SiO_2/Si$ substrate after synthesis process with (c) SiH_4 and H_2 gases, and (d) H_2 gas only.

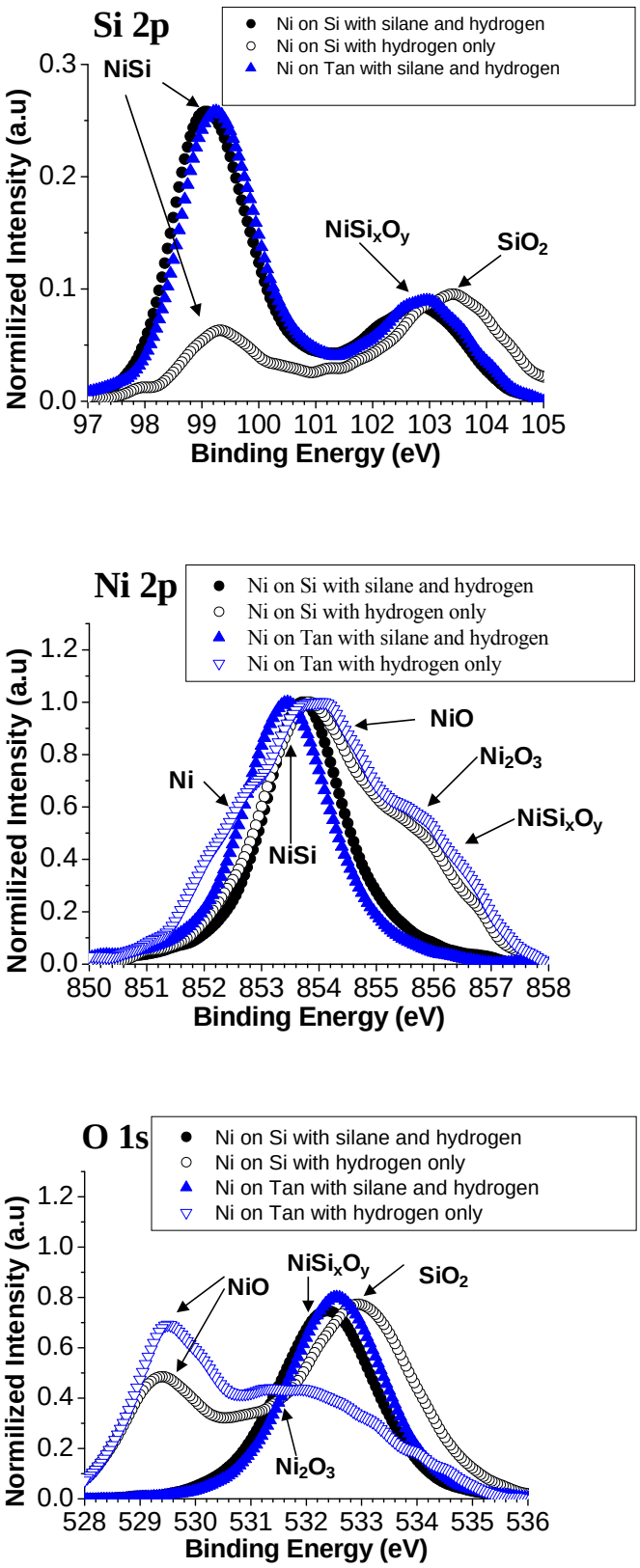
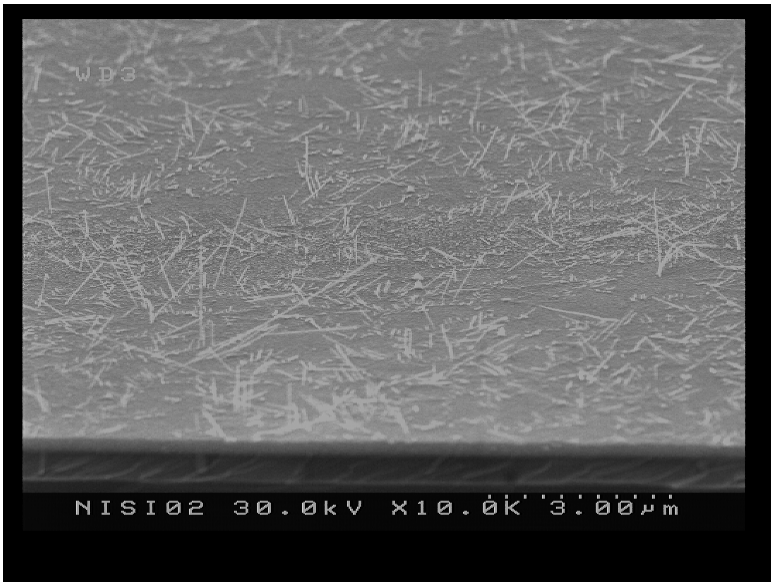


Fig. 2.4: XPS results of Si 2P spectra, Ni 2p spectra, and O 1s spectra of Ni films after synthesis process.

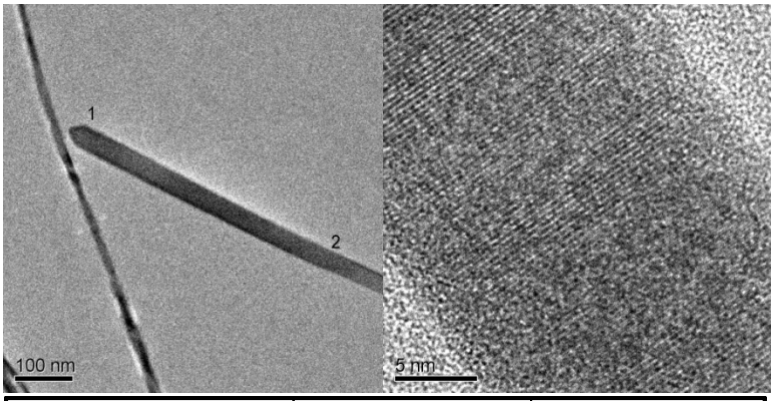
In contrary, as shown in **Fig. 2.3(b)**, there are discrete ball-like clusters with typical diameters of 90 to 120 nm agglomerated among small grains on the surface after synthesis with H_2 gas without SiH_4 gas, in which nickel reacts with the only silicon source of underneath silicon substrate. Although XPS results [**Figs. 2.4**] show that NiSi is the main compound, there are oxygen compounds in certain amounts. Two large peaks of NiO and SiO_2 with the weak presence of Ni_2O_3 dominate the oxygen compounds [**Fig. 2.4**], indicating that Ni_2O_3 changes phase and NiO remains on the surface without reacting with the substrate silicon. This phenomenon agrees with other observations of the impact of oxygen on the formation of NiSi in which oxygen in Ni or Si inhibits NiSi-formation. Ni is not likely to react with SiO_2 at the temperature of 400 to 600 °C, or it is unable to form a NiSi film when annealing excess oxygen-contaminated Ni film on a Si substrate, instead of forming a compound at a ratio of Ni: O: Si at 0.11: 0.60: 1 [12,34]. Considering the fact that a temperature of ~1000 ºC is needed to heat up NiO in order to obtain a Ni-O-Si quasi-liquid alloy, Ni_2O_3 is possibly the compound to induce the agglomeration of surface nickel oxide and to further form ball-like clusters [35]. Regardless, the agglomeration of NiSi is unable to trigger NiSi-NW growth, and the consumption of nickel to silicon substrate leads to no nanowires being synthesized.

A Ni/TaN/SiO_2/Si system was developed to induce a TaN layer as a diffusion barrier. The purpose of the diffusion barrier is to prevent Ni from diffusing into the silicon substrate or reacting with SiO_2. This resulted in nanowires obtained on such a system after synthesis with SiH_4/H_2 gases, which provided the only silicon source for the nanowire formation and the NiSi grains. As shown in **Fig. 2.3(c) and Fig. 2.5(a)**, the growth of the nanowires is either normal or at an angle to the surface, and none of nanowires has a hemispherical cap on the top of nanowires among these examined at SEM and TEM. This kind of cap shows the typical characteristics of nanowires obtained via VLS growth. Furthermore, VLS growth tends to generates kinking in nanowires, mainly due to the instabilities of the alloy droplet at the liquid-solid interface. These nanowires do not encounter this kinking phenomenon, and it reflects

and coincides with the epitaxial growth of nanowire on the NiSi layer [2, 36]. For example, it is noticed that none of the nanowires has a diameter that is bigger than the NiSi grains size of ~43 nm, and the diameters of nanowires are uniform in the range of 18-28 nm with a typical value of ~23 nm.



(a)



	Ni Atomic Content (%)	Si Atomic Content (%)
Tip (Label 1)	48.99	51.01
Stem (Label 2)	47.22	52.78

(b)

Fig. 2.5: (a) SEM images of Ni film deposited on TaN/SiO_2/Si substrate after synthesis process with SiH_4 and H_2 gases, and (b) TEM images and EDS result of nanowire.

Moreover, the nanowires also own a single-crystalline structure with a spear-shaped tip as shown in **Fig. 2.5(b)**. In-situ EDS measurement shows that the

Ni:Si atom ratios at the stem (0.90:1) and the tip (0.96:1) have good agreement with single-crystalline NiSi composition. However, unlike the diameter dependence of growth velocity for silicon nanowire via the VLS method, these nanowires have a wide spread of lengths of several um with existence of some thick and short nano-whiskers [37]. This suggests that the VLS mechanism is not the mechanism which elongates the length of nanowire.

This Ni/TaN/SiO_2/Si system is also employed to synthesize with H_2 gas without SiH_4. As shown in **Fig. 2.3(d)**, dense island-shape blisters are spread over the surface with a large variation in size, indicating the exhibition of agglomeration phenomenon. **Figure 2.4** shows that nickel does not get transferred to NiSi and remains in the film, and NiO becomes the dominant oxygen compound with the decrease in concentration of Ni_2O_3 after H_2 deoxidizes Ni_2O_3.

These results suggest that the surface nickel oxides agglomerate first and then change to a liquid state during the NiSi-NW synthesis, thus enhancing the adsorption of SiH_4 and forming complex Ni-O-Si quasiliquid droplets, therefore enabling the high concentration of silicon source to be absorbed into the droplets and diffusing towards the liquid-solid interface inside the droplets. Compared to a vapor-solid interface, a liquid phase generally provides a silicon diffusion coefficient two orders higher, and reduces the activation energy of nucleation for the incorporation of the material in a crystal lattice at the liquid-solid interface [28-29]. Hence, these droplets provide the sites for the initiation of NiSi-NWs with the aid of fast Ni diffusion.

2.3.2.2 NiSi Nanowire Synthesis on Nickel Film after Oxygen Treatment

Nickel film expands its volume and forms grains when it reacts with SiH_4 during the nanowire synthesis process. Therefore, these grains may cover the agglomerated Ni-Si-O droplet with a relatively smaller size located at the foot of nanowire. Thus, in order to further investigate the role of nickel oxides, the surface of nickel film in the Ni/TaN/SiO_2/Si system received oxygen plasma treatment before synthesis. In the

inductively coupled plasma, oxygen ions were accelerated through the plasma ion sheath and punched into the nickel film to the depth of up to several nm. Meanwhile, these bombardments also raised the surface temperature and made the surface oxide agglomerated. As can be seen in **Fig. 2.6**, blister-like dots of various diameter sizes up to 200 nm can be found on the surface. Furthermore, the XPS results [**Fig. 2.7]** show the radical decrease of Ni peak and the radical increase of both Ni_2O_3 and NiO peaks, indicating that a thick layer of nickel oxide has been formed after oxygen plasma treatment.

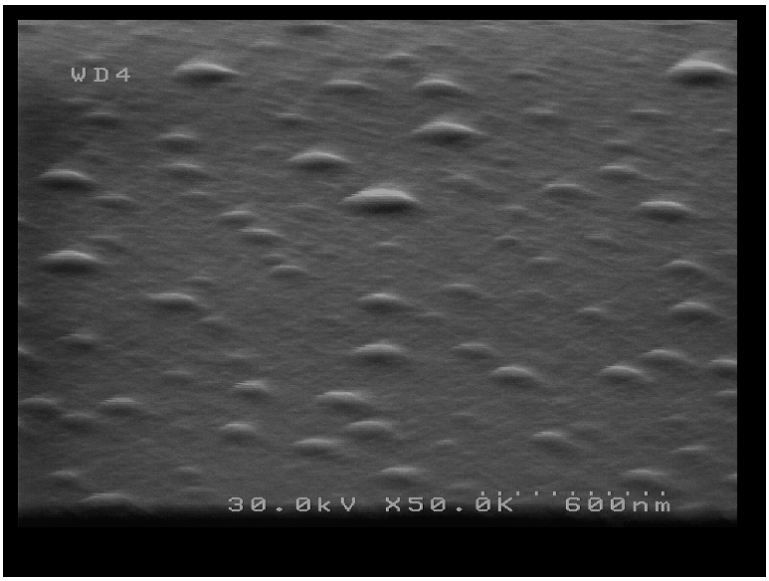


Fig. 2.6: SEM image of Ni film after receiving oxygen plasma treatment.

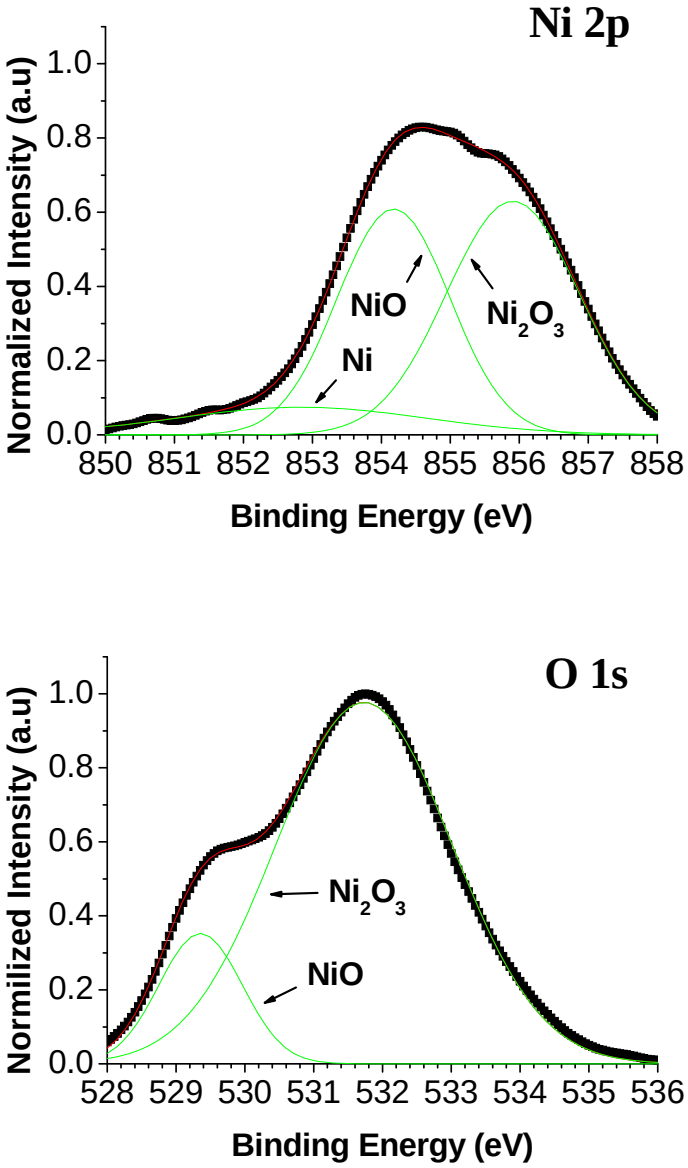


Fig. 2.7: XPS result and their curve fittings of Ni film after receiving oxygen plasma treatment.

The Ni film further proceeded to the synthesis of nanowires, and heavily agglomerated clusters were present as expected. These thicker non-conductive clusters on the surface impact the clarity of the SEM image, as shown in **Fig. 2.8**. Straight nanowires grow through these massive clusters, whereas none of the nanowires are

observed in these open areas without a covered cluster, suggesting that it is possible that the mechanism to trigger nanowire growth is not the vapor-solid model. It is worthy to note that these nanowires have uniform diameters in the range of 17 to 27 nm, without being affected by oxygen plasma treatment and regardless of the size of clusters. The clean surface of a crystal silicon substrate is important for epitaxial growth of silicon nanowires and pre-treatments are applied to get oxide-free surfaces [38-41]. The agglomeration of surface nickel oxides exposes the Ni surface to these Si-rich droplets and triggers the growth of nanowires of different lengths. Longer nanowires are located at relatively small clusters, while short and thick nanowhiskers are observed in relatively large clusters. In addition, there are only sprouts or no nanowires at large clusters. This phenomenon of cluster-size-dependent growth velocity is believed to be associated with the localized temperature at the liquid-solid interface because the consumption of energy for NiSi-formation leads to a lower temperature at a larger cluster and retards the formation of NiSi-NW.

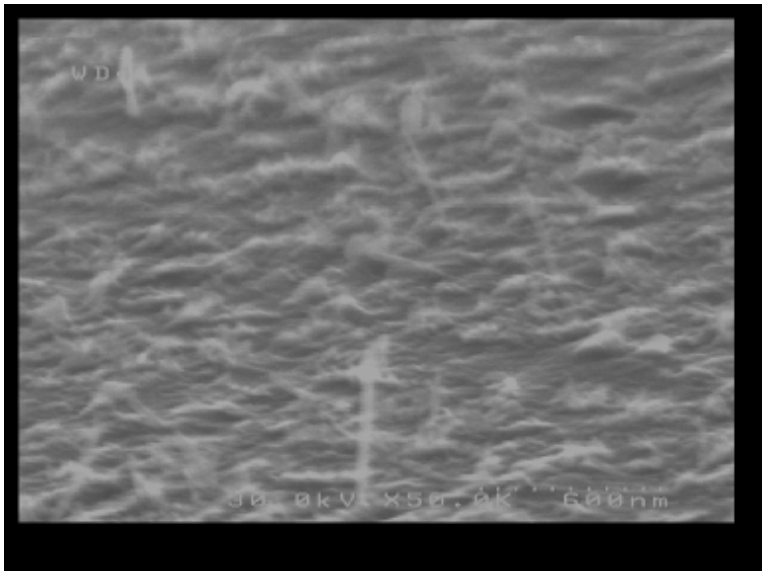


Fig. 2.8: SEM image after synthesis process with SiH_4 and H_2 gases on nickel film deposited on $TaN/SiO_2/Si$ substrate after receiving oxygen plasma treatment.

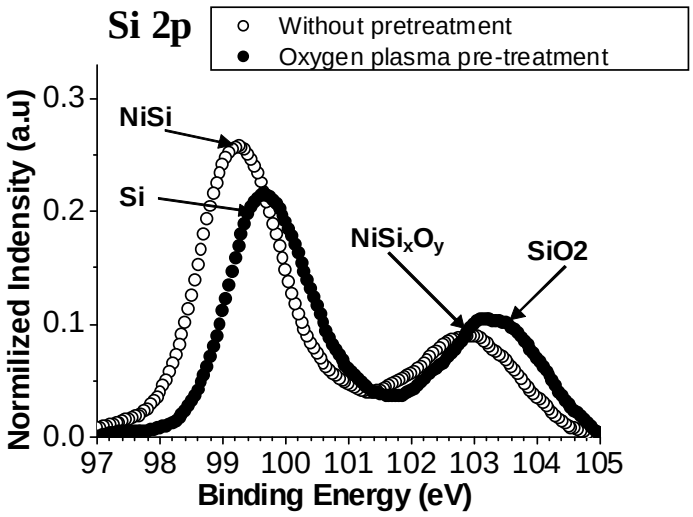


Fig. 2.9: XPS result of Si 2p spectra for Ni films on TaN/SiO_2/Si substrate after synthesis with SiH_4 and H_2 gases.

Figure 2.9 compares the Si 2p spectra of Ni films with and without plasma treatment after the nanowire synthesis process. The increase of Si and SiO_2 peaks indicates the absorption of silicon in the droplets was enhanced during synthesis and was further oxidized after cooling down, further supporting the prior hypothesis that agglomeration of surface nickel oxides forms the liquid droplets and triggers NiSi-NW growth inside these droplets.

2.3.2.3 NiSi Nanowire Synthesis Model

The proposed growth mechanism of NiSi-NW is depicted in **Fig. 10**. First, quasi-liquid droplets are formed after surface nickel oxides are heated and agglomerated [**Fig. 10(a)-(b)**]. SiH_4 gas provides the Si source and approaches the surfaces of nickel film; Si diffuses into these oxide droplets in a much higher degree of absorption, and therefore forms Ni-O-Si saturation droplets [**Fig. 10(c)**]. Subsequently, saturated Si in Ni-Si-O droplets rapidly diffuses towards the liquid-solid interface

underneath these droplets, precipitates and forms NiSi at the place wherein Ni cubic structure provides initial nucleation sites, and rich silicon in the droplets together with fast nickel diffusion enables nanowires to be grown epitaxial above the silicide layer [**Fig. 10(d)**] [2,5]. Simultaneously, Si in the droplets also binds to these oxide compounds and forms Ni-Si-O compounds remaining at the root. Following this, Ni rapidly travels to the tip of the nanowire along the direction of the nanowire axis and continuously elongates the nanowire with the feeding of Si source via a vapor-solid mechanism until a point where the Ni source is used up [**Fig. 10(e)-(f)**] [1]. At the open area, SiH_4 concurrently provides the silicon source as a result of thermal decomposition and reacts with Ni to form NiSi [**Fig. 10(d)**]. This NiSi layer gradually increases the thickness with continuing Si deposition [**Fig. 10(e)**] and forms grains [**Fig. 10(f)**]. Finally, straight nanowires are synthesized and Ni-Si-O compounds surround the feet of nanowires or appear as nanowhiskers or clusters. In-situ TEM during growth is a powerful technique of obtaining detailed information of nanowire, hence further investigation is needed to provide deep understanding of NiSi-NW synthesis, such that the exact structure and chemical status of the foot of nanowire could be known.

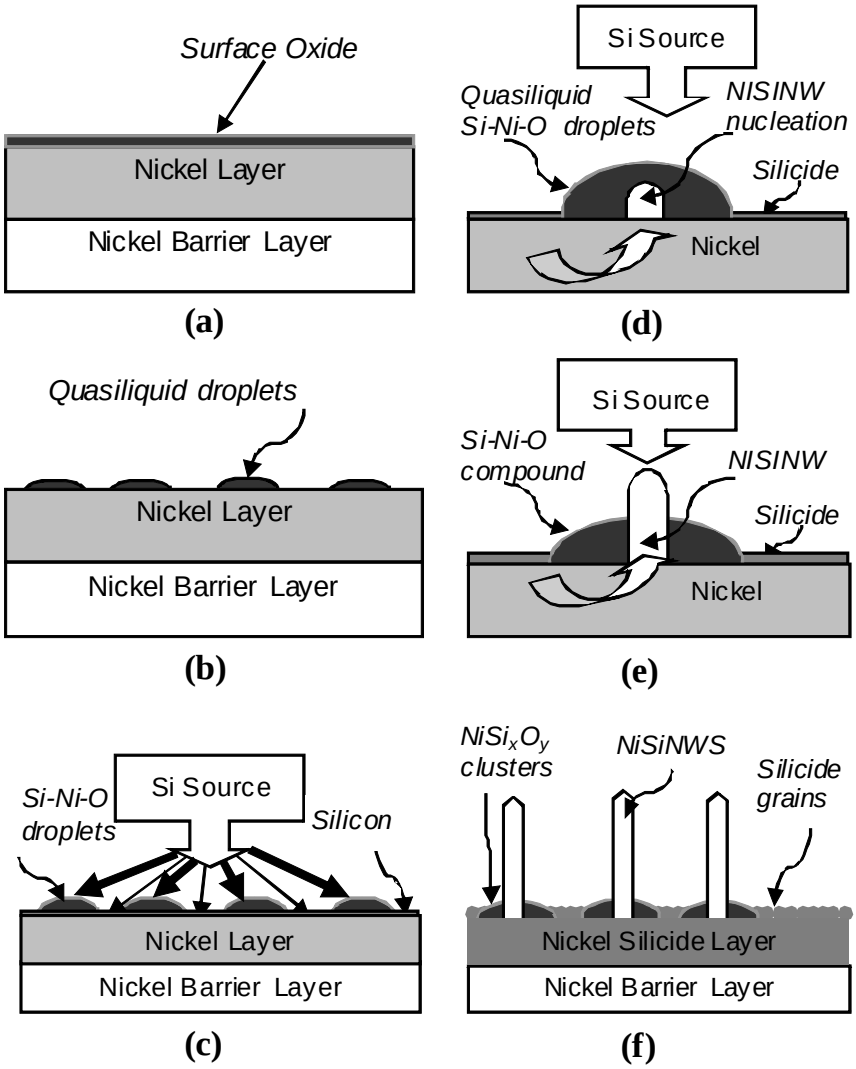


Fig. 2.10: Schematic illustrations of the NiSi nanowire growth mechanism: (a) initial status, (b) agglomeration after heating, (c) silicon incorporation, (d) triggering of NiSi nanowire growth, (e) elongation growth of NiSi nanowire, and (f) NiSi synthesized.

2.3.3 NiSi Nanowire Synthesis Characteristics

2.3.3.1 The Effect of NiSi Nanowire Synthesis Conditions

The synthesis of the nanowire has also been studied under various conditions at 550 °C. The nickel film provides the only Ni source for the synthesis and thus the thickness of film is crucial to the length of nanowire. Therefore, none of nanowires

besides small grains were obtained using nickel film with a thickness of 5 nm, and a 10-nm-thick nickel film received only sprouts and a few very short nanowires. While the partial pressure of SiH_4 gas plays an important role in determining the density of nanowire, only a few nanowires of various lengths were synthesized when the synthesis pressure was reduced down to 2 Torr. On the other hand, the replacement of H_2 gas to N_2 gas prevents the deoxidization of Ni_2O_3 to NiO and also enhances SiH_4 decomposition, contributing to the significant increase of nanowire density without any obvious change of nanowire diameters, as shown in **Fig. 2.11**.

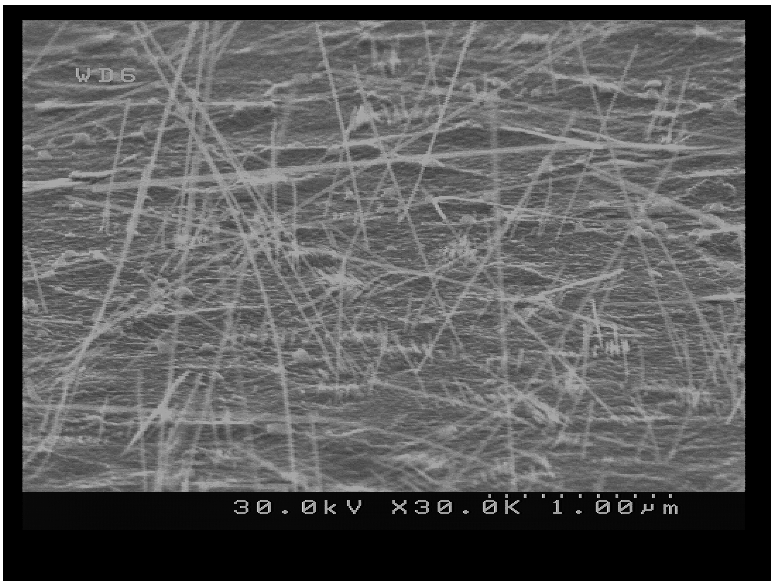
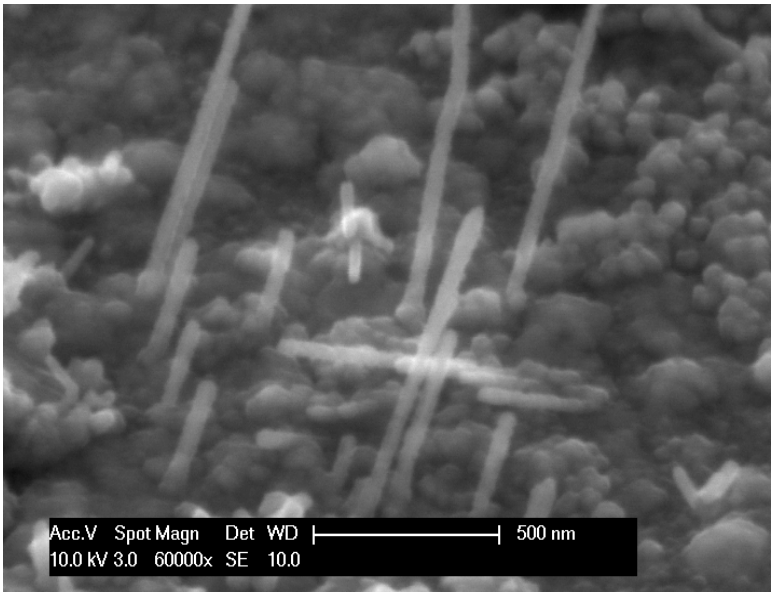
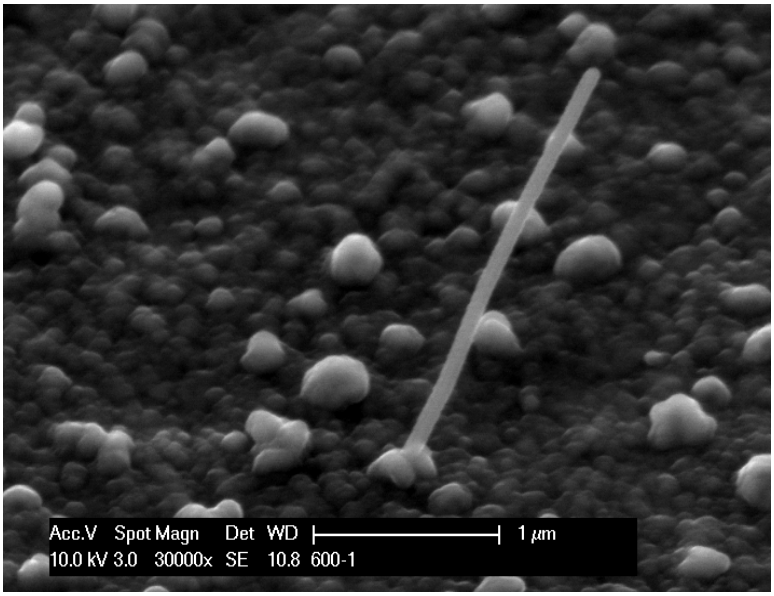


Fig. 2.11: SEM image of a 30-nm-thick Ni film on $TaN/SiO_2/Si$ substrate after synthesis process at 550 °C with SiH_4 and N_2 gases.

The synthesis has also been studied at elevated temperatures of 575 °C and 600 °C on the $Ni/TaN/SiO_2/Si$ system. As show **Fig. 2.12(a)** and **2.12(b),** higher temperatures resulted in nanowires of thicker diameters and less dense growth through larger agglomerated islands, and more sprouts breaking through islands. It is observed that these nanowires still own straight and uniform stems and spear-like tips as these of nanowires were synthesized at 550 °C, except the diameters increased as the temperature increased.



(a)



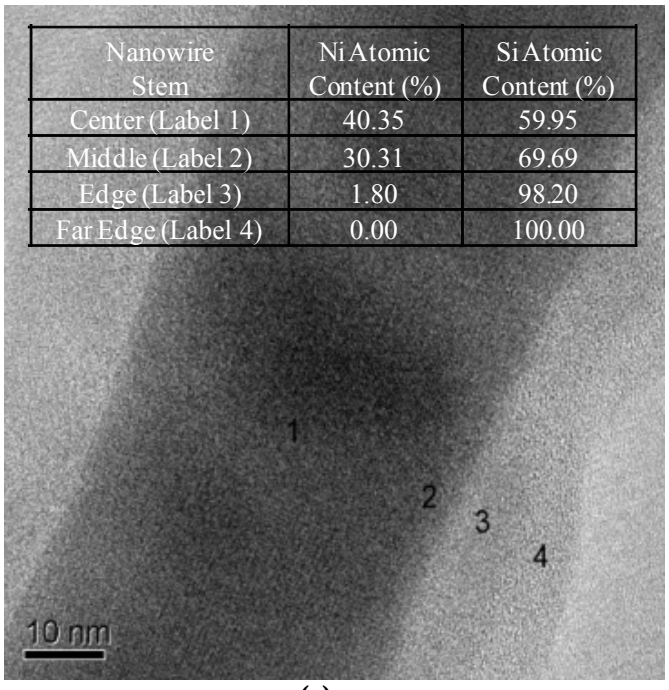
(b)

Fig. 2.12: SEM images of Ni films on $TaN/SiO_2/Si$ substrates after synthesis process with SiH_4 and N_2 gases at (a) at 575 °C, and (b) 600 °C.

2.3.3.2 Properties of NiSi Nanowires

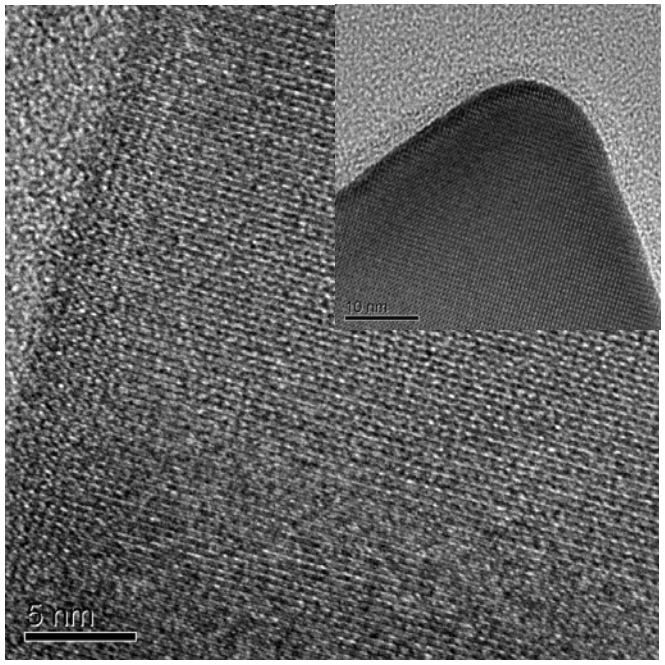
The clear single-crystalline structure of a nanowire tip and stems grown at 575 °C is displayed in **Fig. 2.13**. EDS analysis (**Fig. 2.13(a) insert**) reveals the ratio of Ni:Si

along the direction perpendicular to the nanowire stem axis decreases from 0.67:1 (center) and 0.43:1 (middle) to 0.02:1 (edge) and 0.00:1 (far edge), indicating the NiSi core is surrounded by a SiO_2 shell.



Nanowire Stem	Ni Atomic Content (%)	Si Atomic Content (%)
Center (Label 1)	40.35	59.95
Middle (Label 2)	30.31	69.69
Edge (Label 3)	1.80	98.20
Far Edge (Label 4)	0.00	100.00

(a)



(b)

Fig. 2.13: TEM results of nanowires stem grown at 575 °C with SiH_4 and N_2 gases: (a) a stem (insert: EDS result), and (b) another stem (insert: a tip).

Table 2.2 lists the lattice spacing measured for several nanowires grown at 550 °C and 575 °C. The lattice spacing of 0.57 nm along the growing axis in this work is well matched with Kim *et al*.'s observation, and the lattice spacing of 0.53 nm is measured at the direction perpendicular to the growing axis [1]. Other latter spacing are also measured, in which 0.33 nm is the lattice spacing along the growing axis, while 0.53 or 0.57 nm is the lattice spacing at a direction perpendicular to the growing axis, showing there are other orientations in NiSi-NWs. These results of lattice spacing are closely matched to the parameters (a=0.5233 nm, b=0.3258 nm, c=0.5659 nm) of a NiSi orthorhombic unit cell under normal conditions [45]. Nevertheless, there are other structural formations of NiSi, such as cubic and tetragonal structures, and another lattice spacing of 0.82 nm is reported for carbon-coated NiSi-NWs synthesized in a RF-CVD at 700 °C, implying that further study is needed in order to obtain NiSi-NWs in a single or high purity of structure and orientation [1,4].

Table 2.2: Ni-catalyzed nickel silicide nanowire properties.

Synthesis system	Temperature (°C)	Si source	Diameter (nm)	Silicide phase(s)	Sturcture	Lattice spacing (nm)	Reference
Tube furnace	420	SiH_4 gas	~ 15	NiSi, Ni_2Si, Ni_3Si_2			5
Tube furnace	500	SiH_4 gas	30-80	Ni_2Si	Orthorhombic	0.25	44
DC magnetron sputter	575	Si nanoparticle	20-100	NiSi	Orthorhombic	0.5714	1
RF-CVD	700	SiH_4 gas	20-40	NiSi		0.82	4
CVD	550	SiH_4 gas	18-28	NiSi	Orthorhombic	0.57, 0.33	This study
CVD	575	SiH_4 gas	35-55	NiSi	Orthorhombic	0.57, 0.33	This study

2.3.3.3 Diameters of NiSi Nanowires

It is well known that the diameter of semiconductor nanowires via VLS growth is determined by the size of a catalyst-nanoparticle. Therefore, the size of a Si-Ni alloy liquid droplet controls the diameter of Si nanowire via Ni-catalyzed VLS growth [10]. On the other hand, Ni-catalyzed NiSi-NWs exhibit relatively consistent diameters at a fixed synthesis temperature regardless of the sizes of particular clusters. As the synthesis temperature increases, the diameters of nanowires appear to increase from 18-28 nm (550 °C) to 35-55 nm (575 °C) and 93 nm (600 °C), respectively. The diameters of NiSi-NWs are plotted against the reciprocal of the synthesis temperatures

in **Fig. 14**. This Arrhenius plot shows that the diameter of a NiSi-NW may be expressed as:

$$D = A \cdot \exp\left(\frac{-E_a}{kT}\right) \qquad (\mathbf{2\text{-}1})$$

where D is the diameter of a NiSi-NW, A is a constant in given conditions, k is Boltzmann constant, T is the synthesis temperature, and E_a is the NiSi-NW formation activation energy which is calculated to be ~1.72 eV.

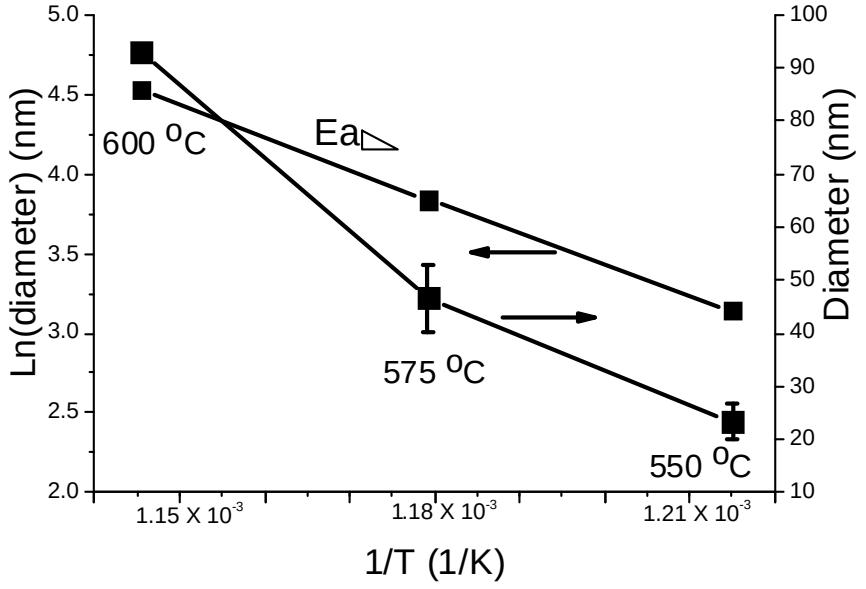


Fig. 2.14: Arrhenius plots of the diameters of NiSi nanowires against inverse of the synthesis temperatures.

This activation energy is higher than that of NiSi formation at 1.6 eV, but much lower than that of 2.9 eV for NiSi agglomeration [12, 22]. These variations suggest that the formation of NiSi-NW occurs after forming NiSi without NiSi agglomeration. Furthermore, the difference (0.12 eV) of the activation energies between NiSi-NW formation and NiSi formation is far less than that of NiSi nucleation at 0.93 eV, thus further supporting Decker *et al.*'s finding that the Ni crystal cubic structure provides the

nucleation sites of NiSi-NW initiation [5,12,22].

Corresponding to the lattice spacing of 0.356 nm of Ni cubic structure, which would be the possible minimum diameter of NiSi-NW, the minimum temperature to synthesize NiSi-NWs is plotted to be ~427 °C in a CVD chamber. However, the process chamber configuration plays an important role in the thermal or heat transport and therefore has an impact on the synthesis temperature. For example, a furnace tube is able to synthesize nickel silicide nanowires at a much lower temperature because gases are heated up when they flow to the synthesis sites, as opposed to the cool gas flow in a CVD system. Nevertheless, it is important to note that a lower temperature is associated with the other phases of nickel silicide. As listed in **Table 2.2**, Ni_2Si nanowires of diameters of 30 to 80 nm were formed at 500 °C, and the co-existence of several silicide phases were found among nanowires obtained at 370-420 °C [5,44]. Thus, the diameters of NiSi-NWs are tunable and predictable within a specific temperature window.

2.4 Conclusion

Nickel mono-silicide nanowires (NiSi-NWs) have been synthesized on electron-beam-evaporated Ni films with SiH_4/H_2 gases in a CVD chamber, and the structures of the resultant nanowires have been examined.

The role of surface nickel oxides has been investigated with the aid of oxygen plasma treatment. The presented results suggest that surface oxides provide droplets to trigger NiSi-NW growth via a VLS mechanism with the aid of nickel diffusion, followed by a metal-assisted vapor-solid mechanism to elongate the nanowires.

The diameter of NiSi-NWs is found to be dominated by the synthesis temperature with an activation energy of ~1.72 eV, hence the diameter of NiSi-NWs is tunable within the temperature window. More detailed study will benefit the integration of NiSi-NWs into device fabrication and the potential applications in field emitters and

interconnections.

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Chapter 3

Synthesis of Single-crystalline $Si_{1-x}Ge_x$ Nanowire by Au-catalyzed Chemical Vapor Deposition

3.1 Introduction

As discussed in **Chapter 1.2.3.4**, a $Si_{1-x}Ge_x$ nanowire may have favorable thermoelectric properties for various applications on nanowires. As such, single-crystalline $Si_{1-x}Ge_x$ nanowires of different diameters and chemical component ratios were required for physical measurement and characterization.

$Si_{1-x}Ge_x$ nanowires have been synthesized via Au-catalyzed vapor-liquid-solid (VLS) growth and were further integrated in metal-oxide-semiconductor field-effect transistors (MOSFET) [1-3]. It has been demonstrated that the synthesis temperature and the flow rate of GeH_4 are key factors in the synthesis of $Si_{1-x}Ge_x$ nanowires with uniform stems and without amorphous Ge covering layers. However, these nanowires have only up to 25.7 atomic % of Ge, and there are limited reports on the achievement of $Si_{1-x}Ge_x$ nanowires of a higher concentration of Ge [1-3]. Furthermore, the diameter-dependent growth velocity and diameter-selective synthesis of Si and other semiconductor nanowires via the VLS method have been well studied, whereas there are few studies of diameter effects on the synthesis of $Si_{1-x}Ge_x$ nanowires, in particular, the atomic ratio of compounds [4-12].

In this work, various synthesis conditions were applied to synthesize single-crystalline $Si_{1-x}Ge_x$ nanowires via the Au-catalyzed VLS growth technique. Various nanowires with uniform and long stems of different diameters were obtained. These nanowires have a high concentration of Ge, and it was found that the ratio of Ge to Si is diameter-dependent and varies along the stem of a nanowire. It was also

found that there is an Au compound at more than one atomic % detected in some of the upper parts of $Si_{1-x}Ge_x$ nanowire stems, suggesting the thermal conductivity of nanowire plays an important role in the synthesis of nanowires. The preliminary measurement of the thermoelectric properties and the challenges of measurement are also presented.

3.2 Experiments

As illustrated in **Fig. 3.1**, p-type Si (100) wafers were first cleaned using diluted hydrofluoric acid (DHF), before proceeding to thermally grow 400-nm-thick SiO_2, followed by the dispersion of Au nano-particles of the nominal size of 20 nm on the SiO_2 layer. In order to make Au nano-particles adhere on the oxide surface, Poly-L-Lysine solution (Ted Pella) was coated on oxidized silicon for 1 minute before being removal using acetone solution, then Au colloid (BB International) was dispersed on these charged surfaces for 5 minutes, lastly followed by DI water cleaning and drying using N_2. Following this, nanowires were synthesized in a CVD chamber at various temperatures in the range of 490 to 550 °C with a flow rate of GeH_4-Ar gas in the range of 20 to 160 sccm, in which GeH_4 is diluted by Ar at the ratio of 1:9. Each synthesis consists of 3 consecutive steps without varying the synthesis temperature during the process: thermal heating in vacuum for 3 minutes; treatment in the flow of 1000 sccm H_2 for 1 minute; and growth with GeH_4-Ar / 200 sccm SiH_4 / 200 sccm H_2 gases at a total pressure of 25 Torr for 10 minutes.

A 10-nm-thick Au film deposited on DHF-cleaned Si (100) wafers and different synthesis pressure was also applied in this study. Scanning electron microscopy (SEM), high resolution transmission electron microscope (HRTEM), energy-dispersive X-ray spectroscopy (EDS), and selected area electron diffraction (SEAD) techniques were used to characterize the physical structures and chemical properties of the produced nanowires.

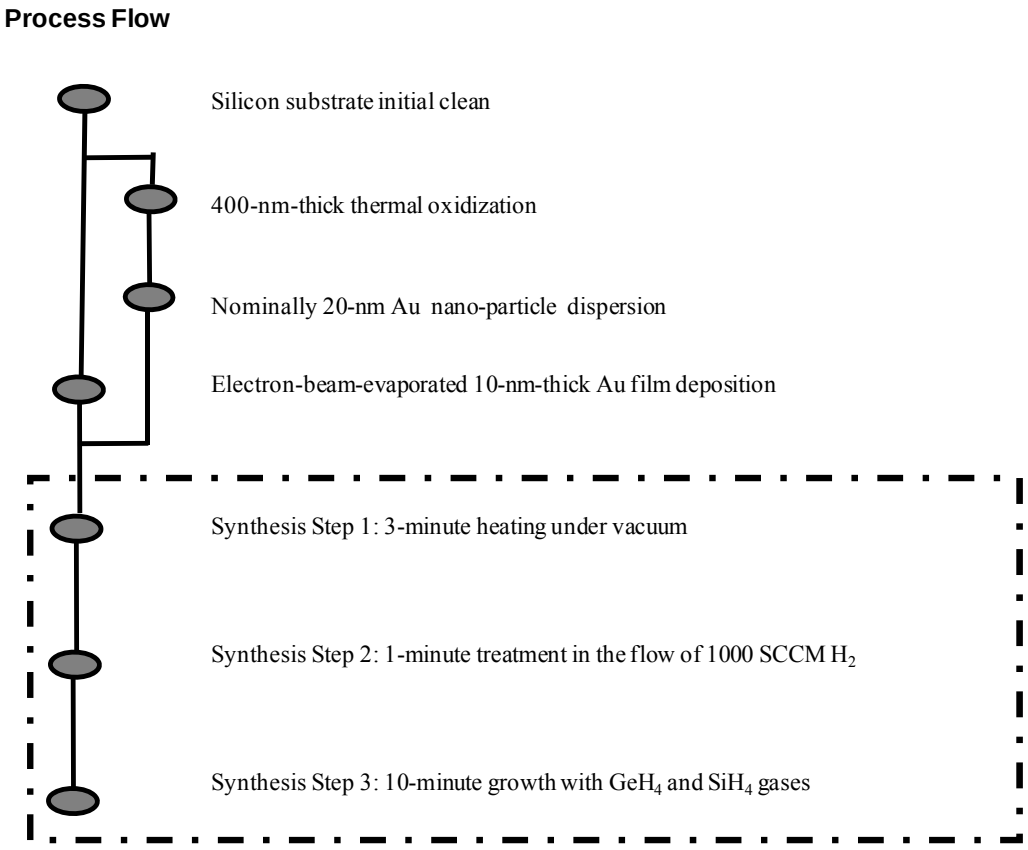


Fig. 3.1: The process flow for $Si_{1-x}Ge_x$ synthesis: the 3 steps of synthesis were sequentially executed in a thermal-heated chemical-vapor-deposition (CVD) chamber, in which GeH_4-Ar/200 sccm SiH_4/200 sccm H_2 gases provided silicon and germanium source for the Au-catalyzed VLS growth.

In order to characterize the thermoelectric properties, Si nanowires were also prepared using the same synthesis method except for the presence of GeH_4/Ar gases, and testing devices were fabricated on Si_3N_4 membranes. A four-pin-probe measurement and a 3ω method were used to obtain preliminary results of resistance and thermal conductance, respectively.

3.3 Results and Discussion

3.3.1 Synthesis of $Si_{1-x}Ge_x$ Nanowires

3.3.1.1 Synthesis on Au Nano-particle/SiO_2/Si Substrate

Au nano-particles were employed as the catalyst to synthesize long and straight $Si_{1-x}Ge_x$ nanowires of small diameters. As shown in **Fig. 3.2(a)-(c)**, the increase of GeH_4 flow from 2 sccm to 16 sccm leads to less bending phenomena of the nanowires and an overall increase in the diameters of the nanowires, producing nanowires with more straight and uniform stems. However, nanowires of small diameters are desirable; hence a decreased synthesis temperature was applied. **Figure 3.2(c)-(e)** shows that the diameters of nanowires are significantly reduced as the temperature decreases from 550 °C to 490 °C and the smallest distribution of diameters is also obtained at 490 °C.

The high density of these nanowires grown in disorderly directions generates nanowires in bundles, and even the Au-alloyed tip of a nanowire may encounter other nanowires during growth. Hence, several unwanted symptoms are observed as circled in **Fig. 3.2(a)-(e)**, such as the sudden termination of growth, the abruptly bent stems, the crosslink of nanowires, and the sub-branches. These will degrade the quality of the nanowires, including the structure defects and the Au-contaminated nanowire surface.

In the VLS growth, the combination of higher temperature and lower pressure is critical to synthesize a kink-free nanowire due to the instabilities of the liquid-solid interface at the catalyst droplet sitting at tip of nanowire. However, an elevated temperature is associated with an increase in diameter [11-14]. On the other hand, the decrease in pressure within the high partial pressure range has less impact on the diameters of nanowires, despite a decreased growth velocity and lower nanowire density [5,11,15]. After reducing the synthesis pressure to 8 Torr, as can be seen in **Fig. 3.2(f)**, the density of nanowires was dramatically reduced and much shorter length of nanowires was obtained, i.e. from nano-dot to 1.2 μm in the diameter of 25 to 41 nm. The nanowires have straight and uniform stems, and the lengths can be extended by increasing the synthesis time. However, dense grown worm-like structures have larger Au droplets at their tips and have randomly grown among the surface of the substrate. These worm-like structures are of irregular shapes and of larger diameters, in

particular, they are often of an amorphous structure. Hence, they are unwanted for our study and thus, the migration and coarsening of catalyst droplets should be restrained during the synthesis process.

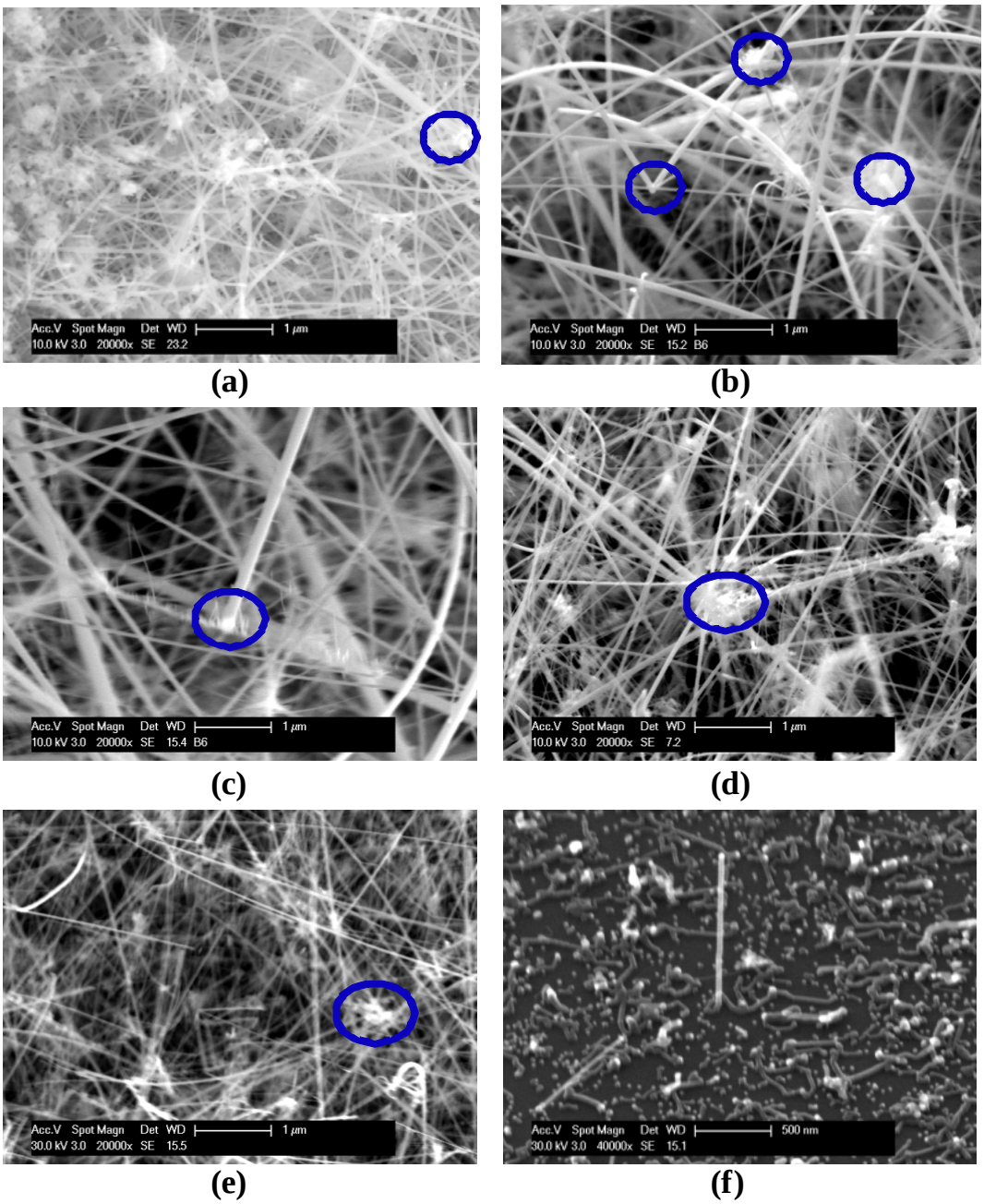


Fig. 3.2: SEM images of nanowires grown on 20-nm Au nanoparticles/SiO_2/Si substrates at 25 Torr with (a) 2 sccm GeH_4 at 550 °C, (b) 8 sccm GeH_4 at 550 °C, (c) 16 sccm GeH_4 at 550 °C, (d) 16 sccm GeH_4 at 520 °C, (e) 16 sccm GeH_4 at 490 °C, and (f) at 8 Torr with 16 sccm GeH_4 at 490 °C.

3.3.1.2 Synthesis on an Au Film/Si Substrate

It has been documented that an Au-Si alloy is able to migrate among a Si surface and thus coarsens the catalyst droplet [16]. Furthermore, Au has a very weak affinity for oxygen and a much larger contact angle with a SiO_2 surface than that on a Si substrate. Hence an Au-Si alloy tends to form larger droplets on the SiO_2 surface [17-18]. As the eutectic point of Ge-Au (361 °C) is slightly lower than that of Si-Au alloy (363 °C), the synthesis of $Si_{1-x}Ge_x$ nanowires on a Si substrate, instead of a SiO_2/Si substrate, may result in less migration phenomenon of catalyst alloy and fewer worn-like nanowires [19].

Moreover, the studies of Si nanowire synthesis in plasma enhanced chemical vapor deposition (PECVD) chambers, which technique has the unique feature of being able to synthesize nanowires at a temperature lower than 400 °C, show that the obtained nanowires on a Si substrate are more disorderly when using the Au nanoparticle catalyst, than those seen when using a thin Au film. It has also been demonstrated that the nanowires obtained on a SiO_2/Si substrate are of short lengths and of cone shapes [20-21]. These findings further suggest that it is important for the Au catalyst to anchor on the Si substrate in order to obtain orderly $Si_{1-x}Ge_x$ nanowires in small diameters.

Compared to Au nanoparticles, a thin Au film has a much large contacting area to Si substrate and adheres well to it. When such a system is heated to a temperature around the eutectic point, the Au-Si alloy is formed on the Si (100) surface and further agglomerate to form Au-Si alloy droplets at a smaller contact angle with the Si substrate [22]. Furthermore, there is little lattice mismatch between Si and Ge, and the superlattice structure of a nanowire is more capable of tolerating lattice mismatches among components, suggesting that the $Si_{1-x}Ge_x$ nanowires are able to grow on the Au-Si droplets [23-24]. Hence, a 10-nm-thick Au catalyst film was deposited on a DHF-cleaned Si substrate in order to form uniform droplets of Au-Si alloy adhering well on the Si substrate before the growth of $Si_{1-x}Ge_x$ nanowires.

Figure 3.3(a) shows the surface of the Au film/Si substrate after synthesis. The catalyst nano-dots are evenly dispersed among the surface, and the bottom part of them anchors at the substrate (**Fig. 3.3(a) insert**), indicating the alloy droplets have partially penetrated into the Si substrate and thus prevents the further migration of alloy among the substrate surface.

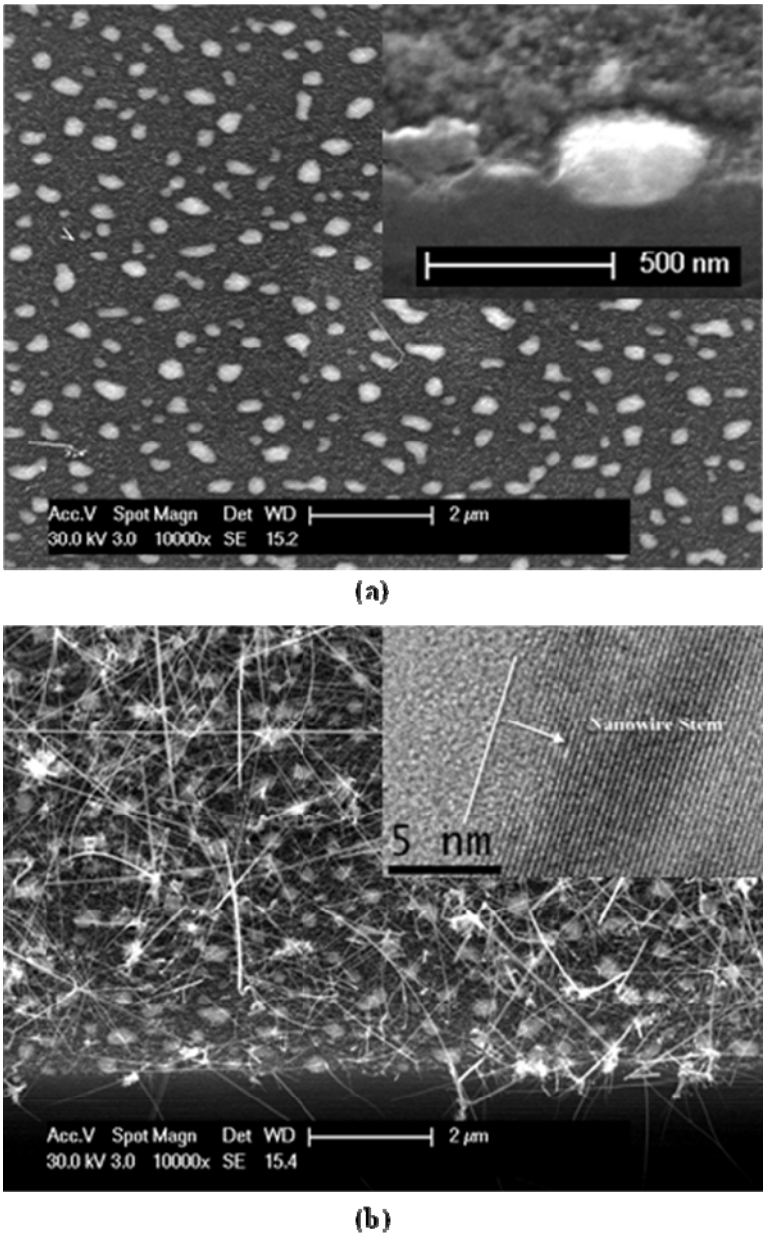


Fig. 3.3: SEM images of nanowires grown on 10-nm-thick Au film/Si substrates at 490 °C with 16 sccm GeH_4 at (a) 8 Torr (insert: cross section of substrate), and (b) 25 Torr (insert: TEM image of one stem).

To some degree, these nano-dots have various sizes and hence, offer the advantage of obtaining nanowires of different diameters in a single process. As shown in **Fig. 3.3(b)**, a higher synthesis pressure of 25 Torr was applied to increase the density and lengths of nanowires. These nanowires in the length of up to ~15 μm have the majority of diameters in the range of 13 to 58 nm, and the single-crystalline structure [**Fig. 3.3(b) insert**] is present for these nanowires examined. As such, these properties have been further studied.

3.3.2 Properties of $Si_{1-x}Ge_x$ Nanowires

3.3.2.1 Component and Structure Properties of Straight $Si_{1-x}Ge_x$ Nanowires

Figure 3.4 shows a straight nanowire with a semispherical cap at the tip and an amorphous shell shielding the core of the stem. The EDS result of component analysis for this nanowire is listed in **Table 3.1**. This amorphous shell layer is due to the surface oxidation of Si and Ge when the nanowire was exposed to air, with this phenomenon further verified by another EDS analysis in our study, which shows that the portion of a nanowire suspended across a opened window in the TEM grid has only the elements Si, Ge, and O within the EDS detection limit. This oxide layer can cause high contact resistance. As such, the DHF cleaning process is widely applied to remove these surface oxides during the fabrication of nanowire devices.

This shell layer has a uniform thickness of ~3 nm along the stem. However, it appears to gradually thicken near the tip. The thickness further increases from 4.4 nm at the bottom part of the tip to the maximum of 14.7 nm at the top part of the tip. This indicates that Si and Ge have been released from the Au-alloyed droplet at the tip of nanowire after cooling. Furthermore, an EDS result shows the tip of the nanowire has an atomic ratio of Si:Ge at 0.64:1 with the coexistence of Au, indicating more Ge has dissolved in the Au-Si-Ge alloy droplet during nanowire growth. This is in good agreement with the trend that much higher Ge atomic % in Au-Ge alloy than that of Si in Au-Si alloy at a same temperature above their eutectic points [19]. The binary phase

diagrams of bulk alloys also shows that the mixture of Au-Si alloy and Si-Ge alloy at 1:1 atomic ratio has an atomic ratio of Si:Ge at 0.64:1 at the temperature of ~420 °C, suggesting the liquid Au-Si-Ge alloy was possibly at a temperature below 420 °C during the nanowire growth at a nominal temperature of 490 °C at the synthesis tool because of small size effect [14,17,19,25].

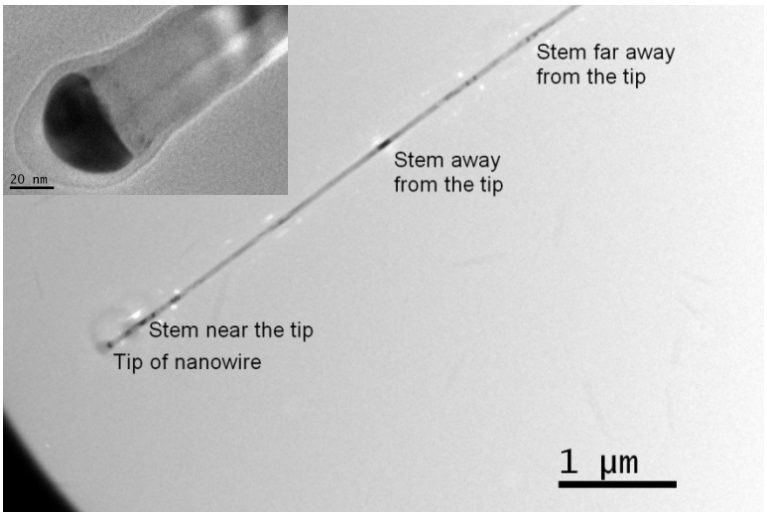


Fig. 3.4: TEM image of a straight nanowire (insert: the tip of nanowire).

Table 3.1: Diameter measurement and component result of a straight nanowire.

Location	Distance to tip (μm)	Diameter (nm)	Au Atomic %	Si Atomic %	Ge Atomic %
Stem far away from the tip	4.5	61.8	0.00	30.00	70.00
Stem away from the tip	3.0	57.1	0.00	32.31	67.69
Stem near the tip	0.5	48.5	0.00	33.06	66.94
Tip of nanowire	0.0	65.9	54.68	17.69	27.63

It was observed that the Ge atomic % decreases and Si atomic % increases along the stem from a position ~4.5 μm away from the tip of nanowire to another position ~0.5 μm near the tip [**Fig. 3.4**], and the diameter of the stem gradually decreases from 61.8 nm to 48.5 nm. This phenomenon also agrees satisfactorily with the trend derived from the binary phase diagrams of bulk Au-Si and Au-Ge alloys, which shows that the ratio of Si to Ge tends to increase as the temperature is reduced, and the diameter of

Au-Si-Ge catalyst droplet is correspondingly reduced because less Si and Ge are dissolved into this liquid Au-Si-Ge alloy. This suggests the Au-Si-Ge catalyst droplet keeps decreasing its temperature as the nanowire grows, generating the nanowire with a slightly tapered profile.

The sidewall deposition of Si and Ge is another possible reason for tapered profile, despite H_2 gas can passivate the sidewall of $Si_{1-x}Ge_x$ nanowires. However, the rate of diameter reduction of 3.13 nm per μm length from the position of stem far away from the tip to away from the tip is less than that of 3.44 nm per μm length from the positions of stem away from the tip to near the tip [**Fig. 3.4**]. This higher reduction rate of the diameter at the upper portion of stem indicates sidewall deposition is not the only reason for a tapered profile and further supports the hypothesis that the temperature of the Au-Si-Ge catalyst droplet reduces as the nanowire grows.

During the $Si_{1-x}Ge_x$ nanowire growth, heat is transferred along the stem from the substrate to the tip of a nanowire, and the thermal effect of a stem on the temperature at the catalyst tip of the nanowire can be described as follows. The thermal resistance (R_{th}) can be defined as **Equation 3-1**:

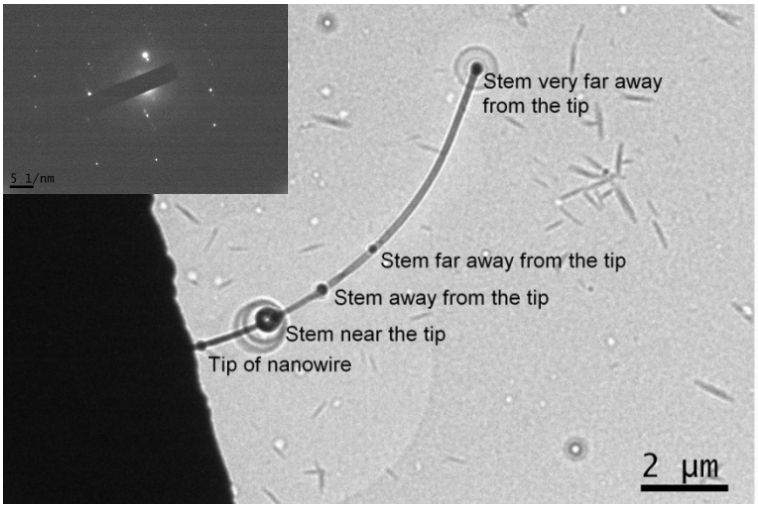
$$R_{th} = \frac{L}{\beta A} \qquad \textbf{(3-1)}$$

where L is the length of nanowire stem, A is the cross-sectional area, and β is the thermal conductivity [26]. Hence, a longer and smaller nanowire has larger thermal resistance and constrains heat energy thermally transferring to the tip of the nanowire, resulting in a reduced temperature at the catalytic alloy droplet. In addition, VLS-grown Si nanowires and Si/SiGe superlattice nanowires have a substantial reduction of thermal conductivity with a diameter-dependent effect, and it is expected that $Si_{1-x}Ge_x$ nanowires have more of a reduction in thermal conductivity than the Si nanowire, as discussed in **Chapter 1** [26-28]. However, direct temperature measurement at the catalyst tip of a nanowire to date remains a challenging problem,

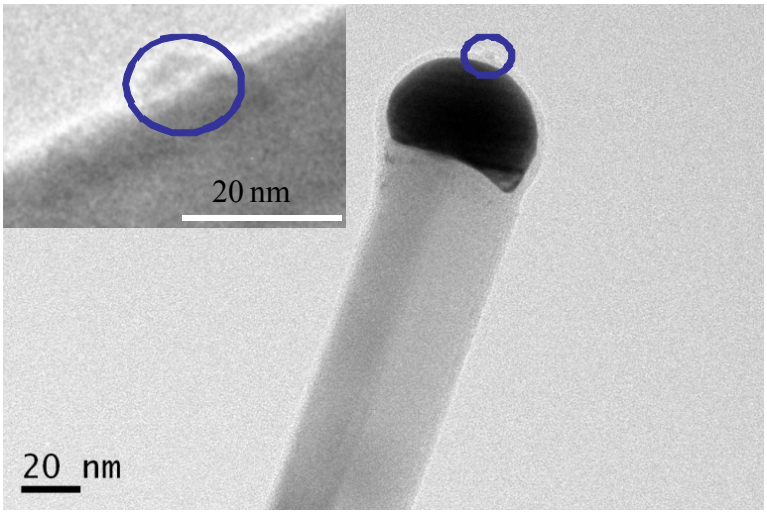
thus future study on the thermal conductivity of these $Si_{1-x}Ge_x$ nanowires is required.

3.3.2.2 Component and Structure Properties of Bent $Si_{1-x}Ge_x$ Nanowires

A few bent nanowires are also present among the straight nanowires [**Fig. 3.3(b)**]. **Figure 3.5** and **Table 3.2** present the results of a bent nanowire examined in the TEM. The lower portion of stem remains straight for ~2 μm [**Fig. 3.5(a)**]; while it starts to bend near the medial portion and the curve shape of stem extends up to the tip of nanowire without any sudden changes of growth direction or diameter. This bent structure of the nanowire may imply stacking defects in the stem [14,29].



(a)



(b)

Fig. 3.5: TEM image of (a) a bent nanowire (insert: the SEAD image of the stem at the position near the tip), and (b) the tip of the nanowire (insert: a nano-particle at the stem).

Table 3.2: Diameter measurement and component result of a bent nanowire.

Location	Distance to tip (μm)	Diameter (nm)	Au Atomic %	Si Atomic %	Ge Atomic %
Stem very far away from the tip	9.5	56.5	0.00	31.42	68.58
Stem far away from the tip	4.5	54.8	0.00	32.47	67.53
Stem away from the tip	3.1	51.3	1.01	35.43	63.56
Stem near the tip	1.7	48.4	1.04	33.53	65.51
Tip of nanowire	0.0	59.8	52.12	9.53	38.36

The TEM and EDS analysis resulted given in **Table 3.2** show that this nanowire has a similar trend of a tapered profile and increase in Si:Ge atomic ratio along the nanowire growth axis compared to these of the straight nanowire (**Table 3.1**), while the diameter at the upper portion of the stem shrinks at a much faster rate than that at lower portion, where a lower Ge atomic % and higher Si atomic % are found. Furthermore, Au was detected at a concentration of more than 1 atomic % at the position of the stem near the tip for ~3 μm, with a worsening at a position closer to the tip and the co-existence of a sudden increase of Ge atomic %. SEAD result [**Fig. 3.5(a) insert)**] confirms that the Au-contaminated stem still has crystalline structure, while irregular-shaped nano-particles [**Fig. 3.5(b) insert)**] are present at the surface of the stem.

It was also observed that there is a greater gap of the Si:Ge atomic ratio between the stem (0.51:1) and the catalyst tip (0.25:1). Unlike the symmetric catalyst tip existing at the top of the straight nanowire, **Fig. 3.5(b)** shows that part of the lower portion of the catalyst tip extends and emerges into the stem surface, with a nano-particle present at the top of the catalyst tip. Whereas there is no branching nanowire observed [**Fig. 3.3(b)**], which is associated with the migration of a molten catalyst alloy along the surface of each stem [16,30]. These indicate the catalyst alloy droplet was unable to remain high quality during the whole growth process and the molten alloy breaks into nano-particles after attaching on the stem as the nanowire grows. This results in the eventual consumption of the Au catalyst, and is also the possible reason for a widely observed phenomenon as the catalyst droplets rapidly to reduce their size at the upper portion of the nanowire [14,16,31].

Two reasons can be attributed to these findings. Firstly, the efficiency of heat transfer to the catalyst droplet via a nanowire stem appears to reduce because of increasing thermal resistivity as the length of the nanowire elongates, and such a trend has been further enhanced due to the reduction of the diameter of the stem. Secondly, the gases at relatively lower temperature diffuse into the alloy droplet at the gas-liquid

interface and decrease the temperature of the outer portion of the alloy droplet. Thus, some part of the alloy near the droplet surface may change phases from pure liquid to a mixture of liquid-solid nano-particles, and some of these particles may attach to the growing segment of the stem right below the alloy droplet and further appear as nano-particles on the surface of the stem. This explanation may also be relevant to several VLS synthesis characteristics of Si nanowires, including that the growth velocity tends to saturate as the nanowire grows and the straight nanowires are able to be generated in conditions of a higher temperature and lower silane particle pressure. It could also be one of important factors observed in other synthesis phenomena of Si nanowires, such as that as an elevated temperature increases nanowire growth velocity with a diameter-dependent activation energy, a larger size of catalyst can result in a faster growth velocity of nanowire [4-5,7-9,11,14].

3.3.2.3 Diameter Effect on the Component Composition of Nanowires

It has been observed that the concentration of Au has been detected as 0.00 atomic % within the EDS detection limit for stems in the straight nanowires or the straight portions of bent nanowires. More interestingly, these stems in the diameter range of ~40 nm and above have considerably more consistent Si:Ge ratios as shown in **Fig. 3.6**. However, the Si atomic % significantly increases for a stem of a diameter of ~28 nm and has even a much higher concentration than Ge for a stem of a diameter of ~20 nm. This diameter-dependent effect on the Si and Ge component ratio may suggest that the thermal conductivity reduction is even more effective for nanowires of a diameter less than 30 nm.

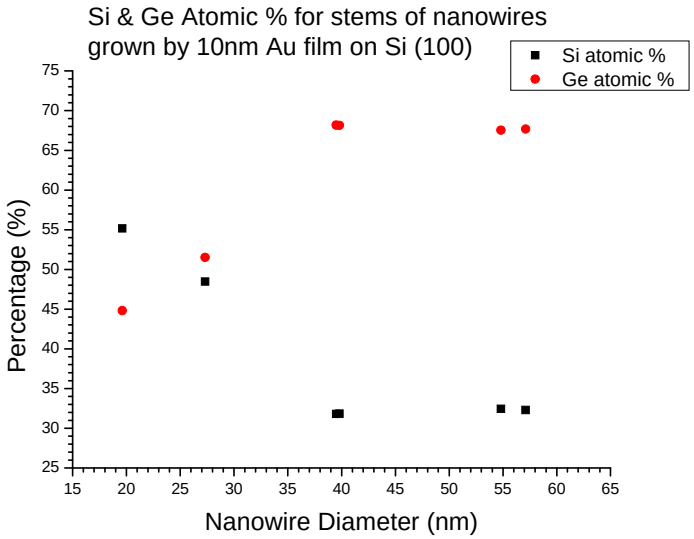


Fig. 3.6: Si and Ge atomic percentage plotted against the diameters of straight nanowire stems.

3.3.2.4 Thermoelectric Properties Characterization

The electric resistivity of one bent $Si_{1-x}Ge_x$ nanowire of a diameter of ~60 nm was tested by the 4-point-probe method, showing that the resistivity (4.0 Ω.cm) is more than one order of magnitude lower than that of bulk Ge (50 Ω.cm). This reflects that the Au contamination reduces the electric resistivity of $Si_{1-x}Ge_x$ nanowires.

Au-catalyzed Si nanowires are reported as having a lower electric resistivity after post-synthesis thermal annealing because of a much larger solid solubility of gold in silicon [32-33]. These heavy Au atoms in nanowires may have an influence on phonon scattering, thus Au doping could be a positive factor when considering the thermoelectric properties of $Si_{1-x}Ge_x$ nanowires. In addition, Au nanoparticles deposited on as-grown Si nanowire can form Au and Au silicide layers on the surface of nanowire by electron beam annealing [34]. These kinds of nanoparticles are also observed on some surfaces of $Si_{1-x}Ge_x$ nanowires in this study, and may influence thermal conductivity. As such, the measurement of thermoelectric characteristics for these $Si_{1-x}Ge_x$ nanowires is required. However, as the 3ω method was unsuccessful in obtaining any thermal conductance features of these $Si_{1-x}Ge_x$ nanowires due to high

resistance.

For the comparison purposes, a Si nanowire test structure was fabricated as illustrated in **Fig. 3.7**. A Si nanowire was transferred to a Si_3N_4 membrane with some windows in the width of μm opened by focus ion beam (FIB), and crossed over the widow with pre-fabricated Pt contacts at the both sides. In order to ensure good contacts, top contacts of Cr/Au were further made with the aid of electron beam lithography (EBL). The resistivity of ~27.5 Ω.cm was measured. However, the high resistance of the order of MΩ was too large to measure its thermal conductance by the 3ω method.

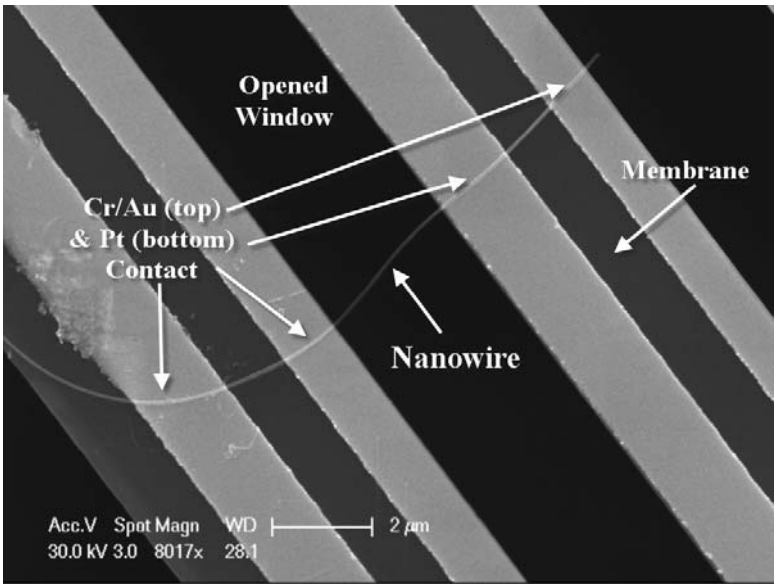


Fig. 3.7: A test device for the thermoelectric properties characterization: a Si nanowire was suspended across an opened window in a Si_3N_4 membrane and 4-pin contacts were fabricated for probes.

Review of successful measurements in the literature of thermoelectric properties of Si nanowires shows that Pt transducer pads are popularly applied in the micro-test devices. The Pt transducers are located at the both ends of a nanowire and function as both Joule heaters and resistance thermometers [26-28,35-36]. Hence, future works on the fabrication and calibration of such Pt pads will provide a fundamental test method and should be implemented as a priority for the further characterization of these

$Si_{1-x}Ge_x$ nanowires.

3.4 Conclusion

Long and straight $Si_{1-x}Ge_x$ nanowires in high Ge atomic % have been synthesized via Au-catalyzed VLS growth. The effect of temperature at the catalyst droplet for the synthesis of $Si_{1-x}Ge_x$ nanowires and the influence of a stem for the heat transfer have been discussed.

The results presented show that the concentration of Ge decreases as a nanowire grows and there is no Au detected by EDS in the straight portions of the stems. It has also been found that the concentration of Ge is diameter-dependent and a significant increase of Si atomic % occurs for these nanowires for diameters less than 30 nm. However, limited measurement results of the thermoelectric properties of these $Si_{1-x}Ge_x$ nanowires have been obtained, hence future characterizations are necessary to extend the understanding and benefit of their possible application in thermoelectric devices.

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Chapter 4

Conclusions and Future Work

4.1 Conclusions

One-dimensional nanowires exhibit many novel properties useful in nanoscale devices and applications. As such, the development of techniques for controllable synthesis of nanowires is a research priority. In this thesis, nickel mono-silicide (NiSi) nanowires and $Si_{1-x}Ge_x$ nanowires have been synthesized via a bottom-up approach in a CVD chamber. The synthesis characteristics have been investigated and studied. The nanowires produced have been examined and found to have single-crystalline structures.

The growth mechanism of NiSi nanowires has been investigated. The surface nickel oxides present on the nickel film agglomerate and form nano-droplets after heating. This triggers NiSi nanowire growth inside the droplets via the vapor-liquid-solid (VLS) mechanism, with the aid of nickel diffusion towards the droplets. Following this, the nanowire elongates axial growth via a metal-assisted vapor-solid (VS) mechanism. It has also been found that synthesis temperature is the dominant factor controlling the diameters of the NiSi nanowires, with an activation energy of ~1.72 eV. As a result, this provides a predictable process window of tuning the diameters of NiSi nanowires.

Long and uniform $Si_{1-x}Ge_x$ nanowires of various diameters and in different component ratios were also prepared via Au-catalyzed VLS growth for the study of their thermoelectric properties. A high concentration of Ge is contained in the stems of these nanowires and gradually decreases towards the tips as the nanowires grow. It has also been found that the Si:Ge ratio is diameter-dependent and the Si

concentration rapidly increases as the diameters of nanowires reduce to a range of < 30 nm. Furthermore, the Au compound is present in a concentration greater than one atomic percentage in the upper part of a few of $Si_{1-x}Ge_x$ nanowire stems, while no Au was detected within the EDS limit on the straight stems. These observations indicate that the thermal transportation along the nanowire stems influences the nanowire synthesis characteristics.

4.2 Further Work and Recommendations

This work has identified several areas which require further study and may present opportunities for new applications.

First, the synthesis of high quality nanowires in large amounts and in a well-aligned structure is the fundamental work. This outcome still remains a challenge for commercial applications. In particular for the bottom-up approach, the preparation of a high quality catalyst on a crystalline substrate is a crucial step. The further refinement and optimization of synthesis conditions will contribute to this process.

Next, the technique used to precisely manipulate the transfer and disposition nanowires to a prepared device will significantly benefit the study of the properties of nanowires and the fabrication of functioning devices. To date, the integration of bottom-up nanowires into devices lacks precise control of synthesis and alignment. In this way, the mechanical, thermoelectric and other properties of nanowires could be more effectively studied and investigated.

Furthermore, a high-aspect-ratio (length/diameter) nanowire with a core/shell diode architecture possesses a unique advantage. The longer axial direction provides sufficient thickness and a large surface area to obtain optical abortion, while the small diameter in the radial direction provides short carrier collection length [1-6]. The small radial distance is comparable to the minority carrier diffusion length and therefore it may be able to enhance the collection efficiency of photo-generated

carriers and diminish the impact of poor quality materials. In addition, $Si_{1-x}Ge_x$ nanowires have a lower band gap energy than that of the Si nanowire and it is tunable, hence future work on a well-aligned $Si_{1-x}Ge_x$ nanowires array will benefit the application of a nanowire solar cell.

Finally, Schottky photodiodes in a thin film structure of NiSi and microcrystalline Si have been recently demonstrated [7]. It is of interest to study the possible use of NiSi nanowires as the back contact of a thin solar cell, or even in the NiSi-semiconductor in core/shell structure.

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