Thermal Processing in Lithography: Equipment Design, Control and Metrology

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Summary

Lithography is the key technology driver in semiconductor manufacturing. In lithography, the most important variable to be controlled is the critical dimension (CD) uniformity. As transistor dimension continues to scale down, lithography process equipment and materials are stretched towards their limits, thus making the process very sensitive to even small perturbations of process conditions. Advanced control, process/equipment modeling and metrology are widely believed to be the enabling technology needed to enhance CD uniformity in lithography. In this thesis, the application of advanced process control (APC) techniques, new equipment design and sensing technology for the processes in the lithography sequence are investigated to meet the stringent requirement of CD uniformity control.

As the final CD value is very sensitive to the wafer temperature during the thermal processing steps in lithography, it is important to control the wafer spatial temperature uniformity for enhancing the CD uniformity. Based on the detailed thermal model of baking process and the real-time measurement of bake-plate temperature, an in-situ approach is developed to estimate and control the wafer temperature. Using the proposed approach, the wafer spatial temperature uni-

formity during the entire thermal cycle can be improved more than 80% when compared to the existing methods.

Although the wafer temperature uniformity was successfully improved by the proposed advanced control technique, the performance gain is ultimately limited by the inherent drawbacks of the conventional hot plate. To overcome this limitation, a new programmable integrated bake/chill thermal processing module is designed and implemented. By employing a set of thermoelectric devices (TEDs), resistance temperature detectors (RTDs) and model-based control method, the spatial wafer temperature non-uniformity can be well-controlled during the transient and steady-state period of thermal cycle respectively.

In real-time process control system, CD metrology is also critical in enabling the application of APC in lithography. Hence in this thesis, we investigated the CD metrology offered by scatterometer. For the very small CD value measurement using scatterometer, the beam size effect on the measurement result is not neglectable. Based on the direct beam size measurement method in a spectroscopic ellipsometry setup, the ray path of the scatterometer is numerically calculated for different beam sizes. The analysis shows that both the average optical path lengths and the optical path length differences are sensitive to the focus beam size. Experimental results also show that the difference in beam size led to different ellipsometric measurement results for both uniform film and patterned wafer.

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Chapter 1

Introduction

1.1 Motivation

Lithography has been extensively used in the manufacturing process of Very Large Scaled Integrated (VLSI) circuit and Micro-electromechanical system (MEMS) [1]-[3]. In semiconductor manufacturing, lithography alone takes up about 40% to 50% of the total wafer-processing time [4] and accounts for 30% to 35% of the chip manufacturing cost [5, 6]. The demand for faster and larger scale integrated circuits (IC) has pushed the continuing down-scaling of the transistors printed on the silicon wafer. As a result, the IC production equipments and materials are stretched towards their limits and the lithography process is seen as the key driver in feature shrinkage.

Figure 1.1 shows a typical lithography sequence [7]. This sequence of opera-

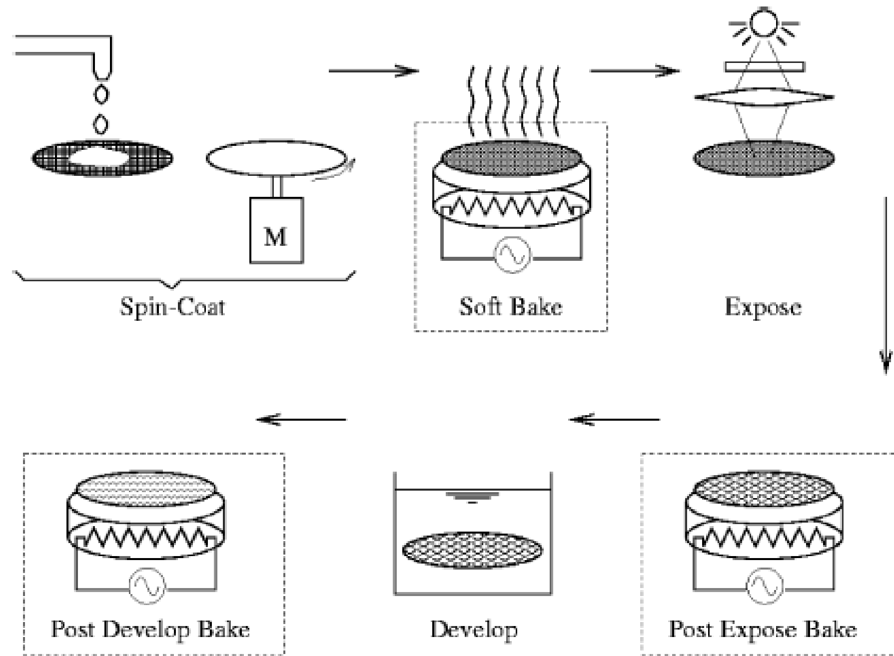


Figure 1.1. Typical steps in the lithography sequence [7].

tions begins with a priming step to promote adhesion of the polymer photoresist material to the substrate. The solvent is evaporated from the photoresist by a soft-bake process. In the exposure step, the resist-coated substrate is exposed to project the desired patterns from the photomask to the resist film. After patterning with deep ultraviolet (DUV) radiation, a post-exposure bake (PEB) is performed to stimulate the chemical reaction that alters the resist solubility of the exposed areas. A subsequent chemical development step then removes the exposed/reacted photoresist material while keeps the non-exposed areas in place (or vice versa for negative resists). The developed resist is then baked to promote etching stability. In a typical IC fabrication process, these steps could be repeated up to 30 times [7].

The accuracy of circuit patterns generated by the lithography process is assessed by critical dimension (CD) or line-width of the patterned feature on the photoresist.

Both gate delay and drive current are proportional to the inverse of the gate length which is determined by CD. It is estimated that 1nm variation in channel CD is equivalent to 1MHz chip-speed variation, and is thus worth about US$7.50 in the chip's unit selling price [8]. Yu *et al.* [9] have concluded that CD variation is mostly attributed to the lithography step, rather than the other process steps. It is therefore of great importance to precisely control and monitor the dimensions of these resist features in lithography, as these features that determine the dimensions of the actual device features may be reworked upon detecting a deviation from the process specification [10].

Table 1.1 shows the lithography technology node as outlined by the International Technology Roadmap for Semiconductors (ITRS) [11]. A 20% to 30% shrinkage in CD value is projected every two or three years. The drive towards smaller device geometries has placed much tighter control limits on the various semiconductor manufacturing processes. As the industry transitions to sub-100 nm, maintaining adequate and affordable lithographic process latitude becomes an increasingly challenging and difficult task.

Table 1.1. Lithography technology requirements

Year of Production	2007	2009	2011	2013	2015	2017
DRAM 1/2 pitch (Linewidth) (nm)	65	50	40	32	25	20
CD control (3 sigma) (nm)	6.6	5.3	4.2	3.3	2.6	2.1
PEB Sensitivity (nm/°C)	1.75	1.5	1.5	1	1	1

The application of advanced process control (APC) methodology has been increasingly utilized in recent years to enable the lithography process to print smaller

devices [12]- [14]. However, the APC method alone can not meet the stringent CD uniformity requirements because of the inherent drawbacks of the traditional equipments and lack of real-time sensing technology.

Thermal processing system in lithography is conventionally designed with large thermal mass and sluggish dynamics so that it is robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Although advanced control can be used to improve performance [15]- [18], it has been shown that the conventional hotplate design has poor controllability [19] due to its inherent sluggish dynamic response and that ultimately limits the achievable performance. Moreover, to achieve demanding CD control tolerances, the process parameters need to be real-time adjusted based on in-situ sensors monitoring the conditions of the process [12]. The lack of in-situ metrology has become a major bottle-neck to meet the more and more stringent requirements [11].

Consequently, the prossing control system in lithography requires careful consideration, including advanced process control techniques, equipment design and process monitoring. In this thesis we will investigate the application of APC, new equipment design and sensing technology for the processes in the lithography sequence.

(A) Process Control & Equipment Design

As shown in Figure 1.1, the lithography sequence includes numerous baking steps such as the soft bake, post-exposure bake and post-develop bake [20]. In some cases, additional bake steps are employed. Each of these baking steps serve different roles in transferring latent image into the substrate. To meet the stringent CD control specification, temperature uniformity is critical in photoresist processing, and the most important or temperature sensitive step is post-exposure bake among all of the bake steps in lithography [21]. Zhang *et al.* [22] showed that the CD variation reduction of 40% can be realized by employing advanced thermal processing system and control method in PEB step. Ho *et al.* [23] also demonstrated that real-time control of the PEB temperature to give nonuniform temperature distribution across the wafer can reduce CD nonuniformity to as small as 1nm across the wafer. Masahide *et al.* [24] further verified that the resist pattern CD uniformity improvement through PEB control can contribute to device performance improvement. It was reported that the temperature variation in PEB step can results in more than 10% of target CD [25]. For every degree variation in wafer temperature uniformity during the baking process, CD can vary by as much as 20nm [26]. Parker and Renken [21] list the temperature specifications for resist processing steps which include a uniformity requirement of 0.12°C for DUV PEB. A number of recent investigations also show the importance of proper temperature uniformity, during both transient and steady-state conditions, in significantly enhancing the CD uniformity across the wafer [27]- [32]. According to the ITRS lithography report [11], the post-exposure bake resist sensitivity to temperature will be more stringent for each new lithography generation as depicted in

Table 1.1. By the year 2013, the post-exposure bake resist sensitivity is expected to be 1nm/°C, making temperature control even more critical. One approach is to make less temperature sensitive resist materials. Our approach is to apply control and signal processing technologies together with equipment design to reduce wafer temperature variation. With precise temperature control, existing resists can be used for future technology nodes.

The conventional PEB step is conducted by transferring the cold wafer to the hot bake-plate where it is baked at a temperature typically between 70°C and 150°C for a time period between 60s and 90s. The heated wafer is then mechanically transferred to a chill-plate where it is cooled to a temperature between 18°C and 30°C [33]. Even with state-of-the-art wafer tracks, the across-wafer PEB temperature range can be as much as 9°C during the heating and cooling transient and 0.7°C during the steady-state [29]. While better performance has been recorded [34]- [37], it is very difficult to achieve good uniformity, especially during the transient phase, due to the lack of temperature control during wafer transport, heating and cooling transients. Our objective is to provide an effective control method to improve the dynamic performance of the wafer temperature the baking process using conventional bake-plate.

As discussed previously, the application of advanced control algorithm alone is not sufficient to meet the stringent CD uniformity requirement. The poor controllability of the conventional hotplate design ultimately limits the achievable performance of APC method. Other disadvantages of the hot plates include un-

controlled and non-uniform temperature fluctuation during the mechanical transfer of the substrates from the bake plate to chill plate, and spatial temperature non-uniformities during the entire thermal cycle [13], [38]. The lacking of a real-time, distributed and closed-loop temperature control method in the conventional hot plate is a source of process error in the lithography chain. Our objective is to design a new thermal processing system to achieve rapid dynamic temperature response and minimize the temperature nonuniformity during the transfer from heating to cooling process by real-time wafer temperature control method.

(B) Integrated Metrology

Real-time process control requires in-situ measurement. CD metrology plays a key role enabling productivity gains made through APC in lithography. The continuing decreasing of CD size has also led to smaller process control windows that drive a need for higher precision metrology to maintain an acceptable precision-to-tolerance ratio. According to the metrology report of ITRS [11], the next generation lithographic technology requires advances in the area of metrology for CD measurement.

Various techniques have been both proposed and implemented for these purposes. Among them, scatterometry is considered as an ideal candidate for in-situ process monitoring. The optical instrument can be made small enough to fit in the space of the bake module on a wafer track, enabling a true wafer-by-wafer metrology scheme. Furthermore, the quality (full profile versus top-town view)

and quantity (accuracy, precision, and throughput) of the collected data underscore its clear advantage for inline application [39].

Scatterometry is based on the reconstruction of the index of refraction grating profile from its optical diffraction responses. Single-wavelength variable-angle reflectometer is the first optical configuration used on commercial scatterometry systems [40]. The system shines a beam of light perpendicular to the direction of the grating lines, and analyzes the reflectance from the grating at multiple angles of incidence.

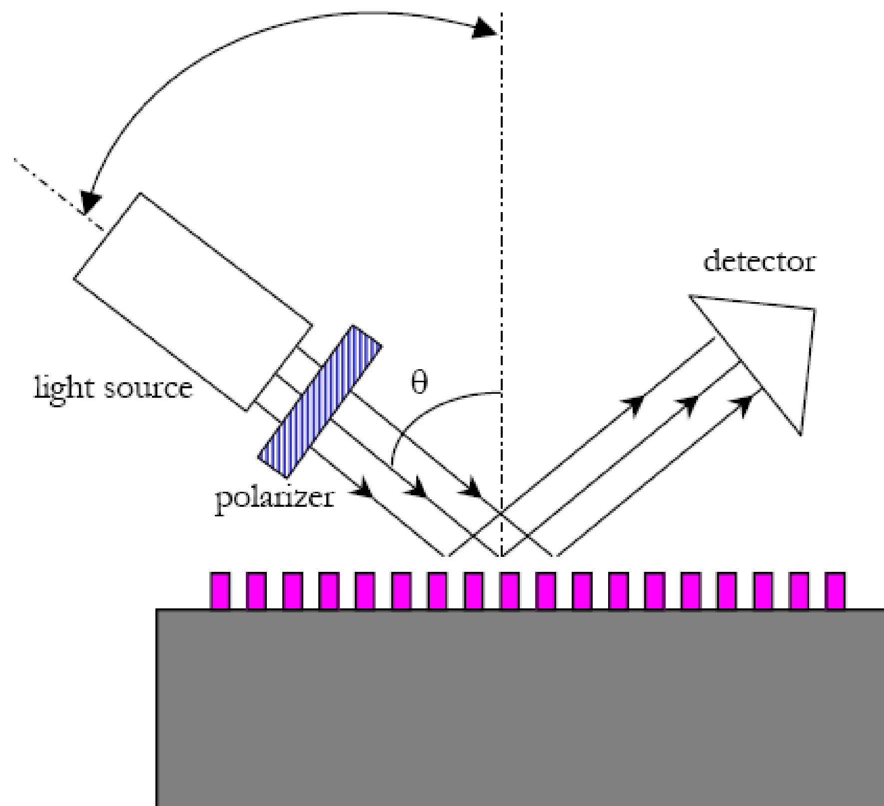


Figure 1.2. Single wavelength, variable angle reflectometer

Figure 1.2 illustrates a typical single-wavelength variable-angle reflectometer system. A laser light source directs single-wavelength light on the sample structure

after passing a polarizer. Depending on the grating pitch and the light wavelength, there can be multiple orders of diffraction from the grating (which are not drawn in the figure), but only the zeroth-order of diffracted light is collected by the detector. When the angle of incidence is varied, the detector angle varies accordingly. Therefore, this configuration is also called $2-\theta$ scatterometry.

Since a laser source can be used for $2-\theta$ scatterometry, its optical setup is relatively easy compared to configurations with broadband light sources, and the signal to noise ratio can be quite high. The key drawback of the $2-\theta$ scatterometry configuration is also due to its single-wavelength light source. For most of the grating structures, the sensitive wavelength range can vary from UV to IR depending on the structure, and very often it does not cover the wavelength of the $2-\theta$ scatterometry light source. Furthermore, it is unable to distinguish neighboring film stacks with similar refractive indices at the measurement wavelength. The other disadvantage is that only the intensity of the reflectance signal is obtained, which may contain less profile information than those systems such as the ellipsometer that can also get phase information from the reflectance.

In contrast to variable-angle scatterometry, Niu *et al.* [41] proposed a specular spectroscopic scatterometry, which makes use of the existing spectroscopic ellipsometry (SE) equipment to measure intensity and phase of the zeroth-order diffraction at a fixed incident angle and multiple wavelengths. This type of information, coupled with a very efficient rigorous coupled-wave analysis (RCWA) [42] implementation, seems to be adequate for detailed reconstruction of the profiles of

periodic gratings.

Spectroscopic ellipsometry is a surface analytical technique that provides the reflected light amplitude and phase information through measurement of states of polarization of the reflected light. This technique is widely used in thin film analysis [43]- [46] due to its ability to provide easily conducted nondestructive measurements without the need for vacuum environments. It has been established that the measured ellipsometric signal will vary according to the probing light beam size and its collimation under the presence of optical inhomogeneity in the film [46]. Thus, using the specular spectroscopic scatterometry to measure photoresist layer thickness and CD value, the beam size effect of the ellipsometer must be taken into consideration.

1.2 Contributions

In this thesis, advanced process control, equipment design and metrology design are applied to the lithography sequence. The thesis contributions are summarized as follows.

(A) Real-time Spatial Wafer Temperature Control

As discussed in section 1.1, the wafer temperature spatial uniformity, in both transient and steady-state phase, plays an important role in final CD uniformity. A real-time wafer temperature control method is thus proposed to minimize tem-

perature nonuniformity in the whole heating process and improve the dynamic performance of the wafer temperature. To control the wafer temperature uniformity, we developed a detailed simulation model based on first principle heat transfer analysis of the system. By adopting the model, the average air-gap thickness between the bake-plate and wafer in each of the heating zones can be extracted and consequently the wafer temperature can be estimated online. Experimental result shows that the estimated wafer warpage and temperature are accurate, with which the wafer temperature nonuniformity can be controlled in real time.

Comparing to the steady-state wafer temperature control approach [47], the proposed real-time control approach takes the dynamic properties of the system into consideration. A detailed physical model of the thermal system is first developed with unknown air-gap thickness. Next, by monitoring the bake-plate temperature and fitting these data into the model, the air-gap thickness can be estimated and the wafer temperature can be calculated and controlled in real-time. This is useful as production wafers usually do not have temperature sensors embedded on it, these bake-plates are usually calibrated based on test wafers with embedded sensors. However, as processes are subjected to process drifts, disturbances, and wafer warpages, real-time correction of the bake-plate temperatures to achieve uniform wafer temperature is not possible in current baking systems. Any correction is done based on run-to-run control techniques which depend on the sampling frequency of the wafers. The approach is real-time and can correct for any variations in the desired wafer temperature performance during both transient and steady-state phase.

The proposed approach is applied to a conventional multi-zone thermal processing system, where the root mean square (RMS) of temperature nonuniformity in the entire thermal cycle was improved by more than 80%. The profile of the warped wafer can also be estimated from the extracted air-gap thickness during the steady-state phase.

(B) Design and Implementation of Programmable Integrated Bake/Chill System

The real-time spatial wafer temperature control method provides an effective way to improve wafer transient temperature uniformity. However, the achievable performance gain is ultimately limited by the drawbacks of the conventional baking system. Firstly, the wafer dynamic response is constrained by the inherent sluggish dynamic of the bake plate due to its large thermal mass. Secondly, the mechanical wafer transfer from hot plate to chill plate results in the uncontrollable wafer temperature fluctuations.

To solve the above mentioned problems, we developed a novel design of bake/chill integrated thermal processing module to achieve rapid dynamic response and good wafer temperature controllability throughout the entire processing temperature cycle of ramp, hold and quench in lithography. The system integrates the baking and chilling processes of the lithography sequence, and thus eliminates the undesirable and uncontrollable temperature fluctuations during the substrate transfer process. Moreover, the system is also physically compact and easy to implement.

In the designed bake/chill integrated thermal processing module, a set of thermoelectric devices (TEDs) are employed as the main mode of heat transfer. The TEDs can provide rapid distributing heating to the substrate for facilitating uniformity and transient temperature control. Besides, the TEDs are also used to provide active cooling for chilling the substrate to a temperature suitable for subsequent processing steps. In the designed module, the resistance temperature detectors (RTDs) are embedded in the proximity pins to provide in-situ temperature measurement.

The proposed module is analyzed via first principle heat transfer analysis and backed up by experimental validation. By adopting a new proposed model based feedback control algorithm, the temperature difference between the feedback points can be minimized to less than 0.1°C in the entire thermal process. In addition, the wafer spatial temperature nonuniformity can be well-controlled within the range of ±0.3°C and ±0.1°C during the transient and steady-state phase respectively.

(C) Investigation of Beam Size Effect on Scatterometer Measurement

As discussed in section 1.1, scatterometer, which makes use of the existing spectral ellipsometry, has been considered as an ideal candidate for in-situ process monitoring. Our ultimate objective is to integrate SE-based CD metrology in the real-time control process in lithography. For the decreasing CD value measurement, the effect of beam size on the ellipsometry measurement result must be taken into consideration. In this thesis, the beam size effect on ellipsometry result is

investigated.

A new direct beam size measurement method in a spectroscopic ellipsometry setup is firstly proposed to define the beam size value. The technique uses the existing detection facilities in a spectroscopic ellipsometry setup to determine the beam size without the need to rearrange the optical components. The change of the reflected light when the incident light illuminates on the moving sample's edge is recorded in experiment. In this case the recorded intensity signal comprises a coupled boundary diffraction and knife edge wave that can be isolated using nonlinear fitting. This then permits an accurate measurement of the beam size with the stronger knife edge component.

Based on the beam size measurement method, geometric ray at the illumination and recording ends of spectroscopic ellipsometry is then analyzed for different beam size values. The numerical analysis and further experimental results revealed substantial changes ellipsometry result with different beam sizes for both uniform thickness films and patterned samples.

1.3 Organization

This thesis is organized as follows. In Chapter 2, a real-time and in-situ approach to control the wafer spatial temperature uniformity in both transient and steady-state phase of the thermal process using a multi-zone baking system. A programmable multi-zone integrated bake/chill thermal processing system for across-wafer tem-

perature uniformity control is designed and developed in Chapter 3. Chapter 4 describes a direct beam size measurement method based on the spectroscopic ellipsometry setup and investigates the beam size effect on the ellipsometer measurement result for both uniform film and patterned wafer. Conclusions and future work are given in Chapter 5.

Chapter 2

In-situ Real-time Spatial Wafer Temperature Control

2.1 Introduction

Thermal processing of semiconductor substrate is common and critical to photoresist processing in the lithography sequence. As discussed in Chapter 1, temperature uniformity control is an important issue in photoresist processing with stringent specifications and has a significant impact on the linewidth or CD. The most temperature sensitive step in the lithography sequence is the PEB step. Requirements call for temperature to be controlled within 0.1°C at temperatures between 70°C and 150°C. A number of recent investigations also showed the importance of proper bake-plate operation, both in steady-state and transient, on CD control [48], [49].

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake-plate for a given period of time. The heated bake-plate is usually of large thermal mass and is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake-plate near the surface. The wafers are usually placed on proximity pins. When a wafer at room temperature is placed on the bake-plate, the temperature of the bake-plate drops at first but recovers gradually because of closed-loop control. Different air-gap sizes will result in different wafer and plate temperature due to the difference in the air-gap thermal resistance between the substrates and the bake-plate. A warped wafer will thus affect the various baking processes in the lithography sequence and cause temperature nonuniformity across wafer.

A fast in-situ approach to estimating wafer warpage profile during thermal processing [50] was developed to deal with the problem. It demonstrates that information of the average air-gap between the wafer and the bake-plate can be obtained with the use of system theory tools. The relationship between the wafer and plate temperature at steady-state can be derived from physical modeling of the baking process. By monitoring the maximum plate temperature drop, the average air-gap in each bake-plate zone can be estimated, and the new bake-plate temperature set point to achieve desirable wafer steady-state temperature [47]. In this way, the wafer steady-state temperature nonuniformity can be controlled to less than 0.1°C, but one of the major drawbacks of the mentioned approach is that it does not take into account the dynamic performance of the wafer temperature.

It has been reported that even though the steady-state temperature ranges was minimized, the resulting gains in CD uniformity cannot be realized attributed to the temperature distribution while rising to the PEB temperature [51].

In this work, we present an in-situ approach to real-time estimation of wafer warpage and control of both the transient and the steady-state wafer temperature uniformity during the baking steps in the lithography process. Our objective is to control the wafer temperature to its desired value and minimize the spatial temperature nonuniformity across the wafer during the whole thermal cycle using the multi-zone bake-plate as shown in Figure 2.1. Based on the detailed thermal model of baking process and the real-time measurement of bake-plate temperature, an in-situ approach is developed to estimate and control the wafer temperature. Using the proposed approach, the wafer spatial temperature uniformity during the entire thermal cycle achieved an improvement of more than 80% when compared to the existing methods.

This chapter is organized as follows, in section 2.2 the detailed model of the thermal processing system is developed based on first principle of heat transfer. The control structure and experimental result are given in section 2.3 to demonstrate the effectiveness of the proposed method. Finally, conclusions are given in section 2.4.

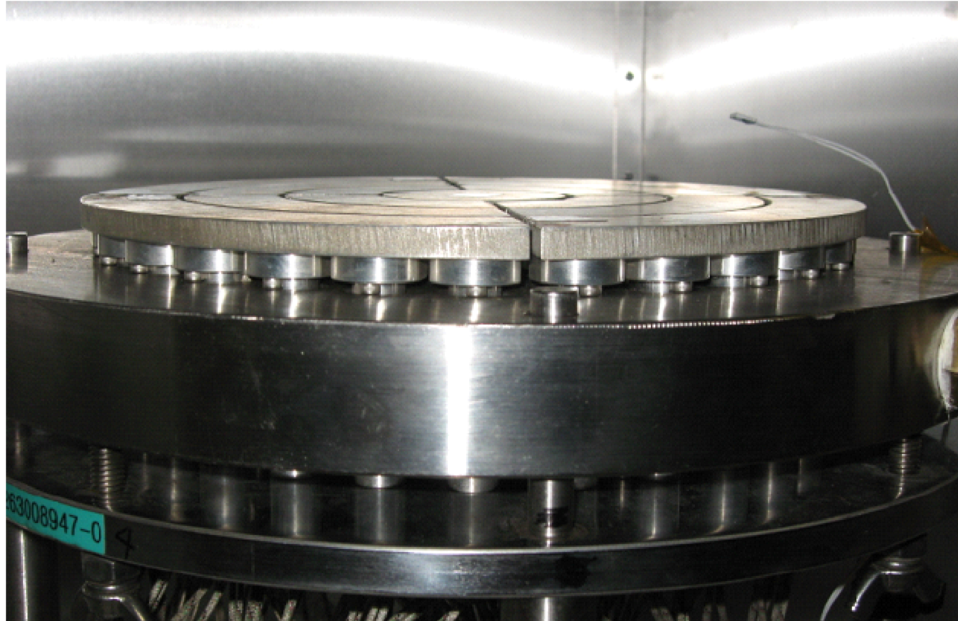


Figure 2.1. Programmable multi-zone thermal processing system.

2.2 Thermal Modeling of the System

The distributed thermal processing system used in this work is shown in Figure 2.2. In this section, a physical model will be derived for a N-zone bake-plate based on first principle of heat transfer. Analysis of the thermal processing system can be done with a model considering radial as well as the axial effects of heat transfer in the module. The bake-plate is discretized into different zones and separated with a small air-gap of approximately 1mm for thermal insulation. The fact that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability.

In the baking process, the bake-plate is heated up by the cartridge heater attached to it. Resistive heating elements are embedded in each of the heater. Each heating zone is configured with its own temperature sensor and electronics

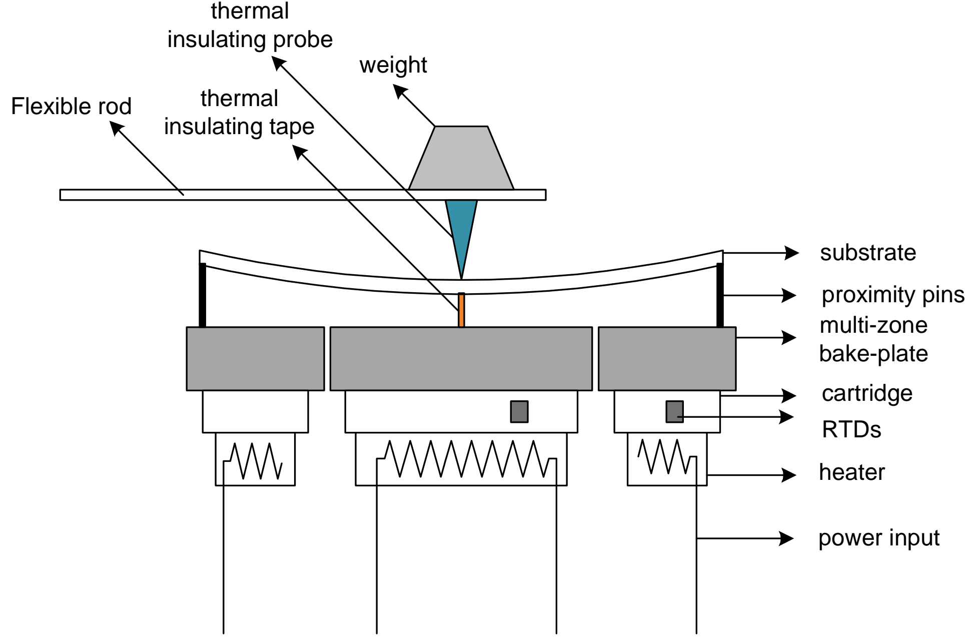


Figure 2.2. Schematic diagram of the thermal processing system.

embedded in the cartridge for feedback control. Depending on application, the number of zones of the bake-plate can be easily configured.

Spatial distribution of temperature and other quantities in a silicon wafer are most naturally expressed in a cylindrical coordinate system as shown in Figure 2.3. Energy balances on the elements in the system can then be carried out to obtain a thermal model as follows:

$$C_w \dot{T}_w = q_w^{in} + q_w^{out} + q_w^{top} + q_w^{bottom} \tag{2.1}$$

$$C_{ag} \dot{T}_{ag} = q_{ag}^{in} + q_{ag}^{out} + q_{ag}^{top} + q_{ag}^{bottom} \tag{2.2}$$

$$C_p \dot{T}_p = q_p^{in} + q_p^{out} + q_p^{top} + q_p^{bottom} \tag{2.3}$$

$$C_{ap} \dot{T}_{ap} = q_{ap}^{in} + q_{ap}^{out} + q_{ap}^{top} + q_{ap}^{bottom} \tag{2.4}$$

$$C_c\dot{T}_c = q_c^{side} + q_c^{top} + q_c^{bottom} \tag{2.5}$$

$$C_h\dot{T}_h = q_h^{side} + q_h^{top} + q_h^{bottom} + q^{input} \tag{2.6}$$

where T is the temperature above the ambient, q^{in}, q^{out}, q^{top}, and q^{bottom} the heat flow into the element from inner zone, outer zone, top surface and bottom surface respectively, q^{side} the heat flow rate from side surface, q^{input} the heater input power, and the subscribe w, ag, p, ap, c, and h represent the wafer, the air-gap, the bake-plate, the air-gap separating the bake-plate, the cartridge and the heater respectively, C is the thermal capacitance, for each element, $C = \rho c_v V$, where ρ is the density, c_v the specific heat capacity, and V the volume of the element.

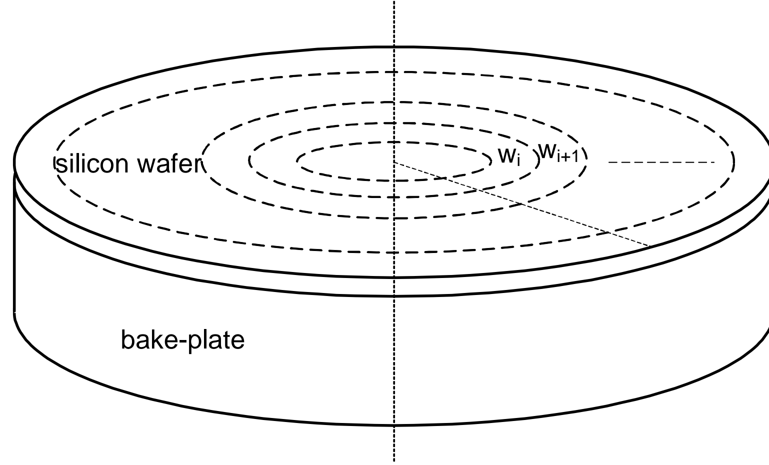


Figure 2.3. Thermal model discretization of wafer and bake-plate.

2.2.1 Wafer and Air Gap Modeling

For the wafer in the system, q_w^{in} and q_w^{out} are the conduction heat flow from the inner and outer adjacent wafer element, for the wafer of zone i, we have

$$q_{w(i)}^{in} = \frac{k_w A_{ws(i-1)}}{\triangle_r}(T_{w(i-1)} - T_{w(i)}), \qquad 2 \leq i \leq N \tag{2.7}$$

$$q_{w(i)}^{out} = \begin{cases} \frac{k_w A_{ws(i)}}{\triangle_r}(T_{w(i+1)} - T_{w(i)}), & 1 \leq i \leq N-1 \\ h_w A_{ws(N)}(-T_{w(N)}), & i = N \end{cases} \tag{2.8}$$

where k is the thermal conductivity coefficient, $A_{s(i)}$ the contact area between the adjacent elements i and $i+1$, $A_{s(N)}$ the side surface area, and $\triangle_r$ the distance between the centroid of the adjacent element, h the convection coefficient, which can be calculated from [52] as

$$h = \frac{k}{L}\overline{N_u} \tag{2.9}$$

where $\overline{N_u}$ is the Nusselt number, L is the characteristic length, and from [52], we have

$$\overline{N_u} = \{0.60 + \frac{0.387Ra^{1/6}}{[1 + (0.559/Pr)^{9/16}]^{8/27}}\}^2 \tag{2.10}$$

The wafer top surface is exposed to the surroundings and so we have

$$q_{w(i)}^{top} = h_w A_{wz(i)}(-T_w), \qquad 1 \leq i \leq N \tag{2.11}$$

where $A_{wz(i)}$ the top area of wafer element i exposed to the ambient.

The air-gap between the wafer and bake-plate is about 210μm. Since it is much less than 5.8mm, and their temperature difference is considerably smaller than 200°C [53], the heat transfer mechanism is essentially conductive and given by

$$q_{w(i)}^{bottom} = -k_{ag} A_{ag} \frac{\partial T_{ag}}{\partial z_{ag}} |_{boundary} \tag{2.12}$$

where z is the thickness.

The above equation can be expressed in difference equation as

$$q_{w(i)}^{bottom} = \frac{A_{wag(i)}(T_{ag(i)} - T_{w(i)})}{z_{ag}/2k_{ag} + z_w/2k_w}, \qquad 1 \leq i \leq N \tag{2.13}$$

where $A_{wag(i)}$ is the contact cross-sectional area between wafer and air-gap layer of element i.

For the air-gap layer, similarly, we have,

$$q_{ag(i)}^{in} = \frac{k_{ag} A_{ags(i-1)}}{\triangle_r}(T_{ag(i-1)} - T_{ag(i)}), \qquad 2 \leq i \leq N \tag{2.14}$$

$$q_{ag(i)}^{out} = \begin{cases} \dfrac{k_{ag} A_{ags(i)}}{\triangle_r}(T_{ag(i+1)} - T_{ag(i)}), & 1 \leq i \leq N-1 \\ h_{ag} A_{ags(N)}(-T_{ag(N)}), & i = N \end{cases} \tag{2.15}$$

$q_{ag(i)}^{top}$ is the heat flow from the wafer layer by conduction,

$$q_{ag(i)}^{top} = \frac{A_{wag(i)}(T_{w(i)} - T_{ag(i)})}{z_{ag}/2k_{ag} + z_w/2k_w}, \qquad 1 \leq i \leq N \tag{2.16}$$

For the bottom of the air-gap layer, one part of the layer contact with the bake-plate and the other part contact with the air-gap inside the bake-plate, so we have

$$q_{ag(i)}^{bottom} = \frac{A_{agp(i)}(T_{p(i)} - T_{ag(i)})}{z_{ag}/2k_a + z_p/2k_p} + 2k_a A_{agap(i)} \frac{T_{ap(i)} - T_{ag(i)}}{z_{ag} + z_p}, \qquad 1 \le i \le N \quad (2.17)$$

where $A_{agp(i)}$ is the contact cross-sectional area between air-gap layer and the bake-plate of element i, and $A_{agap(i)}$ the contact cross-sectional area between air-gap layer and the air-gap in the bake-plate of element i.

2.2.2 Bake-Plate Modeling

The bake-plate in different zones are seperated by small air-gaps with thickness of 1mm, so q_p^{in} and q_p^{out} are the conduction heat flow from the inner and outer air-gap, thus we have

$$q_{p(i)}^{in} = \frac{A_{ips(i)}}{t_{p(i)}/2k_p + t_{ap(i-1)}/2k_a}(T_{ap(i-1)} - T_{p(i)}), \qquad 2 \le i \le N \qquad (2.18)$$

$$q_{p(i)}^{out} = \begin{cases} \frac{A_{ops(i)}}{t_{p(i)}/2k_p + t_{ap(i)}/2k_a}(T_{ap(i)} - T_{p(i)}), & 1 \le i \le N-1 \\ h_p A_{ps(N)}(-T_{p(N)}), & i = N \end{cases} \qquad (2.19)$$

where $A_{ips(i)}$ is the contact area between the bake-plate of zone i and the inner adjacent air-gap, $A_{ops(i-1)}$ the contact area between the bake-plate of zone i and

the outer adjacent air-gap, and $t_{p(i)}$ and $t_{ap(i)}$ represent the horizontal thickness of the bake-plate and the air-gap inside the bake-plate of element i respectively.

$$q_{p(i)}^{top} = \frac{A_{agp(i)}(T_{ag(i)} - T_{p(i)})}{z_{ag}/2k_a + z_p/2k_p}, \qquad 1 \leq i \leq N \tag{2.20}$$

For the bottom of the air-gap layer, one part of the layer contact with the cartridge via epoxy layer and the other part contact with the ambient, so we have

$$q_{p(i)}^{bottom} = \frac{T_{c(i)} - T_{p(i)}}{\dfrac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}} + h_p A_{pa(i)}(-T_{p(i)}), \qquad 1 \leq i \leq N \tag{2.21}$$

where $A_{pc(i)}$ is the contact cross-sectional area between the bake-plate and the cartridge of element i, and $A_{pa(i)}$ the contact cross-sectional area between the bake-plate and the bottom ambient of element i, $R_{ex(i)}$ the thermal resistance of epoxy layer of element i, $R_{ex(i)} = \dfrac{z_{ex}}{k_{ex}A_{pc(i)}}$.

For the air-gap separating the bake-plates, we have

$$q_{ap(i)}^{in} = \frac{A_{ops(i)}}{t_{p(i)}/2k_p + t_{ap(i)}/2k_a}(T_{p(i)} - T_{ap(i)}), \qquad 1 \leq i \leq N-1 \tag{2.22}$$

$$q_{ap(i)}^{out} = \frac{A_{ips(i+1)}}{t_{p(i+1)}/2k_p + t_{ap(i)}/2k_a}(T_{p(i+1)} - T_{ap(i)}), \qquad 1 \leq i \leq N-1 \tag{2.23}$$

$$q_{ap(i)}^{top} = 2k_a A_{agap(i)} \frac{T_{ag(i)} - T_{ap(i)}}{z_{ag} + z_p}, \qquad 1 \leq i \leq N-1 \tag{2.24}$$

$$q_{ap(i)}^{bottom} = h_{ap} A_{agap(i)}(-T_{ap(i)}), \qquad 1 \leq i \leq N-1 \tag{2.25}$$

2.2.3 Cartridge and Heater Modeling

The cartridge's side surface are exposed to the ambient air, so the heat transfer on the side surface is convection with the air,

$$q_{c(i)}^{side} = h_c A_{cs(i)}(-T_{c(i)}), \qquad 1 \leq i \leq N \tag{2.26}$$

The cartridge top surface is attached to the bake-plate via epoxy layer, so we have

$$q_{c(i)}^{top} = \frac{T_{p(i)} - T_{c(i)}}{\frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}}, \qquad 1 \leq i \leq N \tag{2.27}$$

For the bottom surface of the cartridge,one part of the bottom heat flow is the conduction with the heater and the other part is the convection with the ambient air,

$$q_{c(i)}^{bottom} = \frac{A_{ch(i)}(T_{h(i)} - T_{c(i)})}{z_c/2k_c + z_h/2k_h} + h_c A_{ca(i)}(-T_{c(i)}), \qquad 1 \leq i \leq N \tag{2.28}$$

where $A_{ch(i)}$ is the contact cross-sectional area between the cartridge and the heater of element i, and $A_{ca(i)}$ the area of the cartridge bottom surface of element i exposed to the ambient .

Similarly, for the heater, we have

$$q_{h(i)}^{side} = h_h A_{hs(i)}(-T_{h(i)}), \qquad 1 \leq i \leq N \tag{2.29}$$

$$q_{h(i)}^{top} = \frac{A_{ch(i)}(T_{c(i)} - T_{h(i)})}{z_c/2k_c + z_h/2k_h}, \qquad 1 \leq i \leq N \tag{2.30}$$

$$q_{h(i)}^{bottom} = h_h A_{ha(i)}(-T_{h(i)}), \qquad 1 \leq i \leq N \tag{2.31}$$

where $A_{ha(i)}$ is the area of the heater bottom surface of element i exposed to the ambient.

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from 15°C to 150°C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks [54] as tabulated in Table 2.1.

From the heat transfer differential equations, we can derive the state-space format model of the system as Equation 2.32 (See Appendix A1 for details).

Table 2.1. Physical parameters of the thermal processing system [54].

	Property	Value
Wafer (silicon)	Density, ρ	2330kgm^{-3}
	Specific heat capacity, c_v	$750\text{JK}^{-1}\text{kg}^{-1}$
	Thermal conductivity, k	$99\text{Wm}^{-1}\text{K}^{-1}$
	Convection coefficient, h	$3.3824\text{Wm}^{-2}\text{K}^{-1}$
	Thickness, z	0.700mm
Air	Density, ρ	1.1kgm^{-3}
	Specific heat capacity, c_v	$1000\text{JK}^{-1}\text{kg}^{-1}$
	Thermal conductivity, k	$0.03\text{Wm}^{-1}\text{K}^{-1}$
Bake-plate (aluminum)	Density, ρ	2700kgm^{-3}
	Specific heat capacity, c_v	$917\text{JK}^{-1}\text{kg}^{-1}$
	Thermal conductivity, k	$250\text{Wm}^{-1}\text{K}^{-1}$
	Convection coefficient, h	$7.271\text{Wm}^{-2}\text{K}^{-1}$
	Thickness, z	6.8mm
Epoxy	Thermal conductivity, k	$0.35\text{Wm}^{-1}\text{K}^{-1}$
	Thickness, z	0.02mm
Cartridge (aluminum)	Density, ρ	2700kgm^{-3}
	Specific heat capacity, c_v	$917\text{JK}^{-1}\text{kg}^{-1}$
	Thermal conductivity, k	$250\text{Wm}^{-1}\text{K}^{-1}$
	Convection coefficient, h	$4.86\text{Wm}^{-2}\text{K}^{-1}$
	Thickness, z	4.4mm
Heater (aluminum)	Density, ρ	2700kgm^{-3}
	Specific heat capacity, c_v	$917\text{JK}^{-1}\text{kg}^{-1}$
	Thermal conductivity, k	$250\text{Wm}^{-1}\text{K}^{-1}$
	Convection coefficient, h	$5.7828\text{Wm}^{-2}\text{K}^{-1}$
	Thickness, z	5.4mm

$$\dot{T} = \begin{bmatrix} \dot{T}_w \\ \dot{T}_{ag} \\ \dot{T}_p \\ \dot{T}_{ap} \\ \dot{T}_c \\ \dot{T}_h \end{bmatrix} = \begin{bmatrix} F_{ww} & F_{wag} & 0_{NN} & 0_{NN} & 0_{NN} & 0_{NN} \\ F_{agw} & F_{agag} & F_{agp} & F_{agap} & 0_{NN} & 0_{NN} \\ 0_{NN} & F_{pag} & F_{pp} & F_{pap} & F_{pc} & 0_{NN} \\ 0_{NN} & F_{apag} & F_{app} & F_{apap} & 0_{NN} & 0_{NN} \\ 0_{NN} & 0_{NN} & F_{cp} & 0_{NN} & F_{cc} & F_{ch} \\ 0_{NN} & 0_{NN} & 0_{NN} & 0_{NN} & F_{hc} & F_{hh} \end{bmatrix} \begin{bmatrix} T_w \\ T_{ag} \\ T_p \\ T_{ap} \\ T_c \\ T_h \end{bmatrix} + \begin{bmatrix} 0_N \\ 0_N \\ 0_N \\ 0_N \\ 0_N \\ G_{hh} \end{bmatrix} q^{input} = FT + Gq^{input} \quad (2.32)$$

To assess the quality of the proposed system model, we perform conventional baking process experiment and compare the simulation with the experimental results. The programmable thermal system can be configured up to 13 zones. Without loss of generality, we will verify the system dynamics for a two-radial-zone

system . Our objective is to demonstrate that the proposed model succeeds in predicting the experimental wafer temperatures using bake-plate temperature data and the input signal without resorting to the use of any fitting parameter and is therefore useful for scaling up.

In the experiment, a room temperature flat 200mm wafer is dropped on the baking system with proximity pin height of 140μm. This causes the bake-plate temperature drop at first but recovers gradually because of closed-loop control. Two proportional-integral (PI) controllers are used to control the two zones of the bake-plate. Figure 2.4 shows the comparison result of the simulation and experimental bake-plate and wafer temperature when the air-gap thickness is 140μm.

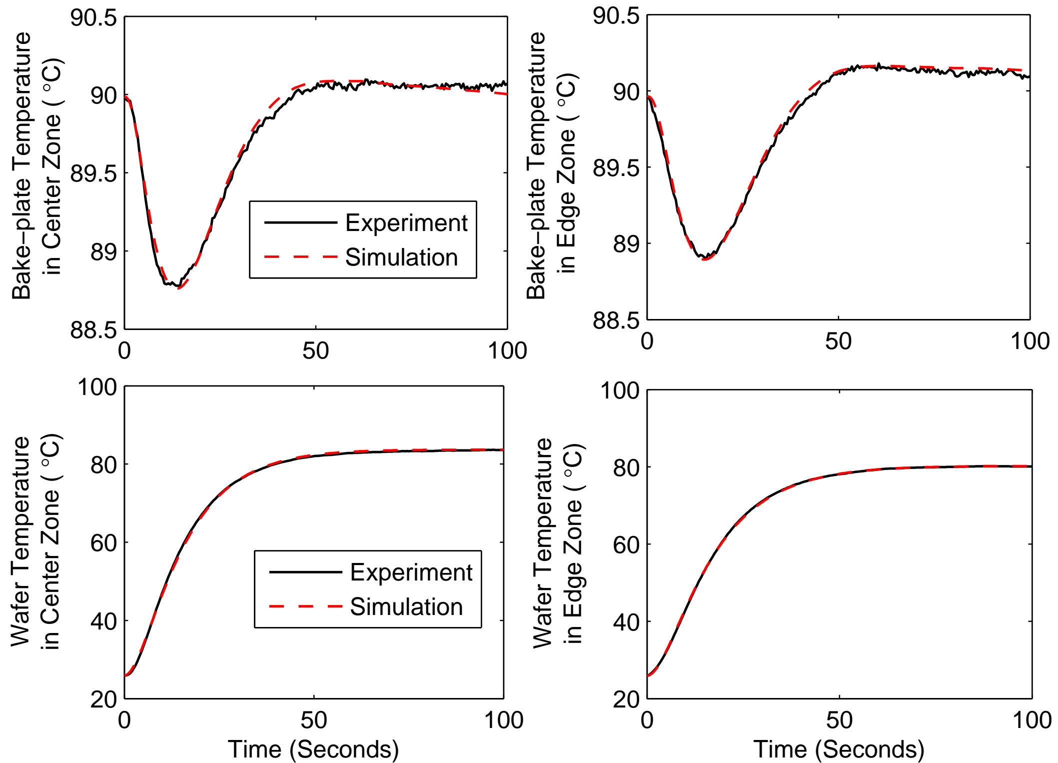


Figure 2.4. Plate and wafer temperature in simulation and experiment with air-gap thickness be 140μm using the calculated model.

It can be seen that the fit between of both the wafer and the bake-plate tem-

perature from simulation and experimental results are very closed, which verify the effectiveness of the proposed thermal model. This result demonstrates that by monitoring the bake-plate temperatures, T_p, and making use of system identification techniques, we are able to extract the air-gap information, z_a, between ith wafer and bake-plate elements from the system model. Then we will be able to calculate the wafer temperature and fulfill real-time control experiment to minimize the wafer temperature nonuniformity in the baking process.

2.3 Experimental Result

2.3.1 Experimental Setup

For experimental verification, warpage must be known. Wafer warpage is created mechanically as shown in Figure 3.2. We ensure minimal warpage during the baking experiment by mechanically pressing the center of the wafer against a thermal insulating tape of known thickness. The center-to-edge warpage is given by the difference between height of proximity pin and thermal tape thickness.

To guarantee the temperature accuracy in experiment, the temperature sensors (RTDs) are calibrated using a constant temperature heat bath NESLAB EX251HT. Measurements are taken from a range of temperatures between 25°C and 95°C and at intervals of 5°C. At every temperature interval, 50 readings are recorded for each of the sensors. An average value is then calculated for that sensor and

that particular temperature. For temperatures below 150°C, RTDs show strong linearity in the resistance-temperature relationship. Hence, a linear equation can be written as follows:

$$Y_T = \alpha T + \beta \tag{2.33}$$

where Y_T is the averaged temperature reading at temperature T, α and β are the coefficients to be determined. Least Squares Linear Regression can be used to calculate the coefficients α and β. Let

$$\theta = \begin{bmatrix} \alpha \\ \beta \end{bmatrix}, \Phi = \begin{bmatrix} T_1 & 1 \\ T_2 & 1 \\ \vdots & \vdots \\ T_2 & 1 \end{bmatrix} \; and \; Y = \begin{bmatrix} Y_{T_1} \\ Y_{T_2} \\ \vdots \\ Y_{T_n} \end{bmatrix}$$

Hence, θ can be found by

$$\theta = (\Phi^T \Phi)^{-1} \Phi^T Y \tag{2.34}$$

Obtaining α and β and using backward calculation

$$T = \frac{1}{\alpha} Y - \frac{\beta}{\alpha} \tag{2.35}$$

we can get the calibrated temperature from RTDs measurement.

The RTDs are attached to the wafer [33], [37] for temperature measurement. A control-system software was developed using the National Instruments LabView

programming environment [55] to create a multivariable PI control framework and a dynamic temperature control system. Two PI controllers of the following form are used to control the two zones of the bake-plate:

$$u(t) = K_{ci}\left(e(t) + \frac{1}{T_{Ii}}\int e(t)dt\right) \tag{2.36}$$

where $u(t)$ is the heating power injected in to the heater and $e(t)$ is the error between the desired and actual bake-plate temperatures. The experiments were conducted at a temperature setpoint of 90°C with a sampling and control interval of 0.2 seconds.

2.3.2 Control Structure

The proposed approach required detailed information of the system in order to identify the average air-gap during subsequent processing. We have got accurate state-space model in section 2.2. Based on the model, we can develop a grey-box state-space model with the air-gap thickness of the two zones as unknowns. In the experiment, the bake-plate temperature readings and input control signals are collected and fitted into the model to extract the air-gap thickness and wafer temperature.

Figure 2.5 shows the control systems framework, the bake-plate temperature, T_{p1} and T_{p2}, and the control signal, u_1 and u_2, in the two zones system are measured and sent to the estimator. The grey-box-model-based estimator will then estimate

the air-gap thickness and the wafer temperature of the two zones. The estimated air-gap thickness t_{ag} is then used to determine the set point r_{p1} of the bake-plate and the estimated wafer temperatures T_{ew1} and T_{ew2} are used to control the wafer temperature uniformity in the process.

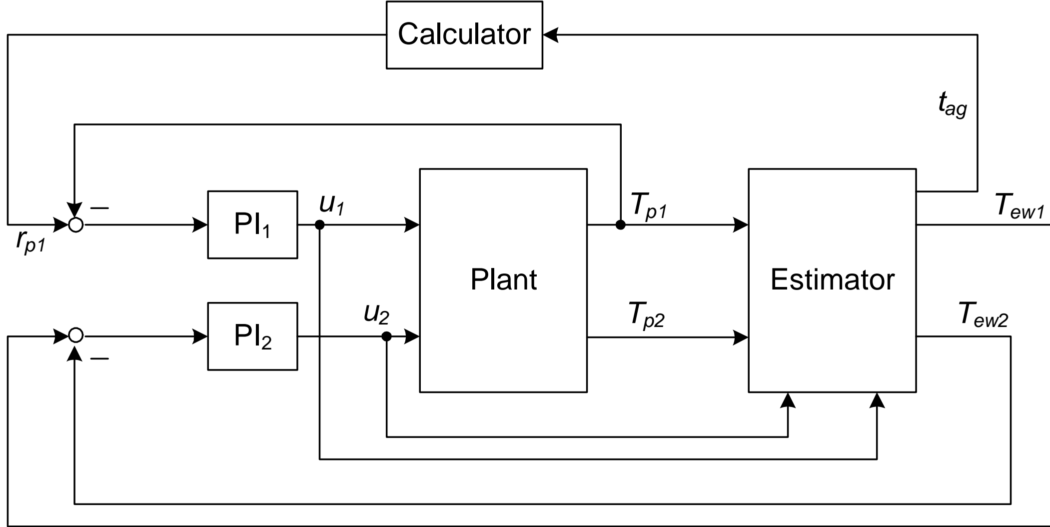


Figure 2.5. Block diagram of control structure.

Using this method, we can real-time estimate the air-gap thickness and wafer temperature and consequently regulate the control signal on-line to achieve desired wafer temperature and minimize temperature nonuniformity in the whole process. Furthermore, with the estimated air-gap thickness in steady-state, we can extract the wafer warpage profile.

2.3.3 Experimental Result

To demonstrate our approach, a flat wafer is firstly dropped on the bake-plate with a proximity pin height of 210μm. Figure 2.6 shows the estimated air-gap thickness with real-time control method. The final estimated air-gaps are tabulated

in Table 2.2. A good measure of extent warpage is to measure the deviation of the average air-gap from the proximity pin height. For the flat wafer, we can see that deviations are close to zero as expected.

Figure 2.7 shows the bake-plate and wafer temperature profiles using the steady-state temperature control method [47] and the proposed real-time control method. To validate our results, two temperature sensors (in this case RTDs) are embedded on the wafer surface corresponding to the center of each zone to monitor the wafer temperature. Figure 2.7 consists of two experimental runs, (1) and (2). Run (1) corresponds to the steady-state control approach when the wafer is dropped on the bake-plate. The air-gaps are first estimated based on the maximum bake-plate temperature drops. Then the new bake-plate temperature are set based on the estimated air-gap thickness as shown in Figure 2.7(a). Notice that the wafer temperature is controlled 90°C with a steady-state temperature nonuniformity of about 0.1°C as shown in Figure 2.7(b) and (c) .However, since the new bake-plate temperature set-points are implemented about 20 seconds after the wafer is dropped to allow the maximum temperature drop point to occur as well as for computational delay of the corresponding air-gap, the wafer can only reach steady-state after about 80 seconds as shown in Figure 2.7(b). Furthermore, the wafer has a temperature nonuniformity of about 4°C in transient period as shown in Figure 2.7(c).

Next, real-time control of the wafer temperature is implemented. Figure 2.7(b) and (c) of run (2) shows that the wafer temperature is controlled to 90°C within

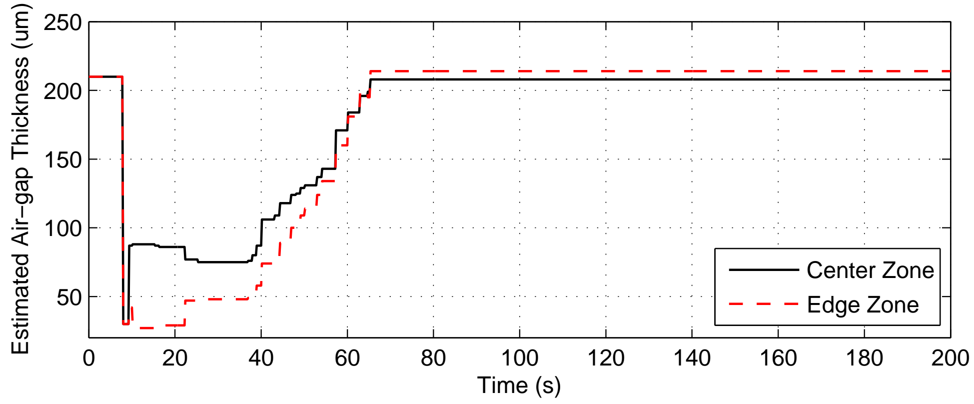


Figure 2.6. Estimated air-gap thickness using real-time control method when a flat wafer is dropped on bake-plate with proximity pin height of 210μm.

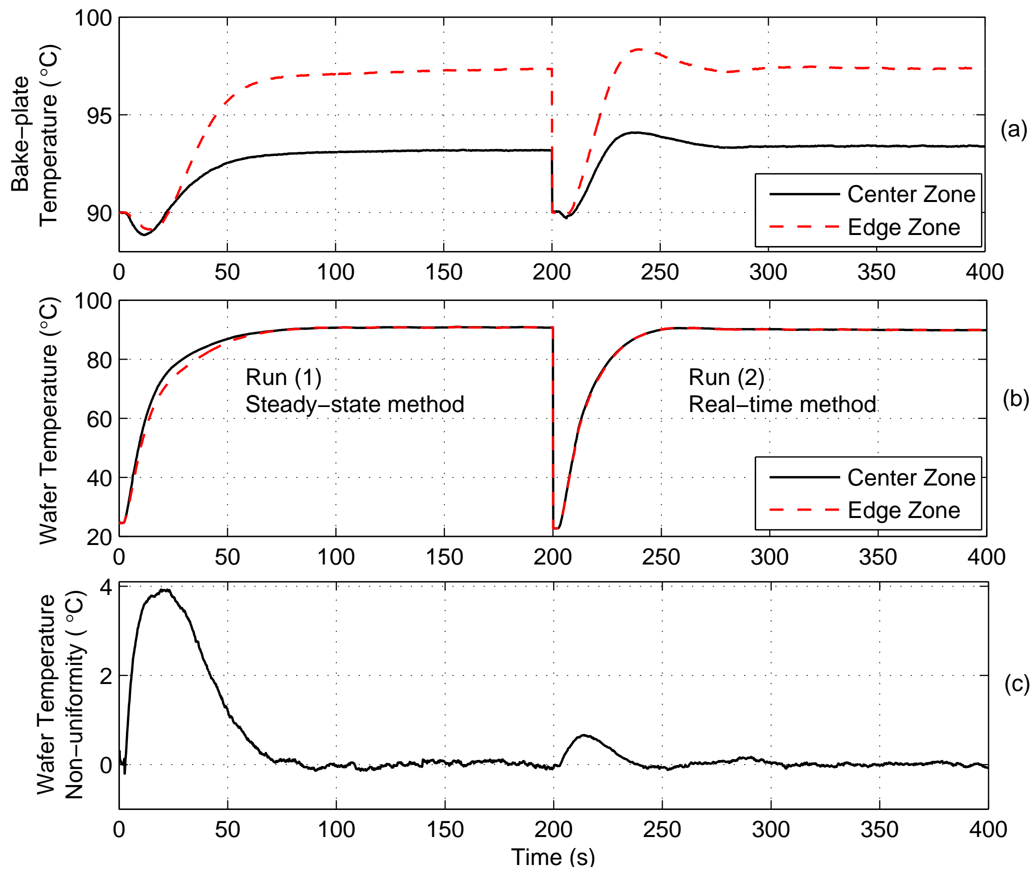


Figure 2.7. Temperature profile of bake-plate and wafer when a flat wafer is dropped on bake-plate with proximity pin height 210μm. The bake-plate temperatures, wafer temperatures and wafer temperature non-uniformity during the baking process are shown in subplots (a), (b) and (c) respectively.

50 seconds with the maximum temperature nonuniformity less than 1°C during the transient and steady-state temperature nonuniformity less than 0.1°C. The corresponding maximum temperature nonuniformity and root mean square (RMS) error during the thermal processing for experimental runs (1) and (2) are also shown in Table 2.3. It can be seen that the temperature nonuniformity RMS in the heating process is decreased form 1.4806°C to 0.1842°C, an improvement of over 80%.

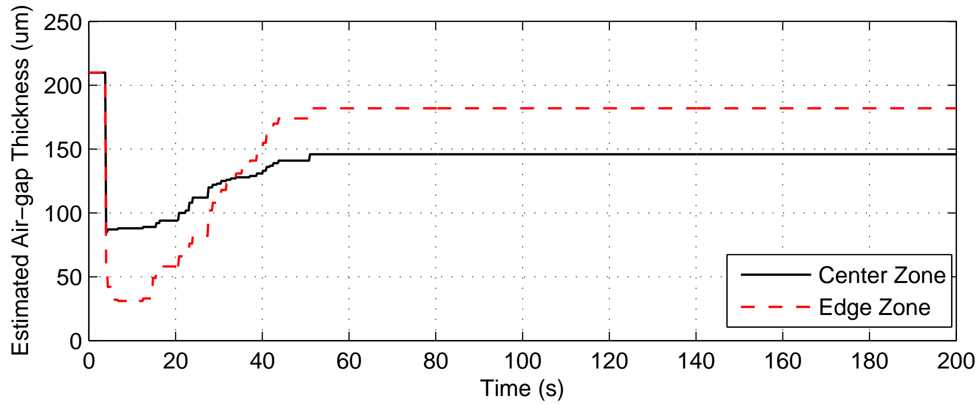


Figure 2.8. Estimated air-gap thickness using real-time control method when a wafer with center-to-edge warpage of 70μm is dropped on bake-plate with proximity pin height of 210μm.

The feasibility of the approach is further demonstrated by heating warped wafer. Firstly, the wafer with center-to-edge warpage of 70μm is dropped on the same bake-plate with the proximity pin height of 210μm. Wafer warpage is created mechanically as shown in Figure 2.2. The corresponding estimated air-gap thickness is plotted in Figure 2.8 and tabulated in Table 2.2. Based on the final estimated air-gap thickness together with the proximity pin height, the profile of the wafer can be obtained by extrapolation as shown in Figure 2.12. An estimated warpage of 72μm from center-to-edge for the warped wafer is obtained which is close to the

known warpage of 70μm.

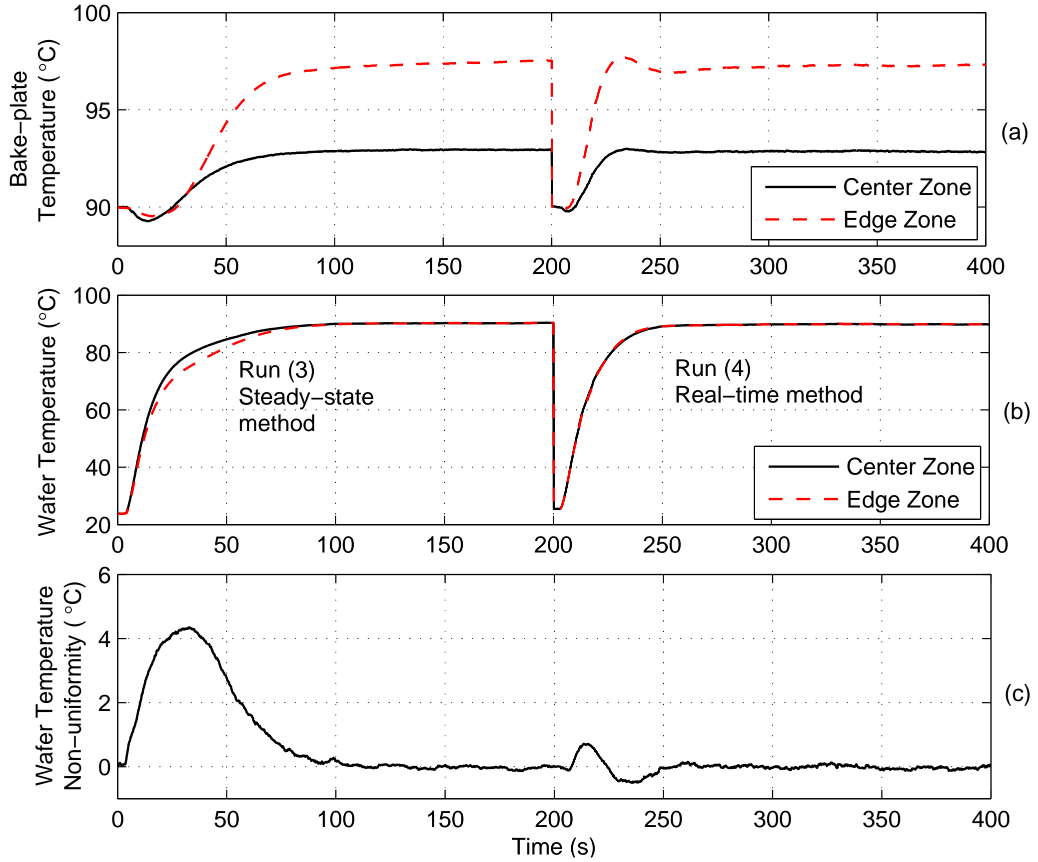


Figure 2.9. Temperature profile of bake-plate and wafer when a wafer with center-to-edge warpage of 70μm is dropped on bake-plate with proximity pin height of 210μm. The bake-plate temperatures, wafer temperatures and wafer temperature non-uniformity during the baking process are shown in subplots (a), (b) and (c) respectively.

The temperature results using the steady-state and real-time control methods are tabulated in Table 2.3 and shown in Figure 2.9 experimental run (3) and run (4). It can be seen that for the warped wafer, using the real-time control method, wafer temperature can reach the steady-state temperature within 50 seconds, with a maximum temperature nonuniformity less than 1°C during the transient and steady-state temperature nonuniformity less than 0.1°C.

Then, the wafer with center-to-edge warpage of 140μm is dropped on the same

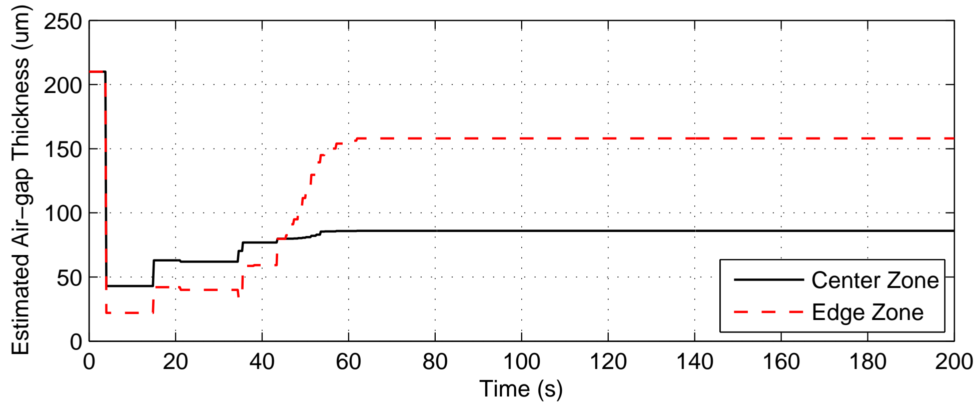


Figure 2.10. Estimated air-gap thickness using real-time control method when a wafer with center-to-edge warpage of 140μm is dropped on bake-plate with proximity pin height of 210μm.

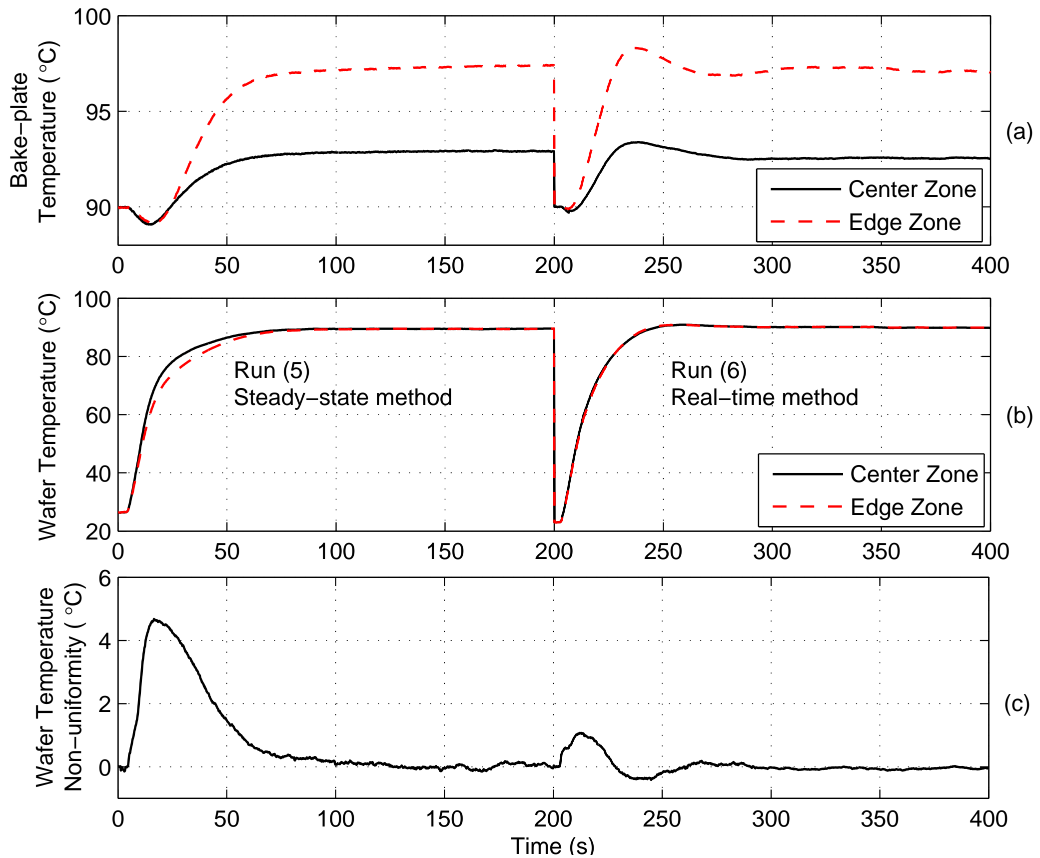


Figure 2.11. Temperature profile of bake-plate and wafer when a wafer with center-to-edge warpage of 140μm is dropped on bake-plate with proximity pin height of 210μm. The bake-plate temperatures, wafer temperatures and wafer temperature non-uniformity during the baking process are shown in subplots (a), (b) and (c) respectively.

Table 2.2. Estimated air-gap thickness and wafer warpage using the real-time control method with the proximity pin height of 210μm

Wafer	Expt. run	Estimated air-gap		Deviation from pin		Estimated warpage (μm)
		center zone (μm)	edge zone (μm)	center zone (μm)	edge zone (μm)	
Flat wafer	(2)	208	214	2	4	4
70 μm warpage	(4)	146	182	-64	-28	72
140μm warpage	(6)	86	158	-124	-52	144

Table 2.3. Maximum temperature nonuniformity and root mean square (RMS) error during the thermal processing using the steady-state and real-time control method.

Wafer	Method	Expt. run	Maximum nonuniformity (°C)	Nonuniformity RMS (°C)
Flat wafer	Steady-state	(1)	3.92	1.48
	Real-time	(2)	0.66	0.18
70 μm warpage	Steady-state	(3)	4.35	1.78
	Real-time	(4)	0.71	0.19
140μm warpage	Steady-state	(5)	4.68	1.62
	Real-time	(6)	1.07	0.29

bake-plate with the proximity pin height of 210μm to verify the effectiveness of the method in detecting different warped wafer. The estimated air-gap thickness is plotted in Figure 2.10 and tabulated in Table 2.2 and the extracted wafer profile is also shown in Figure 2.12. An estimated warpage is 144μm from center-to-edge which is also close to the known warpage of 140μm.

The corresponding temperature results are tabulated in Table 2.3 and shown in Figure 2.11 experimental run (5) and run (6). As expected, using the real-time control method, the 140μm warped wafer can also reach the steady-state

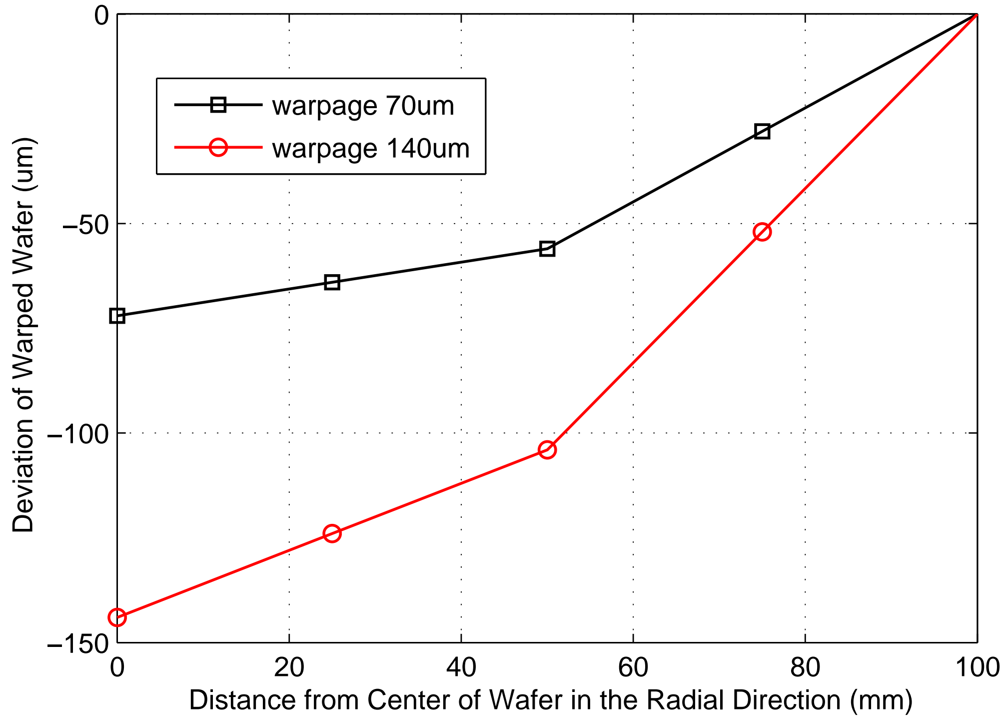


Figure 2.12. Estimated profile of the warped wafers with center-to-edge warpage of 70μm and 140μm based on experimental run (4) and (6) respectively.

temperature within 50 seconds, with much better temperature uniformity than steady-state control method.

2.4 Conclusion

In this chapter, we have demonstrated an in-situ approach to real-time detect wafer warpage and control of the wafer temperature uniformity in baking process. Wafer temperature uniformity in transient period has been improved greatly compared to the previous steady-state method. With the proposed approach, the wafer spatial temperature uniformity in the whole baking process achieved an improvement of more than 80% when compared to the existing steady-state control method. The

proposed approach can also be scaled up for larger wafers by increasing the number of sensors, actuators, and controllers.

Chapter 3

Programmable Integrated Bake/Chill System

3.1 Introduction

In Chapter 2, we have proposed an in-situ approach to real-time detect wafer warpage and wafer temperature by monitoring the bake-plate temperature in baking process. We also demonstrated experimentally that the wafer transient temperature uniformity can be improved greatly using the proposed control method. However, in conventional resist processing, after the baking step, the wafer will then be mechanically moved to a fixed temperature chill-plate where it is cooled to a temperature between 18°C and 30°C [33] as shown in Figure 3.1. Thus, the uncontrolled and non-uniform temperature fluctuation during the mechanical transfer of the substrates from the bake to chill plates will result in spatial temperature

non-uniformities during the entire thermal cycle [13], [38]. Moreover, constrained by the inherent sluggish dynamic response of the conventional bake-plate, the wafer temperature response is not fast enough in the transient period.

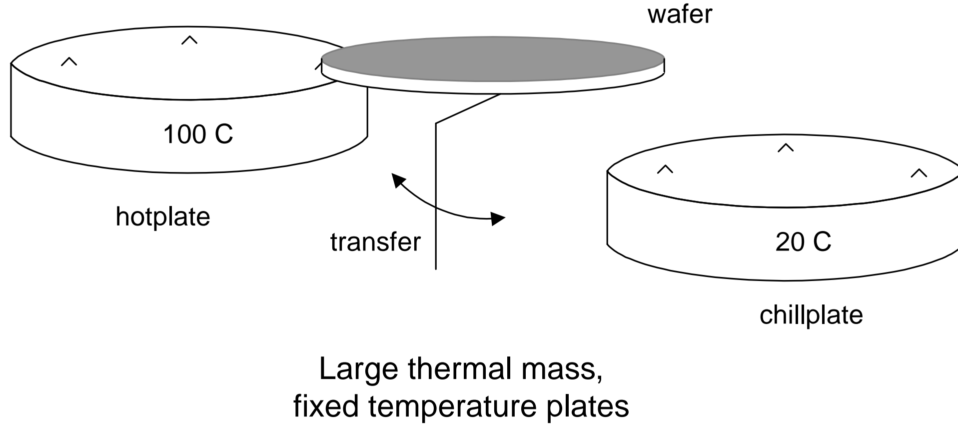


Figure 3.1. The conventional approach for lithography baking and chilling involves substrate transfer between large thermal mass, fixed temperature plates [38].

To deal with the problems, in this chapter, we propose an integrated bake/chill system to provide fast dynamic response and achieve spatial temperature uniformity of a silicon wafer throughout the entire processing temperature cycle of ramp, hold and quench. In the proposed system, a set of thermoelectric devices is employed to provide spatial and temporal temperature uniformity control. The TEDs sit on the surface of a heat sink and together forming an active cooling system so that we completely eliminate substrate movement and the attendant temperature uncontrollability between the baking and chilling processes.

In this work, a mathematical model of the system is developed via detailed modeling and simulations based on first principle heat transfer analysis to ascertain the performance of the proposed design. To improve the temperature uniformity in the process, we propose a model based control method using the dynamic model iden-

tified the by injecting two independent pseudo-random-binary sequence (PRBS) to the system.

This chapter is organized as follows. In Section 3.2, the proposed integrated bake/chill thermal processing system is illustrated. The thermal modeling of the system is presented in Section 3.3 and the effectiveness of the model is verified in Section 3.4. In Section 3.5, the model-based controller is designed to achieve temperature uniformity in the thermal process. Experimental results are given in Section 3.6 to demonstrate the effectiveness of the proposed method. Finally, conclusions are given in Section 3.7.

3.2 Proposed Thermal Processing Model

The schematic of the proposed thermal processing system is shown in Figure 3.2 (A). In this system, wafer sits on an array of proximity pins and is set approximately 5mils above the TEDs. These proximity pins can be embedded with "S102404" thin film RTD (class B) sensors from Minco Corporation [56] to provide in-situ temperature measurement. The "HOT2.0-65-F2A" TEDs from Melcor Corporation [57] are attached to the top of a heat sink via carbon film and integrally form the cooling system. Figure 3.2 (B) depicts the plan view of the heat sink.

The photograph of the prototype two-zone system is shown in Figure 3.3. Two RTD sensors are positioned on the 2-inch wafer to monitor the temperature of the two zones. The TEDs are grouped into 2 pseudo-circular zones and their behaviors

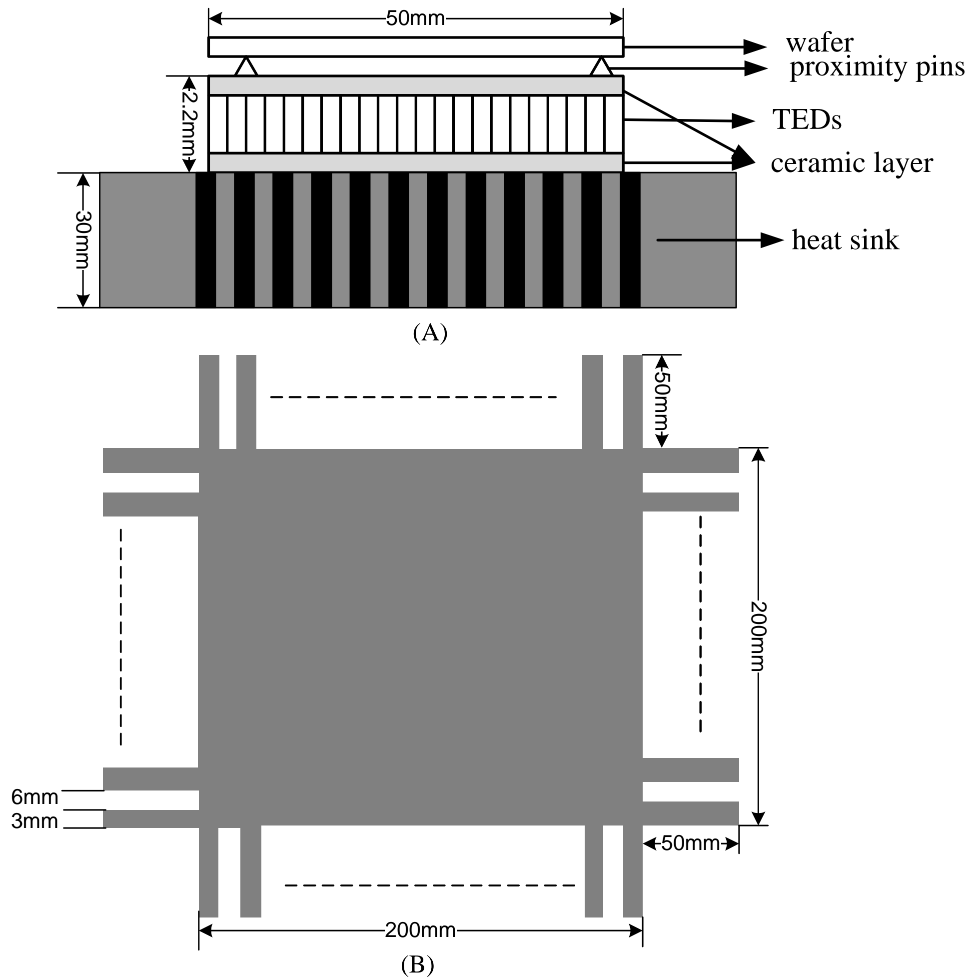


Figure 3.2. Schematic diagram of the integrated bake/chill design. (A) schematic drawing of the system, (B) plan view of the heat sink. (Note: Figures are not drawn to scale).

are dictated by the calculated control signal to provide the desired heating and cooling processes and maintain temperature uniformity. In each zone, all TEDs are powered identically and one temperature sensor is chosen to represent the temperature of the zone.

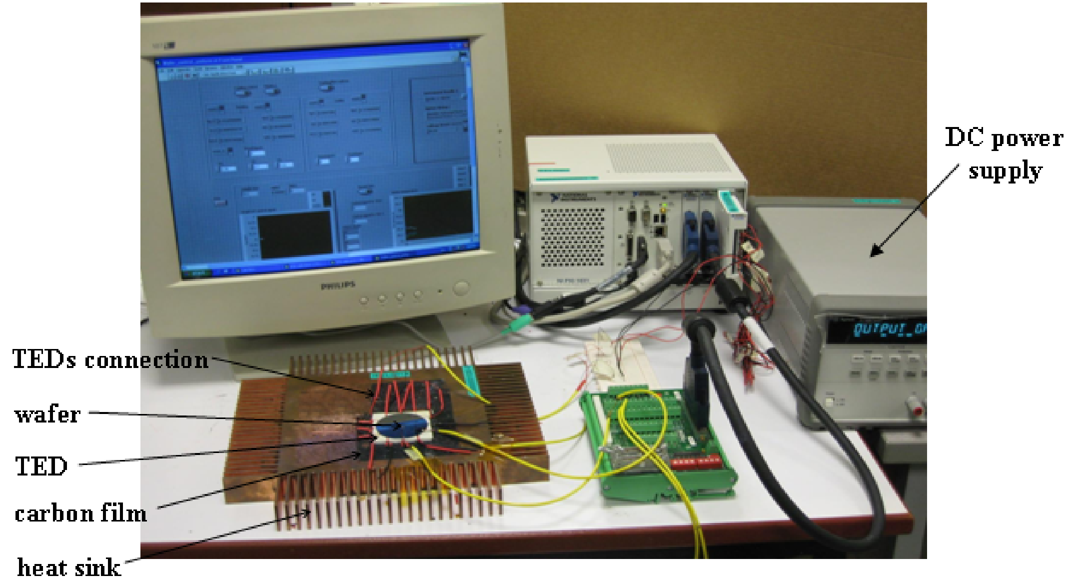


Figure 3.3. Photograph of the experimental setup.

3.3 Thermal Modeling of the System

To ascertain the performance of the proposed design, a mathematical model is developed for the integrated bake/chill operation. The system consists of three main components: the wafer, the TEDs and the heat sink. The wafer is assumed to be perfectly cylindrical with a diameter 50mm. The TEDs employed in the system have length L_T and width W_T that satisfy $L_T = W_T = 13.2$mm. The TEDs' bottom side is attached to a passive heat sink that dissipates heat through natural convection. Referring to Figure 3.2 (A), some TEDs disposed at the edge of the wafer are exposed to the surroundings and epoxy is used to insulate those exposed surfaces. We will next consider the governing thermal equations for the essential components in the system.

3.3.1 Heat Transfer in Wafer

A typical 2-inch wafer thickness is 0.350mm. This is sufficiently thin to consider a uniform temperature across the thickness of the wafer. Considering both heat conduction and convection, we invoke a two-dimensional transient heat diffusion equation and adopt a finite-difference numerical technique. The whole wafer is discretized into several elements for analysis and each element's size is constrained by the physical size of TED. For each wafer element (i, j) in Figure 3.4, we have

$$\rho v_{i,j} c_v \frac{\partial T_w}{\partial t} = q_{i,j}^{up} + q_{i,j}^{down} + q_{i,j}^{left} + q_{i,j}^{right} + q_{i,j}^{top} + q_{i,j}^{bottom} + q_{i,j}^{conv} \tag{3.1}$$

where $q_{i,j}^{up}, q_{i,j}^{down}, q_{i,j}^{left}, q_{i,j}^{right}, q_{i,j}^{top}$ and $q_{i,j}^{bottom}$ are respectively the heat flow into the (i, j) wafer element from the $(i, j + 1), (i, j - 1), (i - 1, j), (i + 1, j)$ element, air on top and below the (i, j) element, $q_{i,j}^{conv}$ is relevant to elements at the edge of the wafer and refers to the heat flow into the element from the side surface via convection. To calculate $q_{i,j}^{up}, q_{i,j}^{down}, q_{i,j}^{left}$ and $q_{i,j}^{right}$ correctly, we need to ascertain the centroidal location $(C_x, C_y\ )$ of each element and its contact areas with the adjacent zones ($A_{i,j}^{up}, A_{i,j}^{down}, A_{i,j}^{left}$ and $A_{i,j}^{right}$). (Refer to Appendix A2)

Accordingly we have

$$q_{i,j}^{up} = kA_{i,j}^{up} \frac{T_{i,j+1} - T_{i,j}}{C_{y(i,j+1)} - C_{y(i,j)}},$$

$$q_{i,j}^{down} = kA_{i,j}^{down} \frac{T_{i,j-1} - T_{i,j}}{C_{y(i,j)} - C_{y(i,j-1)}},$$

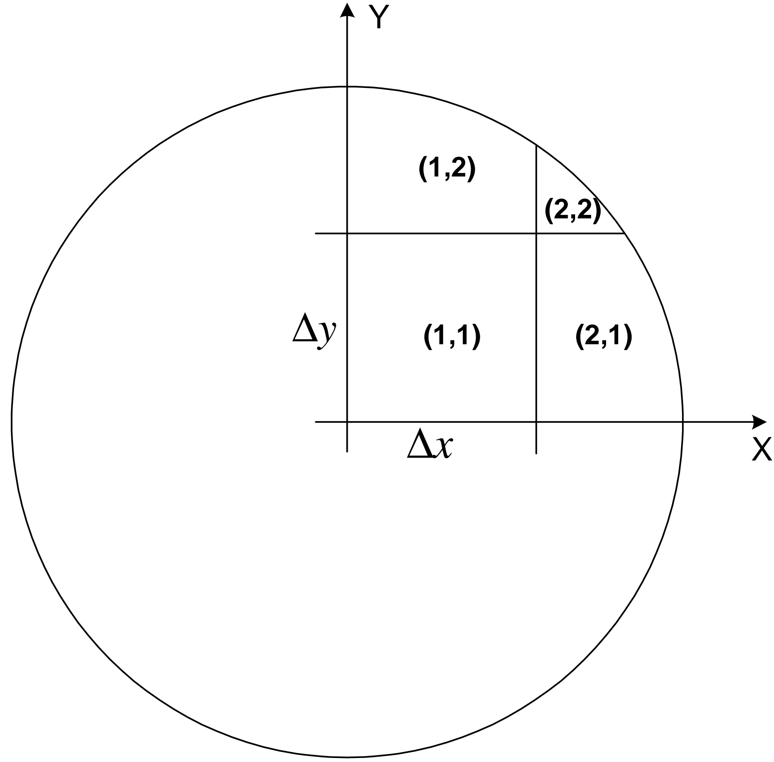


Figure 3.4. Illustration of wafer discretization in system modeling

$$q_{i,j}^{left} = kA_{i,j}^{left}\frac{T_{i-1,j} - T_{i,j}}{C_{x(i,j)} - C_{x(i-1,j)}},$$
$$q_{i,j}^{right} = kA_{i,j}^{right}\frac{T_{i+1,j} - T_{i,j}}{C_{x(i+1,j)} - C_{x(i,j)}} \quad (3.2)$$

The wafer's top surface is exposed to the surroundings and so we have

$$q_{i,j}^{top} = hA_{i,j}^{top}(T_{am} - T_{w(i,j)}) \quad (3.3)$$

where h is the convective heat transfer coefficient over the exposed area $A_{i,j}^{top}$ of element (i,j) and the subscript am denotes the ambient air.

The air-gap between the wafer and the TED is 5mils. Since it is much less than 5.8mm, and their temperature difference is considerably smaller than 200°C [53],

the heat transfer mechanism is essentially conductive and given by

$$q^{bottom} = -k_{ag} A_{ag} \left. \frac{\partial T_{ag}}{\partial z_{ag}} \right|_{boundary} \tag{3.4}$$

The convective heat transfer between each element (i, j) of wafer and surrounding air is given by

$$q_{i,j}^{conv} = hAs_{(i,j)}(T_{am} - T_{w(i,j)}) \tag{3.5}$$

where $A_{s(i,j)}$ is the side surface area of the edge element. The geometry of the curvature at the edge has been fully accounted for in the above equation.

3.3.2 Thermoelectric Devices Modeling

Referring to Figure 3.5, a thermoelectric device is composed of different layers of material with different properties, including ceramic layers, metal films and thermoelectric elements. The metal film is sandwiched between thermoelectric elements and the ceramic substrates. The Peltier, Seebeck, Thomson and Joulean effects are the governing principles of thermoelectricity. For bismuth telluride, the Thomson effect is insignificant so it is neglected in the simulation [58]. Consequently, the governing thermal transport in the semiconductor arms is given by [59]

$$\rho_t c_{v,t} \frac{\partial T_t}{\partial t} = k_t \frac{\partial^2 T_t}{\partial z_t^2} + \frac{J^2}{\sigma_t} \tag{3.6}$$

where σ is the electrical conductivity, $J(= I/A)$ the current flux where I and A are respectively the direct current flowing through the TEDs and the cross-sectional area. The subscript t denotes the thermoelectric modules.

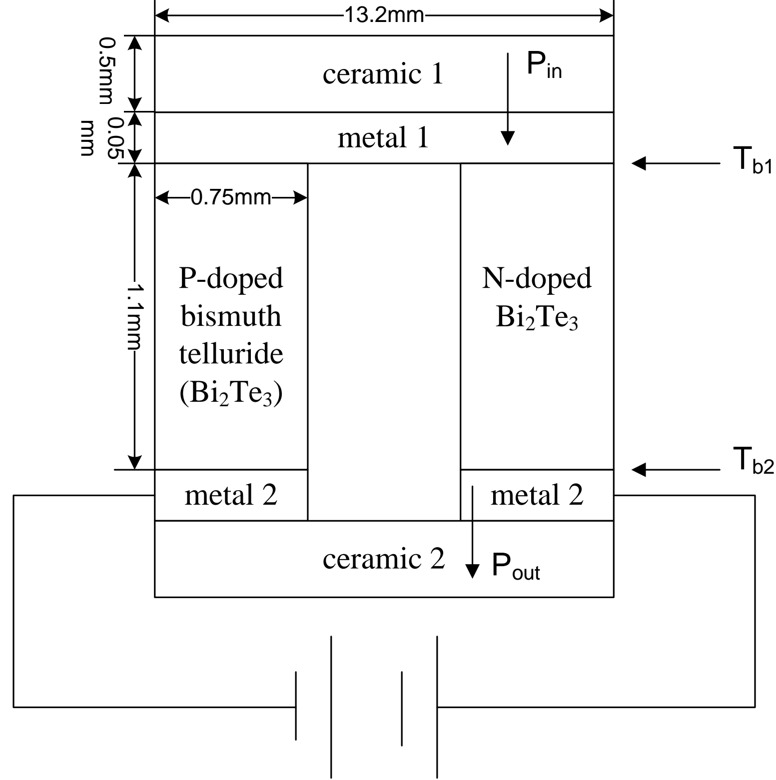


Figure 3.5. Schematic diagram of a thermoelectric element. (Note: Figure is not drawn to scale)

The Peltier effect is manifested at the boundary between the TED's metal contacts and the thermoelectric elements. It is given by:

$$k_t A_t \frac{\partial T_t}{\partial z_t} + k_m A_m \frac{\partial T_m}{\partial z_m} \pm \alpha I T_{bd} = 0 \tag{3.7}$$

where α is the Seebeck coefficient and the subscripts m and bd denotes the metal film contacts in the TEDs and the boundary layer respectively. The first two temperature gradient terms denote the temperature gradient from the boundary

to the corresponding materials. The last term denotes the Peltier effect at the boundary. The sign in the last term in Equation 3.7 is positive in heating mode and negative in chilling mode. The thermal transport phenomenon in the metal film element is similarly expressed as

$$\rho_m c_{v,m} \frac{\partial T_m}{\partial t} = k_m \frac{\partial^2 T_m}{\partial z_m^2} + \frac{J^2}{\sigma_m} \tag{3.8}$$

The governing thermal transport equation of the ceramic substrate is

$$\rho_{ce} c_{v,ce} \frac{\partial T_{ce}}{\partial t} = k_{ce} \frac{\partial^2 T_{ce}}{\partial z_{ce}^2} \tag{3.9}$$

where the subscripts ce denotes the ceramic substrate.

The boundary heat transfer equation at the interfaces between ceramic and metallization of a TED is expressed below as a mixed boundary condition:

$$-k_a A_{ce} \left. \frac{\partial T_{ce}}{\partial z_{ce}} \right|_{boundary} = -k_m A_m \left. \frac{\partial T_m}{\partial z_m} \right|_{boundary} \tag{3.10}$$

The electricity power consumed by each TED zone can be computed via an energy balance as

$$P_{electricity} = [P_{out} - P_{in} + \triangle P + 2\alpha \times I \times (T_{b1} - T_{b2})]N \tag{3.11}$$

where $P_{out} = -k_m A_m \frac{\partial T_{m2}}{\partial z_{m2}}$, is the energy transferred from metal2 to ceramic2;

$P_{in} = -k_{ce}A_{ce}\frac{\partial T_{ce1}}{\partial z_{ce1}}$, the energy transferred from ceramic1 to metal1; $\triangle P = \sum_i \int_{vi} \rho_i c_{v,i}\frac{\partial T_i}{\partial t}dv_i$, the rate of change of internal energy, i stands for metal1, metal2 or TED; N is the number of pairs of TED arms in a particular zone and T_{b1}, T_{b2} are the respective metal-ceramic boundary temperatures.

3.3.3 Heat Sink Design

During the cooling process, heat absorbed at the cold junction of TEDs is pumped to the hot junction at a rate proportional to the current passing through the circuit. At the hot junction, the absorbed energy needs to be dissipated via a heat dissipating device. To meet this target, a heat sink with extended fins is designed.

The heat sink is shown in Figure 3.2 (B). It is a copper plate with fins on the top and four sides. The length and width of the heat sink are 300mm. The fins are 50mm in length and 3mm in width and the fin spacing is 6mm.

1. Heat transfer from the fins

The convective heat transfer coefficient, $h_{a,f}$ for the fins can be calculated from [52] as

$$h_{a,f} = \frac{k}{S}\overline{Nu}_s \tag{3.12}$$

where the Nusselt number is $\overline{Nu}_s = [\frac{C_1}{(Ra_s S/L)^2} + \frac{C_2}{(Ra_s S/L)^2}]^{-\frac{1}{2}}$ [60], and S is the space distance between fins.

2. Heat transfer from the top surface

For the upper surface of the heat sink, the convective heat coefficient, $h_{a,s}$ can be calculated from [52] as

$$h_{a,s} = \frac{k}{L}\overline{Nu_L} \tag{3.13}$$

where $\overline{Nu_L} = 0.54Ra_L^{1/4}$.

On account of the thermal conductivity of copper in relation to the convective heat transfer coefficients, we assign the heat sink with a uniform temperature. The governing thermal equation of the heat sink is accordingly expressed as

$$\rho_{hs}c_{v,hs}\frac{\partial T_{hs}}{\partial t} = k_{ce}A_{ce}\frac{T_{ce} - T_{hs}}{Z_{ce}/2} + (\eta_0 \times h_{a,f}A_{a,f} + h_{a,s}A_{a,s})(T_{ambient} - T_{hs}) \tag{3.14}$$

where η_0 is the fin efficiency of the heat sink and the subscript hs denotes heat sink.

The fins on the heat sink can be designed a priori from the following considerations. The heat that is to be dissipated stems from:

1. cooling the wafer at -3°C/s:

$$P_w = \frac{\partial T_w}{\partial t}\rho_w c_{v,w} V_w \tag{3.15}$$

2. TED power consumption: $P_{electricity}$

Designing for a heat sink equilibrium temperature $T_{hs,E}$ = 60°C, we require the

convection heat transfer coefficient of the designed heat sink to satisfy

$$t_{cd} \times (P_w + P_{electricity}) \leq t_{cc} \times (\eta_0 \times h_{a,f}A_{a,f} + h_{a,s}A_{a,s}) \times (T_{hs,E} - T_{ambient}) \quad (3.16)$$

where t_{cd} is the time needed to cool wafer from 100°C to room temperature and t_{cc} is the time period of the cooling cycle.

With the thermal model of all of the components, simulations can be carried out to assess the performance of the proposed thermal processing system. Table 3.1 lists the values or the correlations used for all the parameters [54], [59] in the model.

Simulations show that the designed heat sink would equilibrate at $T_{hs,E} \approx$ 57.5°C after several consecutive thermal cycles. So the heat sink can dissipate heat effectively and will stabilize at the intended temperature.

3.4 Open Loop Model Validation

To assess the quality of the proposed system model, we perform open loop experiments and compare the simulation with the experimental results. Our objective is to demonstrate that the proposed model succeeds in predicting the experimental wafer temperatures using the same input signal without resorting to the use of any fitting parameter and is therefore useful for scaling up. Firstly the TED surface temperature is monitored under the condition of fixed input current in a heating-and-cooling cycle. Figure 3.6 shows the comparison of the experimental

Table 3.1. Physical parameters of the integrated bake/chill thermal processing system [54], [59].

	Property	Value
Wafer (silicon)	ρ	2330kgm^{-3}
	c_v	$750\text{JK}^{-1}\text{kg}^{-1}$
	k	$99\text{Wm}^{-1}\text{K}^{-1}$
	z	0.350mm
Air	ρ	1.293kgm^{-3}
	c_v	$1000\text{JK}^{-1}\text{kg}^{-1}$
	k	$0.025\text{Wm}^{-1}\text{K}^{-1}$
	h	$10\text{Wm}^{-2}\text{K}^{-1}$
	$h_{a,f}$	$6.5\text{Wm}^{-2}\text{K}^{-1}$
	$h_{a,s}$	$6.0\text{Wm}^{-2}\text{K}^{-1}$
Ceramic	ρ	3110kgm^{-3}
	c_v	$375\text{JK}^{-1}\text{kg}^{-1}$
	k	$36\text{Wm}^{-1}\text{K}^{-1}$
Metal contact (copper)	ρ	8933kgm^{-3}
	c_v	$385\text{JK}^{-1}\text{kg}^{-1}$
	k	$401\text{Wm}^{-1}\text{K}^{-1}$
Thermoelectric devices[a]	ρ	7534kgm^{-3}
	c_v	$554\text{JK}^{-1}\text{kg}^{-1}$
	k	$1.5\text{Wm}^{-1}\text{K}^{-1}$
	α	$(22224 + 930T - 0.9905T^2) \times 10^{-9}\text{VK}^{-1}$
	R	$(5112 + 163.4T - 0.6279T^2) \times 10^{-10}\Omega\text{m}$
Heat sink (copper)	ρ	8933kgm^{-3}
	c_v	$385\text{JK}^{-1}\text{kg}^{-1}$
	k	$401\text{Wm}^{-1}\text{K}^{-1}$
	η_0	0.99
RTD sensor	τ	1.2s

[a] In the computation of the Seebeck coefficient, α, and electrical resistivity, R, the temperature, T, is the average temperature of the hot and cold junctions of the TED [57].

and simulated results in the process. Figure 3.6 (A) shows the experimental and simulated TED temperatures. Figure 3.6 (B) presents the difference between experimental and simulation results, and Figure 3.6 (C) features the input currents during the process. It can be seen that the simulation and experimental TED tem-

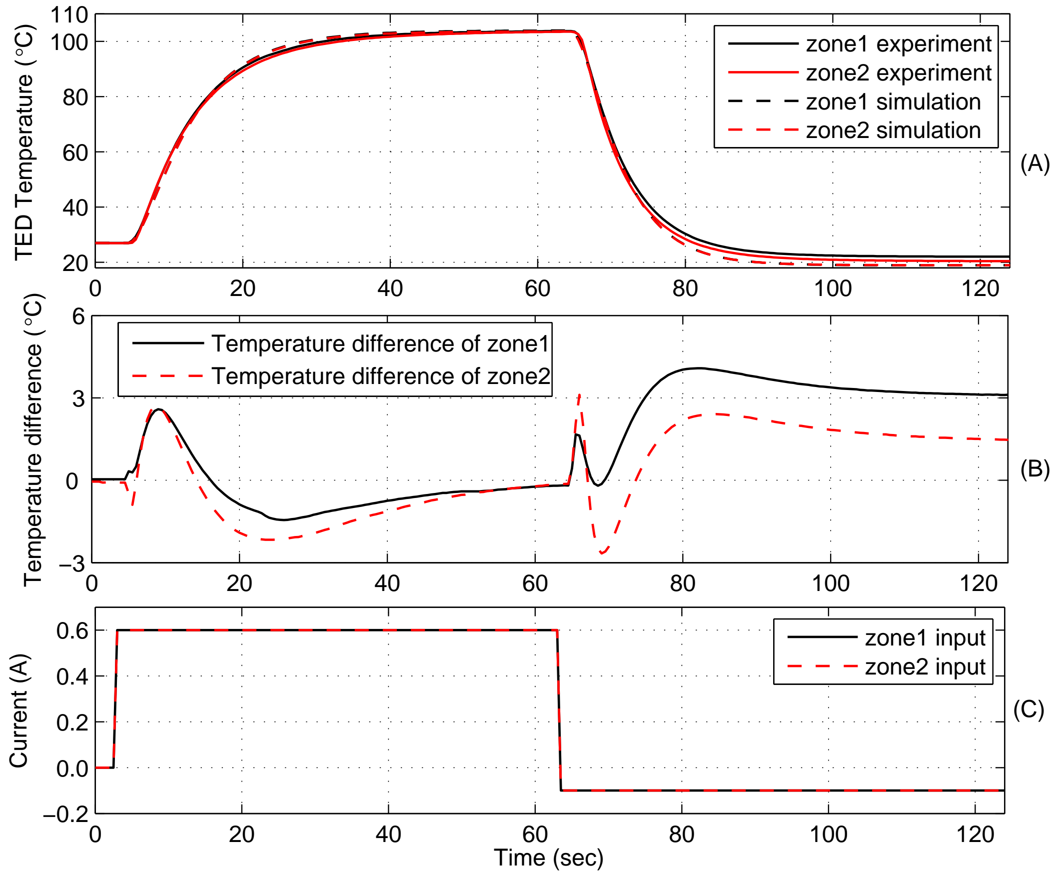


Figure 3.6. Comparison of experimental and simulated TED temperatures in a heating and cooling cycle. (A) experimental and simulated TED temperature response, the solid line shows the experimental zone1 and zone2 TED temperatures and the dashed line shows the simulated zone1 and zone2 TED temperatures, (B) TED temperature difference between experiment and simulation, the solid line shows the temperature difference of zone1 and the dashed line shows the temperature difference of zone2, (C) input currents during the process.

perature can match very well with fixed input signals in both heating and cooling processes, which verify the effectiveness of the thermal modeling in simulating the TED surface temperature.

With the satisfactory agreement achieved for the TED surface temperature, we next investigate the effectiveness of the model to predict the wafer temperature. We generate a series of different input steps that range from -0.15A to 0.65A to test the validity of the system model. Each step is held long enough, e.g. 1

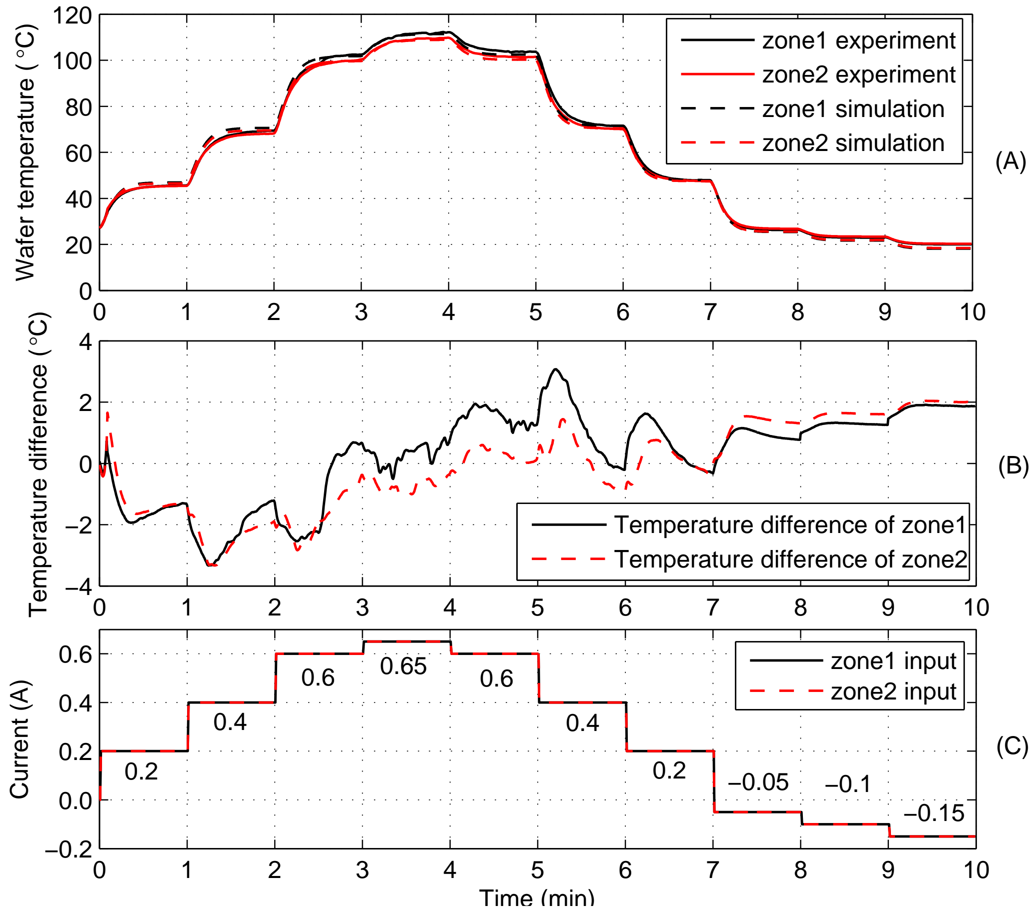


Figure 3.7. Comparison of experimental and simulated wafer temperatures at different input signals. (A) experimental and simulated wafer temperature response, the solid line shows the experimental zone1 and zone2 wafer temperatures and the dashed line shows the simulated zone1 and zone2 wafer temperatures, (B) wafer temperature difference between experiment and simulation, the solid line shows the temperature difference of zone1 and the dashed line shows the temperature difference of zone2, (C) input currents during the process.

minute, for the temperatures to approach steady-state. The comparison of the experimental and simulation results is shown in Figure 3.7. Figure 3.7 (A) shows the experimental and simulated wafer temperatures. Figure 3.7 (B) presents the difference between experiment and simulation results, and Figure 3.7 (C) features the input currents during the process. It can be seen that the simulation and experimental wafer temperatures can match very well with different input signals, thereby verifying the effectiveness of the thermal modeling in the event of input

signal changes.

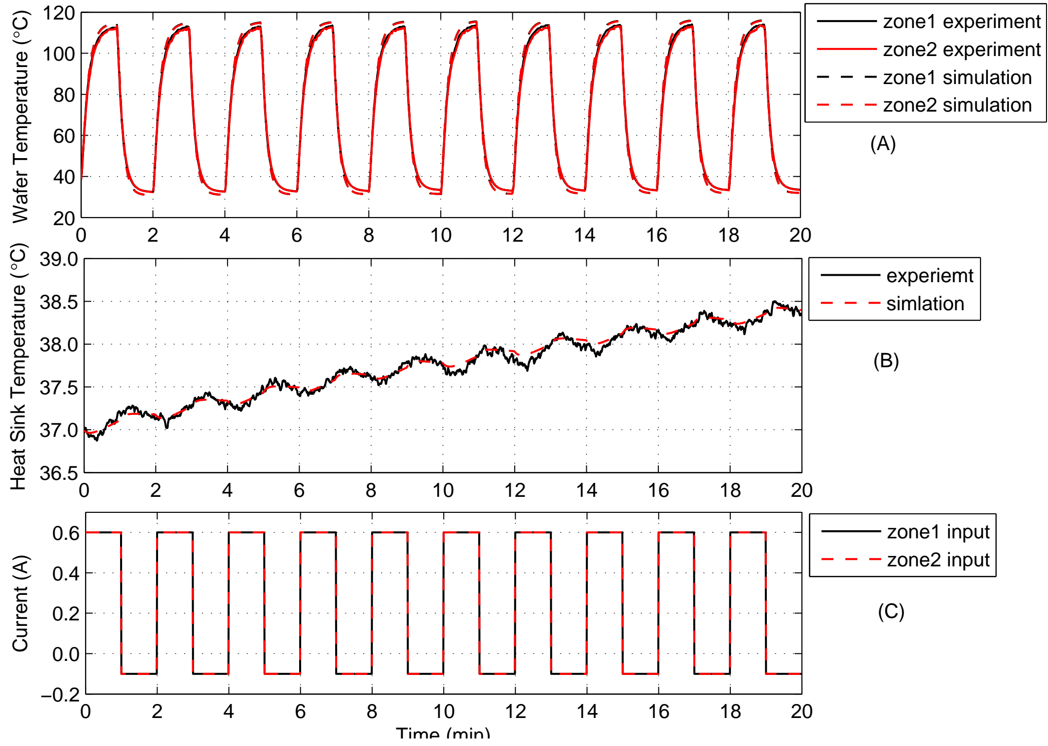


Figure 3.8. Comparison of experimental and simulated wafer temperature over 10 consecutive cycles after the heat sink is saturated. (A) experimental and simulated wafer temperature responses, the solid line shows the zone1 and zone2 wafer temperature in experiment and the dashed line shows the zone1 and zone2 wafer temperature in simulation, (B) experimental and simulated heat sink temperature over the 10 cycles, the solid line shows the heat sink temperature in experiment and the dashed line shows the heat sink temperature in simulation, (C) input currents during the process.

The comparison of the experimental and simulation results over ten successive cycles after the heat sink is saturated is shown in Figure 3.8. Figure 3.8 (A) shows the comparison of experimental and simulated wafer temperatures. It can be seen that the simulated and experimental wafer temperatures agree very well over the entire process and that the system continues to work well over several successive runs after the heat sink is saturated. Figure 3.8 (B) compares the simulated and experimental heat sink temperatures and reveals their close agreement. This confirms that the proposed system can work properly with the designed heat sink even

after the heat sink is saturated. Figure 3.8 (C) records the input currents over the ten successive runs.

3.5 Model Based Controller

With the designed thermal processing system, we will next use it to control wafer temperature in the thermal process. Two objectives are sought from the proposed model based controller. The module should provide the necessary transient and steady-state spatial temperature uniformity, as well as tracking the system set point.

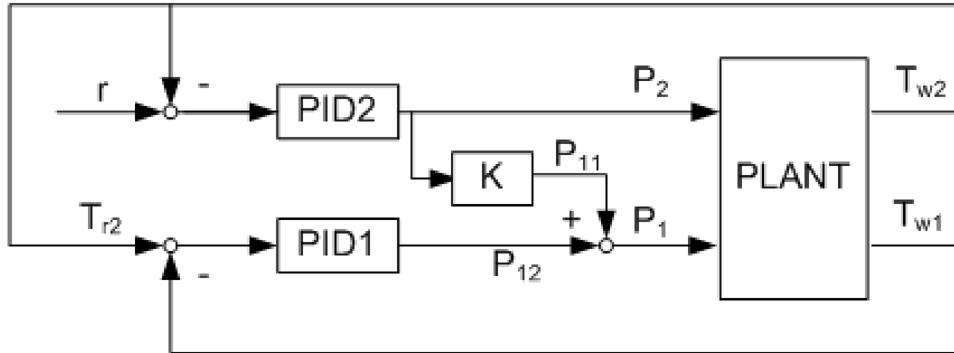


Figure 3.9. Block diagram of the proposed model based control scheme.

The block diagram of the control strategy is shown in Figure 3.9. The outer zone (i.e. at the edge of the wafer) manipulates the wafer edge temperature so that it follows a desired wafer temperature set point. The inner zone (i.e. at the center of the wafer) maintains temperature uniformity by forcing the wafer center temperature to follow that of the edge. The individual controllers used are of the proportional-integral-derivative (PID) type. In order to guarantee the temperature

uniformity in the transient period, the ratio of the two control signals is added to the output of the PID controller of zone1 so as to formulate the control signal of zone1.

Consider the plant described by the following transfer function matrix

$$\begin{bmatrix} T_{w1} \\ T_{w2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} \tag{3.17}$$

where T_{w1} and T_{w2} represent temperature change of wafer's zone1 and zone2 respectively, and P_1 and P_2 represent the current change in TEDs of zone1 and zone2 respectively.

To guarantee the temperature uniformity of the two zones we impose

$$T_{w1} = T_{w2} \tag{3.18}$$

With the system model, this equation can be expressed as

$$G_{11}P_1 + G_{12}P_2 = G_{21}P_1 + G_{22}P_2 \tag{3.19}$$

Thence we can get the ratio of the control signal of the two zones as

$$K = \frac{P_1}{P_2} = \frac{G_{22} - G_{12}}{G_{11} - G_{21}} \tag{3.20}$$

Thus in the control structure shown in Figure 3.9 PID2 is used to formulate P_2 which in turn forces the temperature of zone2 to track the set point. Referring to Figure 3.9, P_{11} is set to KP_2 in order to minimize the temperature difference between the two zones during the transient period. Finally PID1 is used to formulate P_{12} which controls the temperature uniformity in the steady-state. The approach is easily extended to a multi-zone system.

Prior to implementing the control scheme in the thermal processing system, a calibrated model of the prototype system must first be identified experimentally. The model relates the change in wafer temperature to the change in TED current. It is determined by injecting a different set of independent PRBS into each of the two control zones of the TEDs. Using least squares estimation, the process model is identified as

$$\begin{aligned} G_{11} &= \frac{1.482d^{-3}}{1-0.9681d^{-1}} \qquad G_{12} = \frac{0.956d^{-4}}{1-0.9796d^{-1}} \\ G_{21} &= \frac{0.524d^{-6}}{1-0.9625d^{-1}} \qquad G_{22} = \frac{1.101d^{-3}}{1-0.9767d^{-1}} \end{aligned} \tag{3.21}$$

where d represent the backward-shift operator.

The identification results are shown in Figure 3.10. Figure 3.10 (A) shows the modeled and experimental results when the PRBS are injected into the zone1 TEDs. The top subplot shows the zone1 wafer temperature response, and the middle subplot indicates the zone2 wafer temperature response, where the solid line and the dashed line represent experimental and modeled results respectively. It can be seen that the identified model output is sufficiently close to the experimental

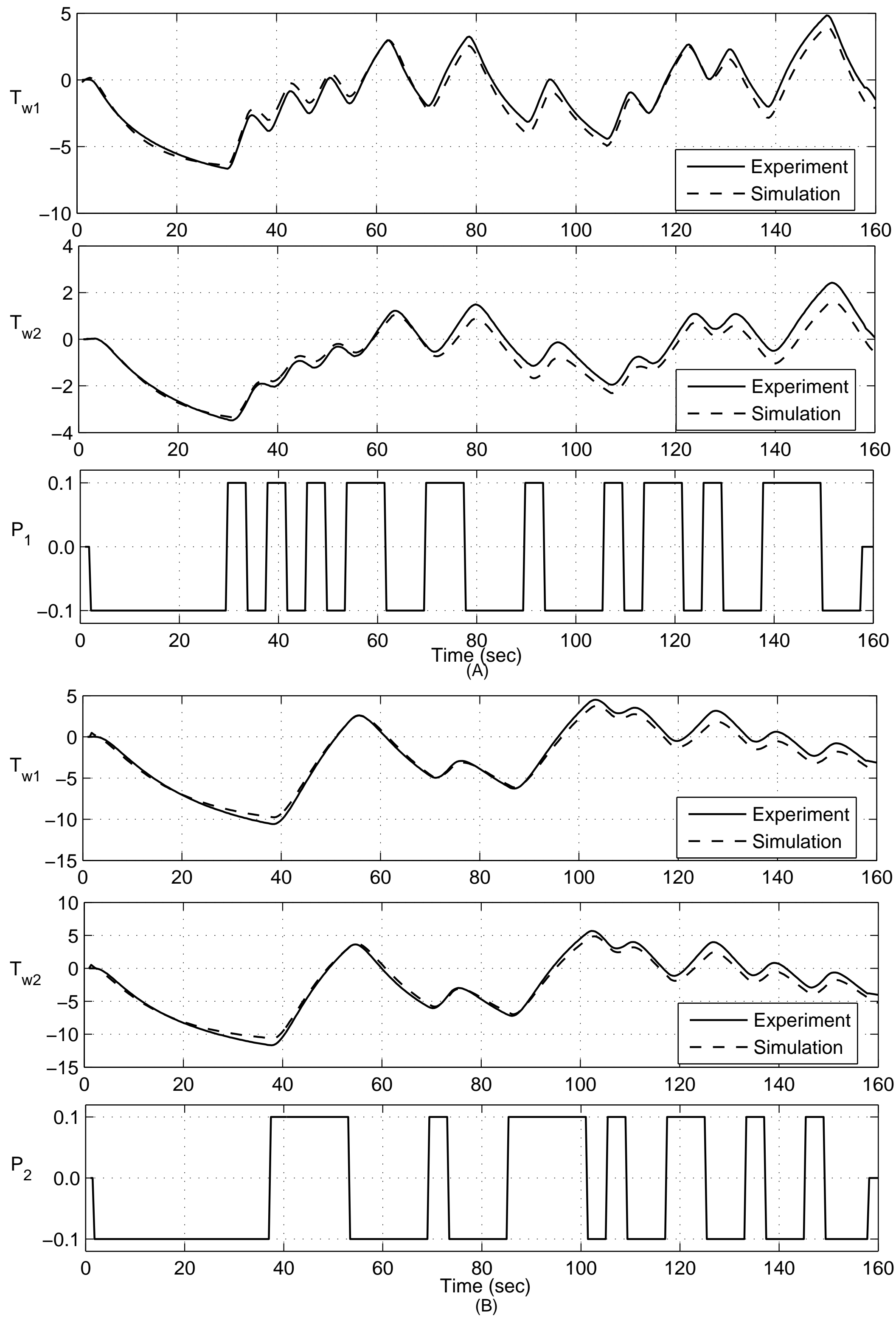


Figure 3.10. System identification result with two independent pseudo-binary random sequences injected into two control zones respectively. The solid line shows the resulting change in wafer temperature in experiment and the dotted line shows the calculated response using the identified model.

wafer temperature response, which shows the accuracy of the identified models. The bottom subplot shows the PRBS input signal of zone1. Figure 3.10 (B) shows the simulation and experimental results when the PRBS is injected into the zone2 TEDs. The top subplot shows the zone1 wafer temperature responses in simulation and experiment, the middle subplot presents the zone2 wafer temperature responses in simulation and experiment, and the bottom subplot indicates the PRBS input signal of zone2. It can be seen that the identified model output is sufficiently close to the experimental result. Thus we can use the identified model to calculate the ratio between the two zones as

$$\begin{aligned} K = \frac{G_{22} - G_{12}}{G_{11} - G_{21}} &= \frac{1.101 - 2.034d^{-1} + 0.934d^{-2}}{1.482 - 1.4301d^{-1} - 0.524d^{-3} + 0.507d^{-4}} \\ &\times \frac{1 - 1.9306d^{-1} + 0.9318d^{-2}}{1 - 1.9563d^{-1} + 0.9568d^{-2}} \end{aligned} \tag{3.22}$$

3.6 Experimental Results

The proposed control scheme is then tested using the identified model. Figure 3.11 shows the results of the computer simulation. In the experiment, the heating set point is set to 90°C and the chilling set point is room temperature. The top plot shows the wafer temperature of center and edge zones during thermal cycle. The middle plot shows the temperature nonuniformity of the wafer. The bottom plot shows the control input. It can be seen that the wafer temperature can rise up to set point in heating process and fall down to room temperature in chilling process fast enough, and in the whole process, the temperature difference between the two

zones is almost zero.

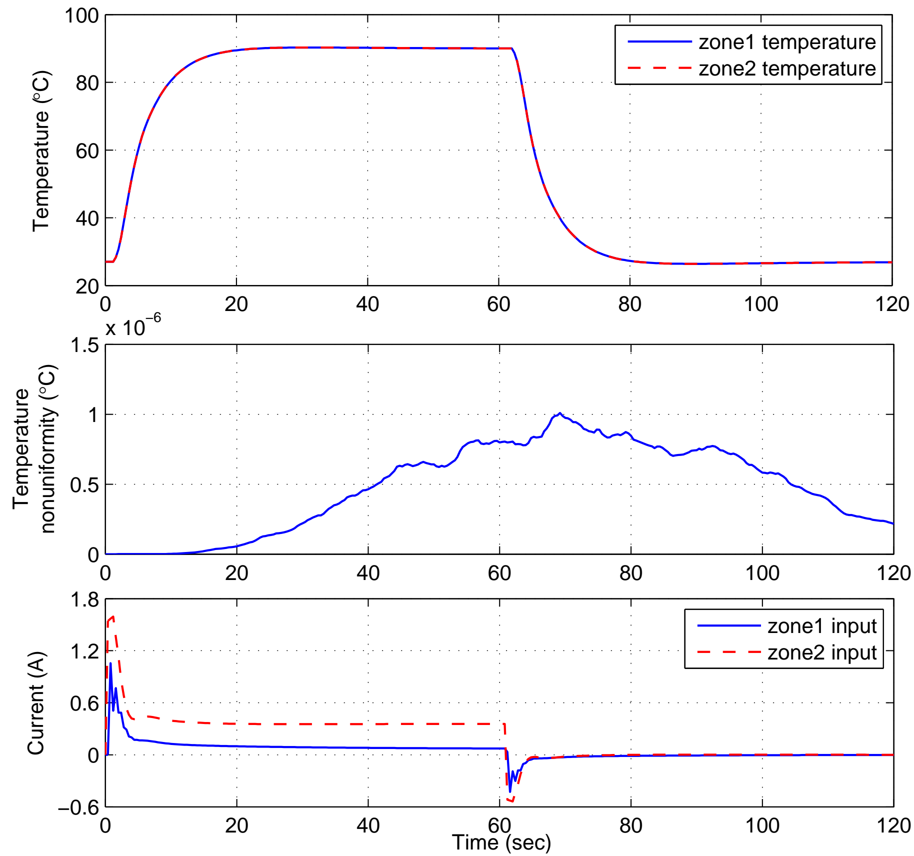


Figure 3.11. Simulation result of the identified system. (A) temporal wafer temperature in the simulation, (B) wafer temperature difference of the control zones during the entire thermal cycle, (C) input current of the TEDs in the two control zones.

Armed with the satisfactory simulation result, experiments demonstrating the operation of our module as an integrated bake/chill unit are then conducted. The temperatures at five judicious locations along a common radius of the wafer are monitored as shown in Figure 3.12. Among the five RTD sensors, R1 and R5 are used as the feedback variables of zone1 and zone2 respectively for the purpose of model based control. R2, R3 and R4 are placed between R1 and R5. R2 is placed on the same TED as R1 in zone1, R4 is located on the same TED as R5 in zone2 and R3 is judiciously positioned above the air strip between the two

TEDs which will expectedly experience the poorest controllability. This sensor arrangement guarantees the wafer spatial temperature uniformity along the radius can be representatively monitored. In the experiment, the baking and chilling set points are chosen to be 90°C and 25°C, respectively. The same unit is capable of baking at higher temperatures, we just choose a typical baking temperature in the thermal process of lithography for demonstration purposes.

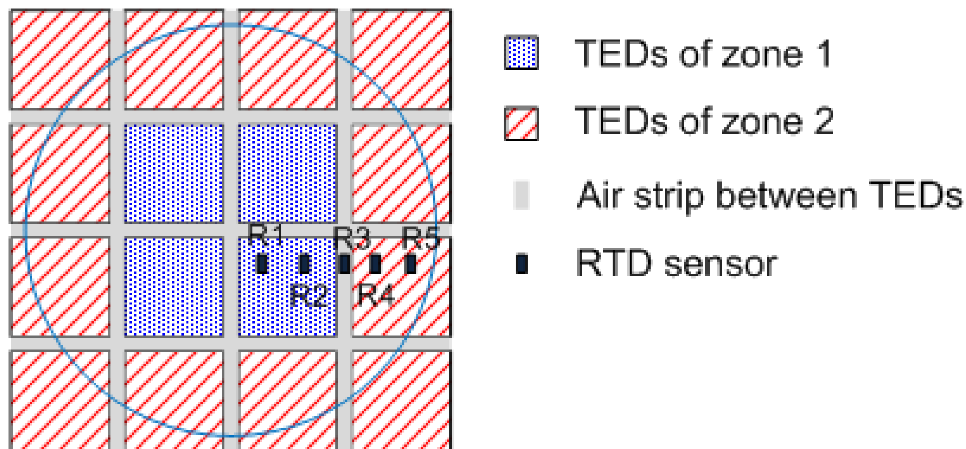


Figure 3.12. Location of temperature sensors for the integrated bake/chill experiment. R1 and R5 are used as feedback variables.

Figure 3.13 shows the experimental result using the model based control method. The subplot (A) shows the five wafer temperatures in the entire cycle. The bake rise and chill fall times are seen to be less than 20 seconds, which is fast enough for the thermal process in lithography. The subplot (B) shows wafer temperature nonuniformity along the radius, defined as the difference between the temperature at any instant and the mean of the five RTD readings. The subplot (C) shows the temperature difference between the two feedback points on the wafer. It can be seen that with the model based control method, the temperature difference is less than 0.1°C in the entire thermal process. Throughout the whole cycle, the nonuni-

formity never deviates beyond $\pm 0.3°C$, and at steady-state it is within $\pm 0.1°C$. In subplot (D) we show the control current input of TEDs in zone1 and zone2 during the thermal cycle respectively. The TEDs current input is positive during the baking process so as to heat the wafer and negative in the cooling process to chill the wafer. In order to impose the fastest rising or falling gradient, the input signal of zone2 saturates during the transient state, whereas the input signal of zone1 oscillates in the transient state to minimize the temperature difference between the two control zones.

Using the proposed thermal processing system and model based control method, the wafer can be heated to a desired temperature and chilled to room temperature with a single, integrated processing system. During the whole process the temperature non-uniformity can be maintained to within $\pm 0.3°C$.

3.7 Conclusion

In this chapter, an integrated bake/chill module for photoresist processing in lithography is presented and implemented. It consists of an array of TEDs to provide real-time dynamic, spatial temperature control and active cooling to the wafer, as well as a heat dissipating device. To achieve the desired wafer temperature uniformity in the whole thermal cycle, we discretize the TEDs into multiple control zones and propose a model based control method. Using the system, the bake and chill processes are integrated into one continual process, the wafer temperature

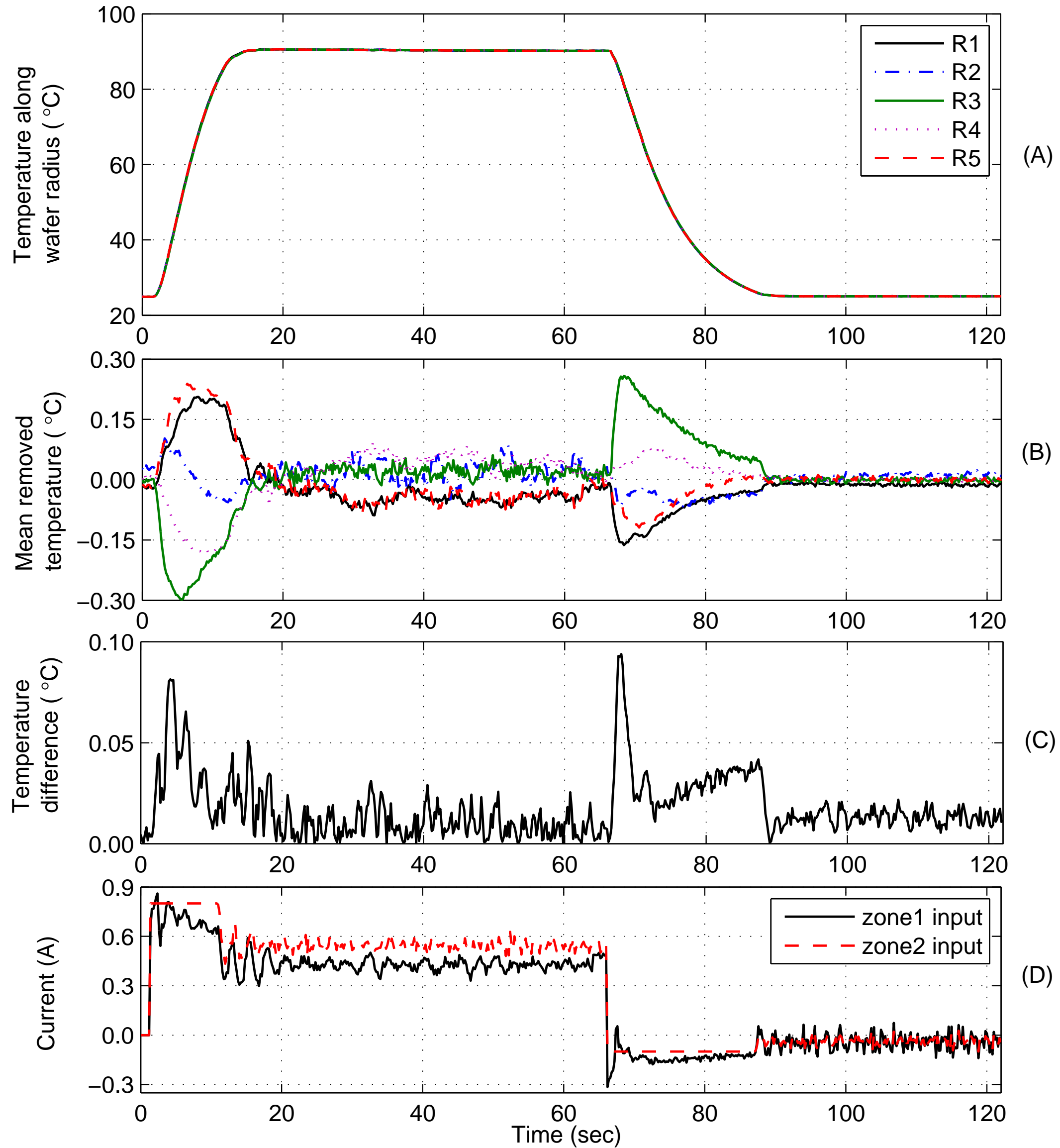


Figure 3.13. Experimental wafer temperature along the wafer radius with the temperatures of sensors R1 and R5 being treated as feedback variables using model based control method. (A) wafer temperature response at the five points during the whole thermal cycle, (B) mean removed wafer temperature of the five points, (C) temperature difference between the two feedback points on the wafer in the process, (D) control current inputs of TEDs during the thermal cycle.

non-uniformity is minimized in the whole thermal cycle, and fast wafer temperature response can be achieved. Experimental results have been presented that demonstrate the effectiveness of the proposed module and control method.

Chapter 4

Beam Size Effect on the Spectroscopic Ellipsometric Measurement Result

4.1 Introduction

Metrology is a key element in maintaining an adequate and affordable process latitude in real-time process control. For tight CD uniformity control in lithography, accurate metrology is needed for characterizing and monitoring the processing states.

Various techniques have been both proposed and implemented for these purposes. Scanning electron microscopes (SEM) and atomic force microscopes (AFM)

can deliver direct images of the patterned features. However, they are very expensive, and can be either time-consuming or destructive, and thus not suitable for real-time monitoring. A number of methods have been proposed for lithography process metrology. Nyyssonen *et al.* [61] presented a monochromatic waveguide model that can predict the optical microscope images of line objects with arbitrary edge geometry. Yuan *et al.* [62] developed a simulator called METRO to obtain more accurate alignment. Jakatdar *et al.* [63] proposed a metrology based on deprotection induced thickness loss (DITL) and Ziger [64] correlated ultraviolet reflectance spectra to the linewidth of *i*-line photoresist. Usually these methods deliver the effective linewidth values. However, the actual CD profile information is needed because it contains information about the overall lithography quality.

To provide an in-situ metrology technique, Niu [65] proposed the specular spectroscopic scatterometer in 1999. The scatterometer provides an accurate, inexpensive, and non-destructive CD metrology solution. Specular spectroscopic scatterometry uses traditional spectroscopic ellipsometers to measure the 0th order diffraction responses of a grating at multiple wavelengths. Given the 0th order diffraction responses, one can then attempt to reconstruct the grating profile.

Spectroscopic ellipsometry is a surface analytical technique that determines optical properties and morphology through measurement of states of polarization of light reflected. The practice of ellipsometry is well established as a non-destructive approach to determining characteristics of sample, and can be applied in real-time process control [66]. Since scatterometry is still a new technology, before integrat-

ing it into the control framework, it is important to characterize the ellipsometry system, and understand the system specifications and limitations.

Ellipsometry is an indirect measurement method, which means the measured signal cannot be converted directly into the structure and composition of the sample. Normally, a mathematical model based analysis must be performed, which uses an iterative procedure to evaluate the sample structure parameters so that the obtained experimental data, and values calculated by the mathematical model having a "best match" relationship.

In spectroscopic ellipsometry measurements analysis, the spot size of the probe beam on the sample surface is a highly critical parameter in the treatment of the experimental data. It has been established that the measured ellipsometric signal will vary according to the probing light beam size and its collimation [46]. In this study, we investigated the effect of beam size on the ellipsometer measurement result.

To characterize the beam size effect, we firstly provided a technique to determine the beam size that uses the existing detection facilities in a spectroscopic ellipsometry setup without the need to rearrange the optical components. The intensity signal recorded with the technique comprises a coupled boundary diffraction and knife edge wave that can be isolated using nonlinear fitting. This then permitted an accurate measurement of the beam size with the stronger knife edge component. The technique has the added advantage of picking up chromatic aberration in the probing lens which may be a factor in ellipsometry measurement.

Then the beam size effect on the ellipsometry measurement is investigated using numerical analysis and verified by experimental result.

This chapter is organized as follows. Section 4.2 introduces the principle of specular spectroscopic ellipsometry. Section 4.3 presents the direct beam size measurement method using a spectroscopic ellipsometry setup, and Section 4.4 gives the numerical analysis and experimental result of the beam size effect on ellipsometry measurement. Conclusions are given in Section 4.5.

4.2 Principle of Ellipsometry

Ellipsometry is an optical technique devoted to the analysis of surfaces. It is based on the measurement of the variation of the polarization state of the light after reflection on a plane surface. The strong advantages of ellipsometry are its non destructive character, its high sensitivity due to the measurement of the phase of the reflected light, its large measurement range (from fractions of single layers to micrometers), and the possibilities to control in real-time complex processes.

When linearly polarized light shines on the sample, the reflected light becomes elliptically polarized due to the different magnitude and phase responses of TE (transverse electric, meaning that the E-field vector is parallel to the grating lines) and TM (transverse magnetic, when the E-field is perpendicular to the grating

lines) lights. We can represent the ratio of the responses as

$$\rho = \frac{\widetilde{r}_p}{\widetilde{r}_s} = \tan \Psi \cdot e^{i\Delta} \tag{4.1}$$

where $\widetilde{r}_s$ and $\widetilde{r}_p$ are the complex reflectivity for TE and TM waves respectively, $\tan \Psi$ the amplitude ratio upon reflection and Δ the phase difference. Since ellipsometry measures the ratio of two values, it is relatively insensitive to scatter and fluctuations, and requires no standard sample or reference beams. Furthermore, since both the intensity response Ψ and the phase response Δ are measured, more information about the sample can be extracted from these signals.

The rotation-polarizer configuration has been used by many state-of-the-art commercial ellipsometer systems. As shown in Figure 4.1, the optical path consists of the broadband light source, two rotatable polarizing filters known as the polarizer and the analyzer, the sample, and the spectrometer. During the measurement, the analyzer stays at a certain position where the angle between the polarization direction and the incidence plane is A, and the polarizer rotates continuously to create time-variant signal at the spectrometer. We can get the $\tan \Psi$ and $\cos \Delta$ from the integral of the measured signal.

When the angle between the polarizer polarization direction and the incidence plane is P, the resulting electrical fields at the end of the optical path can be represented using Jones matrices as [67]

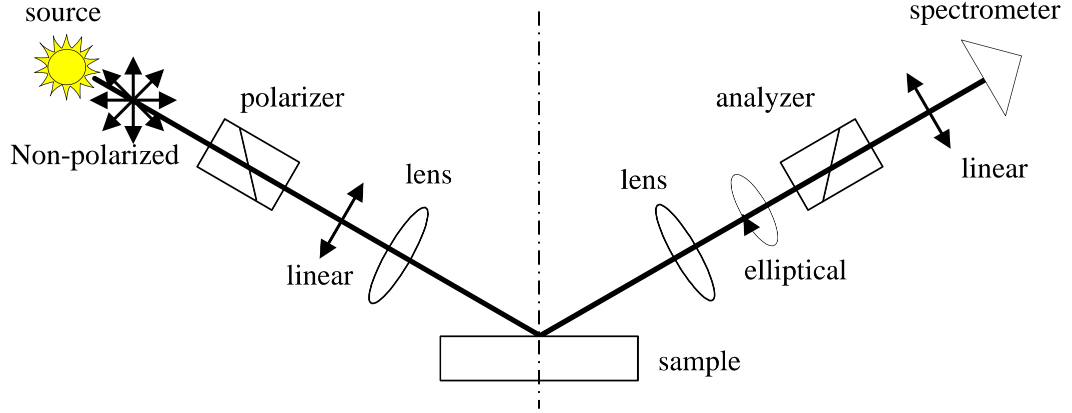


Figure 4.1. Illustration of the rotating-polarizer ellipsometer setup.

$$\begin{pmatrix} \widetilde{E}_p \\ \widetilde{E}_s \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \cos A & \sin A \\ -\sin A & \cos A \end{pmatrix} \begin{pmatrix} \widetilde{r}_p & 0 \\ 0 & \widetilde{r}_s \end{pmatrix} \begin{pmatrix} \cos P & -\sin P \\ \sin P & \cos P \end{pmatrix} \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \widetilde{E}_0 \\ \widetilde{E}_0 \end{pmatrix}$$

where the matrices on the right hand side of the equation represent the effects of analyzer, coordinate rotation for analyzer, sample, coordinate rotation for polarizer, polarizer, and light source, respectively, from left to right. Then the light intensity can be simplified as

$$I(P) = |\widetilde{E_p}|^2 + |\widetilde{E_s}|^2 = I_0(1 + \alpha \cos 2P + \beta \sin 2P) \tag{4.2}$$

where

$$\alpha = \frac{\tan^2 \Psi - \tan^2 A}{\tan^2 \Psi + \tan^2 A} \tag{4.3}$$

$$\beta = \frac{2 \cos \triangle \tan \Psi \tan A}{\tan^2 \Psi + \tan^2 A} \tag{4.4}$$

$$I_0 = \frac{1}{2} |\widetilde{E}_0 \widetilde{r}_s|^2 \cos^2 A (\tan^2 \Psi + \tan^2 A) \tag{4.5}$$

and $\tan\Psi$ and Δ is same as that defined in equation (4.1). The time-variant signal is sampled for a few periods while the polarizer is rotating, then Hadamard transform is used to extract the coefficients α and β for each wavelength. The signal is integrated every quarter of the half-turn of the polarizer:

$$S_1 = \int_0^{\pi/4} I(P)dP = \frac{I_0}{2}(\frac{\pi}{2} + \alpha + \beta) \tag{4.6}$$

$$S_2 = \int_{\pi/4}^{\pi/2} I(P)dP = \frac{I_0}{2}(\frac{\pi}{2} - \alpha + \beta) \tag{4.7}$$

$$S_3 = \int_{\pi/2}^{3\pi/4} I(P)dP = \frac{I_0}{2}(\frac{\pi}{2} - \alpha - \beta) \tag{4.8}$$

$$S_4 = \int_{3\pi/4}^{\pi} I(P)dP = \frac{I_0}{2}(\frac{\pi}{2} + \alpha - \beta) \tag{4.9}$$

Then α and β can be expressed as

$$\alpha = \frac{1}{2I_0}(S_1 - S_2 - S_3 + S_4) \tag{4.10}$$

$$\beta = \frac{1}{2I_0}(S_1 + S_2 - S_3 - S_4) \tag{4.11}$$

and $\tan\Psi$ and $\cos\triangle$ can be derived from Equations (4.3) and (4.4):

$$\tan\Psi = \tan A\sqrt{\frac{1+\alpha}{1-\alpha}} \tag{4.12}$$

$$\cos\triangle = \frac{\beta}{\sqrt{1-\alpha^2}} \tag{4.13}$$

After getting of $\tan\Psi$ and $\cos\triangle$, data processing (solving) is almost always required because the desired reflecting surface parameters, such as film thickness and CD value, are related to the $\tan\Psi$ and $\cos\triangle$ through a system of equations which are typically non-invertible and non-linear. We will restrict the investigation to measurements of $\tan\Psi$ and $\cos\triangle$ in this thesis.

The advantage of the rotating polarizer technique is that it is optically and mechanically simple. Only polarizers and focusing lenses (focusing reflecting mirrors in production configuration) are used in the light path, and these optical elements are relatively easy to make and characterize. Furthermore, since the analyzer angle is fixed during the measurement, the spectrometer does not need to be insensitive to the polarization of the incidence light. Due to its popularity in the scatterometry applications, we will focus on rotating polarizer configurations for the analysis in the remainder part of this chapter.

4.3 Direct Measurement of Beam Size in a Spectroscopic Ellipsometry Setup

Spectroscopic ellipsometry signals used in thin film analysis is dependent on the beam probe size. Hence, it is important to establish the beam size in any measurement conducted as results with wide variances can occur otherwise. A variety of methods have been proposed to measure beam sizes. These include the usage of knife-edges [68], [69], gratings [70], [71], boundary diffraction waves [72], and

quadrant photodiodes [73], [74]. The boundary diffraction wave approach is conducted with the illumination normal to a straight boundary and recording done at an angular position far away from the illumination axis (Figure 4.2A). With the knife edge approach, recording is done at the opposite end along the illumination axis (Figure 4.2B). In a spectroscopic ellipsometry setup as shown in Figure 4.1, it would be ideal to be able to determine the beam size without rearranging the optical components as well as using the existing ellipsometric detection facilities. The application of either the conventional boundary diffraction wave or knife edge technique would violate these requirements. Here, we report an adapted approach that is workable.

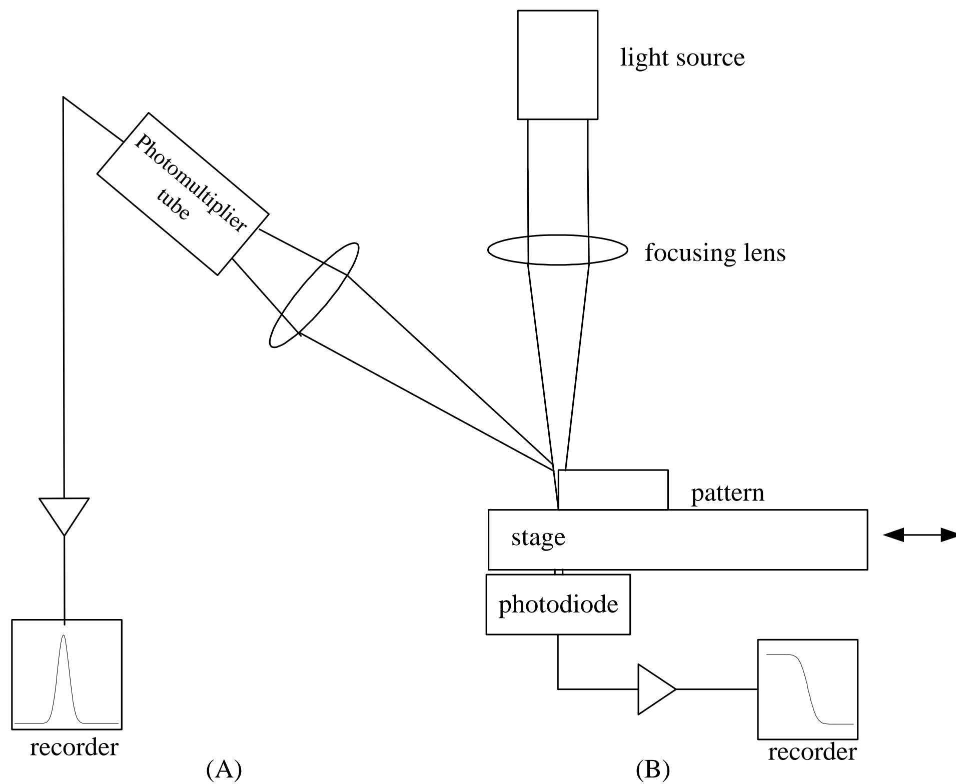


Figure 4.2. Schematic description of the (A) boundary diffraction wave and (B) knife edge methods for beam size measurement.

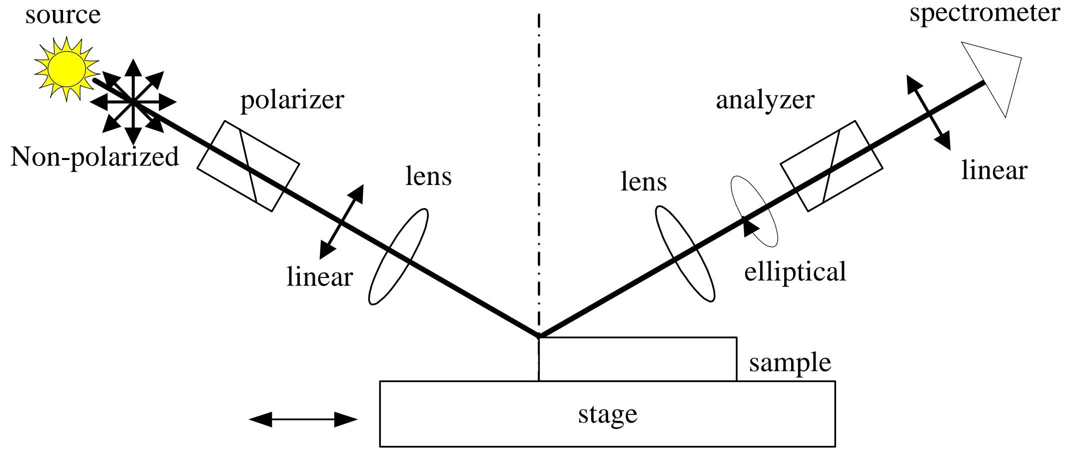


Figure 4.3. Schematic description of the Experimental Setup.

The experimental setup to measure the beam size is shown in Figure 4.3, where we move the sample and monitor the change of the reflected light when the incident light illuminates the sample's edge. In this case the light comes in from an angle instead of perpendicular to the sample surface, so we have both the knife-edge effect and the boundary wave effect recorded at the spectrometer, and our recording data is the combination of the two effects. The knife-edge effect can be expressed in the following equation [75]

$$I_k(x) = K_0 \int_x^{\infty} \sqrt{\frac{2}{\pi}} \frac{1}{\omega_k} e^{(-\frac{2x^2}{\omega_k^2})} dx \tag{4.14}$$

where I_k is the reflected light intensity caused by knife-edge effect, K_0 is a constant parameter, x, y the coordinates on the plane vertical to the beam axis, and ω_k is a parameter representing the beam size in knife-edge effect. The function of

boundary diffraction wave effect is [72]

$$I_b(x) = B_0 e^{(-\frac{2x^2}{\omega_b^2})} \tag{4.15}$$

where I_b is the reflected light intensity caused by boundary diffraction wave, B_0 is a constant parameter, and ω_b is a parameter representing the beam size in boundary diffraction wave effect. The detected light in the setup is essentially a sum of both measures or

$$I(x) = I_k(x) + I_b(x) = K_0 \int_x^{\infty} \sqrt{\frac{2}{\pi}} \frac{1}{\omega_k} e^{(-\frac{2x^2}{\omega_k^2})} dx + B_0 e^{(-\frac{2x^2}{\omega_b^2})} \tag{4.16}$$

The signal for the knife edge will typically be stronger than the boundary wave component. Thus, a nonlinear least squares data fitting method applied on the parameters in Equation (4.16) will allow the beam radius, to be determined. The fitting algorithm is based on the Gauss-Newton method, which uses an iterative procedure to find the point along the searching direction that optimizes the objective function in the least squares sense [76].

Figure 4.4 shows the prototype spectroscopic rotating ellipsometer setup used for thin-film and linewidth measurement. In the system, a high power Xenon light source (HPX-2000 from Photonitech) was used to provide light with wavelengths ranging from 400-800nm. A high-resolution spectrometer (HR4000 CG-UV-NIR from Ocean Optics) was used to detect the reflected light and the signal recorded in a computer. The sample 4 inch prime silicon wafer (P-type doped with boron)

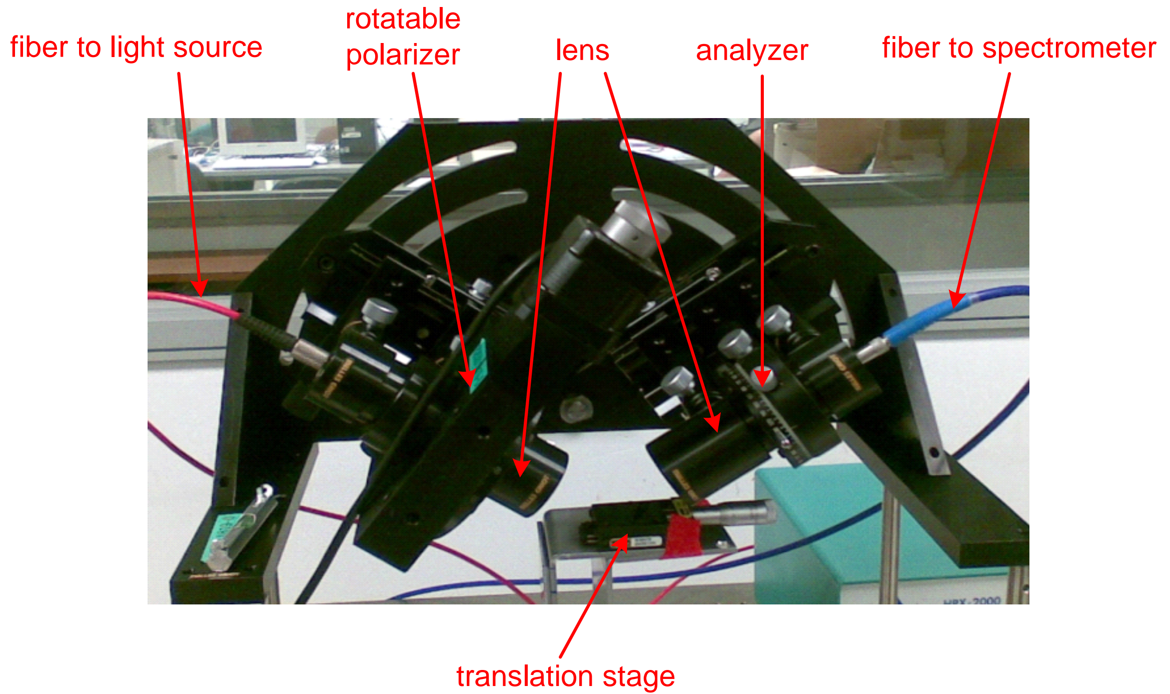


Figure 4.4. Photograph of the experimental setup used.

of thickness $525 \pm 25\mu$m and with a straight edge was mounted on a translation stage with 10 microns resolution along the axis of traveling. The polarizer on the incident side was mounted with a rotating motor and the analyzer on the recording side is fixed at 45°. In this section, the ellipsometric phase and amplitude was not extracted as the objective was to measure the beam size, so the polarizer of the ellipsometer in this case was not rotated, but fixed at 0°. The measured intensity was the reflected light intensity with these fixed polarizer angle (0°) and analyzer angle (45°).

In determining beam radius along the x-axis, the sample wafer was first positioned such that the whole light beam illuminated the wafer's surface. Subsequently, readings with the spectrometer were made as the wafer was translated

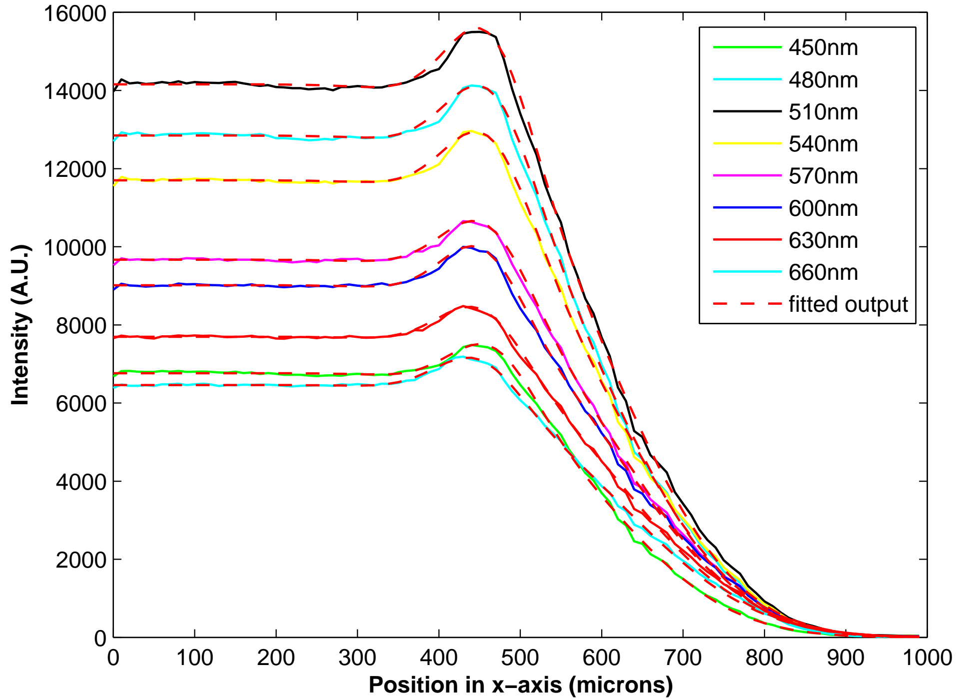
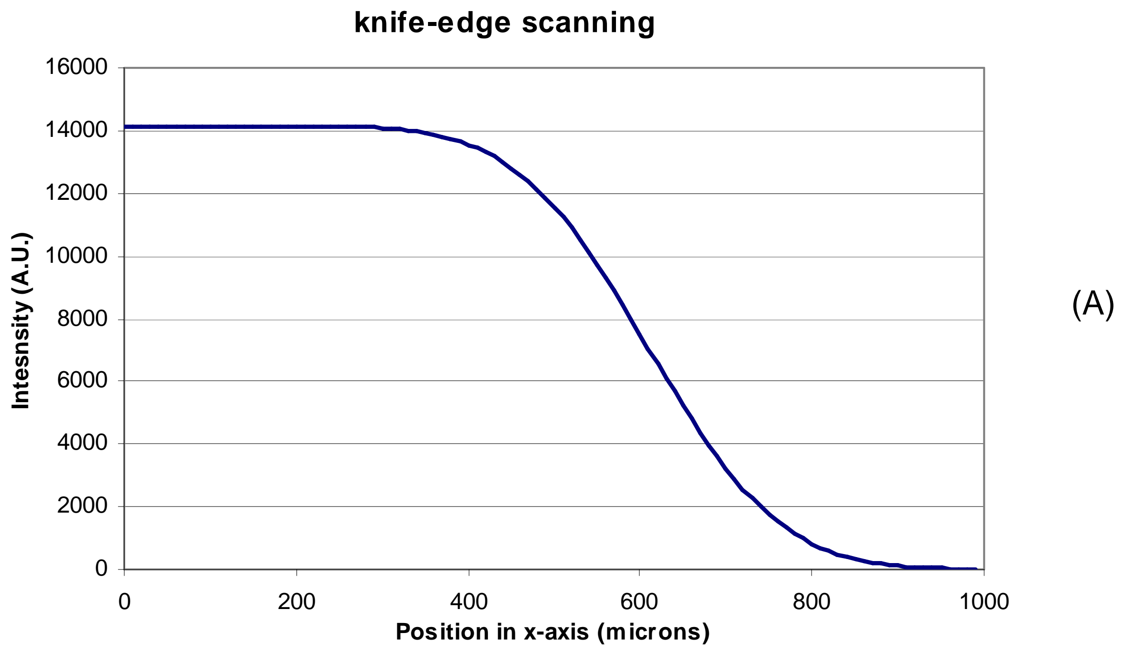


Figure 4.5. Plots of experimental (solid) and simulation (dashed) results obtained with recording at selected wavelengths from 420nm to 750nm.

in the x-axis until the whole light beam is out of the wafer's surface. The spectrometer provided plots of reflected light intensity at different wavelengths. By using a nonlinear least squares data fitting method to equation (4.16), we could extract all the unknown parameters, including K_0, B_0, ω_k and ω_b. With K_0 and ω_k we could plot knife-edge wave using equation (4.14), and with B_0 and ω_b we can also plot boundary-diffraction wave using equation (4.15). Figure 4.5 shows the comparison of the experimental and simulation result for selected wavelengths ranging from 450nm to 660nm. It can be seen that the experimental data matches the fitted output very well for each wavelength. The signal is clearly strongest when the wavelength is in the vicinity of 500nm and is due to the spectral output nature of the source. In order to reduce the effect of electronic noise, the usage



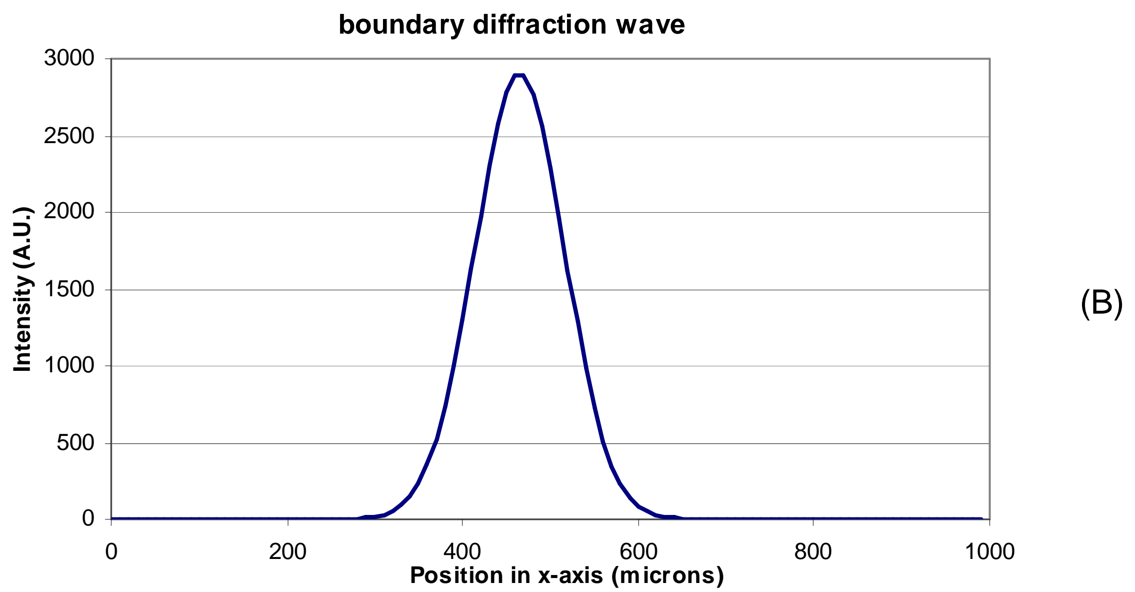


Figure 4.6. Reconstruction of knife-edge and boundary diffraction wave components for 520nm light.

of signals at wavelengths close to 500nm is recommended. Figure 4.6(A) shows a typical fitting output of the knife-edge effect, and Figure 4.6 (B) shows the model output of boundary diffraction wave effect. With the identified model of the two

effects, we can derive the beam radius. It is important to note that the signal from the boundary wave component is typically five times weaker than the knife edge component. Coupled with the observation that fitting deviation tend to be higher at the region where the boundary wave signal resides, it is desirable to use only the isolated knife edge signal to determine the diameter accurately; i.e. the beam radius is based on ω_k.

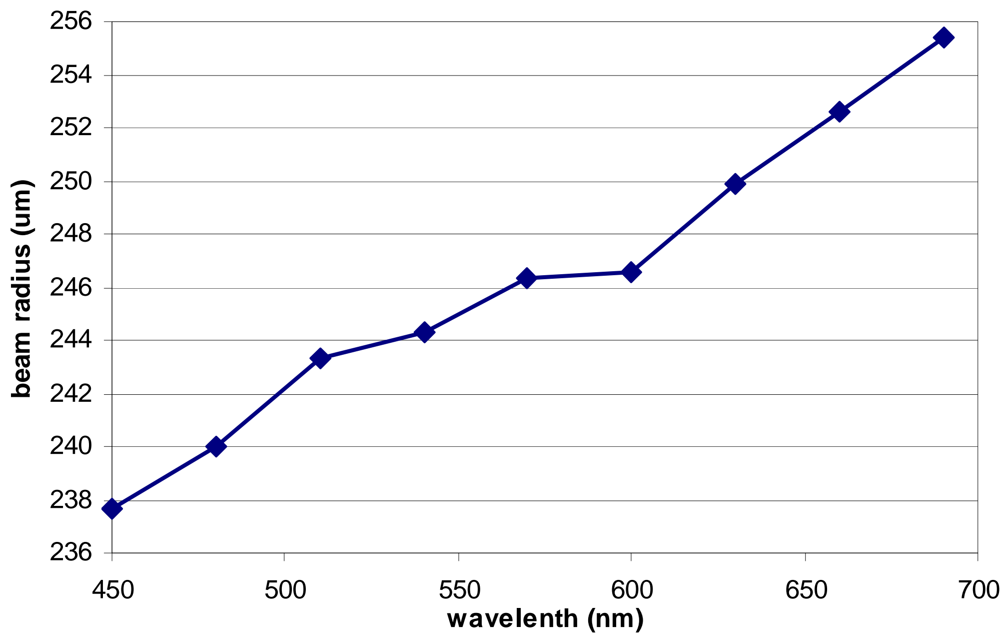


Figure 4.7. Plots of beam sizes computed using different wavelengths.

The beam sizes obtained at different wavelengths are shown in Figure 4.7. It can be seen that the measured beam size is not uniform but rather increases with wavelength. This is likely to be attributed to chromatic aberration in the probe lens of the system. The spectroscopic nature of the system proposed here offers the advantage of ascertaining this, which will typically be missed using conventional setups. The presence of chromatic aberration effects in spectroscopic ellipsometry

is an acknowledged artifact and a scanning focus scheme has been described to account for it [77]. It is conceivable that achromatic lenses may help mitigate the problem to some extent as well.

In summary, we report the ability to determine the probing light beam size in a spectroscopic ellipsometer setup that uses the existing detection facilities without the need to rearrange the optical components. The data collected can be accurately isolated into the knife-edge and boundary diffraction wave components using a nonlinear fitting model. This then permitted accurate determination of beam size via the stronger knife edge component. An added advantage of the approach is the ability to account for beam size variation as a consequence of chromatic aberration in the probe lens.

4.4 Spot Focus Size Effect in Spectroscopic Ellipsometry Result

When ellipsometry is used on films, an optical path length exists between the light reflected from the surface and that travelling through the film. This optical path length change is proportional to the film phase thickness β. This results in the phenomenon of interference which strongly influences the values of $\tan\Psi$ and $cos\Delta$ measured in ellipsometry. Thus film thickness is a parameter that can be readily revealed using ellipsometry. Adopting the model of an ideally optically isotropic three-phase ambient-film-substrate system [78], the ratio of the reflected TM and

TE light response can be expressed as

$$\rho = \left(\frac{r_{01p} + r_{12p} e^{-j2\beta}}{1 + r_{01p} r_{12p} e^{-j2\beta}} \right) \left(\frac{1 + r_{01s} r_{12s} e^{-j2\beta}}{r_{01s} + r_{12s} e^{-j2\beta}} \right) \tag{4.17}$$

where (r_{01p}, r_{01s}) is the ambient-film and (r_{12p}, r_{12s}) the film-substrate interface Fresnel reflection coefficients. From Equation (4.17), it can be seen that β, and thus the optical path length change, can strongly affect the ellipsometric measurement.

In most analysis, the probing light beam is assumed to be collimated. A previous study established that the measured ellipsometric signal will be altered if a collimated light probe of different size is used to interrogate a coated wafer with varying thickness [46]. Typical probe spot sizes for collimated beam SE can range between $2mm$ and $5mm$ in diameter. It is assumed that the wafer characteristics are reasonably uniform within this probe size region. In most situations, however, a focused as opposed to collimated light beam is used as probe in order to overcome the restriction of uniform characterisitics within a relatively large region. Several ellipsometer instruments use "micro-focused" probe beams that are of the order of $25\mu m$ in diameter [79] [80]. The intricacies of probe beam size control is also discussed in a recently awarded patent [77]. The main advantage of the focused light beam is its smaller as well as more intense light interrogation area. However, the focused light beam should intuitively create a higher degree of optical path length distribution as a consequence of the geometry of light rays reflected from the surface and passing through the film. It also imputes that rays of light arrive at the sample surface at different incident angles. In this work, we investigate the

effect when varying spot focus sizes are used.

4.4.1 Geometric Ray Analysis of Spot Focusing

For the rotating polarizer spectroscopic ellipsometer depicted in Figure 4.1. The optics can be considered at the incidence and recording sides of the system. At the light incidence side, a lens is used to focus light from a source in order to achieve a smaller as well as more intense light interrogation area. The light spot size on the sample surface can be easily altered by changing the lens position along the optic axis of illumination as shown in Figure 4.8. The spot diameter can be measured directly on the ellipsometer setup using the approach described in section 4.3.

Now we consider the path of a single ray of light through the film as shown in Figure 4.9. From Snell's Law, we have

$$\frac{\sin\theta_i}{\sin\theta_0} = \frac{n_w}{n_a} \tag{4.18}$$

where θ_i is the incident angle, θ_0 the refractive angle, n_w the refractive index of the medium, and n_a the refractive index of air. From Figure 4.9, we can calculate the optical path length

$$\delta = XYZ = \frac{2t}{\cos\theta_0} \tag{4.19}$$

where t is the normal thickness of the film. From Equations (4.18) and (4.19) we

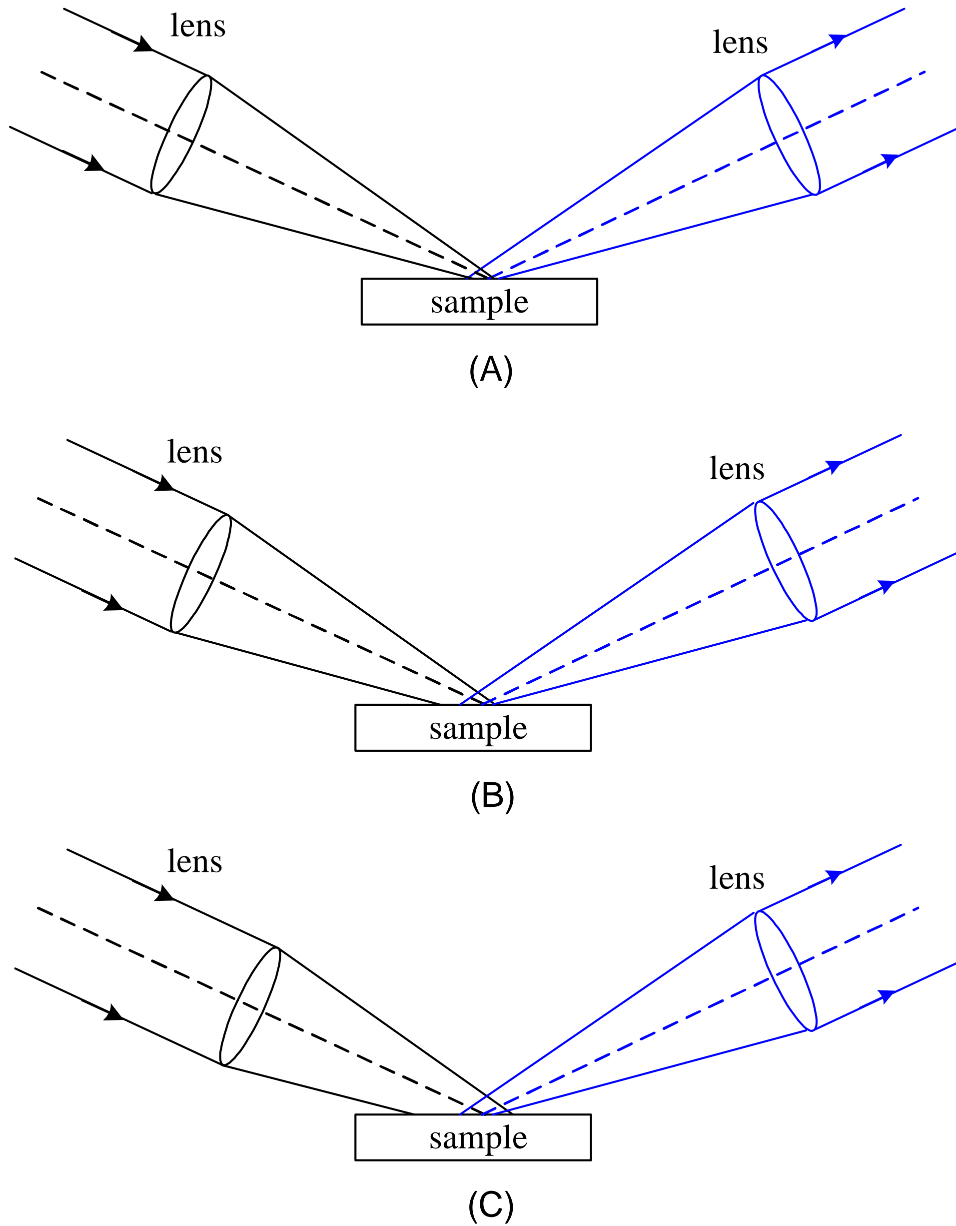


Figure 4.8. Various SE incident lens positions for the different beam size: (A) distance between lens and sample is 55mm to form small beam size; (B) distance between lens and sample is 45mm to form medium beam size; (C) distance between lens and sample is 35mm to form large beam size.

have

$$\delta = \frac{2t}{\cos\left[sin^{-1}\left(\frac{n_a \sin\theta_i}{n_w}\right)\right]} \tag{4.20}$$

From Equation (4.20), it can be seen that the optical path length δ is dependent

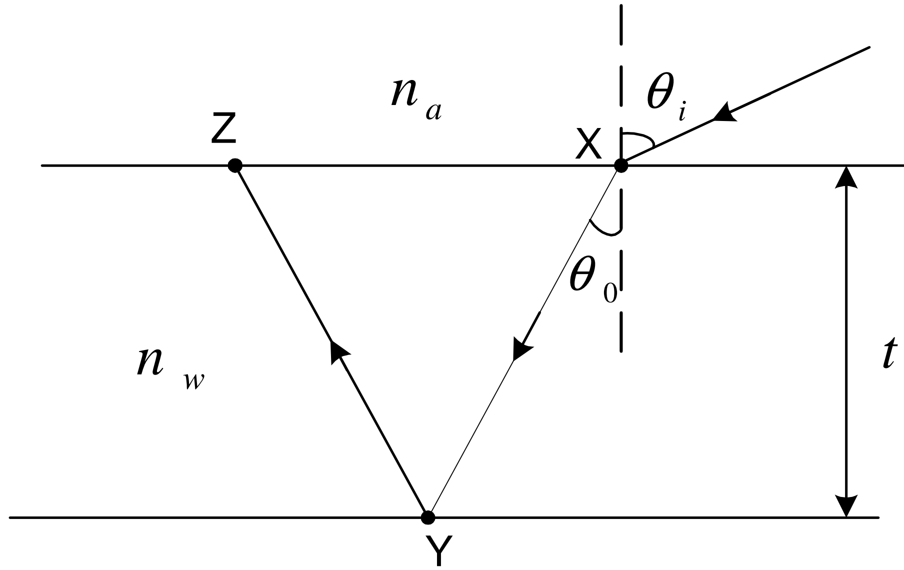


Figure 4.9. Illustration of optical path length calculation for the thin film with uniform thickness.

on the incident angle θ_i of the ray. If a collimated beam is used, all the rays arriving on the sample surface have the same incident angle. However, a focused beam will have rays coming in at different incident angles and thus result in different optical path lengths.

The geometric description of focused rays incident on a sample is given in Figure 4.10. The known parameters include the beam size AB, the illumination angle along the optical axis θ, and beam angle α. The beam angle is related to the numerical aperture of the lens via $NA = n_a \sin\alpha$, where α defined for every beam. Considering triangle BCD in Figure 4.10,

$$\begin{aligned} \angle CBD &= 180^\circ - \angle BDC - \angle DCB \\ &= 180^\circ - (90^\circ + \theta) - \alpha = 90^\circ - \theta - \alpha \end{aligned} \tag{4.21}$$

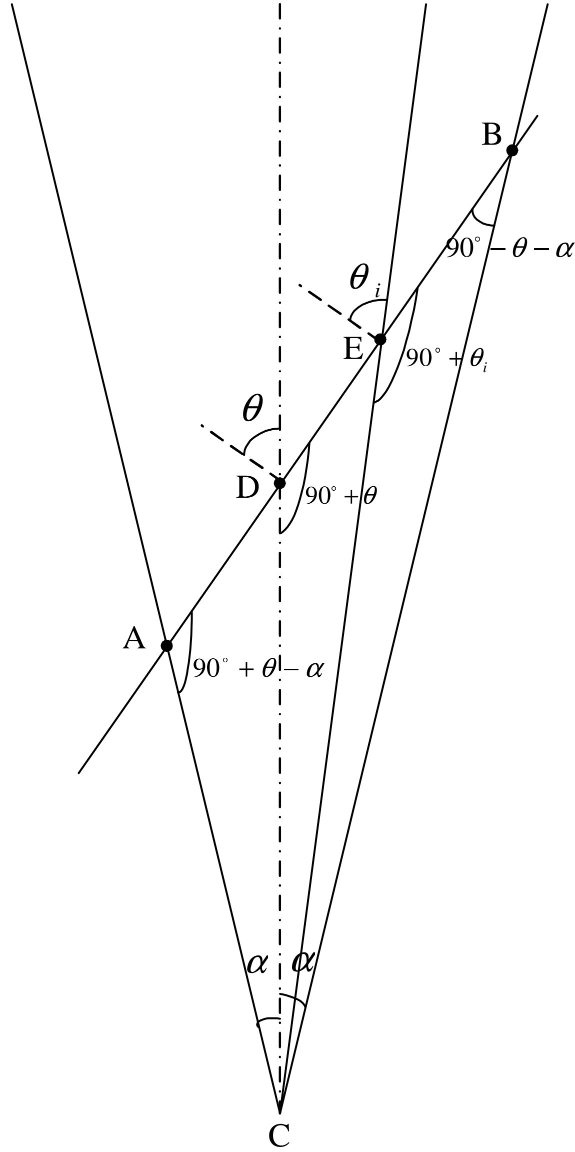


Figure 4.10. Illustration of incident angle calculation for different point of the light beam on sample top surface.

With the geometry of triangle ABC, we have

$$\begin{aligned} \angle BAC &= 180^\circ - \angle ABC - \angle ACB \\ &= 180^\circ - (90^\circ - \theta - \alpha) - 2\alpha = 90^\circ + \theta - \alpha \end{aligned} \tag{4.22}$$

$$\therefore \frac{AB}{\sin 2\alpha} = \frac{BC}{\sin(90^\circ + \theta - \alpha)} \tag{4.23}$$

Considering triangle BCE, we have

$$\begin{aligned} \angle BCE &= 180^\circ - \angle EBC - \angle CEB \\ &= 180^\circ - (90^\circ - \theta - \alpha) - (90^\circ + \theta_i) = \theta + \alpha - \theta_i \end{aligned} \tag{4.24}$$

$$\therefore \frac{BE}{\sin(\theta + \alpha - \theta_i)} = \frac{BC}{\sin(90^\circ + \theta_i)} \tag{4.25}$$

Eliminating BC in Equation(4.23) and (4.25), provides us with

$$\frac{\sin(90^\circ + \theta - \alpha)}{\sin(2\alpha)} = \frac{BE}{AB} \times \frac{\sin(90^\circ + \theta_i)}{\sin(\theta + \alpha - \theta_i)} \tag{4.26}$$

Equation (4.26) allows us to find θ_i for $0 \leq BE \leq AB$. If we use $L = \frac{BE}{AB}$ as a non-dimensional parameter, we can calculate the incident angle θ_i for L as it varies from 0 to 1. Knowledge of θ_i then allows the optical path length δ to be determined.

It is important to note that δ is also wavelength dependent. From Equation (4.20) we can see that the optical path length is dependent on the medium refractive index (n_i). The variation of refractive index with wavelength λ is given by the Cauchy equation [81]:

$$n_i(\lambda) = A_i + \frac{B_i}{\lambda^2} + \frac{C_i}{\lambda^4} \tag{4.27}$$

where A_i, B_i and C_i are the Cauchy parameters.

The extent of optical path length variation at each wavelength can be approximated using $\delta(\lambda)_{max} - \delta(\lambda)_{min}$ for $0 \leq L \leq 1$.

For the recording side of ellipsometer, a lens is similarly used to collect the reflected light. The recording with a lens however is limited by diffraction and aberration. The recording spot size subject to spherical aberration can be expressed as

$$Size = \frac{0.067f}{(f/\#)^3} \tag{4.28}$$

where f is the focal length of the lens and $f/\# = \dfrac{1}{2NA}$ is the f-number. The numerical aperture of the lens is given by

$$NA = \sin\left(\frac{D}{2S}\right) \tag{4.29}$$

where D is the lens diameter and S the distance between the lens and the sample surface. If we assume that the optical axes of the illumination and recording lens are coincident, the recorded spot size will then correspond to a range of values of L extending from $L^{'}$ to $L^{''}$. The average optical path length at each wavelength and beam size can be found using $\langle\delta(\lambda, L)\rangle$ for$L^{'} \leq L \leq L^{''}$; where $\langle\rangle$ is the mean operator. The extent of optical path length variation at each wavelength and beam size can be approximated using $\delta(\lambda)_{max} - \delta(\lambda)_{min}$ for $L^{'} \leq L \leq L^{''}$.

4.4.2 Numerical Analysis

In the experiment, the recording lens has focal length $f = 55$mm, diameter $D = 30$mm, and distance between lens and sample $S = 62$mm . Thus the spot size at the recording end is 0.43mm based on Equations (4.28) and (4.29).

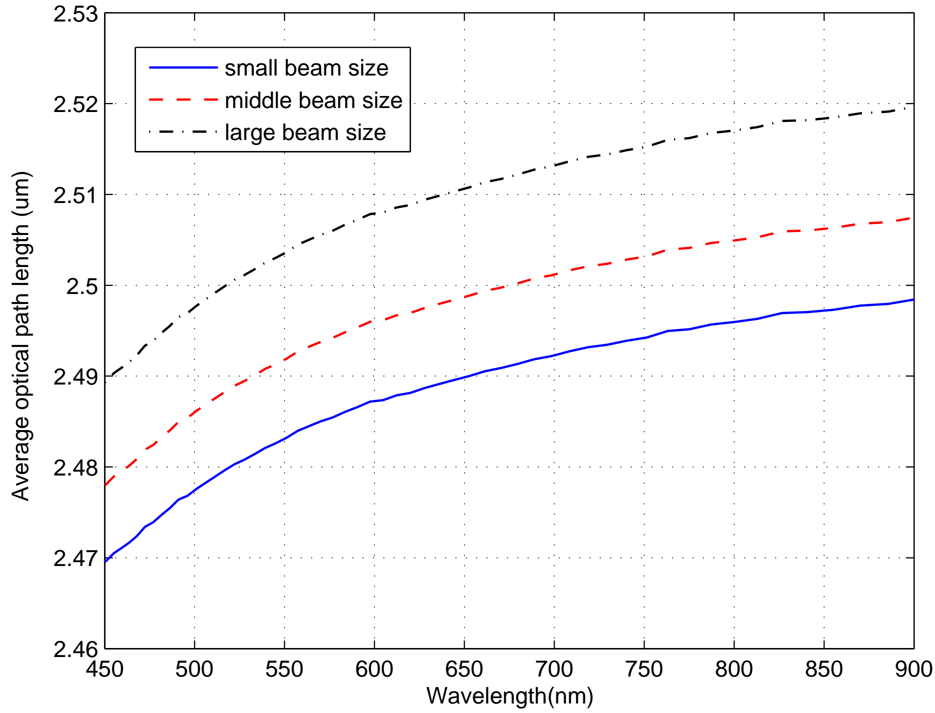


Figure 4.11. Simulation result of the average optical path length for different beam sizes at different wavelengths.

We assume the case where all samples have a silicon substrate and illumination is made with the beam angle along the optical axis of $\theta = 65°$. Illumination sizes for the small, medium and large beams are taken to be 0.109mm, 0.537mm, and 1.467mm respectively. The size of the small beam is smaller than the recording spot size. Hence for this beam, $L^{'} = 0$ and $L^{''} = 1$. For the medium size beam, the ratio of the recording spot to the beam size is $0.43/0.537 = 0.81$. Hence for

this beam $L^{'} = 0.1$ and $L^{''} = 0.9$. In the case of the large beam, the ratio is 0.2932 which gives $L^{'} = 0.35$ and $L^{''} = 0.65$. The average optical path length at each wavelength and beam size computed is shown in Figure 4.11. In the simulation, the film thickness is assumed to be 1μm. It can be seen that an increasing trend of average optical path length with wavelength is obtained for all beam sizes with the shapes looking very much alike. The average optical path values were highest for the large beam size and decreased in the order of the beam size.

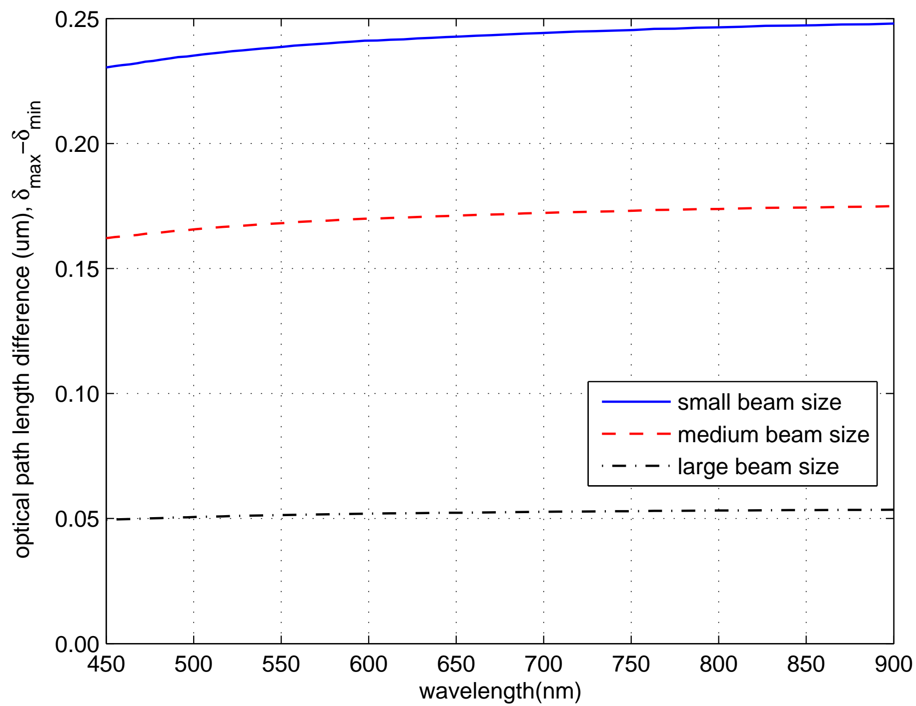


Figure 4.12. Simulation result of optical path length difference for different beam sizes at different wavelengths.

The extent of optical path length variation at each wavelength and beam size, approximated using $\delta(\lambda)_{max} - \delta(\lambda)_{min}$ for $L^{'} \leq L \leq L^{''}$, is shown in Figure 4.12. As in the case of the average optical path length, the extent of variation will increase with wavelength. Nevertheless, in this case the highest optical path length variation

occurs for the small beam and decreased in the opposite order of beam size. These results indicate that beam sizes play a role in optical path length characteristics, which should therefore also affect spectroscopic ellipsometry measurements.

4.4.3 Experimental Result

In the experiment, AZ7200 photoresist, formulated with propylene glycol monomethyl ether acetate (PGMEA) solvent from Clariant, was used to form a layer on the wafer's surface. Two 4 inch P type wafers with the thicknesses $525 \pm 25\mu$m were used as the substrate. The first wafer (wafer1) was coated with 4ml photoresist to form a relatively thick layer and spun coated at a speed of 4000rps to get a uniform layer. The second wafer (wafer 2) was coated with 2ml photoresist and spun coated at the same speed.

The ellipsometric measurements with wafer1 of $\tan\Psi$ and $cos\Delta$ against wavelength distributions obtained are given in Figure 4.13(A) and (B) respectively. There are clearly a series of peaks and valleys in the distributions; indicating the presence of an optical interference effect. The positions of the peaks and their values are tabulated in Table 4.1. It can be seen that the spacing between the peaks reduces with increasing size beams. This corresponds with the numerical simulation results in Figure 4.11 wherein higher values of average optical path lengths are obtained with larger beam sizes. In interferometry, it is well known that the spacing of fringes decrease with optical path length. It can also be seen that departure in peak positions are more pronounced with increasing wavelength.

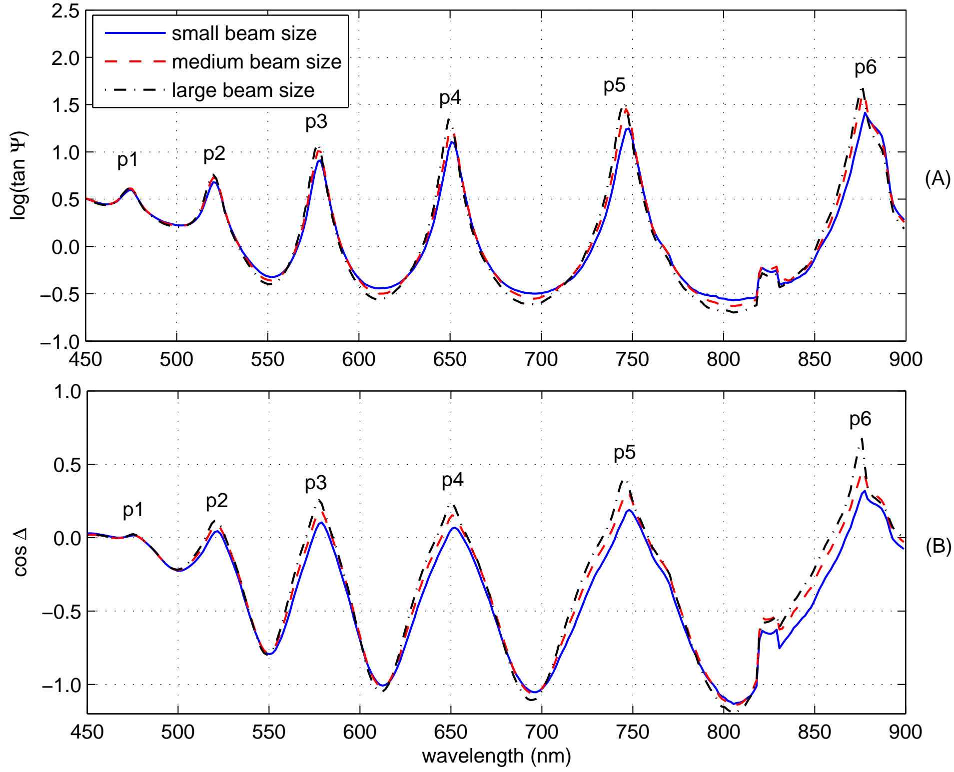


Figure 4.13. Experimental result of the wafer with thick photoresist layer for different beam sizes.

This again corresponds closely with the numerical simulation results in Figure 4.11 wherein values of average optical path lengths increase with wavelength.

In Figure 4.13 and Table 4.1, it can also be seen that the amplitudes and values of the peaks are lower for the small beam and increased with size. This corresponds with the numerical simulation results in Figure 4.12 wherein higher values of optical path length variation are obtained with a smaller beam size. In interferometry, it is well known that fringe visibility decreases with increasing optical path length mismatch between recombined beams. It can also be seen that departure in peak positions are more pronounced with increasing wavelength. This again corresponds closely with the numerical simulation results in Figure 4.12 wherein values of the

Table 4.1. Wavelengths locations and values corresponding to the peaks of the $log(\tan\Psi)$ and $\cos\Delta$ distributions in Figure 4.13 for wafer with a relatively thick photoresist layer.

		$log(\tan\Psi)$			$\cos\Delta$		
Peak	Beam size	Large	Medium	Small	Large	Medium	Small
p1	Wavelength(nm)	473.86	473.86	475.45	475.45	475.45	475.45
	Value	0.6189	0.6126	0.5973	0.0236	0.0149	0.0158
p2	Wavelength(nm)	520.09	520.09	520.09	520.09	521.69	521.69
	Value	0.7604	0.7287	0.6797	0.1165	0.0860	0.0451
p3	Wavelength(nm)	577.74	577.74	579.01	577.74	579.01	579.01
	Value	1.0895	1.0075	0.9124	0.2562	0.1824	0.1035
p4	Wavelength(nm)	649.10	650.70	650.70	650.70	650.70	652.29
	Value	1.3444	1.2390	1.1044	0.2364	0.1523	0.0672
p5	Wavelength(nm)	744.89	746.48	748.08	746.48	746.48	748.08
	Value	1.5091	1.4535	1.2484	0.4029	0.3097	0.1894
p6	Wavelength(nm)	876.05	876.05	877.60	876.05	876.05	877.60
	Value	1.7135	1.6104	1.4147	0.6737	0.4567	0.3186

optical path length variation increase with wavelength.

Table 4.2. Wavelengths locations and values corresponding to the peaks of the $log(\tan\Psi)$ and $\cos\Delta$ distributions in Figure 4.14 for wafer with a relatively thin photoresist layer.

		$log(\tan\Psi)$			$\cos\Delta$		
Peak	Beam size	Large	Medium	Small	Large	Medium	Small
p1	Wavelength(nm)	489.81	491.41	493.00	491.41	491.41	493.00
	Value	0.6666	0.6571	0.6377	0.0398	0.0345	0.0207
p2	Wavelength(nm)	543.98	545.58	545.58	543.98	545.58	547.17
	Value	0.9762	0.9051	0.8523	0.1974	0.1522	0.1005
p3	Wavelength(nm)	612.45	614.04	615.63	612.45	614.04	615.63
	Value	1.2798	1.1702	1.0823	0.1857	0.1182	0.0532
p4	Wavelength(nm)	701.77	703.36	704.96	701.77	703.36	704.96
	Value	1.5229	1.4155	1.2776	0.3346	0.2410	0.1417
p5	Wavelength(nm)	822.82	824.40	830.71	822.82	824.40	830.71
	Value	1.9773	1.8030	1.5239	0.6416	0.4523	0.2898

The ellipsometric measurements with wafer2 of $\tan\Psi$ and $cos\Delta$ against wavelength distributions obtained are given in Figure 4.14 (A) and (B) respectively.

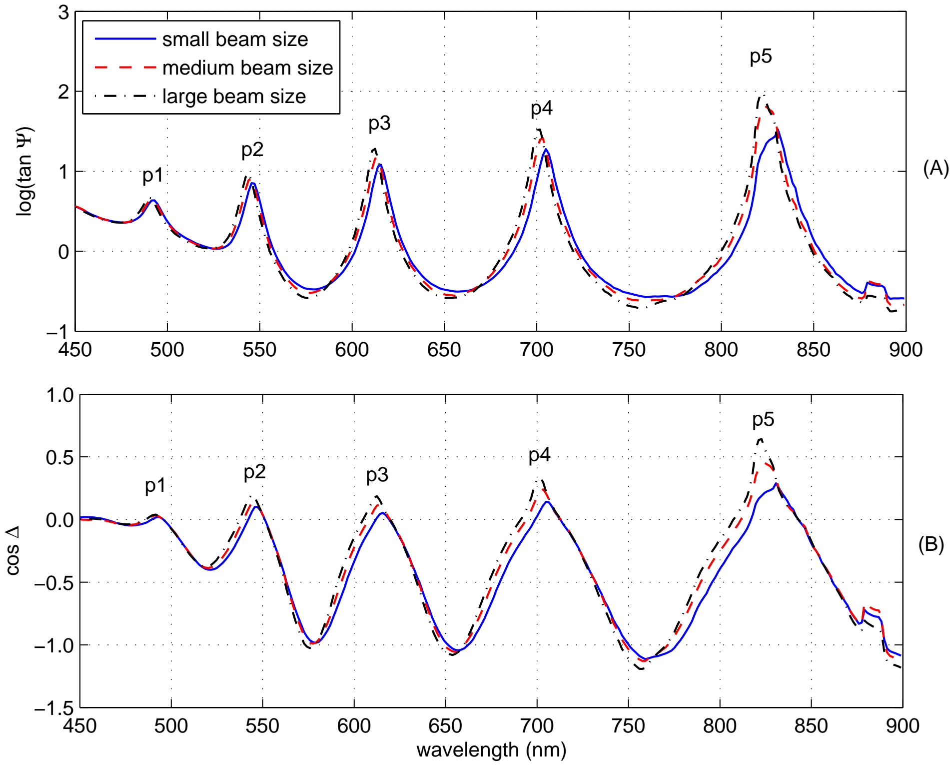


Figure 4.14. Experimental result of the wafer with thin photoresist layer for different beam sizes.

A series of peaks and valleys are again found in the distributions. The positions of the peaks and their values are tabulated in Table 4.2. The results follow an identical trend as with wafer1. As all parameters, except film thickness, are kept the same, this demonstrates the consistency of the findings. It can be seen that spacings between the distribution peaks in Figure 4.13 are smaller than those in Figure 4.14. This is consistent with the physical case of wafer1 being thicker than wafer2. Obviously, the average optical path length should be greater in a thicker than a thinner film.

It is found here that different focus probe beam sizes can cause variations in spectroscopic ellipsometry measurements of wafer films despite them having uni-

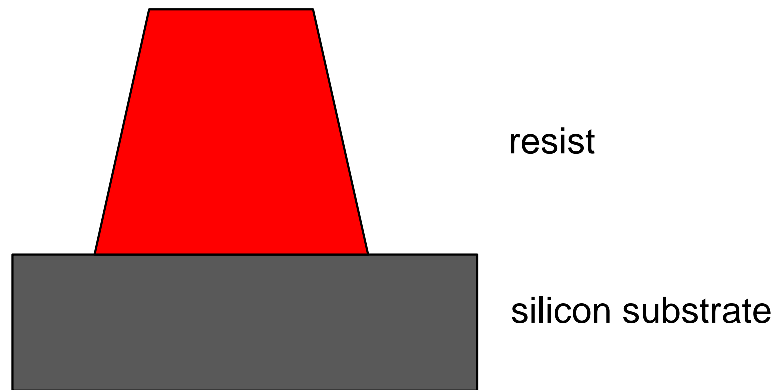


Figure 4.15. Grating structure used in experiment

form thicknesses. To verify the effect of beam size on the ellipsometry readings of the etched structures, we did experiments with different beam sizes on patterned wafer sample. The photoresist used in the experiment is Shipley SL4000 positive photoresist. The grating schematic structure is shown in Figure 4.15. The patterned resist sits on silicon substrate top surface. The grating pitch is 800nm, the width of the channel is 240nm and the height of the photoresist is 215nm.

Using the same method described in section 4.4.1, we can change the beam size on the patterned sample and get the ellipsometric measurements using the system shown in Figure 4.4. The ellipsometric measurements with the patterned wafer of $\tan\Psi$ and $cos\Delta$ against wavelength distributions obtained are given in Figure 4.16 (A) and (B) respectively.

It can be seen that the ellipsometric measurements will vary with different beam sizes.

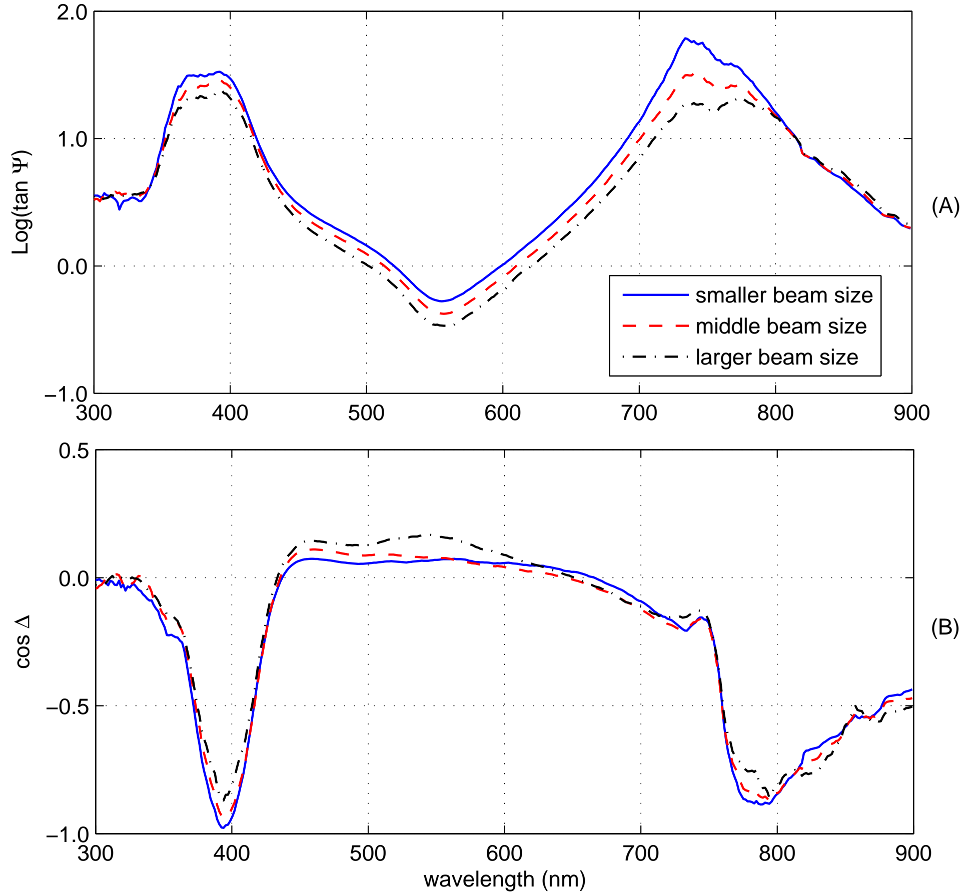


Figure 4.16. Experimental result of the wafer with patterned structure photoresist for different beam sizes.

4.5 Conclusion

In this work, we proposed a method to directly measure the beam size in a spectroscopic ellipsometry setup. Based on this method, we investigated the beam size effect on the ellipsometric measurement using a numerical ray path analysis. The analysis conducted showed that both the average optical path lengths and the optical path length differences displayed increasing trends with wavelength. These trends were found to be sensitive to the focus beam size and could be used to account for the anomalous nature experimental measurements of amplitude and

phase obtained with spectroscopic ellipsometer. Experimental results show that the difference in beam size will lead to different ellipsometric measurement results for both uniform film and patterned wafer.

Chapter 5

Conclusions

5.1 Summary

Real-time process feedback control is a promising solution to meet the ever demanding CD control tolerances. This thesis examines the three major elements of real-time process control: control method, processing system and integrated metrology in advanced lithography process.

In Chapter 2, an in-situ approach is proposed for real-time estimation and control of both the transient and the steady-state wafer temperature during the baking steps in the lithography process. Based on the detailed thermal model of baking process and the real-time measurement of bake-plate temperature, the average air-gap thickness between the bake-plate and wafer in each of the heating zones can be estimated. Consequently, the in-situ wafer temperature can be calculated and

controlled to minimize the temperature non-uniformity using a PI controller. With the proposed approach, the wafer spatial temperature uniformity during the entire thermal cycle achieved an improvement of more than 80% when compared to the existing methods.

In Chapter 3, a new design of integrated bake/chill thermal processing module is developed to achieve spatial temperature uniformity of a silicon wafer throughout the entire processing temperature cycle in lithography. A set of TEDs is employed to provide spatial and temporal temperature uniformity control in the process. The wafer sits on an array of proximity pins above the TEDs, and RTD sensors can be embedded into the proximity pins to provide in-situ temperature measurement. The wafer temperature non-uniformity in the process is minimized by adopting the new proposed model-based feedback control algorithm. Experimental results show that the temperature difference between the feedback points can be less than 0.1°C in the whole PEB process, and the spatial wafer temperature non-uniformity can be well-controlled to within ±0.3°C and ±0.1°C during the transient and steady-state period of thermal cycle respectively.

In Chapter 4, the effect of beam size on the scatterometer CD measurement result is investigated. The beam sizes are measured using the new proposed direct beam size measurement method in a spectroscopic ellipsometry setup, in which the change of the reflected light when incident light illuminates the moving sample's edge is recorded. This recorded signal can be isolated into boundary diffraction and knife edge wave effects using nonlinear fitting algorithm, and the stronger

knife edge component provides an accurate measurement of the beam size. Based on the measured beam size value, numerical ray path analysis is done to analyze the optical path length of the light. The analysis shows that both the average optical path lengths and the optical path length differences are sensitive to the focus beam size. Experimental results also show that different beam sizes lead to different ellipsometric measurement results for both uniform film and patterned wafer.

5.2 Future Work

Since scatterometry is one of the few metrologies that have true in-situ potential for deep sub-micron CD and profile analysis, it can be treated as an effective sensor to monitor the formation of latent image for chemically amplified resists in PEB process. One possible future work is to integrate the thermal processing system and the scatterometer to form a real-time CD control system in PEB process as shown in Figure 5.1. In the system, the scatterometric sensor can be used to monitor the latent image formation in PEB process. With the measured information, an inverse model can be used to determine the optimal PEB temperature reference. The in-situ PEB temperature reference can then be the new setpoint for the thermal processing module.

To fulfill the CD control system, an inverse model of the system has to be developed. The inverse model will be used to obtain the optimum PEB temperature

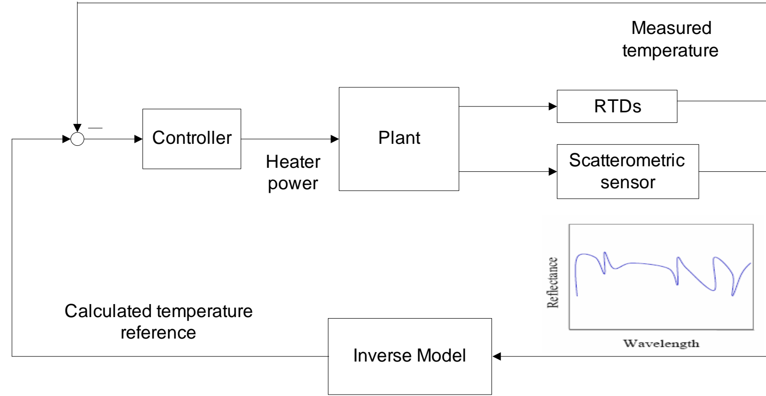


Figure 5.1. Schematic diagram of the CD control strategy.

reference from the measured scattered light. It will comprise signature library and PEB parameters model as shown in Figure 5.2.

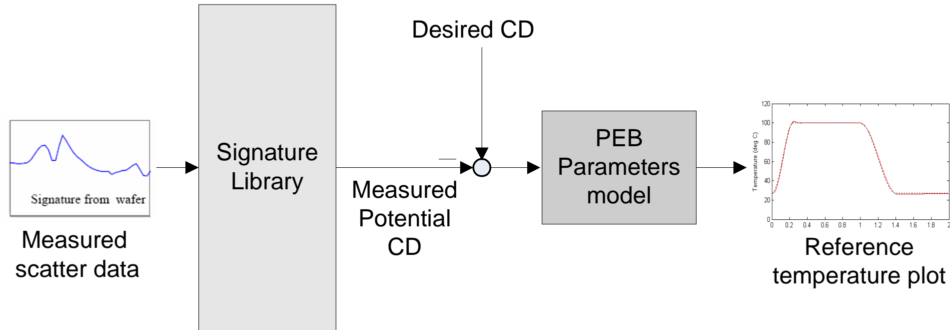


Figure 5.2. Diagram of the inverse model.

In the inverse model, the features of potential latent image is firstly reconstructed from the scattered data using the library-based method as shown in Figure 5.3 [82]. With this method, the measured data is compared with the reference data in signature library (which is derived from the Maxwell equations using rigorous coupled-wave analysis (RCWA) [42]), and the closest match is then reported as the potential CD value. Next, the measured potential CD will be compared with the desired CD value and their difference is referenced to the PEB parame-

ters model, as shown in Figure 5.2, to determine the optimum PEB temperature reference.

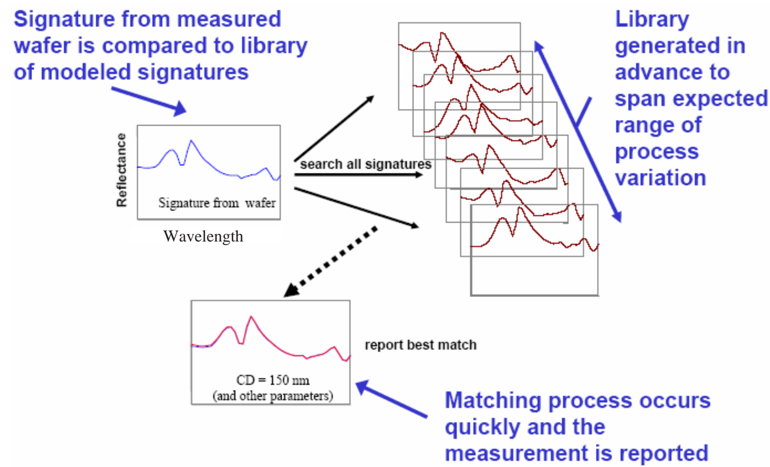


Figure 5.3. Library-based method for inverse problem.

With our designed thermal processing system, the wafer temperature can follow the reference rigorously in the entire process. Using the multi-zone bake plate design, we can even control the wafer temperature at different position to follow different reference to achieve uniform CD across the wafer.

The diagram of a multi-zone CD control system is shown in Figure 5.4. In the multi-zone system, the in-situ spectral detectors will update the potential CD values for different control zones, and the controller will thus be able to calculate the new desired wafer temperature reference for each of the control zones. The thermal processing system will consequently tune the thermal power to achieve temperature reference values. Using this method, the PEB temperature reference can be adjusted on-line so that the process error occurred in the previous steps of lithography can be compensated and the final CD uniformity can be guaranteed.

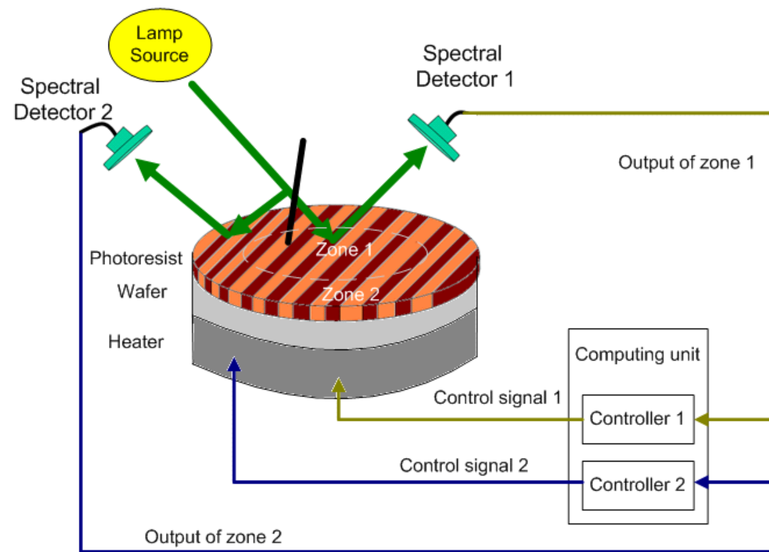


Figure 5.4. Schematic diagram of a 2-zone system.

It has been verified in Chapter 4 that the difference in ellipsometer beam size will lead to different ellipsometry measurement result. Another possible future work is to quantify the optimal focus beam size value for CD profile measurement. Based on the standard AFM CD profile measurement, it is possible to extract the best matched CD profile with different beam size values in ellipsometer measurement. The optimal focus beam size value can thus be determined.

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Appendix A1: Derivation of State-space Model of the System

For the wafer modeling, define

$$r_{w(i)} = \begin{cases} \dfrac{\triangle_r}{k_w A_{ws(i)}}, & 1 \leq i \leq N-1 \\ \dfrac{1}{h_w A_{ws(N)}}, & i = N \end{cases} \tag{A.1}$$

$$r_{aw(i)} = \frac{1}{h_w A_{wz(i)}}, \qquad 1 \leq i \leq N \tag{A.2}$$

$$r_{wag(i)} = \frac{z_{ag}/2k_{ag} + z_w/2k_w}{A_{wag(i)}}, \qquad 1 \leq i \leq N \tag{A.3}$$

$$\frac{1}{R_{w(i)}} = \frac{1}{r_{w(i-1)}} + \frac{1}{r_{w(i)}} + \frac{1}{r_{aw(i)}} + \frac{1}{r_{wag(i)}} \tag{A.4}$$

Thus, Equation (2.1) can be expressed as

$$C_{w(i)}\dot{T}_{w(i)}(t) = \frac{1}{r_{w(i-1)}}T_{w(i-1)}(t) + \frac{1}{r_{w(i)}}T_{w(i+1)}(t) + \frac{1}{r_{wag(i)}}T_{ag(i)}(t) - \frac{1}{R_{w(i)}}T_{w(i)}(t) \tag{A.5}$$

In the state-space model, we can get

$$
\begin{aligned}
F_{ww}(i,i) &= -\frac{1}{C_{w(i)}R_{w(i)}}, \qquad 1 \le i \le N \\
F_{ww}(i,i+1) &= \frac{1}{C_{w(i)}r_{w(i)}}, \qquad 1 \le i \le N-1 \\
F_{ww}(i,i-1) &= \frac{1}{C_{w(i)}r_{w(i-1)}}, \qquad 2 \le i \le N \\
F_{wag}(i,i) &= \frac{1}{C_{w(i)}r_{wag(i)}}, \qquad 1 \le i \le N
\end{aligned} \tag{A.6}
$$

For the air-gap layer modeling, define

$$
r_{ag(i)} = \begin{cases} \dfrac{\triangle_r}{k_{ag}A_{ags(i)}}, & 1 \le i \le N-1 \\ \dfrac{1}{h_{ag}A_{ags(N)}}, & i = N \end{cases} \tag{A.7}
$$

$$
r_{agp(i)} = \frac{z_{ag}/2k_a + z_p/2k_p}{A_{agp(i)}}, \qquad 1 \le i \le N \tag{A.8}
$$

$$
r_{agap(i)} = \frac{z_{ag} + z_p}{2k_a A_{agap(i)}}, \qquad 1 \le i \le N \tag{A.9}
$$

$$
\frac{1}{R_{ag(i)}} = \frac{1}{r_{ag(i-1)}} + \frac{1}{r_{ag(i)}} + \frac{1}{r_{wag(i)}} + \frac{1}{r_{agp(i)}} + \frac{1}{r_{agap(i)}} \tag{A.10}
$$

Thus, Equation (2.2) can be expressed as

$$
\begin{aligned}
C_{ag(i)}\dot{T}_{ag(i)}(t) &= \frac{1}{r_{ag(i-1)}}T_{ag(i-1)}(t) + \frac{1}{r_{ag(i)}}T_{ag(i+1)}(t) + \frac{1}{r_{wag(i)}}T_{ag(i)}(t) \\
&+ \frac{1}{r_{agp(i)}}T_{p(i)}(t) + \frac{1}{r_{agap(i)}}T_{ap(i)}(t) - \frac{1}{R_{ag(i)}}T_{ag(i)}(t)
\end{aligned} \tag{A.11}
$$

The state-space model matrix can be calculate as

$$\begin{aligned}
F_{agag}(i,i) &= -\frac{1}{C_{ag(i)}R_{ag(i)}}, & 1 \le i \le N \\
F_{agag}(i,i+1) &= \frac{1}{C_{ag(i)}r_{ag(i)}}, & 1 \le i \le N-1 \\
F_{agag}(i,i-1) &= \frac{1}{C_{ag(i)}r_{ag(i-1)}}, & 2 \le i \le N \\
F_{agw}(i,i) &= \frac{1}{C_{ag(i)}r_{wag(i)}}, & 1 \le i \le N \\
F_{agp}(i,i) &= \frac{1}{C_{ag(i)}r_{agp(i)}}, & 1 \le i \le N \\
F_{agap}(i,i) &= \frac{1}{C_{ag(i)}r_{agap(i)}}, & 1 \le i \le N
\end{aligned} \tag{A.12}$$

For the bake-plate modeling, define

$$r_{ip(i)} = \frac{t_{p(i)}/2k_p + t_{ap(i-1)}/2k_a}{A_{ips(i)}}, \qquad 2 \le i \le N \tag{A.13}$$

$$r_{op(i)} = \begin{cases} \dfrac{t_{p(i)}/2k_p + t_{ap(i)}/2k_a}{A_{ops(i)}}, & 1 \le i \le N-1 \\ \dfrac{1}{h_p A_{ps(N)}}, & i = N \end{cases} \tag{A.14}$$

$$r_{pc(i)} = \frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}, \qquad 1 \le i \le N \tag{A.15}$$

$$r_{pe(i)} = \frac{1}{h_p A_{pa(i)}}, \qquad 1 \le i \le N \tag{A.16}$$

$$\frac{1}{R_{p(i)}} = \frac{1}{r_{ip(i)}} + \frac{1}{r_{op(i)}} + \frac{1}{r_{agp(i)}} + \frac{1}{r_{pc(i)}} + \frac{1}{r_{pe(i)}} \tag{A.17}$$

Thus, Equation (2.3) can be expressed as

$$\begin{aligned} C_{p(i)}\dot{T}_{p(i)}(t) &= \frac{1}{r_{ip(i)}}T_{ap(i-1)}(t) + \frac{1}{r_{op(i)}}T_{ap(i)}(t) + \frac{1}{r_{agp(i)}}T_{ag(i)}(t) \\ &+ \frac{1}{r_{pc(i)}}T_{c(i)}(t) - \frac{1}{R_{p(i)}}T_{p(i)}(t) \end{aligned} \quad (A.18)$$

The state-space model matrix can be calculate as

$$\begin{aligned} F_{pp}(i,i) &= -\frac{1}{C_{p(i)}R_{p(i)}}, \qquad 1 \le i \le N \\ F_{pap}(i,i) &= \frac{1}{C_{p(i)}r_{op(i)}}, \qquad 1 \le i \le N-1 \\ F_{pap}(i,i-1) &= \frac{1}{C_{p(i)}r_{ip(i)}}, \qquad 2 \le i \le N \\ F_{pag}(i,i) &= \frac{1}{C_{p(i)}r_{agp(i)}}, \qquad 1 \le i \le N \\ F_{pc}(i,i) &= \frac{1}{C_{p(i)}r_{pc(i)}}, \qquad 1 \le i \le N \end{aligned} \quad (A.19)$$

For the air-gap inside the bake-plate modeling, define

$$r_{ape(i)} = \frac{1}{h_{ap}A_{agap(i)}}, \qquad 1 \le i \le N-1 \quad (A.20)$$

$$\frac{1}{R_{ap(i)}} = \frac{1}{r_{op(i)}} + \frac{1}{r_{ip(i+1)}} + \frac{1}{r_{agap(i)}} + \frac{1}{r_{ape(i)}} \quad (A.21)$$

Thus, equation (2.4) can be expressed as

$$\begin{aligned} C_{ap(i)}\dot{T}_{ap(i)}(t) &= \frac{1}{r_{op(i)}}T_{p(i)}(t) + \frac{1}{r_{ip(i+1)}}T_{p(i+1)}(t) \\ &+ \frac{1}{r_{agap(i)}}T_{ag(i)}(t) - \frac{1}{R_{ap(i)}}T_{ap(i)}(t) \end{aligned} \quad (A.22)$$

The state-space model matrix can be calculate as

$$\begin{aligned}
F_{apap}(i,i) &= -\frac{1}{C_{ap(i)}R_{ap(i)}}, \qquad 1 \le i \le N-1 \\
F_{app}(i,i) &= \frac{1}{C_{ap(i)}r_{op(i)}}, \qquad 1 \le i \le N-1 \\
F_{app}(i,i+1) &= \frac{1}{C_{ap(i)}r_{ip(i+1)}}, \qquad 1 \le i \le N-1 \\
F_{apag}(i,i) &= \frac{1}{C_{ap(i)}r_{agapp(i)}}, \qquad 1 \le i \le N-1
\end{aligned} \tag{A.23}$$

For the cartridge modeling, define

$$r_{c(i)} = \frac{1}{h_c A_{cs(i)}}, \qquad 1 \le i \le N \tag{A.24}$$

$$r_{ch(i)} = \frac{z_c/2k_c + z_h/2k_h}{A_{ch(i)}}, \qquad 1 \le i \le N \tag{A.25}$$

$$r_{ce(i)} = \frac{1}{h_c A_{ca(i)}}, \qquad 1 \le i \le N \tag{A.26}$$

$$\frac{1}{R_{c(i)}} = \frac{1}{r_{c(i)}} + \frac{1}{r_{pc(i)}} + \frac{1}{r_{ch(i)}} + \frac{1}{r_{ce(i)}} \tag{A.27}$$

Thus, Equation (2.5) can be expressed as

$$C_{c(i)}\dot{T}_{c(i)}(t) = \frac{1}{r_{pc(i)}}T_{p(i)}(t) + \frac{1}{r_{ch(i)}}T_{h(i)}(t) - \frac{1}{R_{c(i)}}T_{c(i)}(t) \tag{A.28}$$

The state-space model matrix can be calculate as

$$
\begin{aligned}
F_{cc}(i,i) &= -\frac{1}{C_{c(i)}R_{c(i)}}, && 1 \le i \le N \\
F_{cp}(i,i) &= \frac{1}{C_{c(i)}r_{pc(i)}}, && 1 \le i \le N \\
F_{ch}(i,i) &= \frac{1}{C_{c(i)}r_{ch(i)}}, && 1 \le i \le N
\end{aligned} \tag{A.29}
$$

For the heater modeling, define

$$
r_{h(i)} = \frac{1}{h_h A_{hs(i)}}, \qquad 1 \le i \le N \tag{A.30}
$$

$$
r_{he(i)} = \frac{1}{h_h A_{ha(i)}}, \qquad 1 \le i \le N \tag{A.31}
$$

$$
\frac{1}{R_{h(i)}} = \frac{1}{r_{h(i)}} + \frac{1}{r_{ch(i)}} + \frac{1}{r_{he(i)}} \tag{A.32}
$$

Thus, Equation (2.6) can be expressed as

$$
C_{h(i)}\dot{T}_{h(i)}(t) = \frac{1}{r_{ch(i)}}T_{c(i)}(t) - \frac{1}{R_{h(i)}}T_{h(i)}(t) \tag{A.33}
$$

The state-space model matrix can be calculate as

$$
\begin{aligned}
F_{hh}(i,i) &= -\frac{1}{C_{h(i)}R_{h(i)}}, && 1 \le i \le N \\
F_{hc}(i,i) &= \frac{1}{C_{h(i)}r_{ch(i)}}, && 1 \le i \le N
\end{aligned} \tag{A.34}
$$

Appendix A2: Centroid Calculation

In the system, the wafer is descritized as shown in Figure 3.4. Constrained by the TED's length, we have $\Delta x = \Delta y = 13.2$mm. To get the internal heat transfer equation of wafer, we need to calculate the area, centroid location of the squares.

For the regular squares, we have the area of the square is

$$A_{(i,j)} = \Delta x \Delta y \tag{A.35}$$

and the centroid of the square is

$$C_{x(i,j)} = (i - \frac{1}{2})\Delta x, C_{y(i,j)} = (j - \frac{1}{2})\Delta y \tag{A.36}$$

For the edge irregular squares, we need to calculate their area and centroid by integral equations.

1. Area calculation

For square (1,2)

$$\begin{aligned} A_{(i,j)} &= \int_{(i-1)\triangle x}^{i\triangle x} (\sqrt{R^2 - x^2} - (j-1)\triangle y) dx \\ &= \frac{1}{2}\triangle x[i\sqrt{R^2 - (i\triangle x)^2} - (i-1)\sqrt{R^2 - (i-1)^2(\triangle x)^2}] \\ &\quad + \frac{1}{2}R^2[\arcsin\frac{i\triangle x}{R} - \arcsin\frac{(i-1)\triangle x}{R}] - (j-1)\triangle y\triangle x \end{aligned} \tag{A.37}$$

For square (2,2)

$$\begin{aligned} A_{(i,j)} &= \int_{(i-1)\triangle x}^{\sqrt{R^2-(j-1)^2\triangle y^2}} (\sqrt{R^2 - x^2} - (j-1)\triangle y) dx \\ &= \frac{1}{2}R^2[\arccos\frac{(j-1)\triangle y}{R} - \arcsin\frac{(i-1)\triangle x}{R}] - \frac{1}{2}(j-1)\triangle y\sqrt{R^2 - (j-1)^2\triangle y^2} \\ &\quad - \frac{1}{2}(i-1)\triangle x\sqrt{R^2 - (i-1)^2\triangle x^2} - (j-1)(i-1)\triangle y\triangle x \end{aligned} \tag{A.38}$$

Since the wafer is symmetric, and $\triangle x = \triangle y$, we can get the area of squares with $i > j$ from $A_{(i,j)} = A_{(j,i)}$.

2. Centroid area (A_x)

For square (1,2)

$$\begin{aligned} A_{x(i,j)} &= \int_{(i-1)\triangle x}^{i\triangle x}\int_{(j-1)\triangle y}^{\sqrt{R^2-x^2}} x dy dx \\ &= \frac{1}{3}[(R^2 - (i-1)^2\triangle x^2)^{\frac{3}{2}} - (R^2 - i^2\triangle x^2)^{\frac{3}{2}}] - \frac{1}{2}[(2i-1)(j-1)\triangle y\triangle x^2] \end{aligned} \tag{A.39}$$

For square (2,2)

$$
\begin{aligned}
A_{x(i,j)} &= \int_{(i-1)\triangle x}^{\sqrt{R^2-(j-1)^2\triangle y^2}} \int_{(j-1)\triangle y}^{\sqrt{R^2-x^2}} xdydx \\
&= \frac{1}{3}[(R^2-(i-1)^2\triangle x^2)^{\frac{3}{2}} - ((j-1)\triangle y)^3] \\
&\quad + \frac{1}{2}[(i-1)^2(j-1)\triangle y\triangle x^2 - (j-1)\triangle y(R^2-(j-1)^2\triangle y^2)]
\end{aligned}
\tag{A.40}
$$

3. Centroid area (A_y)

For square (1,1)

$$
\begin{aligned}
A_{y(i,j)} &= \int_{(i-1)\triangle x}^{i\triangle x} \int_{(j-1)\triangle y}^{\sqrt{R^2-x^2}} ydydx \\
&= \frac{1}{2}[(R^2-(j-1)^2\triangle y^2)\triangle x - \frac{1}{3}[(3i^2-3i+1)\triangle x^3]
\end{aligned}
\tag{A.41}
$$

For square (2,2)

$$
\begin{aligned}
A_{y(i,j)} &= \int_{(i-1)\triangle x}^{\sqrt{R^2-(j-1)^2\triangle y^2}} \int_{(j-1)\triangle y}^{\sqrt{R^2-x^2}} ydydx \\
&= \frac{1}{3}[(R^2-(j-1)^2\triangle y^2)^{\frac{3}{2}} + \frac{1}{6}(i-1)^3\triangle x^3 - \frac{1}{2}(R^2-(j-1)^2\triangle y^2)(i-1)\triangle x
\end{aligned}
\tag{A.42}
$$

For square (7,16), (9,15), (10,14) and (12,13)

So, the centroid of the irregular squares can be get as

$$C_{x(i,j)} = \frac{A_{x(i,j)}}{A_{i,j}}, C_{y(i,j)} = \frac{A_{y(i,j)}}{A_{i,j}} \tag{A.43}$$

Since the circle is symmetric, and $\triangle x = \triangle y$, we have $C_{x(i,j)} = C_{y(j,i)}, C_{y(i,j)} = C_{x(j,i)}$. So we can easily get $C_{x(i,j)}$ and $C_{y(i,j)}$ of the squares with $i > j$.

To get the heat transfer equation inside the wafer, we also need to calculate the contact area of adjacent squares. Firstly, we will calculate the length of the contact area. For the regular inner squares, we have

$$l_{up} = l_{down} = \triangle x, l_{left} = l_{right} = \triangle y \tag{A.44}$$

For the marginal irregular squares with $i < j$, we have

$$\begin{aligned}
l_{i,j}^{left} &= \sqrt{R^2 - [(i-1)\triangle x]^2} - (j-1)\triangle y, if \quad l_{i,j}^{left} > \triangle y \longrightarrow l_{i,j}^{left} = \triangle y \\
l_{i,j}^{right} &= \sqrt{R^2 - (i\triangle x)^2} - (j-1)\triangle y, if \quad l_{i,j}^{right} < 0 \longrightarrow l_{i,j}^{right} = 0 \\
l_{i,j}^{down} &= \sqrt{R^2 - [(j-1)\triangle y]^2} - (i-1)\triangle x, if \quad l_{i,j}^{down} > \triangle x \longrightarrow l_{i,j}^{down} = \triangle x \\
l_{i,j}^{up} &= \sqrt{R^2 - (j\triangle y)^2} - (i-1)\triangle x, if \quad l_{i,j}^{up} < 0 \longrightarrow l_{i,j}^{up} = 0
\end{aligned} \tag{A.45}$$

Similarly, we have $l_{i,j}^{left} = l_{j,i}^{down}, l_{i,j}^{right} = l_{j,i}^{up}$. So we can easily get $l_{up}, l_{down}, l_{left}, l_{right}$ of the squares with $i > j$. And the contact area of adjacent squares can be calcu-

lated as

$$
\begin{aligned}
A_{i,j}^{left} &= l_{i,j}^{left} \times Z_w \\
A_{i,j}^{right} &= l_{i,j}^{right} \times Z_w \\
A_{i,j}^{up} &= l_{i,j}^{up} \times Z_w \\
A_{i,j}^{down} &= l_{i,j}^{down} \times Z_w
\end{aligned}
\tag{A.46}
$$

where Z_w is the thickness of the wafer.

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