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NATIONAL UNIVERSITY OF SINGAPORE

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Abstract

As CMOS transistors scale beyond the 45 nm technology node, ultra-thin equivalent oxide thickness less than 1 nm and enhanced effective saturation carrier velocity due to quasi-ballistic transport are required. Germanium MOSFET with high-κ gate dielectric provides a promising solution to continue improving the device performance. However, the replacement of silicon channel by germanium induces various material and process integration issues. This work has attempted to investigate the material properties and electrical performance of Ge MOSFET with a high-κ gate dielectric to access its feasibility as an alternative channel material.

The successful development of a high-κ gate stack on germanium is essential for Ge MOSFET. Two kinds of popular high-κ gate dielectric deposition approaches (PVD Hf oxynitride and ALD Al_2O_3 + NH_3 surface nitridation) were explored on germanium. The results show that the thermal budget of processing is critical for Ge device fabrication. A lower processing temperature than that of Si MOSFET fabrication is required by Ge MOSFET. Otherwise, the Ge device characteristics will deteriorate dramatically.

Germanium diffusion in high-κ gate dielectric is proposed as the root of Ge device degradation. The Ge incorporation in high-κ gate dielectric (e.g. HfO_2) occurs by two mechanisms: Ge atoms out-diffusion from Ge substrate and airborne GeO transportation. When oxygen is present, the germanium incorporates into HfO_2 in the

form of oxide and, in turn, forms a new dielectric ($Hf_{1-x}Ge_xO_2$). $Hf_{1-x}Ge_xO_2$ has a similar dielectric constant to that of HfO_2 but has a high interface state density which will degrade the MOSFET performance.

The fabrication of heavily doped, shallow junctions in the source and drain regions of a transistor presents another significant process integration challenge. This task is more challenging for Ge nMOSFET. Laser annealing was introduced as a superior source/drain activation technique. By applying an aluminum laser reflector on the metal gate electrode, S/D regions of MOSFET were selectively annealed without heating gate stack. Good gate stack integrity, shallow junction depth and small S/D series resistance were achieved simultaneously.

The self-aligned germanide is investigated to further reduce the source/drain series resistance of Ge MOSFETs. The formation and thermal stability of nickel germanide on germanium substrate were systematically examined. Improved drive current of Ge diode with NiGe contact was demonstrated without degrading leakage current.

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List of Symbols

A	Area
C	capacitance (F)
C_{hf}	high frequency capacitance (F/cm^2)
C_{it}	interface state capacitance (F)
C_{lf}	low frequency capacitance (F/cm^2)
C_{ox}	oxide capacitance (F)
C_s	semiconductor capacitance (F)
d	thickness
D_{it}	density of interface states
E	energy (eV)
ε	electrical field (V/cm)
G	conductance
h	Planck's constant (6.626×10^{-34} J s)
I	current (A)
I_d	drain current (A)

I_g	gate leakage current (A)
J	current density (A/cm^2)
L	channel length (μm)
m^*	effective mass (kg)
n	refractive index
n	electron density (cm^{-3})
p	hole density (cm^{-3})
Q	charge (C)
r_s	series resistance (ohms)
R_s	sheet resistance
T	temperature
t	time
V	voltage (V)
V_d	drain voltage (V)
V_g	gate voltage (V)
V_{fb}	flatband voltage (V)
V_{inj}	injection carrier velocity
V_{th}	threshold voltage (V)
W	channel width (μm)

ε_0	permittivity of free space (8.854 x 10^{-14} F/cm)
ϕ_B	barrier height (eV)
λ	wavelength (cm)
κ	dielectric constant
μ	mobility (cm^2 /Vs)
τ	lifetime (s)
τ	time constant (s)
Ψ	ellipsometric angle
Δ	ellipsometric angle

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Chapter 1

Introduction

1.1 Scaling of MOSFETs

Since the invention of metal oxide semiconductor field-effect transistor (MOSFET) in 1940s, the rapid development of integrated circuit (IC) fabrication has led to unprecedented levels of growth in semiconductor industry. Among the whole semiconductor industry, the major contribution comes from the integrated circuit made by complementary metal oxide semiconductor (CMOS) field-effect transistor technology. In the past decades, the performance and complexity of CMOS integrated circuit are continuously improved by scaling the device to smaller dimensions. The scaling of MOSFET device was originally predicted by Gordon Moore in 1965 [1.1]. Benefiting from the dramatic progress in lithography, the minimum feature size of MOSFET has scaled from several microns in 1970's to sub-100 nm today. Through the years, the scaling of MOSFET to smaller dimensions has been governed by a delicate scaling criteria proposed by Dennard *et al* in 1974 [1.2]. The key concept is that various structural and electrical parameters of the MOSFET (such as gate length, gate width, gate oxide thickness and power supply voltage) should be scaled in concert, which guarantees the reduction in device dimensions without compromising the current-voltage characteristics. The improved performance associated with the scaling of device dimensions can be seen by considering a simple model for the drive current associated with a MOSFET. The drive current can be written as

$$I_d = \mu_{eff} C_{eff} \frac{W}{L}(V_g - V_{th} - V_d / 2)V_d , \quad (1.1)$$

where W is the width of the transistor, L is the channel length, μ_{eff} is the channel mobility, C_{eff} is the gate capacitance, V_g and V_d are the voltages applied to the transistor gate and drain, respectively, and the threshold voltage is given by V_{th}. Apparently, a reduction in the channel length or an increase in the channel mobility or gate capacitance will result in an increased I_d. The gate capacitance could be considered as a parallel plate capacitor (ignoring quantum mechanical and depletion effects from Si substrate and gate)

$$C = \frac{\kappa \varepsilon_0 A}{t}, \quad (1.2)$$

where κ is the dielectric constant of the gate dielectric, and t is the thickness. Obviously, to obtain a large capacitance, the dielectric thickness is needed to scale down.

The future scaling of MOSFET is predicted by the international technology roadmap of semiconductor (ITRS) by Semiconductor Industry Association (SIA) [1.3]. The technology requirement table in ITRS includes the transistor requirements of both high-performance and low-power digital ICs. High-performance logic refers to chips of high complexity, high performance, and high power dissipation, such as microprocessing unit (MPU) chips. On the contrary, low-power logic refers to chips for mobile systems etc, where the allowable power dissipation and hence the allowable leakage currents are limited by the battery life. The transistors for high-performance have the highest performance, largest leakage current and stand for the most aggressively scaled device.

Table 1.1. ITRS technology requirement table for high performance technology

Year of Production	2004	2007	2010	2013	2016
Technology Node	hp90	hp65	hp45	hp32	hp22
DRAM 1/2 Pitch (nm)	**90**	**65**	**45**	**32**	**22**
MPU/ASIC $^1/_2$ Pitch (nm)	**90**	**65**	**45**	**32**	**22**
MPU Physical Gate Length (nm)	**37**	**25**	**18**	**13**	**9**
EOT: equivalent oxide thickness (physical) for high-performance (nm)	**1.2**	**0.9**	**0.7**	**0.6**	**0.5**
Nominal gate leakage current density limit (at 25°C) (A/cm^2)	**4.5E+2**	**9.3E+2**	**1.9E+3**	**7.7E+3**	**1.9E+4**
Nominal high-performance NMOS sub-threshold leakage current , $I_{sd,leak}$ (at 25 °C)(mA/um)	**0.05**	**0.07**	**0.1**	**0.3**	**0.5**
Nominal power supply voltage (V_{dd}) (V)	**1.2**	**1.1**	**1**	**0.9**	**0.8**
Required "mobility/transconductance improvement" factor	**1.3**	**2**	**2**	**2**	**2**
Effective saturation carrier velocity enhancement factor (due to quasi-ballistics transport)	**1**	**1**	**1.1**	**1.1**	**1.3**

Manufacturable solution exist, and are being optimized

Manufacturable solution are known

Manufacturable solution are NOT known

Table 1.1 shows the ITRS technology requirement table for high performance technology. Current mainstream high performance 90 nm technology requires a small physical gate length of 37 nm and a low equivalent oxide thickness (EOT) of 1.2 nm. It also allows high leakage currents which include gate leakage current ($4.5x10^2$ A/cm^2) and sub-threshold leakage current (0.05 mA/μm). ITRS has predicted that the gate length and EOT will shrink rapidly to 9 nm and 0.5 nm respectively in the 22 nm technology node in year 2016. As highlighted in Table 1.1, such an ultra-small EOT cannot be achieved with any known manufacturable solution. Novel technology with alternative gate dielectric must be employed to ensure the continual scaling of CMOS technology.

In addition to the rapid scaling of gate length and EOT, mobility/ transconductance enhancement is needed since year 2004 to meet the required MOSFET saturation current value. And in highly scaled, ultrathin body MOSFETs, particularly with multigate, quasi-ballistic operation with enhanced thermal velocity injection at the source is required in order to meet the saturation current target. Therefore, it is necessary to explore novel channel materials with high mobility and thermal velocity injection.

1.2 High-κ Gate Dielectric

Although the use of thermally grown amorphous silicon dioxide as gate dielectric of MOSFET offers several key advantages including superior thermal stability, high-quality SiO_2/Si interface and large bandgap, traditional SiO_2 cannot meet the requirement of further scaling of MOSFETs.

Theoretic modeling as well as experiment results show that a minimum of 7 Å of SiO_2 is required to maintain the full SiO_2 bandgap [1.4][1.5][1.6]. It sets up an

absolute physical thickness limit of the scaling of SiO_2.

It has been experimental proved that the inherent bandgap of SiO_2 remains even down to only a few monolayers of materials. MOSFETs with gate oxides as thin as 13-15 Å continue to work satisfactorily [1.7]. Despite a huge gate leakage current was observed, it is still sustainable for high performance technology. However, MOSFETs with SiO_2 gate oxides thinner than about 10-12 Å resulted in no further gain in transistor drive current [1.8]. This result gave out a practical limit for scaling the SiO_2 thickness.

In addition to leakage current increasing with scaled oxide thickness, the issue of boron penetration through gate dielectric is another concern. In CMOS process, heavily boron doped polysilicon is used as gate electrode for pMOSFET. Therefore, there is a high boron concentration gradient between polysilicon gate, gate oxide and substrate. Upon thermal annealing, the boron from polysilicon could easily diffuse through the thin gate oxide into substrate owing to the low atomic mass and small size of boron. Boron penetration caused threshold voltage shift and concern in the reliability of the device [1.9].

The concerns regarding high leakage current and boron penetration of ultrathin SiO_2 have led to the use of silicon oxynitride. The silicon oxynitride has a relative higher dielectric constant than silicon dioxide (Si_3N_4 has a dielectric constant ~ 7), hence a film with large physical thickness which reduces leakage current. And introducing nitrogen into silicon dioxide greatly reduces the boron diffusion through dielectric benefited from the Si-O-N networking bond formed in silicon oxynitride [1.10][1.11]. Despite the encouraging result of silicon oxynitride, the scaling of silicon oxynitride is limited and therefore would make it relatively short-term solution for industry's need. According to ITRS roadmap, the EOT in the current 90 nm high performance technology node is 1.2 nm and it is expected to reach 0.5 nm in the year

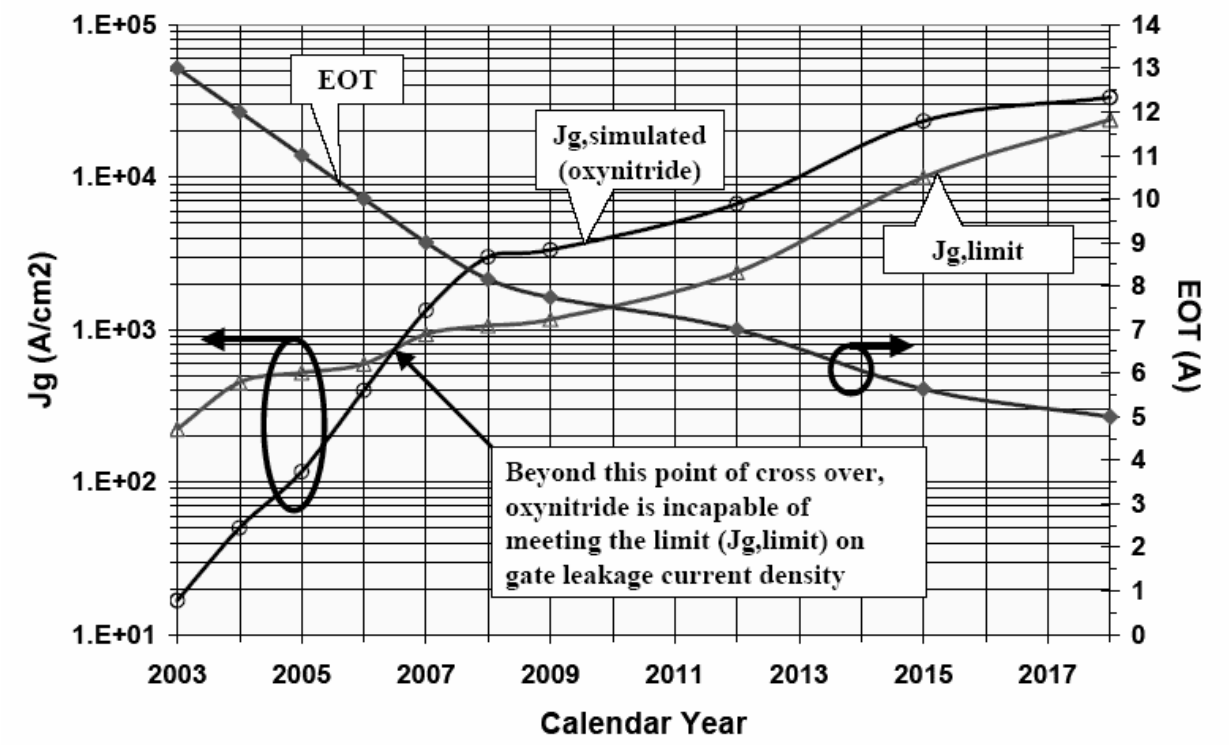

Figure 1.1. Leakage current requirement of high performance technology and simulated gate leakage current of oxynitride by ITRS [1.3].

of 2016 [1.3]. In this ultra thin EOT regime, the gate leakage current is dominant by direct tunneling and hence the gate leakage current increases exponentially with decreasing EOT. Figure 1.1 shows the simulated gate leakage current of silicon oxynitride due to direct tunneling at each technology node with scaled V_{dd} and EOT [1.3]. The gate leakage current limit requirement (Jg, limit) of gate dielectric at each technology node are also plotted for reference. It was found that the two Jg lines (simulation result and leakage limit) cross just before year 2007 and hence for the year 2007 and beyond, the gate leakage current limit requirement cannot be met using silicon oxynitride when EOT becomes approximately 9 Å. Novel gate dielectric such as high-κ material is suggested to replace the traditional silicon dioxide and silicon oxynitride since 2007.

The alternative gate dielectric such high-κ materials must meet a set of criteria to perform as a successful gate dielectric [1.12]. The following lists the minimum

requirements for high-κ dielectric in the transistor application:

1. Permittivity and barrier height
2. Thermodynamic stability
3. Interface quality
4. Film morphology

1.2.1 Permittivity and barrier height

Selecting a gate dielectric with a higher dielectric constant than that of SiO_2 is clearly essential from Equation 1.2. The increasing of the gate capacitance could be achieved by either decreasing oxide thickness or increasing dielectric constant. For an example, a dielectric with a relative permittivity of 16 hence affords a physical thickness of ~40 Å to obtain an EOT of 10 Å. Therefore, a larger permittivity is more favorable for highly scaled MOSFET with ultrathin EOT. However, the permittivity of alternative gate dielectric is limited due to fringing field induced barrier lowering (FIBL) at the drain region of the device. Frank *et al* modeled gate dielectrics with various permittivities in a planar, bulk CMOS structure to predict the effect of high-κ gate dielectric on transistor performance [1.13]. An upper limit of κ~20 was reported to prevent a significant fringing field from the edge of a high-κ dielectric, which in turn lowered the barrier for transport into the drain and degraded the transistor on/off characteristics seriously. Krishnan *et al* reported similar modeling results for high-κ dielectric but also claimed that the FIBL problem with high-κ dielectric could be relieved with a SiO_2 interface layer between high-κ dielectric and substrate channel [1.14].

The selection of high-κ dielectric with appropriate barrier height is also important. As the gate dielectric thickness scales below 35 Å, the dominant

conduction mechanism of leakage current through gate dielectric changes from Fowler-Nordheim (FN) tunneling to direct tunneling. The tunneling current of direct tunneling is given by the expression

$$I_{dir} = A_G A \varepsilon_{ox}^2 \exp\left(\frac{-B[1-(qV_{ox}/\phi_B)^{1.5}]}{\varepsilon_{ox}}\right) \quad (1.3)$$

where A_g is the gate area, A and B are usually considered to be constants, ε_{ox} and V_{ox} are the electrical field and voltage drop cross the gate oxide. Since the direct tunneling current increases exponentially with decreasing barrier height ϕ_B, it is essential to ensure an enough high barrier height to reduce carrier tunneling transport. Robertson and Chen summarized the barrier height of many high-κ materials [1.15]. As shown in Fig. 1.2, some high permittivity materials such as Ta_2O_5 have small conduction band

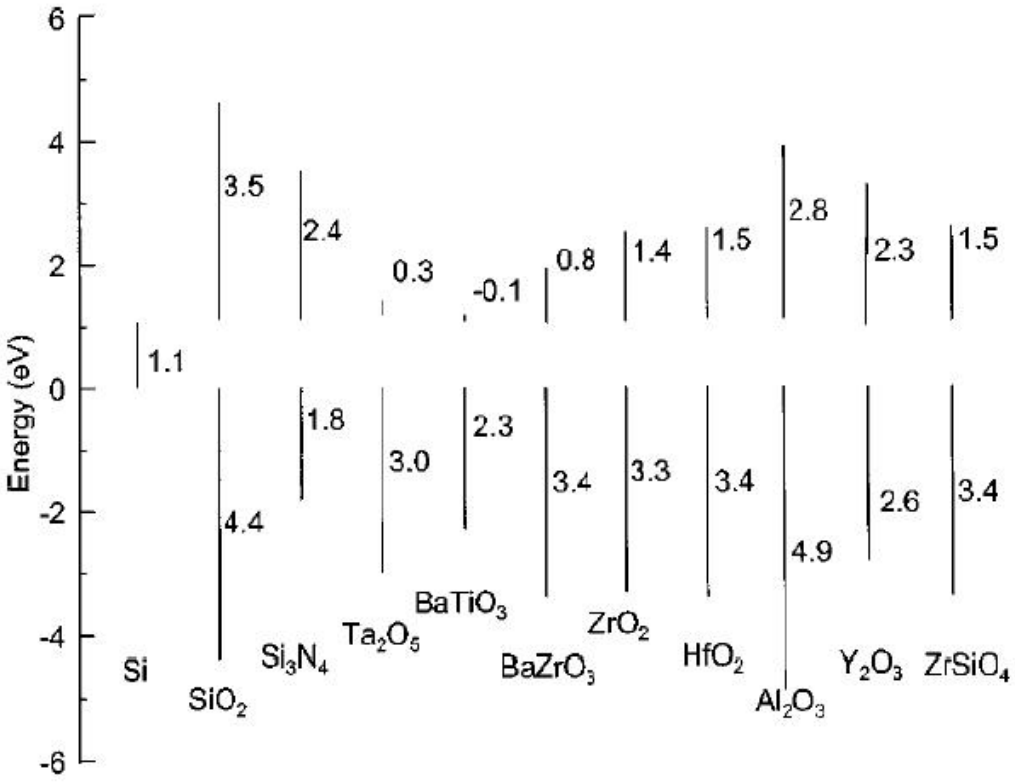

Figure 1.2. Band offset calculations for a number of potential high-κ gate dielectric materials [1.15].

barrier heights less than 1.0 eV, the electron transport by either thermal emission or tunneling would be unacceptably high and precludes using these oxides as gate dielectrics. In addition, a small barrier height leads to steep slope of leakage current versus thickness curve than that of silicon dioxide [1.16]. It limits the scalability of materials to ultra-thin EOT regime. Therefore, large barrier heights for both conduction band and valence band (e.g. large bandgap) are desirable for high-κ dielectric. However, in contrast to the trend of increasing permittivity with increasing atomic number, the bandgap of the metal oxide tends to decrease with increasing atomic number [1.17]. Therefore, a trade-off between permittivity and bandgap must be well balanced when selecting a suitable high-κ gate dielectric.

1.2.2 Thermodynamic stability

Another important consideration in the selection of an alternative gate dielectric is its thermodynamic stability in contact with the substrate. A number of metal oxide materials were reported to be unstable with silicon after high temperature annealing during processing. The reaction leads to the formation of interfacial silicide, silicate or SiO_2 layer and consequently degrades the device performance. Therefore, it is important to understand and predict the thermodynamics of alternative gate dielectric/substrate system. A method of calculating Gibbs free energy was used to predict possible reaction between binary metal oxide and silicon. Any reaction leading to a lowering of Gibbs free energy ($\Delta G<0$) implies that the interface between these oxide and silicon is thermodynamically unstable. Hubbard *et al* did an extensively study on many potential oxide materials for alternative gate dielectric with this method [1.18]. The results excluded the possibility of many oxide materials as gate dielectric such as Ta_2O_5, Ti_2O_5 since these materials are unacceptable for integration

with silicon. Potential candidate material including Al_2O_3, HfO_2, ZrO2 etc were suggested.

1.2.3 Interface engineering

The interface between substrate and gate dielectric plays the most important role and its thickness and quality are the dominant factors determining the overall electrical properties. The thickness and dielectric constant of interfacial layer affect the EOT of the whole gate stack significantly. The contribution of interfacial layer to the final EOT can be easily seen from Equation 1.4, considering a device with a high-κ dielectric layer and a low-κ interfacial layer beneath.

$$EOT = \frac{\kappa_{IL}}{\kappa_{SiO_2}} \bullet t_{IL} + \frac{\kappa_{high-\kappa}}{\kappa_{SiO_2}} \bullet t_{high-\kappa} \qquad (1.4)$$

It is clear that the minimum EOT is limited by the thickness (t_{IL}) and dielectric constant (K_{IL}) of the interfacial layer. If a thick and SiO_2-like interfacial layer exists between the high-κ dielectric layer and substrate, much of the expected decrease in the EOT associated with high-κ dielectric is compromised. In addition, the quality of interface determines the density of interface states (D_{it}) and hence affects the mobility. A high quality interface with D_{it} as low as SiO_2/Si ($2x10^{10}$ $eV^{-1}cm^{-2}$) is desired.

The thickness and quality of interfacial layer are closely related with process conditions including surface treatment, high-κ deposition methods, and thermal cycles undergone after high-κ deposition etc. A thick interfacial layer between high-κ dielectric and silicon substrate is commonly observed for directly high-κ deposition on bare silicon [1.19][1.20]. And the interfacial layer continues to grow during the subsequent thermal processes, in particular, post-deposition annealing and source/drain activation annealing. Surface nitridation prior to high-κ deposition is

recognized as an effective method to suppress the formation of interfacial layer [1.21]. However, accumulation of nitrogen near the interface increases the D_{it} and therefore results in mobility degradation. A high D_{it} on the order of 10^{11} - 10^{12} $eV^{-1}cm^{-2}$ was commonly observed in the device with surface nitridation. Recently, several research groups proposed to intentionally grow a thin chemical or thermal SiO_2 dioxide prior to high-κ deposition [1.22]. Much improved D_{it} and mobility close to that of SiO_2/Si system were achieved. However, this approach will severely compromise the capacitance gain from any high-κ layer in the gate stack.

1.2.4 Film morphology

Unlike SiO_2 or oxynitride which has a very high crystallization temperature, most metal oxide films examined to date appear to be polycrystalline, as growth or after moderately low temperature annealing. Polycrystalline dielectrics may be deleterious to device performance, as the existence of grain boundaries may serve as boron diffusion and high leakage paths through the oxide. In addition, changes in the grain size and orientation throughout the whole polycrystalline film may lead to non-uniformity in κ value and film thickness. Thus, it appears that amorphous film structure is the ideal one for the gate dielectric. It was found that adding nitrogen, aluminum and silicon into HfO_2 can effectively increase the crystallization temperature so that the film remains amorphous after going throughout the necessary thermal processing [1.23][1.24][1.25].

1.3 Germanium Channel Transistor

1.3.1 Advantages of germanium as alternative channel material

As indicated in Section 1.1, further scaling of MOSFETs requires the scaling of device dimensions as well as the channel mobility enhancement. Novel channel materials such as germanium or III-V provide potential solution for mobility enhancement. Table 1.2 lists the properties of common semiconductor materials.

Table 1.2. Properties of common semiconductor materials.

	Si	Ge	GaAs	InAs	InSb
Electron mobility (cm^2/Vs)	1400	3900	8000	33000	77000
Hole mobility (cm^2/Vs)	470	1600	340	460	1000
Bandgap (eV)	1.12	0.67	1.42	0.36	0.17
Melting point (K)	1685	1231	1510	1215	798

Among these materials, germanium is the only material that provides mobility enhancements for both electron and hole with an appropriate bandgap and melting point. Germanium offers about two times higher electron mobility and four times higher hole mobility than that of silicon, which satisfies the ITRS transconductance/mobility enhancement requirement.

In addition, germanium is suitable for highly scaled transistor working in quail-ballistics transport operation. It is expected for MOSFETs with ultra-short gate length

less than 20 nm that carriers flowing from source to drain region encounter little scatterings inside channel and, thus, are dominated by ballistic transport, where injection carrier velocity at the source edge, V_{inj} determines the drive current. Low effective mass along channel orientation is necessary in order to obtain high injection velocity at the source end of the channel. Compared with Si, Ge has smaller carrier transport mass and gap energy, giving rise to higher drive current I_{on} but also higher tunneling leakage I_{off}. Encouraging results were reported from several research groups by quantum simulation to access the prospect of germanium channel in highly scaled advanced MOSFETs [1.26][1.27] [1.28]. Low *et al* examined the performance limit and engineering issues of ultra-thin body double gate Ge channel nMOSFETs with different orientations [1.28]. Ge <110> channel exhibits highest I_{on} which increases with body thickness scaling. Band to band (BTB) tunneling due to the small bandgap of germanium imposes a limit on standby current I_{off} and it can be effectively suppressed by body scaling. A superior performance is obtained in engineered Ge <110 > device compared with silicon.

III-V materials like GaAs, InAs and InSb are also considered as the channel material for high performance nMOSFETs whereas not recommended for pMOSFETs. It is vague whether germanium or III-V material exhibits best nMOSFET performance. To the author's best knowledge, only two reports existed in the literature, which gave out contrary conclusions. Results of Pethe *et al* show that large bandgap III-V material GaAs outperforms other III-V materials and Ge which suffer from excessive BTB tunneling [1.29]. However, Rahman *et al* claimed that III-V materials offered no performance advantage at the scaling limit since very low conduction band density-of states compromised the high electron injection velocity [1.30]. Due to high density-of-states for both electrons and holes in Ge, germanium is found to be the best choice for CMOS application.

1.3.2 Gate dielectric development for germanium MOS device

Historically, germanium has been one of the most important semiconductor materials in the past as the first MOSFET and integrated circuit were fabricated in Ge [1.31][1.32]. On the other hand, oxides of Ge (GeO and GeO_2) are known to be hygroscopic and water-soluble, which hinder the processing and application Ge MOS device. Complex process such as nitridation to thermal growth Ge oxide was developed to improve the quality of germanium oxide for Ge MOSFET fabrication. Rosenberg and Martin reported germanium MOSFETs using thick (250 Å) germanium oxynitride insulator [1.33] [1.34]. A dummy gate process was utilized to realize self-alignment. High electron and hole mobility was estimated as 940 $cm^2/V*s$ and 770 $cm^2/V*s$ respectively. In their following work, the hole mobility of was improved to 1050- $cm^2/V*s$ with reducing gate dielectric thickness to 220 Å [1.35]. Jackson *et al* reported gate-self-aligned p-channel germanium MOSFET [1.36]. The gate dielectric was formed by nitridation of thermally grown germanium oxide. The final dielectric was expected to be 21 nm essentially stoichimetric Ge_2N_2O. An hole mobility of 640-$cm^2/V*s$ was calculated. And they also published both n- and p-channel devices with mobility greater than 1000 $cm^2/V*s$ in the subsequent work [1.37].

In all of works above, the gate dielectric thickness is quiet large, which is not suitable for modern VLSI technology. In a recent report by Shang *et al*, the EOT was successfully reduced to ~8 nm with thin germanium oxynitride [1.38]. The gate stack consisted with 6 nm Ge oxynitride and 3nm low temperature Si oxide. An excellent subthreshold slope of 82 mV/dec was achieved. Hole mobility was enhanced by about 40% compared to the Si control.

Chi On Chui *et al* studied germanium MOS capacitors and MOSFETs with

high-κ gate dielectric (zirconium oxide) for the first time. A record low EOT of 5–8 Å has been demonstrated by both of p-channel and n-channel MOS capacitors with a huge gate leakage current at 3.3 A/cm^2 [1.39]. And Ge pMOSFET with an EOT of 6-10 Å has been also demonstrated [1.40]. However, suffered from the huge leakage, the MOSFETs in their work cannot achieve a normal turn-on and turn-off characteristics. The peak effective hole mobility was 313 cm^2/V*s.

1.3.3 Junction formation on germanium

Advanced MOSFET structure requires a shallow and low resistance source/drain junction. In contrast to the situation in silicon, the task of achieving shallow junction is more challenging for Ge nMOSFET than pMOSFET since the high diffusivity and activation temperature of n-type dopants. N-type dopants (phosphorus, arsenic, antimony) diffuse fast in germanium while p-type dopant (boron) has a relative small diffusivity in germanium [1.41]. Besides, n-type dopants require a higher temperature annealing (600 ^{o}C) than p-type dopants (350 ^{o}C) to repair the defect in germanium induced by the ion implantation [1.42]. In addition to be very shallow, the source/drain regions also need to be heavily doped to reduce the S/D series resistance. However, n-type dopant has a poor activation rate in germanium. A large fraction of implanted dosage of dopant loses after rapid thermal annealing [1.43]. Large series resistance due to poor activation was observed in recent reported Ge nMOSFET and limited the performance [1.42].

1.4 Motivation of Thesis

The goal of this thesis to develop high performance germanium MOSFET with high-κ gate dielectric, which features with low EOT, low gate leakage current and

enhanced mobility to provide a potential solution for future CMOS technology.

One of the critical challenging is the thermal stability of high-κ gate stack on germanium. Since the high-κ gate dielectric is subject to several high temperature annealings during the device fabrication, it must be thermal stable without any degradation in electrical performance. Since post deposition annealing and source/drain activation annealing (post metal annealing) employ the highest process temperature in the process flow, it is crucial to evaluate the thermal stability of high-κ/Ge upon them. During the research of high-κ dielectric on silicon, it has been widely reported that noticeable degradation in EOT and other electrical properties happens after PDA and PMA. For germanium device, severe flatband voltage shift was observed with Ge oxynitride gate dielectrics [1.42]. Therefore, it is necessary to investigate the effect of high temperature annealing on electrical properties of high-κ dielectric on germanium. In addition, it is important to study the root cause of performance degradation after annealing.

Another critical challenging to develop high mobility Ge MOSFET is the formation of source/drain junction. First of all, the source/drain must be formed without degrading the gate stack. Furthermore, source/drain must be heavily doped with a low sheet resistance to reduce series resistance. A high source/drain series resistance degrades the drain current and consequently it results in an underestimated channel mobility. Additionally, for MOSFET with small gate length, the junction depth should be well controlled to suppress short channel effect. In this thesis, a novel approach by using laser annealing to activate source/drain is presented. High dopant activation rate without dopant loss as well as maintaining good gate stack integrity is achieved by this approach.

Although advanced annealing such as laser annealing is able to improve the activation efficiency and reduce the sheet resistance effectively, the source/drain

series resistance is still not low enough and it compromises the drive current. Self-aligned silicide contact is an essential component of modern MOSFET structure to reduce S/D series resistance. Nickel silicide is considered as the material choice for the future technology nodes replacing titanium silicide and cobalt silicide which are used in sub-micron and sub-0.25 μm nodes. Similarly, Ni shows advantages to form germanide for Ge MOSFET application over other materials. It has been reported that high processing temperatures are required to form low-resistivity titanium germanide (>800 ^{o}C) and cobalt germanide (>500 ^{o}C), while nickel germanide can be formed at a low temperature of 270 ^{o}C [1.44]. Such a low processing temperature is effective to prevent the degradation of high-κ gate stack on germanium substrate and makes nickel germanide more suitable for Ge device fabrication. In this thesis, the formation and thermal stability of nickel germanide are studied. Enhanced drive current benefited from reduced series resistance is observed on germanium junction with nickel germanide contact.

1.5 Organization of Thesis

The remainder of this thesis has been organized as follows. Chapter Two shows the preliminary results of the electrical performance of high-κ/Ge MOS devices. A high hole mobility which exceeds the SiO_2/Si universal curve has been demonstrated. In addition, the thermal stability of high-κ/Ge upon PDA and PMA is studied. Severe degradation of capacitance-voltage characteristic and increased leakage current after high temperature post metal annealing is observed. Germanium out-diffusion from substrate into high-κ dielectric is believed to be responsible for the degradation. Chapter Three investigates the germanium out-diffusion mechanism in high-κ HfO_2 dielectric with details. The effect of high-κ dielectric deposition methods and post

deposition annealing conditions on germanium incorporation in HfO_2 is presented. And the impacts of germanium incorporation on electrical properties of HfO_2 such as dielectric constant and interface state density are investigated. Since the source/drain activation by the conventional rapid thermal annealing method requires a high temperature which degrades the gate stack as shown in the previous chapters, in Chapter Four, a novel laser annealing source/drain activation is developed. By employing nano-seconds high temperature laser annealing to melt the source/drain regions into liquid, the dopants are frozen into germanium lattice and fully activated. Additionally, with an aluminum laser reflector on the gate electrode, the source/drain regions are selectively annealed without heating gate stack. As a result, good gate stack integrity and fully activation of S/D are achieved. Chapter Five addresses the formation of nickel germanide as source/drain contact to further reduce series resistance and improve drive current. The appropriate annealing temperature for nickel germanide formation is defined. The NiGe film degrades after high temperature annealing and it is ascribed to film agglomeration. The activation energy of agglomeration is extracted. An optical model is created to measure the thickness of NiGe and monitor the agglomeration of NiGe. Chapter Six concludes the thesis by summarizing the results obtained and the contributions made to the field along with suggestions for future work in related areas.

References

[1.1] Gordon Moore, “Cramming more components onto integrated circuits,” Electronics, vol. 38, no. 8, April 1965.

[1.2] R.H. Dennard, F. F. Gaensslen, Nwa-Nien Yu, V. L. Rideout, E. Bassous, A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” IEEE J. Solid-State Circuits, vol. SC-9, p. 256, 1974.

[1.3] International Technology Roadmap for Semiconductors (ITRS) 2004, Semiconductor Industry Assoc., San Jose, CA., Available: http://www.itrs.net/Common/2004Update/2004Update.htm.

[1.4] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, “The electronic structure at the atomic scale of ultrathin gate oxides,” Nature (London), vol. 399, 758, 1999.

[1.5] J. B. Neaton, D. A. Muller and N. W. Ashcroft, Phys. Rev. Lett., “Electronic properties of the Si/SiO_2 interface from first principles,” vol. 85, pp. 1298, 2000.

[1.6] S. Tang, R. M. Wallace, A. Seabaugh, and D. King-Smith, “Evaluating the minimum thickness of gate oxide on silicon using first-principles method,” Appl. Surf. Sci., v.135, pp.137, 1998.

[1.7] H. S. Momose, M. Ono, T. Yoshitoi, T. Ohguro, S.-I. Nakamura, M. Saito, and H. Iwai, “1.5 nm direct-tunneling gate oxide Si MOSFET's,” IEEE Trans. Electron Devices, v. 43, pp.1233, 1996

[1.8] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, M. Green, “Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm nMOSFETs,” Tech. Dig. Int. Electron Devices Meet. 1997, p. 930, 1997.

[1.9] M. Chao, P. V. Voorde, M. Cox and W. Green, "Boron diffusion and penetration in ultrathin oxide with poly-Si gate," IEEE Electron Device Lett., vol. 19, pp. 291-293, 1998.

[1.10] Y. Wu, G. Lucovsky and Y. M. Lee, "The performance and reliability of PMOSFET's with ultrathin silicon nitride/oxide stacked gate dielectrics with nitrided Si-SiO_2 interfaces prepared by remote plasma enhanced CVD and post-deposition rapid thermal anneal," IEEE Tran. Electron Dev., vol. 47, pp. 1361-1369, 2000.

[1.11] T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato and D. L. Kwong, "Engineering of nitrogen profile in an ultrathin gate insulator to improve transistor performance and NBTI," IEEE Electron Device Lett., vol. 24, pp. 150-152, 2003.

[1.12] G. D. Wilk, R. M. Wallace, J. M. Anthony, "High-κ gate dielectrics: current status and materials properties considerations," J. Appl. Phys., v. 89, pp. 5243, 2001.

[1.13] D. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," IEEE Electron Device Lett., v.19, pp. 385 1998.

[1.14] S. Krishnan, G. C.-F. Yeap, B. Yu, Q. Xiang, and M.-R. Lin, "high-κ scaling for gate insulators: an insightful study," Proc. SPIE, 3506, pp. 65, 1998.

[1.15] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," J. Vac Sci. Technol., B 18, pp. 1785, 2000.

[1.16] Y. C. Yeo, T. J. King and C. Hu, "Direct tunneling leakage current and scalability of alternative gate dielectrics," Appl. Phys. Lett., vol. 81, pp. 2091-2093, 2002.

[1.17] S. A. Campbell, D. C. Gilmer. X.-C. Wang, M.-T. Hsieh, H.-S. Kim, W. L.

Gladfelter and J. Yan, "MOSFET Transistors Fabricated with High Permittivity TiO2 Dielectrics," IEEE Tran. Electron Dev., vol. 44, pp. 104-109, 1997.

[1.18] K. J. Hubbard and D. G. Schlom, "Thermodynamic stability of binary oxides in contact With silicon," J. Mater. Res., V. 11, pp. 2757, 1996.

[1.19] Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Tat Ngai, Sanjay Banerjee, and Jack C. Lee, "MOSCAP and MOSFET characteristics using ZrO2 gate dielectric deposited directly on Si,". Tech. Dig. Int. Electron Devices Meet., pp.145, 1999.

[1.20] H.F. Luan, S.J. Lee, C.H. Lee, S.C. Song, Y.L, Mao, Y. Senzaki, D. Roberts, and D.L. Kwong, "High Quality Ta_20_5 Gate Dielectrics with $T_{ox.eq}$<10A," Tech. Dig. Int. Electron Devices Meet., p.141, 1999.

[1.21] Rino Choi. Chang Seok Kang. Byoung Hun Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, J.C. Lee, "High-quality ultra-thin HfO_2 gate dielectric MOSFETs with TaN electrode and nitridation surface preparation," VLSI Tech.Dig. 2001, p. 15, 2001.

[1.22] L. Pantisano, E. Cartier, A. Kerber, R. Degraeve, M. Lorenzini, M. Rosmeulen, G. Groeseneken and H. E. Maes, "Dynamics of Threshold Voltage Instability in Stacked high-κ Dielectrics: Role of the Interfacial Oxide," Symp. VLSI Technology, pp. 163-164, 2003.

[1.23] C.S. Kang, H.J.Cho, R. Choi, Y.H. Kim, C.Y Kang, S.J Rhee, C. Choi, M.S. Akbar, and Jack C. Lee, "The electrical and material characterization of hafnium oxynitride gate dielectrics with TaN-gate electrode," IEEE Trans. Electron Device, Vol. 51, No. 2, pp. 220-227, 2004.

[1.24] M.S. Joo, B.J. Cho, C.C Yeo, S.H. Chan, D.; S.J. Whoang, S. Mathew, L.K. Bera, N. Balasubramanian, D.-L Kwong, "Formation of hafnium-aluminum-

oxide gate dielectric using single cocktail liquid source in MOCVD process," IEEE Trans. Electron Device, Vol. 50, pp. 2088-2094, 2003.

[1.25] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, A. Nishiyama, "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics," in IEDM Tech. Dig., pp. 849 – 852, 2002.

[1.26] Shin-ichi Takagi, "Re-examination of subband structure engineering in ultra-short channel MOSFETs under ballistics carrier transport," VLSI Tech.Dig. 2003, pp, 115, 2003.

[1.27] Anisur Rahman, Avik Ghosh, and Mark Lundstrom, "Assessment of Ge n-MOSFETs by Quantum Simulation," Tech. Dig. Int. Electron Devices Meet. 2003, pp. 471, 2003.

[1.28] Tony Low, Y. T. Hou, M. F. Li, Chunxiang Zhu, Albert Chin, G. Samudra, L. Chan, and D. –L. Kwong, "Investigation of performance limits of germanium double-gated MOSFETs," Tech. Dig. Int. Electron Devices Meet. 2003, pp. 691, 2003.

[1.29] Abhijit Pether, Tejas Krishnamohan, Donghyun Kim, Saeroonter Oh, H. –S. Philip Wong, Yoshio Nishi and Hrishna C. Saraswat, "Investigation of the performance limits of III-V double-gate n-MOSFETs," Tech. Dig. Int. Electron Devices Meet. 2005, pp. 619, 2005.

[1.30] Anisur Rahman, Gerhard Klimech, and Mark Lundstrom, "Novel channel materials for ballistic nanoscale MOSFETs-bandstructure effects," Tech. Dig. Int. Electron Devices Meet. 2005, pp.615, 2005.

[1.31] J. Bardeen and W. H. Brattain, "The transistor, a semiconductor triode," Phys. Rev., pp. 230-231, 1948.

[1.32] H. R. Huff, "From the lab to the fab: transistors to integrated circuits," Proc

2003 International Conference on Characterization and Metrology for ULSI Technology., 3-39, 2003.

[1.33] James J. Rosenberg and Suzanne C. Martin, "Self-aligned germanium MOSFETs using a nitrided native oxide gate insulator," IEEE Electron Device Lett., vol. 9, pp. 639, 1988.

[1.34] Suzanne C. Martin, Lorin M. Hitt, and James J. Rosenberg, "p-channel germanium MOSFETs with high channel mobility," IEEE Electron Device Lett., vol. 10, pp.325, 1989.

[1.35] Suzanne C. Martin, Lorin M. Hitt, and James J. Rosenberg, "Germanium p-channel MOSFET's with high channel mobility, transconductance, and k-value," IEEE Trans. Electron Device, vol.36, pp. 2629, 1989.

[1.36] Thomas N. Jackson, C. M. Ransom, and J. F. DeGelormo, "Gate-self-aligned p-channel germanium MISFETs," IEEE Electron Device Lett., vol.12, pp.605, 1991.

[1.37] C. M. Ransom, T. N. Jackson, and J. F. DeGelormo, "Gate-self-aligned n-channel and p-channel germanium MOSFETs," IEEE Trans. Electron Device, vol.38, pp. 2695, 1991.

[1.38] Huiling Shang, Harald Okorn-Schmidt, Kevin K. Chan, Matthew Copel, John A. Ott, P. M. Kozlowski, S. E. Steen, S. A. Cordes, H.-S. P. Wong, E. C. Jones and W. E. Haensch, "High Mobility p-channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric," Tech. Dig. Int. Electron Devices Meet. 2002, pp. 441, 2002.

[1.39] C. O. Chui, S. Ramanathan, B.B. Triplett, P. C. McIntyre, and K. C. Saraswatl, "Germanium MOS capacitors incorporating ultrathin high-κ gate dielectric," IEEE Electron Device Lett., v. 23, pp.473, 2002.

[1.40] Chi On Chui, Hyoungsub Kim, David Chi, Baylor B. Triplett, Paul C. McIntyre, and Krishna C. Saraswat, "A Sub-400ºC Germanium MOSFET Technology with high-κ Dielectric and Metal Gate," Tech. Dig. Int. Electron Devices Meet. 2002, pp. 437, 2002.

[1.41] C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat, "Activation and diffusion studies of ion-implanted p and n dopants in germanium, " Appl. Phys. Lett., vol. 83, pp.3275, Oct., 2003.

[1.42] H. Shang, K.-L. Lee, P. Kozlowski, C. D. Emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, and W. Haensch, "Self-aligned n-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric and tungsten gate," IEEE Electron Device Lett., v. 25, pp. 135, 2004.

[1.43] C. Jasper, L. Rubin, C. Lindfors, K. S. Jones, and J. Oh," Electrical activation of implanted single crystal germanium substrates," Proc. of Ion Impla. Tech., pp. 548, 2002.

[1.44] S.P. Ashburn, M.C. Ozturk, J.J. Wortman, G. Harris, J. Honeycutt and D.M. Maher, "Formation of titanium and cobalt germanides on Si(100) using rapid thermal processing," J. Electron. Mater., v.21, pp.81, 1992.

Chapter 2

Germanium MOS Device with High-κ Gate Dielectric

2.1 Introduction

Germanium is a promising channel material for future advanced complementary metal-oxide-semiconductor (CMOS) device as it offers 4X higher mobility for holes (1900 cm^2/V-s) and 2X higher mobility for electrons (3900 cm^2/V-s) compared to silicon (450 and 1500 cm^2/V-s respectively) [2.1]. In addition, germanium is also a potential choice for supply voltage scaling down to meet ITRS requirements [2.2]. Furthermore, germanium is suitable for highly scaled MOSFET under ballistic transportation operation due to its small carrier effective mass [2.3]. However the lack of a stable Ge oxide makes it difficult to fabricate germanium metal-oxide-semiconductor field effect transistor (MOSFET). Inspired by the recent progress of high-κ dielectric deposition technology in Si MOSFET application, germanium MOSFETs have attracted attention again.

In the first part of this chapter, a preliminary study was carried out to explore the feasibility of integrating high-κ gate dielectric with germanium substrate. Ge pMOS capacitor and pMOSFET with hafnium oxynitride (HfO_xN_y) gate dielectric were demonstrated. The thermal stability of germanium MOS capacitor upon post deposition annealing (PDA) was evaluated. Next, the electrical characteristics of both Ge n- and pMOS capacitors with Al_2O_3 and surface nitridation were in-depth

discussed. The thermal stability of germanium MOS capacitor upon post metal annealing (PMA) was systematically studied.

2.2 Experiment

2.2.1 Ge MOS devices with Hf oxynitride gate dielectric

The Ge substrates used in this work were (100) Sb doped n-type wafers with a resistivity of 2-3.2 Ω·cm. First, the substrates were dipped in ammonia aqueous solution (28% NH_4OH: H_2O=1:4) for 300 s to etch native oxide selectively from the Ge substrates and to remove residual metal contaminations [2.4]. Then the wafers were re-oxidized by dipping in diluted hydroperoxide (30% H_2O_2:H_2O=1:5) for 60 s. Following that, the wafers were cleaned by diluted-HF solution for 60 s to remove Ge oxide and achieve a clean and passivated surface [2.5]. HfO_xN_y was formed by physical vapor deposition (PVD) method. A thin HfN film was deposited by reactive sputtering using a pure Hf target, followed by post-deposition anneal (PDA) using rapid thermal annealing (RTA) for oxidation and densification. The HfN sputtering was performed in an Ar+N_2 ambient [N_2/(Ar+N_2)=0.5] with a power of 250 W and a chamber pressure of 5 mTorr. To avoid excessive oxidation and minimize interfacial layer (IL), the PDA was performed in a N_2 ambient instead of O_2 ambient. The dependence of electrical performance on the different PDA temperatures was investigated at temperatures ranging from 500 to 700 ^oC. The film thicknesses measured by ellipsometer were 5.1, 5.0, 5.1, 6.1 and 12.2 nm after 500, 550, 600, 650 and 700 ^oC PDA, respectively. After PDA, 1500 Å tantalum nitride (TaN) gate electrode was deposited and patterned by dry etch. For MOSFET fabrication, the sample after gate patterning was subjected to B^{11} implantation (Dose=$5x10^{15}/cm^2$, Energy=35keV, 7^o tilt). Forming gas annealing at 425 ^oC for 2 hours was performed as

the last step and it also behaved as the activation annealing for pMOSFET.

2.2.2 Ge MOS capacitors with Al_2O_3 and surface nitridation

Both n-type and p-type germanium MOS capacitors were fabricated on (100) germanium substrates. The resistivities were 0.2-0.27 Ω·cm and 0.45-0.51 Ω·cm for p- and n-type substrates respectively. First, the native oxide on the Ge substrates was removed using a cyclic rinse of 50:1 HF solution and de-ionized water, followed by surface nitridation performed in NH_3 ambient at 600 ^oC for 60 sec using rapid thermal process (RTP). Then, Al_2O_3 films were deposited by atomic layer deposition (ALD) using trimethylaluminum (TMA) precursor and H_2O at 320 ^oC. The film thickness was ~7.3 nm measured by spectroscopic ellipsometer. Subsequently, TaN gate electrode was deposited by reactive sputtering, and was patterned by lithography and dry etching. Following that, post metal annealing was performed in an RTP machine at different temperatures for 60 sec in a pure N_2 ambient or a mixed gas ambient of N_2+10%O_2. Finally, backside Al deposition and sintering (N_2 with 10% H_2) at 300 ^oC for 30 min were performed to reduce the contact resistance. For comparison, silicon MOS capacitors were also fabricated with the identical process conditions as the Ge devices.

The current-voltage (I-V) characteristics were measured using an HP4155B semiconductor parameter analyzer and the capacitance-voltage (C-V) characteristics were measured using an HP4284A precision LCR meter. High-resolution X-ray photoelectron spectroscopy (XPS) analysis was performed using a Physical Electronics Quantum 2000 Scanning ESCA Microprobe with a monochromatic and standard Al X-ray source.

2.3 Results and discussion

2.3.1 Ge MOS devices with HfO_xN_y gate dielectric

A. Electrical characteristics of Ge MOS capacitors

Figure 2.1 shows the variation of the EOT as a function of the PDA temperatures ranging from 500 to 650 ^oC (The duration of PDA is 1 min). The solid square symbols represent the EOT before forming gas annealing (FGA). It was found that the smallest EOT of 17 Å was obtained with PDA at 500 ^oC without FGA. A higher PDA temperature resulted in a larger EOT. Once the PDA temperature reached 650 ^oC, the interfacial layer began to grow rapidly, and led to a noticeable increase in EOT (24.2 Å). Furthermore, when the PDA was performed at a higher temperature such as 700 ^oC (not plot in the figure), the EOT increased significantly and the value showed a large spreading ranging from 4 nm to 6 nm. This huge EOT increase is due

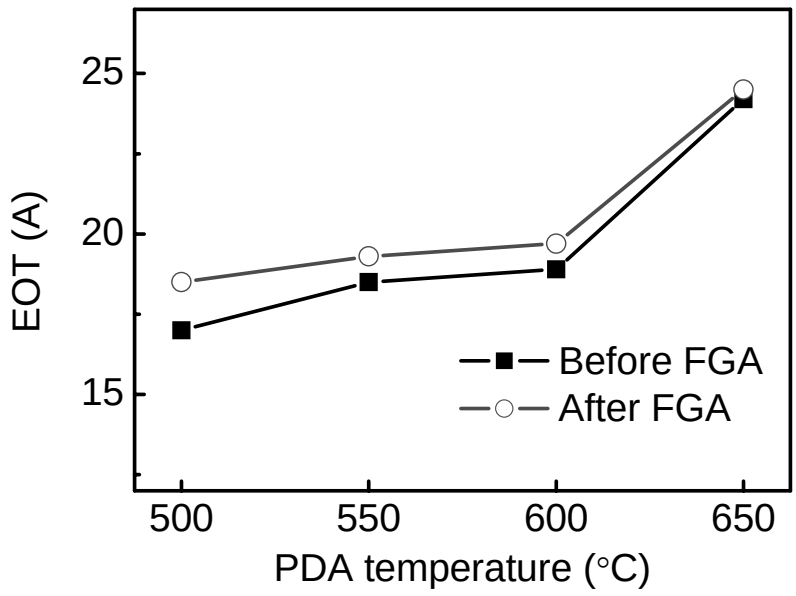

Figure 2.1. The dependence of the EOT of HfO_xN_y Ge MOS capacitors on PDA temperature and FGA.

to the significant interfacial layer growth. As measured by ellipsometer, the film thicknesses after PDA increased dramatically from 6.1 nm to 12.2 nm with increasing annealing temperature from 650 ^{o}C to 700 ^{o}C. Since the XPS results (data shown later) indicate that, after 600 ^{o}C PDA, the HfN metal film is already fully oxidized into Hf oxynitride, this huge increase in physical thickness could be only attributed to additional interfacial layer growth due to the Ge substrate oxidation. Unlike silicon on which interfacial layer growth is relative slow during PDA at the same temperature, the IL growth problem is very severe on germanium because germanium is much easier oxidized. For an instance, even at a relative low oxidation temperature such as 550 ^{o}C for 10 min in dry O_2 ambient, 8 nm Ge oxide has grown [2.6], whereas the silicon oxide growth under the same condition is negligible. Therefore, it is necessary to keep a low thermal budget for germanium process to achieve a small EOT. On the other hand, a high temperature PDA is always desirable for a high quality film. A PDA temperature of 650 ^{o}C was suggested for HfO_xN_y dielectric on silicon [2.7]. Regarding the easy oxidation behavior of germanium, a low PDA temperature of 600 ^{o}C or less is recommended for germanium process.

Another important property of device with high-κ gate dielectric is the increase of EOT after dopant activation annealing. Fortunately, the required activation temperature for dopants in germanium is much lower than that of silicon. It has been reported that low dose B^{11} dopants were electrically active without any post implantation annealing and BF_2 dopants were 100% activated after 350 ^{o}C annealing for 30 min [2.8]. Therefore, alloying at 425 ^{o}C for 2 hours was used to test the EOT increase in this study. The open circular symbols in Fig. 2.1 depict the EOT after FGA. The device with a higher PDA temperature has a smaller EOT increase after FGA. The EOT increase was 1.5 Å in the device with PDA at 500 ^{o}C, whereas it was

reduced to 0.3 Å with PDA at 650 °C. This indicates that the nitrogen bonding in HfO_xN_y effectively inhibits oxygen diffusion through the gate dielectric.

Severe C-V hystereses have been observed with high-κ gate dielectrics, which may lead to instability of threshold voltage of MOSFET. In Fig. 2.2, the hystereses of samples with different PDA temperatures are compared before and after FGA. The hysteresis was calculated by the difference between the flatband voltages of C-V curves from bi-directional voltage sweep between ± 1 V. As shown in Fig. 2. 2, the germanium device has much higher hysteresis than that of the silicon control sample. The forming gas annealing can passivate traps and relieve the hysteresis.

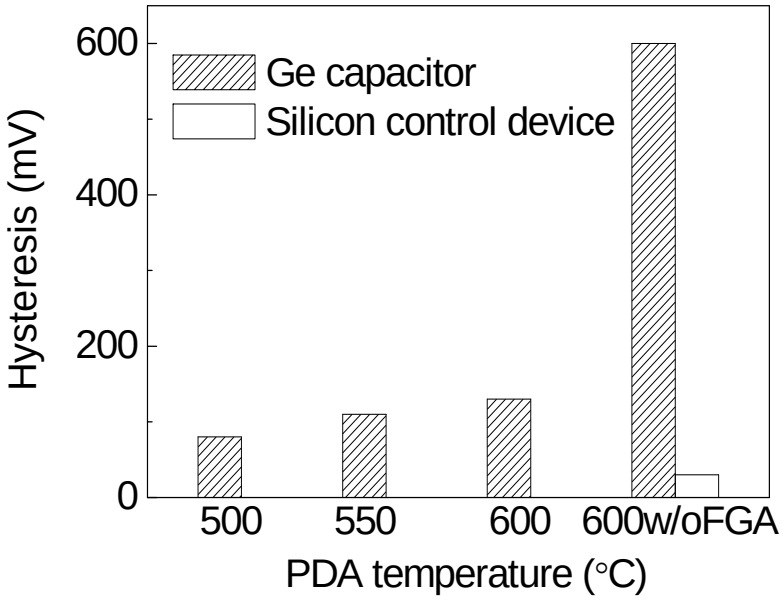

Figure 2.2. Comparison of hysteresis of devices with different PDA temperatures after FGA. One silicon control device was shown for comparison with PDA at 600 °C.

Figure 2.3 shows the typical C-V curves of HfO_xN_y Ge MOS capacitors with PDA at 600 °C before and after FGA. The C-V measurement was done at 100 kHz, sweeping from inversion to accumulation. A significant stretch-out was observed in the C-V curve of sample before FGA, which was not observed in the silicon control sample. It was noted that the stretch-out was much relieved after FGA. In addition,

the flatband voltage after FGA shifted to 0.07 V, which is close to the ideal flatband voltage. Considering the low hysteresis and good C-V curve of Si control device, we can rule out the possibility that the poor C-V characteristic of Ge devices is due to bulk traps in HfO_xN_y. The distorted C-V curve and large hysteresis of Ge device can be attributed to the formation of unstable germanium oxide interfacial layer. This is also consistent with our previous discussion that the higher PDA temperature results in a thicker germanium oxide interfacial layer, and hence leads to a lager hysteresis and EOT. The gate leakage current of Ge MOS capacitor is shown in the inset of Fig. 2.3. A leakage current density of 3.1×10^{-5} A/cm^2 was obtained at Vg=1 V.

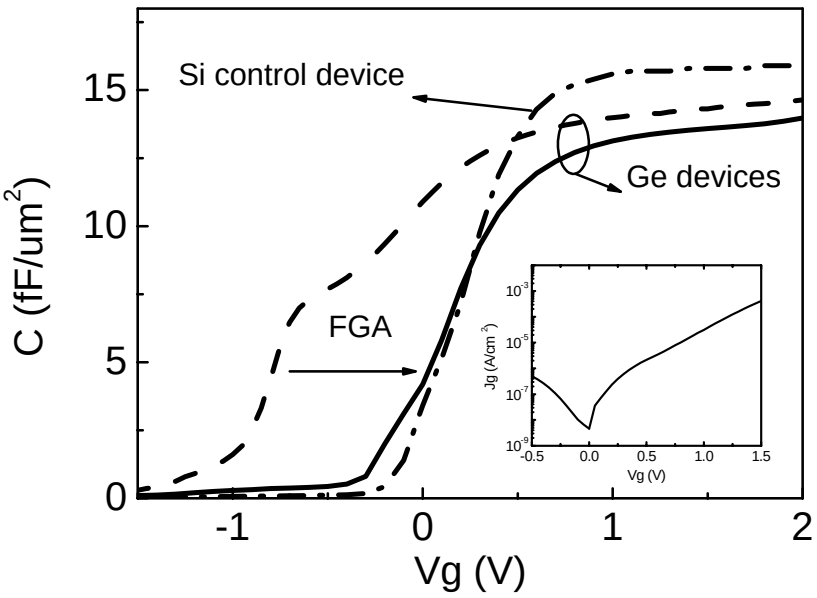

Figure 2.3. The capacitance-voltage (C-V) characteristics of HfO_xN_y Ge MOS capacitors before and after FGA. The PDA was performed at 600 ^oC for 1 min. One silicon control device without FGA was plotted for comparison. The inset shows the gate leakage current versus voltage (Jg-V) characteristic of Ge device after FGA.

B. MOSFET Characteristics

MOSFET devices were fabricated using the identical process flow of MOS capacitors with a fixed PDA temperature at 600 ^{o}C. Ring-type structure with gate length of 20 μm was used to eliminate the need for isolation. Figure 2.4 shows the well-behaved output curve of Ge pMOSFET with Hf oxynitride gate dielectric. The device exhibited normal turn-on behavior with increasing gate voltage above threshold voltage. Compared with the reported Ge pMOSFET with high-κ ZrO_2 which can not turned off due to high gate leakage [2.9], the turn-off behavior of Ge pMOSFET in this work is much better. With reducing the gate overdrive close to zero, the drive current reduces to zero and the transistor is successfully turned off. Figure 2.5 shows the transfer curve of the device. The extracted threshold voltage is -0.05 V which is relative low for real circuit application (~ -0.2 V). The optimization of threshold voltage could be done by increasing substrate doping concentration and

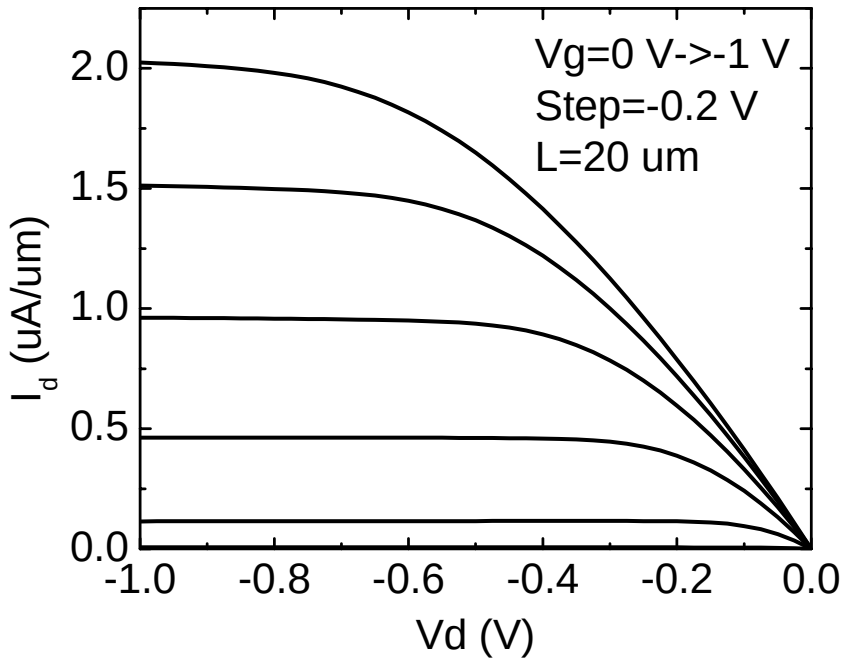

Figure 2.4. As-measured output characteristic of Ge pMOSFET with HfO_xN_y gate dielectric.

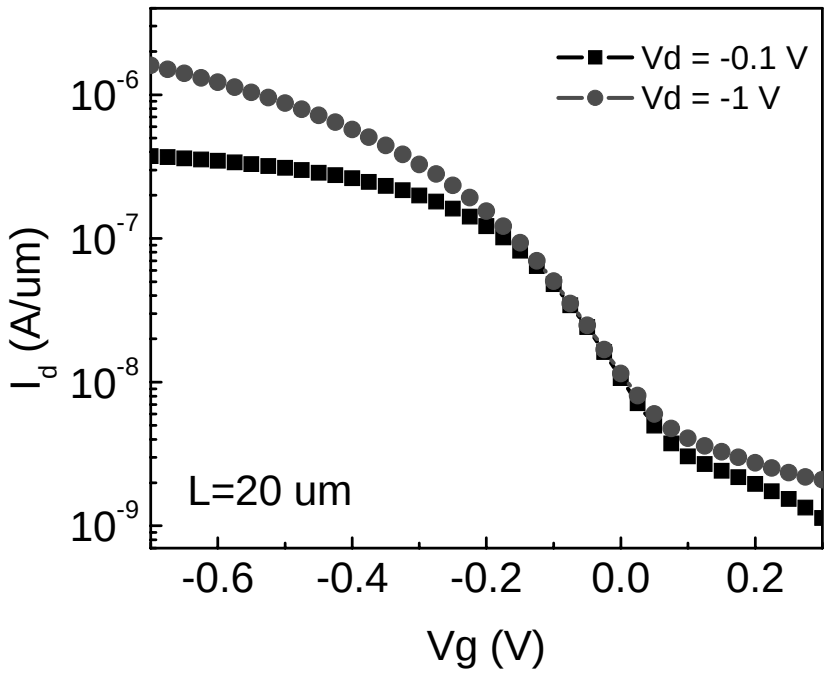

Figure 2.5. As-measured transfer characteristic of Ge pMOSFET with HfO_xN_y gate dielectric.

work function tunning of metal gate. The device exhibits 140 mV/decade subthreshold swing and this implies high interface states. Figure 2.6 shows the extracted hole mobility of the Ge pMOSFET. The germanium device exhibits much higher hole mobility than high-*κ*/Si references in the literature [2.10][2.11]. Compared with SiO_2/Si universal curve, germanium device also shows enhanced mobility at the peak region. This proves that, with Ge as channel material, a higher mobility than SiO_2/Si universal curve could be achieved. However, the mobility of germanium device degrades at high effective electrical field. It is probably due to the high source/drain series resistance. Since the device characteristics were measured by direct probing source/drain (S/D) area without any metal contact, a very large S/D series resistance has been observed. The effect of series resistance on limiting device drive current is the most pronounced when the device is biased at high gate voltage

(corresponding to high electrical field). As a result, the device mobility under high electrical field is severely underestimated.

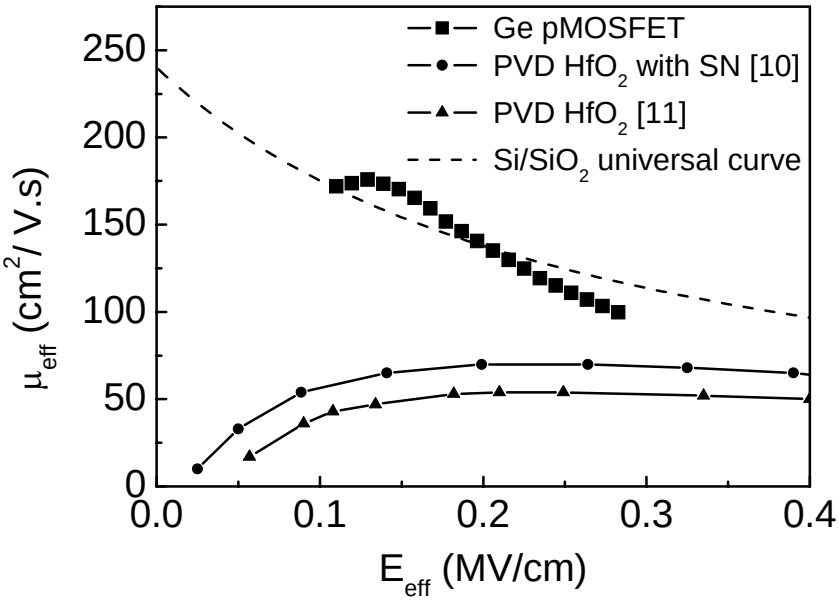

Figure 2.6. The extracted hole mobility of Ge pMOSFET with HfO_xN_y gate dielectric. The hole mobility of PVD HfO_2/Si pMOSFET and device with PVD HfO_2 and surface nitridation (SN) are included for comparison.

C. Material properties of HfO_xN_y on germanium substrate

The material property of Hf oxynitride dielectric on germanium was analyzed by XPS. Figure 2.7(a) shows the Hf_{4f} spectrum for samples before and after PDA (600 ^oC 1 min). For the sample before PDA, the binding energies corresponding to $Hf_{4f5/2}$ and $Hf_{4f7/2}$ peaks located at 17.6 eV and 16.4 eV. Compared with the reported binding energies of Hf-N at 17.2 eV and 15.6 eV and 19.64 eV and 17.93 eV for HfO_2 [2.13], the higher binding energies than Hf-N and lower binding energies than Hf-O indicate the presence of Hf-O bonds in addition to Hf-N bonds in the

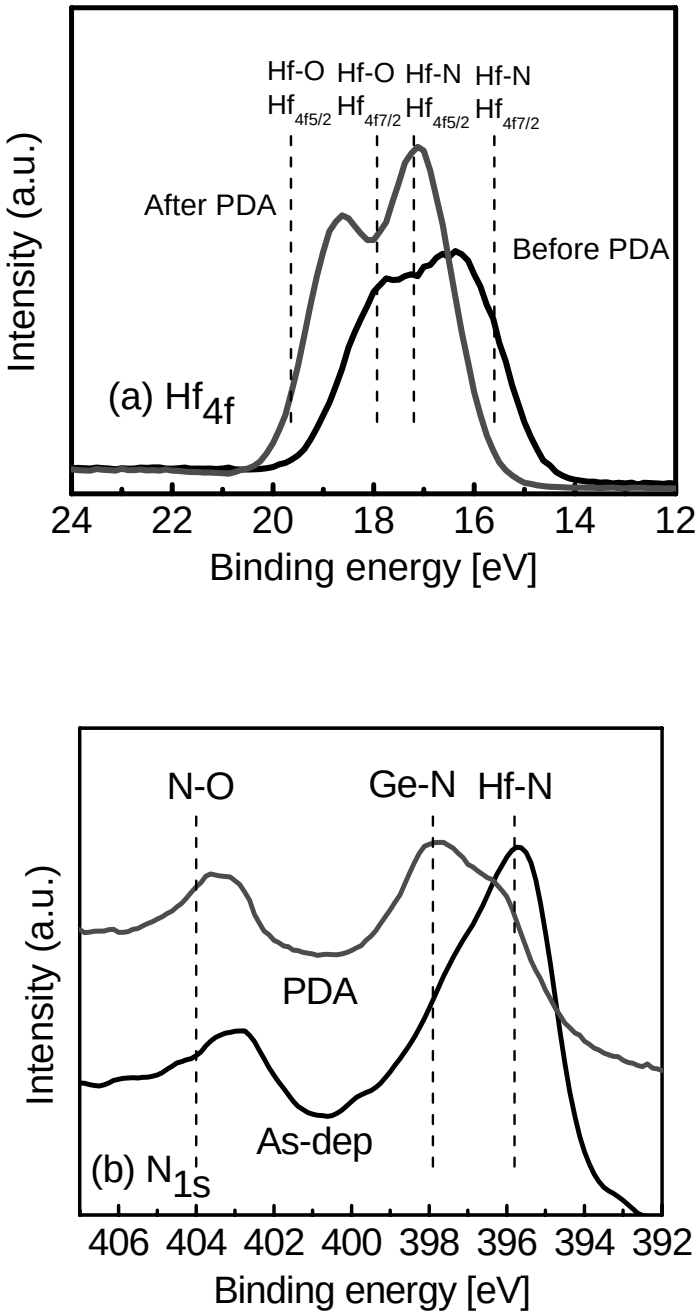

Figure 2.7. XPS spectra of (a)Hf_{4f} and (b)N_{1s} for the samples before and after PDA.

nitrogen-incorporated films. It implies that the oxidation of HfN already occurred before PDA (during the deposition or exposure to air). After PDA, the binding energies corresponding to $Hf_{4f5/2}$ and $Hf_{4f7/2}$ shift higher to 18.7 and 17.0 eV, respectively. This indicates that Hf-N bonds were replaced by Hf-O bonds after the PDA. However, each Hf_{4f} peak shows a noticeable shift from the ideal HfO_2. It implies the presence of remaining Hf-N bonds in the films. Fig. 2.7(b) shows N_{1s} peaks for the samples before and after PDA. N_{1s} peak at 395.8 eV is attributed to Hf-N bonds. After 600 ^{o}C PDA, it shifted to 397.9 eV corresponding to Ge-N bonds. This is consistent with the result of HfO_xN_y on silicon that nitrogen bonds with silicon after annealing [2.7]. N_{1s} peak around 404 eV can be attributed to N-O bonds.

Figure 2.8 shows the angle-resolved analysis of nitrogen concentration. The nitrogen concentration decreased after PDA and nitrogen piled up at the gate dielectric/germanium interface. Similar behavior of nitrogen on Si substrate has been reported by other groups [2.7].

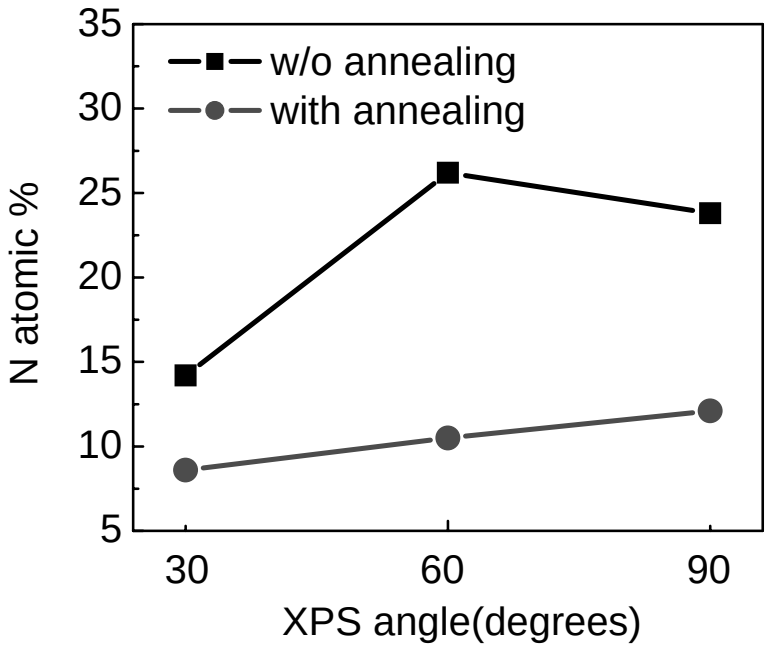

Figure 2.8. XPS angle-resolved analysis shows that nitrogen piles up at the interface.

2.3.2 Germanium MOS capacitor with Al_2O_3 and surface nitridation

In the previous section, germanium pMOSFET with PVD Hf oxynitride dielectric has been demonstrated. Although PVD is a flexible way to deposit a large variety of high-*κ* dielectrics for research and development, it is not suitable for mass manufacturing since it is hard to control the thickness and repeatability of thin layer deposition. Atomic layer deposition is recognized as a reliable method for high-*κ* dielectric deposition due to its precise deposition controllability which meets industry's need. However, high-*κ* deposition by chemical vapor deposition (CVD) on bare silicon usually results in a thick interfacial layer because of its relative high deposition temperature. Therefore, a surface treatment such as NH_3 nitridation prior to high-*κ* deposition is widely adopted to prevent the excessive interfacial layer growth.

In this section, we systematically studied both n-channel and p-channel germanium MOS capacitors with ALD Al_2O_3 gate dielectric with surface nitridation. In particular, the thermal stability of high-*κ* gate stack on germanium upon post-metal annealing (source/drain activation annealing) was evaluated.

A. Capacitance-voltage characteristics of device without PMA

Figure 2.9 (a) (b) shows the capacitance-voltage characteristics of Ge p- and n-MOS capacitors without PMA. Good C-V characteristics were obtained at 1 MHz while a kink was observed at 100 kHz in depletion region. This frequency dependence effect could be explained by interface states.

The existence of interface states affects the C-V curve by two ways [2.14]. The first effect is the stretchout of C-V curve along the gate bias axis. Stretchout occurs because the interface state charge varies with gate bias. For a MOS capacitor, to satisfy the overall charge neutrality, the change in gate charge must be balanced by a

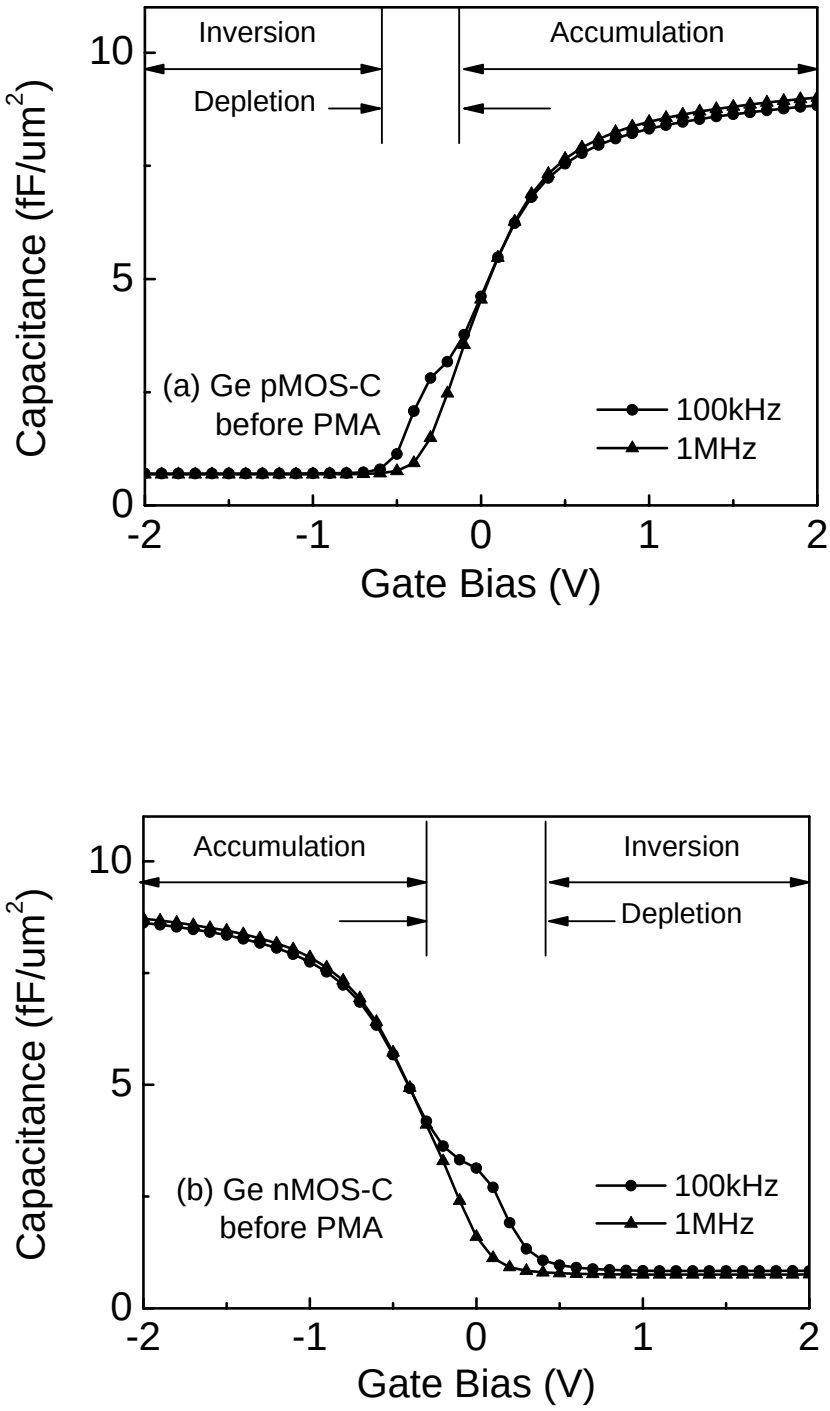

Figure 2.9. Capacitance-voltage characteristics of (a) p-MOS capacitor and (b) n-MOS capacitor without PMA measured at 100 kHz and 1 MHz. Small hysteresis (~100 mV) was estimated from bi-directional voltage sweep between ±2 V beginning at inversion (not shown in the figure).

change in substrate surface charge and interface state charge. That is, $\delta Q_G + \delta Q_{it} + \delta Q_s = 0$, where δQ_G, δQ_s and δQ_{it} are the changes of gate, surface and interface state charge density respectively. Because the MOS capacitor with interface states includes the additional change in δQ_{it} as compared with MOS capacitor without interface states, the required change in δQ_s is less. Thus the change in band bending is less in the MOS capacitor with interface states than in the one without. Consequently, to drive the MOS capacitor from accumulation to inversion (or vice verse) requires a larger range of gate charge variation for the case with interface states, than for that without interface states. Because gate charge and gate bias are related $[dQ_G = C\delta V_G]$, a larger swing of gate bias also will be required. Thus the C-V curve is stretched out along the gate bias.

The second effect of interface states is the contribution to the measured capacitance [2.14]. The capacitance of the MOS capacitor is defined by

$$C = \frac{dQ_T}{dV_G} = \frac{dQ_T}{d\psi_s}\frac{d\psi_s}{dV_g} = (C_s + C_{it})\frac{C_{ox}}{C_{ox} + C_s + C_{it}} \tag{2.2}$$

where the total charge per unit area is $Q_T = -(Q_s + Q_{it})$, $C_{it}(\varphi_s) = -\frac{dQ_{it}}{d\varphi_s}$ and $C_s(\varphi_s) = -\frac{dQ_s}{d\varphi_s}$ are the interface state and the silicon surface capacitances density respectively.

Equation (2.2) shows that, in addition to stretchout, measured C is increased as a result of Cit. The equivalent circuit corresponding to (2.2) is shown in Fig. 2.10. Since the interface state capacitance (Cit) is in parallel with substrate capacitance (Cs), the change of the capacitance of the MOS capacitor due to interface state is dependent with substrate capacitance (Cs). When the C_s is much larger than C_{it} (e.g. in the accumulation region of capacitor), the contribution to the measured capacitance by C_{it}

is negligible. When the C_s is small (e.g. in depletion region and inversion region for high frequency measurement), the increase of measured capacitor due to C_{it} is more noticeable.

The interface state capacitance also depends C-V measurement frequency. Since the interface states have finite charge/discharge time constant, when an extremely high frequency small-signal alternating component of gate bias $dV_g(\omega)$ is applied, interface states will not respond fully. Only those interface states that can capture electrons within the period of the AC gate voltage will respond. Consequently, C_{it} becomes smaller for higher frequency C-V measurement. Traditionally, those interface states which can follow high frequency small signal (several kHz or above, which is usually used for C-V measurement) are called as "fast interface states". On the contrary, those which can not are called "slow interface states".

The kink observed in the depletion region of C-V curves in Fig. 2.9 suggests the existence fast interface states which can follow 100 kHz measurement signal. As a result, an increased capacitance is recorded at 100 kHz due to Cit and it leads to the kink in the depletion region. On the contrary, for 1 MHz measurement, the interface states can not fully follow the AC signal. Therefore, the Cit decreases and the kink effect diminishes.

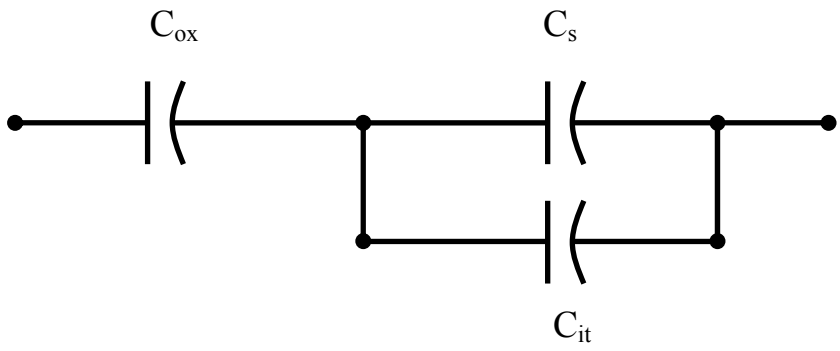

Figure 2.10. Equivalent circuit of the MOS capacitor. C_{ox}, C_s and C_{it} stand for gate oxide capacitance, substrate capacitance and interface state capacitance.

B. C-V characteristic degradation after PMA

To evaluate the thermal stability of Ge MOS capacitors with Al_2O_3 and surface nitridation, post metal annealing was performed at different temperatures from 500 ^oC to 700 ^oC in N_2 ambient. As the annealing temperature increased, the C-V characteristics exhibited systematical degradation. Figure 2.11 (a) and (b) show the typical degraded C-V characteristics after post metal annealing for Ge p- and n-MOS capacitors respectively. For the p-MOS capacitors, the shape of C-V curves is normal but they have a parallel shift with different frequencies. On the other hand, the n-MOS capacitors exhibit an abnormal high frequency C-V characteristic measured at 100 kHz which looks similar with the low-frequency C-V characteristic. Besides, nMOS capacitors also show frequency dependence in the depletion/inversion regions. In contrast to the abnormal C-V observed on Ge devices, there are no C-V degradation on Si control devices as shown in Fig. 2.11 (c)(d) after post metal annealing at the same condition. It implies that the C-V degradation is not related with pre-existing traps in the as-deposited high-*κ* material, high-*κ* crystallization or metal gate/high-*κ* interdiffusion after PMA.

The frequency dependence of Ge pMOS capacitor could be understood by a huge kink appearing from strong accumulation region (the remark in Fig. 2.11a). This kink is attributed to a series of high density interface states whose energy levels lie around midgap and the upper half of Ge (illustrated in Fig. 2.12) which correspond to p-MOS accumulation to depletion regions.

For the nMOS C-V degradation, there are two possible causes as followings. The first hypothesis is that the anomalous high capacitance may be due to small minority carrier generation time (τ_R) in high-*κ*/Ge after PMA [2.15]. The small minority carrier generation time could be attributed by metal atoms which diffuse

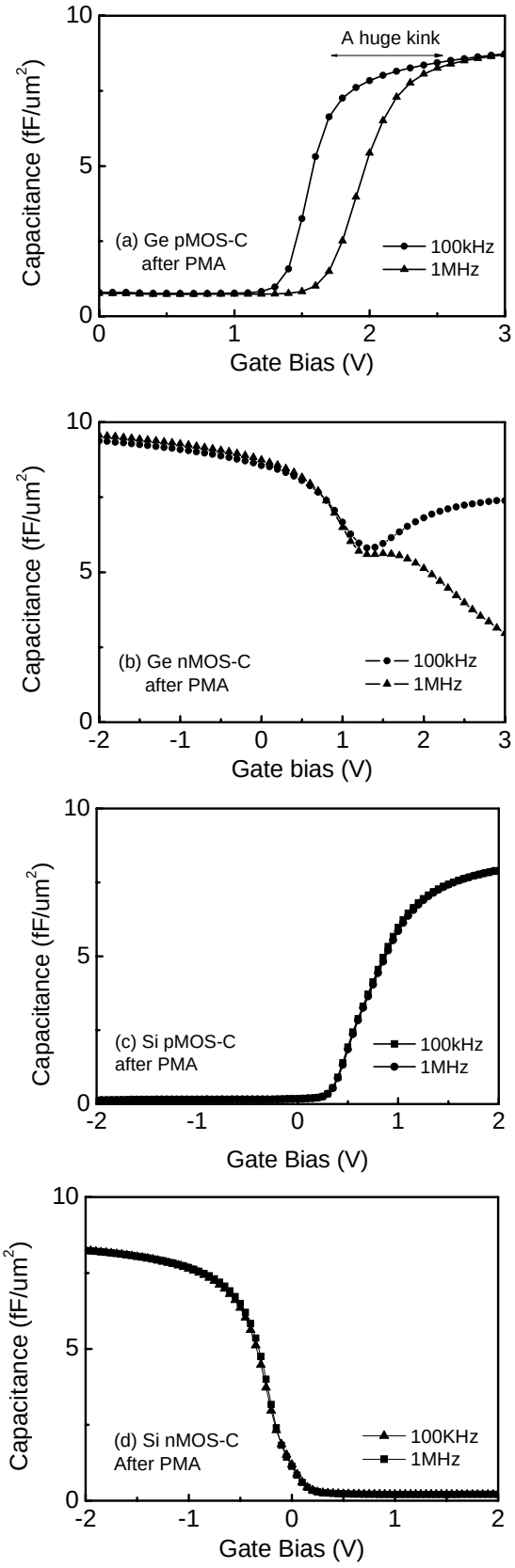

Figure 2.11. Capacitance-voltage characteristics of (a) Ge p-MOS capacitor, (b) Ge n-MOS capacitors after PMA at 600 ^{o}C for 1 min under pure nitrogen ambient. The results of Si control samples are plotted together (c)(d).

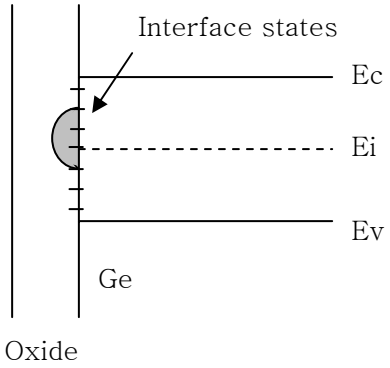

Figure 2.12. Illustration of the energy distribution of interface state.

from dielectric into Ge bulk after high temperature annealing and form bulk traps as generation/recombination centers. Under this hypothesis, when a high positive gate bias is applied (e.g. V_g=2-3 V as shown in Fig. 2.11b), the device is in inversion region. Due to a very short τ_R, there are enough minority carriers which can follow high frequency signal and therefore the device exhibits a low frequency like C-V curve at 100 kHz. However for 1 MHz, the τ_R is not small enough and the generation of minority carriers can not fully respond with AC signal. This results in the frequency dependence observed in Fig. 2.11(b). However, this hypothesis conflicts with the observed pMOS device characteristics. If metal atoms diffusion after PMA results in generation/recombination centers, an anomalous high capacitance should appear in pMOS device inversion region too but this is not observed experimentally. In addition, we measured the room temperature minority carrier response time of Ge pMOS capacitors before and after PMA. The τ_R is around 2 μsec and it does not change before and after PMA. This value is comparable with the data of Dimoulas *et al* measured on HfO_2/Ge without PMA (0.7 μsec) [2.16]. The unchanged minority carrier response time implies that the C-V deterioration is not caused by the additional bulk traps created by metal diffusion into Ge substrate.

The anomalous C-V characteristics of Ge nMOS after PMA are successfully explained by high density fast interface states. As the gate bias increases, the nMOS

changes from strong accumulation to weak accumulation and depletion. Correspondingly, the Fermi level sweeps over Ge bandgap where fast interface states exist as shown in Fig. 2.12. Since these fast interface states can follow the 100 kHz signal, it leads to the high interface state capacitance and changes the measured capacitance. For 1 MHz measurement, since the interface states can not respond, only the stretch-out of C-V curve is observed.

It is noticed in Fig. 2.11(b) that the capacitance value keeps increasing with gate bias from 1 V to 3 V which is not commonly observed in degraded C-V curve with interface states. This behavior misleads the people and induces the first hypothesis based on metal diffusion theory which was proved to be wrong. To have a correct understanding of C-V degradation, there is a need to obtain the C-V characteristics at higher gate bias (>3 V). However, due to the low breakdown voltage or high gate leakage current which minds C-V measurement , there is no report in the

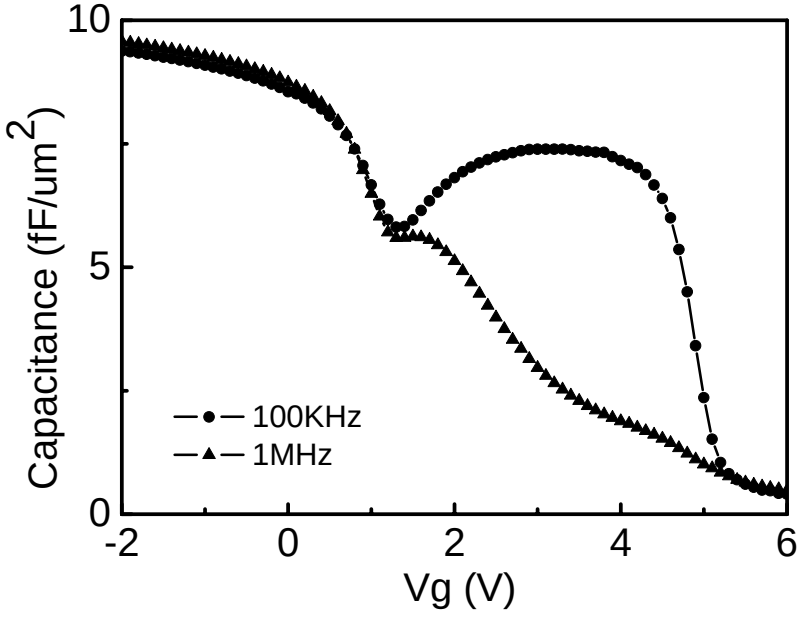

Figure 2.13. Capacitance-voltage characteristics of nMOS capacitor after PMA with increased measurement range to +6 V.

literature with high voltage C-V characteristic of Ge device. In this work, benefited from high-quality Al_2O_3, the high voltage C-V curves was obtained and it gave a clear picture of Ge n-MOS capacitor behavior. As shown in Fig. 2.13, the Ge n-MOS capacitor after PMA shows a huge kink and stretch-out around gate bias from 1 V to 5 V which is corresponding to n-MOS depletion and inversion regions. The abnormal C-V behavior at gate bias from 1 V to 3 V in Fig. 2.11(b) is actually a part of this huge kink. This huge kink indicates that a series of high density interface states locate at the midgap and the upper half of Ge bandgap. This result is consistent with the previous discussion that the interface states at the same energy levels are responsible for pMOS capacitor degradation. Since the interface state density at different energy level is different, the height of kink (i.e. the measured capacitance) varies with different gate voltage. This leads to the increase of capacitance value from 1 V to 3 V and the decrease from 3 V to 6 V.

The explanation of abnormal n-MOS C-V curve by interface state is also supported by the measured high conductance value (G) at positive gate voltage (Vg>1 V). If the anomalous high capacitance is due to minority carriers generated by bulk traps, a low conductance should be observed. Instead, a high conductance was obtained which is a clear evidence of interface states.

C. Flatband voltage variation after PMA

Besides the C-V deterioration, significant positive shift in flatband voltage (V_{fb}) was observed in both p- and n-MOS capacitors after post metal annealing. Figure 2.14 summarizes the V_{fb} of Ge p-MOS capacitors after annealing in N_2, measured at 1 MHz. The positive flatband voltage shift is not due to the reduction of fixed charge in the bulk Al_2O_3 since the Si control devices only have a small and negative V_{fb} shift

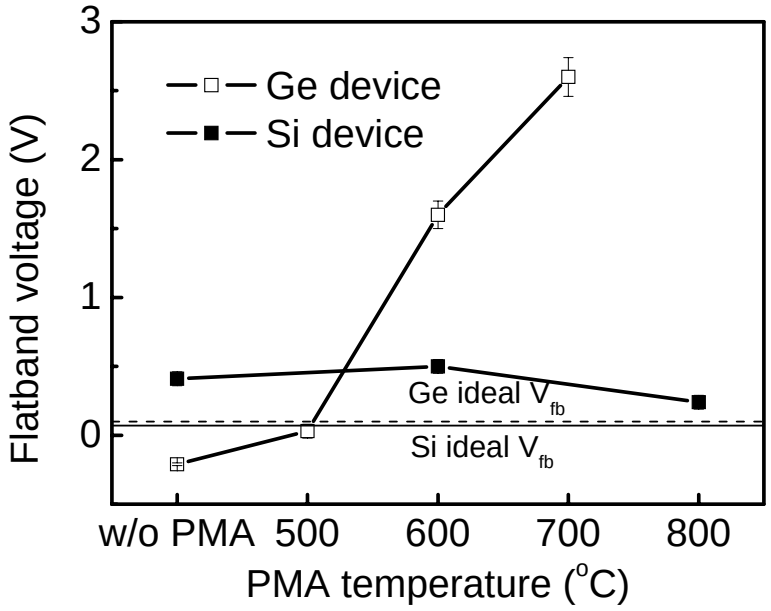

Figure 2.14. Flatband voltage shifts in Ge and Si p-MOS capacitors after PMA. The V_{fb} was extracted from the C-V curves measured at 1 MHz. The ideal V_{fb} values were calculated with the reported TaN work function and the Fermi-level of Ge and Si substrates respectively.

after the same annealing. The C-V deterioration and V_{fb} shift could be ascribed to Ge diffusing out from substrate into dielectric. It has been reported that germanium diffused through 20 nm Al_2O_3 after 800 ^oC annealing and significant Ge diffusion into HfO_2 was observed for Ge MOS devices after >500 ^oC annealing [2.17][2.18][2.19]. And germanium incorporation in dielectrics such as Al_2O_3 and SiO_2 introduces negative fixed charge and leads to positive flatband voltage shift [2.18][2.20]. These are fully consistent with our observation of significant positive shift of V_{fb} in Ge MOS capacitors with Al_2O_3 after annealing. The C-V deterioration could also be explained by Ge out-diffusion. Recent electron spin resonance (ESR) analysis revealed that dangling bonds at crystal surface were not present in high-κ/Ge device and were not responsible for interface state [2.21]. And it suggested that interface states were related with the defects originating from Ge-related imperfections in gate dielectric. This finding helps to explain the C-V deterioration. After PMA, a large amount of

germanium atoms diffuse into dielectric and result in more Ge-related imperfections which consequently generate more traps. As a result, strong frequency dependence and huge kink were observed in the C-V characteristics.

D. Gate leakage current

Post metal annealing also affected gate leakage current. Figure 2.15 (a) shows the gate leakage currents of p-MOS capacitors without PMA. In the case of negative bias corresponding to gate injection, the leakage current at high gate voltage can be well fitted by FN tunneling (Fig. 2.15b). The FN tunneling current density is given by $J_{FN} = AE_{ox}^2 \exp\left(\frac{-B}{E_{ox}}\right)$, where E_{ox} is the electric field through the gate dielectric, A and B are constants as given by $A = \frac{q^3(m/m_{ox})}{8\pi h\Phi_B}$ and $B = \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh}$. The fitted barrier height value of 3.03 eV is consistent with the band offset between TaN and Al_2O_3 conductance band [2.22][2.23]. However, in the case of positive bias corresponding to substrate injection, though the leakage current can be fitted to FN tunneling, the barrier height at Al_2O_3/Ge substrate interface (0.52 eV) is lower than the theoretical value (Fig. 2.15c). Similarly, for n-MOS capacitors without post-metal annealing (Fig. 2.16), a normal barrier height at the gate/dielectric interface (3.15 eV) and a low barrier height at the dielectric/substrate are also extracted. The low dielectric/substrate barrier heights in both p- and n-MOS capacitors imply that there are states above the Ge conduction band near the dielectric/substrate interface, which acts as electron injection centers. It is also noticed that post metal annealing in pure N_2 ambient increases leakage current dramatically (~4 orders) and decreases the dielectric breakdown voltage. It is noted that the post metal annealing in N_2+O_2 mixed

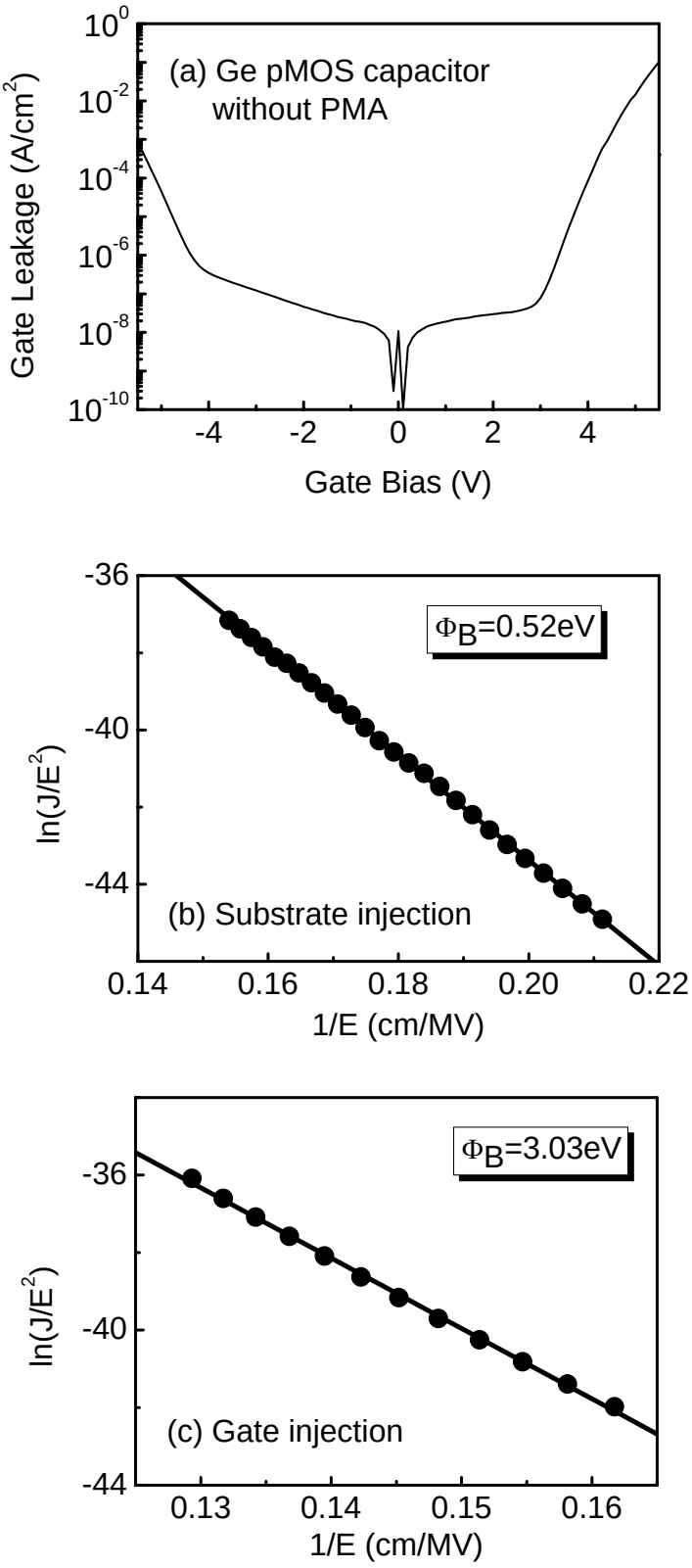

Figure 2.15. (a) I-V characteristics of Ge p-MOS capacitor. The leakage currents under high positive and negative biases were fitted to FN tunneling corresponding to (b) substrate injection and (c) gate injection.

gas ambient maintains a low gate leakage of Ge device. For comparison, no leakage current increase has been observed on Si n-MOS capacitor as a control sample after PMA (Fig. 2.17). Again, this indicates that the leakage degradation of Ge devices after PMA is not due to high-*κ* crystallization or metal gate/high-*κ* diffusion. The high leakage current after PMA in pure N_2 ambient can be another consequence of Ge out-diffusion. After annealing, the germanium resides in Al_2O_3 in an oxygen-deficient form, which results in the large increase of gate leakage current. By annealing in oxygen contained ambient, the germanium atoms diffusing into Al_2O_3 form germanium oxide and therefore a low leakage is maintained.

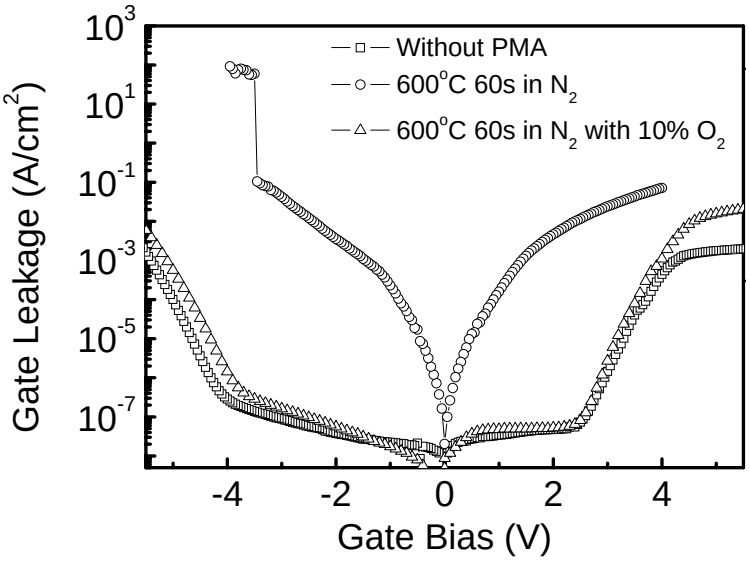

Figure 2.16. Leakage current-voltage characteristics of Ge n-MOS capacitor. After PMA under N_2, the leakage current of Ge n-MOS capacitor increased dramatically. Annealing in the mixed gas (N_2 with 10% O_2) does not increase the leakage current.

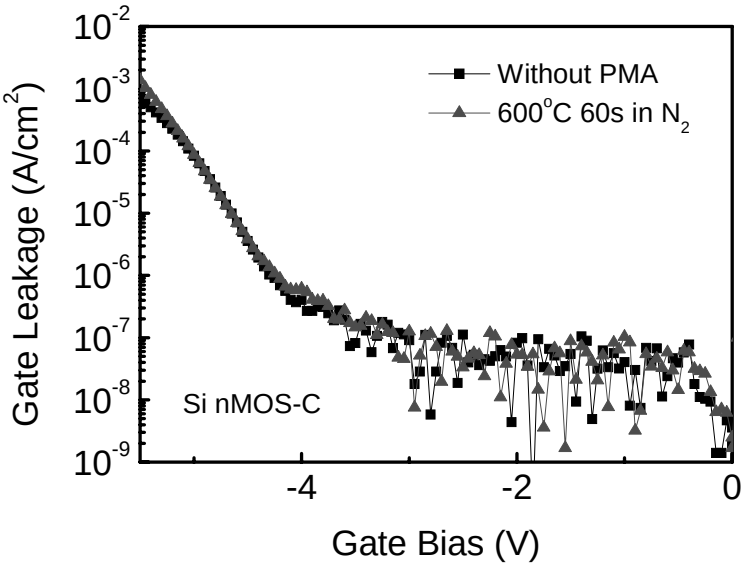

Figure 2.17. Leakage current-voltage characteristics of Si n-MOS capacitor before and after PMA under N_2.

2.4 Conclusion

In summary, Ge pMOSFET and pMOS capacitor with high-*κ* gate dielectric are demonstrated in the first part of this chapter. The results show that the PDA temperature for germanium device with HfO_xN_y should not exceed 600 °C due to a significant increase of the interfacial layer between high-*κ* film and Ge substrate. With a low thermal budget processing, promising electrical performance is shown in the Ge pMOSFET with high-*κ* gate dielectric.

In the second part of this chapter, the electrical properties of Ge MOS capacitors with NH_3 surface nitridation and Al_2O_3 gate dielectric were investigated on both p- and n-type devices. Normal C-V characteristics were obtained in the devices without high temperature PMA. The device characteristics after high temperature post metal annealing were systematically studied, and three major thermal stability issues were characterized: (1) deterioration of *C-V* curves, (2) positive shift of V_{fb}, and (3) leakage current increase. It is suspected that Ge out-diffusion from substrate into

dielectric is the root of Ge device performance deterioration.

References

[2.1] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1981), p849.

[2.2] Tony Low, Y. T. Hou, M. F. Li, Chunxiang Zhu, D. -L. Kwong, and Albert Chin, "Germanium MOS: An Evaluation from Carrier Quantization and Tunneling Current," VLSI Tech. Dig. 2003, pp.117, 2003.

[2.3] Tony Low, Y. T. Hou, M. F. Li, Chunxiang Zhu, Albert Chin, G. Samudra, L. Chan, and D. –L. Kwong, "Investigation of performance limits of germanium double-gated MOSFETs," Tech. Dig. Int. Electron Devices Meet. 2003, pp.691, 2003.

[2.4] T. Akane, J. Tanaka, H. Okumura, and S. Matsumoto, "Preparation of high-quality Ge substrate for MBE," Appl. Surf. Sci., v.108, pp.303, 1997.

[2.5] Terri Deegan, Greg Hughes, "An X-ray photoelectron spectroscopy study of the HF etching of native oxides on Ge(111) and Ge(100) surfaces," Appl. Surf. Sci., v.123, pp.66, 1998

[2.6] Y. Wang, Y. Z. Hu, and E. A. Irene, "Electron cyclotron resonance plasma and thermal oxidation mechanisms of germanium," J. Vac. Sci. Technol., A12, pp.1309, 1994.

[2.7] Chang S.K., Hag-Ju Cho, Katsunori Onishi, Renee Nieh, Rino Choi, Sundar Gopalan, Sid Krishnan, Jeong H. Han, and Jack C. Lee, "Bonding states and electrical properties of ultrathin HfO_xN_y gate dielectrics," Appl. Phys. Lett., v.81, pp.2593, 2002.

[2.8] Kevin S. Jones and E.E. Haller, "Ion implantation of boron in germanium," J. Appl. Phys., v.61, pp.2469, 1987.

[2.9] Chi On Chui, Hyoungsub Kim, David Chi, Baylor B. Triplett, Paul C.

McIntyre, and Krishna C. Saraswat, "A Sub-400ºC Germanium MOSFET Technology with high-κ Dielectric and Metal Gate," Tech. Dig. Int. Electron Devices Meet. 2002, pp. 437, 2002.

[2.10] Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Sundar Gopalan, Renee Nieh, Siddharth Krishnan, and Jack C. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," VLSI Tech. Dig. 2002, pp.22, 2002.

[2.11] Rino Choi, Katsunori Onishi, Chang Seok Kang, Sundar Gopalan, Renee Nieh, Y. H. Kim, Jeong H. Han, "Fabrication of high quality ultra-thin HfO_2 gate dielectric MOSFETs using deuterium anneal," Tech. Dig. Int. Electron Devices Meet. 2002, pp.613, 2002.

[2.12] Siddarth Krishnan, Hag-ju Cho, Akbar Shahriar, and Jack C. Lee, "Fabrication of High Quality Ultra-thin HfO2 Gate Dielectric MOSFETs Using Deuterium Anneal,"

[2.13] A. J. Perry and L. Schlapbach, "An XPS study of hafnium nitride films," Solid State Commun., v56, pp,837, 1985.

[2.14] E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology", pp.321, John Wiley& Sons, 1991.

[2.15] A. Dimoulas, G. Mavrou, G. Vellianitis, E. Evangelou, and N. Boukos, "HfO_2 high-κ gate dielectrics on Ge (100) by atomic oxygen beam deposition," Appl. Phys. Lett., v.86, pp.032908, 2005.

[2.16] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos., " Intrinsic carrier effects in HfO_2–Ge metal–insulator–semiconductor capacitors," Appl. Phys. Lett., v.86, pp.223507, 2005.

[2.17] K. Kita, M. Sasagawa, K. Tomida, K. Kyuno, and A. Toriumi, "Oxidation-Induced Damages on Germanium MIS Capacitors with HfO_2 Gate

Dielectrics," Proc. SSDM, 2003, 292 (2003)

[2.18] Q. Wan, C. L. Lin, W.L. Liu, and T.H. Wang, "Structural and electrical characteristics of Ge nanoclusters embedded in Al_2O_3 gate dielectric," Appl. Phys. Lett., v.82, pp.4708, 2003.

[2.19] Q. Zhang, N. Wu, L.K. Bera, and C. Zhu, "Study of Germanium Diffusion in HfO2 Gate Dielectric of MOS Device Application," Mat. Res. Soc. Symp. Proc. Vol. 829, 449 (2005).

[2.20] E.S. Marstein, A.E. Gunnaes, A. Olsen, T.G. Finstad, R. Turan, and U. Serincan, "Introduction of Si/SiO_2 interface states by annealing Ge-implanted films," J. Appl. Phys., 96, 4308 (2004).

[2.21] V. V. Afanas'er, Y. G. Fedorenko, and A. Stesmans, "Interface traps and dangling-bond defects in (100)Ge/HfO_2," Appl. Phys. Lett. 87, 032107, (2005).

[2.22] C. Ren, H.Y. Yu, J.F. Kang, Y.T. Hou, M.-F. Li, W. D. Wang, D.S.H. Chan, D.-L. Kwong, "Fermi-level pinning induced thermal instability in the effective work function of TaN in TaN SiO2 gate stack," IEEE Electron Device Lett., v. 25, pp.123, 2004.

[2.23] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-*κ* gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. 89, 5243 (2001).

Chapter 3

Germanium Incorporation in HfO_2 Gate Dielectric and its Impacts on Electrical Properties

3.1 Introduction

With the recent development of high-κ dielectric material replacing the conventional thermal oxide to form gate stack, germanium MOSFET draws a great attention again. High mobility long channel bulk germanium, germanium-on-insulator and strained germanium MOSFETs with various high-κ gate dielectrics have been reported [3.1][3.3][3.3][3.4]. Deep sub-micron (0.15 μm) Ge MOSFET with HfO_2 was also demonstrated in a 200 mm Si prototyping line [3.5]. It shows that Ge MOSFET fabrication is compatible with the mainstream Si processing technology. Despite that the preliminary results of Ge MOSFET with high-κ are encouraging; a new phenomenon "germanium incorporation in high-κ" has been recently reported. A large amount of germanium inside HfO_2 film deposited by metal organic chemical vapor deposition (MOCVD) technique on germanium substrate was firstly reported by our research group [3.3] and it was also observed by other researcher [3.6]. Similar germanium incorporation was noticed in physical vapor deposition (PVD) HfO_2 on Ge substrate after high temperature annealing [3.7]. However, there is no detailed investigation of the dependence of germanium incorporation on process conditions (i.e. temperature, ambient). Besides, it is not clear about the change in electrical

properties of HfO_2 film after germanium-incorporation. In the previous chapter, it is suspected that germanium diffusion into Al_2O_3 gate dielectric after post metal annealing causes significant flatband voltage shift and the increase of interface state density. Same C-V characteristic degradation is reported with Ge MOS device with HfO_2 after PMA [3.8]. In addition, since GeO_2 has lower dielectric constant (~9) than HfO_2 (~20), it is suspected that the Ge-incorporation would degrade the κ value of HfO_2 and thus would increase the EOT of Ge MOS device with HfO_2 gate dielectric. It is therefore highly desirable to investigate the change in dielectric constant and other electrical properties of HfO_2 with Ge incorporation. These results could help us to understand the observed electrical characteristics of high-κ/Ge MOS device with the presence of Ge incorporation issue. Since different HfO_2 deposition method and annealing result in different amount of Ge in HfO_2, it is interesting to evaluate the change of electrical properties of HfO_2 with different Ge concentration.

In the first part of this chapter, the mechanism of germanium incorporation into HfO_2 is extensively evaluated on bulk germanium wafers with varied process conditions. In the second part of this work, the impacts of germanium incorporation on HfO_2 electrical properties have been investigated with MOS capacitor structures.

3.2 Experiment

3.2.1 Germanium incorporation in HfO_2

HfO_2 films were deposited on (100) germanium substrates by either MOCVD or PVD method. Before deposition, the wafers were cleaned by diluted-HF. MOCVD deposition employed Hf t-butoxide precursor and O_2 at 400 ^oC in the MOCVD chamber of Jusung gate cluster. To evaluate the dependence of Ge incorporation on deposition method, reactive sputtering method (i.e. PVD) using a pure Hf target in O_2

ambient at room temperature, was used to prepare HfO_2 films. To study the Ge incorporation in HfO_2 upon subsequent thermal processes after deposition, post-deposition annealing (PDA) was performed in a rapid thermal processing (RTP) machine in N_2 or O_2 ambient at temperatures ranging from 400 to 700 ^oC.

Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was used to investigate the chemical species profiles. Sputtering was accomplished by Ar^+ at 0.5 keV for all thin HfO_2 films (≤10 nm), while the analysis was made in positive polarity by using Ga^+ primary ion beam operating at 25 keV. For all thick PVD HfO_2 films (~100 nm), the Ar^+ sputtering energy was increased to 3 keV to avoid unreasonable long experiment time. With the higher sputtering energy, the sensitivity of SIMS decreases and the intensity of the signal decreases consequently. Therefore, in the subsequent discussion, only the results with same sputtering condition were compared quantitatively. X-ray photoelectron spectroscopy (XPS) was used to investigate the film composition and chemical states.

3.2.2 Evaluation of $Hf_{1-x}Ge_xO_2$ dielectric

MOS capacitors with HfO_2 and $Hf_{1-x}Ge_xO_2$ gate dielectrics were fabricated on p-type (100) Si wafers with a resistivity of ~10 ohm-cm. Si substrate instead of Ge was used due to the following reasons: (1) It is difficult to fabricate Ge MOS devices with pure HfO_2 without any Ge incorporation as a standard sample to compare. (2) The Ge concentration in HfO_2 could not be controlled precisely on Ge substrates since the amount of Ge in HfO_2 keeps increasing with thermal process. On the contrary, by fabricating devices on Si substrate with deposited $Hf_{1-x}Ge_xO_2$, the effect of Ge incorporation on HfO_2 electrical properties could be clearly observed with precise control of Ge concentration. (3) Because the electrical properties of bulk

$Hf_{1-x}Ge_xO_2$ such as dielectric constant are independent with the substrate used, the results obtained on Si device are also applicable to Ge device. After active area definition, standard pre-gate cleaning with diluted-HF last process was performed. Pure HfO_2 and $Hf_{1-x}Ge_xO_2$ films with three different Ge compositions were deposited using reactive co-sputtering technique at room temperature. The composition was controlled by the ratio of applied powers between Hf and Ge targets. Then, post-deposition annealing in N_2 ambient was carried out by rapid thermal annealing (RTA) at 700 ^oC for 45 sec. Following that, TaN metal gate was deposited and patterned by lithography and dry etching. For some MOS capacitors, post-metal-annealing (PMA) was performed at 800 ^oC for 30 s in nitrogen ambient. Finally, Al deposition on the back side of the substrates and forming gas annealing at 425 ^oC for 30 min were performed. Electrical characteristics were measured by an HP 4284 LCR meter and an HP 4156C semiconductor parameter analyzer. EOT was extracted from the capacitance-voltage (C–V) curve measured at 1 MHz after considering the quantum mechanical effect. The area of the capacitor was $1x10^{-4}$ cm^2.

3.3 Results and Discussion

3.3.1 Dependence of germanium incorporation on process conditions

A. Ge incorporation in as-deposited MOCVD HfO_2 dielectric

The germanium incorporation in the HfO_2 film deposited by MOCVD method is first discussed. Figure 3.1 shows TOF-SIMS depth profiles of chemical species in the as-deposited 5 nm MOCVD HfO_2. Bulk HfO_2, interfacial layer (IL) and germanium substrate regions are roughly deduced from the Ge and Hf intensity variations. It is noticed that a ~3 times higher Ge intensity exists in the IL region than that in the substrate due to the enhanced sputtering yield in the oxide environment. In

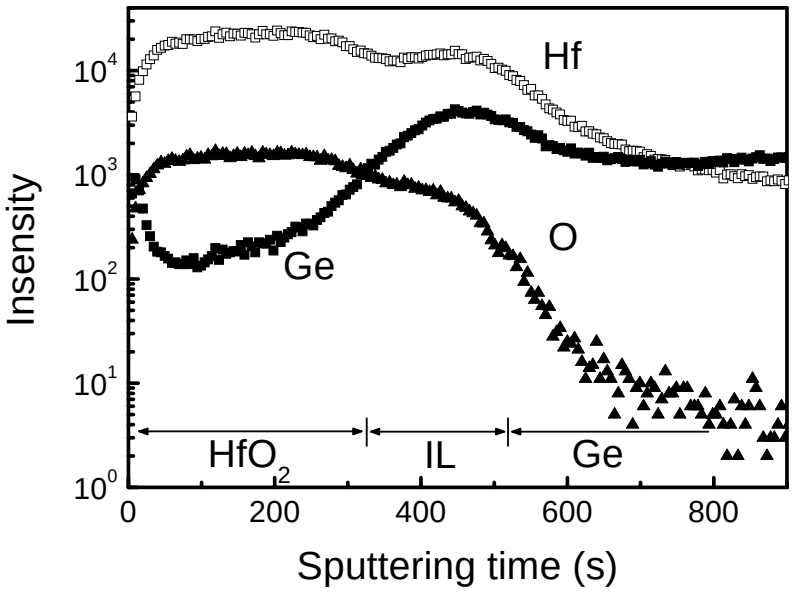

Figure 3.1. TOF-SIMS profiles of the as-deposited HfO_2 by MOCVD. The solid square symbols represent the Ge profile in HfO_2 deposited directly on HF-cleaned substrate.

addition, the existence of IL is confirmed by a smaller Hf intensity (~12,000-15,000) than that in the HfO_2 (~20,000-25,000). The simultaneous presence of Hf, Ge and O species in the IL region implies that the IL composition appears to be hafnium-germanium-oxide. It is worth noting that the germanium intensity in the HfO_2 region is still very large (>150), which is far beyond the background noise level of SIMS machine. This result confirms the Ge incorporation during MOCVD HfO_2 deposition. It needs to be noticed that the germanium incorporation in HfO_2 is not uniform. The germanium profile exhibits a U-shape characteristic: one peak locates at the interfacial region and another peak locates near the sample surface. The chemical nature of incorporated Ge is of great concern; if it exists as clusters of elemental Ge, the electrical properties (such as leakage current) of the HfO_2 would be expected to be unacceptably poor. In addition, because of the lack of sputtering yield information of Ge in HfO_2, the amount of germanium in HfO_2 cannot be calculated from the SIMS data. Therefore, XPS analysis was performed to investigate the amount as well as

chemical state of germanium in HfO_2. The Ge $2p_{3/2}$ peak was located at 1220.1 eV, with C_{1s} peak calibrated to 284.5 eV. This peak position corresponds to Ge dioxide. Since no elemental Ge peak was observed, the MOCVD HfO_2 deposition on germanium actually results in a new dielectric of $Hf_{1-x}Ge_xO_2$. Angle-resolved XPS was used to estimate the Ge atomic composition in the HfO_2. Figure 3.2 shows germanium atomic percentage at different take-off angles (10^o, 30^o, 50^o and 70^o). The smaller take-off angle refers to information from the film closer to the surface while a large take-off angle can detect Ge signal relative deep inside film. As the take-off angle increases from 10^o to 50^o, the germanium concentration decreases from 11.6% to 6.7%. It implies that there is more Ge near the HfO_2 surface than the bulk HfO_2. A further increase of take-off angle to 70^o results in an increased Ge concentration to 8.9%, which is due to high Ge composition at IL region. The XPS results agree well with U-shape Ge profile measured by SIMS.

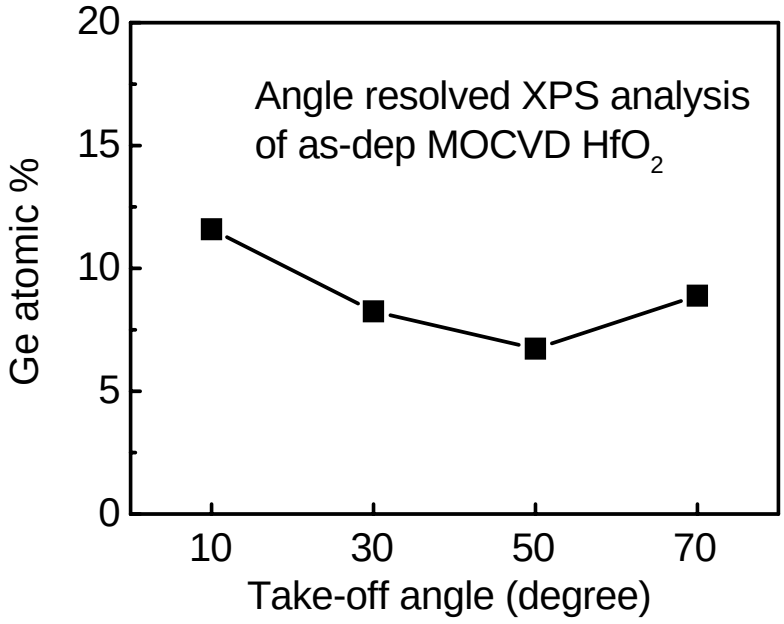

Figure 3.2. Atomic germanium concentration in the as-deposited MOCVD HfO_2 changes with the take-off angles used in the angle-resolved XPS analysis.

B. Influence of high-κ deposition method

It is reported that the Ge incorporation in HfO_2 relates with MOCVD deposition temperature. Lowering deposition temperature from 485 ^oC to 300 ^oC can effectively reduce Ge incorporation [3.6]. However, a high temperature deposition is always favorable to reduce impurities in HfO_2 such as C and Cl during CVD process. Therefore, reactive sputtering at room temperature may show advantage over MOCVD to achieve high quality HfO_2 deposition without Ge incorporation.

Figure 3.3 shows the SIMS profiles of species in the 7.5nm PVD HfO_2 on Ge. The shape of Ge profile is generally similar with the MOCVD one. There is an HfO_2 layer, including region A where Ge concentration gradually decreases and region B in which Ge concentration increases with depth, an interfacial layer (IL) and germanium substrate. As can be seen in Fig. 3.3, the as-deposited PVD HfO_2 film shows much less germanium incorporation in HfO_2 than the as-deposited MOCVD film (Fig. 3.1). The reduced Ge incorporation in the PVD HfO_2 owes to its low deposition temperature. Therefore, PVD at room temperature is superior in term of preventing

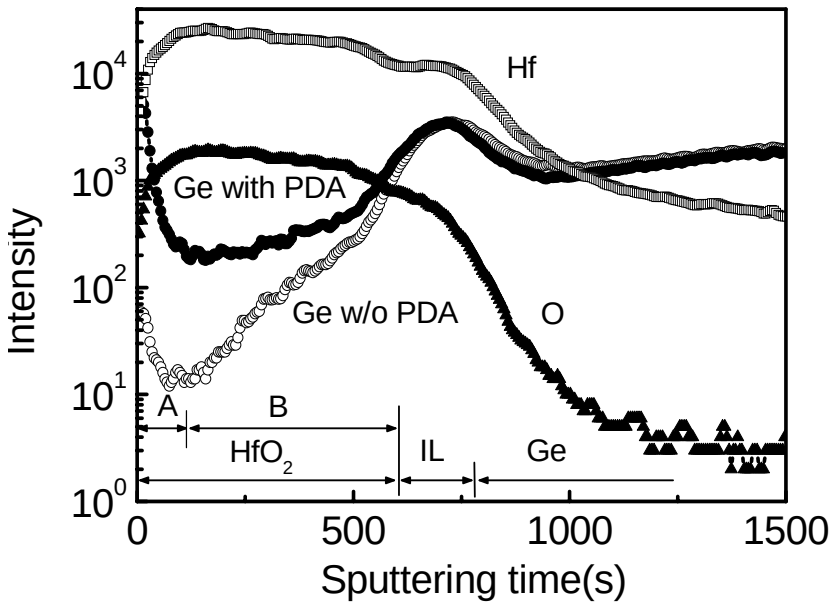

Figure 3.3. SIMS profiles of the HfO_2 deposited by PVD. The solid circle symbols represent the Ge profile in HfO_2 after 700 ^oC PDA. The open circle symbols represent the Ge profile in as-deposited HfO_2.

the Ge incorporation during HfO_2 deposition. However, after PDA at 700 ^oC for 2 min in nitrogen ambient, the germanium concentration in the PVD HfO_2 increased dramatically (solid circles of Fig. 3.3) and the germanium distribution in HfO_2 is very similar to the MOCVD one. The increased Ge incorporation in the region B is due to Ge diffusing from Ge substrate. Germanium diffusion in dielectrics such as SiO_2 and Al_2O_3 has been widely reported [3.9][3.10][3.11]. The fast germanium diffusion in dielectrics is probably due to its much higher self-diffusivity coefficient compared to Si [3.12]. However, Ge out-diffusion cannot account for the high Ge concentration in the region A. The germanium concentration in the region A after PDA increases by ~2 orders which is far beyond those in the region B. Besides, the germanium concentration gradient is opposite to that in the region B. The mechanism of germanium accumulation in the region A will be discussed later.

C. Influence of post deposition annealing temperature

The preceding result has shown that thermal annealing after PVD HfO_2 deposition causes more Ge into HfO_2. Here, the effects of annealing temperature on Ge incorporation in HfO_2 are extensively studied. Thick PVD HfO_2 films (100 nm) were used to exclude the possible interference on Ge distribution from region B so as to analyze the Ge incorporation behavior in region A. Figure 3.4 presents germanium depth profiles in the thick HfO_2 after different PDA temperatures (from 400 to 700 ^oC in N_2 for 2 min) as well as that of as-deposited one. Same as the thin MOCVD and PVD films, Ge in the thick PVD films shows a U-shape profile after annealing. Again, we can divide the Ge profile in HfO_2 into two regions (Region A and B) where the Ge incorporation shows different behaviors. In the region B, germanium diffuses up into HfO_2 at all temperatures (400-700^oC) and the Ge concentration increases along with

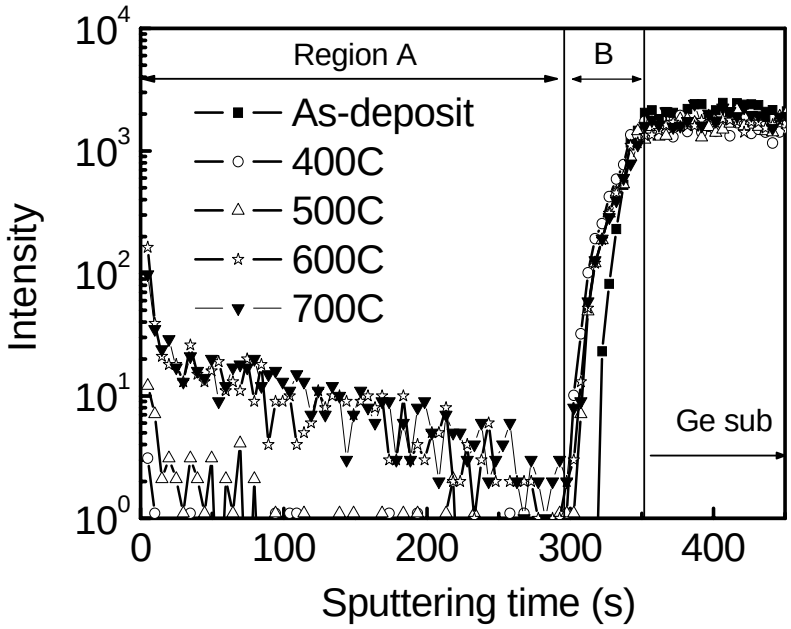

Figure 3.4. SIMS profiles of Ge in the HfO_2 deposited by PVD with different temperature PDA from 400 ^oC to 700 ^oC. The Ge profile in the as-deposited film is plotted together for comparison.

the depth. On the other hand, in the region A, the results show a systematic increase of germanium concentration with increasing temperature. No germanium was detected in the as-deposited thick HfO_2 film, which is different with thin film. It is probably due to the lower sensitivity of SIMS with increased sputtering rate for thick film. Trace amount of germanium was detected in the sample with 400 ^oC PDA. The Ge intensity fluctuating between 0 and 1 indicates a very low germanium concentration which is near TOF-SIMS detection limit. A higher temperature annealing at 500 ^oC resulted in a noticeable Ge intensity increase. After 600 ^oC and 700 ^oC PDA, germanium intensity in HfO_2 increased dramatically.

D. Germanium incorporation mechanism

The contrary germanium gradients in the two regions of thick HfO_2 suggest that

there are two different germanium diffusion mechanisms. In the region B, germanium diffuses up from substrate into HfO_2. In the region A, germanium diffuses down into HfO_2 from sample surface. It is speculated that the germanium is supplied by airborne transportation to sample surface in the chamber and the airborne Ge incorporation is related with germanium oxidation. Germanium oxidation has been studied by many researchers. It is widely reported that the formation of Ge monoxide (GeO) precedes the growth of GeO_2 [3.13][3.14]. The gaseous GeO can desorb from Ge substrate and transport in the chamber along with process gas flow. Even though the sample is annealed in nitrogen ambient, the germanium substrate could be oxidized by the residual oxygen in the chamber. Therefore, when a Ge substrate with HfO_2 is annealed, the following processes take place:

(1) reaction of oxygen with the bare Ge surfaces without HfO_2 covering (such as the backside and sidewall of Ge substrate),

(2) formation of molecules of GeO,

(3) desorption of GeO gas,

(4) transportation of GeO in process chamber in gas phase,

(5) absorption on the HfO_2 top surface and the chamber wall,

(6) diffusion downwards into HfO_2.

But it is not clear if, in the region A, Ge diffusion occurs in the form of either Ge atoms or GeO. If it diffuses in the form of Ge atoms as that in the region B, Ge should diffuse by similar distances in both region A and region B. However, the results show that the depth of the region A is obviously larger than the region B (see Fig. 3. 4). It suggests Ge diffusion mechanism in the region A is different from region B. It is probable that Ge diffuses in the region A in the form of GeO. It is reported that SiO's diffusivity in SiO_2 is near 3 orders of magnitude higher than Si atoms [3.15]. To our knowledge, there is no report on Ge and GeO diffusivity in GeO_2 or HfO_2 matrix. We

speculate that GeO may have a larger diffusivity than Ge atoms. This accounts for the faster Ge diffusion in the region A of HfO_2.

The above model can also explain the temperature dependence of Ge incorporation in the region A of HfO_2. It is reported that germanium oxidation starts at temperature ≥400 °C [3.16]. However, germanium oxidation is very slow at 400 °C and only a small amount of GeO is produced, which accords with the very low Ge concentration detected in HfO_2 after annealing at 400 °C. When samples are annealed at 600 °C and above, fast germanium oxidation occurs, which leads to strong germanium incorporation in HfO_2.

To prove the airborne Ge transportation in the chamber, a Si sample with thick PVD HfO_2 was annealed alongside Ge sample with the identical PVD HfO_2 in O_2 ambient at 600 °C. The as-deposited silicon sample with HfO_2 is free of germanium. After annealing together with germanium sample, a noticeable Ge incorporation is

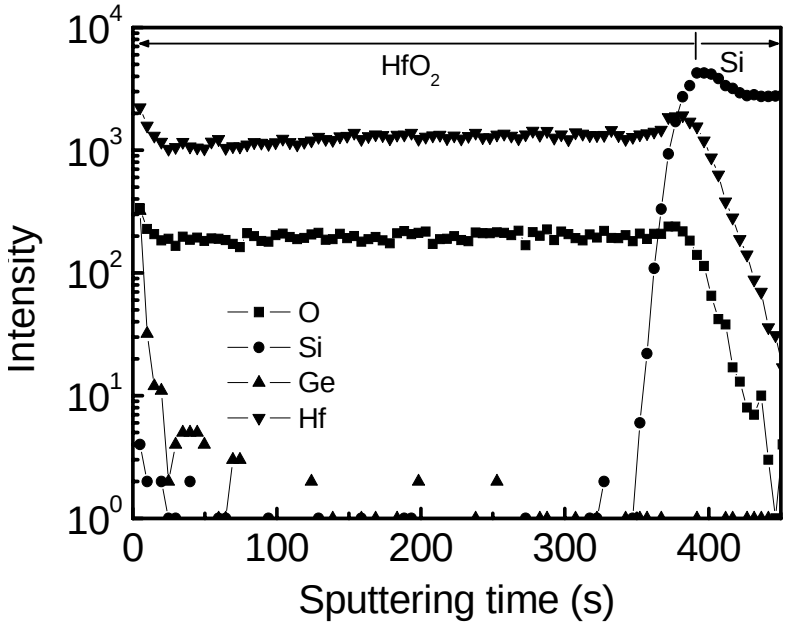

Figure 3.5. SIMS profiles of the 100 nm PVD HfO_2 on silicon reference sample annealed in O_2 alongside a Ge sample with 100 nm PVD HfO_2.

found in HfO_2 on Si, as seen in Figure 3.5. The Ge concentration decreases from HfO_2 surface along the depth direction, which is the same as Ge profile in HfO_2 (Region A) on Ge substrate. XPS analysis also confirms the existence of Ge in the surface region of HfO_2 after such annealing. The results verify that Ge contamination happens between the Si sample and the Ge sample by the airborne Ge transportation. The lower Ge intensity and shallower incorporation depth in the Si sample is possibly due to limited Ge supply. Since there is certain distance between the Si sample and the Ge sample, less amounts of germanium can reach the Si sample surface compared to the case of Ge sample.

E. Influence of annealing ambient and time

The proposed mechanisms of Ge incorporation are also supported by its dependence on annealing ambient. The germanium incorporation in HfO_2 is found to be strongly dependent on oxygen concentration in the chamber. Thick PVD HfO_2 (100 nm) films were annealed under either nitrogen ambient with very low residual oxygen concentration (less than several ppm) or pure oxygen ambient at 600 ^oC for 2 min. The very low concentration oxygen residual in the chamber was achieved by cyclically pumping the chamber down to high vacuum and venting for 5 times before annealing. The SIMS profiles of chemical species are shown in Figure 3.6. Obviously, the sample annealed in O_2 shows much higher germanium intensity near sample surface than the sample annealed in N_2 with low oxygen concentration due to much stronger Ge oxidation.

In addition, another Ge sample with 100 nm SiO_2 deposited at the backside by E-beam evaporator at room temperature with a pure SiO_2 target was prepared and subsequently annealed in O_2 ambient at 600 ^oC. Figure 3.6 shows that, with backside

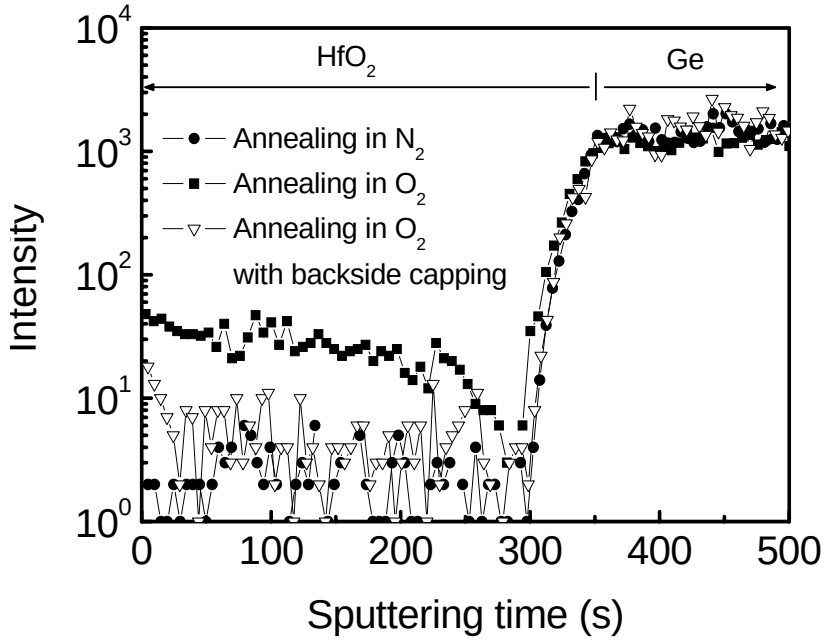

Figure 3.6. SIMS profiles of the samples with 100 nm PVD HfO_2 annealed in (a) N_2 and (b) O_2 ambient. For a selected sample (c), a layer of 100 nm SiO_2 film was capped at the backside of the sample by E-beam evaporator before annealing in O_2.

SiO_2 capping, the Ge incorporation after O_2 annealing was dramatically reduced. However, a slightly higher Ge incorporation is still observed in the capped sample annealed in O_2 than the sample annealed in N_2 with low oxygen concentration. This is due to the oxidation of bare sidewall of Ge substrate since E-beam deposition is not conformal. The ambient dependence and effect of capping are fully consistent with our proposed mechanism that the Ge incorporation in the region A of HfO_2 is through gaseous GeO produced by the oxidation of bare Ge area without HfO_2 covering. By suppressing oxidation (annealed under high purity N_2 ambient) or reducing bare Ge exposing area (by capping), there is much less amount of Ge oxidized, which leads to a significantly reduced Ge incorporation in HfO_2.

At last, the effect of annealing time on Ge incorporation was also studied. Figure 3.7 shows the Ge profiles in HfO_2 after annealing at 600 ^oC for 30 s and 300 s under O_2 ambient. It is found that although obvious Ge incorporation is observed after 30 s annealing, there are more Ge in HfO_2 if the annealing time is extended to 300 s.

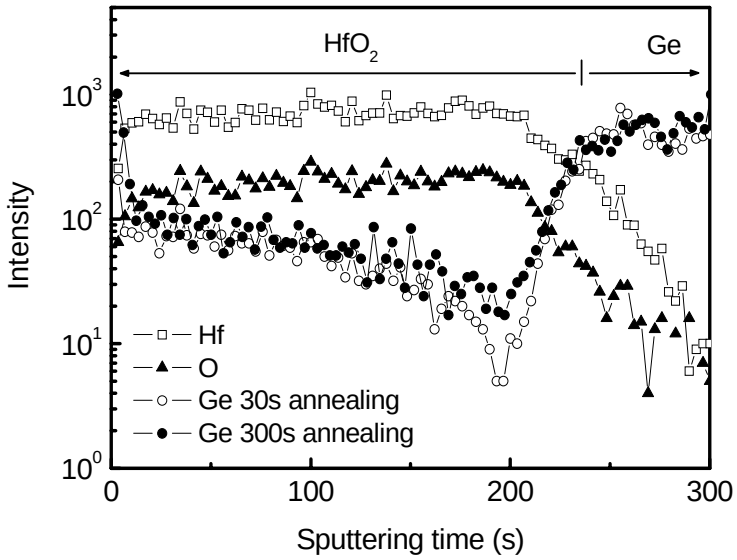

Figure 3.7. The dependence of Ge profile on annealing time. The annealing was done at 600 ^{o}C in O_2 ambient.

3.3.2 Effect of germanium incorporation on HfO_2 electrical properties

The dependence of Ge-incorporation in HfO_2 upon process conditions has been discussed in the previous section. Different HfO_2 deposition method and subsequent thermal process result in different amount of Ge in HfO_2. Furthermore, it is shown previously that the Ge distribution in HfO_2 is not uniform. Therefore, in this experiment, we investigated the dielectric constant of $Hf_{1-x}Ge_xO2$ with difference Ge composition.

A. Effect on dielectric constant

It is widely reported that the addition of Si or Al into HfO_2 causes a significant reduction in dielectric constant due to the low κ values of SiO_2 (~3.9) and Al_2O_3 (~8-9) [3.17]. Since the dielectric constant of GeO_2 is ~9 [3.18], which is very similar to Al_2O_3, it was suspected that the dielectric constant of the HfO_2 incorporated with Ge will degrade. Fig. 3.8 exhibits the EOTs of devices with different Ge contents in HfO_2.

It is noted that the sample with $Hf_{1-x}Ge_xO_2$ (x=15%) shows a smaller EOT (1.63 nm) than that of HfO_2 (1.85 nm). This is mainly due to smaller physical thickness of $Hf_{1-x}Ge_xO_2$. Measured by ellipsometer, the HfO_2 and $Hf_{1-x}Ge_xO_2$ (x=6%, 10% and 15%) film thicknesses (including interfacial layers) are 8.0, 7.9, 7.8 and 7.2 nm respectively. If considering overall effective dielectric constant k_{eff} (ε_{SiO2}*physical thickness/EOT), the $Hf_{1-x}Ge_xO_2$(x=15%) shows a similar value with that of pure HfO_2. Furthermore, TEM pictures were taken from the pure HfO_2 device [Fig. 3.9(a)] and $Hf_{1-x}Ge_xO_2$ (x=15%) [Fig. 3.9(b)]. For the device with HfO_2, the thicknesses of bulk HfO_2 and interfacial layer are 7.2 nm and 0.8 nm respectively. The thicknesses measured from TEM agree well with the data from ellipsometer. An accurate EOT after considering interfacial layer can be calculated as,

$$EOT = \varepsilon_{SiO_2}\left(\frac{t_{IL}}{k_{IL}} + \frac{t_{bulk}}{k_{bulk}}\right)$$

where k_{bulk} and k_{IL} are bulk and IL dielectric constant, t_{bulk} and t_{IL} are bulk and IL

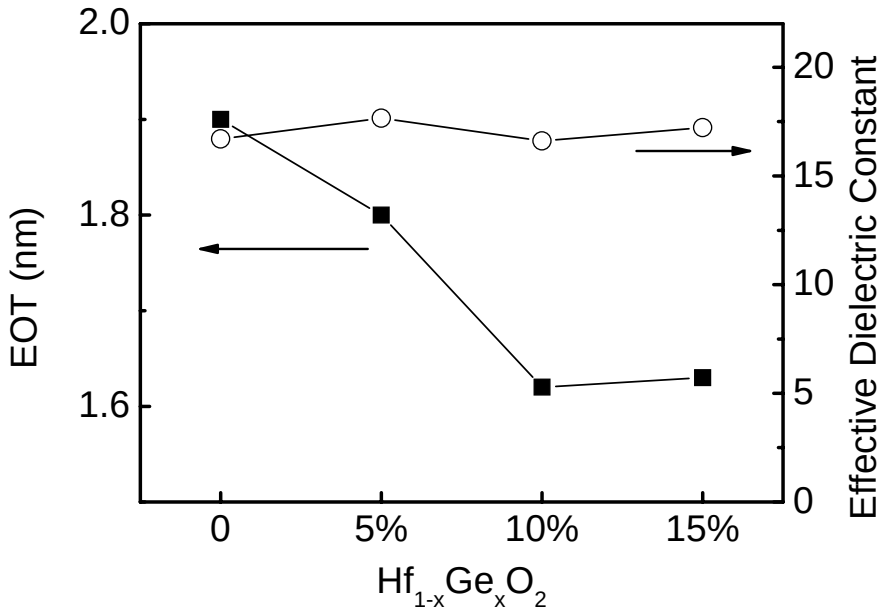

Figure 3.8. EOTs and effective dielectric constants of MOS capacitors with HfO_2 and $Hf_{1-x}Ge_xO_2$ dielectrics.

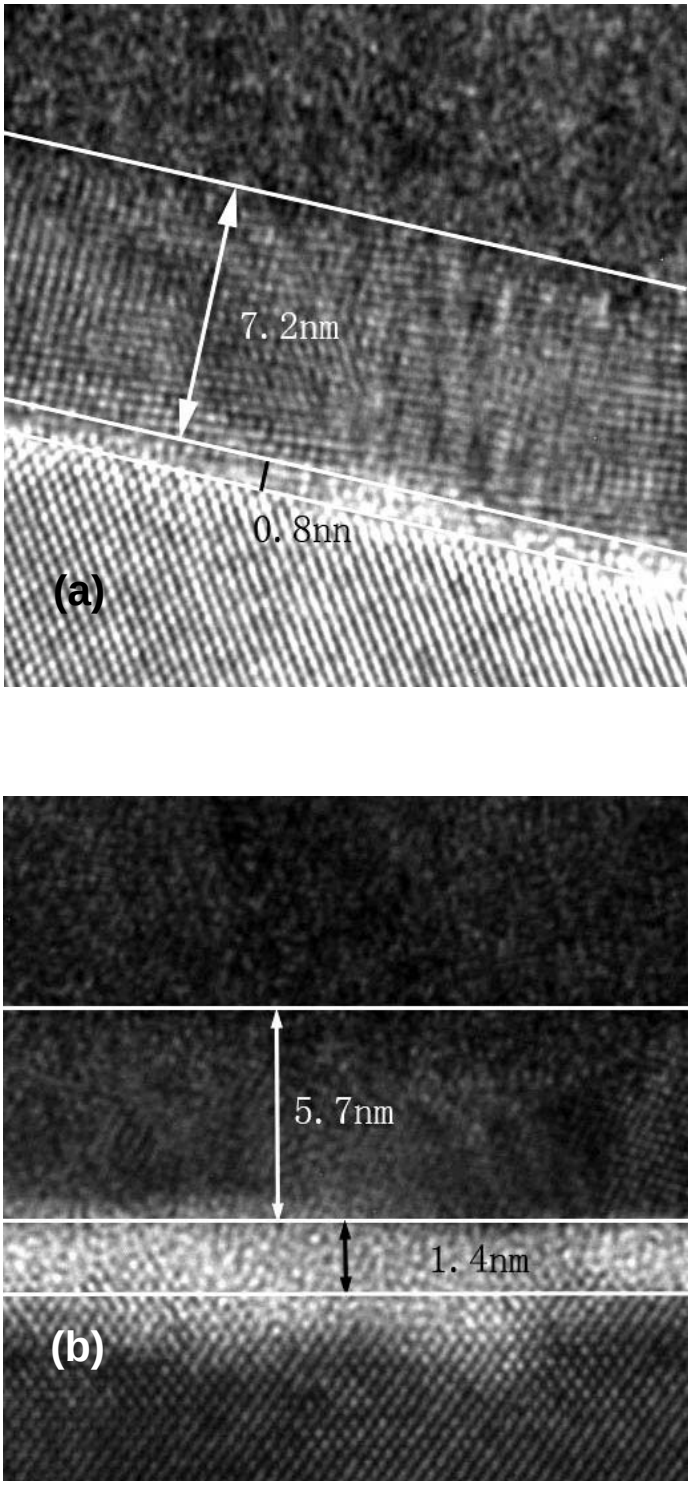

Figure 3.9. The TEM pictures of MOS capacitor with (a) HfO_2 and (b) $Hf_{85\%}Ge_{15\%}O_2$ dielectrics without post metal annealing.

thickness. Kang *et al* reported that the dielectric constant of bulk PVD HfO_2 and interfacial layer are 19 and 7.8 respectively [3.19]. Provided the same HfO_2 k_{bulk} in this work, the extracted k_{IL} is 8.4, which is consistent with Kang's result. From Fig. 3.9(b), a thicker and rougher interfacial layer (1.4 nm) is observed in $Hf_{1-x}Ge_xO_2$ device. If we assume the same k_{IL}(8.4), the calculated k_{bulk} of $Hf_{1-x}Ge_xO_2$ is 22.7 which is similar to that of HfO_2 control. Therefore, at a low concentration ($\leq$15%), incorporating low-*k* dielectric germanium oxide into HfO_2 does not degrade the dielectric constant obviously.

B. Effect on density of interface state

Figure 3.10 shows the hystereses of the devices with various Ge compositions in $Hf_{1-x}Ge_xO_2$. The hysteresis is defined as the difference between flatband voltages of C-V curves swept from 2 V to -2 V and vice versa. As shown in Fig. 3.10, $Hf_{1-x}Ge_xO_2$ (170-200 mV) shows a 2 times higher hysteresis than pure HfO_2 (95 mV). For the HfO_2 device, the hysteresis was reduced to 5 mV after an 800 ^oC 30 s post metal annealing (PMA). With the same PMA condition, the hysteresis of $Hf_{1-x}Ge_xO_2$

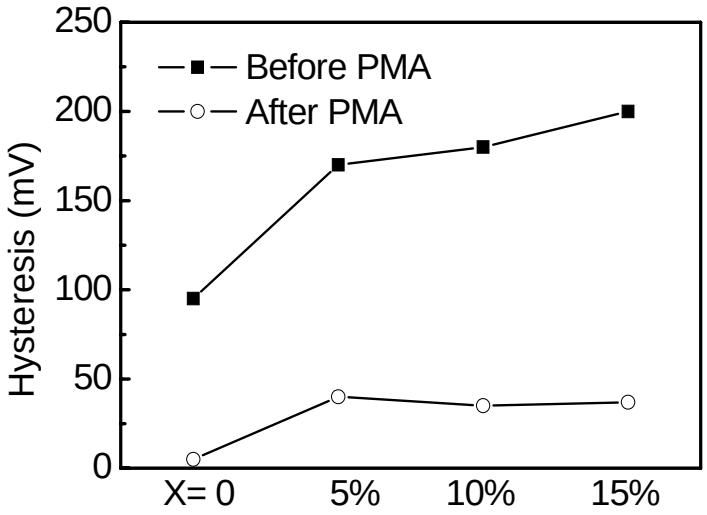

Figure 3.10. The hysteresis of MOS capacitor with HfO_2 and $Hf_{1-x}Ge_xO_2$ dielectrics before and after 800 ^oC 30 s post metal annealing.

is ~40 mV, which is 8 times larger than HfO_2. Although such a high temperature PMA could relieve the hysteresis, it is not applicable to Ge device because of the low melting point of Ge (937 ^oC). The large hysteresis of $Hf_{1-x}Ge_xO_2$ would lead to instability of threshold voltage of MOSFET.

Figure 3.11 shows the typical C-V characteristics of HfO_2 and $Hf_{1-x}Ge_xO_2$ measured at multiple frequencies. An obvious kink due to the presence of germanium oxide is observed in $Hf_{1-x}Ge_xO_2$ and the C-V distortion is stronger in the sample with higher germanium composition. This kink effect is often observed in Ge MOS devices [3.7][3.16]. High-low dual frequency method is used to measure the interface state densities (Fig. 3.12). The lines with open symbol represent the C-V characteristics measured by quasi-static method while the lines without symbol represent the C-V characteristics measured at high frequency (1 MHz). It is clearly observed that the quasi-static C-V curve of $Hf_{1-x}Ge_xO_2$ is distorted due to the huge density interface states [Fig. 12(b)]. A 6x higher D_{it} is observed with $Hf_{1-x}Ge_xO_2$ ($6.6x10^{12}$ $eV^{-1}cm^{-2}$) compared that with HfO_2 ($0.96x10^{12}$ $eV^{-1}cm^{-2}$) near mid-gap. This is consistent with the previously report that the existence of germanium at interface will increase interface states [3.20].

Although Ge incorporation does not degrade the dielectric constant of HfO_2, a large interface state density introduced is detrimental, as it will degrade the carrier mobility severely by Coulomb scattering as well as threshold voltage instability. Thus, minimizing the Ge out-diffusion into high-κ gate dielectric seems to be critical to fabricate well-performed Ge MOSFET, especially for nMOSFET where higher thermal budget is needed for dopant activation.

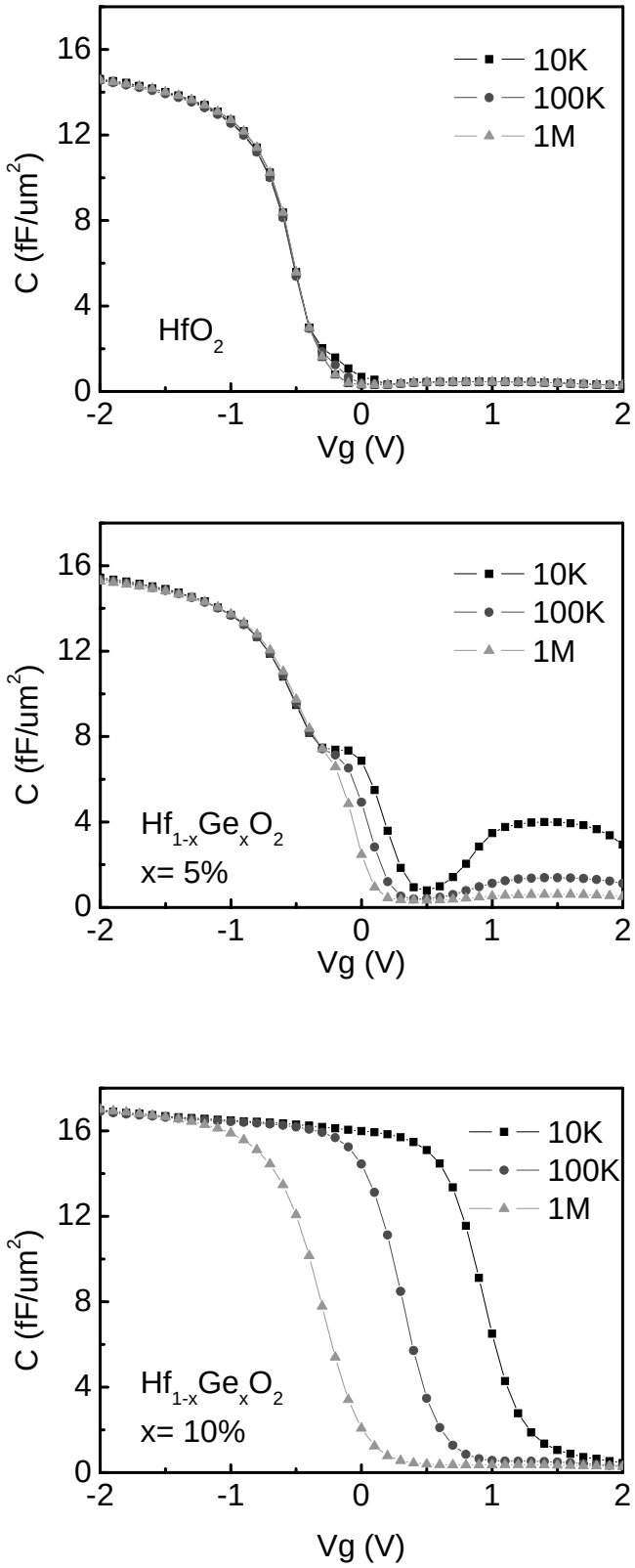

Figure 3.11. C-V characteristics of MOS capacitors with HfO_2 and $Hf_{1-x}Ge_xO_2$ dielectrics. Severe kink and frequency dependence are observed on sample with $Hf_{1-x}Ge_xO_2$.

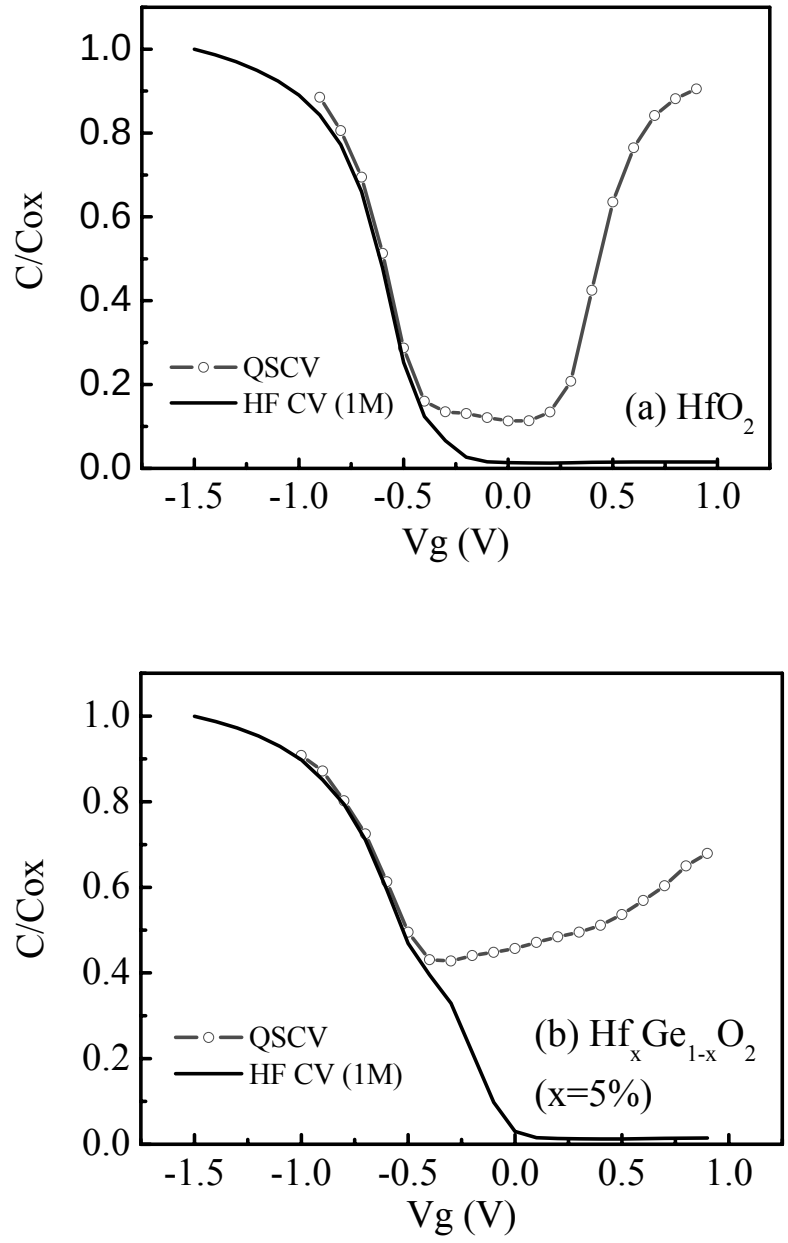

Figure 3.12. High-low frequency C-V of samples with HfO_2 and $Hf_{1-x}Ge_xO_2$ (x=5%).

3.4 Conclusion

The dependences of germanium incorporation during HfO_2 gate stack formation on germanium substrate have been extensively evaluated with varied process conditions. Severe Ge incorporation in HfO_2 occurs after high temperature annealing by two mechanisms: Ge atoms out-diffusion from Ge substrate and airborne GeO transportation. The Ge incorporation by GeO transportation is related with Ge substrate oxidation. The germanium incorporated into HfO_2 in the form of oxide and, in turn, formed a new dielectric ($Hf_{1-x}Ge_xO_2$). $Hf_{1-x}Ge_xO_2$ with low Ge content has a similar dielectric constant with that of HfO_2 but has a high interface state density which will degrade the MOSFET performance. Therefore, the thermal budget of Ge process must be tightly controlled to minimizing the Ge out-diffusion into high-κ gate dielectric.

References

[3.1] Chi On Chui, Hyoungsub Kim, David Chi, Baylor B. Triplett, Paul C. McIntyre, and Krishna C. Saraswat, "A Sub-400ºC Germanium MOSFET Technology with high-κ Dielectric and Metal Gate," Tech. Dig. Int. Electron Devices Meet. 2002, pp. 437, 2002.

[3.2] C. H. Huang, M. Y. Yang, Albert Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics," VLSI Tech.Dig., 2003, 119 (2003).

[3.3] N. Wu, Q. Zhang, Chunxiang Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B.J. Cho, A. Chin and D.-L Kwong, "Effect of surface NH3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," Appl. Phys. Lett., v. 84, pp.3741, 2004.

[3.4] A. Ritenour, S. Yu, M.L. Lee, Z. Lu, W. Bai, A. Pitera, E.A. Fitzgerald, D.L. Kwong and D.A. Antoniadis, "Epitaxial strained germanium p-MOSFETs with HfO2 gate dielectric and TaN gate electrode," IEDM Tech. Dig., 2003, pp.422 (2003).

[3.5] B. De Jaeger, M. Houssa, A. Satta, S. Kubicek, P. Verheyen, J. Van Steenbergen, J. Croon, B. Kaczer, S. Van Elshocht, A. Delabie, E. Kunnen, E. Sleeckx, I. Teerlinck, R. Lindsay, T. Schram, T. Chiarella, R. Degraeve, T. Conard, J. Poortmans, G. Winderickx, W. Boullart, M. Schaekers, P.W. Mertens, M. Caymax, W. Vandervorst, E. Van Moorhem, S. Biesemans, K. De Meyer, L. Ragnarsson, S. Lee, G. Kota, G. Raskin, P. Mijlemans, J.-L Autran, V. Afanas'ev, A. Stesmans, M. Meuris and M. Heyns, "Ge deep sub-

micron pFETs with etched TaN metal gate on a high-κ dielectric, fabricated in a 200 mm silicon prototyping line," Proceeding of ESSDERC, 2004, 189 (2004).

[3.6] S. Van Elshocht, B. Brijs, M. Caymax, T. Conard, T. Chiarella, S. De Gendt, B. De Jaeger, S. Kubicek, M. Meuris, B. Onsia, O. Richard, I. Teerlinck, J. Van Steenbergen, C. Zhao, and M. Heyns, "Deposition of HfO_2 on germanium and the impact of surface pretreatments," Appl. Phys. Lett., 85, 3824 (2004).

[3.7] K. Kita, M. Sasagawa, K. Tomida, K. Kyuno, and A. Toriumi, "Oxidation-Induced Damages on Germanium MIS Capacitors with HfO_2 Gate Dielectrics," Proc. SSDM, 2003, 292 (2003)

[3.8] J. J.-H Chen, N. A. Bojarczuk, Jr., H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO2 Gate Dielectrics on Surface-Nitrided Ge," IEEE Trans. Electron Device, Vol. 51, No. 9, pp. 1441-1447, 2004.

[3.9] W. K. Choi, V. Ho, V. Ng, Y. W. Ho, S. P. Ng, and W. K. Chin, "Germanium diffusion and nanocrystal formation in silicon oxide on silicon substrate under rapid thermal annealing," Appl. Phys. Lett., 86, 143114 (2005).

[3.10] V. Ho, L.W. Teo, W. K. Choi, W. K. Chim, M.S Tay, D.A. Antoniadis, E.A. Fitzgerald, A.Y Du, C.H.Tung, R.Liu, and A.T.S. Wee, "Effect of germanium concentration and tunnel oxide thickness on nanocrystal formation and charge storage/retention characteristics of a trilayer memory structure," Appl. Phys. Lett., 83, 3558 (2003).

[3.11] Q. Wan, C. L. Lin, W.L. Liu, and T.H. Wang, "Structural and electrical

characteristics of Ge nanoclusters embedded in Al_2O_3 gate dielectric," Appl. Phys. Lett., v.82, pp.4708, 2003.

[3.12] B. Tuck, Introduction to Diffusion in Semiconductors. Stevenage, U.K.: Peter Peregrinus, 1974, p. 227.

[3.13] L. Surnev and M. Tikhov, "Oxygen adsorption on a Ge(100) surface. I. Clean surfaces," Surf. Sci., v. 123, 505 (1982).

[3.14] N. A. Tabet, M.A. Salim, A. L. Al-Oteibi, ""XPS study of the growth kinetics of thin films obtained by thermal oxidation of germanium substrates, J. Electron Spectroscopy, v. 101, 233 (1999).

[3.15] Masashi Uematsu, Hiroyuki Kageshima, and Yasuo Takahashi, "Modeling of Si self-diffusion in SiO_2: Effect of the Si/SiO_2 interface including time-dependent diffusivity," Appl. Phys. Lett., 84, 876 (2004).

[3.16] M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Advantages of Ge (111) Surface for High Quality HfO_2/Ge Interface," in SSDM Tech. Dig., pp226-227, 2004.

[3.17] M.S. Joo, B.J. Cho, C.C Yeo, S.H. Chan, D.; S.J. Whoang, S. Mathew, L.K. Bera, N. Balasubramanian, D.-L Kwong, "Formation of hafnium-aluminum-oxide gate dielectric using single cocktail liquid source in MOCVD process," IEEE Trans. Electron Device, Vol. 50, pp. 2088-2094, 2003.

[3.18] S.B. Krupanidhi, M.Sayer, and A. Mansingh, "Electrical characterization of amorphous germanium dioxide films," Thin Sold Films, Vol. 113, pp. 173-184, 1984.

[3.19] C.S. Kang, H.J.Cho, R. Choi, Y.H. Kim, C.Y Kang, S.J Rhee, C. Choi, M.S. Akbar, and Jack C. Lee, "The electrical and material characterization of hafnium oxynitride gate dielectrics with TaN-gate electrode," IEEE Trans.

Electron Device, Vol. 51, No. 2, pp. 220-227, 2004.

[3.20] E.S. Marstein, A.E. Gunnaes, A. Olsen, T.G. Finstad, R. Turan, and U. Serincan, "Introduction of Si/SiO_2 interface states by annealing Ge-implanted films," J. Appl. Phys., Vol. 96, pp. 4308-4312, 2004.

Chapter 4

Ge MOSFETs with Shallow Junction Formed by Laser Annealing

4.1 Introduction

Besides the gate stack formation, junction formation is another major obstacle to fabricate germanium MOSFETs. First of all, the source/drain must be formed without degrading the gate stack. However, because of the poor thermal stability as described in the previous chapters, the source/drain activation by rapid thermal annealing will inevitably degrade the high-κ gate stack on Ge. Furthermore, advanced deep sub-micron MOSFET requires ultra shallow source/drain (S/D) extension to suppress severe short channel effect. In addition to being very shallow, the source/drain region must be heavily doped in order to reduce source/drain series resistance to improve device drive current.

In contrast to silicon MOSFET in which p^+/n shallow junction is the major challenge, it is more difficult to form shallow junction in germanium nMOSFET owing to the following problems. (1) N-type dopants (such as P and As) have higher diffusivity than boron in germanium [4.1]. (2) N-type dopants require a higher activation annealing temperature than that for p-type dopant. It has been reported that all of boron ions are electrically active after implantation over a wide dose range ($5x10^{11}/cm^2$ to $1x10^{14}/cm^2$) and energy range (25-100 keV) [4.2]. For BF_2^+, room-

temperature implantation into Ge does not lead to active boron while a low temperature annealing at 350 ^{o}C for 30 min activates 100% of the boron. On the contrary, a relative high temperature (600 ^{o}C) is recommended to activate n-type phosphorus in Ge [4.3]. (3) Even though a high temperature is applied to dopant annealing in germanium, the activation rate of n-type dopant in germanium is poor. A significant dose loss has been observed after rapid thermal annealing (RTA) of phosphorus-implanted germanium [4.4][4.5]. As a result, it is hard to achieve a high active doping concentration in germanium. Hence, the source/drain series resistance of MOSFET is large and limits the drive current [4.3]. (4) The thermal budget of activation annealing is limited by the poor thermal stability of high-κ gate stack on germanium [4.3][4.6][4.7]. The relative high thermal budget required to activate n-type dopants in Ge challenges the gate stack integrity.

Laser annealing has been extensively explored as an alternative source/drain activation method in Si MOSFET fabrication. Compared with RTA, laser annealing has the following advantages [4.8]: (1) ultra-short laser pulse lasting only a few nanoseconds, which is about eight orders of magnitude shorter than the RTP, resulting in minimal thermal diffusion of dopants; (2) box-like dopant profile after annealing which is favorable for short channel effect suppression; (3) metastable process without dopant solid solubility limit; (4) local selective heating of specific regions of the wafer substrate and negligible heating of the other areas of the devices.

In this chapter, laser annealing was employed to activate ion-implanted phosphorus in germanium. The dopant diffusion, dose loss and sheet resistance by laser annealing were investigated and compared with RTA on bare germanium wafers. The laser annealing was also integrated into Ge MOSFET fabrication. By simply applying an aluminum laser reflector on the TaN metal gate electrode, S/D regions were selectively annealed without heating the gate stack. Small S/D resistance as well

as good gate stack integrity was achieved simultaneously.

4.2 Experiment

The Ge MOSFETs were fabricated on (100) germanium substrates. After pre-gate cleaning, a 40 Å MOCVD HfO_2 was deposited on germanium with silicon passivation as described in [4.9]. Two kinds of gate electrodes (Al/TaN and TaN) were deposited by DC magnetron sputtering. The thickness of TaN gate was ~150 nm and the thickness of Al/TaN gate was ~100 nm/150 nm. After gate definition and patterning, a 10 nm screening SiO_2 was deposited by E-beam evaporator. Phosphorus (20 keV, 10^{15} cm^{-2}, 7^o tilt) and boron (10 keV, 10^{15} cm^{-2}, 7^o tilt) were implanted to form source/drain for n- and pMOSFET respectively. The source/drain activation annealing was performed by a KrF excimer laser. The 248 nm excimer laser had duration of 23 ns at repetition rate of 1 Hz. Varied irradiation energies were applied to evaluate dopant activation as well as device performance. For comparison, samples for dopant activation study and Ge nMOSFETs activated by RTA were also prepared at same time with identical conditions except activation. The sheet resistance was measured by a four point probe on bare Ge wafers which were implanted and annealed along with device wafers. Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was used to investigate dopant profiles. Sputtering was accomplished by Cs^+ at 3 keV, while the analysis was made in negative polarity by using Ga^+ primary ion beam operating at 25 keV. The capacitance-voltage and current-voltage characteristics (C-V) were measured by HP4284 LCR meter and HP4156 semiconductor analyzer respectively.

4.3 Results and Discussion

4.3.1 Dopants activation by rapid thermal annealing

First, phosphorus activation and diffusion after rapid thermal annealing were investigated. Figure 4.1 shows the sheet resistance (Rs) of of Ge junctions activated by RTA at temperatures of 400-700 ^{o}C for 30 s. It is observed that, as the annealing temperature increases, the sheet resistance first decreases. Although 500 ^{o}C RTA was widely used in previously reported Ge nMOSFETs source/drain activation [4.3] [4.10], it cannot fully active phosphorus with a large sheet resistance of 100 Ω/square. A minimum value is obtained after annealing at 600 ^{o}C (74 Ω/square). The 700^{o}C annealing shows slight higher Rs (81 Ω/square) than 600^{o}C due to dose loss.

Figure 4.2 shows the phosphorus profiles of as-implanted sample and those after annealing at 500-700 ^{o}C. For the sample after 500 ^{o}C annealing, obvious phosphorus diffusion occurs at high concentration region while negligible dopant diffusion is found at low concentration part. Higher temperature annealings (600 and 700 ^{o}C) lead

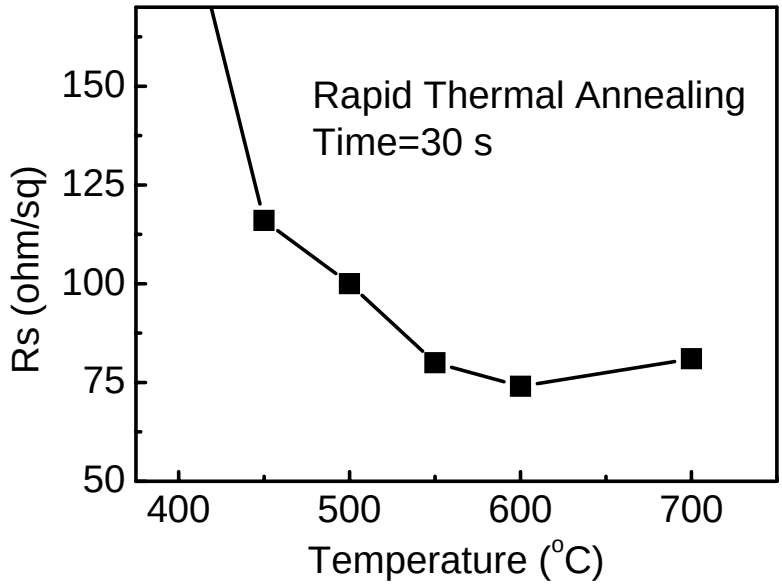

Figure 4.1. Sheet resistance of Ge junctions, formed by implantation of P with an energy of 20 keV and a dose of 1x10^{15}/cm^{2} and annealed by RTA at temperatures from 400 ^{o}C to 700 ^{o}C.

to dramatic dopant diffusion and the profiles exhibit box-shaped characteristics. The phosphorus diffusion behavior suggests a concentration dependent diffusivity. By using a diffusivity model with (n/n_i) dependency, the phosphorus profile after annealing was well fitted with the T-SUPREM simulation result [4.1]. The chemical dose of phosphorus in germanium after annealing is calculated and shown in Fig. 4.3. Note that the dose in as-implanted sample ($7.1x10^{14}/cm^2$) is smaller than the implantation dose ($1x10^{15}/cm^2$) due to the 10 nm SiO_2 capping layer. A large fraction of total dose resides in the capping oxide after implantation. As indicated in Fig. 4.3, significant dose loss (>70%) is found after RTA. The sheet resistance variation in Fig. 4.1 is the concurrent effects of dopant activation and dose loss. As the RTA temperature increases from 400 to 600 ^oC, the phosphorus dopants are gradually activated and the implantation damages in Ge are repaired. Although the remaining dopant dose in Ge reduces with increasing annealing temperature (dopant loss), the

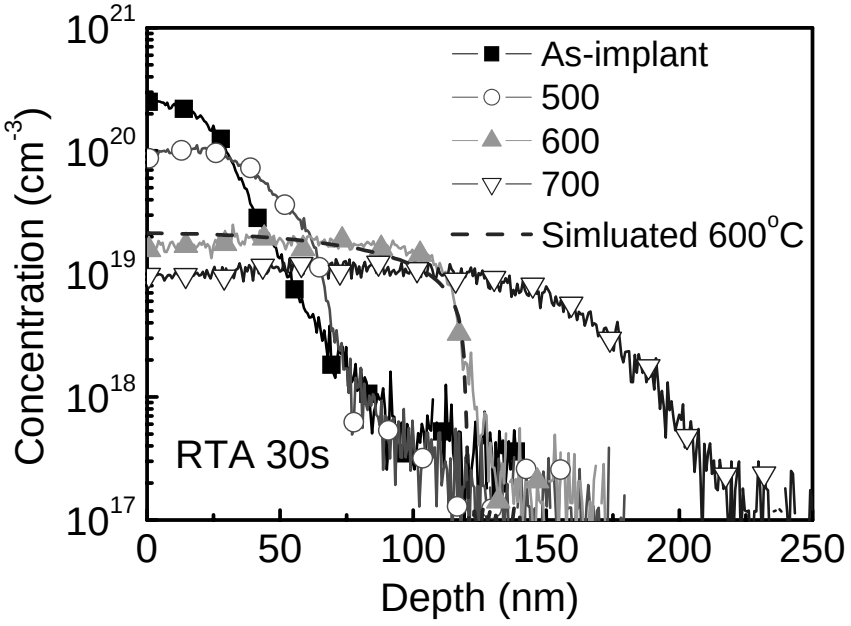

Figure 4.2. SIMS profiles of as-implanted phosphorus in germanium and after RTA at 500-700 ^oC for 30 s. Dashed line is the T-SUPREM simulation fitting of dopant diffusion at 600 ^oC for 30 s.

percentage of remaining dose been electrically activated increases. As a result, the Rs keeps reducing. A 100% dopant activation and defect-free single crystal Ge (the highest mobility) are achieved at 600 ^{o}C and Rs achieves the minimum [4.5]. Annealing at temperature higher than 600 ^{o}C does not help to improve the mobility but leads to increased dose loss, which in turn increases the sheet resistance.

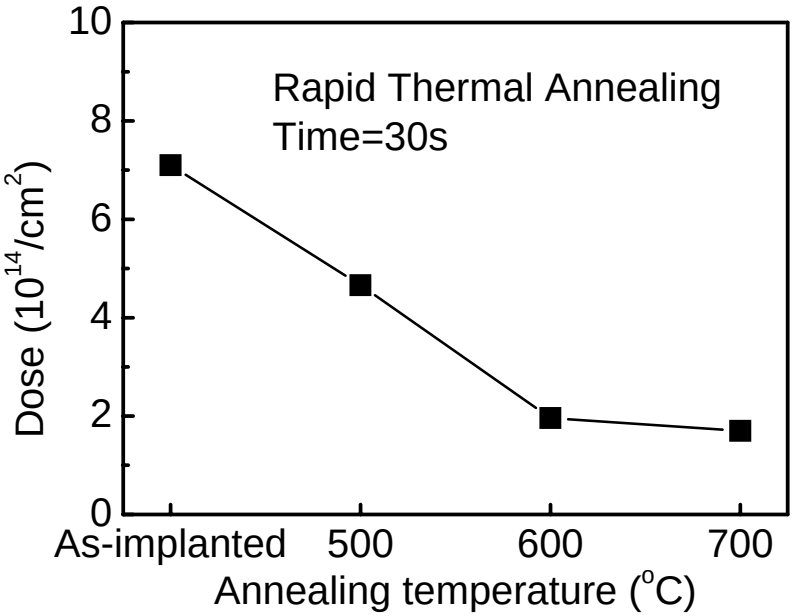

Figure 4.3. Chemical dose of as-implanted phosphorus in germanium and after annealing.

4.3.2 Dopant activation and diffusion by laser annealing

The sheet resistance of Ge junctions activated by laser annealing with various energies for one pulse is shown in Fig. 4.4. With increasing the laser energy, a sharp reduction of the sheet resistance is recorded and after that the Rs saturates slowly. At a low energy of 0.1 J/cm^2, the sheet resistance after laser annealing is around 150 Ω/square close to the Rs before annealing (180 Ω/square). It indicates that almost no activation occurs with such a low energy. By increasing the laser energy to

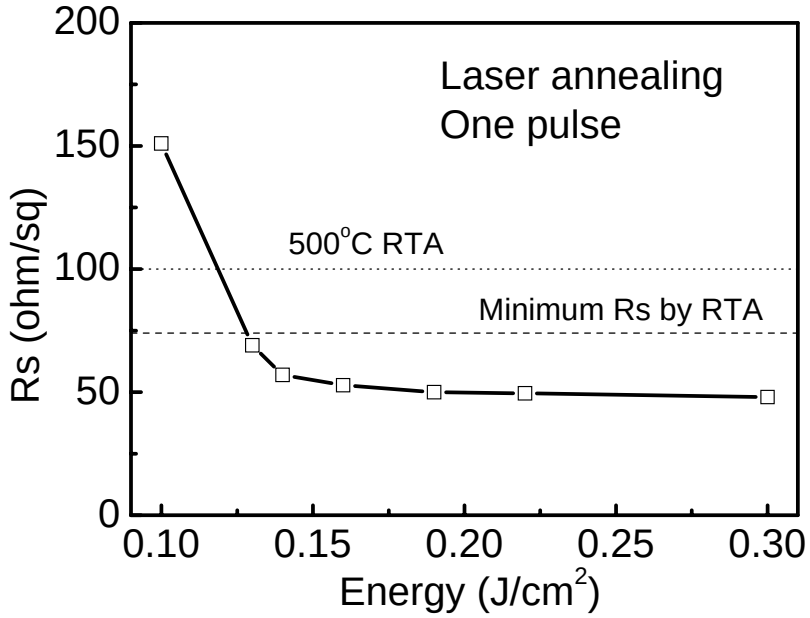

Figure 4.4. Sheet resistance of Ge junctions, annealed by laser annealing at energy from 0.1-0.3 J/cm^2 for one pulse.

0.13 J/cm^2, the sheet resistance is effectively reduced to 70 Ω/square which is lower than the minimum value (74 Ω/square) achieved by RTA. The small Rs value indicates that the phosphorus dopants have been electrically activated.

The Rs variation behavior is consistent with the mechanism of laser dopant activation. The key point of laser activation is to melt the Si or Ge [4.12]. During the cooling down and recrystalization, the dopants are frozen into the substitution position in the lattice and become electrically active at a concentration well above dopant solubility. In this experiment, the source/drain area in the Ge substrate was heavily damaged during ion implantation and became amorphous (TEM shown later). And it was reported that amorphous Ge melted and formed a continuous Ge liquid layer after laser annealing at the energy ≥0.125 J/cm^2 [4.11]. Therefore, at low laser energy (0.1 J/cm^2), the Ge is not melted and it leaves a high Rs. At the energy of 0.13 J/cm^2 or higher which is beyond the Ge melting threshold energy, the a-Ge in the source/drain regions is melted and Rs drops suddenly. The lowest sheet resistance of

48 Ω/square is obtained. It is 35% lower than the minimum value achieved by RTA and clearly shows the advantage of laser annealing to reduce source/drain resistance of Ge MOSFETs.

Figure 4.5 shows the dopant profiles after laser annealing with different energies. No dopant diffusion is observed after 0.1 J/cm^2 laser annealing. It is consistent with the sheet resistance result that dopant is not activated at this low energy. However, noticeable phosphorus dopant redistribution is observed on the samples with energy of 0.14 J/cm^2 and 0.16 J/cm^2. The sample with the higher energy of 0.16 J/cm^2 shows a deeper dopant diffusion step. The residual dose after laser annealing is summarized in Figure 4.6. With single pulse annealing, there is negligible dopant loss after annealing at energy up to 0.19 J/cm^2. This accounts for the lower sheet resistance after laser annealing than that after RTA which suffers severe dopant loss.

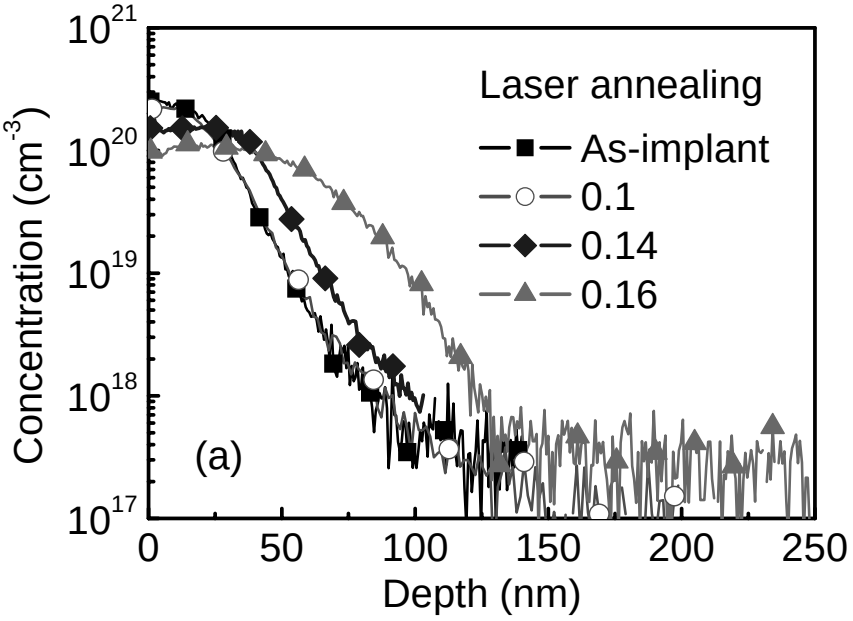

Figure 4.5. SIMS profiles of as-implanted phosphorus in germanium and after laser annealing (a) at different energies for one pulse.

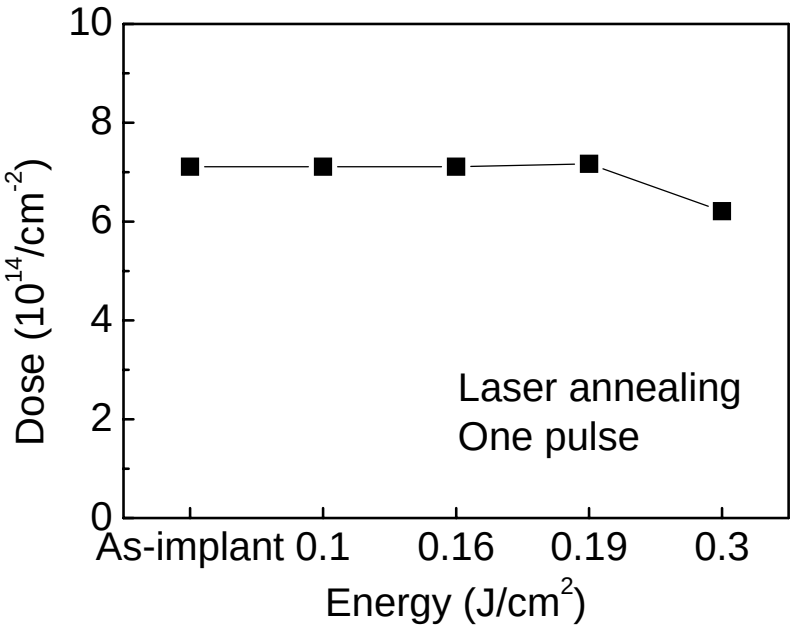

Figure 4.6. Chemical dose of as-implanted phosphorus in germanium and after laser annealing.

Figure 4.7 summarizes the sheet resistance and junction depth of samples after rapid thermal annealing and laser annealing with different process conditions. It shows that, at same junction depth, laser annealing is able to achieve smaller sheet resistance than rapid thermal annealing. Considering the trade-off between low Rs and junction depth, laser annealing at 0.14 J/cm^2 was chosen to be the optimum condition with small Rs of 57 Ω/sq and junction depth of 96 nm (compared with 86 nm for as-implanted sample and 74 Ω/sq, 122 nm for RTA at 600 ^{o}C). TEM analysis has been performed to examine the effect of laser annealing on damage reparation. The left picture of Fig. 4.8 shows that after phosphorus implantation, a 39.2 nm amorphous Ge layer was produced. After laser annealing, a defect-free single crystal Ge was obtained (right picture of Fig. 4.8).

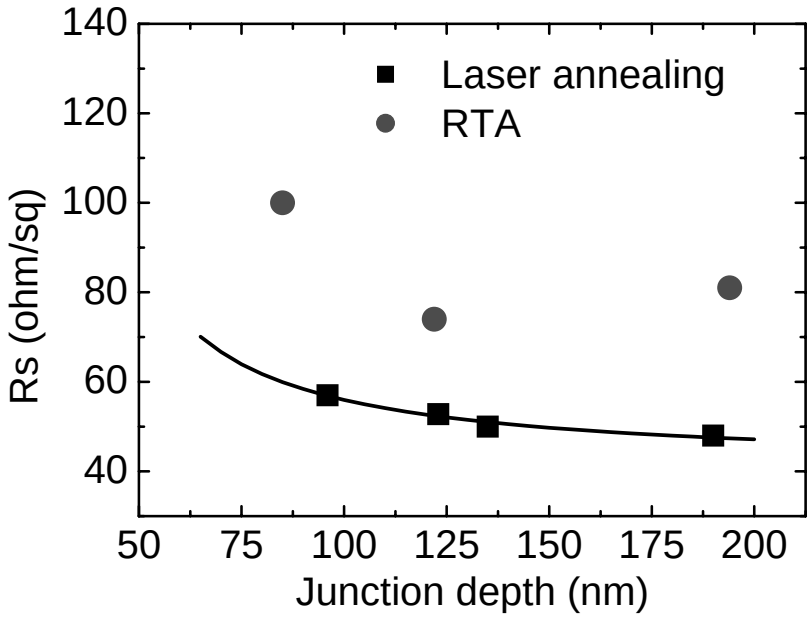

Figure 4.7. Sheet resistance versus junction depth of samples activated by rapid thermal annealing and laser annealing.

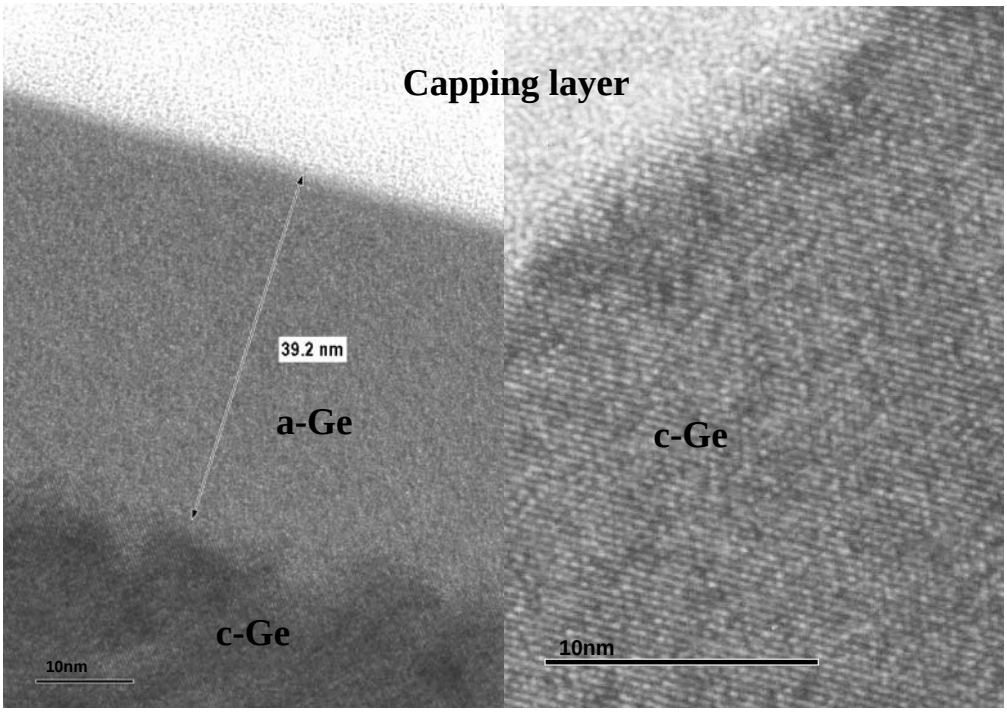

Figure 4.8. TEM pictures of the (left) as-implanted sample and (right) that after 0.14 J/cm^2 one pulse laser annealing.

4.3.3 Ge MOSFETs with laser annealing as junction activation method

Laser annealing has exhibited advantages to form n^+/p shallow junction in bulk germanium substrate with low sheet resistance. However, to incorporate this technique into germanium MOSFET fabrication, the thermal stability of high-κ gate stack upon laser annealing is of great concern. Previous works showed that high-κ/germanium stack had a poor thermal stability after furnace or rapid thermal annealing [4.3][4.6][4.7]. A significant flatband voltage (V_{fb}) shift toward positive direction has been commonly observed with various high-κ materials (Ge oxynitride, Al_2O_3, HfO_2) after source/drain activation annealing or post metal annealing which is used to simulate the S/D annealing. For an instance, post metal annealing by RTA at 400-600 ^oC for 30 sec was performed in this experiment. Fig. 4.9(a) shows the equivalent oxide thickness (EOT) and flatband voltage variation after RTA. Although the EOT does not change after RTA, the positive V_{fb} shift starts to occur at temperature around 500^oC. The high temperature RTA leads to a dramatically V_{fb} increase (ΔV_{fb}=1.8 V for RTA at 600 ^oC). The positive V_{fb} shift is speculated due to germanium out-diffusion into gate dielectric which introduces additional negative fixed charge [4.7][4.13][4.14]. These negative fixed charges result in an unaccepted high threshold voltage and may degrade mobility due to strong Coulomb scattering. To evaluate the thermal stability of high-κ gate stack upon laser annealing, Ge MOS capacitors with TaN or Al/TaN gate electrodes were subjected to laser annealing with different energies for one pulse. Fig. 4.9(b) shows the EOT and flatband voltage change after laser annealing. The device with TaN gate electrode shows poor thermal stability with laser annealing. The device does not work after laser annealing at the irradiation >0.13 J/cm^2 because of the deformation of TaN film which was observed under high magnification microscope. On the contrary, the device with Al/TaN shows

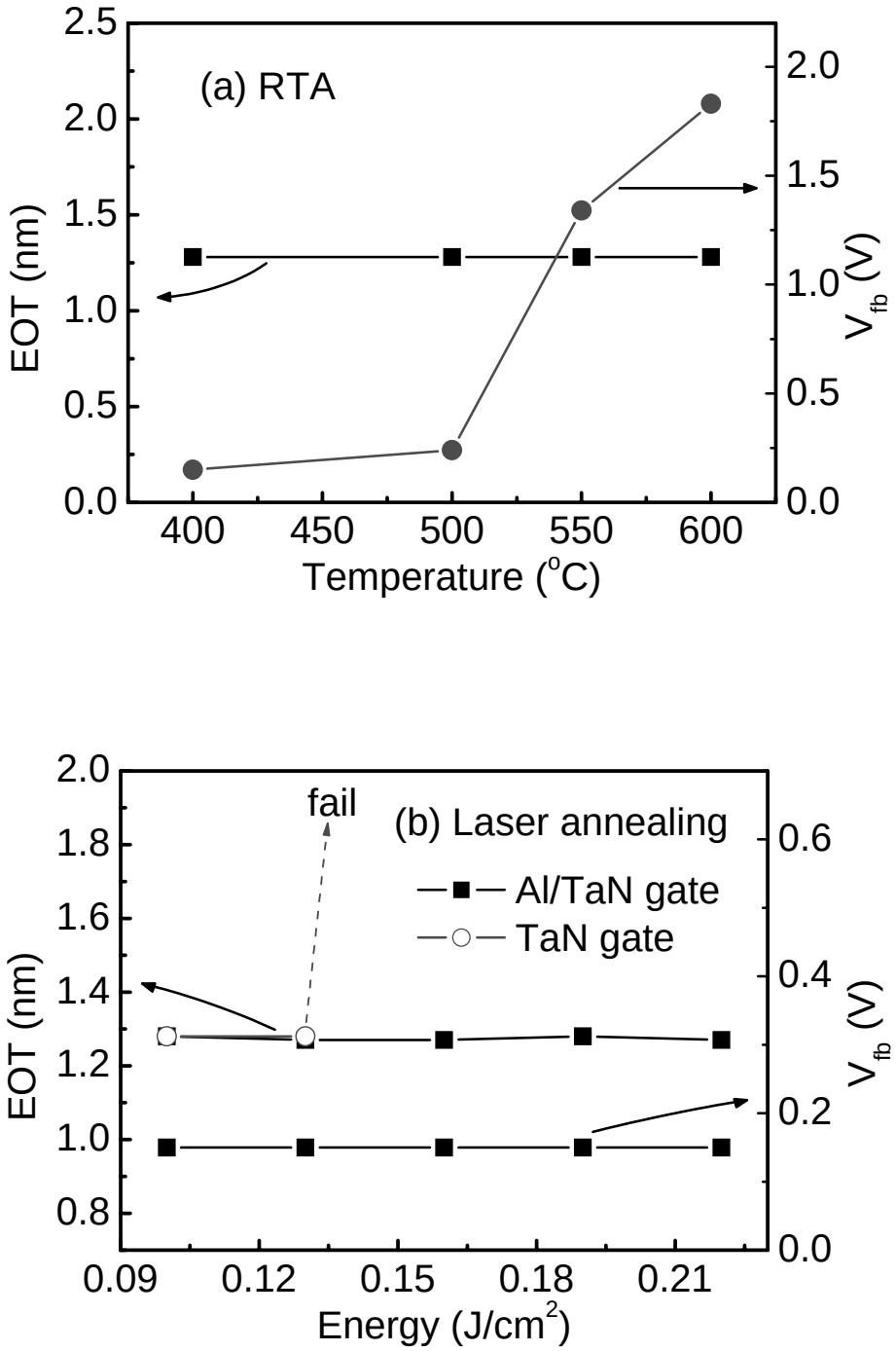

Figure 4.9. EOT and flatband voltage variations of Ge nMOS capacitors after (a) RTA and (b) laser annealing.

superior gate stack integrity after laser annealing. No EOT and flatband voltage variation is observed after laser annealing up to 0.22 J/cm^2.

The good thermal stability of device with Al/TaN owes to the higher reflectivity of Al with 248 nm laser than TaN. With the Al capping layer on TaN metal gate, much less energy is absorbed in the gate stack, and the S/D regions are selectively heated as shown in Figure 4.10 [4.16]. For 248 nm light, the reflectivity of Al is 92% and it is much higher than the reflectivity of TaN (69%) [4.15]. In addition, since the characteristic depth of absorption of 248 nm light in Al (6.7 nm) is much smaller than the Al layer thickness (200 nm), light could not penetrate through the Al capping. Therefore, most of laser light is reflected away from the Al capping layer rather than being absorbed in or penetrating through it. For TaN, to author's best knowledge, there is no report on its characteristic depth of absorption of 248 nm light. Since the characteristic depths of absorption of 248 nm light in most of metal films are less than 20 nm (e.g. ~9 nm for pure Ta), it is unlikely that 248 nm light can penetrate through

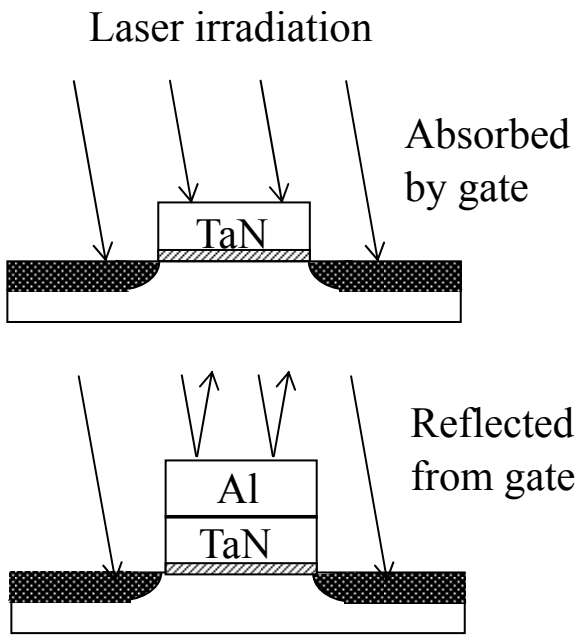

Figure 4.10. Schematics illustrating the selective heating of LTP with Al reflector on TaN gate.

150 nm TaN film. As a result, much more energy was absorbed by TaN than Al/TaN and the gate stack with pure TaN was thus heated up.

Figure 4.11 shows the excellent C-V characteristic of Ge nMOS capacitor with Al/TaN gate after laser annealing. The symbols represent the high-frequency C-V characteristic measured at 1 MHz. The line is the theoretical curve from a modified Berkeley simulator with parameters of Ge. A low EOT of 1.27 nm was extracted considering quantum effect. And a negligible hysteresis (<10 mV) was recorded from bi-direction sweeping between ±1 V. Figure 4.12(a) shows the output characteristics of Ge nMOSFETs with RTA and laser annealing activation. The device with 500 ^{o}C RTA activation shows a slow saturation behavior due to large source/drain series resistance, while the device with laser annealing offers well-behaved I_d-V_d characteristics. In addition, the device with laser annealing exhibits larger saturation current than RTA device (1.64 uA/um versus 1.47 uA/um @ Vg-Vth=0.5 V). Fig. 4.12(b) shows the transfer curve of device with laser annealing. The threshold

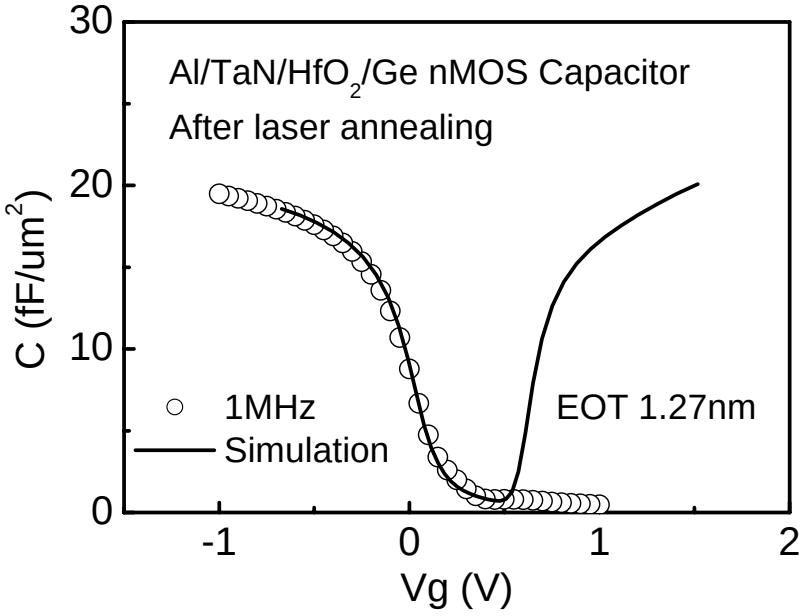

Figure 4.11. Capacitance-voltage characteristics of Ge nMOS capacitor with Al/TaN gate electrode after 0.14 J/cm^2 laser annealing.

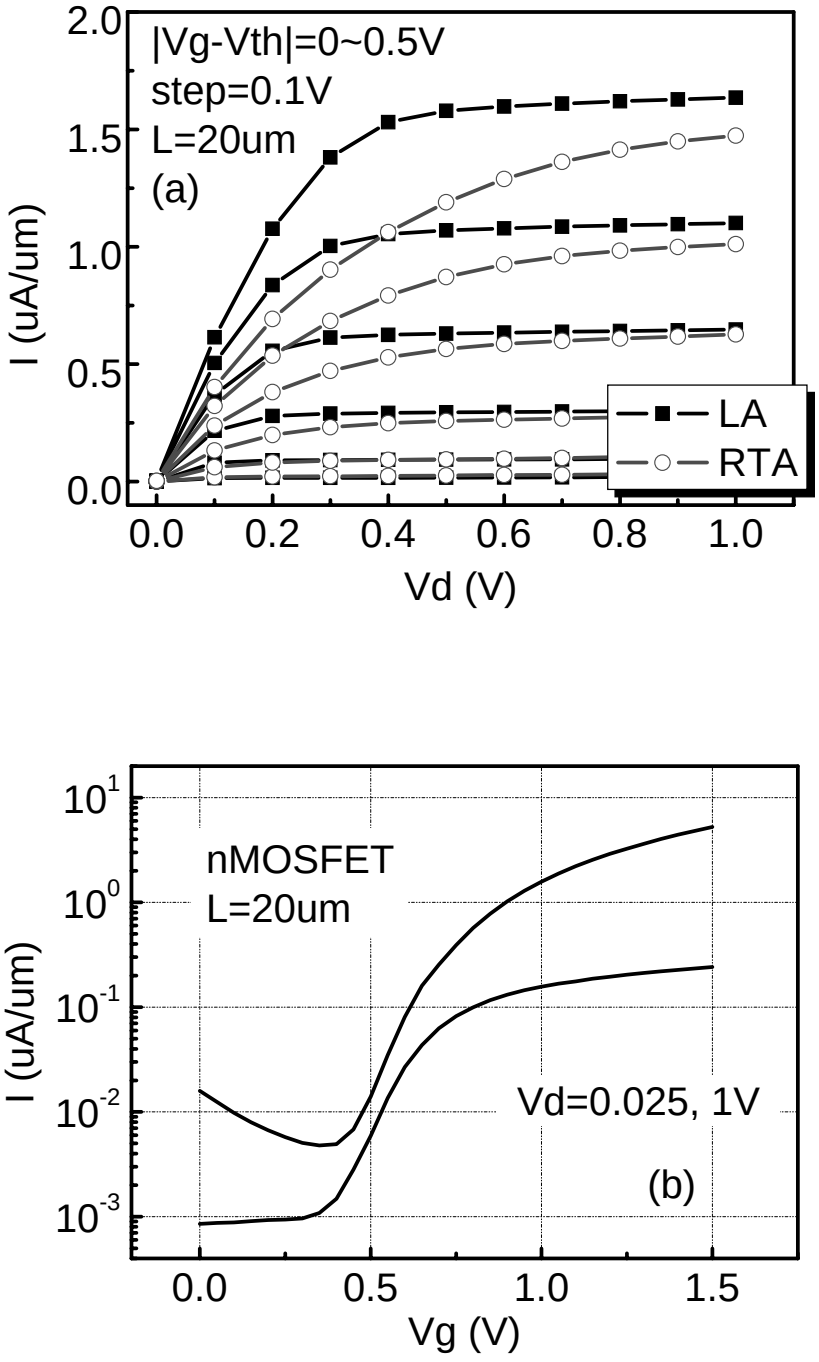

Figure 4.12. (a) Output and (b) transfer characteristics of Ge nMOSFET with laser annealing (LA) source/drain activation. The output curve of device with RTA was also included in (a) as a reference.

voltage is extracted to be 0.54 V, which is 0.19 V lower than the one with 500 ^{o}C RTA activation (0.73 V). This is consistent with our previous discussion that high temperature RTA results in additional negative fixed charge and hence a high threshold voltage. By implementing laser annealing, due to the selective heating, the flatband shift problem can be successfully eliminated and a low threshold voltage could be achieved. Figure 4.13 shows the electron mobility as a function of effective electrical field of Ge nMOSFETs by laser annealing and RTA activation as well as Si control device. An increased electron mobility at high effective electrical field region is observed in the device with laser annealing which attributes to the reduced series resistance. Compared with HfO_2/Si device, the Ge nMOSFET shows 175% of peak electron mobility.

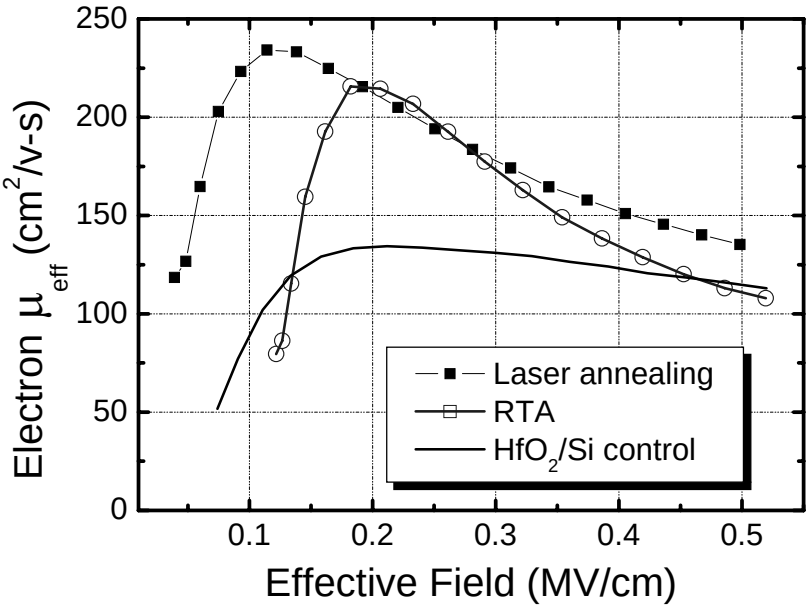

Figure 4.13. Extracted electron mobility as a function of effective electrical field for Ge nMOSFETs with laser annealing and RTA source/drain activation as well as an HfO_2/Si control device.

At last, laser annealing was also applied to Ge pMOSFET fabrication to demonstrate its compatibility to produce CMOS devices. A low EOT ~1.2 nm and a negligible hysteresis (<10 mV) were recorded with laser annealing, which are consistent with nFET shown in the Fig. 4.11. Figure 4.14(a) shows the Id-Vd characteristics of Ge pMOSFET. The device exhibited good turn-on and turn-off behavior and a relatively high on current of ~8.8 μA/μm at 1 V gate overdrive and 1 V drain voltage. Whereas, a slow saturated Id is observed with high gate overdrive. This implies that the source/drain series resistance is still not low enough even with laser annealing and compromises the drive current. The Id-Vg characteristic is shown in the Fig 4.14(b). An excellent sub-threshold swing of 77 mV/dec is recorded which is much better than Ge pMOSFET in the literature (100 mV/dec) [4.17] and is very close to the ideal value of 67 mV/dec. The on-off ratio of device is about 4 orders and it is comparable with device activated by RTA [4.17]. The hole mobility of Ge pMOSFET is shown in Fig. 4.15. The Ge device shows 1.9 times of the SiO_2/Si universal mobility and much beyond other reported Ge pMOSFET with high-κ [4.17][4.18].

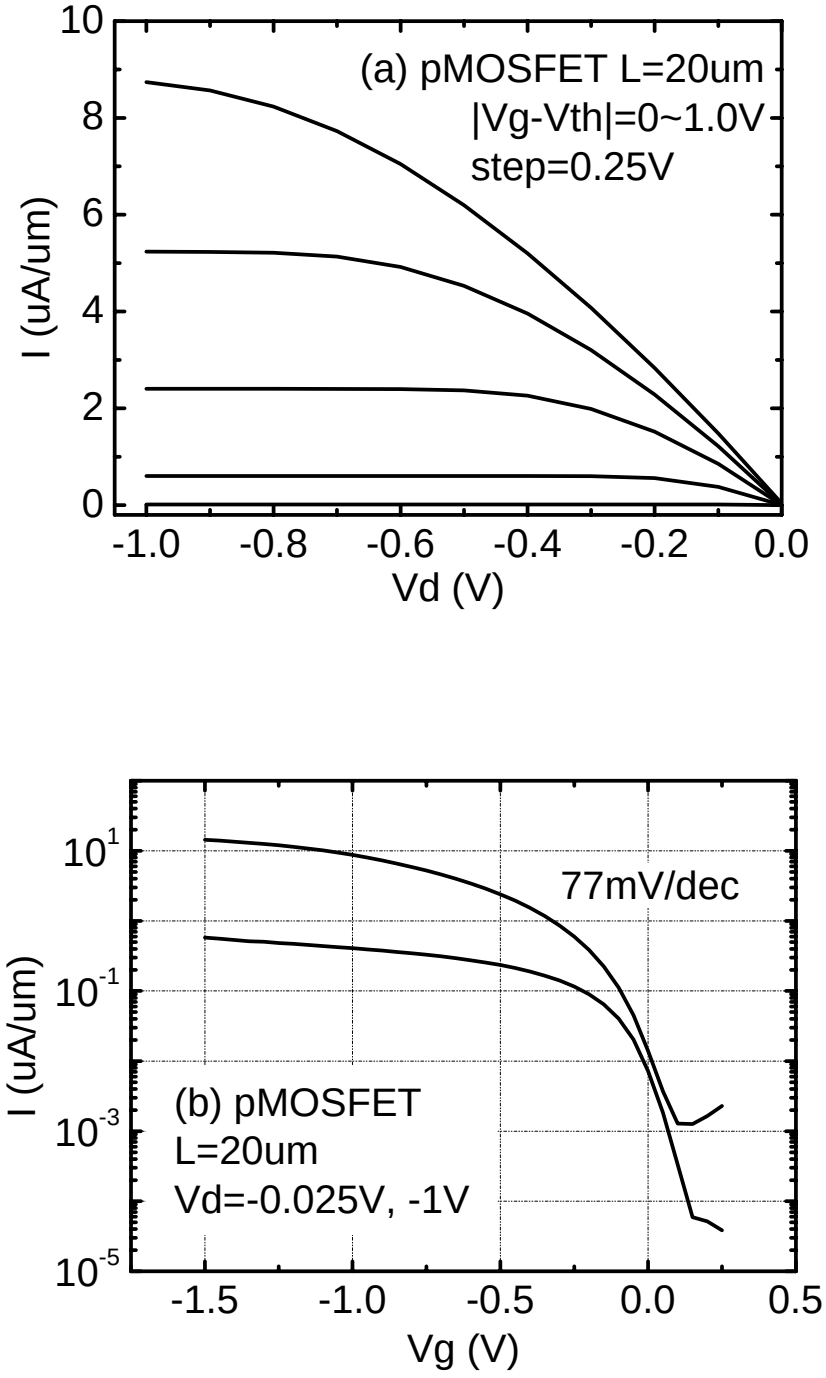

Figure 4.14. Output (a) and transfer (b) characteristics of Ge pMOSFET with laser annealing (LA) source/drain activation.

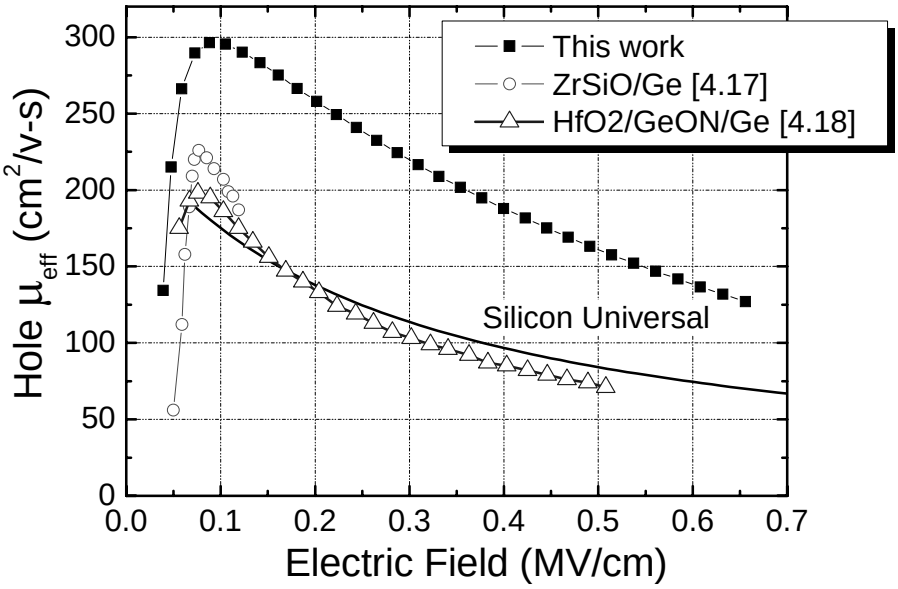

Figure 4.15. Extracted hole mobility as a function of effective electrical field for Ge pMOSFETs with laser annealing.

4.4 Conclusion

For the first time, gate-first self-aligned Ge MOSFETs with metal gate and CVD HfO_2 have been successfully fabricated, using a novel laser annealing dopant activation. Compared with conventional rapid thermal annealing source/drain activation, laser annealing provides shallower junction depth and smaller sheet resistance at a same time. Furthermore, by applying an aluminum laser reflector on the TaN gate, S/D regions of MOSFET are selectively annealed without heating gate stack. Good gate stack integrity and small S/D series resistance are achieved simultaneously. With these benefits, a larger drive current, a lower threshold voltage and a higher electron mobility at high effective electrical field are achieved in Ge nMOSFET with laser annealing activation than that with RTA activation. High mobility Ge pMOSFETs with excellent characteristics are also demonstrated with laser annealing.

References

[4.1] C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat, "Activation and diffusion studies of ion-implanted p and n dopants in germanium," Appl. Phys. Lett., vol. 83, pp.3275, Oct., 2003.

[4.2] Kevin S. Jones and E. E. Haller, "Ion Implantation of Boron in Germanium," J. Appl. Phys., vol. 61, pp. 2469, Apr, 1987.

[4.3] H. Shang, K.-L. Lee, P. Kozlowski, C. D. Emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, and W. Haensch, "Self-Aligned n-Channel Germanium MOSFETs With a Thin Ge Oxynitride Gate Dielectric and Tungsten Gate," IEEE Electron Device Lett., v. 25, pp. 135, 2004.

[4.4] C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat, "Germanium n-type shallow junction activation dependences," Applied Physics Lett., vol. 87, pp.91909, Aug., 2005.

[4.5] C. H. Poon, L. S. Tan, B. J. Cho, and A. Y. Du, "Dopant loss mechanism in n^+/p germanium junctions during rapid thermal annealing," J. Electrochem. Soc., vol.152, pp. G895, 2005.

[4.6] J. J.-H. Chen, N. A. Bojarczuk, Jr., H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al_2O_3 and HfO_2 gate dielectrics on surface-nitrided Ge," IEEE Trans. Electron Devices, vol.51, p.1441, Sep., 2004.

[4.7] W. P. Bai, N. Lu, and D.-L. Kwong, "Si interlayer passivation on germanium MOS capacitors with high-κ dielectric and metal gate," IEEE Electron Devices Lett., vol. 26, p.378, June, 2005.

[4.8] B. Yu, Y. Wang, H. Wang, Q. Xiang, C. Riccobene, S. Talwar, and M. Lin, "70nm MOSFET with Ultra-Shallow, Abrupt, and Super-Doped S/D

Extension Implemented by Laser Thermal Process (LTP)," Tech. Dig. - Int. Electron Devices Meet. (IEDM), 1999, pp.509.

[4.9] N. Wu, Q. C. Zhang, C. X. Zhu, C. Shen, M. F. Li, D.S.H Chan, and N. Balasubramanian, "BTI and charge trapping in germanium p-and n-MOSFETs with CVD HfO2 gate dielectric," Tech. Dig. - Int. Electron Devices Meet. (IEDM), 2005, pp. 563.

[4.10] C. H. Huang, D. S. Yu, A. Chin, W. J. Chen, C. X. Zhu, M.-F. Li, B. J. Cho, and D. L. Kwong, "Fully silicided NiSi and germanided NiGe dual gates on SiO_2–Si and Al_2O_3 /Ge-on-insulator MOSFETs," in IEDM Tech. Dig., 2003, pp. 319.

[4.11] F. Vega, R. Sema, C. N. Afonso, D. Bermejo and G. Tejeda, "Relaxation and crystallization kinetics of amorphous germanium films by nanosecond laser pulses," J. Appl. Phys., vol.75, pp. 7287, Jun, 1994.

[4.12] Sungho Heo, Sungkweon Baek, Dongkyu Lee, Musarrat Hasan,Hyungsuk Jung, Jongho Lee, and Hyunsang Hwanga, "Sub-15 nm n+/p-Germanium Shallow Junction Formed by PH3 Plasma Doping and Excimer Laser Annealing," Electrochem. and Solid-State Lett., vol.9, G136, 2006.

[4.13] Q. C. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C.X. Zhu, "Germanium incorporation in HfO2 dielectric on germanium substrate," J. Electrochem. Soc., vol.153, pp. G207, 2006.

[4.14] Q. C. Zhang, N. Wu, L. K. Bera, and C. X. Zhu, "Germanium out-diffusion in HfO2 and its impact on electrical properties," Tech. Dig. of Solid State Device Meeting (SSDM), P1-14, 2005.

[4.15] Handbook of Chemistry and Physics, chapter 12, CRS press.

[4.16] S. Baek, S. Heo, H. Choi, and H. Hwang, "Characteristics of HfO_2 pMOSFET prepared by B2H6 plasma doping and KrF excimer laser

annealing," IEEE Electron Devices Lett., vol. 26, p.157, March, 2005.

[4.17] Y. Kamata, Y. Kamimuta, T. Ino, R. Lijima, M. Koyama, and A. Nishiyama, "Dramatic improvement of Ge p-MOSFET characteristics realized by amorphous Zr-Silicate/Ge gate stack with excellent structural stability through process temperatures," Tech. Dig. - Int. Electron Devices Meet. (IEDM), 2005, pp. 441.

[4.18] A. Riteaour, S. Yu, M.L. Lee, N. Lu, W. Bai A. Pitera, E.A. Fitzgerald, D.L. Kwong and D.A. Antoniadis, "Epitaxial Strained Germanium p-MOSFETs with HfO2 Gate Dielectric and TaN Gate Electrode," Tech. Dig. - Int. Electron Devices Meet. (IEDM), 2003, pp.433.

Chapter 5

Formation and Characterization of Nickel Germanide Contact

5.1 Introduction

Germanium is always an interesting material for metal oxide semiconductor field effect transistor (MOSFET) application because of its high intrinsic mobility (two times higher for electrons and four times higher for holes as compared to those in Si). Recently, germanium MOSFETs with high-κ gate dielectrics have attracted lots of interests as a potential solution for high-scaled CMOS technology. Although Ge MOSFETs with germanium oxynitride, ZrO_2 and HfO_2 gate dielectrics have been successfully demonstrated, very high source/drain series resistance was observed in these Ge MOSFETs and severely degraded the device performance [5.1][5.2][5.3]. A high source/drain series resistance is also observed in the previous chapters of this thesis. Self-aligned silicide is essential in current deep-sub micron very-large-scale-integrated circuit fabrication to reduce parasitic source/drain resistance. Titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$) and nickel silicide (NiSi) have been extensively studied. Titanium silicide was widely used in sub-micron CMOS technologies, however, it has been replaced by cobalt silicide for the sub-0.25 μm technology nodes. Nickel silicide, considered as the material choice for the future nodes, has several advantages over titanium silicide and cobalt silicide which include: low temperature

silicidation, no bridging failure property, small mechanical stress, low silicon consumption, and one step silicidation process [5.4]. Similarly, Ni shows advantages of forming germanide for Ge MOSFET application over other materials. It has been reported that high processing temperatures are required to form low-resistivity titanium germanide (>800 ^{o}C) and cobalt germanide (>500 ^{o}C), while nickel germanide can be formed at a low temperature of 270 ^{o}C [5.5]. Such a low processing temperature is effective to prevent the degradation of high-κ gate stack on germanium substrate and makes nickel germanide more suitable for Ge device fabrication.

In this chapter, the formation of nickel germanide on single crystal germanium substrate by rapid thermal annealing (RTA) was investigated over a wide range of temperatures (250–700 ^{o}C). Various characterization methods including sheet resistance measurement, spectroscopic ellipsometry (SE), X-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectroscopy (RBS) and scanning electron microscopy (SEM) were employed to study the physical and electrical properties of nickel germanide. In addition, the application of self-aligned NiGe contact on germanium junctions was demonstrated.

5.2 Experiment

Nickel germanide formation was carried out on (100) single crystal germanium substrates. First, the substrates were dipped in diluted-HF solution (1:20) to remove the native oxide and passivate the surface with hydrogen. After that, the substrates were transferred into an E-beam evaporator with a base pressure of 5 x 10^{-7} mbar. Ni films with different thicknesses were deposited at room temperature. Following that, nickel germanide was formed by RTA at temperatures ranging from 250 ^{o}C to 700 ^{o}C under N_2 at atmosphere. To study the thermal degradation behavior, several NiGe

samples, formed at the same condition (400 ^{o}C, 30 sec), were subsequently annealed at different temperatures ranging from 450 ^{o}C to 650 ^{o}C. A four-point probe was used to measure the sheet resistance of nickel germanide films. Rutherford backscattering spectroscopy, with a 2 MeV He^{+} ion beam of approximate 5 μm^2 raster-scanned over a square pad of 50 x 50 μm^2, was used to measure the thicknesses of as-deposited Ni and nickel germanide films as well as the film composition. Scanning electron microscopy was employed to examine the morphology of the films. Optical properties of nickel germanide were investigated by Sentech SE800 spectroscopic ellipsometer with wavelength at 300-900 nm. The nickel germanide film composition was studied by a JEOL X-ray photoelectron spectroscopy machine with an Al source.

To evaluate the electrical performance of NiGe as contact, Ge n^{+}/p diode was also fabricated. A thick SiO_2 was deposited on bare germanium substrate as field isolation, followed by active area definition and etching. Arsenic dopants ($1X10^{15}$ cm^{-2} @120 keV) were implanted into p-type substrates and activated at 600 ^{o}C. After a dilute-HF cleaning, 30 nm nickel was deposited by E-beam evaporator and annealed at 400 ^{o}C for 30 s by RTA. After annealing, the spare Ni was removed by diluted HNO_3 (1:20). A thick Al film (500 nm) was deposited on the backside of devices by E-beam evaporation to form a good contact. The diode I-V characteristics were measured using an HP4155B semiconductor parameter analyzer.

5.3 Formation of Nickel Germanide

5.3.1 Sheet resistance measurement

Nickel germanide formation was first studied over a wide range of temperatures. Figure 5.1 shows the sheet resistance (R_s) of nickel germanide as a function of annealing temperature with initial Ni film thickness (nominal) of 10 nm and 20 nm.

For comparison, the sheet resistance of the silicide formed by reaction of nominal 20 nm Ni on single crystal silicon is also shown in Fig. 5.1. The nickel germanide shows a similar trend of sheet resistance versus annealing temperature with nickel silicide. All the films exhibit high sheet resistances at low temperatures due to the formation of Ni-rich phases (predominantly Ni_2Si, Ni_2Ge or Ni_5Ge_3) [5.4][5.6][5.7]. At elevated temperatures, the sheet resistance maintains at a minimum value over a range of temperatures (400-550 ^oC for germanide, 400-700 ^oC for silicide with 20 nm initial Ni). In this temperature range, mono-silicide or mono-germanide films were formed. When the annealing temperature increases further, a sharp and slight increase in the sheet resistance of nickel germanide and silicide are observed due to the thermal degradation, respectively. It is noticed that the thermal degradation of germanide films occur at lower temperatures than that of NiSi films (Fig. 5.1). Hsu *et al* reported similar results on NiGe on single-and poly crystalline Ge substrates [5.8].

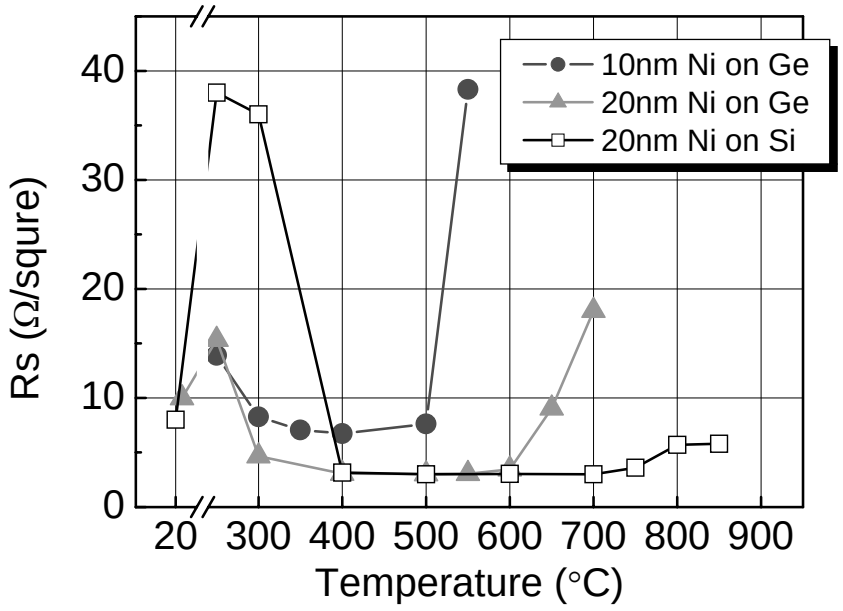

Figure 5.1. The sheet resistance of NiGe formed at temperatures ranging from 250 ^oC to 700 ^oC for 30 sec. The sheet resistance was measured after removing the unreacted Ni by wet etching after reaction. The nominal 10 nm and 20 nm Ni films were deposited on (100) single crystalline germanium and silicon substrates.

It is well known that the thermal degradation of NiSi at high temperature includes two mechanisms: agglomeration and phase transformation [5.9]. The desired low-resistivity phase NiSi tends to transform to high-resistivity $NiSi_2$ above 700 ^oC which accounts for the high sheet resistance plateau around 800 ^oC. Further increasing annealing temperature will cause the initial continuous silicide film to break up into discrete silicide islands. On the contrary, the nickel germanide shows a different degradation characteristic. The NiGe does not transform to Ge-rich phase after annealing since no Ge-rich phase (>50 at.% Ge) exists in the equilibrium phase diagram [5.10]. Morphological degradation due to the agglomeration is the only mechanism of thermal degradation of NiGe. The agglomeration of NiGe starts with grain boundary grooving and results in islands formation, as the same as silicide agglomeration [5.11]. The agglomeration is driven by the minimization of the total surface/interface energy of the germanide and germanium substrate [5.12]. In addition, it is noted from Fig. 5.1 that the temperature at which agglomeration occurs decreases with reducing film thickness. This is also consistent with the grooving model of agglomeration.

5.3.2 RBS analysis

RBS was employed to measure the thickness as well as composition of the films. The RBS result of nominal 20 nm as-deposited Ni film fits well with the simulation curve of 22 nm pure nickel on germanium substrate [Fig. 5.2(a)]. The RBS analysis also confirms that mono-nickel-germanide was formed after 500 ^oC annealing and the film thickness is 58 nm [Fig. 5.2(b)]. Therefore, the thickness ratio of the NiGe film to the as-deposited Ni film is about 2.55 which is consistent with the result from other group (2.5 ± 0.1) [5.13]. With the knowledge of the thickness and

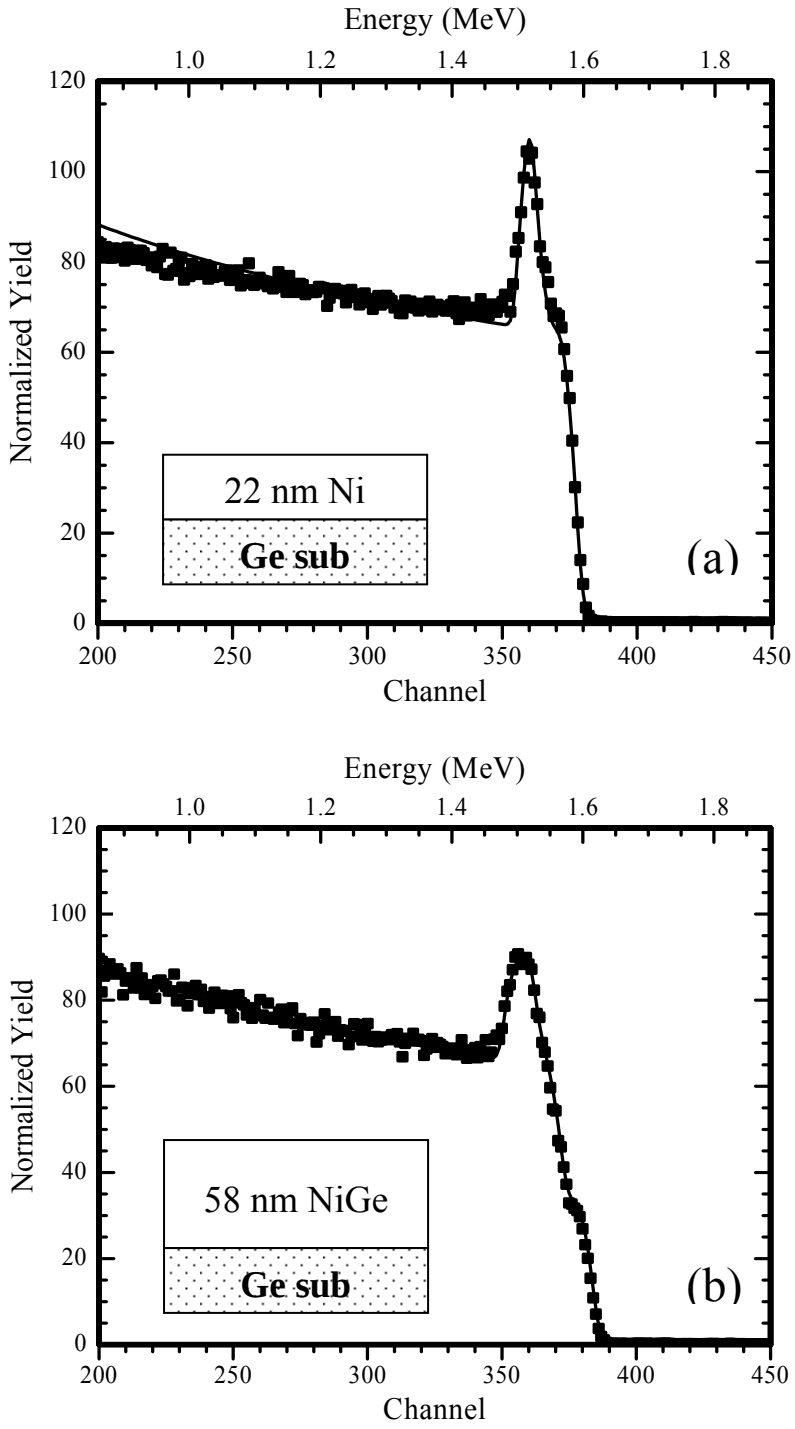

Figure 5.2. RBS spectrum of (a) as-deposited Ni on Ge substrate and (b) NiGe formed at 500 ^{o}C. The symbols are the RBS experimental data and the solid line is the simulation curve of the film structure as shown in the inset.

sheet resistance, the resistivity of NiGe is extracted to be 14 μΩ-cm from a series of NiGe samples with different as-deposited Ni thicknesses. This value is comparable with the resistivity of NiSi (14 μΩ-cm) and the resistivity of NiSiGe (18 μΩ-cm) [5.9][5.14].

5.3.3 Spectroscopic ellipsometry characterization

Ellispometry is a fast, sensitive and non-destructive method for monitoring film properties and measuring thickness and layers uniformity. It measures the change in polarization of a circularly polarized incident light beam by interaction with a sample. When the measurement is performed at various wavelengths, it is called spectroscopic ellipsometry. The spectroscopic ellipsometry records the complex reflectance ratio ρ as a function of the incident light wavelength. For isotropic materials,

$$\rho = \frac{r_p}{r_s} = \tan\Psi e^{i\Delta},$$

where r_p and r_s are the complex reflection coefficients of light polarized parallel (p) and perpendicular (s) to the plane of incidence. The relative phase change is denoted as Δ, while the amplitude is denoted as Ψ. During the measurement, these angles are recorded as a function of the wavelength of the incident light.

Figure 5.3 shows the ellipsometric spectra of bare germanium substrate, pure nickel film on Ge and nickel germanide annealed at 200, 250, 300, 400, 500, and 600 °C. It is noticed that the spectrum of 200 ^{o}C is same with that of pure nickel and a great change in spectrum happens after annealing at temperatures ≥300 ^{o}C. At elevated temperatures ranging in 400-500 ^{o}C, the spectra remain identical and are irrelevant with annealing temperature. When the annealing temperature is further increased to 600 ^{o}C, a big change in spectrum from that of 500 ^{o}C is observed. The

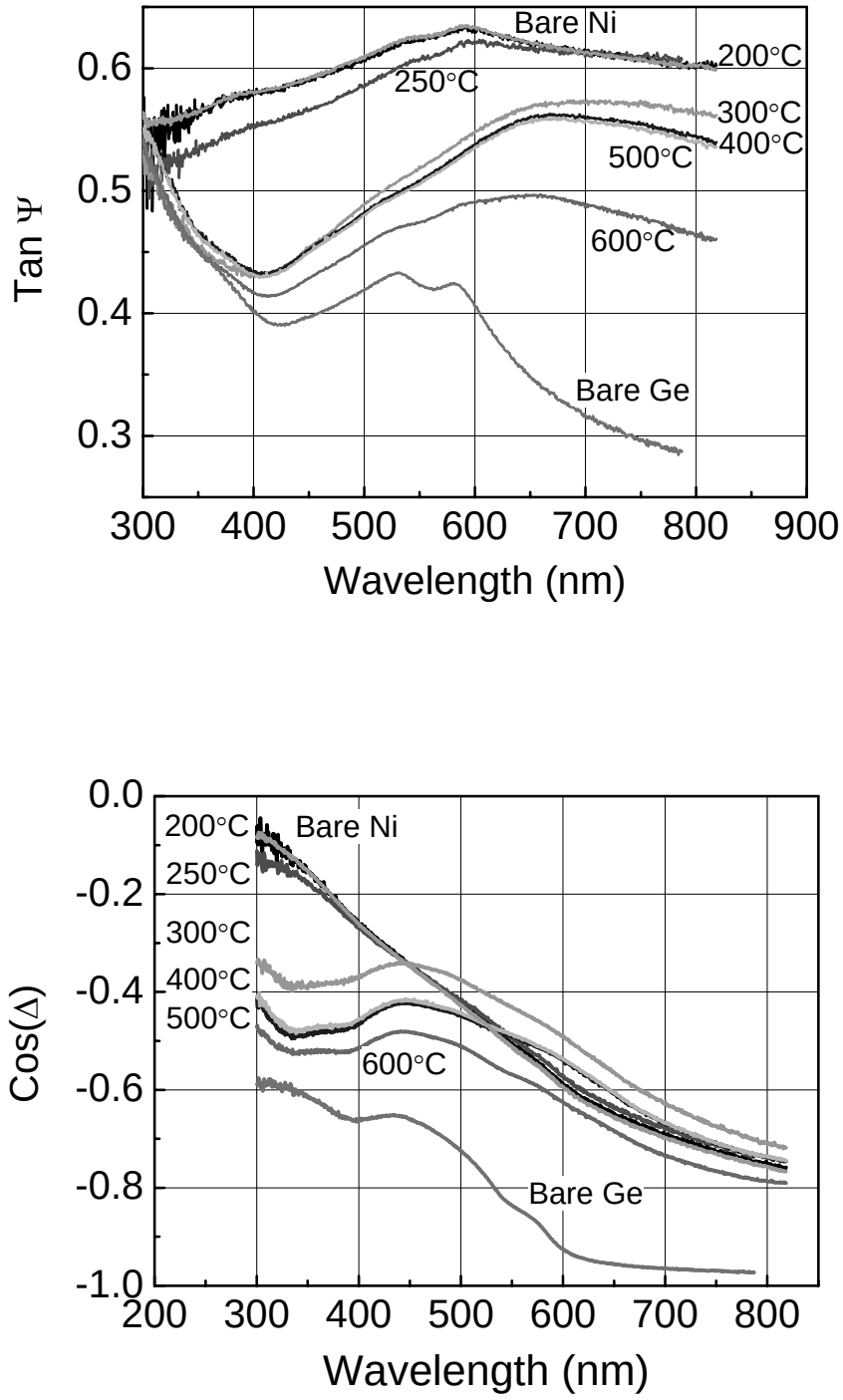

Figure 5.3. Spectroscopic ellipsometry results of pure germanium substrate, as-deposited Ni films and nickel germanide annealed at 200, 250, 300, 400, 500 and 600 ^{o}C.

evolution of ellipsometric spectra can be explained by the nickel germanium formation and phase transformation and is fully consistent with sheet resistance measurement. After low temperature (250-300 ^{o}C) annealing, nickel-rich germanide films are first formed. As the annealing temperature increases, the germanium composition in germanide film increases and approaches 50%. Correspondingly, the spectrum evolves from pure nickel like to mono-NiGe like. After annealing at 400-500 ^{o}C, uniform mono-nickel-germanide films are formed. Therefore, there is no change in spectrum within this temperature range. Annealing at elevated temperature results in agglomeration, hence the spectrum deviates from that of NiGe and is getting similar to that of bare Ge substrate.

In order to measure the NiGe thickness by ellipsometer, it is necessary to obtain the refractive index of NiGe. The data reduction function in the program of SE800 ellipsometer allows calculation of the index of refraction and thickness of a layer

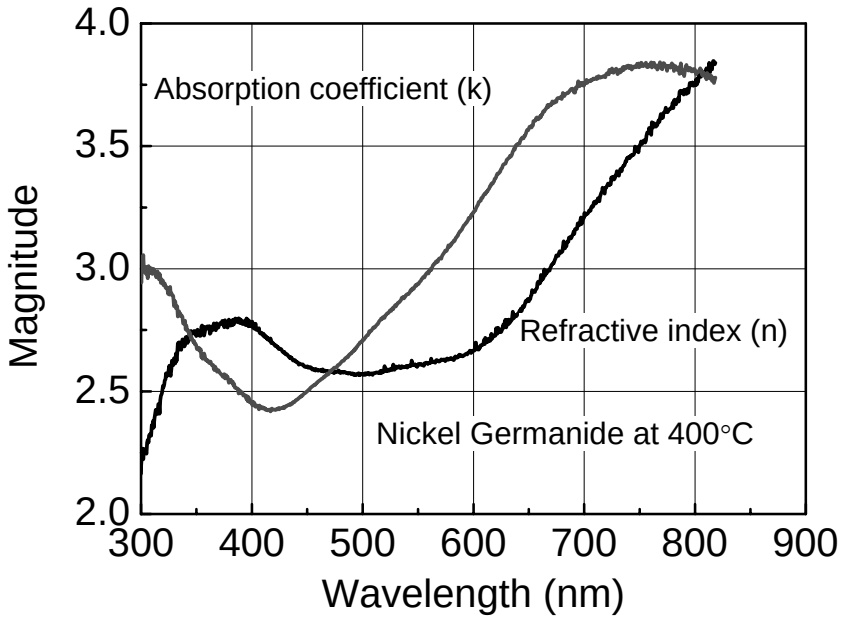

Figure 5.4. Refractive index (n) and extinction coefficient (k) of NiGe film formed at 400 ^{o}C.

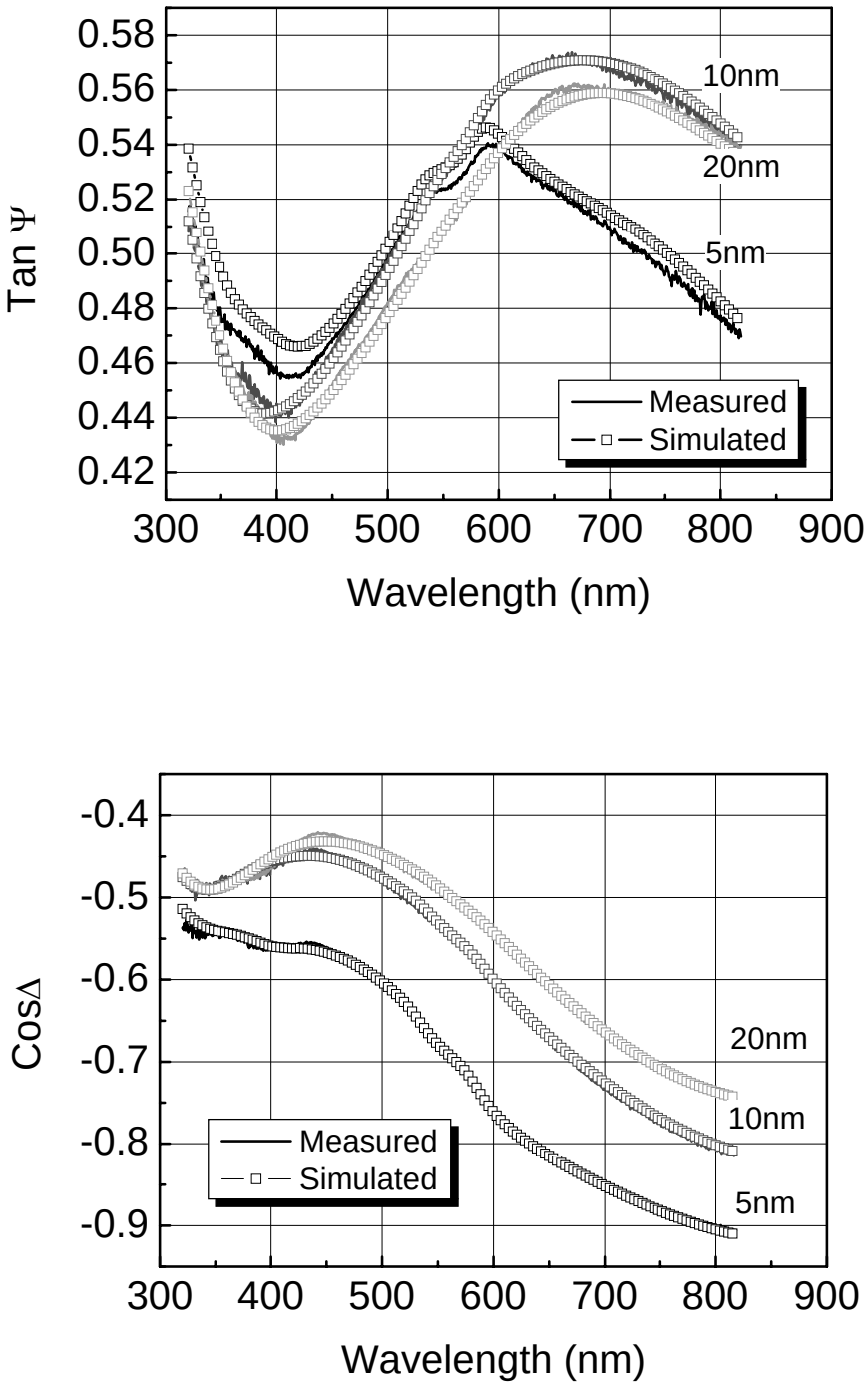

Figure 5.5. The measured and simulated spectrum of NiGe with various initial Ni thicknesses.

inside a multilayer structure based on a known disperse law for indexes n and k versus wavelength. Drude-Lorentz model [5.15], which is suitable for metal-like film, is chosen to model the refractive index of NiGe. The real (n) and imaginary (k) parts of the refractive index of NiGe films are shown in Figure 5.4. With the obtained refractive index of NiGe, the film thickness was successfully measured. Figure 5.5 shows the measured and simulated spectrum of NiGe with various initial Ni thicknesses. With 5.6, 12.1, 21 nm initial Ni films, the measured thicknesses of NiGe by ellipsometer are 12.5, 30, 55 nm, respectively. It agrees well with ratio of NiGe/Ni of 2.55 and is consistent with result of RBS measurement. Note that, for the 5 nm initial Ni film, there is a small deviation of simulation curve from the measured spectra of NiGe with a smaller tanΨ. It is possible due to the agglomeration of ultra-thin NiGe film. As discussed above, it is more feasible for thinner NiGe to agglomerate after annealing. A noticeable agglomeration has been observed after 500 ^{o}C 30 s annealing for 10 nm initial Ni film. Therefore, for a 5 nm initial Ni film, agglomeration may occur after 400 ^{o}C 30 s annealing. As a result, there is difference between simulated and measured ellipsometric spectrum.

5.3.4 Film composition profile by XPS characterization

Figure 5.6 shows the XPS depth profiles of NiGe films after annealing at 200, 250, 300 and 400 ^{o}C. As seen is Fig. 5.6(a), the film remained as pure nickel after 200 ^{o}C annealing. It is corresponding to the measured SE spectrum which is as same as pure nickel. After 250 ^{o}C annealing, a bi-layers structure consisting with a pure nickel on the top and a Ni-rich germanide layer underneath was formed. Accordingly, the SE spectrum has a small change from pure nickel. The depth profiling at 300 ^{o}C shows a uniform layer with a slightly higher Ni composition (54%) than Ge (46%).

The non-stoichiometric germanide film formed at 300 ^{o}C is possible due to the embedded Ni-rich germanide particle in the film [5.11]. The size of these particles diminishes with increasing temperature and disappears at 400 ^{o}C. As shown in Fig. 5.6(d), the depth profile of sample annealed at 400 ^{o}C shows an even closer 1:1 ratio of Ni to Ge composition. The result is consistent with the SE results (Fig.5.4) that mono–nickel-germanide is formed at 400 ^{o}C. The nickel-rich property of the film annealed at 300 ^{o}C was observed in the SE spectrum (Fig. 5.4). The spectrum of film annealed at 300 ^{o}C is between that of pure Ni and NiGe annealed at 400 ^{o}C and is close to that of NiGe but has a small deviation.

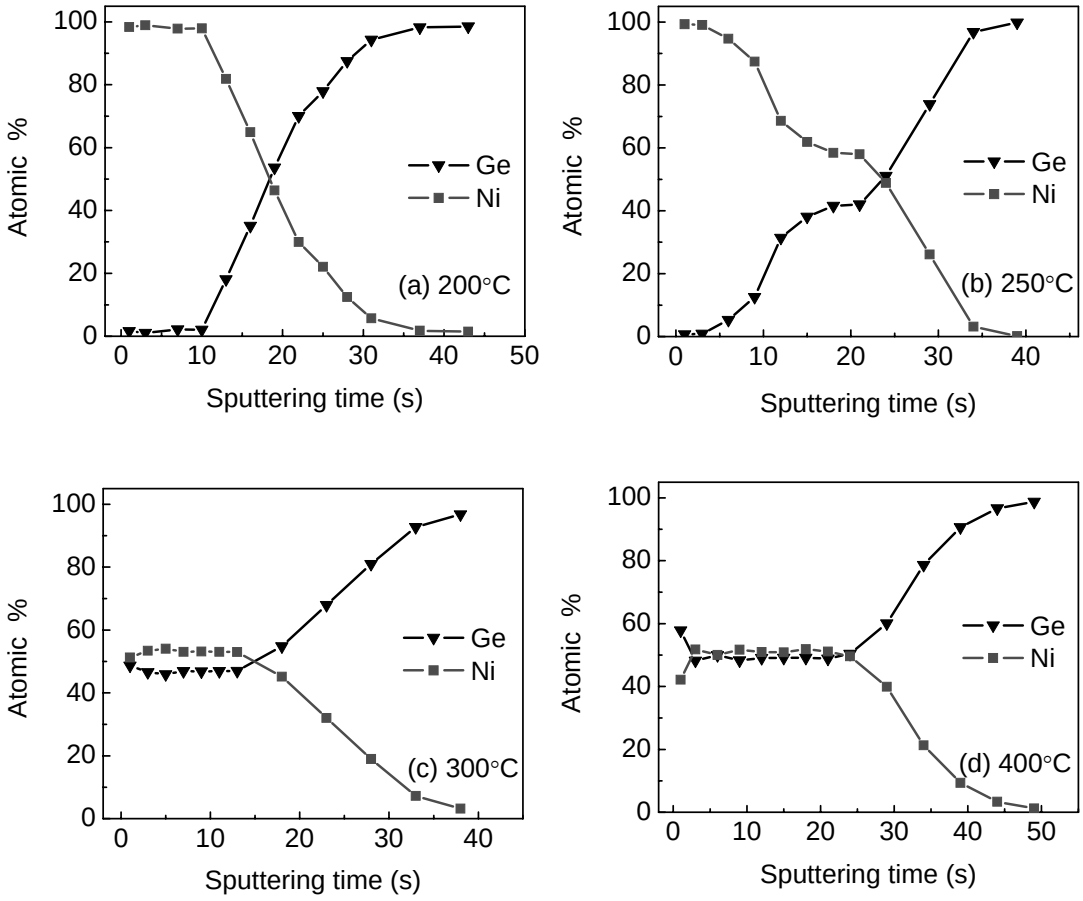

Figure 5.6. XPS depth profiles of NiGe films after annealed at (a) 200, (b) 250, (c) 300 and (d) 400 ^{o}C.

5.3.5 Scanning electron microscope analysis

The NiGe films annealed at temperature of 400, 500, 600, 700 ^{o}C with 15 nm initial nickel thickness were analyzed by scanning electron microscope (SEM). The samples annealed at 400-500 ^{o}C showed smooth and continuous films [Fig. 5.7 (a)(b)]. The sample annealed at 600 ^{o}C was partially agglomerated [Fig. 5.7(c)] and the sample annealed at 700 ^{o}C agglomerated and broke into separated islands [Fig. 5.7(d)]. This is consistent with our previous results that the Rs increases with high temperature annealing due to agglomeration.

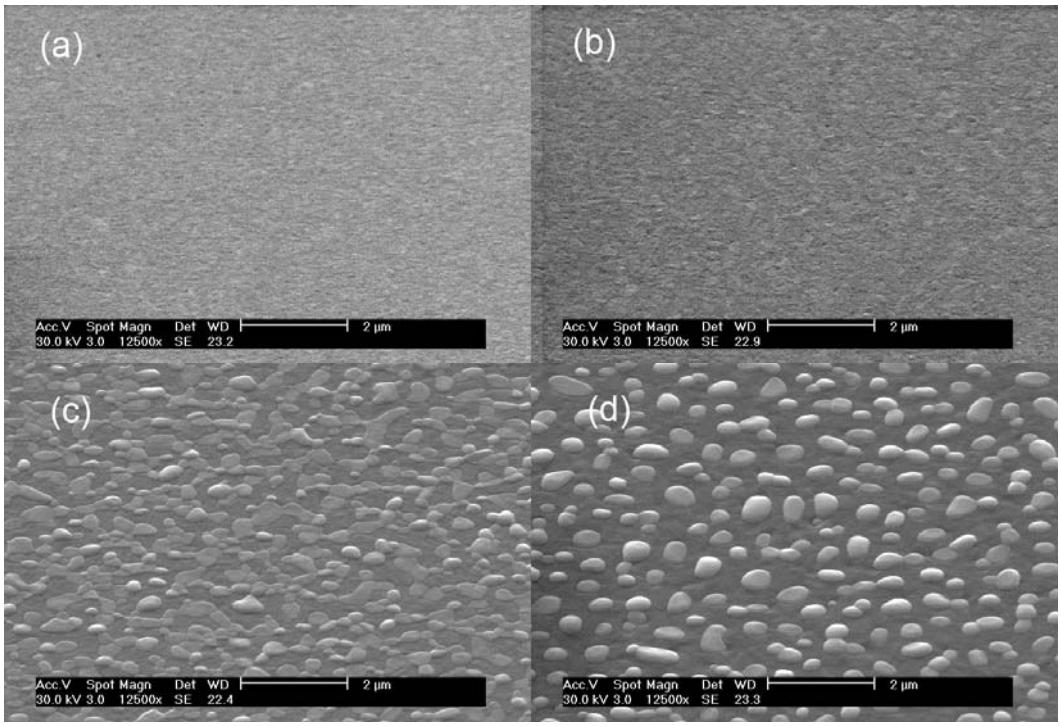

Figure 5.7. SEM pictures of nickel germanide formed at annealing temperature of (a) 400, (b) 500, (c) 600 and (d) 700 ^{o}C. The initial Ni thickness is 15 nm.

5.4 The Thermal Stability of Nickel Germanide

The results above have shown that the thermal stability of nickel germanide is poor and the agglomeration occurs at a relative low temperature compared with nickel

silicide. In this section, the dependence of agglomeration of NiGe on both annealing temperature and time was studied by monitoring the sheet resistance variation. The germanide films were first formed by the same RTA condition (400 ^{o}C, 30 sec). Following that, the samples were subsequently annealed at different temperatures and durations. Figure 5.8 shows the sheet resistance ratio (R_s/R_{s0}) of NiGe, formed with nominal 10 nm and 20 nm Ni on Ge substrates, as a function of annealing time at varying temperatures, where R_{s0} is the initial sheet resistance value measured after NiGe formation annealing and R_s is the sheet resistance measured after the second annealing. All the sheet resistance ratios increase linearly with annealing time at different annealing temperatures. A higher annealing temperature leads to a faster increase in R_s/R_{s0}. These results are consistent with the morphological degradation due to agglomeration.

To further characterize the thermal degradation of NiGe, the activation energy of agglomeration was estimated. Figure 5.9 shows the Arrhenius plots of $ln\tau_0(T)$ as a function of 1/kT for NiGe formed with 10 nm and 20 nm Ni on germanium substrates, where $\tau_0(T)$ is degradation time defined as the time at a given temperature (T) corresponding to a 20% increase in sheet resistance (R_s) from its initial sheet resistance (R_{s0}). From Fig. 5.9, the activation energy of NiGe agglomeration is estimated to be 2.2±0.2 eV. The activation energy value of NiGe agglomeration is smaller than the reported values of NiSi. By measuring the degradation of sheet resistance of NiSi films, Chamirian *et al* reported the activation energy values to be 2.5±0.25 eV and 2.6±0.3 eV for the n^+ and p^+ Si(100) substrates, respectively [5.16]. Colgan *et al* also reported that the activation energy of the NiSi agglomeration was2.9±0.2 eV with the same method [5.17]. Okubo *et al* reported activation energy at 2.8±0.4 eV by calculating exposed-Si area [5.18]. They suggested that the

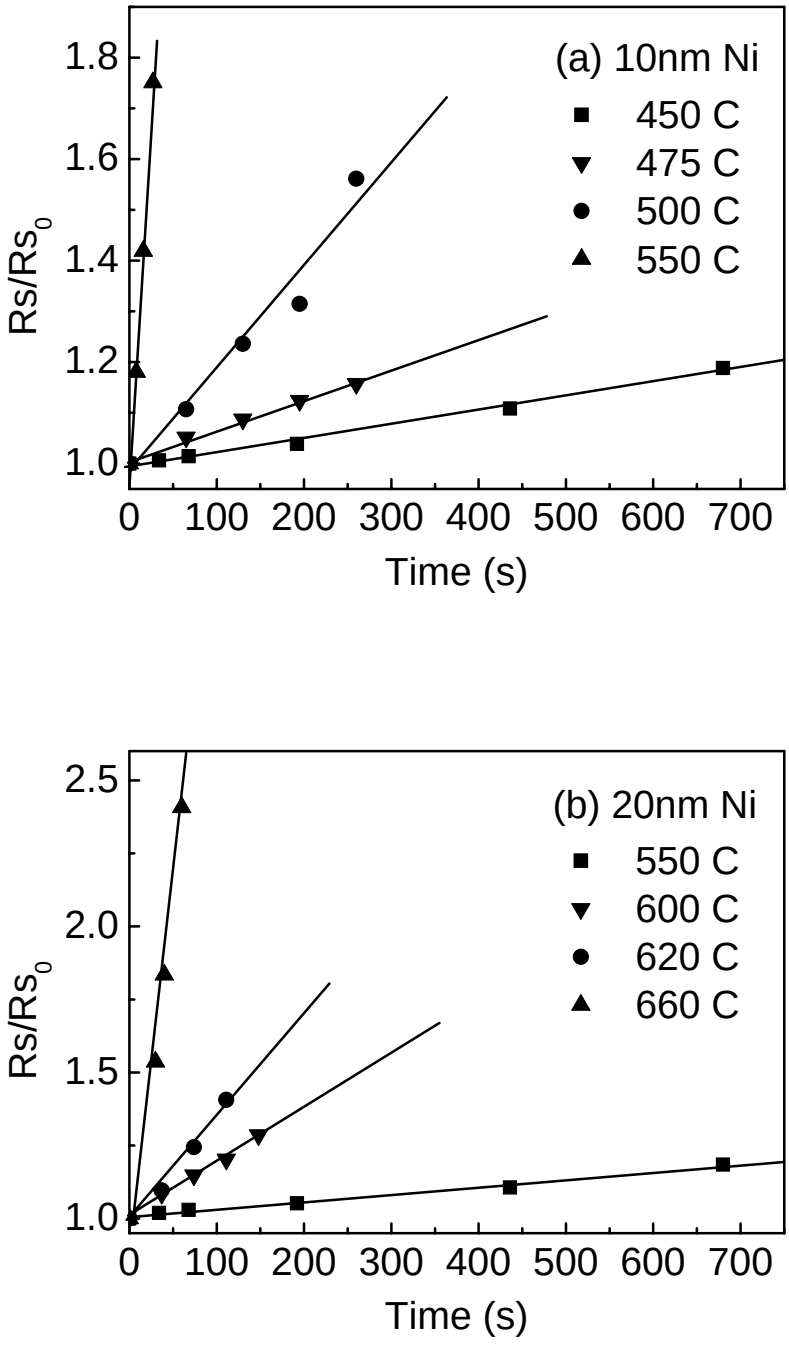

Figure 5.8. Evolution of NiGe sheet resistance with annealing time for samples with (a) 10 nm as-deposited Ni and (b) 20 nm as-deposited Ni.

activation energy of NiSi agglomeration corresponded to the energy needed for adding a Si atom to the epitaxial Si that grows between NiSi grains. The lower activation energy of the NiGe agglomeration could be attributed to the lower activation energy of Ge epitaxy than Si epitaxy [5.19].

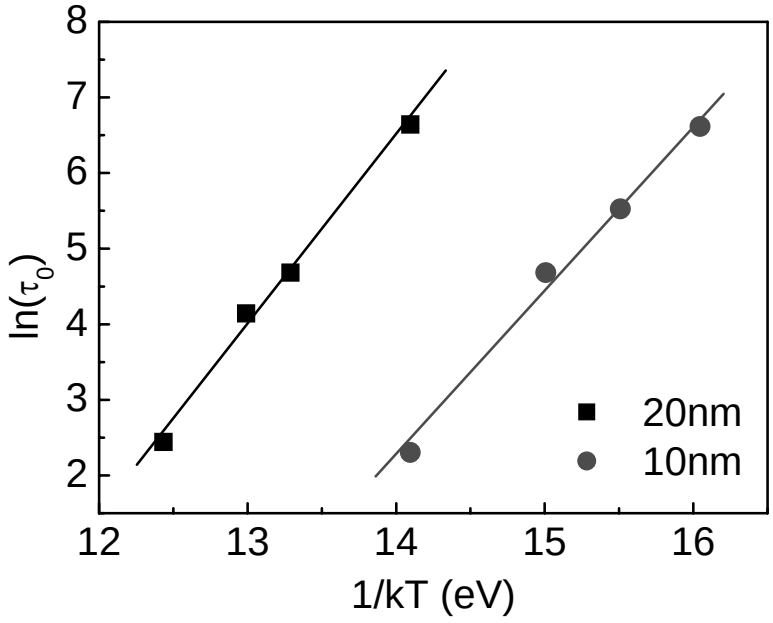

Figure 5.9. Arrhenius plots of degradation time for NiGe films with 10 nm and 20 nm as-deposited Ni. The degradation time is defined as corresponding to a 20% increase in sheet resistance.

5.5 Germanium Junction with NiGe Contacts

Finally, NiGe was applied on germanium junction as contacts. Figure 5.10(a) shows the current-voltage characteristic of n^+/p diode with NiGe contact. The diode without NiGe contact was also characterized as control sample. Dramatic on-current improvement (9X @V=-0.75 V) is observed on n^+/p diode. This significant increase of on-current attributes to the improved series resistance with NiGe contact. The total

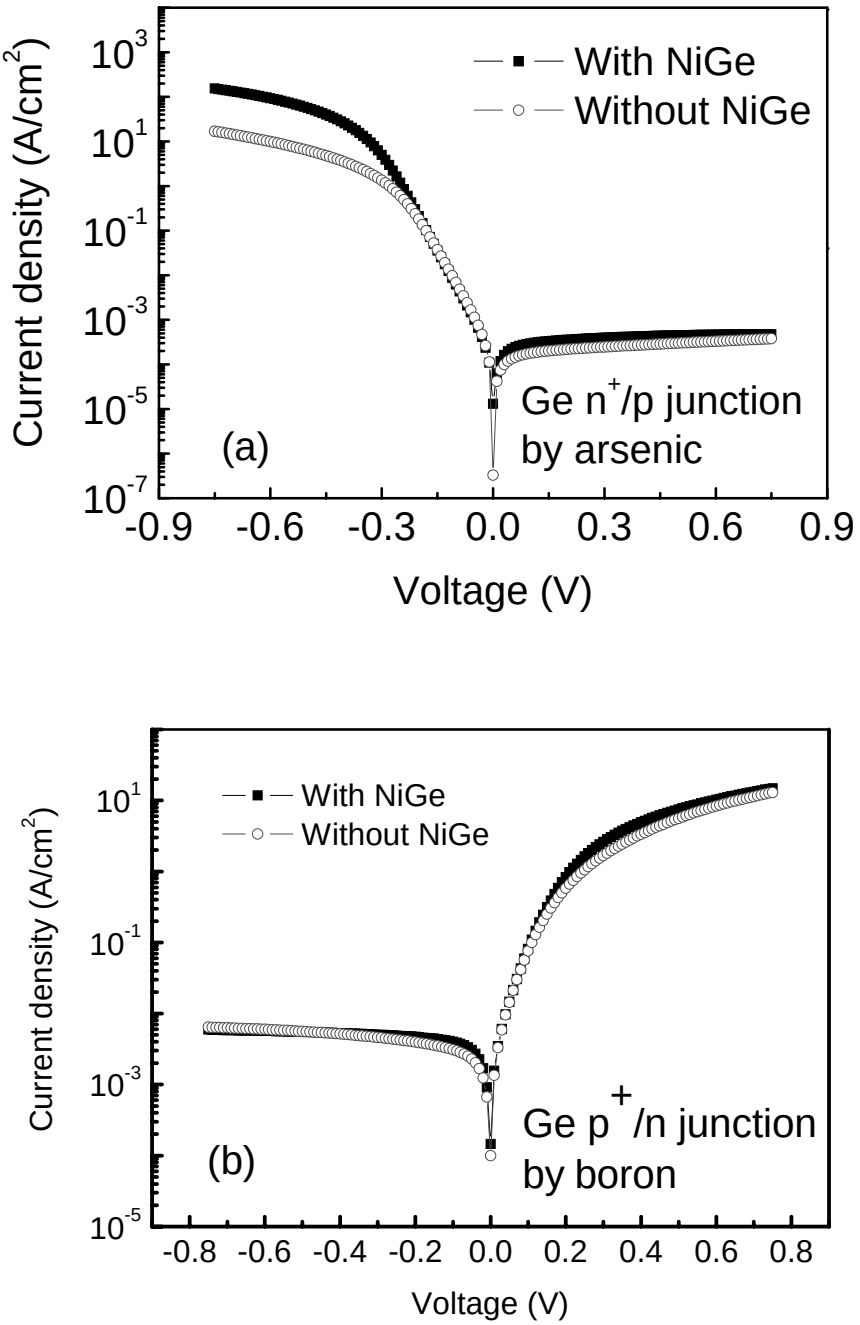

Figure 5.10. Current-voltage characteristics of germanium (a) n^+/p junction and (b) p^+/n junction with and without NiGe contact. The n^+/p junction was formed by arsenic ($1X10^{15}cm^{-2}$, 120 keV) and annealed at 600 ^oC for 2 mins. The p^+/n junction was formed by boron ($1X10^{15}cm^{-2}$, 35 keV) and annealed at 500 ^oC for 2 mins.The self-aligned NiGe contact was formed at 400 ^oC with 30 nm initial Ni.

series resistance of the junction reduces by 10.8 Ω from 14.7 Ω for the device without contact to 3.9 Ω with a NiGe contact. Good I-V characteristics are maintained and no degradation of reverse-bias leakage current is observed with implementation of NiGe contact.

Figure 5.10(b) shows the current-voltage characteristic of p^+/n diode with and without NiGe contact. Again, there is no leakage current degradation observed with NiGe contact. However, compared with n^+/p junction, the drive current enhancement with NiGe is much smaller on p^+/n junction. By extracting the total series resistance, it was found that with NiGe contact, a comparable amount of Rs reduction is recorded on p^+/n junction (from 52 Ω to 38 Ω). However, even with NiGe contact, the series resistance of p^+/n junction is still very high and limits the drive current. Therefore, there is only a slight drive current improvement with NiGe contact. The high series resistance could be attributed by a high resistance in n-type substrate used for p^+/n junction. The n-type Ge substrate has a much higher resistivity (1.2-1.1 Ωcm) than that of the p-type substrate (0.19 to 0.18 Ωcm) used for n^+/p junction due to lower substrate doping concentration. By using high doping concentration substrate or improved junction structure with well contact, it is believed that a significant drive current improvement will be observed on Ge p^+/n junction with NiGe contact.

5.6 Conclusion

The formation and thermal stability of nickel germanide on germanium substrate were systematically examined by various physical and electrical methods. The results show that nickel started to react with germanium at a low temperature of 250 ^oC and a Ni-rich germanium was produced at low temperature. A uniform stoichiometric mono nickel germanide was formed with a low resistivity of 14 μΩ-cm

after 400 ^{o}C annealing. The formation of NiGe was monitored by a spectroscopic ellipsometer. And the refractive index of NiGe was extracted successfully. With the knowledge of refractive index, the thickness of NiGe was measured. Nickel germanide showed a poor thermal stability due agglomeration after high temperature annealing. A low activation energy of agglomeration (2.2±0.2 eV) was estimated which accounted for the poor thermal stability of NiGe. The germanium diode with NiGe contact showed good I-V characteristics. The drive current of diode was much improved due to reduced series resistance while low leakage current was maintained.

References

[5.1] H. Shang, K.-L. Lee, P. Kozlowski, C. D. Emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, and W. Haensch, "Self-Aligned n-Channel Germanium MOSFETs With a Thin Ge Oxynitride Gate Dielectric and Tungsten Gate," *IEEE Electron Device Lett.*, v. 25, pp. 135, 2004.

[5.2] Huiling Shang, Harald Okorn-Schmidt, Kevin K. Chan, Matthew Copel, John A. Ott, P. M. Kozlowski, S. E. Steen, S. A. Cordes, H.-S. P. Wong, E. C. Jones and W. E. Haensch, "High Mobility p-channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric," *Tech. Dig. Int. Electron Devices Meet. 2002*, pp. 441, 2002.

[5.3] Chi On Chui, Hyoungsub Kim, David Chi, Baylor B. Triplett, Paul C. McIntyre, and Krishna C. Saraswat, "A Sub-400ºC Germanium MOSFET Technology with High-κ Dielectric and Metal Gate," *Tech. Dig. Int. Electron Devices Meet.* 2002, pp. 437, 2002.

[5.4] T. Morimoto, T. Ohguro, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, "Self-aligned nickel-mono-silicide technology for high-speed deep submicrometer logic CMOS ULSI," IEEE Tran. Electron Devices, vol.42, pp.915, 1995.

[5.5] S.P. Ashburn, M.C. Ozturk, J.J. Wortman, G. Harris, J. Honeycutt and D.M. Maher, "Formation of titanium and cobalt germanides on Si(100) using rapid thermal processing," J. Electron. Mater., vol.21, pp.81, 1992.

[5.6] M. Wittmer, M.-A. Nicolet and J. W. Mayer, "The first phase to nucleate in planar transition metal-germanium interfaces," Thin Solid Films, vol.42, pp.51, 1977.

[5.7] F. Nemouchi, D. Mangelinck, J.L.Labar, M. Putero, C. Bergman, and P.Gas, "A comparative study of nickel silicides and nickel germanides: Phase formation and kinetics", Microelectronics Engineering, vol.83, pp.2101, 2006.

[5.8] S.-L Hsu, C.-H Chien, M.-J Yang, R.-H Huang, C.-C Leu, and S.-W Shen, "Study of thermal stability of nickel monogermanide on single- and polycrystalline germanium substrates," Appl. Phys. Lett., vol.86, pp. 251906, 2005.

[5.9] E.G. Colgan, M. Maenpaa, M. Finetti and M.-A. Nicolet, "Electrical characteristics of thin Ni2Si, and NiSi2 layers grown on silicon," J. Electron. Mater., vol.12, pp.413, 1983.

[5.10] A. Nash, P. Nash, Bull: Alloy Phase Diagrams 8 (1987) 255.

[5.11] K.Y. Lee, S.L. Liew, S.J. Chua, D.Z. Chi, H.P. Sun, and X.Q. Pan, "Formation and Morphology Evolution of Nickel Germanides on Ge (100) under Rapid Thermal Annealing," Mat. Res. Soc. Symp. Proc., vol.810, pp.55, 2004.

[5.12] J.P. Gambino, E.G. Colgan, "Silicides and ohmic contacts," Mat. Chem. and Phys., vol.52, pp.99, 1998.

[5.13] J. Y. Spann, R. A. Anderson, T. J. Thornton, G. Harris, S. G. Thomas, C. Tracy, "Characterization of nickel Germanide thin films for use as contacts to p-channel Germanium MOSFETs," IEEE Electron Device Lett., vol. 26, pp. 151, 2005.

[5.14] C. Isheden, J. Seger, H. H. Radamson, S.-L Zhang and M.Östling, "Formation of Ni mono-germanosilicide on heavily B-doped epitaxial SiGe for ultra-shallow source/drain contacts," Mat. Res. Soc. Symp. Proc., vol.745, N 4.9.1, 2003.

[5.15] J. A. Dobrowolski, F. C. Ho, and A. Waldrof, "Determination of optical

constants of thin film coating materials based on inverse synthesis," Appl. Opt., vol. 22, pp. 3191–3200, 1983.

[5.16] O. Chamirian, J. A. Kittl, A. Lauwers, O. Richard, M. van Dal and K. Maex, "Thickness scaling issues of Ni silicide," Microelectron. Eng., vol.70, pp.201, 2003.

[5.17] E. G. Colgan, J. P. Gambino and B. Cunningham, "Nickel silicide thermal stability on polycrystalline and single crystalline silicon," Mater. Chem. Phys. B, vol.46, pp.209, 1996.

[5.18] K. Okubo, Y. Tsuchiya, O. Nakatsuka, A. Sakai, S. Zaima and Y. Yasuda, "Influence of Structural Variation of Ni Silicide Thin Films on Electrical Property for Contact Materials," Jpn. J. Appl. Phys., vol.43, pp. 1896, 2004.

[5.19] O. Hellman, "Topics in solid phase epitaxy: Strain, structure and geometry," Mater. Sci. Eng. R, vol.16, pp.1, 1996.

[5.20] Dieter K. Schroder, Semiconductor Material and Device Characterization, 2nd ed. (Wiley, New York, 1998), p200.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

As CMOS transistors scale beyond 45 nm technology node, ultra-thin equivalent oxide thickness less than 1 nm and enhanced effective saturation carrier velocity due to quasi-ballistic transport are required [6.1]. New material and innovative device structure are thus needed. Germanium MOSFET with high-κ gate dielectric provides a promising solution to continue improving the device performance. However, the replacement of channel material from Si to Ge induces various material and process integration issues. This work has attempted to investigate the electrical performance of Ge MOSFET to access its feasibility as alternative channel material.

Firstly, the preliminary results of Ge MOSFET with high-κ gate dielectric are shown in the Chapter 2. Ge pMOSFET with Hf oxynitride gate dielectric exhibits good I-V characteristics and high mobility which exceeds Si universal curve. The thermal stability of high-κ upon post deposition annealing is evaluated. The results suggest that the PDA temperature should not exceed 600 ^{o}C to prevent significant equivalent oxide thickness increase due to interfacial layer growth. Then, the thermal stability of high-κ upon source/drain activation annealing (post metal annealing) is studied with high-κ dielectric Al_2O_3 and NH_3 surface nitridation. The high temperature PMA induces three major thermal stability problems: (1) deterioration of

C-V curves, (2) positive shift of flatband voltage, and (3) the increase of gate leakage current. Ge out-diffusion from substrate into dielectric is believed to be the root cause of Ge device performance deterioration.

Germanium incorporation in high-κ gate dielectric on germanium substrate after high temperature process has been discovered to be determinant for the electrical performance of Ge devices. The Ge incorporation in high-κ gate dielectric (e.g. HfO_2) occurs by two mechanisms: Ge atoms out-diffusion from Ge substrate and airborne GeO transportation. The Ge incorporation by GeO transportation is related with Ge substrate oxidation. When oxygen is present, the germanium incorporates into HfO_2 in the form of oxide and, in turn, forms a new dielectric ($Hf_{1-x}Ge_xO_2$). Although $Hf_{1-x}Ge_xO_2$ has a similar dielectric constant with that of HfO_2, it has a high interface state density which degrades the MOSFET performance. Therefore, the thermal budget of Ge process must be tightly controlled to minimizing the Ge out-diffusion into high-κ gate dielectric.

Since the poor thermal stability of high-κ gate stack on germanium due to germanium out-diffusion, the high temperature source/drain activation annealing by RTA will inevitably degrade the electrical performance. As a solution, laser annealing was introduced as a superior source/drain activation technique. Smaller source/drain sheet resistance as well as shallower junction depth is realized by laser annealing than conventional rapid thermal annealing. Furthermore, laser annealing has been integrated into Ge MOSFET fabrication. By applying an aluminum laser reflector on the TaN metal gate electrode, S/D regions of MOSFET are selectively annealed without heating gate stack. Good gate stack integrity and small S/D series resistance are achieved simultaneously. With these benefits, a larger drive current, a lower threshold voltage and a higher electron mobility at high effective electrical field are achieved in Ge nMOSFET with laser annealing activation than that with RTA

activation. Ge pMOSFET with high mobility (1.9 times of Si universal curve) and low EOT (1.2 nm) is also demonstrated with laser annealing. This performance is very close to the ITRS requirements of high performance CMOS technology in the future (2.0 times mobility of Si and EOT less than 1 nm). With the scaling of the physical thickness of high-κ gate dielectric and optimization of source/drain, Ge MOSFET with high-κ is very promising to achieve the low EOT and high mobility target in ITRS.

At last, the self-aligned germanide is studied to further reduce the source/drain series resistance of Ge MOSFETs. The formation and thermal stability of nickel germanide on germanium substrate were systematically examined. Nickel starts to react with germanium and produces Ni-rich germanide at a low temperature of 250 ^{o}C. Stoichiometric mono-nickel germanide is formed with a low resistivity of 14 μΩ-cm after 400 ^{o}C annealing. The formation and agglomeration of nickel germanide could be monitored by spectrum ellipsometer. With the extracted optical model of NiGe, it is able to measure the thickness of thin NiGe film accurately. Nickel germanide shows a poor thermal stability due a low activation energy of agglomeration (2.2±0.2 eV). Improved drive current of Ge diode with NiGe contact is demonstrated without degrading leakage current.

6.2 Suggestions for future work

This thesis explored the potential of Ge MOSFET with high-κ gate dielectric as a candidate for highly scaled CMOS technology. High hole mobility has been demonstrated in Ge pMOSFET. However, poor electron mobility is extensively observed in Ge nMOSFET by this work and other research groups. The root cause of low electron mobility is not well elaborated. Generally, it is associated with Coulomb

scattering from the interface and fixed charge of high-κ gate dielectric. Similarly, silicon nMOSFETs suffer low electron mobility with high-κ gate dielectric while less mobility degradation has been observed on pMOSFETs. Recently, a improved interface state measurement method for Ge revealed that peaked and very high density ($1.4x10^{13}/cm^2$) interface states existed near the Ge conduction band and led to Fermi-level pinning [6.2]. It implied the absence of full inversion and explained the low mobility extracted in the nMOSFET devices. More evidences are necessary to confirm this hypothesis. With the clarification of the cause of low electron mobility of Ge nMOSFET, new material and process are to be developed to improve the Ge nMOSFET performance.

In the area of advance source/drain structure of Ge MOSFETs, the laser annealing source/drain activation has been demonstrated with superior performance compared with rapid thermal annealing. The application of this technique to ultra shallow source/drain extension (<10 nm) which is demanded by 45 nm and further technology nodes can be examined. This could be realized by ultra-low energy ion implantation or other novel doping technique such as plasma doping followed by laser annealing. The application of nickel germanide as contact to deep Ge junction has been described in the chapter 5. The detailed examination of performance of thin NiGe contact on ultra-shallow Ge junctions is needed. In addition, the contact resistivity of NiGe to p-type heavily doped germanium has been reported in [6.3] while it is unknown for n-type germanium. Besides, the possible improvement of thermal stability of NiGe by adding other element (e.g. Pt and Pd) will be desirable.

References

[6.1] International Technology Roadmap for Semiconductors (ITRS) 2004, Semiconductor Industry Assoc., San Jose, CA., Available: http://www.itrs.net/Common/2004Update/2004Update.htm

[6.2] Koen Martens, Brice De Jaeger, Renaud Bonzom, Jan Van Steenbergen, Marc Meuris, Guido Groeseneken, and Herman Maes, "New Interface State Density Extraction Method Applicable to Peaked and High-Density Distributions for Ge MOSFET Development," IEEE Electron Device Lett., vol. 27, pp. 405-407, 2006.

[6.3] JohnY. Spann, Robert A. Anderson, Trevor J. Thornton, Gari Harris, Shawn G. Thomas, and Clarence Tracy, "Characterization of Nickel Germanide Thin Films for Use as Contacts to p-Channel Germanium MOSFETs," IEEE Electron Device Lett., vol. 26, pp. 151-153, 2005.

Appendix A

List of publications:

Journal:

1. Qingchun Zhang, Chia Wai Han, Chunxiang Zhu, "Spectroscopic ellipsometry investigation of nickel germanide formation", Journal of the Electrochemical Society, v 154, n 4, p H314, 2007
2. Qingchun Zhang, Jidong Huang, Nan Wu, Guoxin Chen, Monghui Hong, L. K. Bera, and Chunxiang Zhu, "Drive current enhancement in Ge n-Channel MOSFET using laser annealing source/drain activation", IEEE Electron Device Lett., vol. 27, pp728, 2006.
3. Qingchun Zhang, Nan Wu, Doreen Mei Ying Lai, Yakovlev Nikolai, L. K. Bera and Chunxiang Zhu, "Germanium incorporation in HfO_2 dielectric on germanium substrate," Journal of The Electrochemical Society, vol.153, No.3, pp.207-210, 2006.
4. Qingchun Zhang, Nan Wu, Thomas Osipowicz, Lakshmi Kanta Bera and Chunxiang Zhu, "Formation and thermal stability of nickel germanide on germanium substrate," Jap. J. Appl. Phys., vol. 44, No. 45, pp.L1389-L1391, 2005.
5. Qingchun Zhang, Nan Wu, Chunxiang Zhu, "The electrical and material properties of HfO_xN_y dielectric on germanium substrate," Jap. J. Appl. Phys., vol.43, No.9, pp.L1208-L1210, 2004.

Conference:

1. Qingchun Zhang, Nan Wu, Chunxiang Zhu, L. K. Bera, "Germanium out-diffusion in HfO_2 and its impact on electrical properties," Solid State Device Meeting (SSDM), P1-14, 2005.
2. Qingchun Zhang, Nan Wu, L.K. Bera, and C. Zhu, "Study of germanium diffusion in HfO_2 gate dielectric of MOS device application," Mater. Res. Soc. Symp. (MRS), vol.829, B9.26, 2004.
3. Qingchun Zhang, Nan Wu, Chunxiang Zhu, Li, M.F., Chan, D. S. H., Chin, A., Kwong, D.L., Bera, L. K., Balasubramanian, N., Du, A.Y., Tung, C.H., Haitao Liu, and Sin, J.K.O., "Germanium pMOSFET with HfON gate dielectric," pp.256-257, International Semiconductor Device Research Symposium

(ISDRS), 2003.

Other Publication:

1. Nan Wu, Qingchun Zhang, Chunxiang Zhu, "Gate-first Germanium nMOSFET with CVD HfO_2 gate dielectric and silicon surface passivation," IEEE Electron Device Lett., vol.27, pp.479-481, 2006.
2. Jidong Huang, Nan Wu, Qingchun Zhang, Chunxiang Zhu, M.F. Li, Andrew A. O. Tay, Zhi-Yuan Cheng, Chris W. Leitz, Anthony Lochtefeld, "Surface NH_3 anneal on strained-$Si_{0.5}Ge_{0.5}$ for metal-oxide-semiconductor applications with HfO_2 as gate dielectric," Appl. Phys. Lett., vol.88, pp.143506-143508, 2006.
3. Jidong Huang, Nan Wu, Qingchun Zhang, Chunxiang Zhu, Andrew A. O. Tay, Guoxin Chen, Minghui Hong, "Germanium n^+/p junction formation by laser thermal process," Appl. Phys. Lett., vol.87, pp173507-173509, 2005.
4. Nan Wu, Qingchun Zhang, Chunxiang Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, D.-L. Kwong, "Alternative surface passivation on germanium for metal-oxide semiconductor applications with high-κ gate dielectric," Appl. Phys. Lett., vol.84, pp.4127-4129, 2004.
5. Nan Wu, Qingchun Zhang, Chunxiang Zhu, D. S. H. Chan, Anyan Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, D. –L. Kwong, "A TaN-HfO_2-Ge pMOSFET With novel SiH_4 surface passivation," IEEE Electron Device Lett., vol.25, pp.631-633, 2004.
6. Nan Wu, Qingchun Zhang, Chunxiang Zhu, Chia Ching Yeo, Sung Jin Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," Appl. Phys. Lett., vol.84, pp.3741-3743, 2004.
7. Nan Wu, Qingchun Zhang, Chunxiang Zhu, Chen Shen, M.F. Li, D. S. H. Chan, and N. Balasubramanian, "BTI and charge trapping in germanium p- and n-MOSFETs with CVD HfO_2 gate dielectric," IEEE Int'l Electron Device Meeting (IEDM) 2005, pp.563, 2005.
8. Yoke Ping Tan, Mang-Kin Lau James, Qingchun Zhang, Nan Wu, Chunxiang Zhu, "A Simulation Study of FIBL in Ge MOSFETs with High-κ Gate Dielectrics," IEEE Conference on Electron Devices and Solid-State Circuits, pp.111-112, 2005.
9. Nan Wu, Qingchun Zhang, Chunxiang Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Y. Du, Albert Chin, Johnny K. O. Sin, D.-L. Kwong, "A novel surface passivation process for HfO_2 Ge MOSFETs," Device Research Conference (DRC), II.A-4, Jun 2004.
10. Nan Wu, Qingchun Zhang, Chunxiang Zhu, M.F. Li, DSH Chan, Albert Chin, D.

L. Kwong, L.K.Bera , N. Balasubmanian, A.Y. Du, C.H. Tung, Haitao Liu, and Johnny K. O. Sin, "Ge pMOSFETs with MOCVD HfO_2 gate dielectric," International Semiconductor Device Research Symposium (ISDRS), pp.252-253, 2003.