ADVANCED GATE STACKS FOR NANO-SCALE CMOS TECHNOLOGY

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Summary

Rapid advances in CMOS technology have led to aggressive scaling of the MOSFET gate stack. Conventional poly-Si/SiO_2 gate stack is approaching some practical limits, and advanced gate stacks involving metal gate materials and high-*k* dielectrics may need to be introduced into IC industry as well as some novel process integration technologies. However, immense challenges arise in material engineering and process integration of the advanced gate stacks. This thesis attempts to address some of these challenges.

One of the most serious challenges for the advanced gate stacks is to find a way to tune the work function of metal gates to Si band edge for future CMOS applications. In **Chapter 3**, a gate dielectric material HfLaO was investigated systematically for the first time. By incorporating La into HfO_2 film, not only the crystallization temperature and *k* value of the dielectric film are increased substantially, also the effective work function (EWF) of TaN (HfN or TiN) can be effectively tuned from Si mid-gap to the conduction band edge of Si by optimizing the La composition in HfLaO to meet the n-MOSFET work function requirement. Simultaneously, the Si valence band edge EWF can be obtained by employing HfLaO and Pt (or Ru) even after a 1000^{o}C thermal treatment, which is very suitable for p-MOSFETs. Superior n-MOSFET characteristics have also been demonstrated using HfLaO dielectric compared to those with pure HfO_2, including an enhancement of ~70% for drive current and electron mobility and one order reduction of dielectric charge trapping induced V_{th} shift. Moreover, the reliability issue for HfLaO dielectric in terms of charge trapping induced V_{th} shift was further investigated comprehensively in **Chapter 5**. It is found that the V_{th} shifts, evaluated by either static (DC) or transient (pulsed I_d-V_g) measurement technique, are obviously suppressed with the incorporation of La into HfO_2. All these excellent properties observed in HfLaO gate dielectric suggest that it could be a very promising candidate as the alternative gate

dielectric for future CMOS application.

In addition, to interpret the significant EWF shift for both n- and p-type metal gates, a specific model based on the interfacial dipole theory between the gate electrode and the gate dielectric is also proposed in **Chapter 3**, wherein the effects of different electronegativities among materials involved in the gate stack and oxygen vacancy (V_O) density in the dielectric film on the EWF of metal gates are highlighted and it seems the effect caused by different electronegativities is more significant for n-type metal gates and the effect of V_O is more obvious for p-type noble metals. Experimentally, this model has been demonstrated by other gate stacks including more metal gates and lanthanide elements incorporated HfO_2 dielectrics. Therefore, this model regarding the metal-dielectric interface could be useful for work function tuning and interface engineering between metal gates and high-*k* dielectrics in future MOS devices.

Dual metal gate integration issues for advanced CMOS devices are also discussed in this thesis and two gate-first integration schemes for dual MG CMOS technology are proposed in **Chapter 4**. The first one involves novel gate stacks to create wide enough EWF tunability by using a high-temperature metal inter-diffusion technique. In this process, a HfLaO dielectric layer is employed to increase the tunable EWF range based on the results shown in **Chapter 3**. Furthermore, to avoid the gate dielectric from being exposed during the metal etching process, the original Ru capping layer is kept throughout the process flow. This addresses the etching damage issues associated with the conventional direct-etching integration scheme. More importantly, the EWF of the Ru layer can be modulated by a high-temperature metal inter-diffusion between Ru and upper TaN layer, and this diffusion process is compatible with the conventional gate-first CMOS process flow. By using this integration scheme, the EWF of these gate stacks has a wide EWF tunable range from 3.9 eV to 5.2 eV. These results make TaN/Ru (for n-MOSFETs) and Ru (for p-MOSFETs) on HfLaO gate stacks promising candidates for future CMOS

integration technology. The other novel integration scheme is proposed by positively utilizing unavoidable FLP effect in gate stacks involving high-*k* dielectrics and gate electrodes (poly-Si or metal gates). By incorporating La (or other lanthanide elements) and Al into selected MN_x (TaN, HfN or TiN), the EWF of MN_x clearly shifts to the conduction band edge and valence band edge of Si respectively, which is very suitable for bulk-Si CMOS technology. These proposed integration schemes may provide some useful discussions to address some of the major issues associated with the conventional integration schemes, and are believed to make a contribution to the development of the dual MG integration processes for future bulk-Si CMOS technology.

Overall, the results of all studies presented in this thesis may contribute to a good understanding of material properties, electrical characteristics and reliability in high-*k* gate dielectrics and metal gates for advanced CMOS application. Several approaches presented in this thesis can be used to effectively solve the major challenges for implementation of the advanced gate stacks.

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List of Abbreviations

AES	Auger electron spectroscopy
AFM	atomic force microscopy
ALCVD	atomic-layer chemical vapor deposition
ALD	atomic-layer deposition
ASIC	application-specific integrated circuit
BTBT	band-to-band tunneling
BTI	bias-temperature-instability
CES	constant-field scaling
CET	capacitance equivalent thickness
CMOS	complementary metal-oxide-semiconductor
CMP	chemical mechanical polishing
C-V	capacitance-voltage
CVD	chemical vapor deposition
CVS	constant-voltage scaling
DG	double-gate
DHF	dilute hydrofluoric
DRAM	dynamic random access memory
EDX	energy dispersive X-ray
EOT	equivalent oxide thickness

EWF	effective work function
FDSOI	fully depleted silicon-on-insulator
FGA	forming-gas annealing
FIBL	fringing-induced barrier lowering
FLP	Fermi-level pinning
FTIR	Fourier transform infrared
FUSI	fully-silicided (metal gate)
GIDL	gate-induced-drain leakage
HK	high-k (dielectric)
HP	high-performance
I/I	ion implantation
IC	integrated circuits
IL	interfacial layer
ITRS	International Technology Roadmap for Semiconductors
I-V	current-voltage
LDD	lightly-doped-drain
LSI	large-scale integration
MG	metal gate
MIGS	metal-induced gap state
MNx	(refractory) metal nitride
MOCVD	metal-organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field-effect transistor

MPU	microprocessor unit
MSI	medium-scale integration
OES	optical emission spectroscopy
PDA	post-deposition-annealing
PMA	post-metal-annealing
PR	photoresist
PVD	physical vapor deposition
RCS	remote Coulomb scattering
RMS	root mean square
RTA	rapid thermal annealing
S/D	source/drain
SC-1	standard cleaning-1 (NH4OH+H2O2+H2O) solution
SRAM	static random access memory
SS	sub-threshold swing
SSDOI	strained-Si directly on insulator
SSI	small-scale integration
SSOI	strained-Si on insulator
STI	shallow trench isolation
TEM	transmission electron microscope
UHV	ultra high vacuum
ULSI	ultra-large-scale integration
UTBSOI	ultra-thin-body silicon-on-insulator

UV	ultraviolet
VASP	Vienna Ab Initio Simulation Package
VLSI	very-large- scale integration
Vo	oxygen vacancy
WF	work function
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Chapter 1

Introduction

1.1 Overview of MOSFET Scaling

It has been around fifty years since the invention of the integrated circuit (IC) technology (1958), and during this period, there has been an unprecedented growth of the semiconductor industry, wherein the most prominent growth area lies in the silicon-based IC technology, which has evolved from small-scale integration (SSI), to medium-scale integration (MSI), to large-scale integration (LSI), to very-large- scale integration (VLSI), and finally to ultra-large-scale integration (ULSI). Currently, the ULSI technology has infiltrated practically every aspect of our daily life, making an enormous impact on the way we work and live.

To start, metal-oxide-semiconductor field-effect transistor (MOSFET, first invented by Dawon Kahng and Martin Atalla in 1960) is definitely the most important and basic IC device due to its advantages in device miniaturization, low power dissipation, and high yield compared to all other semiconductor devices. Moreover, it also serves as a basic component for many key device building blocks, including the complementary metal-oxide-semiconductor (CMOS), the dynamic random access memory (DRAM), and the static random access memory (SRAM) [1]. Therefore, the history of IC development is almost in tandem with that of MOSFET development, and the sustained growth in IC technology is actually driven by the continuous scaling of MOSFET to ever smaller dimensions.

The primary motivation for continuous scaling of MOSFET is to increase the number of transistors per chip, which may reduce cost effectively. For much of the history of semiconductor industry, the behavior of scaling of MOSFET has followed

the well-known Moore's law, which predicts that the number of transistors per chip would double every ~18 months [2]. At this rate, the number of transistors per chip has been increasing from 10^3 in the year 1972 to more than 10^9 of today's leading-edge technology, as shown in **Fig. 1.1** [3]. In the meantime, cost per function has decreased at an average rate of ~ 25-30% per year per function [4], implying similar price reductions are expected for logic ICs.

Additional benefits from device scaling down include improvement of device speed and reduction of power consumption. Higher speeds lead to expanded IC functional throughput rates, so that future ICs can perform data processing, numerical computation, and signal conditioning at 100 and higher gigabit-per-second rates [5]. Reduced power consumption will result in lowering the energy required for each switching operation. The required energy, called the power-delay product, has decreased by six orders of magnitude since 1960 [6].

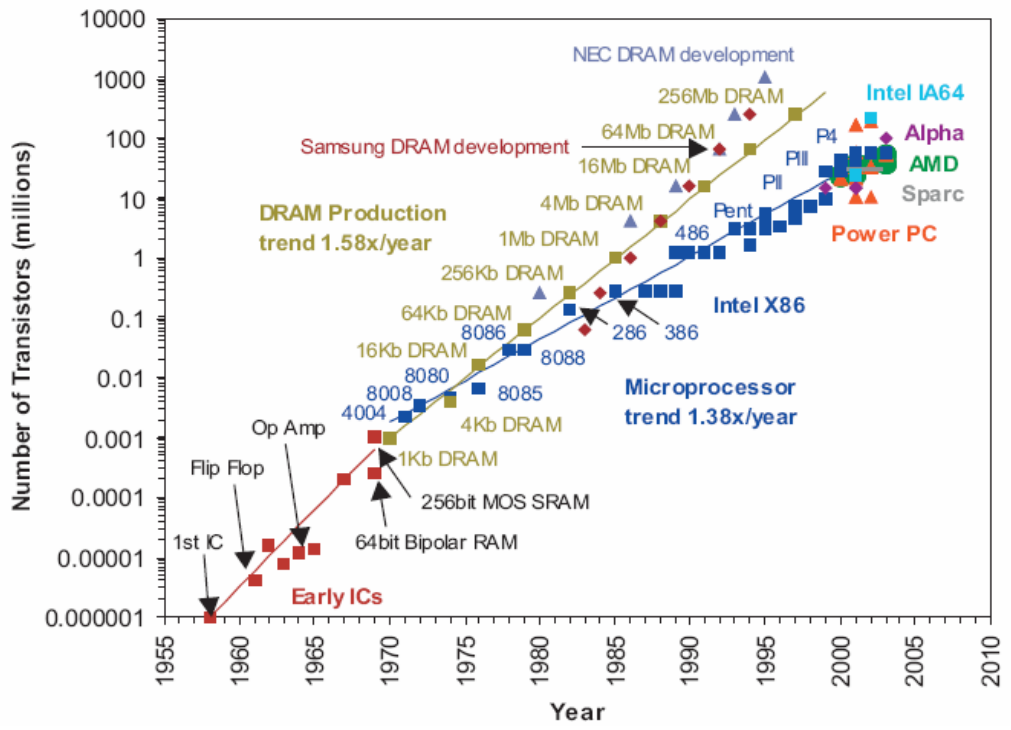

Fig. 1.1: The increasing trend of transistors' production in a Microprocessor and DRAM during the last several decades based on the information from some famous corporations, showing the device scaling basically following Moore's Law.

1.2 Approaches for MOSFET Scaling

To scale down the device size continuously while maintaining device function, there have been various proposed sets of scaling rules, such as constant-field scaling (*CES*), constant-voltage scaling (*CVS*), and the generalized scaling rules [7-9].

In *CES*, it was proposed to keep the electric field unchanged in a short-channel device in order to maintain comparable characteristics and reliability relative to a long channel device. The idea behind *CES* is to scale the device voltages and the device dimensions (both vertical and lateral) by the same factor, so that the electric field remains unchanged. However, the requirement to reduce the supply voltage by the same factor as the physical dimension reduction in *CES* is difficult to meet since the threshold voltage (V_{th}) and sub-threshold slope are not easily controlled for scaling [10]. If the V_{th} scales down slower than other factors, the drive current will be reduced. Thus, a *CVS* rule was proposed to address this issue, where the voltages remain unchanged while device dimensions are scaled. However, *CVS* will result in an extremely high electric field, which causes unacceptable leakage current, power consumption, and dielectric breakdown as well as hot-carrier effects [10]. To avoid the extreme cases of *CES* and *CVS*, a generalized scaling approach has been developed, where the electric field is scaled by a factor of κ while the device dimensions are scaled by a factor of α [8]. The scaling parameters for *CES*, *CVS* and generalized scaling schemes are summarized in **Table 1.1**. In reality, the CMOS technology evolution has followed mixed steps of *CES*, *CVS*, and other generalized scaling schemes.

1.3 Challenges during MOSFET Scaling

MOSFET scaling is governed by the duality of speed versus power, where transistor speed, which is dependent upon drive current (I_d), should be increased while

decreasing transistor power consumption (*P*), while the transistor power consumption is determined by the total transistor leakage current.

Based on **Table 1.1**, it is necessary to increase the dimensional scaling factor (α) for enhancing speed, or reducing delay time (τ) in a circuit. That means gate oxide thickness (T_{ox}), gate length (L_g), gate width (W) and source/drain junction depth (X_j) for a MOSFET device must be scaled down significantly at the same time. Subsequently, as the technology scales down to the ultra deep-submicron, there are a lot of challenges facing the CMOS fabrication in the semiconductor industry.

Table 1.1: The scaling parameters for *CES, CVS* and generalized scaling schemes

MOSFET Device and Circuit parameters	Multiplicative Factor for MOSFETs		
	CES	*CVS*	Generalized
Device Dimensions (T_{ox}, L_g, W, X_j)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Voltage (V)	$1/\alpha$	1	κ/α
Electric Field (E)	1	α	κ
Capacitance ($C = \varepsilon A/t$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Inversion Layer Charge Density (Q_i)	1	α	κ
Circuit Delay Time ($\tau \sim CV/I$)	$1/\alpha$	$1/\alpha^2$	$1/\kappa\alpha$
Power per Circuit ($P \sim VI$)	$1/\alpha^2$	α	κ^3/α^2
Power-Delay Product per Circuit ($P\tau$)	$1/\alpha^3$	$1/\alpha$	κ^2/α^3
Circuit Density ($\propto 1/A$)	α^2	α^2	α^2
Power Density (P/A)	1	α^3	κ^3

(α: Dimensional Scaling Factor; κ: Voltage Scaling Factor)

One of the most fundamental challenges for scaling down MOSFET structures has been photolithography, so much so that each of the new generation is described by a new lithographic dimension [4]. Previously it was believed that optical lithography would eventually reach its limit [11,12], yet International Technology Roadmap for Semiconductor (*ITRS*) [4] suggested that 193-nm deep ultraviolet (UV)

optical lithography is available to produce 0.1-μm devices. When the limit for optical lithography is to be surpassed, X-ray and e-beam may be introduced into CMOS manufacturing. Therefore, for the present and near future, it appears unlikely that lithography will limit the scaling of silicon devices. However, the cost of lithography tools, including those required for making masks, may impede future scaling of devices to some extent. It seems more likely that a fundamental limit will halt further scaling. This will occur when at least one of the device physical dimensions, gate oxide thickness (T_{ox}), gate length (L_g), gate width (W), or junction depth (X_j), approaches the dimensions of a few silicon atoms. However, manufacturing tolerances, and therefore economics, may dictate an end to the scaling of silicon devices before these fundamental limits are reached. Therefore, in this part, only some currently perceived fundamental challenges will be considered.

1.3.1 High Leakage Currents

First of all, an important challenge is high leakage current caused by aggressive MOSFET scaling, which is becoming the most serious issue in the ultra deep-submicron CMOS technology due to the large power consumption of the devices. Therefore, these high leakages are very likely to be the show-stopper for the MOSFET scaling eventually. There are six sources of leakage currents in short channel MOSFETs, as shown in the **Fig. 1.2** [13], where I_1 is the oxide tunneling current; I_2 is the gate current due to hot carrier injection; I_3 is the subthreshold leakage; I_4 is the channel punchthrough current; I_5 is the reverse bias pn junction leakage and I_6 is the Gate Induced Drain Leakage (GIDL).

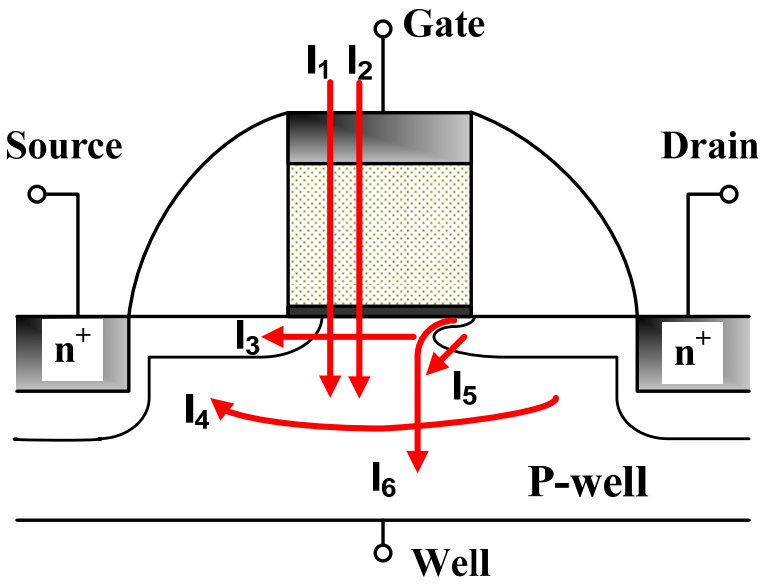

Fig. 1.2: Schematic illustration of leakage current paths in a MOSFET device, where I_1 is the oxide tunneling current; I_2 is the gate current due to hot carrier injection; I_3 is the subthreshold leakage; I_4 is the channel punchthrough current; I_5 is the reverse bias pn junction leakage and I_6 is the GIDL.

In short, the main reason for these high leakage currents in a MOSFET device is due to the decreasing distance between the four terminals (gate, source, drain and substrate) in both vertical and lateral directions, i.e. the scaling of gate oxide thickness (T_{ox}) and gate length (L_g). In addition, it has been shown for current thin gate oxide structures, the gate oxide tunneling current (I_1) is dominant among these leakages [14,15].

SiO_2, as a conventional gate oxide, has enabled the vertical scaling of Si-based MOSFET for several decades due to its outstanding dielectric properties. However, the gate oxide thickness of MOSFET has been scaled from 1000 Å of the first MOSFET to around 12 Å (65 nm technology node) of today's leading-edge technology. Moreover, it has been demonstrated that when the physical thickness of SiO_2 becomes thinner than ~30 Å, the gate leakage current will be dominated by direct tunneling through the dielectric, and the gate leakage current through the film increases exponentially with further decrease of SiO_2 thickness according to the fundamental quantum mechanical rules [16]. This will pose serious concerns

regarding the operation of CMOS devices, especially with respect to power consumption. Therefore, silicon oxynitride (SiON) and nitride/oxide stack (Si_xN_y/SiO_2) structure as the near-term gate dielectric alternatives have been proposed to address the high leakage and other concerns for ultra thin SiO_2 [4]. However, the thickness scaling limits for SiON (Si_xN_y/SiO_2) would be around 13 Å [17].

Consequently, the aggressive shrinking of gate dielectric thickness is driving the conventional SiO_2 or SiON gate dielectrics to its physical limit so alternative gate dielectric candidates have to be found for future CMOS application to meet the *ITRS* specifications.

1.3.2 Gate Electrode Issues

The aggressive scaling down of MOSFET device dimension (including L_g, W and T_{ox}) will also aggravate several problems for conventional gate electrode, polysilicon (poly-Si), such as poly-Si gate depletion, high sheet resistance and boron penetration from the p^+-doped poly-Si gate into the channel region [4].

Poly-Si depletion occurs due to insufficient active dopant density in the gate [18]. It can compromise device performance because it donates an additional thickness of about 4 Å to the capacitance equivalent thickness (CET) of the gate stack [19,20]. It reduces the gate capacitance in the inversion regime and hence the inversion charge density, or leads to a lower effective gate voltage to the substrate. This problem is especially serious when the gate oxide scales to sub-10 Å regime.

Theoretically, we can reduce the high sheet resistance of poly-Si gate by increasing the active dopant density in the poly-Si gate. However, it has been demonstrated that the active poly-Si dopant density will saturate due to the limitation of solid solubility for both n^+-doped and p^+-doped poly-Si [18]. Moreover, for p^+-doped poly-Si, the increasing doping concentration will aggravate boron penetration phenomenon. The penetration of boron into gate dielectrics is another

critical issue for conventional MOSFET with poly-Si gate electrode [21,22], and it becomes more serious as the thickness of gate oxide layer is below 20 Å.

Hence, to suppress these issues for poly-Si induced by the scaling of gate length and gate oxide thickness, it is necessary to look for a new approach.

1.3.3 Mobility Degradation

Carrier mobility (μ) in a MOSFET channel, which is a critical parameter for determining a number of transistor metrics, such as saturation current (I_{dsat}), speed ($1/\tau$), threshold voltage (V_{th}), transconductance (G_m), sub-threshold swing (SS) and the corresponding MOSFET performances, is significantly degraded with the continuous scaling down of gate oxide thickness and the increase of poly-Si doping concentration [23].

Generally, there are three scattering mechanisms to determine the inversion carrier mobility. They are namely, the Coulomb charge scattering, the phonon scattering, and the surface roughness scattering [24], where Coulomb scattering may originate from different scattering centers. Coulomb scattering centers was traditionally known to be due to the substrate impurities. However, remote Coulomb scattering (RCS) has been identified to play an important role for the mobility degradation phenomena in MOSFET with thin gate oxide layer [23]. Those remote scattering centers are away from the inversion layer, and may result from the presence of ionized charges in the gate dielectric and in the depleted poly-Si gate electrodes. In addition, it has been deduced that mobility degradation may be the main limitation in gate oxide scaling down to the 9 Å regime [23]. Therefore, the problem of carrier mobility degradation is necessary to be solved for maintaining the MOSFET performance in device scaling [25].

1.4 Opportunities during MOSFET Scaling

As predicted by *ITRS* [4], MOSFET scaling will continue further despite the challenges mentioned above. However, in order to achieve the maximum performance gain from the continuous MOSFET scaling while maintaining the power consumption at an acceptable level, innovative device structures and new materials have to be explored extensively. Therefore, CMOS technology is facing exciting opportunities now.

1.4.1 Innovations in Device Structure

As discussed above, the channel length is reduced aggressively with the continuous scaling down of MOSFET dimension, and MOSFETs with short channels differ in many important aspects from those with long channels, such as (a) short-channel effect, (b) velocity saturation, (c) channel length modulation, (d) source/drain series resistance, and (e) MOSFET breakdown. All these features are very important for device performance and design consideration [10]. In order to manage these features caused by the reduced channel length, many novel device structures have been proposed and investigated, including ultra-thin-body silicon-on-insulator (UTBSOI), double-gate (DG), FinFET, triple-gate, Ω-gate FET, nanowire FET and so on [26-33]. In these device structures, the potential coupling from gate to channel can be greatly improved by their special device geometry compared with conventional planar bulk-Si CMOS, so that the short-channel characteristics can be effectively controlled. Consequently, the intrinsic silicon can be adopted as the channel substrate, which enables lower channel electric field, lower Band-To-Band Tunneling leakage (BTBT, I_5 in **Fig. 1.2** due to heavily doped shallow junctions and halo doping), sharper *SS* and better carrier mobility to be achievable. These advantages make them very attractive as potential technology options for the future high-performance applications.

However, there are still some challenges for these novel device structures for comprehensive application. One of them is threshold voltage (V_{th}) moderating. Due to the small amount of depletion charges and the intrinsic Si channel used, the gate work function close to mid-gap of Si for these devices would be preferred [4]. Thus, conventional poly-Si gate can not work properly in this situation and novel gate electrode materials with mid-gap work functions are required [34]. Secondly, the high source/drain series resistance caused by the thin silicon body used in these 3-D structures is another concern which may affect the overall performance of these novel FETs, as discussed in the previous paragraph. Thirdly, the carrier transport characteristics in the ultra-thin Si channels will be very sensitive to the Si-body thickness [35-37]. Thus the body thickness must be strictly controlled to an acceptable range during processes. However, the manufacturing tolerance for body thickness would be added up with the tolerance in defining the gate length, resulting in even smaller process windows and higher manufacturing cost in fabricating these novel structures compared with the conventional planar devices. Therefore, these novel structures may only be used for some kernel parts in particular applications, such as, microprocessor unit (MPU) or application-specific integrated circuit (ASIC).

1.4.2 Innovations of Materials in MOS Structure

1.4.2.1 For Channel Material

As discussed in the section 1.3.3, carrier mobility is significantly degraded with the continuous scaling down of gate oxide thickness and channel length in a MOSFET device. Therefore, there is a need to improve carrier mobility in the channel region to obtain overall performance enhancement. Basically there are three ways to enhance mobility for MOSFET device, including (a) inducing strain to the channel region, (b) utilizing the high mobility surface orientation, and (c) employing new channel materials with high mobility and high saturation velocity.

In the first method, currently there are two groups of technologies to introduce strain into the channel of MOSFET. One group is global-strain technologies, in which the strain is induced from modified substrates other than conventional pure Si substrate, such as strained-Si on relaxed-SiGe, strained-Si on insulator (SSOI), strained-Si directly on insulator (SSDOI), and so on [38-41]. However, optimizing the n-MOSFET and p-MOSFET simultaneously in a CMOS would be an issue for this global-strain technique due to the different requirements of stress for electron and hole mobility enhancement. Moreover, the cost issue may be another concern because the required strained-Si substrates with very low defect level are very expensive. The other group is the local strain, namely process induced strain technologies, including the strain from shallow trench isolation (STI), Si_3N_4 stress liners, silicide induced strain, and embedded SiGe or SiC stressors in the source-drain region [42-47]. These techniques are based on the conventional bulk-Si CMOS process and thus have the advantages like low-cost and easy integration. Some of these techniques have already been adopted in the latest 65 nm CMOS technology for mass production.

The surface orientation and channel direction (current flow direction) can also affect the carrier mobility in MOSFET. In conventional bulk-Si CMOS technology, Si with uniform (100) surface orientation is commonly used. Recently it has been demonstrated (100) and (110) surface orientation can be integrated on the same wafer by a novel technology to get ideal mobility for electron and hole, respectively [48].

In addition, SiGe, Ge, InP, GaAs and other III-V compound semiconductors, as the possible candidates for channel materials, have attracted considerable attention due to their high-mobility and high-saturation-velocity [49-51]. However, compared with Si, the physical properties of these materials are still not very well understood. Many process issues also need to be addressed, including the dielectric/channel interface engineering and the source-drain junction formation [52]. Moreover, integration of alternative semiconductors into the conventional Si-based CMOS

process flow would be another concern. More comprehensive study on these materials will be appreciated in the future.

1.4.2.2 For Gate Oxide

As discussed in the section 1.3.1, the aggressive shrinking of gate oxide thickness is driving the conventional SiO_2 or SiON to its physical limit. In addition, the exponential increase in oxide tunneling leakage through gate oxide also causes significant concerns regarding to the operation of CMOS devices, particularly standby power consumption, reliability and lifetime. Currently, high-permittivity (*k*) dielectrics are regarded as potential candidates to replace SiO_2 or SiON for further scaling of the gate stack in MOSFET [53]. The most important advantage of the high-*k* gate dielectrics rather than SiO_2 or SiON is to provide a physically thicker film for leakage current reduction while improving the gate capacitance by higher permittivity, as described in **Equation 1-1**,

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{high-k,phy} \qquad (1\text{-}1)$$

where *EOT* is the equivalent oxide thickness of high-*k* dielectric, ε_{SiO2} and $\varepsilon_{high\text{-}k}$ are the permittivity of SiO_2 (3.9) and the high-*k* dielectrics, respectively, and $T_{\text{high-}k,\text{phy}}$ is the physical thickness of high-*k* film. Thus, a high-*k* dielectric with a relative permittivity of ~20 affords a physical thickness of 50 Å to obtain *EOT* of 10 Å. However, the relative permittivity, or *k* value, is not the only criterion for selecting an alternative gate dielectric because other material properties can also contribute to the final MOSFET performance, such as band gap, barrier height, film morphology, reliability and so on [53]. The detailed selection guidelines and research status for high-*k* dielectrics will be introduced in **Chapter 2**.

1.4.2.3 For Gate Electrode

As discussed in the section 1.3.2, as the gate oxide thickness of MOSFET scales into sub-10 Å regime, some fundamental limits of conventional poly-Si become more and more serious and tend to retard the improvements made to CMOS devices. Metal gate electrodes can be used to eliminate the poly-Si depletion effect and hence improve the device performance. Meanwhile, they can also address other concerns associated with the poly-Si gate electrodes. These make the metal gate technology one of the hottest research areas in recent years. However, there are still a lot of issues in the material selection and process integration need to be thought out before employing this kind of new materials. The detailed backgrounds and current research status about metal gate technology will also be discussed in **Chapter 2**.

1.5 Summary

As discussed above, currently CMOS scaling will no longer be driven by photolithography solely. In fact, it will be driven by the innovations in developing advanced structures/materials and the ability to integrate these novel materials and structures into CMOS fabrication processes. This brings immense challenges and great opportunities at the same time. As required by the semiconductor industry to keep step with Moore's law in the future ten years [4], metal gate and high-*k* technologies are among the most urgent technologies. Therefore, new materials and process schemes associated with advanced gate stacks involving metal gates and high-*k* dielectrics will be the main focus of this thesis.

The background, selection guidelines and recent research developments of the metal gate and high-*k* technologies will be introduced in detail in **Chapter 2**, wherein the major issues and challenges will be highlighted. Following the different challenges and the efforts to address these problems, the subsequent contents in this thesis will be divided into four parts. In **Chapter 3**, physical and electrical

characteristics for lanthanide incorporated HfO_2 gate dielectrics, especially HfLaO, will be investigated systematically. After that, an integration scheme for dual metal gate CMOS technology by employing HfLaO dielectric and specific metal gates will be presented at the beginning of **Chapter 4**, followed by a proposal for dual metal gate integration using a comparable method with conventional CMOS technology. A comprehensive investigation of bias-temperature-instability (BTI) degradation under both static and dynamic stresses for n- and p-MOSFETs with HfO_2 gate dielectric will be presented at the beginning of **Chapter 5**, then the evaluation of reliability for TaN/HfLaO gate stack will be performed as compared with TaN/HfO_2 gate stack. Finally, the major results achieved in this thesis will be summarized in **Chapter 6**, as well as some suggestions on future research work, such as the effect of Si deposition process on physical and electrical characteristics for Ni-based fully silicided (FUSI)/HfO_2 (and HfLaO) gate stacks.

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Chapter 2

Developments in Advanced Gate Stacks Involving High-*k* Dielectrics and Metal Gates

2.1 High-*k* Gate Dielectrics

2.1.1 Scaling Limits for Conventional Gate Dielectrics

As briefly discussed in **Chapter 1**, SiO_2 has always been used in conventional CMOS technology for the past several decades due to its excellent material and electrical properties as a gate dielectric. Generally, the amorphous, thermally grown SiO_2 as the gate dielectric offers several key advantages in CMOS processing. First, it can provide a stable (thermodynamically and electrically), high-quality interface as well as superior electrical isolation properties. Moreover, high breakdown fields of 15 MV/cm can be obtained in SiO_2. In addition, minimal low-frequency *C-V* hysteresis and frequency dispersion (< 10 mV), minimal dielectric charging and interface degradation, and the sufficiently high carrier mobility (both electrons and holes) can be usually obtained for the MOSFET with SiO_2/Si system [1].

Despite this remarkable contribution of SiO_2, further scaling of the SiO_2 thickness (< 3 nm) is problematic in advanced CMOS technology. The major concerns are the exponential increase in gate leakage current under the required operating voltages, which would lead to heat dissipation, power consumption and degradation of input impedance. The CMOS devices suffer from standby power dissipation [2,3], as well as boron penetration from poly-Si gate [4], and reliability issues [5-7].

To address these concerns, silicon oxynitride (SiON) and silicon nitride/oxide stack (Si_xN_y/SiO_2) structures as the near-term gate dielectric alternatives have been proposed, mainly due to a slightly higher permittivity (*k*) for pure Si_3N_4 (~7.8) than SiO_2 (3.9) [8-10]. However, the concentration of N through the dielectric layer must be controlled exactly because a small amount of N at or near the Si channel interface can control channel hot-electron degradation effects [11], while large amount of N near this interface will degrade device performance [12]. Till now, improved electrical properties have been obtained by using Si_xN_y/SiO_2 gate stack and a leakage current of ~10^{-3} A/cm^2 at 1.0 V bias with equivalent oxide thickness (*EOT*) thinner than 17 Å was achieved, which is ~100 times lower than that for a pure SiO_2 layer at the same *EOT* [13]. However, scaling with the SiON and Si_xN_y/SiO_2 appears to be limited to *EOT* ~ 13 Å, below which the effects of high gate leakage, reliability issue or electron channel mobility degradation will most likely prevent further improvements in device performance [14]. On the other hand, it has been suggested that 7 Å is the physical thickness limit for SiO_2 or SiON, because the SiO_x sub-oxide region at any oxide/Si interface is ~3.5 Å thick and there are two oxide/Si interfaces at the channel and the gate electrode. According to the most recent International Technology Roadmap of Semiconductor (*ITRS*), the current gate dielectrics (SiO_2 or SiON) may only represent current two years near-term solutions for scaling the CMOS transistors [1], as shown in **Table 2.1**.

Table 2.1: The scaling of dielectric thickness with year predicted in *ITRS* 2005 [1]

Year of Production	***2004***	***2007***	***2010***	***2013***	***2016***
Technology node	hp90	hp65	hp45	hp32	hp22
Physical gate length for MPU (nm)	37	25	18	13	9
Physical gate length for low-operating-power (nm)	53	32	22	16	11

Physical gate length for low-standby-power (nm)	65	37	25	18	13
EOT for MPU (nm)	1.2	0.9	0.7	0.6	0.5
EOT for low-operating-power (nm)	1.5	1.2	0.9	0.8	0.7
EOT for low-standby-power (nm)	2.1	1.6	1.3	1.1	1
Gate leakage at 100^{o}C for high performance (A/cm^2)	460	920	1,833	7,692	18,556
Gate leakage at 100^{o}C for low-operating-power (A/cm^2)	1.9	5.2	10.6	20.8	90.9
Gate leakage at 100^{o}C for low-standby-power (A/cm^2)	0.0046	0.0216	0.08	0.15	0.254

Consequently, the aggressive shrinking of gate dielectric thickness is driving the conventional SiO_2 or SiON gate dielectrics to its physical limit and further scaling of gate dielectrics requires other materials with higher permittivities (*k* values) based on **Equation 1-1**.

2.1.2 Selection Guidelines for High-*k* Gate Dielectrics

As an alternative to SiO_2 or SiON gate dielectric, high-*k* materials provide a substantial physically thicker dielectric layer for reduced leakage current and improved gate capacitance. According to *ITRS* 2005, the high-*k* gate dielectric will be required around 2008 [1]. Therefore, the timely implementation of high-*k* gate dielectric is an imperative task for maintaining the historical trend of device scaling in semiconductor industry. However, before that, all of the alternative high-*k* materials must meet a set of criteria, in addition to its *k* value, to serve as a successful gate dielectric. In this section, a systematic consideration of the selection guidelines for the appropriate high-*k* materials will be discussed.

2.1.2.1 Permittivity, Barrier Height and Band Gap

Theoretically, selection of a gate dielectric with a higher permittivity than that of SiO_2 is essential. However, in real fabrication processes, it cannot be assumed that the higher *k* value, the better the performance improvement.

The required *k* value must be balanced with the barrier height for both electrons and holes (ΔE_C and ΔE_V) to Si, especially ΔE_C value, in the tunneling regime because the gate leakage current will increase exponentially with the decrease of barrier height for electron direct tunneling transport [15]. Since the ΔE_C and ΔE_V of many potential gate dielectrics have not been reported, the closest, most readily attainable indicator of band offset is the band gap (E_G) of the dielectric. Generally, a large E_G corresponds to a large ΔE_C. Therefore, the E_G of the dielectric should be balanced against its *k* value. The *k* value generally increases with increasing atomic number for a given cation in a metal oxide. However, the E_G of the metal oxides tends to decrease with increasing atomic number [16]. **Table 2.2** summarizes relevant properties for various gate dielectric materials. As shown, the E_G tends to decrease with increasing *k* value. This is the first reason why *k* value for a dielectric candidate cannot be too high.

Table 2.2: Comparison of relevant properties on Si for various gate dielectric materials [11,16-19]

Dielectric Material	Dielectric constant (*k* value)	Gap energy (E_G: eV)	Electron barrier to Si (ΔE_C: eV)
SiO_2	3.9	9	3.2
Si_3N_4	7-7.5	4.5-5.3	2.4
Al_2O_3	9-9.5	8.8	2.8
Y_2O_3	15	6	2.3
ZrO_2	22-25	4-5.8	1.5

HfO_2	20-25	4.5-5.8	1.4
Ta_2O_5	22-25	4.4-5	0.35
La_2O_3	30	6	2.3
TiO_2	80	3-3.5	0

In addition, it has also been reported that the dielectric materials with ultra-high *k* value may cause fringing-induced barrier lowering (FIBL) effect [20], which means that a significant fringing field at the edge of a high-*k* dielectric could lower the barrier for carriers transport into the drain, and hence seriously degrade the off-state characteristics of the device.

Therefore, it is more appropriate to find a dielectric with moderate *k* value for advanced CMOS gate dielectric application. With this in mind, a single high-*k* dielectric layer, even with *k* value ~ 12–25, will allow a physical dielectric thickness of 35–50 Å, which is already thick enough to obtain the *EOT* required for 65 nm CMOS and beyond.

2.1.2.2 Thermodynamic Stability on Si and Film Morphology

As gate oxides must sit directly on the Si substrate, thus the second requirement arises from the condition that the oxides must not react with Si to form either SiO_2 or a silicide during deposition or subsequent processing at elevated temperatures, such as source/drain activation annealing. This is because the resulting SiO_2 layer would increase the overall *EOT* and compromise the effect of using the high-*k* dielectric. In addition, any formed silicide would generally be metallic and would short out the field effect. However, most of the high-*k* materials investigated would react with the Si substrate during high thermal budget process due to their thermodynamic instability, forming an undesirable interfacial layer. Moreover, the thickness of this interfacial layer will normally increase with the temperature of the process, which results in increased *EOT* eventually.

In addition to good thermodynamic stability on Si, alternative high-*k* dielectrics should also have good kinetic stability for themselves, i.e. they must withstand the high thermal budget processing. Most of the advanced gate dielectrics are either polycrystalline or single crystal films, but generally, those which can retain the amorphous structure throughout the subsequent processes are desirable because the polycrystalline structure for gate dielectrics would lead to undesirable interfacial growth, electrical instability and defect generation due to grain boundaries through the polycrystalline high-*k* layer, which may serve as high-diffusion paths for oxygen and dopant [21]. In addition, grain size and orientation changes throughout the polycrystalline dielectric layer could cause significant variations in dielectric constant, leading to inconsistent properties.

2.1.2.3 Interface Quality

For all thin gate dielectrics, the interface with Si play a key role, and in most cases is the dominant factor in determining the overall electrical properties. A potential high-*k* gate dielectric should be able to provide a sufficiently high-quality interface with the Si channel, as close as possible to that of SiO_2. However, the typical production SiO_2 gate dielectrics have a midgap interface state density (D_{it}) of ~2×10^{10} states/cm^2, whereas most of the high-*k* materials show D_{it} ~ 10^{11}-10^{12} states/cm^2, and these increases in D_{it} observed in high-*k* gate dielectrics will tend to degrade leakage current and carrier mobility in the channel region. As discussed in **Chapter 1**, these two parameters are very important for evaluating MOSFETs' performances. Therefore, it seems that the ideal gate dielectric stack could have an interfacial layer comprised of several monolayers of Si-O containing material to improve interface properties, and also a high-*k* film on top of the interfacial layer to provide physically thicker gate dielectric. Even though the overall *k* value will be compromised in this case, this tradeoff for interfacial control will be acceptable as long as the resulting leakage currents are low enough.

2.1.2.4 Gate and Process Compatibility

As discussed in **Chapter 1**, poly-Si gate has been found to be reliable in CMOS technology for decades because precise control of dopant implant energy and dopant concentration can accurately tune the desired threshold voltage (V_{th}) for both n-MOS and p-MOS. However, it will likely be phased out for CMOS scaling in the longer term, after which a metal gate substitute seems to be required [1]. It is therefore desirable to employ a gate dielectric which will be compatible in direct contact with poly-Si gate, especially with potential metal gate materials. A detailed background for this point will be presented in the next section.

In addition, currently the process integration components have been well established in industry, such as depositing, annealing, and etching for conventional CMOS technology. It has also been shown that the method by which the dielectrics are deposited in a fabrication process is a crucial factor in determining the final film quality and properties. Therefore, the deposition process for the dielectric must be compatible with current or expected CMOS processing, cost, and throughput.

2.1.2.5 Reliability

The electrical reliability of a new gate dielectric must also be considered seriously for application in CMOS technology. Due to the difference of materials and fabrication process for high-*k* dielectrics from SiO_2, there are several areas of concerns for high-*k* dielectric reliability.

First of all, charge trapping during electrical stress is observed to be significant for high-*k* dielectrics. Large amount of fixed charge and charge trapping compared to SiO_2 were observed for various types of high-*k* dielectrics independent of the deposition techniques. The charge trapping centers responsible for the fixed and mobile charge may be at the interface of the bulk high-*k* and interfacial layer [22,23] or within the bulk high-*k* layer itself [24], and are highly polarity dependent [25].

These charge centers result in hysteresis, mobility degradation and significant instability in the V_{th}, which will pose a serious problem for high-*k* dielectric implementation. In addition, it has been shown that charge trapping may lead to polarity dependent high-*k* degradation and breakdown [24,25].

Secondly, it is believed that the breakdown mechanism of high-*k* stack is much more complicated than single SiO_2 dielectric. Previously, it was reported that gate current through high-*k* dielectrics showed both high level and low level fluctuations at the onset of soft breakdown [26]. At the same time, another report had also indicated that breakdown may occur at either the bulk or interfacial layer of the high-*k* stacks due to its intrinsic multi-layer structure [27]. As such, the breakdown mechanism as thickness of the high-*k* film is scaled downward is not clearly determined at the moment.

Besides these two major reliability issues, there are several other important reliability issues caused by the introduction of high-*k* dielectrics, including hot carrier aging due to the reduction of barrier height for electron and hole injection, the impact of plasma damage and process-related defects, which also need to be carefully considered for high-*k* real application.

2.1.3 Research Status of High-*k* Dielectrics

Initially, high-*k* materials were chosen as potential alternative gate dielectric candidates inspired by memory capacitor application, wherein the most commonly studied high-*k* gate dielectric candidates include Ta_2O_5, $SrTiO_3$ and Al_2O_3 material systems. Besides their feasibility in memory capacitor application, they have also been comprehensively investigated for the possible replacement of conventional SiO_2.

The *k* value of Ta_2O_5 is around 26, appropriate permittivity for the gate dielectric application. However, Ta_2O_5 is not thermally stable in direct contact with Si [28]. Thus an interfacial buffer layer of SiO_2 may be necessary to prevent the

interfacial reaction between Ta_2O_5 and Si substrate. This may increase process complexity and compromise the thickness scaling of gate dielectric. Also, the conduction band offset (ΔE_C) for Ta_2O_5 is much less than 1 eV [16], it will likely preclude using the Ta_2O_5 for gate dielectric application, since electron transport would lead to unacceptably high leakage currents.

At the same time, it has been reported that the materials with ultra high *k* value such as $SrTiO_3$ ($k \sim 80$) may cause fringing induced barrier lowering effect (*FIBL*) when used as the gate dielectric [17]. As introduced previously, this effect may seriously weaken the gate control capability and degrade the off-state characteristics in MOSFETs. Moreover, the thermal stability of $SrTiO_3$ in direct contact with Si is not very good, which has the similar problem as with Ta_2O_5.

Unlike the thermally unstable Ta_2O_5 and $SrTiO_3$, Al_2O_3 is a very stable and robust material when in direct contact with Si [16], and its ΔE_C is ~2.8 eV [19]. Moreover, it can maintain an amorphous structure under the process condition of interest. Hence, Al_2O_3 has many favorable properties compared to the above-mentioned high-*k* dielectrics. However, the Al_2O_3 gate dielectric shows poor reliability characteristics such as V_{th} instability induced by charge trapping effect [29]. Also, the *k* value of Al_2O_3 is only around 9.5 [19], which may not provide adequate benefits compared to the present SiON gate dielectric.

Due to the difficulties in searching for a suitable high-*k* gate dielectric among the mature materials for memory capacitor application mentioned above, some novel high-*k* materials have been studied and most of them, to date, are the metal oxides as shown in **Table 2.2**. It can be seen some of them are from group IIIB in the periodic table, such as Y_2O_3 and La_2O_3, and others are from group IVB, such as TiO_2, ZrO_2 and HfO_2.

Several research groups have studied the group IIIB metal oxides Y_2O_3 and La_2O_3 for the purpose of high-*k* dielectrics [30-34]. It has been demonstrated that the

Y_2O_3 gate dielectric showed very low leakage current and interface state density, without obvious relationship with the deposition process [30-32]. Also, it has been reported that a thick interfacial SiO_X layer between Y_2O_3 and Si substrate was formed during process [30,32], which indicates that the thermal stability of Y_2O_3 in direct contact with Si is still a serious issue. In addition, Chambers and Parsons found that the flat band voltages (V_{fb}) for the Y_2O_3 films shifted by 300-600 mV from those expected for ideal capacitors using the respective electrodes and substrate types [33]. Similarly, the La_2O_3 gate dielectric also exhibited low leakage currents and a large V_{fb} shift [32,34]. In addition, the interfacial SiO_X layer between La_2O_3 and Si is very thin, which implies its thermodynamic stability is better than that of Y_2O_3. However, the magnitude of the V_{fb} shifts measured in these two high-*k* systems, suggests a substantial fixed charge density in the bulk of the film, which may impede their application as gate dielectric.

For the group IVB metal oxides, TiO_2 as the gate dielectric was first reported by Campbell *et al.* [35]. The authors found that the TiO_2 gate dielectric showed a thick interfacial layer formation due to thermal instability, unacceptably high leakage current due to the low ΔE_C and large D_{it} of $10^{12}/cm^2$-eV. These results rule out TiO_2 application as the gate dielectric. ZrO_2 and HfO_2, also from group IVB metal oxides, received considerable attention due to their appropriate *k* value, ΔE_C, E_G and acceptable thermal stability in direct contact with Si. However, it was also found that compared with the case of HfO_2, the chemical properties for ZrO_2 would be degraded possibly due to the interaction of ZrO_2 with the poly-Si gate electrode as well as with the Si substrate to form silicide [36]. In addition, for chemical vapor deposited (CVD) ZrO_2 on Si substrate, interfacial SiO_X triggers the formation of Zr-silicide at the channel interface during ultra high vacuum (UHV) annealing with high temperature [37]. Thus, recently HfO_2 has been extensively studied among various high-*k* dielectric candidates. To further improve its thermal stability and crystallization temperature, several research groups incorporated silicon, aluminum and/or nitrogen into HfO_2 to form Hf-based gate dielectrics, such as HfSiO [38], HfAlO [39], HfON

[40], HfSiON [41] and HfAlON [42]. Moreover, some excellent electrical and reliability characteristics were also reported on this kind of Hf-based gate dielectrics, which are much closer to meet the requirements for future CMOS technology. Therefore, a lot of research groups from the semiconductor industry and academia have been making great efforts in an attempt to implement the Hf-based gate dielectrics in next generation CMOS technology.

2.1.4 Major Challenges of High-*k* Gate Dielectric Implementation

Even though the Hf-based gate dielectrics show the most promising characteristics for advanced CMOS application, however, there are still some challenges for integration of these Hf-based gate dielectrics, such as (1) permittivity degradation, (2) mobility degradation, (3) charge trapping induced V_{th} instability, and (4) high V_{th} induced by Fermi-level pinning (FLP) effect, which will be described as below. Besides these major challenges, some process issues of the Hf-based gate dielectrics, such as the film deposition and etching, needs to be carefully considered for their real application.

2.1.4.1 Permittivity Degradation

As discussed above, to further improve the thermal stability, the incorporation of Si, Al and/or N into HfO_2 film was proposed to form HfSiO (HfSiON) or HfAlO (HfAlON), which can retain its amorphous structure even after high temperature process. However, the dielectric constant of HfO_2 is significantly degraded by incorporating the Si or Al. The lower dielectric constant obtained in HfSiO (HfSiON) or HfAlO (HfAlON) is due to the oxide of Si or Al with much lower permittivity (SiO_2 ~ 3.9, Al_2O_3 ~ 9.5) as compared to HfO_2 (~ 25). This may compromise the benefits of the HfSiO (HfSiON) or HfAlO (HfAlON) gate dielectrics and limit the continuous scaling of gate dielectric thickness. Consequently, a high-*k* dielectric candidate with reasonable dielectric constant and also acceptable thermal stability is

still needed.

2.1.4.2 Mobility Degradation

Mobility is also a key parameter influencing overall MOSFET performance. However, serious mobility degradation can be observed for most of the high-*k* gate dielectrics, including Hf-based gate dielectrics [19,43]. Coulomb scattering due to the pre-existing and trapped charges in high-*k* films [44,45] and remote phonon scattering associated with the ionic properties of the "soft" metal-oxygen bonds in high-*k* films [46,47] have been proposed to account for the electron mobility degradation in high-*k* gate stacks. Among various high-*k* dielectric candidates, $HfSiO_X$ shows the most promising mobility characteristic [48], but its permittivity is relatively low. Even though some methods have been demonstrated to improve the mobility characteristics effectively, such as improving the microstructures of HfO_2 film [49,50] or inserting a $SiO_X(N)$ layer under the high-*k* film [50-52], the mobility degradation for high-*k* dielectrics as *EOT* scales down is still a concern [19].

2.1.4.3 Charge Trapping Induced V_{th} Instability

Charge trapping, which causes V_{fb} and V_{th} instability during operation, is also a key integration challenge for Hf-based gate dielectrics application in future CMOS technology [53]. The charge trapping centers responsible for the fixed charges are likely to occur within the bulk of the high-*k* film as well as at the interfaces of the high-*k* layer with the gate electrode [54] and with the underlying interfacial layer [22]. The fixed charge within the high-*k* film shifts V_{th} relative to that of SiO_2, and poses a serious issue for V_{th} control for production of circuits using high-*k* gate dielectrics. Even though rapid trapping and de-trapping have been observed recently during measurements [55] and demonstrated that the V_{th} shift under uniform static stress was overestimated compared to that under practical dynamic stress condition, the presence of charge trapping centers still fundamentally influences reliability of high-*k* stacks

and poses a challenge for the attainment of reliability goals.

2.1.4.4 Fermi Level Pinning Induced High V_{th}

Unacceptably high FLP-induced V_{th}, in particular for p-MOS, is another serious challenge for integration of the Hf-based gate dielectrics into poly-Si gate or even the advanced metal gate process [56]. It has been proposed that the V_{th} behavior in poly-Si/high-*k* device is dominated by the FLP effect, which is totally different from the poly-Si/SiO_2 device [56]. Hf-Si bond induced interface dipole [56] and/or oxygen vacancy induced charge transfer across the poly-Si/high-*k* interface [57-58] have been proposed to explain the FLP phenomenon. Moreover, the FLP effect was also observed in high-*k* gate dielectric with metal gate electrode, which may be due to the existence of metal induced gap states [59,60]. The unacceptably high V_{th} induced by the FLP effect seriously impedes the implementation of high-*k* gate dielectrics and metal gate electrodes and this effect will be further discussed in the following sections.

2.2 Metal Gate Electrodes

2.2.1 Scaling Limits for Conventional Gate Electrode

Before discussing metal gate (MG) electrodes, let us briefly review the background of the conventional gate electrode: poly-Si. Poly-Si is currently the most widely used gate electrode material for MOSFETs because it has an excellent compatibility with the self-aligned gate-first process and can be easily formed for dual gates. These merits make the poly-Si a superior gate electrode material for the gate-first CMOS process.

However, as discussed in **Chapter 1**, with MOSFETs scaling into the high performance (hp) 45 nm technology node and beyond, some fundamental limits of poly-Si become more and more serious and tend to retard the further improvement of

CMOS performance, such as poly-Si depletion, high sheet resistance and dopant penetration effect as mentioned before. In addition, high-*k* dielectrics would probably be finally required to break through the scaling limits of SiO_2 and SiON dielectrics in hp 45 nm technology and beyond. Therefore, besides the considerations from the high-*k* dielectrics themselves, the compatibility (or interface quality) between poly-Si and some promising high-*k* candidates is also a big challenge for the implementation of high-*k* with the conventional poly-Si electrode.

First and foremost, the FLP phenomenon will occur when poly-Si gate is in contact with many Hf-based high-*k* dielectrics, which leads to an undesirable V_{fb} shift, especially for p-MOSFETs [54,61-63]. This will lead to asymmetric high V_{th} for n- and p-MOSFETs, making these gate stacks difficult to be used for circuit design. To explore the origin of the FLP problem, dopant penetration from poly-Si gate into dielectric [61] or the formation of HfB_2 at the interface between p-type poly-Si and HfO_2 [64] were proposed to explain the high V_{th} in p-MOSFETs. But some later studies showed no evidence of HfB_2 formation at poly-Si/HfO_2 interface [57], and the high V_{th} in p-MOSFET had been established during the poly-Si deposition, irrespective of the dopant-type and the activation process [65]. C. W. Yang *et al.* suggested that the FLP effect can be attributed to the formation of accepter- and donor-like interface states, but the origin of the interface states was not identified [54]. C. Hobbs *et al.* proposed an Hf-Si bond induced dipole theory to explain the observed FLP phenomenon at the poly-Si/HfO_2 interface [56,66], however, this theory can not explain their own experiment that V_{fb} difference between p^+ and n^+ gates decreases remarkably by a only very small amount of HfO_2 deposition. Recently, K. Shiraishi *et al.* proposed another model in which the V_{fb} shift for p^+ poly-Si on Hf-based dielectrics was attributed to the oxygen vacancy (V_O) which promoted charge transfer across the interface [57]. However, it is difficult to explain the opposite shift of V_{fb} for n^+ and p^+ poly-Si gates using this model. Thus far there is still no universal theory or model to address this phenomenon. Apart from the disagreements in understanding the origin of the FLP effect, it is also a practical challenge to minimize this effect and

to obtain reasonably low V_{th} for p-MOSFETs. M. Koyama *et al.* demonstrated a method to reduce the FLP effect by carefully engineering the gradient of Hf concentration in HfSiON film, where a low Hf concentration near the poly-Si/HfSiON interface is required to achieve large V_{fb} difference between n^+ and p^+ poly-Si [67]. But the disadvantage of this method is the overall dielectric constant of the high-*k* dielectric will be sacrificed. Another way to reduce the high V_{th} for p-MOSFETs is to cap the Hf-based high-*k* by a thin AlO_x layer in the p-MOSFET region [68,69]. However, this will lead to a different *EOT* for n- and p-MOSFETs, as well as immense challenges in process integration. Finally, adding Ge into the poly-Si gate or using n^+ Ge as the gate electrode was proposed as potential solutions to reduce FLP due to the lower probability of forming V_O in Ge/high-*k* interface [70], but the process integration will be a potential issue.

The thermodynamic instability between poly-Si and many high-*k* materials will be another concern for the applications of poly-Si with high-*k* dielectrics. Poly-Si was found to be reactive with some of the high-*k* materials, e.g. ZrO_2 and HfO_2, which leads to excess leakage current and poor charge trapping properties to the high-*k* films. Inserting an Al_2O_3, Si_3N_4 or amorphous-Si layer between poly-Si and HfO_2 had been demonstrated to improve the thermodynamic stability and lower the gate leakage density of poly-Si/HfO_2 stack by several orders [63,71,72]. Incorporating nitrogen into gate dielectric to form HfON or HfSiON is another approach to improve the thermal/electrical stability of poly-Si/high-*k* gate stacks [40,73]. Similarly, the overall dielectric constant of the high-*k* dielectric will be sacrificed by these methods.

As a result, MG technology has been extensively studied in recent years and is likely to replace poly-Si gate in hp 45 nm technology node and beyond because a MG material not only eliminates the poly-Si depletion and dopant penetration problems, but also greatly reduces the gate sheet resistance. However, the insertion of MG electrodes may also bring about other new problems. Therefore, careful consideration of the choice of metals for the gate electrode is needed. The following sections will

review the selection guidelines for MG candidates first, followed by research status of MG technology and major challenges of MG implementation.

2.2.2 Selection Guidelines for Metal Gate Electrodes

2.2.2.1 Material Considerations for Metal Gate Electrodes

The metal for the gate electrode application should possess all the good characteristics of poly-Si that are qualified for the gate application. Firstly, the thermal stability of MG candidates at processing temperatures is an important issue. It should be stable with the underlying gate oxide so as to sustain the high processing temperature without mechanical failure and not be oxidized during the process. In addition, it should be free of mobile charge, have low resistivity, surface states and satisfactory breakdown strength. The more subtle electrical property issue is that it should have a suitable work function, which ultimately affects V_{th} of MOSFET. The following subsections will describe the required material properties in terms of thermal stability considerations and work function requirements.

(a) Thermal Stability Considerations

One of the most important parameters for MG candidates is their thermal stability. In current gate-first process, gate electrode is formed prior to the source/drain implantation and dopant activation annealing, which implies that the metal candidate and the metal-dielectric interface should be robust enough to stand up to a high thermal budget. However, the interface reaction or inter-diffusion between MG and the underlying gate dielectric always happen during the device fabrication process, wherein the interface reaction is thermodynamically driven, and likely to happen at the interface where the atoms have large differences in electronegativity and radius [74]. It has also been found that many metals with low work function (WF), like Ta, Hf, Ti and so on, tend to react with the gate dielectric at high temperature

[75,76]. On the other hand, some metals with high WF such as Pt, Ir, and Ni tend to diffuse or penetrate through the gate dielectric during the high temperature process.

In addition to the metal reaction/diffusion, some other thermal stability issues such as microstructure change, stress generation, and oxygen penetration at high-temperature should also be carefully avoided. Phase change or grain growth may affect the WF of MGs and roughen the gate-dielectric interface, leading to a change of V_{th} and channel mobility upon annealing [77,78]. Moreover, due to the extreme high temperature and the ultra-fast temperature ramp up/down rate used in conventional CMOS manufacturing process, the thermal induced stress would be a serious problem for MGs, especially for those who have very different expansion properties from Si and/or the underlying dielectric. The generated stress in the MOS stack will bring in some adherence problems, and even cause the metal film to crack or peel off after annealing. Besides these above-mentioned thermal stability issues, some metals also show poor barrier properties due to the diffusion of oxygen at high temperature [79]. This can lead to re-growth of the interfacial layer under the high-*k* dielectric due to the penetration of oxygen residues or moisture from the gas ambient during annealing, which makes it challenging to scale the *EOT* down to sub-1 nm.

(b) Work Function Requirements

Another important parameter for MG candidates is their WF because it directly affects V_{th} of MOSFET, which has the most direct impact on the operation of a MOSFET. In MOSFET, the V_{th} of a surface channel device is typically expressed as [80]:

$$V_{th} = V_{fb} + 2\Phi_B + \frac{Q_d}{C_{ox}} = V_{fb} + 2\Phi_B + \frac{\sqrt{4\varepsilon_{Si} q N_b \Phi_B}}{C_{ox}} \qquad (2\text{-}1)$$

where Φ_B is the difference between the Fermi-level and the intrinsic level in Si, ε_{Si} is the permittivity of Si, Q_d is the total depletion charge in the channel region, N_b is the doping concentration of Si substrate (for uniform channel doping), C_{ox} is the gate

oxide capacitance, and V_{fb} is the flat band voltage across the MOS stack. V_{fb} can be further given by the following equation:

$$V_{fb} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} = (\Phi_M - \Phi_S) - \frac{Q_{ox}}{\varepsilon_0 \varepsilon_{SiO_2}} \bullet EOT \qquad (2\text{-}2)$$

where Φ_{MS} denotes the WF difference between the metal gate and silicon substrate, Q_{ox} represents the equivalent oxide charge density at the oxide/Si interface. It is therefore clear that V_{th} is directly controlled by Φ_M for a given technology (such as N_b, C_{ox} and Q_{ox}).

For sub-50 nm bulk-Si devices, it has been demonstrated that the optimal WF values required for NMOS and PMOS should be about 4.05~4.25 eV and 4.97~5.17 eV, respectively [81]. In other words, the WF of MGs should be within 0.2 eV from the band-edges of Si. In addition, for the fully-depleted and multi-gate devices, e.g. FDSOI or FinFET, the V_{th} will be determined only by the WF of MG since the channel region is almost intrinsic; accordingly the MGs with WF of ± 0.15 eV from the midgap position of Si will be best served for high-performance applications [1,82]. Recent study also shows that when the body thickness of UTBSOI devices shrinks to less than 5 nm, band-edge WF will again be required due to the carrier quantization effect [83]. Therefore, metal materials with different WF values will be needed for various applications [1].

2.2.2.2 Process Considerations for Metal Gate Electrodes

Process integration issue is another tough challenge for the implementation of MG in CMOS fabrication. It includes metal deposition techniques, metal etching and post-etching cleaning issues, and the dual metal gate integration process.

The metal deposition techniques can affect the properties of metal gate electrode in many aspects, such as film morphology, resistivity, work function, thermal stability, and even the gate stack reliability [85-87]. The most commonly used method to deposit metal gate is physical vapor deposition (PVD) technique, including

sputtering, evaporation and so on. For all the PVD deposition techniques, a fundamental limit is the step coverage issue in high aspect ratio structures [88], which may limit the applications of PVD techniques in 3-D device structures. However, this problem can be addressed by using CVD methods. The CVD methods not only have the advantages such as good step coverage and low damage to the dielectric, but they provide a number of variables, including temperature, pressure and gas flows which could be useful to control the film microstructure [88]. Among many kinds of CVD techniques, metal-organic chemical vapor deposition (MOCVD) and atomic-layer chemical vapor deposition (ALCVD) are two most important forms. Recently, ALCVD (or ALD) has drawn considerable attention and has been utilized to deposit metal gate as well as high-*k* films. The major advantage of ALD technique is that it provides the ability to control the atoms layer by layer such that the film concentration and even the interface chemistry can be well engineered. However, one concern for ALD technique is its relative long lead time and hence low throughput due to the need to purge the ambient in every deposition cycle.

Metal etching and post-etching cleaning of metal gate electrodes is another practical issue for the integration of MG in CMOS process. To achieve high selectivity, vertical profile, and small feature size in the metal gate etching process, the selections of masks (photoresist or hard mask), etchant and the post-etching cleaning process need to be optimized systematically according to the properties of the specific MG materials. These practical issues can even affect the selection of metal gate candidates.

For the dual MG integration, a simple, reliable, and cost-effective scheme to integrate dual MGs on a same wafer would be desirable. The integration schemes generally fall into either metal gate first or metal gate last categories. For metal gate first integration, the gate electrode is typically patterned by dry etching at the same place in the flow as for conventional poly-Si and is therefore subjected to the source/drain anneal, which requires excellent thermal stability for both n- and p-type

MG candidates, as well as refined metal etching and post-etching cleaning techniques [89,90]. While for metal gate last integration, the gate electrode in its final state is formed much later in the flow, typically after the source/drain activation anneal, and is therefore exposed to a much lower back-end thermal budget, which results in much less stringent requirements on the thermal stability for MG materials, but the process is relatively complex [91,92]. More details on the dual MG integration schemes will be discussed in **Section 2.2.4.2**.

2.2.3 Research Status of Metal Gate Electrodes

Many MG candidates have been investigated in recent research, including some pure refractory metals, metal nitrides, metal carbides, conductive metal oxides and fully silicided (FUSI) metal gates.

(a) Pure Refractory Metals

For pure refractory metals, they are good choices primarily due to their high melting points, which allow them to be used at the high temperatures necessary for source/drain activation. Some metals such as W, Mo, Ta, Ni and Pt have been studied [93-95]. However, it was found that many of these elemental materials, especially those with n-type WF, undergo reactions with the underlying gate dielectrics, while some of them become unstable due to agglomeration. In addition, the use of this kind of refractory metals additionally introduces the complexity of etching. To achieve dual WF values for n- and p-MOSFET respectively, some of these refractory metals were used to form a new alloy by inter-diffusion with another metal, such as Ti-Ni alloy [91], Ru-Ta alloy [96], Ta-Pt alloy [97], Ti-Pt alloy [98], and Hf-Mo alloy [99]. The advantage of this approach is that there is no need to expose the dielectric to any etching process and wide range WF modulation (more than 1 eV) and precise WF control could be achieved using this approach. However, an inherent concern of this method is the thermal stability, which is typically limited by n-type metals with low

WF used in the alloys. As a result, the alloying temperature is typically around 400^{o}C to 600^{o}C. This greatly limits the applications of these metal candidates in gate-first CMOS process.

(b) Metal Nitrides and Metal Carbides

Compared with many pure metal materials, metal nitrides and metal carbides, such as HfN, WN, TiN, TaN, TaC and HfC, would be of priority due to their excellent thermal stability as well as exceptional mechanical and electrical properties [79,86,100-103]. In addition, these MG candidates also tend to have stable interface with high-*k* dielectrics, rendering excellent *EOT* scalability to be achievable. However, most of these MG candidates possess WF values close to the mid-gap of Si, which are inappropriate for bulk-Si dual MG CMOS technology. To enlarge the WF tuning range, several approaches have been explored. Adding Si [104] and Al [105] into metal nitrides to form ternary compound or modifying the nitrogen concentration [106,107] of metal nitrides have been demonstrated to be useful for NMOS and PMOS, respectively, but the work function tuning range is not adequate for bulk-Si CMOS. In recent works, a novel approach to incorporate lanthanide into metal nitrides to reduce the work function of TaN or HfN was proposed [108,109], but some of those promising characteristics are only limited to n-MOS.

(c) Conductive Metal Oxides

Conductive metal oxides become a possible choice as the effective electronegativity of conductive oxides is generally higher than those of other compound metals such as metal nitrides and metal carbides. This will also increase the corresponding WF, such as those of IrO_2, ReO_2, MoO_2, WO_2 and RuO_2, which have vacuum WF larger than 5.0 eV [74,110,111]. However, the drawback of these conductive oxides lies in the poor stability at elevated temperatures [74,112].

(d) FUSI Metal Gates

FUSI metal gate technology has drawn considerable attention and steady progress have been achieved in recent years because of compatibility with conventional CMOS process flow, which will reduce the cost and risk for the technology migration. In 2001, FUSI Co-silicide ($CoSi_2$) and Ni-silicide (NiSi) were first proposed for gate application, wherein the WF of $CoSi_2$ is about 4.6 eV, rendering the V_{th} of bulk-Si CMOSFET too high to be acceptable [113]. The work function of NiSi can be modulated from about 4.6 eV to 5.0 eV by changing the dopants in poly-Si [114] and there is no voiding problem in the formation of NiSi, unlike $CoSi_2$. These make NiSi gate process a promising candidate for dual metal gate process [115-118]. However, the WF tuning of NiSi through the dopant segregation approach seems ineffective on high-*k* dielectrics because of the FLP effect caused by Hf-Si bonds at the NiSi/high-*k* interface, similar to that in poly-Si/high-*k* interface [65,119,120]. In order to solve this problem, phase-controlled silicide technology was developed [119,120]. It has been found that the Ni_3Si phase with the high WF of 4.8 eV and $NiSi_2$ phase with the low WF of 4.4 eV on HfSiON dielectric, are still far away from the required WF for p- and n-MOSFET respectively. In order to enlarge the work function tunable window in FUSI/high-*k* stacks further, some NiSi alloy FUSI gates were proposed, such as $Ni_{1-x}Yb_xSi_y$, $Ni_{1-x}Ta_xSi_y$, or $Ni_{1-x}Al_xSi_y$ for NMOS and $Ni_{1-x}Pt_xSi_y$ for PMOS [121-123]. However, the WF tuning range is still not large enough for planar bulk-Si devices, especially for p-type MG. In addition, no appropriate integration scheme is demonstrated to integrate this kind of FUSI gates together with high-*k* dielectrics.

In summary, even though promising results have been achieved in developing potential MG materials for next generation CMOSFETs, there are still some challenges for MG implementation which needs to be addressed.

2.2.4 Major Challenges of Metal Gate Implementation

According to *ITRS* 2005 [1], it is most likely that MG technology will be introduced into production together with high-*k* dielectric. However, it has been found that the effective work function (EWF) of some MGs measured on high-*k* dielectrics deviates from the WF values measured in vacuum and exhibits large dependence on the underlying dielectrics [59], which makes the identification of right MG materials on high-*k* dielectrics more complicated. In addition, when employing dual MG CMOS technology, i.e. n-type metal for n-channel devices and p-type metal for p-channel devices, the appropriate integration of two different types of MGs in a device fabrication process is also one of the most important challenges.

2.2.4.1 Right Metal Gate Materials

Although the WF of a metal material in vacuum can be precisely measured as a physical parameter of the metal material itself, the EWF of MG in a real MOS structure, affecting V_{th} and performance of the MOSFET eventually, will be affected by many other factors, such as the crystallinity, deposition technique, impurity, and most importantly, the underlying gate dielectrics [59]. Therefore, the first issue that needs to be considered for MG implementation is its EWF on high-*k* dielectric candidates. The dependence of the metal gate EWF on the gate dielectric materials was explained by applying an interface dipole theory [59,124], wherein the intrinsic states or metal-induced gap states (MIGS) are believed to be the major factor in determining the EWF of metals on high-*k* materials. This model has been particularly successful for metal/dielectric interfaces where there is minimal interfacial reaction or where MIGS dominate. However, it is not clear whether this model can be applied to explain the instability of the metal gate WF during the thermal annealing processes, which becomes more pronounced when the annealing temperature is higher. Another model that takes into account the role of extrinsic states at metal/dielectric interfaces, possibly arising from defects, or interfacial reaction, was recently proposed to

qualitatively explain the WF instability phenomenon [125]. However, the knowledge on this crucial interface is still insufficient to guide us in choosing the right MG materials. Therefore, engineering of the material system at the metal/dielectric interface is a very important consideration for device integration, especially for conventional bulk-Si CMOSFETs.

2.2.4.2 Appropriate Dual Metal Gate Integration Process

Besides the achievement of the appropriate EWF at the metal/dielectric interface, one of the most important challenges in MG CMOS technology is the integration of two different types of MGs for n- and p-MOSFETs respectively in a device fabrication process. Many factors need to be considered when integrating dual MGs, such as process complexity and controllability, gate oxide integrity, *EOT* scalability, which will ultimately affect the selection of metal materials.

As described before, there are basically two groups of integration schemes: metal gate first and metal gate last.

Gate first integration is extremely challenging because it requires the gate electrode to undergo many front-end steps. The first step is to form different metals over the n- and p-MOSFETs. Once the electrodes are formed, the ability to define the gates by simultaneously dry etching the two dissimilar materials must be established. Integration of the patterned electrode with the subsequent cleans and sidewall formation is challenging as well. Since gate first integration requires the MG electrode to be in contact with the gate dielectric during the source/drain activation anneal, the thermal stability of the gate electrode with respect to the underlying gate dielectric and any other films (e.g., sidewalls) in the gate stack is a critical issue. Many of the metals considered for n-type metal candidates, such as Ti, Hf, Zr and Ta, tend to be quite reactive with the dielectric. As a result, *EOT* and leakage current of the gate dielectric and/or the WF of the electrode itself may be uncontrollably modified during high-temperature processing. Even though some metal nitrides and

ternary metal nitrides have been proposed since they tend to be more stable in contact with dielectrics than the transition metals [100-109], gate first CMOS integration with satisfying band edge electrodes has not yet been reported on any gate dielectric.

Gate last integration options are attractive because they eliminate exposure of the MG to many of the front-end process steps associated with gate first flows and they relax the thermal stability requirements of the gate stack materials. However, gate last integration scheme are not without issues themselves. The damascene replacement gate process flow, extensively used for evaluation of metal gates, has inherent disadvantages, such as etching down to the gate dielectric, having a gate dielectric grown at low temperatures, planarization control and self-alignment issues [92,126]. Doped FUSI gates, using NiSi formed from doped poly-Si has received much attention lately as a gate last approach [114-118]. The use of NiSi is highly desirable because it utilizes known materials and processes with only little modifications to the conventional integration process, can be scaled to narrow line widths, and has a relatively low volume expansion upon full silicidation. Even with these advantages, this approach is not without its own challenges. For example, WF tuning to satisfying band edge values for NiSi has not been reported yet on high-*k* dielectrics, especially for p-type gate electrode. In addition, there could be problems with the simultaneous silicidation of n- and p-type gates. Although gate last integration alleviates some of the gate electrode issues associated with gate first scheme, considerable work remains for a full CMOS demonstration.

2.3 Research Scope and Major Achievements in This Thesis

The implementation of advanced gate stacks involving high-*k* gate dielectrics and MG electrodes for next generation CMOS technology is the overall objective of this thesis. In particular, several approaches will be presented to address the major challenges for integration of the high-*k* gate dielectrics and MG electrodes as

described above, including the selection of appropriate gate stack materials as well as proper dual MG CMOS integration schemes.

In **Chapter 3**, lanthanum (La) was incorporated into HfO_2 to form HfLaO gate dielectric, which possesses sufficiently high crystallization temperature, good thermal stability, high carrier mobility, and also maintains a high *k* value. In addition, by employing this high-*k* gate dielectric, the V_{fb} and V_{th} of metal electrode gated MOS devices can be tuned effectively in a wide range (wider than that from Si conduction band-edge to Si valence band-edge), after a 1000^{o}C annealing required by a conventional CMOS source/drain activation process. These results suggest that lanthanum-incorporated HfO_2 could be a promising gate dielectric candidate in advanced gate stacks. Moreover, a specific model based on the interfacial dipole between MG and HfLaO is proposed to interpret the particular results above and more experimental data from other gate stacks have been demonstrated to agree with this model. Therefore, this may provide an additionally practical guideline for choosing appropriate gate stacks to meet the requirements of future CMOS devices.

Based on the above understanding and results, dual MGs with continuously tunable WF in a very wide range from 3.9 eV to 5.2 eV by using HfLaO gate dielectric and vertical stacks of TaN/Ru metal layers were experimentally demonstrated for the first time in **Chapter 4**. The wide tunability of WF for this bilayer metal structure is attributed to metal inter-diffusion during annealing and the release of Fermi level pinning between metal gates (Ru and TaN) and HfLaO. Moreover, this change is thermally stable and not affected by subsequent high temperature process (1000^{o}C). Based on these results, a gate-first integration process using high-temperature metal inter-mixing technique to achieve dual WF is proposed and demonstrated. In addition, another feasible dual MG integration process, which has good compatibility with conventional CMOS technology, is also proposed in this chapter by employing doped refractory metal nitrides, where lanthanide and aluminum doped refractory metal nitrides ($(M_xLa_{1-x})N_y$ and $(M_xAl_{1-x})N_y$) act as n- and

p-type MG respectively. All of these attempts could be of practical values for the community in developing the dual MG solutions for future CMOS technology.

In **Chapter 5**, reliability issue regarding bias temperature instability (BTI) degradation in MOSFETs with TaN/high-*k* gate stacks (including HfO_2 and $Hf_{1-x}La_xO_y$) were investigated. First, the V_{th} instability in both n- and p-MOSFETs with HfO_2 gate dielectric under both static and dynamic stresses was systematically investigated. The V_{th} evolution was shown to have a power law dependence on stress time, having a fast initial stage followed by a slow stage. In addition, the BTI degradation is frequency dependent with reduced degradation at higher stress frequency for a given gate voltage amplitude and stress time, which suggests that BTI degradation under static stresses was overestimated compared to that in practical digital IC applications and it may not be the "show-stopper" in the implementation of HfO_2 MOSFETs. A new physical model that accounts for carrier trapping/de-trapping and trap generation in the HfO_2 dielectric under stress is proposed, with simulation results in good agreement with all experiment data. After that, BTI degradation in n-MOSFETs with $Hf_{1-x}La_xO_y$ gate dielectric was compared to that with HfO_2 gate dielectric under dynamic stresses. The observation of one order reduction of V_{th} shift for $Hf_{(1-x)}La_xO_y$ with 50% La compared to HfO_2 implies that the incorporation of La into HfO_2 also suppresses charge trapping in the dielectric, which further justifies HfLaO as a promising gate dielectric.

Finally, **Chapter 6** concludes the thesis with some suggestions for future research based on the findings and conclusions arrived in this thesis.

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Chapter 3

A Novel HfLaO Gate Dielectric with Excellent Properties for Advanced Gate Dielectric Application

3.1 Introduction

The aggressive down scaling of complementary metal-oxide-semiconductor (CMOS) devices has led to a substantial increase in tunneling currents (i.e. an increase in gate leakage current) through the ultra-thin gate dielectrics. High dielectric constant (*k*) materials are currently explored as alternative gate dielectrics to replace conventional SiO_2 and SiON gate dielectrics to address the issues of high gate leakage currents and device reliability [1]. Currently, HfO_2 has emerged as one of the most promising high-*k* gate dielectrics for integration in CMOS devices due to its high dielectric constant, wide band gap and good thermal stability on Si [2]. However, HfO_2 has been shown to crystallize at relatively low temperatures (~400^oC) [3], which leads to an increase in grain boundary leakage, inhomogeneity of the dielectric constant and variations in film thicknesses uniformity [2,4]. Recently, the incorporation of Si, Al, N or Ta into the HfO_2 film has been demonstrated to increase the crystallization temperature of HfO_2 films. The increase in crystallization temperature relaxes the constraint on the maximum permissible dopant activation temperature in the implementation of high-*k* dielectrics in metal-oxide-semiconductor field-effect transistors (MOSFETs) [3,5-7]. However, the incorporation of SiO_2, Al_2O_3 or their nitrides degrades the dielectric constant, while adding Ta_2O_5 into HfO_2 reduces the electron barrier between HfO_2 and Si substrate. All of these lead to larger gate leakage currents compared to pure HfO_2 for the same equivalent oxide thickness (*EOT*) and limit the continuous scaling of gate dielectric thickness. Moreover, as discussed in **Chapter 2**, there is still a challenge for these Hf-based dielectrics, i.e.

effective work functions (Φ_{eff} or EWFs) after high thermal budget treatment for most of gate electrodes including poly-Si and metal gates (MGs), especially for p-type MGs, can not match their vacuum work functions, possibly due to Fermi-level pinning (FLP) effect [8,9].

Recently, La_2O_3 have been shown to possess advantageous material characteristics favourable for integration as a high-*k* dielectric material in advanced MOSFETs, such as a high dielectric constant (*k*~30), a relatively large band gap (~6 eV) and a high electron barrier to Si (2.3 eV) [2,10]. In addition, La_2O_3 possesses a higher film crystallization temperature as compared to HfO_2 and is thermodynamically stable on Si [11]. However, it is important to note that pure La has shown to absorb moisture readily when exposed to air [2,12].

In this chapter, we first demonstrate that the incorporation of La into HfO_2 increases the crystallization temperature (up to 900^{o}C) of pure HfO_2 and maintains comparable gate leakage currents with pure HfO_2 film. Then we show that n-MOSFETs fabricated with HfLaO gate dielectric exhibit superior device characteristics (such as drive current and effective electron mobility) compared to n-MOSFETs fabricated with HfO_2 gate dielectric. We also report for the first time that with a thermal budget of 1000^{o}C, FLP in the MG/high-*k* stacks can be released by employing HfLaO. The EWF can be tuned in a wide range, more than the requirements of bulk-Si CMOSFETs. As prototype examples, TaN gate with EWF ~3.9-4.4 eV and Pt gate with EWF ~5.5 eV are shown. To interpret the above particular results, a specific model based on the interfacial dipole theory between MG and HfLaO is proposed and is validated by subsequent electrical data from more gate stacks involving other lanthanide elements incorporated HfO_2 films and MGs.

3.2 Experiments

MOS devices were fabricated on n- or p-type (100) Si substrates with doping concentration of $6x10^{15}$ cm^{-3}. Field oxide of approximately 400 nm was thermally grown and subsequently patterned for active area definition. A standard pre-gate clean was performed prior to high-*k* dielectric deposition. HfO_2 and HfLaO films with different La concentration and thicknesses were deposited using reactive DC magnetron sputtering with low oxygen concentrations at room temperature. Ex-situ post deposition anneal (PDA) in N_2 were then performed at 600^oC for 30 s with a small amount of O_2 to improve the high-*k* film quality. Here, it should be noted that HfLa target (Hf:La=1:1, atomic percentage) was used in this work to reduce moisture absorption of La during exposure to air [12]. We also tried to shorten the period between metal gate deposition and HfLaO deposition to minimize the possible moisture absorption. In addition, even though there was still some water absorbed during the device fabrication, it has been demonstrated that the absorbed moisture can be annealed out, even at relatively low temperatures [13]. The composition of La in HfLaO films was controlled by the DC power ratio between Hf and HfLa targets during co-sputtering. The gate electrode comprises of either a pure TaN (~150 nm) or HfN (~50 nm) capped with a TaN layer (~100 nm) for n-MOS devices and Pt (~50 nm) for p-MOS devices, formed by reactive sputtering and DC sputtering respectively, followed by gate patterning. The devices then went through rapid thermal annealing (RTA) treatment from 600°C to 1000°C with different ambient for thermal stability evaluation. For MOSFET fabrication, source/drain implantations of arsenic (100 keV, $1x10^{15}$ cm^{-2}) / BF_2 (50 keV, $1x10^{15}$ cm^{-2}) were performed for n-MOSFETs / p-MOSFETs, respectively, followed by RTA activation at 1000^oC for 5 s. Finally, all samples received backside Al metallization and forming gas annealing (FGA) at 420^oC for 30 min.

The ratio of La to (La+Hf) in the HfLaO films was determined to be 15% and 50% by X-ray photoelectron spectroscopy (XPS) using La 3d and Hf 4f region.

Structural analysis was then performed with X-ray diffraction (XRD) and Fourier transform infrared (FTIR) analysis for the deposited HfO_2 and HfLaO films with thicknesses of ~30 nm and ~200 nm, respectively. The physical thicknesses of the films were determined by ellipsometer and/or transmission electron microscopy (TEM). Capacitance-voltage (*C-V*) measurements were performed on (100x100 μm^2) MOS capacitors at a frequency of 100 kHz with a HP 4284A precision LCR meter. Quantum mechanical correction was applied to the simulated *C-V* curves for the extraction of flat-band voltage (V_{fb}) and *EOT* in this work. Current-voltage (*I-V*) measurements were performed using a HP 4156A semiconductor parameter analyzer. Electron mobility was calculated by a standard split *C-V* method on MOSFETs.

3.3 Results and Discussion

3.3.1 Physical Properties of HfLaO

The XRD spectra for HfO_2 and HfLaO films with 15% and 50% La are shown in **Fig. 3.1**. The films were checked for similar physical thickness (~30 nm), and were subjected to an identical RTA at 600^{o}C or 900^{o}C for 30 s in a N_2 ambient for consistency. It can be seen the $(\bar{1}11)$ crystalline peak of HfO_2 emerges clearly after 600^{o}C anneal, while the incorporation of La in HfO_2 suppresses the crystallization of the HfLaO films. In addition, the crystallization temperature was observed to increase with increasing La concentration. This is believed that the incorporation of La breaks the periodicity and/or inhibits the continuous crystal growth of HfO_2 during rapid thermal annealing [14].

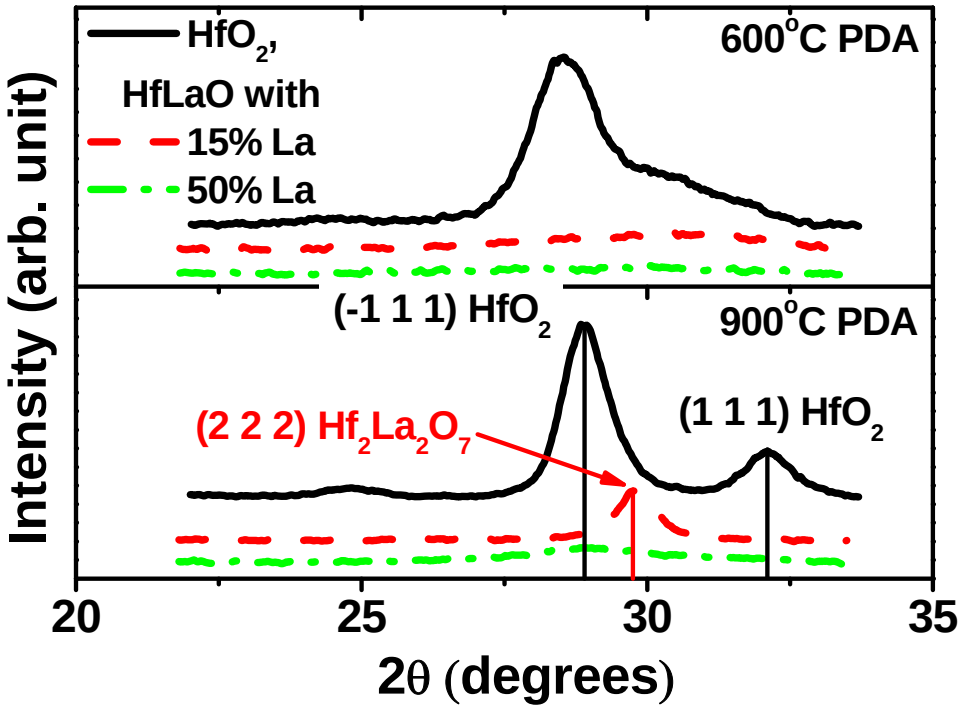


Fig. 3.1: XRD spectra of HfO_2, HfLaO films with 15% and 50% La after 600°C and 900°C annealing for 30 s in N_2. The La incorporated in HfO_2 films can increase the crystallization temperature up to 900°C.

To further investigate the structural characteristics of HfLaO films, FTIR spectroscopy was employed due to its unique ability to detect the onset of HfO_2 crystallization and its microscopic bonding state change in the far infrared region [15]. The infrared absorption spectra of HfO_2 and HfLaO films with 50% La (~200 nm) as a function of annealing temperature are shown in **Fig. 3.2**. The undoped HfO_2 film, after annealing at 600°C and 900°C, shows several peaks corresponding to the monoclinic HfO_2 phonon modes [16]. However, the HfLaO film shows a broad peak around 300 cm^{-1}, which indicates that the structure of HfLaO with 50% La remains amorphous after 900°C annealing. This also indicates an enlargement of the crystallization due to the incorporation of La into HfO_2 dielectric. The different coordination structure and bonding between HfO_2 and La_2O_3 are held responsible for the enlargement of crystallization energy observed. The structural modification is speculated to improve the carrier mobility because of the reduction of the phonon polarization in dielectric layer and disappearance of lowest energy phonons, P4 and

P5 in HfO_2 spectra in **Fig. 3.2** [17], which probably correspond to the remote phonon scattering.

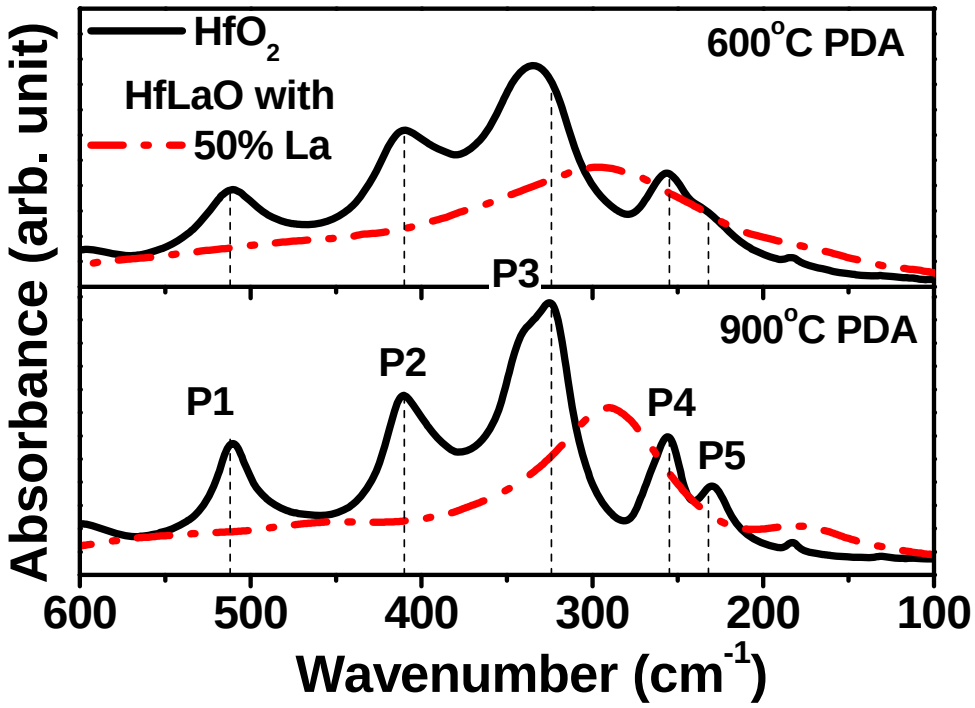


Fig. 3.2: FTIR spectra of HfLaO with 50% La and HfO_2 films annealed at 600°C and 900°C. The HfO_2 films show the FTIR peaks P1-P5, which are consistent with 512, 410, 324, 255 and 232 cm^{-1} peaks of the monoclinic HfO_2 phase reported in [16]. However, adding La into HfO_2 changes the spectra, indicating changes of atomic bonding and phonon energy.

The cross-sectional high-resolution TEM images of HfO_2 and HfLaO films with 15% and 50% La incorporation after PDA at 600°C for 30 s and activation at 900°C for 30 s are shown in **Fig. 3.3**. The TEM pictures confirmed that the HfO_2 high-*k* layer, corresponding to "Hi-*k*" layer in the figure, is fully crystallized, while HfLaO high-*k* films with 15% and 50% La remain amorphous following identical annealing conditions. It should be noted that the crystallinity for HfLaO films with 15% La observed by TEM is different from that of XRD as shown in **Fig. 3.1**. This is attributed to the difference in thicknesses for samples selected for XRD (~ 30 nm) and TEM (~ 5nm) analysis.

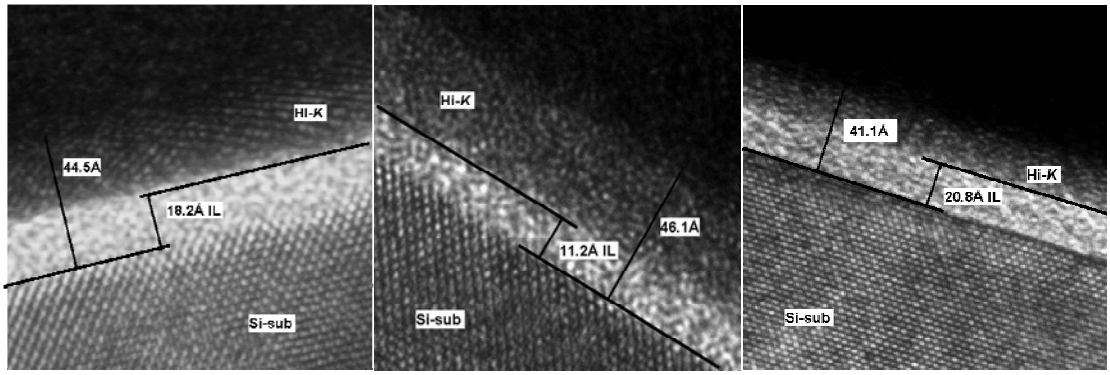


Fig. 3.3: TEM images of HfO_2 (Left) and HfLaO with 15% (Middle) and 50% La (Right) after PDA at 600ºC for 30 s and RTA at 900ºC for 30s. The HfO_2 film is fully crystallized whereas both of the HfLaO films remain amorphous. In addition, all of them have a thick interfacial layer (IL) compared to total thickness of dielectric layer, including Hi-*k* and IL in the figure.

Figure 3.4 shows the XPS Si 2p spectra of HfO_2 and HfLaO with 15% and 50% La films after 900^{o}C PDA for 30 s. The two main peaks observed in the spectra for the samples investigated can be attributed to that of the Si substrate (~99.3 eV) and the interfacial layer. For the HfO_2 sample, the location of that peak is approximately 102.8 eV, which is different from that of a pure SiO_2 layer (103.6 eV) [18]. The difference in the binding energies obtained for the SiO_2 and interfacial layer indicates that the composition of interfacial layer is possibly a silicate-like compound [19]. However, as the La concentration is increased from 0 to 15% and subsequently to 50%, there is an obvious increase in the intensity of the peak and a shift towards a higher binding energy (~103.6 eV). Although the signal of the Si 2p peak from the interface between HfLaO and Si was partially overlapped by the La $4d_{5/2}$ peak, we are still able to detect the existence of the Si−O bond at the interface from the change in relative intensity of the La $4d_{3/2}$ and La $4d_{5/2}$ peaks. Therefore, the increase of the intensity and the shift of the peak are partially due to the increase in atomic percentage of Si–O bonds in the interfacial layer with the incorporation of La into HfO_2. It is believed that a chemical similarity between that of HfLaO/Si interface and the high quality SiO_2/Si interface exists.

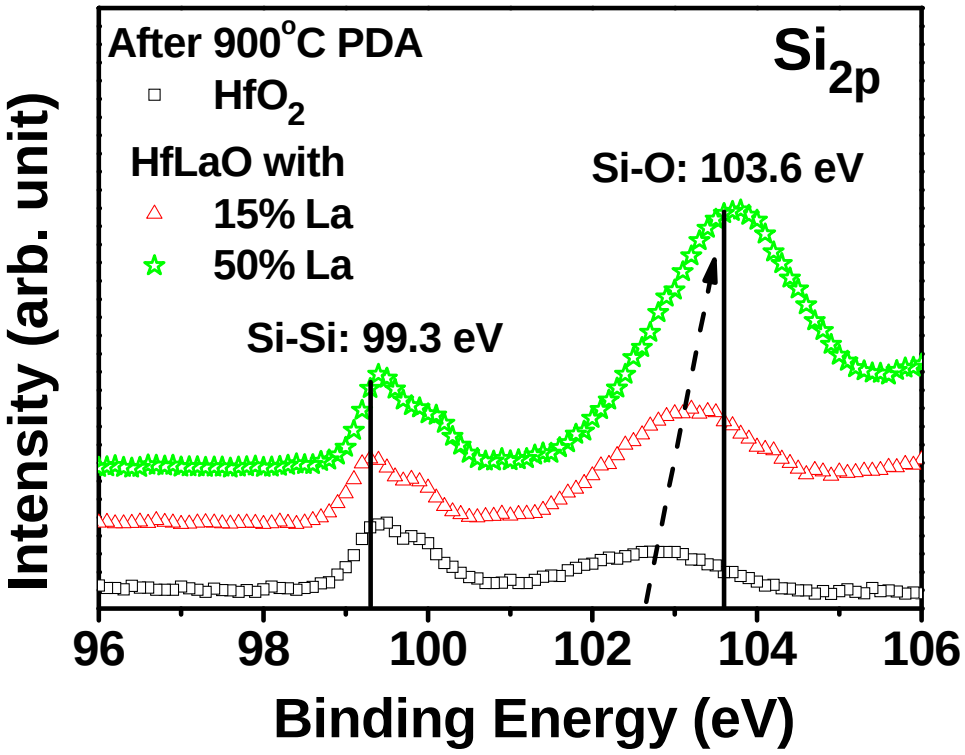


Fig. 3.4: XPS spectra for Si 2p core level taken from HfO2, HfLaO with 15% and 50% La films after PDA at 900°C for 30 s. The increase of the peak intensity for silicate-like interfacial layer and a shift toward high binding energy are observed after incorporating La into HfO_2.

Figure 3.5 shows hysteresis for HfO_2 and HfLaO with 50% La films after post-metallization annealing (PMA) at 900ºC for 30 s, where the hysteresis was quantified by the difference in V_{fb} during the voltage sweeps without delay time between ±3 V. It can be seen that the hysteresis for HfO_2 film was significantly improved by incorporating La, which indicates that the interface traps and/or oxide traps may be significantly reduced by incorporation of La into HfO_2. This may be due to the increased atomic percentage of Si-O bonds in interfacial layer as discussed in **Fig. 3.4**.

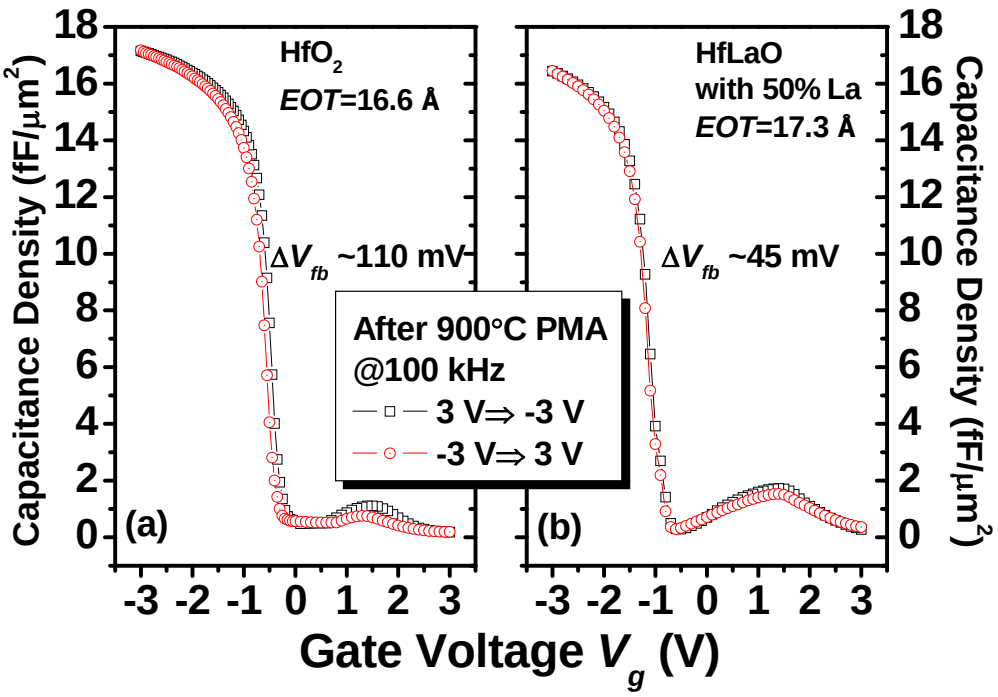


Fig. 3.5: Hysteresis of TaN/high-*k* stacks with HfO_2 (a) and HfLaO with 50% La (b) films after annealing at 900ºC for 30 s.

Figure 3.6 illustrates thermal stability by comparing the typical variation of *EOT* for HfO_2 and HfLaO with 15% and 50% La samples with TaN metal gate after different temperature PMA. It was observed that the annealing temperature has more impact on *EOT* variation for HfO_2 film than that for HfLaO films. This may be attributed to the fact that the amorphous HfLaO films effectively block oxygen diffusion through the grain boundaries to form low-*k* interfacial layer during high temperature annealing.

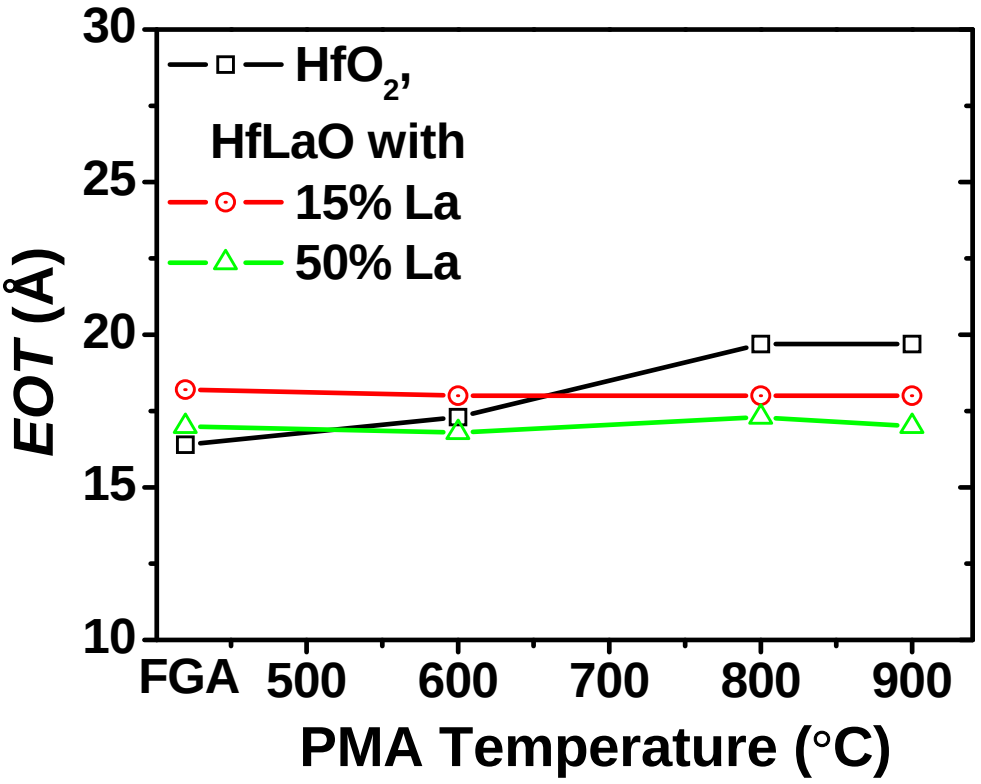


Fig. 3.6: *EOT* variation for MOS devices with TaN/high-*k* stacks as a function of PMA temperatures, which indicates HfLaO films have better thermal stability than HfO_2.

Based on the *EOT* data shown in **Fig. 3.6**, the equivalent dielectric permittivities of HfLaO + interfacial layer (IL) films with 15% and 50% La after 900°C PMA are subsequently extracted from $k = \varepsilon_{SiO_2} t_{physical} / EOT$ (where ε_{SiO_2} is the permittivity of SiO_2 and $t_{physical}$ means the total physical thickness of high-*k* layer and interfacial layer, determined by ellipsometer or TEM) and summarized in **Fig. 3.7**. They show larger *k* values than that of HfO_2 + IL. This increase of the dielectric constant by incorporating La into HfO_2 is attributed to the higher *k* value of La_2O_3 (~30) compared to that of HfO_2 (~25).

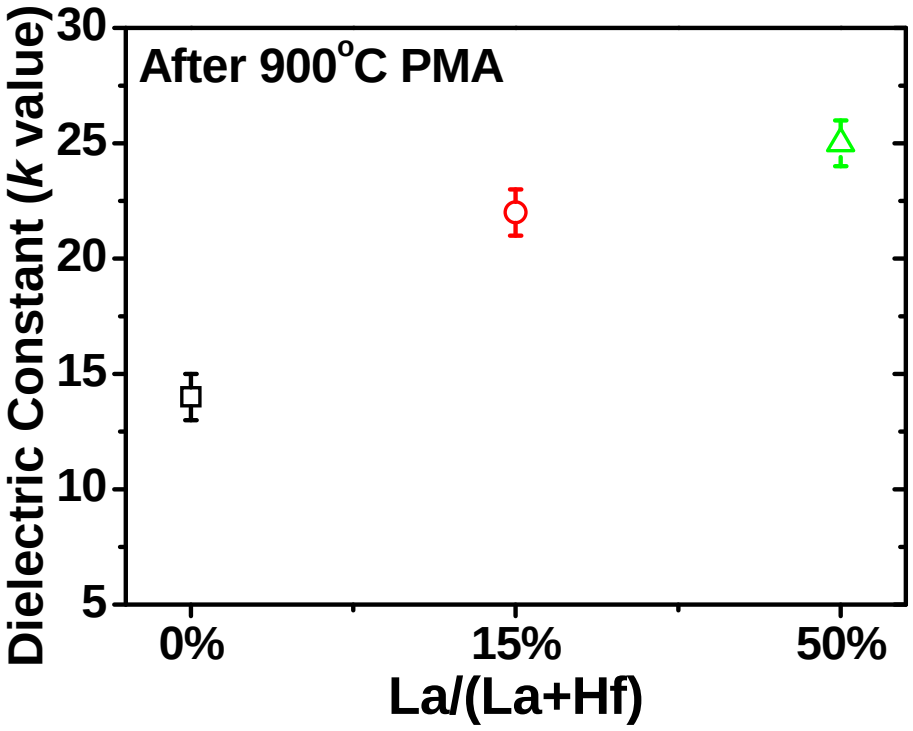


Fig. 3.7: Relationship between the dielectric constant and the concentration of La in HfLaO films.

3.3.2 Electrical Properties of HfLaO

Figure 3.8 shows that the gate leakage current densities of HfLaO films with 15% and 50% La are comparable to that of pure HfO_2 at the same EOT of ~1.2-1.8 nm. HfLaO films also exhibit approximately 5 orders of reduction in gate leakage current density when compared to a poly-Si/SiO_2 benchmark.

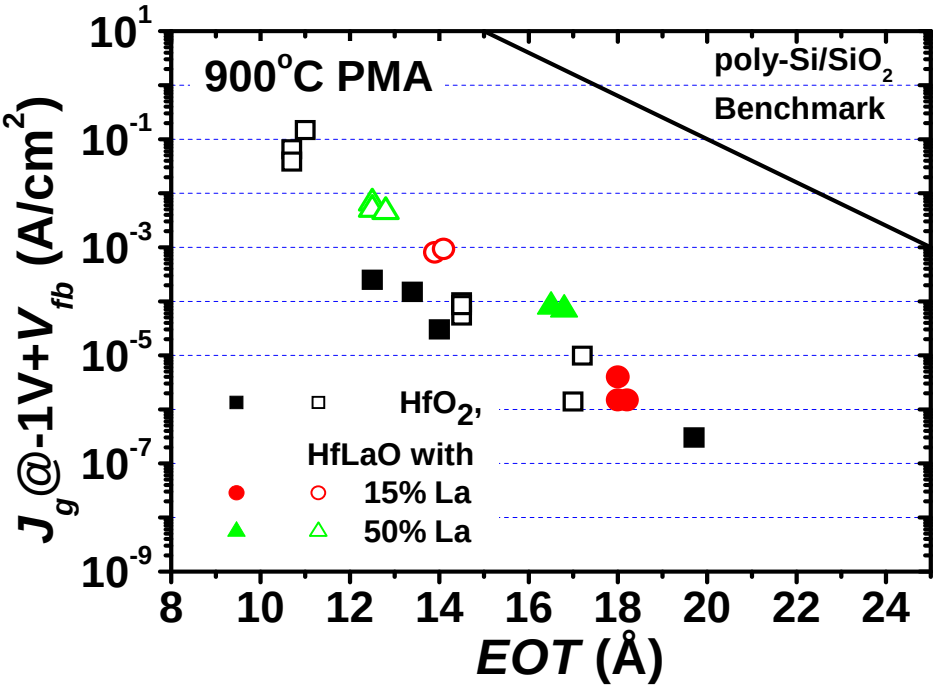


Fig. 3.8: The relationship between gate leakage current density and *EOT* for MOS devices with HfO_2, HfLaO with 15% and 50% La gate dielectrics and TaN (solid data point) or HfN (open data point) metal gate. Compared with poly-Si/SiO_2 benchmark at the same *EOT*, both HfO_2 and HfLaO provide ~5 orders reduction in gate leakage current.

In **Fig. 3.9**, the effective electron mobility is extracted for both HfO_2 and HfLaO devices using a standard split *C-V* technique. It is obvious that the electron mobility for n-MOSFETs fabricated with HfO_2 improves by approximately ~70% with the incorporation of La. The incorporation of La is believed to reduce remote phonon scattering and increase the electron channel mobility due to the modification of the atomic bonding and the low energy phonon spectra of HfO_2 as observed in the FTIR spectra [17]. The observed mobility increment is also ascribed partially to the formation of a thick (as shown in **Fig. 3.3**) and high quality HfLaO/Si-substrate interfacial layer.

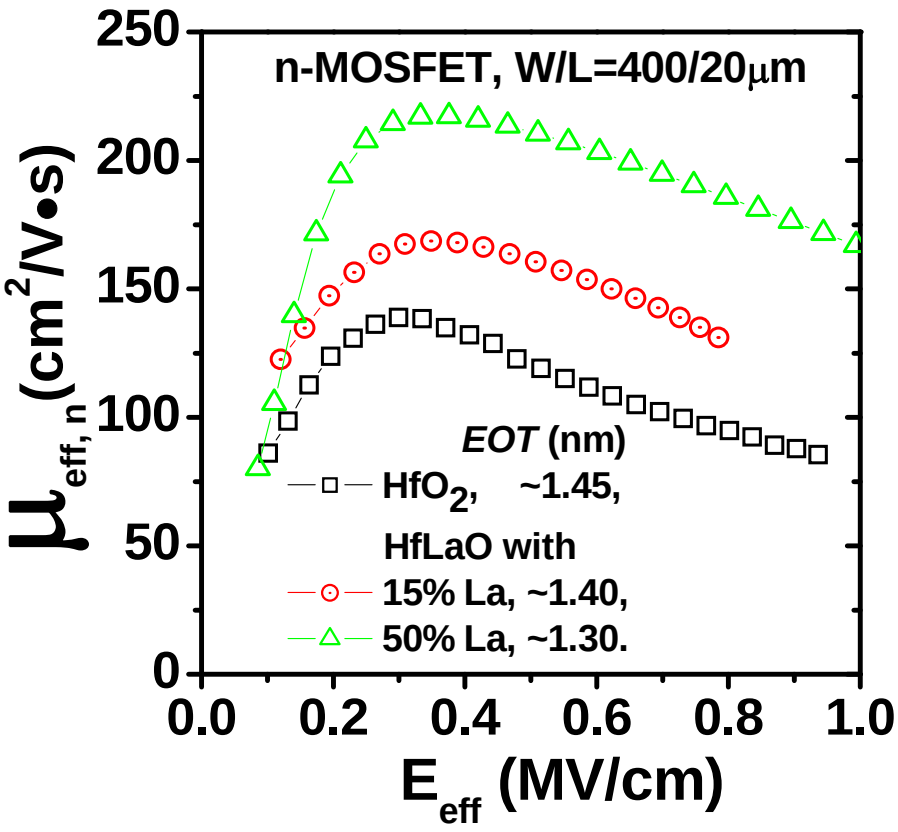


Fig. 3.9: Effective electron mobility of HfO_2, HfLaO with 15% and 50% La gate dielectric n-MOSFETs after activation at 900°C for 30 s extracted by split *C-V* method.

In addition, the output characteristics (I_d-V_d) of n-MOSFETs fabricated with HfO_2 and HfLaO with 15% and 50% La after activation at 900°C for 30 s are shown in **Fig. 3.10**. Scaling to the same *EOT*, I_d also has ~70% improvement when using HfLaO with 50% La to replace HfO_2 as gate dielectric, which should be attributed to the increase of electron mobility in the channel region, as shown in **Fig. 3.9**.

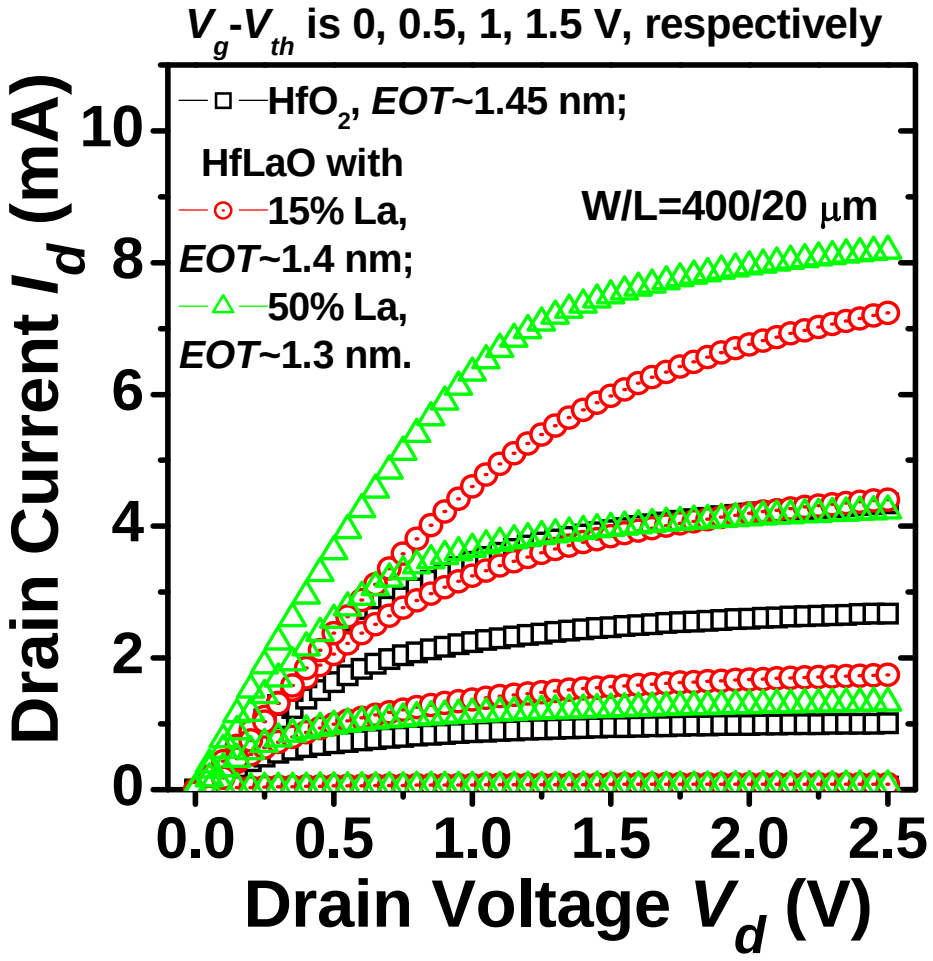


Fig. 3.10: I_d-V_d characteristics of n-MOSFETs with HfO_2, HfLaO with 15% and 50% La gate dielectrics. I_d is observed to increase with increasing concentration of La at the same gate overdrive.

A comparison of the threshold voltage (V_{th}) shift under constant voltage stress in HfO_2 and HfLaO films is shown in **Fig. 3.11**. The observation of one order reduction of V_{th} shift for HfLaO with 50% La compared to HfO_2 implies that the incorporation of La into HfO_2 also suppresses charge trapping in the dielectric. The reliability issue concerning the charge trapping induced V_{th} instability will be further discussed in **Chapter 5**.

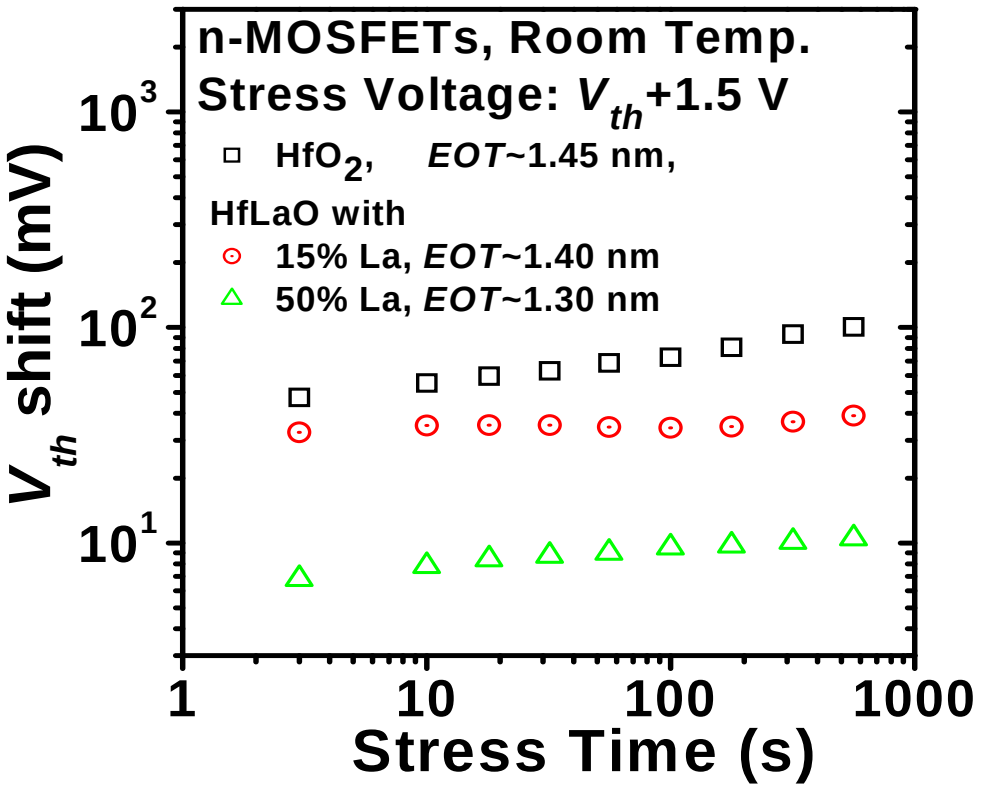


Fig. 3.11: Charge trapping induced V_{th} shift under constant voltage stress in HfO_2, HfLaO with 15% and 50% La gate dielectric n-MOSFETs.

3.3.3 Work Function Tunability by Employing HfLaO

Figure 3.12 shows the typical *C-V* curves (after normalization) of MOS capacitors with TaN and Pt metal gates on either HfO_2 or HfLaO (with different La concentration). It should be mentioned that the incorporation of La in HfO_2 improves the thermal stability of the gate stack with Pt electrode from less than 600°C [20] to 1000°C, probably due to the release of stress between Pt and HfO_2 after La incorporation. More importantly, significant V_{fb} shifts can also be observed after the incorporation of La into HfO_2 for both n- and p-MOS devices, which are very suitable for bulk-Si CMOSFET application.

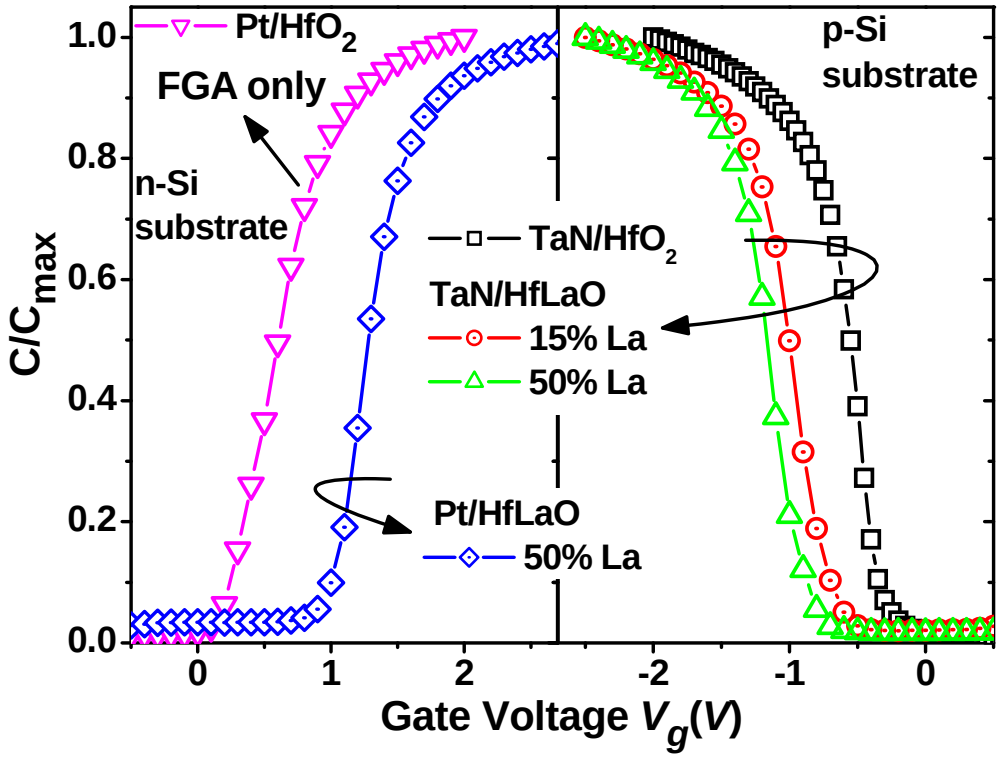
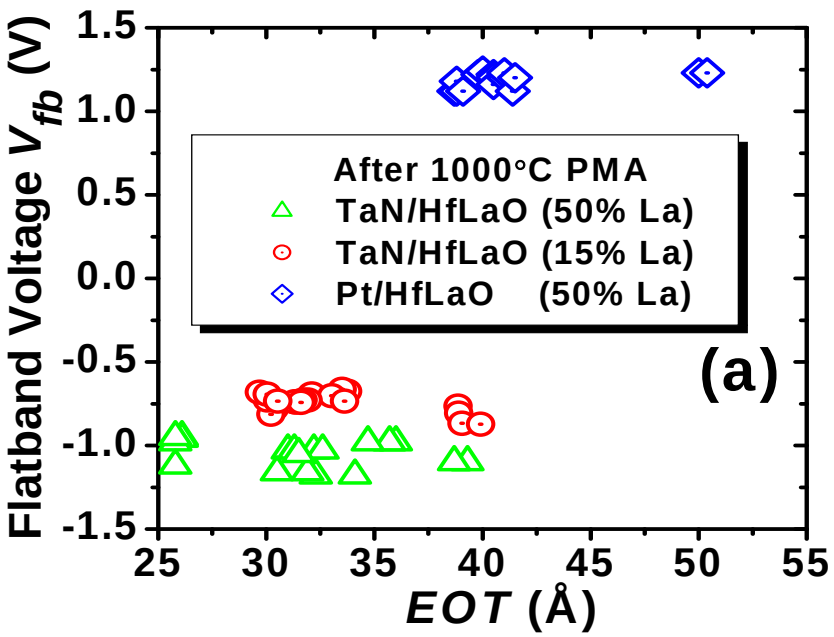


Fig. 3.12: Comparison of typical *C-V* curves for MOS HfLaO capacitors with different La concentration (including 50%, 15% and 0 %) after 1000ºC PMA. Obvious V_{fb} shift can be seen after La incorporation for both n- and p-MOS devices.

To further clarify the origin of this V_{fb} shift, MOS capacitors with different dielectric thickness were fabricated. V_{fb} was then extracted from the *C-V* curves and plotted as a function of *EOT* for the HfLaO films as shown in **Fig. 3.13(a)**. It is obvious that for a fixed La concentration, the V_{fb} shift remains almost constant with *EOT* variations. This indicates low charge density near the HfLaO interface with the channel. In addition, it is unlikely that the difference of fixed charge in HfLaO near the TaN gate would be large enough from that under Pt gate to explain the observed difference in V_{fb} shifts. Therefore the observed V_{fb} shifts for HfLaO films cannot be attributed entirely to the presence of oxide charges, but to a modification of the effective metal gate work function. By assuming that dielectric charge effects are negligible for the films investigated, work functions for TaN and Pt on HfLaO film can be accurately extracted and are summarized in **Fig. 3.13(b)**. It can be seen that the

EWF of TaN shifts to more n-type with the increase of La% in HfLaO, up to conduction band edge (E_C). In the case of 50% La in HfLaO film, the EWFs of TaN and Pt are approximately 3.9 eV and 5.5 eV respectively, which are sufficient to meet the work function requirements for both n- and p-MOSFETs. From the FTIR measurements, we have found that the incorporated La atoms in HfO_2 distort the monoclinic structure of HfO_2 due to the different bonding properties of La in terms of ionicity or coordination number. This change in dielectric structure and atomic bonds is postulated to change the energy of the interface states between HfLaO and the MGs. This causes a change in the FLP effect and modifies the EWF of TaN and Pt.



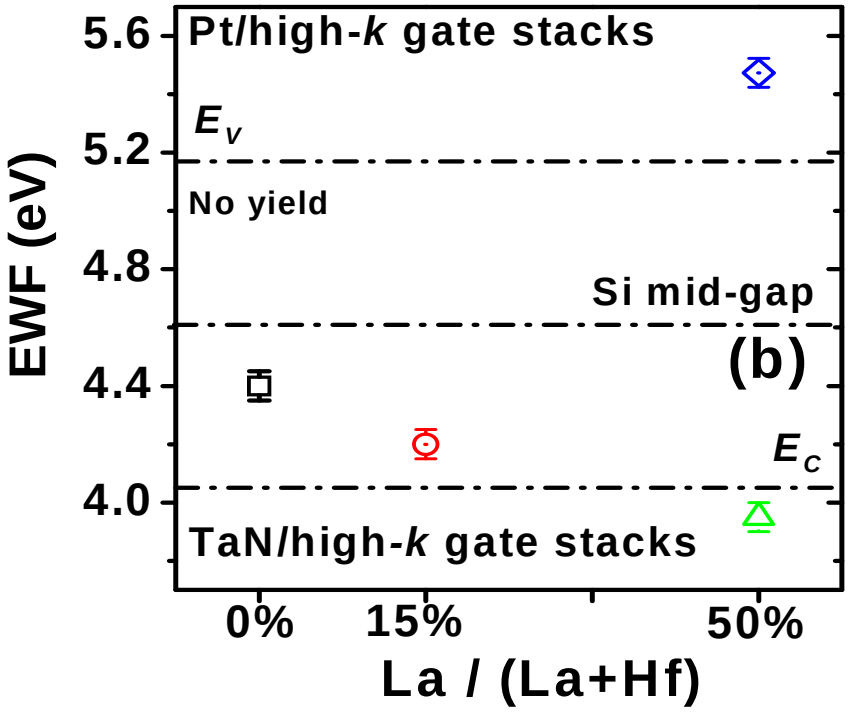


Fig. 3.13: V_{fb} as a function of *EOT* (a) and the corresponding metal EWF as a function of La concentration in HfLaO films (b). Based on the V_{fb} values on $6x10^{15}$ cm^{-3} n- and p- doped Si, corresponding EWFs of around 5.5 eV for Pt and around ~3.9 eV for TaN on HfLaO with 50% La are extracted, neglecting the very weak dielectric charge effect.

In **Fig. 3.14**, MOSFETs with the same gate stacks mentioned in **Fig. 3.12** were also fabricated and their transfer characteristics are shown. The V_{th} values for all devices are consistent with the EWF values obtained in **Fig. 3.13(b)**, indicating that the wide V_{fb} and V_{th} tunability for these gate stacks stems from the modulation of the metal gate EWF.

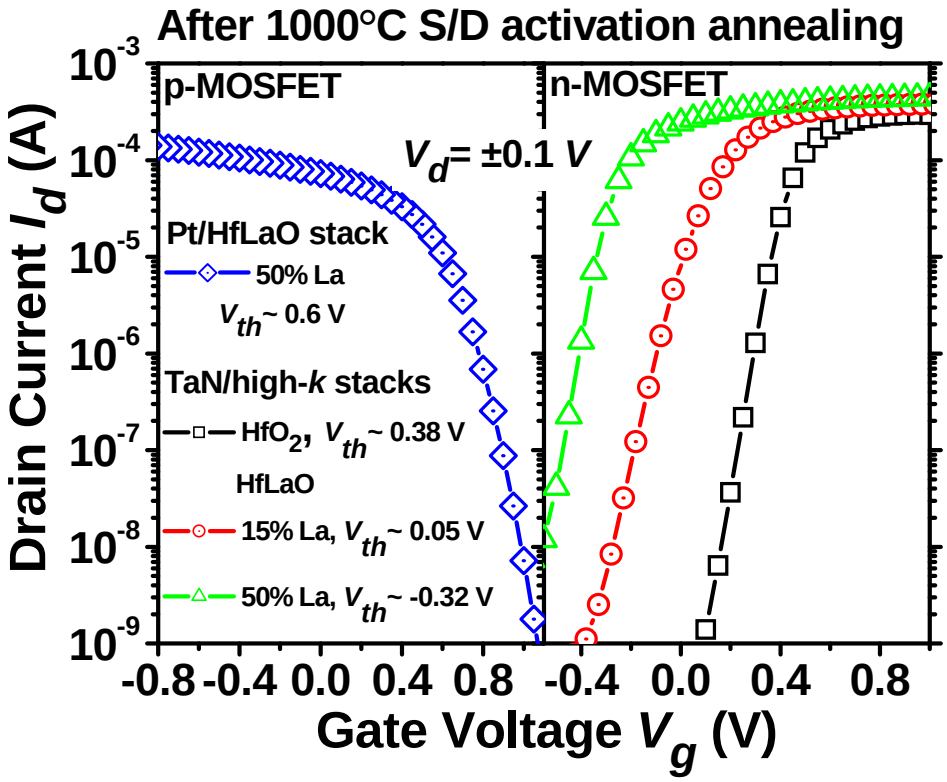


Fig. 3.14: Transfer characteristics (I_d-V_g) of MOSFETs with TaN (for n-MOSFET) and Pt (for p-MOSFET) on HfO_2 and HfLaO (with 15% and 50% La) gate dielectrics.

3.3.4 Mechanism Investigation for the EWF Tunability

When MGs and high-*k* dielectrics are placed in contact, especially during high temperature treatments, MG/high-*k* interface states would be created and generally charge transfer could occur across these interface states at the dielectric side and the metal electrode side, leading to the formation of a dipole layer and Fermi level pinning of EWF [9,21]. As discussed in **Chapter 2**, two models taking into account the role of intrinsic states and extrinsic states at MG/high-*k* dielectric interfaces respectively were proposed to explain the instability of the metal EWF. However, the knowledge on this crucial interface is still insufficient to guide us in choosing the right MG/high-*k* gate stacks for device integration, especially for conventional bulk-Si CMOSFETs. Based on the previous data in this chapter, two additional effects which

influence the charge transfer, causing release or partial release of FLP of Φ_{eff} are considered.

The first effect is charge transfer due to electronegativity of the materials, which is the tendency of an atom in a molecule to attract electrons to it. When atoms react with each other, they will compete for the electrons involved in a chemical bond. The atom with the higher electronegativity value will always "pull" the electrons away from atom that has the lower electronegativity value. The degree of "movement or shift" of these electrons toward the more electronegative atom is dependent on the difference in electronegativities between the atoms involved. Generally, there are three trends for electronegativity values of elements in the Periodic Table as shown in **Table 3.1** [22]:

(1) Metals generally have low electronegativity values, while nonmetals have relatively high electronegativity values;
(2) Electronegativity values generally increase from left to right within the Periodic Table;
(3) Electronegativity values generally decrease from top to bottom within each family of elements in the Periodic Table.

La is known to have an electronegativity of 1.1 on the Pauling scale, which is lower than those of Hf (1.3) and Ta (1.5). Therefore, for the case of TaN gate, additional electrons transfer from HfO_2 to TaN through the dipole layer would be expected when La atoms replace Hf atoms near to the interface, due to the lower electronegativity of La atoms. This effect will compensate the original electrons transfer from TaN to HfO_2 due to FLP, giving rise to partial release of FLP and reduction of Φ_{eff} of TaN. The corresponding energy band diagram for this case is schematically shown in **Fig. 3.15(a)**.

Table 3.1: Periodic Table of electronegativity using the Pauling scale [22].

IA	IIA	IIIB	IVB	VB	VIB	VIIB	VIIIB	VIIIB	VIIIB	IB	IIB	IIIA	IVA	VA	VIA	VIIA	VIIIA
1																	2
H																	He
2.20					Key:												
3	4				Atomic number							5	6	7	8	9	10
Li	Be				Symbol							B	C	N	O	F	Ne
0.98	*1.57*				*Electronegativity*							*2.04*	*2.55*	*3.04*	*3.44*	*3.98*	
11	12											13	14	15	16	17	18
Na	Mg											Al	Si	P	S	Cl	Ar
0.93	*1.31*											*1.61*	*1.9*	*2.19*	*2.58*	*3.16*	
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
0.82	*1.00*	*1.36*	*1.54*	*1.63*	*1.66*	*1.55*	*1.83*	*1.88*	*1.91*	*1.90*	*1.65*	*1.81*	*2.01*	*2.18*	*2.55*	*2.96*	*3.00*
37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
0.82	*0.95*	*1.22*	*1.33*	*1.6*	*2.16*	*1.9*	*2.2*	*2.28*	*2.20*	*1.93*	*1.69*	*1.78*	*1.96*	*2.05*	*2.1*	*2.66*	*2.6*
55	56	57	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86
Cs	Ba	La*	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
0.79	*0.89*	*1.1*	*1.3*	*1.5*	*2.36*	*1.9*	*2.2*	*2.20*	*2.28*	*2.54*	*2.00*	*1.62*	*2.33*	*2.02*	*2.0*	*2.2*	
87	88	89	104	105	106	107	108	109	110	111							
Fr	Ra	Ac**	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg							
0.7	*0.9*	*1.1*															
La*		58	59	60	61	62	63	64	65	66	67	68	69	70	71		
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu		
		1.12	*1.13*	*1.14*	*1.13*	*1.17*	*1.2*	*1.2*	*1.1*	*1.22*	*1.23*	*1.24*	*1.25*	*1.1*	*1.27*		
Ac**		90	91	92	93	94	95	96	97	98	99	100	101	102	103		
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr		
		1.3	*1.5*	*1.38*	*1.36*	*1.28*	*1.13*	*1.28*	*1.3*	*1.3*	*1.3*	*1.3*	*1.3*	*1.3*	*1.3*		

In the case of p-type MGs, electron transfer from La to Pt due to low electronegativity of La would not be feasible because Pt, as a noble metal, generally shows intrinsically inert performances. However a second effect should be considered. Oxygen vacancies (V_O) creation in a dielectric are believed to induce the electron transfer from V_O to gate electrode, which would lead to a reduction of Φ_{eff} of p-type MGs, such as Pt [20]. In addition, it is reported that the presence of V_O can serve as a trapping center [23], and the increase of V_O density will enhance the charge trapping effect, which will deteriorate the V_{th} instability and degrade the channel mobility as a result. Therefore, in this work, we have estimated the V_O density ratio for HfLaO to HfO_2 by Vienna *ab-initio* simulation package (VASP). **Table 3.2** shows the first-principles calculation results of V_O formation using monoclinic HfO_2 [24] and pyrochlore $Hf_2La_2O_7$ [25] configurations by VASP, where the monoclinic HfO_2 (m-HfO_2) primitive cell without and with possible V_O are shown in **Fig. 3.16**, while the pyrochlore $Hf_2La_2O_7$ (p-$Hf_2La_2O_7$) without and with possible V_O are shown in **Fig.**

3.17. Based on **Table 3.2**, the V_O density ratio between $Hf_2La_2O_7$ and HfO_2 with the same volume was estimated to be 0.2 by the equation below:

$$Ratio = \frac{D_{Td}\exp[-\frac{E_{Td}-E_{V4}}{k_BT}]+D_{C2v}\exp[-\frac{E_{c2v}-E_{v4}}{k_BT}]}{D_{v3}\exp[-\frac{E_{v3}-E_{v4}}{k_BT}]+D_{v4}} \quad (3\text{-}1)$$

where *D* and *E* stand for density and formation energy for different oxygen vacancy sites, including v3, v4 in m-HfO2 and Td, C2v in p-HfLaO.

By considering the non-fully thermal equilibrium under PMA annealing, the difference between the real amorphous phase and simulated crystal phase, the calculated ratio of 0.2 gives a reasonable explanation of reduction of V_{th} shift under constant voltage stress and improvement of electron channel mobility for HfLaO device compared to those for HfO_2, as shown in **Fig. 3.9 & 3.11**. In addition, the lower V_O density in HfLaO also leads to the decrease in the amount of electron transfer induced by V_O for gate stacks with HfLaO dielectric compared to those with HfO_2 and the partial release of FLP between HfO_2 and Pt. The corresponding energy band diagram for this case is schematically shown in **Fig. 3.15(b)**.

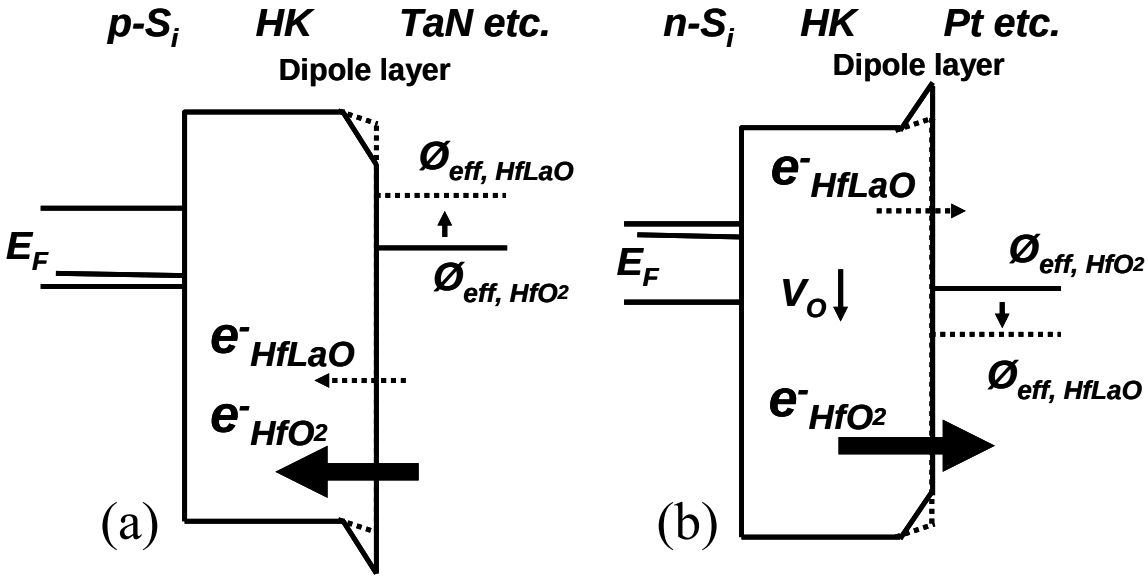
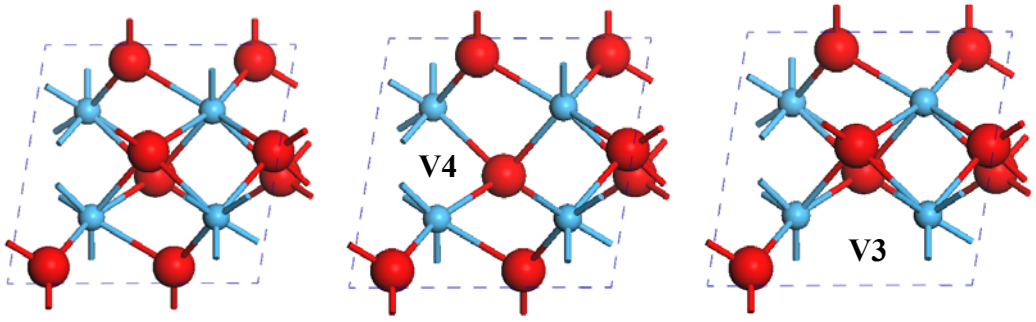


Fig. 3.15: Energy band diagram for MG/high-*k* gate stacks. The dashed (solid) lines indicate the case whereby HfLaO (HfO_2) is used as the gate dielectric. The subscripts of Φ_{eff} and e^- (HfLaO and HfO_2) represent Φ_{eff} of MGs and

electron transfer for HfLaO and HfO_2 case, respectively. The amount and direction of net electron transfer are indicated by horizontal arrows. (a) For n-MOS device with TaN/HfO_2 gate stack, electron transfer from TaN to HfO_2 due to FLP shifts the Φ_{eff} to midgap [21]. In the case of TaN/HfLaO gate stack, additional electron transfer from HfLaO to TaN would be expected due to the lower electronegativity of La atoms. This effect compensates the electron transfer from TaN to HfO_2 due to FLP, giving rise to the reduction of TaN's Φ_{eff}. (b) For p-MOS device with Pt gate, V_O in a dielectric are believed to induce electron transfer from V_O to MG, which would lead to FLP and reduction of the MG's Φ_{eff} [20]. When La atoms replace Hf atoms, V_O concentration is reduced. This leads to the reduction of the amount of electron transfer and the release of FLP, increasing the Φ_{eff} of MG.

Table 3.2: The formation energies of V_O at varies sites in m-HfO_2 and p-$Hf_2La_2O_7$ (as shown in **Fig. 3.16 & 3.17**), calculated by first-principles calculations using VASP software.

Oxygen vacancy site	Formation energy	Site density
	E (*eV*)	*D* (nm^{-3})
V3 site in m-HfO_2	6.51	28.6
V4 site in m-HfO_2	6.39	28.6
Td site in p-$Hf_2La_2O_7$	7.23	6.3
C_{2V} site in p-$Hf_2La_2O_7$	6.51	38.0



Dark (red color) balls – oxygen atoms;

Shallow (blue color) balls – Hf atoms.

Fig. 3.16: (a) M-HfO_2 primitive cell without V_O. (b) & (c) Two possible V_O sites in m-HfO_2: V4 (4-fold coordinated site) and V3 (3-fold coordinated site).

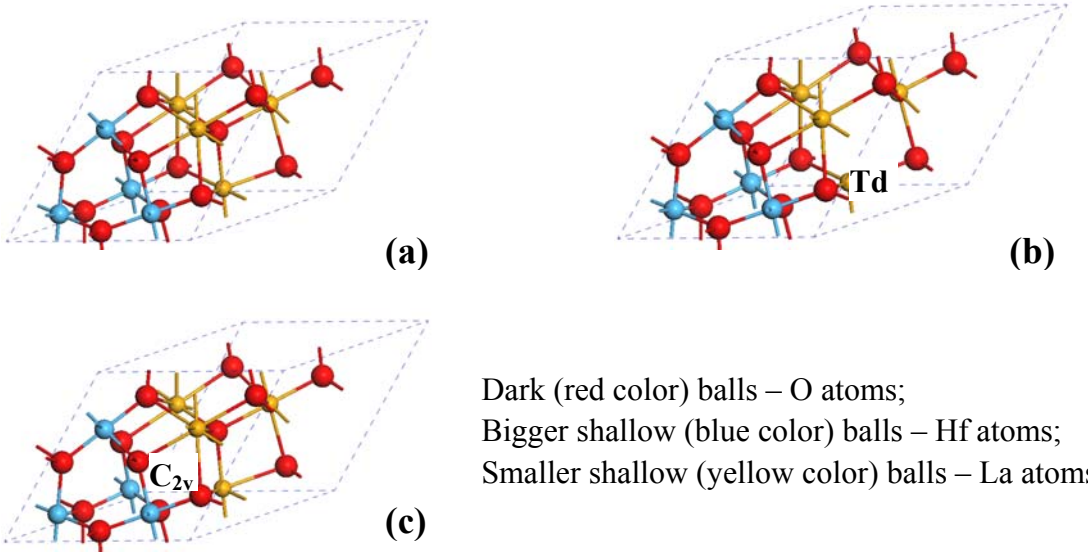


Fig. 3.17: (a) P-$Hf_2La_2O_7$ primitive cell without V_O. (b) & (c) Two possible V_O sites in p- $Hf_2La_2O_7$: Td symmetry site and C_{2V} symmetry site.

In short, the change of MG's Φ_{eff} is attributed to not only V_O density in dielectric layer, but also the difference of electronegativities among materials involved in gate stacks. Moreover, it seems the effect of V_O is more obvious for p-type noble metals and the effect caused by electronegativity differences is more obvious for n-type MGs. To check this specific model based on the interfacial dipole theory, MOS devices with more MG/high-*k* gate stacks were also fabricated using the similar process flow as described in the experiment part and some key results will be presented in the following section.

3.3.5 Electrical Properties for More Lanthanide Elements Incorporated HfO_2

First, we investigate MOS devices with another noble metal, Ru and HfLaO dielectric with 50% La. **Figure 3.18** shows the typical normalized *C*-*V* curves of TaN/Ru/high-*k* capacitors with HfO_2 and HfLaO (50% La), respectively. An obvious positive V_{fb} shift of 600 mV was seen after the incorporation of La into HfO_2. Moreover, negligible frequency dispersion among 10 kHz, 100 kHz and 1 MHz and <50 mV hysteresis of the HfLaO with 50% La are shown in **Fig. 3.19**, where the hysteresis was quantified by the difference in V_{fb} during the voltage sweeps without

delay time between ±3 V. These results indicate that the interface traps and/or oxide traps may be significantly reduced by incorporation of La into HfO_2 and cannot respond at high frequency [26], which is consistent with the previous result as shown in **Fig. 3.5**.

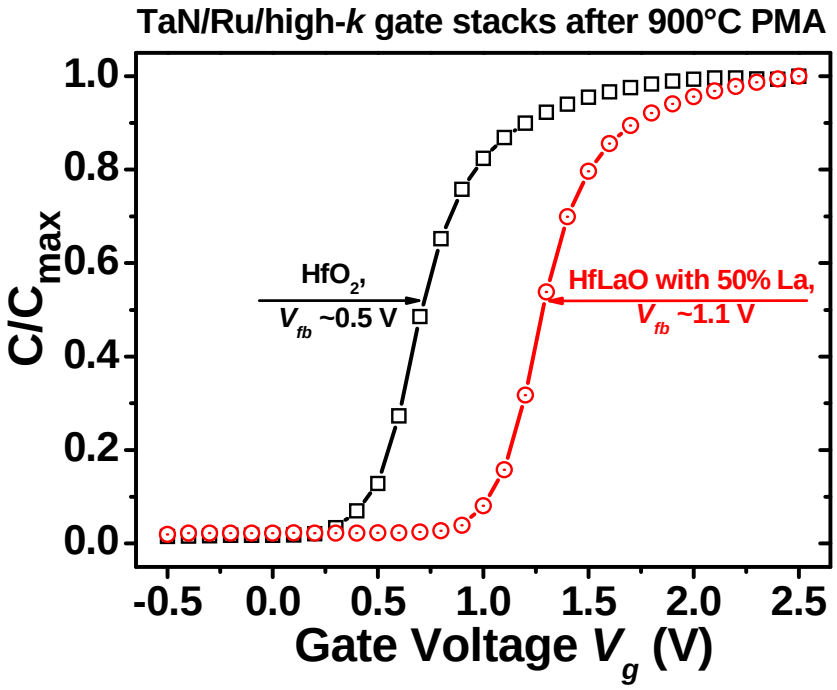


Fig. 3.18: Comparison of typical normalized *C*-*V* curves for MOS capacitors with HfO_2 and HfLaO (50% La) dielectrics after 900ºC PMA. Obvious V_{fb} shift can be seen after La incorporation.

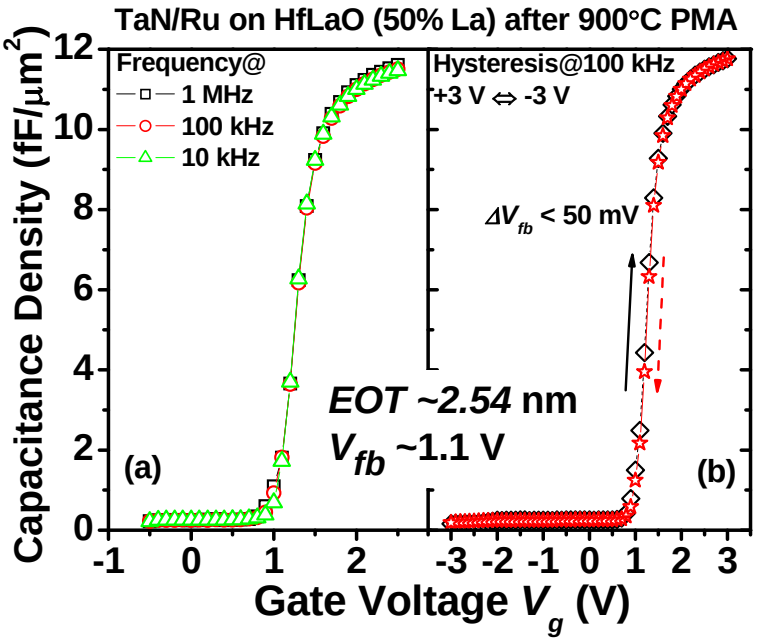


Fig. 3.19: (a) Frequency dispersion of the HfLaO with 50% La among 10 kHz, 100 kHz and 1 MHz. (b) Hysteresis of HfLaO film with 50% La after annealing at 900ºC for 30 s.

To investigate the origin of this significant V_{fb} shift, MOS capacitors with pure Ru and HfLaO (50%) gate stacks with different dielectric thicknesses were also fabricated and all devices were annealed at 1000°C, which is required by a conventional CMOS source/drain activation process. V_{fb} values and *EOT* extracted from these MOS capacitors are summarized in **Fig. 3.20**, which shows that the shift of V_{fb} for HfLaO dielectric is not mainly caused by fixed charges in the dielectric film, but by the change of Ru's EWF compared to HfO_2 case. Based on **Equation (2-2)**, the EWF of Ru on HfLaO with 50% La around 5.2 eV can be extracted, which is very close to the EWF value extracted from pure Ru on SiO_2 gate stack [27]. Just as discussed previously, the FLP between Ru and HfO_2 dielectric may be released due to the incorporation of La into HfO_2 followed by the reduction of V_O.

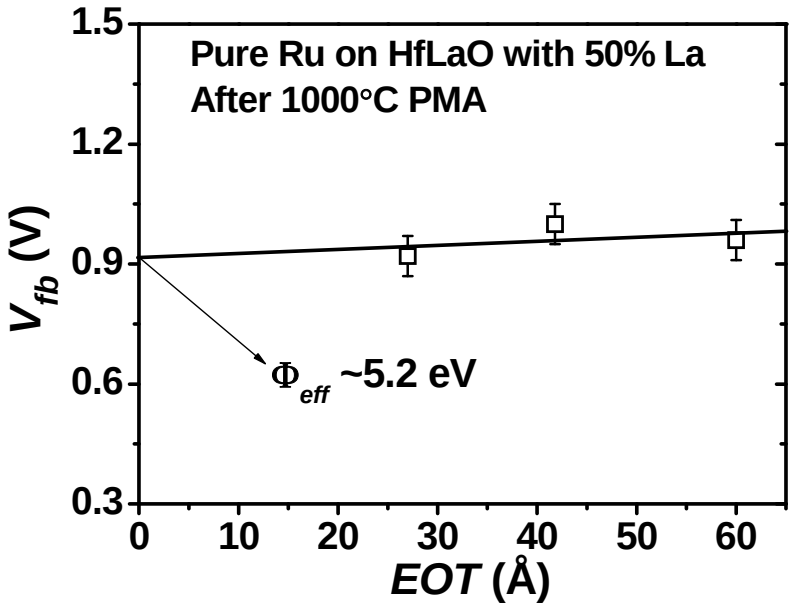


Fig. 3.20: The plot of V_{fb} versus *EOT* for devices with pure Ru metal on HfLaO dielectric on n-Si substrate ($6x10^{15}$ cm^{-3} n-doped) after 1000ºC PMA. Both V_{fb} and *EOT* were extracted from high-frequency *C-V* measurement (100 kHz). The corresponding EWF of Ru on HfLaO (50% La) is ~5.2 eV.

In addition to this p-type metal, n-type metals were also investigated on the HfLaO with different La concentrations and thicknesses using the same method, and these include TaN, HfN and TiN. The extracted EWF for these gate stacks together with previous results are summarized in **Fig. 3.21**. Similar to the case of TaN, both HfN and TiN show obvious EWF shift towards the conduction band edge with the incorporation of La into HfO_2. The electronegativities of Hf atom and Ti atom on the Pauling scale are 1.3 and 1.54 respectively, higher than that of La (1.1). Therefore, these results may provide some support for the previous model, i.e. the effect of electronegativity difference between MG and gate dielectric on EWF is more obvious for n-type MGs. Also, it can be seen from **Fig. 3.21** that both conduction and valence band edge EWFs after high temperature annealing (1000°C) can be obtained on the HfLaO (50% La) film, which are very suitable for bulk-Si CMOS technology.

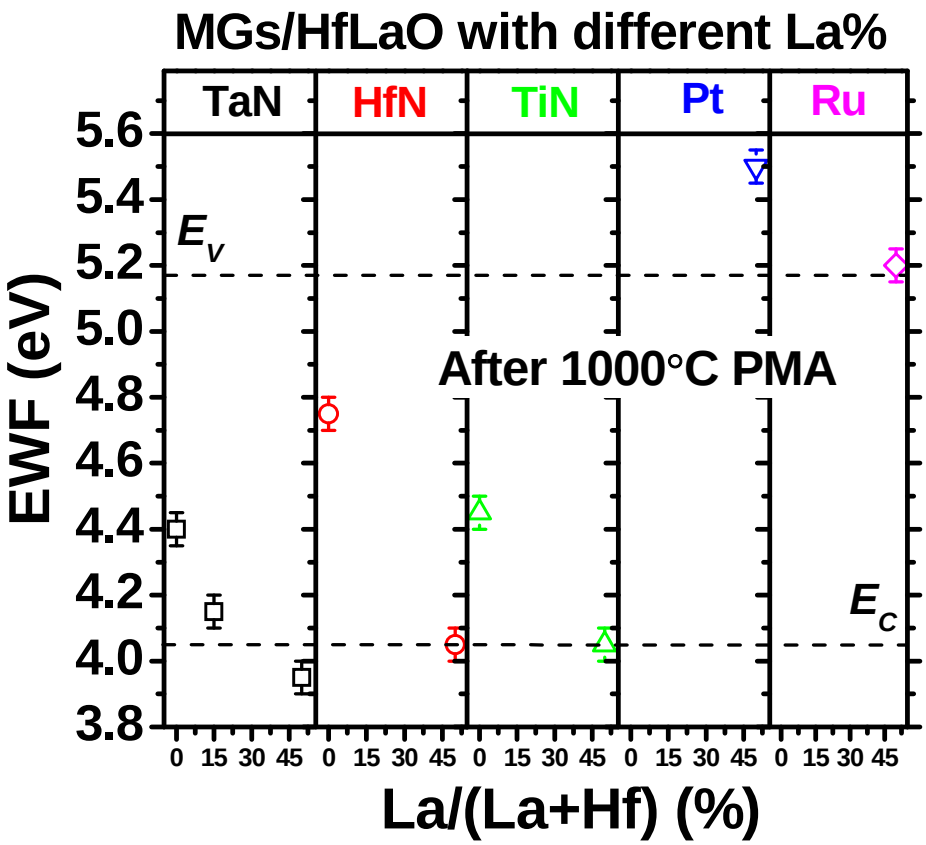


Fig. 3.21: The extracted EWF of MGs on HfLaO dielectric films with different La concentration (0%, 15% or 50%).

To confirm the effect of electronegativity on EWF values for n-type MGs, more elements with low electronegativities were incorporated into HfO_2 as gate dielectrics, including Tb (1.1), Dy (1.22), Yb (1.1) and Er (1.24). All of them are lanthanide elements, with similar physical and chemical properties to La. Normalized *C-V* curves for MOS capacitors with these dielectrics and TaN gate electrode are summarized in **Fig. 3.22**. With the incorporation of these lanthanide elements (~30% concentration) with low electronegativities, V_{fb} for TaN/HfO_2 gate stack obviously shifts negatively (~250 mV). To account for these V_{fb} shifts with this kind of gate stacks, the case of HfErO was investigated systematically.

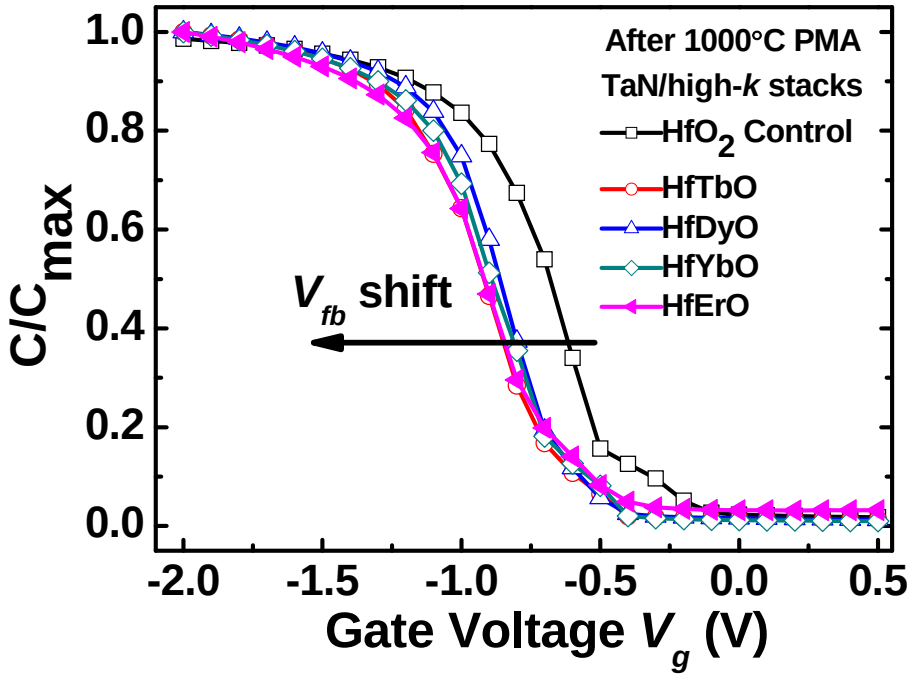


Fig. 3.22: Normalized *C-V* curves for MOS capacitors with TaN/high-k gate stacks after 1000°C PMA, where high-k dielectrics include HfO_2, HfTbO, HfDyO, HfYbO and HfErO.

Fig. 3.23(a) shows the negligible frequency dispersion among 10 kHz, 100 kHz and 1 MHz *C-V* characteristics, which indicates that the low interface trap density in the HfErO gate dielectric is unable to respond to high frequency [26]. **Fig. 3.23(b)** shows a slightly larger hysteresis (~95 mV) for HfErO film (with 30% Er) after activation annealing at 1000ºC for 5 s. The hysteresis was quantified by the difference in V_{fb} during the voltage sweeps without delay time between ±3 V. To rule out the possible reason for V_{fb} shift from oxide charges in HfErO film, MOS capacitors with different HfO_2 and HfErO thicknesses were fabricated. V_{fb} values and *EOT* extracted from *C-V* curves are summarized in **Fig. 3.24**. It can be seen even though oxide charges in the HfErO film have some effect on V_{fb} values, the lower slope (0.0030) and the extracted TaN's $\boldsymbol{\Phi}_{eff}$ (~4.1 eV) indicate the V_{fb} shift compared to HfO_2 case (slope ~0.0065, $\boldsymbol{\Phi}_{eff}$ ~4.4 eV) is not purely due to the oxide charges in HfErO film, but the change of TaN's $\boldsymbol{\Phi}_{eff}$.

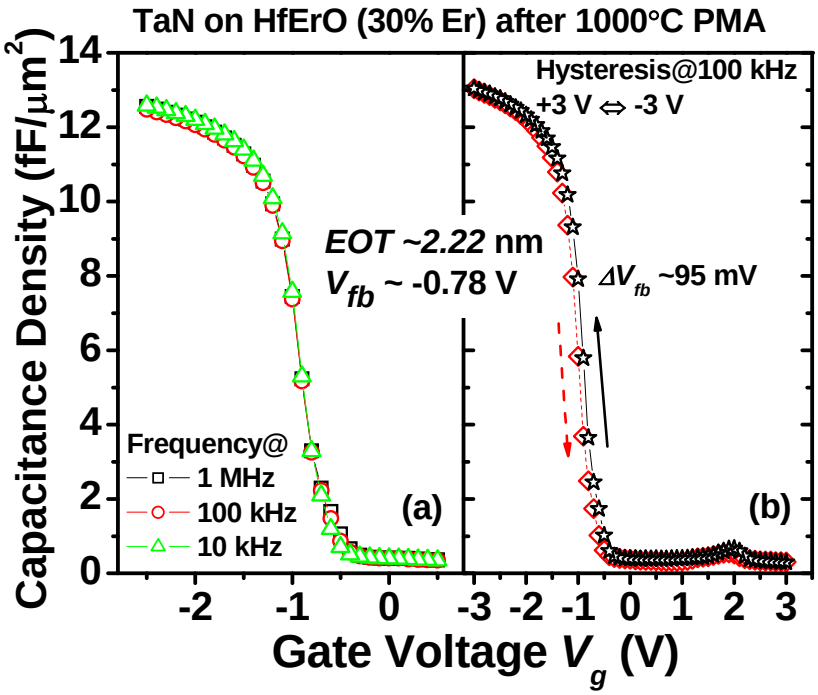


Fig. 3.23: (a) Frequency dispersion of the HfErO with 30% Er among 10 kHz, 100 kHz and 1 MHz. (b) Hysteresis of HfErO film with 30% Er after annealing at 1000ºC for 5 s.

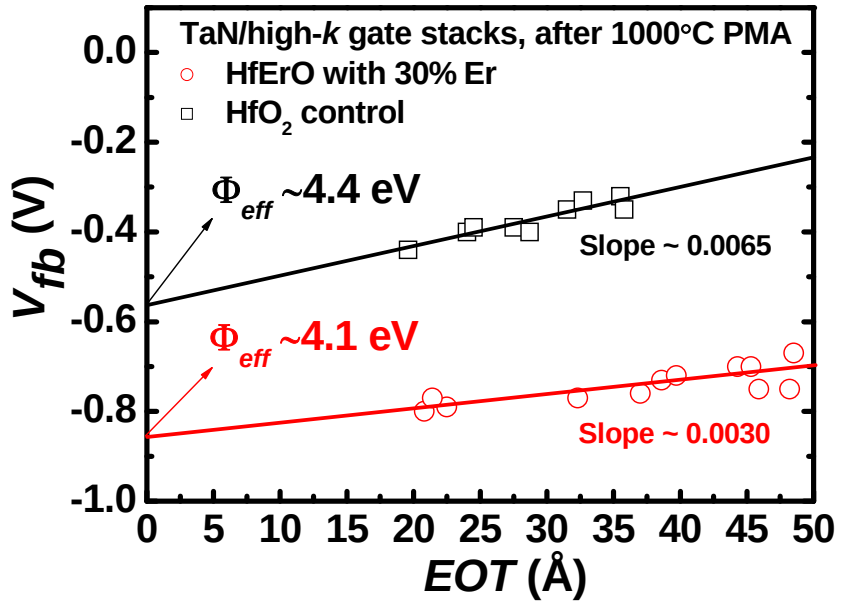


Fig. 3.24: The plot of V_{fb} versus *EOT* for devices with TaN metal on HfO_2 and HfErO dielectrics on p-Si substrate ($6x10^{15}$ cm^{-3} p-doped) after 1000ºC PMA. Both

V_{fb} and *EOT* were extracted from high-frequency *C-V* measurement (100 kHz). The corresponding EWF of TaN is ~4.4 eV on HfO_2 and ~4.1 eV on HfErO (30% Er).

Till now, all of above-mentioned results agree with the proposed model very well, therefore, this specific model based on the interfacial dipole theory between MGs and high-*k* dielectrics may provide an additional practical guideline for choosing appropriate gate stacks (MG + high-*k* dielectric) to meet the requirements of future CMOS devices.

3.4 Conclusion

In summary, gate dielectric material HfLaO was investigated systematically for the first time. By incorporating La into HfO_2 film, the crystallization temperature and *k* value of the film are increased substantially, and better thermal stability subsequently. N-MOSFETs fabricated with HfLaO exhibit superior device characteristics compared to n-MOSFETs fabricated with pure HfO_2, including an enhancement of ~70% for drive current and electron mobility and one order reduction of dielectric charge trapping induced V_{th} shift. We have also found the EWF of TaN (HfN or TiN) can be effectively tuned from Si mid-gap to the conduction band edge by optimizing the La composition in HfLaO to meet the n-MOSFET work function requirement. Simultaneously, the valence band edge EWF can be obtained by employing HfLaO and Pt (or Ru), which is very suitable for p-MOSFET. All these excellent properties observed in HfLaO gate dielectric suggest that it is a very promising candidate as the alternative gate dielectric for future CMOS application.

In addition, to interpret the significant EWF shift for both n- and p-type MGs, a specific model based on the interfacial dipole theory between gate electrode and dielectric is proposed, wherein the effects of different electronegativities among materials involved in the gate stack and V_O density in the dielectric film on the EWF of MGs are highlighted and it seems the effect caused by different electronegativities is more significant for n-type MGs and the effect of V_O is more obvious for p-type

noble metals. Experimentally, this model has been demonstrated by other gate stacks including more MGs and lanthanide elements incorporated HfO_2 dielectrics. Therefore, this model regarding the metal-dielectric interface could be useful for work function tuning and interface engineering of the MGs in future MOS devices.

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Chapter 4

Process Integration for Dual Metal Gate CMOS

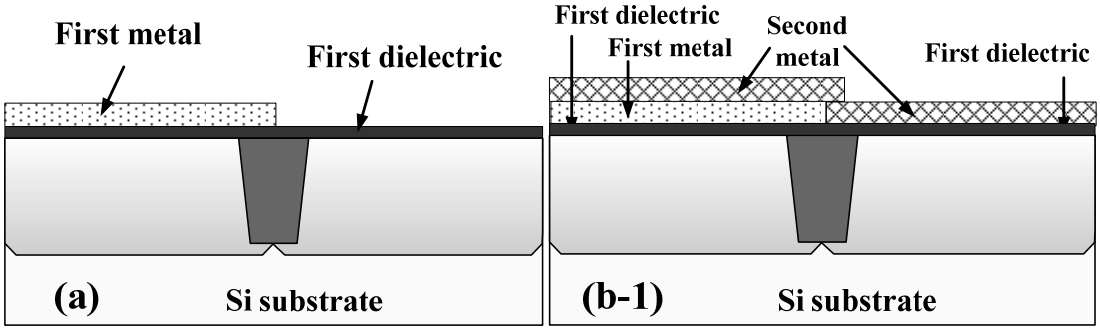
4.1 Introduction

As discussed in **Chapter 2**, metal gate (MG) technology would be required to replace conventional poly-Si gate in high performance (hp) 45 nm technology node and beyond. To achieve symmetric and lower threshold voltages (V_{th}) for both n- and p-MOSFETs, dual MGs with two different work functions (WFs), one for p-MOS and the other for n-MOS devices, will be needed because the V_{th} can be controlled by the WFs of MGs. Generally, an ideal dual MG integration process should possess dual WF values for n- and p-MOS respectively, and has no process-induced damages or reliability concerns for the gate oxide and minimal process complexity. However, integration of dual MGs into the CMOS process is still a major challenge for the development of MG technology. Next, let us review the existing dual MG integration processes and discuss the problems and concerns related to these processes. Based on these, we will further explore the motivation and innovations of two proposed integration schemes in this work subsequently.

The first demonstration of a dual MG CMOS integration process was reported by Lu and Yeo *et al.* [1,2]. The basic steps of this integration scheme are illustrated in **Fig. 4.1**. A first metal is deposited on the whole wafer first, followed by selective etching from one side (n-MOS or p-MOS). Next, a second metal with or without (w/o) a poly-Si capping layer is deposited, and finally it is the gate patterning and source/drain (S/D) formation. This approach is a gate-first integration scheme and in principle is applicable to any combination of metal candidates with good thermal stability, which has been further demonstrated by TiN-TaSiN, TaSiN-Ru, etc [3,4].

However, this approach exposes the gate dielectric to dry etch or wet etch ambient during the first metal etching back process. Dry etching of the first metal from the gate dielectric will easily cause a loss of gate dielectric, leading to different *EOT* for n- and p-MOS, as observed in [1]. While a wet etching process will be more gentle and safer for the gate dielectric, there are some reliability concerns because the gate dielectric is exposed to a series of wet chemicals during processing.

In order to avoid possible etching damage to the gate dielectric, a dual high-*k* (HK) dual MG integration process was proposed [5]. The basic idea of this process is to remove the first metal together with the underlying HK dielectric, or the first HK dielectric, during the metal etching process, and then deposit a new HK dielectric layer (second HK dielectric) and second metal material as a new gate stack, as illustrated in **Fig. 4.1**. By using this process, the final gate dielectric in either n-MOS or p-MOS region will not be exposed during the metal etching process, thus less reliability problem would be expected. An additional advantage of this integration scheme is that the metal gate/high-*k* stacks for n- and p-MOSFETs can be engineered independently to get optimized transistor characteristics. However, an additional lithography and chemical mechanical polishing (CMP) step is required in this scheme and thus the process complexity increases. In addition, the roughness or quality of original interfacial layer between HK film and Si substrate may be degraded to some extend during the etching process.



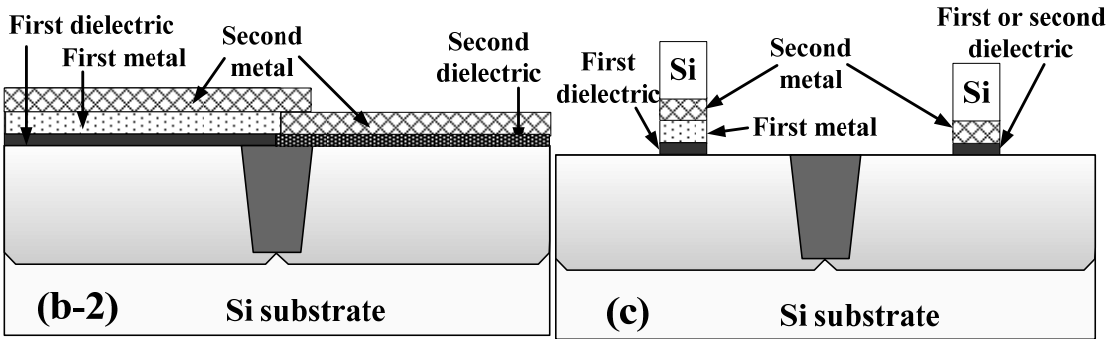


Fig. 4.1: Schematic process flow for dual MG integration by direct etching method. (a) First dielectric and first metal gate deposition, followed by selective etching of first metal from one side (n- or p-MOS); (b-1) Second metal deposition directly or (b-2) after selective removal of the first dielectric; (c) Poly-Si capping and gate patterning.

Another alternative approach in which dual MGs can be fabricated without exposing the gate dielectric to the etchant is the metal inter-diffusion approach [6]. In this approach, a thin layer of the first metal is deposited on top of the gate dielectric over the whole wafer. A second metal is then deposited on top of the first metal, which is removed in selected regions, as shown in **Fig. 4.2**. Because the first metal is the only metal remaining on the n-(or p-) MOS region, it will determine the V_{th} of the MOS transistor in this region. Subsequently, the remaining metals on the other MOS region are allowed to inter-diffuse. In some cases, the two metals will mix, yielding an intermediate gate WF, which can also be controlled by appropriate thickness compositions of the metal layers. In some extreme cases, the second metal can even segregate at the metal-dielectric interface and push the first metal atoms away from the interface. This approach has been applied to many metal combinations, such as Ru-Ta alloy [7], Ta-Pt alloy [8], Hf-Mo alloy [9], Hf-Ni alloy [10], Hf-Pt alloy [10], and even Mo-Si pair [11]. However, the concern of this approach is the thermal stability of the MG candidates, especially for n-type MGs. This suggests that the application of inter-diffusion approach is more suitable for the gate last process and may not be feasible for the conventional CMOS process because thermally stable metals will be required for subsequent thermal processing.

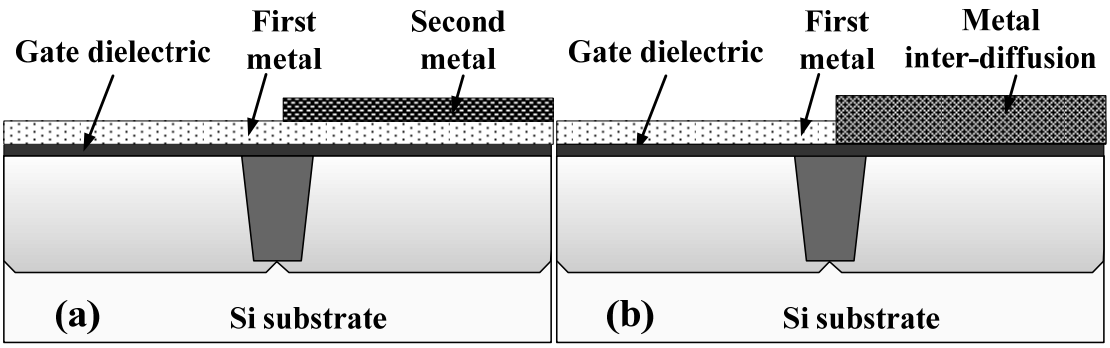


Fig. 4.2: Schematic illustration for dual MG CMOS technology by tuning WF with metal inter-diffusion. (a) Uniform dielectric, first metal and second metal deposition, followed by removal of the second metal on selected region; (b) The second metal can inter-diffuse with the underlying first metal or even segregate at the metal-dielectric interface and push the first metal atoms away from the interface during subsequent annealing processes.

Another example which does not require etching of the first-deposited layers, including gate dielectric layer and gate electrode layer, is the fully silicided (FUSI) silicide gate process, where the conventional poly-Si gate is used as the bottom protective layer [12,13]. The use of poly-Si as the bottom layer makes the FUSI process very attractive because of its compatibility with the conventional CMOS process flow. As illustrated in **Fig. 4.3**, a poly-Si gated CMOSFET is first fabricated using a conventional gate-first CMOS process. After S/D activation, a dielectric layer is deposited over the transistors. A CMP step is then performed to expose the poly-Si gate. After that, a metal film (pure metal, metal alloy or different metal materials for n- and p-MOS regions) is deposited over the exposed poly-Si followed by proper rapid thermal annealing (RTA) steps to form the desired silicide phases. In addition, some optional process steps, such as an ion implantation (I/I) process (to introduce impurities) or a poly-Si etch-back step (to adjust the poly-Si thickness for desired silicide phases) [14-18], can also be introduced before the metal deposition. Therefore, the FUSI process is less challenging from the integration point of view. However, the WF tunability on HK dielectric in these gate stacks still needs to be improved. **Chapter 6** will focus on this point and describe two practical solutions to enhance the effective WF (EWF or Φ_{eff}) tunability of Ni FUSI gate electrode on HfO_2 dielectric.

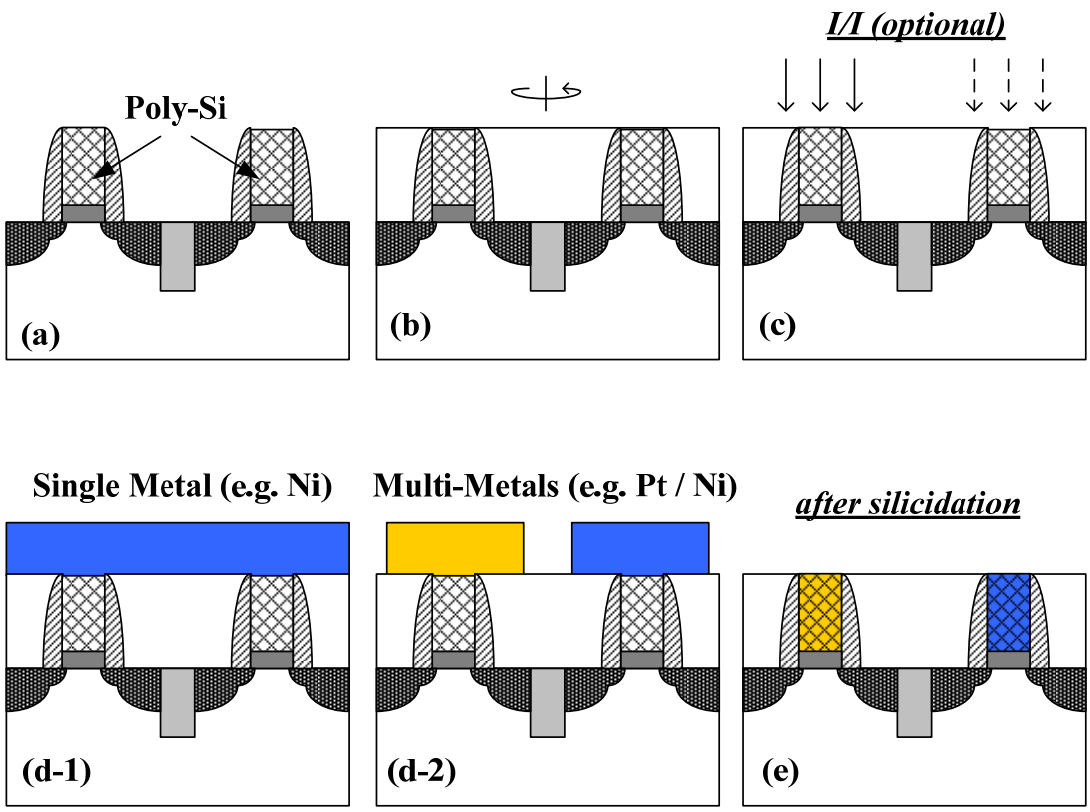


Fig. 4.3: Schematic process flow for dual MG CMOS technology by employing FUSI gate. (a) Conventional poly-Si gate CMOS fabrication; (b) Dielectric deposition over the transistors and planarization by CMP; (c) Optional ion-implantation (*I/I*) or poly-Si etch-back; (d-1) Deposition of a same metal, e.g. Ni, for both n-MOS and p-MOS or (d-2) Deposition of different metals for n- and p-MOS, respectively; (e) Silicidation process and excess unreacted metal removal.

In the above integration schemes, two different metal materials with appropriate WFs would ordinarily be required, which introduce substantial process complexity. Therefore, a method for tuning WF for a single deposited MG layer was also proposed to offer minimal process complexity by selective implantation, as illustrated in **Fig. 4.4**. As dual MGs are implemented based on nitrogen (N) implantation, TiN and N implanted TiN_x and Mo and N implanted MoN_x have been reported [19,20]. It has been suggested that the WF of a metal can be tuned by incorporating N into the metal. However, the tunable range in WF by N incorporation was not sufficient for bulk-Si CMOS transistors although it may be acceptable for ultra-thin body (UTB) MOSFETs or fully depleted silicon-on-insulator (FDSOI)

MOSFETs [21].

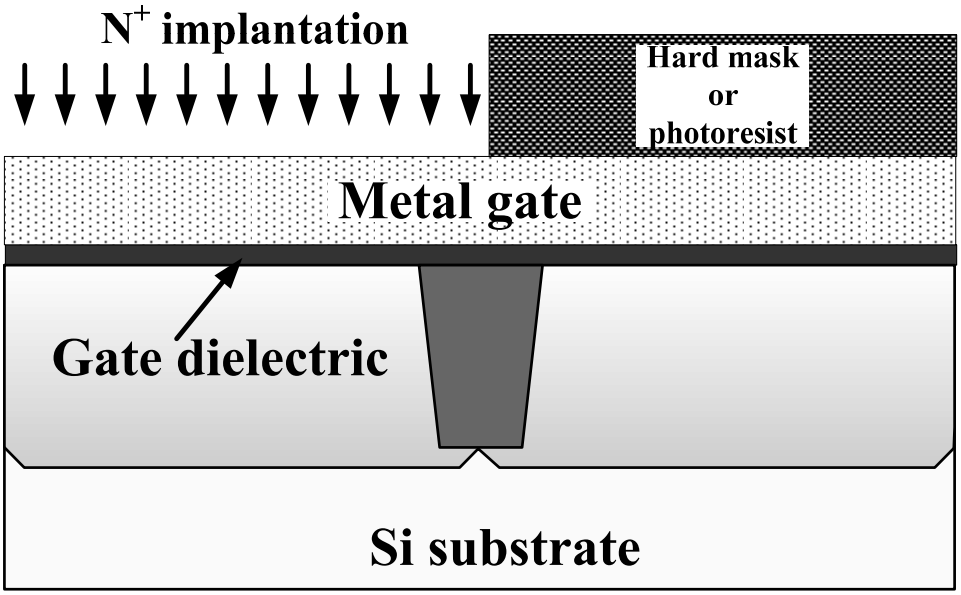


Fig. 4.4: Single metal dual WF approach using ion implantation of nitrogen into the selective metal gate region to modify metal WF.

In summary, the integration process of dual MG in CMOS technology, especially for gate first integration scheme, is a very challenging task and there are many material and process issues to be considered. Innovations in both the novel materials and process integration schemes will be highly valued. In order to address or improve some of the issues and limitations in existing integration schemes mentioned above, we have proposed two novel gate first dual MG integration methods in this chapter. The first method's aim is to solve the etching damage issue associated with the direct-etching method and thermal stability issue for n-type MG. In this process, a Ru layer is utilized to protect the underlying novel gate dielectric (HfLaO) during metal etching process and a subsequential high-temperature intermixing technique with a thermally stable n-type metal (TaN) is used to tune the EWF of Ru for both n- and p-MOS devices. The second method is to employ lanthanide elements and aluminum doped refractory metal nitride to act as n- and p-type MG respectively, which shows significant EWF tunability and good compatibility with conventional CMOS technology. It is believed that these attempts will be of practical values for the

development of the dual metal gate CMOS technology.

4.2 Highly Manufacturable CMOSFETs with Single High-*k* and Dual Metal Gate Integration Process

4.2.1 Motivation

Several approaches have been proposed to integrate dual MGs into the CMOS platform using a gate-first process flow, as discussed in the Section 4.1. Some of them employ the conventional direct-etching method, where the first-deposited metal is selectively removed from the gate dielectric, followed by the deposition of the second metal [1,3,4]. However, this may introduce a potential reliability concern as the gate dielectric is exposed to plasma or several chemical solutions during metal etching process. To avoid the exposure of gate dielectric during processing, the metal inter-diffusion process was proposed [6-11]. But the concern for this approach is that the thermal stability of these metal alloys is always limited by the properties of the low WF metal counterpart and is not suitable for a gate-first CMOS process. Park *et al.* has proposed a novel method in which an ultra-thin AlN buffer layer is used to protect the gate dielectric during metal etching, and is later consumed by Ta and Hf in an alloying process [22]. However, obtaining a thermal stability which is adequate for the S/D dopant activation step in a gate first CMOS process is still challenging. In addition, it has also been shown that the desired EWFs of MGs for the bulk-Si n- and p-MOS devices (close to the conduction and valence band edges of Si) are very difficult to be achieved in the gate first technology due to either (a) Fermi level pinning (FLP) effect between MGs and gate dielectrics [23-25], (b) reaction between metal and dielectric, or (c) oxygen vacancy at metal/dielectric interface [26,27]. As discussed in **Chapter 3**, MOS devices with lanthanum doped HfO_2 (HfLaO) dielectric have shown superior performance compared to those using pure HfO_2 gate dielectric after high temperature annealing, especially obtainable band edge EWF. TaN, HfN and TiN on HfLaO show conduction band edge EWFs, suitable for n-MOS devices,

which has also been demonstrated by other research groups [28,29]. On the other hand, Pt and Ru on HfLaO show valence band edge EWFs, suitable for p-MOS devices.

In this work, we report a dual MG integration scheme on the basis of the above gate stacks, where Ru is chosen as a p-type MG candidate because Pt is very resistant to chemical or plasma etching, which would make gate patterning for short-channel devices particularly challenging, and a TaN/Ru bilayer stack is chosen as the n-type MG candidate because the EWF of Ru can be modulated due to the inter-diffusion between TaN and Ru during a subsequently high temperature annealing. Owning to the good thermal stability of TaN and Ru on HfLaO, the temperature for the metal inter-diffusion process can be elevated to 1000^{o}C, compatible for the gate-first CMOS process. Moreover, by controlling the thickness of the bottom metal layer Ru in TaN/Ru bilayer stack on HfLaO dielectric, we have shown that the EWF of MGs can be tuned continuously in a wide range from n-type band edge (3.9 eV) to p-type band edge (5.2 eV).

4.2.2 Experiments

(100) Si substrates with n- and p-type doping concentration of 6x10^{15} cm^{-3} were used. For MOS capacitor (MOSCAP), after a dilute hydrofluoric (DHF)-last RCA pre-gate clean, HfLaO films (with 50% La) with different physical thicknesses were deposited using reactive sputtering, followed by post-deposition anneal (PDA) in N_2 with a small amount of O_2 at 600ºC for 30 s. A HfLa target (Hf:La=1:1, atomic ratio) was used to reduce moisture absorption of La during exposure to air [30]. Different thicknesses (from 2 nm to 50 nm) of the bottom Ru metal layer were promptly deposited on HfLaO by DC sputtering in physical vapor deposition (PVD) tool. The top TaN metal layer (150 nm) was then deposited in situ by reactive sputtering. In addition, MOS devices with single metal layer, pure Ru (50 & 100 nm) or TaN (150 nm), were fabricated for comparison. After gate patterning, all the

devices went through rapid thermal annealing (RTA) with different temperatures up to 1000°C for thermal stability evaluation. For MOSFET fabrication, source/drain implantations of BF_2 (50 keV, $1x10^{15}$ cm^{-2}) were performed, followed by RTA activation at 1000°C for 5 s. Finally, all samples received a backside Al metallization and forming gas annealing (FGA) at 420°C for 30 min.

4.2.3 Results and Discussion

4.2.3.1 Physical and Electrical Characteristics

Before describing the dual MG CMOS integration scheme, let us review some key results mentioned in **Chapter 3**, especially for MOS devices with pure Ru (and TaN) and HfLaO gate stack. **Figure 4.5** shows the plot of flat band voltage (V_{fb}) versus equivalent oxide thickness (*EOT*) for pure Ru metal on HfLaO with 50% La after 1000°C annealing. The low dependence of V_{fb} with varying *EOT* implied that there was a very low fixed charge density near the interface between HfLaO and the Si channel. However, the contribution of charges in HfLaO near the gate cannot be completely ruled out to explain the observed difference in V_{fb}. Still, it is unlikely that any modification of fixed charges by Ru would be significantly different from the modification by TaN (see the inset of **Fig. 4.5**). Therefore, the changes of V_{fb} for these gate stacks are mainly due to the changes of metal EWF. In addition, based on the V_{fb} values on $6x10^{15}$ cm^{-3} n-doped Si, a corresponding EWF of around 5.2 eV for Ru on HfLaO is extracted. Combining with the results of TaN on HfLaO (shown in the inset of **Fig. 4.5)**, we provide evidence that the incorporation of La can release the FLP between metal and HfO_2 dielectric, causing EWF shifts from mid-gap 4.64 eV [4] to 5.2 eV for p-metal Ru, and from 4.4 eV [25] to 3.9 eV for n-metal TaN respectively. A specific model has been proposed in **Chapter 3** to explain these results, where the change of the metal EWF is attributed not only to the oxygen vacancy (V_O) density in the HK layer, but also to the difference in electronegativities of the materials in gate stacks.

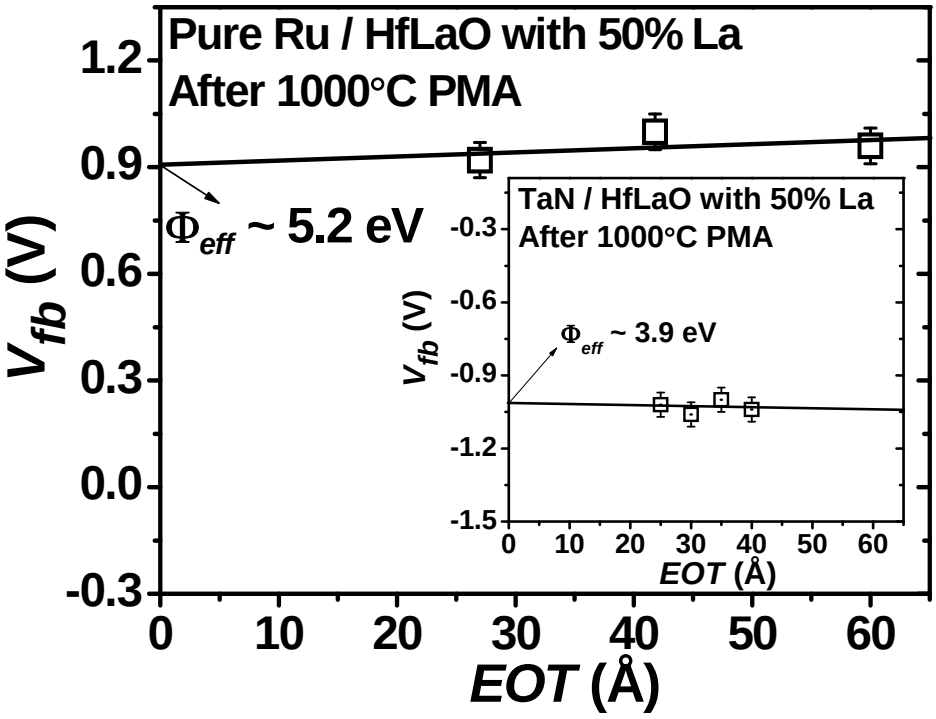


Fig. 4.5: The plot of V_{fb} versus *EOT* for devices with pure Ru on HfLaO dielectric on n-type Si substrate ($6x10^{15}$ cm^{-3} doping concentration) after 1000ºC post metal annealing (PMA). The case for devices with pure TaN gate on HfLaO dielectric on p-type Si substrate ($6x10^{15}$ cm^{-3} doping concentration) is shown in the inset. Both V_{fb} and *EOT* were extracted from high-frequency *C-V* measurement. The corresponding Φ_{eff} of Ru (TaN) on HfLaO is 5.2 (3.9) eV.

Based on the results above and the characteristics of metal inter-diffusion approach as described in last section, some physical and electrical characteristics of TaN/Ru bilayer structure were further investigated in this work.

Figures 4.6(a) and **(b)** show the energy dispersive X-ray spectroscopy (EDX) results of TaN and Ru (~5 nm) bilayer structure for as-deposited and annealed samples (1000^oC), respectively. It can be observed that the top metal layer has little inter-diffusion with the bottom metal layer after deposition and this is probably due to the sputter process, while more TaN has obviously diffused through the Ru layer up to the Ru/HfLaO interface during high temperature annealing. Moreover, the cross-sectional transmission electron microscopy (TEM) pictures (in the insets)

indicate good continuity and uniformity of the different layers before and after high temperature annealing.

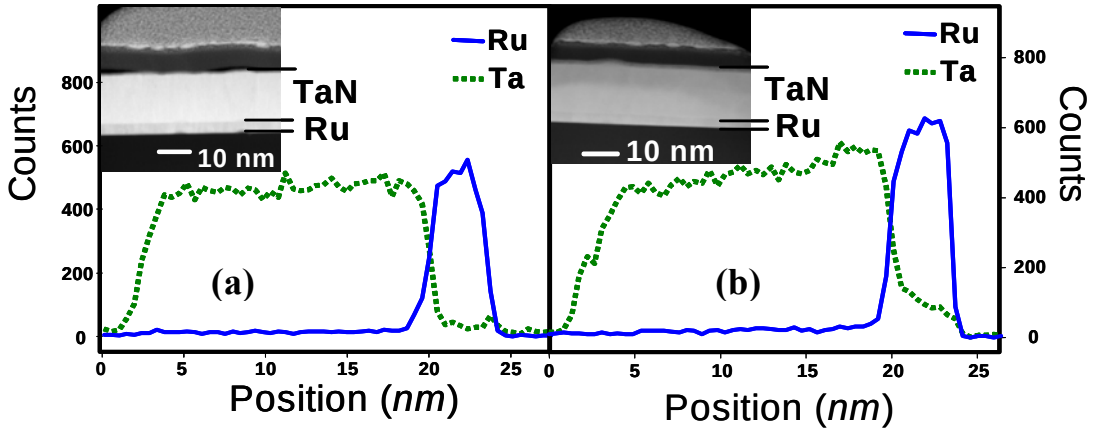


Fig. 4.6: EDX analysis for TaN/Ru/HfLaO stack, (a) as deposited and (b) after 1000ºC RTA with 5 s. Ta diffusion into Ru layer up to the interface between Ru and HfLaO after high temperature annealing was detected. Moreover, the corresponding TEM pictures (insets) indicate good continuity and uniformity for different layers in the gate stack, please note here that the top layers above TaN layer were only used for the EDX analysis.

Figure 4.7(a) shows the normalized *C-V* curves of MOSCAPs with TaN, TaN/Ru bilayer structure (with different Ru thicknesses), and Ru MGs on HfLaO after high temperature annealing (1000^{o}C). The gradual V_{fb} shift from that of single TaN layer (~ -0.3 eV) to that of single Ru layer (~ 1.0 eV) can be clearly seen as the bottom layer Ru thickness increases from 0 to 50 nm. This causes an EWF difference for TaN and Ru which can be explained by the observation from EDX shown above. Due to the diffusion of the top metal layer (TaN) to the bottom layer (Ru) up to the Ru/HfLaO interface, the EWF of Ru can be modulated accordingly. The similar phenomena at relatively low annealing temperature have been reported in previous works [6,9,10]. **Figure 4.7(b)** shows an example for TaN/Ru gate stack with ~10 nm Ru after different temperature annealing. The EWF decreased dramatically with the increase of annealing temperature due to the increase of TaN concentration at the interface between Ru and HfLaO. However, the EWF of the MGs remained the same after the gate stack went through two subsequent annealing at 1000^{o}C, which suggests

that the EWF changes after high temperature annealing are stable and permanent [31].

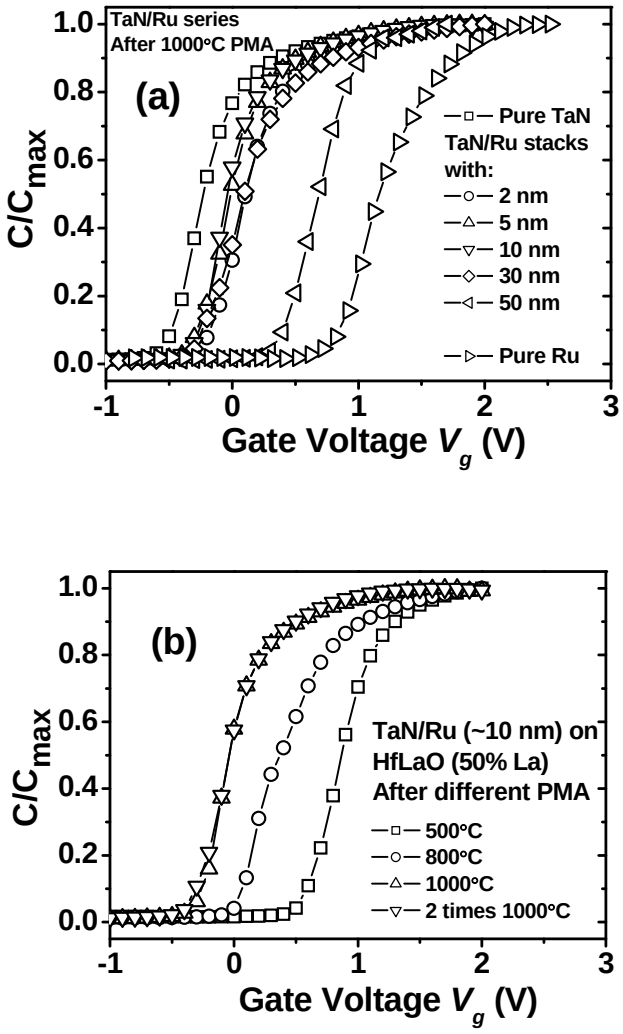
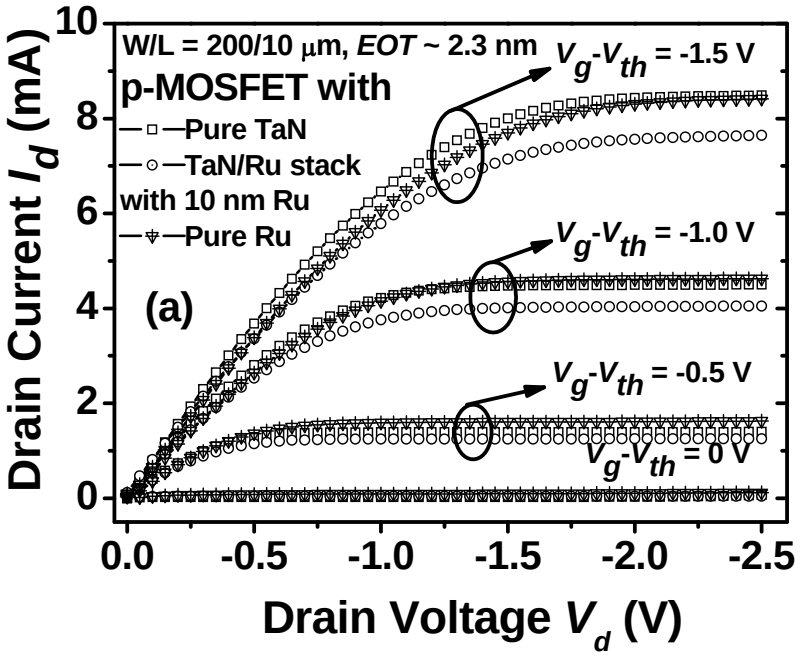


Fig. 4.7: (a) *C-V* curves for pure TaN, TaN/Ru stacks and pure Ru after 1000ºC PMA. As the thickness of bottom metal layer Ru decreases, there are more n-type metal TaN diffusion through Ru to the Ru/HfLaO interface so as to decrease the EWF of MGs. (b) *C-V* curves for TaN/Ru stack with 100 Å Ru on HfLaO after different temperature PMA. The V_{fb} shifts toward negative direction with the increase of annealing temperature up to 1000ºC. However, the *C-V* curve showed stable V_{fb} and no significant *EOT* variation during consecutive annealing at 1000ºC after the first 1000ºC annealing process. This indicates that the EWF changes are stable and permanent after high temperature annealing and are not affected by the subsequent thermal treatments.

Figure 4.8(a) shows the plots of the drain current versus drain voltage (I_d-V_d) for long-channel p-MOSFETs with pure TaN, TaN/Ru stack with ~10 nm Ru and pure Ru MGs on HfLaO dielectric. Compared with the case of pure TaN, the

well-behaved and similar I_d-V_d characteristics for the cases of pure Ru and TaN/Ru stack indicate the channel region of MOS devices has no obvious degradation due to the introduction of Ru and the inter-diffusion annealing for TaN/Ru stack. **Figure 4.8(b)** shows the plots of the drain current versus gate voltage (I_d-V_g) for long-channel p-MOSFETs with pure TaN, TaN/Ru stack with different Ru thicknesses and pure Ru metal gates on HfLaO dielectric. Very good transfer characteristics with an around 75 mV/dec subthreshold slope (*SS*) are demonstrated. Considering the V_{th} values for the devices with single TaN and single Ru gate, EWFs can be extracted as ~3.9 eV and ~5.2 eV respectively, which are in good agreement with the results extracted from the MOSCAPs. In addition, the V_{th} shift for those devices with TaN/Ru stacks follows the same trend as the V_{fb} shift observed in MOSCAPs. These results confirm that by employing HfLaO dielectric and TaN/Ru bilayer structure with different Ru thicknesses, EWF can be tuned continuously from n-type band edge (3.9 eV) to p-type band edge (5.2 eV).



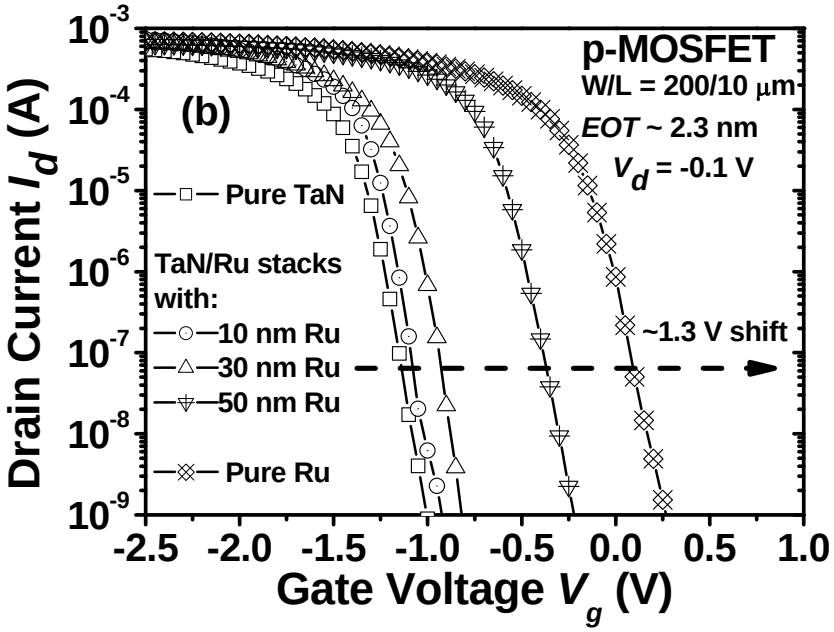
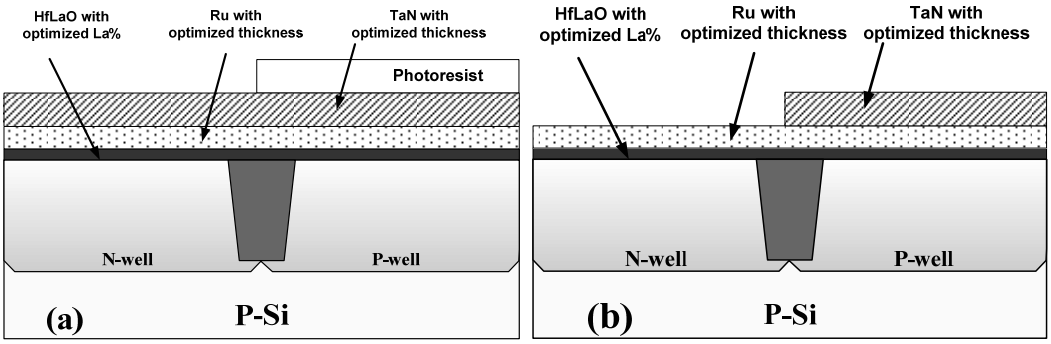


Fig. 4.8: (a) I_d-V_d and (b) I_d-V_g characteristics of p-MOSFETs with pure TaN, TaN/Ru stack with 10 nm Ru and pure Ru MGs after 1000ºC annealing.

4.2.3.2 Integration Scheme for CMOS Technology

Based on the above results, a simplified process flow for dual MG CMOS fabrication is shown in **Fig. 4.9**, wherein a single HK layer (HfLaO with optimized La%) was obtained without being exposed during the process and the thickness ratio of TaN to Ru metal layer should also be optimized to obtain n-type band edge EWF.



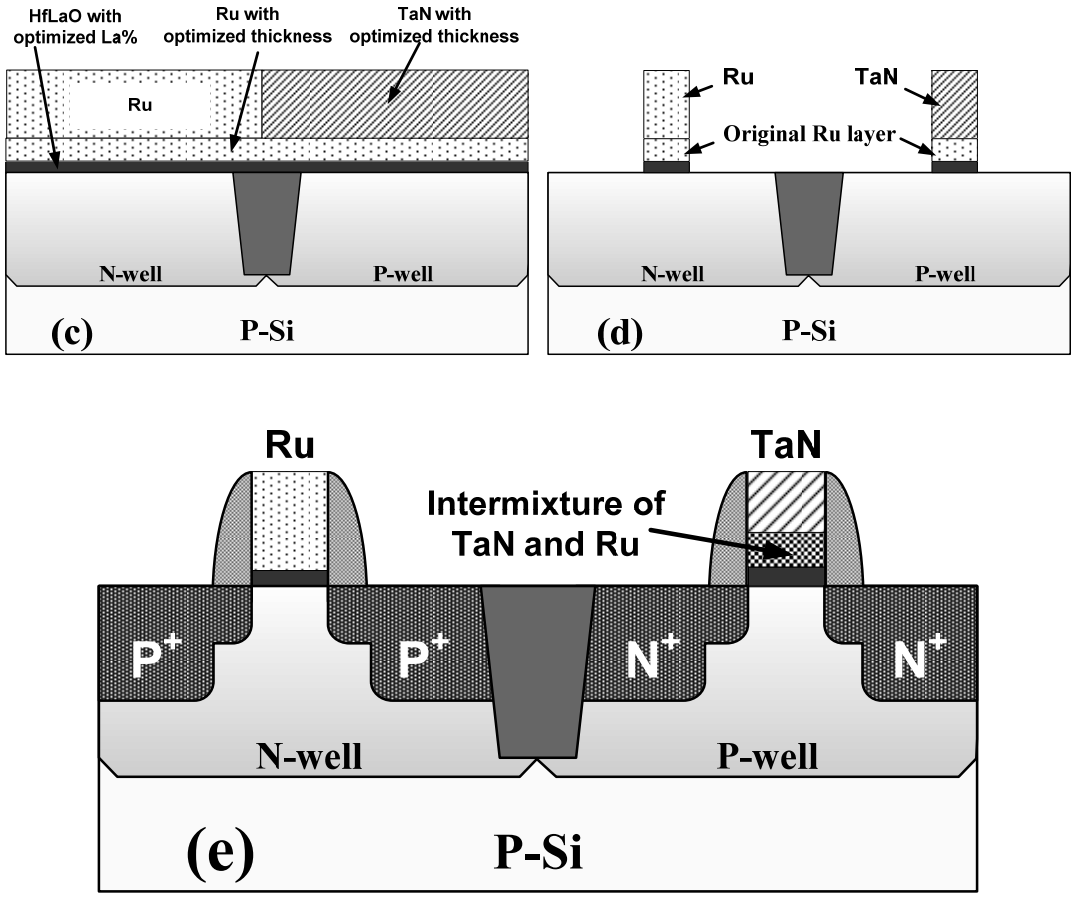


Fig. 4.9: (a)-(e) Schematic illustration of the process flow for possible dual metal gate CMOS integration.

In addition, to study the feasibility of this proposed metal inter-diffusion process, we first investigate the selectivity of TaN with respect to Ru. The selectivity of etching rate between Ru and TaN in both dry etch and wet etch ambient was investigated. **Figure 4.10** shows optical emission spectra (OES) intensities detected during etching of Ru gate stack in O_2 plasma, line spectra of the Ru elements are also shown on the right axis. The endpoint of TaN, etched in Cl_2 plasma is obtained using 520 nm wavelength. When Ru is exposed to Cl_2 plasma, the Ru film is not etched due to formation of nonvolatile $RuCl_x$. Similarly, when TaN is exposed to O_2 plasma, it cannot be etched. Moreover, the HfLaO film is not etched either when it is exposed to O_2 plasma, which indicates an easy way to integrate such dual MGs. While for wet etch ambient, **Table 4.1** summarizes the etch rates of TaN and Ru in standard cleaning-1 (SC-1) ($NH_4OH+H_2O_2+H_2O$) solution at 80^oC. The etch rate of TaN is

around 16 nm/min while that of Ru is almost negligible. This also demonstrates the very high etching selectivity of the TaN over Ru.

Table 4.1: Etching rates of TaN and Ru in hot SC-1 solution.

Solution	Etching rate (nm/min)	
	TaN	Ru
Hot SC-1 ($NH_4OH : H_2O_2 : H_2O$)	~16	0

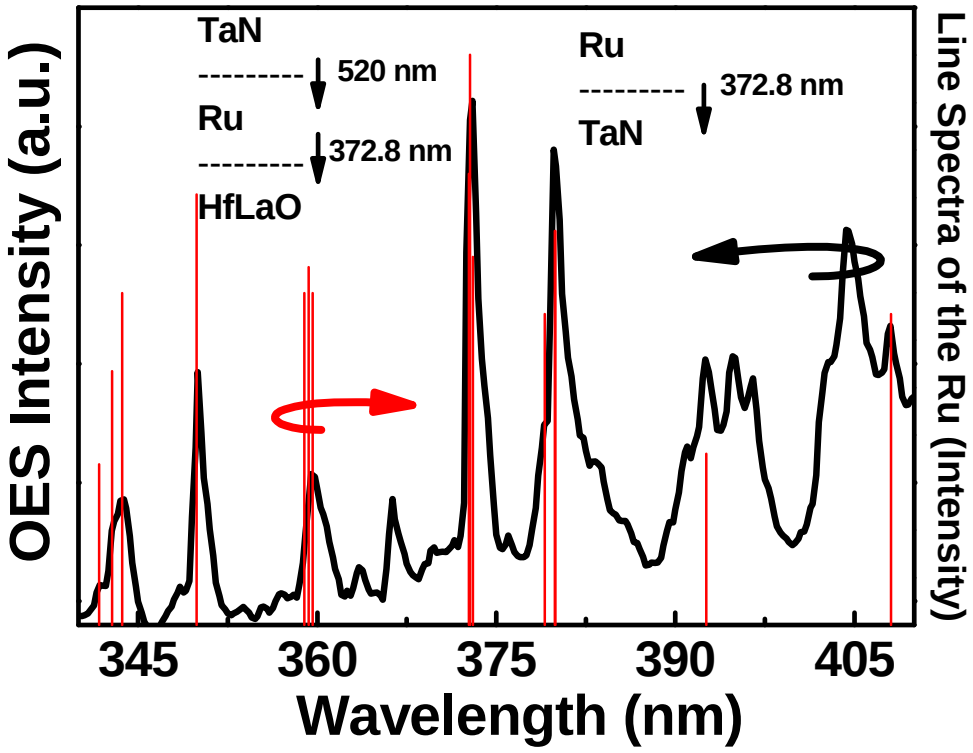


Fig. 4.10: OES intensities detected during etching of Ru gate stack in O_2 plasma, line spectra of the Ru elements also shown on the right axis. The endpoint of TaN, etched in Cl_2 plasma is obtained using 520 nm wavelength. When Ru is exposed to Cl_2 plasma, Ru film is not etched due to formation of nonvolatile $RuCl_x$. Moreover, HfLaO film is not etched either when it is exposed to O_2 plasma.

After evaluating the selectivity of TaN with respect to Ru, the surface morphology of the Ru films with similar thickness under three different conditions:

as-deposited Ru film and Ru films with the top TaN layer removed by dry etch and wet etch method respectively was examined by atomic force microscopy (AFM). As shown in **Fig. 4.11**, the root mean square (RMS) roughness variation induced by the TaN etching process is only about 0.064 nm compared to the original as-deposited Ru film, indicating that the TaN removal process has negligible physical impact to the underlying Ru film. In addition, the X-ray photoelectron spectroscopy (XPS) was also employed to further analyze the surfaces for these three cases. As shown in **Fig. 4.12**, the consistent XPS spectra for Ru 3d core level indicate minimal TaN residue after etch process and no significant influence on chemical bond change for the originally underlying Ru layer.

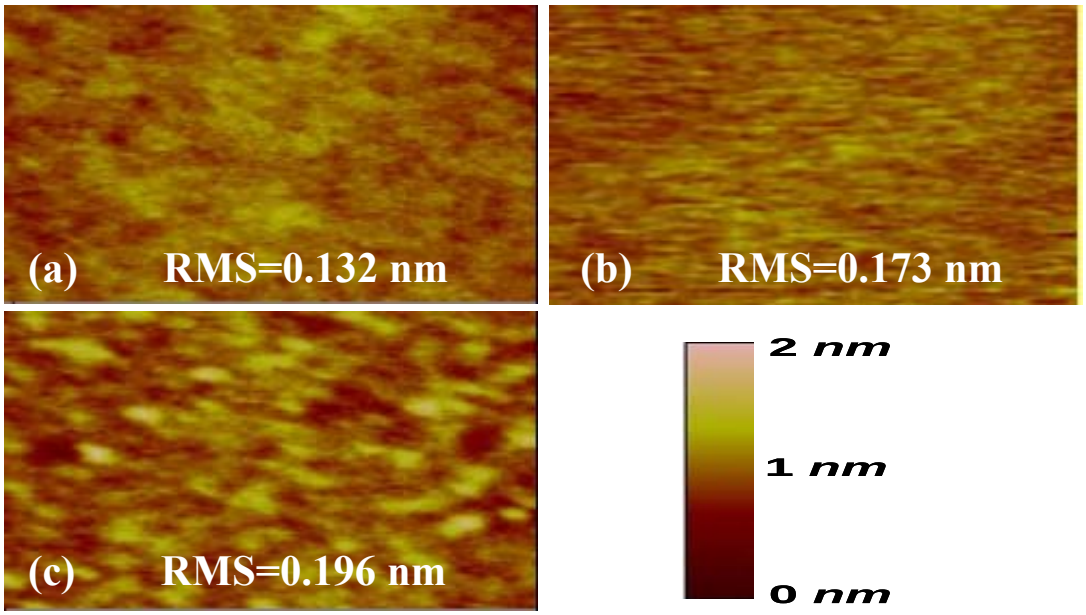


Fig. 4.11: AFM pictures for pure Ru film (a), TaN/Ru stacks after TaN etching in both dry and wet mode, respectively (b) & (c). 0.064 nm variation of RMS indicates negligible physical damage to the original Ru layer during the etch processes.

To further examine the potential influence of the etching process on the electrical properties of MOS devices with Ru/HfLaO gate stack, Ru was re-deposited onto the exposed Ru layer after removing the TaN gate by dry etch and wet etch methods in the p-MOS region. Some electrical characteristics of these MOS devices

are compared in **Figs. 4.13**. The typical *C-V* curves as shown in **Fig. 4.13(a)** were measured at 100 kHz. The *EOT* and V_{fb} of the three gate stacks can thus be extracted by fitting the *C-V* measurements with simulated curves which takes quantum mechanical effect into account. It can be seen that the *EOT* and V_{fb} of the three gate stacks are almost identical as well as the *I-V* characteristics for them, as shown in **Fig. 4.13(b)**. In addition, the distributions of gate leakage current (J_g) for these three gate stacks are summarized in **Fig. 4.13(c)** and no significant degradation in *I-V* characteristics is observed after removing TaN process by dry etch or wet etch method. All of these results suggest that the underlying Ru and HfLaO dielectric layers are not damaged during the processes for removing the TaN layer.

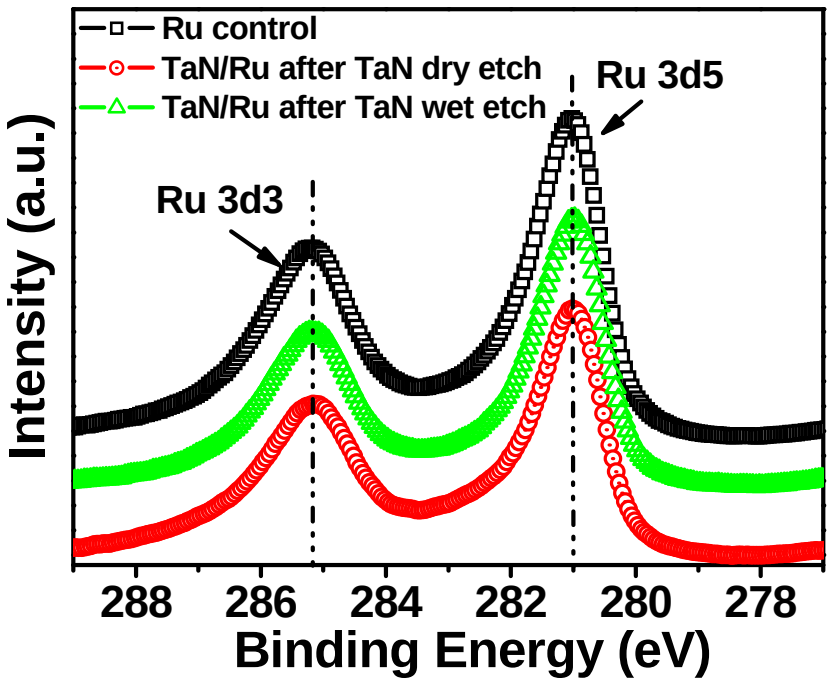


Fig. 4.12: XPS spectra for Ru 3d core level taken from pure Ru film, TaN/Ru stacks after TaN etching in both dry and wet etch methods.

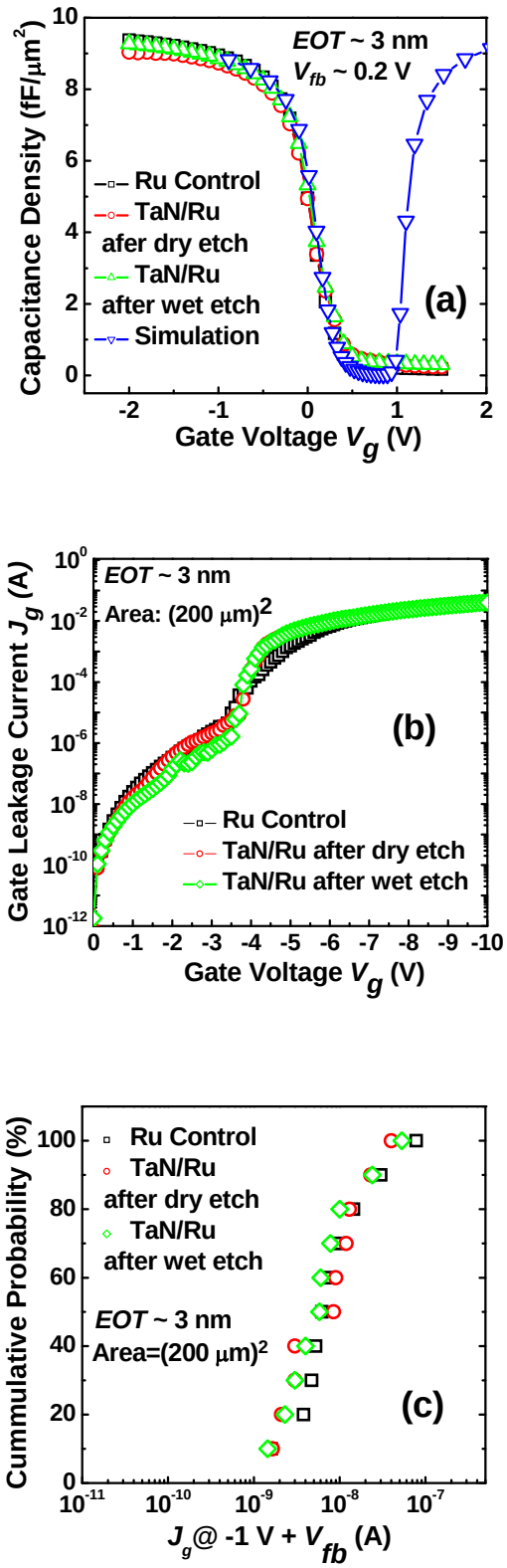


Fig. 4.13: Comparison of *C-V* characteristic (a), *I-V* characteristic (b) and J_g distribution @ V_{fb}-1 V (c) among the Ru control devices and re-deposited Ru layer after removal of TaN layer by dry etch and wet etch methods respectively.

4.2.4 Summary

In this part, a novel dual MG technology by using TaN/Ru bilayer metal structure on HfLaO HK gate dielectric is demonstrated. Due to the inter-diffusion between the top layer metal (TaN) and the bottom layer (Ru) during high temperature annealing (1000°C) and the release of FLP between gate electrodes (Ru and TaN) and HfLaO, the EWF of these gate stacks has a wide EWF tunability range from 3.9 eV to 5.2 eV. These results show that TaN/Ru (for n-MOSFETs) and Ru (for p-MOSFETs) on HfLaO gate stacks are promising candidates for future CMOS integration technology. In addition, we also propose and demonstrate a very highly manufacturable CMOS integration process for these gate stacks.

4.3 Work Function Tunability of Refractory Metal Nitrides by Lanthanum or Aluminum Incorporation for Advanced CMOS Devices

4.3.1 Motivation

Refractory metal nitrides (MN_x) such as TaN, TiN, HfN and WN have been widely studied for gate electrode applications [32,33]. Their good thermal stability, excellent scalability and compatibility with HK dielectrics make them one of the leading candidates to replace conventional poly-Si gate. However, the EWFs of most MN_x materials are close to the mid-gap position of Si, especially after high temperature annealing [25], which are insufficient for planar bulk-Si CMOS technology.

Based on the understanding in **Chapter 2 & 3**, the metal-dielectric interface or dipole layer is indeed a critical factor in determining the EWF of MGs. In fact, interface states, either intrinsic or extrinsic, would be created when MGs and HK dielectrics are placed in contact and generally charge transfer could occur across these interface states at the dielectric side and/or the metal electrode side, which tends to drive (or pin) the EWF of metals at a particular position, namely FLP, related to the materials involved in gate stacks, the thermal treatment condition and so on [23-27]. Since this FLP effect between the dielectric and the gate electrode seems unavoidable, we can use this property to our advantage to engineer metal-dielectric interface, i.e. utilize this FLP effect positively to obtain appropriate EWF values.

In this study, we report the work function tunability of MN_x (TaN and HfN) by incorporating lanthanum (La) and aluminum (Al), which is believed to be due to the change of interface states resulting from the incorporation of La or Al. The compatibility of this work function tuning method with conventional high temperature source/drain (S/D) annealing is also investigated. Based on our results, we further

propose a dual MG integration process using refractory metal nitrides.

4.3.2 Experiments

(100) n- & p-doped ($6x10^{15}$ cm^{-3}) Si substrates were used in MOS fabrication process. After active area definition and standard RCA clean, thermal SiO_2 with 4 different thicknesses (35 Å, 55 Å, 75 Å and 95 Å) or sputtered HfO_2 (50 Å) was deposited, wherein the thicknesses were evaluated by ellipsometer. Subsequently, either $(Hf_xLa_{1-x})N_y$, or $(Ta_xAl_{1-x})N_y$ gate, followed by an *in-situ* TaN capping layer were deposited to complete the gate stack. The concentration of La in $(Hf_xLa_{1-x})N_y$ was controlled by varying the sputter power ratio between the HfLa target and the Hf target. It is noteworthy that a HfLa target (Hf:La=1:1) instead of a La target, was used for $(Hf_xLa_{1-x})N_y$ deposition to reduce moisture absorption of pure La [30]. For the $(Ta_xAl_{1-x})N_y$ gate, the concentration of Al was controlled by varying the power ratio between the Ta target and the Al target. PMA splits were conducted by RTA at 900–1000°C in N_2 ambient to study the thermal stability of the MGs. The detailed process flow for this work is shown in **Table 4.2**. The atomic concentrations of the ternary nitride gates were determined by XPS. Quantum-mechanical effects were taken into account when simulating the measured *C-V* curves for V_{fb} and *EOT* extraction.

Table 4.2: Process flow for MOS device fabrication in this work.

* Active area definition and RCA cleaning;
* Thermal oxidation SiO_2 with 4 thicknesses, or ~50 Å PVD HfO_2;
* 500 Å $(Hf_xLa_{1-x})N_y$ or $(Ta_xAl_{1-x})N_y$ gate reactive co-sputtering; For $(Hf_xLa_{1-x})N_y$ case, different La% was obtained by changing DC power for HfLa target with fixed Ar/N_2 flow rate (25/5 sccm) and DC power for Hf target (200 W); For $(Ta_xAl_{1-x})N_y$ case, different Al% was obtained by changing DC power for Al target with fixed flow rate of Ar/N_2 (25/5 sccm) and DC power for Ta target (450 W).
* In-situ TaN capping layer (1000 Å);
* Gate patterning;
* PMA (900°C, 950°C 30 sec or 1000°C 2 sec in N_2 ambient);
* Forming gas anneal (FGA) 30 min @420°C.

4.3.3 Results and Discussion

4.3.3.1 Lanthanide Doped MN_x, $(M_xLa_{1-x})N_y$, for n-MOS

Figure 4.14 shows the Auger electron spectroscopy (AES) analysis of $(Hf_{0.70}La_{0.30})N_y$ composition in a MOS structure. There is an obvious difference in the N concentration at the TaN layer and the $(Hf_{0.70}La_{0.30})N_y$ layer, which implies that N bonding with HfLa alloy could be easier than that with Ta metal. It is seen that an additional 900°C anneal to the initial FGA does not cause a significant change to the depth profile of the gate stack, highlighting the thermal stability of the gate stack at high annealing temperatures.

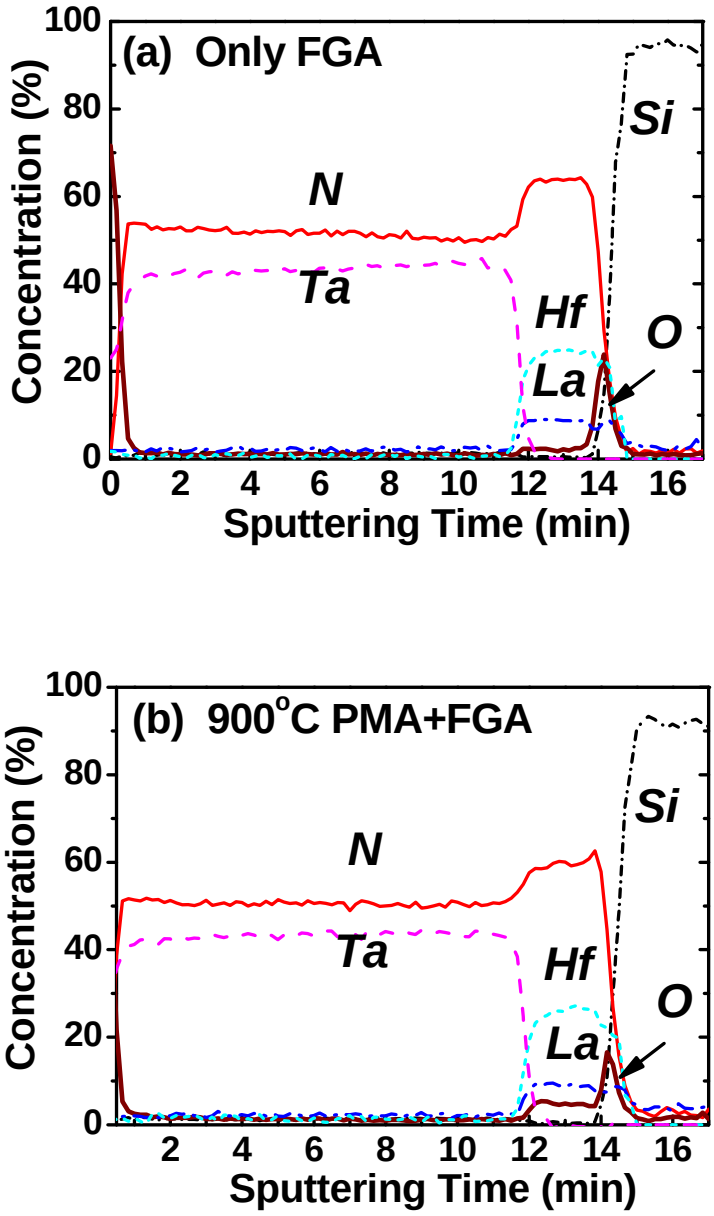


Fig. 4.14: AES depth profiles of the TaN/$(Hf_{0.70}La_{0.30})N_y/SiO_2$ gate stack (a) only FGA; (b) 900°C PMA for 30 sec and FGA.

The modulation of V_{fb} with varying La concentration in $(Hf_xLa_{1-x})N_y/SiO_2$ /p-Si capacitors is seen in **Fig. 4.15**. The V_{fb} shifts towards the negative direction with the increase in La composition for $(Hf_xLa_{1-x})N_y$ gate electrodes. In addition, excellent fit of the simulated *C-V* curve to the measured *C-V* curves confirm that SiO_2/Si substrate interface quality was not degraded with La incorporation.

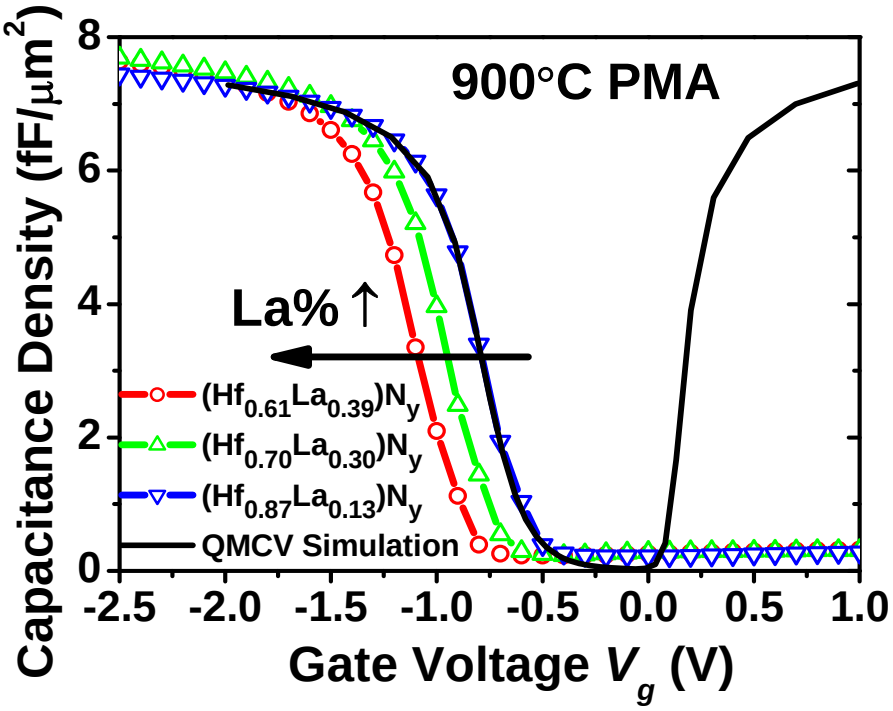


Fig. 4.15: Typical 100 kHz *C-V* curves of MOS Capacitors with $(Hf_xLa_{1-x})N_y$ grown on SiO_2 after 900°C PMA annealing. With the increase of La% in $(Hf_xLa_{1-x})N_y$, V_{fb} shifts to more negative direction.

Figure 4.16 gives the relationship between V_{fb} and *EOT* which were obtained from the *C-V* curves of $(Hf_xLa_{1-x})N_y/SiO_2$/p-Si capacitors by varying the SiO_2 thicknesses. Based on the following equation,

$$\Phi_M = \Phi_{Si} + V_{fb} - \frac{Q_{ox}}{C_{ox}} \qquad (4\text{-}1)$$

where $\boldsymbol{\Phi}_M$ and $\boldsymbol{\Phi}_{Si}$ are the work functions of the metal gate and Si substrate, respectively, Q_{ox} is the equivalent oxide charge per unit area, and C_{ox} is the oxide capacitance, the $\boldsymbol{\Phi}_M$ of $(Hf_xLa_{1-x})N_y$ with different La composition were extracted and given in **Fig. 4.16**. It can be seen that with the increase in La composition for $(Hf_xLa_{1-x})N_y$ gate, the $\boldsymbol{\Phi}_M$ decreases continuously, down to a value of 3.91 eV (for $Hf_{0.61}La_{0.39}N_y$ gate).

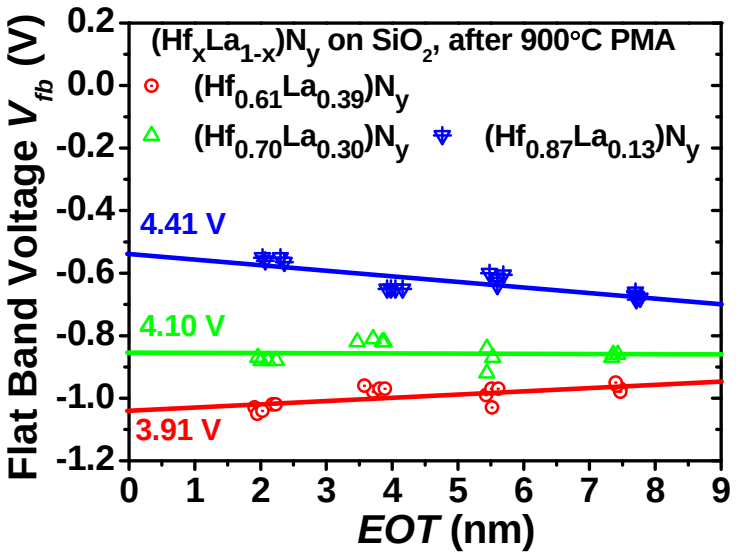


Fig. 4.16: V_{fb} vs *EOT* extracted from *C-V* curves, for different La composition in $(Hf_xLa_{1-x})N_y$ metal gates after 900°C annealing. Metal work function $\boldsymbol{\Phi}_M$ was extracted by extrapolating the line to eliminate the contribution of fixed oxide charges.

From the V_{fb} vs *EOT* plot in **Fig. 4.16**, we found that the magnitude of Q_{ox} does not change significantly for $(Hf_xLa_{1-x})N_y$ metal gates with different La composition. However, the polarity of Q_{ox} changes from positive to negative with increasing La composition. The extracted *EOT* for all the gate stacks were also found to be thinner than the original SiO_2 thicknesses. **Figure 4.17** shows the cross-sectional TEM picture of a $(Hf_{0.70}La_{0.30})N_y/SiO_2/Si$ gate stack after 900°C, 30 s PMA. It is seen that the formation of an intermediate layer has occurred between the metal gate and underlying SiO_2 after the high temperature anneal. In addition, the SiO_2 physical thickness (~23.5 Å) after annealing was found to be thinner than the deposited SiO_2 thickness. EDX depth profile of the same gate stack [**Fig. 4.18(a)**] shows the intermixing of La and Hf with the original SiO_2 layer. In contrast, **Figure 4.18(b)** shows the HfN/SiO_2 gate stack, wherein no Hf diffusion into the SiO_2 layer was detected. Therefore, the intermediate layer formed was probably a metal silicate and the change in the polarity of Q_{ox} could be due to the reaction/intermixing between the metal gate and SiO_2. This was also observed when other lanthanide elements were incorporated into another refractory metal nitride, TaN [34]. Despite this, **Figure 4.19**

indicates that La incorporation in $(Hf_xLa_{1-x})N_y$ improves the leakage current by ~ 2–3 orders when compared with a conventional poly-Si/SiON stack. This was attributed to the increase in dielectric physical thickness due to the high-*k* layer formation (metal silicate) between the gate electrode and SiO_2 layer.

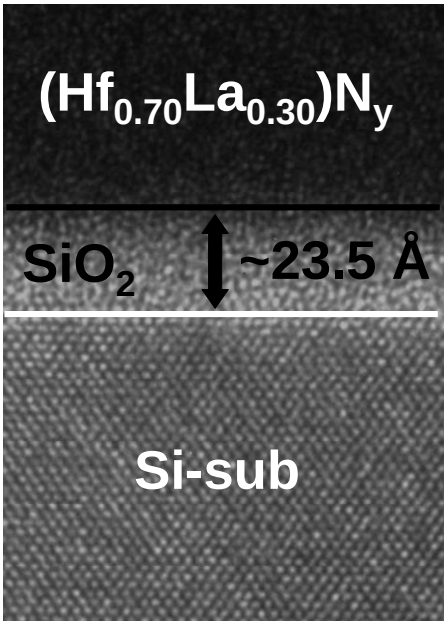
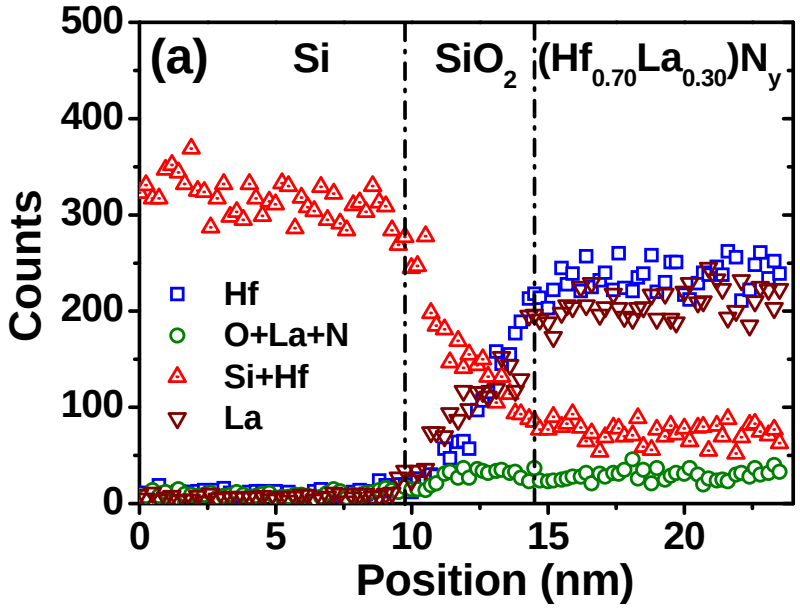


Fig. 4.17: Cross-sectional TEM for $(Hf_{0.70}La_{0.30})N_y/SiO_2/Si$ gate stack after 900°C, 30 s PMA.



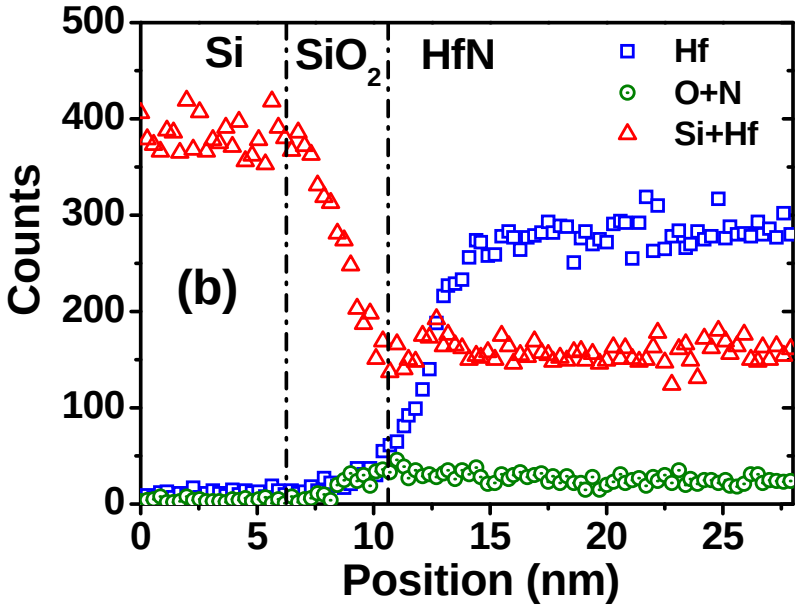


Fig. 4.18: EDX depth profile (a) for $(Hf_{0.70}La_{0.30})N_y/SiO_2/Si$ gate stack and (b) $HfN/SiO_2/Si$ gate stack. Intermixing of La and Hf with SiO_2 was found in (a), while no Hf diffusion into SiO_2 was detected in (b).

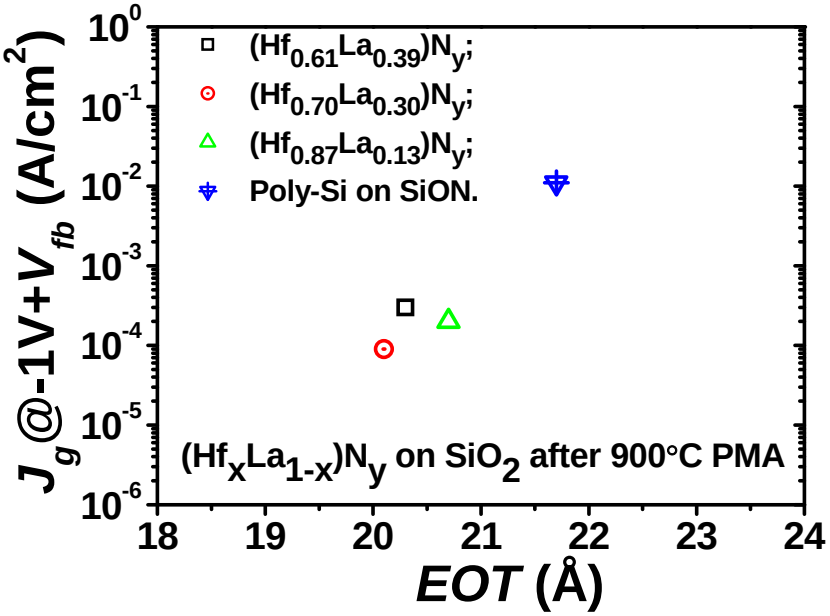


Fig. 4.19: Gate leakage current comparison of $(Hf_xLa_{1-x})N_y/SiO_2$ gate stacks with poly-Si/SiON gate stack. A lower J_g was obtained for $(Hf_xLa_{1-x})N_y/SiO_2$ gate stacks due to the formation of a high-*k* layer.

Figure 4.20 summarizes the EWF values of $(Hf_xLa_{1-x})N_y$ metal gates with varying La composition under different annealing conditions. It can be seen clearly that the EWF of HfN metal gate is modulated from 4.6 eV to 3.9 eV continuously by changing the La composition in the $(Hf_xLa_{1-x})N_y$ metal gate. This is stable after 900–1000°C anneal and the excellent thermal stability could be related to the enhanced N content in the $(Hf_xLa_{1-x})N_y$ films. **Figure 4.21** compares EWF data from this work and our previous work [35], for lanthanide (LA) doped refractory metal nitrides on SiO_2 gate dielectric after a 1000°C anneal. It can be seen that wide EWF tunability can be obtained by the incorporation of LA into refractory metal nitride gates.

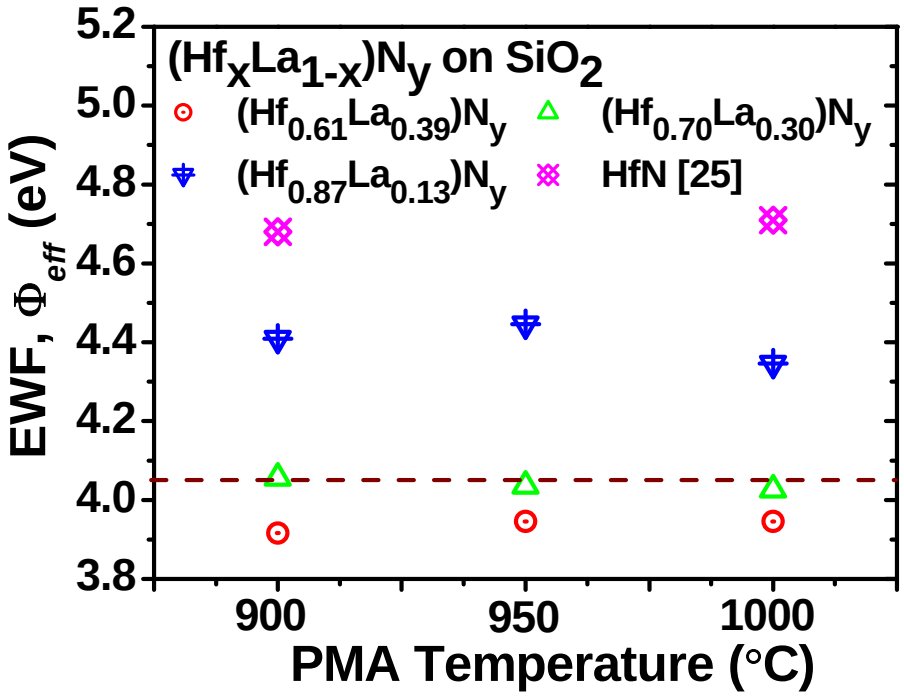


Fig. 4.20: Summary of the Φ_{eff} values for $(Hf_xLa_{1-x})N_y/SiO_2$ capacitors with varying La composition under different annealing conditions. The Φ_{eff} of HfN can be modulated from 4.6 eV to 3.9 eV continuously by changing the La composition in $(Hf_xLa_{1-x})N_y$ film.

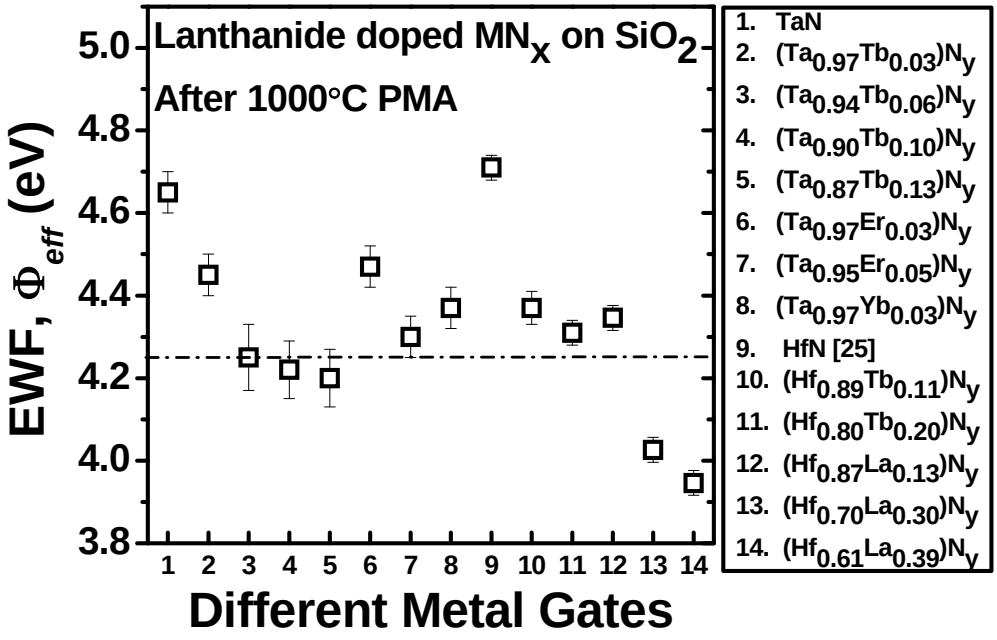


Fig. 4.21: Summary of $\boldsymbol{\Phi_{eff}}$ for lanthanide doped MN_x on SiO_2 after 1000°C PMA. The effect of lanthanide on $\boldsymbol{\Phi_{eff}}$ tunability is clearly seen.

Besides the investigation of EWF tunability for $(M_xLA_{1-x})N_y/SiO_2$ gate stacks, the EWF modulation for $(M_xLA_{1-x})N_y$ on Hf-based HK dielectric by lanthanide incorporation into TaN, is also shown in **Fig. 4.22**. ~310 mV V_{fb} shift can be seen with 10% Tb incorporation into TaN. EWF tunability was similarly reported for a $(M_xLA_{1-x})N_y$/HfSiON gate stack in [34], which indicates the good compatibility of LA incorporated metal nitrides with HK dielectrics.

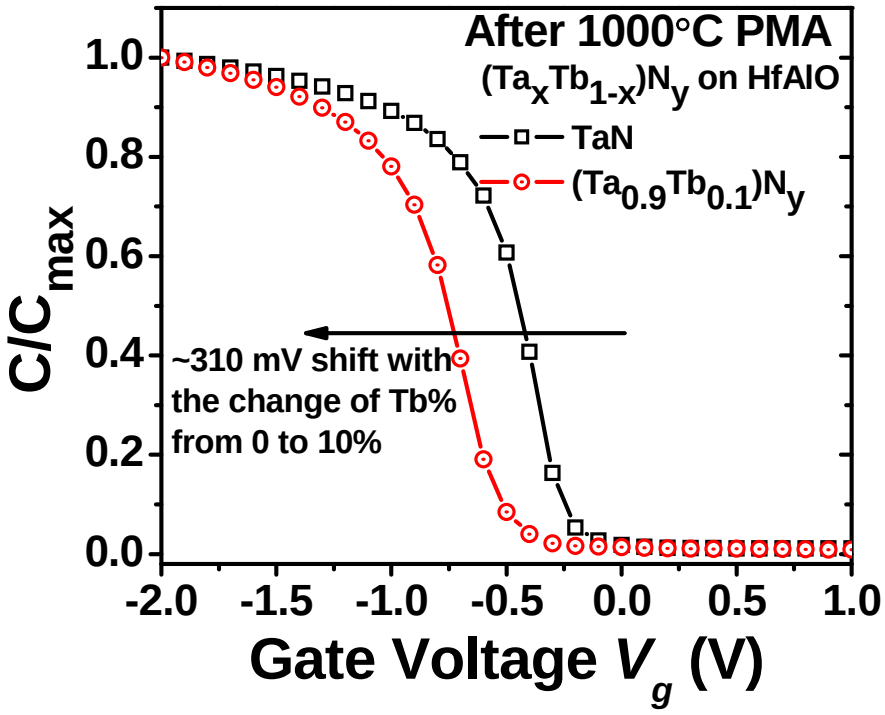


Fig. 4.22: *C-V* curves of $(Ta_xTb_{1-x})N_y$/HfAlO/Si MOS capacitors with different Tb composition after 1000ºC PMA. The V_{fb} shift indicates the Φ_{eff} difference of the metal gates.

4.3.3.2 Aluminum Doped MN_x, $(M_xAl_{1-x})N_y$, for p-MOS

As reported before, the addition of aluminum into MN_x could tune the WF to p-type band-edge on SiO_2 dielectric [36,37], and the key experimental results are summarized in the **Fig. 4.23**. It is observed that with the increase of Al% in $(M_xAl_{1-x})N_y$, the EWF is modulated towards the Si valence band-edge with good thermal stability till 1000°C.

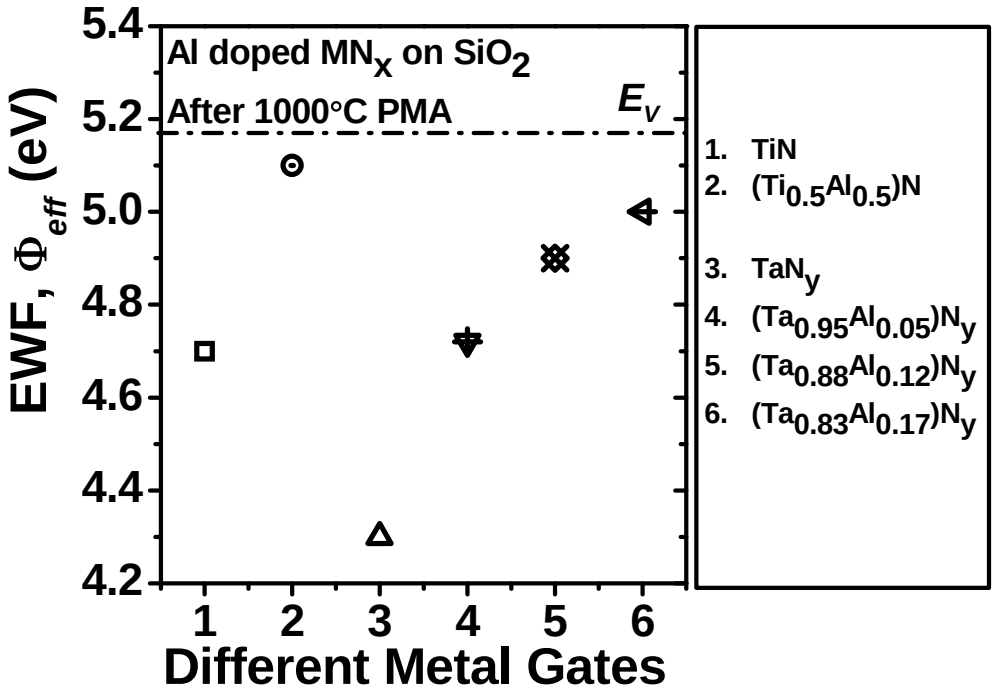


Fig. 4.23: Φ_{eff} summary for aluminum doped MN_x on SiO_2 after 1000°C PMA from previous works [36,37]. The effect of aluminum on the Φ_{eff} tunability is clearly seen.

The compatibility of $(M_xAl_{1-x})N_y$ work function tunability on HfO_2 HK dielectric is further investigated. **Figure 4.24** shows the typical *C-V* curves of $(Ta_xAl_{1-x})N_y/HfO_2$ capacitors fitted with the simulated *C-V* curve. A positive V_{fb} shift of ~250 mV was seen after 24% Al incorporation which reflects the approximate EWF change of MG. Gate leakage current for $(Ta_xAl_{1-x})N_y$ metal gates (with different Al%) and TaN gate after a 1000°C anneal is shown in **Fig. 4.25**. The incorporation of Al did not show any appreciable increase in gate leakage current as compared with TaN/HfO_2 gate stack which indicates there is no degradation to the underlying HfO_2 dielectric.

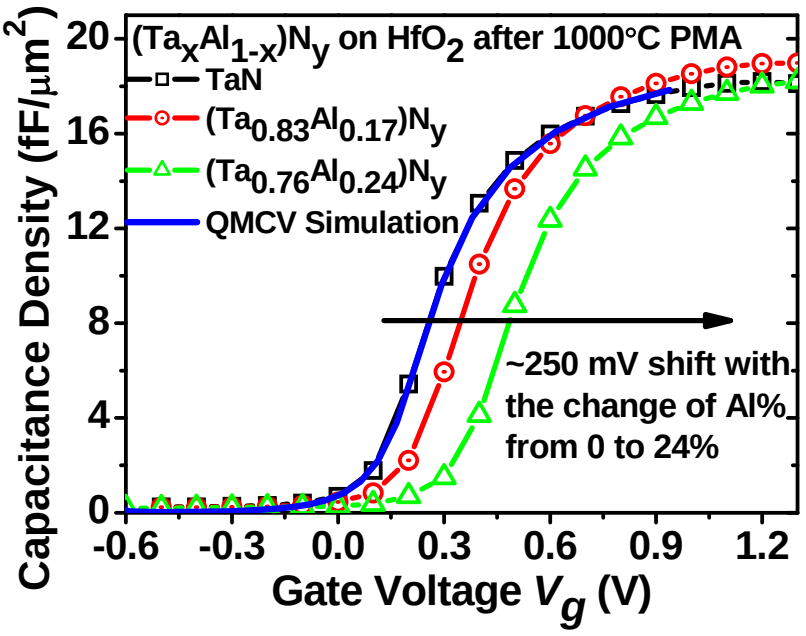


Fig. 4.24: *C-V* curves of $(Ta_xAl_{1-x})N_y/HfO_2/Si$ MOS capacitors with different Al composition after 1000ºC PMA. V_{fb} shifts to more positive direction with the incorporation of Al into TaN, due to the Φ_{eff} difference among these metal gates.

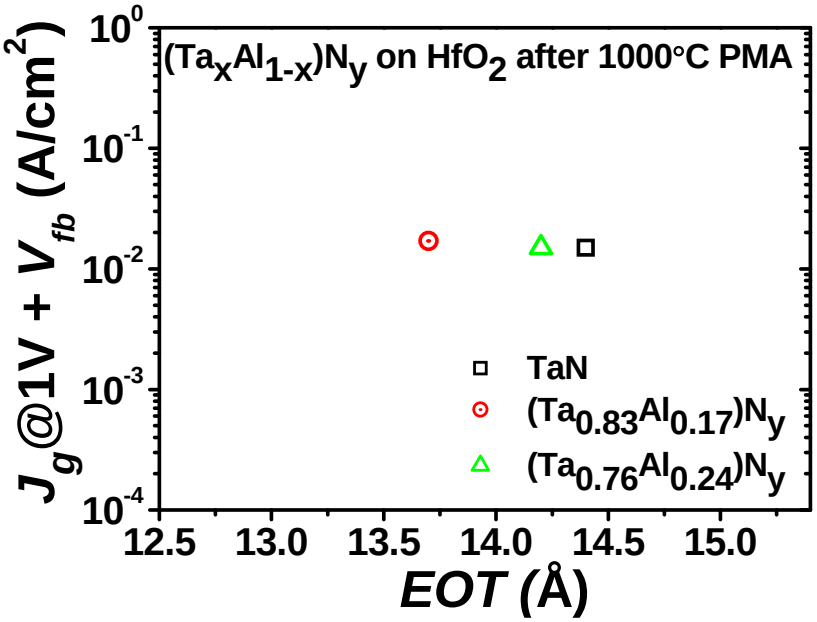


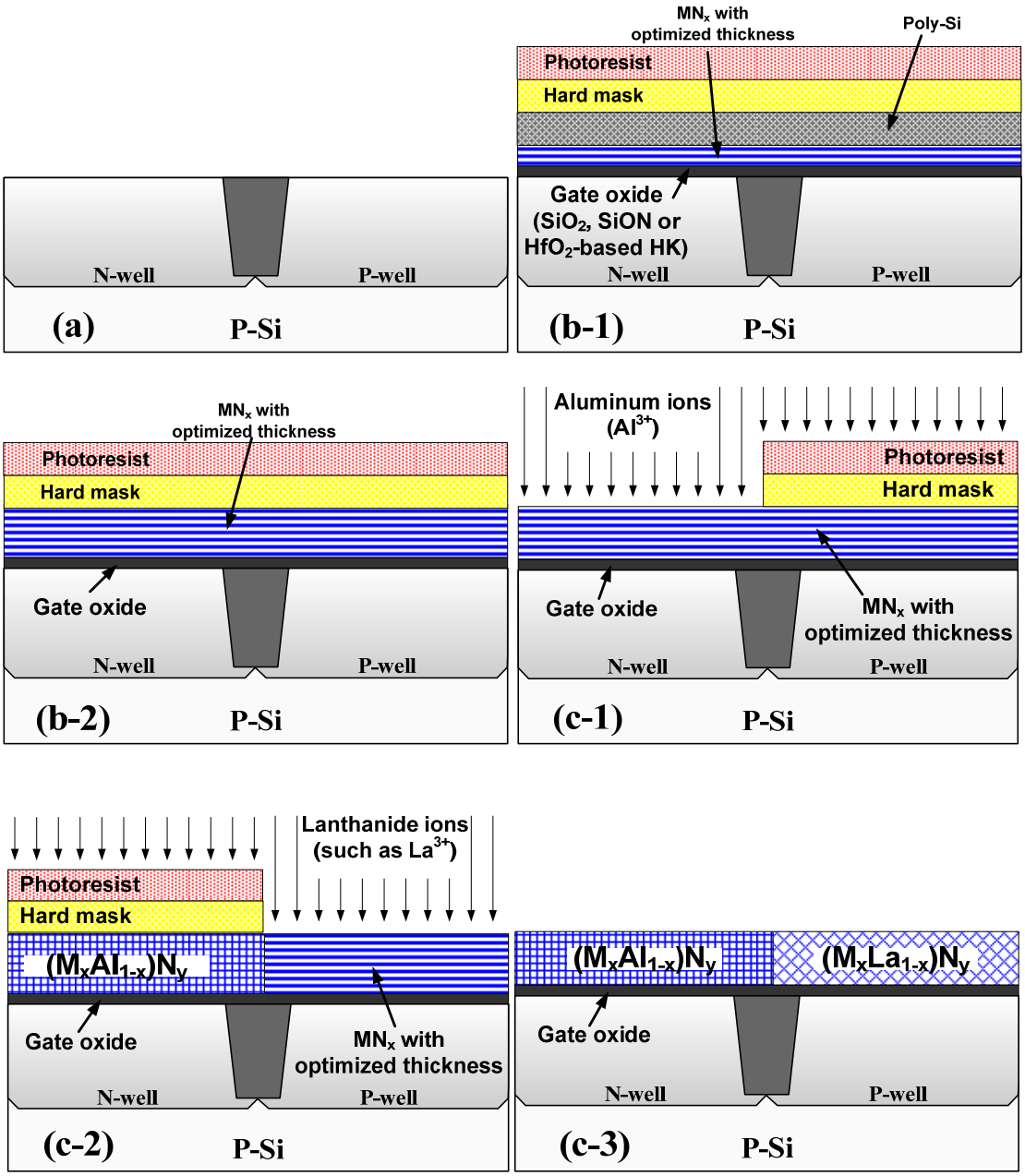
Fig. 4.25: Comparison of gate leakage current among $(Ta_xAl_{1-x})N_y/HfO_2$ gate stacks with different Al composition, with no obvious damage to the dielectric layer due to the incorporation of Al into TaN.

4.3.3.3 Dual Metal Gate Integration Process for CMOS

Based on above results, we can see that the effect of the incorporated La (or other lanthanide elements) and Al into gate electrodes (MN_x) on the EWF tunability is very clear. In addition, similar effect of La and Al on EWF has also been found when they are incorporated into the gate dielectrics [28,29,38-40]. Therefore, it can be concluded that the existence of La and Al or their oxides over the interface between gate electrodes and dielectrics is the key factor to tune the EWF of MGs possibly by changing the FLP position, and the utilization of this significant FLP effect positively to obtain appropriate EWFs for CMOS technology will attract immense interest. In this work, we propose a novel alternative integration process for dual MG CMOS technology to introduce La (or other lanthanide elements) and Al into n-MOS and p-MOS gate stacks respectively by employing metal ion implantation. In fact, the feasibility of implanting Al and other lanthanide ion (Yb) has been demonstrated successfully for Ni-based FUSI gate electrodes [41,42]. The schematic process flow of this CMOS compatible scheme for dual MG integration is shown in **Fig. 4.26**. After shallow trench isolation (STI) formation, well and threshold adjust implants, gate oxide, either SiO_2, SiON or HfO_2-based HK dielectrics, selected MN_x with optimized thickness and/or poly-Si capping layer are subsequently deposited. With the help of photoresist (PR) and/or hard mask, N-well and P-well region are then implanted by Al and La ions respectively. After gate patterning, lightly doped drain (LDD) and sidewall spacers are formed, followed by S/D implantation and activation. A dual MG CMOS device with $M_xAl_{1-x}N_y$ for p-MOS and $M_xLa_{1-x}N_y$ for n-MOS respectively is thus fabricated.

In addition, it is also possible to simplify the above integration scheme by depositing Al doped MN_x or lanthanide doped MN_x gate electrode directly on the dielectric layer, and followed by lanthanide ion implantation for the n-MOS region or Al ion implantation for the p-MOS region. Considering the large atom radii of lanthanide, there may be a concern during the implantation. Therefore, the latter

method would be more preferable, i.e. depositing a lanthanide doped MN_x layer first on the whole wafer, followed by selective Al ion implantation for p-MOS region. Here note that a small amount of lanthanide at the metal/dielectric interface would be sufficient to modify the WF of MN_x toward the conduction band of Si [43,44], therefore we can choose a low concentration of lanthanide in the original lanthanide doped MN_x gate electrode so that the subsequent implanted Al can pile up and become a dominant element to affect the final EWF of MG in the interfacial layer between the lanthanide doped MN_x and the dielectric.



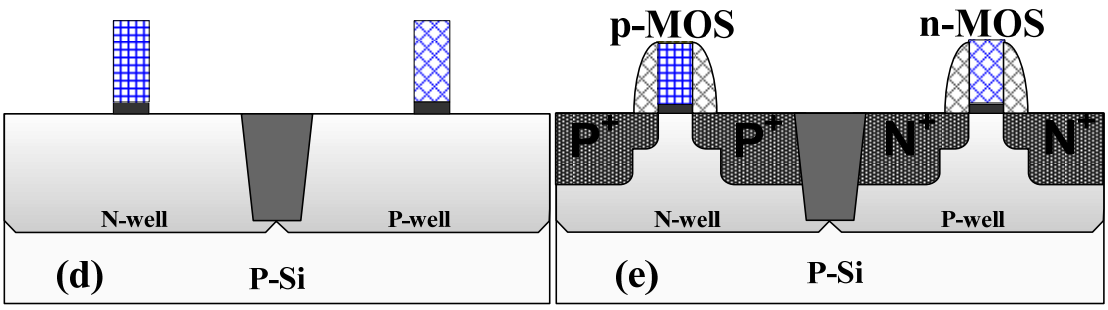


Fig. 4.26: Schematic illustration of the process flow for possible dual MG CMOS integration. (a) STI formation, well and threshold adjust implantations; (b-1) Gate dielectric and MN_x capped with poly-Si layer or (b-2) single MN_x layer, followed by hard mask deposition and PR coating; (C-1~C-3) Interface engineering by lanthanide and aluminum ion implantation for n-MOS and p-MOS, respectively; (d) Gate pattern; (e) Formation of LDD and sidewall spacer and S/D implantations.

4.3.4 Summary

In this part, we report EWF tunability by incorporating lanthanum and aluminum into MN_x on both SiO_2 and HfO_2-based dielectrics with good thermal stability (up to 1000°C), which is believed to be due to the change of interface states resulting from the incorporation of La or Al. Based on our results and previous data, we further propose an easy and feasible integration process for dual MG CMOS technology.

4.4 Conclusion

In this chapter, we proposed two integration schemes for dual MG CMOS technology based on our experimental results, and both of them belong to gate first integration process.

The first scheme involves novel gate stacks to create wide enough EWF tunability by using a high-temperature metal inter-diffusion technique. In this process, HfLaO dielectric layer is employed to increase the tunable EWF range based on the results of **Chapter 3**. In addition, to avoid the gate dielectric from being exposed

during the metal etching process, the original Ru capping layer is kept throughout the process flow. This addresses the etching damage issues associated with the conventional direct-etching integration scheme. More importantly, the EWF of the Ru layer can be modulated by a high-temperature metal inter-diffusion between Ru and upper TaN layer, and this diffusion process is compatible with the conventional gate-first CMOS process flow. By using this integration scheme, the EWF of these gate stacks has a wide EWF tunable range from 3.9 eV to 5.2 eV. These results make TaN/Ru (for n-MOSFETs) and Ru (for p-MOSFETs) on HfLaO gate stacks promising candidates for future CMOS integration technology.

Since FLP effect seems unavoidable in gate stacks involving HK dielectrics and gate electrodes (poly-Si or MGs), another novel integration scheme is also proposed in this chapter, where FLP effect is utilized positively to obtain appropriate EWFs for both n- and p-MOS devices. By incorporating La (or other lanthanide elements) and Al into selected MN_x (TaN, HfN or TiN), the EWF of MN_x clearly shifts to conduction band edge and valence band edge of Si respectively, which is very suitable for bulk-Si CMOS technology. This phenomenon is believed to be due to the change of interface states resulting from the incorporation of La or Al, and is independent of whether they are at gate electrode side or gate dielectric side. In addition, the compatibility of this EWF tuning method with conventional high temperature S/D annealing is also demonstrated.

The proposed novel integration schemes may provide some useful discussions to address some of the major issues associated with the conventional integration schemes, and are believed to make a contribution to the development of the dual MG integration processes for future bulk-Si CMOS technology.

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Chapter 5

Evaluation of Reliability in MOSFETs with HfO_2 and HfLaO Gate Dielectrics

5.1 Introduction

With the continuous scaling of the planar CMOSFET, the replacement of the conventional SiO_2 gate dielectric with high-permittivity (k) materials is required to suppress the exponential increase in gate leakage current [1]. Although a large amount of effort has been invested toward high-k gate dielectrics, currently many critical problems still remain. One of them for high-k integration is charge trapping and de-trapping, which causes the threshold voltage (V_{th}) instability. Recently, it was demonstrated that severe charge trapping phenomena occurs in transistors with high-k gate dielectrics under uniform static stress, i.e. the stress voltage (V_g) is always applied and $V_{ds} = 0$, leading to concerns on the bias temperature instability (BTI) in such transistors [2-4]. However, in practical digital CMOS integrated circuits (ICs), MOSFETs typically operate under dynamic stress conditions, i.e. V_g and V_{ds} are opposite in terms of phase. It has been shown that the V_{th} shift under the dynamic stress exhibits better stability than that under the static stress for transistors with SiO_2 gate dielectric [5]. Therefore, understanding the dynamic BTI behavior in transistors with high-k gate dielectrics is crucial for their introduction in practical digital ICs.

HfO_2 has been demonstrated as a promising high-k dielectric candidate because of its relatively high permittivity (~25), large band gap (~5.8 eV) and relatively good thermal stability [6]. In this chapter, a comprehensive investigation of BTI degradation under both static and dynamic stresses is first performed for n- and p-MOSFETs with HfO_2 gate dielectrics deposited by metal-organic chemical vapor

deposition (MOCVD), including the dependence of the V_{th} shift on stress time, stress amplitude and stress mode (static stress or dynamic stress). We find the experimental evidence that BTI degradation in HfO_2 gate dielectric improves with the increase of stress frequency in both n- and p- MOSFETs under dynamic stresses, and hence the device lifetime is prolonged. In addition, to evaluate the feasibility of HfLaO dielectric further, its BTI characteristic has been also investigated by both static (DC) and transient (pulsed I_d-V_g) measurement techniques under dynamic stress, which shows a significant improvement as compared to that of HfO_2 dielectric.

5.2 Dynamic Threshold Voltage Instability in MOSFETs with HfO_2 Gate Dielectric and Its Impact on Device Lifetime

5.2.1 Motivation

As mentioned above, HfO_2 or HfO_2-based gate dielectrics are extensively investigated as alternatives to future CMOS technology. However, their reliability must be satisfactorily demonstrated before any of them can be selected by the semiconductor industry.

In this part, a comprehensive investigation of BTI degradation under both static and dynamic stresses is performed for n- and p-MOSFETs with HfO_2 gate dielectric. We examine the dependence of the V_{th} shift on stress time, stress amplitude and stress mode (static stress or dynamic stress). Moreover, we report the experimental evidence that BTI degradation in HfO_2 gate dielectric improves, and hence the device lifetime prolongs, with the increase of stress frequency in both n- and p- MOSFETs under dynamic stresses. This is distinct from the case of SiO_2 gate dielectric, for which the improvement of BTI shows little dependence on stress frequency [5,7,8]. Lastly, we introduce a new physical model that accounts for carrier trapping/de-trapping and trap generation in the HfO_2 dielectric under stress, with simulation results in good agreement with all experiment data.

5.2.2 Experiments

MOSFETs were fabricated using a self-aligned process [9]. After a dilute HF-last RCA pre-gate cleaning, HfO_2 films with a physical thickness of ~50 Å were deposited on silicon substrates in a MOCVD cluster tool, followed by an in-situ post-deposition anneal (PDA) in N_2 ambient to improve the film quality. A HfN film (~50 nm) with 100 nm TaN as a capping layer was then deposited *ex-situ* by DC sputtering in a mixed Ar and N_2 gas ambient, and patterned using a Cl_2-based etchant. For n- and p- channel MOSFETs, implantation of phosphorus and BF_2, respectively, at a dose of $5x10^{15}$ cm^{-2} was performed to form the source/drain (S/D) regions. Rapid thermal anneal (RTA) in N_2 at 950 °C for 30 s was employed to activate the dopants. After patterning the Al interconnect, the MOSFETs were subjected to back side Al metallization and sintering in a forming-gas ambient (H_2:N_2 = 1:10) at 420 °C for 30 mins.

The equivalent oxide thickness (*EOT*) of the HfO_2 gate dielectric is ~1.3 nm for both n- and p-MOSFETs, as obtained by *C-V* measurement with quantum mechanical correction. To simulate the actual stress condition in circuits, voltage stresses with square wave but with opposite phases at the gate and the drain were applied, as described in [5]. The values of V_{th}, sub-threshold swing (*SS*), and transconductance (G_m) were obtained from measurements of I_d-V_g which were periodically monitored during stressing. In order to minimize the effect of charge de-trapping in the static (DC) measurement technique, we tried to reduce the stress break-time when the stress was removed during the I_d-V_g measurement by a computer program (~2 sec in this experiment), and the schematic illustration for measure equipment is shown in **Fig. 5.1**. The measured V_{th} from fresh devices were 0.5 V for n-MOSFETs and -0.45 V for p-MOSFETs.

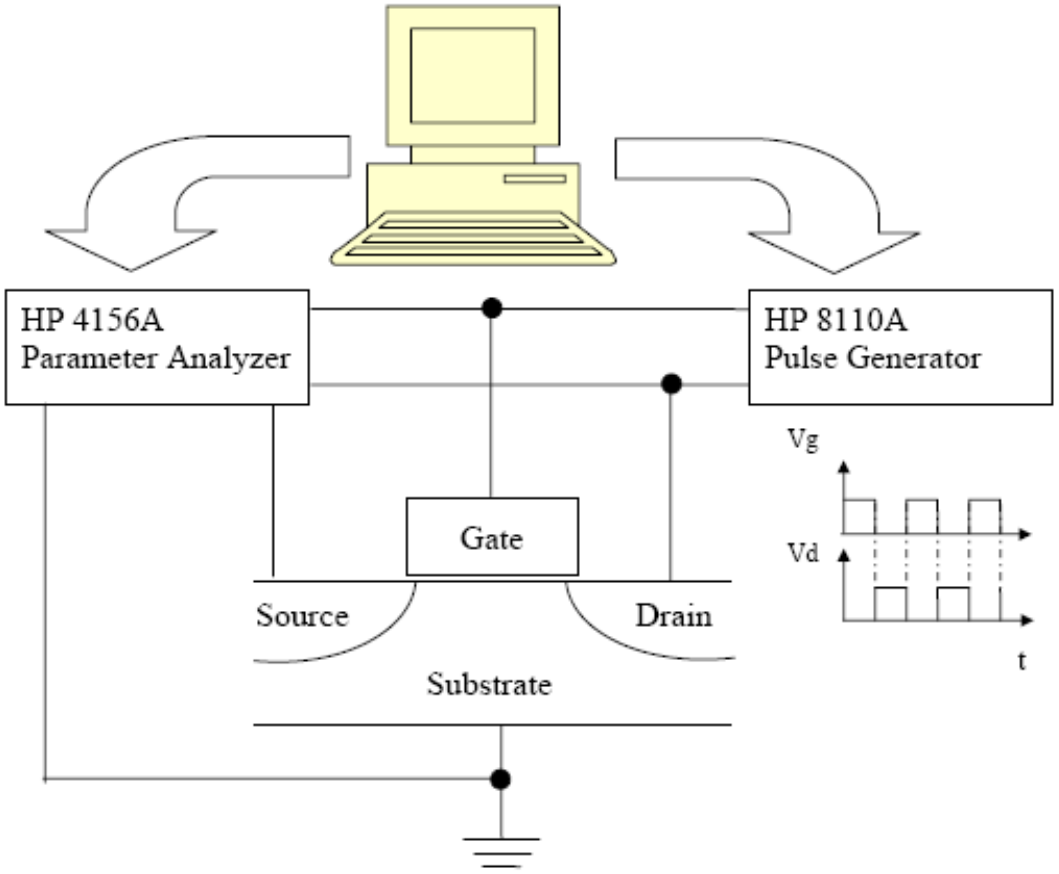


Fig. 5.1: A square wave with 50% duty cycle is imposed at gate and drain terminals with opposite phases respectively, and drain current (I_d) versus gate voltage (V_g) is measured between the consecutive stress.

5.2.3 Experimental Results and Discussion

V_{th} instability was first investigated under the static stress for both n- and p-channel MOSFETs at room temperature. V_{th} shift shows a power law dependence on stress time, as shown in **Figs 5.2 (a)** and **(b)**. It is also observed that V_{th} instability shows strong dependence on the stress voltages: V_{th} shifts more with an increase in stress voltages. Furthermore, from the insets of **Figs 5.2 (a)** and **(b)**, it is noted that there exist two different slopes (S) in the time evolution of V_{th} under all the stress biases: a fast stage followed by a slow stage. Sub-threshold swing (SS) was monitored during the stress to evaluate the correlation between V_{th} shift and interface state density. For both n- and p-MOSFETs, we observed that SS does not show any observable change with stress time in contrast to the case of SiO_2 gate dielectric,

indicating that interface state generation plays no significant role in the V_{th} instability. This suggests that the BTI issue is primarily due to charge trapping in the bulk dielectric [2-4].

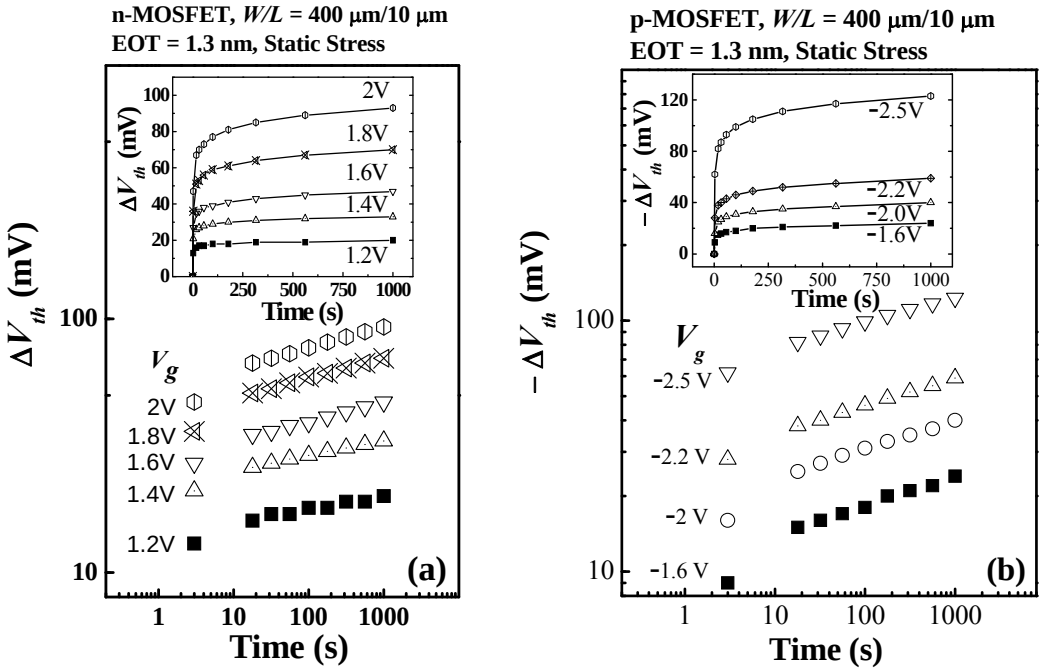
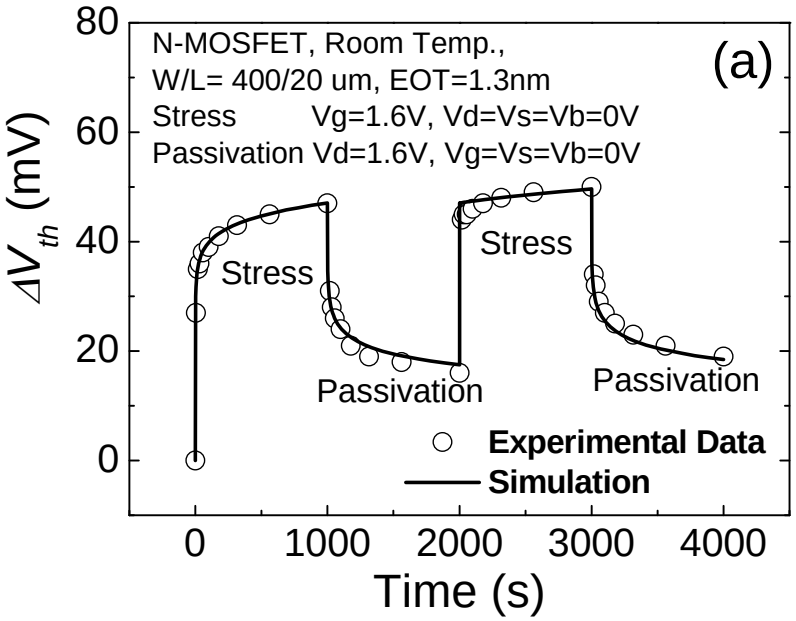
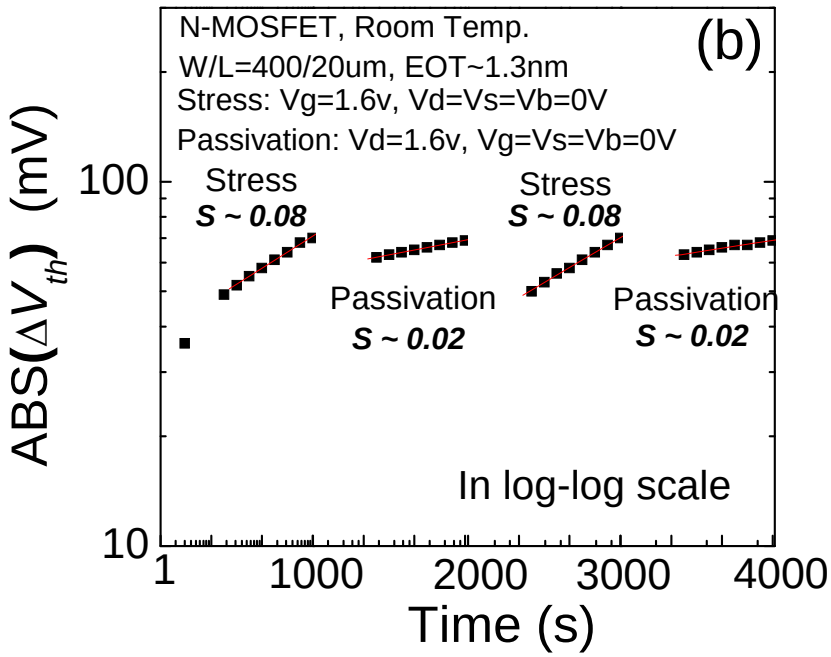


Fig. 5.2: The time evolution of the change in V_{th} (ΔV_{th}) follows a power law dependence on stress time for both (a) n-MOSFETs and (b) p-MOSFETs under various static inversion biases. There exist two components, a fast initial stage followed by a slow stage, as observed in the insets.

In the case of dynamic stresses, as shown in **Figs 5.3 (a)** and **(c)** for n- and p-MOSFETs respectively, although HfO_2 dielectrics exhibit significant V_{th} shifts after stress, a large portion of the V_{th} shift can be recovered in the passivation phase due to charge de-trapping, and the recovery of V_{th} shifts also has a quick initial stage followed by a slower stage. Moreover, in **Fig. 5.3 (b)**, we can notice that there are different slopes in the stress and passivation phase, and the slope in the stress phase is larger than that in the passivation phase, which can result in V_{th} shifts accumulate in every cycle. **Figures 5.3 (a)**, **(c)** and the insets of **Fig. 5.2** also suggest that there could be two different kinds of traps in the HfO_2 gate dielectric: fast traps and slow traps with different frequency dependency. It should be noted that opposite V_{th} shifts are

observed for n- and p-MOSFETs under stresses in the inversion regime, and a smaller $|V_{th}|$ shift in p-MOSFETs as compared to n-MOSFETs is obtained under the same gate stress amplitude.





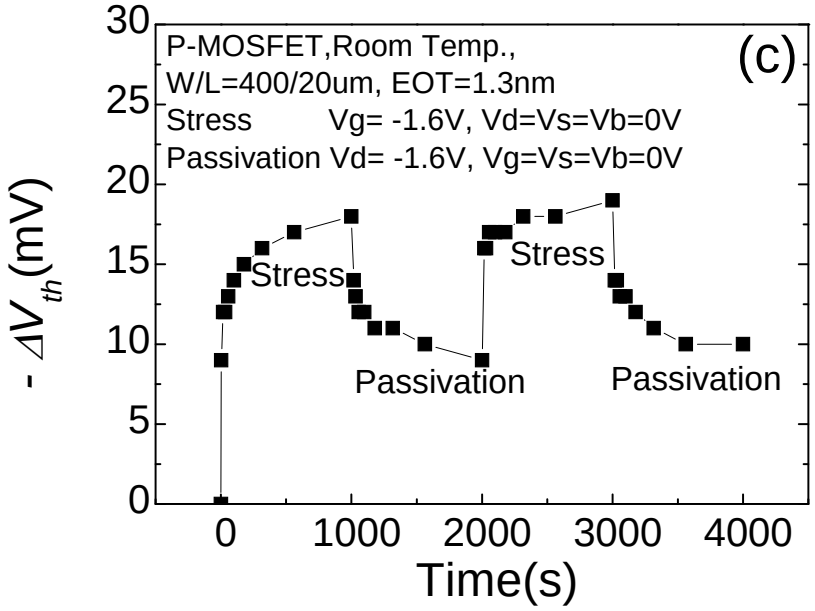


Fig. 5.3: Time evolution of V_{th} shift for (a, b) n-, and (c) p-MOSFETs under dynamic stressing with a duty cycle of 50%. Figure 5.3(b) re-plots the data of each stress/passivation phase from Fig. 5.3(a) in the log-log scale. The V_{th} degradation/recover is due to charge trapping and de-trapping of two different kinds of traps in the HfO_2 gate dielectric, fast traps and slow traps, with different capture and emission rates of carriers. Fast traps appear as sharp rising or dropping edge of ΔV_{th} evolution in the initial stage of each phase. In Fig. 5.3(a), the simulation results for n-MOSFETs V_{th} degradation /recover based on the model proposed in this work are shown.

An examination of the carrier separation results (**Fig. 5.4**) and the corresponding energy band diagrams under inversion bias (**Fig. 5.5**) reveals the nature of the current flowing through the gate dielectric. For n-MOSFETs under inversion, the gate leakage current (J_g) is mainly dominated by electrons from the Si substrate. In other words, only electrons are available for trapping in the HfO_2 dielectric of n-MOSFETs. On the other hand, for p-MOSFETs under inversion, both electrons (from HfN gate) and holes (from the valence band of Si substrate) can be injected into HfO_2 and be trapped, with the hole current component larger than the electron component. Therefore, the V_{th} shift in p-MOSFETs is smaller and has an opposite polarity compared to that in n-MOSFETs due to the net charge trapping effect of both electrons and holes. We have also compared the G_m variation during stressing for n-

and p-MOSFETs and found that G_m degradation was larger for p-MOSFETs than for n-MOSFETS under the same absolute gate voltage (**Fig. 5.6**). This could also be explained by the analysis in **Fig. 5.5**: the remote Coulomb scattering centers [10] responsible for the G_m degradation are provided by both trapped electron and hole charges in the dielectric, therefore larger magnitude of $J_{s/d}$ in p-MOSFETs will induce G_m degradation more seriously. However, the $\Delta G_m/G_m$ variation is significantly smaller than $\Delta V_{th}/V_{th}$ variation in both of static and dynamic stresses, and thus the V_{th} shift is taken as the limiting factor for the device lifetime projection subsequently.

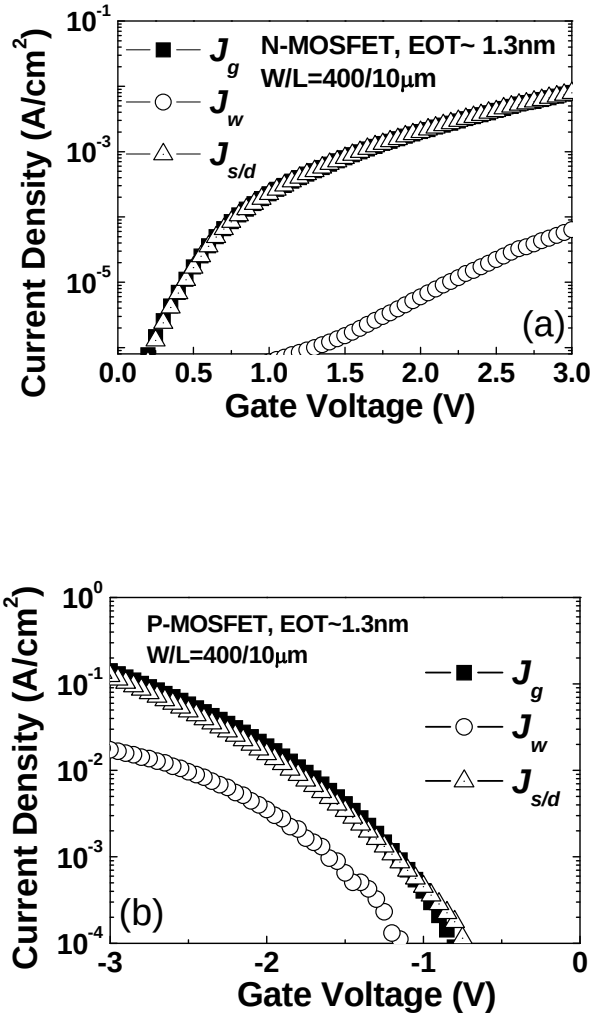


Fig. 5.4: Carrier separation result of (a) n- and (b) p-MOSFETs under inversion biases.

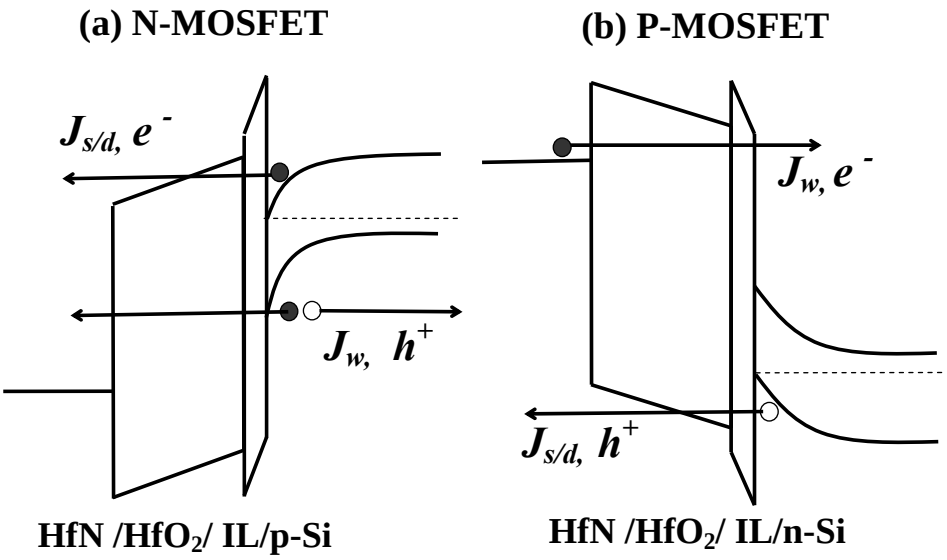


Fig. 5.5: Schematic energy band diagram for (a) an n- and (b) a p-MOSFET under inversion biases, which illustrates the electron or hole leakage currents shown in the **Fig. 5.4**.

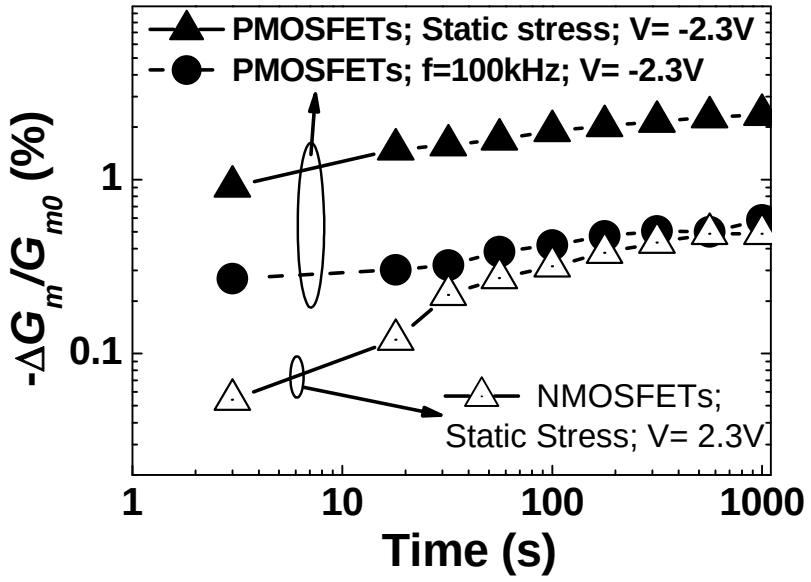
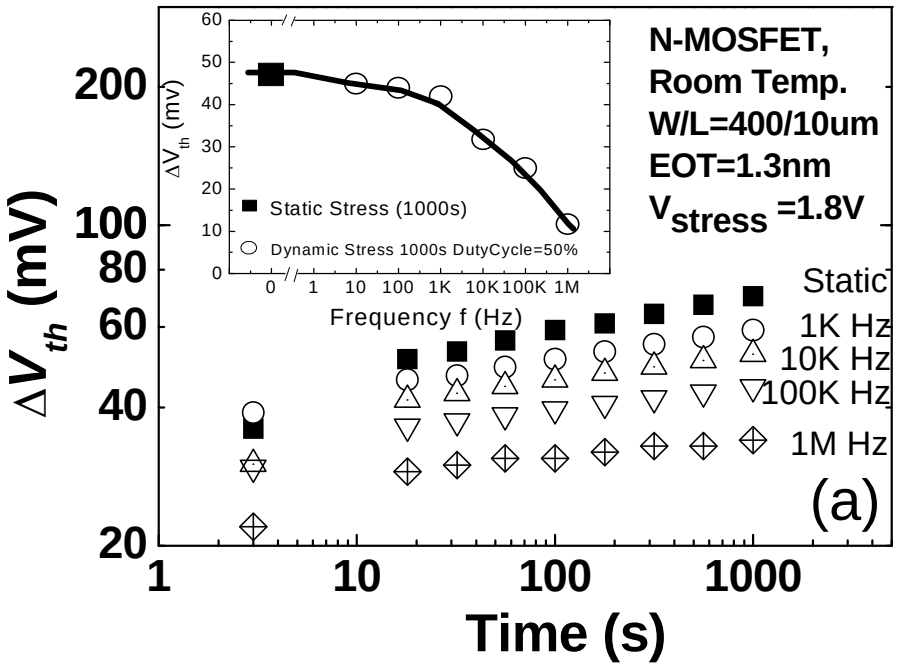


Fig. 5.6: Time dependence of G_m degradation for both n- and p-MOSFETs. Under the same static inversion bias, p-MOSFETs show higher G_m degradation. In addition, with the increase of stress frequency, G_m degradation is improved for p-MOSFETs.

Figure 5.7 examines the frequency dependence of the V_{th} degradation. BTI degradation under dynamic stresses is improved over that under static stresses, and this improvement becomes more significant when the stress frequency is increased (up to 1 MHz as demonstrated in this work). This is in contrast to the case of SiO_2 gate dielectric where the dynamic NBTI results for p-MOSFETs are almost frequency independent [5,8]. Moreover, G_m degradation also improves with increasing of stress frequency as shown in **Fig. 5.6**. It is likely that both ΔG_m and ΔV_{th} are induced by the same physical origin of trapped charge in the HfO_2 dielectric. **Figure 5.8** shows that for n-MOSFETs under dynamic stress, a larger ΔV_{th} is observed at 100°C than at room temperature, which is consistent with [3]. Based on V_{th} shift (ΔV_{th} = 50 mV as the device failure criterion), the 10-year lifetime projection for both n- and p-MOSFETs under various stress frequencies is shown in **Fig. 5.9**. Devices' lifetime is significantly prolonged with the increase of stress frequency. This suggests that BTI induced V_{th} shift may not be the limiting factor in digital ICs employing transistors with HfO_2 gate dielectric.



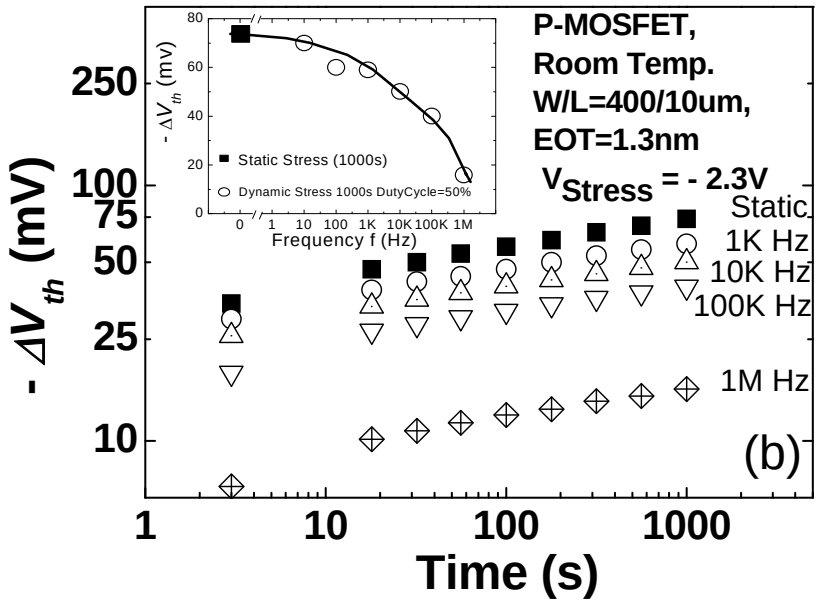


Fig. 5.7: V_{th} shift time evolution for (a) n-MOSFETs, and (b) p-MOSFETs, under static and dynamic stresses of different frequency. Insets of Fig. 5.7(a) and (b) show the ΔV_{th} at the 1000^{th} second, stressed under both static and dynamic stress of different frequencies for n- and p- MOSFETs respectively.

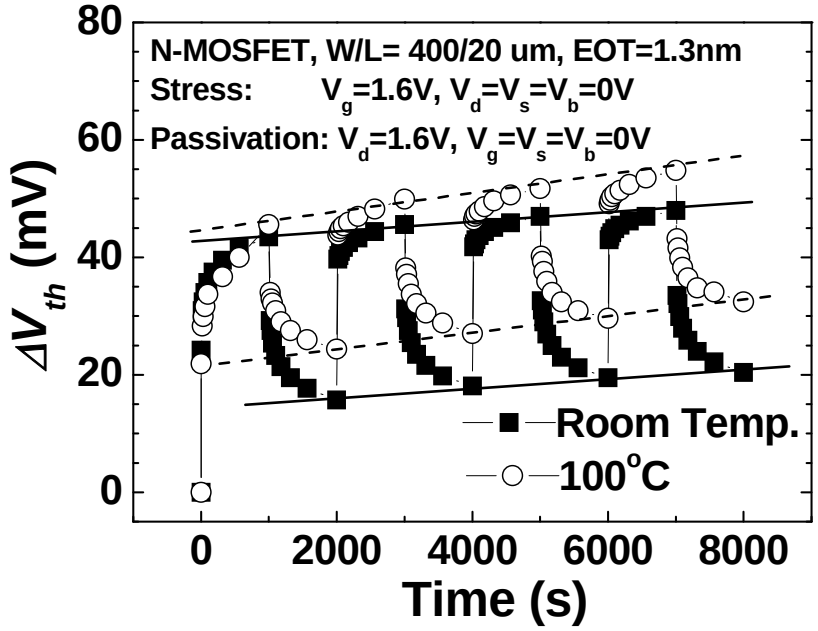


Fig. 5.8: Time evolution of V_{th} shift for n-MOSFETs under dynamic stressing at both room temperature and 100°C.

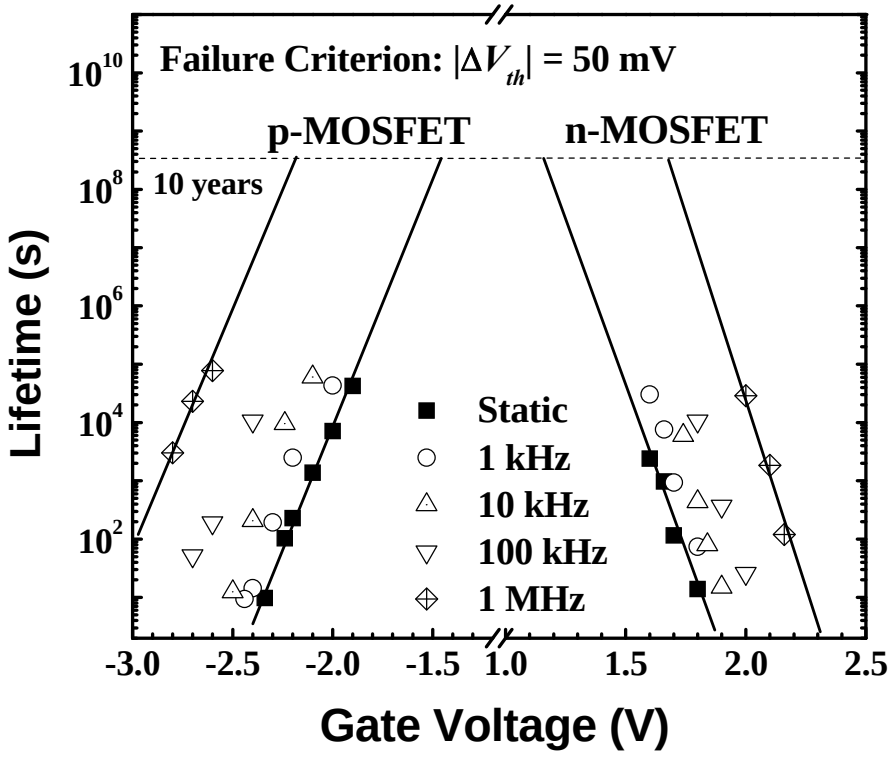


Fig. 5.9: Lifetime projection for n-MOSFETs and p-MOSFETs based on $|\Delta V_{th}|$ = 50 mV as the device failure criterion. To ensure a lifetime of ten years under static stress, the maximum operating voltage is 1.2 V or -1.5 V for n- or p-MOSFETs. When the operating frequency is 1 MHz, the maximum operating voltage is improved to 1.7 V and -2.2 V for n- or p-MOSFETs, respectively.

5.2.4 Model for Dynamic BTI in HfO_2

Here we will only consider the model for the case of n-MOSFETs and it can be easily extended to p-MOSFETs in a complementary way. To explain the frequency-dependence of V_{th} shift in dynamic BTI, we set the number of trapped electrons during one stress cycle in the dynamic BTI experiment as Δn, and the stress time in one stress cycle as Δt (**Fig. 5.10**). When the stress cycle increases from T (T = 1/f, where f is the stress frequency) to 2T, the number of trapped electrons increases from Δn_T to Δn_{2T}. Since ΔV_{th} is reduced with the increase of frequency f when the stressing time is the same, Δn_{2T} must be larger than $2\Delta n_T$. This means that the Δn~Δt relationship should be described by a concave curve (*CC*), as shown in **Fig. 5.10**.

Further, the curve shall become convex (*CX*) for a sufficiently large Δt, so that Δn tends to saturate [3].

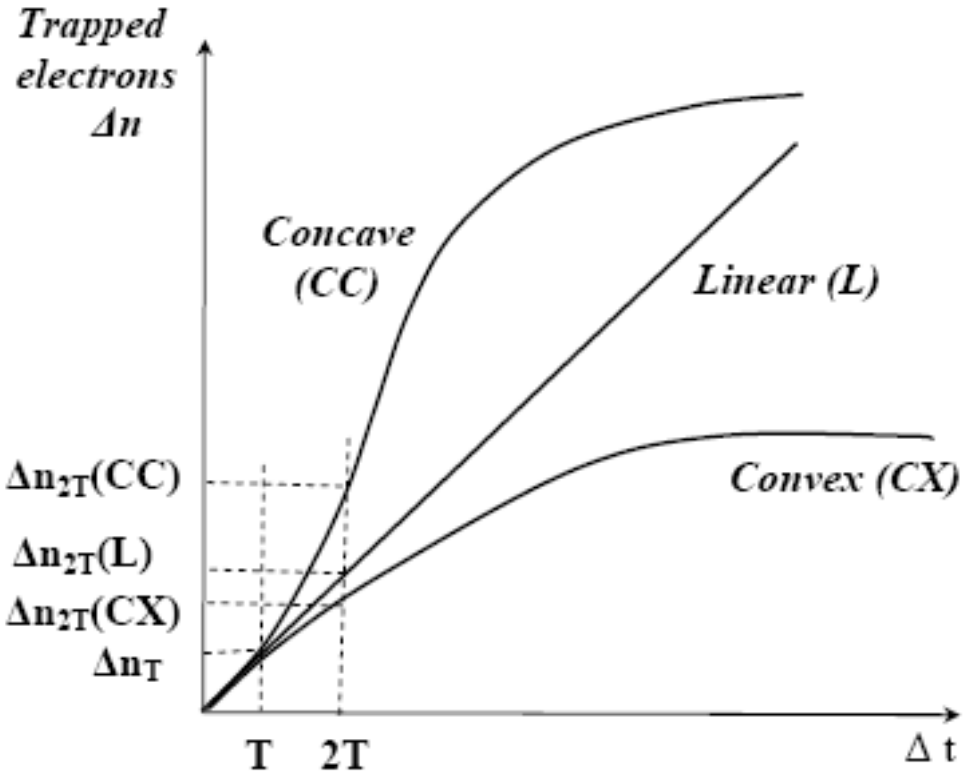


Fig. 5.10: Three possible cases of trapped electrons Δn versus stress time Δt in one cycle of stress phase. Only concave curve (*CC*) can explain the observed frequency dependence of dynamic BTI.

The basic rate equations for electron capturing is $\boldsymbol{dn(t)/dt = [\rho_c(t)-n(t)]/\tau_c}$ [3,11], where $n(t)$, $\rho_c(t)$, and τ_c are the trapped electron density, total electron trap density and capturing time constant, respectively. If the trap density $\rho_c(t)$ is only a constant given by the pre-existing trap density N_{T0} [2-4,11], the solution of capturing equation gives $\boldsymbol{\Delta n = (N_{T0} - n_0)(1- e^{-\Delta t/\tau})}$, where n_0 is the trapped electron density at $\Delta t = 0$. This corresponds to a convex curve (*CX*), or an approximately linear curve for small Δt. The experimentally observed frequency dependence of BTI can only be explained when the trap density $\rho_c(t)$ increases with time t, giving rise to a concave curve (*CC*) for small Δt, as shown in **Fig. 5.11**. The recent experiment also suggested trap generation under stress [12]. We therefore propose pre-existing trap precursors in HfO_2 high-*k* dielectric, which can trap electrons only when they are activated by stress

field, temperature or by carrier injection. This would lead to the effective trap density increases with time. A more sophisticated model to describe the frequency dependence of HfO_2 BTI degradation can be found elsewhere [13]. According to **Fig. 5.2**, we also consider traps having a distribution in the time constant domain, $\rho_c(\tau_c)$ [3]. Further, $\rho_c(\tau_c)$ with two peaks representing fast and slow traps is taken into account (**Figs. 5.2 & 5.3**). Following this model, simulation results match well with the experimental data, as substantiated in **Fig. 5.3 (a)** and **Fig. 5.11**.

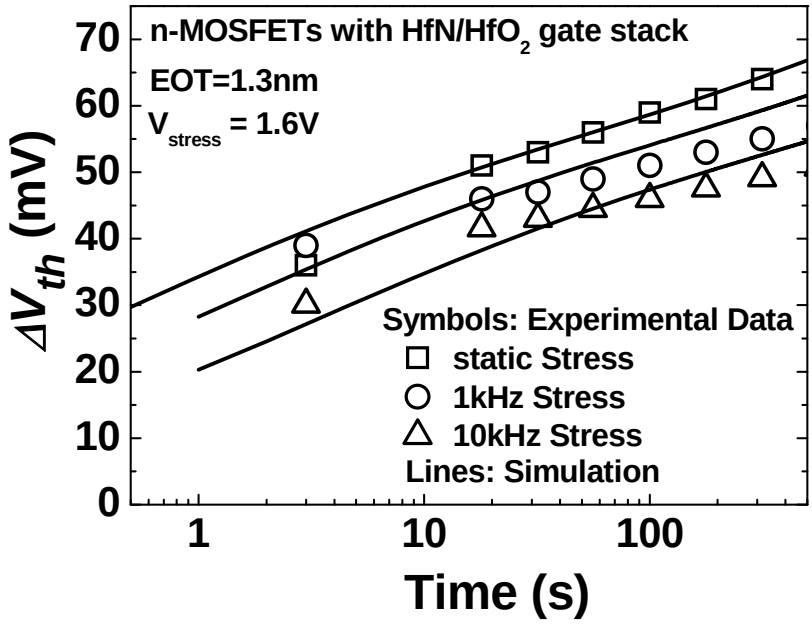


Fig. 5.11: Simulation of static and dynamic BTI based on the physical model accounting for carrier trapping/de-trapping, and generation of new traps.

5.2.5 Summary

We performed a systematic investigation of the V_{th} instability in n- and p-MOSFETs with MOCVD HfO_2 dielectric under both static and dynamic stresses. The V_{th} evolution was found to exhibit a power law dependence on stress time with two components, a fast initial stage followed by a slow stage. For a given gate voltage amplitude and stress time, the BTI degradation is frequency dependent with reduced

degradation at higher stress frequency. As an operating frequency is 1 MHz, the operating voltage to ensure a 10-year BTI lifetime is 1.7 V and -2.2 V, respectively, for n- and p-MOSFETs with HfO_2 of 1.3 nm. Therefore, BTI induced V_{th} shift may not be a limiting factor in practical high-speed digital ICs employing such transistors. Moreover, a model that accounts for carrier trapping/de-trapping process and generation of new traps in HfO_2 dielectric under stress is proposed to explain the above-mentioned phenomena. The calculated results from the model are consistent with V_{th} shifts at different stress voltages for both static and dynamic stresses.

5.3 BTI Instability Investigation in MOSFETs with HfLaO Gate Dielectric

5.3.1 Motivation

As discussed in **Chapter 3**, HfLaO has shown some advantageous material and electrical characteristics, and may become another HfO_2-based high-k candidate in future CMOS technology, especially for n-MOSFETs. Also, the similar results have been reported by other groups [14,15]. However, the BTI characteristics have not been investigated in detail thus far. Therefore, in this part, we provide a comprehensive investigation for the BTI characteristics of HfLaO dielectric as compared to those of HfO_2 dielectric, which is of paramount importance in evaluating the feasibility of this dielectric material.

5.3.2 Experiments

N-MOSFETs with TaN/HfLaO gate stacks were fabricated, where the ratio of La to (La+Hf) in the HfLaO films was 0%, 15% and 50% determined by X-ray photoelectron spectroscopy (XPS). The detailed process conditions for these gate stacks can be found in **Chapter 3**.

The BTI characteristics of HfLaO and HfO_2 were evaluated by both static and transient measurement techniques under dynamic stress in this work, where the former denotes DC measurement technique as employed in the previous sub-section, a conventional technique to study the electrical instability of CMOS devices. The schematic diagram is show in **Fig. 12(a)**. The initial V_{th} was extracted from an initial I_d-V_g measurement. Then a constant stress voltage was applied at gate electrode (V_g) with different stress time, followed by a measurement of I_d-V_g curve again to identify the V_{th} shift after the stress. It is to be noted that there is a delay time (~2 sec in this experiment) during the measurement of I_d-V_g, in which no constant voltage stress was

applied. Since the charged traps due to the constant voltage stress could discharge during this delay time, a shorter delay time is desirable to minimize the impact of discharging. Therefore, we also employ an improved transient (or pulsed I_d-V_g) measurement technique to accurately estimate fast charge trapping and de-trapping in HfO_2 and HfLaO dielectrics [16]. The schematic diagram is shown in **Fig. 5.12(b)**. The V_g and V_d biases can be simultaneously recorded in this technique by using a digital scope and converted into a I_d-V_g measurement. Compared to the static measurement technology mentioned above, the transient measurement technique reduces the delay time for I_d-V_g measurement down to the μs range, dependent on the falling and rising time of the applied pulse (~5 μs in this experiment).

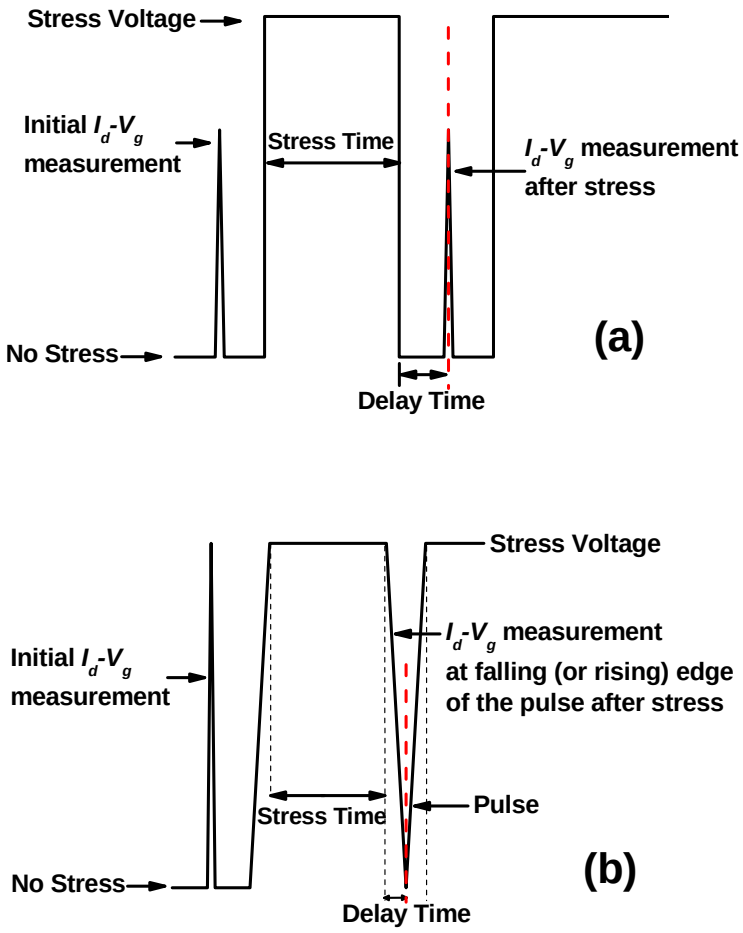


Fig. 5.12: Schematic diagrams for (a) static (DC), and (b) transient (pulsed I_d-V_g) measurement techniques.

5.3.3 Results and Discussion

First, the V_{th} instability in HfO_2 and HfLaO gate dielectrics were examined by applying the static measurement technique. **Figures 5.13** summarizes the V_{th} shifts for all the gate stacks after 1000 s stress with different stress voltages (V_g). Exponential voltage dependence of the V_{th} shifts can be observed for both HfO_2 and HfLaO dielectrics and they show similar voltage acceleration factors. More importantly, the V_{th} shift of HfO_2 can be suppressed after the incorporation of La and much lower (~10 times) V_{th} shift was achieved by HfLaO with 50% La as compared with HfO_2.

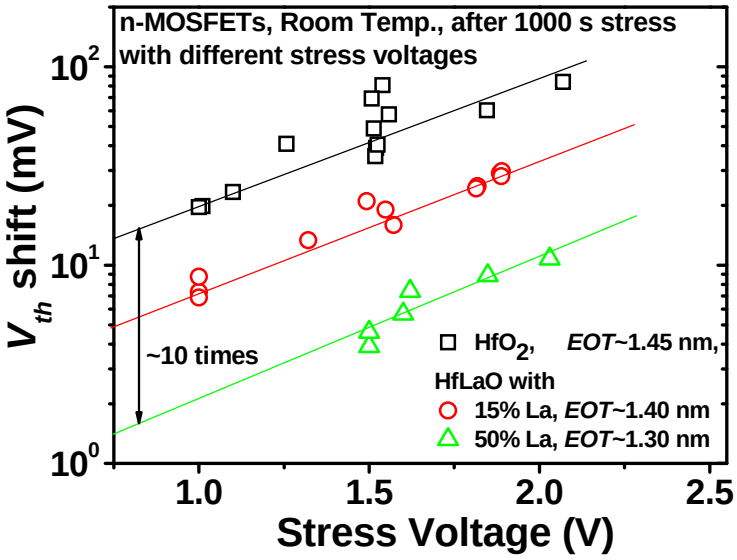


Fig. 5.13: V_{th} shifts for TaN/HfLaO gate stacks with different La% after 1000 s stress with different stress voltages. Exponential voltage dependence can be observed for all the stacks with similar voltage acceleration factors. In addition, much lower (~10 times) V_{th} shift was achieved by HfLaO with 50% La as compared with HfO_2.

In addition, to provide a more impartial comparison, the V_{th} shift was also compared for these gate stacks with a stress voltage as V_{th}+1.5 V, as shown in **Fig. 5.14(a)**. It can be seen that V_{th} shift increases with stress time for all the gate stacks and shows a power law dependence on stress time. In addition, the data clearly show that V_{th} shift at the same stress time is reduced with the incorporation of La into HfO_2

and has around 10 times lower V_{th} shift for HfLaO with 50% La than HfO_2. Similarly, the reduced V_{th} shift for HfLaO dielectrics as compared with HfO_2 can also be found by a transient measurement technique, as shown in **Fig. 5.14(b)**.

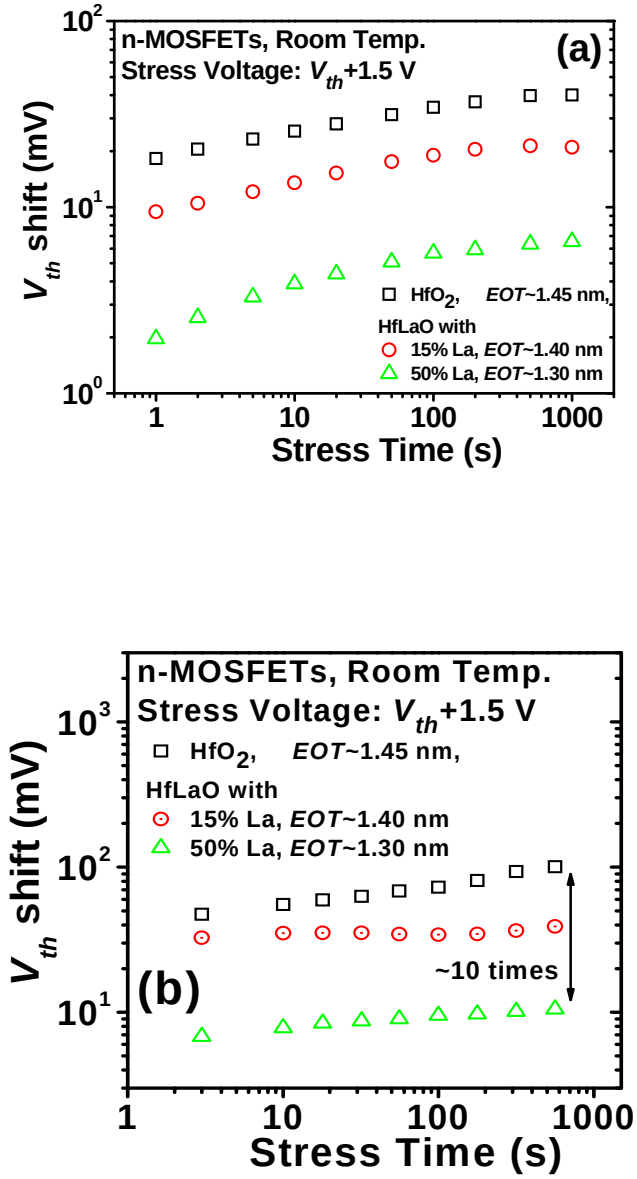


Fig. 5.14: Comparison of the V_{th} shifts due to constant voltage stress of V_{th} +1.5 V in HfO_2 and HfLaO films measured by (a) static and (b) transient measurement techniques, respectively.

However, it should also be noted that the V_{th} shift measured by the transient measurement technique is always higher than that measured by the static measurement technique, as shown in **Figs. 5.15(a)**, **(b)** and **(c)**. This is due to the

conventional static (DC) measurement technique generally with longer delay time, which will underestimate the fast trapping and de-trapping effects in high-*k* gate dielectrics compared to the pulsed I_d-V_g measurement [2,16]. Even so, both results measured by the static and transient measurement technologies clearly show that the charge trapping induced V_{th} shifts in HfLaO films are much lower than that in HfO_2. This indicates that the HfLaO films show better electrical stability and have lower bulk traps compared to HfO_2, which is possibly due to the reduced oxygen vacancy density after the La incorporation into HfO_2, as discussed in **Chapter 3**.

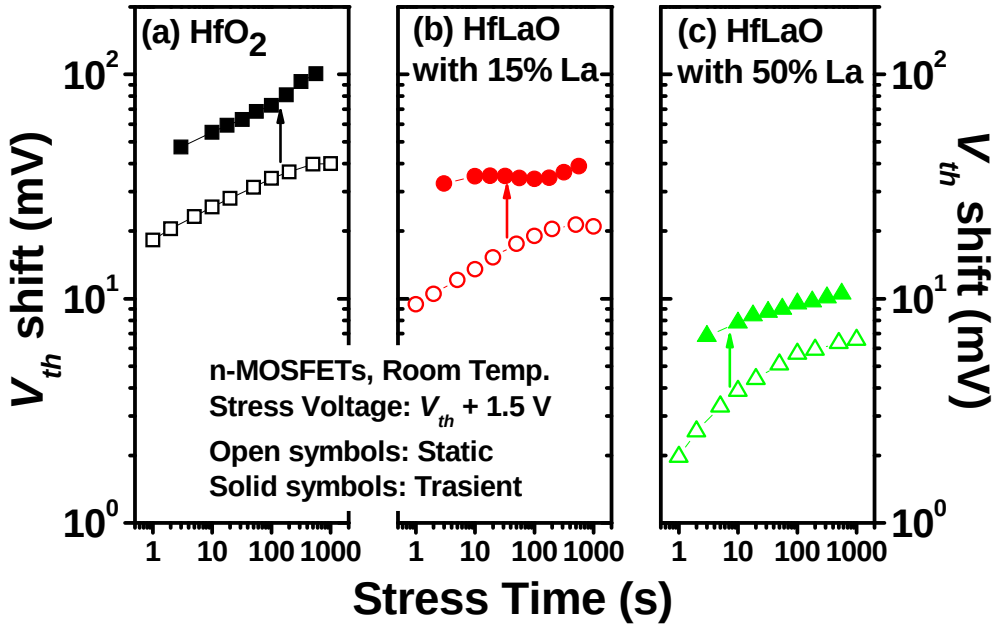


Fig. 5.15: Comparison of the V_{th} shifts for n-MOSFETs with (a) HfO_2, HfLaO with (b) 15% and (c) 50% La gate dielectrics by employing static and transient measurement techniques at a constant voltage stress of V_{th} +1.5 V.

5.3.4 Summary

In this part, we compare the V_{th} shift between HfO_2 and HfLaO dielectrics by employing both static and transient measurement techniques under dynamic stress. The results show that with the incorporation of La into HfO_2, the charge trapping induced V_{th} shift is obviously suppressed, indicating that the HfLaO films possess

better electrical stability and lower bulk traps as compared with HfO_2.

5.4 Conclusion

A systematic investigation of BTI induced V_{th} shift in n- and p-MOSFETs with HfO_2 dielectric under both static and dynamic stresses was first performed in this chapter. The V_{th} evolutions were found to exhibit a power law dependence on stress time with two components for HfO_2 dielectric, a fast initial stage followed by a slow stage. Moreover, for a given gate voltage amplitude and stress time, the BTI degradation is frequency dependent with reduced degradation at higher stress frequency so that the lifetime extracted under the static stress was underestimated. Therefore, BTI induced V_{th} shift may not be a limiting factor in practical high-speed digital ICs employing such transistors.

In addition, the reliability issue for HfLaO dielectrics in terms of BTI induced V_{th} shift was also investigated in this chapter. It is found that the V_{th} shifts, evaluated by either static or transient measurement technique, are obviously suppressed with the incorporation of La into HfO_2. By combining its excellent electrical stability and other characteristics mentioned in **Chapter 3**, HfLaO may become another promising HfO_2-based high-*k* candidate in future CMOS technology.

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Chapter 6

Conclusions and Recommendations

6.1 Summary and Conclusions

This work has sought to address some of the most pressing issues in advanced gate stack technology. As the time of writing this dissertation, the 65 nm CMOS technology is being introduced into production, and the 45 nm CMOS technology is under development at most leading semiconductor manufacturers. Concurrently, the whole semiconductor community is initiating the research and development efforts for the 32 nm technology node and beyond, where it is likely that some of the materials and process integration challenges discussed herein must be addressed. The task for finding replacement materials for SiON gate dielectric and poly-silicon gate electrode is by no means trivial. Numerous problems related to the material selection and the process integration of high-*k* gate dielectrics and metal gates (MGs), such as the thermal stability, mobility degradation, charge trapping induced threshold voltage (V_{th}) instability, and unacceptably high V_{th} induced by Fermi Level pinning (FLP) effect between dielectrics and electrodes, need to be addressed before a suitably advanced gate stack solution can be transferred to manufacturing.

As discussed in **Chapter 3**, a gate dielectric material HfLaO was investigated systematically for the first time. By incorporating La into HfO_2 film, the crystallization temperature and *k* value of the film are increased substantially, and better thermal stability subsequently. N-MOSFETs fabricated with HfLaO exhibit superior device characteristics compared to n-MOSFETs fabricated with pure HfO_2, including an enhancement of ~70% for drive current and electron mobility and one order reduction of dielectric charge trapping induced V_{th} shift. We have also found the effective work function (EWF) of TaN (HfN or TiN) can be effectively tuned from Si

mid-gap to the conduction band edge of Si by optimizing the La composition in HfLaO to meet the n-MOSFET work function requirement. Simultaneously, the Si valence band edge EWF can be obtained by employing HfLaO and Pt (or Ru), which is very suitable for p-MOSFETs. All these excellent properties observed in HfLaO gate dielectric suggest that it could be a very promising candidate as the alternative gate dielectric for future CMOS application. In addition, to interpret the significant EWF shift for both n- and p-type MGs, a specific model based on the interfacial dipole theory between the gate electrode and the gate dielectric is proposed, wherein the effects of different electronegativities among materials involved in the gate stack and oxygen vacancy (V_O) density in the dielectric film on the EWF of MGs are highlighted and it seems the effect caused by different electronegativities is more significant for n-type MGs and the effect of V_O is more obvious for p-type noble metals. Experimentally, this model has been demonstrated by other gate stacks including more MGs and lanthanide elements incorporated HfO_2 dielectrics. Therefore, this model regarding the metal-dielectric interface could be useful for work function tuning and interface engineering between MGs and high-*k* dielectrics in future MOS devices.

In addition, we proposed two integration schemes for dual MG CMOS technology in **Chapter 4** and both of them belong to gate first integration process. The first scheme involves novel gate stacks to create wide enough EWF tunability by using a high-temperature metal inter-diffusion technique. In this process, HfLaO dielectric layer is employed to increase the tunable EWF range based on the results shown in **Chapter 3**. Furthermore, to avoid the gate dielectric from being exposed during the metal etching process, the original Ru capping layer is kept throughout the process flow. This addresses the etching damage issues associated with the conventional direct-etching integration scheme. More importantly, the EWF of the Ru layer can be modulated by a high-temperature metal inter-diffusion between Ru and upper TaN layer, and this diffusion process is compatible with the conventional gate-first CMOS process flow. By using this integration scheme, the EWF of these

gate stacks has a wide EWF tunable range from 3.9 eV to 5.2 eV. These results make TaN/Ru (for n-MOSFETs) and Ru (for p-MOSFETs) on HfLaO gate stacks promising candidates for future CMOS integration technology. The other novel integration scheme is proposed by positively utilizing unavoidable FLP effect in gate stacks involving high-*k* dielectrics and gate electrodes (poly-Si or MGs). By incorporating La (or other lanthanide elements) and Al into selected MN_x (TaN, HfN or TiN), the EWF of MN_x clearly shifts to conduction band edge and valence band edge of Si respectively, which is very suitable for bulk-Si CMOS technology. This phenomenon is believed to be due to the change of interface states resulting from the incorporation of La or Al, and is independent of whether they are at gate electrode side or gate dielectric side. These proposed integration schemes may provide some useful discussions to address some of the major issues associated with the conventional integration schemes, and are believed to make a contribution to the development of the dual MG integration processes for future bulk-Si CMOS technology.

Finally in **Chapter 5**, a systematic investigation of bias temperature instability (BTI) induced V_{th} shift in n- and p-MOSFETs with HfO_2 dielectric under both static and dynamic stresses was first performed. The V_{th} evolution was found to exhibit a power law dependence on stress time with two components, a fast initial stage followed by a slow stage. For a given gate voltage amplitude and stress time, the BTI degradation is frequency dependent with reduced degradation at higher stress frequency. At an operating frequency is 1 MHz, the operating voltage to ensure a 10-year BTI lifetime is 1.7 V and -2.2 V, respectively, for n- and p-MOSFETs with HfO_2 of 1.3 nm. Therefore, BTI induced V_{th} shift may not be a limiting factor in practical high-speed digital ICs employing such transistors. Moreover, a model that accounts for carrier trapping/de-trapping process and generation of new traps in HfO_2 dielectric under stress is proposed for the first time to explain the above-mentioned phenomena. The calculated results from the model are consistent with V_{th} shifts at different stress voltages for both static and dynamic stresses. In addition, the reliability issue for HfLaO dielectrics in terms of BTI induced V_{th} shift was also

investigated in **Chapter 5**. It is found that the V_{th} shifts, evaluated by either static or transient measurement technique, are obviously suppressed with the incorporation of La into HfO_2. By combining its excellent electrical stability and other characteristics mentioned in **Chapter 3**, HfLaO may become another promising HfO_2-based high-*k* candidate in future CMOS technology.

6.2 Recommendations for Future Work

The work in this thesis has been very exploratory. More detailed investigation and more rigorous characterization will be necessary to further optimize the processes described in this thesis. Suggestions for future work will be directly or indirectly related to the concerns described earlier in this thesis.

In **Chapter 3**, the effects of different electronegativities among materials involved in the gate stack and V_O density in the dielectric film on the EWF of MGs has been highlighted and it seems the effect caused by different electronegativities is more significant for n-type MGs and the effect of V_O is more obvious for p-type noble metals. However, there is still no clear guideline to precisely engineer the EWF for MG and high-*k* gate stacks, which would be an important question for discussion in future work. In addition, for the integration schemes proposed in **Chapter 4**, the etching and cleaning issues need to be well optimized in order to examine the feasibility of these gate stacks in short-channel transistor fabrication.

Moreover, Ni-based fully silicided (FUSI) gate electrodes have been investigated comprehensively for next generation CMOS technology due to their ability to eliminate poly-Si depletion and compatibility with the conventional CMOS process [1-5]. The initial Si gate in conventional Ni-based FUSI gate electrode is commonly deposited using a CVD tool. However, it was previously reported that flat band voltage (V_{fb}) for both PVD n^+ and p^+ poly-Si/Hf-based dielectric gate stacks shifts in the same direction as compared to CVD poly-Si gates [6]. Another report shows that an inserted PVD Si layer before CVD Si deposition can effectively reduce

high leakage currents [7]. However, the impact of different Si deposition process on Ni-based FUSI gate/Hf-based dielectric stacks has not been investigated. In addition, the EWF tunability for MGs by incorporating La into HfO_2 has been experimentally demonstrated in **Chapter 3** and there is still no publications regarding the effect of HfLaO on EWF for the gate stacks involving FUSI gate electrode. Therefore, the effects of both Si deposition process and La incorporation on the performances of FUSI gate are also worthy to investigate in future research, such as EWF tunability and gate leakage current.

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C) Patents

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