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STRUCTURAL DESIGN AND OPTIMIZATION OF 65NM Cu/LOW-K FLIPCHIP PACKAGE

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A THESIS SUBMITTED
FOR THE DEGREE OF MASTER OF ENGINEERING
DEPARTMENT OF MECHANICAL ENGINEERING

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PREFACE

This thesis is submitted for the degree of Master of Engineering in the Department of Mechanical Engineering, National University of Singapore, under the supervision of Professor Andrew A. O. Tay and Dr. Kripesh Vaidyanathan (IME). No part of this thesis has been submitted for any degree at any other University or Institution. As far as this candidate is aware, all work in this thesis is original unless reference is made to other work. Parts of this thesis have been submitted for publication in the conference proceedings and international journals as stated below:

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Abstract

In the future, copper/low-k structures are the desired choice for advanced integrated circuits (ICs). The low-k materials improve chip speed and performance by allowing manufacturers to achieve smaller and higher density semiconductor devices with multilayer interconnect structures, especially for memory devices. Nevertheless, reliability might become a concern due to the considerably lower strength and greater coefficient of thermal expansion (CTE) of the low-k materials. The low-k materials have intrinsically lower modulus, lower fracture toughness and poorer adhesion compared to other dielectric materials. Packaging is suspected to affect the reliability of Cu/low-k interconnects. The induction of interfacial delamination along low-k material interfaces has been widely observed.

In the present study, a 2D plane strain analysis was performed to investigate the reliability of Chartered's C65nm 21x21mm 9metal Cu/ low-k, chips with 150um interconnect pitch in a FCBGA package. A series of parametric studies was performed by using Polymer Encapsulated Dicing Lane Technology (PEDL) to reduce 1 layer of FSG, variation of Cu post height, die thickness, substrate thickness, and underfill selection. The results obtained from the reduction of the stress in the low-k structure and the inelastic energy in the solder bumps modeling is useful to formulate design guidelines for packaging of large dies.

Next, three parametric cases involving different geometries of solder joints were analyzed using 3D finite element simulation: (A) All 20 rows with spherical solder joints,

(B) 10 hourglass joints followed by 10 spherical joints, and (C) 10 spherical joints followed by 10 hourglass joints. It was found that Case C gave the lowest inelastic energy dissipation (ΔW) implying that the solder joints for Case C will have the longest fatigue life. It was also found that Case C gave the lowest maximum stress in the low-k material and it was further shown that reliability will be enhanced by decreasing die thickness and substrate thickness.

List of Abbreviations

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CTE – Coefficient of thermal expansion………………..3, 4, 7, 11, 12, 15, 20, 28, 39, 40, 41, 46, 49, 49, 52, 60, 61, 68

ILD – Inter-dielectric layer……………………………………………………………..5

MVCC - Modified virtual crack closure………………………………………………..5

FSG – Fluorinated silicate glass…....6, 9, 27, 28, 30, 32, 33, 35, 36, 41, 45, 48, 52, 60, 61

PEDL - Polymer Encapsulated Dicing Lane...6, 7, 8, 33, 34, 35, 40, 41, 42, 45, 46, 47, 60

UBM – Under bump metallization……………………………………………………..1, 6

ICs – Integrated circuits………………………………………………………………...7

MSL – Moisture Sensitivity Level…………………………………….……..7, 9, 31, 41

TC – Temperature cycling…………………………………….7, 31, 32, 35, 36, 39, 41, 42

FCBGA – Flip chip ball grid array……………………………………………………..6

Mx – Metal x where x = 1,2,3,4,5,6,7……………………………………………………10

Vx – Via x where x = 1,2,3,4,5,6,7………………………………………………………10

LM – Last metal…………………………………………………………………………10

LV – Last via……………………………………………………………………………10

PCB - Printed circuit board……………………………………………………..2, 11, 12

FEA – Finite element analysis………………………………...4, 25, 32, 33, 35, 37, 46, 47

DNP - Distance to the neutral point……………………………………………….15, 41

BCB – Benzocyclobutene……………………………………………..33, 34, 41, 47, 60

PI – Polyimide…………………………………………………………………………...28

CSAM – C-Mode Scanning Acoustic Microscopy……………………………31, 41, 42

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CHAPTER 1

INTRODUCTION

1.1 Background on lead-free low-k filpchip Packaging

Since February 13, 2003, use of lead in electronic products has been prohibited by law in the EU (European Union). The implementation date was July 1, 2006. This means that, after July 1st, all the electronic products containing lead (except those with exemptions) cannot be put into the market of EU. At the time being, China is considering to have her own lead-free law. Recently, packages such as PBGA (plastic ball grid array), CSP (chip scale package), and especially WLCSP (wafer level chip scale package) have been very popular for consumer, computer, communication and mobile products. Most of these packages use solders as their interconnects, thus they are affected by the lead-free regulations [1].

The worldwide trend toward lead-free electronics, as well as the demand for high melting solders for the automotive sector, has pushed the industry to alternative solder systems. One concern regarding these new systems is their reliability. Because of slightly higher yield stress and slightly lower fatigue ductility of SnAgCu compared with $SnPb_{37}$, fatigue life and failure mechanisms are assumed to be nearly identical for both solder alloys. In practice, the thermal history and geometry of solder joints play a dominant role in their fatigue life, not so much the alloy composition. For electroless nickel UBM, Popelar et al. [2] demonstrated an excellent shear performance for $SnPb_{37}$, as well as for

$Sn_{95.5}Ag_{3.8}Cu_{0.7}$ solder bumps. In addition, underfilling, typically needed for reliable performance of any flip-chip product on laminate PCB, will remove much of the stress from the solder joint, thereby extending lifetime to the desired range [3].

As flip-chip packaging achieves growing acceptance throughout the industry, flip-chip producers are faced with solving manufacturing challenges for optimum yield and throughput. Although flip chip assembly is not a new technology, it is gaining increasing popularity as a packaging strategy due to the benefits it can provide. By using the entire surface of the die for establishing interconnects, the need for wire bond interconnect is eliminated and package size can be reduced [4].

More importantly for high-performance applications, directly connecting the die to a substrate or board greatly shortens the signal path while reducing the interconnect inductance and capacitance, all of which serves to greatly improve electrical performance. Microprocessor designs are getting complex and challenging as we move from one generation to the next. This is due to the need to get higher clock speeds and to have more functionality built into the chip. The number of transistors per unit area keeps increasing while the chip size is shrinking. Continuous improvements in manufacturing design rules and new process technologies are required to deliver a cost-effective and high-performance products in the marketplace. Low-k materials have very low mechanical strength compared to the traditional dielectric films due to their porous nature, which results in lower cohesive strength [5]. These lead to a unique set of mechanical issues when low-k dies are packaged. The low-k materials also have weak adhesion properties and make it more difficult to stack them together to form multilevel

stacks during the fabrication process. In an extreme case, thermal stress on the die alone can lead to separation at the interfaces or even cohesive fractures in the film. The interfacial stress induced in the layers during fab processing only gets worse when they are packaged, due to coefficient of thermal expansion (CTE) mismatch between silicon (CTE 3 ppm) and ceramic (6 ppm) or organic (15 ppm) buildup substrate. In addition, the rigidity or modulus of the substrate plays an important role. It is generally accepted that ceramic substrate/die mismatch is tolerable. In addition, due to its rigid nature the die does not exhibit camber when packaged in the ceramic package, thus the resulting stress induced in the low-k stack is tolerable. However, the ceramic package suffers from lower performance and supports lower total power. This is due to the high dielectric constant (K=10) and higher internal electrical resistance due to resistance of Molybdenum or Tungsten conductors. Thus, the only realistic option is to package the die in an organic buildup substrate.

Organic substrate/die mismatch is significant. In addition, due to its lower rigidity it can flex more relative to the ceramic substrate. Typically, to enhance fatigue life of flip chip solder joints, an epoxy material known as underfill is dispensed between the die and the package [6,7]. Underfill acts to reduce shear stress on the solder joints exerted due to the CTE mismatch. These materials are typically high modulus and cured at temperatures from 100 to 200 C. On the cool-down from the curing temperature, the CTE mismatch translates into bending of the die. This camber is permanent when the assembled package is cooled to room temperature. As one can imagine, the multilevel-stacked low-k film is subjected to bending stresses. These bending stresses can lead to both adhesive and cohesive fracture of the film. Fractures thus created can propagate in any direction under

further stress, resulting in disruptive mechanical and electrical failures of the die. During temperature cycling, CTE mismatch between the silicon and package cause delamination and cracking at the low-k to metal interface within a few hundred cycles, raising a major concern on reliability of the product. This is quite challenging and is one of the key problems faced by the industry today. This thesis will focus on the improvements in chip and package technologies, and enhancements in the assembly process that have a potential to overcome low-k packaging issues.

Package, silicon, and assembly processes form a mutually interactive system. When designing the silicon, it is essential to consider the manufacturability of the entire system for a successful product in the marketplace. Our study started with FEA modeling of the silicon and the package with underfill [8].

The assembly process used to package the low-k die into the organic package also plays a crucial role. This begins with sawing the wafer into individual dies. This has been traditionally done by using mechanical blades. These generate micro and macro cracks at the edges of the die into the scribe alleys. These cracks could enhance the propensity of propagation along the boundary between the low-k film layers. Another area, as previously mentioned, is designing the optimal underfills. This consists of customizing mechanical properties of the underfill to achieve low stresses in the die, as well as processing of underfill to minimize the stress induced during temperature cycling that could be detrimental to the mechanical integrity of the low-k stack.

1.2 Motivation of the Work

To reduce the stresses in the ILD, the materials and processing of the packaging play an important role. Film adhesion to the metal is very critical to reduce interfacial separation. There is an optimum modulus and adhesion strength that allows for lower stresses and can be arrived at by running several experiments on different film types. Unfortunately, there are many films available in the marketplace, and selecting the correct film that provides both electrical and mechanical performance can take a long time at huge expense. Typically, the cracks start at the edges of the die, and one needs to optimize the design on the flip chip die to stop the propagation of cracks induced by either mechanical or thermal stresses. Further analysis on the crack driving forces for relevant interfaces in Cu/low-k interconnect structures are required. The modified virtual crack closure (MVCC) technique was used to calculate the energy release rate in 3D-IC Cu/low-k interconnect structures.

Lead-free materials show brittle behaviour based on creep fatigue at high temperature. Experiments show that the trends in lead-free solder joint reliability are cycling-condition and package dependent. For long dwell times and stiff packages, lead-free assembled components show an inferior reliability compared to eutectic SnPb. In order to reduce the inelastic energy dissipation per temperature cycle induced in the solder joints, and hence improve the fatigue life of the joints, studies have to be made on the effect of chip-to-substrate interconnect compliance.

1.3 Objective and Scope

A 2D plane strain analysis was performed to investigate the reliability of Chartered's C65nm 21x21mm 9metal Cu/ low-k, chips with 150um interconnect pitch in a FCBGA package. The reliability performance of lead-free solder bump vs Cu post interconnect will be compared. The feasibility of reducing one layer of FSG by PEDL will also be investigated. Polymer Encapsulated Dicing Lane Technology (PEDL) concept is used to address the dicing challenges of Cu/low-k and simultaneously improve the reliability performance by reducing the corner stress in the Cu/low-k. We will perform modeling stress levels in Cu/low-k structure using Cu post vs lead free solder bump. We will do a reliability assessment of Ti/Ni/Cu/Au UBM Vs Cu post interconnects and 2 layer FSG Vs one layer FSG with PEDL in front end/back end integration.

Next a 3D plane-strain finite element analysis was performed on a diagonal strip of a 21mmx21mm Cu/low-k chip. There are 20 rings of solder joints (height 60um, pad diameter 80um) around the periphery of the chip at a pitch of 150um which gives a total number of interconnects of about 11000. The distance between the outermost row of solder joints from the edge of the die is 150um. Three parametric cases involving different geometries of solder joints were analyze: (A) All 20 rows with spherical solder joints, (B) 10 hourglass joints followed by 10 spherical joints, and (C) 10 spherical joints followed by 10 hourglass joints.

CHAPTER 2

LITERATURE REVIEW

In the future, copper/low-k structures are the desired choice for advanced integrated circuits (ICs). The low-k materials improves chip speed and performance by allowing manufacturers to achieve smaller and higher density semiconductor devices with multilayer interconnect structures, especially for memory devices. Nevertheless, the reliability might become a concern due to the considerably lower strength and greater coefficient of thermal expansion (CTE) of the low-k materials. The low-k materials have intrinsically lower modulus, lower fracture toughness and poorer adhesion compared to other dielectric materials. Packaging is suspected to affect the reliability of Cu/low k interconnects. The induction of interfacial delamination along low k material interfaces has been widely observed.

Under the Cu/low-k packaging program, IME has developed Polymer Encapsulated Dicing Lane Technology (PEDL) [9] to address the dicing challenges of Cu/low-k and simultaneously improve the reliability of the packages (MSL, TC performance) by reducing the corner stress of the Cu/low-k die. Fig. 2.1 shows the schematics of PEDL process flow. Finite element model is built by using PATRAN and ABAQUS. Overall finite element mesh for interconnect is optimized. All the prior simulations have shown that the local maximum shear stress concentration is located at the outermost corner of the silicon die, i.e. at the interface of underfill and die corner. This is due to the stress singularity at the corners of the die. This stress is critical and it

may cause delamination of underfill material, which in turn causes the solder bump failure. Low-k dielectric film which is encapsulated with the polymer dielectrics, gives better moisture and reliability performance.

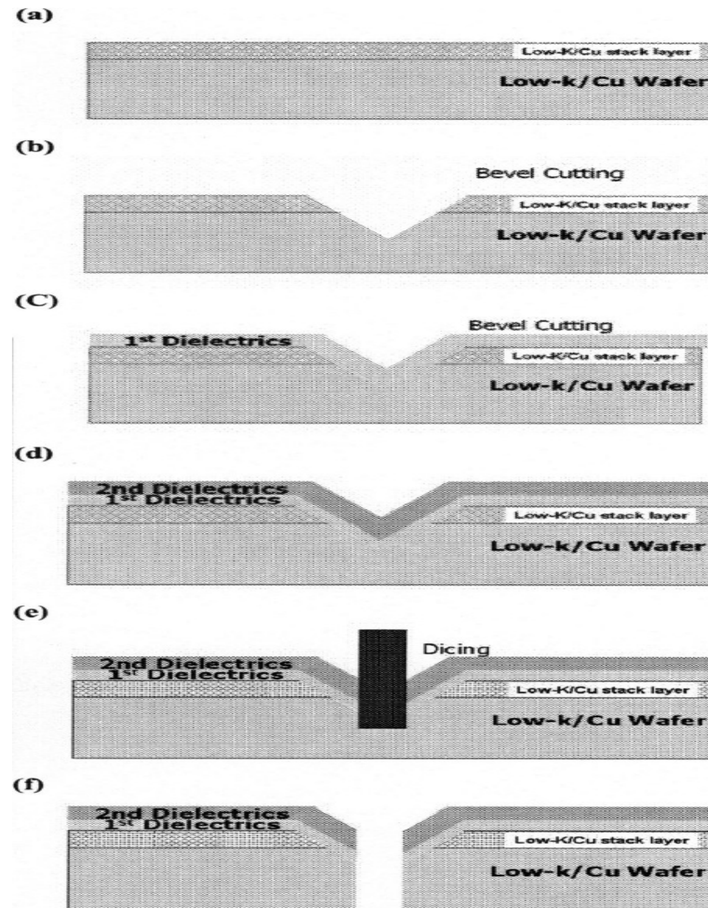


Fig. 2.1 Schematics of PEDL process flow

Ki-Bon Cha [10] (refer to Fig. 2.2) showed that the sharp edge of the chip can create high internal stress and cause crack initiation. When the temperature difference between the intemal chip and outside epoxy moulding compound is large, a higher shear stress will be generated at the chip-molding compound interface

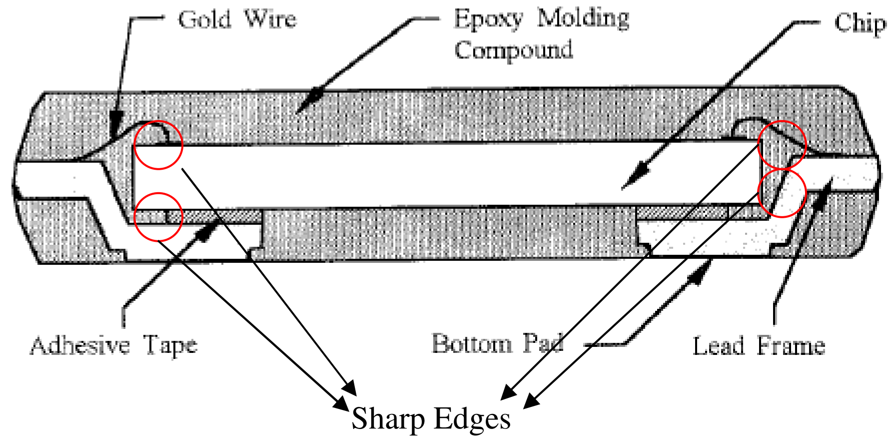
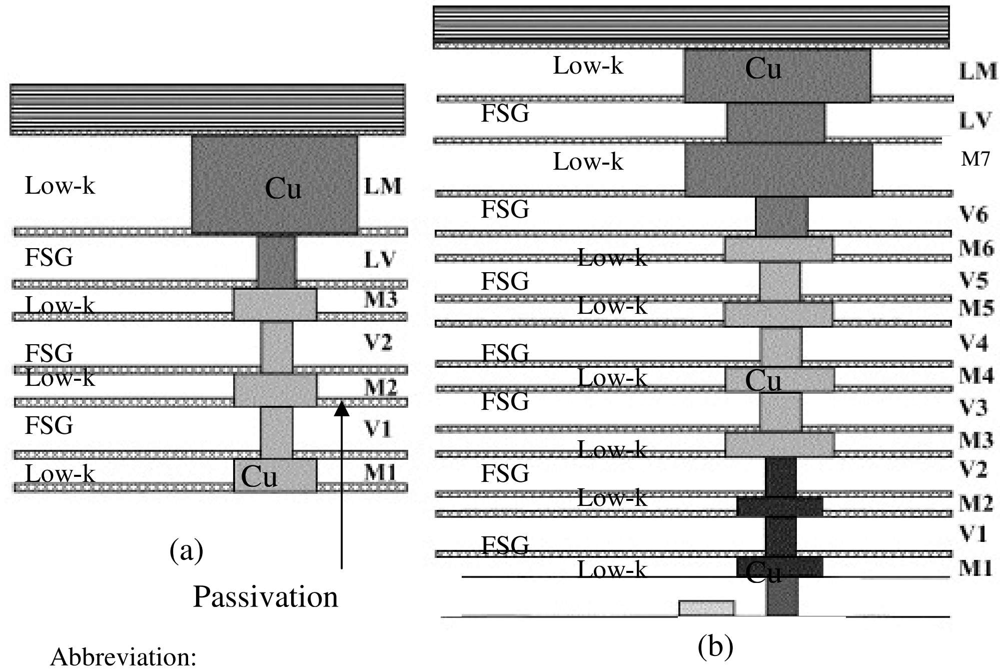


Fig. 2.2 The cross-sectioned View of the BLP Package

He also demonstrated that reliable MSL level 3 lead free 35x35mm FC BGA package with a 15x15mm 4metal Cu/low-k die. Placing low-k material at this high stress location will negatively impact the reliability of the entire low-k stack.

The impact of increasing number of metal layers has also been evaluated [11]. From Fig. 2.3, thicker metal layer (8-metal layer) structures are more prone to fracture than thinner metal layer (4-metal layer) structures as shown in Fig. 2. 4. Fig. 2. 4 shows the crack driving force, J-integral, computed from finite element analysis. A greater value will likely to cause delamination between the interfaces of low-k and passivation. Low-k has a weaker adhesion properties as compared to FSG. The figure shows that the low-k at the last metal layer has the highest value which indicate that delamination is likely to occur at the last interface of low-k and passivation.



Abbreviation:

Mx – Metal x where x = 1,2,3,4,5,6,7, LM – Last metal
Vx – Via x where x = 1,2,3,4,5,6,7, LV – Last via
FSG – Fluorinated Silicate Glass

Fig. 2.3 (a) 4-metal Cu/low-k test structure, (b) 8metal Cu/low-k test structure

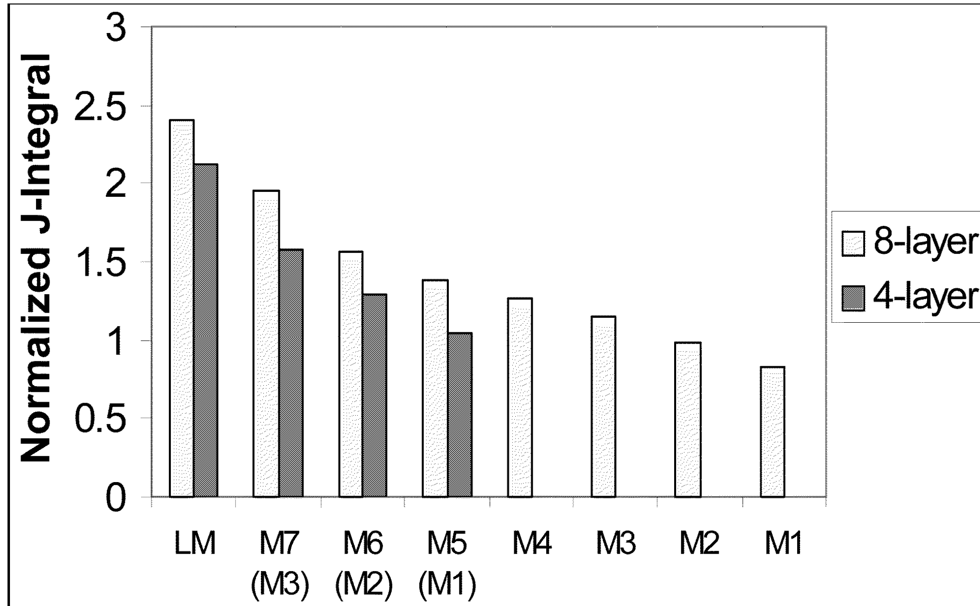


Fig. 2.4 Crack driving force with low-k at last metal.

The effect of having low-k or SiO at the last metal layer is investigated with an interface-fracture-mechanics-based finite element analysis (refer to Fig. 2.5). The critical interface is the last metal/passivation interface. Placing low- material at this high stress location will negatively impact the reliability of the entire low- stack

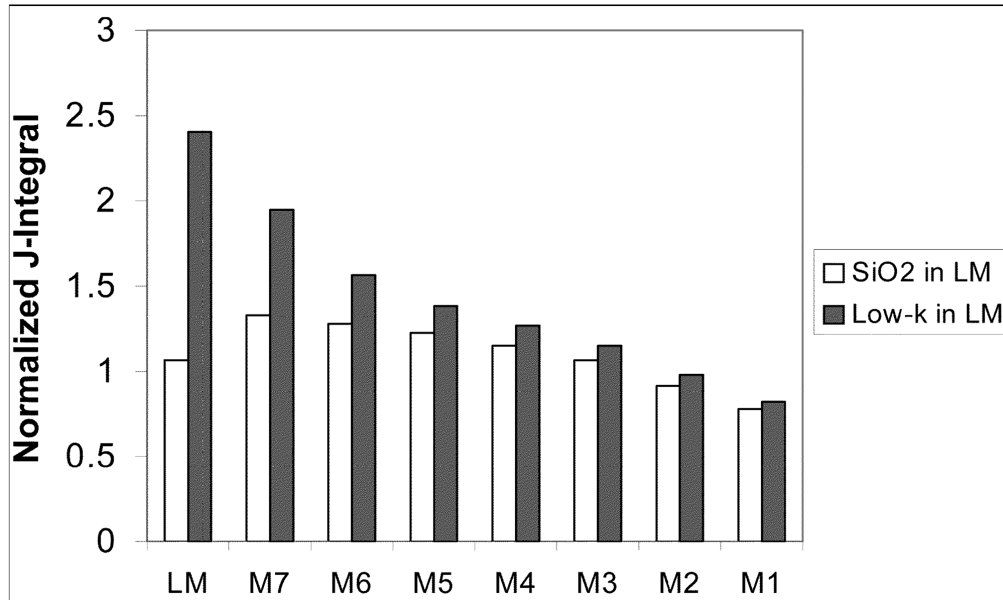


Fig. 2.5 SiO versus low-k at last metal for eight-metal-layer structures.

A solution to reduce the delamination of low-k material is to use tiles or slots in the copper low-k structure to effectively reduce the available area for crack growth [12]. This has been seen in testing where delamination was eliminated when tiling was used. At present 9-metal Cu/low-k on a large die (21X21mm) is still a novel concept in the industry.

It is well known that the coefficient of thermal expansion (CTE) mismatch between the package and the printed circuit board (PCB) and the local CTE mismatch

between the solder and the adjacent materials have been a problem in the solder reliability [13-15]. In general, an increase of the solder joint height reduces the solder strains of surface mounting components. The maximum achievable solder height is proposed to maximize the effect. A thinner PCB can also reduce the solder strains. This is ascribed to the reduced bending stiffness of the assembly with a thinner card, which allows the assembly to bend more and thus reduce the shear strains of the solder joint. The thinner die allows more high-CTE-EMC material in the package and increases the effective CTE of the package accordingly. A copper lead frame is proposed whose higher CTE and compliance should significantly reduce the solder strains of the packages

A parametric study has been done to investigate the reliability of solder joints using leaded and leadless packages. An underfill encapsulant (refer to Fig 2.6) was used to fill the gap between the chip and substrate around the solder joints to improve the reliability of the flip chip interconnects system. The filled materials relax the mismatch of the coefficient of thermal expansion of the chip and substrate, and thus reduce the thermal stresses imposed on the solder joint giving an increase in solder fatigue resistance [16-18].

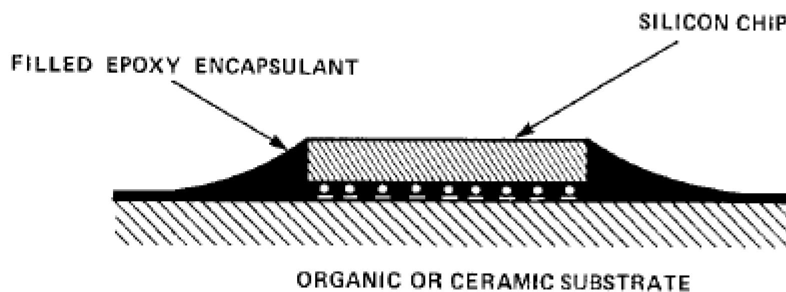
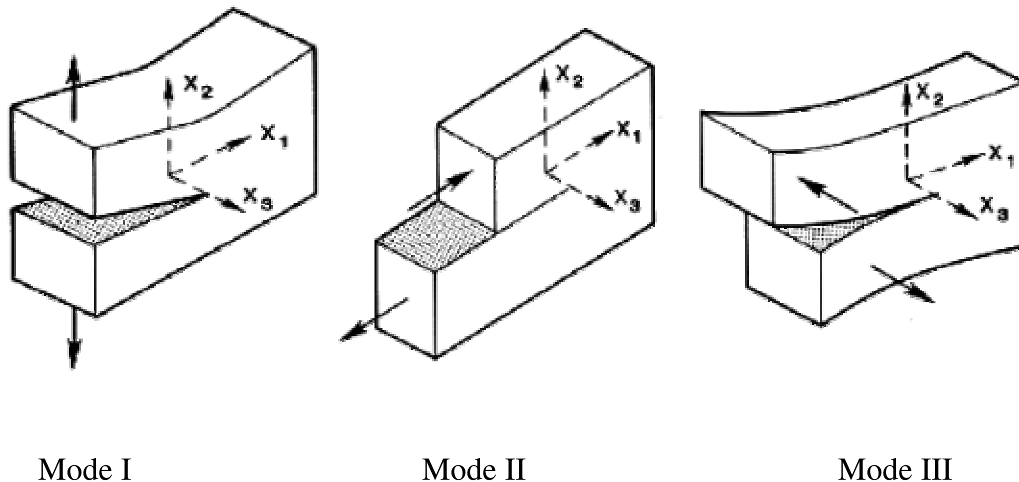


Fig. 2.6 Schematic representation of the encapsulated C4 joints

Some authors have investigated interface delamination and cracking of the underfill in flip chip packages under temperature cyclic loading using finite element analysis [19-22]. In order to investigate the delamination behaviors of underfill at the edge of chip in a flip-chip assembly under thermal loading, it is necessary to perform a fmite element analysis to extract the fracture or delamination parameter. The most important region in a fracture (delamination) model in a finite element analysis is the region with stress singularity (refer to Fig. 2.7). For a crack in homogeneous material, the well-known mode I, 11 and III stress intensity factors (KI, KII, and KIII) were found to be the only parameters that characterize the magnitude of the singular stress field at the crack tip for each basic failure mode, respectively (refer to Fig 2.7)



Mode I Mode II Mode III

Fig. 2.7 Mode I, Mode II and Mode III of Fracture.

The total energy release rate or J integral can he used as fracture parameter to describe the energy flow into the crack tip per unit fractured area. It is given by:

$$J = \int_{\Gamma} (wdy - T_i \frac{\partial u_i}{\partial x}) dS \tag{2.1}$$

where $w = \int_0^{\varepsilon_{ij}} \sigma_{ij} d\varepsilon_{ij}$ is the strain energy density, $T_i = \sigma_{ij} n_j$ is the traction vector on an arbitrary contour Γ (Fig. 2.8) and u_i are the displacement vector components. The path Γ can be any shape and size around the crack tip and the J-Integral is path-independent. Rice [23] further showed that it was equal to the energy release rate G in a linear as well as a nonlinear elastic body that contains a crack, i.e. $G = J$.

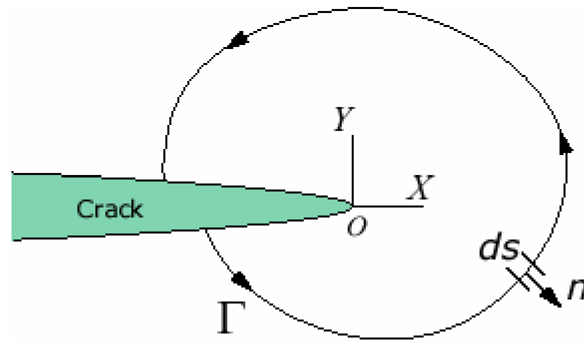


Fig. 2.8 J-integral.

Finite element analyses have also been performed on the solder joints [24-27]. They refer to two high stress concentration areas in the solder joint. Fig. 2.9 shows the schematic view of a SLICC package, the primary region is the top right and the secondary region is the bottom left of the solder joint. The first area has the largest work energy density induced in the solder joint and is typically closer to the package side creating a crack from the inside periphery of the joint from the corner of the joint propagating along the joint-package interface. The second area has the highest stress concentration and is typically closer to the board side of the solder joint creating a crack

from the inside periphery of the joint outwards propagating along the joint-board interface.

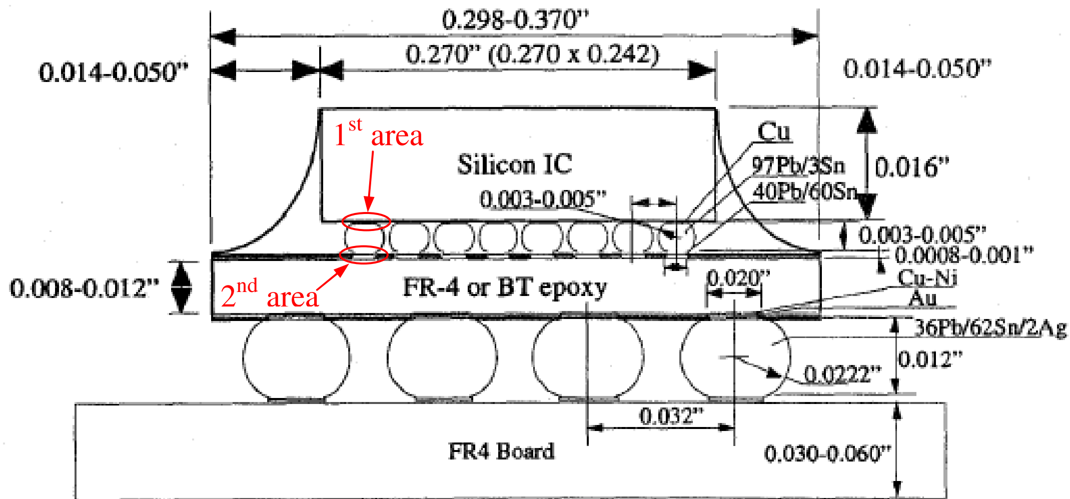


Fig. 2.9 Schematic of a SLICC package.

Even with the addition of an underfill material, it has been supposed that there are limits on the chip size used in flip chip applications. The effects of CTE mismatch are assumed to become more severe with increasing chip size [28]. Such CTE mismatch-induced stresses, manifested by the increasing die size and temperature excursions, have posted a great challenge to the thermomechanical reliability of flip-chip DCA packages. To prevent premature thermomechanical failure and ensure the reliability of a DCA package, the thermomechanical stresses caused by the CTE mismatch, which is the driving force to failure, must be understood.

The FE analyses have also shown that the fundamental limits on chip size for an underfilled flip chip with a clamped board are not crucially influenced by the distance to

the neutral point (DNP) of the outermost solder joint. The strain fields are relatively independent of chip size and DNP (refer to Fig. 2.10). These facts also suggest that larger die samples will have increased propensities for fracture, not due to increased internal strains and stresses, but due to the fact that they are statistically more likely to contain the critical size flaws under stress conditions for catastrophic crack propagation [29].

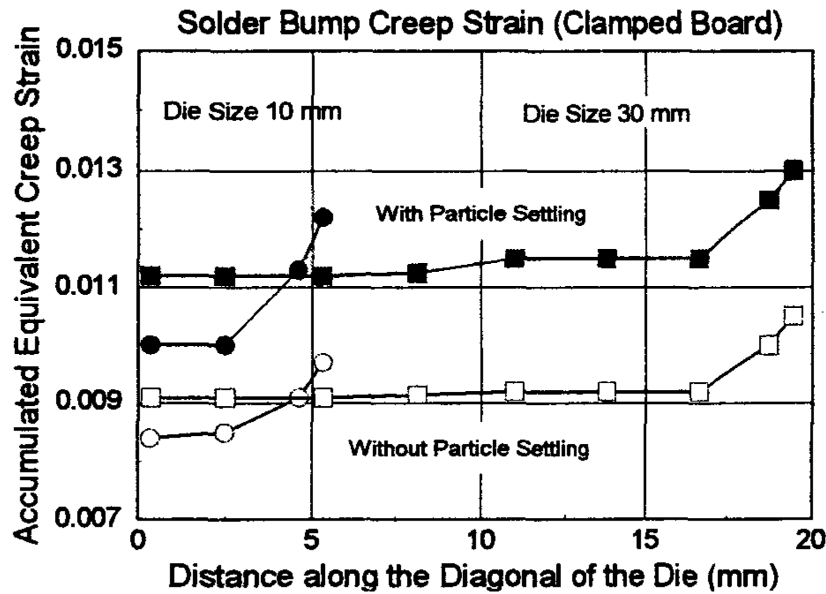


Fig. 2.10 Creep strains in the solder bumps in dependence of bump position

For future devices with very fine pitch and large chip size, solder joint reliability might be a serious obstacle to package design engineers, since the joints become much smaller and yet are expected to accommodate much higher strain due to thermal mismatch between chip and substrate. Copper or gold solder columns has been a solution to replace solder joints at wafer level packaging in order to decrease the stresses at

specific stress concentrations locations and enhance thermomechanical reliability [30]. Fig. 2.11 shows a schematic view on a package using solder joint columns.

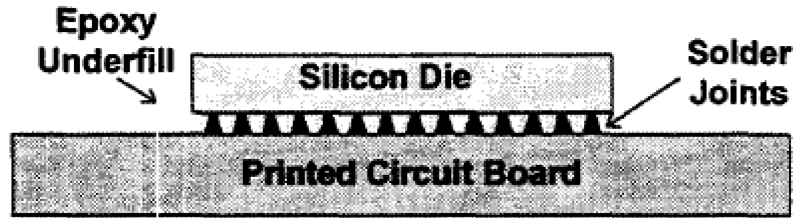


Fig. 2.11 Schematic of FCOB Assembly using solder joint columns

Higher deformation of the molten solder during reflow also leads to more acute angles at the corners of the barrel shaped joints. In typical barrel-shaped flip chip solder joints, failure due to mismatch stresses and electromigration usually initiate at the joint corners on the die side that act as stress raisers. As the joint diameter is reduced the effect of these corners in initiating fatigue cracks is aggravated. Modeling shows that for a 100 um diameter barrel-shaped solder joint fatigue life reduction due to corner stress effects is about 25% whereas that for a joint 60 um in diameter it is as much as 50% [31].

Three basic interconnection technologies for WLPs [32] at 100um pitch have been pursued, each extending the state of the art (Fig. 2.12):

1) Lead-free solder ball (SB) with underfill, a rigid interconnection;

2) Bed of nails (BON), a compliant interconnection;

3) Stretched solder column (SSC), a semi-compliant interconnection.

Of the three interconnection schemes proposed, the scheme which best meets the electrical requirements is the SB interconnection while the scheme which best meets the mechanical requirements is the SSC.

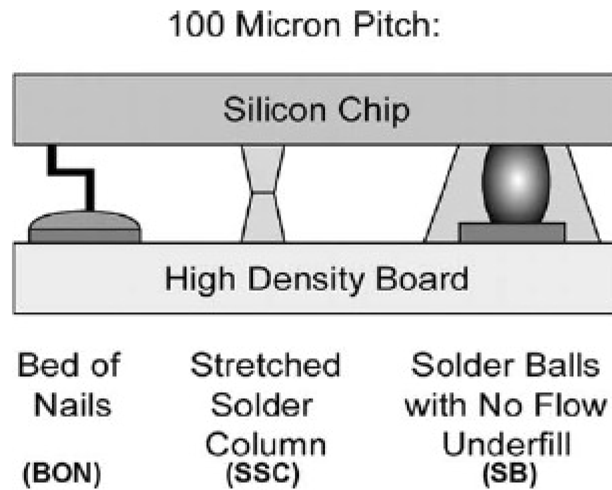


Fig. 2.12 Proposed 100-um-pitch interconnections.

CHAPTER 3

Verification of 2D and 3D model using modified Suhir's solution

3.1 Verification of 2D and 3D model using modified Suhir's solution

A fundamental solution to thermal stresses of a die-substrate assembly was initially proposed by Suhir [38–40] in the mid-1980's after Timoshenko [33] and Chen and Nelson [34]. It has been revised in its die attach (adhesive) peel solution by Suhir himself [35, 36], and with his co-author Mishkevich [37]. The solution is relatively simple and easy-to-use, compared to Chen and Nelson [34] and Mirman [41], and can be allowed to explicitly and instantly indicate important parameters affecting the stresses and deformations of the assembly. However, there are still some existing controversies and inconsistencies regarding die stresses, die attach shear and peel stresses and warpage deformation of the assembly. For example, the Suhir solution is inconsistent with the finite element solutions in certain sections [42]. The original solution, despite the controversies and inconsistencies, is still good enough for parametric identification and trend prediction as seen in the literature. Recently Tsai [43] modified Suhir's theory to get a more accurate numerical solution to measure die stresses, die attach shear and peel stresses and warpage.

Tsai [43] has performed some finite element simulations to correlate correctly with the modified Suhir's theory. To keep it concise, the objective of this chapter is to verify that our 2D and 3D modeling techniques are following the same trend as Tsai's [43] simulation results before we proceed into the subsequent chapters on the modeling

of flip chip packaging. Tsai has used a linear 2D axis-symmetry and 3D solid element models to predict the warpage of the package from a thermal loading of 116°C to 25°C. The geometry of the model is shown in Fig. 3.1. A die flip chip package with 15mm x 15mm die size and 40mm x 40mm substrate size has been undertaken for analysis. Table 3.1 show the material properties used in the modeling by Tsai. Tsai assumed the following conditions

- Isothermal loads are assumed (stress free at 116^{0}C)
- Each layer in the assembly acts as a spherically bending thin plate for linear 2D axis-symmetry with perfectly bonded interfaces existing between the layers in the assembly for linear 2D axis-symmetry and 3D model

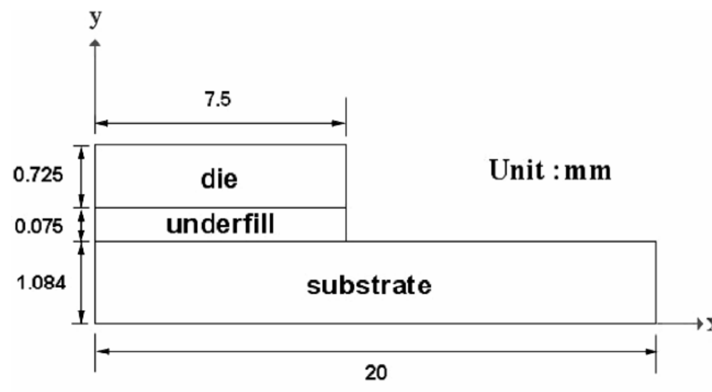


Fig. 3.1 Schematic diagram of the diagonal cross-section of the package

Table 3.1 Material properties used

Materials	Young Modulus (GPa)	CTE (ppm/°C)	Poisson ratio
Die	163	2.5	0.28
Underfill B	E_1=6.3 E_2=0.0276	α_1=33 α_2=133	0.35
Substrate	Ex=Ez=11 Ey=5.5	αx=αz=15.7 αy=58	Vxy=Vyz=0.42 Vxz=0.11

Note: Subscript 1 and 2 represent the properties under and above Tg=84°C for Underfill B

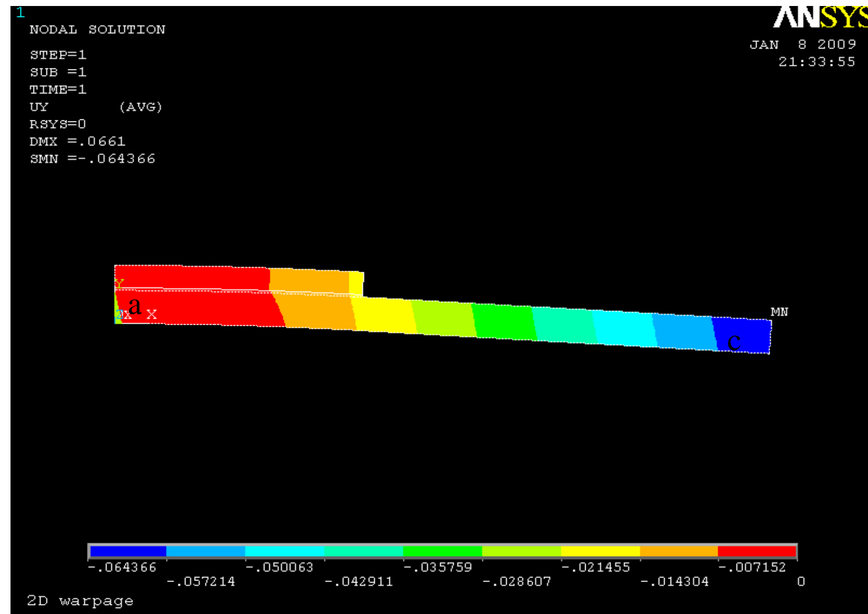


Fig 3.2 Current 2D model after thermal loading

Fig 3.2 and 3.3 show the 2D axis-symmetry model and the 3D model, respectively, built to verify Tsai's [43] simulation results. The 2D model uses 2751 linear quadrilateral elements and 2972 nodes. The 3D model uses 3794 8-node hexahedron elements and 5122 nodes.

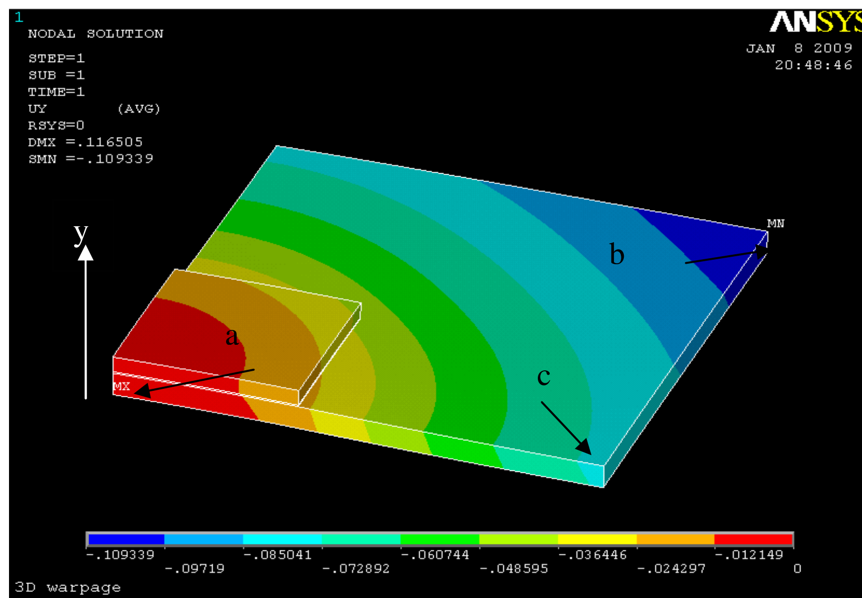


Fig 3.3 Current 3D model (without fillet)

For Tsai, the warpage distributions along the center line (ac) and diagonal line (ab) are shown in Fig. 3.4 for the packages with full fillet and without fillet after thermal loading. It is clear that the warpages at die/substrate assembly from 2D and 3D simulation analyses are almost identical for packages with and without fillets. The maximum warpage occurs at the end of the diagonal line, rather than the center line. The fillet effect on the warpage is negligible for this flip-chip BGA. And the 2-D axis-symmetrical model can be approximately used for addressing the global warparge.

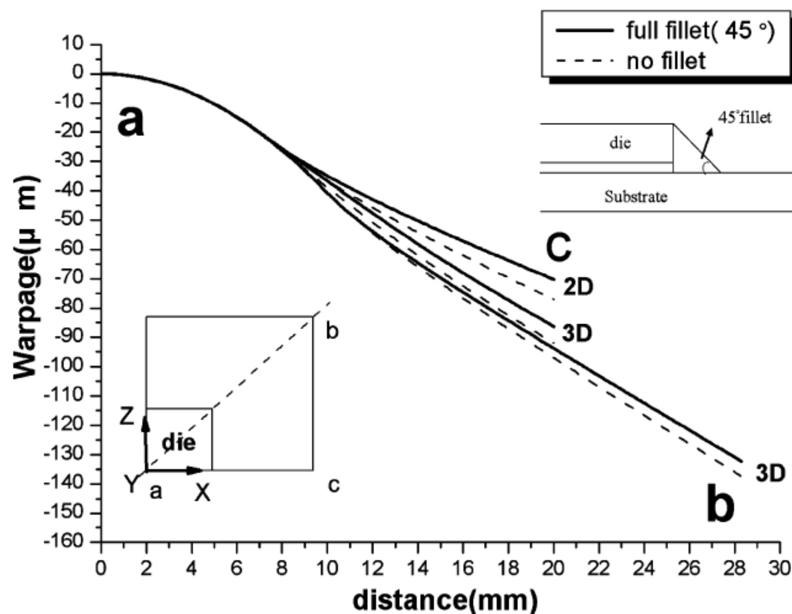


Fig. 3.4 Fillet effect on warpages of flip-chip BGA with underfill B (Tg = 84^0C) along the central line (*ac*) and diagonal line (*ab*), obtained from 2-D and 3-D FEM, under temperature loading from 116^0C to 25^0C.

For our interest we will focus on one case (without fillet) to verify the accuracy for our 2D and 3D models along the center line (ac). Displacements in the y direction (refer to Table 3.3) are obtained along the center line (ac) across the substrate after thermal loading and plotted in Fig. 3.5 to compare with Tsai's results.

Table 3.3 Warpage (deflection along y-axis) values obtained along the center line (ac)

Distance from centre *a*/mm	0	3	7	10	13	16	20
Warpage/um For 2D	0	-7.59	-18.34	-28.51	-39.33	-50.74	-64.44
Warpage/um For 3D	0	-8.71	-20.14	-34.25	-49.60	-63.55	-79.89

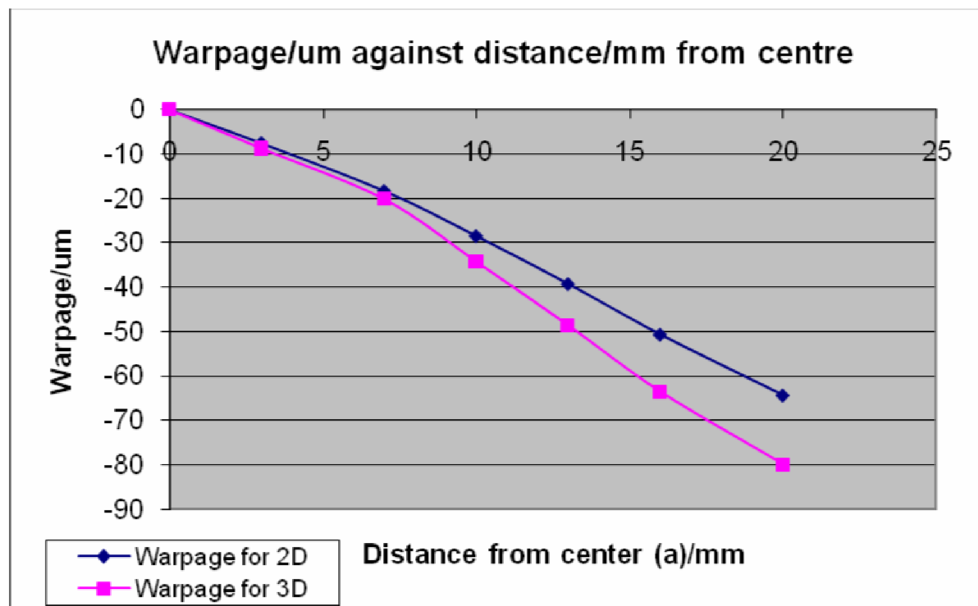


Fig 3.5 Warpage values for 2D and 3D model after thermal loading

Results show that our current 2D and 3D model are following the same trend with Tsai's results (Fig 3.4). There is some slight deviation, which could be due to the fact that both of us are using different mesh sizes but it is a pity Tsai [43] did not mention the mesh sizes used in his simulation.

Since Tsai's simulation results [43] are based on the modified Suhir's solution and the results from our current 2D and 3D models are also following the same trend with

Tsai's [43], we are confident that our models are accurate for parametric studies and can be further used in the subsequent chapters for applications in 2D and 3D parametric studies.

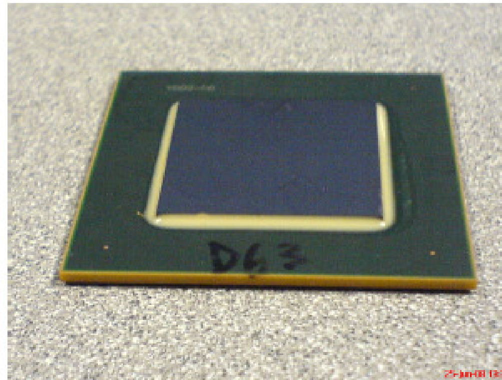
CHAPTER 4

Structural design and optimization of 65nm Cu/low-k flipchip package

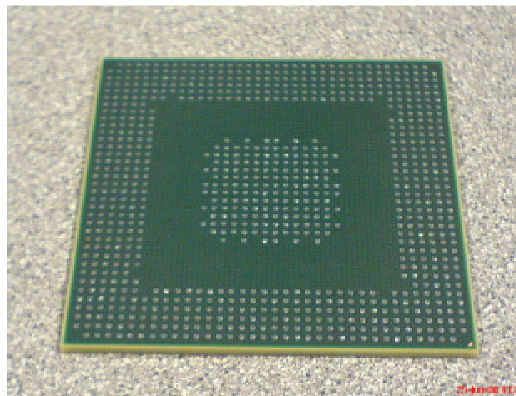
4.1 Finite Element modeling

A large die flip chip package with 21 mm x 21 mm die size, 150 um bump pitch, 60 um bump height on a 37.5 mm x 37.5 mm build-up organic substrate with lead free solder is to be optimized for thermo-mechanical reliability when temperature-cycled between -40 °C to 125 °C. Each cycle was 1 hour long with 2 rampings of 15 minutes and 2 constant temperature dwells at -40°C and 125 °C of 15 minutes each.. This package, shown in Fig. 4.1, consists of a 9-metal Cu/low-k layer with ~11000 bumps as on-chip level interconnects. Fig. 4.2 gives the details of the various layers of material in the package and geometry of the solder bump. Two-dimensional plane-strain finite element analyses (FEA) were performed on the diagonal cross-section of the package (Fig. 4.3) to obtain the thermally-induced stresses in the low-k layer and inelastic strain energy density dissipation per cycle (ΔW) in the solder bumps. The 2D model uses 2990 linear quadrilateral elements and 5989 nodes. The following assumptions were made in the modeling:

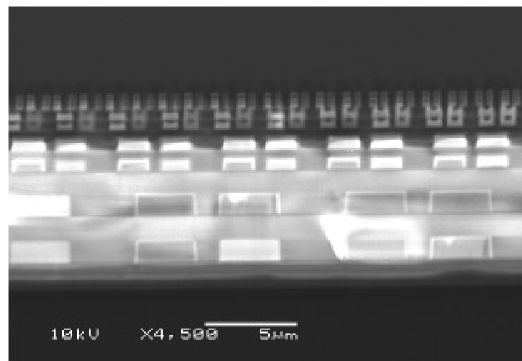
- The temperature change was assumed to be the same throughout the package.
- Perfect adhesion was assumed at all material interfaces.
- All materials were modeled as elastic materials except the solder material.
- Underfill was modeled as a temperature-dependent material.
- A viscoplastic constitutive relation was adopted for the lead-free solder.



(a)



(b)



(c)

Fig. 4.1. (a) Top view of package, (b) Bottom view of package, (c) SEM images of the 9 metal Cu/low-k layer

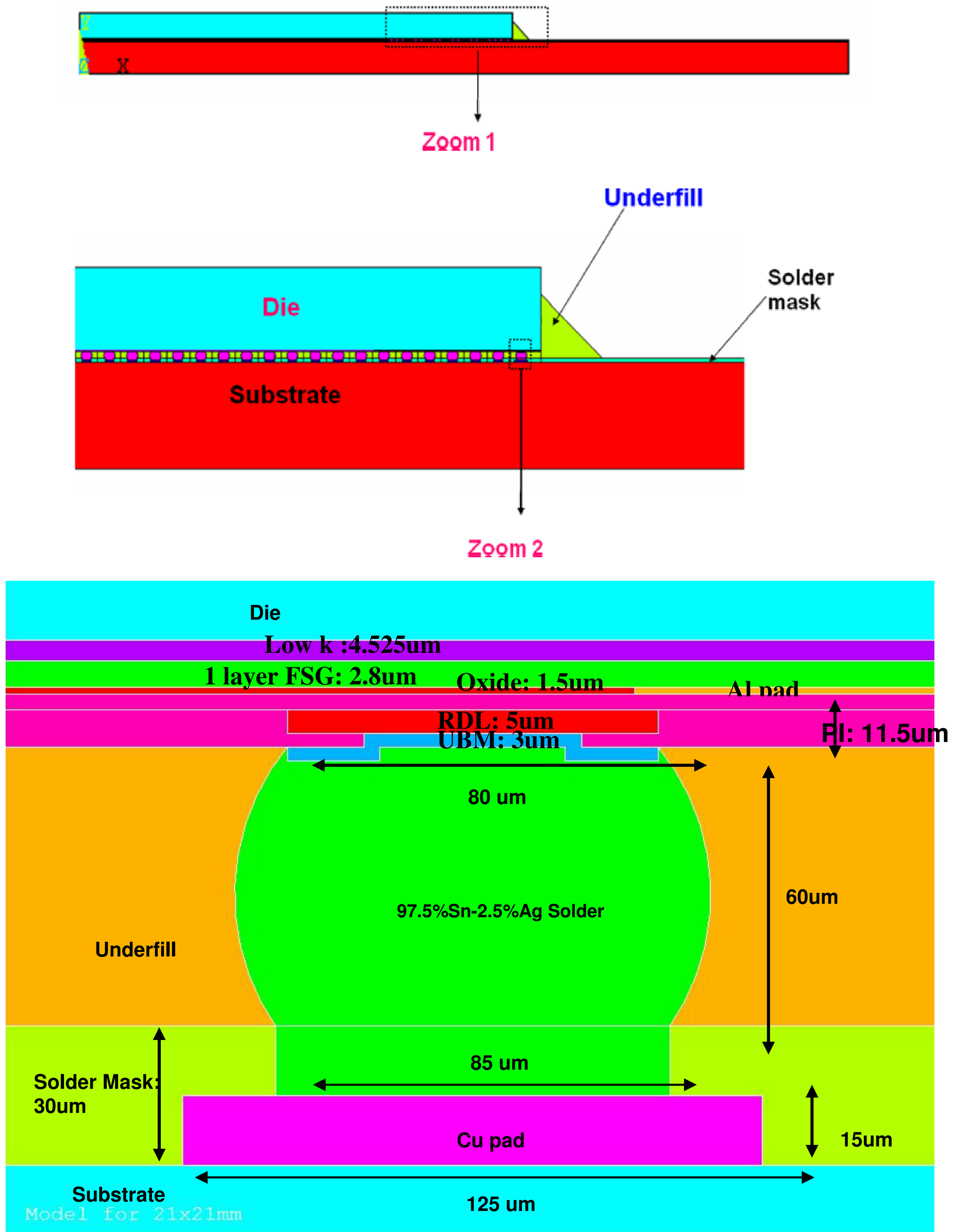


Fig. 4.2. Cross-section of the 21 mm x 21 mm test vehicle with FSG layer.

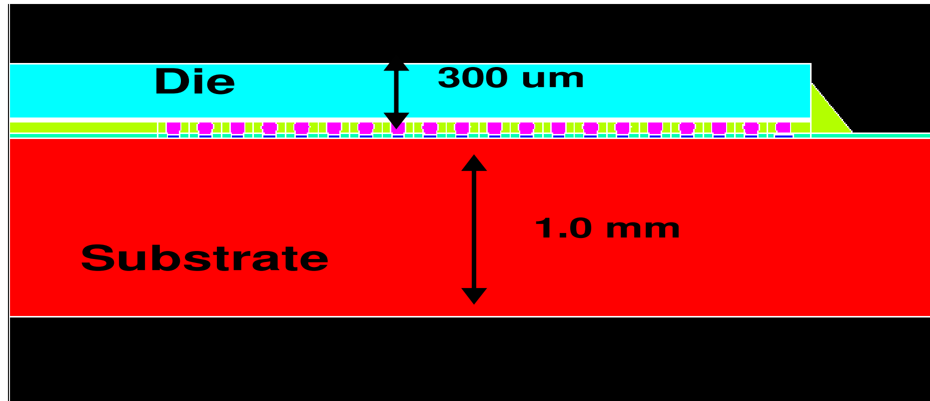


Fig. 4.3. Schematic view of solder bumps at the right side of the die with 0.3 mm die thickness and 1.0 mm substrate thickness.

Table 4.1 shows the material properties used in the modeling. Please refer to Appendix A details of the underfills' properties. The creep properties of the lead free solder are given in [46]. A typical stress distribution obtained is shown in Fig. 4.4.

Table 1: Material properties used in the study

Materials	CTE (ppm/C)	Young's Modulus (GPa)	Poissons Ratio
Silicon	2.7	131	0.28
Low-k	23	7.7	0.3
USG (undoped silicate glass)	0.57	66	0.18
FSG (fluorinated silicate glass)	0.25	70	0.16
PI (polyimide)	57	4	0.35
RDL (redistribution layer)	17	110	0.34
Underfill E	40.75	9.07	0.3
Cu	17	110	0.34
Solder bump	22	44.4 (25°C), 18.8 (125°C)	0.4
Core in Substrate	16	24.5	0.22
Build Up material	95	3	0.41
Solder mask	52	4	0.4

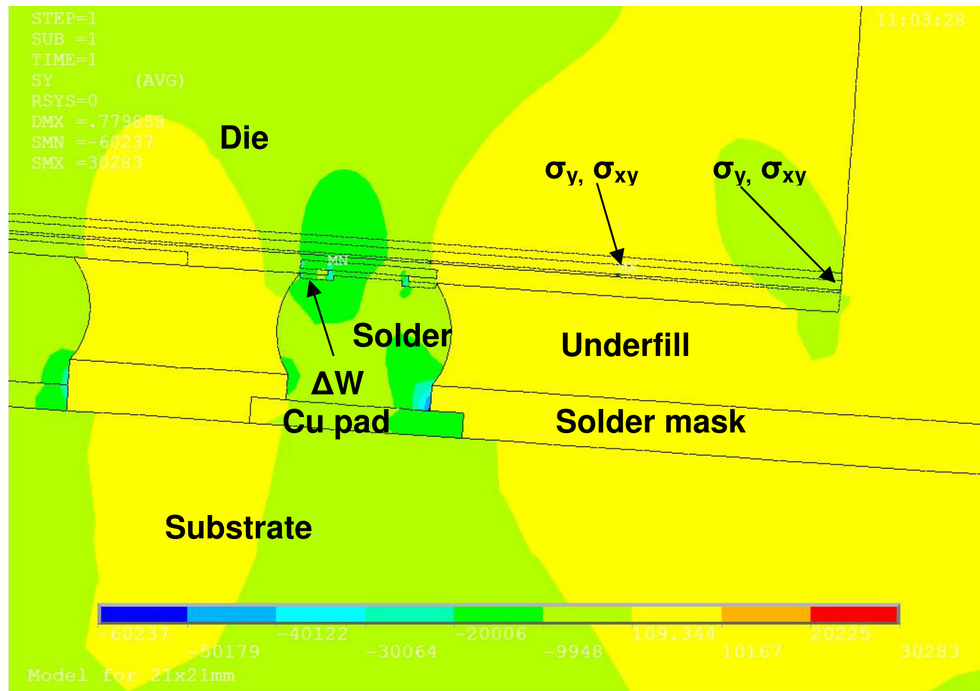


Fig. 4.4. Potential failure sites in the solder bump and low-k layer

While 2D finite element analysis is not as accurate as 3D finite element analysis, it is much easier to perform and hence more practical for engineers to use. It can definitely be used for predicting trends in a parametric analysis. In this study, we will further explore the use of experimental data to predict the thermo-mechanical reliability of the package.

Failure Criteria

Two failure criteria will be considered – one for the delamination at the low-k layer and the other for the fatigue failure of the solder bumps. It has been found [44, 45] that delamination, if it occurs, usually occurs at the interface between the low-k layer and the FSG layer directly under the outer edge of the aluminum die pad associated with the last bump or at the die edge, as shown in Fig. 4.4. Hence, the parameters used for

predicting the delamination at the low-k layer is the shear stress (σ_{xy}) and the normal stress (σ_y) at the interface between the low-k layer and the FSG layer, directly under the outer edge of the aluminum die pad associated with the outermost solder bump, denoted by $\sigma_{xy,dp}$ and $\sigma_{y,\ dp}$, respectively, as well as at the outermost edge of the die, denoted by $\sigma_{xy,de}$.and $\sigma_{y,\ de}$, respectively These 2 areas are critical for package reliability because peeling and shearing of the low-k material is often dominant at these locations during thermal cycling. It should be noted that a tensile σ_y at the interface will promote delamination but a compressive σ_y will not. Hence only tensile values of σ_y will be considered in evaluating the reliability of the low-k layer.

The parameter used for fatigue failure of the solder joints is the inelastic strain energy density dissipation per cycle, ΔW, in the critical element of the outermost solder bump. From the finite element simulations carried out in this study, the maximum ΔW always occurred at the outermost element of the outermost solder bump. The lower the ΔW, the longer the thermal fatigue life of the solder joint [46].

In order to obtain some failure criteria for the reliability analysis of the yet-to-be-built 21 mm x 21 mm die, Cu-low k flip chip package which was being designed, some reliability tests were carried out on an existing Cu/low-k flip chip package with a 15 mm x 15 mm x 750 um die, 150 um bump pitch, 60 um bump height, on a 30 mm x 30 mm build-up organic substrate with lead free solder and underfill E. This package was identical to the yet-to-be-built larger package in all aspects except for the smaller die size, a 6-metal Cu/low-k layer and ~8000 solder bumps. 25 specimens of this package were

subjected to JEDEC-MSL3 preconditioning followed by TC 1000 between -40 °C to 125 °C. Each cycle was 1 hour long with 2 rampings of 15 minutes and 2 constant temperature dwells of 15 minutes each at -40°C and 125 °C. After 1000 temperature cycles, random samples were picked from the lot for CSAM and cross-section inspection. It was found that all the specimens passed the 1000 TC test. Photographs of the cross-sections of the left and right solder bumps after 1000 temperature cycles are shown in Fig. 4.5, which shows intact solder bumps and no delamination in the low-k material.

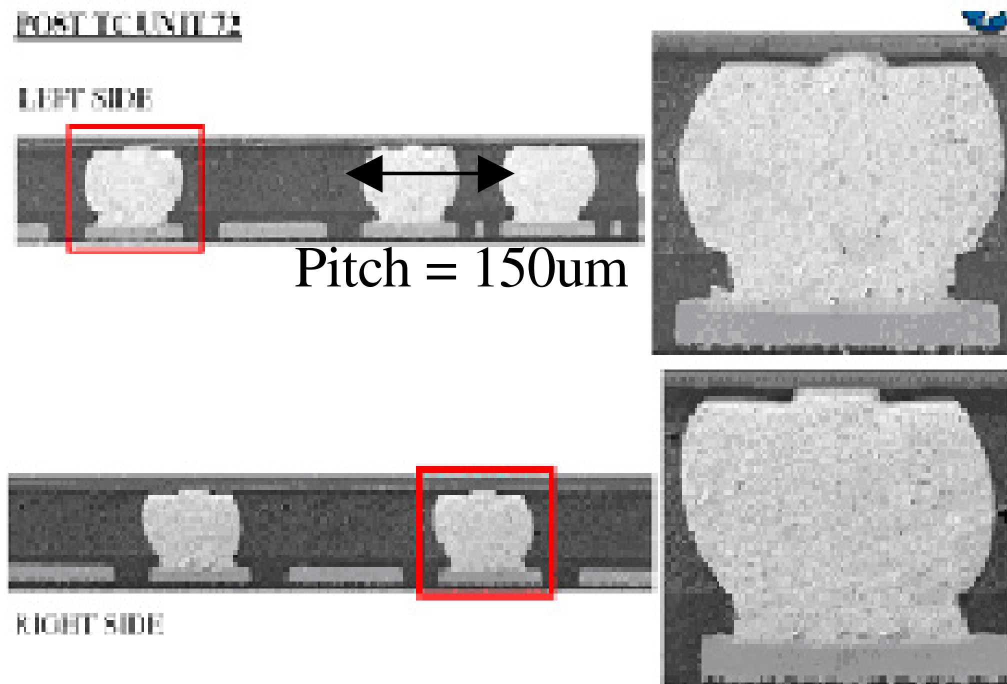


Fig. 4.5. Photographs of solder bumps at the left and right sides of the 15 mm x 15 mm die after 1000 TC testing.

Since the experimental studies described in the previous section have shown that the 15 mm x 15 mm die packages all passed the TC1000 test, we may use the stresses and ΔW computed for those packages as benchmark values for determining the reliability of

the yet-to-be-built large die package. The stresses and ΔW at the potential failure sites (Fig. 4.4) were hence obtained from the finite element analysis of the 15 mm x 15 mm die test vehicle. The results are shown in Table 4.2. These values can be regarded as the reliability benchmark values for the type of Cu/low-k chip packages studied, i.e. if the stress and ΔW parameters computed for any low-k flip chip packages using 2D FEA are lower than the corresponding benchmark values, then we can be confident that the package will pass the TC1000 test. But if the stress and ΔW parameters computed using 2D FEA are higher than the benchmark values, we cannot be confident that the package will pass the TC1000 test, although we also cannot conclude that it will fail the TC1000 test either. However, it may be reasonable to conclude that the higher the values of the parameters are above the benchmark values, the greater will be the probability that failure will occur.

Table 4.2: Stresses at potential failure sites and ΔW for the 15 mm x 15 mm x 750 um die package

$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
107.95	61.20	1.790	-293.30	5.98

4.2 Parametric Study

In order to optimize the design of the 21 mm x 21 mm die low-k flip chip package, a parametric numerical study of the effect of various parameters such as number of layers of FSG, the thickness of the die and the thickness of the substrate on the reliability of the package was carried out. The reliability performance of lead free solder bump versus Cu post interconnect was also compared. The Polymer Encapsulated Dicing Lane Technology (PEDL) concept is used to address the dicing challenges of Cu/low-k and simultaneously improve the reliability performance by reducing the corner stress in

the Cu/low-k layer. The feasibility of reducing one layer of fluorosilicate glass (FSG) using PEDL technology and other means was also investigated.

4.3 Results and Discussion

4.3.1 Effect of PEDL

FEA was performed for the package with a die thickness of 750um and a substrate thickness of 1mm, using underfill E and various PEDL (bevel cut) technology. From Table 4.3 results show that stresses in the low-k layer are reduced when PEDL technology is used. It can be seen that the shear stress (σ_{xy}) using the 35um by 35um bevel cut (refer to Fig. 4.6) decreases by 33.9% at the die edge and 42.6% under the die pad, while σ_y decreases by 70.1% at the die edge and 66.7% under the die pad. Also ΔW using bevel cut decreases by 20.7% as compared to the package without bevel cut. This shows that PEDL is very effective in lowering the stresses likely to cause delamination.

Table 4.3: Effect of bevel cut (PEDL)

Bevel cut	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
no bevel cut	81.16	67.70	1.961	-96.50	34.83
bevel cut using BCB	50.45	38.68	1.556	-118.69	11.52
bevel cut using underfill	53.65	38.87	1.554	-118.55	11.60
Bench mark	107.95	61.20	1.790	-293.30	5.98

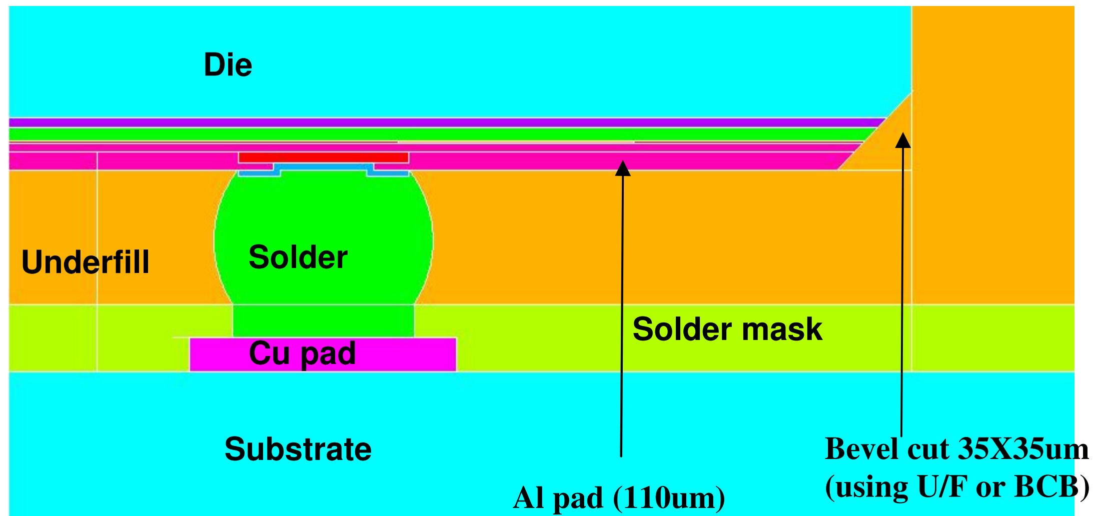


Fig. 4.6. Cross-section of package showing bevel cut (PEDL)

The material for the triangle bevel cut (35 x 35um) can either be BCB or underfill itself (Fig. 4.6). From Table 4.3, it can be seen that using BCB for the bevel cut is a better choice than using underfill as the delamination stress values are slightly lower. However the impact of using the different bevel cut materials is not significant as the stress values do not differ much.

As can be seen in Table 4.3, if PEDL technology is not used (i.e. no bevel cut), all the computed delamination stresses and ΔW values except $\sigma_{xy,de}$, exceed the reliability benchmark. This suggests that if PEDL technology were not used in the new die, there is a high probability that delamination of the low-k layer and fatigue failure of the solder bumps will occur. However, when PEDL technology is employed, all the computed delamination stresses and ΔW are all within the benchmark values, except for $\sigma_{y,dp}$ which is almost doubled. As elaborated earlier, even though a benchmark value has been exceeded, the probability of failure may be increased but it is not a certainty.

The PEDL (bevel cut) technology is very efficient but it has a drawback in that extra steps have to be added in order to fabricate the bevel cut, leading to increased

manufacturing cost. However, it is a good solution to reduce delamination at the low-k layers for large die applications.

4.3.2 Effect of the number of layers of FSG used

The effect of using 1 layer of FSG versus 2 layers of FSG will now be studied. Each layer of FSG is 2.8 um thick. Underfill E and PEDL technology will be used in both the packages analyzed using FEA. As can be seen from Table 4.4, shear stress (σ_{xy}) in the low k layer decreases slightly by 6.2% at the die edge and 7.7% under the die pad with the use of 2 layers FSG while σ_y decreases by 12.6% at the die edge and 9.4% under the die pad. It appears that two layers of FSG act as a better cushion to reduce the stresses in the low-k layer during thermal cycling as compared to one layer of FSG. However, since the differences in the delamination stresses and ΔW are small, one layer of of FSG will be used in the new design since the manufacturing costs will be lower.

Table 4.4: Effect of number of layers of FSG

Number of FSG layers	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
1	50.45	38.68	1.556	-118.69	11.52
2	47.33	35.69	1.541	-103.74	10.44
Bench mark	107.95	61.20	1.790	-293.30	5.98

As can be seen in Table 4.4, all computed stresses and ΔW values were lower than the benchmark, except for $\sigma_{y,dp}$, which, at 11.52 MPa for one layer of FSG, is slightly more than double the benchmark value of 5.98 MPa. While this may not mean that the new package will fail TC1000, there is some probability that it would fail

TC1000. Hence, additional ways of reducing $\sigma_{y,dp}$ will be explored in the following sections where only one layer of FSG layer will used.

4.3.3 Effect of die thickness

A parametric study was done to investigate the influence of the die thickness on the delamination stresses and ΔW induced in the package. Finite element analyses were performed with 4 values of die thickness (750, 500, 300, 100um) for the 21 mm x 21 mm die package with bevel cut using underfill E. The results are tabulated in Table 4.5. They show that the stresses in the low-k material and ΔW in the critical solder bump decrease as the die gets thinner. This can be explained by the fact that a thinner die is more compliant, thus the delamination stresses and ΔW induced in the solder bumps are reduced. All computed delamination stress and ΔW values passed the reliability benchmark except for $\sigma_{y,dp}$.

Table 4.5: Effect of die thickness

Die thickness (um)	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
750	50.45	38.68	1.556	-118.69	11.52
500	45.26	33.21	1.330	-101.72	9.36
300	43.50	28.89	1.176	-96.28	8.25
100	41.43	25.69	1.036	-67.34	6.31
Bench mark	107.95	61.20	1.790	-293.30	5.98

4.3.4 Effect of substrate thickness

Next, 2 cases were analysed where the substrate thickness was varied (1.0, 0.6mm) on the 21 mm x 21 mm die package with a die thickness of 300 um, with bevel cut and using underfill E. From Table 4.6, it can be seen that all the computed delamination stresses and ΔW values decrease as the substrate thickness gets smaller,

since a thinner substrate is more compliant. All the computed delamination stress and ΔW values for the 0.6 mm thick substrate passed the reliability benchmark. Thus, with a thinner die (300 um) and a thinner substrate (0.6 mm), based on the comparison with the benchmark stress and ΔW values, we have achieved the optimum design for the large 21 mm x 21 mm die package with solder bump interconnects.

Table 4.6: Effect of substrate thickness

Substrate thickness(mm)	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW (J.m^{-3})	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
1.0	50.45	38.68	1.556	-118.69	11.52
0.6	40.95	26.27	1.006	-88.73	5.21
Bench mark	107.95	61.20	1.790	-293.30	5.98

4.3.5 Effect of Cu-post

The use of Cu-post interconnects is becoming more prevalent due to its greater resistance to electromigration. Additionally, Cu-post interconnects can be used to increase the standoff height to increase the compliance of the interconnects, so that the shear stress in the low-k material and ΔW in the solder joints may be reduced. Thus, the use of Cu-post interconnects instead of solder bumps will be explored in this section. FEA was performed for the package with a die thickness of 300um and a substrate thickness of 0.6 mm, using underfill E and 80 um high Cu-post interconnects instead of solder bumps (refer to Fig. 4.7). From Table 4.7, it can be seen that with the 80 um high Cu-post interconnects, $\sigma_{y,dp}$ is almost 50% higher than the package using solder bumps while the other reliability parameters are all only less than 10% lower. This could be due to the fact that the Young's modulus of Cu is much higher than that of the solder bumps so that even though the standoff height is greater with the Cu-post, the overall stiffness of the interconnect is higher. A parametric study was carried out on the effect of Cu-post

height (40um, 80um, 120um). From Table 4.7, all the stress values decrease when Cu-post height increases but $\sigma_{y,dp}$ is still significantly greater than the package with solder bumps as well as the reliability benchmark. This is likely due to the rigidity of the Cu material which causes the $\sigma_{y,dp}$ to be high. Although taller Cu-posts are preferred, a longer plating time and higher cost is associated with the taller Cu-post. Hence in this project an 80 um Cu-post height will used instead of 120 um. Moreover, from the results in Table 4.7, the differences in stress and ΔW for the two heights are small.

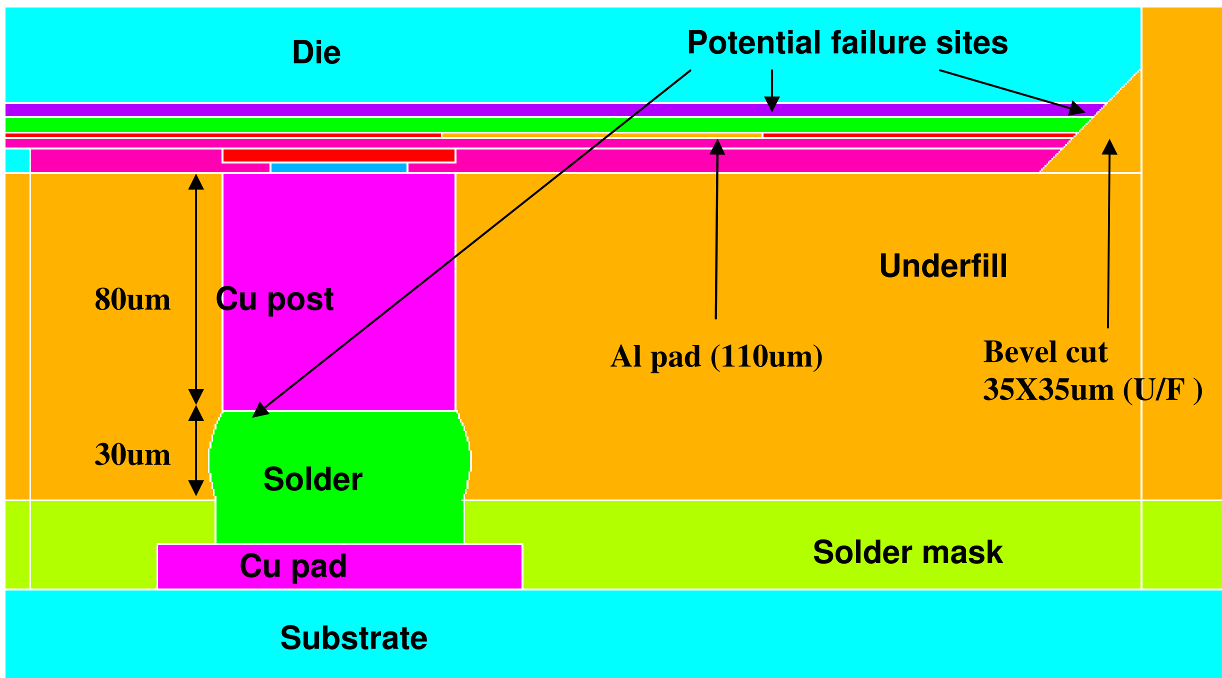


Fig. 4.7: Schematic view of Cu-post interconnects

Table 4.7: Effect of height of Cu-post interconnects

Height of Cu post (um)	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
0 (solder only)	50.45	38.68	1.556	-118.69	11.52
40	46.28	38.97	1.536	-145.4	18.40
80	45.99	38.48	1.430	-151.9	17.38
120	45.45	38.36	1.351	-168.9	16.61
Bench mark	107.95	61.20	1.790	-293.30	5.98

4.3.6 Effect of underfill

In attempting to lower $\sigma_{y,dp}$ for the package with Cu-post interconnects, the use of a better underfill will be explored in this section. An underfill which gives a lower CTE mismatch with the substrate and die should result in lower induced stresses induced and higher solder fatigue life. This can be achieved by increasing the filler loading in the underfill. However, an increase in filler loading will increase the E of the underfill, thereby increasing the stress in the low-k material. There is thus a tradeoff involved and achieving both low E and low CTE is still a challenging problem in the industry today.

Finite element analysis was carried out for the 21 mm x 21 mm x 300um die package with 80 um Cu-post height and 0.6 mm-thick substrate with 4 different underfills (refer to Table 4.8 for the underfill properties). The results of the analysis are given in Table 4.9, where it can be seen that all the computed delamination stresses and ΔW for all the underfills considered were within the benchmark values except for $\sigma_{y,dp}$. As it appears that it would be very difficult to reduce $\sigma_{y,dp}$ further, it was decided to go ahead with the package design using underfill I which gave the lowest value of for $\sigma_{y,dp}$. As mentioned earlier, if the computed delamination stresses and ΔW exceeded the benchmark values, it is not certain that the package will fail TC1000. Hence some test vehicles will be fabricated and tested to establish experimentally if the proposed design of the Cu-post interconnected large die flip chip package will be reliable.

Table 4.8: Material properties for different underfills studied

U/F	Young's Modulus [GPa] (25 ^{o}C)	CTE1/CTE2 [ppm]	Tg (deg ^{o}C)
E	6.16	32/ 95	100
I	4.38	40 /141	132
J	6.30	30/ 102	117
K	5.33	25/ 100	95

Table 4.9: Effect of underfill type

Underfill type	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW (J.m^{-3})	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
I	44.81	32.01	1.211	-116.63	10.27
J	48.42	36.51	1.462	-104.82	13.53
K	46.63	30.62	1.355	-122.51	12.02
E	50.45	38.68	1.556	-118.69	11.52
Bench mark	107.95	61.20	1.790	-293.30	5.98

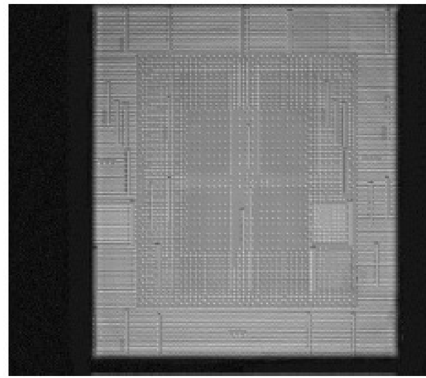
4.4 Experimental Verification

In order to establish the reliability of the large die packages analyzed in the previous sections, some test vehicles (TVs) were fabricated and tested in the same manner described earlier for the 15 mm x 15 mm die package. The test vehicles tested were all 21mm x 21mm die flip chip packages with 150 um bump pitch on a 37.5mm x 37.5mm build-up organic substrate with underfill I. Two versions of the test vehicles have lead free solder bump interconnects of height 60 um – one with a thick (750 um) die with PEDL (Test Vehicle A) and the other with a thin (300 um) die with PEDL (Test Vehicle B). The third version has a thick (750 um) die with Cu-post interconnects and *without* PEDL (Test Vehicle C). Although in the packages with Cu-post interconnects studied earlier had employed PEDL, it was decided to fabricate and test such packages without PEDL for reasons of cost. The sample sizes were 21, 22 and 27 for test vehicles A, B and C, respectively.

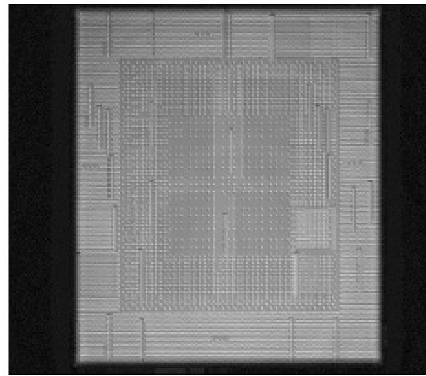
The experimental results are shown in Table 4.10. The CSAM inspections revealed no delamination problems (Fig. 4.8a, b, c) for all the specimens. Three important conditions were analyzed: (1) underfill adhesion to polyimide and soldermask, (2) low-k chip dielectric integrity, and (3) underfill fillet cracking. All specimens showed good adhesion at both underfill interfaces i.e. between underfill and BCB, and between underfill and soldermask. A very positive result is that no low-k dielectric cracking was found for all the 3 types of test vehicles after TC 1000. Fig. 4.9(a, b, c) shows the cross-section pictures of the left, centre and right solder bumps of test vehicle A after 1000 TC. Fig. 4.10(a, b, c) shows the respective cross-section pictures of the left, centre and right solder bumps of test vehicle C after 1000 TC. As can be seen, the solder bumps are slightly out of shape for the package with Cu-post interconnects. This is because the SEM pictures were taken after temperature cycling. As the solder bumps at the edge have the largest distance from neutral point (DNP), they experienced the greatest CTE mismatch and strain during temperature cycling, resulting in the deformed shape of the solder joints due to creep. However no leakage current and resistance failure was found during electrical testing.

Table 4.10: Reliability results for 3 test vehicles of 21 mm x 21 mm die package with 1 FSG layer

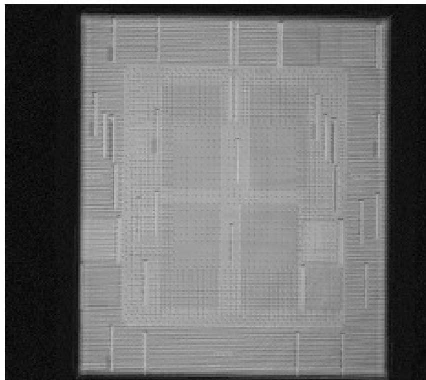
Test Vehicle	Manufacturing evaluation on 150 µm pitch TV (after TC 1000cycles)		Reliability of TVs (JEDEC-MSL3 followed by 1000 TC -40/125°C)
	Visual inspection	Void (CSAM)	Adhesion & low-k cracking (CSAM)
A: Thick die (750um) with PEDL	Pass	No	No delamination and no low-k cracking
B: Thin die (300um) with PEDL	Pass	No	No delamination and no low-k cracking
C: Cu-post with thick die (750um) without PEDL	Pass	No	No delamination and no low-k cracking



(a)

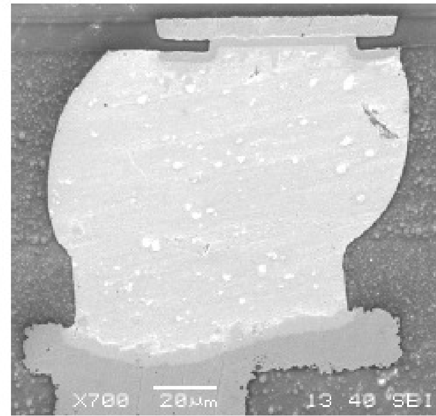


(b)

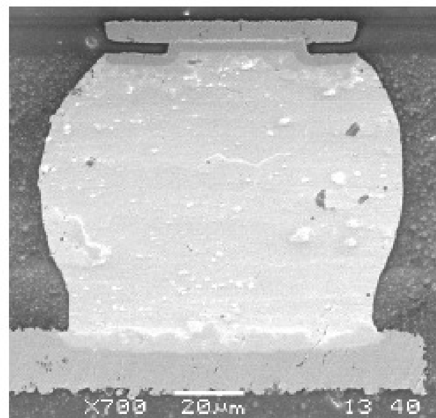


(c)

Fig. 4.8: (a) Typical CSAM result for TV A after 1000 TC, (b) Typical CSAM result for TV B after 1000 TC, (c) Typical CSAM result for TV C after 1000 TC.



(a)



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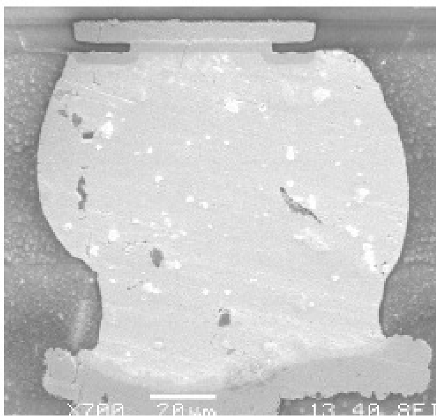
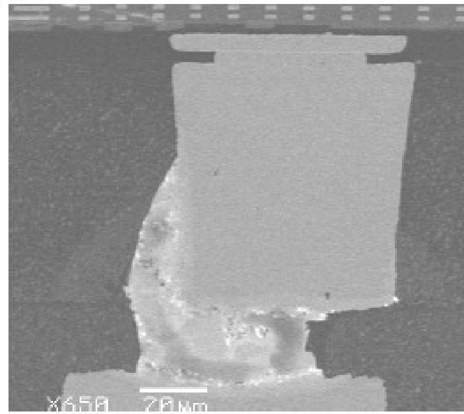
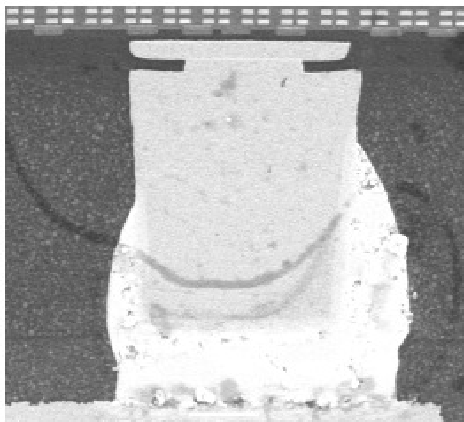


(c)

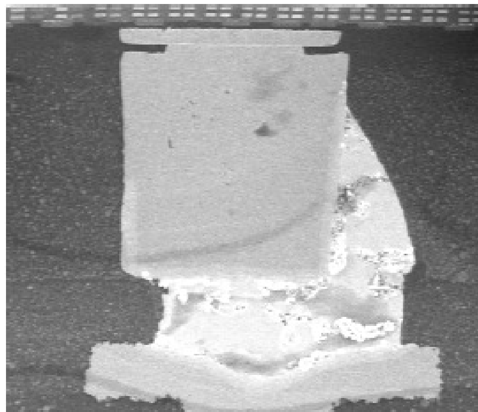
Fig. 4.9: Photographs of solder bumps at (a) right, (b) centre and (c) left of TV A after 1000 TC testing.



(a)



(b)



(c)

Fig. 4.10: Photographs of solder joints at (a) right, (b) centre and (c) left of TV C after 1000 TC testing.

Table 4.11 gives a summary of the results for all the samples that underwent electrical testing after subsequent TC. Electrical testing was carried out after 0, 500 and 1000 cycles using a 4-point probe. An increase of 20% in electrical resistance from the start of the TC or a value of 300Ω and above during electrical testing constituted a failure. As can be seen in Table 4.11, no failures were observed in all the samples. Furthermore, no underfill fillet cracking was observed after TC 1000. This demonstrates that for the 750um-thick die packages with 80um Cu-post interconnects and one layer of FSG, acceptable reliability can be achieved *without* PEDL if a good underfill were employed.

Table 4.11: Electrical testing results after subsequent TC for the 3 different types of test vehicles.

Test Vehicle	Electrical test (failures)					
	TC=0		TC=500		TC=1000	
	Resistance	Leakage	Resistance	Leakage	Resistance	Leakage
A: Thick die (750um) with PEDL	0/21	0/21	0/21	0/21	0/21	0/21
B: Thin die (300um) with PEDL	0/22	0/22	0/22	0/22	0/22	0/22
C: Cu-post with thick die (750um) without PEDL	0/27	0/27	0/27	0/27	0/27	0/27

To experimentally establish the efficacy of PEDL technology, 21 specimens of the 21 mm x 21 mm x 750um die solder bump package *with* PEDL and 21 specimens of the package *without* PEDL were fabricated, temperature cycled and electrically tested. Table 4.12 shows a summary of the results for both types of specimens that underwent electrical testing after 0, 500, 1000, 2000, 3000, and 3500 temperature cycles. As can be seen, with PEDL, the package passed TC 3000 but without PEDL the package can only

pass TC 2000. This demonstrates that PEDL technology can help to increase the reliability of a package by approximately 50%.

Table 4.12: Electrical testing results after subsequent TC for the 21 mm x 21 mm x 750 um die solder bump package with and without PEDL.

Test Vehicle	Electrical test (failure)											
	TC=0		TC=500		TC=1000		TC=2000		TC=3000		TC=3500	
	Resistance	Leakage	Resistance	Leakage	Resistance	Leakage	Resistance	Leakage	Resistance	Leakage	Resistance	Leakage
With PEDL	0/21	0/21	0/21	0/21	0/21	0/21	0/21	0/21	0/21	0/21	5/21	0/21
Without PEDL	0/21	0/21	0/21	0/21	0/21	0/21	0/21	0/21	4/21	0/21	9/21	0/21

4.5 New Benchmark Values for Delamination Stresses and ΔW

In the parametric study described in Section 4.3, reliability benchmark values for delamination stresses and ΔW were obtained from the 2D FEA of an existing 15 mm x 15 mm die package, and used to predict package reliability. Although it was possible to design a solder-bump interconnected package to pass all the benchmark values, it was not possible to pass the $\sigma_{y,dp}$ stress benchmark for the Cu-post interconnected package. Since experimental tests on the test vehicles A, B and C have now been conducted and shown to pass TC1000 without delamination of the low-k layer or fatigue failure of the solder joints, 2D FEA was performed on the three test vehicles and a new set of benchmark values for the delamination stresses and ΔW was obtained by taking the highest values from all the test vehicles tested. The FEA results for all the test vehicles are given in Table 4.13. The new reliability benchmark values are shown in the last line of Table 4.13.

Table 4.13: FEA results for all test vehicles tested and new reliability benchmark

Test Vehicle	$\sigma_{xy,de}$ (MPa)	$\sigma_{xy,dp}$ (MPa)	ΔW ($J.m^{-3}$)	$\sigma_{y,de}$ (MPa)	$\sigma_{y,dp}$ (MPa)
A: Thick die (750um) with PEDL	62.68	36.22	1.281	-71.35	9.10
B: Thin die (300um) with PEDL	53.13	27.76	0.989	-60.96	5.29
C: Cu-post with thick die (750um) without PEDL	80.41	70.66	1.622	-261.57	10.62
15mm x 15mm x 750um die without PEDL (Old Benchmark)	107.95	61.20	1.790	-293.30	5.98
New Reliability Benchmark	107.95	70.66	1.790	-293.30	10.62

4.6 Summary

From the above studies, the following conclusions can be made in respect of the structural design of large flip chip packages:

1) PEDL can help to reduce the stresses at the low-k layer and improve solder bump reliability by approximately 1.5 times.

2) Using BCB instead of underfill as the bevel cut material reduces the stresses in the low-k but the reduction is negligible. As such underfill is actually recommended as it has less fabrication steps and more cost effective.

3) Both thin substrate and thin die are recommended to reduce the stresses in the low-k layer and enhance solder joint reliability. A substrate thickness of 0.6 mm and a die thickness of 300 um using underfill E have been found to optimize the structural requirements for a 21 mm x 21 mm die package with solder bump interconnects. This was subsequently confirmed experimentally although a different underfill was used.

4) Cu-post interconnects can be used to reduce the ΔW to enhance solder joint reliability but may increase the tensile stresses in the low-k material under the die pad associated with the outermost solder bump and increase the possibility of delamination there.

5) Increase in the height of Cu-posts from 80 um to 120 um helps to reduce the stresses in the low-k layer at the die edge but the reduction is not significant.

6) It has been demonstrated experimentally, that for the case where Cu-post interconnects and 1 layer of FSG are specified for a 21 mm x 21 mm die package, acceptable reliability can be achieved if a good underfill with bevel cut, 80um Cu-post height, 750um die thickness and 0.6 mm substrate thickness were used.

7) Optimization of the structural design of a large die Cu/low-k flip chip package was achieved through finite element analysis and the use of reliability benchmark values of delamination stresses and ΔW obtained from experimental tests carried out on actual packages. New reliability benchmark values of delamination stresses and ΔW have been obtained which can be used to aid the structural design of large die flip chip packages.

CHAPTER 5

Optimization of Reliability of Copper-Low k Flip Chip Package with Variable Interconnect Compliance

5.1 Background of variable interconnect compliance

With cyclic changes in temperature, due to the mismatch in CTE between die and substrate, inelastic energy dissipation W per temperature cycle will occur in the solder joints of a flip chip package which will lead to fatigue failure of the solder joints. The critical solder joint with the greatest W is usually furthest away from the center (neutral point) of the chip. In order to reduce the W induced in the solder joints, and hence improve the fatigue life of the joints, studies have been made on the effect of chip-to-substrate interconnect compliance on the fatigue life of solder joints [47, 48]. Conventionally, all interconnects are identical and hence have the same compliance. It was found that if this compliance is varied, there exists an optimum value which gives maximum reliability. However, it was also further found [47, 48] that the fatigue life of the solder joints can be further optimized if the compliance of the interconnects on the chip are varied such that stiffer interconnects are placed in the central region of the chip while more compliant interconnects are placed towards the periphery of the chip.

Borgesen and Li [49] analysed the stresses in flip-chip solder joints of spherical (convex) and hourglass (concave) shapes. They showed that the maximum tensile stress in the critical interconnect is lower if the solder joints were all of the hourglass shape compared to the situation when the joints were all spherical. Kacker [50] compared the reliability of flip-chip packages employing three different arrangements namely the high-

compliance G-Helix interconnects, stiff column interconnects, and a mixture of interconnects are used - stiff copper column interconnects in the central region of the package, high-compliance G-Helix interconnects at the perimeter and low-compliance G-Helix in the region in between. They found that the high-compliance G-Helix interconnects gave the best reliability. In this chapter, finite element analysis will be used to investigate the reliability for flip chip packaging using variable interconnect compliance.

5.2 3D finite element modeling

A 3D plane-strain finite element analysis was performed on a diagonal strip of a 21mmx21mm Cu/low-k chip with 4.525um thick low-k layer, 5.6um FTEOS layer, 1.5um silicon oxide layer, 3.5um passivation layer, 750um thick die and 1.0mm thick substrate. There are 20 rings of solder joints (height 60um, pad diameter 80um) around the periphery of the chip at a pitch of 150um which gives a total number of interconnects of about 11000. The distance between the outermost row of solder joints from the edge of the die is 150um. Three parametric cases involving different geometries of solder joints were analyze: (A) All 20 rows with spherical solder joints, (B) 10 hourglass joints followed by 10 spherical joints, and (C) 10 spherical joints followed by 10 hourglass joints. The following assumptions were made:

- The temperature change is assumed to be the same throughout the package.
- Perfect adhesion is assumed at all material interfaces.
- All materials are modeled as elastic materials except the solder material.
- A viscoplastic constitutive relation is adopted for the lead-free solder.

The visco-elastic behavior of the lead free solder joint is modeled after Anand [51, 52]. The maximum ΔW in the solder joint has been used as an indicator of the reliability of the joint. The greater the ΔW in the joint, the lower the reliability (fatigue life).

Fig. 5.1 shows the slice model created in the software. Table 5.1 shows the material properties used in the analysis. Fig 5.2 and Fig 5.3 show the detailed model for the different shapes of solder joints employed. The 3D model uses 14343 8-node hexahedron elements and 20045 nodes. On both cut surfaces, a state of general plain strain is imposed. As a result this model actually simulates a package with infinite extent in the direction perpendicular to the plane of the slice. This 3D model will be able to capture a complete description of the solder balls, leading to a more accurate definition of the stress and strain state within the interconnects as compared to a 2D model.

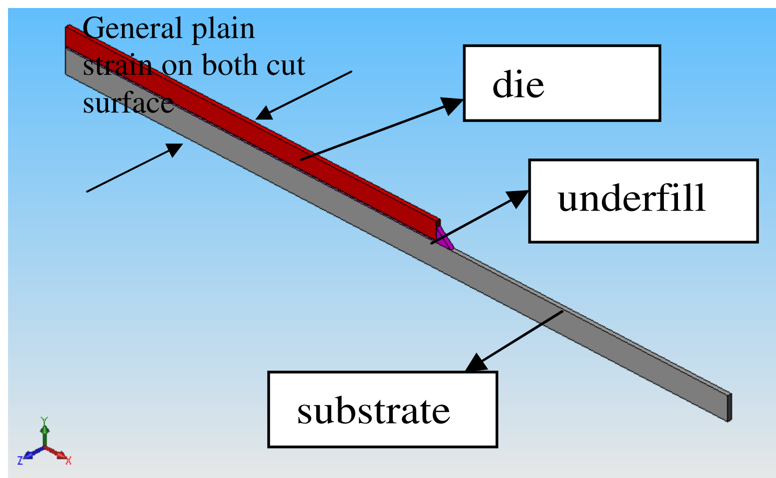


Fig. 5.1. 3D slice model from centre to corner of die

Table 5.1. Material properties used

Materials	CTE (ppm/C)	Young's Modulus (GPa)	Poisons Ratio
Silicon	2.7	131	0.28
Low-k	23	7.7	0.30
Oxide	0.57	66	0.18
FSG	0.25	70	0.16
Underfill	40.75	6.16	0.30
Lead free Solder	22	44.4 (25°C), 18.8 (125°C)	0.40
Substrate	16	24.5	0.22
Polyimide	3.5	35	0.35

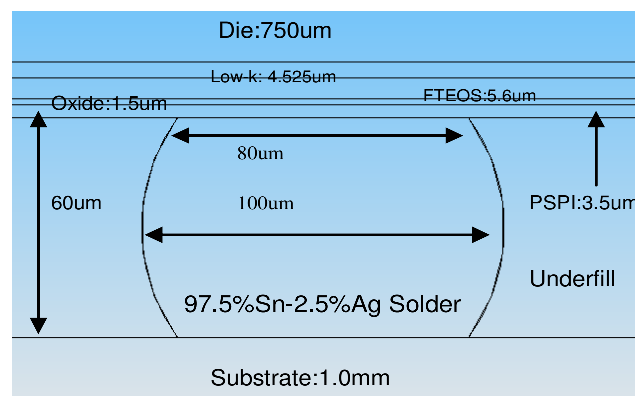


Fig. 5.2. The detailed model for the lead free spherical joint.

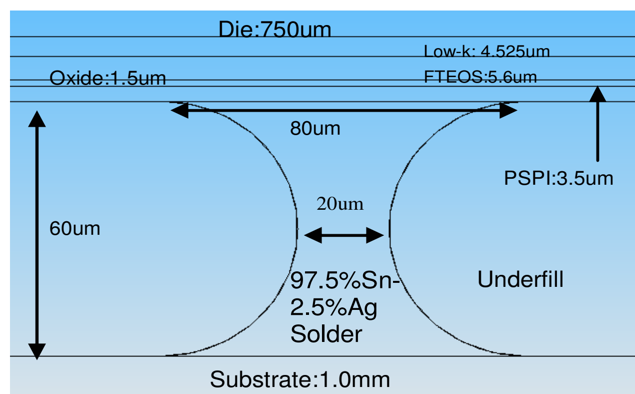


Fig. 5.3. The detailed model for the lead free hourglass joint.

5.3 Results and Discussion

5.3.1 Effect of the shape of solder joints used

Figs. 5.4, 5.5 and 5.6 show the transparent view of the 3 parametric cases (20 spherical solder joints, 10 hourglass joints followed by 10 spherical joints, 10 spherical joints followed by 10 hourglass joints) that were analysed, respectively. The packages were subjected to an external thermal loading condition, which is a temperature cycling between 125°C to -40°C where 125°C was the stress-free condition. Fig. 5.7 shows the plot of the temperature cycles with 15 min hold time and 15 min ramp time. ΔW per TC cycle from 125ºC to -40ºC in the joint was obtained for comparative study. The 4th cycle of loading was chosen since the ΔW had converged by the 4th cycle as shown in Fig.5.8 and Table 5.2. The solder was assumed to be a viscoplastic material while the rest of the materials were modeled as temperature-independent linear elastic materials.

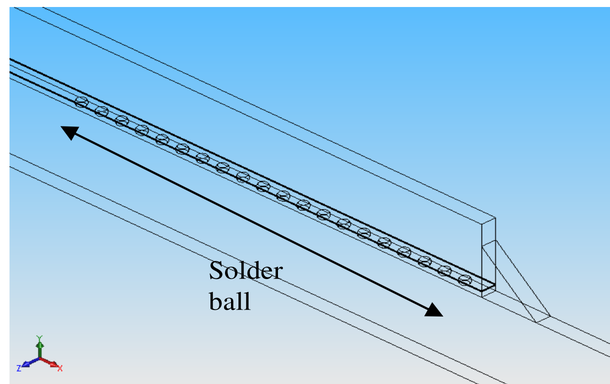


Fig. 5.4. 20 spherical joints along the diagonal

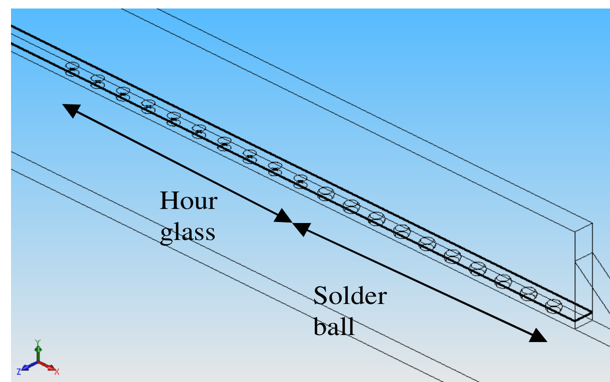


Fig. 5.5. 10 hourglass joints followed by 10 spherical joints

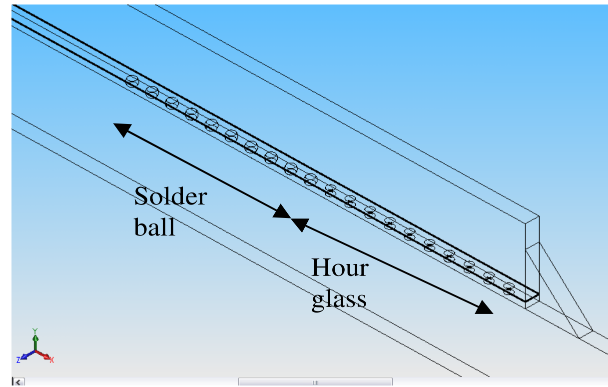


Fig. 5.6. 10 spherical joints followed by 10 hourglass joints

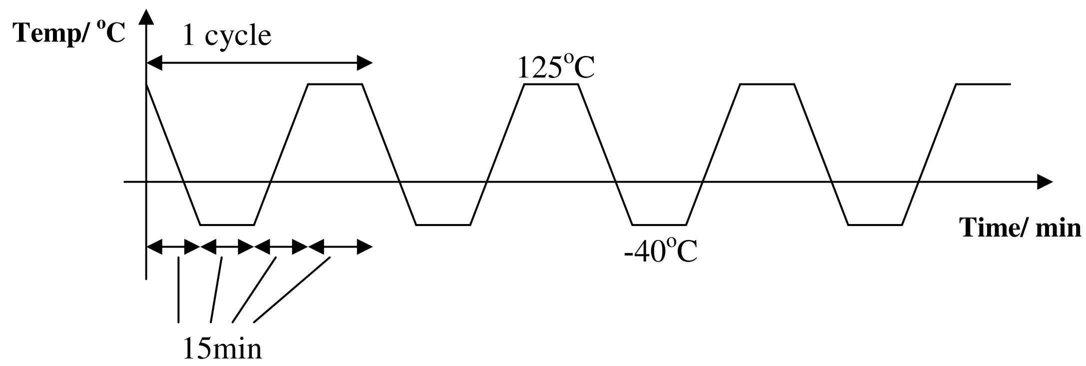


Fig. 5.7 Thermal cycling (TC) from 125ºC to -40ºC with 15 min hold time and 15 min ramp time

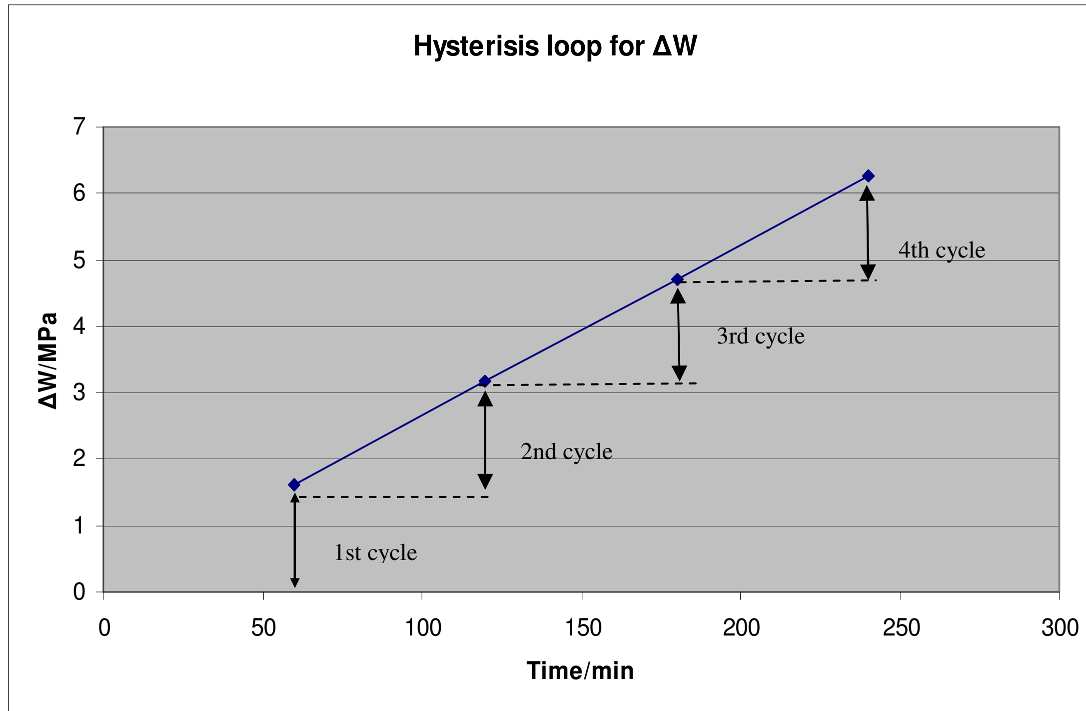


Fig. 5.8 Strain Energy Density (MPa) ΔW at the end of each cycle for the case of with all joints spherical

Table 5.2 ΔW at the end of each cycle for the case with all joints spherical.

Time/min	ΔW/ MPa
60	1.6022 (1st cycle)
120	1.5648 (2nd cycle)
180	1.5411 (3rd cycle)
240	1.5383 (4th cycle)

From Table 5.3 it was shown that the maximum ΔW in the critical joint is 21.2% higher with a value of 1.7504MPa if the joints were all of the hourglass shape compared to the situation when the joints were all spherical with a value of 1.5383MPa. It was

further shown that if the joints in the inner region were of the stiffer spherical shape and those near the perimeter of the package were of the hourglass shape, the best reliability could be achieved with an improvement of 8.5%. Fig 5.9 shows the joints at the edge of the die for the case 10 spherical joints followed by 10 hourglass joints

Next we compared the von mises stresses induced in the low-k material (refer to Fig. 5.10) during underfill reflow from 260ºC to -55ºC. It was again shown that if the joints in the inner regions were of the stiffer spherical shape and those near the perimeter of the package were of the hourglass shape, the minimum stress with a value of 250.8MPa was induced in the low-k material.

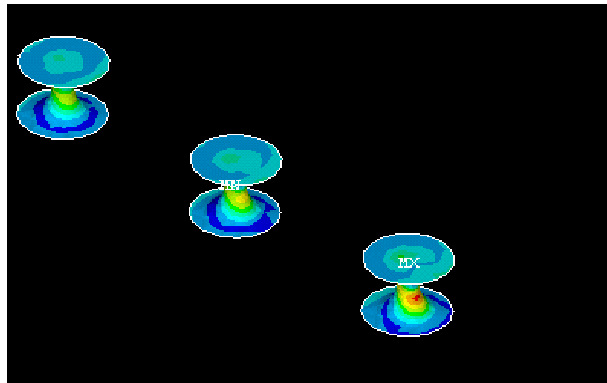


Fig. 5.9 Critical hourglass joints at the edge of die

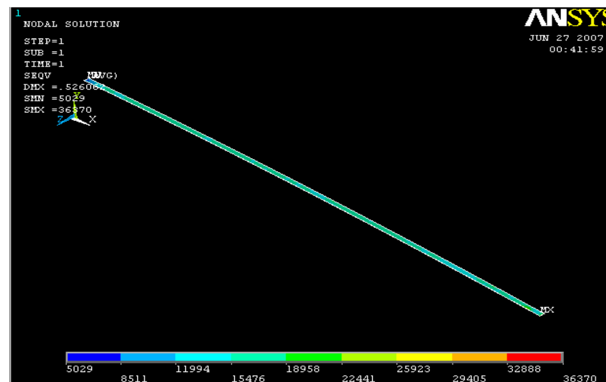


Fig 5.10 Von mises stress in the low-k material for 10 spherical joints followed by 10 hourglass joints

Table 5.3 Results for different shapes of solder

Different shapes of solder	Max. Von mises Stress in low-k at die edge		ΔW	
	Magnitude (MPa)	% increase	Magnitude (MPA)	% increase
20 spherical joints (reference)	282.9	-	1.5383	-
10 hourglass joints followed by 10 spherical joints	345.6	22.16	1.7504	13.78
10 spherical joints followed by 10 hourglass joints	250.8	-11.34	1.4079	-8.47

5.3.2 Effect of die thickness

A parametric study was done to investigate the impact of the die thickness on stress values and W induced. Analyses were performed for 3 cases of die thickness (750, 400, 100um) for the 21 X 21mm die size with 10 spherical joints followed by 10 hourglass joints. The results are tabulated in Table 5.4. The results show a similar trend in that the stress values in the low-k material and ΔW in the solder joints decreases gradually as the die gets thinner.

Table 5.4 Results for variation of die thickness

Die thickness	Max. Von mises Stress in low-k at die edge (MPa)	ΔW/ MPa
750um	250.8	1.4079
400um	221.6	1.3022
100um	201.3	1.2561

5.3.3 Effect of substrate thickness

Next, analyses were performed for 2 cases of substrate thickness (1.0, 0.6mm) for the 21 X 21mm die with a thickness of 100um, with 10 spherical joints followed by 10 hourglass joints (refer to Fig. 5.11). From Table 5.5 all the stated values decrease as the

substrate thickness decreases. A substrate thickness of 0.6mm and a die thickness of 100um with 10 spherical joints followed by 10 hourglass joints is a possible design for the 21 X 21mm chip.

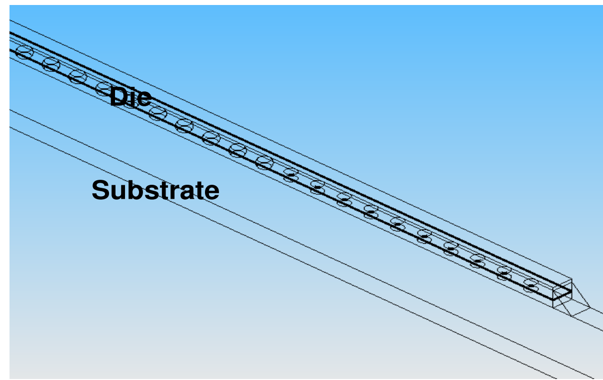


Fig 5.11. Schematic view of a flip chip package with 100um die thickness and 0.6mm substrate thickness using 10 spherical joints followed by 10hourglass joints

Table 5.5. Results for variation of substrate thickness

Substrate thickness	Max. Von mises Stress in low-k at die edge (MPa)	ΔW/ MPa
1.0mm	201.3	1.2561
0.6mm	190.2	1.1964

5.4 Summary

From the above studies, the following conclusions can be made on the optimization of the structural design of a large die using variable interconnect compliance

1. A variable compliance solder joint configuration where stiffer joints are placed in the central region of the chip and more compliant joints at the periphery of the chip, can give rise to greater reliability.

2. A variable compliant configuration also led to the lowest stress in the low-k layer, resulting in greater reliability.
3. Reliability increases with decrease of die thickness and substrate thickness.

CHAPTER 6

CONCLUSION

6.1 Conclusions

In this study, the modeling techniques used for 2D and 3D simulations have been shown to agree well with the modified Suhir's solution proposed by Tsai. The models are further applied in 2D and 3D parametric studies.

We have arrived at the following observations which can be used to optimize the structural design of an IC package with a large die. Two layers of FSG is a better cushion to reduce the stresses in the low-k layer as compared to one layer. PEDL can help to reduce the stresses at the low-k corner. Using BCB instead of underfill as the bevel cut material reduces the stresses in the low-k but the values are negligible. As such underfill is actually recommended as it has less fabrication steps and more cost effective. Both thin substrate and thin die are recommended to reduce the stresses in the low-k and enhance the solder joint reliability. Comparing with our benchmark stresses and ΔW a thickness of 0.6mm substrate and 300um die thickness using underfill E can optimize the structural requirement for a die size of 21 X 21mm. Cu-post interconnects can be used to reduce the ΔW to enhance solder joint reliability but by doing so will increase the tension and compressive forces in the low-k material under the last bump. Increasing the height of the Cu posts can help to reduce the stresses in the low-k layer. However the reduction is not significant. The stresses in the low-k layer under the last bump is still very high. High Tg, low CTE and low young modulus underfill are advantageous as they lead to lower

stress in the low-k layer and lower ΔW in the solder joints. Among the 11 underfills considered, three which have high Tg, low CTE and low young modulus are recommended. In the case where Cu-post interconnects and 1 layer of FSG is needed, using a good underfill with bevel cut, 80um Cu-post height, die thickness of 300um and substrate thickness of 0.6mm, the structural requirement for 21 X 21mm die size looks promising. However further improvement is still required to make it work.

To optimize the structural design for large die using variable interconnect compliance, a variable compliance solder joint configuration where stiffer joints are placed in the central region of the chip and more compliant joints at the periphery of the chip, can give rise to greater reliability. A variable compliant configuration also led to the lowest stress in and hence maximum reliability of the low-k layer. Reliability decreases with increase of die thickness and substrate thickness.

6.2 Suggestions for Future Study

Using ultra-low-k materials as a dielectric material in the backend interconnects, the introduction of porosity is a necessity. However, this reduces the mechanical strength of the materials, which makes the integration process more difficult. The interfacial strength between ultra-low-k dielectric and interconnect materials has been found to be much weaker than conventional dielectric materials. This effect is exaggerated during packaging when the chip undergoes thermal loading. Cases of delamination between ultra low-k and adjacent materials are often seen after thermal loading during packaging. Understanding the mechanical properties of these thin films and choice of appropriate

mechanical performance is necessary for successful full-scale integration into a reliable packaged product.

So far in this study, we have managed to derive the driving crack energy between the interconnects during thermal loading using numerical methods. But experimental results are also needed to quantify the adhesion strength between the thin layers. Theoretically if the driving crack energy in between the thin films is greater than the corresponding adhesion strength, delamination will occur.

In the market there are currently nine methods that have been used to calculate the interface adhesion strength between thin films, namely the 4-point bending, 3 point bending, nanoindentation, nanoscratch, modified decohesion test, single strip decohesion test, peel test, pull test and blister test. Each has its own pros and cons. The use of each method to calculate the adhesion strength of thin films should be analyzed. After which the best and most accurate method should be selected to use on ultra low-k materials.

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APPENDIX A

Properties of Underfill E

Temperature/^{o}C	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poissons Ratio
45	32	6.16	0.3
65	32	5.61	0.3
85	32	5.01	0.3
105	95	4.06	0.3
125	95	1.11	0.3

Properties of Underfill I

Temperature/^{o}C	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poissons Ratio
45	40	4.38	0.3
65	40	4.19	0.3
85	40	4.04	0.3
105	40	3.92	0.3
125	40	3.71	0.3

Properties of Underfill J

Temperature/^{o}C	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poissons Ratio
45	30	6.30	0.3
65	30	6.06	0.3
85	30	5.90	0.3
105	30	5.75	0.3
125	102	5.51	0.3

Properties of Underfill K

Temperature/^{o}C	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poissons Ratio
45	25	5.33	0.3
65	25	4.82	0.3
85	25	4.32	0.3
105	100	3.92	0.3
125	100	3.43	0.3