SCHOTTKY SOURCE/DRAIN TRANSISTOR INTEGRATED WITH HIGH-K AND METAL GATE FOR SUB-TENTH NM TECHNOLOGY

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A THESIS SUBMITTED
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2008

ACKNOWLEDGMENTS

I wish to express my sincere appreciation to my supervisors Dr. Sung-Joo Lee (Department of Electrical and Computer Engineering) and Dr. Dong-Zhi Chi (Institute of Materials Research and Engineering) for their continuous encouragement, advice and support throughout this research project.

I would like to thank Dr. Shiyang Zhu from the Institute of Microelectronics for his helpful advice and guidance during the first year of my PhD study. My gratitude also goes to Dr. Minghui Hong and Dr. Wendong Song from the Laser Microprocessing Lab for their great help on laser annealing.

I gratefully acknowledge all of my lab fellows for their help on research, learning, and many other aspects during the past a few years: Fei Gao, Sung Jin Whang, Nan Wu, Qingchun Zhang, Xiongfei Yu, Chi Ren, Moon Sig Joo, Jinghao Chen, Sung Jung Kim, Yingqian Wang, Chen Shen, Jingde Chen, Xinpeng Wang, Yan Song, Rinus Tek-Po Lee, Kian Ming Tan, Wan Sik Hwang, Andy Eu-Jin Lim, Zerlinda Tan, Chia Ching Yeo, Debora Poon, Samanta Santanu Kumar, Eric Yeow-Hwee Teo, Jia Fu, Wei He, Hui Zang, Gang Zhang, Yi Tong, Jing Pu, Hoon-Jung Oh, Yu Fu Yong, Patrick Tang, Wai Linn O-Yan, Boon Tech Lau and many others from the Silicon Nano Device Lab; In particular, I wish to express my sincere thanks to Fei Gao, Sung Jin Whang, Rinus Tek-Po Lee, Kian Ming Tan, Wan Sik Hwang, Chen Shen, for their innumerable helpful discussion and constructive suggestions on device fabrications, characterizations as well as data analyses in this project.

The financial support from the National University of Singapore is also gratefully acknowledged.

My special recognition goes to Jidong Huang for his help. He has always been with me during the most difficult moments in this journey.

Finally, I would like to thank my parents for their love, constant support and encouragement in all of my life.

CONTENTS

SUMMARY

As complementary metal-oxide semiconductor (CMOS) transistors scale beyond 45 nm technology node, several key innovations become more and more attractive in different aspects, including: high-k gate dielectric and metal gate to provide the possibility that equivalent oxide thickness scales to less than 1 nm, high mobility channel materials for increment of carrier saturation velocity, and Schottky barrier source/drain structure for shallow and sharp junction with low resistance. This project explores the feasibility of integration of germanide Schottky source/drain Ge channel MOSFET with high-k gate dielectric and metal gate for sub-tenth nm technology application.

The comprehensive knowledge on metal germanide properties is essential for the successful replacement of doped source/drain with metal germanide Schottky source/drain. Therefore systematic studies on Ni- and Pt- germanide for Ge p-MOSFET application have been carried out. Both the germanides offer promising merits: low effective hole barrier height, morphological stability, low resistance and abrupt junction with germanium. Ge p-MOSFETs with Ni- or Pt- germanide Schottky source/drain are also successfully fabricated on n-Ge-substrate with chemical vapor deposition (CVD)-HfO_2/TaN gate stack. Improved junction forward and reverse current were obtained from Ni- and Pt- germanide source/drain junction compared to conventional B-doped p^+/n junction. In addition, the higher drive-on current and lower drive-off current were also obtained from Pt-germanide MOS field effect transistor (MOSFET) than conventional Ge-pMOSFET.

Exploration of metal germanide for Ge n-MOSFET application has been focused in two material groups: i) rare earth metal germanide, such as Er- and Yb- germanide, which has a low metal work function, and ii) NiGe with modified electron barrier height. By introducing an interfacial Sb layer, NiGe was found to show low resistivity and low electron barrier height simultaneously, which make NiGe with such modification a good ohmic contact material to n^+ source/drain regions as well as a promising Schottky source/drain candidate for Ge n-MOSFETs.

Laser annealing was introduced as an alternative germanide source/drain formation technique to conventional rapid thermal annealing, providing the advantages of local selective heating of specific regions and reduced thermal budget. A smooth and uniform Pt-germanide film has been obtained through laser annealing, with effective hole barrier height as low as 0.12~0.14 eV. A Ge p-MOSFET with Pt-germanide Schottky source/drain formed by laser annealing was successfully demonstrated with well-behaved output and transfer characteristics.

List of Figures and Tables

List of Symbols and Abbreviations

A	Area of the capacitor
A^*	Richardson's constant
Å	Angstrom
CET	capacitive equivalent thickness
CMOS	Complementary metal-oxide-semiconductor
C_{inv}	Gate to channel capacitance under inversion per unit area
DHF	Diluted HF solution
D_s	Density of interface states
σ	Thickness of interfacial layer
ε_0	Permittivity of the vacuum ($8.85\times10^{-3}\ fF/\mu m$)
E_C	Conduction band edge of semiconductor
E_V	Valence band edge of semiconductor
E_F	Fermi level of semiconductor
EOT	Equivalent oxide thickness
ER	Etching rate
ϕ_b	Barrier height of the metal/Ge contacts
ϕ_m	metal work function
ϕ_{bh}	Hole barrier height from metal to semiconductor
ϕ_{be}	Electron barrier height from metal to semiconductor
HRTEM	High resolution TEM
IC	Integrated circuit
ICP	Inductively coupled plasma
ITRS	International Technology Roadmap for Semiconductors
I	Current
I_d^n	Drive current of nMOSFETs
I_d^p	Drive current of pMOSFETs

I_d	Drive current of MOSFETs
$I_{d,sat}$	MOSFET saturation current
I_f	Diode forward current
I_{off}	MOSFET off-state current
I_{on}	MOSFET on-state current
I_s	Diode saturation current
I_r	Diode reverse current
K	Boltzmann constant
k	Relative permittivity (dielectric constant) of dielectric
k_{high-k}	Relative permittivity of the high-k gate dielectric
L	Length of transistor channel
LPCVD	Low-pressure chemical vapor deposition
MIGS	Metal-induced gap states
MOSFET	Metal-oxide-semiconductor field effect transistor
MOCVD	Metal-organic chemical vapor deposition
n	Ideality factor
μ	Channel carrier mobility
$\mu_{electron}$	Mobility of electron
μ_{hole}	Mobility of hole
ρ	Resistivity of material
PC	Photocurrent
PDA	Post deposition anneal
PECVD	Plasma Enhanced Chemical Vapor Deposition
PR	Photo-resist
PVD	Physical vapor deposition
q	Electronic charge
QMCV	Quantum-Mechanical CV simulator
R_s	Sheet resistance,
REM	rear earth metal
RIE	Reactive Ion Etch

RTA	Rapid thermal annealing
RTO	Rapid thermal oxidation
RTP	Rapid thermal process
S	Slope parameter of ϕ_b as function of ϕ_m
SEM	Scanning Electron Microscopy
SIA	Semiconductor Industry Association
SIMS	Secondary ion mass spectrometry
SSDT	Schottky Source and Drain Transistor
S/D	Source/drain
GOI	Ge-On-Insulator
T	Temperature
TEM	Transmission Electron Microscopy
t_{high-k}	Physical thickness of the high-k gate dielectric
t_{inv}	CET of the gate dielectric
t_{poly}	CET contribution from poly depletion effect from the poly-Si gate
t_{QM}	CET contribution from quantum mechanical effect from the channel.
t_{ox}	EOT of the gate dielectric
$\bar{\tau}$	Average switching response time of the IC
V	Voltage
V_d	Drain voltage
V_f	Forward voltage bias to diode
V_g	Voltage applied to the transistor gate
V_{th}	Threshold voltage of transistor
V_r	Reverse voltage bias to diode
V_{FB}	Flatband voltage
W	Width of the transistor channel
XPS	X-ray photoelectron spectroscopy
XRD	X-Ray Diffraction

Chapter 1

Introduction

As the beginning of this thesis, in this chapter I will start with a brief introduction to metal-oxide-semiconductor field effect transistor (MOSFET) and its scaling trend. The challenges associated with MOSFET scaling down will be discussed. Subsequently, to overcome the challenges, high-k gate dielectric, metal gate and Schottky source/drain structure will be introduced respectively. Finally the objectives to be achieved in this project and organization of this thesis will be given.

1.1 Introduction to MOSFET

Since the invention of the integrated circuit (IC) some forty years ago, engineers and researchers around the world have been continuously working on realization of better circuit performance with a smaller chip size and lower manufacturing cost. Actually, the semiconductor industry has been very successful in providing continuous achievements on system performance improvement year after year. In 1992, the Semiconductor Industry Association (SIA) published the international technology roadmap for semiconductors (ITRS) which basically affirms the development to follow closely with Moore's law [1.1], i.e. the number of transistors per unit area on IC doubles approximately every 18 months. It was also pointed out by Moore that reduction of cost per function is the driving force behind the exponential increase in transistor density. This exponential reduction in cost per function, which driving improvement of microprocessor

performance and growth of the information technology and semiconductor industry, however, leads to the shrinking of the transistor feature size approaching its fundamental limits in the traditional silicon-based IC technology today. The dramatic decrease in transistor feature size and cost per transistor during the last three decades are shown in Fig 1.1.

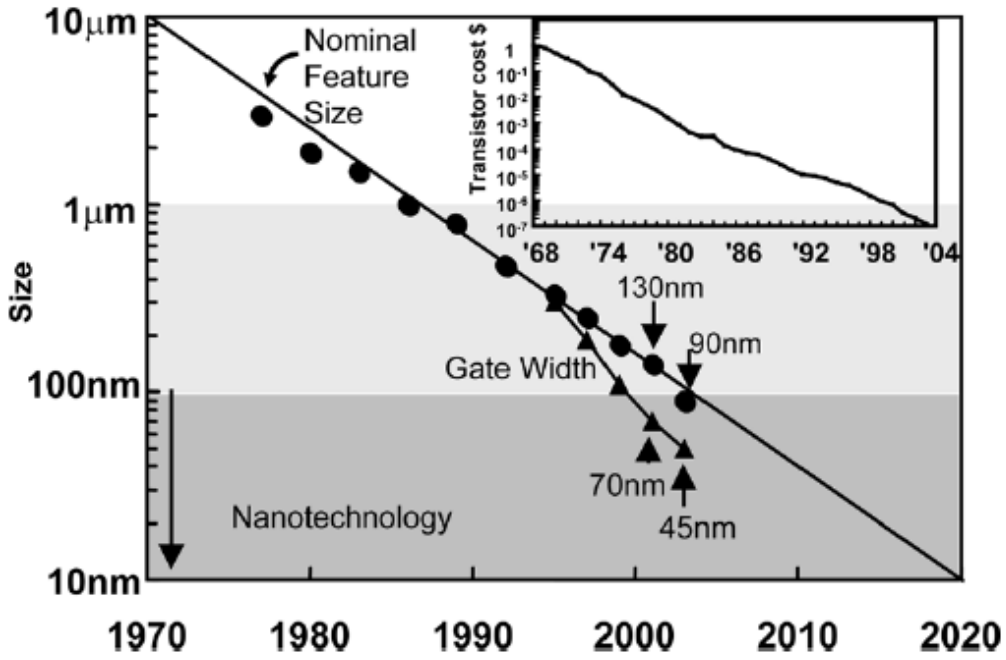

Figure 1.1 Technology and transistor feature size and transistor cost versus year (after [1.2]).

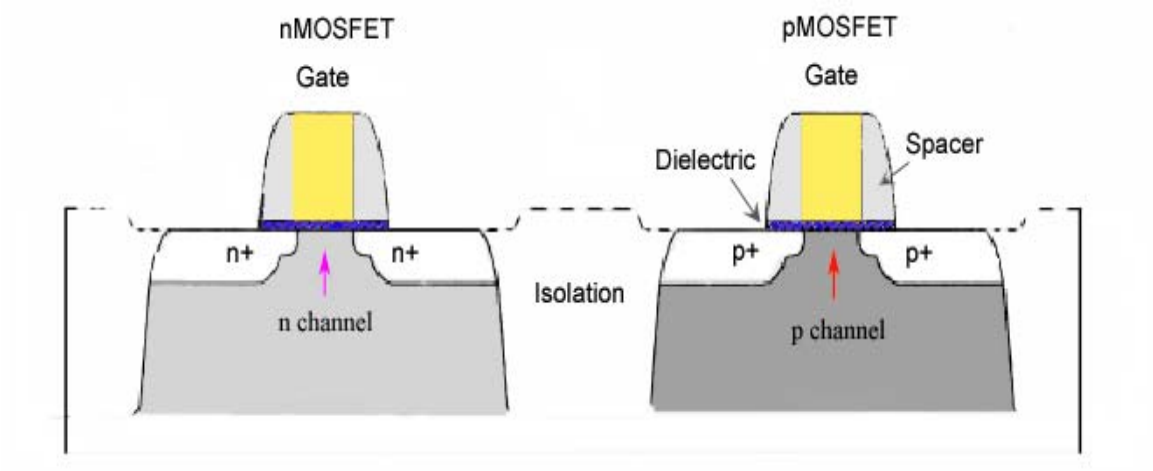

Figure 1.2 Schematic illustration of a complementary MOSFET (CMOSFET).

Among various semiconductor devices, the most important device used in modern circuits is the MOSFET. A schematic illustration of a complementary metal-oxide-semiconductor (CMOS) consists of an n-MOSFET and a p-MOSFET is shown in Fig. 1.2.

One of the most important parameter to evaluate the performance of an IC is the dynamic response (i.e. charging and discharging) of load capacitance, associated with a specific circuit element and the supply voltage provide to the element at a representative (clock) frequency. A common element employed to examine such switching time effects is a CMOS inverter where the input signal is attached to the gates and the output signal is connected to both an NMOS and a PMOS transistor as shown in Fig. 1.3. The switching time is limited by both the fall time required to discharge the load capacitance by the NMOS drive current and the rise time required to charge the load capacitance by the PMOS drive current. The average switching response time ($\bar{\tau}$) of an inverter is given by [1.3]

$$\bar{\tau} \propto \frac{1}{I_d^n + I_d^p} \tag{1.1}$$

where I_d^n and I_d^p are the drive current of n- and p-MOSFETs, respectively. The performance of an IC then can be characterized through this switching response time. It is easily seen that to achieve a decrease in $\bar{\tau}$ (higher switching speed, better IC performance), increase in the drive current I_d of the n- and p-MOSFETs is required. Therefore, the improvement of IC performance can be taken as linked to the enhancement of drive current I_d associated with the MOSFETs.

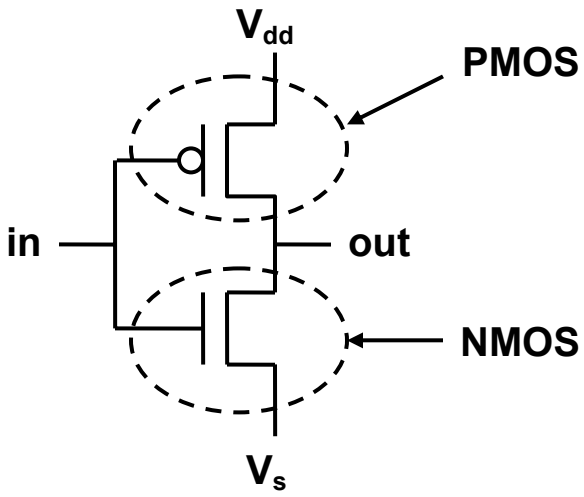

Figure 1.3 Schematics of a CMOS inverter where V_s and V_{dd} serve as the source and drain voltages, respectively.

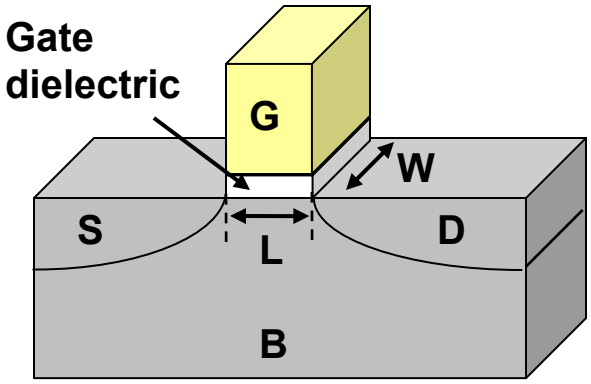

Figure 1.4 Sketch of a typical MOSFET structure on a bulk (B) substrate, in which L and W represent the channel length and width, respectively. When the channel is inverted with a voltage applied on the gate (G), carriers can flow from the source (S) to drain (D) forming the drive current of the MOSFET.

Figure 1.4 shows a sketch of a typical MOSFET structure on a bulk substrate. When a voltage is applied on the gate to invert the channel and a potential drops between source and drain, carriers flow from the source to drain and form the drive current of the transistor. The saturation drive current $I_{d,sat}$ is given by [1.4]

$$I_{d,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_g - V_{th})^2}{2} \tag{1.2}$$

where

W : the width of the transistor channel

L : the length of transistor channel

μ : the channel carrier mobility

C_{inv} : the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state

V_g : the voltage applied to the transistor gate

V_{th} : the threshold voltage of transistor.

According to Eq. (1.2), to achieve an increase of drive current $I_{d,sat}$ for a given power supply voltage can be taken as to modify the values of the parameters in the right side of the equation. However, increase of the term $(V_g - V_{th})$ is limited in range due to reliability considerations and room temperature operation constraints. Increase of the channel width W is contrary to the scaling of device dimension. The channel length L has been continually reduced and is approaching its fundamental limits today. Therefore, the remaining approaches to enhance the drive current $I_{d,sat}$ and eventually improve MOSFET performance are increases of either the gate dielectric capacitance density C_{inv} or the channel carrier mobility μ, or both of them.

1.2 High-k gate dielectrics and metal gate

The MOS gate structure in a transistor (see Fig. 1.4) can be simplified as a parallel plate capacitor. The gate capacitance C_{inv} can be given by [1.5]

$$C_{inv} = \frac{k \cdot \varepsilon_0 \cdot A}{t_{inv}} \tag{1.3}$$

where

k : the relative permittivity (i.e. dielectric constant) of dielectric ($\kappa = 3.9$ for SiO_2)

ε_0 : the permittivity of free space ($8.85 \times 10^{-3}\ fF/\mu m$)

A : the area of the capacitor

t_{inv}: the capacitive equivalent thickness (CET) of the gate dielectric.

With a traditional ploy-Si gate, t_{inv} consists of the following three CET components:

$$t_{inv} = t_{poly} + t_{ox} + t_{QM} \tag{1.4}$$

where

t_{poly}: contribution from poly depletion effect from the poly-Si gate

t_{QM}: contribution from quantum mechanical effect from the carriers channel.

t_{ox}: the main part of t_{inv} attributes to the gate dielectric, also known as equivalent oxide thickness (EOT).

Therefore, an increase of C_{inv} requires the decrease in t_{inv}. Among the three CET components of t_{inv}, t_{QM} is attributed to intrinsic mechanism which cannot be eliminated; t_{poly} comes from the poly-Si gate, thus can be eliminated by replacing poly-Si gate with metal gate. One of the most widely studied metal gate materials, Tantalum Nitride (TaN), was used as metal gate in this project. The down scaling of t_{ox}, the main component of t_{inv}, has been continuous during the past several decades with the thinning of the physical thickness of SiO_2 gate dielectric. However, it is known that a minimum thickness of 7 Å for SiO_2 is required to maintain its bulk properties, such as its band gap. Furthermore, when gate leakage current is taken into consideration, the practical limit for SiO_2 thickness scaling becomes 10-12 Å [1.6], which makes industry face a great challenge on high performance device scaling after 2007 as shown in Table 1.1.

Table 1.1. Near-term high-performance logic technology requirements in ITRS 2005 [1.7].

Year of Production	2006	2007	2008	2009	2010	2011	2012
DRAM 1/2 Pitch (nm) (contacted)	70	65	57	50	45	40	36
MPU/ASIC Metal1 1/2 Pitch (nm) (contacted)	78	68	59	52	45	40	36
MPU Physical Gate Length (nm)	28	25	23	20	18	16	14
EOT for extended planar bulk (Å)	11	11	9	7.5	6.5	5	5
Effective NMOS $I_{d,sat}(\mu A/\mu m)$ (extended planar bulk) ($I_{d,sat}$ of PMOS is ~ 40-50%)	1130	1200	1570	1810	2050	2490	2300
Mobility Enhancement Factor for $I_{d,sat}$ (extended planar bulk)	1.09	1.08	1.09	1.10	1.10	1.12	1.11

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

Fortunately, the application of high-k gate dielectrics in recent decade allows people to use physically thicker dielectric film therefore reduce the gate direct tunneling current while maintains the same EOT of a thin SiO_2 gate dielectric. The physical thickness of an alternative high-k dielectric to achieve the equivalent capacitance density with t_{ox} of a SiO_2 can be obtained from the expression

$$t_{high-k} = \frac{t_{ox}(EOT)}{3.9} \cdot k_{high-k} \tag{1.5}$$

where

t_{QM} : contribution from quantum mechanical effect from the carriers channel.

t_{high-k} : the physical thickness of the high-k gate dielectric

k_{high-k} : the relative permittivity of the high-k gate dielectric

In the past few years, a number of studies has been carried out on high-k metal oxides and several promising high-k gate dielectric candidates have been identified, such as La_2O_3, HfO_2 and Hf-based pseudo-binary alloys (HfSiO, HfSiON, HfTaO, and HfLaO). In this project, HfO_2 was used as gate dielectric for its higher k value, relatively simple formation techniques and good interface with Ge after substrate passivation.

1.3 High mobility channel materials

As stated in Section 1.1, another way to enhance the drive current $I_{d,sat}$ and eventually improve MOSFET performance is to increases the channel carrier mobility μ. Novel channel materials such as germanium and III-V semiconductors provide potential solution for mobility enhancement by replacing conventional silicon channel. Table 1.2 lists the properties of common semiconductor materials.

Table 1.2 Properties of common semiconductor materials (Si, Ge, GaAs, InAs, and InSb). $\mu_{electron}$ and μ_{hole} represent electron mobility and hole mobility respectively.

	Si	Ge	GaAs	InAs	InSb
$\mu_{electron}$ (cm^2/Vs)	1400	3900	8000	33000	77000
μ_{hole} (cm^2/Vs)	470	1600	340	460	1000
Bandgap (eV)	1.12	0.66	1.42	0.36	0.17
Melting point (K)	1685	1231	1510	1215	798

From Table 1.2, it is noted that germanium is the only material that offers mobility enhancement for both electron and hole with appropriate bandgap and melting points compared to other semiconductor materials, making it an attractive channel material for both NMOS and PMOS devices application. However, although the first MOSFET and IC were fabricated on Ge half century ago [1.8], the poor properties of germanium oxides and lack of good quality gate dielectric greatly hindered the development of Ge MOS device. Until recent years, Ge MOS devices with various high-k gate dielectrics were reported with the progress in high-k deposition and surface passivation techniques [1.9]-[1.12]. Ge pMOSFET with an EOT of 6-10 Å has also been demonstrated [1.13].

1.4 Schottky barrier source/drain MOSFET

1.4.1 Motivation

The idea of completely replacing doped source/drain with metal was first proposed by Nishi in 1966 in a Japanese patent which was issued four years later [1.14]. The first paper on the topic, however, was published in 1968 by Lepselter and Sze [1.15], focusing on a PMOS bulk device employing PtSi for the source/drain regions. Although a variety of Schottky barrier MOS devices were studied in the 1980s [1.16]-[1.20], the poor performance due to device architecture and process technology issues, hindered the progress of Schottky barrier MOSFET until the advantages of Schottky barrier MOSFET for device scaling were realized by Tucker [1.21] and Snyder [1.22] in 1994. In recent years, Schottky barrier MOSFET have received tremendous attention due to its numerous

benefits in making CMOS technology scalable to sub-10-nm gate length dimensions [1.23], which will be briefly introduced as following.

Table 1.3 Introduction of roadmap challenges addressed by Schottky barrier MOSFET (SBMOS). Most of the categories have multiple line items in the detailed roadmap tables. The box color for a given year and category above reflects the worst case, considering all of the roadmap line items within each category. (red) = manufacturable solution not known; (yellow) = manufacturable solutions are known; = manufacturable solutions exist and being optimized (after [1.24]).

Roadmap Challenge	Roadmap	2005	2007	2010	SBMOS
Technology Node (nm) [DRAM ½ Pitch]		80	65	45	
MPU Physical Gate Length (nm) [High-performance logic]		32	25	18	Help
Gate dielectric requirements	Front End				Help
Source-drain shallow implant requirements	Front End				Solve
Source-drain junction resistivity requirements	Front End				Solve
Source-drain lateral abruptness requirements	Front End				Solve
Gate requirements (e.g. metal gates)	Front End				Help
Channel doping requirements	Front End				Help
Sub-threshold leakage current requirements (High performance and Low operating power)	Process Integration				Help
Mobility/Transconductance requirements and technologies (e.g. strained silicon)	Process Integration				Help
MOS RF Device requirements (e.g. fT)	Proc. Int.				Help
Soft error rates	Design				Help

Figure 1.5 shows an XTEM (cross-sectional transmission electron microscope) image of a 27 nm channel length PtSi source/drain device with 19 Å gate oxide. It is obvious that in a Schottky barrier MOSFET, the metallic source/drain replace doped source/drain and form a Schottky barrier with the semiconductor substrate and channel region. Table 1.3 summarized the impact of Schottky barrier MOSFET in a variety of general ITRS roadmap categories, including “Process Integration, Devices and Structures”, “Front End Processes” and “Design.”. ITRS roadmap indicates predicts that there is no known solution to meet the requirements for the source/drain parasitic

resistance, shallow implant and lateral abruptness within the next two years. By replacing doped source/drain with metal silicide source/drain, challenge for the source/drain resistance can be easily solved since the metal silicide has low sheet resistance and the contact resistance is very low in metal-to-metal contacts. Without the difficulties in achieving shallow implant, the junction depth in metal silicide source/drain can be easily controlled from metal-Si reaction with atomically sharp interface (see Fig. 1.5). Since Schottky barrier source/drains require no impurity doping, the carrier concentration is no longer limited by the dopant solid solubility in the substrate material, which has been a bottleneck for some high mobility substrate material such as germanium and GaAs. On the other hand, the implantless Schottky barrier MOSFET process also eliminates the high-temperature 1000^{o} C spike or flash anneals to activate the source/drain dopants. Instead, the formation temperature of metallic source/drain is usually less than 600^{o} C, which enables the integration of other new critical materials into CMOS process flows, such as high-k gate dielectrics, metal gate, strained silicon and germanium. The properties of these new materials tend to degrade upon high-temperature anneal in doped source/drain technology, but are more stable when the process thermal budget is less than 600^{o} C [1.25]-[1.30]. With the elimination of implantation, the manufacturing process becomes simpler and cost is also reduced especially for short channel devices.

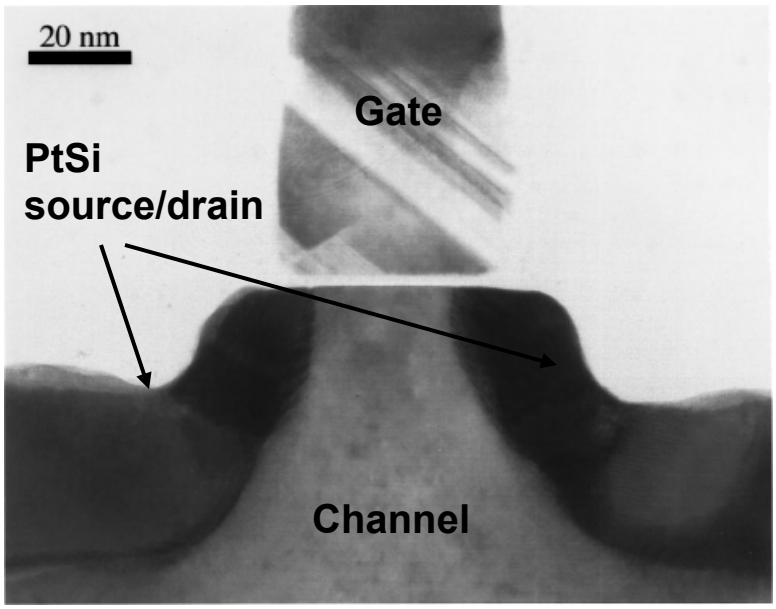

Figure 1.5 XTEM of a PtSi source/drain device with 27 nm channel length, 19 Å gate oxide, and n^+ poly gate (after [1.31]).

Another advantage of Schottky barrier MOS device is the latchup immunity. In the1980s, Sugino and Swirhun first realized that Schottky barrier MOSFET can naturally eliminate parasitic bipolar gain [1.19] [1.32]-[1.34], due to the reduction in theoretical emitter efficiency at the source by eight orders of magnitude from 10^4 for a conventional MOS device to 10^{-4} for a Schottky barrier MOS device. Therefore a Schottky barrier MOS device is inherently radiation tolerant. Consequently, circuits manufactured with Schottky barrier MOSFET technology will benefit from unconditional latchup immunity and substantially reduced soft error rates, thereby improving field level product reliability for both memory and logic applications, especially as device dimensions scale into the sub-50 nm regime [1.35].

1.4.2 Operation principles

The operation principles are fundamentally different between Schottky barrier source/drain MOSFET and doped source/drain MOSFET although technically these two kinds of devices have many similarities in the fabrication process. The main difference is the nature of the junction between the source/drain regions to the semiconductor substrate: the junction is a metal/semiconductor Schottky diode in Schottky barrier MOSFET, while it is a PN junction in doped source/drain MOSFET.

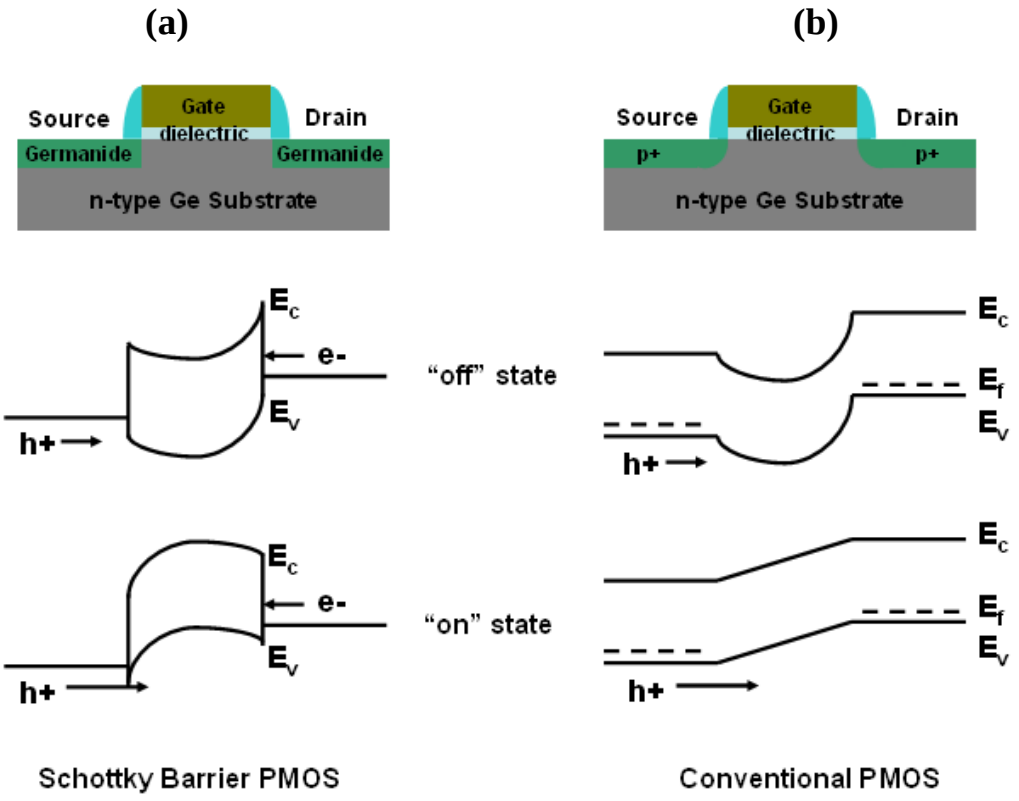

Figure 1.6 Band diagrams of (a) Schottky barrier PMOS device and (b) conventional impurity-doped source/drain MOS device.

Band diagrams of germanide Schottky barrier source/drain p-MOSFET and conventional impurity-doped source/drain Ge p-MOSFET are shown in Figure 1.6. In the Schottky barrier PMOS device in Fig. 1.6 (a), the Fermi level of the source and drain

germanide are attached to the Ge band gap close to the valence band in the "off" and "on" state respectively. The band diagrams for Schottky barrier PMOS and conventional MOS are quite similar except at the source and drain region, where the metal germanide Fermi level is replaced by the germanium bands in conventional PMOS, and the Schottky barrier PMOS bands have a built in Schottky barrier at the source and drain interface with the channel. In the off-state, the built-in Schottky barrier and substrate doping combine to limit electron and hole thermal emission into the channel. Compared to a Schottky barrier MOS device, a conventional MOS device requires a much higher channel doping concentration to achieve the same effective barrier to thermal emission in the off-state. Therefore to achieve a given off-state leakage current, channel doping in Schottky barrier MOSFET can be reduced compared to conventional MOS. As the gate voltage become more negative and the Schottky barrier MOS device is turned on, a gate induce electric field renders the source barrier virtually transparent and carriers are injected into the channel region. The net field emission current through the source Schottky barrier is exponentially sensitive to the electric field intensity at the source.

The band diagrams for a Schottky barrier NMOS device are the mirror image of those of PMOS as shown in Fig. 1.6. Similar discussion on device operation principles can also be applied.

1.4.3 Literature review

During the past ten years, the development of Schottky barrier MOSFET technology has advanced significantly in the aspects of device architectures, Schottky barrier height engineering and integration of new silicide materials such as $ErSi_x$ and $YbSi_x$ into device-fabrication process flows [1.36]-[1.38]. Table 1.4 summarized the

Schottky barrier NMOS and PMOS in the literature with gate length less than 250 nm. As one can see, high-performance Schottky barrier NMOS using thin dopant-segregation junctions and PMOS with a PtSi source/drain have been demonstrated. However, the on-current of these devices does not yet meet the ITRS requirements. Naturally, integration of Schottky barrier source/drain with other unconventional approaches (see Eq. 1.2) needs to be considered for further enhancement of the device on-current.

Among these unconventional approaches, Schottky barrier MOSFET fabricated on high mobility channel materials has received more and more attentions since past a few years. Germanium is one of the most promising channel materials as it offers mobility enhancement for both electron and hole with appropriate bandgap and melting points as shown previously. However, on the road to Schottky source/drain transistors, the metal Fermi level pinning is always a big challenge in work function and Schottky barrier tuning, especially at metal/germanium interface. This is the reason why low Schottky barrier is difficult to achieve, and extremely low work function metals such as Yb, Er have to be used for NMOS. A simulation work shows that for typical Schottky source and drain transistor, it is the carrier tunneling through the metal-semiconductor barrier height that limits the on-current. Thus only a negative metal-semiconductor barrier height could deliver the on-current of a ballistic MOSFET [1.40]. However, this simulation ignored the Schottky barrier lowering, phonon- and defect-assisted tunneling, band structure effects, etc, which could increase the transmission of the barrier. Recently, simulation studies suggest a finite positive barrier of 0.06-0.1 eV is needed for Schottky barrier PMOS and NMOS to make Schottky barrier CMOS technology speed performance competitive with doped source/drain technology [1.41] [1.42].

Table 1.4 Summary of sub-250-nm-gate length Schottky barrier NMOS and PMOS literature. The column labeled "Technology" has a comma-separated list for each row with the format "Type, device structure, source/drain silicide type, source/drain engineering type". (N=NMOS, P=PMOS; B= bulk, S= SOI, F= FinFET; 1= standard, 2= interfacial layer) [1.23].

#	Year	Technology	L_g [nm]	Gate type	*EOT* [Å]	V_{ds} [V]	V_{gs} [V]	I_{on} [μA/μm]	I_{off} [nA/μm]	I_{on}/I_{off}	Swing [mV/dec]	g_m [mS/mm]
1	1999	N,B,ErSi,1	35	Au/Cr	35	2.0	2.0	45	7500	6	-	20
2	2004	N,B,CoSi,1	65	-	60	1.5	3.0	350	2000	175	320	-
3	1999	N,S,ErSi,1	25	Au/Cr	35	2.0	2.0	75	$3.75x10^4$	2	-	9.5
4	2000	N,S,ErSi,1	15	N^+	40	1.5	1.2	190	19	10^4	150	-
5	2004	N,S,ErSi,1	50	N^+	50	1.0	3.0	120	10	$1.2x10^4$	-	-
6	2004	N,S,ErSi,1	25	Au/Cr	35	1.5	2.0	11	2000	6	-	-
7	2004	N,S,CoSi,1	65	-	60	1.5	3.0	25	70	357	1500	-
8	2005	N,S,CoSi,2	50	-	25	2.0	2.0	1670	100	$1.7x10^4$	-	-
9	1997	P,B,TiGeSi,1	250	Al	70	-2.0	-2.0	350	-	-	70	210
10	1997	P,B,PtGeSi,1	250	Si/Al	70	-2.0	-2.0	250	-	-	78	145
11	1999	P,B,PtSi,1	27	P^+	19	-1.2	-1.2	350	$1.0x10^4$	35	-	-
12	1999	P,B,PtSi,1	40	P^+	19	-1.2	-1.2	350	$1.5x10^4$	23	-	-
13	2002	P,B,PtGeSi,1	50	N^+	20	-1.5	-1.5	339	$1.0x10^4$	34	-	285
14	2004	P,B,PtSi,1	25	N^+	20	-1.1	-2.6	314	168	1869	117	500
15	2005	P,B,PtSi,1	25	N^+	18	-1.1	-1.8	460	168	2700	117	500
16	2005	P,B,PtSi,1	25	N^+	18	-1.1	-1.8	629	6149	102	-	558
17	2005	P,B,PtSi,1	60	N^+	18	-1.2	-1.7	311	12	$2.6x10^4$	96	400
18	2005	P,B,PtSi,1	80	N^+	18	-1.4	-1.7	300	6	$5.0x10^4$	91	417
19	2004	P,F,NiSi,2	25	P^+	40	-1.0	-2.0	250	$2.5x10^{-4}$	$1.0x10^9$	83	-
20	1999	P,S,PtSi,1	35	Au/Cr	35	-1.2	-1.2	70	167	420	-	216
21	1999	P,S,PtSi,1	56	Au/Cr	35	-1.2	-1.2	60	20	3000	-	220
22	2000	P,S,PtSi,1	38	Au/Cr	35	-1.5	-1.5	168	457	368	-	175
23	2000	P,S,PtSi,1	25	Au/Cr	35	-1.5	-1.5	293	8879	33	-	431
24	2000	P,S,PtSi,1	20	N^+	40	-1.5	-1.2	270	1	$5.0 x10^4$	100	-
25	2004	P,S,PtSi,1	25	Au/Cr	35	-1.5	-2.0	16	30	533	-	-

Heine, in 1965, pointed out that any intrinsic electron states which may be present on a free semiconductor surface will be replaced by metal-induced gap states (MIGS) when a metal is deposited on that surface [1.43] [1.44]. Besides MIGS, for a surface which is imperfect, defects such as steps or vacancies may lead to additional localized states. The energy levels associated with these defects may lie in the band gap of the semiconductor. Both of them may present at metal-semiconductor interface in densities

sufficient to cause strong pinning of the metal Fermi level.

Table 1.5 summarized measured barrier height values of the metal germanide/Ge contacts and pure metal/Ge contacts in the literature. The dependence of the barrier height on the metal work function is reflected by the equation

$$\phi_b = S \cdot \phi_m + C \tag{1.6}$$

where

S : slope parameter

ϕ_b : the barrier height of the metal/Ge contacts

ϕ_m : the metal work function

C : a constant

The value of S is a direct reflection of interface states density D_s given by

$$S = \frac{1}{1 + (q^2 D_s \sigma)/(\varepsilon \varepsilon_0)} \tag{1.7}$$

where

q : the electronic charge

σ : the thickness of interfacial layer

ε : the absolute permittivity of interfacial layer

ε_0 : the permittivity of free space

In an ideal metal/semiconductor system, according to the Schottky-Mott theory, Schottky barrier height can be controlled by the metal work function. However, the low values of S in Table 1.5 indicate a high density of interface states at the metal/Ge interface and the Fermi level is pinned at between 0.54 and 0.61 eV below the conduction-band edge, independent of the contacting metallization [1.45].

The lowest values of ϕ_{bh} and ϕ_{be} in Schottky source/drain Si MOSFET technology are achieved both ~ 0.27 eV by using PtSi [1.23] [1.37] and $YbSi_{2-x}$ [1.46] for PMOS and NMOS device respectively. The strong Fermi level pinning near valence band of germanium in metal/Ge contacts makes it much easier to achieve lower ϕ_{bh}（$\phi_{bh} < 0.1$ eV）compared to in metal/Si case, implying Schottky source/drain Ge PMOS device is promising to be realized with improved performance than Schottky source/drain Si PMOS device. However, the Fermi level pinning at metal/Ge interface also provides high ϕ_{be} for NMOS device, which is a great challenge to the realization of NMOS device.

Various attempts have been carried out to alleviate the Fermi level pinning phenomenon. M. Tao [1.47]-[1.49] and D. Udeshi [1.50] demonstrated that, by terminating dangling bonds and relaxing strained bonds on the silicon (001) surface with a monolayer of selenium, low Schottky barriers can be obtained. Dan Grupp *et al.* [1.51] has proposed x-junction structure by inserting thin insulator between metal and semiconductor to reduce pinning while still maintaining high conductance. Another way to modify barrier height is to introduce a thin, highly doped interfacial region at metal/semiconductor interface by shallow ion implantation, epitaxial growth or diffusion form a doped layer [1.45]. However, the low ϕ_{be} in metal/Ge contacts has not yet been reported so far in the literature.

Table 1.5 Summary of barrier heights of various metal germanide/Ge contacts and pure metal/Ge contacts in the literature. ϕ_m is the metal work function, ϕ_{be} is barrier height for electron, ϕ_{bh} is barrier height for hole, and S is slope parameter.

Metal	ϕ_m (eV)	Contact	ϕ_{be} (eV)	ϕ_{bh} (eV)	S	Ref.
Pt	5.65	Pt/Ge	0.62	0.04	0.02	[1.39]
		Pt_2Ge/Ge	0.61	0.05		
		PtGe/Ge	0.62	0.04		
		$PtGe_2$/Ge	0.62	0.04		
Ni	5.15	Ni/Ge	0.57	0.09		
		Ni_2Ge/Ge	0.58	0.08		
		NiGe/Ge	0.59	0.07		
Pd	5.12	Pd/Ge	0.61	0.05		
		Pd_2Ge/Ge	0.61	0.05		
		PdGe/Ge	0.61	0.05		
Er	3.12	Er/Ge	0.54	0.12		
		$ErGe_2$/Ge	0.52	0.14		
Ni	5.15	Ni/Ge	0.44	0.22	0.40	[1.53]
Pb	4.20	Pb/Ge	0.38	0.28		
Au	4.70	Au/Ge	0.54	0.12		
Pd	5.12	Pd/Ge	—	—	0.16	[1.55]
Ni	5.15	Ni/Ge	—	—		
Ag	4.26	Ag/Ge	0.54	0.12	0.11	[1.56]
		Ge/Ag	0.48	0.18		
Ni	5.15	Ni/Ge	0.49	0.17		
		Ge/Ni	0.49	0.17		

1.5 Thesis organization

As discussed in Section 1.2 to Section 1.4, high-k gate dielectric, metal gate, high mobility germanium channel and Schottky barrier source/drain structure are all attractive elements for future CMOS technology in different aspects. Therefore the main objective of this project is to explore the feasibility of integration of germanide Schottky

source/drain MOSFET with high-k gate dielectric (HfO_2) and metal gate (TaN) for sub-tenth nm technology.

Following this introduction chapter, Chapter 2 describes the typical fabrication process of a metal-germanide Schottky source/drain MOSFET integrated with HfO_2 high-k dielectric and TaN metal gate, as well as that of a metal-germanide/Ge Schottky diode in this project. Some techniques for characterization of physical and electrical properties of MOSFET are also briefly introduced at the later part of this chapter.

Chapter 3 and 4 focus on the studies of material and electrical properties of several novel germanides, including Ni-, Pt-, Er- and Yb- germanides, and the successful demonstration of metal-germanide Schottky source/drain n- and p-MOSFETs. A simulation work on the impact of spacer thickness on MOSFET drive current and a robust self-aligned Pt-germanide process are also shown. Chapter 5 describes the second part of this PhD project which focuses on demonstration of Ge pMOSFET with Pt-germanide Schottky source/drain formed by laser annealing.

Finally, Chapter 6 summarizes the results drawn from this project and suggests recommendations for the future work.

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Chapter 2

Device fabrication and characterization

For decades, conventional technology has been developed on Si-based CMOS process flow where SiO_2 was successfully integrated due to the high-quality Si-SiO_2 interface, thermodynamic and electrical stability as well as superior electrical isolation properties. However, the thermodynamically unstable and water-soluble properties of Ge oxides (GeO and GeO_2) [2.1] and the low melting temperature of Ge (937^{o} C) present significant challenges in the process integration and greatly hinder the processing and application of Ge MOS devices, in particular Schottky source/drain MOSFETs.

The use of Schottky contact in electronic devices can be traced back by almost four decennia when Pt [2.2], Cu [2.2], Mo [2.2] and W [2.3] silicides were used for manufacturing planar Schottky diodes with enhanced rectifying characteristics. Today, metal silicides have become an inseparable part of an electronic device because they meet the basic requirements: low specific resistivity, low contact resistance to both type of Si, high thermal stability, good processibility, and excellent process compatibility with standard Si technology [2.4] [2.5]. Since Nishi first proposed the idea of completely replacing doped source/drain with metal in 1966 [2.6], silicide source/drain Schottky barrier MOSFET structure has draw more and more attention throughout decades as one solution for the source/drain shallow implant, junction resistivity and lateral abruptness requirements forecasted by ITRS [2.7]-[2.10]. However, the development of germanide Schottky source/drain MOSFET is relatively lagged, partly due to the incompatibility

with Si technology and until 2005, Ni [2.11] and Pt [2.12] germanide Schottky source/drain Ge p-MOSFETs were first demonstrated with the process-induced hole between gate and source/drain for isolation by lateral encroachment of the gate electrode [2.11] and back gate structure [2.12], respectively.

In this chapter, fabrication of a typical top-gate self-aligned metal-germanide Schottky source/drain MOSFET integrated with HfO_2 high-k dielectric and TaN metal gate will be shown first, followed by descriptions of some critical process steps in detail. Some techniques for characterization of physical and electrical properties of MOSFET will be briefly introduced at the final part of this chapter.

2.1 Device fabrication process

2.1.1 Fabrication process for metal-germanide Schottky source/drain Ge MOSFETs integrated with TaN/HfO_2 gate stack

Our MOSFETs fabrication is a self-aligned single-mask process, patterned in ring-shaped patterns, as shown in Figure 2.1. The fabrication of ring-shaped MOSFETs is usually on one mask level so it provides a rapid and simple way for MOSFETs fabrication, while most electrical characteristics of MOSFETs, such as the output and transfer characteristics, junction and gate properties, mobilities, and so on, can be easily measured, making it a preferred choice for novel material studies. Additionally, in principle, material properties of source/drain regions and impact of germanide source/drain on device performances should be the same regardless the channel length of a device is in micrometer scale or nanometer scale. The gate length is 5 ~ 20 μm and the

width is 400 μm in our experiments, with an additional square area of 100 × 100 μm^2 for probing. The sketch of a single mask ring-shaped MOSFET from top view is shown in Figure 2.1.

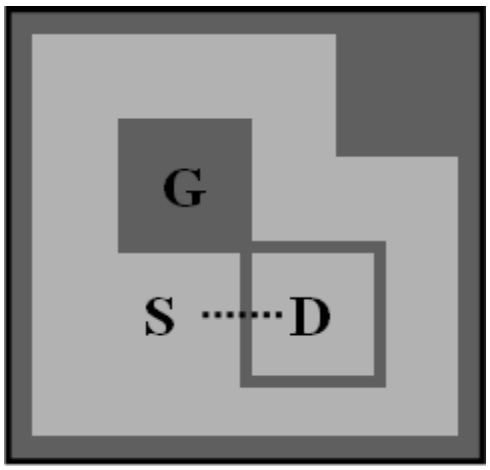


Figure 2.1 A sketch of single mask ring-shaped MOSFET where G, S and D presenting gate, source and drain regions, respectively.

The typical Schottky source/drain MOSFET fabrication process used in this project includes following steps:

1) Substrate pre-gate cleaning (see Fig. 2.2 (a)): The standard Si substrate cleaning process is known to consist of SC-1 (NH_4OH : H_2O_2 : H_2O=1:1:5), SPM (sulfuric-peroxide mixture with H_2SO_4 : H_2O_2 = 4:1) and DHF (diluted HF with HF : H_2O=1:100) cleaning, rinsed by de-ionize (DI) water. However, because germanium can be rapidly etched by both SC-1 and SPM, for Ge substrate pre-gate cleaning, only DHF cleaning (5 min) and DI water rinsing were adopted, with N_2 gun blowing to dry.

2) Substrate surface treatment before high-k gate dielectric deposition (see Fig. 2.2 (b)): Besides the hygroscopic and water-soluble properties of Ge oxides, distorted C-V characteristics from Ge MOS capacitor with GeO_2 as the gate dielectric also indicate the high density of interface states and interface traps [2.13] [2.14]. Degradation of device performance has been reported due to the presence of Ge oxides which usually form during high-k dielectric deposition and post process [2.15]-[2.18]. As a result, Ge substrate surface treatment before high-k gate dielectric deposition becomes a critical step to passivate interface states and traps and suppress Ge oxidation. Among various attempts on passivation technique exploration, plasma-PH_3 and thin AlN turned out to be the most promising for both Ge p- & n-MOS devices [2.19] [2.20]. In this project, plasma-PH_3 was generally used due to the in-situ process with high-k gate dielectric deposition in MOCVD (metal organic chemical vapor deposition). This process was carried out at 430^{o} C for 60 sec, with a flow of mixed gas PH_3:N_2 = 1:100 of 300 sccm, working pressure of 323 mTorr and RF (radio frequency) power of 200 W.

3) High-k gate dielectric deposition and PDA (Post-Deposition Anneal) (see Fig. 2.2 (c)): The high-k gate dielectric used for this project is HfO_2 due to its high k value (~25) and acceptable conduction band offset. After the surface plasma-PH_3 treatment, the deposition of HfO_2 is carried out in MOCVD by reaction between $Hf(OC(CH_3)_3)_4$ and O_2. The PDA procedure is in-situ performed in N_2 ambient with working pressure of 200 Torr at 400^{o} C for 1 min.

4) Metal gate electrode deposition (see Fig. 2.2 (d)): the metal gate electrode of TaN is deposited at a rate of 9 nm/min by reactive sputtering of Ta in N_2 and Ar

ambient (N_2: 5 sccm, Ar: 25 sccm) at a working pressure of 3 mTorr with DC and RF power of 450 W and 12 W, respectively.

5) Photolithography process (see Fig. 2.2 (e)): the process in this project used only one mask to pattern gate and source/drain region at the same time. During lithography process, a layer of PR (photo-resist) is spun-on the wafer surface with a highest spin rate at 5000 r/sec. After soft baked at 95^{o} C for one min, wafer was loaded into mask aligner where UV light exposure with the mask shown in Fig. 2.1 was carried out, followed by post exposure baking at 95^{o} C for one min. Finally after a develop procedure and hard baking (115^{o} C for 10 min), the wafer is patterned with gate region covered with PR and source/drain region open.

6) Gate RIE (Reactive Ion Etch) and PR removal (see Fig. 2.2 (f)): the gate stack is defined and patterned by Cl_2 plasma dry etching procedure in Lam Etcher. The etching removes all TaN in source/drain region and stops on HfO_2 dielectric layer with Ge substrate untouched. The un-crystallized HfO_2 layer can be removed by DHF in later step. The residual PR is removed by a combustion procedure in Asher at 170^{o} C for 10 min with O_2 gas flow of 10 sccm, RF power of 250 W and working pressure of 300 mTorr.

7) Spacer material deposition and spacer etching (see Fig. 2.2 (g)): Spacer formation is one of the most important steps in Schottky source/drain MOSFET fabrication, which makes metal gate and metal source/drain electrically isolated. A thin sidewall spacer helps minimize source/drain-to-gate underlap so that the Schottky source/drain to the channel region is in close proximity to the gate electrode and the source/drain junction parasitic resistance induced by underlap can be reduced.

The optimized thickness of the spacer should be about 10 nm [2.21]. In the literature study, the thin sidewall spacer is mostly formed by RTO (rapid thermal oxidation) of poly-Si gate electrode with thickness of 10 – 15 nm [2.22] [2.23] [2.25] [2.26] or Si oxide/nitride by LPCVD (Low-pressure chemical vapor deposition) [2.27] followed by an anisotropic sidewall spacer etch. However, neither of these two approaches is applicable in this project due to the TaN metal gate used and the thermal stability consideration of HfO_2/Ge. Instead, Si nitride by PECVD (Plasma Enhanced Chemical Vapor Deposition) is mostly used as spacer material in this project [2.28] [2.29] considering its efficiency and simpler process. Considering the DHF cleaning before the deposition of source/drain metal, during which PECVD Si nitride will be isotropically etched at a rate of ~ 15 nm/min, a relatively thick Si nitride (~30 nm) is deposited. The spacer etching is carried out first in Lam Etcher where 20~25 nm Si nitride is dry etched in Cl_2 plasma, followed by dipping into DHF to remove the residue 10~5 nm Si nitride (Fig. 2.2 (g) – I).

Besides the Si nitride, HfN sidewall hole and AlN_x/SiO_2 stacked spacer were also tried in experiments for this project. To form HfN sidewall hole, the gate electrode should be deposited a layer of HfN prior to TaN deposition. During source/drain pre-metal deposition cleaning, the HfN interlayer is laterally etched by DHF at a rate of ~30 nm /min and a hole is created in gate edge at HfN interlayer, which will act as spacer (shown in Figure 2.2 (g) – II). This approach simplifies the Schottky source/drain MOSFET fabrication further, and well-behaved silicide and germanide Schottky MOSFETs have been demonstrated in

this way [2.30] [2.31]. However, the difficulty in the control of lateral encroachment of HfN makes this process unpredictable. On the other hand, AlNx/SiO_2 stacked spacer shown in Fig. 2.2 (g) – III is formed by deposition of ~ 6 nm SiO_2 by e-beam evaporation and ~ 4 nm AlN by reactive sputtering in consequence, followed by anisotropic dry etching, where AlN protects spacer from being etched during DHF etch in the next step due to its low etching rate in DHF and SiO_2 plays a role of dry etching stop layer to prevent over etching of Ge substrate. This stacked spacer turned out to be successful and PtGe p-MOSFET was demonstrated in this way [2.32].

8) Source/drain pre-metal deposition cleaning and metal deposition (see Fig. 2.2 (h)): to remove Si nitride etch residue and native oxides in the source/drain region, wafer is dipped into DHF (HF: H_2O=1: 50) for 40 seconds. Metal is deposited by sputter or e-beam evaporator with the base pressure is kept around 5×10^{-7} mTorr.

9) Germanidation process (see Figure 2.2 (i)): metal germanides are formed by RTA (rapid thermal annealing) carried out in RTP (rapid thermal process) chamber in N_2 ambient at various temperature. In this project, laser annealing was also applied for germanidation process, and will be elaborated in Chapter 5.

10) Removal of unreacted metal (see Figure 2.2 (j)): the aim for this step is to selectively remove unreacted metal, especially metal on spacer that can cause electrical short between the gate and source/drain, while leaving formed germanide intact, known as selective etching. The most important factor is the high etching selectivity of the chemical solution, i.e., selectivity = etching rate of metal: etching rate of metal germanide. Due to the fast etching rate of germanium

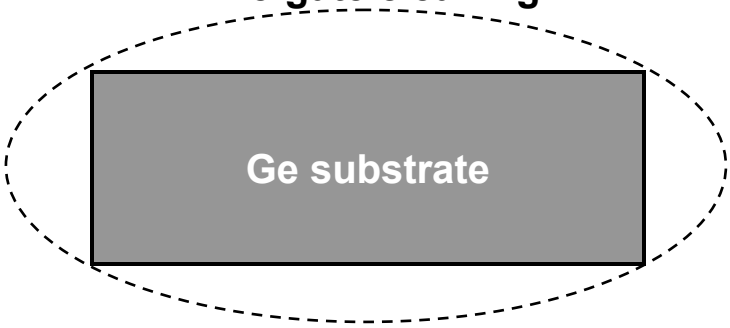
and germanide in SC-1 and SPM, such solutions widely used in Si technology however should be avoid in this project. It is found diluted HNO_3 (HNO_3: H_2O= 1: 20 by volume) has a high selectivity for metal such as Ni, Er, Yb to corresponding germanides with a metal etching rate of 10 ~ 12 nm/min. On the other hand, Pt is known to be the most difficult metal to etch and usually is etched by heated aqua regia (HCl: HNO_3 = 3: 1) [2.32]. However, during experiments in this project, the following relationship was found:

ER (etching rate) of Pt-germanide > ER of Pt > ER of Pt silicide

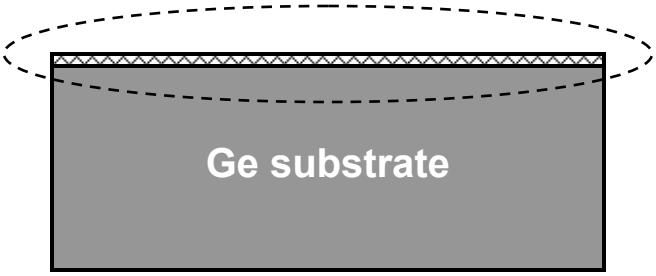
As a result, although aqua regia is widely used in Pt-silicide Schottky MOSFETs fabrication process [2.22] [2.23], it is not compatible for a Pt-germanide MOSFETs process. Instead, dry etching by Cl_2 is applied to remove Pt (deposited by e-beam evaporation) during which Pt-germanide and Pt are etched at a comparable rate. Since the thickness of Pt-germanide formed is double of the thickness of Pt deposited, source/drain region can still have remaining Pt-germanide after Pt dry etching. However, sputtered Pt film turns out to be more difficult to etch by RIE compared to evaporated Pt film, and can only be removed by wet chemical etching.

11) Backside ohmic contact (see Figure 2.2 (k)): as the last step, 100 nm Al is deposited by e-beam evaporator at the wafer backside to form ohmic contact at a deposition rate of 1 angstrom/sec with a base pressure of 5×10^{-7} mTorr.

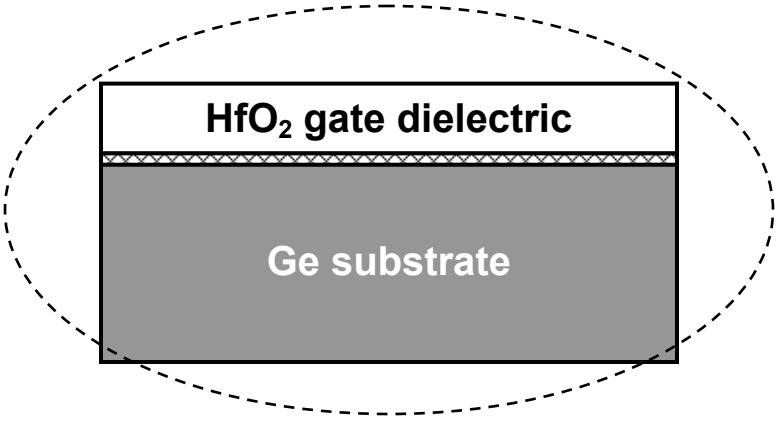
(a) **Pre-gate cleaning**



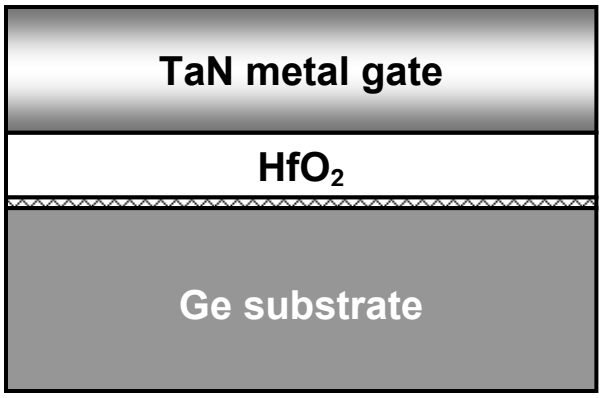
(b) **Surface treatment**



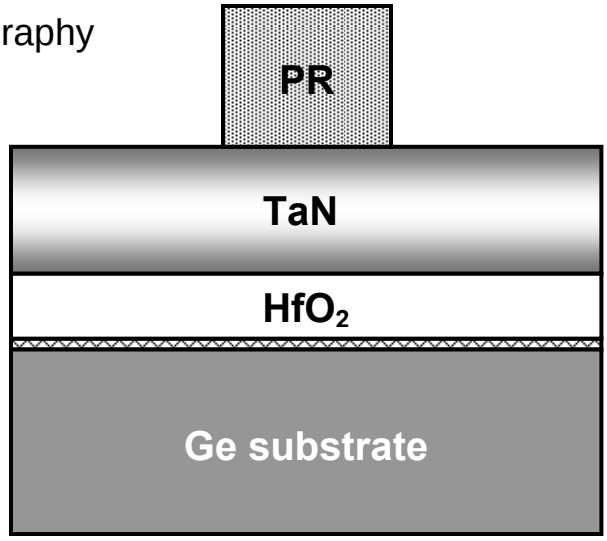
(c) **PDA**



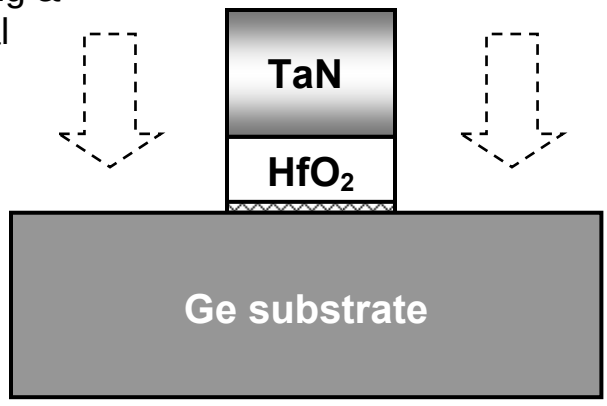
(d)
Gate electrode
deposition



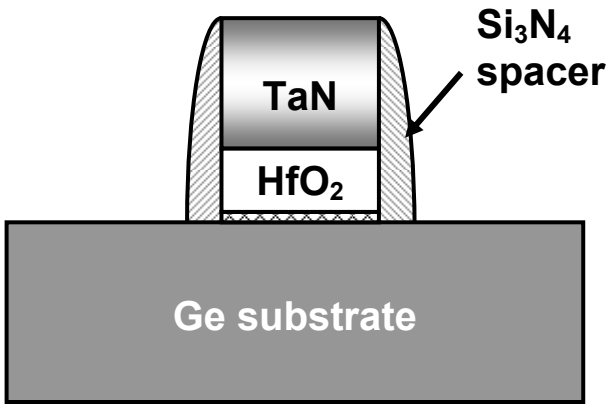
(e)
Photolithography



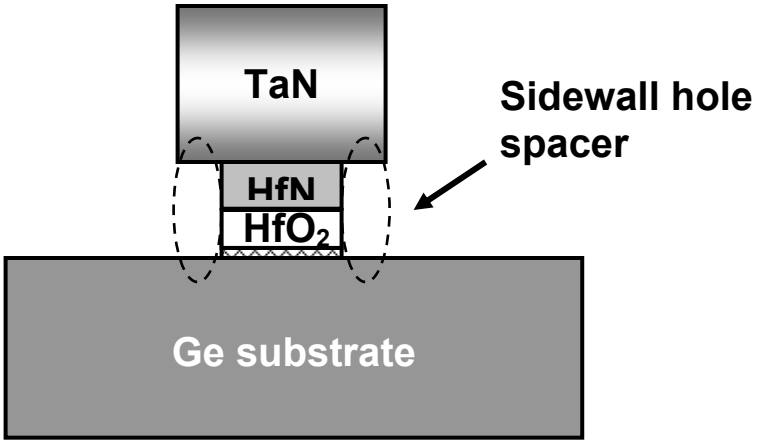
(f)
Gate etching &
PR removal



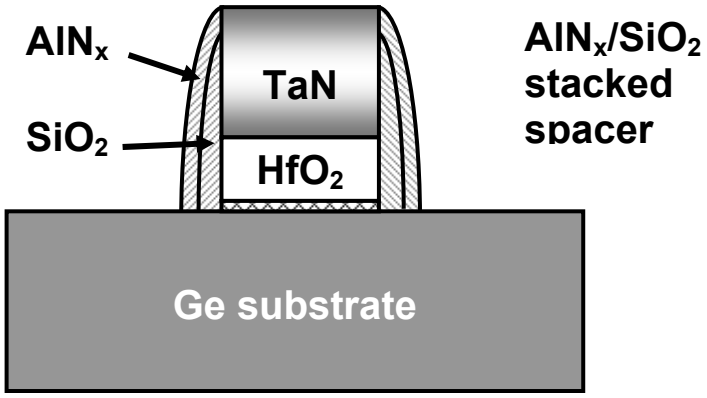
(g)
Spacer
formation



(g) – I

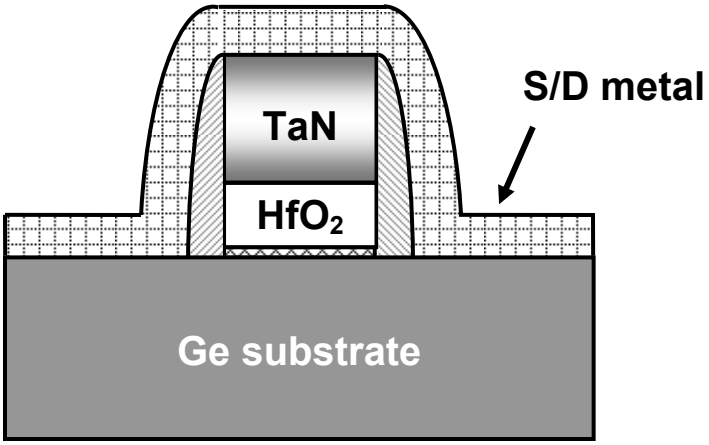


(g) – II

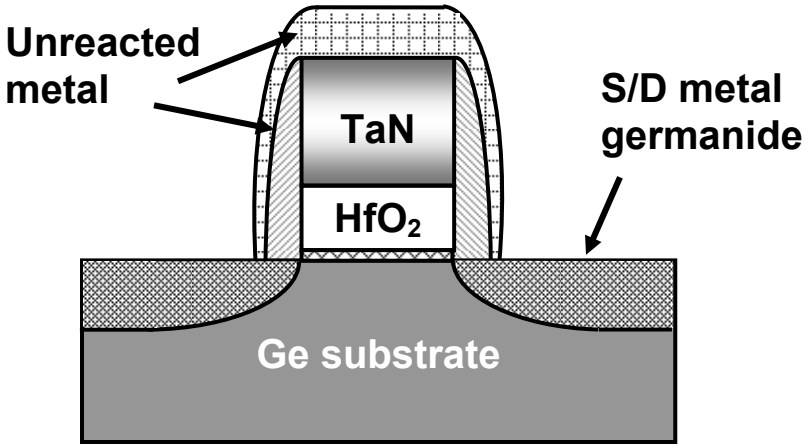


(g) – III

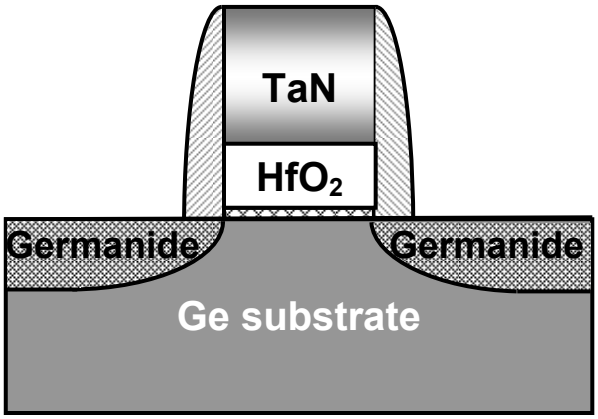
(h)
S/D metal
deposition



(i)
Germanidation



(j)
Selective etch



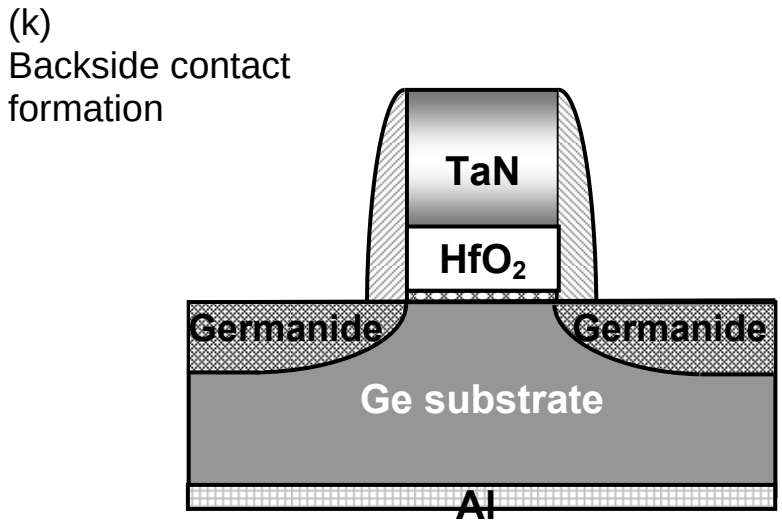


Figure 2.2 A typical fabrication process flow of a Schottky source/drain MOSFET in this project.

2.1.2 Fabrication process for metal germanide/Ge Schottky diodes

The fabrication of germanide/Ge Schottky diodes contains fewer steps compared to the fabrication of Schottky MOSFETs. It includes the following steps:

1) Substrate cleaning and field isolation material deposition (see Fig. 2.3 (a)): after dipped into DHF for 1 min to remove native oxides, Ge wafer is loaded into PECVD chamber and ~ 100 nm Si_3N_4 is deposited at 250^o C. The deposition rate of Si_3N_4 is kept at 1 nm/sec.

2) Photolithography (see Fig. 2.3 (b)): the same procedure as MOSFET photolithography which is elaborated earlier in this chapter is applied for diode fabrication using the same single mask.

3) Diode etching and PR removal (see Fig. 2.3 (c)): the diode pattern is etched by RIE. 80~90 nm Si_3N_4 is removed in Cl_2 plasma ambient and the remaining Si_3N_4

is removed by DHF at a etching rate of 15 nm/min. PR is removed in Asher at 170 ^{o}C for 10 minutes with O_2 gas flow of 10 sccm, RF power of 250 W and working pressure of 300 mTorr.

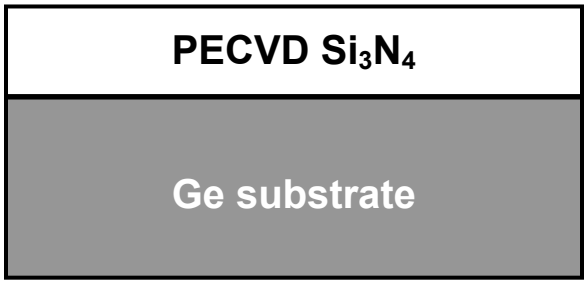
4) Pre-metal-deposition-cleaning and metal deposition (see Fig. 2.3 (d))

5) Germanidation and selective etch (see Fig. 2.3 (e))

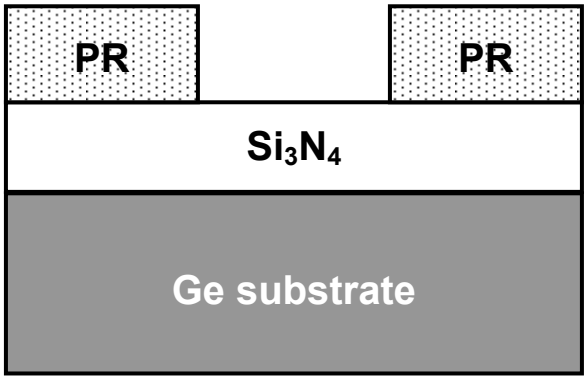
6) Backside ohmic contact (see Fig. 2.3 (f))

Steps 4 – 6 follow the same procedure as MOSFETs fabrication steps 8 – 11.

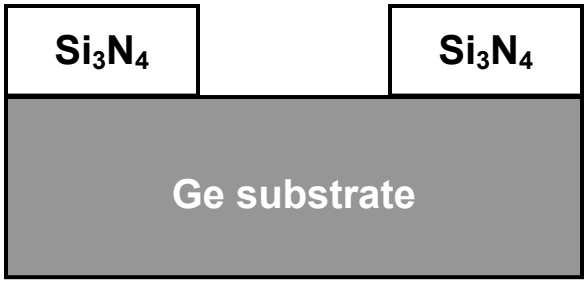
(a)



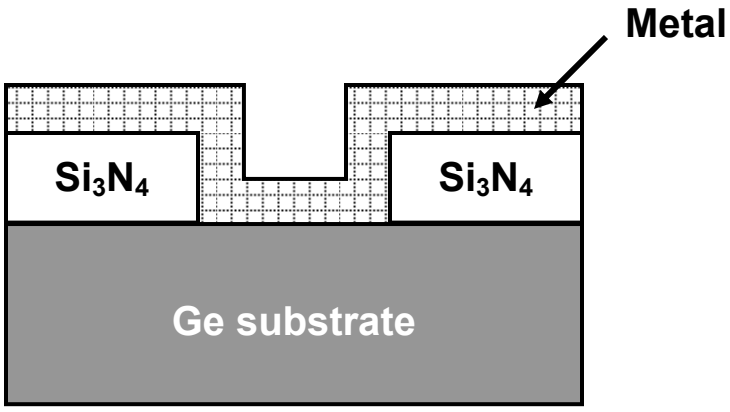
(b)



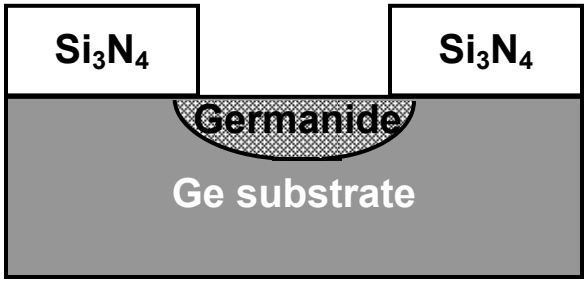
(c)


Si3N4
Si3N4
Ge substrate

(d)


Metal
Si3N4
Si3N4
Ge substrate

(e)


Si3N4
Si3N4
Germanide
Ge substrate

(f)

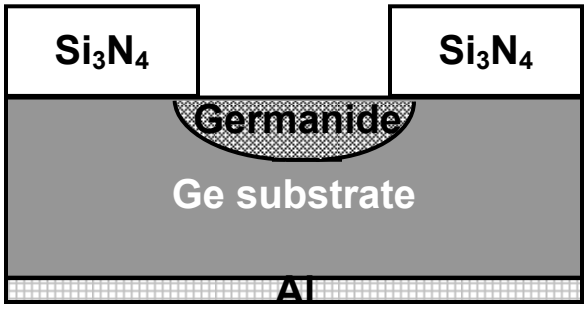


Figure 2.3 A typical fabrication process flow of a metal germanide/Ge Schottky diode in this project.

2.2 Device characterization

The physical and electrical properties of a device during process and after full fabrication are characterized by various techniques. This part will categorize and introduce briefly the techniques that are most frequently used in this project.

2.2.1 Chemical and physical properties

1) Spectroscopic ellipsometer

Ellipsometer is a true contactless, noninvasive technique measuring changes in the polarization state of light reflected from a surface. It is used predominantly to determine the thickness of thin films on highly absorbing substrates in industry. In this project, we are using a commercially available spectroscopic ellipsometer (SE800 from SENTECH Instruments GmbH), with a resolution of ~ 0.1 nm applicable to material that

is able to be penetrated by the light with wavelength roughly from 250 nm to 650 nm. A schematic sketch is shown in Figure 2.4. The physical thickness of dielectrics, such as HfO_2, SiO_2, Si_3N_4 etc, and thin metal film (thickness less than 30 nm) is measured by this technique.

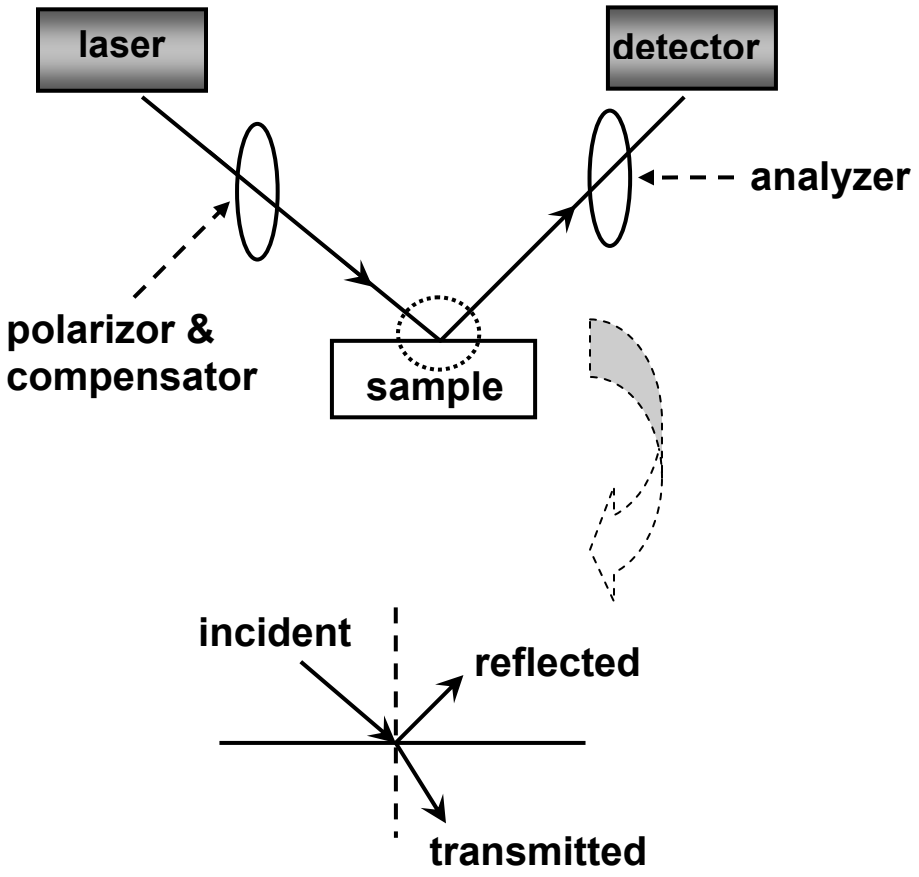


Figure 2.4 A schematic sketch of spectroscopic ellipsometer.

2) SEM (Scanning Electron Microscopy)

In SEM, an electron beam incident on the sample with electron energy of typically 10-30 KeV, produces a magnified image of the sample [2.34]. Compared to optical microscopes, SEM provides much larger magnifications and much higher depth of

field, making it widely used to view the surface of the device or to determine device dimensions. In this project SEM is mainly used for a direct evaluation of film morphology.

3) TEM (Transmission Electron Microscopy) & HRTEM (High resolution TEM)

In spite of the complicated sample preparation procedure, TEM provides the extremely high resolution; especially HRTEM gives structural information on the atomic size level and has become very important for interface analysis. In this project, TEM and HRTEM were used in studies of germanide film texture and properties of germanide/Ge and HfO_2 dielectric/Ge interfaces.

4) XRD (X-Ray Diffraction)

XRD is a nondestructive technique that requires little sample preparation and gives structural crystal information over entire semiconductor wafers. In this project, Bruker D8 GADDS X-ray diffraction is used for germanide crystallization study and phase identification.

5) XPS (X-Ray Photoelectron Spectroscopy)

XPS is primarily used for identifying chemical species at the sample surface (the emitted photoelectrons originate from the upper 0.5-5 nm of the samples), allowing all elements except hydrogen and helium to be detected. We are using a JEOL XPS (JPS-9010MX) in this project.

6) SIMS (Secondary Ion Mass Spectrometry)

SIMS is one of the most powerful and versatile analytical techniques for semiconductor characterization. It is element specific and is capable of detecting all elements. Dynamic SIMS is used for a depth profile which is obtained by record of the

intensity of one peak for one particular mass as a function of sputter time when the sample is sputtered at a higher sputter rate (~ 10 μm per hour).

2.2.2 Electrical properties

1) Sheet resistivity measurement

The four-point probe technique is the most common method for resistivity measurement which was originally proposed by Wenner in 1916 [2.34] and adopted for semiconductor wafer resistivity measurement by Valdes in 1954 [2.35]. The four probes are generally collinear, i.e., arranged in-line with equal probe spacing, as illustrated in Figure 2.5, where two probes carry current and the other two carry voltage. After considering the correction factors, the sheet resistivity can be derived from

$$\rho = \frac{\pi \cdot t}{\ln(2)} \cdot \frac{V}{I} = 4.352 \cdot t \cdot \frac{V}{I} \tag{2.1}$$

where ρ is the sheet resistivity (μΩ•cm), t is the film thickness, V and I are voltage applied between two probes and current flowing through the other probes, respectively.

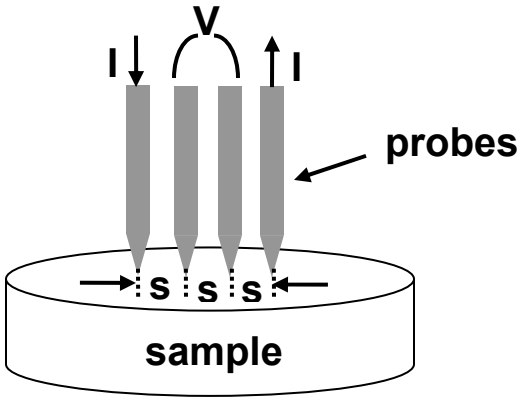


Figure 2.5, A typical collinear four-point probe set up.

However, resistivity measured by this method is geometry-dependent and quite sensitive to boundary conditions, especially in the case of small size samples with irregular area. Van der Pauw method has been demonstrated to be more effective in resistivity measurement for this case [2.36], where four probes contact with sample at arbitrary places along the circumference as shown in Figure 2.6. The sheet resistivity is determined as [2.37]

$$\rho = \frac{\pi}{\ln 2} \cdot \frac{R_1 + R_2}{2} \cdot f(\frac{R_1}{R_2}) \cdot t \tag{2.2}$$

where $f(\frac{R_1}{R_2})$ is Van der Pauw correction factor as a function of the ratio of $\frac{R_1}{R_2}$ ($R_1 > R_2$) with $R_1 = \frac{V_{CD}}{I_{AB}}$ and $R_2 = \frac{V_{DA}}{I_{BC}}$. In our project, the size of germanide samples is within 5×5 mm^2 – 8×8 mm^2 with irregular shape, so the resistivtiy and sheet resistance of germanide films are measured using this method.

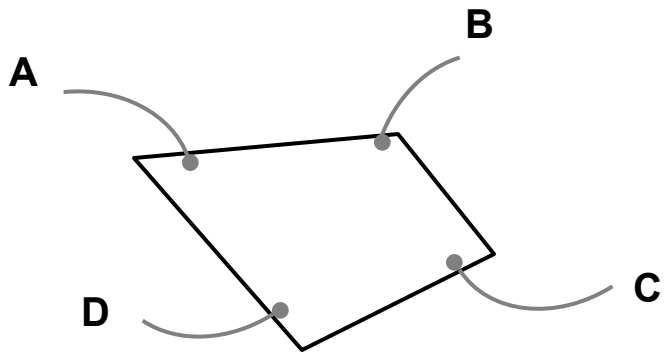


Figure 2.6 Sample of irregular shape with four contacts at arbitrary places along the circumference.

2) Metal/Ge Schottky barrier height measurement

The Schottky barrier height is one of the key parameters in a metal/semiconductor contact. Numerous techniques have been developed to extract barrier heights accurately such as the current-voltage ($I-V$), current-temperature ($I-T$), capacitance-voltage ($C-V$) and photocurrent (PC) techniques. In this project, the Schottky barrier heights of germanide/Ge contacts were extracted by $I-V$ and $I-T$ method, which will be briefly introduced below.

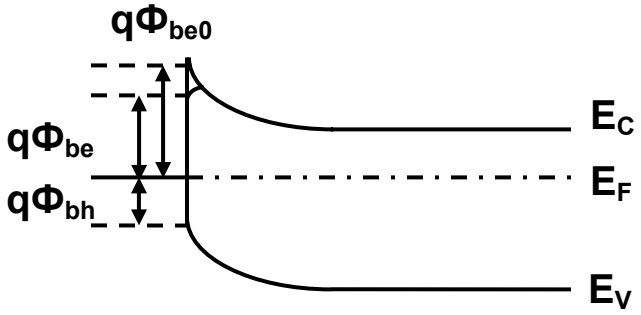


Figure 2.7 Schottky barrier energy band diagram on an n-type substrate.

The band diagram of a Schottky barrier diode on an n-type substrate is shown in Figure 2.7, where E_C, E_V and E_F represent the conduction band, valence band and semiconductor Fermi level, respectively. Due to image force barrier lowering and other factors, the actual electron barrier height $q\phi_{be}$ is less than the ideal barrier height $q\phi_{be0}$. The thermionic current-voltage relationship of the Schottky barrier diode is given by [2.38]

$$I = I_s(\exp(\frac{qV}{nkT}) - 1) \tag{2.3}$$

or

$$I = I_s \exp(\frac{qV}{nkT})[1-\exp(\frac{-qV}{kT})] \tag{2.4}$$

where I_s is the saturation current given by

$$I_s = AA^*T^2 \exp(\frac{-q\phi_{be}}{kT}) \tag{2.5}$$

A is the diode area, A^* is the Richardson's constant, T is the measurement temperature, k is the Boltzmann constant, q is the electron charge, ϕ_{be} is the effective electron barrier height and n is the ideality factor. In ideal case, the value of n should be unity. But in real case n is larger than unity due to mostly unknown effects making the device nonideal such as the presence of a thick interfacial layer, the recombination of electrons and holes in the depletion region or the nonuniformity over entire Schottky diode. Recombination current is most important at low forward voltages and leads n approach 2.

The $I-V$ method is most commonly used in barrier height measurement, in which barrier height ϕ_b is calculated from the saturation current I_s. According to Eq. (2.4), the following equation can be derived:

$$f(V) = \frac{I}{(1-\exp(\frac{-qV}{kT}))} = I_s \exp(\frac{qV}{nkT}) \tag{2.6}$$

Further we can get

$$\log(f) = \log I_s + \frac{qV}{nkT} \tag{2.7}$$

So I_s can be determined by an extrapolation of the log(f) versus V curve to $V = 0$ while n can be determined from the slope. According to Eq. (2.5) the barrier height ϕ_{be} can be calculated from

$$\phi_{be} = \frac{kT}{q} \ln(\frac{AA^* T^2}{I_s}) \tag{2.8}$$

The $I-T$ method utilizes Richardson plot, i.e., a plot of $\ln(\frac{I}{T^2})$ versus $\frac{1}{T}$ at a constant forward bias voltage $V = V_0$. According to Eq. (2.3) and Eq. (2.5), for $V >> \frac{kT}{q}$

$$\ln(\frac{I}{T^2}) = \ln(AA^*) - \frac{q(\phi_{Be} - V/n)}{kT} \tag{2.9}$$

The Richardson plot has a slope of $-\frac{q(\phi_{be} - V/n)}{k}$ and an intercept $\ln(AA^*)$ on the vertical axis. So the barrier height is given by

$$\phi_{be} = \frac{V_0}{n} - \frac{k}{q} \cdot \frac{d[\ln(I/T^2)]}{d(1/T)} \tag{2.10}$$

where n is determined by the $I-V$ method.

Table 2.1 A comparison between Schottky barrier height measurements by $I-V$ and $I-T$ methods.

Method		Advantage	Disadvantage
$I-V$	**Fitting forward current**	**Widely used, simple**	○ **Uncertain** A^* ○ **Contact resistance**
	Fitting reverse current	**Less affected by contact resistance**	○ **Uncertain** A^* ○ **Image effect should be considered**
$I-T$		A^* **is not used**	○ **Assumption:** ϕ_B **is temperature independent.**

A comparison between Schottky barrier height measurements via the two methods is summarized in Table 2.1. The uncertain value of Richardson constant A^* that is frequently observed varying greatly with processing conditions is the main disadvantage for $I-V$ method. On the other hand, using $I-T$ method to determine barrier height does not involve A^* value, however, it is accurate based on the assumption that barrier height is temperature independent. Both of the two methods are used to analysis the germanide/Ge diodes in our project, and the results will be discussed in Chapter 3.

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Chapter 3

Metal germanide Schottky source/drain Ge channel p-MOSFETs integrated with TaN/HfO_2 gate stack

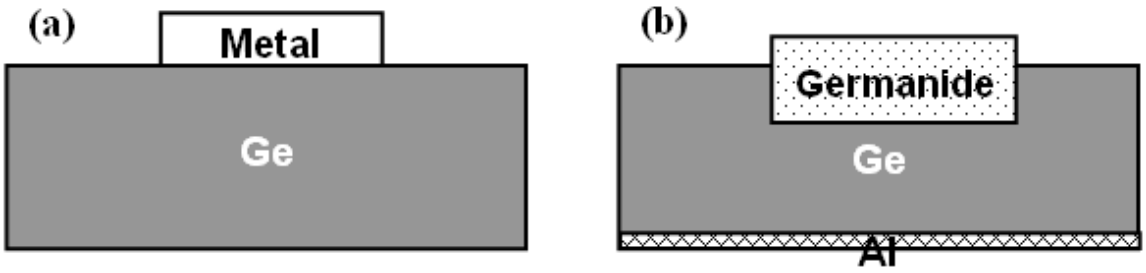
Germanium-channel MOSFETs have recently attracted tremendous attentions for future high performance CMOS devices due to its higher carrier mobility. Successful demonstration of high-k dielectric deposition on Ge substrate using surface passivation techniques [3.1]-[3.3] enhances the feasibility of Ge-MOSFETs. However, it is also pointed out that the limited thermal stability of Ge/high-k/metal gate stack and difficulties in achieving highly doped source/drain due to the poor activation and solid solubility limits of dopants may deteriorate the performance improvement of Ge MOSFET [3.4]-[3.6]. Schottky source/drain structure is an attractive alternative to conventional doped source/drain to overcome these challenges. In addition to providing advantages of low resistivity, atomically sharp junction, and a simpler implantless fabrication process, the successful integration with low-temperature Schottky source/drain structure is critical for the full potential of Ge/high-k/metal gate stack to be realized. However, most of previous researches on Schottky source/drain transistor have been performed on Si-based devices using metal-silicides [3.7]-[3.9], and some reports on metal-germanides were performed with impractical device structures [3.10][3.11]. In this chapter, comprehensive studies on material and electrical properties of Ni- and Pt- germanide contacts on n-type Ge are

carried out, and the low temperature self-aligned Schottky source/drain p-MOSFETs integrated with HfO_2/TaN gate stack are also demonstrated.

3.1 Ni- and Pt-germanides investigation for Ge channel p-SSDT application

3.1.1 Experiment introduction

N-type (Sb-doped) (100) Ge wafers with a resistivity of 2.0~3.2 Ω·cm were used in this study. Wafers were dipped in diluted HF for 5 min to remove native oxide, and loaded into sputter system where Ni and Pt films with thickness of 10 and 30 nm were deposited, respectively. A shadow mask was used to form the Schottky contact with diodes diameter of ~1 mm. After metal deposition, samples were loaded into RTP and annealed at 300~500°C in N_2 ambient. Samples with diode structure were loaded into sputter system again and ~100 nm Al was deposited at wafer backside to form ohmic contact. The as-deposited and final contact structure as well as contact top view are illustrated in Fig. 3.1. SEM, HRTEM and XRD were applied to examine surface morphology, interface quality and crystallinity of Ni- & Pt-Ge after annealing, respectively, and the Schottky contacts were characterized by a Hewlett-Packard 4156A semiconductor parameter analyzer.



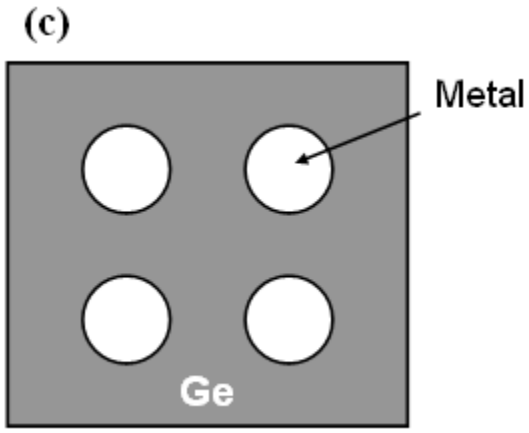


Figure 3.1 Schottky contact structure cross section view (a) as metal deposited (b) after RTA and germanide formation, and (c) top view of contacts.

3.1.2 Results and discussion

Figure 3.2 shows XRD scans of Ni- & Pt-germanide as a function of RTA germanidation temperature. Results show that at the annealing temperature ranging from 300 to 500°C, only single phase of NiGe was observed for Ni-germanide formed from 10 nm and 30 nm as-deposited Ni on Ge. Ge peak is detected from 10 nm Ni sample when temperature increases to 500°C. On the other hand, the formation of three different phases (PtGe, Pt_2Ge_3, and $PtGe_2$) and their transition of phases with increasing temperature are observed for Pt-germanides. The transition from the metal-rich phase PtGe to Ge-rich phase $PtGe_2$ with increased temperature shows that the Pt-Ge phase growth obeys the ordered Cu_3Au rule, which was proposed by d'Heurle in 1986 [3.12], and the reaction between Pt and Ge is diffusion controlled. It is also found that the transition to the $PtGe_2$, which shows the lowest resistivity of ~ 25 μΩ·cm (confirmed in Fig. 3.4), occurs at lower temperature for thinner Pt film (10 nm) and on patterned diode samples rather than on blanket Ge substrate.

The morphological stability of Ni- & Pt-germanides was investigated by SEM selectively shown in Fig. 3.3. For germanides formed by Ni and Pt with 30 nm thickness, no significant agglomeration is observed as shown in Fig. 3.3 (a) and (b). However, an apparent agglomeration after 450°C (Fig. 3.3 (c)) and increased agglomeration after 500°C (Fig. 3.3 (d)) were observed for Ni-germanide from 10 nm Ni sample. Pt-germanide from 10nm Pt exhibited no agglomeration up to 500°C (Fig. 3.3 (e) and (f)), suggesting better morphology than Ni-germanide.

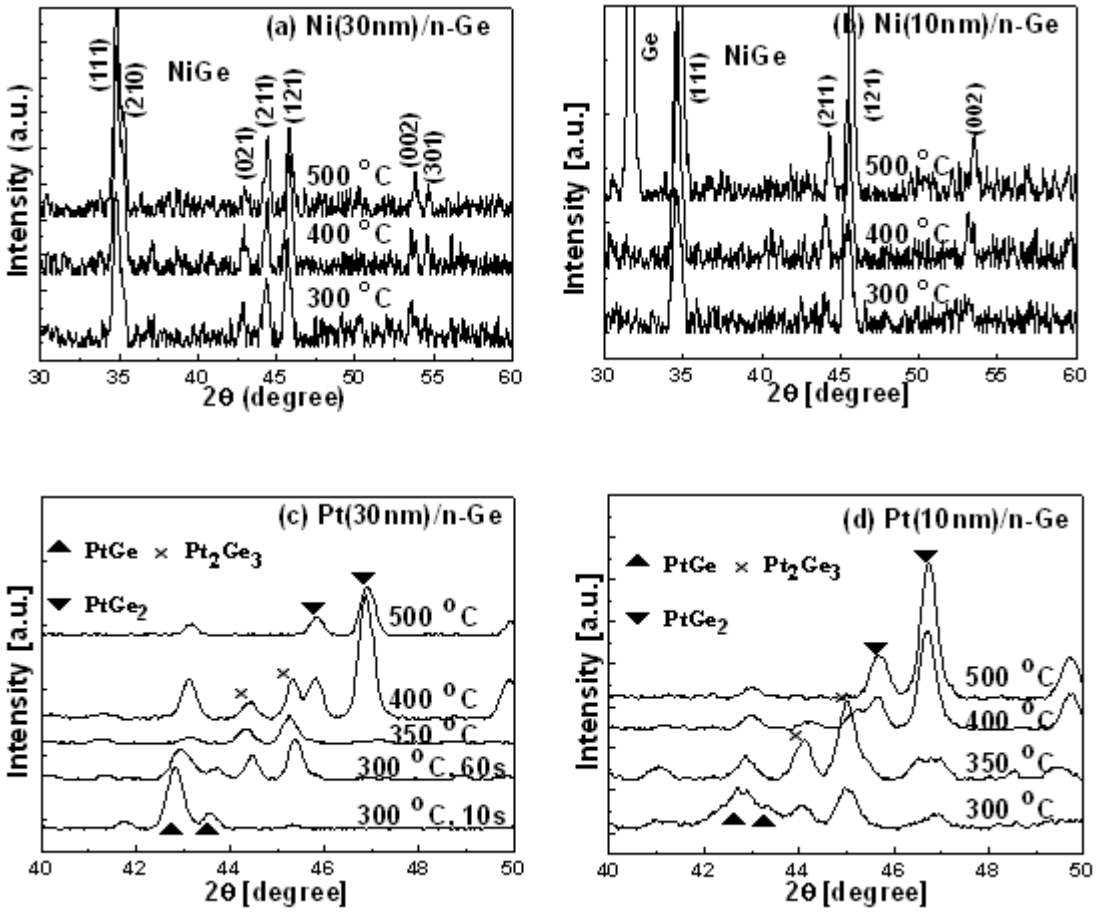


Figure 3.2 XRD results of Ni- and Pt-germanides formed from (a) 30 nm Ni, (b) 10 nm Ni, (c) 30 nm Pt, and (d) 10 nm Pt on Ge and annealed at 300~500°C for one minute.

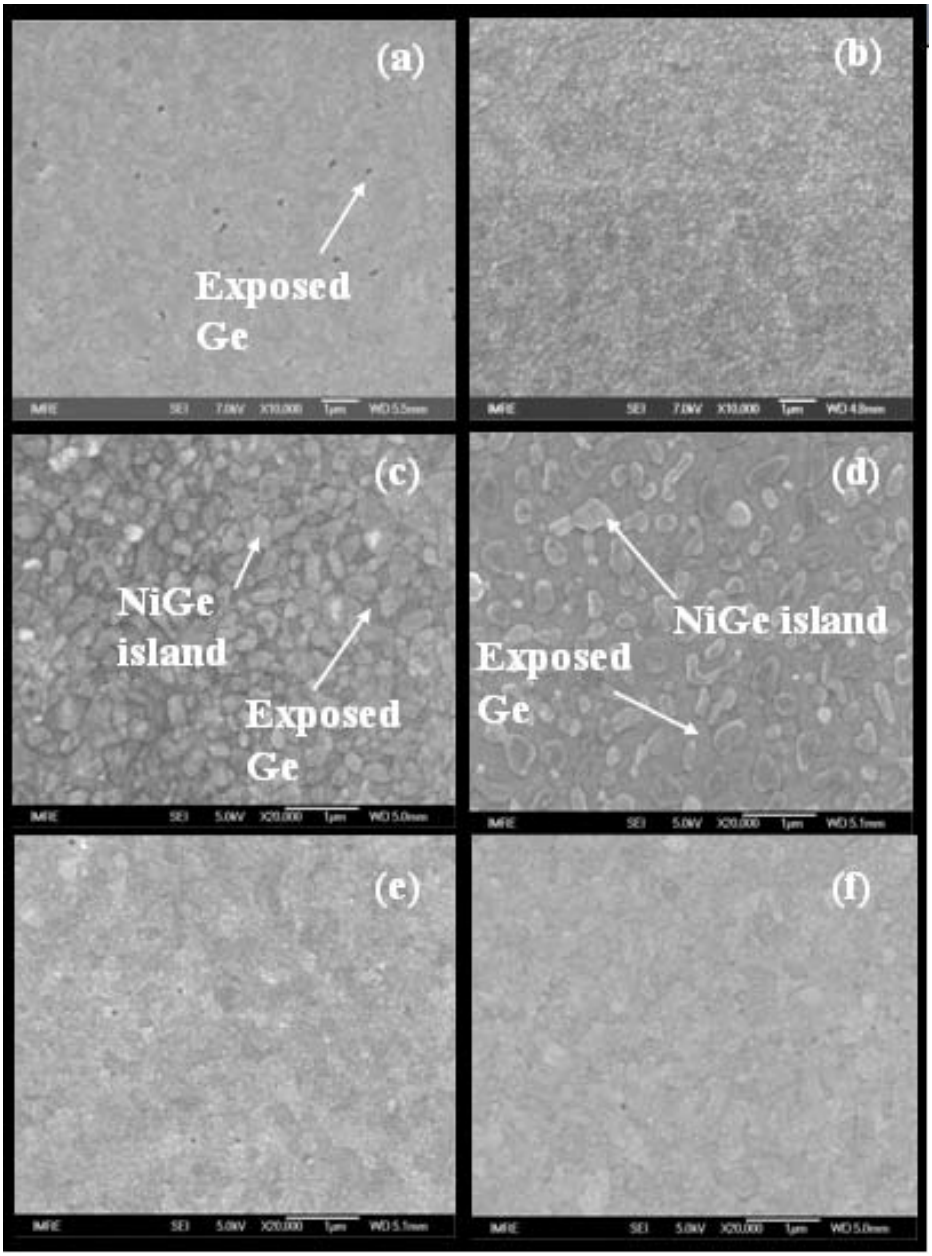


Figure 3.3 SEM images of Ni- and Pt-germanides formed by (a) 30 nm Ni at 500°C, (b) 30 nm Pt at 500°C, (c) 10 nm Ni at 450°C, (d) 10 nm Ni at 500°C, (e) 10 nm Pt at 450°C and (f) 10 nm Pt at 500°C.

The sheet resistance of Ni- & Pt-germanides formed at different temperatures is shown in Fig. 3.4. Constant sheet resistance of 3.4 ohm/sq was measured for NiGe (30nm Ni) formed at 300~500°C, which corresponds to resistivity of ~16 μΩ·cm. A dramatic

increase at 450°C for NiGe (10 nm Ni sample) is attributed to the significant agglomeration of NiGe as shown in Figure 3.3 (c). Recent research [3.13] has pointed out that by additional Ti incorporation, the agglomeration of NiGe can be significantly alleviated for thin Ni film (<10 nm) so that the process window of NiGe in Ge technology can be widened. On the other hand, the Pt-germanide film formed from 10 nm and 30 nm Pt respectively, both show a rapid decrease in sheet resistance above 350°C. This can be explained by the phase transition of Pt-germanide from PtGe phase to $PtGe_2$ phase as RTA temperature increases, as can be seen in Fig. 3.2 (c) and (d). No significant increase in sheet resistance was observed for Pt-germanide film with both thicknesses up to 500°C, indicating better thermal stability of $PtGe_2$ compared to NiGe with comparable germanide film thickness.

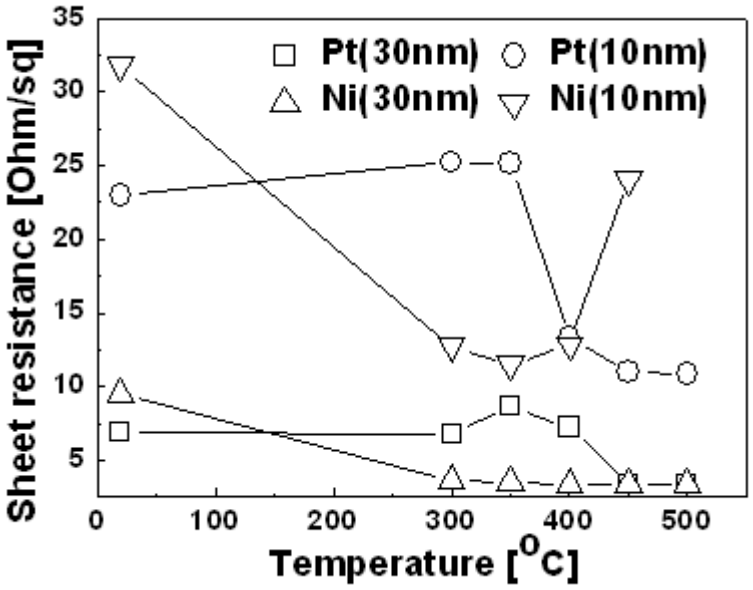
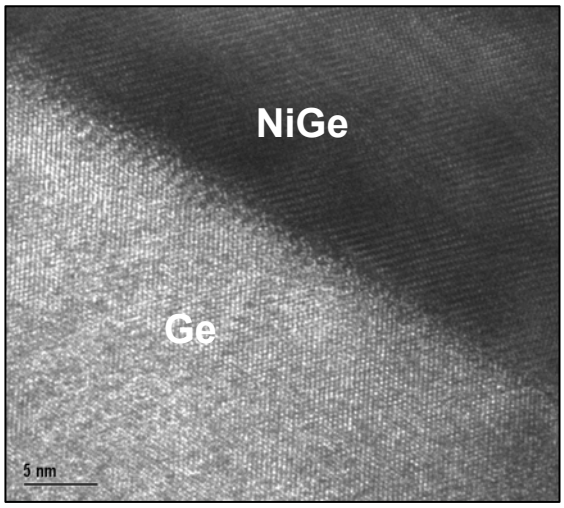
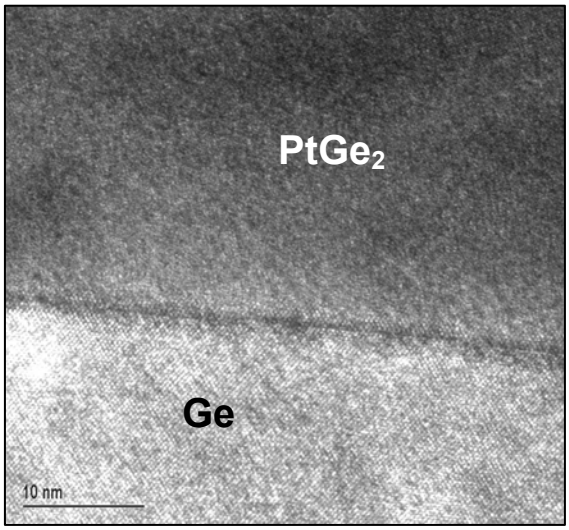


Figure 3.4 Sheet resistance of Ni- and Pt-germanides formed from 10 and 30 nm Ni and Pt at 300~500°C, respectively.



(a)



(b)

Figure 3.5 HRTEM pictures of (a) NiGe and (b) $PtGe_2$ formed at 400^o C.

HRTEM analysis was also used to study the Ni- & Pt-germanides after RTA at 400°C, as shown in Figure 3.5. Results show that uniform, epitaxial growth of NiGe and $PtGe_2$ germanide films are formed with smooth and sharp interfaces on Ge.

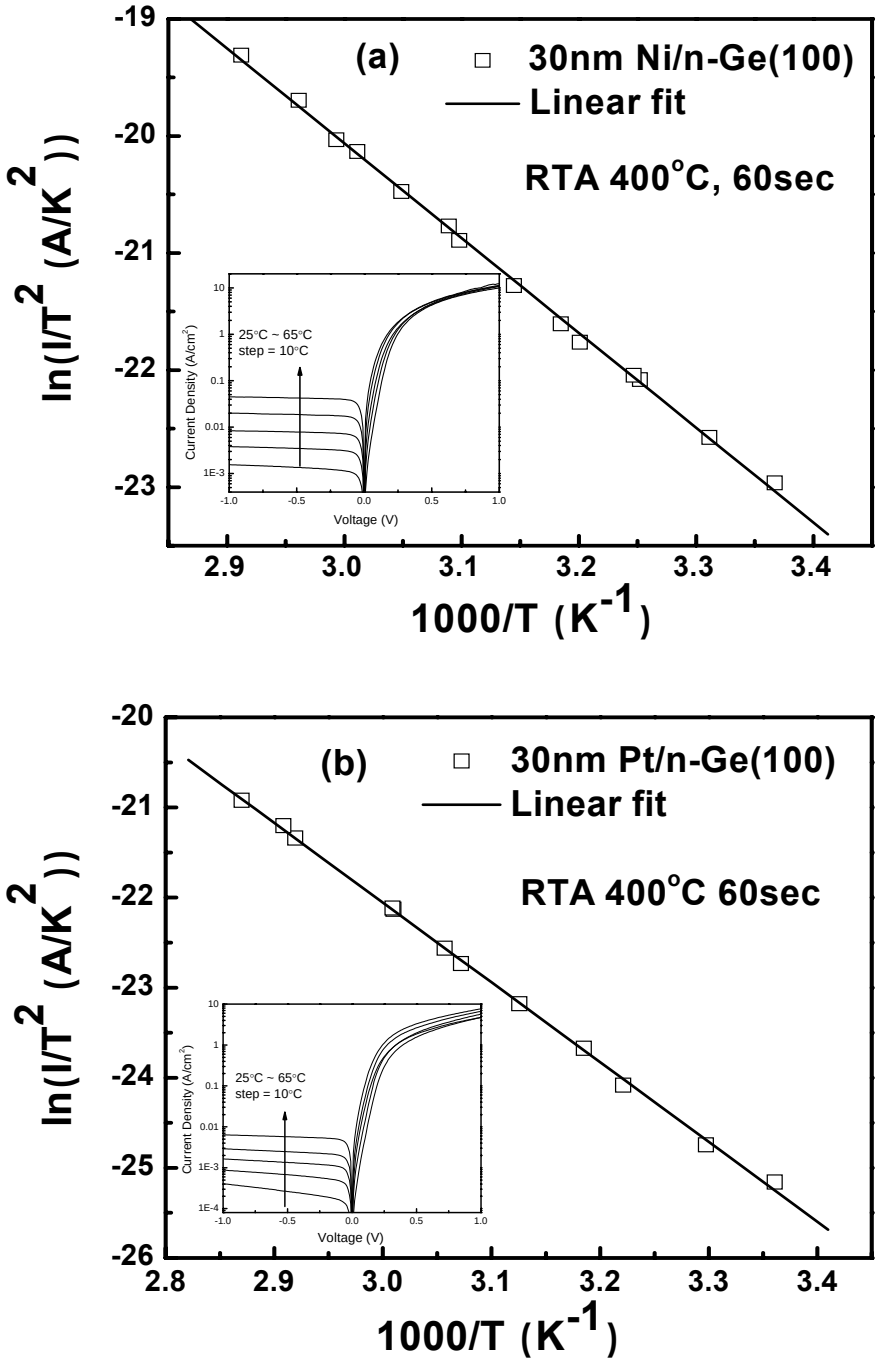


Figure 3.6 Richardson plots of forward current of (a) NiGe/n-Ge (100) and (b) $PtGe_2$/n-Ge (100) contacts with inset temperature dependent $I-V$ curves.

Figure 3.6 shows the Richardson plots of forward current of the Ni- & Pt-germanide Schottky diodes formed at 400°C with the temperature dependent $I-V$ curves as inset figure. From the $I-T$ method mentioned in Chapter 2, calculated effective $q\phi_{be}$ of Ni and Pt-germanides are 0.74 eV and 0.76 eV, respectively, even larger than Ge bandgap of 0.66 eV. Pt-germanides formed at 300~500°C exhibited similar $q\phi_{be}$ with ideality factor of $n = 1.0 \sim 1.1$, in spite of their different phases.

On the other hand, according to Eq. (2.8) in the $I-V$ method of barrier height measurement in Chapter 2, where Richardson constant A^* = 50 A $cm^{-2}K^{-2}$ for n-Ge (100) [3.14] [3.15], the $q\phi_{be}$ of NiGe/n-Ge and $PtGe_2$/n-Ge diodes extracted from the room temperature $I-V$ curves are 0.58 eV and 0.62 eV, respectively. A higher $q\phi_{be}$ therefore a lower $q\phi_{bh}$ obtained for PtGe suggests that PtGe could be more promising for Ge p-MOSFETs application than NiGe. A further discussion will be carried out in Chapter 3.3 and Chapter 4.2. The much higher barrier heights obtained from the $I-T$ method is most likely due to the presence of temperature dependent barrier height, i.e., $q\phi_{be} \approx q\phi_{be}(T=0K) - \beta T$, which means that $q\phi_{be}$ values of 0.74 and 0.76 eV determined from Richardson plots more or less reflect $q\phi_{be}$ values at $T = 0K$, rather than the value at measured temperatures [3.15]. The band gap of Ge decreases with increasing temperature is given by [3.16]

$$E_g(T) = 0.7437 - \frac{0.0004774 \times T^2}{235 + T} \text{ (eV)} \tag{3.1}$$

So the assumption of $I-T$ method that the barrier height is temperature independent is not satisfied, leading to an inaccurate value of $q\phi_{be}$.

3.2 Metal germanide Schottky source/drain Ge pMOSFETs integrated with TaN/HfO_2 gate stack

3.2.1 Experiment introduction

The fabrication of Schottky source/drain Ge MOSFETs follows the procedure described in previous chapter. After dipped in diluted HF to remove native oxide, n-type (Sb-doped) (100) germanium wafers were loaded into multi-cluster CVD system, where Ge substrate received plasma PH_3 treatment at 400^{o}C to improve the interface quality [3.4], followed by in-situ MOCVD HfO_2 deposition and post anneal at 400^{o}C. ~100 nm TaN was deposited as gate electrode by reactive sputtering. After gate patterning, ~30 nm Si_3N_4 spacer was deposited by PECVD at 250^{o}C. Before source/drain metal deposition, wafer received DHF clean again to remove native oxide and Si_3N_4 residue at source/drain region. ~30 nm Ni and Pt were respectively deposited by sputter, followed by rapid thermal anneal in N_2 ambient at 400^{o}C to form germanide at source/drain. Unreacted Ni and Pt were removed with diluted HNO_3 and diluted aqua regia solution respectively. Finally, ohmic contacts were formed on the backside of the substrates by deposition of Al film.

3.2.2 Results and discussion

The HRTEM image of TaN/HfO_2/n-Ge (100) gate stack of the p-MOSFETs fabricated with conventional self-aligned process is shown in Fig. 3.7. Owing to the low-temperature process (highest temperature is 400°C), the conformal MOCVD HfO_2 film remained amorphous maintaining ultra thin interfacial layer which is mainly formed

during HfO_2 deposition [3.4]. The $C-V$ curve measured at 1 MHz and gate leakage current of the TaN/HfO_2/Ge gate stack are shown in Fig. 3.8. By using a software developed by the UC Berkeley Device Group, and taking into account of quantum confinement effects, the EOT can be extracted. The extracted EOT is ~ 2.9 nm and the leakage current at 1 V is about 2×10^{-6} A/cm^2, which is consistent with the HfO_2 physical thickness of ~ 8 nm.

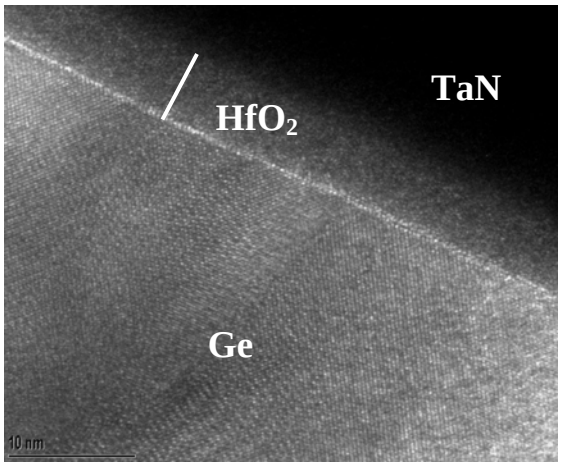
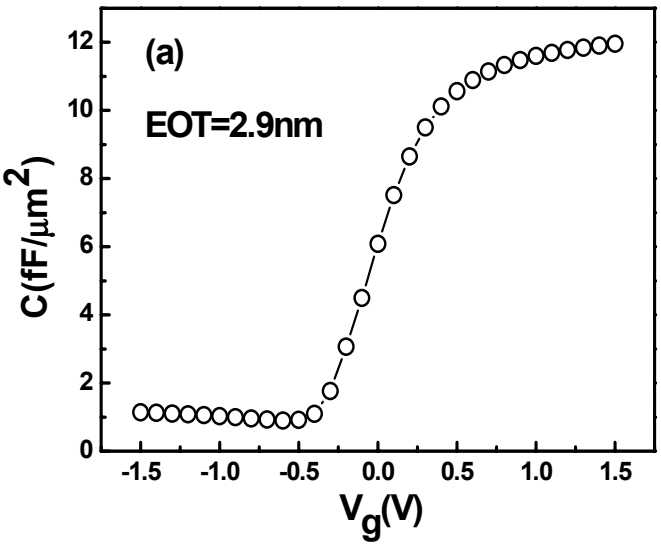


Figure 3.7 HRTEM image of the TaN/HfO_2/n-Ge (100) gate stack of a fully processed Schottky source/drain Ge p-MOSFET.



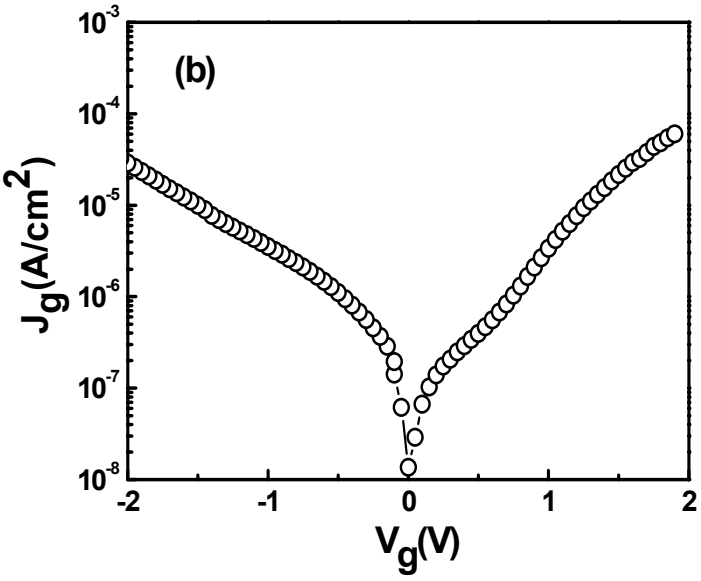


Figure 3.8 (a) capacitance-voltage and (b) current-voltage characteristics of TaN/HfO_2/n-Ge (100) gate stack.

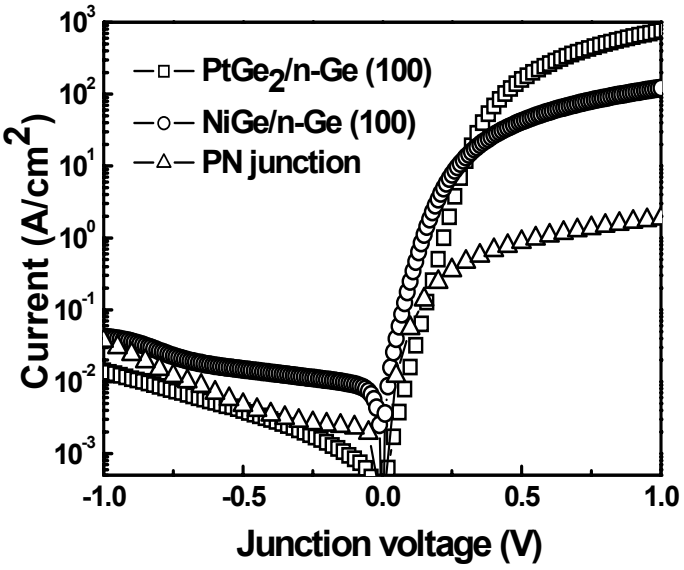


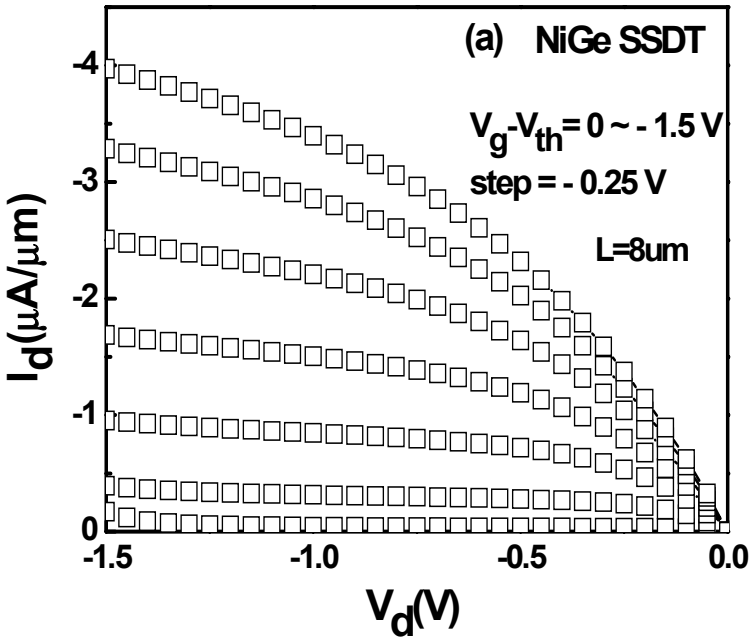
Figure 3.9 Forward and reverse current at junctions of Ni- & Pt-germanide source/drain and B-doped p^+/n junction.

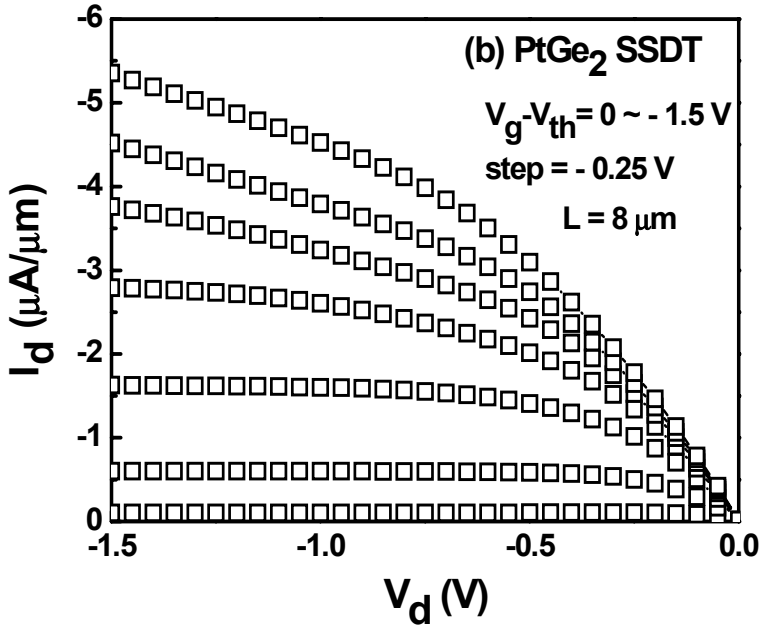
$I-V$ curves measured from NiGe/n-Ge and $PtGe_2$/n-Ge Schottky contacts at source/drain after SSDT fabrication as well as germanium p^+/n junction (Boron 1×10^{16}

cm^{-2}, 35 KeV, forming gas anneal at 400° C, 10 min) are shown in Fig. 3.9. Since limited dopant solid solubility in Ge and un-efficient activation, compared to p^+/n junction, Ni- & Pt germanide/n-Ge Schottky diodes have comparable reverse current, but much higher forward current, which can be attribute to the higher density of available electrons in metal-germanide than in doped source/drain. $PtGe_2$/n-Ge junction exhibits lower reverse current compared to NiGe/n-Ge due to higher electron barrier height between $PtGe_2$/n-Ge (0.51 eV for NiGe/n-Ge and 0.60 eV for $PtGe_2$/n-Ge extracted from Fig. 3.9 using $I-V$ method in Chapter 2). It is noted that rectification character of the NiGe/n-Ge and $PtGe_2$/n-Ge Schottky contacts degraded after transistor fabrication compared to diodes made by shadow mask (0.56 eV for NiGe/n-Ge and 0.63 eV for $PtGe_2$/n-Ge), which will be discussed later.

Figure 3.10 shows the output characteristics ($I_d - V_d$) and transfer characteristics ($I_d - V_g$) of NiGe and $PtGe_2$ Schottky source/drain Ge p-MOSFET with channel width/length = 400/8 μm. The drain current at $V_d = V_g - V_{th} = -1$ V is ~ - 2.3 and - 3.5 μA/μm, and the I_{on}/I_{off} ratio obtained at $V_d = -0.1$ V is ~ 10^3 and 10^4 for NiGe and $PtGe_2$ Schottky source/drain MOSFETs, respectively. The main reason for the I_{on} increase and I_{off} reduction in $PtGe_2$ SSDT than that of NiGe SSDT, is believed to be ~ 0.1 eV higher ϕ_{be} of $PtGe_2$/n-Ge contact than that of NiGe/n-Ge contact by using the same $I-V$ method to extract ϕ_{be}. Moreover, compared to the conventional Ge p-MOSFET with boron-doped source/drain [3.4], $PtGe_2$ source/drain p-MOSFET provides a comparable I_{on} but 80% decrease in I_{off} with similar effective hole mobility, suggesting no degradation induced by Schottky contact at the source/drain. Further reduction of I_{off}

can be achieved by using ultrathin Ge/SiGe on insulator substrates where the contact areas can be dramatically reduced.





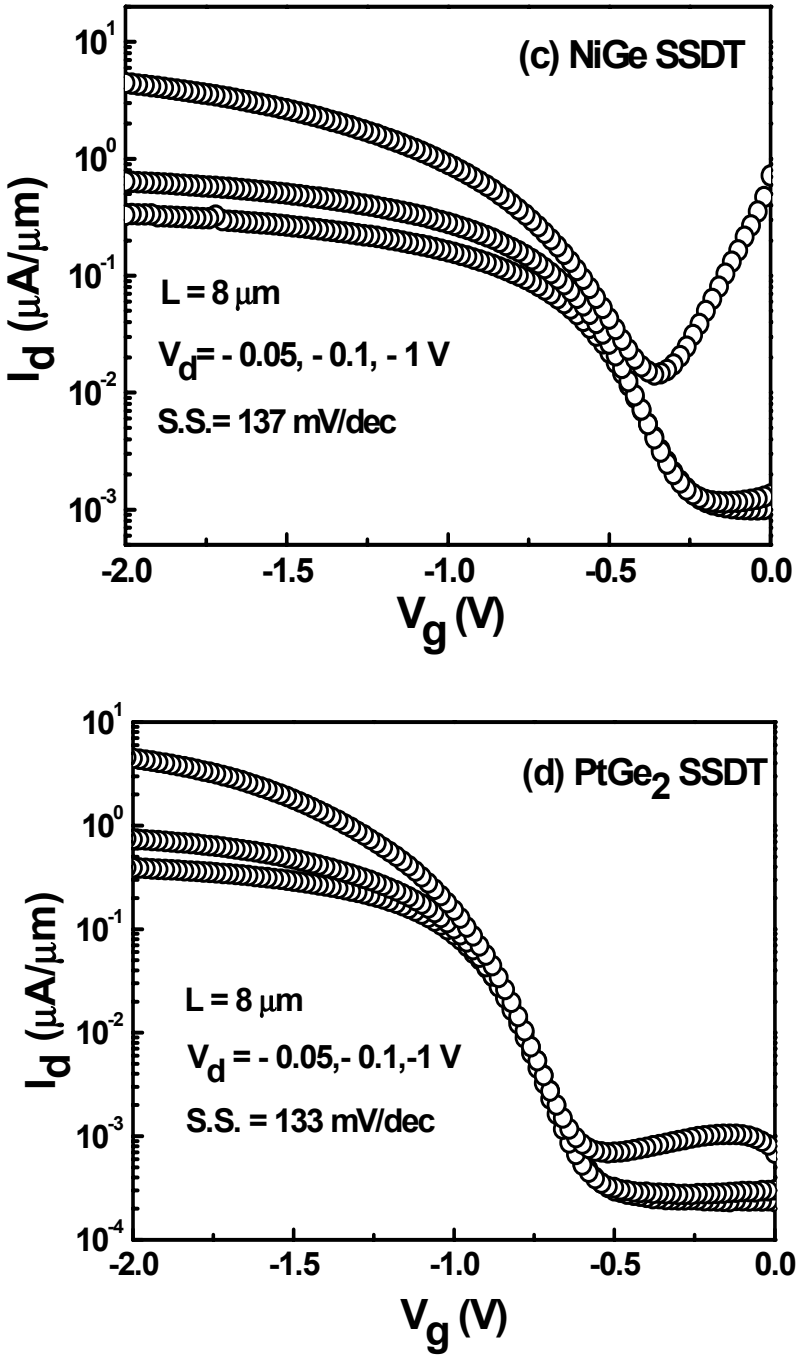


Figure 3.10 Output characteristics of (a) NiGe and (b) $PtGe_2$ Schottky source/drain Ge p-MOSFETs; and transfer characteristics of (c) NiGe and (d) $PtGe_2$ Schottky source/drain Ge p-MOSFETs.

3.3 Process integration issues in Schottky source/drain Ge p-MOSFETs integrated with TaN/HfO_2 gate stack

3.2.1 Simulation of NiGe Schottky source/drain Ge p-MOSFET with different spacer thickness

Since spacer is one of the most important parts in a Schottky source/drain transistor, which physically and electrically isolated metal source/drain and metal gate, simulation was carried out to investigate the suitable spacer thickness based on the assumptions: (1) no pinning at metal/Ge interface; (2) metal work function equals to metal germanide work function; (3) no contact resistance, all the resistance come from channel and under spacer region; and (4) no degradation of carrier mobility. The work function of NiGe source/drain used in this simulation is 5.15 eV, Ge substrate doping concentration is 1×10^{16}cm^{-3} and gate lengths are 8μm and 50nm, respectively, with SiO_2 of 5 nm as gate dielectric. The simulation is programmed by Argarwal Naveen (Silicon Nano Device Laboratory, National University of Singapore) with Synopsys Medici.

Simulated output characteristics I_d–V_d curves of NiGe Schottky p-MOSFETs with gate length of 8 μm and 50 nm are shown in Fig. 3.11 (a) and (b), respectively. As can be seen, the channel conductance in linear region of I_d–V_d curve increases with spacer thickness decreases in both cases. Especially, the dependence becomes more significant when channel length is comparable to spacer thickness in dimension, such as in short channel transistor.

However, simulation results also show that long channel (gate length of 8 μm, Fig. 3.12 (a)) transistor with spacer thickness less than 10nm experiences high off current at

high V_d . As such, a spacer with thickness of 10~20 nm seems to be appropriate for long channel device and has been applied in this study. For short channel transistor, generally a thicker spacer helps to reduce punch through effect which results in high off current, however, with a trade-off of I_d as shown in Fig. 3.11 (b).

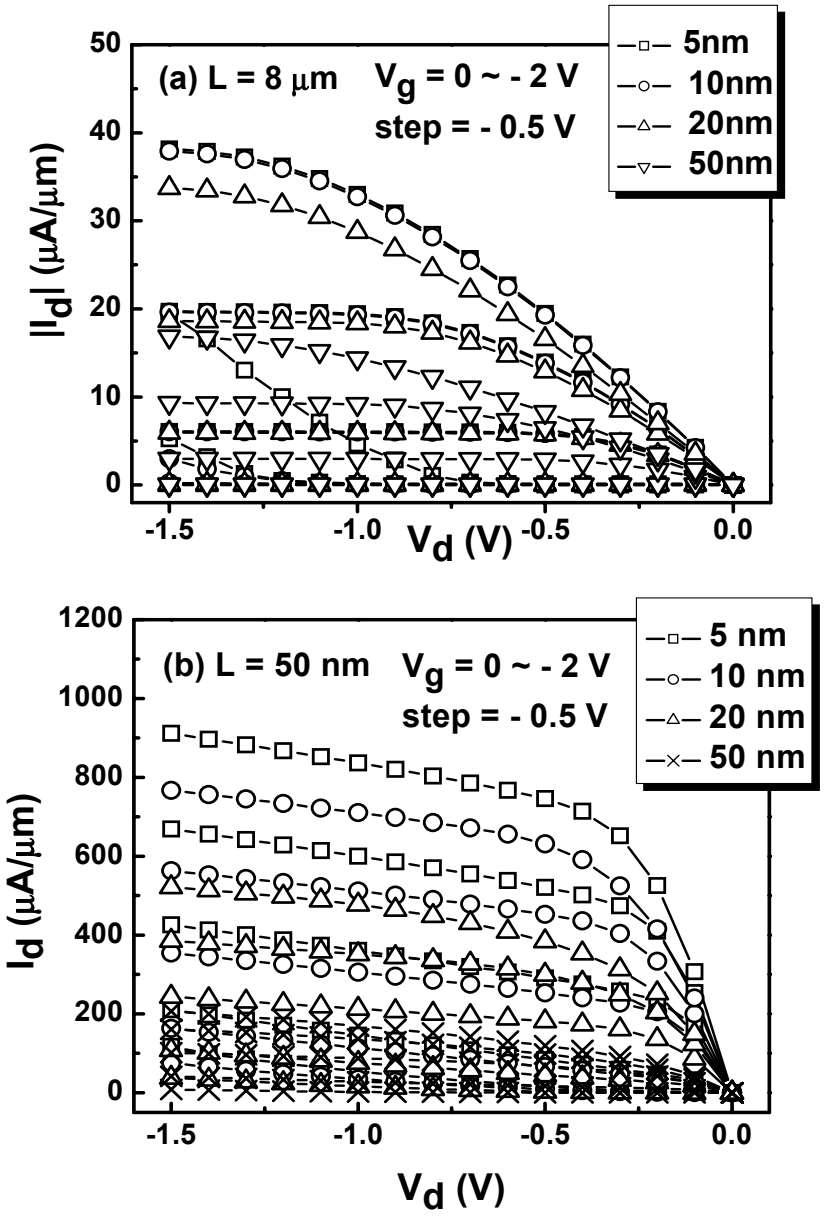


Figure 3.11 Simulated output characteristics (I_d–V_d) of NiGe Schottky p-MOSFETs with gate length of (a) 8 μm and (b) 50 nm for different spacer thickness.

3.2.2 A robust, self-aligned Pt germanide process

It is well known that one of the most critical process steps for the formation of Pt germanide Schottky source/drain Ge MOSFETs is the selective removal of unreacted Pt after germanide formation. In literature Pt germanide process usually integrated with unconventional back gate configuration structure where a buried oxide and the substrate work as gate dielectric and gate electrode of the transistor by lift-off process [3.10]. Reactive ion etching (dry etching) process is also used which removes both uncreative Pt and Pt germanide without selectivity [3.17] [3.18]. However, there is no report available on conventional self-aligned wet etching process for the formation of Pt germanide Schottky source/drain. This is mainly due to the fact that the Pt etching solution, aqua regia, aggressively etches Pt germanide at an even faster rate than Pt, leading to non-uniformity and low yield of well-behaved $PtGe_2$ Schottky source/drain transistors shown earlier in this chapter. Later, enlightened by the studies [3.19] on formation of a protective SiO_x surface hard mask on Pt silicide by surface oxidation of Pt silicide, a study on surface nitridation treatment, i.e. plasma nitridation of Pt germanide, was carried out and found that the formed GeN_x can effectively protect Pt germanide from being etched during aqua regia wet etching process, which is believed to be a promising method to realize the robust self-aligned selective wet etching process for Pt germanide Schottky source/drain Ge MOSFETs formation.

The Ge wafers used in this experiment were also n-type Sb doped (100) wafers with a resistivity of 2.0 ~ 3.2 Ω • cm. After DHF cleaning, ~30 nm pure Pt was deposited on the wafers by sputter and received a RTA process in N_2 ambient at 400^{o}C for 1 minute to form $PtGe_2$. Some Pt germanide samples were subjected to plasma nitridation

process with a power supply of 400 W, a fluence of N_2 at 120 sccm and a chamber pressure at 4 mTorr with a temperature of ~150° C in an inductively coupled plasma (ICP) chamber for one min, without or with substrate bias at 100 W. XPS with a standard Al X-ray source was used to analyze the chemical states of the samples. All of the XPS spectra were collected at a take-off angle of 30°, with beam energy of the X-ray source at 10 KeV, and the path energy of the photoelectron analyzer at 30 KeV with a step size of 0.1 eV. After being dipped in diluted aqua regia ($HCl:HNO_3:H_2O$=3:1:7) at 80° C, the surface morphology and sheet resistance (Rs) of the samples were characterized by SEM and a four-point probe using the van der Pauw method with a correction factor [3.20] as discussed in Chapter 2, respectively.

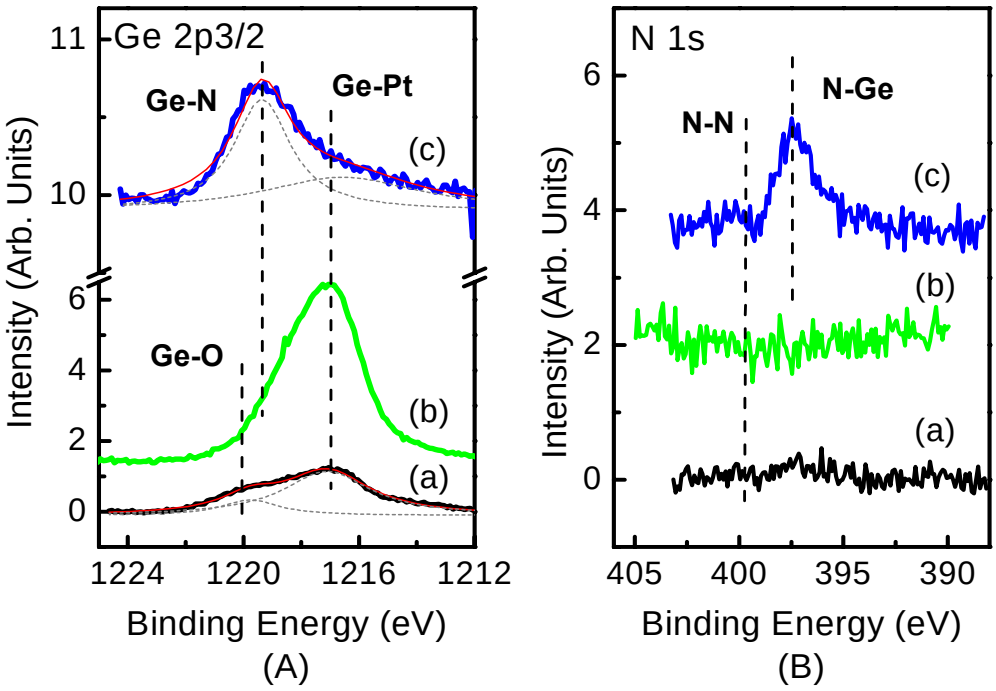


Figure 3.12 XPS data of (A) Ge 2p3/2 and (B) N 1s spectra for Pt/Ge substrate with RTA at 400° C for 1 minute [curve (a)], and the substrate with RTA and nitridation without [curve (b)] or with [curve (c)] substrate bias.

To understand both the effects of RTA and nitridation treatment on Pt/Ge samples, the Ge 2p3/2 [Fig. 3.12 (A)] and N 1s XPS [Fig. 3.12 (B)] spectra were obtained for a ~30 nm Pt/n-Ge (100) substrate with RTA at 400°C for 1 minute [curve (a)], and the Pt/Ge substrates with the same RTA treatment followed by a ICP plasma nitridation treatment for 1 minute without [curve (b)] or with [curve (c)] substrate bias at 100 W. Previously, we have shown [3.21] that after being anneal in N_2 ambient at 400°C for 1 minute, the ~30 nm Pt has fully reacted with the Ge substrate to form a layer of ~60 nm single phase $PtGe_2$ with a sharp $PtGe_2$/Ge interface on the Ge substrate. Therefore, the peaks located at ~1217 eV and ~1220 eV in curve (a) are attributed to the Ge-Pt bond and Ge-O bond [3.22] on the sample surface, respectively. The oxygen is believed to be introduced by the residual O_2 in the RTA chamber, which reacts with Ge substrate to form GeO_x on sample surface during RTA.

For the sample with the RTA followed by nitridation treatment for one min without substrate bias, the Ge 2p3/2 spectrum [Fig. 3.12 (A) curve (b)] is dominated by Ge-Pt peak with a significant enhancement on its intensity while the intensity of Ge-O peak becomes negligible as compared to the counter parts in curve (a) for the sample with RTA only. Also, there is absence of indications of any N-N bond (~399 eV) [3.22] and Ge-N bond (~397.4 eV) [3.22] in curve (b) of Fig. 3.12 (B), as the same of the RTA sample. These may be attributed to the decomposition of Ge-O bonds while unsuccessful formation of Ge and Pt nitridation products during the plasma nitridation treatment, which leaves the sample surface to be mainly covered by Ge-Pt bonds and Ge dangling bonds.

However, when the sample is subjected to the RTA followed by nitridation treatment for one min with substrate bias at 100 W, curves fitting of the Ge 2p3/2 spectrum reveal two peaks: one at ~1219 eV with a relatively strong intensity, another at ~1217 eV with a weak intensity which is attributed to Ge-Pt bond as also observed in spectra for the samples with RTA only [curves (a)] and RTA followed by nitridation without substrate bias [curves (b)]. The peak at ~1219 eV that dominates the Ge 2p3/2 spectrum is attributed [3.22] to Ge-N bond corresponding to the occurrence of GeN_x on sample surface. In ICP etching process, it is well known that a substrate bias greatly enhances the extraction of ions from the plasma above the substrate surface. Therefore, it is believed that additional supply of 100 W substrate bias helps sample to extract much more nitrogen ions in the plasma to bombard the $PtGe_2$ surface in comparison with the situation in the nitridation process without substrate bias, which results in the formation of a very thin layer of GeN_x covering the substrate. The existence of GeN_x is also confirmed by the observation of N-Ge peak (~397.4 eV) [3.22] in the N 1s spectrum as shown in curve (c) of Fig. 3.12 (B).

Figure 3.13 shows the surface morphology of Pt/Ge samples with the RTA and nitridation treatment before and after wet etch by a diluted aqua regia for 1 or 5 minutes. For the sample with nitridation without substrate bias, it is clear that the substrate surface has been aggressively attacked after being etched for one minute, leaving a high density of large-area pits as shown in Fig.3.13 (c). In contrast, as Fig. 3.13 (d) indicates, for the sample treated by nitridation with substrate bias, the substrate surface keeps smooth and uniform before and after being etched up to 5 min. It is believed that the GeN_x layer formed during nitridation treatment prevents the $PtGe_2$ underneath from being etched,

similar to the function of SiO_2 layer formed by surface oxidation of Pt silicide in Pt/Si system [3.19], which acts as a protective surface hard mask for Pt silicide during aqua regia etching. In addition, it is observed that the etching rate for $PtGe_2$ and Pt in the diluted aqua regia at 80° C is 30~40 nm/min and 6~7 nm/min, respectively. Therefore, a 5-minute etching is able to remove a Pt layer of ~30 nm which is corresponding to a $PtGe_2$ source/drain with depth of 60 nm.

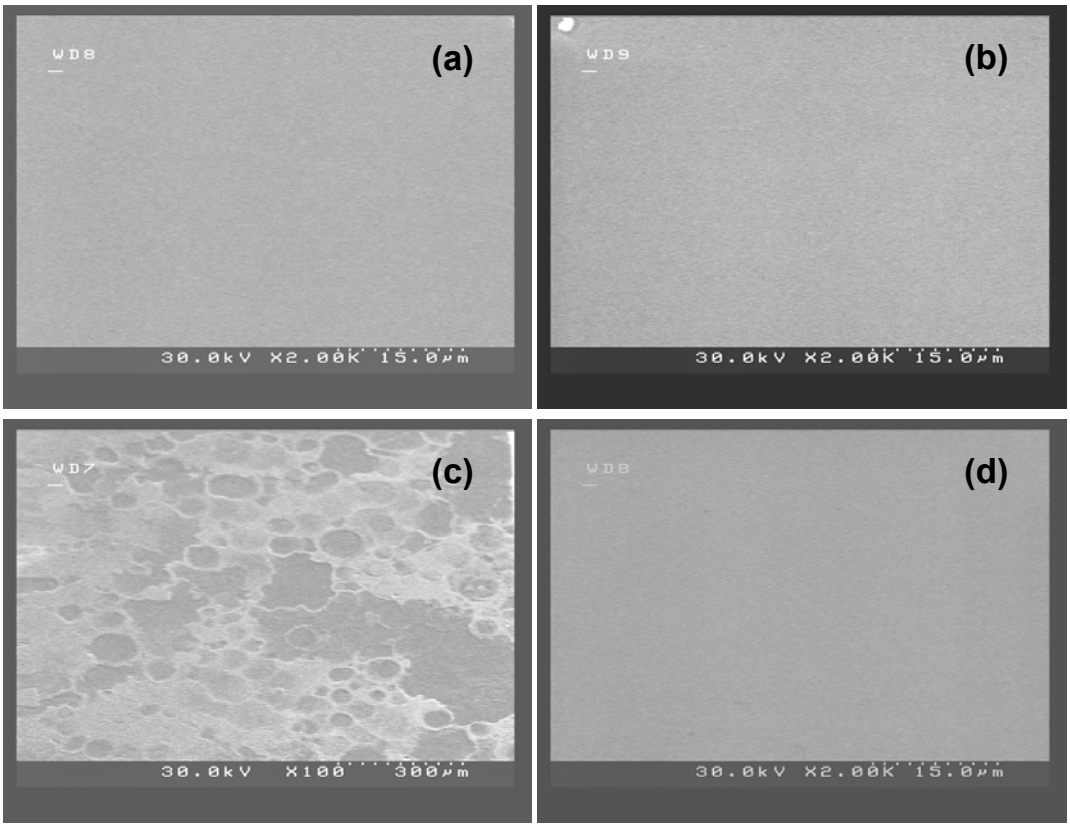


Figure 3.13 Surface morphology (by SEM) of Pt/Ge substrates with RTA and (a) one min nitridation without bias, (b) one min nitridation with bias, (c) one min nitridation without bias and wet etch for one min, and (d) one min nitridation with bias and wet etch for 5 minutes.

Furthermore, measurement of Rs was taken before and after a sample was etched. As Table 3.1 indicates, for Pt/Ge sample with RTA only or with both RTA and nitridation without substrate bias, the Rs dramatically increases after being etched for one min from 5.5 to 89.0 Ω/□, and 6.6 to 86.8 Ω/□, respectively. However, for the sample with RTA and nitridation with substrate bias the Rs value remains consistently low as 6.9, 6.9 and 6.7 Ω/□ for the sample before etching, after etching for one and 5 minutes, respectively. This further implies that the GeN_x layer effectively protects $PtGe_2$ from being attacked during wet etching.

Table 3.1. Summary of Rs values for samples with different treatments before and after diluted aqua regia etching.

Pt/Ge treatment		Sheet resistance (Ω/□)		
		RTA	RTA and plasma nitridation for 1 min without substrate bias	RTA and plasma nitridation for 1 min with 100 W substrate bias
Before wet etch		5.5	6.6	6.9
After wet etch	1 min	89.0	86.8	6.9
	5 min			6.7

3.4 Conclusion

In this chapter, comprehensive studies on Schottky contact properties of Ni- & Pt-germanides on n-Ge show that both materials provide promising merits for p-MOSFETs. While only single phase of NiGe was observed by XRD analysis after Ni-Ge anneal from

300 to 500°C for Ni thickness of both 10 and 30 nm, Pt-Ge system shows the formation and transition of 3 different phases (PtGe, Pt_2Ge_3, $PtGe_2$) after anneal and the germanium concentration in Pt germanide increase with increasing anneal temperature. The $PtGe_2$ phase also shows the lowest resistivity of ~ 25 μΩ·cm, which is higher than that of NiGe phase (~ 16 μΩ·cm). $PtGe_2$ film has a better thermal stability compared to NiGe. SEM analysis revealed that agglomeration happens in NiGe film when annealed at 500^{o} C, especially for thinner NiGe film, while smooth morphology for $PtGe_2$ annealed at the same temperature. Uniform, epitaxial growth of germanide films with smooth and sharp interfaces on Ge are observed for both materials. $q\phi_{be}$ extracted from $I-V$ curves $PtGe_2$/n-Ge and NiGe/n-Ge Schottky contacts are 0.62 and 0.58 eV, respectively, which means $q\phi_{bh}$ as low as 0.04 and 0.08 eV can be achieved.

Schottky source/drain transistors using Ni and Pt germanide are also fabricated on n-Ge-substrate with CVD-HfO_2/TaN gate stack which has a highest process temperature at 400^{o} C. Ni and Pt germanide Schottky junction at source/drain show improved forward and reverse current, compared to conventional B-doped Ge MOSFET. In addition, the higher I_{on} and lower I_{off} are obtained from Pt-germanide MOSFET than those of Ni-germanide MOSFET and convention Ge-pMOSFET.

Some work on process optimization is also included. Simulation on spacer thickness shows that for long channel transistors, the suitable spacer thickness seems to be 10~20 nm, while for short channel transistor, thicker spacer can help to reduce short channel effect but at the cost of reduced I_{on}.

At last, we proposed a robust self-aligned Pt germanide process by demonstration a surface plasma nitridation treatment on Pt germanide that is able to effectively protect Pt germanide from being attacked during aqua regia wet etching process. XPS analysis suggests that a very thin protective GeN_x layer exists on the sample surface after plasma nitridation for one min with substrate bias at 100 W. A smooth and uniform surface morphology and consistent low Rs of the samples are also obtained after wet etching by SEM and four-point probe method, respectively. This nitridation treatment seems to be a promising method to realize robust self-aligned selective wet etching process for Pt germanide Schottky source/drain MOSFETs formation.

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Chapter 4

Metal germanides with low electron barrier height for Ge n-MOSFET application

As mentioned in Chapter 1, the potential use of Ge as channel material and Schottky source/drain structure in future MOSFETs have triggered the active search for suitable germanides, which can be formed in a self-aligned manner through solid-state reactions of Ge and metals. In Chapter 3, studies on Ni- and Pt- germanides have shown that they are among the most promising candidates for Schottky source/drain Ge p-MOSFETs application [4.1] [4.2] and Ni- & Pt- germanide Schottky source/drain p-MOSFETs have been demonstrated with improved performance compared to conventional-doped source/drain Ge p-MOSFETs [4.3]-[4.5]. However, for n-MOSFETs, there has been no serious attempt to identify suitable germanide materials for the same application, i.e., germanides with low barriers to n-type Ge. In this chapter, two tempts were carried out to explore potential germanide candidates for n-MOSFETs application. One is to investigate metal germanide properties formed by reaction between Ge and rare earth metal (REM) which has a low metal work function. The other is to reduce NiGe barrier height to n-Ge by using a valence mending adsorbate, Sb, segregation during Ni germanidation.

4.1 REM metal (Er, Yb) germanide/p-Ge (100) contacts and Er-germanide Schottky S/D Ge n-MOSFETs

4.1.1 Introduction

Earlier works on electrical contact formation on n-Si have shown that REM silicides (e.g., $ErSi_2$ and $YbSi_2$) yield low Schottky barriers (~0.28 eV) on n-type Si and can be grown with high-quality epitaxy on Si (111) and (100). Ge has the same face-centered cubic structure as Si and REM germanides typically have a hexagonal AlB_2 structure as their silicide analogues. It is thus expected that REM germanides also exhibit low Schottky barrier heights to n-Ge (100) and therefore suitable for electrical contact formation in Ge n-MOSFETs either as ohmic contacts to n^+ source/drain or as Schottky source/drain. In this part, Er and Yb germanides are investigated in the view of material and electrical properties, and Ge n-MOSFET with Er germanide Schottky source/drain is also demonstrated.

4.1.2 Experiment

Germanide/p-Ge contacts were fabricated using Ga doped p-Ge (100) wafers (5.10-3.90 Ω•cm). After dipping in diluted HF (HF: H_2O=1:100) for 5 min to remove native oxides from the surfaces, wafers were loaded into PECVD chamber where ~100 nm Si_3N_4 was deposited as field isolation material. The active region was defined by lithography and RIE, followed by DHF clean for one min to remove residue Si_3N_4 and germanium native oxide. After loading the wafers into the chamber of a dc magnetron sputtering system, ~30 nm thick Er and Yb were sputter-deposited onto the wafers,

followed by a reactive sputtering deposition of W with a thickness of 50 nm as capping layer to prevent REM from oxidation in consequent RTA process. After germanidation in RTA chamber, W capping layer was removed by RIE and unreacted REM was selectively removed by diluted HNO_3 (HNO_3:H_2O=1:20) for 3 min. Finally ~100 nm Al was deposited at wafer backside to form backside ohmic contact.

The Er-germanide Schottky source/drain n-MOSFET fabrication follows the similar procedure with Ni and Pt p-MOSFETs fabrication discussed in Chapter 2. After DHF cleaning and surface passivation, CVD HfO_2 and PVD TaN were deposited consequently to form the gate electrode. 30 nm Er and 50 nm W were deposited after spacer formation, followed by RTA germanidation, RIE to remove W and selective etch process to remove unreacted erbium.

4.1.3 Results and discussion

Figure 4.1 (a) shows the XRD results of as deposited 50 nm W/30 nm Er film and Er-germanide formed after anneal from 250^{o}C to 400^{o}C. No Er-germanide peak was detected up to 250^{o}C though Er peak was weaker compared to that observed in as deposited sample, showing that at 250^{o}C, Er and Ge interdiffusion happens, may be accompanied with slightly amorphous germanide formation. Obvious Er_2Ge_3 peak was observed when the anneal temperature increased to 300^{o}C, indicating a highly textured Er_2Ge_3 film was formed. The absence of Er peak implies the full reaction of as-deposited Er with Ge substrate after anneal at 300^{o}C 1min. With anneal temperature increased to 400^{o}C, weak Er_3Ge_4 peaks were detected too. It is also noted that, no erbium oxide peak was detected and the intensity of W peak was strong and constant from the as-deposited

sample to the sample after anneal at different temperature, proving that W film which acted as oxygen barrier that can prevent erbium from oxidation and still remained intact after anneal, is promising as capping layer for REM process.

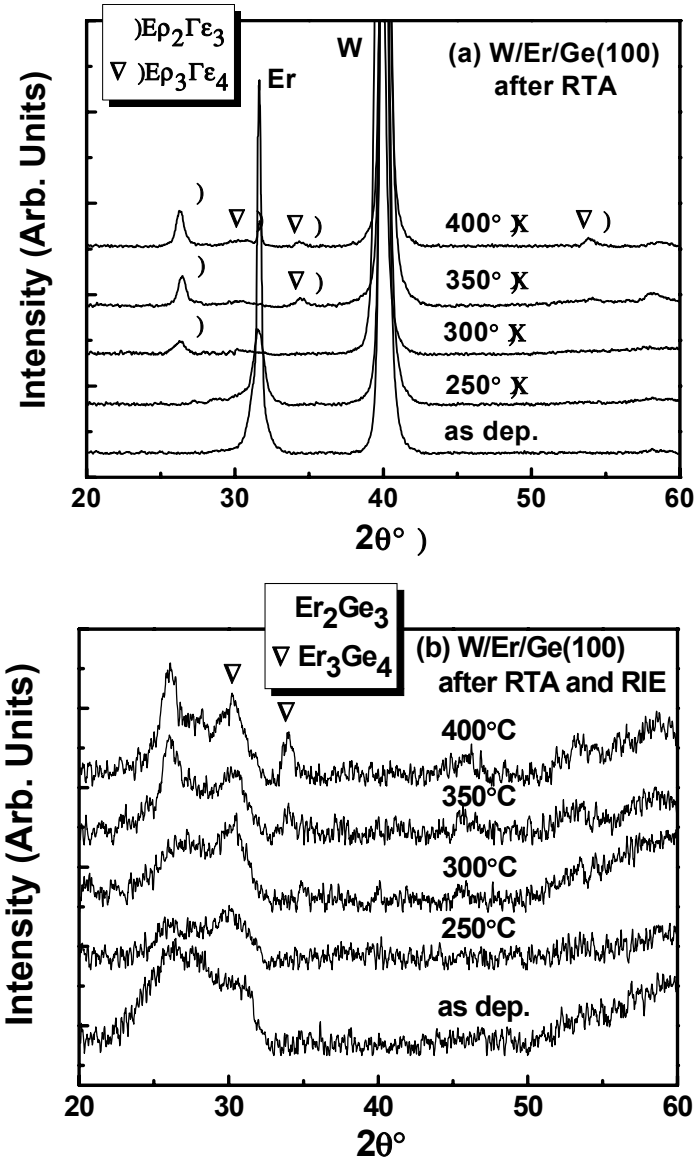


Figure 4.1 XRD results of (a) Er-germanide formed by 50nm W/30 nm Er/p-Ge (100) after RTA at 300^{o} C, 400^{o} C and 500^{o} C, respectively, and (b) Er-germanide in (a) after W removal by RIE.

The XRD results of Er-germanide after W capping layer removed by RIE are also shown in Fig. 4.1 (b). It is observed that although RIE does not alter the Er-germanide phases, crystallized germanide film tends to be amorphous. Due to the lack of information on Yb-Ge in the respective powder diffraction file [4.6], XRD results of Yb germanide are not included here.

The sheet resistance value of Er-Ge and Yb-Ge phases formed at different RTA temperatures were obtained using four-point probe measurement, shown in Figure 4.2. It is clear that the Er_2Ge_3 formation is correlated well to the variation of the sheet resistance. A minimum sheet resistance of 6.8 and 5.95 Ω/□, corresponding to a resistivity value of 27.2 and 26.8 μΩ•cm are obtained for Er and Yb germanide respectively, which is significantly lower than the resistivity values of ~30-40 μΩ•cm reported for REM silicides such as $YbSi_{2-x}$ and $ErSi_{2-x}$ [4.7] [4.8].

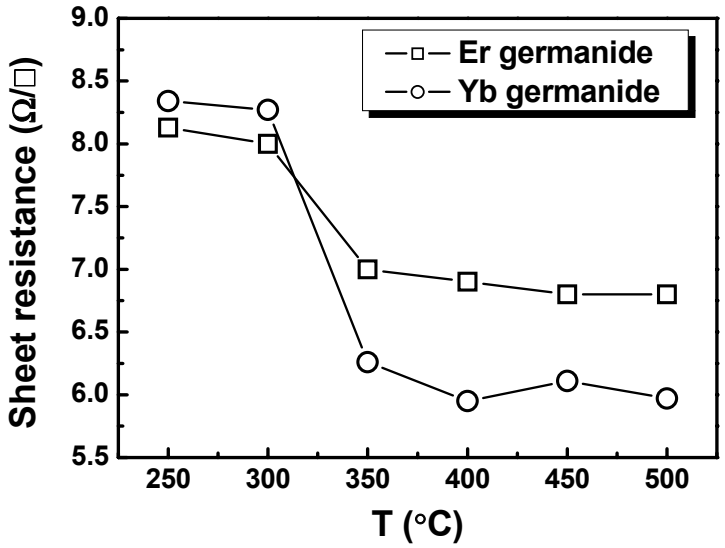


Figure 4.2 Sheet resistance of 30 nm Er/p-Ge (100) after annealing at temperature from 250° C to 500° C.

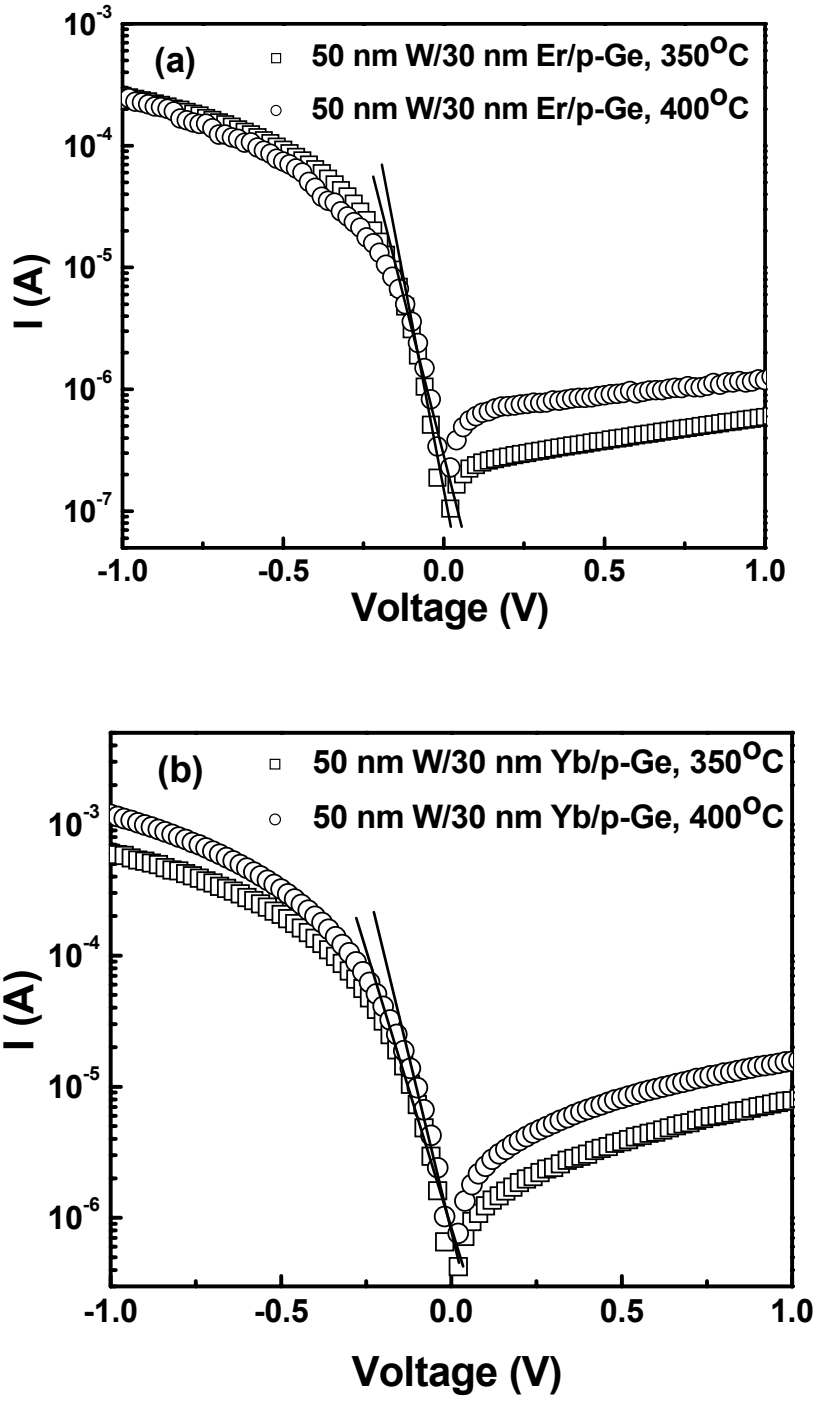


Figure 4.3 Current-voltage ($I-V$) characteristics at room temperature for (a) 50 nm W/ 30 nm Er/p-Ge (100) and (b) 50 nm W/ 30 nm Yb/p-Ge (100) contacts after anneal at 350 ^{o} C and 400^{o} C, respectively.

Current-voltage characteristics measured at room temperature for Er-germanide/p-Ge (100) and Yb-germanide/p-Ge (100) contacts after RTA 350^{o} C and 400 ^{o} C respectively, are shown in Figure 4.3. Well rectifying characteristics were observed in all the contacts, while higher annealing temperature led to higher reverse current. Ideality factor n and hole barrier height $q\phi_{bh}$ extracted from the linear part of the forward current are summarized in Table 4.1, where $q\phi_{be}$ was calculated according to the assumption that the sum of $q\phi_{be}$ and $q\phi_{bh}$ equals to germanium band gap (0.6634 eV). Although $q\phi_{be}$ less than 0.2 eV was obtained for all the diodes, it is noted that n value is significantly larger than unit. It implies the REM germanide/p-Ge (100) diodes are far from ideal and the current flows over REM germanide/p-Ge (100) interface is not fully determined by the thermionic emission theory. This probably due to the defects which formed during germanidation process and act as recombination centers or as intermediate states for trap-assisted tunnel currents, leading to a rising n value. Photocurrent measurements mentioned in Chapter 2 could be used to extract more accurate barrier height values.

Table 4.1 Ideality factor (n), ϕ_{bh} and ϕ_{be} for Er-Ge/p-Ge (100) and Yb-Ge/p-Ge (100) contacts after RTA at 350^{o} C and 400^{o} C, respectively.

	Er-Ge			Yb-Ge		
	n	ϕ_{bh} (eV)	ϕ_{be} (eV)	n	ϕ_{bh} (eV)	ϕ_{be} (eV)
350^{o} C	1.29	0.52	0.14	1.57	0.49	0.17
400^{o} C	1.55	0.51	0.15	1.71	0.48	0.18

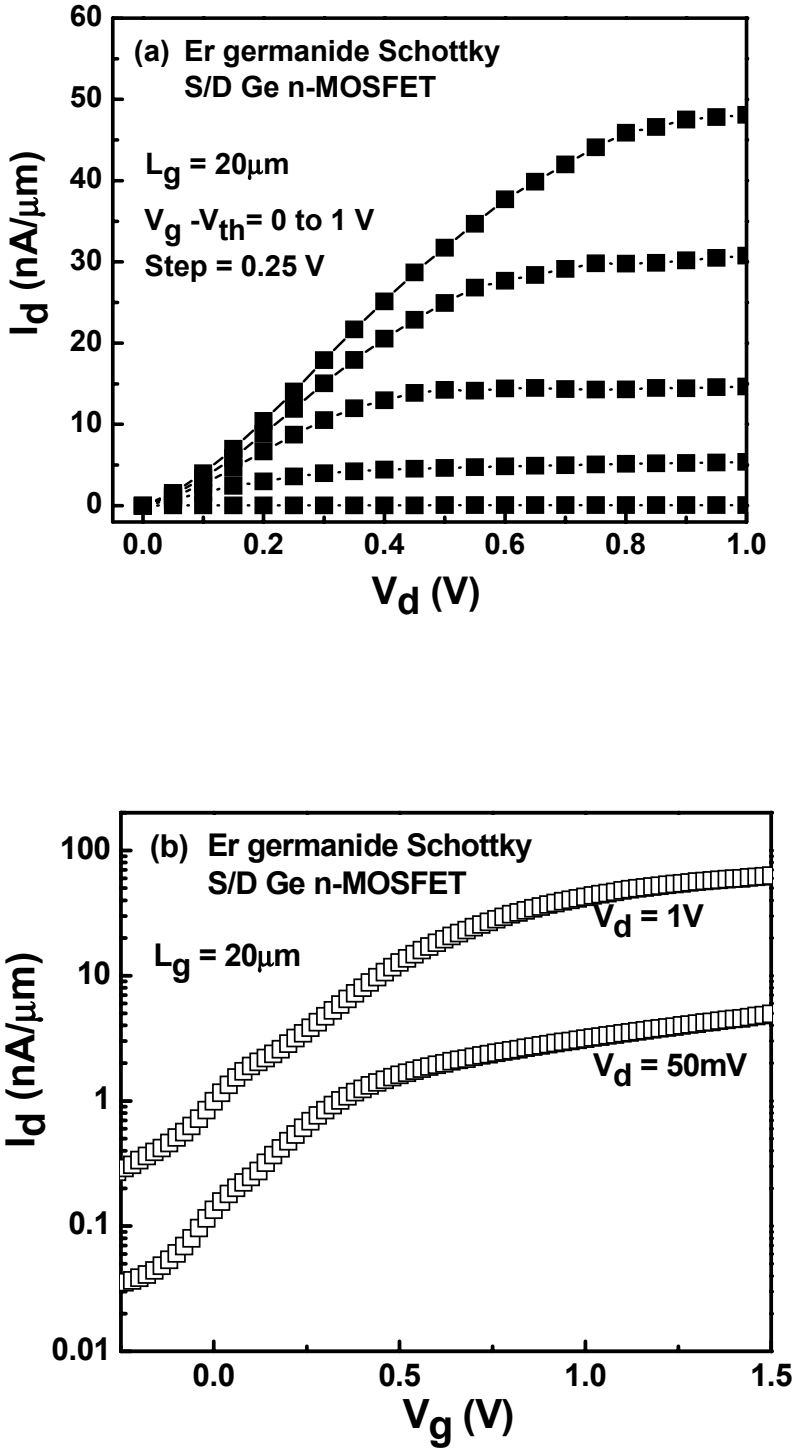


Figure 4.4 (a) output characteristics and (b) transfer characteristics of Er-germanide Schottky source/drain Ge n-MOSFETs.

Er-germanide Schottky source/drain Ge n-MOSFET with gate length of 20 μm and EOT of 3.1 nm was also demonstrated. Well-behaved I_d-V_d and I_d-V_g curves are shown in Figure 4.4. The relatively low drive current in Figure 4.4 (a) I_d-V_d curves exhibits high channel to source/drain resistance, which may come from limited Er-germanide source/drain extension towards the channel, and high Φ_{Be} due to Fermi level pinning between Er-germanide/p-Ge interfaces.

4.1.4 Conclusion

In conclusion, studies on Er- and Yb- germanides show that, although a resistivity value as low as of 27.2 and 26.8 μΩ•cm are obtained for Er- and Yb- germanides respectively, and well rectifying characteristics were also observed in Er- and Yb-germanide/p-Ge (100) contacts, the ideality factor values larger than unit implied high density of defects were formed during germanidation leading to higher *n* value. Er-germanide Schottky source/drain Ge n-MOSFET was also demonstrated with well-behaved output and transfer characteristics but a relatively low drive current.

4.2 Ni-Ge barrier height modulation by Sb segregation

4.2.1 Introduction

Previous studies on nickel and platinum germanides have shown that they are among the most promising candidates for Schottky source/drain Ge p-MOSFETs application [4.1] [4.2] and recently Ni- and Pt- germanide Schottky source/drain p-MOSFETs have been demonstrated with improved performance compared to conventional-doped source/drain Ge p-MOSFETs [4.3]-[4.5]. In contrast, studies on germanides for Ge n-MOSFETs so far have been mainly focused on rare earth elements such as Er and Yb with low metal work function [4.9] [4.10]. Inspired by the studies on low resistance contacts to n-Si [4.11] [4.12], which have shown effective Schottky barrier height reduction at NiSi/n-Si interface by introducing valence-mending adsorbates, in this work, by inserting an interfacial layer of Sb, we show that Ni-germanide is able to give both low resistivity and low electron barrier height, which make Ni-germanide with such modification a good ohmic contact material to n^+ source/drain regions as well as a promising Schottky source/drain candidate for Ge n-MOSFETs.

4.2.2 Experiment

The starting wafer is Sb doped (doping concentration is $6\times10^{14}cm^{-3}$) n-type Ge (100) as substrate. ~100 nm PECVD Si_3N_4 was deposited at 250° C for field isolation followed by lithography patterning and dry etching to define diode pattern. After dipping in diluted hydrofluoric acid ($HF:H_2O$=1:100 by volume) for one minute to remove residue Si_3N_4 and native germanium oxide in opened diode region, Sb and Ni were deposited by e-beam evaporator in sequence with Sb thickness of 0, 5 nm, 10 nm and 15 nm, respectively and Ni thickness of 30 nm for all samples. Then samples were rapid thermal annealed at 300° C and 400° C for one min respectively to form NiGe. Unreacted Ni was removed by diluted HNO_3 ($HNO_3:H_2O$=1:20). Finally ~100 nm Al was deposited by e-beam evaporator at the wafer backside to form ohmic contact for diode electrical measurement. The process flow and schematic structure are shown in Fig. 4.5, where as-deposited Sb is sandwiched at Ni and Ge interface. For the material study, Sb and Ni were deposited onto blank Ge wafer with the same thickness as diodes and also RTA annealed at 300° C and 400° C respectively. The germanide phases were identified with XRD, atoms profiles were examined with SIMS, the electrical sheet resistance was measured with the Van der Pauw method [4.13], and the contact electrical properties were characterized with an Agilent 4284A LCR semiconductor parameter analyzer.

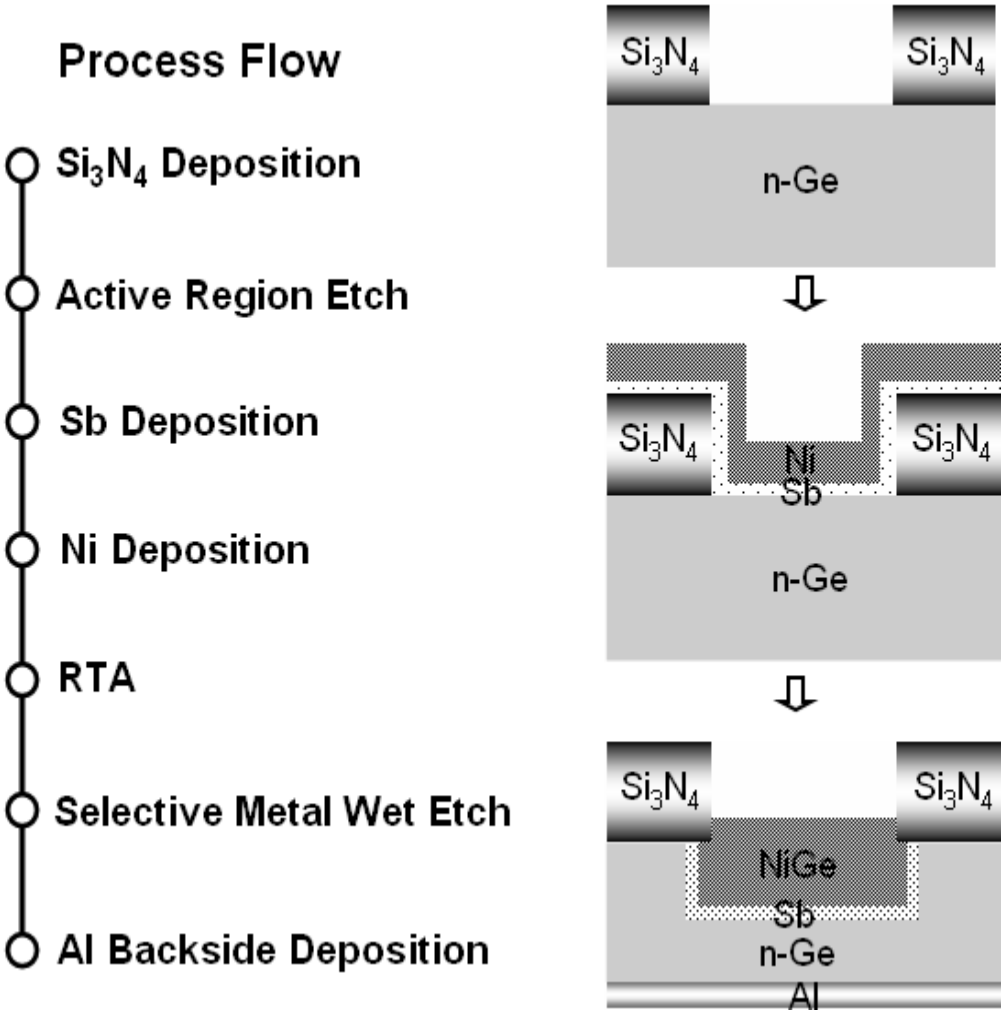


Figure 4.5 Process flow for fabricating low Schottky barrier height diodes using Sb segregation and device final structure after fabrication.

4.2.3 Result and discussion

The XRD results of NiGe formation with and without Sb inter-layer after RTA are shown in Figure 4.6. For samples without Sb interlayer, at 300^{o}C and 400^{o}C, Ni monogermanide phase is identified with a high intensity NiGe (111) peak, indicating a highly textured nature of the formed NiGe film with a (111) NiGe||Ge (100) orientation relationship [4.1]. By adding a 15nm Sb inter-layer, NiSb peaks are detected for the

sample annealed at 300° C however cannot be observed at 400° C. In reference [4.14], it is reported the NiSi formation at the present of Sb and also found that no NiSb was formed after RTA at 500° C and above, indicating Ni prefers reacting with Ge and Si compared to Sb at higher temperature. No degradation of NiGe structural properties induced by Sb interlayer are observed when anneal temperature increase to 400° C.

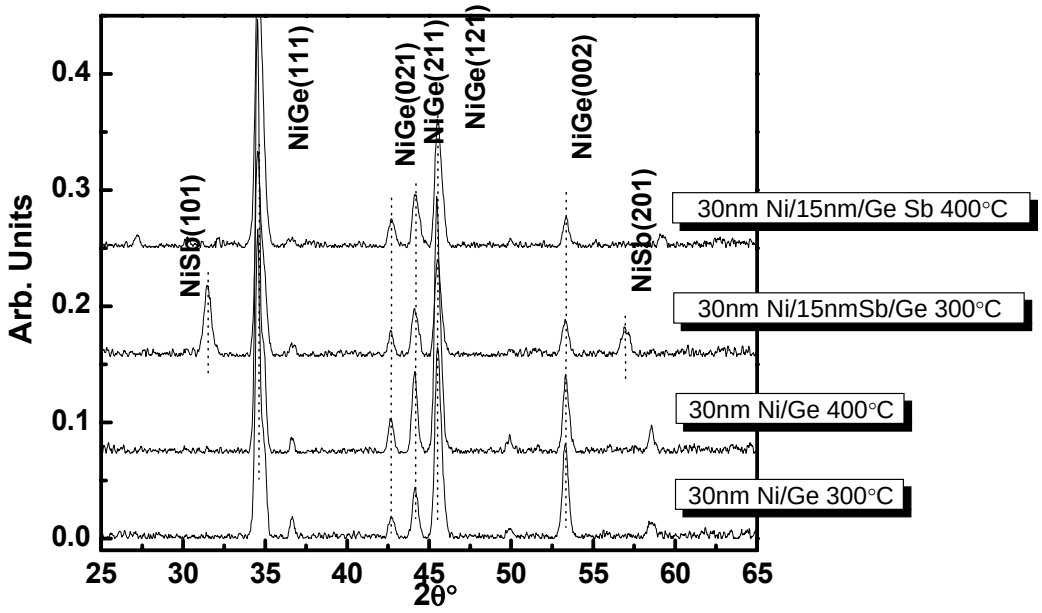


Figure 4.6 XRD profiles of 30 nm Ni/n-Ge (100) and 30 nm Ni/15 nm Sb/n-Ge (100) after RTA at 300° C and 400° C, respectively.

Figure 4.7 shows the SIMS depth profiles of Ni, Ge and Sb for the device with Sb interlayer thickness of 15 nm and annealed at 300° C and 400° C, respectively. Figure 4.7 (a) shows that the peak of Sb concentration is located near NiGe surface for the diode annealed at 300° C, and no peak of Sb concentration at NiGe/Ge interface is observed. According to the traditional Thermal Emission model [4.15], the electron barrier height

(ϕ_{be}) and ideality factor extracted from the room temperature $I-V$ characteristics of NiGe/n-Ge diodes annealed at 300^{o} C (Fig. 4.8 (a)), are within 0.528~0.525 eV and 1.04~1.14, respectively, regardless of the Sb thickness, indicating that after anneal at 300 ^{o}C, Sb cannot effectively reduce ϕ_{be} due to the failure of Sb segregation at NiGe/Ge interface. The formation of NiSb at 300^{o} C could be one of the reasons for the absence of Sb at NiGe/Ge interface.

On the contrary, significant amount of Sb is detected to be located at NiGe/Ge interface region for the diode annealed at 400^{o} C (Fig. 4.7 (b)), showing that the Sb segregation occurred at NiGe/Ge interface after anneal at 400^{o} C. $I-V$ characteristics in Figure 4.8 (b) shows that, for diodes annealed at 400^{o} C, the reverse current (I_r) significantly increases as the Sb thickness increased from 0 to 15 nm, showing the successful modulation of ϕ_{be} by the segregation of Sb. Due to the difficulties to extract low barrier height, the rectification ratio R_c is used to evaluate Schottky barrier height which is defined as the ratio of forward current I_f at forward voltage V_f of 0.5 V to reverse current I_r at reverse voltage V_r of -0.5 V applied to the diodes. It is known that higher effective Schottky barrier height leads to higher R_c value and R_c should be 1 for an ideal ohmic contact [4.15]. In Fig. 4.8 (c), it is observed that the R_c value can be widely modulated for the diodes annealed at 400^{o} C. R_c of 1.14 was obtained for the diode with Sb thickness of 15nm, indicating that ϕ_{be} can be greatly reduced and an almost ideal ohmic contact of NiGe/n-type Ge can be achieved, although an additional Sb layer will increase complexity and cost of the device fabrication process. The R_c value achieved in

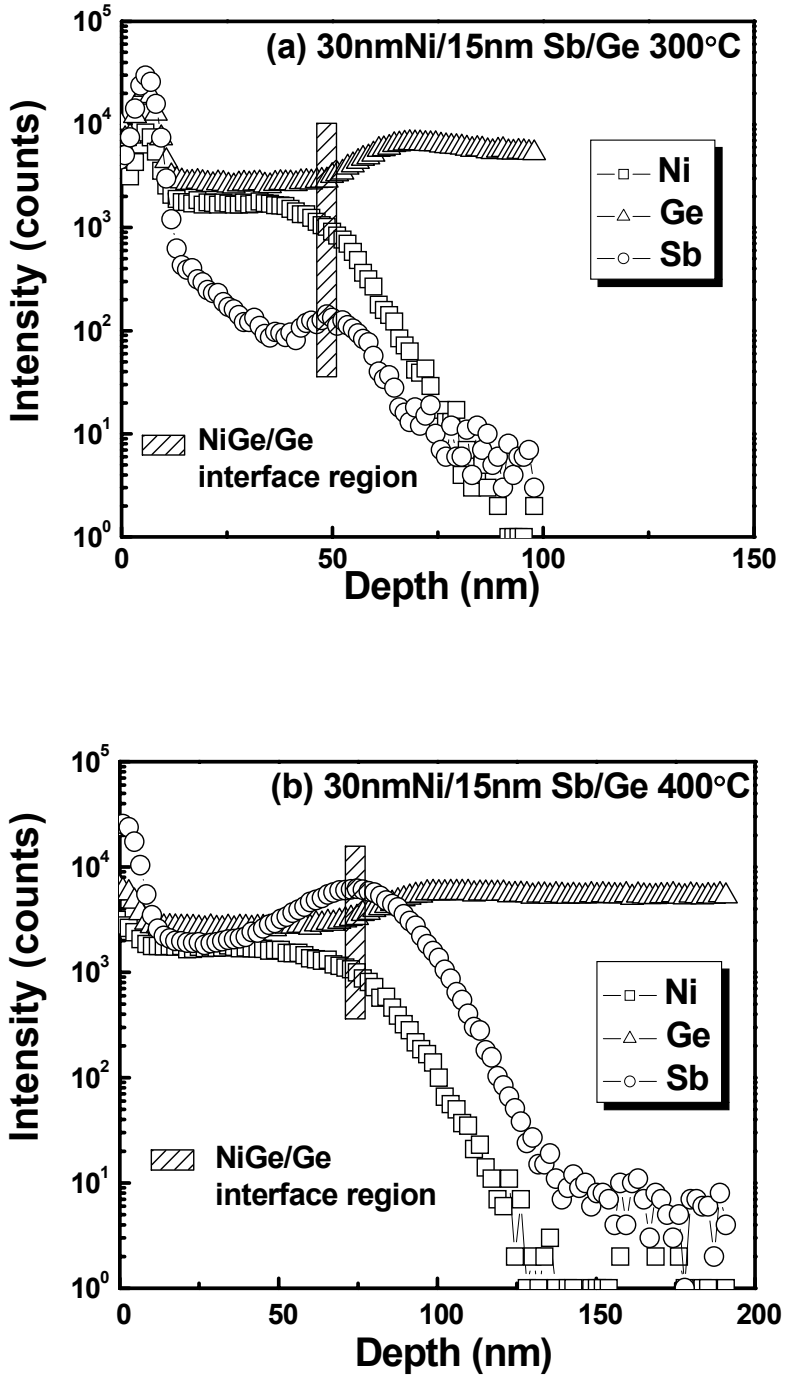
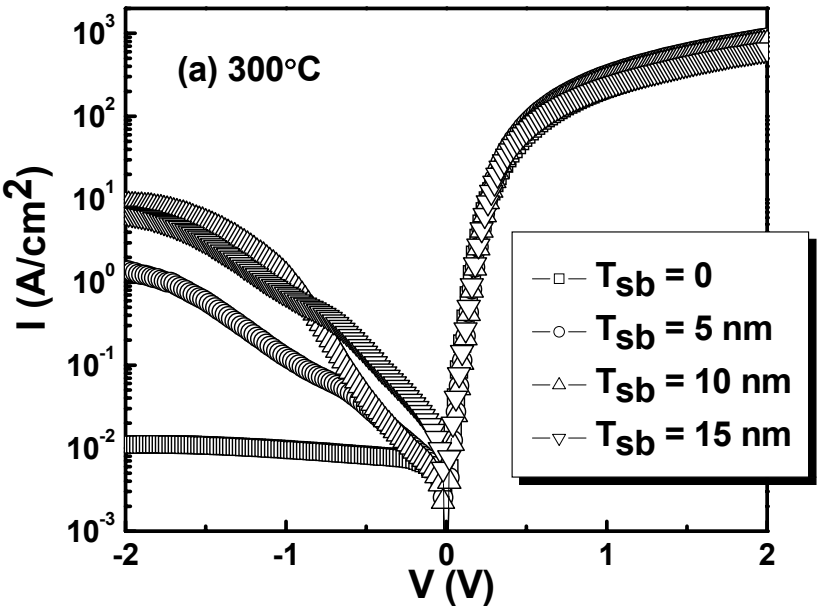
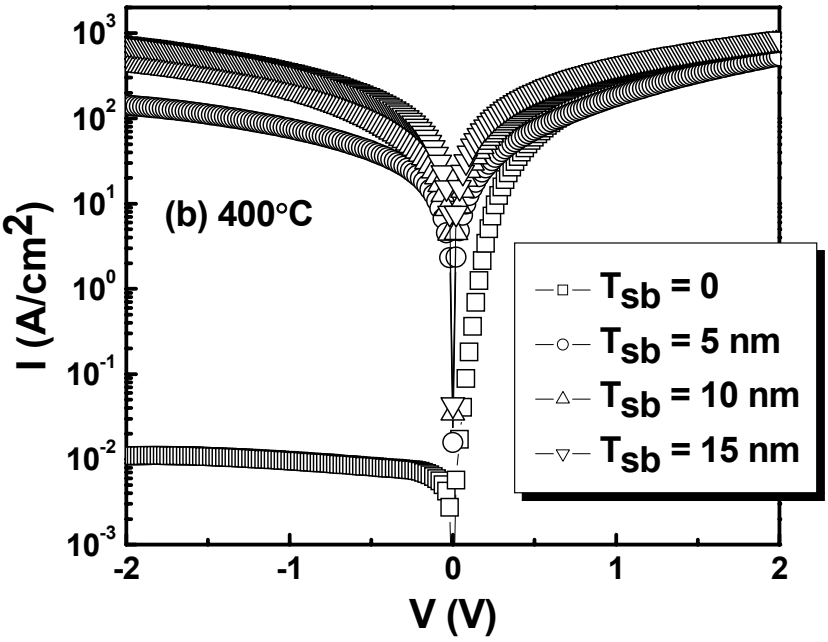


Figure 4.7 SIMS depth profile of Ni, Ge and Sb for the device with 30 nm Ni and 15 nm Sb interlayer annealed at (a) 300^{o} C and (b) 400^{o} C, respectively.


(a) 300°C
I (A/cm2)
V (V)
Tsb = 0
Tsb = 5 nm
Tsb = 10 nm
Tsb = 15 nm


(b) 400°C
I (A/cm2)
V (V)
Tsb = 0
Tsb = 5 nm
Tsb = 10 nm
Tsb = 15 nm

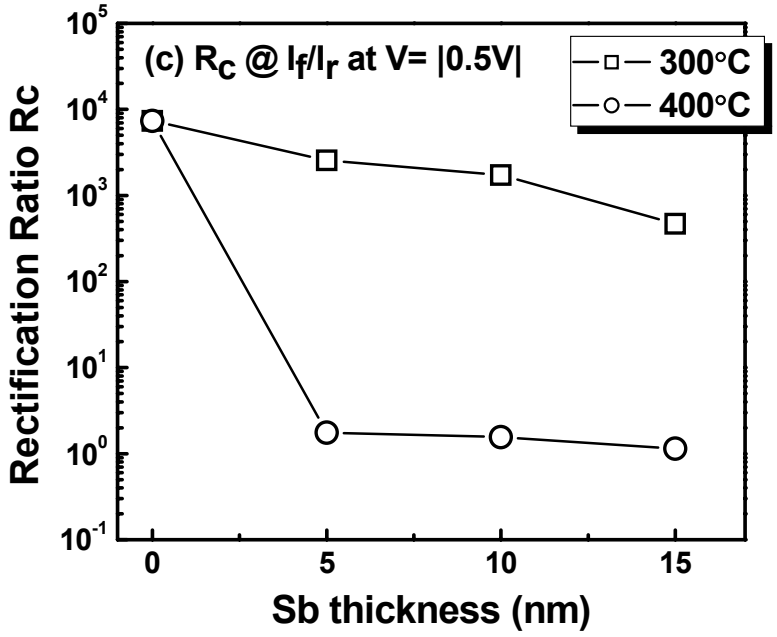


Figure 4.8 Current-voltage ($I-V$) characteristics at room temperature for NiGe/n-Ge (100) diodes with and without Sb interlayer annealed at (a) 300° C and (b) 400° C, respectively, and (c) rectification ratio R_c (I_f / I_r) as a function of Sb interlayer thickness (T_{sb}).

this work is significantly lower compared to the R_c value of ~ 100 in reference [4.16] where sulfur segregation is applied to lower ϕ_{be} of NiGe/n-Ge contact. It is also noticed that, different from the case in NiSi/n-Si contact [4.14], the ϕ_{be} modulation of NiGe/n-Ge contact is more dependent on anneal temperature, less dependent on Sb interlayer thickness.

Figure 4.9 shows the resistivity ρ measured from samples annealed at 400° C with different Sb inter-layer thickness. No obvious increase in Rs is observed for various Sb thickness, which means ϕ_{be} can be modified through Sb segregation while the low sheet resistivity properties of NiGe film (~ 17 μΩ•cm) still can be maintained, which is

slightly higher than the resistivity of NiSi (~ 15 μΩ•cm), the silicide material with the lowest resistivity reported [4.18] [4.19]. Although a resistivity value as low as ~19μΩ• cm has been reported for $ErGe_{1.5}$ [4.10], the REM germanides (silicides) have been known to form through a nucleation-controlled growth, usually leading to a rough germanide (silicide)/Ge (Si) interface, which makes REM germanides not suitable for n^+ source/drain contacts in spite of their low metal work function [4.18] [4.19]. From this point of view, because of the diffusion-controlled growth mechanism, which would lead to a smooth germanide/Ge interface, NiGe could be a more promising candidate for contact material to n^+ source/drain regions and Schottky source/drain material for Ge n-MOSFETs.

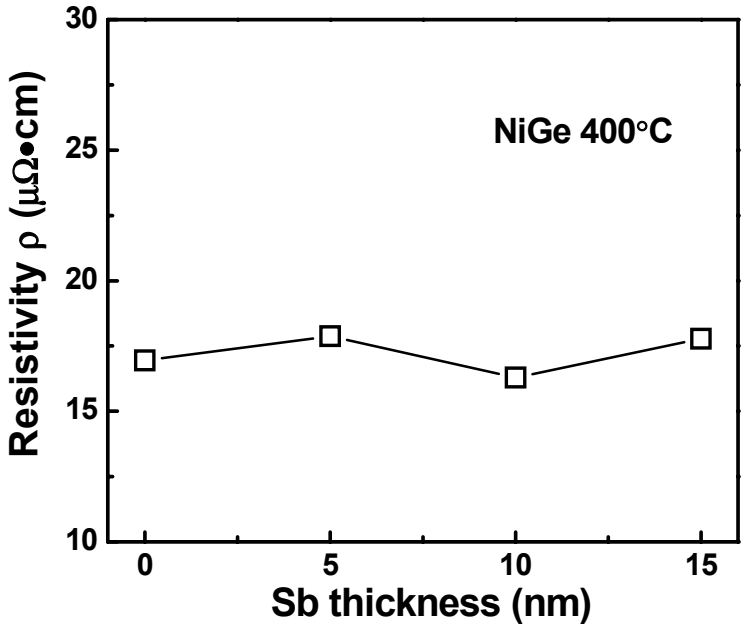


Figure 4.9 Electrical resistivity of Ni/n-Ge (100) as a function of Sb interlayer thickness after annealing at 400° C.

4.2.4 Conclusion

In conclusion, we demonstrated a novel method to effectively reduce ϕ_{be} of NiGe on n-type Ge (100) by inserting a Sb interlayer at Ni/Ge interface prior to RTA process. Sb segregation is found to be highly dependent on anneal temperature, while less dependent on Sb thickness. After anneal at 400^{o} C, an almost ideal ohmic contact of NiGe/n-type Ge with R_c and ρ as low as 1.14 and ~ 17 μΩ•cm was obtained, indicating that through ϕ_{be} modulation by adding a Sb interlayer, NiGe could be a good ohmic contact material to n^+ source/drain regions as well as a promising Schottky source/drain candidate for Ge n-MOSFETs.

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Chapter 5

Laser application in metal germanide formation as an alternative annealing method

5.1 Introduction

In previous chapters, all the studies were carried out by subjecting the whole device wafer to an elevated temperature using RTA to form metal germanide. A laser annealing process, as an alternative, can be adapted to form metal germanide with additional potential advantages, including control of tailored germanide profile with suppressed metal/Ge diffusion due to possible local selective heating of specific regions and reduced thermal budget, enhanced germanide/Ge interface quality with suppressed diffusion of impurities, and better process flexibility with low process cost [5.1]-[5.3]. Owing to theses unique characteristics, in recent years laser irradiation has received more and more attention in growing thin films of silicides [5.4]-[5.6], germanosilicides [5.7]-[5.9]. However, the report of studies on metal germanide formation by laser anneal is still rare in literature. In this chapter, a preliminary study on investigation of Pt-germanide formation by laser annealing process was carried out to explore the feasibility of using laser annealing as an alternative method in germanide source/drain formation. A well-behaved laser annealed Schottky source/drain Ge pMOSFET integrated with HfO_2/TaN gate stack is also demonstrated.

5.2 Experiment

5.2.1 Laser annealed Pt-germanide/n-type Ge (100) Schottky contacts

The Ge substrates used in this work were Sb-doped n-type (100) wafers with a resistivity of 2.0~3.2 Ω·cm. First, the substrates were dipped in diluted HF (H_2O: HF=100:1 by volume) for 5 min followed by de-ionized water to remove surface native oxide selectively from the substrate. Then the wafers were loaded into an E-beam evaporator with a chamber base pressure at 10^{-6} mTorr where ~30 nm Pt was deposited to form Pt dots by a shadow mask with dots diameter of 1 mm. A KrF excimer laser with a wavelength of 248 nm was used to irradiate the samples to form germanide at a laser fluence from 0.10 to 0.22 J/cm^2 with pulse number from 1 (1 p) to 10 pulses (10 p). The laser pulses were produced at a repetition frequency of 1 Hz and pulse duration of 23 ns. SEM, HRTEM and Bruker D8 GADDS XRD were applied to examine surface morphology, interface quality and crystallinity of Pt-Ge after the laser annealing, respectively, and the Schottky contacts were characterized by a Hewlett-Packard 4156A semiconductor parameter analyzer.

5.2.2 Laser annealed Pt-germanide Schottky source/drain Ge p-MOSFET integrated with TaN/HfO_2 gate stack

The self-aligned fabrication of Pt-germanide Schottky source/drain p-MOSFETs also uses Sb-doped n-type (100) Ge wafers with a resistivity of 2.0~3.2 Ω·cm as starting substrates. After removal of surface native oxide by dipping the substrate into diluted HF for 5 min, Ge substrate received plasma PH_3 treatment to improve interface quality [5.10], followed by *in situ* metal organic chemical vapor deposition of HfO_2 as gate dielectric

and post-deposition-annealing at 400° C. 100 nm TaN was deposited by reactive sputtering as gate electrode. After gate patterning, ~30 nm Si_3N_4 was deposited by plasma enhanced chemical vapor deposition at 250° C and formed the spacer by the reactive ion etching. ~30 nm Pt was deposited by ebeam evaporator and then samples were irradiated at a laser fluence of 0.14 J/cm^2 and 1 pulse. A schematic sketch of the laser annealing experimental setup and transistor structure is illustrated in Fig. 5.1. In laser annealing process, the laser light generated by the KrF excimer laser is reflected by a mirror and focused on the sample by a lens. The size of the light spot on sample is about 4×5 mm. The sample was placed on a stage that can move in vertical direction. By fixing the laser energy and only changing samples position in vertical direction, laser focused area on sample was also varying, resulting in different laser fluence.

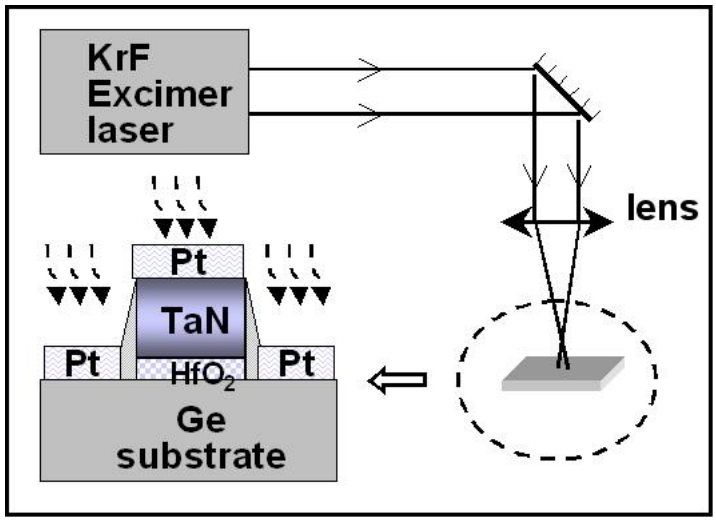


Figure 5.1. A schematic sketch of the laser annealing experimental setup and transistor structure.

Unreacted Pt was removed by reactive ion etching process with Cl_2 gas. Finally, the backside ohmic contact was formed by 100nm Al deposited by the E-beam

evaporator. The MOSFET performance was characterized by a Hewlett-Packard 4156A and Agilent 4284A LCR semiconductor parameter analyzer.

5.3 Results and discussion

5.3.1 Electrical and material characterization of laser annealed Pt-germanide/n-type Ge (100) Schottky contacts

In order to evaluate the impact of laser annealing condition on sample surface morphology, SEM was used to examine Pt-Ge samples irradiated with laser fluence from 0.10 to 0.22 J/cm^2 with different pulse, and results are shown in Fig. 5.2. It was observed that the Pt-germanide films remain smooth and uniform with laser fluence up to 0.18 J/cm^2 for 1 pulse and 10 pulses, as shown in Fig. 5.2 (a), (b) and (c), which are similar with the morphology of Pt-germanide formed by an optimized RTA at 400^o C (Fig. 5.2 (f)) [5.11]. However, an apparent agglomeration phenomenon was observed on sample surface at a laser fluence of 0.20 J/cm^2 with even 1 pulse. Furthermore, it seems that a higher fluence of 0.22 J/cm^2 with 1 pulse results in a more serious agglomeration (see Fig. 5.2 (c) and (d)), which means the upper limit for Pt germanide by laser annealing should not exceed 0.20 J/cm^2.

The crystallinity of Pt-Ge films after laser annealing was analyzed by XRD as shown in Fig. 5.3. For the irradiation fluence of 0.10 J/cm^2, there is no germanide peak but Pt peak detected at 1 pulse. However, both Pt-rich germanide (such as Pt_3Ge_2) peaks and Pt peak can be observed as pulse number increases to 10, which means reaction

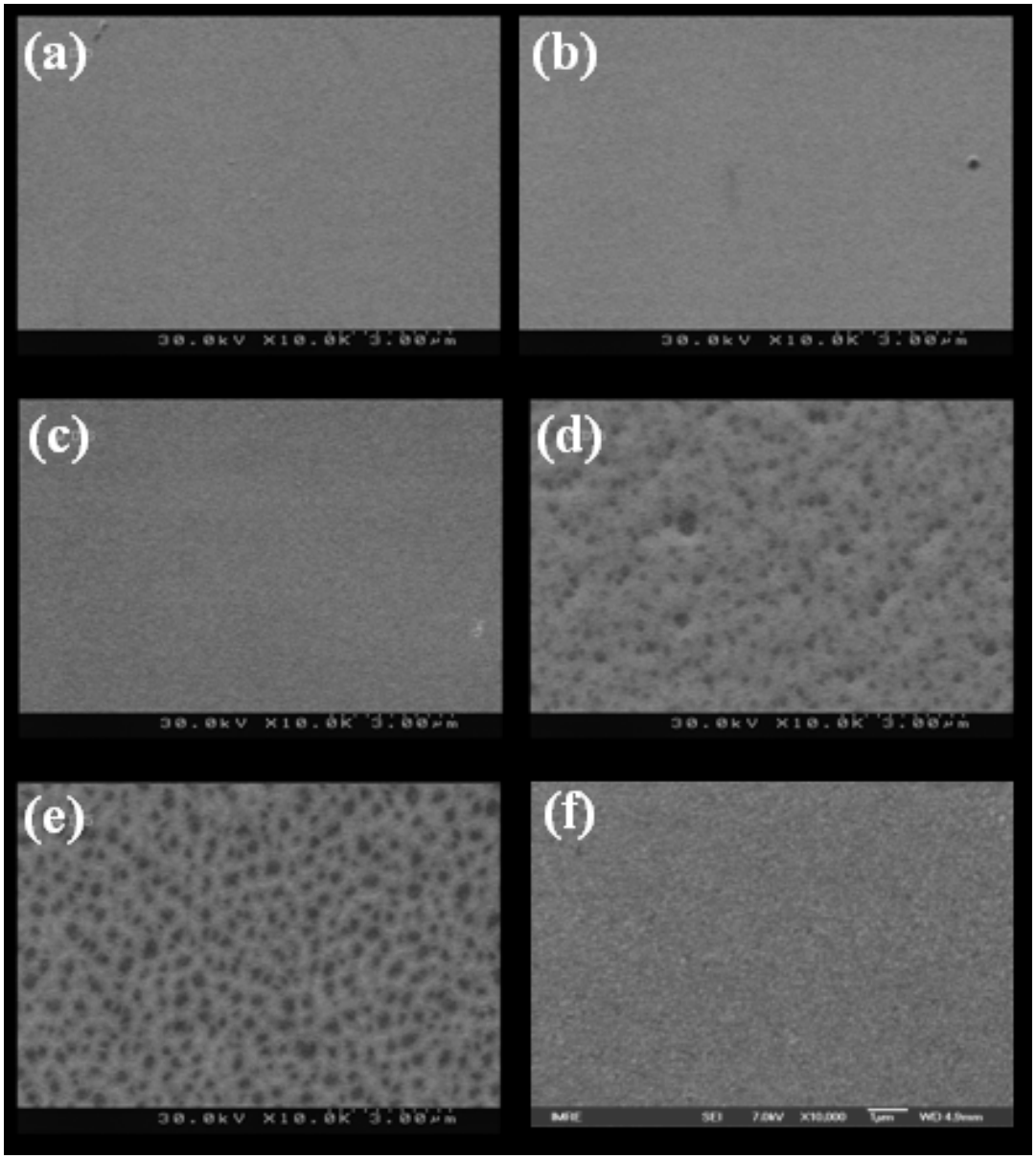
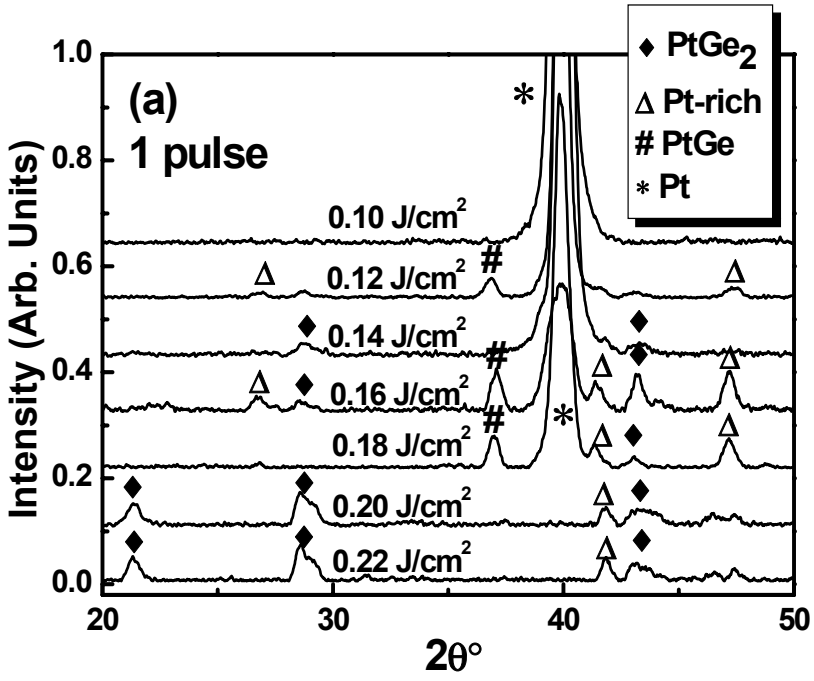


Figure 5.2. SEM images of Pt/Ge by laser annealing at (a) 0.10 J/cm^2 for 1 pulse, (b) 0.18 J/cm^2 for 1 pulse, (c) 0.18 J/cm^2 for 10 pulses, (d) 0.20 J/cm^2 for 1 pulse, (e) 0.22 J/cm^2 for 1 pulse and by RTA at (f) 400^o C.

between Pt and Ge can proceed at laser fluence as low as 0.10 J/cm^2 with sufficient pulses. For an irradiation with a higher fluence from 0.12 to 0.18 J/cm^2, besides the Pt peaks, there is co-existence of Pt-rich germanide and $PtGe_2$ in the films at 1 pulse. When the irradiation was increased to 10 pulses, relatively weakening of the Pt-rich germanide

peaks as well as stronger $PtGe_2$ peaks were observed which implies that a portion of Pt-rich germanide has transformed into $PtGe_2$ phase. The co-existence of germanide can be attributed to the rapid melting and re-solidification processes that happened in the film during pulse laser annealing. Different from RTA process, the inter-diffusion of metal and Ge and redistribution of metal atoms are greatly suppressed during pulse irradiation, which result in a film with varying Pt-Ge concentration starting with Ge rich at the Pt-Ge interface, to Pt rich at the film surface. For irradiation at fluence of 0.20 or 0.22 J/cm^2 with 1 pulse, there is no more Pt peak detected, and the $PtGe_2$ peaks become even stronger while Pt-rich germanide peaks become weaker compared to the spectra at lower fluence in Fig. 5.3 (a). This observation implies that Pt film is completely consumed at fluence of 0.20 J/cm^2, and higher irradiation fluence will cause more portion of Pt-rich germanide to be transformed. Therefore, it is believed that fluence of 0.20 J/cm^2 is sufficient to cause the Pt film melted and fully reactive with Ge substrate, which also results in the serious



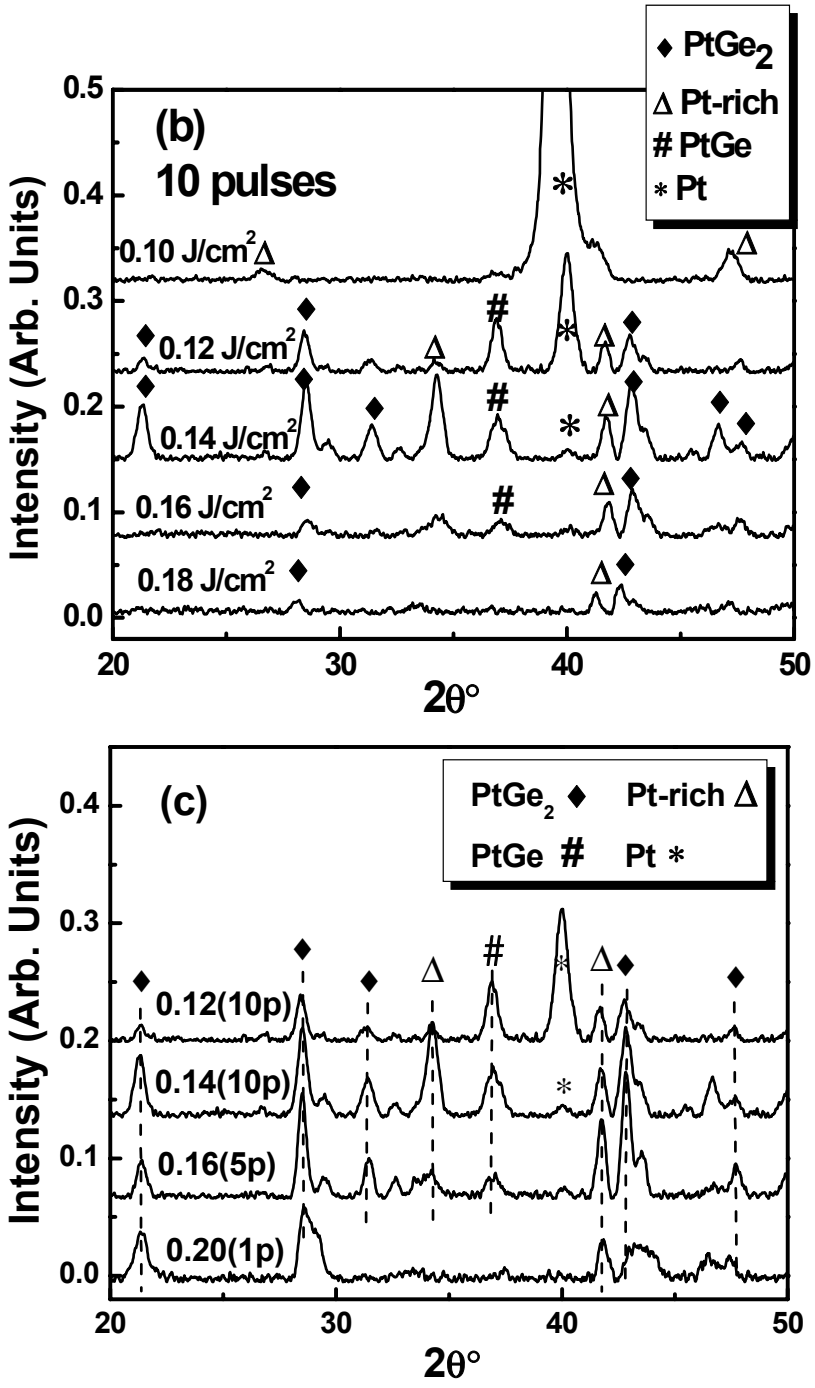


Figure 5.3. XRD results of Pt germanide formed by laser annealing at laser fluence of (a) 0.10~0.22 J/cm^2 for 1 pulse, (b) 0.10~0.18 J/cm^2 for 10 pulses, and (c) 0.12 J/cm^2 for 10 pulses, 0.14 J/cm^2 for 10 pulses, 0.16 J/cm^2 for 5 pulses and 0.20 J/cm^2 for 1 pulse, respectively.

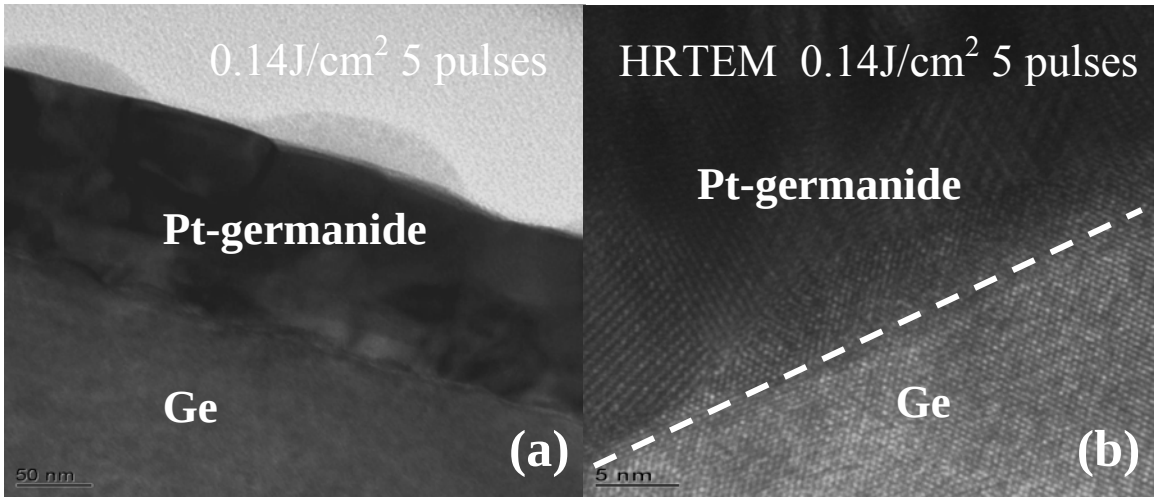


Figure 5.4. (a) TEM and (b) high resolution TEM pictures of Pt-germanide formed by laser annealing at 0.14 J/cm^2 for 5 pulses.

agglomeration surface morphology observed in Fig. 5.2 (d) and (e). Unlike the Pt germanide formed by RTA, by which germanide phase formation is determined by temperature [5.12]-[5.14], the same phase can be obtained at various laser fluence at specific pulse number, as shown in Fig. 5.3 (c).

TEM and HRTEM analysis were also carried out to study the Pt-germanide and Ge interface after laser annealing. As shown in Fig. 5.4 (a), uniform Pt-germanide films are formed with sharp interface with the Ge substrates. Epitaxial growth of Pt-germanide on Ge substrate is also observed as shown in Fig. 5.4 (b).

The Schottky contact characteristics for Pt-germanide/n-type Ge (100) are listed in Table 5.1. Barrier heights for electron ($q\phi_{be}$) were extracted according to the Eq. (2.8) where the Richardson constant $A^* = 50 A cm^{-2} K^{-2}$ for n-type Ge (100) [5.13] [5.16], and I_s the forward saturation current fitting from diode forward current. As can be seen, almost identical $q\phi_{be}$ values of 0.52 ~ 0.54 eV, equivalent to hole barrier height of 0.12 ~ 0.14 eV, were obtained for all the Pt-germanide/n-type Ge samples annealed at laser

fluence of 0.10 to 0.18 J/cm^2 for 1 to 10 pulses. The behavior of constant barrier height over a wide fluence range is similar to Pt-germanide/n-Ge contacts formed by RTA [5.13] [5.14].

Table 5.1. Calculated effective electron barrier height of Pt-germanide/n-type Ge (100) contacts annealed at different laser fluence and pulse numbers.

Fluence (J/cm^2)	Pulse Num.	$q\phi_{be}$ (eV)
0.10	10	0.54
0.12	1	0.54
	5	0.54
	10	0.54
0.14	1	0.54
	5	0.52
	10	0.53
0.16	1	0.52
	5	0.53
	10	0.54
0.18	1	0.54
	5	0.52
	10	0.53

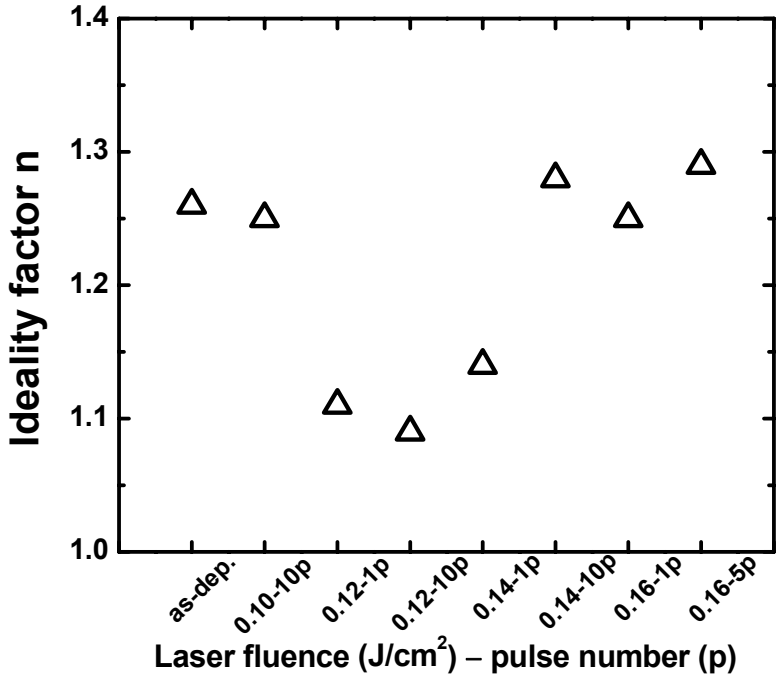


Figure 5.5. Ideality factor n value of Pt-germanide/ n-type Ge (100) contacts annealed at laser fluence from 0.10 to 0.16 J/cm^2 with different pulse number, as well as as-deposited Pt/n-type Ge (100) contact.

Figure 5.5 shows the effect of laser fluence and pulse number on the ideality factor n, which represents the dependence of barrier height on voltage applied on a Schottky diode. n is near unity for well-behaved Schottky diodes and can be obtained from current-voltage equation Eq. (2.7) when $V >> KT/q$, n can be extracted from the slope of $\ln[I/(1-\exp(-qV/KT))]$ vs. V. An n value larger than 1.2 was obtained for as-deposited Pt/n-type Ge contacts, which can be attributed to the presence of germanium native oxide at Pt/Ge interface. For Pt/Ge structures annealed at fluence of 0.12~0.14 J/cm^2, the n values decrease to ~1.1 which implies good Pt-germanide/n-Ge Schottky

contacts are formed. As expected, a uniform Pt-germanide film with sharp interface on the Ge substrate was observed for sample annealed at 0.14 J/cm^2 for 1 pulse as shown in Fig. 5.4. However, a further increase of laser fluence and pulse number leads to the n value increases again, which is probably due to the increased recombination in the depletion region induced by higher irradiation energy.

5.3.2 Electrical characterization of laser annealed Pt-germanide Schottky S/D Ge p-MOSFET

The laser annealing condition of 0.14 J/cm^2 for 1 pulse was applied for the formation of Pt-germanide Schottky source/drain of Ge pMOSFETs with TaN/HfO_2 gate stack. Figure 5.6 shows the excellent $C-V$ characteristics of Ge pMOSFET gate stack after laser annealing. The symbols represent the high-frequency $C-V$ characteristics measured at 1MHz. An EOT of 3.8 nm considering quantum effect and a flat band voltage (V_{FB}) of –0.5 V were extracted. The gate leakage current as a function of gate voltage, as shown in the inset of Fig. 5.6, exhibits a low leakage current of 2×10^{-5} A/cm^2 at $|V_g - V_{FB}| = 1$ V.

Furthermore, well-behaved output ($I_d - V_d$) and transfer characteristics ($I_d - V_g$), of laser annealed Pt-germanide Schottky source/drain Ge pMOSFET with channel width/length = 400/10 μm were obtained as shown in Fig. 5.7. A relatively low drive current was observed as compared to RTA samples in our previous study [5.11]. This can

be attributed to a higher source/drain to channel series resistance associated with the laser annealed samples, since the lateral diffusion of germanide from source/drain towards channel region during laser annealing (in nanoseconds) is far more limited than that during RTA (in minutes). A thinner spacer is expected to reduce the series resistance therefore improve the drive current.

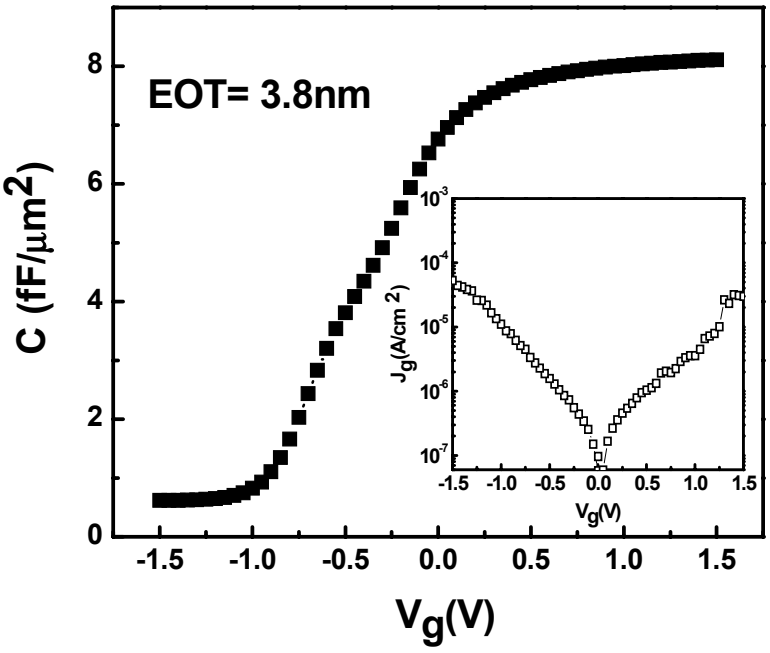


Figure 5.6. Capacitance-voltage ($C-V$) and current-voltage ($I-V$) characteristics of TaN/HfO_2/Ge gate stack of Ge p-MOSFET with laser annealing Pt-germanide Schottky source/drain.

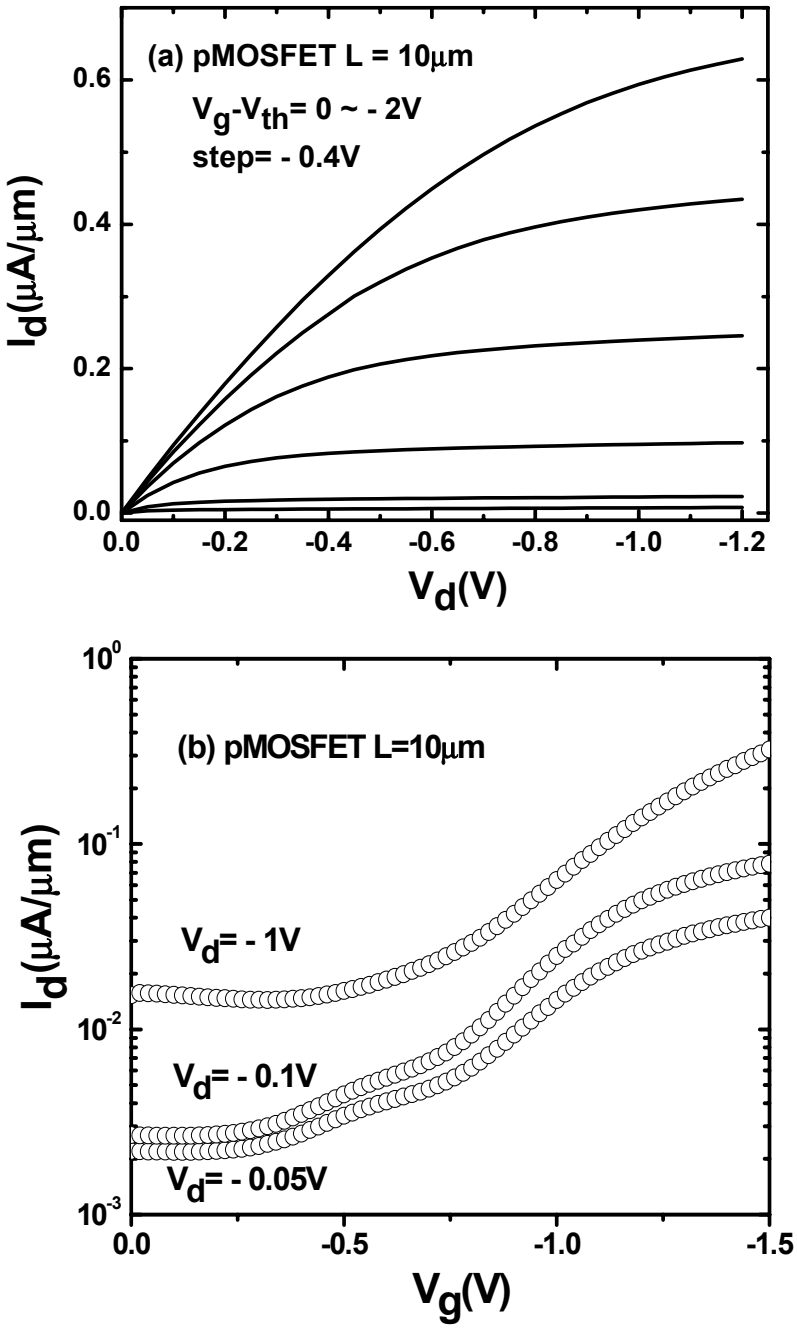


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Figure 5.7. Output (a) and transfer (b) characteristics of Ge p-MOSFET with laser annealing Pt-germanide Schottky source/drain.

5.4 Conclusion

We have studied the formation and characteristics of Pt-germanide films formed on n-Ge (100) through solid-state reaction between Pt and Ge via pulsed laser annealing. For laser fluence varied from 0.10 to 0.18 J/cm^2 for 1 to 10 pulses, smooth and uniform Pt-germanide film surfaces and co-existence of Pt, $PtGe_2$ and Pt-rich germanide in the films were observed; almost identical effective $q\phi_{be}$ of 0.52~0.54 eV for Pt-germanide/Ge Schottky contacts were also achieved. A Pt-germanide Schottky source/drain p-MOSFET integrated with HfO_2/TaN gate stack and source/drain formed at 0.14 J/cm^2 for 1 pulse gives a V_{FB} of – 0.5 V, a low leakage current of 2×10^{-5} A/cm^2 at $|V_g - V_{FB}| = 1$ V and a well-behaved output and transfer characteristics.

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Chapter 6

Conclusion

As the closing chapter of the thesis, first, summary of this project discussed in previous chapters will be made. Then recommendations for future studies will be suggested.

6.1 Conclusion

As CMOS transistors scale beyond 45 nm technology node, numerous "Grand Challenges" for the semiconductor manufacturing industry are becoming significant barriers. Many requirements forecasted by ITRS for the next 1-15 years have "no known solution," in some cases within the next two years [6.1]. This predicament is forcing the industry to consider alternative non-conventional CMOS architectures and integration of new and novel performance enhancing materials. Metal Schottky source/drain germanium MOSFET integrated with high-k gate dielectric and metal gate provides numerous and broad benefits, which are promising solution to the industry's roadmap and technology challenges in both the near and long term. However, the replacement of channel material from Si to Ge induces various material and process integration issues; few studies have been done on the material and electrical properties of metal germanide and the relevant knowledge is rather exiguous compared to highly integration of silicide contacts in modern technology. This project has attempted to investigate the material and

electrical properties of metal germanide/Ge contacts as well as the feasibility of integration of germanide Schottky source/drain with Ge channel and high-k dielectric and metal gate.

Studies on Schottky contact properties of Ni- & Pt- germanides on n-type Ge show that both materials provide promising merits for p-MOSFET; low effective hole barrier height (0.08 and 0.04 eV for Ni- and Pt- germanide, respectively), low resistance (16 μΩ·cm and 25 μΩ·cm for Ni- and Pt- germanide, respectively), uniform epitaxial germanide film growth and abrupt junction with Ge. While agglomeration happens in NiGe film when annealed at 500° C, especially for thinner NiGe film, $PtGe_2$ film maintains smooth morphology and shows better thermal stability than NiGe.

Ge Schottky source/drain p-MOSFETs using Ni- and Pt- germanide are demonstrated on n-Ge-substrate with CVD-HfO_2/TaN gate stack. The highest processing temperature is only 400° C that eliminates the thermal stability concern of high-k dielectric/Ge stack [6.2] [6.3]. Ni- and Pt- germanide Schottky junction at source/drain show improved forward and reverse current, compared to conventional B-doped Ge-MOSFET. Higher drive current and lower off-state current are obtained from Pt-germanide Ge p-MOSFET than those of Ni-germanide Ge p-MOSFET and conventional doped source/drain Ge-pMOSFET.

The studies on germanide with low electron barrier height on Ge for Ge n-MOSFET application were focused on two categories. One is rare-earth-metal (Er and Yb) germanide with low metal work function; the other is, engineering of NiGe barrier height to n-Ge by using a valence mending adsorbate, Sb, segregation during Ni germanidation. Studies show that, although resistivity value as low as of 27.2 and 26.8 μΩ•cm are

obtained for Er and Yb germanide respectively, and well rectifying characteristics were also observed in Er and Yb germanide/p-Ge (100) contacts, the high ideality factor values ($n > 1.2$) implies high density of defects were formed during germanidation. Er-germanide Schottky source/drain Ge n-MOSFET was also demonstrated with well-behaved output and transfer characteristics but a relatively low drive current.

On the other hand, we demonstrated a novel method to effectively reduce ϕ_{Be} of NiGe on n-type Ge (100) by inserting a Sb interlayer at Ni/Ge interface prior to germanidation process. Sb segregation is found to be highly dependent on anneal temperature, while less dependent on Sb thickness. An almost ideal ohmic contact of NiGe/n-type Ge with R_c and ρ as low as 1.14 and $\sim 17\ \mu\Omega\bullet$cm was obtained, indicating that through ϕ_{Be} modulation by adding a Sb interlayer, NiGe could be a good ohmic contact material to n^+ source/drain regions as well as a promising Schottky source/drain candidate for Ge n-MOSFETs.

As an alternative, the formation and characteristics of Pt-germanide films formed via pulsed laser annealing are also studied. Smooth and uniform Pt-germanide film was achieved. Pt-germanide/Ge Schottky contacts annealed at different laser fluence show almost identical effective electron barrier height of 0.52~0.54 eV, equivalent to hole barrier height as low as 0.12~0.14 eV. A Pt-germanide Schottky source/drain p-MOSFET integrated with HfO_2/TaN gate stack and source/drain formed at 0.14 J/cm^2 for 1 pulse gives a V_{FB} of –0.5 V, a low leakage current of 2×10^{-5} A/cm^2 at $|Vg-V_{FB}|$= 1V and a well-behaved output and transfer characteristics.

6.2 Suggestions for future work

This thesis explored the potential of germanide Schottky source/drain Ge MOSFET integrated with high-k dielectric and metal gate. Although many positive results have been published so far, some issues need to be further investigated and understood for device performance improvement and implementation in the future.

1) Metal Schottky source/drain Ge p-MOSFET

In despite of good thermal stability and low hole barrier height of Pt-germanide, one weak point of Pt-germanide to be integrated with CMOS process is the difficulty in Pt etching. In Chapter 2, we have proposed a robust self-aligned Pt-germanide process by demonstration a surface plasma nitridation treatment on Pt-germanide that is able to effectively protect Pt-germanide from being attacked during aqua regia wet etching process. This nitridation treatment condition can be further optimized and a robust self-aligned selective wet etching process for Pt-germanide Schottky source/drain MOSFETs formation could be realized.

2) Metal Schottky source/drain Ge n-MOSFET

Although REM germanides/p-Ge diodes exhibit rectifying Schottky properties, the performance of Ge n-MOSFET with REM germanide Schottky source/drain is still quite disappointing and requires further study in future. Dopant segregation provides a promising way to effectively reduce electron barrier height for Ge n-MOSFET application. Although dopant segregation has been proven successfully modifying silicide/Si barrier height and Schottky source/drain Si n-MOSFET has been demonstrated

in this way, little information related to dopant segregation in Ge is reported so far, which should be more intensively studied.

3) Ge Schottky MOSFETs on GOI technology

Schottky source/drain integrated with high-k dielectric and metal gate on Ge substrate has been demonstrated to alleviate the challenges faced with channel length scale down with demonstrated MOSFETs. However, for better control of short channel effects for the sub-tenth nm technology, Schottky MOSFET fabricated on GOI (germanium on insulator) substrate should be also investigated, which requires creative studies in many aspects including the substrate fabrication and process integration issues.

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Appendix I: List of Publications

Journal papers

[1] Rui Li, Sungjoo Lee, Minghui Hong, Dongzhi Chi, Dim-Lee Kwong, "Pt-germanide formed by laser annealing and its application for Schottky Source/Drain MOSFET integrated with TaN/CVD-HfO_2/Ge gate stack" Japanese Journal of Applied Physics (accepted).

[2] Rui Li, Sungjoo Lee, Haibiao Yao, Dongzhi Chi, Mingbin Yu, Dim-Lee Kwong, "Germanium p-MOSFETs with Pt-Germanide Schottky Source/Drain, HfO_2 Gate Dielectric and TaN Gate Electrode" IEEE Electron Device Letters, vol. 27, No. 6, 476 (2006).

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Conference papers

[1] Rui Li, S. J. Lee, D. Z. Chi, M. H. Hong and D. –L. Kwong, "Pt-germanide Formed by Laser Annealing and Its Application for Schottky Source/Drain MOSFET Integrated with TaN/CVD-HfO_2/Ge Gate Stack," Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 36-37.

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