STRAIN ENGINEERING FOR ENHANCED P-CHANNEL FIELD EFFECT TRANSISTOR PERFORMANCE

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Abstract

Metal-oxide-semiconductor field effect transistors (MOSFETs) are continuously scaled down in the past four decades to increase its speed and performance. However, due to short channel effects and reliability issues, further scaling faces immerse challenges in achieving the aggressive on-off current target for high performance logic applications. Alternative approaches such as new device structures and new materials are being actively explored to extend the limits of transistor performance improvement. One promising approach is to enhance the carrier mobility through strain engineering.

In this work, we focus on the strain engineering related issues for p-channel transistors.

To enhance the level of strain in p-channel field effect transistors (p-FETs), a novel method of increasing Germanium content in a p-FET with SiGe source/drain (S/D) stressor is demonstrated. The process involves laser-induced local melting and intermixing of a Ge layer with an underlying $Si_{0.8}Ge_{0.2}$ S/D region, leading to a graded SiGe S/D stressor with significant increase in the peak Ge content. Various laser fluences were investigated for the laser annealing process. The process is then successfully integrated in a device fabrication flow, forming strained silicon-on-insulator p-FETs with high Ge content in SiGe S/D. A drive current enhancement of ~14% was achieved with this process, as compared to a strained p-FET with $Si_{0.8}Ge_{0.2}$ S/D p-FETs with similar control of short channel effects.

Furthermore, a new device structure employing a reverse embedded Silicon-Carbon (Si:C) stressor under the transistor channel is also investigated. As the Si:C was formed in the early stage of transistor fabrication, there are concerns such as the potential C precipitation and relaxation of Si:C during subsequent high temperature

processes. These concerns are addressed through material studies using high resolution x-ray diffraction (HRXRD), and micro Raman analysis. Device fabrication process was also discussed with the focus on key process steps, challenges and solutions. For the device performance, due to the defects at the Si-Si:C heterojunction interface caused by poor epitaxy quality and/or implantation and annealing damages, devices with Si:C stressor below the channel currently has a high source to drain leakage current. Proposals on further work to improve the device performance are covered.

In addition, issues related to the undesirable tensile stress caused by high Boron doping in p-FETs S/D is also discussed in the thesis work. Due to the smaller covalent bond radius of boron than silicon, when highly activated boron formed in S/D or S/D extension regions in a p-channel transistor, it can cause local lattice contraction of Si S/D, and introduce undesirable tensile channel strain in p-FET channel. Incorporation of Sn was investigated as a strain compensation implant. HRXRD measurement after the laser annealing confirms that the tensile strain caused by supersaturated boron was relieved by tin co-implantation. In addition, this Sn strain compensation implant was also found to enhance boron's thermal stability, and improves the retention of highly-activated and metastable boron during subsequent thermal anneals through a local strain compensation effect. The physics behind this enhanced thermal stability was explained.

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List of Symbols

Symbol	Description	Unit
a_{Si}	Lattice constant of silicon	Å
a_{Ge}	Lattice constant of germanium	Å
a_{SiGe}	Lattice constant of silicon-germanium	Å
C_{ox}	Oxide capacitance	F
m^*	Conductivity effective mass	kg
m_0	Free electron mass (= 9.1 x 10^{-31} kg)	kg
m_l	Longitudinal effective electron mass	kg
m_t	Transverse effective electron mass	kg
ε_{xx}	Strain component in *x* or [110] channel direction	none
ε_{yy}	Strain component in *y* or [-110] channel direction	none
ε_{zz}	Strain component in *z* or out-of-plane direction	none
G_m	Transconductance	S
I_D	Drain current (per unit width)	A/µm
I_S	Source current (per unit width)	A/µm
I_{Dsat}	Saturation drain current (per unit width)	A/µm
$I_{D,lin}$	Linear drain current (per unit width)	A/µm
I_{OFF}	Off-state current (per unit width)	A/µm
L_G	Gate length	m
R_{SD}	Source/drain external resistance or series resistance	Ω-µm
R_{Total}	Total resistance	Ω-µm
μ_{eff}	Effective mobility	cm^2/V-s
V_D	Drain voltage	V
V_G	Gate voltage	V
V_T	Threshold voltage	V
x	Mole fraction of Ge	none
ΔEc	Conduction band offset	eV
Δ_6	Six-fold degenerate conduction band	none
Δ_4	Four-fold in-plane degenerate bands	none
Δ_2	Two-fold perpendicular degenerate bands	none
τ	Scattering time	s
k	Partition coefficient at liquid/solid interface	none

CHAPTER 1

Introduction and Background

1.1. Background

For the past decades, geometrical scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) dimensions-Moore's Law, has dominated the semiconductor industry for greater transistor density and the corresponding transistor performance enhancement. The basic proposal by Dr. Gordon E. Moore in 1965 was that transistor density on an integrated circuit would approximately double every two years [1.1]. Since then, much innovation in the area of transistor scaling to follow the Moore's Law has been accomplished and led to the state-of-the-art MOSFET today. With the advance in lithography, the minimum feature size of a transistor has been remarkably scaled from several microns in the 1970's to merely sub-30 nm at 65 nm logic technology generation. The exponential progress predicted by Moore's Law stayed firm on its path for over four decades, however, the physical scaling can not continue the trend forever [1.2].

As the industry enters the 45 nm generation, where the transistor gate length drops down to 35 nm and the gate oxide thickness to 1 nm, aggressive scaling of planar bulk MOSFETs has faced significant challenges due to the inadequate control of short channel effects (SCE) and physical limitations such as increasing gate leakage current. Therefore, researchers have been actively searching for new materials and methods that can extend the conventional scaling, and some of the candidates are shown in Fig. 1.1.

Fig. 1.1. New materials or new research directions to extend Si MOSFET scaling.

Adoption of high-κ gate dielectrics provides an alternative way to reduce the equivalent oxide thickness, yet maintain the gate leakage current in a tolerable range. However, issues such as the high-κ dielectric interface defects, and mobility degradation must be solved before adoption of high k dielectrics [1.3]. On the other hand, the conventional poly-Si gate depletion effect increases the effective gate dielectric thickness, and causes drop in drive current. The use of metal gate solves the gate depletion issue. However, issues such as the appropriate tuning of metal gate work function and the process integration of these materials in complementary metal-oxide-semiconductor (CMOS) process must be solved before pursuing adoption of metal gate in production [1.4].

Another approach to enhance the performance of MOSFET is through carrier mobility enhancement by strain-induced modification of the band structure. The introduction of strain in the channel of a CMOS silicon transistor has been widely accepted as a way to boost integrated circuit performance by using a relatively simple

change in starting materials, allowing less aggressive scaling of the transistor's gate length and oxide thickness. The technique has become an integral part of the International Technology Roadmap for Semiconductors (ITRS), starting at the 90 nm technology node, and is considered a gift in the way that it enables the postponement of the implementation of more challenging process options such as metal gates and non-planar devices by one or two generations.

In this thesis work, issues related to strain engineering for p-FET performance improvement are discussed.

1.2. Physics of Strain Induced Mobility Enhancement

Strained engineering is a technology which increases the switching speed by enhancing the carrier mobility. In this section, the physics governing the mobility enhancement due to strain effects will be discussed.

The carrier mobility μ_{eff} is given by

$$\mu_{eff} = \frac{q\tau}{m^*} \quad , \tag{1-1}$$

where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass.

The carrier mobility can be enhanced by reducing the effective mass and/or reducing the scattering rate of carriers.

For electron transport in bulk Si at room temperature, the conduction band comprises six degenerate valleys of equal energy, as shown in Figure1.2 (a) which reflect the cubic symmetry of the Si lattice. The constant energy surface is ellipsoidal with longitudinal effective mass $m_l = 0.916m_o$, and transverse effective mass $m_t = 0.19m_o$ (m_o denotes the free electron mass).

Under biaxial tension, the degeneracy of the valleys is broken [Fig. 1.2(b)], and the energy level of the two valleys perpendicular to the growth plane ($\triangle_2$) is lowered

with respect to the energy level of the four in-plane valleys ($\triangle_4$). The lower energy of the $\triangle_2$ valleys means that they are preferentially occupied by electrons. Therefore, the electron mobility partly improves via a reduced in-plane and increased out-of-plane m^* due to the favorable mass of the $\triangle_2$ valleys. In addition, the inter-valley scattering is efficiently reduced due to the splitting in energy between the $\triangle_2$ and $\triangle_4$ valleys, and contributes to the improvements of electron mobility [1.5, 1.6].

Similar to the case of biaxial tensile strain, uniaxial tensile strain induced along the longitudinal channel direction also results in reduced electron effective mass and enlarged energy splitting, which both contributes to electron carrier mobility enhancement [1.7].

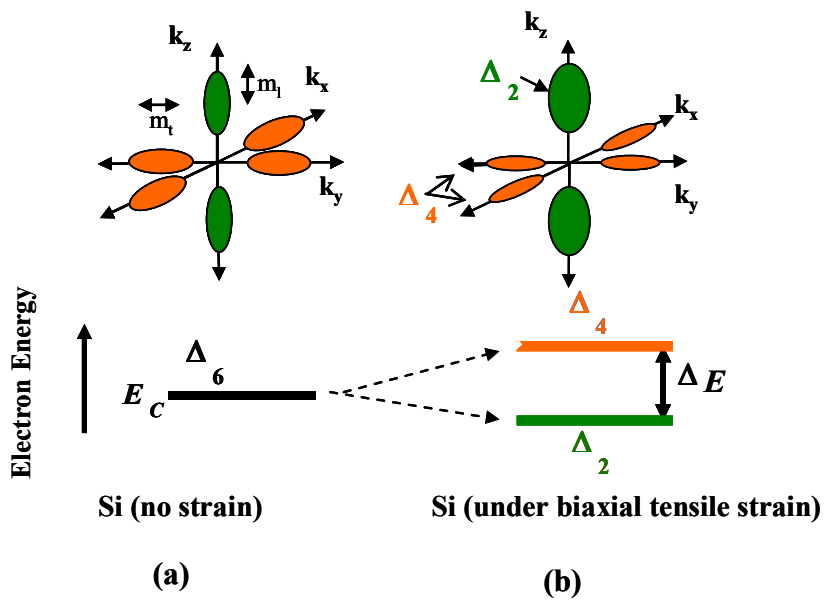

Fig. 1.2. Conduction bands for (a) unstrained Si and for (b) Si under biaxial tensile strain.

For hole transport, the hole mobility improves in a similar way, however, the valence band structure of silicon is much more complex. The valence band comprises of three bands: heavy-hole(HH), light-hole(LH) and split-off bands(SO). In unstrained silicon, the heavy hole and light hole sub-bands are degenerate at the Γ point, while the spin-orbit sub band is located only 0.44 eV below these 2 sub-bands [Fig 1.3 (a)]. With biaxial tensile strain, the energy of the heavy hole and spin-orbit sub-bands is lowered relative the light hole sub-band [Fig. 1.3 (b)]. The strain also lowers the spin orbit band and deforms all the bands, changing the hole effective mass in each. The heavy hole effective mass reduces for both biaxial compressive and tensile strain. For the light-hole mass, biaxial tensile strain reduces the mass value but biaxial compressive strain increases the mass (Fig. 1.4) [1.8]. The reduction in the heavy-hole mass with biaxial compressive strain, however, is significantly higher, results in a net effect of reduced in-plane effective mass. Reduced hole intervalley scattering with band splitting under biaxial strain [1.9] also contributes to the improved carrier mobility. With stress more than 1 GPa, the band splitting is comparable to the optical phonon energy of ~60 meV, and the intervalley scattering can be significantly reduced [1.10].

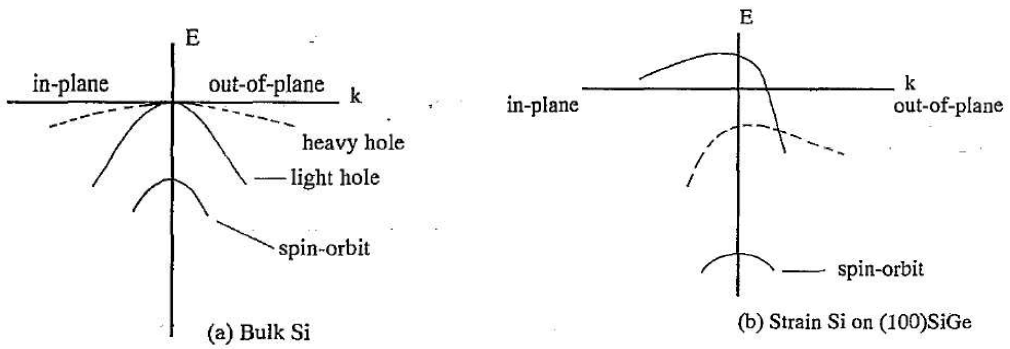

Fig. 1.3. Valence bands structure of (a) unstrained Si and (b) baxial tensile strained Si [1.12].

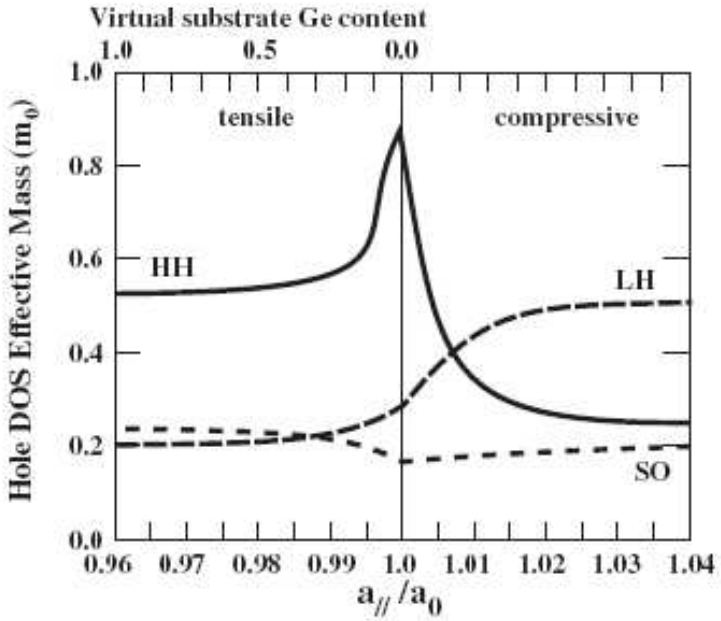

Fig. 1.4. Hole effective mass with biaxial strain. The heavy hole (HH) density of states is reduced for both compressive and tensile strain, while light-hole (LH) mass reduces with tensile strain and increases with compressive strain [1.8]. a_0 is the substrate lattice constant, and $a_{//}$ represents the lattice constant for epitaxial grown layer on substrate. When $a_{//}/a_0<1$, there will be tensile strain in the top layer.

For an uniaxial compressive strain, the hole mobility can also be improved as described in [1.7, 1.11]. A redistribution of the carrier population at the lowest energy hole band with steeper gradient results in reduced hole transport mass in the channel direction. The advantage of a uniaxial strain compared to a biaxial strain, is the enhancement of mobility sustains at a high electric field [1.12].

1.3. Sources of Strain in Transistors

To date, various strain engineering options have been proposed and demonstrated to introduce beneficial strain in the transistor channel region. We discuss the sources of stress/strain in MOSFETs in this section.

The stress in a transistor channel could be from the deposition of a film with intrinsic stress, annealing of materials with different thermal expansion coefficients, lattice interaction at heterojunctions between lattice mismatched films, and/or introduction of a dopant with larger or smaller covalent bond radius.

1.3.1. Intrinsic Stress Films

Strain in a transistor could be introduced by depositing a material with intrinsic stress. Intrinsic stress is a type of residual stress, generated due to factors such as deposition rate, thickness and deposition temperature of a thin film. For example, silicon nitride (SiN) with different deposition process conditions can be either tensile or compressive strained [1.13]. Diamond like carbon (DLC) film, as a dense form of amorphous carbon with significant sp^3 bonding, can have a high compressive stress of more than 6 GPa [1.14]. These high stress films could be deposited over the transistor as an etch stop layer to transfer its intrinsic stress to the channel, and improve the drive current of a transistor [1.15, 1.16].

1.3.2. Thermal Mismatch Stress

Thermal mismatch stress occurs when two materials with different thermal expansion coefficients are heated and expanded in contact at different rates. For example, due to a difference in thermal expansion coefficient between silicon and silicon oxide in the shallow trench isolation (STI), a compressive stress develops during oxidizing thermal anneals. For TaN metal gate capped with silicon nitride, due to the thermal-expansion coefficient mismatch between the gate and the capping layer, resulting strain can be retained and transferred to the Si channel after annealing [1.17].

1.3.3. Stress Induced from Lattice Interaction

When a film with a different lattice constant from the substrate is grown epitaxially on it, a strain develops due to the lattice interaction at the hetrojunction.

For example, as Germanium (Ge) has a lattice constant larger than Si, when the cubic SiGe alloy is formed, its equilibrium lattice constant can be estimated by the linear interpolation between the lattice constant of Si and Ge according to the Vegard's law [Fig. 1.5 (a)],

$$a_{SiGe} = (1-x)\, a_{Si} + x\, a_{Ge} \tag{1-2}$$

where a_{Si} and a_{Ge} are the lattice constant of Si and Ge, respectively, and x is the Ge concentration incorporated in the SiGe alloy.

When a thin Si film is grown pseudomorphically on the relaxed SiGe layer, the silicon lattice will be biaxially stretched to match the larger lattice constant of SiGe alloy [Fig. 1.5 (b)].

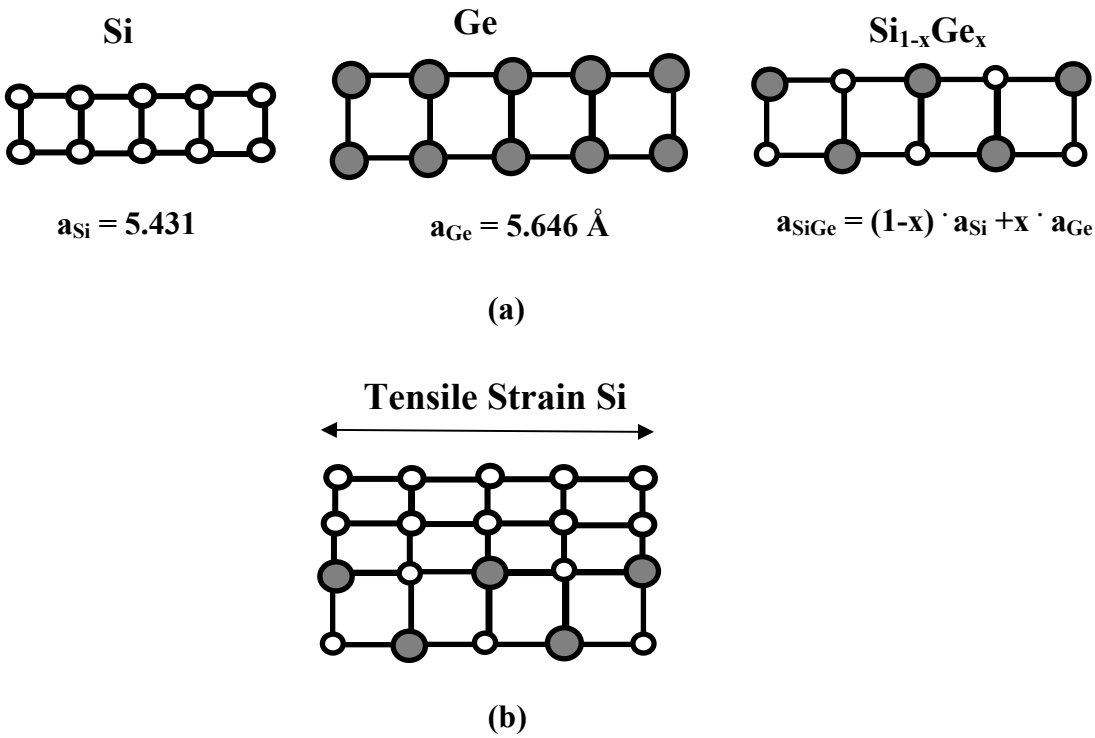

Fig.1.5. (a) Schematic drawing of he lattice constant of Si, Ge, and SiGe alloy. The equilibrium lattice constant of SiGe is estimated using Vegard's law. (b) When a thin Si film is grown pseudomorphically on the relaxed SiGe layer, a tensile strained in silicon will be achieved.

1.3.4. Dopant Induced Stress

When a dopant atom is introduced through ion implantation or diffusion, a local lattice expansion or contraction occurs depending on the varying atomic sizes and bond lengths of the atoms.

For example, Boron has an atomic size that is much smaller than Si. When it is incorporated substitutionally in Si, a local lattice contraction is introduced (Fig. 1.6). This configuration with local lattice contraction would increase the strain energy stored in the lattice. Deactivation of highly activated and metastable boron in S/D or S/D extension of a p-FET may occur during subsequent thermal process and lead to performance degradation.

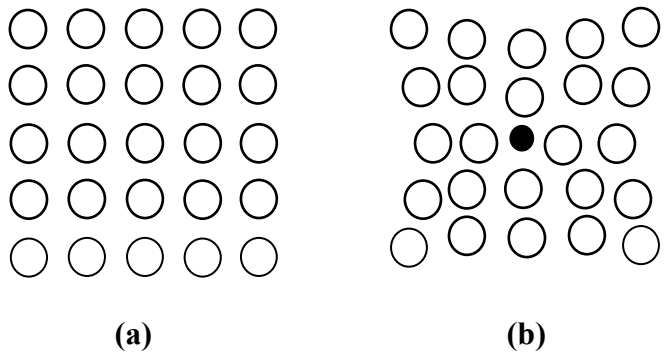

Fig.1.6. Schematic drawing of (a) Silicon Lattice and (b) Silicon lattice contraction caused by Boron doping.

In addition, the overall equilibrium lattice constant of Si S/D would be reduced with the incorporation of a high concentration of B. This reduction of S/D lattice constant would introduce an undesirable tensile strain in the transistor channel and lead to p-FET performance degradation. Therefore, reduction of the undesirable strain caused by boron doping is an important issue.

1.4. Strained P-FET Technologies

Strain engineering is a very effective way to improve p-FET performance and reduce the gap between p-FET and n-FET in current drivability. After knowing the sources of strain in a transistor we review the strained p-FET technologies in this section.

Generally, the strain techniques can be classified into global strain and local strain techniques.

1.4.1. Global Strain Technique

For the global strain, it is usually introduced early in the fabrication process, for example, by growing Si channel on relaxed silicon-germanium (SiGe) (Fig 1.7). In

such an approach [1.18], a thick layer of graded SiGe buffer is firstly grown on Si. This graded SiGe buffer confines the dislocations at the bottom, and results in the relief of elastic strain. A relaxed SiGe layer can then be grown on the thick graded buffer layer. Finally, a layer of Si is grown pseudomorphicly on the relaxed SiGe. Due to the lattice mismatch of Si and relaxed SiGe, the pseudomorphic layer of Si is under biaxial tensile strain, which modifies the band structure and enhances carrier transport [1.18].

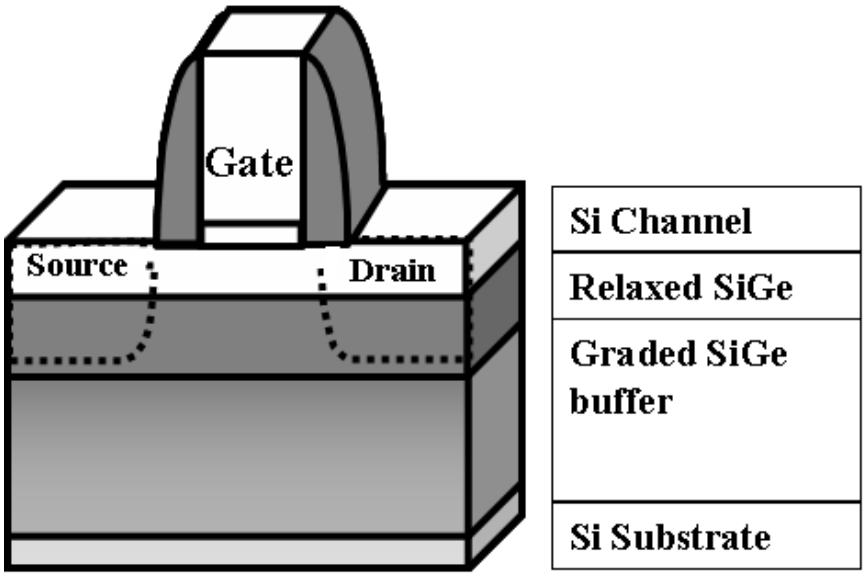

Fig. 1.7. Schematic drawing of strained Si channel transistor formed by growing Si channel on relaxed SiGe. The relaxed SiGe was grown on a thick graded SiGe buffer, which serves as the dislocation filter and trap the dislocations at the interface between graded SiGe buffer and Si substrate.

However, there are several drawbacks of this method. Firstly, even after extensive effort has been made, high surface dislocation density remains an issue [1.19]. Secondly, dislocations at the Si channel/relaxed SiGe interface can causes high leakage current from source to drain. It is known that a higher Ge concentration in the relaxed SiGe layer requires thinner Si channel, consistent with the model of defect introduction via partial relaxation [1.20]. Though a higher Ge content is desired for introducing larger strain in the channel, a reduction of Si layer thickness and/or increase in the Ge concentration in the substrate increases the likelihood of Ge atoms diffusing to the interface between the gate dielectric and the strained Si channel [1.21]. This introduces interface states and oxide charges and degrades the carrier mobility. Thirdly, the hole mobility enhancement observed in a strained-Si/relaxed SiGe *p*-MOSFET diminishes at high vertical field regime, making it a less attractive option for implementation in high volume production.

1.4.2. Local Strain Techniqes

For local strain, the strain is introduced only in specific regions of device, and introduced only in the later stage of a fabrication process. Some examples of local strain techniques include using shallow trench isolcation (STI) to introduce compressive strain in the p-FET channel, using silicide-induced stress, adoption of the compressive nitride or diamond like carbon (DLC) stress liner, or incorporation of lattice mismatched S/D stressors.

Shallow trench isolation process may induce significant mechanical stress in devices [1.22]. The higher the distance STI to gate edge is, the lower the compressive stress is. This stress technique enhances p-FET performance and degrades n-FET performance.

Another approach for introducing beneficial strain in p-FET is by silicide induced stress [1.23]. Nickel-platinum silicide (NiPtSi) was reported as a S/D material for strain engineering in p-MOSFETs to improve drive current performance. During the nickel-platinum silicidation process due to volume change and reaction parameters, a compressive strain can be generated in the channel region.

In addition, films with intrinsic compressive stress deposited as an etch stop layer can also transfer its intrinsic stress to transistor channel and generate beneficial strain in p-FETs. Currently, SiN linear, with the highest reported compressive stress of around 2.4–3.5 GPa is being employed to give significantly boost the transistor performance [1.24, 1.25]. Very recently, Diamond-like carbon (DLC) film, known to exhibit a very high intrinsic compressive stress more than 6 GPa, was first introduced in a p-FET to drastically increase the stress level and drive current of a p-FET [1.14, 1.26].

Furthermore, using a lattice mismatched S/D stressor, such as $Si_{1-x}Ge_x$ S/D [1.27-1.30], is also a very promising technique to introduce local compressive strain in channel region for p-FET performance boost. More than 50% enhancement in hole mobility over universal mobility curve can be achieved [1.30] with only a few key process steps added to the standard CMOS fabrication (Si recess etch after the spacer formation, and $Si_{1-x}Ge_x$ S/D selective epitaxy growth). The origin of the strain in the channel region is from the interaction between the pair of lattice-mismatched materials at semiconductor heterojunctions (Fig. 1.8), which induces lateral compressive strain along the Si channel direction and enhances the hole mobility.

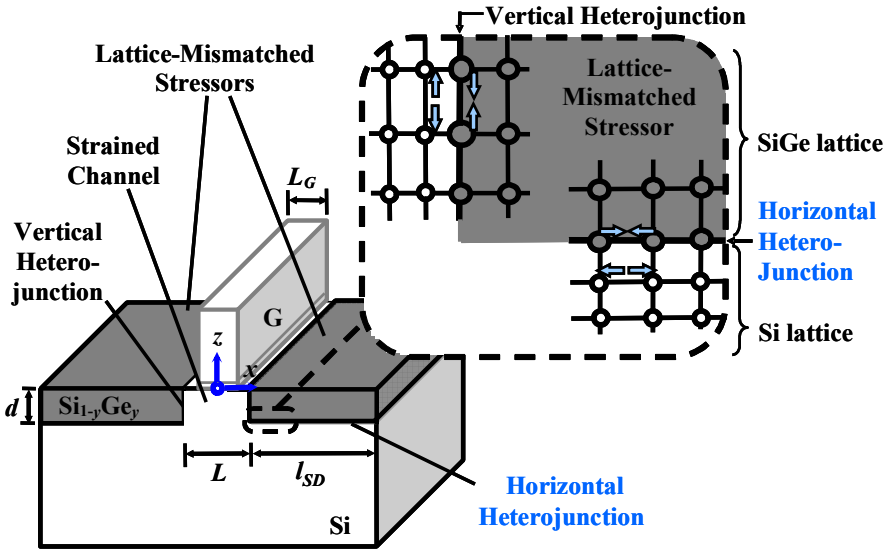

Fig. 1.8. Schematic drawing of a transistor with SiGe S/D. Lattice interactions at the hetero-interfaces induces compressive strain in the channel region along the carrier transport direction [1.31].

For p-MOSFET with $Si_{1-x}Ge_x$ S/D, early numerical simulation studies [1.31] indicate that the magnitude of the lateral compressive strain ε_{xx} and the vertical tensile strain ε_{zz} induced in the Si channel can be increased by increasing the Ge mole fraction x in the $Si_{1-x}Ge_x$ S/D region, by increasing the recess depth of the $Si_{1-x}Ge_x$ S/D, or by reducing the separation between the $Si_{1-x}Ge_x$ S/D regions.

1.5. Objective of Research

The main objective of this thesis work is to explore various potential ways to enhance p-MOS performance through strain engineering. These include demonstration of new process technology to increase the strain level in SiGe S/D p-FET, adoption of novel device structures to introduce strain from beneath the channel, and reducing the undesirable tensile strain caused by boron doping in p-FET S/D.

1.6. Outline

The issues discussed in this thesis are as following:

Chapter 2 demonstrates a new method of local Germanium enrichment in S/D stressor for transistor performance enhancement. By laser induced melting, intermixing, and re-growth of amorphous Germanium on $Si_{0.8}Ge_{0.2}$ S/D, a graded Ge profile with peak Ge content of ~37% in the S/D was formed upon recrystallization. Process integration issues are addressed, including selection of laser anneal conditions for increasing Ge content in SiGe S/D without degrading gate stack integrity. High resolution x-ray diffraction (HRXRD) was used to characterize the change in lattice constant after the Germanium enrichment process. Micro Raman analysis confirmed the retention of high strain level after recrystallization. Device characterization was performed, and we observed an I_{Dsat} enhancement of ~14% for Ge-enriched S/D device over control strained p-FETs with $Si_{0.8}Ge_{0.2}$ S/D at comparable short-channel effects and S/D sheet resistance. The issues and limitations of this technique will also be discussed, and future work is proposed.

Chapter 3 explores a novel structure in employing a reverse embedded Silicon-Carbon (Si:C) stressor (also known as the strain transfer structure STS) under the transistor channel, which makes use of the lattice interactions at the vertical heterojunction between the Si and the embedded Si:C STS to impart lateral compression in the Si channel. However, as the Si:C stressor is grown at the early stage of fabrication, there are concerns on the potential relaxation of Si:C during subsequent high temperature process. These concerns are addressed in this chapter by material studies with high resolution x-ray diffraction (HRXRD), and micro Raman analysis. Device fabrication is also discussed with the focus on key process step

challenges and solutions. Finally a summary of device performance and proposal on further work to improve the device performance are covered.

Chapter 4 discusses the undesirable tensile stress caused by high concentration of Boron doping in p-FETs S/D. Incorporation of Sn was investigated as a strain compensation implant. High resolution XRD measurement after laser annealing at a fluence of 740 mJ/cm^2 confirms that the tensile strain caused by supersaturated boron was relieved by tin co-implantation. In addition, this Sn strain compensation implant was also found to enhance boron's thermal stability, and improves the retention of highly-activated and metastable boron through a local strain compensation effect. A correlation was observed between the overall tensile strain in the film and the sheet resistance increment during post-LA thermal processing. Detailed explanations on the physics behind were discussed.

Finally, a summary of this thesis work and proposal for future works are included in chapter 5.

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CHAPTER 2

Germanium Enrichment in Silicon-Germanium Source/Drain for P-FETs Strain and Performance Enhancement

2.1 Introduction

As we discussed previously, in recent technology development, a promising and effective method for extending p-FETs performance makes use of lattice-mismatched silicon-germanium (SiGe) source and drain (S/D) stressors [2.1-2.3]. Due to the lattice interactions at the vertical SiGe/Si heterojunction, a lateral compressive strain and vertical tensile strain are induced in the adjacent transistor channel region, which contributes favorably to drive current improvement. Moreover, retention of the significant hole mobility enhancement even at a high effective field E_{eff} regime [2.1] makes it an attractive strain engineering approach.

Larger strain effects and further performance improvement can be achieved by increasing the Ge content x in the $Si_{1-x}Ge_x$ S/D stressors [2.4, 2.5]. However, strain relaxation and defect formation may occur during the epitaxial growth process which typically employs temperatures above 500°C. The retention of strain in SiGe (on bulk Si) formed by conventional epitaxy process is difficult when the Ge content is very high. Non-equilibrium processes, such as pulsed laser annealing (LA), with a heating time down to nano-seconds, could be a good candidate for suppressing the propagation and growth of misfit dislocations and for forming highly strained $Si_{1-x}Ge_x$ [2.6]. Laser-induced and localized surface melting of both a Ge film and a part of the underlying

substrate can lead to inter-diffusion of liquid Ge and Si, the resulting melt can then re-crystallize epitaxially with the substrate as a template. This laser-assisted epitaxy of $Si_{1-x}Ge_x$ alloys has been reported to produce strained crystalline $Si_{1-x}Ge_x$ [2.7, 2.8]. However, such process has never been exploited for transistor fabrication, particularly for defect/strain management during SiGe S/D formation in strained p-FETs.

Therefore, we investigate the laser-induced intermixing and recrystallization of amorphous Ge (α-Ge) on SiGe S/D for increasing the Ge content in S/D stressors of strained p-FETs.

2.2 Process Flow

Silicon-on-insulator (SOI) substrates with a Si thickness of ~60 nm were used for this technology demonstration. SOI substrate was chosen because both the thin silicon film on buried oxide (BOX) and the polysilicon gate pattern on gate oxide are thermally isolated from bottom silicon substratewhich is a good heat dissipation path. As a result, the low laser fluencemay be used to activate the impurities in SOI without any other integration problem such as poly gate distortion [2.9].

The key process steps and schematic drawing after several critical steps are shown in Fig. 2.1.

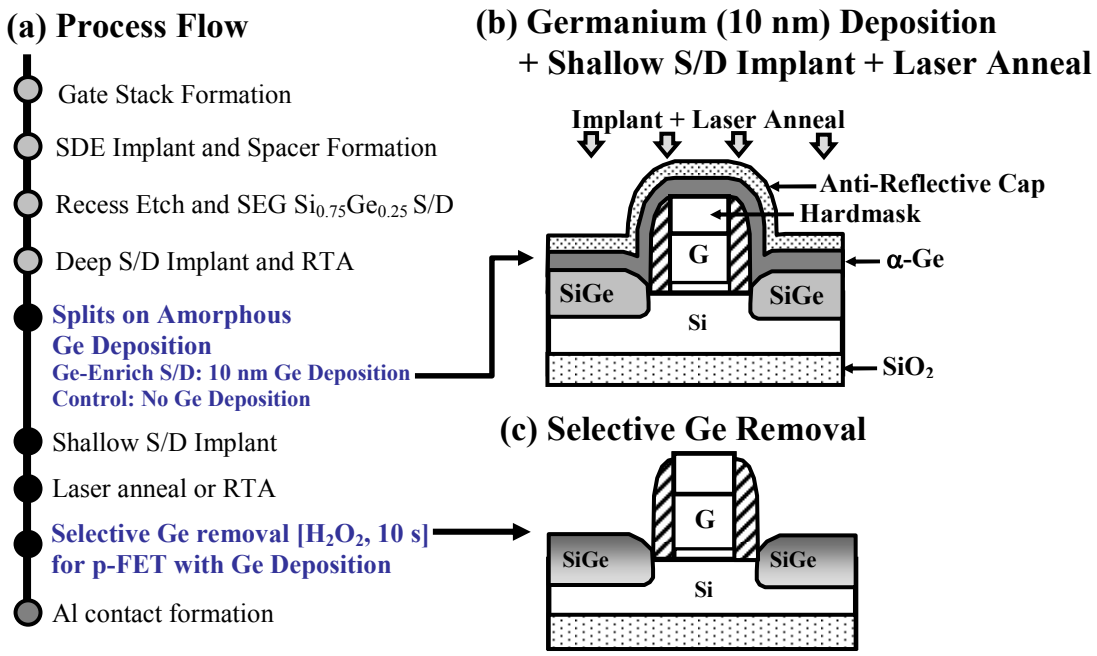


Fig. 2.1. (a) Key process steps to form a p-FET with enriched Ge content in SiGe S/D stressor. The novel Ge enrichment process involves (b) deposition of α-Ge (10 nm), laser annealing, and (c) selective removal of unreacted Ge to form the complete device.

After LOCOS formation, threshold voltage V_T adjust implant was performed. A 3.0 nm SiO_2 was thermally grown as the gate dielectric, followed by a 100 nm poly-Si gate which was subsequently implanted with BF_2 and activated.

A SiO_2 hardmask or optical layer (100 nm) was formed to protect the gate stack in a laser annealing step to be performed later. This SiO_2 coating reduces the laser absorption on gate, and it increases the process window for the melting laser annealing [2.10]. Optical lithography and photo-resist trimming were then employed for gate patterning. After gate etch, S/D extension and slim silicon nitride spacers were formed. S/D recess etch of ~30 nm and $Si_{0.8}Ge_{0.2}$ selective epitaxy using ultra-high vacuum chemical vapor deposition (UHVCVD) were performed to form slightly raised embedded $Si_{0.8}Ge_{0.2}$ S/D stressors. Deep S/D implants and rapid thermal anneal (RTA) at 900 ºC for 30 s were then performed.

For the Ge enrichment device split, 10 nm of α-Ge was sputter-deposited over the entire device region. All wafers went through a shallow S/D implant. For laser annealing splits, deposition of an additional 30 nm thick SiO_2 layer as an anti-reflection layer for laser annealing was then performed. While the wafer without α-Ge deposition may have some additional implant damage in the SiGe from the shallow S/D implant, significant impact on strain level is not expected following laser annealing and rapid re-crystallization [2.11].

The laser was operated in N_2 ambient at wavelength of 248 nm with pulse duration (FWHM) of 23 ns, with 10 pulses, and repetition rate of 1 Hz. The laser fluence ranges from 150 to 400 mJ/cm^2. Ten laser pulses were applied on all laser-annealed samples in this work. Multiple pulses are used to reduce the variation of laser fluence and to achieve a more homogenous Ge profile and higher strain level [2.12]. The localized surface melting of both the α-Ge film and a part of the underlying $Si_{0.8}Ge_{0.2}$ S/D formed a melt, in which inter-diffusion occurred. Upon cooling and recrystallization, a SiGe S/D with good crystalline quality and high Ge content was formed. The remaining Ge and $Si_{1-x}Ge_x$ (where $x > 60\%$) over gate and spacer were selectively etched using hot H_2O_2 solution. Aluminum contacts to S/D (unsilicided) were made for device characterization.

2.3 Selection of Laser Fluence

Proper selection of laser fluence is the key to this technique. To have successful laser assisted epitaxy, the energy absorbed needs to be high enough to melt the whole amorphous Ge layer, and sufficient amount of underlying substrate for good crystalline re-growth. Yet at this fluence, the gate stack integrity must be preserved for a device integration. If the gate stack is heated to excessively high temperature, it potentially

deforms or explodes. As the energy absorbed is very close to the surface and due to short wavelength of the laser, the Ge layer thickness was kept low to be around 10nm.

Figure 2.2 shows the Ge profile obtained after LA at various fluences. A graded gradual change in Ge profile was observed for most LA fluences. A possible mechanism for the graded Ge profile is due to the Ge partitioning at the solid-liquid SiGe interface at ultrafast cooling rate. Solute segregation is usually characterized by the partition coefficient k, the ratio of the atomic fraction of solute in the solid X_s to that in the liquid X_l at the interface ($k=X_s/X_l$) [2.13]. The equilibrium k value of Ge is 0.45 [2.13] or 0.33 [2.14]. With laser annealing, which is a localized heating process, the Si around acts as a heat sink, leading to the ultrafast cooling rate that induces Ge trapping in the solid phase. The partition coefficient of Ge in this case increases to around 0.73 [2.13], but it is still less than 1, hence the graded $Si_{1-x}Ge_x$ is observed. Another possible reason of the graded Ge profile could be due to the local diffusion of Ge. During the recrystallization process (i.e. the melt transfer from liquid to solid phase), large amount of heat was released from the melt, and transferred to underlying or surrounding Si. This heat, confined by LOCOS and buried oxide, can lead to local diffusion of Germanium, and result in a graded Ge profile.

It is also observed that at a low fluence of 230 mJ/cm^2, there is a steep grading of Ge concentration, while with increasing fluence, the Ge profile becomes more uniform due to increased intermixing of the Ge layer with the underlying SiGe S/D with higher energy absorbed.

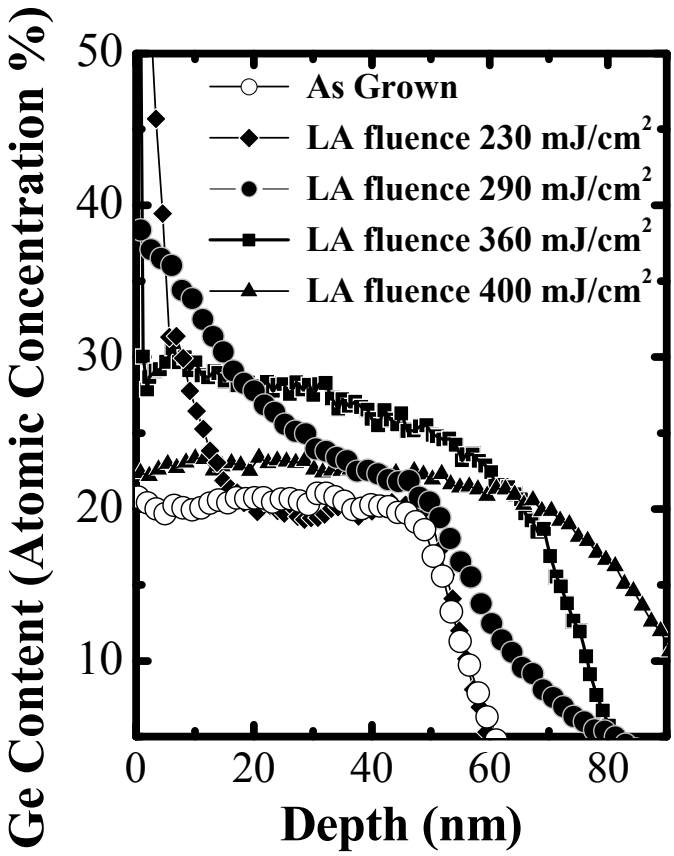
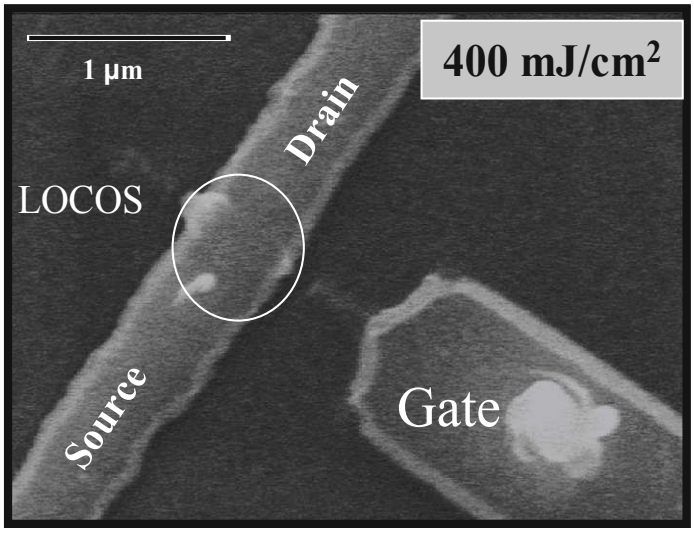
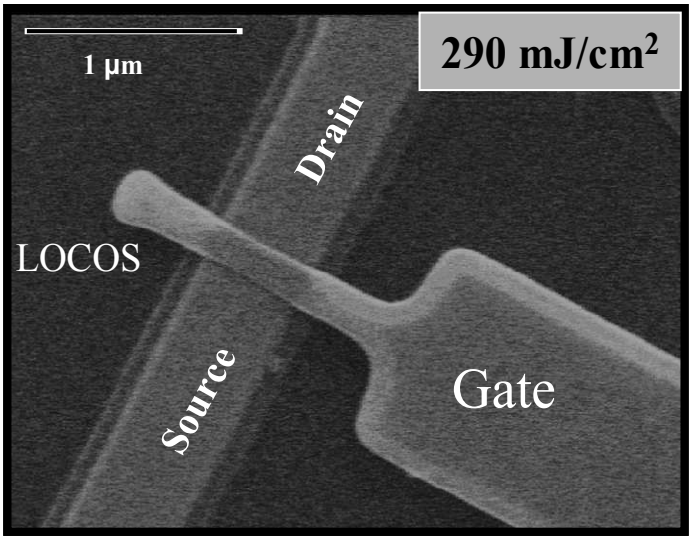


Fig. 2.2. Depth profile of Ge obtained by SIMS analysis after laser annealing (LA) of amorphous Ge on $Si_{0.8}Ge_{0.2}$ using different laser fluences. 10 laser pulses were used at each fluence. Ge concentration was increased in the SiGe S/D after LA.

For a S/D stressor application, uniformed Ge profile in the S/D is more desirable, because with raised S/D, the top Ge enrichment would have limited strain benefits, and could lead to high silicide resistance. However, when this technique is integrated into transistor fabrication flow, high laser fluence could cause boron penetration through gate dielectric and increase the gate leakage current. In extreme cases, it can also cause severe gate deformation. Figure 2.3 (a) shows a device with severely deformed or broken gate line after being annealed at 400 mJ/cm^2 10 pulses, compared to a device annealed at 290 mJ/cm^2 for 10 pulses [Fig. 2.3(b)].



(a)



(b)

Fig. 2.3. (a) SEM images of p-FET after laser annealing at a fluence of 400 mJ/cm^2 (10 pulses). The gate line was broken due to excessive heat at this laser fluence. (b) SEM image of p-FET after the Ge-enrichment process using a laser fluence of 290 mJ/cm^2 (10 pulses). The gate integrity was preserved.

Therefore, to integrate the laser-induced Ge-enrichment process in device fabrication, LA conditions have to be carefully selected in addition to the use of a protective gate hardmask. Figure 2.4 illustrates how the laser fluence was chosen for device integration.

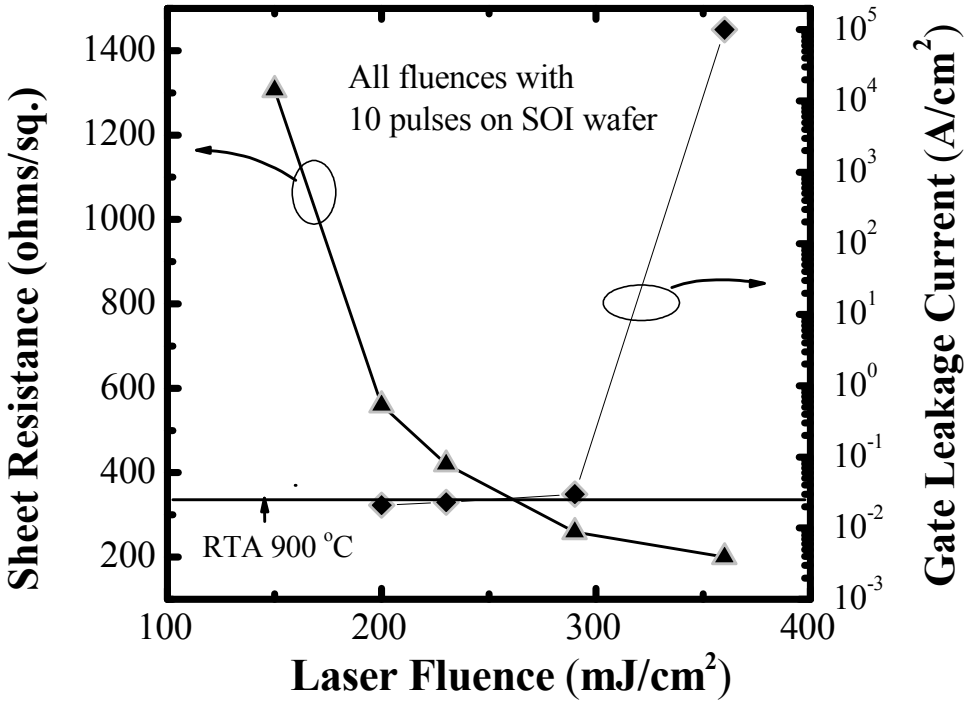


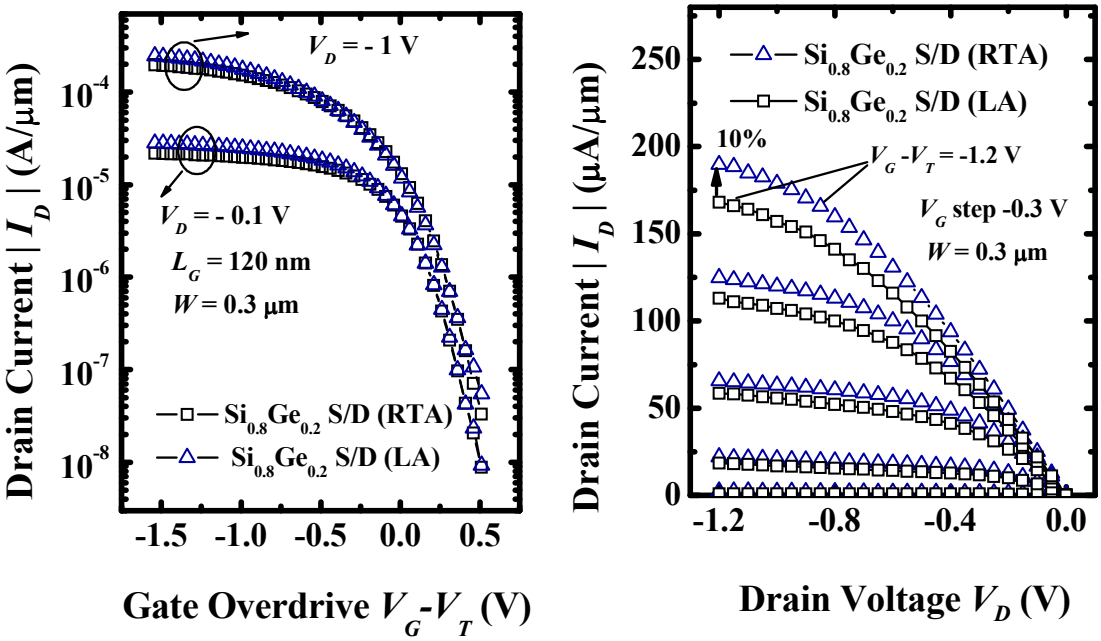
Fig. 2.4. S/D sheet resistance and gate leakage current when being annealed using different laser fluences for 10 consecutive pulses. LA at 290 mJ/cm^2 is observed to substantially lower the sheet resistance, and still preserve the gate stack integrity.

The sheet resistance of laser annealed samples as well as RTA (annealing temperature of 900 ^{o}C) annealed blanket samples are plotted in Figure 2.4. It is observed that with increasing laser fluence, the dopant activation improves. At a laser fluence of 290 mJ/cm^2, the laser annealed S/D has substantially lower sheet resistivity as compared to rapid thermal annealed S/D. This high efficiency of dopant activation can be attributed to melting and the fast re-growth time of the silicon (10^{-10} s) which allows trapping of the dopants in substitutional lattice sites in great excess of the maximum solid solubility in the metastable state [2.15].

The gate leakage current for laser annealed and RTA devices was measured at $V_D = V_G - V_T = -1.2$ V after different annealing conditions and also shown in Figure 2.4. Devices laser-annealed using a fluence of 290 mJ/cm^2 shows comparable gate leakage

current with rapid thermal annealed devices, indicating no gate dielectric degradation due to LA. Thus this laser annealing fluence of 290 mJ/cm^2 could be used on transistor fabrication.

To further examine the device performance with this laser annealing condition, the I_D-V_D and $I_D - V_G$ characteristics of a laser annealed device (process flow shown in Figure 2.1 (a)) compared to an RTA control is shown in Figure 2.5. Comparable off-state leakage current (I_{OFF}), sub-threshold swing (SS) and drain induced barrier lowering (DIBL) was observed. This confirms that the laser annealing process did not have negative effect on the transistor performance. Furthermore, a drive current enhancement of ~ 10 % was observed for the laser annealed (290 mJ/cm^2, 10 pulses) $Si_{0.8}Ge_{0.2}$ S/D p-FET, compared to RTA annealed control due to lower S/D resistance, and higher dopant activation.



(a) (b)

Fig. 2.5. (a) I_D-V_G characteristics for laser annealed and RTA devices with a gate length of 120nm show comparable off-state leakage current, sub-threshold swing(SS) and drain induced barrier lowering (DIBL). (b) I_D-V_D characteristics of these closely matched devices. The laser annealed $Si_{0.8}Ge_{0.2}$ p-FET shows a drive current enhancement of ~10% compared to RTA control

Therefore, 290 mJ/cm^2 is an appropriate LA condition for integration of the Ge-enrichment process on p-FETs.

2.4 Material Study with Selected Fluence

Material studies on large areas are performed with this selective laser annealing condition (290 mJ/cm^2) after Germanium enrichment process.

The crystal quality and change in lattice constants for $Si_{1-x}Ge_x$ formed by laser annealing of amorphous Germanium on $Si_{0.8}Ge_{0.2}$ stack are examined by high resolution x-ray diffraction (HRXRD) (Fig.2.6). The well-defined $Si_{1-x}Ge_x$ satellite peaks (shown in the insert) indicate the formation of a high-quality $Si_{1-x}Ge_x$ epi-layer

after the Ge enrichment process. The increase of lattice constant over that of Si can be calculated based on the displacement of the satellite peak from Si substrate peak [2.16, 2.17]. The as-grown $Si_{0.8}Ge_{0.2}$ has a lattice constant that is 0.78% larger than that of Si. While Ge-enriched $Si_{1-x}Ge_x$ (peak Ge content of ~38%) formed by laser annealing of α-Ge/$Si_{0.8}Ge_{0.2}$ at 290 mJ/cm^2 has a lattice constant that is 1.1% larger than that of Si, which corresponds to an equivalent average Ge content of 30%. This matches the spatially averaged Ge content (obtained from SIMS). Strain relaxation does not generally occur for this Ge content.

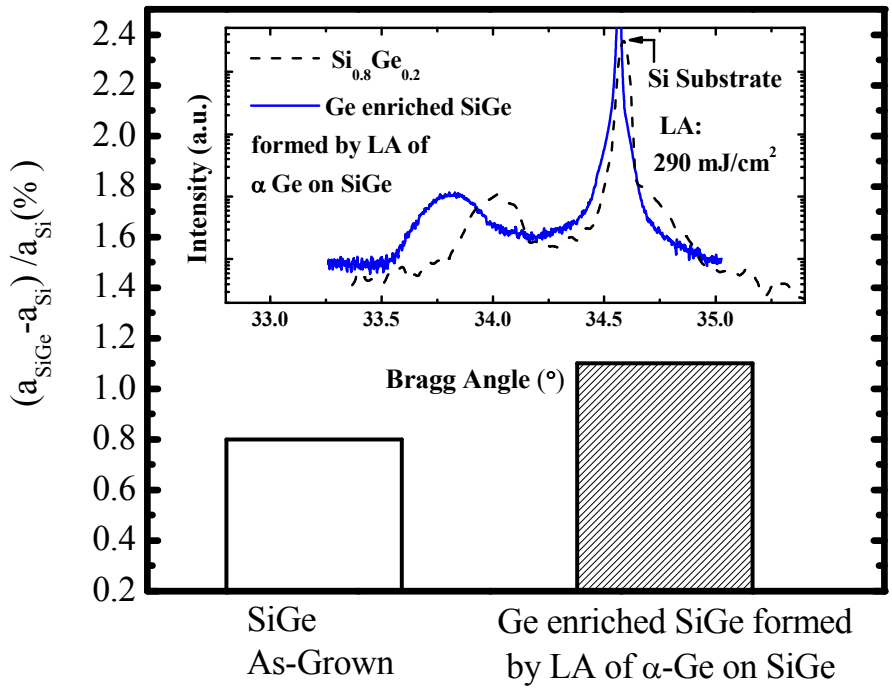


Fig. 2.6. HRXRD spectra for Ge-enriched SiGe formed after LA of α-Ge/$Si_{0.8}Ge_{0.2}$ with a fluence of 290 mJ/cm^2 (10 pulses), showing excellent crystalline quality of the $Si_{1-x}Ge_x$ film on Si. The shift of the satellite peak to a lower angle indicates an increase in the lattice constant in the SiGe film or a successful increase in Ge content.

UV Raman measurement was also performed for $Si_{1-x}Ge_x$ grown on Si to determine the strain in $Si_{1-x}Ge_x$ before and after Germanium enrichment process. It is known that Raman frequency of the Si-Si vibrational mode in heteroepitaxial $Si_{1-x}Ge_x$ (represented by $\omega_{Si\text{-}Si}(x)$) shift from the unstrained Si substrate peak due to both germanium content, x, and the strain in $Si_{1-x}Ge_x$ layer, ε [2.18] is given by

$$\omega_{Si-Si}(x) = 520.0 - 68x - 830\varepsilon . \tag{2-1}$$

When there is no strain in $Si_{1-x}Ge_x$, i.e. fully relaxed, $\omega_{Si-Si}(x)$ is equal to $520.0 - 68x$, where x is the Ge content in $Si_{1-x}Ge_x$. When there is strain in $Si_{1-x}Ge_x$, the level of strain is proportional to extend of the peak shift from the relaxed $Si_{1-x}Ge_x$ peak.

As shown in Figure 2.7, the Ge enriched sample has a very high compressive strain of -1.1%, as compared to a -0.7% strain for laser-annealed $Si_{0.8}Ge_{0.2}$ (Fig. 2.7).

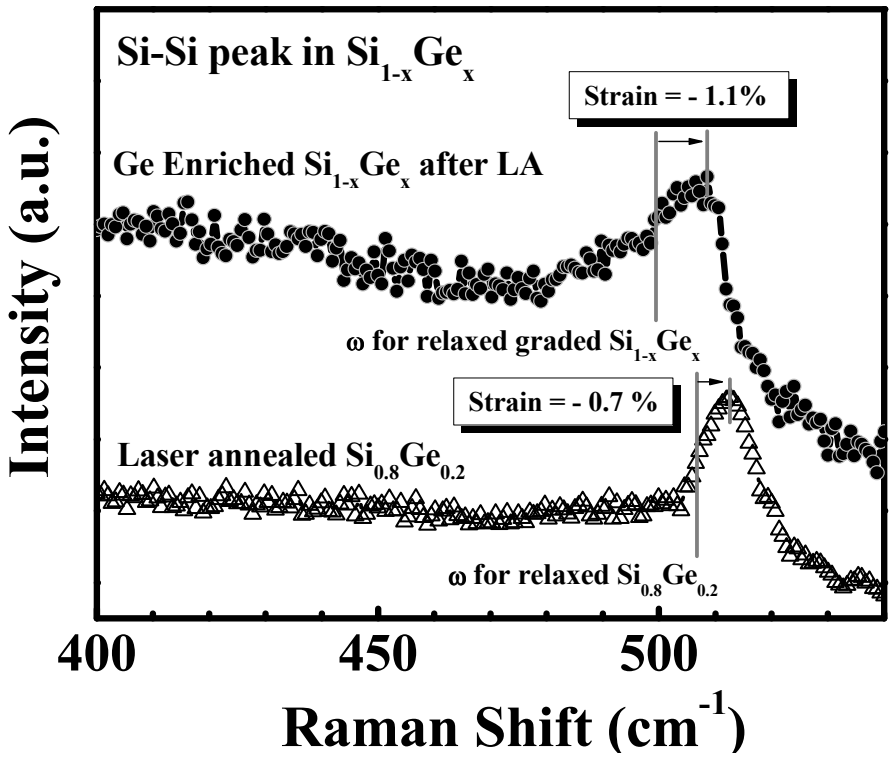


Fig. 2.7. UV Raman spectra showing that Ge enriched SiGe layer formed by laser annealing of α-Ge on SiGe has a higher compressive strain of -1.1%.

2.5 Device Characteristics

Fig. 2.8 shows a TEM image of the completed Germanium enriched S/D device with gate length of 120 nm.

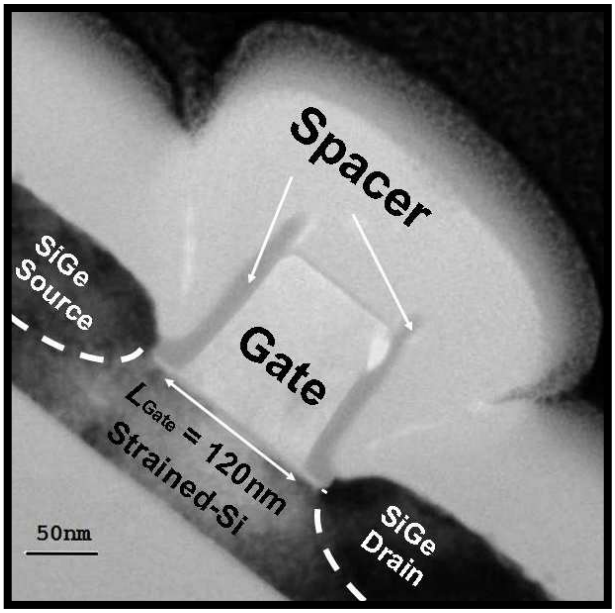
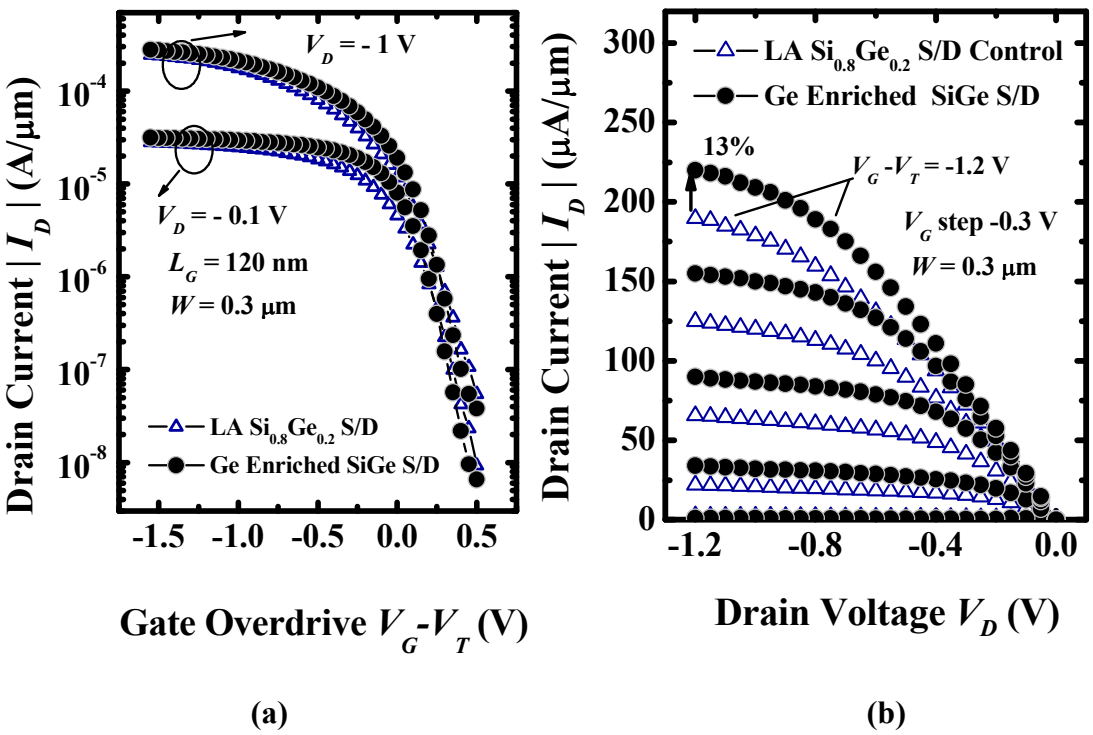


Fig. 2.8. TEM image of a completed p-FET with Ge-enriched SiGe S/D.

The device performance of laser annealed $Si_{0.8}Ge_{0.2}$ S/D and Germanium enriched SiGe S/D p-FETs are shown in Figure 2.9. I_D-V_G characteristics of these devices [Fig 2.9 a)] shows comparable off-state leakage current I_{OFF}, sub-threshold swing (SS), and drain-induced barrier lowering (DIBL). This indicates that the germanium enrichment process did not cause degradation in the transistor short-channel performance. At the same time, with the same gate over-drive of -1.2 V, a drive current enhancement of approximately 13% was observed for Ge-enriched S/D over laser annealed p-FETs with $Si_{0.8}Ge_{0.2}$ S/D [Fig 2.9 b)].



(a) (b)

Fig. 2.9. (a) I_D-V_G characteristics for laser annealed $Si_{0.8}Ge_{0.2}$ S/D and Germanium enriched S/D devices with a gate length of 120nm show comparable off-state leakage current, sub-threshold swing(SS) and drain induced barrier lowering (DIBL). b) I_D-V_D characteristics of these closely matched devices. The Germanium enriched S/D p-FET shows a drive current enhancement of ~13% compared to the laser annealed device with $Si_{0.8}Ge_{0.2}$ S/D.

To verify the impact of S/D series resistance R_{SD} and carrier mobility on I_{Dsat} enhancement, a total resistance slope-based approach [2.19] was employed. The total resistance R_{TOT} (=V_D/I_D) as a function of gate length L_G is plotted (Fig. 2.10) for p-FETs with both LA $Si_{0.8}Ge_{0.2}$ S/D and Ge enriched S/D at V_G-V_T of -1.2 V.

The total resistance(R_{TOT}) measured with presence of series resistance is given by the sum of channel resistance (R_{CH}) and S/D series resistance (R_{SD}) [2.19], i.e.

$$R_{TOT} = R_{CH} + R_{SD} = A(L_G - \Delta L) + R_{SD} = AL_G + B \qquad (2\text{-}2)$$

where $A = \dfrac{1}{\mu_{eff} W Q_{inv}}$ and,

$B = R_{SD} - A\Delta L$, and

L_G is the measured physical gate length.

Physically, A is the intrinsic channel resistance per unit effective channel length, and can be obtained from the slope of R_{TOT} versus physical gate length L_G plot, i.e. A= dR_{TOT}/dL_G.

It was observed that Ge-enrichment in S/D stressors leads to reduced dR_{TOT}/dL_G or in other words, mobility enhancement. The S/D series resistance is also slightly improved for p-FETs with Ge-enriched S/D stressors, probably due to the enhanced B dopant activation with increasing Ge content.

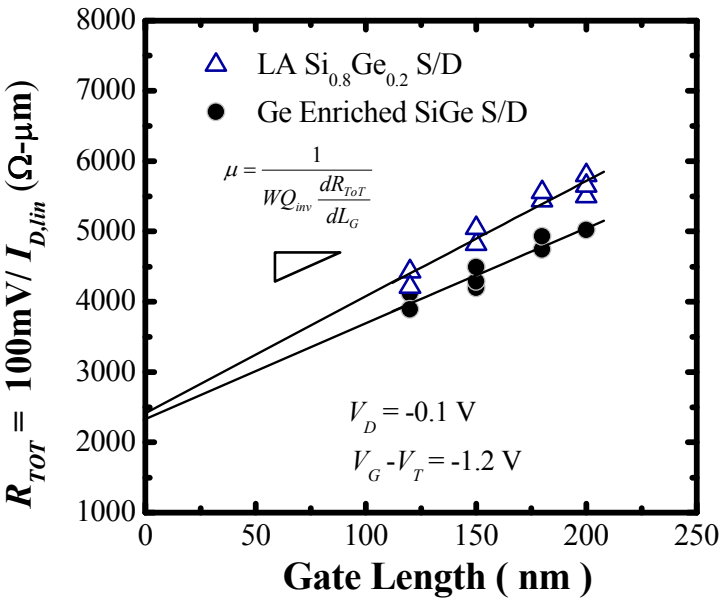


Fig. 2.10. Total resistance R_{TOT} (= V_D/I_D) as a function of gate length L_G. Devices with Ge enriched S/D have a smaller slope (dR_{TOT}/dL_G), indicating enhanced carrier mobility.

Figure 2.11 shows the saturation drive current I_{Dsat} enhancement as a function of gate length for p-FETs fabricated using this novel Ge-enrichment process compared to LA $Si_{0.8}Ge_{0.2}$ S/D control. I_{Dsat} is measured at a gate overdrive of -1.2 V and a V_D of -1.2 V. In general, I_{Dsat} enhancement increases with decreasing L_G due to the enhanced strain effects or influence of S/D stressors in shorter channel devices when the stressors are of close proximity.

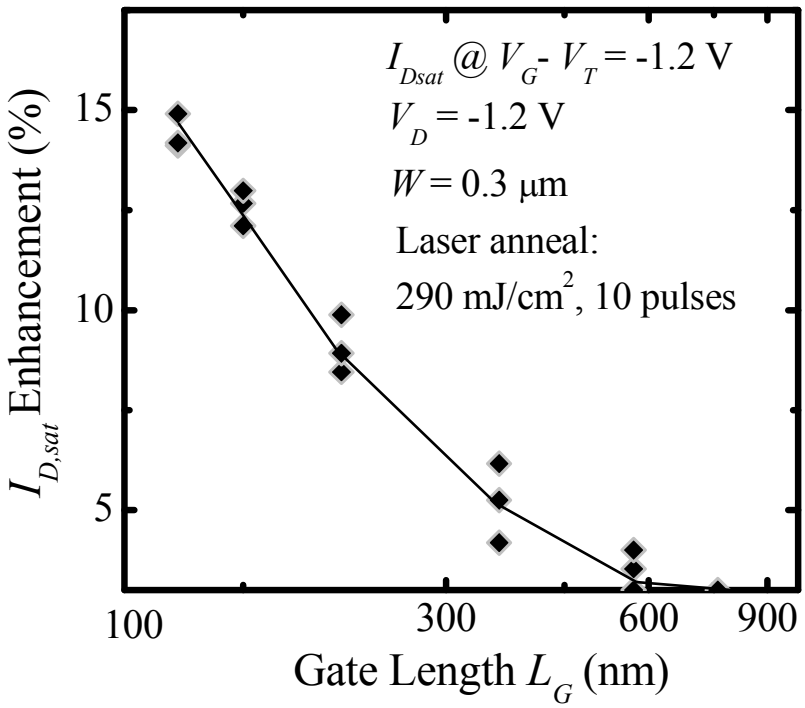


Fig. 2.11. Saturation drain current I_{Dsat} of p-FETs with Ge-enriched SiGe S/D is enhanced over that of p-FETs with $Si_{0.8}Ge_{0.2}$ S/D. Larger I_{Dsat} enhancement is observed at smaller gate length L_G due to enhanced strain effects when S/D stressors are placed in closer proximity.

The I_{OFF} -I_{Dsat} for laser annealed $Si_{0.8}Ge_{0.2}$ S/D and Germanium enriched S/D p-FETs with L_G in the range of 120-150 nm is plotted in Figure 2.12. The Ge-enriched graded SiGe S/D gives an I_{Dsat} enhancement of ~12% compared to the laser annealed $Si_{0.8}Ge_{0.2}$ p-FETs at a fixed off-state current of 20 nA/µm due to strain enhanced transistor performance.

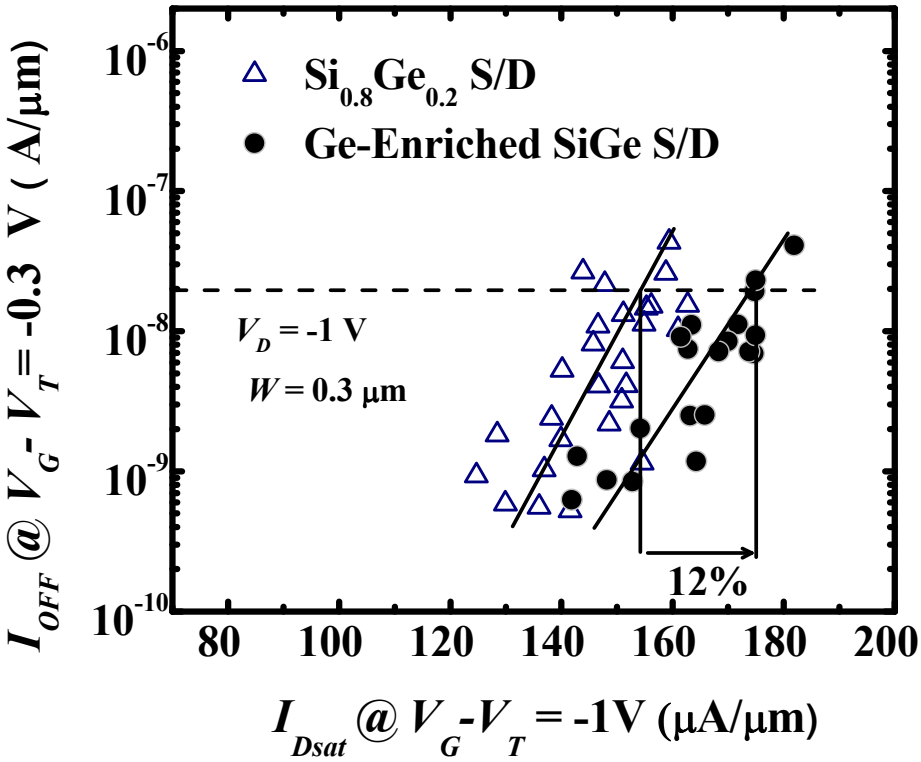


Fig. 2.12. I_{OFF} -I_{Dsat} for laser annealed $Si_{0.8}Ge_{0.2}$ S/D and Germanium enriched S/D p-FETs. At I_{OFF} of 20nA/µm, Ge enriched S/D p-FET shows an I_{Dsat} enhancement of 12% compared to LA $Si_{0.8}Ge_{0.2}$ S/D p-FETs.

For $I_{D,lin}$, a higher enhancement of ~21% was observed for the Ge enriched p-FET compared to LA $Si_{0.8}Ge_{0.2}$ S/D p-FETs (Fig. 2.13) due to the higher sensitivity of $I_{D,lin}$ to mobility enhancement [2.20].

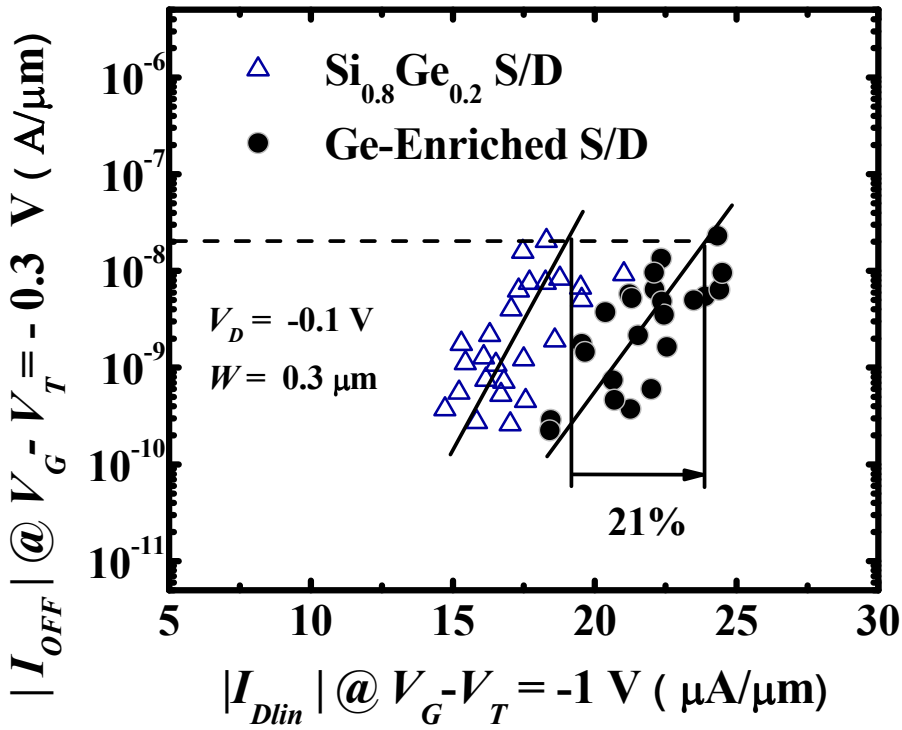


Fig. 2.13. I_{OFF} **-**I_{Dlin} **for laser annealed** $Si_{0.8}Ge_{0.2}$ **S/D and Germanium enriched S/D p-FETs. At** I_{OFF} **of 20nA/μm, Ge enriched S/D p-FET shows an** I_{Dlin} **enhancement of 21% compared to LA** $Si_{0.8}Ge_{0.2}$ **S/D p-FETs.**

In addition, as the laser annealing condition of 290 mJ/cm^2 gives higher dopant activation and lower S/D resistance compared to RTA (900 C, 30s) (Fig 2.14), the Germanium enrichment process has an additional ~9% drive current enhancement compared to an RTA control, as shown in the I_{Dsat}-I_{OFF} plot in Figure 2.15.

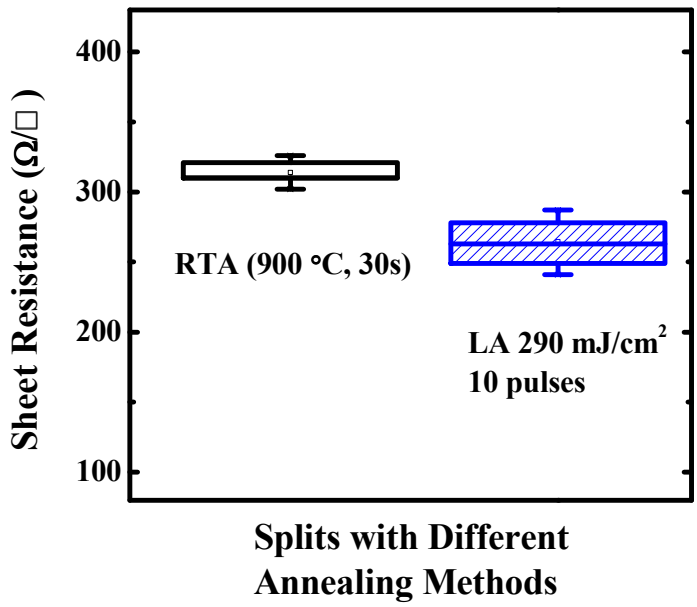


Fig. 2.14. Statistical plot of S/D sheet resistance for LA at 290 mJ/cm^2 and RTA 900 °C 30s. LA at 290 mJ/cm^2 achieves lower sheet resistance compared to RTA. The box contains the middle 50% of data, the top edge of the box indicates the 75th percentile of the data set, and the lower edge of box indicates the 25th percentile.

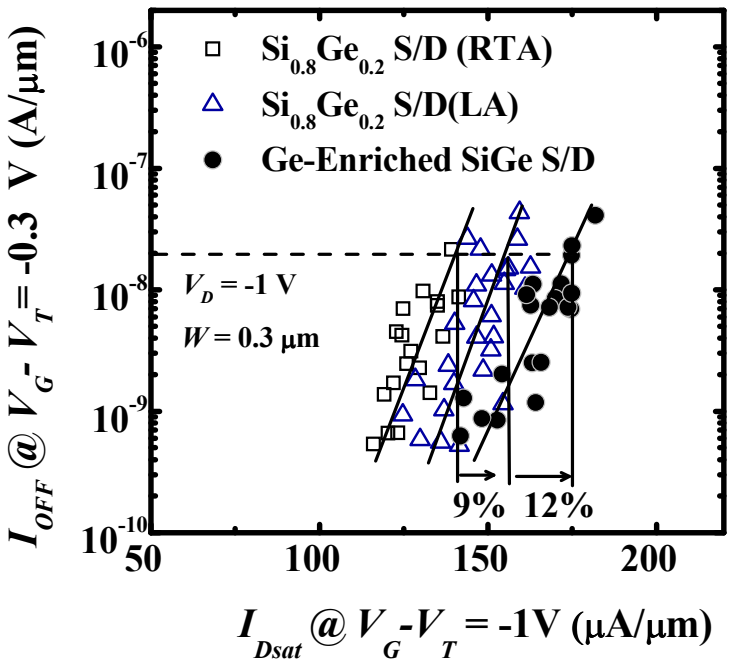


Fig. 2. 15. ***I_{OFF} -I_{Dsat}*** **for RTA annealed $Si_{0.8}Ge_{0.2}$ S/D, laser annealed $Si_{0.8}Ge_{0.2}$ S/D and Germanium enriched S/D p-FETs. Additional drive current enhancement was observed compared to an RTA $Si_{0.8}Ge_{0.2}$ S/D p-FETs due to higher dopant activation.**

I_{Dsat} performance for all these 3 splits is also compared at a given DIBL (Fig. 2.16). At a DIBL of 0.07V/V (DIBL = $\frac{|V_T(V_D=-1)-V_T(V_D=-0.1)|}{1-0.1}$), p-FETs with Ge-enriched graded SiGe S/D demonstrate ~14% improvement over the LA control p-FET, and an additional 10% enhancement compared to an RTA control.

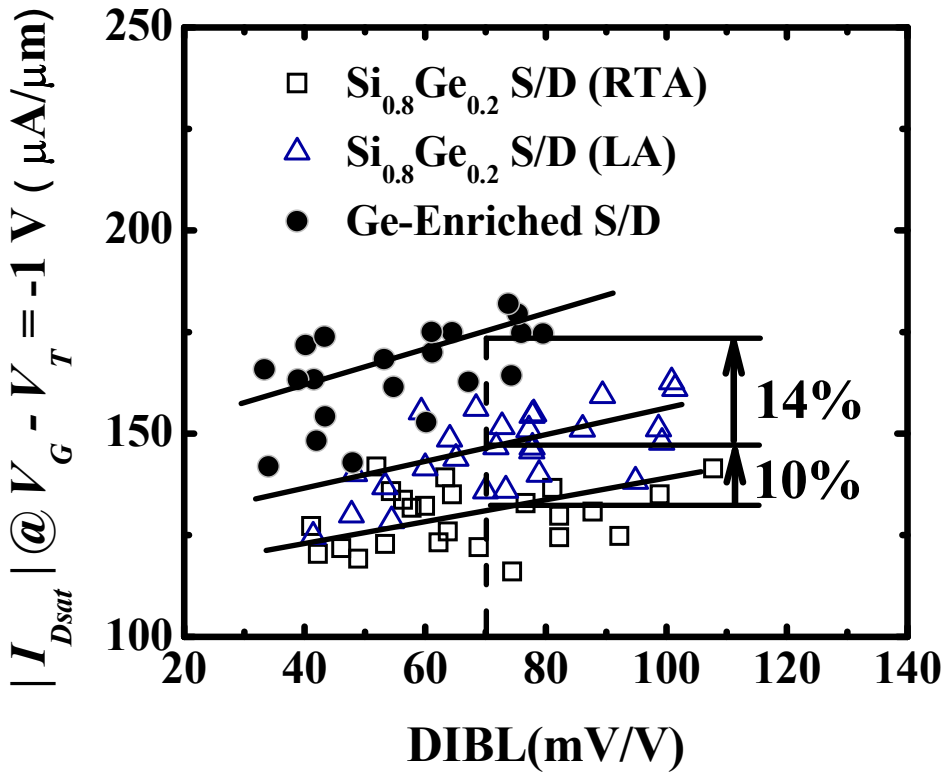


Fig. 2.16 Excellent I_{Dsat} improvement is demonstrated by the novel S/D Ge enrichment process at a comparable DIBL of 70 mV/V.

2.6 Summary

In summary, a new process technology for boosting the Ge content in SiGe source/drain (S/D) stressors was demonstrated to increase strain and performance levels in p-FETs. Selection of laser annealing conditions for device integration was an important issue for this Germanium enrichment process. Using a laser fluence of 290 mJ/cm^2, laser-induced local melting and intermixing of an amorphous Ge layer with an underlying $Si_{0.8}Ge_{0.2}$ S/D region enable the formation of p-FETs with Ge-enriched graded SiGe S/D, giving an I_{Dsat} enhancement of about ~14% over control strained p-FETs with $Si_{0.8}Ge_{0.2}$ S/D at similar short-channel effects and S/D sheet resistance.

2.7 Limitations and Future Work

As the laser spot size is 3mm×3mm, the non-uniformity of the laser fluence at the edge of the spot can causes large device performance variation. Therefore, the amount of overlap between the spots could be of great interest to achieve uniform device performance. Furthermore, as the Ge enrichment achieved using this technique is more pronounced near the S/D surface, silicidation process would consume the top high Ge content SiGe and lead to lost of strain benefits and increase in silicide sheet resistance. Therefore, further process tuning, e.g. using a higher laser fluence, might be needed to achieve a more uniform Ge-enrichment in the S/D. However, with higher laser fluence, melting or rapid thermal expansion of the poly-Si gate sandwiched between spacers can cause gate deformation, and pose integration challenges. Therefore, how to effectively protect the gate line is an important issue.

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CHAPTER 3

Strained P-MOSFETs with Reverse Embedded Silicon-carbon (Si:C) Stressor

3.1 Introduction

As we discussed in earlier chapters, strain engineering is a very promising way to improve transistor performance.

Recently, a new device heterostructure with an embedded SiGe region beneath the Si channel [3.1], also known as strain-transfer structure (STS) [3.2, 3.3] or reverse-embedded SiGe region [3.4], was demonstrated to induce tensile strain in the longitudinal direction of the transistor channel for electron mobility enhancement in nMOSFET. Unlike conventional methods of strain introduction, this approach makes use of the lattice interactions at the vertical heterojunction between the Si regions and the embedded SiGe STS to impart lateral tension to the Si channel. This concept can be combined with other stressors.

In this chapter, we utilize a similar concept and investigate a new structure with only reverse embedded silicon-carbon (Si:C) stressor to impart stress from beneath the channel for p-FET performance enhancement.

3.2 Process Flow and Key Process Steps for Fabricating P-FET with Reverse Embedded Si:C Stressor

Fig. 3.1 shows the schematic drawing of main process steps involved in fabricating a transistor with reverse embedded Si:C stressor.

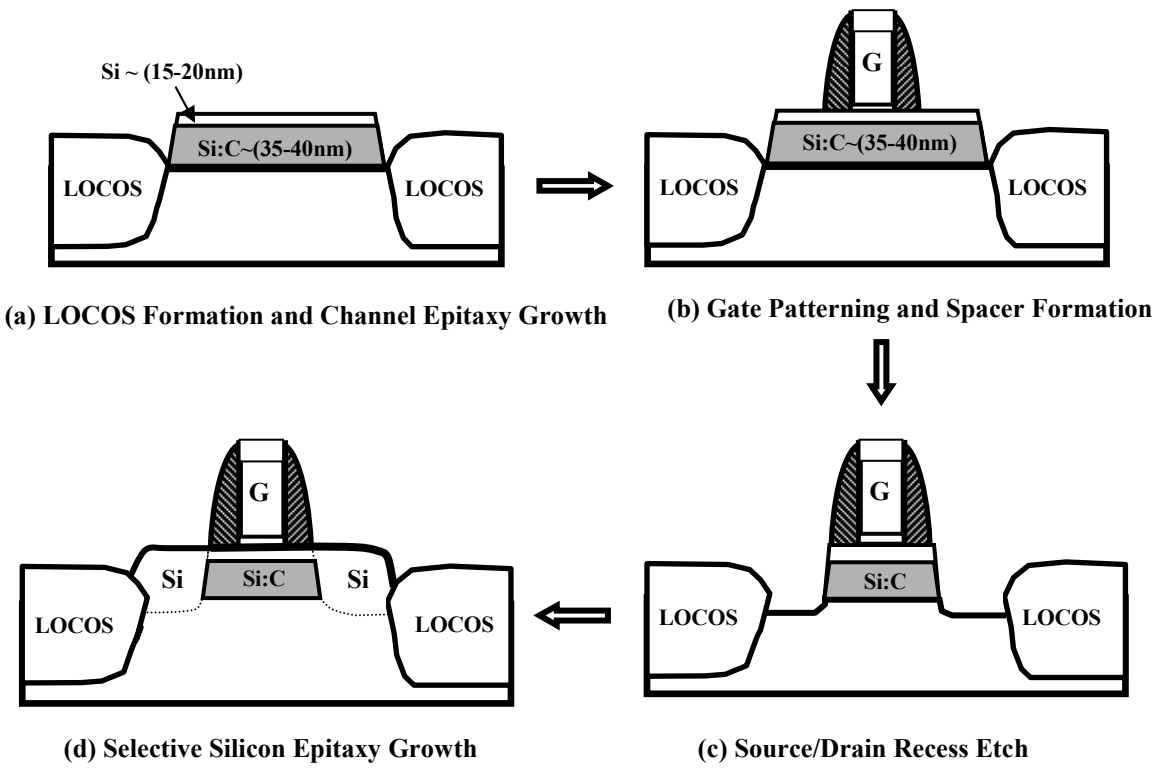


Fig. 3.1. Schematic drawing of key process steps involved in the fabrication flow of p-FET with reverse embedded Si:C stressor. (a) After LOCOS formation and channel epitaxy of Si(15- 20nm) /Si:C(35-40nm) stack (b) After gate patterning and spacer formation. (c) after S/D recess etch. (d) Final device structure after S/D Si selective epitaxial growth.

8-inch bulk (001) Si substrates were employed in the device fabrication. Isolation was first formed using the local oxidation of silicon (LOCOS) process. On a first wafer, silicon-carbon (Si:C) of thickness t_{SiC} ~ 32nm and a thin Si channel layer of thickness t_{Si} ~ 15 nm were grown selectively using ultra-high-vacuum chemical vapor deposition on the active region (as shown in Fig. 3.1 a). On the control wafer, a selective epitaxial growth of Si with thickness of ~50nm was performed to make a fair comparison. After that n-well, punchthrough, and threshold voltage V_T adjust implants were subsequently performed and activated at 900 ºC for 10s.

Gate stack comprised of a thermally grown SiO_2 gate dielectric with a thickness of 3 nm and a SiO_2-hardmask capped the poly-Si gate electrode (100nm) was then formed and patterned. Following that, S/D extension implant, and a ~40nm nitride spacer was formed [Fig. 3.1 (b)]. Then S/D recess etch on all of the wafers was performed [Fig. 3.1 (c)]. An in-situ prebake step at 800 °C for 5 min was carried out to remove the native oxide before the selective epitaxy growth (SEG). S/D implantation was performed and dopant activation was carried out using rapid thermal anneal at 900°C for 10s.

Some critical process steps in making a pFET with reverse embedded Si:C stressors are discussed in following sections.

3.2.1 Channel Epitaxy Growth

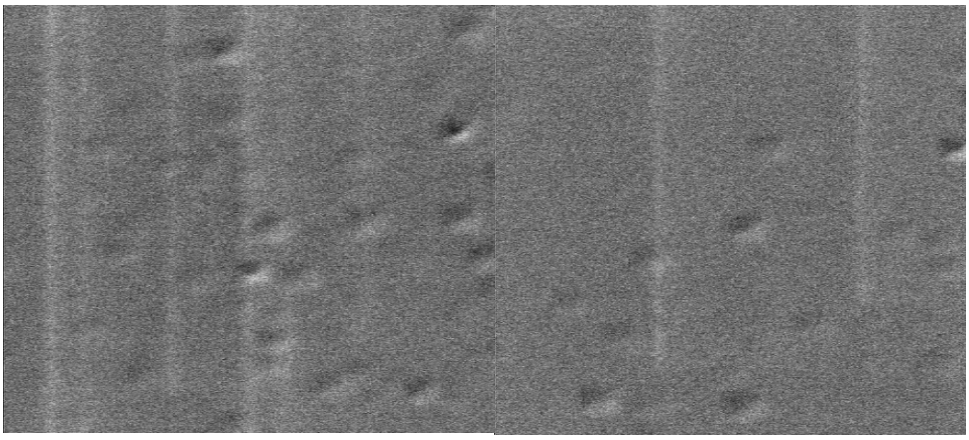
The channel epitaxy process is a very critical step for this process flow. Dilute HF solution was used to remove of any native oxide in the channel regions prior to selective epitaxial growth in an ultra high vacuum chemical vapor deposition (UHVCVD) chamber.

To achieve selective epitaxial growth of Si or $Si_{1-y}C_y$, the epitaxy reactor uses a cyclic process. Each cycle comprising a growth period and an etch period. For selective growth of Si:C, it is achieved by flowing disilane (Si_2H_6) and dilute monomethylsilane (SiH_3CH_3) precursor gases. For Silicon growth step, only disilane was used as the growth precursor gas for the epitaxy growth. A low growth temperature (~640°C) was employed to avoid carbon precipitation. During the growth period, Si or Si:C is first grown on Si with intrinsic selectivity, and after a brief period of time (known as the incubation time), both Si channel region and LOCOS were grown. As the incubation time is often too short for sufficient thickness of epi layers, a

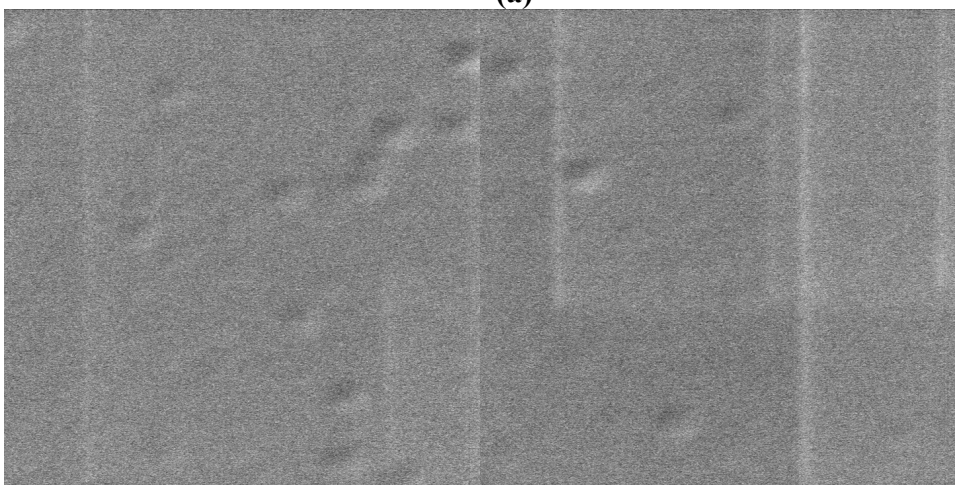
etch step after each growth period is often introduced. The etch step utilizes diluted chlorine (Cl_2) to etch back the islands of Si or Si:C on LOCOS. It also attacks the Si/Si:C grown on the channel region. Due to the Si / Si:C growth rate difference on Si and dielectrics and different etch rate between good crystalline quality Si/Si:C on Si and the polycrystalline Si/Si:C on LOCOS, selective growth is achieved.

For a good selective epi growth, the ratio of the growth and etch back period needs to be maintained within a certain range. An insufficient etch back time would cause lost of selectivity, while too long etch back time will cause an increase in surface roughness due to excessive attack from the chlorine.

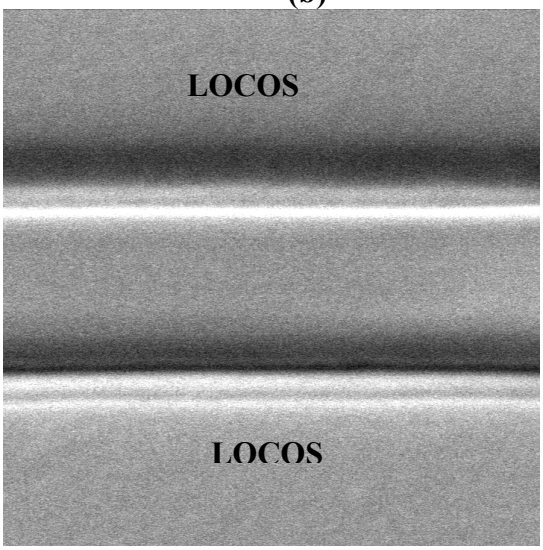
As shown in Figure 3.2 are the SEM images after selective Si channel growth with (a) 60 s Cl_2 etch time /cycle, (b) 56 s Cl_2 etch time /cycle, and (c) 53 s Cl_2 etch time/cycle at a fixed disilane (Si_2H_6) precursor flow time of 20 s/cycle. It is observed that with the reduced Cl_2 etch time per cycle, density of surface pits reduces. With 53 s/cycle Cl_2 flow time, a smooth surface was achieved and it also maintained a good selectivity towards oxide.



(a)



(b)



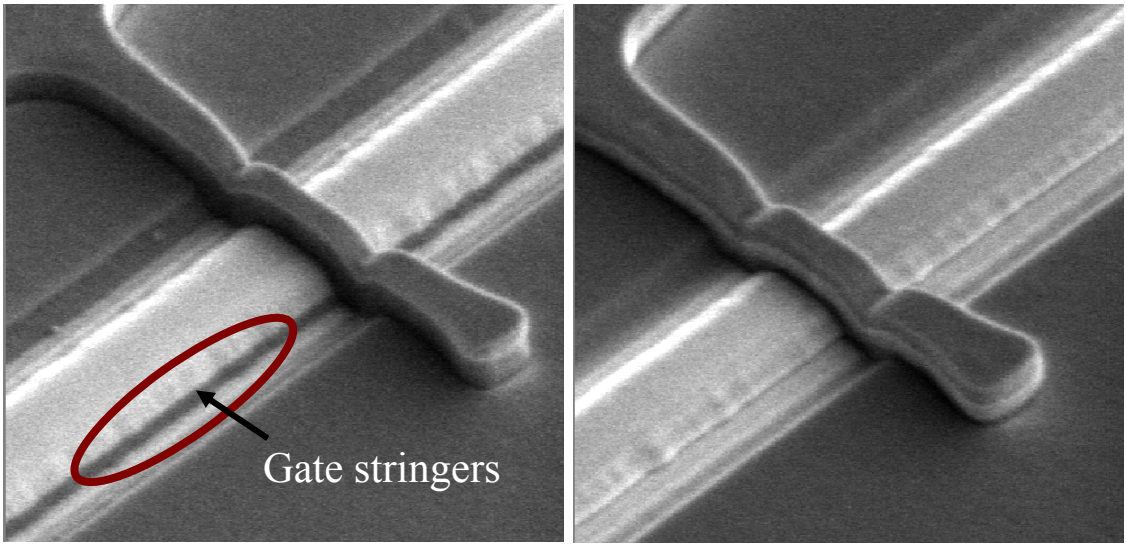
c)

Fig. 3.2. SEM images after selective epitaxy growth of Si with different Cl_2 etch time and fixed disilane (Si_2H_6) precursor flow time of 20s/cycle. (a) with 60s Cl_2 etch time/cycle, (b) with 56s Cl_2 etch time /cycle, and (c) with 53s Cl_2 etch time/cycle.

3.2.2 Gate etch

Gate etch process for a p-FET with STS structure also needs extra attention. Due to the raised channel region, the morphology would leave a gate stringer at the sidewall of channel region if extensive over etch is not performed. These gate stringers remaining at the sidewall of LOCOS or raised channel region would cause short circuit between gate and S/D during subsequent S/D epitaxy growth or silicidation.

To remove the stringers completely without etching through the gate oxide, a improved $HBr/Cl_2/He/O_2$ plasma etch process described in [3.5] is used. Figure 3.3 shows the SEM images after gate etch with a) conventional gate etch recipe for planner devices and b) improved gate etch with 75% HBr in Cl_2/HBr gas as described in [3.5].



(a) **(b)**

Fig 3.3. SEM images after gate etch. Extensive over-etch is required to remove the gate stringers remaining at the sidewall of raised channel. (a) SEM image of STS device after gate etch with conventional etch process for planner devices. (b) SEM image for gate etch using improved gate etch recipe with 75% HBr in Cl_2/HBr gas mixture. Stringers removed without etching through gate oxide.

3.3 Selection of Annealing Conditions for Minimizing Carbon Precipitation and Strain Relaxation

As the Si:C stressors are grown at the early stage of a transistor fabrication, after several thermal cycles, relaxation of Si:C with C precipitation might occur. The main process steps causing Si:C relaxation would be n-well and S/D activation steps, which usually requires high temperature above 800 ºC. Thus, in this section, we investigate the effect of temperature and annealing time on strain relaxation and C precipitation in the embedded Si:C. This serves a guideline for selection of annealing conditions.

To determine the subsitutional carbon content (C_{sub}) in the buried Si:C stressor, HRXRD scans were performed on blanket samples with Si(15nm) on Si:C(32nm) stack grown on Si substrate after threshold V_T adjustment, punchthrough and well implants and different annealing conditions (Fig. 3.4).

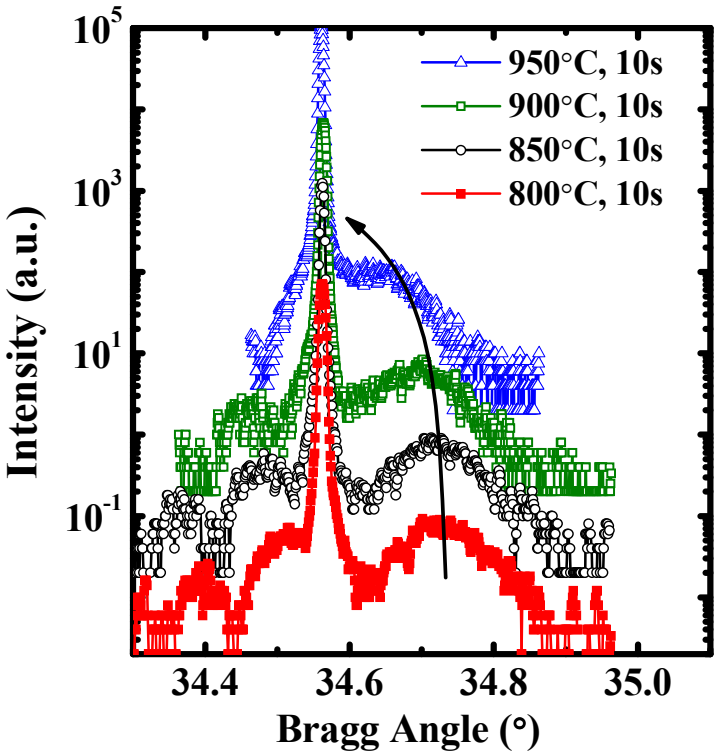


Fig. 3.4. HRXRD of Si(15nm)/Si:C((32nm) grown on Si substrate after V_T, punch through, and well implants and annealing. The Si:C satellite peaks shift towards Si substrate peak with increasing annealing temperature indicates a decrease in substitutional Carbon content (C_{sub}) with increasing annealing temperature.

The displacement of satellite peaks from Si substrate peak (change in Bragg angle) due to the Si:C layer is proportional to the subsitutional Carbon content in the epi layer. It is observed that the Si:C satellite peak shifts to lower angles, closer to Si substrate peak, with increasing annealing temperature, which indicates a drop in subsitutional carbon content (C_{sub}).

To determine the C_{sub} in the buried Si:C after each annealing condition, simulations are done to match the experiment results. For example, Figure 3.5 shows the simulated HRXRD curve for Si(15nm)/ $Si_{0.992}$:$C_{0.008}$(32nm) on Si substrate, which matches well with the experimental result obtained after annealing at 850 ºC for 10s.

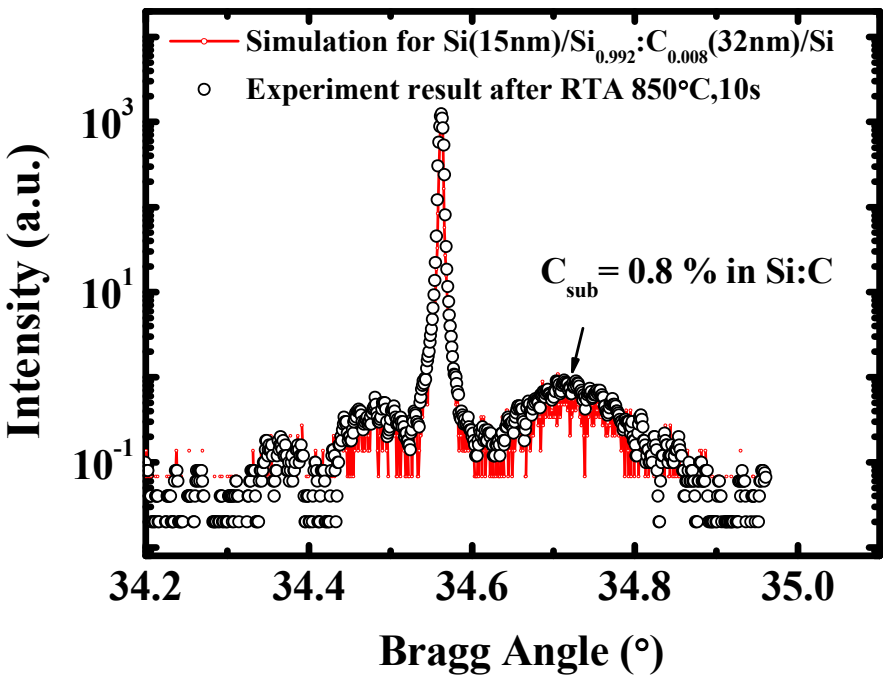


Fig. 3.5. Simulation of HRXRD spectrum for Si(15nm)/$Si_{0.992}$:$C_{0.008}$(32nm) stack grown on Si substrate shows a good agreement with the experiment result after annealing at 850 ºC for 10s. C_{sub} in the buried Si:C layer is thus determined to be 0.8 atomic percent with this annealing condition.

Therefore, the C_{sub} in the buried Si:C after annealing at 850 ºC for 10s is approximately 0.8 atomic percent.

We then plot the C_{sub} vs. annealing temperature (Time is 10s for each anneal split) in Figure 3.6. A steeper drop in C_{sub} was observed with temperature higher than 900 ºC.

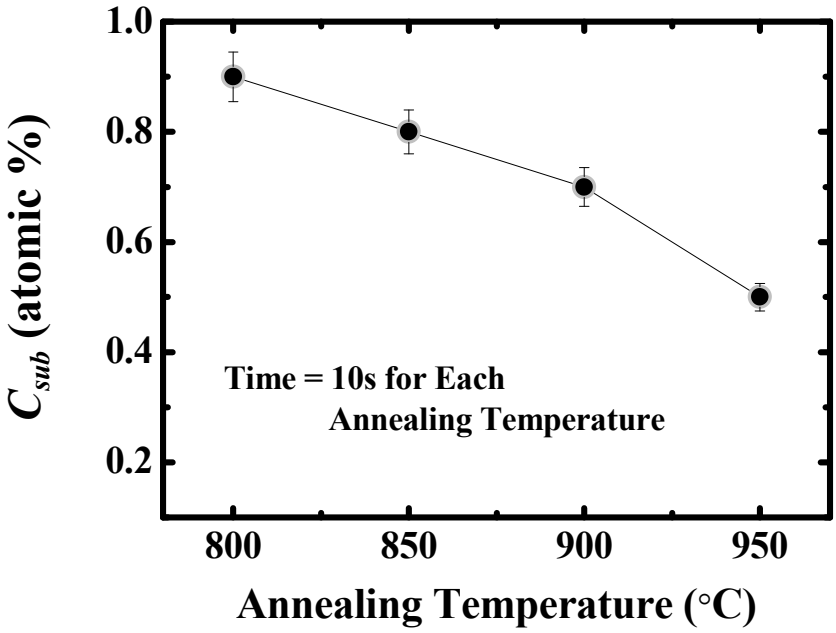


Fig. 3.6. C_{sub} vs. annealing temperature. A drop in C_{sub} is observed with increasing temperature, indicating that more C atoms diffuse from substitutional sites into interstitial sites with increasing annealing temperature. Thus, the use of high temperature process should be avoided for structures with Si:C stressors.

Another parameter which affects the C_{sub} is annealing time. With increasing annealing time at 900 ºC, the C_{sub} drops from 0.7 at. % for 10s anneal, to 0.6 at. % for 30s anneal (as seen from Fig. 3.7).

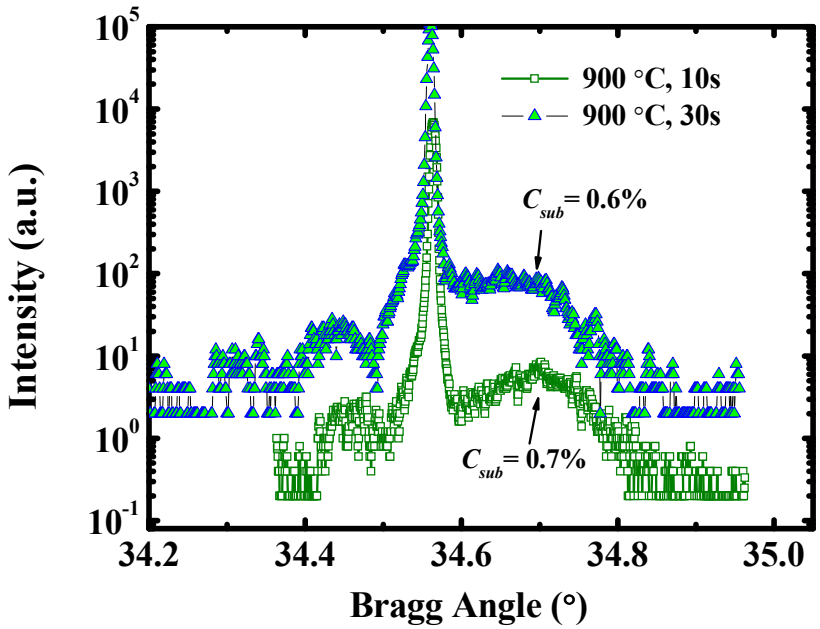


Fig. 3.7. HRXRD rocking curves of implant and annealing Si(15nm)/Si:C (32nm) epi layers grown on Si substrate. The substitutional C content drops from 0.7 atomic percent with 10s anneal to 0.6 atomic percent for 30 s anneal.

The substitutional carbon content after different annealing conditions are summarized in Table 3.1. This can serves as a guideline when choosing S/D annealing conditions in device fabrication. The annealing condition used in this study is 900 ºC, 10s, which has a C_{sub} of approximately 0.7 atomic percent.

Table 3.1. Summary of C_{sub} after different annealing conditions.

Annealing Temperature (ºC)	Time (s)	C_{sub}(atomic %)
800	10	0.9
850	10	0.8
900	10	0.7
900	30	0.6
950	10	0.5
1000	1	0.7

3.4 Device Characteristics and Strain Measurement

Figure 3.8 shows the TEM image of a p-FET with reverse embedded Si:C stressor beneath the channel. The gate length of this device is around 90 nm.

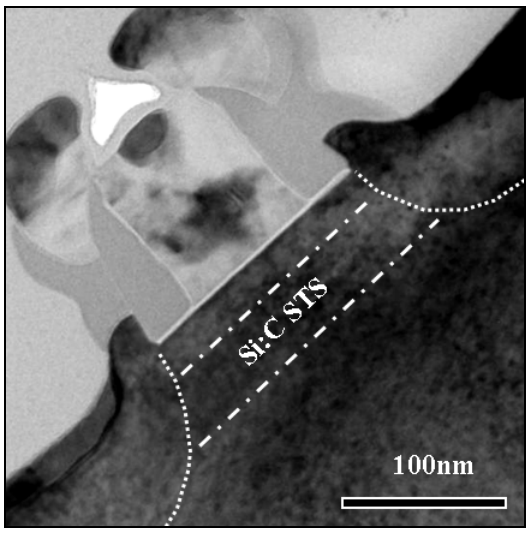


Fig. 3.8. TEM image for device with Si:C strain transfer structure.

S/D annealing at 900 ºC for 10s was performed for all the devices. Figure 3.9 shows the I_S-V_G plot of typical devices with Si epi channel and reverse embedded Si:C stressor. It is observed that generally, devices with Si:C STS has higher I_{OFF} . This could be attributed to higher source to drain leakage current which is caused by defects along the channel region shown in the insert. These defects could be caused by poor quality of the epitaxy growth, or formed by implantations and subsequent annealing. In addition, it is observed that the sub-threshold swing (SS) of devices with Si:C strain transfer layer is degraded compared to the Si control device. This could be due to the diffusion of C atoms to the oxide interface which degraded the oxide quality. This issue could be solved by increasing the thickness of Si channel epi layer.

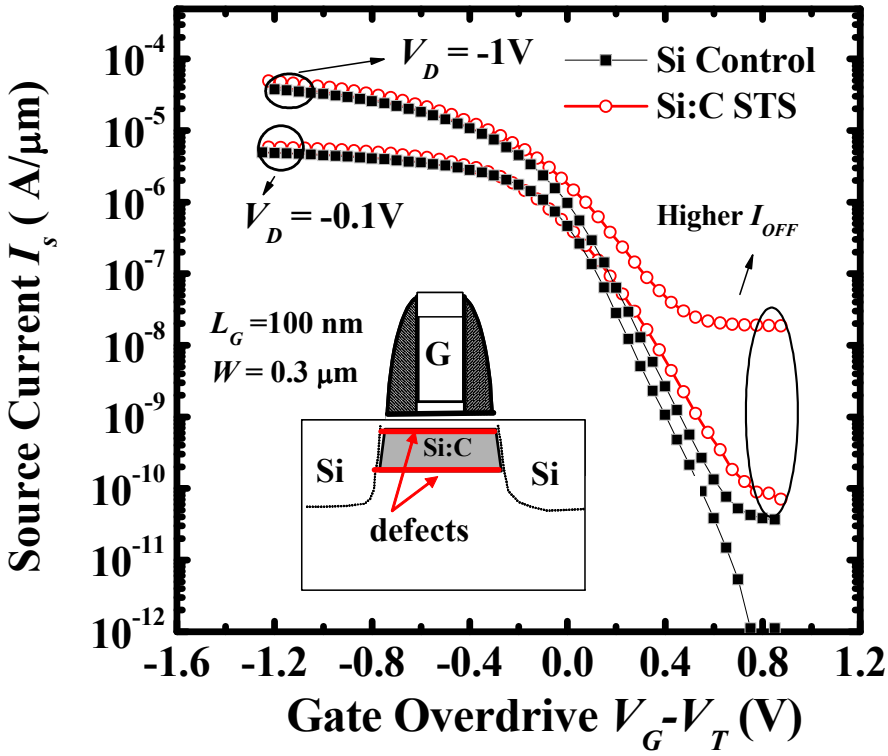


Fig. 3.9. Typical I_S-V_G plot of devices with Si epi channel and reverse embedded Si:C stressor. Higher source current was observed for devices with strain transfer structure. This could be due to defects along the channel as depicted in the inset.

Direct measurement of channel strain using UV Raman analysis was also performed on blanket samples with Si(15nm)/Si:C(32nm) on Si substrate after implantations and annealing.

A 325nm He-Cd laser was used to measure the strain in top Silicon epitaxy layer (The probing depth of the UV Raman is around 10nm in Si). To avoid down shift of the Si-Si peak caused by laser heating, the laser power on the samples surface was kept to be less than 250 microwatt. Since the spectral resolution of the UV Raman is only 0.6 cm^{-1}, a fit by Lorenztian function was used to extract the peak position.

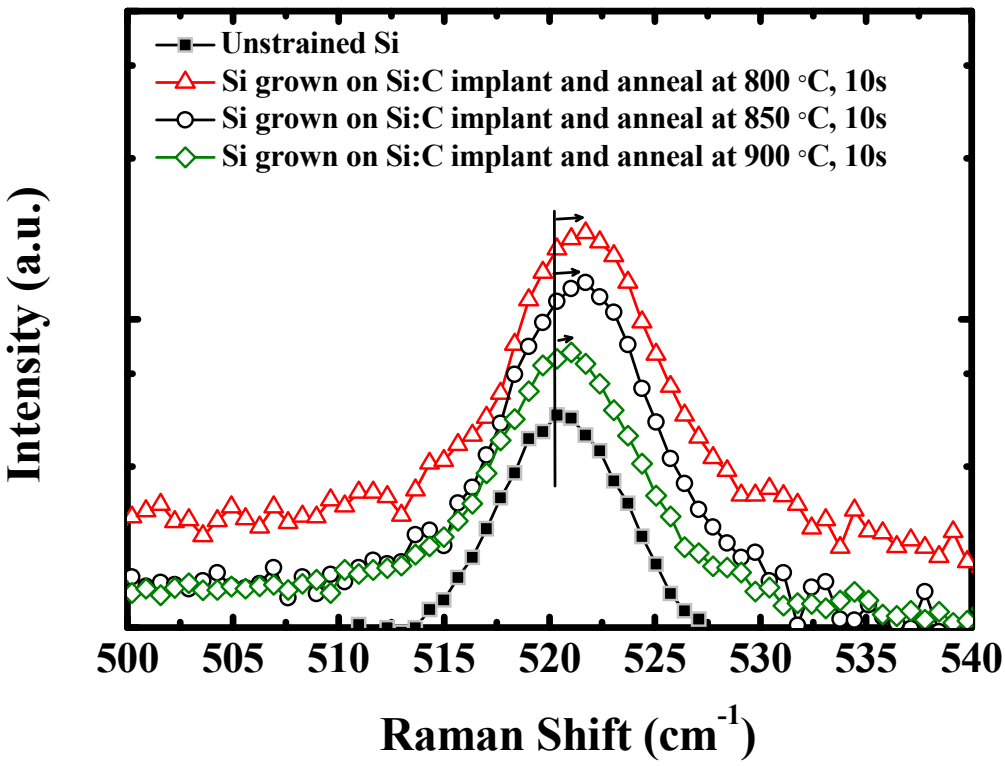


Fig. 3.10. UV Raman analysis of Si grown on Si:C after implantations and annealing. The probe depth of UV Raman is within the top Si epi layer. The strain in Si is proportional to the extent of red shift from the unstrained Si peak.

Figure 3.10 shows the locations of Si peaks in the top Si epi layer after implantations and different annealing conditions.

A theoretical calculation of strain was performed assuming the Si is grown on fully relaxed Si:C with carbon concentration of C_{sub} (measured from HRXRD). And this was compared to the UV Raman measured compressive strain for each annealing condition in Table 3.2.

It is observed that the actual strain level measured by UV Raman is much smaller than that of the theoretical calculation.

There are several reasons behind.

Firstly, due to thin layer of Si:C growth(~32 nm) on Si, the Si:C layer is not fully relaxed. The Si:C lattice conforms to the Si substrate template with partial relaxation, therefore during subsequent Si channel epitaxy growth, less strain is experienced in the top Si layer compared to the case of Si growth on fully relaxed Si:C.

Another possible reason is that, due to the defects at Si/Si:C interface by epi growth or defects caused by implantation and annealing, the strain level in the top Si epi layer drops further.

Table 3.2 Summary of calculated strain and measured strain by UV Raman Spectroscopy

Annealing Temperature (^{o}C)	Time (s)	C_{sub} measured from XRD	Theoretical strain for Si grown on fully relaxed Si:C	Strain measured by UV Raman
800	10	0.9	0.30%	0.13%
850	10	0.8	0.27%	0.10%
900	10	0.7	0.24%	0.03%

To improve the transistor performance, the thickness of Si:C strain transfer layer could be increased, and the usage of high thermal budget process should be avoided.

3.5 Summary and Future work

P-FET with reverse embedded Si:C stressor beneath the channel was fabricated. The process related issues are discussed, however, the performance of these devices are poor due to high source drain leakage current and poor SS. This could be due to low epitaxy quality, C precipitation and diffusion, and/or strain relaxation of Si:C during subsequent implantation, and thermal processes.

To further improve the device performance, the epitaxy Si:C quality needs to be improved, and thermal budget after this epitaxy process needs to be kept low. In

addition, for channel epitaxy, we could also adopt insitu doped Si channel and insitu doped Si:C strain transfer layer to minimize defects and strain relaxation caused by subsequent implantation and annealing processes.

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CHAPTER 4

Stress by Boron Doping in P-channel Devices and Strain Compensation Implant

4.1 Introduction

As we know, besides the strain generated by lattice mismatched epitaxy layers, when a dopant atom is introduced into silicon substrate through ion implantation or diffusion, a local lattice expansion or contraction will occur depending on the varying atomic sizes and bond lengths of the atoms. Boron, widely used as a dopant in the p-FET S/D, with a small covalent radius of 0.9 Å, introduces lattice contraction in Si when it is in substitutional sites [4.1]

Nowadays, nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs) require heavily doped ultra-shallow source/drain extensions for good control of short-channel effects and superior drive current performance. These shallow, yet highly activated implants can be achieved by laser anneal, which activates dopants to concentrations exceed their solid solubility [4.2-4.4]. For p-FETs, ultra shallow and highly activated boron is desired in the S/D and S/D extension region. However, a layer of Si supersaturated with boron has a smaller over-all lattice constant than Si, and when formed in source and drain extension regions in a p-channel transistor, this can cause undesirable tensile strain in the channel and lead to p-FET performance degradation (Fig. 4.1). The stress induced in the channel due to boron doping was insignificant for long-channel devices, but for CMOS transistor channel lengths in the nanometer realm, this stress could play a significant role in determining the carrier mobility.

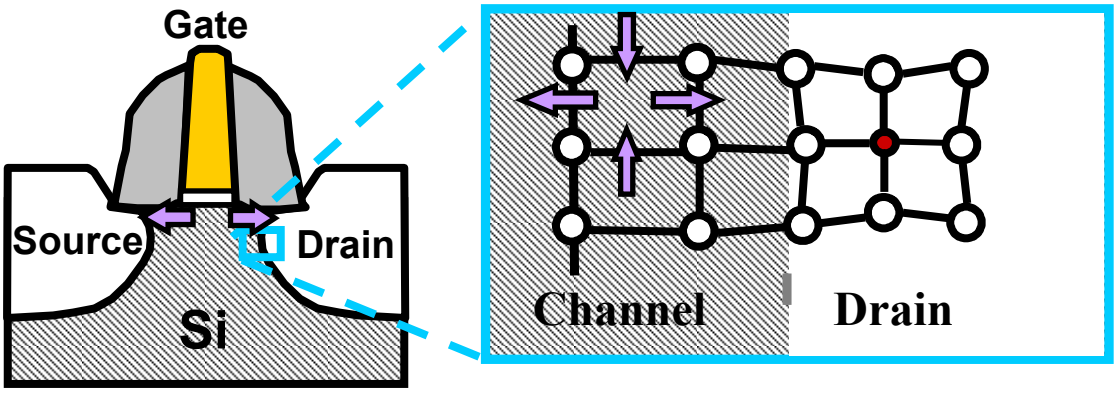


Fig. 4.1. Schematic drawing of Si transistor with high concentration of Boron doping in the S/D. In the S/D region boron doping causes local lattice contraction. The overall lattice constant of S/D is reduced, and a tensile strain in the channel along the carrier transport direction is introduced.

In addition, though a highly activated boron profile is desirable in the S/D and S/D extension of a p-FET for lower series resistance and higher drive current performance, the retention of supersaturated boron produced by laser annealing is difficult during subsequent thermal processes. The mechanism of deactivation was suggested to be high strain energy caused by local contraction of Si lattice with boron doping, which accelerates the injection of Si interstitials [4.5], and makes the retention of high boron concentration difficult.

Therefore, the stress generated due to boron doping can cause undesirable performance degradation of p-FET performance, and it is a case of technical importance.

In this chapter, we discuss the effect of tin (Sn) strain compensation implants, and its effects on reducing the local strain energy and enhancing boron's thermal stability. Tin was chosen as the strain compensation implant, as it is a group-IV element with a large covalent bond radius of 1.4 Å. Sn, when incorporated in Si,

contributes to an increase in lattice constant, which counteracts the contraction of lattice constant caused by a high concentration of boron.

4.2 Experiments

N-type bulk Si wafers were used in this experiment. A 10 nm sacrificial silicon oxide was deposited prior to ion implantation of BF_2 at a dose of 6×10^{15} ions/cm^2 with an energy of 8 keV (7˚ tilt).

Sn co-implantation at 15 keV with a dose of 2×10^{14} cm^{-2} and 1×10^{15} cm^{-2} was performed for some wafers. The Sn co-implant was skipped for a control wafer. P-N diodes were also fabricated with the same implantation conditions to monitor the leakage current of the junctions. Laser annealing was carried out in nitrogen ambient using a 248 nm KrF excimer laser with full-width half-maximum pulse duration of 23 ns. The laser fluence was varied from 670 mJ/cm^2 to 800 mJ/cm^2 to melt the Sn- and B- implanted layer on the Si surface.

4.3 Strain Compensation with Sn Implants

The strain for control and Sn co-implanted wafers after laser annealing are measured through high resolution x-ray diffraction (HRXRD).

In the x-ray rocking curves shown in Figure 4.2, the satellite peak from the boron-implanted layer (with no Sn implant) has a larger Bragg angle than the Si (004) peak, showing a lattice constant that is smaller than Si, which indicates tensile strain in the top boron doped film. With increasing Sn dose, the satellite peak shifts towards Si substrate peak, demonstrating that Sn incorporation has increased the lattice constant and relieved the tensile strain in the top boron doped Si layer.

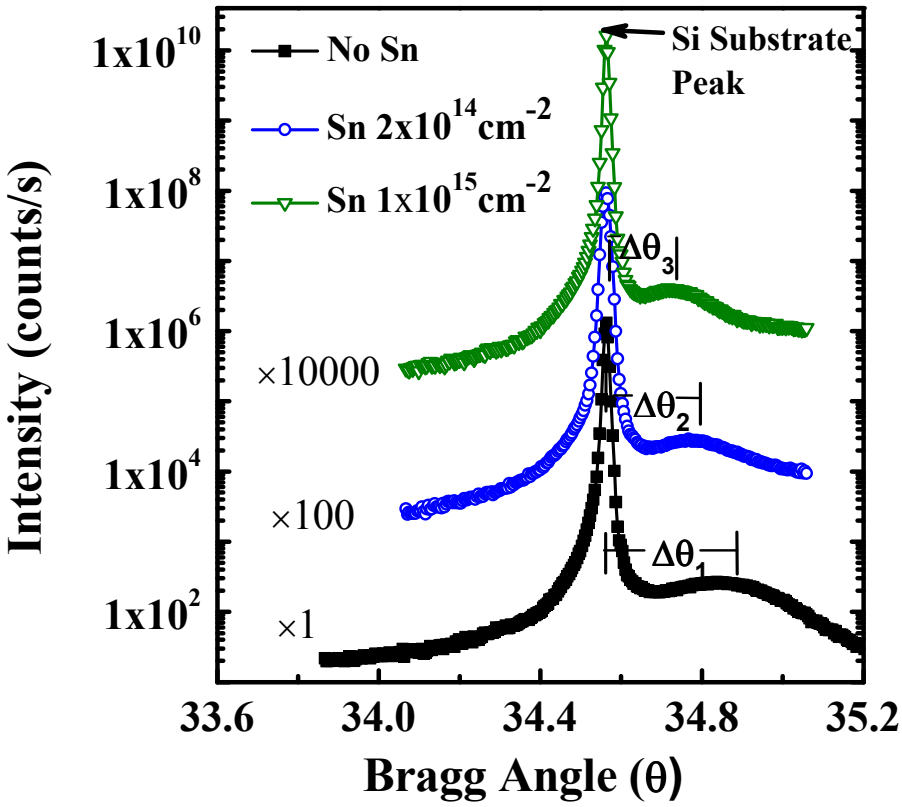


Fig. 4.2. High Resolution XRD rocking curves measured after laser annealing. The satellite peak from Boron implanted film has a larger Bragg angle than the Si (004) substrate peak, showing a lattice constant smaller than Si, which indicates a tensile strain in the film. The satellite peak shift towards silicon substrate peak with increasing Sn dose demonstrates the tin incorporation has indeed relieved the strain formation in the boron doped silicon layer.

The stress (strain) calculation is based on the change in the interplanar spacing Δd which will produce a corresponding change in the Bragg angle, $\Delta\theta$, such that lattice expansion in normal direction could be obtained by [4.6, 4.7]

$$(\Delta d/d) = (\cot\theta)\cdot\Delta\theta, \qquad (4\text{-}1)$$

where d is the unstrained lattice spacing, and $\Delta\theta$ is the change in Bragg diffraction orientation due to the strain. When a film is biaxially stretched to adopt the lattice parameter of the substrate and consequently contract in the direction perpendicular to the film, this tetragonal distortion can be obtained according to the pseudomorphic lattice growth mismatch formula, and the change of the alloy lattice constant ($\Delta a/a$) is related to the lattice contraction in normal direction by [4.8]

$$\frac{\Delta a}{a} = \frac{C_{11}}{C_{11} + 2C_{12}} \times \frac{\Delta d}{d}, \tag{4-2}$$

where C_{11}=16.577×10^{11} dynes/cm^2, and C_{12} =6.39×10^{11} dynes/cm^2 are the elastic moduli of Si.

The satellite peaks for laser annealed samples with 0 cm^{-2}, 2×10^{14} cm^{-2}, and 1×10^{15} cm^{-2} Sn implant dose are located at 0.31, 0.22, and 0.16 degree, respectively, above the silicon substrate peak, which correspond to $\frac{\Delta d}{d}$ of 0.78%, 0.55%, and 0.403%, respectively. Therefore, the lattice strain in the top Boron doped layer, i.e. $\frac{\Delta a}{a}$, for those samples is equal to 0.44%, 0.31%, and 0.227%, respectively. Therefore, the Sn co-implantation has indeed successfully compensated the strain caused by boron implant.

4.4 Boron's Thermal Stability with Strain Compensation Implants

The local lattice contraction caused by Boron doping may increase the strain energy in the lattice and make the retention of high concentration Boron difficult

during subsequent thermal cycles. Thus, in this section, we investigate the effect of Sn strain compensation implant on Boron's thermal stability, and explain the physics behind the observed phenomenon.

4.4.1 Motivation for Post LA Rapid Thermal Anneal

Figure 4.3 shows the B and Sn depth profiles in three samples with various Sn doses (0, 2×10^{14}, and 1×10^{15} cm^{-2}) which were laser-annealed at a laser fluence of 740 mJ/cm^2. The top surface comprising the B- and Sn- implanted layer (~ 15 nm) was melted and re-crystallized, as evident from the flat boron profile in the top region.

However, residual defects, such as stacking faults, dislocation, or end-of-range damage, that were not removed by LA or secondary defect generated during laser annealing can be detrimental and can drastically increase the leakage current when the defects are situated in the depletion region of the junction. Figure 4.4 shows the diode characteristics of the p+/n junction formed by laser annealing at 740 mJ/cm2, 1 pulse, 5 pulses, and 10 pulses. A high reverse leakage current was observed for diodes after a single pulse laser annealing indicating high density of electrical active defects in the depletion region.

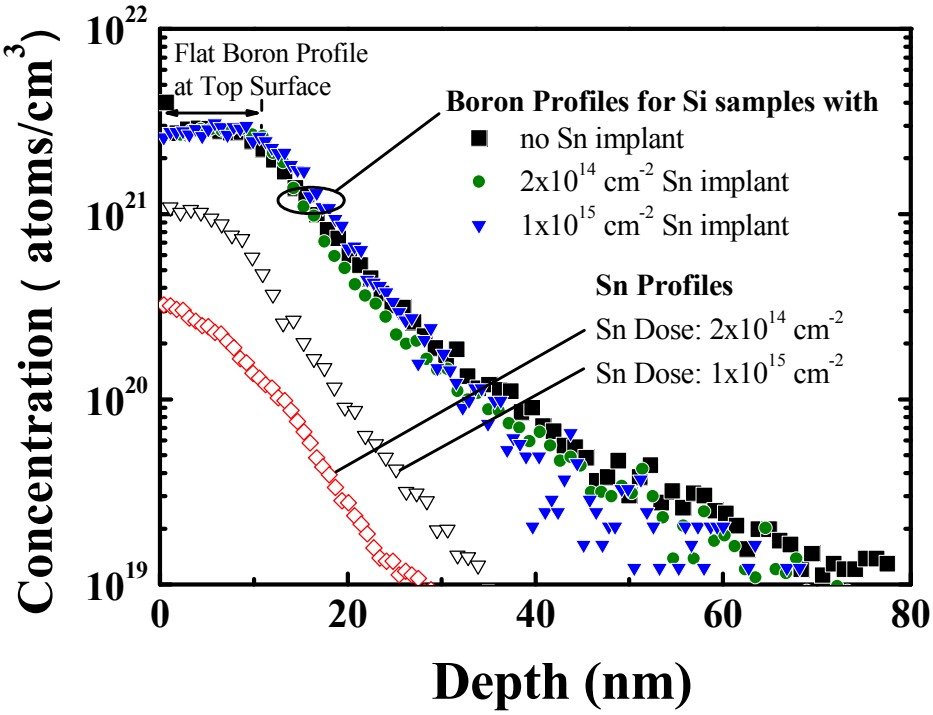


Fig. 4.3. SIMS profile of boron and tin after laser annealing at a laser fluence of 740 mJ/cm^2. The laser light melts the top layer which was implanted with B and Sn. A flat boron distribution in the top layer was observed. Similar boron profiles were obtained for samples with various doses of Sn implanted.

By increasing the number of pulses, eg. from 1 pulse to 5 pulses, or 10 pulses, the reverse leakage current reduces. However, the diode characteristics still suggest that there are large amount of remaining crystalline defects at the p/n junction.

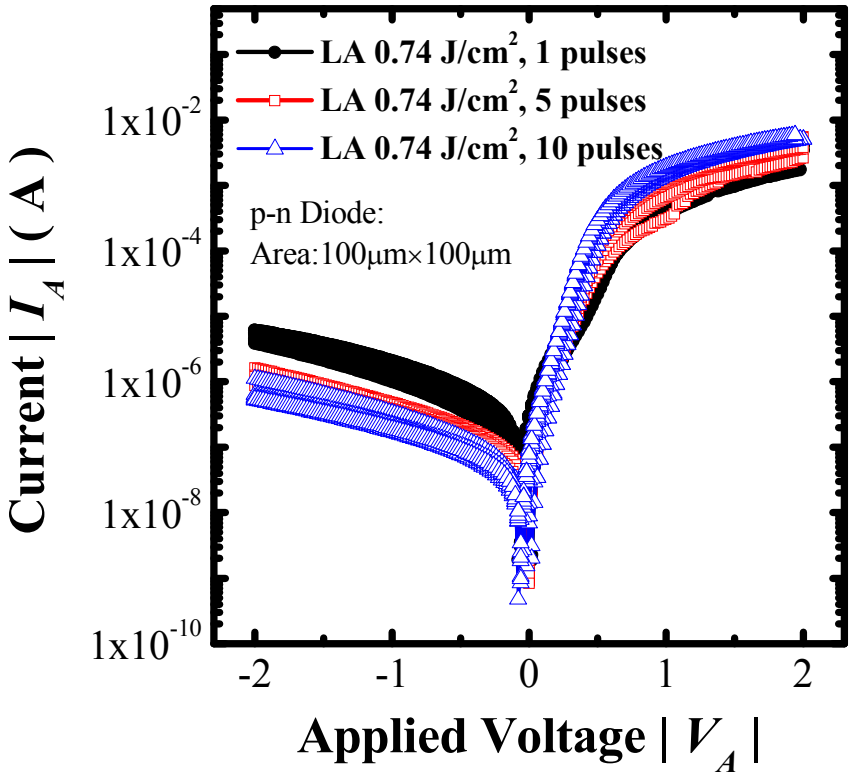


Fig. 4.4. *I-V* characteristics of p+/n junction subjected to laser annealing of 740 mJ/cm^2 with 1 pulse, 5 pulses, or 10 pulses.

To further reduce the electrically active defects, a post laser annealing RTP was carried out at 700 ºC for 20 s. The post-LA RTP conditions were chosen such that no observable diffusion of boron would occur [4.9]. Characterization of diodes shows that the post-LA RTP at 700 ºC for 20 s significantly reduced the leakage current, as seen in Figure 4.5, and Figure 4.6. Without the post-LA RTP, the junction leakage current is ~4 orders of magnitude higher. Therefore, the post laser annealing RTP has effectively reduced the electrical active defects.

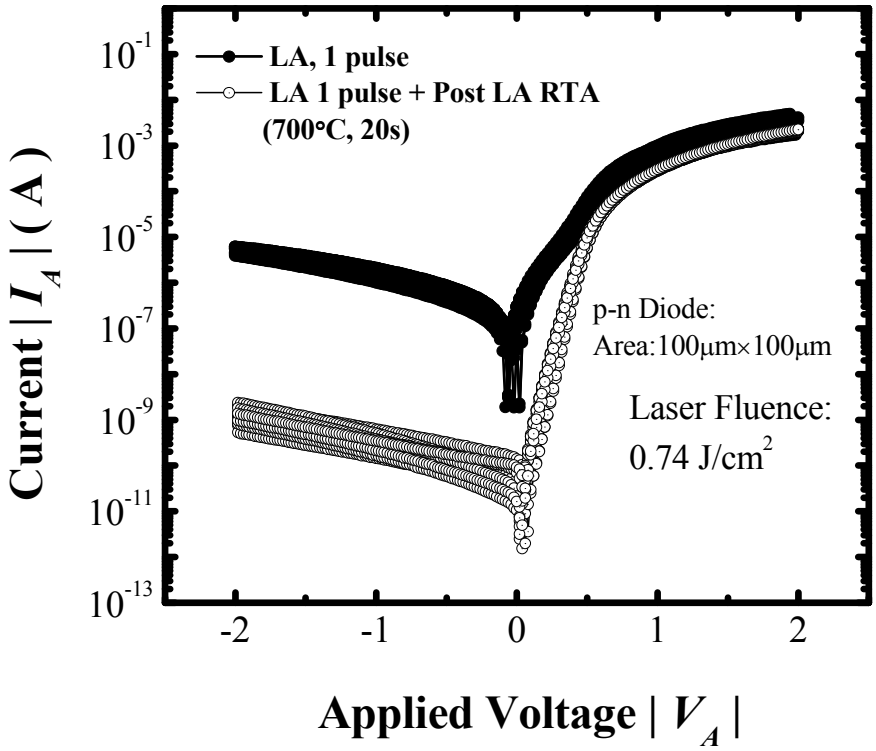


Fig. 4.5. ***I-V*** **characteristics of p+/n junction subjected to laser annealing of 740 mJ/cm^2 only and laser annealing of 740 mJ/cm^2 followed by an RTA of 700 ºC for 20s.**

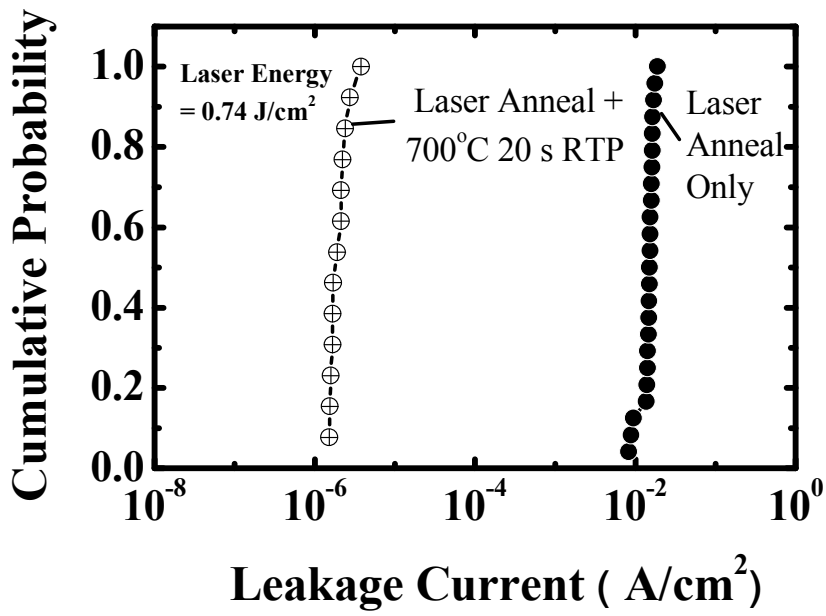
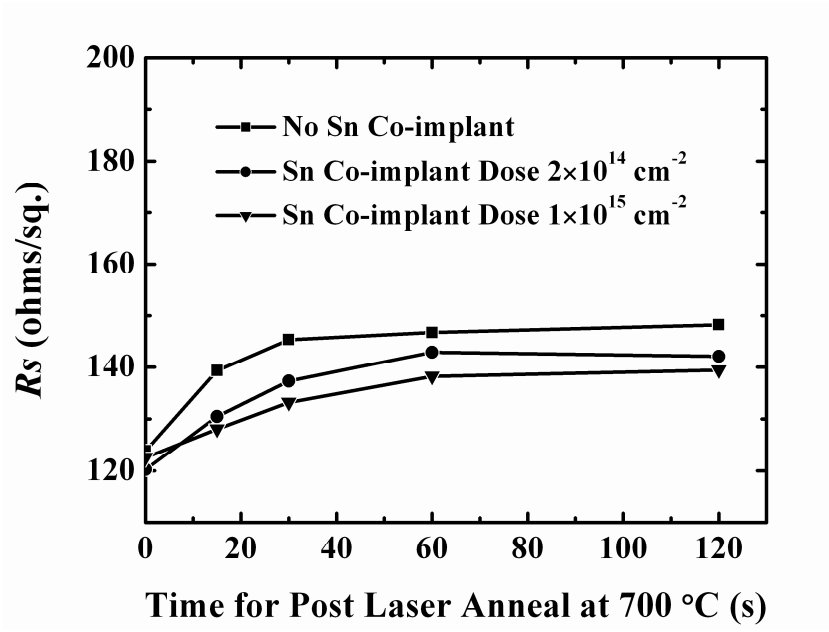


Fig. 4.6. Distribution of diode leakage current for BF_2 implanted n-type wafer before and after post laser annealing rapid thermal processing (RTP). More than 15 diodes were characterized for

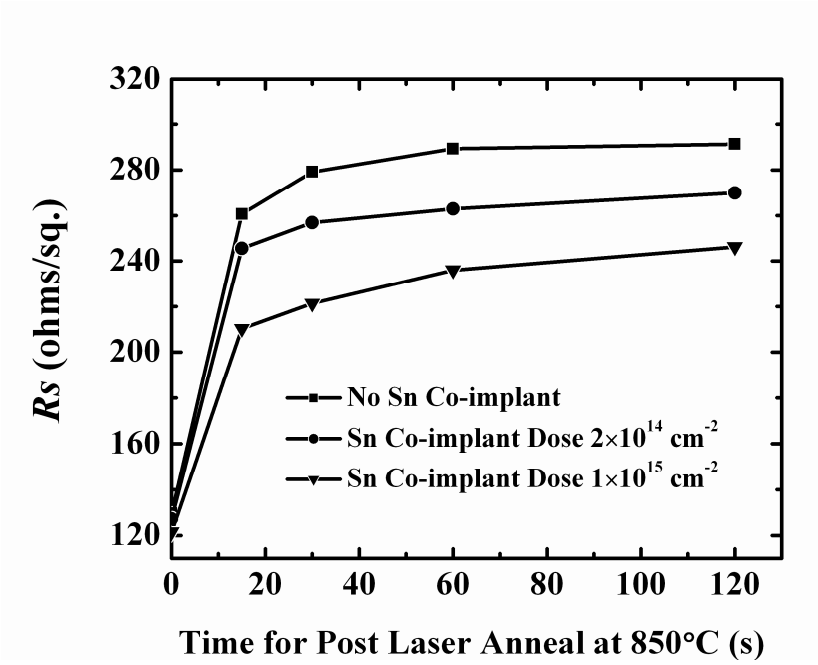
each curve to get cumulative results. The post LA RTP condition was 700 °C for 20 s, which significantly reduced the leakage current.

4.4.2 Boron's Thermal Stability

In order to study the effect of Sn strain compensation implant on boron's thermal stability, samples with only Boron implant, and samples with both Boron and Sn implantation were subject to RTP at a temperature of 700 ºC or 850 ºC for a duration ranging from 15 to 120 s in a nitrogen ambient after laser annealing. The sheet resistance R_S of these samples was monitored vs. annealing time at a post LA-RTP temperatures of 700 ºC [Fig. 4.7(a)] and 850 ºC [Fig. 4.7(b)].



(a)



(b)

Fig. 4.7. Sheet resistance *Rs* increases as a function of time for (a) post laser annealing at 700 ºC, and (b) post laser annealing at 850 ºC. Suppressed increase in R_S with increasing dose of co-implant was observed.

Time-dependent electrical deactivation of B was observed as R_S increases with increasing t. The deactivation occurs even with a post-LA RTP time as short as 15 s. For samples without Sn implant, this increase in R_S with t is the most rapid. This fast deactivation process relates to the transfer of boron atoms from substitutional to interstitial lattice sites, releasing strain energy in the tensile strained layer comprising supersaturated boron. With the incorporation of Sn, the rate of increase of R_S with t is reduced. In addition, a higher Sn dose causes the value of R_S to settle at a lower value even with extended anneal time, suggesting that Sn stabilizes the deactivation of electrically active B.

For post-LA RTP condition of 850 ºC for 120 s, the R_S values for a sample without Sn co-implant and a sample implanted Sn at a dose of 1×10^{15} cm^{-2} are ~290 Ω/square and 246 Ω/square, respectively. This difference in R_S is not due to a difference in the Boron depth distribution, as the Boron profiles are comparable (Fig. 4.8), hence the level of dopant activation is indeed higher with Sn co-implantation after post-LA RTP.

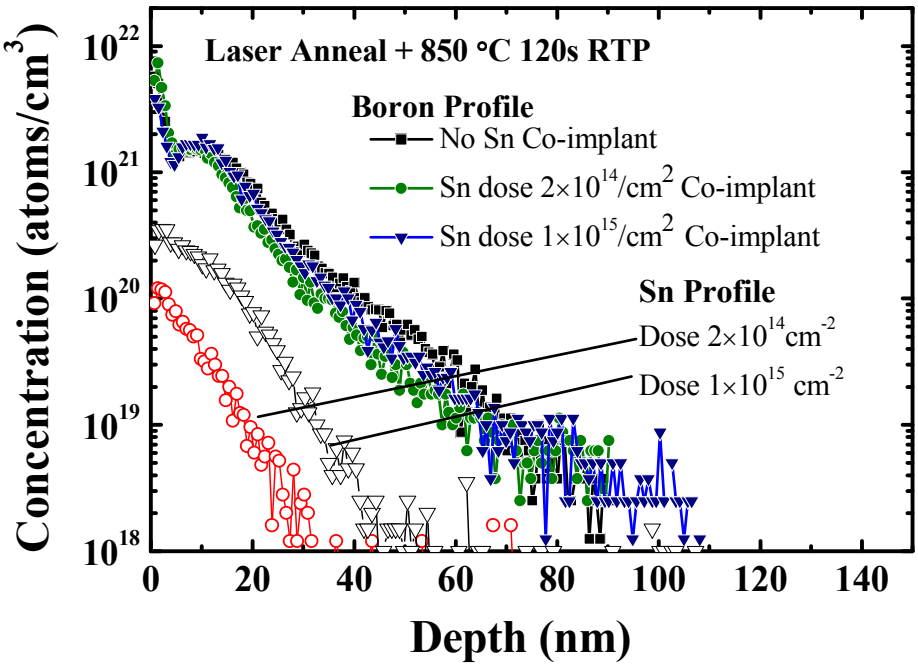


Fig. 4.8. SIMS profiles of B and Sn after post laser RTP. The filled symbols indicate the boron depth profile, while the open symbols indicate the tin depth profile. Comparable Boron profile observed regardless of Sn co-implantation does. The co-implants did not cause an increased diffusion or deeper of junction depth.

4.4.3 Physics of Enhanced Thermal Stabilty

To further confirm and understand the relation between enhanced boron's thermal stability with Sn strain compensation implant, we correlate the lattice strain calculated after laser annealing (obtained in section 4.3) with the change in sheet resistance $(R_f - R_0)/R_0$ after post LA RTP of 800 ºC, 120s, as shown in Figure 4.9.

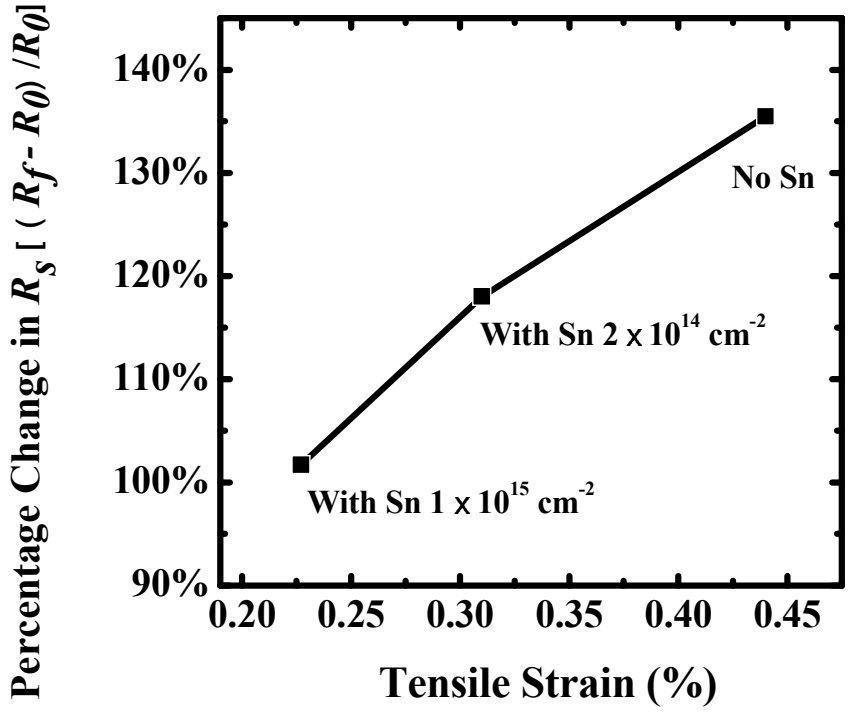


Fig. 4.9. Percentage change in R_s decreases with reduced tensile strain. R_f is the final sheet resistance measured after post laser annealing at 850ºC for 120s, while R_0 is the initial sheet resistance after laser annealing.

This relation could be understood by considering the strain energy w of lattice mismatched epitaxial layer on Si <100> substrate. The strain energy stored in this system can be obtained by the elastic energy expression for semiconductor materials. $w = (\Delta a/a)^2(C_{11} + C_{12} - 2C_{12}^2/C_{11})$.[4.10, 4.11] With the larger lattice deformation or $\Delta a/a$ in the control sample with BF_2 implant only, the elastic energy stored is higher. With the introduction of an increasing dose of Sn, the strain energy is reduced. So the lower tensile strain energy in the whole system with the Sn co-implantation leads to reduced boron deactivation and less change in sheet resistance.

4.5 Summary

Incorporation of Sn was investigated as a means to reduce undesirable lattice strain caused by boron doping.

High resolution XRD measurement after laser annealing at a laser fluence of 740 mJ/cm^2 confirms that the tensile strain caused by supersaturated boron was indeed relieved by tin co-implantation. This strain compensation by Sn implantation also suppresses Boron deactivation during post laser annealing thermal processing. Therefore, Sn co-implantation with Boron in S/D or S/D extension could be an effective way to reduce the potential p-FET performance degradation due to tensile strain caused by Boron doping.

4.6 Future Work

There may be concerns about the implantation of heavy atoms such as Sn causing an increase in crystal damage in the substrate, leading to increase in junction leakage. However, electrical characterization shows that this is not the case with Sn dose up to 1×10^{15} cm^{-2}. Comparable diode leakage current was observed independent of Sn implantation dose (Fig. 4.10).

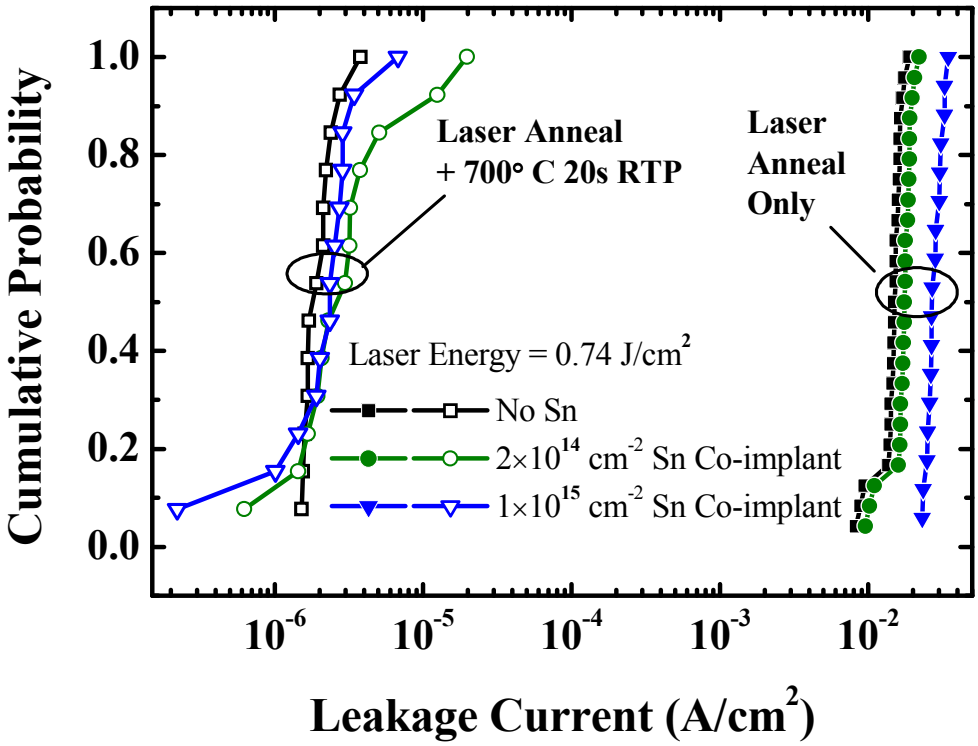


Fig. 4.10. Diode leakage current measured before and after post laser annealing at 700 ºC for 20 s with different Sn dose. The co-implants did not increase the leakage current.

To further improve the performance of a p-FET, high compressive strain levels in the channel can also be achieved by $Si_{1-z}Sn_z$ S/D stressors with high subsitutial Sn content formed using Sn implantation and anneal. However, due to the low solid solubility of Sn in Si (the solubility of Sn in silicon is limited to ≈0.01%), it is very challenging to produce $Si_{1-z}Sn_z$ S/D with large Sn content. Up to now, molecular beam epitaxial (MBE) growth at relatively low temperature for $Si_{1-z}Sn_z$ growth can achieve metastable, pseudomorphic $Si_{1-z}Sn_z$ films with Sn content up to 5% [4.12],. However, Sn metallic precipitates would occur with subsequent thermal process[4.13, 4.14],. How to produce SiSn S/D with high Sn content is still challenging and an interesting direction for further research.

4.7 References

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CHAPTER 5

Conclusions and Future Work

In conclusion, novel process, structures, or concept related to strain engineering techniques have been proposed and experimentally explored for nanoscale p-channel transistors. The major conclusions and contributions of this work are summarized as following:

5.1 Ge Enrichment in $Si_{1-x}Ge_x$ S/D Stressor for P-FET Performance Enhancement

Increasing the Ge content in the embedded SiGe (eSiGe) Source/Drain (S/D) stressors improves p-FET performance. However, challenges are faced in managing strain relaxation and defect formation in an epi-SiGe S/D formed using a conventional process. A new process technology for boosting the Ge content in SiGe source/drain (S/D) stressors was demonstrated to increase strain and performance levels in p-FETs. By laser-induced local melting and inter-mixing of an amorphous Ge layer with an underlying $Si_{0.8}Ge_{0.2}$ S/D region, a graded SiGe S/D stressor is formed upon recrystallization. Raman analysis confirmed the retention of high S/D strain levels due to the rapid non-equilibrium recrystallization process. For a p-FET with Ge enriched S/D, an I_{Dsat} enhancement of about ~14% over control strained p-FETs with $Si_{0.8}Ge_{0.2}$ S/D at similar short-channel effects and S/D sheet resistance was observed.

5.2 Reverse Embedded Si:C stressor for P-FET Performance Enhancement

A new structure with reverse embedded Si:C stressor was fabricated. Unlike the conventional stress from the S/D region, this stress comes from beneath the channel. The challenges and issues of the fabrication process were discussed. Issues like carbon precipitation and strain relaxation expose a limitation for high temperature process in the later stage of device fabrication. The channel epitaxial process is extremely challenging, excellent epitaxy quality is required for good transistor performance and drive current enhancement. Our current results showed poor device performance with high leakage current from source to drain due to defects from the low epitaxy quality or defects generated during subsequent implantation and annealing. To further improve the transistor performance with this reverse embedded Si:C stressors, the epitaxial quality need to be improved, and the process of implantation and activation for V_T adjustment and punch through suppression implants need to be optimized. This implantation and annealing could be even omitted by growing in-situ doped Si/ Si:C layer.

5.3 Tin Strain Compensation Implant for Reduction of Tensile Strain Caused by Boron Doping

Nanoscale p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) require heavily doped and highly activated boron in the source/drain or source/drain extensions for good control of short-channel effects and low series resistance. However, due to the smaller covalent bond radius of boron than silicon, a layer of Si supersaturated with boron will have a smaller lattice constant and

experience a local lattice contraction. When highly activated boron formed in S/D or S/D extension regions in a p-channel transistor, it can cause undesirable tensile channel strain that leads to p-FET performance degradation due to the smaller lattice constant of the S/D region. The supersaturated and metastable boron that produced by laser annealing could also deactivate during post laser thermal cycles, and lead to undesirable performance degradation. Effect of tin incorporation on the strain compensation and thermal stability of boron was studied for the first time. High resolution XRD measurement indicates that the tensile strain caused by a high boron concentration was reduced by the introduction of tin. Sn co-implantation also effectively reduces the strain energy and therefore enhances the thermal stability of boron in post-laser-anneal rapid thermal processing. Therefore, Sn co-implantation with Boron in S/D or S/D extension could be an effective way to reduce the possible p-FET performance degradation due to tensile strain caused by Boron doping.

5.4 Future Work

This thesis explored several technology options for the enhancement of p-channel transistor performance. Some further work in this area is open for investigation.

Laser annealing, being a non equilibrium process, could be useful for prevention of strain relaxation, and to activate dopants such as carbon or Sn to concentrations far excess of their solid solubility for S/D stressor application. A high laser fluence is usually required to achieve better activation of dopants, however, the excess heat absorbed by the gate can cause dopants penetration, high gate leakage current, or even gate deformation. Therefore, how to effectively protect the gate, and

reduce the laser absorption by gate line is an important issue, and can be of interest of future research.

In addition, reverse embedded Si:C strain transfer structure could be used to impart strain from beneath the channel for transistor performance enhancement. Further performance optimization work could be done. These include increasing the thickness of embedded Si:C layer for higher strain, or/and adopting in-situ doped Si:C strain transfer regions with high [C] content, for minimizing strain relaxation. An integration of high stress diamond like carbon (DLC) etch stop layer with this novel device structure could also be exploited for further strain and performance enhancement. This structure could also be integrated with the metalized S/D for high channel mobility and low S/D resistance. Other characterization work, such as direct measurement of strain using a nano Raman with a dummy/ disposable gate, could provide insights to the actual strain distribution under the gate, and is an interesting direction of future work.

In the case of Sn incorporating for strain compensation of boron, we show that the lattice constant has been enlarged by Sn co-implantation and anneal. Other p-type dopants such as Ga or In, with the larger atomic radius than Si can also been explored as alternative dopant or co-implant with boron in Si for p-MOS S/D application.

Areas that are not discussed in this thesis work, such as the silicide induced stress could also be interesting direction of future research.

Appendix A

Selected List of Publications:

1. F. Liu, K.-M. Tan, X. Wang, D. K. Y. Low, D. M. Y. Lai, P. C. Lim, G. Samudra, and Y.-C. Yeo, "Incorporation of tin in boron-doped silicon for reduced deactivation of boron during post-laser-anneal rapid thermal processing," J. Applied Physics, vol. 102, 093717, Nov. 2007.

2. F. Liu, H.-S. Wong, K.-W. Ang, M. Zhu, X. Wang, D. M.-Y. Lai, P.-C. Lim, B. L. H. Tan, S. Tripathy, S.-A. Oh, G. S. Samudra, N. Balasubramanian, and Y.-C. Yeo, "A new source/drain Germanium-enrichment process comprising Ge deposition and laser-induced local melting and recrystallization for P-FET performance enhancement," Symp. on VLSI Tech. 2007, Honolulu HI, USA, Jun. 17-19, 2008.

3. F. Liu, H.-S. Wong, K.-W. Ang, M. Zhu, X. Wang, D. M.-Y. Lai, P.-C. Lim, and Y.-C. Yeo, "Laser annealing of amorphous Germanium on Silicon-Germanium source/drain for strain and performance enhancement in P-MOSFETs," IEEE Electron Device Letters, vol. 29, 2008.