STRAIN ENGINEERING FOR ADVANCED TRANSISTOR STRUCTURE

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NATIONAL UNIVERSITY OF SINGAPORE

2008

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A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTING ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2008

Acknowledgements

First and foremost, I would like to thank my supervisor, Dr. Yeo Yee-Chia who has provided much support and encouragement throughout the course of my Ph.D candidature. I have benefited a lot from the numerous discussions that we have. I would also like to thank all my co-supervisors, A/P Yoo Won Jong, Dr Lap Chan, Dr Narayanan Balasubramanian and Dr Patrick Lo who have always been generous in helping me in whatever ways they can. In addition, I will also like to thank A/P Ganesh S. Samudra for giving his advice and suggestions during our research group meetings. Special thanks to Dr Yang Mingchu for constantly provide the support and help, which we need in using the FCVA system.

My work is mainly done in 2 laboratories in this period of time, Semiconductor Processing Technology (SPT) Lab at the Institute of Microelectronics (IME), and the Silicon Nano Device Lab (SNDL) at the National University of Singapore (NUS). I am very grateful to all the staffs in both laboratories as they have provided assistance in one way or another which made my work possible.

I have also learnt a lot from the friends that I have made from Chartered, SNDL and IME. In particularly, I am extremely thankful that the development of FinFET process flow is done together with Tsung-Yang (Jason). We practically started the FinFET process from scratch and spend countless night in the cleanroom developing all the necessary process steps.

I will also like to express my deepest gratitude to my family, especially my parents who have been very supportive ever since I started my graduate studies

from MASTER to Ph.D. It has been a very long journey, and I truly hope I can spend more time with them in the future.

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Abstract

With the aggressive scaling of device dimensions to meet performance requirements, various techniques have been proposed to improve device performance and among them, strained silicon technology has been very successful and is currently implemented and used in manufacturing. However, the scaling of technologies node is still on-going and researchers from all over the world are still trying to push silicon to its limit. Advanced transistors structure like FinFET or multiple-gate devices are also introduced to control the short channel effects which increase significantly as the physical gate length approach sub-50 nm. In this thesis, various approaches are also explored to enhance the device performance for sub-32 nm technology node. The effect of having a SiN capping layer on a tantalum nitride (TaN) metal gate FinFET during source/drain anneal was studied. Enhancement in drive current is observed when compared to a similar but un-capped FinFET device. The increased in drive current is attributed to the constraint in the expansion of TaN which result in a residual stress being induced in the channel that improve electron mobility. Therefore, strain effect due to the introduction of new materials for metal gate and high-k gate dielectric should be taken into considerations

SiGe source/drain (S/D) which is lattice mismatched to Si has been used to induce compressive stress in the channel to enhance the performance of p-channel transistors. Recently, this has also been applied on FinFET device demonstrating larger drive current performance. Improving the performance of FinFET device with SiGe S/D is also investigated in thesis. Ge condensation is adopted to form a FinFET device with an embedded SiGe S/D showing better performance than the

control device. In addition, a novel extended-pi (Π) shaped SiGe S/D stressor is also formed for the first time on FinFET device which shows an increase in drive current over FinFET with pi-shaped SiGe S/D stressor, attributed to the enhancement of strain effect and lower series resistance.

With the decrease in gate pitch, strain induced in the channel by highly stressed contact etch stop liner (CESL) also decreases. Therefore, it will be advantageous that the intrinsic stress of CESL can be tuned to a much higher level. In this thesis, a new CESL liner material, diamond-like carbon (DLC) is introduced which has a much greater intrinsic compressive stress than SiN ever reported. The properties of DLC are characterized and enhancement in drive current on both p-channel SOI and FinFET devices are demonstrated experimentally. In addition, studies of DLC on bulk planar device having an embedded SiGe were also made and it is observed that the strain effect couple to the channel can be larger when the DLC stressed liner is integrated on to a device with an intentionally recessed S/D profile. The efficiency of the transfer stress is higher with the closer proximity of the DLC stress liner to the channel.

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G_m	Transconductance	S
H_{fin}	Fin height	nm
κ	Permittivity dielectric	
$I_{D,sat}$	Saturation drain current	μA/μm
$I_{D,Lin}$	Linear drain current	μA/μm
I_D	Drain Current	μA/μm
I_S	Source Current	μA/μm
I_{off}	Off-state leakage current	A/μm
I_{on}	On-state leakage current	μA/μm
m	body-effect factor	
p_{fin}	Fin pitch	nm
ρ	Resistivity	Ωcm
r_c	back scattering coefficient	
S_{xx}	Stress Component in x-direction	MPa
S_{yy}	Stress Component in y-direction	MPa
u_{eff}	Effective mobility	cm^2/Vs
V_G	Gate Voltage	V
V_D	Drain Voltage	V
V_{th}	Threshold voltage	V
v_T	Thermal velocity	cm/s
ν_{sat}	Saturation velocity	cm/s
W_{fin}	Fin width	nm
X_λ	Component of the stress in six-component vector notation	MPa
Φ_m	Gate work function	eV
Π_l	Longitudinal piezoresistance coefficient	
Π_t	Transverse piezoresistance coefficient	
$\Pi_{\omega\lambda}$	Component of the piezoresisance tensor.	

Chapter 1

Introduction

1.1 Background

The scaling of CMOS technology which allows higher packing density and better device performance has become more challenging as we approach sub-100 nm node. While the transistor dimension has become smaller, more of them can be packed per unit area (Moore's law: double of chip components for every 24 months), the electrical performance will have to be improved at the same time. For high performance device, there are several requirements to meet and among them are the control of short channel effects (SCEs) to give a low off-state leakage current (I_{off}) and also high drive current (I_{on}) to booast the speed of the circuit.

Very often, a plot of I_{on} in linear scale on the x-axis and I_{off} in log scale on the y-axis is used to describe and compare the performance of different devices. A typical plot of this is shown in Fig 1.1 where the data points are taken from transistors having different L_G characterized by each I_{on} and I_{off}. The data points formed a straight line as seen in Fig. 1.1. Transistor with smaller L_G demonstrates higher I_{on} and I_{off}. For each technology node, the objective is to push the "line" further to right. This means that either at the same I_{off}, the device will demonstrate higher drive current (line A) or alternatively, at the same I_{on}, the device will give a smaller I_{off} (line B).

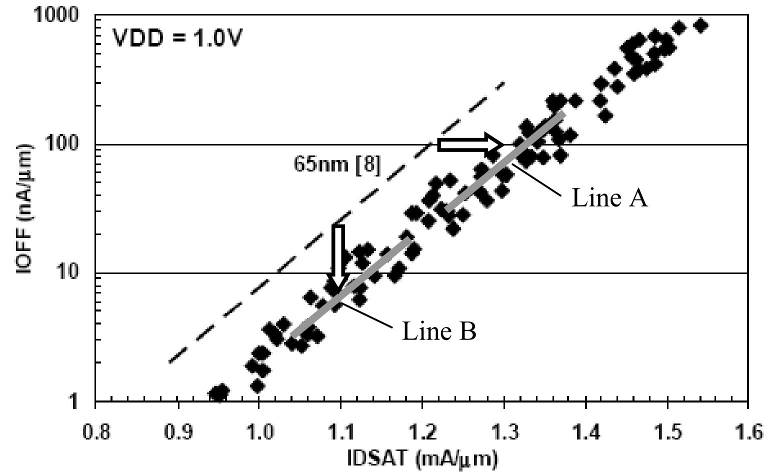

Fig. 1.1 A typical plot of I_{off}-I_{on} for 65 nm technology node taken from Ref. [1.1]. Additional arrows and lines are added for illustration purpose.

For a MOSFET, the drive current can be simply increased by decreasing L_G as suggested by the following equation

$$I_{D,Sat} = \mu_{eff} C_{ox} \frac{W}{L_G} \frac{(V_{GS} - V_{th})^2}{2m}, \qquad \text{--- eq. (1.1)}$$

where m: body-effect factor, typically lies between 1.1 and 1.4.

However, with the scaling down of the supplied voltage at the same time to maintain an appropriate electric field in the transistor, the increase of drive current is reduced. Increasing the gate oxide capacitance (C_{ox}) by scaling down the thickness of the conventionally used SiO_2 gate dielectric has also become more challenging. As the thickness of SiO_2 gate dielectric approaches 1 nm, the gate leakage current increases mainly due to direct tunneling. This render the used of high-κ gate dielectric materials to give a thicker physical thickness for the control of gate leakage issues. Therefore, to increase drive current, enhancing the mobility (u_{eff}) of the carrier has been proposed.

Replacing Si with other materials having a much higher intrinsic mobility has been suggested. Candidates like Ge [1.2]-[1.3] and III-V compounds eg. GaAs [1.4]-[1.5] are currently being investigated. However, adopting these materials for device fabrication has problems of their own. Finding a compatible gate dielectric, source/drain contact and several other issues will have to be overcome before it can be used in manufacturing. A more near-term solution is to boost the electron and hole mobility of Si, which can be achieved by straining the Si channel [1.6]-[1.7]. When Si is under strain, the Si lattice crystal gets distorted and this changes the electronic band structure. Splitting of the bands can occur and the effective mass can also be modified. A review paper on this phenomenon and application was reported by *Lee et al.* [1.8]. Different strain techniques have been explored to induce strain in the device channel, some of them are listed as followed,

1) making use of the lattice mismatch between Si and $Si_{1-x}Ge_x$ [1.9], Si and $Si_{1-y}C_y$ [1.10]-[1.11] for PMOS and NMOS devices, respectively,
2) making used of a highly tensile or compressive stress contact etch stop liner (CESL), typically SiN [1.12],[1.13],
3) stress induced by a fully silicided (FUSI) gate [1.14],
4) stress memorization techniques which until now is only reported for NMOS device [1.15],
5) reverse embedded SiGe structure [1.16],
6) and also instinctively, a combination of the above stressors (multiple stressors) [1.17].

With the scaling down of device dimension below sub-micron regime (eg. L_G at 100 nm for a V_D of 1.2 V), the lateral electric field now (1.2×10^5 V/cm) becomes larger than the critical field of velocity saturation and eq. 1.1 becomes

$$I_{D,Sat} = \nu_{sat} C_{ox} W (V_{GS} - V_{th}) \frac{\sqrt{1 + 2\mu_{eff}(V_{GS} - V_{th})/(m\nu_{sat}L_G)} - 1}{\sqrt{1 + 2\mu_{eff}(V_{GS} - V_{th})/(m\nu_{sat}L_G)} + 1}, \quad \text{--- eq. (1.2)}$$

where ν_{sat} is around 7-8$\times10^6$ cm/s for electrons.

In Equation 1.2, the carriers are treated to be in thermal equilibrium with the Si lattice. When L_G is scaled down further to sub 100 nm, it has been reported that velocity overshoot can occurred [1.18] where the velocity of the carrier can exceed that that of ν_{sat}. For 90 nm technology node and beyond, the physical L_G of the tranisisor is in fact smaller than 50 nm and thus the carrier should no longer be treated to be in thermal equilibrium with the Si lattices. For MOSFET, the current is mainly dependent on the average carrier velocity at the source end of the channel and a simple one-flux scattering is introduced [1.19] as follows

$$I_{D,Sat} = \nu_T C_{ox} W \left(\frac{1 - r_c}{1 + r_c} \right) (V_{GS} - V_{th}) , \quad \text{--- eq. (1.3)}$$

where v_T is the thermal velocity and r_c is the back scattering coefficient. Treatment of eq. 1.3 for the case of degenerate condition is described in [1.20]. It has been reported that the effect of strain can change both v_T and r_c [1.21]. Therefore, with careful optimization of the process, even for extremely small L_G the technique of strain will still be useful in improving the I_{on}.

A major issue accompaning L_G scaling is the increase in off-state leakage current. This is usually due to an increase in subthreshold swing (SS) and larger drain induced barrier lowering (DIBL) effect as illustrated in Fig 1.2. To control

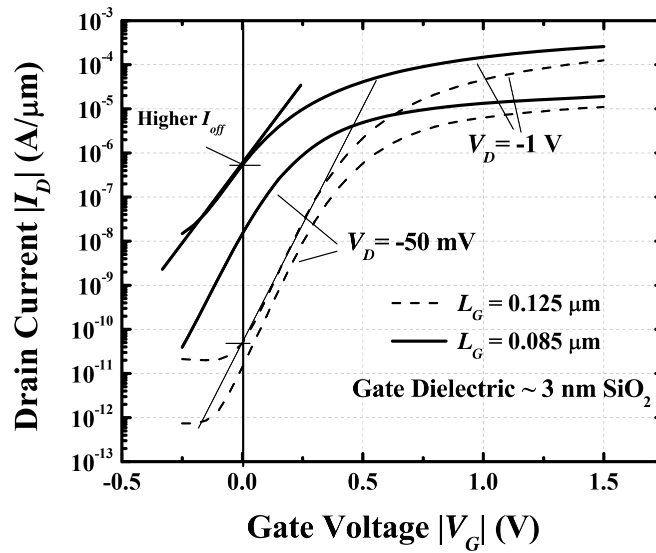

Fig. 1.2 A typical plot of I_D-V_G comparing short and long L_G devices. Device with small L_G shows smaller V_{th}, and larger SS, DIBL and I_{off}.

the short channel effect (SCEs) at small L_G, higher channel doping, and halo implants are used. However, incorporating more dopants in the channel degrades mobility. Efforts have been put in to push the device L_G to sub-10 nm, however the DIBL and SS observed are still very large [1.22]. Devices fabricated on ultra-thin silicon-on insulator (SOI) wafer (Fig. 1.3(a)) is able to achieve a smaller I_{off} by eliminating the leakage path which is far away from the gate control. When L_G is scaled down to less than 15 nm, according to the International Technology Roadmap for Semiconductors (ITRS) 2008 Update PIDS, FinFET or multi-gate device structure as shown in Fig. 1.3(b) will be required to control the I_{off} more effectively.

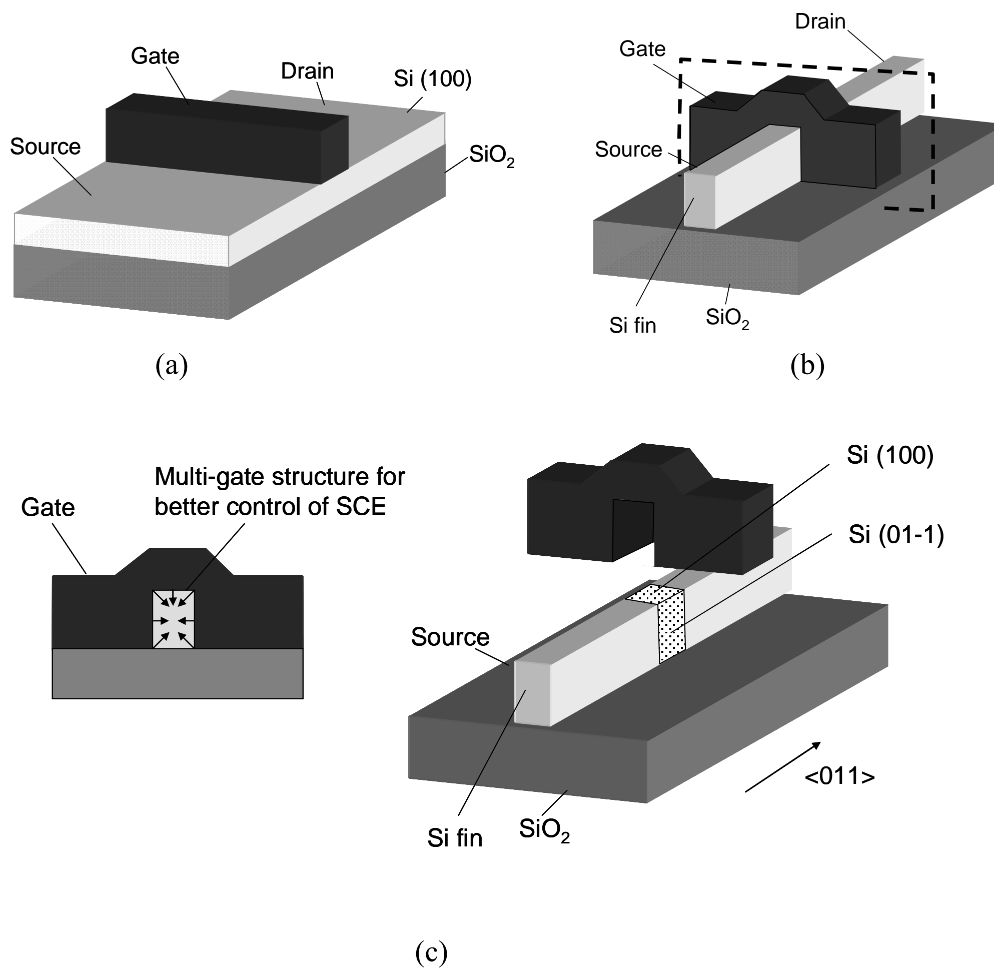

Fig. 1.3 Schematics of a (a) planar device fabricated on SOI wafer, (b) a FinFET or multiple-gate device, and (c) cross-section showing the control by multi-gate structure and the different planes of conduction.

As shown in Fig. 1.3(c), the drain current can flow from the source to the drain on the top surface and on both sidewall surfaces of the fin. The surface orientations are different with the top surface being (100) and the sidewall surfaces being (110). The mobility of the carriers travelling in the different surfaces will be also different. For example, it is well-known that the hole mobility is higher on a (110) plane when compared to the (100) [1.23]. The performance of the multi-gate device will depend a lot on the dimension of the fin

width (W_{fin}). Devices with smaller L_G will usually require smaller W_{fin} for better SCEs control. However, the decrease in W_{fin} is accompanied by an increase in series resistance and this degrades the drive current. Therefore, performing selective epitaxy raised source/drain (S/D) on the multiple-gate device has been proposed for the reduction of series resistance [1.24]. To give even better device performance, SiGe [1.25] or Si:C which is lattice mismatched to Si can be grown instead to induce strain in the channel for mobility improvement. In addition, SiGe can also be exploited to lower the contact resistance due to the smaller bandgap of SiGe as Ge concentration increases [1.26].

1.2 Objective of Research

The objection of this thesis work is to investigate and demonstrate novel device structure and idea that can improve the device performance for sub-32 nm node and beyond. Study of strain engineering on bulk, planar SOI and multiple-gate or FinFET device is being made based on each device structure.

1.3 Organization of Thesis

Chapter 2 of this thesis investigates the effect of having a silicon nitride (SiN) capping layer on a TaN metal gate FinFET device during the high temperature S/D anneal. Comparison of performance is made to a similar device but without the capping SiN. In this thesis work, the I_D-V_D is plotted with different gate overdrive (V_G-V_{th}) biasing. Saturation V_{th} is used here, where V_{th} is taken at high V_D. The V_{th} is taken based on a constant I_D value chosen from the plot of Log I_D against V_G curve below the turning point where the subthreshold slope start to

flatten which is an indication that the transistor is about to “turn on”. In chapter 3, poly-Si gate etching issues on FinFET device are discussed. Due to the 3D topography which results in the formation of gate stringer, conventionally gate etch recipe used for the planar device is not suitable and thus a new gate etch recipe specifically for the FinFET structure is developed.

In chapter 4, strained FinFET with SiGe S/D was studied. By having a better understanding of the FinFET device structure and fabrication process, enhanced versions of FinFET with SiGe S/D was proposed which demonstrated better device performance. With the rapid shrinking of device dimension, strained techniques employing highly stress contact etch-stop liner (CESL) becomes less efficient. In chapter 5, a novel material diamond-like carbon (DLC) having an extremely high intrinsic compressive stress is introduced for high stress CESL application. Performance enhancement on p-channel planar SOI and FinFET devices are also discussed.

Further investigations of DLC are made in chapter 6. Process conditions affecting the intrinsic stress of DLC are reported and integration with planar device having an embedded SiGe S/D was also demonstrated for the first time. In addition, DLC integrated with an intentionally recessed S/D profile show better coupling of strain from the DLC stressor to the channel. Lastly, in chapter 7, a conclusion is made and future work with regards to this thesis are suggested.

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Chapter 2

Drive Current Enhancement in FinFETs Using Gate-Induced Stress

2.1 Background

As mentioned in chapter 1, the multiple-gate transistor or FinFET device structure [2.1]-[2.4] has superior scalability over conventional planar metal-oxide-semiconductor (MOS) transistor structures, and enables gate length scaling well beyond the 32 nm technology generation. In addition, the FinFET device structure allows the use of low channel dopant concentration, and avoids problems associated with random dopant fluctuation. The threshold voltage V_{th} of FinFETs can be set through gate work function Φ_m engineering using metal gates, which additionally eliminate the gate depletion effect and dopant penetration problem for improved drive current $I_{D,sat}$ performance. For n-channel FinFET devices, the optimal gate work function lies between the mid-gap and the conduction band of Si, which necessitates the use of metal gates. It has been reported that fully-silicided metal gate can induce strain in the transistor channel [2.2], and the localized strain could be exploited to enhance the performance of aggressively scaled transistors. While many approaches to strained-Si has been demonstrated, strain introduction by metal-nitride gate has not been experimentally reported.

In this chapter, we report the first demonstration of a strained n-channel FinFET with a tantalum nitride (TaN) gate stressor. We also report a novel and simple process that exploits the stress developed in the metal gate during an anneal process to introduce strain in the Si channel. The resulting drive current enhancement in FinFET devices will be discussed

2.2 Device Fabrication

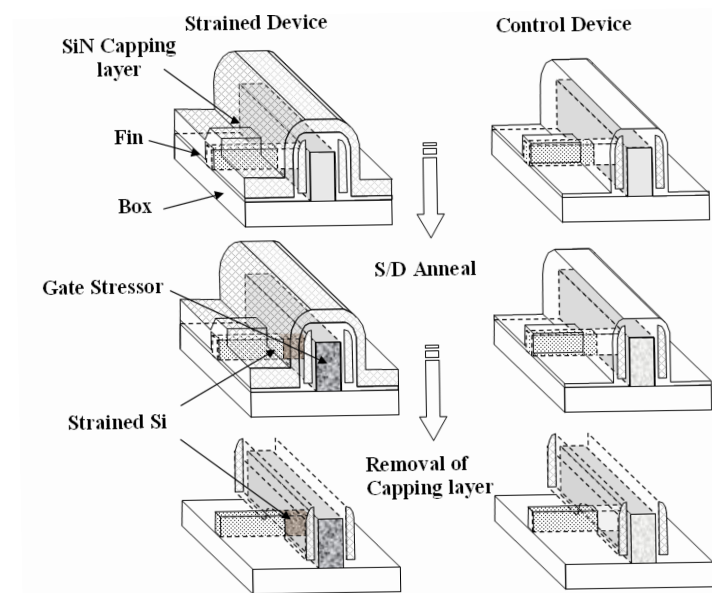
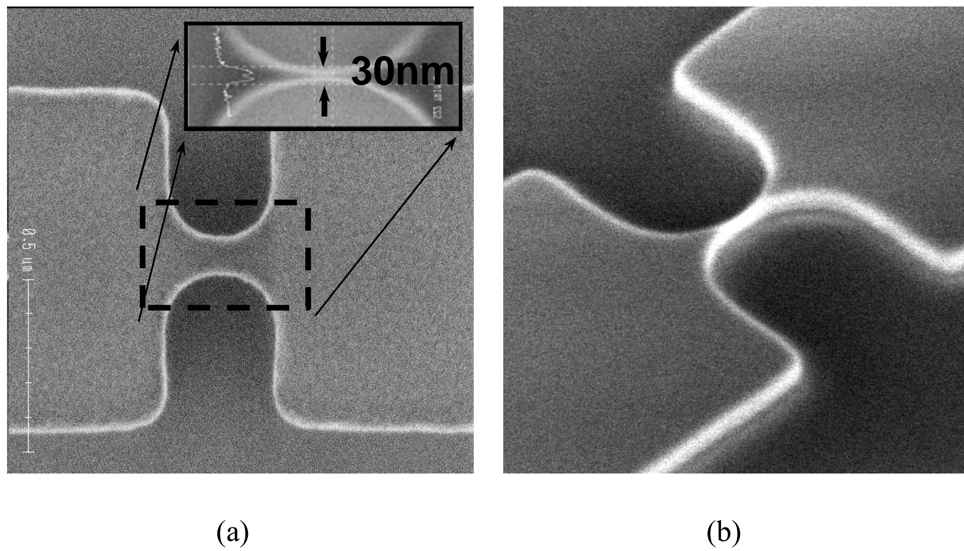


Fig. 2.1. Process flow and schematics showing the FinFET fabrication process and the incorporation of metal-gate stressor. The introduction of an additional SiN layer prior to the S/D dopant activation anneal serves to induce high stress in the channel by constraining the gate structure's volume expansion. The strain is retained even after SiN removal.

Mesa-isolated n-channel FinFETs with TaN gates were fabricated on SOI wafers. The process sequence adopted is illustrated in Fig. 2.1. Silicon on insulator (SOI) wafers with (001) surface and 45 nm thick Si were used. Gate etching development was first done to see the feasibility of etching TaN gate



(a) (b)

Fig. 2.2. (a) Top view SEM images of the fin pattern before and after resist trim as shown in the inset. Fin width as small 30 nm can be achieved using a mixture of O_2 and Ar plasma. (b) Tilted SEM images of the fin after dry etch where the fin pattern is transferred down to the Si.

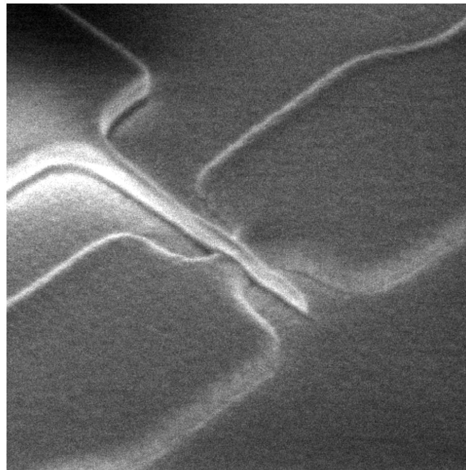


Fig. 2.3. SEM images of the pattern gate line running across the fin. Resist trimming were also used here to achieve small gate length.

electrode on FinFET. After fin patterning using 248 nm lithography, resist trimming is applied to achieve fin width of sub-30 nm as shown by the Scanning

Electron Microscopy (SEM) image in Fig. 2.2(a). This is later transferred to the Si as observed in Fig. 2.2(b). Figure 2.3 shows the gate pattern running over the fin and small gate line was achieved by adopting a similar scheme as in the fin definition.

The etching of metal gate was done using an Applied Material Centura etch system. Figure 2.4 shows the SEM images of the FinFET structure after TaN metal gate etch, using a mixture of HBr/Cl_2 and Ar. The stopping of the metal gate etch on the thin dielectric can be quite challenging and even if this can be done, there is still some metal gate stringers which remained and surround the FinFET device as seen from Fig. 2.4(a). In the attempt to remove the stringer by increasing the metal gate etched time, it results in the etching away of the fin as observed in Fig. 2.4(b). While the Si at the source/drain (S/D) pad remain, Si

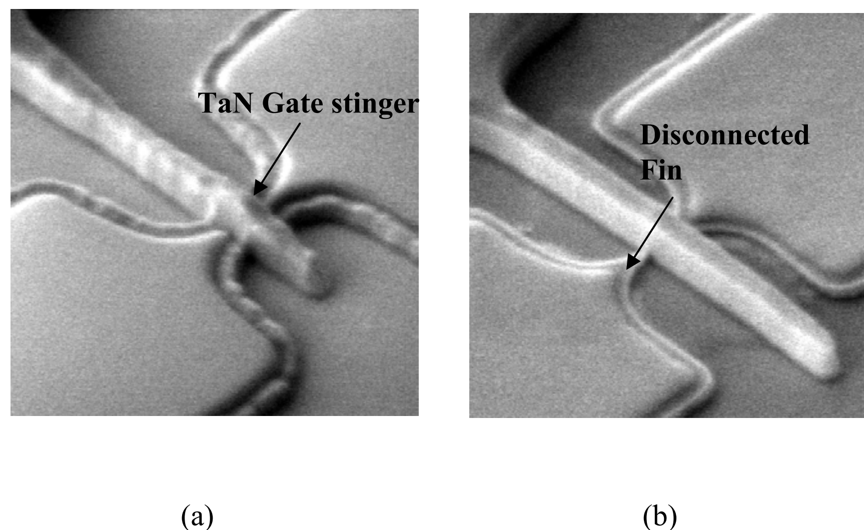
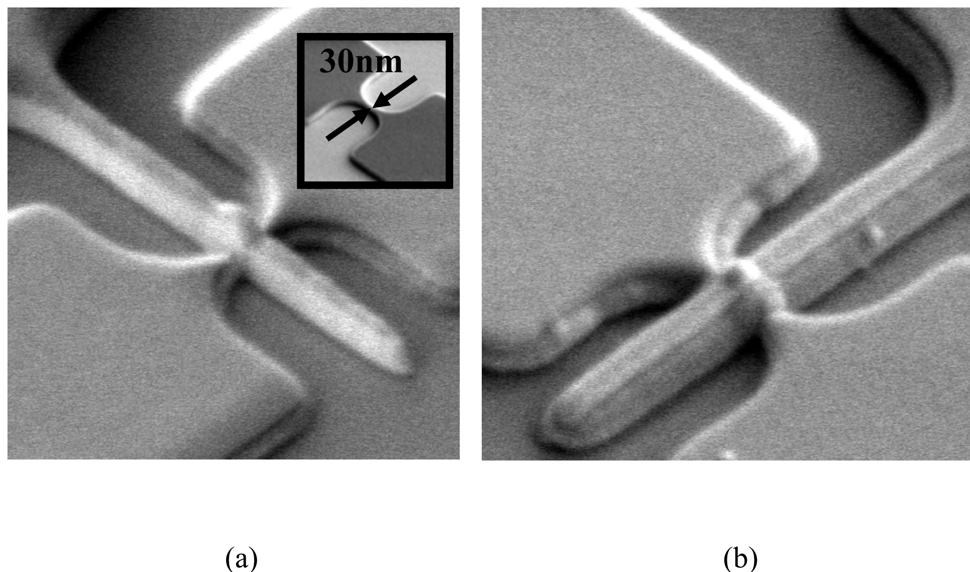


Fig. 2.4. (a) SEM image showing the FinFET structure after TaN gate etch. The fin height is 45 nm and 3 nm SiO_2 is used as the gate dielectric. TaN gate stringer can be seen surrounding the FinFET structure. (b) An extended gate etch was done to remove the stringer, but the gate etch selectivity to SiO_2 dielectric is not sufficient high too protect the fin from getting etch away.

at the edges of the S/D pads was already gone as seen in Fig. 2.4(b). The faster etch rate at the Si fin corners make the etching of TaN gate on FinFET even more challenging. A thicker SiO_2 (60 nm) was therefore deposited as a hard mask for the definition of the Si fin. The hard mask was retained for the protection of the fin in a subsequent gate etch process.

A 2 nm sacrificial oxide was then grown on the fin sidewalls to repair the damage caused by plasma etching. Following its removal, SiO_2 with a target EOT of 25 Å was used as the gate dielectric before depositing 100 nm of TaN as the gate electrode. Gate etch profile has improved after the new approach was adopted as shown Fig. 2.5(a). After S/D extension implant, spacer formation, and the deep S/D implant, the resulting structure is shown in the SEM image in Fig. 2.5(b). PECVD SiO_2 liner layer (6 nm) was then deposited on all wafers. On one wafer in which the metal gate stress is to be introduced to form the strained-



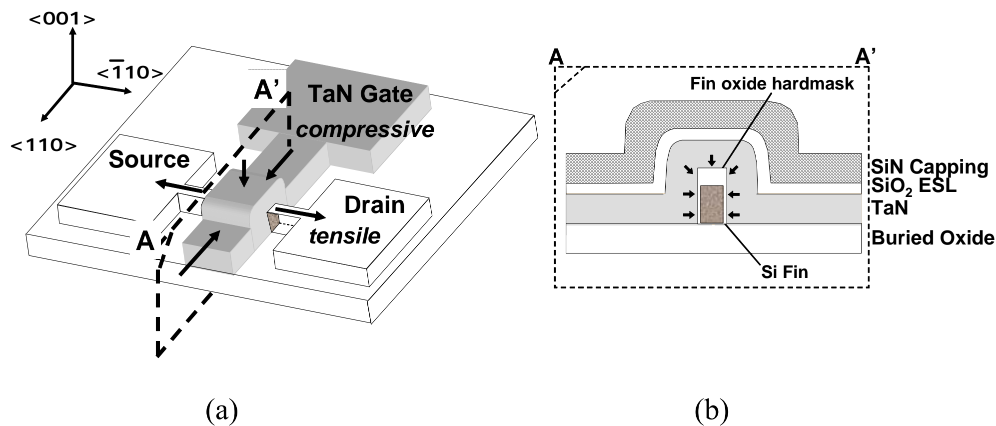
(a) (b)

Fig. 2.5. (a) SEM image showing a FinFET structure with an improved gate profile. The inset shows an image of the fin profile. (b) SEM image of the FinFET structure after spacer formation.

channel FinFET, an additional PECVD SiN capping layer with a thickness of 50 nm was deposited over the gate stack [Fig. 2.1]. The SiN capping layer has a relatively low intrinsic compressive stress of about -100 MPa. On another wafer where the control FinFETs is to be fabricated, the SiN capping layer deposition was skipped. This was followed by S/D anneal (1000°C for 5 s) on all wafers. The SiN capping layer on the strained-channel FinFET was then removed by hot phosphoric acid at 150°C. The PECVD SiO_2 liner layer was removed on both wafers. Forming gas anneal was carried out at 420°C for 30 min to complete the device fabrication.

2.3 Results and Discussion

Figure 2.6 illustrates the mechanism by which channel stress could be induced by the metal gate. This mechanism is different from the stress memorization technique reported for poly-Si gate in [2.5]. In the strained- channel FinFET



(a) (b)

Fig. 2.6. Schematic showing how the TaN gate layer can compressively stress the Si fin channel from 3 directions. The cross-section schematic illustrates the compressive stress exerted perpendicular to fin body during S/D implant activation anneal.

reported in this work, the metal gate electrode tends to expand more than the SiN capping layer or the Si fin during the S/D anneal. The thermal coefficient of expansion(TCE) is 2.44 - 2.48×10^{-6}/ºC for Si_xN_y [2.6], and 2.5×10^{-6}/ºC for Si. For the gate electrode, the TCE ranges from 3.6×10^{-6}/ºC (for TaN [2.7]) to 7×10^{-6}/ºC (for Ta [2.8]), depending on the stoichiometry.

With the presence of the SiN capping layer during the S/D anneal, limited expansion of the TaN gate in the upward direction is allowed. This results in a compressive stress being exerted onto the Si fin, as illustrated in Fig. 2.6(a). This compressive stress in the channel can be retained even after the SiN capping layer is removed. Figure 2.6(b) illustrates that due to the unique structure of the FinFET device, a constrained expansion of the metal gates on both the left and the right side of the fin effectively compresses or squeezes the fin on at least two sides. The stress is exerted perpendicularly to the fin sidewall with a (110) surface orientation, and the current conduction occurs in the $<\bar{1}10>$ direction. To study this effect, one can look at the piezoresistance coefficient [2.9] which relate the effect of resistivity and stress as shown by

$$\frac{\Delta\rho_{\omega}}{\rho}=\sum_{\lambda=1}^{6}\Pi_{\omega\lambda}X_{\lambda} \quad , \qquad \text{----------------} \quad (2.1)$$

where X_λ is the component of the stress in six-component vector notation and $\Pi_{\omega\lambda}$ is the component of the piezoresisance tensor. The tensor $\Pi_{\omega\lambda}$ is given by

$$[\Pi_{\omega\lambda}] = \begin{bmatrix} \Pi_{11} & \Pi_{12} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{11} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{12} & \Pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \Pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \Pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \Pi_{44} \end{bmatrix}.$$

In particular, we are interested in the longitudinal piezoresistance coefficient (Π_l) when the current and field are in the same direction as the applied stress and also the transverse piezoresistance coefficient (Π_t) where the current and field are perpendicular to the applied stress. We have

$$\Pi_l = \Pi_{11} - 2(\Pi_{11} - \Pi_{12} - \Pi_{44})(l_1^2 m_1^2 + m_1^2 n_1^2 + n_1^2 l_1^2),$$

$$\Pi_t = \Pi_{12} + (\Pi_{11} - \Pi_{12} - \Pi_{44})(l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2),$$

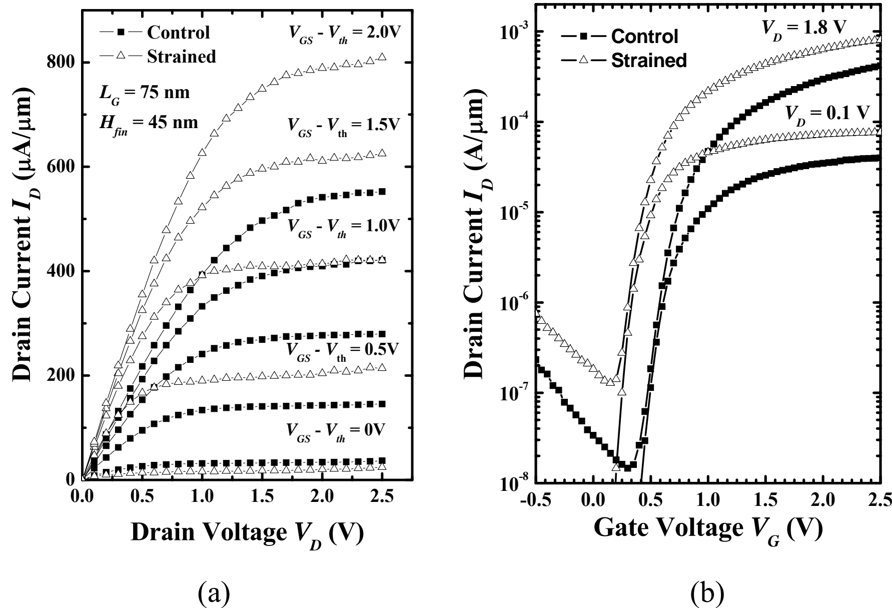
$$c\phi \equiv \cos\phi, \quad s\phi \equiv \sin\phi,$$

and $\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_{21} & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} c\phi c\theta c\varphi - s\phi s\psi & s\phi c\theta c\psi + c\phi s\psi & -s\theta c\psi \\ -c\phi c\theta s\psi - s\phi c\psi & -s\phi c\theta s\varphi + c\phi c\psi & s\theta s\psi \\ c\phi s\theta & s\phi s\theta & c\theta \end{bmatrix}$

It can thus be seen from eq. 2.1 that when the stress applied is compressive (negative), depending on the configuration (direction of applied stress with respect to the direction of current flow, surface orientation, and type of carrier), a positive value of Π_l or Π_t is desired for a reduction of resistivity and hence an increase in the mobility of carriers.

Under this configuration, the transverse piezoresistance coefficient is positive ($+52\times10^{-12}$cm^2/dyne) for electron conduction, and given that the applied stress is compressive (negative), a reduction in the channel resistance can be deduced from the above simple consideration of the piezoresistance effect. In addition, the transverse compressive strain component in the Si fin is related to the longitudinal tensile strain component by the Poisson's ratio, both of which contribute to mobility enhancement.

The I_D-V_D characteristics of a 75 nm gate length L_G FinFET is shown in Fig. 2.7(a) with the current being normalized by 2 times of the fin height H_{fin}. The strained-channel FinFET gives a significantly higher drive current compared to the control FinFET. The subthreshold swing of the devices is comparable, as shown in Fig. 2.7(b). Furthermore, they also demonstrate similar drain-induced barrier lowering (DIBL). Transconductance measurements, as plotted in Fig. 2.8



(a) (b)

Fig. 2.7. (a) I_D-V_D characteristics of control and strained FinFET devices at various gate over-drives. The strained FinFET has significantly higher drive current. (b) Subthreshold characteristics of the control and strained FinFET devices at V_D = 0.1 V and V_D = 1.8 V.

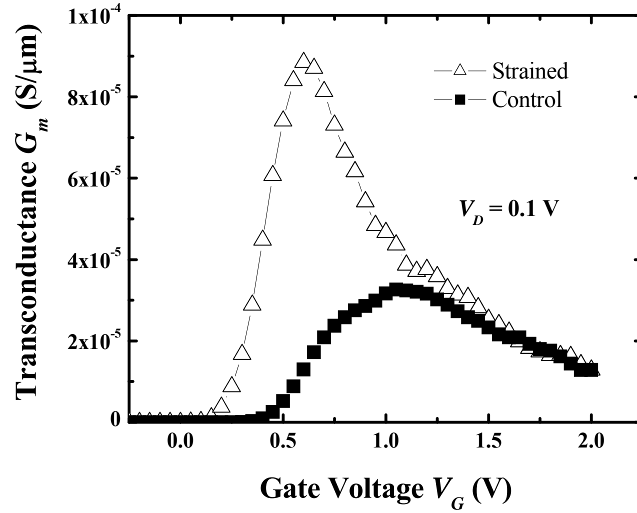


Fig. 2.8. Comparison of transconductance of the strained and control devices. The higher peak transconductance seen for the strained device, indicate a higher mobility.

shows a higher peak linear transconductance for the strained-channel FinFET compared to the control FinFET, indicating electron mobility enhancement as a result of the strain. It can also be observed that the strained FinFET exhibits a lower threshold voltage compared to the control FinFET. This could be contributed by the lowering of the conduction band energy due to the strain effect.

In this work, it is shown that the metal gate can affect the transistor performance through the stress developed during the fabrication process. While gate work function tuning, process integration, and compatibility with gate dielectric continue to be major challenges in metal gate technology development, stress contribution from the metal gate should not be disregarded, particularly since stress-induced mobility variation could result in degradation in device performance. Although the drive current of n-channel FinFETs can be enhanced by this process, the performance of p-channel devices would be degraded. For CMOS fabrication, a selective removal of the SiN capping layer over the p-channel devices should be performed prior to the S/D anneal to achieve overall

performance enhancement.

2.4 Summary

A simple and cost-effective technique was used to incorporate strain in the channel region of FinFET devices. Annealing of a TaN gate electrode capped with a SiN layer leads to the exertion of a compressive stress on the Si fin. This results in a significant enhancement of the drive current in n-channel FinFETs. This approach may be applicable to other metal gate materials having a mismatch in thermal expansion coefficient with surrounding materials like silicon oxide and silicon nitride.

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Chapter 3

Plasma Etching of Gate Electrode and Gate-Stringer for the Fabrication of Nanoscale Multiple-Gate

3.1 Background

Advanced transistor structures such as multiple-gate transistors or FinFETs enable scalability to sub-10 nm gate lengths due to improved control of short-channel effects. Major gate-etch issues in fabricating planar transistors relate to the achievement of a vertical gate sidewall profile, high etch selectivity between gate electrode and gate dielectric materials, and the control of critical dimension (CD) or gate length variability. In the fabrication of FinFETs, the fin topology over which the gate material straddles introduces additional gate etch challenges. While the gate etch process for FinFET fabrication was recently modeled [3.1], there are few reports discussing the gate etch challenges [3.2]-[3.3]. Except in one report where the removal of gate hardmask stringers [3.4] is discussed, most reports focus on the electrical characteristics of FinFETs [3.5]-[3.9]. There is also little discussion on the enabling etching technology that allows gate formation over fin structures. Issues related to the increased topography need to be considered. In particular, the gate electrode material is deposited over a step introduced by the fin, and a gate stringer is typically formed by the sidewalls of

the fins or active regions as seen earlier in chapter 2. Removal of the gate stringer can be performed in a gate over-etch step, but this could lead to either etching away of the fin or gate-line breakage, especially for aggressive gate dimensions when the etch process is not optimized.

In this chapter, we report an improved gate etch process technology for FinFET fabrication that enables a prolonged gate over-etch for gate stringer removal. The gate etch process was experimentally verified using FinFETs with sub-50 nm gate lengths.

3.2 Experiment

Experiments were performed using 8-inch silicon-on-insulator (SOI) wafers with 140 nm of buried silicon oxide and 50 nm of Si. A reactive ion etching (RIE) system (Applied Material P5000 Etcher) was employed for patterning the mesa-isolated active regions. The active regions comprise silicon fins with a fin width W_{Fin} of about 30 nm. SiO_2 with a thickness of 6 nm was then deposited using PECVD to act as a dummy gate dielectric. Silicon with a thickness of 100 nm was then deposited using LPCVD as the gate electrode material. A 50 nm SiO_2 hardmask covered the gate electrode material prior to the optical lithography step. Sub-50 nm linewidths were patterned using 248 nm lithography and resist trimming. The pattern was transferred to the hardmask and the photoresist was removed before the etching of the gate electrode using a RIE system. Tilted- SEM and CD-SEM measurements were used to characterize the transistor structure and the etching rate. In this study, HBr, Cl_2, and He/O_2 gas chemistries were used for the gate etch process.

3.3 Results and Discussion

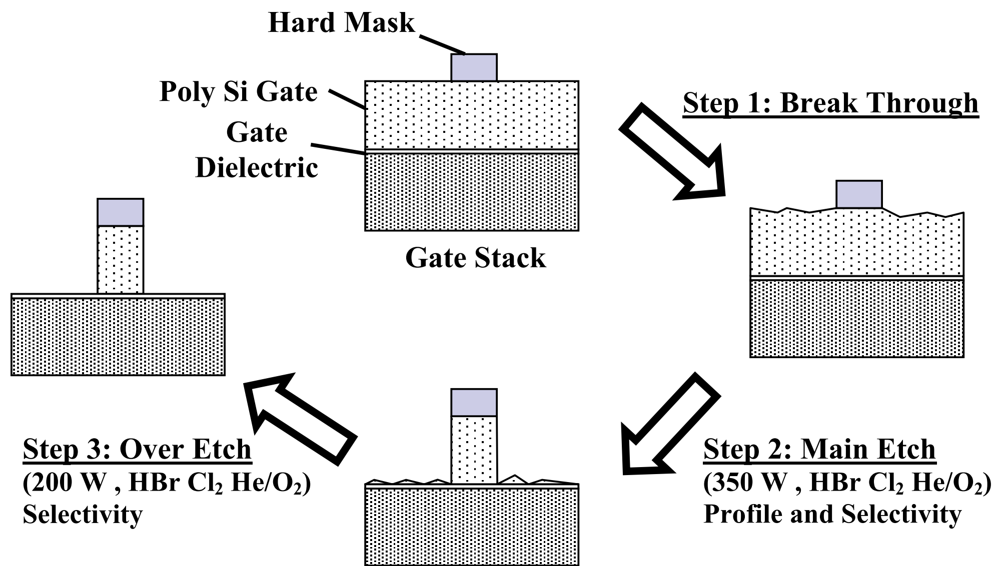


Fig. 3.1. Illustration of the various steps and the requirement in a typical gate etch process.

The gate-etch process typically comprises several steps, including the breakthrough step, the main etch, and the over-etch step. A simply illustration of these steps are seen in Fig 3.1. High anisotropy in the main etch ensures a good gate electrode profile, while high selectivity in the over-etch step maintains minimum loss of the gate dielectric. During the fabrication of the FinFET structure, however, a gate stringer can be formed adjacent to the fin structure due to the topography created by the fin step height, as shown in the SEM image in Fig. 3.2.

The gate stringer is formed in the same way as the formation of the silicon nitride spacer adjacent to the gate. If un-removed, the gate stringer would result in a large overlap capacitance between the gate and the source/drain regions, and is therefore detrimental for circuit applications. The amount of over-etching to be

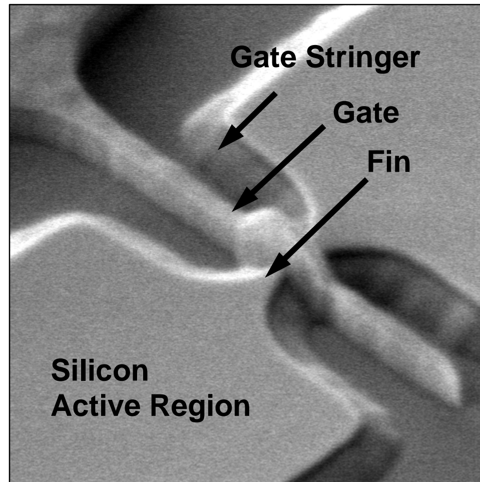


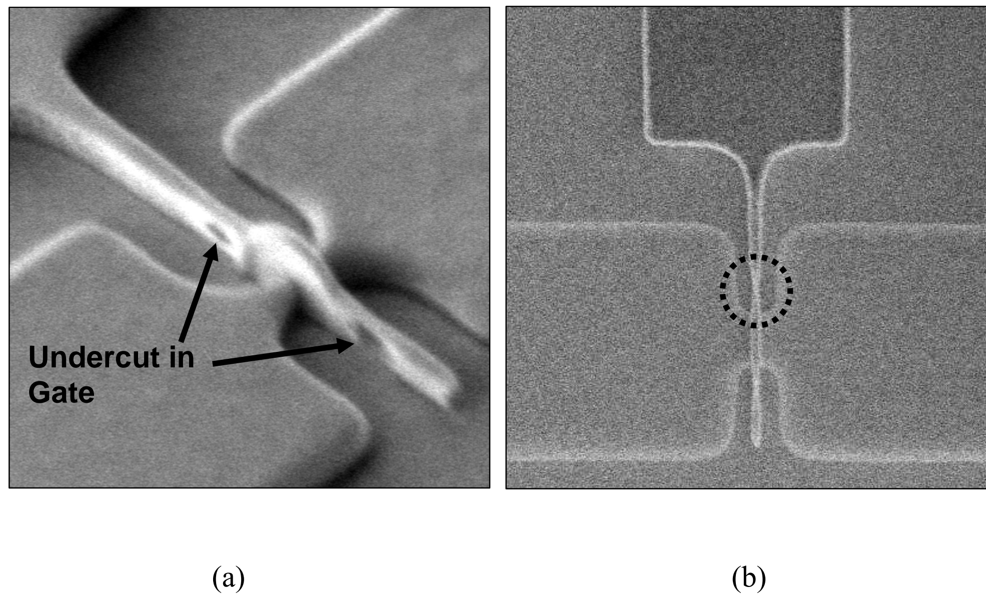
Fig. 3.2. SEM image of a FinFET device formed without an extended gate over-etch step, showing the existence of an uncleared gate stringer surrounding the active region. This leads to increased overlap capacitance and reduced circuit speed.

performed in this case depends on the fin height H_{Fin}, and also on the uniformity of the gate deposition process. From a device perspective, the device width of a triple-gate FinFET is given by ($2H_{Fin} + W_{Fin}$) [3.7]. Since a taller fin gives a higher drive current and better layout efficiency, tall fins are desirable. Nevertheless, the gate-stringer will be thicker when the fin is taller.

An extended over-etch step for gate stringer removal is required and this places a greater process challenge on the FinFET gate-etch. Furthermore, in the fabrication of a triple-gate transistor where the top surface of the fin is cover by an ultrathin gate dielectric, a higher etch selectivity between the gate electrode and the gate dielectric material is required since the gate dielectric on the top surface of the fin would have been exposed during the gate stringer removal or over-etch step. Alternatively, a thick fin hardmask can be adopted and this can helps to protect the fin during the extended over-etch process for the clearing of the gate

residue. This method was actually adopted in chapter 2 to protect the fin during metal gate etch process. However, due to the thicker fin hardmask at the top surface, the effective conduction channel will only be from the 2 sidewalls, making this a double-gate FinFET device. For better short channel effects control, a Tri-gate FinFET is preferred over the double-gate FinFET structure [3.8] and hence the process development done in this chapter allows us to fabricate a Tri-gate FinFET device to be used in later works.

Figure 3.3(a) shows a SEM image of a FinFET structure that underwent excessive gate over-etch step with a long over-etch time. The gate etch process used to form the structure in Fig. 3.3 is detailed in Table 3.1. As observed in the SEM image, the gate stringer can be cleared but this resulted in a broken gate line.



(a) (b)

Fig. 3.3. (a) SEM image of a FinFET that underwent excessive gate over-etch process. The lateral etch component during the over-etch step leads to significant gate uncut. The gate line can be broken at the narrowest portion or where there is severe line-edge roughness. (b) SEM image showing the top-view of a FinFET with gate-pattern. The gate line is narrowest at both sides of the silicon fin.

Step	Power (W)	Etchants (sccm)	Time (s)
Breakthrough	300	CF_4 (35)	5
Main Etch	350	HBr (70), Cl_2 (30), He-O_2 (5)	Endpoint
Over Etch	200	HBr (60), Cl_2 (20), He-O_2 (6)	20

Table 3.1. Gate-etch process conditions used to form the FinFET structure in Fig. 3.3. Etchants used and the flow-rates are included. The main etch employed end-point detection.

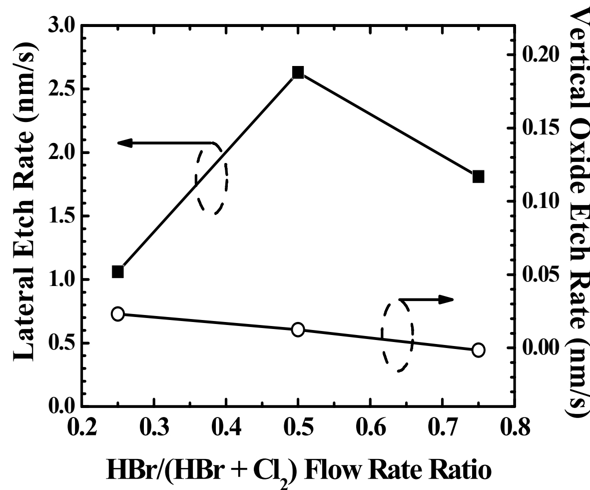


Fig. 3.4. Lateral etch rate of a silicon gate electrode (left axis) and vertical etch rate of silicon oxide (right axis) with varying HBr/(HBr + Cl_2) flow rate ratio.

This is because the extended gate over-etch step is significantly isotropic and the lateral etch component leads to an under-cut etch occurring at the sidewalls of the gate. This causes the gate line to break for very small linewidths or where there is significant line-edge roughness. An example is shown in Fig. 3.3(b) where the narrowest portion of the gate lines is broken.

In order to reduce the lateral etch rate in the over-etch step, the etchant composition was varied. To monitor the amount of lateral etch, the hardmask CD was measured prior to the gate etch, and the poly gate CD was measured after etch

and hardmask removal using dilute HF. The difference between the hardmask CD and the gate CD after etch was used to obtain the lateral etch rate. Figure 3.4 plots the lateral etch rate as a function of the HBr/(HBr + Cl_2) flow rate ratio. The maximum lateral etch rate occurs at 50% HBr composition in a mixture of HBr and Cl_2. The vertical etch rate of silicon oxide is not affected much by changing the gas composition, which may be attributed to the low RF power used. By tuning the over-etch step, we could effectively reduce the amount of gate undercut, achieving a minimum undercut etch rate of about 1 nm/s for the range of HBr/(HBr + Cl_2) flow rate ratio used in this work.

Another approach to limit the extent of lateral etch of the FinFET gate electrode is investigated in this work: increase the amount of gate sidewall passivation layer which provides some protection of the gate electrode from a

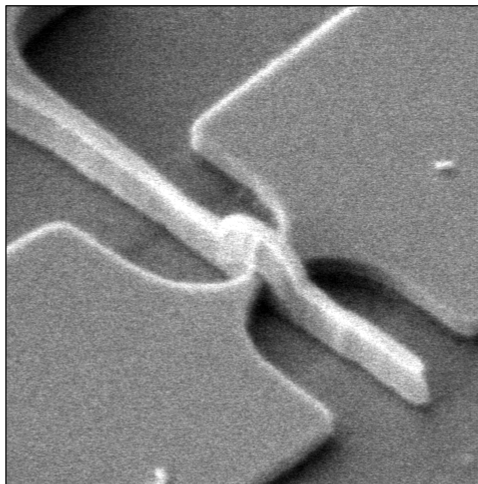


Fig. 3.5. By increasing the He-O_2 flow rate in the main etch step from 5 to 18 sccm, increased sidewall surface passivation was achieved. This contributed to adequate sidewall protection during the over-etch step. Consequently, the FinFET gate electrode did not suffer from an undercut even during the extended over-etch step, as shown in the SEM image.

lateral undercut [3.10] (Fig. 3.3). With a prolonged over-etch step, as in the case of FinFET gate etching, a thin passivation layer would have been fully consumed. This also contributed to the problem illustrated in Fig. 3.3(a). In this work, we modified the main etch step such that a thicker sidewall passivation layer is deposited. This is achieved by increasing the flow rate of He/O_2 in the main etch step from 5 sccm to 18 sccm. Figure 3.5 shows a SEM image of a FinFET structure formed with the improved main etch step and with a $HBr/(HBr + Cl_2)$ flow rate ratio of 0.75 in the over-etch step. No uncut profile was observed and gate electrodes with very small critical dimension can be achieved. Table 3.2 summaries what has been achieved in this work.

Poly Gate Etch	**Poly Stringer**	**Poly Gate Breakage**
Original Recipe	Yes	No
Original Recipe + Additional OE	No	Yes
Newly Developed Recipe	**No**	**No**

Table 3.2. The newly developed poly gate etch recipe has neither poly stringer nor poly gate line breakage issues.

3.4 Summary

To summarize, gate etch issues related to the removal of gate stringer in FinFET device fabrication was explored. Process optimization of the gate over etch step and the main etch step was performed, and the underlying etch chemistry was discussed. This allowed the successful removal of gate stringer for the fabrication of FinFET devices with Si or SiGe growing on the fin sidewalls at the S/D region for the reduction of series resistance and hole mobility enhancement.

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Chapter 4

Strained P-channel FinFET with Enhanced SiGe S/D Stressor

4.1 Sub-30 nm Strained p-Channel FinFETs with Condensed SiGe Source/Drain Stressors

4.1.1 Background

To meet the requirement for high drive current, mobility-enhancing strain technology can also be applied on FinFETs. For p-channel transistors, SiGe source and drain (S/D) stressor is commonly used to induce strain in the device channel. By making use of the lattice mismatch between Si and SiGe, compressive strain can be induced in the channel to enhance hole mobility. For enhanced strain effect, a recess etch can be performed on the S/D region prior to the SiGe epitaxial growth to realize embedded SiGe S/D stressors [4.1], [4.2]. The fabrication of p-channel FinFETs with embedded SiGe S/D has been demonstrated by Verheyen *et al.*, [4.3] achieving an I_{Dsat} enhancement of 25% over control FinFETs. Their integration scheme involved an anisotropic S/D recess etch prior to SiGe epitaxy on the top surface. However, for maximum effect, an isotropic etch should be performed on the S/D regions and the SiGe epitaxial layer should also be grown on the sidewalls [4.4],[4.5]. This is illustrated in Fig

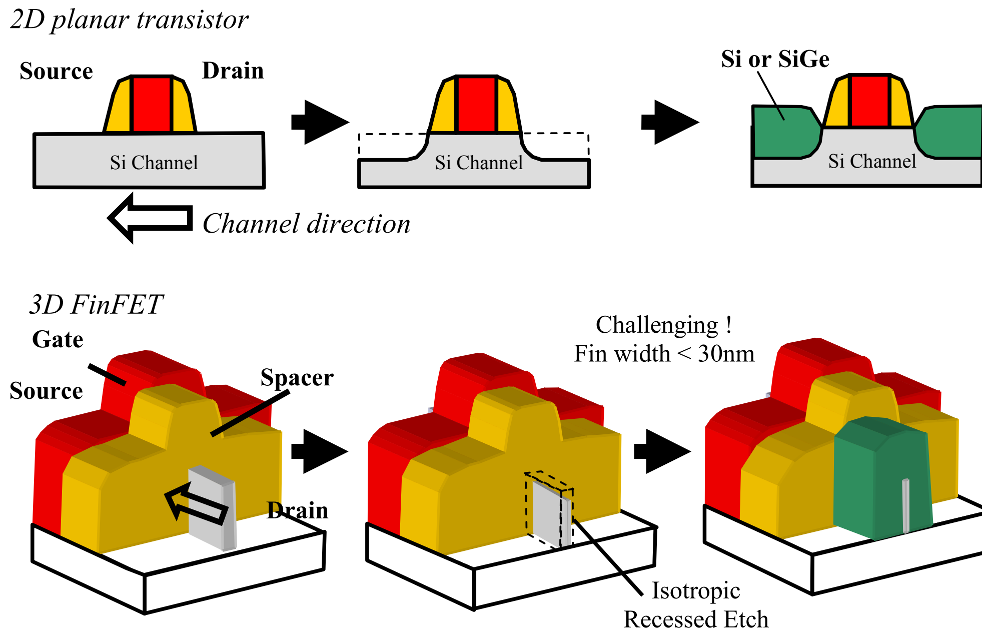


Fig. 4.1. Illustration of the scheme for FinFET with SiGe S/D stressor based on that of the bulk devices.

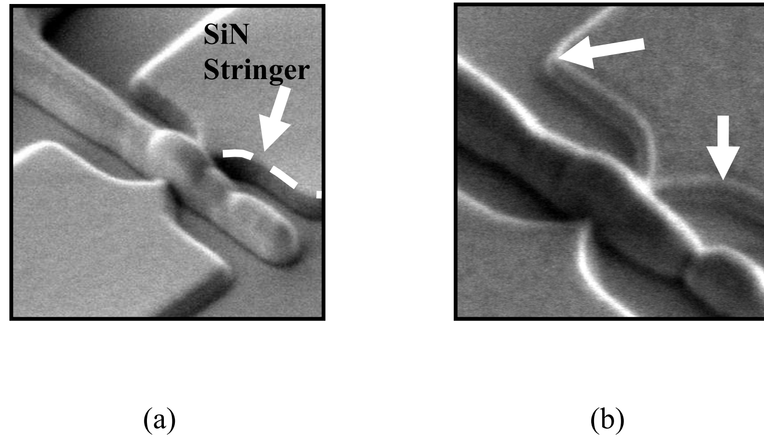
4.1 in which a comparison to bulk device with embedded SiGe S/D stressor was made.

Unlike the planar device, the major conducting surfaces of the FinFET devices came from the sidewalls of the fin, having a surface orientation of (110). To exert a strain in the channel similar to that of the planar 2D devices, an embedded SiGe around the fin at the S/D regions will have to be formed as shown in Fig. 4.1. However, to fabricate such a structure can be quite challenging especially when the fin width W_{fin} is scaled down drastically to less than 10 nm for better SCE control. A very precise isotropic S/D recess etch will be needed to control the etch depth, without etching away the entire fin. Conversely, local Ge condensation has been reported as an alternative technique for the fabrication of embedded SiGe S/D stressors, eliminating the need for a recess etch [4.6]. In this chapter, we report the first demonstration of sub-30 nm tri-gate FinFETs with embedded SiGe S/D stressors formed using a novel local condensation process.

Compressive stress is exerted on the channel from the SiGe S/D regions on both the top and sidewalls.

4.1.2 Device Fabrication

Silicon-on-insulator (SOI) substrates with 35 nm thick Si were used. Threshold voltage V_t adjust implant was performed. Fin patterning employed 248 nm lithography, resist trimming, and reactive ion etching (RIE) to achieve W_{fin} down to 30 nm. Sacrificial oxidation was performed to repair the fin sidewall damage due to the RIE. SiO_2 gate dielectric (~3 nm) was thermally grown, followed by poly Si gate deposition and gate definition. During the silicon nitride (SiN) ~ 40 nm spacer formation process, an optimized over-etch time was used for the removal of SiN stringer at the fin sidewall as shown in Fig. 4.2. Figure 4.2(a) show a FinFET structure with the SiN spacer stringer remaining at the sides of the fin which prevent the growing of SiGe at the fin sidewalls for maximize strain effects. The spacer stringer was therefore cleared away by increasing the time during the over etch step as shown in Fig. 4.2(b). The removal of the nitride stringer will require careful tuning because if this is done excessively, the poly Si gate may get exposed at the top corners as shown in Fig. 4.3. In the subsequent SiGe epitaxy process, SiGe can also grown at the exposed gate corners causing possible short between the gate and the S/D regions. To prevent this, the thickness of poly gate, hardmask and fin height will have to be adjusted accordingly. Selective epitaxial growth of SiGe, having a Ge concentration of 25 % was then performed on all wafers using an ultra high vacuum CVD system. Figure 4.4 shows a SEM image of a FinFET with the S/D region of the fin and contact covered by the SiGe epi-layer. The existence of epitaxial SiGe on the fin



(a) (b)

Fig. 4.2. SEM images of FinFET devices showing (a) SiN spacer etch to end-point with the nitride stringer remaining at the sides of the fin. (b) Extensive spacer over etch is done to remove the nitride stringer as shown.

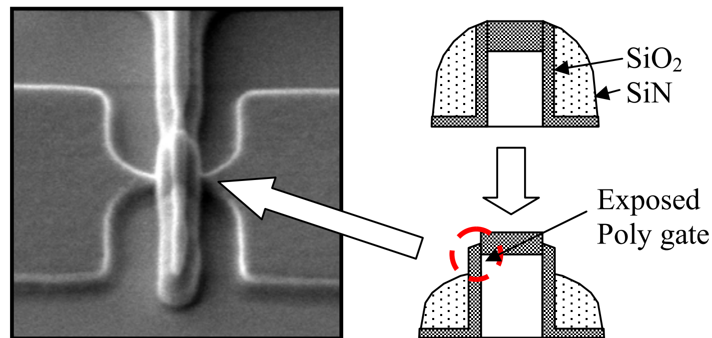


Fig. 4.3. SEM image of the FinFET device showing the expose of the gate corner when excessive spacer nitride is done. This result in the risk of shorting between the gate and S/D regions when selective epitaxy is performed.

sidewall and top surfaces in the S/D regions was clearly observed. The inset in Fig. 4.4, shows a TEM image of the gate having a gate length of 26 nm. On one device structure with SiGe S/D, Ge condensation, which is essentially a thermal oxidation process, was performed at 950°C for 5 min. This temperature was chosen following [4.6], as Ge diffuse faster at 950°C than 900°C. For the control wafer, the Ge condensation process step was skipped. The Ge condensation will be described in more detailed in section 4.1.3. Source/Drain implant and anneal

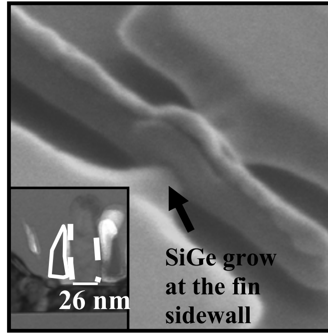


Fig. 4.4. SEM image of the FinFET device with SiGe raised S/D grown even at the side of the fin at the S/D regions. The inset shows a TEM image of the gate having a gate length of 26 nm.

were performed after the removal of gate hardmask to complete the fabrication process. As the thermal budget due to Ge condensation is quite high especially with the used of a furnace oxidation system, S/D extension implantation was not done. To reduce the series resistance, a thinner spacer can be used in the future. Direct probing was done to obtain the electrical characteristics of the device.

4.1.3 Ge Condensation Process

Ge condensation is basically used to describe the oxidation of SiGe film. It is reported that during the oxidation of SiGe film, Ge is rejected from the oxide and this caused a pile up of Ge at the interface between top SiO_2 layer and SiGe [4.7]. A proposed explanation [4.8] is that, Si_xGe_{1-x} alloy and GeO_2 cannot coexist at equilibrium unless the concentration of silicon in Si_xGe_{1-x} is below 1.6×10^4 atoms/cm^3. When Si_xGe_{1-x} is in contact with GeO_2, the latter will be reduced according to the reduction reaction

$$Si + GeO_2 \rightarrow SiO_2 + Ge \quad \text{eq. 4.1}$$

When the Ge atoms get rejected from the oxide, the Ge concentration at the interface can be much higher than the as-grown Ge concentration depending on the oxidation conditions. This property is used in the fabrication of SiGe on insulator [4.9] or even Ge on insulator [4.10] wafer. In addition, local Ge condensation had also been demonstrated on the S/D regions to form a strained p-channel transistor with embedded SiGe S/D. The Ge concentration in the S/D regions has also been observed to have increased [4.6].

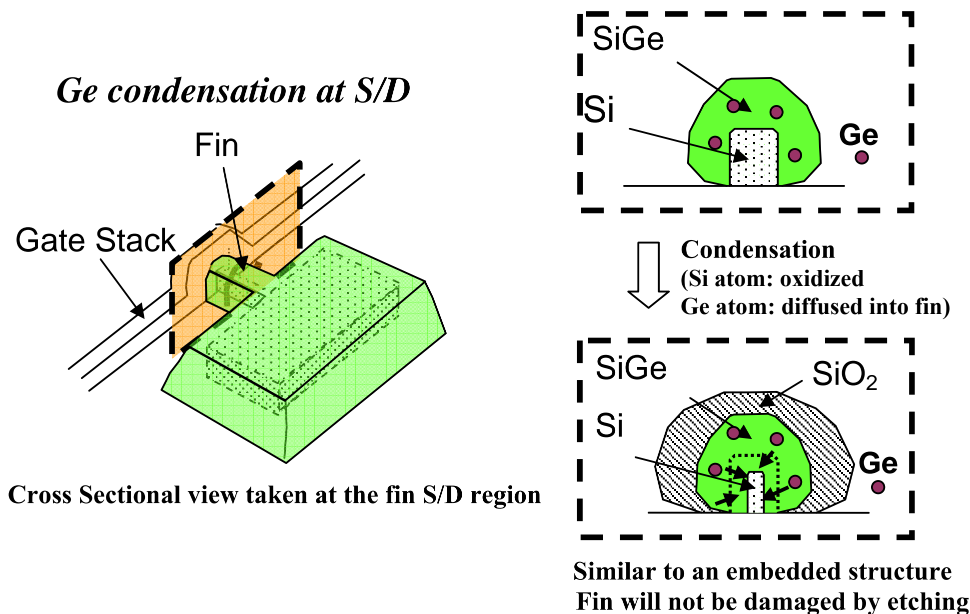
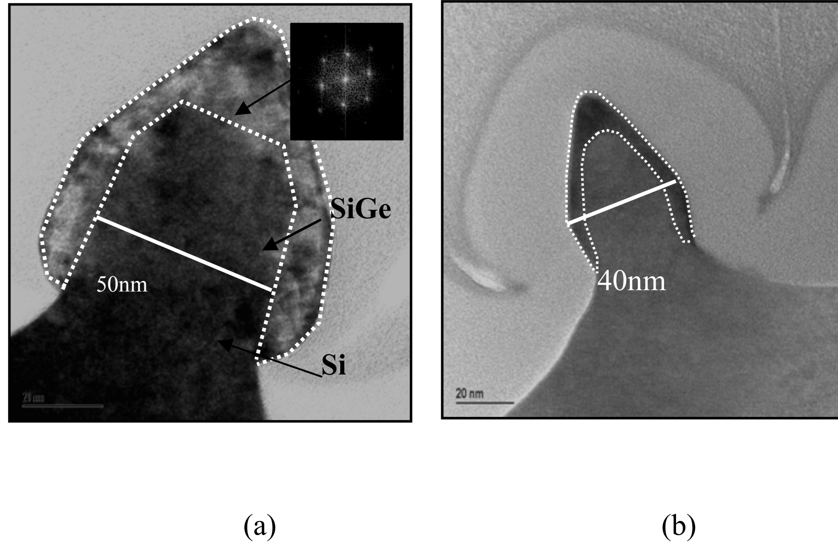


Fig. 4.5. Schematics of propose scheme using Ge condensation to form FinFET with embedded SiGe at the fin S/D regions.

In this work, we proposed to use the Ge condensation technique for the formation of FinFET with embedded SiGe S/D stressor. This is illustrated in Fig. 4.5, where SiGe was first selectively grown on the S/D regions and followed by an oxidation process. Ge atom is therefore rejected from the SiO_2 formed and move further into the fin. A fin with an embedded SiGe is thus formed without any damage to the fin itself. From this schematic, we can also see that for the SiGe to



(a) (b)

Fig. 4.6. (a) TEM image of a fin structure with SiGe grown on the top (100) and the sidewall (110) surfaces. (b) Ge diffuses into the fin after condensation at 950^0C for 20 mins in an oxygen ambient.

be embedded on all 3 sides, the residual gate and spacer stringers at the sides of the fin will have to be removed. Ge condensation on fin structure was also studied by first growing SiGe (25% Ge) on fin test structures.

Figure 4.6(a) shows the Transmission Electron Microscopy (TEM) image of the fin after the epitaxy process. The inset of Fig. 4.6(a) shows the diffractogram image taken at the SiGe layer, showing the good crystalline quality. From Fig. 4.6(a), it can be observed that the thickness of SiGe is larger at the top when compared to the sidewalls indicating a higher growth rate for the (100) surface orientation as compared to the (110) surface. Similar findings were also reported in [4.12]. A longer growth time will therefore be needed to grow the SiGe at the sidewalls for the FinFET structure for a targeted thickness as compare to a planar device. Ge condensation was performed on this structure at 950°C for 20 min and Fig. 4.6(b) shows the TEM image of the fin after the condensation process. In Fig. 4.6(b), it is observed that the Ge has diffused into the Si fin from all the three

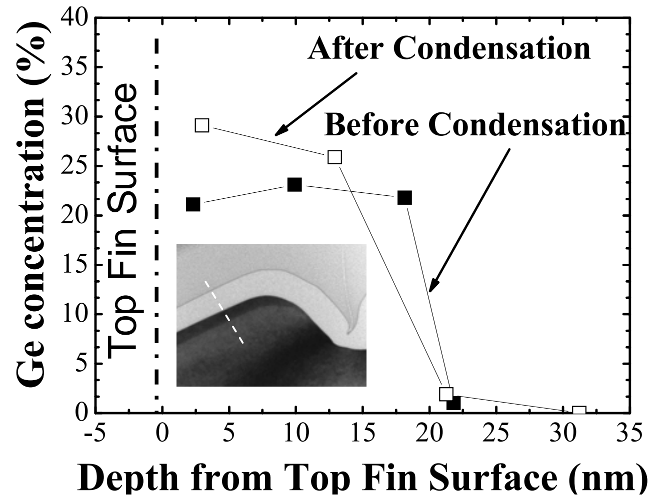


Fig. 4.7. EDX taken from the top of a larger fin test structure showing the increase in Ge concentration after condensation.

sides, creating a SiGe profile that is similar to an epi-grown SiGe layer on an isotropically recess-etched fin. An embedded SiGe at the S/D region of the fin is thus created, eliminating the need for a recess etch that will become increasingly challenging as the fin width becomes smaller. Even if the isotropic recess etch can be achieved, Si migration may also become a problem for such thin Si fins during the SiGe epitaxy process [4.13]. The oxidation of SiGe in the (110) surface orientation is also observed to be faster when compared to the (100) surface orientation. By optimizing the process and the dimensions of the fin, it is also possible to achieve a higher Ge concentration at the S/D regions due to the piling up of Ge atoms [4.9], thereby enhancing the effect of strain further as shown also by Fig. 4.7.

4.1.4 Results and Discussion

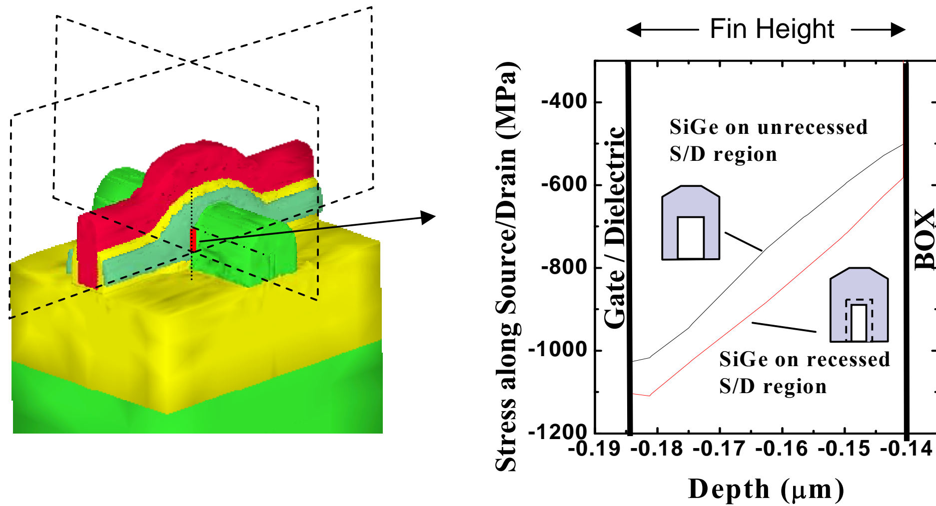


Fig. 4.8. Stress simulation for FinFET (fin width = 20 nm) with recessed profile (embedded SiGe) shows a larger compressive strain in the channel when compare to an unrecessed S/D.

Three-dimensional stress simulation was performed using Taurus Process simulator. Comparison was made between a FinFET with SiGe S/D structure having a 5 nm recessed profile on both the sides and top of the fin to a FinFET with epitaxial SiGe grown on un-recessed S/D regions. The former structure simulates the stress effect for the FinFET device that undergoes an additional Ge condensation step (FinFET with embedded SiGe S/D) while the latter simulates the control device (FinFET with non-embedded SiGe S/D). As shown in Fig. 4.8, the compressive stress along the S/D direction at the center of the channel is found to be larger for the FinFET having an embedded SiGe S/D. For both types of FinFET structures, the magnitude of compressive stress decreases from the top to bottom of the fin. The average stress of the FinFET with embedded SiGe S/D is consistently larger than that of the control. Hence, better device performance can be expected for the FinFET with embedded SiGe S/D.

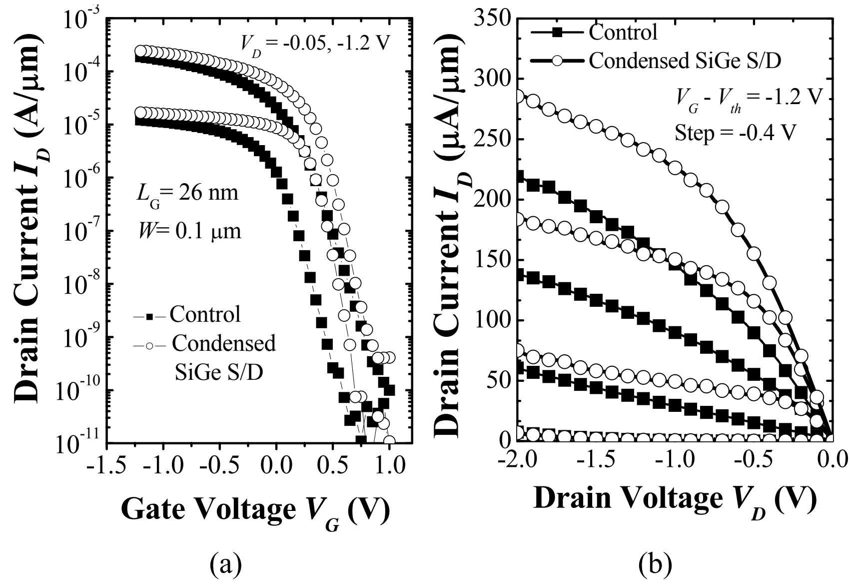


Fig. 4.9. (a) I_D-V_G characteristics of FinFET devices having an L_G of 26 nm. (b) I_D-V_D characteristics of FinFET devices at various gate overdrives (V_G-V_{th}). FinFET with condensed SiGe S/D shows a higher drive current.

The drain current I_D versus gate voltage V_G characteristics of a FinFET with a condensed SiGe S/D and the control device are shown in Fig. 4.9 (a). The L_G = 26 nm FinFET with condensed SiGe S/D shows a subthreshold swing of ~100 mV/decade and drain induced barrier lowering (DIBL) of 0.13 V/V. It can also be observed that the additional condensation step does not degrade the performance of the FinFET. The difference in DIBL between the control and the FinFET with condensed SiGe S/D maybe attributed to the control device having a smaller effective length due to process differences. Since an extension S/D implantation is not done, the effective gate length will depend on the deep S/D implant, and the activation steps. While these are kept the same for both control and FinFET with condensed SiGe S/D devices, the Ge concentration profile in the S/D region for the latter may be different and it has been reported that Ge can retard boron diffusion and thus affect the effective gate length.

The I_D-V_D characteristics of the devices are plotted in Fig. 4.9(b) at various gate overdrives (V_G - V_{th}). At a gate overdrive of -1.2 V, FinFET with condensed SiGe S/D shows a 28% higher I_{Dsat} than the control device. This is possibly attributed to a recessed Ge profile and an increased Ge concentration for larger strain effects. FinFET with condensed SiGe S/D also shows a larger peak tranconductance than the control device as observed in Fig. 4.10(a), indicating a higher hole mobility which can be attributed to the enhanced strain effect. As shown in Fig. 4.10(b), the two devices have comparable source/drain series resistances. This can be deduced from the plot of the total channel resistance R_{tot} ,

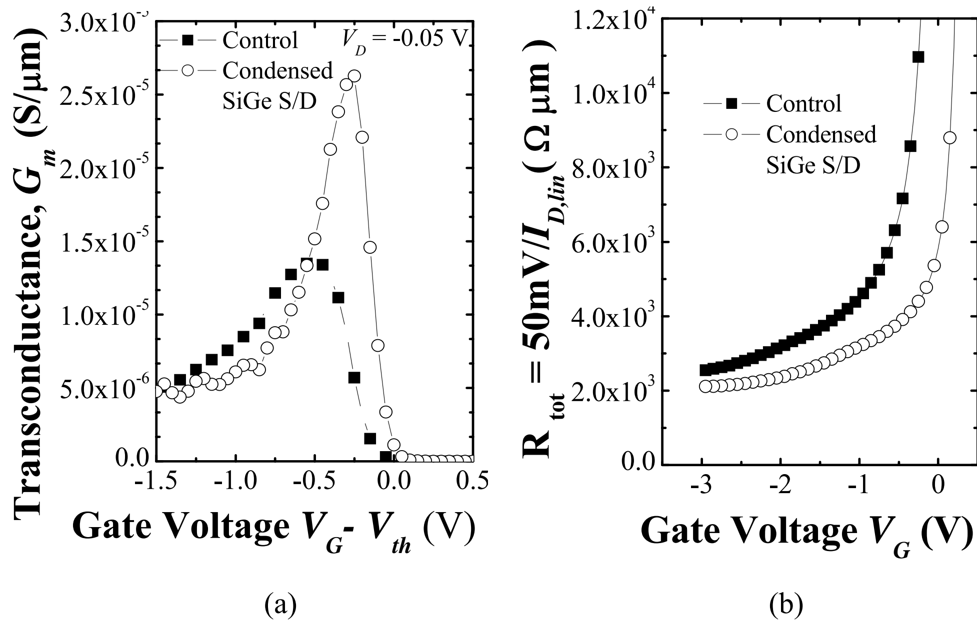


Fig. 4.10. (a) Comparison of transconductance G_m at the same gate overdrive, illustrating an enhancement of 91% for the FinFET with condensed SiGe S/D over the control device. (b) Extraction of series resistance by examining the asymptotic behavior of the total resistance at large gate bias.

where

$$R_{tot} = \frac{V_{DS}}{I_D} = R_{CH} + R_{SD} \text{ , ...eq. (4.1)}$$

as a function of gate voltage as seen in eq. 4.1. As V_G increases, R_{CH} decreases and at large $|V_G|$, it is assumed that the channel resistance is much smaller than the series resistance R_{SD} [4.11]. This is evident from the asymptotic behavior of the curve, which tends towards the source/drain series resistance at large $|V_G|$.

4.1.5 Summary

P-channel FinFETs with condensed SiGe S/D regions were demonstrated for the first time, with gate lengths down to 26 nm. 28% drive current enhancement was observed in comparison with a FinFET with an uncondensed SiGe S/D. The Ge condensation process leads to a more recessed Ge profile in the S/D regions and possibly higher Ge concentration, both of which give rise to higher uniaxially compressive channel strain for hole mobility enhancement. A FinFET with embedded SiGe S/D stressor can therefore be fabricated without the use of an isotropic recess etch process that becomes increasingly challenging as fin dimensions scale down.

4.2 Novel Extended-Pi Shaped Silicon-Germanium (*e*Π-SiGe) Source/Drain Stressors for Strain and Performance Enhancement in P-Channel FinFET

4.2.1. Background

As mentioned earlier, since the majority portion of the current will be flowing on the sidewalls, to better exploit the strain effects, the SiGe S/D stressor has to be

grown on the fin sidewalls as well. This requires the removal of all the stringer materials formed at the sidewalls of the fin which is necessary for the formation of a Π-shaped S/D stressor. Nevertheless, even for fins stressed by the Π-shaped S/D, the stress distribution in the Si fin still shows lower stress at the foot of the fin due to limited SiGe growth (geometrical effects on epitaxial growth) or stressor volume, and the non-compliance of the buried oxide (BOX). This can be seen also in the simulation results shown in Fig. 4.8 where the compressive stress is observed to be smaller at the foot of the fin as compared to the top. A novel extended-Pi SiGe (*e*Π-SiGe) S/D stressor with significantly enhanced strain effects to boost the performance of p-channel FinFETs was thus proposed. FinFET having different orientations were studied which verified the effect of strain.

In addition, the relation of fin width and the strain effect due to *e*Π-SiGe S/D stressor was reported for the first time. Compared to FinFETs with Π-shaped SiGe S/D, FinFETs with the *e*Π-SiGe S/D have higher strain in the fin channel, leading to further performance improvement without any additional cost or process complexity.

4.2.2 Device Fabrication

The process flow for the fabrication of p-channel FinFET is similar to the one mention in section 4.1.2. The fin height is 30 nm and W_{fin} down to 60 nm is fabricated. The fin hard mask was removed for the fabrication of a tri-gate FinFET device and 3 nm SiO_2 was used as the gate dielectric. Unlike the FinFET

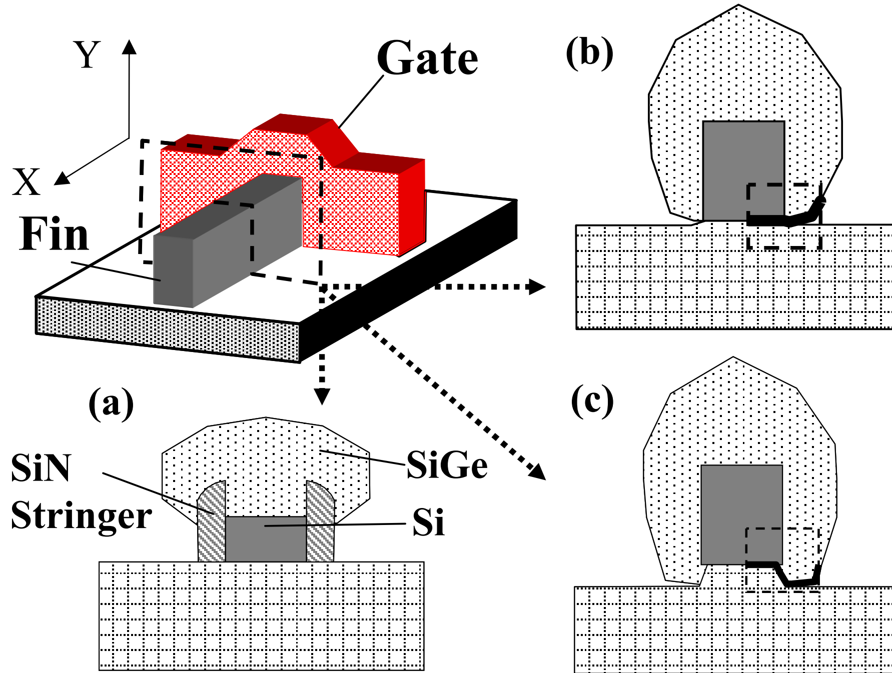


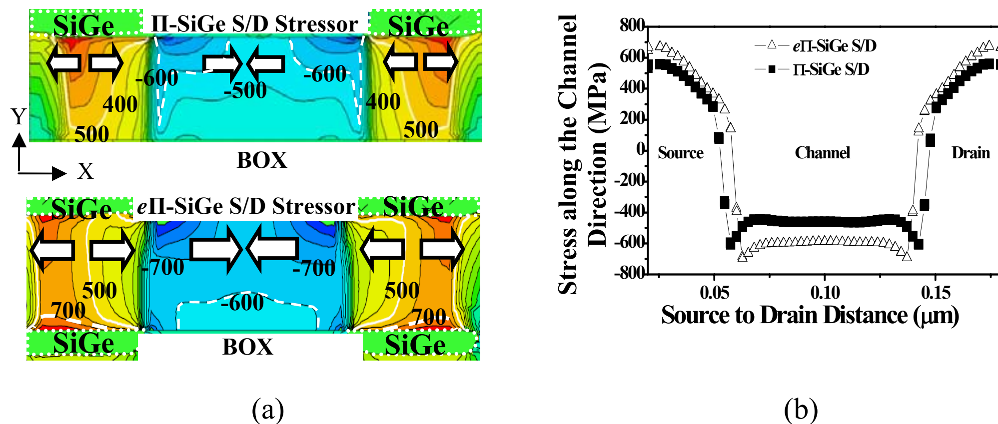
Fig. 4.11. (a) SiGe S/D stressor from ref. 4.3. This work realizes (b) Π-SiGe S/D stressor. (c) *e*Π-SiGe S/D stressor with SiGe growth below the BOX.

device with condensed SiGe S/D stressor, S/D extension implantation was performed in this work. Similarly, in the spacer formation process, SiN stringers at the base of the fins were removed to enable epitaxial growth of SiGe on the fin sidewalls. If the SiN stringers were not removed, SiGe S/D can only grow on the top surface of the fin [Fig. 4.11(a)]. The SiN stringer was removed by extending the over etch step and at the same time, the ratio of fin to gate height is taken into consideration to ensure sufficient SiN spacer remained after etching.

Prior to the growth of SiGe at the S/D regions, a pre-epitaxy cleaning step is needed. For the device in which FinFETs with *e*Π-SiGe S/D will be formed, an extended pre-epitaxy clean was done using HF (4%) solution. The extended HF clean of 120 s as compared to the usual 30 s, formed a recess in the buried oxide

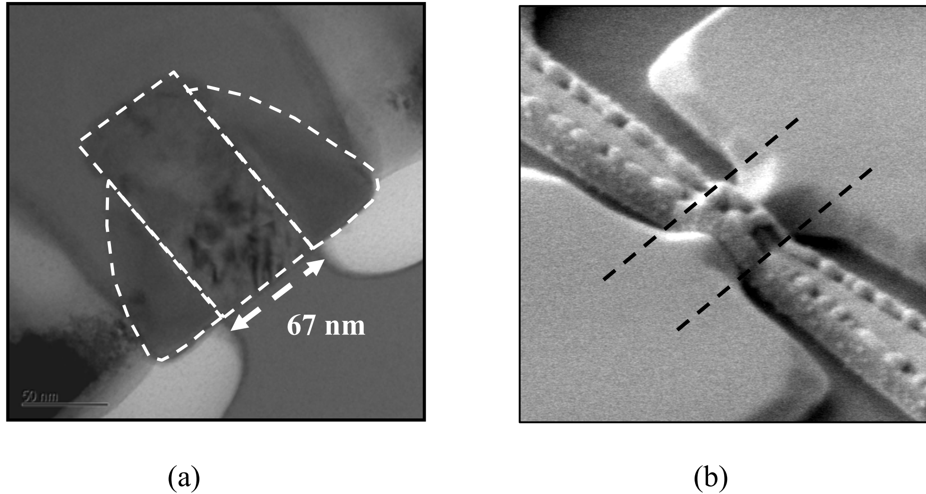
which exposed a portion of the bottom surface of the fin. The etch rate of thermally grown oxide is ~10 nm/min using this HF bath. Selective epitaxial growth of SiGe having a Ge concentration of 25% was then performed. Fig. 4.11 (b) shows the cross-sectional profile of a fin (without SiN stringer) with SiGe S/D grown on the fin sidewalls, forming a Π-shaped SiGe S/D. Fig. 4.11(c) shows the *e*Π-SiGe S/D which extends into the buried oxide and encroaches under the Si fin to give a more highly strained Si fin. S/D formation, oxide passivation, and metallization were performed to complete the devices. We shall compare the performances of FinFETs with Π-SiGe S/D [Fig. 4.11(b)] and *e*Π-SiGe S/D [Fig. 4.11(c)].

4.2.3 Results and Discussion



(a) (b)

Fig. 4.12. (a) Simulated stress (in MPa) for Π-SiGe (top) and *e*Π-SiGe S/D stressor (bottom) stressors. Contour interval is 100 MPa. L_G = 30 nm, W_{fin} = 30 nm. Si at S/D and channel region is under tensile and compressive strain respectively. (b) Simulated stress along the channel direction taken near the bottom of the fin. *e*Π-SiGe S/D stressor has a larger tensile stress near to the BOX at the S/D region which result in a higher compressive stress in the channel.

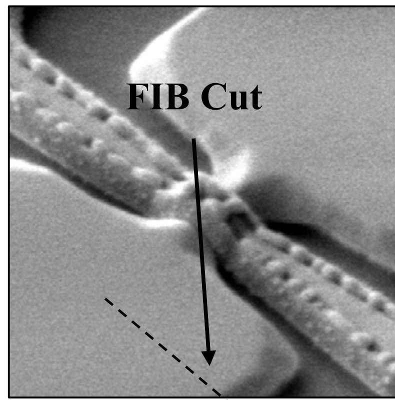


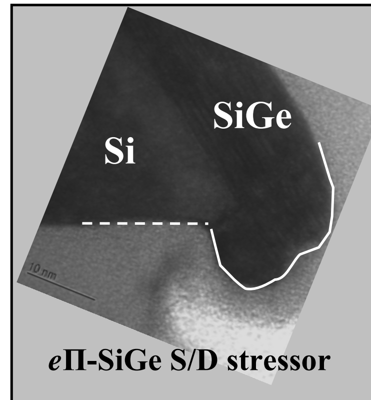
(a) (b)

Fig. 4.13. (a) TEM image of the gate profile taken along the S/D direction shows a gate length of 67 nm. (b) SEM image shows the FinFET having a raised SiGe S/D.

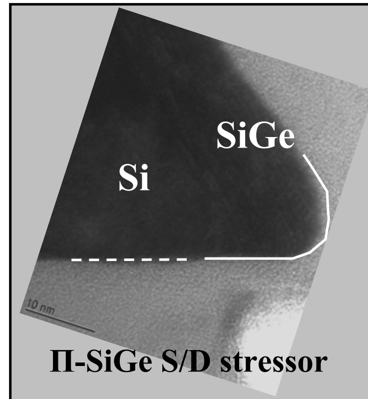
Figure 4.12(a) shows the results of a 3D stress simulation for a FinFET having *e*Π-SiGe S/D stressors. The recess in the BOX is 6 nm. A 2D cross-sectional view was taken close to the fin sidewalls so that SiGe regions of the *e*Π- SiGe stressor appear on the top and bottom of the Si fin in the S/D regions. The Si fin in the S/D region is under tensile stress (indicated by arrows in Fig. 4.12 (a)). This tensile stress in the S/D is larger in the device with *e*Π-SiGe S/D as compared to the case for device with Π-SiGe S/D, attributed to the additional growth of SiGe at the bottom of the Si fin regions. Consequently, the channel stress is more compressive for the FinFET with *e*Π-SiGe S/D stressors, as portrayed in Fig. 4.12(b).

Figure 4.13(a) shows the TEM gate stack image of the fabricated device, indicating a gate length L_g of 67 nm. Although an extended SiN spacer over etch was performed, sufficient SiN spacer remained, to prevent shorting of the gate to the S/D regions. TEM images are also taken at the edge of the S/D pad for both Π-SiGe and *e*Π-SiGe S/D devices as shown in Fig. 4.14. For the *e*Π-SiGe





(a) (b)



(c)

Fig. 4.14. (a) SEM image of the FinFET device with SiGe S/D. (b) and (c) TEM images taken at the edge of the FinFET device near the S/D region. SiGe is observed to have grown below the bottom of the fin for the *e*Π-SiGe S/D device.

structure, the recess in the BOX is clearly seen which is a result of using a longer HF cleaning time. This recess allows the growth of SiGe below the base of the Si fin (Fig. 4.14 (b)) which is not observed for the Π-SiGe structure where the BOX is not recessed (Fig. 4.14 (c)). The slightly larger cross-sectional profile of the *e*Π-SiGe stressor as compared to the Π-SiGe stressor could also lead to a slightly lower series resistance. The additional SiGe growth at the foot of the fin also

enhances the channel strain contribution from the SiGe S/D stressors. The slight encroachment of the eΠ-SiGe stressor beneath the fin may be desirable for high stress effects, however very tight process control on the amount of lateral encroachment in the buried oxide recess etch will be required for narrow (e.g. sub-20 nm) fin. A more diluted HF solution can be used, to achieve slower oxide etch rate for better controllability.

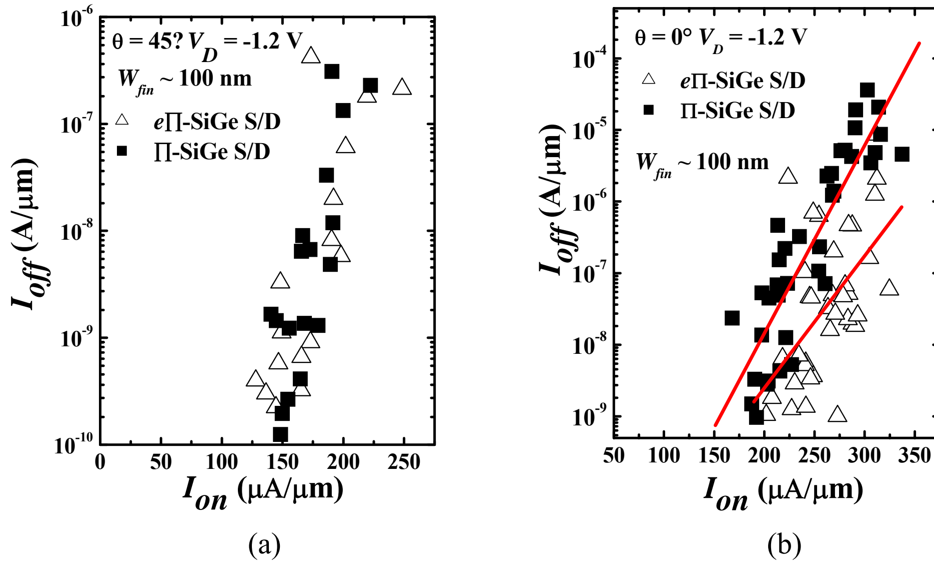
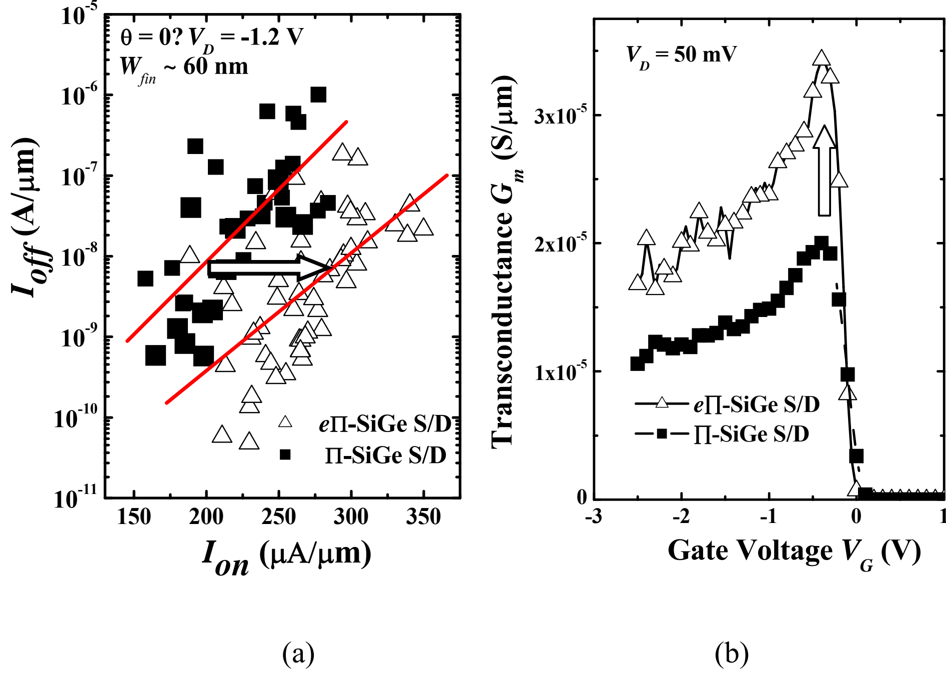


Fig. 4.15. (a) I_{off} (V_G = 0.15 V) - I_{on} (V_G = -1.05 V) comparison showing not much difference between *e*Π and Π-SiGe S/D stressors for FinFETs having <100> channel direction. (b) I_{off} (V_G = 0.15 V) - I_{on} (V_G = -1.05 V) comparison shows an I_{on} enhancement of 21% at I_{off} = 1×10^{-7} A/μm for FinFET having *e*Π-SiGe S/D stressor over Π-SiGe S/D stressor. Channel direction is <110>.

Alternatively, a vertical buried oxide recess can also be considered which we believed will also enhance device performance with less challenges in process. FinFETs having W_{fin} of 100 nm are first examined along 2 orientations, <110> and <100>, as shown in Fig. 4.15 (θ of 0° and 45°) with strong (+75) and weak (+10) piezoresistance coefficients, respectively [4.15]. Figure 4.15 (a) plots the I_{off}-I_{on} data for <100>-oriented (θ = 45°) FinFETs with Π-SiGe and *e*Π-SiGe S/D, showing little difference due to the negligible piezoresistance effect for that



(a) (b)

Fig. 4.16. (a) I_{off} (V_G = 0.15 V) versus I_{on} (V_G = -1.05 V), showing larger enhancement [~50% at $I_{off} = 1\times10^{-8}$ (A/μm)] for W_{fin} of 60 nm over 100 nm. (b) FinFET with *e*Π -SiGe SD shows a 71% transconductance enhancement.

orientation. The L_G of the devices are from 60 nm to 80 nm. Figure 4.15(b) reveals that if the channel orientation is <110> (θ = 0°), FinFETs with *e*Π-SiGe S/D give a 21% larger I_{on} at an I_{off} of 100 nA/μm over FinFETs with Π-SiGe S/D.

Figure 4.16(a) shows the I_{off}-I_{on} plots for FinFET with Π-and *e*Π-SiGe S/D stressors having W_{fin} of 60 nm. When W_{fin} is reduced from 100 to 60 nm, a larger enhancement in I_{on} from 21% to 50% can be observed. This is possibly attributed to a larger strain effect and also a larger I_{on} contribution by the sidewalls which benefits more from the *e*Π-SiGe S/D. It can also be observed in 4.16(b) that a significant 71% increase in the peak G_m value is obtained for FinFET having *e*Π-SiGe S/D, indicating higher hole mobility. Figure 4.17 shows the I_D-V_G characteristics of FinFETs with Π-SiGe and *e*Π-SiGe S/D (W_{fin} of 60 nm), having similar subthreshold swing and DIBL. SCEs are therefore not compromised with

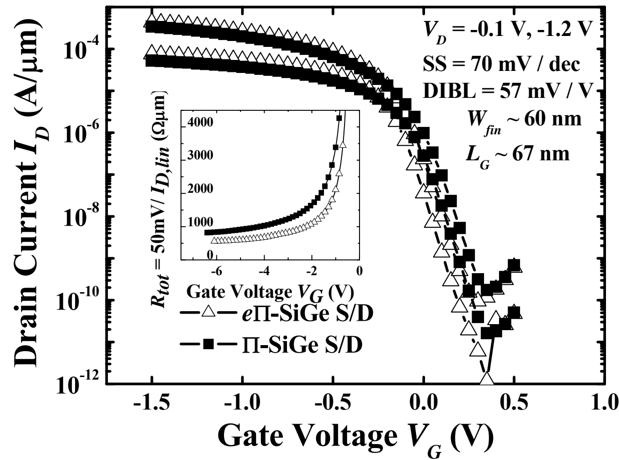


Fig. 4.17. I_D-V_G characteristics of FinFET having *e*Π and Π-SiGe S/D stressors shows similar subthreshold swing and DIBL value. Inset shows that the series resistance for FinFET with *e*Π-SiGe S/D stressors is slightly lower.

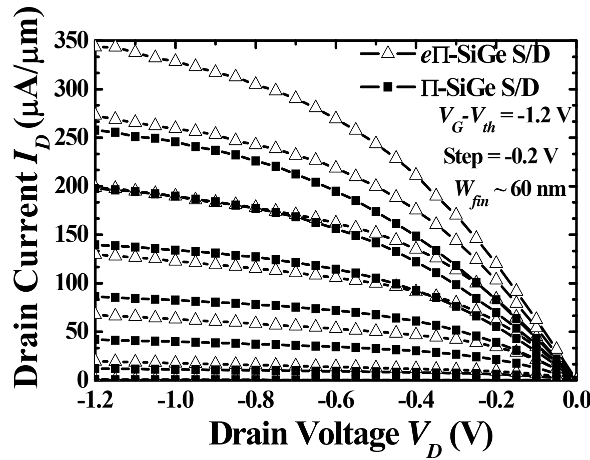


Fig. 4.18. I_D-V_D characteristics of both types of devices showing a higher drive current for FinFET having *e*Π-SiGe S/D stressors.

the used of *e*Π-SiGe S/D. Series resistance is also plotted as shown in the inset of Fig. 4.17. Figure 4.18 compares the I_D-V_D characteristics of the same devices shown in Fig. 4.17. Significant I_D enhancement achieved by the *e*Π-SiGe S/D stressor over a Π-SiGe S/D can be observed. This enhancement is largely

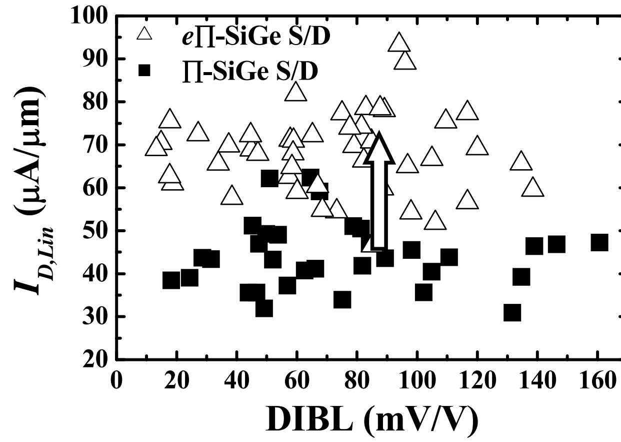


Fig. 4.19. $I_{D,Lin}$ obtained at V_G-V_{th} = -1.2 V and V_D = -0.1 V. 75% enhancement in linear drain current is observed for a given DIBL.

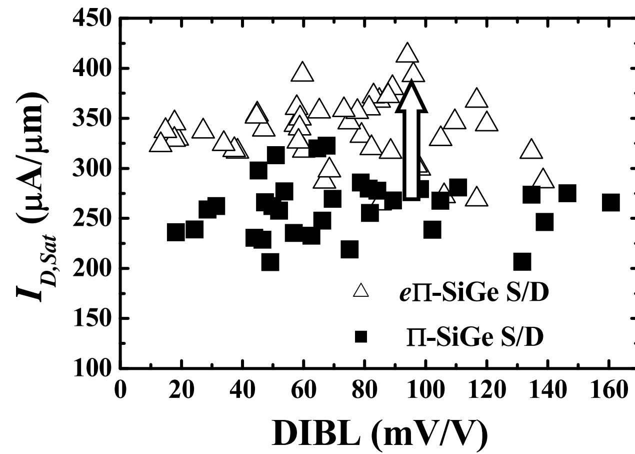


Fig. 4.20. $I_{D,Sat}$ obtained at V_G - V_{th} = V_D = -1.2 V. 33% enhancement in drive current can be observed at a fixed DIBL.

attributed to the increase in hole mobility as suggested by the transconductance G_m gain as shown in Fig. 4.16(b). Figure 4.19 and 4.20 show the enhancement in both $I_{D,Lin}$ and $I_{D,Sat}$ for FinFETs with *e*Π-SiGe S/D over FinFETs with Π-SiGe S/D plotted against DIBL. The enhancement in $I_{D,Lin}$ (~75%) is roughly 2× higher than that of I_{Dsat} or I_{on} (33%) for a given DIBL. The higher enhancement in $I_{D,Lin}$

than $I_{D,Sat}$ can be explained to be due to the higher sensitivity of drive current to the change in mobility at low drain biased [4.16].

4.2.4. Summary

P-channel FinFETs with *e*Π-SiGe S/D stressors were demonstrated for the first time, showing a further I_{on} enhancement of up to 33% over FinFETs that are already strained by Π–shaped SiGe S/D stressors. I_{on} enhancement increases with reduced fin width. *e*Π-SiGe S/D stressors offer the highest compressive strain for hole mobility enhancement among the SiGe S/D stressors, made possible by a recessed buried oxide, prior to selective epi-growth of SiGe. The integration scheme for *e*Π-SiGe S/D is very attractive as no additional process complexity is introduced. *e*Π-SiGe S/D will thus be promising for performance enhancement in aggressively scaled FinFET devices.

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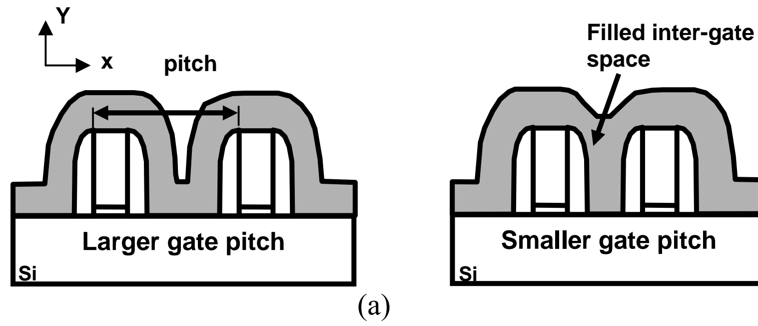
Chapter 5

Diamond-Like Carbon (DLC): A New Liner Stressor with Very High Intrinsic Compressive Stress (> 6 GPa)

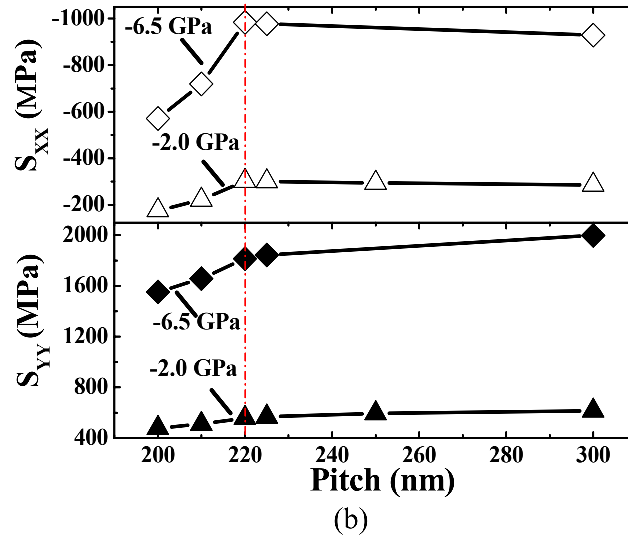
5.1 Integration of DLC on P-Channel SOI Transistors for Strain and Device Performance Enhancement

5.1.1 Background

Strain engineering using SiN liner or contact etch-stop layer (CESL) have been widely adopted [5.1]-[5.5]. Aggressive gate pitch scaling leads to performance degradation due to reduced channel stress [5.3]. As gate pitch decreases, stress in the channel contributed by SiN liner starts to decline when the inter-gate space is filled by SiN as shown by the stress simulation in Fig. 5.1. Taurus process simulation was used in this work and the simulation results show that the stress in the channel starts to decease significantly when the pitch is reduced beyond 220 nm (merging of CESL from both sides). Utilizing a CESL with a higher intrinsic stress can increase the stress impart to the channel as shown in Fig. 5.1(b). In addition, the onset of reduction in channel stress with pitch scaling can be delayed if a thinner CESL with higher stress is used. For p-FETs,



(a)



(b)

Fig. 5.1. (a) Schematics showing the used of highly stressed CESL on 2 transistors placed side by side having different pitch value. For the schematics having a smaller gate pitch, the inter-gate space is completely filled (b) Simulation of stress induced in the channel from SiN (-2.0 GPa and -6.5 GPa) for L_G of 50 nm and spacer width of 35 nm. Thickness of CESL is 50 nm. Stress value is taken at ~4 nm beneath the Si surface at the center of the channel. The channel stress decrease significantly at a pitch value of 220 nm.

however, reported stress magnitudes for compressive SiN rarely exceed 2.5 GPa. Moreover, thick SiN liner requirement to achieve the desired stress amount also adversely affects pitch scalability.

In this chapter, we report the demonstration of a new liner stressor material comprising diamond-like carbon (DLC) with very high intrinsic compressive stress (> 6 GPa) and low permittivity. DLC liner stressor used in this work is less

than 50 nm, which is much thinner than the works reported with SiN. We have also demonstrated the integration of DLC liner in nanoscale SOI p-FETs for strain engineering and performance enhancement.

5.1.2 Properties of Diamond-Like Carbon

Tuning of SiN to give an even higher intrinsic stress can be quite challenging [5.6], alternatively materials with intrinsic stress magnitude greater than SiN may already exist and a search in literature was thus made. Among the reported works found are boron nitride (BN) having an intrinsic stress ranging from 1 up to 20 GPa [5.7] - [5.9] and DLC. DLC are studied here due to its availability and potential of being used as a low κ dielectric material in CMOS technology, with permittivity ranging from 2.7 to 3.8 [5.10]. Such low permittivity can be exploited to reduce parasitic capacitance for higher circuit speeds. In addition, for CESL application, it has been reported that DLC can be etched using either pure O_2 [5.11] or a mixture of Ar and O_2 plasma [5.12]. We employed a filtered cathodic vacuum arc (FCVA) system for the deposition of DLC films with high

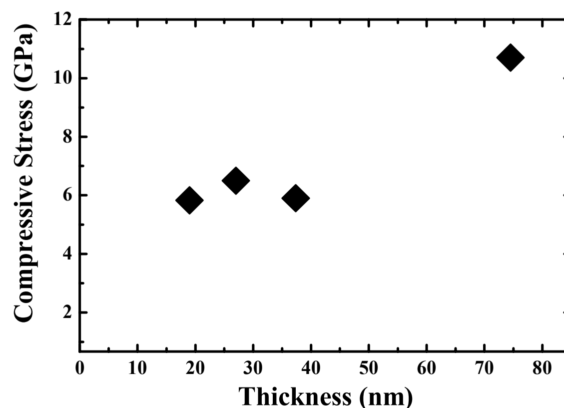


Fig. 5.2. Intrinsic stress of DLC layer, obtained from wafer curvature measurement, showing high compressive stress value > 6 GPa.

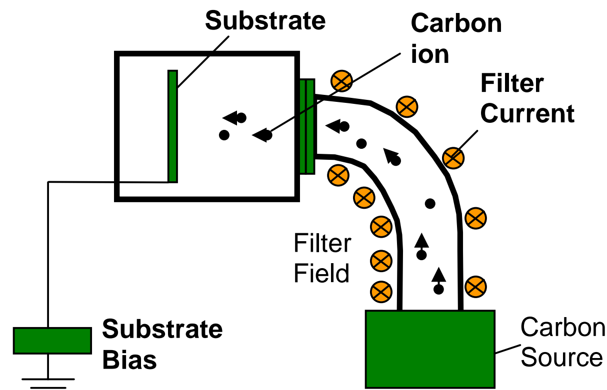


Fig. 5.3. Schematic of a FCVA system showing the deposition of DLC by carbon ions. The carbon ions are guided by a filter field and a voltage bias is applied to the substrate.

intrinsic stress and excellent thickness uniformity. The deposited DLC films exhibit high intrinsic compressive stress typically above 6 GPa as shown in Fig. 5.2 measured using a wafer curvature system. Figure 5.3 show a schematic diagram of the FCVA system. Carbon ions (C^+) are generated by an arc discharge and are guided by the filter field to the substrate. A bias voltage can also be applied to the substrate for process tuning. The arc current, filter current and bias voltage used are 26 A, 9 A and 80 V respectively. Negative bias voltage are used to vary the carbon ion energy.

DLC is a dense form of amorphous carbon with significant sp^3 bonding. The material characteristics of DLC film depend heavily on the ratio of the sp^3 to the sp^2 content. Film having higher sp^3 content will demonstrate more diamond-like characteristics, including mechanical hardness, chemical inertness, and higher resistivity. Therefore, a higher sp^3 content is desirable for the achievement of a high resistivity value. To estimate the sp^3 content in the DLC film, visible Raman (514 nm) spectroscopy was used [5.13]. Fig. 5.4 shows a Raman spectrum

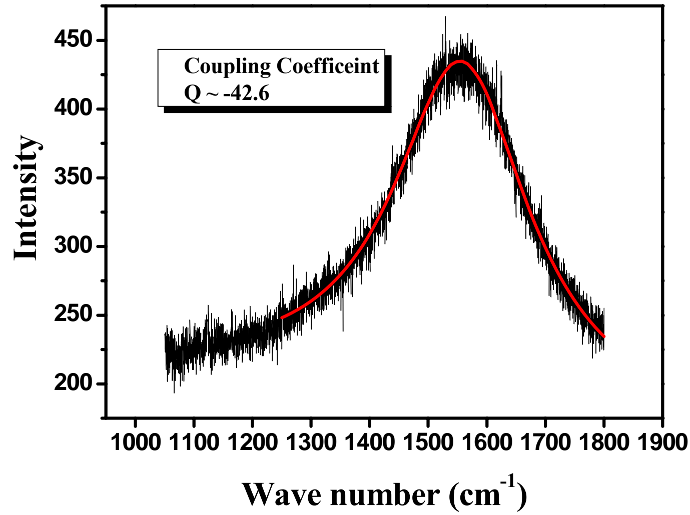


Fig. 5.4. Raman spectroscopy of DLC film having a peak value at ~1580 cm^{-1}. The sp^3 content of the film can be estimated from the "skewness" of the peak and the coupling coefficient Q. A more negative value of Q indicates a higher sp^3 content.

having a peak value at around 1580 cm^{-1} as obtained from the DLC film used in this work. The data was fitted using a Breit–Wigner–Fano (BWF) line shape, as given by

$$I(\omega) = \frac{I_0[1 + 2(\omega - \omega_0)/Q\Gamma]^2}{1 + [2(\omega - \omega_0)/\Gamma]^2} + (a + b\omega), \qquad \text{------ eq. 5.1}$$

where $I(\omega)$ is the Raman scattered intensity as a function of ω, while ω_0, I_0, Γ, are the peak position, peak height, full wave half maximum (FWHM), respectively. Q is the skewness factor and a, b are constants. The coupling coefficient Q which is an indication of the "skewness" of the peak is found to be -42.6. Generally, a large negative Q value indicates high sp^3 content. The sp^3 content of this particular DLC film is estimated to be greater than 80% based on [5.13]. Alternatively, the sp^3 content of the DLC film can also be estimated using X-ray Photoelectron Spectroscopy (XPS) as reported in [5.14]. Figure 5.5 shows

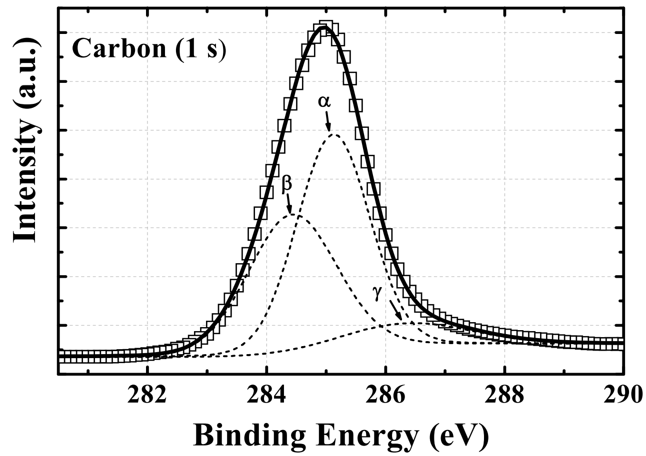


Fig. 5.5. (a) X-ray Photoelectron Spectra of Diamond-Like Carbon (DLC) film showing the Carbon 1 s core level. The spectrum is fitted with curves having peaks corresponding to sp^3-hybridized carbon (α), sp^2-hybridized carbon (β), and C-O (γ) bonds.

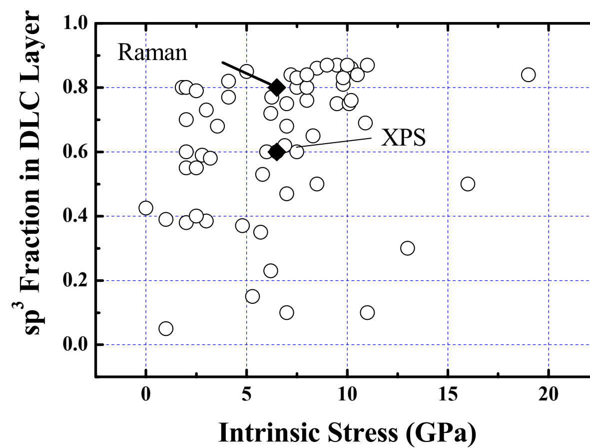


Fig. 5.6. DLC film is characterized by its sp^3 content and intrinsic stress.

a XPS spectrum obtained from our DLC film, showing the carbon 1s core level. The spectrum is deconvoluted into 3 peaks corresponding to sp^3, sp^2 and C-O bonds.

In this technique, the DLC film shows a sp^3 content of ~60%, estimated by taking the ratio of the area under the curve due to sp^3-hybridized C to the total

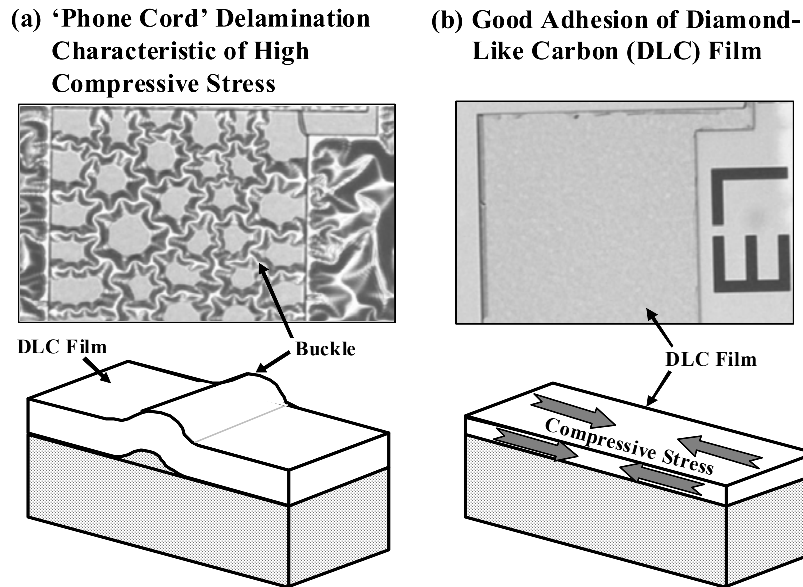


Fig. 5.7. (a) Optical microscopy image of a DLC film on wafer with FinFET devices, in which film delamination and buckling occurs due to the large intrinsic compressive stress. A schematic showing the buckling of film to relieve the high compressive stress is shown below. (b) Optical image of a thinner DLC film (~20 nm) adhering well to the substrate when the DLC thickness is reduced.

area under the C 1s curve. As mentioned earlier, it is desired to achieve high sp^3 content and also a high stress magnitude for large resistivity and better device performance. A graph of sp^3 content against compressive stress is plotted in Fig. 5.6. We compared the properties of our DLC film to that of others reported in the literatures using various form of deposition techniques. It can be seen that, it is be possible to achieve an even higher sp^3 content and compressive stress value by further optimizing the process conditions. In addition, to increase resistivity, hydrogenation of DLC can also be employed [5.15],[5.16].

For a given compressive stress, e.g. ~ 6 GPa, the DLC film formed on transistors, can locally delaminate and buckle, as illustrated in the optical image of Fig. 5.7(a). 'Phone-cord-like' delamination occurred in the DLC film of Fig. 5.7(a). Films under compressive stress are susceptible to buckling delamination

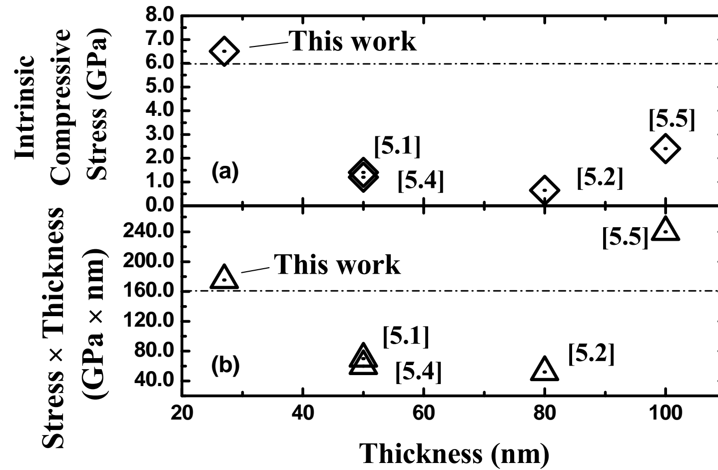


Fig. 5.8. Intrinsic stress of DLC layer is well above reported values for compressive SiN CESL. This work realizes a liner stressor with the highest (a) compressive stress or (b) stress-thickness product for sub-60 nm thick films.

when the elastic energy per unit area stored in the film exceeds the energy per area required to de-coherent the interface. Such buckling delamination is commonly observed in thin films with high compressive stress, films that are too thick, or with inadequate interfacial adhesion [5.17]. By reducing the deposition time and therefore the thickness of the DLC film deposited, good adhesion was achieved. We were able to avoid buckling of the DLC film, as shown in Fig. 5.7(b). Figure 5.8(a) highlights the superiority of DLC films over conventional SiN films in achieving high intrinsic stress. Very high stress-thickness product of above 160 GPa•nm can be achieved with a DLC thicknesses as small as 27 nm.

5.1.3 Device Fabrication

Eight-inch SOI substrates with 35 nm thick Si were used in a p-channel device fabrication process. After threshold voltage adjust implants, gate stacks comprising pre-doped poly-Si/SiO_2 (3 nm) were defined. S/D extension, spacers, and deep S/D were formed. Ni with a thickness of 7 nm was then sputter-

deposited for salicidation. For wafers on which strained P-FETs are to be formed, 10 nm SiO_2 was deposited to improve the adhesion of DLC film to the device and also prevent possible degradation to the silicide due to the bombardment of carbon ions. Photoresist was patterned at the contact regions and DLC was deposited using a FCVA system which is capable of producing films with very high intrinsic compressive stress. The DLC at the contact regions were removed using a resist lift-off process, followed by the removal of SiO_2 using dilute HF. Control devices were also fabricated where the step of depositing DLC was skipped. Electrical characterization was performed by direct probing on the NiSi source, drain, and gate pads. Two DLC thicknesses, 19 nm and 27 nm, with ~6.5 GPa intrinsic stress were used, and hereafter will be referred to as thin-DLC and thick-DLC, respectively.

5.1.4 Results and Discussion

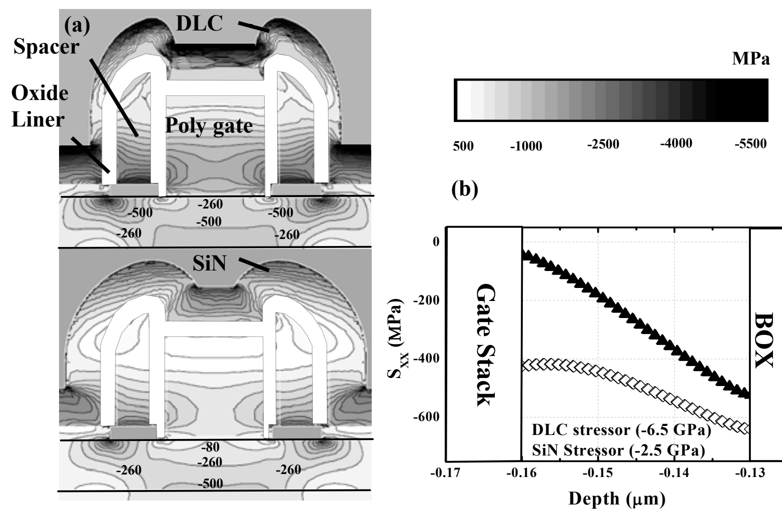


Fig. 5.9. Simulation comparing the stress effects of DLC (-6.5 GPa) and SiN (-2.5 GPa) in p-FETs with 70 nm L_G. Slight differences in DLC and SiN conformality is accounted for. Stress in (a) 2D and (b) 1D (vertical profile at the center of channel) show that the DLC exerts a higher compressive channel stress than SiN.

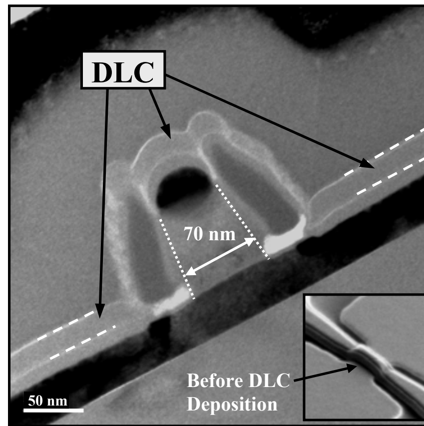
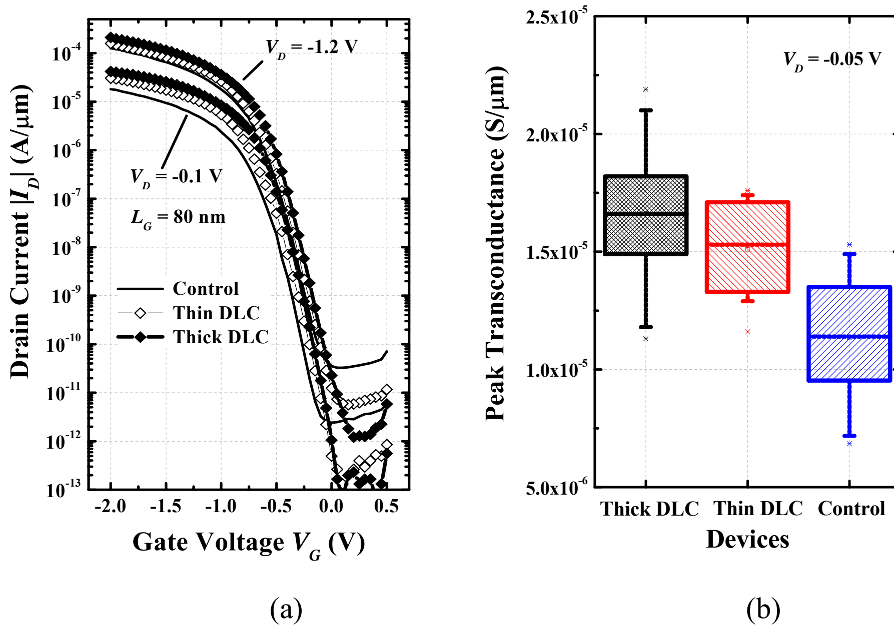


Fig. 5.10 TEM image of a planar strained SOI p-FET with 70 nm gate length. The deposited DLC adheres very well over topological features. A SEM picture of the device prior to DLC deposition is shown in the inset



(a) (b)

Fig. 5.11. (a) I_D-V_G characteristics of planar SOI p-FETs with different DLC layer thicknesses. Similar SS and DIBL were obtained. The $|V_t|$ for the strained p-FETs is slightly lower than that of the control. (b) The p-FET with thick-DLC (27 nm) has a peak transconductance improvement of 47% and 10%, respectively, over control p-FET and strained p-FET with thin-DLC (19 nm).

Simulation results in Fig. 5.9 show that for a given liner thickness, DLC (-6.5 GPa) gives a much higher lateral compressive channel stress S_{XX} than even one of

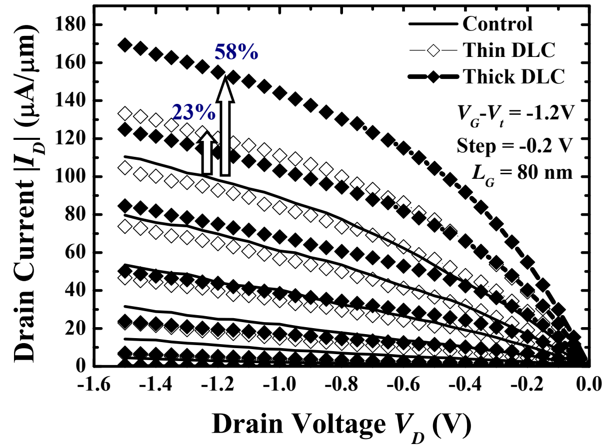


Fig. 5.12. I_D-V_D characteristics of p-channel SOI devices with different DLC layer thicknesses. The p-FET with thicker DLC shows 58% drive current enhancement over a control p-FET without liner stressor.

the most compressively stressed SiN liner (-2.5 GPa). Young Modulus and poisson's ratio of DLC reported in [5.18] was used in the simulation. Fig. 5.10 shows a TEM image of a p-FET with DLC liner. Excellent DLC film coverage and adhesion was achieved, as seen in the TEM view. I_D-V_G characteristics of

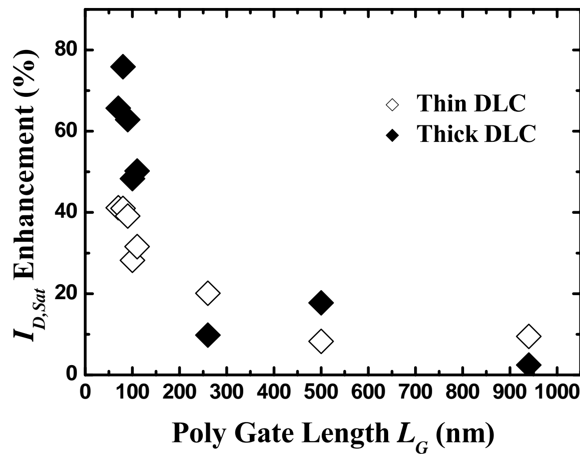


Fig. 5.13. Drive current $I_{D,Sat}$ enhancement increases with decreasing gate length L_G. For L_G less than 200 nm, $I_{D,sat}$ enhancement for p-FETs with thicker DLC increases more rapidly with decreasing L_G.

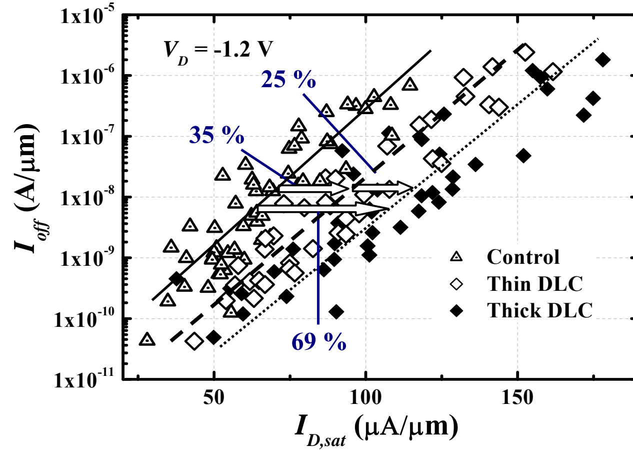


Fig. 5.14. Comparison of I_{off} (V_G = -0.35 V) versus $I_{D,Sat}$ (V_G = -1.55 V) showing $I_{D,Sat}$ enhancement of 35% and 69% for p-FETs with thin and thick DLC, respectively, over the control p-FET at I_{off} = 10 nA/µm.

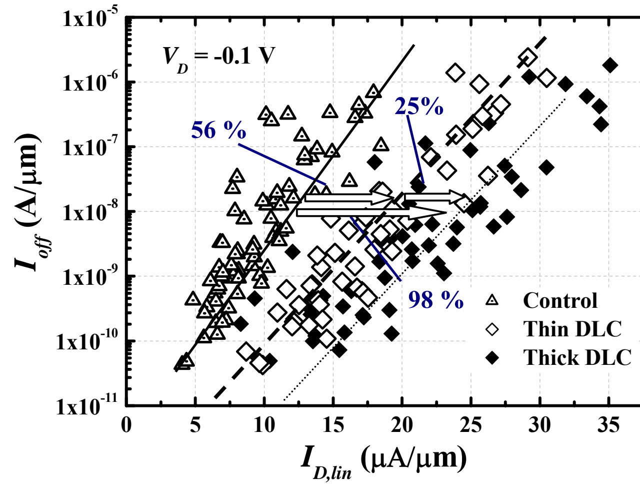


Fig. 5.15. Comparison of I_{off} (V_G = -0.35 V) versus $I_{D,Lin}$ (V_G = -1.55 V) showing $I_{D,Lin}$ enhancement of 56% and 98% for p-FETs with thin and thick DLC, respectively, over the control p-FET at I_{off} = 10 nA/µm.

devices with 80 nm gate length L_G show comparable control of short-channel effects (Fig. 5.11(a)). Devices with thin- and thick- DLC show 33% and 47% improvement in peak G_m over the control device as shown in Fig. 5.11(b). This is due to hole mobility enhancement resulting from the compressive channel stress. A thicker DLC liner give a higher performance enhancement. Fig. 5.12 shows the

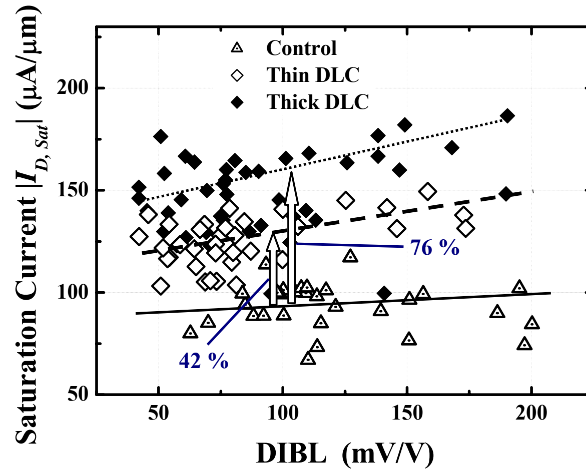


Fig. 5.16. $I_{D,Sat}$ taken at V_G-V_t = -1.2 V and V_D = -1.2 V. At a fixed DIBL of 0.1 V/V, 42 % and 76 % $I_{D,Sat}$ enhancement can be observed for p-FETs with thin and thick DLC, respectively.

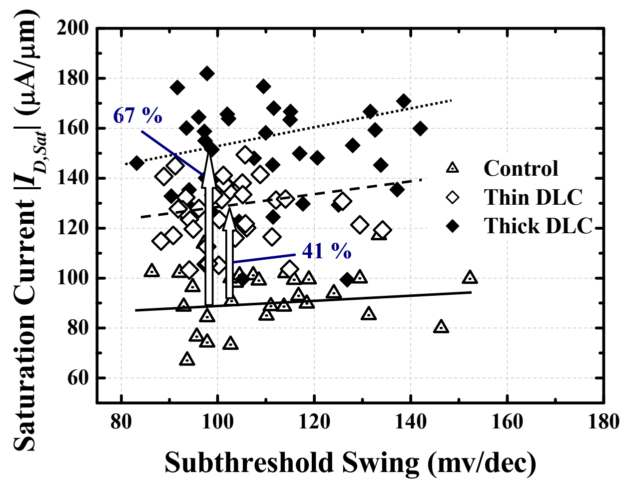


Fig. 5.17. At a fixed subthreshold swing of 100 mV/decade, significant $I_{D,Sat}$ (V_G-V_t = -1.2 V and V_D = -1.2 V) enhancement of 67% is observed for p-FETs with thick (27 nm) DLC liner stressor.

I_D-V_D characteristics of p-FETs with comparable DIBL and subthreshold swing (SS). $I_{D,Sat}$ enhancement at a gate overdrive of -1.2 V is 23% and 58% for p-FETs with thin- and thick- DLC, respectively. Generally, $I_{D,Sat}$ enhancement increases with decreasing L_G (Fig. 5.13) due to increased channel strain levels in smaller

devices. Figure 5.14 compares the I_{off}-$I_{D,sat}$ characteristics, and L_G ranging from 70 nm to 100 nm were measured. At a given I_{off} of 10 nA/μm, $I_{D,Sat}$ enhancement of 35% and 69% over the control device were observed for p-FETs with thin- and thick-DLC liner, respectively. $I_{D,Sat}$ values will be higher if state-of-the-art baseline processes are used. For $I_{D,lin}$, a higher enhancement of 56% and 98%, respectively, was obtained for the p-FETs with thin- and thick- DLC liner as shown in Fig. 5.15. Device performance is also compared at the same DIBL (Fig. 5.16) and SS (Fig. 5.17). $I_{D,Sat}$ enhancement at a fixed DIBL of 0.1 V/V or SS of 100 mV/decade is 76% and 67%, respectively, for p-FETs with a thick DLC.

5.1.5 Summary

A new DLC liner with intrinsic compressive stress above 6 GPa was successfully developed and integrated in nanoscale SOI p-FETs for strain engineering and performance enhancement. Significant $I_{D,Sat}$ enhancement was observed even for DLC films below 30 nm thickness. Replacement of compressive SiN liner with DLC holds promise for further performance improvement of p-FETs beyond the 22 nm technology node. The new DLC liner technology potentially offers a superior density-performance tradeoff, and should be compatible with a tensile-stress SiN in a dual-stress liner approach.

5.2 Integration of DLC on P-Channel Multiple-Gate Transistors for Advanced Device Scaling

5.2.1. Background

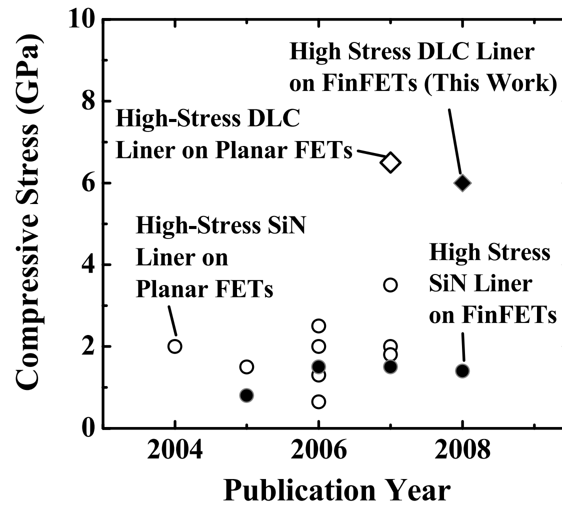


Fig. 5.18. Comparison of reported intrinsic compressive stress levels in high-stress liners employed in transistor demonstrations. Open symbols represent integration of such high-stress liners on planar transistors, while closed symbols represent integration of high-stress liners on multiple-gate transistors or FinFETs. Silicon nitride high-stress liners are plotted in circles and diamond-like carbon (DLC) liners are plotted in diamonds. Intrinsic compressive stress of DLC is much higher than that of SiN.

SiN liner stressor has also been demonstrated to improve the saturation drain current I_{Dsat} in multiple-gate device structures [5.19]-[5.22]. Nevertheless, the intrinsic stress of SiN is also not high. P-channel FinFETs integrated with SiN liner employed intrinsic compressive stress values in the range of ~0.8 to 2 GPa as shown in Fig. 5.18. A higher magnitude of stress has to be induced in the transistor channel region to give further boost in device performance.

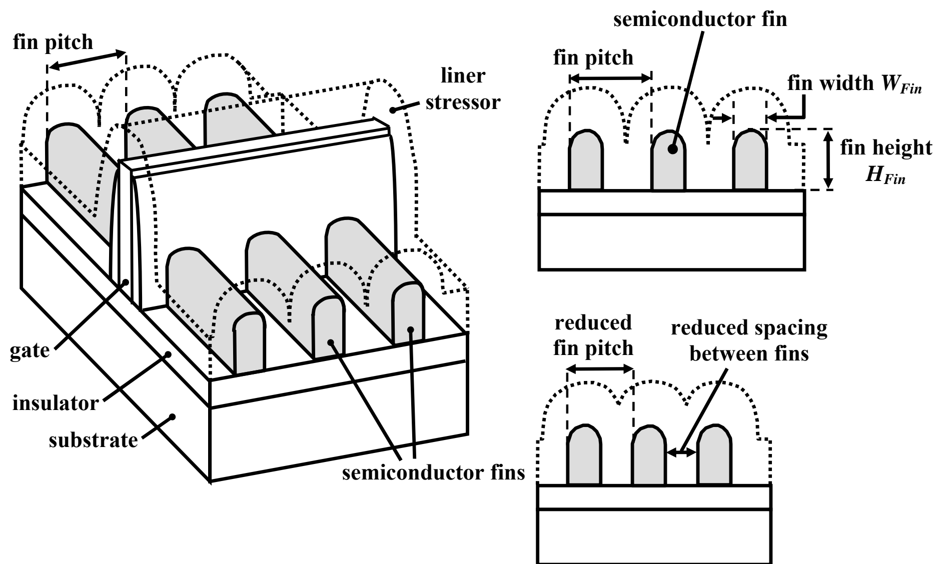
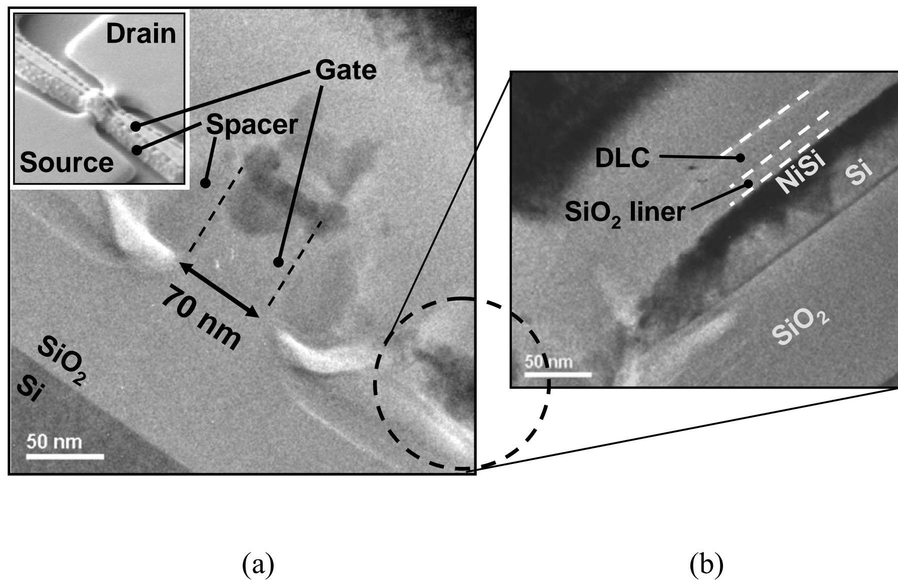


Fig 5.19. Schematic of a FinFET device with a liner stressor and multiple semiconductor fins with a fin pitch p_{fin}. Cross-sections through the fin and liner stressor on the right illustrate that fin pitch reduction leads to reduced spacing between fins, and the volume of liner stressor material found between fins will be reduced, leading to reduced stress effects.

For FinFETs, interactions between the liner stressor and the fin sidewalls is an important contributor to the channel stress as well. To increase the compactness of circuits employing FinFETs with multiple fins, the fin pitch has to be reduced. Fin pitch reduction, however, will reduce the amount of liner stressor material found between the fins, as shown in Fig. 5.19, and could decrease the stress effects. This is similar to the decline in channel stress due to a reduced gate pitch [5.3]. Similarly, increasing the intrinsic stress rather than the thickness of the liner stressor is expected to be beneficial. The highly compressive stressed DLC will therefore also be applicable on multiple-gate transistor.

5.2.2 Device Fabrication



(a) (b)

Fig. 5.20. (a) Transmission Electron Microscopy (TEM) image taken along the S/D direction of a multiple-gate transistor showing a gate length of 70 nm. A Scanning Electron Microscopy (SEM) image of the device is also shown as an inset. (b) A TEM image taken in the nickel-silicided source/drain region clearly showing the DLC film formed on a SiO_2 liner.

The major process steps are similar to section 5.1.3 except that FinFET devices are fabricated with H_{Fin} and W_{Fin} being 35 and 45 nm respectively. To reduce series resistance, slightly elevated Si S/D regions were formed. The thickness of Si that was selectively grown in the S/D is ~15 nm. A thin NiSi was used (~5 nm Ni), and the fin was not completely silicided. Similarly, a lift-off process was used for contact definition by patterning photoresist on the contact regions, followed by deposition of ~20 nm of DLC as measured from the TEM shown in Fig. 5.20. As the deposition rate of DLC was found to have decreased significantly, the deposition conditions were changed to using filtered current, arc current and biased conditions of 11 A, 50 A and 95 V respectively. The sp^3 content and stress of the DLC film were also characterized and found to be ~60%

(estimated using XPS) and 6 GPa (measured using wafer curvature system). Electrical characterization was performed by direct probing on the NiSi source, drain, and gate contact regions.

5.2.3 Results and Discussion

The electrical characteristics of FinFETs with and without DLC liner stressor are compared next. Fig. 5.21(a) shows the I_D-V_G plot of a pair of devices having similar V_{th}. Both devices have a gate length of 70 nm and comparable

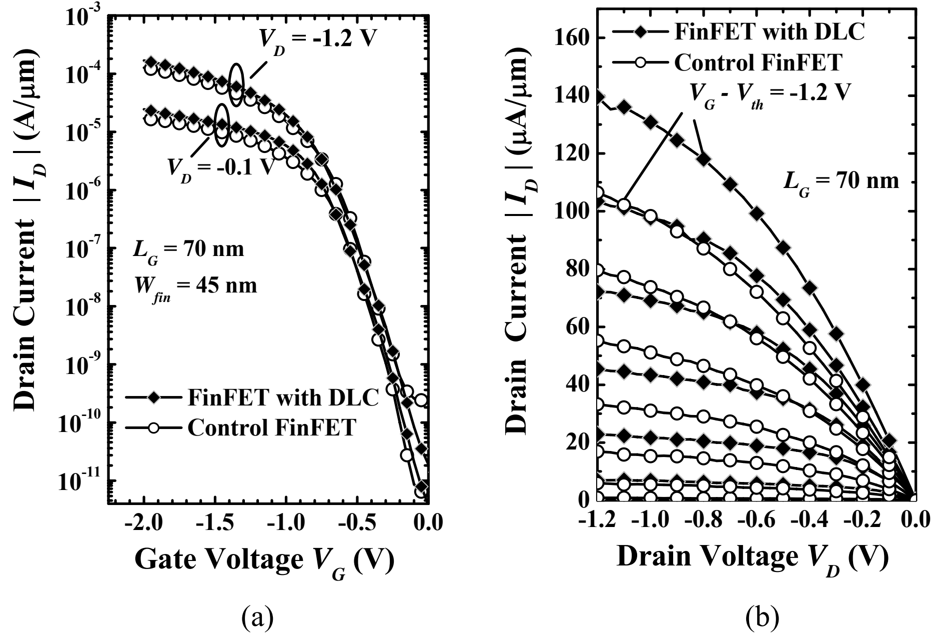


Fig. 5.21. Comparison of (a) I_D-V_G and (b) I_D-V_D characteristics for FinFETs with and without DLC liner, showing similar subthreshold swing and drain-induced barrier lowering. I_D-V_D curves with gate overdrive $V_G - V_{th}$ from 0 to -1.2 V in steps of -0.2 V are shown. A 31% enhancement in saturation drain current is observed for the FinFET with DLC liner stressor over the control FinFET.

short-channel effects. The subthreshold swing (SS) and DIBL is around 120 mV/decade and 0.05 V/V, respectively. The I_D-V_D characteristics for the matched pair of FinFETs is shown in Fig. 5.21(b). The drain current is normalized based

on a tri-gate structure with a device width given by ($2H_{Fin}$ + W_{Fin}). At a gate overdrive ($V_G - V_{th}$) of -1.2 V and a drain voltage V_D of -1.2 V, the strained FinFET having a DLC liner shows a 31% enhancement of saturation drain current I_{Dsat} over the control device.

Since the process flow for the control FinFET and the strained FinFET are identical except for the DLC deposition step, the enhancement in I_{Dsat} is attributed to the presence of the highly compressive-stressed DLC liner. Compressive strain is induced in the Si channel which leads to hole mobility and drive current enhancement. Fig. 5.22 compares the transconductance of the devices in Fig. 5.21. A 43% higher peak transconductance is observed for the strained FinFET over the control FinFET, indicating hole mobility enhancement. This is consistent with the enhancement observed in the drain current shown in the I_D-V_D plot.

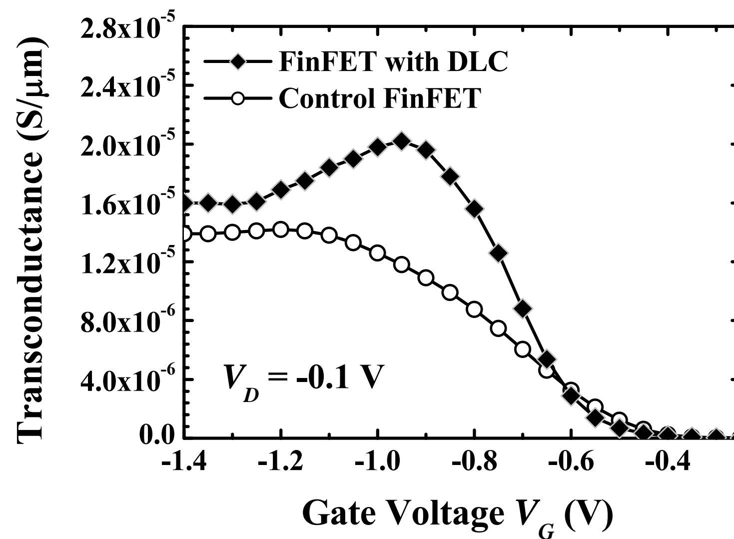


Fig. 5.22. Transconductance as a function of gate voltage, showing 42% improvement in peak transconductance for the strained FinFET with DLC liner over the control FinFET.

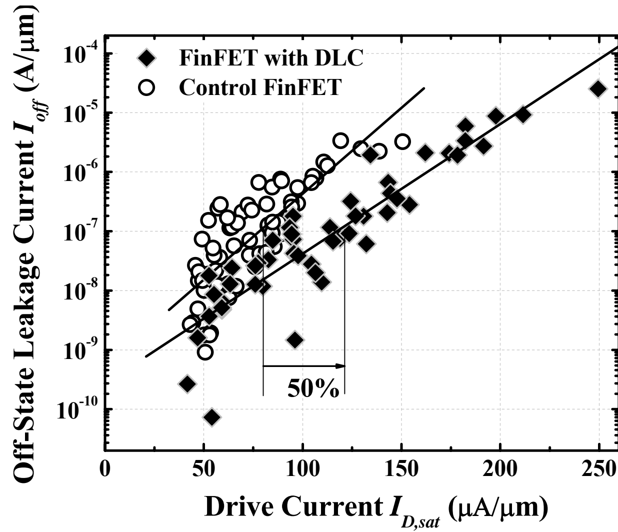


Fig. 5.23. Plot of off-state leakage current I_{off} (V_G = -0.5 V) and saturation drain current I_{Dsat} (V_G = -1.7 V) for strained FinFETs and control FinFETs. The V_D was fixed at -1.2 V. For each device split, about 50 FinFETs or data points were measured, to which a best-fit line is drawn. Strained FinFETs show ~50% enhancement in I_{Dsat} at an I_{off} of 100 nA/μm.

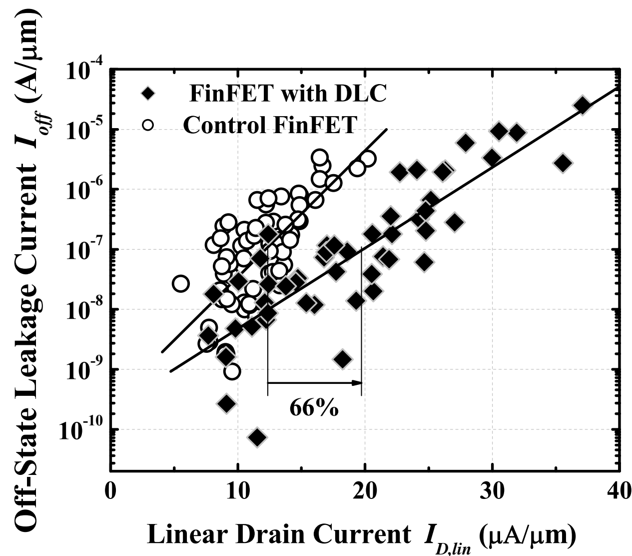


Fig. 5.24. Comparison of I_{off} (V_G = -0.5 V) versus I_{Dlin} (V_G = -1.7 V). The V_D was fixed at -0.1 V. FinFETs with DLC liner have enhanced I_{Dlin} over control FinFETs.

A large number of devices were characterized to obtain the off-state leakage current I_{off} versus the saturation drain current I_{Dsat} plot, as shown in Fig. 5.23. Gate lengths of the devices characterized range from 50 nm to 80 nm. At an I_{off} of 100 nA/μm, 50% enhancement in I_{Dsat} was observed for the strained FinFETs. The drive current performance of the devices can be further improved with use of a thinner gate dielectric, and further optimization of the S/D doping and activation conditions.

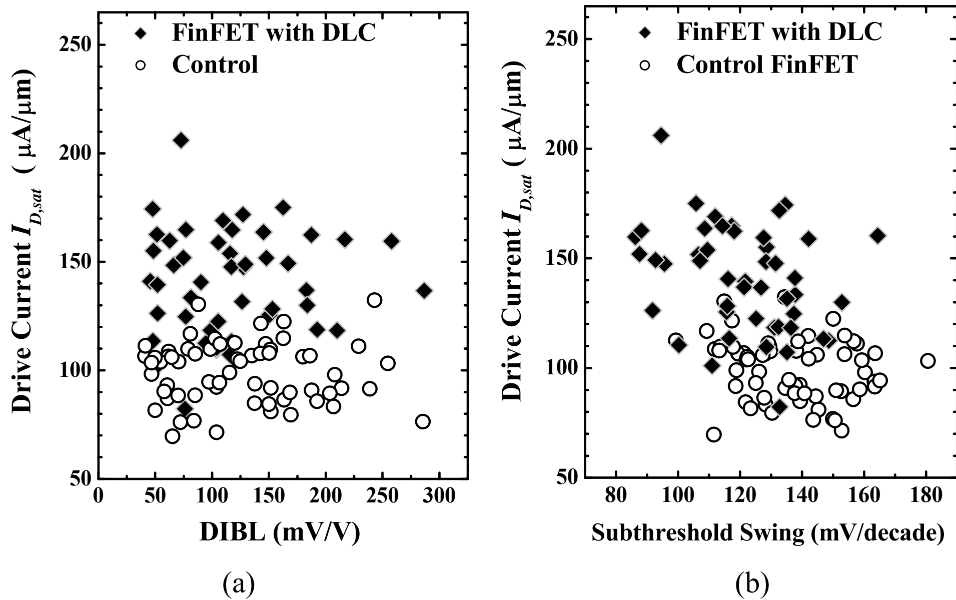


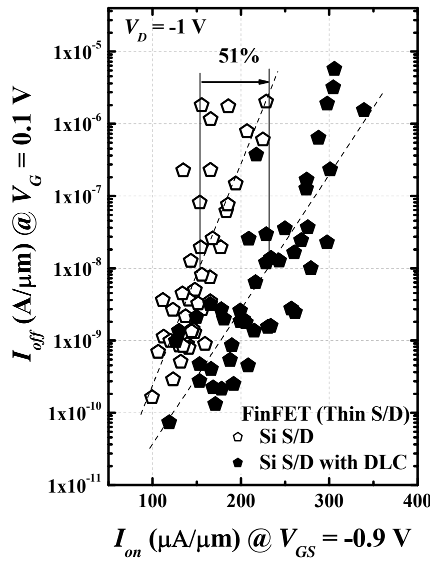
Fig. 5.25. (a) DLC liner stressor significantly enhances the drive current I_{Dsat} of FinFET at various values of drain-induced barrier lowering (DIBL). Devices with gate lengths ranging from 50 nm to 80 nm were characterized. The I_{Dsat} was measured at gate over-drive ($V_G - V_{th}$) = -1.2 V and V_D = -1.2 V. At a fixed DIBL of 0.1 V/V, stress from DLC liner contributed to a 42% I_{Dsat} enhancement. (b) At a fixed subthreshold swing of 120 mV/decade, DLC liner stressor contributes to a significant I_{Dsat} enhancement of 39%.

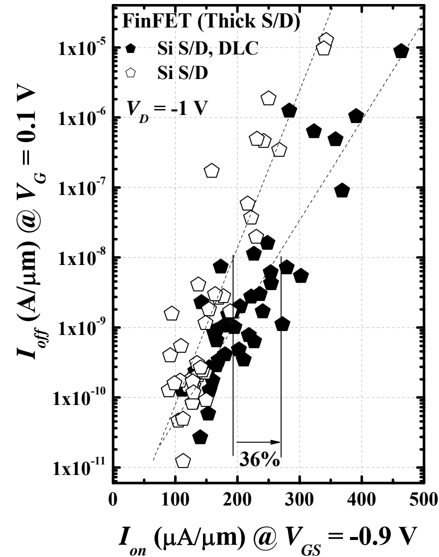
In general, the coupling of stress from the DLC film to the channel is also influenced by the source/drain topology. A higher mobility and drive current enhancement can be achieved for a FinFET structure with reduced S/D elevation. I_{off}-I_{Dlin} plot in Fig. 5.24 shows that the DLC liner stressor increased I_{Dlin} by 66%

at an I_{off} of 100 nA/µm. We also plot the drive current performance as a function of indicators of short-channel effects such as drain-induced barrier lowering (DIBL) and subthreshold swing in Fig. 5.25(a) and (b), respectively. Data points in Fig. 5.25(a) and (b) are obtained from FinFETs with L_G ranging from 50 to 80 nm. At a fixed DIBL of 0.1 V/V, the I_{Dsat} enhancement is 42%, and at a fixed subthreshold swing of 120 mV/decade, the I_{Dsat} enhancement is 39%. Thus, for a given controllability of short-channel effects, the DLC liner stressor provides significant performance enhancement for FinFETs.

5.2.3.1 Impact of DLC Stressed Liner on FinFET Devices with Si S/D Raised with Different Thicknesses

In this section, the integration of DLC with FinFET having a thicker raised S/D studied. A new device run is done, with two different Si thicknesses (thin and thick) grow on the FinFET devices. For the split with a thin and thick raised S/D, 22 nm and 37 nm Si was grown respectively. In addition the S/D extension implant dose was also increased and a new lift-off mask was used which allow the DLC to cover a larger portion of the FinFET device. The intrinsic compressive of DLC used is around 5 GPa having a thickness of 27 nm. Similarly directing probing of the NiSi is used to characterize the transistor. Figure 5.26(a) show the I_{on}-I_{off} plot comparing the effect of having DLC stress liner on FinFET with a thin raised Si S/D to device that is without the DLC liner. Similar to Fig. 5.23, significant enhancement can be seen here. For FinFET devices, the thickness of





(a) (b)

Fig. 5.26. I_{off}-I_{on} plot showing I_{on} enhancement of 51% and 36% for p-channel FinFET integrated with DLC liner with (a) thin and (b) thick Si S/D, respectively.

the raised S/D can affect the device performance [5.23]. Due to the small fin W_{fin}, width dimension, the series resistance can be quite huge and selective epi-growth at the S/D regions will help to alleviate this issue. FinFET devices with a thicker raised S/D integrated with the DLC stressed liner is shown in Fig 5.26(b). The enhancement in I_{on} by the high stressed DLC liner observed is about 36%, which is smaller as compared to the case for FinFET devices with a thin raised S/D. The thicker raised S/D for the FinFET devices placed the DLC film further away from the channel and therefore decreases the strain transfer. Optimization of device performance based on series resistance and strain transfer is therefore required.

5.2.4. Summary

P-channel multiple-gate transistor with DLC liner stressor was demonstrated. At a fixed I_{off} of 100 nA/μm, FinFETs with DLC liner stressor show a 50% I_{Dsat} enhancement over control FinFETs without DLC liner stressor. The intrinsic compressive stress in the DLC film is effectively coupled to the FinFET channel, leading to increase in hole mobility and drive current. Due to the large intrinsic stress in DLC, a relatively small thickness of ~20 nm was sufficient to provide significant performance enhancement. As a thicker raised S/D reduces the strain transfer from the DLC to the channel, device optimization is therefore needed give the best performance.

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Chapter 6

Diamond-like Carbon Liner: Integration with SiGe Source/Drain for Multiple-Stressors Effect

6.1 Background

In chapter 5, we have introduced a new CESL material, Diamond-Like Carbon (DLC), having a much higher compressive stress than SiN, and showed its benefits on p-channel SOI planar and FinFET devices. However, it is essential that the stress induced in the channel to be further enhanced for additional boost in performance which can be achieved by combining multiple stressors. It has been shown that, highly stressed SiN can be used together with stress memorization techniques [6.1], $Si_{1-x}Ge_x$ [6.2],[6.3] and $Si_{1-x}C_x$ [6.4] source/drain (S/D). As such, device performance improved significantly due to the enhanced strain effects. The stress effects of DLC liner can therefore be integrated with other stressors such as SiGe S/D, but this has never been explored before. In this chapter, we will discuss the effects of DLC liner on p-channel bulk transistors having an embedded SiGe S/D stressor. In addition, since the strain effect from SiN CESL stressor can be enhanced with a recessed S/D [6.5] profile, the effects of using a recessed SiGe S/D on the planar FET are also investigated with comparison made to a device with an un-recessed SiGe S/D profile.

6.2 Effects of Deposition Conditions on the Intrinsic Stress of DLC

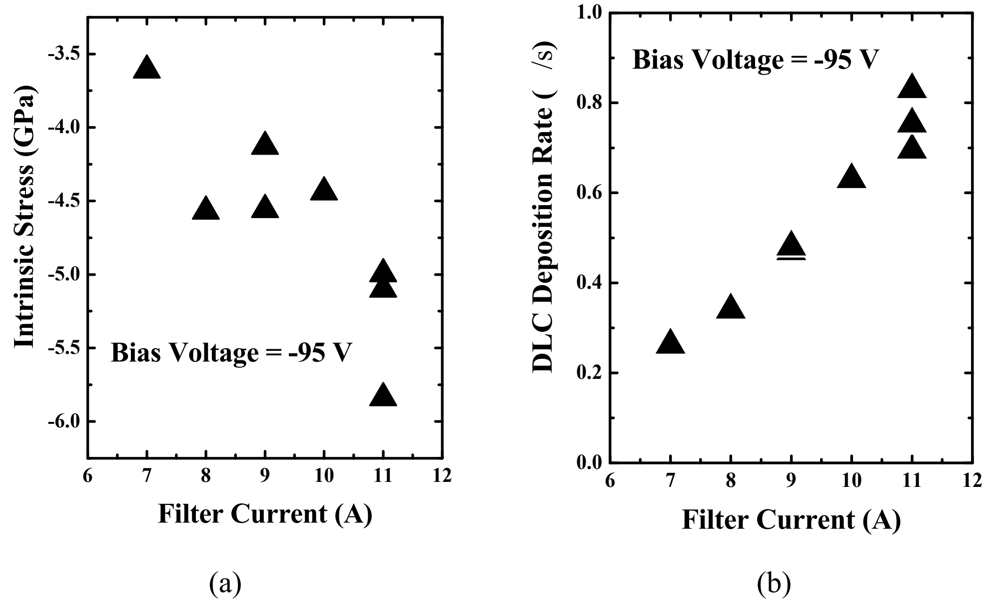


Fig. 6.1. Effect of filter current on the (a) intrinsic stress and (b) deposition rate of DLC. Higher intrinsic compressive stress and deposition rate are obtained with the used of a larger filter current.

The deposition of DLC is done using the FCVA system describes in chapter 5. The effect of filter current on the intrinsic stress of DLC is first studied. As shown in Fig. 6.1(a), the intrinsic stress level of the DLC film increases from around -3.6 GPa to more than -5 GPa when the filter current is changed from 7 A to 11 A. It is also observed that the deposition rate of DLC increases at the same time with increasing filter current, as shown in Fig. 6.1(b). The change in deposition rate is quite significantly (~ 3 times) for this range of filter current used.

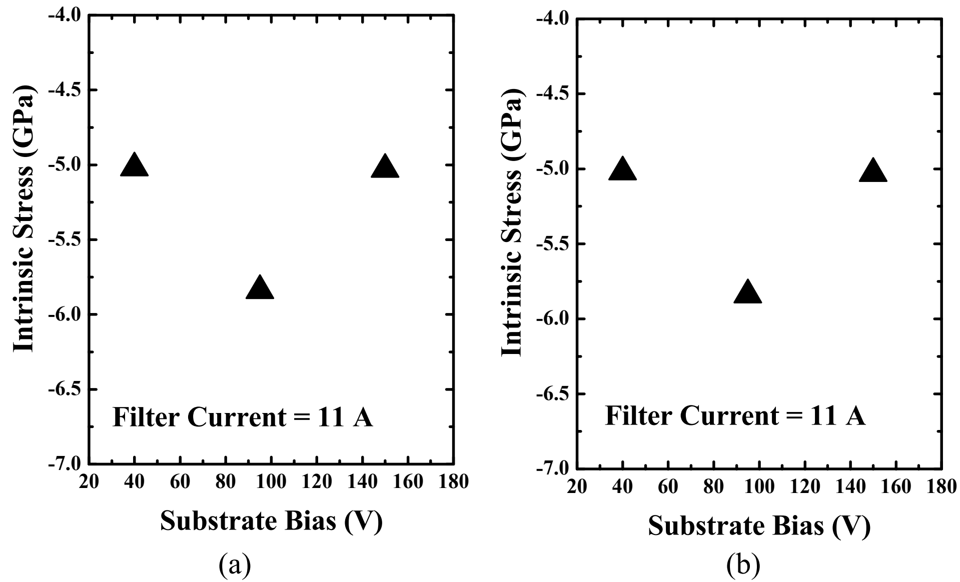


Fig. 6.2. Effect of substrate bias on the (a) intrinsic stress and (b) deposition rate of DLC.

The increased in intrinsic stress obtained at a higher filter current may be attributed to an increase in the number of C^+ ions deposited per unit time. The effect of substrate bias is also studied and a peak in intrinsic stress is seen at a negative bias voltage of 95 V (Fig. 6.2(a)). It has been reported that the intrinsic stress of DLC increases with ion energy and it peaks at around 100 eV. When the ion energy is further increased, the stress starts to decrease gradually [6.6]. This is attributed to the increase in penetration probability of the carbon ions when the ions energy exceed a certain threshold value needed to penetrate the surface layer and following which any extra energy is evolved as heat. Local heating as such may relax the stress and density of the film. However, this large dependence of intrinsic stress on ion energy is not seen here. As we are using bias voltage to control the ion energy, the range of bias voltage used here may not be sufficient enough to cover up to 100 eV. It is also observed that the deposition rate of DLC

does not seen to vary as much with respect to the substrate bias (Fig. 6.2(b)) when compared to varying filter current.

6.3 Device Fabrication

Bulk planar p-field effect transistor (FET) devices were fabricated in this work. After threshold voltage V_{th} adjust implants, gate stack comprising pre-doped poly-Si/SiO_2 (3 nm) was formed followed by S/D extension and SiN spacer formation. The S/D extension implantation dose was also increased in this work to give better device performance. S/D recessed etch (56-66 nm) was done on some of the bulk devices, followed by selective SiGe epitaxy (~72 nm) in the S/D regions. The targeted Ge concentration is ~25 %. For the device split with recessed SiGe S/D (R-SiGe S/D), thinner SiGe was grown (52 nm). Figure 6.3 shows the device splits for the planar p-channel transistor and the actual device structure is shown by the SEM images in Fig. 6.4.

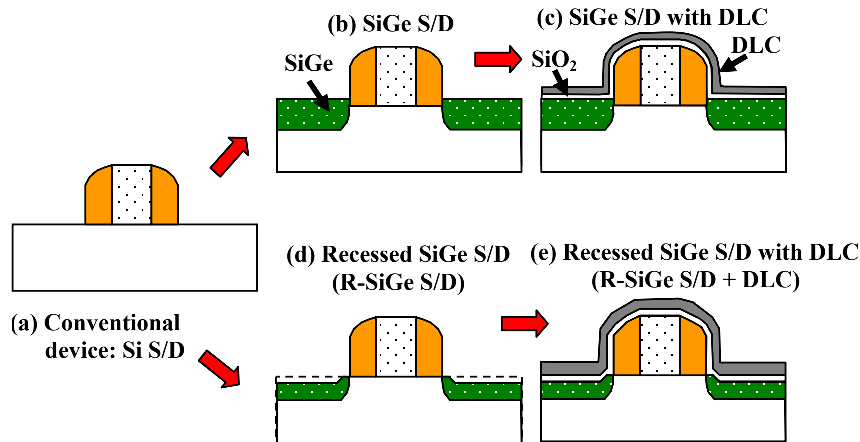


Fig. 6.3. Schematics showing the various planar structures fabricated and compared in this chapter. The respective transistors are (a) conventional device with Si S/D, (b) device with SiGe S/D, (c) device with SiGe S/D and DLC, (d) device with intentionally recessed SiGe S/D (R-SiGe S/D), and (e) device with R-SiGe S/D and DLC.

After S/D formation, Ni salicidation was performed. A very thin Ni ~5 nm was used together with a 2 steps salicidation process to reduce the consumption of the raised SiGe. A 10 nm SiO_2 was then deposited prior to DLC deposition and patterning. The sp^3 content and the intrinsic stress of DLC obtained in this run is around ~46% and 5 GPa respectively, measured using XPS and wafer curvature measurement. Devices were directly probed on the NiSi or NiSiGe S/D regions and the silicided gate after the DLC lift-off step. Fig. 6.5 shows a TEM image of the recessed SiGe S/D planar device with the DLC liner, having a gate length L_G of ~90 nm and a DLC thickness of ~27 nm. The recessed in the S/D can be clearly seen which is around 20 nm.

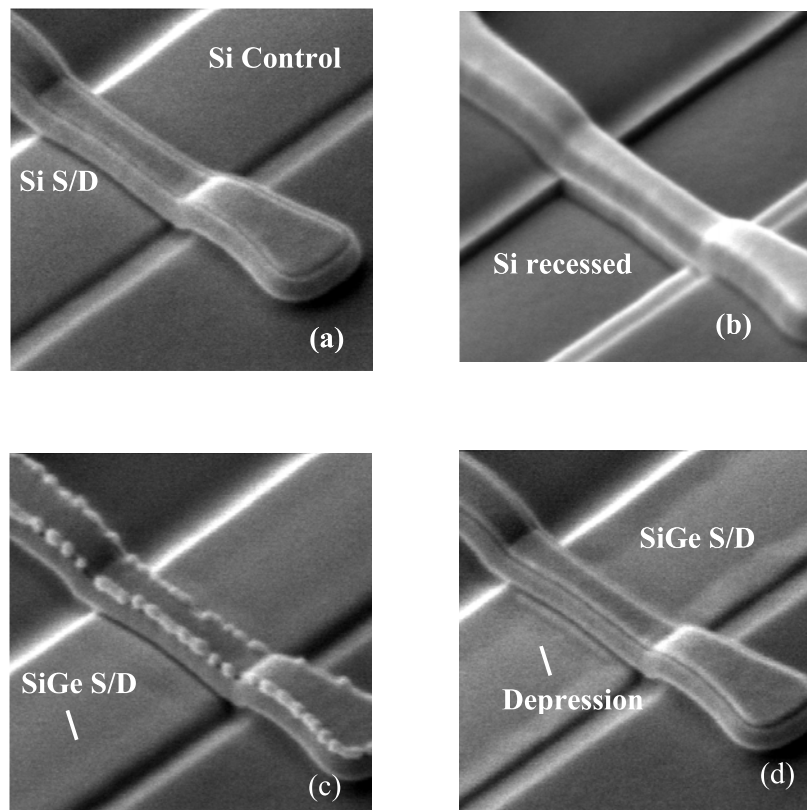


Fig. 6.4. SEM images of the fabricated device after gate stack formation showing (a) Control device with Si S/D. (b) A device after S/D recessed etch. (c) A device with a regrown SiGe S/D. (d) A device with an intentionally recessed SiGe S/D. A depression in the S/D regions can be observed.

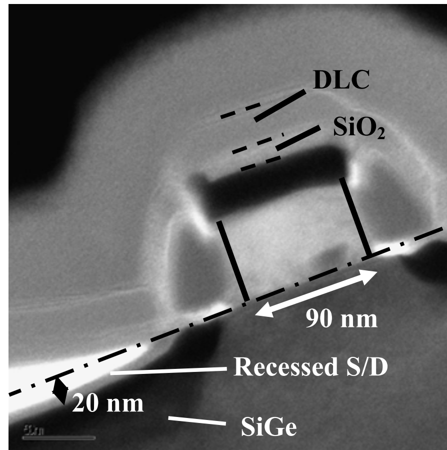


Fig. 6.5. TEM image of a transistor with recessed SiGe S/D and DLC liner. Gate length is 90 nm.

6.4 Results and Discussion

6.4.1 Integration of DLC with SiGe Source/Drain Stressors in Planar Transistors

As the process conditions for SiGe S/D have not been optimized yet, the measured junction leakage is significantly larger than the control device having a Si S/D junction. In addition, as directly probing is done here, the large S/D pad area enhances the magnitude of this leakage current. Increase in junction leakage with increase of Ge concentration in the SiGe S/D regions had been reported in literatures [6.7],[6.8]. The increase in extended defects penetrating into the depletion region is one of the proposed reasons [6.7]. To alleviate this problem, highly doped drain (HDD) implant prior to epi-deposition and in-situ B doped SiGe layers can be adopted. Since the main focus of the this work is to investigate the strain effects of DLC stressed liner with SiGe S/D stressor, the source current

I_S is used as shown in Fig 6.6. I_S is the current flowing from source to drain and unlike I_D, the junction leakage is not included.

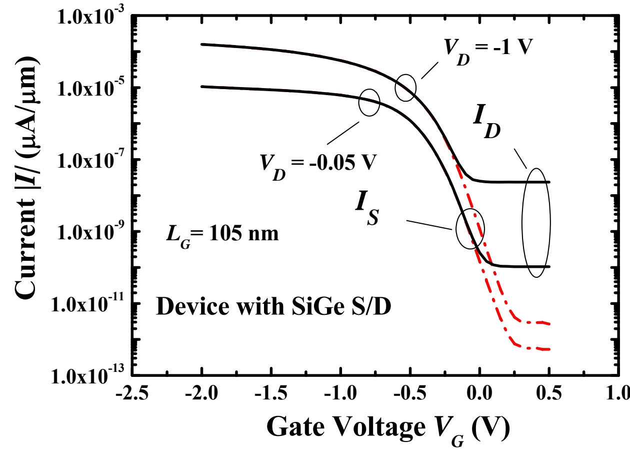


Fig. 6.6. A graph of drive current against gate voltage is plotted for a p-channel device having SiGe S/D. The source current *(I_S)* and drain current *(I_D)* are shown in the plot. Difference observed between these current is attributed to the high leakage of SiGe S/D junctions.

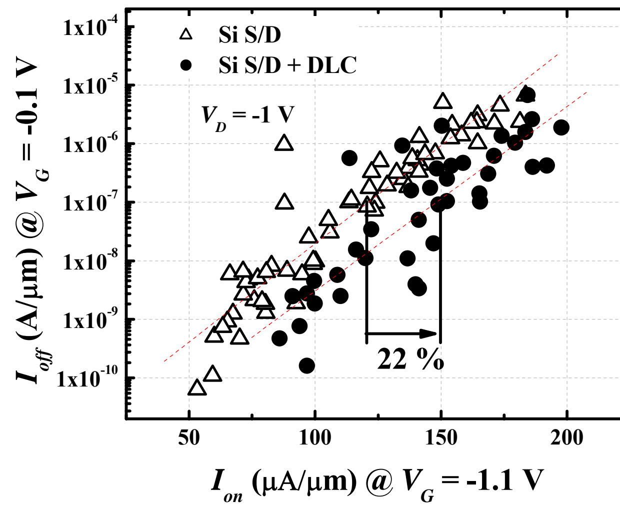


Fig. 6.7. I_{off} versus I_{on} for two groups of p-FETs with Si S/D. P-FETs with DLC liner have 22% higher I_{on} than those without DLC liner.

First, we will investigate the performance of DLC stressed liner on the performance of conventional p-channel device with Si S/D. Figure 6.7 compares the I_{off}-I_{on} characteristics of the conventional Si S/D devices with and without DLC, showing a 22% enhancement in I_{on} for devices with DLC liner at an I_{off} of 1×10^{-7} A/µm. L_G of the devices ranged from 85 nm to 125 nm, and this is same for other I_{on}-I_{off} plots shown in this chapter. Compared to the much larger enhancement seen in the previous chapter for the planar SOI devices, the stress induced in the SOI device is larger than the device demonstrated in this work. Possible reasons attributed can be due to the smaller L_G in the former case and also the used of SOI wafers. It has been shown by simulation that the stiffness of the material beneath the channel can affect the strain transfer and therefore compliant effect of the buried oxide (BOX) in SOI improves the efficiency of induced channel stress [6.9],[6.10].

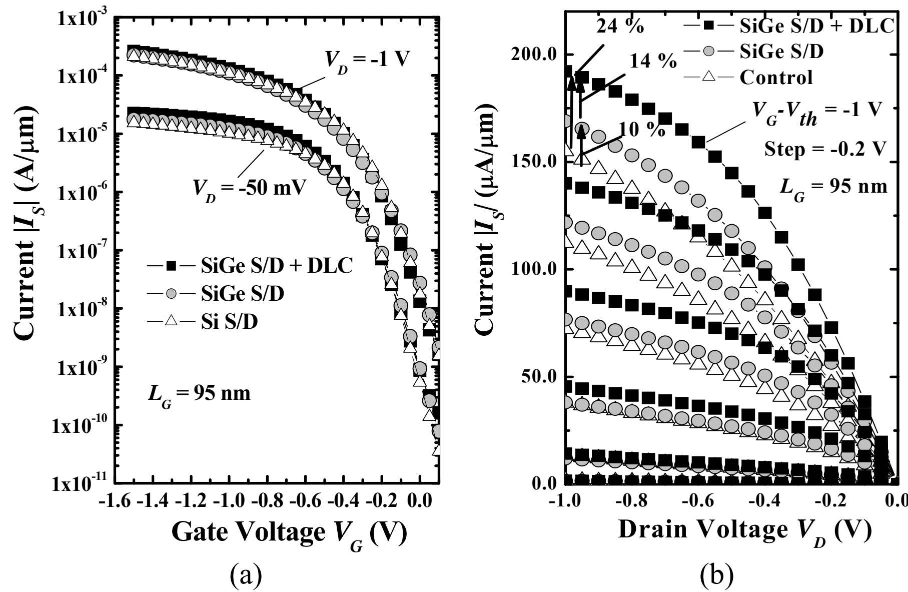


Fig. 6.8. (a) I_S-V_G characteristics of various planar devices showing similar subthreshold swing (SS) and DIBL. (b) Comparison of I_S-V_D characteristics of the devices, where P-FET with SiGe S/D only and p-FET with SiGe S/D and DLC show 10% and 25% higher current, respectively, than over the control (Si S/D).

Figure 6.8(a) and (b) compare the I_S-V_G and I_S-V_D characteristics for planar p-FETs with Si S/D or SiGe S/D. Short-channel effects such as drain-induced barrier lowering DIBL and subthreshold swing are matched. Compared to the control p-FET with Si S/D, p-FET with SiGe S/D shows 10 % current enhancement while p-FET with SiGe S/D and DLC liner show a much larger current enhancement of 24% (Fig. 6.8(b)). Figure 6.9 compares the I_{off}-I_{on} characteristics of these device splits, giving similar enhancement levels as observed in Fig. 6.8. Fig. 6.10 plots the transconductance G_m for these 3 types of devices. The device with both SiGe S/D and DLC liner shows the highest peak G_m value of 83% over the control, indicating a significantly increased of hole mobility due to the high stress from DLC and SiGe S/D. Similarly, as shown in Fig. 6.11, I_{lin} improvement of 17 % and 42 % was observed for p- FETs with SiGe S/D and with SiGe S/D and DLC, respectively. At a fixed DIBL of 150 mV/V, the improvement observed in Fig. 6.12(a) is 12 % and 31 %, respectively.

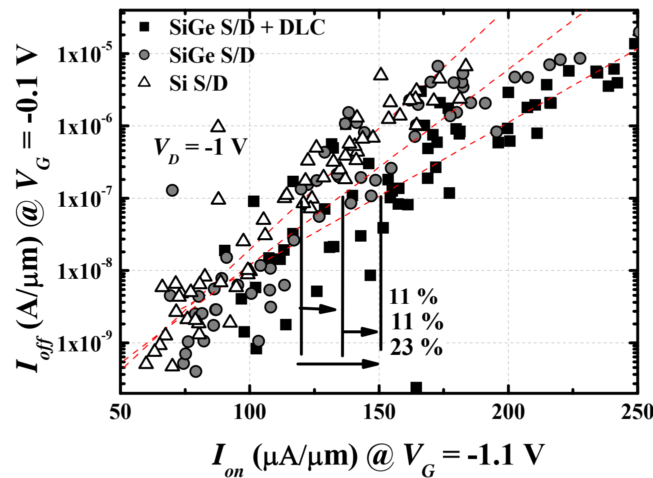


Fig. 6.9. I_{off}-I_{on} plot showing I_{on} enhancement of 11% and 23% for p-FETs with SiGe S/D only and p-FETs with SiGe S/D and DLC liner, respectively.

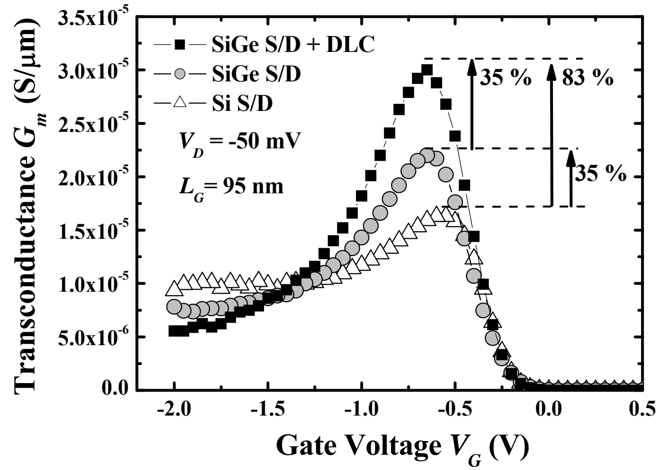


Fig. 6.10. Peak transconductance increases by 35% and 83% for p-FET with SiGe S/D only and p-FET with SiGe S/D and DLC liner, respectively.

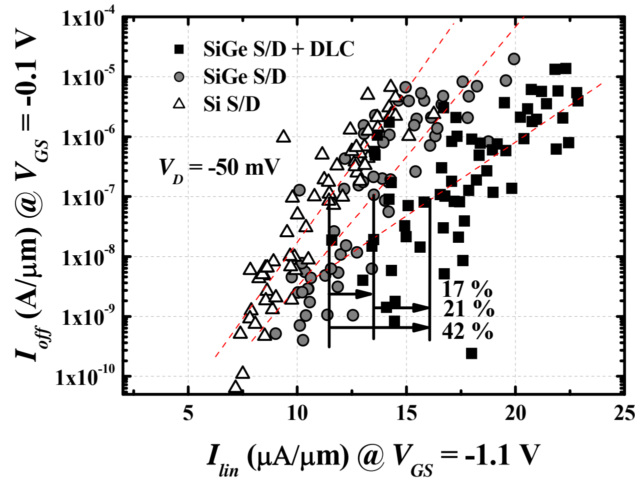
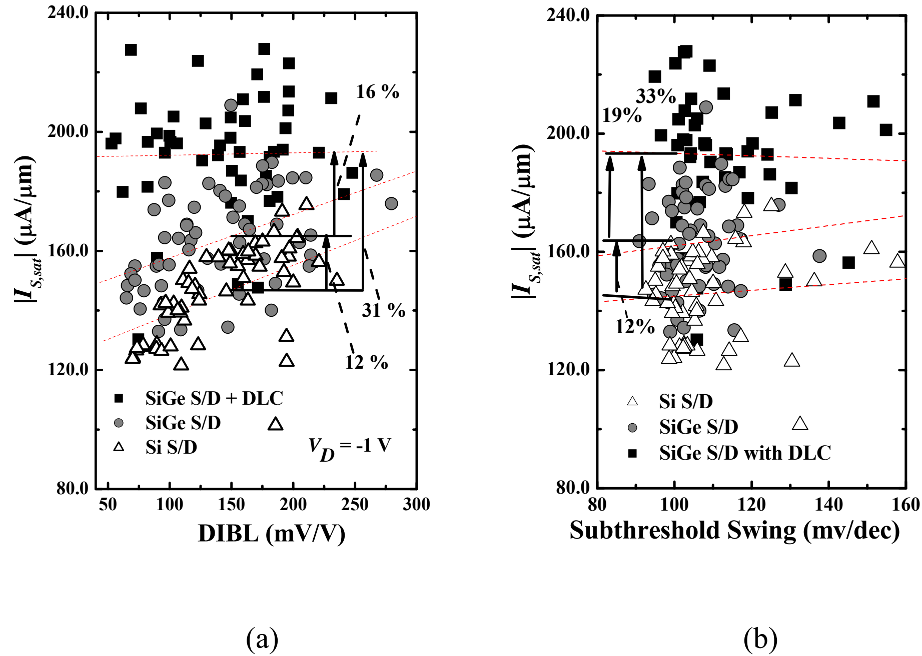


Fig. 6.11. 17 % enhancement of I_{lin} can be observed for devices with SiGe S/D and with the addition of DLC liner, a total of 42 % enhancement can be achieved.

Likewise, comparing the devices under the same subthreshold swing for similar short channel effects (Fig. 6.12(b)), show an enhancement of $I_{S,sat}$ of 12% and 33% for p-FETs with SiGe S/D and p-FETs with SiGe S/D and DLC, respectively.



(a) (b)

Fig. 6.12. $I_{S,sat}$ taken at V_G-V_{th} = -1 V and V_D = -1 V. (a) At a fixed DIBL of 150 mV/V and (b) SS of 100 mV/dec, device with DLC show 31% and 33% enhancement of $I_{S,sat}$ over the control device.

6.4.2 Impact of a Recessed SiGe S/D on the Strain transfer of DLC

The effect of a recessed S/D profile on strain transfer due to DLC is also studied. The performance of the devices with recessed-SiGe S/D is observed to be degraded when compared to devices having either Si or SiGe S/D as shown by the I_{off}-I_{on} plot in Fig. 6.13. The degradation in performance is possibly caused by an increase in series resistance due to the recessed S/D profile. A comparison of I_S-V_G characteristics were also made for a device with SiGe S/D, recessed SiGe S/D and recessed SiGe S/D integrated with the DLC stressed liner. These devices demonstrate similar short channel effects (Fig. 6.14(a)) but for the device with recessed SiGe S/D, a much higher series resistance is seen as (estimated at high gate bias from the plot of R_{tot}) shown in the inset in Fig. 6.14(a). However, when the device with recessed-SiGe S/D is integrated with the DLC liner, a significant

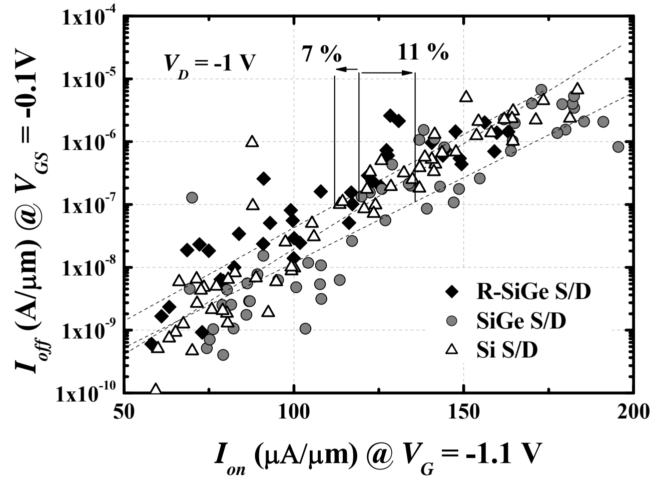


Fig. 6.13. 7 % degradation of I_{on} can be observed for devices with recessed SiGe S/D when compared to the device with Si S/D at an I_{off} of 100 nA/μm. The degradation is even larger when compared to the device with SiGe S/D.

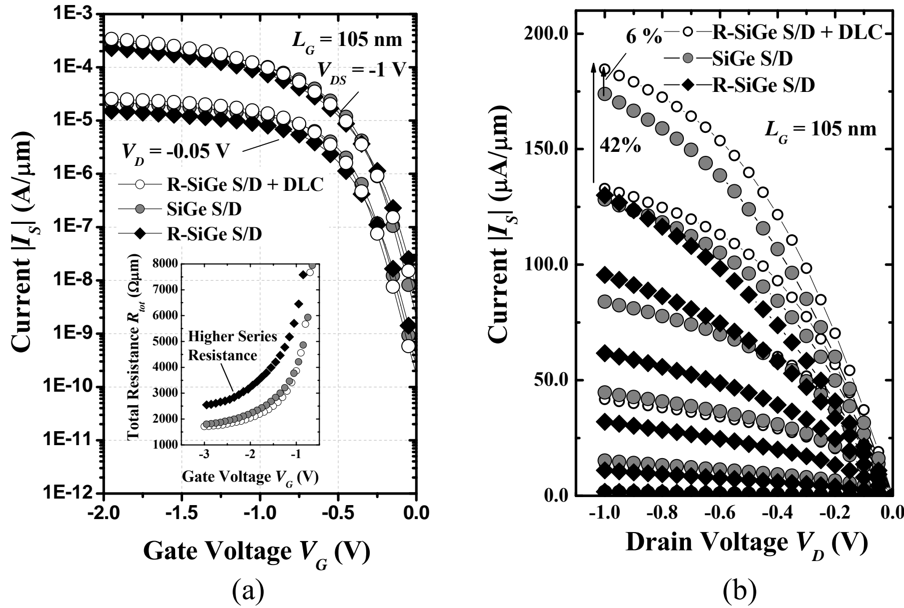
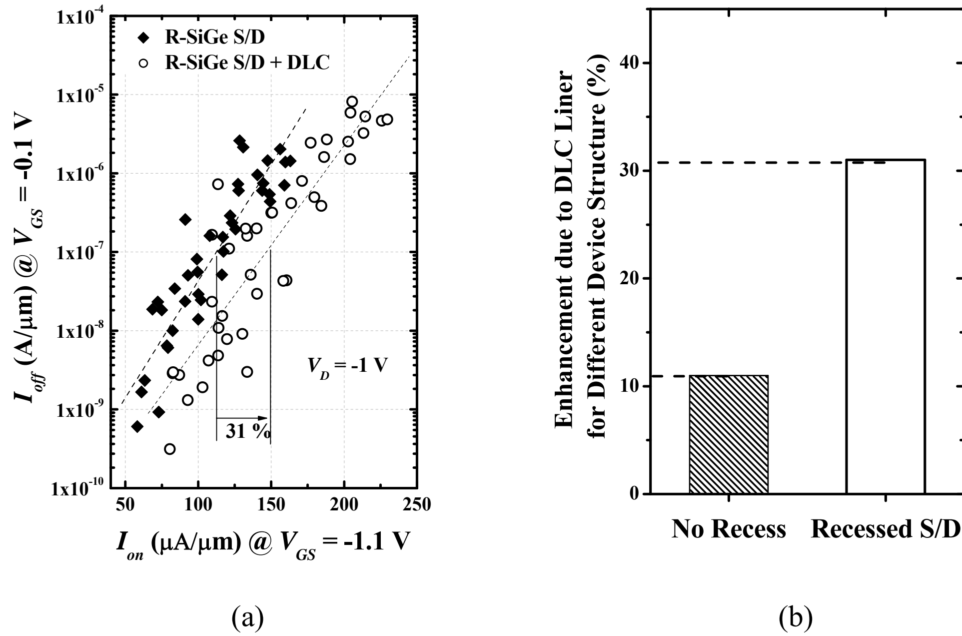


Fig. 6.14. (a) I_S-V_G characteristics of various planar devices showing similar subthreshold swing (SS) and DIBL. The inset in the graph show a higher series resistance for R-SiGe S/D device (b) Comparison of I_S-V_D characteristics of the devices, where P-FET with R-SiGe S/D and DLC shows 42% enhancement over device with R-SiGe S/D. The performance of devices with R-SiGe S/D is comparable or better than device with SiGe S/D.



(a) (b)

Fig. 6.15. (a) I_{off}-I_{on} plot showing I_{on} enhancement of 31% for p-FETs recessed SiGe S/D integrated with DLC as compared to one that does not have. (b) Comparison of enhancement due to DLC liner on devices with SiGe S/D, having two different S/D profiles (without and with recess S/D topology).

increase in saturation current of 42% was achieved and as such the device performed even better than the device with SiGe S/D by around 6% (Fig. 6.14(b)).

Comparison of devices having a recessed-SiGe S/D profile, with and without DLC liner is also made using the I_{on}-I_{off} plot (Fig. 6.15(a)). It can be observed that on average, a 31% enhancement of I_{on} is demonstrated at an I_{off} of 100 nA/μm. A summary of the effect of recessed SiGe S/D on the enhancement of I_{on} by DLC stressed liner is illustrated in Fig. 6.15(b). The improvement is larger in the case of a recessed profile as compared to a non-recessed case (enhancement of I_{on} taken from Fig. 6.9). A larger strain transfer from the DLC film can thus be obtained for the device with recessed S/D topology. Comparing to the device with SiGe S/D at similar short channel effects (ie. at a DIBL of 150 mV/V), device with recessed SiGe S/D integrated with DLC stressed liner is still able to perform

better as illustrated in Fig. 6.16. Due to the recessed S/D profile, the DLC liner is now closer to the channel and this increase the coupling effect of stress from the compressive film into the channel. In addition, in view of this characteristic, performance degradation due to process variation in recessed etch (deeper) and epi-growth rate (low) can be therefore be compensated by the DLC stressed liner.

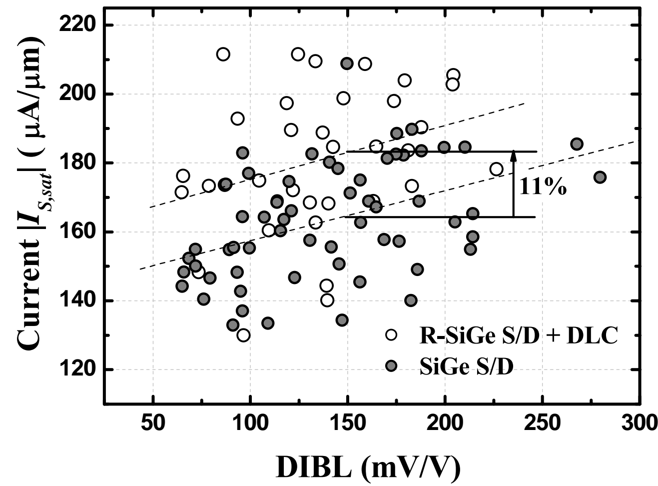


Fig. 6.16. $I_{S,sat}$ taken at V_G-V_{th} = -1 V and V_D = -1 V. At a fixed DIBL of 150 mV/V, device with a recessed SiGe S/D integrated with DLC stressed liner show 11% enhancement of I_{sat} over device with SiGe S/D.

6.5 Summary

Detail process data for DLC deposition was presented for the first time. P-channel bulk planar FET were employed in this work for technology demonstration. DLC liner stressor with an intrinsic stress of -5 GPa was integrated with SiGe S/D for the first time, demonstrating significant performance enhancement. Compared to a control device, device with SiGe S/D gives 11% I_{on} enhancement while device having SiGe S/D and DLC gives 23% I_{on} enhancement. DLC liner can provides a larger stress effect in the channel and a higher I_{on} if the S/D topology is slightly recessed.

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Chapter 7

Conclusion and Future Work

7.1 Conclusion

In this thesis, various techniques of straining the device had been explored to further enhance device performance on different transistor structure. In chapter 2, the effect of annealing the FinFET device having a TaN gate electrode capped with SiN has been investigated. Comparison of performance is done with a control device without the capping nitride during high temperature S/D anneal. As the major difference between the strained and control device is the presence of SiN, we believe that the constraint in the expansion of TaN gate electrode by the capped SiN results in a residual stress in the channel which improve the electron mobility. In the future, with the adoption of metal gate and high-*k* dielectric, stress induced by these new materials will have to be taken into considerations and can exploited for better device performance.

In chapter 3, a new poly Si gate etch process specifically for FinFET device was developed to remove the gate stringer on the fin sidewalls. The lateral etching of the poly gate which results in the breaking of the gate line is overcome by tuning the gate etch recipe to increase the sidewalls passivation in the main etch step. Working devices with L_G as small as 26 nm is therefore achieved. In addition, the removal of the gate stringer allows the epi-raised S/D growth to

occur also at the sidewalls which improve device performance. Recently, the importance and challenges of this issue are mention again in [7.1].

For FinFET device, due to its unique 3D-structure, strain technology that is used in the planar devices will have to be applied accordingly. In chapter 4, novel strain techniques are employed to further enhance the performance of FinFET with SiGe raised S/D. Ge condensation on raised SiGe S/D is investigated to form an embedded SiGe S/D stressor for FinFET device. This avoids the challenge of performing an isotropic recess etch on the fin at the S/D regions and possible Si migration issues for a narrow Si fin during the epitaxy growth process. In addition to performing raised S/D on the fin sidewalls, by recessing the box and allowing the SiGe to grow beyond and possibly encroach beneath the fin, we have shown that the device performance can be further enhanced. The additional growth in SiGe volume allows better enhancement of strain and series resistance improvement. This is simply achieved by extending the pre-epitaxy cleaning time which is an essential step for epitaxy growth. Therefore, little cost is incurred as no additional equipment or process step is added.

With the scaling down of device dimension and gate pitch, the effective stress transfer from the highly stressed CESL to the channel decreases. In chapter 5, a new CESL material diamond-like carbon (DLC) is introduced, having a much higher intrinsic compressive stress than the currently used SiN. The properties of DLC are characterized and integration with both p-channel SOI and FinFET devices show improvement in drive current over the respective control device. This is attributed to the strain transfer from the highly compressive stress DLC to the channel which increases hole mobility.

More extensive works were done to study DLC as a CESL material in chapter 6. It is found that the intrinsic stress of DLC increases with the used of a larger filter current while there is little change when the substrate bias is varied. When DLC is integrated with a bulk planar device having an embedded SiGe S/D stressor, further enhancement in device performance is observed. This shows that device performance can be further improved by combining multiple stressors to achieve a higher strain effect. In addition, we have also showed that the DLC stressed liner can provide a high strain effect when deposited on an intentionally recessed SiGe S/D when compared to an un-recessed one. Therefore, DLC stressed liner can improve the performance of devices that suffered from process non-uniformity due to over recess etched and insufficient Si/SiGe epitaxy-growth in the S/D regions.

7.2 Future Work

This thesis has explored the various techniques for straining the device for CMOS performance enhancement in which novel device structures and materials are introduced that can be useful for sub-32 nm technology. Further works can be done to bring an even larger improvement in the device performance. For example, for the FinFET device with *e*Π-SiGe S/D, if one can remove the oxide beneath the fin at the S/D regions entirely, and performed the epitaxy raised S/D, a wrap-around S/D stressor can be formed. This gives an even larger strain effect and the series resistance can also be improved greatly.

However, to achieve this, a major concern is the much longer HF cleaning time to be used which tend to etch away the liner oxide beneath the SiN spacer. The consequences can be either the lifting-off of the spacer or the growth of SiGe

into the space created by the absence of the liner and when this touches the gate, it results in a short between the gate and S/D electrodes. To overcome this issue, spacer consisting of purely SiN or other material that will not be attacked by HF, can be adopted but this place a greater challenge in the etching of spacer, which need to be able to etch-stop on the Si fin and at the same time remove the spacer stringer. A spacer etch recipe having an extremely high selectivity between the spacer material and Si is therefore needed.

For the study of DLC, more investigations are needed to characterize its properties for CESL application. The respective etch selectivity between oxide and the bottom silicide will be needed for DLC to function as a CESL material. Furthermore, after the removal of DLC stressed liner in the contact holes, proper cleaning process is also required. This can be quite challenging, as DLC maybe inert to the common chemicals used in Si processing. While it is known that post-deposition annealing can change the sp^2/sp^3 bond ratio, on the other hand it has been reported that when the initial sp^3 content is high (> 80%), the film is stable and little change in sp^2/sp^3 bond is observed during post-deposition thermal anneal [7.2],[7.3]. Therefore, achieving DLC film with high sp^3 content as deposited is of great importance. More importantly, the intrinsic stress of DLC can also be affected by the post-deposition process where a 60% reduction of stress can occur at an annealing temperature of 400^0C [7.3]. This reduction in the intrinsic stress of DLC will reduce the effectiveness of DLC as a CESL stressor and thus is undesirable. However, in the actual process flow, the thermal budget that DLC film see, will most likely be due to the deposition process of another dielectric film and hence interaction between DLC and the dielectric film during the deposition process itself may have a different impact on the stress evolution.

More works will therefore be needed to study this and also to increase/retain the stress of DLC during the subsequent process after DLC is deposited.

For device performance, as it is has been reported that the permittivity of DLC can be tuned to quite low, it will be interesting to investigate the effect on parasitic capacitance by comparing DLC stressed liner to SiN. As the distance between gate to contact plug decreases, this parasitic capacitance component will tend to increase and therefore DLC stressed liner maybe able to provide an additional advantage. To further improve the stress coupling of DLC to the channel, the DLC should be place closer to the channel and it may be worthwhile to study this by either using a thinner spacer or to remove it entirely before depositing the DLC stressed liner [7.4]. The scheme of removing the spacer will also aid in the trend of decreasing gate pitch and the increased of parasitic capacitance. As mention in chapter 1, currently, Ge channel transistor is also being study due to its high intrinsic mobility. By integrating DLC with a p-channel Ge transistor, it is likely that the device performance can be further improved. For p-channel FinFET with SiGe or Ge [7.5] raised S/D, it will be great if DLC is compatible with this scheme as it is expected that a further boast in device performance can be achieved with the combination of the various stressors on multiple-gates transistor platform. Lastly, study of reliability issues, like negative bias temperature instability (NBTI) should also be done for devices having DLC stressed liner with or without the SiGe S/D stressor.

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Appendix: Publication List

Journal/Letter Publications

From Thesis Work:

[1] **K.-M. Tan**, T.-Y. Liow, R. T.-P. Lee, C.-H. Tung, G. S. Samudra, W.-J. Yoo, and Y.-C. Yeo, "Drive current enhancement in FinFETs using gate-induced stress," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 769 - 771, Sep. 2006.

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