HIGH-SPEED FLASH ADC DESIGN

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NATIONAL UNIVERSITY OF SINGAPORE

2006

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(B.Eng.(Hons.), NUS)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER

ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2006

ACKNOWLEDGEMENTS

I would like to thank the National University of Singapore for the support they had given, which had led to the success of this Master Project.

I would also like to thank my project supervisors, Associate Professor Lian Yong and Dr Shi Bo, for their kind support and advice so as to make this project a success.

Many thanks should be given to my colleagues in the Signal Processing and VLSI Design Laboratory for their support and also joy given to me during these two and a half years.

Last but not least, I would like to thank everyone who had helped, in one way or another, towards the completion of this project.

TABLE OF CONTENTS

SUMMARY

As Ultra Wideband (UWB) Communications become more and more popular, the design of analog-to-digital converters (ADC) used in this area also requires more attention. The ADC sampling speed will be the most critical issue. Flash ADCs are known to be one of the fastest possible converters. But the performance of a flash ADC strongly depends on that of their constituent comparators. For an *N*-bit flash ADC, $2^N - 1$ comparators are needed. Therefore, how to increase the comparator speed while not increasing power dissipation too much is a challenge to the designer. Another challenge is that the resolvable minimum differential input should not be too large such that a flash ADC with moderate resolution can be built. To reduce minimum input, input referred offset must also be reduced.

In this thesis, two types of master-slave comparators and the analog part of a flash ADC built on one of the comparators are presented. Some critical design issues are considered when designing the master-slave comparators, which try to increase the sampling speed and reduce minimum differential input voltage while maintaining power dissipation at a relatively low level. The final comparator design for both topologies presented has a very high speed of 16 GHz clock rate with post-layout simulations. One of the two types of the master-slave comparators uses standard design. The other one uses an improved bias scheme which can give rise to the optimum bias condition in master-slave comparators in term of regeneration time constant and power dissipation. Both of the comparators have also passed the overdrive recovery test which is the most stringent test for comparators at a clock frequency of 16 GHz.

The analog part of a flash ADC is built based on the master-slave comparator with the improved bias scheme. A track-and-hold amplifier is added before the differential resistive-ladder of the flash ADC to improve its dynamic performance. Actually due to the increased requirements on the sampling circuit with respect to sampling jitter at gigahertz operating speed, it is almost necessary to incorporate a track-and-hold amplifier in the flash ADC design. A bubble error correction logic circuit is added after the slave comparators which can correct bubble errors. The analog part of the flash ADC designed can work at a sampling speed of 6 GSample/s with resolution of 5 bits. The thermometer-to-binary encoder is added as the last stage to generate the flash ADC output.

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

AD	Analog-to-Digital
ADC	Analog-to-Digital Converter
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
DAC	Digital-to-Analog Converter
DNL	Differential Nonlinearity
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
FoM	Figure-of-Merit
HBT	Heterojunction Bipolar Transistor
IF	Intermediate Frequency
INL	Integral Nonlinearity
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
RF	Radio Frequency
RMS	Root Mean Square
SEF	Switched Emitter Follower
SFDR	Spurious-Free Dynamic Range
SiGe	Silicon-Germanium
SNDR	Signal-to-(Noise + Distortion) Ratio
SNR	Signal-to-Noise Ratio

SOC	System-On-Chip
THA	Track-and-Hold Amplifier
UWB	Ultra Wideband
VLSI	Very Large Scale Integration

α	Common-base current gain
β	Common-emitter current gain
ε_q	Quantization error
I_S	Saturation current
V_A	Early voltage
V_T	Thermal voltage
r_π	Small-signal input resistance between base and emitter, looking into the base
r_e	Emitter resistance
r_b	Base resistance
g_m	Transconductance
r_o	Output resistance
f_T	Transit frequency
$f_{\max}$	Maximum oscillation frequency
BV_{CEO}	Collector to emitter breakdown voltage

CHAPTER 1

INTRODUCTION

1.1 Introduction to Analog-to-Digital Converter

Data conversion provides the link between the analog world and digital systems and is performed by means of sampling circuits, analog-to-digital converters (ADC), and digital-to-analog converters (DAC). With the increasing use of digital computing and signal processing in applications such as medical imaging, instrumentation, consumer electronics, and communications, the field of data conversion systems has rapidly expanded over the past thirty years.

Compared with their analog counterparts, digital circuits exhibit lower sensitivity to noise and more robustness to supply and process variations, allow easier design and test automation, and offer more extensive programmability. But, the primary factor that has made digital circuits and processors ubiquitous in all aspects of our lives is the boost in their performance as a result of advances in integrated circuit technologies. In particular, scaling properties of very large scale integration (VLSI) processes have allowed every new generation of digital circuits to attain higher speed, more functionality per chip, lower power dissipation, or lower cost. These trends have also been augmented by circuit and architecture innovations as well as improved analysis and synthesis computer-aided design (CAD) tools.

While the above merits of digital circuits provide a strong incentive to make the world digital, two aspects of our physical environment impede such globalization: (1) naturally occurring signals are analog, and (2) human beings perceive and retain information in analog form (at least on a macroscopic scale). Therefore, ADCs are

needed to convert those analog signals to digital form for processing and DACs are needed to convert processed digital signals back to analog form so that they can be accepted by human being or other natural things. The important functions of ADCs and DACs in connecting analog world and digital world thereby are clearly shown.

Due to their extensive use of analog and mixed analog-digital operations, A/D converters are often the bottleneck in data processing applications, limiting the overall speed or precision.

The basic function of an A/D converter is described as follows. An ADC produces a digital output, D, as a function of the analog input, A:

$$D = f(A). \tag{1.1}$$

While the input can assume an infinite number of values, the output can be selected from only a finite set of codes given by the converter's output word length (i.e. resolution). Thus, the ADC must approximate each input level with one of these codes. This is accomplished, for example, by generating a set of reference voltages corresponding to each code, comparing the analog input with each reference, and selecting the reference (and its code) closest to the input level. In most ADCs, the analog input is a voltage quantity because comparing, routing and storing are easier for voltages than for currents.

Figure 1.1(a) depicts a simple ADC input/output characteristic where the analog input is approximated with the *nearest smaller* reference level. If the digital output is an m-bit binary number, then

$$D = \left\lfloor 2^m \frac{A}{V_{REF}} \right\rfloor, \tag{1.2}$$

where [●] denotes the integer part of the argument and V_{REF} is the input full-scale voltage. Note that the minimum change in the input that causes a change in the output is $\Delta = V_{REF} / 2^m$ and corresponds to the least significant bit of the digital representation.

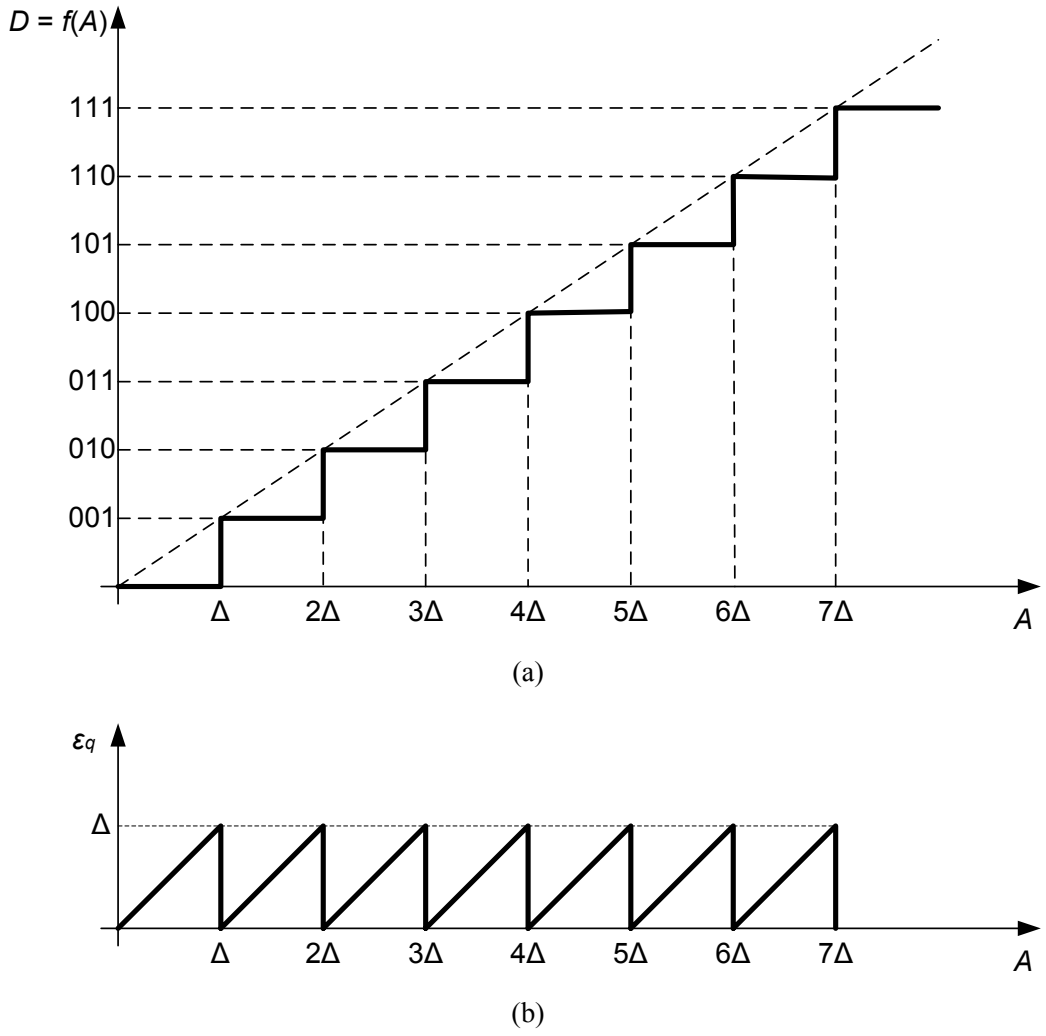


Figure 1.1: (a) Input/output characteristic; (b) quantization error of an A/D converter

The approximation or "routing" effect in A/D converters is called "quantization", and the difference between the original input and the digitized output is called the "quantization error" and is denoted here by ε_q. For the characteristic of Figure 1.1(a), ε_q varies as shown in Figure 1.1(b), with the maximum occurring before each code transition. This error decreases as the resolution increases, and its effect can

be viewed as additive noise (called "quantization noise") appearing at the output. Thus, even an "ideal" *m*-bit ADC introduces nonzero noise in the converted signal simply due to quantization.

Some of the performance metrics of ADCs are described here. Illustrated in Figure 1.2, the following definitions describe the static behavior of ADCs.

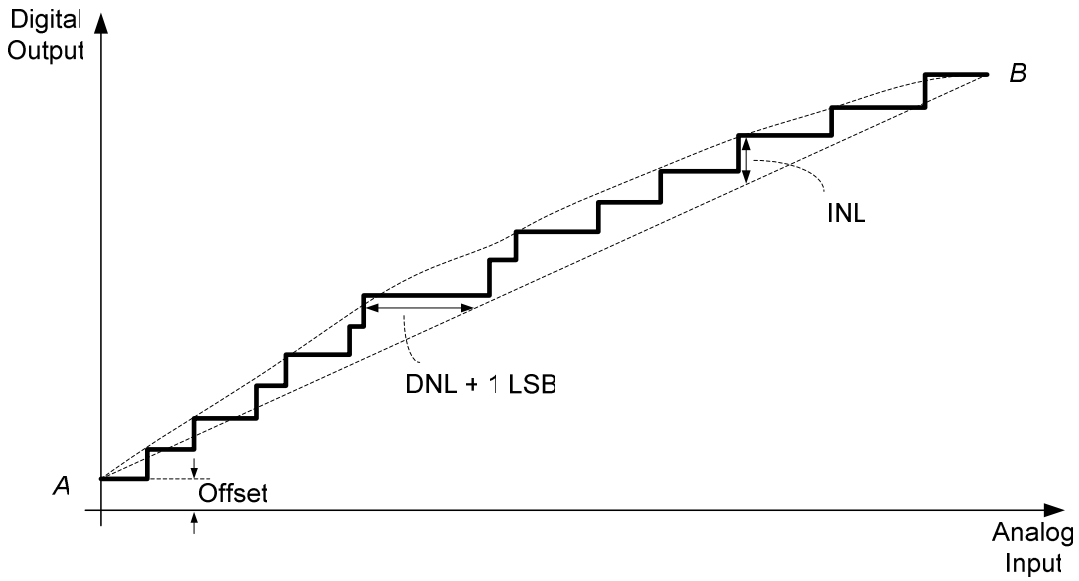


Figure 1.2: Static ADC metrics

- Differential nonlinearity (DNL) is the worst-case deviation in the difference between two consecutive code transition points on the input axis from the ideal value of 1 LSB.
- Integral nonlinearity (INL) is the worst-case deviation of the input/output characteristic from a straight line passed through its end points (line *AB* in Figure 1.2). The overall difference plot is called the INL profile.
- Offset is the vertical intercept of the straight line through the end points.
- Gain error is the deviation of the slope of line *AB* from its ideal value (usually unity).

Often specified as a function of the sampling and input frequencies, the following terms are used to characterize the dynamic performance of converters.

- Signal-to-noise ratio (SNR) is the ratio of the signal power to the total noise power at the output (usually measured for sinusoidal input).
- Signal-to-(noise + distortion) ratio (SNDR) is the ratio of the signal power to the total noise and harmonic power at the output, when the input is a sinusoid.
- Effective number of bits (ENOB) is defined by the following equation [1]:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}_P - 1.76}{6.02}, \tag{1.3}$$

  where SNDR_P is the peak SNDR of the converter expressed in decibels.
- Dynamic range is the ratio of the power of a full-scale sinusoidal input to the power of a sinusoidal input for which SNR = 0 dB.

Now different types of analog-to-digital converters are briefly summarized here. A convenient way to classify all ADCs is to group them into different categories, which differ in terms of conversion speed. Then, a way to rapidly inspect the speed of each converter is to see how many clock cycles are used to perform a single conversion. Three main categories are identified as follows.

1) Converters using an exponential number of cycles, in the order of 2^N, where N is the converter resolution. The integrating dual ramp and incremental ADC, which can offer very high resolution (16-bit or more), are part of this category.
2) A very wide category of converters has medium-high speed and high-medium resolution. Here are some examples: Sigma-delta converters, which use a number of clock cycles still exponential 2^k, with k somewhat lower than N; the algorithmic converters, which use $m \times N$ clock cycles, arising from m clock

cycles used to resolve each bit; and finally the successive approximation converters, which use normally around N clock cycles, with one clock cycle per bit.

3) The last category of highest speed converters, which use just 1 – 2 clock cycles to perform a conversion. The two-step flash, the full flash, the pipeline, and the folding ADCs fall in this category.

Table 1.1: A/D converter classification

Type	**Clock Cycles / Conversion**	**Family**
Very Fast Speed – Medium, Low Resolution		
Folding	1	(full) Nyquist
Full Flash	1	(full) Nyquist
Pipeline	1 – 2	(full) Nyquist
Two-step Flash	2	(full) Nyquist
Medium, Fast Speed – High, Medium Resolution		
Successive Approximation	$\sim N$	Nyquist
Algorithmic	$\sim m \times N$	Nyquist
Sigma-Delta	$m \times N < 2^k < 2^N$	Oversampled
Slow Speed – Very High Resolution		
Incremental	$[2^N, 2^{N+1}]$	Nyquist
Integrating Dual Ramp	2^{N+1}	Nyquist

The terms “high”, “medium”, “low” resolution are purely indicative, and must be interpreted in a flexible way. For example, a pipeline or two-step flash “medium” resolution ADC can be in the order of up to 10-bits, anyway if self-calibration techniques are deployed, its resolution may increase to 12-bits or more. All the above

mentioned ADCs are summarized in Table 1.1. Also it is not uncommon to find data converters exploiting a combination of the ones listed in Table 1.1.

The classification of ADCs between the two big families of Oversampled or Nyquist rate ones is not obvious. A Nyquist-rate converter can be defined as an ADC capable to operate under Nyquist condition, namely with a sampling close to twice the maximum input frequency. All the converters listed in Table 1.1, apart from the sigma-delta, are suitable to operate in this way. The sigma-delta ADC, due to its structure, is quickly losing its performance if some level of oversampling is not applied. For some sigma-delta architectures, it is not mandatory to keep high oversampling ratios to achieve high performance. In fact, sigma-delta converters, even if commonly defined as oversampled converters, exploit the benefits of combining oversampling with quantization noise shaping. On the other hand, Nyquist rate converters, whenever possible, are slightly oversampled. Only the fastest Nyquist-rate ADCs in the category of 1 – 2 clock cycles (flash, pipeline, folding) are typically used in extreme sampling condition to not lose any speed performance. For this reason, they are also defined as "full Nyquist-rate" converters.

1.2 Introduction to Flash Analog-to-Digital Converter

The flash ADC, due to the exploitation of a full parallelism, is one of the fastest possible converters, since a conversion is handled within only one clock cycle. Its architecture is attractive because it is very simple, but it is area consuming and power hungry and also several design trade-offs are necessary. The electrical behavior of each block will be investigated in detail (Figure 1.3).

A resistive ladder, containing 2^N resistors, generates the reference voltages within the full scale range, going to the inverting inputs of the comparators, whilst the input signal is fed into the non-inverting inputs of the 2^{N-1} comparators. At the comparator outputs, a thermometer digital code, proportional to the input signal, is generated, and further converted onto an N-bit code by a 2^N-to-N encoder.

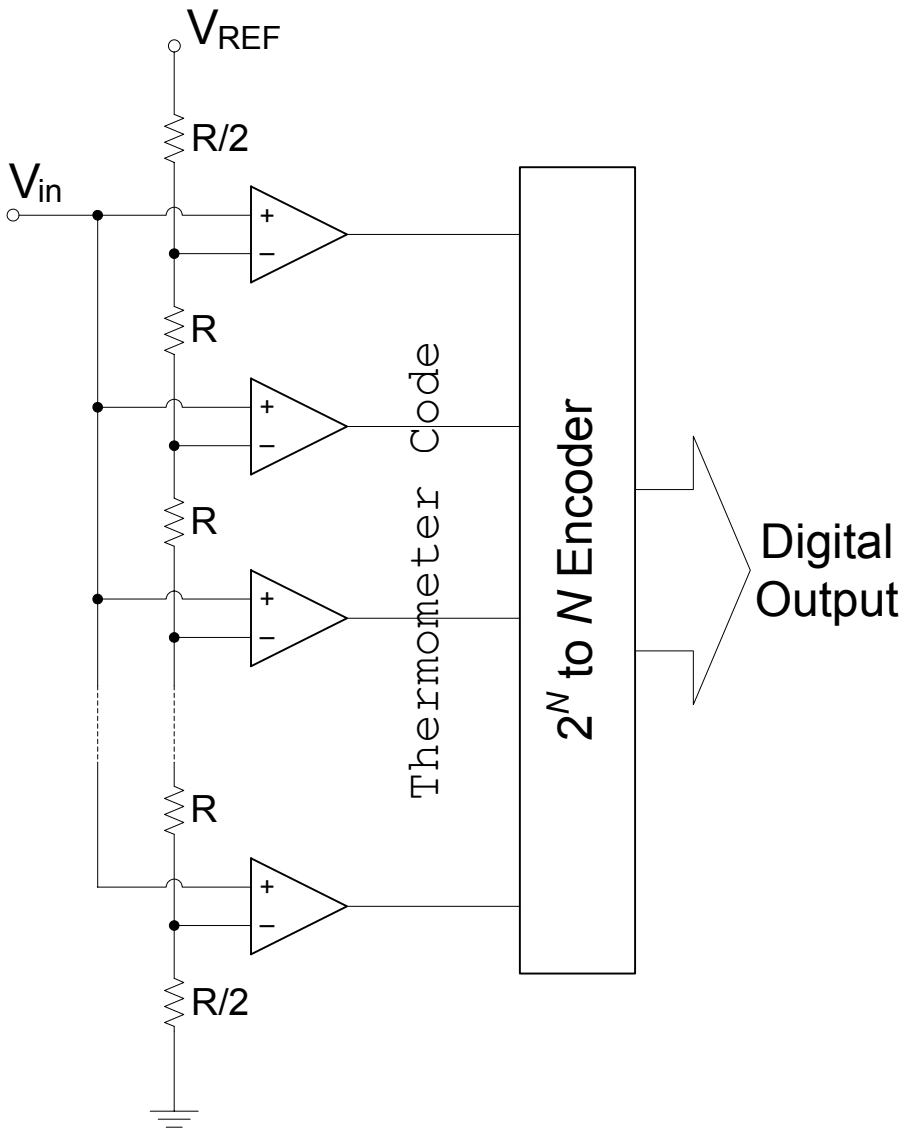


Figure 1.3: Flash ADC architecture

An interesting feature of the flash architecture is that an input track-and-hold amplifier (THA) is not necessary. In fact, the comparators typically use a first amplifier stage, cascaded with a dynamic latch, providing very high gain. The

comparators are clocked, and in a first phase the input is sampled and amplified, while in the second the difference between the signal and the reference is instantaneously latched. In practice, assuming that the master clock transition arrives simultaneously on all the latches, the 2^N comparators perform the operation of a distributed track-and-hold.

There are a number of considerations which limit the maximum resolution for this architecture to roughly N = 8-bit. The parallelism implies an exponential increase of area: for 8-bit $2^8 = 256$ comparators are necessary, whilst for 10-bit they rise up to $2^{10} = 1024$, which is a prohibitive number. The area occupation for high resolutions becomes so significant that makes its deployment not suitable, at least for SOC (System-On-Chip) applications. The increase of the number of comparators enhances the input capacitance with the same exponential rule. If from one side the track-and-hold is not necessary, on the other side a powerful voltage buffer is required to drive the load, and its design becomes impractical if not unfeasible if the capacitive load is excessive. Another limitation can arise from thermal dissipation. Since the flash ADC is used at high speed, the power consumption of the comparators is not negligible and power dissipation may not be handled by the IC package over a certain limit. The sizing of the comparator is probably the most critical issue of the design. About this issue, it is worth to note that a random offset of the comparator has the consequence that the real thermometer code, thus the digital code, is directly affected, producing nonlinearity errors. One possibility could be to reduce the offset by careful design, but this choice implies an increase of the input transistors area, and then of the input capacitance. The other is to perform offset compensation at each cycle, but this often results in loss of conversion speed, caused by the offset compensation, which can be the bottleneck operation in terms of speed; the only way to recover the situation is to

increase further the consumption. Other critical design issues that need to be addressed are: 1) loading effect of the resistive ladder, causing nonlinearity, kickback noise; 2) capacitive coupling at the comparator inputs, disturbing the input signal and reference ladder tap points; 3) clock dispersion, causing non perfect distribute sampling of the input signal. In conclusion, the flash ADC is an attractive solution in terms of architecture due to its simple structure, but the resolution should be kept low for performance and mainly cost considerations.

1.3 Introduction to High-Speed Comparator

The performance of A/D converters that employ parallelism to achieve a high speed strongly depends on that of their constituent comparators. In particular, flash architecture requires great attention to the constraints imposed on the overall system by the large number of comparators.

Comparison is in effect a binary phenomenon that produces a logic output of ONE or ZERO depending on the polarity of a given input. Figure 1.4(a) depicts the input/output characteristic of an ideal comparator, indicating an abrupt transition (hence infinite gain) at $V_{in,1} - V_{in,2} = 0$. This nonlinear characteristic can be approximated with that of a high-gain amplifier, as shown in Figure 1.4(b). Here, the slope of the characteristic around $V_{in,1} = V_{in,2}$ is equal to the small-signal gain of the amplifier in its active region (A_V), and the output reaches a saturation level if $\left|V_{in,1} - V_{in,2}\right|$ is sufficiently large. Thus, the circuit generates well-defined logic outputs if $\left|V_{in,1} - V_{in,2}\right| > V_H / A_V$, suggesting that the comparison result is reliable only for input differences greater than V_H / A_V . In other words, the minimum input that can be

resolved is approximately equal to V_H / A_V. (The effect of noise is ignored here.) As a consequence, higher resolutions can be obtained only by increasing A_V because V_H, the logic output, cannot be arbitrarily reduced. Since amplifiers usually exhibit strong trade-offs among their speed, gain, and power dissipation, a comparator using a high-gain amplifier will also suffer from the same trade-offs.

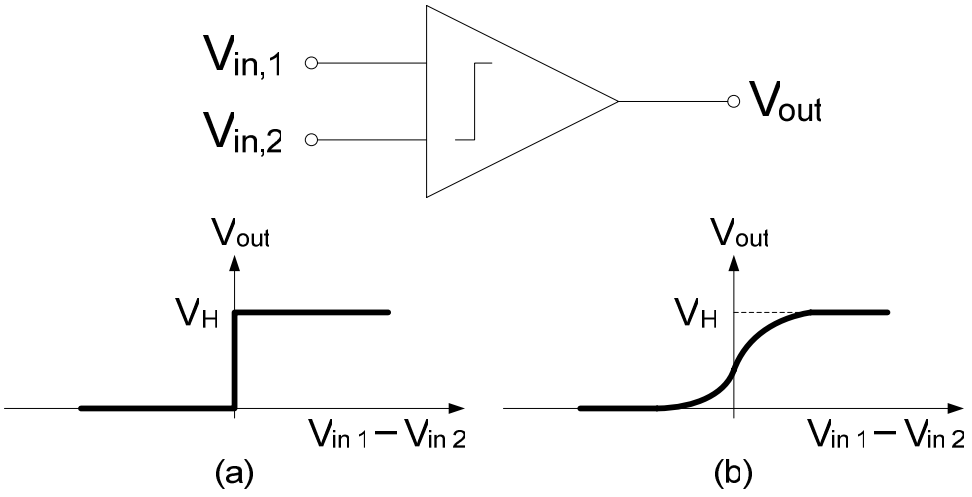


Figure 1.4: Input/output characteristic of (a) an ideal comparator, (b) a high-gain amplifier

Since the amplifiers used in comparators need not be either linear or closed-loop, they can incorporate positive feedback to attain virtually infinite gain. However, to avoid unwanted latch-up, the positive-feedback amplifier must be enabled only at the proper time; i.e., the overall gain of the comparator must change from a relatively small value to a very large value upon assertion of a command.

Figure 1.5 illustrates a typical comparator architecture often utilized in A/D converters. It consists of a preamplifier A_1 and a latch and has two modes of operation: tracking and latching. In the tracking mode, A_1 is enabled to amplify the input difference, hence its output "tracks" the input, while the latch is disabled. In the latching mode, A_1 is disabled and the latch is enabled (strobed) so that the instantaneous output of A_1 is regeneratively amplified and logic levels are produced at

V_{out}. Note that it is assumed that the clock edge is sufficiently fast so that the output of A_1 does not diminish during the transition from tracking to latching due to the parasitic capacitance at the output of A_1. Another advantage of the architecture of Figure 1.5 over a simple high-gain amplifier is that the strobe signal (*CLK*) can be used to define a sampling instant at which the polarity of the input difference is stored.

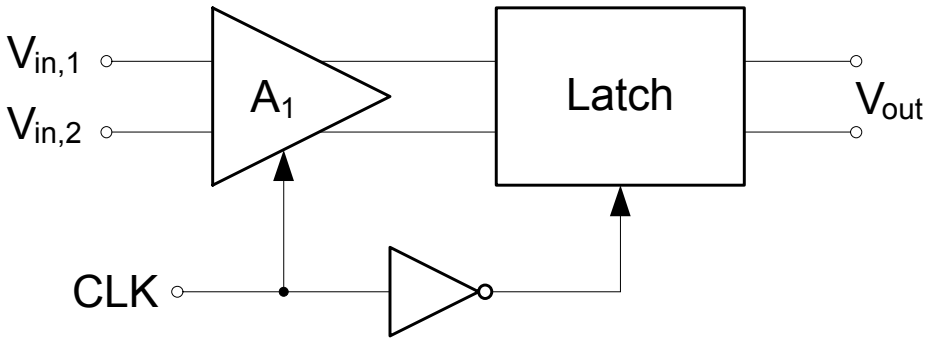


Figure 1.5: Typical comparator architecture

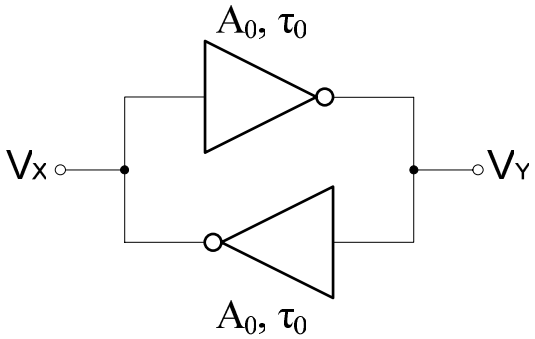


Figure 1.6: A latch comprising two back-to-back amplifiers

The use of a latch to perform sampling and amplification of a voltage difference entails an important issue related to the output response in the presence of small inputs: metastability. Figure 1.6 shows a latch comprising two identical single-pole inverting amplifiers each with a small-signal gain of $-A_0$ ($A_0 > 0$) and a characteristic time constant of τ_0. Assume the initial difference between V_X and V_Y is V_{XY0}, then after a time period of t, the difference becomes [1]

$$V_X - V_Y = V_{XY0} \exp\left[\left(A_0 - 1 \right) \frac{t}{\tau_0} \right]. \tag{1.4}$$

For a typical latch, $A_0 \gg 1$, yielding the important property that the argument of the exponential function is *positive* and hence $V_X - V_Y$ regenerates rapidly. The regeneration time constant is equal to $\tau_0 / \left(A_0 - 1 \right)$.

An important aspect of latch design is the time needed to produce logic levels after the circuit has sampled a small difference. If $V_X - V_Y$ is to reach a certain value V_{XY1} before it is interpreted as a valid logic level, then the time required for regeneration is

$$T_1 = \frac{\tau_0}{A_0 - 1} \ln \frac{V_{XY1}}{V_{XY0}}. \tag{1.5}$$

Equation (1.5) indicates that T_1 is a function of $\tau_0 / \left(A_0 - 1 \right)$ (and hence the unity-gain bandwidth of each amplifier) as well as the initial voltage difference V_{XY0}. Thus, the circuit has infinite gain if it is given infinite time provided there are no other limitations, such as the bias current. In other words, if at the sampling instant V_{XY0} is very small, T_1 will be quite long. This phenomenon is called "metastability" and requires great attention whenever a latch samples a signal that has no timing relationship with the clock.

Since in most practical cases V_{XY0} is (or can be considered) a random variable, metastability must be quantified in terms of the probability of its occurrence. Suppose in a system using a clock of period T_C, each latch is allowed a regeneration time of $T_C / 2$. Then, a metastable state occurs if a latch does not produce an output of V_{XY1}

within $T_C/2$ seconds. If the sampled value V_{XY0} has a uniform distribution between $-V_{XY1}$ and $+V_{XY1}$, then the probability of observing a metastable state is [2] [3]

$$P(T_1 > T_C) = \exp\frac{-(A_0 - 1)T_C}{2\tau_0}. \tag{1.6}$$

This probability can be lowered by increasing A_0, decreasing τ_0, or pipelining the comparator output.

Here, some of the comparator performance metrics are described as follows.

- Resolution is the minimum input difference that yields a correct digital output. It is limited by the input-referred offset and noise of both the preamplifier and the latch. We call this minimum input 1 LSB (also denoted by V_{LSB}).
- Comparison rate is the maximum clock frequency at which the comparator can recover from a full-scale overdrive and correctly respond to a subsequent 1-LSB input. This rate is limited by the recovery time of the preamplifier as well as the regeneration time constant of the latch.
- Dynamic range is the ratio of the maximum input swing to the minimum resolvable input.
- Kickback noise is the power of the transient noise observed at the comparator input due to switching of the amplifier and the latch.

In addition to these, input capacitance, input bias current, and power dissipation are other important parameters that become critical if a large number of comparators are connected in parallel.

1.4 Introduction to SiGe Heterojunction Bipolar Transistor

Traditionally, silicon (Si) integrated circuits such as those found in computers, appliances and many other applications have used Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Bipolar Junction Transistors (BJTs), but neither of these transistors operate above a few gigahertz because of the material properties of Si.

Heterojunction bipolar transistors are bipolar junction transistors, which are composed of at least two different semiconductors. As a result, the energy bandgap as well as all other material properties can be different in the emitter, base and collector. Moreover, a gradual change also called grading of the material is possible within each region. Heterojunction bipolar transistors are not just an added complication. On the contrary, the use of heterojunctions provides an additional degree of freedom, which can result in vastly improved devices compared to the homojunction counterparts.

Since a heterojunction transistor can have large current gain, even if the base doping density is higher than the emitter doping density, the base can be much thinner even for the same punchthrough voltage. As a result one can reduce the base transit time without increasing the emitter charging time, while maintaining the same emitter current density. The transit frequency can be further improved by using materials with a higher mobility for the base layer and higher saturation velocity for the collector layer.

The maximum oscillation frequency can also be further improved. The improved oscillation frequency means the increase of the transit frequency. The higher base doping also provides a lower base resistance and a further improvement of f_{max}. As in the case of a homojunction BJT, the collector doping can be adjusted to trade off

the collector transit time for a lower base-collector capacitance. The fundamental restriction of heterojunction structures still applies, namely that the materials must have a similar lattice constant so that they can be grown without reducing the quality of the material.

Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) is similar to a conventional Si bipolar transistor except for the base, where the alloy combining silicon (Si) and germanium (Ge) is used as the base material. The material, SiGe, has narrower bandgap than Si. Ge composition is typically graded across the base to create an accelerating electric field for minority carriers moving across the base. A direct result of the Ge grading in the base is higher speed, and thus higher operating frequency. The transistor gain is also increased compared to a Si BJT, which can then be traded for a lower base resistance, and hence lower noise. For the same amount of operating current, SiGe HBT has a higher gain, lower RF noise, and lower $1/f$ noise than an identically constructed Si BJT. The higher raw speed can be traded for lower power consumption as well.

Table 1.2 compares different parameters among CMOS, Si BJTs and SiGe HBTs. The superior performance of SiGe HBTs with high operating frequency, good noise immunity is clearly shown. Therefore, SiGe HBTs are well suited to design integrated circuits above 10 GHz.

Table 1.2: Comparison of CMOS with conventional and SiGe BJTs

Parameter	CMOS	Si BJT	SiGe HBT
f_T	High	High	High
f_{max}	High	High	High
Linearity	Best	Good	Better
V_{be} (or V_T) tracking	Poor	Good	Good
$1/f$ noise	Poor	Good	Good
Broadband noise	Poor	Good	Good
Early voltage	Poor	OK	Good
Transconductance	Poor	Good	Good

1.5 Scope of the Whole Project

As Ultra Wideband (UWB) Communications become more and more popular, the design of analog-to-digital converters used in this area also requires more attention. The ADC sampling speed will be the most critical issue. Flash ADCs are known to be one of the fastest possible converters. But the performance of a flash ADC strongly depends on that of their constituent comparators. For an n-bit flash ADC, $2^n - 1$ comparators are needed. Therefore, how to increase the comparator speed while not increasing power dissipation too much is a challenge to the designer. Another challenge is that the resolvable minimum differential input should not be too large such that a flash ADC with moderate resolution can be built. To reduce minimum input, input referred offset must also be reduced. This thesis presents both a master-slave comparator design which tries to increase the sampling speed and reduce minimum differential input voltage while maintaining power dissipation at a relatively

low level and the analog part of a high-speed flash ADC design based on the master-slave comparator.

Post-layout simulations for the master-slave comparator and the analog part of the flash ADC have been done to verify their performance.

1.6 Contributions

A paper titled as "Design and analysis of a high-speed comparator" was published in the 1st IEEE International Workshop on Radio-Frequency Integration Technology. This paper presents the design and analysis of an ultra high-speed bipolar comparator based on master-slave architecture. The comparator can be used for very high speed data converters design. Master-slave structure is used to improve metastability behavior and reduce minimum differential input voltage. The contents of this paper will be elaborated in Chapter 3 and Chapter 5.

1.7 Organization of this Thesis

In this thesis, the high-speed comparator design and the analog part of a high-speed flash ADC design using HBT technology are discussed. The circuits' simulation results are also presented. The text is organized as follows:

Chapter 2: This chapter gives a literature review of high-speed comparator design and high-speed flash ADC design. A detailed introduction to the bipolar implementation of a high-speed comparator design will be given. Previous works on flash ADC design using CMOS and bipolar technology will be summarized.

Chapter 3: This chapter presents the high-speed comparator design using bipolar technology. Circuit analysis of some basic bipolar circuits will be given first, followed by the master-slave comparator design. Two topologies of the master-slave comparator will be described. The main difference between them is the bias scheme which affects power dissipation of the comparator.

Chapter 4: The design of the analog part of a flash ADC will be presented. By adding a track-and-hold amplifier and a differential resistive ladder which are in front of the master-slave comparator designed in Chapter 3 and a bubble error correction logic circuit after the comparator stage, the analog part of a flash ADC can be constructed. The digital part, i.e., the thermometer-to-binary encoder will also be briefly introduced.

Chapter 5: This chapter presents the simulation results of all the circuits built. The simulation results will verify the overall performance of the two types of master-slave comparator built in Chapter 3 and also the performance and correctness of the analog part of the flash ADC built in Chapter 4. The digital part, i.e., the thermometer-to-binary encoder will also be briefly introduced.

Chapter 6: This thesis concludes by showing how the goals of this project have been met. The important results obtained are highlighted.

CHAPTER 2

LITERATURE REVIEW

2.1 Review of High-Speed Comparator Design

Heterojunction bipolar transistors are used to implement the comparator architecture shown in Figure 1.5. Figure 2.1 depicts the circuit design [1]. The differential pair Q_3-Q_4 and resistors R_{L1}-R_{L2} form the preamplifier stage while transistors Q_5-Q_6 and resistors R_{L1}-R_{L2} form the latch stage. Two clock signals *track* and *latch* control the differential pair and the latch through Q_1 and Q_2, respectively. When *track* is high, the differential pair tracks the input and when *latch* is high, the latch establishes a positive feedback loop and amplifies the difference between V_{out1} and V_{out2} regeneratively.

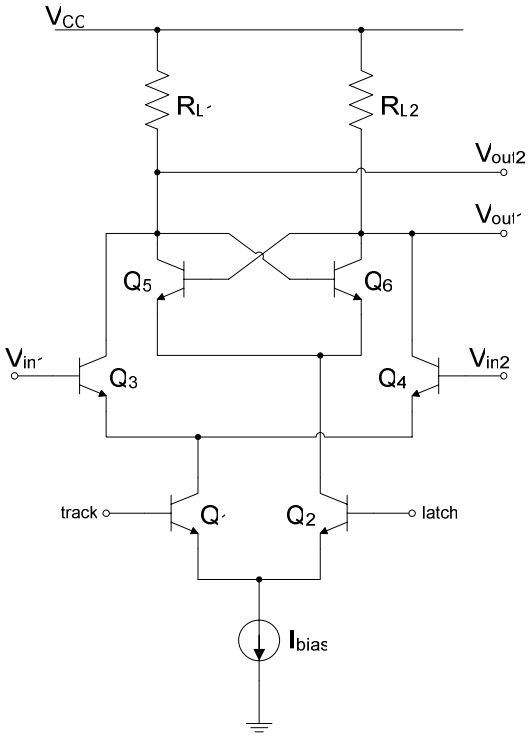


Figure 2.1: Bipolar implementation of the comparator architecture

It is instructive to derive some of the performance metrics of this comparator so as to understand its limitations.

The resolution of the comparator depends on both its input offset voltage and its input-referred noise. The input offset voltage arises from the mismatch between nominally identical devices Q_3-Q_4, Q_5-Q_6 and R_{L1}-R_{L2}. Since mismatch contributions of Q_5-Q_6 and R_{L1}-R_{L2} appear at the output, they are divided by the voltage gain of the differential pair ($g_{m34}R_L$, where R_L is the mean value of R_{L1} and R_{L2}) when referred to the input. For two nominally identical bipolar transistors, the V_{BE} mismatch can be expressed as [4]

$$\begin{aligned} \Delta V_{\mathrm{BE}} &= V_T \ln \frac{\Delta I_S}{I_S} \\ &= V_T \ln \frac{\Delta A}{A} \\ &\approx V_T \frac{\Delta A}{A}, \end{aligned} \tag{2.1}$$

where ΔI_S and I_S are the standard deviation and mean value of the saturation current, respectively, and ΔA and A are those of the emitter areas. Equation (2.1) indicates that if, for example, two transistors have a 10% emitter area mismatch, then their V_{BE} mismatch is approximately equal to 2.6mV at room temperature. Another important observation is that the offset voltage *varies* with temperature; i.e., if it is corrected at one temperature, it may manifest itself at another. It should be mentioned that equation (2.1) does not include base and emitter resistance mismatch, errors that become increasingly noticeable as devices scale down and are biased at relatively high current densities.

The overall input-referred offset can then be written as

$$V_{\mathrm{OS}} = V_T \ln \frac{\Delta A_{34}}{A_{34}} + V_T \frac{\Delta R_L}{R_L} + \frac{1}{g_{m34}R_L} V_T \ln \frac{\Delta A_{56}}{A_{56}}. \tag{2.2}$$

The last term in this equation is negligible if $g_{m34}R_L \gg 1$.

The comparator input-referred noise consists primarily of the thermal and shot noise of Q_3 and Q_4 and the thermal noise of R_{L1} and R_{L2} (neglecting the latch noise). The spectral density of this noise is

$$\frac{\overline{v_n^2}}{\Delta f} = 8kT\left(r_{b34} + r_{e34} + \frac{1}{2g_{m34}}\right) + \frac{8kT}{g_{m34}^2 R_L}, \tag{2.3}$$

where r_{b34} and r_{e34} denote base and emitter resistance, respectively, and all the noise components are assumed to be uncorrelated.

Equations (2.2) and (2.3) reveal a number of trade-offs in the design of this comparator. First, to reduce the input offset and r_{e34}, the emitter area of Q_3-Q_4 must increase, thereby increasing the input capacitance. Second, to reduce r_{b34}, the emitter width must increase, again raising the input capacitance. Third, to increase g_{m34}, the bias current must increase, thus increasing the power dissipation. Finally, if R_L is increased, the time constant at the output nodes increases and so does the voltage drop across R_{L1} and R_{L2}, thus limiting the input voltage swing. Note that the voltage drop across R_{L1} and R_{L2} should not exceed approximately 300 mV if Q_5 and Q_6 are to remain out of heavy saturation in the latching mode.

In order to study the comparison rate of the circuit shown in Figure 2.1, the overdrive recovery test which is often used as the most stressful assessment of comparator performance is described here. In this test, the input difference toggles between full-scale value V_{FS} and 1 LSB in consecutive clock cycles, yielding the waveforms depicted in Figure 2.2. For a large $\Delta V_{in} = V_{in1} - V_{in2}$ (or "overdrive"), the input pair of Figure 2.1 switches completely, steering all of the bias current to one side and producing a large V_{out} (which is $V_{out2} - V_{out1}$). When ΔV_{in} goes from full-scale to 1

LSB, V_{out} must "recover" from a large value and become approximately equal to $g_{m34}R_L \times 1$ LSB before the latch is strobed. It is noted from Figure 2.2 that overdrive recovery has two extreme cases. In the first case, ΔV_{in} goes from $-V_{FS}$ to +1 LSB and the output must recover and change polarity. In the second case, ΔV_{in} goes from $-V_{FS}$ to –1 LSB and the output must recover but not change polarity; i.e., it must be free from overshoot. In the first case, if V_{out} has not changed its polarity before the latch is activated, the latched output will regenerate to its previous value; i.e., the comparator tends to follow residues left from the previous cycle. This phenomenon is called "hysteresis" and results from insufficient time allowed for overdrive recovery.

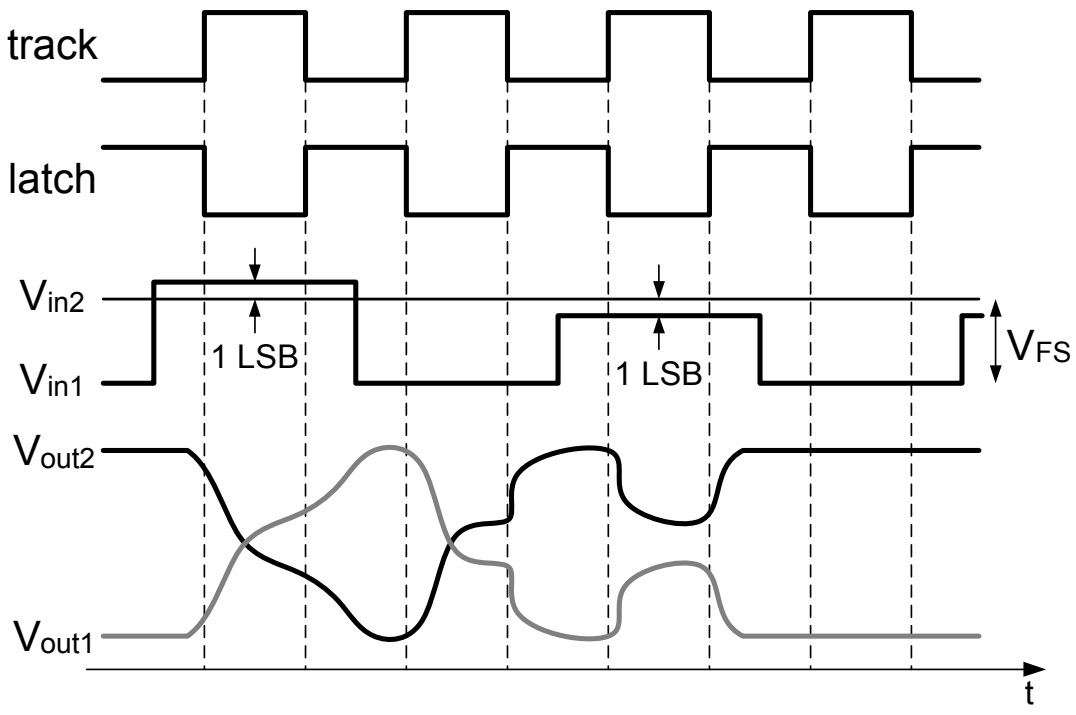


Figure 2.2: Comparator overdrive test

From the above discussion, it can be concluded that, in order for a comparator to respond correctly in an overdrive recover test, the minimum clock period must allow two phenomena to complete: overdrive recovery in the preamplifier and generation of

logic levels after the latch is strobed. In the circuit of Figure 2.1, the preamplifier overdrive recovery can be express as

$$V_{\text{out,ov}} = g_{m34}R_L V_{\text{LSB}} + \left(V_{CC} - I_{bias}R_L - g_{m34}R_L V_{\text{LSB}}\right)\exp\frac{-t}{R_L C_{\text{ov}}}, \tag{2.4}$$

where C_{ov} is the average capacitance at the two output nodes during overdrive recovery (consisting of the collector-base and collector-substrate capacitance of Q_3-Q_6 and the base-emitter junction capacitance of Q_5 and Q_6). The regeneration can be expressed as

$$V_{\text{out,reg}} = V_{\text{out,0}}\exp\frac{\left(g_{m56}R_L - 1\right)t}{C_{\text{reg}}}, \tag{2.5}$$

where $V_{\text{out,0}}$ is the difference between V_{out2} and V_{out1} when regeneration begins and C_{reg} is the average capacitance at the two output nodes during regeneration (consisting of C_{ov} and the base-emitter diffusion capacitance of Q_5 and Q_6) [2].

The dynamic range of the comparator is given by the ratio of the maximum input swing (which if exceeded, the signal will be clipped or saturated) and V_{LSB}. The maximum allowable differential input voltage is determined by the input common mode range. So the dynamic range can be calculated by noting that the input common-mode level $V_{\text{in},CM}$ is limited as follows:

$$2V_{\text{BE}} + V_{Sbias} \le V_{\text{in},CM} \le V_{CC}, \tag{2.6}$$

where V_{Sbias} is the minimum voltage required across the current source I_{bias} and it is assumed that $I_{bias}R_L \le 300$ mV so that Q_3 and Q_4 do not saturate heavily when the input common-mode level reaches V_{CC}.

Another important property of comparators is their kickback noise. Figure 2.3 illustrates how this noise is generated. Suppose the circuit is in the latching mode; i.e., the input pair is off. In the transition to tracking, *CLK* goes high and turns Q_1 on, pulling current from Q_3 and Q_4. However, since Q_3 and Q_4 are initially off, this current

first flows through their base-emitter junction, giving rise to a large current spike at V_{in1} and V_{in2}. The magnitude of this current is approximately equal to half I_{bias} before Q_3 and Q_4 turn on and provide current gain. The duration of this spike depends on the time constant at the input and may extend from one cycle to the next, thereby corrupting the analog input. For example, if I_{bias} = 200 μA, in an 8-bit flash ADC which has 256 comparators the kickback noise amplitude may reach tens of milliamperes. This noise can take a long time to decay to below 1 LSB.

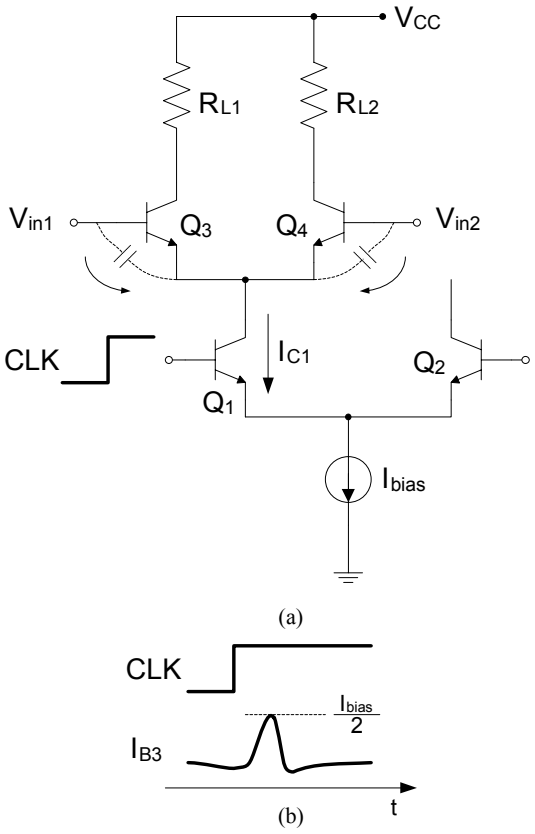


Figure 2.3: Generation of kickback noise in a bipolar comparator

The comparator of Figure 2.1 exhibits a nonlinear input capacitance as a function of the input difference, as illustrated in Figure 2.4. If V_{in1} is more negative than V_{in2} by several V_T, Q_3 is off and the input capacitance is equal to $C_{jc,3} + C_{je,3}$ (for input frequencies much less than f_T of transistors, so that the impedance seen at the emitter of Q_4 is small). As V_{in1} approaches V_{in2}, Q_3 turns on, introducing a base-emitter

diffusion capacitance $C_D = g_m\tau_F$, where τ_F is the base transit time. If V_{in1} exceeds V_{in2} by several V_T, Q_4 turns off and Q_3 operates as an emitter follow. In this region, the input capacitance is approximately equal to $C_{jc,3}$ plus a small fraction of $C_{je,3} + C_D$ and increases with V_{in1} because $C_{jc,3}$ experiences less reverse bias. In a flash ADC, for a given input voltage most of the comparators operate in either region 1 or 3, with only a few in region 2. As a result, the converter's input capacitance arises primarily from C_{jc} and C_{je} of the transistors (and interconnect capacitance). Due to the low-pass filter formed by the signal source resistance and the ADC input capacitance, the variation of input capacitance with the input voltage causes input-dependent delay and hence harmonic distortion [1].

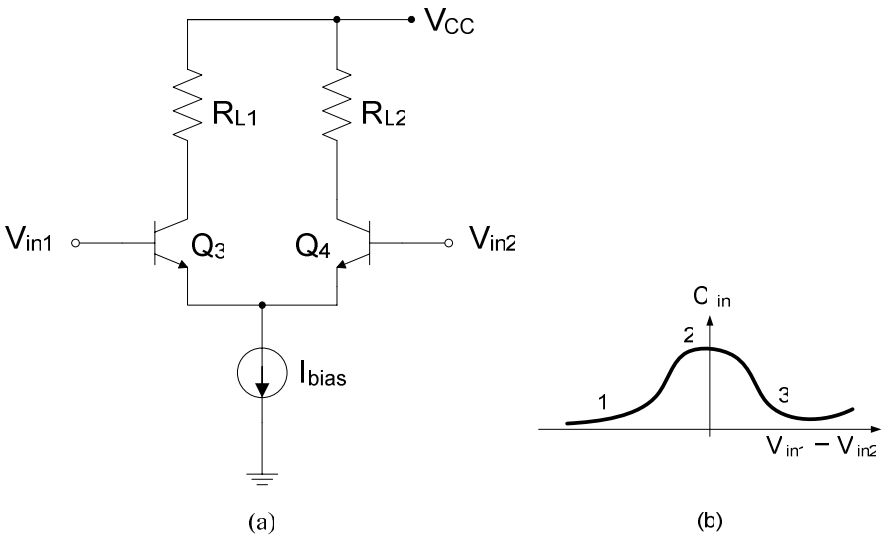


Figure 2.4: (a) Input stage; (b) small-signal input capacitance versus differential input

Another important parameter of the comparator of Figure 2.1 is its input bias current. In the tracking mode, this current varies between zero and I_{bias}/β as the input difference changes, and in the latching mode, it is zero. In a flash converter, the input bias current of comparators introduces a nonlinear variation in the reference ladder tap voltages [1], which can be considered as kickback noise and should be taken care.

The limitations described above for the comparator of Figure 2.1 can be significantly relaxed through the circuit design and optimization. In particular, the input differential pair can be preceded with another stage to suppress kickback noise and provide more gain, while the latch can employ emitter followers to enhance the regeneration speed and allow larger voltage swing.

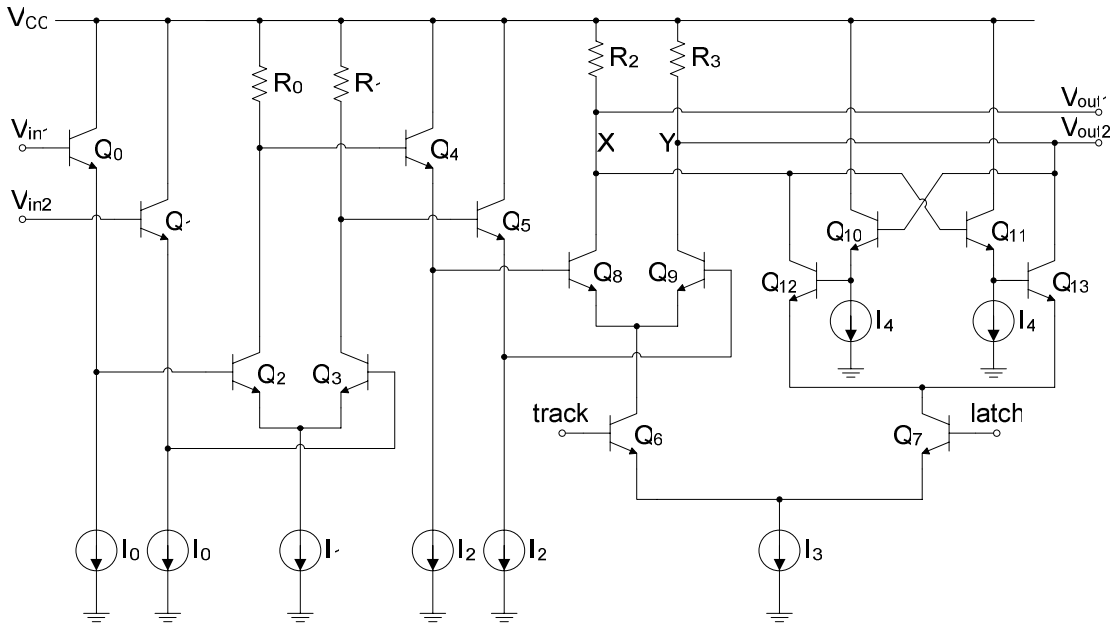


Figure 2.5: Improved bipolar comparator design

Shown in Figure 2.5 is a comparator circuit often utilized in flash ADCs [5]. It consists of an input stage, a switched differential pair, and a latch comprising Q_{10}-Q_{13}. The input stage serves the following purposes: (1) it suppresses the kickback noise to acceptably low levels; (2) it provides a relatively high gain, thereby lowering the offset contributed by the latch and improving metastability behavior; (3) it exhibits less input capacitance and less feedthrough from one input to the other; (4) its input bias current is relatively constant and can be canceled if necessary. These merits are attained at the cost of larger power dissipation, complexity, and some reduction in small-signal bandwidth. Note that the input offset voltage of the input stage is higher than that of a

simple differential pair because the V_{BE} mismatch of Q_0-Q_3 appears directly at the input. By the same token, the input noise is larger as well.

The emitter followers Q_{10} and Q_{11} used in the latch section of Figure 2.5 improve the performance in several ways. First, they reduce the loading effect of the parasitic capacitances of Q_{12} and Q_{13} on nodes X and Y, thus enhancing both the small-signal bandwidth and the regeneration speed. Second, they allow larger voltage swings at nodes X and Y because, unlike the circuit of Figure 2.1, the regeneration pair does not enter saturation for swings as large as V_{BE}. Third, they provide a low output impedance for driving the following stage.

In order to increase the input dynamic range, emitter followers Q_0 and Q_1 can be removed from the input stage, and the maximum voltage drop across R_0 and R_1 can be limited to a few hundred millivolts. In this way, the input common-mode level can vary between V_{CC} and $V_{BE} + V_{I1}$, yielding a wider input range. The input offset and noise will be less as well. Such a circuit, however, exhibits larger analog input feedthrough and variable input bias current.

2.2 Review of High-Speed Flash ADC Design

As is generally known, flash architectures are typically the simplest and the fastest structures that can be used to implement ADCs. The block diagram of a flash ADC has been shown in Figure 1.3 and a brief introduction has also been given in Section 1.2. Due to its high power consumption, this architecture normally is only used to implement converters with a resolution less than or equal to 6 bits.

Flash ADC is used for very high-speed conversion and its performance is dominated by matching issues. The correct operation of a flash ADC depends on the

accurate definition of the reference voltages sensed by each comparator. These reference voltages are compared with the input, but due to comparator offset voltages this comparison is not exactly equal to the reference level. Since the comparator offset voltage is a random variable which depends on the matching properties of the used technology, it directly influences the differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics of the ADC. Therefore, the first step in the design of a flash ADC consists in deriving an offset voltage standard deviation that guarantees with a high probability that the design complies with a certain performance specification or high yield or

$$\sigma_{\text{offset}} \leq \lambda \times \text{lsb} \tag{2.7}$$

with λ a constant depending on the resolution and the wanted yield percentage and the least significant bit of the converter.

The bit accuracy that can be achieved is proportional to the matching of the transistor. To improve the system accuracy, larger devices are required, but at the same time the capacitive loading of the circuit nodes increases and more power is required to attain a certain speed performance. In [6], the authors derived the following equation

$$\frac{\text{Speed} \times \text{Accuracy}^2}{\text{Power}} \approx \frac{1}{C_{ox} A_{Vt}^2} \tag{2.8}$$

where C_{ox} is the gate capacitance per unit area and A_{Vt} is a mismatch parameter of the technology used. This relationship implies that, for the circuits of today which aim high speed, high performance or accuracy, and low-power drain, a technological limit is encountered, namely the mismatch of the devices. This means that for a given technology, if high speed and high accuracy is required, this can only be achieved by consuming power. For example, if one bit extra accuracy is required in the design of

ADC, the power drain for the same speed performance will increase with a factor of four.

The authors in [6] discussed the actual trend of MOS parameters relevant to ADC design. Although the technology used in this thesis is HBT, it is worth mentioning the important results from [6] which are for CMOS technology since the basic design principles are the same. To determine the impact of scaling on the speed-power-accuracy tradeoff, they first discussed three scaling trends, namely the mismatch scaling, the supply voltage scaling and the relatively increasing importance of parasitic capacitances.

To reduce the short channel effects in deep submicron transistors, the oxide thickness is scaled down together with the minimum transistor length. The threshold mismatch parameter A_{Vt} decreases as technology scales down. The gate-oxide capacitance, on the other hand, increases when technology scales down (inversely proportional with the oxide thickness). Nevertheless, $C_{ox}A_{Vt}^2$ decreases as technology scales down and as a result the tradeoff becomes better. This means that, e.g., for the same speed and accuracy, less power is needed when technology is scaled down. For present-day processes the impact of the V_t mismatch is dominant.

To reduce the short channel effects in submicron CMOS transistors, the maximum supply voltage is scaled down together with the oxide thickness. Usually, the input range of the ADC is made as large as possible. Therefore, the least significant bit of the converter scales down together with the supply voltage, leading to a smaller allowable mismatch. Consequently, the scaling advantage for the tradeoff with smaller technology line-widths is reduced.

Also the impact of parasitic capacitances is very important and does not scale down with the downscaling of technology. So the impact of V_{DD}, A_{Vt}, and parasitic capacitance scaling is summarized as follows:

- Case 1: Supply voltage scaling and Drain-bulk capacitance scaling: because of the increasing matching demands the downscaling of the supply voltage is no longer compensated and so a straight line is the conclusion for power consumption.
- Case 2: Identical as Case 1 but now the drain-bulk capacitance scaling is not included: the extra load on the driver transistors leads to a slightly increasing straight line for power consumption.
- Case 3: No supply voltage scaling and drain-bulk capacitance scaling: the increasing matching properties lead to a decreasing power consumption of the implemented converter.

To conclude, the expected power-decrease is counteracted by the more stringent mismatch demand and the relatively increasing drain-bulk capacitance.

When technology scales further (for an $l_{\min}$ of 0.12 μm and a gate-overdrive voltage of 0.2 V), the β-mismatch is dominant. This makes the case even worse, power increases approximately linearly with downscaling. The reduced signal swing (and thus increased matching demand) is no more compensated by the increased matching of the technology.

Therefore, without extra precautions, technology scaling will increase the power consumption of high-speed ADCs in the future. To circumvent this power-

increase, modifications have to be found. From a general point of view, this can be done on three levels: system level, architectural level, and technology level.

- Technological Modifications: More effort may be spent at extensive research to achieve much better mismatch parameters in future technologies. Another technological adaptation is the use of dual oxide processes which can handle the higher supply voltages necessary to achieve the required dynamic range in data converters.
- System Level: Good system level design can substantially decrease the needed performance of the data converter in the system. High level design decisions can have a huge impact on the speed-power-accuracy of the ADC. This high level design needs behavioral models, including power estimators.
- Architectural Level: Analog preprocessing techniques reduce the input-capacitance of the flash ADC and the number of preamplifiers. Examples are interpolating (voltage/current), folding. These techniques do not really improve the speed-power-accuracy tradeoff; they only decrease the input capacitance (limiting the highest input frequency) and the number of preamplifiers or comparators. Averaging is a technique which reduces the offset specification for high-speed ADCs without requiring larger transistors areas. This technique makes a tradeoff between the improvement in DNL/INL and the gain of the preamplifier. An improved version of this technique is presented in [7] where the improvement in DNL/INL only depends on the number of stages which contribute the averaging. Averaging can be seen as taking the average value of neighboring node-voltages and thereby reducing the offset demand. The offset of the averaged value is equal to the original offset divided by the square root of the number of values one has averaged. The latest published high-speed 6-b

converters use this technique to reduce the input referred offset of the preamplifiers and comparators [7]–[9].

With the technologies nowadays, flash ADCs using CMOS technology can also work in gigahertz range. Several such works have been published and some of them will be reviewed here. These ADCs work with resolution of 5 bits or 6 bits and clock frequency above 1 GHz and normally below 2 GHz.

The ADC reported in [7] has a resolution of 6 bits without auto-zero or self-calibration, and it digitizes a 630 MHz input with a linearity of 5.5 effective bits at 1 GSample/s, and a 650 MHz input with 5 effective bits at 1.3 GSample/s. This ADC uses resistor averaging in two places to filter out random mismatch between arrays of differential pairs, substantially improving the accuracy of small MOSFETs which bias at a small current and present low input capacitance. The first resistor averaging is placed between the differential preamplifiers and the comparators to lower the effect of FET mismatch in the preamplifiers. Since the low voltage gain of 3 in the single-stage preamplifier required for wideband operation is insufficient to suppress random offsets due to the regenerative comparators, the outputs of the sense amplifier array driving latches in the comparators are averaged as well. The ADC occupies 0.8 mm^2 active area fabricated in a 0.35 μm CMOS 4-metal process. Excluding output buffers, it consumes about 500 mW from 3.3 V at 1 GHz conversion rate, and 545 mW at 1.3 GHz. The logic circuits and clock buffers consume half the power. At 1 GSample/s, INL and DNL are below ±0.3 LSB. The ADC dynamic performance shows an effective resolution bandwidth exceeding Nyquist input frequency, and flat reconstructed SNDR and SFDR (Spurious-Free Dynamic Range) up to 1.3 GHz conversion rate.

The ADC presented in [8] achieves a maximum sample rate of 1.1 GSample/s and an effective resolution bandwidth (ERBW) of 450 MHz. This result is obtained with full flash interpolating/averaging architecture with distributed track-and-hold in a standard 0.35 μm single-poly five-metal 3.3 V digital CMOS process. Amplification, interpolation and averaging are applied to relieve comparators offset requirements such that a fast design can be achieved. The comparator consists of a folded cascode input stage and a latch followed by a level shifter and a flip-flop to force clear decision. The transistors in the comparator are chosen small for high-speed operation. This ADC works with ENOB of 5.65b and consumes 300 mW at 900 MSample/s. DNL and INL are both less than 0.7 LSB and the ADC area is 0.3 mm^2.

In [9], the averaging technique is also used. The authors discussed the shift of the output zero crossings due to the averaging resistors. They introduced a way to solve the problem by redefining the edge averaging resistors. This flash ADC has a resolution of 6 bits built in 0.18 μm CMOS. The ADC with all decoupling capacitance, in total 60 pF, is positioned inside 300 × 400 μm^2 active area. A typical sample has a 0.42 LSB INL showing the device mismatch to be dominant. The sample rate approaches 1.6 GSample/s. The ADC achieves 5.7 ENOB at DC while maintaining a performance of 5.0 ENOB up to 660 MHz signal frequency, measured at 1.5 GSample/s. The ADC consumes 328 mW with 1.95 V analog and 2.25 V digital supply when used at 1.5 GSample/s. At the 1.6 GSample/s the digital supply is set at 2.35 V, increasing the power consumption by 12 mW. Together with the measured values of ENOB and ERBW, the compared figure-of-merit, $P/(2^{ENOB} \cdot 2 \cdot ERBW)$, for this ADC yields a state-of-the-art lower limit of 4.8 pJ per conversion step.

The flash ADC presented in [10] uses an analog power supply of only 1.8V. The maximum sampling speed is 1.3 GHz. The SNDR at 133 kHz is 33.2 dB, and the SNDR at 500 MHz is 32 dB. The total power consumption of the converter at full speed is 600 mW and the total active area is only 0.13 mm^2. The ADC is implemented in a 0.25-μm pure digital CMOS technology. The output pole preamplifier and comparator speed are optimized for high performance. It has also been shown that low-voltage design of high-speed ADCs is feasible in deep-submicron CMOS technologies.

A 4 GSample/s 6-bit flash ADC with 8-bit output is presented in [11] and it is realized in a 0.13μm standard CMOS technology. The outputs of 255 small-area comparators with comparatively large input offsets are averaged by a fault tolerant thermometer-to-binary converter. The ADC uses an on-chip low jitter VCO for clock provision and consumes 990 mW at a single supply voltage of 1.5 V. DNL of the ADC is –0.23/+0.91 LSB and INL is –0.98/+1.2 LSB. The chip area is 4.6 mm^2 and the active area is 0.5 mm^2.

The authors present a 6-bit 1.2-GSample/s flash-ADC with wide analog bandwidth and low power, realized in a standard digital 0.13μm CMOS copper technology in [12]. Employing capacitive interpolation gives various advantages when designing for low power: elimination of a reference resistor ladder, implicit sample-and-hold operation, no edge effects in the interpolation network (as compared to resistive interpolation), and a very low input capacitance of only 400 fF, which leads to an easily drivable analog converter interface. Operating at 1.2 GSample/s the ADC achieves an effective resolution bandwidth (ERBW) of 700 MHz, while consuming 160 mW of power. At 600 MSample/s the ADC can work with an ERBW of 600 MHz with only 90 mW power consumption, both from a 1.5 V supply. This corresponds to

outstanding figure-of-merit numbers (FoM) of 2.2 and 1.5 pJ/convstep, respectively. The module area is 0.12 mm^2.

As discussed in Section 1.4, SiGe HBT technology is a proven technology to provide very high-speed integrated circuit design. It is well suited to design ICs above 10 GHz. Therefore, flash ADCs designed using this technology can also operate in a very high-speed. Here, two flash ADCs presented in [13] and [14] and a folding-interpolating ADC presented in [15] using SiGe HBT technology are introduced.

Presented in [13] is a 5-b flash A/D converter developed in a 0.18-μm SiGe BiCMOS that supports sampling rates of 10 GSample/s. The ADC is optimized to operate in digital equalizers for 10-Gb/s optical receivers, where the ADC has to deliver over three effective number of bits at Nyquist. A fully differential flash ADC incorporating a wide-band track-and-hold amplifier, a differential resistive ladder, an interpolation technique, and a high-speed comparator design is devised to resolve the aperture jitter and metastability error in this paper. The ADC achieves better than 4.1 effective bits for lower input frequencies (950 MHz) and three effective bits for Nyquist input (4.8 GHz) at 10 GSample/s. The ADC dissipates about 3.6 W at the maximum clock rate of 10 GSample/s while operating from dual –3.7/–3 V supplies and occupies 3 × 3 mm^2 of chip area.

In [14], a 4-bit flash-type ADC with pipelined encoder has been implemented in a SiGe bipolar technology for very high-frequency mixed-signal applications. This chip is fully functional at 8 GSample/s. Maximum input bandwidth is 4 GHz based on beat frequency measurements. Both DNL and INL are within 0.25 LSB. The chip includes over 1000 transistors and consumes 500 mW at 3.6 V. The SiGe technology used here offers 0.5 × 2.5 mm^2 npn devices with f_T and f_{max} in excess of 45 GHz and 60

GHz at 1 mA collector current, respectively. Current gain exceeds 100 and the Early voltage is 60 V. High-speed GaAs ADCs usually consume several Watts. In contrast, SiGe HBT technology offers a better solution since the device has a lower turn-on V_{be} of less than 0.9 V. This allows a lower supply voltage and hence reduces chip power consumption. Furthermore, the technology uses a silicon substrate that offers higher thermal conductivity. These attributes make the high-speed SiGe HBT technology very attractive for ADC design. The ADC has 15 comparators and a 2 pF decoupling capacitor is added in each comparator to filter out the high-frequency cross coupling. The comparator sensitivity is less than 2 mV.

The work in [15] deals with the design and implementation of an 8-bit, 2-GSample/s folding-interpolating ADC using a 0.5-μm SiGe technology with a unity gain cut off frequency f_τ of 47 GHz. The converter occupies an area of 3.5 × 3.5 mm^2 including pads and exhibits a better than 7-bit ENOB for an input signal frequency up to 500 MHz and a sampling rate of 2 GSample/s. The maximum value of DNL and INL are 0.6 and 1 LSB respectively. The power dissipation of the ADC is 3.5 W using a –3.3 V power supply. This high-speed, high-resolution ADC has applications in direct IF sampling receivers for wideband communication systems. The comparators consist of a 2-stage preamplifier and a latch. Such a comparator architecture suppresses the kickback noise to an acceptably low level and provides a relatively high gain, which in turn lowers the offset contributed by the latch, and therefore improves the metastability behavior of the comparator.

Based on above literature research, the flash ADC presented in this thesis will achieve resolution of 5 bits and sampling rates of 6 GSample/s using a 0.35-μm SiGe BiCMOS process. The ADC can be used in the area of UWB Communications which

requires high sampling speed circuit. A fully differential flash ADC incorporating a wide-band track-and-hold amplifier, a differential resistive ladder, an interpolation technique, and a high-speed comparator design is devised to resolve the aperture jitter and metastability error. The analog part of the flash ADC will operate from a single 3.3 V power supply. The thermometer-to-binary encoder is used as the last stage of the flash ADC to convert the output from the comparator array to digital output. Gray code is used as the intermediate step to enhance encoding performance.

CHAPTER 3

HIGH-SPEED COMPARATOR DESIGN

3.1 Analysis of Basic Single-Stage BJT Amplifiers

In this section, a brief introduction of two basic configurations of BJT amplifiers, namely the common-emitter and the common collector amplifiers, will be given. These two configurations are very basic to BJT integrated circuits design and will be used a lot in this thesis. Before starting analysis of these two types of amplifiers, the relationships between the small-signal model parameters of the BJT are shown in Table 3.1 for further reference.

Table 3.1: Relationships between the small-signal model parameters of the BJT

Model parameters in terms of DC bias currents:		
$g_m = \frac{I_C}{V_T}$	$r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right)$	
$r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right)$	$r_o = \frac{V_A}{I_C}$	
Model parameters in terms of g_m:		
$r_e = \frac{\alpha}{g_m}$	$r_\pi = \frac{\beta}{g_m}$	
Model parameters in terms of r_e:		
$g_m = \frac{\alpha}{r_e}$	$r_\pi = (\beta+1) r_e$	$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$
Relationships between α and β:		
$\beta = \frac{\alpha}{1-\alpha}$	$\alpha = \frac{\beta}{\beta+1}$	$\beta + 1 = \frac{1}{1-\alpha}$

3.1.1 The Common-Emitter Amplifier

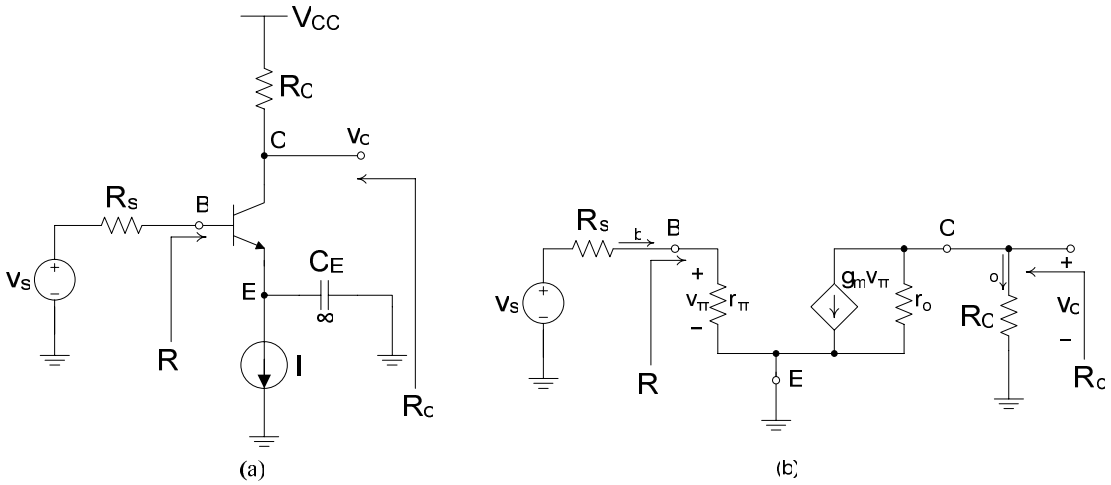


Figure 3.1: The common-emitter amplifier with its hybrid-π model

Figure 3.1(a) shows the basic configuration of the common-emitter amplifier. The BJT is biased with a constant-current source I that is assumed to have a high output resistance (a few hundred KΩ). A capacitor C_E connects the emitter to ground. Its capacitance is assumed to be sufficiently large so that its reactance is negligibly small at all signal frequencies of interest. Typical value of C_E can be in the range of pF for high frequency signals. Thus C_E in effect short-circuits the emitter to ground as far as signals are concerned. Correspondingly, a signal ground is established at the emitter, and signal current flows through C_E to ground bypassing the output resistance of the current source I. Capacitor C_E is therefore called a bypass capacitor. Here the load resistor R_L is not shown and is merged into R_C.

The BJT shown in Figure 3.1(a) is replaced with its hybrid-π model shown in Figure 3.1(b) where the DC sources are eliminated. By using the equivalent circuit, the common-emitter amplifier can be analyzed to determine its input resistance R_i, voltage gain v_o/v_s, current gain i_o/i_b, and output resistance R_o.

Examination of the circuit in Figure 3.1(b) reveals that the input resistance R_i is given by

$$R_i = r_\pi . \tag{3.1}$$

The overall voltage gain A_v is

$$A_v \equiv \frac{v_o}{v_s} = -\frac{g_m r_\pi \left(R_C // r_o\right)}{R_s + r_\pi} = -\frac{\beta \left(R_C // r_o\right)}{R_s + r_\pi} . \tag{3.2}$$

From equation (3.2), it can be noted that if $R_s \gg r_\pi$, the gain will be highly dependent on the value of β. This dependence decreases for lower values of R_s, and in the extreme, for $R_s \ll r_\pi$, the gain is independent of β, becoming

$$A_v \cong -g_m \left(R_C // r_o\right). \tag{3.3}$$

For discrete circuits, R_C is usually much lower than r_o, and r_o can be eliminated from the preceding expressions. However, this is usually not the case in the integrated-circuit amplifiers. For IC amplifiers, the interest will be normally in the maximum possible gain achieved in a common-emitter circuit, which can be found by setting $R_C = \infty$ (which can be achieved by using active loading) in equation (3.3) and the result is

$$A_{v\max} = -g_m r_o . \tag{3.4}$$

Substituting $g_m = I_C / V_T$ and $r_o = V_A / I_C$ from Table 3.1,

$$A_{v\max} = -\frac{V_A}{V_T}, \tag{3.5}$$

which is independent of the bias current I_C.

The current gain of the common-emitter amplifier is found from the circuit of Figure 3.1(b) to be

$$A_i \equiv \frac{i_o}{i_b} = \frac{-g_m v_\pi r_o / (r_o + R_C)}{v_\pi / r_\pi} = -\beta \frac{r_o}{r_o + R_C} . \quad (3.6)$$

For $R_C \ll r_o$, $A_i \cong -\beta$, which again explains that β is the common-emitter short-circuit (i.e., $R_C = 0$) current gain.

Finally, the output resistance R_o can be found by inspection of the circuit of Figure 3.1(b) as follows: setting $v_s = 0$, which results in $v_\pi = 0$, and thus

$$R_o = R_C // r_o . \quad (3.7)$$

To summarize, the common-emitter amplifier can be designed to provide substantial voltage and current gains, it has an input resistance of moderate value, and it has a high output resistance. In multistage high-gain amplifiers, the bulk of the voltage gain is usually realized using one or more common-emitter stages.

3.1.2 The Common-Collector Amplifier (Emitter Follower)

The common-collector amplifier is a very significant circuit that finds frequent application in the design of amplifiers, both small-signal and large-signal and even in digital circuits. The circuit is shown in its basic form in Figure 3.2(a). Here, the collector is connected to the positive supply V_{CC} and thus is at signal ground. The input signal is applied to the base, and the output is taken from the emitter. The most convenient way to analyze the common-collector amplifier is to use the T model for a bipolar transistor. Figure 3.2(b) shows the equivalent circuit of the common-collector amplifier with the BJT replaced with the T model augmented with the collector output resistance r_o. Noting from Figure 3.2(b) that r_o in effect appears in parallel with R_L, the circuit is redrawn in Figure 3.2(c) to make this connection more apparent and thus simplify the analysis.

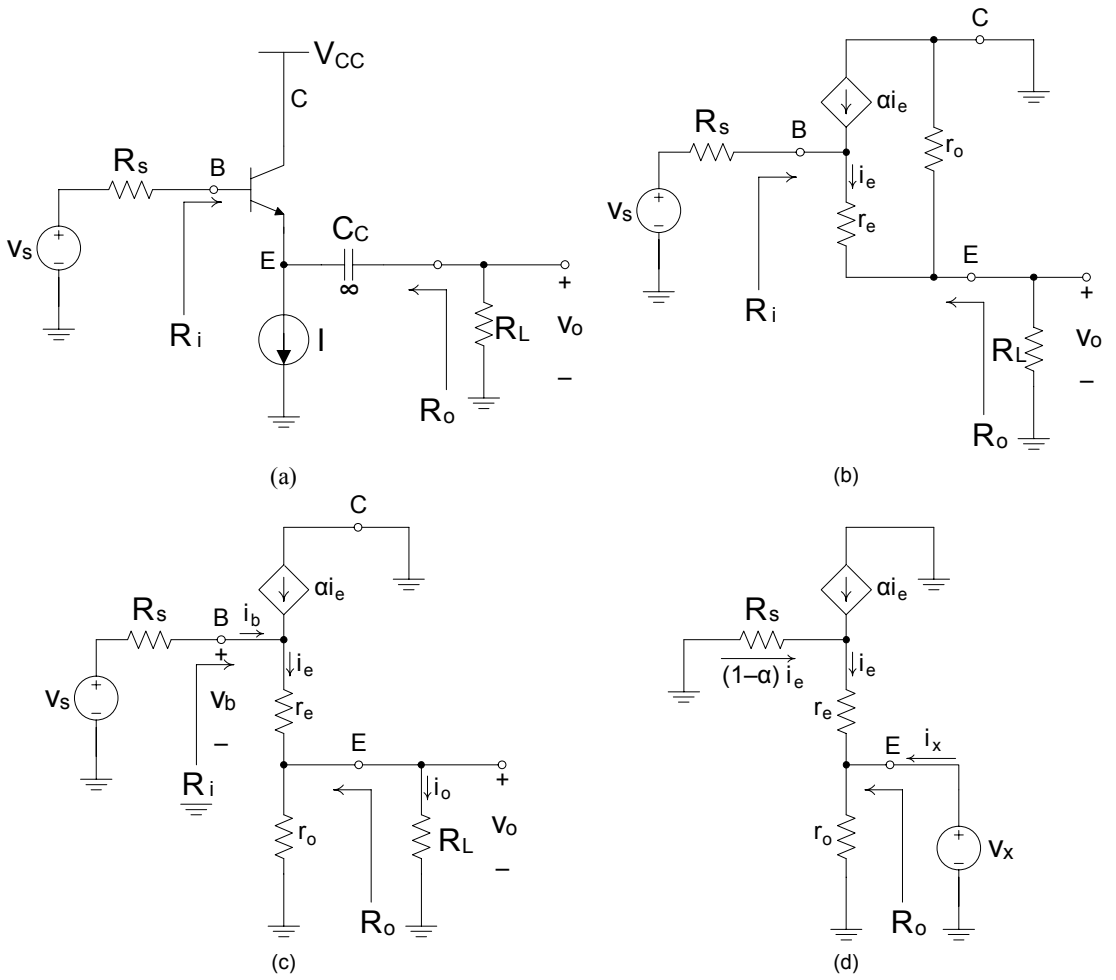


Figure 3.2: The common-collector amplifier with its T model and equivalent circuits

By doing some simple circuit analysis, the input resistance R_i can be obtained as

$$R_i \equiv \frac{v_b}{i_b} = (\beta+1)\left(r_e + (r_o \,//\, R_L)\right). \tag{3.8}$$

This is a very important result and it says that the input resistance looking into the base is $(\beta+1)$ times the total resistance in the emitter. Multiplication by the factor $(\beta+1)$ is known as the resistance-reflection rule. For the case $r_e \ll R_L \ll r_o$,

$$R_i \cong (\beta+1) R_L . \tag{3.9}$$

This equation illustrates an important characteristic of the common-collector amplifier: The amplifier exhibits a relatively large input resistance. Specifically, the effect on the

signal source of connecting a load R_L is reduced because R_L is in effect multiplied by $(\beta+1)$. The overall voltage gain can also be obtained from Figure 3.2(c) and expressed as

$$A_v \equiv \frac{v_o}{v_s} = \frac{(\beta+1)(R_L // r_o)}{R_s + (\beta+1)(r_e + (R_L // r_o))}, \tag{3.10}$$

which can be expressed in the slightly different form

$$A_v \equiv \frac{v_o}{v_s} = \frac{(R_L // r_o)}{\frac{R_s}{(\beta+1)} + r_e + (R_L // r_o)}. \tag{3.11}$$

Both equation (3.10) and equation (3.11) indicate that the voltage gain of the emitter follower is less than unity. The voltage gain, however, is usually close to unity, which is a result of the increase in the resistance seen by the signal source due to the multiplication by $(\beta+1)$.

The output resistance R_o of the emitter follower can be determined from the circuit shown in Figure 3.2(d), where v_s has been set to zero and a test voltage v_x is applied to the emitter. After doing some circuit analysis, R_o can be obtained as

$$\frac{1}{R_o} \equiv \frac{i_x}{v_x} = \frac{1}{r_o} + \frac{1}{r_e + (1-\alpha) R_s}.$$

Thus R_o is the parallel equivalent of r_o and $\left[r_e + (1-\alpha) R_s\right]$, or

$$R_o = r_o // \left[r_e + \frac{R_s}{\beta+1}\right], \tag{3.12}$$

where $1-\alpha = 1/(\beta+1)$ is substituted. Examination of equation (3.12) reveals that R_o is usually low. To complete the analysis of the emitter follower, its current gain can be shown as

$$A_i \equiv \frac{i_o}{i_b} = \frac{\left[r_o/(r_o + R_L)\right] i_e}{i_e/(\beta+1)} = (\beta+1)\frac{r_o}{r_o + R_L}, \tag{3.13}$$

which approaches $(\beta+1)$ for $R_L \ll r_o$.

In summary, the emitter follower exhibits a high input resistance, a low output resistance, a voltage gain that is smaller than but close to unity, and a relatively large current gain. It is therefore ideally suited for applications in which a high-resistance source is to be connected to a low-resistance load, namely, as a voltage buffer amplifier. Its low output resistance makes it also useful as the last stage or output stage in a multistage amplifier where its purpose would be not to supply additional voltage gain but rather to give the cascade amplifier a low output resistance.

The question of the maximum allowed signal swing of the emitter follower is discussed as follows. Since only a small fraction of the input signal appears between base and emitter, the emitter follower exhibits linear operation for a large range of input-signal amplitude. There is, however, an absolute upper limit imposed on the value of the output-signal amplitude by transistor cutoff. To see how this comes out, consider the circuit of Figure 3.2(a) when the input signal is a sine wave. As the input goes negative, the output v_o will also go negative, and the current in R_L will be flowing from ground into the emitter terminal. The transistor will cut off when this current becomes equal to the bias current I. Thus peak value of v_o can be found from $\frac{\hat{V}_o}{R_L} = I$ or $\hat{V}_o = IR_L$. The corresponding value of v_s will be $\hat{V}_s = \frac{IR_L}{A_v}$. Increasing the amplitude of v_s above this value results in the transistor becoming cut off, and the negative peaks of the output-signal waveform being clipped off.

3.2 Analysis of the BJT Differential Pair

The differential amplifier is the most widely used circuit building blocks in analog integrated circuits. For instance, the input stage of every operational amplifier is a differential amplifier. A brief introduction of the BJT differential pair is presented here.

3.2.1 Large-signal operation of the BJT differential pair

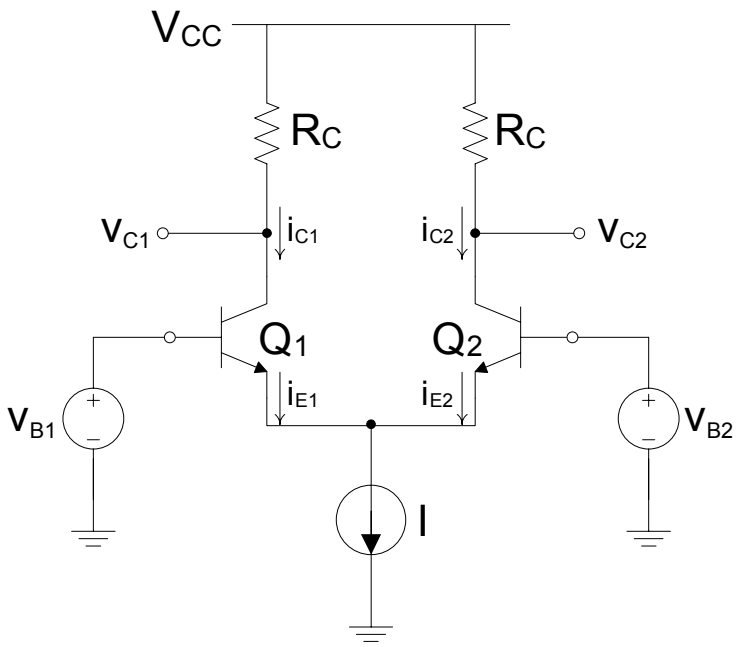


Figure 3.3: The basic BJT differential-pair configuration

Figure 3.3 shows the basic BJT differential-pair configuration. It consists of two matched transistors, Q_1 and Q_2, whose emitters are joined together and biased by a constant-current source I. By using bipolar I_C–V_{BE} equations and doing some mathematical manipulations, the following two equations can be obtained,

$$i_{E1} = \frac{I}{1+\exp\left[\left(v_{B2}-v_{B1}\right)/V_T\right]}, \tag{3.14}$$

$$i_{E2} = \frac{I}{1+\exp\left[\left(v_{B1}-v_{B2}\right)/V_T\right]}. \tag{3.15}$$

The collector currents i_{C1} and i_{C2} can be obtained simply by multiplying the emitter currents in equations (3.14) and (3.15) by α, which is normally very close to unity.

The fundamental operation of the differential amplifier is illustrated by equations (3.14) and (3.15). Note that the amplifier responds only to the difference voltage $v_{B1}-v_{B2}$. That is, if $v_{B1}=v_{B2}=v_{CM}$ where v_{CM} is the common-mode voltage, the current I divides equally between the two transistors irrespective of the value of the common-mode voltage v_{CM}. This is the essence of the differential amplifier operation.

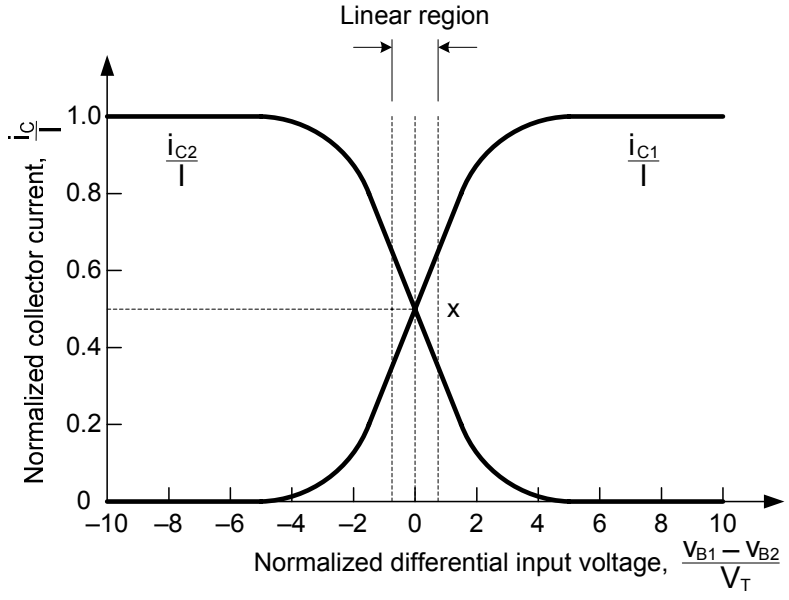


Figure 3.4: Transfer characteristics of the BJT differential pair

Another important observation is that a relatively small difference voltage $v_{B1}-v_{B2}$ will cause the current I to flow almost entirely in one of the two transistors. Figure 3.4 shows a plot of the two collector currents (assuming $\alpha \approx 1$) as a function of the difference signal. Note that a difference voltage of about $4V_T$ (≈ 100 mV) is sufficient to switch the current almost entirely to one side of the pair. The analysis of

the differential pair as a small-signal amplifier where the amplifier operates in a linear segment of the characteristics around the midpoint *x* in Figure 3.4 will be given in the next section.

3.2.2 Small-signal operation of the BJT differential pair

Figure 3.5 shows the differential pair with a difference voltage signal v_d applied between the two bases. It is implied that the DC level at the input has been established such that the transistors are operating in the active region. The input differential resistance and the differential voltage gain can be derived from the circuit.

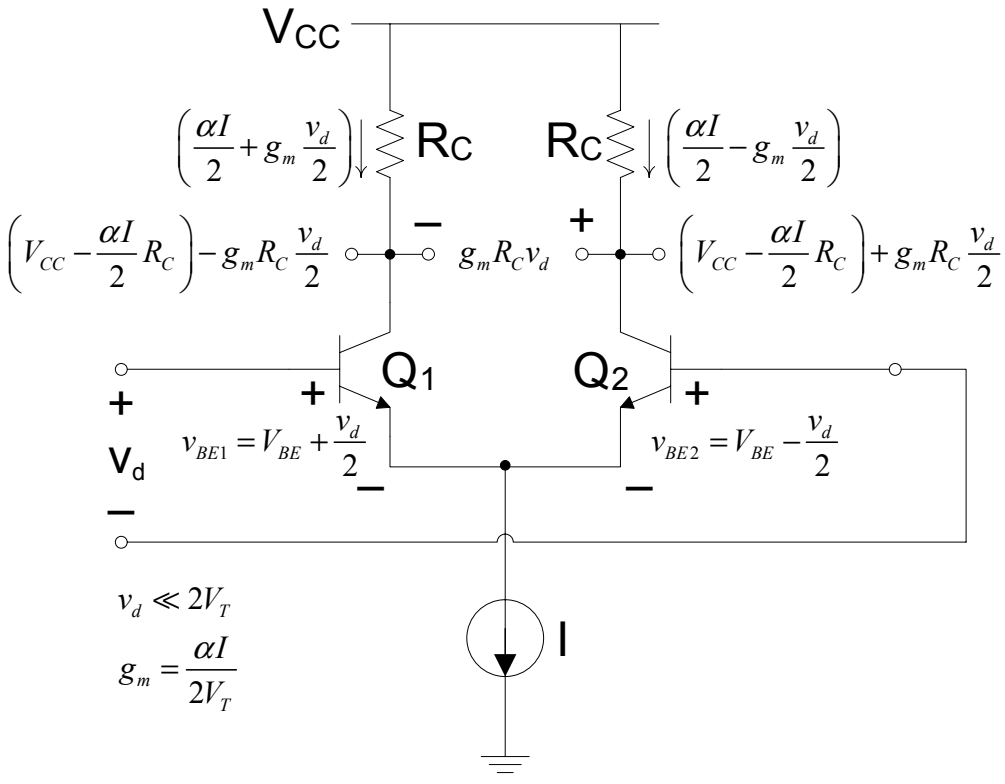


Figure 3.5: The currents and voltages in the amplifier with a small differential input

By doing some mathematical manipulations, the differential input resistance R_{id} is obtained as

$$R_{id} \equiv \frac{v_d}{i_b} = (\beta+1)2r_e = 2r_\pi \,. \tag{3.16}$$

The output voltage signal of a differential amplifier can be taken either differentially (that is, between the two collectors) or single-ended (that is, between one collector and ground). If the output is taken differentially, then the differential gain of the differential amplifier will be

$$A_d = \frac{v_{c1} - v_{c2}}{v_d} = -g_m R_C \,. \tag{3.17}$$

On the other hand, by taking the single-ended output (say, between the collector of Q_1 and ground), then the differential gain will be given by

$$A_d = \frac{v_{c1}}{v_d} = -\frac{1}{2} g_m R_C \,. \tag{3.18}$$

Here g_m denotes the transconductance of Q_1 and Q_2, which are equal and given by

$$g_m = \frac{I_C}{V_T} = \frac{\alpha I/2}{V_T} \,. \tag{3.19}$$

Thus, the differential gain by taking the single-ended output is half that by taking the differential output.

3.3 Design of a High-Speed Comparator

The functionality of a comparator has been described in Section 1.3 and the bipolar implementation of the comparator structure shown in Figure 1.5 has been given a detailed description in Section 2.1. To improve the metastability behavior so as to reduce the minimum input difference of the comparator, the master-slave structure is implemented in the design as shown in Figure 3.6. The input stage consisting of a preamplifier is used to suppress kickback noise which comes from the master comparator stage due to the back injection of stored base-emitter charge into base when Q_6-Q_7 are suddenly shut off and also reduces input-referred offset such that the minimum input difference is reduced. Emitter followers are used in both latches to

enhance the comparator performance as discussed in Section 2.1. The slave comparator is used which greatly reduces the resolvable minimum input difference. The resistances R_0-R_5 are carefully chosen such that the input referred offset and noise are kept low as seen from equations (2.2) and (2.3) and gains of the differential pair stages are not too low while maintaining low output nodes time constants and not affecting unity-gain bandwidth too much. All the transistors' sizes are also optimized to obtain best performance of the comparator design.

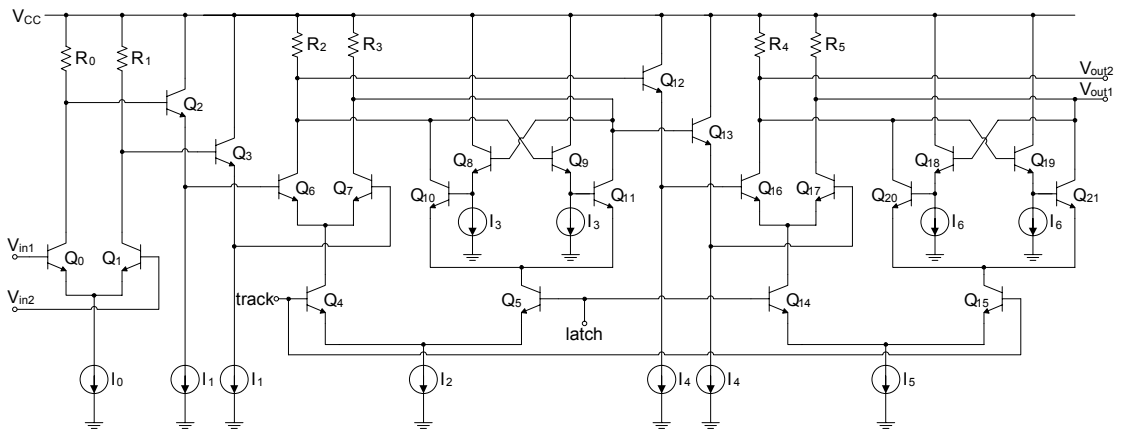


Figure 3.6: The high-speed master-slave comparator structure

High gain and wide bandwidth of the preamplifier are required to reduce the effect of mismatches and kickback noise in the latches and to reduce the recovery time. The preamplifier stage is a simple differential pair consisting of Q_0-Q_1 and R_0-R_1. It provides over 14 dB gain and a wide 3-dB bandwidth of 13 GHz. R_0 and R_1 are chosen to be small so that the time constant at the output is small. R_0 and R_1 are set to be 100Ω. Therefore, I_0 is 2.6mA according equations (3.17) and (3.19). So the gain is

$$A_p = g_m R = \frac{I_0}{2V_T} R = \frac{2.6}{2\times 25}\times 100 = 5.2\,. \tag{3.20}$$

Converting A_p to dB, it is $20\log(5.2) = 14.32\text{dB}$. Here to achieve wide bandwidth such that the preamplifier can operate in high-speed, the load of the preamplifier is

chosen to be small and thereby the current bias becomes large (i.e., large power dissipation). This is a tradeoff between speed and power dissipation. The AC response of the preamplifier is shown in Figure 3.7. Figure 3.8 shows the AC response around the 3-dB bandwidth frequency after zooming in Figure 3.7.

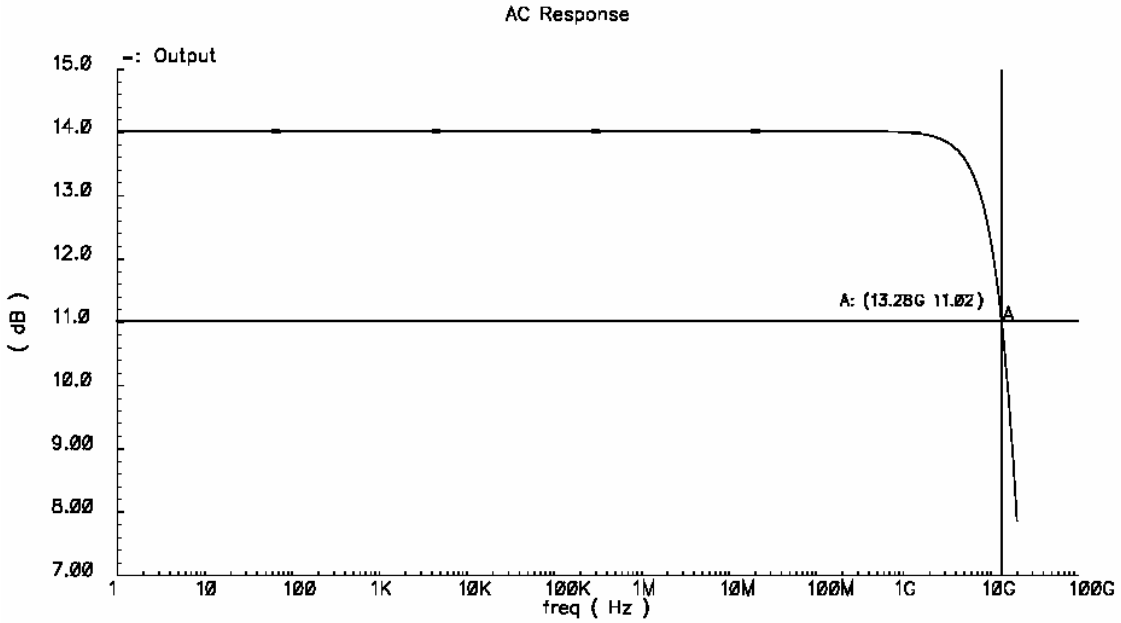


Figure 3.7: AC response of the preamplifier

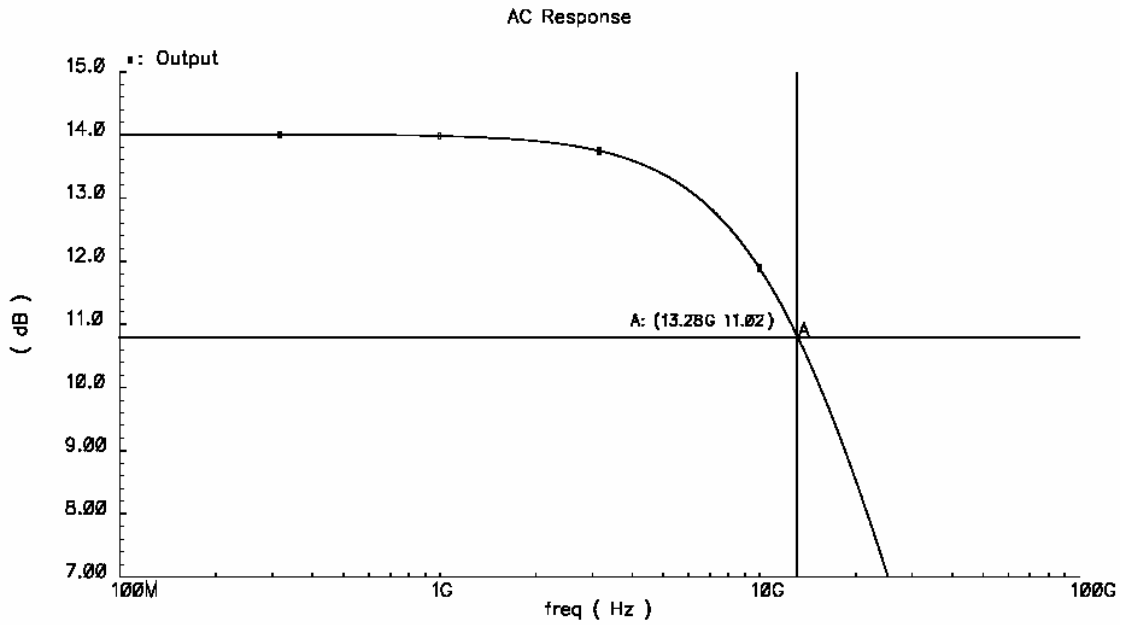


Figure 3.8: AC response of the preamplifier after zooming in

As shown in Figure 3.6, the structures of the master comparator and the slave comparator are the same as the basic bipolar comparator shown in Figure 2.1. Each one consists of a preamplifier and a latch. As discussed before, the comparator's metastability error is an important performance metric and it may cause erroneous decisions by the comparator and deteriorate the BER of the comparator. It is limited by the recovery time (t_{recovery}) of the preamplifier and the regeneration time constant (τ_{reg}) of the latch. Like the behavior of CMOS preamplifiers [7], the recovery time of an HBT preamplifier can be expressed by

$$t_{\text{recovery}} = -\frac{1}{2\pi f_{BW,PA}} \ln\left(1 - \frac{V_T}{\Delta V + V_T}\right), \tag{3.21}$$

where $f_{BW,PA}$ represents the bandwidth of a preamplifier, ΔV is the initial input voltage of the preamplifier, and V_T is the thermal voltage. With $\Delta V = 0.5$ LSB, the required bandwidth is greater than 10 GHz for a 10-ps recovery time.

The regeneration time constant of a latch is a function of the unity gain bandwidth of the amplifiers used in the latch and can be expressed in term of transistor parameters [16]

$$\tau_{\text{reg}} = \frac{C_{be}\left(r_b + R_L\right) + C_{bc}\left[4R_L + r_b\left(g_m R_L + 1\right)\right] + C_L R_L}{g_m R_L - 1}, \tag{3.22}$$

where g_m is the transconductance of latch devices, R_L is the load resistance, and C_{be}, C_{bc}, and r_b represent the device capacitances and base resistance, respectively. Note that τ_{reg} is dependent on the cut-off frequency (f_T) of the device employed. The probability of metastability error can be expressed by [2]

$$P_{\text{ME}} = \frac{2}{A_p} \frac{\Delta V_{\text{Logic}}}{I_{EE} R_L} \exp\left(-\frac{T_{\text{Logic}}}{\tau_{\text{reg}}}\right). \tag{3.23}$$

As the time duration (T_{Logic}) to a given logic level (V_{Logic}) is directly related to the decision cycle, the metastability probability is a function of sampling frequency and regeneration time constant.

Therefore, in order to lower the error probability, the circuit uses: 1) SiGe HBT devices with high f_T; 2) the smallest device size to ensure low capacitance; 3) an emitter coupled logic (ECL)-type latch with a small load resistance (R_L); 4) a high g_m latch at large bias current (I_{EE} or I_2, I_5 in Figure 3.6); 5) less than 300 mV output voltage swing; 6) a high gain of the preamplifier A_p; and 7) a master-slave-sensitive clocked comparator. The design of the comparator shown in Figure 3.6 considers all these factors.

The gain stage in the master/slave comparator provides another 5 dB gain during its track phase. This gain is relatively low in order to maximize speed. Note that since the unity-gain bandwidth $f_u = A_v \times f_{BW}$ is a constant, with the increase of the open-loop gain of the amplifier, its –3 dB cut-off frequency or its bandwidth decreases. Then from equation (3.21), t_{recovery} will increase, which means during the track phase it takes longer time for the preamplifier to recover from a logic value which is produced by the latch. This in effect will deteriorate the comparator performance.

The overall input-referred offset is shown by Equation (2.2) which is shown here again for easy reference,

$$V_{\text{OS}} = V_T \ln\frac{\Delta A_{6,7}}{A_{6,7}} + V_T \frac{\Delta R_{2,3}}{R_{2,3}} + \frac{1}{g_{m6,7}R_{2,3}} V_T \ln\frac{\Delta A_{10,11}}{A_{10,11}}. \tag{3.24}$$

The offset is induced by mismatch between nominally identical devices of Q_6-Q_7, Q_{10}-Q_{11} and R_2-R_3. From Equation (3.24), it is clear that with increase of those device sizes, the input-referred offset will decrease and also the increase of bias current through Q_6-

Q_7 decreases offset. This is the tradeoff of the high-speed comparator design. To increase the resolution of the comparator, the input-referred offset must decrease. However, the increase of device sizes will increase output node capacitance and resistance, which in effect will decrease the comparator speed due to increased time constant. Also, with the increase of the bias-current, the overall power consumption will become larger. The above statements again clearly expatiate on Equation (2.8).

The preamplifier stage formed by Q_0-Q_1 helps a lot in reducing input-referred offset. So R_2-R_3 can be set to relatively low value of 80 Ω and Q_6-Q_7, Q_{10}-Q_{11} are chosen to be relatively small size bipolar transistors such that the comparator speed can be promised.

Implemented in a 0.35-μm SiGe BiCMOS process, the comparator shown in Figure 3.6 consumes approximately 70mW with sampling speed of 16 GHz and resolvable minimum input voltage of 8mV peak-to-peak. This comparator also passes the overdrive recovery test. Detailed simulation results will be presented in Chapter 5.

3.4 High-Speed Comparator Design with a Modified Bias Scheme

Figure 3.9 shows the high-speed master-slave comparator design with a modified bias scheme. This bias scheme can give rise to the optimum bias condition in master-slave comparators in term of regeneration time constant and power dissipation.

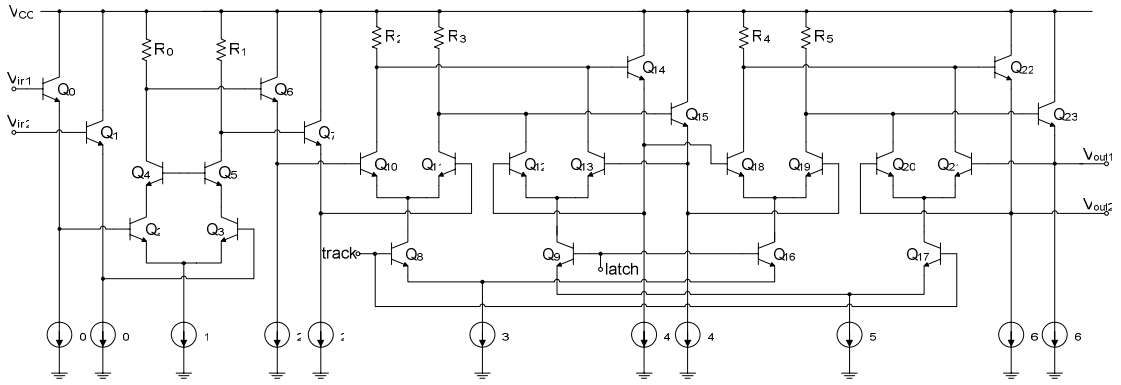


Figure 3.9: Master-slave comparator with a modified bias scheme

A comparator consists of a gain stage and a regenerative latch with clocked control. With the same bias current as in Figure 3.6, the recovery time is much longer than the estimated regeneration time constant [16]. Thus, the current required for overdrive recovery is much larger than that needed for sufficiently fast regenerative amplification. This comparison requires a new bias design of the gain and latch stage in a comparator. The current path (I_3) of the gain stage (Q_{10} and Q_{11}) in a master comparator is separated from that of the latch (I_5) and connected to a gain stage (Q_{18} and Q_{19}) in a slave comparator (also, the same configuration for latch stages) in a manner similar to that of the static frequency divider in [17]. This technique gives a better bias condition than that in Figure 3.6. The gain stage has a bias current $I_3 = 0.8$ mA and the gain is also limited to approximately 5 dB in order to maximize speed as in Section 3.3. The latch stage has a bias current $I_5 = 1.2$ mA . This bias scheme is very effective to suppress metastability and power dissipation in a comparator design with sufficient gain of the preamplifier stage formed by Q_0-Q_5 and R_0-R_1.

The preamplifier stage in Figure 3.9 is also different from that in Figure 3.6. Here the cascode configuration is used. It consists of a common-emitter stage (Q_2 and Q_3) followed by a common-base stage (Q_4 and Q_5). The load resistance seen by the

common-emitter transistor Q_2 is no longer R_0 but is the much lower input resistance of the common-base transistor Q_4, namely its r_e; and the same case for Q_3. The reduction in the effective load resistance of Q_2 and Q_3 leads to a tremendous improvement in the amplifier frequency response, which is a very important feature of the cascode amplifier. Also, the function of the common-base stage is to act as a current buffer. It accepts the signal current from the collectors of Q_2 and Q_3 at a low input resistance (r_e) and delivers an almost equal current to the load at a high output resistance. The output resistance of the cascode configuration is actually β times greater than that of the common-emitter amplifier [18].

Similarly as discussed in Section 3.3, the preamplifier stage formed by Q_0-Q_5 and R_0-R_1 is used to suppress input-referred offset. Resistors R_2-R_3 are set to relatively low value of 110 Ω and transistors Q_{10}-Q_{13} are chosen to be relatively small size bipolar transistors to enhance comparator sampling speed.

Implemented in a 0.35-μm SiGe BiCMOS process, the comparator shown in Figure 3.9 consumes approximately 80mW with sampling speed of 16 GHz and resolvable minimum input voltage of 10mV peak-to-peak. This comparator also passes the overdrive recovery test. The simulation results of the comparator with this new bias scheme will also be shown in Chapter 5. The master-slave comparator used in the high-speed flash ADC design presented in the next chapter uses the one with the improved bias scheme.

Presented in this chapter is the design of high-speed comparators. Two types of master-slave comparators are designed. The design focuses are to increase the sampling speed and reduce minimum differential input voltage while maintaining power dissipation at a relatively low level. The final comparator design for both

topologies presented has a very high speed of 16 GHz clock rate and very low resolvable minimum input voltage. One of the two types of the master-slave comparators uses standard design. The other one uses an improved bias scheme which can give rise to the optimum bias condition in master-slave comparators in term of regeneration time constant and power dissipation.

Some important design issues such as input-referred offset and design tradeoff have been given a detailed discussion. Timings related to the preamplifier and the latch of a basic comparator have also been analyzed. The comparators designed here can be used in very high speed flash ADC design with moderate resolution. Next chapter will present a high speed flash ADC design with the comparator structure shown in Figure 3.9 used as the comparator array.

CHAPTER 4

HIGH-SPEED FLASH ADC DESIGN

In this chapter, the design of the analog part of a high-speed flash ADC will be presented. The basic structure of a flash type ADC has been shown in Figure 1.3 and the introduction of how a flash ADC works has been presented in Section 1.2. The analog part of a flash ADC excludes the 2^N-to-N thermometer-to-binary encoder. The digital part, i.e., the thermometer-to-binary encoder will be briefly introduced at the end of this chapter. The ADC designed achieves a resolution of 5 bits and clock frequency of 6 GHz in the post-layout simulation.

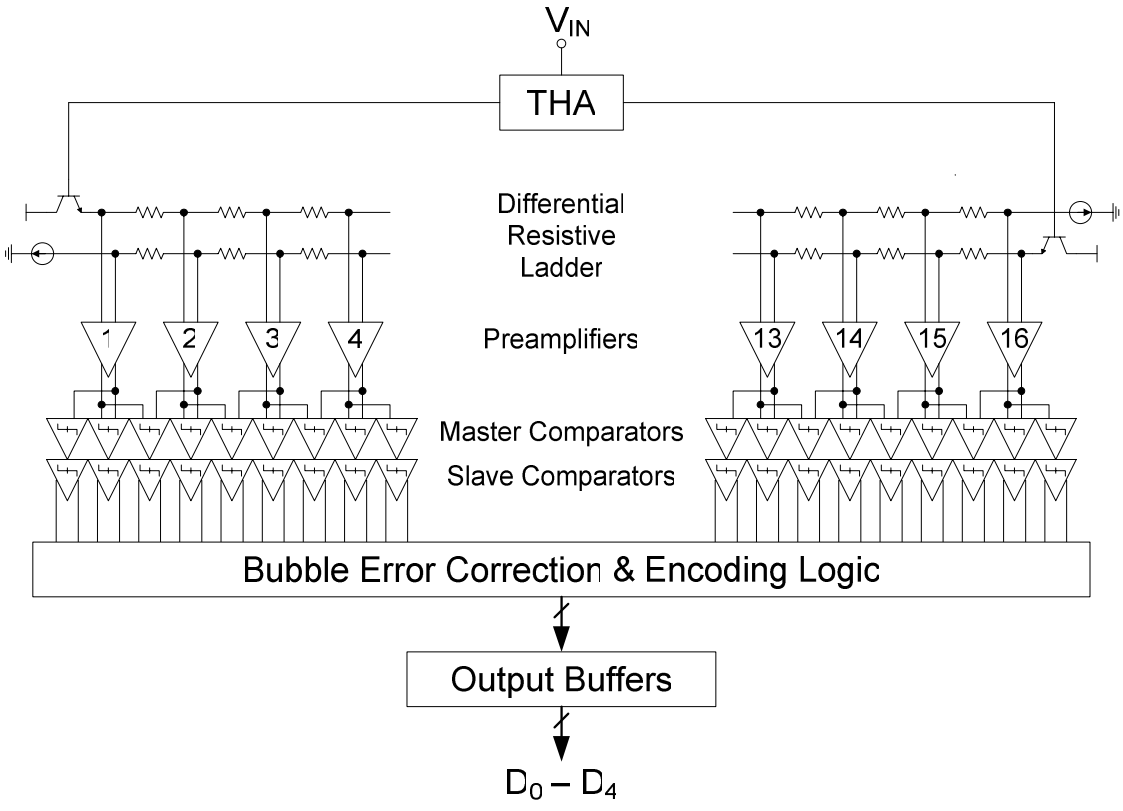


Figure 4.1: Fully differential 5-b flash ADC architecture

The flash ADC designed here should be able to work in the area of UWB Communications. The use of UWB signals for communication purposes is approved

by the Federal Communications Commission from 3.1 to 10.6 GHz. It is shown that pulsed UWB signals need 1 or 2 bits in the presence of AWGN, and 4 bits in the presence of a narrowband interferer [19]. Therefore, this ADC should have a sampling rate over Giga-Hertz and 5-bit resolution is enough. To achieve moderate resolution, the resolvable minimum input voltage (which should be slightly higher than the comparator offset to make the input distinguishable) of each comparator employed should be low. Thereby, the high-speed master-slave comparator designed in Section 3.4 satisfies the requirement and can be used here to make the comparator array of the flash ADC.

Figure 4.1 shows a fully differential 5-bit full-flash architecture. The differential input signal is sampled at a balanced track-and-hold amplifier, followed by a differential resistive ladder [20] generating 16 differential reference voltages. The $2\times$ interpolation technique [21] (refer to the connection between the preamplifier stage and the comparator array in Figure 4.1) employed by the ADC reduces the total parasitic capacitance loads and power dissipation, and improves the differential nonlinearity, which also allows the full excursion of the input signal at lower taps in a differential ladder. After amplification with a wide-band preamplifier stage, the master-slave comparator stage generates the thermometer output codes which are transferred to a bubble error correction logic. Then, the pipelined encoder can be used to convert the Gray coded data into a 5-bit binary code.

The master-slave comparator used has been presented in Section 3.4. In the following sections, the track-and-hold amplifier, the differential reference ladder and the bubble error correction logic after the comparator stage will be presented. Lastly, the thermometer-to-binary encoder will be briefly introduced.

4.1 Track-and-Hold Amplifier

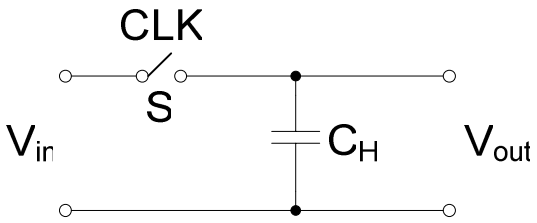


Figure 4.2: Simple track-and-hold circuit

Figure 4.2 shows a simple track-and-hold circuit. In the tracking/sampling (acquisition) mode, switch *S* (controlled by *CLK*) is on and the output voltage, V_{out}, tracks the input voltage, V_{in}. In the transition to the hold mode, *S* turns off and V_{out} remains constant until the next tracking period. In this circuit, the switching operation and the transient currents drawn by C_H introduce noise at the input, often mandating the use of a front-end buffer. Furthermore, since the voltage stored on C_H during the hold mode can be corrupted by any constant or transient current drawn by the following circuit, a buffer must also be placed at the output, resulting in the circuit shown in Figure 4.3.

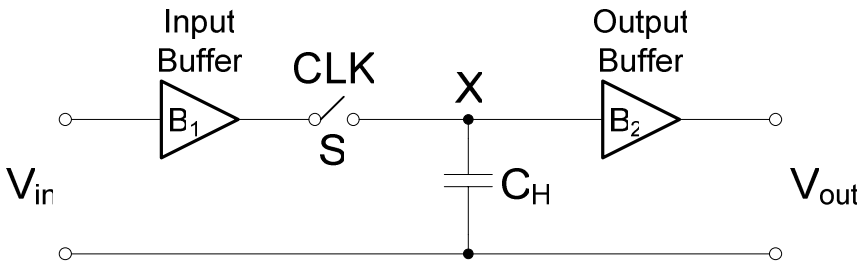
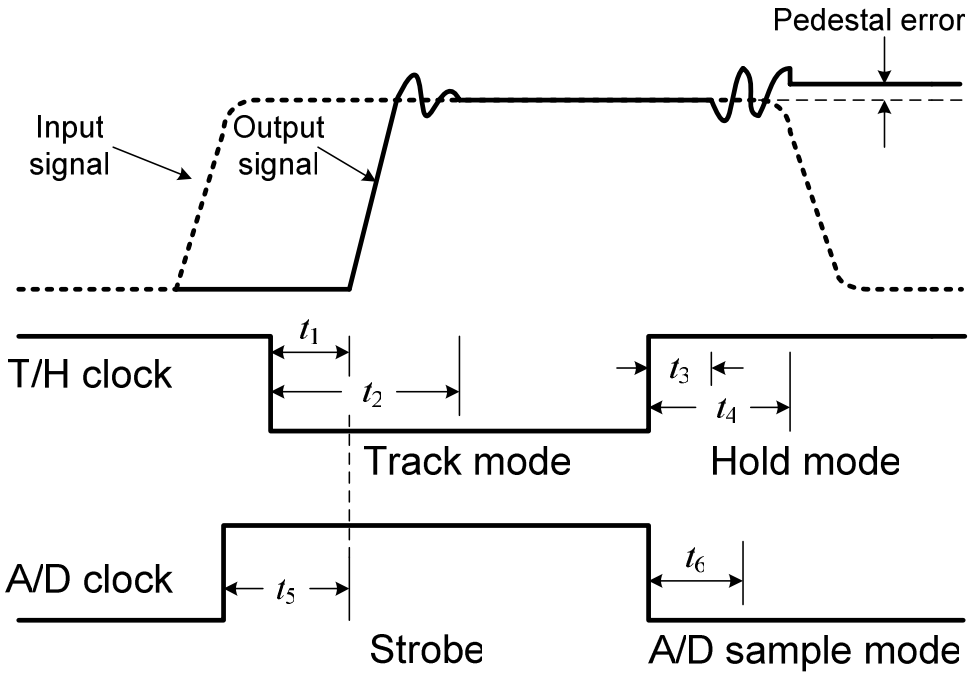


Figure 4.3: Track-and-hold circuit with input and output buffers

Although it is not necessary to include a THA in the flash architecture, a flash ADC's dynamic performance can be improved by adding an external THA. By adding a THA to a flash AD system, it is possible to effectively extend the converter's DC

performance to higher frequencies. Some of the factors which limit the ADC's dynamic performance will be nullified, such as small-signal input bandwidth, dynamic nonlinearity, and aperture jitter. The performance requirements for these specifications will be transferred to the THA. Other factors, such as large-signal bandwidth and slew-rate limitations, may not necessarily benefit as much from a THA since they still depend on the converter's ability to recover from full-scale voltage swings at the input.

Probably the most difficult aspect of applying a THA to a flash ADC is properly setting the timing relationship between the two devices. The goal is to have the THA acquire the signal during the interval that the ADC is *not* sampling its input, the strobe or latching phase for the bipolar ADC.



t_1 = T/H hold-track delay
t_2 = T/H acquisition time
t_3 = T/H aperture delay
t_4 = T/H setting time
t_5 = A/D aperture delay
t_6 = A/D sampling delay

Figure 4.4: Timing diagram for application of THA with flash ADC

A timing diagram which will illustrate the important relationships between the THA and AD clocks is shown in Figure 4.4. The proper timing is established by considering the performance specifications that are important to the THA circuit. In the figure, the falling edge of the THA clock sets it to the tracking mode. Near this time instant the rising edge of the AD clock removes it from the sampling mode. There will be a delay t_1 between the application of the hold signal and the actual return to the tracking of the THA. Proper design will guarantee that the aperture delay of the ADC, t_5, has expired before the signal from the THA starts slewing to its new level.

For track-and-hold amplifiers, a key specification is the acquisition time t_2, which is properly defined as the total time in tracking mode for the THA to slew to the new input level with the desired accuracy. This parameter will determine the minimum pulse width for the strobe cycle of the bipolar flash ADC.

After application of the hold signal, the THA will have its own aperture delay specification t_3, which is defined as the time required to terminate the tracking mode. t_4 is the track-and-hold settling time of the THA. For flash ADC applications, it is not necessary that the signal be completely settled at the beginning of the ADC's sampling interval, only that the slewing be completed and the THA is clearly in the hold mode. This is accomplished by considering the delay before sampling actually begins in the ADC, t_6, which should be set to occur after the aperture delay of the THA.

The pedestal error is the result of the feedthrough of switching transients onto the hold capacitor, which causes the THA output in the hold mode to deviate from the actual signal level at the end of tracking interval. Besides representing an error in accuracy, the important consideration with pedestal error is how it varies with the input signal level. A THA linearity specification must not be limited to the effects of the

buffer amplifier. Linearity in the final held voltage will ultimately be determined by the combination of the switch and buffer.

The ADC operating with a sampling speed in Giga-Hertz range increases the requirements on the sampling circuit with respect to sampling jitter. The main sources of sampling jitter are the phase noise of the reference clock source and the sampling time uncertainty of the quantizer (i.e., 2^N – 1 comparators). The sampling time uncertainty effect can be measured in terms of the SNR [22]:

$$\mathrm{SNR} = -20\log\left(2\pi f_{\mathrm{in}}\sigma_{\mathrm{jitter}}\right). \tag{4.1}$$

This equation demonstrates the necessity of RMS jitter under 1 ps to maintain 5-bit accuracy at a full-scale 5 GHz sinusoidal signal. Therefore, the use of a track-and-hold amplifier at the front of the quantizer can greatly reduce the sensitivity of the ADC to sampling jitter with a very low slew rate. The error source of sampling jitter is then shifted to the aperture jitter of the THA.

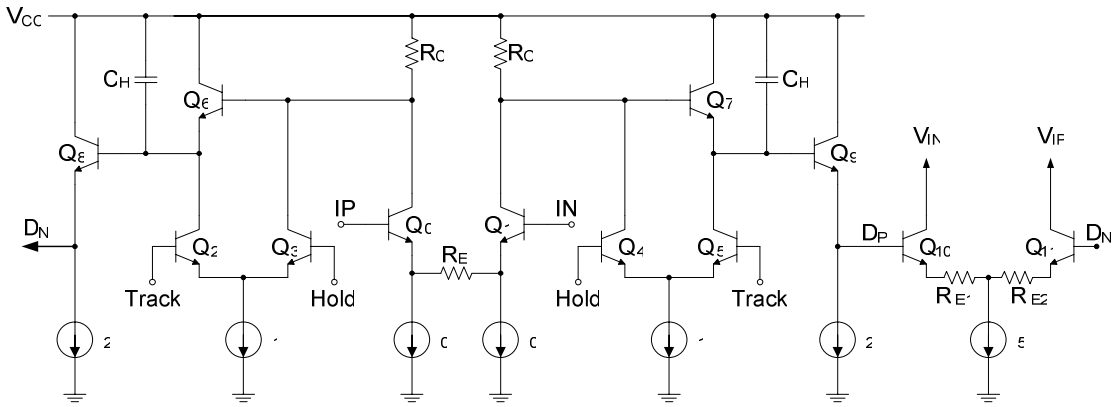


Figure 4.5: Schematic of a track-and-hold amplifier

The pedestal error of the THA may affect the comparator resolution. Consider the case when the pedestal error makes the THA output lower than the actually signal. Then originally distinguishable signals may become undistinguishable by the comparator. Slightly higher output than the actually signal will not deteriorate

comparator resolution. Since this pedestal error is not a fixed value, in general, this error should be made as small as possible so that the performance of the succeeding comparator array will not be affected a lot.

A simplified schematic of the THA is shown in Figure 4.5. It is designed for more than 5-bit linearity with the highest possible bandwidth. Open-loop architecture and fully differential signaling are used to enhance the sampling rate and common-mode noise rejection, respectively. The input differential pair Q_0-Q_1 and R_C form the input buffer of the THA. Optimization of the input buffer dynamic range is achieved by operating the input differential pair at a higher current level ($2\times I_0 = 7.8$ mA). This allows use of smaller emitter-degeneration resistors for a given degree of linearity and, thus, less input-referred noise. Without the use of diode-connected active loads [23], a lower power supply can be used to minimize power dissipation and to operate within the limited BV_{CEO} of a SiGe HBT. Current-driven switched emitter follower (SEF) is a proven technique for high-speed analog switches in bipolar/HBT technologies [23] [24]. The output of the differential pair is fed to the current-driven switched emitter followers whose switches are controlled by track and hold signals. The use of smaller hold capacitance ($C_H = 290$ fF) allows wide signal bandwidth over 16 GHz at the bias current of about 4.5 mA. The signals after track and hold operations are fed to the emitter followers Q_8-Q_9 which act as buffers. The pairs Q_{10}-Q_{11} and R_{E1}-R_{E2} form the output buffer of the THA which drives the sampled signal to the differential reference ladder. The emitter degeneration resistors, R_{E1}-R_{E2}, can make the input resistance of the output buffer increase by a factor of ($1 + g_{m10,11}R_{E1,2}$). Also the introduction of the emitter degeneration resistance makes the voltage gain less dependent on the value of β and improves high-frequency response, although the voltage gain is somewhat sacrificed.

The simulation results of the track-and-hold amplifier circuit will be shown in Chapter 5.

4.2 Differential Reference Ladder

A simplified circuit of the differential reference ladder is shown in Figure 4.6. It has 15 resistors on each ladder and generates 16 differential reference voltages to the preamplifiers preceding the comparators. While the differential ladder has the significant advantages of reducing the capacitive loading of the sampled signal and reducing threshold bowing, the performance of the differential ladder is hampered by several effects: settling time, full-scale quantization range, and device mismatch.

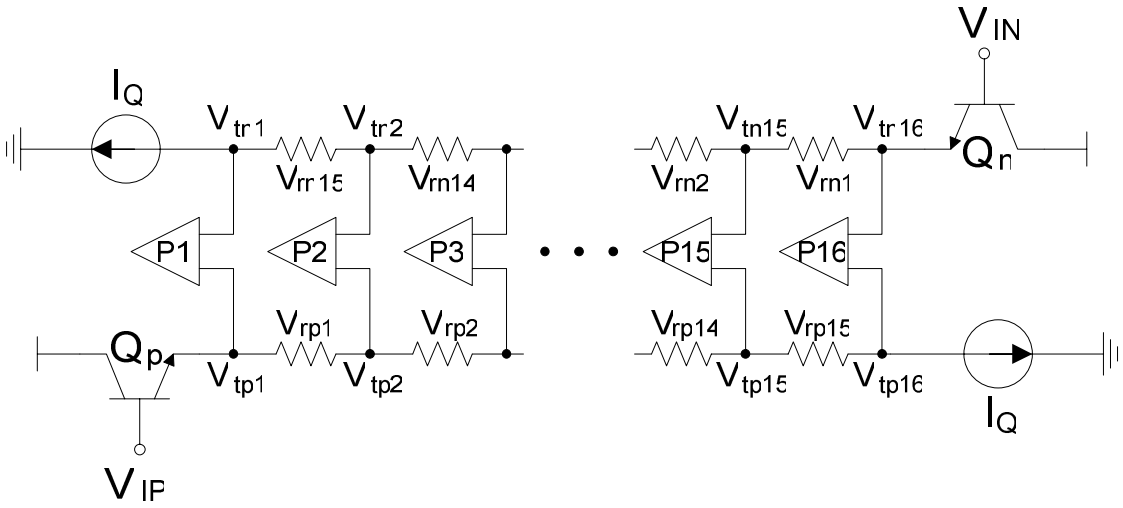


Figure 4.6: Differential reference ladder

The distributed nature of the loading places a practical upper limit on the number of preamplifiers, tap resistance, and resistor material. Incorporating the interpolation technique can enhance settling time tolerance. The total capacitance at each tap is calculated to be approximately 0.65 pF. Since the allowable settling time is 25 ps and 3.5 time constants are needed for 5-bit accuracy, the required output resistance of the ladder is then 11 Ω. The output resistance peak occurs in the middle

of the ladder and at that point is one quarter of total tap resistance [1], thus total tap resistance is 44 Ω. With design margin for implementation, each tap resistance on the ladder is chosen to be 3.5 Ω.

The bias current source of the resistive ladder is made from a high gain op amp buffer with the addition of an emitter follower. Figure 4.7 shows the bias circuit. The drive transistor is connected to the op amp in the unity gain configuration and $V-$ of the op amp is connected to an externally applied voltage V_{ref}.

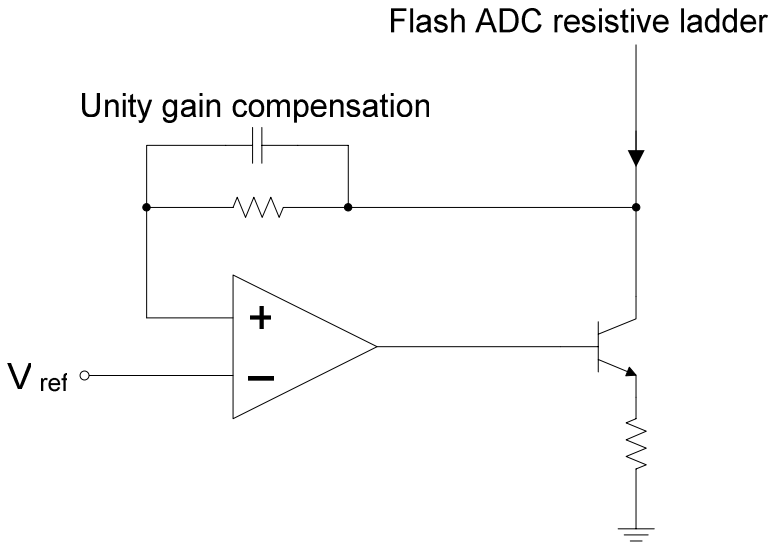


Figure 4.7: Bias circuit of the resistive ladder

The design uncertainties in a differential ladder (i.e., errors in the tap resistances as well as in the bias currents and base currents of the next stage) give rise to severe nonlinearities. From the investigation of normally distributed resistor matching requirement for a 4-bit resistor string with 5-bit matching property, σ_R / R is less than 12.5% [25]. In Figure 4.6, the tap voltages of the differential ladder can be derived as

$$V_{tpk} = V_{IP} - V_{be}\left(Q_p\right) - \sum_{i=0}^{k-1} V_{rpi} \,, \tag{4.2}$$

$$V_{tnk} = V_{IN} - V_{be}(Q_n) - \sum_{j=0}^{N-k} V_{rnj}\,, \tag{4.3}$$

where V_{IP} and V_{IN} represent the sampled differential inputs from the THA, V_{tp} (or V_{tn}) represents a tap voltage, and V_{rp} (or V_{rn}) denotes the voltage across a tap resistor. N is the total number of quantization levels. Here, N = 16, V_{rp0} = 0, V_{rn0} = 0. The differential preamplifier input is then given by

$$V_{Pk} = V_{tpk} - V_{tnk} = (V_{IP} - V_{IN}) - \Delta V_{rk}\,, \tag{4.4}$$

where

$$\Delta V_{rk} = \sum_{i=0}^{k-1} V_{rpi} - \sum_{j=0}^{N-k} V_{rnj}\,, \tag{4.5}$$

and

$$V_{rpk} = R\left(I_Q + \sum_{i=k+1}^{N} I_{bi}\right), \tag{4.6}$$

$$V_{rnk} = R\left(I_Q + \sum_{i=1}^{N-k} I_{bi}\right), \tag{4.7}$$

for k = 1, 2, …, 15. I_{bi} is the base current of the ith preamplifier as shown in Figure 4.6. Suppose the base currents I_{bi}'s are sufficiently small, then the differential inputs for the preamplifiers are just (V_{IP} – V_{IN}) and (–15, –13, –11, …, –1, 1, 3, …, 11, 15) × V_r where V_r = R × I_Q. The differential input for each preamplifier in Figure 4.6 is summarized in Table 4.1.

Table 4.1: Differential input for each preamplifier

Preamplifier	Input 1	Input 2	Preamplifier	Input 1	Input 2
P1	$V_{IP} - V_{IN}$	$-15 \times RI_Q$	**P9**	$V_{IP} - V_{IN}$	$1 \times RI_Q$
P2	$V_{IP} - V_{IN}$	$-13 \times RI_Q$	**P10**	$V_{IP} - V_{IN}$	$3 \times RI_Q$
P3	$V_{IP} - V_{IN}$	$-11 \times RI_Q$	**P11**	$V_{IP} - V_{IN}$	$5 \times RI_Q$
P4	$V_{IP} - V_{IN}$	$-9 \times RI_Q$	**P12**	$V_{IP} - V_{IN}$	$7 \times RI_Q$
P5	$V_{IP} - V_{IN}$	$-7 \times RI_Q$	**P13**	$V_{IP} - V_{IN}$	$9 \times RI_Q$
P6	$V_{IP} - V_{IN}$	$-5 \times RI_Q$	**P14**	$V_{IP} - V_{IN}$	$11 \times RI_Q$
P7	$V_{IP} - V_{IN}$	$-3 \times RI_Q$	**P15**	$V_{IP} - V_{IN}$	$13 \times RI_Q$
P8	$V_{IP} - V_{IN}$	$-1 \times RI_Q$	**P16**	$V_{IP} - V_{IN}$	$15 \times RI_Q$

4.3 Bubble Error Correction Logic

Figure 4.8 shows a schematic of the bubble error correction circuit. The bubble error correction circuits are preceded by slave comparators. Each thermometer code is examined and amplified relative to its two nearest neighbors based on a voting process, and the output is corrected if it disagrees with both. Thus, the output can be given by [26]

$$B_o = T_a T_b + T_b T_c + T_c T_a . \tag{4.8}$$

However, this circuit entails several issues. First, the voting process is not effective in removing consecutive two bubbles in a thermometer code (i.e., …0011**00**111…). Second, there exits input pattern-dependent decision time variations, so flip-flops after the bubble logics are necessary to synchronize the data. Third, use of this complex circuit increases the power dissipation. The thermometer code output from the

correction circuits can be decoded to pipelined Gray code, and then later decoded to binary code, which are presented in the next section.

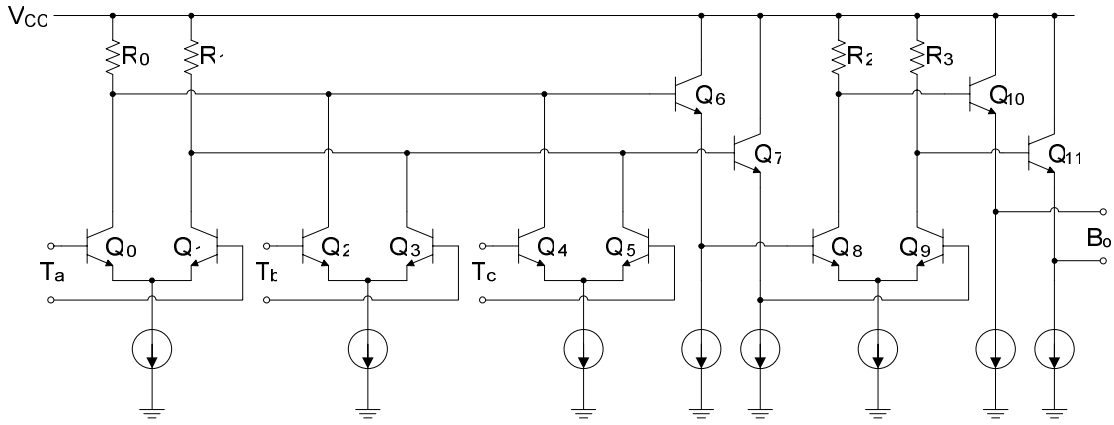


Figure 4.8: Bubble error correction logic

4.4 Thermometer-to-Binary Encoder

Two of the potential errors in flash converters, namely, metastability and sparkles, can be suppressed using Gray encoding as an intermediate step between thermometer and binary codes. The probability of metastable states can be lowered because in Gray encoding no signal is applied to more than one input, allowing the use of pipelining to increase the time for regeneration. The effect of sparkles is reduced because the accuracy of the Gray code degrades very gradually as more sparks appear in the thermometer code.

For the 5-bit flash ADC designed here, the thermometer code, Gray code and Binary code are shown in Table 4.2. From the correspondence shown in the table, the Gray code output $G_4G_3G_2G_1G_0$ can be expressed in terms of the thermometer code as follows:

$$
\begin{aligned}
G_0 &= T_1\overline{T_3} + T_5\overline{T_7} + T_9\overline{T_{11}} + T_{13}\overline{T_{15}} + T_{17}\overline{T_{19}} + T_{21}\overline{T_{23}} + T_{25}\overline{T_{27}} + T_{29}\overline{T_{31}},\\
G_1 &= T_2\overline{T_6} + T_{10}\overline{T_{14}} + T_{18}\overline{T_{22}} + T_{26}\overline{T_{30}},\\
G_2 &= T_4\overline{T_{12}} + T_{20}\overline{T_{28}},\\
G_3 &= T_8\overline{T_{24}},\\
G_4 &= T_{16}.
\end{aligned}
\tag{4.9}
$$

Table 4.2: Correspondence among thermometer, Gray and binary codes

Thermometer																																Gray					Binary				
T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{16}	T_{17}	T_{18}	T_{19}	T_{20}	T_{21}	T_{22}	T_{23}	T_{24}	T_{25}	T_{26}	T_{27}	T_{28}	T_{29}	T_{30}	T_{31}	G_4	G_3	G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
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1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	1

The key point in these equations is that T_j appears in only one expression and hence no signals in the logic split. As a result, metastable errors can be reduced by pipelining the encoding, which is shown in Figure 4.9.

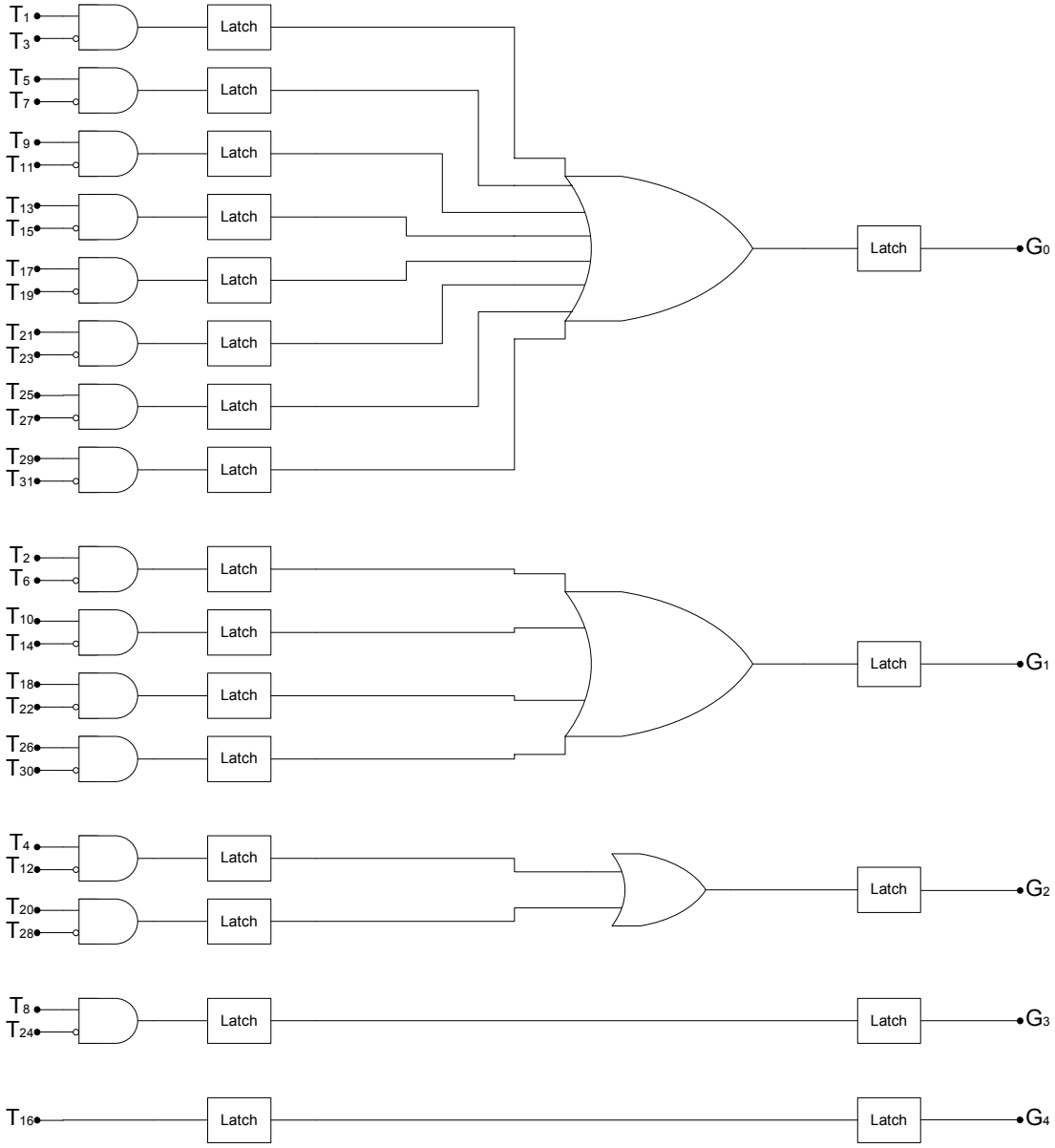

Figure 4.9: Gray encoding with pipelining

To see the robustness of Gray encoding with respect to sparkles, consider the case illustrated in Table 4.3. Here 4-bit is used for easy demonstration. Note that while the number of sparkles increases, the Gray output remains fairly close to the top of the thermometer code, providing a reasonable approximation of the sampled value.

Table 4.3: Gray encoding in the presence of sparkles

	Thermometer Code	Gray Code	Equivalent Decimal Output
No Sparkle:	1111111111111100	1011	13
One Sparkle:	1111111111111010	1000	15
Two Sparkles:	1111111111111001	1010	12

The logic expressions to convert Gray code to Binary code are as follows:

$$\begin{aligned} B_4 &= G_4, \\ B_3 &= B_4 \oplus G_3, \\ B_2 &= B_3 \oplus G_2, \\ B_1 &= B_2 \oplus G_1, \\ B_0 &= B_1 \oplus G_0, \end{aligned} \tag{4.10}$$

where $\oplus$ indicates exclusive OR operation. Figure 4.10 shows the corresponding logic circuits design.

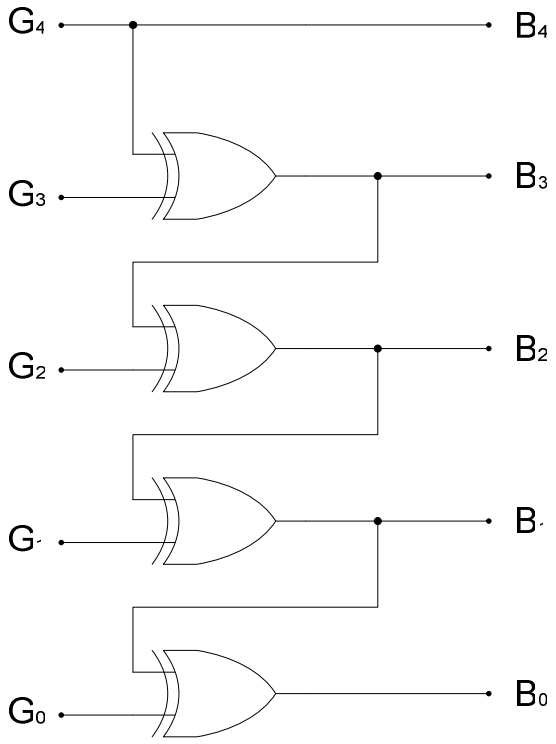

Figure 4.10: A parallel Gray to binary converter

The thermometer-to-binary encoder is the last stage of the flash ADC design. The flash ADC output is thereby a 5-bit digital output.

Presented in this chapter is the design of a high-speed flash ADC. The design of the analog part of the flash ADC has been given a detailed expatiation. By adding a track-and-hold amplifier and a differential resistive ladder which are in front of the master-slave comparator designed in Chapter 3 and a bubble error correction logic circuit after the comparator stage, the analog part of a flash ADC can be constructed. The digital part, i.e., the thermometer-to-binary encoder has also been briefly introduced to complete the flash ADC design.

Although THA is not necessary in flash ADC design, when the operating frequency is over Giga-Hertz, the introduction of a THA in the flash ADC will greatly enhance the ADC performance. The resulting THA can work for wide-band signals over 10 GHz. A differential resistive ladder follows the THA. The resistive ladder generates 16 differential reference voltages which are fed into 16 wide-band preamplifiers. Here the 2× interpolation technique is employed to reduce the number of preamplifiers. In this way, the parasitic capacitance loads and power dissipation will be lowered. After the interpolation, 33 outputs from the preamplifiers stage are connected to the master-slave comparators array. The high-speed master-slave comparator design has been presented in Chapter 3. The bubble error correction circuits succeed the slave comparators. The thermometer code output from the correction circuits is decoded to pipelined Gray code, and then later decoded to binary code.

CHAPTER 5

SIMULATION RESULTS

The comparators presented in Chapter 3 as well as the flash ADC presented in Chapter 4 are implemented in a 0.35-μm SiGe BiCMOS process which has an f_T of 60-GHz for the bipolar NPN transistor. In this chapter, the simulation results for both of the comparators in Chapter 3, the track-and-hold amplifier in Chapter 4 and the whole analog part of the flash ADC in Chapter 4 are going to be presented. Finally, the flash ADC performance will be summarized.

5.1 Simulation Results for the Comparator in Section 3.3

Implemented in a 0.35-μm SiGe BiCMOS process, the active area of the master-slave comparator presented in Section 3.3 is only 145 μm × 165 μm in the test chip layout. The clocks used are sinusoidal signals. The master-slave comparator functions properly when the clock frequency is at 16 GHz with 3.3 V power supply. The input common-mode level is between 1.1 V and 3.2 V. The resolvable minimum input difference is 10 mV and the power consumption is approximately 87 mW with post-layout simulation. Figure 5.1 shows the layout of the comparator. Figure 5.2 shows a sample input and the resulting output. The differential input is a sinusoidal signal with frequency of 8 GHz and amplitude of 10 mV. In this case, the comparator samples the voltages of ±10 mV. Therefore, Figure 5.2 actually shows the comparator functionality when it resolves minimum input voltage. From the output waveform, it clearly shows that the output can reach ±380 mV which is a valid logic level for the next stage. Since the comparator operates at the fastest sampling rate, there is no flat region in the output during the hold mode.

The voltage difference between the inputs needed to switch the comparator is the offset voltage. Simulation shows that the comparator is able to distinguish input difference of ±8 mV. When the input difference is ±8 mV, the comparator is able to generate correct polarity, although not able to generate the output to a valid logic level. When the input difference is below ±8 mV, the comparator cannot generate a meaningful output. Therefore, the offset of the comparator is 8 mV.

The overdrive recovery test has been done for input signal varying from positive full scale to −1 LSB (−10 mV) and from negative full scale to 1 LSB (10 mV). The simulation result shows that when the differential input voltage varies from 20 mV to −10 mV and from −20 mV to 10 mV, the output generates correct logic levels. Sample output waveforms for overdrive recovery test are shown in Figure 5.3 and Figure 5.4. The clock frequency is at 16 GHz which means that the comparator designed also passes overdrive recovery test.

The overall performance of the comparator designed in Section 3.3 is summarized in Table 5.1.

Table 5.1: Performance of the comparator designed in Section 3.3

Performance Metrics	Simulated Results
Maximum operating frequency	16 GHz
Minimum input voltage	±10 mV
Offset	8 mV
Active area	145 μm × 165 μm
Supply voltage	3.3 V
Power consumption	87 mW

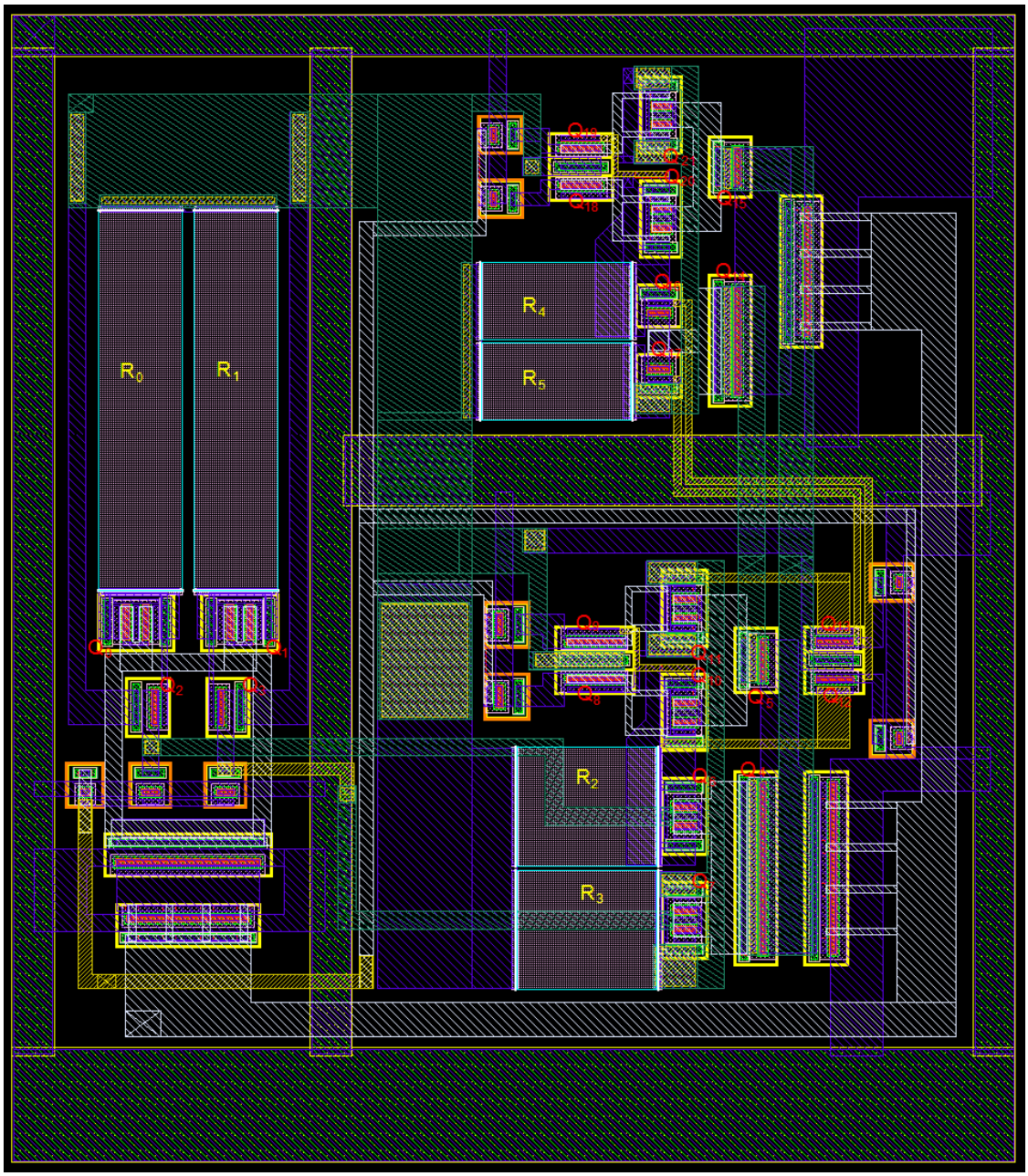

Figure 5.1: Layout of the master-slave comparator in Section 3.3

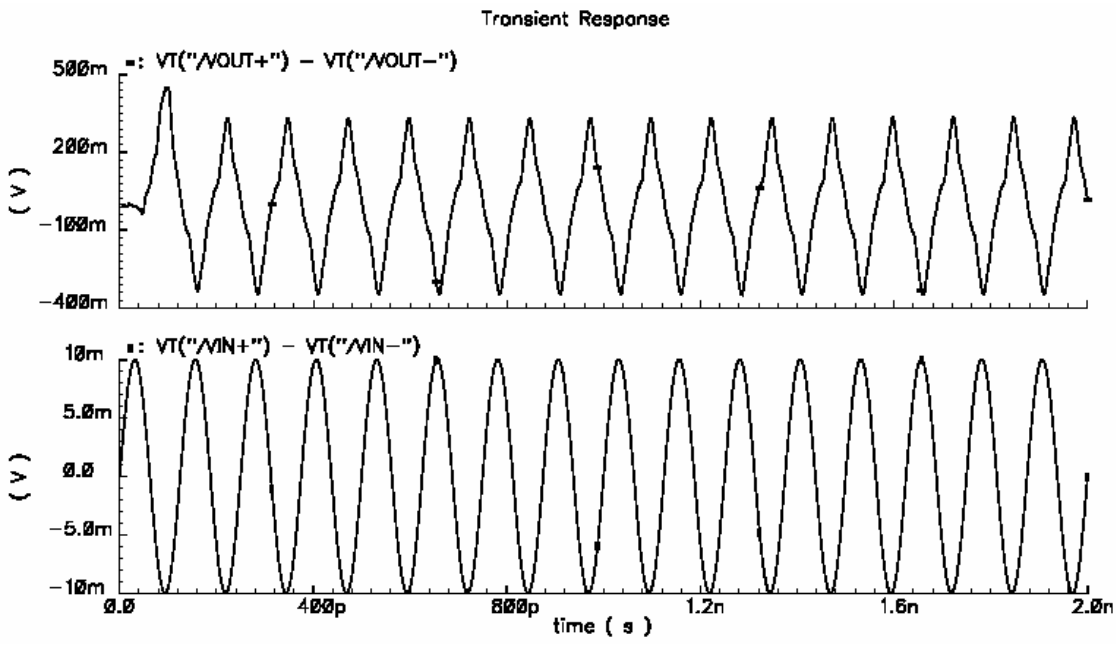

Figure 5.2: Sample input and output of the comparator in Section 3.3

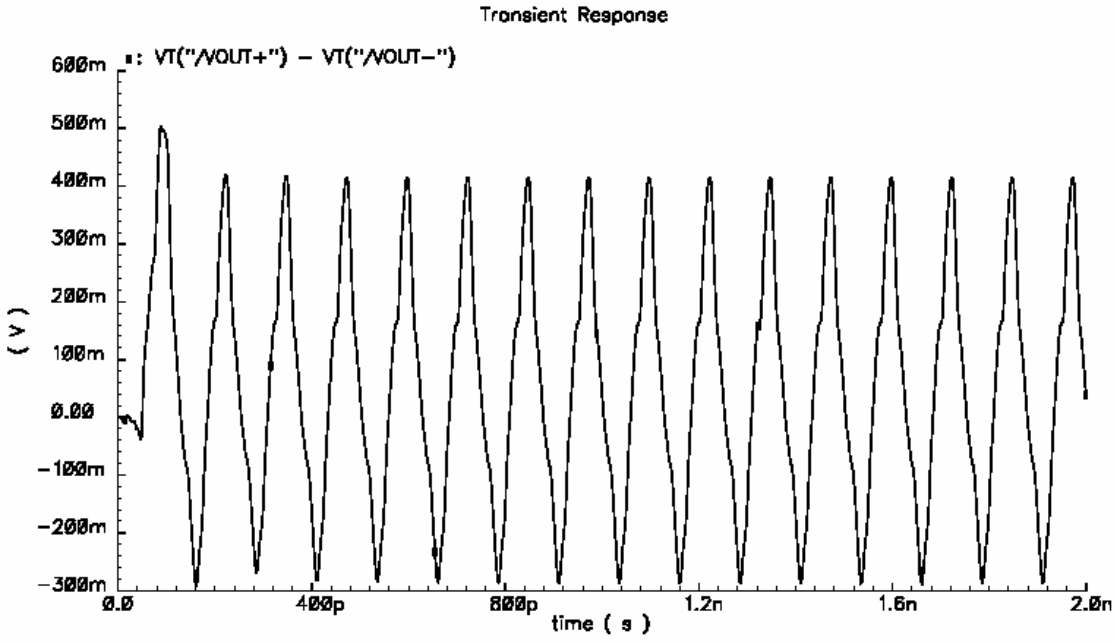

Figure 5.3: Overdrive recovery test for positive full-scale input to –1 LSB (Section 3.3)

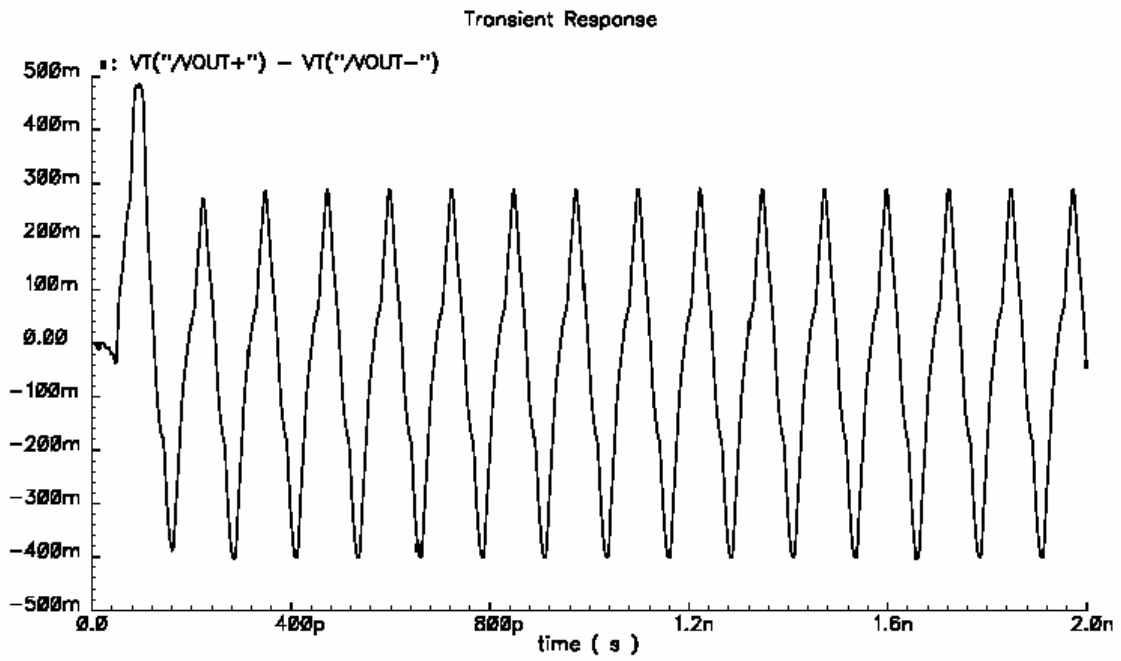

Figure 5.4: Overdrive recovery test for negative full-scale input to +1 LSB (Section 3.3)

5.2 Simulation Results for the Comparator in Section 3.4

The active area of the master-slave comparator presented in Section 3.4 is only 180 μm × 110 μm in the test chip layout. This master-slave comparator also functions properly when the clock frequency is at 16 GHz with 3.3 V power supply. The input common-mode level is between 1.1 V and 3.2 V. The resolvable minimum input difference is 10 mV and the power consumption is approximately 80 mW with post-layout simulation. Figure 5.5 shows the layout of the comparator. The comparator offset voltage is also measured to be 8 mV. Since the simulation results are quite similar to those presented in Section 5.1, they are not redundantly shown here. Table 5.2 summarizes the comparator performance.

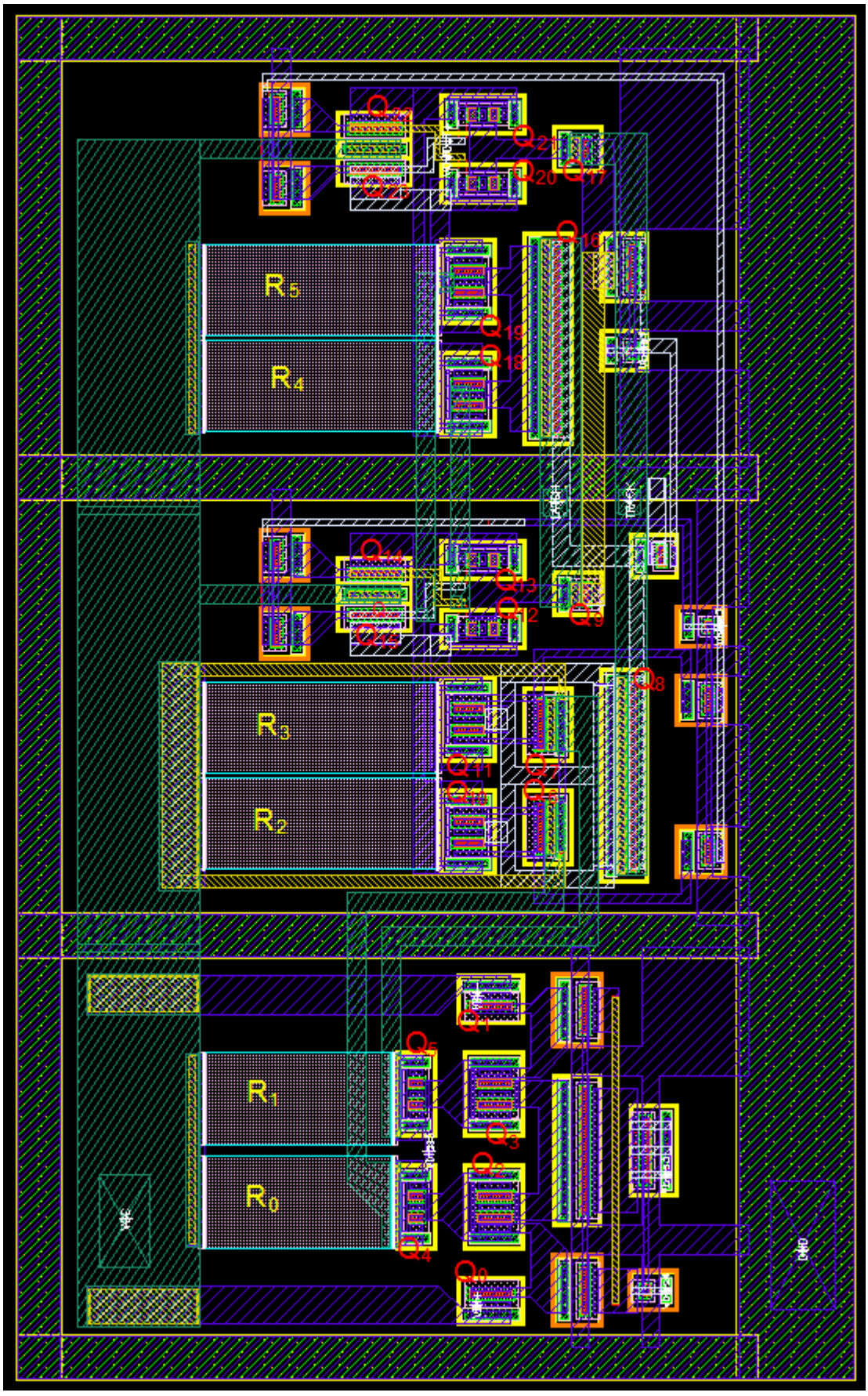

Figure 5.5: Layout of the master-slave comparator in Section 3.4

Table 5.2: Performance of the comparator designed in Section 3.4

Performance Metrics	Simulated Results
Maximum operating frequency	16 GHz
Minimum input voltage	±10 mV
Offset	8 mV
Active area	180 μm × 110 μm
Supply voltage	3.3 V
Power consumption	80 mW

5.3 Simulation Results for the Track-and-Hold Amplifier

The track-and-hold amplifier shown in Figure 4.5 has been tested to verify its functionality. Figure 5.6 shows the layout of the THA and Figure 5.7 shows a sample input and the resulting output with clock frequency at 12 GHz. The track/hold clocks used are sinusoidal signals and the differential input is a sinusoidal signal with frequency of 6 GHz and amplitude of 10 mV. The track phase and the hold phase of the THA are clearly shown from the output in Figure 5.7, thus it verifies that the track-and-hold amplifier functions properly. The distortion behavior of the THA can be understood by measuring its gain variation. Figure 5.8 shows the gain variation under 2% over full-scale input range. From Figure 5.8, the gain variation of the THA is small and the THA has high linearity. Simulation has been done to show the total harmonic distortion of around –30 dBc at a full-scale 6 GHz input signal.

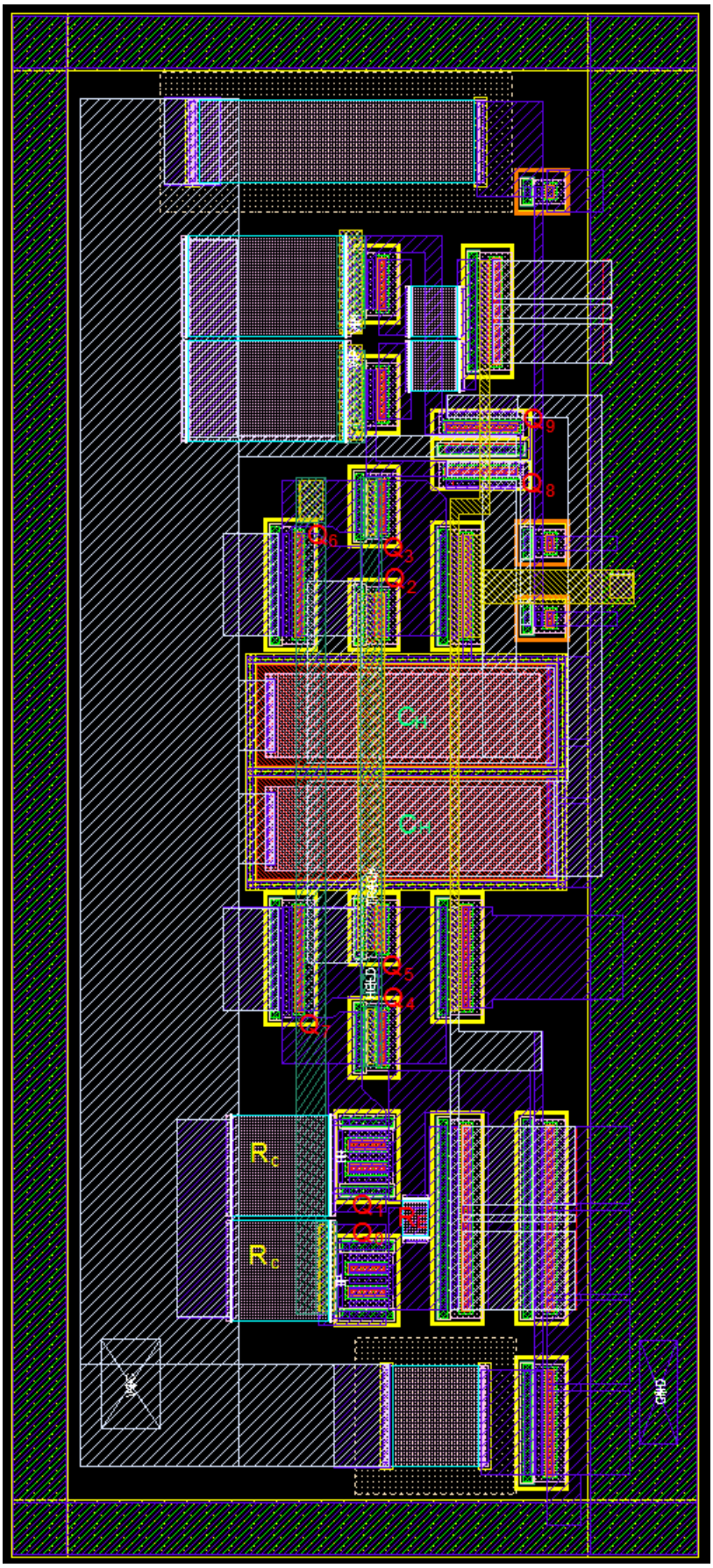

Figure 5.6: Layout of the track-and-hold amplifier

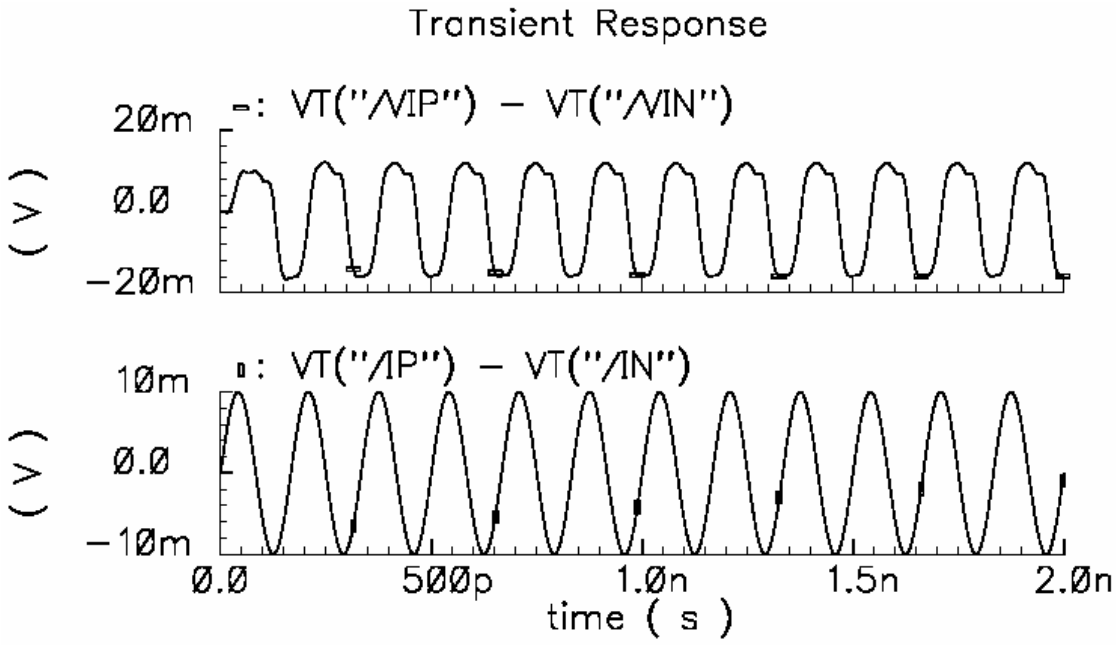

Figure 5.7: Sample input and output of the THA

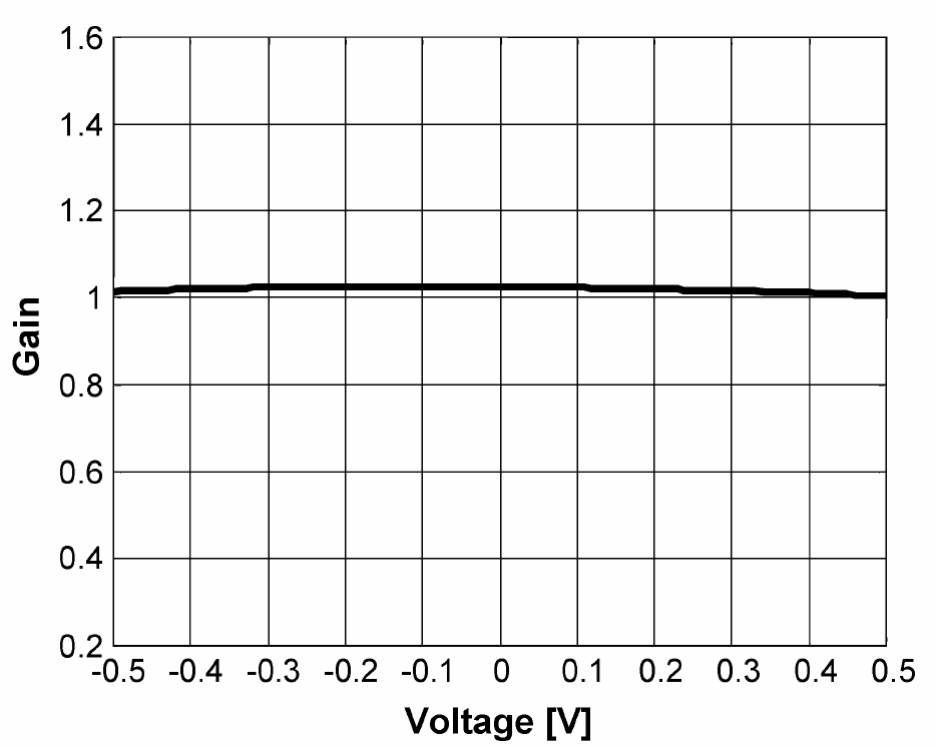

Figure 5.8: Gain variation of the THA

5.4 Simulation Results for the Flash ADC

The design of the analog part of a flash ADC based on the comparator with improved bias scheme has been presented in Chapter 4. Here, some simulation results are presented to verify the performance of the analog part of the ADC and the performance of the complete ADC will be given as well.

Since differential clocks are used to define the tracking/hold modes in the track-and-hold amplifier and the tracking/latching modes in the master-slave comparator, their relationship needs to be explicitly explained. Figure 5.9 shows the relationship between the differential clocks and the corresponding output at each stage with a sinusoidal input. It is clearly shown that when the THA is in the tracking mode, the master comparator is in the latching mode and the slave comparator is in the tracking mode; and when the THA is in the hold mode, the master comparator is in the tracking mode and the slave comparator is in the latching mode.

For example, at time instant (1) which is at $0.5T$ with T being the clock frequency, the THA stops tracking the input signal and enters the hold mode; the master comparator at this time starts to track the THA output. After half period which is at T, the THA finishes the hold mode and the master comparator finishes the tracking mode and starts to regenerate its output tracked from the THA; at this time the slave comparator starts to track the output of the master comparator. Then after another half period which is at $1.5T$, the master comparator finishes the latching mode and the slave comparator finishes the tracking mode and starts to regenerate its output tracked from the master comparator. The latching mode of the slave comparator also lasts for half period. Therefore, at time instant $2T$, the slave comparator generates the logic output corresponding to the input sampled at time instant $0.5T$. The delay from the

time the clock samples the input to the time when the actual logic output is generated is thereby 1.5*T*. But since this is a constant delay, it will not affect the functionality of the flash ADC. Similarly in Figure 5.9, the input sampled at 1.5*T* (2) will generate a logic value at 3*T* and the input sampled at 2.5*T* (3) will generate a logic value at 4*T*.

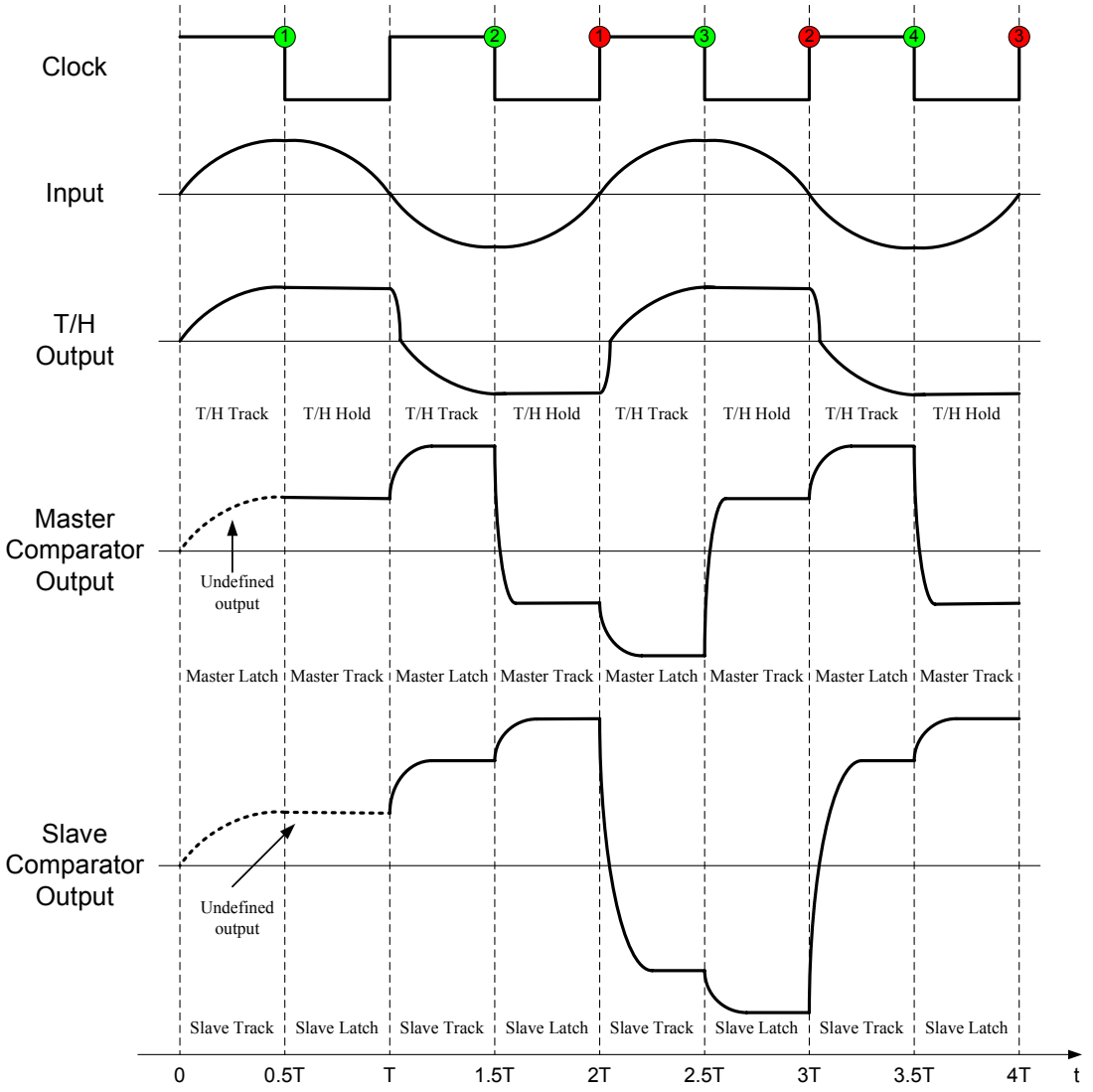

Figure 5.9: Relationship between the differential clocks

The analog part of the flash ADC consists of a track-and-hold amplifier, a differential resistive ladder generating 16 pairs of differential input which are fed to the 16 preamplifiers. By using the interpolation technique, the number of preamplifiers is reduced from 32 to 16, which saves the power and also reduces the capacitive load

to the differential resistive ladder. There are 33 master comparators and 33 slave comparators that are connected after the preamplifier stage. The last stage is 31 bubble error correction logic circuits. The analog part of the flash ADC is implemented in a 0.35-μm SiGe BiCMOS process, the active area is 0.7 mm × 3.3 mm in the test chip layout. The clocks used are sinusoidal signals. The ADC functions properly when the clock frequency is at 6 GHz with 3.3 V power supply and the power consumption is approximately 4.88 W with post-layout simulation. Figure 5.10 shows a part of the layout for the analog part of the flash ADC.

To test the functionality of the analog part of the flash ADC, a differential sinusoidal signal with frequency of 3 GHz and amplitude of 10 mV is fed into the input. Each of the bias current sources in the differential resistive ladder as shown in Figure 4.6 is set to 1 mA. Since each tap resistance on the differential resistive ladder is set to 3.5 Ω, the voltage across each tap resistance will be 3.5 mV neglecting the input base currents of the preamplifiers. Then the input to each of the 16 preamplifiers can be obtained according to Table 4.1. Since the numbering sequence of the preamplifiers in the testing circuit is reversed compared to the circuit drawn in Figure 4.6, the preamplifier input voltages shown in Table 5.3 will be slightly different from those shown in Table 4.1. But it is irrelevant to the performance and the testing results of the ADC.

Noting from Table 5.3, only the 8^{th} and the 9^{th} preamplifiers generate outputs with both positive and negative parts. Preamplifiers 1 ~ 7 generate all negative outputs and preamplifier 10 ~ 16 generate all positive outputs. After interpolation, the outputs of the preamplifiers are fed into 33 comparators. Based on the polarities of the preamplifiers' outputs, the resulting comparators outputs are also shown in Table 5.3.

Note that comparators 14 ~ 18 generate outputs with both positive and negative parts. All the others generate output with single polarity. After the comparator stage, 31 bubble error correction logic circuits are connected. Each nearby 3 comparators are connected to one bubble error correction circuit. Also, only BEC 14 ~ 18 generate outputs with both positive and negative parts.

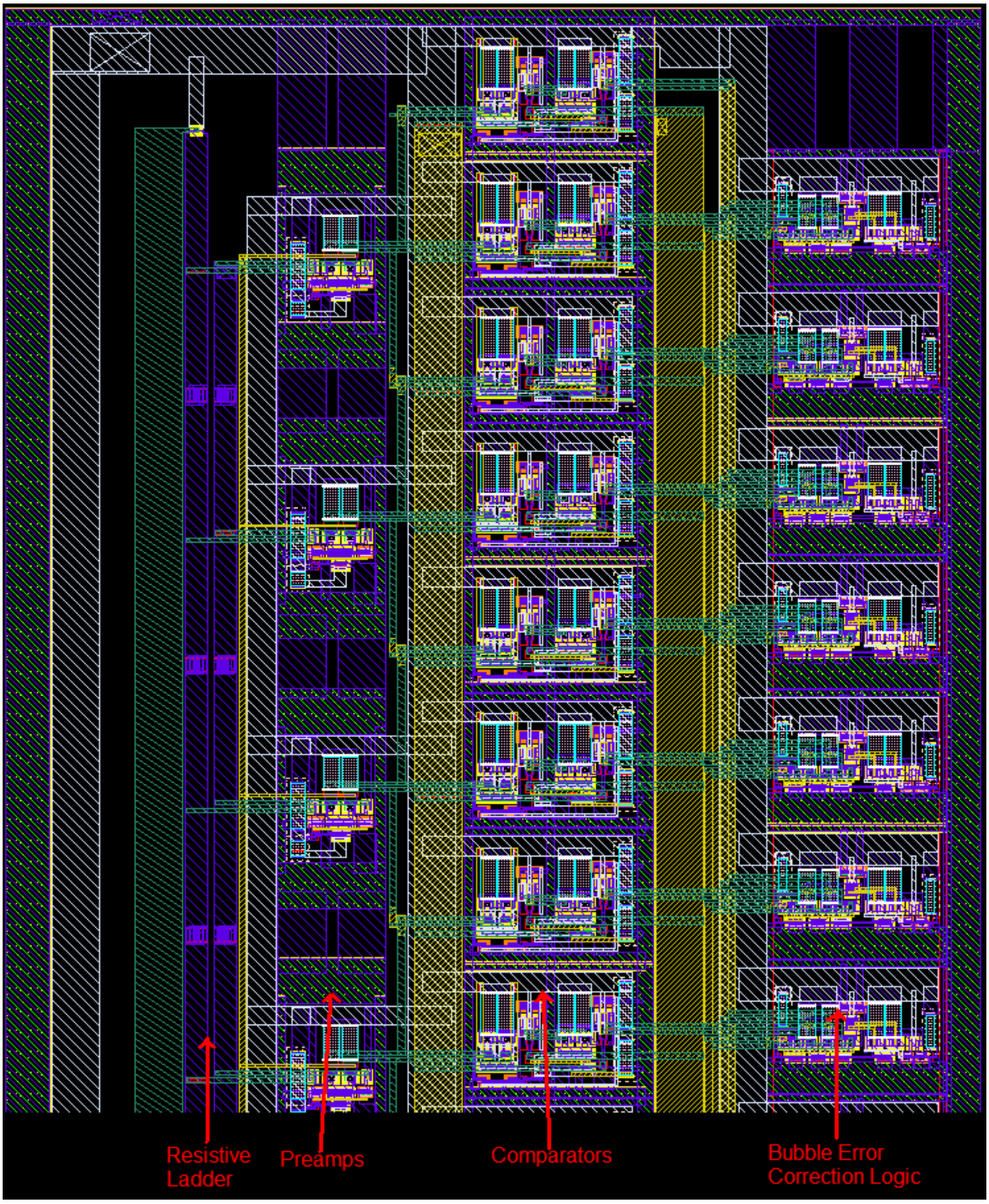

Figure 5.10: Part of the layout for the analog part of the flash ADC

The simulation results are shown from Figure 5.11 to Figure 5.15. Some of the BEC outputs are presented. Figure 5.11 shows the 16^{th} BEC output. It is clearly shown that the output follows the input polarity correctly. Figure 5.12 and Figure 5.13 shows the $14^{th}/15^{th}$ and $17^{th}/18^{th}$ BEC output respectively. The simulation results match the results in Table 5.3 and also verify that the output follows the input polarity correctly. In Figure 5.11 to Figure 5.13, there are labels indicating the sampling point and the corresponding output. It shows that the time from the sampling point to generating the output logic is (0.75 × input sinusoid period). Since the frequency of the input sinusoid is half of that of the clock, the time delay is (1.5 × clock frequency). Figure 5.14 shows the 9^{th} – 13^{th} BEC output and they are all logic low and Figure 5.15 shows the 19^{th} – 22^{nd} BEC output and they are all logic high. Since the other outputs are all either logic high or logic low, they are the same as the waveforms in Figure 5.14 or Figure 5.15. They are not redundantly shown here.

Therefore, the simulation results verify that the analog part of the flash ADC functions correctly. This ADC works at speed of 6 GSample/s with 5-bit resolution with post-layout simulation.

Table 5.3: Output at each stage

Preamplifier Stage			Comparator Stage Output	BEC Stage Output
Input 1	Input 2	Output		
			C0: –	
Sinusoidal signal with frequency of 3 GHz and amplitude of 10 mV	52.5 mV	P1: –	C1: –	B1: –
			C2: –	B2: –
	45.5 mV	P2: –	C3: –	B3: –
			C4: –	B4: –
	38.5 mV	P3: –	C5: –	B5: –
			C6: –	B6: –
	31.5 mV	P4: –	C7: –	B7: –
			C8: –	B8: –
	24.5 mV	P5: –	C9: –	B9: –
			C10: –	B10: –
	17.5 mV	P6: –	C11: –	B11: –
			C12: –	B12: –
	10.5 mV	P7: –	C13: –	B13: –
			C14: +/–	B14: +/–
	3.5 mV	P8: +/–	C15: +/–	B15: +/–
			C16: +/–	B16: +/–
	–3.5 mV	P9: +/–	C17: +/–	B17: +/–
			C18: +/–	B18: +/–
	–10.5 mV	P10: +	C19: +	B19: +
			C20: +	B20: +
	–17.5 mV	P11: +	C21: +	B21: +
			C22: +	B22: +
	–24.5 mV	P12: +	C23: +	B23: +
			C24: +	B24: +
	–31.5 mV	P13: +	C25: +	B25: +
			C26: +	B26: +
	–38.5 mV	P14: +	C27: +	B27: +
			C28: +	B28: +
	–45.5 mV	P15: +	C29: +	B29: +
			C30: +	B30: +
	–52.5 mV	P16: +	C31: +	B31: +
			C32: +	

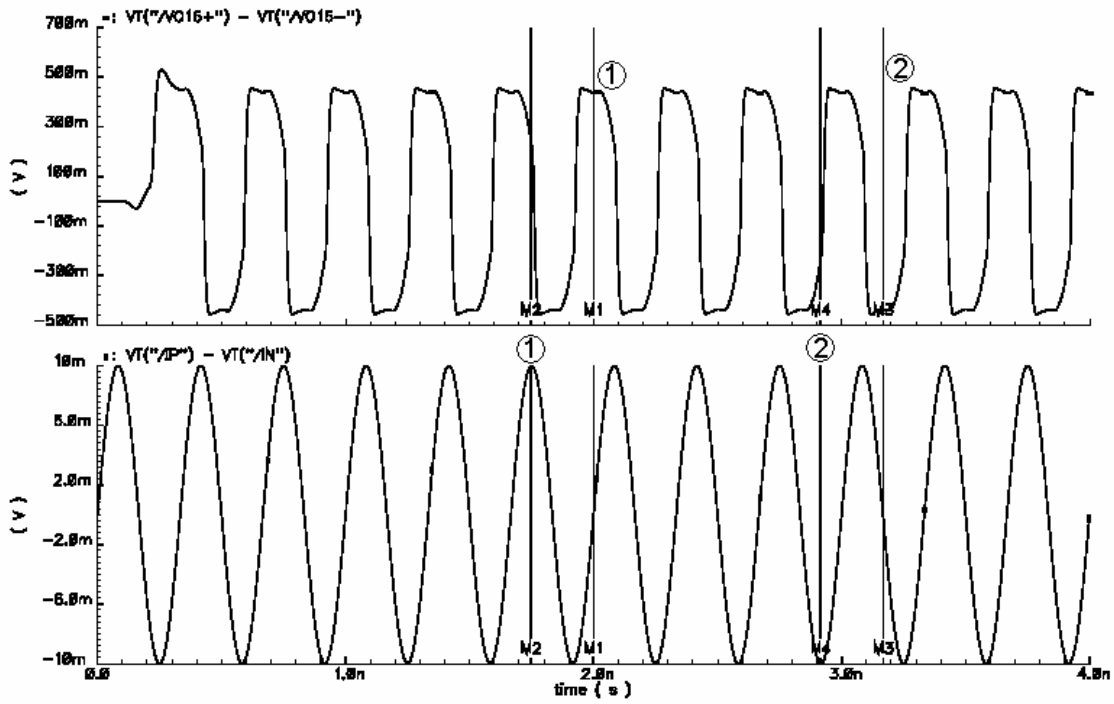

Figure 5.11: Output of the 16th BEC

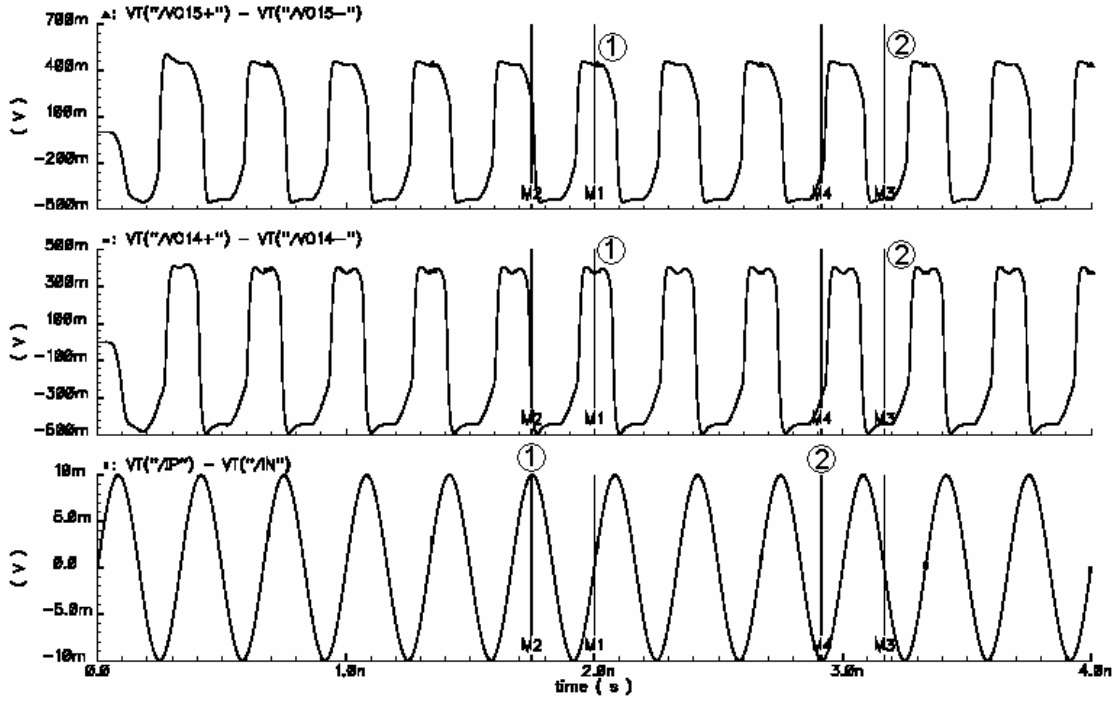

Figure 5.12: Output of the 14th and the 15th BEC

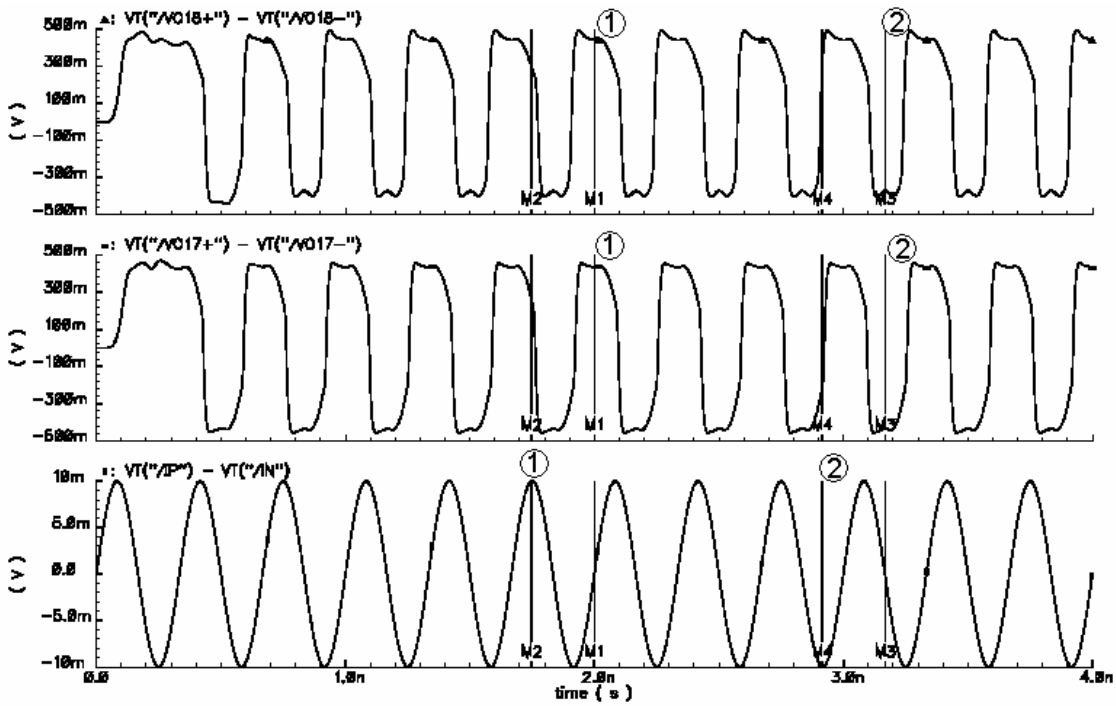

Figure 5.13: Output of the17th and the 18th BEC

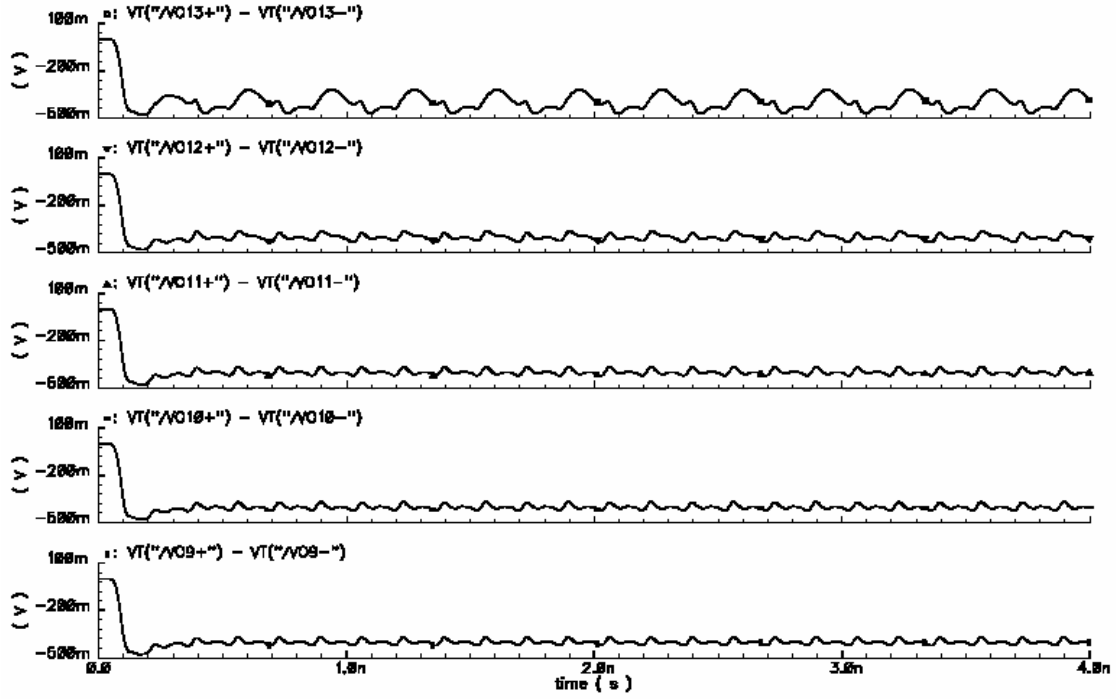

Figure 5.14: Output of the 9th to the 13th BEC

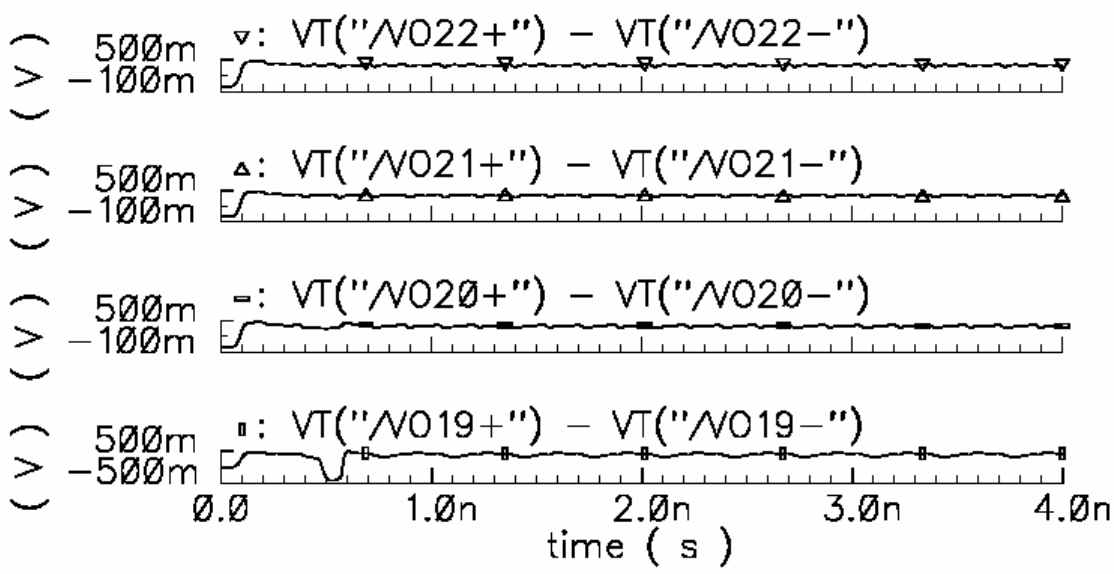

Figure 5.15: Output of the 19th to the 22nd BEC

The basic approach used here to minimize mismatch during layout is symmetry. As shown in Figure 5.1, Figure 5.5 and Figure 5.6, those devices in differential pairs are drawn to be symmetric to each other. Unlike CMOS process in which source and drain can share the same active region, in HBT process, only collector region can be shared. Some emitter followers share the common collector. To minimize signal interference, most of the signal lines use high-layer metals (Metal 3 and Metal 4). Also signal lines are carefully routed to minimize parasitic capacitances.

By adding the thermometer-to-binary encoder after the BEC stage, the final digital output of the flash ADC can be generated. The final layout occupies an active area of 2.1 mm × 3.3 mm. INL and DNL can be measured with a low-frequency sine wave as the input. Here a low-frequency sinusoid at a conversion rate of 1 GHz is used. The simulation shows that the DNL is around 0.6 LSB and the INL is around 0.8 LSB. SNR measurement can be done at a constant frequency. Sweeping the entire amplitude range, for example, from zero to full scale and vice versa, produces large deviations from the source signal, as source amplitude approaches the converter's full-scale limit.

The measured SNR is around 28 dB. Table 5.4 summarizes the performance of the final flash ADC design.

Table 5.4: Performance of the flash ADC

Performance Metrics	Simulated Results
Maximum operating frequency	6 GSample/s
Resolution	5-bit
Active area of the analog part	0.7 mm × 3.3 mm
Active area of the complete ADC	2.1 mm × 3.3 mm
Supply voltage	3.3 V
Power consumption of the analog part	4.88 W
DNL	0.6 LSB
INL	0.8 LSB
SNR	28 dB

CHAPTER 6

CONCLUSIONS

In this thesis, two types of the master-slave comparators and the analog part of a flash ADC have been presented. All the circuits are built using SiGe HBT technology to achieve high speed of operation. The circuits are all operate in gigahertz range; therefore, they can be used in Ultra-Wideband communications.

Flash-type ADCs are possibly the fastest analog-to-digital converters. But its performance strongly depends on its constituent $2^N - 1$ comparators. Since the number of comparators used in a flash ADC increases exponentially with the resolution of the ADC, flash-type ADCs can only be built with low or moderate number of bits of resolution. The speed of operation, the power consumption and the area of the comparators employed directly influence the performance of the ADC. Therefore, a lot of attention should be paid to the design of the high-speed comparator. Especially, the trade-off between the operating speed and the power consumption must be considered very carefully.

Two types of master-slave comparators are presented in Chapter 3. The main difference between them is the bias scheme. Master-slave structure is used to improve metastability behavior of the comparator so that the minimum input difference of the comparator can be lowered down, which can make the design of a flash ADC with moderate resolution possible. Both of the comparators presented can work with sampling speed of 16 GHz with post-layout simulations. The active areas of the two comparators are quite small in the test chip layout and the power consumption for the comparators is moderate. Probably the most stringent test for a comparator is the

overdrive recovery test. Both of the master-slave comparators designed pass the overdrive recovery test with clock frequency of 16 GHz.

The comparator presented in Section 3.3 is a standard design. Comparator design trade-offs have been carefully considered to achieve best design for this comparator. Presented in Section 3.4 is an improved master-slave structure where a different bias scheme is used. The preamplifier stages in the master comparator and the slave comparator share the same bias current source, while the latch stages from the master comparator and the slave comparator share the other. Traditionally, the master comparator uses a bias current source while the slave comparator uses the other. The improved bias scheme can give rise to the optimum bias condition in master-slave comparators in term of regeneration time constant and power dissipation. Therefore, the master-slave comparator with the improved bias scheme is used in the design of the flash ADC presented in Chapter 4.

The analog part of a flash ADC has been presented in Chapter 4. Based on the master-slave comparator built in Chapter 3, the flash ADC works with sampling speed of 6 GSample/s and resolution of 5 bits. A track-and-hold amplifier is added before the differential resistive-ladder of the flash ADC to improve its dynamic performance. Also since the ADC operates with a sampling speed in gigahertz range, it increases the requirements on the sampling circuit with respect to sampling jitter, which makes the introduction of a track-and-hold amplifier almost necessary. The track-and-hold amplifier is designed for more than 5-bit linearity with the highest possible bandwidth. A bubble error correction logic circuit is added after the slave comparators, by which, each thermometer code is examined and amplified relative to its two nearest neighbors based on a voting process, and the output is corrected if it disagrees with both. The

final stage is the 2^N-to-N thermometer-to-binary encoder which generates the digital output. Gray code is used as the intermediate code to enhance encoding performance because Gray code can lower the probability of metastable states from the comparator and reduce the effect of sparkles.

The performance of the master-slave comparators and the high-speed flash ADC has been tested in Chapter 5 where the simulation results are presented. The functionality and their correctness of operation have been examined. The simulation results verify that the flash ADC designed in Chapter 4 operates correctly with a very high speed of 6 GSample/s.

The objective of this thesis has been met. The high-speed flash ADC designed can be used in UWB Communications area where high sampling rate circuits are required.

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