HIGH PERFORMANCE CONTROL OF VRM CIRCUITS

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NATIONAL UNIVERSITY OF SINGAPORE

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All praise belong to Him alone.

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SUMMARY

Voltage Regulator Modules (VRM), which are used to power advanced microprocessors, have stringent efficiency and transient response requirements. The multiphase buck converter scheme is a popular topology for use in this application because of its ability to handle large load currents and to achieve fast dynamic transient response under large step-load conditions. However, its various advantages are compromised should a significant current unbalance occur either under steady-state or transient conditions among the different phases of the circuit. The first part of this thesis fully investigates this issue for three popular control schemes used currently: Voltage Mode Control (VMC), Average Current Mode Control (ACMC), and Peak Current Mode Control (PCMC).

The concept of critical inductance plays an important part in analyzing the dynamic performance of the converter with each of these schemes. The critical inductance can be defined as the largest inductance capable of achieving the fastest transient response for a given load transient. Analytical results are presented in this thesis which allows one to estimate accurately the critical inductance value for the three control schemes. Simulation results have also been provided to confirm the analytical results.

Among the three control schemes, the VMC was found to be the simplest since only the knowledge of the output voltage is needed for implementing the control scheme. Furthermore, in the multiphase converter, the output voltage ripple frequency in considerably increased using the interleave technique. This allows a higher overall system bandwidth to be realized with the VMC scheme as compared to the current

mode control schemes. This has been shown in this work to improve the converter transient response. However, due to the absence of any control over the inductor current, it is also shown that large current unbalances can occur in practice due to component parameter variations. On the other hand, it has been demonstrated that the ACMC and PCMC schemes ensure accurate load sharing between the phases of the converter both during transient and steady state. Among the two current control schemes, the overall bandwidth with the ACMC scheme is significantly lower than that obtained with the PCMC scheme and this results in slow operation of the converter during load induced transients. Thus, it is shown in the first part of the thesis that in modern VRMs where equal current sharing between phases and good dynamic performance are essential, the PCMC scheme is the best candidate.

A critical bottleneck in realizing VRMs with the PCMC scheme is the need for a small, efficient and accurate current sensor for sensing the instantaneous current for implementing the peak current mode control. The second part of the thesis focuses on this topic.

The thesis contains a detailed investigation of current sensing schemes that can be used for current mode control of VRMs. The resistive current sensing scheme is generally popular and used for PCMC schemes. This may be attributed to its accuracy and large bandwidth and also due to its ease of use. However, it can lead to increased losses especially due to the low output voltages involved. Other available current sensing methods for DC-DC converters are also not shown to be very suitable.

In this thesis, a novel current sensing technique capable of high performance based on current transformers is proposed. Current transformers are generally not used in DC-DC converters due their inability to sense DC current. Nevertheless, in this thesis, it is shown that by placing the current transformers at appropriate locations,

the lost DC component can be recovered through simple signal processing. The proposed scheme exhibits much higher efficiency than the classical current sense resistor. Besides, if properly designed, the high accuracy and the high bandwidth of the proposed current sensing method allow its use in PCMC schemes. The design issues regarding the novel current sensing method when used in multiphase converters are also covered in this thesis. The requirements and the obtainable accuracy of the proposed current sensor are in particular investigated.

Finally, experimental results on a step down buck converter, controlled in PCMC using such a sensor, are provided to confirm the sensor's performance and suitability with PCMC scheme. The proposed current sensing technique can also be applied to several other types of power converters besides the multiphase buck converter.

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CHAPTER 1

INTRODUCTION

1.0 Background

With advances made in Very Large Scale Integration techniques (VLSI), the microprocessor has continuously gained in speed and compactness over the past 40 years. As predicted by Moore's law, the number of transistors in a single chip has consistently increased over this time period in an exponential way [1]-[2] (see Fig. 1.1). The current Pentium 4 contains several million transistors, and Intel is even planning to reach the billion transistor mark for the next generation of the processor.

However, with the multiplication of the number of transistors integrated into the microprocessor, the power requirements of such an IC have also shot up [3]-[4]. The dramatic increase in the power required to drive the microprocessor may be seen from Fig. 1.2.

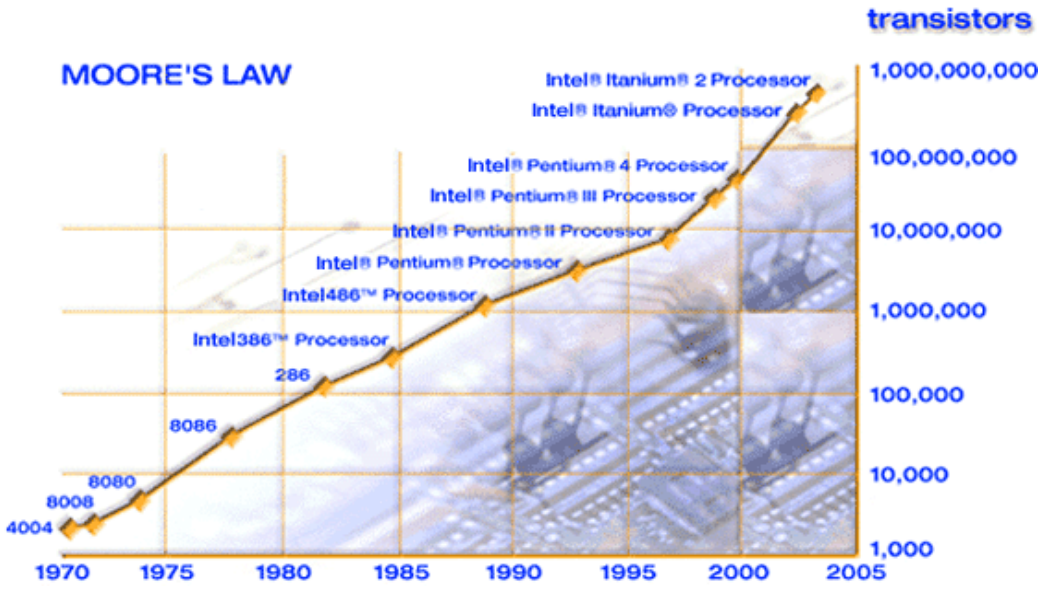

Fig.1.1 Exponential increase of the number of transistors integrated in a single chip (http://www.intel.com/technology/silicon/mooreslaw/)

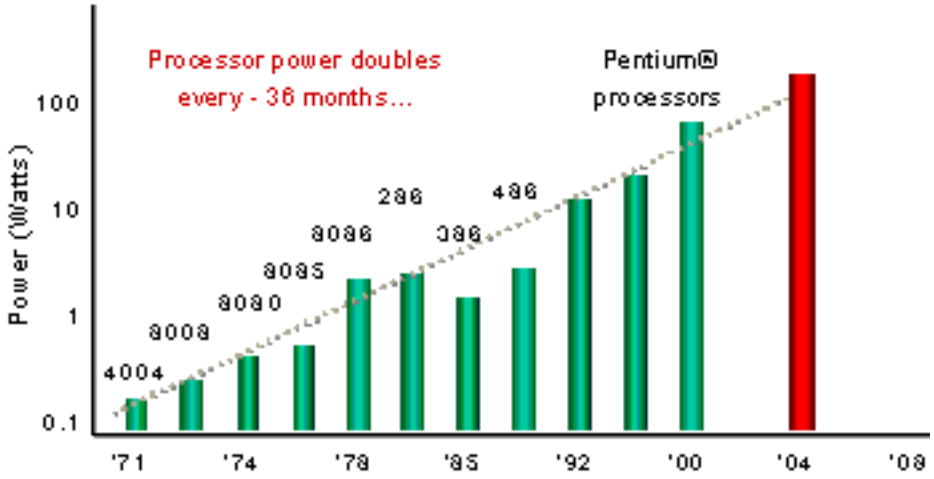

Fig.1.2 Evolution of power consumption in the microprocessor [5]

As may be noted, the current high speed processor is consuming more than a hundred watts of power and this may be compared to the low value of only several milli-watts dissipated in the early days. At the same time, current CPUs are also demanding an increasingly superior performance, such as ability to handle very fast current transients within a very tight voltage tolerance.

Indeed, for the CPU to work, a constant voltage V_{cc}, called core voltage has to be applied across it. Initially, V_{cc} was fixed at 5 V. However, with a large clock frequency f_{clock}, the dynamic power loss P_L can become substantial since

$$P_L \propto C_L V_{cc}^2 f_{clock}, \tag{1.1}$$

where C_L is the capacitive loading of a single CMOS cell [6].

Consequently, to limit this power loss, and thereby the heat stress on the CPU, the core voltage has been considerably decreased in recent years, as shown in Fig. 1.3(a). In today's Pentium IV, the core voltage is kept to a range of 0.8 V to 1.8 V, and this trend of decreasing core voltage is expected to continue. Furthermore, the smaller voltage goes with an even tighter tolerance band, as shown in Fig. 1.3(a). The tolerance band was 5 % for the 3.3 V-Pentium II, whereas it has been reduced to only 1.2% for the current 1.8 V-Pentium IV [6].

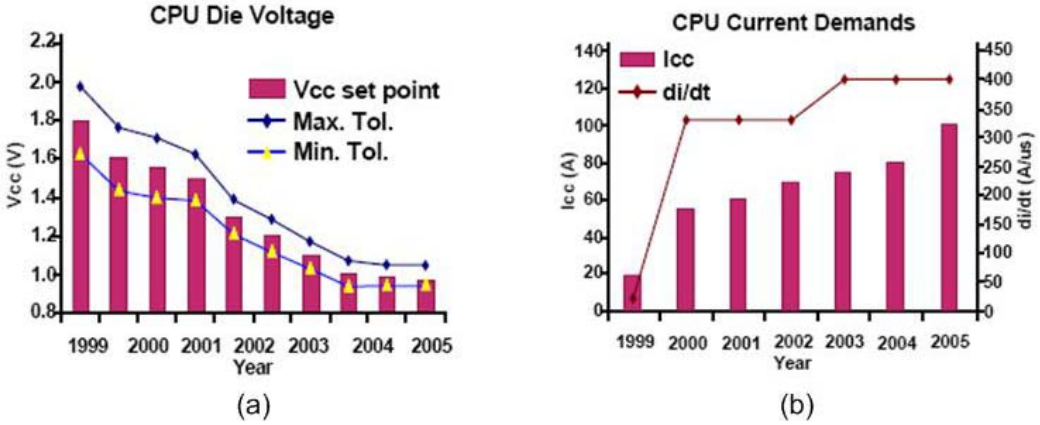

Fig.1.3 Intel roadmap of the 32-bit CPU load at CPU-system connector [5]
(a) CPU die voltage
(b) CPU current demands

Hence, the microprocessor has become increasingly sensitive to voltage fluctuations requiring the core voltage to be controlled within a tight window, should a load perturbation occur.

Moreover, since the required power to drive the CPU is considerable, reduction in core voltage means a significant increase in the demanded current, as shown in Fig. 1.3(b). In today's CPU, the peak current demand is as high as 120 A, and this value may even reach several hundred amperes in the next generation processor [4], [5]. This complicates the circuit design and thermal management very much, since even low values of parasitic resistances in the circuit will lead to significant power loss [3], [5].

Meanwhile, another aspect of modern day CPUs is their power adaptability to the working load. Indeed, in order to comply with new environmental rules such as "Energy Star" norms, and/or extend the battery life for laptops, modern CPU goes through different power stages depending on the running task [7], [8]. Therefore, the performance is maximized while the expenditure of energy is minimized. Microprocessors, which used to work either fully or not, have been replaced since

1989 by new processors, in which parts of them are able to go into a sleep mode, when not used [7]. In such a processor, both the voltage to be supplied, and the current drawn, vary according to the load. In fact, the microprocessor acts as a variable current sink requiring a specific and adjustable input voltage, V_{cc} [9]. The desired reference voltage V_{ccref} is communicated to the supply via a number of bits called 'Voltage Identification' (VID).

However, as mentioned earlier, the power loss is proportional to V_{cc}^2 and the clock frequency. In spite of the fact that the core voltage varies with the power level, it is still kept low and within a relatively small range (for example, from 0.8 V to 1.8 V in the current Pentium IV). Consequently, the power saving scheme results mainly in large variations in the current drawn by the processor. In the present day processor, the load varies thus from a few amperes to 120 A [9]. Moreover, this new CPU architecture comes with an expected high speed performance. Thus, the user expects his computer to be able to recover from standby quickly, or even to switch in no time from a relatively non-power consuming task, such as writing a memo, to a higher demanding application such as playing a movie from a hard disk. It is therefore required for the CPU to toggle between two different power stages in a very rapid manner. As a result, manufacturers have designed today fast reactive CPUs, where the current drawn can vary suddenly over a magnitude of 100 A, with a rate which may be as high as 930 A/μs [9].

Hence, to summarize, depending on the running task, the microprocessor draws or switches off a huge amount of current from its power supply in a very short period of time. Usually, the power supply does not react that fast, and though a considerable number of high frequency decoupling capacitors are connected across the CPU, large variations in load current still cause significant disturbances in V_{cc}, which may lead to

system failure. Nevertheless, modern processors allow the voltage to exceed the tolerance band within certain boundaries for a short time period. But this transient time period is relatively small, and the transient voltage range is also low. For example, these values are, respectively, less than 25 μs and 50 mV in the current Pentium IV [9]. Therefore, a fast power supply is required so that the core voltage perturbation during a step load is contained within the tight window fixed by processor requirements.

To help in this task, most of today's processors have adopted the Adaptive Voltage Positioning (AVP) method, where V_{cc} varies depending on the load (Fig. 1.4) [9]. Here, the final V_{cc} voltage presented to the microprocessor is lower than V_{ccref}, with the difference varying according to the load as shown in Fig. 1.4. This difference can then be used to limit the voltage jump or drop beyond the allowable limits during the load transients. The voltage perturbation amplitude is hence considerably reduced, as is the settling time (Δt) during step load, as can be seen in Fig. 1.5. Different methods exist to implement such a scheme and are commonly used in today's CPU power supply [10]-[16].

Therefore, to summarize, the CPU power supply of today must be able to identify the VID codes, continuously sense the load current, deduce from Fig. 1.4 the correct core voltage to be supplied, and finally manage to present the desired voltage in spite of large load variations within a tight settling time of 25 μs for the current Pentium IV. The CPU power management has thus become increasingly complex and stringent. As a result, a dedicated module, called a Voltage Regulator Module (VRM) is needed to control accurately and rapidly the core voltage in spite of large load variations, or other disturbances. In the following, before investigating the VRM in detail, the overall power delivery architecture is first presented briefly.

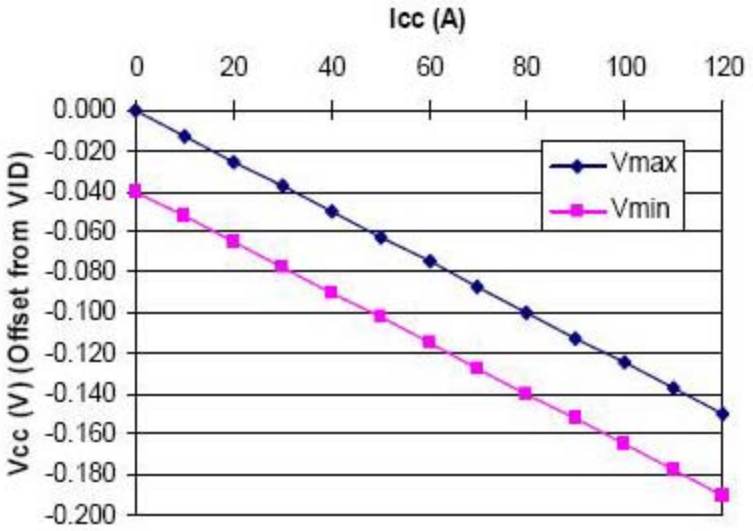

Fig. 1.4 Processor equipped with AVP load line [9]

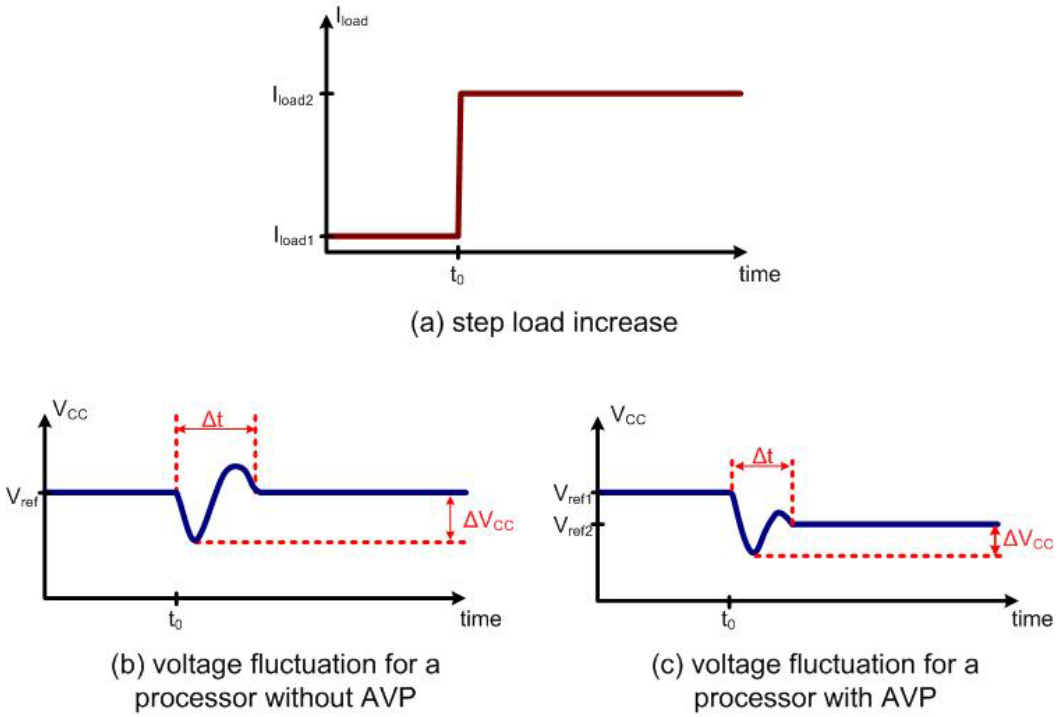

Fig. 1.5 Comparison of voltage fluctuations during a step load increase between processors with and without AVP

1.1 Computer power delivery architecture

The power delivery architecture used to be relatively simple in the early days. The 110 V or 220 V main AC source was simply converted via a “silver box” to a fairly constant 5 V. The microprocessor and all the other electronic systems were then drawing power directly from this 5 V plane present in the motherboard [5].

However, with the increase in the number of peripherals in the computer, besides the power demand rising tremendously, the different peripherals also require different voltage inputs. Hence, in today’s PC, typically, three different voltages are supplied by the silver box; 3.3 V, 5 V and 12 V. The 3.3 V and 5 V output are usually used by the digital circuits, while the 12 V is used mainly to run motors in disk drives and fans. A forward converter fed from an AC to DC front end rectifier is commonly used in these cases.

Due to the stringent voltage requirements and large load variations, a dedicated DC-DC converter called Voltage Regulator Module (VRM) is used to regulate the voltage supplied to the microprocessor from one of the silver box output. The 5V output was initially used for this purpose until the Pentium IV and its equivalents were introduced. With the dramatic increase in the power delivered to the CPU, the distribution loss in the 5 V bus was becoming increasingly significant. Therefore, to reduce this additional loss, the source voltage of the VRM has been switched to the higher voltage of 12 V, also available at the output of the silver box. This power delivery architecture presented in Fig. 1.6 is the most commonly used in today’s desktop [17].

Nevertheless, to reduce further the loss in the 12 V voltage bus, the industry is currently considering switching to an even higher voltage of 48 V in the next

generation microprocessors, including multi-processor system. In such a case, the silver box will deliver only a constant DC voltage of 48 V. Each peripheral will then be preceded by a dedicated DC-DC converter, which will convert the applied 48 V into the required voltages [18]-[19].

In the laptops, heat management is a major concern. Here, the silver box is substituted by an AC/DC adapter placed outside and delivering only one DC constant output voltage in the range of 14 to 18 V. Different DC-DC converters are then placed inside, to convert this voltage into other suitable voltages as needed.

This thesis will mainly focus on the microprocessor voltage regulator module. The constant 12 V output delivered by the silver box will be considered for the VRM source. In the following, an introduction to VRM topologies is presented.

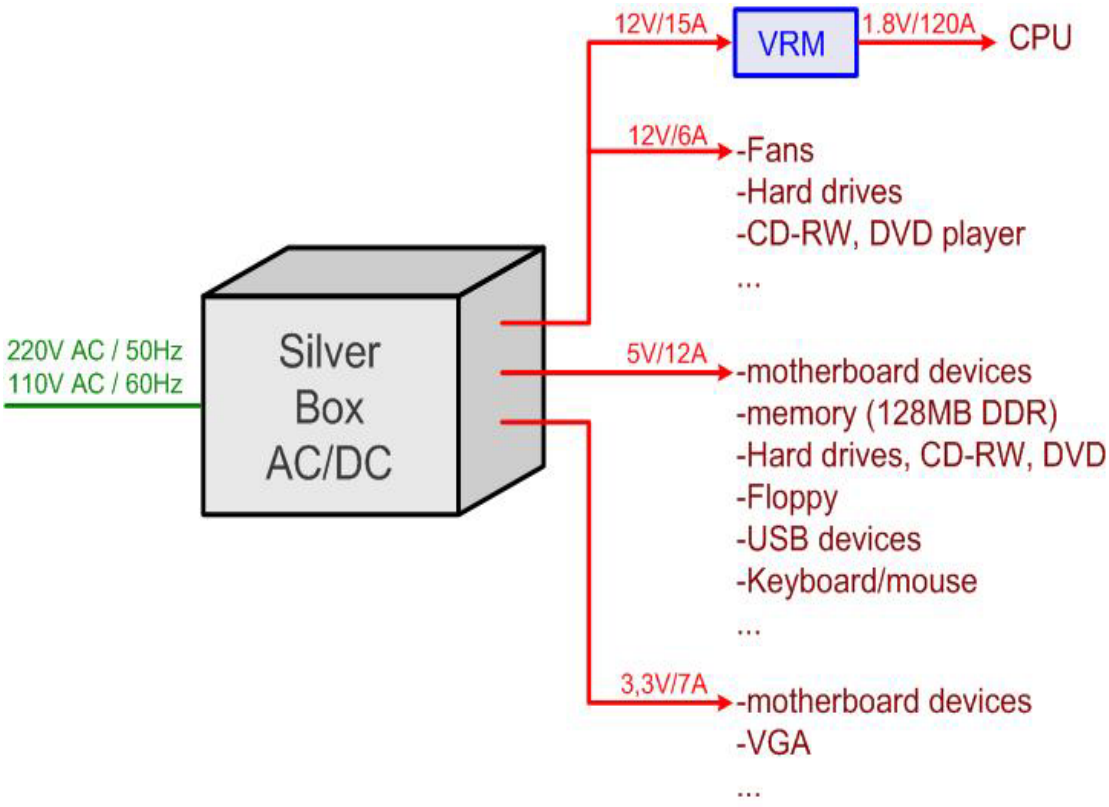

Fig. 1.6 Power system architecture commonly used in current desktops
The current values shown are estimated based on AMD technical documents.

1.2 VRM topologies

From the power requirements for present-day microprocessors given by Intel [9], as seen earlier, today's VRM has to be accurate with fast response, and be able to accommodate large changes in load current in a very short time without great disturbance in the V_{cc} voltage. Also, the VRM is placed in close proximity to the microprocessor, in order to minimize the parasitic inductances and resistances which affect greatly the transient characteristics [20]-[22]. Since the motherboard is limited in space, the VRM has to be small in size. Last but not least, to comply with tight regulation regarding energy saving, efficiency is an essential criterion that modern VRMs have to take into account.

From the early days, buck converter topologies have been widely used in VRMs, since they meet most of the above requirements in terms of efficiency, size, and control. Fig. 1.7 shows a conventional buck converter feeding a current-sink-modeled CPU [23]. The converter consists of two stages. In the first stage, a switching circuit connects the indicated point A to the source or to the ground. Since the current in this circuit loop has high *di/dt*'s due to the switching, the inductance in the loop should be kept as small as possible [24]. In the second stage, there is an LC low pass filter which is designed to pass only the average of V_A to the load. By turning on the MOSFET Q_1 during a fraction d of the period, called duty cycle, and turning off during the rest of the period, the voltage across the load can ideally be maintained to be $V_{in}.d$, with a small ripple depending on L and C values. The load voltage is thus directly controlled by adjusting the duty cycle. If the inductor current does not hit zero in a period, the circuit is said to work in Continuous Conduction Mode (CCM). Besides, in the VRM, the power supply for the control box is derived directly from the 12V or 5V plane present in the motherboard [15], [16].

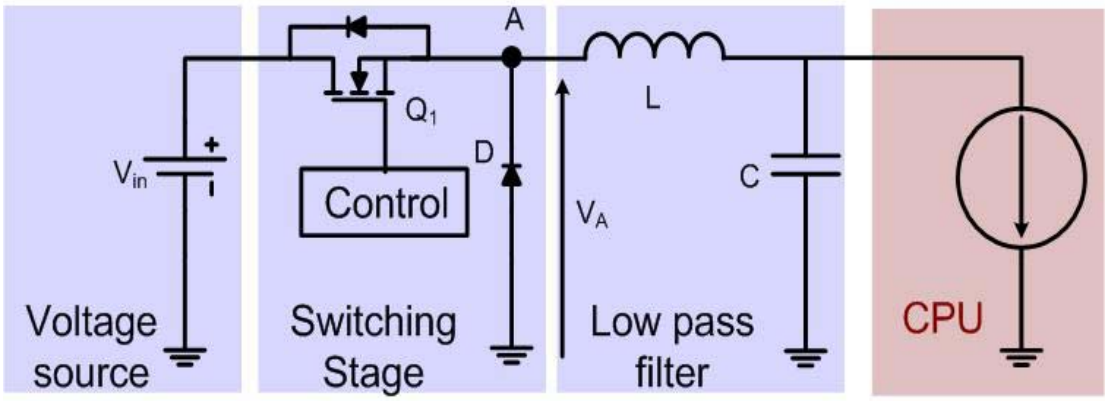

Fig.1.7 Conventional buck converter

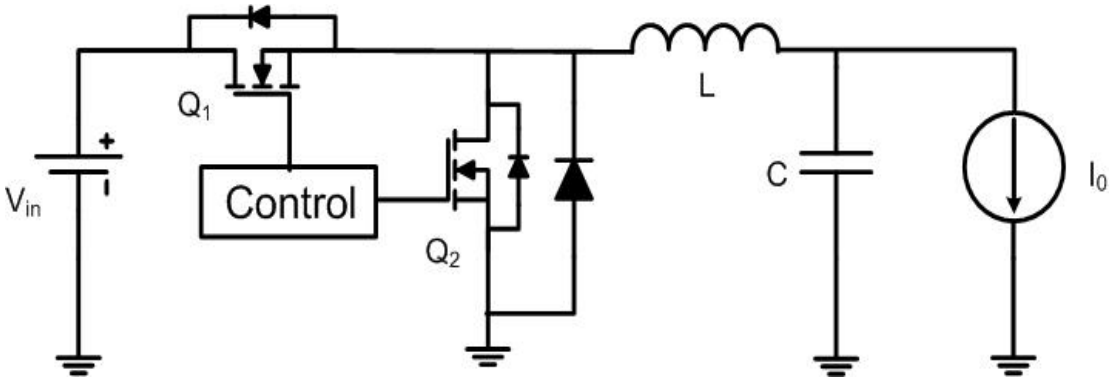

Fig.1.8 Synchronous buck converter with fast recovery diode

However, VRMs are expected to carry a large amount of current, which leads to significant diode power loss in the conventional buck converter. For this reason, the synchronous buck converter, where the diode is replaced by a MOSFET as shown in Fig. 1.8, is preferred in a VRM [4] ,[25]-[26]. In such a scheme, Q_1 is called the high side or the control switch and Q_2 is called the low side or the synchronous switch. Also, the presence of Q_2 allows a negative current to flow through the inductor, which avoids the discontinuous conduction mode (DCM) of operation [23]. Therefore, the output voltage is proportional to the input voltage and the duty cycle even under very low load.

In practice, a MOSFET takes a finite time to turn on or off. Hence, to avoid a short circuit across V_{in} during switch transitions, a dead-time has to be provided before turning on Q_2 or Q_1, during which the inductor current flows through the internal diode of Q_2. Due to the usual poor characteristics of this diode, a fast recovery diode or Schottky diode is commonly placed in parallel, as shown in Fig. 1.8.

This topology was widely used in VRMs, until the introduction of Pentium III and its equivalents. Indeed, in that processor, the operating voltage was drastically reduced from 2.5 V to 1.5 V, and the tolerance band was decreased from 85 mV to 75 mV. Also, the current to be supplied was increased to a larger value of 30 A instead of 10 A, and its slope could attain 8 A/ns instead of 1 A/ns [27]. With such tight steady state and transient requirements, the design of a suitable synchronous buck converter became highly problematic [4], [26]-[27]. The reasons will be explained in the following.

First, with a large load current, the stress endured by each component in the converter is considerable. The power loss in the switches becomes significant; the inductor size also becomes greater with the increase in current [23], [28].

Secondly, the dynamic and steady state requirements of the microprocessor lead to contradictory design choice for the inductance value. Thus, during a load transition, as VRM is inherently slow, the current is first provided by the output capacitors, causing a voltage fluctuation. In response, the VRM has to charge or discharge the capacitor so that the default reference voltage could be met. However, the charging or discharging current I_L flowing into the capacitor has its slew rate limited by the output inductance. Fig. 1.9 shows a typical inductor and load current waveforms during transient.

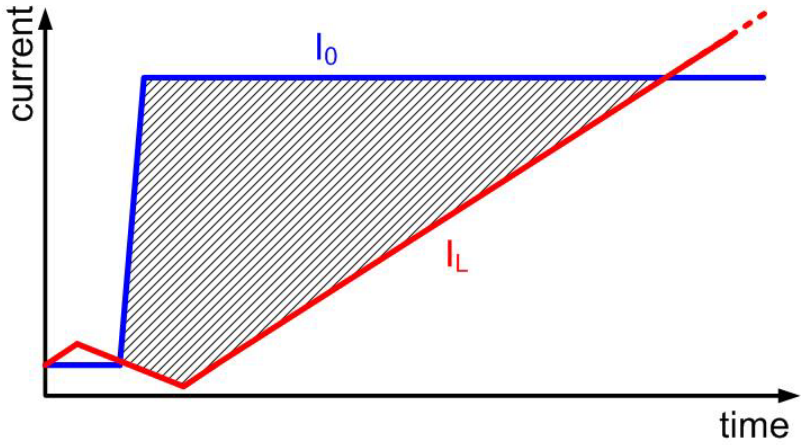

Fig.1.9 Large unbalanced charges during load transient

As can be seen in that figure, the difference between the inductor current and the load current during transient causes vast imbalance in the charge that has to be provided by the output capacitor. The inductor current will generally rise beyond the load current value in order to compensate the capacitor discharge, and to recover from the output voltage deviation caused by the discharge from the capacitor. Hence, by decreasing the inductance value and therefore increasing the inductor current slope, both the settling time and the output voltage deviation can be reduced. But, a small inductance leads to high current ripple, which increases the switching loss. Furthermore, with high current ripple, the capacitance required to keep the voltage ripple within the small window allowed by the processor can also become considerable. Such high value capacitors are large in size and the motherboard real estate is expensive.

As it was getting impossible to meet the microprocessor's requirement using classical methods without increasing the VRM size greatly, a new topology was needed for future processors. In 1999, a novel VRM, called multiphase interleaved converter [4], [20]-[22], [27], [29]-[33], was utilized to power the new Pentium III. Such an n-phase interleaved converter is shown in Fig. 1.10.

In this scheme, in order to reduce the increased current stress endured by each converter component, several complete buck converter modules are paralleled, as shown in Fig. 1.10. In each module, called a channel or a phase, the inductance is chosen to be the same, and as in a classical buck converter each inductor carries a triangular shape current. Through appropriate control, these waveforms are phase shifted in such a way that the ripple in the overall current I_0 is reduced, as can be seen in Fig. 1.11 for a two phase converter.

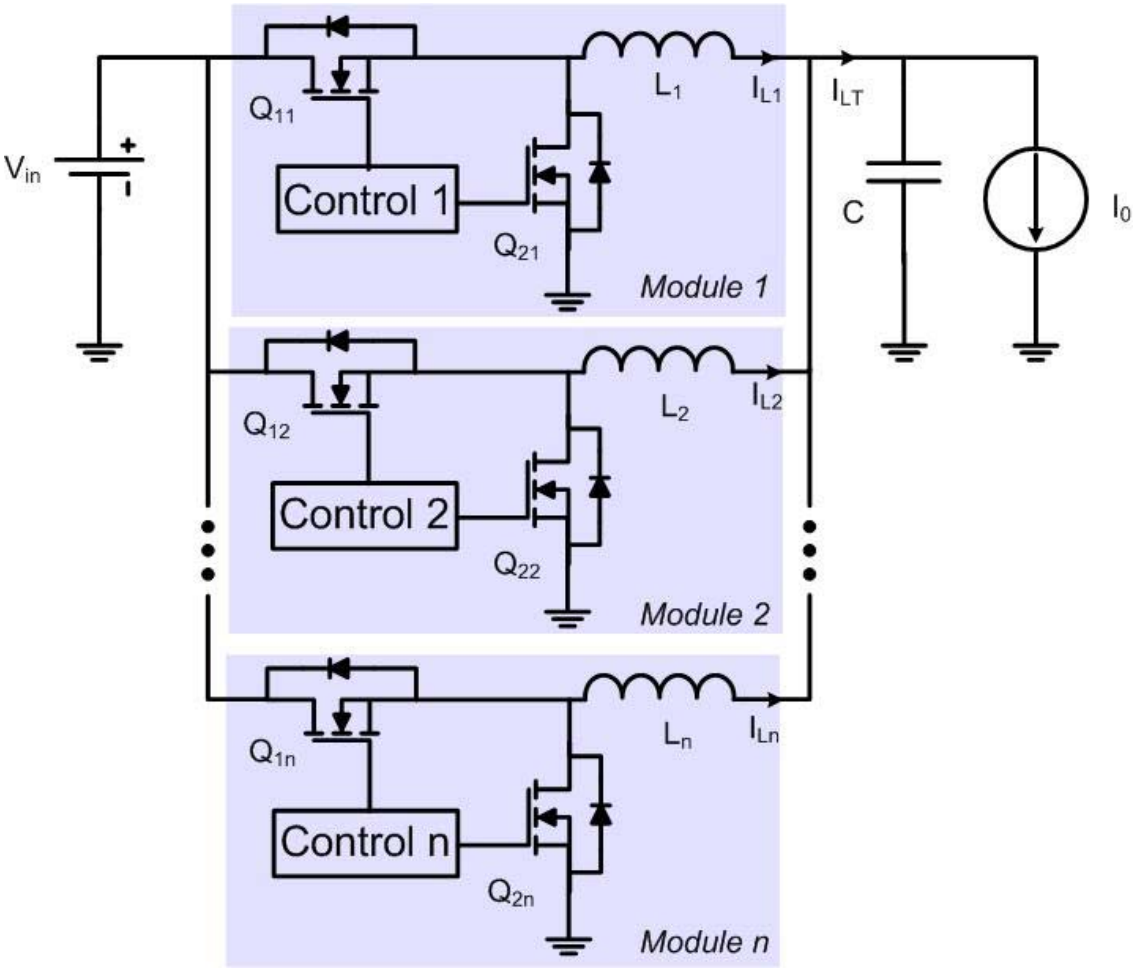

Fig. 1.10 n-phase interleaved converter

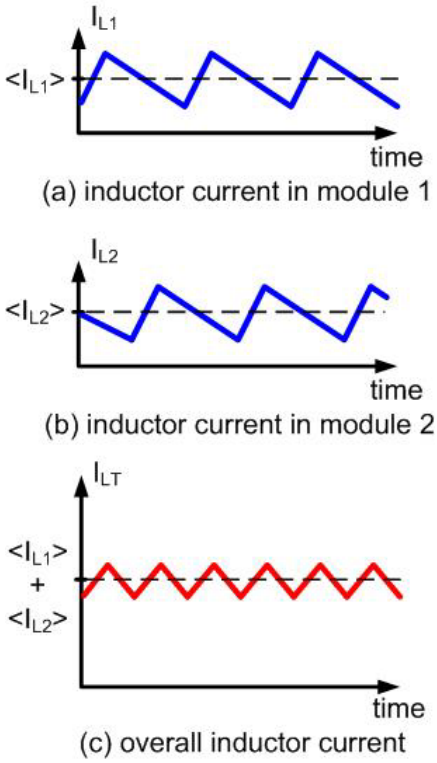

Fig. 1.11 Each inductor and overall inductor current in a two phase buck converter

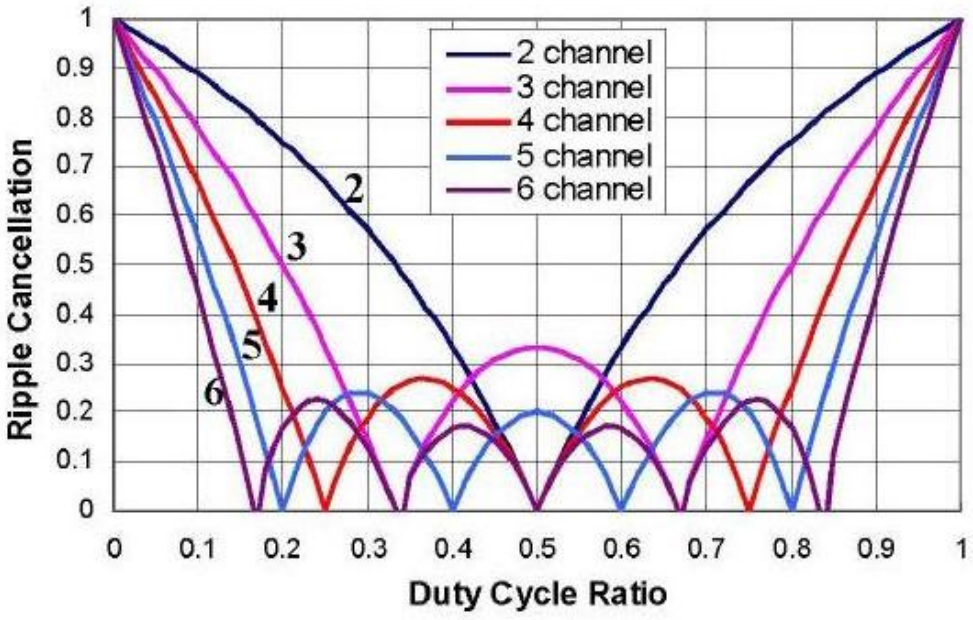

Fig. 1.12 Overall current ripple cancellation for a 2-6 phase buck converter [34]

Hence, a smaller inductance value can be chosen when compared to a single phase VRM, without increasing the overall current ripple. Besides, the use of several modules helps to spread the power dissipation, and hence facilitate the heat management, which is critical in motherboards. Finally, the phase shift in the control offers the additional advantage of increasing the fundamental frequency of the overall inductor current, I_{LT}. Therefore, as a side benefit, a smaller capacitor can be selected for the same voltage ripple, reducing in a way the VRM size. Though it requires more space and components, the multiphase topology presents an affordable solution for present day and future processors.

The ripple reduction depends actually on the number of phases and the operating duty cycle, as shown in Fig. 1.12 [34]. Currently, the steady state duty cycle is around 0.16. Therefore, a six phase converter may be used to minimize the current ripple. However, four channel interleaved converters are presently widely used, as a compromise between cost, size, and efficiency [35]-[36]. Yet, for the next generation of processors, a higher number of phases will most likely be selected to cater to the constant increase in power requirements.

One of the important issues in this topology is the load current sharing among the phases [32]. Indeed, should a current unbalance occur among the channels, the system will become less effective, and the steady state and transient characteristics of the system will greatly suffer. Hence, in present and future VRMs, in which the power and heat management is getting to be increasingly critical, a current sharing process must be included in the control scheme.

Another difficulty in using this topology is with regard to its size. In order to reduce the space occupied, the different inductances of the multiphase converter may be integrated into one unique core [34]-[35], [37]-[39]. In such a circuit, called the

multiphase coupled converter, the mode of operation is completely changed, since all the inductors are coupled together. Nevertheless, the coupling may be optimized so that it offers several other advantages, such as better dynamic response under a load-induced transient, smaller current ripple in each channel, and less inductor core losses. However, the coupled inductor makes the core structure complex, especially when more than two phases are used. Also, phase shifts are no more introduced in the phase inductor currents, which compromises some of the benefits associated with the multiphase structure. Therefore, so far, the normal multiphase converter is still more popular.

Another VRM candidate proposed currently in the literature is the stepping inductance scheme [40]-[42]. It consists of a classical synchronous buck converter in which the filter inductor is replaced by a transformer M in series with an inductance L_r, as shown in Fig. 1.13.

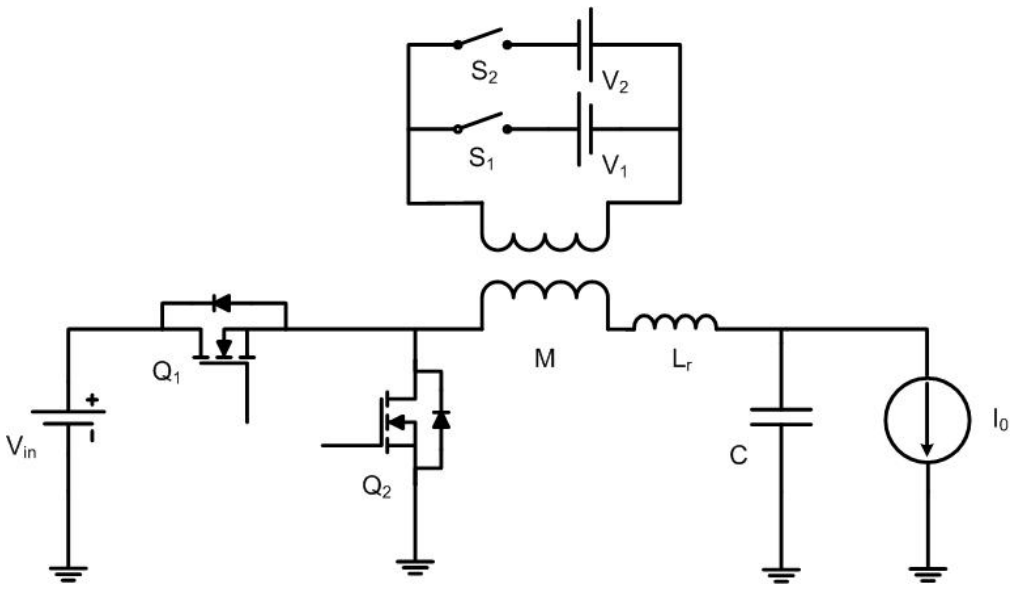

Fig.1.13 Basic configuration of stepping inductance based VRM

The secondary side of the transformer is here connected to the voltage sources V_1 and V_2, through the switches S_1 and S_2. These sources are derived from the supply voltage V_{in} through appropriate arrangement of auxiliary switches and transformer windings, not shown here. Also, L_r, which could be the leakage inductance of the transformer, is chosen to be very small compared to the primary inductance L_1 of M.

In the control scheme given in [42], during steady state, the switches S_1 and S_2 are fully off, so that the output inductance is the sum of L_1 and L_r. Due to this relatively large inductance value, the inductor current ripple is very low, and so is the output voltage ripple. When a large load step occurs, the transformer primary inductance is then shorted by turning on S_1 or S_2. Consequently, the filter inductance is reduced to L_r, and therefore a faster variation in inductor current is permitted. Also, at the same time, the voltage source V_1 or V_2 will charge or discharge the transformer's secondary. The switch S_1 or S_2 is finally turned off only when the resulting primary current would be equal to the current already flowing through L_r, in order to ensure a smooth transition.

Though having fewer components, this scheme's main drawback is the control and circuit design complexity. Also, during transient, the reflected voltage of V_2 or V_1 affects the slope of variation of the inductor current. This must be taken into account in the design of the transformer. Furthermore, usually it takes a long time to charge or discharge the transformer to the desired value. As a result, there is a significant time period, in which the output filter inductor is limited to the very small value of L_r, and hence the current ripple will be very large during this time. To limit the resulting voltage ripple to reasonable values without using large capacitance, a hysteresis current mode control is employed [42]. This control, however, complicates the design of the converter because of the varying switching frequency. Moreover, a highly

accurate and efficient current sensor is needed to sense the inductor current. Consequently, this scheme, though promising, is not yet widely used in VRM.

Therefore, the great majority of today's VRMs use the four phase interleaved converter topology, which is the main focus in this thesis. For more information regarding the stepping inductance system, [40]-[42] may be referred to.

In the following, a brief introduction to the several issues covered in this thesis as well as the scope of this thesis are presented.

1.3 Thesis motivation and outline

The multiphase converter has gained its popularity based on superior power and heat management. The dynamic and steady state requirements of the CPU are fulfilled relatively easily without using bulky capacitors, by simply decreasing the inductance value in each phase, thus, allowing higher current slope. However, during transient, the inductor current's rate of rise or fall does not only depend on the inductance value, but also on the controller characteristics. In other words, below a certain limit, which depends on the selected control scheme, decreasing the inductance value further does not improve the transient response, but only affects the converter's steady state performance including efficiency. In this thesis, ways to optimize the inductor value in order to have the best transient response with minimum steady state voltage ripple will be investigated for the three kinds of control schemes mostly used in today's VRM; Voltage Mode Control (VMC), Average Current Mode Control (ACMC), and Peak Current Mode Control (PCMC). These studies are carried out both analytically and through simulations. The studies bring out the superiority of a PCMC scheme over the ACMC scheme and the currently popular VMC scheme.

Another topic covered in this thesis is current sensors in buck derived topologies for use in high performance control schemes, such as the PCMC scheme. As mentioned earlier, the numerous advantages of the multiphase converter are in fact effective only if the load current is shared correctly among the phases. Therefore, in order to prevent system failures, the converter control circuit must include a current sharing scheme. By controlling directly each inductor current, current mode control offers an easy solution to this load sharing problem in steady state as well as during transients. However, in order to implement a current mode control of maximum bandwidth, a fast and accurate current sensor is needed. Yet, in current sensors for DC-DC converters existing today, accuracy and rapidness come always with a price in cost and efficiency. Therefore, voltage mode control scheme had been preferred in practice, though it results in a poor current sharing. However, given the Intel voltage/current road map, current mode control scheme is gathering popularity, and presently, there is a need for developing high performance current sensors for use in converters such as the multiphase converter. This thesis proposes a novel, highly accurate and efficient current sensing method based on the use of current transformers. Analytical design and experimental studies have been performed on the proposed current sensor technique and on a single phase synchronous buck converter using these sensors.

These different issues will be presented as follows:

- **Chapter 2**: In this chapter, the selection of the different components of the multiphase converter is first presented. The converter equipped with a voltage mode control is then analyzed and a large signal model of the system is proposed. This model will next be used for the design of the voltage controller, and for the inductance optimization. Finally, the complete system equipped

with the optimized inductance is simulated in order to investigate the current sharing among the channels in steady state as well as during step load changes.

- **Chapter 3:** In this chapter, the two most popular current mode controls are investigated: average current mode control and peak current mode control. For each case, a large signal model is derived, the controller design procedure is presented, and methods to optimize the inductance values are investigated. Simulations under maximum load step for each case is also provided to verify and confirm the theoretical results. The results in Chapter 2 & Chapter 3 confirm the potential superiority of the peak current mode control scheme. This also makes the need for an accurate, fast, small, and efficient current sensor for the VRM application apparent.

- **Chapter 4:** In this chapter, a literature survey is conducted on existing current sensors used in DC-DC converters for control purposes. Firstly, the difficulties in sensing the current in actual VRM are presented; then, for each sensor, its efficiency, accuracy and speed of response are investigated. This chapter is actually an introduction to the chapter 5, where a new current sensing method, which overcomes most of the discussed difficulties, will be introduced.

- **Chapter 5:** In this chapter, a novel current sensing technique based on current transformers and capable of high performance is proposed. The requirements and the design of the current transformer to be used are presented. The accuracy of the sensing method is also analyzed. Finally, experimental results on a step down buck converter, controlled with peak current control using such a sensor, are provided to confirm its performance. The proposed technique can also be applied to several other types of power converters besides the multiphase buck converter.

1.4 Thesis Contributions

The major contributions of this thesis are as follows:

- Large signal models of the four phase converter with VMC, ACMC and PCMC have been proposed. These models have been verified using simulation results. The models are useful in the design of the controllers and for an accurate analysis of the dynamic performance of the converter, which will be used later on.
- Critical inductance analyses have been carried out for the system with ACMC and PCMC using the proposed large signal models. Analytical methods to estimate the critical inductance value are presented and these are verified with simulation results.
- A novel current sensing technique based on current transformers and capable of high performance is proposed. Experimental results based on the use of such a sensor in PCMC on a single phase buck converter are also provided.

CHAPTER 2

VOLTAGE MODE CONTROL METHOD

2.0 Introduction

The Voltage Regulator Module (VRM) concept and the multiphase interleaved buck topology have been introduced in Section 1.2. Several ways exist to control such a complex converter, the most popular among them being the Voltage Mode Control (VMC), the Average Current Mode Control (ACMC) and the Peak Current Mode Control (PCMC) [43]-[45]. In this thesis, the design issues regarding these control schemes are investigated and compared for a four phase converter.

The present chapter is mainly focused on the VMC scheme, which offers the advantage of a simpler control structure as opposed to schemes employing current mode control techniques. Moreover, as mentioned earlier, the output voltage, which is the only variable used in the feedback loop in VMC, has an increased ripple frequency due to the adoption of the interleaving method. As a result, the allowable bandwidth is also increased using this control method. However, the scheme's main drawback is the absence of a current sharing feature, as will be shown in this chapter. Therefore, though this control method was popular in earlier VRMs, it is no longer preferred for the current and future VRMs, where the load sharing capability is critical.

The VMC scheme has been investigated in the past, especially the issue of optimizing the control design as well as the system design, in order to have the best transient response with minimum steady state voltage ripple [45]-[48]. However, in most of the cases, the switch resistances are conveniently ignored in the circuit analysis [46]-[48], or arbitrarily added to the resistance of the inductor [45], in order

to be able to derive a large signal model. The limitations of such an approximation are brought out in this chapter, and a more accurate large signal model is proposed. The design methodology, in particular the inductance optimization method, is then investigated in the present chapter for such a control scheme. These analytical methods will be extended for application to the current mode control schemes in the next chapter.

The first part of this chapter discusses issues regarding the selection of the main components to be used in the four phase converter. This part, in fact, is applicable to the VRM module in general irrespective of the control scheme adopted.

Following this, in the second part of the chapter, the implementation of the VMC scheme in the multiphase converter is presented and analyzed. The limitations of the linear model derived by ignoring the switch resistances are particularly highlighted. A more accurate large signal model taking into account the MOSFET on-state resistances and the loss resistances of the inductors and the capacitors is then proposed and verified and compared to other models using simulation results. Using the proposed large signal model, the design of the voltage controller is carried out. The dynamic performance of the converter is then studied for different inductance values. A critical inductance value, for which the transient response is optimized with minimum steady state voltage ripple, is identified. This critical inductance concept is based on that presented in [45]. A method to estimate the critical inductance using the proposed large signal model is presented. The critical inductance estimation method presented in this chapter for the VMC scheme will be extended to the ACMC and PCMC schemes in the next chapter. Finally, the four phase converter equipped with the critical inductance and the designed voltage controller is simulated, and its current sharing capability discussed.

2.1 Selection of power stage components

In this section, the selection of the various components, as well as the choice of the switching frequency in the multiphase converter, are briefly discussed.

2.1.1 MOSFET selection

By supplying and regulating the power to the load, MOSFETs are playing a key role in the switching converter. Their characteristics affect directly the performance of the converter, and they account for more than 50% of the power dissipation in the overall module [49]. Therefore, they should be carefully selected when used in VRMs, and always suitable thermal management is needed for these components.

For this purpose, the power losses in the switches in the multiphase converter are briefly analyzed and estimated here. The power dissipation in the MOSFET can be divided into several main categories [49]-[51]:

- Conduction loss: this power dissipation occurs when the MOSFET is fully conducting; it can easily be estimated by approximating the MOSFET to a resistance during the on-state.
- Switching loss: this loss occurs during the MOSFET transition from one state to the other due to a positive drain source current flowing in the switch while the drain source voltage is not equal to the on-state voltage.
- Diode conduction and recovery loss: this loss is particular to the low side switch, in which the internal body diode conducts during the dead time.
- Gate loss: this loss represents the energy to be supplied by the driver to switch each MOSFET effectively.
- Output parasitic capacitance loss: this loss is caused by the output capacitance of the MOSFET discharging through the MOSFET channel during turn on.

Considering one channel with the upper MOSFET Q_1 and the lower MOSFET Q_2, these power losses can be directly approximated using the equations presented in Table 2.1 [50]-[51]. It can be noted that these losses are in fact different for Q_1 and Q_2. Firstly, since the steady state duty cycle D is close to only 15%, the conduction loss is more significant for Q_2 than for Q_1. Secondly, the internal diode of Q_2 conducts during the dead time. As a result, there is a natural Zero Voltage Switching (ZVS) for Q_2, and therefore its switching loss is considerably reduced compared to Q_1. However, this diode conduction also brings additional losses depending on Q_2 characteristics. As a consequence, since the power loss expression depends on the MOSFET's position in the phase, each one of the two switches is required to have different characteristics for efficiency maximization.

Hence, in the selection of Q_1, the switching loss is particularly taken into consideration. Therefore, MOSFET with low gate to drain charge Q_{GD} and gate to source charge Q_{GS}, both normally indicated in the datasheet, is preferred for the high side position. Furthermore, with low Q_{GS} and Q_{GD} values, fast switching can be achieved, which is also required for Q_1, since the conduction time is very low. However, this kind of MOSFET comes with an increase in the on-state resistance R_{DSon}, and therefore, a compromise between conduction loss and switching loss has to be made.

As for Q_2, with its zero voltage switching, reducing the conduction loss is the main priority. Consequently, a MOSFET with very low on-state resistance and reasonable Q_{GS} and Q_{GD}, is preferred for the low side position. Additionally, if a Schottky diode is not used in parallel, the reverse recovery charge Q_{rr} may also be considered in order to limit the diode recovery current flowing through Q_1.

TABLE 2.1 POWER LOSS EVALUATION FORMULAS FOR A SYNCHRONOUS DERIVED CONVERTER

		High Side Switch Q_1	Low Side Switch Q_2
$P_{conduction}$		$R_{DSonQ1}.I_L^2.D$	$R_{DSonQ2}.I_L^2.(1-D)$
$P_{switching}$		$V_{in}.\left(Q_{GD}+\frac{Q_{GS}}{2}\right).f_s.\frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	**Recovery**	Not Applicable	$V_{in}.Q_{rrQ2}.f_s$
	Conduction	Not Applicable	$V_D.I_L.t_{deadtime}.f_s$
P_{gate}		$Q_{GQ1}.V_{GS}.f_s$	$Q_{GQ2}.V_{GS}.f_s$
P_{Co}		$\frac{C_{oQ1}.V_{in}^2.f_s}{2}$	$\frac{C_{oQ2}.V_{in}^2.f_s}{2}$

-D is the duty cycle.

-I_L is the average inductor current (the ripple is neglected).

-V_{in} is the input voltage.

-f_s is the switching frequency.

-R_{DSonQ1} and R_{DSonQ2} are respectively the on state resistance of Q_1 and Q_2.

-Q_{GSQ1} and Q_{GSQ2} are the gate to source charges of Q1 and Q_2, respectively.

- Q_{GDQ1} and Q_{GDQ2} are the gate to drain charges of Q_1 and Q_2, respectively.

-Q_{GQ1} and Q_{GQ2} are the total gate charges of Q_1 and Q_2, respectively.

-I_g is the gate current.

-Q_{rrQ2} is the reverse recovery charge of Q_2.

-$t_{deadtime}$ is the dead-time.

-V_D is the forward internal diode voltage drop during conduction.

-V_{GS} is the gate to source voltage applied to the MOSFET to turn it on.

-C_{oQ1} and C_{oQ2} are the output capacitances of Q_1 and Q_2, respectively.

Note: - The internal diode recovery loss is in fact dissipated through the switch Q_1.

- If a Schottky diode is used in parallel to Q_2 the recovery loss presented in the table should be replaced by $\frac{C_{Schottky}.V_{in}^2.f_s}{2}$, where $C_{schottky}$ is the diode's capacitance.

- For details regarding the Table 2.1 please refer to [50]-[51]

Finally, given the load presented by the CPU, MOSFETs with high current handling capability are needed for both positions. However, such MOSFETs are expensive. In addition, Q_{GS} and Q_{GD} become larger with the maximum drain current supported by the MOSFET. Hence, in the system design, instead of choosing a MOSFET able to handle the full load current (120 A), MOSFETs with a maximum drain current of 40 to 50 A are employed in today's VRM [52]. Indeed, if the load is correctly shared among the phases, each channel will carry a maximum current close to 30 A only. It is therefore all the more essential to ensure the correct current sharing in the multiphase converter in order to protect these MOSFETs.

In today's multiphase converter used to regulate the CPU voltage, the high side MOSFET has a drain source resistance close to 5 mΩ, and this resistance is around 2 mΩ for the low side switch [52]. Therefore, in this thesis, these values will be considered for the MOSFETs in the four phase converter.

2.1.2 Output capacitor selection

Output capacitance is another important factor to be considered, since it directly contributes to the fulfillment of steady state and transient requirements of the CPU. Currently, a very high output capacitance value is needed to contain the transient voltage fluctuations within the allowed limits. Such large valued capacitors are big in size, and their Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) are also substantial. These parasitic elements affect significantly the voltage transient during a step load [21], [53]. Therefore, to reduce their importance, several capacitors are placed in parallel [9]. The capacitors used are mainly of two kinds, viz., Aluminum Polymer and Multi-layer ceramic types.

The overall capacitor value is typically around 8 mF. Typically, the capacitor also has an Equivalent Series Resistance (ESR) of 0.15 mΩ and an Equivalent Series

Inductance (ESL) around 25 pH [9]. Since the ESL value is very small, only the ESR will be taken into consideration in the control design analysis.

2.1.3 Inductor selection

As mentioned in Section 1.2, the inductance used in each channel has been constantly decreased to meet the transient requirements of the CPU. In this thesis, methods to estimate the optimum inductance value that gives the best transient response with minimum steady state ripple will be presented for the three investigated control schemes. The inductance value will be determined later in this chapter.

Depending on the inductance value, a toroid shape inductor or a Surface Mount Device (SMD) power inductor are chosen in modern VRMs. Depending on the technology used, the inductor series resistance, R_3, varies typically between 0.3 mΩ and 2 mΩ [54]-[55]. In this thesis, a value of 0.8 mΩ has been assumed. Besides, in order to investigate the impact of only the inductance value on the dynamic performance of the converter, the resistance R_3 change when varying the inductance value will be ignored.

2.1.4 Switching frequency

The switching frequency f_s in the VRM has been constantly increased, in order to have a suitable control bandwidth to meet the CPU requirements, as well as to reduce the filter size. However, as shown in Table 2.1, the power loss also increases with f_s. Therefore, in today's multiphase converter, f_s is typically selected to be around 300 KHz [54], as a compromise between size, speed and efficiency.

2.1.5 Simulation parameters

In Table 2.2, the different characteristics of the multiphase converter considered in this thesis are summarized. As shown, the various known parasitic resistances have been considered and included. However, since the various leakage and parasitic inductances vary with the layout, they are not taken into account in this thesis. Also the switches are assumed to be ideal with a resistance in series. Finally, the CPU is modeled as an ideal variable current sink.

In this thesis, the various simulations are carried out using Matlab/Simulink software together with the Piece-wise Linear Electrical Circuit Simulation (PLECS) Simulink toolbox for electrical circuit simulations. Simulation details are provided in Appendix A.

TABLE 2. 2 FOUR PHASE CONVERTER CHARACTERISTICS USED IN THIS THESIS

Input voltage	V_{in}=12 V
Desired output voltage	V_{ref}=1.8 V
High side switch resistance	R_1=5 mΩ
Low side switch resistance	R_2=2 mΩ
Inductance series resistance	R_3=0.8 mΩ
Output capacitor and resistance	C=8 mF, ESR=0.15 mΩ
Switching frequency	f_s=300 KHz

2.2 Investigation of the power stage dynamics for step load changes with VMC

In this section, the multiphase converter controlled in a traditional VMC manner will be investigated under maximum step load condition. The implementation of the VMC scheme is first presented, and an equivalent simplified single phase converter is derived. Following this, a large signal model considering the various resistances of the converter is proposed and tested through simulations. Finally this model will be used to design the controller and to explain the concept of critical inductance. Simulation results will be provided to confirm the theoretical predictions.

2.2.1 VMC presentation and equivalent single phase converter

The overall Voltage Mode Control scheme implemented in an n-phase interleaved converter is presented in Fig. 2.1. In this figure, the various parasitic resistances have not been shown and the PWM blocks represent the pulse width modulation module [23].

In VMC, the control signal is derived directly from the output voltage error, via a voltage controller, and compared to the ramp signal in each PWM block to finally obtain the duty cycle in each channel. The ramp signals are equally phase-shifted, resulting in the gate signal provided to each upper MOSFET also being appropriately phase-shifted, as required in an interleaved converter. The control signal being the same for each PWM block, each channel will also exhibit similar gate signal, but phase-shifted correspondingly.

However, in this scheme, even though the output voltage is effectively controlled, the current sharing among the phases is not ensured. As will be seen later, this is the main drawback of the scheme.

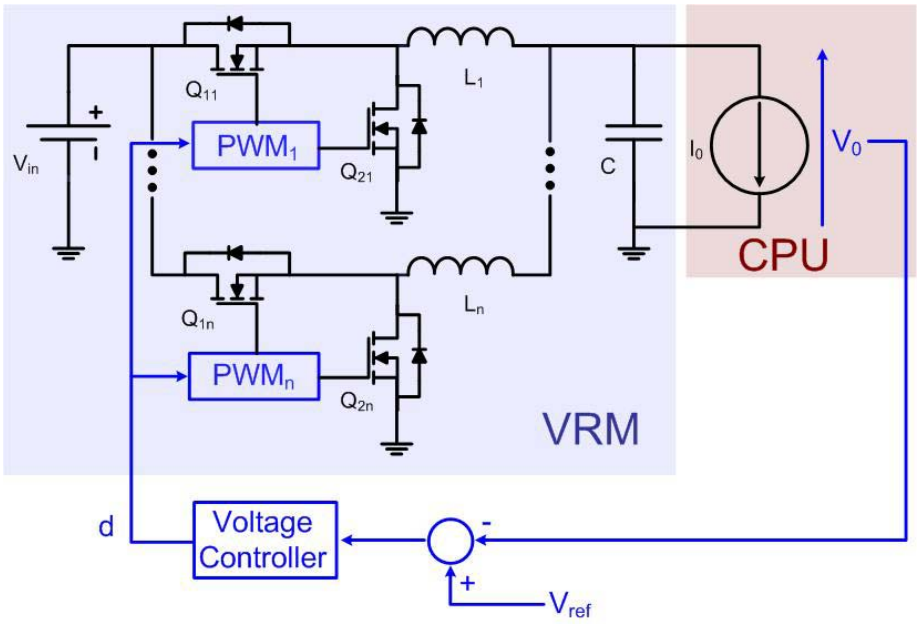

Fig. 2.1 Voltage Mode Control scheme in an n-phase buck converter

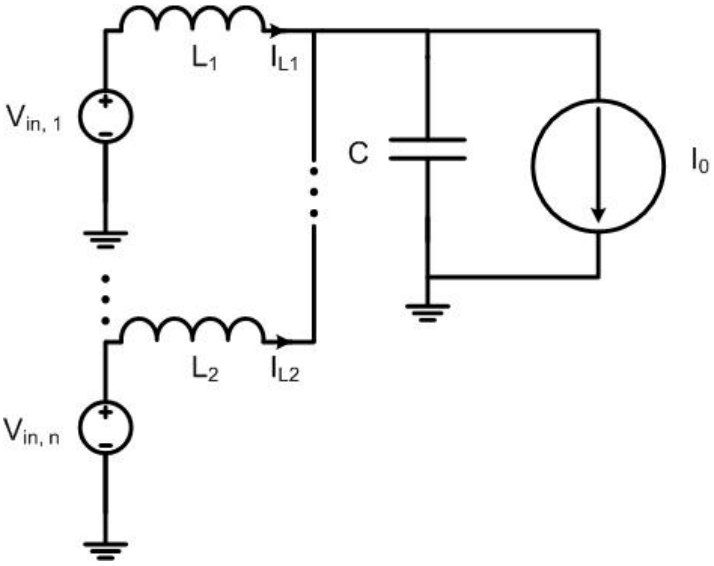

Fig. 2.2 Average circuit model of the n-channel interleaving buck converter

When analyzing the circuit, only the variation of the average voltages and currents are considered and investigated. This is a low frequency approximation, which is generally adopted in dealing with switch mode power converters [28]. In this case, the multiphase converter can be simplified into an equivalent single phase converter with corresponding equivalent parameters, as will be briefly explained in the following [56]-[57].

In an averaged model, the input voltage source together with the MOSFETs in one channel can be replaced by a controllable voltage source $V_{in,\mathrm{i}}$ (i=1...n), as shown in Fig. 2.2. This voltage source represents in fact the average potential across the synchronous MOSFET. Here, since the on-state resistances of the MOSFETs are considered, $V_{in,\mathrm{i}}$ value, not only depends on the duty cycle D, but also on the average current flowing in that particular channel, i. However, assuming a correct current sharing, and also since in a VMC scheme all the channels operate with the same duty cycle, all the $V_{in,\mathrm{i}}$ sources shown in Fig. 2.2 are of the same value. As a result, the inductors are in a parallel configuration, and can be replaced by an equivalent inductor. Consequently, the voltage sources are also in parallel and can be replaced by an equivalent voltage source.

Thus, by re-replacing the resulting voltage source by the original input voltage source V_{in} followed by switches, the average model of the interleaving buck can be simplified to an equivalent single buck converter [34], [46]. In this simplified topology, the input voltage source, the output capacitor and the load remain the same. However, the resistances of the switches and the values of the inductance are divided by the number of phases. The inductor current in the simplified circuit represents the total inductor current of the multiphase converter. Therefore, the switching frequency

in the equivalent circuit, f_{seq}, is equal to the original switching frequency f_s in the multiphase converter multiplied by the number of phases.

In the following, such an equivalent circuit for the four phase converter introduced in Section 2.1.5, is analyzed to derive a large signal model, which can then be used for the control design.

2.2.2 Proposed averaged linear large signal model

The equivalent circuit of the four phase converter presented in Section 2.1.5, is shown in Fig. 2.3. In this figure, R_{1eq} and R_{2eq} are the equivalent drain source resistance of the upper and lower MOSFET. From Table 2.2 they are, respectively, 1.25 mΩ and 0.5 mΩ. The equivalent parasitic resistance of the inductor R_{3eq} is also estimated to be 0.2 mΩ.

The switching converter is inherently non-linear. However, a linear model is many times desirable in order to design the controller using classical linear system techniques or to predict the variation of circuit variables, such as inductor current or output voltage. To obtain such a linear model, the converter is usually linearized around one DC operating point using state space averaging techniques [23], [28], [58]. In the synchronous buck converter, should we neglect the difference between the two on-state resistances of the MOSFETs (Q_1 & Q_2), the resulting linear averaged model from state space averaging is valid for large signals also, as shown in [46]. However, if this difference is taken into account, the model validity is restricted to small signals only, as will be shown in the following. In the following, an approximate large signal model will be proposed and its validity verified using simulations. This model will be useful in investigating the converter dynamics under large load disturbances.

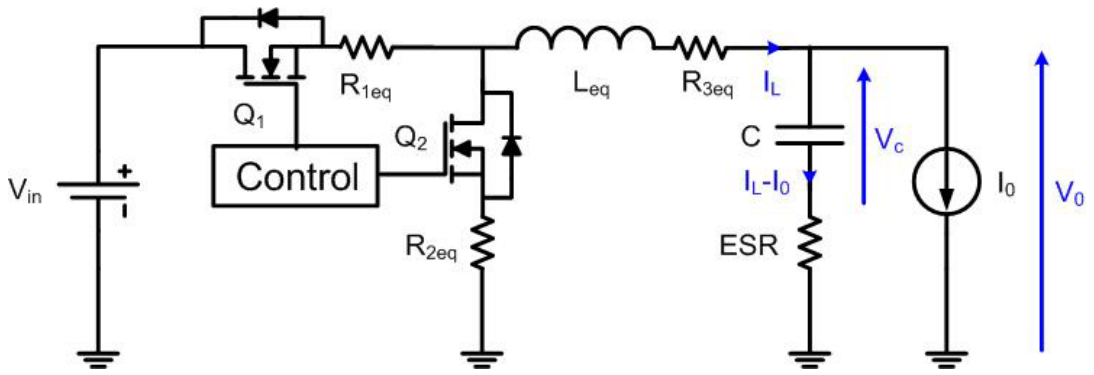

Fig. 2.3 Single phase equivalent model

In the converter presented in Fig. 2.3, the inductor current I_L and the output capacitor voltage V_C are chosen to be the state variables, whereas the duty cycle D, and the load current I_0 are the inputs, and the output voltage V_0 is the output.

During on-state (Q_1 on and Q_2 off), the following state-space equations can be written:

$$\begin{cases} L_{eq}\dfrac{dI_L}{dt} + R_{3eq}.I_L = V_{in} - R_{1eq}.I_L - V_C - ESR.\left(I_L - I_0\right) \\ C\dfrac{dV_C}{dt} = I_L - I_0 \\ V_0 = V_C + ESR.\left(I_L - I_0\right) \end{cases} \tag{2.1}$$

During off-state (Q_1 off and Q_2 on), the state-space equations become

$$\begin{cases} L_{eq}\dfrac{dI_L}{dt} + R_{3eq}.I_L = -R_{2eq}.I_L - V_C - ESR.\left(I_L - I_0\right) \\ C\dfrac{dV_C}{dt} = I_L - I_0 \\ V_0 = V_C + ESR\left(I_L - I_0\right) \end{cases} \tag{2.2}$$

Thus, by averaging the currents and voltages over one time period, we obtain

$$\begin{cases} L_{eq}\dfrac{d\langle I_L\rangle}{dt} + R_{3eq}\langle I_L\rangle = \langle D\rangle.V_{in} - R_{1eq}\langle D\rangle\langle I_L\rangle - R_{2eq}.\left(1-\langle D\rangle\right)\langle I_L\rangle - ESR\left(\langle I_L\rangle - \langle I_0\rangle\right) - \langle V_C\rangle \\ C\dfrac{d\langle V_C\rangle}{dt} = \langle I_L\rangle - \langle I_0\rangle \\ \langle V_0\rangle = \langle V_C\rangle + ESR.\left(\langle I_L\rangle - \langle I_0\rangle\right) \end{cases} \tag{2.3}$$

where the terms within brackets represent the variable averaged over a cycle.

If R_{1eq} and R_{2eq} are of different values, equation (2.3) is non-linear due to the presence of the non-linear terms involving $<D>.<I_L>$. Therefore, in order to obtain a linear model, a first order approximation is performed using small perturbations around the steady state values. In the following, the capital letter will symbolize the steady state value, and the small letter, the small perturbation around it.

Hence by perturbing the duty cycle and the load current by d and i_0, respectively, the state variables and the output voltage are also perturbed from their steady-state values. Thus,

$$\begin{cases} \langle D \rangle = D + d \\ \langle I_0 \rangle = I_0 + i_0 \\ \langle I_L \rangle = I_L + i_L \\ \langle V_C \rangle = V_C + v_C \\ \langle V_0 \rangle = V_0 + v_0 \end{cases} \tag{2.4}$$

Hence, by injecting (2.4) into (2.3), the equation (2.3) can be rearranged after simplification as

$$\begin{cases} L_{eq}\dfrac{di_L}{dt} = (V_{in} - R_{1eq}I_L + R_{2eq}I_L)d - (DR_{1eq} + (1-D)R_{2eq} + R_{3eq} + ESR)i_L + (R_{2eq} - R_{1eq})di_L + ESRi_0 - v_c \\ C\dfrac{dv_C}{dt} = i_L - i_0 \\ v_0 = v_c + ESR(i_L - i_0) \end{cases} \tag{2.5}$$

$$\text{since} \begin{cases} DV_{in} - R_{1eq}DI_L - R_{2eq}(1-D)I_L - R_{3eq}I_L - ESR(I_L - I_0) - V_C = L_{eq}\dfrac{dI_L}{dt} = 0 \\ I_L - I_0 = C\dfrac{dV_C}{dt} = 0 \\ V_0 = V_C + ESR.(I_L - I_0) \end{cases} \tag{2.6}$$

Equation (2.6) is based on the assumption that under steady state, the following is valid: $\dfrac{dD}{dt} = \dfrac{dI_0}{dt} = \dfrac{dI_L}{dt} = \dfrac{dV_C}{dt} = \dfrac{dV_0}{dt} = 0$

In a first order approximation, the terms in $d.i_L$ can be neglected. Hence, the following linear equation can be obtained for small perturbations around the DC operating point:

$$\begin{cases} L_{eq}\dfrac{di_L}{dt} = \left(V_{in} - \left(R_{1eq} - R_{2eq}\right)I_L\right)d - \left(R_{eq} + ESR\right)i_L + ESRi_0 - v_c \\ C\dfrac{dv_C}{dt} = i_L - i_0 \\ v_0 = v_c + ESR\left(i_L - i_0\right) \end{cases} \tag{2.7}$$

where, $R_{eq} = D.R_{1eq} + \left(1-D\right)R_{2eq} + R_{3eq}$ (2.8)

Therefore, by combining the preceding set of equations, and transforming into the Laplace domain, we get:

$$v_0 = \frac{\left(1+ESR.Cs\right)\left(V_{in} - \left(R_{1eq} - R_{2eq}\right)I_L\right)}{L_{eq}Cs^2 + \left(R_{eq} + ESR\right)Cs + 1}d - \frac{\left(1+ESR.Cs\right)\left(L_{eq}s + R_{eq}\right)}{L_{eq}Cs^2 + \left(R_{eq} + ESR\right)Cs + 1}i_0 \tag{2.9}$$

It is important to note that this Laplace domain equation is only valid as a small signal approximation. However, as mentioned earlier, if the difference between the two switch resistances, R_{1eq} and R_{2eq} is not taken into account, its validity is extended over a large range of duty ratio and load variation. Hence, generally, the switch resistances are simply neglected in the circuit analysis, though the inductor and capacitor series resistances are considered [21], [45]-[48]. In the following, in order to investigate the importance of the MOSFET drain-source resistances in the circuit analysis, a comparison between three different situations is performed:

Case 1: none of the parasitic resistances are taken into account

Case 2: only the *ESR* and R_{3eq} are considered

Case 3: all the resistances are taken into account.

The output voltage to duty cycle transfer function for all the three cases are first compared in Fig. 2.4, for an equivalent inductance of 300 nH, and an average output

current of 100 A. For such a load, the steady state duty cycle D is found to be 0.157 and the average inductor current equals 100 A. These values are used to estimate the transfer function in case 3. It may be noted that the Bode diagrams in Figs. 2.4 and 2.5 for the first two cases represent both the small signal and large signal responses.

The bode diagrams presented in Fig. 2.4 show that the approximations made in the first two cases, fail to follow closely the exact system curves presented in case 3, especially around the resonant frequency. An investigation of the Bode plots of the output voltage to load current transfer function for the same three situations (see Fig. 2.5) leads to the same conclusion. Since the models derived from the first two situations fail to track precisely the more precise small signal model of case 3, where none of the resistances have been neglected, case 1 and case 2 models can only be considered as very approximate models, in general. Hence, they are not suitable for use as large signal models for accurate circuit analysis.

Therefore, in the following, instead of neglecting the MOSFET drain-source resistances to derive a large signal model, the validity of the accurate small signal transfer functions found in (2.9) for large signal perturbations is considered. But, in this case, the resulting transfer functions depend on the steady state duty cycle D and inductor current I_L, which both vary with the load. This may complicate the circuit analysis.

However, D does not vary much with the load. In the simulations using the set of equations (2.6), it is estimated to be 0.151 for a minimum output current of 0.5 A, and it increases to only 0.159 for a maximum load of 120 A. Hence, an average duty cycle of 0.155 may be employed in (2.9) independently of the load current. As for the dependency of the transfer function on the inductor current, it is investigated in the following.

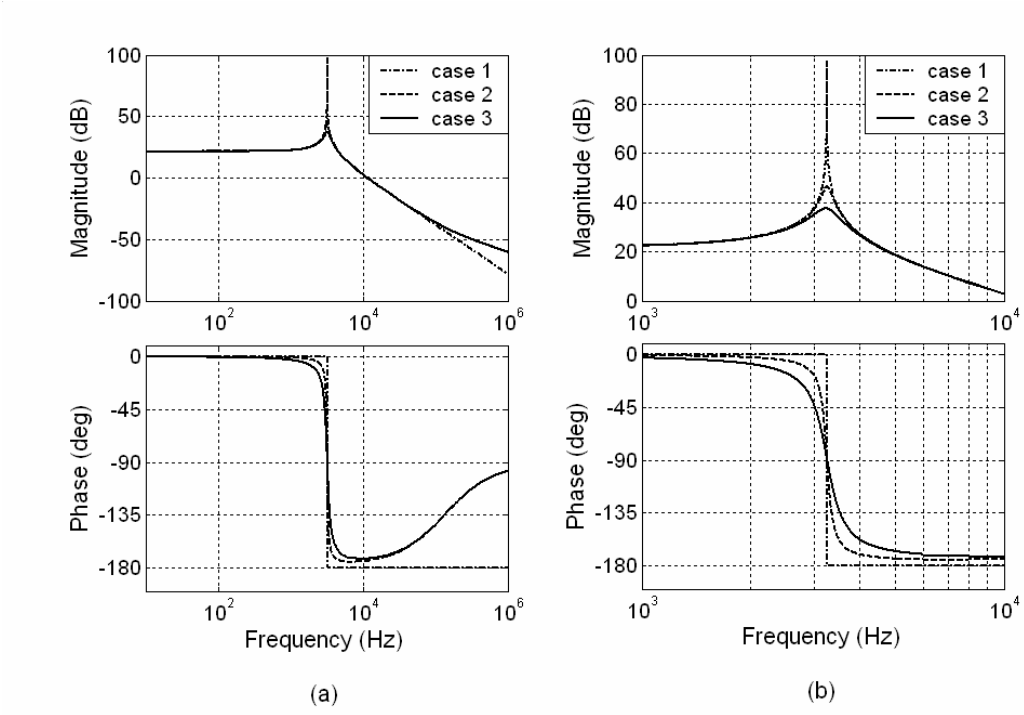

Fig. 2.4 Output voltage to duty cycle transfer function for the three cases
(a) overall
(b) around the resonant frequency

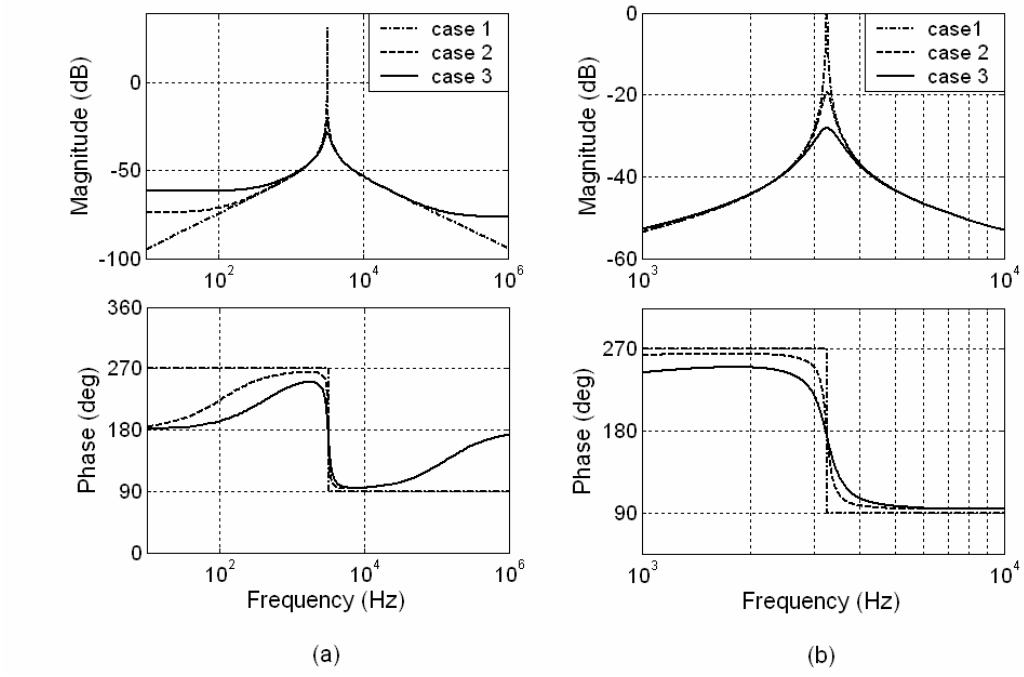

Fig. 2.5 Output voltage to load transfer function for the three cases
(a) overall
(b) around the resonant frequency

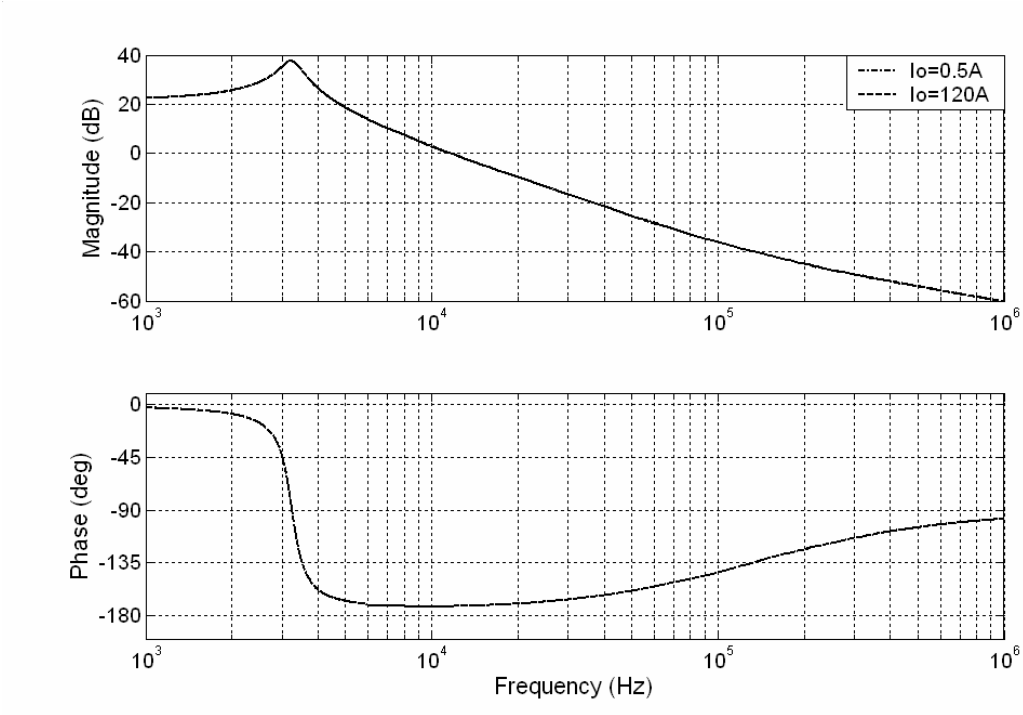

Fig. 2.6 Small signal output voltage to duty cycle transfer function for different average inductor current

The inductor current I_L affects only the output voltage to duty cycle transfer function. Fig. 2.6 shows the corresponding Bode diagrams in case of the two extreme average inductor currents usually occurring in VRMs (0.5 A and 120 A). It is shown in this figure, that the differences between the two Bode plots are insignificant.

This can be simply explained by the fact that, in the v_0/d transfer function shown in (2.6), $(R_{1eq}\text{-}R_{2eq}).I_L$ is negligible compared to V_{in} for the range of inductor currents usually carried by the VRM. Consequently, this term can reasonably be ignored in order to obtain a linear model independent of the load.

Hence, the large signal output voltage to duty cycle transfer function v_0/d and output voltage to load current transfer function v_0/i_0 can be fairly approximated by:

$$\frac{v_0}{d} = G_{vd} = K_{vd} \frac{1+\dfrac{s}{\omega_{ESR}}}{\dfrac{s^2}{\omega_0^2}+\dfrac{s}{Q.\omega_0}+1}, \text{ and} \tag{2.10}$$

$$\frac{v_0}{i_0} = G_{vi} = -K_{vi} \frac{\left(1+\frac{s}{\omega_{ESR}}\right)\left(1+\frac{s}{\omega_{Req}}\right)}{\frac{s^2}{\omega_0^2}+\frac{s}{Q.\omega_0}+1}, \tag{2.11}$$

where $\omega_0 = \frac{1}{\sqrt{L_{eq}.C}}$, $Q = \frac{1}{R_{eq}+ESR}\sqrt{\frac{C}{L_{eq}}}$, $\omega_{ESR} = \frac{1}{ESR.C}$, $\omega_{Req} = \frac{R_{eq}}{L_{eq}}$, $K_{vd} = V_{in}$, $K_{vi} = R_{eq}$

To verify the validity of these transfer functions for inputs of large magnitude, a large step response is simulated using Matlab and PLECS softwares. Here, the load is varied in a step manner in both ways with a large magnitude of 90A, and the resulting output voltage fluctuation in the single phase equivalent buck converter for a constant duty cycle of 0.155 as well as the output variation obtained from the linear model proposed in (2.11) are plotted in Fig. 2.7. In the same manner, the output voltage responses for a duty cycle variation of 0.9 are shown in Fig. 2.8. Also in both cases, for comparison purposes, the predicted output voltage waveforms in case none of the switch resistances are considered, are also presented in Fig. 2.7 and Fig. 2.8.

Here, the proposed model is shown to follow accurately the actual output voltage waveform sensed from a simulated buck converter, under heavy load and duty cycle disturbance. However, the model differs slightly from the actual case when increasing the duty cycle from a very low value to a very high value (0.155 to 0.955). This is due to the approximation with regard to the duty cycle made in (2.7). Indeed, the non-linear parts that have been neglected were in terms of variation in duty cycle d and in average inductor current i_L. When increasing d in the buck converter, i_L is also increased, causing the non-linear terms to become less negligible. This explains the small deviation of the proposed model for large duty ratios. Nevertheless, overall, (2.10) and (2.11) are reasonably accurate over a large range of d and i_0 values.

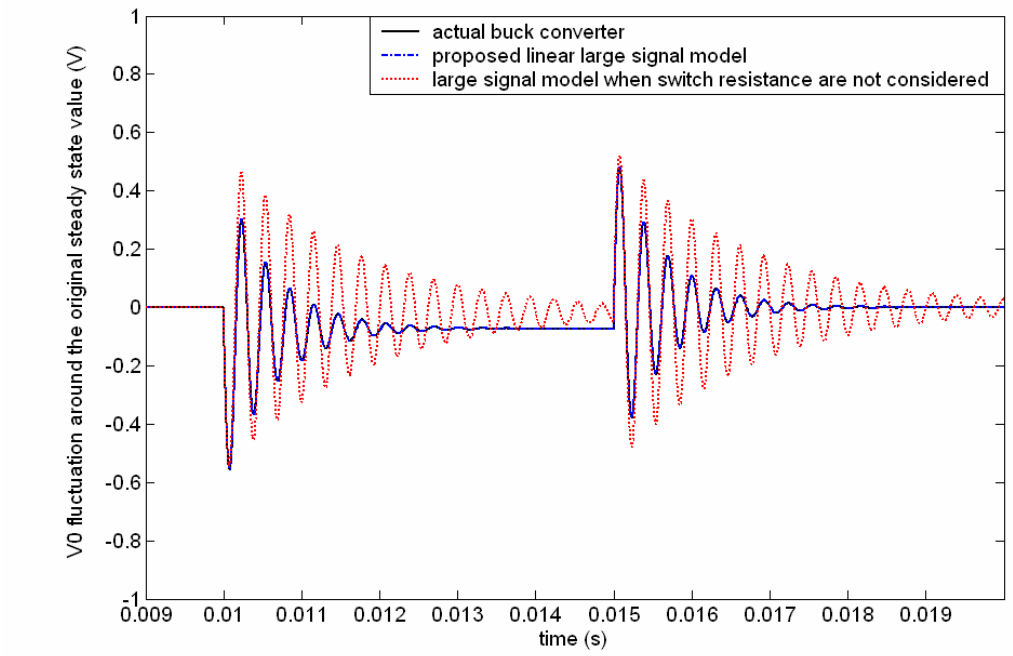

Fig. 2.7 Output voltage fluctuation due to a step load from 10A to 100A in the normal buck converter for different large signal models

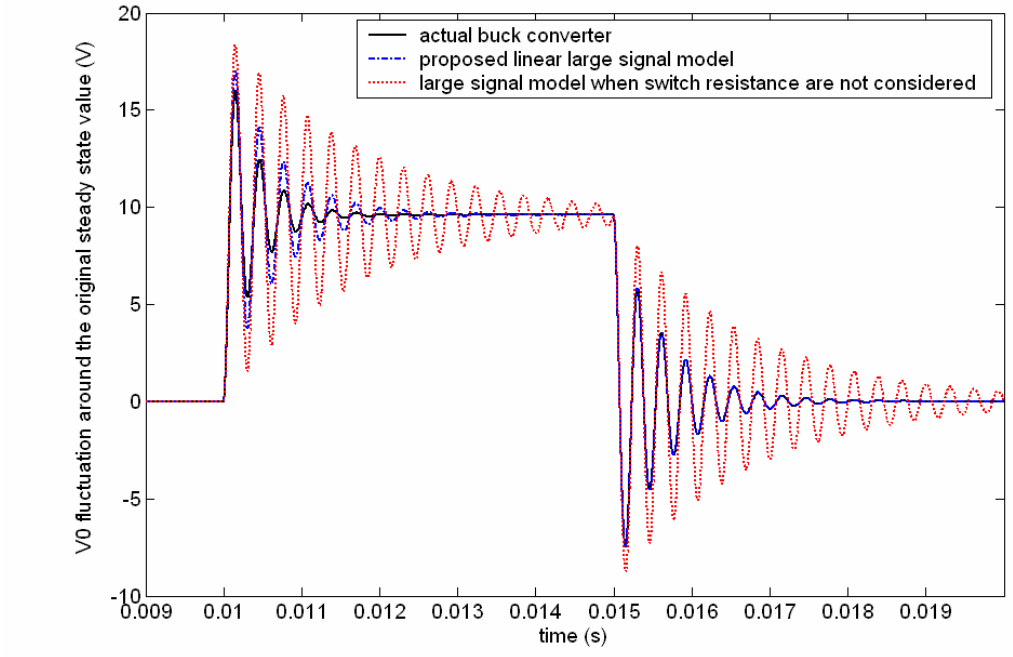

Fig. 2.8 Output voltage fluctuation due to a step variation in the duty cycle from 0.16 to 0.96 in the normal buck converter for different large signal models

On the contrary, the classical large signal model, where the switch resistances are ignored, is shown to be very approximate. The modeled system is indeed very less damped than the actual converter, causing large output oscillations, which do not occur in the real system. Furthermore, by neglecting the switch resistances, the steady state output voltage deviation due to different loads is wrongly predicted as shown in Fig. 2.7.

Based on the above, the transfer functions proposed and obtained in (2.10) and (2.11) are considered valid for signals of large magnitude, provided no duty cycle saturation occurs. Following this, these transfer functions can be used to design the voltage controller, and to predict accurately the output voltage waveform, for a given large load disturbance.

2.2.3 Voltage controller design

In this section, the voltage controller C_v is designed based on the G_{vd} transfer function presented in (2.10). The Bode diagram of G_{vd} is shown in Fig. 2.9 for an equivalent inductance of 300 nH.

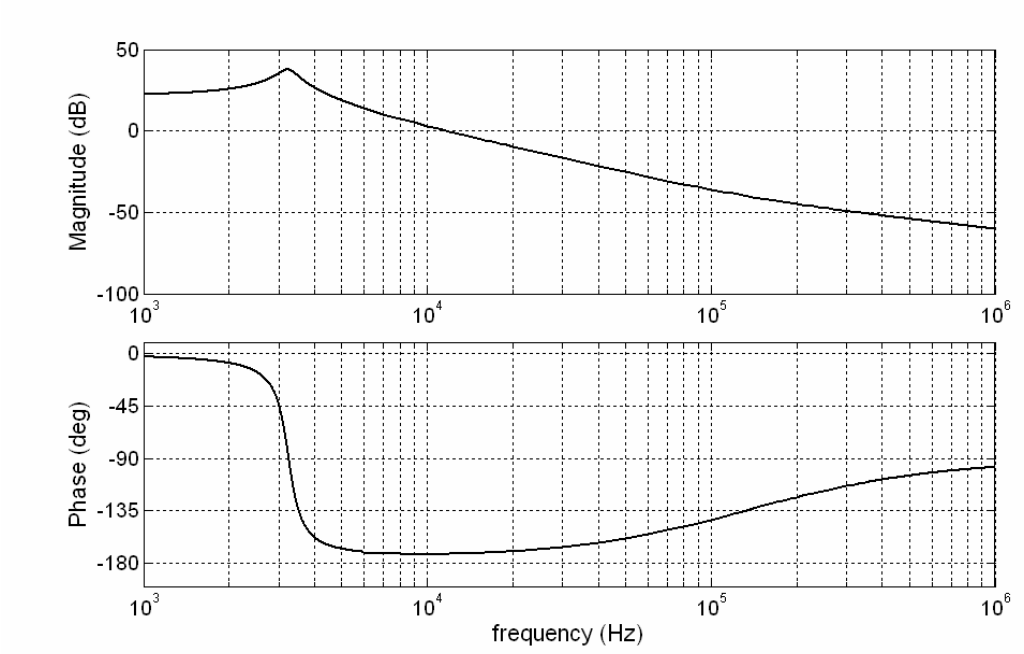

Fig. 2.9 Output voltage to duty cycle transfer function G_{vd} for an equivalent inductance value of 300 nH.

It has been noticed that for the range of inductances studied in this thesis, the frequency responses of G_{vd} have a similar waveform. Hence, though the following design methodology is based for an equivalent inductance of 300 nH, the same design procedure has been applied for the other inductor values also.

From Fig. 2.9, an integrator is first added in the controller to avoid any steady state error. Besides, as a compromise between the controller's sensitivity to the inherent output voltage ripple and the speed of the controller, a bandwidth of one tenth of the voltage ripple frequency is chosen. Since in the equivalent circuit the output voltage has a ripple at 1.2 MHz, the overall bandwidth is thus selected close to 120 KHz. For stability purposes, the open loop transfer function must cross the 0 dB line with a slope of -20 dB/decade. Hence, given the selected bandwidth frequency, a double zero ω_z is added in the controller close to the resonant frequency ω_0 of G_{vd}. Subsequently, an additional pole ω_h is also included in the controller around ω_{ESR}, to compensate the controller's double zero, and at the same time decrease the high frequency open loop gain. Finally, the DC gain of the controller K_{Cv} is adjusted to have the desired bandwidth.

Thus, overall, the controller has the following form:

$$C_v = K_{Cv} \frac{\left(1+\frac{s}{\omega_z}\right)^2}{s\left(1+\frac{s}{\omega_h}\right)} \tag{2.12}$$

Given the design methodology, the open loop transfer function may be approximated to ω_b/s (ω_b is the selected bandwidth in *rad/s*), as shown in Fig. 2.10, where both the frequency response of the resulting open loop transfer function T_v, and its approximation as ω_b/s are presented.

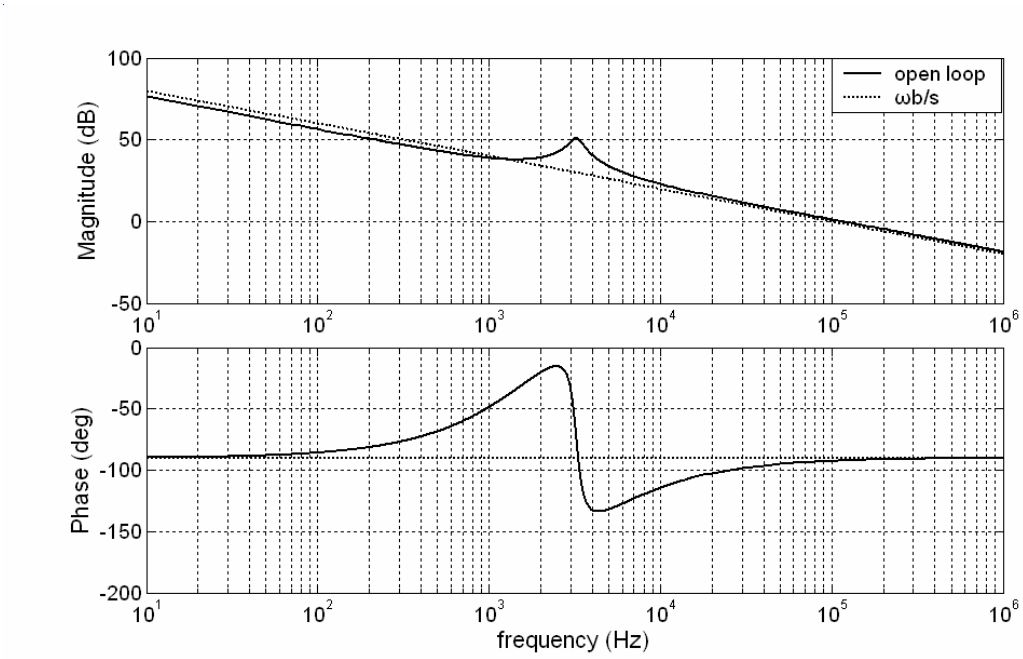

Fig. 2.10 Open loop corrected system and its approximation

In the following, the dynamic performance of the converter is investigated for different values of inductances. For a fair comparison, the controller's DC gain K_{cv} and zero ω_z are adjusted each time so as to keep the same open loop characteristics (e.g. bandwidth and phase margin). However, the positions of the poles remain unchanged (one integrator and one high frequency pole at 8.33×10^5 rad/s). Table 2.3 lists the selected K_{cv} and ω_z in the simulation according to the inductor value.

TABLE 2.3 CONTROLLER GAIN AND ZERO SELECTION FOR DIFFERENT INDUCTANCES

L_{eq}(nH)	300	250	200	150	100	50	40	30	20	10
K_{cv} ($\times10^4$)	6.05	6.05	5.80	5.50	5.15	4.00	3.86	3.57	3.45	2.83
ω_z(rad/s) ($\times10^4$)	2.00	2.22	2.38	2.70	3.23	4.00	4.35	5.00	5.88	7.69

2.2.4 Simulation results according to the equivalence inductance value

As mentioned in Chapter 1, from one generation of microprocessor to the next, the magnitude of variation in the drawn current has increased greatly while the core voltage requirements have become more stringent. As a result, to improve the dynamic response of the converter in regulating the output power, a lower inductance and a larger output capacitance values are being used in VRMs, thus, sacrificing the efficiency for the benefit of dynamic performance. However, in the literature, it has been shown for the voltage mode control that there exists a limit below which decreasing the inductance does not shorten any more the transient time for a given control bandwidth [45]-[48]. In the following, such a limit, called the critical inductance, is presented through simulation results for the four phase converter.

The equivalent circuit of the four phase converter has been simulated for the various inductance values presented in Table 2.3. The load was varied in a step manner from 10 A to 100 A and vice versa. The transient time is defined as the time taken by the system to recover fully the output voltage to the desired value within a particular voltage tolerance band. For each inductance value and for both load increase and load decrease, the transient time is measured, as shown in Fig. 2.11 for two different inductances. For this purpose, a 20 mV band is chosen to measure the transient time. These transient times, indicated as $\Delta t_{20mV\uparrow}$ and $\Delta t_{20mV\downarrow}$ for load step up and step down respectively, are listed in Table 2.4. The minimum and maximum output voltage, V_{min} and V_{max}, reached respectively during load step up and load step down are also indicated.

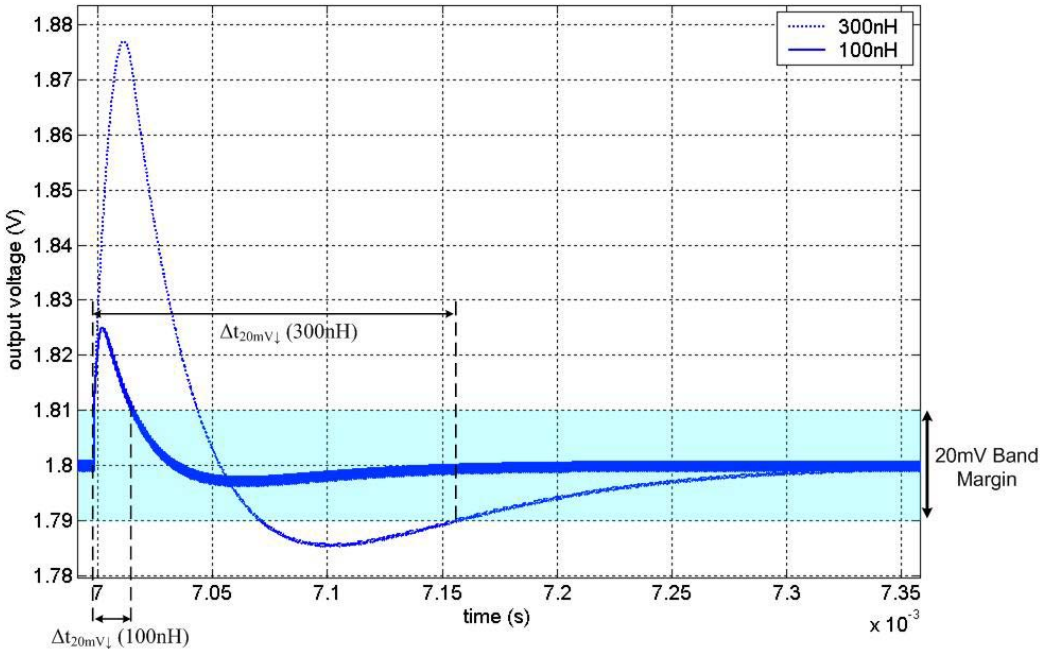

Fig. 2.11 Output voltage waveforms during a load step down for two different inductor values

TABLE 2.4 SIMULATION RESULTS FOR A 90A STEP UP AND STEP DOWN IN LOAD

L (nH)	$\Delta t_{20mV\uparrow}$ (µs)	V_{min} (V)	$\Delta t_{20mV\downarrow}$ (µs)	V_{max} (V)
300	18	1.78	161	1.88
250	16	1.78	123	1.86
200	13	1.78	32	1.85
150	11	1.78	25	1.84
100	11	1.78	18	1.82
50	11	1.78	12	1.81
40	11	1.78	11	1.81
30	13	1.78	10	1.82
20	15	1.78	13	1.82
10	∞	1.78	∞	1.82

For an inductance value of 10 nH and less, the output voltage ripple exceeds 20 mV. Therefore, the 20 mV-transient time does not exist, and the symbol ∞ is indicated in Table 2.4 next to such an inductor value. It is also shown from Table 2.4, that for a same inductor value, the transient time and voltage fluctuation are more important when the load varies suddenly from a high to a low value, than in the reverse direction. This is, in fact, due to the very low steady state duty cycle value, which limits the range of variation of the duty ratio over one cycle under a step down load transient since the duty cycle value cannot go below zero.

The transient time is plotted in Fig. 2.12 against the inductance value, for load step up and load step down separately. From this figure, we note that at first, the transient time decreases almost linearly as the inductance is reduced. But, as shown in Fig. 2.12 for the load step down case, as the inductance is reduced the transient time jumps discontinuously to a lower value at around an inductance value of 200 nH, and then keeps decreasing again in a linear manner. This is simply due to the fact that, as presented in Fig. 2.11, the output voltage waveform may enter directly the narrow voltage band and remain inside, or after one or several oscillations. Hence, in the load step down case, for an inductance of 200 nH and less, the transient time is reached without any oscillation, whereas, for 250 nH and more there is at least one cycle of oscillation before the output voltage waveform is contained within the 20 mV band. This explains the discontinuity in the transient time graph in Fig. 2.14.

However, overall, except for this discontinuity, the transient time decreases linearly with the inductance until a certain point. Then, it remains fairly constant with decreasing inductance. The voltage overshoot or undershoot magnitude is also minimized around the same point. The transient time increases once again at very low inductances due to the increased voltage ripple.

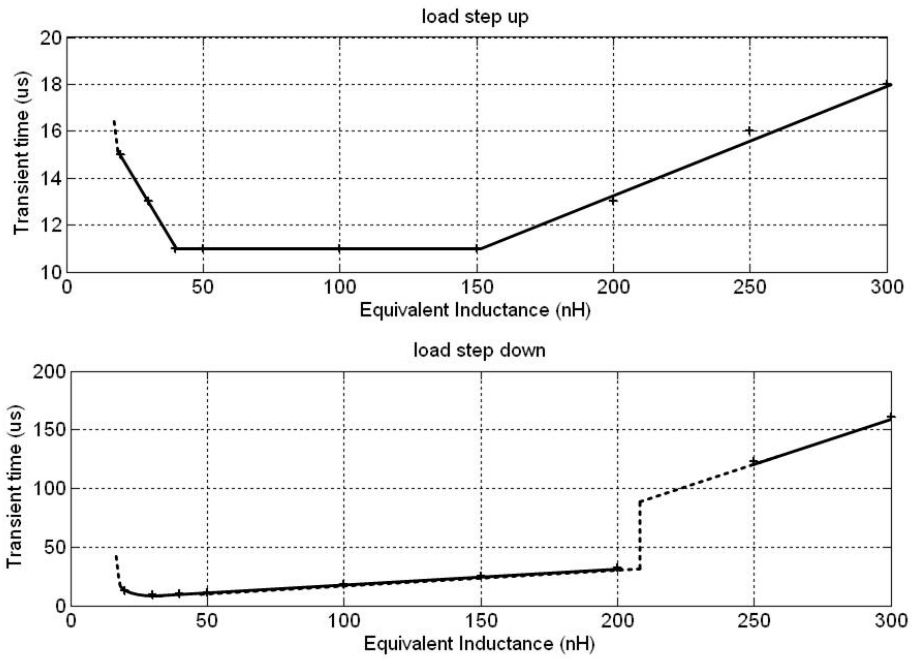

Fig. 2.12 20 mV-band transient time vs inductance for load step-up and step down

The inductance below which the transient time does not decrease further is called the critical inductance, and is estimated from Fig. 2.12 to be around 150 nH for a load step up of 90 A, and close to 30 nH for a load step down of same magnitude. The critical inductance concept is analytically investigated in the following section using the large signal transfer functions derived in Section 2.2.2.

2.2.5 Critical inductance analysis

Through the preceding simulations, it has been shown that, though having almost the same open loop characteristics, the systems with different inductance values do not exhibit the same transient waveforms. However, when the inductance is reduced below a certain level called the critical inductance, it has been noticed that the fluctuation of the average output voltage does not change, as shown in Fig. 2.13 for three different inductances for the load step down. As presented in Fig. 2.14, the same fact is observed for the inductor current. These simulation results can be explained through the duty cycle saturation phenomenon.

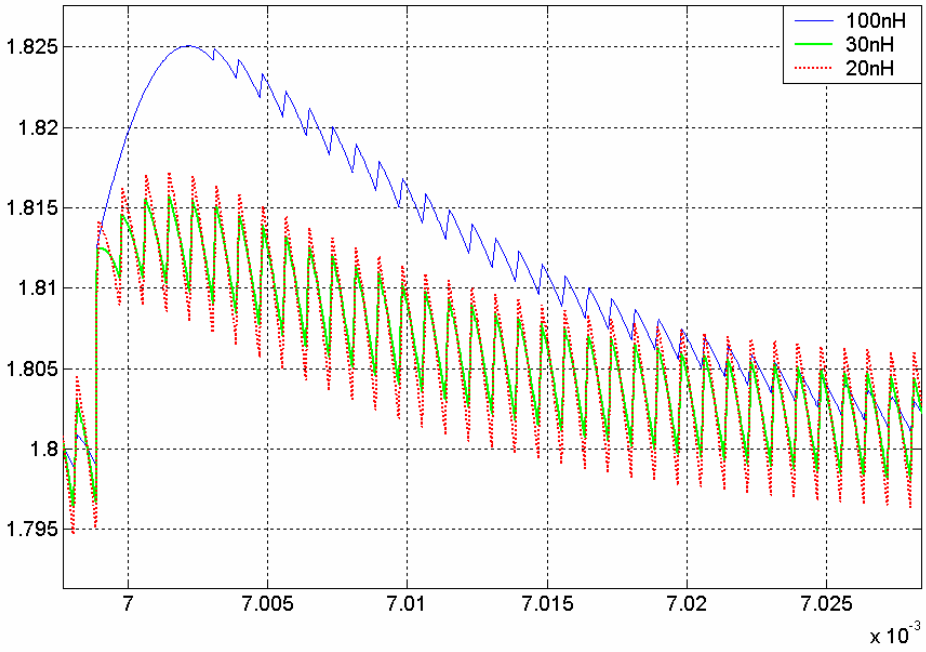

Fig. 2.13 Output voltage fluctuation for three different inductances for a load step up of 90 A.

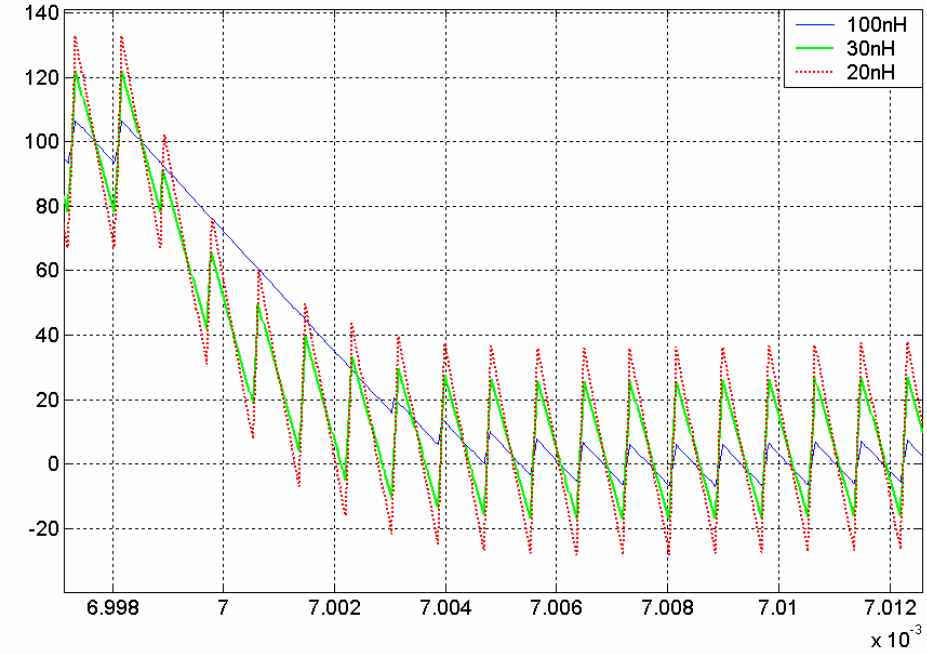

Fig. 2. 14 Inductor current variation during load step down of 90 A for three different inductances

For a given control bandwidth, with a large inductance, the DC gain K_{cv} of the controller has to be increased and its zero frequency ω_z decreased, as shown in Table 2.3. Therefore, the controller needs greater high frequency gain in order to achieve the same open loop bandwidth. As a result, when a sudden load change occurs, the controller provides duty cycle values below zero or beyond one, which are interpreted by the system through the PWM block as a duty cycle value of either zero or unity. This phenomenon is called duty cycle saturation. Hence, during transient, the system is not fully controlled, and the inductor current variation depends on the selected inductor value. Thus, the transient time increases with the inductance.

However, when the inductance is lower than the critical inductance value, the duty cycle saturation no longer occurs; thus, the converter is all the time controlled, and the rising or falling time of the inductor current is fixed by the controller. Hence, since all of the systems are designed to have the same bandwidth, the transient performances do not vary when decreasing the inductor value further.

Various methods to estimate analytically the critical inductance in the case of the VMC have been suggested [45]-[48]. In [46]-[48], the method is primarily based on the average inductor current waveform. Here, the inductor current variation for a given load disturbance is first predicted using an assumed large signal model. The large signal model is based on neglecting the switch resistances and is identical to case 2 studied in Section 2.2.2. As has already been shown in that section, this large signal model is not accurate for our purpose. Following the development of the large signal model in [46], the inductor current rise time and fall time are determined for a given load disturbance. The inductance is then chosen in such a way that it allows the predicted current variation in the measured time. This method is however been proven to be approximate [45].

A more precise methodology based on the duty cycle to load current transfer function is presented in [45]. In the following, a method is provided for determining the critical inductance for the VMC case, which is largely based on [45]. In [45], the loop transfer function is designed to be a second order function, whereas in the present work, it has been designed to be a first order function, which results in convenient closed form expressions (unlike in [45]) for the critical inductance. The duty cycle variation to load change transfer function d/i_0, is first estimated, in order to predict the duty cycle variation during a sudden load step. The inductance is then selected so to avoid duty cycle saturation.

Given the large signal model derived in section 2.2.2, the VMC block diagram is shown in Fig. 2.15. From this figure, for a constant reference voltage, the duty cycle variation d to load current variation i_0 transfer function can be directly obtained:

$$\frac{d}{i_0} = -\frac{C_v.G_{vi}}{1+C_v.G_{vd}} \tag{2.13}$$

By noting $G_n = \dfrac{1}{L_{eq}Cs^2 + \left(R_{eq} + ESR\right)Cs + 1}$ (2.14),

we obtain from (2.10) and (2.11):

$$\frac{d}{i_0} = \frac{\left(Ls + R_{eq}\right)C_v.G_n}{1+V_{in}.C_v.G_n} \tag{2.15}$$

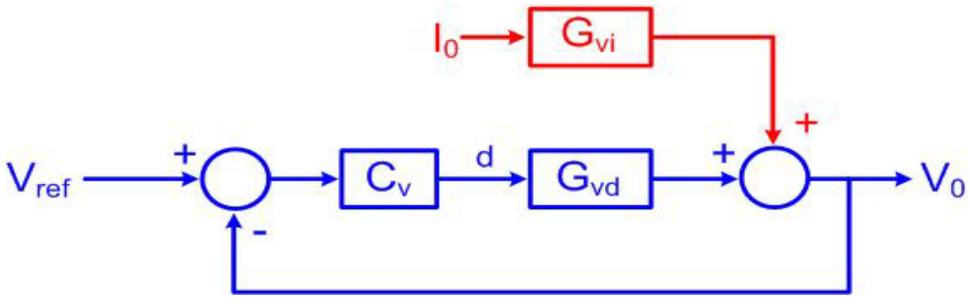

Fig. 2.15 VMC block diagram

Since the open loop transfer function T_v is given by:

$$T_v = C_v.G_{vd} = C_v.V_{in}.G_n, \tag{2.16}$$

(2.15) can be simplified into:

$$\frac{d}{i_0} = \frac{\left(Ls + R_{eq}\right)}{1 + T_v} . \frac{T_v}{V_{in}} \tag{2.17}$$

For a given open loop transfer function, (2.17) can readily be used to estimate the duty cycle to load current transfer function. In Section 2.4, the controller has been designed in such a way, that T_v can be approximated by ω_b/s. As a result, d/i_0 is close to:

$$\frac{d}{i_0} \approx \frac{\left(L_{eq}s + R_{eq}\right)\omega_b}{V_{in}\left(s + \omega_b\right)} \tag{2.18}$$

For comparison, in Fig. 2.16, both the exact transfer function and the approximation in (2.18) are presented for an equivalent inductance of 300 nH. The close similarity between the two bode diagrams justify the approximation once again, and in the following the d/i_0 transfer function will be assumed as given in (2.18).

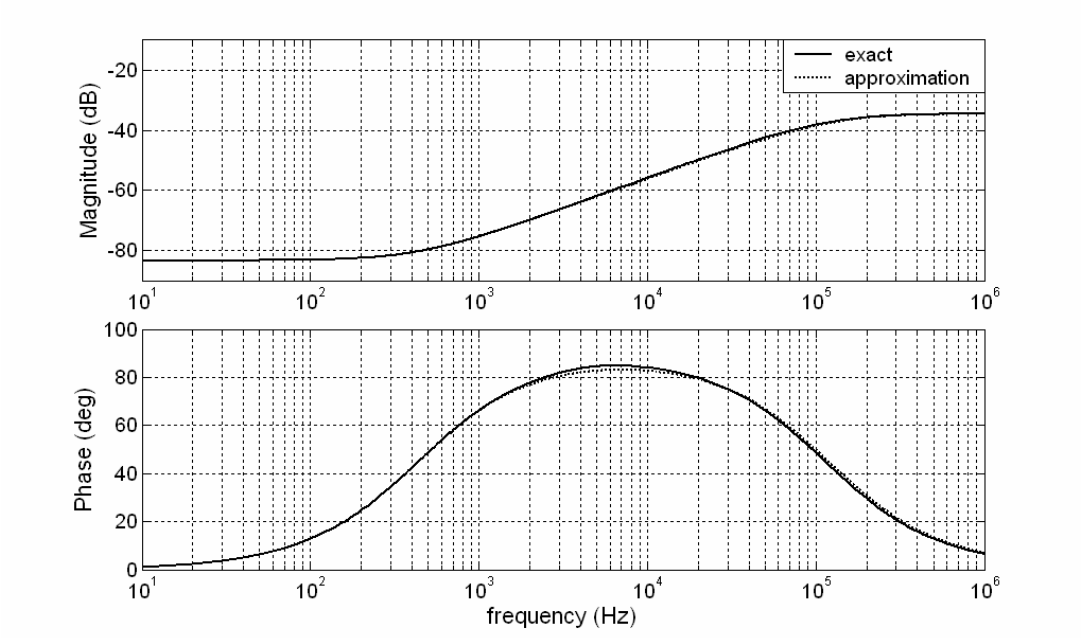

Fig. 2.16 Bode plot comparison between d/i0and its approximation for an equivalent inductor of 300nH

Consequently, the Laplace transform of the controller's output variation, due to the load step change of magnitude i_0, can be approximated to:

$$d(s) = \frac{\omega_b L_{eq} i_0}{V_{in}} \frac{1}{s+\omega_b} + \frac{\omega_b R_{eq} i_0}{V_{in}} \frac{1}{s(s+\omega_b)} \tag{2.19}$$

Hence, provided there is no duty cycle saturation, if the load changes by i_0 in a step manner at time t=0, the duty cycle will vary around its original value, following:

$$d(t) = \frac{R_{eq}}{V_{in}} i_0 + \frac{\omega_b L_{eq} - R_{eq}}{V_{in}} i_0 . e^{-\omega_b . t} \tag{2.20}$$

From (2.20), the maximum duty cycle variation ΔD_{max}, occurs therefore at the time when load step change occurs and is given by:

$$\Delta D_{max} = \frac{\omega_b . L_{eq}}{V_{in}} . i_0 \tag{2.21}$$

The duty cycle will then slowly stabilize at a new steady state value, which differs from the previous one by $R_{eq}.i_0/V_{in}$. This small correction in the steady state duty ratio is in fact to compensate the power loss change due to the different current now carried by the VRM.

To prevent the duty cycle saturation during the transient, the duty ratio must be contained in the [0, 1] interval. Hence, if D is the steady state duty cycle, ΔD_{max} must be less than 1-D for load step up, and less than D for load step down. Therefore, the critical inductances, for load step up and step down of magnitude i_0, can be respectively estimated by:

$$L_{c\uparrow} = \frac{(1-D)V_{in}}{\omega_b . i_0} \tag{2.19}$$

$$L_{c\downarrow} = \frac{D.V_{in}}{\omega_b . i_0} \tag{2.20}$$

Similarly, for a fixed inductor value, a critical bandwidth ω_{bc}, can also be defined and be estimated by the following:

$$\omega_{bc\uparrow} = \frac{(1-D)V_{in}}{L_{eq}.i_0} \text{ (for step up)} \tag{2.21}$$

$$\omega_{bc\downarrow} = \frac{D.V_{in}}{L_{eq}.i_0} \text{ (for step down)} \tag{2.22}$$

For the chosen bandwidth of 120 KHz, and a maximum load step of 90A, the critical inductance is estimated to 148 nH for load increase, and 28 nH for load decrease, which are in confirmation with the simulated results presented in the previous section. Normally, the smaller of these two inductance values is chosen for designing an optimized converter. Hence, in the following part, where the four phase converter is simulated, in each channel, the inductance will be set at 30 nH × 4, that is at 120 nH.

2.3 Four phase interleaved converter: simulation results

The four-phase interleaved converter, as presented in Section 2.1.5, is simulated. The inductor in each phase is fixed to be equal to four times the critical inductance of 30 nH calculated in the previous section and is placed in series with a resistance of 0.8 mΩ (as assumed in Section 2.1.5). Finally, the voltage controller parameters are fixed according to Table 2.3 corresponding to an equivalent inductance of 30 nH.

The output voltage responses in the multiphase converter and in the equivalent single phase converter are compared in Fig. 2.17 and 2.18, for a load increase and load decrease of 90 A respectively.

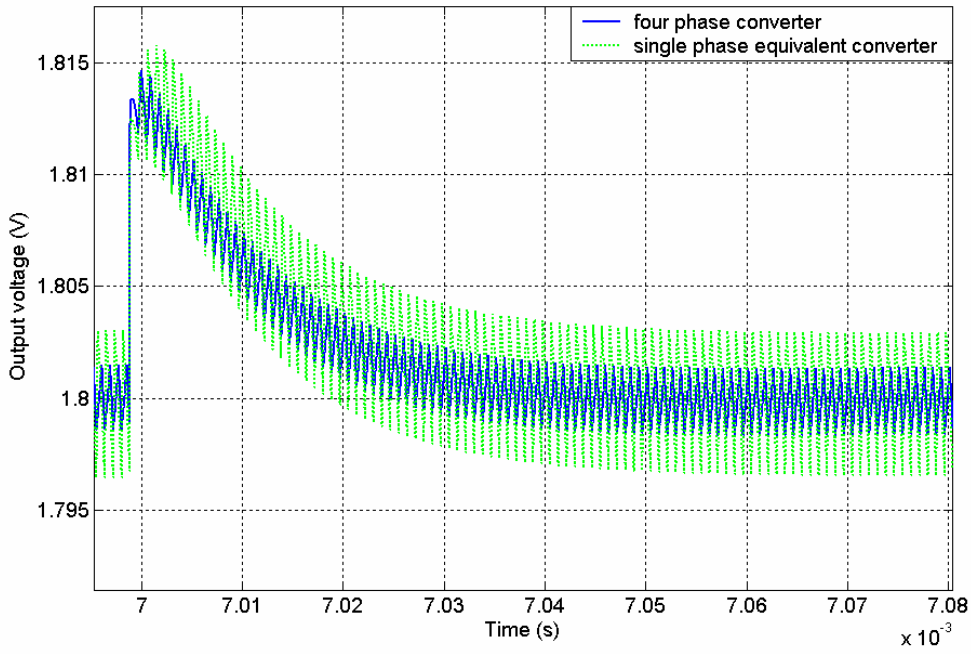

Fig. 2.17 Output voltage response to a load decrease of 90A, in a multiphase converter, and its equivalent single-phase converter.

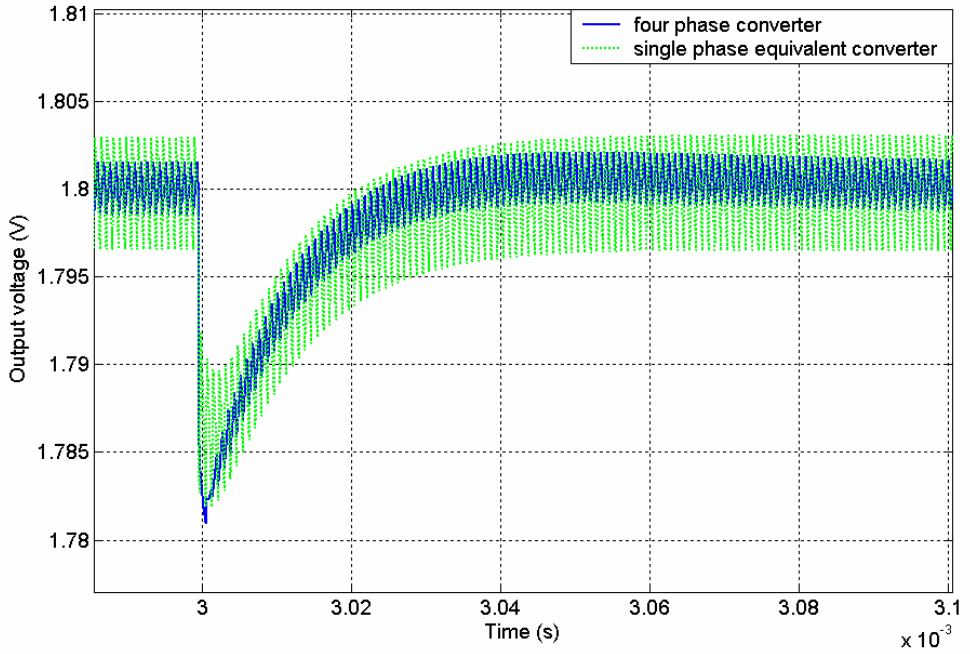

Fig. 2.18 Output voltage response to a load increase of 90A, in a multiphase converter, and its equivalent single-phase converter.

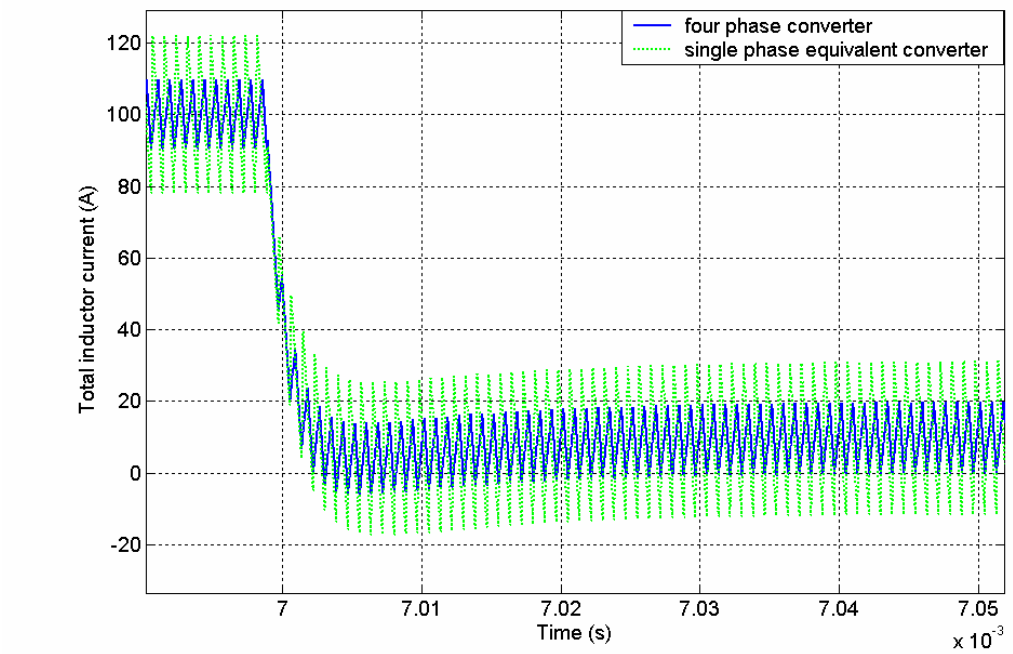

Fig. 2.19 Total inductor current in the multiphase converter and in the single phase equivalent converter.

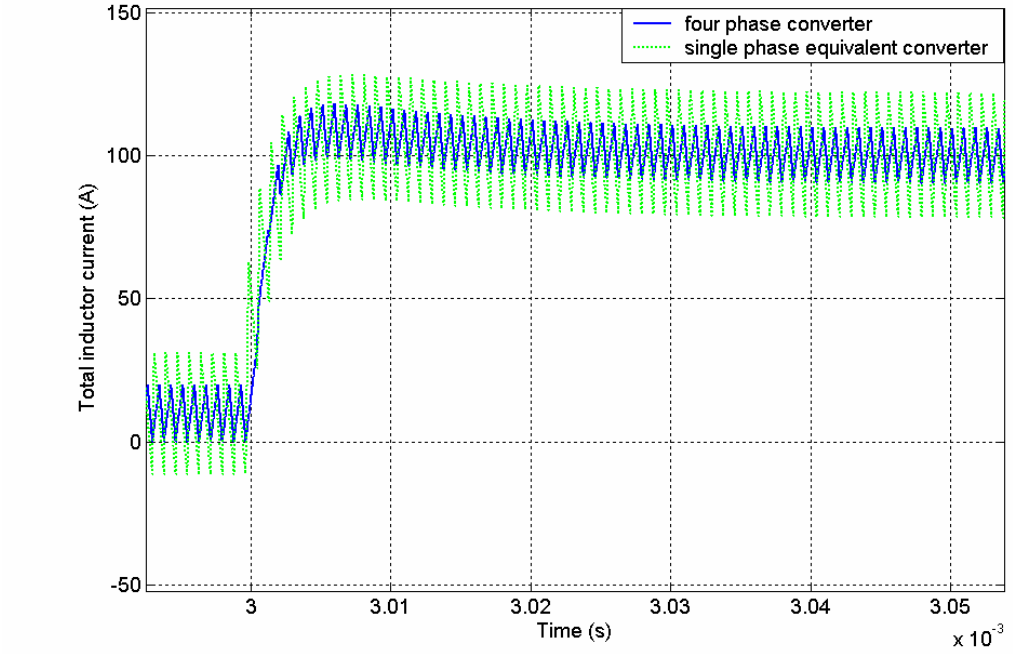

Fig. 2.20 Total inductor current in the multiphase converter and in the single phase equivalent converter.

As expected the voltage overshoot and undershoot at the step time are the same. However, the multiphase converter output voltage recovers faster than the single phase equivalent circuit. This is due to the ripple reduction effect, which was not fully taken into account when simplifying the interleaved converter into a single phase circuit. Hence, as shown in Figs. 2.19 and 2.20, although the average total inductor current have similar waveforms in the single phase equivalent circuit and in the multiphase converter, the interleaved converter exhibits better dynamics and steady state performance because of the output current ripple reduction. This shows again the superiority of the interleaved converter over the simple synchronous converter, although it uses a lower switching frequency.

By using only the output voltage in the feedback loop, the bandwidth is here maximized to be 120 KHz, although a switching frequency of only 300 KHz is being used. From the simulation results, with such a bandwidth, the VRM would fulfill most of the CPU requirements. However, as will be shown in the following, when using VMC, the inductor current is not controlled and therefore the load may be shared unequally among the channels due to component mismatches [45].

So far, in the simulations, all the four phases were having exactly the same inductor values, which may not be possible in practice. Hence a small variation of 2 % in the inductance value is now introduced in the simulations, in order to analyze the impact of these inequalities in the current sharing. The resulting current in the four phases are presented in Fig. 2.21 and 2.22, in the case of a high load of 100 A and in the case of light load of 10 A. It is shown that even in steady state, in each channel there are significant disparities in the current being carried. Hence, for a load current of 100 A, an average current of 30 A is flowing through one phase, whereas another channel carries only an average current of 20 A.

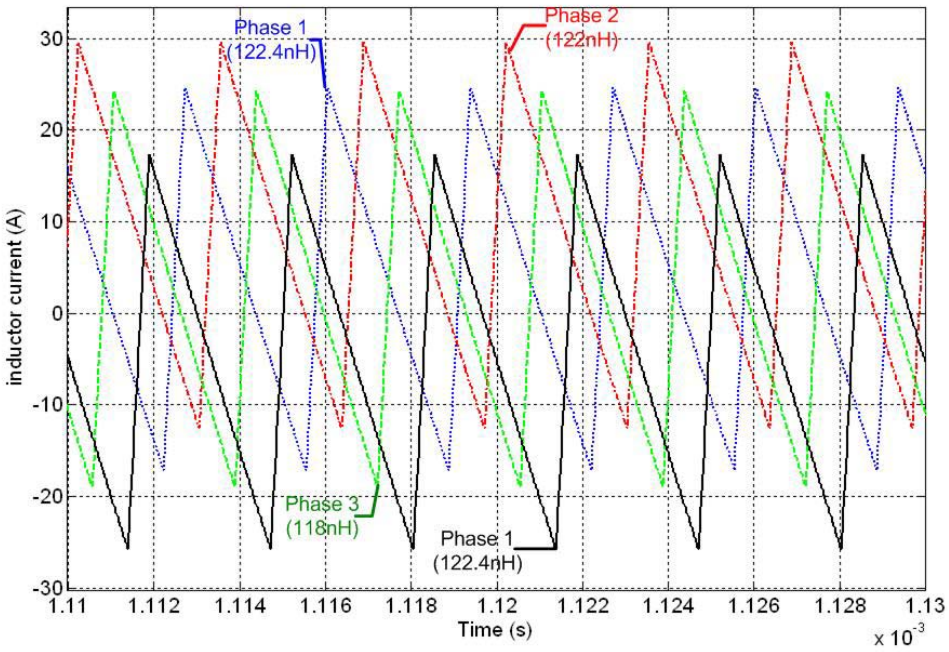

Fig. 2.21 Inductor current in each phase for a light load of 10A

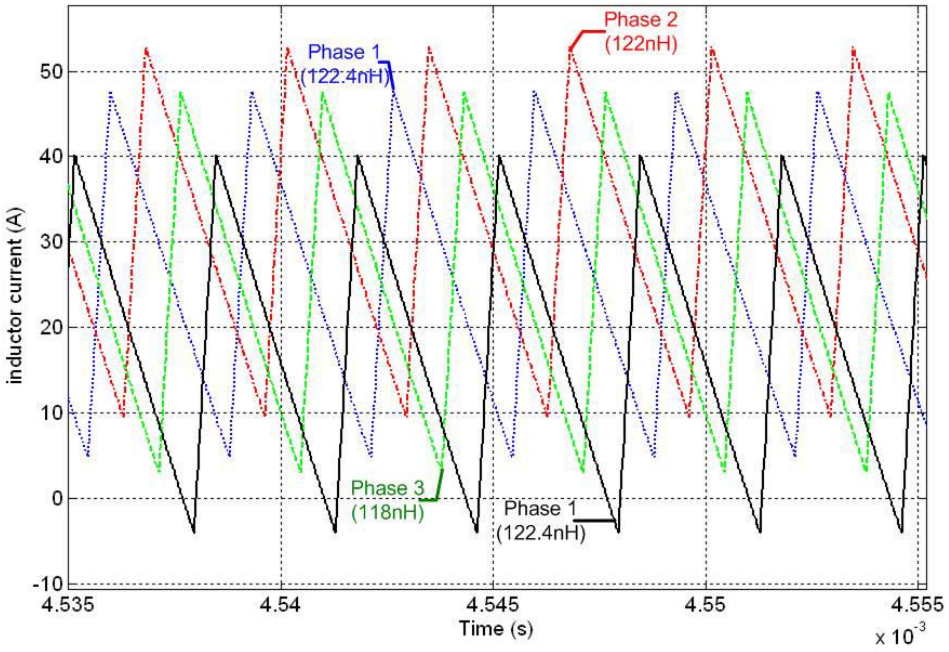

Fig. 2.22 Inductor current in each phase for a high load of 100A

These current flow disparities are found to increase further when the inductance values differ by a greater amount. This poor current sharing in the multiphase converter when the inductance values are not exactly identical to each other can be explained by the following.

As the inductors are different, the multiphase converter loses its symmetry and each phase behavior differs. Overall, the VMC scheme ensures that the total average inductor current is equal to the load. However, if the load current is not shared equally among the channels, the controller will not correct it. In the actual converter, since all the channels differ slightly from one another, the load is naturally shared unequally. Besides inductor value mismatches, other mismatches among the channels, such as for example mismatches in the gate characteristics of the series MOSFETs, can also be expected to cause differences in the power handled in each channel. These current disparities cause an efficiency drop in the converter and a poorer heat management. Besides, it may damage the circuit components, since they are generally selected assuming an equal current sharing among the phases, as shown in section 2.1.

Thus, usually, today's VRM designers add a current loop in each phase to force accurate current sharing. In the following chapter, two popular current control methods, called Average Current Mode Control (ACMC) and Peak Current Mode Control (PCMC), will be presented.

2.4 Conclusion

In this chapter, the selection of the various components and parameters for the popular four phase converter used in today's VRM have been presented. A simple and once popular control scheme, called Voltage Mode Control, has been presented and the design process investigated. For this purpose, the multiphase circuit has been shown to be equivalent to a simple single phase buck converter. Then, a large signal linear model for this circuit has been proposed and shown to be accurate. This model is useful in the design of the voltage controller and analysis of the dynamic performance of the converter. Through simulation and analysis, it has also been demonstrated that for a given control bandwidth, there exists an inductance value, called critical inductance, for which the dynamic performance of the converter is optimized while keeping the ripple minimum. Methods to estimate its value in a VMC scheme has been presented. Finally, the optimized four phase converter with VMC has been simulated. While ideally VMC works very well with the multiphase buck converter, it was shown that small variations in inductances lead to unequal current sharing among the phases during the transient as well as the steady state period. This renders the VMC scheme unsuitable for powering today's microprocessor. In the next chapter, current mode control methods, which prevent this situation from occurring, will be presented and analyzed.

CHAPTER 3

CURRENT MODE CONTROL METHODS

3.0 Introduction

The four phase converter has been introduced and the design methodology for the Voltage Mode Control has been presented in the second chapter. It has also been shown that though capable of high bandwidth, the VMC scheme fails to control the current sharing among the channels both during steady-state and transient. As a result, there is always a current unbalance in the system which can cause an overall reduction in efficiency and also reduce the life span of the converter. Besides, the ratings of components in individual phases have to be kept larger than needed to accommodate this unbalance. Hence, in order to prevent this situation, current control schemes are being preferred in modern day VRMs.

In this chapter, the two most popular methods, Average Current Mode Control (ACMC) and Peak Current Mode Control (PCMC), are investigated. In each of these controls, the addition of the current loop brings additional issues in terms of stability, accuracy and speed, which will be covered. The concept of critical inductance introduced in the last chapter is expanded for these current mode controls and methods to estimate it are also presented. Finally, small variations in the circuit parameters will be introduced and the system simulated in order to investigate their effect on particularly the load sharing among the channels.

The ACMC and PCMC designs are examined separately, and simulations are based on the same four phase converter introduced in Section 2.1.5.

3.1 Average current mode control

3.1.1 Presentation

The overall ACMC scheme implemented on an n-phase interleaved converter is shown in Fig. 3.1.

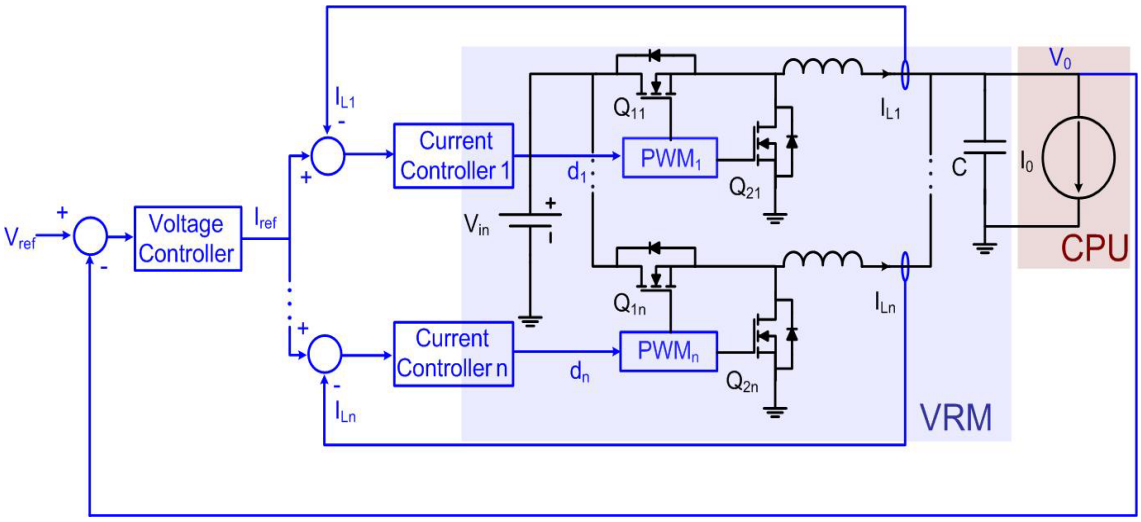

Fig. 3.1 Average Current Mode Control scheme in an n-phase buck converter

As shown in this figure, this control scheme is a multiloop system, where n number of current loops are in a parallel configuration and placed inside a common voltage loop. Its mode of operation can be explained as follows.

The voltage loop fixes the reference average current I_{ref} to be carried by each inductor, according to the output voltage error. Then, in each channel, the inner current loop will ensure that the average inductor current follows I_{ref} accurately, by providing the appropriate duty cycle.

When used in multiphase converters, such a complex control scheme offers many advantages when compared to the simpler VMC scheme, particularly the current controlling capability in each channel [59]. Since the reference current signal is common to each current loop, each channel will carry equal amount of current,

resolving the load sharing issue in multiphase converters. However, as will be shown in the next sections, the control design increases in complexity, and the control bandwidth has to be drastically reduced for achieving good stability and performance.

In the following, the control design methodology, inspired from methods generally used in single phase converter [60]-[61], is presented for the four phase converter introduced in the second chapter. The current controller design is first investigated, followed by the voltage controller design.

3.1.2 Current Controller design

The multiphase converter is usually built in a symmetrical manner. Therefore, the same current controller is generally used for each channel. Consequently, in this section, the current controller design process is detailed for one of the phases.

The current loop scheme in one channel is presented in Fig. 3.2, where I_L is the average inductor current in that channel. Since the inductor current slope depends upon the output voltage, which gets disturbed during load transition, the load is also represented in Fig. 3.2 as a perturbation on the system. The current controller design is hence based on the average inductor current to duty cycle transfer function, which is derived in the following.

Fig. 3.3 shows the circuit schematic for one channel. From this figure, the average inductor current in one cycle is written as:

$$L\frac{d\langle I_L\rangle}{dt} = \langle D\rangle V_{in} - \langle D\rangle . R_1 \langle I_L\rangle - \left(1-\langle D\rangle\right) R_2 \langle I_L\rangle - R_3 \langle I_L\rangle - \langle V_0\rangle \tag{3.1}$$

Note: As in the last chapter, the symbol <> stands for the respective average value of a variable in one cycle, the capital letter for the steady state value, and small letter is used for the small perturbation around it.

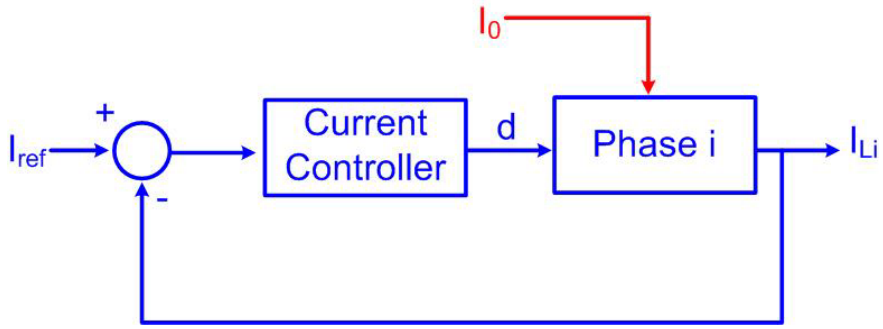

Fig. 3.2 Current loop scheme

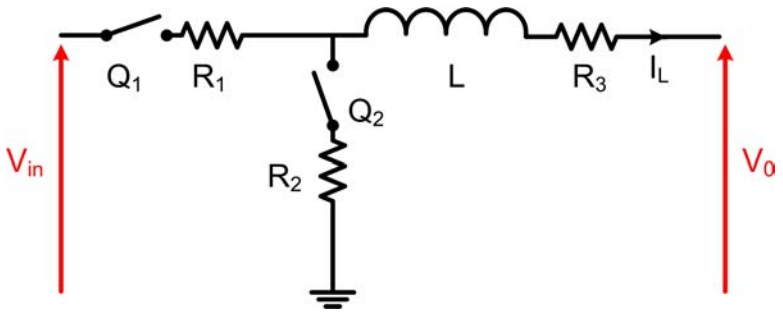

Fig. 3.3 One channel circuit diagram

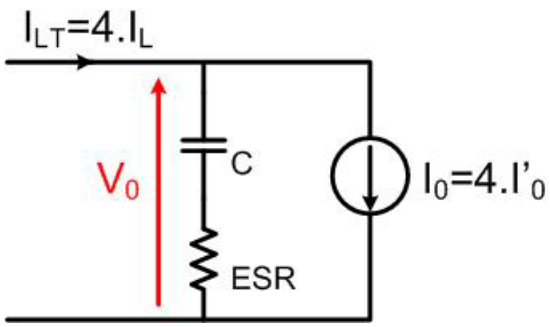

Fig. 3.4 Output Voltage System

Performing a small signal analysis as was done in the second chapter, the following linear equation can be obtained:

$$L\frac{di_L}{dt} = \left(V_{in} - \left(R_1 - R_2\right).I_L\right)d - \left(D.R_1 + \left(1-D\right)R_2 + R_3\right)i_L - v_0 \tag{3.2}$$

In order to eliminate v_0 from (3.2), the output voltage equation is derived in the following. For this purpose, the circuit diagram of the total inductor current feeding the output capacitor and the CPU, as shown in Fig. 3.4, is considered. By assuming the current to be identical in all the four phases, the total average inductor current is equal to four times the average current in one phase. Also, to keep the symmetry in the equations, the load I_0 is also replaced by a value of $4.I_0'$, where I_0' is the load current corresponding to each phase, as shown in Fig. 3.4.

Thus, the following equation can be obtained:

$$\begin{cases} C\dfrac{dv_c}{dt} = 4\left(i_L - i_0'\right) \\ v_0 = ESR.4.\left(i_L - i_0'\right) + v_c \end{cases} \tag{3.3}$$

It may be noted that (3.2) is valid for small signal perturbations only whereas (3.3) is valid both for small signal and large signal perturbations.

Finally by combining (3.2) and (3.3), and transforming into the Laplace domain, we obtain the following small signal linear model:

$$i_L = \frac{\left(V_{in} - \left(R_1 - R_2\right)\langle I_L\rangle\right)Cs}{LCs^2 + \left(R_{ieq} + 4ESR\right)Cs + 4}d + \frac{4\left(1 + ESR.Cs\right)}{LCs^2 + \left(R_{ieq} + 4ESR\right)Cs + 4}i_0' \tag{3.4}$$

where $R_{ieq} = D.R_1 + \left(1-D\right)R_2 + R_3$ (3.5)

However, in the second chapter, it has already been demonstrated, that for the range of variation of the load current in usual VRMs, $(R_1\text{-}R_2).\langle I_L\rangle$ is negligible compared to V_{in}. Hence, (3.4) can be simplified into:

$$i_L = \frac{V_{in}.Cs}{LCs^2 + \left(R_{ieq} + 4ESR\right)Cs + 4}d + \frac{4\left(1 + ESR.Cs\right)}{LCs^2 + \left(R_{ieq} + 4ESR\right)Cs + 4}i_0' \tag{3.6}$$

Once again, we verify whether the above small signal linear model continue to remain valid when large signal perturbations are considered. For this purpose, a step response comparison is conducted through simulations, using (3.6) and the actual four phase converter with current mode control. In (3.6) the steady state duty cycle D is fixed at 0.155, and inductors of 1 μH are selected. The simulation results are presented in Fig. 3.5 and Fig. 3.6.

These simulation results show a similar behavior for the inductor current as for the output voltage in the second chapter. Indeed, the model follows accurately the actual converter for a step load, whereas it lacks some dynamic precision when large duty ratio values are considered. This is again due to the neglecting of non linear terms in (3.2), which were in terms of d. Nevertheless, even with the limitations of (3.6), the proposed model is still a fair large signal approximation, and will be used in the design of the current controller.

Hence, the inductor current to duty cycle transfer function i_L/d and inductor current to load i_L/i_0' can be estimated by:

$$\frac{i_L}{d} = G_{id} = K_{id} \frac{\frac{s}{\omega_{iC}}}{\frac{s^2}{\omega_{i0}^2} + \frac{s}{Q_i.\omega_{i0}} + 1} \tag{3.7}$$

$$\frac{i_L}{i_0'} = G_{ii} = \frac{1 + \frac{s}{\omega_{ESR}}}{\frac{s^2}{\omega_{i0}^2} + \frac{s}{Q_i.\omega_{i0}} + 1} \tag{3.8}$$

where, $\omega_{i0} = \frac{2}{\sqrt{LC}}, Q_i = \frac{8}{R_{ieq} + 4ESR}\sqrt{\frac{C}{L}}, \omega_{ESR} = \frac{1}{ESR.C}, \omega_{iC} = \frac{1}{C}, K_{id} = \frac{V_{in}}{4}.$

In the following, the transfer function obtained in (3.7) is used to design the current controller. In the calculations, a steady state duty cycle of 0.155 is employed.

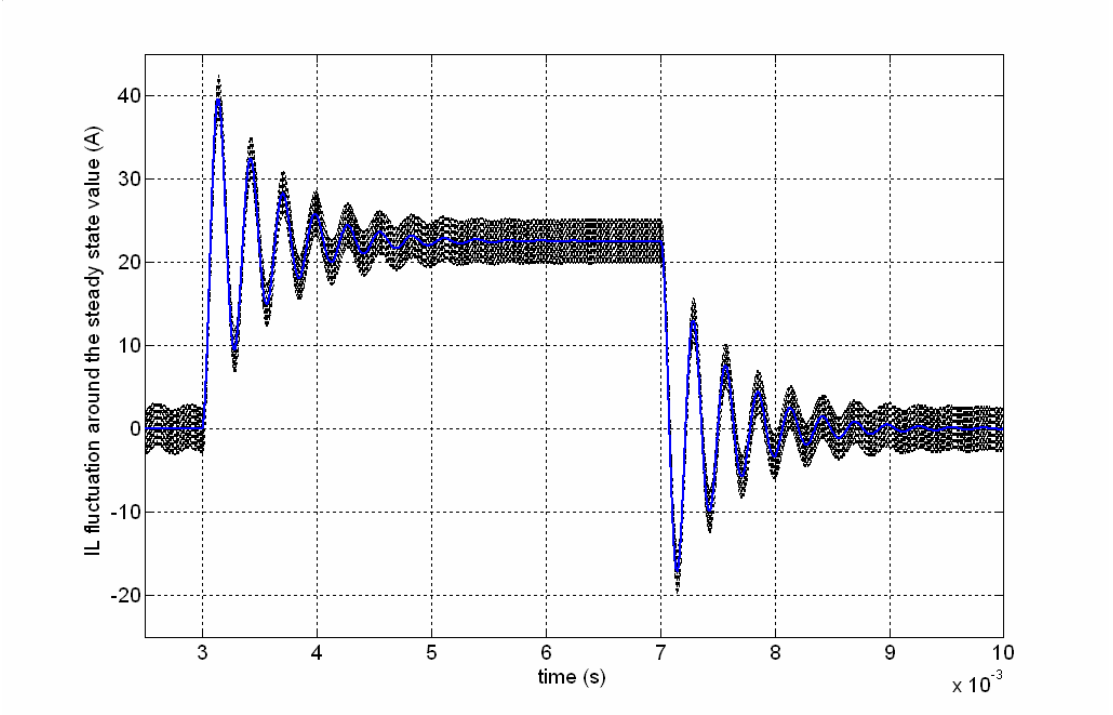

Fig. 3.5 Inductor current fluctuation in one channel due to a step load from 10 A to 100 A using the actual multiphase converter and the large signal model (3.2)

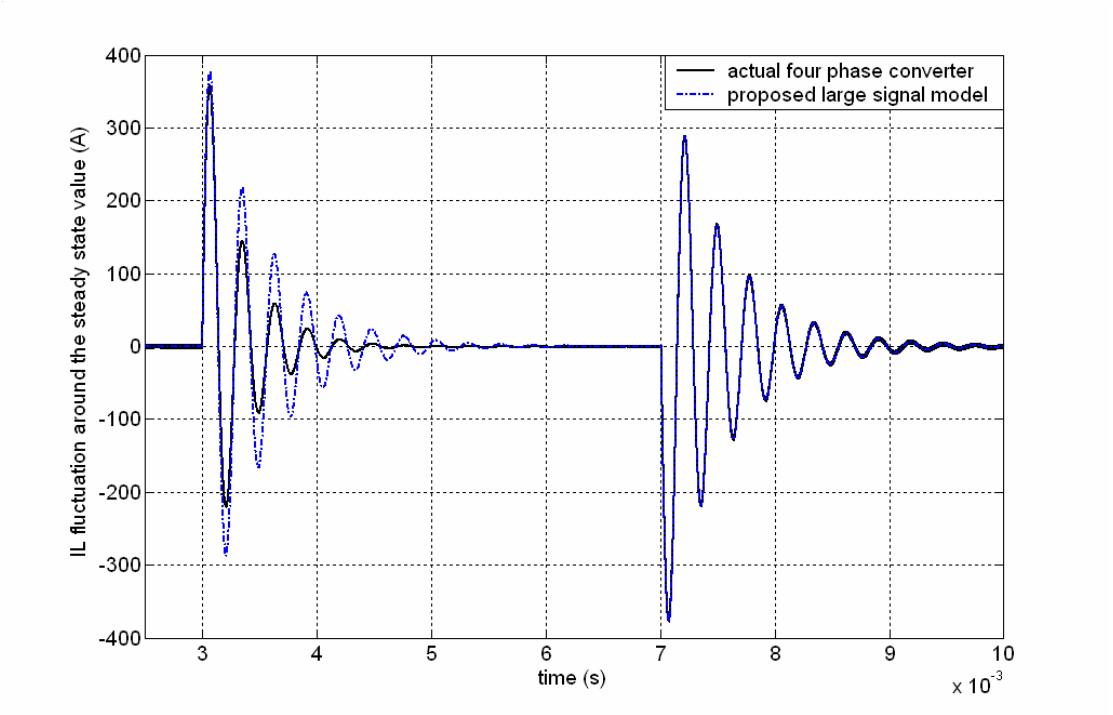

Fig. 3.6 Inductor current fluctuation in one channel due to a step variation in the duty cycle from 0.16 to 0.96 using the actual multiphase converter and the large signal model (3.2)

For an inductance of 5 μH, the Bode diagram of i_L/d transfer function is presented in Fig. 3.7. Moreover, it has been noticed that for the range of inductance values studied in this thesis, the frequency response of G_{id} has a similar characteristics. Hence, though the following design methodology is based on an inductance of 5 μH per phase, the same procedure can be applied for other inductor values also.

Based on the plant transfer function in Fig. 3.7, a double pole at the origin is added in the controller, in order to have a single integrator in the inner open loop transfer function and hence, avoid any steady state error in the current loop. Since in the following section the voltage loop will be designed to be much slower than the inner current loop, the tracking errors need not be considered. A double zero near the resonant frequency ω_{i0} is also added in the controller for stability purposes. Finally, the DC gain is adjusted so as result in a reasonable system bandwidth. Since the switching frequency f_s is 300 kHz, the inductor current will also have a natural ripple frequency of 300 kHz. Based on this, the cross over frequency is chosen to be around 30 kHz. With this design, the phase margin is found to be close to 85°.

Thus, overall, the controller has the following form:

$$C_{ii} = K_{ii} \frac{\left(1+\frac{s}{\omega_{zi}}\right)^2}{s^2} \tag{3.9}$$

Given the design methodology, the open loop transfer function may be approximated to ω_{bi}/s (ω_{bi} being the inner loop bandwidth), as shown in Fig. 3.8, where both the frequency response of the resulting open loop transfer function T_{ii}, and its approximation into ω_{bi}/s are presented. Also, since G_{id} depends on the inductance value, the controller has to be adjusted each time the inductor is changed, in order to keep the same open loop bandwidth and phase margin.

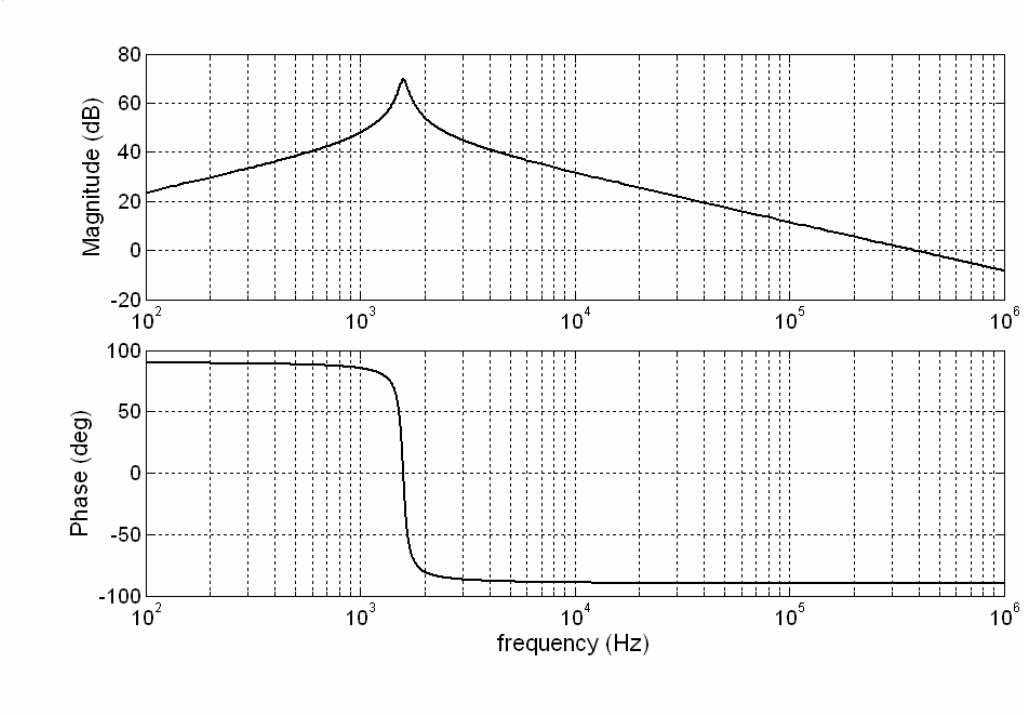

Fig. 3.7 Inductor current to duty cycle transfer function for 5μH inductance

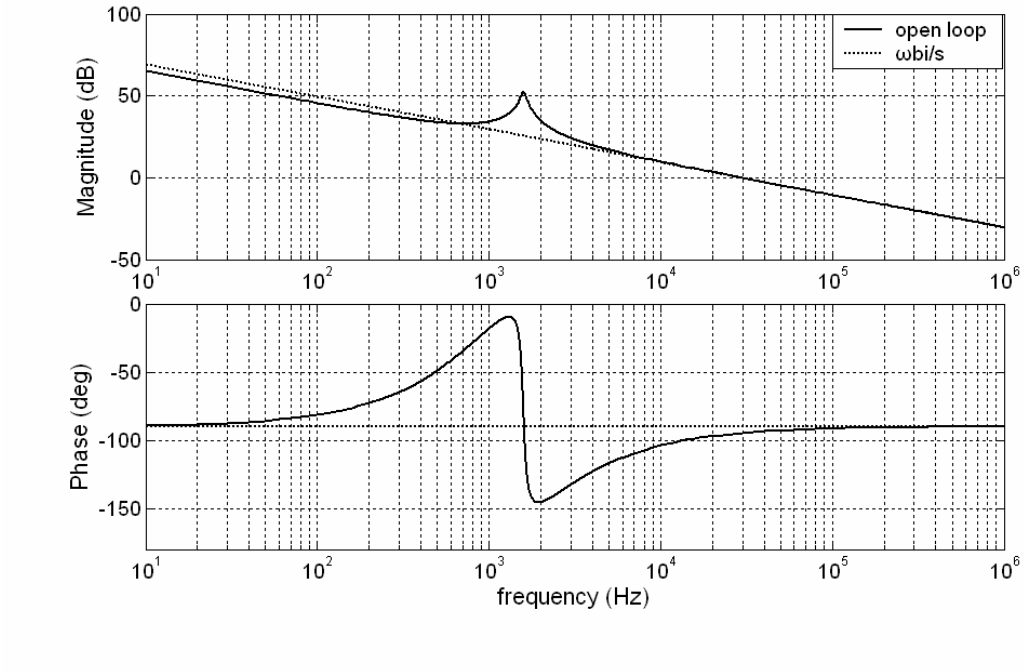

Fig. 3.8 Open loop corrected system for the current loop and its approximation

3.1.3 Voltage Controller design

The voltage controller design method for ACMC presented in the following is generally similar to that used for single phase converters [60]-[61].

In order to avoid loop interaction, the voltage loop is designed to be much slower than the current loop, which is assumed to be fast and accurate. As a consequence, when considering the voltage loop, each channel together with its current loop can be replaced by an instantaneously controllable current source. Hence, in the control diagram each current loop can be simplified into a simple unity gain block. Moreover, since each current loop receives the same control signal I_{ref}, each channel carries the same amount of current, which after being summed, feeds the output capacitor and the load. Therefore, the overall control scheme for the four phase converter can be given by the simplified block diagram shown in Fig. 3.9. The output equivalent circuit presented in this figure is the same as that introduced in Fig. 3.4. The load disturbance on the output voltage is also represented in Fig. 3.9.

In the following, the output voltage to inductor current transfer function is derived, in order to design the voltage controller. In order to be able to relate to the analysis in the preceding section, the load I_0 is replaced by $4.I_0$'.

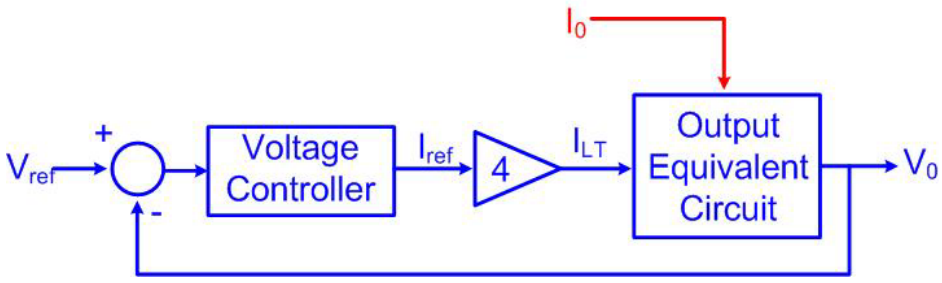

Fig. 3.9 Simplified voltage loop scheme for the four-phase converter

From Fig. 3.4, the following equation can be directly derived:

$$v_0 = 4.\frac{1+ESR.Cs}{Cs}\left(i_L - i_0'\right) \tag{3.10}$$

Hence, the output voltage to reference current transfer function v_0/i_{ref} is given by:

$$\frac{v_0}{i_{ref}} = G_{iv} = 4.\frac{1+ESR.Cs}{Cs} \tag{3.11}$$

The Bode diagram of this transfer function is shown in Fig. 3.10. The system itself includes an integrator. However, since the same integrator is present in the load disturbance also, an additional integrator in the voltage controller is required in order to avoid any steady state error. One zero will be added for stability purposes at the frequency ω_{zv}, and one pole to compensate the zero introduced by the capacitor ESR. Finally, to ensure the validity of the design approach, the voltage loop is designed five to ten times slower than the current loop. Hence, the DC gain of the controller is adjusted in order to have a bandwidth ω_{bv} chosen to be a maximum of five times less than the current loop bandwidth: $\omega_{bv}=\omega_{bi}/5$.

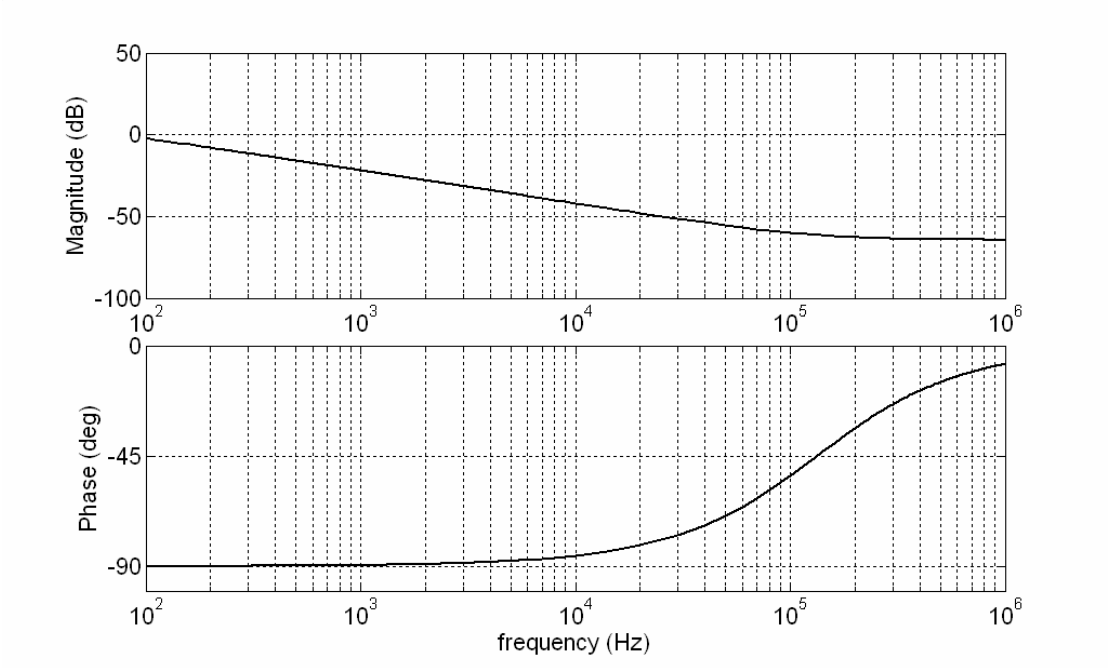

Fig. 3.10 v_0/i_{ref} Bode diagram

Thus, overall, the controller has the following form:

$$C_{iv} = K_{iv} \frac{\left(1+\frac{s}{\omega_{zv}}\right)}{s\left(1+\frac{s}{\omega_{hv}}\right)} \tag{3.12}$$

In the simulations, the following controller parameters have been chosen based on the above design methodology.

K_{iv}=9.62×10^4, ω_{zv}=1256,6 rad/s, ω_{hv}=83.33×10^4 rad/s

Since G_{vi} does not depend on the inductance value, the voltage controller is not changed when considering different inductors.

With the above design methodology, the open loop transfer function may be approximated to:

$$T_{iv} = \omega_{bv} . \frac{s+\omega_{zv}}{s^2} \tag{3.13}$$

The frequency response of the resulting open loop transfer function T_{iv}, and its approximation as given in (3.13) are presented in Fig. 3.11 for comparison.

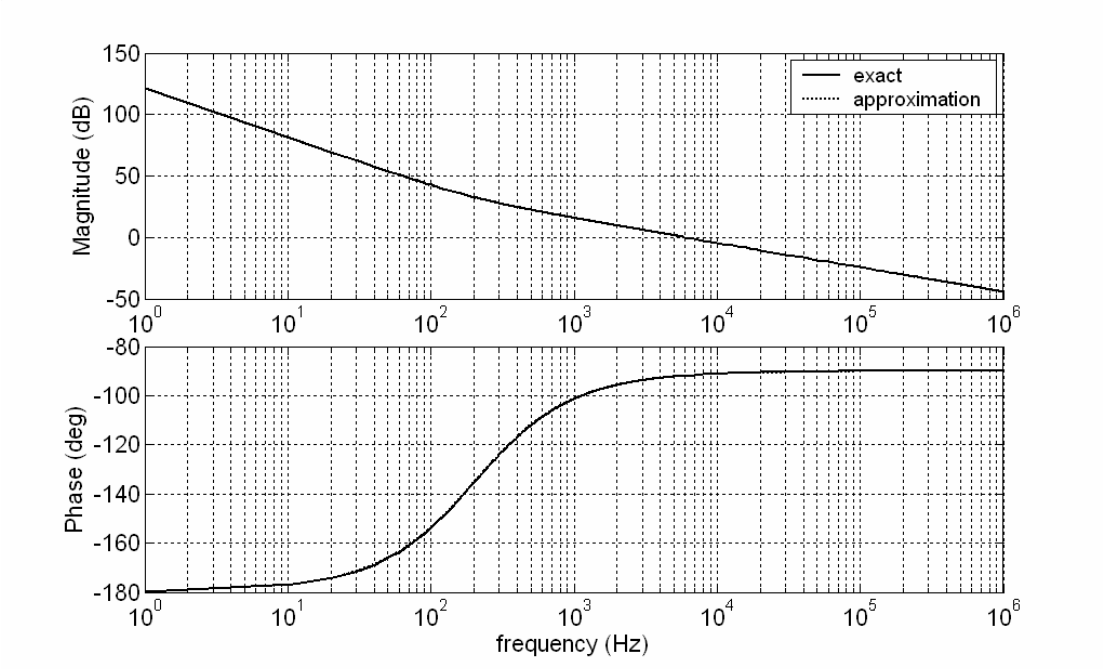

Fig. 3.11 Open loop corrected system for the simplified voltage loop and its approximation

In the following section, given the overall designed control scheme, the system is theoretically analyzed in order to obtain the critical inductance value, as per the concepts introduced in the second chapter.

3.1.4 Critical inductance analysis

As mentioned in the second chapter, the critical inductance for a given load disturbance, is obtained by finding the largest inductance, which avoids the duty cycle saturation. For this purpose, the transfer function d/i_0 of the variation of the duty cycle d in one channel over the load variation i_0, is first derived.

Assuming the four channels of the multiphase converter to be similar, the overall control scheme presented in Fig. 3.12 can be derived. As mentioned earlier, the variable symbol I_0' is used instead of I_0.

Also, in the following, for the sake of simplification of notation, G_{ni} is defined as:

$$G_{ni} = \frac{1}{LCs^2 + \left(R_{eq} + 4ESR\right)Cs + 4} \tag{3.14}$$

Therefore, the inductor current variation can be re-expressed in terms of d and i_0' as follows:

$$i_L = V_{in}Cs.G_{ni}.d + 4\left(1 + ESR.Cs\right)G_{ni}.i_0' \tag{3.15}$$

Furthermore, by substituting (3.15) into (3.10) the output voltage variation v_0 can also be expressed in terms of d and i_0':

$$v_0 = 4\frac{1+ESR.Cs}{Cs}\left[V_{in}Cs.G_{ni}.d + \left(4\left(1+ESRCs\right)G_{ni} - 1\right)i_0'\right], \tag{3.16}$$

which can be simplified into

$$v_0 = 4V_{in}\left(1+ESRCs\right)G_{ni}.d - 4\left(1+ESRCs\right)\left(Ls + R_{eq}\right)G_{ni}.i_0' \tag{3.17}$$

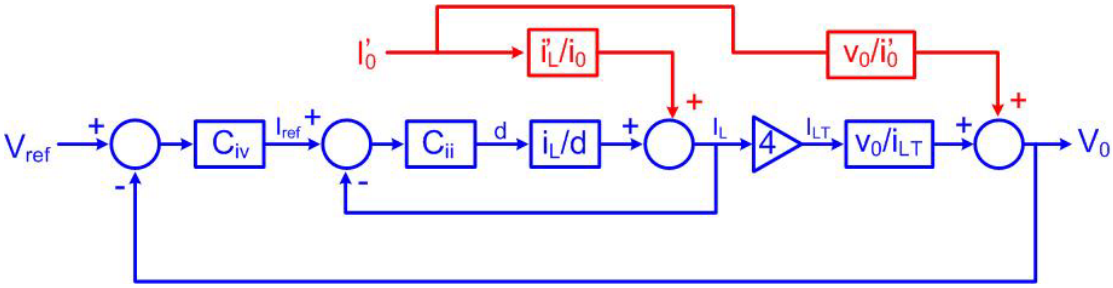

Fig. 3.12 Overall ACMC scheme

From the block diagram presented in Fig. 3.12, when a load perturbation of magnitude $4.i_0$' occurs, the output voltage fluctuation v_0 leads to a variation in the reference current i_{ref} provided by the voltage controller, which causes finally a duty cycle variation d, as follows:

$$i_{ref} = -C_{iv}.v_0 \tag{3.18}$$

$$d = C_{ii}\left(i_{ref} - i_L\right) = -C_{ii}.C_{iv}.v_0 - C_{ii}.i_L \tag{3.19}$$

Hence, by substituting into (3.19) the expressions of v_0 and i_L found in (3.15) and (3.17), the following equation for duty cycle can be obtained:

$$d = -C_{ii}C_{iv}.4\left(1+ESRCs\right)V_{in}G_{ni}.d + C_{ii}C_{iv}.4\left(1+ESRCs\right)\left(Ls+R_{eq}\right)G_{ni}.i_0' - C_{ii}.V_{in}Cs.G_{ni}.d - C_{ii}.4\left(1+ESRCs\right)G_{ni}.i_0' \tag{3.20}$$

Equation (3.20) can also be expressed in terms of the open loop transfer functions T_{iv} and T_{ii} since

$$T_{iv} = C_{iv}.G_{iv} = C_{iv}.4\frac{1+ESR.Cs}{Cs} \tag{3.21}$$

$$T_{ii} = C_{ii}.G_{ii} = C_{ii}.V_{in}Cs.G_{ni} \tag{3.22}$$

Hence,

$$d = -T_{ii}.T_{iv}.d + \frac{T_{ii}.T_{iv}}{V_{in}}\left(Ls+R_{eq}\right)i_0' - T_{ii}.d - 4\frac{1+ESR.Cs}{Cs}\frac{T_{ii}}{V_{in}}i_0' \tag{3.23}$$

Therefore, from (3.23) and given the open loop transfer functions T_{ii} and T_{iv} of the inner current loop and the outer voltage loop, the duty cycle d can be related to current i_0' as follows:

$$d = \frac{T_{ii}}{V_{in}\left(1+T_{ii}+T_{ii}T_{iv}\right)}\left[T_{iv}\left(Ls+R_{eq}\right)-4\frac{\left(1+ESR.Cs\right)}{Cs}\right]i_0' \tag{3.24}$$

Hence, for given open loop characteristics, the duty cycle to load current transfer function can readily be estimated using (3.24). In the control design procedure detailed in the previous sections, it has been shown that the open loop transfer functions can be approximated by:

$$T_{ii} = \frac{\omega_{bi}}{s} \tag{3.25}$$

$$T_{iv} = \omega_{bv}\frac{s+\omega_{zv}}{s^2} \tag{3.26}$$

Hence, given the current loop crossover frequency ω_{bi}, and the voltage loop bandwidth ω_{bv}, d/i_0' can be estimated by:

$$\frac{d}{i_0'} = \frac{\omega_{bi}}{V_{in}}\frac{\left(L\omega_{bv}-4ESR\right)s^2+\left(R_{eq}\omega_{bv}+L\omega_{zv}\omega_{bv}-4/C\right)s+R_{eq}\omega_{bv}\omega_{zv}}{s^3+\omega_{bi}s^2+\omega_{bi}\omega_{bv}s+\omega_{bi}\omega_{bv}\omega_{zv}} \tag{3.27}$$

In the following, (3.27) is used to estimate the duty cycle variation caused by a sudden load change of 90 A. Due to the complexity of this transfer function, the step response is not analytically expressed in the time domain as in the VMC case but rather obtained through simulations using MATLAB. In Fig. 3.13, the duty cycle variation for a step load of 90 A obtained through simulation is shown for three different inductance values.

Since it has been demonstrated that the load step down transient response is more critical than the response during load step up, the duty cycle variation due to a sudden load decrease of 90 A is alone investigated.

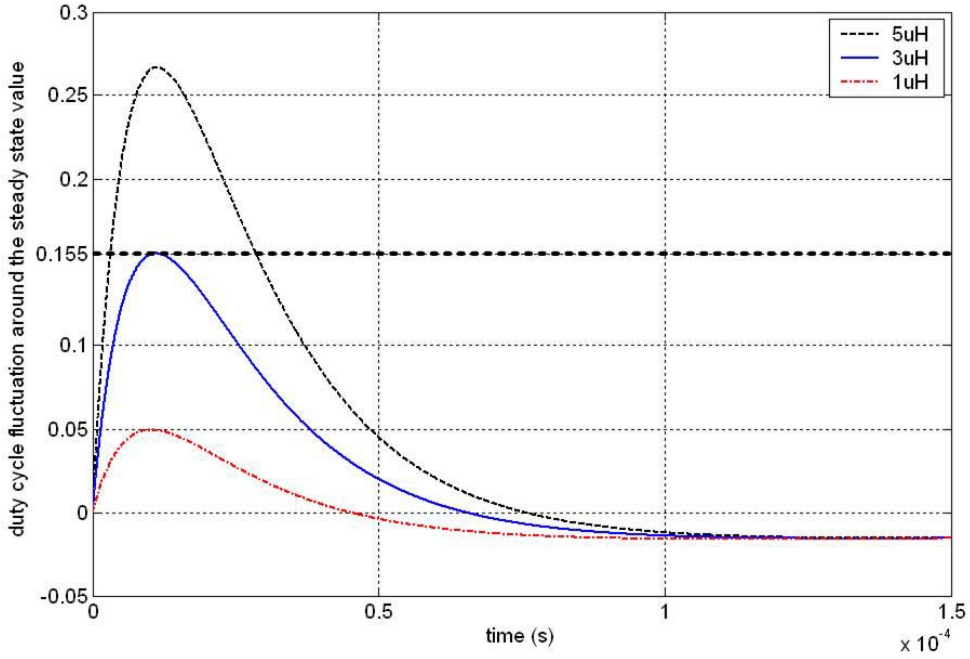

Fig. 3.13 Duty ratio fluctuation around the original steady state due to a step change in the load of 90A
Note: Duty cycle saturation has been ignored

During load step down, as the steady state duty cycle in the converter is close to 0.155, the duty cycle is allowed to decrease by only 0.155 during transient. Hence, from Fig. 3.13, the critical inductance, which is defined as the largest inductance that avoids the duty cycle saturation, is found to be close to 3 μH. These large critical inductance value found for ACMC as compared to VMC is due to the low bandwidth involved.

In the following section, simulations results are presented confirming the theoretically found critical inductance. The load sharing issues in the multiphase converter when the phase inductances are not identical are also investigated.

3.1.5 Simulation results for the dynamic performance of the converter

To verify the theoretically found critical inductance, the four phase converter is first simulated for five different inductance values: 1 μH, 2 μH, 3 μH, 4 μH and 5 μH. For a fair comparison, the current controller is adjusted each time to keep the same current loop bandwidth and phase margin. The DC gain and the zero frequency of the selected controller for these three different inductances are listed in Table 3.1. As in the design of the voltage controller in the VMC, an increase in required DC gain and a decrease in the zero frequency are noted when increasing the inductance value, in order to keep the same bandwidth.

The maximum voltage reached during load step down transient is also measured for each inductance and are listed in Table 3.1. From this table, it is shown that, the voltage overshoot decreases with increase in inductance. However, it stops decreasing further for inductances below 3 μH. As in the VMC scheme, this is again due to the stopping of duty cycle saturation.

TABLE 3.1 CURRENT CONTROLLER CHARACTERISTICS AND OUTPUT VOLTAGE OVERSHOOT FOR A LOAD STEP DOWN OF 90 A FOR DIFFERENT INDUCTANCE VALUES

L (μH)	5	4	3	2	1
K_{ii} ($\times 10^6$)	5	4.62	3.96	2.99	2.22
ω_{zi} (rad/s) ($\times 10^3$)	7.69	8.33	9.09	10	12.05
V_{max}	2.13	2.08	2.06	2.06	2.06

For inductances larger than 3 μH, the duty ratio saturates, and this causes the response to be slower if the inductance value is increased any further. This increases the inductor current falling time as shown in Fig. 3.14 (see the curves for 3 μH and 5 μH). The decreasing current falling rate causes higher output voltage deviation for inductance larger than 3 μH. It may be noted also in Fig. 3.14 that with 5 μH though the current has slowed down still it catches up with the waveforms with the smaller inductances by about 7.3 ms.

Fig. 3.15 shows the transient output voltage waveforms for the case of 5 μH, 3 μH and 1 μH, for a sudden load decrease from 100 A to 10 A. As shown in this figure, for the range of inductances considered in this section, the duty cycle saturation affects the transient response at the beginning of the transient (till about 7.3 ms). Consequently, the settling time for a 20 mV voltage band is not affected in any significant manner for inductances less than 5 μH.

These simulation results confirm also the theoretical value of the critical inductance found in the previous section.

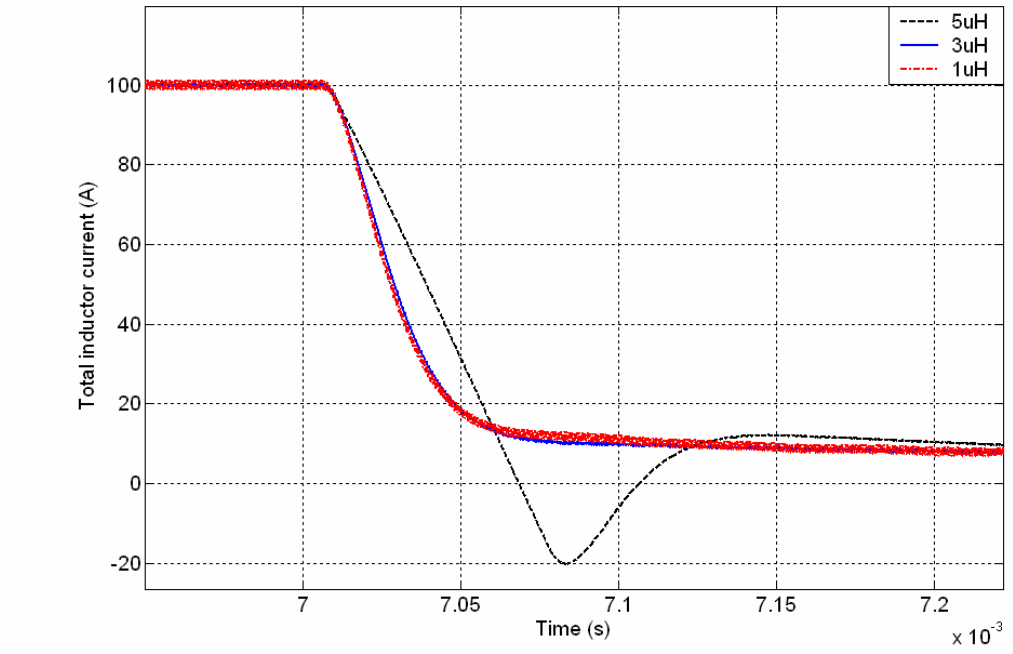

Fig. 3.14 Total inductor current waveforms for a load decrease from 100 A to 10 A in the four phase converter for three different values of inductance per phase.

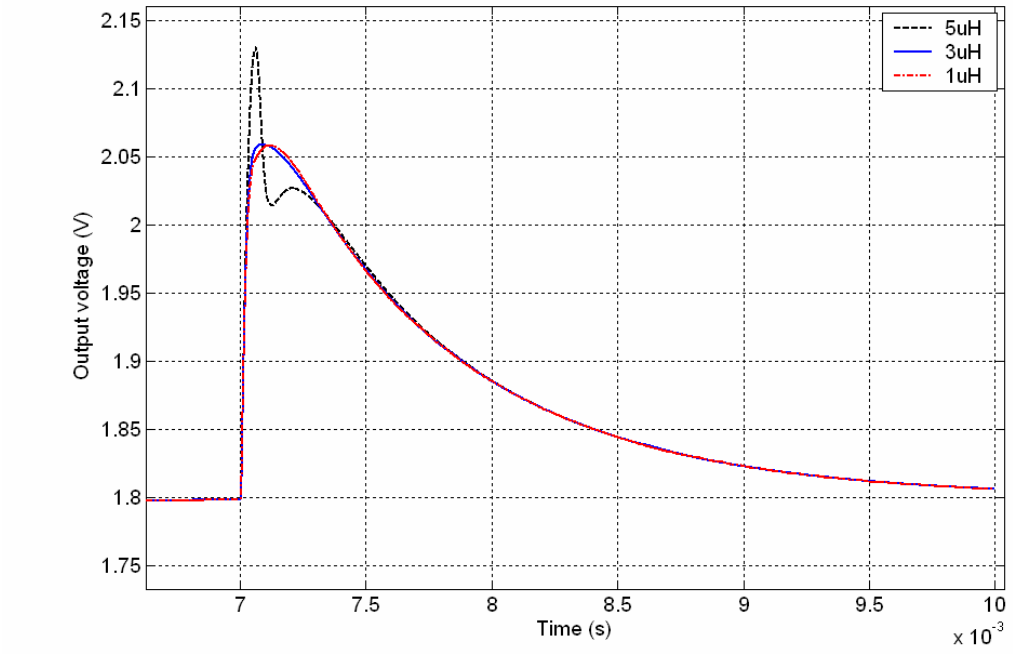

Fig. 3.15 Output voltage waveform during a load decrease from 100 A to 10 A in the four phase converter for three different values of inductance values per phase.

The inductance per phase is therefore nominally fixed at 3 μH. Next, in order to investigate the sensitivity of the converter to slight parameter changes, in particular the load sharing capability in transient as well as in steady state, the inductor in each phase is set at a value slightly different from 3 μH within a 10% margin. The inductor current waveforms for a load step down from 100 A to 10 A and vice versa are shown in Fig. 3.16 and Fig. 3.17 with these inductance values.

The load is shown to be shared equally among the channel both during transient and steady state, even though the inductances are assumed to differ from each other by as much as 10%. However, this equal current sharing benefit comes with a cost in the dynamic performance. Indeed, since with the ACMC scheme the control bandwidth has been decreased to only 6 kHz compared to the value of 120 kHz obtained for the VMC scheme, a comparison of Fig. 3.15 with Fig.2.17 reveals that both the voltage deviation and transient time have increased. Thus, the transient CPU requirements are not fulfilled with the designed ACMC scheme. In order to be able to use the ACMC scheme, the VRM designer must go for a higher switching frequency and then correspondingly increase the bandwidth or the designer must increase the output capacitor value even more. Both these approaches carry their own penalties, with the first approach resulting in higher losses and the second in larger VRM size.

In the following section, another popular control scheme called Peak Current Mode Control which allows a higher bandwidth to be realized is presented.

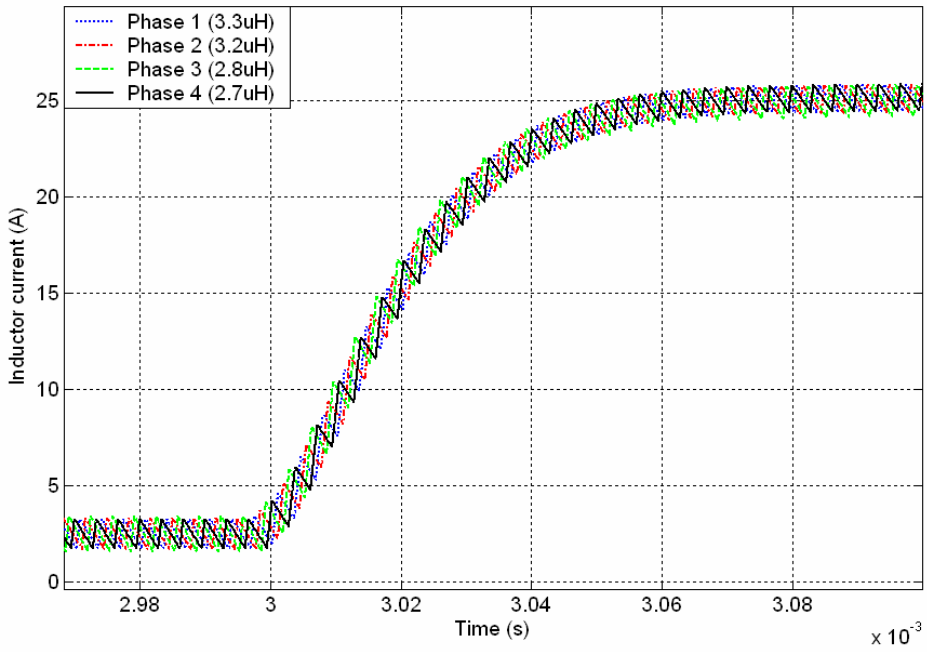

Fig. 3.16 Inductor current variation in each phase for a load increase from 10 A to 100 A

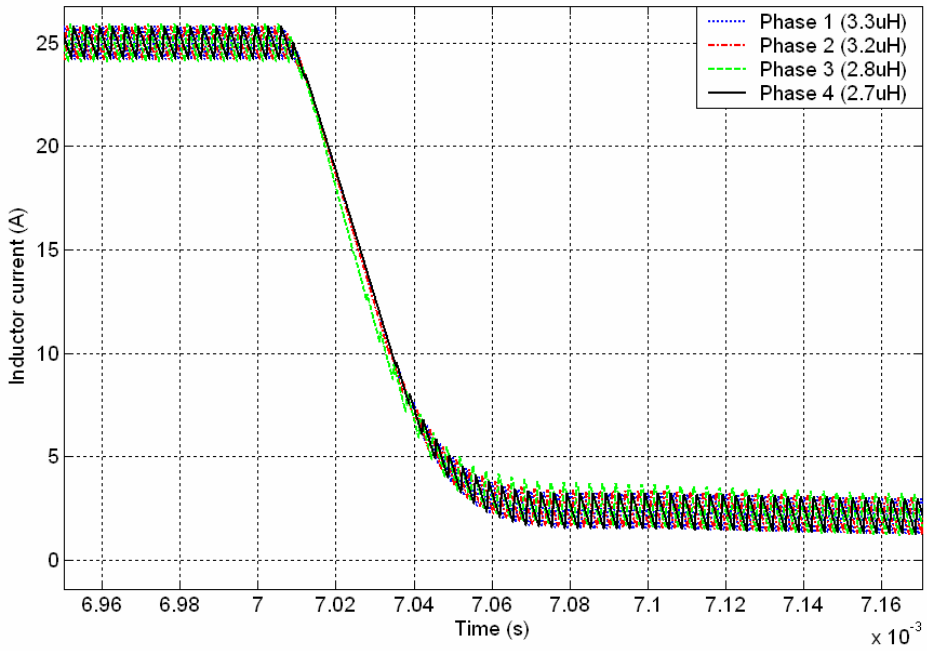

Fig. 3.17 Inductor current variation in each phase for a load decrease from 100 A to 10 A

3.2 Peak current mode control

3.2.1 Peak current mode control presentation

This control scheme (see Fig. 3.18) differs from the ACMC scheme on how the Pulse Width Modulation is carried out in its control logic [23], [62]-[63]. Instead of using an independent ramp signal to generate the duty cycle, the inductor current or more commonly the high side switch current is used to derive the logic signal with which the MOSFETs are driven. Thus, in this method of control, the turn on instant of the switch is clocked periodically; however, the switch is turned off only when the inductor current reaches the threshold value determined by the control signal.

This current control scheme offers the advantage of being faster than ACMC since the instantaneous inductor current rather than the average inductor current is controlled in the inner loop. Another candidate with instantaneous current control is the hysterisis current mode control. However, the PCMC scheme operates with a constant switching frequency which allows the various components in the converter to be optimally selected. Moreover, the control design also becomes simpler as compared to the ACMC scheme, since the design is only limited to the voltage controller. However, the PCMC method also suffers from certain drawbacks; these drawbacks and solutions for them are discussed below.

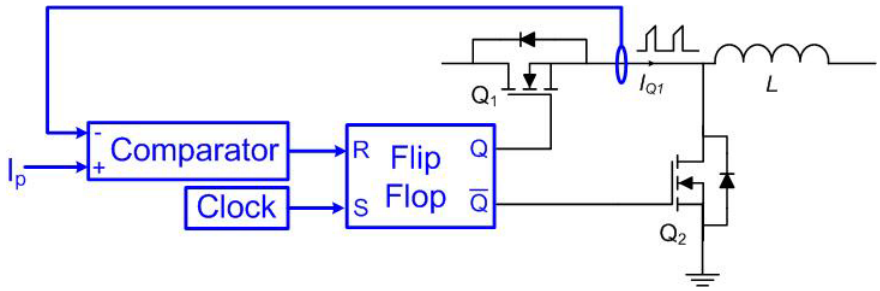

Fig. 3.18 PCMC logic scheme

Firstly, since the switch current is used directly to derive the MOSFET logic signal, the sensed current must be relatively noiseless and accurate. Hence, an instantaneous and accurate current sensor is needed to sense the switch current. The obtained sensed signal must be reasonably clean. Since this control scheme is applied in VRM, the efficiency and the size of the sensor has also to be taken into account. These problems relating to current sensing will form the focus of Chapters 4 and 5.

Secondly, in normal synchronous buck topologies, the high side switch current is usually affected significantly during switching [64]. Indeed, when using a MOSFET in place of the freewheeling diode, a dead time has to be provided during which both of the MOSFETs are in the off state. Throughout that period of time, the inductor current flows though the body diode of the lower MOSFET Q_2. Unfortunately, this diode is generally characterized by a large recovery time and current, which is in fact carried by the high side switch Q_1 during turn on. As a result, there is a peak in the leading edge of the input current, as can be seen in Fig. 3.19. This peak also increases with the current being carried. In PCMC, this perturbation may lead to instabilities, since this peak can be interpreted as the control threshold being hit, and thus Q_1 may be turned off prematurely.

To avoid this disturbance, a fast recovery diode or Schottky diode is placed in parallel with the synchronous MOSFET, as shown in Fig. 3.20 [64]. Indeed, in this case, during the dead time, the external diode will carry the inductor current, and its low recovery current will limit significantly the leading edge peak. Furthermore, in today's peak current mode controller IC, such as *UC3825*, a time period called *Leading Edge Blanking* (*LEB*) can be programmed, during which the control logic ignores the current waveform, and keeps Q_1 on [67]. Hence, by programming correctly the *LEB*, the control is not affected by the unwanted peak current.

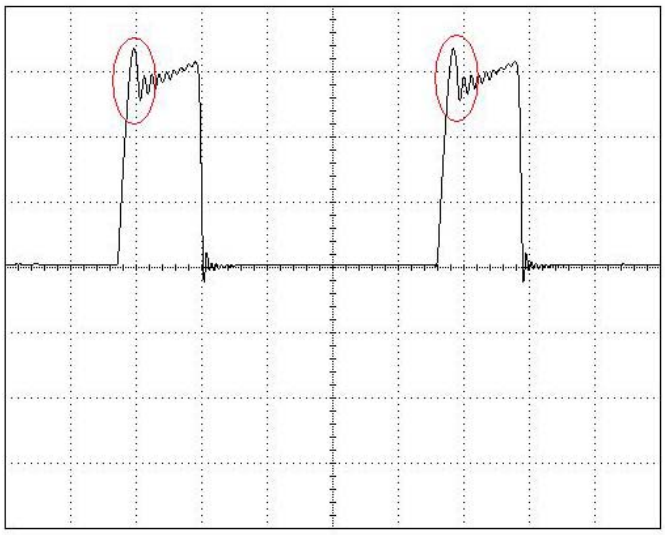

Fig. 3.19 Peak in the input current due to reverse recovery current of Q_2 5A/DIV, 1μs/DIV Experimental results from a synchronous converter carrying an average current of 15A. The current is sensed by the Yokogawa 700937 Hall Effect current sensor. The upper MOSFET is Harris Semiconductor's RFP70N03 [65] and the lower MOSFET is Infineon's SPP80N03S2L [66]

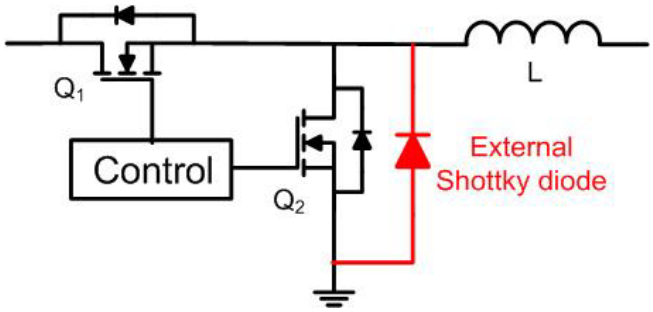

Fig. 3. 20 External Shottky diode placed in parallel with the synchronous MOSFET

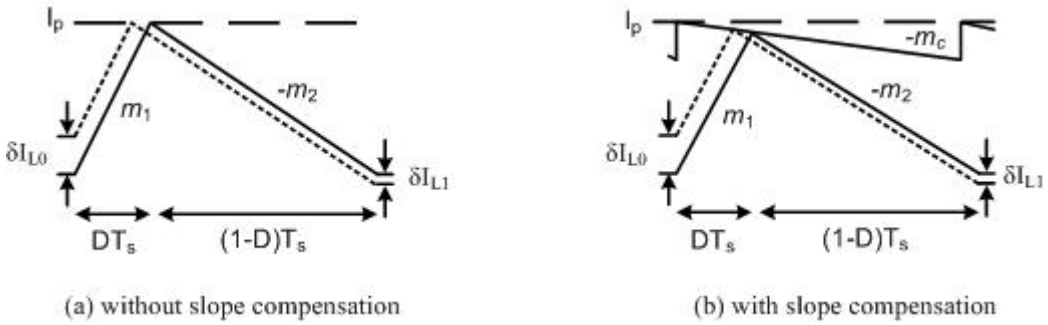

Fig. 3.21 Inductor current instability in PCMC

Finally, the PCMC is inherently unstable in open loop, when the duty ratio exceeds 50% [63], [68]-[69]. This open loop instability can be explained graphically using Fig. 3.21. The rising and falling slope of the inductor current are noted respectively as m_1 and m_2. If the inductor current is perturbed from its steady state value by a magnitude of δI_{L0} at the beginning of a particular cycle, from Fig. 3.21(a), the perturbation after one cycle will propagate to:

$$\left|\delta I_{L1}\right| = \frac{m_2}{m_1}\left|\delta I_{L0}\right| = \frac{D}{1-D}\left|\delta I_{L0}\right| \tag{3.28}$$

Hence, after n cycles, the error will become:

$$\left|\delta I_{Ln}\right| = \left(\frac{D}{1-D}\right)^n \left|\delta I_{L0}\right| \tag{3.29}$$

Thus, if D exceeds 0.5, the error exponentially increases in an open loop scheme and the system fails to revert to its steady state. This instability can be eliminated through a method called slope compensation. Here, a suitable periodic ramp with a falling slope of $-m_c$ is added to the control signal, as shown in Fig. 3.21(b). This is also equivalent to adding a ramp signal of slope $+m_c$ instead to the current waveform itself and comparing it to the control signal. In this case, the situation is similar to Fig. 3.21(a), except that the current signal rises now with a slope of m_1+m_c, and falls with a slope of m_2-m_c. Hence, an argument similar to that used previously can show that a perturbation δI_0 will propagate now after n cycles as:

$$\left|\delta I_n\right| = \left|\frac{m_2 - m_c}{m_1 + m_c}\right|^n \left|\delta I_0\right| \tag{3.30}$$

A suitable choice of the ramp slope $-m_c$ can thus cause the perturbation to die out under transient even when the duty cycle exceeds 0.5. However, when used in VRM applications, the duty cycle is close to only 15% during steady state, and may exceed 50% only during transient. Therefore, the slope compensation may not be truly needed for such an application.

In the following, the implementation of such a PCMC scheme in the multiphase converter and its control design are presented.

3.2.2 Implementation of the PCMC scheme in the multiphase converter

The overall PCMC scheme implemented on an n-phase interleaved converter is presented in Fig. 3.22.

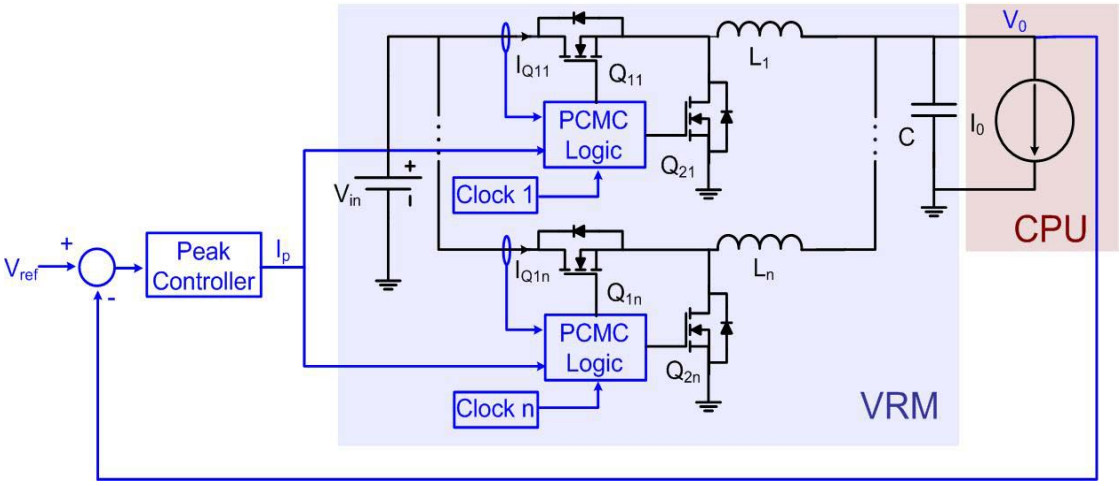

Fig. 3.22 Peak current mode control scheme in an n-phase buck converter

Here, according to the output voltage error, the peak controller fixes the peak current in each individual channel. The reference peak being the same, each phase therefore exhibits the same maximum inductor current. Besides, we assume the inductance to be nearly the same in each phase. Hence, equal current ripple occurs in each phase resulting in the average inductor currents also being identical. Therefore, the load is equally shared in the converter. The clock signals which turns on the Q_1 MOSFET of each channel are equally phase shifted, so that the inductor currents in each channel are evenly phase shifted too, as required in an interleaved converter. As a result, the total inductor current ripple is reduced and so is the output voltage ripple.

Since the steady state duty cycle is much less than 50% in the steady state, the slope compensation is usually not implemented. In the following, the control design process is detailed.

3.2.3 Control design

In the following, the transfer function v_0/i_p linking the variation of output voltage v_0 to the variation of controller output i_p is first estimated. Fig. 3.23 shows the typical inductor current waveform over one switching period T_s in the PCMC scheme. The resulting duty ratio is also indicated.

From this figure, the steady state peak reference I_p can be related to the steady state duty cycle D and the steady state average inductor current I_L as follows:

$$I_p = I_L + m_1 \frac{DT_s}{2} = I_L + \frac{V_{in} - V_0}{L} \frac{D}{2f_s}, \tag{3.31}$$

where T_s is the switching period, and f_s the switching frequency.

In a small signal model, (3.31) can be approximated by:

$$i_p = i_L + \frac{V_{in} - V_0}{2Lf_s} d - \frac{D}{2Lf_s} v_0, \tag{3.32}$$

where the lower case letters representing the variables stand for small variations around the steady state value.

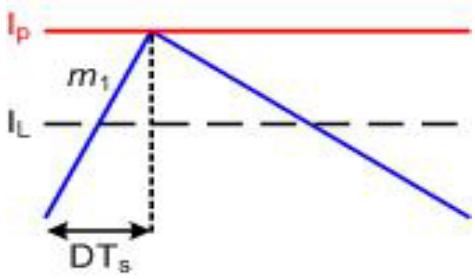

Fig. 3.23 Inductor current in a PCMC scheme

Furthermore, the large signal model derived in Section 3.1.2 and Section 3.1.3 is still valid if the current is equally shared among the phases. Hence, assuming a correct current sharing in the multiphase converter, the duty cycle variation *d*, and average inductor current variation i_L are given by:

$$d = \frac{LCs^2 + \left(R_{eq} + 4ESR\right)Cs + 4}{V_{in}Cs} i_L - \frac{4\left(1 + ESR.Cs\right)}{V_{in}Cs} i_0' \tag{3.33}$$

$$i_L = \frac{Cs}{4\left(1 + ESR.Cs\right)} v_0 + i_0', \tag{3.34}$$

where, $R_{eq} = DR_1 + \left(1 - D\right)R_2 + R_3$ and i_0' is the load current variation corresponding to each phase.

By combining (3.32), (3.33) and (3.34), we can obtain after simplification the output voltage transfer functions.

$$v_0 = G_{pp}\left(s\right) i_p + G_{pi}\left(s\right) i_0', \tag{3.35}$$

where G_{pp} and G_{pi} are given by

$$G_{pp}\left(s\right) = \frac{4\left(1 + ESRCs\right)}{\frac{V_{in} - V_0}{2V_{in}f_s}Cs^2 + Cs\left(1 - 2\frac{D}{Lf_s}ESR + \frac{V_{in} - V_0}{2LV_{in}f_s}\left(4ESR + R_{eq}\right)\right) + 2\frac{V_{in} - V_0}{LV_{in}f_s} - 2\frac{D}{Lf_s}} \tag{3.36}$$

$$G_{pi}\left(s\right) = -\left(1 + \frac{V_{in} - V_0}{2LV_{in}f_s}\left(Ls + R_{eq}\right)\right) G_{pp}\left(s\right) \tag{3.37}$$

The control design procedure presented in the following is based on the G_{pp} transfer function. Fig. 3.24 shows the Bode diagram of G_{pp} for an assumed inductance of 500 nH. It has also been noticed that for the range of inductance values studied in this thesis, the frequency response of G_{pp} has similar characteristics. Hence, though the following design methodology is presented for an inductance of 500 nH per phase, the same design procedure can be applied for other inductor values also.

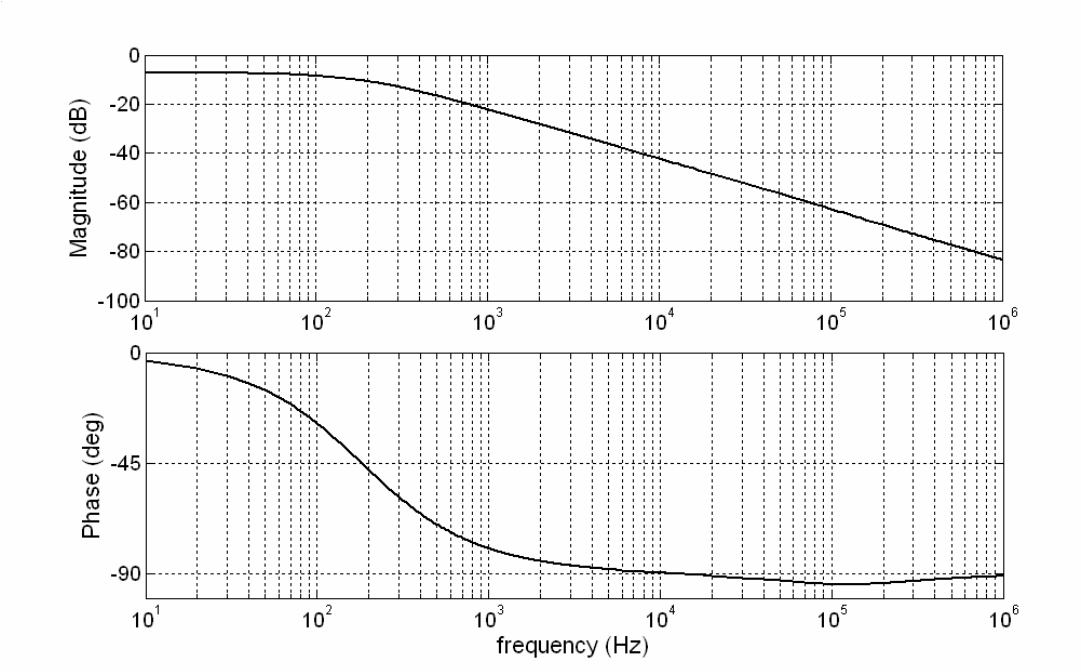

Fig. 3.24 v_0/i_p Bode diagram

As shown in Fig. 3.24, the G_{pp} transfer function has a low frequency pole close to 200 Hz, and a high frequency pole and zero around 120 kHz. Hence, overall, G_{pp} can be approximated as a first order system.

An integrator is added in the peak controller C_p in order to avoid any steady state error. Besides, an additional low frequency zero is introduced to compensate the low frequency pole. Finally, the DC gain of the controller is adjusted in order to have a bandwidth frequency fixed normally ten times less than the switching frequency for stability purposes. Thus, overall, the controller has the following form:

$$C_p = K_p \frac{\left(1+\frac{s}{\omega_{zp}}\right)}{s} \tag{3.38}$$

Hence, for an inductance of 500 nH per phase, K_p is fixed at 4.3×10^5 and ω_{zp} at 1123.6 rad/s to ensure a bandwidth of 30 kHz and a phase margin of 88º. Given the design methodology, the open loop transfer function may be approximated to ω_{bp}/s (ω_{bp} being the selected bandwidth in rad/s), as shown in Fig. 3.25.

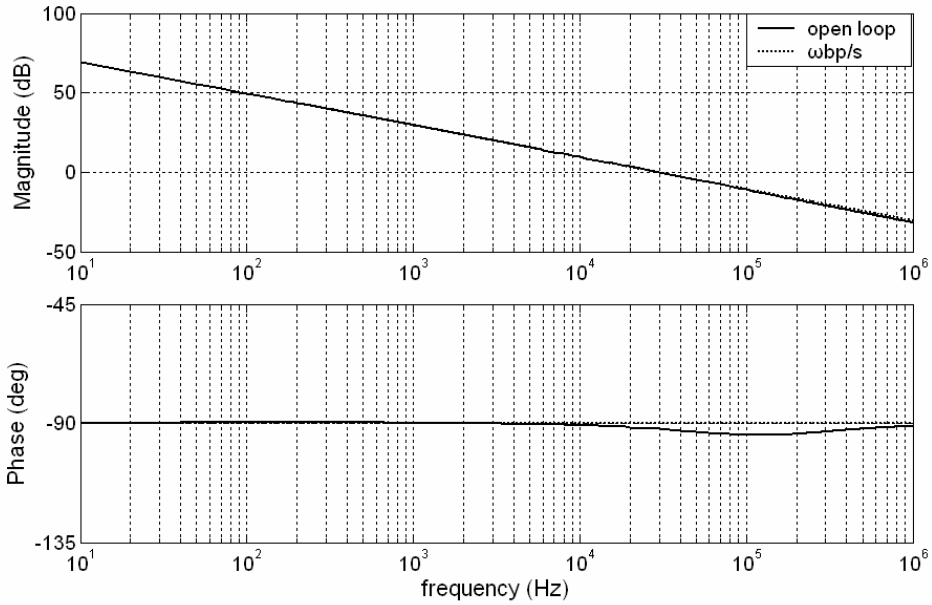

Fig. 3.25 Open loop compensated system for the PCMC and its approximation

Since G_{pp} depends on the inductance value, the controller has to be adjusted each time the inductor is changed, so as to keep the same open loop bandwidth and phase margin.

In the following sub-section, a critical inductance analysis is carried out for the PCMC scheme using the transfer functions estimated in (3.36) and (3.37).

3.2.4 Critical inductance

In the PCMC scheme, the output of the controller is not the duty ratio but the peak current reference. However, there can still be control saturation, if the converter is unable to reach the indicated peak current within one switching period. This indirectly causes the duty cycle to saturate. In such an event, the situation is similar to the VMC or the ACMC case when the duty ratio saturates. The voltage deviation and the settling time increases with the inductance value, when it is higher than the critical inductance value. In order to analyze this phenomenon, the transfer function of the output of the controller i_p over the load change i_0' is derived in this section using the G_{pp} and G_{pi} transfer functions found in the Section 3.2.3.

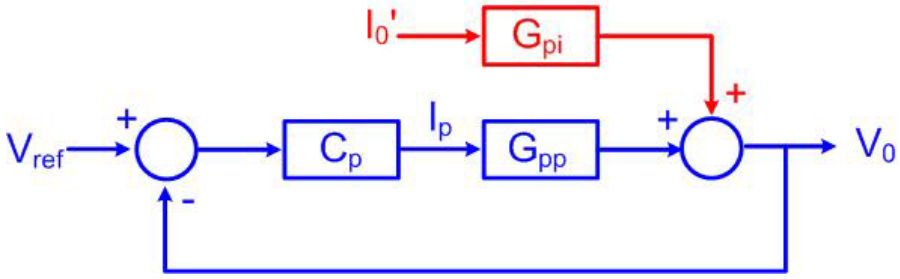

Fig. 3.26 PCMC simplified block diagram for the four phase converter

With identical phases, the simplified control block diagram presented in Fig. 3.26 can be considered for the four-phase converter, though the transfer functions G_{pp} and G_{pi} have been estimated with a small signal assumption. In the following, the validity of such a model for large load changes is examined. In Fig. 3.27 and Fig. 3.28, the output voltage variations given by the control diagram due to a maximum load change of 90 A, are compared to the output voltage fluctuation in the actual four-phase converter due to the same load change. Also, the controller output variations i_p, are compared in the same manner in Fig. 3.29 and Fig. 3.30. These comparisons are conducted for an inductance of 500 nH per phase, for which it has been noticed that there are no duty cycle saturations.

It is noticed from these figures, that the control diagram presented in Fig. 3.26 predicts accurately the average output voltage fluctuation in spite of large load disturbance. As shown in Fig. 3.29 and Fig. 3.30, the control output variation for large load disturbance can be accurately estimated using the same control diagram and the transfer function G_{pp} and G_{pi}. Hence, in the following, the transfer functions G_{pi} and G_{pp} will be used to estimate the transfer function of the controller output variation i_p over the load disturbance i_0, i_p/i_0. This transfer function will then be analyzed to predict the control saturation for a given load disturbance.

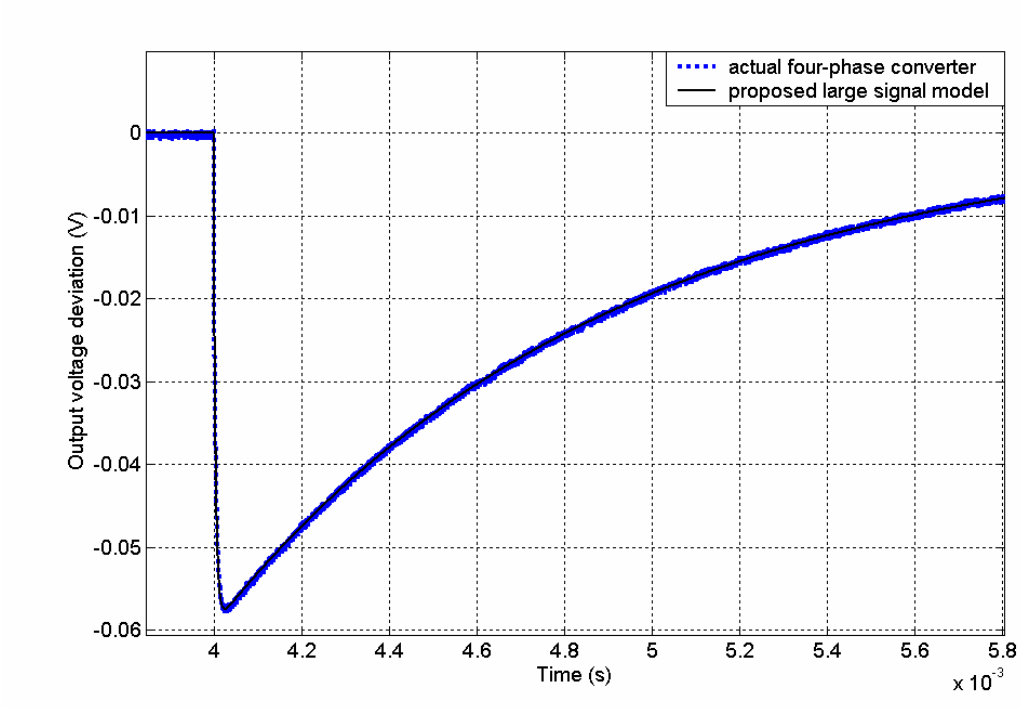

Fig. 3.27 Output voltage fluctuation comparison for a step change from 10 A to 100 A

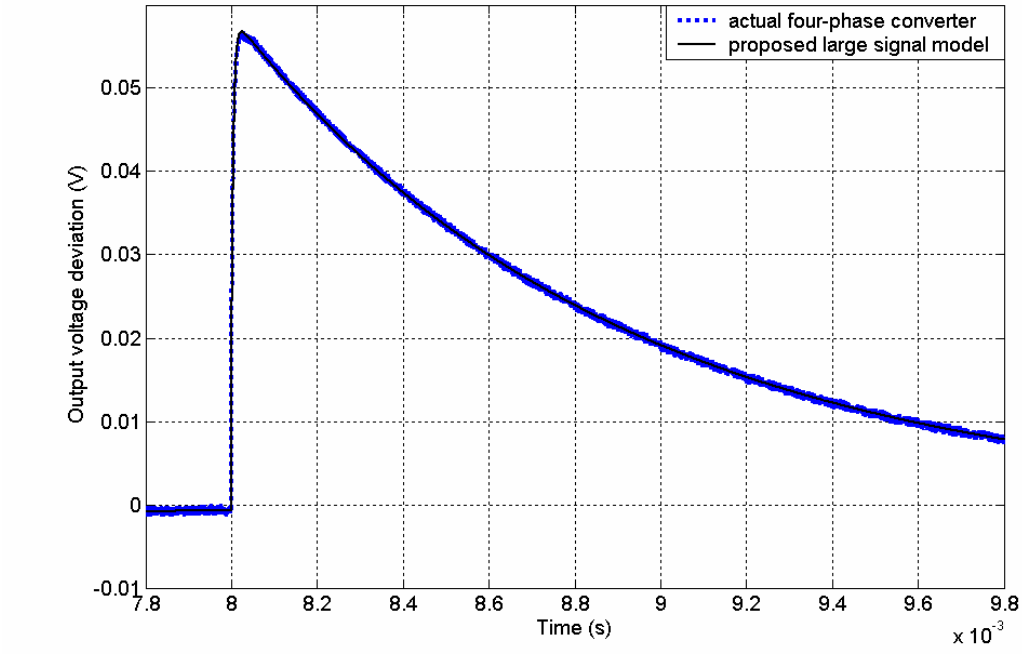

Fig. 3.28 Output voltage fluctuation comparison for a step change from 100 A to 10 A

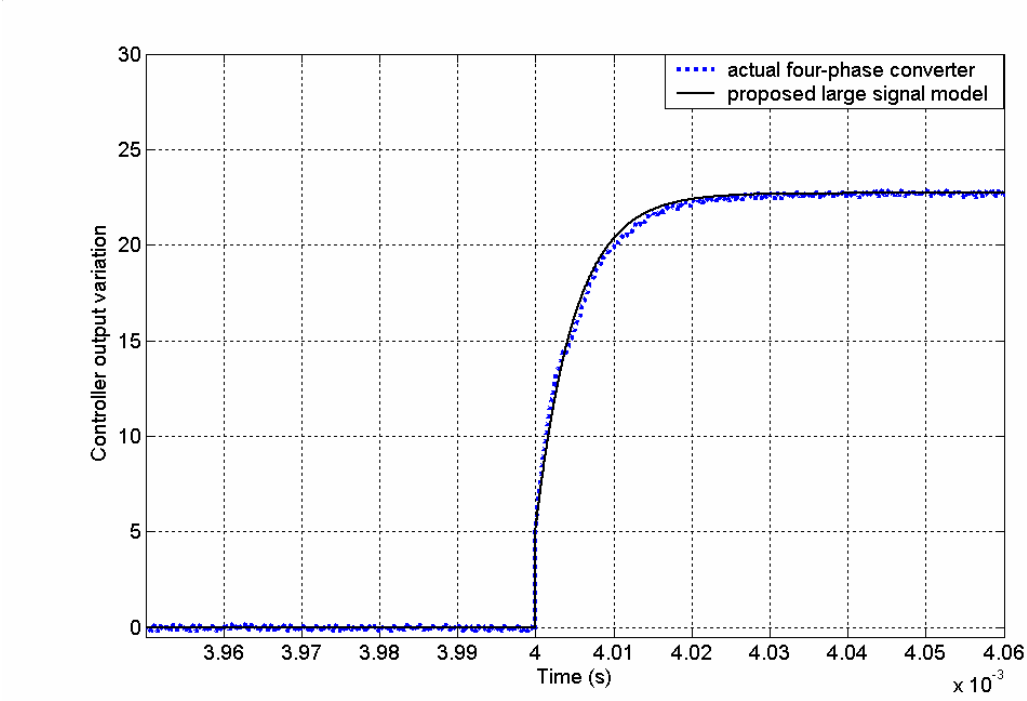

Fig. 3.29 Controller output variations comparison for a load step up from 10 A to 100 A.

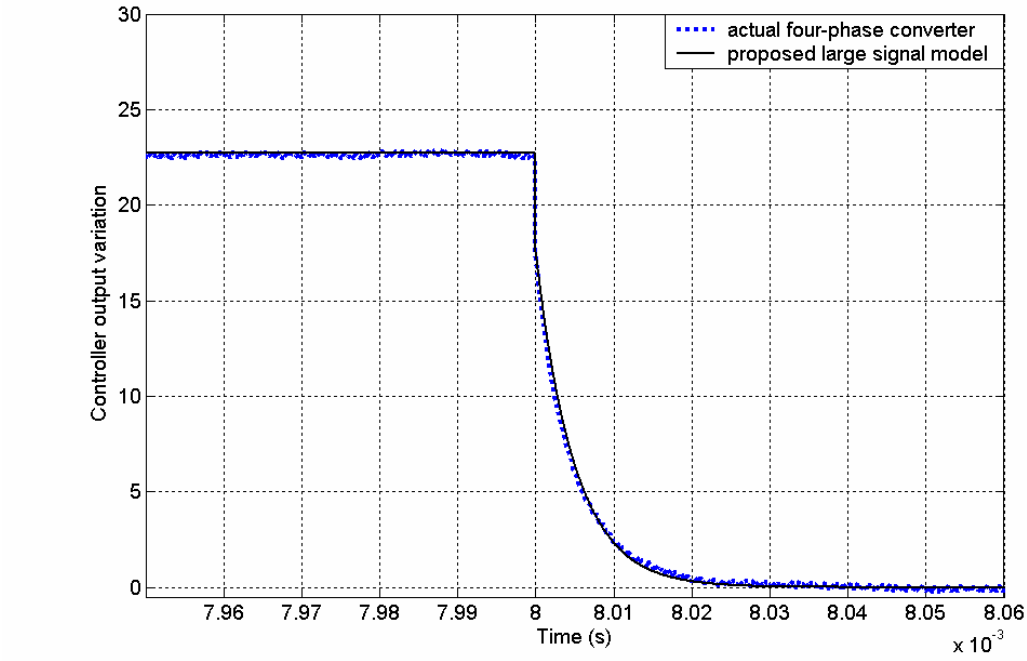

Fig. 3.30 Controller output variations comparison for a load step down from 100 A to 10 A.

From Fig. 3.26, for a constant reference voltage, the transfer function i_p/i_0' can directly be obtained as

$$i_p = -\frac{C_p.G_{pi}}{1+C_p.G_{pp}} i_0' = \left(1+\frac{V_{in}-V_0}{2LV_{in}} T_s\left(Ls+R_{eq}\right)\right)\frac{T_p}{1+T_p} i_0' \tag{3.38}$$

Again, given the chosen control design, the duty cycle to load current transfer function can be estimated using (3.38). In the employed control design methodology the open loop transfer function is found to be close to ω_{bp}/s. Equation (3.38) can therefore be approximated by:

$$i_p = \left(\left(1+\frac{V_{in}-V_0}{2LV_{in}} T_s R_{eq}\right)+\frac{V_{in}-V_0}{2V_{in}} T_s s\right)\frac{\omega_{bp}}{s+\omega_{bp}} i_0' \tag{3.39}$$

As a consequence, the Laplace transform of the controller's output variation, due to a load step change of magnitude $4.i_0'$, can be calculated as:

$$i_p(s) = \left(1+\frac{V_{in}-V_0}{2LV_{in}} T_s R_{eq}\right)\frac{\omega_{bp}}{\left(\omega_{bp}+s\right)s} i_0' + \frac{V_{in}-V_0}{2V_{in}} T_s.\frac{\omega_{bp}}{\left(\omega_{bp}+s\right)} i_0' \tag{3.40}$$

Hence, provided there is no duty cycle saturation, if the load changes by $4.i_0'$ in a step manner at time t=0, the peak current reference given by the controller will vary around its original value, as follows.

$$i_p(t) = i_0'\left(1+\frac{V_{in}-V_0}{2LV_{in}} T_s R_{eq}\right)\left(1-e^{-\omega_{bp}t}\right)+\frac{V_{in}-V_0}{2V_{in}} T_s i_0'.e^{-\omega_{bp}t} \tag{3.41}$$

For the range of inductance studied in this thesis, $\frac{V_{in}-V_0}{2LV_{in}} T_s R_{eq}$ is negligible compared to 1. Therefore, for a maximum load change of 90 A, the maximum variation of i_p, $\Delta i_{p\max}$ can be approximated independently of the inductance value as:

$$i_p(t) = i_0'\left(1-e^{-\omega_{bp}T_s}\right)+\frac{V_{in}-V_0}{2V_{in}} T_s i_0'.e^{-\omega_{bp}T_s} = 10.5 \text{ A} \tag{3.42}$$

However, during one switching period, the inductor current is allowed to rise only by a maximum of $(V_{in}\text{-}V_0)T_s/L$ or decrease by a maximum of $V_0.T_s/L$.. Therefore, since the inductor current falling slope is smaller than the current rising slope, the critical inductance, which can be defined as the largest inductance avoiding the control saturation for a given load change, can be approximated by:

$$L_c = \frac{V_0.T_s}{\Delta i_{p\max}} \tag{3.43}$$

The numerical value is found close to 570 nH.

In the following, the four phase converter is simulated with different inductance values in order to confirm this theoretical result. The current sharing is also analyzed when the inductance value in each channel differs within a small 10% margin.

3.2.5 PCMC simulation results

To verify the theoretically found critical inductance, the four phase converter is simulated for different inductance values from 100 nH to 1 μH as listed in Table 3.2. For each inductance value, the peak controller is adjusted as shown in Table 3.2, to keep the same open loop characteristics. The maximum output voltage fluctuations for a sudden load decrease from 100 A to 10 A were also measured during simulations and are listed in Table 3.2.

From this table, it is shown that, the voltage overshoot decreases with inductance and reaches a minimum when the inductance value is close to 570 nH. This is due to the control saturation occurring for inductance values higher than the critical inductance value. Indeed, in such cases, the converter is unable to reach the peak value indicated by the controller over one cycle causing a higher voltage overshoot than in the case when a smaller inductance is used, as shown in Fig. 3.33.

TABLE 3.2 PEAK CURRENT CONTROLLER CHARACTERISTICS AND OUTPUT VOLTAGE OVERSHOOT FOR A LOAD STEP DOWN OF 90A FOR DIFFERENT INDUCTANCE VALUES

L (nH)	1000	800	570	400	100
K_p ($\times 10^5$)	2.2	2.74	3.07	5.54	21.3
ω_{zp}(rad/s)	588	714	765	1449	5263
V_{max} (V)	1.870	1.859	1.857	1.857	1.858

These simulation results confirm also the critical inductance value found analytically in the previous section. The voltage overshoot starts increasing for inductance less than 570 nH due to higher voltage ripple. However, as shown in Fig. 3.31 and Fig. 3.32 the average output voltage waveform and the average total inductor current waveform remain the same. Also, as shown in these figures, for the range of inductances examined in this section, the control saturation affects only the transient response at the beginning. Consequently, the 20 mV settling time is not affected for inductances less than 1 μH.

The inductance per phase is therefore fixed at 570 nH.

Next, in order to investigate the sensitivity of the converter to slight parameter changes, in particular the load sharing capability in transient as well as in steady state, the inductor in each phase is chosen to differ slightly from 570 nH, within a 10 % margin. The inductor current waveforms for a load step down from 100 A to 10 A and vice versa are shown in Fig. 3.33 and Fig. 3.34 with the assumed inductor values.

The load is shown to be fairly shared among the channels both during transient and steady state. Hence, the PCMC scheme also ensures accurate current sharing though the inductance may differ from one phase to another. In the following section, the dynamic performance of the three modes of control studied in this thesis are compared.

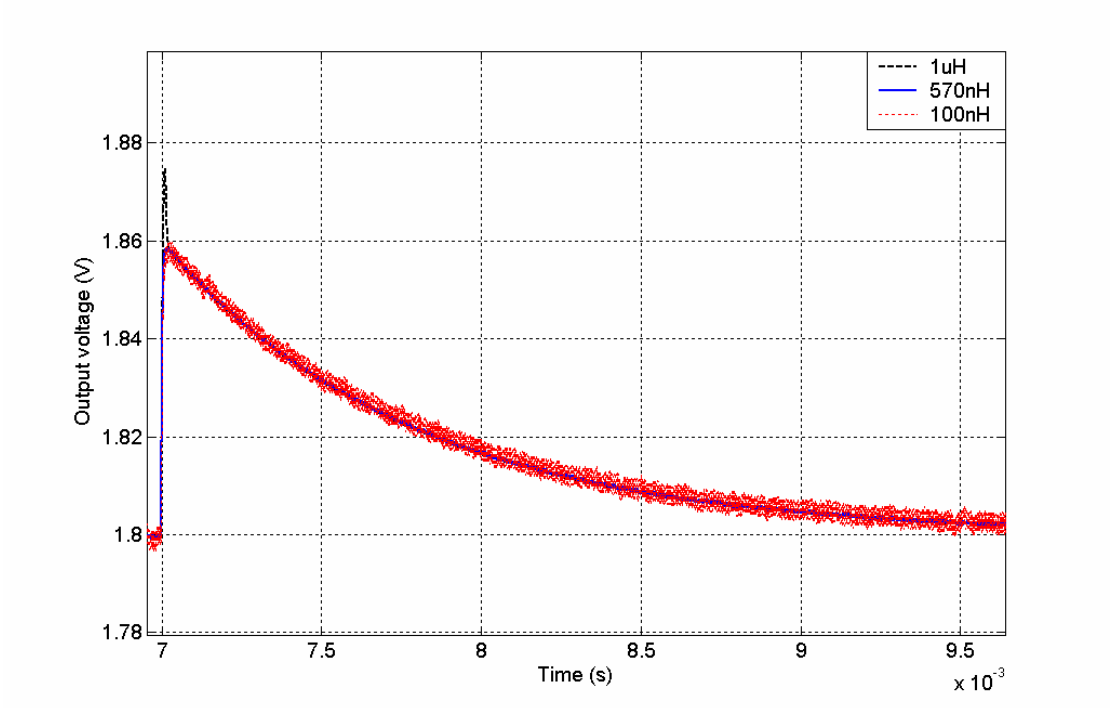

Fig. 3.31 Output voltage waveform during a load decrease from 100 A to 10 A in the four phase converter for three different inductance values per phase.

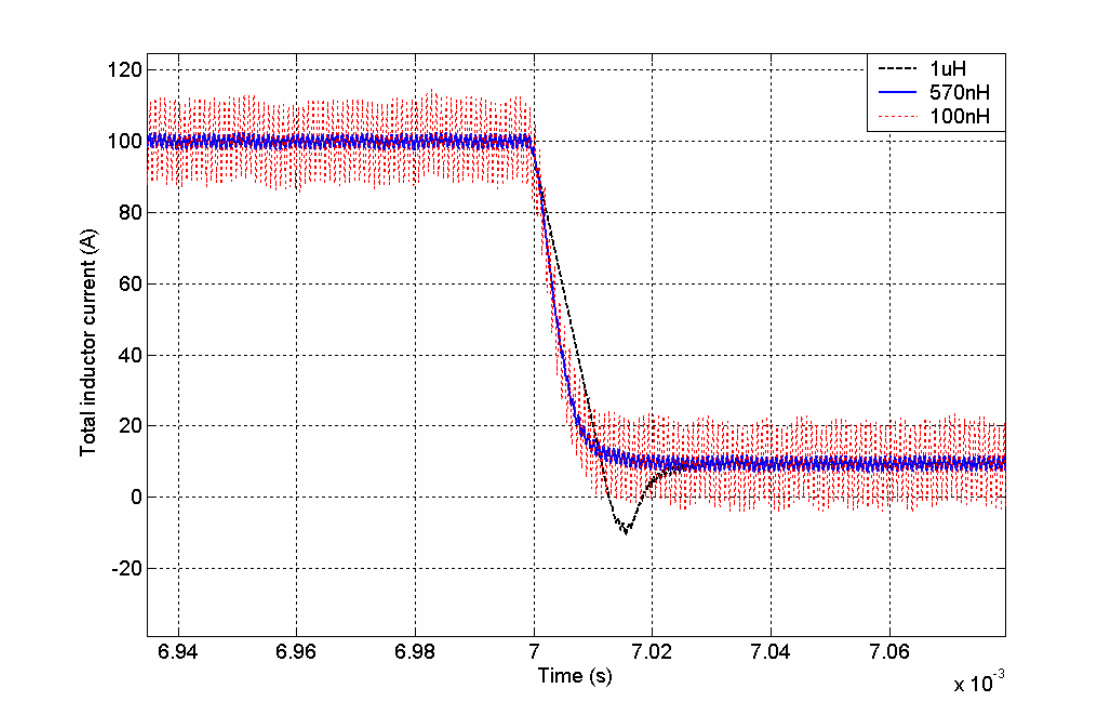

Fig. 3.32 Total inductor current waveforms for a load decrease from 100 A to 10 A in the four phase converter for three different inductance values per phase.

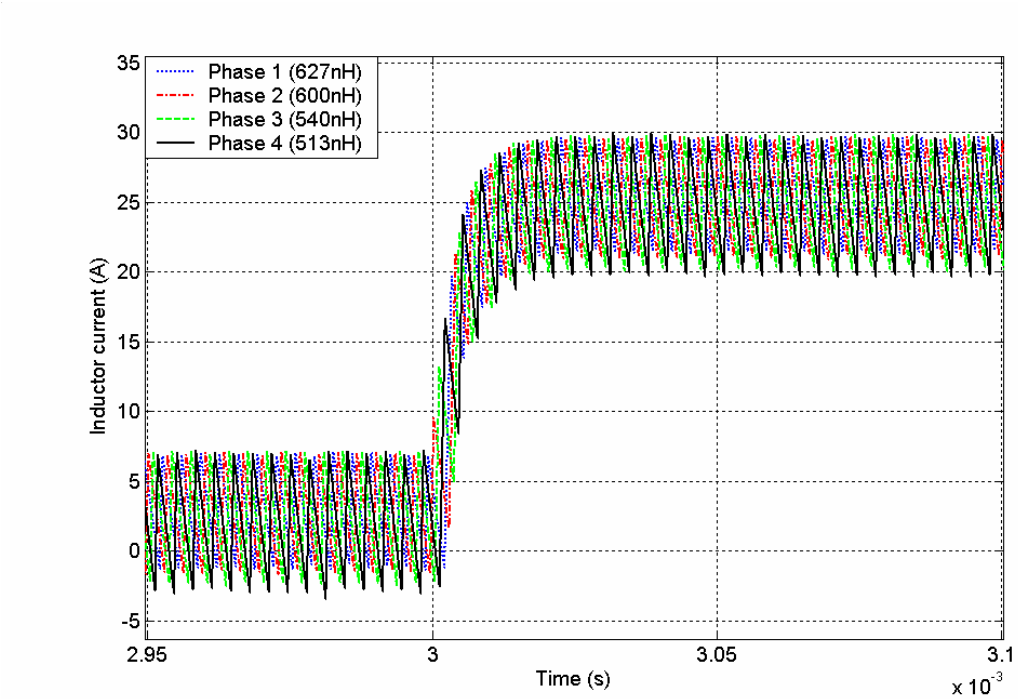

Fig. 3.33 Inductor current variation in each phase for a load increase from 10 A to 100 A

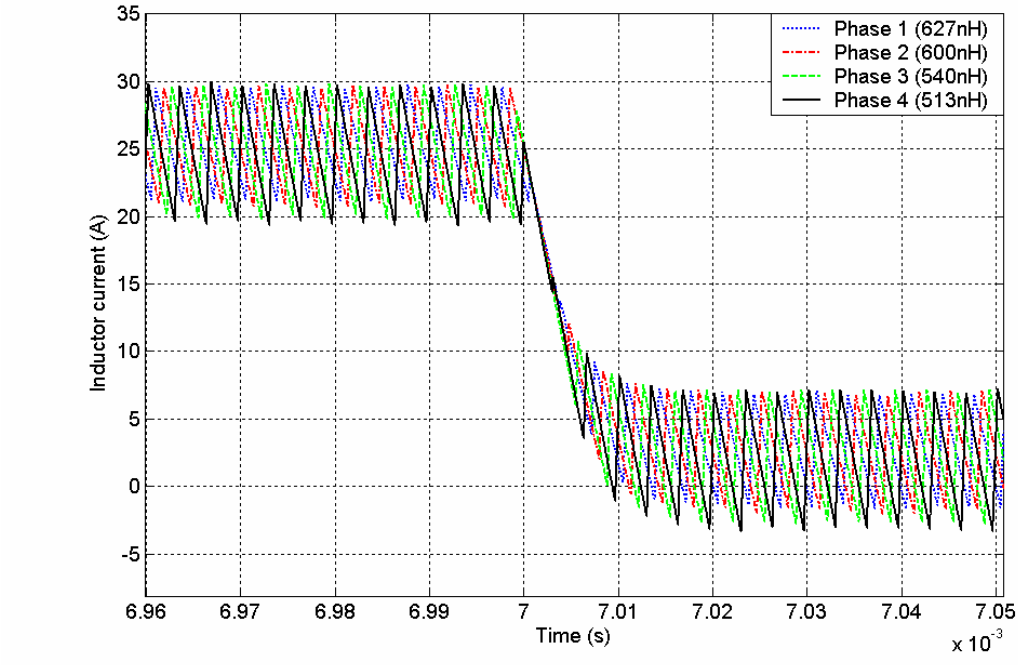

Fig. 3. 34 Inductor current variation in each phase for a load decrease from 100 A to 10 A

3.3 Comparison of the VMC, ACMC, PCMC schemes

In this thesis, three kinds of control have been investigated for the four-phase converter. For each type of control, the control design methodology has been presented, and a critical inductance analysis has been carried out. The four phase converter equipped with the critical inductance has then been simulated with the corresponding control scheme, and its dynamic and steady state performances for a given load disturbance have been looked into. These different characteristics are summarized and listed in the Table 3.3. The critical inductance and the various transient characteristics indicated in this table are valid for the case of a sudden load decrease from 100 A to 10 A.

It is shown from this table, that VMC scheme presents the best transient performance. However, its inability to ensure accurate current sharing is a serious drawback. ACMC scheme guarantees the average inductor current to be identical in each channel. But, this benefit comes with a cost in allowable bandwidth. Hence, in such a scheme, the dynamic performance of the converter suffers, and the output capacitor or the switching frequency has to be increased to fulfill the tight transient VRM requirements. Finally, the PCMC scheme achieves a performance which places it in between the other two schemes. An overall bandwidth of 30 kHz can be easily achieved, while ensuring an equal current sharing in the multiphase converter. Hence, this control scheme offers high transient and steady state performance, and is gaining popularity in present and future VRMs [45]. However, its main drawback lies in the difficulties faced in the practical implementation of the scheme. A relatively clean inductor or switch current waveform is needed to derive the logic signal, which usually comes with a cost in efficiency. This current sensing issue in buck derived topologies is investigated in the following chapters.

TABLE 3.3 FOUR-PHASE CONVERTER CHARACTERISTICS FOR THE THREE KINDS OF CONTROL METHODS.

	VMC	ACMC	PCMC
Bandwidth	120 kHz	6 kHz	30 kHz
Critical Inductance	30 nH	3 µH	570 nH
Steady state voltage ripple	3 mV	0.1 mV	0.5 mV
Maximum transient voltage deviation	1.815	2.06	1.86
20mV band settling time	10 µs	2.63ms	1.25ms
Current sharing capability	No	Yes	Yes

3.4 Conclusion

Design methods for average current mode control and peak current mode control for multiphase converter have been presented. For each system, a critical inductance has been identified and ways to estimate it have been explained in detail. It has also been shown that with both the current mode control methods, the load is shared equally in the multiphase converter among the phases under steady state, as well as under transient even when the inductance values differ slightly from each other. Besides, the PCMC offers the advantage of a higher bandwidth than the ACMC, thus, is capable of better fulfilling the CPU requirements.

Both the current control methods need the inductor current or the switch current to be sensed in each phase. This sensor has to be small and efficient. In addition, the current sensor used in the PCMC scheme has to have fast dynamic response with high bandwidth, besides being capable of accurately reproducing the current waveform.

In the next chapter, the existing current sensors used in today's VRM units are presented and discussed.

CHAPTER 4

CURRENT SENSING TECHNIQUES IN VRM

4.1 Introduction

As shown in Chapter 1, the current to be delivered to the CPU has significantly increased in the last few years, and the trend can be expected to continue. The multiphase topology fulfills the requirements of the latest CPUs, but its efficiency will be considerably reduced, should a current unbalance among the channels occur. Also, the channels must be overdesigned in order to accommodate the possible occurrence of such current unbalance. As a result, although the current mode control scheme has in general a lower bandwidth than the voltage mode control, it is being preferred for future VRMs, where the current sharing in steady state as well as during transient is an essential criterion.

In a current mode control scheme, the inner current loop requires information regarding the instantaneous current flowing through the inductor or the high side switch in each channel. Hence, a current sensor has to be added in each channel, whose accuracy will be a major contributor to the success or the failure of the design. The accuracy of the sensed signal is all the more important in a PCMC scheme, which offers a larger bandwidth than the ACMC scheme. Finally, the current sensor has to be small and efficient to match the stringent requirements of VRMs. These overall requirements in terms of size, efficiency, large bandwidth and accuracy present a great challenge for VRM designers.

It is indeed instructive to note that the voltage measurement is mostly a "passive" activity as it can be readily done at almost any place in the system without

affecting significantly the performance of the overall module. On the contrary, the integration of a current sensor in the system disturbs more severely the variable which we are trying to monitor. Various methods exist to minimize this disturbance, but they mostly come with a cost in accuracy or bandwidth, as will be shown in the following. As a result, they are generally not applicable in current mode control and are usually used only to prevent overload or other faults. In the following, existing current sensors used in multiphase converters are presented and their limitations highlighted.

4.2 Resistive sensing

Current sensing requires the development of a voltage signal corresponding to the current flowing at the particular place of interest in the circuit. A classical method to do it would be by simply adding in series a Current Sense Resistor (CSR) at the required location [70]-[71]. This approach is highly popular and is used in current mode control because of its simplicity, accuracy and relatively large bandwidth. However, this method has several limitations when implemented in the VRM, which are detailed in the following.

The main drawback lies in the resulting additional power loss. Indeed, in a multiphase converter, the current in each leg to be sensed can attain 30A. Since the output voltage to be delivered is small (less than 1V), the additional voltage drop across the sensing resistor can be relatively significant, and the loss in efficiency will be considerable, unless a very low CSR resistance is used. However, by decreasing this value, the voltage across the CSR becomes smaller in magnitude, which is harder to be sensed in a reasonably noiseless manner as required for current mode control. Hence, there exists a trade-off between efficiency and noise in signal output, when using CSR. Often, a noise filter is needed in such a case, which will affect the overall system bandwidth, besides rendering the method not applicable to PCMC.

Secondly, as with any material, the CSR undergoes a resistivity change with temperature [70]-[72]. Since the indicated resistance is valid only for a reference temperature, the sensed signal becomes less accurate under changes in the working temperature, which is likely to happen in the VRM where the current to be sensed has a large variation. To measure the resistance variation with temperature, the Temperature Coefficient of Resistance (TCR) is normally indicated by the manufacturer. TCR can be translated into resistance accuracy by the following formula [70]:

$$\Delta R(\%) = \left(T - T_{ref}\right).\frac{TCR}{10^6}.100, \tag{4.1}$$

where ΔR represents the variation in resistance in percentage, T and T_{ref} the operating temperature and the reference temperature indicated by the manufacturer, respectively.

To be used in a VRM, where a high precision sensor capable of functioning over a large range of operating temperature is needed, the TCR has to be as small as possible.

Finally, the self inductance of the CSR may be problematic, particularly when measuring varying currents with very large slopes such as the high side switch current [70]. Indeed, the CSR can be modeled as a resistance R_{CSR} in series with an inductance L_{CSR} (Fig. 4.1). Since the voltage across the L_{CSR} is also included in the sensed voltage, the output signal will exhibit voltage spikes when measuring current with high *di/dt* as shown in Fig. 4.2. Usually, this inductance is minimized by the manufacturer, and if necessary, a noise filter is used to remove these spikes.

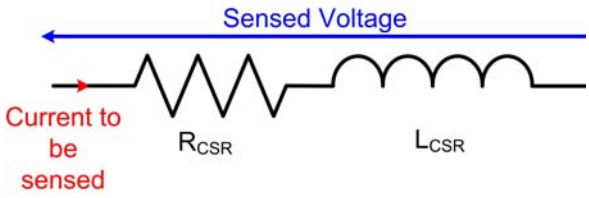

Fig. 4.1 CSR model with its self inductance

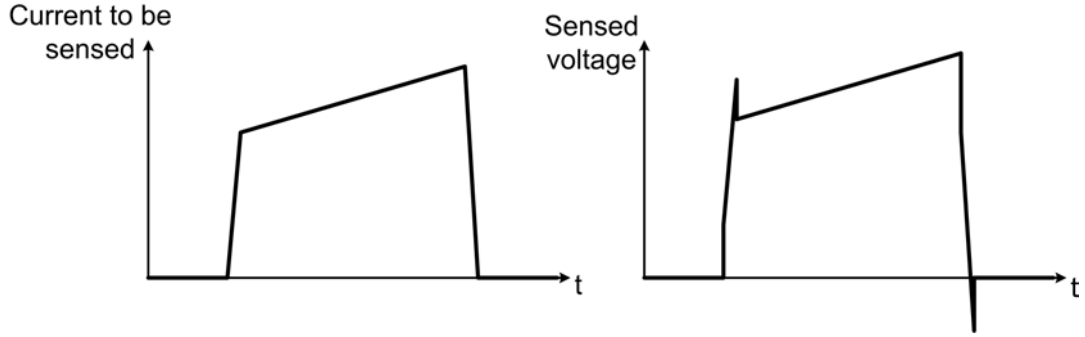

Fig. 4.2 Voltage spikes in the sensed signal due to the CSR self inductance

A lot of progress has been made in CSR technology, and manufacturers have drastically minimized these various drawbacks detailed previously. Materials such as manganin or constantan are being used in order to have a very low TCR (less than 30ppm/°C) [70]-[72], and CSRs are manufactured with "non-inductive" techniques to minimize the self inductance. With all these advances, the tolerance band of a CSR can be reduced up to 5% over the working temperature range [72]. Their size has also been considerably reduced, as they now come as Surface Mount Devices (SMD) and their inductance can go as low as 0.2nH [71]. Moreover, to avoid the voltage across the contact resistance with the PCB board to be also sensed, a four-point sensing method is often used [70]-[71]. Here, as shown in Fig. 4.3, the CSR soldering points are different from the sense leads. Therefore, we bypass the contact resistances, which do not have the same desired characteristics as the CSR.

However, even with a good design, there is still close to 5% loss in efficiency due to the CSR when used in today's VRM [72].

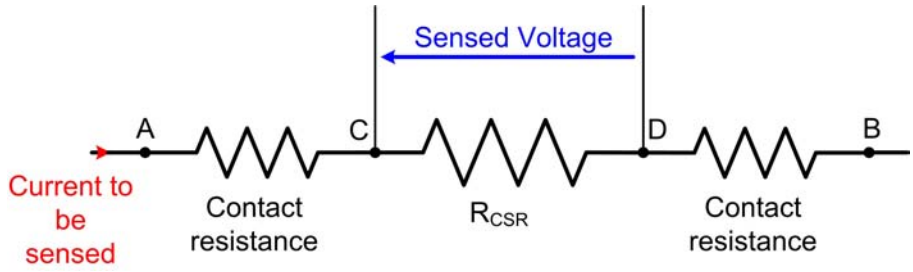

Fig. 4.3 Four point sensing technique
A and B are the point where the CSR is soldered, C and D where the voltage is sensed.

For a cost-effective solution, the PCB track may also be used as a CSR [72]. However, since the copper resistance is very small, a long track is needed so that the sensing resistance reaches a reasonable resistance value. As a result, the self inductance also increases. Furthermore, the copper's TCR is also an important consideration. The total error margin for the resistance value in this case can go as high as 20% [72]. Hence, although more costly, the rather classical CSR is usually preferred for current mode control.

4.3 R_{DS} sensing

MOSFETs when conducting can be fairly approximated as resistances. Thus, if the on-state resistance of the MOSFET, R_{DSon}, is known, the current being carried by the switch can be estimated by measuring the voltage across it. Hence, we can either measure the voltage across the high side switch Q_1 in order to have an indication of the high side switch current I_{Q1} alone, or measure the voltages across Q_1 and also the low side switch Q_2, and then add them together to obtain an estimation of the inductor current I_L [72]-[73]. This method can therefore be theoretically used for PCMC, as well as ACMC. However, although this measurement is cost effective since no additional components are required, it has some issues to be considered in its implementation.

Firstly, the voltage across the switch swings between two largely different values. For instance, the voltage across Q_1 is close to a high voltage of V_{in} during off state, and a very low voltage of $R_1.I_{Q1}$ during the on-state, where R_1 is the drain-source resistance of Q_1. Besides, only one of these values contains the desired information ($R_1.I_{Q1}$ here). Hence, to ignore the measurement when the switch is not conducting and also at the same time avoid saturation of any amplifier placed in the control IC, the controller must include some kind of blanking during the MOSFET off state [72].

Secondly, during turn on and turn off, there will be some voltage ringing due to stray inductances and capacitances. During the process of turn on, the MOSFET drain-source voltage drop will not be proportional to the drain current. Thus, to ignore these measurements as well, the blanking time should be extended partly into the on time [72].

The main issue that prevents this scheme from being used in high performance current controllers is the variation of R_{DSon} with temperature, current and applied gate voltage. For the low voltage MOSFET used in VRMs, this resistance can be estimated as [74]:

$$R_{DSon} = \frac{L_a}{W_a.\mu.C_{ox}.\left(V_{GS} - V_T\right)}, \tag{4.2}$$

where L_a and W_a are the length and the width of the active region, μ the mobility of majority carriers, C_{ox} the oxide capacitance per unit area, V_T the threshold voltage, and V_{GS} the applied gate to source voltage.

Though on-state resistance is unique to each MOSFET as per the expression in (4.2), the value given in the datasheet comes usually with an error margin of 10%. The mobility μ is also highly dependent on the temperature. Thus, R_{DSon} varies

significantly with temperature and with device. Since the MOSFET gets heated according to the current being carried, the resistance depends on the switch current.

The variation of the resistance with the temperature and the drain current for a typical low voltage high current MOSFET are presented in Fig. 4.4 and Fig. 4.5. In a normal MOSFET, the total variation in R_{DSon} can become as high as 50 to 100% when used in VRMs [73]. Therefore, this method of current sensing is not suitable for current mode control. However, it is widely used for overload or fault protection, where a high precision current estimation is not generally needed.

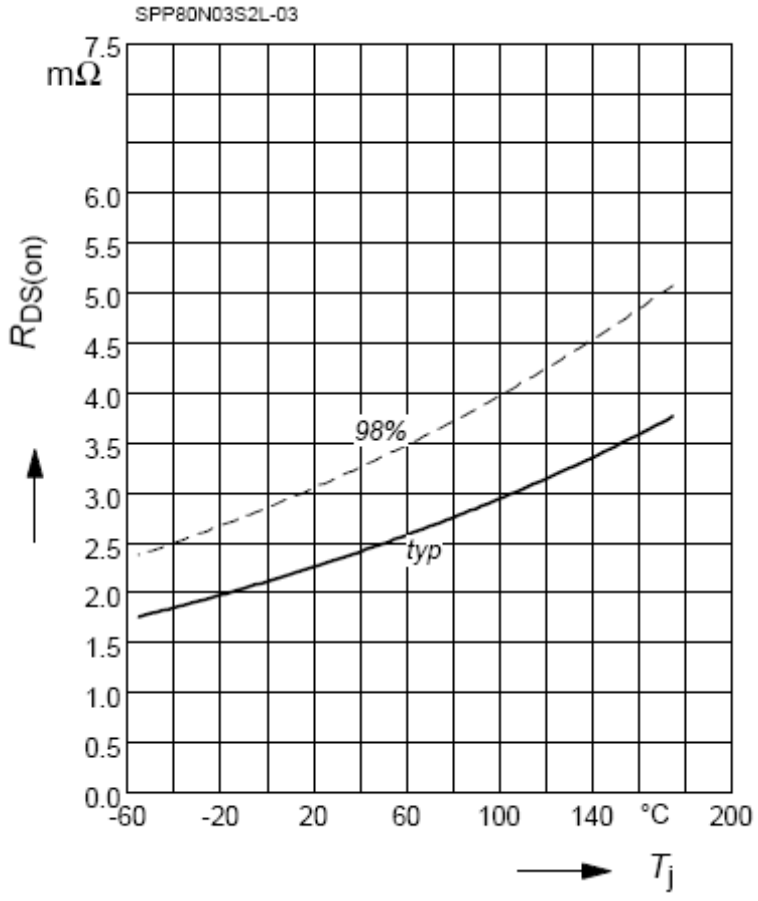

Fig. 4.4 On-state resistance variation according to the temperature for a constant drain current of 80A and a gate source voltage of 10V for SPP80N03S2L-03 Infineon MOSFET. The bold line is the typical characteristic, and the dashed curve represents the experimental limit for 98% of the commercialized MOSFET of this type [66].

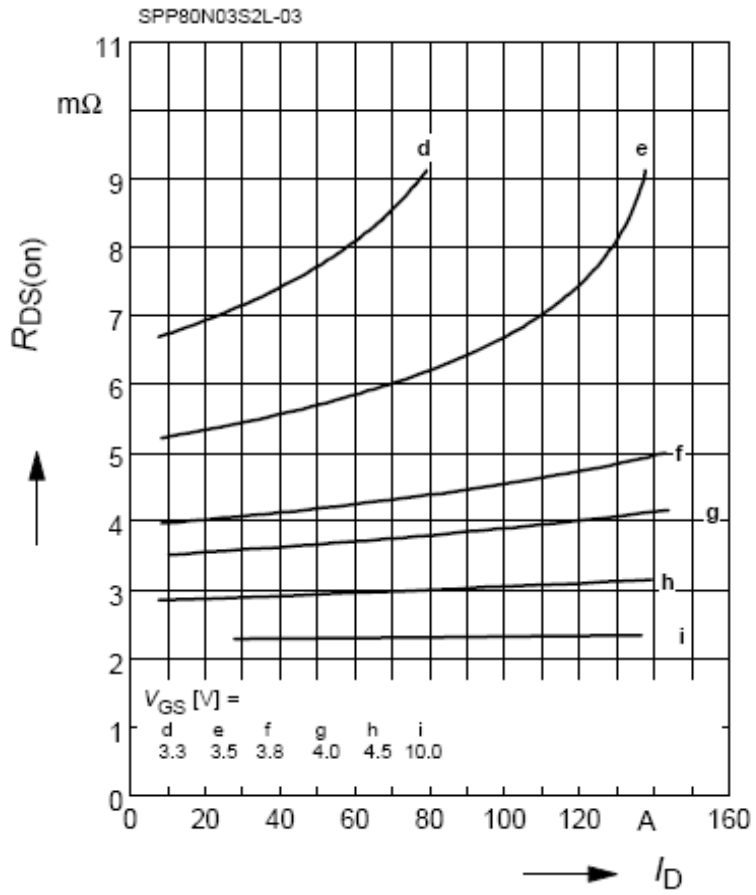

Fig. 4.5 Drain source resistance variation according to the drain current for a given gate source voltage, for SPP80N03S2L-03 Infineon MOSFET [66]

Some of today's MOSFETs come with an internal current sensor, called SENSEFET. In such a power MOSFET, an additional current sensing FET is built in parallel and its measuring capability is used for sensing the current. Although it is proven to be more accurate, this method is not yet popular in current mode control, because of its low bandwidth (typically 1MHz) [73]. Such a low bandwidth will result in inaccurate reproduction of the current waveform.

4.4 Sensing the inductor voltage

Since the inductor voltage varies according to the current being carried, different ways to deduce the current information from the voltage waveform have been suggested. Indeed, the voltage V_L across the inductor consists mainly of the sum of two parts; the first one due to the inductance L, the other one due to the inductor's series resistance, R_L:

$$V_L = L\frac{dI_L}{dt} + R_L.I_L \tag{4.3}$$

A first approach would be to measure the average inductor current $<I_L>$ by adding a low pass filter, as shown in Fig. 4.6 [72]. In fact, the inductor voltage's AC component is due to the current ripple through the resistance R_L and the induced voltage $L.di_L/dt$, whereas the DC component is only the product of the average current $<I_L>$ and the resistance R_L. Hence, the DC value can be obtained using a low pass filter. Thus, the inductor current can be estimated, provided the R_L value is known. This method can theoretically be used only for ACMC.

However, the exact knowledge of the inductor series resistance is needed in this case, which is, in particular, subject to variation with temperature. Besides, to achieve a proper filtering of AC ripple, particularly in today's high current ripple VRMs (due to the low inductance value needed), the bandwidth of the low pass filter has to be fixed very low, which as a result reduces greatly the dynamic performance of the converter [72]. Consequently, this method is not used in current mode control.

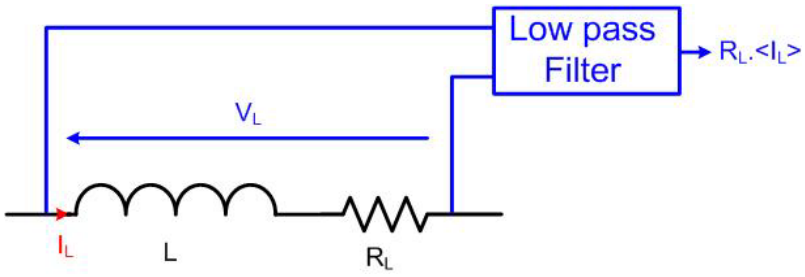

Fig. 4.6 Inductor current sensing using a low pass filter

A second approach consists of placing a resistance R_f followed by a capacitor C_f in parallel with the inductor, as shown in Fig. 4.7 [73], [75]. If R_f and C_f are properly designed, then the voltage across the capacitor, V_{Cf} can be used as a current estimator. R_f has also to be sufficiently large, so that only a small amount of current compared to I_L, flows through it.

Thus, the total voltage across the inductor is:

$$V_L = L\frac{dI_L}{dt} + R_L I_L = R_L\left(\frac{L}{R_L}.\frac{dI_L}{dt} + I_L\right) \tag{4.4}$$

However, from Fig. 4.8, the inductor voltage can be shown to be:

$$V_L = R_f.C_f\frac{dV_{Cf}}{dt} + V_{Cf} \tag{4.5}$$

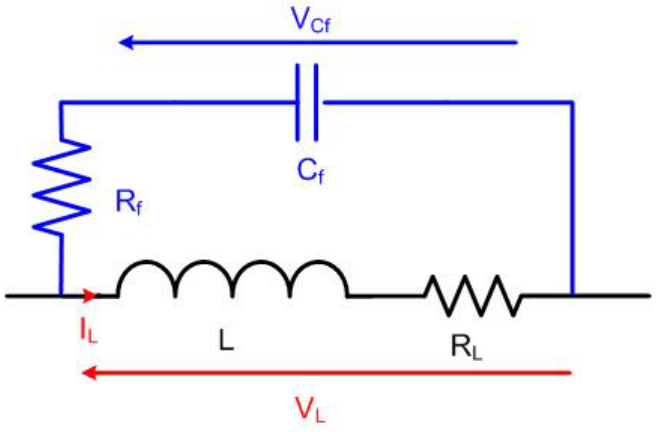

Fig. 4.7 Inductor current sensing using resistance and capacitor across the inductor

Hence, by accurately matching $R_f.C_f$ and L/R_L, the capacitor voltage V_{Cf} varies in the same manner as the inductor current I_L. However, V_{Cf} will be directly proportional to I_L only if they both have identical initial conditions. If these conditions are ensured, the capacitor voltage can be used in principle as an estimator of the inductor current. However, in practice, small disturbances in the capacitor voltage or the inductor current will lead to steady state error over a period of time between the estimated current and the actual current. Hence, such a current sensing technique will not work over time unless there is a resetting of the capacitor voltage corresponding to the inductor current during operation. Besides, the exact values of L and R_L must be known, not to mention their variations with temperature. Therefore, although highly efficient, this method is not widely used in current mode control and is still under investigation [76].

4.5 RC network across Q_2

Fig. 4.8 presents yet another current sensor scheme for a buck-derived converter topology [77]. The current sensor is here implemented by a low pass filter connected across the low side MOSFET, Q_2. Under steady-state, the voltage V_{Cf2} across the capacitor will be equal to the average voltage across Q_2. If the parasitic resistance R_L of the inductance is known, the average inductor current can then be estimated by using the relation

$$I_L = \frac{V_{Cf2} - V_0}{R_L}, \tag{4.6}$$

where V_0 is the sensed output voltage.

Although this method is simple, it requires again accurate knowledge of the inductor's series resistance, R_L, which, as noted earlier, is sensitive to temperature. Besides, the estimation is valid only for the average current; consequently it cannot be

used in a PCMC scheme. Also, the sensing itself has its own dynamics dependent on the R_{f2} and C_{f2} values, which are generally selected to filter the switching component of the voltage across the low side switch Q_2. This will, in turn affect the overall bandwidth and performance, as in the first approach presented in Section 4.3.

It may be noted that instead of estimating the inductor current using (4.6), the voltage signal V_{Cf2} itself can be used as the feedback variable as in [77]. Indeed, as the output voltage V_0, and the average voltage across Q_2 are usually very close, the computation of (4.6) will lead to significant rounding error. Hence, as in a multiphase converter, the output voltage is the same in each channel, instead of calculating I_L as (4.6), V_{Cf2} itself is directly used as a feedback variable in each channel. However, in this case, while the average V_{Cf2} will be accurately controlled by the inner V_{Cf2} loop of the control system, the inductor current will not be, due to the sensing errors involved. Hence, this scheme is again not suitable for current mode control.

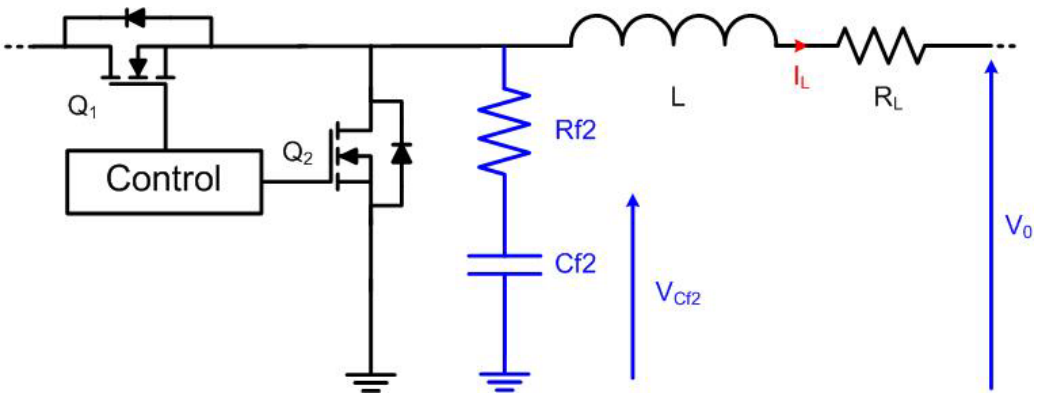

Fig. 4. 8 Current sensor using RC network across Q_2

4.6 Conclusion

In a current mode control scheme, current measurements are the key for the success or the failure of the design. The principal current sensors used in VRMs have been overviewed in this chapter. Their main advantages and disadvantages are summarized in Table 4.1.

Existing current sensors can be divided into two categories. In the first category, the current is actually measured via a resistance (CSR method and MOSFET R_{DSon} sensing method). The instantaneous current is thus measured, and the performance of the sensor depends only on the sensor's characteristics. In the second category such as in the inductor voltage and Q_2 voltage sensing methods, the sensor scheme performs rather as an observer, and the exact knowledge of several circuit component values is needed. Hence, they are less accurate and highly sensitive to parameter variations in the circuit. Besides, they are mostly limited to the average current measurement. As a result, these methods are still under investigation or used in a VMC scheme only for over-load current protection.

Other current sensing methods, such as Hall Effect sensors or Current Transformers (CT) based techniques are also available though they are not being used in VRM applications. Among them, the Hall Effect sensor, though accurate, is complex, bulky, and expensive and hence may not be applicable for our application. Some CT based techniques also exist for current sensing. The problems that these techniques suffer from in a VRM application will be discussed in Chapter 5.

Hence, although resistive sensing leads to a drop in efficiency, the majority of today's commercialized current controllers for VRM use it because of its performance and accuracy. In the following chapter, a novel CT based current sensor, which is as accurate as the resistive sensing but more efficient, will be presented.

TABLE 4.1 COMPARATIVE OVERVIEW OF VRM CURRENT SENSING TECHNIQUES

Technique	Advantage	Disadvantage
CSR(accurate resistance)	-Good accuracy -Instantaneous current sensing	-High power dissipation
CSR(PCB track)	-Reduced loss -Instantaneous current sensing	-Low accuracy
R_{DSon}	-No additional loss -Instantaneous current sensing	-Low accuracy
SENSEFET	-Lossless -Instantaneous current sensing	-Special MOSFETs -Low bandwidth
Inductor voltage-low pass filter	-Lossless	-Low accuracy -Sensitivity to R_L variation -Average current sensing only
RC observer across the inductor	-Lossless (Negilgible loss) -Instantaneous current sensing	-Low accuracy -Sensitivity to L and R_L variations
RC network across the synchronous MOSFET	-Lossless (Negligible loss)	-Low accuracy -Average current sensing only -Sensitivity to R_L variation

CHAPTER 5

NOVEL CURRENT TRANSFORMER BASED CURRENT SENSOR

5.0 Introduction

As seen earlier in Chapter 3, current control provides a solution to the current sharing issue in the multiphase converter. However, for implementing the current control, small, efficient, and accurate current sensors with large bandwidth are needed, especially for the PCMC scheme where a relatively clean waveform is needed.

In the last chapter, a brief overview of existing current sensing methods in DC-DC buck converter has been provided, and their limitations highlighted. It has been shown that among the currently available methods, the resistive sensing approach is the only one currently capable of fulfilling the task and thus, is commonly preferred in current mode control, in spite of a decrease in overall efficiency of at least 5%. Indeed, most of the other more efficient ways of current sensing come with a cost in accuracy and/or bandwidth. As a result, they are used only for certain applications, such as overload protection. In this chapter, a novel current sensing technique, which can be used in current mode control including PCMC, is proposed and investigated.

The proposed sensor is based on the use of current transformers, and aims to recover the DC component which is normally filtered by such a transformer. It thus aims to combine the accuracy of the resistive sensing and the efficiency of current transformers.

In the following, the basic operation of current transformer will be first explained, and a scheme to build DC current transformers using AC current

transformers for switching power supplies will be briefly discussed. The proposed method for DC recovery is then explained in detail. Design issues and trade-off are also discussed. Finally, experimental results on a step-down buck converter, controlled in peak current mode using such a sensor, are provided to confirm its performance. The proposed technique can also be applied to several other types of power converters besides the multiphase buck converter.

5.1 Current Transformer (CT)

In power systems, current transformers are widely preferred to sense the current for control purposes. They offer several advantages compared to other types of current sensors. Firstly, they provide electrical isolation between control and power. They also have a relatively large bandwidth depending on the winding characteristics, and with the availability of today's materials can go up to several MHz without significant power loss [70]. Moreover, by using a higher number of turns on the secondary side, the current can be first stepped down before being sensed. Therefore, for the same resistance (used as CT burden) the conductive power loss will be significantly lower. Furthermore, this lower power dissipation allows a much higher signal level, which inherently improves the signal to noise ratio in the sensed signal. Usually toroid shaped current transformers are preferred, as this shape minimizes the leakage inductance. Current transformers do have some limitations, the most significant among them being their inability to sense DC current.

To investigate this aspect, let us first consider the current transformer presented in Fig. 5.1. The current source I_1 on the primary side represents the current to be sensed. On the secondary side a burden resistance R_B is placed, through which a current I_2 is flowing. The voltage V_2 across it constitutes the sensed signal.

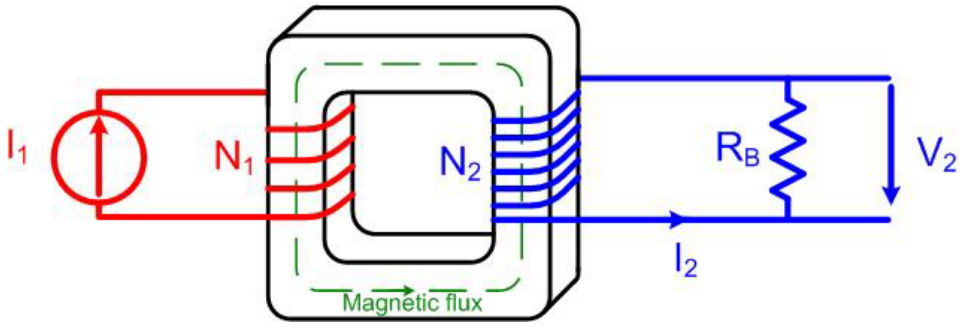

Fig. 5.1 Current transformer

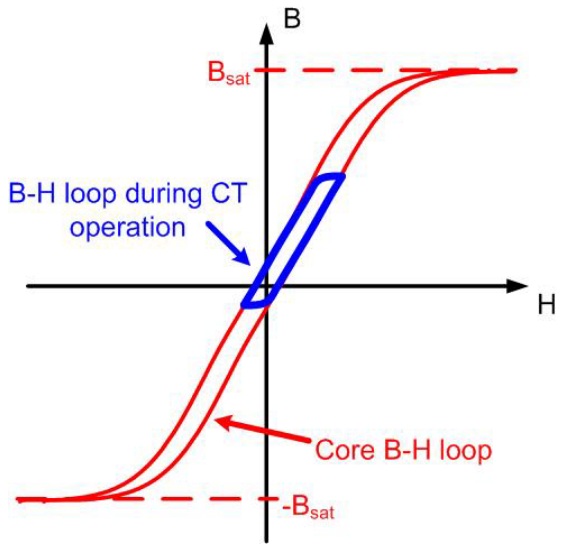

Fig. 5.2 B-H characteristics of a typical magnetic core material

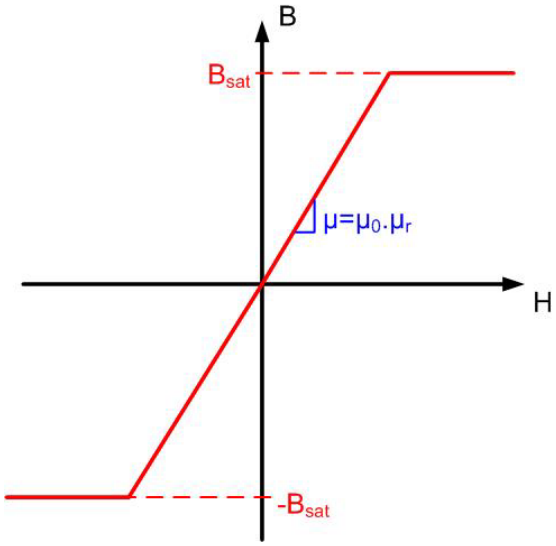

Fig. 5.3 Approximation of the B-H characteristics of a typical magnetic core material by neglecting the hysteresis

Usually, the current transformer core is chosen to be small, and the wire carrying the current to be sensed, simply goes through the toroid's hole. However, here, for generality, N_1 number of turns in the primary, and N_2 number of turns in the secondary are considered. Various leakage fluxes and also winding capacitors are neglected in this model.

Furthermore, in the core, the relation between the flux density B, and the magnetic field H, is determined by the core material characteristics. Fig. 5.2 presents a typical B-H curve of a ferrite magnetic material [28]. As shown in bold line, the B-H relation is non linear even when operation away from the saturation region is considered. However, for purpose of analysis, the core material characteristic of Fig. 5.2 will be modeled in this thesis by the piecewise-linear characteristics of Fig. 5.3. Such an approximation is commonly performed in the literature to model magnetic components, such as inductors and transformers [28]. The validity of the design will be validated later using experimental results.

Following this, the full characteristics linking the current transformer's voltage and current variables can be derived using Ampere's law and Faraday's law.

According to Ampere's law, in Fig. 5.1,

$$N_1.I_1 - N_2.I_2 = H.l, \tag{5.1}$$

where l is the mean magnetic path length.

Furthermore, we assume the transformer to be working in the linear region where the flux density B is proportional to the magnetic field H (see Fig. 5.3)

Thus, the total flux φ is given as:

$$\varphi = B.A = \mu_0.\mu_r.A.H, \tag{5.2}$$

where μ_0 is the permeability of the vacuum, μ_r the relative permeability of the core material, and A the cross sectional area of the core.

Hence, the following equation can be obtained

$$N_1.I_1 - N_2.I_2 = \frac{\varphi.l}{\mu_0.\mu_r.A} = \varphi.R_e, \tag{5.3}$$

where R_e is the reluctance of the magnetic circuit.

The expression $\varphi.R_e/N_2$ represents actually the magnetizing current I_m on the secondary side.

However, according to Faraday's law, the voltage V_2 across the secondary side resistor R_B is given by:

$$V_2 = R_B.I_2 = N_2 \frac{d\varphi}{dt} \tag{5.4}$$

Therefore, by combining (5.3) and (5.4), a differential equation relating I_1 and I_2 can be obtained:

$$N_1 \frac{dI_1}{dt} = N_2 \frac{dI_2}{dt} + \frac{R_e.R_B}{N_2} I_2 \tag{5.5}$$

By transforming (5.5) into the Laplace domain, the overall transfer function of the current transformer, relating the secondary current I_2 to the primary current I_1 can be estimated as:

$$\frac{I_2}{I_1} = \frac{N_1.s}{N_2.s + R_e.\frac{R_B}{N_2}} = \frac{N_1}{N_2}\left(1 - \frac{1}{1 + \frac{N_2^2}{R_e.R_B}s}\right) \tag{5.6}$$

This transfer function consists of two parts: a proportional part equal to the turns ratio, N_1/N_2, and a low pass filter part with a corner frequency at:

$$f_c = \frac{R_B.R_e}{2\pi.N_2^2} \tag{5.7}$$

Hence, from (5.6), any current flowing in the primary, whose frequency is much less than f_c including DC, will be filtered and will not appear in the secondary. However, for a frequency much greater than f_c, there will be a secondary current directly proportional to the primary current. In most cases, the current transformer is designed so that the corner frequency is very low and only the DC value will be filtered off in the sensing of the current. Therefore, this model explains how the current transformer is basically only an AC current sensor, and thus cannot be used to sense directly the inductor current in multiphase converter.

This inability to sense DC current has so far prevented its use in buck and buck derived converter topologies. Yet, some methods based on current transformers exist to overcome this difficulty, particularly when sensing the switching current in power converters. However, in our investigation, these methods are found to be unsuitable for use in VRM. In the following, one such method will be presented, and its limitations highlighted.

The method consists of placing a diode in the secondary, in order to avoid negative current, as shown in Fig. 5.4 [70]. Therefore, it appears that the DC filtering cannot take place in the current transformer. Although the idea seems simple, the mode of operation is complex, as explained in the following. For this purpose, the transformer is modeled as an ideal transformer with a magnetizing inductance in the secondary side. The resulting equivalent circuit, as shown in Fig. 5.5, is analyzed when a switching current flows in the primary side. The reason for the inclusion the winding capacitor in the model will become clearer during the following discussion.

The secondary magnetizing inductance L_m can be directly estimated as:

$$L_m = \frac{\mu_0 \mu_r A}{l} N_2^2 \tag{5.8}$$

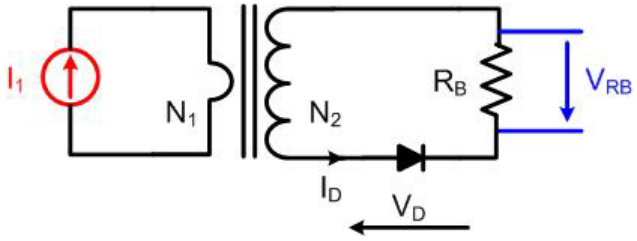

Fig. 5.4 Switch current sensing technique using current transformer and a diode.

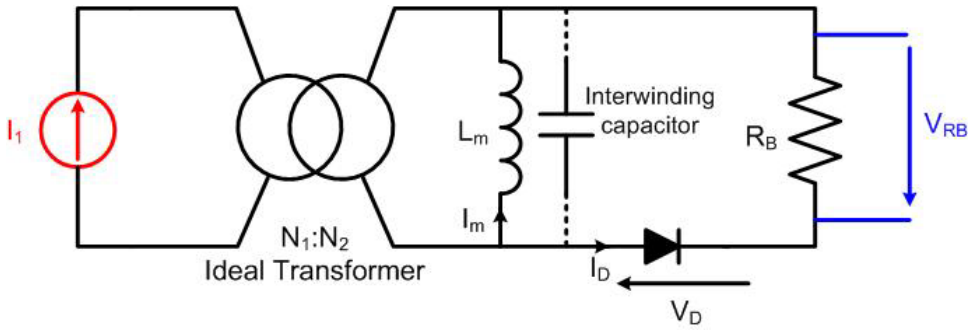

Fig. 5.5 A simple model for the CT-diode current sensing technique

The magnetizing current I_m, as well as the primary current I_1 and the diode current I_D, are assumed to be initially zero. The primary current, which actually represents the switch current, rises then in a step manner. The induced voltage due to the sudden current rise forward biases the diode.

Since $N_1.I_1 = N_2\left(I_D + I_m\right)$, (5.9)

at the start, I_D is directly proportional to the switch current I_1. However, at the same time, I_m starts also rising up due to the positive voltage drops across the diode and across the resistance:

$$L_m \frac{dI_m}{dt} = V_D + R_B.I_D, \tag{5.10}$$

where V_D represents the voltage drop across the diode.

Thus, according to (5.10) part of the primary current is used to build up the magnetizing current, which is not being sensed. Consequently, I_m contributes to the sensing error. The diode is usually forward biased throughout the on time of the main

switch, and thus I_m keeps increasing during this period - the diode will become reverse biased only when I_m equals I_D in magnitude.

The primary current then stops abruptly due to device turn-off. Consequently, the diode becomes reverse biased, and the current stops flowing through the burden resistance. However, a path should be ensured for the built up magnetizing current to flow. Otherwise, an over-voltage will indeed occur, which will either destroy the diode or disturb significantly the primary current. In the circuit, the current I_m flows actually through the secondary interwinding capacitor, represented in Fig. 5.3 in dashed line.

In fact, during this off interval, the operation is even more complicated. In fact, part of the current will also be carried by the diode as reverse recovery current and leakage current. Besides, the interwinding capacitor is very small (less than 100pF), and the magnetizing current will oscillate with the capacitor voltage. If the off interval is long enough, the capacitor voltage may also forward bias the diode, and the current will then flow through the burden resistance. These currents will also contribute to the error in the sensed signal. Finally, this type of sensor is unable to sense negative current, which occur in a synchronous buck converter with very light load.

Apart from these accuracy issues, this CT-based method also affects significantly the normal operation of the converter. Firstly, when the main switch is conducting, the secondary voltage will be larger due to the additional voltage drop in the diode. This causes the power loss in the CT to be larger; besides the primary side voltage during on state will be higher. Secondly, the switching characteristics are heavily affected due to the magnetizing inductance. During on state, the diode is forward biased, and the reflected impedance on the primary side is usually negligible. However, when the switch is off, the diode is reverse biased, and the reflected

impedance consist primarily of the magnetizing inductance, which is usually of the order of several μH. This is not negligible, considering that the output inductances in usual VRMs are mostly less than 1 μH. Consequently, the MOSFET turn on will be slowed down, and the efficiency of the converter diminished.

Hence, in our opinion, this method is not suitable for use in VRMs. In the following, the proposed CT-based current sensing method will be introduced. Here, the use of the diode will be avoided, and a rather classical current transformer will be used.

5.2 Proposed current sensing method

In this section, the proposed current sensing method is first introduced and its operation explained. The proposed current sensing method is also based on the use of current transformers. However, the secondary side circuit is now only limited to the burden resistance. This method actually rebuilds the lost DC component from the sensed signal.

Let us first consider one channel in the multiphase converter as shown in Fig. 5.6. In this figure, CT_1 is a current transformer measuring the current I_{Q1} through the high side switch. A small and accurate current sensing resistor of value R_{B1} is connected across the secondary of CT_1 and the voltage V_{2Q1} across this resistor is sensed. Assuming the switching frequency f_s to be much higher than the current transformer corner frequency, f_c, as expressed in (5.7), only the DC component will get filtered off in the secondary, and the AC part will pass fully without much alteration. Therefore, the sensed signal will have an offset compared to the original waveform.

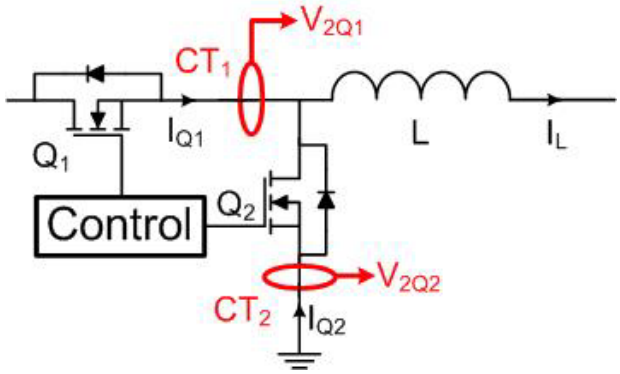

Fig. 5.6 One channel of the multiphase converter with current transformers CT_1 and CT_2

Next we shall see how the original current in Q_1 can be accurately obtained by canceling the DC offset.

The current sensor waveforms corresponding to CT_1 are shown in Fig. 5.7. Fig. 5.7(b) shows the ideal waveform of the high-side switch current while Fig. 5.7(c) shows that of V_{2Q1}, which will be equal to the secondary current multiplied by the value of resistor R_{B1}. It may be noted that the primary side DC component of current has been filtered off in the secondary side voltage. However, we have not lost any information in the process. We know that once Q_1 is turned off, the primary current is zero. Hence, the secondary voltage signal can be simply moved up, such that it is equal to zero during the switch off interval. Thus, a signal proportional to the switch current can be directly obtained. In this manner, the DC value of the signal is restored.

One way to do so is to sample the value of V_{2Q1} during Q_1 off interval in each cycle, hold that value, and then deduct it from V_{2Q1} waveform itself. We use a high bandwidth sample and hold IC for this purpose. The switch control signal of Q_1 (Fig. 5.7(a)), which is zero during the interval that V_{2Q1} has to be sampled and constant when V_{2Q1} has to be held, can be conveniently used to control the sample and hold IC. The output of the sample and hold (-A in Fig. 5.7(d)) is then subtracted from V_{2Q1} waveform to finally obtain a signal proportional to the high side current I_{Q1}.

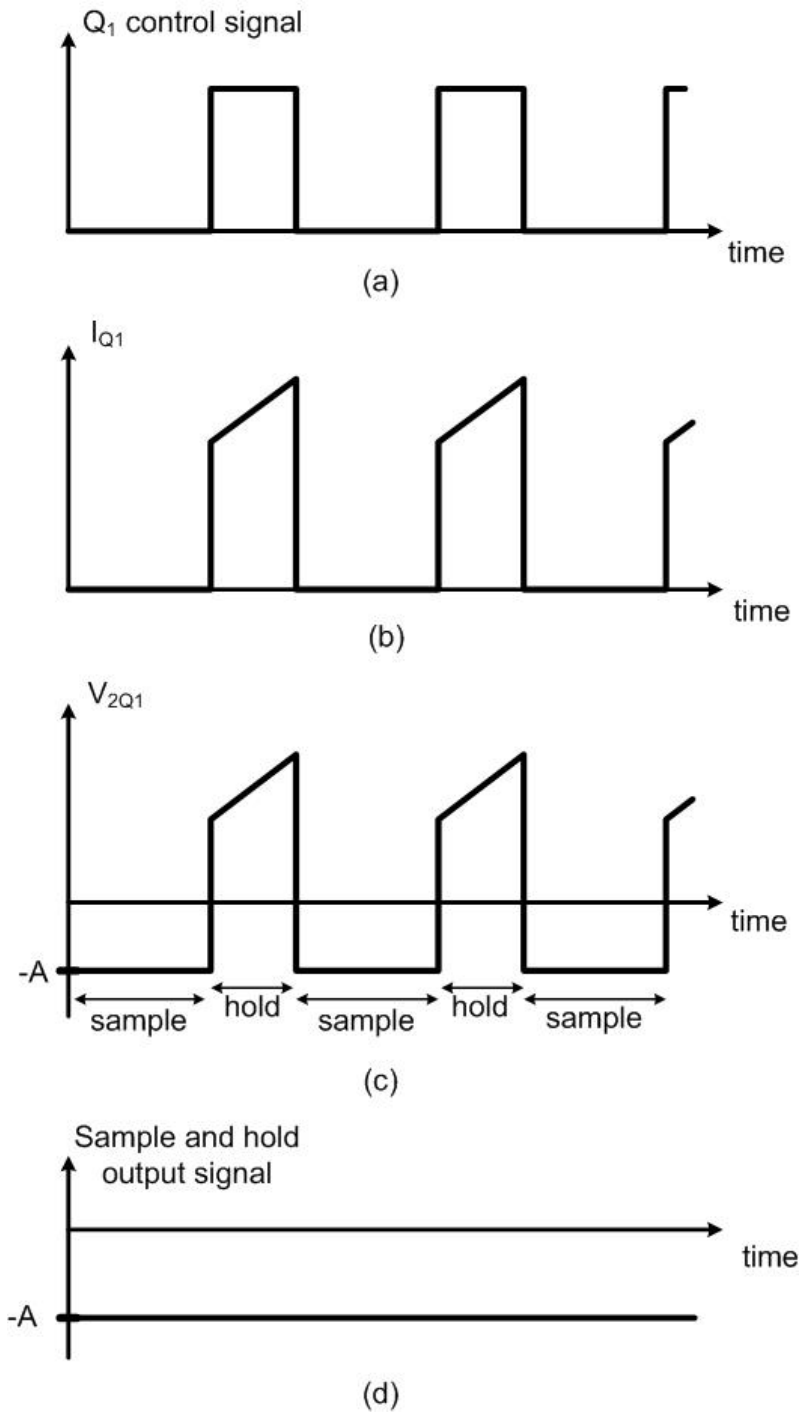

Fig. 5.7 Waveforms corresponding to sensing of high side switch (Q_1) current

The Q_1 current signal reconstructed in this manner is adequate for use in the PCMC method. Should we however need the complete inductor current waveform for the average current mode control scheme for instance, we can in fact reconstruct the same. We know that the inductor current is of a triangular shape with a DC offset. Information regarding the maximum and the minimum value of the current is already contained in the high side switch signal itself (see Fig. 5.8).

Hence, as shown in Fig. 5.8, one method of obtaining the overall inductor current signal waveform is by using a suitable analog circuit to connect the maximum and the minimum points during the on-interval of the Q_1 current signal obtained earlier. This method, though using only one current transformer, is tough to implement due to the difficulties in accurately determining the minimum and maximum points during the on-interval of the Q_1 current signal.

A simpler way to obtain the inductor current signal is by adding another current transformer CT_2 in series with the low side switch Q_2. We estimate the current I_{Q2} through the switch Q_2 in the same manner as we did for Q_1. Then, by adding together the reconstructed signals from both the current transformers (after proper scaling), we obtain the full inductor current signal, which can be directly used in average current mode control. The implementation of such an inductor current sensing scheme is straight forward and is shown in Fig. 5.9.

Due to the different characteristics of the currents flowing in the high side switch and in the low side switch, the number of turns and the burden resistance may not be the same for both the current transformers. In Fig. 5.9, N_{1Q1}, N_{2Q1}, R_{B1}, N_{1Q2}, N_{2Q2}, R_{B2} are the number of turns in the primary side, the secondary side, and the burden resistance for the high side switch and the low side switch respectively. Also, the blocks showing $(N_2/N_1)/R_B$ are needed to adjust for the different scaling that may

be used with the two current transformers. Optionally, these two gains may also be multiplied by a common factor α, in order to adjust the estimated inductor current to a desired scaling. Besides, both the sample and hold ICs and the amplifier used to add the switch current signals must have high bandwidth (much higher than the switching frequency f_s), so that the sensor bandwidth is not affected.

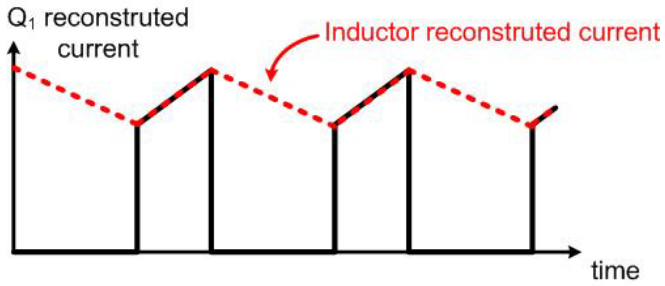

Fig. 5.8 Inductor current reconstruction by joining the minimum and the maximum of the high side switch current during switch turn-on

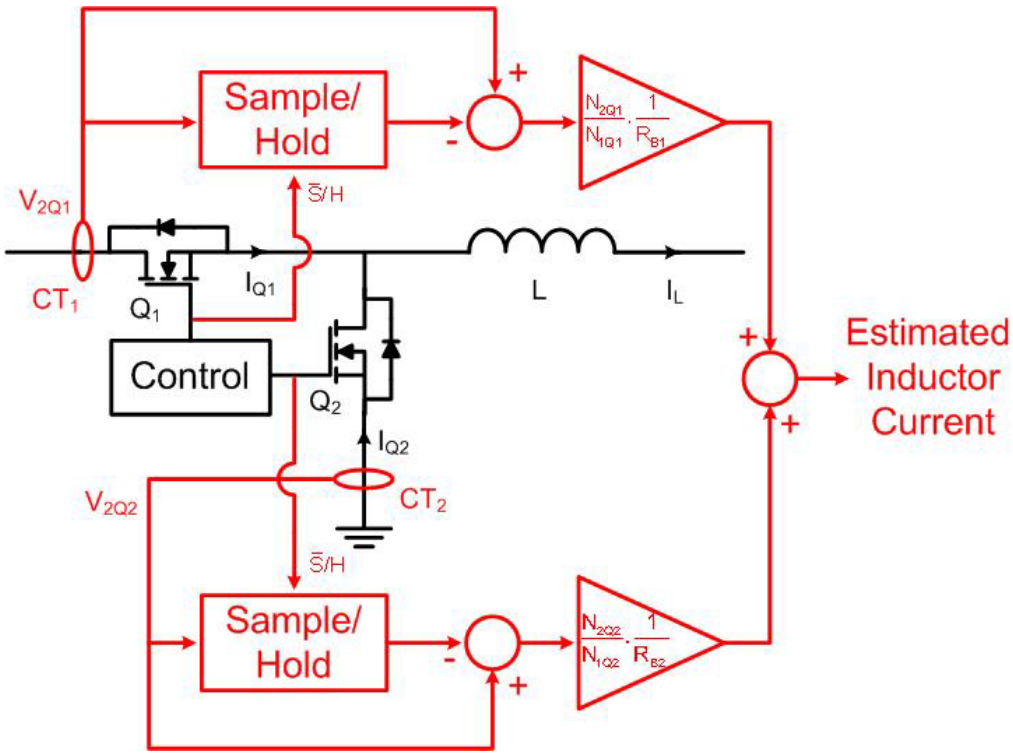

Fig. 5.9 Overall inductor current estimation circuit using two current transformers

There are many advantages for the proposed method compared to other current sensing methods. By using a large turns ratio, the secondary side current can be made much smaller than the primary side current, which is particularly useful in VRM modules, where the instantaneous current may attain 30A in one phase. A relatively large resistance can then be used to sense the secondary current. Such a design will lead to lower conduction loss and less noise problems when compared to a simple current sensing resistor placed in series with the inductor or the high side switch. Also, contrary to most methods presented in the last chapter, it is the instantaneous current which is sensed, and the sensor performance is independent of circuit parameter variations. The proposed method has obviously a greater bandwidth and can be used for either peak or average current mode control.

However, so far, the current transformers have been assumed to work in their linear region. To achieve this, it has to be ensured that no saturation of the transformer core occurs. Besides, the accuracy of the method both in steady state and in transient has to be estimated. There is also additional power loss due to the flux density swing in the transformer core. In the next section, the design issues regarding these aspects will be discussed.

5.3 Design issues in the proposed method

In this section, the design of the current sensor is presented and the design issues and trade-offs are discussed. The accuracy of the current transformer is also investigated. As the DC current flowing in the primary may lead to saturation, requirements for a suitable current transformer will also be presented.

5.3.1 AC attenuation

From (5.6), the transfer function relating the sensed voltage V_{2Q} to the primary current I_Q to be sensed is given by:

$$\frac{V_{2Q}}{I_Q} = R_B \frac{N_1}{N_2}\left(1 - \frac{1}{1+\frac{s}{2\pi f_c}}\right), \tag{5.11}$$

where $f_c = \frac{R_B.R_e}{2\pi N_2^2}$ (5.12)

The transformer acts therefore as a high pass filter with a corner frequency placed at f_c. Thus, it is critical to ensure that this corner frequency is kept much lower than the switching frequency f_s in the design of the current transformer. In this way, only the DC value will be removed from the switch current in the steady state.

To highlight the error due to this low frequency filtering, the measurement of the high side switch current in a single phase converter for a 100A load is simulated for the case of a current transformer having only 5 turns and a high burden resistance of 5 Ω in the secondary. The simulation results are presented in figure 5.10. This steady state sensing error is in fact due to the magnetizing current built up in the core.

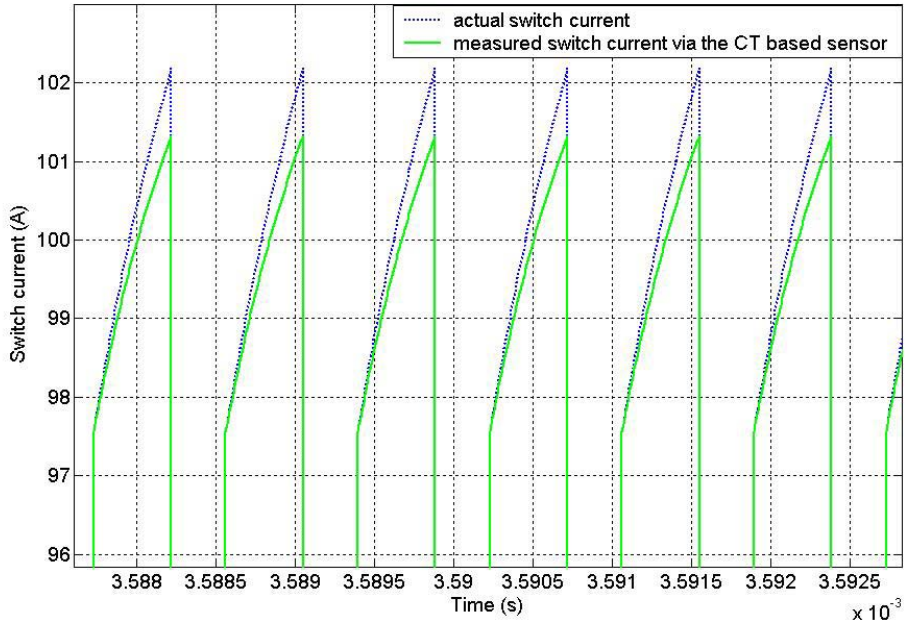

Fig. 5.10 Steady state measurement error for a current transformer having 5 turns in the secondary and 5Ω burden resistance

The AC sensing error due to the current transformer can be defined as:

$$\Delta V_{sAC} = \left| \frac{V_{2Q} - R_B \left(N_1 / N_2 \right) I_Q}{R_B \left(N_1 / N_2 \right) I_Q} \right| \tag{5.13}$$

Therefore, from (5.11), for a primary current of switching frequency f_s, the AC attenuation in magnitude can be estimated by:

$$\Delta V_{sAC} = \frac{1}{\sqrt{1 + \frac{f_s^2}{f_c^2}}} \tag{5.14}$$

In the experimental work presented later in this chapter, the current transformer has 15 turns in the secondary and a maximum of 1 Ω burden resistance. As a result, for the selected toroid, the corner frequency is close to 600 Hz. The AC sensing error is then limited to 0.6 %. However, in an even tighter design, where the burden resistance is reduced to 10 mΩ, the corner frequency is reduced to 6 Hz, and thus the AC sensing error is theoretically drastically reduced to 0.006 %, which is quite negligible.

5.3.2 Transient error

If a sudden step change of ΔI_Q occurs in the primary average current, the new DC value will be slowly filtered off by the current transformer. The following proposes to find the variation of the average secondary voltage V_{2Q} due to the step change in the primary current.

From (5.11), V_{2Q} is given by the inverse Laplace transform of:

$$V_{2Q} = R_B \frac{N_1}{N_2} \left(1 - \frac{1}{1 + \frac{s}{2\pi . f_c}} \right) . \frac{\Delta I_Q}{s} \tag{5.15}$$

Thus, V_{2Q} will vary according to:

$$V_{2Q}(t) = R_B \frac{N_1}{N_2} . \Delta I_Q . e^{-2\pi f_c . t} \tag{5.16}$$

Hence, the DC component is not removed immediately, but in an exponential manner. However, in the reconstructed signal, the DC correction is only made during the off interval. Therefore, there would be a small error *e* during the on interval due to this slow DC filtering. This error is highlighted in Fig. 5.11 for the case of a current transformer having 5 turns in the secondary and 5 Ω burden resistance.

For one cycle starting at time t, this error can be estimated by:

$$e(t) = R_B \frac{N_1}{N_2} . \Delta I_Q \left(e^{-2\pi f_c t} - e^{-2\pi f_c (t + t_{on})} \right), \tag{5.17}$$

where t_{on} is the on-interval in that cycle.

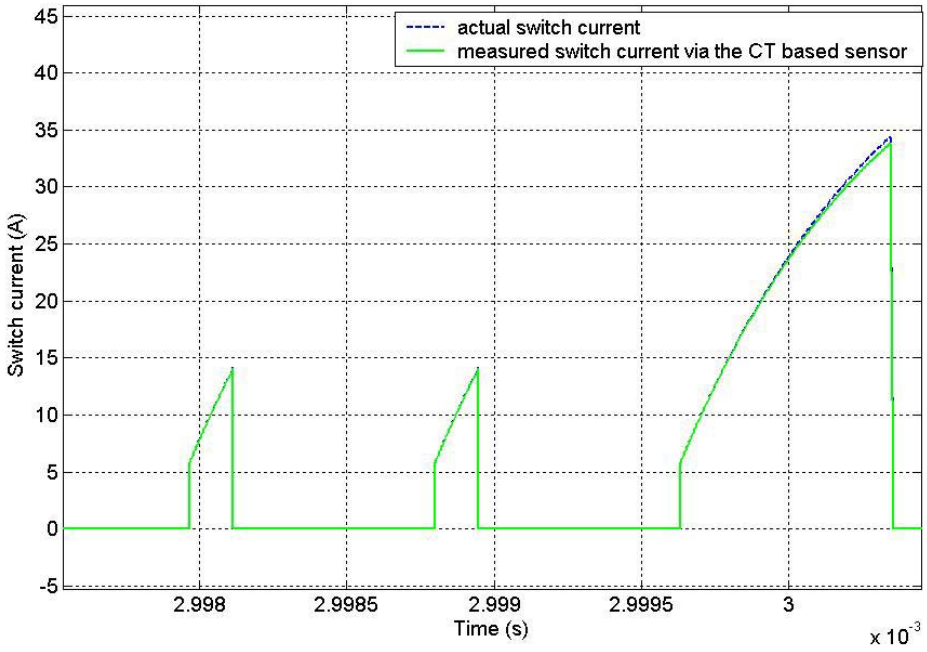

Fig. 5.11 Transient measurement error for a current transformer having 5 turns in the secondary and 5Ω burden resistance

Since under ideal conditions, the primary step change should be fully sensed in the secondary with proper scaling, the transient accuracy ΔV_{sT} can be defined as:

$$\Delta V_{sT} = \left| \frac{e(t)}{R_B \frac{N_1}{N_2} \Delta I_Q} \right|_{\max} \tag{5.18}$$

Assuming there will be at least one switching during one cycle, from (5.16) the transient accuracy in the worse condition can then be estimated to be

$$\Delta V_{sT} = \left(1 - e^{-2\pi \frac{f_c}{f_s}} \right) \tag{5.19}$$

Hence, keeping the switching frequency much higher than the corner frequency also helps in the transient accuracy. For a corner frequency around 600Hz, the transient error is, in the worst case 3%. However, this can be reduced to 0.03% if a smaller burden resistance of 10mΩ is used.

The error *e* represents actually the magnetizing current that is not being sensed during the on-interval. In the worst condition (the switch is fully on during one complete cycle), this current will reach 0.7 mA if a 10 mΩ resistance is used in the secondary. For comparison purposes, for the same type of toroid, if the switch current sensing technique presented in Section 5.1 (Fig. 5.4) is used, and considering only the voltage drop across the diode approximated as 0.5 V, the magnetizing current can reach a value of 23 mA. This also highlights the superiority of this technique over the one proposed in [70] and presented in Fig. 5.4.

Hence, overall, the sensing accuracy is only decreased to less than 0.04 % by using a current transformer (with a burden of 10 mΩ) instead of directly using a current sensing resistance in series. Therefore, this method is almost as accurate as the classical resistive sensing, while being much more efficient as will be shown later in this chapter.

5.3.3 Core saturation

Another aspect of the design is to ensure that the current transformer does not saturate in its operation. If it does, its characteristics will change drastically, and our estimated current will likely be wrong.

By neglecting the hysteresis characteristic of the core, the typical B-H curve during CT operation is shown in Fig. 5.12. Since a switching current with a positive DC component, is applied on the primary side of the current transformer, the core's flux density will settle to an average value B_{DC}, and oscillate around this point, as shown in Fig. 5.12. Thus, we have to ensure that the whole operating domain, shown in Fig. 5.12 is contained within the linear region. In the following, the average flux density and the overall flux ripple are estimated, when the current transformer is subject to a switching current in the primary.

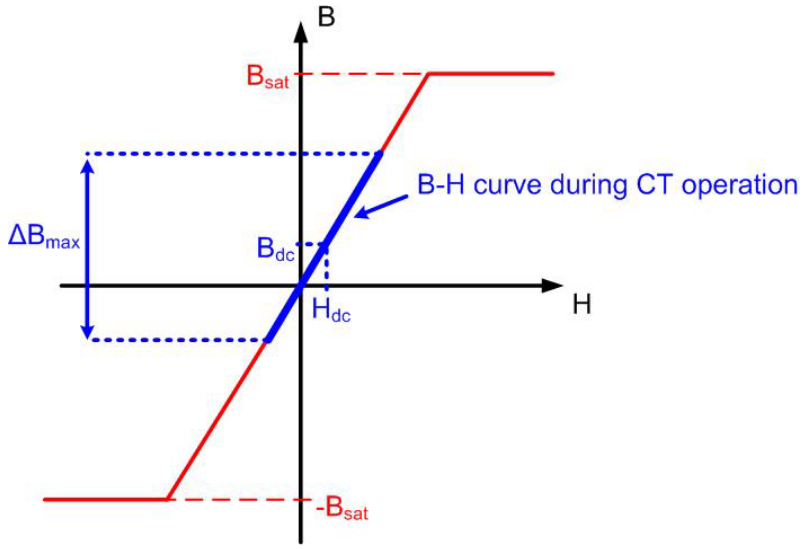

Fig. 5.12 B-H curve during CT operation

a. DC flux estimation

The average flux density B_{DC} under the steady state in the core can be estimated via the Ampere's law. Thus,

$$N_1.I_{DC} = H_{DC}.l, \tag{5.20}$$

where H_{DC} is the DC magnetic field in the core due to I_{DC}, the DC component of the primary current.

Since the operation is assumed to be taking place in the non-saturated region, the DC value of the flux density in the current transformer can be estimated by:

$$B_{DC} = \frac{\mu_0.\mu_r}{l} N_1.I_{DC} \tag{5.21}$$

Let D be the duty cycle, and I_L the average inductor current.

In this case,

- I_{DC}=I_{DCQ1}=$D.I_L$ for the high side switch
- I_{DC}=I_{DCQ2}=(1-D).I_L for the low side switch

It may also be noted that in a multiphase converter, I_L equals the DC load current I_0' corresponding to each phase.

Thus, we can determine the DC core flux density for CT_1 and CT_2 separately as follows:

- $B_{DC} = \frac{\mu_0 \mu_r D}{l} N_{1Q1}.I_0'$ for CT_1 (5.22)

- $B_{DC} = \frac{\mu_0 \mu_r (1-D)}{l} N_{1Q2}.I_0'$ for CT_2 (5.23)

Since usually the steady state duty cycle is quite small (less than 0.2), the average flux density will tend to settle to a higher value in the low side switch current transformer, compared to the high side one. Hence, there will be more constraints in designing CT_2, as this higher flux density should be kept lower than the saturation flux density (B_{sat}).

b. Flux ripple estimation

When the switch current varies around its average, the core flux density will also fluctuate (Fig. 5.10). In the following, the maximum variation of the flux density is estimated from the secondary sensed signal, V_{2Q}. Fig. 5.13 shows the voltage waveform on the secondary side for the current sensors in series with both the switches.

In the steady state, the volt-second balance is valid in the sensed signal. Hence, the shaded areas are equal in Fig. 5.13. Moreover, from Faraday's law, the flux variation in the core is given by:

$$\Delta\varphi = \frac{1}{N_{2Q}} \int V_{2Q} dt \tag{5.24}$$

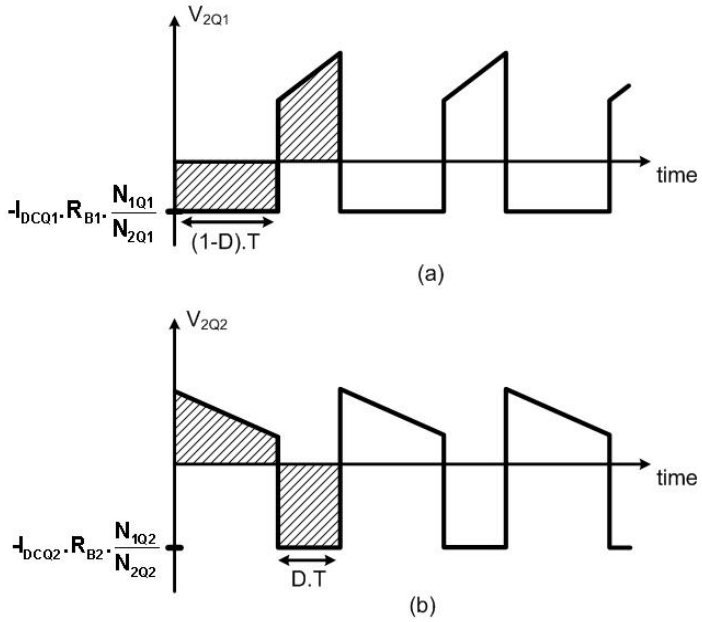

Fig. 5.13 Secondary side voltages for the current transformers on (a) the high side and (b) the low side switches.

Consequently, by calculating the shaded areas in Fig. 5.13, the flux ripple in one cycle can be deduced:

- $\Delta\varphi_1 = \frac{1}{N_{2Q1}} I_{DCQ1}.R_{B1}.\frac{N_{1Q1}}{N_{2Q1}}.(1-D).T = \frac{I'_0.R_{B1}.N_{1Q1}.(1-D).D}{N^2_{2Q1}.f_s}$ for CT_1 (5.25)

- $\Delta\varphi_2 = \frac{1}{N_{2Q2}} I_{DCQ2}.R_{B2}.\frac{N_{1Q2}}{N_{2Q2}}.D.T = \frac{I'_0.R_{B2}.N_{1Q2}.(1-D).D}{N^2_{2Q2}.f_s}$ for CT_2 (5.26)

Therefore, the amplitude of variation of the flux density can be obtained for both current transformers in terms of average inductor current I_L, steady state duty cycle D, secondary burden resistances R_B, switching frequency f_s, core's cross sectional area A, and primary and secondary number of turns N_{1Q}, N_{2Q} .

- $\Delta B_1 = \frac{I_L.R_{B1}.D.(1-D).N_{1Q1}}{N^2_{2Q1}.f_s.A}$ for CT_1 (5.26)

- $\Delta B_2 = \frac{I_L.R_{B2}.D.(1-D).N_{1Q2}}{N^2_{2Q2}.f_s.A}$ for CT_2 (5.27)

In this case, the equations for the flux density ripples are similar for the low side and high side switches. However, as the DC flux has been shown to be higher for the low side switch, we can use higher number of turns in the secondary to limit the flux ripple.

In order to ensure that the core does not saturate, we should make sure that for both current transformers $B_{DC}+\Delta B/2$ is less than the saturation flux density B_{sat} limit fixed by the core material, under the worst case operating condition.

5.3.4 Current sensor power loss analysis

By having a high number of turns in the secondary, the conduction loss is drastically reduced in the proposed current sensing method compared to the CSR. Let us consider a current transformer with 15 turns and a burden resistance of 0.5 Ω in the secondary side, placed in series with the high side switch of a synchronous converter. The average inductor current and duty ratio of the converter are assumed to be 25 A and 0.16 respectively. Neglecting the current ripple, the conduction loss in the burden resistance can be estimated to be approximately 0.22 W. However, if in place of a CT-based sensor, a CSR of only 10 mΩ is used, the resulting power loss is as high as 1.44 W. Hence, the conduction loss is considerably reduced in the proposed scheme as compared to the CSR. Nevertheless, the use of magnetic material in the proposed current sensing scheme introduces also additional losses called core losses [28].

This power loss constitutes mainly of two kinds: hysteresis power loss P_H and eddy current loss P_e [28]. These losses are dependent on the operating frequency, flux ripple, core volume, and material characteristics. For high frequency operation, as required in our application, ferrite materials are generally employed though they exhibit low saturation flux density [28]. Fig. 5.14 shows the typical core loss for such a material for different operating frequencies and according to the flux density ripple.

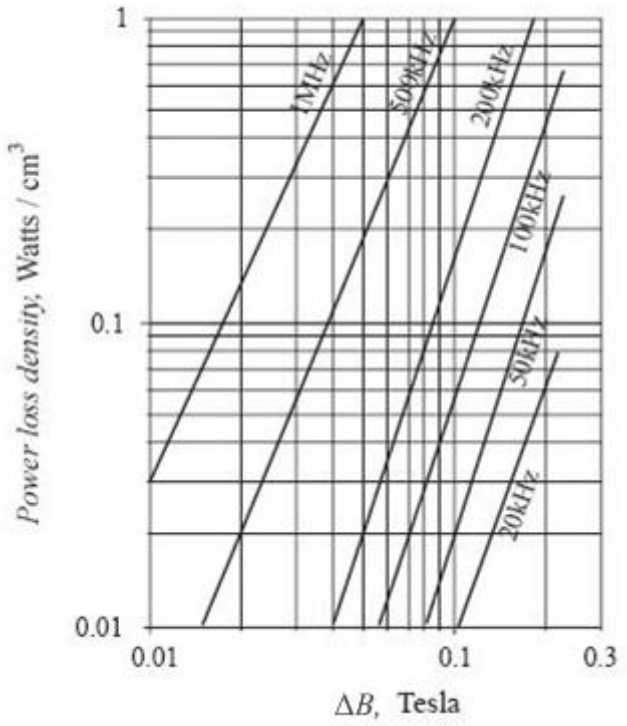

Fig. 5.14 Typical core loss data for a high-frequency power ferrite material [28].

This figure is usually provided by the core manufacturer, and is generally used to estimate the core losses. However, in our application, the resulting core loss estimation is only an approximation, since the DC flux density present in the core is usually not taken into account in the data provided by the manufacturer.

Nevertheless, in the magnetic core used in the experimental work presented later, with a 0.5 Ω resistance in the secondary and a maximum of average inductor current of 30 A, the flux ripple (peak-to-peak ripple/2) is estimated to 2.4 mT. Therefore, from the manufacturer datasheet [78], the total maximum core loss can be estimated approximately to be only 10 mW.

Hence, the total power loss including the burden resistance loss for the CT as detailed previously is less than 0.4 W as against the 1.5 W loss of the 10 mΩ CSR. This shows the potential superiority of the proposed current sensing scheme over the classical current sensing resistor.

5.4 Experimental results

Experimental work for CT based sensor has been carried out to demonstrate the feasibility and the performance of the proposed current sensor. For this purpose, a single phase buck converter controlled in a peak current mode control manner, has been built for a switching frequency of 150 kHz.

The input DC voltage is fixed at 12 V and the output voltage is regulated to be 1.8 V. A ferrite core made of 3C90 material with an initial relative permeability (μ_r) of 2300 is used for designing the current transformers. The core size is small with a mean magnetic path length (l) of 30.1 mm and cross sectional area (A) of 12.2 mm^2. These values show that a relatively small core is enough for this method. A single turn primary is used for both the current transformers with the switch current passing through the hole in the core. The secondary side consists of fifteen turns and a burden resistance (R_B) of 1 Ω for both CT_1 and CT_2. Thus, the corner frequency f_c, is close to 600 Hz and for an average inductor current of 5 A, the maximum flux density is estimated close to 0.07 T for CT_1 and 0.3 T for CT_2. This difference is due to the low duty cycle value; a higher number of turns can in fact be used for CT2 in order to avoid saturation.

The sample and hold amplifier used is *Harris Seminconductor*'s HA-5320 [81]. The voltage feedback amplifier used in the summer circuit is AD8056 manufactured by *Analog Devices* [82]. A simple PI controller is designed in the outer voltage loop in the same manner as in Chapter 3, and the overall bandwidth is designed to be 21 KHz. The closed loop scheme has been implemented using the UC3825 (*Unitrode*) PWM controller [67].

More hardware details are provided in Appendix B.

Fig. 5.15 shows the reconstruction of both the switch currents with Fig. 5.15(a), Fig. 5.15(b), Fig. 5.15(c) showing the reconstruction of the high side switch current and Fig. 5.15(d), Fig. 5.15(e), Fig. 5.15(f) showing that of the low side switch current. Fig. 5.16(a) & Fig. 5.16(c) show the high side and the low side current waveforms both sensed by a Hall Effect sensor (*Yokogawa* 700937) and also by the proposed current transformer based sensor. The two waveforms are superimposed in Fig. 5.16(a) & Fig. 5.16(c) and it may be noted that there is very little error between the two. This is further illustrated in the waveforms in Fig. 5.16(b) & Fig. 5.16(d) which show directly the error between the Hall Effect sensor and the proposed sensor.

These experimental results clearly confirm the accuracy of the proposed sensor in sensing the switch currents. The close matching of the waveforms, even during switching oscillations, clearly shows the high bandwidth of the proposed current sensor. We may notice that each switch current shows some oscillations which is reproduced faithfully by the sensor. This is attributed to the parasitic capacitance of the MOSFET. We may use a small capacitor in parallel with the secondary side resistance, in order to filter these high frequency oscillations, if necessary. This capacitance should be chosen high enough to filter the parasitic oscillation, but should not affect the switching frequency components in the signal.

Finally, by adding the two signals, we obtain the inductor current signal shown in Fig. 5.17, where the resulting inductor current waveforms is superimposed with the signal sensed by the hall-effect sensor. The noise in the signal is due to the parasitic oscillation in the MOSFET. As stated, we may use a low pass filter to filter it. In fact, if used in an average current mode control scheme, the controller itself will filter it.

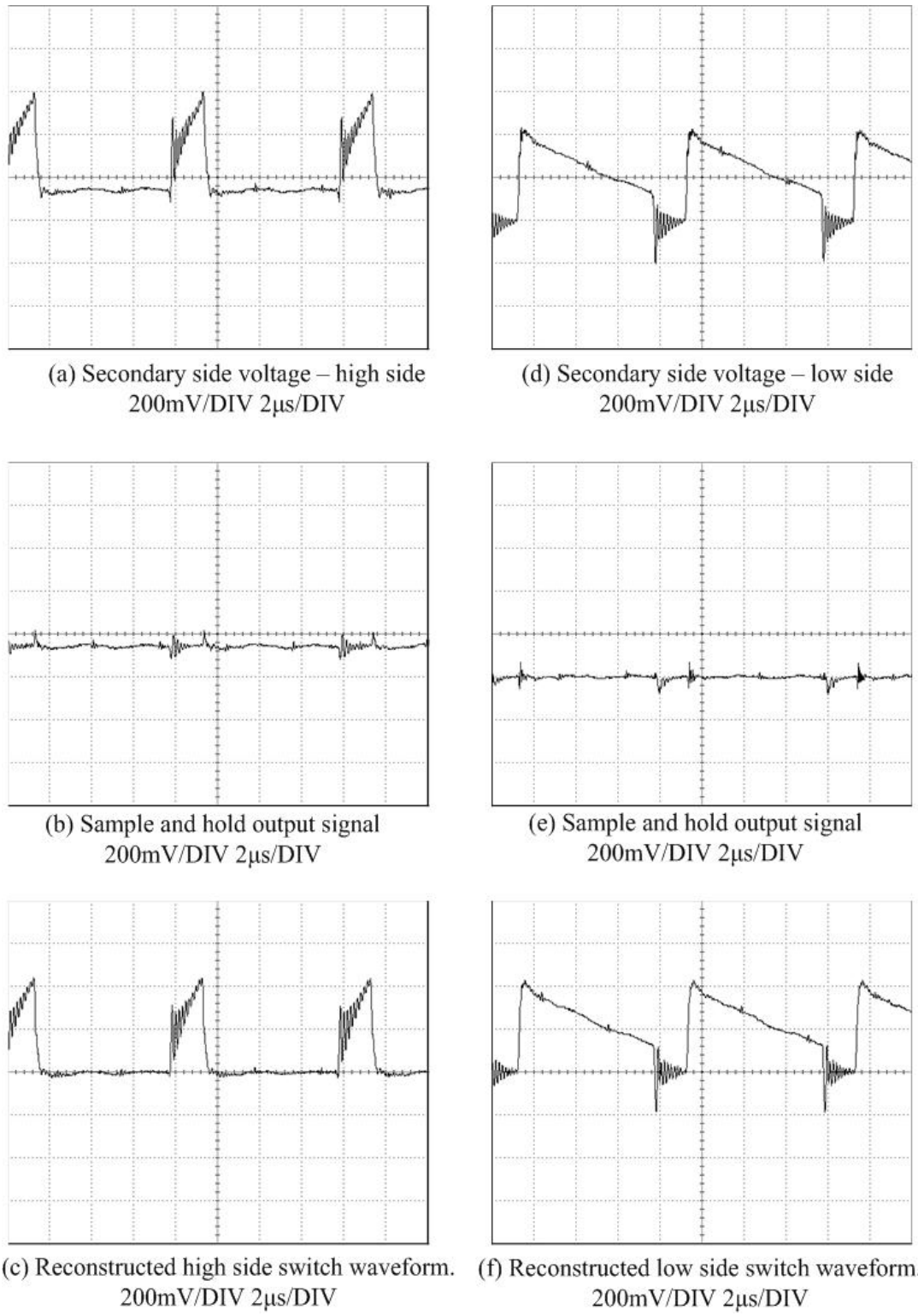

Fig. 5.15 Reconstruction of current signal waveform

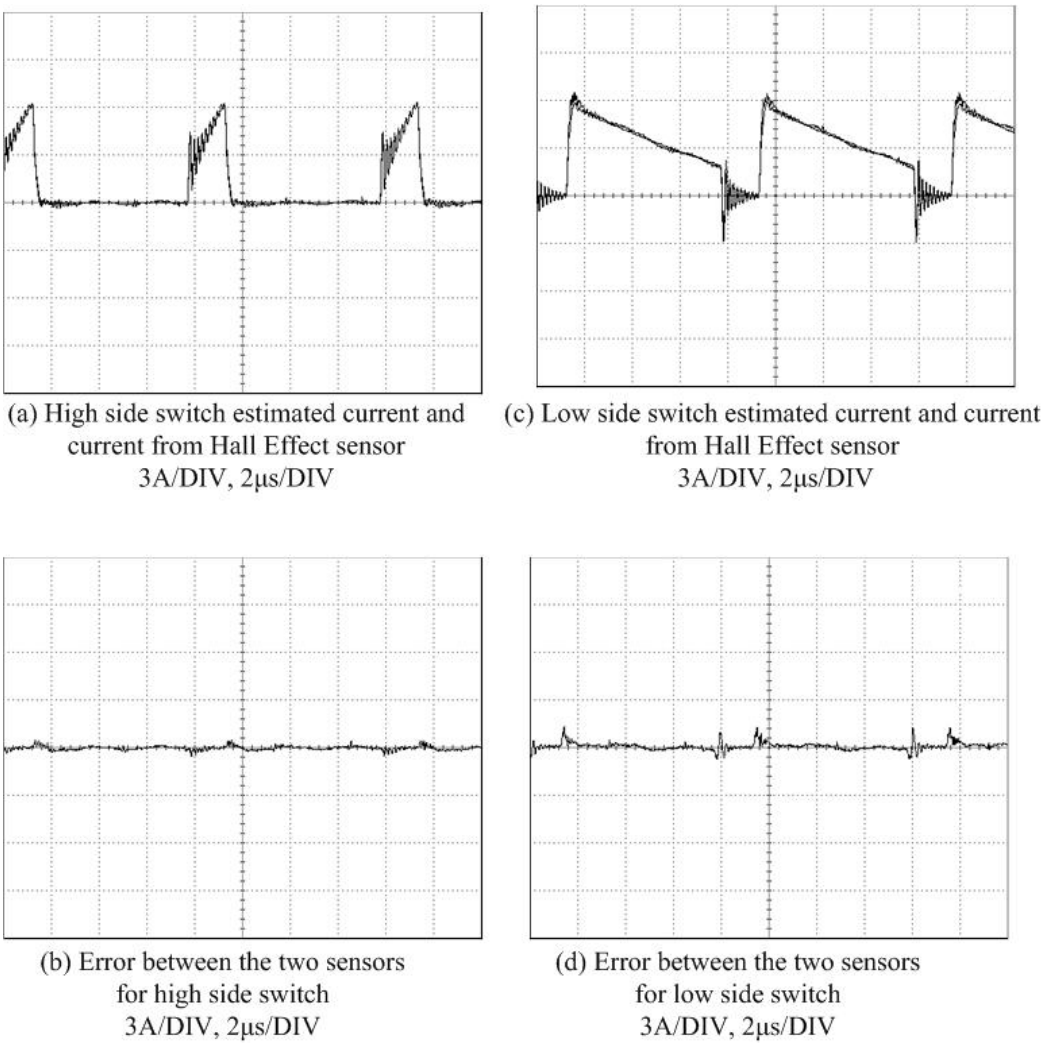

Fig. 5.16 Comparison between the current transformer sensor and Hall Effect sensor

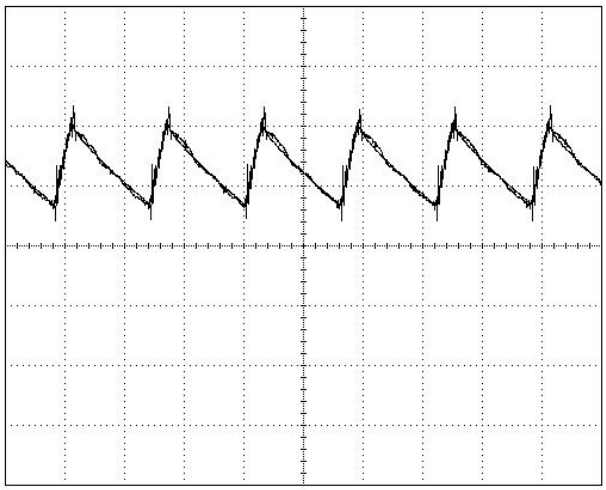

Fig. 5.17 Estimated inductor current 200mV/DIV⇔3A/DIV, 5μs/DIV
and sensed current from the hall-effect sensor 3A/DIV, 5μs/DIV

The performance of the converter has also been tested during a step load, with the output current abruptly changing from 3.5 A to 25.6 A. During this part of the experiment, 0.5 Ω secondary side burden resistors have been used.

The converter using a peak current mode control will have, in general, a fast transient response. Fig. 5.18 presents the secondary side voltage of the current transformer, the output of the sample ad hold IC, and the final reconstructed signal. It can be noticed that the DC component of the switch current (see the top waveform in Fig. 5.18) does not vanish instantaneously in the secondary side of the current transformer, but slowly reduces to zero, as expected from the transfer function (5.11). As the switching frequency is much higher than the corner frequency of the current transformer (f_c), the sample and hold IC is able to reconstruct accurately the valley of the current transformer output signal. Thus, the signal is well reconstructed even during transient as shown in Fig. 5.19, which compares the high side switch current signal waveforms as measured by a hall-effect sensor current probe and by the proposed current transformer based current sensor.

These experimental results confirm also the design methodology adopted in Section 5.2 and 5.3.

Fig. 5.18 Experimental waveforms for a step-up load from 4A to 25A;
CH4-CT secondary signal; CH1-sample and hold IC output;
CH2-reconstructed high side switch current. 500mV/DIV, 10μs/DIV

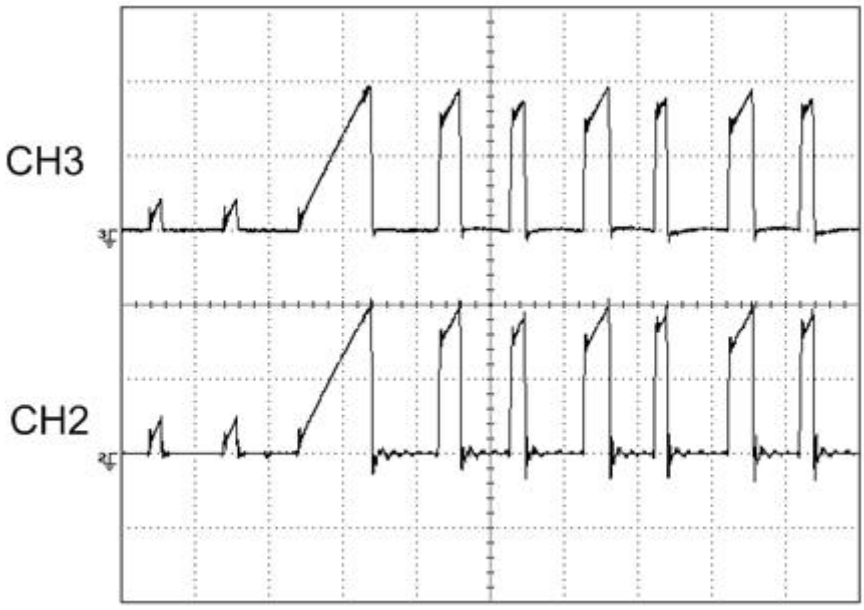

Fig. 5.19 Experimental waveforms for a step-up load from 3.5A to 25.6A;
CH3-High side switch current sensed by the Yokogawa Hall-Effect sensor, 15A/DIV; CH2- reconstructed switch current, 500mV/DIV, 10μs/DIV

5.5 Conclusion

Current transformers are widely used in power systems due to their efficiency and accuracy and their isolation property. However, their inability to sense the DC current has prevented their use in buck derived topologies and, so far current transformers based technique to sense the switch current were not capable of delivering the required performance.

In this chapter, a new technique overcoming these problems has been presented. Indeed, via simple signal processing, the DC component is recovered when sensing the switch current using current transformers. This method can also be used to deduce the instantaneous inductor current waveforms, if needed. Analysis both under steady state and under dynamic conditions has been carried out to explore the design issues involved. Experimental results have also been provided to demonstrate the feasibility, fast response and accuracy of the sensor.

The proposed current sensor has low power loss, fast response and is accurate. Its potential superiority over other current sensing schemes presently being used in VRMs, has been demonstrated throughout this chapter. The proposed current sensing method is hence well suited for demanding applications such as the multiphase converter used in VRM applications. It can be used to implement fast response PCMC in such applications. Besides a multiphase buck converter, the proposed technique can also be applied to charge mode control of flyback converter, which is used in Power Factor Conversion units. Hence, it has a large domain of applications in power electronics.

CHAPTER 6

CONCLUSION

6.0 Background

With the development of Very Large Scale Integration techniques (VLSI), the number of transistors integrated in the microprocessor has continually increased in an exponential way. As a result, the CPU computation speed has increased greatly. At the same time, power consumption by the CPU has also gone up tremendously. In order achieve a high efficiency, modern processors work under very low core voltage. Moreover, depending on the running task, the current drawn by the CPU varies over a large range of magnitude. In many cases, slew rates as high as 930 A/ μs are also required. Due to the stringent power requirements, a dedicated high bandwidth and efficient DC-DC converter, called Voltage Regulator Module (VRM) is used to power up the CPU.

6.1 Thesis Overview

Voltage Regulator Modules used in modern day CPUs employ multiphase interleaved buck converter topology. This topology, as discussed earlier in the thesis, has several advantages such as good heat management, and capability of achieving fast transient response. The stringent requirements of CPU make the control of VRM challenging. In interleaved VRMs, sharing of load current among the various phases (both under transient and steady-state) complicates the control task further. A proper sharing of current in the various phases is indeed essential to ensure low device stresses.

Thus, the first part of the thesis focuses primarily on the modeling, design and control of multiphase interleaved VRMs. This part establishes that peak current mode control technique is capable of achieving excellent dynamic and steady state performance in VRM units. A high performance current sensor is an important requirement for such control scheme. Thus, the second part of the thesis focuses on a novel current sensor for this application, which synthesizes the inductor current in the VRMs for control purposes.

6.1.1 Interleaved VRMs

a. Modeling, Design, and Control

In this thesis, the current sharing in the individual phases in a VRM is investigated using three popular control techniques, namely

1. Voltage Mode Control (VMC)

2. Average Current Mode Control (ACMC), and

3. Peak Current Mode control (PCMC).

To begin with, approximate large-signal models of the converter using the above-mentioned control techniques were developed. The accuracy of the developed models was evaluated using computer simulations.

In general, the design of the converter is independent of the control scheme employed. However, in the case of VRMs where fast dynamic response is essential, the choice of converter parameters depend on the control technique employed. For every control technique considered, there exists an inductance value called the 'critical' inductance that optimizes the dynamic response of the converter. This critical inductance value corresponds to the highest inductance using which the desired change in system operating point is achieved without control saturation, for

example during a light-load to full-load transient. Beyond this value of inductance, the duty ratio saturates during transient, and hence the response is slower. The critical inductance value corresponding to various control techniques considered were obtained using the approximate large-signal models developed earlier and were verified using simulation results. Thus, the proposed large signal model allows the design and the evaluation of the different control techniques that can be applied to the VRM.

b. Comparison of Various Control Techniques

The dynamic performance of the various control schemes equipped with the corresponding critical inductor were compared for a simulated load transient from 100 A to 10 A. The load change from high to low value was considered since it was shown to be a more constraining change than in the opposite direction from a dynamic performance point of view.

The VMC was observed to achieve a large closed loop bandwidth and resulted in fast transient response. On the downside, even a 2 % variation in the inductor value in the phases resulted in improper current sharing even under steady state. This is due to the fact that VMC does not have any control on the current sharing process in the interleaved converter. This has efficiency, size and cost implication for the converter.

The ACMC is able to achieve good current sharing both under transient state and under steady state of operation. However, on account of low bandwidth, the dynamic response of the converter is rather slow.

The PCMC achieves good current sharing besides offering better transient performance when compared to ACMC. On the downside, a good PCMC scheme requires a clean inductor current waveform, as the control is susceptible to noise.

6.1.2 Current Transformer Based Current Sensor

As mentioned before, sensing the current in VRMs accurately is essential to achieve proper current sharing, particularly with PCMC scheme. Chapter 4 discussed the various techniques employed to sense the inductor current. The popular current sensing techniques are either susceptible to changes in circuit parameters or sluggish in nature.

In Chapter 5, a novel current synthesizing technique based on current transformers was proposed. The proposed technique senses the switch currents using current transformers. From the sensed switch currents, the inductor current is reconstructed using simple signal processing. Detail analysis has been carried out to estimate the accuracy and efficiency of the proposed current sensing scheme. Various design issues involved has also been discussed. The proposed current sensor was shown to be efficient, yet capable of fast dynamic response. Due to these advantages, the method has the potential to be implemented in PCMC applications. Experimental results have been provided to demonstrate the feasibility, fast response, and accuracy of the sensor.

6.2 Future works

In this thesis, in order to demonstrate the potential of the proposed current sensing scheme, the CT based sensor has been tested in the case of the high frequency single phase buck converter. In the future, the proposed sensor may be extended to control the multiphase converter used in VRM applications.

Furthermore, the electronic circuitry used to synthesize the inductor current or the switch current can be integrated into a single IC. Using such an IC, the user will

only need to select the number of turns and the burden resistance to be placed in the secondary side of the CT.

Finally, although a PCMC technique applied to a buck converter was used to demonstrate the performance of the proposed current sensing technique, the technique can also be extended to other control techniques involving current sensing such as the charge control. The proposed current synthesizing technique can also be extended to other AC current sensors such as the Rogowski coil.

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PUBLICATION RELATED TO THIS RESEARCH WORK

- H. Marecar, R. Oruganti, "Fast and Accurate Current Sensing in a Multiphase Buck converter", in *Proceedings of 6th IEEE International Conference on Power Electronics and Drive Systems*, vol. 2, pp. 166-171, November 2005

APPENDIX A

SIMULATION DETAILS

In this thesis, the Matlab/Simulink software together with PLECS toolbox has been used to simulate the various converter and control circuits. In this section, details of these simulations are provided.

A.1 Steady state duty cycle estimation

The following program is used to estimate the steady state duty cycle that has to be provided by the control circuit to achieve the desired output voltage in the converter.

```
function y=dutycycle(x,r1,r2,r3,esr,l,c,vin,i0,vodes)
%r1=Upper Mosfet On resistance
%r2 =Lower Mosfet On resistance
%r3 =Inductor series resistance
%esr =Output capacitor ESR
%l =Inductor Value
%c =Output capacitor value
%rL =load resistance
%vin =Input voltage
%i0 =output current
%vodes =desired output voltage

%voltage to duty cycle trasnsfer function
%steady state vector:(IL, Vc)
%input: Vin
% steady state equation during on time
aon=[-(r1+r3+esr)/l -1/l;1/c 0] ;
bon=[vin/l esr/l; 0 -1/c];
con=[esr 1];
don=[0 -esr];
% steady state equation during off time
aoff=[-(r2+r3+esr)/l -1/l; 1/c 0];
boff=[0 esr/l;0 -1/c];
coff=con;
doff=don;

%steady state vector for a given duty cycle x
```

```
SV=-(aon*x+aoff*(1-x))^(-1)*(bon*x+boff*(1-x))*[1;i0];
y=con*SV+don*[1;i0]-vodes;

%D=steady state duty cycle value
D=0;
while dutycycle(D,R1,R2,R3eq,ESR,Leq,C,RL,Vin,I0,Vodes)<0
   D=D+0.001;
   dutycycle(D,R1,R2,R3eq,ESR,Leq,C,RL,Vin,Vodes);
end
D
```

A.2 PLECS converter circuit diagrams

PLECS (Piece-wise Linear Electrical Circuit Simulation) is a Simulink toolbox for system-level simulations of electrical circuits. It is especially designed for power electronic circuits. In this thesis, the various converters have been simulated using this toolbox. In the following the PLECS circuit diagram for different converters used in this thesis are presented.

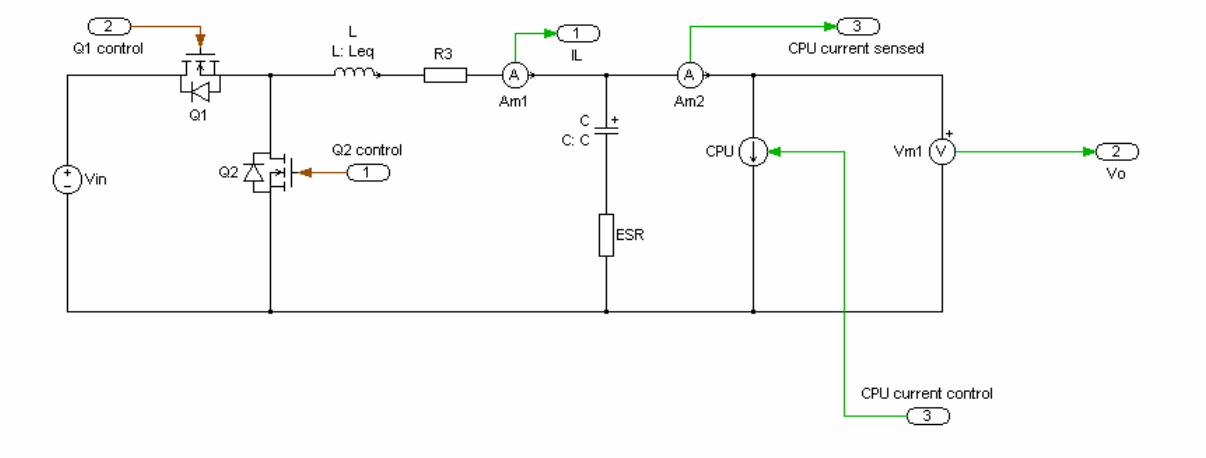

Fig. A.1 Single phase equivalent circuit used in the simulation for the VMC

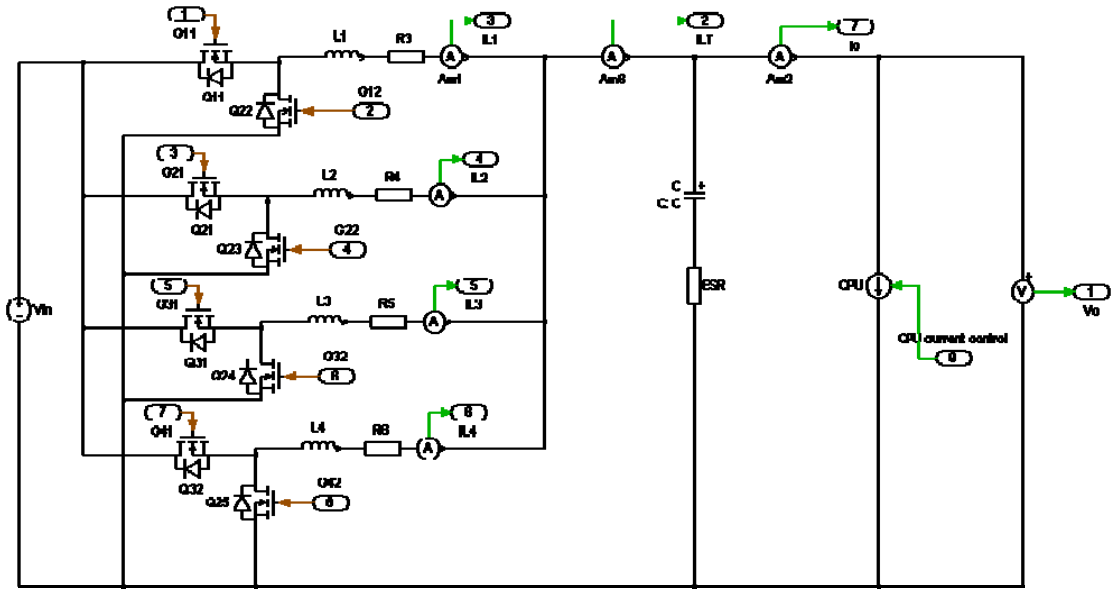

Fig. A.2 Multiphase converter circuit used in the simulations

A.3 Control logic circuit diagram

In this section, the control logic circuits used to drive the MOSFETs are presented.

Fig. A.3 represents the PWM logic diagram used in the simulations. As shown in this figure, the PWM logic has been modified to allow only one turn on or turn off during one switching period. Such constraint is indeed present in most PWM control ICs used for VRM applications.

Fig. A.4 shows the logic diagram used in Peak Current Mode Control.

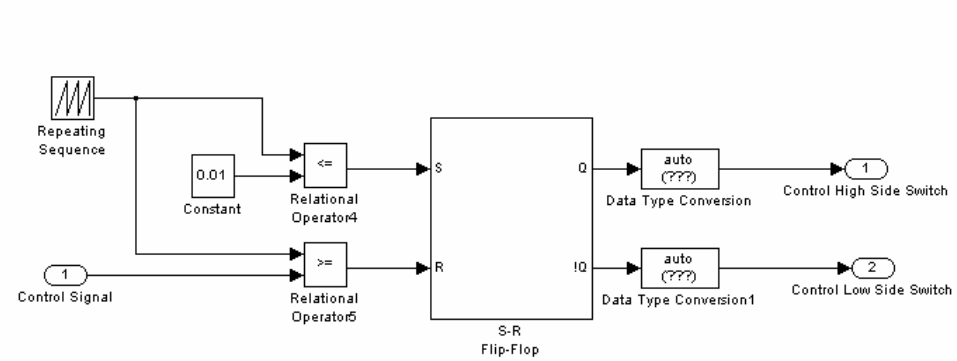

Fig. A. 3 PWM logic diagram

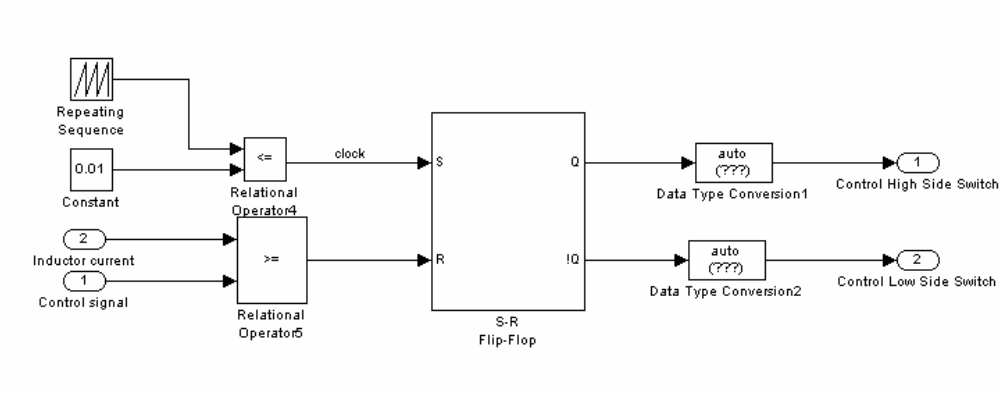

Fig. A.4 Peak Current Mode Control logic diagram

A.4 Large signal model comparison

In this thesis, it has been shown that the different state variable in the converter can be predicted using large signal models, as shown in Fig. A.5 and Fig. A.6.

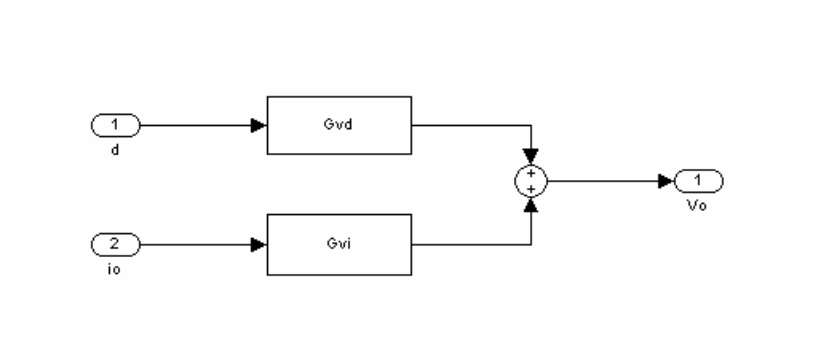

Fig. A.5 Large signal model used in VMC

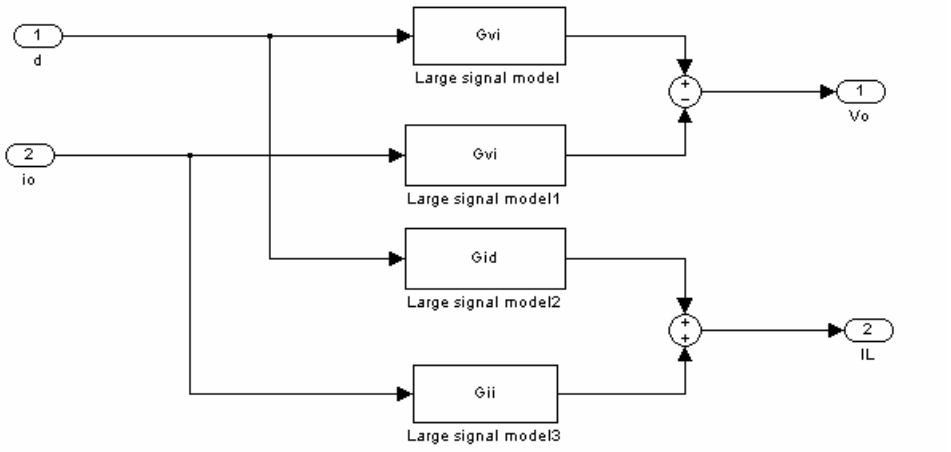

Fig. A.6 Large signal model used in ACMC

The results from these models are compared with the results from the actual converter using the simulation diagrams shown in the following.

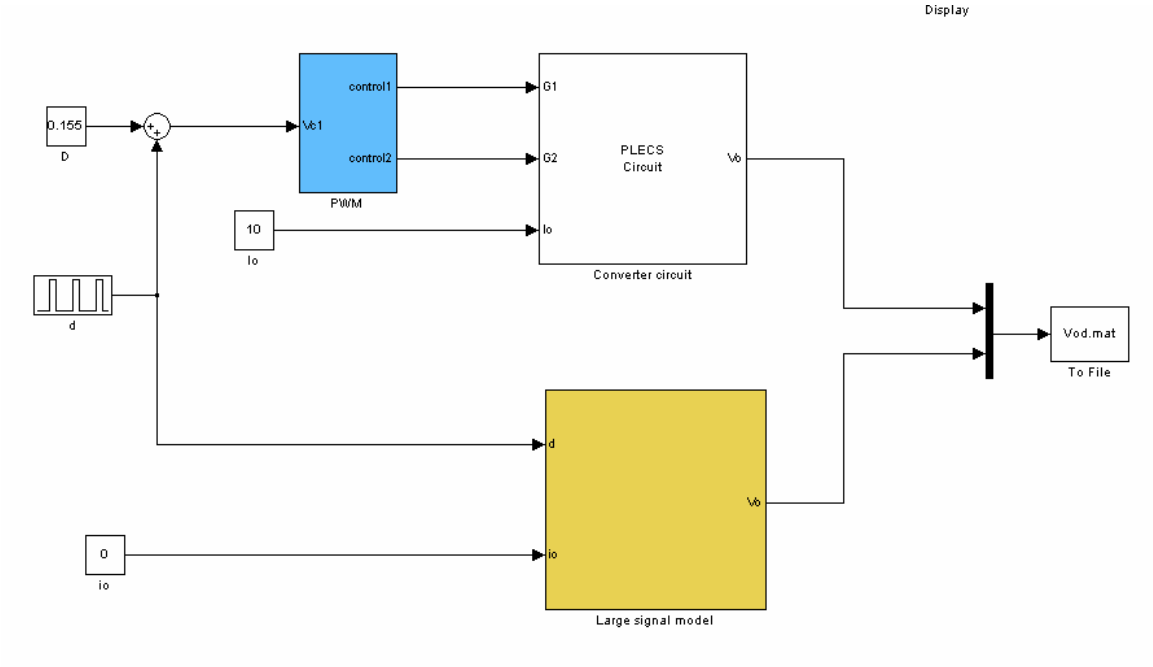

Fig. A. 7 Simulation diagram used to compare the large signal model in VMC with the actual converter when the duty cycle vary in a step manner

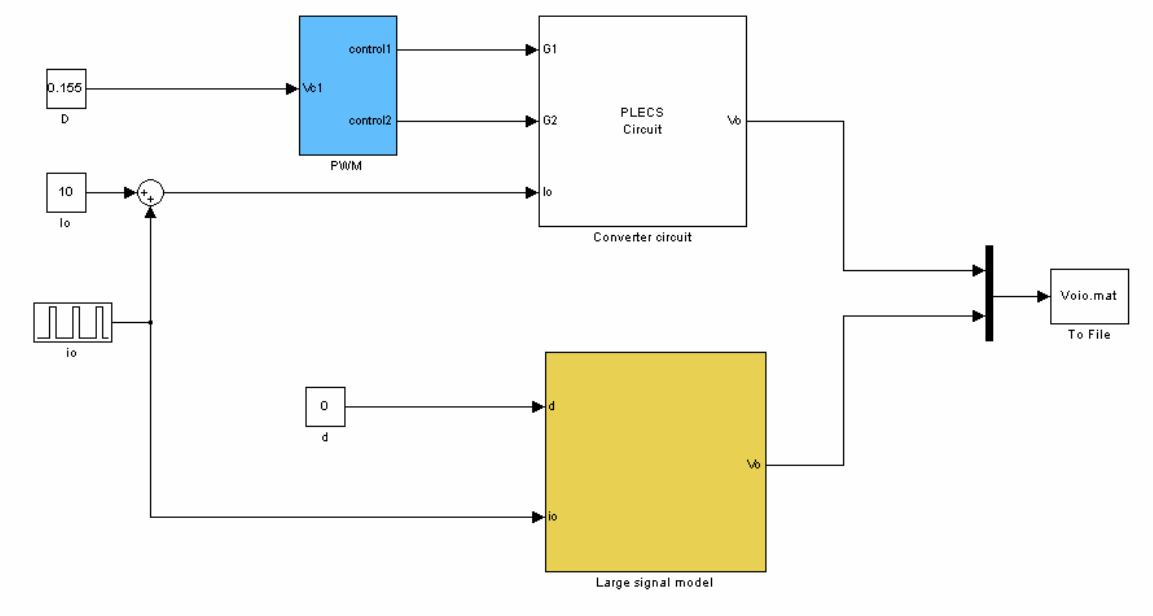

Fig. A.8 Simulation diagram used to compare the large signal model in VMC with the actual converter when the load vary in a step manner

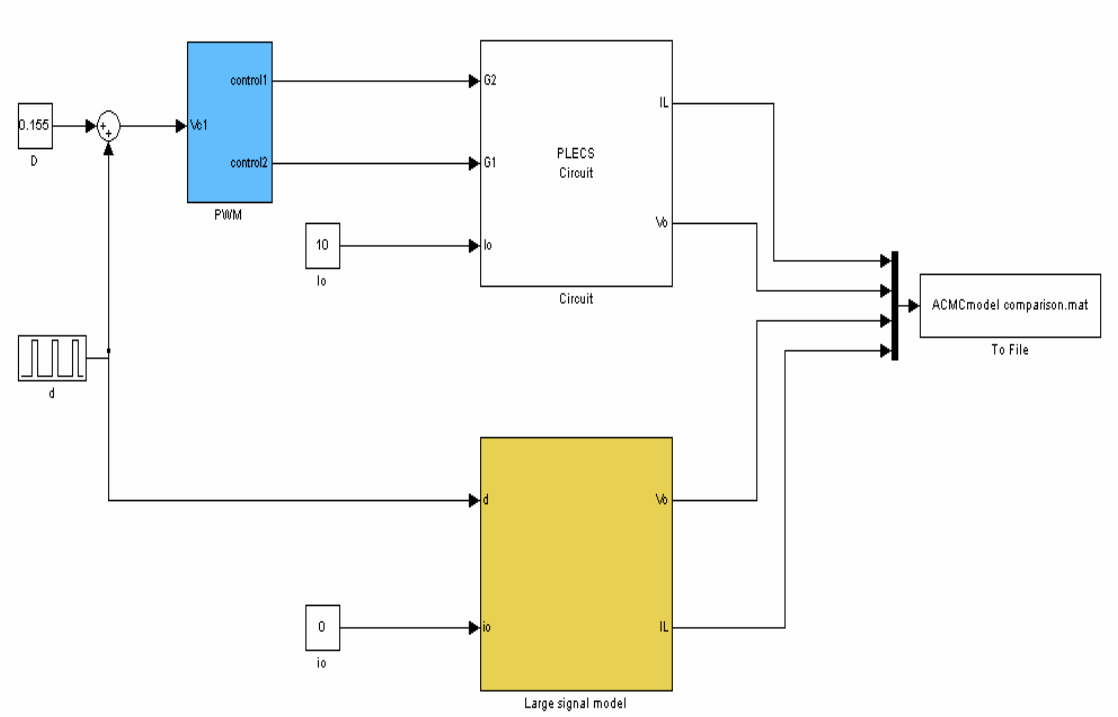

Fig. A.9 Simulation diagram used to compare the large signal model in ACMC with the actual converter when the duty cycle vary in a step manner

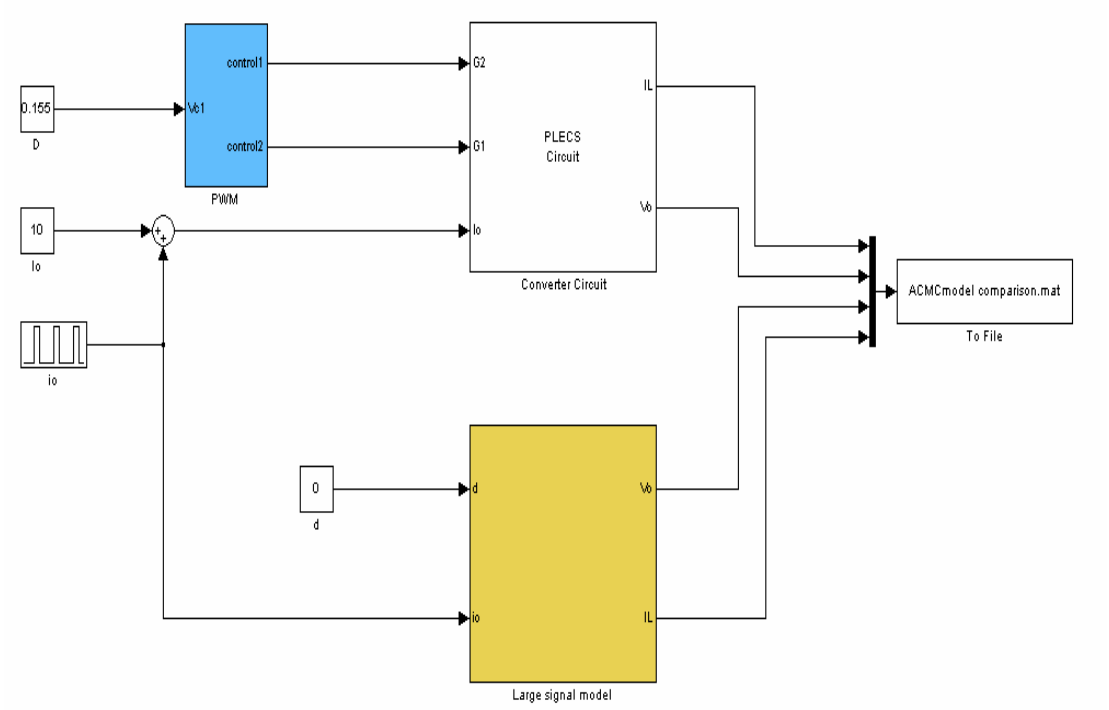

Fig. A.10 Simulation diagram used to compare the large signal model in ACMC with the actual converter when the load vary in a step manner

A.5 Control diagrams

The converter is finally simulated together with the control circuit for each kind of control method, as shown in the following figures. In PCMC, the proposed large signal model is also simulated with the overall scheme for comparison.

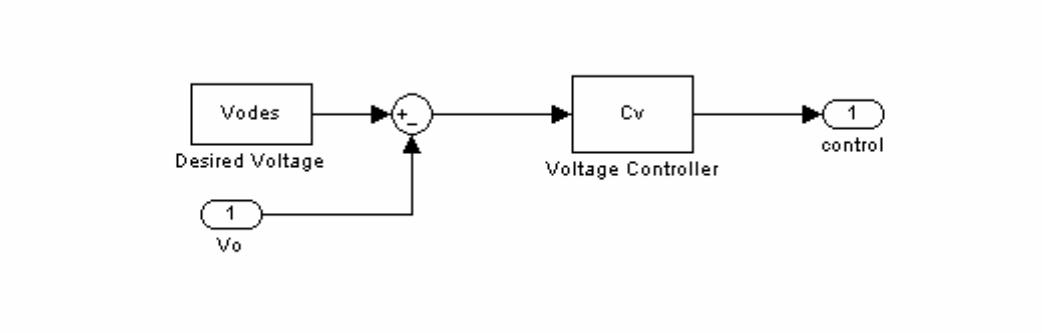

Fig. A.11 VMC Control diagram used in the single phase equivalent circuit

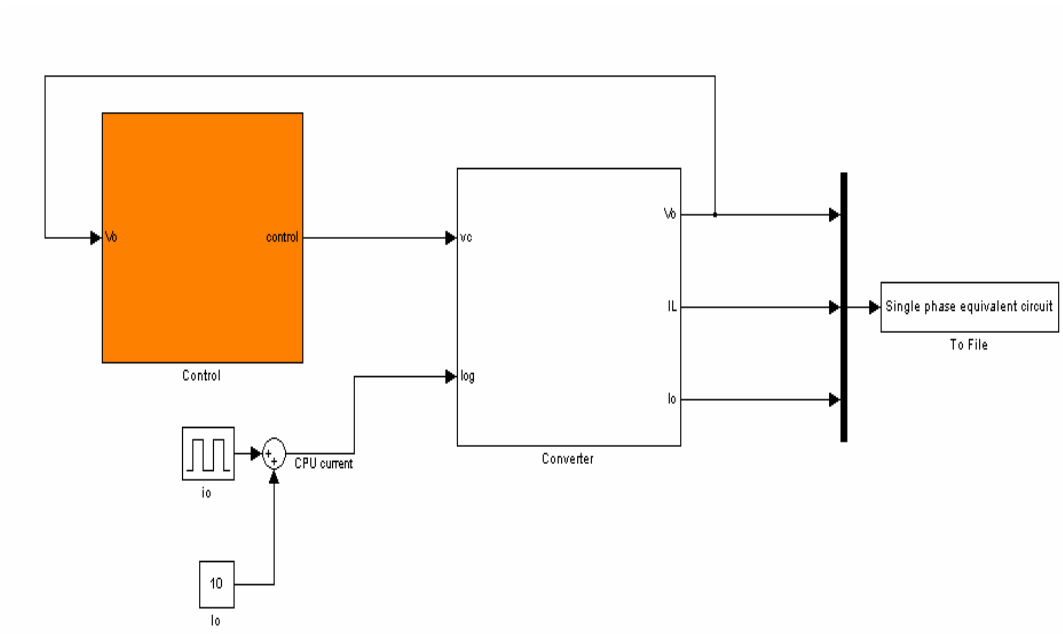

Fig. A.12 Overall simulation diagram for the single phase equivalent circuit in VMC

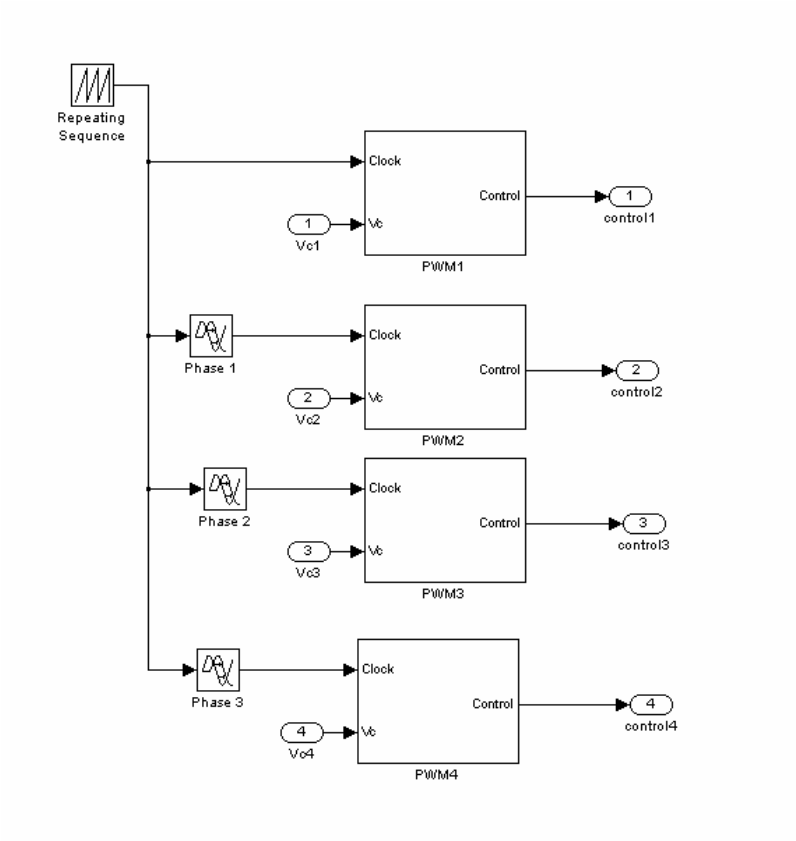

Fig. A.13 PWM Control diagram used for VMC and ACMC in the multiphase converter

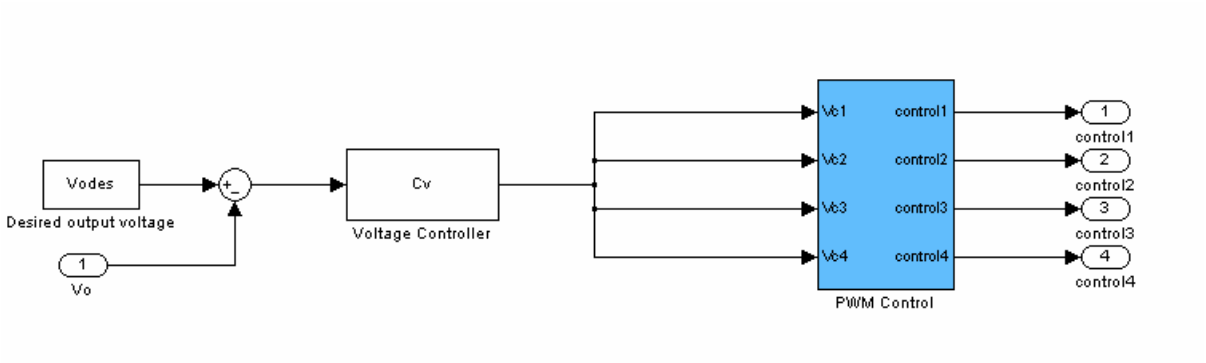

Fig. A.14 VMC Control diagram used in the multiphase converter

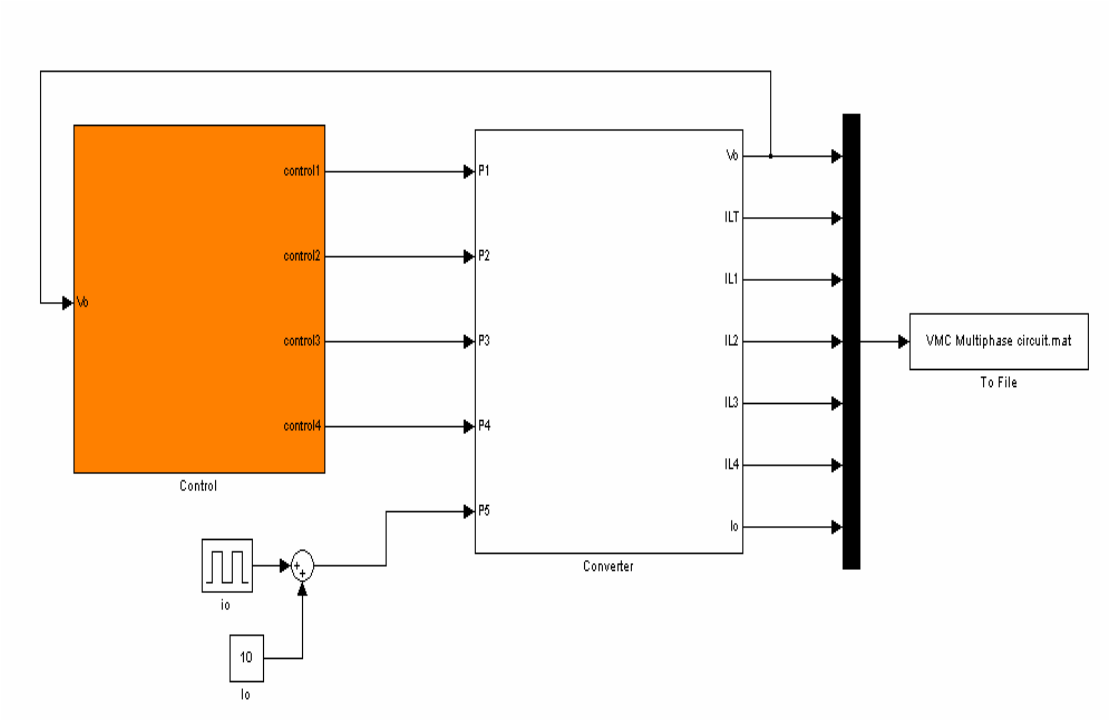

Fig. A.15 Overall simulation diagram used for VMC in the multiphase converter

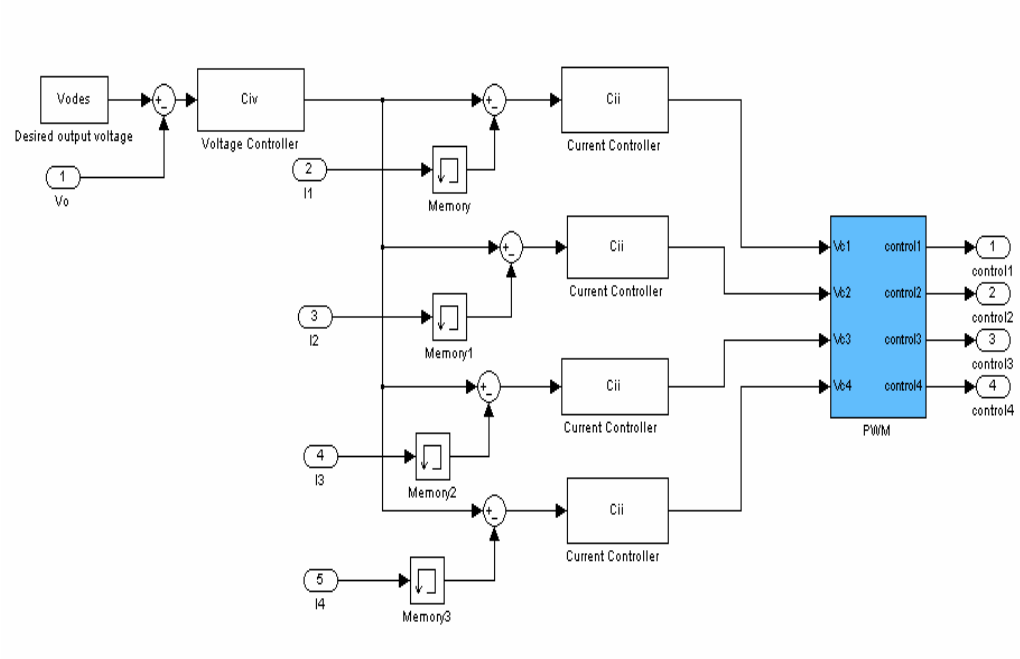

Fig. A.16 ACMC Control diagram used in the multiphase converter

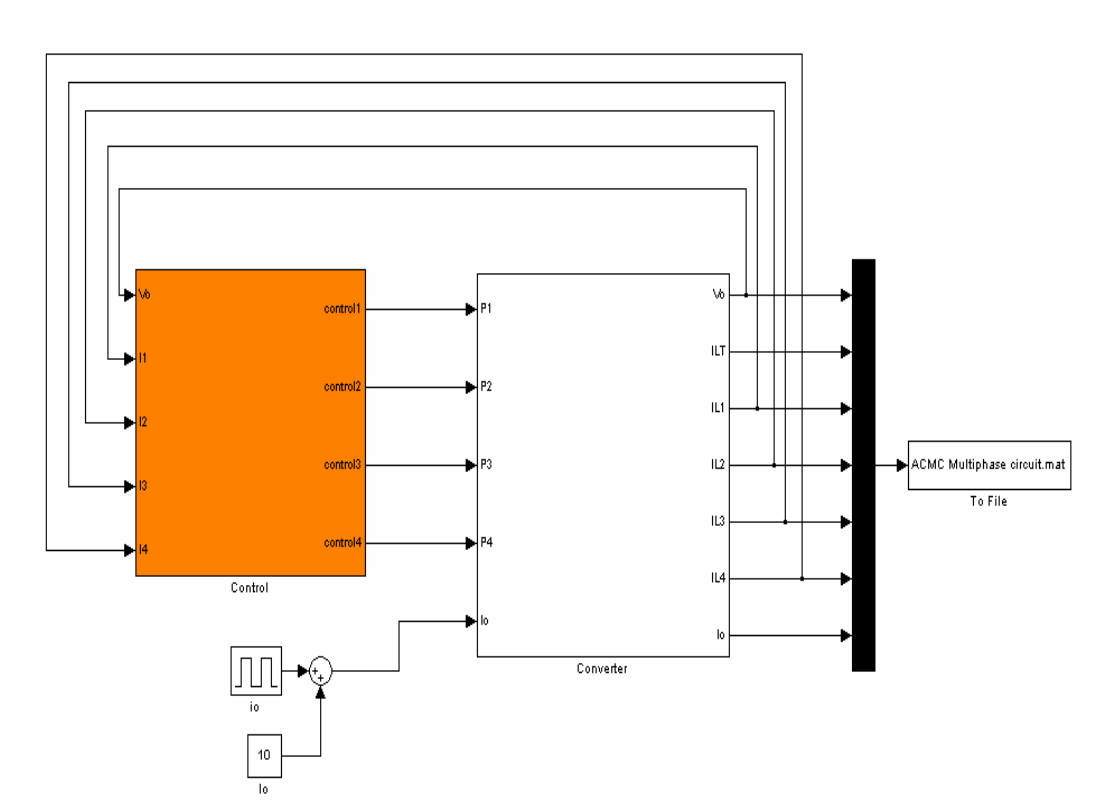

Fig. A.17 Overall simulation diagram used for ACMC in the multiphase converter

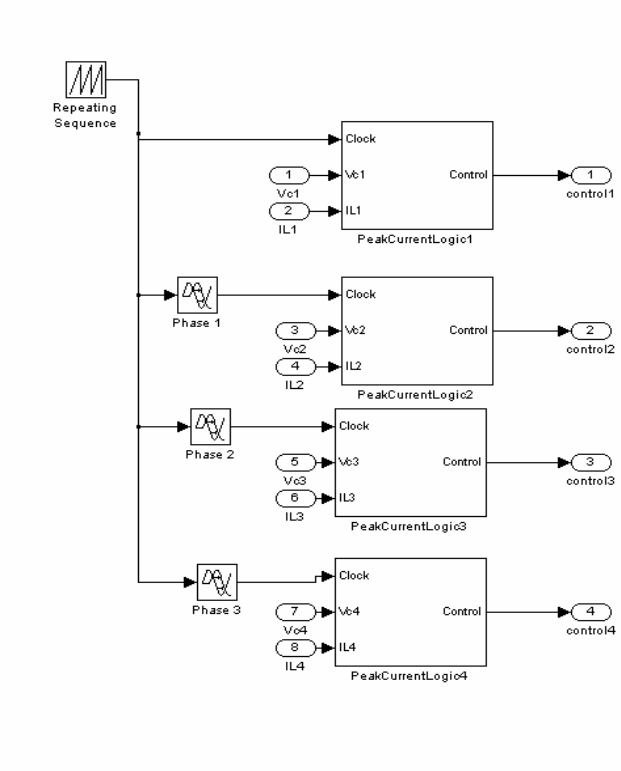

Fig. A.18 PCMC logic diagram used in the multiphase converter

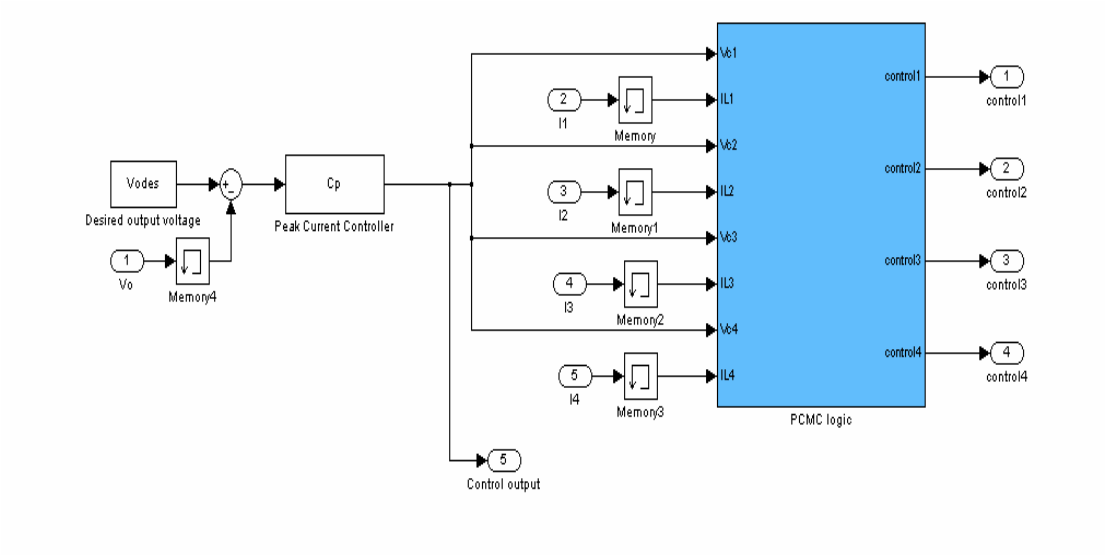

Fig. A.19 PCMC Control diagram used in the multiphase converter

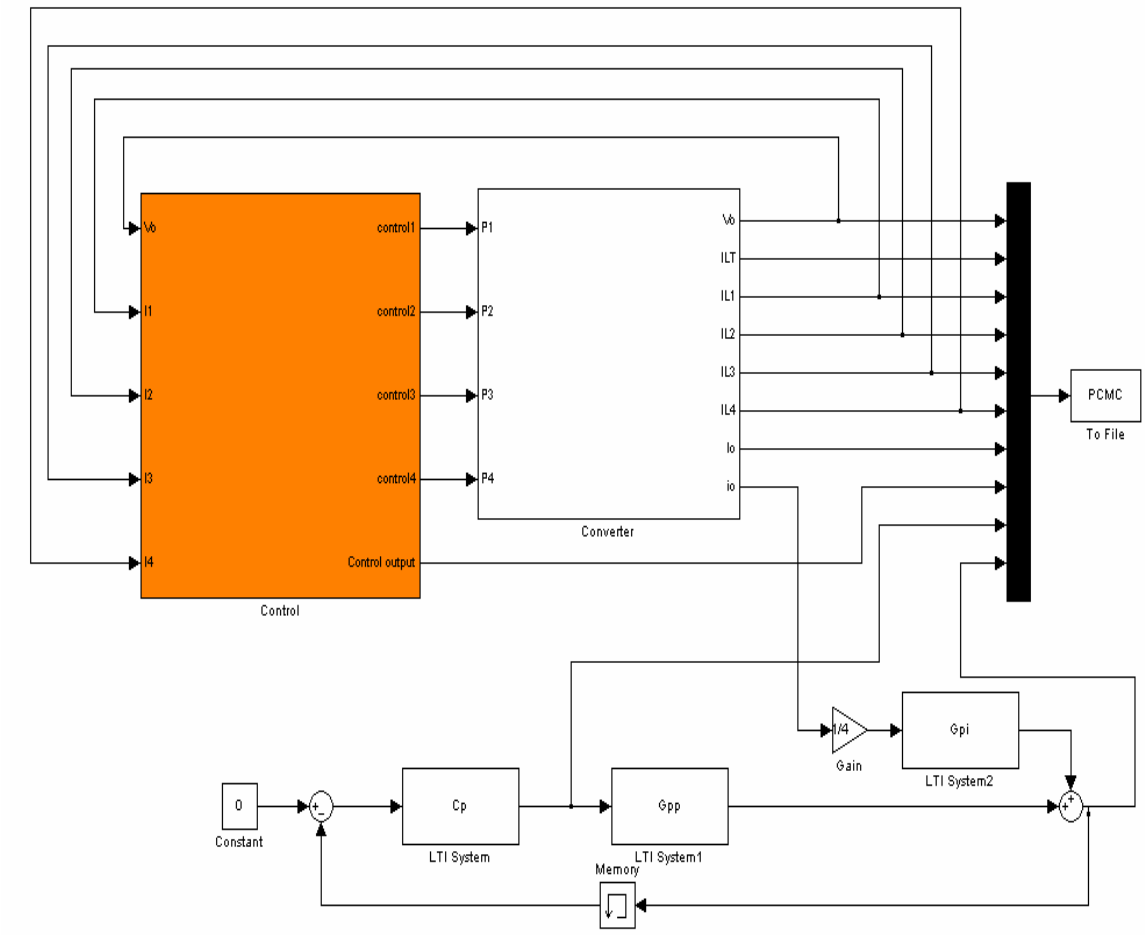

Fig. A.20 Overall simulation diagram used for PCMC in the multiphase converter

A.6 Switch current estimation circuit diagrams

The presence of the current transformer in the converter is simulated as shown in Fig.A.21. The proposed switch current estimation method using current transformer is also simulated using the circuit diagram shown in Fig. A.22.

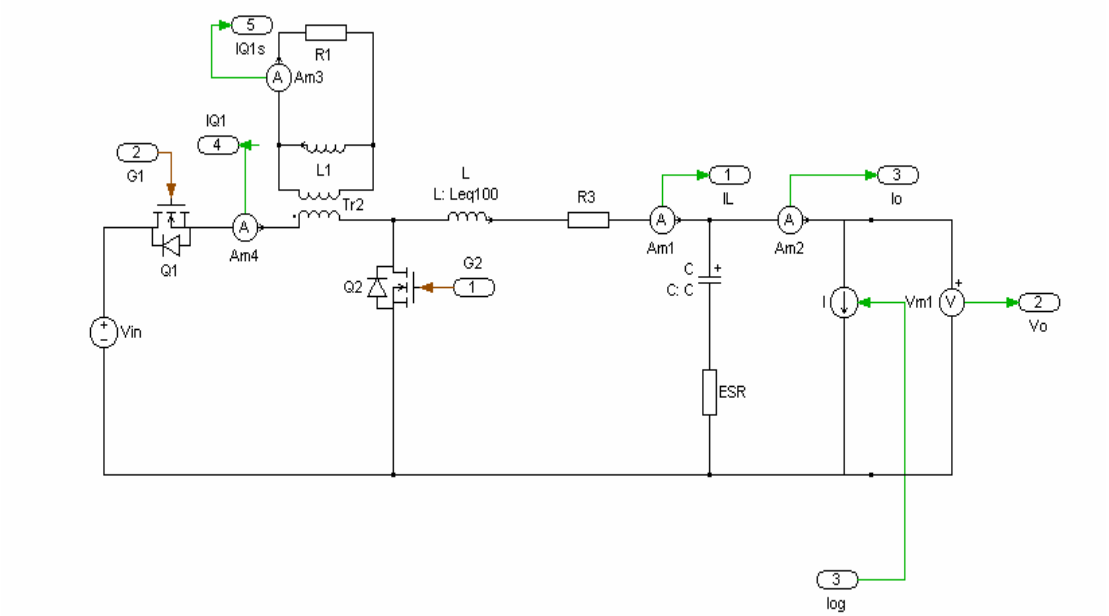

Fig. A.21 Single phase buck converter circuit with a CT in series with the high side switch.

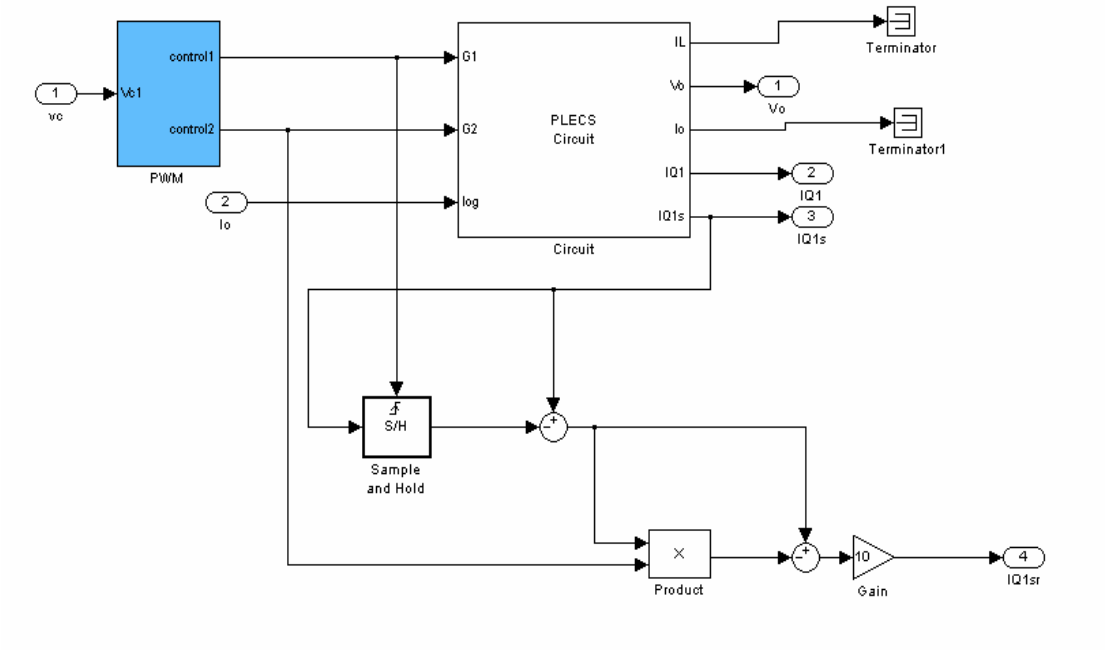

Fig. A.22 Switch current estimation circuit diagram

APPENDIX B

HARDWARE DETAILS

In this section, the various experimental circuits' details and photos are provided.

B.1 Inductor current estimating scheme

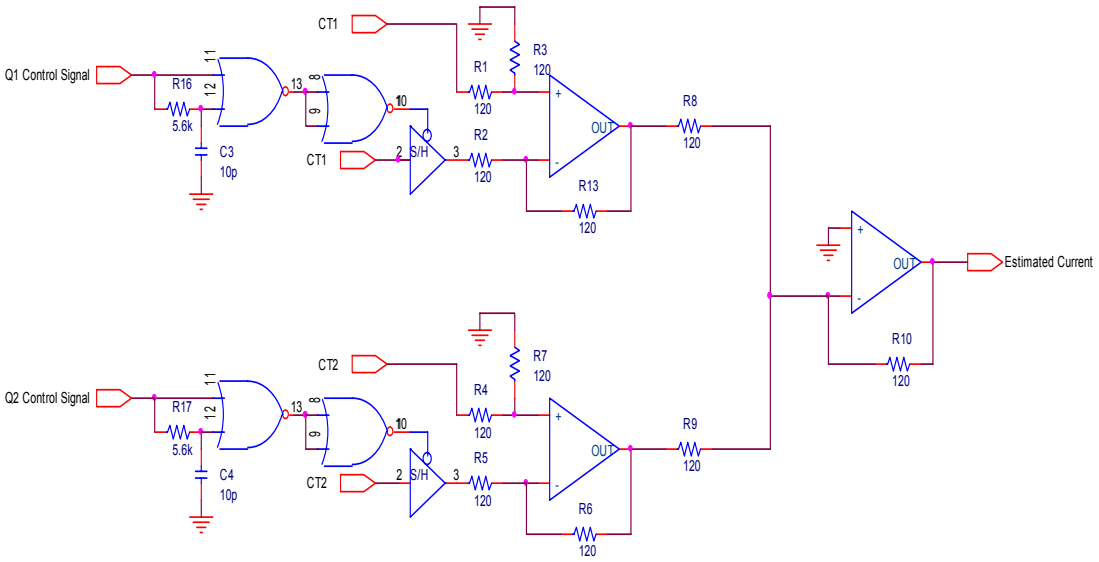

Fig. B.1 Inductor Current estimation circuit diagram

Note: Since the two CT ratios are the same in our experimental implementation, the gains of the two amplifiers have also been kept identical, in order to ensure the scale factors used in the two current sensing paths are the same. Besides, there is a small time delay between the switch control signal and the actual switching in the converter. In the experimental circuit, in order to compensate this delay, a time delay of same value is added in the control of the sample and hold IC, using some NOR switches, resistances and capacitors, as shown in Fig. B1.

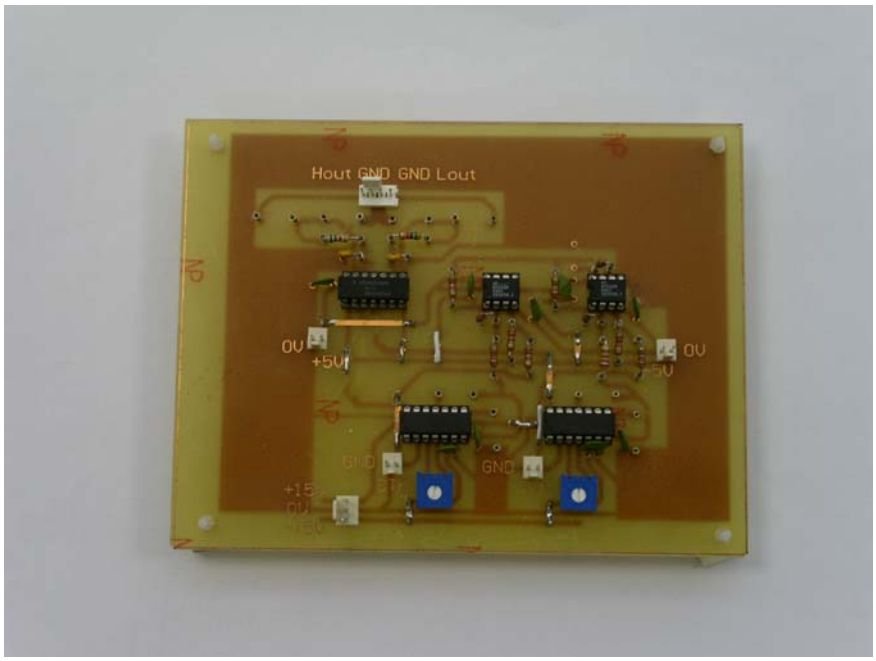

Fig. B. 2 Inductor current estimation PCB circuit

B.2 PCMC scheme using the proposed current sensing technique

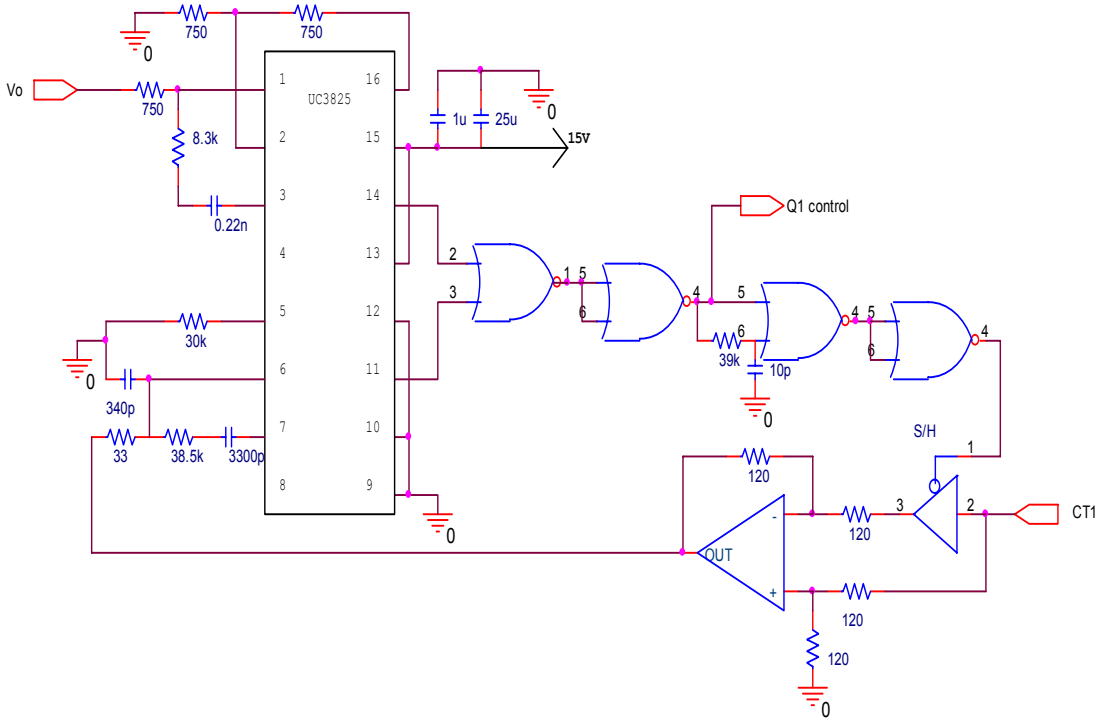

Fig. B.3 PCMC circuit diagram

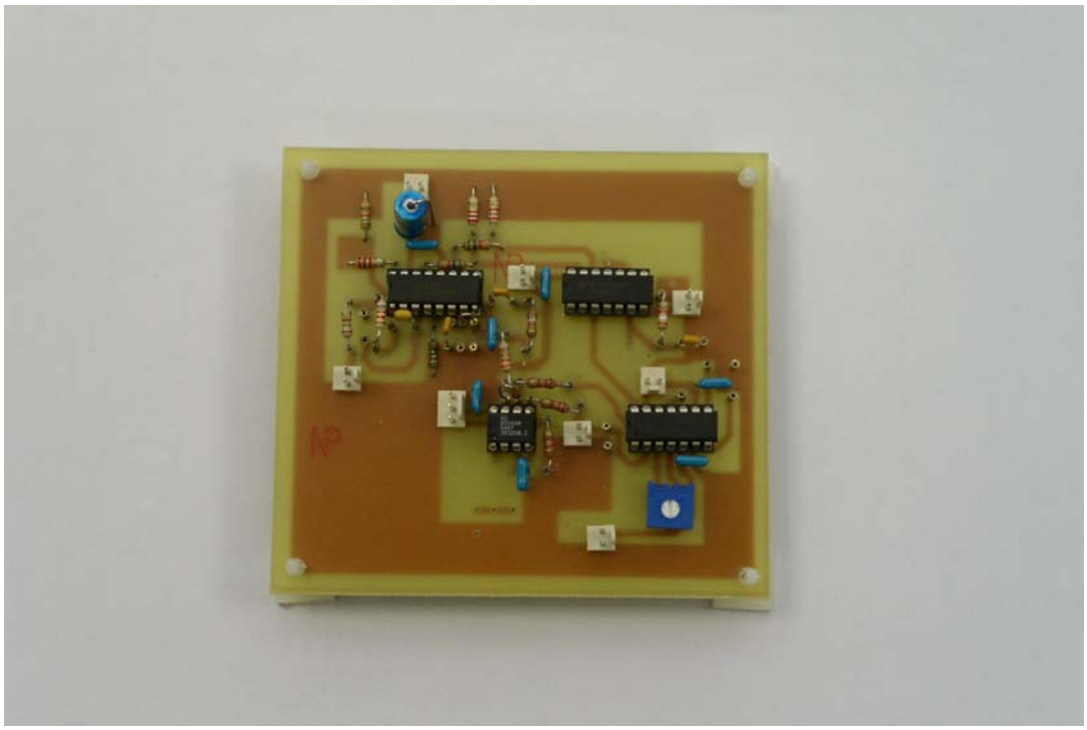

Fig. B.4 PCMC PCB circuit

B.3 Converter circuit

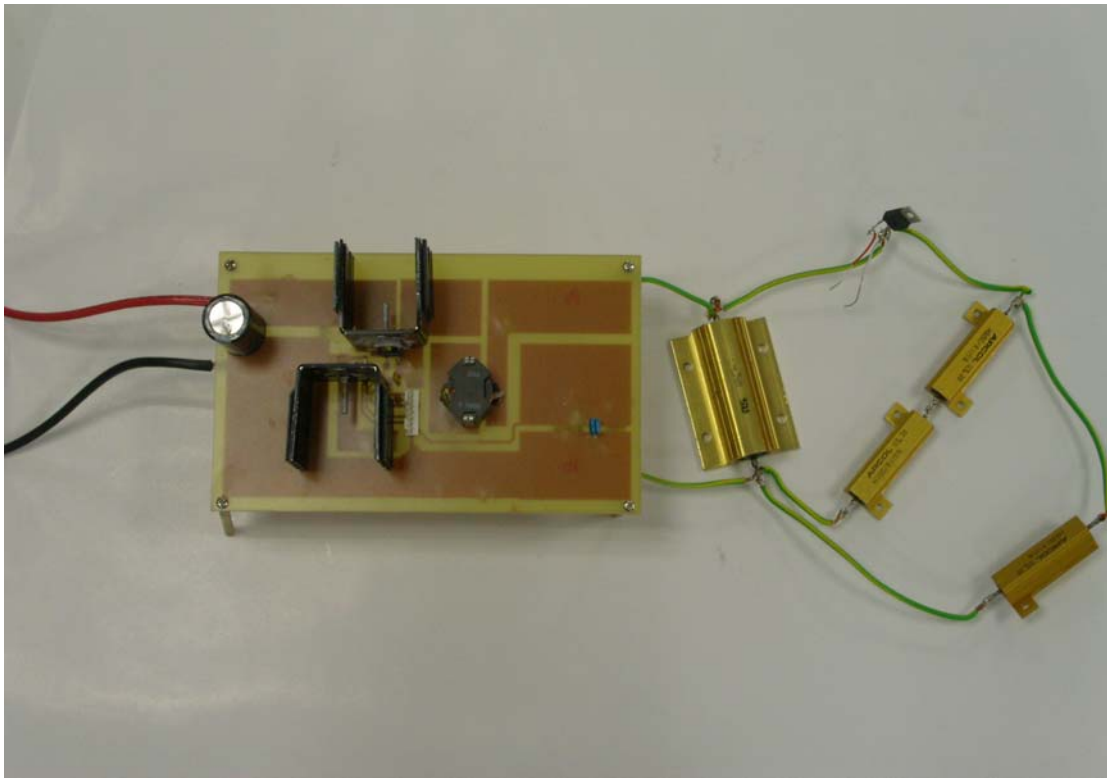

Fig. B.5 Single phase buck converter PCB circuit with load

Note: The MOSFETs are driven using the driver HIP6602B [78]. The output capacitor consists of five tantalum parallel capacitors of 100 μF each. The input capacitor is an electrolytic capacitor of 4700 μF in parallel with a 100 μF tantalum capacitor. The inductor is of 2.98 μH. Its ESR is estimated to 3.5 mΩ. The upper MOSFET is Harris Semiconductors' RFP70N03 [65]. The lower MOSFET is Infineon's SPP80N03S2L [66].

The CTs are placed at the downside of the PCB board (not shown in the picture). The CT core material is 3C90. For more information regarding this core characteristics, one may refer to [79]-[80].