GATE STACK ENGINEERING OF GERMANIUM MOSFETS WITH HIGH-K DIELECTRICS

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Summary

With the rapid development of modern semiconductor industry, metal-oxide-semiconductor field effect transistor (MOSFET) is approaching fundamental limits for Very Large Scale Integration (VLSI) applications. Germanium, for channel material combining with high-k gate dielectric, has become attractive to overcome the limits. However, development of germanium MOSFET is at the early stage with quite a number of challenges but limited knowledge. This dissertation mainly presents the development of gate stack formation technology on germanium with CVD hafnium dioxide (HfO_2) gate dielectric.

The general approach in this study is as follows: the new processes on germanium (Ge) substrate were first characterized by physical analyses; MOS capacitors and MOSFETs were then fabricated for electrical characterization.

Surface nitridation was first developed as a surface passivation technique on germanium to reduce the leakage current of the gate stack. However, it was found that interface trap density is very high for the device fabricated with the nitridation technique. Consequently, these traps have led to severe degradation of the channel mobility. To overcome the problem, a novel approach of silicon passivation by SiH_4 annealing was developed. The feasibility of the passivation technique was first studied, followed by electrical characterization. Results showed that, by introducing an ultra-thin Si layer, Si passivation is more reliable than the nitridation technique. It can yield lower interface states and much higher mobility, compared to the p-MOSFETs that

were fabricated in the same way. The optimal amount of silicon might be related the deposition technique and the deposition time of the subsequent high-k dielectrics. Further study showed that most of the interface traps might be located within the upper half of the germanium band gap, which could be a major factor that limits the electron mobility of the germanium n-MOSFETs. Subsequently, Ge n-MOSFET was fabricated successfully with electron mobility enhancement over the HfO_2/Si counterpart. Additional reduction of fixed oxide charge and hysteresis were also achieved.

Finally, the reliability issue of threshold voltage instability was also addressed qualitatively. Negative bias temperature instability (NBTI) is reduced in high-k/Ge p-MOSFETs, while positive bias temperature instability (PBTI) in high-k/Ge n-MOSFETs becomes a more serious reliability issue than its high-k/Si counterpart.

This study has set up a research framework for the development of germanium MOSFETs for VLSI applications. In conclusion, the leakage problem of gate stack technology on germanium has been solved. Germanium shows promising performance of MOSFET drive current with silicon passivation for future VLSI circuits.

List of Figures and Tables

List of Symbols

A	Area
k_B	Boltzmann's constant
$\hbar$	Modified Planck's constant
ε_0	Permittivity in vacuum
ε_{Si}	Permittivity of Si
ε_{Ge}	Permittivity of Ge
ε_{SiO2}	Permittivity of SiO_2
k_{Si}	Dielectric constant of Si (relative permittivity)
k_{Ge}	Dielectric constant of Ge (relative permittivity)
k_{SiO2}	Dielectric constant of SiO_2 (relative permittivity)
φ_S	Surface potential of semiconductor
μ_e	Mobility of electron
μ_h	Mobility of hole
μ_{eff}	Effective mobility
λ_0	Attenuation length of photo-electron within the overlayer originated from the overlayer
λ_S	Attenuation length of photo-electron within the overlayer originated from the substrate
Φ_M	Workfunction of metal
Φ_B	Electron barrier height from metal to oxide
θ	Take-off angle of the XPS analysis
χ	Electron affinity of a semiconductor
ψ_B	E_F-E_i
C_D	Depletion layer capacitance per unit area
C_{ox}	Oxide capacitance per unit area
C_{it}	Interface trap capacitance per unit area
C_{inv}	Gate to channel capacitance under inversion per unit area
C_S	Intensity of XPS spectrum in the substrate
C_0	Intensity of XPS spectrum in the overlayer

EOT	Equivalent oxide thickness
CET	Capacitive equivalent thickness
D_{it}	Interface trap (states) density per unit area, per unit energy
E_F	Fermi level of a semiconductor
E_i	Intrinsic fermi level of a semiconductor
E_C	Conduction band edge
E_v	Valence band edge
E_{ox}	Electric field in oxide
E_{eff}	Vertical effective electric field in a MOSFET channel
E_g	Energy band gap of a semiconductor
E_0	Kinetic energy of the photo-electron from the overlayer
E_S	Kinetic energy of the photo-electron from the substrate
ΔE_C	Conduction band offset between the semiconductor and the oxide
ΔE_v	Valence band offset between the semiconductor and the oxide
g_m	Transconductance of a MOSFET (I_d with respect to V_g)
I_g	Leakage current through gate electrode
I_d	Current through the drain
I_s	Current through the source
I_{on}	Channel saturation current when the MOSFET is on
I_{off}	Drain leakage (sub-threshold) when the MOSFET is off
I_{CP}	Charge pumping current
J	Current density
L	Gate length of a MOSFET
m^*	Effective electron mass
n_i	Intrinsic carrier concentration in a semiconductor
q	Electronic charge
Q_{inv}	Inversion charge in the channel per unit area
Q_B	Depletion charge in the bulk per unit area
Q_f	Fixed oxide charge per unit area
R_{SD}	Source/drain resistance
SS	Sub-threshold swing (mV/dec)
S_0	Sensitivity factor of the photo-electron from the overlayer
S_S	Sensitivity factor of the photo-electron from the substrate
t_{inv}	Equivalent oxide thickness (electrical) in inversion
t_{poly}	Equivalent oxide thickness (electrical) due to poly depletion effect

t_{qm}	Equivalent oxide thickness (electrical) due to quantum mechanics in the channel
t_{ox}	Physical oxide thickness
V_{dd}	Supply voltage to drain
V_{dsat}	Drain saturation voltage
V_{ds}	Drain-source bias
V_{th}	Threshold voltage
V_g	Gate voltage
V_{gs}	Voltage from gate to source
V_{gb}	Voltage from gate to bulk
V_{ox}	Voltage dropped on the oxide
V_{fb}	Flat-band voltage
$V_{Si/Ge}$	CVD deposition rate of silicon on germanium surface
$V_{Si/Si}$	CVD deposition rate of silicon on silicon surface
W	Gate width of a MOSFET

Chapter 1

Introduction

Inside an integrated circuit (IC) nowadays, metal-oxide-semiconductor field effect transistors (MOSFET) are the majority components. Their performance is a key factor for the whole circuit performance. Thus, intensive study has been carried out to improve the MOSFET performance for the last four decades. In addition, the technology roadmap for the improvement of MOSEFT in the next 15 years is well planned.

1.1 Approaches to improve MOSFET performance

A MOSFET is a switch in digital circuits (Figure 1.1), which is controlled by its gate (G) terminal. Carriers (electrons or holes) flow from source (S) to drain (D) in the semiconductor channel, forming an on-current (I_{on}) when the device is in the on-state, and an off-current (I_{off}) when the device is in the off-state. A larger output current (I_{on}) will result in faster charging of the capacitive load, and a consequent higher switching speed. Therefore, it has been one of the main objectives to increase the MOSFET output current in recent research activities. Figure 1.2 summarizes I_{on} versus I_{off} for high-performance (HP) logic and low operating power (LOP) applications that are targeted in the international technology roadmap of semiconductor (ITRS) 2004 [1.1]. It can be clearly seen that the output current (I_{on}) needs to be increased continuously every year, especially for HP applications (144% improvement from year 2005 to year 2011).

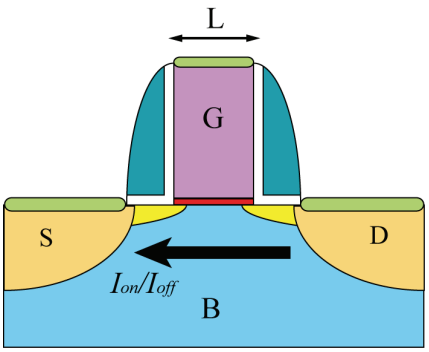

Figure 1.1 A typical MOSFET structure in modern VLSI circuits. L represents the gate length. The current between the source (S) and the drain (D) through the channel is controlled by the gate (G). When a voltage is applied to the gate, carriers can flow from the source to the drain and forms the on current (I_{on}).

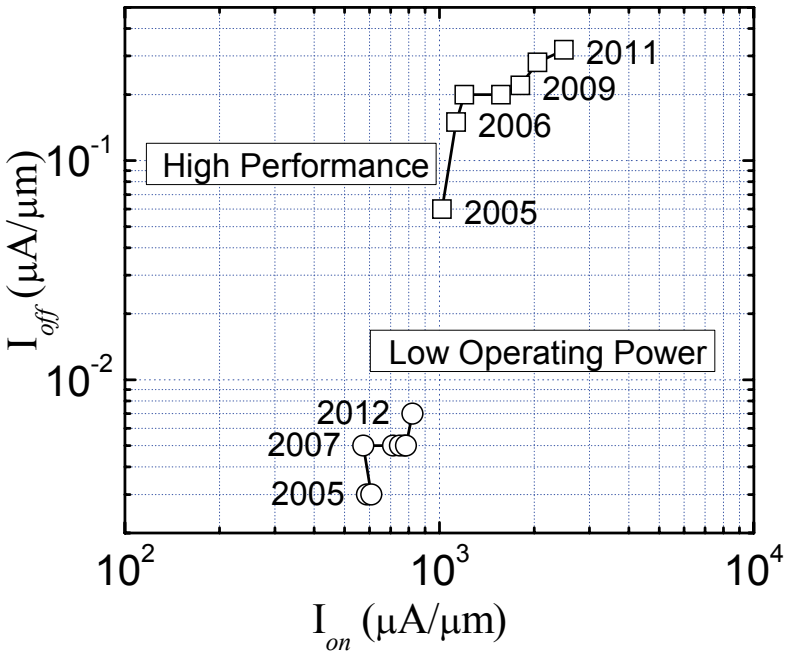

Figure 1.2 I_{on}-I_{off} requirements from Year 2005 to Year 2012 in ITRS [1.1]. There is a substantial demand to increase the on-state current while keeping the off-state current low for High performance logic applications and for Low Operating Power applications.

The possible approaches for performance improvement associated with a long-channel MOSFET can be seen by considering a simple equation describing the MOSFET drive current (I_d) working in the saturation region:

$$I_{d,sat} = \frac{W}{2L}\mu_{eff} C_{inv}(V_g - V_{th})^2 \quad (1.1)$$

where W is the width of the transistor channel, L is the channel length, μ_{eff} is the channel carrier mobility, C_{inv} is the capacitance density associated with the gate dielectric when the underlying channel is in the inversion condition, V_g and V_{th} are the voltage applied to the gate electrode and the MOSFET threshold voltage, respectively. In order to increase $I_{d,sat}$ under a given power supply voltage (which means the maximum V_G is fixed), there are five approaches to increase I_d : (1) to increase W; (2) to decrease V_{th}; (3) to decrease L; (4) to increase C_{inv}; (5) to increase μ_{eff}. Approach (1) is not a good approach because it increases the chip size, which increases the cost per chip. Approach (2) is not a straightforward approach because it increases I_{off} and the consequent power consumption of the circuit simultaneously. Therefore, it requires trade-off between I_{on} and I_{off}. Approach (3) is to scale down the MOSFET size. This approach has been adopted by industry for many years, because it also reduces the circuit area as well. However, simple scaling of gate length would lead to the undesired short channel effects, which limits the improvement due to gate length scaling. Velocity saturation is also another limiting factor. The result is that the output current does not increase proportionally. The remaining approaches, (4) and (5), have led to research topics that have received tremendous attention recently. They are also the motivation for this research. While C_{inv} in Approach (4) will be discussed later in Section **1.3**, we will focus on μ_{eff} in Approach (5) first in Section **1.2**.

1.2 Germanium for mobility enhancement

Table 1.1 Long-Term Requirements of High-performance Logic Technology in ITRS [1.1]

Year of Production	**2010**	**2013**	**2016**
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Capacitive equivalent oxide thickness* (nm)	1.1	1	0.9
Nominal power supply voltage (V_{dd}) (V)	1.0	0.9	0.8
Nominal high-performance NMOS sub threshold leakage current, $I_{sd,leak}$ (at 25° C) (μA/μm)	0.1	0.3	0.5
Nominal high-performance NMOS saturation drive current , $I_{d,sat}$ (at V_{dd}, at 25° C) (μA/μm)	1900	2050	2400
Required percent current-drive "mobility/transconductance improvement"	100%	100%	100%
Static power dissipation (NMOSFET) due to drain and gate leakage (W/μ)	1.1e-6	2.97e-6	4.4e-6

Legend:

Manufacturable Solutions Exist, and Are Being Optimized:

Manufacturable Solutions are Not Known:

Since carrier mobility is a material property, Approach (5) requires considering a different channel material other than ordinary silicon. To be quantitatively, Table 1.1 shows some performance parameters that are required in the long term for HP logic [1.1]. When the gate length is scaled from 25 nm (Year 2010) to 13 nm (Year 2016), the capacitive equivalent oxide thickness is planned to scale from 1.1 nm to 0.9 nm. Theoretically this should lead to ~122% improvement of saturation drive current ($I_{d,sat}$). However, the saturation drive current is required to improve more than that even with scaling of power supply voltage, reaching 2400 μA/μm in Year 2016. The solution is to enhance the mobility/transconductance. According to the roadmap, mobility should be enhanced by 100% starting from the year of 2010. In other words, μ_{eff} in Eq. (1.1) must double. Since this μ_{eff} is usually an intrinsic material property, changing the channel material (silicon) must be considered to overcome the challenge.

* Capacitive equivalent oxide thickness, CET=$k_{SiO2}\varepsilon_0/C_{inv}$.

Germanium is one of the candidates for replacing silicon because it can offer double the electron mobility and triple the hole mobility. Although historically it was the first semiconductor that was widely studied, the development of MOSFET fabricated on germanium substrate was hampered for decades because of the lack of a stable native oxide in contrast to its counterpart silicon, which has silicon oxide. Recent development of high-*k* dielectric technology has provided some potential technology solution for germanium MOSFET because one no longer needs to use the substrate native oxide for the gate dielectric.

In addition, germanium has been used for making optical devices. However these devices have never been integrated into VLSI systems. Hence, it is also an attractive possibility to implement germanium in VLSI so that optical devices can also be integrated together. This approach can improve the functionality of an IC.

This section would give a general evaluation of germanium for modern MOSFET technology.

Table 1.2 A comparison of some basic material properties between germanium and silicon **Error! Reference source not found.**

Item	Si	Ge
Electron Affinity (eV)	4.05	4.13
Bandgap (eV)	1.12	0.66
n_i (cm^{-3})	$1.5x10^{10}$	$2.4x10^{13}$
Dielectric Constant	11.9	16
Mobility (e) ($cm^2/v*s$)	1350	3900
Mobility (h) ($cm^2/v*s$)	500	1900
Melt point (ºC)	1420	941
Native oxide quality	Good	Bad

1.2.1 Basic material properties

Silicon has been the substrate for VLSI circuits for four decades. Changing the substrate material from silicon to germanium will be a great challenge for the whole industry. Research on germanium has to start from the very beginning - basic comparison of material properties.

Table 1.2 shows a basic comparison of material properties between germanium and silicon. The electron affinity of germanium and silicon are similar. The band gap energy of germanium is about half of that of silicon. This has led to 3 orders of magnitude difference in intrinsic carrier concentration (n_i) between germanium (Ge) and silicon. As a result, the leakage current of a Ge pn junction is much larger than that of silicon. At the same time, it should be noticed that germanium has a larger dielectric constant than silicon. This may result in less channel potential controllability by the gate and more serious short channel effects. Therefore, there may be issues to be solved if Ge MOSFET is implemented in VLSI circuits. Nevertheless, despite the above drawbacks, the most attractive property of germanium is its carrier mobility. Both electron and hole mobilities of germanium surpass those of silicon by ~2 and ~3 times, respectively. On the other hand, in terms of difficulty of integrating germanium into the VLSI process, the true challenge is associated with the native oxide and the low melting point of germanium, which will be discussed in detail below.

1.2.2 Challenges with fabrication of MOSFETs on germanium

With the basic comparison of the above material properties between germanium and silicon, the challenges associated with the MOSFET fabrication on germanium substrate can be summarized in the following aspects.

a. Germanium oxide

The first and the biggest challenge for germanium arises from its native oxide which has much poorer properties than its counterpart – silicon oxide. Germanium oxide is found to be water soluble. It decomposes at a relatively low temperature (~400ºC), which makes it unsuitable for the modern VLSI industry. Moreover, while thermal oxidation of silicon crystal can produce SiO_2 film with excellent quality, germanium oxide obtained by a similar method is found to be rough with a poor surface morphology, poly-crystalline, and with poor insulating property that is not suitable for a MOSFET dielectric [1.3]. Tabet *et al.* also reported on the presence of high density of electron states at the oxide/germanium interface [1.4]. Therefore, it is possibly better to use other insulators that are deposited instead of thermally grown.

b. Junction

To fabricate MOSFETs on germanium substrate, both n+/p and p+/n junctions has to be formed on p- and n- type substrates for source and drain. While junction formation technology on silicon is well known, it remains relatively un-developed on germanium. Historically, pn junctions in germanium were fabricated by diffusion. However, it is not suitable for modern MOSFET in VLSI, because it is difficult to achieve shallow junction (<20nm for drain extension depth X_j) by diffusion. In this study, we will use implantation of boron and phosphorus followed by RTA to form n+/p and p+/n junctions. Therefore, it would be necessary to explore recipes for implantation and activation annealing.

c. Process integration

In this study, all the experiments will be conducted on germanium substrate. This means that the fabrication flow should be germanium compatible. As mentioned in Table 1.2, germanium has a much lower melting temperature than silicon. Hence

processes should be carefully selected so that they are well below the Ge melting point. Moreover, the chemical property of germanium is also very different from silicon. Chemicals should also be carefully selected for germanium processes. For instance, germanium can be easily oxidized, and germanium oxide is water-soluble. Therefore, any strong oxidizing solution such as SC1 ($NH_4OH+H_2O_2+H_2O$), HNO_3+H_2O, etc. with water would attack germanium. Hence, germanium is incompatible with the standard CMOS process flow.

1.3 High-k gate dielectrics for gate oxide scaling

This section will continue to discuss Approach (4), which is to increase C_{inv}. Since,

$$C_{inv} = \frac{k_{SiO2}\varepsilon_0}{t_{inv}}, \tag{1.2}$$

where k_{SiO2} is the relative permittivity of silicon oxide ($k_{SiO2}=3.9$), ε_0 is the permittivity of free space, t_{inv} is the capacitive equivalent oxide thickness (CET) of the gate oxide. A detailed analysis of t_{inv} reveals that t_{inv} has three components:

$$t_{inv}=t_{poly}+t_{ox}+t_{qm} \tag{1.3}$$

t_{poly} is the thickness contributed by poly depletion effect in small devices, t_{ox} is the equivalent oxide thickness (EOT) of the gate dielectric*, and t_{qm} is the capacitive thickness attributed to the quantum mechanical effect of the carriers in the channel. Decreasing any of the components can help to increase C_{inv}. Efforts to reduce t_{poly} have triggered the recent study on metal gate technology, which is not the focus of this study. t_{qm} is an intrinsic mechanism that cannot be eliminated. Thus, it is a practical approach to reduce the gate oxide thickness (t_{ox}).

* $t_{ox}=t_{high\text{-}k}*k_{SiO2}/k_{high\text{-}k}$, where $t_{high\text{-}k}$ and $k_{high\text{-}k}$ are the physical thickness and the effective relative permittivity of the high-k dielectric,

It should be noted that the gate oxide thickness is actually the smallest dimension parameter in a MOSFET. Figure 1.3 summarizes the physical gate length and the gate dielectric thickness (SiO_2) of the MOSFET at each technology generation over the last four decades. The physical gate oxide thickness has also been scaled with the gate length and remains around ~100 times smaller than the gate length in order to maintain the proper function of a MOSFET. It is obvious that the gate oxide thickness would be the first parameter to reach the physical limitation of below 1 nm due to the unacceptably high leakage through the gate oxide in the near future. This limit will be reached in the coming generation of MOSFETs (45 nm technology node).

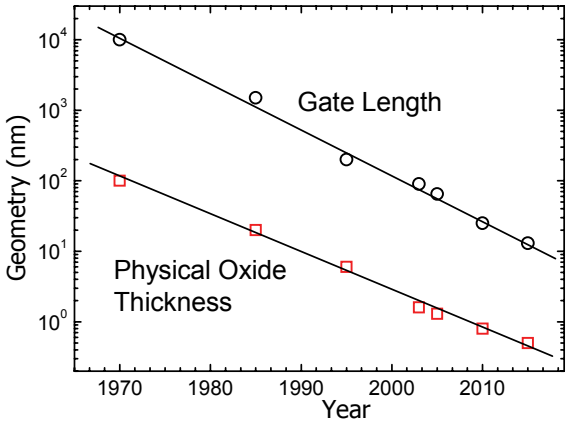

Figure 1.3 Scaling trend of gate length and physical oxide thickness of the gate dielectric since 1970's. [1.1]

Table 1.3 shows more complete gate stack related technology requirements for high-performance logic applications from the International Technology Roadmap for Semiconductors (ITRS) 2004 [1.1]. Besides the mobility enhancement as discussed in the previous section, it is expected that the physical oxide thickness will reach 0.9 nm in the year of 2007. However, the physical thickness of the conventional gate dielectric cannot be scaled down infinitely. When this gate dielectric (SiO_2) approaches and becomes smaller than ~2 nm, the gate leakage current starts to increase dramatically due to direct tunneling of the carriers through the gate oxide (Figure 1.4), ruining the

Table 1.3 Near-Term Requirements of High-performance Logic Technology in ITRS [1.1]

Year of Production	**2005**	**2006**	**2007**	**2008**	**2009**
MPU Printed Gate Length (nm)	45	40	35	32	28
MPU Physical Gate Length (nm)	32	28	25	22	20
EOT: equivalent oxide thickness (physical) for high-performance (nm)	1.1	1.0	0.9	0.8	0.8
Gate depletion and quantum effects electrical thickness adjustment factor (nm)	0.7	0.7	0.4	0.4	0.4
Equivalent oxide thickness (electrical) (nm)	1.8	1.7	1.3	1.2	1.2
Nominal power supply voltage (V_{dd}) (V)	1.1	1.1	1.1	1.0	1.0
Nominal gate leakage current density limit (at 25ºC) (A/cm^2)	5.2e+2	6.0e+2	9.3e+2	1.1e+3	1.2e+3
Required percent current-drive "mobility/transconductance improvement"	30%	40%	100%	100%	100%
Static power dissipation per NMOSFET (Watts/ µm)	6.05e-7	6.05e-7	8.37e-7	7.7e-7	7.7e-7

Legend:

Manufacturable Solutions Exist, and Are Being Optimized:
Manufacturable Solutions are Known :
Manufacturable Solutions are Not Known:

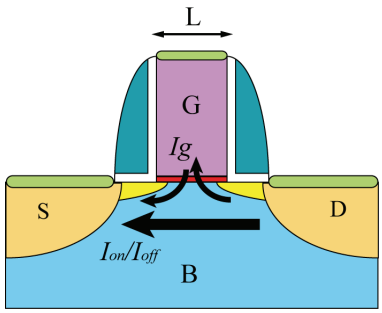

Figure 1.4 A typical MOSFET structure in the modern VLSI circuits. If the gate leakage current (I_g) becomes too high due to the direct tunneling through the gate oxide, the power consumption increases substantially. In extreme case, the MOSFET will not be functioning properly.

normal operation of a MOSFET and increasing the power consumption of the whole IC dramatically [1.5]. As can be seen in Table 1.3, the nominal gate leakage current density needs to be controlled to or below 9.3x10^2 A/cm^2 at the year of 2007 in order to maintain the static power dissipation. But the way to achieve this target is unknown. Therefore, this issue is more urgent than the mobility enhancement. One has to find an alternative way to increase C_{inv}. From Eq. (1.2) and (1.3), a practical choice would be

to use other dielectrics that have a higher dielectric constant (k) than that of SiO_2 (high-k gate dielectrics), which are generally metal oxides. Intensive research has therefore been carried out to study these materials for MOSFET applications.

1.3.1 Material selection criteria

There are a wide range of materials with higher dielectric constants than that of silicon dioxide. An appropriate high-k material for gate dielectric application should meet the following criteria.

a. Thermal stability with substrate

For all thin high-k dielectrics, the first criterion is that they must be thermodynamically stable on the substrate during CMOS processing. This is because the interface of the high-k material with the substrate plays a critical role, and in most of the cases, is the dominant factor in determining the overall electrical properties. In most of the recent studies, most of the high-k metal oxides have unstable interface with Si. They react with Si at an elevated temperature during either deposition or post deposition processes such as post deposition anneal, source/drain activation anneal to form an undesirable interfacial layer (IL). This not only reduces the advantage of the high k value since most of the interfacial layers have a lower k value, but also brings in the concerns on quality, uniformity and reliability issues, etc.

b. Permittivity and energy barrier

Selecting the right insulating material with a higher dielectric constant than that of SiO_2 (k=3.9) is clearly essential for gate dielectric application. However, the required permittivity must be balanced against the energy barrier height for the carrier tunneling process between the gate and the substrate. For electrons traveling from the

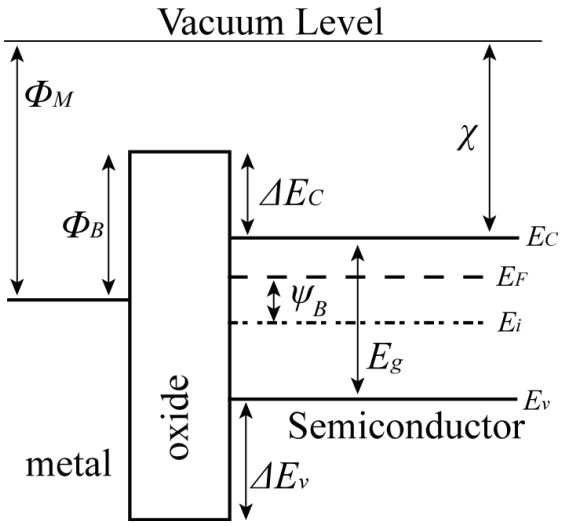

Figure 1.5 Energy band diagram of a MOS structure in flatband condition. Φ_M, workfunction of metal; Φ_B electron barrier height from metal to oxide; ΔE_C and ΔE_V, conduction band offset and valence band offset between semiconductor and oxide; E_g, bangap; χ, electron affinity of semiconductor; E_F and E_i, Fermi level and intrinsic Fermi level; $\psi_B = E_F - E_i$.

Si substrate to the gate, this is the conduction band offset, $\Delta E_C \approx q[\chi - (\Phi_M - \Phi_B)]$; for electrons traveling from the gate to the Si substrate, this is Φ_B (shown in Figure 1.5). For instance, when the oxide is thin and direct tunneling is the dominant mechanism (a common case in today's VLSI technology), the current from the gate to the substrate can be described as:

$$J = \frac{C}{t_{ox}^2} \exp\left[-2t_{ox} \sqrt{\frac{2m^* q}{\hbar^2}\left(\Phi_B - \frac{V_{ox}}{2}\right)} \right] \tag{1.4}$$

where C is a constant, $\hbar$ is the modified Planck's constant, q is the electronic charge, t_{ox} is the physical thickness of the gate oxide, V_{ox} is the voltage drop across the dielectric, and m^* is the electron effective mass in the gate oxide. As can be seen, the tunneling current increases exponentially with decreasing the barrier height and/or the gate oxide thickness. The decrease of Φ_B can easily become a factor that is as important as the decreased t_{ox}. Therefore, there is usually a trade-off in a high-k material between the barrier height and the dielectric constant. Yeo *et al.* has proposed

to use a figure-of-merit to compare the relative advantages of various gate dielectrics based on the composite effect of k, m^*, and Φ_B [1.6]. Figure 1.6 shows the band offset of a number of high-k materials [1.7]. Based on Yeo's discussion, high-k gate dielectric would be first used for low standby power application. HfO_2 is the first binary high-k material to be used.

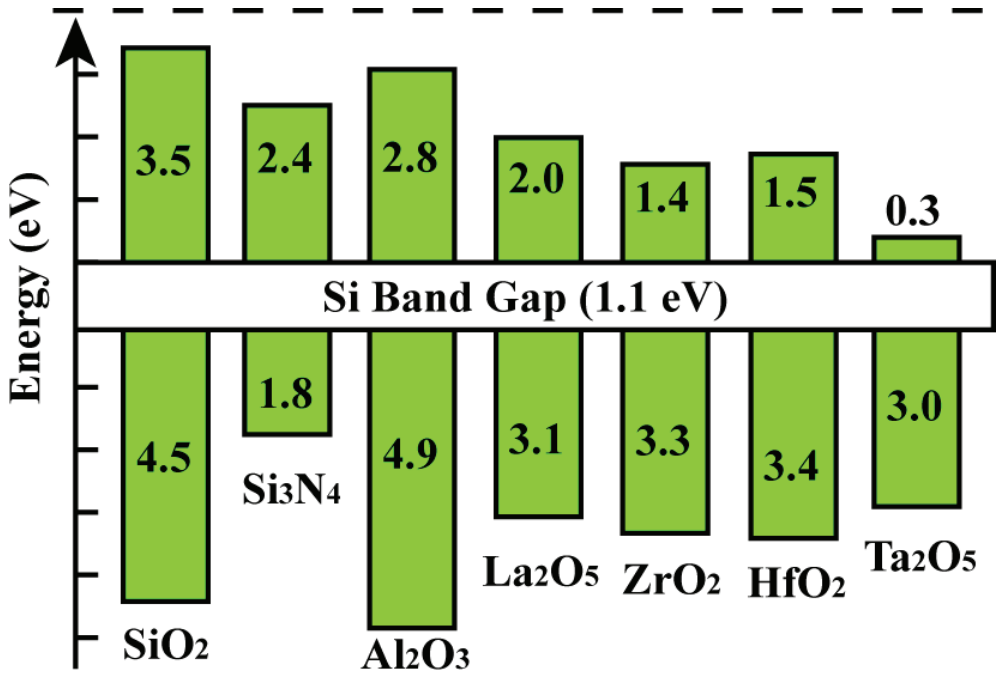

Figure 1.6 Bandgaps of selected high-k dielectrics [1.7]. The conduction band offset and valence band offset with respect to the Si band gap are also included, and compared to that of silicon oxide (SiO_2).

c. Thin film technology

Selecting a suitable high-k material should be based on the facilities that are available currently in the laboratory. There are two kinds of film formation technologies, physical vapor deposition (PVD) and chemical vapor deposition (CVD). Both deposition technologies can be used for high-k film formation.

Physical vapor deposition (PVD) includes evaporation and sputtering. In the evaporation method, a film is deposited by condensation of the vapor on a substrate, which is maintained at a lower temperature than that of the vapor. Evaporation can deposit a large variety of metals because all metals vaporize when heated to

sufficiently high temperatures. This is very helpful for studying various high-k dielectrics in a laboratory environment. A second advantage of evaporation is that an alloy or mixture of two or more materials can be deposited by the use of two or more independently controlled evaporation sources. The individual component evaporation rates are determined independently under experimental conditions. However, there are also disadvantages with evaporation for transistor fabrication: (1) since pure metal is evaporated on the substrate surface, a post-deposition oxidation is necessary to convert the metal film into a metal oxide film. This requires a very precise control of the oxidation process right to the semiconductor surface with the high-k film thickness less than 10 nm. If the oxidation is incomplete and there is metal remaining at the semiconductor surface, the transistor will not function at all; on the other hand, if the oxidation is excessive, the semiconductor starts to be oxidized and a low-k film (SiO_2) forms; the advantage of the high-k film can be easily ruined. (2) Good calibration is needed in order to maintain uniformity and repeatability during a run and from run to run. Hence, it is usually difficult to control the formation of a thin oxide film (for gate oxide application) using the evaporation technique.

In sputter deposition, the target material is bombarded by energetic ions (usually Ar) to release target atoms. These atoms are then condensed on the substrate to form a film. Sputtering can be more well controlled than evaporation, and is generally applicable to an even larger variety of materials, including metals, alloys, semiconductors, and insulators. Compound films can be formed in many ways. Metal oxide films can be sputtered using a metal oxide target, or reactively by a pure metal target with O_2 flow, or formed in a similar way to that of evaporation – pure metal first and then oxidation. Alloy-film can be achieved using a composite metal target, or by co-sputtering of individual targets. Nitrogen (N_2) can also be incorporated into the film

by having N_2 gas in the sputtering chamber. Hence, this is generally an easy way to deposit and study different materials for gate dielectric application. However, there are also disadvantages and limitations in sputtering: (1) sputtering is very sensitive to machine configuration and condition. The deposition rate for thin film application may vary easily from run to run. This brings additional process difficulties in the experiment setup. (2) Sputtering is usually carried out at a relatively higher pressure than evaporation in order to create enough gas (Ar) ions for bombardment. As a result, the films usually end up including small amount of the gas and other impurities. The trapped gas may cause stress changes and/or reliability concerns of the gate dielectrics. (3) Sputtering is a physical process which involves plasma. The ions can cause sputtering damage, which leads to unwanted charges and internal electric fields that affect device properties. For the latter two reasons, a post deposition anneal is usually necessary for reparation of defects in the film. This brings in additional experimental factors, and hence, increases the process complexity.

Chemical vapor deposition (CVD) forms a nonvolatile solid film on a substrate by reaction of vapor-phase chemicals (reactants) that contain the require constituents. The chemical reaction occurs near or on the substrate surface, and the reaction products (except the solid film) are also gaseous which can be pumped away easily. Further, it usually takes place at elevated temperature and reduced pressure for a surface-reaction-controlled process window. Thus in contrast to PVD, CVD has good process controllability for deposition rate, uniformity, repeatability, purity, etc. Moreover, it is also damage free since no plasma is involved. These advantages make CVD very suitable in the mass production of transistors.

There are currently two kinds of CVD technology for high-k film formation, atomic layer deposition (ALD) and metal-organic chemical vapor deposition

(MOCVD). The first one utilizes a self-saturating process in which the precursor reacts chemically with the sample surface. As the process is self-saturating, only one monolayer is deposited. A bulk film is then deposited by alternating injection of two precursors into the reaction chamber divided by purge process. MOCVD utilizes a metal-organic molecule as the carrier for large metal atoms. These metal-organic compounds are generally liquids. They can be injected into the reaction chamber by a bubbler technique or by vaporization technique.

Although CVD has many advantages, it also has several disadvantages. First of all, CVD is not suitable for experiments that need frequent changing of the deposition materials, since it depends on the availability of the chemical precursors. Another disadvantage is that an interfacial layer would easily grow between the high-k and the substrate (Si). This is because any CVD techniques of interest typically operate under non-equilibrium conditions, and they need to use precursors that contain oxygen to form the metal oxide. For ALD, it is H_2O; and for MOCVD, oxygen is usually in the metal-organic precursor or intentionally introduced into the reaction chamber. The interfacial layer issue would be discussed later.

1.3.2 Possible candidates of high-k materials

Research on high-*k* gate dielectrics have been ongoing, focusing on several appropriate materials which included silicon oxynitride (SiO_xN_y) and *Group IIIA*, *IIIB* and *IVB* metal oxides [1.8].

SiO_xN_y provides a slightly higher *k* value than SiO_2 due to the presence of nitrogen (pure Si_3N_4 has a *k* of ~7), for slightly reduced gate leakage [1.9]. However, this slightly higher *k* value actually still cannot meet the requirements for rapide scaling of MOSFET.

Among group *IIIA* candidate dielectrics, aluminum oxide (Al_2O_3) is a very stable and robust material. It has a dielectric constant of ~8-10, and makes it a relatively short-term solution for industry. Much research has been done on this material. Gusev *et al.* studied thin Al_2O_3 films deposited by atomic layer chemical vapor deposition (ALCVD) at temperatures below 400 ºC [1.10]. The study has been focused on the control of the interfacial layer. Transistor results for a physical thickness of 21Å of Al_2O_3 have been achieved by Chin *et al.* [1.11] with an equivalent oxide thickness (EOT) of 9.6Å, 22mV of hysteresis and D_{it} $\geq 3x10^{10}$ cm^{-2}, and a flatband shift ΔV_{fb}~600mV, suggesting negative fixed charge in the film.

Lanthanum oxide (La_2O_3) is the candidate that is widely studied in group *IIIB*. Chin *et al.* [1.11] reported transistor results from La_2O_3 films which were formed by evaporation and low-temperature thermal oxidation. Remarkable device results were shown. A physical thickness of 33Å La_2O_3 produced an EOT of 4.8Å, J~10^{-1} A/cm^{-2} at 1.0 V gate bias, and D_{it}~$3x10^{10}$ $eV^{-1}cm^{-2}$. Long-channel transistors with the same films for the gate dielectric exhibited very good turn-on characteristics. However, the film also showed a flat band voltage shift of ~700 mV, indicating negative fixed charge in the film.

Group IVB candidates include titanium oxide (TiO_2), zirconium oxide (ZrO_2), and hafnium oxide (HfO_2). TiO_2 has been intensively studied on as a dielectric for DRAM capacitors due to its attractively high permittivity (k=80-110), depending on the crystal structure and deposition method. However, Ti has several stable oxide states: Ti^{3+} and Ti^{4+}, which lead to a well-known problem with the materials containing Ti-O bond: a reduced oxide. Such a reduced oxide has many oxygen vacancies acting as carrier traps and leakage paths, which make it unfavorable for gate

dielectric application. Moreover, TiO_2 is not stable on Si during deposition by CVD. All studies on this high-k system contain a reaction layer at the channel interface.

ZrO_2 and HfO_2 are the most widely studied high-k dielectrics with encouraging results. Copel *et al.* [1.12] demonstrated that a highly uniform layer of ZrO_2 deposited by ALD can be as thin as 20Å on top of a SiO_2 layer. Perkins *et al.* [1.13] reported an the electrical characteristics of polycrystalline ZrO_2 ALD films deposited on chemically grown oxides. Using TiN as the gate electrodes, they achieved EOT<14Å with a leakage current density $J\sim 2\times10^{-4}$ A/cm^{-2} at $|V_G-V_{fb}|=1$V. Hysteresis was ~10mV with ±2V bias sweep. Electrical properties of HfO_2 film were also studied with TaN electrode [1.14]. By initially sputtering Hf metal in an Ar ambient onto the Si substrate, followed by reactive sputtering of Hf in an Ar/O_2 ambient, a low EOT of 11.5Å with a leakage current $J\sim 1\times10^{-2}$ A/cm^{-2} ($@V_G-V_{fb}=1$V) were reported. With process condition tuning, negligible hysteresis was also achieved. Although very encouraging electrical results for both ZrO_2 and HfO_2 were reported, there remains an unsolved issue which is the fixed charge. Studies show that it can be positive or negative, depending very much on the process conditions during deposition and post-annealing. Houssa *et al.* [1.15] studied the fixed charge in ZrO_2 on native silicon oxide deposited by ALD. It was found that the net fixed charge density could be altered significantly ($Q_f/q>4\times10^{12}$ cm^{-2}) depending on the post-annealing conditions (temperature, gas).

Besides the materials discussed above, pseudo-binary alloys have also gained attention recently. $(ZrO_2)_x(SiO_2)_{1-x}$, $(HfO_2)_x(SiO_2)_{1-x}$, and $(HfO_2)_x(Al_2O_3)_{1-x}$, are the materials that people are particularly interested in. Nitrogen incorporation to high-k films was also studied. To date, research on high-k gate dielectrics is still on-going, as there is still no satisfactory material/technology to form an acceptable high-k dielectric which can fulfill all the requirements of a gate dielectric (a higher dielectric constant

than SiO_2 yet comparable performance with SiO_2 for all other aspects). This is due to several intrinsic limitations which will be discussed in the following session.

1.3.3 Limitations of major high-k gate dielectrics

Although it is attractive to use high-k material for gate dielectric application, there remains several issues that is not completely solved yet. These factors should be considered especially in this case that the high-k is going to be used on germanium.

a. Scaling limit due to interfacial layer (IL)

As is mentioned in the previous discussion, actual experiments show that an interfacial layer between the high-k and the substrate is usually inevitable, even though they are predicted to be thermal-dynamically stable with the silicon substrate. This is mainly because depositions are generally in an oxidation ambient under non-equilibrium conditions, especially for the CVD process. The second reason is that oxygen/water diffuses easily through high-k materials under elevated temperature. As a result, oxidation at the substrate surface easily happens during any post-deposition anneals, and a relatively low k film (SiO_2 like) forms.

IL is very crucial to gate capacitance because

$$\frac{1}{C_{total}} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots \tag{1.5}$$

So the total gate capacitance C_{ox} would be significantly dominated by the smallest capacitance in series. As we know, IL is generally a SiO_2-like film that has a k value just slightly higher than ideal thermal oxide. If 5-6 Å IL would form after the entire IC fabrication flow, it would be very difficult to achieve sub-10 Å (Table 2) of the total EOT together with the top high-k film (EOT of the high-k film has to be less than 4-5

Å). Hence, it is always an issue on how to control and minimize the IL growth, either by deposition technology or process integration consideration.

b. Problems related to film morphology

As thermal oxide is always an amorphous film, high-k films behave in a different way. They re-crystallize from an amorphous phase during the deposition or in a post-deposition annealing. Different materials have different re-crystallization temperatures. Recent studies show that they are all within the temperature range of the standard CMOS process. For instance, HfO_2 re-crystallizes at ~400ºC. Such a polycrystalline film can likely have higher leakage current, less uniform, and less reproducible than an amorphous film. Dopants might also diffuse from the poly gate to the channel faster through the grain boundary of polycrystalline gate dielectric. Further, the anisotropic property of different polycrystalline grain might also have a negative effect on device performance and reliability issues. Although the correlation between film morphology and device performance/reliability requires further investigation, a polycrystalline gate dielectric is generally undesirable.

c. Degradation of carrier mobility

Although recent research on high-k gate dielectrics has shown very encouraging results achieving aggressively scaled EOT with low leakage current in MOS capacitors, the results on transistors fabricated with high-k dielectrics are in a different situation. There is a similar phenomenon for the high-k transistors: the drive current does not increase in the same percentage as the gate capacitance increases [1.16]. The normalized MOSFET transconductance was found to be smaller than those with SiO_2 [1.17]. This seriously affects the implementation of high-k dielectrics for high-

performance CMOS application, where increasing I_d is one of the key motivations. Detailed studies have shown that the carrier mobility of the high-k transistors is much lower than that of the SiO_2 transistors [1.16]. Therefore, the use of germanium as the channel material is attractive because it may compensate the mobility reduction.

At this point, an overview of high-k gate dielectric for MOSFET application is provided, mostly focusing on the choice of materials. Among the many available high-*k* materials, for example, Al_2O_3, HfO_2, $HfAlO_x$, $HfSiO_x$, HfON, HfSiON, etc., we will choose MOCVD HfO_2 as the particular high-k gate dielectric in this study. This is because HfO_2 is a simple binary metal oxide, which is most widely studied to date. It has better thermal stability than ZrO_2 on Si, moderate k value, and relatively wide band gap. The CVD technology is also available in this lab, which is a good facility in terms of repeatability for experiments.

1.4 Current status of Ge MOSFET with high-k dielectrics

Historically, the study of germanium MOSFET started with the focus on obtaining device quality germanium oxide (GeO_2) by different techniques other than simple thermal oxidation. Craciumn *et al.* used low temperature vacuum ultraviolet-assisted oxidation to grow the dielectric on germanium substrate [1.18]. With this technique, the thickness of the grown dielectrics increased with both oxidation time and temperature. The film was also found to be stoichiometric GeO_2. However, the physical thickness of this GeO_2 was 18.8 nm, which is not thin enough for modern VLSI. In addition, there is no electrical characteristic reported for a MOSFET fabricated by this technique. Wang *et al.* compared the GeO_2 films produced by

thermal oxidation and electron cyclotron resonance (ECR) plasma oxidation at lower temperature [1.19]. With this technique, less charge was formed at the interface for ECR plasma oxide. However, detailed analysis shows that there is an interface between the oxide film and the substrate that could be composed of germanium oxide and amorphous germanium. This amorphous germanium might lead to serious mobility degradation. But this remains a speculation because there is no electrical result reported for a germanium MOSFET fabricated with this technique, either.

Since it is difficult to obtain germanium oxide with device quality on germanium crystal, germanium nitride was also ever considered as a dielectric candidate. Hua *et al.* reported germanium nitride films grown on a germanium wafer by thermal reaction in NH_3 and N_2 ambient [1.20]. The film grown by this technique was found to contain oxygen as well (N:O = ~2.5:1). Hence, this film is actually a germanium oxynitride (GeO_xN_y) film. Again, although film morphology and optical property were characterized, there is no electrical result in the report.

While it may be difficult to achieve pure germanium nitride, it is actually more practical to use germanium oxynitride as the gate dielectric. Rosenberg and Martin reported this kind of Ge p-MOSFET in 1988 [1.21]. Some subsequent result of a hole mobility of 1050 cm^2/V-s from the same group of researchers was reported in [1.22]. Further progress was made by Ransom *et al.* with both n-channel and p-channel MOSFETs together [1.23]. As was reported in this paper, the fabrication flow of the device was also a gate-self-aligned process, which is very close to the contemporary device fabrication flow already. Channel mobilities were greater than 1000 cm^2/V-s for both n- and p- channel devices obtained from long-channel device characteristics. They are far higher than the mobilities that are obtained with silicon devices. The effective hole mobility measured by the split-CV method was reported by Shang *et al.*

recently with GeON gate dielectric [1.24]. Gemanium shows ~40% enhanced hole mobility over the silicon universal curve at a vertical electric field of 0.25 MV/cm. Although these results are encouraging, the gate dielectrics thicknesses were all too large to meet the ITRS requirement. Chui *et al.* studied the scalability of GeON on germanium for MOS application [1.25]. Although GeON can be considered a high-k material, it is not a suitable candidate for future ultra-scaled MOSFETs due to its high leakage based on experimental result.

Recently, with the rapid development of high-*k* gate dielectrics for silicon substrate, germanium MOS capacitor combined with high-*k* gate dielectric was first reported by Chui *et al*. [1.26]. The high-*k* gate dielectric - ZrO_2 was prepared by sputtering pure metallic zirconium onto a germanium surface, followed by oxidation in ultra-violet ozone. High frequency capacitor-voltage (C-V) characteristics were reported. P-type transistor was also reported subsequently [1.27], but the gate insulator was very leaky, preventing further measurement of other device characteristics. The deposition technique was then changed to atomic layer deposition (ALD) directly on HF-cleaned germanium surface [1.28]. It was found that local expitaxial growth occurs, and the ZrO_2 film becomes poly-crystalline. This characteristic may introduce a reliability issue of the device when the high-k dielectric is deposited on germanium directly.

Bai *et al.* [1.29] provided a solution to reduce the gate leakage current by nitridation (subjecting the germanium in NH_3 ambient at 600 ºC) just before the chemical vapor deposition of HfO_2. Subsequently, self-aligned Ge p-MOSFETs with CVD HfO_2 were demonstrated by Ritenour *et al.* with this nitridation technique. Similar hole mobility enhancement with Shang was observed [1.30]. Gusev *et al.* used ALD HfO_2 [1.31]. The microstructure and thermal stability of the dielectric on Ge

(100) was studied by transmission electron microscope (TEM), medium energy ion scattering (MEIS), and MOS capacitors. There is no significant structural degradation for the dielectric film deposited on nitrided germanium surface, up to temperatures only 150ºC below the melt point of germanium. The film also maintained its good insulating property.

Although Ge p-MOSFET shows encouraging performance, Ge n-MOSFET remains to have poor characteristics. Ritenour *et al.* reported one I_D-V_D data of a Ge n-MOSFET with extremely low output current [1.30]. Chui *et al.* reported a Ge n-MOSFET with CVD HfO_2 [1.32]. The process flow is non-conventional. Source and drain is formed by diffusion before the gate stack formation. However, the output drive current is not promising, either. Shang *et al.* continued to use GeON as the gate dielectric and fabricated self-aligned Ge n-MOSFET with improved electron mobility. However, it is still far lower than the silicon counterpart.

Besides CVD high-k gate dielctrics, another research group pursued PVD high-k materials to fabricate Ge MOSFETs. Al_2O_3 was firstly used for p-MOSFETs fabricated on Ge-on-insulator (GOI) substrate [1.34], followed by n-MOSFETs with $LaAlO_3$ [1.35], and CMOSFETs with $LaAlO_3$ [1.36]. In contrast, the most significant achievement is that the electron mobility is comparable with the SiO_2/Si universal curve in the most recent result.

On the other hand, formation of Ge n+/p junction is challenging. Both Shang *et al.* and Chui *et al.* studied n+/p junction formation by n-type dopant (P, As) implantation and rapid thermal annealing (RTA) [1.33][1.37][1.38]. This also imposes a challenge in the gate-first self-aligned fabrication of Ge n-MOSFETs.

In summary, the use of high-k gate dielectrics has enabled the fabrication of MOS system with reasonable EOT that meets the future requirement in ITRS. Germanium can be potentially brought back to CMOS area in VLSI.

1.5 Objective of study

As discussed above, many problems are encountered when high-k dielectrics and germanium are implemented in CMOS VLSI device. At the same time, it seems that some of these problems can be solved when the two materials are used together. Moreover, germanium seems to be a possible solution to meet the long term requirement for improved mobility/transconductance in ITRS, based on the early reports that much higher channel mobility can be achieved on germanium than on silicon. Hence, the objective of this study was to try to combine the above two materials together for CMOS field effect transistor (FET) application. Specifically, the engineering issue between the oxide and the semiconductor in a MOS gate stack was studied. This includes two aspects: (1) the effects of germanium on high-k dielectric; (2) the effects of high-k dielectrics on germanium. From the discussion in Section **1.1.2** and **1.2.2**, one can notice that the major challenge for high-k Ge MOSFET is the incompatibility between IL formation arising from the high-k dielectric deposition and germanium oxide formation by the Ge substrate. Thus, a reliable gate stack formation technology for the electrical device operation needs to be developed to facilitate the introduction of both materials to future VLSI. The goal in terms of transistor performance is to achieve both aggressively scaled EOT (the advantage of using high-k gate dielectric) and enhanced mobility (the advantage of germanium) at the same time.

As mentioned, hafnium oxide (HfO_2) was chosen to be the specific dielectric in this study for its simplicity of element composition and simple film formation

technique. If the mobility degradation due to high-k dielectrics can be compensated by using germanium, some reliability issues of the transistors can be evaluated for further understanding.

In terms of device fabrication, the study also aimed to enable a gate-first self-aligned MOSFET fabrication flow, so that it is suitable for VLSI applications.

Because the gate stack is the most important part of a MOSFET, this study may provide essential information for the realization of germanium MOSFET. It could also contribute to the development of a candidate approach to maintain the continuous growth of the semiconductor industry.

1.6 Organization of thesis

The experimental setup for the gate stack formation and fabrication of the Ge MOSFETs is described in Chapter 2. The process integration issues will be discussed here. This is because the fabrication of a MOSFET actually includes many steps besides the oxide/semiconductor stack, for instance, isolation, patterning of gate electrode, etc. Hence these problems should be solved before looking into the critical engineering issues of the gate stack formation.

Chapter 3 will discuss the surface nitridation technique to achieve good insulating property of the high-*k* gate dielectrics which is subsequently deposited on germanium. The physical and electrical effect of this technique is also discussed by using n-type germanium substrates.

Chapter 4 provides an alternative and novel surface passivation technique – silicon passivation on germanium surface by silane (SiH_4) annealing. This chapter consists two parts: firstly, the validity of this novel passivation is evaluated; secondly, the electrical result of the gate stack fabricated on n-type substrate with this technique is reported.

Chapter 5 will focus on the fabrication of Ge n-MOSFETs. In this chapter, we will first discuss the difficulty in making Ge n-MOSFET. Then, the problem is tackled by engineering of the silicon passivation.

After successful fabrication of both p- and n-MOSFETs, Chapter 6 will have a brief study on the reliability of the gate stack. Charge trapping and bias temperature instability (BTI) will be discussed.

The conclusion of this study will be given in Chapter 7. The limitation and the recommendation for future work are also discussed.

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Chapter 2

Experimental Setup for Device Fabrication

There are many process steps needed to fabricate a MOSFET. In a conventional CMOS process flow, silicon is not only used as the channel material, but also as the mechanical support for the integrated circuit. In this study, we will use germanium as the substrate instead of silicon. This means germanium is also used for mechanical support. Hence, the entire process flow will need to be re-considered and examined in order to set up a framework for experiments. The processing and fabricating Ge MOSFETs on the existing processing equipments requires the development of a modified experimental setup. This chapter will describe the experimental setup used to enable the processing and fabrication of the Ge MOSFETs.

2.1 Gate stack formation

In this section, we will briefly discuss the process flow and setup for basic gate stack formation. A conventional gate-first self-aligned process sequence is developed, as this is the current standard gate formation sequence in CMOS integration and it is suitable for mass production because the process cost is low.

2.1.1 Gate oxide deposition

The gate oxide (HfO_2) is deposited on the sample surface by an MOCVD machine (Jusung Eureka 2000®) at 400mTorr and 400 ºC. The liquid metal-organic

source (Hf tert-butoxide) is injected into the reaction chamber by the bubbler method using argon (Ar) as the carrier gas. An additional Ar line is used for chamber pressure control and uniformity improvement. Another line of O_2 is also used to prevent formation of Hf-rich film.

The difficulty is that this machine can only process 6-inch wafers. But the current price of 6-inch germanium wafers is ten times higher than that of silicon wafers because they are not widely available. It is not economical to do experiments directly on 6-inch germanium wafers. The easiest way to reduce experiment cost is to cut the germanium wafer into small pieces for device fabrication. One of the issues is how to deposit high-k dielectric on these small pieces of wafers because the machine is a 6-inch single-wafer processor. An easy approach is to place the small pieces of wafers on top of a 6-inch silicon wafer for deposition since the wafer lies horizontally in the process chamber during the deposition.

Figure 2.1 Sample configuration for CVD high-k deposition. The Ge wafer is placed on a grooved 6-inch silicon wafer to deposit HfO_2 in a 6-inch single-wafer MOCVD reactor.

Basically, there are some aspects which need to be considered in this approach, since the high-k deposition is fine-tuned for gate oxide deposition on silicon substrate, not for gate oxide deposition on a germanium wafer sitting on a silicon substrate. These aspects are gas flow, pressure, and temperature. They are the 3 key parameters in a CVD process. For pressure and gas flow, the deposition will not be affected much

on the small piece of sample because the CVD process is controlled in the surface-reaction-limited region [2.1]. Hence, the remaining dominant factor is temperature. Since the heating element is a graphite heater under the silicon wafer, the temperature of the small Ge sample on the silicon wafer could be ~10-20 ºC lower than that of the silicon wafer. Consequently, the deposition rate and film structure could change on the small germanium wafer. In order to control the gate oxide thickness precisely, it is at least necessary to test the deposition rate just before a gate oxide deposition for germanium device fabrication.

Another concern is that the small germanium wafer might move out of the silicon wafer during the deposition process and drop into the process chamber. To prevent this kind of accident, a safe way would be to make a silicon groove-wafer which is thinner in the center than at the edge (Figure 2.1). Another advantage of this approach is that the surface temperature difference between the germanium and the silicon wafers can be reduced.

Figure 2.2 shows the fabrication flow of the silicon groove-wafer. A wet oxide layer of 4000 Å thickness was firstly grown on the surface of the silicon substrate in conventional oxidation furnace (a). Photo resist was then spun onto the wafer front side (b), followed by a conventional lithography process for photo resist patterning (c). Baking was conducted to harden the photo resist. Subsequently, photo resist was spun onto the wafer back side and baked again. The wafer was entirely covered by photo resist (d). The SiO_2 was then etched by Buffer Oxide Etchant (BOE, NH_4F: HF= 6:1) (e), followed by the removal of photo resist in a piranha chemical solution (H_2SO_4:H_2O_2=4:1) (f). At this stage, the silicon wafer was completely covered by silicon oxide with an open window in the center of the front side. This silicon oxide

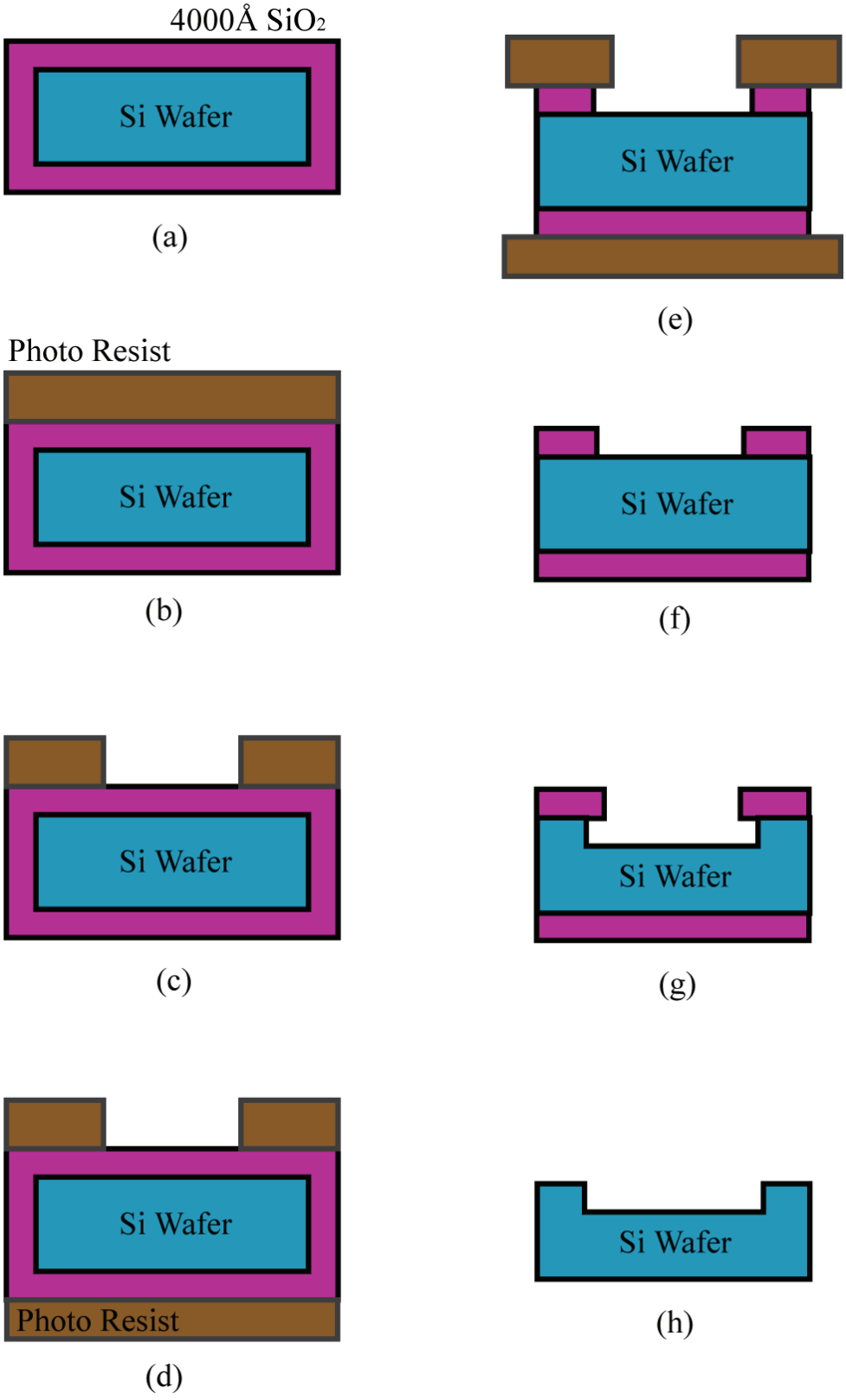

Figure 2.2 Fabrication of Si groove-wafer. (a) wet oxidation; (b) Photo-resist spin-on; (c) Lithography; (d) Back-side photo-resist spin-on; (e) Wet etch of SiO_2; (f) Photo-resist removal; (g) Wet etch of silicon wafer; (h) Oxide removal.

was then used as the hard mask for silicon etching. The silicon etching was carried out in a concentrated KOH solution (45%). The etch rate selectivity between silicon and silicon oxide can be as high as 1000:1. However, as the etching process takes place in room temperature (short of heating equipment), it takes 1 week to etch away ~160 μm of silicon (g). Thorough rinsing in de-ionized water (DIW) was carried out carefully at this step to remove any possible KOH residue as potassium is a contaminant in CMOS integration. The remaining silicon oxide was then stripped away in BOE (h). The silicon groove-wafer can also be recycled.

2.1.2 Gate electrode formation

To simplify the experiment, only one kind of gate electrode material was used throughout the study, and this is tantalum nitride (TaN).

The tantalum nitride film can be deposited onto the sample surface by reactively sputtering of a pure tantalum (Ta) target in N_2 + Ar ambient (PVD). Argon ion is used as the bombardment species. The process takes place in room temperature at 3 mTorr with 25 sccm Ar flow and 5 sccm N_2 flow. The applied DC power is 400 W.

While the formation of TaN films is relatively straightforward and simple due to PVD's advantage as discussed earlier in Page 14, it is difficult to pattern the TaN film. Figure 2.3 shows the target structure of TaN patterning. After lithography of the photo resist (PR), TaN shall be etched away selectively on the HfO_2 film.

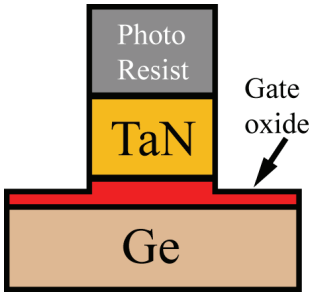

Figure 2.3 Target structure after plasma etching of the gate electrode. The etch process should be stopped at the gate oxide so that the germanium substrate remains intact.

In the wet etch method, TaN was found to neither react with concentrated acid solution, nor with NH_4OH at room temperature. On the other hand, oxidants such as H_2O_2 and concentrated H_2SO_4, which are used commonly in a standard CMOS integration, must be avoided because they attack germanium. Hence, TaN on Ge has to be etched by dry etch methods.

Since the gate length of the transistors used in this experiment are relatively large (>5 μm) compared to the state-of-art VLSI MOSFETs, there is no difficult requirement for the etch profile of TaN. The only two criteria are etching uniformity across the wafer and the selectivity of TaN over HfO_2. The need is to ensure that the TaN etching can be stopped at the HfO_2 film precisely. These two criteria would be addressed in the following discussion of the process development.

The dry etching was done by high-density plasma in a LAM TCP9400® machine. Plasma is generated by inductive coupling method. There are four major process parameters to be determined. They are RF upper power, RF lower power, gas flow rate, and pressure. As a detailed theory of plasma etch can be found elsewhere [2.2], only a brief functional description of these four parameters would be discussed here. The dry etch process involves chemical and physical mechanisms. RF upper power is the output power of the RF inductor coil above the process chamber. It is directly related to the plasma density during process, which is the chemical component of the etching. RF lower power is the output power of the electrode under the wafer, which is to control the ion energy in the vertical direction to the sample surface. This is to control the ion bombardment to the sample surface, which is mainly the physical component in plasma etching. Gas species and their flow rate into the etching chamber are also critical for plasma etching. The flow rate determines the supply of reactants and the removal efficiency of reaction products. The last parameter (pressure) determines the

plasma density in the etching chamber. A successful process setup for TaN etch would include complex parameter tuning.

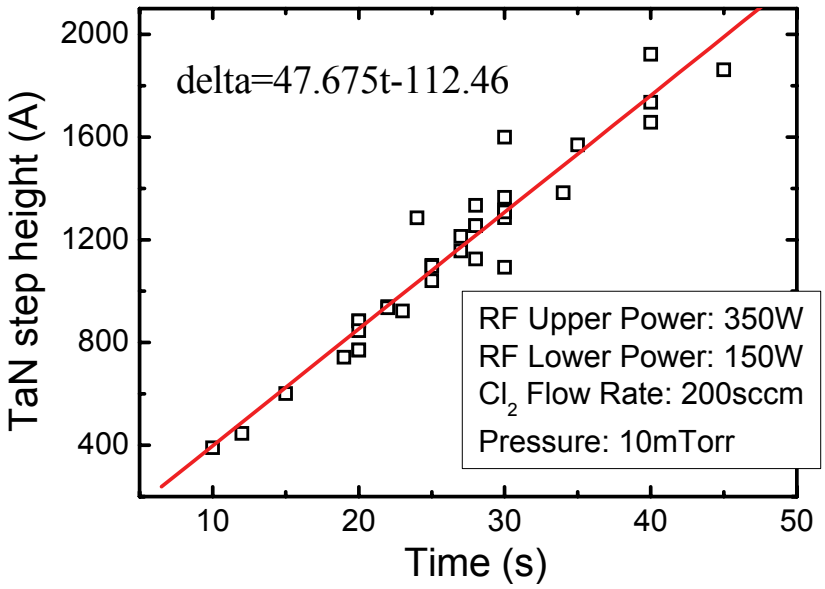

Figure 2.4 Etch of TaN film with different etching time

In order to have a better control of the etching process to achieve uniformity and selectivity at the same time, a two-step etching process is adopted. The first step etch is the main etch, in which TaN would be etching fast. In this step, the process condition is tuned to have more physical ion bombardment to assist the etching in order to have good uniformity across the wafer. However, the selectivity of the metal over the oxide underneath would be low. This step must be stopped before the exposure of oxide to the plasma, because there is no optical emission spectroscopy available for endpoint detection. Hence, the etch step has to be controlled by precise timing. A large amount of TaN samples were first tested with different etching time and the step height was measured by a step profiler. Chlorine (Cl_2) plasma was used. The results are shown in Figure 2.4 with etching parameters. A linear fitting of the data was then obtained where *t* is time in seconds. This equation will provide essential

timing information for gate etch of actual devices if the initial TaN film thickness is known.

The main etching time is calculated to etch TaN to the point where 100~150Å TaN remains on the gate oxide. Then, the etching is switched to another step called over-etch. In this step, the process recipe is tuned to another condition in order to increase the selectivity of TaN over HfO_2. The basic guideline is to increase the chemical etching component and reduce the physical etching component in the etching process. After fine tuning, the RF upper power was increased from 350 W to 450 W to increase the plasma density. The RF lower power was reduced from 150 W to 40 W to reduce the ion bombardment effect in the etching. Chamber pressure was increased from 10 mTorr to 40 mTorr. This also helps to move the process towards chemical etching dominated region. With this recipe, it was found that the etch rate of TaN is ~25 Å/s. At the same time, it was found that the selectivity is ~9, which means it is safe for a 30-second over-etch if the HfO_2 thickness is ~80Å.

By the two-step plasma etching, the structure in Figure 2.3 can be achieved.

2.2 Process integration

A complicated process sequence is required in order to fabricate the usual CMOS transistor structure in Figure 1.1. Since the study here is to focus on transistor using new materials and substrate, the process used here was made as simple as possible. Hence, transistors were fabricated with a ring-type structure, the number of masks can be kept minimum in the process flow. Figure 2.5 shows the gate-mask structure used in this study. The gate includes a square area (100 μm X 100 μm) for probing. There is another ring outside of the transistor for isolation purposes in the case of depletion-mode transistor.

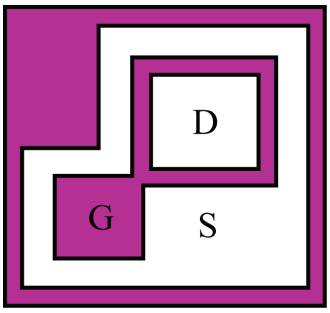

Figure 2.5 Mask pattern for the gate electrode

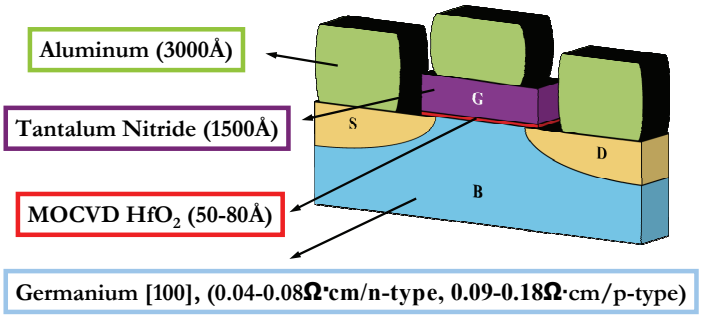

Figure 2.6 The cross-section of the final MOSFET structure in this study

If it is necessary to reduce contact resistance, aluminum can be deposited and patterned in the source/drain region by one additional mask. The cross-section view of the device is shown in Figure 2.6.

Here is a brief description of the target process flow:

(1) Pre-clean of the wafers (chemical dip followed by DIW rinse)

(2) Oxide deposition (including pre-treatment and MOCVD)

(3) Post-deposition anneal

(4) Metal gate (TaN) deposition (sputtering)

(5) Lithography (Gate mask)

(6) Plasma dry etch

(7) Photo resist removal (O_2 plasma ashing / Acetone clean)

(8) Source/drain implantation (Boron for p-MOSFET and phosphorus for n-MOSFET)

(9) Post-metallization anneal / source and drain activation anneal

(10) Back-side Aluminum deposition (sputtering or e-beam evaporation)

(11) Forming gas anneal ($H_2 + N_2$)

(12) Aluminum deposition (sputtering or e-beam evaporation)

(13) Lithography (Al contact mask)

(14) Aluminum etching (wet method)

(15) Photo resist removal (Acetone clean)

It should be mentioned that the device fabrication flow is not always the same in this study. According to different objectives of the experiments, the above flow would be re-arranged or abbreviated to facilitate the development of Ge MOSFETs.

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Chapter 3

Passivation of Germanium Surface by Nitridation for Fabrication of p-MOSFETs

As has been mentioned in Chapter 1, the major challenge for high-k Ge MOSFET is the incompatibility between interfacial layer formation due to high-k deposition and germanium oxide formation due to oxidation of Ge substrate. Chui *et al.* has demonstrated p-channel germanium MOSFETs with ultra low equivalent oxide thickness (EOT) of 6-10Å, which utilized ultra-thin ZrO_2 fabricating by direct Zr sputtering at room temperature followed by UV ozone oxidation [3.1]. One of the limitations of this device is that the gate leakage is very high, ~2 A/cm^2 for nMOS-capacitors and ~0.8 A/cm^2 for pMOS-capacitors under 1V accumulation bias [3.2]. Hence, the surface treatment used to passivate germanium surface prior to high-k deposition is the critical process in gate stack integration for Ge MOSFET. Bai *et al.* reported the first HfO_2/Ge MOS capacitors in which the HfO_2 dielectric was deposited by CVD method [3.3]. It was found that surface nitridation by annealing in ammonia is effective in improving the gate leakage performance (6.14×10^{-3} A/cm^2 for pMOS-capacitors under 1V accumulation bias). However, physical characteristics were not evaluated for further understanding. It is also unknown whether the nitridation is affected by the Ge surface cleaning process. Thus, it is of great importance to study the effect of surface NH_3 annealing on the Ge substrate with different cleaning methods, and to combine the physical and electrical characterization of the CVD HfO_2 layers on Ge substrates.

3.1 Experiment

Table 3.1 Split conditions of the experiment

No.	Split	Condition
1	Surface cleaning	(1) NH_4OH, H_2O_2; (2) DHF
2	Surface treatment	(1) without nitridation; (2) with nitridation

Table 3.1 describes the split conditions in this experiment. The starting Ge wafers were n-type (100) wafers (Sb doped, resistivity=0.04~0.08 Ω•cm). The wafers were prepared with two different surface cleaning methods. The first one is to dip in NH_4OH:DI-water (1:4, 300 seconds) to remove the native Ge oxide, then in H_2O_2:DI-water (1:5, 60 seconds) to form a chemical oxide on the surface, and again in NH_4OH:DI-water (1:4, 300 seconds) for chemical oxide removal with de-ionized water rinsing between each chemical dipping [3.4]. Another set of Ge substrates were cleaned by DHF and rinsed in de-ionized water. Following that, annealing in a NH_3 ambient (50 Torr, NH_3 purity=99.999%) was performed inside a chamber with a base pressure of $5x10^{-6}$ Torr and at a constant temperature of 600ºC. After that, HfO_2 was deposited in another chamber using MOCVD with Hf tert-butoxide as the metal organic precursor in an Ar+O_2 ambient (400 mTorr) at 400ºC in another chamber with a base pressure of $3x10^{-3}$ Torr (target thickness: 50Å). Both the NH_3 treatment chamber and HfO_2 deposition chamber are within a cluster system (Jusung Eureka 2000®) with vacuum load lock used to store and transfer wafers. A post-deposition anneal (PDA) was then performed in a rapid thermal processor (RTP) in N_2 ambient under 760 Torr at 600ºC for 30 seconds. After that, a layer of 150 nm TaN was sputtered at room temperature. This was followed by lithography. The TaN dry etching was based on the earlier process development which is described in Chapter 2. Forming gas annealing was performed in H_2+N_2 ambient at 300ºC for 10 minutes.

Additionally, p-MOSFET devices were implanted with boron ($5x10^{15}$ cm^{-2}, 35 keV), and then annealed in furnace at 425 ºC for 10 minutes for dopant activation. No aluminum contact was employed for the transistors in order to simplify the device fabrication flow. High-resolution angle-resolved *ex situ* X-ray Photoelectron Spectroscopy (XPS) analysis was performed using a *Physical Electronics Quantum 2000 Scanning ESCA Microprobe* with a monochromatic and standard Al X-ray source. Capacitance-voltage (C-V) characteristics were measured by an Agilent 4284A LCR meter and leakage current density-voltage (J-V) curves were measured by a Hewlett-Packard 4156A semiconductor parameter analyzer. High-resolution cross-sectional transmission electron micrographs (HR-XTEM) were also taken for physical characterization.

3.2 The physical effects of surface nitridation

The physical effect of surface nitridation is studied by *ex situ* X-ray photoelectron spectroscopy (XPS). Two aspects were considered: (1) the effects on the germanium surface before HfO_2 deposition; (2) the effects on the subsequent HfO_2 film.

To study the first aspect, the sample cleaned by NH_4OH and H_2O_2 was annealed in NH_3 ambient for 10 minutes, and its Ge 2p3 core-level XPS spectrum was presented in Figure 3.1 by empty-circle line. For comparison, two samples which did not undergo NH_3 annealing were also analyzed. One was only with the wet cleaning; the other was annealed in vacuum (without NH_3 gas flow) in the same process chamber for 10 minutes after the wet cleaning. The result from these two control samples were shown with closed-boxed line and empty-triangle line.

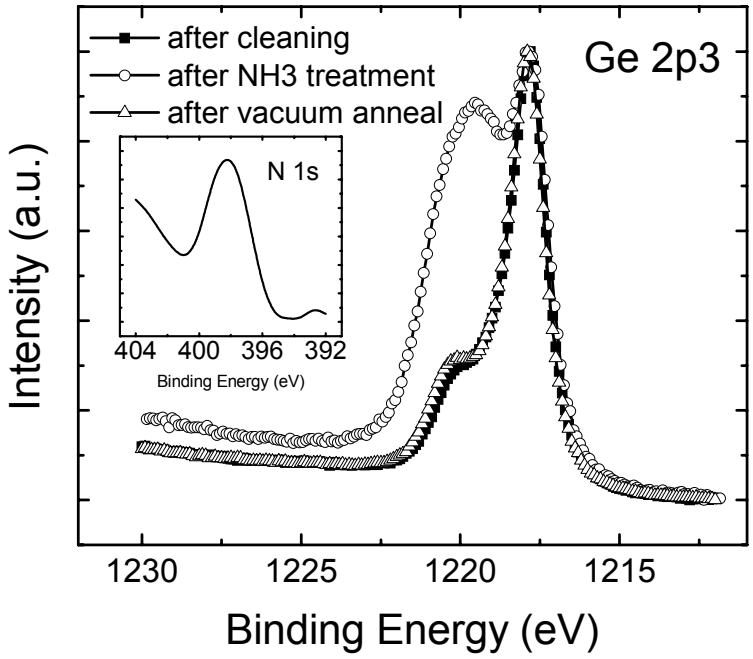


Figure 3.1 XPS analysis of nitridation process on germanium surface. GeON is formed on top of the germanium surface after NH_3 treatment. There is no additional oxidation of the sample that is with vacuum anneal, as compared to the as-cleaned sample. This indicates the additional oxygen in the GeON film is from the impurities in the NH_3 gas.

For the sample that underwent wet cleaning, the main peak located at 1217.8 eV is attributed to metallic germanium from the substrate [3.5]. The shoulder, ranging from 1219 eV to 1221 eV, is attributed to GeO_x ($x \leq 2$) [3.5] which is believed to be introduced during sample transportation. The empty-circled line shows the sample which has undergone NH_3 annealing after the same cleaning procedure. The background level of this spectrum is higher than the previous one, which implies that a film is formed after the NH_3 annealing. This is because a certain amount of the photoelectrons excited from the substrate interact with the top film and increase the background level. Another important finding is that the small shoulder in the previous spectrum has evolved into a broad peak (~1219.5 eV). Considering all the possible bonds that Ge atoms may have, it is reasonable to infer that the broad peak consists of

two types of bonds: the Ge-O (1220.1 eV) and the Ge-N (1218.9 eV). Detailed curve fitting is carried out with Shirley background and Gaussian-Lorentzian lines. The obtained χ^2 is around 4.151, which is considered to be a good fitting. The whole Ge 2p3 spectrum consists of three peaks, which are identified as metallic germanium, Ge-N and Ge-O bonds, respectively [3.5]. The nitrogen existence is also confirmed by the N 1s signal that is shown in the inset figure in Figure 3.1. Hence, it can be concluded that germanium oxyniride (GeO_xN_y) is formed after the NH_3 annealing. Moreover, the N1s binding energy (397.8 eV) also suggests N binds to Ge instead of O in this compound. By calculating the area under the fitted Ge-O and Ge-N curves, x and y can be quantified to be around 0.83 and 0.17, respectively. In order to clarify where this large amount of oxygen in GeON is from, one needs to analyze the spectrum from the sample with vacuum annealing. It clearly shows that there is no substantial oxidation, compared to the as-cleaned sample. This means that the high oxygen content in the GeON film is likely introduced by the NH_3 gas source, even though the purity of the NH_3 gas is 99.999% (with the main impurities of O_2, H_2O, and H_2). This high oxygen concentration implies that germanium is much easier to be oxidized than nitridized.

It is found that the pre-clean methods do not affect the NH_3 annealing process. The Ge 2p3 spectra are similar between the samples with different cleaning procedures, which is shown in Figure 3.2. A GeON film forms on the DHF-cleaned sample surface after NH_3 annealing.

In order to investigate the NH_3 annealing effect on the subsequent HfO_2 chemical vapor deposition, XPS spectra were collected from another two CVD HfO_2 deposited samples (same HfO_2 deposition time). One is with NH_3 annealing (annealing time was reduced to 30 seconds); the other is without NH_3 annealing. The Ge 2p3 and Hf 4f spectra were collected and shown in Figure 3.3. For comparison, the Hf 4f spectrum of

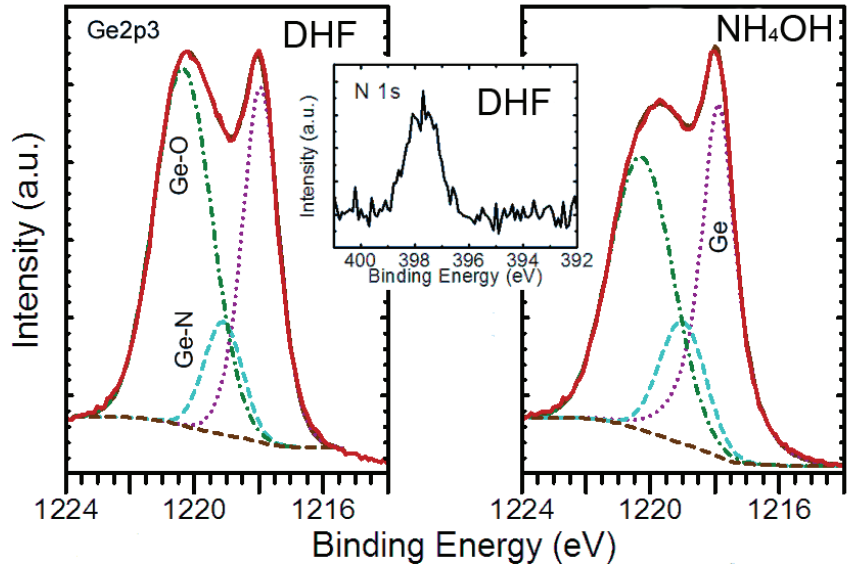


Figure 3.2 Ge 2p3 XPS spectra of nitrided Ge surface with different cleaning processes. There is no substantial difference in the two spectra. GeON film forms on top of the germanium surface.

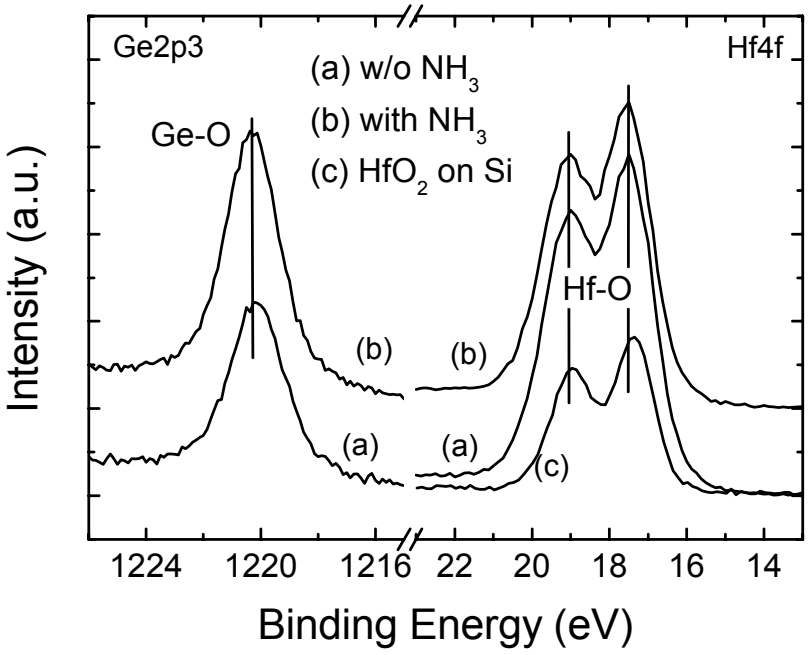
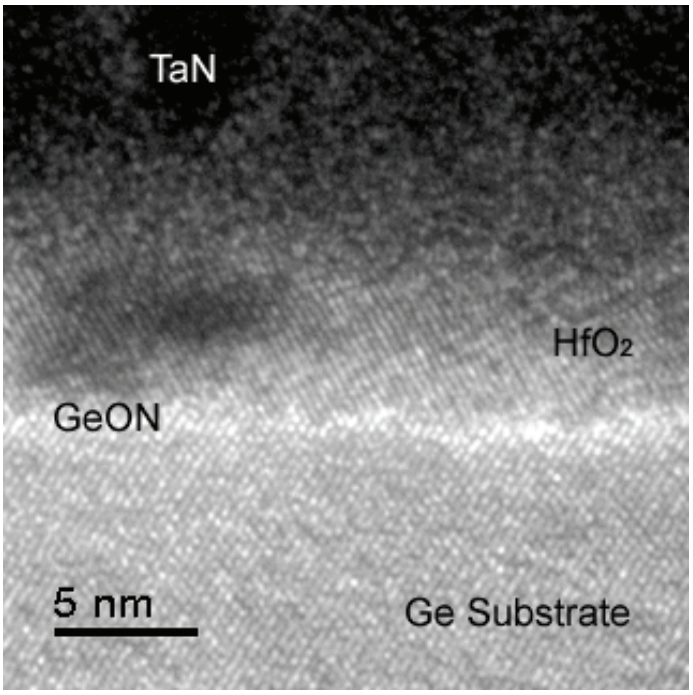


Figure 3.3 Ge 2p3 and Hf 4f XPS spectra of HfO_2 deposited on germanium surface with (b) and without (a) nitridation. Germanium is incorporated in the HfO_2 films in both samples. The GeON film induced by nitridation does not act as an effective barrier against germanium out-diffusion.

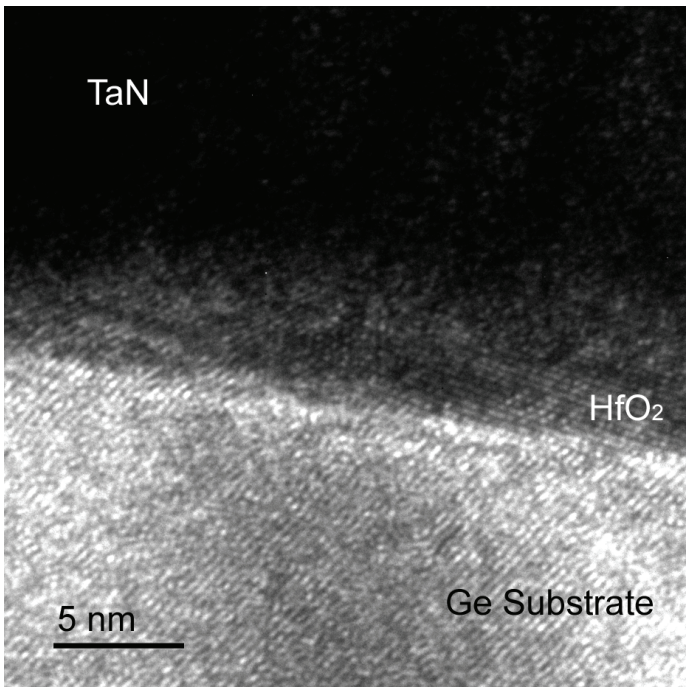
HfO_2 on silicon substrate is also plotted. There is no substantial difference in the binding energy of the Hf 4f peaks between silicon and germanium substrates, implying that the hafnium is fully oxidized on both substrates. On the other hand, Ge 2p3 peaks at 1220.1 eV were detected and are identified as Ge-O bonds for the two Ge samples with and without surface nitridation. Since there was no metallic Ge bonds found in these two samples, the Ge signals are believed to come from the HfO_2, which means that Ge had been incorporated in the HfO_2 films. This Ge incorporation phenomenon is probably a result of the Ge out-diffusion from the substrate during the CVD process, which occurs at a temperature of 400ºC. Further, since no Ge-Hf bond is detected in either samples, the dielectric should be of good electrical insulating property in terms of chemical states. Considering the chemical similarities between Ge and Si [3.6], two kinds of possible structures may exist for the Ge incorporated HfO_2 film. The first possibility is that the dielectric film is a mixture of HfO_2 and GeO_2. The other possibility is that the film is hafnium germinate and that the Hf 4f bonds are not affected by the vicinity of Ge atoms. However, this cannot be addressed by analyzing the O 1s signal in this experiment because it overlaps with the Ge LMM Auger signal. To overcome this, one should either use the Mg kα X-ray instead of Al kα X-ray to move away from the Ge LMM Auger signal, or analyze other electrons of the oxygen atoms.

By now, the material structure of the sample with surface nitridation and after MOCVD HfO_2 is clear.. After surface nitridation, a layer of GeON was formed on top of the germanium surface (however, the thickness is not known yet). When HfO_2 is deposited on the sample, GeON acts as an interfacial layer between HfO_2 and the Ge substrate. Meanwhile, large amount of germanium was also found in the HfO_2 film.

This indicates that the GeON film does not act as an effective barrier against the out-diffusion of germanium from the substrate.



(a)



(b)

Figure 3.4 TEM images of HfO_2 deposited on germanium surface with nitridation (a) and without nitridation (b).

In order to have additional information of the gate stack, HR-XTEM images were taken on the Ge MOS capacitors with and without NH_3 anneal (capped with TaN gate electrode). Figure 3.4(a) presents the capacitor with surface nitridation. The dielectric thickness measured from the TEM picture is ~51Å. From Figure 3.4(a), it is also noticed that, unlike the interfacial layer on Si substrate [3.7], the interfacial layer on Ge substrate is crystallized. The crystallized interfacial layer may be related to its high oxygen concentration, since GeO_2 induced by gaseous O_2 on Ge substrate was found to be poly-crystalline [3.8]. It is also noted from the TEM picture that the dielectric film has re-crystallized, which implies that the crystallization temperature of the HfO_2 film with Ge is lower than 600 ºC. For comparison, the TEM image of MOS stack without NH_3 anneal is also presented in Figure 3.4(b). As can be observed, there is no sharp interface between the dielectric and the substrate in some local position. This could be the consequence of the non-uniform interfacial layer, which is due to the non-uniform oxidation behavior of the germanium [3.8].

3.3 The electrical effects of surface nitridation

Figure 3.5 shows the C-V characteristics of HfO_2 Ge MOS capacitors with surface nitridation (30 seconds) fabricated with an area of 100µm x 100µm. The device was swept from inversion to accumulation, and the J-V characteristics are shown in the inset. For comparison, both C-V and J-V characteristics of HfO_2 Ge MOS capacitor without surface nitridation (same dimension) are also included. By fitting the C-V data to a simulation model which took into account the quantum confinement effects, it is shown that a small EOT of 10.5Å and a low leakage current of 5.02×10^{-5} A/cm^2 at V_g=1 V was achieved for the MOS capacitor with surface nitridation. If the physical thickness of the gate dielectric that is observed in the TEM is accepted (Figure 3.4(a)), the effective dielectric constant of dielectric is ~18.9. For

the MOS capacitor without surface nitridation, an EOT of 16.8Å is obtained with a leakage current of 1.01 A/cm^2 at V_g=1 V. Since the workfuntion of TaN [3.9] is 4.4~4.6 eV, the device without NH_3 anneal has a closer flatband voltage to the ideal one than the device with surface nitridation. The negative shift of the flatband voltage of the surface nitridation device may be due to a significant positive charge (~5.3x10^{12} cm^{-2}) introduced by the NH_3 annealing. Figure 3.6 shows the gate leakage current density as a function of EOT together with existing published data [3.1] [3.3] [3.10]. Thus, though the Ge incorporation in HfO_2 films is observed for both samples with and without surface nitridation and both samples show similar chemical states, the NH_3 annealing is very effective in improving the electrical properties of Ge MOS capacitors. The smaller EOT of the MOS capacitor with NH_3 annealing may indicate that its dielectric and/or the interfacial layer is thinner than that of the capacitor without NH_3 annealing. On the other hand, the leakage current result is different from high-k MOS capacitors on silicon substrates where larger dielectric/interfacial layer usually yields smaller gate leakage current. Considering the fact that there is no significant difference in the chemical bonding in the dielectrics of both samples, the large difference of the leakage currents could be likely attributed to the interfacial layer. Therefore, the large leakage current of the Ge MOS capacitor implies a poor quality of interfacial layer (GeO_x) when there is no surface nitridation. This is reflected in Figure 3.4(b) where a lot of non-uniformity in the interfacial layer is observed, which can eventually degrades the MOS leakage current.

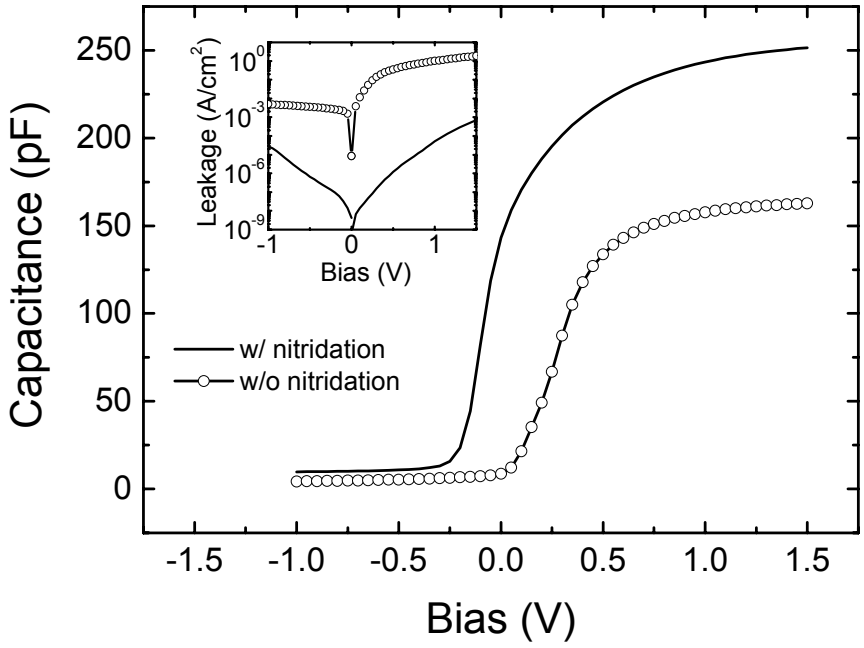


Figure 3.5 C-V curves of the TaN/HfO_2/Ge MOS capacitors with and without nitridation. The inset shows the J-V curves of the capacitors with and without nitridation.

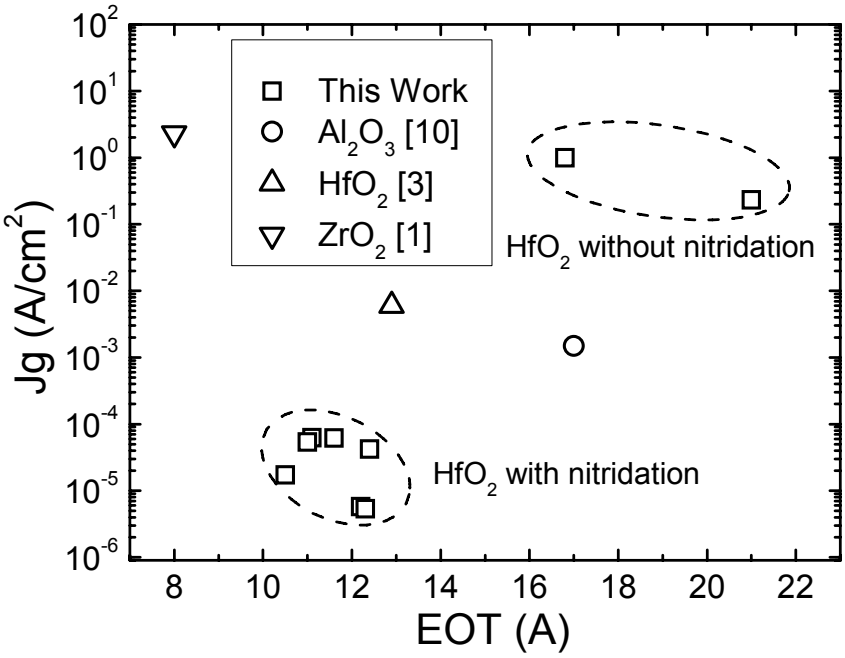


Figure 3.6 Leakage-EOT performance of the TaN/HfO_2/Ge MOS capacitors with and without nitridation. Results from other research groups are also included.

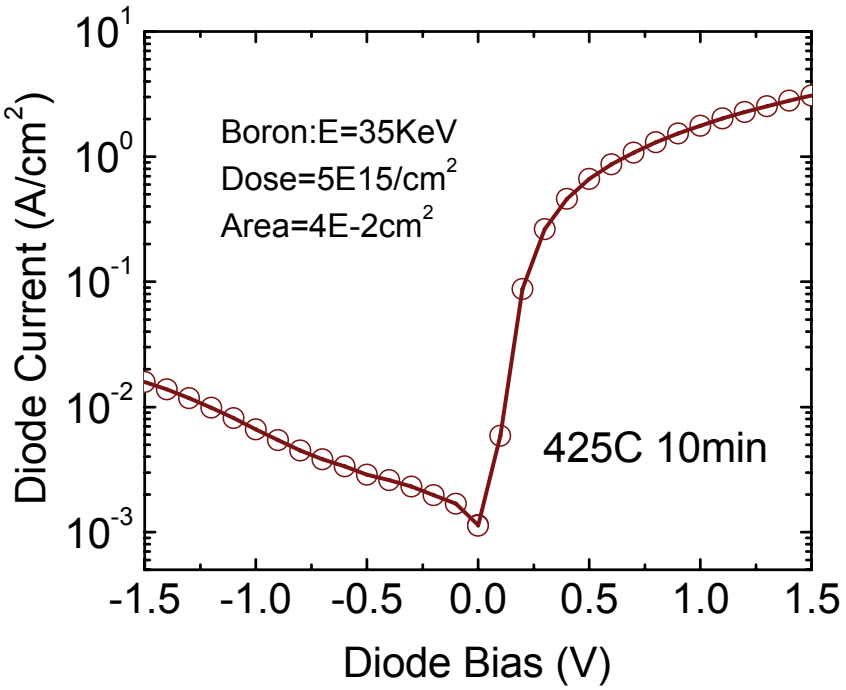


Figure 3.7 I-V characteristic of the p+/n diode of the Ge p-MOSFETs. Boron can be activated at ~425ºC.

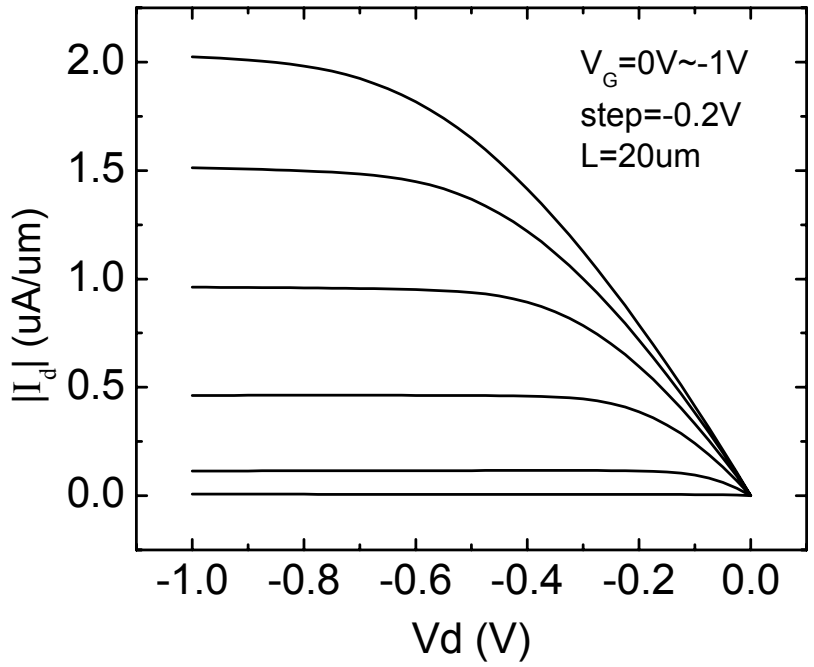


Figure 3.8 Output characteristic (I_D-V_d) of the Ge pMOSFET with surface nitridation.

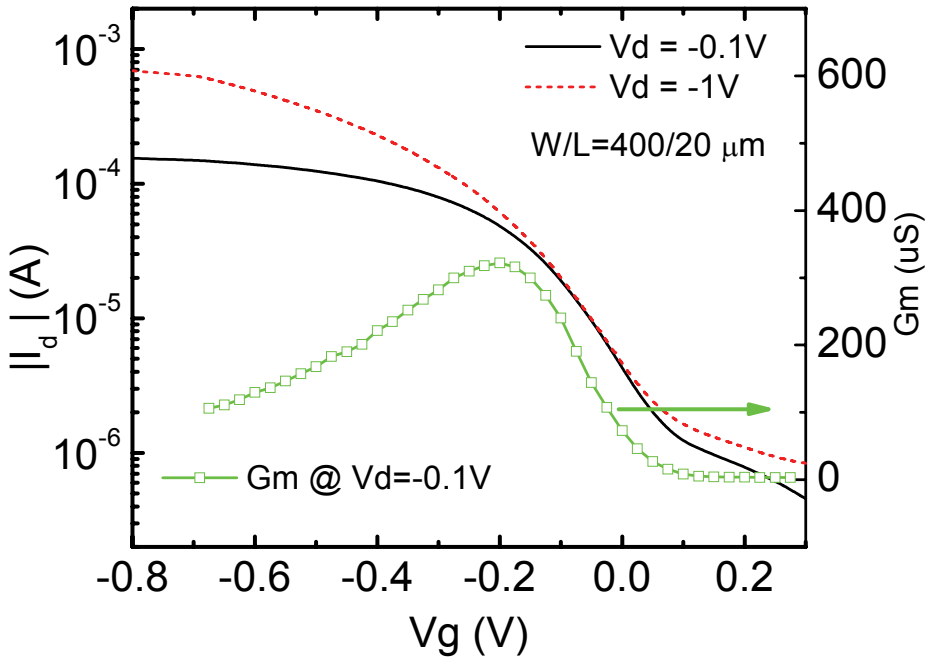


Figure 3.9 Transfer characteristic (I_D-V_g) and the transconductance of the Ge pMOSFET with surface niridation.

A transistor was fabricated with this gate stack with surface nitridation (30 seconds), cleaned by the first method. Figure 3.7 is the diode characteristic of source/drain area. It shows that boron can be activated at 425ºC as a ~2-order on/off ratio is observed. Figure 3.8 presents the I_d-V_d characteristics of device with SN+HfO_2 dielectric. The device exhibits good output behavior. The threshold voltage is -0.025 V. The drive current is ~ 2 μA/μm for a gate over drive (V_g-V_{th}) of -1 V. The transfer I_d-V_g characteristics of Ge pMOSFETs are shown in Figure 3.9. For the moment, only 2 orders of on-off current ratio was obtained. This may be due to the large junction leakage current which makes small off-current difficult. The sub-threshold swing (SS) is large (~139 mV/dec) probably due to the small on/off current ratio and/or a large interface trap density, which requires further study and improvement. Figure 3.10 shows the calculated mobility data. The inversion charge Q_{inv} estimated by C_{inv}x(V_g-V_{th}), and the depletion charge Q_B is estimated by $\sqrt{4\varepsilon_{Ge} q N_d \psi_B}$. Subsequently, the hole

mobility was calculated by $\mu_{hole} = \frac{I_D L}{Q_{inv} V_{ds} W}$, and the channel vertical electric field was calculated by $E_{eff} = (Q_B + \frac{1}{3} Q_{inv}) / \varepsilon_{Ge}$. The mobility is comparable with the silicon universal curve. Germanium pMOSFET can gain 2.3x peak mobility compared with published Si counterparts with HfO_2 dielectric [3.11].

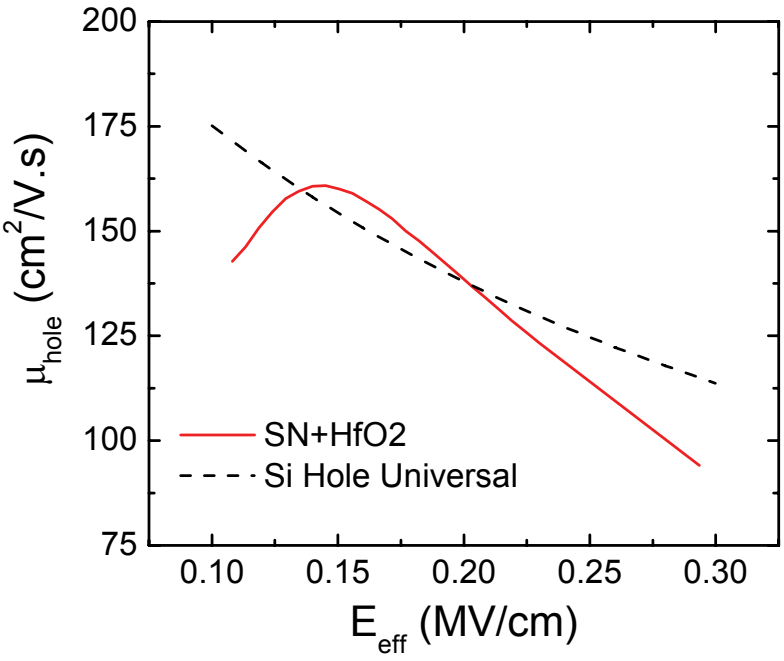


Figure 3.10 Estimated hole mobility of the Ge pMOSFET with surface nitridation The hole mobility in germanium is comparable to the silicon universal curve.

3.4 Summary and discussion

In summary, the surface NH_3 annealing effects on the physical and electrical properties of MOCVD HfO_2 Ge MOS capacitors have been investigated. It is found that GeON is formed during surface nitridation (NH_3 annealing). Germanium is found to be incorporated within CVD HfO_2 films which may be related to the Ge diffusion at

high temperature during the CVD deposition. In addition, the electrical characteristics of HfO_2 Ge MOS capacitors show that surface nitridation is a very effective way to improve the electrical properties in terms of I_G and EOT. An EOT of 10.5 Å and gate leakage of 5.02×10^{-5} A/cm^2 @ V_G=1V are achieved simultaneously on a MOS capacitor. A transistor was fabricated successfully. Although there are imperfections in areas such as on-off current ratio, sub-threshold swing, etc, the output current is encouraging and comparable with the silicon universal curve. This does show that HfO_2/Ge system does have some advantage over its silicon counterpart.

The nitridation technique relies on the fact that GeON is more stable than GeO_2. The gate leakage current was found to be greatly reduced. However, there are several critical limitations for surface nitridation: (1) recent research on silicon substrate shows that nitrogen in the gate oxide degrades oxide/interface quality and increases the interface trap density [3.12]. Consequently, nitrogen degrades the mobility in such MOSFETs [3.12]. This will reduce the mobility gain that one can achieve with a germanium channel, and this probably is the reason that the peak hole mobility is only ~5% higher than the silicon universal curve at the same electric field in Fig. 9 in Chapter 3; (2) Ge n-MOSFET fabrication has not been successful with surface nitridation. The reason for this will be addressed in the next chapter; (3) surface nitridation on silicon substrates also leads to a large hysteresis in the MOS device properties [3.12], implying that there is serious charge trapping in the gate oxide. This makes such devices unacceptable for circuit application; (4) surface nitridation cannot prevent germanium from out-diffusing from the substrate into the gate oxide, and this could potentially degrade the gate oxide performance and/or reliability. Therefore, surface nitridation for germanium MOSFET could provide very limited performance and is not promising for real VLSI applications.

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Chapter 4

Passivation of Germanium Surface by Silicon for Fabrication of p-MOSFETs

In the last chapter, the surface nitridation technique for germanium passivation was studied and a Ge p-MOSFET with CVD HfO_2 was demonstrated successfully. However, there are limitations which hamper the device performance. In this chapter, an alternative surface passivation process for high-k/Ge MOS device will be proposed and developed by using SiH_4 gas in a conventional LPCVD reactor. Its inspiration comes from high-k deposition on silicon substrate, which inevitably involves the growth of an interfacial layer (IL) between the high-k and the silicon substrate. The process scheme is described in Figure 4.1.

In Figure 4.1, after a pre-clean of the germanium wafer (a), the native germanium oxide is removed (b). Subsequently, the wafer is annealed in a SiH_4 ambient in the LPCVD reactor in order to form an ultra-thin silicon layer on top of the germanium surface (c). In the following HfO_2 deposition, the Si passivation layer would contribute to an interfacial layer (IL) which is likely to be silicate ($HfSiO_x$) [4.1], because a chemical vapor deposition process always occurs in a non-equilibrium condition [4.2].

The silicon passivation layer works in such a way that it is consumed before the underneath germanium is oxidized. Therefore, formation of the notorious germanium oxide can be minimized and improved MOSFET performance can be expected. The

second advantage is the natural lattice compatibility between silicon and germanium. Thus, the dangling bonds between silicon and germanium can be minimized by careful process optimization so that the interface state density between silicon and germanium is also minimized.

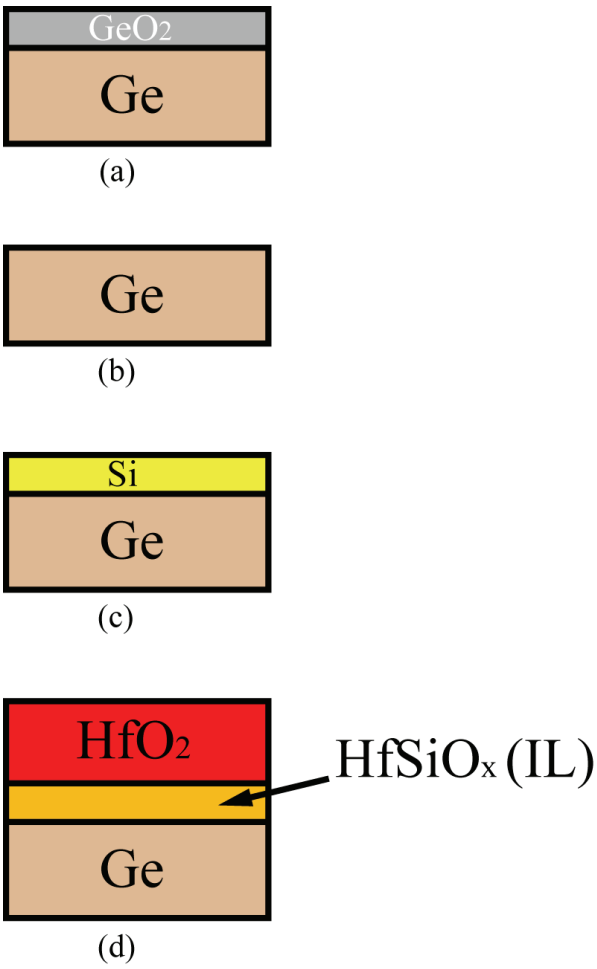


Figure 4.1 Silicon passivation (SP) scheme for Ge MOS application. (a) the starting wafer after pre-clean in atmospheric ambient; (b) the wafer surface is free of germanium oxide in the process reactor; (c) an ultra-thin silicon layer is deposited on the germanium surface; (d) after the subsequent HfO_2 deposition, the silicon layer contributes to a hafnium silicate-like interfacial layer.

4.1 Principle

The passivation is a CVD process at its initial stage, since it is an annealing in SiH_4 ambient and the target is an ultra-thin silicon layer. The first stage is the heterogeneous deposition of silicon (from SiH_4) on the clean germanium surface. The second stage is the homogeneous deposition of silicon (from SiH_4) on the newly laid silicon surface. The entire process consists of a large ensemble of gas phase and surface reactions that include adsorption of silane on silicon and on germanium, H desorption from silicon and from germanium, surface diffusion, dissociation of SiH_4, etc.

Early study has shown that the silane adsorption rate on silicon surface is very low (0.5%) and the reactive sticking coefficient was found to be almost independent of temperature [4.3]. Hence, it is suggested that the activation energy of overall silicon film growth from silane is due to surface processes in the decomposition mechanism that follows the chemisorption of silane [4.3]. On the other hand, adsorption of Si_2H_6 at room temperature on germanium surface increases monotonically with exposure time [4.4]. This suggests that the chemisorption of silane could be higher on germanium than on silicon. The result is the initial hetero-deposition rate of silicon on germanium can be different on silicon itself, that is, the deposition rate of silicon on germanium ($V_{Si/Ge}$) is higher than on silicon ($V_{Si/Si}$) [4.5]. In fact, Lee *et al.* has already demonstrated this phenomenon in the hetero-epitaxy of silicon on germanium [4.6]. This deposition property enables silicon to meet many of the above-mentioned criteria for successful germanium passivation.

Figure 4.2 illustrates how the deposition rate (a) and the film thickness (b) evolve along with the process time. At the beginning of the treatment, silicon is deposited on the germanium surface to form a monolayer at an accelerated rate ($V_{Si/Ge}$) due to the

presence of germanium. With the process time increases, silicon becomes deposited on the newly deposited silicon, resulting in a reduced rate ($V_{Si/Si}$). Integration of the deposition rate with respect to the deposition time yields the film thickness shown in Figure 4.2 (b) on the right side. The deposition starts right from the beginning. This means that, by carefully selecting the CVD process condition, the Si passivation process can be controlled in such a region that (1) silicon atoms completely cover the germanium surface before the subsequent deposition of silicon atoms on silicon; (2) the subsequent silicon deposition rate saturates to a low enough value to precisely control the silicon thickness in the angstroms region for gate oxide application.

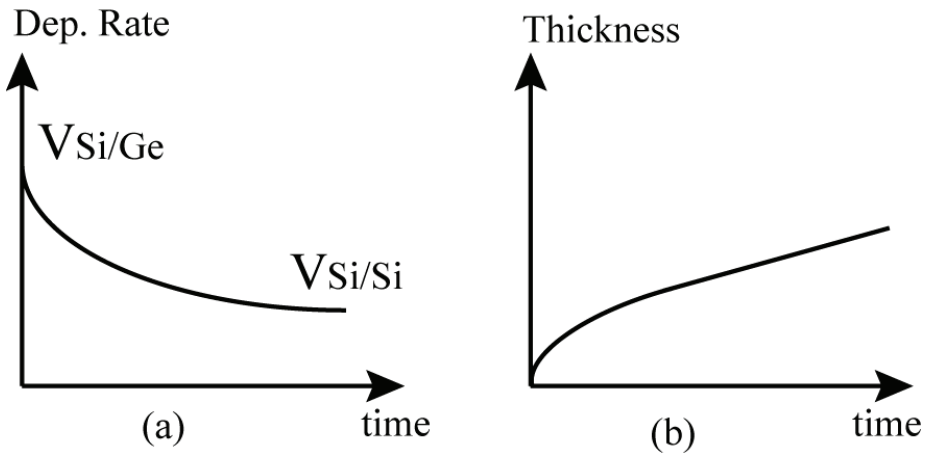


Figure 4.2 Deposition rate (a) and thickness (b) plotted against time of silicon deposited on germanium surface for passivation. By careful selecting of CVD condition, deposition rate of silicon on silicon ($V_{Si/Si}$) can be low enough for precise thickness control and complete surface coverage.

4.2 Evaluation of the suitability of silane treatment for passivation

From an engineering point of view, an effective silicon passivation on germanium must meet the following **four criteria**: **(1)** the germanium surface should be free of germanium oxide; **(2)** Silicon must completely cover the germanium surface; **(3)** The silicon passivation layer should be thin enough and consumed during the

subsequent high-k deposition so that the MOSFET channel is still kept in germanium; **(4)** Surface roughness must be kept to a minimum so that mobility enhancement due to germanium channel can be maximized. Therefore, the validity of the SiH_4 treatment shall be evaluated firstly.

4.2.1 Experiment

The purpose of the first experiment is to compare the substrate's effect on silicon deposition. Two types of samples were prepared. The Ge wafers were Sb-doped n-type wafers with a resistivity of 0.04-0.08 Ω-cm. The native oxide (GeO_2) was removed by dipping the sample in a diluted HF solution (1:50) for 5 minutes, followed by rinsing in de-ionized water [4.7]. The wafers were then deposited with silicon in a constant-temperature (450 ºC) CVD reactor with SiH_4 + N_2 flux at 5 Torr. The SiH_4 flow rate was 60 sccm and the N_2 flow rate was 250 sccm. Control experiments were also done on silicon wafers where 1000Å SiO_2 was firstly grown in a conventional furnace. CVD silicon was then deposited at a higher temperature to achieve a higher deposition rate. The CVD silicon thickness was measured by a *Sentech SE800* spectroscopic ellipsometer.

The second experiment is to verify the effectiveness of the silicon passivation for gate oxide application. The starting Ge wafers were also Sb-doped n-type wafers (resistivity= 0.04-0.08 Ω-cm). The native oxide (GeO_2) was removed by dipping the sample in a diluted HF solution (1:50) for 5 minutes, followed by rinsing in de-ionized water [4.7]. After that, the wafers were transferred to the same CVD reactor (base pressure = 3 mTorr) and annealed in the same SiH_4+N_2 ambient at 5 Torr for 60 seconds but with a lower temperature (400 ºC). Subsequently, the wafers were transferred to another chamber for the metal organic chemical vapor deposition (MOCVD) of HfO_2. The deposition was performed at 400 ºC using Hf tert-butoxide as

the metal organic precursor with O_2 flux (400 mTorr). A load-lock was used for wafer loading, un-loading and transferring between the process chambers. Because the load-lock is kept at a base pressure of ~$5x10^{-7}$ Torr, the SiH_4 surface passivation on the Ge substrate can be considered an *in-situ* process prior to the HfO_2 MOCVD. High-resolution *ex-situ* X-Ray Photoelectron Spectroscopy (XPS) analysis was performed using a *Physical Electronics Quantum 2000 Scanning ESCA Microprobe* with a monochromatic and standard Al X-ray source. Atomic Force Microscopy (AFM) was used to examine the surface morphology.

4.2.2 Results and discussion

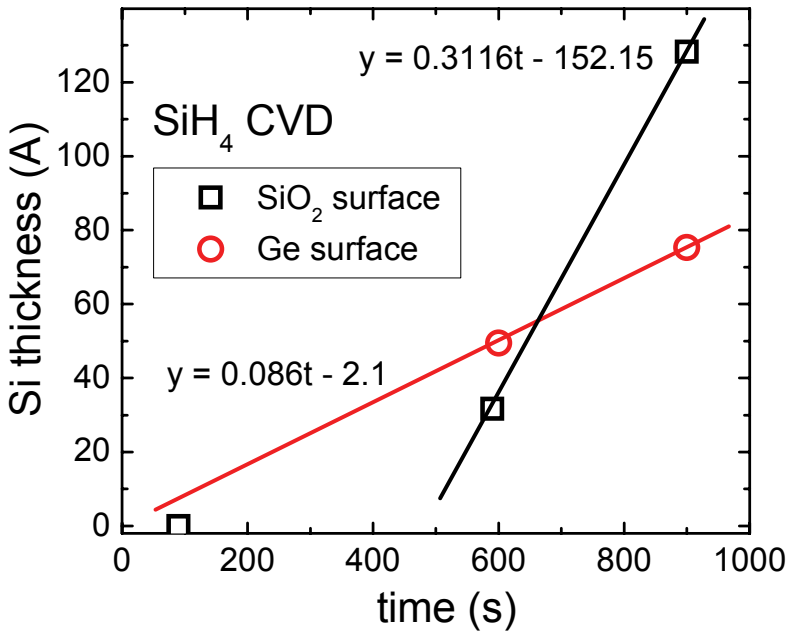


Figure 4.3 Experimental result of chemical vapor deposition of silicon on SiO_2 surface or on germanium surface. An almost zero incubation time is observed on germanium surface even though the deposition rate is lower than that of on SiO_2 surface.

Figure 4.3 shows the CVD silicon thicknesses in the first experiment. For CVD Si on SiO_2 surface on the silicon wafer (square points), there is no deposition with the process time of 90 seconds. Duration of 590 seconds and 900 seconds resulted in 31.7

Å and 128.3 Å, respectively. Assuming the deposition follows a linear relationship with deposition time once it starts, the silicon thickness can be described by an equation y=0.3116t-152.15. It can be found that the deposition on SiO_2 surface starts at ~ 488 second. This incubation time is attributed to the fact that the continuous deposition requires initial nucleation of silicon atoms from the SiH_4 gas molecules onto the solid SiO_2 surface, which in other words can be expressed as $V_{Si/SiO2} < V_{Si/Si}$. Incubation time generally increases with decreasing deposition rate (by for instance, reducing temperature in this experiment). However, the Si deposition on germanium surface exhibits a different trend. Although the deposition rate is lower (due to a lower process temperature), the deposition was found to start almost at the beginning (y=0.086t-2.1). The small positive incubation time that is different from Figure 4.2(b) might be due to the limited number of available data points. Nevertheless, the result suggests that silicon passivation could be possible if the process time is scaled down.

The second experiment further evaluates the SiH_4 treatment with reduced process time and temperature. Figure 4.4 shows the Ge 2p3 XPS spectra of the sample just after DHF cleaning and the sample after the SiH_4 surface passivation. The inset is the Si 2p XPS spectrum of the sample after the SiH_4 surface passivation. As can be seen, a Ge-O peak [4.8] can be observed on the sample immediately after DHF cleaning, which suggests that germanium oxide forms immediately after wet cleaning, which means the germanium surface shown in Figure 4.1(b) actually never exists in atmosphere at room temperature. However, the Ge-O peak observed on the DHF as-cleaned Ge surface disappeared after the SiH_4 treatment. Moreover, the Si-passivated Ge surface was stable even when the sample was exposed to the air. The existence of silicon is confirmed by the Si 2p spectrum of the same sample, as shown in the inset. This Si signal includes two types of bonds [4.8]: one is the elemental Si, and the other

is SiO_x. Based on the above result, the germanium surface is free of germanium oxide after the SiH_4 treatment, because otherwise, a Ge-O peak would have been observed. Thus, **Criterion (1)** is fulfilled. Further, **Criterion (2)** says that the germanium surface should be completely covered by silicon. The sample in the second experiment had been exposed to atmosphere but no oxidation of germanium was observed, which was different from what was seen in the as-cleaned sample. It should also be emphasized that silicon atoms were in direct contact with germanium atoms. As suggested by the single binding energy of the Ge 2p3 spectrum, because Ge-O bond formation would have been inevitable if silicon oxide is in direct contact with germanium. So the silicon oxide contributing to the Si-O peak in the Figure 4.4 inset should be induced by the air when sample was transferred from the CVD reactor to the XPS analyzer. Therefore, **Criterion (2)** is fulfilled.

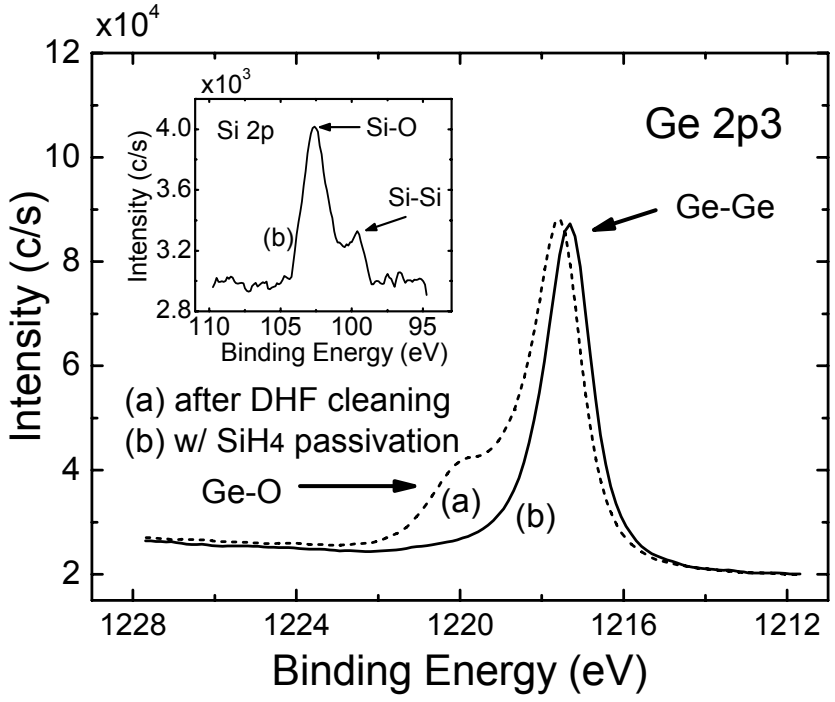


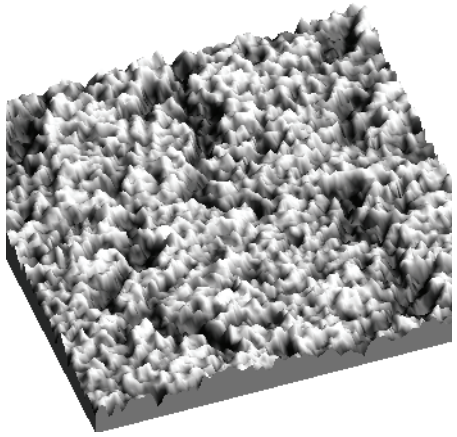
Figure 4.4 XPS analysis on the as-cleaned germanium surface (a) and on the SiH_4 treated germanium surface (b). The disappearance of the Ge-O peak tells that germanium oxide is removed after the SiH_4 treatment. The SiH_4 treatment also successfully results in an ultra-thin silicon passivation layer completely sealing the germanium surface and preventing the oxidation of germanium surface.

Although the sample structure described in Figure 4.1 (b) is not observed in the second experiment, the wafer structure described in Figure 4.1 (a) and (c) are confirmed. The absence of germanium oxide can be due to the following reasons. It is well known that Ge oxide is very unstable at moderately high temperatures (≥400 ºC) in vacuum. Therefore, it is possible that the germanium oxide is removed when the sample is heated in the hot chamber and before gases are supplied to raise the chamber pressure. Further, the extreme deficiency of oxygen in the SiH_4 CVD chamber may also enhance the tendency for reduction reaction of germanium in GeO_x.

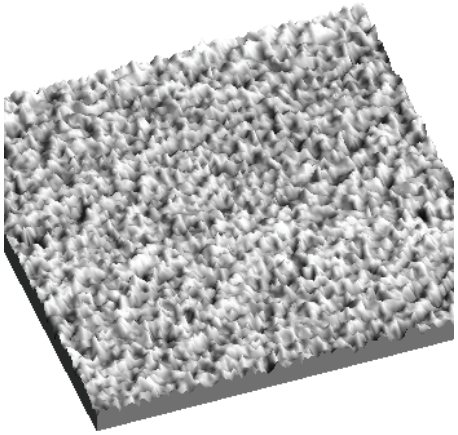
It is also noticed in Figure 4.4 that: (1) the intensity of the Si-O peak (~102.6 eV) is much lower (~65 times) than that of the Ge-Ge peak (~1217.4 eV) for the sample after passivation; (2) the Ge-Ge peak (~1217.4 eV) of the sample after passivation shows a negligible intensity reduction compared to the as-cleaned sample. Both imply that the amount of the top silicon is so little that the thickness is much less than the attenuation length of Ge 2p3 electrons traveling in silicon. The small value of the attenuation length [4.9] indicates the silicon layer should be only a few monolayers. Such result suggests that the passivation meets **Criterion (3)** by a self-limiting process condition at a temperature of ~400 ºC.

In order to examine the surface roughness, AFM analysis was performed on the fresh sample, the as-cleaned sample, and the Si-passivated sample. **Figure 4.5** shows the AFM results with a scanning area of 1μm x 1μm. As can be seen, the surface roughness is greatly reduced after the DHF cleaning (RMS=0.157 nm) [Figure 4.5 (b)] compared to the fresh sample (RMS=0.340 nm) [Figure 4.5(a)]. Besides, comparable surface roughness between the DHF-cleaned sample [Figure 4.5(b)] and the Si-passivated sample (RMS=0.166 nm) [Figure 4.5(c)] were observed. Such results can also be explained by the self-limiting nature of the Si passivation process which tends

to preserve the roughness of the germanium surface. Therefore, **Criterion (4)** is also fulfilled.



(a)



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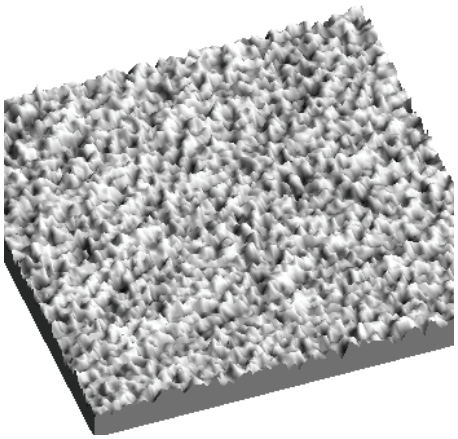

(c)

Figure 4.5 Comparison of wafer surface roughness by AFM. (a) the un-processed germanium wafer; (b) the as-cleaned germanium surface; (c) the SiH_4 treated germanium wafer.

Based on the above study, it is successfully demonstrated that the SiH_4 treatment can induce an ultra-thin silicon layer to seal the germanium surface. The next step is to study its effect on the material properties of the subsequently CVD deposited HfO_2.

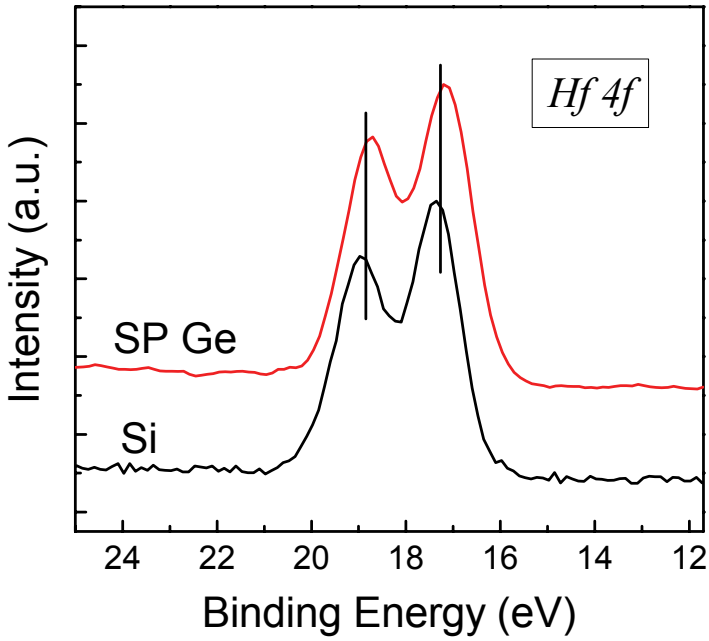

Figure 4.6 Hf 4f XPS spectra of MOCVD HfO_2 deposited on silicon and on SP treated germanium. No significant difference in the Hf 4f binding energy can be observed.

Figure 4.6 compares the Hf 4f XPS spectra of the HfO_2 deposited on the germanium substrate using silicon passivation (SP Ge) with that using silicon substrate (Si). No significant difference can be observed, suggesting that the silicon interlayer does not induce change of the HfO_2 film in terms of chemical states.

In the previous chapter, studies showed that germanium out-diffuses into MOCVD HfO_2 during the deposition when there is no surface treatment [4.10]. The effect of the SiH_4 surface passivation on this issue is studied using angle-resolved XPS analysis and shown in Figure 4.7. The sample after HfO_2 deposition without Si-passivation is included for comparison. Both samples are characterized at take-off angles of 10º and 90º, respectively. In order to have a fair comparison and since there

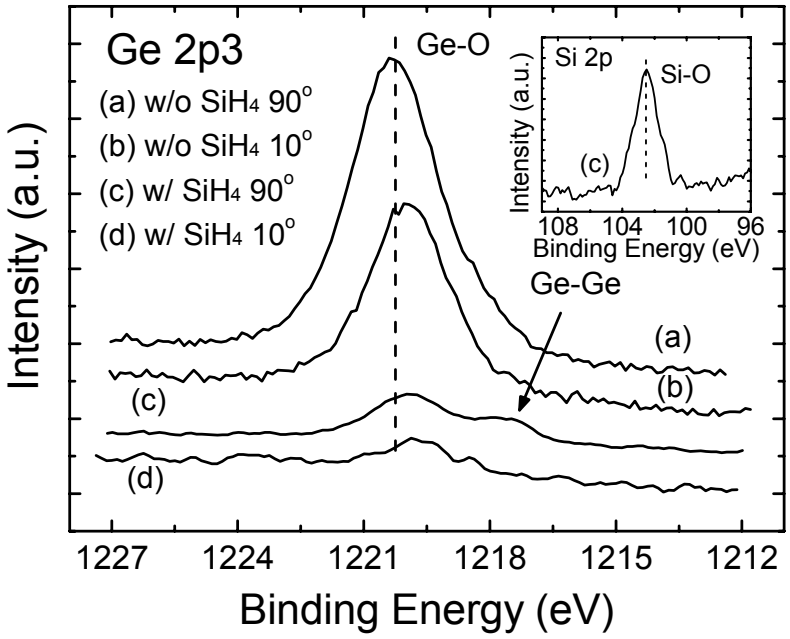

Figure 4.7 Ge 2p3 XPS spectra of the HfO_2 films deposited on germanium surface without (a, b) and with (c, d) silicon passivation. Germanium out-diffusion into HfO_2 can be significantly suppressed by silicon passivation.

is no difference in the binding energy between all the Hf 4f spectra (not shown), the Hf 4f spectra are normalized to the same level, and then, all the correspondent Ge 2p3 signals are scaled respectively with the same factors as the Hf 4f (shown in Figure 4.7). As can be seen, only the sample with Si passivation at the 90º take-off angle shows a two-peak spectrum [curve (c)], representing the elemental germanium and the germanium oxide states [4.8]. The detection of element Ge bonds indicates that the HfO_2 film on this sample is thinner than the sample without Si passivation [curve (a)]. Moreover, the Ge-O peak area of the Si passivated sample [curve (c)] is much smaller than that of the sample without passivation [curve (a)]. This means the passivation is very effective in suppressing formation of germanium oxide. The small take-off angle (10º) in the analysis was then used to examine the dielectric film. By comparing the intensities, the amount of Ge in the sample with Si passivation is much less than that of the sample without Si passivation. Therefore, it can be concluded that the

significant Ge out-diffusion during HfO_2 MOCVD is greatly suppressed by Si passivation. At the same time, only Si in its oxide state is detected (inset of Figure 4.7), indicating that there is no Hf-silicide formation at the interface, and the silicon was fully consumed to form the interfacial layer. On the other hand, it is difficult to tell the interfacial layer is silicon oxide or silicate based on the Si 2p signal. This is because in both case the silicon is in oxide states. In addition, there is no significant difference in the Hf 4f signals between the Ge sample and the Si sample (Figure 4.6). Therefore, there is no evidence of hafnium silicate at the interface from the XPS results. However, this doesn't necessarily mean that there is no silicate in fact, because the amount of the interfacial layer might be out of the detection limit of XPS.

4.2.3 Summary

A novel surface passivation by *in-situ* SiH_4 treatment on germanium is proposed and demonstrated successfully. The passivation relies on the formation of an ultra-thin silicon interlayer of approximately several monolayers directly on top of the germanium surface. The process meets the four Criteria stated earlier for successful surface passivation. This is verified by *ex-stiu* XPS and AFM analysis. Moreover, the silicon passivation is promising for Ge MOS application with high-k gate dielectric, as it shows that both formation of germanium oxide and out-diffusion of germanium into the gate oxide are greatly suppressed during HfO_2 deposition.

4.3 Performance of p-MOSFET on silicon-passivated germanium

Currently, there have been several successful demonstrations about Ge MOSFETs with a GeON/Ge interface. Shang *et al* has recently reported germanium

pMOSFETs with up to 40% mobility enhancement compared to Si universal data [4.11]. However, the gate dielectric used was GeON and the equivalent oxide thickness (EOT) is ~8 nm, which is not suitable for modern VLSI devices. Besides, several works (including this work) on Ge MOSFETs or MOS-CAPs with sub-2 nm EOT have been reported recently using HfO_2 recently [4.7], [4.10], [4.12], [4.13]. Hence, the evaluation of the electrical performance by silicon passivation shall be done by comparison with surface nitridation devices with sub-2nm EOT.

4.3.1 Experiment

The device fabrication flow is similar with what is described in Chapter 2 on (100) n-type wafers (Sb doped, 0.04-0.08 Ω-cm). Wafers were first cleaned by diluted HF (1: 50) and rinsed by DI water. Wafers were then passivated in SiH_4 ambient using the condition described in this chapter (silicon passivation, SP). To compare the effects of this surface treatment with surface nitridation, control wafers were prepared by annealing in NH_3 ambient (600ºC, 30 seconds, surface nitridation, SN) instead. After that, samples were transferred through a loadlock into a Metal-Organic Chemical Vapor Deposition (MOCVD) chamber under vacuum. Various thicknesses of HfO_2 gate dielectric was then deposited using Hf tert-butoxide as the precursor at the temperature of 400ºC on different wafers. Samples were then subject to different post-deposition anneal (PDA) conditions in order to study the PDA effect. One condition was 500 ºC, 200 Torr for 1 minute in N_2 ambient; the other condition is 500 ºC in N_2 at atmospheric pressure for 1 minute. A TaN gate electrode was then deposited by reactively sputtering of Ta in a N_2 + Ar ambient. Following that, a lithography process and Cl_2 plasma dry etching were employed to define and pattern the gate stack. Wafers were then implanted with boron (35keV, $1x10^{15}cm^{-2}$) to form a self-aligned source and drain (S/D). A dopant activation anneal was done in N_2 ambient at 420ºC. Finally,

forming gas annealing was carried out at 300ºC. No aluminum contact was employed in this experiment in order to simplify the device fabrication flow. Capacitance-voltage (C-V) characteristics were collected by an Agilent 4284A LCR meter and leakage current-voltage (J-V) curves were measured by a Hewlett-Packard 4156A semiconductor parameter analyzer. High-resolution cross-sectional transmission electron micrographs (HR-XTEM) were also taken to characterize the final gate stack.

4.3.2 Results and discussion

(a) Physical Properties

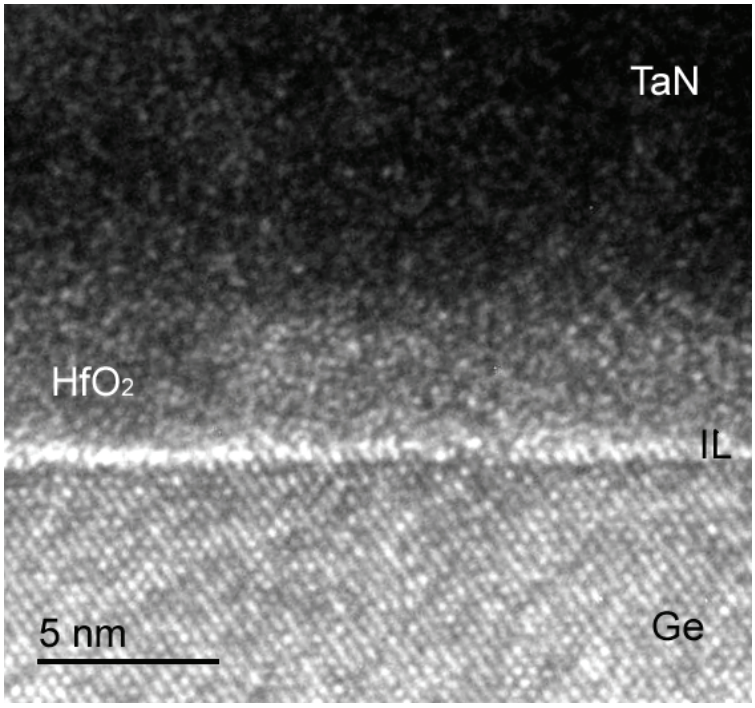

Figure 4.8 TEM image of the cross-section of the Ge MOS stack with silicon passivation. HfO_2 remains amorphous after the transistor fabrication flow.

Figure 4.8 shows the high-resolution transmission electron microscope (TEM) image of the TaN/HfO_2/Ge gate stack cross-section with 60 second Si-passivation. A uniform amorphous interfacial layer (IL) is observed. This is due to the fact that the Ge surface is fully covered with a few monolayers of uniform elemental silicon, and

this led to SiO_x formation during the HfO_2 MOCVD and the subsequent thermal processes [4.14]. It was also observed that the HfO_2 remains amorphous after device fabrication. This result is different from that with surface nitridation or direct deposition of germanium (Figure 3.5). The reason could be the amorphous IL that blocks the local epitaxial growth [4.15] and/or the significant reduction of germanium out-diffusion (thermal germanium oxide is poly-crystalline [4.16]).

(b) MOS Capacitor Properties

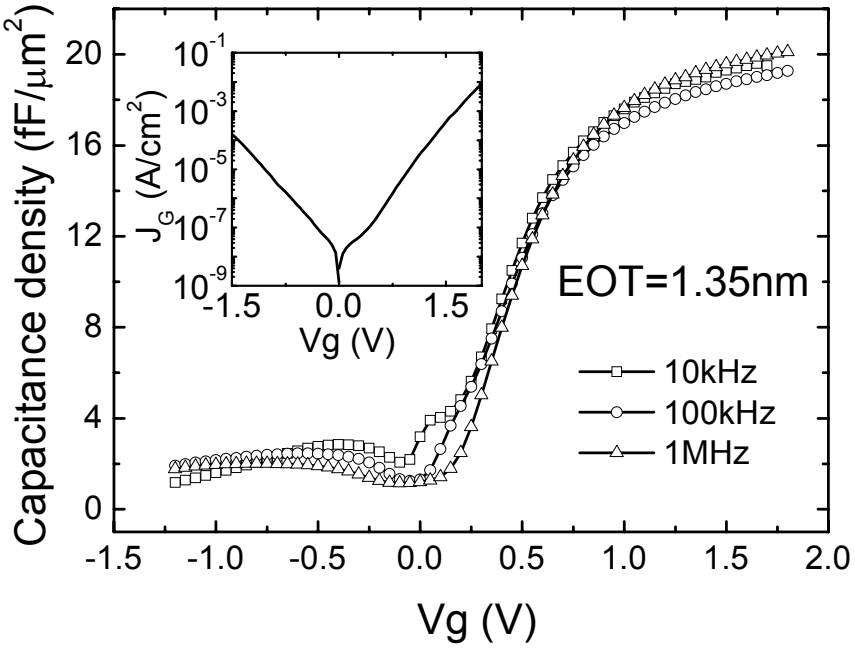

Figure 4.9 C-V and I-V (inset) characteristics of the Ge p-MOS capacitor with silicon passivation. Frequency dispersion is only observable near the inversion region.

The C-V and I-V characteristics of the SP TaN/HfO_2/Ge MOS capacitor (area=100μmx100μm) with PDA at 1 Atmospheric pressure are shown in Figure 4.9. The capacitance was measured by sweeping the gate bias from inversion to accumulation. There is no substantial frequency dispersion across the entire measurement region in contrast to ref. [4.15]. However, a small kink can be observed

when the measurement frequency is reduced to 10 kHz, indicating there are some "slow" interface states near the valence band (E_V) [4.17]. An EOT of ~13.5 Å is obtained after comparison with simulation which took into account of quantum-mechanical effects [4.18]. The leakage current as a function of gate bias is shown in the inset figure. A leakage current of 1.16×10^{-5} A/cm^2 was achieved at 1V gate bias. The good performance of I_g-EOT shows the potential of SiH_4 surface passivation for HfO_2 scaling in forming future ultra-scaled gate stack on germanium, as compared to direct HfO_2 deposition.

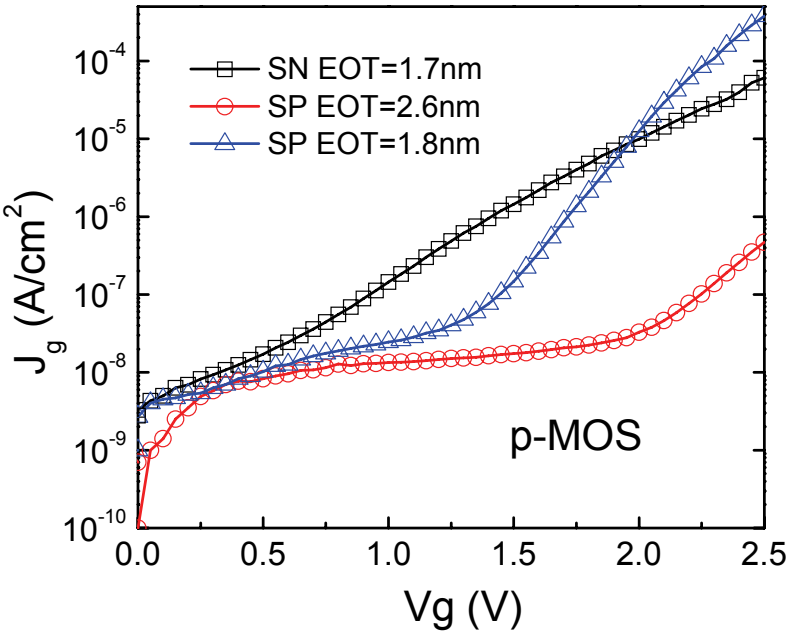

Figure 4.10 I-V characteristics of Ge p-MOS capacitors with different surface treatments. The circled line represents the SP device with the same duration of HfO_2 deposition as the SN device as shown by squared line. The triangled line shows the SP device with reduced duration of HfO_2 deposition to achieve a similar EOT with the SN device.

Figure 4.10 shows the gate current density, measured when the capacitor was biased in the accumulation region, as a function of gate voltage of both SN and SP processed capacitors. The circle-dotted line refers to the SP samples with identical HfO_2 deposition time with the SN samples shown by square-dotted line. The EOT of

the SN sample (1.7 nm) is smaller than that of the SP sample (2.6 nm). There could be three reasons for this EOT difference. The first one is that the permittivity of the GeON IL obtained by the SN technique is higher than that of the silicate-like IL from the SP technique [4.19]. The second reason could be the physical IL thickness. It was found that the IL growth is not substantial for the SN technique probably because of the presence of nitrogen. This has been confirmed by TEM in the previous chapter as well as in a similar analysis by Gusev *et al* [4.20]. On the other hand, it is well reported that silicon is prone to IL growth when HfO_2 is directly deposited on it. As a result, the SN IL could be physically thinner that the SP IL. The third reason might be related to the crystalline structure of the gate dielectrics. It is already observed that the HfO_2 layer is more crystallized for the surface nitrided device (Fig. 3.4(a)), whereas that for the silicon passivated device is relatively amorphous (Fig.4.8). A greater degree of crystallization could result in a higher permittivity, thus resulting in a smaller EOT. These three effects can add up together and finally contribute to the ~0.9 nm difference in EOT. Therefore, it should be reasonable to observe a higher leakage current of the SN device than the SP device. Another SP device was fabricated with a reduced HfO_2 deposition time in order to achieve a similar EOT with the SN device. Its J-V characteristic is shown by the triangle-dotted line. It can be observed that the SP device has a lower leakage current when the gate bias is below ~2V. Therefore, SP is still superior to SN because the power supply used in modern VLSI circuits is lower than 2V.

The MOS capacitors with post-deposition anneal (PDA) under *reduced* pressure were used to further compare the robustness between the surface treatments. The gate leakage currents at +1V gate bias were measured and compared across the whole wafer. Devices were randomly selected and the cumulative probabilities were then

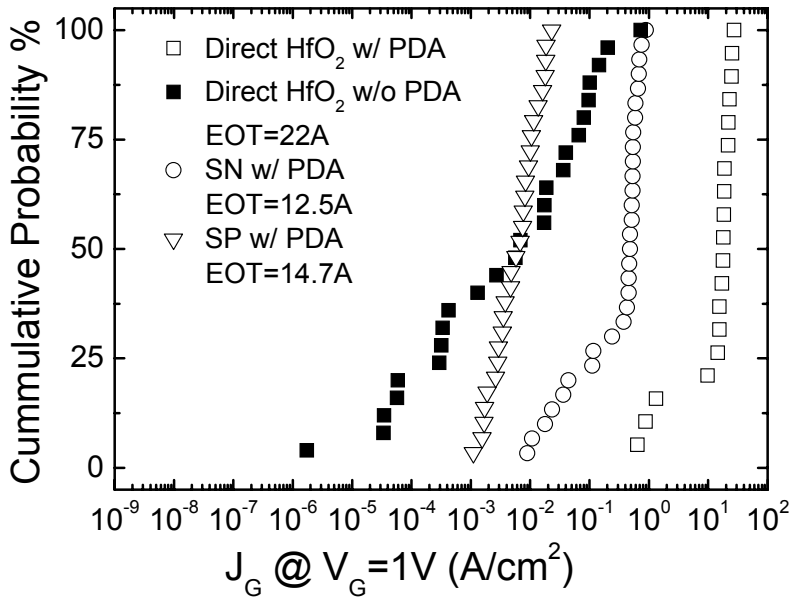

Figure 4.11 Cumulative percentage of the leakage current of the Ge MOS capacitors fabricated with different technology. When there is no surface treatment, PDA results in initial breakdown of the Ge MOS capacitors. Nitridation improves the process robustness and silicon passivation shows the best process robustness.

plotted in Figure 4.11. It is observed that the devices without any surface treatment (direct HfO_2 w/o PDA) had a wide distribution in leakage currents. This could be due to the formation of the unstable germanium oxide during the HfO_2 deposition. Post deposition annealing leads to initial breakdown of the devices when there was no surface treatment. This is illustrated in Figure 4.11 as the distribution with the highest leakage currents. The devices with surface nitridation exhibit an improved distribution. However, it is noticed that there is a tail in the distribution at low leakage region, where the tail has a similar slope as the devices with direct HfO_2 deposition (without post-deposition annealing). On the other hand, the devices with SP process show the narrowest distribution in leakage current, indicating that the SP process is more robust than the SN process. The improved leakage distribution is believed to result from the significant suppression in the formation of the unstable germanium oxide at the

interface [4.14] as well as the formation of a uniform amorphous interfacial layer after the SP process which is observed in Figure 4.8.

Figure 4.12 summarizes the leakage currents of all the MOS capacitors in this experiment. The gate leakage currents of the p-MOS capacitors at $|V_g-V_{fb}|=1V$ under accumulation were plotted as a function of the equivalent oxide thickness (EOT). The theoretical gate leakage currents of SiO_2/Si and HfO_2/Si systems attributed to direct tunneling mechanism were also plotted with solid lines for reference. Once again, direct CVD HfO_2 on germanium results in a large gate leakage current that is higher than that of thermal SiO_2 on Si at the same moderate EOT. The formation of unstable germanium oxide during the HfO_2 CVD is the main cause of this large leakage. The

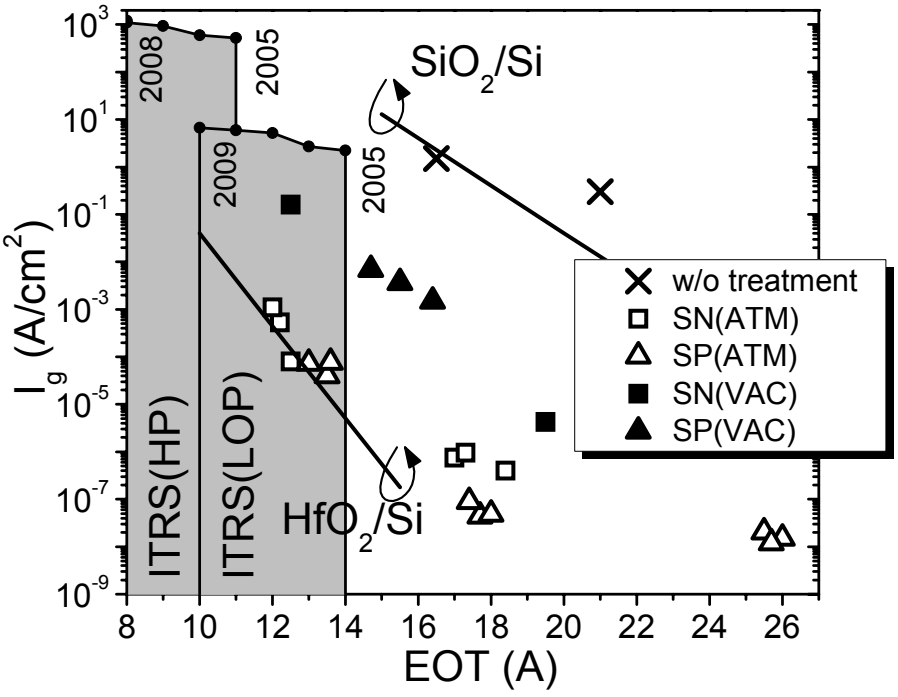

Figure 4.12 I_g-EOT performance of Ge p-MOS capacitors w/ different surface treatments, and w/ different PDA conditions: Atmospheric pressure (ATM) and reduced pressure (VAC). The performance is benchmarked with the theoretical direct tunneling current of SiO_2/Si and HfO_2/Si systems. The leakage requirements for high-performance logic application (HP) and for low operating power application (LOP) that are projected in ITRS 2004 in the near future are shown in shadow area.

large gate leakage current can be reduced significantly by ~6 orders of magnitude by using either surface nitridation or Si passivation, as shown in Figure 4.12 with empty data points (atmospheric PDA). There is not much current increase when the EOT is scaled from 25Å to 18Å, because the dominant conduction mechanism is not direct tunneling in this range. Below 18Å, the leakage starts to increase exponentially. The SN devices behave in a similar way in the EOT range smaller than 18.5Å, but the leakage currents are always slightly higher than those of the SP devices in the same EOT region. This is consistent with the result in Figure 4.10. Since the total dielectric permittivity obtained by SN technique should be larger than that of SP technique ($k_{GeON}>k_{SiOx}$), this higher leakage may imply that the SN technique results in either a trappier dielectric (for Frenkel-Poole tunneling) or a poorer electron barrier near the interface. Further evaluation will be required to clarify the reason for this. Nonetheless, although the two surface passivation techniques both result in slightly higher leakage currents than the theoretical direct tunneling leakage of the HfO_2/Si system, the extrapolation also suggests that the gate leakage currents can still meet the requirements of both high performance (HP) and low operation power (LOP) MOSFETs at the year 2009 according to the International Technology Roadmap for Semiconductor (ITRS2004, shadow region in Figure 4.12). Further scaling of EOT can be achieved by thinning down the physical thickness of the high-κ layer. On the other hand, it is also found that the leakage current strongly depends on the PDA ambient pressure. The leakage currents increase 2-3 orders of magnitude when the devices were annealed at reduced pressure (VAC) of 200 Torr, as shown by solid data points. The reason could be related to the enhanced decomposition of germanium oxide at the oxide/semiconductor interface. This result provides important guideline in selecting thermal processes for Ge MOSFET fabrication.

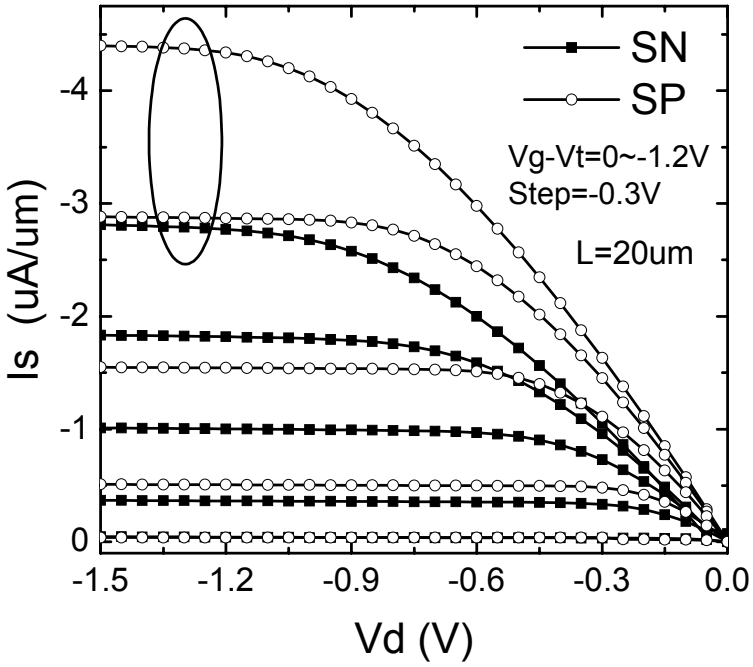

Figure 4.13 I_D-V_D characteristics of Ge p-MOSFET fabricated with different surface treatments. Squared line represents the device with surface nitridation (SN); circled line represents the device with silicon passivation (SP).

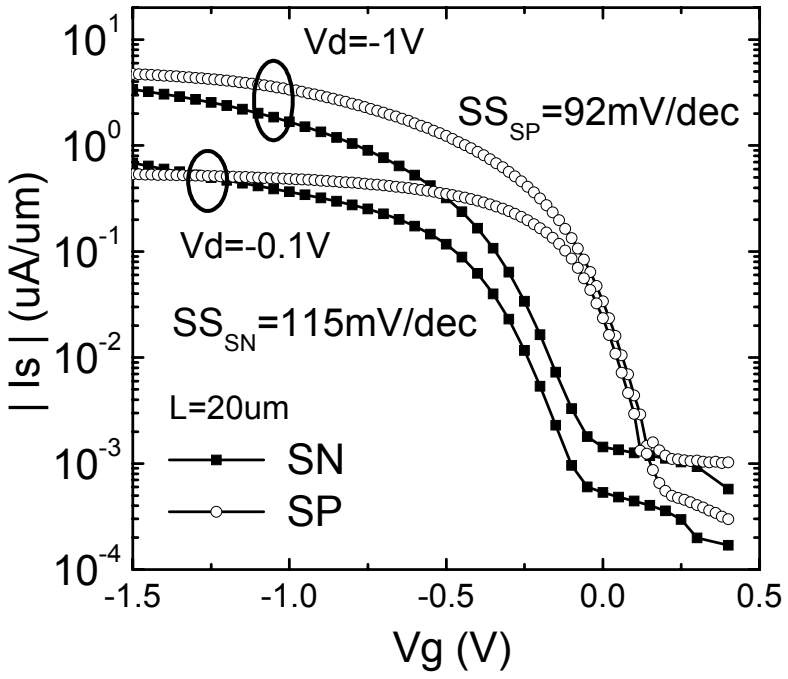

Figure 4.14 I_D-V_G characteristics of Ge pMOSFET fabricated with different surface treatments. Squared line represents the device with surface nitridation (SN); circled line represents the device with silicon passivation (SP).

(c) MOSFETs Properties

Typical output characteristics of the pMOSFETs with both SP and SN processes are compared in Figure 4.13. The EOTs are 15.5Å and 12.5Å for the devices with SP and with SN respectively. The SP processed pMOSFET shows a ~56.4% higher drive current than the device with SN at bias of V_{gs}-V_{th}=-1.2 V and V_{ds}=-1.5 V. Figure 4.14 compares the transfer characteristics between the two surface treatments. SP results in a better sub-threshold swing (SS) than SN, implying that the interface trap density should be lower. One can also notice that the threshold voltage (V_{th}) of the SP MOSFETs is closer to the ideal value, considering the gate workfuction (TaN) [4.21] and the substrate doping. Therefore, there is significant positive fixed charge in the surface nitride layer of the SN MOSFET. Our result is consistent with Cho *et al.*'s result on silicon substrate [4.22].

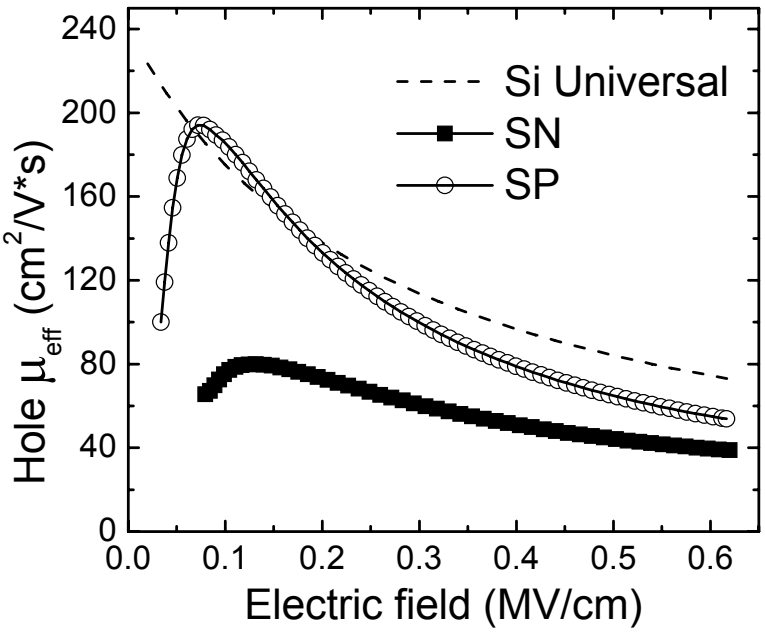

Figure 4.15 Comparison of effective hole mobility resulted from different surface passivation. Squared line represents the device with surface nitridation (SN); circled line represents the device with silicon passivation (SP).

The effective mobility (μ_{eff}) was extracted using the split CV technique. The channel current under different gate biases was estimated by (I_D+I_S)/2 with the V_{DS}=-50mV [4.23] due to the high gate leakage. The charges (Q_{inv} and Q_B) were extracted from CV measurement at 100 kHz. The effective electric field normal to the channel was then estimated as E_{eff} = (Q_B+Q_{inv}/3)/ε_{Ge}, where Q_B is the depletion-charge and Q_n is the inversion charge. Figure 4.15 plots the μ_{eff} versus E_{eff} for both SN and SP devices. The SP processed device exhibits a much higher effective hole mobility than that of the SN process device. The peak hole mobility for SN and SP processed MOSFET are 79.9 cm^2/V-s and 194.1 cm^2/V-s respectively. A ~140% improvement in peak hole mobility was achieved in SP processed Ge MOSFET compared to that that in the SN processed Ge MOSFET. This could be due to the significant reduction of Coulomb scattering, because silicon passivation is more effective than surface nitridation in reducing fixed charge and interface traps. There is an issue that the SP mobility drops more rapidly than the SN mobility for increasing electric field. By comparing the transistors with different channel lengths, it was found that this could be due to the large contact resistance in the direct probing of the source/drain area from the measurement instrument. Therefore, the mobility values could be underestimated. Adding a contact metal, such as aluminum, could help to increase the measurement accuracy. This will be addressed in the next chapter.

4.4 Conclusion

A novel surface passivation by *in-situ* SiH_4 annealing prior to high-k deposition was proposed and demonstrated for Ge MOS applications. The technique introduces an ultra-thin silicon layer with several monolayers to fully seal the germanium surface, which was verified by *ex-situ* XPS and AFM analyses. Germanium remained un-

oxidized after the silicon passivation (SP) process and the formation of germanium oxide was greatly suppressed during the subsequent HfO_2 deposition. There is also no significant difference in chemical states between the HfO_2 bulk deposited on SP Ge surface and that deposited on silicon surface. However, when it is compared to surface nitridation (SN) in the previous chapter from a material point of view, SP is superior because it can greatly suppress germanium out-diffusion and the HfO_2 film remains amorphous after the entire device fabrication flow.

TaN/HfO_2/Ge pMOS-capacitors and pMOSFETs with SP were fabricated to study the electrical characteristics, and compared to those using SN surface treatment. In the sub-2nm region, SP reduces the gate leakage current significantly and results in a slightly better Ig-EOT performance than SN. The more important advantage of silicon passivation is that it leads to low fixed charge as well as interface trap charge. As a result, the p-MOSFET exhibits higher drive current, smaller sub-threshold swing, and higher hole mobility than that with surface nitridation. These electrical results reveal the potential of the Ge MOS system with SiH_4 surface passivation for future ultra-scaled VLSI devices.

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Chapter 5

Development of Germanium n-MOSFETs

All the studies in this thesis which have been discussed so far were on germanium p-MOSFETs, but n-MOSFET is also required for CMOS applications. However, a literature survey shows that historically there have been very limited reports on germanium n-MOSFETs due to limitation in the material quality in the process technology.

There have been two encouraging reports: Rosenberg *et al.* fabricated a self-aligned Ge n-MOSFET with GeON gate oxide in 1988 and inferred an electron low field mobility of ~940 cm^2/V-s [5.1]; Ransom *et al.* also reported an electron mobility higher than 1000 cm^2/V-s in 1991 [5.2].

Table 5.1 Recent results of Ge n-MOSFETs reported by different research groups.

Research Group	Gate oxide	EOT (nm)	Gate length (um)	Drive current (uA/um) @ V_{GS}-V_{th}=1 V
Chui *et al.* [5.3]	HfO_2 w/ SN	2.2	2	6.5
Ritenour *et al.* [5.4]	HfO_2 w/ SN	1.8	10	0.014
Shang *et al.* [5.5]	GeON	8.0	100	0.0044
Yu *et al.* [5.6]	$LaAlO_3$	1.4	10	28

However, these results seem to differ from several recent reports of Ge n-MOSFET, where much poorer performance was obtained. This is summarized in Table 5.1. Chui *et al.* have demonstrated a germanium n-MOSFET with metal-gate and high-k dielectric recently in 2003 [5.3]. The EOT was 2.2 nm for the HfO_2 transistor, but the drive current (I_s) was only ~6.5 μA/μm @ V_{GS}-V_{th}=1 V with a gate length of 2 μm. This implies that the measured result of the electron mobility is ~5

times lower than the hole mobility demonstrated in the last chapter. Consistently, Ritenour *et al.* reported a similar result for a TaN/HfO_2/Ge n-MOSFET [5.4]. The output current (I_s) was 0.014 μA/μm @ V_{GS}-V_{th}=1 V with a gate length of 10 μm. Considering the ~1.8 nm EOT in Ritenour's work, it suggests that electron mobility is even substantially lower than Chui's result. The above two reports were both using surface nitridation (SN) technology, which introduces a GeON layer in between HfO_2 and Ge channel. Shang *et al.* reported Ge n-MOSFET using only GeON as the gate dielectric [5.5]. The resultant electron mobility was higher than the result from the previous two research groups, reaching 100 cm^2/V-s at low electric field. However, it is still un-reasonably low when it is compared to the theoretical value. The highest electron mobility was reported recently by Yu *et al.* on a germanium-on-insulator (GOI) substrate [5.6]. The electron mobility there was comparable with the silicon universal curve at 1 MV/cm vertical electric field. Yu *et al.* used $LaAlO_3$ as the gate oxide, which is different from CVD HfO_2 and GeON. The gate oxide formation technology is also different. The $LaAlO_3$ gate dielectric was deposited by physical vapor deposition from a $LaAlO_3$ source followed by 400 ºC oxidation [5.7]. Therefore, it may suggest that the gate stack formation technology could be a critical technology for successful fabrication of Ge nMOSFET with higher electron mobility than the silicon countpart.

In this chapter, the major difficulty of the gate stack for n-channel operation is first studied by further comparing the two surface treatments developed in the previous chapters. Subsequently, the silicon passivation technology is further explored to understand its limitations.

There is another issue in Ge n-MOSFET which is associated with the n+/p junction for the source/drain, as mentioned in Chapter 1. The difficulty arises mainly

from the dopant solid solubility and its activation. Generally it is found that the activation temperature for n-type dopants in germanium should not be lower than 450 ºC either by rapid thermal processor (RTP) or by furnace [5.5][5.8]-[5.10], which is higher than that of p+/n junctions. In previous demonstrations of Ge n-MOSFETs, Chui *et al.* [5.3] and Yu *et al.* [5.7] both used a gate-last approach which forms n+/p junctions before the high-k gate stack on germanium in order to avoid possible gate stack integrity problems. However, this gate-last approach is not promising as it is different from the current gate-first approach in modern CMOS technology. Therefore, if a gate-first approached is adopted, it is also necessary to evaluate the gate stack integrity after the the thermal processes used in source and drain activation. In other words, the gate stack technology should also be able to achieve or maintain the high performance and the integrity after the entire process flow.

5.1 Comparison of the two surface treatments

The study here needs to consider two kinds of substrates (n- and p-type) and two kinds of surface treatments, surface nitridation (SN) and silicon passivation (SP). Hence, it is necessary to fabricate at least four samples to have a thorough comparison of the two surface treatments.

5.1.1 Experiment

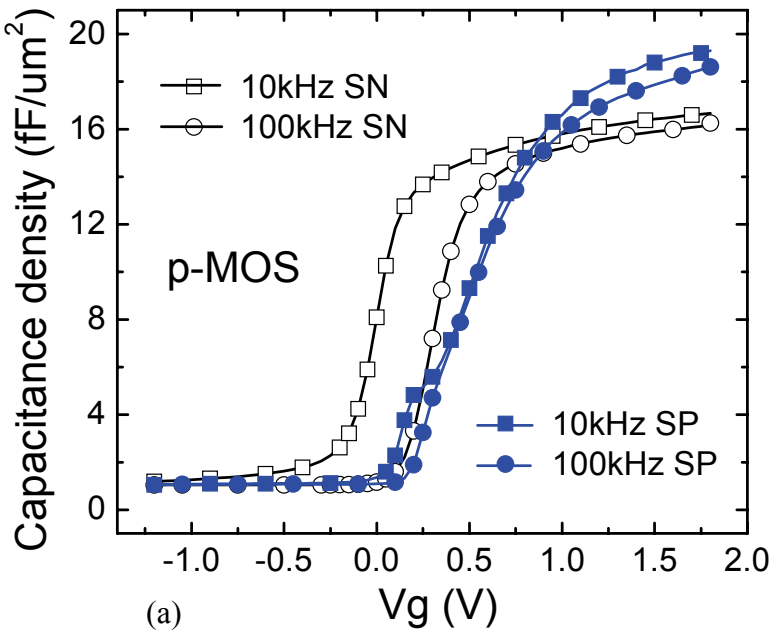
MOS capacitors were fabricated on both n- and p-type substrates. The starting Ge wafers are either Sb-doped n-type (100) wafers (0.04-0.08 Ω·cm) or Ga-doped p-type (100) wafers (0.09-0.18 Ω·cm). After pre-clean, the wafers were processed with different surface passivations: Surface nitridation at 600 ºC; Silicon passivation at 450 ºC. The subsequent processes were the same as those in the previous studies, except a

back-side aluminum deposition followed by the forming gas annealing at 350 ºC. I-V and C-V characteristics were measured by a HP4196 semiconductor parameter analyzer and an Agilent 4284 LCR meter.

5.1.2 Results and discussion

Figure 5.1 (a) shows the typical C-V measurement result of p-MOS capacitors. It is known that, if the leakage was low enough, the impact of the parasitic series resistance on the measurement would be small, and thus, the capacitance value under accumulation with different frequency (10 kHz and 100 kHz here) would converge [5.11]. The first anomaly observed in Figure 5.1 (a) is that there is frequency dispersion in depletion and weak-inversion regions for the SN device. As a result, it seems that the flat-band voltage (V_{fb}) measured at 100 kHz shifts by +0.31 V as compared to that of 10 kHz. In contrast, this phenomenon is much less evident for the devices processed by the SP technique. The V_{fb} difference between the two frequencies can be as low as ~0.01V. It needs to be mentioned that the capacitance of the SP device is larger than that of the SN device, which might contribute to the reduction of V_{fb} difference if this frequency dispersion originates from the semiconductor surface caused by the surface treatments. However, an 11% increase of capacitance from 16.7 fF/um^2 (SN) to 18.6 fF/um^2 (SP) cannot lead to a 0.3V (=0.31V-0.01V) decrease of V_{fb} dispersion. Hence, the reduction of V_{fb} frequency-dependence must be attributed to other factors besides the MOS capacitance. The second anomaly is that a small kink is observed near the inversion region for the SP device. Figure 5.1 (b) shows the typical C-V measurement results of n-MOS capacitors. Frequency dispersion of V_{fb} is not observed for either device. Instead, it is observed that there is a large amount of abnormal charge in the inversion region for the SN device irrespective of measurement frequency, while this is not observed with

the SP device. The capacitor with SP technique only exhibits a small kink near the inversion region with frequency dependence.



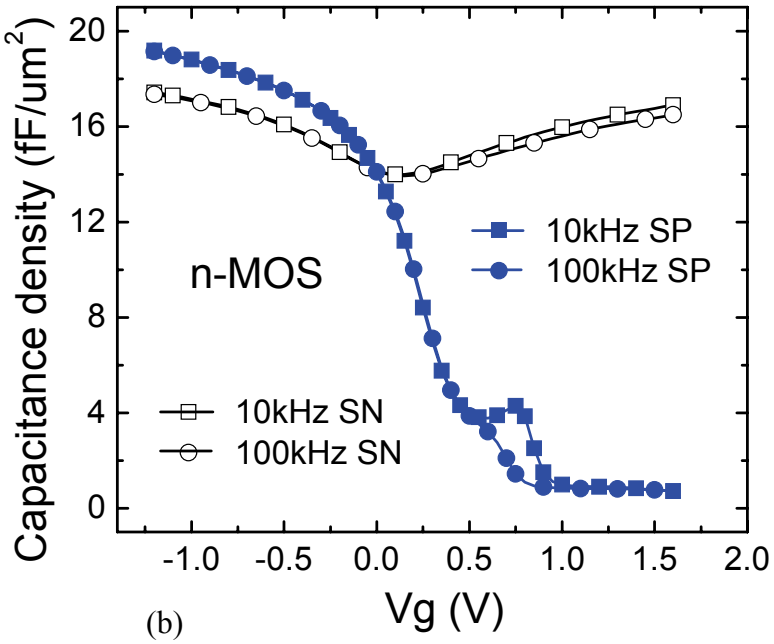


Figure 5.1 C-V characteristics of Ge p-MOS (a) and n- MOS (b) capacitors with different surface passivation. The devices were measured under different frequency (10 kHz and 100 kHz). Normal MOS system can be achieved on germanium with SP technique.

5.2 Model of the phenomena

The above anomaly of both n- and p-MOS capacitors can be interpreted by a simple model. In this model, there are quite a number of interface states located at the upper half of the semiconductor band gap, and the density (D_{it}) is much higher than the lower half of the band gap. This is illustrated in Figure 5.2. For simplicity, the interfacial layer is not shown. Figure 5.2(a) shows the p-MOS capacitor under flat-band condition. The high density interface traps in the upper half band gap lead to a stretch-out effect of the C-V curve from accumulation to mid-gap [Figure 5.2(b)] when the measurement frequency is low (10 kHz), as compared to the curve under the high frequency (100 kHz). It gives an illusion that the V_{fb} shifts towards the negative direction when the measurement frequency decreases, due to the capacitance contribution from the interface traps. This corresponds to the SN capacitor in Figure 5.1(a). If the interface trap density in the upper half band gap decreases, the frequency dispersion for p-MOS decreases [the SP capacitor in Figure 5.1(a)]. Under such circumstances, the interface traps in the lower half band gap contributes to the small kink that is observed with the 10 kHz C-V curve.

As for the case of n-MOS [energy diagrams shown in Figure 5.2 (c) and (d)], the same interface state model can be applied. For SP n-MOS, when the Fermi level is swept from the edge of valence band towards the mid-gap where the majority interface states (above the mid-gap) are above the Fermi level and do not contribute to the capacitance, the resultant capacitance at these biases is independent of measurement frequency, as observed in Figure 5.1(b). When the Fermi level crosses the mid-gap and approaches the upper half of the interface states (inversion), these interface states can lead to a kink in the C-V curve, where the size depends on the measurement frequency [the SP device in Figure 5.1(b)]. If this interface trap density increases, the kink in the

C-V curve increases as well under the same frequency. At the same time, a higher positive gate bias would be needed to fill up the states below the Fermi level before C_{min} is observed. From this point of view, the abnormal charge for the SN capacitor in the inversion region can be attributed to the high density interface states that lead to a very large kink which extends beyond the measurement range.

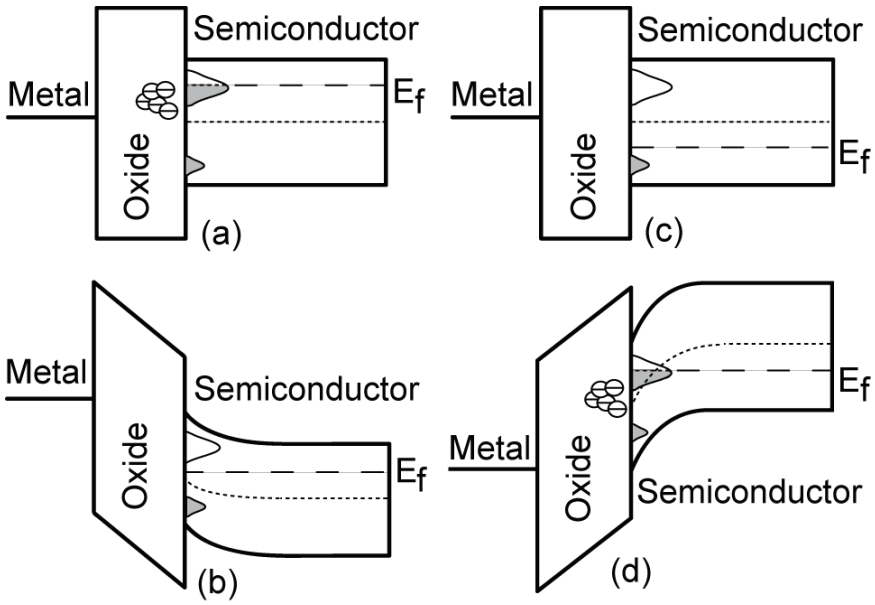


Figure 5.2 Energy band diagrams of MOS system with asymmetrical distribution of interface trap density along the bandgap. (a) p-MOS under flat-band; (b) p-MOS near weak inversion; (c) n-MOS under flat-band; (d) n-MOS near strong inversion.

With this model, one can speculate that there could be significant degradation of electron mobility but less degradation of hole mobility. Bardeen introduced the concept of interface neutral Fermi level (V_{FN})* [5.12]. For Ge, V_{FN} is at about $E_V+(1/3)E_g$ when the interface trap density is high enough [5.13]. This implies that the interface traps in the upper half of band gap with much higher density are acceptor traps. For n-MOSFET in the inversion case [Figure 5.2(d)], the interface traps are occupied by the electrons and therefore become negative charge centers, contributing to additional Coulomb scattering and mobility reduction. On the other hand, for p-

* Interface neutral Fermi level: the position of the Fermi level at the semiconductor surface for which there is no net charge.

MOSFET in the inversion case [Figure 5.2(b)], the interface traps are emptied and are neutral, and hence there is no contribution to Coulomb scattering. At the same time, these traps must be filled before the surface is inverted (generation of free inversion carriers). Consequently, one can also expect significant increase of threshold voltage due to the high density interface traps. Therefore, based on the previous qualitative study in **Section 5.1**, it can be concluded that surface passivation plays a critical role in obtaining a proper Ge n-MOS system for transistor operation.

5.3 Engineering of the silicon passivation layer

This section will show how the proper working of the Ge n-MOS system in **Section 5.1** was achieved by controlling the thickness of the silicon passivation layer.

The silicon layer works in such a manner that it is consumed to form the interfacial layer before the underneath germanium is oxidized. The experiment was carried out by fabrication of p- and n-MOS capacitors with different thicknesses of silicon passivation layer, as well as different HfO_2 thicknesses. The thickness variation of the silicon layer was achieved by varying the duration of SiH_4 annealing. Three thicknesses were used, named with SP-1, SP-2, and SP-3. The same approach of varying deposition duration was used to change the HfO_2 thickness. Two thicknesses were used, named with HfO_2-1 and HfO_2-2. Monitor Ge wafers were processed together for the measurement of the silicon layer thickness. Electrical characteristics of the capacitors were then investigated, using the measured Si thicknesses for reference.

5.3.1 Measurement of the silicon passivation layer thickness

It is essential to physically characterize the silicon passivation layer (thickness measurement). While ellipsometry can be used to measure the HfO_2 thickness, it is incapable of accurately measuring the Si thickness due to the ultra-thin nature of the

surface layer (<10Å), nor is TEM which requires complex sample preparation and is destructive to the surface film. In such a case, XPS is a useful approach for fast and nondestructive measurements.

The thickness measurement of a surface film on a substrate by XPS is derived from the exponential attenuation of photo-electrons by the overlying film [5.14], which is a good approximation when the take-off angle (θ) is between 30º to 90º. Hence, there is:

$$C_S/S_S=\exp(-t/\lambda_S \sin\theta) \tag{5.1}$$

and,

$$C_0/S_0=1-\exp(-t/\lambda_0 \sin\theta) \tag{5.2}$$

where t is the overlayer thickness; C_0 and C_S are the intensities of the respective XPS spectra in the ovelayer and in the substrate; λ_0 and λ_S are the attenuation length of photo-electrons within the overlayer that originated in the overlayer and in the substrate, respectively; and S_0 and S_S are their sensitivity factors. Combining (5.1) and (5.2) yields,

$$\ln\left(\frac{C_0/S_0}{C_S/S_S}\right)-\left(\frac{\lambda_0}{\lambda_S}-\frac{1}{2}\right)\frac{t}{\lambda_0 \sin\theta}-\ln 2=\ln\sinh\left(\frac{t}{2\lambda_0 \sin\theta}\right) \tag{5.3}$$

The peak kinetic energies (E_0 and E_S) are easily available from the XPS spectra, so that it is more convenient to use the ratio of these energies rather than the ratio of the attenuation lengths of the substrate and the overlayer electrons in the overlayer. A good approximation is

$$\frac{\lambda_0}{\lambda_S}=\left(\frac{E_0}{E_S}\right)^{0.75} \tag{5.4}$$

which is good for $E \geq 100$ eV for low atomic number overlayers, and good above ~500 eV for overlayers of all atomic numbers [5.14]. Thus, (5.3) becomes

$$\ln\left(\frac{C_0 / S_0}{C_S / S_S}\right) - \left[\left(\frac{E_0}{E_S}\right)^{0.75} - \frac{1}{2}\right]\frac{t}{\lambda_0 \sin\theta} - \ln 2 = \ln\sinh\left(\frac{t}{2\lambda_0 \sin\theta}\right) \qquad (5.5)$$

In Equation (5.5), I_0, I_S, E_0, E_S can be measured directly from the XPS spectra of Si 2p and Ge 2p3 or Ge 3d. The take-off angle is kept constant in the measurement. It should be noticed that, since the XPS analysis is an *ex-situ* measurement, and the top overlayer of interest in the monitor sample is actually a "double-layer" which consists of silicon oxide and pure silicon (the twin-peak Si 2p spectrum in Figure 4.4). So Equation (5.5) may not apply to the sample exactly. However, it is also noticed that the electron attenuation lengths of silicon and silicon oxide are very similar [5.15], and the average E_0 (Si 2p) is much larger than the difference in the Si 2p kinetic energy between silicon oxide and pure silicon ($E_{0,\,avg} >> |E_{0,SiO2}-E_{0,Si}|$). Therefore, it is a good approximation to consider the top "double-layer" a homogeneous single film, by averaging the attenuation lengths and the kinetic energies, and adding up the two peak intensities (Si 2p). It should also be noticed that the attenuation lengths of photoelectrons in bulk silicon was used (λ_0, λ_S). This requires an additional assumption that they are the same as that in ultra-thin strained silicon (the Si-passivation layer) grown on germanium. Consequently, Equation (5.5) can be solved numerically to measure the top silicon layer thickness (t).

5.3.2 Results and discussion

Figure 5.3 shows the XPS spectra that were collected from the monitor wafers with a 45º take-off angle. The x-axis is the kinetic energy of photo-electrons excited by the Al x-ray photons. The corresponding thickness of the silicon layer was calculated by Equation (5.5) and shown in Table 5.2 (a). It suggests that the silicon layer only consists of several monolayers even with the longest treatment in this experiment. Such a thin layer can be consumed after the subsequent deposition of

HfO_2 to form the dielectric interfacial layer (IL). The table also presents the HfO_2 thicknesses (b) which were measured by ellipsometry.

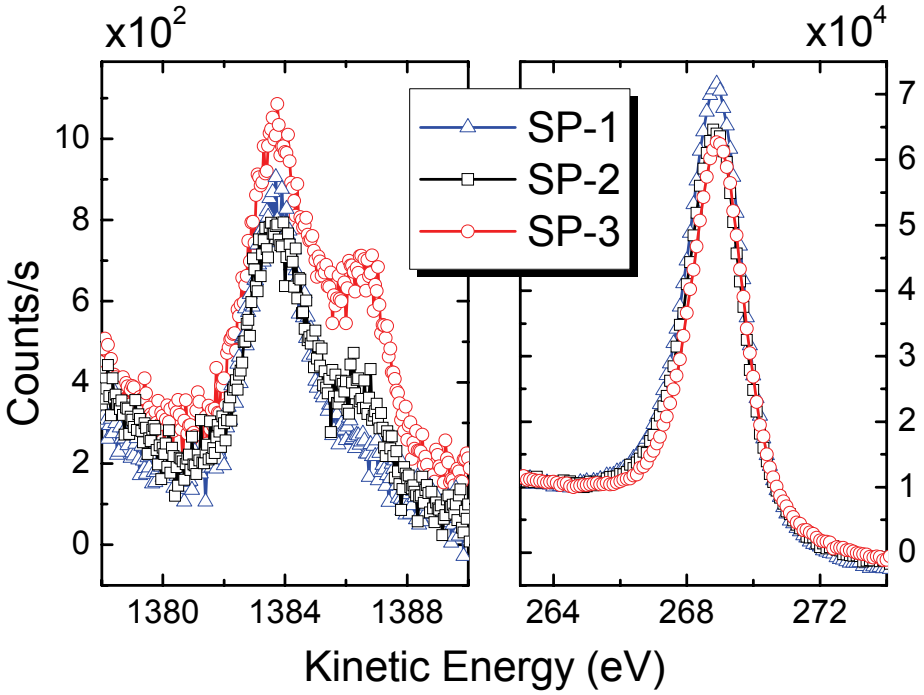


Figure 5.3 XPS spectra of germanium surface passivated by different silicon thicknesses. The intensity and the kinetic energy of photo-electrons were then used to calculate the silicon thickness.

Table 5.2 The thicknesses of the silicon passivation layers (a) and the HfO_2 dielectrics (b) in this experiment. The silicon thicknesses were calculated from the XPS spectra in Figure 5.3. The HfO_2 thicknesses were measured by ellipsometry.

(a)

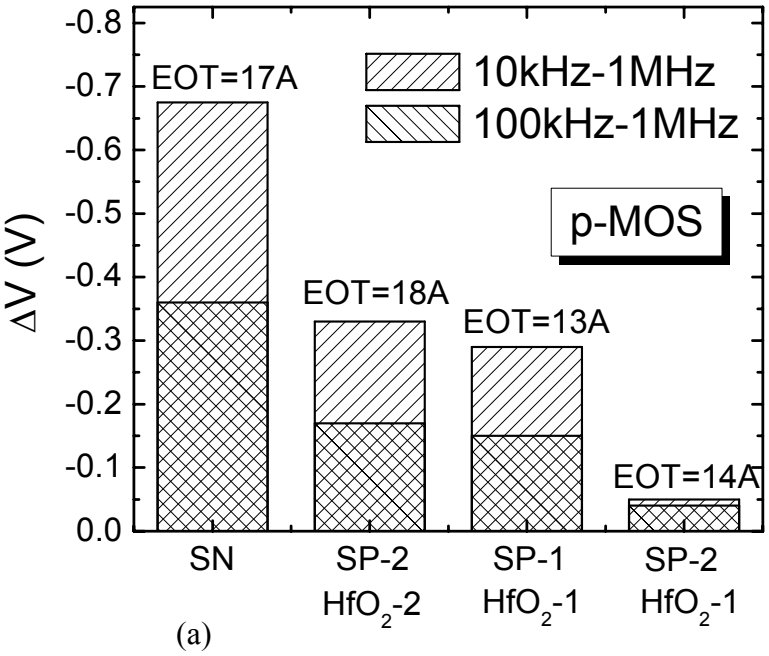
Passivation condition	SP-1	SP-2	SP-3
Si layer thickness (nm)	0.32	0.38	0.48

(b)

HfO_2 deposition condition	HfO_2-1	HfO_2-2
HfO_2 thickness (nm)	~5.2	~7.4

C-V measurements show that the amount of Si on germanium substrate after SiH_4 surface treatment affects device performance. Figure 5.4(a) summarizes the frequency dispersion of p-MOS capacitors by SiH_4 surface passivation with different Si amounts. The SN devices are also included for comparison. The Y-axis is the voltage difference (ΔV) at the ideal flat-band capacitance (i.e. no interface trap

capacitance) under 10 kHz and 100 kHz with respect to those under 1 MHz. For SN capacitors, this ΔV between 10 kHz and 1 MHz can be as high as -0.67V. Using SiH_4



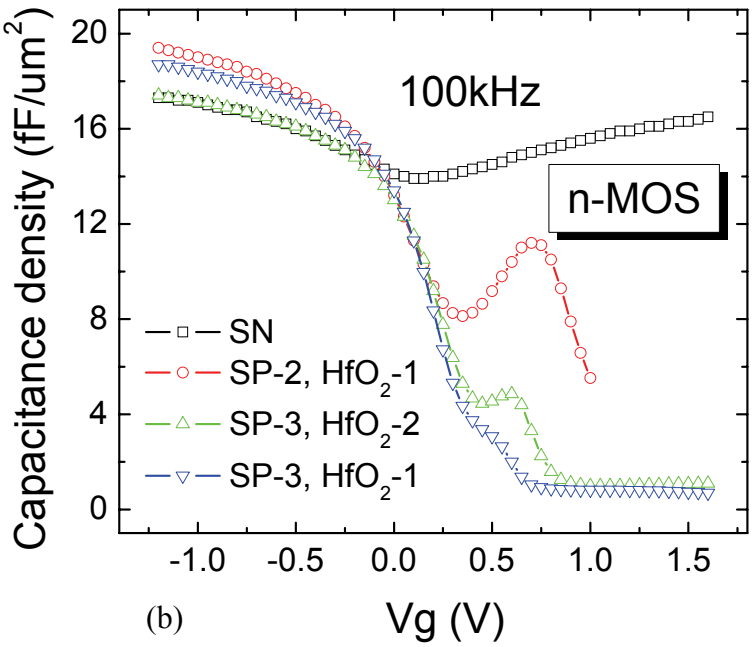


Figure 5.4 Effect of the silicon and the HfO_2 thicknesses on the C-V characteristics of Ge MOS capacitors. (a) Frequency dispersion was characterized by the difference in the voltage at flat-band capacitance of the Ge p-MOS capacitors; (b) C-V curves of the Ge n-MOS capacitors measured at 100 kHz.

surface passivation instead of surface nitridation can reduce this dispersion. When increasing the amount of silicon from SP-1 to SP-2 while retaining the same amount of CVD oxide (HfO_2-1), ΔV between 10 kHz and 1 MHz was reduced to ~0.05 V. At the same time, the EOT increased by 1Å, implying there is a slightly thicker IL. This ΔV also depends on the high-k thickness. Increasing the high-k thickness from HfO_2-1 (EOT=13Å) to HfO_2-2 (EOT=18Å), while remaining the same amount of silicon (SP-2), will increase ΔV increases again. This might be attributed to the additional oxidation of germanium at the IL/semiconductor interface. Figure 5.4(b) shows the C-V characteristics of n-MOS capacitors processed by SiH_4 surface passivation with different Si amounts and the C-V curve of a SN device. The SN device exhibits a large capacitance value at positive gate bias (an MIM-like C-V curve), while the SP device with a thinner silicon passivation layer (SP-2, HfO_2-1) shows a large kink in the inversion region. By increasing the amount of silicon (SP-3, HfO_2-1), this kink can be greatly reduced by sacrificing 0.7 fF/um^2 of capacitance. Meanwhile, the kink increases again with a larger amount of high-k material (SP-3, HfO_2-2). These suggest that the introduction of silicon by the SiH_4 surface passivation helps to reduce the oxide/semiconductor interface traps by reducing the amount of germanium oxide underneath. Increasing the amount of silicon would reduce the amount of germanium oxide at the interface, and hence, lead to fewer interface traps. At the same time, increasing HfO_2 thickness tends to consume more silicon, and more germanium oxide might form, resulting in worse interface quality. Therefore, the optimum amount of silicon also depends on the actual deposition of the subsequent high-k material.

The monitor wafer with SP-3 and HfO_2-1 was also analyzed by XPS with Ge 2p3 and Si 2p core level spectra Figure 5.5. The observation of elemental chemical state of germanium indicates the analysis includes the oxide/semiconductor interface. Silicon

is fully consumed as only the Si-O peak is observed, which also leads to additional oxidation of germanium (Ge-O peak). Hence, it can be confirmed that the channel is kept in germanium for the gain of electron mobility.

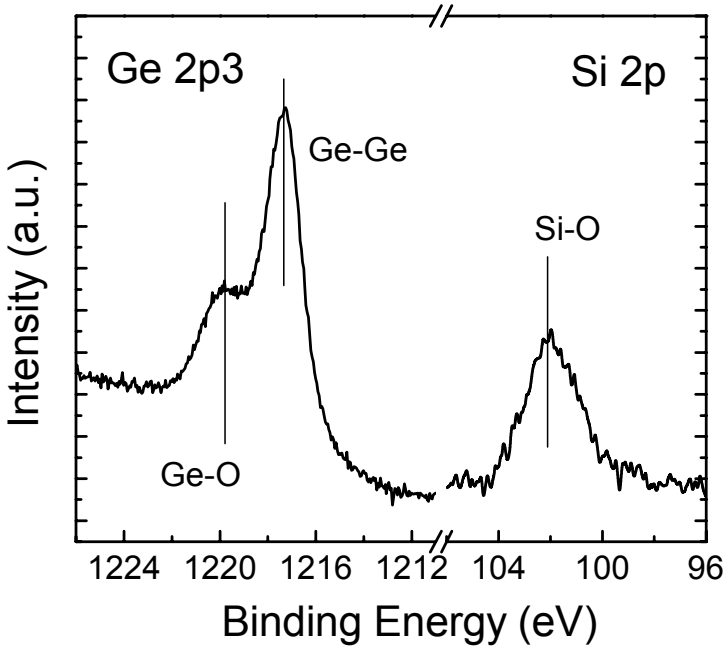


Figure 5.5 Ge 2p3 and Si 2p XPS spectra of the monitor sample that was done with thick silicon passivation and HfO_2 deposition. Silicon is completely consumed after HfO_2 deposition.

5.4 Fabrication of Ge n-MOSFET

In the conventional gate-first self-aligned MOSFET fabrication, source/drain activation anneal is usually the highest thermal process after the gate stack formation. For germanium, an annealing temperature 450 - 700 ºC is needed for n-type dopant activation and reparation of implant damage in the source/drain area [5.5][5.8][5.9], which is equal or higher than the gate stack formation temperature. Therefore, the fabrication of Ge n-MOSFET shall start with a study of the thermal stability of the gate stack.

5.4.1 Gate stack integrity upon annealing

The thermal stability of the gate stack in terms of leakage current and EOT is analyzed with SP processed n-MOS capacitors (Figure 5.6). The leakage current is taken at -1V of gate bias. From the device without annealing (RTA) to the device processed with the highest thermal budget (600 ºC, 30s), the leakage current increases by around one order of magnitude, and EOT increases by 2.8Å. Thus, a higher temperature annealing on the gate stack generally degrades the I_g-EOT characteristic. The increase in EOT might be due to an additional growth of the interfacial layer. At the same time, the increase in leakage current could also be related to the additional

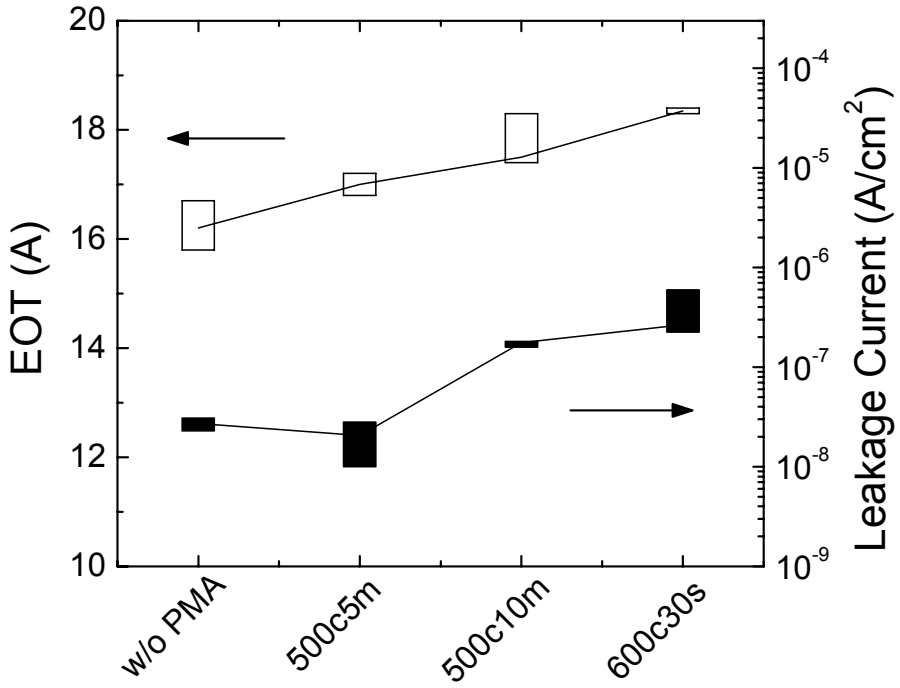


Figure 5.6 Thermal stability of Ge MOS capacitor in terms of EOT and gate leakage. Both EOT and the gate leakage increases with increasing the annealing temperature and/or time.

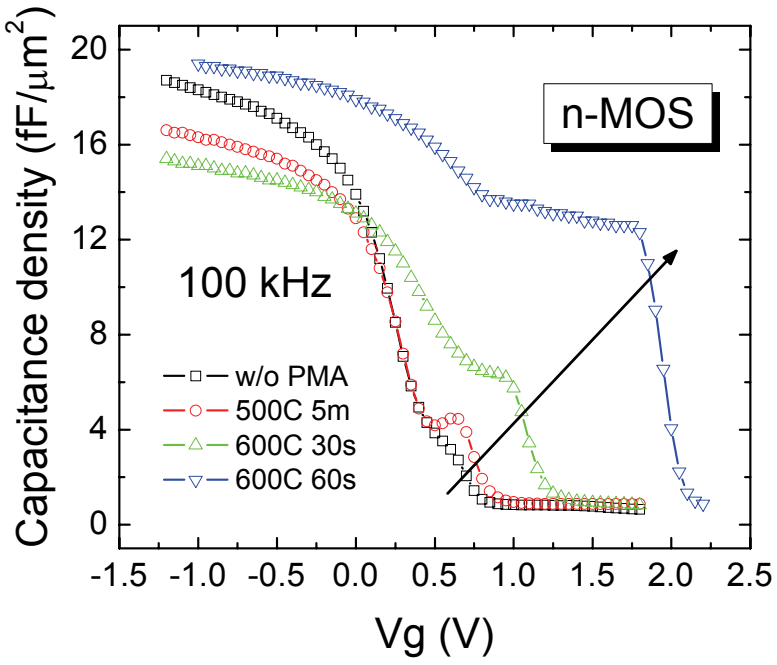


Figure 5.7 Thermal stability of the Ge MOS capacitors in terms of C-V characteristics. The kink increases with increasing annealing temperature and/or time, indicating that the interface trap density increases.

germanium oxide formation which has led to the high leakage of direct HfO_2 deposition, and/or the Ge out-diffusion from the substrate into the oxide [5.16][5.17]. This limitation should be considered in selecting the right process condition for source/drain (S/D) formation.

The thermal stability of the SP n-MOS capacitors in terms of C-V characteristics was also analyzed by subjecting the devices to different annealing conditions in RTP, and the results are shown in Figure 5.7. Similar temperatures and durations were chosen with the source/drain junction anneal. As can be seen, the kink of the C-V curves increases when the thermal budget increases from 500 ºC at 5 min to 600 ºC at 1 min, suggesting the interface quality degrades when the device is subjected to a high thermal budget annealing. As a result, these interface states may degrade the electron mobility severely through Coulomb scattering. This limitation might be associated with the additional formation of germanium oxide at the interface during annealing.

Hence, extra caution should also be taken with the S/D annealing in the integration of the transistor fabrication process to prevent interface states (D_{it}) from increasing.

5.4.2 Transistor characteristics

The transistors fabrication flow was described exactly in Chapter 2. In order to evaluate the effect of silicon passivation on transistor performance, two treatment conditions were employed (SP-2 and SP-3). The gate oxide deposition is with the HfO_2-1 condition. Following the gate patterning (after the photo-resist was removed), 100 Å SiO_2 was deposited by electron beam (e-beam) evaporation. The samples were implanted with phosphorus in the source/drain area with a dose of $1x10^{15}$ cm^{-2} (50keV). The activation of dopants was performed at 450ºC using rapid thermal annealing (RTA). The front side SiO_2 was then removed by diluted-HF and Aluminum was deposited by e-beam evaporation on the backside. After forming gas annealing at 350ºC, contact metal (Al-Si) was deposited and patterned.

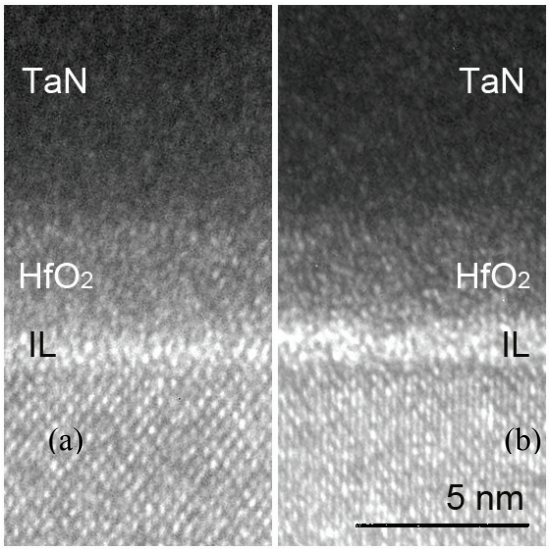


Figure 5.8 TEM images of the gate stack cross-section with the silicon passivation of SP-2 (a) or SP3 (b). A thicker silicon interlayer of SP-3 results in a thicker interfacial layer (IL).

The final gate stacks with the two different silicon passivation layers (SP-2, and SP-3) were examined with TEM and Figure 5.8 shows the cross-sections of the gate stacks. There is no observable hetero-structure in the channel region under the amorphous interfacial layer, suggesting that the channel is germanium and the silicon is fully consumed. A thicker silicon interlayer results in a thicker interfacial layer. At the same time, the HfO_2 bulk thickness is smaller with the thicker interfacial layer, which suggests that the interfacial layer formation is probably an intermixing of the silicon passivation layer and the HfO_2.

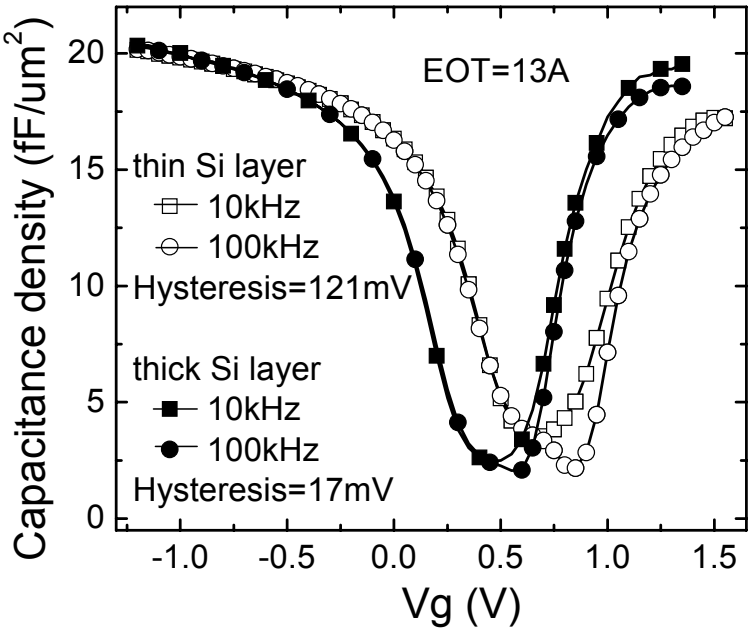


Figure 5.9 C-V comparison of Ge n-MOSFETs with thin or thick silicon layer. The thick silicon layer results in less fixed charge, less frequency dispersion, less hysteresis in the device than the thin silicon layer.

Figure 5.9 shows the capacitance–voltage (*C-V*) characteristics of Ge n-channel MOSFETs fabricated with the two different silicon passivation conditions. The EOTs of the devices were observed to be 13 Å after taking into account of quantum-mechanic correction. From Figure 5.9, no "kink" in the accumulation region for all the curves can be observed, which also implies that the silicon layer is oxidized and

contributed to the interfacial layer, and the MOSFETs are surface channel devices. Besides, it was also observed that there is a positive shift of the curves with thin silicon passivation, suggesting there is significant negative fixed charge (~$3.82\text{x}10^{12}$ cm^{-2}) in the gate dielectric. Such V_{fb} shift is possibly due to the Ge out-diffusion from substrate into the gate dielectric during thermal process (deposition, PDA, S/D anneal) [5.17][5.18][5.19]. This Ge out-diffusion is dependent on the amount of germanium oxide in contact with HfO_2 at the interface [5.17]. Therefore, a thick silicon layer could reduce the Ge out-diffusion [5.18] significantly in two ways: (1) by reducing the amount of germanium oxide; (2) or by separating HfO_2 from germanium oxide by a silicate-like IL. Consequently, less positive V_{fb} shift can be observed in Figure 5.9. Moreover, it was found that the large hysteresis (121 mV) of the device with thin silicon passivation can be effectively reduced to 17 mV for the device with thick silicon passivation, again probably attributed to less Ge concentration in the high-k bulk. At the same time, the thick silicon passivation also effectively reduces the interface trap density as evidenced by reduced frequency dispersion between 10 kHz and 100 kHz, which could be attributed to less formation of germanium oxide at the interface. This result is consistent with Figure 5.4(b). The interface trap density (SP-3) is measured to be $3.2\text{x}10^{11}$ $cm^{-1}eV^{-1}$ using the charge pumping technique, which would be shown in the next chapter.

The output characteristics of the n- MOSFETs (L_g=20 μm) are shown in Figure 5.10 plotted at the same V_G-V_{th}. The transistor with the thick silicon layer has a significantly higher I_d than that with the thin silicon layer. Figure 5.11 shows the I_d-V_g characteristics of the transistors. Due to the reduction of negative charge that is observed in the *C-V* curve, the transistor with the thick silicon layer has a smaller V_{th} (0.6 V) than its counter-part (0.9 V). In addition, it also exhibits a smaller sub-

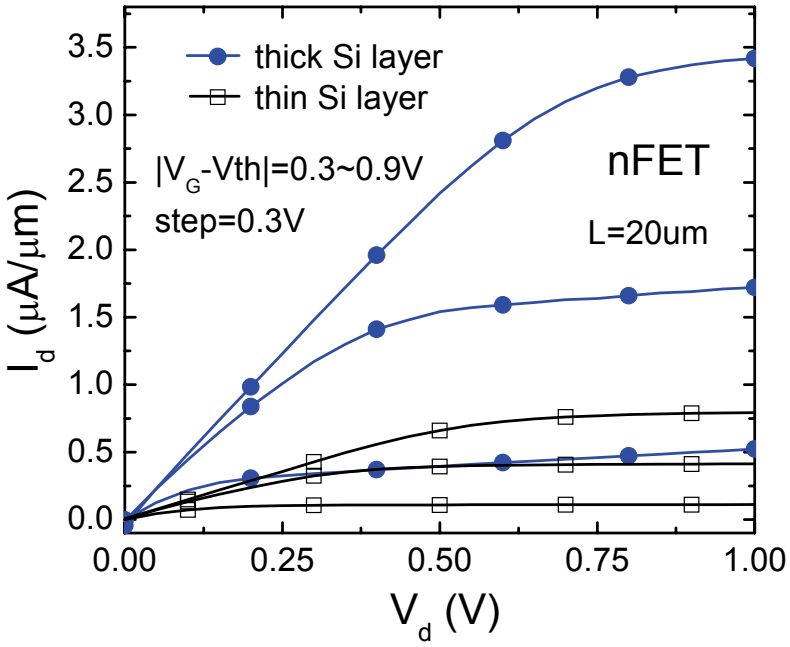


Figure 5.10 I_D-V_D characteristics of Ge n-MOSFETs with thin or thick silicon layer. The thick silicon layer results in higher drive current in the device than the thin silicon layer.

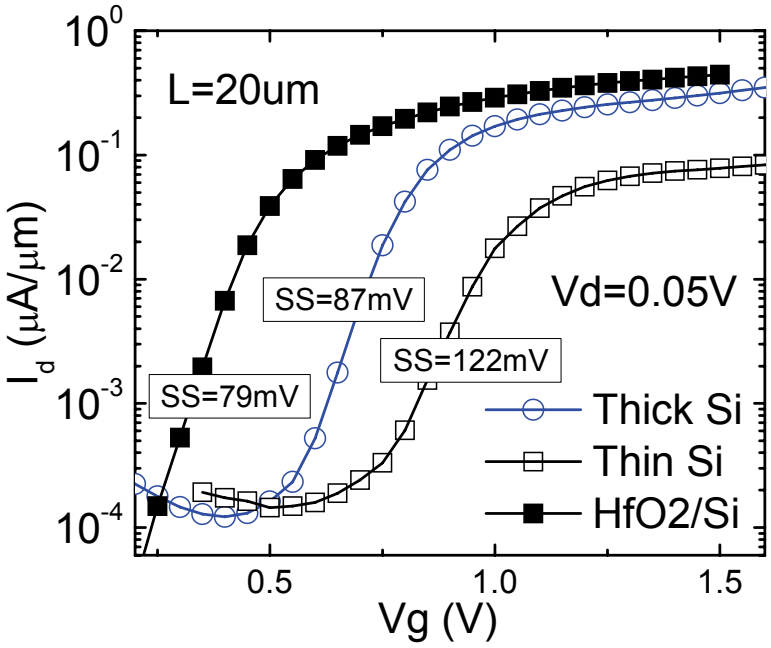


Figure 5.11 I_D-V_G characteristics of Ge n-MOSFETs with thin or thick silicon layer. The thick silicon layer results in higher output current in linear region, smaller sub-threshold swing in the device than the thin silicon layer.

threshold swing than that with the thin silicon passivation layer. This agrees well with the discussion that the interface trap density reduces when there is more silicon on the germanium surface prior to HfO_2 deposition. At the same time, the sub-threshold swing is still larger than the silicon control (solid-square line) which has the same HfO_2 deposition process and EOT. This also agrees well with the observation of small CV kinks of the optimized SP devices in Figure 5.4 and Figure 5.7.

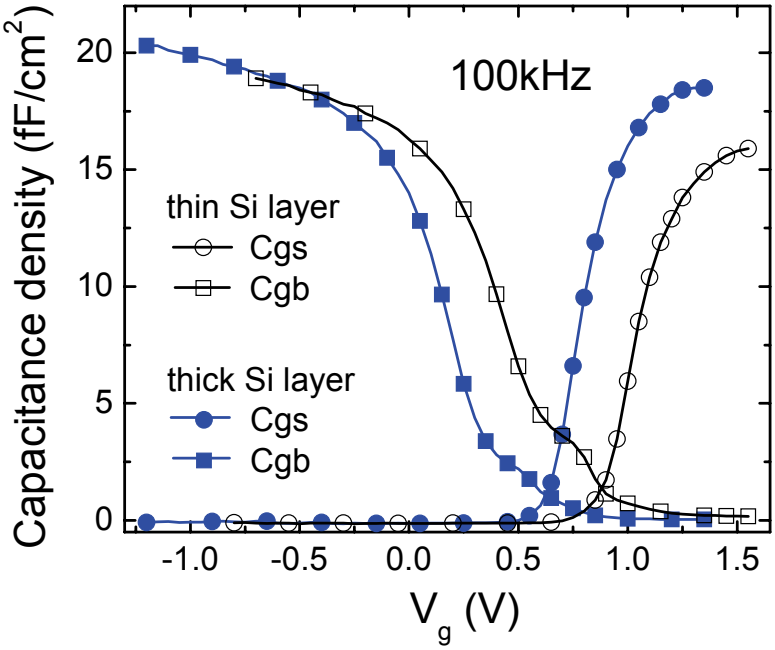


Figure 5.12 Split C-V was measured for mobility extraction. The results match with C-V curves in Figure 5.8, which enables the accurate extraction of inversion charge and depletion charge, respectively.

Figure 5.12 shows the split C-V measurement results for the two transistors. They match well the full C-V results in Figure 5.9 and enable the accurate extraction of depletion charge Q_B and inversion charge Q_{inv} respectively. Subsequently, the mobility was extracted using split C-V method and shown in Figure 5.13. The channel vertical electric field was estimated by $E_{eff} = \frac{Q_B + 0.5 \bullet Q_{inv}}{\kappa_{Ge}\varepsilon_0}$, where κ_{Ge} is the Ge dielectric constant, and ε_0 is the permittivity of vacuum. A silicon n-channel MOSFET

with the same MOCVD HfO_2 is also characterized for comparison. For the thin silicon passivation, the Ge transistor exhibits lower electron mobility than the silicon device. This is probably due to the significant negative fixed charge in the dielectric and the high interface trap density at the oxide/semiconductor interface, both leading to serious Coulomb scattering of the channel carriers. Increasing the silicon amount helps to improve the mobility significantly. The peak mobility is improved by ~55%. As a result, the Ge transistor shows ~61% higher peak electron mobility than that of the silicon control.

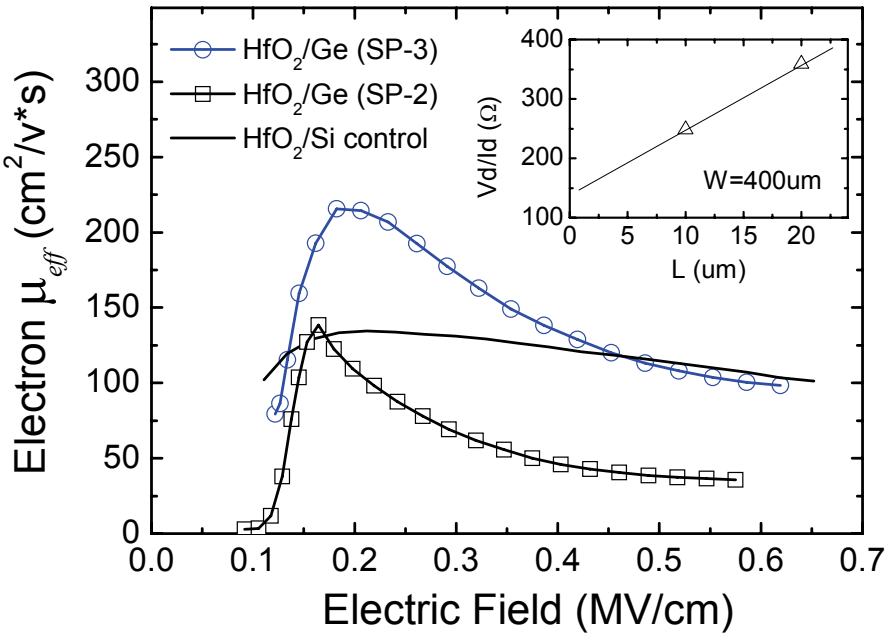


Figure 5.13 Effective electron mobility of Ge n-MOSFETs with thin or thick silicon layer. The thick silicon layer improves the electron mobility in the device significantly over the thin silicon layer.

Furthermore, it should be mentioned that SP-3 in this experiment may not be the most optimized passivation condition as germanium oxide was still observed in that sample (Figure 5.5). Since the charge centroid of channel carriers are ~10Å or even farther away from the interface, which is thicker than the ultra-thin silicon passivation layer, there must be an optimum amount of silicon in which the silicon is not fully

consumed and the majority of electrons are kept in germanium for further drive current enhancement.

It was also noticed that, in the high electric field regime, the Ge transistor shows a comparable electron mobility to that of the Si control. At the same time, it was found that the drive current (I_d) does not increase in proportion to $\frac{1}{L}$ for both samples. For instance, the drive current is 0.347 μA/um for a thick SP transistor of 20 μm channel length @ V_D=0.05V and V_G-V_{th}=1.0V (linear region), while the drive current for a 10 um transistor is 0.502 μA/um. This may suggest that there is a considerable series resistance in the source/drain region, which limits the drive current significantly. This can be seen by the relationship $\frac{V}{I_D} = \frac{L}{\mu_{eff} C_{OX} W (V_G - V_{th})} + R_{SD}$ (Figure 5.13 inset), where V is the applied voltage to the drain area, I_D is the measured current, R_{SD} is the source/drain resistance, and μ_{eff}, C_{ox}, V_g, V_{th} are all independent of the measurement condition. This high source/drain series resistance is likely due to the relatively low temperature of activation annealing (450ºC), and it consequently leads to underestimation of electron mobility. Therefore, the measured electron mobility at high electric field can be further improved if the source/drain series resistance can be reduced.

5.4.3 Summary

Self-aligned Ge n-MOSFETs with CVD high-k gate dielectric (HfO_2) were demonstrated with conventional gate-first process sequence. The silicon passivation by SiH_4 annealing prior to the gate dielectric deposition plays a critical role in the device performance. The process was first engineered with different silicon thicknesses as

well as different HfO_2 thicknesses, and this was followed by the thermal stability study of the gate stack. Provided that the silicon passivation layer thickness is small enough to be oxidized during the thermal process of gate stack formation, it was found that increasing the silicon thickness helps to reduce hysteresis, fixed charge in the gate dielectric, and interface trap density at the oxide/semiconductor interface. As a result, n-channel Ge MOSFET with CVD HfO_2 is demonstrated with a peak mobility that is ~61% higher, and with a high field mobility that is comparable to that of the silicon counterpart with the same deposition of HfO_2.

5.5 Overall comparison of p- and n-MOSFETs

In CMOS applications, both p- and n-type MOSFETs should be fabricated on the same substrate simultaneously. However, Ge p- and n-MOSFETs have been developed separately until now, and the silicon passivation condition for Ge p-MOSFET in Chapter 4 is not as optimal as what was achieved in this chapter. At the same time, there was no aluminum source/drain contact in the last chapter, which had possibly led to reduction of output current in the Ge p-MOSFET due to source/drain contact resistance. Therefore, it is necessary to fabricate Ge p-MOSFET again with the improved silicon passivation and aluminum source/drain contact, and compare it with the Ge n-MOSFET. The only different process is the source/drain for which boron was implanted (1×10^{15} cm^{-2}, 35 keV). Again, Ge p-MOSFET with surface nitridation was also fabricated as the control device.

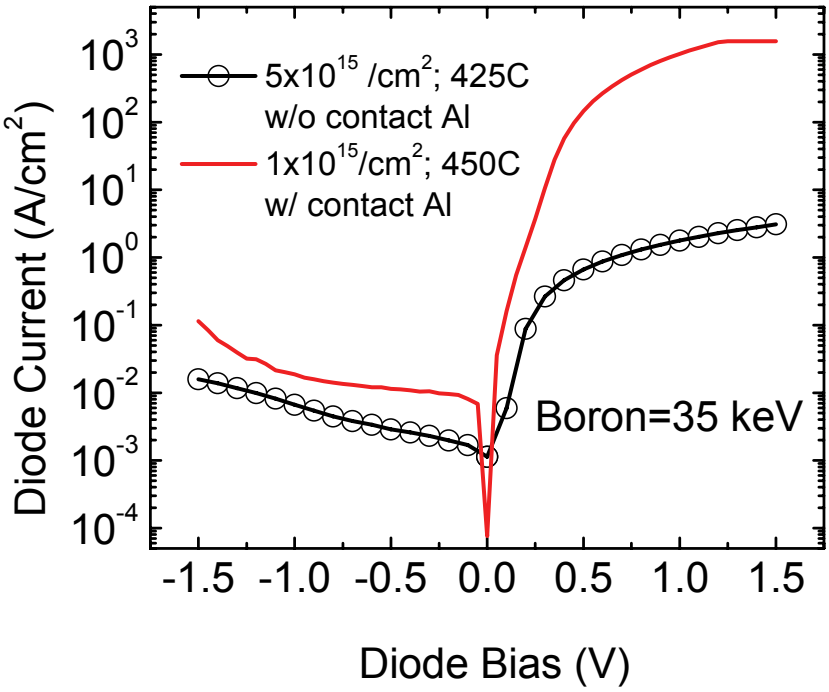


Figure 5.14 Ge p+/n diode with and without aluminum contact. The aluminum source/drain contact reduces the contact resistance and improve the on current. The increased off current is probably due to the reduction of implantation dose.

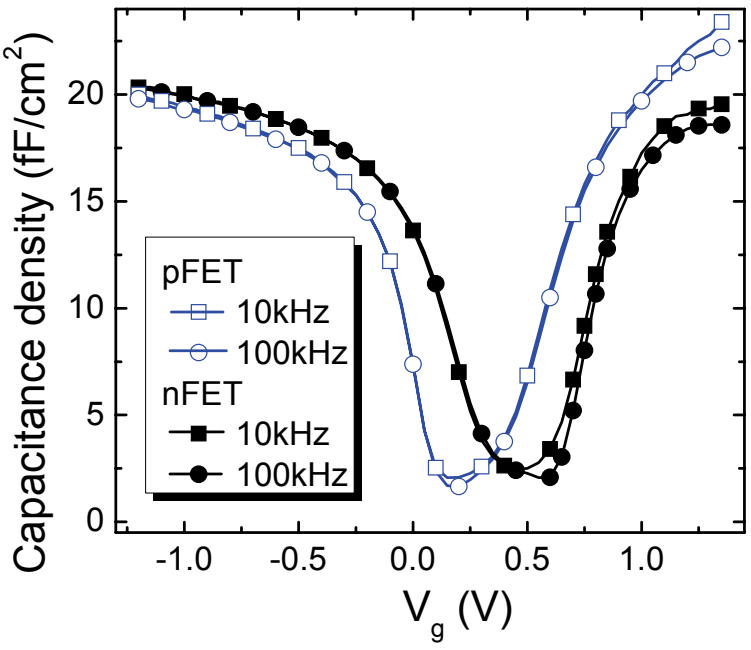


Figure 5.15 C-V characteristics of Ge p- and n-MOSFETs with the thick silicon layer (SP-3). Frequency dispersion is small for both devices.

The p+/n diode performance is first compared to that in Chapter 2 (Figure 5.14). It clearly shows that the contact resistance is significantly reduced by the aluminum contact. As a result, the on-current (positive bias) is significantly increased. But the off-current increases at the same time, probably because of the reduced implantation dose.

Figure 5.15 shows the C-V curves of both p- and n-channel transistors with optimized silicon passivation and CVD HfO_2. The EOTs are both ~13Å. Negligible frequency dispersion is observed for both devices, which suggests the interface trap density is low. Figure 5.16 shows the MOSFETs' output characteristics. The SP p-FET shows a ~1.76x drain current compared to the SN p-FET under the same overdrive of gate bias in saturation region. The n-FET's output drive current is ~57% of the SP p-FET, suggesting the electron mobility is still limited. Figure 5.17 shows the I_d-V_g characteristics of the transistors. The SN p-FET exhibits a sub-threshold

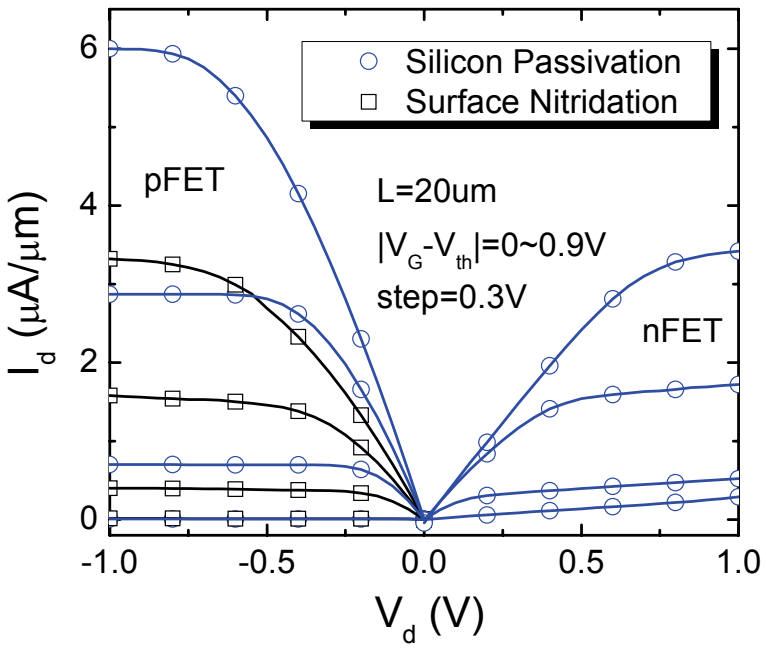


Figure 5.16 I_D-V_G characteristics of Ge p- and n-MOSFETs with thick silicon layer or nitridation The silicon passivation results in higher output current in the devices than the surface nitridation.

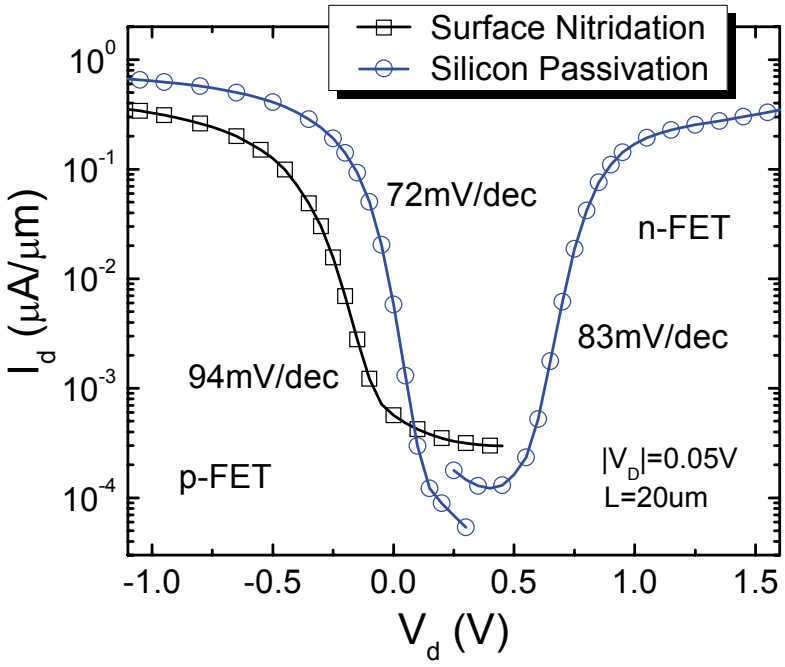


Figure 5.17 I_D-V_G characteristics of Ge p- and n-MOSFETs with thick silicon layer or nitridation. The silicon passivation results in better sub-threshold swing in the devices than the surface nitridation.

swing of 94 mV/dec. Both SP p- and n-FETs show lower sub-threshold swings (72 mV/dec and 83 mV/dec), which is mainly attributed to the reduced interface trap density.

Hole mobility was also extracted by split-CV method. Similarly, the effective channel electric fields were estimated by

$$E_{eff} = \frac{Q_B + nQ_{inv}}{\kappa_{Ge}\varepsilon_0}$$

where κ_{Ge} is the Ge dielectric constant, ε_0 is the permittivity of vacuum, but n=1/3 for holes. Figure 5.18 shows all the carrier mobilities. It can be noticed that the hole mobility is improved significantly as compared to Figure 4.15 in Chapter 4, which should be due to the reduced contact resistance by the additional Al contact. Data from literature where the gate dielectric is GeON is also included for comparison. Comparable hole mobility is observed probably due to the same GeON/Ge interface.

The SN technique results in a peak mobility of 165 $cm^2/V•s$ and 13.4% improved mobility at E_{eff} of 0.6 MV/cm over the Si universal curve of holes. In comparison, the SP technique is superior to the other techniques where nitrogen is introduced at the oxide/semiconductor interface. The peak hole mobility is 240 $cm^2/V•s$ at the effective vertical field of 0.18 MV/cm. In the high vertical field region (0.6 MV/cm), the Ge device with SP treatment shows a mobility which is 82% higher than the universal Si/SiO_2 hole mobility.

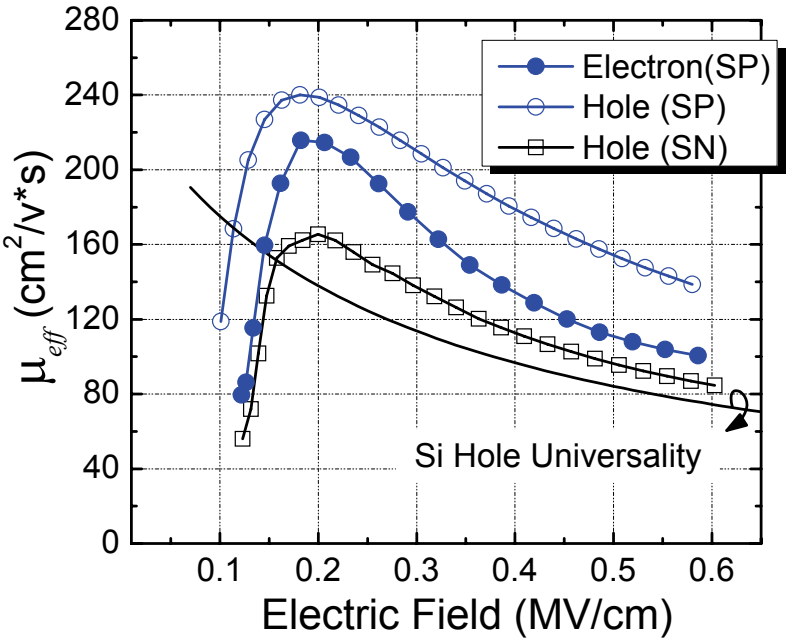


Figure 5.18 Effective carrier mobilities of Ge p-MOSFETs (hole) and n-MOSFET (electron) with thick silicon layer or surface nitridation.

In contrast, the effective electron mobility is much lower than the Si electron universal curve, but also lower than the hole mobility (SP). The possible reasons have been discussed in **Section 5.4.2**. The first cause is the insufficient dopant activation of the n+/p sourc/drain diode, which leads to high series resistance and underestimation of the mobility. However, the other more possible reason is that the electrons may be experiencing more severe scattering than holes, as the reduction of electron mobility is

larger than hole mobility. According to the discussion in **Section 5.2**, the interface trap density in the upper half bandgap is higher than that in the lower half bandgap. Consequently, the electron mobility is reduced more than the hole mobility because there is more Coulomb scattering by the charge at the interface. Furthermore, it should be noticed that this model may not account for all the electron mobility degradation based on the recent study on high-k/Si systems. Several research groups have shown similar results that electron mobility suffers from additional remote phonon scattering due to the ionic nature of high-k dielectrics [5.21]-[5.24], while hole mobility only suffers from Coulomb scattering and surface roughness scattering [5.21][5.23]. This may be valid in the MOCVD HfO_2 in this study, which is evidenced by the very low electron mobility of the HfO_2/Si control device. Nevertheless, this issue has never been studied experimentally for germanium. Therefore, electron mobility should receive more attention in future study.

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Chapter 6

Threshold Voltage Instability in Germanium p- and n- MOSFETs

Germanium p- and n- MOSFETs have been developed successfully with CVD HfO_2 as the gate dielectric and TaN as the metal gate electrode. Gate oxide reliability is an important topic for further study. Hysteresis, threshold voltage (V_{th}) instability and dielectric breakdown are the three important reliability issues of high-k gate dielectrics on silicon substrate [6.1]. Therefore, it is also necessary to evaluate these high-k reliability issues on germanium substrate. In this chapter, V_{th} instability of HfO_2/Ge p- and n- MOSFETs will be studied qualitatively in order to clarify Ge's effect on the high-k gate dielectric reliability.

6.1 Threshold voltage instability in high-k Si MOSFETs

Threshold voltage instability is the major phenomenon in bias temperature instability (BTI). Conventionally, it is a degradation phenomenon in MOSFET using SiO_2 as gate dielectric. Under a constant gate voltage bias and elevated temperature, a build-up of charges occurs either at the SiO_2/Si interface or in the oxide layer leading to the reduction of MOSFET performance. It was found that for p-MOSFET, negative BTI (NBTI) under negative gate bias is the main reliability issue other than the positive BTI (PBTI) in n-MOSFETs. In such NBTI case, positive trapped charge (hole trapping) in the oxide and generation of interface states are observed. Further studies also revealed that the nitrogen in the gate oxide induced by nitridation process accelerates BTI degradation [6.2]. Unlike SiO_2, high-k dielectrics such as Hf-based

dielectric exhibit both negative and positive BTI, especially in the case of nMOS PBTI. The trapped charge in the oxide is the main issue, while interface trap generation is relatively trivial due to the scaled power supply voltage. Such BTI issue of high-k dielectrics has to be improved by means of process optimizations, such as engineering of silicon and/or nitrogen [6.3][6.4] in the high-k dielectrics, etc.

6.2 Measurement setup

The Ge MOSFETs in this experiment were the devices fabricated in the last chapter. Silicon p- and n- MOSFETs with MOCVD HfO_2 (but without surface treatment) were also fabricated as the control devices. All the transistors had similar EOTs (~13Å). Table 6.1 summarizes the major process differences in the fabrication flow between the Ge and Si MOSFETs. The annealing temperatures for the Ge devices were significantly lower than the Si devices.

Table 6.1 Temperatures of major thermal processes in the MOSFET fabrication on germanium or on silicon substrates.

	Ge		Si
Surface treatment	SN	SP	
PDA	500ºC		700ºC
S/D Anneal	450ºC		950ºC

As shown in Figure 6.1, a square wave voltage is applied to the transistor's gate electrode (V_{stress}) with grounded source, drain and bulk. During the stress interval, the stress is removed for device characteristic extraction. The Id-Vg curves were measured to extract the threshold voltage and the sub-threshold swing. Charge pumping measurement was performed before and at the end of the entire stress period for comparison. The measurement instruments (Agilent 4155C + 41501B) were controlled by a programmed PC to conduct the measurements automatically for the sake of minimizing the stressing interval so that charge de-trapping in the gate oxide can be

minimized (Appendix). The extraction of V_{th} is based on an integration approach to attenuate experimental measurement error or noise [6.5]. The charge pumping used is the constant-pulse method, in which a voltage wave is applied to the gate electrode with source, drain and bulk grounded. The base level of the wave is then DC swept from negative to positive direction. Charge pumping current (I_{CP}) is measured by the substrate current.

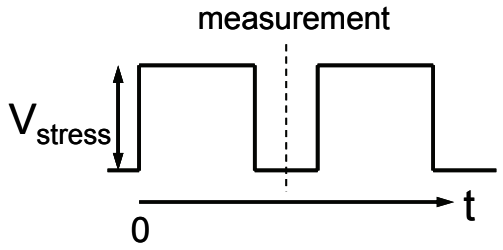


Figure 6.1 Measurement scheme for evaluation of V_{th} instability

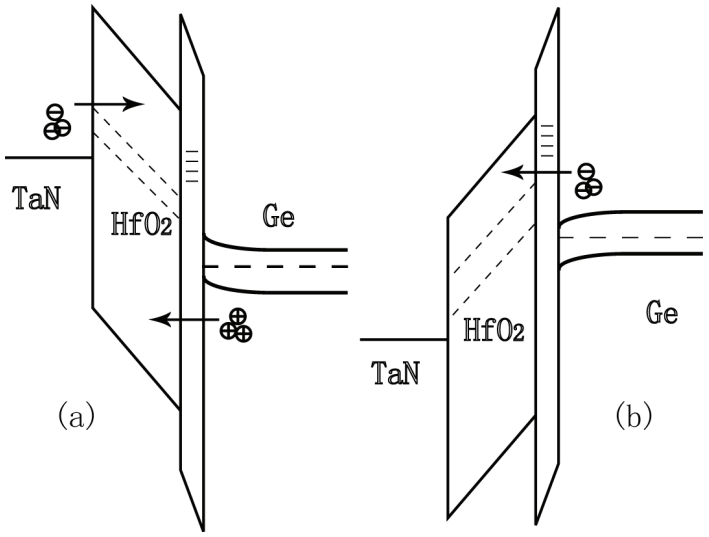


Figure 6.2 Energy band diagram of p- and n- MOSFET under stress. (a) When p-MOSFET is under inversion stress, electrons are injected from the gate electrode, and holes are injected from the substrate; (b) when n-MOSFET is under inversion stress, electrons are injected from the substrate.

Figure 6.2 shows the energy band diagrams (channel region) of Ge MOSFETs under inversion stress. During NBTI stress of p-MOSFETs, electrons are injected from the gate electrode and holes are injected from the substrate, as is shown in Figure 6.2

(a). During PBTI stress of n-MOSFETs, only electrons are injected from the substrate, as is shown in Figure 6.2 (b).

6.3 Results and Discussion

(a) Bias-temperature instability

Figure 6.3 shows the NBTI degradation of V_{th} shift (a) and sub-threshold swing (SS) degradation (b) with stressing for Ge p-MOSFETs as well as the Si control device. It should be noted that the SP Ge p-MOSFETs and the silicon control device were stressed under a higher voltage in order to have the degradation more easily observable. Negative V_{fb} shift was observed on all the p-MOSFETs during stressing. The SN Ge p-MOSFET shows significant V_{th} shift and SS degradation, indicating that the NBTI degradation involves interface trap generation. By employing silicon passivation, Ge p-MOSFET, similar to the silicon control, shows almost no change in SS. This suggests that the immunity to interface trap degradation of the SP Ge p-MOSFETs is comparable to the silicon control. Moreover, the V_{th} shift of the SP Ge p-MOSFET is smaller than that of the silicon control. Based on the band diagram in Figure 6.2 (a), this might be attributed to the larger valence band offset of HfO_2/Ge and hence less hole trapping in the high-k dielectric than the silicon counterparts. Thus, the SP Ge p-MOSFET shows less NBTI degradation than the silicon control.

Figure 6.4 shows the PBTI degradation of V_{th} shift (a) and SS degradation (b) with stressing for SP Ge n-MOSFETs as well as Si n-MOSFETs. The positive shift of V_{th} and the almost constant SS with stressing time suggest that electrons are trapped in the dielectric bulk for both the SP Ge n-MOSFET and the silicon control. However, unlike the Ge p-MOSFET which has a better V_{th} stability than the Si counterpart, the SP Ge n-MOSFET shows a larger V_{th} shift than the silicon control, which suggests a

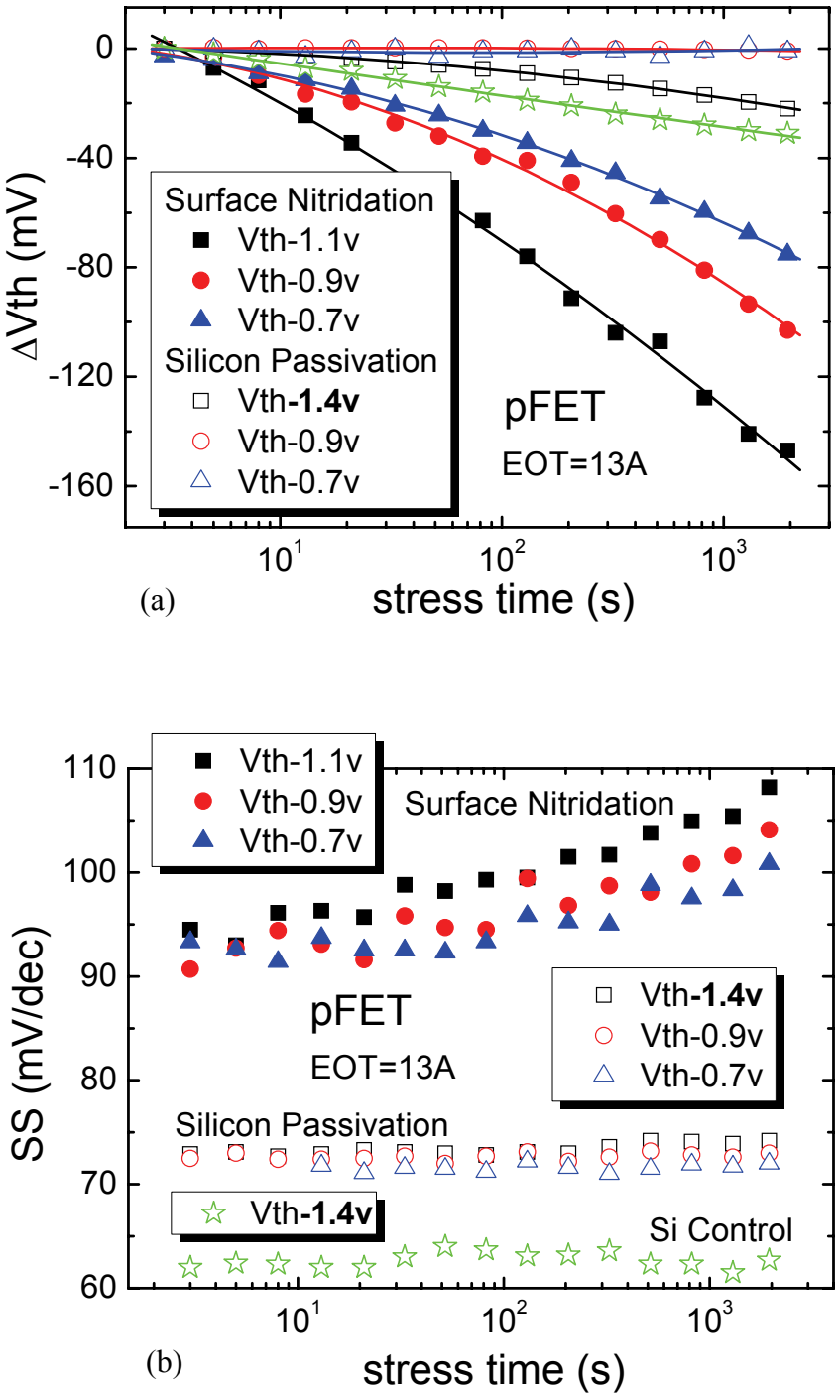


Figure 6.3 Threshold voltage shift (a) and Sub-threshold swing degradation (b) of Ge pMOSFETs under inversion stress. Si pMOSFET with the same EOT is included as the control device. The stress voltage applied to the gate is indicated for each curve.

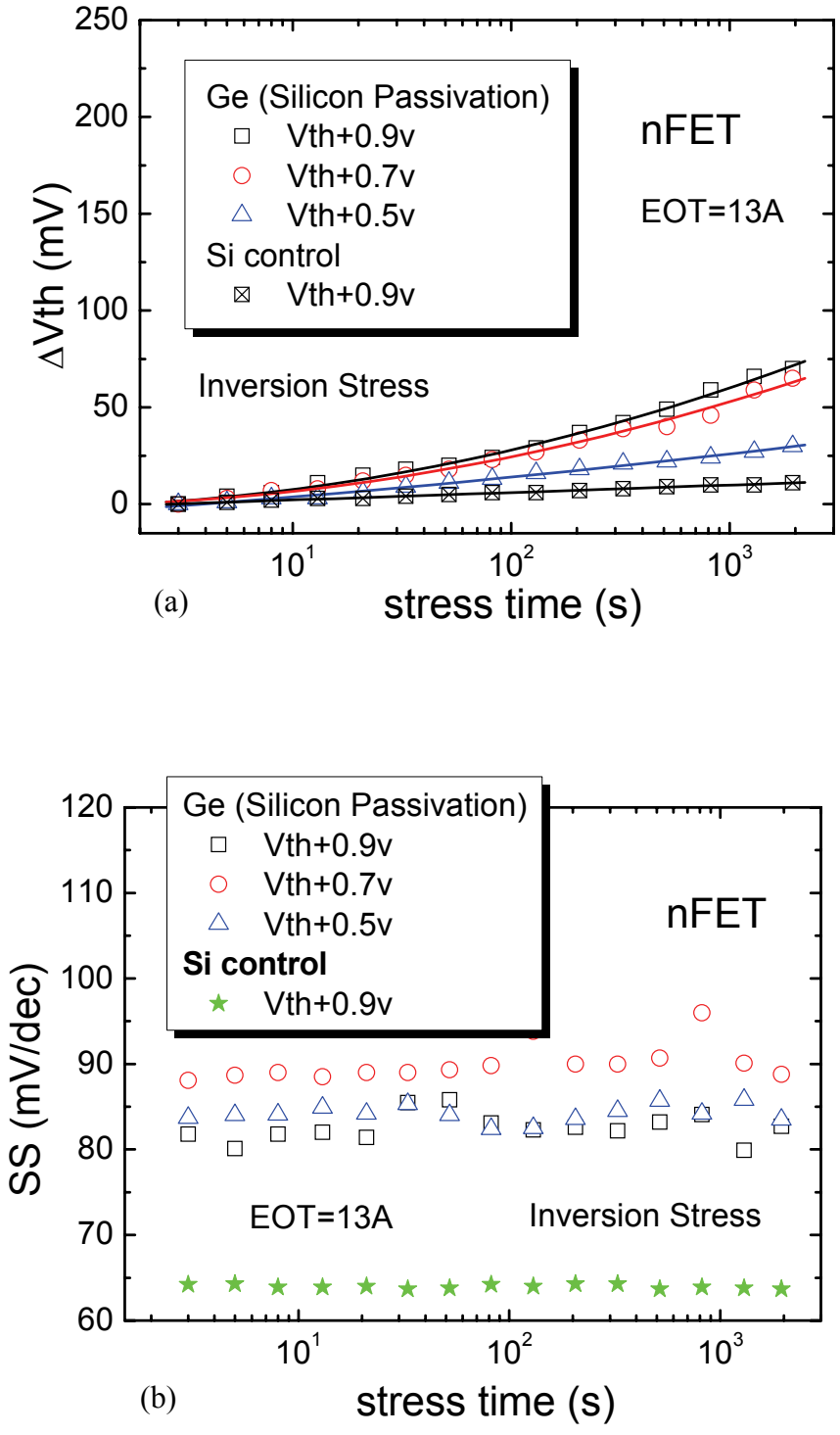
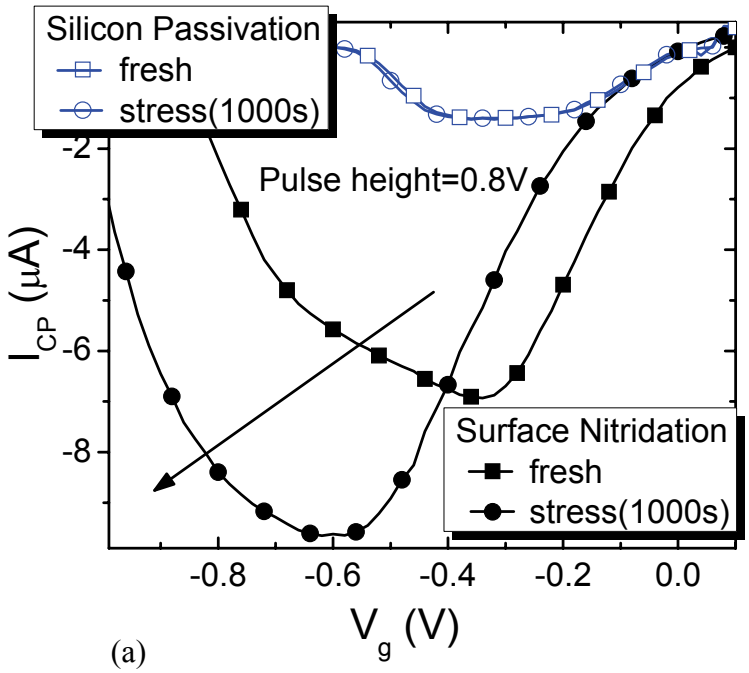


Figure 6.4 Threshold voltage shift (a) and Sub-threshold swing degradation (b) of Ge nMOSFET under inversion stress. Si nMOSFET with the same EOT is used as the control device. The stress voltage applied to the gate is indicated for each curve.

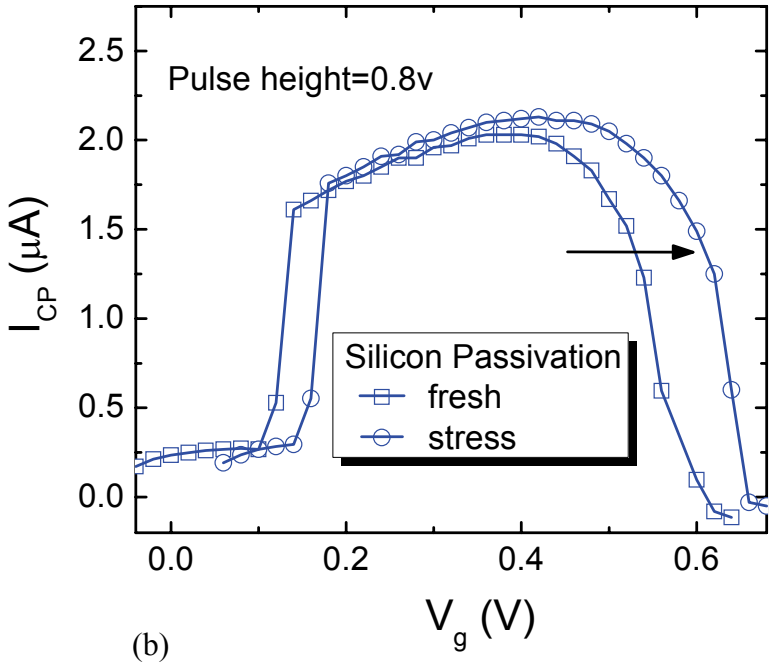
more severe charge trapping in the gate oxide. Since the conduction band offset of the Si device and the Ge device are similar, this phenomenon may be related to the lower processing temperature during the device fabrication (Table 6.1), which results in a larger amount of defects which behave like pre-existing electron traps in the dielectric. Thus, for high-k Ge MOSFETs, PBTI degradation is more significant than NBTI degradation.

Charge pumping measurement was conducted in order to further characterize the V_{th} and SS observation in Figure 6.3 and Figure 6.4. The results are shown in Figure 6.5 for (a) p-MOSFET and (b) n-MOSFET. The interface trap densities observed are $1.6x10^{12}$ $cm^{-2}•eV^{-1}$, $3.2x10^{11}$ $cm^{-2}•eV^{-1}$, and $4.5x10^{11}$ $cm^{-2}•eV^{-1}$ for SN Ge p-MOSFET, SP Ge p-MOSFET, and SP Ge n-MOSFET, respectively. It quantitatively shows that SP can produce much lower interface trap density than SN, which confirms the early discussion in the last chapter on the Ge capacitors in Figure 5.1. After 1000 seconds of stress at V_{th}-1.1V, the increase and the negative shift of the charge pumping current (I_{CP}) for the SN Ge p-MOSFET suggest that its V_{th} instability is attributed both to the increase of interface trap density and to the hole trapping after stressing. This is consistent with the observation in silicon that nitrogen increases NBTI. On the other hand, for both Ge p- and n-MOSFETs made with SP, the I_{CP} remains relatively the same, indicating that there is negligible interface trap generation. The I_{CP} for the SP Ge p-MOSFET after stress remains almost identical for that of the fresh device. This suggests that there is insignificant hole trapping in the SP p-MOSFET. Correspondingly, the positive shift of I_{cp} for the Ge n-MOSFET is attributed to the electron trapping in the high-κ dielectric, which induces the PBTI degradation observed in Figure 6.4.



(a)

p-MOSFETs: D_{it} (SN) = 1.6x10^{12} cm^{-2}•eV^{-1}; Dit (SP) = 3.2x10^{11} cm^{-2}•eV^{-1}.



(b)

n-MOSFET: D_{it} (SN) = 4.5x10^{11} cm^{-2}•eV^{-1}.

Figure 6.5 Charge pumping measurement of Ge p-MOSFET (a) and n-MOSFET (b) before and after inversion stress. Charge trapping is found to be the dominant factor in the reliability of threshold voltage instability.

(b) Charge trapping characteristics

In order to further confirm that BTI in the high-k gate dielectric for the high performance SP Ge transistors is mainly due to charge trapping, we further characterized the charge trapping properties by stress at accumulation with the same scheme as that used in the BTI characterization. In such cases, the majority carriers in the substrate are injected into the gate dielectric. Figure 6.6 shows the V_{th} shift (a) and SS variation (b) stressed at various voltages for all the p-MOSFETs. Electrons were injected from the substrate. Similarly, the SN Ge p-MOSFET shows the highest V_{th} shift and degradation in SS. Negligible degradation in SS is observed for the SP Ge p-MOSFET and the Si control. The larger positive V_{th} shift in SP Ge p-MOSFET than Si control is due to more electron trapping in HfO_2 on Ge substrate. This is consistent with the case of PBTI in n-MOSFETs. Figure 6.7 exhibits the V_{th} shift (a) and SS variation (b) with stressing for both Ge and Si n-MOSFETs. It is noticed that the V_{th} shift in Ge n-MOSFET is less than that in Si control, even though the Ge device was also stressed under higher voltage than the silicon device. Again, there is negligible SS degradation for both devices. These results also indicate positive effective trapped charge occurred in HfO_2 on Ge substrate due to the larger valence band offset (hole barrier) compared to the HfO_2 on Si substrate.

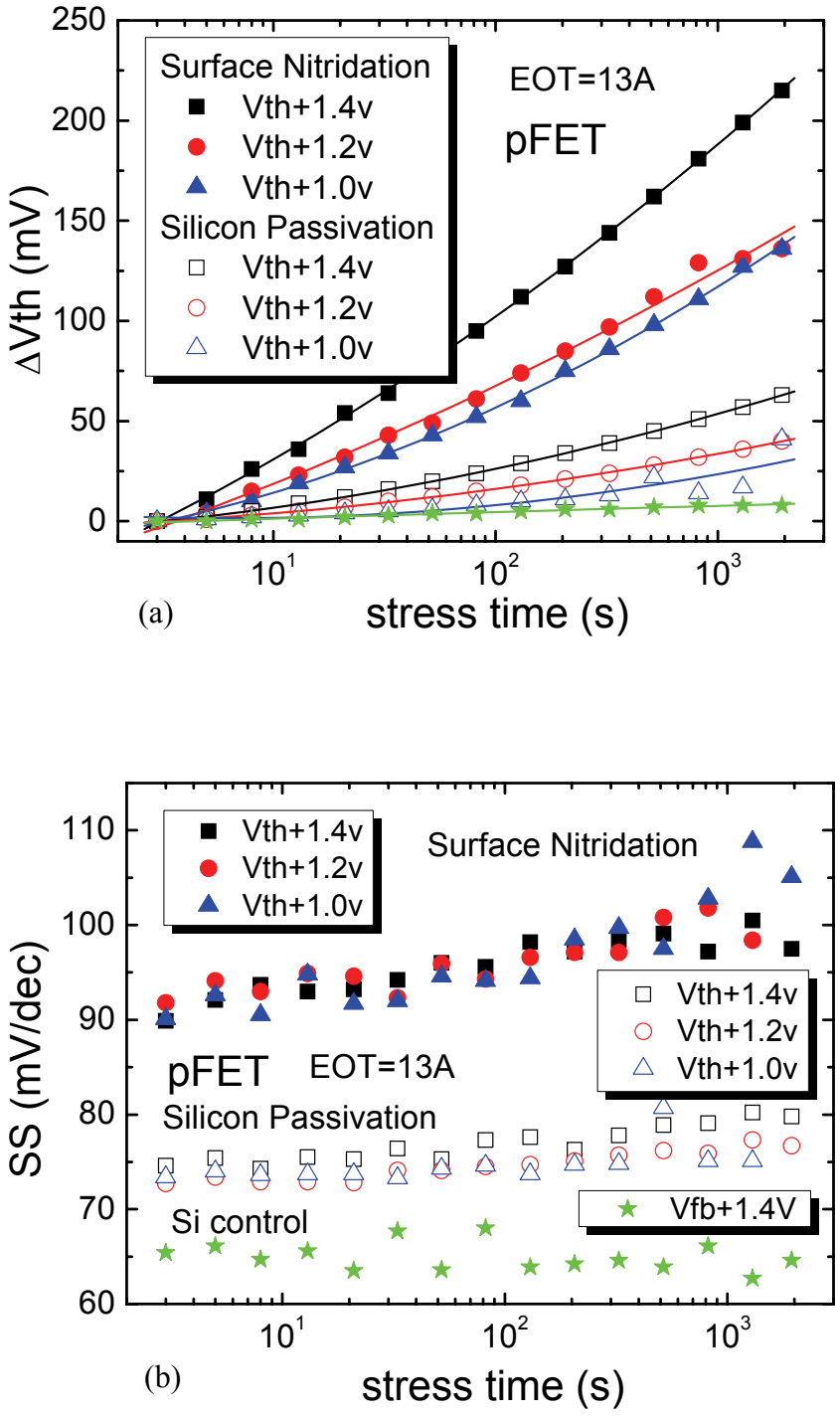


Figure 6.6 Threshold voltage shift (a) and Sub-threshold swing degradation (b) of Ge pMOSFETs under accumulation stress. Si pMOSFET with the same EOT is included as the control device. The stress voltage applied to the gate is indicated for each curve.

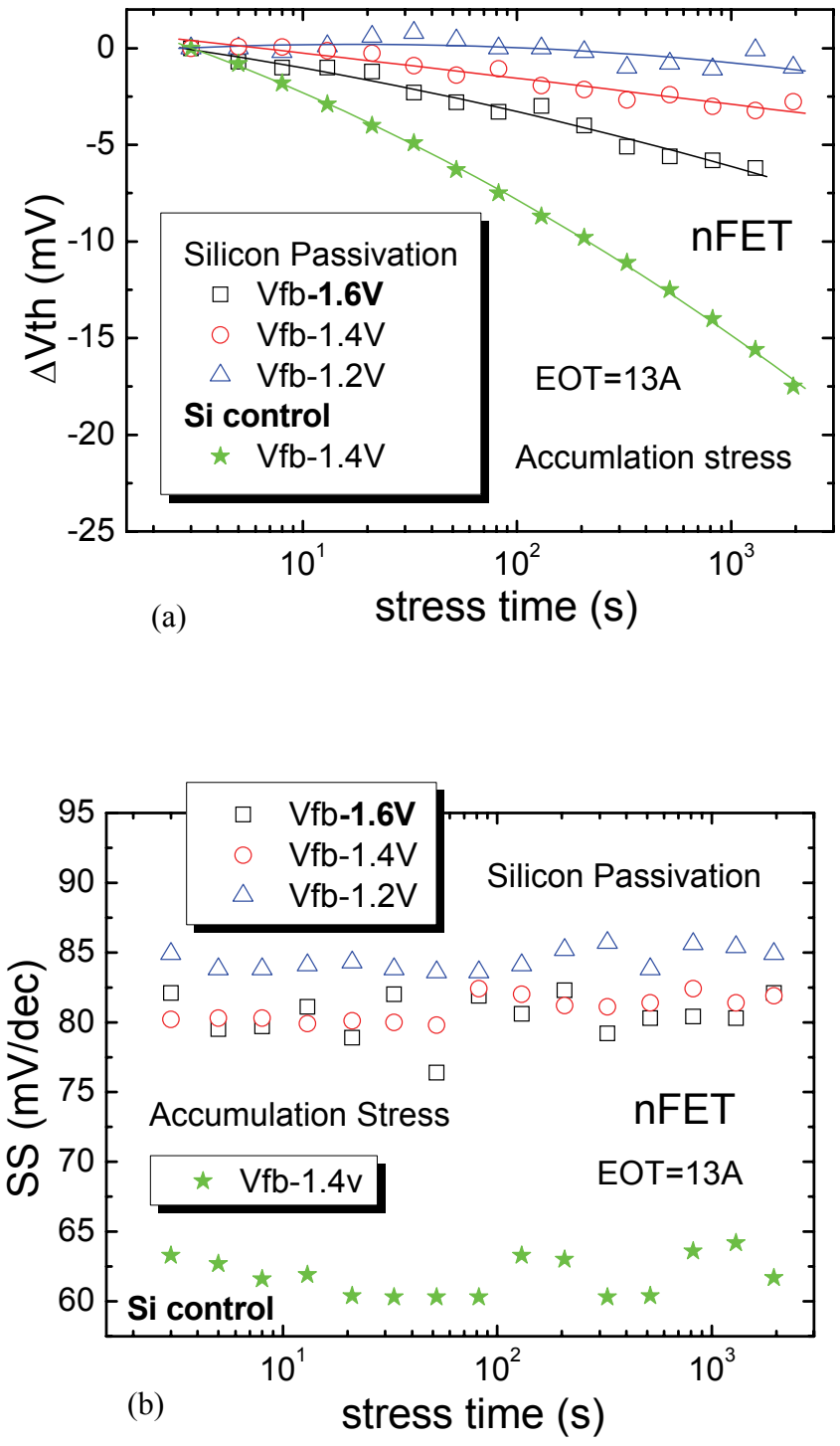


Figure 6.7 Threshold voltage shift (a) and Sub-threshold swing degradation (b) of Ge nMOSFETs under accumulation stress. Si nMOSFET with the same EOT is included as the control device. The stress voltage applied to the gate is indicated for each curve.

6.4 Summary

Threshold voltage instability in the high-k/Ge MOSFETs were studied qualitatively with MOCVD HfO_2 gate oxide. It is found that, similarly to high-k on silicon substrate, BTI is mainly caused by charge trapping. Under negative gate stress, less V_{th} shift and better NBTI for n- and p-MOSFETs were observed at the same time in Ge devices than in Si devices. The reason is probably that there is less hole trapping in the dielectrics of the Ge devices than the Si devices since the Ge devices have a larger valence band offset. For the case of positive gate stress, electrons are injected from the substrate. The charge trapping is more severe for the Ge devices than for the Si devices, probably due to the lower processing temperature which results in more pre-existing traps in the dielectric. Hence, Ge exhibits larger PBTI and V_{th} shift in the n- and p- MOSFET than Si. This imposes an additional challenge for Ge n-MOSFETs development in addition to that of the carrier mobility degradation.

Reference

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Chapter 7

Conclusions

This study focused on gate stack engineering for a germanium MOSFET with high-k gate dielectric. Specifically, fabrication of Ge p- and n-MOSFET with MOCVD HfO_2 for proper electrical performance was studied.

The gate stack formation processes were first characterized by physical analyses. MOS capacitors and FETs were then fabricated for electrical characterization. Surface nitridation was developed as a surface treatment on germanium. The formation of GeON by the nitridation process leads to a reduction of the gate leakage current of the whole gate stack. The experimental data showed that the device was able to meet the leakage requirement for future devices up to the year of 2009. However, based on the electrical result of the p-MOSFETs, nitridation also leads to high density interface states and consequently degrades the channel mobility. To overcome the problem, a novel method of silicon passivation by silane treatment was then developed. The feasibility of the passivation technique was first studied. It was found that the novel passivation process can remove the germanium oxide and passivate the germanium surface with an ultra-thin layer of elemental silicon simultaneously. At the same time, experimental results also agree with the theoretical prediction that the process is robust in terms of film thickness controllability and uniformity. Electrical characterization results also showed that the silicon passivation is more reliable than nitridation and results in comparable Ig-EOT performance. All the MOSFETs are of sub-2nm EOT. More importantly, it can yield lower interface state density and much higher mobility

than the SN process. An 86% improvement of hole mobility over the conventional SiO_2/Si system under high electric field was achieved, which shows that germanium MOSFET could be a promising candidate for advanced VLSI in the near future. The optimal amount of silicon might be related to the deposition technique and the deposition duration of the subsequent high-k dielectrics. Further study showed that most of the interface states might be located within the upper half of the geranium band gap. Moreover, these interface states are acceptor-type interface traps. They are negative charge centers when the n-MOS is under inversion, and hence, could be a major factor that limits the electron mobility of the germanium n-MOSFETs due to Coulomb scattering. These states can also explain the lower degradation in hole mobility that is observed in p-MOSFETs, because they are neutral when the p-MOSFET is under inversion and do not contribute to Coloumb scattering of holes.

Subsequently, Ge n-MOSFET was fabricated successfully by engineering the thickness of the ultra-thin silicon passivation layer and the HfO_2 dielectric. The electron mobility improves significantly with increasing silicon passivation thickness, possibly due to reduction of germanium oxide at the oxide/semiconductor interface. A 61% improvement in peak mobility is achieved over the HfO_2/Si control device.

BTI degradation was investigated qualitatively and systematically on Ge p- and n-MOSFETs with different surface treatments and compared to silicon counterparts. Ge transistors with silicon passivation exhibit less NBTI degradation than its silicon counterparts, probably due to the larger hole barrier in Ge/dielectric compared to that of the Si/dielectric; PBTI degradation of the Ge transistors is more severe than that in the silicon devices, which imposes an important reliability issue for Ge CMOS applications.

There are several limitations with the present study:

(1) Scalability of the electrical gate oxide thickness. For the SiH_4 passivation technique, an ultra-thin layer of silicon is used to seal the germanium surface for the subsequent deposition of high-*k* dielectrics. As a result, the silicon would be changed into a silicate-like layer which is part of the final gate oxide after it is oxidized. This layer would inevitably increase the total effective oxide thickness (EOT) due to its relatively low dielectric constant compared to that of the top high-*k* layer. Hence, it is impossible to achieve the theoretical limit of oxide scalability of high-*k* directly on germanium. Since this problem comes intrinsically with the silicon passivation scheme, the solution is either to increase the dielectric constant of the high-*k* layer for compensation, or to improve the high-*k* deposition technology to reduce silicon consumption during the deposition so that the amount of silicon interlayer can be reduced.

(2) Although it has been demonstrated that silicon passivation can result in significantly reduced interface traps and a doubled hole mobility over that of conventional silicon device for p-MOSFETs, the electron mobility for n-MOSFETs is still very limited. We suggest that this problem is mainly related to the asymmetrical distribution of the interface states that are mainly located in the upper half of the germanium band gap, which consequently leads to a greater reduction in electron mobility than in hole mobility. Detailed XPS investigation shows that germanium oxide still exists at the interface. Therefore, the thickness of the silicon passivation layer may need to further increase to prevent germanium oxide formation. There should be plenty of room to increase silicon layer thickness because the charge centroid of the channel carrier is larger than the silicon layer thickness (10~12Å). This

could guarantee the majority of carriers remain in germanium for mobility enhancement.

Moreover, in contrast to hole mobility, it is reported in literatures recently that electron mobility suffers from remote phonon scattering caused by the high-k dielectrics on silicon. This phenomenon can also be present in germanium substrates, which also leads to the lower electron mobility than hole mobility in Ge MOSFETs. This is also evidenced by the very low electron mobility of the HfO_2/Si control device in this study.

(3) Although high performance Ge MOSFETs have been developed, the real application of a gate insulator requires not only performance but also reliability. For instance, a deeper understanding of hysteresis, charge trapping/detrapping characteristics of the high-*k* dielectric and the interfacial layer on germanium is essential before introducing germanium into circuit application.

As a start, BTI issue was studied qualitatively at room temperature. Although Ge n-MOSFETs exhibit significant PBTI degradation which motivates further study of process development, Ge p-MOSFETs were found to have better NBTI immunity than silicon counterpart. Therefore, it would be good to further study the degradation mechanism quantitatively under various temperatures and stress conditions.

Another issue is that, since the carrier ionization rate in germanium is higher than in silicon, hot carrier reliability of the high-*k* dielectric on germanium is probably a important reliability issue. Nevertheless, it should be noted that the study on all these issues should be accompanied by the study of process technology.

(4) Besides device performance, integrated circuit application of MOSFETs requires other proper parameters like threshold voltage, supply voltage, short channel characteristics, device dimension, etc. For instance, one parameter that is directly

related to the gate stack is the threshold voltage (V_{th}). MOSFETs for integrated circuits require symmetry and precise control of V_{th} for both n-MOSFETs and p-MOSFETs with proper values. As the energy band configuration of germanium is different from that of silicon, the threshold voltage would differ if the oxide and the gate remain unchanged. Another important factor is the oxide fixed charge which also changes the threshold voltage. We have found that this fixed charge is closely related to the process thermal budget. Therefore, further investigation should be carried out to find out the root cause and the possible solution.

(5) So far, we have focused on the gate stack on germanium. It was developed to fulfill the requirement of junction formation in a gate-first self-aligned MOSFET process flow. However, junction technology is also important in order to achieve a good working device. Because of the limited knowledge at this moment, the junction performance of the MOSFETs that we have fabricated is not good. This has, in turn, limited several further investigations on the gate stack, for example, charge pumping measurement and carrier separation stressing. Therefore, research on how to achieve both n+/p and p+/n germanium junctions with good performance is essential. In a complementary way, development of junction technology can be targeted to fulfill the requirement of gate stack formation.

Nevertheless, this study has broken new ground and achieved a reliable technique for Ge CMOSFET fabrication. It can ensure a reliable electrical measurement on the device. Therefore, study on the above issues can be easily carried out with the current laboratory equipment. In other words, this study can be continued to develop the scientific base of the entire Ge MOSFET technology. Many further investigations on Ge MOS system are possible now. Moreover, the high hole mobility

that is achieved in this study shows that germanium MOSFETs could be a promising way to fulfill the requirement of VLSI in the near future.

Based on the limitations of this study, there can be 4 direction for further studies:

(1) Gate oxide on germanium. This includes oxide scaling, interface traps reduction, reliability studies. Engineering the HfO_2 dielectric or replacing it with other high-k gate dielectrics is also an important topic for possible reduction of remote phonon scattering.

(2) Threshold voltage engineering. This includes workfunction engineering of the gate electrode and study of oxide fixed charge. The target is to achieve proper function in relatively low process temperature.

(3) Junction technology. Formation of high performance n+/p junction is the main technology barrier. Detailed rapid thermal process or even laser thermal process should be investigated.

(4) Device physics that is related to device dimension and parameter change due to germanium, such as short channel effects, supply voltage scaling, noise, etc. Novel device structure (ultra-thin body GOI, Ge FinFET, etc) on germanium can be investigated to maximize the benefit of germanium on mobility and supply voltage scaling.

One should note that these 4 aspects may have their own process difficulties and requirement. Thus, research on each individual topic should try to fulfill the requirements from the other aspects.

Appendix – Computer programs

(I) The C program for V_{th} extraction

To extract the threshold voltage of a MOSFET, I_D-V_G curve is first measured with small drain bias. The V_{th} extraction is based on a following function,

$$G(V_G, I_D) = V_G - 2 \bullet \frac{\int_{V_{G0}}^{V_G} I_D(V_G) dV_G}{I_D}$$

where V_G is the gate voltage, I_D is the measured drain current which is a function of V_G, V_{G0} is the starting point of the I_D-V_G measurement (in sub-threshold region).

Function (6.1) is linear when plotted as a function of ln(I_D) where I_D(V_G) is exponential (sub-threshold region), and converge to zero when I_D(V_G) is linear (linear region). The definition of threshold voltage is the gate voltage where the dominant drain current changes from diffusion current to drift current. Therefore, Function (6.1)'s transition point (the maximum value for n-MOSFET or the minimum value for p-MOSFET) corresponds to the threshold voltage of the device.

The following is the C program which is for V_{th} extraction. The measured I_D-V_G curve is stored in two arrays: *Vg* [ ] and *Id* [ ]; *data_points* is the total number of data points that are stored in the array of I_D-V_G curve.

```
/* ======= Vth extraction =========*/

float integ, g, gmin, gmax;
int i, j;
for (j=0; j<data_points; j++)
{
        if (j>0)
        {
                if (Id[j]!=-Id[j-1])
                        integ+=0.5*(Vg[j]-Vg[j-1])*(Id[j]+Id[j-1]);
                if (fabs(Id[j])>0)
                        g=Vg[j]-2*integ/Id[j];                    //Function (6.1)
                gmax=max(g,gmax);                                        //Vth nMOS
                gmin=min(g,gmin);                                         //Vth pMOS
        }
}
```

(II) The C program for sub-threshold extraction

The sub-threshold extraction is based on the following equation:

$$S = \frac{V_{G1} - V_{G2}}{\log(I_{D1} / I_{D2})}$$

where (I_{D1}, V_{G1}) and (I_{D2}, V_{G2}) are any two data points on an I_D-V_G curve. The sub-threshold swing is equal to the minimum S that is found in an I_D-V_G curve in sub-threshold region. The following C program is for sub-threshold extraction.

```
/* ============ Sub-threshold extraction ============*/

float sid, ssid;
int j;
for (j=0; j<data_points; j++)
{
        if (j>0)
        {
          if(fabs(Id[j])!=fabs(Id[j-1]))
                  sid=fabs(fabs(Vg[j]-Vg[j-1])/log(fabs(Id[j]/Id[j-1]))*log(10));
          if(sid>0.06) ssid=min(sid, ssid);                    //Id subthreshold slope
        }
}
```

(III) The C program for charge pumping configuration

Charge pumping measurement requires fine tuning of the following measurement parameters: pulse frequency, pulse height, sweeping range, leading and falling edges of the pulses, integration time, number of data for averaging, etc. The transistor should also be isolated properly (by the guard ring). The following *setupCP()* is the C program to program Agilent 4155C + 41501B for charge pumping measurement.

```
/* Measurement Unit Definition:
SMU2   – Source
SMU3   – Drain
SMU4   – Bulk (Substrate)
PGU    – Gate
VSU    – Guard ring
*/

#define V_GAURD -0.2   //Apply voltage to the guard ring for isolation (accumulation)

#define CP_POINTS 41   //Number of data points in a Icp curve
#define CP_STEP 0.02   //Step range per data
#define CP_BASE -0.6   //Pulse base
#define CP_PULSE 0.2   //Pulse Height = CP_PULSE - CP_BASE
#define CP_AV 12       //Averaging data
#define CP_TW 2e-6             //Charge Pumping pulse width
#define CP_TL 7.5e-7           //Charge Pumping leading edge
#define CP_TT 7.5e-7           //Charge Pumping trailing edge
#define CP_TP 4e-6             //Charge Pumping pulse period

ViStatus setupCP()             //Charge Pumping Program
{
ViStatus ViErr;
char cmd[1000];
double base=CP_BASE;
double pulse=CP_PULSE;
int i;

ViErrChk(Write(resource415x, "ST 3\n", 10));      //store program in memory block 3
```

```
ViErrChk(Write(resource415x, "FMT 2,0\n", 10)); //output data format: ASCII without header

sprintf(cmd, "AV, %d\n", CP_AV);                    //compile a command
ViErrChk(Write(resource415x, cmd, 10));             //number of averaging data

ViErrChk(Write(resource415x, "WM 1\n", 10));        //sweep abort condition & post sweep condition

ViErrChk(Write(resource415x, "SLI 2", 10));         //select integration time: med
ViErrChk(Write(resource415x, "MM 1,4,2,3\n", 10)); /*set SPOT measurement unit: SMU4(Ib), SMU2(Is), SMU3(Id) */

ViErrChk(Write(resource415x, "SSP 0, 2\n", 10));      //select PGU input to output channel
ViErrChk(Write(resource415x, "CN 2,3,4,27\n", 10)); //channel enable (SMU1,2,3,4, VSU1, PGU1)
ViErrChk(Write(resource415x, "DV 2, 0, 0,    0.01\n", 10)); //set SMU2(Vs) const voltage=0
ViErrChk(Write(resource415x, "DV 3, 0, 0,    0.01\n", 10));    //set SMU3(Vd) const voltage=0
ViErrChk(Write(resource415x, "DV 4, 0, 0,    0.01\n", 10)); //set SMU4(Vb) const voltage=0

sprintf(cmd, "DV 21, 0, %f\n", V_GAURD);            //compile a command
ViErrChk(Write(resource415x, cmd, 10));       //force VSU1, auto range, voltage=0, compliance=0.01A

ViErrChk(Write(resource415x, "RI 3, 11\n", 10));//set SMU3 measurement range mode=1nA~Autorange

ViErrChk(Write(resource415x, "POR 27, 0\n", 10)); //set PGU output impedance=low

for (i=0; i<CP_POINTS; i++){
        Fmt(cmd,"%s<SPG    27, 2, %f, %f, 0, %f[e],%f[e],%f[e],%f[e],65535\n", base, pulse, CP_TW,CP_TL,CP_TT,CP_TP);

        ViErrChk(Write(resource415x, cmd, 10));
        ViErrChk(Write(resource415x, "SRP\n", 10));                    //force pulse output
        ViErrChk(Write(resource415x, "XE\n", 10));                  //trigger measurement
        ViErrChk(Write(resource415x, "SPP\n", 10));                 //stop pulse output
                base+=CP_STEP;
                pulse+=CP_STEP;
        }

ViErrChk(Write(resource415x, "SLI 1", 10));         //select integration time=short
ViErrChk(Write(resource415x, "CL\n", 10));          //switch OFF and disable channels
ViErrChk(Write(resource415x, "SSP 0, 1\n", 10)); //select SMU to output channel
ViErrChk(Write(resource415x, "END\n", 10));

Error:
   return ViErr;
}
```