NANOMECHANICAL CHARACTERIZATION OF BD (LOW-K) THIN FILMS AND Cu/BD MULTILAYERED STACKS

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A THESIS SUBMITTED
FOR THE DEGREE OF MASTER OF ENGINEERING
DEPARTMENT OF MECHANICAL ENGINEERING

NATIONAL UNIVERISTY OF SINGAPORE
2006

PREFACE

This thesis is submitted for the degree of Master of Engineering in the Department of Mechanical Engineering, National University of Singapore, under the supervision of Assistant Professor Sujeet Kumar Sinha, Professor Andrew A. O. Tay and Dr. Subramaniam Balakumar (IME). No part of this thesis has been submitted for any degree at any other University or Institution. As far as this candidate is aware, all work in this thesis is original unless reference is made to other work. Parts of this thesis have been submitted for publication in the conference proceedings and international journals as stated below:

Publications

Conference:

1. V. N. Sekhar, A. A. O. Tay, S. K. Sinha, S. Balakumar and Lu Shen, *'Nanoscratch and Nanomechanical Studies on Cu/low-k (Black Diamond^{TM}) Multilevel Stacks with Two Different Barrier Layers'* **ICMAT-2005**, 3-8 July, Singapore

2. V. N. Sekhar, S. Balakumar, S. K. Sinha, Lu Shen, A. A. O. Tay, *'Thickness dependence of nanomechanical properties of BD ^{TM} (low-k) thin films'* **2nd MRS-S** conference on Advanced Materials, 18-20 January, 2006.

3. V. N. Sekhar, R. jayaganthan, V. Srinivasarao, K. Mohankumar, A. A. O. Tay, S. K. Sinha and V. Kripesh, *'A Study on The Mechanical Behavior of Au-Ni multilayer'* 13th **PFAM-2004**, 7C-1, (6-8 December) Singapore

4. V. N. Sekhar, R. jayaganthan, V. Srinivasarao, K. Mohankumar, A. A. O. Tay, S. K. Sinha and V. Kripesh, *'A study on The Mechanical Behavior of Au Thin Films by Nanoindentation'* 13th **PFAM-2004**, 7C-2, (6-8 December) Singapore

Journal:

1. V. N. Sekhar, S. Balakumar, S. K. Sinha and Lu Shen, A. A. O. Tay *'Influence of thickness on the mechanical properties of Black Diamond ^{TM} (low-k) thin films'* (In process)

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deepest gratitude to my supervisors, Asst. Prof. Sujeet Kumar Sinha, S. Balakumar (IME) and Prof. Andrew A. O. Tay for their invaluable guidance, supervison, advice and encouragement throughout my postgraduate studies. I especially thank Ms. Shen Lu (IMRE) for helping me in Nanoindentation and Nanoscratch experiments. Mainly I would like to acknowledge Nano Wafer level Packaging Program (NWLP) and NUS for awarding me the research scholarship for my graduate studies and financial support towards my research project.

Many thanks are owed to the Institute of Microelectronics (IME), which provided vital help in accomplishing my research project. I also thank to Dr. Rakesh Kumar and Dr. Lu Dong for their helpful suggestions regarding my research work. I am very thankful to semiconductor fabrication clean room staff for their guidance and help in preparation of my samples. Thanks to IME staff members, Ms. Lai in, Ms. Catherine Li, Mr. Jessen and Ms. Sandy for their help in using the laboratory equipments.

Finally, I would like to thank my parents, room mates, laboratory colleagues and friends for their constant support and help.

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Summary

The IC (Integrated Circuit) industry is gradually migrating from well established Al/SiO_2 technology to Cu/low-k interconnect technology to meet the next generation device requirements [1]. Copper and low-k inter metal dielectric layers are used as multilevel interconnects to enhance the speed of logic devices. Currently, Black diamond ^{TM} (BD, low-k, SiOC:H) has been considered as potential inter metal dielectric material for integration in ULSI (Ultra Large Scale Integration) due to its better electrical and dielectric properties. But in dielectric material processing the key issue is the trade-off between dielectric property and mechanical strength. Hence it is very important to study the mechanical properties of BD films and Cu/BD stacks.

Present study focuses on nanomechanical characterization of BD thin films of different thicknesses, single and dual dielectric stacks with Ta & TaN barriers, and Cu/BD stacks with SiC & SiN cap layers and barriers. Nanoindentation tests with continuous stiffness measurement (CSM) attachment have been performed on all samples to assess hardness (H) and elastic modulus (E) properties. The CSM attachment is preferable because it provides continuous measurement of the hardness and elastic modulus as a function of indentation depth. All nanoindentation tests were performed with a constant strain rate of 0.05 s^{-1}. In addition, adhesive/cohesive strength of the single and multilayered samples was studied by using nanoscratch technique and reported in terms of critical load (Lc). Scratch profiles on all samples were studied by optical and SEM micrographs. Nanoindentation and nanoscratch results of the present study is demonstrated in three parts as 1) thickness dependence of mechanical properties of BD

thin films, 2) BD films with Ta and TaN barriers (single & dual stacks) and 3) Cu/BD stacks with Ta, TaN, SiC and SiN layers.

To study the thickness dependence of mechanical properties of BD films, nanoindentation and nanoscratch tests were performed on BD films of six different thicknesses. The hardness and elastic modulus values obtained of all BD films (100-1200 nm) are in the range of 2.02to 1.66 GPa and 16.48 to 9.27 GPa respectively. Significant thickness dependence of hardness and elastic modulus is observed when thickness is less than 500 nm. In the nanoscratch testing, critical load (Lc) increases as the thickness of BD film increases and is found to be in the range of 13.02 to 25.86 mN.

The H & E of single dielectric stacks are found to be better than the dual dielectric stacks but dual stacks exhibit higher Lc than the single stacks. Presence of barrier layer at the BD/substrate interface doubles the adhesion strength in terms of critical loads when compared with BD film without barrier. Layer by layer delamination is observed in the case of dual dielectric stacks and reported as Lc_1 and Lc_2.

Mechanical behavior of Cu/BD stacks is some what complex due to variation in residual stresses, stacking of different layers, thickness and adherence between interfaces. Stacks with copper over layer exhibit better nanomechanical properties when compared to without copper over layer. No significant delamination is observed between cap layers & BD film and copper & barriers.

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CHAPTER 1: INTRODUCTION

1.1 Background

As Integrated Circuit (IC) technology scales into the nanotechnology regime, it allows millions of active components to be fabricated on a single chip in accordance with the historical trend of Moore's law. A modern integrated circuit chip contains more than 200 million transistors. For integrating all these active elements on a single IC, multilevel on-chip interconnect system must be integrated in BEOL (Back End of the Line) technology [2]. Accordingly, to meet the industry requirements of scaling for improved performance, semiconductor technologies are forced to shift from well-established Al/SiO_2 interconnect technology to Cu/low-k (Copper/low dielectric constant) technology [3-4]. The main purpose of this transition is to reduce cross talk noise between metal lines, propagation delays and power dissipation from RC delay (R= resistance of the metal lines; C=line capacitance). Till recent past, aluminum was the best choice for BEOL interconnects applications in the semiconductor industry. Due to the trend of miniaturization, copper (Cu) is preferred over aluminum (Al) because of its low resistivity (1.76 μΩ-cm) when compared to that for Al (2.62 μΩ-cm). Copper has higher melting point (1083.4ºC) than Al (660ºC) and this property makes Cu more resistant to electromigration failure than Al [5]. Empirically electromigration resistance of Cu is about two times higher than that of Al interconnect [6]. High processing speed of Memory Processing Units (MPUs) can be attained through Cu/low-k technology.

Fig. 1.1 shows the schematic diagram of the chip cross-section, where front end of the line (FEOL) and back end of the line (BEOL) are indicated. In FEOL chip

manufacturing line the circuit elements are fabricated, where as BEOL technology refers to the interconnect layers (Cu), contacts, vias and dielectric layers (low-k). Currently, microelectronic industry is developing many new materials to enhance the device performance, including low-k dielectric materials and diffusion barriers to reduce the RC delay associated with the Cu/low-k multilevel interconnects [3]. Present study concerns BEOL technology where Cu/low-k (Cu/Black Diamond ^{TM}) multilevel interconnects are used for wiring of the transistor chips in FEOL.

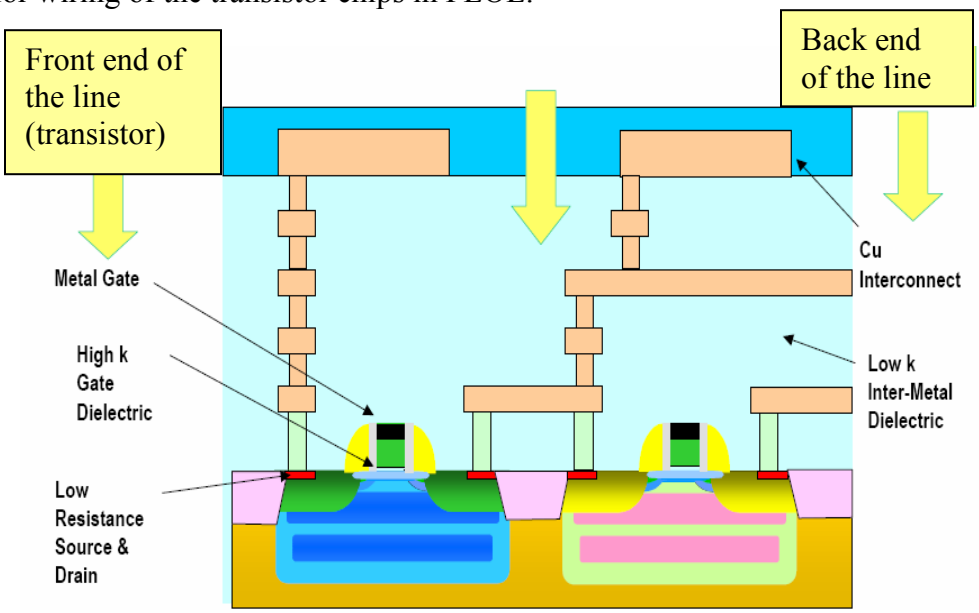


Fig. 1.1 Schematic diagram of cross-section of the IC device.

One of the major challenges associated with low-k materials integration into BEOL (Back End of the Line) interconnect structure is their low mechanical strength. Hence before introducing Cu/low-k materials into the BEOL interconnects a detailed characterization of mechanical properties of the proposed materials is necessary. There are four interdependent properties responsible for the mechanical reliability and they are elastic modulus, hardness, fracture toughness and interfacial adhesion [7]. Parameters

used to characterize the mechanical strength of BEOL interconnect materials include hardness, elastic modulus and adhesion/cohesion strength. Present study focuses on the characterization of hardness and elastic modulus by nanoindentation and, adhesion/cohesion strength by nanoscratch testing. Both theoretical and experimental studies recommend that hardness and elastic modulus are the two key material characteristics affecting the CMP process [8]. The most important challenge lies in producing low-k film that can withstand chemical mechanical polishing (CMP) without low-k film failure.

Generally, mechanical properties of thin films differ from those of the bulk materials. This is mainly attributed to the microstructure and molecular restructuring of the films and the fact that these films are attached to a substrate. Mechanical properties of the thin films can be characterized by microbeam cantilever deflection technique [9-10] and by tensile testing of free standing films [11]. Nanoindentation is a powerful and widely used technique to measure the mechanical properties of thin films. Using this technique both hardness and elastic modulus can be readily extracted directly from the nanoindentation curve. Besides hardness and elastic modulus of the Cu/low-k structure, the most important property in ensuring thermo-mechanical integrity is the thin film interfacial adhesion. Interfacial adhesive failure may occur during fabrication processes such as CMP and high temperature curing steps. In addition, delamination or cracking can also be observed during electronic packaging processes, since there is large difference in thermal expansion coefficients between the chip and the substrate [12]. There are numerous techniques developed for the measurement of thin film adhesion, but among these, scratch test is the straightforward and widely used technique. In the present

study adhesion/cohesion strength of BD films and Cu/BD stacks were assessed by nanoscratch technique and results were reported in terms of critical load (Lc). Both nanoindentation and nanoscratch experiments were performed on Nano Indenter® XP (MTS Corp., USA) system with respective attachments.

1.2 Objectives of the present study

1. *To investigate the effect of thickness on mechanical properties of BD (SiOC:H, Black Diamond ™) dielectric films.* For this study BD films of six different thicknesses; 100, 300, 500, 700, 1000 and 1200 nm were prepared. Nanoindentation and nanoscratch tests were conducted on all these samples (100-1200 nm).

2. *To study the nanomechanical behavior of single dielectric stacks of BD films with Ta and TaN as barrier layers*. Two samples of each single and dual stack with Ta and TaN barriers were prepared for this study.

3. *To study the effect of SiC and SiN cap layers and Ta and TaN barrier layers in nanomechanical behavior of Cu/BD stacks.* This set contains eight samples of different multilayered stacks.

The main intention of investigating mechanical behavior of aforementioned samples relates to the multilayer film structure of the real BEOL interconnect. Accordingly, the present study will be very helpful in assessing the mechanical reliability of various stacks

such as low-k films, barrier layers (Ta & TaN), cap layers (SiC & SiN) and copper layers. In addition it will also give some idea about the material removal rate in the CMP (Chemical Mechanical Polishing) process as this rate depends upon the hardness of the material.

1.3 Thesis organization

Chapter 2 presents literature review of relevant work in the field of Cu/low-k materials focusing on the required properties and mechanical characterization. This is followed by Chapter 3, which describes sample preparation, and nanoindentation and nanoscratch experimental procedures. In chapter 4, results obtained by nanoindentation and nanoscratch experiments are presented. Discussions on nanomechanical behavior of BD thin films and Cu/BD stacks are presented in Chapter 5. Finally, the thesis ends with the conclusions in Chapter 6 and some recommendations to support future research work are provided in Chapter 7.

CHAPTER 2: LITERATURE REVIEW

2.1 Introducing Low-k dielectric material into BEOL interconnects

In the microelectronic industry BEOL interconnect technologies have evolved over the years, and are incessantly changing. BEOL interconnect technology is playing very important role in the development of IC technology. There are numerous driving forces for these changes as the BEOL interconnects are very important in deciding the chip performance [13]. These include miniaturization of device dimensions, increasing the circuit density, lower processing temperatures and integration compliance. All these structures require new architectures, processes and new materials, as semiconductor industry is gradually shifting from well established Al/SiO_2 technology to Cu/low-k interconnect technology.

The introduction of Cu/low-k technology has progressively enhanced the condition when compared to the conventional Al/SiO_2 technology by reducing both resistivity of and capacitance between interconnect lines. BEOL interconnect delay is very crucial in determining signal delay. The RC delay of the BEOL multilevel interconnects increases as interconnect scaling reaches to the nanoscale [14]. At present, copper has become the common metallization material because of its low electrical resistance (1.76 μΩ-cm) and higher melting point (1083.4ºC) when compared to aluminum [15-16]. In addition to RC delay, power consumption and cross-talk between metal lines are the major set backs for BEOL interconnect technology. Continually increasing frequencies and higher densities lead to a significant increase in power

consumption. There are primarily two factors contributing to the power consumption, one is the dynamic power given by

$$P = \alpha C f V^2 \qquad (2.1),$$

where P is the power consumption, α is the wire activity, f is the frequency, V is the supply voltage, and

$$C = C_{output} + C_{wire} + C_{input} \qquad (2.2).$$

Eq. 2.2 depicts the output and input capacitance of the device and capacitance introduced by the interconnect metal itself. The leakage current between multilevel interconnects decides the total power consumption of an IC device. Hence, low leakage is an imperative and supplementary requirement for the low-k dielectric material under consideration [14].

In the trend of miniaturization of IC's for each new generation, approximately $\sqrt{2}$ reduction in device feature size and two fold increase in RC delay is expected [13]. An overview of future projections for BEOL interconnect technology based on NTRS is given in 2.1 [17]. It summarizes the required values of parameters in accordance with miniaturization such as, number of interconnect layers, aspect ratios, metal resistivity and interlayer dielectric constant.

Table 2.1 Characteristic future projections for BEOL technology [16-17].

Year of Production	2003	2006	2009	2012
Minimum feature size (nm)	130	100	70	50
DRAM Bits/Chip	4G	16G	64G	256G
MPU chip size (mm2)	430	520	620	750
Interconnect levels	7	7-8	8-9	9
Metal aspect ratio	2.1	2.4	2.7	3.0
Metal resistivity (μΩ-cm)	2.2	2.2	<1.8	<1.8
Interlayer dielectric constant	1.5-2.0	1.5-2.0	<1.5	<1.5

2.2 The need for low-k dielectric material

So far silicon based dielectrics (SiO_2 and Si_3N_4) have been extensively used as chief dielectrics in interlayer dielectric (ILD) for manufacturing silicon ICs. In Al/SiO_2 interconnect technology, as aluminum metal lines approach 0.18μm in width, the limiting factor is the BEOL interconnect delay caused by the aluminum metal lines and the SiO_2 dielectric material [18]. These interconnect delays also called RC delay. Increasing the interconnect densities will increase unwanted signal delays, unless accompanied by simultaneous decrease in metal resistivity and/or the dielectric constant of insulating media. Figure 2.1 shows the effect of the changing the line and dielectric materials on interconnect and gate delays. This figure also shows that by shifting from Al/SiO_2 to Cu/low-k interconnect technology, the aggregate delay (interconnect and gate delay) will decrease considerably and this shift improves the overall system performance [18]. The low dielectric constant (low-k) film in interconnects, not only decreases line to line

capacitance but also reduces cross talk noise of interconnects and lessen power dissipation issues. The reduced capacitance of low-k material permits decrease of spacing between interconnect metal lines and ability to decrease the number of metallization levels in a device. It eventually leads to lower chip size and cost of the IC processing.

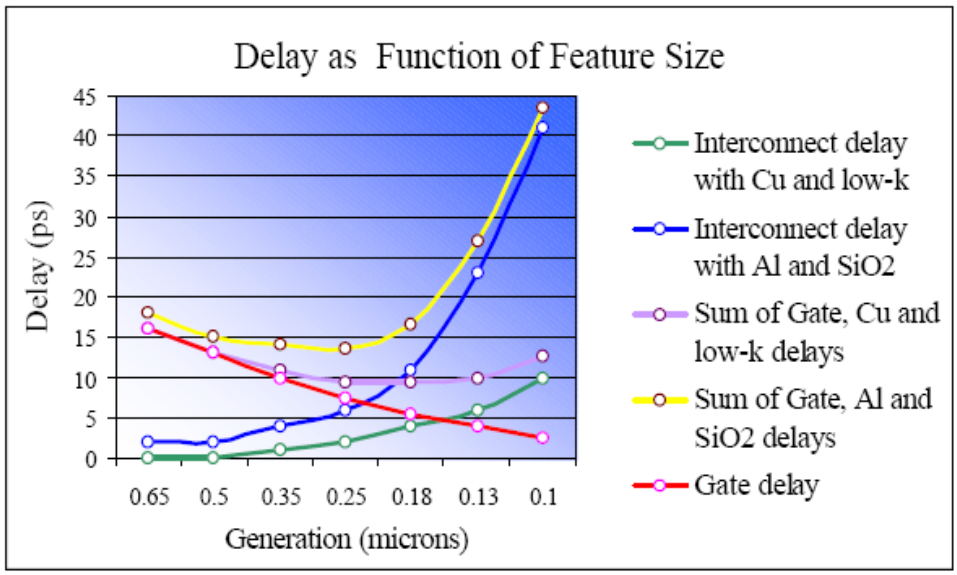


Fig. 2.1 Interconnect and gate delay as a function of device generation [3, 18].

2.3 Classification of low-k materials

Many low-k materials that have been developed in recent past, can be classified into Si-based and non-Si based as shown in Fig.2.2. Si-based materials can be further classified into Si-based and silsesquioxane (SSQ) based, which include hydrogen-SSQ (HSSQ) and methyl-SSQ (MSSQ). Non-Si based low-k materials can be further divided into two groups, polymer based and amorphous carbon. Table 2.2 lists the contemporary deposition techniques together with the k value of various silicon based, non-silicon based and polymer dielectric material candidates for the 0.13µm and 0.1µm technology nodes.

Table 2.2. Dielectric constants of various contemporary low-k materials are the interest of 0.13μm and 0.1μm technology nodes [14, 18-20].

Materials	Application	k value
SiO_2	CVD	3.9 – 4.5
Fluorosilicate glass (FSG)	CVD	3.2 – 4.0
Polyimides	Spin-on	3.1 – 3.4
Hydrogen silsesquioxane(HSQ)	Spin-on	2.9 – 3.2
Diamond-like Carbon (DLC)	CVD	2.7 – 3.4
Black Diamond™ (SiCOH)	CVD	2.7 – 3.3
Parylene-N	CVD	2.7
B-staged Polymers (CYCLOTENE™ and SiLK™)	Spin-on	2.6 – 2.7
Fluorinated Polyimides	Spin-on	2.5 – 2.9
Methyl silsesquioxane (MSQ)	Spin-on	2.6 – 2.8
Poly(arylene ether) (PAE)	Spin-on	2.6 – 2.8
Fluorinated DLC	CVD	2.4 – 2.8
Parylene-F	CVD	2.4 – 2.5
PTFE	Spin-on	1.9
Aerogels/Xerogels (porous silica)	Spin-on	1.1 – 2.2
Porous HSQ	Spin-on	1.7 – 2.2
Porous SiLK	Spin-on	1.5 – 2.0
Porous MSQ	Spin-on	1.8 – 2.2
Porous PAE	Spin-on	1.8 – 2.2
Air Gaps	??	1.0

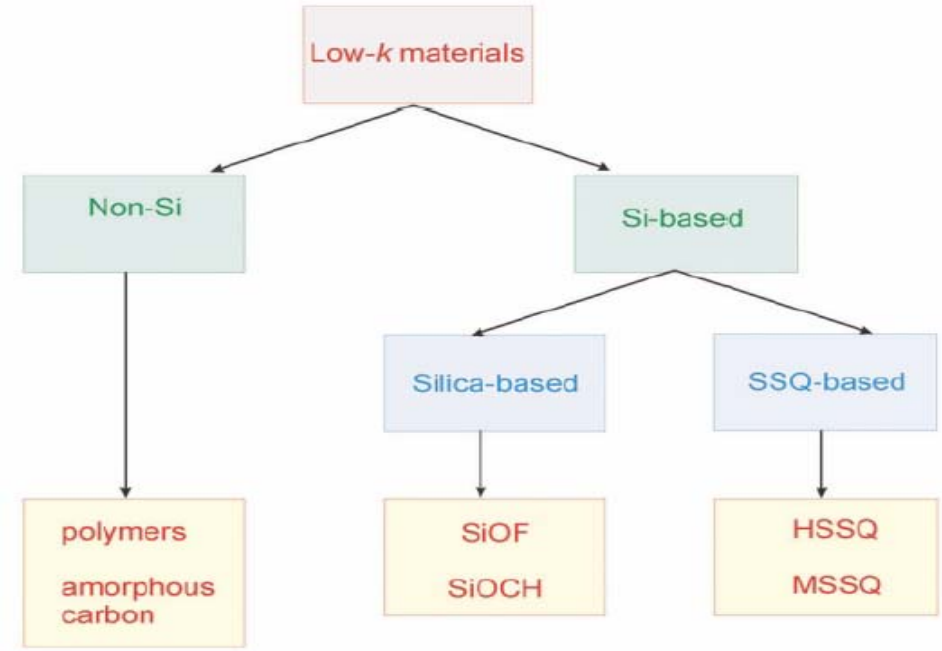


Fig. 2.2 Classification of low-k dielectric materials [21].

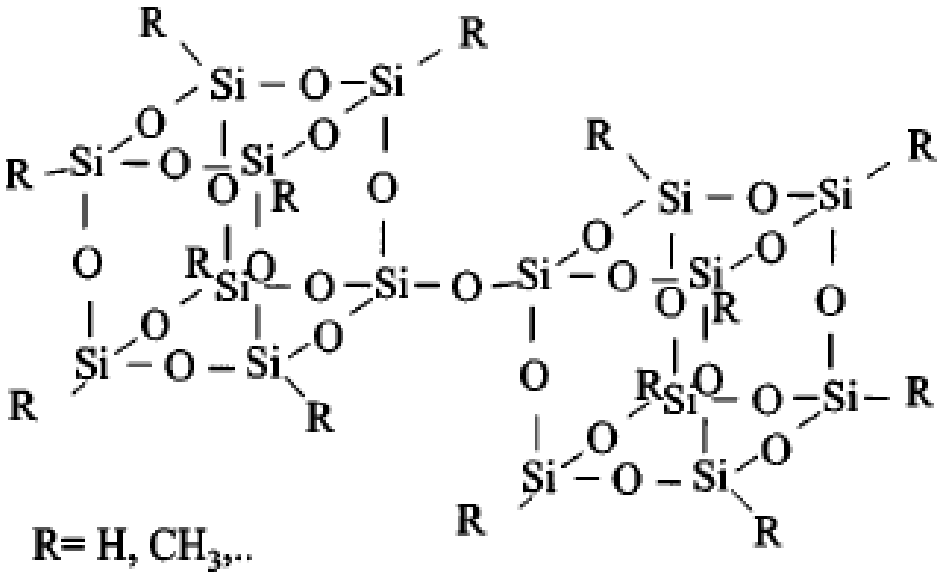


Fig. 2.3 Elementary units of SSQ dielectric materials [14].

2.3.1 Silsesquioxane (SSQ) based low-k materials

In SSQ based low-k materials silsesquixane is the elementary unit. The units contain both organic and inorganic elements, are also called T-resins and have the empirical formula $(R\text{-}SiO_{3/2})_n$. The most common type of SSQ structure can be represented as ladder-type and a cage structure containing eight silicon atoms placed at the corners of the cube, as shown in Fig. 2.3[14]. Organic substituents (-R) in the structure can include hydrogen, alkyl, alkenyl, alkoxy, aryl etc. and these provide low density and low-dielectric constant to the matrix material. The low dielectric constant of this low-k material matrix is mainly attributed to low polarizability of the Si-R bond in comparison with Si-O bond in SiO_2. In microelectronics applications, hydrogen-silsesquioxane (HSQ), and methyl-silsesquioxane (MSQ) are widely used SSQ based low-k materials. MSQ based materials have lower dielectric constant (k=2.6-2.8) when

compared to HSQ based (k=3.0-3.2) ones, because of larger size of the CH_3 groups (their k values have been given in Table 2.2 [14, 22-23]).

2.3.2 Silica based low-k materials

For silica based materials, tetrahedral silica is the elementary unit. Each silicon atom is at the center of the tetrahedron of oxygen atoms as shown in Fig. 2.4 (a). All types of silica structures have dense structures and high chemical and thermal stability. In microelectronic BEOL applications amorphous silica films are widely used. The high frequency dispersion of dielectric constant is mainly related to the high polarizability of the Si-O bonds. Dielectric constant (k) value of the silica based materials can be lowered by replacing the Si-O bonds with Si-F bond, producing fluorinated silica glasses (FSG) or doping with C by introducing CH_3 groups [14]. Carbon doped silicon dioxide, also called Black Diamond ^{TM} (BD), has chemical formula SiOC:H (first introduced by Applied Materials, Inc, USA) [19]. Elementary units of carbon doped silica (BD), with and without cross linking, is shown in Fig. 2.4. This doping by carbon and fluorine increases the interatomic distances or free voids, which results in lowering of k value. The dielectric constant (k) value of silica based dielectrics ranges from 2.6 to 3. Properties of BD low-k material are discussed in detail in the following section.

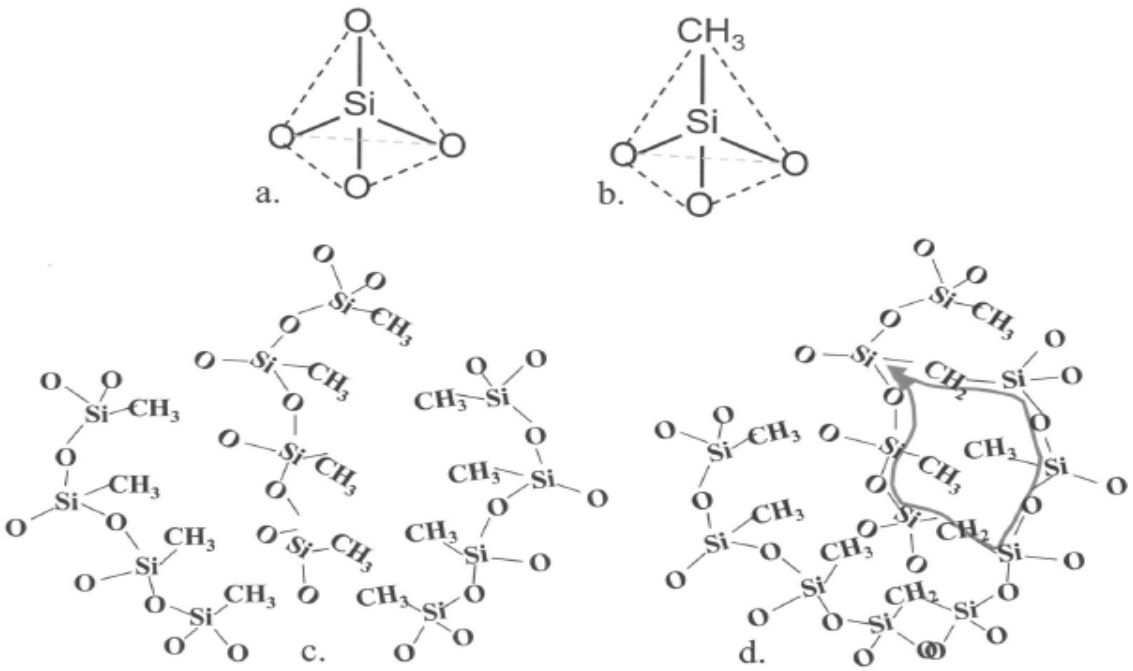


Fig. 2.4 Elementary units of (a) SiO2 (b) carbon doped Silica, called as Black Diamond (SiOCH) (c) C doped silica without cross linking (d) with cross linking [14].

2.3.2.1 Black Diamond ™ (SiOC:H)

Black diamond ™ (BD) is a trade mark of CVD processed dielectric material, introduced by Applied Materials Inc [19]. It is silica based dielectric material, obtained by doping of silica with -CH_3 groups as shown in figure Fig. 2.4 (b). It is also called hybrid dielectric material as it contains both organic (-CH_3) and inorganic (Si-O) constituents.

BD is a low density material formed by Chemical Vapor Deposition (CVD) method near room temperature using organosilane precursor in the presence of oxygen as oxidant. The lower density is achieved by introducing network terminating species (-CH_3) into the Si-O matrix. Addition of the CH_3 group into silica matrix imparts less polar bonds and also creates extra free volume [21]. The density and k value of the BD can be altered by a proper selection of the terminating groups in silica net work. Empirically, a

larger terminating group gives lower density, because it acts as a network terminating group only and it is not part of the Si-O network. Hence BD films retain many of the useful thermo-mechanical properties of silicon oxide. The summary of the properties of the BD are given in Table 2.3. BD films can achieve bulk dielectric constant of around 2.5 to 2.7, and integrated ILD stack dielectric constant of <3 [20]. The glass transition temperature of the BD is well above 450ºC. The dielectric constant of the BD films can be lowered mainly by introducing the constitutive porosity into the microstructure [24]. Good adhesion to barriers, thermal and mechanical properties of BD films provide evolutionary pathway to Cu/low-k interconnect technology.

Table 2.3 Summary of Black Diamond ^{TM} film properties [19, 24].

Property Description	**Value of the Blanket film**
Dielectric Constant-Bulk film(Hg Probe)	2.5-2.7 @ 1 MHz
Uniformity (%, 1σ)	<1.5
Stress (MPa)	40-60 Tensile
Stress Hysteresis (MPa)	<20 (RT-450ºC)
Cracking Threshold (μm; blanket film)	>1.5
ASTM scratch tape test on SiN, SiON, Ta, TaN	Passed
Leakage Current (Amps/cm≤)	10-9 @ 1MV/cm
Glass transition temperature	>450ºC
Hardness (GPa)	1.5 – 3.0
Modulus (GPa)	10 - 20

2.3.3 Organic polymer low-k materials

A large number of organic polymers have been processed, analyzed and reported by many researchers over the last decade [25-27]. These polymers include parylene, poly (naphthalene), polyimides, poly (benzoxazole)s, poly(arylether)s etc. Applicability of some of these polymers in the current BEOL interconnect technology has been limited mainly due to their lower thermo-mechanical strength and incompatibility with the integration processes. Most of the high temperature resistant organic polymers have been preferred as low-k materials in advanced BEOL interconnect. Primarily, aromatic polyimides were the main focus and the main attention was switched to the inclusion of fluorine to decrease the *k* value. Fluorinated polymers such as polyarylene ethers, parylene F, polyperfluocyclobutane and amorphous PTFE-derivatives are being studied for interlayer dielectric (ILD) applications [25].

The aromatic and heteroaromatic polymers were extensively studied because of their high thermal stability and high softening temperatures. Chemical and molecular structure modifications of these organic polymeric materials are being investigated to decrease the dielectric constant and to increase the glass transition temperature. Usually, organic low-k materials with sufficient mechanical strength have dielectric constants in the range of 2.6-2.8 [14].

2.3.4 Amorphous carbon (a-C/DLC) low-k material

This class of low-k polymers is usually deposited by PECVD technique. From a process point of view, amorphous carbon materials are attractive, as the mechanical properties of these materials are closer to inorganic materials. The properties and the

deposition conditions ensure that the resulting films are quite similar to fluorinated aliphatic structures. Limited thermal stability of these films is mainly due to the presence of hydrogen and fluorine. Loss of hydrogen and fluorine on heat treatment of these polymers are observed which results in the formation of carbon double bonds and ultimate graphitization [26]. As the molecular structure becomes dense, the higher the dielectric constant the higher is the thermo-mechanical strength. Grill et al. [28] have demonstrated the integration of the amorphous carbon films with dielectric constants between 2.7 and 3 into BEOL Cu/low-k interconnect technology.

2.4 Required properties of low-k materials

There are several requirements of the dielectric materials in addition to just having low dielectric constant. Table 2.4 summarizes the required electrical, chemical, mechanical and thermal properties of newly developed low-k materials. Choosing a new low-k material with optimal electrical, thermal and mechanical properties for current interconnect technology is very demanding. This is because lower dielectric constants are obtained by modifying of the molecular structure of the materials, which eventually affects the mechanical and thermal properties of the low-k materials. Good thermal stability and low coefficient of thermal expansion is needed to prevent both, damage to the film and, property changes during subsequent thermal processing. The bulk dielectric constant of the ILD stack, when low-k film is stacked with barrier layers and liners (SiC and SiN) should be less then 3.0. It is not recommended to combine the low-k material with highly capacitive barrier layers, because obtaining overall effective k value is the key to BEOL interconnects.

Table 2.4. Summary of required properties of low-k materials [18].

Electrical	**Chemical**	**Mechanical**	**Thermal**
Isotropic k < 3 @ 1 MHz	No material change when exposed to acids, bases and strippers	Thickness uniformity <10% within and <5% wafer to wafer for 8" wafer at 3σ	T_g > 400°C
Low Dissipation	Etch rate and selectivity better than oxide	Good adhesion to metal and other dielectrics	coefficient of thermal expansion <50ppm/°C
Low leakage current	<1% moisture absorption at 100% relative humidity	Residual stress <(±)100MPa	Low thermal shrinkage
Low charge trapping	Low solubility in H_2O	High hardness	< 1% weight loss
High electric field strength	Low gas permeability	Low shrinkage	High thermal conductivity
High reliability	High purity	Crack resistance	
High dielectric breakdown voltage > 2-3 MV/cm	No metal corrosion	Tensile modulus >1GPa	
	Long shelf life	Elongation at break >5%	
	Low cost of ownership	Compatible with CMP	
	Commercially available		
	Environmentally safe		

2.5 Copper as new interconnect material

BEOL interconnect technologies have equally grown as the IC device scaling advanced and played a vital role in improving device performance [29]. Over past four decades aluminum metal was the work horse for the interconnect technology in the production of ICs. High resistance, poor electromigration resistance and lower melting point of aluminum is the major set back for the current interconnect technology which results in an increase in the RC delay of the device. In the current BEOL interconnects the RC delay can be lowered by replacing aluminum interconnects with lower resistivity metals such as silver, gold and copper. Among these interconnect metals, copper is the most popular due to its optimal conductivity, electromigration resistance and cost of fabrication, when compared to other interconnecting metals [13]. Silver exhibits lower

electromigration resistance while gold has marginal lower resistivity and both metals suffer from some integration issues. Table 2.5 summarizes the properties of interconnect metals under consideration, such as electrical properties, mechanical properties and integration compatibility [30].

The IC device performance can be obtained by decreasing the dimensions of the gate length, dielectric thickness and junction depth, also called as device scaling. On the contrary, BEOL interconnects still have to overcome the resistance (R) produced due to decrease in cross-section area of interconnect metal and increased capacitance (C) due to inappropriate aspect ratio. It is collectively being called as RC delay of the circuit. This unwanted RC delay can be lowered by using lower dielectric constant materials (low-k) associated with low resistivity metal (Cu). Besides lowering the RC delay, the low-k material also optimizes the power dissipation and cross talk of the interconnect wiring [31]. In accordance to meet the requirements of prevailing BEOL interconnect technologies, the semiconductor industry is gradually switching from well established Al/SiO_2 technology to Cu/low-k technology.

Table 2.5 Comparison of properties of interconnect metals [30]

Property	Metal				
	Cu	Ag	Au	Al	W
Resistivity ($\mu\Omega$ m)	0.0167	0.0159	0.0235	0.0266	0.0565
Young modulus $\times 10^{-4}$ (MPa)	12.98	8.27	7.85	7.06	41.1
TCR $\times 10^{3}$ (K^{-1})	4.3	4.1	4	4.5	4.8
Thermal conductivity ($W m^{-1}$)	398	425	315	238	174
TEC $\times 10^{6}$ (K^{-1})	17	19.1	14.2	23.5	4.5
Melting point (K)	1358	1235	1337	933	3660
Specific heat capacity ($J kg^{-1} K^{-1}$)	386	234	132	917	138
Delay ($ps mm^{-1}$)	2.2	2.2	3.2	3.7	7.8
Thermal stress on Si (MPa K^{-1})	2.5	1.9	1.2	2.1	0.8
Corrosion in air	Poor	Poor	Excellent	Good	Good
Adhesion to SiO_2	Poor	Poor	Poor	Good	Poor
Deposition					
Sputtering	✓	✓	✓	✓	✓
Evaporation	✓	✓	✓	✓	✓
CVD	✓	?	?	✓?	✓
Etching					
Dry	?	?	?	✓	✓
Wet	✓	✓	✓	✓	✓

2.6 Barriers/Adhesion promoters for Cu/low-k structures

Copper interconnects in BEOL technology have some challenges such as, poor adhesion to dielectric materials and diffusion of copper into silicon substrates. Copper easily reacts with silicon and forms copper silicide at low temperatures [32-33]. Traces of copper in silicon substrate will cause adverse effect on device operation. Interconnect metals under consideration (e.g. Cu, Ag, Au and W) except Al; do not bond well to underlying substrate and ILD. Therefore, the use of diffusion barrier layers and adhesion promoters between copper and underlying silicon substrate in ICs is mandatory. It is beneficial to use a material which acts as diffusion barrier and adhesion promoter.

Over last decade, many researchers have studied the applicability of various metals as diffusion barriers/adhesion promoters [34-35]. An idealized diffusion barrier should also act as an adhesion promoters. Diffusion barriers under consideration are metal nitrides, carbides and borides, and metals such as Ti, Ta, and W. Diffusion barrier should be immiscible and non-reactive with copper. As stated by the studies, sputtered Ta and TaN films act as excellent diffusion barrier layers in Cu/low-k multilevel interconnects [36-37]. In the present investigation Ta, TaN, SiC and SiN are studied as barrier layers/cap layers in Cu/low-k stacks. SiC and SiN diffusion cap layers also acts as etch stops during the BEOL processes. Silicon nitride is widely used cap layer; first, because it acts as an excellent barrier to copper and second, because of it's etch selectivity to oxides.

2.7 Nanomechanical characterization of low-k thin films and Cu/low-k interconnect structures

Millions of active devices are fabricated on a single chip as the IC technology reaches nanoscale regime. The RC delay associated with these technology advances limits the device speed significantly [38]. In an attempt to overcome this limitation, the IC industry is gradually shifting from Al/SiO_2 technology to the Cu/low-k technology. This transition brings the challenges in terms of poor thermal and/or mechanical properties of low-k thin films and Cu/low-k stacks [1]. Hence, it is very important to study the mechanical properties of different Cu/low-k structures to evaluate the device reliability. In the present investigation, hardness, elastic modulus and adhesion strength of various Cu/low-k structures are studied by nanoindentation and nanoscratch techniques.

2.7.1 Mechanical characterization by Nanoindentation

Nanoindentation is a powerful technique and has been widely used for the mechanical characterization of various low-k thin films and Cu/low-k stacks. This technique is widely used to measure the thin film mechanical properties, including hardness, elastic modulus, film–substrate adhesion strength, residual stresses, time dependent creep, fatigue and fracture toughness, which have potential applications in microelectronic industry. It is also employed to evaluate the structural homogeneities of various thin film systems, such as diffusion gradients, precipitates, grain boundaries and surface modifications. The detailed mechanism and testing procedure of nanoindentation will be discussed in the next chapter (Experimental).

The dielectric properties of the low-k materials are altered by modifying molecular structure of the material, eventually to attain the desired *k* value [14]. One rational way to reduce the dielectric constant is by introducing pores into the material without changing the chemical composition, as air has dielectric constant of unity. Usually, the pore size is of the order of several nanometers, and it compromises mechanical properties of low-k films such as hardness, elastic modulus and fracture toughness [1]. Mechanical reliability and dielectric constant are mutually dependent and have inverse relation. For SiO_2 based low-k materials, dielectric constant strongly depends on the density of the material, which in turn also depends upon the amount of porosity introduced, as shown in Fig 2.5. Dielectric constant of low-k material can be determined by using mixture rule, y=0.99+1.334x, as given in Fig. 2.5 [39]. For chemical vapor deposition (CVD) based low-k materials, dielectric constant is decreased by the introduction of terminal methyl ($-CH_3$) groups, that will break the Si-O network and create nanopores. As the concentration of Si-O bonds decreases, percentage of pores and density non-uniformity increases, ultimately increasing the probability of mechanical failure of low-k films.

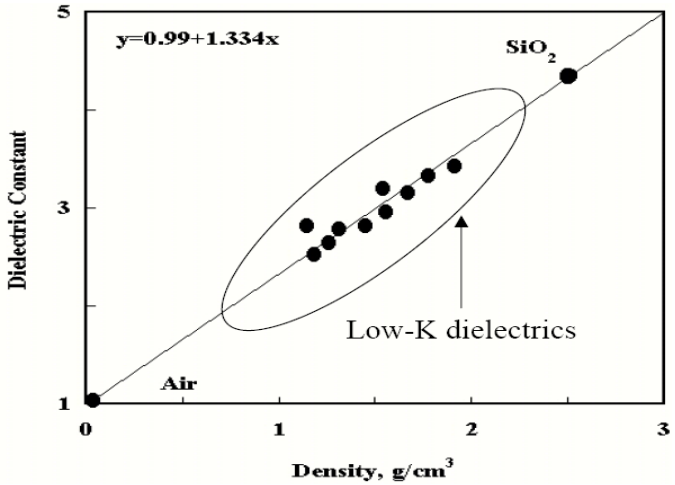


Fig 2.5. Dielectric constant dependence on low-k material density [39].

In Cu/low-k technology, producing a low-k material that can endure chemical mechanical polishing (CMP) without failure is the critical issue. Over last decade, many researchers have been working toward finding threshold values of hardness and elastic modulus that can provide Cu/low-k system the ability to withstand CMP and wirebonding processes [40-42]. Researchers at Motorola [43] have concluded that passing the CMP process of low-k material is not a simple factor of modulus, hardness, adhesion or toughness, but a combination of all of these properties. Hence methods i.e. nanoindentation and nanoscratch tests employed to characterize these properties are very critical. As stated before, the mechanical properties of low-k films depends on chemical structure, amount of porosity and composition, elastic modulus varies from 2 to 14 GPa and hardness varies from 0.5 to 7 GPa [41-45]. Volinsky et al [1] have found a linear relationship between hardness and elastic modulus for silicate low-k dielectric films in nanoindentation testing with continuous stiffness measurement (CSM) attachment. In nanoindentation testing, mechanical response of low-k films is different from the metallic films and usually exhibits little or no plasticity [39]. Hardness and elastic modulus values of various low-k films and Cu/low-k stacks were tested with nanoindentation technique by many researchers and some of those results have been summarized in table 2.6. Based on the extensive literature survey and the present work, it is observed that the mechanical properties of various films and Cu/low-k stacks depend on many factors, more importantly the amount of porosity (Constitutive and Subtractive), composition, molecular structure, thickness, the type of stack and diffusion barrier.

Table 2.6 Mechanical properties of various low-k materials studied by nanoindentation technique.

Low-k thin film or Cu/low-k stack (Si as substrate)	**Thickness (nm)**	**Elastic Modulus (GPa)**	**Hardness (GPa)**	**Researcher**
Organo Silicate Glass (OSG)	2000	6.6-8.4	1.2-1.7	A.A. Volinsky et al [1]
USG (undoped silicate glass)	200-1000	79.06-80.66	5.65-7.52	Lu Shen et al [44]
SiLK ™	600	0.4	6.65	Lu Shen et al
Porous SiLK ™	600	0.26	5.34	[45]
MSQ –Hard	500-1000	12.5	0.936	S. Y. Chang et
MSQ-Soft	500-1000	2.7	0.19	al [46]
Low-k/barrier/Si (Anonymous)	1000	0.5	0.05	I. S. Adhihetty et al [43]
Porous low-k (carbon base)	250-540	4	0.15	Y. H. Wang et al [47]
Porous low-k (silica base)	250-540	0.35	0.45	

2.7.2 Adhesion/Cohesion strength of low-k films and Cu/low-k stacks by Nanoscratch testing

Basic adhesion is used to signify the summation of all interfacial intermolecular interactions. It can also be defined as “the state in which two surfaces are held together by interfacial forces which may consist of valence forces or interlocking forces or both” [48]. There are various theories and mechanisms to explain adhesion phenomenon, but there is no single theory that can explain all aspects of adhesion behaviors [49]. Basic adhesion refers to the interfacial bond strength and mainly depends on the interfacial properties, without any contribution from any other sources. The interactions between the substrate and thin film may be chemical, electrostatic or van der Waals type. To define or

study the basic adhesion phenomena, the interfaces between the adhering phases must be well defined. Experimentally, adhesion strength is the stress required to detach a coating from the substrate. Currently, there are numerous techniques being developed for the measurement of thin film adhesion by using different sample geometries [50]. These include simple scotch tape test, pull-off methods, shock wave loading, indentation test and scratch tests [14, 51]. Among them scratch test on micro- and nanoscales is a widely used technique to measure adhesion/cohesion strength of thin films [49, 52-54]. This is a simple method in which a diamond stylus is drawn across the film under ramp loading (increasing load) until some well defined failure occurs at a load which is often termed as critical load, Lc; usually no special sample preparation is required. Heavens [55] was the first person to introduce the scratch test to measure adhesion strength of the films. In the present study, adhesion/cohesion strength is measured by using nanoscratch technique. All nanoscratch tests were performed on Nano Indenter® XP (MTS Corp. USA) equipment with scratch testing attachment.

In BEOL multilevel interconnects, low-k/substrate and Cu/low-k interfacial adhesion strength is very important for device reliability [56]. Interfacial delamination and mechanical failure of these multilevel interconnects are mainly caused by thermal stresses, residual intrinsic stresses created during deposition, chemical mechanical polishing (CMP) and wire bonding processes, which ultimately results in adverse effect on reliability of microelectronic devices [57]. In the multilevel interconnect thin film structures different failure modes are observed which comprise coating detachment/delamination at the interface (adhesive failure), through-thickness cracking (cohesive failure) and plastic deformation or cracking in the coating or substrate [58-61].

Bull et al [62] characterized scratch failures based on the both substrate and thin film hardness as shown in Fig. 2.11. In an actual nano-/micro-scratch testing, several failure modes may happen concurrently and it may make the scratch interpretation of the scratch test results very difficult [62]. Ye et al [63] studied the adhesion and cohesion strength of two types of SiC/low-k/Si stacked layers by nanosctach technique using Triboscope (Hysitron Inc. USA). Chang et al [46] conducted microscratch experiments on soft and hard methyl silsesquioxane (MSQ). They also studied simulated deformation of damascene structures by micro-scratch tests.

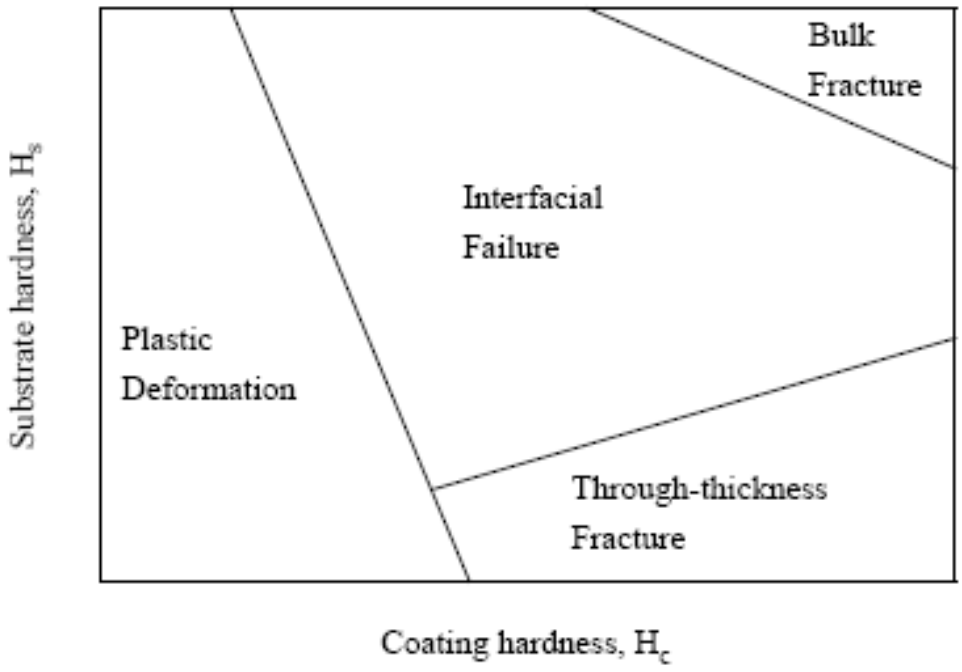


Fig. 2.6 Schematic representation of various scratch test failure modes as a function of coating hardness (H_C) and substrate hardness (H_S) [62].

2.8 Summary

The literature review presented in this chapter has investigated the need of low-k materials, types of low-k materials, and the necessary electrical and mechanical properties. Amongst various types of low-k materials, SSQ based materials, silica based and organic based materials are discussed in detail. Molecular structures, mechanical and electrical properties of the BD films are discussed as the present study focuses on the mechanical characterization of the same. We have also discussed copper interconnects and barrier layers in this chapter. Physical properties, electrical properties and integration compliance of various interconnect metals have been discussed. The reasons behind the selection of copper as interconnect metal over aluminum are explained logically. Nanomechanical characterization of various low-k materials and Cu/low-k stacks by some investigators have been discussed and summarized, as the primary objective of this thesis is the nanomechanical characterization of BD films and Cu/BD stacks.

CHAPTER 3: EXPERIMENTAL DETAILS

3.1 Sample preparation

Materials used in the present work include BD thin films, copper interconnect layer and barrier layers. Different stacks of these layers were deposited by different experimental techniques. All thin film samples were prepared on 8" Si (100) wafer in semiconductor fabrication plant of class 1000 clean room environment. A thin oxide layer of thickness about 5 nm is deposited on the surface of silicon substrates to improve the adhesion between the substrate and the low-k thin films. The schematic diagram of a typical Cu/low-k stack with TaN barrier layer and SiN cap layer is shown in Fig. 3.1.

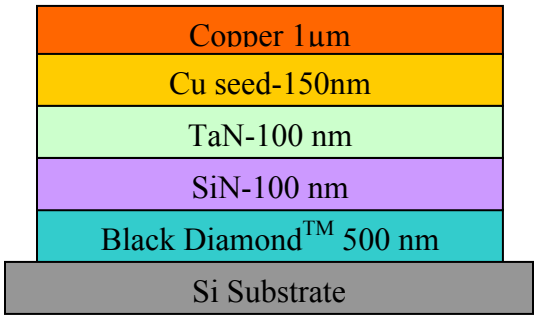


Fig. 3.1 Schematic diagram of a typical Cu/low-k stack.

The equipments used for sample fabrication are described below.

3.1.1 PECVD (Plasma Enhanced Chemical Vapor Deposition)

It is an important deposition technique in the semiconductor fabrication of various thin films of dielectric materials such as SiC and SiN cap layers. In this process, high energy is supplied to reactant gases of the plasma, so that reactions needed for deposition can occur at lower temperatures than other processes.

All BD™ (SiOCH) low-k films were deposited using parallel plate PECVD system (manufactured by Applied materials Inc. USA) using 13.56 MHz radio frequency

power supply. In PECVD process helium is used as the carrier gas to minimize the ion bombardment during growth of the films. The precursors used in the process were trimethylsilane (3MS) and oxygen (O_2), and the gas mix flow ratio of 3MS/O_2 was maintained at around 6. The deposition process was carried out at a temperature of 350ºC to obtain good film properties and optimal precursor reaction. The total rf power and pressure of deposition process is maintained at around 600 W and 4 torr respectively.

SiC and SiN cap layers undertaken in this study are also deposited by the PECVD technique. The precursors used for SiC deposition were liquid trimehylsilane and CO_2 gas and for SiN deposition, NH_3 and SiH_4. The working pressure was maintained at around 2.5 torr and power employed for deposition was around 400 W.

3.1.2 Sputtering

In the Cu/low-k stacks, Ta and TaN films of thickness 25 nm were used as diffusion barrier layers. These Ta and TaN barrier layers were sputter deposited by self-ionized plasma (sip) PVD technique using high purity Ta and TaN targets. A copper seed layer is deposited on these barrier layers and it is required for electroplating copper at later stage (see next section). The thickness of copper seed layer used in the present work is 150 nm.

3.1.3 Electroplating

Electroplating (ECP) is most widely used for the deposition of copper interconnects in BEOL technology. In ECP of copper, the wafers are mounted on cathode and immersed into electrolyte that contains Cu ions. Generally, platinum is used as

anode. A voltage is applied between the two electrodes and current drives the Cu ions toward the wafer and thus metallic copper is deposited on the surface as per the electrochemical reaction,

$$Cu^{2+} + 2e^{-} \longrightarrow Cu$$

The Cu seed layer on the thin film surface helps in maintaining the electrical contact. The electrolyte used in copper plating is normally composed of cupric sulphate ($CuSO_4.5H_2O$) and sulphuric acid (H_2SO_4). Cupric sulphate is a convenient source of copper ions and its prime function is to provide high conductivity of the bath. Excellent filling can be obtained with ECP of copper.

3.2 Nanoindentation

Nanoindentation testing is a simple method consisting essentially of indenting the material of interest whose mechanical properties are unknown with another material (called as indenter) whose properties are known. It is a widely used technique to measure mechanical properties of thin films and solid surfaces. These mechanical properties include hardness and elastic modulus, and also, residual stresses, elasto-plastic deformation behavior, creep, relaxation properties, fracture toughness and fatigue. In nanoindentation testing, length scale of penetration is measured in nanometers rather than micrometers or millimeters. The unique feature of nanoindentation testing is the indirect measurement of contact area i.e. the area of contact between the indenter and the specimen. Indenter with known geometry provides an indirect measurement of contact area at maximum load [64]. Hence, nanoindentation testing can also be termed as depth sensing indentation (DSI).

Nanoindentation technique has many advantages.

1. In most of the cases it can be considered as a non-destructive test as it produces very miniscule impressions on the sample surface.
2. It doesn't require any imaging of residual nanoindentation impressions as mechanical properties are determined by the analysis of load-displacement curve alone.
3. It is very convenient and efficient tool for mechanical characterization and reliability of small scale structures, such as thin films for microelectronic and optoelectronic devices, coatings for magnetic, thermal, environmental and tribological applications and implantable medical devices.
4. No special sample preparation is required and small sampling volume can be used for testing.
5. It gives information about elastic and time dependent plastic properties of materials.
6. We can perform nanoindentation tests on the thin film, coating or surface layer without actually removing them from their substrates, but we should take into account of effect of substrate in the extraction of the mechanical property data.

3.2.1 Nanoindentation Testing by Nano Indenter® XP system

In the present work, all nanoindentation tests were performed on Nano Indenter® XP with continuous stiffness attachment (CSM). Nano Indenter® XP is the latest model introduced by MTS Nano Instruments Innovation Center, Oak Ridge, TN, USA [65]. This system provides reliable and fast mechanical testing data on submicron and nano-scale. It continuously monitors the load and displacement of the indenter into the sample

surface during indentation testing. The contact area of the indentation is calculated by the geometry of the indenter. Specifications of the Nano Indenter XP are given in table 3.1. Primarily, it consists of three key parts 1) the indenter head 2) an optical microscope and 3) x-y-z motorized table for positioning of the sample below the indenter, as shown in Fig 3.2.

Table 3.1. Specifications and operating parameters for Nano Indenter XP, (Source: www.mtsnano.com)

Displacement resolution	<0.01 nm
Total indenter travel	2 mm
Maximum indentation depth	~500 μm
Load application	Coil/magnet assembly
Displacement measurement	Capacitance gauge
Loading Capacity: Maximum Load Max. load with high load option Load resolution Load resolution with high load option Contact force Load frame stiffness	 500 mN ~9800 mN 50 nN 50 nN <1.0 μN 1 X 10^7 N/m
Indentation placement: Useable surface area Position control Positioning accuracy Positioning accuracy (for high performance tables)	 90 X 100 mm By mouse 1.5 μm 0.5 μm
Microscope Video screen Objective	 25X (x objective magnification) 10 X

The instrument applies load through a calibrated electromagnetic coil and displacement of the indenter is measured using a capacitive plate transducer. The electromagnetic coil assembly and capacitive plate transducer is attached to the top of the indenter loading head. The load generated by the instrument is the vector product of the current in the coil and the magnetic field of the same. This mechanism of load application is very simple and effective, and it completely separates the load application system and indentation depth measurement system. The load resolution for standard and high load heads is around 50 nN, and displacement resolution is below 0.01 nm. A photograph of the Nano Indenter® XP system is given in Fig. 3.3.

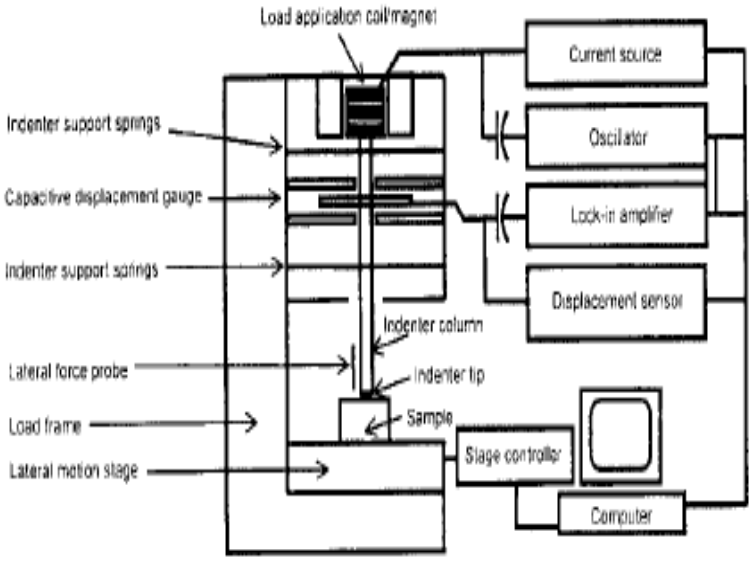


Fig. 3.2 Schematic diagram of Nano Indenter® XP [74].

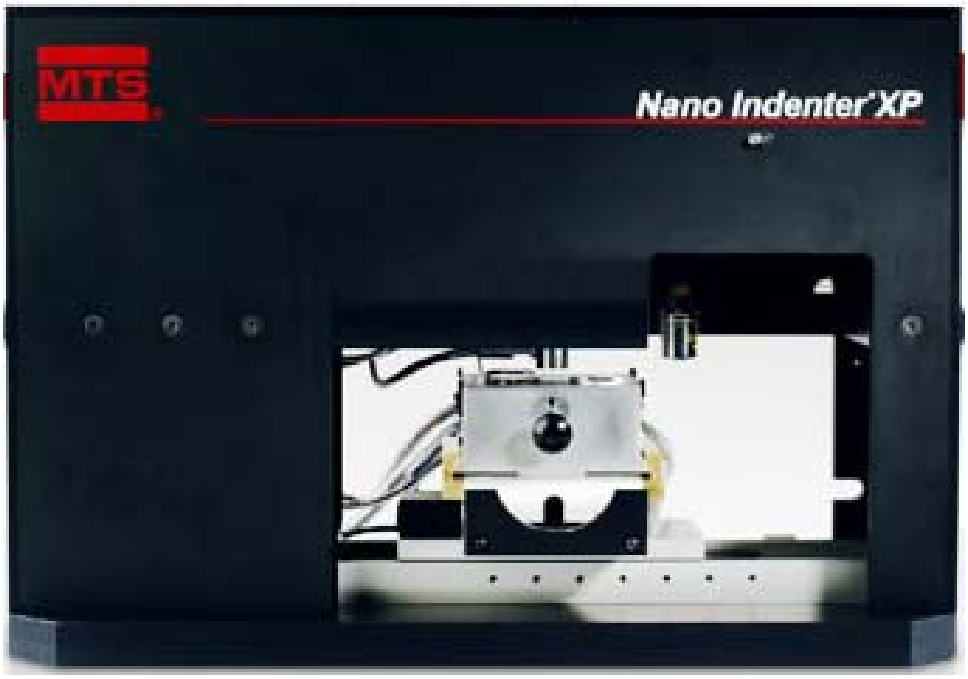


Fig. 3.3 Photograph of Nano Indenter XP system. (Source: www.mtsnano.com)

3.2.2 Indenters

Indentation tests are generally performed by using either spherical or pyramidal indenters. Commonly used indenters in indentation testing are Sphere, Berkovich, Vickers, Knoop, Cube corner and Cone indenters. Among these, Berkovich indenter is very popular and widely used to perform nanoindentation tests. For nanoindentation testing, the indenter should have high elastic modulus, low friction, smooth surface with a precise geometry and should suffer no plastic deformation during indentation.

3.2.2.1 Berkovich indenter

Berkovich indenter is the most popular indenter and widely used for thin film characterization on nano-/micro-scale. It is a three sided pyramid indenter with sharp pointed tip when compared with four sided indenters such as Vickers or Knoop indenters

[64]. Hence it ensures more precise control over the indentation process. Schematic diagram, indent impression and SEM micrograph of Berkovich indenter is shown in Fig. 3.4 and Fig. 3.5 respectively.

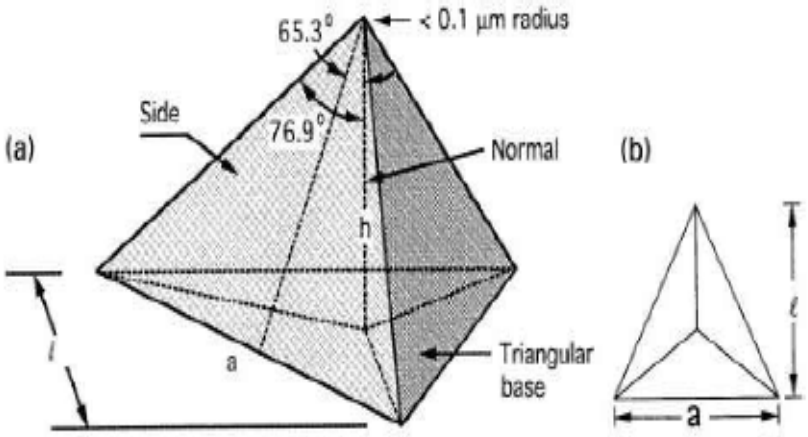


Fig. 3.4 a) Schematic diagram b) nanoindent impression geometry of Berkovich indenter [74].

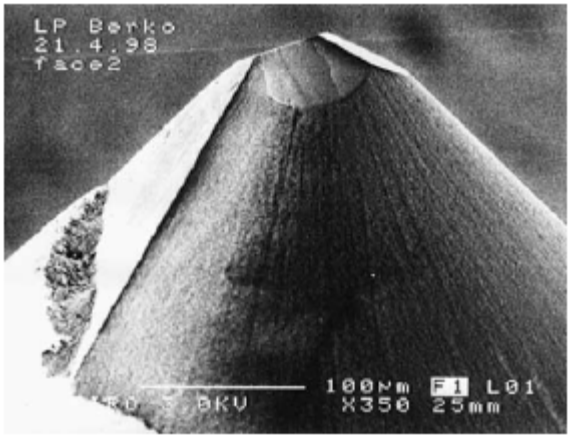


Fig. 3.5 SEM image of standard Berkovich indenter tip [66].

The relation between the contact area and the plastic depth (h_P) of the Berkovich indenter is given as,

$$A = 3\sqrt{3}h_P^2 \tan^2\theta \qquad (3.1)$$

For θ =65.3º, it becomes:

$$A = 24.5h_P^2 \qquad (3.2)$$

Hence the mean contact pressure or hardness [64] is,

$$H = \frac{P}{24.5h_P^2} \qquad (3.3)$$

In indentation testing with Berkovich indenter the term 'mean contact pressure' is used to define the hardness, because the Berkovich indenter was designed to have some ratio of surface area to indentation depth as explained from the above equations.

3.2.3 Indentation testing procedure

Usually nanoindentation test involves penetrating the indenter into the sample surface and measuring the loads and displacements during indentation. The indenter is mounted on a shaft that is made of light-weight and stiff material to minimize compliance and maximize the resonant frequency. Load is typically applied to the indenter shaft by an electromagnetic coil. Displacements are usually measured using changing the capacitance signal. In the present study, all specimens were mounted on an aluminum metal base with commercially available adhesive. The specimen holder is in turn placed on a stage and its movement is controlled by motorized axes with a resolution less than 0.5 μm.

The sample surface is located for every indentation test by lowering the indenter at constant loading rate. The load is increased to maintain a constant loading rate or constant displacement rate. During indentation tests the values of loads and displacements are recorded in the form of loading-unloading cycles. All samples were tested by using standard Berkovich tip as indenter with tip radius around 100 nm. Nanoindentation test consists following steps,

-Approach of the indenter to the sample surface

-Loading on the sample

-Holding of the indenter at a maximum load

-Unloading of the sample.

In some tests multiple loading and unloading steps are carried out to study the reversibility of deformation. Nanoindentation experiments can be carried out either by using constant loading or constant displacement mode [67].

3.2.4 Analysis of nanoindentation data

In nanoindentation testing the load applied on the sample, P and displacement of the indenter into the sample, h (indentation depth), is continuously observed and recorded as load-displacement graph as shown Fig. 3.6. Oliver and Pharr [67] have developed an analytical method to determine the mechanical properties directly from load-displacement curve, without the need to image the hardness impression. Their analysis is based upon relationships proposed by Sneddon [68]. Usually, in a nanoindentation experiment, load is applied from zero to some preset maximum load and then unloaded from maximum load back to zero. If plastic deformation occurs during testing, there will be a residual impression left on the surface of the specimen. A typical deformation pattern of an elastic-plastic sample during and after nanoindentation testing is shown in Fig 3.7 [67]. In general, nearly all engineering materials show real elastic-plastic behavior [69].

From load-displacement curve three parameters must be obtained to assess mechanical properties: 1) the maximum load, P_{max}, 2) the maximum displacement, h_{max} and 3) contact stiffness from initial unloading curve, $S=dP/dh$. The correctness of the

mechanical properties mainly depends on how well these quantities are measured in nanoindentation experiments. The loading portion of the curve is controlled by both elastic and plastic deformation [70]. The unloading portion is controlled only by the elastic property of the indented material.

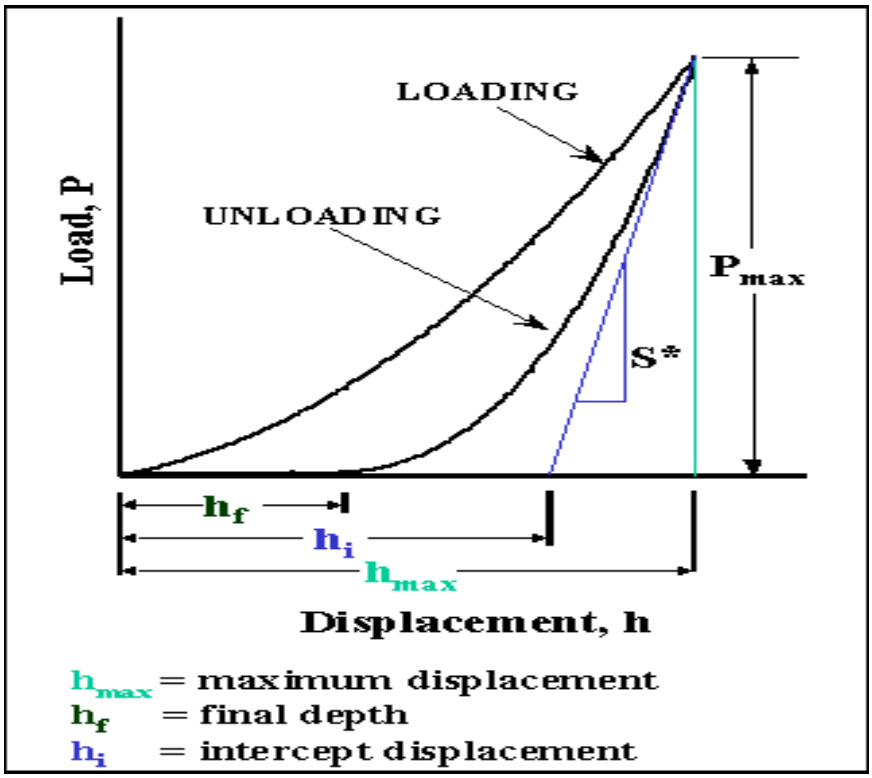


Fig. 3.6 Typical load-displacement curve of nanoindentation experiment [67].

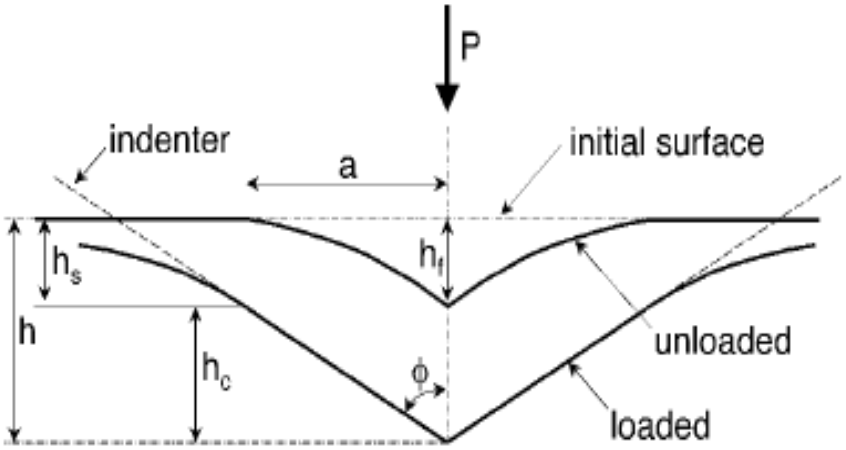


Fig. 3.7 Schematic of specimen surface geometry at full load and full unload in indentation testing [67].

Generally, the relationship between penetration depth, h, and load P can be characterized in the form of power law relation [67],

$$P=\alpha (h-h_f)^m \qquad (3.4)$$

where α is fitting constant which depends upon geometric constants, the sample elastic modulus and Poisson's ratio and the indenter elastic modulus and Poisson's ratio, h_f is the final unloading depth, and m is the power law exponent that is related to the geometry of the indenter; for a flat-ended cylindrical punch, m=1, for a parabolic of revolution, m=1.5, and for a cone and Berkovich tips, m=2. The contact stiffness (S), dP/dh of a material at maximum loading (h_{max}, P_{max}) is given as,

$$S = 2aE_r = \frac{2\beta}{\sqrt{\pi}} E_r \sqrt{A} \qquad (3.5)$$

Where a is the contact radius and A is the projected area of indenter-sample contact. β is used to account for the triangular and square cross sections of the indenters used in the nanoindentation studies. The reduced modulus (E_r) which considers both the indenter and the sample deformation and it is expressed as

$$\frac{1}{E_r} = \frac{(1-\nu_S^2)}{E_S} + \frac{(1-\nu_I^2)}{E_I} \qquad (3.6)$$

Where, E and ν are elastic modulus and Poisson's ratio with subscripts S and I referring to the sample and indenter respectively.

The indenter-sample contact area can be determined by the geometry of the indenter and the contact depth, h_C. Oliver and Pharr [67] stated that, indenter geometry can be described by an area function F (h), which gives the relation between the cross-

sectional area of the indenter and the contact depth of the indenter tip, h. The projected contact area at peak load can be determined from the relation,

$$A=F(h_C) \qquad (3.7)$$

The total displacement, h, of the indenter into the sample at any time during loading is written as,

$$h= h_C + h_S \qquad (3.8)$$

Where h_C is the contact depth and h_S is the displacement of the surface at the perimeter of the contact. The value of h_S depends on the indenter geometry. For a conical indenter, Sneddon's [68] solution for the shape of the surface outside the area of contact can be used to give h_S, as

$$h_S = \frac{(\pi - 2)}{\pi}(h - h_f) \qquad (3.9)$$

Where h_f is the final depth of penetration, at which point unloading begins. The quantity $(h-h_f)$ is used in the equation instead of h, as the Sneddon's [68] solution is applicable to elastic displacement only. The contact depth h_C can be formulated as

$$h_C = h_t - \varepsilon \frac{P_{\max}}{dP/dh} \qquad (3.10)$$

Where ε refers to tip shape constant and for conical tip $\varepsilon = 0.72$ and for a flat punch $\varepsilon = 1$. h_t is the maximum depth, P_{max} is the maximum load and dP/dh is the contact stiffness evaluated at maximum load P_{max}. For a perfect Berkovich indenter, the area is given as

$$A = 24.5h_C^2 \qquad (3.11)$$

The hardness can be calculated by using the following expression

$$H = \frac{P_{\max}}{A_C f(h_C)} \qquad (3.12)$$

The composite modulus or reduced elastic modulus (E_r) can be computed from the following equation

$$E_r = \frac{dp}{dh}\frac{1}{2}\frac{\sqrt{\pi}}{\sqrt{A}} \qquad (3.13)$$

3.2.5 Continuous Stiffness measurements (CSM)

This technique was introduced in the year 1989 by Oliver and Pethica [72-73]. The CSM technique developed over the last decade by researchers offers numerous advantages. It has the unique advantage of providing mechanical properties as a function of penetration depth. Calibration and testing procedure take very less time as there is no need for multiple loading and unloading. High frequencies it allows to avoid obscure effects of the samples like creep, viscoelasticity and thermal drift, which cause much problem in the conventional calibration method. It allows us to measure the effect of contact stiffness changes and damping changes at the point of initial contact [71]. In CSM nanoindentation technique the contact stiffness is measured during loading of the indentation test and there is no need for separate unloading cycles. This is an ideal method to determine contact stiffness and it can measure at very small penetration depths. Hence this method is unique to measure mechanical properties of thin films of few tens of nanometers. It has an additional advantage that if the specimen shows viscoelastic behavior, the phase difference between the force and displacement signals gives idea about the storage and loss modulus of the specimen [64].

In nanoindentation experiment, the CSM technique is carried out by applying a harmonic force at relatively high frequency (69.3 Hz), which is added to increasing load, P, on the loading coil of the indenter as shown in Fig. 3.8. The applied current in this technique is very small, that determines the nominal load of the indenter, which results oscillations to the indenter with a frequency related contact area and stiffness of the sample [82].

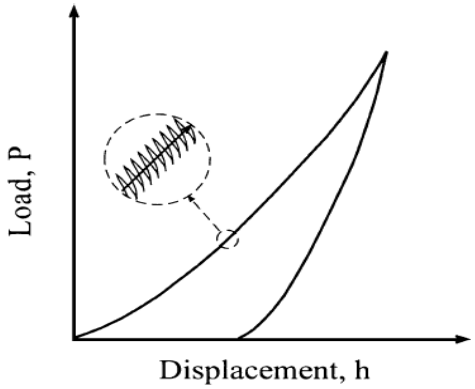


Fig. 3.8 Schematic of nanoindentation CSM load-displacement curve [82].

This technique accurately measures displacements as small as 0.001 nm using frequency specific amplification. To determine the contact stiffness of the sample, the dynamic response of the nanoindenter has to be determined. A dynamic model which is used in CSM system is shown in Fig. 3.9. Major components of the dynamic model are the mass of the indenter, the spring constant of the leaf springs that support the indenter, the stiffness of the indenter frame and the damping constant due to the air in the gaps of the capacitor displacement sensing system.

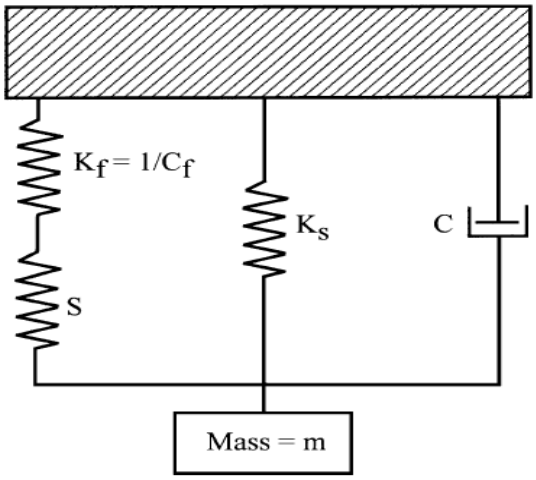


Fig. 3.9 Schematic of components of dynamic model for the indentation CSM system [67].

By analyzing this model, the contact, S, can be calculated from the amplitude of the displacement signal from [82],

$$\left|\frac{P_{OS}}{h(\omega)}\right| = \sqrt{\{(S^{-1} + C_f)^{-1} + K_S - m\omega^2\}^2 + \omega^2 D^2} \qquad (3.14)$$

And the phase angle, ϕ between the driving force and the displacement response is

$$\tan(\phi) = \frac{\omega D}{(S^{-1} + C_f)^{-1} + K_s - m\omega^2} \qquad (3.15)$$

Where

C_f= the compliance of the load frame (~1.13 m/MN)

Ks= the stiffness of the column support springs (~60 N/m)

D= the damping coefficient (~54 N s/m)

P_{os}= the magnitude of the force oscillation

$h(\omega)$= the magnitude of the resulting displacement oscillation

ω= frequency of the oscillation

ϕ = the phase angle between the force and displacement signals

m= mass (~4.7 gm)

3.2.6 Dynamic Contact Module (DCM)

It is a low load dynamic accessory of the existing Nano Indenter® XP system, exclusively used for ultra-low-load mechanical properties characterization. Its operation is similar to the standard Nano Indenter® XP system but provides a high resonant frequency, an increased dynamic frequency range and low damping coefficient. It makes the DCM unit less sensitive to environmental noise than conventional nanoindenters, and with theoretical displacement resolution of 0.0002 nm and load resolution of 1 nN [64]. Hence, DCM is preferred for determining surface forces on an atomic scale. In DCM the indenter column weight is around 100 mg, the system is sensitive to surface forces and dynamics, because it carries very little inertia of its own. The combination of low mass and high resonant frequency has a direct beneficial effect on indenter system performance.

In the present study the mechanical properties of 100 nm thick film were measured using the DCM attachment.

3.2.7 Factors affecting the Nanoindentation results

In nanoindentation testing, load and depth of penetration are continually monitored and recorded as load-displacement curve. This curve is used to determine the mechanical properties especially hardness and elastic modulus. Though theoretically simple, in real practice, various errors are encountered mainly those associated with nanoindentation testing equipment, material related issues and environmental effects. Here, some of these problems are briefly discussed.

3.2.7.1 Indentation size effect (ISE)

Usually, it is expected that for nanoindentation testing of homogeneous and isotropic material same values of hardness and modulus should be recorded, but for a variety of reasons empirically these values often vary with respect to indentation depth. Many materials exhibit indentation size effect (ISE), where hardness decreases as the indentation size or the depth of indentation (or load) increases. Some observed material behavioral effects are due to the existence of very thin oxide films having different mechanical properties, presence of residual stresses and strain hardening arising from the specimen preparation [64]. Friction between the indenter and specimen also causes the ISE [75]. The most frequently observed ISE is mainly due to indenter geometry, especially at very small values of penetration depth.

Several theories have been proposed to elucidate the ISE including artifacts, quantized slip or deformation band formation, existence of strain gradient in indentation stress field, and the low probability of finding mobile dislocations [64, 76]. Hard material exhibit little ISE and in the case of soft materials, especially crystalline materials, significant ISE is expected.

3.2.7.2 Surface roughness

It is very important issue in nanoindentation testing. Surface roughness of the specimen causes errors in the determination of contact area, since the contact area is indirectly measured from the contact depth. Many researchers have proposed analytical models considering the statistical variation in asperity height in real surfaces [64]. Usually, surface roughness is described by the asperity height and spatial distribution of

the asperities across the surface. K. L. Johnson [69] quantified the surface roughness by using roughness parameter α, given as

$$\alpha = \frac{\sigma_S R}{a_O^2} \qquad (3.16)$$

where σ_S is equal to the maximum asperity height, R is the indenter radius, and a_O is the contact radius. From equation 3.16 it is observed that, α depends indirectly on the applied load. According to Johnson [64], the effects of surface roughness on the validity of the equations are of significance for $\alpha > 0.05$. In nanoindentation testing the consequence of surface roughness is to decrease the contact pressure by increasing the contact radius.

3.2.7.3 Thermal drift

In nanoindentation testing, thermal drift refers to change in the dimensions of the sample, indenter and the instrument resulting from temperature variations during the test. The depth sensor, which is used in the nanoindentation system, has a resolution < 1nm and is highly sensitive to temperature changes. Variations in depth sensor output are mainly caused by either creep of the sample or thermal drift. Usually, thermal drift is measured in nm/sec. In nanoindentation testing, thermal drift of few nanometers per second will cause considerable errors in the hardness and elastic modulus values. Thermal drift associated with thermal expansion is most prominent at the contact between the indenter and the specimen.

Feng et al [77] have studied the effect of thermal drift on the calculated elastic modulus values. They have reported that the thermal drift has minimum effect on the determined elastic modulus, if

$$t_h \approx \frac{S}{\left|\dot{P}\right|} h_P \qquad (3.17)$$

Where

t_h = total time of the loading

S=contact stiffness

$\dot{P}$=Unloading rate

h_P = Contact depth at load P.

However thermal drift can be reduced by the following ways,

1) The preferred method is to reduce the thermal variations in the specimen to possible minimum value. It can be accomplished by enclosing the nanoindenter system in insulated cabinet and controlling the laboratory temperature.
2) Correcting the nanoindentation test data for the thermal drift. To accomplish this, usually many of the nanoindentation systems allow for a hold at maximum load for few seconds before unloading starts. In the present study, the load at maximum depth was held constant for ten seconds and indenter was held in contact with sample surface at 10% of the maximum load for 60s before it was withdrawn completely.

3.2.7.4 Piling-Up and Sinking-In

In nanoindentation testing sink-in is associated with elastic materials, when the sample surface is drawn inwards and downwards below the indenter. If the sample undergoes plastic deformation during testing, it may result in either sink-in or pile-up

around the indenter. In completely plastic region this behavior depends on the strain hardening coefficient and the ratio of elastic modulus-yield strength ratio (E/Y) as [64],

$$K=Y\,[E/Y]^{X} \qquad (3.18)$$

The extent of pile-up or sink-in depends on ratio E/Y of the sample material and strain hardening exponent X. Based on the Eq. 3.18, pile-up behavior is most pronounced for non-strain hardening materials with high values of E/Y. Sink-in is more prominent for strain hardening or non-strain hardening materials with low value of E/Y. Materials with pile-up behavior show large values of elastic modulus and low hardness values compared to those obtained by other methods. Correction methods for sink-in and pile-up behavior are different for different type of materials and these corrections are not well characterized yet.

3.3 Nanoscratch testing

Adhesion strength is the load/stress that is required to remove the thin film or coating from the substrate. Scratch test on micro and nanoscale is a widely used technique to measure adhesion of thin films on substrates [51-52]. In the year 1950, Heavens [74] introduced a scratch technique to measure the adhesion of the thin films. A detailed account of the scratch test used in the current work is explained below.

3.3.1 Testing procedure

All nanoscratch tests were performed on the Nano Indenter® XP (MTS Corp. USA) system with nanoscratch option. A diamond stylus of 5 μm radius is drawn across the thin film sample under an increasing load (also called ramp loading) until some well

defined failure (adhesive or cohesive) occurs at a load which is called critical load, Lc. High precision X-Y table was used to locate the sample under the diamond stylus with minimal vibrations and electrical noise. The schematic diagram of the nanoscratch method is shown in Fig.3.10. Two separate capacitive displacement gauges were used to measure the lateral deflection of the indenter column in the X and Y directions. This data is used to determine the coefficient of friction in nanoscratch experiments. Scratch test is performed in sequential steps as, (1) approaching the diamond stylus to the sample surface, (2) Pre-scan: indenting into the sample surface by loading the diamond stylus to 0.02 mN and profiling the pre-defined scratch length, (3) actual scratch test preformed by ramp loading to pre-defined load and with predefined speed, (4) Post-scan: unloading of the diamond indenter back to 0.02 mN to profile entire length of the scratch line one more time.

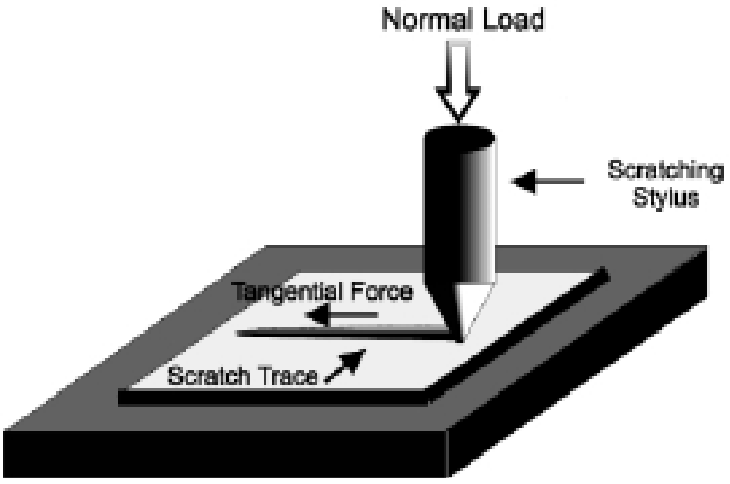


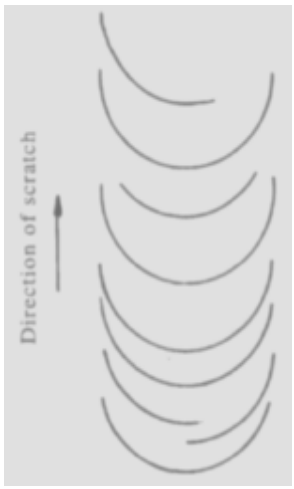
Fig. 3.10 Schematic diagram of nanoscratch testing.

Based on the on the thin film-substrate system under testing, the critical load (Lc) can be determined by acoustic emission, and/or by optical or electron microscopy (SEM, FE-SEM) and/or by variation in the tangential force applied to the system [78]. The critical load (Lc) depends on several test parameters which are both intrinsic and

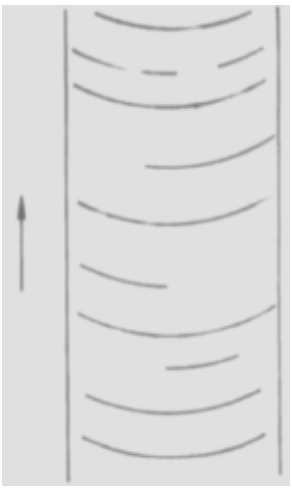
extrinsic. Intrinsic parameters are mainly instrument specific such as scratching speed, loading rate, diamond stylus tip radius and diamond stylus wear. These intrinsic parameters require a careful calibration before the test. Extrinsic parameters are effects of, substrate hardness, coating thickness, thin film roughness, substrate roughness, friction coefficient, residual stresses in the coating and so on. Owing to the dependence of many factors, scratch adhesion test is generally considered as semi-quantitative [62].

3.3.2 Failure modes in scratch adhesion testing

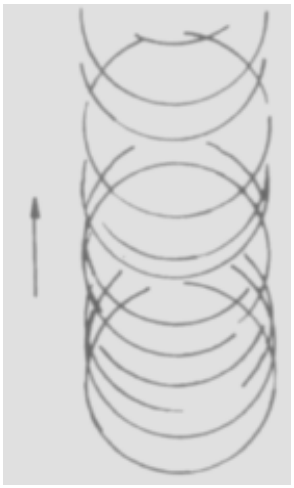
In scratch testing, thin films fail in several different ways and critically depend on the properties of both coating and substrate. In the case of soft coating-hard substrate system, considerable plastic deformation will occur in coating and the critical load can be defined as the load at which the coating is peeled off. However, it is rather difficult to quantify critical load when this type of failure is observed. Usually the type of failure mode depends on the type of scratch loading, scratch test speed, coating thickness, residual stresses in the coating, and indenter radius. In the case of hard coating-soft substrate system, testing interfacial detachment is observed as spallation and buckling failure modes. Buckling and spallation failure can be easily quantified. The failure modes observed in scratch testing can empirically be classified as (1) Through-thickness cracking, (2) Interfacial failure and (3) Chipping in the coating [61].



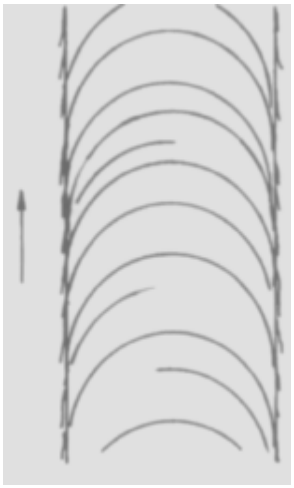
(a) Brittle tensile cracking



(b) Ductile tensile cracking



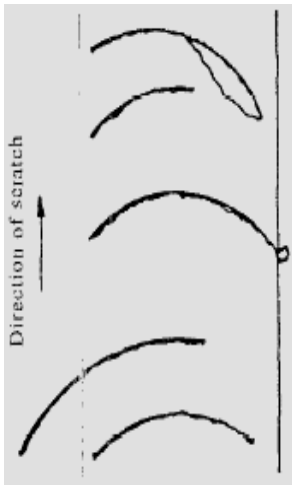
(c) Hertz cracking



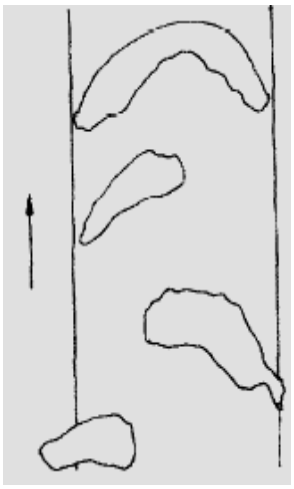
(d) Conformal cracking

Fig. 3.11 Through thickness failure modes in the scratch testing [61].

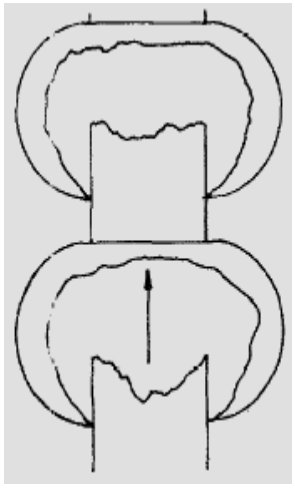
Through-thickness cracking: it includes tensile cracking behind the diamond stylus, conformal cracking and Hertzian cracking [79]. Schematic diagrams of these failure modes are shown in Fig. 3.11. The cracks formed in the coating may extend into the substrate if it is brittle and in the case of softer substrate these cracks are usually stopped at the film-substrate interface.



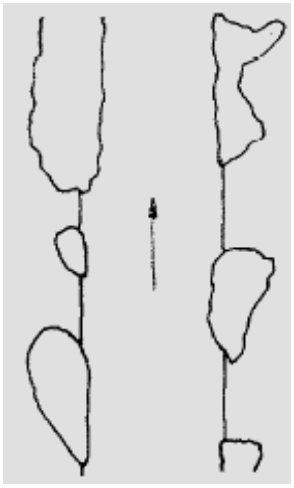
(a) Buckling



(b) Buckle spallation



(c) Wedging/Spallation



(d) Recovery spallation

Fig. 3.12 Interface failure modes in the scratch test [61].

Interfacial failure: In general, interfacial or adhesive failure is associated with buckling, buckling spallation, wedge spallation and recovery spallation modes. Schematic diagrams of these scratch failure modes are given in Fig 3.12. Buckling failure is more prominent in thin coatings (typically < 10 μm thick) as a result of compressive stresses produced by the moving stylus. Interfacial defects in the coating-substrate system allow the coating to

buckle and eventually spread laterally as the interfacial crack propagates. Spallation occurs when through thickness cracks form in the high tensile stresses within the coating. Ductile piling up of the coating material in front of the stylus can enhance the spallation failure mode. Buckling failure regions typically are seen as curved cracks, whilst in spallation buckle failure edges are perpendicular to the interface.

Wedge spallation mode is observed when the compressive shear cracks extend through the thickness of the coating before interfacial detachment happens. Cracks in this mode have sloping sides which act like a wedge. Onward motion of the scratch indenter forces wedges of adjacent coating under the segment surround by shear crack resulting in interfacial failure of the coating-substrate system.

Recovery spallation is usually related with the elastic recovery during scratch testing and mainly depends on the plastic deformation of the substrate and on the through-thickness cracking in the coating. The spreading of the interfacial shear cracks in thin film occurs because of the residual stresses produced by scratch testing which may result in spallation at both sides of the scratch track. This type of scratch failure mode is not observed in hard coating-soft substrate system due to the presence of better adhesion at the interface when compared to other systems.

3.3.3 Factors affecting the critical load (Lc)

In scratch testing, the measured critical load, Lc, depends on several factors including interfacial adhesion strength [80]. Some of the important factors are coating thickness, mechanical properties of the coating and substrate such as hardness and elastic modulus, friction between the diamond stylus and sample surface and residual stresses in

the coating. Some of these factors, which have significant effect on critical load (Lc) are summarized in Table 3.2.

Table 3.2 Factors affecting scratch adhesion critical loads [80].

Factor	**Effects**	**Expected change in *Lc***
Increasing in thickness	-Increases in internal stored energy -Decrease in average friction stress -Increase in coating indentation stored energy -Friction stored energy is almost constant	Increase
Increasing substrate hardness or decreasing substrate modulus	-Decrease in substrate plastic zone -Lowering of interfacial constraint	Increase
Increasing coating hardness or decreasing coating modulus	-Decrease in coating plastic zone -Increase in constraint stress -Increase in coating indentation stored energy	Decrease
Increasing friction coefficient	-Increase in frictional stored energy -Increase in friction stress	Decrease
Increasing internal stress	-Increase in stored energy -Increase in (internal) stress at interface	Decrease

The effect of these factors is considerable when sample fails as buckling or spalling mode (compressive failures). Laugier [81] reported a simple energy balance criterion in which stored elastic energy in front of the diamond stylus is released to form new surfaces, usually at the critical load, Lc. This energy criterion is applicable to both brittle and ductile coatings. Generally, the released energy during failure of the coating could be considered as three components: stored energy around the indentation; stored energy due

to residual stresses present in the coating; and stored energy due to frictional stresses [81]. The critical interfacial shear stress condition, in which adhesive failure happens, when the critical shear stress exceeds, can be divided into three parts: indentation constraint stress due to the presence of substrate, residual stresses present in the coating, and friction stress.

3.4 AFM (Atomic Force Microscopy) analysis:

The residual nanoindentation impressions were scanned using the AFM (Hysitron Triboscope, USA) equipment, to study the pile-up and sink-in behavior of BD films. The scan size used in the analysis was 5 × 5 μm. Such imaging gave a means to quantitatively measure the geometry of the residual indentation mark for final analysis.

CHAPTER 4: RESULTS

4.1 Thickness dependence of nanomechanical properties of BD (Black diamond ™, low-k) thin films

BD thin films of six different thicknesses, 100, 300, 500, 700, 1000 and 1200 nm were deposited on 8" silicon substrate. Nanoindentation and nanoscratch tests have been performed on these films to study the effect of thickness on the nanomechanical behaviors.

4.1.1 Nanoindentation testing

The nanoindentation tests are made with constant strain rate 0.05 s^{-1}. Fig. 4.1 shows some typical load-displacement curves of the BD thin films (100, 300, 500, 700, 1000 and 1200 nm) using nanoindentation CSM technique. The main advantage of CSM technique is that, hardness and modulus can be determined as a function of indentation penetration depth with a single nanoindentation load-unload cycle. Berkovich indenter was employed in all experiments and a series of ten indentation tests were performed on each sample. Tests showed good repeatability. The maximum nanoindentation depth for all the samples was set to at least 100 nm deep into substrate, mainly to study the transition of mechanical properties from thin film to substrate as the tip penetrated through the film-substrate interface. The Poisson's ratio of the BD films of different thicknesses in nanoindentation experiment data is taken as 0.25, because the Poisson's ratio has a negligible effect on the indentation results [83]. Almost all BD films show pop-in events as indicated by arrows in Fig.4.1 due to the failures in the films and it is

evident from the optical micrographs (Fig. 4.2) and corresponding pop-in events as marked on hardness and modulus vs. displacement graphs in Fig. 4.3. As the thickness increases, the degree of failure or the extent of damage increases in nanoindentation testing and it can be observed from the optical images shown in Fig. 4.2, where cracks are indicated by arrows on the micrographs.

From Fig. 4.3a-f large fluctuations and high values of hardness and elastic modulus are observed as the tip touches the film surface which might be due to the equipment noise and the inaccuracy of the indenter tip function at very shallow depth of indentation. As the indentation depth increases, both the hardness and elastic modulus reaches minima region as a property plateau and then tip starts sensing the effect of silicon substrate which results in higher hardness and elastic modulus. This phenomenon is observed only in the case of soft films on hard substrate. Here, the averaged hardness and elastic modulus of this minima plateau region is used to define the properties of the films as presented in Table 4.1. Fig. 4.4 compares the mechanical properties of six different thicknesses of BD samples. Hardness and elastic modulus of the BD films (100 to1200 nm) are in the range of 1.66 to 2.02 GPa and 9.27 to16.48 GPa respectively.

AFM analysis of the residual nanoindentation marks were performed and are presented in Fig 4.5. A cross-sectional analysis along the mid of the vertex of each sample was performed and corresponding line diagram is also shown in Fig. 4.5. In this analysis it is observed that pile-up is prominent in thin films (100-300 nm BD films) and sink-in is prominent in thick films (500-1200 nm BD films).

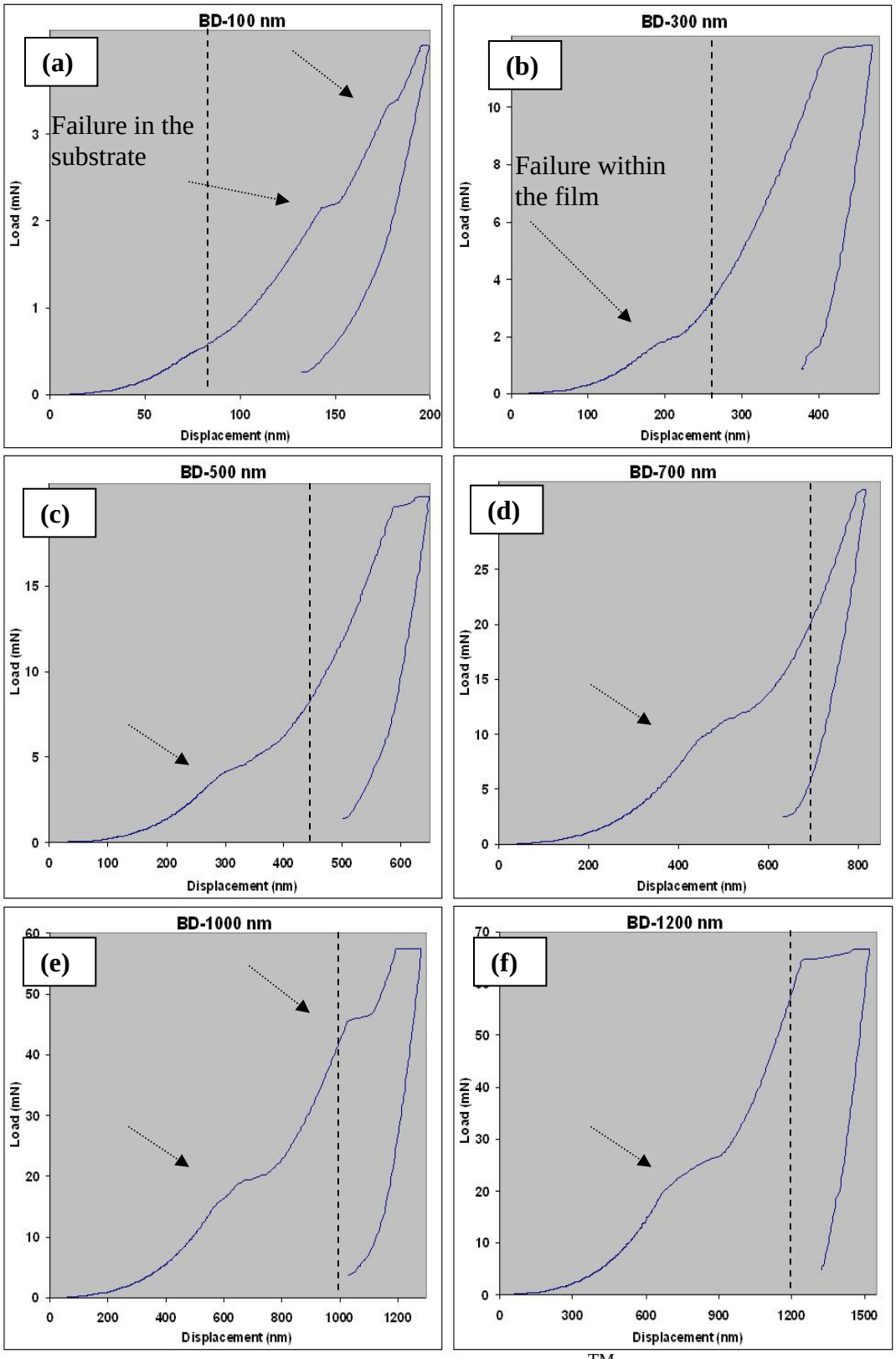
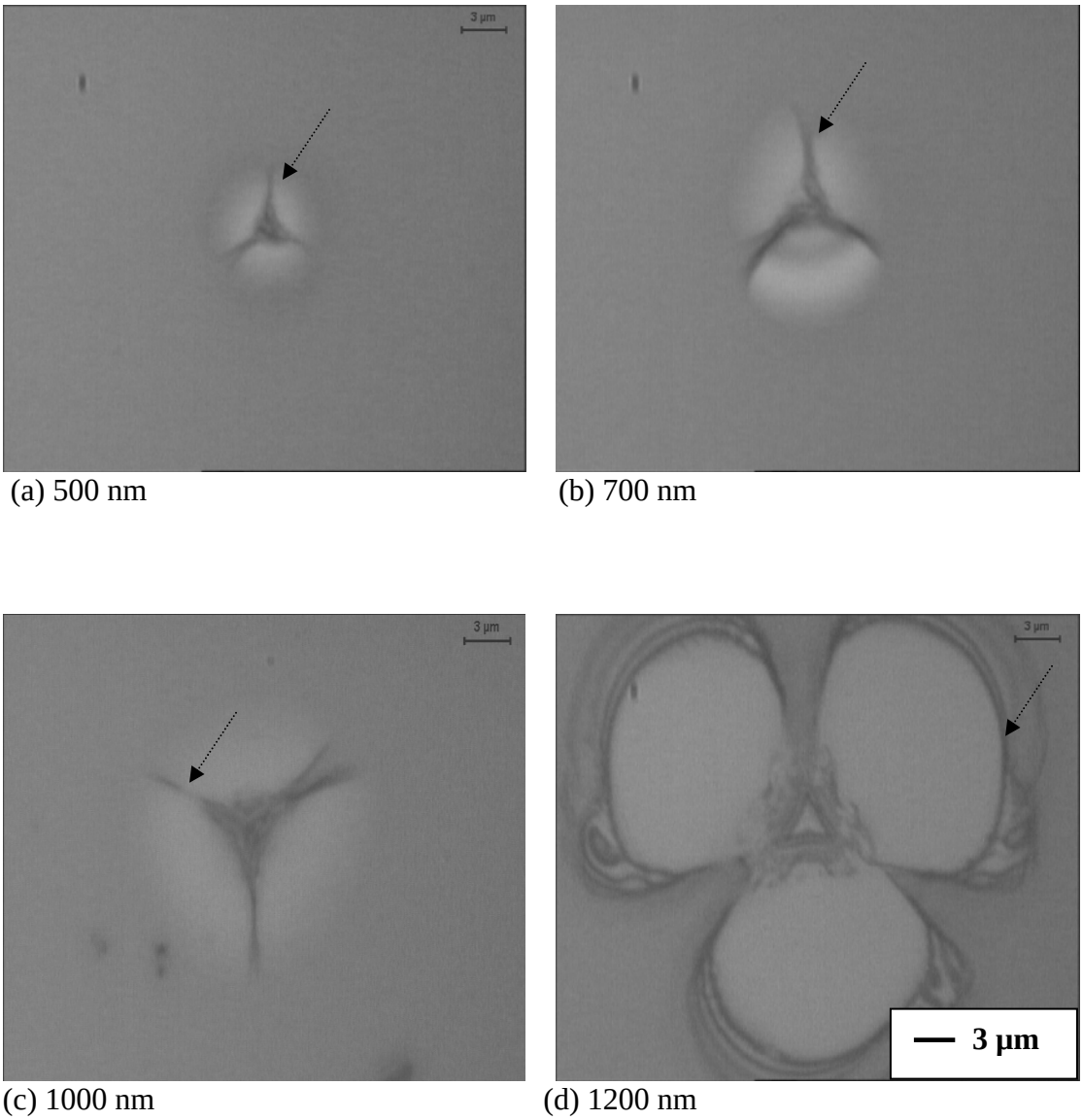


Fig. 4.1 Load-displacement curves for Black Diamond ^{TM} (BD) films of six different thicknesses under nanoindentation, (a) 100, (b) 300, (c) 500, (d) 700, (e) 1000 and (f) 1200 nm. Arrows on the curves indicate the pop-in events.



(a) 500 nm (b) 700 nm

(c) 1000 nm (d) 1200 nm

Fig. 4.2 Optical images of residual nanoindentation impressions of (a) 500, (b) 700, (c) 1000 and 1200 nm BD thin films. Radial cracks in the films observed for all thicknesses as shown by arrows.

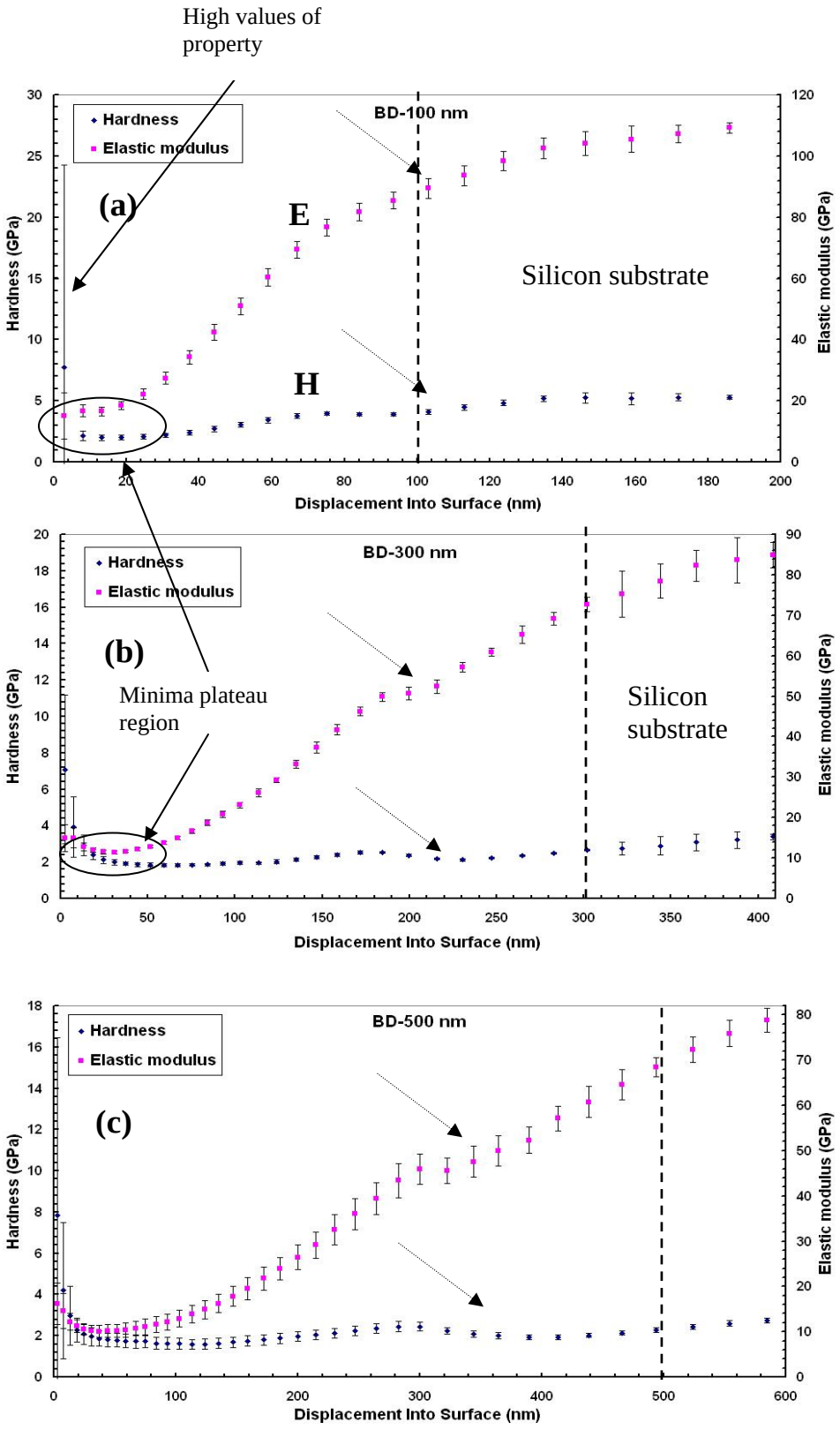


Fig. 4.3 Hardness and elastic modulus as a function of displacement for (a) 100, (b) 300 (c) 500 nm; see next page (d) 700 nm (e) 1000 and (f) 1200 nm BD thin films.

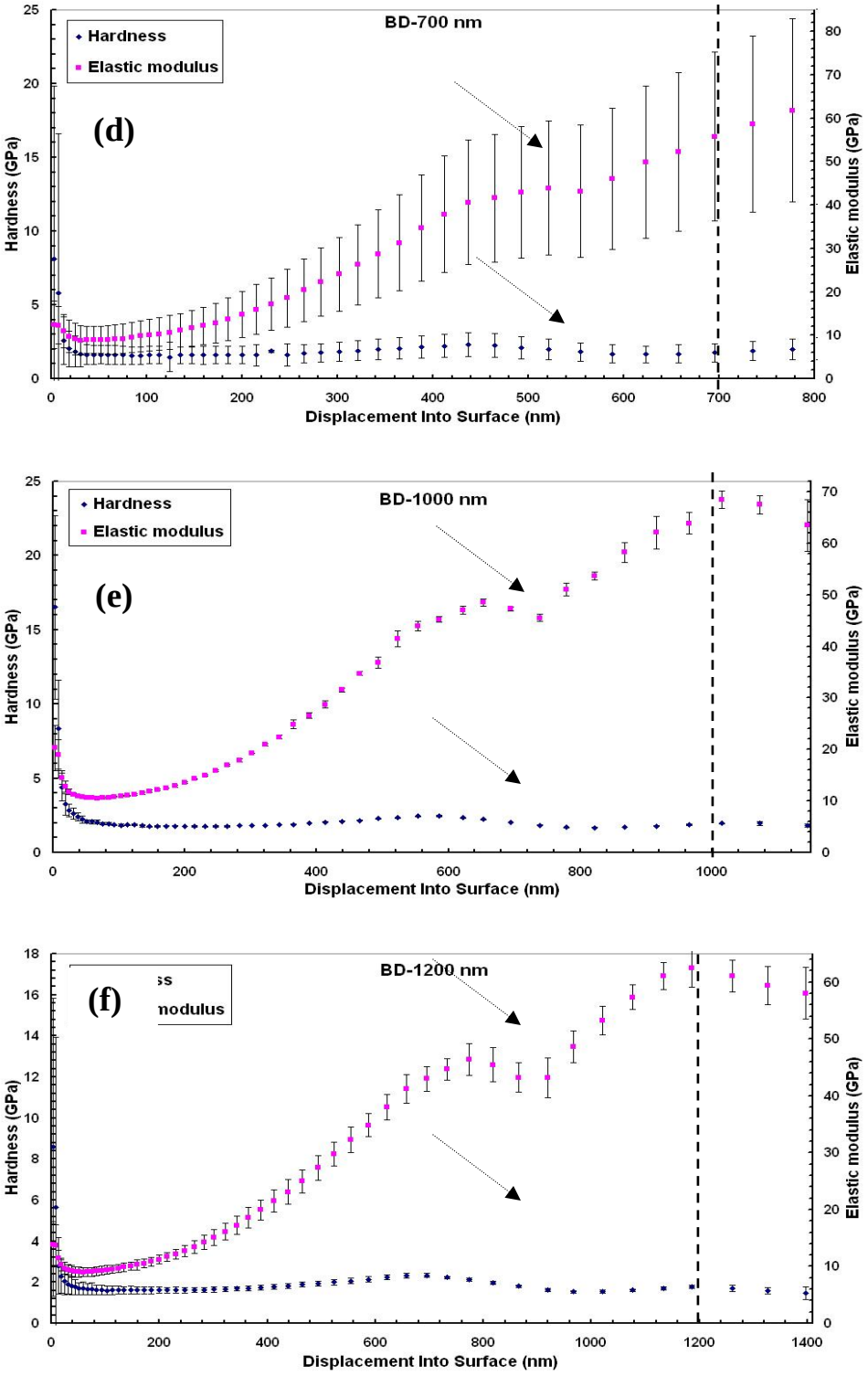


Fig. 4.3 Contd. (d) 700 nm (e) 1000 and (f) 1200 nm BD thin films. Excursions (pop-in event) in the property profile are shown by arrows.

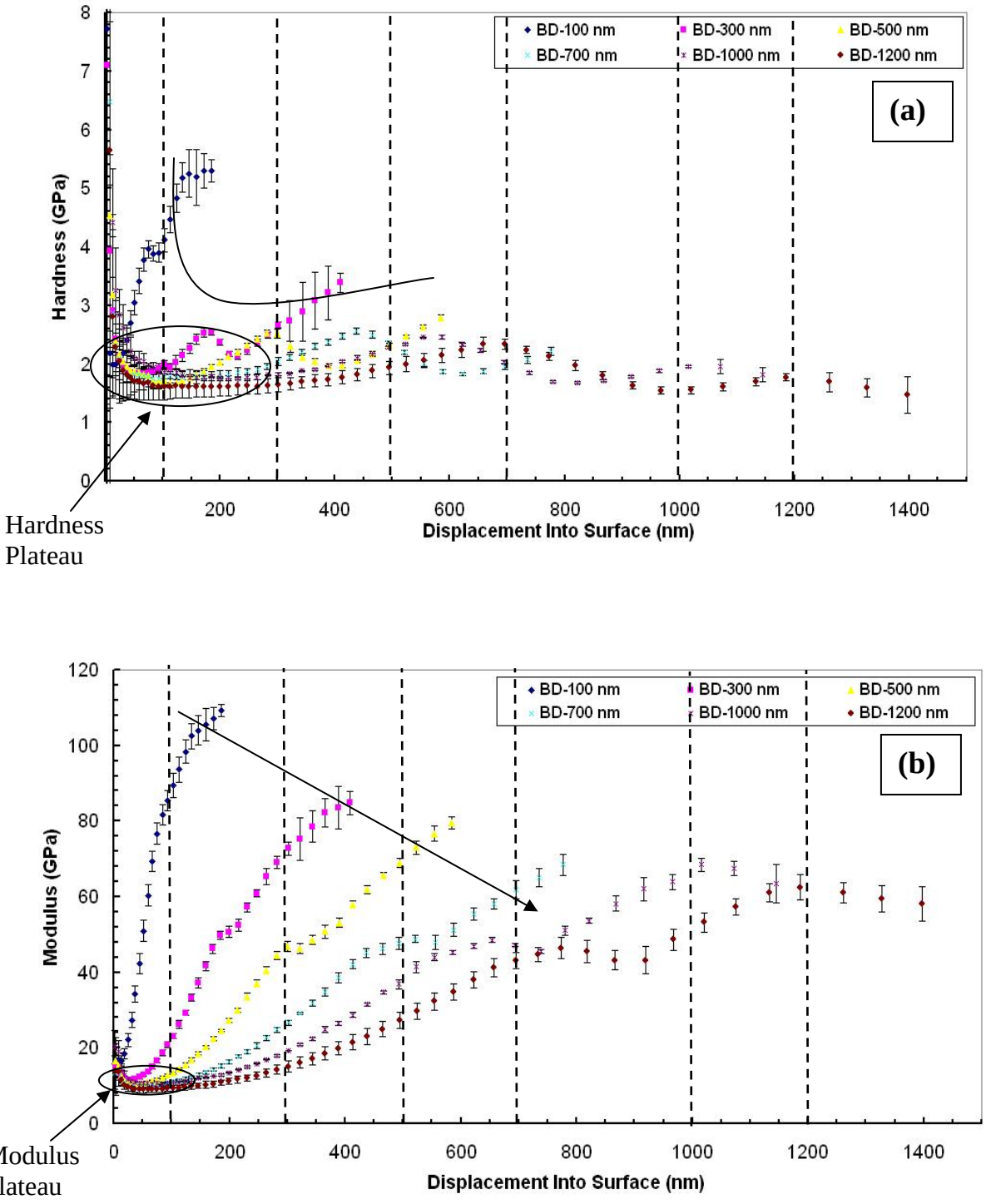


Fig. 4.4 (a) Hardness and (b) elastic modulus as functions of the displacement for BD films with six different thicknesses.

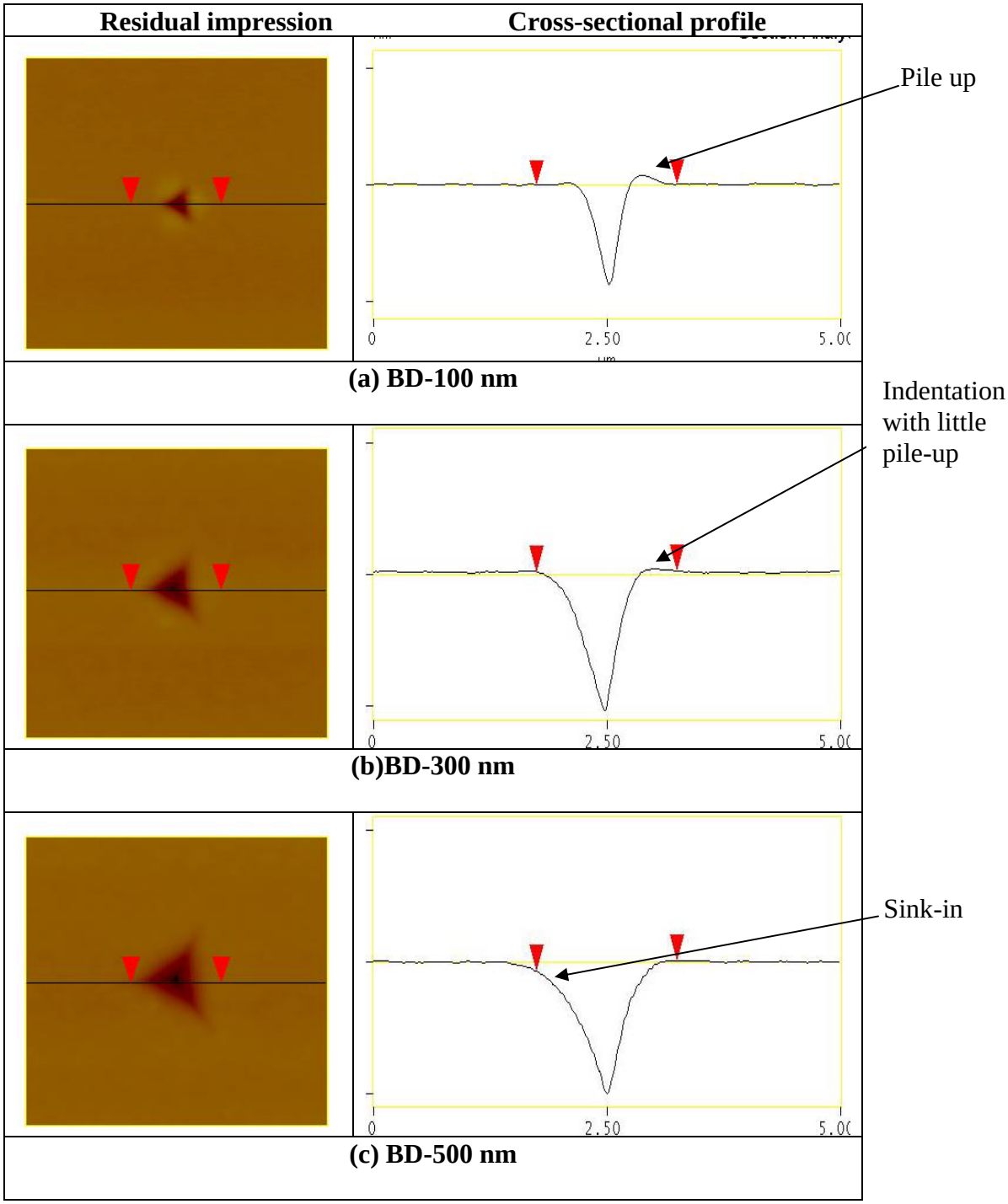


Fig. 4. 5 AFM images of residual nanoindentation impressions and section analysis profiles of (a) 100, (b) 300 and (c) 500 nm BD films.

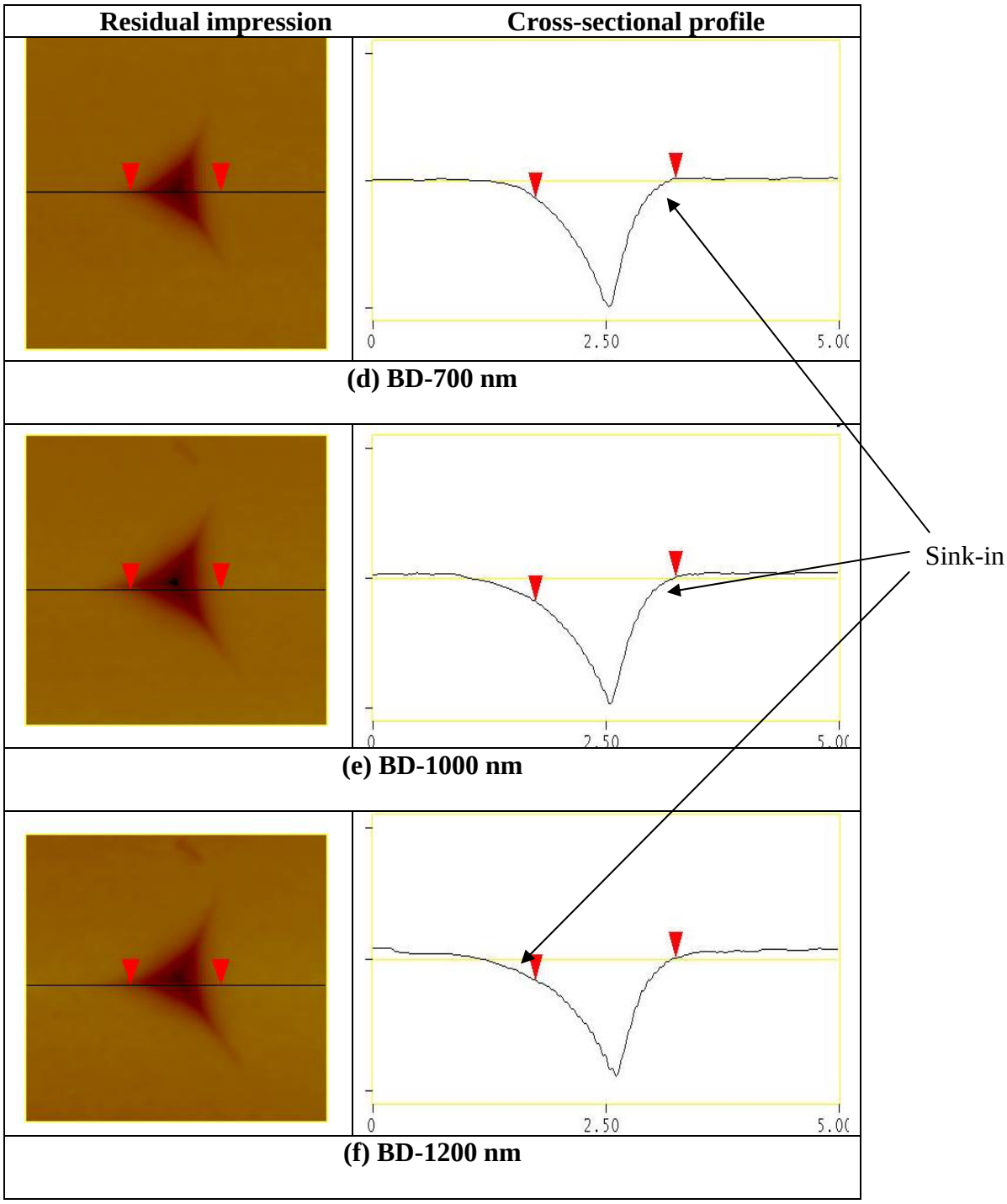


Fig. 4.5 Contd. AFM images of residual nanoindentation impressions and section analysis profiles of (d) 700, (e) 1000 and (f) 1200 nm BD films.

4.1.2 Nanoscratch testing

The adhesion/cohesion strength of BD films was measured using nanoscratch technique by the application of ramp loading. All nanoscratch experiments were performed on Nano Indenter® XP system with nanoscratch attachment. All nanoscratch tests were performed at a speed of 1μm/s. In nanoscratch testing, a ramp load is applied for all BD thin films over a length of 400 μm until the load reaches a pre-set normal load of 50 mN. A conical diamond tip of radius of curvature ~ 5 μm was used to scratch the BD films. The diamond tip shape was verified before and after scratch testing to check whether or not the blunting of the sharp end of the tip had occurred. The scratch profiles of all samples are shown in Fig.4.6 as scratch depth vs. normal load. For all nanoscratch experiments a conical diamond tip was opted as indenter because it is symmetrical in all directions along its axis, which eliminates any possible directionality effect [84]. To avoid the effect of deformation from adjacent scratches, the distance between sequential scratches was set to 200 μm. Each representative value of nanoscratch test is an average of five individual tests performed in different parts of BD sample. All tests showed good repeatability. The scratch track morphologies of each BD sample was observed with an optical microscope as shown in Fig. 4.7. The critical load for BD-100 nm film couldn't be located from the scratch profile, probably due to the limited resolution of the equipment. For other BD films (300-1200) the critical loads are in the range of 13.02 to 25.86 mN.

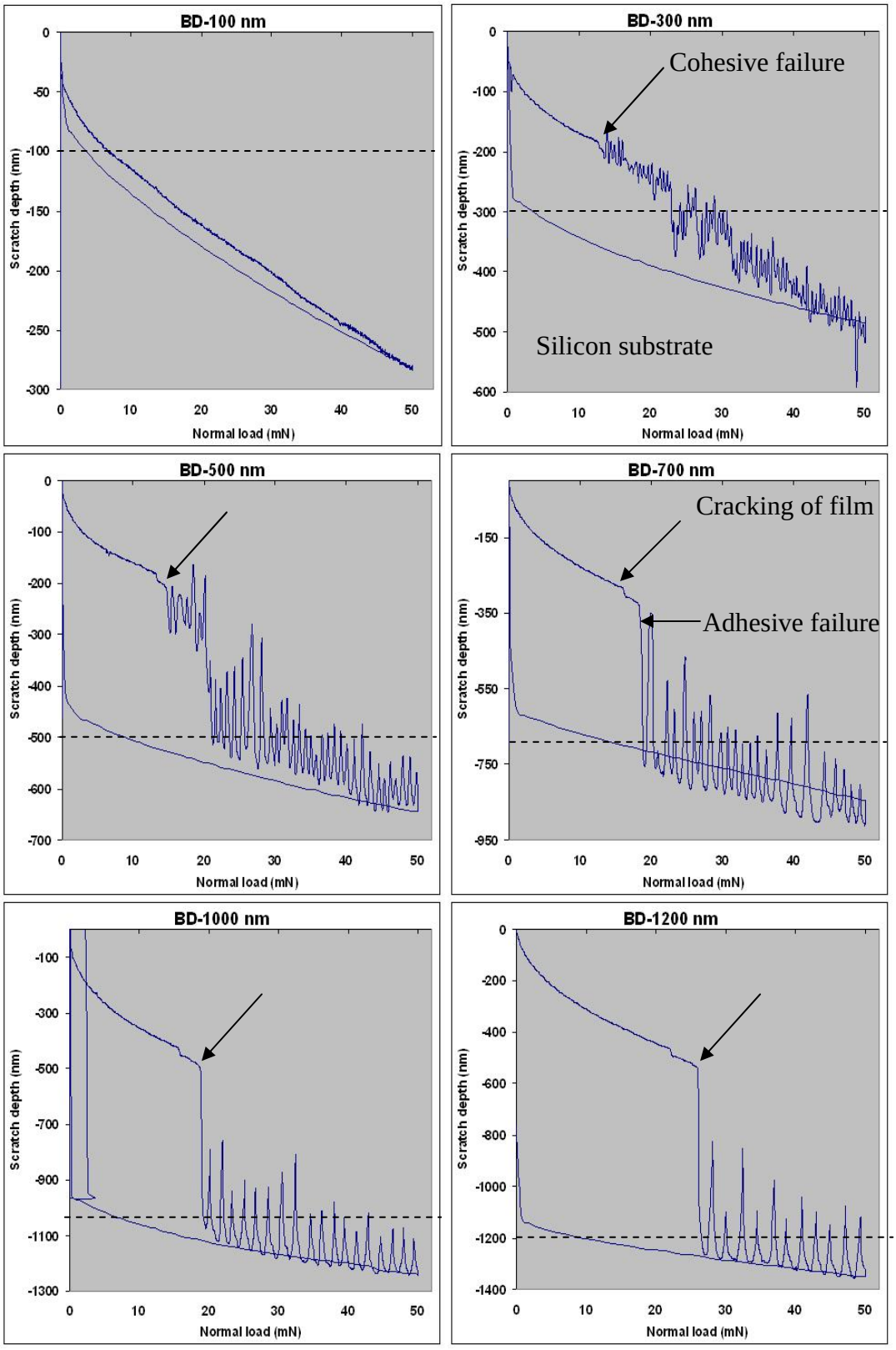
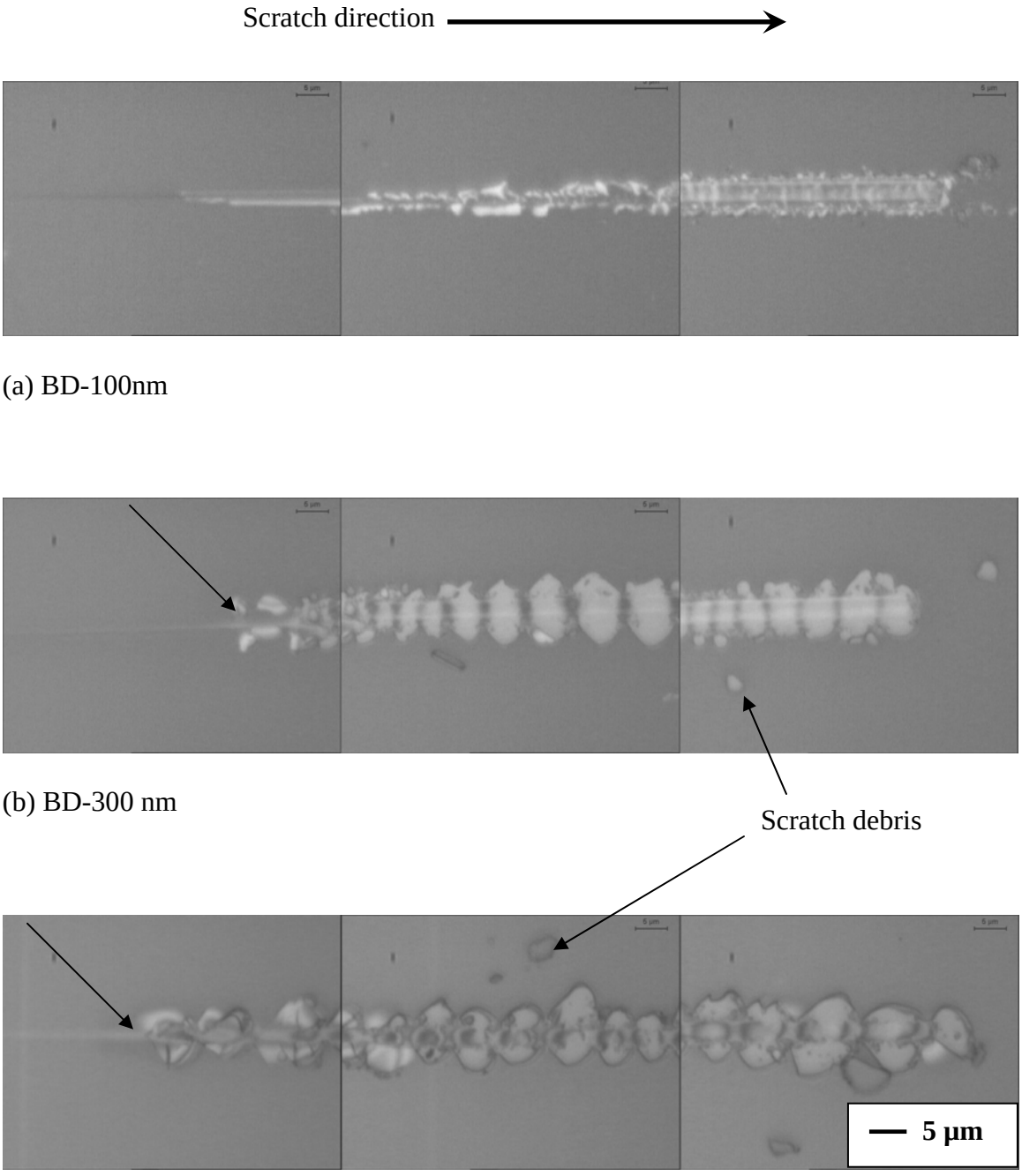


Fig. 4.6 Nanoscratch depth profiles as a function of normal load for all BD films tested with ramp loading of 50 mN. Arrows indicate critical load (Lc).



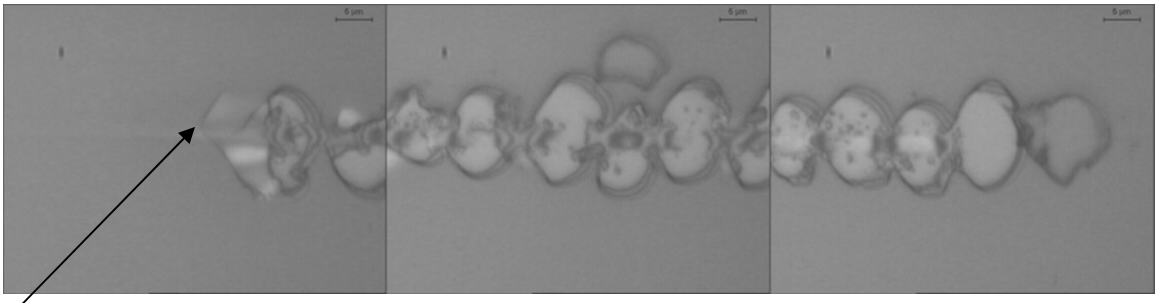
(a) BD-100nm

(b) BD-300 nm

(c) BD-500 nm

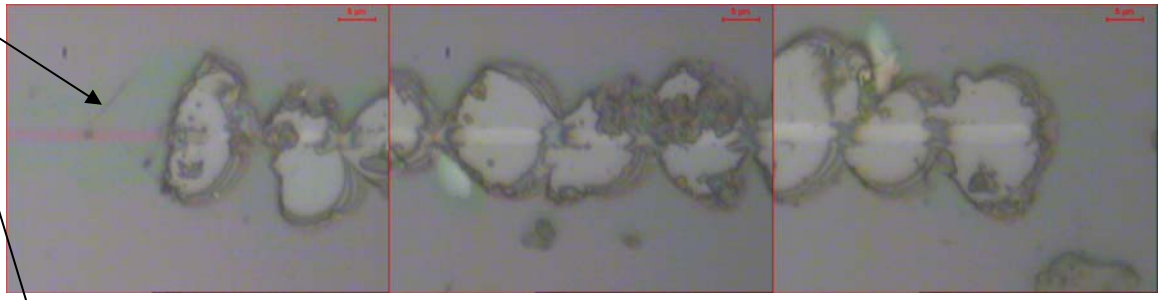
Fig. 4. 7 Optical micrographs of scratch tracks made on BD films of six different thicknesses.

Scratch direction →



(d) BD-700 nm

Initiation of cracks in film before delamination



(e) BD-1000 nm

(f) BD-1200 nm

Fig.4.7 Contd.

Table. 4.1 Summary of mechanical properties of BD films of six different thicknesses.

BD film thickness (nm)	Hardness (GPa)	Modulus (GPa)	Critical load, Lc mN	Scratch failure
100	**2.02**	**16.48**	----	Cohesive-continuous
300	1.85	11.54	13.02	Cohesive
500	1.70	10.58	13.15	Cohesive & little adhesive
700	1.78	9.93	18.52	Adhesive
1000	1.73	10.417	18.98	Adhesive
1200	1.66	9.27	25.86	Adhesive

4.2 BD films with Ta and TaN barrier layers

Single and dual dielectric stacks of BD films with Ta and TaN barriers were deposited on 8” silicon wafer. Mechanical properties were assessed by nanoindentation and nanoscratch techniques. The schematic drawing of each film stack is shown in Fig. 4.8. For single dielectric stack, the silicon substrate is first coated with Ta or TaN barrier layer of 25 nm thickness by using self-ionized metal plasma (SIP) technique at room temperature followed by the deposition of BD film of 1000 nm thickness by PECVD (plasma Enhanced Chemical Vapor Deposition) technique. For the deposition of dual dielectric stack this procedure was repeated one more time with BD films and barrier deposition.

4.2.1 Nanoindentation Testing

Fig. 9 shows the typical nanoindentation load-displacement curves of single and dual dielectric stacks with Ta and TaN barriers. From Fig. 10 optical micrographs of residual nanoindentation impressions of single and double dielectric stacks reveal that massive failure of the films is more prominent in dual dielectric stacks. Fig. 11 & 12

compare the mechanical properties of single and double dielectric stacks and it is observed that single dielectric stacks show higher mechanical properties when compared to double dielectric stacks. Hardness and elastic modulus of single dielectric stacks are in the range of 1.43 to 1.91 GPa and 8.35 to 10.03 GPa respectively. No significant difference is observed in the case of double dielectric stacks. Mechanical properties of both single and dual stacks are given in Table 5.2.

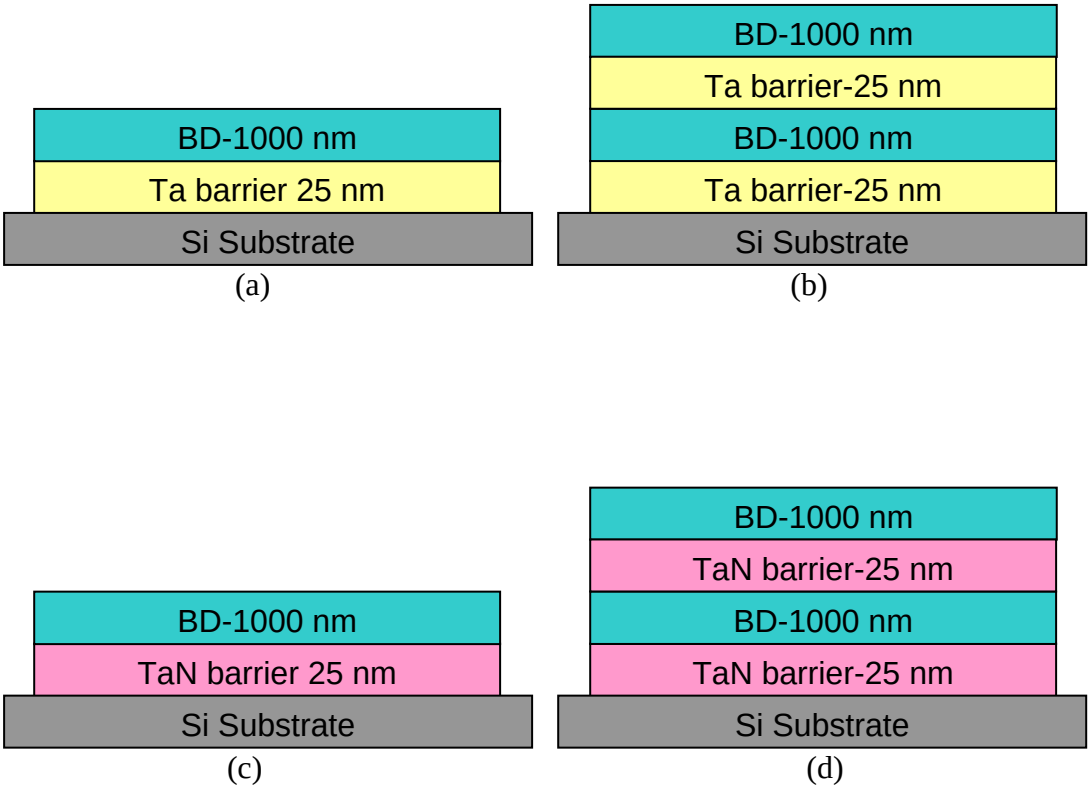


Fig. 4.8 schematic diagrams of (a) BD/Ta/Si (single dielectric stack), (b) BD/Ta/BD/Ta/Si (dual dielectric stack), (c) BD/TaN/Si (single dielectric stack) and (d) BD/TaN/BD/TaN/Si (dual dielectric stack)

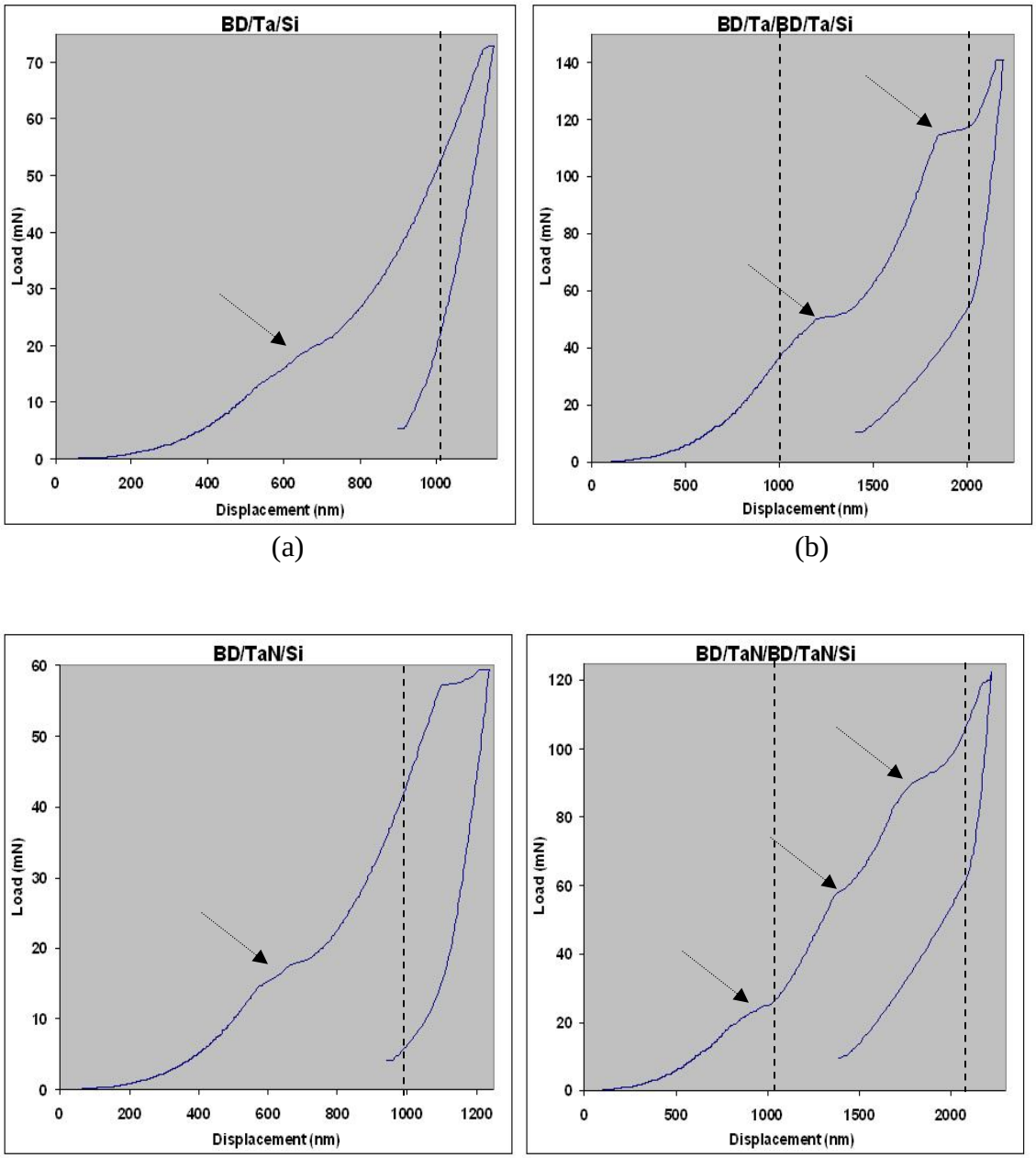
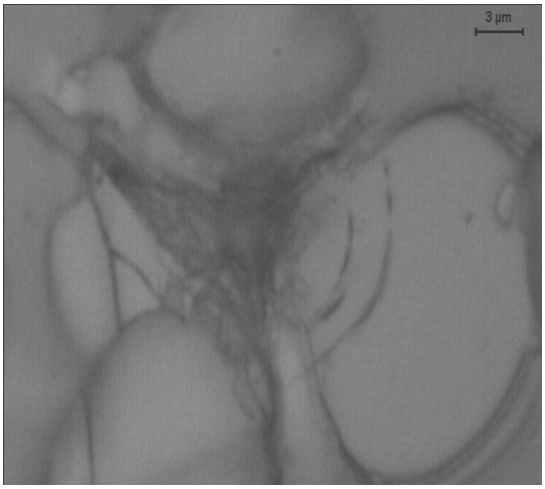


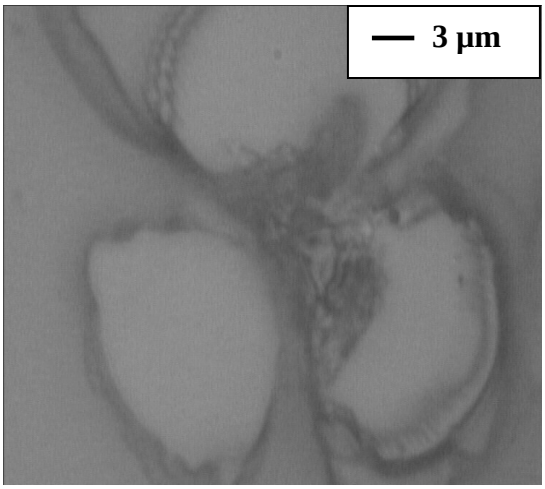
Fig. 4.9 Typical load-displacement curves of (a) BD/Ta/Si (b) BD/Ta/BD/Ta/Si, (c) BD/TaN/Si and (d) BD/TaN/BD/TaNs/Si stacks. Arrows indicate the pop-in events.

(a) BD/Ta/Si (Single dielectric stack)



(b)BD/Ta/BD/Ta/Si (double dielectric stack)

(c) BD/TaN/Si (Single dielectric stack)



(d)BD/TaN/BD/TaN/Si(double dielectric stack)

Fig. 4.10 Optical micrographs of residual nanoindentation impression on single and double dielectric stacks.

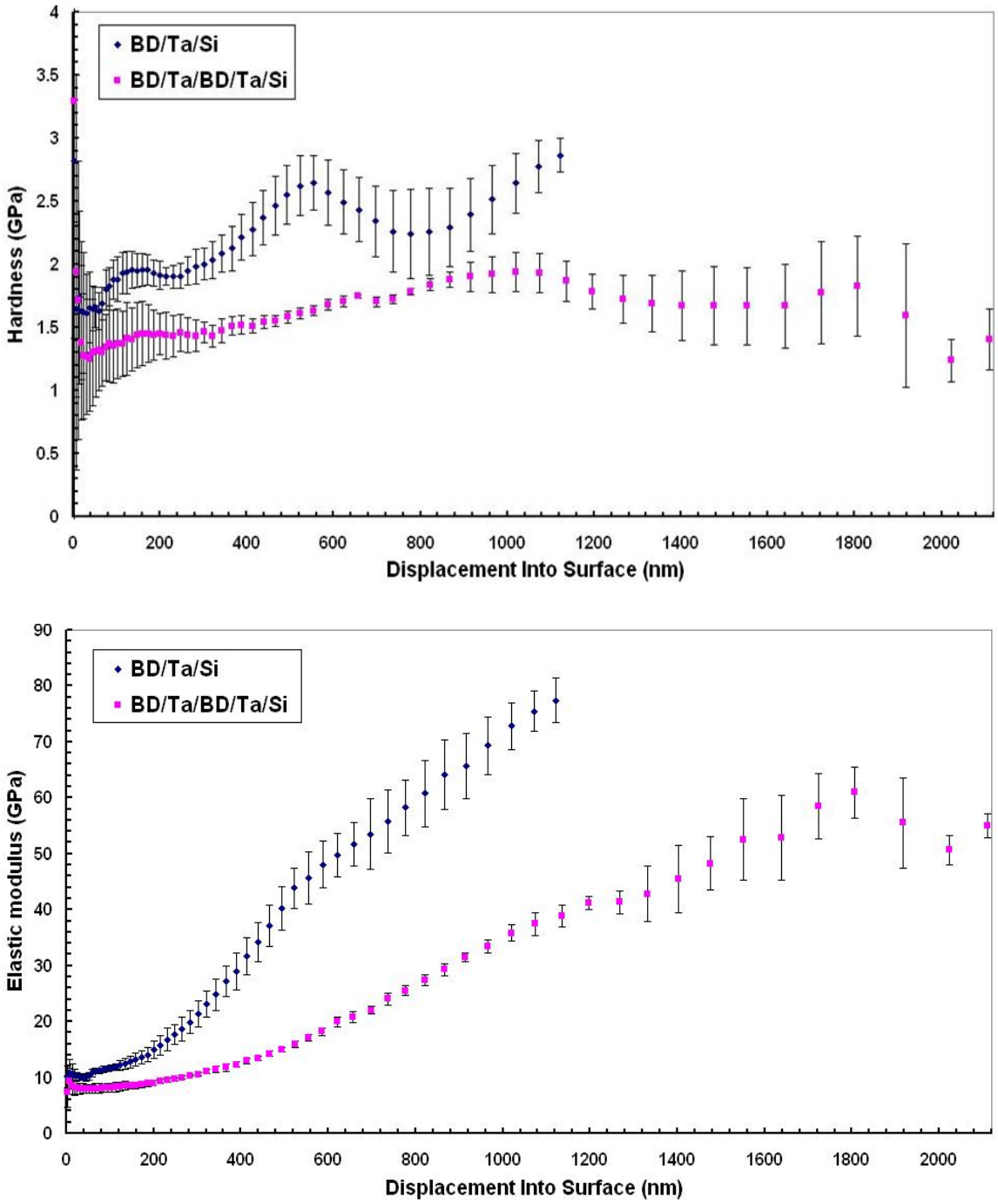


Fig. 4.11 Hardness and elastic modulus as a function of displacement for BD/Ta/Si and BD/Ta/BD/Ta/Si stacks measured using the nanoindentation CSM technique.

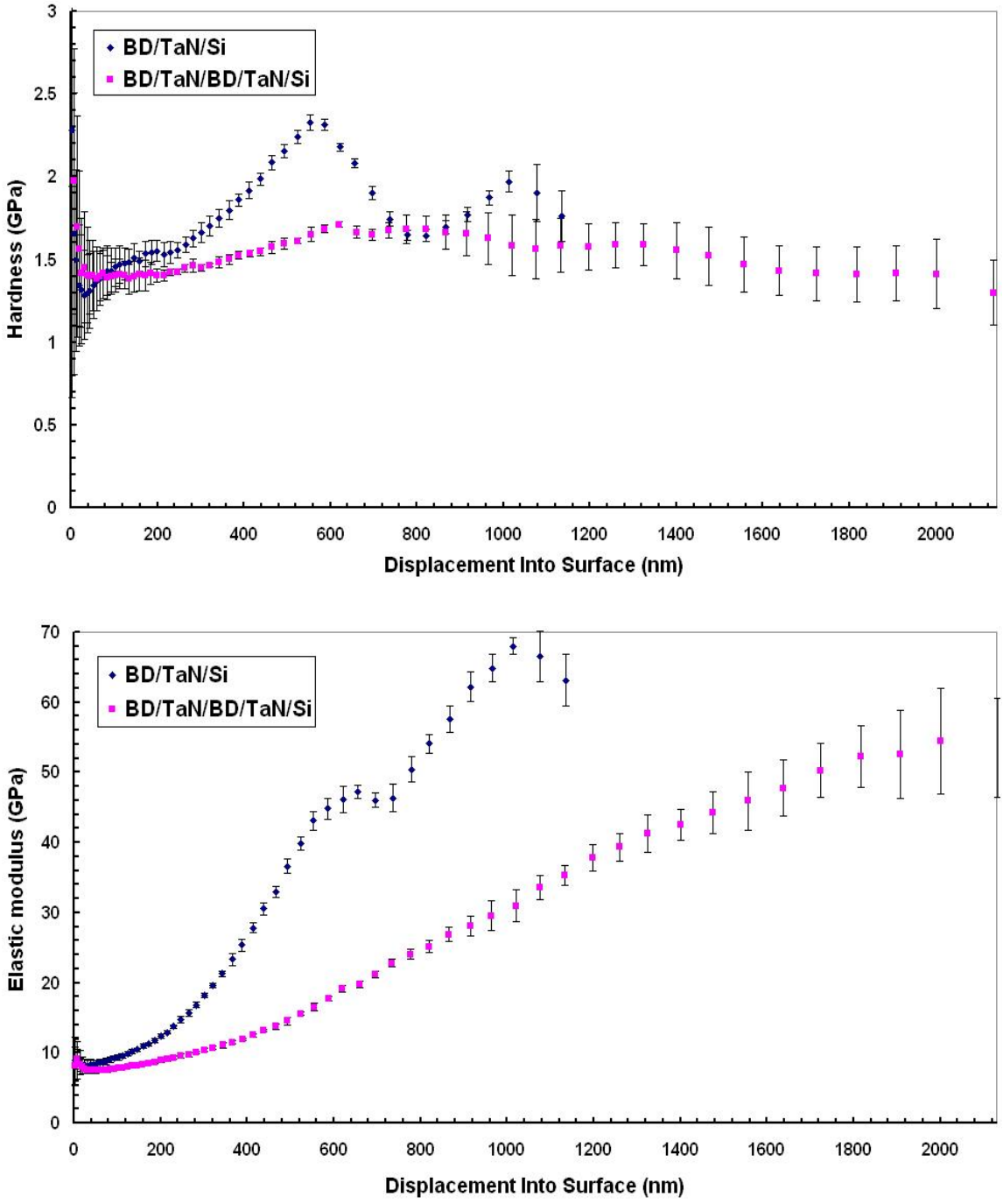


Fig. 4.12 Hardness and elastic modulus as a function of displacement for BD/TaN/Si and BD/TaN/BD/TaN/Si stacks measured using the nanoindentation CSM technique.

4.2.2 Nanoscratch testing

To determine the adhesion/cohesion strength between BD film and barrier layers, scratch test is carried out on both single and dual dielectric stacks. At least five tests were performed and an average of these five tests is reported in the present study. The scratch testing parameters are same for both single and double dielectric stacks, as follows;

Scratch length: 480 μm

Scratch velocity: 1 μm/s

Maximum scratch ramp load: 60 mN

Distance between individual scratches: 200 μm

These scratch test data show good repeatability. Fig. 4.13 shows the scratch profiles of the single and double dielectric stacks. Complete delamination is observed in both single and dual stacks as observed from the scratch profiles. The critical loads observed for single dielectric stacks are approximately 36 mN and for dual stacks in the range of 48.79 to 53.46 mN. Layer by layer delamination is noticed in the case of dual stacks which are reported as Lc1 and Lc2 in Table 5.2. Scratch tracks of single and double dielectric stacks are observed with optical microscope as presented in Fig. 4.14.

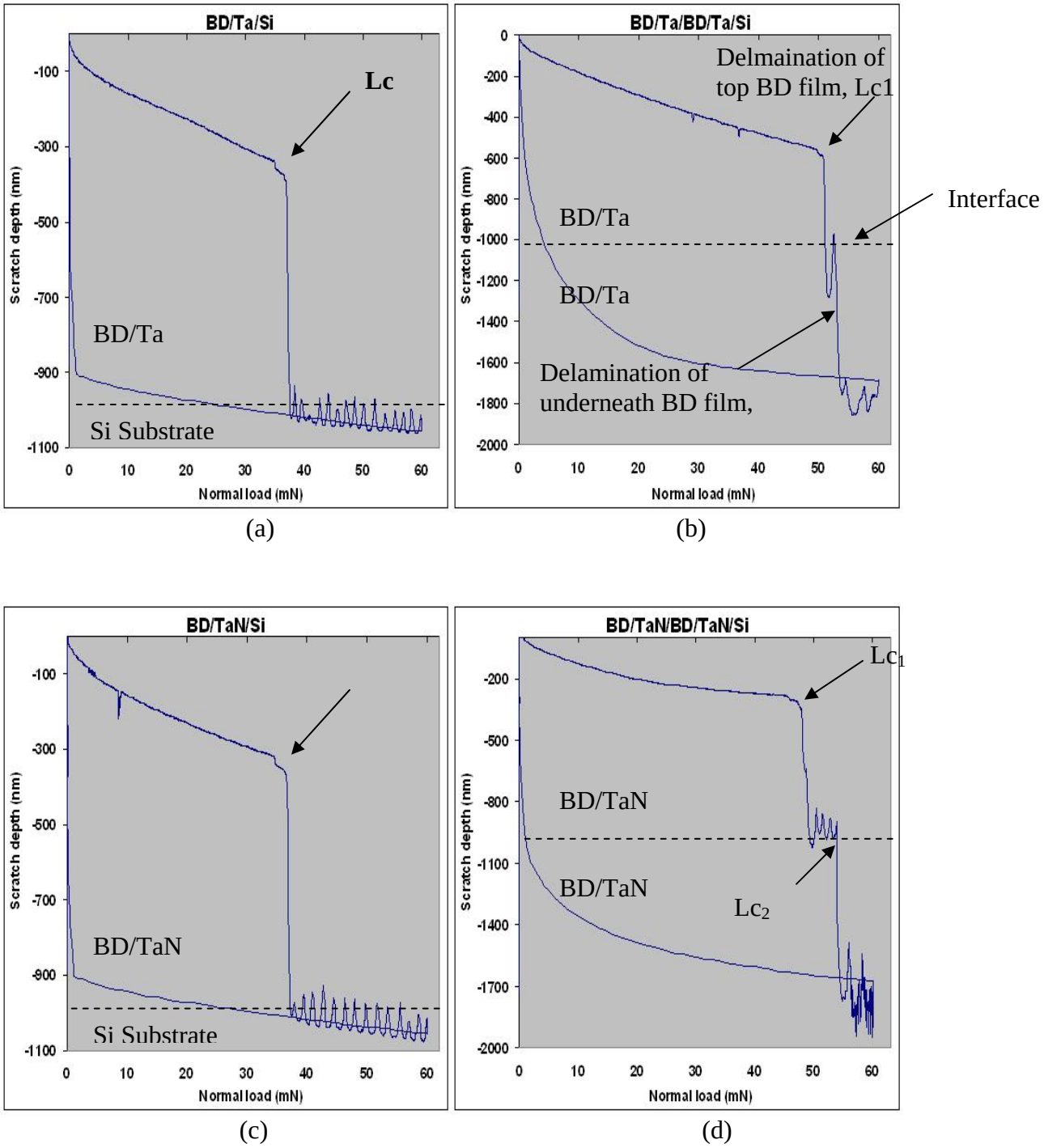
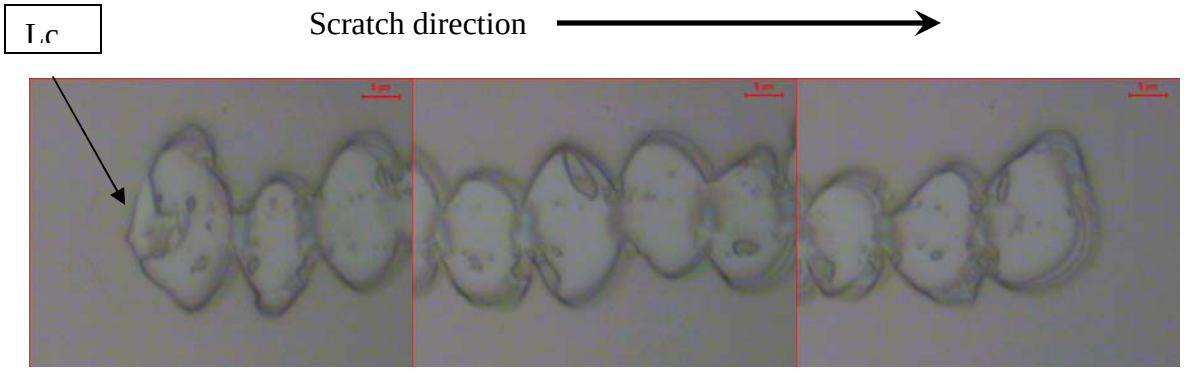
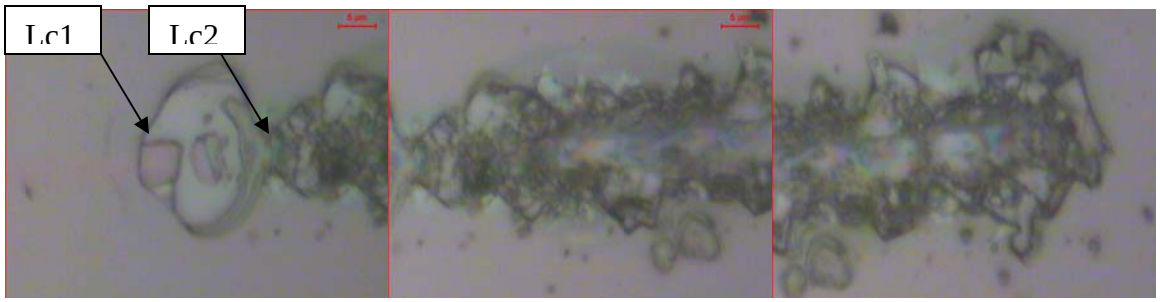


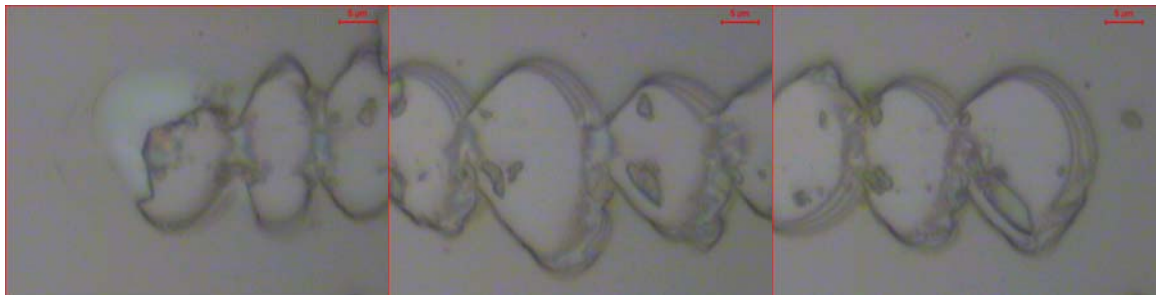
Fig. 4.13 scratch depth vs. normal load profiles for single and double dielectric stacks; (a)BD/Ta/Si, (b) BD/Ta/BD/Ta/Si, (c) BD/TaN/Si and BD/TaN/BD/TaN/Si , Arrows indicate the critical load (Lc).



(a) BD/Ta/Si (single dielectric stack)



(b) BD/Ta/BD/Ta/Si (dual dielectric stack)



(c) BD/TaN/Si-1000x (single dielectric stack)

(d) BD/TaN/BD/TaN/Si (dual dielectric stack)

Fig. 4.14 Optical micrographs of scratch tracks on single and double dielectric stacks.

4.3 Mechanical properties of Cu/BD stacks with Ta and TaN barrier layers and SiC and SiN cap layers

This set comprises eight samples of different multilayered stacks with Ta and TaN as barrier layers and SiC and SiN as cap layers. Schematic diagrams of each stack is shown in Fig.4.15. Since BEOL structures contains different composite stacks and subjected to chemical mechanical polishing (CMP), mechanical characterization results of these stacks are very essential in assessing their abilities to withstand the pressures applied during CMP processes. For ease in the explanation of nanomechanical behavior all samples are labeled from A to H as shown in Fig. 4.15 and Table 5.3.

4.3.1 Nanoindentation testing

Fig.4.16 and 4.17 shows the load-displacement curves of all samples, from A to H. The hardness and elastic modulus can be calculated from these curves. Samples A to D show pop-in events as shown in Fig. 4.16 and continuous load-displacement curves are observed for samples E-H. Fig. 4.18 to 4.21 shows the hardness and elastic modulus as a function of displacement for all the samples (A-H) measured using the nanoindentation CSM technique. Hardness and elastic modulus values presented are an average of ten individual nanoindentation experiments performed on different parts of each sample. For samples A to D the properties at 30 nm indentation depth is reported as properties of the samples, because the minima plateau region is almost at the interface. In the case of samples E to H averaged properties of minima plateau region is used to define the properties (hardness and elastic modulus) of the films as the minima plateau region is in the top copper film; properties of all samples are given in Table 5.3.

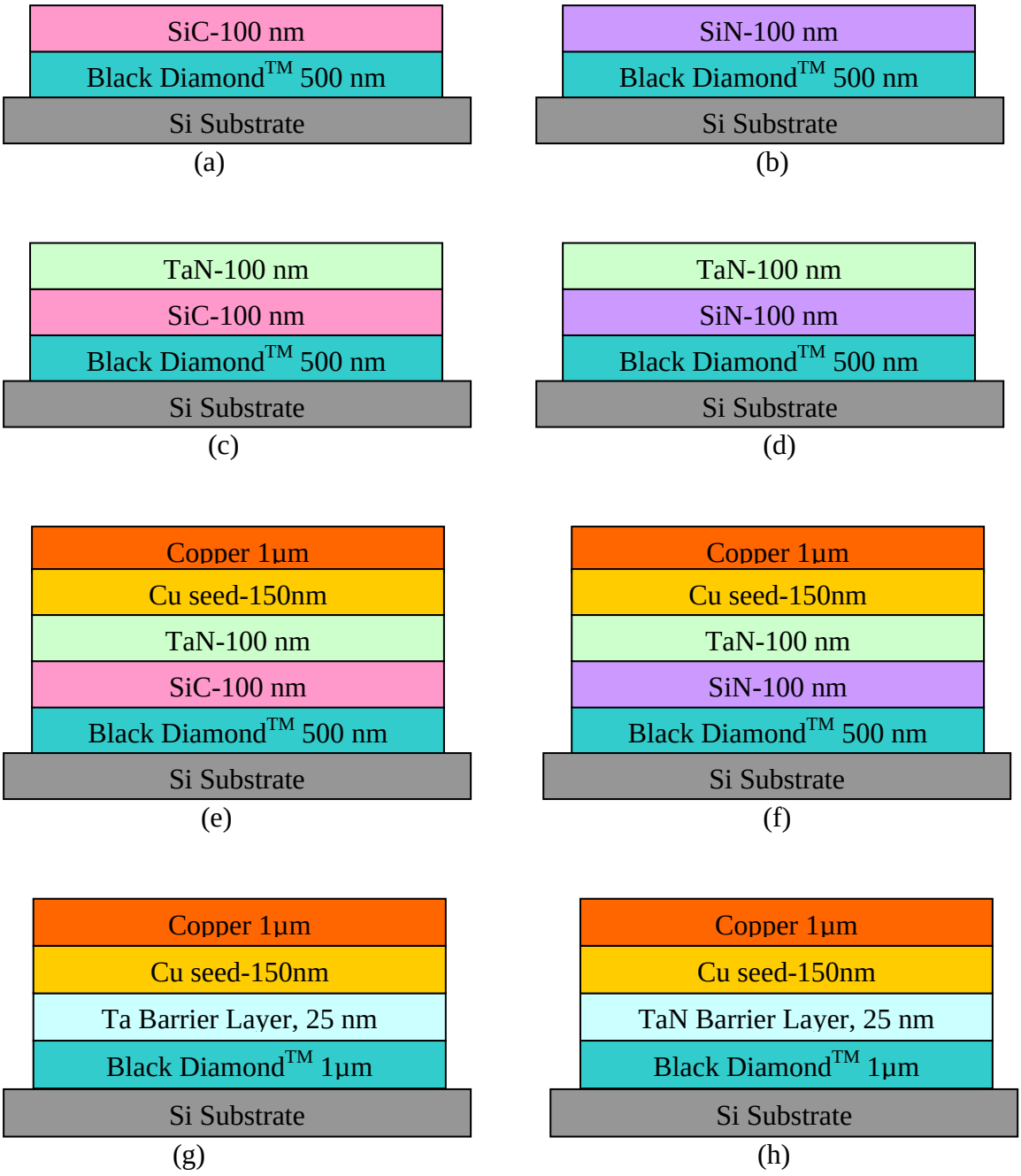


Fig. 4.15 Schematic diagrams of (a) SiC/BD/Si-A , (b) SiN/BD/Si-B, (c) TaN/SiC/BD/Si-C, (d) TaN/SiN/BD/Si-D, (e) Cu/TaN/SiC/BD/Si-E, (f) Cu/TaN/SiN/BD/Si-F, (g) Cu/Ta/BD/Si-G and (h) Cu/TaN/BD/Si-H multilayered stacks.

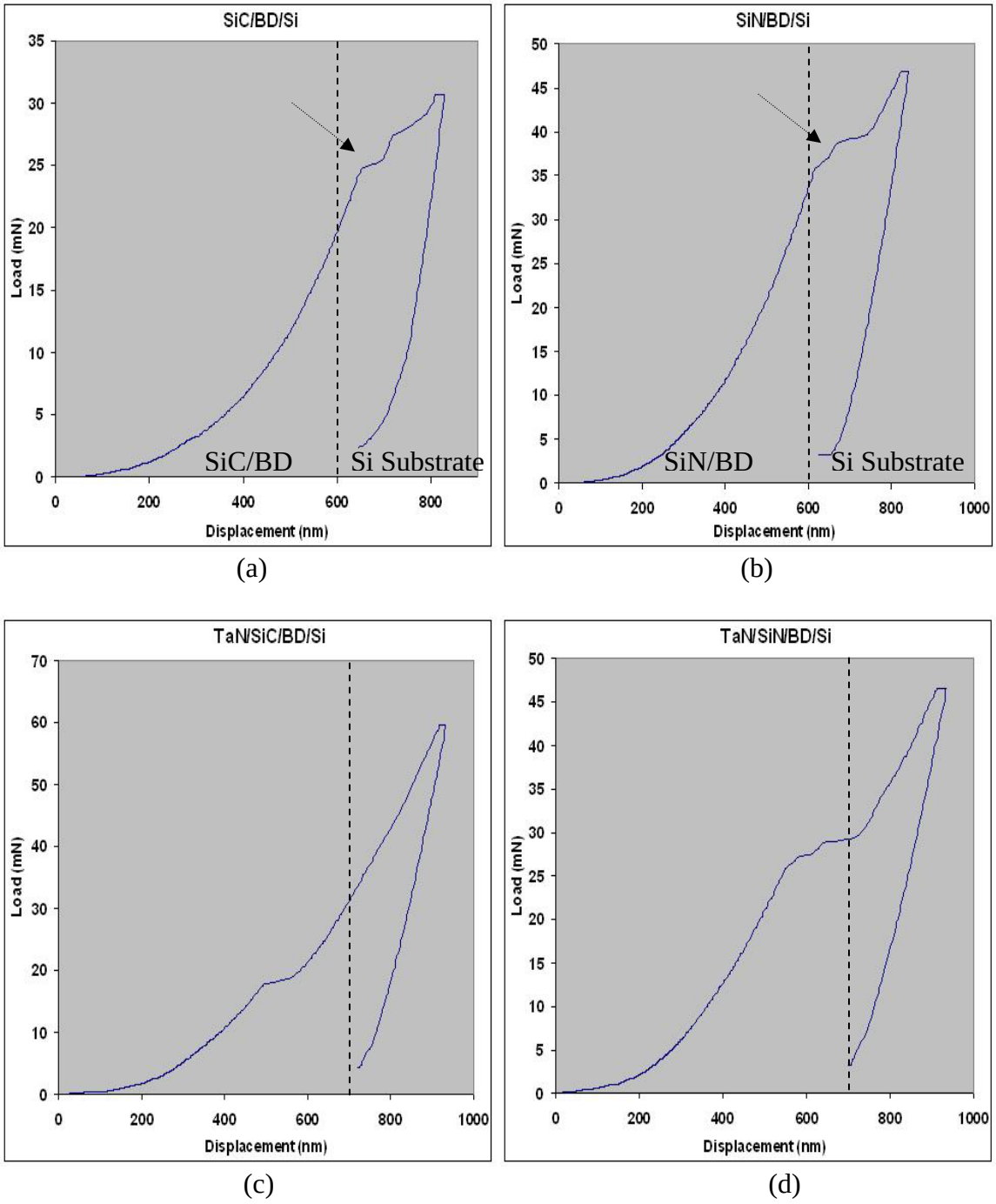


Fig. 4.16 Nanoindentation load-displacement curves of BD films with Ta and TaN barriers and SiC and SiN cap layers. Arrows indicate pop-in events.

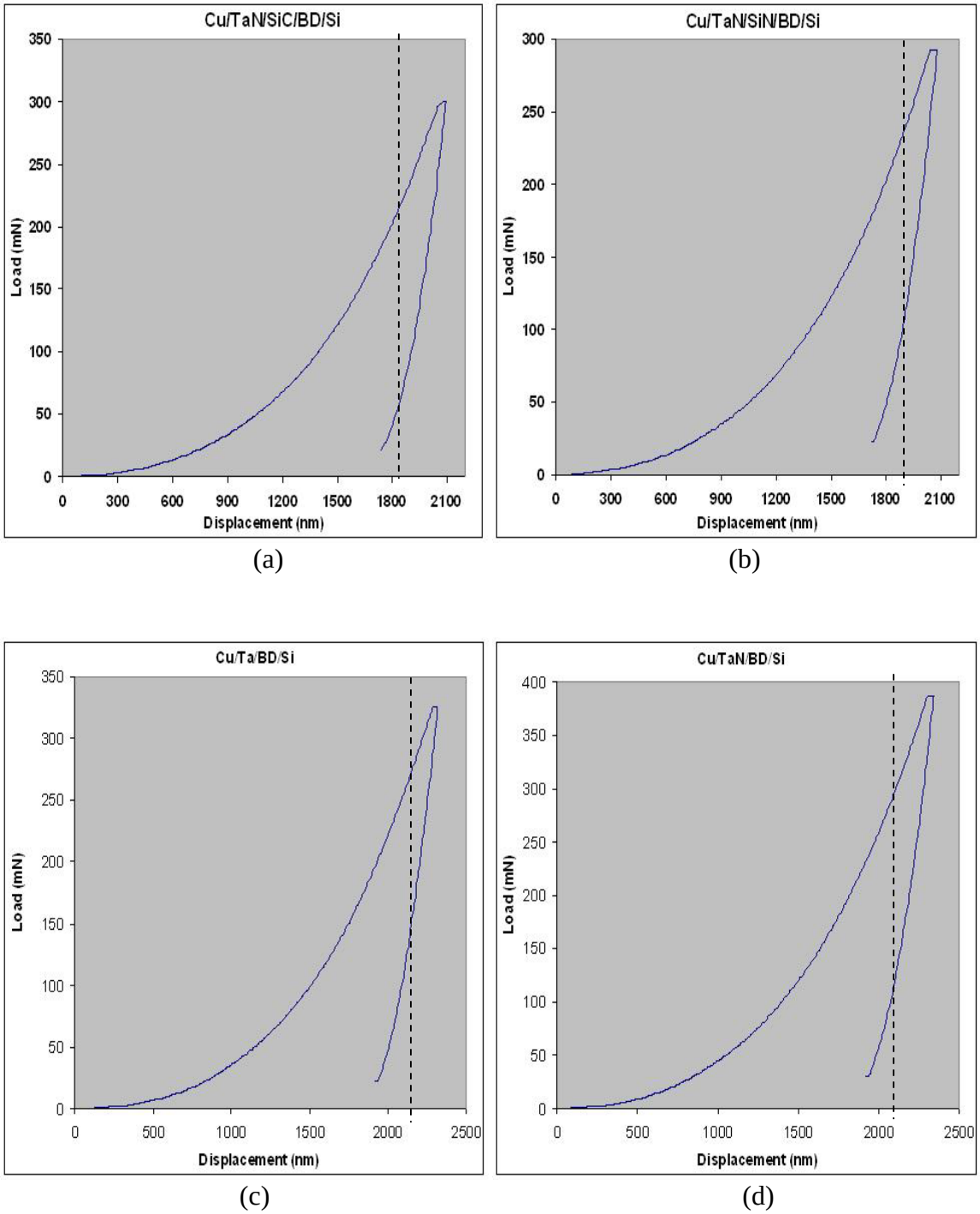


Fig. 4.17 Nanoindentation load-displacement curves of Cu/BD (low-k) stacks with Ta and TaN barrier layers and SiC and SiN cap layers.

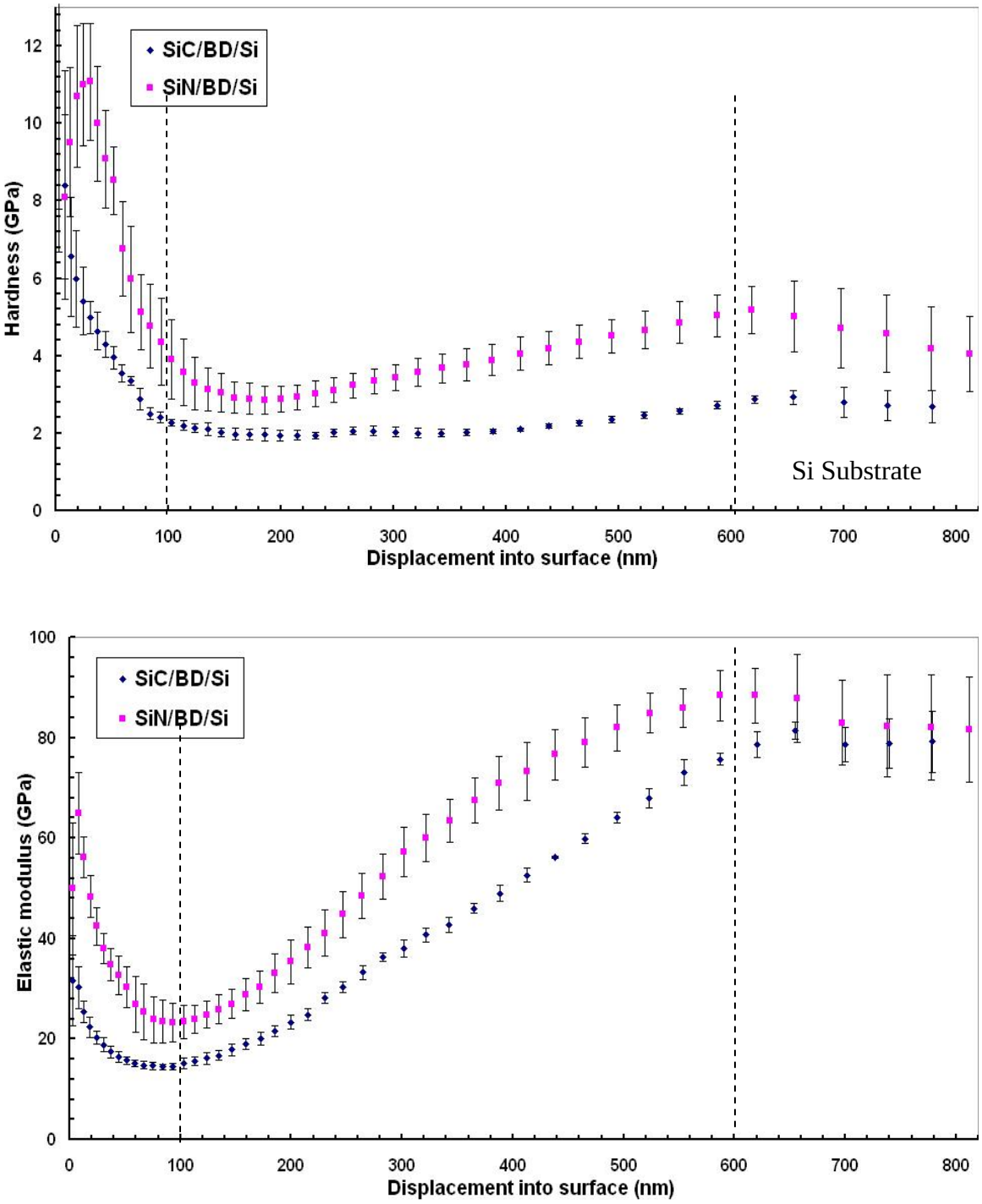


Fig. 4.18 Comparison of mechanical properties of SiC/BD/Si and SiN/BD/Si stacks.

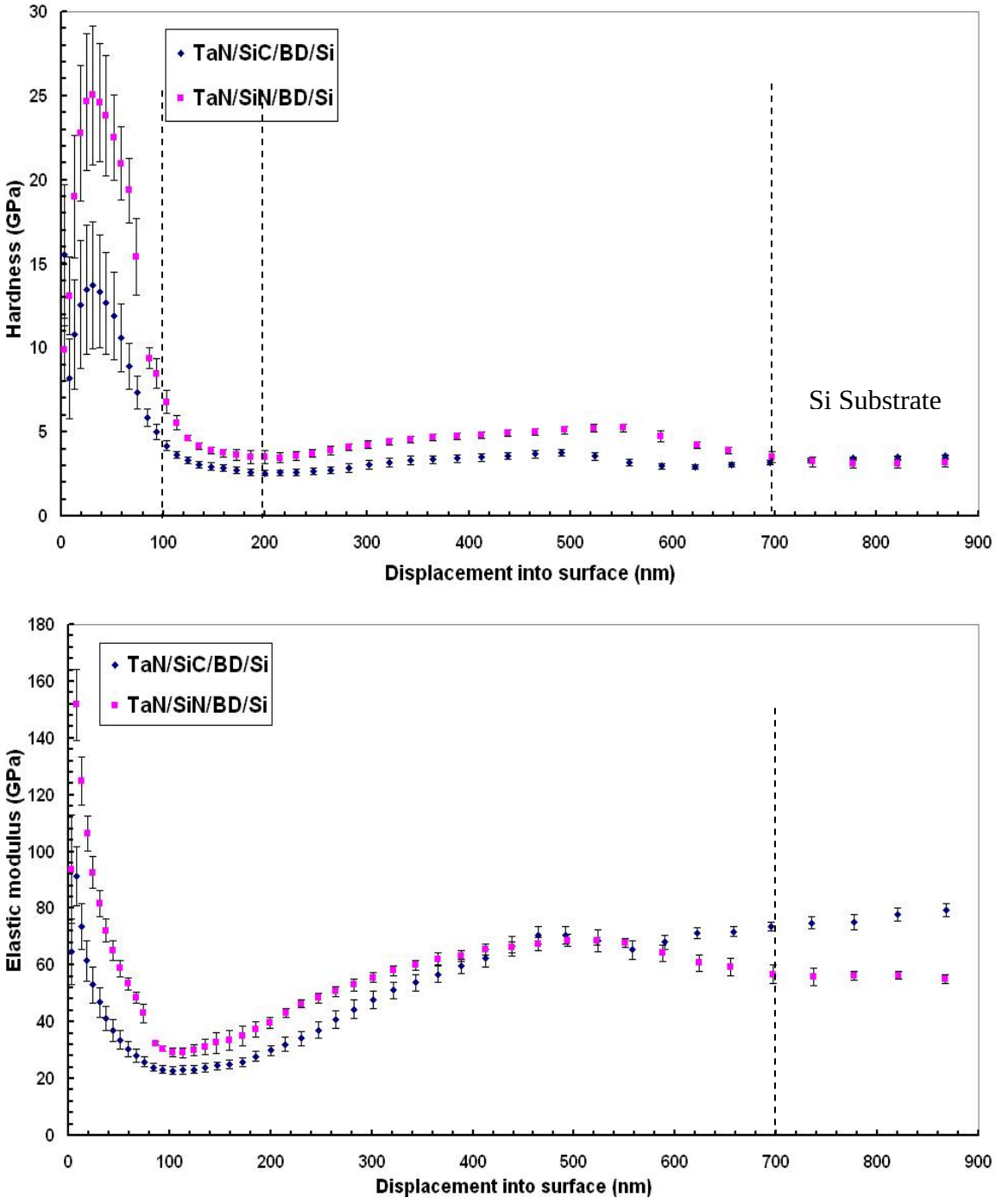


Fig. 4.19 Hardness and elastic modulus of TaN/SiC/BD/Si and TaN/SiN/BD/Si multilayered films.

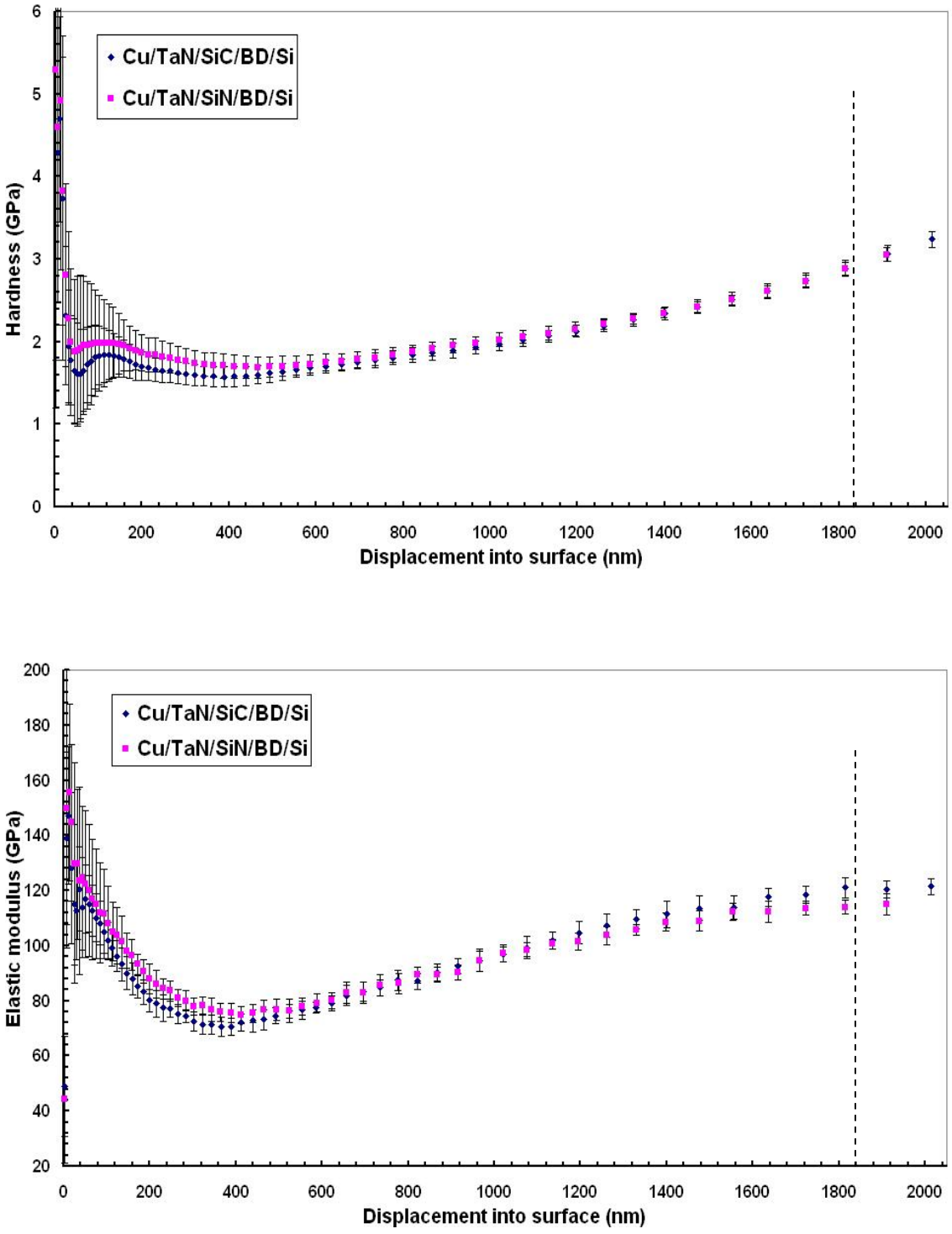
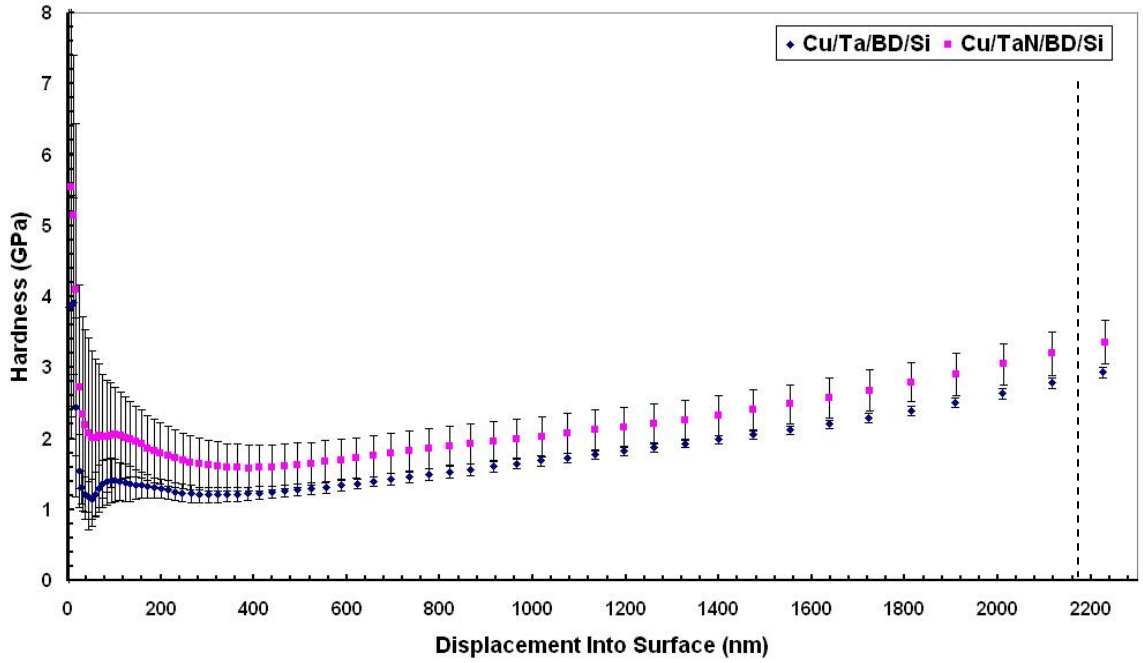


Fig. 4.20 Hardness and elastic modulus as a function of displacement for Cu/BD (low-k) stacked samples with Ta and TaN barrier layers and SiC and SiN cap layers



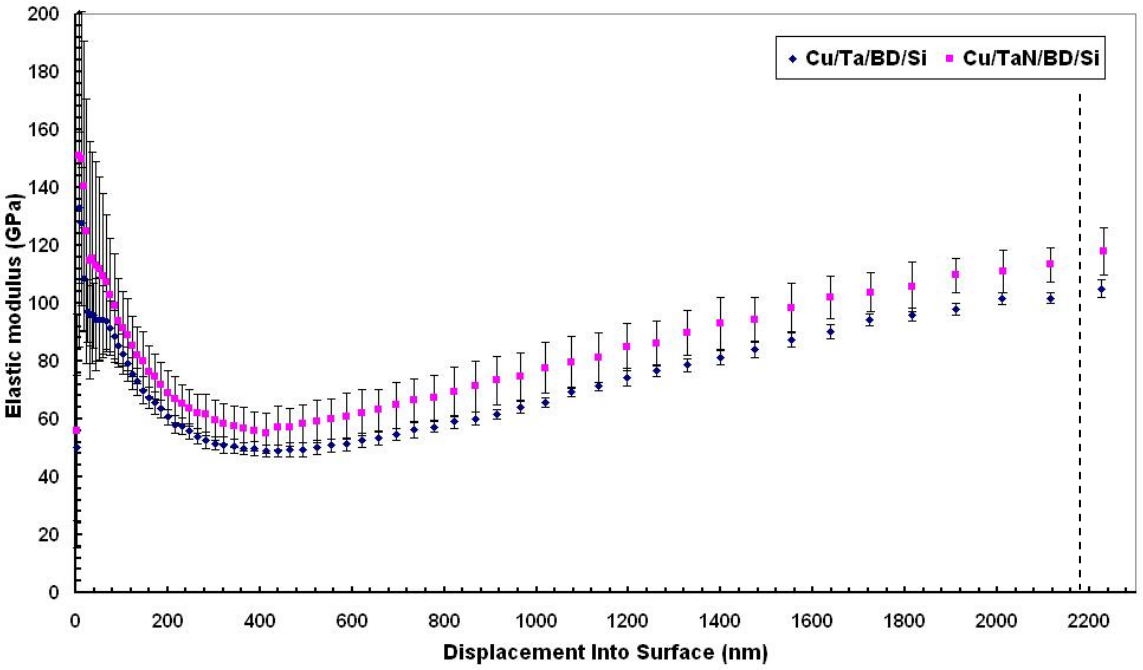


Fig. 4.21 Hardness and elastic modulus as a function of contact depth for Cu/Ta/BD/Si and Cu/TaN/BD/Si stacks measured using nanoindentation CSM technique.

4.3.2 Nanoscarcth testing

Nanoscratch tests were conducted on all samples, A to H, to assess the adhesion/cohesion strength. Nanoscratch behavior of these multilayered samples is rather complex when compared to BD films, single and dual dielectric stacks. Fig. 4.22 and 4.23 show nanoscratch profiles of all samples as scratch depth vs. normal load. Maximum ramp load employed for samples A to D is 50 mN, for samples E to F is 250 mN and for samples G to H, it is 200 mN. All nanoscratch experiments were conducted at a scratching speed of 1μm/s. Adhesive/cohesive strength of all samples reported in terms of critical load (Lc) are given in Table 5.3. Samples E-H show rough scratch profiles when compared to samples A-D mainly due to deep plowing of the indenter tip into the copper surface. Significant delamination is observed in samples A and all other samples show cohesive and mixed failures. Fig. 4.24 and 4.25 show SEM micrographs of scratch tracks on all samples produced during scratch testing. From SEM images, chipping/buckling failures are observed for samples A to D whereas samples E to H show deep plowing and pile up along the scratch tracks. For sample F, critical load couldn’t be measured as it didn’t show any significant excursion in scratch profile and tests couldn’t be performed with higher loads due to load limitation of the equipment.

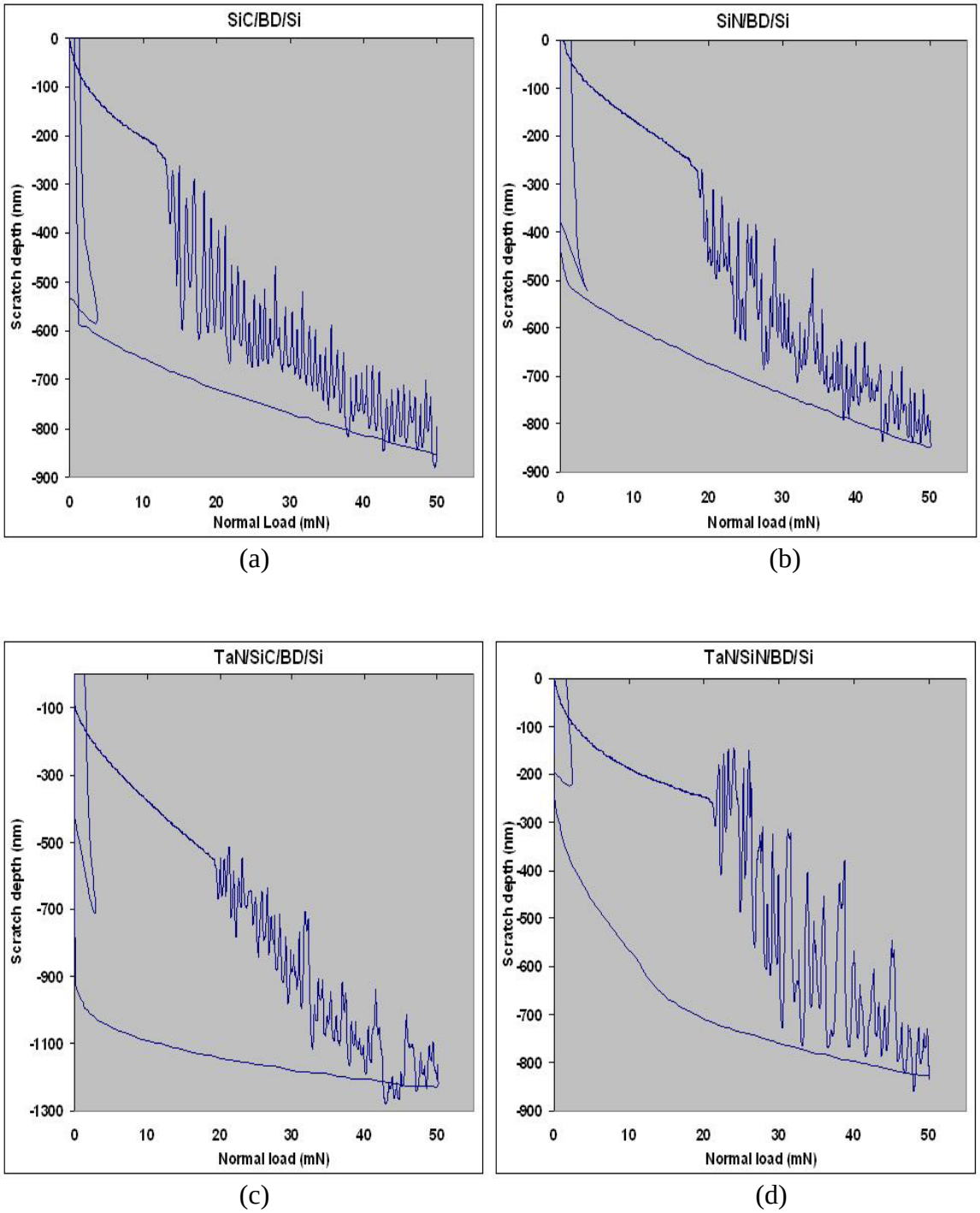


Fig. 4.22 Scratch depth vs. applied normal load curves during ramp loading scratch testing on multilayered samples.

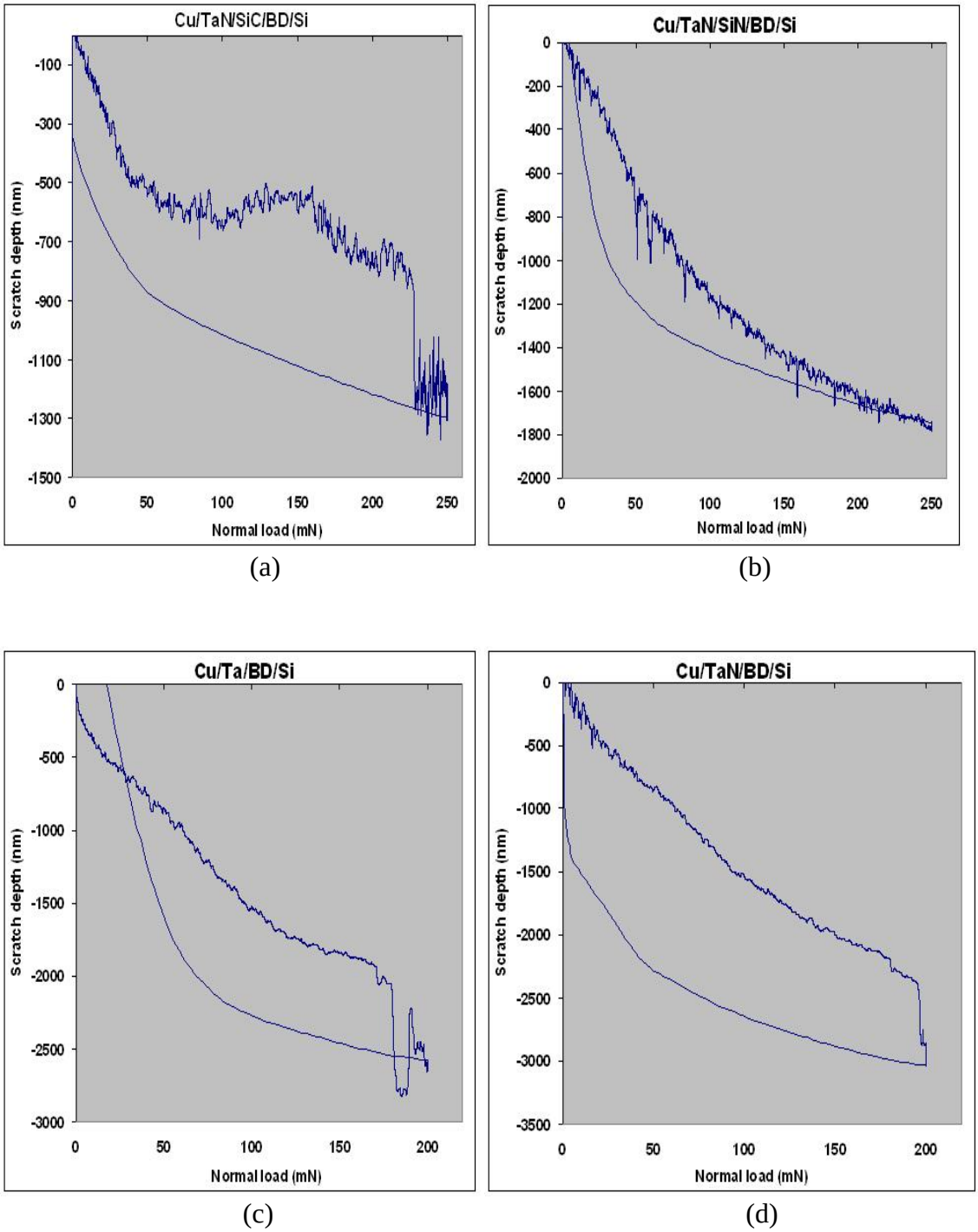
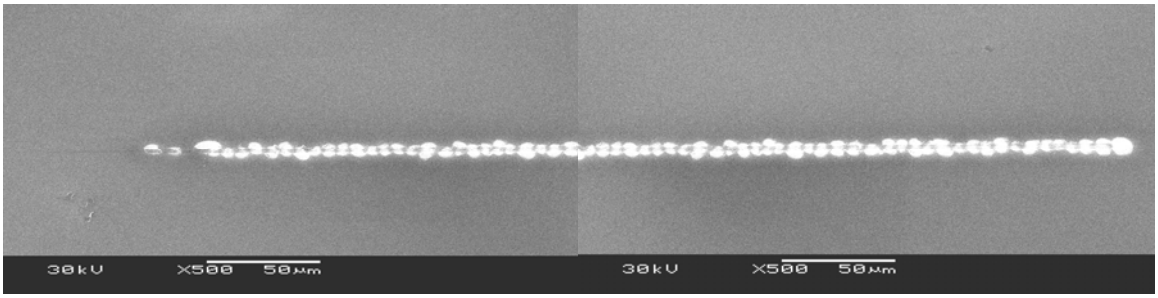
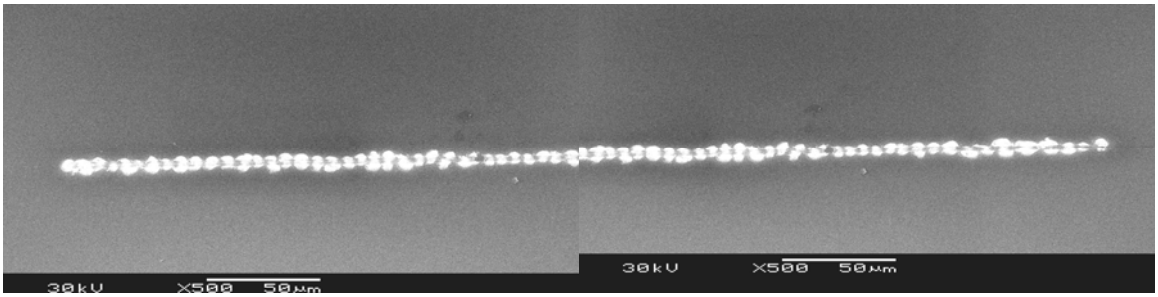


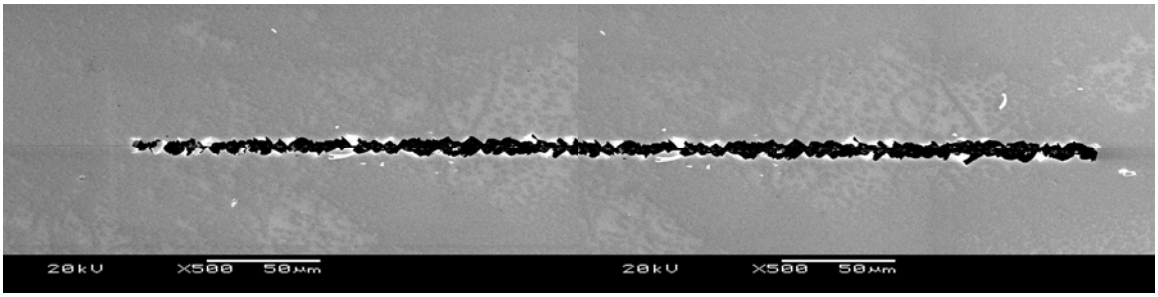
Fig. 4.23 nanoscratch test profiles of multilayered stacks.



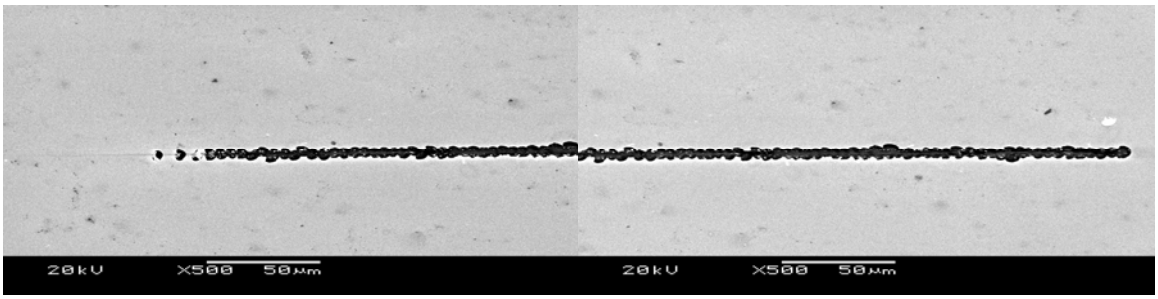
(a) SiC/BD/Si



(b) SiN/BD/Si

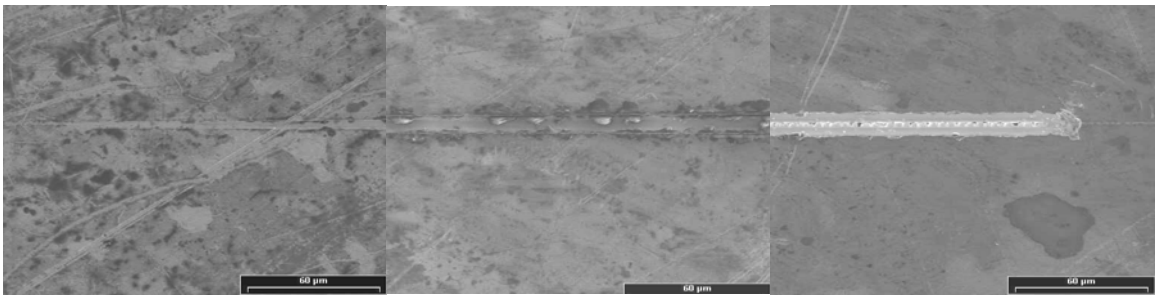


(c) TaN/SiC/BD/Si

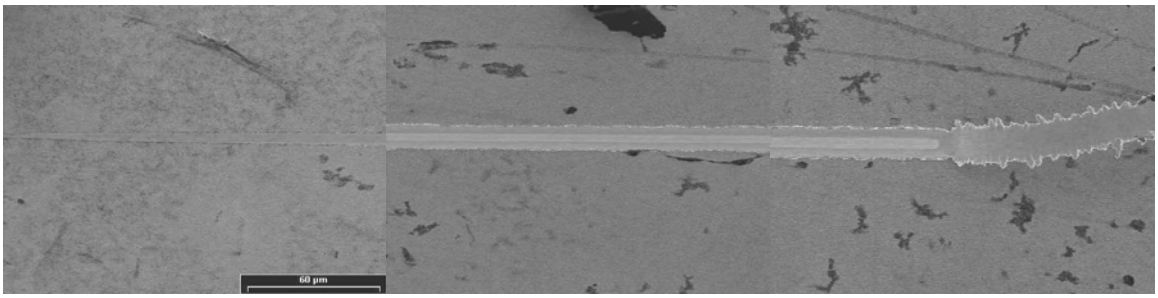


(d) TaN/SiN/BD/Si

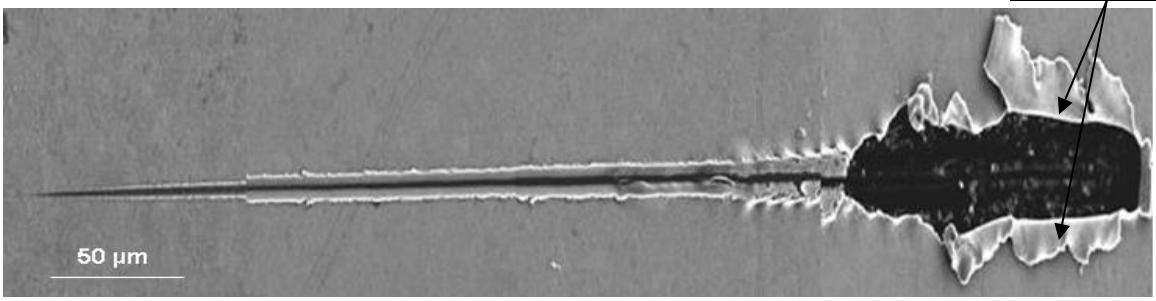
Fig. 4.24 SEM micrographs of scratch tracks made on Cu/low-k stacks.



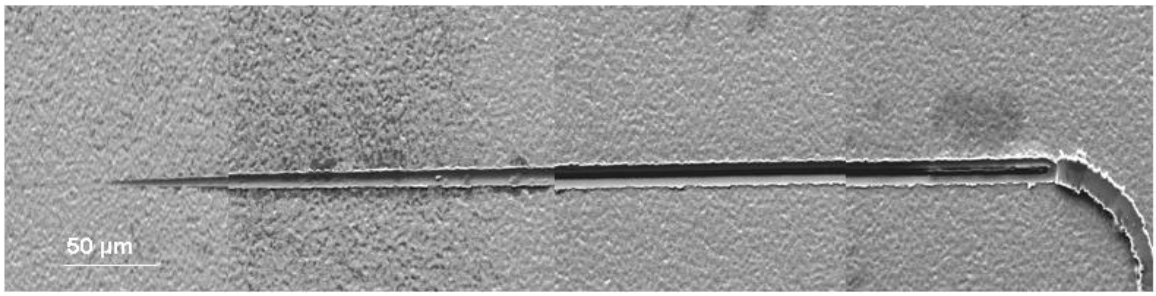
(a) Cu/TaN/SiC/BD/Si



(b) Cu/TaN/SiN/BD/Si



(c) Cu/Ta/BD/Si:



(d) Cu/TaN/BD/Si:

Fig. 4.25 SEM micrographs of Cu/BD stacks with SiC and SiN cap layers and Ta and TaN barriers.

4.4 Summary

This chapter has presented nanoindentation and nanoscratch test results of all samples under consideration. Both nanoindentation and nanoscratch tests were performed using Nano Indenter® XP system with respective attachments. For ease in understanding, the results in the present study are grouped into three sets as, a) Thickness dependence of nanomechanical properties of BD thin films (100-1200 nm), b) BD films with Ta and TaN barrier layers and c) Mechanical properties of Cu/BD stacks with Ta & TaN barrier layers and SiC & SiN cap layers. Nanoindentation and nanoscratch test results of each set were presented separately. At least ten nanoindentation tests and five nanoscratch tests were performed on different parts each sample. All tests have displayed good repeatability and the reported values represent the averaged values of these tests. Further discussions on the aforementioned results are presented in the next chapter.

CHAPTER 5: DISCUSSION

5.1 Thickness dependence of nanomechanical properties of BD (Black diamond ™, low-k) thin films

Film thicknesses of interconnect structures used in semiconductor industry continue to decrease as the chip size decreases. Usually, thickness of the dielectric film has small effect on electrical properties [85], but it has significant influence on the mechanical properties of the film. Hence, it is very important to study the mechanical properties of these films of minute thicknesses. The present study focuses on the thickness dependence of mechanical properties of the BD films of six different thicknesses; 100, 300, 500, 700, 1000 and 1200 nm. Nanoindentation and nanoscratch tests have been performed on all six samples.

5.1.1 Nanoindentation testing

The results presented in this work are an average of ten indentations made on different locations of the sample. The Poisson's ratio of all BD films in the nanoindentation experiment is taken as 0.25 because the Poisson's ratio has negligible effect on the indentation test results. The maximum indentation depth of each BD film is set in such a way that indenter penetrates at least 100 nm deep into the substrate. This is mainly to study the transition of mechanical properties from film to substrate, degree of substrate effect on whole thickness and threshold load of film cracking during indentation.

Fig. 4.1 shows typical load-displacement curves of all BD films (100-1200 nm) which were obtained during nanoindentation testing. All load-displacement curves show elastic-plastic behavior. Except for BD-100 nm film, all films show pop-in event within the film indicated by arrows in Fig 4.1. These pop-in events are results of the film cracking and delaminating between the BD film and the Si substrate. Fig. 4.2 shows the optical images of the cracked BD films after performing the nanoindentation experiment. From Fig. 4.2 (d) it may be observed that thicker films are more prone to delamination than thin films, as the BD-1200 nm film shows chipping around the indentation mark. Many researchers have observed this kind of fracture behavior (pop-in event) in various types of low-k materials, bulk glasses and silica foams [86-90]. Table 5.1 gives the information about BD films fracture/delamination during nanoindentation testing, in terms of threshold load, threshold indentation depth and % of thickness at which film cracking occurs. For 100 nm thick film, failure is observed when the indenter tip is in the substrate and it can be seen in Fig. 4.1 (a). In the case of BD films with thickness 300-1200 nm, failure is observed within the films at different loads and indentation depths as shown in Fig 4.1 b-f and Table 5.1, and, it is found that as the BD film thickness increases the threshold load of cracking and the threshold indentation depth increases. One common trend observed in the fracture among BD films (300-1200 nm) is that, the film failure (crack or/and delmaination) occurs at around 60-65% of the film thickness in indentation testing. This data is very useful in conventional nanoindentation processes to determine the properties of BD films, i.e. the threshold load for the BD films without cracking, threshold loads in CMP process and to measure the fracture toughness of the BD films.

Table 5.1 Summary of fracture behavior data for all BD samples in nanoindentation testing.

BD sample thickness (nm)	Threshold load of cracking (mN)	Threshold indentation depth of cracking (nm)	% of thickness at which cracking occurs (nm)
100	2.17 (*in substrate*)	142 (*in substrate*)	142
300	1.78	190.69	63.56
500	4.28	312.84	62.57
700	11.00	460.00	65.71
1000	18.83	644.00	64.40
1200	25.23	730.00	60.83

Hardness and Elastic modulus:

The hardness and elastic modulus as a function of displacement (indentation depth into the film thickness) of all BD samples are shown in Fig. 4.3 a-f. The property values are very high with large scatter of the data usually at the very beginning of the nanoindentation when the indenter just touches the film. This is mainly due to equipment noise, difficulty in determining the actual point of contact, limited resolution of the nanoindenter, indenter tip roundness, surface roughness, indentation size effect and strain gradient plasticity. Hence, the initial part of the data is usually discarded in nanoindentation analysis and this kind of problem has been observed by other investigators [91-92]. As the indentation depth increases initially slight decrease in hardness and elastic modulus values are observed and as the indentation depth further increases these property values reach minima, then tip starts sensing the effect of the substrate which results in higher hardness and elastic modulus values. The initial decrease of properties as the indentation displacement increases is observed during

nanoindentation of very thin films [93]. The averaged values of properties in minima plateau region are considered to be the real properties of the films and, in the present study, these values are used to define the properties of each film as shown table 4.2. The hardness values of all BD films are in the range of 1.66 to 2.02 GPa and the elastic modulus values are in the range of 9.27 to 16.48 GPa. Sharp deviations are observed in the property vs. displacement (see Fig. 4.3) graphs of all BD films, which corresponds to the pop-in events shown in Fig. 4.1, resulting from film cracking and/or delamination at the BD film-silicon substrate interface. Significant differences in mechanical properties are observed when the BD film thickness is less than 500 nm (100-500 nm), mainly in the case of elastic modulus. When the BD film thickness is greater than the 500 nm (500-1200 nm) very little or no significant variation in mechanical properties are observed and we can assume that these properties are representative of the bulk properties of the BD films. The thickness dependence of hardness and elastic modulus are shown in Fig. 5.1 with respective trend line equations. These curve fitting equations are very useful in estimating the mechanical properties of a BD thin film of any thickness under consideration.

The hardness minima property plateau region is considerably large and there is nearly no change with respect to different thicknesses, when compared with elastic modulus plateau region. The minima elastic modulus plateau region decreases as the BD film thickness decreases because the effect of substrate is more on elastic modulus for thinner films. In Fig. 4.3 and 4.4, it is observed that the sharp increase in modulus from the minima plateau region, mainly due to the effect of substrate, is much more on the

elastic modulus than on the hardness of the BD films. This is because the elastic modulus is associated with the elastic deformation during nanoindentation, and in contrast, the hardness response of the material is associated with plastic deformation. Simulation studies has shown that the a long range effect when compared to plastic deformation and therefore, the effective elastic modulus of a film experiences greater substrate effect than the hardness value [88]. BD -100 nm film shows significantly higher elastic modulus (E=16.48 GPa) when compared with higher thickness BD films and it is expected due to molecular restructuring in very thin BD films (≤100 nm), since the elastic modulus is an intrinsic material property, which largely depends on interatomic or molecular bonds [93]. Hence the higher elastic modulus of BD-100 nm film is probably expected due to stronger molecular bonding between organic (-CH_3) and inorganic (Si-O) constituents.

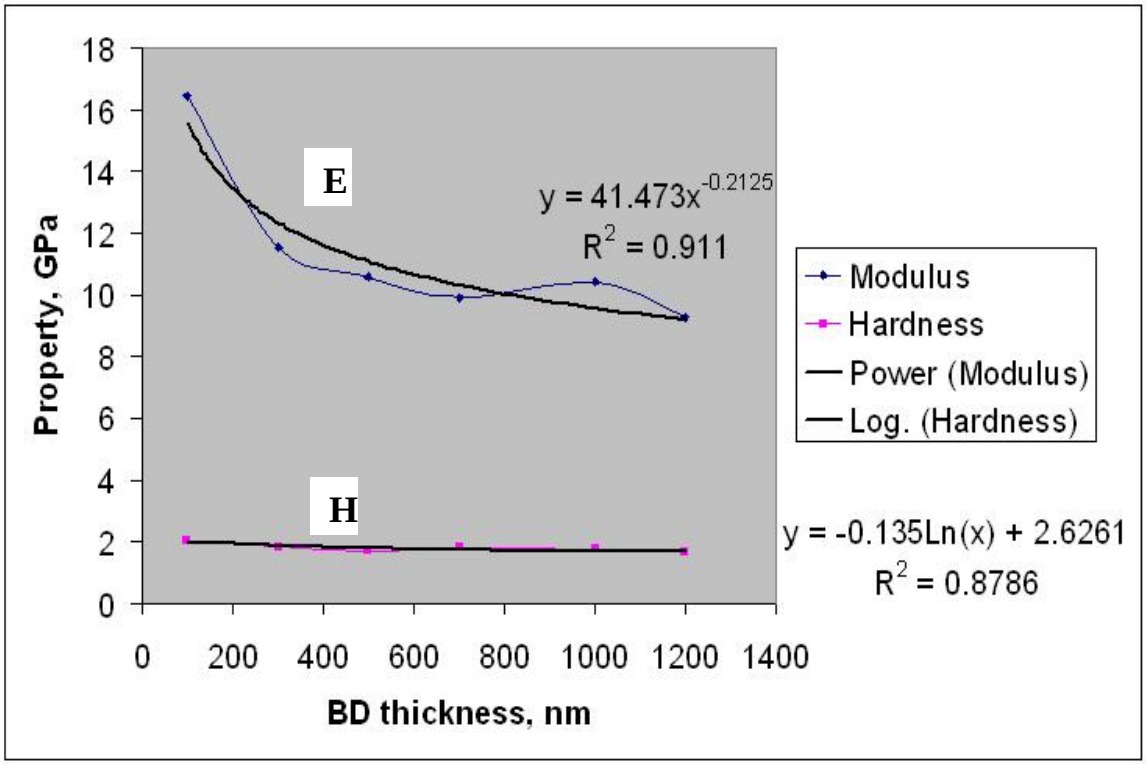


Fig. 5.1 Hardness (H) and elastic modulus (E) as a function of film thickness.

5.1.2 AFM analysis of residual nanoindentation impressions

The nanoindentation AFM analysis is presented for BD films of different thicknesses to examine the pile-up and sink–in behavior. Fig. 4.5 shows the AFM images of residual nanoindentation impressions and section analysis profiles of BD films (100 - 1200 nm). A regular triangular post-indent was observed for all BD films. The cross-sectional profile which corresponds to the thin line drawn on AFM image is presented for all BD films, shown in Fig 4.5. The height of the triangular indent and deformation behavior around the indenter can be estimated from the cross-sectional profile. From AFM analysis it is observed that the deformation behavior is not same for all BD films. The BD -100 nm film shows the pile-up behavior whereas the BD-300 nm film shows little pile-up behavior. BD films 500-1200 nm demonstrate significant sink-in behavior and the degree of sink-in behavior increases as the thickness of the BD film increases. Accordingly, the deformation behavior of BD films during nanoindentation is not same and strongly depends on the thickness. This behavior is dominant in very thin BD films ($\leq$ 100 nm) and it can also be related to the molecular restructuring of BD films.

5.1.3 Nanoscratch testing

Adhesion/cohesion strength of BD films of six different thicknesses was characterized by using the Nano Indenter® XP (MTS Corp., USA) system with nanoscratch option. A conical diamond indenter with tip radius of about 5 μm is employed for all nanoscratch experiments. A diamond conical indenter is preferred because it has uniform facing to all directions and symmetrical at any alignment, which removes directionality effect imposed by pyramid-type tips [84]. A scratch track of 400

μm with a constant scratch velocity of 1 μm/s was applied to all samples. The diamond stylus is ramp-loaded from 0 mN to 50 mN for all BD films.

Fig. 4.6 shows the nanoscratch profiles as scratch depth vs. normal load and Fig. 4.7 shows corresponding optical images of scratch tracks made on BD films of different thicknesses (100-1200 nm). At least five tests were performed on different parts of the each sample and all have displayed good repeatability. Adhesion/cohesion strength of all BD films was characterized by using the critical normal load at the first abrupt decrease (fluctuations) in the scratch depth. The failure of the BD films is identified by sudden decrease in the scratch depth followed by large fluctuations in the frictional force and the corresponding normal load with this failure is known as critical load (Lc). In scratching as in nanoindentation, the BD-100nm film shows completely different behavior when compared to higher thickness films. From Fig. 4.6 it can be observed that BD-100 nm film shows continuous damage, probably ductile deformation, and the detection of Lc is difficult as the resolution of the equipment is not sufficient to detect the same. From the nanoscratch data, as presented in Fig. 4.6 (scratch depth vs. normal load), and corresponding optical images as shown in Fig. 4.7, it is obvious that the critical load is well defined and consistent for all BD films (300-1200 nm). The critical loads for BD films (300-1200 nm) are in the range of 13.02-25.86 mN as summarized in Table 4.2. The critical load of the BD films increases as the thickness increases. The critical load of film failure of BD films as a function of film thickness is given in Fig. 5.2 and polynomial trend line is also shown. In the case of thinner BD films (100-500 nm), the accumulation of stress concentration is more due to substrate restraint which results in damage to the film at lower loads. By increasing the BD film thickness, the effect of the

silicon substrate will be less which ultimately will result in increase in critical load. The increase in the critical load with increasing film thickness doesn't necessarily mean the increase in adhesion between the BD film and silicon substrate [94].

In scratch testing generally two kinds of mechanical failures are observed, 1) delamination at the film-substrate interface due to lower adhesion strength (adhesive failure) and 2) cracking in the films due to lower cohesive strength (cohesive failure) [63]. From Fig 4.6 it is observed that the scratch profile for all BD films is not the same. BD films of thicknesses 300-500 nm show prominent cohesive failure as the stylus does not directly reach the substrate at the critical load. In the case of thick BD films (700-1200 nm), complete delamination is observed as the diamond stylus abruptly reaches the substrate. This can be verified by observing the optical images of the scratch tracks of all BD films as shown in Fig. 4.7. The width of the scratch track is increasing as the BD film thickness increases. Scratch track of BD-100 nm film as shown in Fig. 4.7 is very narrow and debris particles are observed along the scratch track indicating plowing and fracture actions. No debris is observed at the sides of scratch tracks for the BD 300-1200 nm films, whereas BD-300 and BD-500 nm thick films show mixed failure modes such as plowing and buckling. For the BD 700-1200 nm films, failure is initiated by the formation of a crack in the films as shown in Fig 4.7. Buckling or chipping failure is observed in BD films 300 to 1200 nm and the chip size increases as the film thickness increases. This shows that delamination is more prominent as the BD film thickness increases. Before the critical load is reached during ramp-load nanoscratching, no significant debris along the scratch track is observed.

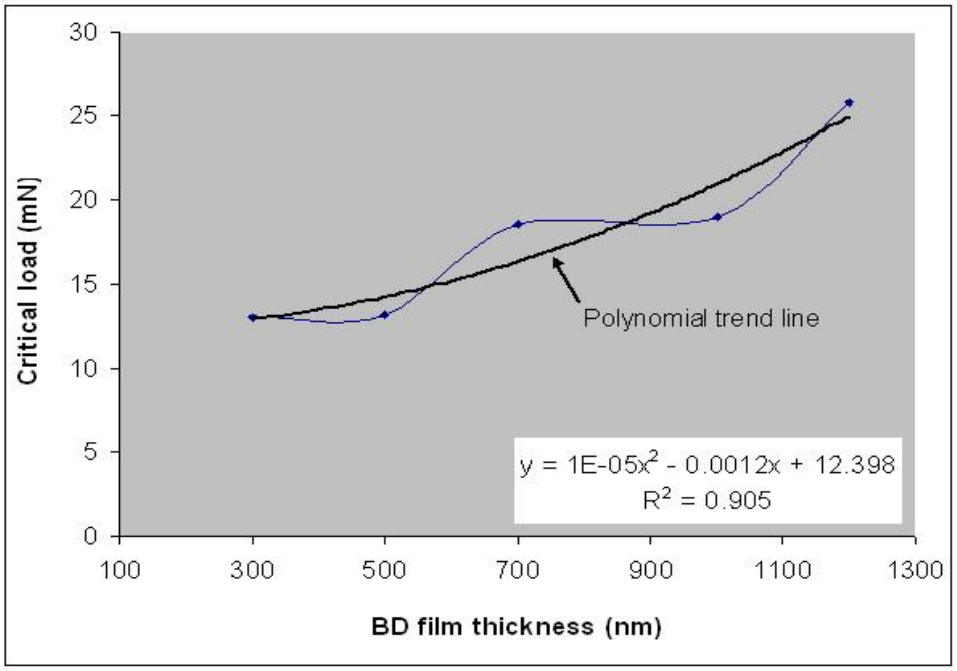


Fig. 5.2 Critical load (Lc) of film failure in scratch testing as a function of thickness for BD films.

5.2 BD films with Ta and TaN barriers

In this set of tests, four samples have been prepared with Ta and TaN barrier layers and dual stacks also have been prepared as BD/Ta/Si, BD/Ta/BD/Ta/Si, BD/TaN/Si and BD/TaN/BD/TaN/Si. Schematic diagrams of these stacks with respective thicknesses are given in Fig. 4.8. The application of Ta and TaN barrier layers to BD films improves stiffness in addition to other mechanical properties.

5.2.1 Nanoindentation testing

Fig. 4.9 a-d shows the load-displacement curves of single and dual dielectric stacks. The total thickness of single and dual dielectric stacks studied in the present work is 1025 and 2050 nm respectively. Both single and dual dielectric stacks show pop-in

events. Dual dielectric stacks demonstrate massive failure which can be observed as more pop-in events in load-displacement curves especially at the interfaces, which are shown as dotted lines in Fig. 4.9 b & d. This can be confirmed by observing the residual nanoindentation marks as shown in Fig. 10 a-d. Hence, it is expected that crack formation and/or delamination may occur at the interfaces due to indenter penetration as observed by J. Vitiello [95]. In the current study, stacks having same barrier layer (Ta or TaN) are compared with respect to mechanical properties.

5.2.1.1 Mechanical properties of BD/Ta/Si (single dielectric) and BD/Ta/BD/Ta/Si (dual dielectric) stacks

Hardness and elastic modulus of these stacks are compared in Fig. 4.11. High hardness values at the film surface for both stacks are observed mainly due to the inaccuracy of indenter tip functions and surface roughness [91]. Large fluctuations in hardness values throughout the film thickness measurements are observed due to the failure of stacks during the nanoindentation. Effect of substrate is more on single dielectric stack when compared with double dielectric stack, this is because the thickness of both the stacks are different and there is difference in the number of interfaces. The hardness and elastic modulus values of single dielectric stack is higher than the values for dual dielectric stack and these properties are consistent throughout the thickness of the stacks as shown in Fig. 4.11. The averaged minima property plateau is used to define the property of each stack and these values are given in Table 5.2. Single dielectric stack has hardness of 1.91 GPa and modulus of 10.03 GPa, whereas for dual stack, the values are 1.38 and 7.98 GPa respectively. From Fig 4.11, sudden deviations in properties are

observed mainly due to the film failure during nanoindentation process which corresponds to pop-in events in load-displacement curves as discussed earlier. This mechanical property data of single and dual stacks are very useful in CMP performance, for example, single dielectric stack has slower removal rate when compared to dual stack for the same CMP pressure [44]. This is mainly due to the higher hardness value of the single dielectric stack. Hence we can set the CMP pressures according to the stacks. From the data given in Fig. 4.11 and 4.12 it shows that, the effect of indentation size is very little or almost negligible.

5.2.1.2 Mechanical properties of BD/TaN/Si (single) and BD/TaN/BD/TaN/Si (dual dielectric) stacks

The schematic diagrams of these stacks with TaN barrier layer have been shown in Fig.4.8 c-d. The total thickness of these stacks are maintained same as in previous section, i.e. 1025 nm for single dielectric stack and 2050 nm for dual dielectric stack. Hardness and elastic modulus as a function of displacement of these stacks measured using the nanoindentation CSM technique is presented in Fig. 4.12. Single dielectric stacks have slightly higher mechanical properties when compared with dual dielectric stacks as summarized in table 5.2. In both cases, the performance of single dielectric stacks is better than that for the dual dielectric stacks.

Comparing the single dielectric stacks, BD/Ta/Si has higher hardness and elastic modulus than for BD/TaN/Si stack (Table 5.2). Thus barrier layer greatly affects the mechanical properties of the single stack. No significant difference is observed in the case of BD/Ta/BD/Ta/Si and BD/TaN/BD/TaN/Si dual dielectric stacks. It is anticipated that the

lower mechanical properties of dual stacks is mainly due to the presence of residual stresses. Usually, dual stacks have more residual stresses when compared with single dielectric stacks as dual-stacked samples are subjected to more processing steps. Compressive stresses in the stacks result in an increased hardness values but tensile stresses cause a decrease in hardness. Therefore, dual stacks are expected to have more tensile stresses when compared with single dielectric stacks.

Table 5.2 Summary of mechanical properties of single and double dielectric stacks.

multilayer stack	**total stack thickness (nm)**	**Hardness (GPa)**	**Elastic modulus (GPa)**	**Critical Load, Lc, (mN)**
BD/Ta/Si (Single dielectric stack)	1025	1.91	10.03	36.99
BD/Ta/BD/Ta/Si (double dielectric stack)	2050	1.38	7.98	50.90 (Lc_1) 53.04 (Lc_2)
BD/TaN/Si (Single dielectric stack)	1025	1.43	8.35	36.70
BD/TaN/BD/TaN/Si (dual dielectric stack)	2050	1.4	7.58	48.79 (Lc_1) 53.46 (Lc_2)

5.2.2 Nanoscracth behavior of BD stacks with Ta and TaN barriers

Nanoscratch tests were performed on both single and dual dielectric stacks with ramp-loading from 0 mN to a maximum load of 60 mN. Scratch test speed of 1 μm/s is maintained for all samples. Fig. 4.13 a-d shows the typical scratch depth vs. normal load profiles for all four samples. In the present study at least five nanoscratch tests were performed on different parts of each sample and all tests have shown good repeatability. Critical loads of all samples are summarized in Table 5.2.

From Table 4.2, BD-1000 nm film without any barrier layers (BD/Si) has critical load (Lc) of only 18.52 mN. Single dielectric stacked samples BD/Ta/Si and BD/TaN/Si record critical loads of 36.99 and 36.70 mN respectively. By obtained results and comparing the critical loads of BD films with and without barrier layers, it is obvious that barrier layer effectively increases the adhesion strength of the BD film to the substrate. No significant difference is observed in critical loads of the single dielectric stacks. Thus the performances of Ta and TaN barrier layers of thickness 25 nm in single dielectric stacks on adhesion strength are almost same. Both stacks (BD/Ta/Si and BD/TaN/Si) show a complete delaminating behavior i.e. at critical load Lc, the diamond stylus abruptly hits the silicon substrate as shown in Fig 4.13 a & c by a dip in the scratch depth. The scratch tracks of these stacks show chipping/buckling failure as shown in Fig. 4.14 a & c and scratch track width is almost same. Just before the critical load, small cracks are observed in the BD films which are expected to initiate the delamination or failure of the film.

Typical scratch profiles of BD/Ta/BD/Ta/Si and BD/TaN/BD/TaN/Si dual stacks are shown in Fig. 4.13 b & d. These dual stacks show two critical loads (Lc_1 & Lc_2) as two steps in scratch depth vs. normal load profile as shown in Fig. 4.13 b & d. Dual stack with Ta barrier layer (BD/Ta/BD/Ta/Si) has critical loads as Lc_1=50.90 and Lc_2=53.04 mN, and dual stack with TaN barrier layer (BD/TaN/BD/TaN/Si) has critical loads of Lc_1=48.79 and Lc_2=53.46 mN. Both dual stacks with Ta and TaN barrier layers show no significant difference in critical loads and critical loads of these stacks are given in Table 5.2. The critical load values of both dual dielectric stacks were summarized in Table. 5.2.

From Fig. 4.13 b & d it is observed that these dual stacks delaminate in the same way as single dielectric stacks, but in two instances. In the first instance at critical load Lc_1, top BD film delaminates as stylus hits at the interface and after attaining little higher load Lc_2 the under BD layer in the dual dielectric stack fractures and delaminates. Optical micrographs of scratch tracks of these dual stacks are given in Fig. 4.14 b & d and corresponding critical loads (Lc_1 & Lc_2) are also indicated. After Lc_1 the failure of the film is like buckling or chipping and as soon as stylus reaches the load corresponding to the Lc_2, massive failure of the film is observed. The massive failure in scratch tracks of dual stacks than single dielectric stacks is mainly because the critical loads associated with dual stacks are much higher than the single dielectric stacks. Hence, once the crack initiates, it propagate to a larger distance for dual stacks than for single dielectric stacks.

Dual stacks have better performances in nanoscratch testing in terms of higher critical loads when compared with single dielectric stacks (see Table 5.2). This is because of the differences in the effects of substrate on single and dual dielectric stacks. Usually, the effect of substrate is more on thinner samples than thicker ones. Single dielectric stacks have total thickness of 1025 nm and dual stacks have total thickness of 2050 nm, and thus, the effect of substrate on single dielectric is more when compared with dual dielectric stacks. Accordingly, single and dual stacks have differences in their recorded critical loads.

5.3 Mechanical properties of Cu/BD multilayered stacks by nanoindentation and nanoscarcth testing

This set contains eight multilayered Cu/BD samples with Ta and TaN as barrier layers and SiC and SiN as cap layers. Nanoindentation and nanoscratch tests have been performed on all samples to asses the mechanical properties of the multilayer stacks. For convenience in elucidation of results, these multilayered samples are labeled from A to H as given in Table 5.3. The mechanical properties of these samples are compared based on cap layers (SiC & SiN) and barrier layers (Ta & TaN), so the comparison would be between samples A &B, C&D, E &F and G&H.

5.3.1 Samples A (SiC/BD/Si) and B (SiN/BD/Si)

The total film stack thickness of these multilayered stacks is 600 nm. The load-displacement curves of these are shown in Fig. 4.16 a & b. Pop-in events in these stacks are observed at an indentation depth of around 650 nm i.e. in the silicon substrate. Hardness and elastic modulus as a function of these stacks stacks are given in Fig. 4.18 and properties are found to decrease as the displacement increases. Sample B shows little fluctuations in properties when compared with sample A, expected mainly due to higher roughness value. Surface roughness of the sample B is Ra= 0.486 nm and for samples A is Ra 0.316 nm. Hardness and elastic modulus of sample B is higher throughout the displacement when compared with the sample A. One common observation for these two samples is that minima property values are observed at the SiC/BD and SiN/BD interfaces. The interface elastic modulus increases with displacement mainly due to the substrate effect. For this reason, the properties at 30 nm indentation depth are used to

define the property of these samples as presented in Table 5.3 and these values (elastic modulus and hardness) are also less than the corresponding single layer materials [96-97]. The commonly used rule of thumb that indentation depth must be less than 10 % of thickness of the film or material is not applicable here as huge fluctuations in the load-displacement curve are observed at the surface (<20 nm). This rule is more feasible for micrometer thick films [91].

The scratch depth vs. normal load profiles of these samples are given in Fig. 4.22 a & b. The maximum ramp load applied during ramp scratch testing is 50 mN. Sample B shows higher critical load (19.15 mN) than sample A (13.00 mN) and corresponding values are presented in Table 5.3. Adhesive failure is more prominent in sample A whereas in sample B, cohesive failure is more prominent as observed from scratch profile from Fig. 4.22 a & b. The failure mode observed in these multilayers does not happen layer by layer but rather the failure is initiated in the BD film as observed from scratch profiles. SEM micrographs of scratch tracks on these samples are given in Fig. 4.24 a-b and chipping/buckling failure is observed on both samples.

5.3.2 Samples C (TaN/SiC/BD/Si) and D (TaN/SiN/BD/Si)

These samples show pop-in behavior within the multilayered stack especially in the BD films because of their lower mechanical properties when compared to SiN and TaN films and it can be observed from Fig. 4.16 b-d. The maximum penetration depth was fixed in such a way that the indenter penetrates into the silicon substrate. Sample C shows pop-in event at lower load (~ 18 mN) when compared to sample D (~27 mN). The hardness and elastic modulus as a function of displacement measured by CSM technique

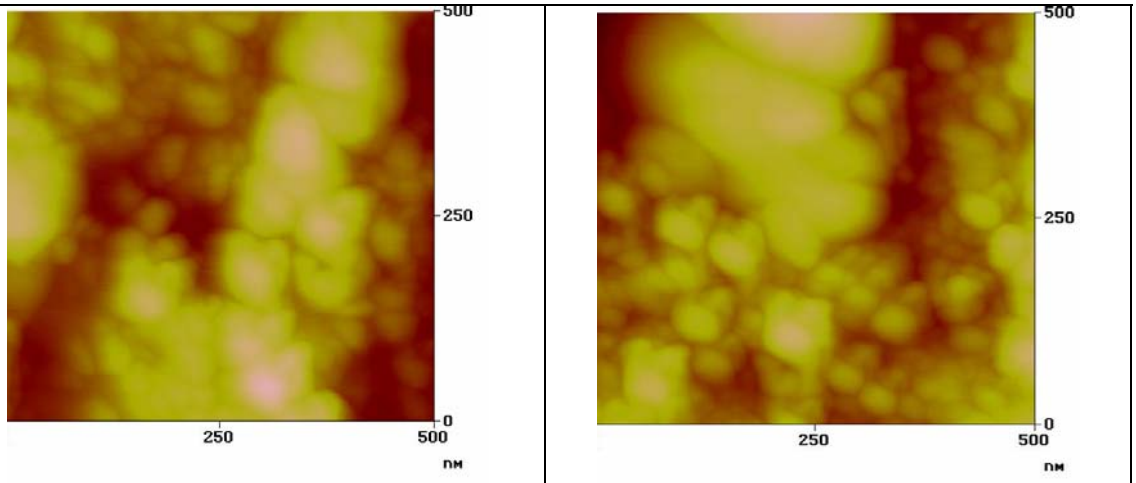
are given in Fig. 4.19. Top layer TaN in both samples shows higher mechanical properties when compared to it's under layer mainly due to better mechanical properties of TaN. Sample D records higher hardness and elastic modulus than sample C because of the presence of SiN layer in sample D. This can be verified from the comparison of mechanical properties of samples A &B in previous section, where sample B shows higher mechanical properties than A due to the presence of SiN top layer in B. The properties of C & D samples decrease as the displacement increases reaching lower values at the (TaN/SiC & TaN/SiN) interface. Hence, hardness and elastic modulus values at 30 nm displacement are used to define the properties of these multilayered stacks as presented in Table 5.3.

Nanoscratch profiles of C & D samples are given in Fig 4.22 c & d. Sample D shows higher critical load (23.04 mN) than sample C (17.37 mN). In both samples no delamination is observed between barriers and cap layers or cap layers and BD. Failure of the films occurred in BD film only and no clear delamination was observed, as noticed from scratch profile of these samples. These samples show almost similar failure mode with different critical loads and scratch tracks of these samples are given in Fig. 4.24.

5.3.3 Samples E (Cu/TaN/SiC/BD/Si) and F (Cu/TaN/SiN/BD/Si)

Both samples have copper as top layer and TaN as barrier layer. Sample E has SiC as cap layer and F has SiN cap layer. These multilayered stacks do not demonstrate any pop-in events in the load-displacement curve, suggesting no cracking or delamination events as shown in Fig.4.17a-b [98]. Hardness and elastic modulus values presented here are averages of ten indentations as given in Fig 4. 20. The reduction of properties (H &

E) is observed as a function of displacement into the surface which is mainly due to the indentation size effect at shallow indentation depths [74]. For these stacks, the averaged values of minima property plateau regions is used to define the properties of respective stacks as the minimum plateau region is in the top copper layer. These elastic modulus values are lower than polycrystalline single copper thin film (E= 120-130 GPa) mainly due to the presence of copper in multilayer, residual stresses in the stack and the corresponding elastic modulus is highly sensitive to substrate and under layers. From minima region, the increase in hardness and elastic modulus might be explained by the influence of under layers and substrate. Sample F exhibits higher hardness and elastic modulus than sample E as shown in Fig 4.20 and Table 5.3. The difference in mechanical properties of these stacks is expected mainly due to presence of under layers, residual stresses and variation in grain size. Typical grain morphology of copper in these stacks was imaged with AFM and higher mechanical properties of sample F mainly attributed due to the finer grain size of copper top layer than copper grain size of sample E as show in Fig. 5.3.



Cu/TaN/SiC/BD/Si (E)- Coarser grains	Cu/TaN/SiN/BD/Si (F) – finer grains

Fig. 5.3 AFM images showing grain structure of copper in E and F sample stacks.

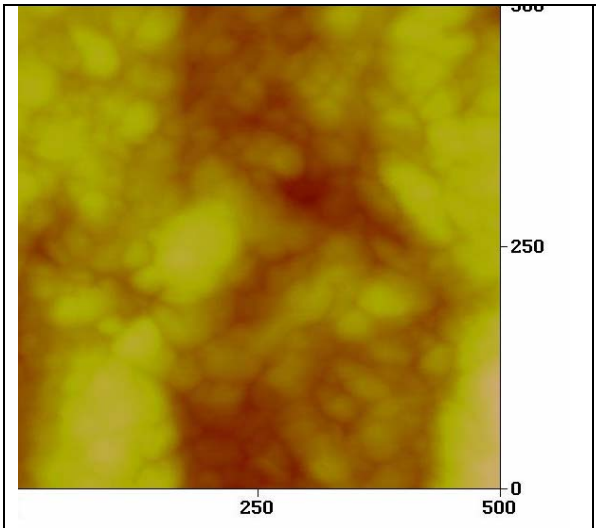
In Fig 4.23 a & b, nanoscratch depth profiles are presented for a normal maximum load of 250 mN. Scratch profiles of these stacks show fluctuations mainly expected due to the ductility of copper layer. Critical load could be identified for sample E (227 mN) and for sample F, no significant critical load is observed from the obtained scratch profile. For sample F, critical load could have been higher than 250 mN and the scratch tests could not be performed with >250 mN due to equipment limitation. The scratch tracks of these films are shown in Fig. 4.23 a-b. From the obtained scratch data and the examination of the scratch tracks under SEM, delmaination of copper top layer is not observed. It infers that copper has good adhesion with its TaN under layer. The scratch performance of sample F is better than that of sample E.

5.3.4 Samples G (Cu/Ta/BD/Si) and H (Cu/TaN/BD/Si)

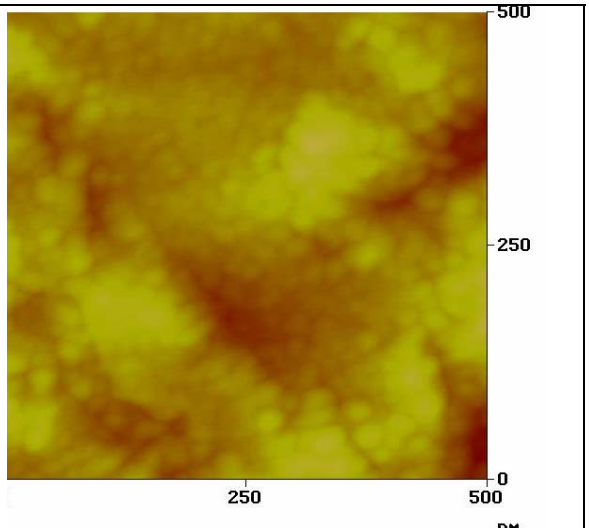
The load-displacement curves of these stacks are given in Fig. 4.17c-d. From the load-displacement curves it is evident that plastic deformation is more dominant due to fast increase in displacement during loading and elastic recovery is very small [99]. The properties of these samples depend on the penetration depth and show similar trends as presented in Fig 4.21. The properties of sample G are hardness=1.54 & elastic modulus=97.24 GPa and for sample H, hardness=2.7 & elastic modulus=124.83 GPa. The reduction in properties (H & E) of these stacks observed with respect to shallow contact depth is due to the indentation size effect. The reasons for the indentation size effect for thin films have been identified as quantized slip or deformation band formation, anelastic recovery of small indents, low probability of finding mobile dislocations, presence of residual stresses in the sample, errors associated with the area function of the

indenter at the small values of penetration depth and friction between the indenter and thin film sample [76]. The most prevailing mechanism of indentation size effect observed in copper thin films is due to the strain gradient plasticity as proposed by Huang et al [100] and Gao et. al [101]. This theory is applicable to sample E and F as they contain copper as top layer of about 1 μm thickness.

The averaged properties of the minima plateau region are used to define the properties of these samples as the minima plateau region is in the top copper layer and the values are tabulated in Table 5.3. From Fig. 4.21 it can be observed that the hardness and elastic modulus of the sample H is higher than the sample G, mainly expected due to the finer grain size of sample H compared to sample G. The AFM grain size images of these samples are presented in Fig. 5.4. Usually, polycrystalline materials with finer grain size show higher yield strength when compared with the coarser grain sized materials [99]. The difference in grain size of these samples is expected due to the differences in the residual stresses and the under layers.



(a) Cu/Ta/BD/Si (G)
Coarser grains



(b) Cu/TaN/BD/Si (H)
Finer grains

Fig. 5.4 AFM images showing grain structure of (a) Cu/Ta/BD/Si-G and (b) Cu/TaN/BD/Si-H

Fig. 4.23 shows the typical scratch depth vs. normal load profiles with ramping normal load of 200 mN. The scratch behavior during application of normal load on these multilayered stacks can be studied from these graphs. It is evident that the increment in the penetration depth with normal load is almost same in these samples. Abrupt changes in penetration depths are observed (Fig 4.23c-d) and loads associated with this event are termed as critical loads (Lc). Sample H shows higher critical load (Lc=198 mN) than sample G (Lc=164 mN), which is expected due to higher mechanical properties of sample H. These samples show severe plowing and pile up along the sides of scratch tracks as observed from SEM micrographs in Fig. 4.25c-d and only sample G shows significant delamination at higher loads.

Table 5.3 Summary of mechanical properties of Cu/BD multilayered stacks.

label	Multilayered stack on Si substrate	Total film thickness (nm)	Hardness (GPa)	Elastic modulus (GPa)	Critical load (mN)
A	SiC/BD/Si	600	4.98	18.86	13.00
B	SiN/BD/Si	600	11.08	38	19.15
C	TaN/SiC/BD/Si	700	13.72	46.82	17.37
D	TaN/SiN/BD/Si	700	25.02	81.80	23.04
E	Cu/TaN/SiC/BD/Si	1850	1.58	71.94	227
F	Cu/TaN/SiN/BD/Si	1850	1.70	76.45	≥250
G	Cu/Ta/BD/Si	2175	1.20	50.13	164
H	Cu/TaN/BD/Si	2175	1.63	58.38	198

CHAPTER 6: CONCLUSIONS

Black diamond, SiC and SiN films were prepared by using PECVD technique. Sputtering technique was employed to deposit the copper seed (150 nm), Ta and TaN layers. Copper film of 1μm thickness was deposited by electroplating process. Present study focuses on the mechanical characterization of BD (low-k, Black Diamond ^{TM}) thin films of various thicknesses and various Cu/BD stacks with Ta & TaN barrier layers and SiC and SiN cap layers which are of interest in BEOL technology. Hardness and elastic modulus properties were measured by nanoindentation CSM technique. Adhesion /cohesion strength of all samples were measured using nanoscracth technique and reported in terms of critical load (Lc). Both nanoindentation and nanoscratch tests have been performed on Nano Indenter® XP (MTS Corp. USA) system with respective attachments. Based on the obtained results and discussions presented in the preceding chapters, following conclusions are made:

Thickness dependence of mechanical properties of BD films (100, 300, 500, 700, 1000 and 1200 nm)

All BD films except BD-100 nm, shows pop-in event within the film. The mechanical properties of BD films of six different thicknesses are in the range of H=2.02-1.66 GPa and E=16.48-9.27 GPa. Thickness dependence of mechanical properties was observed when BD film thickness is less than 500 nm. Among these films, BD-100 nm film shows significantly higher mechanical properties than other films which is expected due to the molecular restructuring in ultra thin BD films (≤ 100 nm).When BD films are thicker

than 500 nm, the elastic modulus and hardness are nearly independent of the film thickness and equal to ~1.70 and ~10 GPa respectively.

In nanoscratch testing, the critical load was strongly dependent on the thickness of the BD films and it increases as the thickness increases. For BD-100 nm, the critical load couldn't be determined due to ductile damage to the film at very lower loads and lower resolution of the equipment. For BD 300-500 nm films, cohesive failure is observed and for 700-1200 nm films, adhesive failure is more dominant. Scratch track width increases as the thickness of the film increases.

BD stacks with Ta and TaN barriers

Single and dual dielectric stacks show pop-in events in load-displacement curve. Dual dielectric stacks experience greater adhesive/cohesive failure in nanoindentation testing than single dielectric stacks. Substrate effect is more pronounced in the single dielectric stacks than in the dual stacks mainly due to the difference in total film thickness. Hardness and elastic modulus of single dielectric stacks are higher when compared to dual dielectric stacks mainly attributed to differences in the number of interfaces, total film thickness and residual stresses.

Barrier layers (Ta or TaN) at the BD/substrate have shown significant improvement in adhesion strength (doubles) when compared with BD film without barrier layers. Single and dual dielectric stacks fail by delamination in nanoscratch testing. Layer by layer delaminations are observed in dual stacks which are reported as Lc_1 and Lc_2. In the dual dielectric stacks the scratch damage is greater than in the single dielectric stacks mainly due to high critical loads associated with dual dielectric stacks.

Cu/BD multilayered stacks with Ta & TaN barrier layers and SiC & SiN cap layers

Nanomechanical behavior of these samples is some what complex due to the variations in the residual stresses and the adherence between interfaces. Pop-in events are observed in load-displacement curves of samples A-D. Samples E-H, with copper as top layer, did not show any pop-in events in load-displacement curves suggesting that no cracking or debonding occurred. Samples with SiN cap layer (samples A-F) have higher hardness and elastic modulus when compared to stacks with SiC cap layer. SiN cap layer in multilayered stack enhances the mechanical properties more in comparison to SiC cap layer. Copper grain size also plays significant role in improving the mechanical properties of Cu/BD stacks (E-H) as studied by AFM grain size analysis.

In the nanoscratch testing, significant delamination is observed between BD/Si interfaces. No or very minor delamination is observed between cap layer & BD, barriers & cap layer and copper & barriers. Cohesive failure is more dominant failure mechanism in multilayered stacks but film failure in scratch track is different and mainly depends upon the nature of the top layer.

CHAPTER 7: RECOMMENDATIONS

- Nanomechanical characterization of BD thicknesses less than the 100 nm as the real IC device consists of minute features of dielectric films.

- Structural analysis of BD 100 nm and <100 nm thick films and relation to the mechanical properties of the BD films, mainly to find whether there is any molecular reorganization of BD ultra thin films.

- Study the mechanical behavior of triple and higher dielectric stacks as the real multilevel interconnects contain up to eight metallization levels.

- Further work should be carried out on multilayered stacks to understand the effects of change of stack order, thickness of each layer in stack, micro structural analysis of metal films and residual stresses on mechanical properties.

- Investigate the nanomechanical behavior of patterned Cu/BD stacks.

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