CHARACTERIZATION AND MODELING OF MOSFETS FOR RF APPLICATIONS

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Summary

Concomitant with a lack of reliable pure-mode multi-port measurement techniques, the conventional characterization of MOSFETs has been carried out in two-port form by tying the bulk and source terminals together to ground. This is found to be an incomplete description of device behavior, as it fails to capture the effect of non-zero body bias and substrate signal coupling at RF, which affects the accuracy of RF device modeling. Moreover, an accurate description of the terminal charges is not possible from two-port characterization involving only the gate and drain terminals. A three-port characterization is thus required to fully describe the electrical behavior of a MOSFET.

This work describes the complete three-port characterization of a MOSFET valid up to 15GHz in all regions of operation, from two-port S-parameter measurements. The approach is to obtain accurate two-port Y-parameters in three different configurations (GD, GS and SD) and appropriately assemble them to generate three-port data. The work reports the characterization of the GPG probe used for bias feed at the un-calibrated third port and identifies the undesirable effect of the probe's 'lossy' and inductive behavior on two-port measurements of the MOSFET at RF. Such a behavior necessitates the de-embedding of the GPG probe's parasitic impedance from the measured two-port Y-parameters of the device. To this effect, a generic RF small-signal equivalent circuit and model-based parameter extraction scheme is developed for the MOSFET. The scheme utilizes the measured probe impedance and three physical parameters extracted from a novel test structure named SD-R. The extracted equivalent circuit model parameters are used to generate the accurate two-port Y-parameters after removing the probe impedance. These two-port Y-parameters are then used to assemble the three-port data.

The same equivalent circuit model parameters obtained uniquely from different two-port configurations are found to match very well, thus establishing the consistency of the extraction scheme. An excellent match is observed in each of the redundant main diagonal elements of the three-port admittance matrix, obtained from two different two-port configurations. This confirms the effective de-embedding of the probe's impedance and establishes the accuracy of three-port characterization. The extracted junction admittances in the on-state, from the measured and simulated SD-R device data are shown here for the first time at different bias and frequency and their behavior is explained with the help of device physics. The general utility of this novel SD-R device towards RF MOSFET modeling and extraction is also discussed.

The measured three-port terminal capacitances of the MOSFET obtained as functions of bias and frequency are reported here for the first time along with 2-dimensional device simulation results to validate the characterization. The non-quasi-static effect is shown to manifest as the increasing difference between the magnitudes of trans-conductance obtained from the common-source configuration and of that obtained from the common-drain configuration.

This work reports the bias and frequency dependence of all terminal charges of the MOSFET, extracted from its measured three-port capacitances, for the first time and discusses its implications towards RF MOSFET modeling and circuit simulation.

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List of Abbreviations and Symbols

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
CMOS	Complementary MOS
RF	Radio Frequency
IC	Integrated Circuits
DC	Direct Current
AC	Alternating Current
BSIM	Berkeley Short-channel IGFET Model
EKV	Enz-Krummenacher-Vittoz MOS model
NQS	Non-Quasi-Static effect
VNA	Vector Network Analyzer
DUT	Device Under Test
EMI	Electro-Magnetic Interference
GSG	Ground-Signal-Ground
GSGSG	Ground-Signal-Ground-Signal-Ground
GPG	Ground-Power-Ground
ISS	Impedance Standard Substrate
LRRM	Load-Reflect-Reflect-Match
LRM	Load-Reflect-Match
TRL	Thru-Reflect-Line
SOLT	Short-Open-Load-Thru
TCAD	Technology Computer-Aided Design

GPIB	General Purpose Interface Bus
IC-CAP	Integrated Circuit - Characterization and Analysis Program
PEL	Parameter Extraction Language
LDD	Lightly Doped Diffusion
RTA	Rapid Thermal Anneal
S-parameters	Scattering parameters
Y-parameters	Admittance parameters
GD	Gate-Drain (common source) configuration
GS	Gate-Source (common drain) configuration
SD	Source-Drain (common gate) configuration
SD-R	New test structure with large resistance on the gate
S	Sub-threshold slope of the MOSFET in mV/decade
V_{th}	Threshold voltage of the MOSFET in V
L	Channel Length of the MOSFET in μm
W	Width of the MOSFET in μm
t_{ox}	Gate oxide thickness of the MOSFET in nm
y_{ij}	Admittance parameter at port 'i' due to port 'j'
c_{ij}	Capacitance at port 'i' due to port 'j'
Re(y)	Real part of a complex number y
Im(y)	Imaginary part of a complex number y
f_t	Cut-off frequency of the MOSFET at a given bias
R_{gsh}	Sheet resistance of the gate poly silicon in Ω/square
R_{dsw}	Drain-to-source resistance in Ω-μm

Chapter 1: Introduction

The advancement in CMOS technology has resulted in rapid downscaling in the size of the MOS transistor. The minimum possible MOS channel length (feature size) for a given technology, also referred to as the technology node, has reached well into the deep sub-micron/nano-meter range. Commercially, the 90nm technology node is already in production and the industry is expected to move on to the 65nm node very soon. In consonance with this trend, the cut-off frequency (f_t) of operation of the MOSFETs has also increased tremendously. This is attributed to the reduced transit time of injected electrons from the source to reach the drain due to reduced channel length, which also gives rise to very high drain fields leading to velocity saturation of carriers. Apart from favoring high-speed digital design applications, this has served as a boon for the RF IC design community, for it has enhanced the prospects of RF design using bulk-CMOS technology [1, 2]. Complete RF circuits and systems implemented with CMOS technology, operating at frequencies up to several Giga Hertz have already been reported [3]. Bulk Silicon CMOS technology is even viewed as a strong contender for emerging wireless millimeter wave applications [4-5].

The requirements of RF design have laid more stress on compact and accurate modeling of circuit elements to increase the capabilities of current RF circuit simulators. The challenges in MOSFET modeling are greatly enhanced with advancing technology as one needs to consider more complex physical issues (quantum effects, poly depletion, stress induced leakage etc) for smaller transistors. Further, the high frequency behavior of a device is significantly affected by all these physical effects and related parasitic. In

order to understand and accurately model the RF behavior of the MOSFET, a comprehensive electrical characterization of the device is indispensable.

1.1 Motivation

The motive behind this work is to find a reliable and cost-effective way to achieve the complete characterization of the MOSFET in the three-port form, extract its terminal charges as a function both bias and frequency and thus facilitate its large-signal modeling for RF applications. The lack of reliable multi-port characterization tools for active devices further fueled the need to provide a solution using conventional two-port measurement techniques. This in turn required the development of a generic small-signal RF MOSFET model and suitable techniques for its parameter extraction. In the following sub-sections, the inadequacies and problems faced in current RF modeling as well as measurement and characterization of the MOSFET are discussed. The next section elucidates some of the problems in today's high frequency MOS models.

1.2 Challenges in MOSFET modeling for RF IC design

The success of RF design depends heavily on the accuracy of circuit simulation tools. This requires efficient and compact models for the active and passive circuit elements. As the MOS transistor is the most important circuit element, a lot of effort has been undertaken to accurately model its DC and AC behavior. The BSIM, EKV and Philips compact models for the MOSFETs are widely used in the industry. Of these, the BSIM model is being regarded as the industry standard. Though these models are very good for predicting DC and lower frequency AC behavior, there are issues in the RF regime of device operation. Especially when one approaches the device cut-off frequency, the non-

quasi-static (NQS) effect becomes significant and the models are not accurate, as they fail to take into account the frequency dependence of the channel charge [6]. The computed terminal charges are thus in error at high frequencies.

The NQS effect has been attributed to the inability of the channel carriers to immediately respond to the applied terminal signal on account of their inertia. This results in temporary storage of transient charge in the channel. The NQS effect is more pronounced in longer channel transistors. They can be analyzed by dividing the channel into multiple small quasi-static sub-sections. As the device channel length comes down, the NQS effect is visible only at higher frequencies. The onset frequency of the non-quasi-static effect is given by [6, 7],

$$2\pi f_{NQS} = n2\pi f_t = n\frac{\mu_{eff}\left(V_G - V_T\right)}{L_{eff}^2}. \qquad (1.1)$$

In (1.1), f_{NQS} is the onset frequency of the NQS effect, f_t is the device cut-off frequency and n is a small fraction chosen to be much less than unity for good simulation accuracy. Current industry models are all Quasi-static implementations and they are valid only up to a third of f_t. The BSIM4 model [8] provides a charge-deficit NQS model for AC and transient simulations using an Elmore equivalent circuit to model channel charge build-up. The relaxation time depends on the intrinsic input resistance of the channel [9-12]. But this results in complex expressions for trans-conductance and trans-capacitances that are not physically correct. This may affect model scalability.

Further, in smaller devices, device parasitic like junction, overlap and fringing capacitances and conductance – all of which show frequency dependence - become increasingly important. The substrate itself introduces some frequency dependence

through signal coupling as will be discussed in the next section. This implies that the terminal capacitances and conductance and thus the charges themselves are bound to be frequency dependent.

A major issue in today's bulk MOS models is in the treatment of the substrate. The substrate in bulk MOS devices plays a significant role in determining the RF performance of a device. Some of the models like BSIM4 take a sub-circuit approach to include effects of the substrate network [8]. Various techniques for substrate network modeling have also been reported in the literature [13-15]. But, this sub-circuit approach makes the resulting RF model non-scalable in nature. A scalable substrate model has been reported in [16] but is valid only up to 10GHz.

To overcome these limitations, a more holistic description of the device is required, which gives an insight into the actual behavior of the substrate and also the bias and frequency dependence of all its terminal capacitances, conductance and charges. The next section presents the conventional incomplete MOS description in its two-port form and brings out the need for a three-port characterization.

1.3 The need for three-port characterization of a MOSFET

The MOS transistor is essentially a four-terminal device. However MOSFET modeling in the RF regime has been guided by the data collected by treating it as a three-terminal device. This means only a two-port characterization and analysis of the device is attempted [11-25], where the source is shorted to the substrate (bulk) to serve as the common terminal. Such an approach gives an incomplete description of the device. The effect of the substrate terminal on the device operation is unaccounted. This is because

charges induced in the substrate terminal are in turn coupled to other terminals and the signal coupling gets more significant at high frequencies.

In a conventional two-port characterization the small-signal current at the source and substrate terminals cannot be isolated from each other because the two terminals are tied together during measurement. Two-port characterization makes it impossible to predict the individual source and substrate terminal small-signal currents. But in reality, the source and substrate currents are distinctly different. And in many practical cases, the Source and Bulk terminals of the MOSFET are not tied together and both AC and DC potentials do exist between them. This means that signals and charges induced on the two terminals are different, e.g. - in a cascode amplifier stage, the Source and Bulk terminals of the MOSFET in common-source configuration are at different potentials. Only a three-port characterization yields each terminal small-signal current of the device distinctly, thus enabling accurate modeling and circuit simulation.

Thus, a complete three-port characterization of the MOSFET is essential for modeling the substrate effects at RF. The next section explores the various means to achieve RF characterization in general. It brings out the relative merits of two-port measurements as against multi-port measurements at RF.

1.4 Issues in RF characterization

Device characterization using direct admittance (Y) or impedance (Z) measurements requires ideal short and open conditions. Such conditions are difficult to achieve at higher frequencies and, open and short ports affect device stability at high frequencies. S-parameter measurements, carried when the ports are terminated in the characteristic impedances are most accurate and reliable at RF and microwave frequencies. Once the S-

parameter data is available, it can be converted to Y, Z or H parameters using simple matrix manipulation, for ease of analysis and parameter extraction.

1.4.1 Multi-port vector network analyzers

The RF characterization of MOS devices is best done using a Vector Network Analyzer (VNA) as it employs direct S-parameter measurements. The aim of this work is to achieve a three-port characterization of the MOSFET. It may seem that a multi-port VNA can offer a solution to this requirement. However, a Pure-mode Multi-port VNA still remains a research concept and is yet to be made commercially available. This is because of the challenge involved in maintaining the signals perfectly aligned to the reference planes (probe tips).

Mixed-mode multi-port VNA are commercially available today. But they have some serious disadvantages [26]. In such an instrument, a four-port network is treated as a two-port network with two modes per port, namely, differential and common modes [27, 28]. Sub-matrices have to be generated for each combination of these modes with stimulus and response signals. The differential sub-matrix is itself evaluated mathematically from single-ended measurements (A single port is excited at a time.), subject to superposition principle. Thus, it requires that the DUT must be linear for accurate computation of the mixed-mode terms.

In case of a purely differential measurement, it is very difficult to get exactly matched (common-mode) or opposite phase (differential) signals. One requires additional equipments like ‘baluns’ to achieve the phase requirements. Even these, are not very accurate and can introduce phase changes. A slight phase mismatch results in mode conversions and Electro-Magnetic Interference (EMI) related problems. The choice of

probes is very important to prevent signal coupling or cross-talks. To ensure proper isolation of RF signals, the multi-port measurement requires very complex probes like GSSG (Ground-Signal-Signal-Ground) and GSGSG (Ground-Signal-Ground-Signal-Ground), which are much more expensive when compared to normal GSG (Ground-Signal-Ground) probes required for two-port measurements.

The calibration of a four-port Network Analyzer is a very tedious process. It has to be done using multiple two-port calibrations. Some methods require short, open and load measurements at each port and all combinations of ideal thru connect [26, 27]. Thus, the required Impedance Standard Substrate (ISS) is quite complex and expensive. The calibration procedure itself is not yet standardized for on-wafer measurements. The reliability of the multi-port calibration is still a subject of investigation. There are no standardized four-port calibration tool-kits available as yet in the market. Further, techniques for multi-port de-embedding of on-wafer parasitic are still being developed and remain a research topic in itself. As the de-embedding techniques are not yet standardized, designing a suitable set of dummy test structures to characterize the parasitic also needs to be investigated. Without complete de-embedding of on-wafer parasitic, the multi-port characterization data is not expected to be meaningful.

1.4.2 Two-port vector network analyzers

The two-port VNA is much simpler and efficient to use than its multi-port counterpart. It is also the least expensive of them all. The two-port calibration techniques are quite well established and standardized – TRL (Thru-Reflect-Line), LRM (Load-Reflect-Match), SOLT (Short-Open-Load-Thru) and LRRM (Load-Reflect-Reflect-Match), to name a few. There are several software tools like WinCal and Nucleus dedicated to two-

port calibration. Signal isolation is not a problem, and the probes (GSG) required are also simpler and cheaper. Considering all the problems in a Multi-port VNA, it can be concluded that two-port VNA measurements are much easier to perform and are more reliable when compared with multi-port measurements. Therefore, carrying out two-port measurements in different permutations and appropriately relating them to the three-port parameters is an excellent option to explore for multi-port characterization.

1.5 Scope of the work

This work evolves a method to obtain the complete three-port characterization of the MOS transistor valid in all regions of operation, up to about 15GHz, with the help of simple two-port RF measurements to overcome issues mentioned in Section 1.4. The method and the techniques presented here are quite generic and can be useful even for millimeter wave applications provided a valid equivalent circuit representation is available. The new test structure (SD-R) developed for this work directly yields the MOSFET junction admittances at all biases and frequencies, which can be used for RF modeling of junction and substrate behavior. The measured three-port terminal capacitances as functions of bias and frequency are presented here for the first time. The terminal charge extraction method presented here is quite efficient and general. All four MOSFET terminal charges obtained as functions of bias and frequency from measured three-port data are reported here for the first time. They are extremely useful for large–signal device modeling and circuit simulations. The many modeling problems presented in Section 1.2 and 1.3 can be effectively addressed with the knowledge of these terminal charges. The next section provides a brief outline of the contents of this thesis.

1.6 An outline of this work

This chapter focused on the motivation and scope of this work along with some of the problems faced in RF modeling and characterization. Chapter 2 gives an overview of past work towards three-port characterization from two-port measurements. It elaborates the limitations of the existing methods. It brings out the practical problems reported in one of the latest papers [32], by a study of the non-ideal behavior of the GPG (Ground-Power-Ground) probe used at the un-calibrated third-port for bias feed, while carrying out two-port measurements. This chapter proceeds to develop the theoretical background required to realize three-port MOSFET characterization from two-port measurements. It provides a detailed description of the MOSFET Admittance Network theory and its application towards the characterization of the device. It also illustrates the three different two-port permutations to be used, along with their equivalent admittance matrix representations.

Chapter 3 and 4 provide a detailed solution to the problem posed by the GPG probe. Chapter 3 describes the measurement set-ups, device characterization and parasitic de-embedding procedures used. It proposes a new test structure (SD-R) to directly extract a set of model parameters, which are of special use in the MOSFET parameter extraction, employed for de-embedding the probe's impedance. It proceeds to explain the RF characterization of the GPG probe using one-port S-parameter measurements, and the undesirable effect of the probe's impedance on two-port measurements of the MOSFET. It stresses the need for de-embedding the probe's impedance from the RF measurements.

Chapter 4 is dedicated towards the de-embedding of the probe impedance using RF MOSFET modeling and parameter extraction techniques for both on-state and off-state behavior of the device. The given method employs small-signal modeling techniques to

develop a general RF equivalent circuit for the MOSFET. Using the general RF equivalent circuit, this chapter demonstrates the use of the SD-R test structure through the extraction of some important physical parameters like junction admittances and the body-effect trans-conductance (which are also useful for RF modeling in general). The work presents a novel parameter extraction scheme, utilizing the physical parameters extracted from the SD-R device, to accurately de-embed the effect of the probe impedance at the un-calibrated third port, from the two-port data of the MOS device. It proceeds to describe the generation of the three-port Y-parameters and terminal capacitances from the corrected two-port data. The chapter concludes with a derivation of expressions for the terminal charges of the device using the three-port terminal capacitances.

Chapter 5 presents the two-dimensional device simulations carried out using TCAD simulators, to serve as a guideline to validate the three-port characterization data of the MOSFET, as well as to verify functionality of the SD-R device and its parameter extraction. It describes the process simulation of a 0.35μm NMOS device in CMOS technology using Synopsys TSUPREM-4 along with DC and RF simulations of the simulated NMOS structure in Synopsys Medici. It gives an overview of the process flow, development of the simulation mesh, adaptive re-grid procedures and the device models used in the simulations. It reports the junction capacitance and conductance of the device extracted from both simulations and measurements of the SD-R structure and verifies its functionality. It provides explanations for both the bias and frequency dependence of the extracted junction admittances.

Chapter 6 illustrates the consistency of the MOS parameter extraction scheme and validates the three-port characterization data by exhibiting the match of the redundant

admittances obtained from different two-port configurations after probe de-embedding. It also verifies the correctness of the extrinsic parameters, by comparing junction admittances extracted from both the normal device and SD-R structure measurements. It presents the three-port capacitances and trans-conductance obtained from measurements for the first time, along with capacitances obtained from simulations and discusses their overall trends. The work presents the NQS effect manifested as the increasing divergence between the gate-to-drain (g_m) and gate-to-source (g_{ms}) trans-conductance obtained from the three-port data for the first time. This chapter depicts the terminal charges of the MOSFET, extracted from its measured three-port capacitances, as functions of both bias and frequency for the first time. It also discusses the bias dependence of the charges using device physics. Chapter 7 presents the conclusions of this work. It also presents some suggestions for future enhancements of this work. The list of publications associated with this work is given in the next section.

1.7 List of publications

1. U. Mahalingam, S. C. Rustagi, and G. S. Samudra, "Three-Port RF Characterization of MOS Transistors," *65th Automated Radio Frequency Techniques Group* (*ARFTG*) *Conference Digest*, June 2005.
2. U. Mahalingam, S. C. Rustagi, and G. S. Samudra, "Direct Extraction of Substrate Network for RF MOSFET Modeling Using a Simple Test Structure," *IEEE Electron Device Letters*, vol. 27, no. 2, pp. 130-132, Feb. 2006.
3. U. Mahalingam, S. C. Rustagi and G. S. Samudra, "Frequency and Bias Dependent Terminal Charge Extraction for a MOSFET using Three-port RF Characterization", draft under preparation.

Chapter 2: Overview of Past Work and Network Theory

This chapter provides a brief study of the various methods developed for active device characterization. It analyzes the limitations of these works and proposes an effective solution to the problem faced in one of the latest reports in literature [32] on three-port MOSFET characterization. The latter portion of this chapter develops the theoretical background needed for the succeeding chapters on measurement and extraction. The general admittance theory of the MOSFET and its abstractions into different two-port configurations has been presented.

2.1 Prior work in MOSFET characterization

Several attempts to obtain a three-port RF characterization from two-port S-parameter measurements have been reported in the literature [29-32]. In one of the methods, the third port is terminated on-wafer with the characteristic impedance. Thus, the two-port S-parameters directly correspond to the elements of a three-by-three S-parameter matrix. The methods in [29-31] employ multiple test structures for the measurements. As device level variations can be significant, the accuracy of the characterization is affected by these variations. Further, de-embedding of shunt and series parasitic is very important at RF regime, and so the use of multiple structures may yield inaccurate data. Some of the methods are also very involved in their analysis. A serious disadvantage in such methods is that the terminating impedance interferes with the DC biasing of the device at the third port [29]. This approach is shown in Figure 2.1.

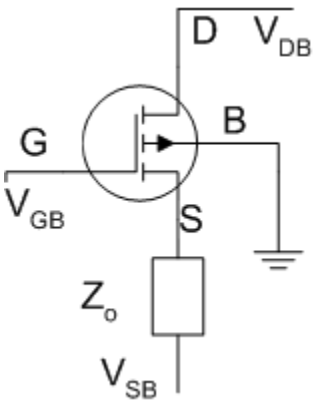


Figure 2. 1 On-wafer termination for two-port S-parameter measurements

Alternatively, to perform a similar experiment with Z-parameters, large impedance in the form of a series inductance is required at the third port probe-tip (so that the third port is practically "open-circuit"). Obtaining sufficiently large impedance to obtain ideal open-circuit conditions is again laced with practical difficulties.

Jha et al [32] had proposed a method to obtain three-port characterization of a MOSFET using two-port measurements in three different configurations of the device. The difference in this case is that, instead of terminating the third port with the characteristic impedance, an external AC short is attempted at the third port. Here, the correspondence to three-port characteristics is established via Y-parameters and not the S-parameters. The measured S-parameters are converted to two-port Y-parameters. The two-port Y-parameters obtained from the three different configurations are properly assembled to yield the three-port Y-parameters of the device. This method proposes a single test structure and thus avoids problems of device-level variation. For on-wafer measurements, a Ground-Power-Ground (GPG) probe is employed to provide the external AC short and the third port DC-feed. In the absence of terminating impedance

the biasing problems mentioned before are also avoided. A large on-probe capacitance serves to bring the AC short close to the probe-tip.

This method is valid only if the GPG probe provides an ideal AC ground at the third port. However, the GPG probe provides an AC short only at low frequencies (up to 1.1GHz as indicated by measurements on GPG probe, which will be discussed later). The probe is 'lossy' and also exhibits a strong inductive behavior at higher frequencies (see Chapter 3). So, the two-port Y-parameters obtained from S-parameter measurement do not correspond to the three-port parameters of the device. The work reported in [32] is valid only up to about 1.1GHz. Thus the effect of this non-ideal AC short, i.e. the probe impedance, must be properly de-embedded to get the correct three-port characteristics of the MOSFET at RF.

The behavior of the GPG probe and its detrimental effect on the device measurements is addressed in Chapter 3 and the probe de-embedding solution is formally evolved in Chapter 4, which paves the way for accurate three-port characterization of the MOSFET. The next section builds up the theoretical background for the MOS device description. The device is described by its admittance matrices in its complete form as well as, by the various two-port configurations in its partial forms. The relation between the three two-port forms and the larger matrix is brought out. The advantages of such a Y-parameter representation towards RF characterization are also clearly established.

2.2 MOS admittance network theory

Any *n*-port device (i.e. a device having '*n*+1' terminals) can be described completely by its corresponding *n*-port S, Y, H or Z parameters. As the MOSFET is a four terminal device, it is completely characterized by its three-port parameters. The different

parameter sets are inter-convertible using simple matrix manipulation techniques [33]. RF measurements using a Network Analyzer yield the S-parameters of the device. These are then converted to Y- or Z-parameters for ease of analysis and parameter extraction. The general 4x4 admittance matrix describes the complete device as given by (2.1).

$$\begin{bmatrix} i_g \\ i_d \\ i_s \\ i_b \end{bmatrix} = \begin{bmatrix} y_{gg} & y_{gd} & y_{gs} & y_{gb} \\ y_{dg} & y_{dd} & y_{ds} & y_{db} \\ y_{sg} & y_{sd} & y_{ss} & y_{sb} \\ y_{bg} & y_{bd} & y_{bs} & y_{bb} \end{bmatrix} \begin{bmatrix} v_g \\ v_d \\ v_s \\ v_b \end{bmatrix} \tag{2.1}$$

As explained earlier, this description covers the effect of the signal coupling to the bulk terminal as well as charges induced at all terminals due to applied DC potential. The well-known admittance conservation principle [7] states that the sum total of the row or column entries of an '*n*-by-*n*' admittance matrix of an *n*-port device, add up to zero. For example considering the first row elements of (2.1), we can conclude that,

$$y_{gg} + y_{gd} + y_{gs} + y_{gb} = 0\,. \tag{2.2}$$

This means that the complete 4x4 Y-matrix can be generated with the knowledge of any 9 of the 16 elements in (2.1). This can be achieved by taking one of the terminals as being common to all other terminals involved in the three-port description. It is convenient to take the bulk as the common terminal at AC ground (v_b=0). The MOSFET thus has three ports, namely, Gate-Bulk, Drain-Bulk and Source-Bulk. Thus we can eliminate the final row and column entries of the 4x4 Y-matrix and reduce the problem to a 3x3 Y-matrix as given in (2.3).

$$\begin{bmatrix} i_g \\ i_d \\ i_s \end{bmatrix} = \begin{bmatrix} y_{gg} & y_{gd} & y_{gs} \\ y_{dg} & y_{dd} & y_{ds} \\ y_{sg} & y_{sd} & y_{ss} \end{bmatrix} \begin{bmatrix} v_g \\ v_d \\ v_s \end{bmatrix} \tag{2.3}$$

The nine elements in (2.3) can be individually generated by three unique two-port configurations [32] in which the third-port is AC shorted. The GD configuration is the common-source configuration where the two RF ports are Gate-Bulk and Drain-Bulk while the Source is AC shorted to the Bulk (v_s=0) as shown in Figure 2.2. The bulk itself is always at AC ground, serving as the common terminal. The corresponding GD admittance matrix is given in (2.4).

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} y_{gg} & y_{gd} \\ y_{dg} & y_{dd} \end{bmatrix} \begin{bmatrix} v_g \\ v_d \end{bmatrix} \tag{2.4}$$

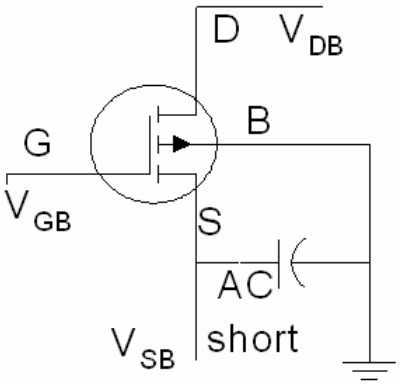


Figure 2. 2 GD configuration

The GS configuration is the common-drain configuration where the two RF ports are Gate-Bulk and Source-Bulk while the Drain is AC shorted to the Bulk (v_d=0) as shown in Figure 2.3. The corresponding admittance matrix is given in (2.5).

$$\begin{bmatrix} i_g \\ i_s \end{bmatrix} = \begin{bmatrix} y_{gg} & y_{gs} \\ y_{sg} & y_{ss} \end{bmatrix} \begin{bmatrix} v_g \\ v_s \end{bmatrix} \tag{2.5}$$

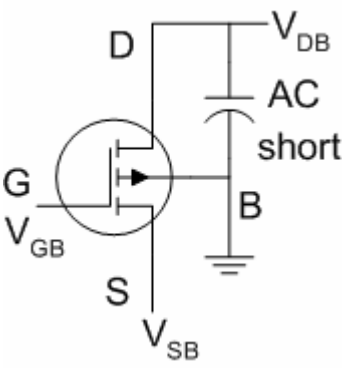


Figure 2. 3 GS configuration

Similarly, the SD (common-gate) configuration is defined, where the two RF ports are Gate-Bulk and Source-Bulk, while the Gate is AC shorted to the Bulk (v_g=0) as shown in Figure 2.4. The corresponding admittance matrix is given in (2.6).

$$\begin{bmatrix} i_s \\ i_d \end{bmatrix} = \begin{bmatrix} y_{ss} & y_{sd} \\ y_{ds} & y_{dd} \end{bmatrix} \begin{bmatrix} v_s \\ v_d \end{bmatrix} \tag{2.6}$$

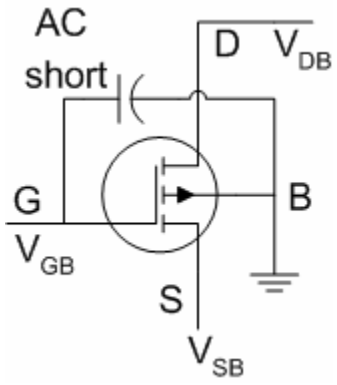


Figure 2. 4 SD configuration

The two-port matrices of (2.4)-(2.6) provide some redundancy as some of the elements are obtained from two different configurations. The next section examines the relevance of this redundancy in validating the device characterization, through an illustration.

2.2.1 Redundancy of the main diagonal elements

Figure 2.5 depicts a consolidated picture of the admittance matrix with contributions from the individual configurations also being highlighted. In the figure, the main diagonal elements of the upper 3x3 Y-matrix (excluding the common terminal elements), namely y_{gg}, y_{dd} and y_{ss}, are each obtained uniquely from two different measurement configurations. The y_{11} of GD and GS configurations yield y_{gg}, while y_{22} of GD and SD configurations yield y_{dd} of the device. Similarly, y_{22} of GS and y_{11} of SD both yield y_{ss}.

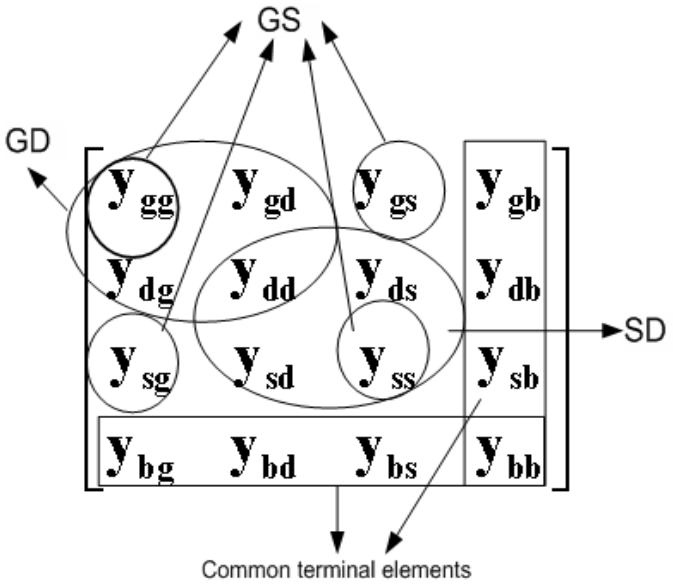


Figure 2. 5 Redundancy of main diagonal elements

As all three configurations are for the same device, any main diagonal element obtained from two different configurations should also be equal. Otherwise, the measured two-port Y parameters do not reflect the true characteristics of the device. Thus, such an agreement of the main diagonal elements serves to validate the entire three-port characterization. We will use this test to confirm the veracity of the three-port data obtained after probe de-embedding, in Chapter 6.

The two-port Y-parameters defined by (2.4)-(2.6) directly correspond to the entries in (2.3) and thus the three-port Y-parameters can be easily assembled from them. The S-parameter measurements for these two-port configurations are carried out by providing an external AC short at the third port at RF. These S-parameters do not enjoy a similar correspondence to the three-port S-parameter matrix of the MOSFET. So, they are not the actual two-port S-parameters of the device. To establish a similar correspondence between two-port S-parameters and the three-port S-parameters, one must terminate the third port of the above-mentioned two-port configurations with the characteristic impedance of the network (e.g. Z_o=50Ω). But, the practical difficulties like DC bias interference make this approach infeasible. However, the measured S-parameters are converted to Y-parameters, which are indeed the actual two-port Y-parameters of the device. So they directly map to the three-port Y-parameter matrix in (2.3). Thus we find that Y-parameters provide the easiest way to get the three-port characteristics of the MOSFET.

This completes the theoretical description of the MOS terminal admittances. The next chapter describes the new test structures, measurement setups and parasitic de-embedding methods used for the MOSFET characterization. It develops a method to characterize the GPG probe and identifies its significant degrading effect on device measurements at RF.

Chapter 3: Test Structures and Measurement

This chapter describes the measurement set-ups and device structures employed for the characterization. It introduces a novel test structure, named the SD-R device and highlights its utility towards physical parameter extraction for RF modeling. It presents a newly developed method for the characterization of the GPG probe and reports its measured RF behavior for the first time. It explains the two-step de-embedding of on-wafer parasitic from the measured data. It also proposes a new approach to eliminate the on-wafer parasitic at the third port. The chapter concludes with an account of the effect of the non-ideal short provided by the GPG probe at the third port, on the two-port device measurements. The effect of probes used at un-calibrated ports of a device, on measured data at RF, has been studied here for the first time.

3.1 Measurement Setup

A two-port Vector Network Analyzer (HP8510c VNA) and a DC source-measure unit (HP4142) were used for the measurements. The measurement system was controlled with the help of a 'UNIX' workstation through a standard GPIB (General Purpose Interface Bus). Two RF GSG (Ground-Signal-Ground) probes (CASCADE-Infinity probes) were used for the RF signal ports while a GPG (Ground-Power-Ground) probe (GGB Industries) was used at the third port to provide DC feed along-with an external AC-short. The RF signal was coupled with DC bias using appropriate Bias Tees (HP 11612B Bias Network). Though the DC source itself can provide the AC-short at the third port, the GPG probe actually helps to bring the short closer to the device through a large on-probe capacitance. This is very important because the third port is un-calibrated and the

cables leading to the DC source can insert significant parasitic impedance before being shorted inside the instrument. A Bias Tee is employed at the third port, whose RF-in terminal is terminated by the characteristic impedance of 50Ω and DC-in is connected to the HP4142. The IC-CAP software tool was used to transfer and store the measured data for future analysis.

3.1.1 A note on IC-CAP

The "Integrated Circuit-Characterization and Analysis Program" – IC-CAP is a state-of-the-art device modeling software from Agilent technologies. It provides powerful characterization and analysis capabilities for semiconductor modeling applications. This work has relied on IC-CAP's capabilities in data acquisition, simulation, and graphical analysis. The special Parameter Extraction Language (PEL) utility of IC-CAP has been extensively exploited in this work to construct efficient transforms (extraction programs) for direct parameter extractions at RF [34]. The huge amount of data generated from RF S-parameter measurements have been efficiently de-embedded and processed using these transforms to achieve the accurate three-port capacitance and conductance coefficients of the MOS device up to several GHz.

3.1.2 Calibration of the Vector Network Analyzer

The VNA ports were calibrated using the Load-Reflect-Reflect-Match (LRRM) technique [35] on the Impedance Standard Substrate (ISS). This requires a golden device for the short, load (50Ω) and thru conditions. The thru is a loss-less delay line with an electrical delay of 1ps for the GD configuration i.e. the normal scenario in which the two RF signal probes are oriented opposite to each other. For the GS and SD case, the RF

signal probes are oriented at right angles to each other, which require a special L-shaped thru line with electrical delay of 3ps. For the LRRM method, measuring load for one of the ports is sufficient. The open and short are measured for both the ports. The source power levels were set at -10dBm and noise tolerance for the calibration is set to within 0.05dB to ensure quality measurements at RF. The PC-based WinCal software [36], a two-port calibration tool-kit, was used for this purpose.

3.2 Device specifications

Enhancement type NMOS devices were fabricated in a local fabrication company, using standard 0.35 micron CMOS technology with single poly and four metal layers. Measurements were carried out on devices with three different channel lengths - 1μm, 0.5μm and 0.35μm respectively. Each device is comprised of 10 fingers of 10μm width each (total W=100μm). Figure 3.1 gives a simplistic view of the measured device's multi-finger architecture (the metal layers used to establish source and drain contacts are not shown here) with shared drain and source diffusion regions. Figure 3.1 shows that the measured ten-finger MOS device is comprised of two four-finger sections and one two-finger section with a focus to minimize the number of drain diffusions. In all, there are eight source diffusion regions and five drain diffusion regions. The gate of each the finger is contacted from both sides to reduce resistance [40].

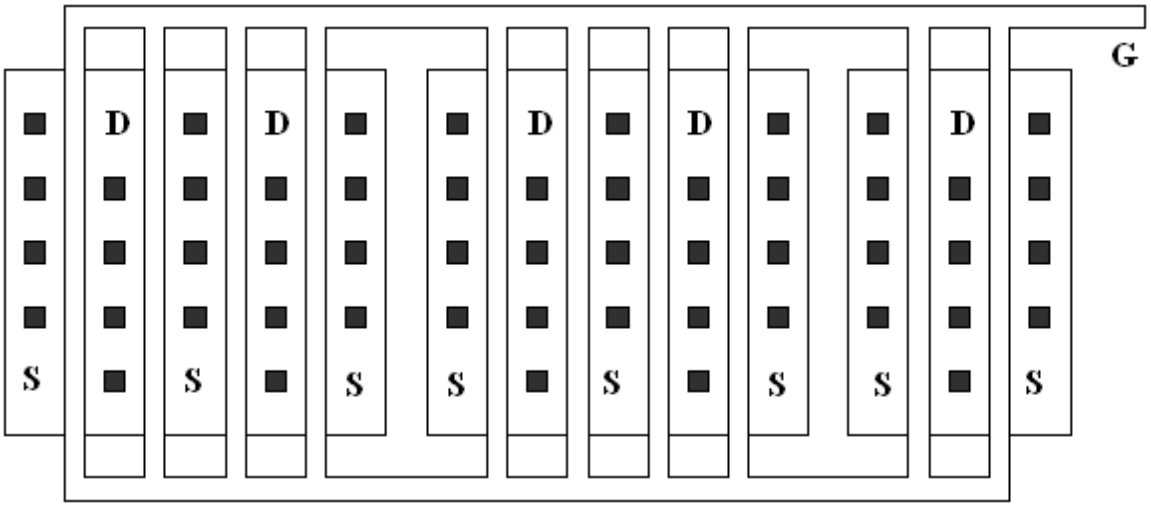


Figure 3. 1 Multi-finger architecture of the measured MOSFET

The measurements covered the entire operational range of the MOS devices with the terminal biases V_{GB}, V_{DB} and V_{SB} each ranging from 0V to 3.2V in steps of 0.2V (V_B=0) and the signal frequency ranging from a 100MHz to 25.1GHz in steps of 500MHz. It may be noted that the maximum acceptable potential at any terminal with respect to the source is 3.3V for the 0.35 micron technology. The two-port S-parameter measurements were repeated as above for the GD, GS and SD configurations.

3.2.1 The SD-R test structure

In addition to the normal devices mentioned in the previous section, a special device structure has been conceptualized to aid the RF parameter extraction of the MOSFET, to be elaborated in Chapter 4. This structure employs a huge resistance (R_G) of about 5kΩ at the Gate terminal of the MOS device. Other features of this device are exactly the same as those of a normal device. The measurements on this structure are carried out in the SD configuration alone. The purpose of the huge gate resistance is to kill any small-signal at the external Gate terminal (Figure 3.2). This enables us to directly extract the junction

admittances of the device in on-state (see Chapter 4). This structure will be henceforth referred to as the SD-R device. It should be noted that, as the gate DC current is negligibly small, the R_G does not in any way hamper the device biasing. Thus, the DC behavior of such a device is exactly the same as that of a normal device.

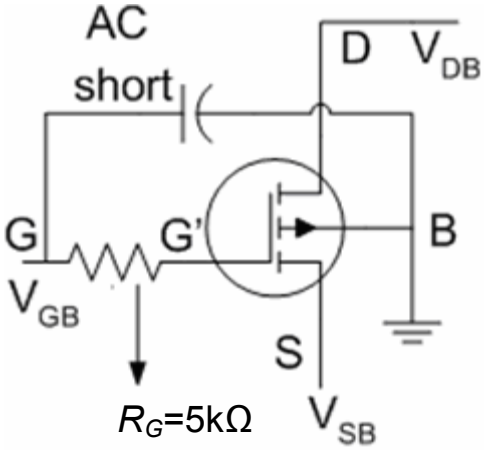


Figure 3. 2 SD-R test structure (in SD configuration)

3.3 The GPG probe

The GPG probe is used at the third port for DC bias feed and for providing the AC-short. The probe has a large mounted capacitance (120pF), which provides an ideal AC ground at low frequencies. A 1-port S-parameter characterization of the GPG probe was carried for frequencies 100MHz to 25.1GHz in steps of 500MHz. A GSG probe was used to measure the s_{11} of the GPG probe through a lossless 'thru' line (electrical delay=1ps). The GPG probe was terminated by 50Ω impedance through an RF cable and Bias-Tee (similar to experimental set-up for device measurement). The characterization set-up is shown in Figure 3.3.

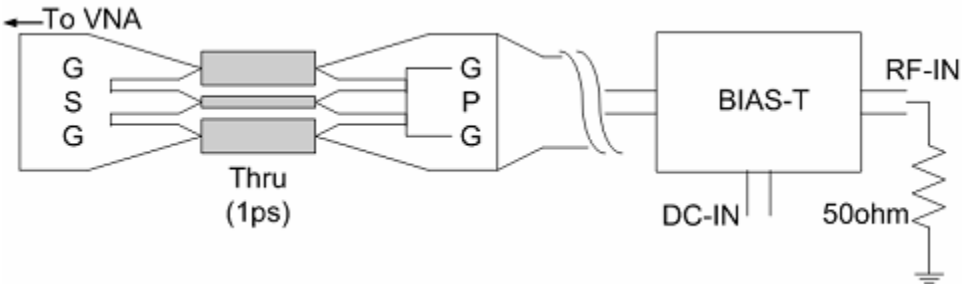


Figure 3. 3 GPG probe characterization

The measured s_{11} ($s_{MS.11}$) of the GPG probe is corrected for electrical delay (T_D=1ps) of the through line as given in (3.1).

$$s_{GPG.11} = s_{MS.11} * e^{j2\pi f(2T_D)} \tag{3.1}$$

The corrected s_{11} of the probe ($s_{GPG.11}$) is shown in Figure 3.4. As expected, the capacitive effect dominates at very low frequencies. But at higher frequencies, especially beyond 1.1GHz, the probe exhibits an increasing loss and significantly large inductive characteristic. The S-parameters are converted to 1-port Z-parameter as given in (3.2).

$$z_{GPG} = 50 * (1 + s_{GPG.11}) / (1 - s_{GPG.11}) \tag{3.2}$$

It is clear from Figure 3.4 that the GPG probe exhibits a non-ideal behavior and thus its effect must be completely removed from the two-port measurements of the MOSFET. The disparity produced by the GPG probe impedance on the measured Y-parameters is discussed in the following sections.

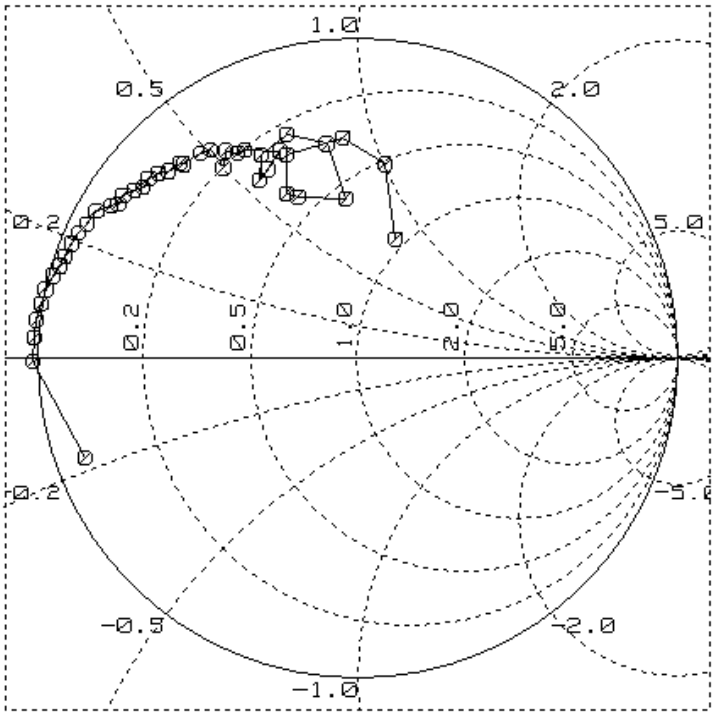


Figure 3. 4 s_{11} of the GPG probe ($s_{GPG.11}$)

3.4 Parasitic De-embedding of measured data

The conventional one-step de-embedding technique is not valid for frequencies beyond 10GHz as the serial parasitic of leading interconnects become significant [37]. The two-step de-embedding approach given in [37] is also not adequate as it makes a lumped approximation of the serial parasitic. To consider the distributed effects of the serial parasitic, the cascaded matrix approach presented in [38] is adopted after removing the pad parasitic. Dummy Test structures were laid out for the de-embedding of on-chip parasitic – both pad and interconnect. Figure 3.5 depicts the DUT with its pads and leading interconnects. The pad parasitic is a parallel component, which can be simply removed from the DUT Y-parameters. The interconnect exhibits a distributed behavior at RF which hinders the possibility of its separation into serial and parallel components. The

best way to handle them is to obtain their two-port characteristics separately and de-embed them from the DUT using the ABC-matrices [38].

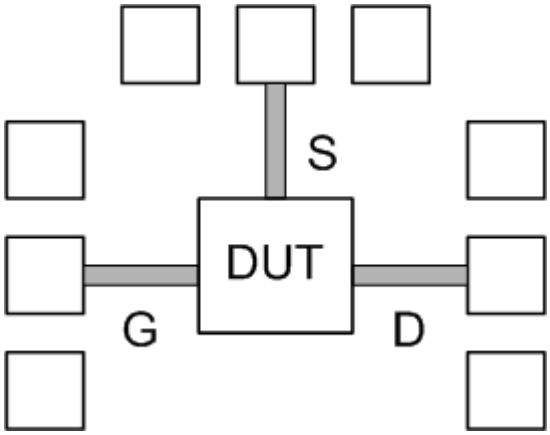


Figure 3. 5 The MOSFET test structure

Figure 3.6 shows the DUT with both its pad (y_{p1}, y_{p2} and y_{p3}) and interconnect (represented by ABC matrices A_G and A_D) parasitic components considering only the two RF signal ports at a time.

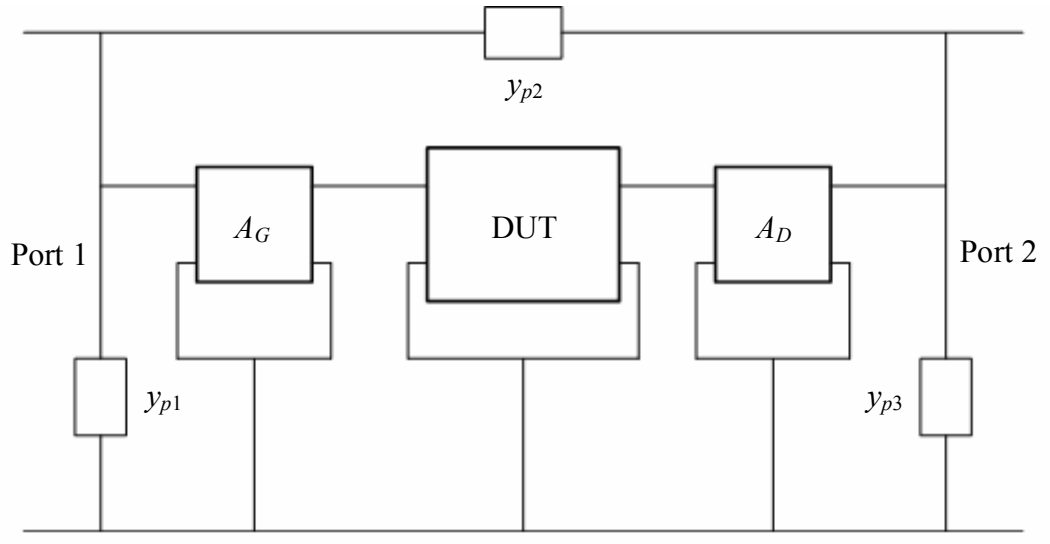


Figure 3. 6 Two-port parasitic representation for the MOSFET in GD configuration

The parasitic associated with the un-calibrated third port is combined with the GPG probe impedance and removed together. The third port parasitic de-embedding is considered in detail in Section 3.4.1.

A dummy containing only the pads was measured to get the parallel parasitic in each two-port configuration. Figure 3.7 depicts the two-port equivalent parasitic admittance elements (y_{p1}, y_{p2} and y_{p3}) representing the pads. The measured two-port S-parameters are converted to Y–parameters. The open parasitic is given by,

$$Y_{OPEN} = \begin{bmatrix} y_{OPEN.11} & y_{OPEN.12} \\ y_{OPEN.21} & y_{OPEN.22} \end{bmatrix} = \begin{bmatrix} y_{p1} + y_{p2} & -y_{p2} \\ -y_{p2} & y_{p2} + y_{p3} \end{bmatrix}. \tag{3.3}$$

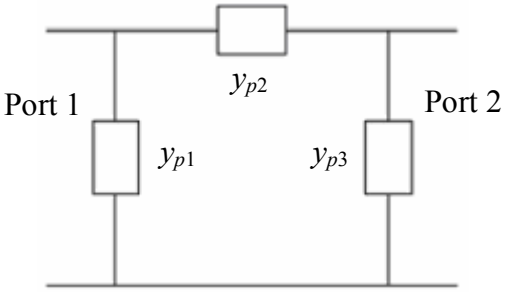


Figure 3. 7 Two-port equivalent parasitic representation of the pads

The measured S-parameters of the MOSFET are converted to Y-parameters ($Y_{DUT,\ MS}$) and the pad parasitic is first removed. This yields the pad de-embedded Y-parameters ($Y_{MS\text{-}PD}$) of the structure.

$$Y_{MS-PD} = Y_{DUT,MS} - Y_{OPEN} \tag{3.4}$$

Considering the Common-Source two-port configuration for the DUT in Figure 3.5 and discounting the gate and drain pads, we are now left with the Gate-side leading interconnect followed by the actual DUT and the Drain-side leading interconnect – all

three in a serially cascaded form. The ABC-matrix by virtue of its mathematical property is best-suited to describe such a chain of two-ports [38]. Thus, we have,

$$A_{MS-PD} = A_G * A_{DUT} * A_D , \tag{3.5}$$

In (3.5), the two-port ABC-matrices denote the pad de-embedded characteristics (A_{MS-PD}), the gate interconnect (A_G), the actual device (A_{DUT}) and the drain interconnect (A_D) respectively.

Each of the leading interconnects was laid out as a 'thru' set-up and measured in two-port form. Figure 3.8 shows the 'thru' setup of the Gate terminal lead interconnect and the corresponding parasitic. It should be noted that this dummy as such includes the pad parasitic also. A pad dummy similar in geometry to the dummy shown in Figure 3.8, without interconnect, is first measured. Its S-parameters are converted to Y-parameters (Y_{OPEN}). The measured interconnect dummy S-parameters are also converted to Y-parameters ($Y_{INTERCON,\ MS}$) and de-embedded of the pad parasitic (Y_{OPEN}), before being converted to ABC-parameters. The A_G so obtained is given in (3.6).

$$A_G = A\left[Y_{INTERCON,\,MS} - Y_{OPEN} \right] \tag{3.6}$$

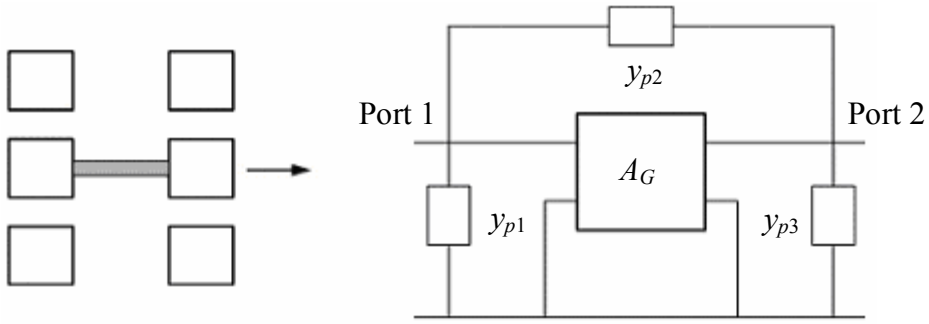


Figure 3. 8 Lead interconnect dummy and its equivalent parasitic representation

Similarly, we obtain A_D and A_S for the drain and source leading interconnects. Through simple matrix manipulations like post multiplication and pre-multiplication by the inverse of the respective interconnect ABC matrices, we obtain the accurate DUT characteristics, which are converted back to Y-parameters for analysis.

$$A_{DUT} = A_G^{-1} * A_{MS-PD} * A_D^{-1} \tag{3.7}$$

$$Y_{DUT} = Y\left[A_{DUT}\right] \tag{3.8}$$

Similarly, for the GS and SD configurations, the respective interconnects are removed using the cascading ABC matrices after de-embedding the pad parasitic.

But it must be re-emphasized that the pad and series parasitic at the third port are still left to be de-embedded from the measured two-port data. The next section demonstrates a new approach to eliminate the third port parasitic.

3.4.1 Eliminating the third port parasitic

The best way to eliminate the parasitic at the third port is to combine them with the larger parasitic impedance of the GPG probe and remove them together. Figure 3.9 shows the third port parasitic along with the probe impedance for the GD configuration of the MOSFET. Here the gate-bulk and drain-bulk ports have been de-embedded of their parasitic as mentioned in the previous section. Looking into the parasitic and probe impedance network at the source terminal of the MOSFET, we define the total impedance at the third port as "z_{probe}", for ease of understanding and analysis. This impedance is calculated using the reflection co-efficient of the parasitic network as explained next. It must be mentioned here that none of the earlier works on two-port measurements reported in literature so far, have succeeded in completely eliminating the parallel and

series parasitic at the un-calibrated third port of the device. The approach presented here is quite general and can be used for parasitic removal at un-calibrated ports for other RF applications as well.

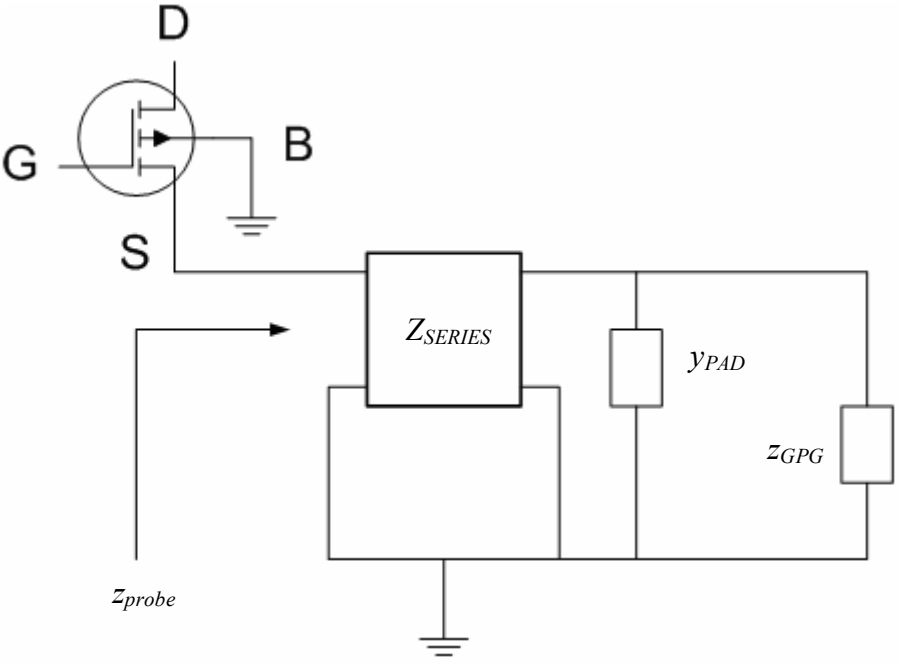


Figure 3. 9 Third port parasitic (GD configuration)

First, the shunting pad admittance at the third port is calculated from the pad dummy measurements. For example, to find the parasitic associated with the source pad (represented as y_{PAD} in Figure 3.9), two-port measurements of the pad dummy (Y_{OPEN}) carried out in the SD configuration (defined with respect to device orientation on the wafer) can be used. Considering the equivalent circuit representation of the pad parasitic provided in Figure 3.7, the source pad parasitic would be given by y_{p1}. This can be directly obtained from the measured Y_{OPEN} using the relation specified in (3.3), as given here in (3.9).

$$y_{PAD} = y_{OPEN.11} + y_{OPEN.12} = y_{p1} \tag{3.9}$$

For convenience of analysis here, the impedance of the GPG probe and the pad are combined together and denoted as z_P.

$$z_P = (z_{GPG}{}^{-1} + y_{PAD})^{-1} \tag{3.10}$$

The reflection co-efficient ρ_p of this network with the characteristic impedance Zo=50Ω, is defined as,

$$\rho_P = \frac{z_P - 50}{z_P + 50}. \tag{3.11}$$

The Z_{SERIES} of the third port inter-connect parasitic is a two-port matrix. It is therefore converted to the corresponding S-parameters (S_{int}).

$$S_{\text{int}} = S[Z_{SERIES}] = \begin{bmatrix} s_{\text{int}.11} & s_{\text{int}.12} \\ s_{\text{int}.21} & s_{\text{int}.22} \end{bmatrix} \tag{3.12}$$

The reflection co-efficient of the combined network ρ_{probe} is obtained as given in [33].

$$\rho_{probe} = s_{\text{int}.11} + \frac{s_{\text{int}.12} s_{\text{int}.21} \rho_P}{1 - s_{\text{int}.22} \rho_P} \tag{3.13}$$

The reflection co-efficient is converted into the effective impedance looking into the network i.e. z_{probe} as given in (3.14).

$$z_{probe} = 50 \frac{(1 + \rho_{probe})}{(1 - \rho_{probe})} \tag{3.14}$$

This impedance must be removed to get the ideal two-port characteristics of the device in each configuration. The next section shows the effect of this probe impedance on actual device measurements.

3.5 Effect of the GPG probe on device measurements

The probe impedance at the third port has a significant effect on the two-port device measurements at RF. The effect of the GPG probe on RF device measurements has not been reported in literature. This is because most of the works on two-port RF characterization [11-25] use a MOSFET with the source and bulk nodes tied together. This makes it impossible to give any DC biasing between the source and bulk nodes and thus the works do not require a GPG probe for the measurements. In [32], a GPG probe has been used for the measurements but only low frequency data (up to 1.1GHz) was reported. This work concentrates on the RF regime and thus has identified the significant problem posed by the GPG probe. In this section, we report the undesirable effects of this probe (used at the un-calibrated third port for biasing) on the measured two-port admittances of the MOSFET. The MOSFET admittance network theory is applied to the measurements here to clearly gauge the magnitude of the problem.

In Section 2.2 of Chapter 2, the redundancy of the main diagonal elements of the three-port admittance matrix was discussed. Accordingly, one expects the y_{gg} obtained as y_{11} from the GD configuration to match with the y_{gg} obtained as y_{11} from the GS configuration as they are obtained from the same device. A similar match is expected for y_{dd} (GD and SD) and y_{ss} (GS and SD) respectively. But the measured y_{gg}, de-embedded of the two-port parasitic, shows a significant variance that increases with frequency. Figures 3.10 and 3.11 show the real and imaginary parts respectively of the measured y_{gg} from the GD and GS configurations as a function of frequency for a 0.35μm device at V_{GS}=3V, V_{DS}=3.2V and V_{SB}=0V.

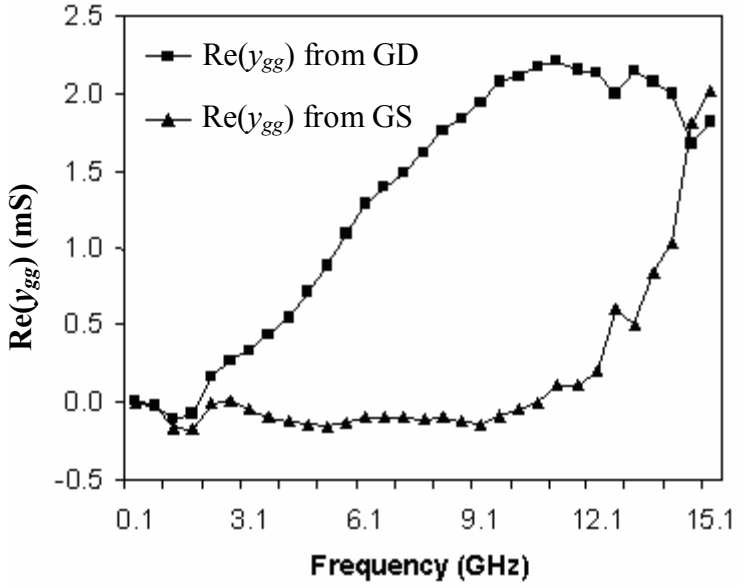


Figure 3. 10 Effect of GPG probe on real part of y_{gg}

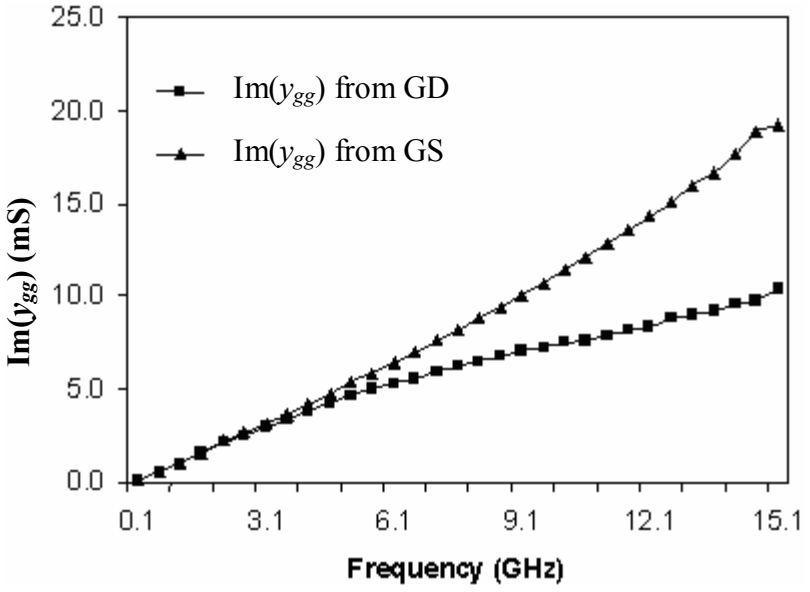


Figure 3. 11 Effect of GPG probe on imaginary part of y_{gg}

As seen from the plots, the error in Re(y_{gg}) grows to more than 100% at just 3GHz, while the error in the Im(y_{gg}) grows to more than 70% at 10GHz. Significant variations have been observed even in the measured y_{dd} and y_{ss}. Similar variations have also been observed in measurements from 1µm and 0.5µm devices. This shows that the data does not represent the actual two-port Y-parameters of the device and thus does not correspond to the three-port admittance matrix. We have identified here, that the large error is primarily due to the probe impedance (Figure 3.4) at the third-port, which is violating the AC short conditions mandatory for obtaining the two-port Y-parameters. The third port pad and interconnect parasitic also adds to the undesired impedance. The probe impedance has been combined with the third port parasitic to ease the analysis (refer Section 3.4.1).

The removal of this probe and parasitic impedance from the measured data is very important for the three-port RF characterization, as it enables us to obtain the correct two-port Y-parameters. The treatment of this parasitic-probe impedance and the subsequent generation of accurate three-port data are taken up in detail in Chapter 4.

3.6 Summary

The two-port S-parameter measurements are carried out on the SD-R (SD configuration only) and normal MOS device (GD, GS and SD configurations) for all biases and frequencies of interest using a Vector Network Analyzer. The GPG probe used at the third port to provide AC-short along with DC feed is also characterized by 1-port S-parameter measurements up to 25.1GHz. The non-ideal behavior (high frequency loss and inductive nature) of the probe is examined. The device measurements are subjected to a two-step de-embedding procedure to eliminate shunt and distributed serial parasitic.

The common admittance elements drawn from different two-port configurations, which should be equal (redundancy of main diagonal elements in the 3x3 Y-matrix), are compared and a substantial difference is observed at frequencies beyond 3GHz. The growing mismatch in the admittances with increasing frequency is rightly attributed to the non-ideal behavior of the probe. The need for de-embedding the probe's effect to obtain correct three-port characterization of the MOSFET is discussed.

Chapter 4: De-embedding of the GPG Probe Impedance

This chapter describes the newly developed method to remove the impedance of the GPG probe used in this work to provide the DC bias at the third port. The approach is to develop a general RF equivalent circuit model for the MOS device, which can be used to analyze any of the two-port configurations described in Chapter 2. The RF small-signal circuit model developed here is very generic and incorporates all extrinsic elements along with the intrinsic MOS model parameters. The next step is to derive expressions for the terminal admittances of the different two-port configurations. The equivalent circuit analysis and parameter extraction of the SD-R device are reported, which aid in accurate extraction of the equivalent circuit model parameters in each of the two-port configurations of the normal device. The de-embedding of the GPG probe and reconstruction of the measured data from the extracted parameters, follow suit. The three-port data is also assembled from these corrected two-port measurements. The parameter extraction of the device in the off-state (at V_{GS}=0) has been carried out using appropriate equivalent circuits to obtain the extrinsic MOS parameters like junction, overlap and fringing admittances. The novel parameter extraction routines presented here for the SD-R structure as well as for the normal device are extremely useful for RF MOSFET modeling.

The technique of obtaining terminal charges of the MOSFET using the three-port terminal admittances is also described at the end of this chapter.

4.1 Equivalent circuit representation of the MOS device

A generalized RF small-signal equivalent circuit model has been conceived for the MOSFET to facilitate the accurate de-embedding of the probe impedance at the third port. The circuit model shown in Figure 4.1 is based on the general admittance model given in [7]. While the model in [7] describes the intrinsic MOS device behavior, the new model developed here includes the extrinsic elements of the real device as well. The extrinsic elements constitute the bulk-source and bulk-drain junction admittances, the gate-drain and gate-source overlap and fringing admittances, the source-drain fringing admittance, the gate-bulk admittance and the gate, source and drain series resistances.

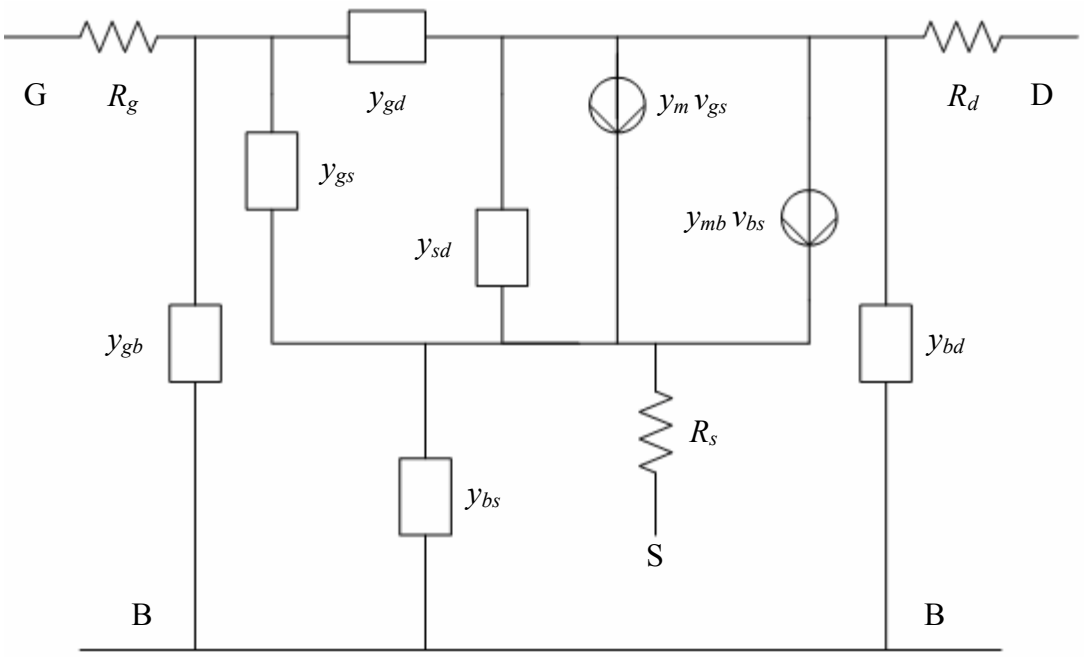


Figure 4. 1 RF Equivalent circuit model for the MOS device

4.1.1 Interpreting the equivalent circuit model parameters

The equivalent circuit model developed here is very generic and it includes both intrinsic and extrinsic components of the MOS device admittances. The following method is adopted in the definition and nomenclature of the admittance elements:

A subscript "i" after the element name denotes an intrinsic MOS admittance parameter. In general all the intrinsic MOS admittances are non-reciprocal in nature.

$$y_{jk} \neq y_{kj} \forall j \neq k \tag{4.1}$$

The definition of the intrinsic admittances follows the general rules adopted in literature [7], which is given in (4.2).

$$y_{jk} = \left.\frac{\partial i_j}{\partial v_k}\right| v_l = 0 \forall l \neq k \rightarrow j,k \in \{d,g,s,b\} \tag{4.2}$$

In (4.2), *d*, *g*, *s* and *b* denote the drain, gate, source and bulk terminals of the transistor respectively.

Thus, the order of literals in the subscripts of intrinsic element names is very important. A subscript "e" after the element name denotes an extrinsic MOS admittance parameter. The extrinsic admittance components are reciprocal and thus the ordering is not important. However, for simplicity the extrinsic parameter adopts the subscripts used for the corresponding intrinsic parameter with which it is associated. A description of the various equivalent circuit model parameters is given below.

$$y_m = y_{dgi} - y_{gdi} \tag{4.3}$$

$$y_{mb} = y_{dbi} - y_{bdi} \tag{4.4}$$

$$y_{gd} = y_{gde} + (-y_{gdi}) \tag{4.5}$$

$$y_{gs} = y_{gse} + (-y_{gsi}) \tag{4.6}$$

$$y_{sd} = y_{sde} + (-y_{sdi}) \tag{4.7}$$

$$y_{bd} = y_{bde} + (-y_{bdi}) \tag{4.8}$$

$$y_{bs} = y_{bse} + (-y_{bsi}) \tag{4.9}$$

$$y_{gb} = y_{gbe} + (-y_{gbi}) \tag{4.10}$$

In (4.3)-(4.10), y_m is the gate-drain trans-admittance controlled by the gate-source small-signal voltage (v_{gs}); y_{mb} is the bulk-drain trans-admittance controlled by the bulk-source small-signal voltage (v_{bs}); y_{gde} and y_{gse} are the gate-drain and gate-source overlap-cum-external fringing [39] admittances respectively; y_{sde} is the source-drain extrinsic fringing admittance; y_{bde} and y_{bse} are the drain and source junction admittances; and y_{gbe} is the extrinsic gate-bulk admittance.

The extrinsic source, drain and gate series resistances were calculated from the process parameters following [40]. As the gate of the MOSFETs that are discussed in this dissertation is contacted from both sides, this resistance is computed as given in (4.11).

$$R_g = R_{gsh} \frac{W_f}{12 L_f N_f} \tag{4.11}$$

In (4.11), R_{gsh} is the sheet resistance of the gate poly in Ω/square, W_f is the width of each finger in μm, L_f is the gate length of the device in μm and N_f is the number of fingers.

For the calculation of source and drain resistance, we assume the device to be symmetric. This implies that, the source and drain resistances are equal and are obtained as given in (4.12).

$$R_s = R_d = \frac{R_{dsw}}{2W_f N_f} \tag{4.12}$$

In (4.12), R_{dsw} is the drain-to-source resistance in Ω-μm. R_{dsw} is available as a standard large signal model parameter, e.g. for BSIM3/4 models. The sheet resistance (R_{gsh}) of the gate poly material is available from the electrical process (EP) parameters.

The next section describes the RF equivalent circuit representation of the SD-R device and its parameter extraction scheme.

4.2 Equivalent circuit representation of the SD-R device

The RF small-signal equivalent circuit for the SD-R device in the SD configuration is shown in Figure 4.2(a). In the SD configuration, the RF signal is applied to the source-bulk and drain-bulk ports. As explained in Chapter 3, this device has a huge resistance (R_G=5kΩ) at its gate (G'). The external gate node (G) of the device is connected to the bulk (B) through the GPG probe. Here, the huge external gate resistance (R_G) and the probe impedance (z_{probe}) dominate the comparatively much smaller R_g which is in series with R_G and z_{probe}.

$$R_g + R_G + z_{probe} \approx R_G + z_{probe} \tag{4.13}$$

Further, when the MOSFET is in the "on-state", the gate-bulk admittance is negligibly small, i.e. $y_{gb} \approx 0$ when $V_{GS} > V_{th}$ [7, 39]. So, the combined admittance of these elements at the bulk terminal is also negligibly small ($y_{gp} \approx 0$ as shown in Figure 4.2(a)). It then follows that there is no direct path for AC signal leakage from the actual MOSFET gate node (G') to the bulk (B). The AC signal at G' can reach the bulk only by signal coupling via the drain or source terminals. This considerably simplifies the small-signal analysis of the circuit as shown in Figure 4.2(b) and directly yields three very important small-signal

parameters of the general MOSFET equivalent circuit. The body-effect trans-admittance parameter (y_{mb}), the bulk-drain admittance (y_{bd}) and the bulk-source admittance (y_{bs}) are obtained for all regions of operation of the device.

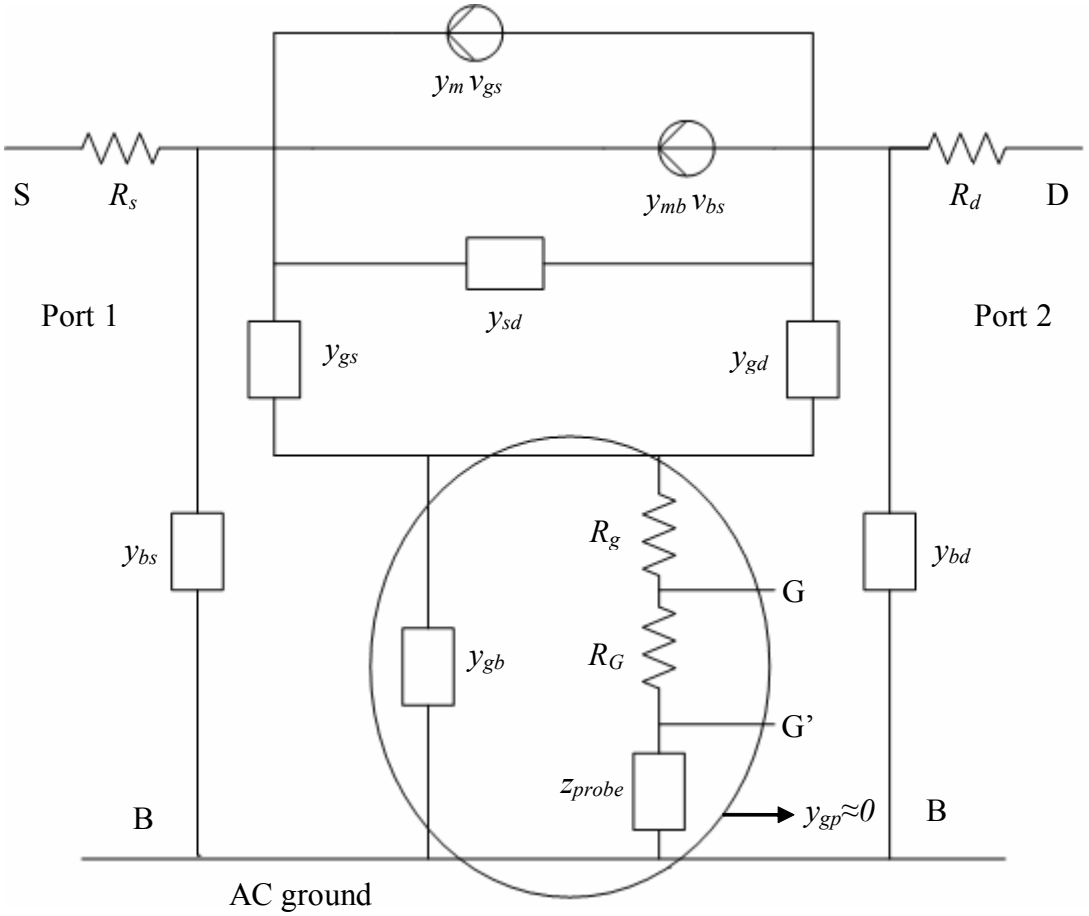


Figure 4. 2(a) RF Equivalent circuit of the SD-R device (SD configuration)

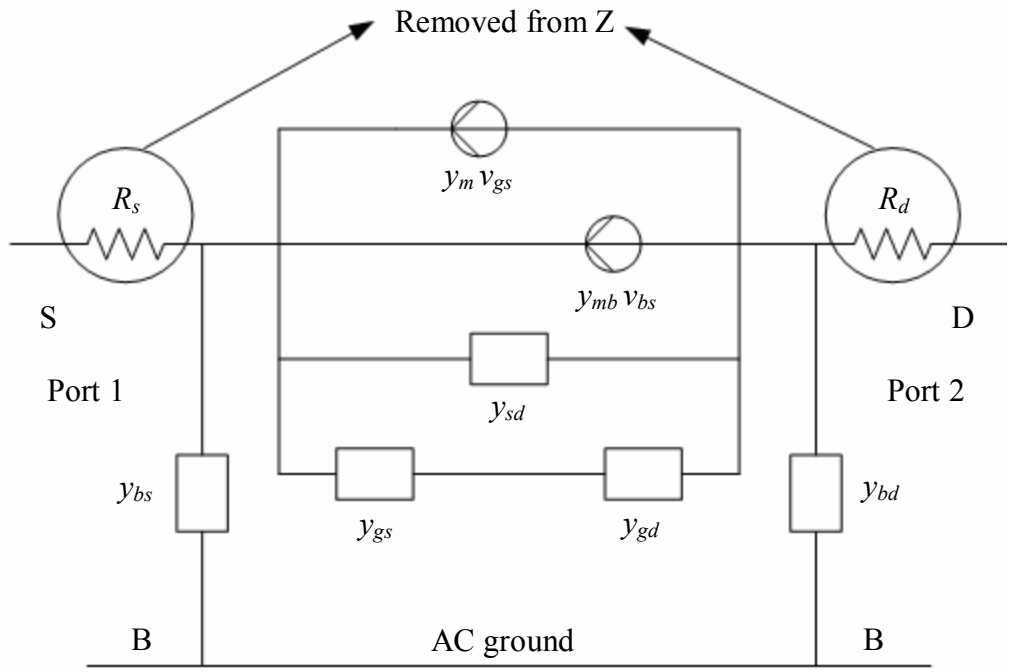


Figure 4. 2(b) Practical Equivalent circuit of the SD-R device (SD configuration)

The significance of this novel test structure in this work is that, it yields three physical parameters that are being directly utilized in the MOS device parameter extraction in the different two-port measurements. The knowledge of the total junction admittances (intrinsic and extrinsic components together) is very crucial to get direct access to the probe impedance network at the third port, in all three two-port configurations. For example, to de-embed the probe network in the GD configuration, we need an accurate estimate of the bulk-drain junction admittance at all biases and frequencies. This facilitates the extraction of the remaining admittance elements of the GD configuration. Similarly, the bulk-source admittance is required in the GS configuration and both y_{bd} and y_{bs} are essential to correct the SD configuration data.

The approach of using junction admittances extracted from off-state (V_{GS}=0) for the on-state extraction is inaccurate, as the intrinsic admittances (y_{bsi} and y_{bdi}) are not available under such conditions. This may result in erroneous extraction of other

equivalent circuit model parameters and thus will not contribute to an effective removal of the probe's effect. The body-effect trans-conductance is also a highly desired model parameter as it is very difficult to directly extract y_{mb} from any other configuration.

The concept of the SD-R test structure and its extracted model parameters are very useful not only in the context of the current work, but also for RF MOSFET modeling and parameter extraction in general. The role played by the substrate at RF is clearly revealed in all these parameters viz. y_{bd}, y_{bs} and y_{mb}. The next section explains the parameter extraction scheme of the SD-R device.

4.2.1 Parameter extraction of the SD-R device

The analysis of the equivalent circuit proceeds by first eliminating the series resistances (i.e. R_s and R_d in SD). The measured data, after de-embedding of on-chip parasitic, is converted to Z-parameters and the inner Z-parameters are obtained by directly subtracting R_s and R_d from z_{11} and z_{22} respectively.

$$Z_{inner} = \begin{bmatrix} z_{11} - R_s & z_{12} \\ z_{21} & z_{22} - R_d \end{bmatrix} \tag{4.14}$$

These inner Z-parameters are converted back to Y-parameters. The expressions for the two-port Y-parameters of the remaining network in SD configuration are then derived from the equivalent circuit in Figure 4.2(b) using small-signal analysis techniques.

$$y_{11} = \frac{y_{gd}(y_{gs} + y_m)}{y_{gs} + y_{gd}} + y_{bs} + y_{sd} + y_{mb} \tag{4.15}$$

$$y_{12} = \frac{-y_{gd}(y_{gs} + y_m)}{y_{gs} + y_{gd}} - y_{sd} \tag{4.16}$$

$$y_{21} = \frac{-y_{gd}(y_{gs} + y_m)}{y_{gs} + y_{gd}} - y_{sd} - y_{mb} \tag{4.17}$$

$$y_{22} = \frac{y_{gd}(y_{gs} + y_m)}{y_{gs} + y_{gd}} + y_{bd} + y_{sd} \tag{4.18}$$

Algebraic manipulation of the above equations directly yields the admittances y_{bs}, y_{bd} and y_{mb} as given in (4.19)-(4.21).

$$y_{11} + y_{21} = y_{bs} \tag{4.19}$$

$$y_{22} + y_{12} = y_{bd} \tag{4.20}$$

$$y_{12} - y_{21} = y_{mb} \tag{4.21}$$

As the SD-R MOS device has the same specifications as the normal device these parameters can be directly used in the equivalent circuit based parameter extraction of the MOS device that follows in the next section.

4.3 MOS device model analysis and extraction

This section provides the Y-parameter expressions we have derived for the different two-port configurations based on our RF MOSFET equivalent circuit model along with our newly developed model parameter extraction scheme. The general RF model for the device in Figure 4.1 is suitably modified to represent the individual two-port measurement configurations by the appropriate inclusion of the probe impedance at the third port. The respective equivalent circuit parameters are then uniquely extracted in each configuration. The gate-bulk admittance y_{gb} is very small in the "On-state" ($V_{GS}>V_{th}$) of a MOSFET and is therefore neglected in the extraction. The y_{mb}, y_{bd} and y_{bs}

obtained from the SD-R device extraction are utilized here to extract the other unknown parameters namely, y_{gd}, y_{gs}, y_m and y_{sd} respectively.

4.3.1 Analysis of the GD Configuration

The RF small-signal model for the GD configuration of the MOSFET is shown in Figure 4.3. The GPG probe impedance along with the parallel and series parasitic at the source terminal - together denoted as "z_{probe}" - is indicated by the elements at the source terminal, shown enclosed in a circle in Figure 4.3. The extraction of the equivalent circuit parameters proceeds by first eliminating the series resistances (i.e. R_g and R_d in GD). The measured data after the de-embedding of pad and interconnect parasitic is converted to Z-parameters and the inner Z-parameters are obtained by directly subtracting R_g and R_d from z_{11} and z_{22} respectively.

$$Z_{inner} = \begin{bmatrix} z_{11} - R_g & z_{12} \\ z_{21} & z_{22} - R_d \end{bmatrix} \tag{4.22}$$

The inner Z-parameters are converted back to Y-parameters. We have derived the expressions (4.23)-(4.28) for the two-port Y-parameters of the RF equivalent circuit in GD configuration (sans R_g and R_d) using small-signal analysis techniques.

$$y_{11} = \frac{y_{gs}(y_{sp} + y_{sd} + y_{mb})}{K_{GD}} + y_{gb} + y_{gd} \tag{4.23}$$

$$y_{12} = \frac{-y_{gs}y_{sd}}{K_{GD}} - y_{gd} \tag{4.24}$$

$$y_{21} = \frac{y_m y_{sp} - y_{gs}(y_{sd} + y_{mb})}{K_{GD}} - y_{gd} \tag{4.25}$$

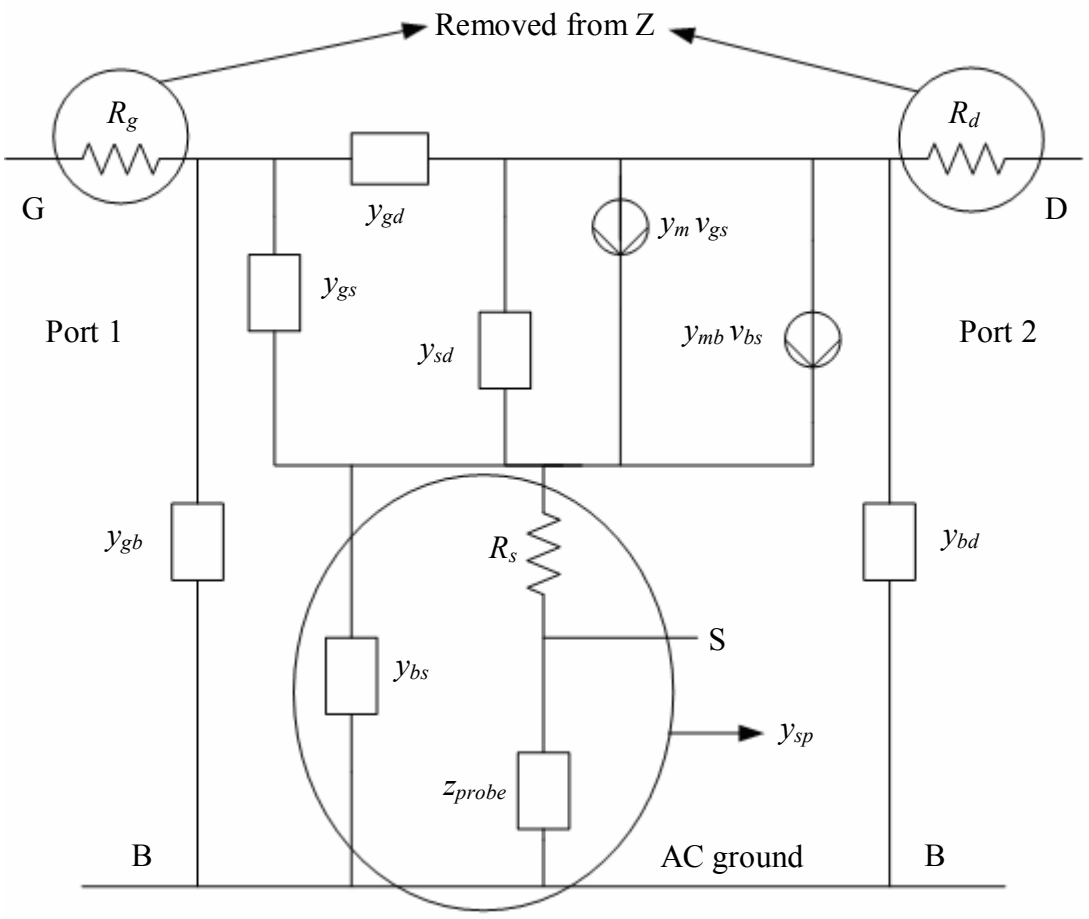


Figure 4. 3 RF Equivalent circuit of the MOSFET in GD configuration

$$y_{22} = \frac{(y_{gs} + y_{sp})y_{sd}}{K_{GD}} + y_{bd} + y_{gd} \tag{4.26}$$

$$y_{sp} = y_{bs} + (R_s + z_{probe})^{-1} \tag{4.27}$$

$$K_{GD} = y_{gs} + y_{sp} + y_{sd} + y_{mb} + y_m . \tag{4.28}$$

K_{GD} is chosen for convenience of mathematical analysis and it represents the sum of several individual admittances, which appears in each Y-parameter expression of the GD configuration. Similarly, K_{GS} and K_{SD} have been defined in the GS and SD analyses respectively, as will be described later.

4.3.2 Parameter extraction for the GD configuration

We have devised a direct model parameter extraction scheme based on algebraic manipulations of the small-signal Y-parameter equations derived in the previous sections. The procedure is described below. The combined admittance y_{sp} is directly calculated from (4.27) with the knowledge of R_s (from 4.12), z_{probe} (from (3.14)) and y_{bs} (from 4.19). To get the expressions in a simpler form we need to find the sum of few of the individual admittance expressions.

From (4.23) and (4.24),

$$y_{11} + y_{12} = \frac{y_{gs}(y_{sp} + y_{mb})}{K_{GD}}. \tag{4.29}$$

From (4.23) and (4.25),

$$y_{11} + y_{21} = \frac{y_{sp}(y_m + y_{gs})}{K_{GD}}. \tag{4.30}$$

From (4.24) and (4.26),

$$y_{22} + y_{12} = y_{bd} + \frac{y_{sp} y_{sd}}{K_{GD}}. \tag{4.31}$$

From (4.28),

$$\frac{y_{sp} + y_{mb} + y_m + y_{gs} + y_{sd}}{K_{GD}} = 1. \tag{4.32}$$

Using (4.29), (4.30) and (4.31) in (4.32), we extract,

$$y_{gs} = \frac{y_{11} + y_{12}}{\left[1 - \left(\frac{y_{11} + y_{21}}{y_{sp}}\right) - \left(\frac{y_{22} + y_{12} - y_{bd}}{y_{sp}}\right)\right]}. \tag{4.33}$$

Using (4.31) and y_{gs} in (4.24), we obtain,

$$y_{gd} = -y_{12} - y_{gs}\left(\frac{y_{22} + y_{12} - y_{bd}}{y_{sp}}\right). \tag{4.34}$$

Substituting y_{gs}, y_{mb} and y_{sp} in (4.29), we get K_{GD} in (4.35).

$$K_{GD} = \frac{y_{gs}(y_{sp} + y_{mb})}{y_{11} + y_{12}} \tag{4.35}$$

Similarly, using y_{bd}, y_{sp} and K_{GD} in (4.31), we extract y_{sd}.

$$y_{sd} = K_{GD}\left(\frac{y_{22} + y_{12} - y_{bd}}{y_{sp}}\right) \tag{4.36}$$

The gate-drain trans-admittance y_m is obtained by using y_{gs}, y_{sp} and K_{GD} in (4.30).

$$y_m = K_{GD}\left(\frac{y_{11} + y_{21}}{y_{sp}}\right) - y_{gs} \tag{4.37}$$

This completes the on-state parameter extraction of the GD configuration.

4.3.3 Analysis of the GS Configuration

For the GS configuration the model can be constructed by placing the GPG probe impedance (z_{probe}) between the bulk and drain terminals. The circuit model for GS is shown in Figure 4.4. The extraction of the equivalent circuit parameters proceeds by first eliminating the series resistances (i.e. R_g and R_s in GS). The measured data after de-embedding of pad and interconnect parasitic is converted to Z-parameters and the inner Z-parameters are obtained by directly subtracting R_g and R_s from z_{11} and z_{22} respectively.

$$Z_{inner} = \begin{bmatrix} z_{11} - R_g & z_{12} \\ z_{21} & z_{22} - R_s \end{bmatrix} \tag{4.38}$$

The inner Z-parameters are converted back to Y-parameters. We have derived here the expressions (4.39)-(4.44) for the two-port Y-parameters of the RF equivalent circuit in the GS configuration (sans R_g and R_s) using small-signal analysis techniques.

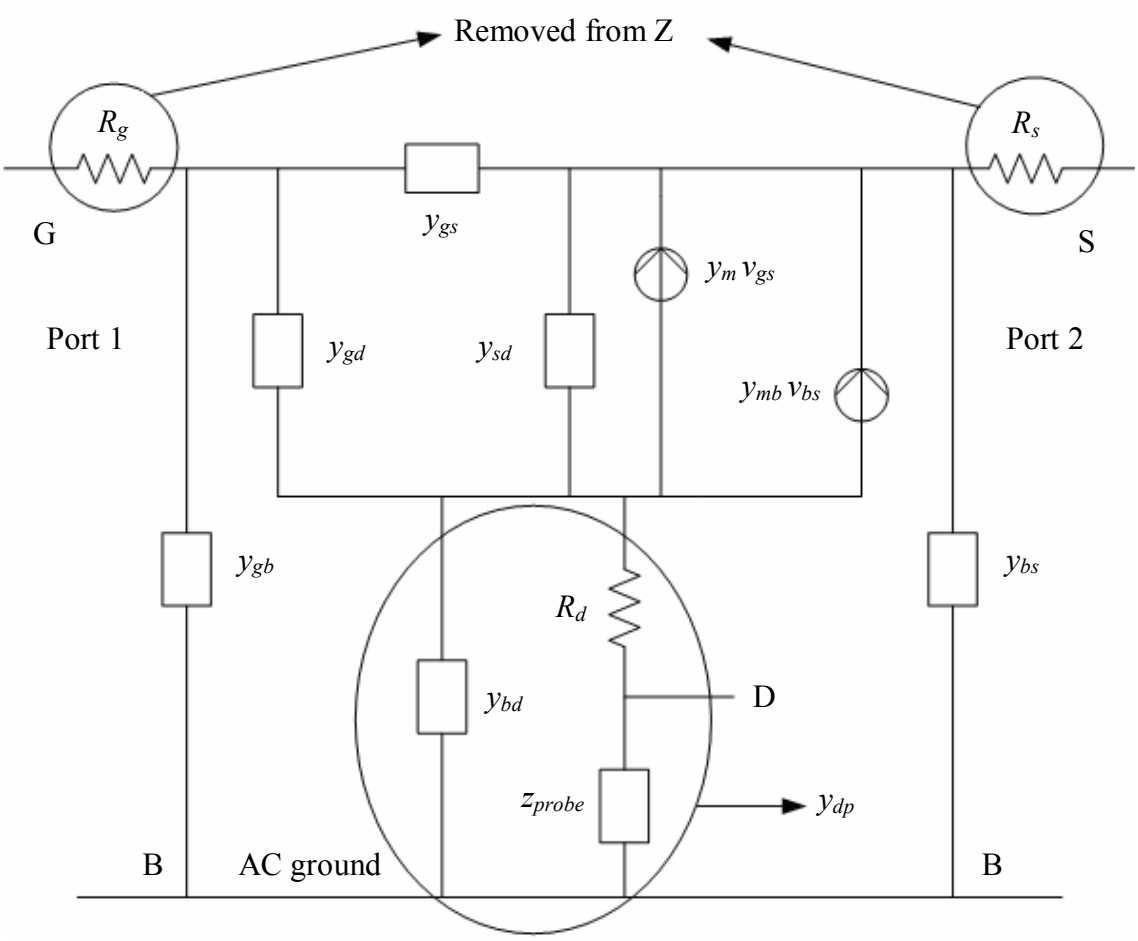


Figure 4. 4 RF Equivalent circuit of the MOSFET in GS configuration

$$y_{11} = \frac{y_{gd}(y_{dp} + y_{sd} + y_m)}{K_{GS}} + y_{gb} + y_{gs} \tag{4.39}$$

$$y_{12} = \frac{-y_{gd}(y_m + y_{mb} + y_{sd})}{K_{GS}} - y_{gs} \tag{4.40}$$

$$y_{21} = \frac{-y_m y_{dp} - y_{gd}(y_{sd} + y_m)}{K_{GS}} - y_{gs} \tag{4.41}$$

$$y_{22} = \frac{(y_{gd} + y_{dp})(y_m + y_{mb} + y_{sd})}{K_{GS}} + y_{bs} + y_{gs} \tag{4.42}$$

$$y_{dp} = y_{bd} + (R_d + z_{probe})^{-1} \tag{4.43}$$

$$K_{GS} = y_{dp} + y_{sd} + y_{gd} \tag{4.44}$$

4.3.4 Parameter extraction for the GS configuration

In the GS configuration the probe impedance cum third port parasitic combination (z_{probe}) is combined along with the drain resistance R_d from (4.12) and the bulk-drain admittance y_{bd} from (4.20) to compute y_{dp} in (4.43). The gate-bulk admittance $y_{gb} \approx 0$ as mentioned before. We have developed the following extraction procedure in this work to uniquely extract the equivalent circuit model parameters y_{gd}, y_{gs}, y_m and y_{sd} from the GS configuration.

From (4.39) and (4.40),

$$y_{11} + y_{12} = \frac{y_{gd}(y_{dp} - y_{mb})}{K_{GS}}. \tag{4.45}$$

Adding (4.40) and (4.42) and suitably re-arranging we obtain (4.46).

$$\frac{y_{22} + y_{12} - y_{bs}}{y_{dp}} = \frac{y_m + y_{mb} + y_{sd}}{K_{GS}} \tag{4.46}$$

From (4.39) and (4.41),

$$\frac{y_{11} + y_{21}}{y_{dp}} = \frac{y_{gd} - y_m}{K_{GS}}. \tag{4.47}$$

From (4.46) and (4.47), we obtain a useful relationship in (4.48).

$$\frac{(y_{11}+y_{21})+(y_{22}+y_{12}-y_{bs})}{y_{dp}}=\frac{y_{mb}+y_{sd}+y_{gd}}{K_{GS}}. \tag{4.48}$$

But from (4.44) it follows that,

$$\frac{y_{dp}+y_{sd}+y_{gd}}{K_{GS}}=1. \tag{4.49}$$

Subtracting (4.48) from (4.49),

$$1-\left[\frac{(y_{11}+y_{21})+(y_{22}+y_{12}-y_{bs})}{y_{dp}}\right]=\frac{y_{dp}-y_{mb}}{K_{GS}}. \tag{4.50}$$

Using (4.50) in (4.45), the y_{gd} model parameter is directly extracted as,

$$y_{gd}=\frac{y_{11}+y_{12}}{1-\left[\frac{(y_{11}+y_{21})+(y_{22}+y_{12}-y_{bs})}{y_{dp}}\right]}. \tag{4.51}$$

Using y_{gd} and (4.46) in (4.40) we can obtain the gate-source model admittance,

$$y_{gs}=-y_{12}-y_{gd}\left(\frac{y_{22}+y_{12}-y_{bs}}{y_{dp}}\right). \tag{4.52}$$

A good match has been obtained between the y_{gd} obtained from the GD and GS configurations. Similar match has been observed in the y_{gs} extracted from the two different configurations.

Substituting y_{gd}, y_{dp} and y_{mb} in (4.45), we extract K_{GS} as shown in (4.53).

$$K_{GS}=\frac{y_{gd}(y_{dp}-y_{mb})}{y_{11}+y_{12}} \tag{4.53}$$

Using y_{gd} and y_{dp} in (4.44), we can extract the source-drain admittance y_{sd},

$$y_{sd}=K_{GS}-y_{dp}-y_{gd}. \tag{4.54}$$

Finally, the device trans-admittance parameter y_m is obtained in (4.55), by substituting y_{gd}, y_{dp} and K_{GS} in (4.47).

$$y_m = y_{gd} - \frac{K_{GS}(y_{11} + y_{21})}{y_{dp}}. \tag{4.55}$$

A good match has been obtained between the y_m obtained from the GD and GS configurations respectively. Similar match has been observed in the y_{mb} extracted from the two different configurations. The results are given in Chapter 6. Such a match ensures the consistency of the extraction routine used to obtain the equivalent circuit model parameters. The extraction for the GS configuration is completed here.

4.3.5 Analysis of the SD Configuration

The SD circuit model is obtained by placing z_{probe} between the bulk and gate terminals of the MOSFET. Here, the probe impedance (z_{probe}) is combined along with the gate resistance R_g from (4.11) to compute y_{gp} while the small gate-bulk admittance y_{gb} is neglected, as it is shunted out by the much larger admittance of the probe combination and gate resistance. Figure 4.5 shows the RF equivalent circuit for the SD configuration. The measured data after the de-embedding of pad and interconnect parasitic is converted to Z-parameters and the series resistances R_s and R_d are removed directly.

As was done for the GD and GS configurations, we have derived in (4.56)-(4.61), the expressions for the two-port Y-parameters of the RF equivalent circuit in the SD configuration (sans R_s and R_d) using small-signal analysis techniques.

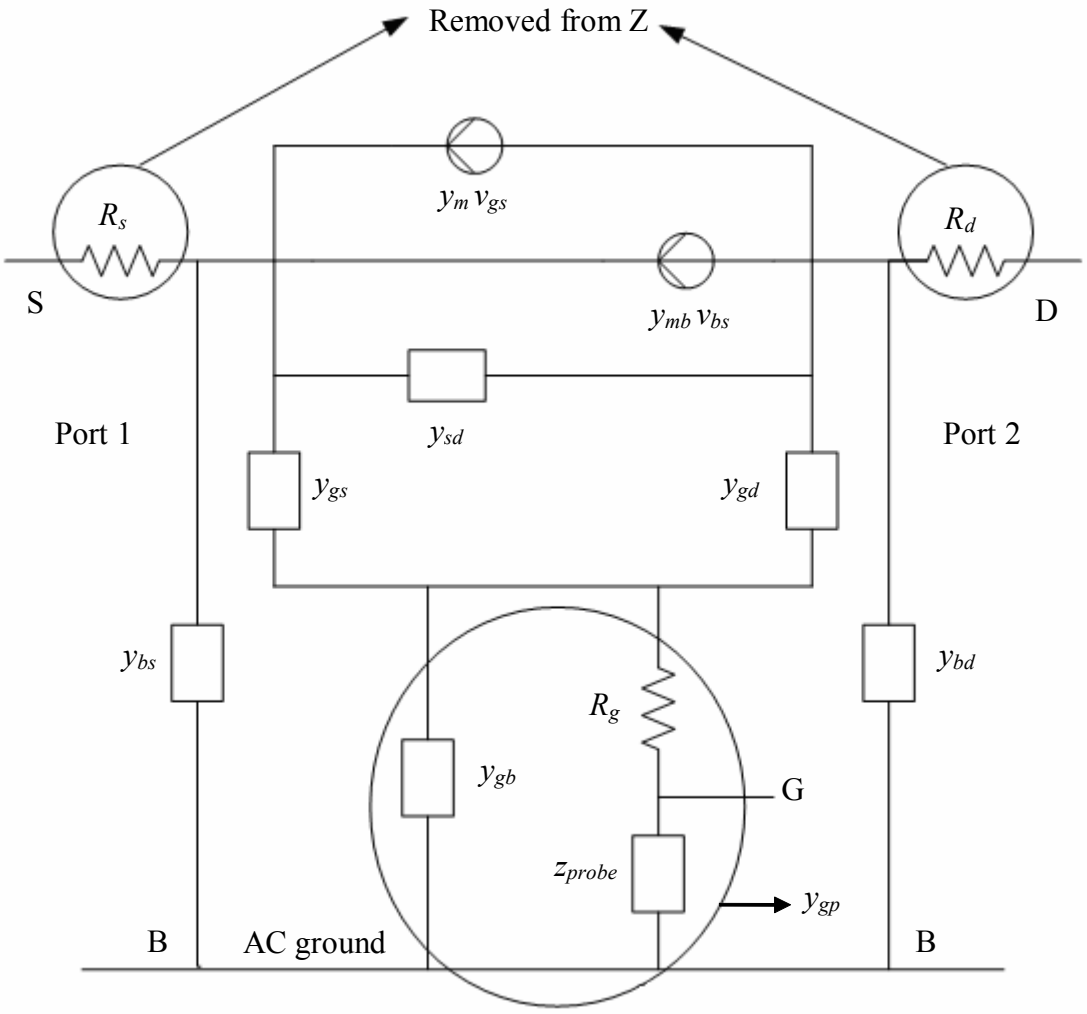


Figure 4. 5 RF Equivalent circuit of the MOSFET in SD configuration

$$y_{11} = \frac{(y_{gd} + y_{gp})(y_{gs} + y_m)}{K_{SD}} + y_{bs} + y_{sd} + y_{mb} \tag{4.56}$$

$$y_{12} = \frac{-y_{gd}(y_m + y_{gs})}{K_{SD}} - y_{sd} \tag{4.57}$$

$$y_{21} = \frac{-y_m y_{gp} - y_{gd}(y_{gs} + y_m)}{K_{SD}} - y_{sd} - y_{mb} \tag{4.58}$$

$$y_{22} = \frac{y_{gd}(y_{gp} + y_m + y_{gs})}{K_{SD}} + y_{bd} + y_{sd} \tag{4.59}$$

$$y_{gp} = y_{gb} + (R_g + z_{probe})^{-1} \approx (R_g + z_{probe})^{-1} \tag{4.60}$$

$$K_{SD} = y_{gp} + y_{gs} + y_{gd} \tag{4.61}$$

4.3.6 Parameter extraction for the SD configuration

We have developed an extraction procedure to uniquely obtain the equivalent circuit model parameters y_{gd}, y_{gs}, y_m and y_{sd} from the SD configuration. The parameter extraction of the device is carried out using the bulk-drain, bulk-source admittances as well as the body-effect trans-admittance (all obtained from the SD-R device) in the Y-parameter equations (4.56)-(4.61), derived in the previous section.

Using y_{bs}, (4.56) and (4.58), we obtain (4.62).

$$\frac{y_{gs}}{K_{SD}} = \frac{y_{11} + y_{21} - y_{bs}}{y_{gp}}. \tag{4.62}$$

Using y_{bd}, (4.57) and (4.59) we get,

$$\frac{y_{gd}}{K_{SD}} = \frac{y_{22} + y_{12} - y_{bd}}{y_{gp}}. \tag{4.63}$$

From (4.61) it follows that,

$$\frac{y_{gp} + y_{gs} + y_{gd}}{K_{SD}} = 1. \tag{4.64}$$

Substituting y_{gp}, (4.62) and (4.63) in the above equation, we can extract K_{SD}.

$$K_{SD} = \frac{y_{gp}}{\left[1 - \left(\frac{y_{22} + y_{12} - y_{bd}}{y_{gp}}\right) - \left(\frac{y_{11} + y_{21} - y_{bs}}{y_{gp}}\right)\right]} \tag{4.65}$$

Using K_{SD} in (4.62) we extract y_{gs} as shown in (4.66).

$$y_{gs} = K_{SD}\left(\frac{y_{11} + y_{21} - y_{bs}}{y_{gp}}\right). \tag{4.66}$$

Similarly K_{SD} is used in (4.63) to yield y_{gd} as shown in (4.67).

$$y_{gd} = K_{SD}\left(\frac{y_{22} + y_{12} - y_{bd}}{y_{gp}}\right) \tag{4.67}$$

From (4.57) and (4.58), we get,

$$y_{12} - y_{21} = y_{mb} + \frac{y_m y_{gp}}{K_{SD}}. \tag{4.68}$$

Substituting y_{mb}, y_{gp} and K_{SD} in the above equation we extract the trans-admittance y_m.

$$y_m = K_{SD}\left(\frac{y_{12} - y_{21} - y_{mb}}{y_{gp}}\right) \tag{4.69}$$

Using y_{gd}, y_{gs}, y_m and K_{SD} in (4.57), we extract the final parameter y_{sd}.

$$y_{sd} = -y_{12} - \frac{y_{gd}(y_m + y_{gs})}{K_{SD}} \tag{4.70}$$

This completes the parameter extraction of the SD configuration. The y_{gd}, y_{gs}, y_{mb} and y_m obtained from this configuration match very well with those obtained from the GD and GS configurations. The results are shown in Chapter 6.

As the equivalent circuit parameters have been extracted in all three configurations, these can be used to reconstruct the actual two-port Y-parameters of the device, which share a direct correspondence with the required three-port Y-parameters. The generation of three-port data by removal of the probe impedance and extraction of the device terminal charges is taken up in Section 4.5. The next section describes the extrinsic parameter extraction of the device.

4.4 Off-state analysis and parameter extraction

The MOS device measurements at V_{GS}=0V are used to extract the extrinsic device parameters like junction and overlap admittances. The device is in the off-state for this gate bias. The admittances are extracted for all drain and source bias points. The general RF equivalent circuit for the GD, GS and SD configurations are simplified by taking y_m=0 and y_{mb}=0 as both the trans-admittances are assumed to be negligible at zero gate bias. All the other parameters reflect the extrinsic admittances and are denoted by an 'e' in their suffix nomenclature (refer Section 4.1.1). The GD model is given in Figure 4.6.

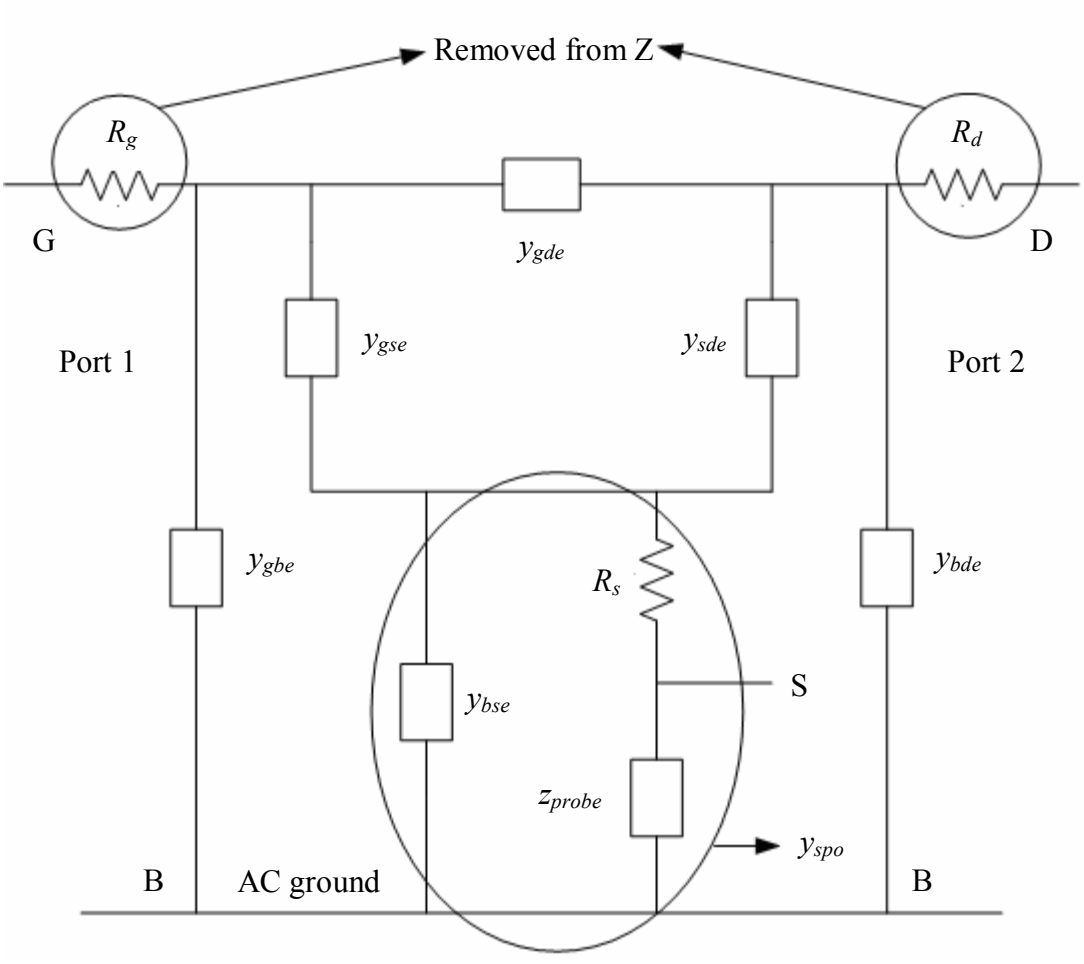


Figure 4. 6 RF Equivalent circuit of the MOSFET in off-state (GD configuration)

The series resistances are removed from the Z-parameters as explained in the on-state extraction. The probe admittance combination is denoted as y_{spo}.

$$y_{spo} = y_{bse} + (R_s + z_{probe})^{-1} \tag{4.71}$$

As the probe admittance is much larger than any of the device extrinsic admittances, we have $y_{spo} >> y_{gse}$, y_{sde}. Thus the gate-drain overlap admittance can be directly obtained as,

$$y_{gde} = -y_{12}\,. \tag{4.72}$$

A similar approach is adopted towards the off-state equivalent circuit for the GS configuration in Figure 4.7. The probe admittance combination is denoted as y_{dpo}. As $y_{probe} >> y_{bde}$,

$$y_{dpo} = y_{bde} + (R_d + z_{probe})^{-1} \approx (R_d + z_{probe})^{-1}. \tag{4.73}$$

As the probe admittance is much larger than any of the device extrinsic admittances, we have $y_{dpo} >> y_{gde}$, y_{sde}. Thus the gate-source overlap admittance can be directly obtained as,

$$y_{gse} = -y_{12}\,. \tag{4.74}$$

A very good estimate of the gate-bulk admittance is obtained as shown in (4.75).

$$y_{11} + y_{12} = y_{gbe} + y_{gse} + \frac{y_{gde}y_{dpo}}{y_{dpo} + y_{gde} + y_{sde}} \tag{4.75}$$

In the off-state we know that $y_{dpo} >> y_{sde}$. Using y_{gde} and y_{gse} while neglecting y_{sde} in (4.75),

$$y_{gbe} = y_{11} + y_{12} - y_{gse} - \frac{y_{gde}y_{dpo}}{y_{dpo} + y_{gde}}\,. \tag{4.76}$$

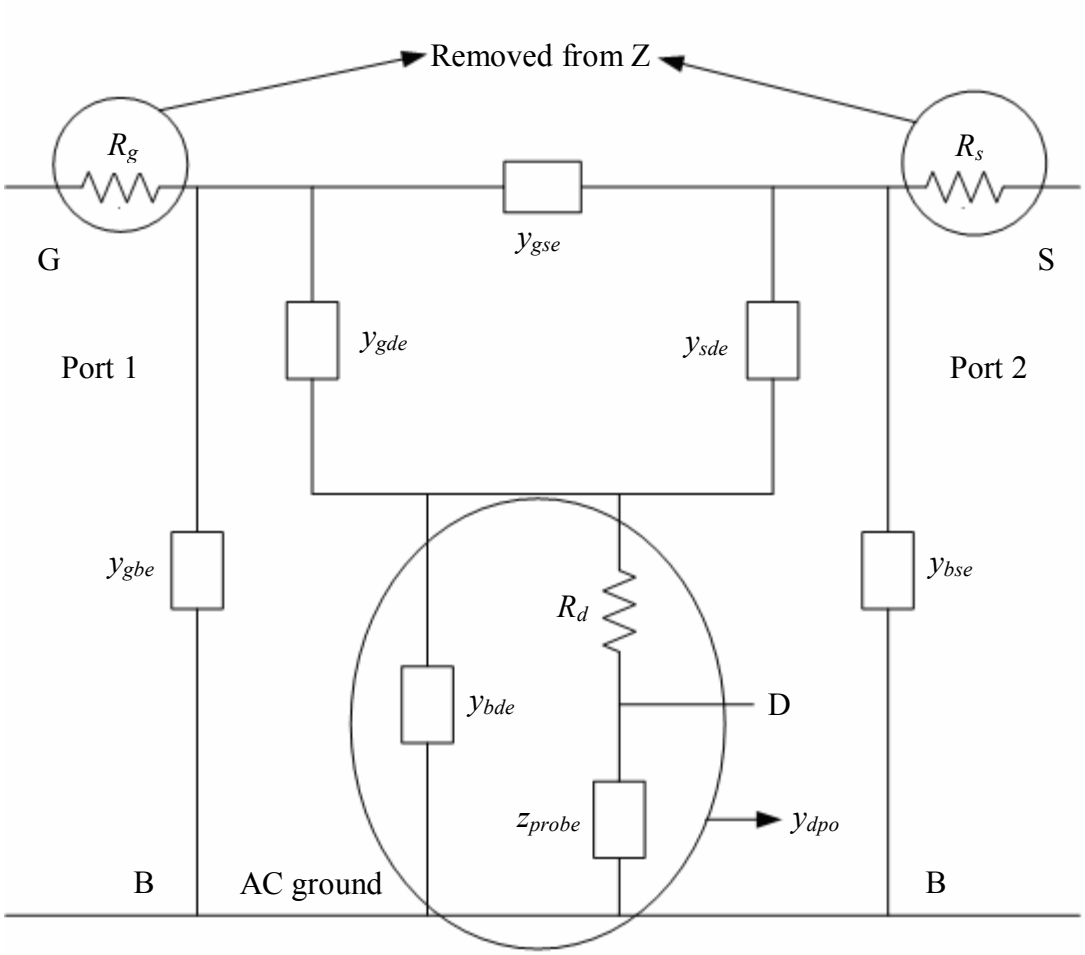


Figure 4. 7 RF Equivalent circuit of the MOSFET in off-state (GS configuration)

In order to extract the remaining extrinsic admittances, we use the off-state measurements in the SD configuration. The corresponding model circuit is shown in Figure 4.8. The source and drain resistances are removed from the Z-parameters. The remaining network is viewed as a combination of a *T*-network (comprising y_{gde}, y_{gse} and y_{gpe}) and a π-network (comprising y_{bde}, y_{sde} and y_{bse}). The probe and gate-bulk admittance combination is given as,

$$y_{gpo} = y_{gbe} + (R_g + z_{probe})^{-1}. \tag{4.77}$$

With the knowledge of y_{gbe}, y_{gde} and y_{gse} from GD and GS off-state extractions, we construct the T-network (Z_T) as,

$$Z_T = \begin{bmatrix} z_{gse} + z_{gpe} & z_{gpe} \\ z_{gpe} & z_{gde} + z_{gpe} \end{bmatrix}. \tag{4.78}$$

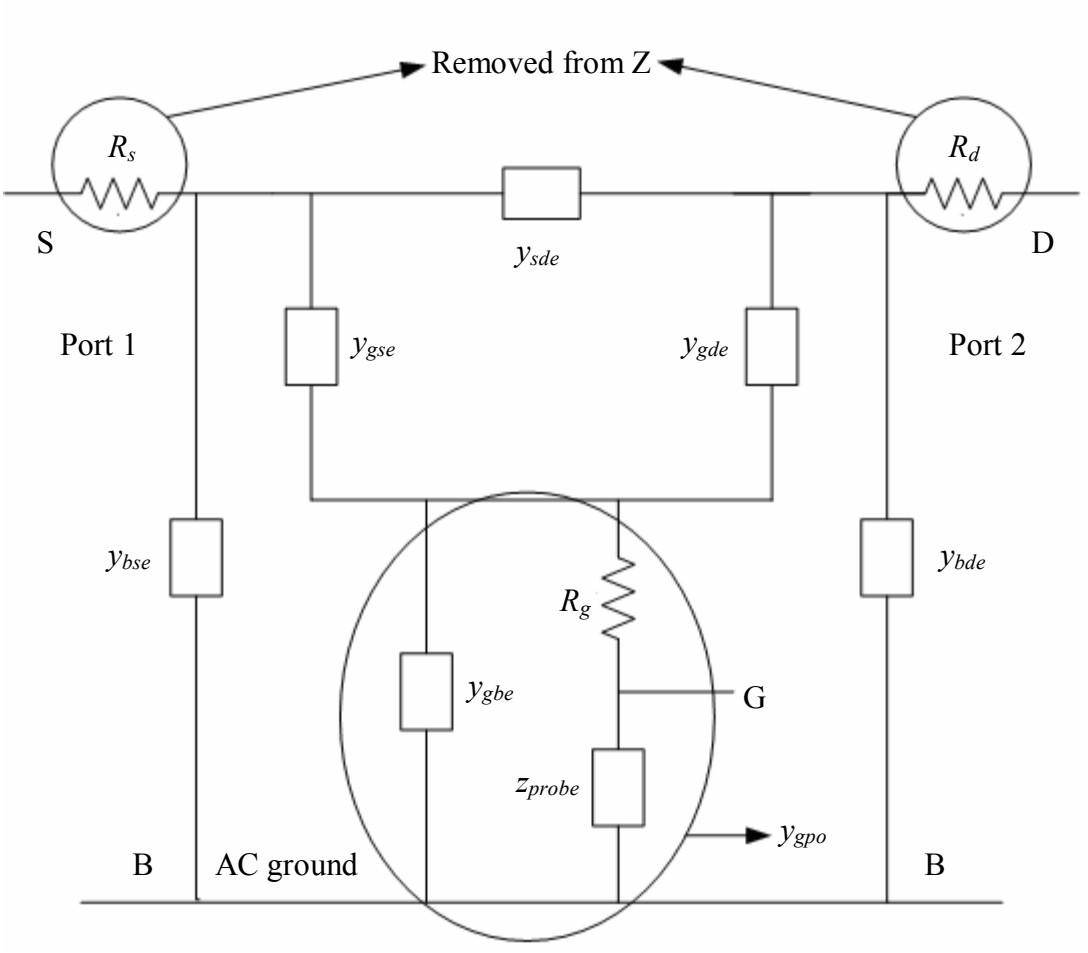


Figure 4. 8 RF Equivalent circuit of the MOSFET in off-state (SD configuration)

Now, as the T- and π-networks are parallel to each other, the admittance matrix of the π-network (Y_π) can be extracted by simply subtracting the admittance matrix of the T-network (Y_T) from the total admittance matrix ($Y_{T+\pi}$) as given in (4.79).

$$Y_{\pi} = Y_{T+\pi} - Y[Z_T] = \begin{bmatrix} y_{\pi.11} & y_{\pi.12} \\ y_{\pi.21} & y_{\pi.22} \end{bmatrix} = \begin{bmatrix} y_{bse} + y_{sde} & -y_{sde} \\ -y_{sde} & y_{bde} + y_{sde} \end{bmatrix} \tag{4.79}$$

We can directly extract the source-drain fringing admittances, the source-bulk and drain-bulk junction admittances from (4.79).

$$y_{sde} = -y_{\pi.12} \tag{4.80}$$

$$y_{bse} = y_{\pi.11} + y_{\pi.12} \tag{4.81}$$

$$y_{bde} = y_{\pi.22} + y_{\pi.12} \tag{4.82}$$

This completes the MOS extrinsic parameter extraction. The extrinsic bulk-source and bulk-drain admittances have also been obtained by direct extraction from the SD-R device and they match quite well with the junction admittances obtained here (Chapter 6).

The next section describes the reconstruction of the measured data by de-embedding the known probe impedance, generation of three-port admittance coefficients and the extraction of the terminal charges.

4.5 Probe de-embedding and generation of three-port data

The knowledge of each of the equivalent circuit model parameters as a function of bias and frequency helps us to reconstruct the measured data of the actual device at every measurement point. In the RF equivalent circuits of Figure 4.3, 4.4 and 4.5, the element z_{probe} representing the probe impedance and the third port parasitic is removed and replaced by an ideal short. Thus we have $y_{sp} = y_{bs} + (R_s)^{-1}$, $y_{dp} = y_{bd} + (R_d)^{-1}$ and $y_{gp} = (R_g)^{-1}$ (neglecting y_{gb}) in the GD, GS and SD models respectively. The same small signal analysis is valid for the new equivalent circuits. The probe impedance is effectively de-

embedded by this approach. The accurate two-port Y-data is now computed using the Y-parameter equations (4.23)-(4.28), (4.39)-(4.44) and (4.56)-(4.61) for the GD, GS and SD configurations respectively. The same procedure is adopted for the device measurements in the off-state, using the corresponding simple admittance equations with modified values of y_{spo}, y_{dpo}, and y_{gpo}. Now, the true two-port Y-data enjoys a direct correspondence to the three-port Y-data as explained in Chapter 2 (Section 2.2). We therefore assemble the three-port admittance parameters to achieve complete characterization of the MOS device.

4.5.1 Three port capacitance and conductance coefficients

The imaginary parts of the admittances divided by the angular frequencies ($\omega=2\pi f$ where f is the frequency of measurement) yield the three-port capacitance coefficients ($\mathrm{Im}(y_{ij})=\omega C_{ij}$). The real parts of the admittances denote the device conductance coefficients. The bias and frequency dependence of these coefficients provides valuable insights into high frequency device physics and modeling. Especially the non-quasi-static effect and the substrate coupling are characterized very effectively by these three port coefficients. A direct consequence of this work is the generation of terminal charges. The next section is devoted to the extraction of the device terminal charges.

4.5.2 Terminal charge extraction

The knowledge of the device terminal charges as a function of both bias and frequency is mandatory for all circuit simulators. These charges provide a complete description of the device and they can be manipulated to generate any other network parameters of our interest. We follow the method described in [32] to extract the charges. We apply the

method to show the frequency dependence of terminal charges for the first time. The procedure is described as follows.

We know that the capacitance is defined as, $c_{ij}=\delta Q_i/\delta V_j$. As the imaginary part of the Y-parameters yield the capacitances, one can find the charge induced at any terminal as a function of the biases at all other terminals. Though the bulk is regarded as the common ground terminal for all the S-parameter measurements, the DC bias at any terminal is denoted with respect to the source, i.e. we have V_{GS}, V_{DS} and V_{BS} as the controlling voltages (note that V_{BS} is always negative for NMOS transistors). The expressions for the charges are derived using the principle of superposition of controlling voltages.

For example, to calculate the gate charge at a bias of (V_{GS}, V_{DS}, V_{BS}), starting from zero bias (0, 0, 0), we raise one voltage (say V_{GS}) at a time while holding the other two fixed and the charge induced by this voltage build-up (V_{GS}, 0, 0) is first calculated from the related admittance co-efficient Im(y_{gg}) – *denotes the effect of the gate terminal on itself* [7]. The voltage at the second terminal is built up next (say V_{DS}) while holding the other two fixed, from the current bias point (V_{GS}, 0, 0) to reach (V_{GS}, V_{DS}, 0) and the charge induced by this change is calculated from the related admittance co-efficient Im(y_{gd}) – *denotes the effect of the drain terminal on the gate.* Similarly, the third terminal voltage is built-up and the induced charge is calculated. The total gate charge is thus the sum of the charges due to these individual voltage changes. The non-dependence of the terminal charges on the order, in which the voltage change is effected, has been proved in [32]. We have also verified the path independence of the extracted charges in our work. So, there can be different expressions to arrive at the same terminal charge based on the

order in which the biases are enforced. We provide one such set of expressions used here to compute the gate, drain and source charges.

$$\omega Q_G(V_{GS}, V_{DS}, V_{BS}) = \int_0^{V_{BS}} \mathrm{Im}(y_{gb}(0,0,V_b))dV_b + \int_0^{V_{GS}} \mathrm{Im}(y_{gg}(V_g,0,V_{BS}))dV_g + \int_0^{V_{DS}} \mathrm{Im}(y_{gd}(V_{GS},V_d,V_{BS}))dV_d \quad (4.83)$$

$$\omega Q_D(V_{GS}, V_{DS}, V_{BS}) = \int_0^{V_{BS}} \mathrm{Im}(y_{db}(0,0,V_b))dV_b + \int_0^{V_{GS}} \mathrm{Im}(y_{dg}(V_g,0,V_{BS}))dV_g + \int_0^{V_{DS}} \mathrm{Im}(y_{dd}(V_{GS},V_d,V_{BS}))dV_d \quad (4.84)$$

$$\omega Q_S(V_{GS}, V_{DS}, V_{BS}) = \int_0^{V_{BS}} \mathrm{Im}(y_{sb}(0,0,V_b))dV_b + \int_0^{V_{GS}} \mathrm{Im}(y_{sg}(V_g,0,V_{BS}))dV_g + \int_0^{V_{DS}} \mathrm{Im}(y_{sd}(V_{GS},V_d,V_{BS}))dV_d \quad (4.85)$$

In the above equations, y_{gb}=-(y_{gg}+y_{gd}+y_{gs}), y_{db}=-(y_{dg}+y_{dd}+y_{ds}) and y_{sb}=-(y_{sg}+y_{sd}+y_{ss}). The bulk charge can be obtained from (4.83)-(4.85) as, Q_B=-(Q_G+Q_D+Q_S) using the charge conservation principle of the device. The charges are then computed by numerical integration using Simpson's Rule on the measured admittance data. Equations (4.83)-(4.85) clearly imply that computation of each charge requires admittance components (see Figure 2.5) obtained from two or more of the different measurement configurations. This demonstrates the importance of the three-port characterization developed here

towards charge modeling and circuit simulation. Such explicit terminal charge extraction is never possible using conventional two-port measurements and characterization.

The next chapter describes the two-dimensional simulation of a 0.35-micron NMOS process and RF device simulations carried out along the lines of device measurements to generate three-port data and thus enable a comparison of trends with measured (probe de-embedded) data.

4.6 Summary

The MOS device is represented by a general RF small-signal equivalent circuit. The admittance analysis and parameter extraction of the SD-R device is first conducted to extract the bulk-source, bulk-drain admittances and the body-effect trans-admittance. The small-signal analysis and parameter extraction of the three two-port measurement configurations are carried out by suitably modifying the equivalent circuit to reflect the position of the third port probe admittance. Similar extraction of extrinsic parameters is carried out in the off-state of the device. The extracted parameters are used to reconstruct the actual two-port admittance parameters of the device in each configuration, after replacing the probe admittance with an ideal short in the analysis. Thus the probe de-embedded measurement data is used to assemble the accurate three-port Y-parameters of the MOSFET. The terminal capacitances obtained from the three-port data are then used to extract the individual terminal charges by numerical integration.

Chapter 5: Device Simulation

This chapter describes the numerical device simulation of a standard 0.35μm NMOS transistor in CMOS process along with its DC cum RF simulations in all the three measurement configurations discussed in earlier chapters. The device simulations have been carried out to compare the trends from measurements of the actual device with the most accurate description of the device available through simulations. However, no attempt has been made to optimize the simulation to match the actual device data, primarily because the exact process is not known. The main purpose of these device simulations is to validate the MOS three-port terminal capacitance trends that are obtained using measurements. The SD-R device functionality is also validated here by a comparison of the extracted junction admittance parameters obtained from both simulations and measurements. This work has utilized the Synopsys TCAD tools, TSUPREM-4 for process simulation and Medici for device simulations, respectively. The following sections give a brief description of these two tools and the results obtained through their usage.

5.1 Overview of TSUPREM-4 and Medici

TSUPREM-4 is a computer program for simulating the processing steps used in the manufacture of integrated silicon devices [41]. The plane of simulation is a two-dimensional device cross-section perpendicular to the surface of the silicon wafer. TSUPREM-4 keeps track of the various material layer boundaries in the structure as well as impurity distributions and redistributions within each layer. Almost all the processing steps like ion implantation, silicon and poly-silicon deposition, oxidation and silicidation

and deposition and etching of various other materials are modeled and supported by the tool. The simulation structure is divided into regions composed of different materials, which may be doped with impurities. TSUPREM-4 calculates point defects distribution (interstitials and vacancies) in silicon layers and its effects on impurity diffusion. It computes oxidation rates dynamically based on distribution of the oxidizing species in silicon dioxide layers.

TSUPREM-4 can output printed information as well as graphical plots of impurity concentrations along vertical or horizontal lines through the structure or along material interfaces, extracted capacitance, channel conductance, sheet resistance, mask information and ion implantation parameters. Two-dimensional plot capabilities of the structure, showing material boundaries, simulation grid and contours of impurity or point defect concentrations are also available.

Medici is a powerful device simulation program that is used to simulate the behavior of MOS transistors and other semiconductor devices [42]. It models the two-dimensional distributions of potential and carrier concentrations in a device structure. The program solves Poisson's equation and both the electron and hole current continuity equations. It incorporates carrier distribution statistics, physical models for incomplete ionization of impurities, recombination, photo-generation, mobility, and lifetime of carriers.

Medici uses a non-uniform triangular simulation grid, and can model devices with non-planar surface topographies. The simulation grid can be refined automatically during the solution process, by introducing additional nodes over existing mesh elements. The refinements are based on variations in potential and/or electron/hole/impurity concentration between adjacent mesh elements. The additional triangles are added if the

variation of targeted variable between adjacent mesh elements exceeds a user-specified tolerance. Impurity distributions created with the help of TSUPREM-4 process simulator can be accepted as input to Medici. The program can be used to predict electrical characteristics for arbitrary bias conditions. Medici can also perform an AC small signal analysis at any frequency in order to calculate frequency-dependent capacitance, conductance, and admittance.

5.2 Simulation of a 0.35μm NMOS structure

A standard 0.35μm NMOS process was developed using TSUPREM-4. The initial mesh was generated and a P-well was created. An oxide layer of 0.3μm thickness was grown using LOCOS process to ensure proper isolation (field oxide) and reflecting boundary conditions. In addition, a Boron field implant was used under the LOCOS to further raise field threshold for effective isolation. Threshold-adjust and anti punch-through implants were used to obtain the right threshold voltage (V_{th}=0.55V) and sub-threshold slope (S=90mV/decade). A gate oxide of thickness 7.4nm was grown. N-type poly-silicon was used for the gate electrode (thickness=0.2μm). Phosphorus and Arsenic were used for the LDD (Lightly Doped Diffusion) and Source/Drain implants respectively. Implant activation was carried out by RTA (Rapid Thermal Anneal) at 1000˚C for 5 seconds. Nitride spacers of 60nm width were formed to achieve proper LDD profiles for source and drain. Silicidation was carried out by titanium diffusion at 650˚C for 1 minute. The source/drain junction depth was found to be 0.15μm and the junction capacitance was 1.4fF/μm^2 at zero junction bias. The source/drain contacts were established with aluminum metal.

The PD.FULL option was chosen to model the point defect distribution for the implants and diffusion processes in order to account for the effect of interstitials on impurity diffusion as well as interstitial redistribution during the diffusion process. A final TSUPREM-4 mesh file with all information about material boundary and impurity concentration was generated. The input files for the process flow and the simulated structure have been included in Appendix A and B respectively.

5.3 DC and RF Simulations of the MOSFET and SD-R structure

The TSUPREM-4 generated structure file with all process information of the device was directly read as input for the Medici simulations. The Bulk electrode was defined at the bottom of the mesh corresponding to a depth of 1.5μm. The carrier mobility models were chosen to accurately model low, medium and high field conditions as well as mobility degradation due to perpendicular field. Normally, the mobility reduction along the side of a triangular mesh element is computed using the electric field components parallel and perpendicular to the side. But deviations of the current flow from the surface (at the oxide interface) are known to occur near the drain region of the channel when the drain is biased beyond the onset of saturation. Also, the drain-side fields have a very complex profile in sub-micron transistors. This means that the components of electric field parallel and perpendicular to the sides of mesh elements at the interface can be much different from the components of the field parallel and perpendicular to the direction of actual current flow. In order to overcome this problem, the EJ.MOBIL option was used to specify that the electric field components used in the mobility calculations are parallel and perpendicular to the current flow.

The DC simulations were carried out by first building the gate voltage to ensure channel formation and then by stepping up the drain voltage. Though the NMOS device physics is dominated by electron flow, the Newton's two-carrier simulation mode is used, as it is a requirement for RF simulations. A number of bias points with a small step-size are chosen and the simulation grids are regularly refined based on potential and electron concentration to accurately capture the DC and RF characteristics. The AC analysis is performed at each bias point (small-signal voltage amplitude is 2.5mV) in all the three two-port configurations, namely GD, GS and SD respectively, from 100MHz to 25.1GHz (chosen to be the same as measurement frequency range for ease of comparison). Finally the simulated Y-parameters of the different configurations are all scaled up by 100 to reflect those of a 100μm wide device for clear visualization of the trends vis-à-vis measured data. The three-port admittances are assembled as done before and the capacitances and conductance are also computed. The Medici input files have been included in the Appendix C.

The width of the measured SD-R device is 100μm, while the 2-D simulations assume a 1μm wide structure. Also, the measured SD-R device has a gate resistance of 5kΩ. We now need to find the appropriate value of gate contact resistance (say R_G) to use for the SD-R simulations. In order to scale up the simulated 1μm wide SD-R device so that it corresponds to the 100μm wide measured device, the simulated Y-parameters have to be multiplied by 100. The scaled up simulated device can be understood of, as being composed of a 100 parallel fingers, each of width 1μm and having a gate contact resistance of R_G. We know that the net resistance of n parallel resistances of R_G each is given by (R_G/n). In our case, n=100 and the net resistance required is R_G/n=5kΩ, which

yields R_G=500kΩ. Thus, the required gate contact resistance (R_G) for the SD-R simulations is about 500kΩ.

First the SD-R DC simulations are carried out and its characteristics are compared with those of the normal device to ensure device functionality. Next the AC analysis is carried out in the SD configuration to get the RF characteristics. The drain-bulk and source-bulk admittances are then extracted using the techniques described in Section 4.2.1, Chapter 4. The next section presents the junction admittance parameters extracted from the SD-R device simulations and measurements and validates the SD-R device functionality.

5.4 Extracted results from SD-R simulations and measurements

This section reports the extracted junction admittance parameters of the SD-R device from both simulations and measurements. The bias and frequency dependence of the physically extracted MOSFET junction capacitance and conductance have been reported here for the first time. A physics-based explanation for the behavior is also provided.

A very good correspondence has been obtained between the junction capacitances and conductance extracted from SD-R simulations and actual device measurements. Figure 5.1(a) and (b) show the simulated and measured values of c_{bs} respectively, at V_{GS}=3V and different drain biases. Figure 5.2(a) and (b) show similar trends of measured and simulated c_{bd} for similar bias conditions. As discussed in Chapter 3 the measured MOS device is comprised of eight source diffusion regions and only five drain diffusion regions (see Figure 3.1). Thus the measured bulk-drain capacitance is smaller than the bulk-source capacitance even at zero V_{DS}. The simulations have been carried out for a single finger transistor structure with one source diffusion and one drain diffusion, which

were then scaled up by a factor of 100. Thus the simulated trends show equal junction admittances at zero drain bias.

A look at the bias and frequency dependence of the extracted capacitances shows that, the simulated and actual measured trends of Figure 5.1(a)-(b) and Figure 5.2(a)-(b) share a broad agreement which can be well understood from the standpoint of device physics. Both the bulk-source and bulk-drain capacitances are composed of two components, namely the extrinsic junction and intrinsic capacitances. The extrinsic capacitances are dominant as they are much larger in magnitude. In Figure 5.1(a)-(b), the bulk-source capacitance gradually increases with the drain bias due to an increase in magnitude of its intrinsic component (c_{bsi}). This is because the source gains control over a greater fraction of the channel charge with the advent of saturation. The extrinsic junction capacitance (c_{bse}) is practically independent of V_{DS}.

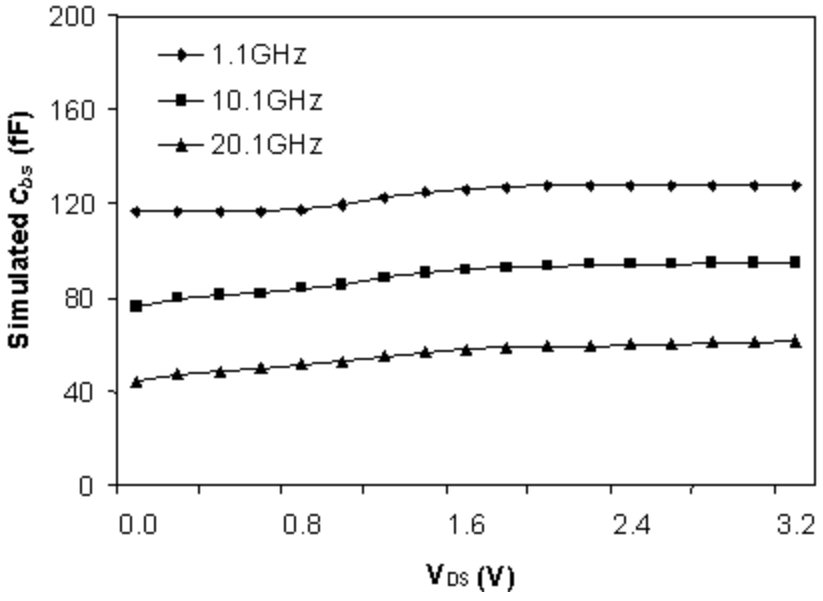


Figure 5. 1(a) Simulated bulk-source capacitance (V_{GS}=3V and V_{BS}=0V)

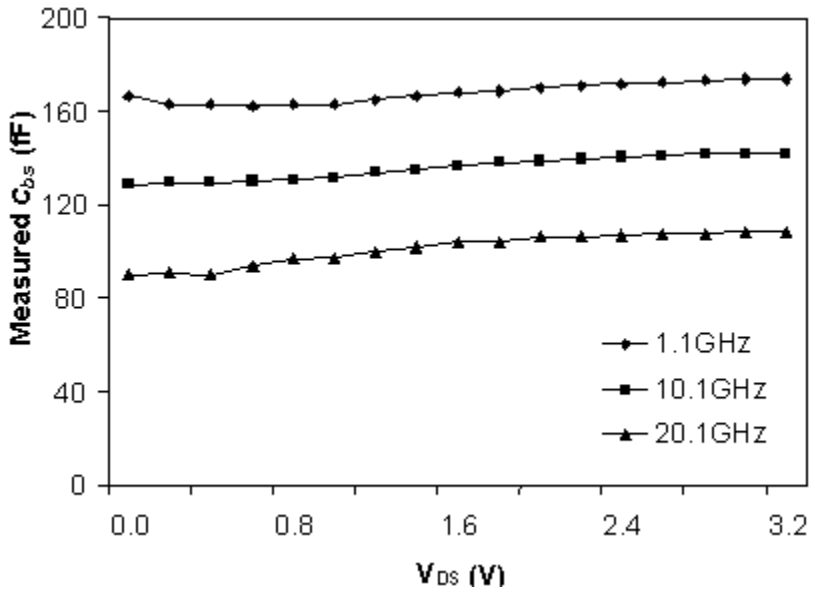


Figure 5. 1(b) Measured bulk-source capacitance (V_{GS}=3V and V_{BS}=0V)

As the V_{DS} increases, V_{DB} also increases, causing the widening of the drain-bulk junction's depletion region. Thus the extrinsic drain-bulk junction capacitance (c_{bde}) decreases significantly. The level of inversion on the drain side of the channel reduces with increasing V_{DS} and thus the intrinsic capacitance (c_{bdi}) also decreases. Thus Figure 5.2(a)-(b) shows a marked decrease in c_{bd} as the device enters saturation from the triode region. In deep saturation, the c_{bd} is almost equal to the extrinsic junction capacitance (c_{bde}) as c_{bdi} becomes negligibly small. The frequency dependence of the capacitance and conductance will be discussed in detail at a later section.

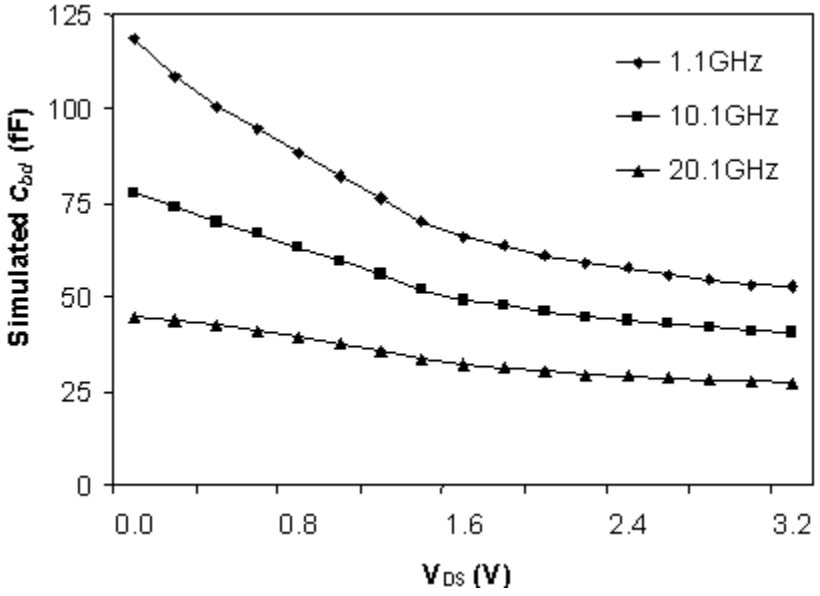


Figure 5. 2(a) Simulated bulk-drain capacitance (V_{GS}=3V and V_{BS}=0V)

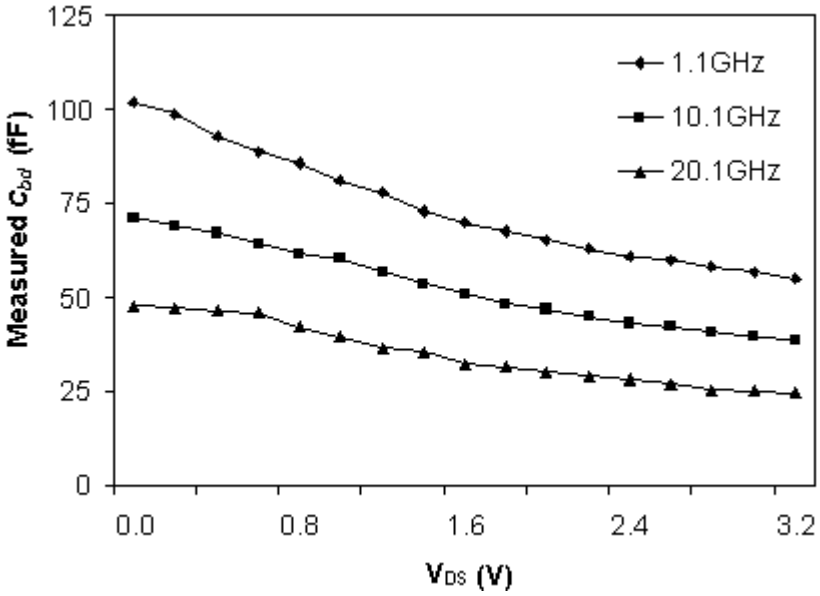


Figure 5. 2(b) Measured bulk-drain capacitance (V_{GS}=3V and V_{BS}=0V)

The g_{bs} and g_{bd} extracted from simulated and measured data are shown in Figure 5.3(a)-(b) and 5.4(a)-(b) respectively. The measured bulk-source conductance in Figure 5.3(b) is seen to be almost independent of V_{DS} at a given frequency. The simulated g_{bs} in Figure 5.3(a) shows a slight increase in g_{bs} with V_{DS} at 20.1GHz. This may be due to an

increase in the intrinsic conductance caused by a greater control of the source over channel charge. However we cannot compare this with the measurements, as the process simulations have not been optimized to exactly match the actual device.

The bulk-drain conductance in Figure 5.4(a)-(b) is negligibly small for all V_{DS} at low frequency (1.1GHz). For the higher frequency plots, g_{bd} decreases with increasing V_{DS}. The explanation for this trend is provided in the next section.

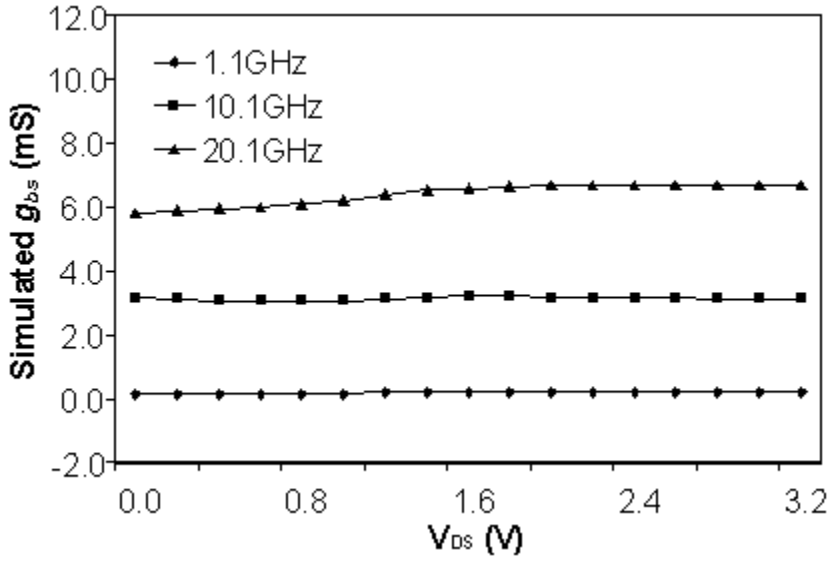


Figure 5. 3(a) Simulated bulk-source conductance (V_{GS}=3V and V_{BS}=0V)

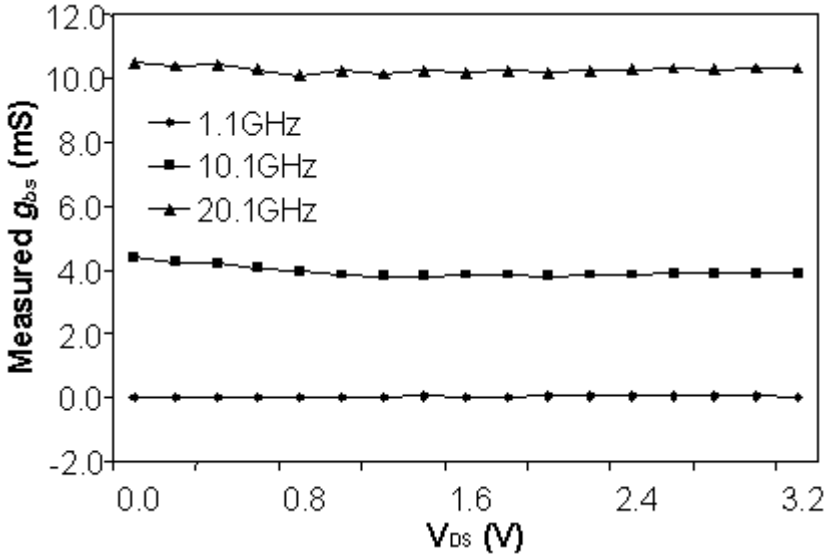


Figure 5. 3(b) Measured bulk-source conductance (V_{GS}=3V and V_{BS}=0V)

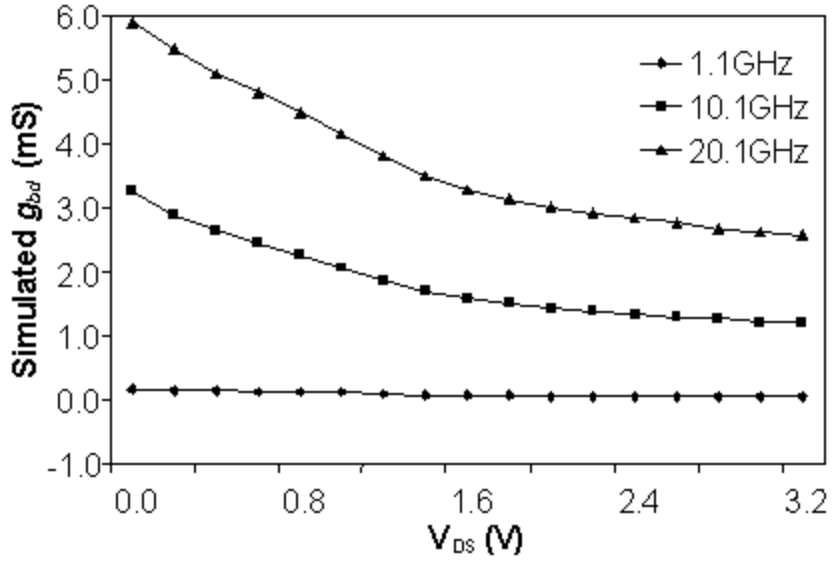


Figure 5. 4(a) Simulated bulk-drain conductance (V_{GS}=3V and V_{BS}=0V)

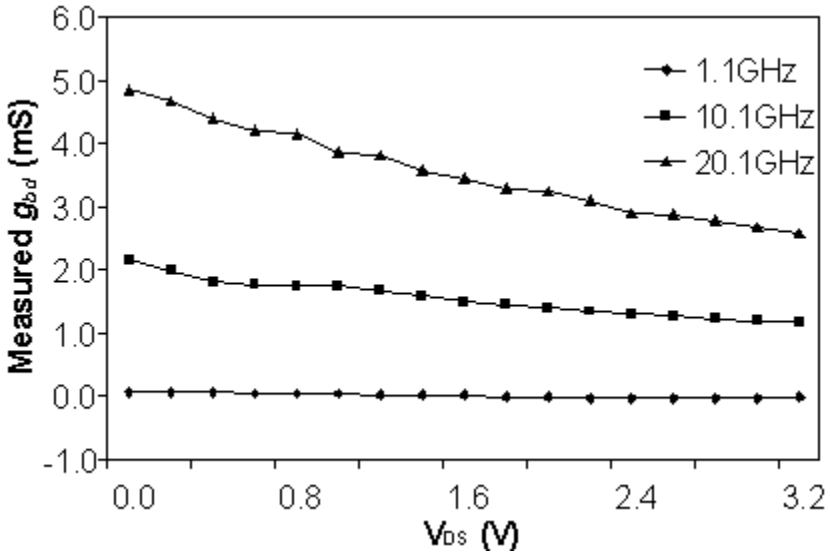


Figure 5. 4(b) Measured bulk-drain conductance (V_{GS}=3V and V_{BS}=0V)

The extracted junction admittance can be visualized as a junction capacitance (C_{BJ}) in series with the substrate resistance (R_{SUB}) as shown in Figure 5.5 [15]. The circuit elements (C_{BJ} and R_{SUB}) nomenclature uses capital letters to distinctly distinguish them from the extracted parameters. The circuit model of Figure 5.5 has been presented here for understanding only.

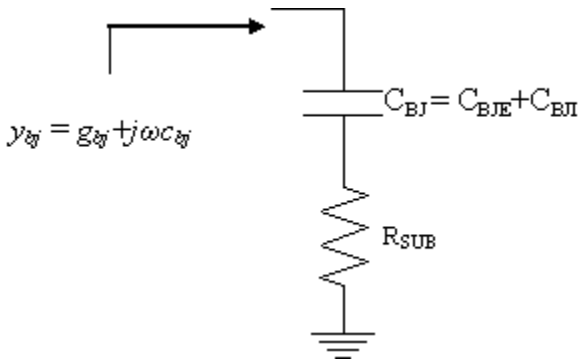


Figure 5. 5 Simple equivalent circuit for the junction admittance

The junction capacitance C_{BJ}, in the equivalent circuit model of Figure 5.5 is shown to include both the extrinsic (C_{BJE}) and intrinsic (C_{BJI}) capacitances and these are not to be confused with the c_{bse}, c_{bde}, c_{bsi} and c_{bdi} of the extracted admittances. The latter are

obtained directly by dividing the imaginary part of the extracted admittance by the angular frequency ($\omega=2\pi f$). Analysis of the simple circuit presented in Figure 5.5 yields (5.1) and (5.2).

$$g_{bj} = \frac{\omega^2 R_{SUB}^2 C_{BJ}^2}{1+\omega^2 R_{SUB}^2 C_{BJ}^2} \tag{5.1}$$

$$c_{bj} = j\omega\left[\frac{C_{BJ}}{1+\omega^2 R_{SUB}^2 C_{BJ}^2}\right] \tag{5.2}$$

The extracted conductance g_{bj} thus depends on the junction capacitance C_{BJ}. As the drain-bulk junction capacitance decreases with increasing V_{DS}, the extracted g_{bd}, shown in Figure 5.4, also decreases with V_{DS} for a given frequency. However, g_{bs} doesn't show much variation because the source junction capacitance is least affected by V_{DS}. The frequency dependent numerator in the RHS of (5.1) is very small at low frequencies. Thus, we find that, at 1.1GHz both g_{bs} and g_{bd} in Figure 5.3 and 5.4 are negligibly small. As the frequency increases, the numerator in (5.1) determines the value of g_{bj} because, in the denominator, we find that $\omega^2 R_{SUB}^2 C_{BJ}^2 << 1$ up to several GHz. Thus the conductance increases almost as the square of frequency. In the case of the capacitance, this simplistic analysis predicts a slowly decreasing c_{bj} as long as $\omega^2 R_{SUB}^2 C_{BJ}^2 << 1$, but much rapid decrease at higher frequencies, when this relation doesn't hold. This analysis to some extent explains the c_{bd} and c_{bs} reduction as well as g_{bs} and g_{bd} increase at higher frequencies.

We can infer from Figure 5.1 (in both the measurement and simulation plots), that the c_{bs} drops by about 50-60% as the frequency increases from 1.1GHz to 20.1GHz. From Figure 5.3 we observe that, between 10.1GHz and 20.1GHz, the bulk-source conductance

increases by more than 100% in magnitude. This significant variation may also be contributed by certain higher order effects, like the NQS effect and substrate coupling which are considered next.

The maximum cut-off frequency of a 0.35μm device at V_{GS}=3V is about 25GHz. The plots here are shown at three different frequencies, one in the quasi-static regime, the second where some amount of NQS is visible and the third point is chosen close to the f_t at about 20.1GHz where the NQS effect is dominating device behavior. The NQS effect causes a decrease in intrinsic capacitances (c_{bdi} and c_{bsi}) at higher frequencies. This is because the intrinsic capacitance is contributed by the channel charge and their response to applied signals at higher frequencies degrades on account of inertia (visualized in simple form as a series RC circuit described above). This causes a reduction in c_{bs} at all regions of operation, and affects c_{bd} only in the linear region, as c_{bdi} is negligibly small when the device enters saturation. So, in the case of c_{bd} in deep saturation, the entire frequency dependent variation is borne by the extrinsic capacitance only. As a result, the frequency dependent bulk-drain capacitance reduction in Figure 5.2 is more significant in the linear region.

The substrate itself cannot be considered as being purely resistive at higher frequencies. It exhibits capacitive coupling, which again significantly affects the extracted junction capacitance beyond a few GHz. Further, this simple capacitor-resistor equivalent circuit is not rigorously accurate as the substrate exhibits a distributed behavior. The substrate behavior also enhances the frequency dependent increase of the extracted conductance.

The extracted junction admittances will directly enable the accurate RF modeling of the junction and substrate behavior of the MOSFET. Thus we find that the SD-R device is very useful in extracting the on-state junction admittances. The measurement and simulation trends are very similar and agree with the behavior expected from device physics. They can be used for direct extraction of the other equivalent circuit model parameters from the normal device. The next chapter presents the results of the parameter extraction, the three-port capacitances from measurements and simulations, the NQS effect on device trans-conductance and the terminal charges as functions of both bias and frequency along with a discussion of their implications towards MOSFET modeling.

5.5 Summary

The process flow of a 0.35μm NMOS was simulated using the TCAD tool TSUPREM-4. The output mesh of the process simulation is used as input for device simulations in a 2-D TCAD simulator Medici. The DC simulations of the device are carried out. The RF simulations (AC Y-parameter analysis) are carried out in the GD, GS and SD two-port configurations of the device to generate the three-port admittance matrix of the MOSFET. The SD-R device simulations were also carried out in the SD configuration. The functionality of the SD-R device is validated. The junction admittances are also extracted.

The junction capacitance and conductance extracted from measured and simulated data are compared with respect to bias and frequency. The capacitance parameters decrease with frequency while the conductance parameters increase with frequency. The bulk-source capacitance shows a monotonous increase with drain bias. The bulk-drain capacitance shows a monotonous decrease with V_{DS}. At low frequency, both g_{bs} and g_{bd}

are nearly equal to zero at all drain bias. At higher frequency, the bulk-source conductance is more or less constant with drain bias while the bulk-drain conductance decreases monotonously with V_{DS}. The behavior of the extracted components is also explained on the basis of device physics.

Chapter 6: Results and Discussion

This chapter presents the results of measurements, extraction and simulations. The initial focus is on the extraction routine and a brief discussion follows with regard to its overall consistency through comparison of equivalent circuit model parameters obtained from different configurations. The extrinsic parameters obtained from the normal and SD-R devices are also compared. The next objective is to validate the three-port characterization approach using a comparison of the main diagonal elements (y_{gg}, y_{dd} and y_{ss}) obtained from probe de-embedded data in different two-port configurations. The discussion then shifts its focus towards the three-port data and investigates the bias and frequency dependence of the terminal capacitance and trans-conductance. The non-quasi-static effect on the trans-conductance at RF is also investigated. This is followed by discussion on the capacitance and conductance trends obtained from device simulations. The chapter concludes with a description of the terminal charges extracted from the three-port data as functions of bias and frequency.

6.1 Consistency of the extraction scheme

The MOSFET has been represented by an RF equivalent circuit. So the equivalent circuit model parameters extracted from different two-port configurations should match reasonably well to ensure the consistency of extraction. Using the current extraction scheme the parameters y_{gs}, y_{gd}, y_{sd} and y_m obtained from the GD, GS and SD configurations match reasonably well up to 15GHz. Figure 6.1-6.4 show the match obtained in different equivalent circuit model parameters at V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V.

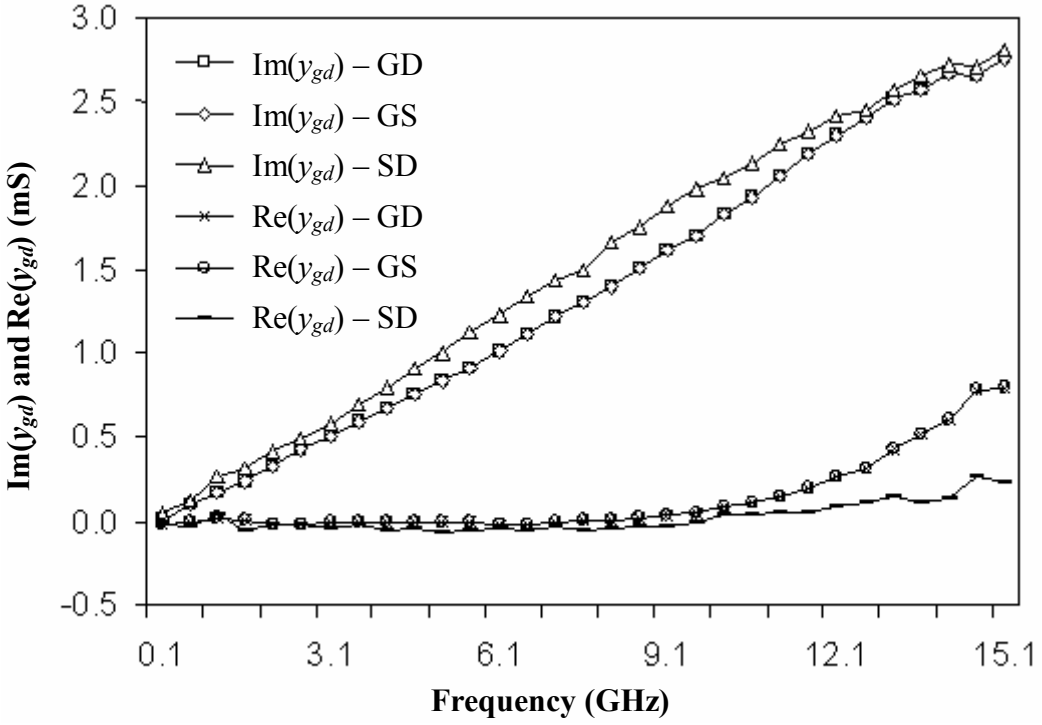


Figure 6. 1 Model-based y_{gd} (V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V)

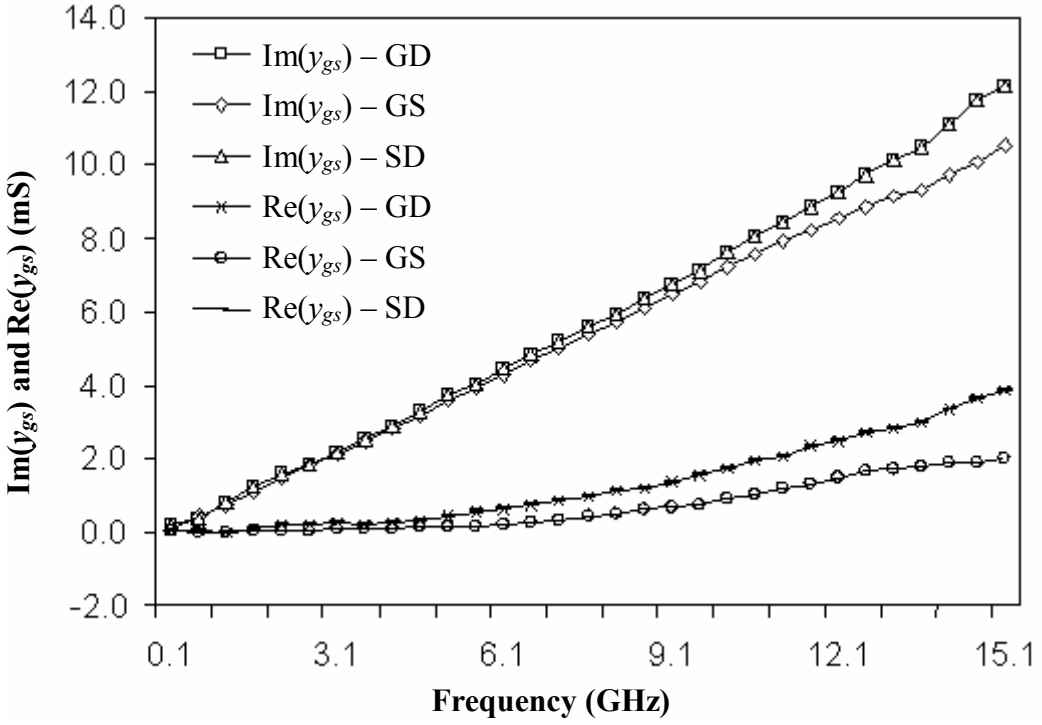


Figure 6. 2 Model-based y_{gs} (V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V)

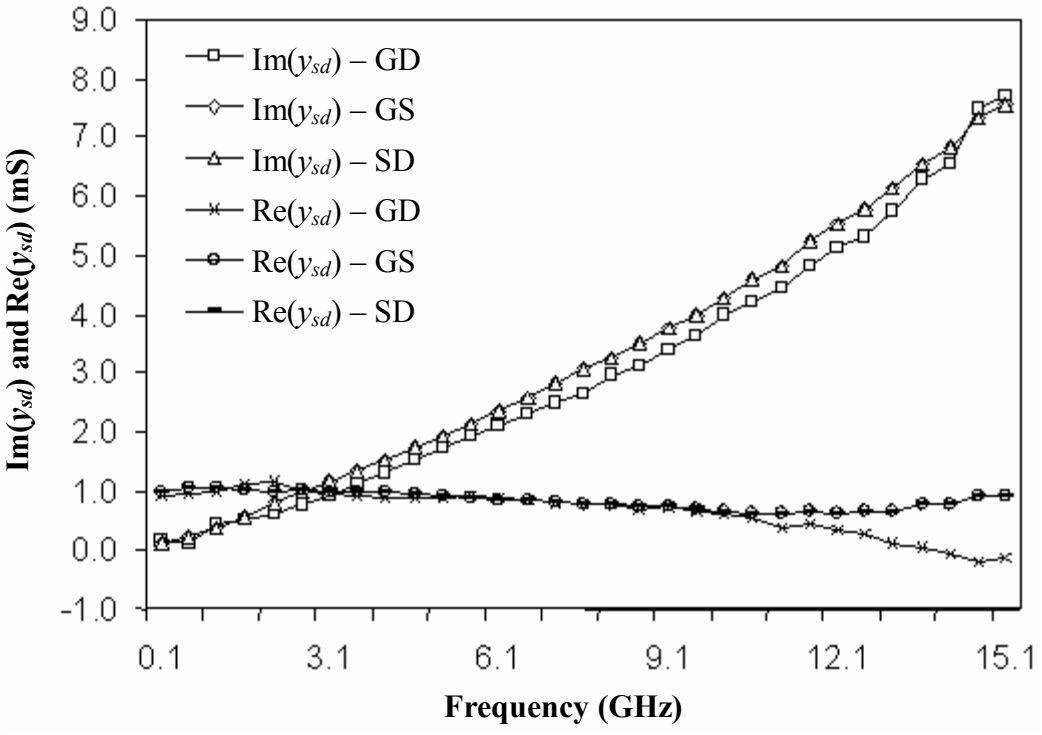


Figure 6. 3 Model-based y_{sd} (V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V)

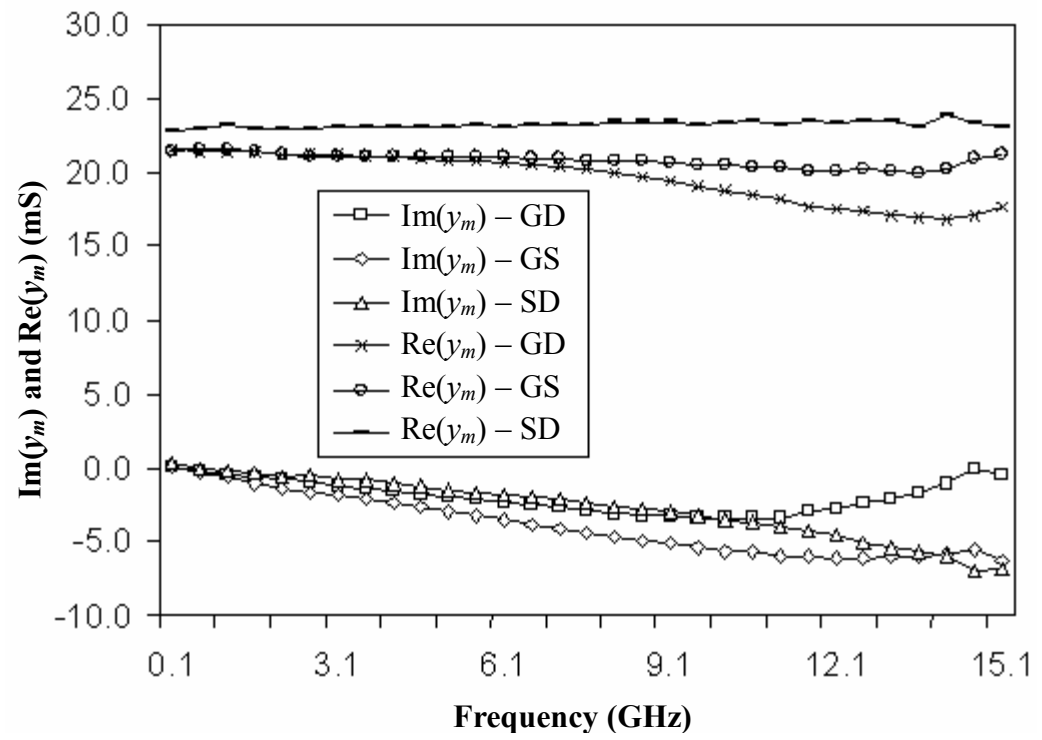


Figure 6. 4 Model-based y_m (V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V)

Some difference does arise in the extracted equivalent circuit model parameters from different configurations. This is because three of the model parameters namely, y_{mb}, y_{bs} and y_{bd}, were obtained from the SD-R device and are used in the GD, GS and SD configurations to extract the remaining equivalent circuit model parameters (y_{gs}, y_{gd}, y_{sd} and y_m). Device-level variations may induce some deviations in these parameter values.

Further, the device measurements are very extensive, covering 17x17x17 bias points (sweeping gate, drain and bulk biases) for 51 frequencies in each two-port configuration. Thus, in order to maintain contact consistency and repeatability of RF characteristics, we had to use three different devices for each of the configurations viz. GD, GS and SD respectively. This was necessitated by the bond pads getting damaged due to repetitive and prolonged probing, which affected the quality of the probe contacts. Without satisfactory on-wafer contact, the RF measurements will not be reliable and the experiment cannot succeed. This approach also leads to some device level variations in the equivalent circuit model parameter values. This can be inferred from the slight difference observed in the real part of y_m in Figure 6.4 even at low frequencies. Re(y_m) models the trans-conductance g_m and thus can vary slightly between devices in the same lot. Similar observations can be made about the variation of the channel conductance (real part of y_{sd}) at higher frequencies. Neglecting y_{gb} can also be the cause for the slight high frequency variations in the modeling of y_{gd} and y_{gs} obtained from different configurations.

But the reasonably close agreement (within intra-wafer device-level variations) justifies the assumptions. The overall trends are conserved well up to about 15GHz. So the extraction routine is found to be quite consistent for all practical purposes.

6.1.1 Comparison of extrinsic model parameters

An interesting way to verify the proper functionality of the SD-R device is to compare the junction admittances extracted in off-state conditions, with the corresponding extrinsic admittances obtained from the normal device (SD configuration) using the procedure described in Section 4.4 of Chapter 4. A very good match has been obtained between the extracted y_{bd} and y_{bs} values as shown in Figure 6.5 and 6.6 respectively.

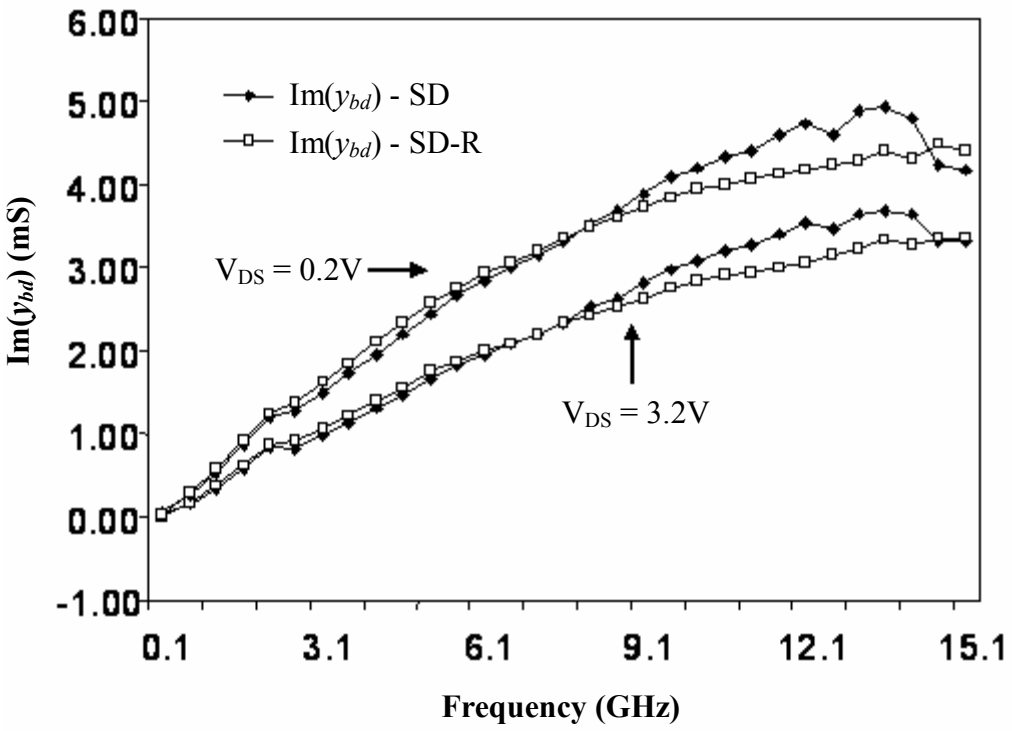


Figure 6. 5 Plot of y_{bd} from SD and SD-R in off-state (V_{GS}=0V and V_{BS}=0V)

Figure 6.5 shows the Imaginary part of bulk-drain admittance Im(y_{bd}) extracted from the SD and SD-R device at two different drain biases, both of which exhibit good match (error is within 10% up to 15GHz). Similarly the Im(y_{bs}) also exhibits excellent match in Figure 6.6. The real part Re(y_{bs}) does display more variation beyond 10GHz which may come from device level variations. The results confirm the utility of the SD-R device as

an excellent alternative for direct extraction of the junction admittances which can be utilized in the on-state parameter extraction of the device, as done in this work (extracted trends from the on-state simulated and measured data were also shown to be similar in Chapter 5).

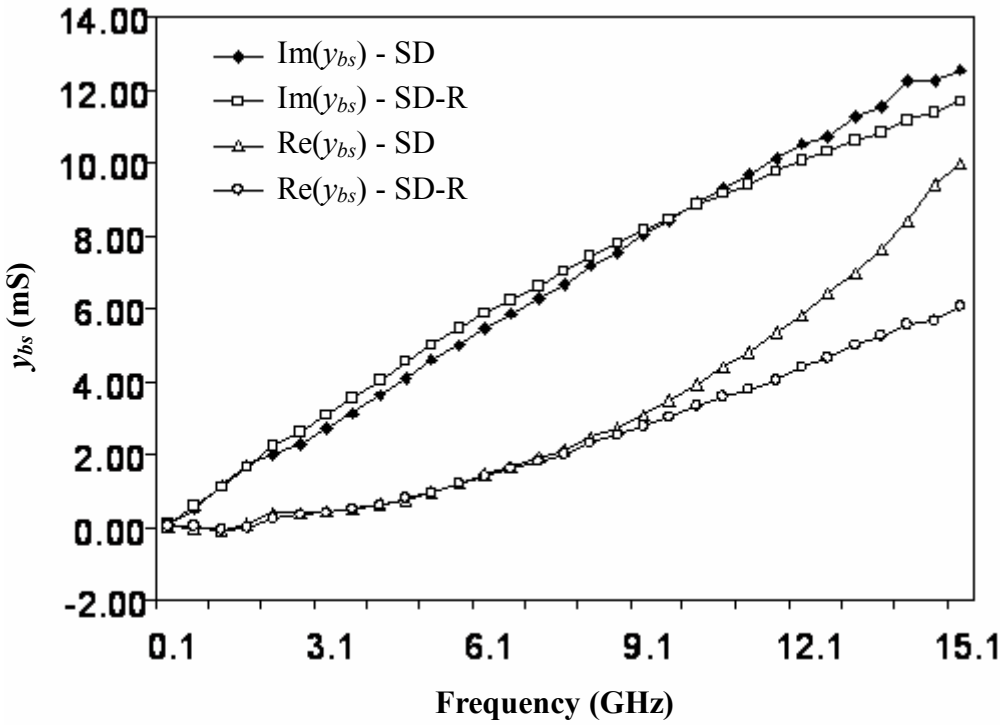


Figure 6. 6 Plot of y_{bs} from SD and SD-R in off-state (V_{GS}=V_{BS}=0V and V_{DS}=3.2V)

Thus we have examined the consistency of the extraction methodology for both the on and off-state of the MOSFET. The next section seeks to validate the three-port characterization.

6.2 Validation of the three-port characterization

As discussed in Section 2.2, the main diagonal elements (y_{gg}, y_{dd} and y_{ss}) of the 3x3 MOS admittance matrix are each obtained from two different two-port configurations. The admittance elements obtained from the probe de-embedded two-port parameters

exhibit a much better match than those from uncorrected data, up to about 15GHz. The data in Figure 6.7-6.12 have been obtained at a bias of V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V. The Re(y_{gg})_pd obtained after probe de-embedding, shown in Figure 6.7, indicates more than 75% reduction in absolute error between admittances from GD and GS configurations, over the uncorrected data (Re(y_{gg})) up to 15GHz.

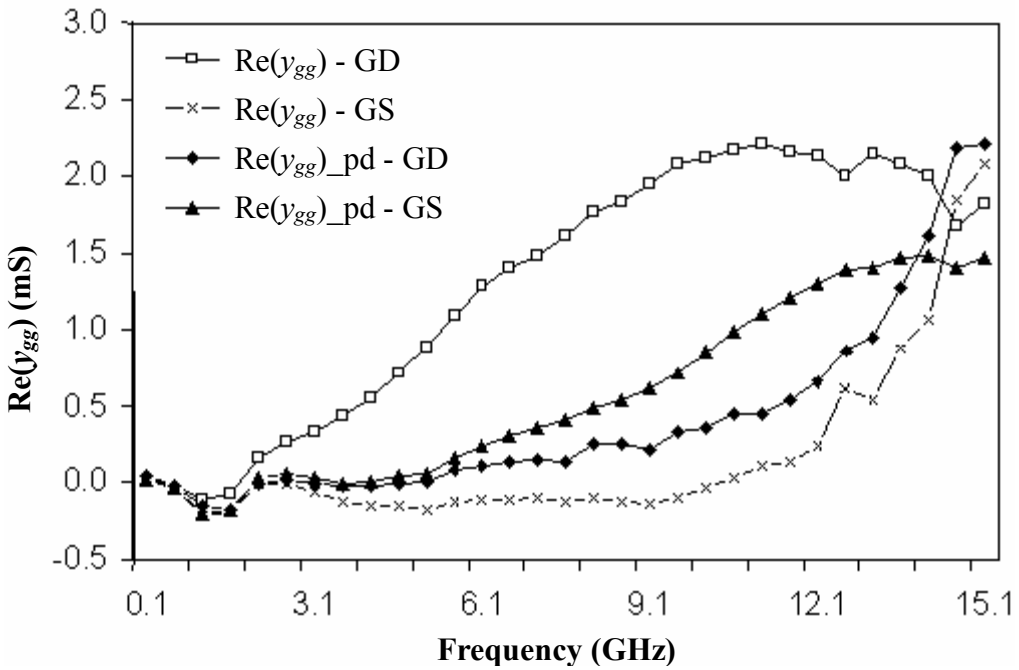


Figure 6. 7 Real part of y_{gg} from GD and GS ("_pd" indicates probe de-embedded data)

In Figure 6.8, the Im(y_{gg})_pd obtained after de-embedding the probe impedance, shows excellent match over the entire frequency range and results in 80% error reduction over the uncorrected data (Im(y_{gg})) even at 15GHz. One can also physically appreciate the effect of probe de-embedding, especially in the Im(y_{gg})_pd from GD configuration. As the probe impedance is predominantly inductive in nature (around 400pH beyond 1.1GHz), its removal at the source terminal (third port) will lead to a remarkable increase

in the capacitive component of the admittance looking into port 1 (G-B), at higher frequencies.

But probe de-embedding doesn't produce as strong an effect in the Im(y_{gg})_pd from GS configuration because, for the bias point in consideration (V_{GS}=3V, V_{DS}=3.2V and V_{BS}=0V) the transistor is in deep saturation and y_{gd} (which is barely the overlap admittance now) is much smaller than y_{gs}. Thus removing the probe inductance at the drain terminal doesn't produce any significant change in admittance looking into port 1 (G-B). The model representation and analysis, which has been described in Section 4.3 of Chapter 4 is useful in this interpretation.

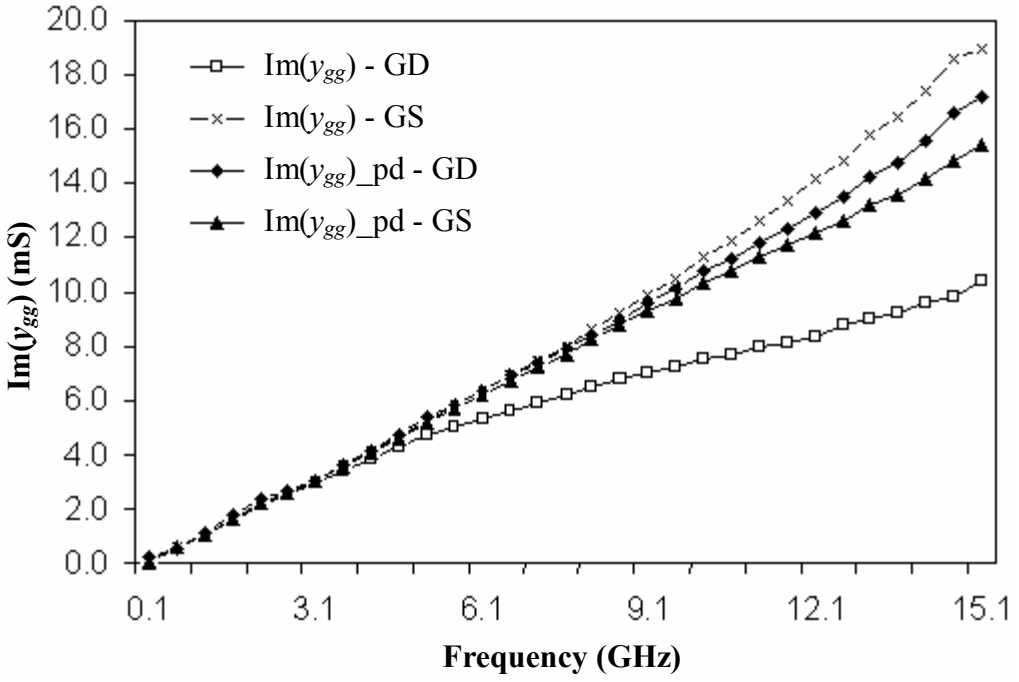


Figure 6. 8 Imaginary part of y_{gg} from GD and GS ("_pd" - probe de-embedded data)

The Re(y_{ss}) in Figure 6.9 shows consistent improvement in matching after probe de-embedding (Re(y_{ss})_pd), indicating 30% error reduction beyond 10GHz. Figure 6.10 shows a very interesting phenomenon and profound implications of corrected

measurements. The uncorrected data, Im(y_{ss}), starts decreasing at about 10GHz and the y_{11} from SD (Im(y_{ss}) - SD) even becomes negative beyond 14GHz. This reduction in magnitude of Im(y_{ss}) is actually caused by the heavy inductance of the probe at the third port and affects both the GS and SD configurations. The probe de-embedding corrects the data and restores the capacitive nature up to a much higher frequency range. Physically, the bulk-source, gate-source and source-drain admittances and trans-admittances contribute to y_{ss} and thus its imaginary part is expected to remain capacitive. The difference between the admittances from two configurations is attributed to device level variations.

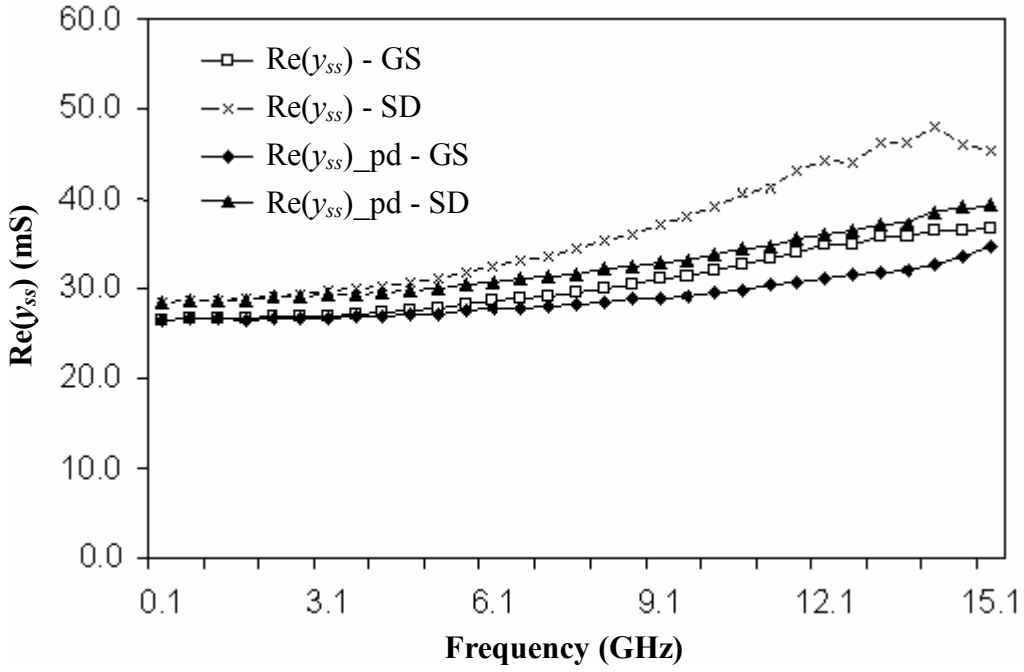


Figure 6. 9 Real part of y_{ss} from GS and SD ("_pd" - probe de-embedded data)

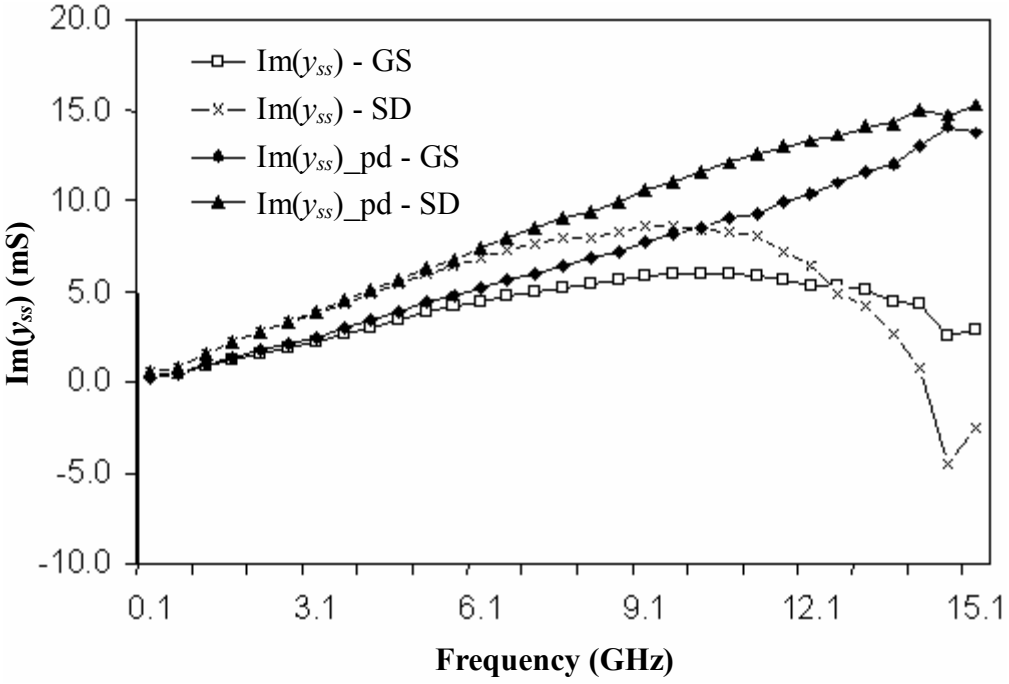


Figure 6. 10 Imaginary part of y_{ss} from GS and SD ("_pd" - probe de-embedded data)

Figure 6.11 shows the Re(y_{dd}) obtained from GD and SD configurations. The probe de-embedded data, Re(y_{dd})_pd, shows excellent match as compared with the uncorrected data. The error reduction is more than 70% beyond 6GHz.

The corrected data Im(y_{dd})_pd in Figure 6.12 also shows excellent match over the entire frequency range and de-embedding the probe impedance results in 90% error reduction over the uncorrected Im(y_{dd}) even at 15GHz! The overall match enjoyed by the main diagonal elements obtained from the probe de-embedded two-port Y-parameters confirms that they are indeed the true two-port parameters of the MOSFET. Thus the construction of the three-port Y-matrix by suitably assembling these two-port Y-parameters is also validated.

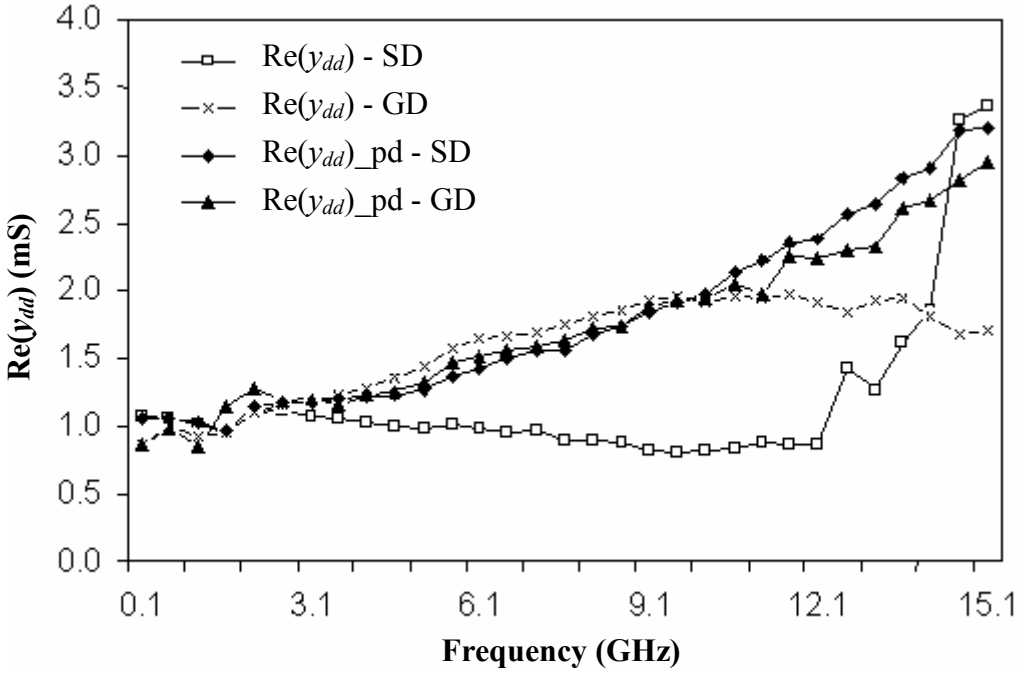


Figure 6. 11 Real part of y_{dd} from SD and GD ("_pd" - probe de-embedded data)

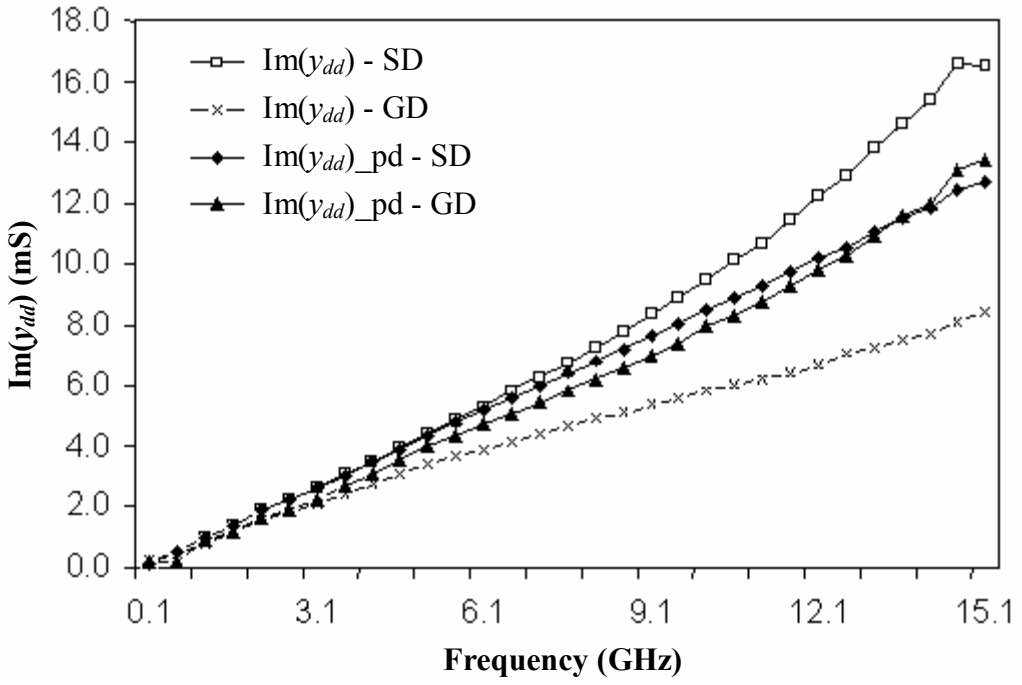


Figure 6. 12 Imaginary part of y_{dd} from SD and GD ("_pd" - probe de-embedded data)

The next section shows the three-port terminal capacitances and conductance of the MOSFET obtained from its three-port characterization data as well as device simulations.

6.3 Three-port terminal capacitance and conductance

There are not many reports on the measured data about the full capacitance matrix as a function of bias and frequency for the MOS transistor. Only analytical results [43] and some low frequency measured data [44] have been reported in literature. The imaginary part of the three-port admittance parameters obtained as described in Chapter 4, when divided by the angular frequency ($\omega=2\pi f$), directly yields the measured capacitance coefficients. The effect of frequency on the measured capacitance coefficients is also reported here for the first time. The capacitances normalized with respect to maximum c_{gg} are shown as a function of drain bias at three different frequencies at V_{GS}=3V in Figure 6.13-6.21. The variations of capacitances with respect to bias are similar to the low frequency analytical plots given in [43]. It is important to mention that the analytical model in [43] presents the intrinsic transistor capacitances only, while Figure 6.13-6.21 depicts the total capacitances, which include the extrinsic junction and overlap capacitances.

There are differences in the trends of variation between the measured and analytical data [43] in the case of three of the capacitances, namely c_{dg}, c_{dd} and c_{ds} (discussed in Section 6.3.1). All the other capacitances show a very good correspondence between measured and simulated or analytical trends [43]. The behavior of c_{dg} and c_{dd} in the linear region differs considerably from the reported analytical results [43]. Figure 6.16 shows an initial fall in c_{dg} while Figure 6.17 depicts an initial rise in c_{dd} in the linear region of device operation. This is unlike the simulated (Figure 6.22) and analytical results.

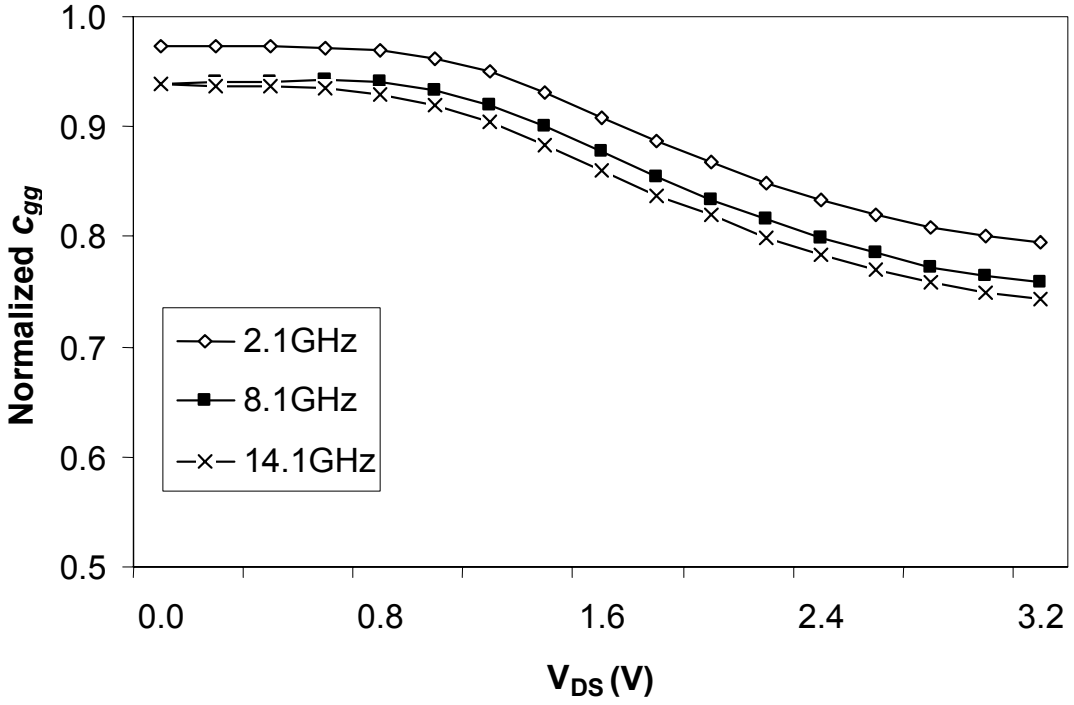


Figure 6. 13 Normalized c_{gg} (V_{GS}=3V, V_{SB}=0V)

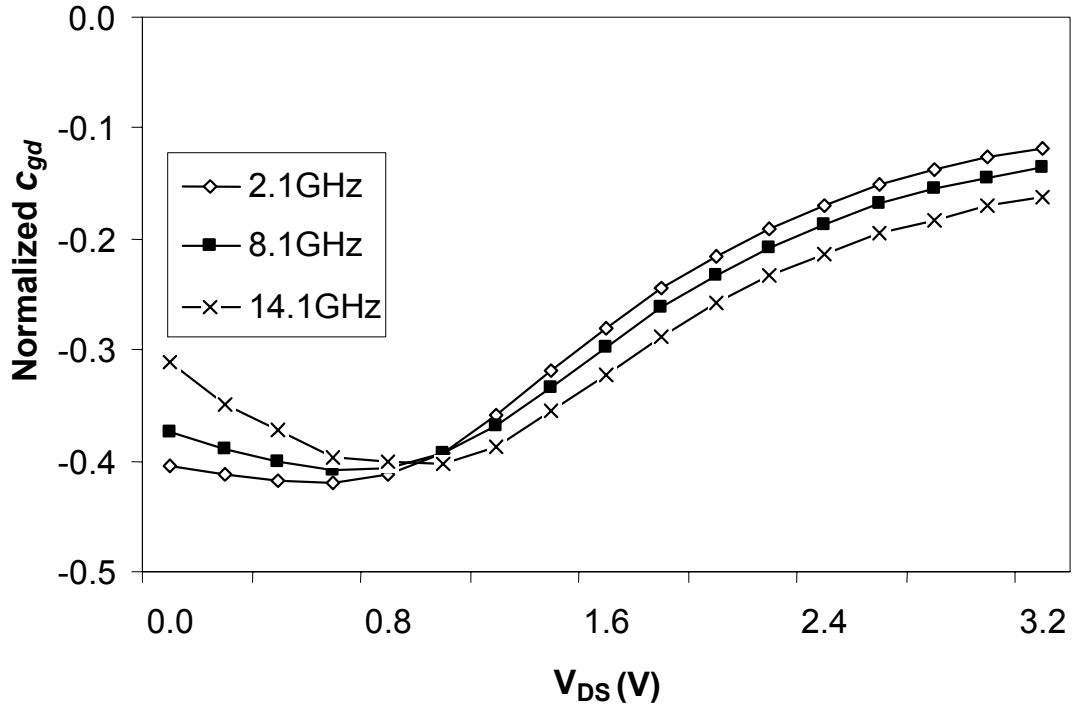


Figure 6. 14 Normalized c_{gd} (V_{GS}=3V, V_{SB}=0V)

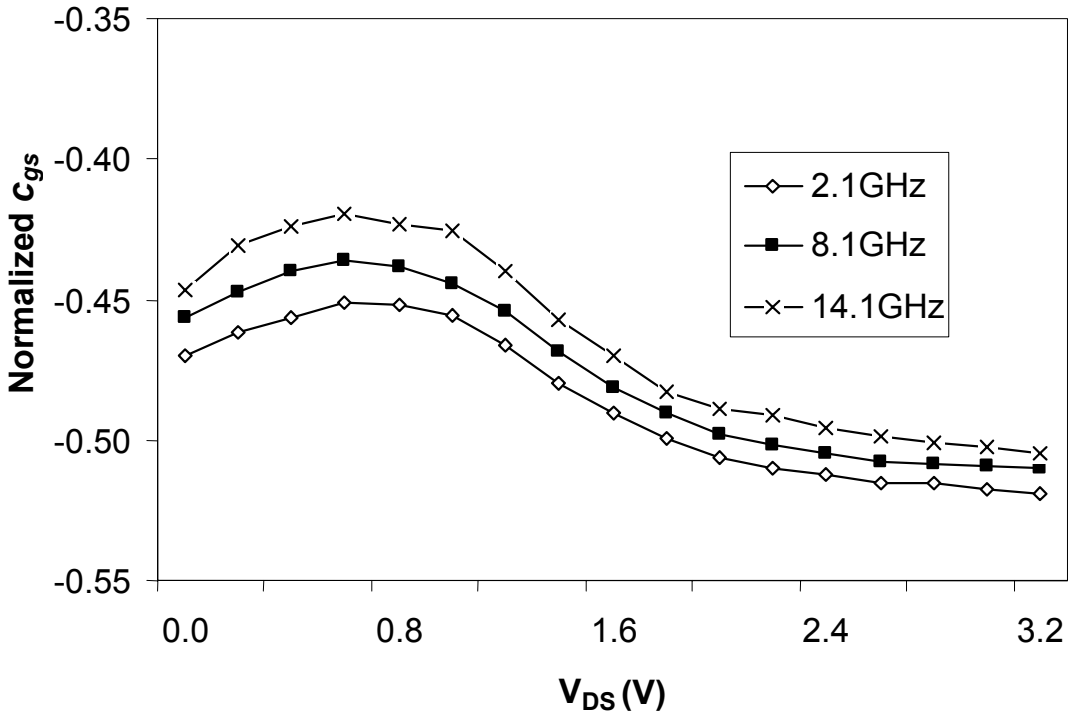


Figure 6. 15 Normalized c_{gs} (V_{GS}=3V, V_{SB}=0V)

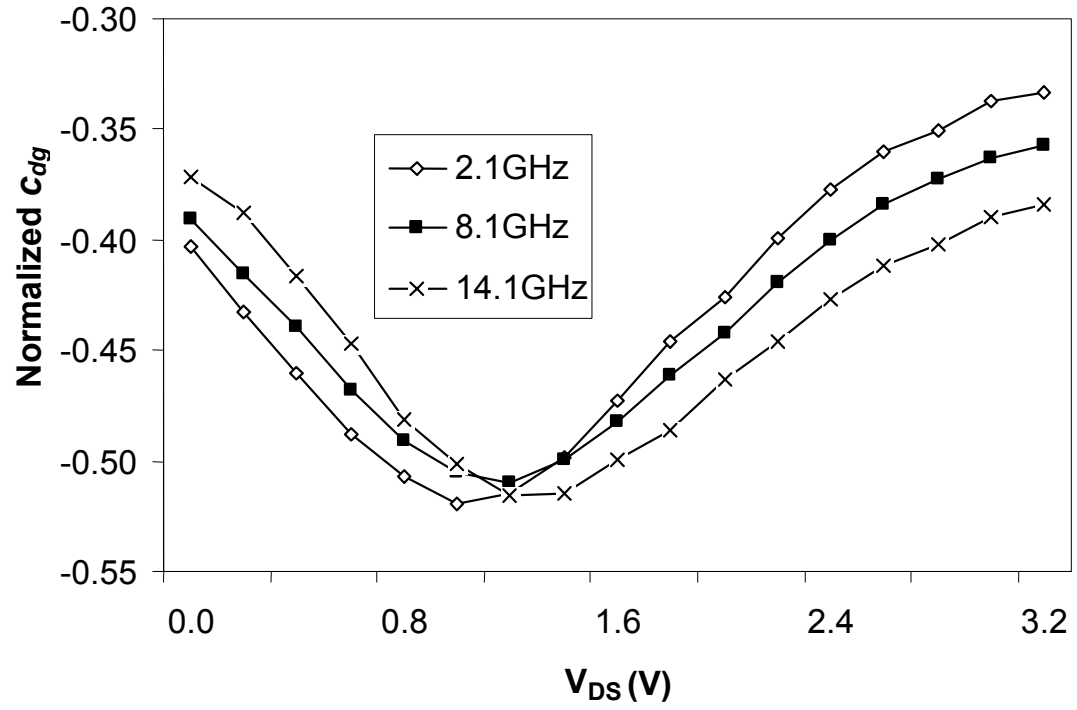


Figure 6. 16 Normalized c_{dg} (V_{GS}=3V, V_{SB}=0V)

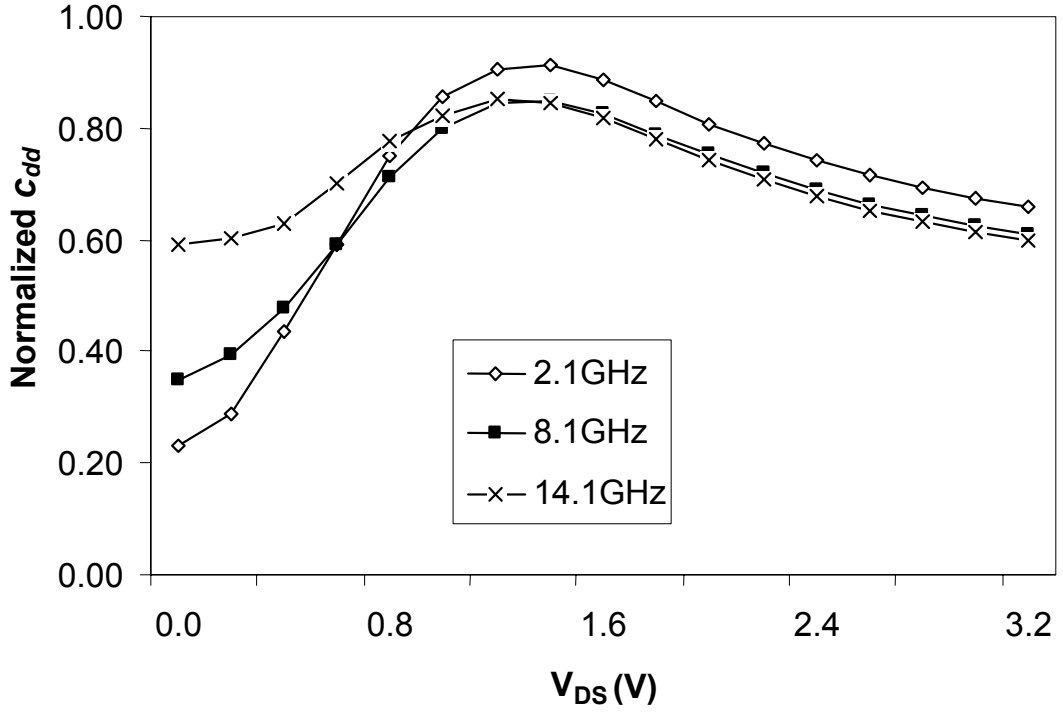


Figure 6. 17 Normalized c_{dd} (V_{GS}=3V, V_{SB}=0V)

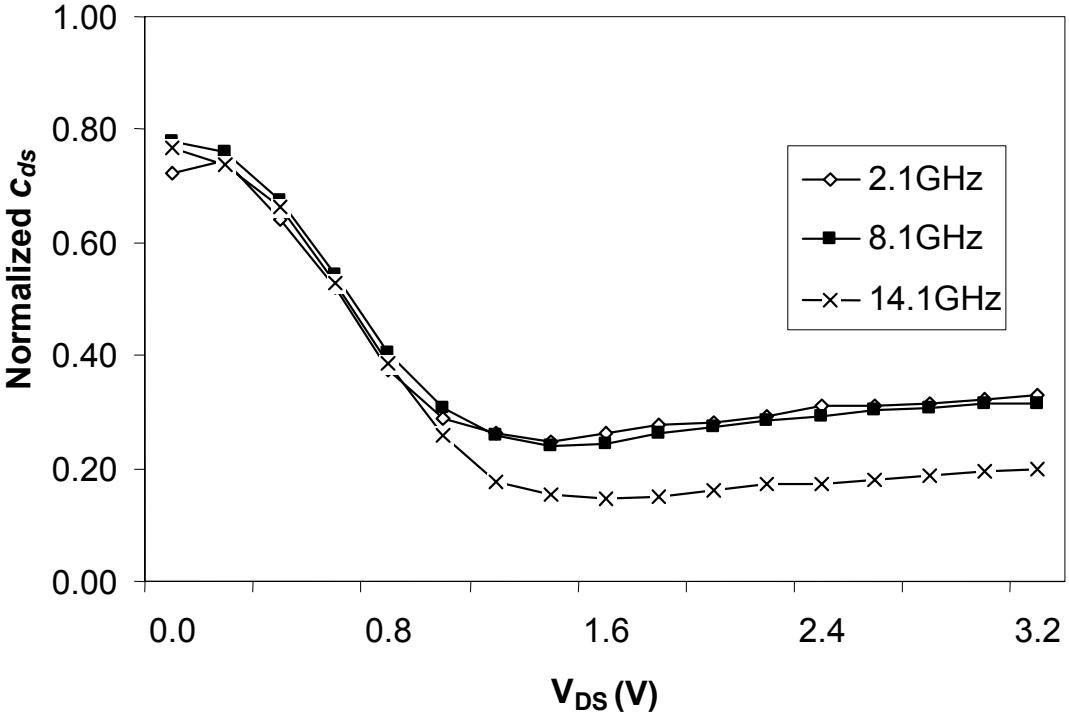


Figure 6. 18 Normalized c_{ds} (V_{GS}=3V, V_{SB}=0V)

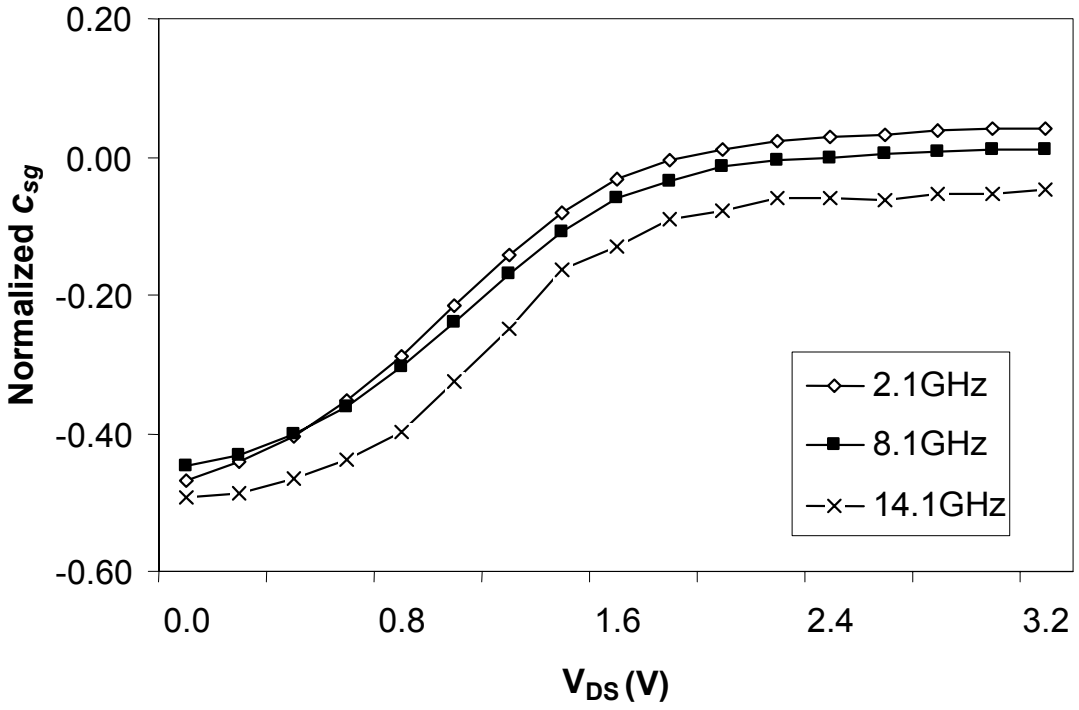


Figure 6. 19 Normalized c_{sg} (V_{GS}=3V, V_{SB}=0V)

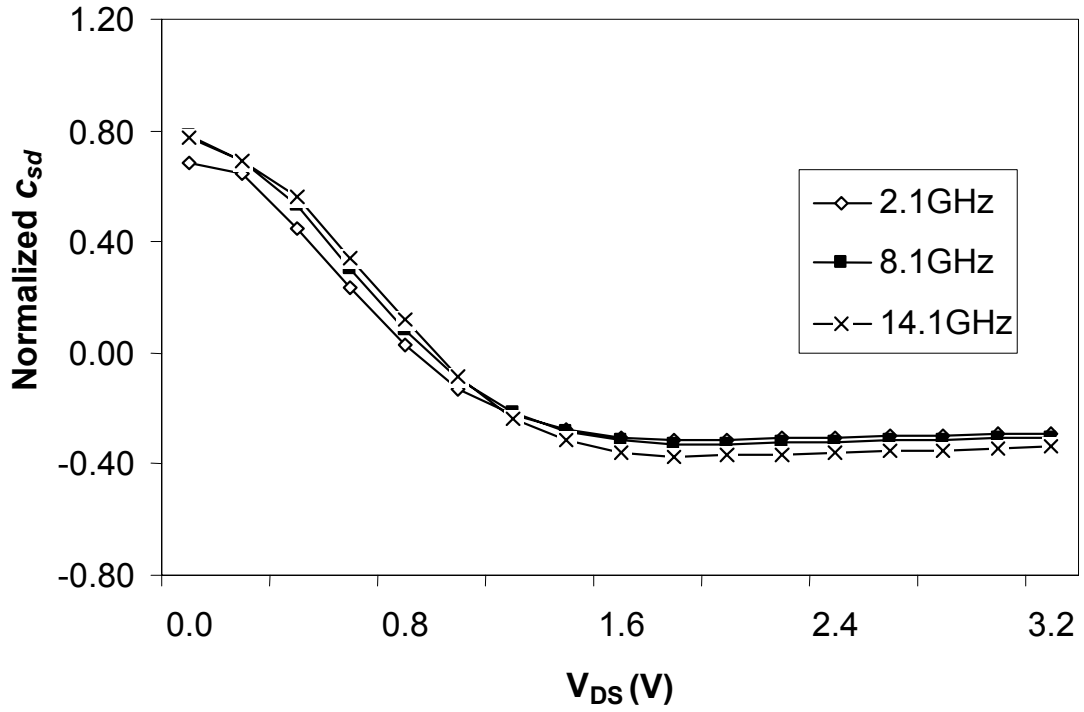


Figure 6. 20 Normalized c_{sd} (V_{GS}=3V, V_{SB}=0V)

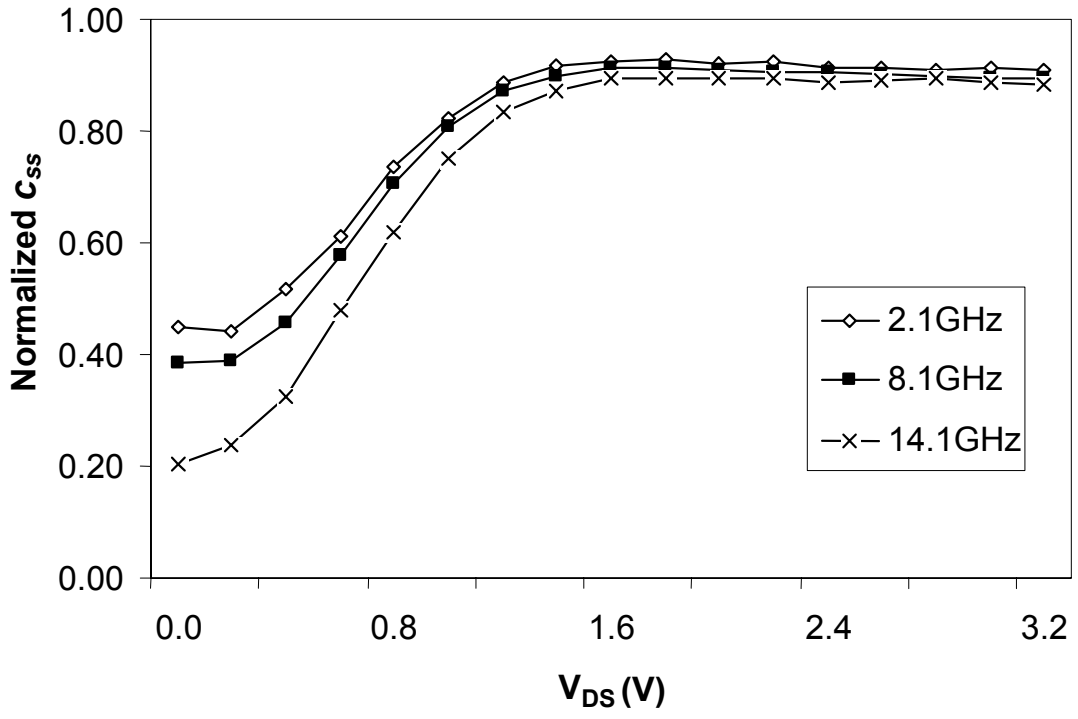


Figure 6. 21 Normalized c_{ss} (V_{GS}=3V, V_{SB}=0V)

Figure 6.22 shows a consolidated plot of the simulated terminal capacitances of a 0.35μm device normalized with respect to maximum c_{gg}, as a function of V_{DS} for V_{GS}=3V at 1.1GHz. The Medici simulation results are shown here as a guideline to validate the measured capacitances. The device simulations are not optimized to match measurements, as exact process data were not available, as mentioned in Chapter 5.

In the case of both measurements and simulations c_{sd} (Figure 6.20 and 6.22) falls with increasing V_{DS} and once the device enters saturation it remains constant. This is because as the V_{DS} increases shifting the device operation closer to saturation, it reduces the level of inversion at the drain end of the channel and increasingly isolates the intrinsic drain from the rest of the device. Thus, with increasing V_{DS}, the intrinsic component c_{sdi} reduces in magnitude and becomes negligible in deep saturation leaving only the extrinsic fringing component c_{sde} to be seen, which is independent of V_{DS}.

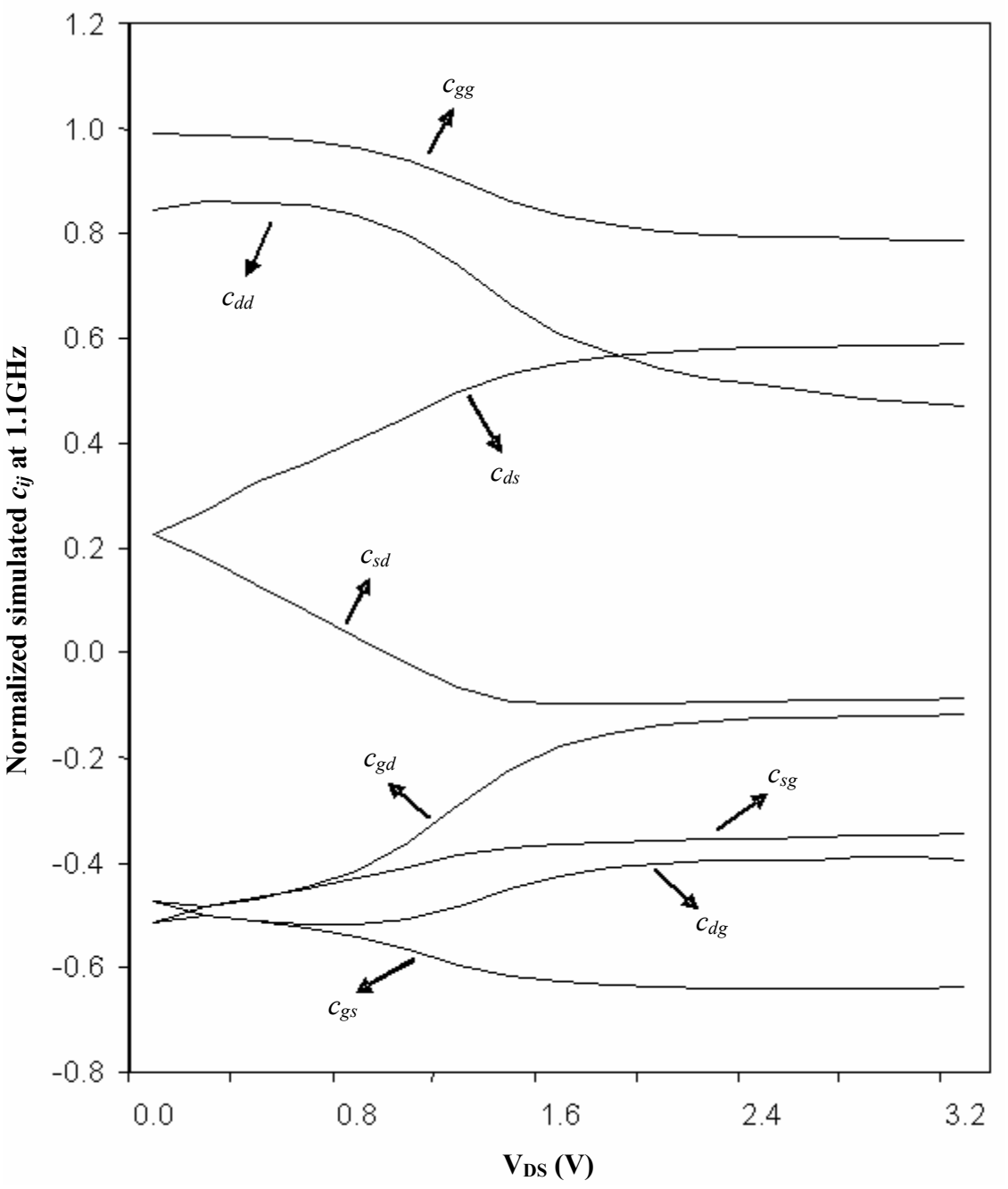


Figure 6. 22 Normalized c_{ij} of a 0.35µm MOSFET from Medici simulations (V_{GS}=3V, V_{SB}=0V)

A similar argument holds good to explain the bias dependent variation of c_{gd} in Figure 6.14. In the deep saturation region c_{gd} is dominated by the gate-drain overlap component.

Both analytical results and simulations (Figure 6.22) report only an increase in the c_{ds} as the drain bias increases. The measured c_{ds} (Figure 6.18) variations of the 0.35µm device are somewhat different. The measured c_{ds} falls first with V_{DS}, and later shows a marginal increase. The possible cause for this variation is discussed in Section 6.3.1. In the c_{ds} obtained from the 1µm device measurements, this fall is much lesser, as shown in Figure 6.23. For the 1µm device, the c_{ds} starts increasing significantly at higher V_{DS} resembling simulated characteristics and analytical results. Still, the variations at lower V_{DS} merit a further investigation.

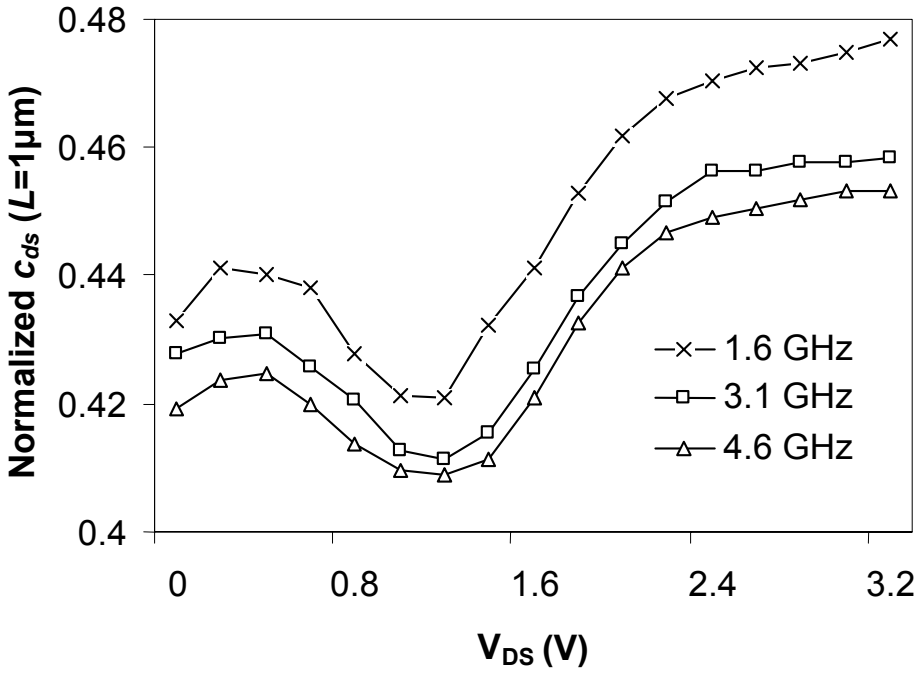


Figure 6. 23 Normalized c_{ds} measured from 1µm device (V_{GS}=3V, V_{SB}=0V)

6.3.1 Differences in measured terminal capacitances

The measured S-parameters and the corresponding admittances are all complex quantities. Whenever the real part of a complex number (say, $a+jb$) is much larger in magnitude than its imaginary part, the phase of the complex quantity ($tan^{-1}(b/a)$) is very

close to zero. This means that even a slight uncertainty in the measured phase of the complex admittance (converted from S-parameters) translates into a large percentage error in its comparatively small imaginary part. As the terminal capacitances are directly obtained from the imaginary part of the measured admittances, the uncertainty in their values is strongly determined by the relative magnitude of the associated conductance.

We have observed that in the case of all three measured terminal capacitances (c_{ds}, c_{dd} and c_{dg}) of the 0.35μm device, whose behavior is different from simulated or analytical trends [43], the magnitude of the associated conductance (g_{ds}, g_{dd} and g_{dg} respectively) is much more dominant compared to the imaginary part, over the bias ranges in which the difference arises. Now at low frequencies, the GPG probe exhibits a large shunt capacitance (~120pF) and acts like an ideal AC short as discussed in Chapter 3. So for this analysis, the measured data at low frequency (1.1GHz) without probe de-embedding is used.

Figure 6.24-6.26 shows a comparison of the magnitudes of real and imaginary parts of y_{dg}, y_{dd} and y_{ds} obtained from measured data at 1.1GHz. It is clear that the imaginary part of the admittances is much smaller than the associated conductance, implying a large measurement uncertainty in these capacitances even for slight phase variations. For example, from Figure 6.25 we expect maximum uncertainty in the imaginary part of y_{dd} in the linear region and correspondingly we observe disagreement in c_{dd} trends only in the linear region (Figure 6.17 and Figure 6.22). Similarly the imaginary component of y_{ds} in Figure 6.26 is insignificantly smaller compared to the measured conductance at all biases. In the linear region the conductance is still higher. Thus the measured c_{ds} exhibits differences from simulations at all V_{DS} (Figure 6.18 and Figure 6.22).

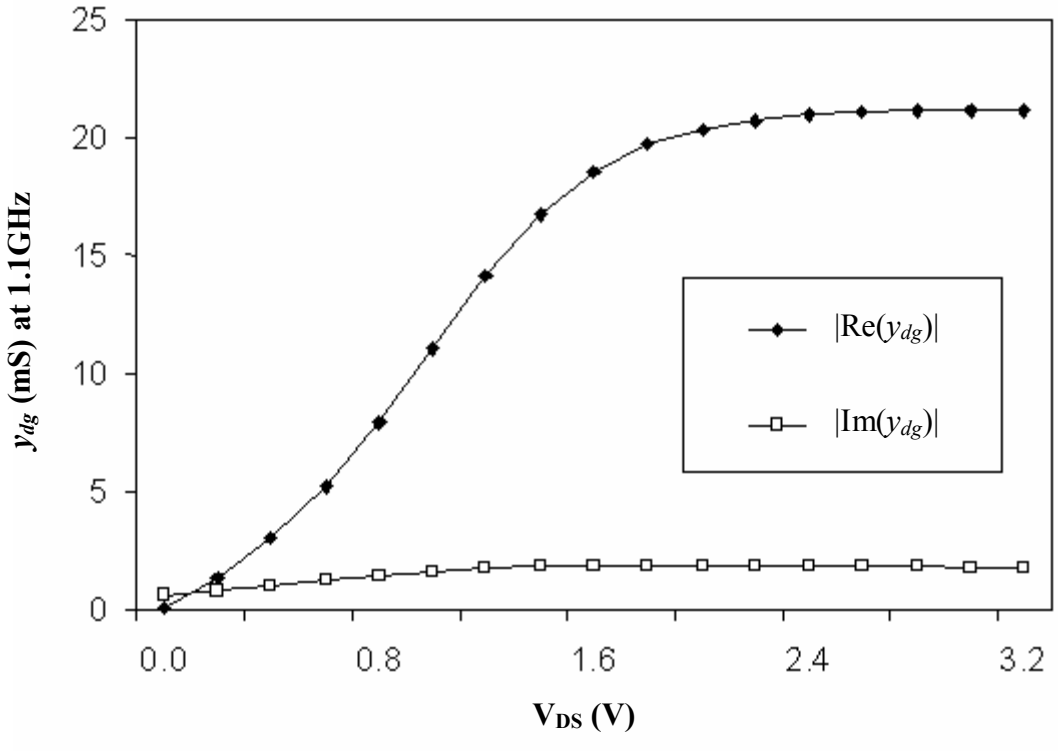


Figure 6. 24 Magnitude of measured Re(y_{dg}) and Im(y_{dg}) (V_{GS}=3V, V_{SB}=0V)

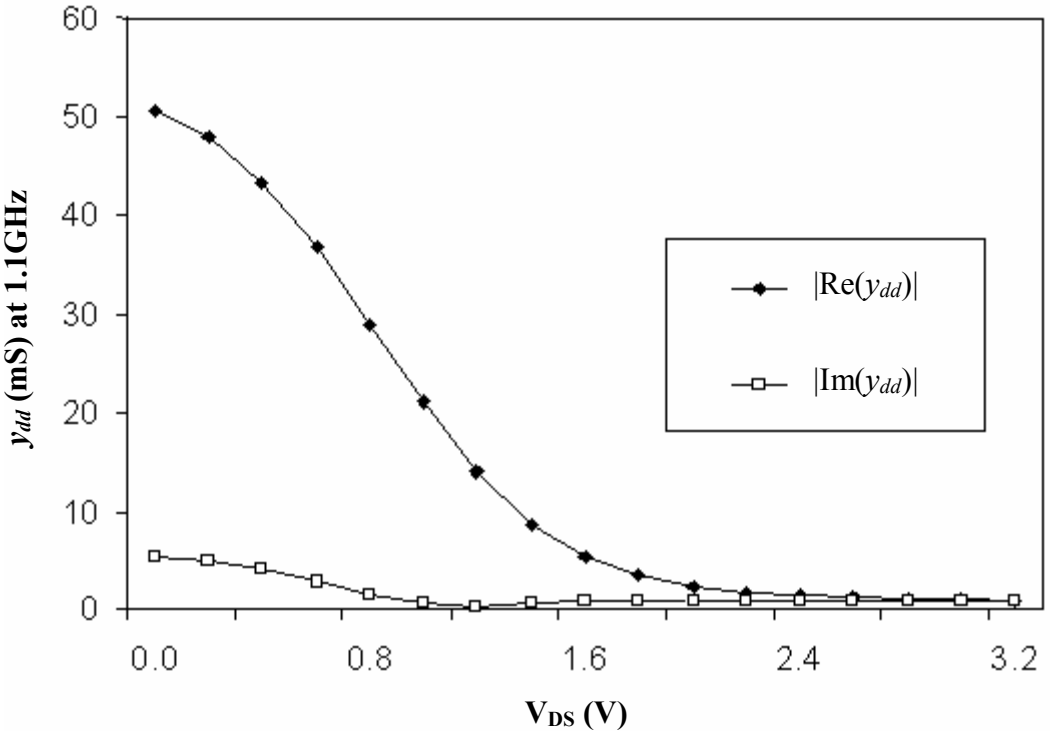


Figure 6. 25 Magnitude of measured Re(y_{dd}) and Im(y_{dd}) (V_{GS}=3V, V_{SB}=0V)

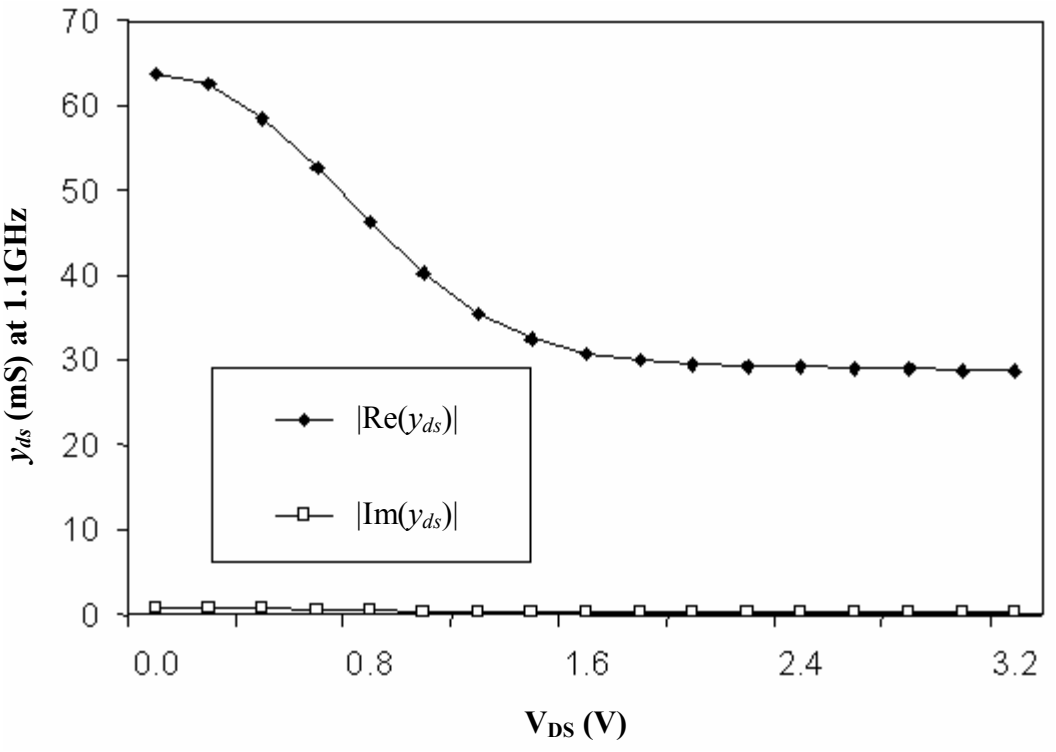


Figure 6. 26 Magnitude of measured Re(y_{ds}) and Im(y_{ds}) (V_{GS}=3V, V_{SB}=0V)

Figure 6.27 shows y_{gg} exhibiting a different scenario, wherein the imaginary part of the measured admittance is much larger than the real part. Here we see that the measured capacitance trend is very much in agreement with analytical and simulated trends. However in this case, the phase is very close to 90° and thus the real part of the measured admittance has a high uncertainty in value. But since this conductance is very small and is not used in charge calculations it may not have any significant bearing on the device modeling. Thus, the observed variations in some of the terminal capacitances obtained from the measured 0.35μm device may arise from measurement uncertainties. However, they do not affect the overall device characterization because they are much smaller in value and all the dominant capacitances and trans-conductance have been obtained in tune with analytical trends.

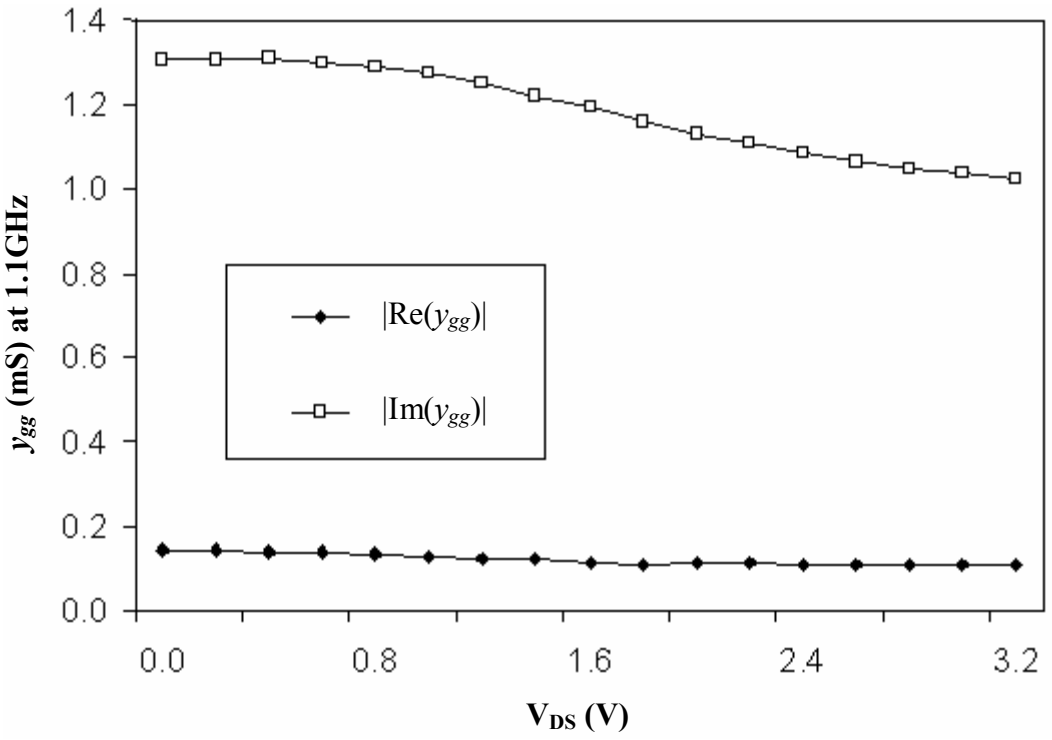


Figure 6. 27 Magnitude of measured Re(y_{gg}) and Im(y_{gg}) (V_{GS}=3V, V_{SB}=0V)

The frequency dependence of the capacitances (Figure 6.13-6.21) is also quite significant. Thus the terminal charges obtained from these capacitances will also exhibit frequency dependent variations, which will be discussed in Section 6.4.1 of this chapter. The next section reports the bias dependence of the device trans-conductance and its decrease with increasing frequency due to the NQS effect.

6.3.2 NQS effect on device trans-conductance

The non-quasi-static (NQS) effect leads to a degradation of the device trans-conductance with increasing frequency. Figure 6.28 shows the measured device trans-conductance from GD and GS at V_{GS}=3V, V_{DS}=3.2V and V_{SB}=0V. The non-quasi-static effect on the device trans-conductance is shown here manifested as the increasing difference in the magnitudes of g_m (trans-conductance in Common Source configuration)

and g_{ms} (trans-conductance in Common Drain configuration) with frequency, for the first time. They are obtained from the three-port data as Re(y_{dg} - y_{gd}) and Re(y_{sg} – y_{gs}) respectively.

According to device symmetry considerations, at low frequency, the magnitudes of both g_m and g_{ms} are expected to be equal (as seen in Figure 6.28), because the gate's effect on the drain and source is equal and opposite. The divergence in the magnitudes of g_m and g_{ms} at higher frequencies is a clear indication that the channel charges are unable to respond immediately to the applied terminal signals on account of their electrical inertia. This would mean that at any instant, the amount of charge that enters the device through the source is not equal to the amount of charge leaving out of the drain, explaining the divergence of the trans-conductance reported here, to be due to non-quasi-static effect (NQS).

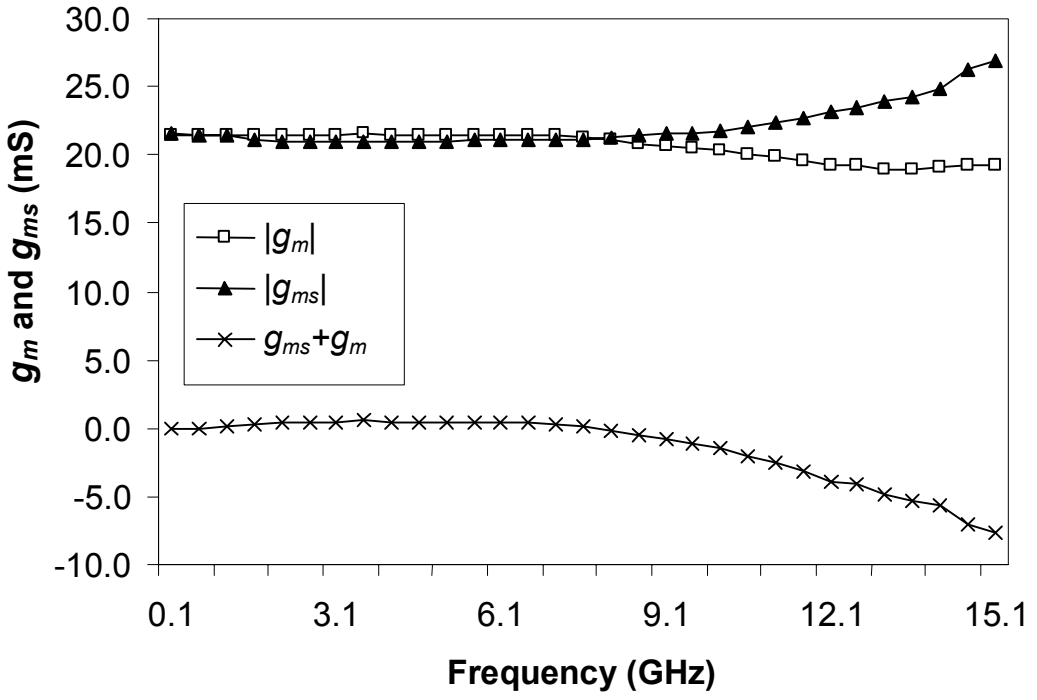


Figure 6. 28 NQS effect on measured trans-conductance (V_{GS}=3V, V_{DS}=3.2V, V_{SB}=0V)

Figure 6.29 shows the device trans-conductance g_m as a function of drain bias at three different frequencies at V_{GS}=3V. The g_m at a given frequency increases rapidly with V_{DS} in the triode region (V_{th}=0.55V) and then saturates. The frequency dependent degradation in g_m is not very obvious at low drain biases as the g_m is very low (the device is in linear region of operation). However in saturation, the g_m at 15.1GHz is about 8% lower than the low frequency g_m. This means that the NQS effect is quite significant and cannot be ignored at such high frequencies. The next section describes the behavior of terminal charges extracted from three-port data.

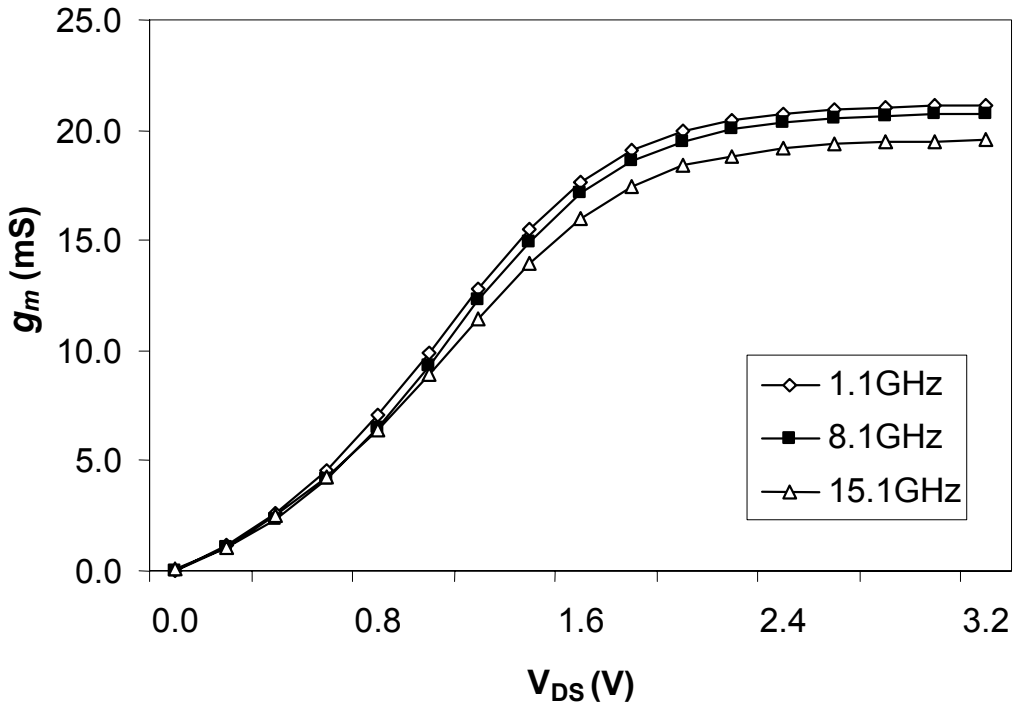


Figure 6. 29 NQS effect on measured g_m at different drain bias (V_{GS}=3V, V_{SB}=0V)

6.4 Terminal charges

All the terminal charges extracted directly from measured three-port data are being reported here for the first time. The charge computation has been discussed in detail in

Section 4.5.2 of Chapter 4. The main equations invoked here are (4.83)-(4.85). All the charges provided here are for the 0.35μm channel length device.

Figure 6.30 shows the gate and bulk terminal charges as functions of V_{GS} for three different V_{DS} values. At V_{DS}=0.2V and V_{GS}=0V, we see that both the gate and bulk charges are nearly zero. But at higher V_{DS}, even for zero V_{GS} we see that, only a small negative charge is induced at the gate and a much larger negative charge develops on the bulk terminal. As V_{GS} is increased, positive charge builds up on the gate while the bulk charge becomes more negative. At a given V_{GS}, we see that the gate charge becomes lower with increasing V_{DS}. This is because a part of the total positive charge is now being induced at the drain terminal to maintain overall charge neutrality. A similar effect of V_{GS} on the drain terminal charge at a given V_{DS} is seen in Figure 6.31.

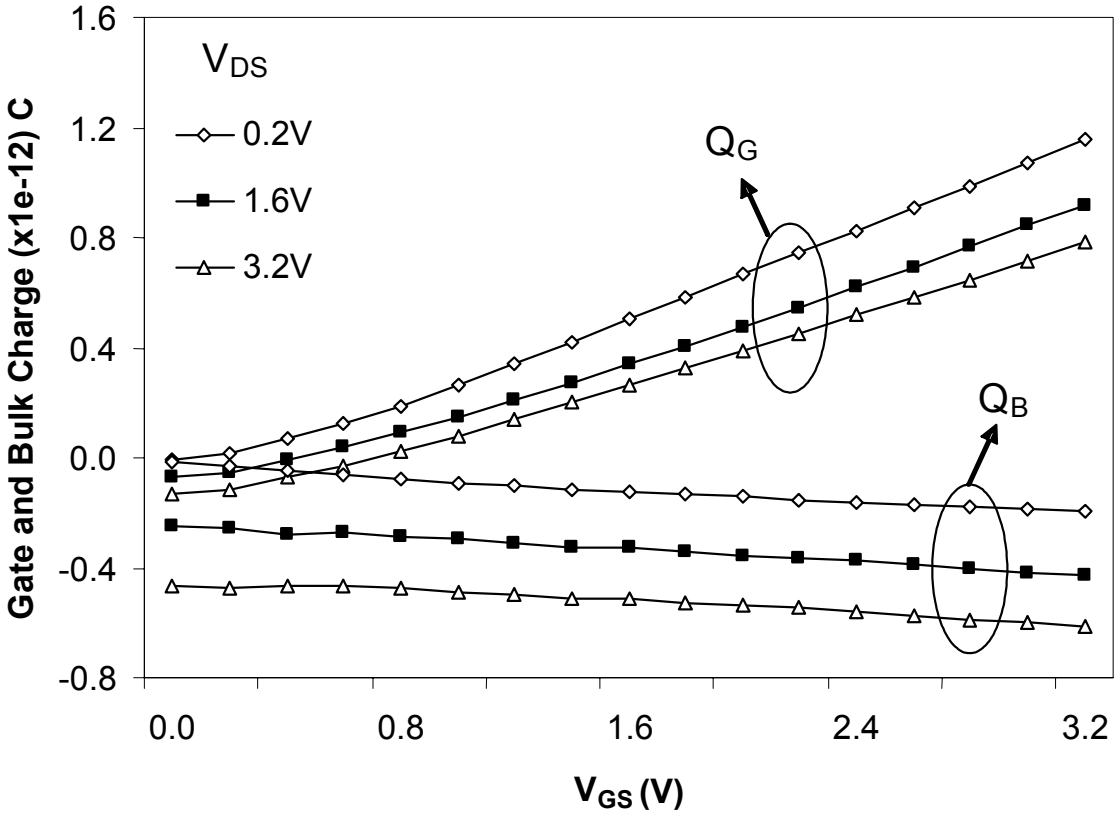


Figure 6. 30 Gate and bulk terminal charges (V_{SB}=0V) at 2.1GHz

Figure 6.31 shows that the drain terminal charges at a given V_{DS} decrease with increasing V_{GS}. And as expected, the drain charge at a given V_{GS} is higher for greater V_{DS}. Figure 6.32 shows that the source charge becomes more negative with increasing gate and drain bias. Thus we can see that both the bulk and source charges serve to balance the positive charges developed on the gate and drain on account of positive V_{GS} and V_{DS}. Figures 6.30 and 6.32 also show that even when V_{SB}=0V, the source and bulk charges have differences in magnitude and behavior. The bulk charge shows a uniform decline with increasing V_{GS} and V_{DS}. But the source charge behavior is more complex and needs further investigation, especially at higher V_{GS}.

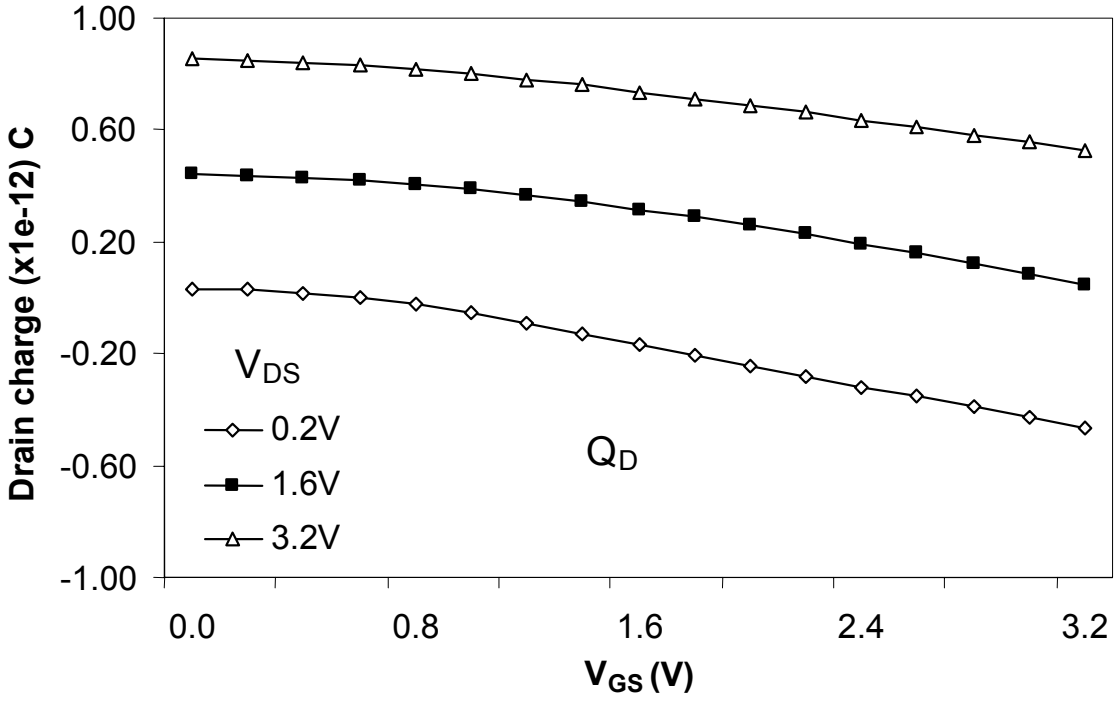


Figure 6. 31 Drain terminal charge (V_{SB}=0V) at 2.1GHz

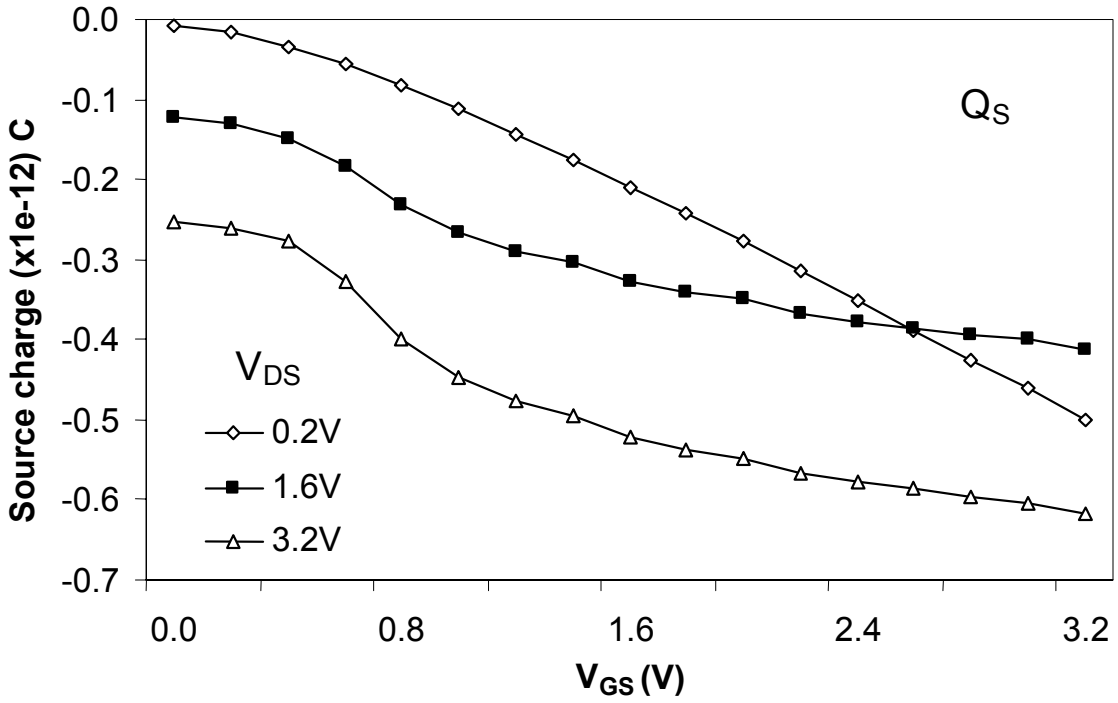


Figure 6. 32 Source terminal charge (V_{SB}=0V) at 2.1GHz

Figure 6.33 depicts the source terminal charge as a function of V_{DS} at different V_{GS}. The source charge at V_{GS}=1.2V falls monotonously with V_{DS}. This is because the transistor is well into saturation even at a low V_{DS} of 0.6V (V_{th}=0.55V). When the V_{GS}=3.2V, the transistor is in the linear region of operation for a greater V_{DS} range. In the linear region of operation we see an interesting behavior in the source charge as it decreases in magnitude with V_{DS}, and then starts increasing once the device gets closer to saturation. This trend is visible even when the V_{GS}=2.2V.

One plausible argument in favor of this behavior is that, in the linear region, the channel is heavily inverted throughout and thus any change in charge due to a positive V_{DS} is effectively shared by both the source and drain terminals. With increasing V_{DS}, just as the drain charge increases, the negative source charge also correspondingly decreases in magnitude. So, the net positive charge induced by the increasing V_{DS} is

being shared by both terminals. But as the device enters into saturation, this kind of direct positive influence of the drain on the source is no longer possible. Thus, beyond the triode region, the source registers a monotonous increase in the charge magnitude. The next section focuses on the frequency dependence of terminal charges.

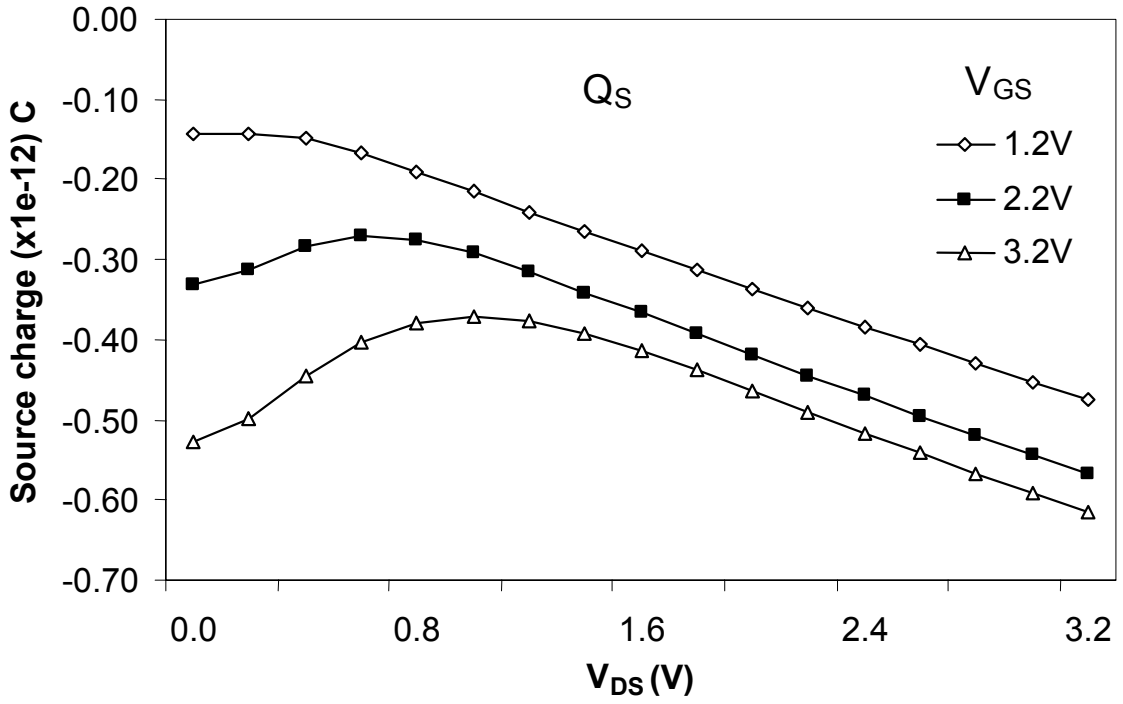


Figure 6. 33 Source terminal charge (V_{SB}=0V) at 2.1GHz

6.4.1 Frequency dependence of terminal charges

Figure 6.34 shows that the gate charge decreases with increasing frequency. The NQS effect and high frequency signal coupling via the gate are possible reasons for this charge deficit. Even at high V_{GS} the gate charge at 14.1GHz falls by as much as 9% from its low frequency values.

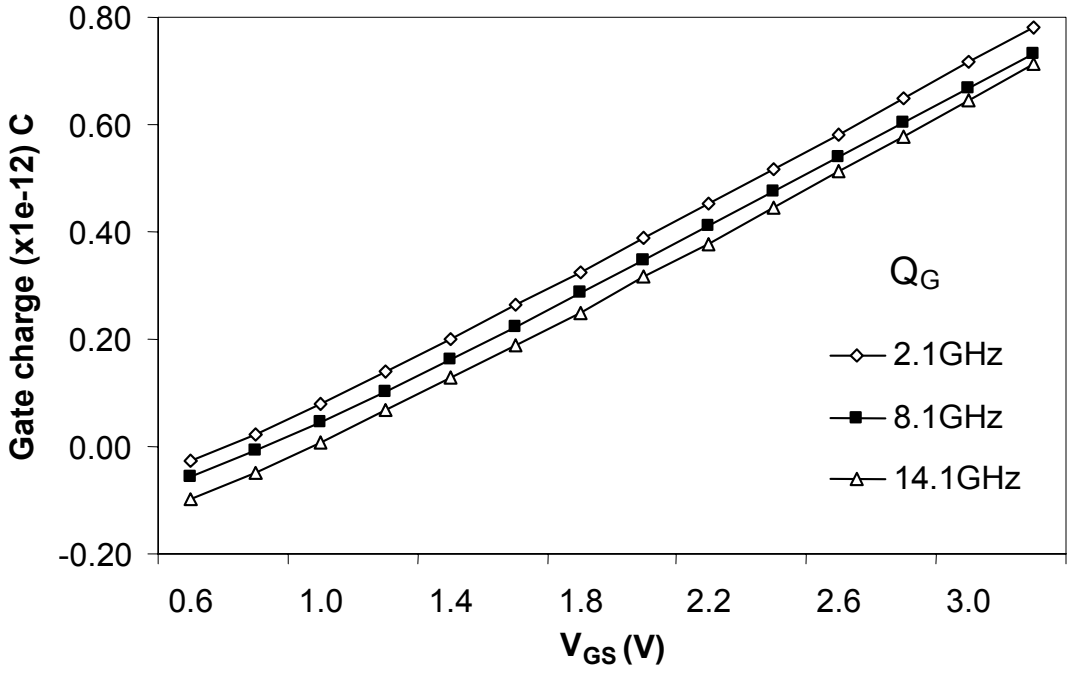


Figure 6. 34 Frequency dependence of Gate charge (V_{DS}=3.2V, V_{SB}=0V)

Figure 6.35 shows the drain charge as a function of V_{DS}, which shows an increase in the charge magnitude at higher frequency for any given bias. Correspondingly, at the same bias conditions, the source terminal charge in Figure 6.36 decreases in magnitude with increasing frequency. This implies a net build-up or storage of transient charge in the channel that conforms to theoretical analysis and simulations of the NQS effect [6, 7].

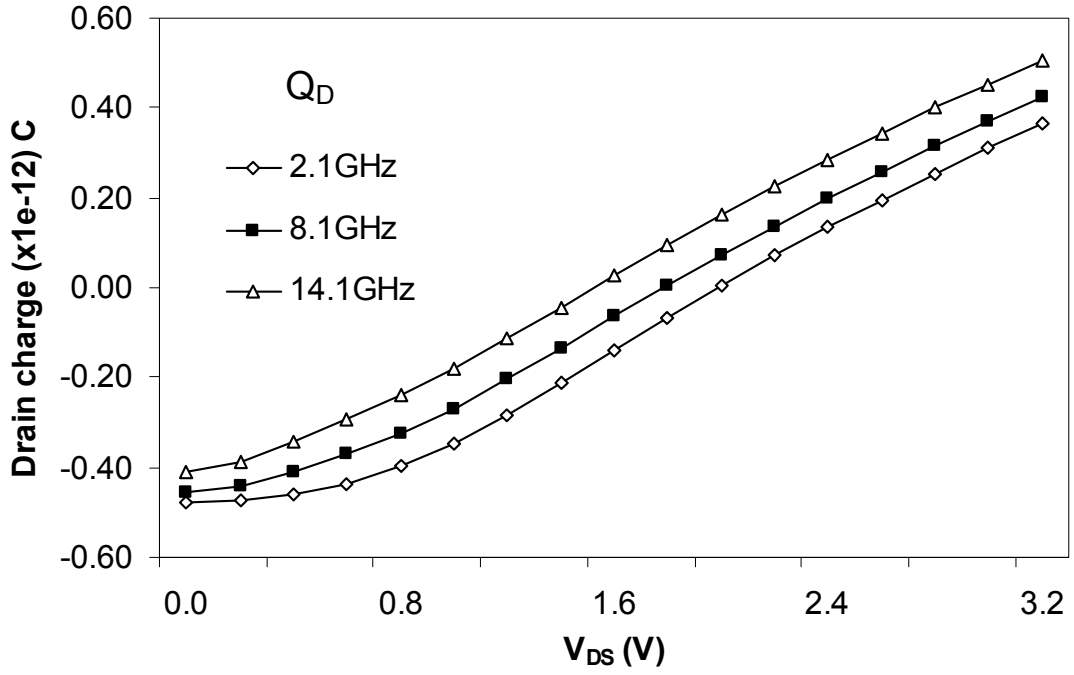


Figure 6. 35 Frequency dependence of drain charge (V_{GS}=3.2V, V_{SB}=0V)

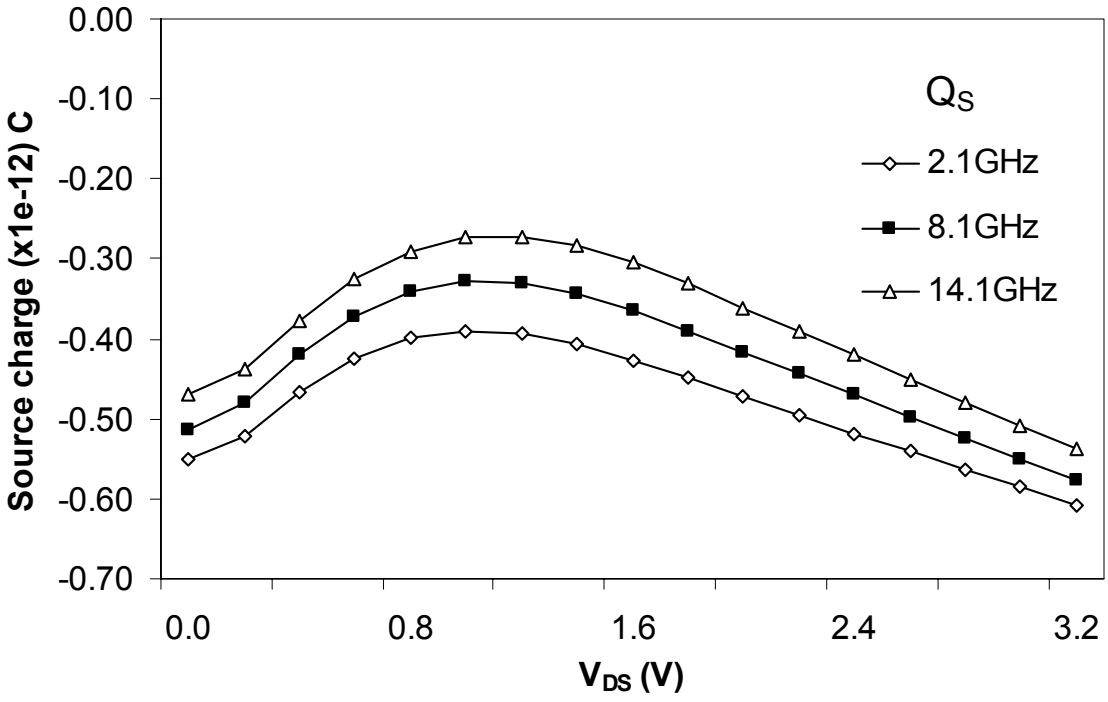


Figure 6. 36 Frequency dependence of source charge (V_{GS}=3.2V, V_{SB}=0V)

The information provided in this work regarding the bias and frequency dependence of the MOS terminal charges is very useful for large signal RF modeling applications and circuit simulations. There have been no prior reports on all the measured terminal charges of the MOSFET. This has been made possible only because of the RF three-port characterization of the MOSFET reported in this work. The next chapter presents the conclusions of this work and also includes a few suggestions for future enhancements.

6.5 Summary

The RF equivalent circuit model parameters obtained from different two-port measurement configurations match well up to 15GHz. This proves the efficacy of the extraction scheme. The redundant main diagonal elements (y_{gg}, y_{dd} and y_{ss}) obtained from different two-port measurement configurations also match very well over the entire frequency range. This mathematically validates the three-port characterization scheme evolved from two-port measurements. The bias and frequency dependence of the terminal capacitances and the device trans-conductance are discussed and the NQS effect is investigated. The results of 2-D device simulations are also provided as a guideline. The bias and frequency dependence of all the terminal charges (obtained from measured terminal capacitances) are presented for the first time and their behavior is discussed with the help of device physics.

Chapter 7: Conclusion and Future Work

7.1 Conclusion

A new method has been demonstrated to obtain three-port RF characterization of a MOS transistor valid up to 15GHz in all regions of operation, from two-port S-parameter measurements of the device carried out in three different configurations (GD, GS and SD). The RF characterization of the GPG probe used for DC bias feed at the un-calibrated third port has been reported. The high frequency loss and inductive behavior of the probe has been identified here for the first time. The large undesirable effect of the GPG probe impedance on two-port RF measurements has been clearly illustrated using MOS admittance network principles as a test of measurement veracity. The need for de-embedding the GPG probe impedance from the two-port measurements to obtain the correct three-port parameters has been clearly established.

An effective method has been advanced to remove the effect of the GPG probe, using an RF equivalent circuit based extraction procedure for the MOS device. A new small-signal equivalent circuit model has been developed to represent the MOSFET at RF. A novel test structure named SD-R has been designed to independently extract the on-state junction admittances in all regions of operation. The utility of the SD-R device towards RF parameter extraction and substrate modeling has been discussed. A new direct parameter extraction scheme has been evolved for the proposed RF small-signal model, to uniquely extract several equivalent circuit model parameters in all three two-port configurations (GD, GS and SD) using the parameters extracted from the SD-R device. An off-state parameter extraction procedure has also been developed to extract the

extrinsic device admittances. The generation of accurate three-port Y-parameters of the device using the extracted equivalent circuit model parameters has been explained. A method has been described to extract the terminal charges of the device from three-port terminal capacitances using numerical techniques.

Process and device simulations have been carried out for an NMOS device and the SD-R structure using the 2-dimensional TCAD simulators TSUPREM-4 and Medici to verify the device characterization and extraction procedure. The extracted junction admittances from both simulations and measurements of the SD-R test structure have been shown to exhibit similar trends and physical explanation has been provided for the bias and frequency dependence of the junction capacitance and conductance.

The parameter extraction procedure has been proved to be consistent by verifying the match of the same equivalent circuit model parameters extracted from different two-port configurations. The three-port characterization scheme has been validated using the redundancy of some of the admittance elements obtained from different two-port configurations. The measured three-port terminal capacitances have been shown as functions of both bias and frequency along with the simulated results as a guideline. The NQS effect has been shown to manifest as the increasing difference between the magnitudes of trans-conductance obtained from the common-source configuration (g_m=g_{dg}-g_{gd}) and of that obtained from the common-drain configuration (g_{ms}=g_{sg}-g_{gs}). All the terminal charges of the MOSFET, extracted using its measured three-port terminal capacitances, have been shown here as functions of both bias and frequency for the first time. The usefulness of such a description of terminal charges towards RF device modeling and circuit simulation has also been discussed.

7.2 Future work

This work has described the three-port characterization of MOS transistors valid up to a frequency of 15GHz. The RF equivalent circuit model used in de-embedding the GPG probe impedance determines the validity of the three-port characterization. For the convenience of parameter extraction, the substrate network has been characterized by two admittances (y_{bs} and y_{bd}). Further, the terminal inductances (L_s, L_d and L_g) have not been included in the equivalent circuit model. At very high frequencies, such a model becomes less accurate. Accordingly, we found that the match between the probe de-embedded main diagonal admittances (y_{gg}, y_{dd} or y_{ss}) obtained from two different configurations slowly degraded beyond 15GHz. Thus, the de-embedding of the GPG probe carried out using the model is not complete beyond 15GHz. As a result the three-port characterization described here is valid up to 15GHz. The frequency validity range could be improved by using a better and more accurate model, which includes a more complex substrate network (say, a three or five resistor network) as well as the terminal inductances in the equivalent circuit. The direct extraction of a three-resistor substrate network using the SD-R device has been reported in our work mentioned in section 1.7 of Chapter 1. The extracted substrate network can be included in the enhanced RF equivalent circuit of the MOSFET. This would further need small signal analysis to develop an algorithm to de-embed GPG probe parasitic.

The match of extracted equivalent circuit model parameters and redundant admittance elements obtained from different two-port configurations should be further improved by carrying out all the two-port measurements from the same device. This requires more improved quality bonding pads to ensure contact consistency over long measurement

durations and repeated probing. Thus device level variations in the equivalent circuit model parameters must be eliminated. The GPG probe must be characterized after completion of measurements in each two-port configuration, to monitor its loss and inductive characteristics.

The charge integration should be performed on the measured data for all different body biases to gain greater understanding of terminal charge behavior at non-zero V_{SB}. Three of the terminal three-port capacitances obtained from 0.35μm device measurements differ from those obtained from the 2-D device simulations as a result of measurement uncertainties caused by dominant conductance. Alternative approaches to isolate these capacitances must be investigated.

If the process parameters of the fabricated device are obtained, the device simulations could be optimized to reflect the actual measurements. The RF simulations may also be performed using compact models like BSIM4 and the terminal charges obtained from them can be studied against the charges extracted from measurements. Ultimately, new compact models can be developed to accommodate the behaviors observed.

References

[1] T. H. Lee, "CMOS RF: No Longer an Oxymoron," *IEEE Gallium Arsenide Integrated Circuit Symposium,* Anaheim, California, pp. 244-247, Oct. 1997.

[2] P. H. Woerlee, M. J. Knitel, Ronald van Langevelde, Dirk B. M. Klassen, Luuk F. Tiemeijer, A. J. Scholten and Adrie T. A. Zegeres-van Duijnhoven, "RF-CMOS Performance Trends," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1776-1782, Aug. 2001.

[3] A. Ajjikuttira, C. Leung, E-S. Khoo, M. Choke, R. Singh, T-H. Teo, B-C. Cheong, J-H. See, H-S. Yap, P-B. Leong, C-T. Law, M. Itoh, A. Yoshida, Y. Yoshida, A. Tamura and H. Nakamura, "A Fully-Integrated CMOS RFIC for Bluetooth Applications," *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, pp. 198-200, Feb. 2001.

[4] R. C. Liu, H. Y. Chang, C. H. Wang, and H. Wang, "A 63-GHz VCO using a standard 0.25-μm CMOS process," *IEEE International Solid-State Circuits Conference Digest*, San Francisco, CA, 2004, pp. 446–447.

[5] M-D. Tsai and H. Wang, "A 0.3–25-GHz Ultra-Wideband Mixer Using Commercial 0.18-μm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 11, Nov. 2004.

[6] F. Allen, Ping K. Ko, and Mansun Chan, "Determining the Onset Frequency of Non-quasistatic effects of the MOSFET in AC simulation," *IEEE Electron Device Letters*, vol. 23, no. 1, pp. 37-40, Jan. 2002.

[7] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., New York: McGraw-Hill, 1999.

[8] BSIM 4.2.1 MOSFET Model and User's Manual, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, *http://www-device.eecs.berkeley.edu/bsim3/~bsim4.html*.

[9] Mansun Chan, K. Hui, R. Neff, C. Hu and P. Ko, "A Relaxation time Approach to Model the Non-Quasi-Static Transient Effects in MOSFETs," *IEEE IEDM Technical Digest*, pp. 169-172, 1994.

[10] X. Jin, Jia-Jiunn Ou, Chih-Hung Chen, W. Liu, M. Jamal Deen, P. R. Gray and Chenming Hu, "An effective Gate Resistance Model for CMOS RF and Noise Modeling," *IEEE IEDM Technical Digest*, 1998, pp. 961-964.

[11] Y. Cheng, M. Matloubian, "High Frequency Characterization of Gate Resistance in RF MOSFETs," *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 98-100, Feb. 2001.

[12] Y. Cheng, Chih-Hung Chen, M. Matloubian, M. Jamal deen, "High-Frequency Small Signal AC and Noise Modeling of MOSFETs for RF IC Design," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 400-408, Mar. 2002.

[13] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal and J. P. Mattia, "RF MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," *IEEE IEDM Technical Digest*, 1997, pp. 309–312.

[14] Suet Fong Tin and K. Mayaram, "Substrate Network Modeling for CMOS RF Circuit Simulation," *IEEE Custom Integrated Circuits conference*, 1999, pp. 583-586.

[15] Y. Cheng and M. Matloubian, "On the High-Frequency Characteristics of Substrate Resistance in RF MOSFETs," *IEEE Electron Device Letters*, vol. 21, no. 12, pp. 604-606, Dec. 2000.

[16] Y. Cheng and M. Matloubian, "Parameter Extraction of Accurate and Scaleable Substrate Resistance Components in RF MOSFET," *IEEE Electron Device Letters*, vol. 23, no. 4, pp. 221-223, April 2002.

[17] S. Jen, C. C. Enz, D. R. Pehlke, M. Schroter and Bing J. Sheu, "Accurate Modeling and Parameter Extraction for MOS Transistors Valid Upto 10 GHz," *IEEE Transactions on Electron Devices*, vol. 46, no. 11, pp. 2217-2226, Nov. 1999.

[18] C. C. Enz and Yuhua Cheng, "MOS Transistor Modeling for RF IC Design," *IEEE Transactions on Solid-State Circuits*, vol. 35, no. 2, pp. 186-201, Feb. 2000.

[19] C. C. Enz, "An MOS Transistor Model for RF IC Design Valid in All Regions of Operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 342-359, Jan. 2002.

[20] I. Kwon, Minkyu Je, K. Lee and Hyungcheol Shin, "A Simple and Analytical Parameter-Extraction Method of a Microwave MOSFET," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 6, pp. 1818-1819, June 2002.

[21] S. Lee and H. K. Yu, "Determining non-quasi-static small-signal equivalent circuit of a RF silicon MOSFET," *Solid State Electronics*, vol. 45, pp. 356-364, 2001.

[22] E. P. Vandamme, D. Schreurs, C. van Dinther, G. Badenes and L. Deferm, "Development of a RF large Signal MOSFET model, based on an equivalent circuit, and comparison with the BSIM3v3 compact model," *Solid State Electronics*, vol. 46, pp. 353-360, 2002.

[23] Alain-Serge Porret, Jean-Michel Sallese, and Christian C. Enz, "A Compact Non-Quasi-Static Extension of a Charge-Based MOS Model," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, August 2001, pp. 1647-1654.

[24] D. R. Pehlke, M. Schroter, A. Burstein, M. Matloubian and M. F. Chang, "High frequency application of MOS compact models and their development for scalable RF model libraries," *Proc. IEEE Custom Integrated Circuit Conference*, May 1998, pp. 219–222.

[25] J-J. Ou, X. Jin, I. Ma, C. Hu and P. R. Gray, "CMOS RF modeling for GHz communication ICs," *1998 Symp. VLSI Technology Technical Digest*, June 1998.

[26] "Cascade Microtech / Agilent Technologies Device Characterization and Modeling Seminar", Tariq Alam, On Wafer Multiport Characterization, April 2005.

[27] Anritsu Application Note: "Three and Four Port S-Parameter Measurements", 2002, *http://www.eettaiwan.com/ARTICLES/2002MAY/PDF/2002MAY02_RFD_EMS_NTES_AN245.PDF*.

[28] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common mode scattering parameters: Theory and simulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-43, July 1995, pp. 1530-1539.

[29] Urs Lott, Werner Baumberger and Urs Gisiger, "Three-Port RF Characterization of Foundry Dual-Gate FETs Using Two-Port Test Structures With On-Chip Loading Resistors," *Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures*, vol. 8, pp. 167-170, March 1995.

[30] Martin Schoon, "A Semi-Automatic three-port Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 6/7, pp. 974-978, June/July 1993.

[31] Steven Goldberg, Michael B. Steer and Paul D. Franzon, "Accurate Experimental Characterization of Three-Ports," *IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, 1991, pp. 241-244.

[32] A. Jha, J. M. Vasi, S. C. Rustagi and M. B. Patil, "A novel method to obtain three-port network parameters using two-port measurements," *IEEE International Conference on Microelectronics Test Structures*, pp. 57-62, March 2004.

[33] G. Gonzalez, *Microwave Transistor Amplifiers*, 2nd-Edition, Prentice-Hall, 1997.

[34] "Agilent 85190A IC-CAP 2004 User's Guide," Agilent Technologies, *http://eesof.tm.agilent.com/docs/iccap2004/icug/index.html*.

[35] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM Calibrations with Automatic Determination of Load Inductance," *36th ARFTG Conference Digest*, November 1990.

[36] Cascade Microtech Software Datasheet: "WinCal Calibration Software", WINCAL-DS-1204, http://www.cascademicrotech.com/pubs/WINCAL-DS.pdf.

[37] M. C. A. M. Koolen, J. A. M. Geelen and M. P. J. G. Verleijen, "An Improved De-embedding Technique for On-Wafer High Frequency Characterization," *IEEE Bipolar Circuits and Technology Meeting*, pp. 188-191, 1991.

[38] F. Sischka and T. Gneiting, "RF MOS Measurements," *International Journal of High Speed Electronics and Systems*, vol. 11, no. 4 (2001), pp. 887-951, World Scientific Publishing Company.

[39] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian and R. W. Dutton, "Analysis of Velocity Saturation and Other Effects on Short-Channel MOS Transistor Capacitances," *IEEE Transactions on Computer-Aided Design*, vol. CAD-6, no.2, March 1987.

[40] Tajinder Manku, "Microwave CMOS Device Physics and Design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, March 1999, pp. 277-285.

[41] Tsuprem-4 User's Manual, Release v2002.3, Synopsys, Inc., Unpublished.

[42] Medici User's Manual, Release v2002.2, Synopsys, Inc., Unpublished.

[43] H. K. Gummel, Kumud Singhal, "Intrinsic MOSFET Capacitance Coefficients," *IEEE Transactions on Electron Devices*, vol. 48, no. 10, pp. 2384-2393, Oct. 2001.

[44] S. H. Jen, B. J. Sheu, A. Y. Park, "An efficient MOS transistor charge/capacitance model with continuous expressions for VLSI," *Proc. IEEE 1998 International Symposium on Circuits and Systems*, vol. 6, pp. 413–416, May 1998.

Appendix A: TSUPREM-4 input files for 0.35μm process

A.1 Generation of initial process mesh

```
$ This is a comment -- Process for a 0.35 MOS application

$ Assign the Channel Length

ASSIGN        NAME=LD  N.VAL=0.35

$ Specify the mesh, overflowing commands start with a '+' in first column of next line

METHOD  ERR.FAC=1

MESH  GRID.FAC=2

MESH LY.SURF=0.05       DY.SURF=0.004       LY.ACTIV=0.6       DY.ACTIV=0.02

+LY.BOT=500 DY.BOT=20

LINE   X       LOCATION=0.0                                    SPACING=0.1

LINE   X       LOCATION=0.25                                   SPACING=0.04

LINE   X       LOCATION=0.7                                    SPACING=0.02

LINE   X       LOCATION=((((1.08*2)+ @LD)/2) - @LD/2)       SPACING=0.004

LINE   X       LOCATION=(((1.08*2)+ @LD)/2)                    SPACING=0.006

LINE   X       LOCATION=((((1.08*2)+ @LD)/2) + @LD/2)       SPACING=0.004

LINE   X       LOCATION=((1.08*2)+ @LD - 0.7)                  SPACING=0.02

LINE   X       LOCATION=((1.08*2)+ @LD - 0.25)                 SPACING=0.04

LINE   X       LOCATION=((1.08*2)+ @LD)                        SPACING=0.1

$ Eliminate unwanted nodes

ELIMINATE  ROWS  Y.MIN=0.0 Y.MAX=0.65 X.MIN=0.0 X.MAX=0.55

ELIMINATE  ROWS  Y.MIN=0.0 Y.MAX=0.65 X.MIN=((1.08*2)+ @LD - 0.55)
```

```
+ X.MAX=((1.08*2)+ @LD)
ELIMINATE  COLUMNS  Y.MIN=0.55 X.MIN=0.6 X.MAX=((1.08*2)+ @LD -0.6)
ELIMINATE  COLUMNS  Y.MIN=0.55 X.MIN=0.9 X.MAX=((1.08*2)+ @LD -0.9)
ELIMINATE  COLUMNS  Y.MIN=0.55 X.MIN=1.05 X.MAX=((1.08*2)+ @LD -1.05)
ELIMINATE  COLUMNS  Y.MIN=0.3 Y.MAX=0.52 X.MIN=0.65
+ X.MAX=((1.08*2)+ @LD -0.65)
ELIMINATE  COLUMNS  Y.MIN=0.15 Y.MAX=0.28 X.MIN=1.05
+ X.MAX=((1.08*2)+ @LD -1.05)
$ Initialize the substrate
INITIALIZE <100> IMPURITY=BORON   I.CONC=5E15   WIDTH=((1.08*2)+ @LD)
$ Plot the initial mesh
SELECT     TITLE="Initial Mesh for LD=@LD"
PLOT.2D    SCALE GRID Y.MAX=1.5 C.GRID=2
SELECT     Z=LOG10(BORON)  TITLE="Initial B doping(LD=@LD)"
PLOT.1D    X.VALUE=((((1.08*2)+ @LD)/2)- @LD/2) RIGHT=1.0 BOTTOM=12
+ TOP=17 LINE.TYP=1 COLOR=2
$ LOCOS process: 300A Sacrificial Oxide growth
METHOD      VISCOELA  DY.OXIDE=0.004  UNREFINE=0
DIFFUSION   TEMP=600 TIME=9.5   T.FINAL=625   N2
DIFFUSION   TEMP=625 TIME=10    T.FINAL=650   N2
DIFFUSION   TEMP=650 TIME=3.0   T.FINAL=675   N2
DIFFUSION   TEMP=675 TIME=4.0   T.FINAL=675   N2
DIFFUSION   TEMP=675 TIME=45    T.FINAL=900   N2
```

```
DIFFUSION   TEMP=900 TIME=20              N2

DIFFUSION   TEMP=900 TIME=177   F.O2=6  PRESSURE=0.6

DIFFUSION   TEMP=900 TIME=140   T.FINAL=600   N2

$ LOCOS process:Deposit 2000A nitride

DEPOSIT  NITRIDE  THICK=0.2  SPACES=20

DEPOSIT  PHOTORESIST  POSITIVE  THICKNESS=1

$ Print the thickness of layers

SELECT  Z=1

PRINT.1D     LAYERS  X.VALUE=0.2

SELECT  Z=1

PRINT.1D     LAYERS  X.VALUE=(((1.08*2)+ @LD)/2)

$ Etch resist and nitride on left and right side to define active area mask

ETCH PHOTORESIST  LEFT  P1.X=0.23

ETCH PHOTORESIST  RIGHT P1.X=((1.08 + @LD) + 0.85)

ETCH NITRIDE   LEFT  P1.X=0.23

ETCH NITRIDE   RIGHT P1.X=((1.08 + @LD) + 0.85)

SELECT  Z=1

PRINT.1D     LAYERS  X.VALUE=0.2

SELECT  Z=1

PRINT.1D     LAYERS  X.VALUE=(((1.08*2)+ @LD)/2)

$ Boron field implant

IMPLANT    BORON  DOSE=2E13  ENERGY=55  TILT=7  ROTATION=30

ETCH PHOTORESIST ALL
```

```
SELECT     Z=LOG10(BORON)  TITLE="B doping before LOCOS"
PLOT.1D    X.VALUE=0.001 LEFT=-0.05 RIGHT=1.0 BOTTOM=13
+ TOP=20 LINE.TYP=1 COLOR=2
$ LOCOS process: Grow the field oxide
METHOD      VISCOELA  DY.OXIDE=0.005  UNREFINE=0
MATERIAL     MAT=Nitride  VC=170
MATERIAL     MAT=OXIDE    VC=425
DIFFUSION   TEMP=700 TIME=100      T.FINAL=1050 N2
DIFFUSION   TEMP=1050 TIME=43      N2
DIFFUSION   TEMP=1050 TIME=6.5     F.O2=11
DIFFUSION   TEMP=1050 TIME=45      F.O2=11   F.H2=16
DIFFUSION   TEMP=1050 TIME=6.0     F.O2=11
DIFFUSION   TEMP=1050 TIME=110     T.FINAL=700     N2
SELECT     Z=LOG10(BORON)
PLOT.1D    ^AX ^CL X.VALUE=(((1.08*2)+ @LD)/2) LEFT=-0.05 RIGHT=0.8
+ BOTTOM=13 TOP=16 LINE.TYP=2 COLOR=2
$ Print the thickness of layers after field oxidation
SELECT       Z=1
PRINT.1D     LAYERS  X.VALUE=0.001
PRINT.1D     LAYERS  X.VALUE=(((1.08*2)+ @LD)/2)
$ Plot the structure after field oxidation
SELECT     TITLE="Structure after FOX LD=@LD"
```

```
PLOT.2D    SCALE    Y.MAX=0.5

COLOR      SILICON  COLOR=7

COLOR      OXIDE    COLOR=5

COLOR      NITRIDE  COLOR=3

PLOT.2D    ^AXES  ^CLEAR  SCALE    Y.MAX=0.5

$ LOCOS process: Removal of masking nitride and pad oxide

ETCH     NITRIDE     ALL

ETCH       OXIDE       THICK=0.015

$ Print layer thicknesses

SELECT     Z=1

PRINT.1D   X.VALUE=(((1.08*2)+ @LD)/2)  LAYERS

PRINT.1D   X.VALUE=0.001  LAYERS

$ Save to output file

SAVEFILE   OUT.FILE=b4wellimpl

STOP
```

A.2 Generation of final structure

```
$ To produce a 0.35 MOS application

$ Assign Channel Length

ASSIGN         NAME=LD  N.VAL=0.35

$ Change P-well Implant (Boron)

ASSIGN         NAME=PWELLDOP      N.VAL=1.3E13

ASSIGN         NAME=PENERG        N.VAL=300

$ Change Profile Implant (Boron)
```

```
ASSIGN        NAME=PFILEDOP     N.VAL=5E12

ASSIGN        NAME=PFILENERG       N.VAL=130

$ Change Anti punch through implant (Boron)

ASSIGN     NAME=PAPT      N.VAL=1E13

ASSIGN     NAME=APTENER   N.VAL=60

$ Change Threshold adjust implant (BF2)

ASSIGN     NAME=VT        N.VAL=5E12

ASSIGN     NAME=VTENERG   N.VAL=40

$ Change P-well Anneal - 8 sec

ASSIGN     NAME=PTEMP     N.VAL=1000

ASSIGN     NAME=PTIME     N.VAL=0.133

$ Change SDE/LDD Implant (Arsenic or Phosphorus)

ASSIGN     NAME=LDD       N.VAL=2E13

ASSIGN     NAME=LDDENER   N.VAL=30

ASSIGN     NAME=LDDTILT   N.VAL=7

$ Change SDE/LDD Anneal - 2 sec

ASSIGN     NAME=LDDTEMP   N.VAL=950

ASSIGN     NAME=LDDTIME   N.VAL=0.033

$ Change Source/Drain Implant (Arsenic)

ASSIGN     NAME=SD        N.VAL=1E15

ASSIGN     NAME=SDENER    N.VAL=70

ASSIGN     NAME=SDTILT    N.VAL=7

$ Change Source/Drain Anneal - 10 sec
```

```
ASSIGN     NAME=SDTEMP    N.VAL=1000

ASSIGN     NAME=SDTIME    N.VAL=0.166

$ Load the mesh file generated using A.1

LOADFILE  IN.FILE=b4wellimpl

$ Mesh plotting before p-well, Threshold & Anti Punch through anneal

SELECT     TITLE="mesh before p-well dope"

PLOT.2D    SCALE GRID Y.MAX=1.0 C.GRID=2

SELECT     Z=LOG10(BORON)  TITLE="B doping before well implant(LD=@LD)"

PLOT.1D    X.VALUE=((((1.08*2)+ @LD)/2)- @LD/2) LEFT=-0.05 RIGHT=1.2

+ BOTTOM=12 TOP=17 LINE.TYP=1 COLOR=2

ETCH OXIDE THICK=0.0062

SELECT     Z=1

PRINT.1D   X.VALUE=(((1.08*2)+ @LD)/2)  LAYERS

$ P-well implant

METHOD PD.FULL UNREFINE=0

IMPLANT        BORON    DOSE=@PWELLDOP    ENERGY=@PENERG   TILT=7

+ROTATION=45

$ Profile implant

METHOD PD.FULL UNREFINE=0

IMPLANT        BORON    DOSE=@PFILEDOP    ENERGY=@PFILENERG  TILT=7

+ROTATION=45

$ Anti-punch through implant

METHOD PD.FULL  UNREFINE=0
```

```
IMPLANT BORON DOSE=@PAPT ENERGY=@APTENER TILT=7
+ROTATION=45
$ Vth adjust implant
METHOD PD.FULL
IMPLANT BF2 DOSE=@VT ENERGY=@VTENERG TILT=7 ROTATION=45
SELECT Z=LOG10(BORON)
PRINT.1D OUT.FILE=boron.txt
$ PLOT the concentration of boron after punch through implant
SELECT Z=LOG10(BORON) TITLE="B after implant and anneal (LD=@LD)"
PLOT.1D X.VALUE=(((1.08*2)+ @LD)/2) LEFT=0.0 RIGHT=1.5 BOTTOM=14
+ TOP=21 LINE.TYP=1 COLOR=2
LABEL X=0.3 Y=18.5 LABEL="B after Vth & Pt impls" LINE.TYP=1 C.LINE=2
$ Implant activations
METHOD PD.FULL UNREFINE=0
DIFFUSE TEMP=@PTEMP TIME=@PTIME
ETCH OXIDE THICK=0.01
$Print layers thickness
SELECT Z=1
PRINT.1D X.VALUE=(((1.08*2)+ @LD)/2) LAYERS
$ PLOT the concentration of boron after activation
SELECT Z=LOG10(BORON)
PLOT.1D ^AX ^CL X.VALUE=(((1.08*2)+ @LD)/2) LEFT=0.0 RIGHT=1.2
+ BOTTOM=14 TOP=21 LINE.TYP=2 COLOR=4
```

```
LABEL      X=0.3  Y=18.0  LABEL="B after impl act"  LINE.TYP=2  C.LINE=4

SELECT     Z=LOG10(Act(BORON))

PLOT.1D    ^AX ^CL X.VALUE=(((1.08*2)+ @LD)/2) LEFT=0.0 RIGHT=1.2

+ BOTTOM=14 TOP=21 LINE.TYP=3 COLOR=5

LABEL      X=0.3  Y=17.5  LABEL="active B after impl act"  LINE.TYP=3  C.LINE=5

SELECT     Z=LOG10(BORON)

TITLE="B doping under LOCOS"

PLOT.1D    X.VALUE=0.001 LEFT=-0.05 RIGHT=0.8 BOTTOM=13 TOP=20

+ LINE.TYP=2 COLOR=2

$ Gate oxidation with dielectric film to 0.005um

METHOD      PD.FULL

METHOD      VISCOELA  DY.OXIDE=0.005  UNREFINE=0

DIFFUSION   TEMP=600  TIME=19  T.FINAL=675   N2

DIFFUSION   TEMP=675  TIME=4      N2

DIFFUSION   TEMP=675  TIME=20  T.FINAL=800    N2

DIFFUSION   TEMP=800  TIME=42  INERT

DIFFUSION   TEMP=800  TIME=123  F.O2=4  PRESSURE=0.6

DIFFUSION   TEMP=800  TIME=10  N2

DIFFUSION   TEMP=800  TIME=60  T.FINAL=625     N2

$ Poly deposition - 2000A

DEPOSIT   MATERIAL=POLYSILI THICKNES=0.20 DIVISIONS=20 IMPURITY=P

+ I.CONC=5E20 TEMPERATE=650

DEPOSIT   OXIDE THICKNES=0.05 DIVISIONS=5 IMPURITY=P CONCENTR
```

```
+ I.CONC=5E20
$ Define gate by etching poly
ETCH      OXIDE   LEFT   P1.X=((((1.08*2)+ @LD)/2) - (@LD/2))
ETCH      OXIDE   RIGHT  P1.X=((((1.08*2)+ @LD)/2) + (@LD/2))
ETCH      POLY   LEFT   P1.X=((((1.08*2)+ @LD)/2) - (@LD/2))
ETCH      POLY   RIGHT  P1.X=((((1.08*2)+ @LD)/2) + (@LD/2))
ETCH      OXIDE  THICK=0.005
$ Deposit thin sacrificial oxide equivalent to poly re-oxidation
DEPOSIT MATERIAL=OXIDE THICK=0.010
$ Print layer thicknesses at LMID and through S/D region
SELECT     Z=1
PRINT.1D   X.VALUE=(((1.08*2)+ @LD)/2)  LAYERS
PRINT.1D   X.VALUE=0.65  LAYERS
$ Source/drain LDD implant through 100A oxide
METHOD PD.FULL  UNREFINE=0
IMPLANT ARSENIC ENERGY=@LDDENER DOSE=(@LDD)/2  TILT=@LDDTILT
+ ROTATION=68  IMPL.TAB=TR.ARSENIC
IMPLANT ARSENIC ENERGY=@LDDENER DOSE=(@LDD)/2  TILT=@LDDTILT
+ ROTATION=112 IMPL.TAB=TR.ARSENIC
METHOD  PD.FULL
DIFFUSE    TEMP=@LDDTEMP TIME=@LDDTIME
$ 60nm Spacer formation
DEPOSIT    MATERIAL=NITRIDE  THICK=0.06
```

```
ETCH       NITRIDE  TRAP      THICK=0.09
$ Print the layer thicknesses after spacer formation
SELECT     Z=1
PRINT.1D   Y.VALUE=-0.05  LAYERS
$ Print layer thicknessesthrough  S/D
SELECT     Z=1
PRINT.1D   X.VALUE=0.65  LAYERS
$ Source/drain implant and activation/anneal
METHOD PD.FULL  UNREFINE=0
IMPLANT ARSENIC ENERGY=@SDENER DOSE=(@SD)/2  TILT=@SDTILT
+ ROTATION=68  IMPL.TAB=TR.ARSENIC
IMPLANT ARSENIC ENERGY=@SDENER DOSE=(@SD)/2  TILT=@SDTILT
+ ROTATION=112 IMPL.TAB=TR.ARSENIC
METHOD  PD.FULL
DIFFUSE    TEMP=@SDTEMP TIME=@SDTIME
$ Etch oxide for S/D silicidation
ETCH    OXIDE START      X=0.38          Y=0.05
ETCH    CONTINUE X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4))      Y=0.05
ETCH    CONTINUE X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4))      Y=0
ETCH    DONE                X=0.38          Y=0
ETCH    OXIDE START      X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4))     Y=0.05
ETCH    CONTINUE X=(((1.08*2)+ @LD)-0.38)      Y=0.05
ETCH    CONTINUE X=(((1.08*2)+ @LD)-0.38)      Y=0
```

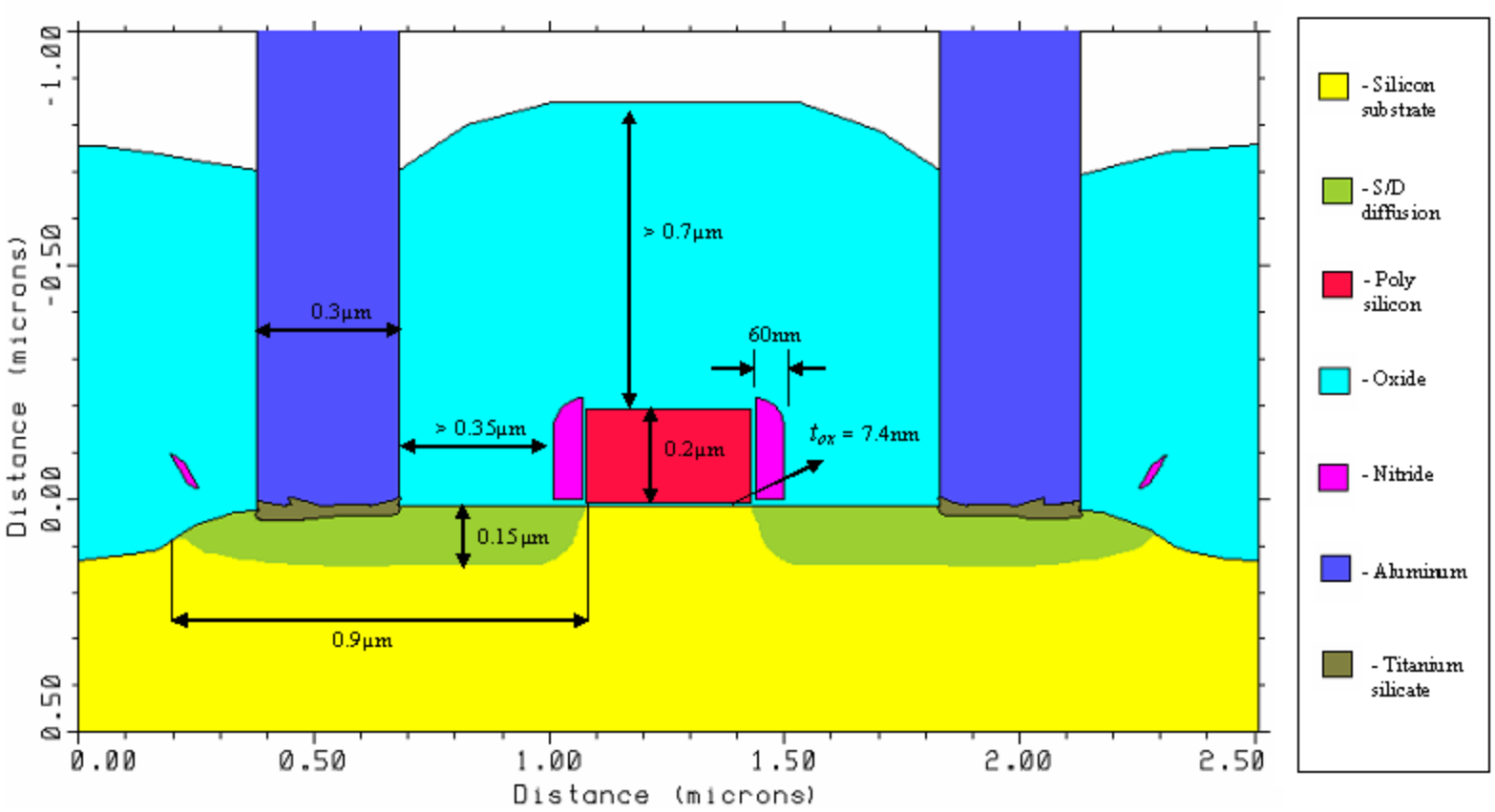
```
ETCH    DONE                X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4))     Y=0
$ Print layer thicknesses through S/D
SELECT    Z=1
PRINT.1D   X.VALUE=0.65  LAYERS
DEPOSIT   MAT=TITANIUM  THICK=0.03  SPACES=4
METHOD PD.FERMI
DIFFUSION TIME=1.287 TEMP=650
ETCH MAT=TITANIUM ALL
SELECT    Z=LOG10(BORON)
+ TITLE="B doping after S/D activation (LD=@LD)"
PLOT.1D    X.VALUE=((((1.08*2)+ @LD)/2)- @LD/2) LEFT=-0.05 RIGHT=0.4
+ BOTTOM=15 TOP=20 LINE.TYP=1 COLOR=2
$ BPSG deposition and etch to open windows for aluminum contact
DEPOSIT    OXIDE  THICK=0.6 SPACES=10
ETCH    OXIDE START      X=0.38          Y=0.2
ETCH    CONTINUE X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4))      Y=0.2
ETCH    CONTINUE X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4))      Y=-0.9
ETCH    DONE                X=0.38          Y=-0.9
ETCH    OXIDE START      X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4))     Y=0.2
ETCH    CONTINUE X=(((1.08*2)+ @LD)-0.38)     Y=0.2
ETCH    CONTINUE X=(((1.08*2)+ @LD)-0.38)     Y=-0.9
ETCH    DONE        X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4))     Y=-0.9
$ Metallization and etch to create a source/drain contact
```

```
DEPOSIT    MATERIAL=ALUMINUM  THICK=0.6  SPACES=6

ETCH   ALUMINUM  START    X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4)) Y=-0.3

ETCH      CONTINUE          X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4)) Y=-0.3

ETCH      CONTINUE          X=((((1.08*2)+ @LD)/2)+(@LD/2+0.4)) Y=-1.5

ETCH      DONE        X=((((1.08*2)+ @LD)/2)-(@LD/2+0.4))  Y=-1.5

ETCH     ALUMINUM LEFT P1.X=0.38

ETCH     ALUMINUM RIGHT P1.X=(((1.08*2)+ @LD)-0.38)

$ Save the file in Tsuprem-4 format

SAVEFILE   OUT.FILE=nmos35T

$ Print the layer thicknesses after metallization along gate poly, spacers

SELECT     Z=1

PRINT.1D   Y.VALUE=-0.05  LAYERS

$ Mesh plotting after LDD anneal

SELECT     TITLE="After METAL ETCH"

PLOT.2D    SCALE GRID Y.MAX=1.0 C.GRID=2

$ Plot final structure (shown in Appendix B)

SELECT     TITLE="Final Structure for LD=@LD"

PLOT.2D    SCALE   Y.MAX=0.5

COLOR           SILICON COLOR=7

COLOR           OXIDE   COLOR=5

COLOR           POLY    COLOR=3

COLOR           ALUMI   COLOR=2

PLOT.2D    ^AX  ^CL
```

```
$ Print S/D Junction Depth
SELECT          Z=DOPING
PRINT.1D   LAYERS X.VALUE=0.65
$ Print the S/D doping
SELECT     Z=LOG10(ARSENIC)
PLOT.1D    X.VALUE=0.65 LEFT=0.0 RIGHT=1.5 BOTTOM=14 TOP=22
+ LINE.TYP=1 COLOR=2
LABEL      X=0.3  Y=18.5  LABEL="Arsenic conc"  LINE.TYP=1  C.LINE=2
SELECT     Z=LOG10(Act(ARSENIC))
PLOT.1D    ^AX  ^CL   X.VALUE=0.65 LEFT=0.0 RIGHT=1.5 BOTTOM=14
+ TOP=22 LINE.TYP=1 COLOR=3
LABEL      X=0.3  Y=17.5  LABEL="Active Arsenic conc"  LINE.TYP=1  C.LINE=3
$ Define Electrode
$ELECTRODE  X=(((1.08*2)+ @LD)/2)     Y=-0.05    NAME=GATE
ELECTRODE  X=0.65                  Y=-0.3    NAME=SOURCE
ELECTRODE  X=((1.08*2)+ @LD)-0.65  Y=-0.3    NAME=DRAIN
ELECTRODE  BOTTOM    NAME=BULK
$ Save in MEDICI format to be used by medici simulations in Appendix C
SAVEFILE   OUT.FILE=nmos350nmt  MEDICI  ELEC.BOT
$ Extract Threshold Voltage
ELECTRIC   X=(((1.08*2)+ @LD)/2) THRESHOLD NMOS V="0 2 0.1"
SELECT     TITLE="Threshold Voltage"
PLOT.1D    ELECTRIC
```

```
$ Extract Junction Capacitance
ELECTRIC   X=0.65  JCAP  JUNCTION=1   V="0 5 0.1"
SELECT     TITLE="S/D Junction Capacitance"
PLOT.1D    ELECTRIC
$ Print Channel Length
SELECT Z=DOPING
PRINT.1D  LAYERS   Y.V=0.0007
$ Print S/D Depth
SELECT Z=DOPING
PRINT.1D  LAYERS   X.V=0.65
$ Print LDD Depth
SELECT Z=DOPING
PRINT.1D LAYERS   X.V=((((1.08*2)+ @LD)/2) - (@LD/2))
STOP
```

Appendix B: Simulated Test structure of a 0.35µm MOSFET from TSUPREM-4



Appendix C: Medici input files for device simulations

C.1 Initial mesh and zero carrier solution

```
$ Initial solution for NMOS Transistor using Medici
$ Import Mesh file from TSUPREM-4
$ Define electrode on gate poly and bottom of the substrate
MESH   TSUPREM4  IN.FILE=nmos350nmt  Y.MAX=1.5  POLY.ELEC   ELEC.BOT
$ Define interface charge
INTERFAC  QF=5E10
$ Plot initial grid
PLOT.2D   GRID  TITLE="Initial Mesh Grid"  FILL  SCALE
+         Y.MAX=1.5 T.SIZE=0.3   X.SIZE=0.2 Y.SIZE=0.2
$ Define source and drain contacts
CONTACT   NAME=SOURCE  ALUMINUM
CONTACT   NAME=DRAIN   ALUMINUM
$ Grid Refinement based on doping gradients
REGRID    DOPING  LOG  RATIO=1  SMOOTH=1
PLOT.2D   GRID  TITLE="Mesh after Doping Regrid"  FILL SCALE
+         Y.MAX=1.5 T.SIZE=0.3   X.SIZE=0.2 Y.SIZE=0.2
$ Specify physical models to use
MODELS   CONMOB  FLDMOB PRPMOB CONSRH EJ.MOBIL
$ Symbolic Factorization and Solve only Poisson for zero potential
SYMB     CARRIERS=0
```

```
SOLVE
$ Grid Refinement Based on Potential ; Save initial mesh for later use
REGRID    POTEN  RATIO=0.1  MAX=1  SMOOTH=1 OUT.FILE=BIAS0_MSH
PLOT.2D   GRID  TITLE="Mesh after Potential Regrid"  FILL  SCALE
+         Y.MAX=1.5 T.SIZE=0.3   X.SIZE=0.2 Y.SIZE=0.2
$ Solve Using Refined Grid ; Save initial solution for later use
SYMB      CARRIERS = 0
SOLVE     OUT.FILE = BIAS0_SOL
STOP
```

C.2 Two-carrier solutions to build up gate bias

```
$ DC Device Simulation of a 0.35u NMOS Transistor using MEDICI
COMMENT   Calculate Gate Characteristics
COMMENT   Solution for different Gate bias (VDS=0V)
COMMENT   Read in simulation mesh
MESH      IN.FILE=BIAS0_MSH
COMMENT   Read in saved solution
LOAD      IN.FILE=BIAS0_SOL
COMMENT   Use Newton's method for the solution
SYMB      NEWTON  CARRIERS=2
COMMENT   Setup log file for data
LOG       OUT.FILE=VG
$ Starting solution for off-state simulation & extrinsic parameters
SOLVE             OUT.FILE=VG00VD00_S
```

```
$Sample RF simulation for GD (common-source) configuration upto 25.1GHz
LOG     OUTFILE = YGD_VG00VD00
SYMB     NEWTON  CARRIERS=2
SOLVE          AC.ANALY       HI.FREQ       FREQUENC=100e6       FSTEP=500e6
NFSTEP=51
+          TERM=(GATE,DRAIN)
$ Build the gate voltage in steps of 0.2V up to 3.2V
$ Use two-carrier Newton's method - Required by RF simulations later
SYMB     NEWTON  CARRIERS=2
SOLVE          V(gate)=0.2
$ Note: Regular re-grids based on potential and electron concentration
$ are necessary for accurate RF simulations
$ Re-grid based on potential and solve
REGRID    POTEN  REGION=1 RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
$ Re-grid based on electron concentration and solve
REGRID    ELECTRON  LOG  REGION=1 FACTOR=1.02  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
SYMB     NEWTON  CARRIERS=2
SOLVE          V(gate)=0.4
REGRID    POTEN  REGION=1 RATIO=0.1  MAX=1  SMOOTH=1
```

```
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID   ELECTRON  LOG  REGION=1 FACTOR=1.02  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
SYMB     NEWTON  CARRIERS=2
SOLVE          V(gate)=0.6
REGRID   POTEN  REGION=1 RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID   ELECTRON  LOG  REGION=1 FACTOR=1.02  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
…
…
…
$ Similarly build gate voltage up to 3.2V in steps of 0.2V
…
…
SYMB     NEWTON  CARRIERS=2
SOLVE          V(gate)=3.0
REGRID   POTEN  REGION=1 RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
```

```
SOLVE
$ Save mesh and solution for building drain voltage and
$ carrying out RF simulations at VGS=3V
REGRID    ELECTRON  LOG  REGION=1 FACTOR=1.01  SMOOTH=1
+ OUT.FILE=VG30VD00_MSH
SYMB      NEWTON  CARRIERS=2
SOLVE             OUT.FILE=VG30VD00_S
SYMB      NEWTON  CARRIERS=2
SOLVE             V(gate)=3.2
REGRID    POTEN  REGION=1 RATIO=0.1  MAX=1  SMOOTH=1
SYMB      NEWTON  CARRIERS=2
SOLVE
REGRID    ELECTRON  LOG  REGION=1 FACTOR=1.01  SMOOTH=1
SYMB      NEWTON  CARRIERS=2
SOLVE
STOP
```

C.3 Building the drain bias and performing RF simulations

```
$ Device Simulation of a 0.35u NMOS Transistor using MEDICI
$ DC and AC analysis (Small-signal voltage amplitude is 2.5mV by default)
$ Read in the mesh and solution at VGS=3V from C.2
MESH      IN.FILE=VG30VD00_MSH
LOAD      IN.FILE=VG30VD00_S
LOG      OUTFILE = DC_VG30VD00
```

```
SYMB      NEWTON  CARRIERS=2
SOLVE     OUT.FILE= SOL
$ Perform AC analysis in GD from 100MHZ to 25.1GHz at VDS=0V
LOG       OUTFILE = YGD_VG30VD00
SYMB      NEWTON  CARRIERS=2
SOLVE             AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+         NFSTEP=51   TERM=(GATE,DRAIN)
$ Perform AC analysis in GS from 100MHZ to 25.1GHz at VDS=0V
LOAD              IN.FILE = SOL
LOG       OUTFILE = YGS_VG30VD00
SYMB      NEWTON  CARRIERS=2
SOLVE             AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+         NFSTEP=51   TERM=(GATE,SOURCE)
$ Perform AC analysis in SD from 100MHZ to 25.1GHz at VDS=0V
LOAD              IN.FILE = SOL
LOG       OUTFILE = YSD_VG30VD00
SYMB      NEWTON  CARRIERS=2
SOLVE             AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+         NFSTEP=51   TERM=(SOURCE,DRAIN)
$ Initial drain bias steps are chosen very close to each other
$ for effective capture of DC and RF behavior
MESH      IN.FILE=VG30VD00_MSH
LOAD              IN.FILE=SOL
```

```
SYMB     NEWTON  CARRIERS=2
SOLVE    V(drain)=0.0125
REGRID   POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
$ Store the mesh and solution for solving at next bias point
REGRID              ELECTRON   LOG   REGION=1   FACTOR=1.03   SMOOTH=1
OUT.FILE=MSH
SYMB     NEWTON  CARRIERS=2
SOLVE    OUT.FILE=SOL
$ Read in earlier mesh and solution for solving at bias point
MESH     IN.FILE=MSH
LOAD             IN.FILE=SOL
SYMB     NEWTON  CARRIERS=2
SOLVE    V(drain)=0.025
REGRID   POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID              ELECTRON   LOG   REGION=1   FACTOR=1.03   SMOOTH=1
OUT.FILE=MSH
SYMB     NEWTON  CARRIERS=2
SOLVE    OUT.FILE=SOL
```

```
MESH     IN.FILE=MSH
LOAD             IN.FILE=SOL
SYMB     NEWTON  CARRIERS=2
SOLVE    V(drain)=0.05
REGRID   POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID             ELECTRON   LOG   REGION=1   FACTOR=1.03   SMOOTH=1
OUT.FILE=MSH
SYMB     NEWTON  CARRIERS=2
SOLVE    OUT.FILE=SOL
MESH     IN.FILE=MSH
LOAD             IN.FILE=SOL
SYMB     NEWTON  CARRIERS=2
SOLVE    V(drain)=0.075
REGRID   POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID             ELECTRON   LOG   REGION=1   FACTOR=1.03   SMOOTH=1
OUT.FILE=MSH
SYMB     NEWTON  CARRIERS=2
SOLVE    OUT.FILE=SOL
```

```
MESH      IN.FILE=MSH
LOAD              IN.FILE=SOL
SYMB      NEWTON  CARRIERS=2
SOLVE     V(drain)=0.1
$ Note: Regular re-grids based on potential and electron
$ concentration  are necessary for accurate RF simulations
$ Otherwise capacitance trends will not be smooth
$ Re-grid based on potential and solve
REGRID    POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
SYMB      NEWTON  CARRIERS=2
SOLVE
$ Re-grid based on electron concentration and solve
REGRID              ELECTRON    LOG    REGION=1    FACTOR=1.03    SMOOTH=1
OUT.FILE=MSH
LOG      OUTFILE = DC_VG30VD01
SYMB      NEWTON  CARRIERS=2
SOLVE     OUT.FILE=SOL
$ Perform AC analysis in GD from 100MHZ to 25.1GHz at VDS=0.1V
LOG      OUTFILE = YGD_VG30VD01
SYMB      NEWTON  CARRIERS=2
SOLVE             AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(GATE,DRAIN)
$ Perform AC analysis in GS from 100MHZ to 25.1GHz at VDS=0.1V
```

```
LOAD            IN.FILE = SOL
LOG     OUTFILE = YGS_VG30VD01
SYMB     NEWTON  CARRIERS=2
SOLVE           AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(GATE,SOURCE)
$ Perform AC analysis in SD from 100MHZ to 25.1GHz at VDS=0.1V
LOAD            IN.FILE = SOL
LOG     OUTFILE = YSD_VG30VD01
SYMB     NEWTON  CARRIERS=2
SOLVE           AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(SOURCE,DRAIN)
...
...
...
$ Similarly build up VDS up to 3.2V and carry out RF simulations
$ in all 3 two-port configurations (GD, GS and SD)
...
...
MESH     IN.FILE=MSH
LOAD   IN.FILE=SOL
SYMB     NEWTON  CARRIERS=2
SOLVE     V(drain)=3.2
REGRID    POTEN  REGION=1  RATIO=0.1  MAX=1  SMOOTH=1
```

```
SYMB     NEWTON  CARRIERS=2
SOLVE
REGRID          ELECTRON      LOG      REGION=1   FACTOR=1.02   SMOOTH=1
OUT.FILE=MSH
LOG     OUTFILE = DC_VG30VD32
SYMB     NEWTON  CARRIERS=2
SOLVE     OUT.FILE=SOL
$ Carry RF simulations and log the outputs of each configuration in separate files
LOG     OUTFILE =YGD_VG30VD32
SYMB     NEWTON  CARRIERS=2
SOLVE           AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(GATE,DRAIN)
LOAD            IN.FILE=SOL
LOG     OUTFILE =YGS_VG30VD32
SYMB     NEWTON  CARRIERS=2
SOLVE           AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(GATE,SOURCE)
LOAD            IN.FILE=SOL
LOG     OUTFILE =YSD_VG30VD32
SYMB     NEWTON  CARRIERS=2
SOLVE           AC.ANALY HI.FREQ FREQUENC=100e6 FSTEP=500e6
+          NFSTEP=51   TERM=(SOURCE,DRAIN)
STOP
```