DESIGN OF A CORRELATOR FOR UWB TRANSCEIVERS

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PUBLICATIONS

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- *Ong Hwee Woon, Zhou Lei and Tian Tong*, "**Research and characterization on the multi-path effect in UWB channel**", Presented in International Symposium on Integrated Circuits, Devices and Systems (ISIC) 2004, Singapore.
- *Zhou Lei, Tian Tong and Xu Yong Ping*, "**Si CMOS sub-nano pulse integrator for UWB system**", Presented in International Symposium on Integrated Circuits, Devices and Systems (ISIC) 2004, Singapore.

CONFERENCE PARTICIPATIONS

Oral presentation at International Symposium on Integrated Circuits, Devices and Systems (ISIC) 2004, Singapore.

CONTENTS

SUMMARY

The thesis describes the design and implementation of a wideband analog correlator for UWB transceivers. UWB signal is characterized with low power narrow pulses with very wide spectrum up to 7.5 GHz, which imposes the challenge in UWB front-end circuit design.

The analog time integrating correlator consists of a transconductor based multiplier and a transconductor-C integrator. In order to increase the bandwidth of the multiplier, a pole-zero cancellation technique is proposed. Similar to the shunt-peaking technique, an inductor is added at the output of the multiplier. With a properly chosen inductance value, the dominant pole located at an internal node can be cancelled by the zero introduced by the inductor. The simulation has shown that the bandwidth can be increased by 5 times from 2 GHz to 10 GHz. The transconductor in the integrator is implemented with a simple inverter that operates in the saturation region. Such a transconductor is chosen for its simple topology and fast response. In addition, the DC gain enhancement is enhanced with negative resistance circuit at the output of the integrator, which effectively increases the overall output resistance of the integrator.

The chip is fabricated in a commercial 0.18-μm CMOS process and operates under a 1.8-V supply. The test results show that the correlator is able to operate with an input

of 0.2-ns narrow monocycle pulse at 50-MHz repetition rate and produce a correct integrated output. The power consumption of the correlator is 13.6mW.

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LIST OF SYMBOLS & ABBREVIATIONS

Symbols

a	Coefficient in polynomial
C	Integration capacitor
C_L	Load capacitor
C_{OX}	Gate oxide capacitance per unit area
ΔI	Differential current signals
f	Frequency
g_m	Transconductance of the MOS transistor
g_{mb}	Transconductance of body effect
G	Equivalent transconductance
GBW	Gain bandwidth product
I_D	DC bias current
I_{SS}	Current value of the current source in differential circuit
I_1, I_2	Current in the branch of differential pairs
K	Transistor characteristic parameter
K_{eff}	Equivalent K considering mobility degeneration
lo	Differential signals in wideband multiplier of large power
L	Length of the transistor
M	Transistor
Q	Inductor quality factor

r_{ds}	Output resistance of the transistor
rf	Differential signals in wideband multiplier of small power
R	Load resistor
RF, LO	Common mode signals in wideband multiplier
R_L	Load resistor
s	Laplacian
T	Absolute temperature
μ_n, μ_p	Mobility of electron
v_{GS}	Differential gate-source voltage
v_x, v_y	Differential signals
v_X, v_Y	Common mode voltage
V_{dd}	Voltage supply
V_{ss}	Ground
V_C	Bias voltage
V_{DS}	Drain-source voltage
V_{GS}	Common mode gate-source voltage
V_T	Threshold voltage
w	Radian frequency
W	Width of the transistor
X	Inverter-based transconductor
Z_o	Output impedance of the wideband multiplier
Z(jw)	Frequency response function

Abbreviations

UWB	Ultra Wideband
WPAN	Wireless Personal Area Network
WLAN	Wireless Local Area Network
WBAN	Wireless Body Area Network
FCC	Federal Communication Commission
HDR	High Data Rate
LDR	Low Data Rate
ISM	Industrial, Scientific and Medical
RF	Radio Frequency
ADC	Analog-to-Digital Converter
LNA	Low Noise Amplifier
VGA	Variable Gain Amplifier
TIC	Time-Integrating Correlator
PCB	Printed Circuit Board
SMA	SubMiniature version A

CHAPTER 1 INTRODUCTION

1.1 About UWB

1.1.1 What is UWB?

Wireless Personal Area Networks (WPANs) aim at the communication among personal devices within a relatively close distance. Different from Wireless Local Area Networks (WLANs), communication channel environment in WPANs includes more peer to peer connection other than connection with infrastructures. This characteristic enable tiny, power saving and cheap scheme to be achieved for a large mount of components [1].

Ultra Wideband (UWB) is a new wireless radio technology for commercial application which has potential to be used for high speed data transmission or long distance location. Taking the advantage of high bandwidth, point-to-point high speeds data transmission between laptop, pocket devices and peripheral consumer handheld within a short distance with low emission is possible, as well as the location tracking through low data rate communication without affecting the existing wireless systems. The UWB pulse signal is difficult to detect, which protects the data in communication by transmitting the low power signals below the noise floor over a larger frequency range than conventional narrowband systems. UWB system is defined by Federal Communication Commission (FCC) to transmit a pulse signal with a spectrum occupation, which is at least 25% of the central frequency. For example, a pulse signal

which is centered at 6GHz, must occupy a bandwidth of more than 1.5GHz to be called as a wideband signal. Therefore a pulse signal with a duty cycle less than 10%, which is about 1 nanosecond, is commonly regarded as a UWB signal.

If the entire 7.5 GHz band is optimally utilized, the maximum power available to a transmitter is approximately 0.5 mW. This is a tiny fraction of what is available to users of the 2.45 GHz Industrial, Scientific and Medical (ISM) bands such as the IEEE 802.11a/b/g standards. This effectively relegates UWB to indoor, short-range communications for high data rates (HDR), or very low data rates (LDR) for substantial link distances. Applications such as wireless UWB and personal area networks have been proposed with hundreds of Mbps to several Gbps with distances of 1–4 m. For ranges of 20 m or more, the achievable data rates are very low compared to existing Wireless Local Area Network (WLAN) systems [2-4].

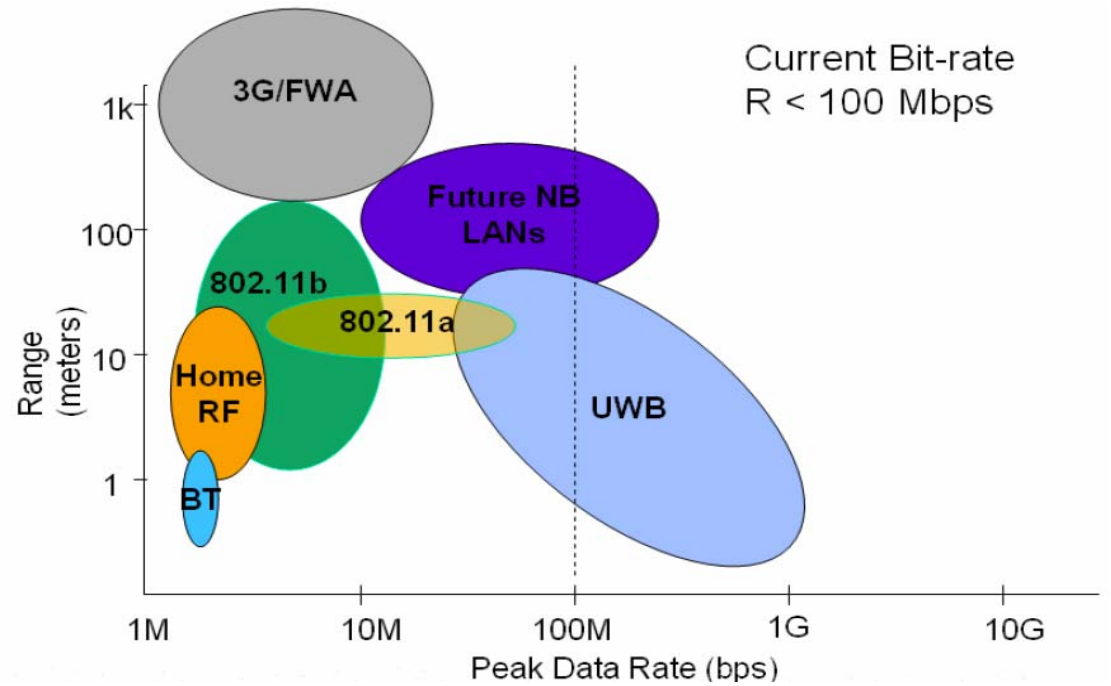


Fig. 1-1 Comparison of UWB with existing WLAN/WPAN system [5].

1.1.2 Why UWB?

"Go wireless" is an emerging trend in communication network nowadays. Although narrow band wireless technology provides a lot of convenience to the consumers, high speed transmission is lacking for short range transmission between pc peripherals and consumer electronics. This has stimulated the researchers to seek ultra wideband (UWB) technology for a performance solution. With the connection speed ranging from 100Mbps to 1Gbps, UWB systems provide a high data rate connection between devices while keeping power consumption at a level low enough without being detected. With the potential of high data rate, a true synchronization within contents such as contacts, multimedia files and notes in different personal sets can be achieved so fast that people will omit the fact that those files are stored on other devices.

The potential application in enormous fields where wireless communication network facilitate the work has greatly boosted up the development of this technology. UWB systems have been targeted at very HDR applications over short distances, such as Wireless USB, as well as very LDR applications over longer distances, such as sensors and RF tags [2]. Fig. 1-2 shows multiple application areas in the life considered by PULSE (a European Union project), which cover WPAN, WBAN, sensor and positioning networks.

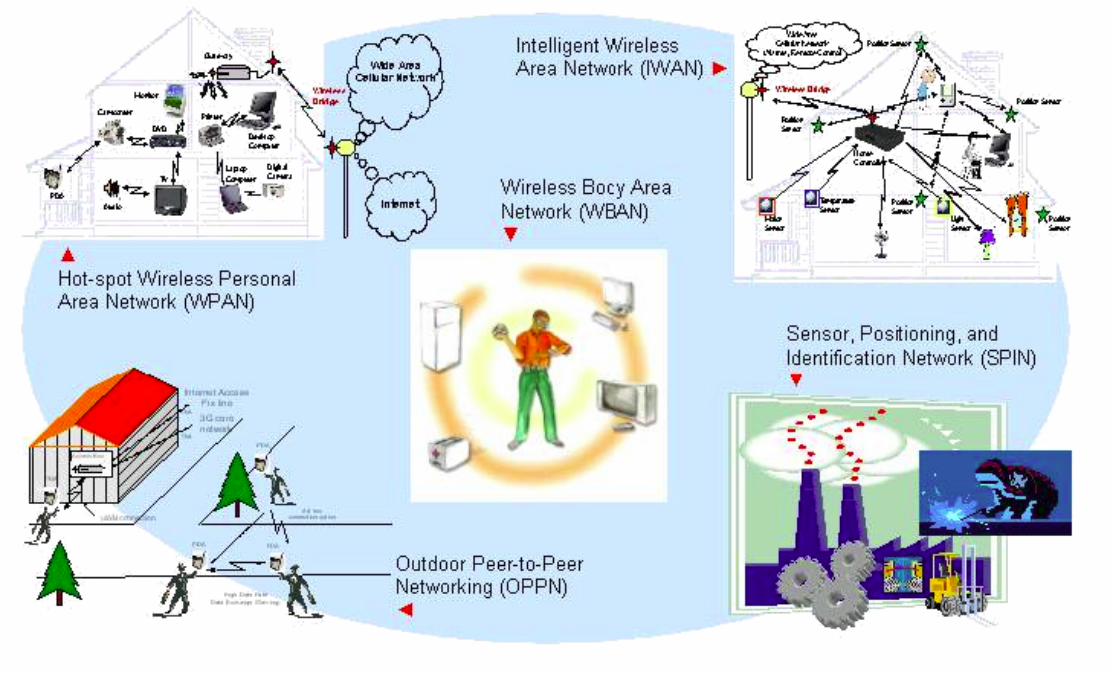


Fig. 1-2 Possible applications for UWB technology [6].

1.1.3 Advantage of UWB

UWB technology has many advantages, including simple transceiver structure, low cost, low power, multipath resistance and the suitability for location.

The low complexity and cost benefit from the simple structure of the transceiver, which is different from conventional narrow band communication system. In the conventional communication system, a baseband signal is mixed with a higher frequency carrier to a radio frequency signal for data transmission in the desired wireless channel. However, in the UWB transmitter, a very short pulse in time duration has the wideband nature which makes it is spanned to the frequencies often used as radio frequencies. Therefore, the baseband signal can pass through the UWB restricted transmission channel without the need for an up-conversion mixer.

Similarly, in the receiver side, an analog correlator as a direct down conversion match filter is applied as a substitute of the traditional downconversion mixer. In addition, many researches are focused on low-cost CMOS implementation of UWB transceivers.

Since the low duty cycle of pseudo random pulse signals, the pulses transmitted in the channel look like thermal noise because of power concentration at very short time in one repetition period. Therefore the UWB systems have the character of good security for the undetectable noise-like signals at a low energy level [2,7]. Recently, the interference to the existing wireless networks, such as 802.11b wireless LAN is studied and the results show that UWB signal has a good resistance to the multipath due to large bandwidth [8].

The UWB transceiver is an impulse radio system with time modulation technique which is reported to be able to support more users than narrowband system. High data rate can be achieved by the wide bandwidth and the time-modulation technique. The short time pulses in one period also exhibit good performance for timing. Because of the good penetration of pulse signals through various materials, the sensors which transmit and receive UWB pulses can potentially be applied for locating.

1.2 UWB Transceiver Architecture

IR-UWB is often known as impulse or carrier less radio technology where the modulated baseband signal can be directly transmitted. This has greatly reduced the complexity of transceiver architecture and RF front-end circuit design, compared to the narrowband receivers. In a typical receiver structure of an impulse radio system, analog-to-digital converter (ADC) is inserted just after low-noise amplifier (LNA) and variable-gain amplifier (VGA) from the antenna, to implement much of the signal processing in the digital part [9].

Although the system architecture is easy to implement, this scheme is not a low-power consumption solution. One possible way to save power without degrading the performance is to move some algorithms to analog domain implementation. That is why a time-integrating correlator is inserted before ADC after VGA. Such a correlator integrates multiple pulses to recover the transmitted information. The whole system block diagram of an impulse radio UWB receiver is shown in Fig. 1-3. A UWB receiver contains a precise pulse generator, which provides a periodic timing signal on the side of a receiver. The local template pulse is triggered by the coded timing signal and produces a series of template signal pulses ideally with the sequence of all the possible transmitted signals. The role of the correlator is to convert the received RF signal to baseband for detection [10]. In a typical spread spectrum receiver, the correlator slides the received signal past a reference code sequence. When the received signal and the reference pulse are synchronized in phase, a peak

emerges to complete the correlation process [11]. The analog correlator consists of a wideband multiplier followed by an integrator [12-15]. The two inputs to the correlator, or the multiplier, are the input monopulse signal and its template generated by the pulse generator. The product of these two input signals at the output of the multiplier is further integrated to produce a robust signal level for A-to-D conversion.

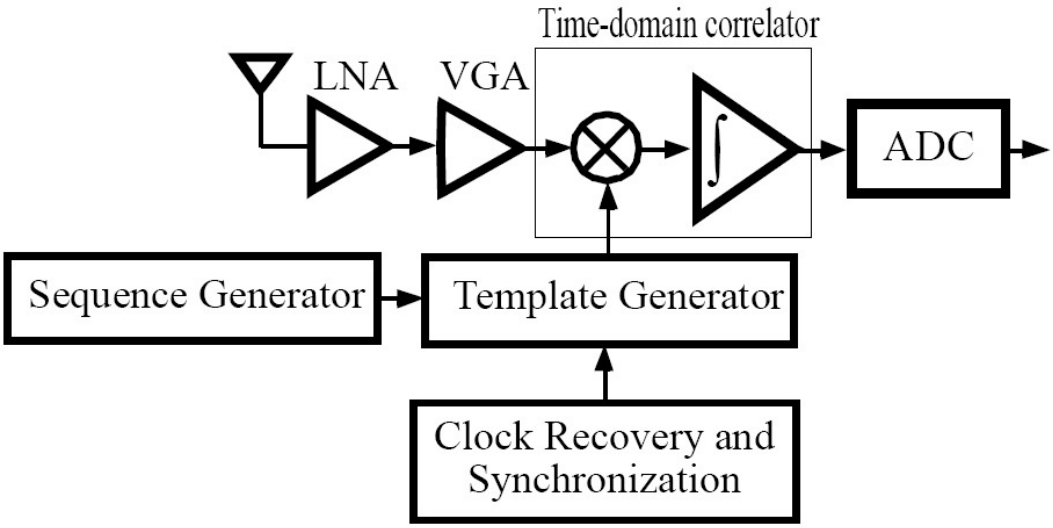


Fig. 1-3 Block diagram of an impulse-radio UWB receiver with a time-integrating correlator [9].

Clearly, designing a front-end circuit in UWB transceivers will face a great challenge in the implementation using low cost CMOS device due to stringent requirements of the UWB technology. For instance, since the free bandwidth of UWB opened by FCC is from 3.1~10.6GHZ, this implies that LNA and correlator in the transceiver front-end should have very wide bandwidth to process signals over the whole frequency spectrum. This is a key challenge to the front-end circuit design besides low power requirement.

1.3 Scope of the Thesis

To best utilize the whole UWB spectrum specified by FCC, it is very challenging for the design of the front end circuits, especially when CMOS technology is used, due to wideband and gain requirement, as well as low power consumption. The scope of this thesis is to design a wideband analog correlator for pulse radio based UWB transceiver using 0.18-μm CMOS technology. The targeted application for the UWB transceiver is the high data rate communication. It also can be used for location due to the simplicity of the analog correlator.

The two input signals of the correlator are narrow monocycle pulses, which cover 7.5GHz bandwidth from 3.1GHz to 10.6GHz. The pulse repetition frequency (PRF) of the input UWB pulses is up to 100 MHz. The integrated output signal from the correlator should be hold for a reasonably long period (nearly 10ns) for the subsequent A-to-D conversion.

1.4 Organization of the Thesis

Chapter 2 reviews the previous work on the design of two sub-circuits, multiplier and integrator, and discusses their advantages and disadvantages.

Chapter 3 describes the correlator design. The first part of this chapter deals with the multiplier design. Two multipliers are designed, namely, an active wideband multiplier and a passive one. The second part is about the design of the integrators,

where an inverter based integrator and its improved version are described. The correlator implemented by the above multiplier and integrator is also described and presented with the post-layout simulation results.

Chapter 4 presents the measurement result of the fabricated correlator. Discussion is given to explain the phenomenon observed in the measurement.

Chapter 5 concludes all the work in this project and proposes some suggestions for the future plan.

CHAPTER 2 OVERVIEW OF MULTIPLIERS AND INTEGRATORS

The correlation process contains two steps: multiplication of two signals (*x(t), y(t)*), followed by the integration for a period of time. Mathematically, the correlation of two signals can be expressed as $R_{xy}(\lambda) = \int_0^T x(t)y(t+\lambda)dt$. λ is the time offset between two signals with the same period T. A larger correlation value $R_{xy}(\lambda)$ represents a strong similarity between the two signals, while a value near zero represents little similarity. Therefore the design of a time-integrating correlator is divided into two parts: multiplier and integrator design. In this chapter, previously reported multipliers and integrators are reviewed. Because the bandwidth of the multiplier is a critical requirement in the analog correlator design, different techniques on bandwidth enhancement are also discussed at the end of this chapter.

2.1 Multiplier Designs

At first, the concept of the multiplier seems confused with that of the mixer. Multiplier is the multiplication process of two input signals, while mixer performs frequency translation. As far as the application is concerned, the multiplier is more general than mixer and focuses more on time domain performance, while mixer more on the frequency domain. There are several ways to design an analog multiplier. Through comparison of different structures in this chapter, architecture to implement the multiplier for the correlator in UWB transceiver will be decided.

2.1.1 Passive multiplier

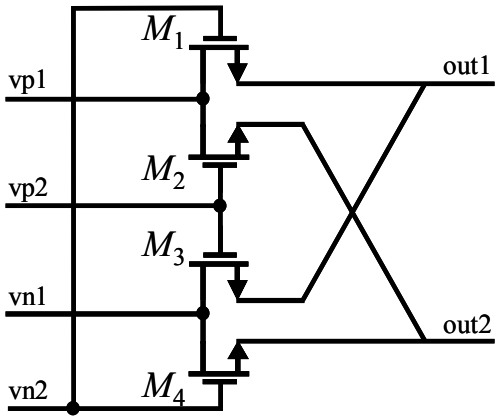


Fig. 2-1 Passive multiplier structure and its symbol [16].

The passive multiplier has been used as a part of the analog correlator in WCDMA receiver [16]. The multiplier is composed of four PMOS transistors operating as switches. The spread spectrum pseudo random codes control the switches to commute the input signals to the output encoded signals. Fig. 2-2 shows the multiplication relation of the input and output signals in time domain analysis.

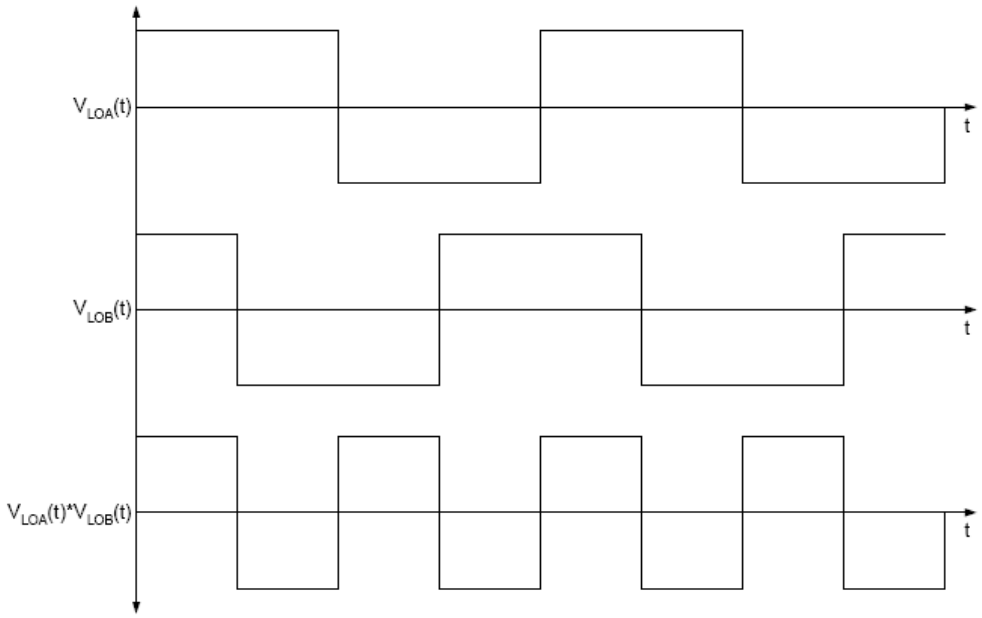


Fig. 2-2 Function demonstration of a passive multiplier [17].

The advantage of this passive multiplier is the response time to wideband signal due to the fast operating speed of switches. However, due to the mobility difference of PMOS and NMOS transistors, the counter-part NMOS version passive multiplier has better performance in dealing with high frequency pulse signals. Considering the over-drive voltage of PMOS and NMOS in switch region, a symmetric switch combined with both PMOS and NMOS transistors is employed in the passive multiplier. However, the passive character limits its application in UWB front-end, because there is a gain loss. Since FCC (Federal Communications Commission) sets the limit to UWB pulse transmitted power, the received signal from the antenna before multiplier is only -60dBm. Without reasonable processing gain, the weak signal will be hidden in the background noise and impossible to be detected.

This is the reason why sometimes active multipliers, which can provide sufficient gain, are preferred over the passive ones. However, passive multiplier does have its own advantages, such as low power consumption and high speed.

2.1.2 Active multiplier

Although active multiplier shows better processing gain over passive one, the wide bandwidth and power consumption are among the most difficult problems in the application of wireless communication.

A most common structure in high frequency CMOS circuit design is transconductor. To design a high speed CMOS analog multiplier, an obvious way is to use transconductor structure. Several multiplier structures have been reported in [18]. However, all will fall into two categories according to the operation conditions of MOS devices, that is, the multipliers in which transistors are operating in the saturation and in the triode region, respectively. Since a single-ended configuration cannot achieve complete cancellation of nonlinearity and has poor power supply rejection ratio (PSRR), a fully differential configuration is preferred for better liniearity. The multiplier has two inputs, therefore there are four combinations of two differential signals, i.e., (x,y), (-x,y), (x, -y) and (-x, -y). The topology of the Fig. 2-3 below is based on single-quadrant multiplier and the other is based on square law devices. These topologies achieve multiplication and simultaneously cancel out all the higher order and common-mode components (X and Y) based on the following equations:

$$[(X+x)(Y+y)+(X-x)(Y-y)]-[(X-x)(Y+y)+(X+x)(Y-y)]=4xy \tag{1.1}$$

$$\{[(X+x)+(Y+y)]^2+[(X-x)+(Y-y)]^2\}-\{[(X-x)+(Y+y)]^2+[(X+x)+(Y-y)]^2\}=8xy \tag{1.2}$$

x, y represents small signals, and X,Y denotes the DC bias voltages.

We note that these equations are very similar to two situations of the I-V characteristic of MOS transistors. Thus it is common to use CMOS to implement the cancellation schemes. The simple I-V models of CMOS transistors [19] are given below:

$$I_d = K[V_{gs} - V_T - \frac{V_{ds}}{2}]V_{ds} \tag{1.3}$$

$$I_d = \frac{K}{2}[V_{gs} - V_T]^2 \tag{1.4}$$

Here, $K = \mu_0 C_{ox} \frac{W}{L}$

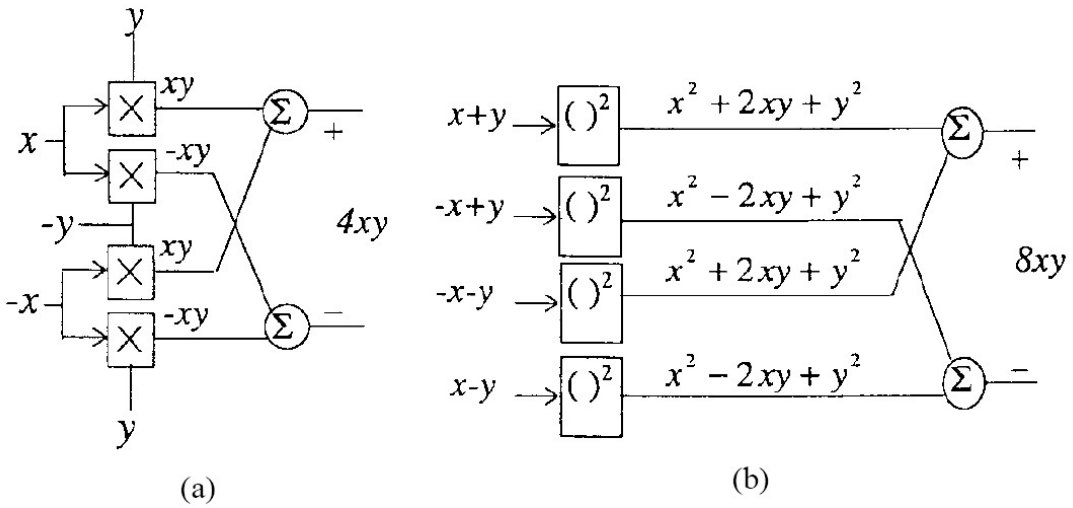


Fig. 2-3 Fout-quadrant multiplier basic architecture (a) Using transistors in linear region (b) Using transistors in saturation resign.

Since all these topologies are based on CMOS I-V characteristics, the multiplier structure is called transconductor multiplier.

A. CMOS transistors working in saturation region

Gilbert-cell is a mature design structure in bipolar analog multipliers [20]. The similar structure can be used in the case of CMOS. Let us consider about the basic CMOS Gilbert-cell [21] shown in Fig. 2-4. M1-M6 are working in saturation region with all having the same transistor size. V_C is the common mode voltage and the voltage at the source of differential transistors is V_S. The upper two differential pairs are controlled by X and the low one is controlled by Y. Referring to the simple MOS square law expression $I_D = K(V_{GS} - V_T)^2, (K = \frac{1}{2}\mu_n C_{ox} \frac{W}{L})$, Then the output current is

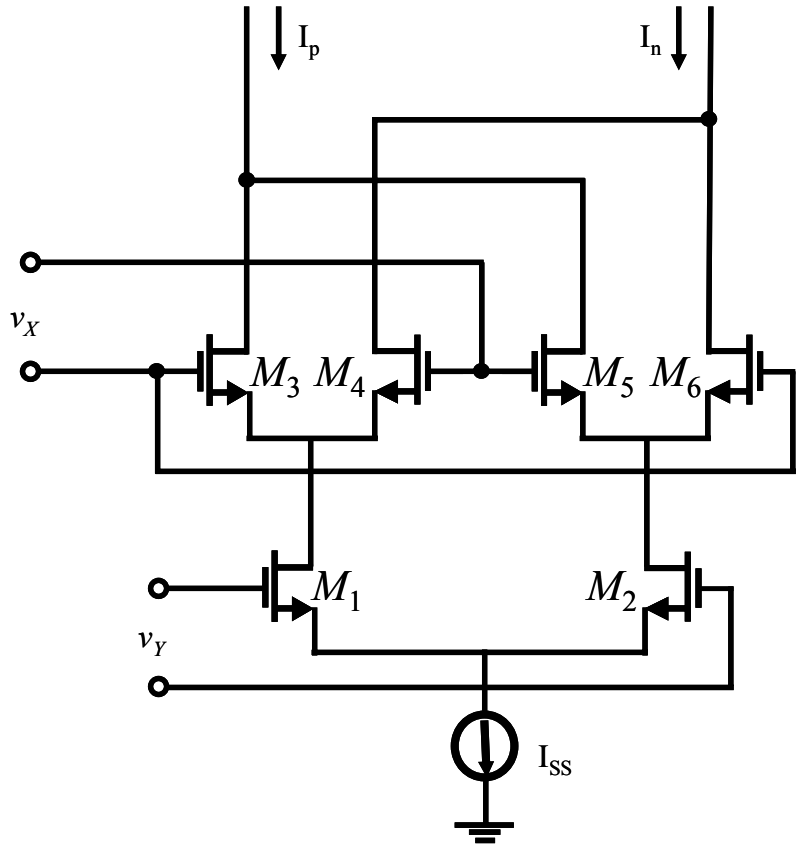


Fig. 2-4 A Gilbert cell multiplier based on CMOS devices [21].

$$I = I_p - I_n = (I_3 - I_4) - (I_6 - I_5) = Kv_X[\sqrt{(\sqrt{\frac{I_{SS}}{K} - \frac{v_Y^2}{2}} + \frac{v_Y}{\sqrt{2}})^2 - v_X^2} - \sqrt{(\sqrt{\frac{I_{SS}}{K} - \frac{v_Y^2}{2}} - \frac{v_Y}{\sqrt{2}})^2 - v_X^2}] \quad (1.5)$$

In Equation (1.5), I3, I4 and I5, I6 are differential output currents from upper two differential pairs, the tail current of each pair is also the output current of the low differential pair. From the equation, the output current is non-linear with v_X and v_Y because there is an additional v_x^2 in the part of v_Y. If the input signal is small enough to be omitted, the expression can be approximately seemed as

$$I = Kv_X[\sqrt{(\sqrt{\frac{I_{SS}}{K} - \frac{v_Y^2}{2}} + \frac{v_Y}{\sqrt{2}})^2} - \sqrt{(\sqrt{\frac{I_{SS}}{K} - \frac{v_Y^2}{2}} - \frac{v_Y}{\sqrt{2}})^2}] = \sqrt{2}Kv_X v_Y \quad (1.6)$$

Under such a requirement $-\sqrt{\frac{I_{SS}}{K}} \le v_i \le \sqrt{\frac{I_{SS}}{K}}$ on the dynamic range of input signals, the circuit can be regarded as a linear multiplier. However the non-linearity comes from the output current is not linear to the differential signal input. This limits the

input voltage of the multiplier to small values. An improved method to linearize the differential pair is proposed by adding a tail current of the multiplier which is proportion to the square of one input differential voltage. Such a linear function is achieved without omitting v_X^2 and only controlled by one input with the other input to be linearized automatically [21,22].

Although the dynamic range of the multiplier can be expanded with the improved linearity performance, the topology still has some drawbacks which limit the application in low voltage and high frequency environment due to the complexity involved in current source design.

Power consumption is another important design consideration in wireless transceiver design. The lower current source of Gilbert cell sometimes can be removed from the stack stage for larger voltage headroom, which is a useful technique for low voltage design [23].

B. Source signal injection multiplier

This circuit shown in Fig. 2-5 is a commonly used quadrant multiplier structure, which is derived from injecting signal to the source of the two pairs of cross-coupling transistors [18,24-32]. In Fig. 2-5, Ms is a source follower to implement source injection. The cross-coupling transistors are biased at saturation region to utilize the

square law cancellation scheme (1.2). Therefore the multiplication can be achieved by subtracting the differential output current.

$$\begin{aligned} I &= I_p - I_n \\ &= K[(X+x)-(Y-y)-V_T]^2 + K[(X-x)-(Y+y)-V_T]^2 \\ &-K[(X+x)-(Y+y)-V_T]^2 - K[(X-x)-(Y-y)-V_T]^2 \\ &= 8Kxy \qquad (K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}) \end{aligned} \tag{1.7}$$

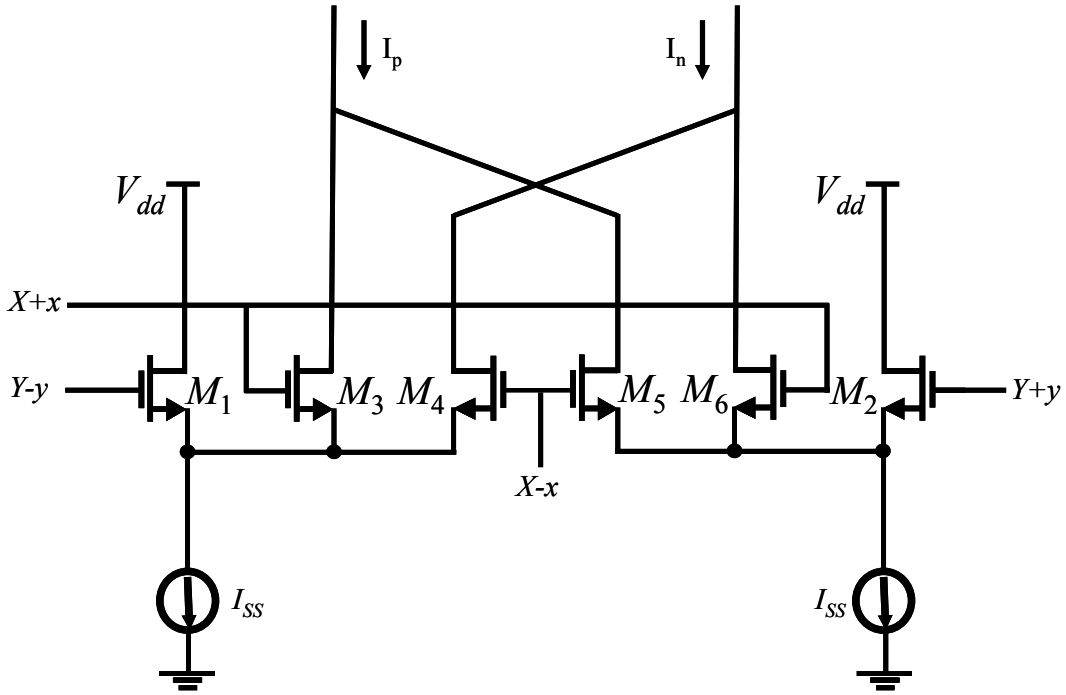


Fig. 2-5 Theory of Source injection [18].

Source follower structure seems to be an easier and more useful way to implement MOS multiplier since the two input signals can be transferred to one transistor to use the square law characteristic of MOS transistor. By symmetric cancellation scheme, a four-quadrant multiplication function can be obtained.

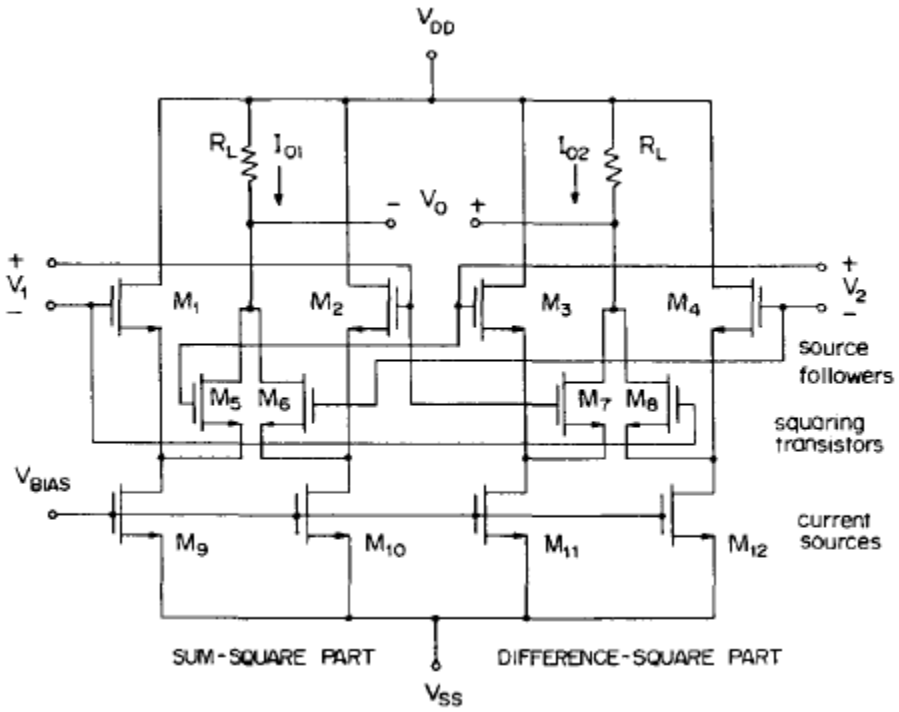


Fig. 2-6 Circuit implementation of source injection [25].

A similar structure shown in Fig. 2-6, which also takes advantage of the source follower, is proposed and analyzed in [25]. Simple summing and subtracting functions are implemented skillfully by taking the advantage of the square law of MOS device without additional adding, subtracting and squaring circuits which limits the multiplier's high frequency performance by introducing lots of parasitic capacitors. Since the linearity of the source follower affects the linearity of the output current to a great extent, increase the W/L ratio can improve the linearity of the circuit. One drawback of this structure is the high power supply voltage due to the additional current source at the tail of the source follower. Another disadvantage is the large noise figure caused by the current mirrors, which has the same g_m as the source follower and contributes higher noise floor.

In order to simplify the implementation of computational circuits for high frequency and low voltage application, a matched MOS transistor pair with two cross-coupling identical DC floating voltage sources is presented as a more efficient structure, which is shown in Fig. 2-7 [33].

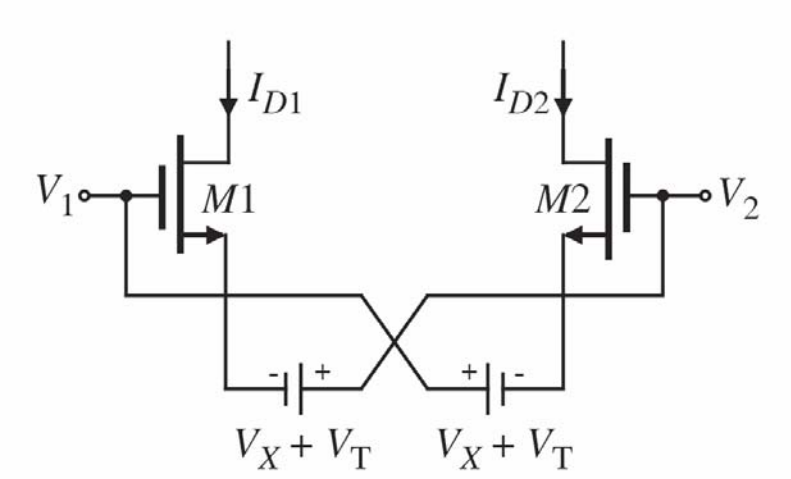


Fig. 2-7 Linear transconductor with DC floating voltage source [33].

Source followers are used as a floating voltage for simplicity. To improve the output impedance of the floating voltage source, the W/L aspect ratio of the source followers must be chosen large enough. Different ways like current [34] and voltage [35] feedback are used to reduce the output impedance at the compensation of high operation speed. Therefore a new flipped voltage follower is utilized to realize floating voltage source. Based on the new circuit structure, the multiplier can solve the power efficiency problem without the trade off of other performance like bandwidth and voltage headroom [36,37]. Although the use of cross-coupling MOS transistor pair can achieve a four-quadrant multiplier with different application, the floating voltage is still an additional circuitry to the multiplier which is not preferred

for wideband high frequency application and the noise of such a circuit is also a concern.

C. Square multiplier with voltage adder

The basic theory of this multiplier shown in Fig. 2-8 is based on the cancellation of non-linearity items caused by square of sum or subtraction of two voltages.

$$K\{[(X+x)+(Y+y)]^2+[(X-x)+(Y-y)]^2\}-K\{[(X-x)+(Y+y)]^2+[(X+x)+(Y-y)]^2\}=8Kxy \quad (1.8)$$

$$K\{[(X+x)-(Y+y)]^2+[(X-x)-(Y-y)]^2\}-K\{[(X-x)-(Y+y)]^2+[(X+x)-(Y-y)]^2\}=-8Kxy \quad (1.9)$$

Therefore the implementation of this kind of multiplier is to design an applicable voltage adder or subtraction subcircuits. A novel new structure was proposed recently with low voltage adder and subtraction circuit. The elementary structure is two transistors connected in series with the same aspect ratio. If both two transistors are biased properly in saturation region and neglect the high order effect of MOS transistor, the gate-source voltage drop across two transistors is the same. Based on this principle, a complete multiplier which is composed of the voltage adder is shown in Fig. 2-8. The function of the transistors M1-M12 is to form the four subcircuits which add two of the four input signals V1-V4 together. M3-M4 and M9-M10 are re-used to supply two circuits each. M13-M16 function as transconductor to convert voltage signals into current ones. M17-M18 are current mirrors to implement the addition and subtraction of the four currents. Here V1 and V3 are X±x, while V2 and V4 are Y±y respectively. According to [38], the output current I_o=8Kxy. This

multiplier requires only two transistors between power supply and ground, therefore it is very suitable for low voltage operation. However the ideal square law characteristic of MOS transistor in saturation without considering the effect of drain-source voltage is only applicable to the transistor with larger aspect ratio, which limits such a structure to be used in high frequency circuit design which needs small size transistors to reduce the parasitic effect. Another drawback comes from the complex implementation of the multiplication, which requires four square items to achieve two signals' multiplication instead of two. Therefore, simple cancellation scheme is needed for low power multiplier.

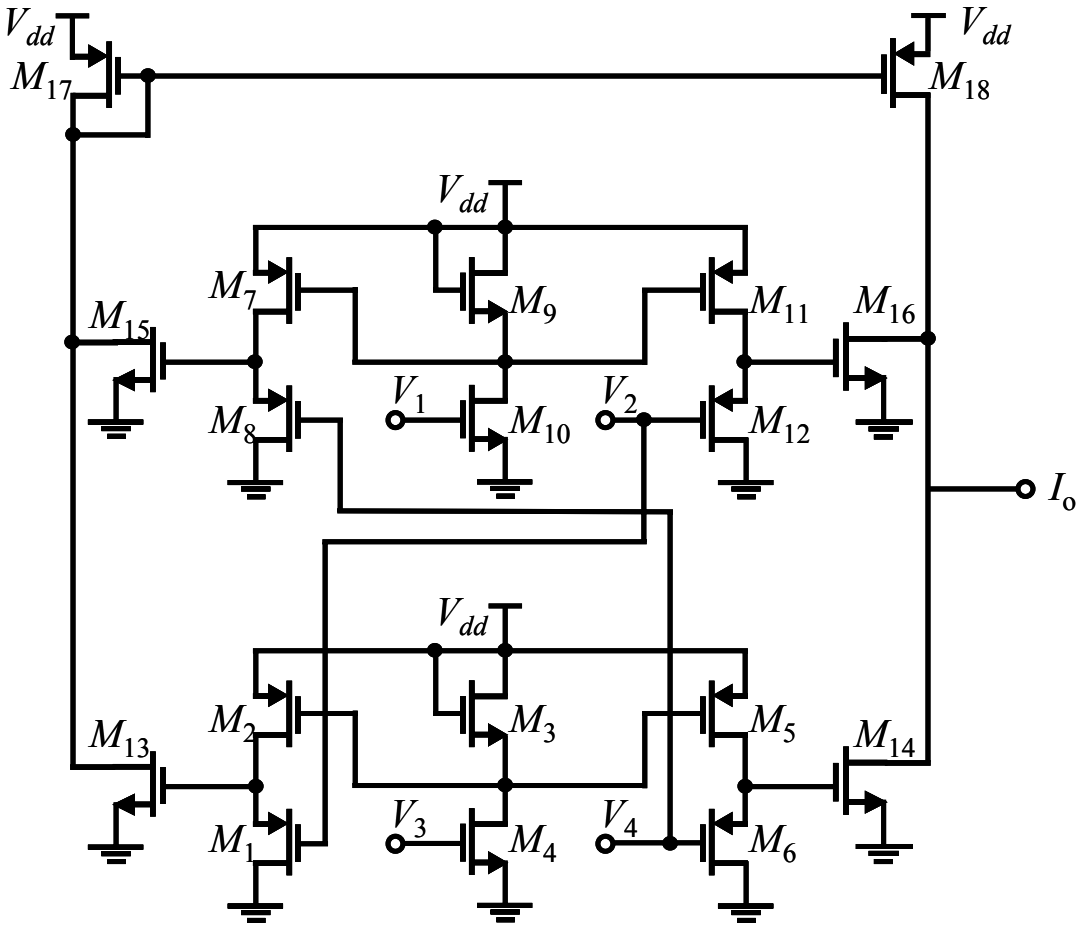


Fig. 2-8 A complete multiplier with voltage adder and subtractor [38].

D. Floating-gate MOS transistor structure

Floating-gate MOS transistor structure found many applications in the implementation of analog multiplier recently. There are two types of floating-gate MOS (FGMOS) structures: voltage and current mode. Voltage mode is first used to the build a four-quadrant multiplier [39,40] on the same cancellation principle in (1.8). Because the output voltage of a FGMOS is also proportional to the square of the weighted sum of the input signals [41], a simple cancellation scheme with a voltage mode FGMOS transistor is proposed in [42].

$$x^2 + y^2 - (x-y)^2 = 2xy \tag{1.10}$$

x^2,y^2 and $(x-y)^2$ are implemented by three FGMOS squarer with the input voltage of 0 and V_x, 0 and V_y, V_x and V_y respectively.

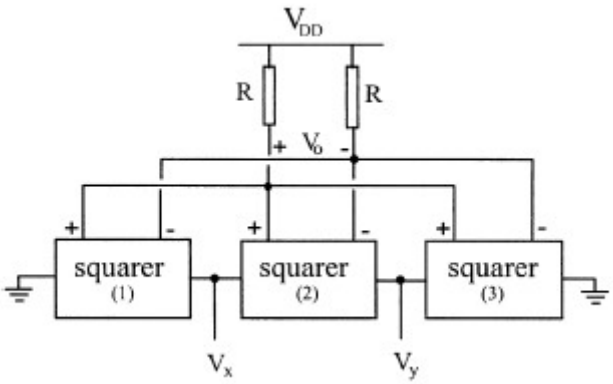


Fig. 2-9 Four quadrant multiplier with FGMOS squarer [42].

Since this circuit is a single-end input to realize a four-quadrant multiplication, additional common mode feedback circuit is needed at the output stage. In addition, in high frequency front-end circuit, differential signal is preferred for balance and non-linearity cancellation. A current mode FGMOS transistor is also introduced in

[42] to have more accuracy on output current because it is independent of body effect.

E. Multiplier with transistors in weak inversion

The basic principle of the multiplier operating in weak inversion is to use a source follower to inject an input signal into the drain of a transistor that is operating in triode region. Thus the current output is proportional to the multiplication of the two input signals due to the MOS characteristic in triode region. With the non-linear cancellation method in the equation (1.1), the four quadrant multiplication function can be realized.

Since such a circuit has a superior performance in linearity, noise and low voltage supply [18] and potential for high frequency implementation [43], it is used later in our design with some modifications to improve the bandwidth.

2.2 Integrator

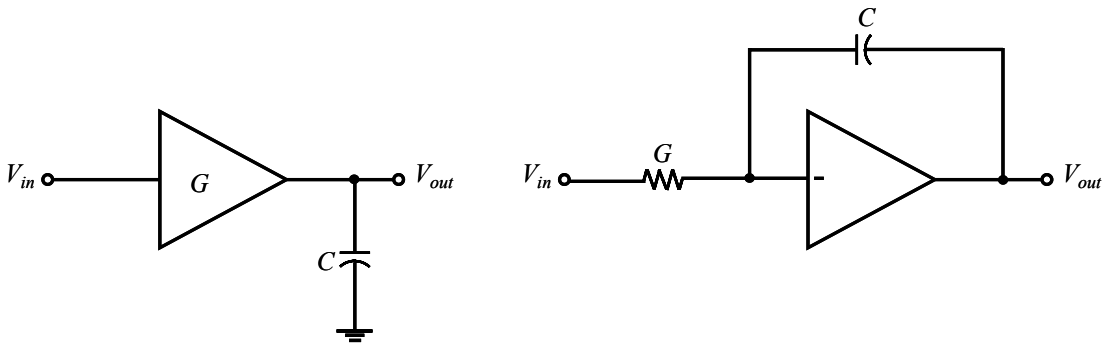


Fig. 2-10 (a) Transconductor based and (b) Op-amp based integrators.

There are basically two types of integrators, namely, the transconductor and op-amp based integrators, as shown in Fig. 2-10. The former converts the voltage signal into current and charge or discharges a capacitance load at the output. Where as the latter has a capacitor connected between the input and output of an op-amp, and charged and discharged through resistor. In general, the transconductor based integratore has much wider bandwidth than the op-amp based ones.

2.2.1 Op-amp based integrators

The structure is commonly used for low frequency applications. The integrator is usually composed of a resistor and an op-amp in Fig. 2-10(b). The potential at the two input ports are assumed to be equal because of the high gain of the op-amp. Since one port is connected to ground, the current through the resistor is Gv_i. Due to the large input impedance of the op-amp, the current which goes through the resistor is forced to be injected into the integration capacitor. Thus the transfer function of the integrator can be expressed as $\frac{v_o(s)}{v_i(s)} = \frac{G}{sC}$

As the integration capacitor can be considered as a Miller capacitor, the integrator is also referred to as a Miller integrator. Different designs for Miller integrators have been reported [44-47]. Among them, the current feedback amplifier (CFA) is said to be a wideband alternative to the voltage-mode op-amps (VOA) because of its near constant close loop bandwidth and high slew rate [48]. However, due to the stability problems in the negative feedback path, only very limited success is achieved [49].

The resistor is often replaced by a transistor in linear region in practical implementations. The current through the capacitor is derived according to the simple MOSFET model in linear region.

$$I_d = 2K[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \tag{1.11}$$

Since the non-linearity of the resistor comes from a second order term of V_{DS}, a differential scheme is adopted to cancel the redundant item in the current to linearize the resistor [50], as shown in Fig. 2-11 .

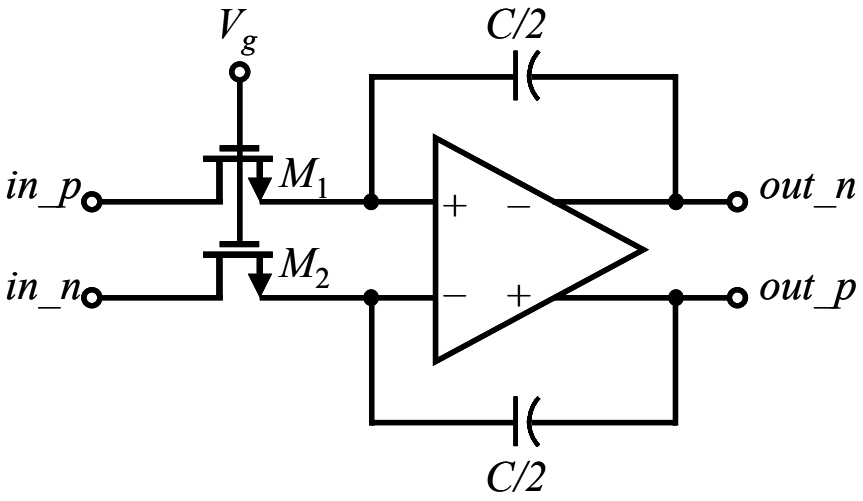


Fig. 2-11 Op-amp integrator with a MOS transistor as resistor [51].

Fig. 2-12 shows a transconductor based integrator. The transconductor is implemented with a simple differential pair. Transistor M1 functions as a source degeneration resistor. The use of source degeneration allows low-voltage operation, because the DC current through the transistor M2, M3 is provided by the current source below, there is no extra voltage drop at the source degeneration resistor.

$$g_{d1} = K_1(V_g - V_{M1} - V_Q)$$

Transistor M1 functions as a source degeneration resistor. One advantage of the use of source degeneration is for low-voltage design. Because the DC current through the transistor M2, M3 is provided by the current source below, there is no extra voltage drop at the source degeneration resistor.

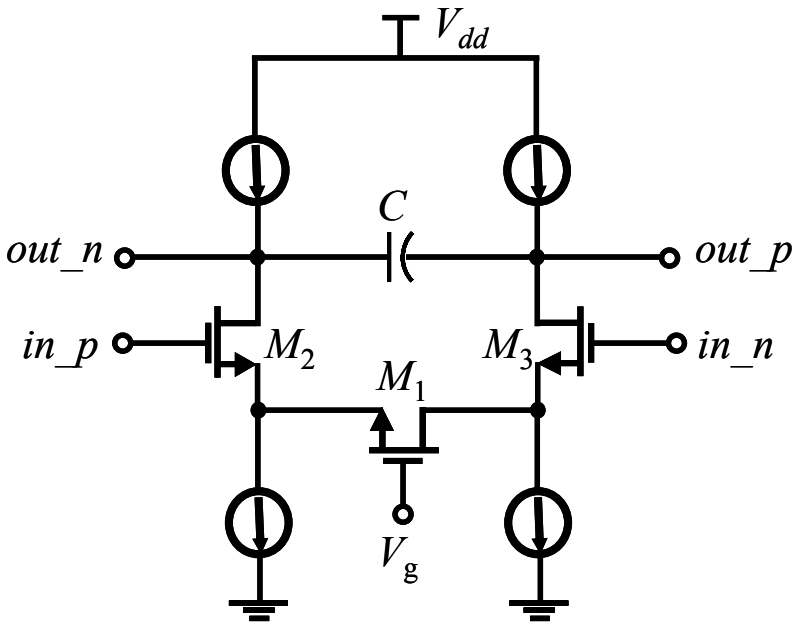


Fig. 2-12 Transconductor based integrator with source degeneration [51].

Assuming that the output impedance of the current source below is large enough, the transconductance Gm of such a differential pair with source degeneration is given by [52]

$$G_m = i / v_i = \frac{1}{2/g_{md} + 1/g_{d1}}$$

Due to the imperfection of the transconductance [53], several methods are proposed to raise the output resistance of the transconductor. In [54], a cascade gain boost current buffer is added to the output of the transconductor. In order to get high voltage swing

and common-mode flexibility, a folded cascade structure is reported as a better one than the telescope one [55].

However, such a topology is not suitable for a high frequency integrator design, because two pairs of ideal current sources are difficult to implement with small sized transistors under low supply voltage, while larger transistors with high parasitic capacitance will still decrease the high frequency performance of the integrator.

2.2.2 Active-triode op-amp based integrator

A practical circuit of the active-triode integrator [56] is described in Fig. 2-13. M3, M4 are current sources which provide DC bias for a pair of common-source transistor M1,M2. The current Io is set to a small value to ensure that M1, M2 operate in linear region with a reasonable large dynamic range. Since the input impedance of the op-amp is large enough to force the current changed in M1, M2 directly flow through the feedback capacitors, the output current is given by

$$\Delta I = I_1 - I_2 = 2KV_X v_{id} \tag{1.12}$$

V_X is the drain voltage of the two transistors and v_{id} is the differential input voltage.

Therefore, if the input voltage can maintain the two transistors M1, M2 operating in linear region, the transconductance of the current converter is $G_m = \Delta I / v_{id} = 2KV_X$. Then the output differential voltage of the op-amp based integrator is given by

$$v_o = v_{o\_}p - v_{o\_}n = \frac{1}{C_f}\int \Delta I dt = \frac{2KV_X}{C_f}\int v_{id} dt \tag{1.13}$$

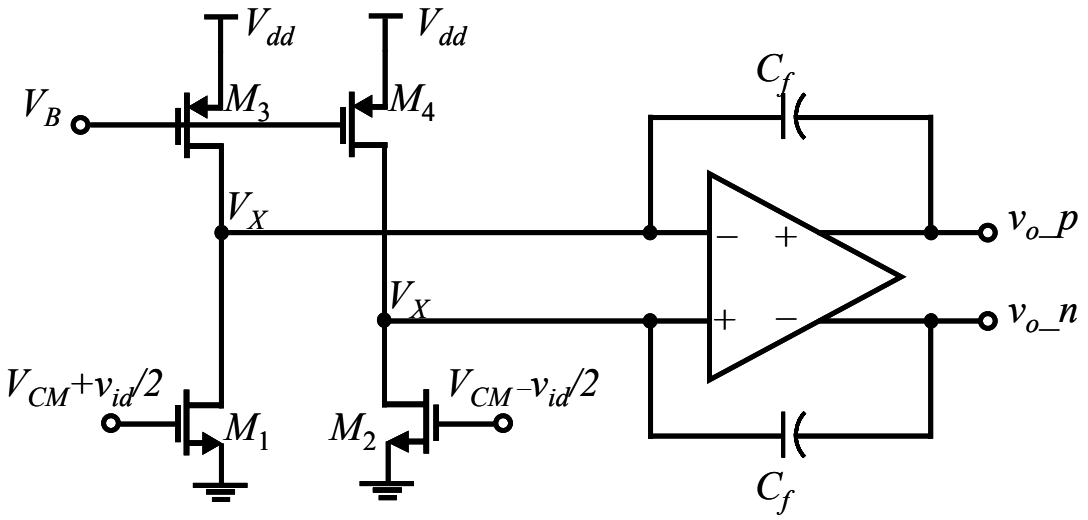


Fig. 2-13 Active triode integrator structure [56].

The complexity of op-amp limits such a circuit to be used to implement high speed integrators because the cut-off frequency of an op-amp is hardly achieved above GHz.

Since the high-frequency poles of the op-amp cause excess phase causing error in the integrator, most of the high frequency integrator is implemented with transconductor whose non-dominant poles are normally located at very high frequency [57].

2.2.3 Transconductor based integrator

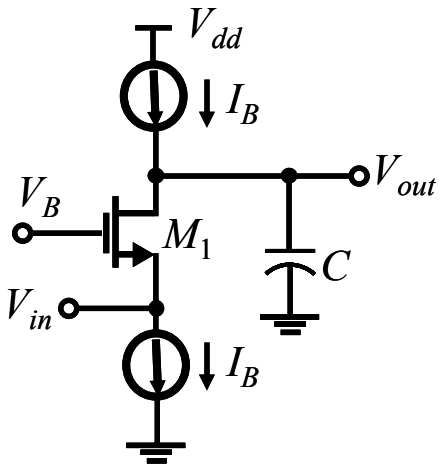


Fig. 2-14 Transconductor based integrator [51].

Fig. 2-14 is an unbalanced transconductor based integrator. Being different from the conventional structure, the input signal is fed to the source of the transistor, insteas of its gate. M1 operates in saturation region and I_B is a DC bias current provided by two current source with the same value. Since M1 is operating in saturation, its transconductance is $\sqrt{2KI_d}$. Since the current source is assumed to have very high output impedance, the drain current variation directly reflects the current through the output integration capacitor [58]. The disadvantage of this integrator is that it requires two current sources at the source and drain of the transistor to be exactly matched. This is difficult to realize in practice.

2.2.4 Transconductor-C integrator

The G_m-C integrator has the advantage of high bandwidth that is directly proportional to the overdrive voltage (V_{GS}-V_T) when transistors are biased in saturation region [59]. However, the finite output resistance of the linear transconductor limits the integrator's performance and causes it deviate from the ideal one that has exact 90^o phase shift. Thus, the use of additional circuit to enhance the output resistance is mandatory. Some previous reported output resistance enhancement techniques are shown in Fig. 2-15.

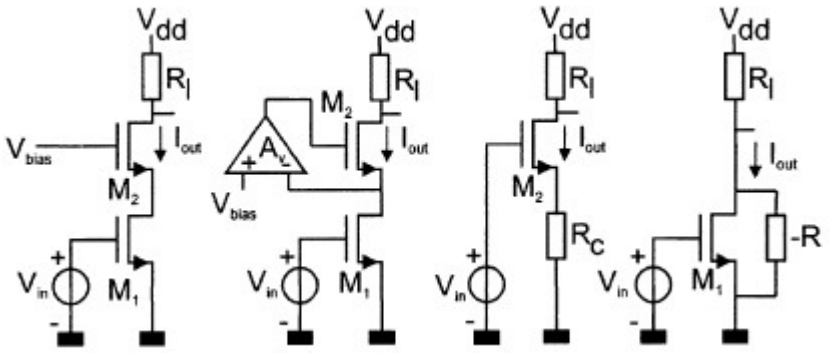


Fig. 2-15 Ways to increase output resistance
(a) Simple cascade (b) active cascade (c) source degeneration (d) negative resistance [60].

Cascode structure has been used to enhance the DC gain of the op-amps and hence the gain of the integrator, for it has high output resistance [61-65]. However, such cascode structures will introduce additional internal nodes which may cause a low non-dominant pole that in turn degrade the performance of the integrator.

Another way to improve the output impedance is to cancel the finite output resistance of the transconductor with a negative resistor load [59]. Ideally the DC gain can be increased to infinity without mismatch and second order effect [66]. An integrator is based on Nauta's inverter transconductor shown in Fig. 2-16 [67], where the inverter is operating in the saturation region. This transconductor has proved to have a good linearity and wide bandwidth, and is suitable for high frequency application.

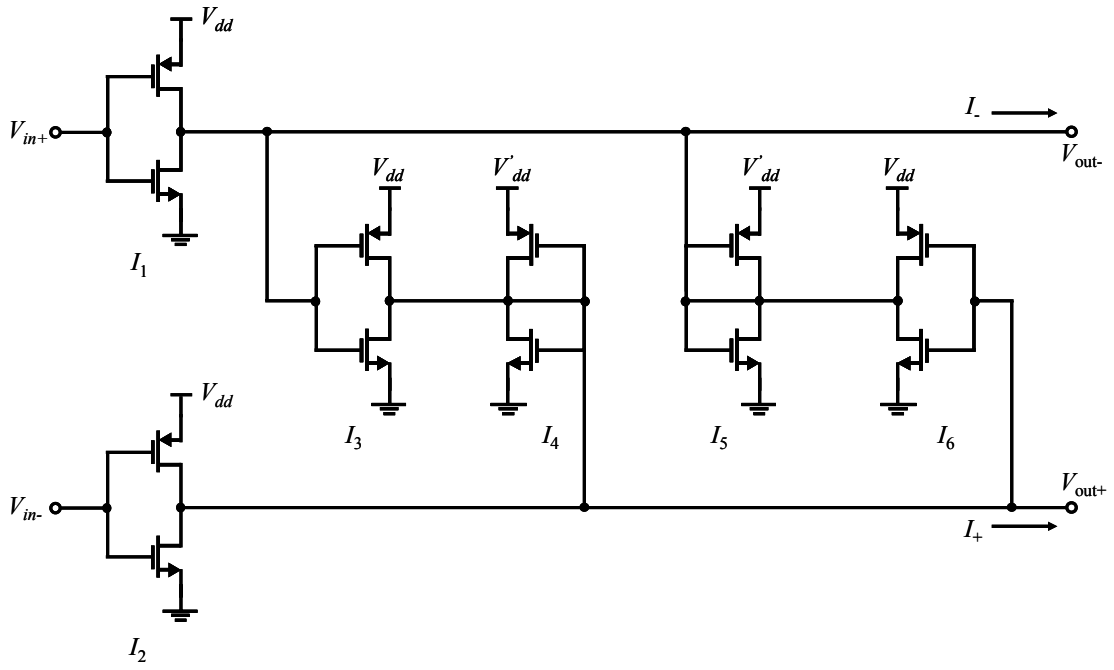


Fig. 2-16 Nauta's transconductor integrator with DC gain enhancement [68].

This transconductor structure later was used to enhance the performance of the integrator such as tunability for filter design [68-70]. With common-mode feedback and DC gain enhancement, this architecture can tune the output resistance and capacitance separately, which makes it possible to achieve high speed and long sample holding time. It is therefore a preferred transconductor for the implementation of the integrator in our correlator.

2.3 Bandwidth Enhancement Techniques

There are different ways to enhance the bandwidth of an amplifier or other circuits. In this section, the shunt-peaking and multi-pole bandwidth enhancement techniques will be briefly reviewed.

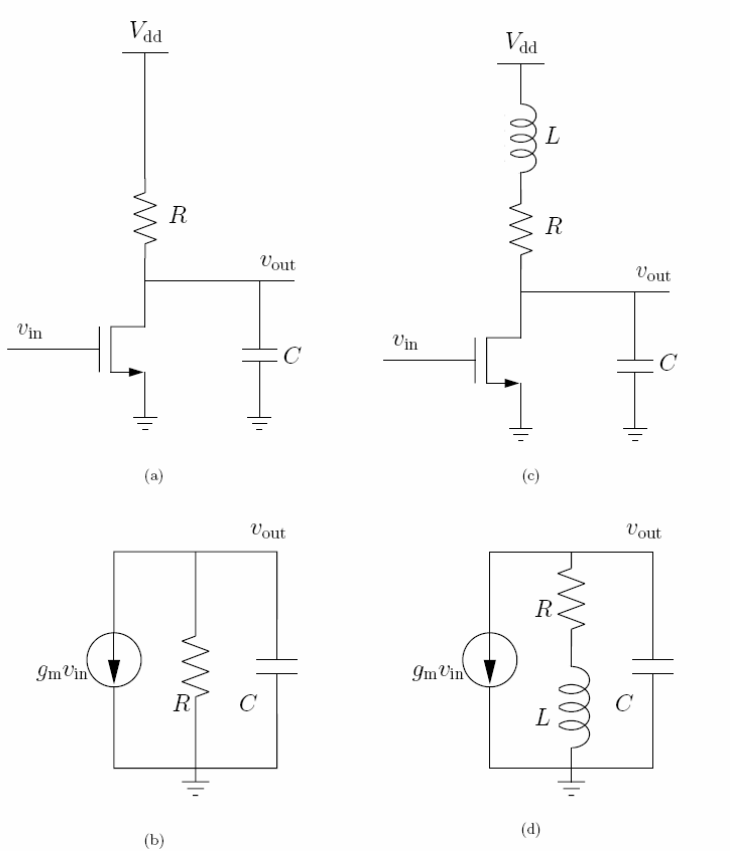


Fig. 2-17 (a) Schematic and simple small signal circuit without shunt-peaking (b) Schematic and simple small signal circuit with shunt-peaking [71].

2.3.1 Shunt-peaking technique

Shunt-peaking technique is not a new technique for bandwidth enhancement. It was originally used to extend the bandwidth of television tubes in the 1940's [71]. However, with developments in technology, large value inductors can be integrated on-chip, which stimulates the emergence and development of radio frequency integrated circuit (RFIC) design. Here a common source amplifier is used as an example to illustrate the shunt-peaking technique. As shown in Fig. 2-17, to enhance the bandwidth of this amplifier, an inductor is added in series with the output resistor load. Without the output inductor, only the output capacitor and resistor load determines the bandwidth of the amplifier.

$$\frac{v_{out}}{v_{in}}(w) = \frac{g_m R}{1 + jwRC} \tag{1.14}$$

With the introduction of the shunt-peaking inductor L, the frequency response becomes

$$\frac{v_{out}}{v_{in}}(w) = \frac{g_m (R + jwL)}{1 + jwRC - w^2 LC} \tag{1.15}$$

where there are two poles and one zero. The zero is set by the L/R time constant, which cancels on of the poles and increases the bandwidth. The detailed analysis has been done in [71], where a new parameter m was introduced, which is defined as the ratio of L and R^2C. The frequency responses for different m are listed in Table 2-1.

Factor (m)	Normalized w_{3dB}	Response
0	1.00	No shunt peaking
0.32	1.60	Optimum group delay
0.41	1.72	Maximally flat
0.71	1.85	Maximum bandwidth

Table 2-1 Bandwidth comparison for shunt peaking [71].

As shown in Fig. 2-18, the -3dB bandwidth increase with m. The maximum bandwidth situation happens when m=0.71 with a bandwidth extension to a factor of 1.85. However the magnitude response shows that there is a significant peaking in the gain which is intolerant in wideband application. To get an approximately maximum flat magnitude response, m reduces to 0.41 and also improves the bandwidth to 72%. Another interesting thing exists in the phase response instead of the magnitude response. When m=0.32, there is a best approximation to a linear plot in phase response below 3-dB point with 60% bandwidth improvement. In this case, which is

called optimum group delay is required to minimize the distortion of the wideband pulse in broadband systems.

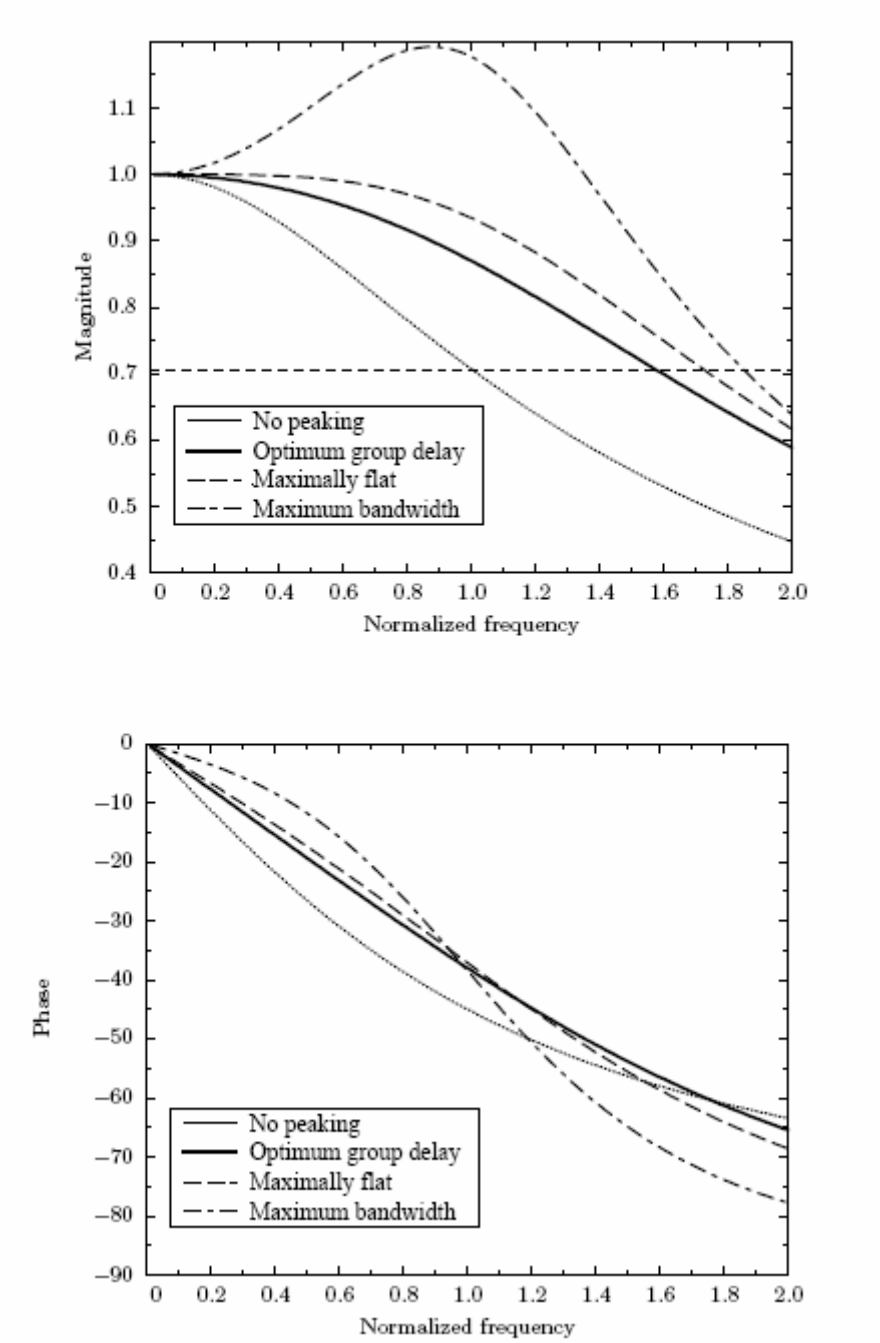


Fig. 2-18 Frequency response comparison of the shunt peaking amplifier [71].

2.3.2 Multi-pole bandwidth enhancement

The bandwidth extension technique originates from the design of broadband matching network for amplifiers [72]. Since the procedure of such a matching network needs the two-port parameter and is only limited to two port amplifier of a single stage, In [73], passive structures are used as an alternative method to overcome Bode-Fano's gain bandwidth limit.

$$(GBW)_{\max} = \frac{g_m}{\pi C} = g_m \cdot Z(j\omega) \tag{1.16}$$

Here, g_m is the device transconductance and C is defined as $C = \lim_{\omega \to \infty}(\frac{1}{j\omega Z})$

Since the practical amplifier is more than one stage, the introduction of passive network between each stage is possible. In Bode-Fano's bandwidth limitation theory, if $Z(jw)$ is not a function of impedance, in which the order of the numerator is not greater than the order of the denominator, the limit does not take effect. Because the passive network between two gain stages will change $Z(jw)$ to a frequency dependent transfer function with the numerator polynomial one degree higher than the denominator one, the amplifier with such a structure is able to overcome the Bode-Fano limit and achieve wider bandwidth. In his system design, a cascade structure of gain amplifiers and filters with different frequency response is presented. By tuning the frequency response of the next stage, an amplitude falling edge in the previous stage can be flattened by the peaking due to higher frequency pole in the next stage.

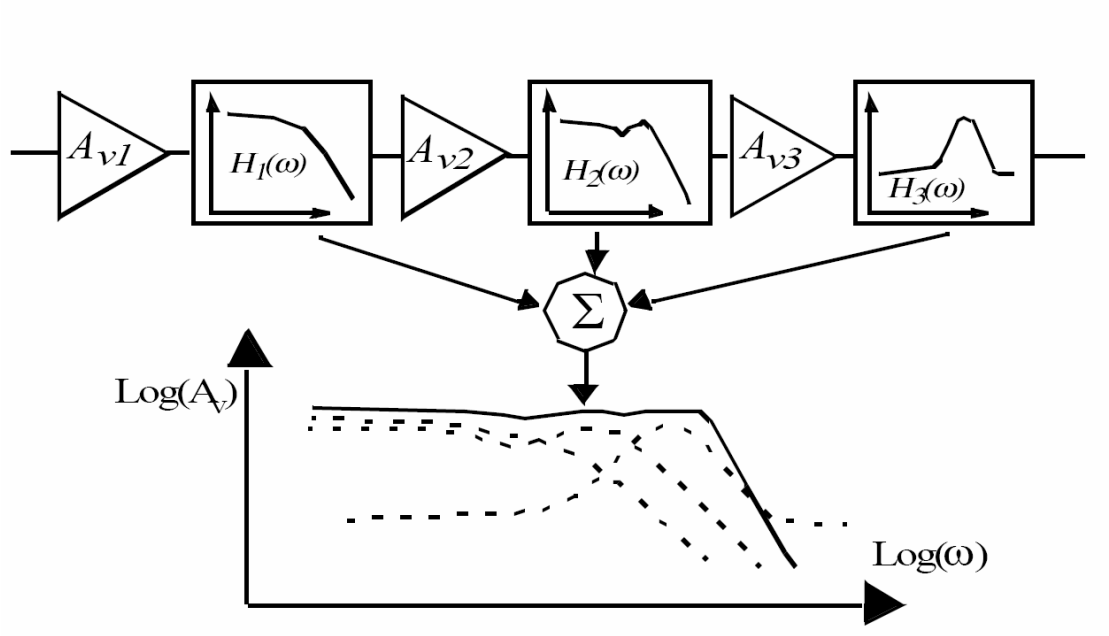


Fig. 2-19 Illustration of multistage bandwidth extension [72].

The Fig. 2-19 explains the methodology of this bandwidth enhancement technique. The wideband amplifier is composed of three single stage transistors with the same structure. Assuming all the three stages have the same transfer function $A_{vi}(j\omega) = g_{mi} \cdot Z_i(j\omega) \quad (i = 1,2,3)$, thus the whole frequency response of the amplifier can be expressed as

$$A_v(j\omega) = G_m \cdot Z(j\omega) \tag{1.17}$$

Here, $G_m = g_{m1} \cdot g_{m2} \cdot g_{m3}$, $Z(j\omega) = Z_1(j\omega) \cdot Z_2(j\omega) \cdot Z_3(j\omega)$

$Z(jw)$ is a frequency dependent function and can be shaped by additional passive network. Therefore the order of the numerator is not always lower than that of the denominator and can be made higher by tuning the parameters in the passive network. That is how the wideband is achieved using multiple-pole technique. Using 0.18um MOS transistor in a BiCMOS process technology, a 9.2GHz bandwidth is obtained with 54dBΩ transimpedance gain.

CHAPTER 3 CORRELATOR DESIGN

Time Integrating Correlator

In a UWB receiver part, the received pulse signal from the antenna is very weak with background noise. In addition, the wide bandwidth of the pulse adds difficulty to the detector to filter out the noise and pick up the information coded signals, because the noise energy in the signal band is still comparable to the power of the pulse signal. Unlike traditional detector solution in frequency domain, a cross correlator is often used as an efficient way to filter out the noise in the signal band in spread spectrum transceiver. Refering to the correlation functions, the correlator can be implemented with a multiplier followed by an integrator. The correlation process in a UWB transceiver is shown in Fig. 3-1. The two inputs of the correlator are the received signal from antenna and a template pulse generated by local pulse generator in the transceiver. Here it is assumed that the template is synchronized with the received signal from the antenna and the transceiver uses BPSK modulation scheme. After the correlation, the transmitted data of "1" and "0" is detected.

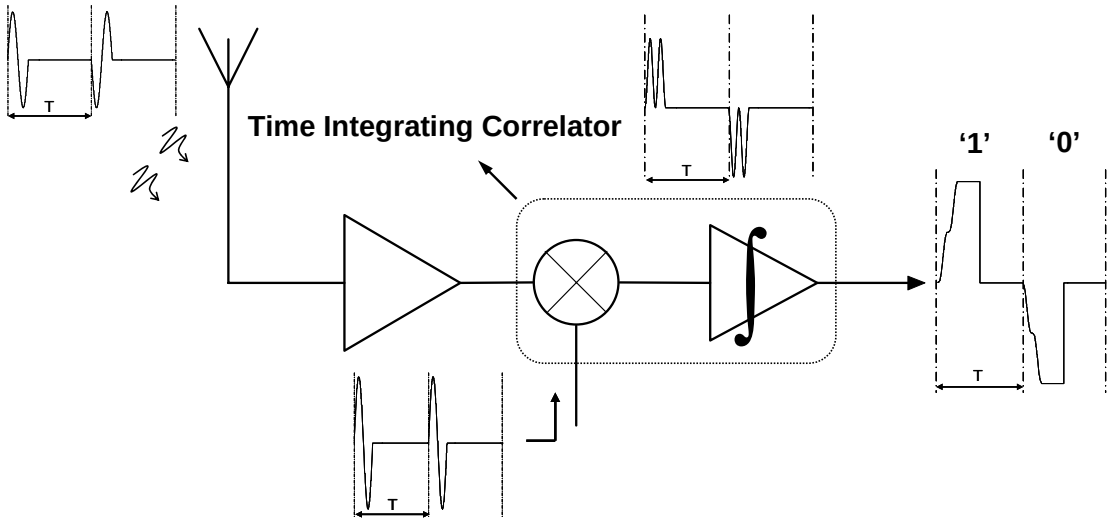


Fig. 3-1 the cross correlation process in a time integrating correlator [74].

3.1 Wideband Multiplier Design

3.1.1 DC analysis

Fig. 3-2 shows the proposed multiplier for the correlator. It is based on the transconductor multiplier structure in [18]. The lower eight transistors forms the core of the four quadrant multiplier, which is a CMOS programmable transconductors and converts input voltage signals (rf and lo) into current to realize the multiplication.

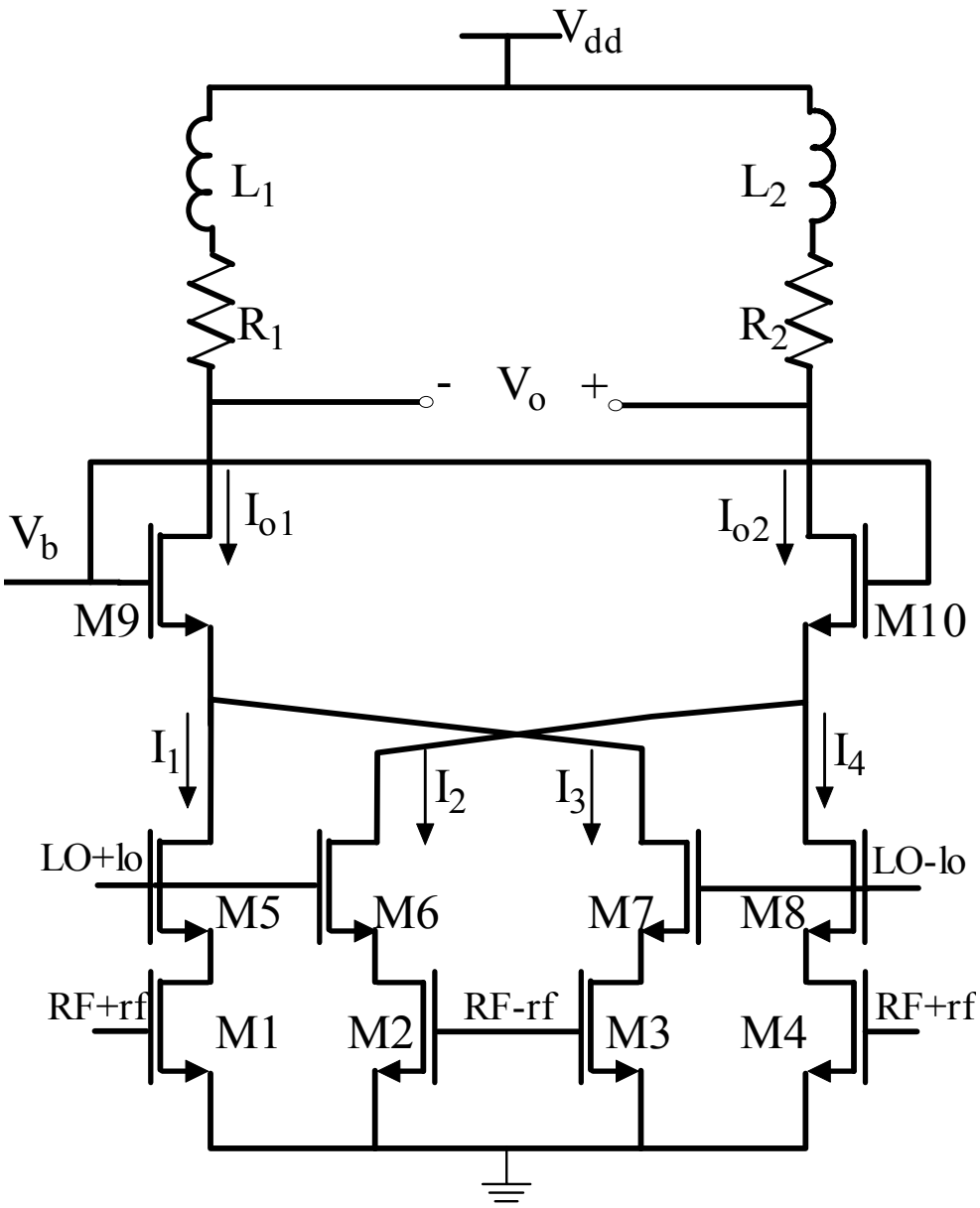


Fig. 3-2 Schematic diagram of the four quadrant multiplier.

To enhance the linearity of the multiplier, the bottom four transistors, M1 – M4, are working in triode region with differential structure to suppress the common-mode signal. M5-M8 operate in saturation region as a source follower by proper voltage bias. A pair of NMOS transistors (M9 and M10) is inserted between the outputs of the transconductor M5 – M8 and the output of the multiplier, to avoid the leakage of the input signal to the output.

The lower eight transistors contain the core of the wideband multiplier. Since there is a comparatively high parasitic capacitance from the output buffer at the output nodes of the multiplier core in order to reduce speed degradation caused by this capacitance, a common-gate stage with its low input impedance is inserted between the multiplier core and the load resistor. This cascade configuration increases the output bandwidth substantially. Two inductors are added at the output in series with load resistors to further enhance the bandwidth.

According to the large signal MOS transistor model in the triode region, the current flowing through each of the lower branches, I_1 to I_4, can be expressed as

$$I_i = K(RF + rf - V_{tn} - \frac{V_{dsi}}{2})V_{dsi} \tag{1.18}$$

where $K = \mu_n C_{ox} \frac{W}{L}$. Since the transconductance of the transistor in the saturation region is larger than that of the transistor in the triode region, the upper transistors operating in the saturation region act as source followers. Thus, the source-drain voltage of the lower transistors, M1- M2 and M3 – M4, can be expressed as

$$V_{dsi} = V_{ds} + lo \tag{1.19}$$

and

$$V_{dsj} = V_{ds} - lo \tag{1.20}$$

respectively, where V_{ds} is the drain-source voltage at bias point when $x = y = 0$. According to (1.18) – (1.20), the total output current can be obtained as follows,

$$\begin{aligned} I_0 &= (I_1 - I_2) + (I_3 - I_4) \\ &= 2K(rf)V_{ds1} - 2K(rf)V_{ds2} \\ &= 4K(rf \times lo) \end{aligned} \tag{1.21}$$

where assuming that all transistors are matched (K is same for all transistors). Thus the output voltage of the multiplier is

$$V_o = -I_o Z_o = -4K(rf \times lo)Z_o \tag{1.22}$$

and the multiplication function is realized.

3.1.2 Frequency domain analysis

Since multiplier is often used in analog signal processing, the linearity is a major consideration of the multiplier design. However in UWB application, because the duration of the pulse signal is only 1ns or less, the multiplier must be able to respond to the high speed low duty cycle pulse quickly. Therefore, the bandwidth becomes a major problem to design the wideband multiplier. Some bandwidth enhancement technique has to be adopted in the design.

For the bandwidth of the multiplier, we follows the definition given in [75]. Because the two input signals of the multiplier is symmetric, but different in amplitude, to analyze the frequency response we treat the multiplier as a wideband amplifier by feeding the signal in one port and biasing the other port at a constant differential value. Then the magnitude frequency response is defined as the absolute value of S21 parameter versus the frequency of the input signal.

A. Bandwidth enhancement technique

Shunt peaking technique has been widely used in wideband amplifier design, where an inductor is introduced to form a resonant circuit. The use of shunt peaking circuit

to extend the bandwidth was proposed in [71]. A typical shunt-peaked amplifier is shown in Fig. 3-3, where assumed that the uncompensated bandwidth is determined by the load resistance and capacitance if the inductor is not included. The detailed analysis was done in [71] where it showed that the maximum bandwidth expansion is 1.85 time of the uncompensated one.

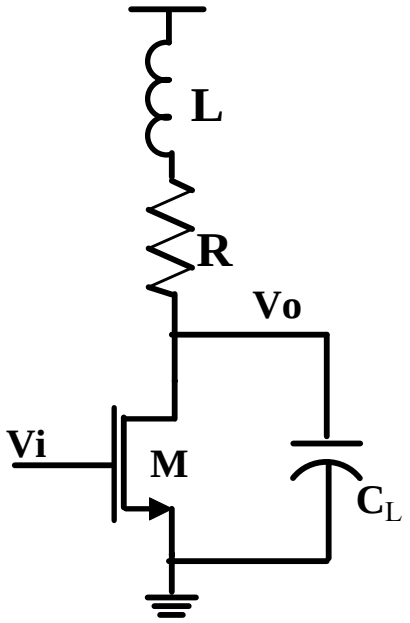


Fig. 3-3 Shunt-peaked amplifier [71].

However, in some circuits, the dominant pole may be caused by the parasitic capacitor at the internal stage instead of at the output node. Under such a circumstance, the original shunt peaking concept cannot effectively increase the bandwidth. In this thesis, we propose a modified approach to increase the bandwidth using the shunt peaking technique. To illustrate it, a cascode amplifier shown in Fig. 3-4 is used as an example. Due to the low voltage operation (<1.8V), the load resistor cannot be large. On the other hand, the large dimension of common-gate transistor M2 is normally required in order to reduce its overdrive voltage and hence a low voltage drops across

its drain and source. As a result, the dominant pole is shifted from the output node to the internal one, that is, the source of common-gate transistor.

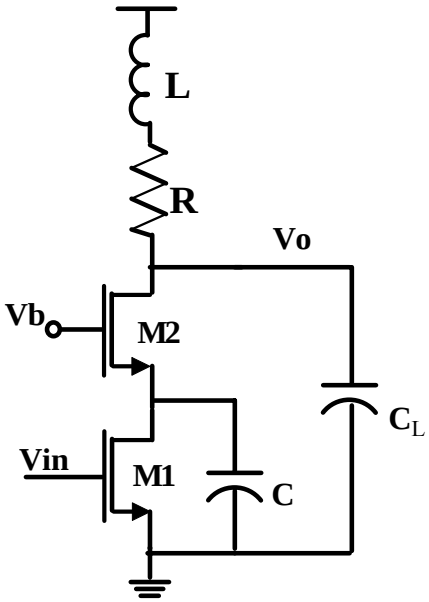


Fig. 3-4 Shunt-peaking of a cascade amplifier.

To illustrate the principle of bandwidth enhancement, the analysis is done using a simplified small-signal equivalent circuit given in Fig. 3-5, where the output resistance of the transistor r_{ds} is ignored initially. Thus, the transfer function can be written as

$$\frac{v_0(s)}{i(s)} = \frac{R_L\left(1+s\frac{L}{R_L}\right)}{(s\frac{C}{g_m}+1)(s^2C_LL+sC_LR_L+1)} \tag{1.23}$$

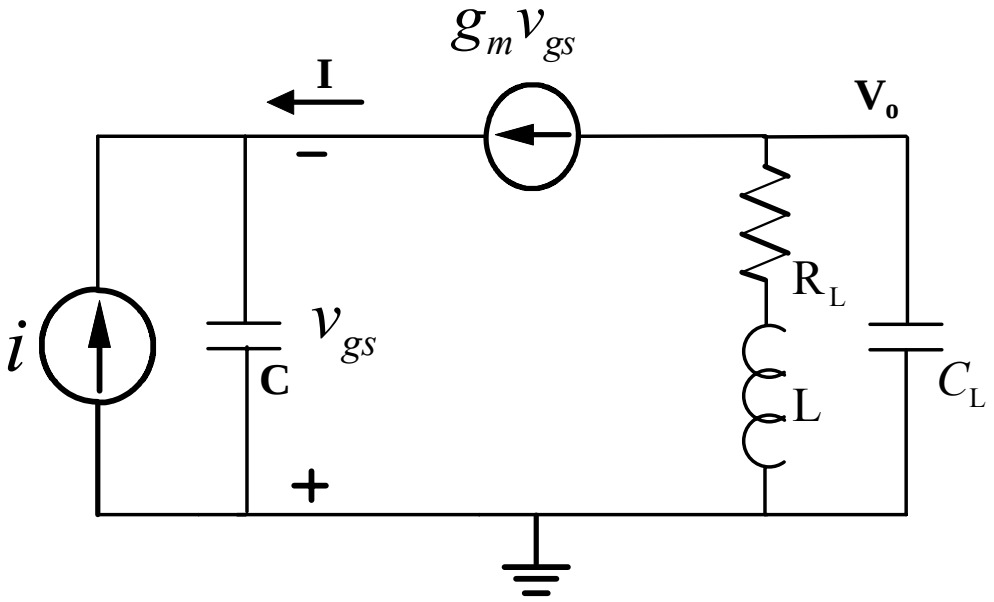


Fig. 3-5 Small signal model of the cascade amplifier.

The pole at the internal node is determined by g_m/C and the other two poles, likely to be the complex poles, are from the shunt peaking circuit at the output. In addition, the inductor L introduces a zero in the transfer function. On the assumption of the dominant pole at $\omega_{p1} = \frac{g_m}{C}$, the zero can be made equal to the dominant pole, that is, $\omega_z = \omega_{p1} = R_L/L$ by choosing a proper inductance value, and thus the dominant pole can be effectively cancelled. The resultant transfer function becomes a low pass and second-order one with -3dB frequency around $\omega_0 = (LC_L)^{-1/2}$. Since ω_0 is much higher than ω_{p1}, the bandwidth of the amplifier can be greatly extended. To further analyze it, the following extracted circuit and device parameters in Table 3-1 are used to get the magnitude response in Matlab. Change the value of L from 0 to 30nH, which simulates the circuit without inductor and with inductor, the output magnitude response in Fig. 3-6 shows that the effect of shunt-peaking inductor on the bandwidth is quite obvious.

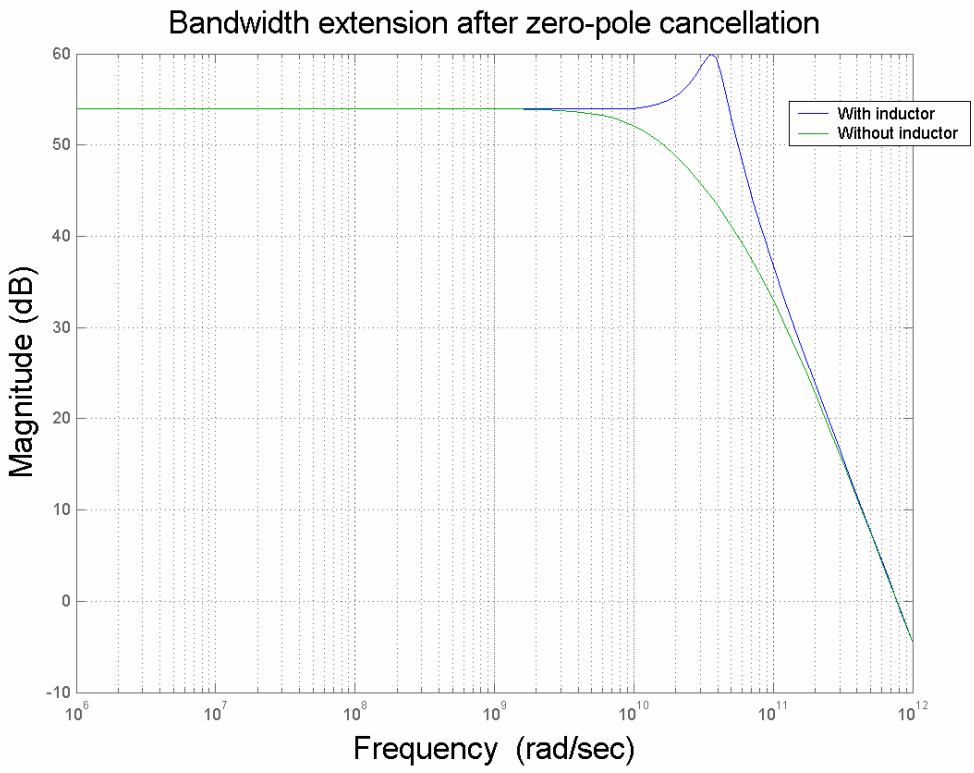


Fig. 3-6 Comparison of the magnitude response with and without inductor.

Parameter	R	L	C	r_{ds}	g_m
Value	500 Ω	30 nH	160 fF	3850 Ω	2.2*10-3 A/V

Table 3-1 Parameter extracted from the component used in simulation.

B. AC analysis of the wideband multiplier

For the AC analysis, we make the following assumptions. First, for a fixed rf, the resistance associated with each drain node of M1-M4 is very low as they operate in triode region. Thus, parasitic capacitance at those nodes has little contribution to the bandwidth of the multiplier. Secondly, M5-M8 can be viewed as a transconductor that has a current output. Under the above assumptions, the small-signal model of the

multiplier can be simplified to that in Fig. 3-7. The output resistance of the transconductor (M5- M8) can be omitted as it is much higher than that seen from the source of the common-gate transistor (M9 or M10). The capacitance of C is the lumped parasitic at the source node of M9 or M10.

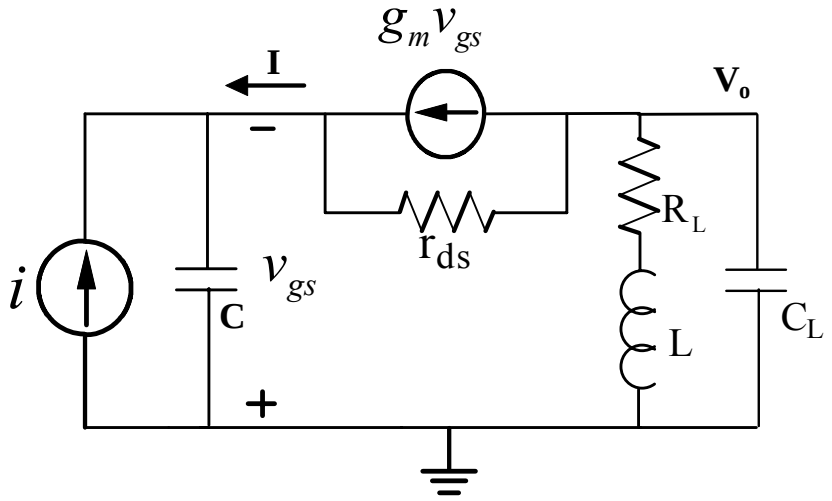


Fig. 3-7 Simplified small signal model of the wideband multiplier.

According to Fig. 3-7, the transfer function of the simplified multiplier is

$$\frac{v_o}{i} = \frac{sL + R_L}{as^3 + bs^2 + cs + 1} \tag{1.24}$$

$$a = \frac{CC_L L}{g_m + \frac{1}{r_{ds}}}, b = \frac{CC_L R_L + C_L L(g_m + \frac{1}{r_{ds}}) + \frac{CL}{r_{ds}}}{g_m + \frac{1}{r_{ds}}}, c = \frac{C + C_L R_L (g_m + \frac{1}{r_{ds}}) + \frac{CR_L}{r_{ds}}}{g_m + \frac{1}{r_{ds}}}$$

The third-order transfer function is expected since the inclusion of the inductor adds a zero and an additional pole at the output. In general, a third-order system can be at least divided into one second-order and a first-order system. If the dominant pole is assumed to be far away from other poles, the transfer function in Equation (1.24) can be written as

$$\frac{v_o}{i} = \frac{R_L(s\frac{L}{R_L}+1)}{(\frac{s}{p_1}+1)(\frac{s^2}{p_2 p_3}+s(\frac{1}{p_2}+\frac{1}{p_3})+1)} = \frac{R_L(s\frac{L}{R_L}+1)}{(s\frac{C+C_L R_L(g_m+\frac{1}{r_{ds}})+\frac{C}{r_{ds}}R_L}{g_m+\frac{1}{r_{ds}}}+1)(s^2\frac{CC_L L}{C+C_L R_L(g_m+\frac{1}{r_{ds}})+\frac{CR_L}{r_{ds}}}+s\frac{CC_L R_L+C_L L(g_m+\frac{1}{r_{ds}})+\frac{CL}{r_{ds}}}{C+C_L R_L(g_m+\frac{1}{r_{ds}})+\frac{CR_L}{r_{ds}}}+1)} \quad (1.25)$$

where p_1 is the dominant pole, p_2 and p_3 are likely to be two complex conjugate poles. If the dominant pole is cancelled by the zero, the transfer function becomes second-order lowpass, whose bandwidth is determined by the complex poles. Using the parameter in Table 3-1, the resultant pole locations are drawn in Fig. 3-8. From the plot, p2 and p3 are indeed two complex conjugate poles, whose distance from the origin is much further than that of p1.

$$p_1 = 1.5195\times10^{10}, p_{2,}p_3 = 1.2242\times10^{10} \pm 2.9018\times10^{10} i$$

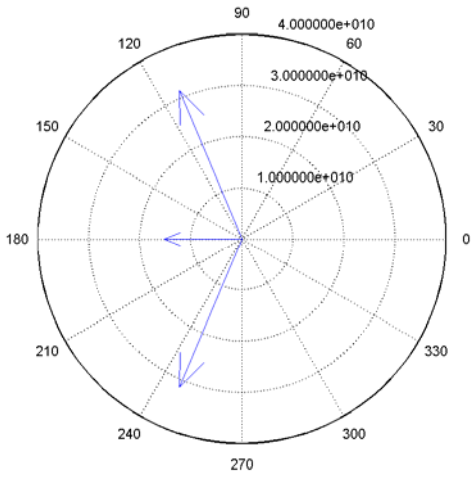


Fig. 3-8 Poles of the third order system in the polar axis.

The corresponding dominant pole frequency, ω_{p1} is around 2.42 GHz. Since p_1 is independent of L according to (1.25), it can be cancelled by the zero, $\omega_z = R_L / L$, for

a correctly chosen inductance of L. Given g_m, r_{ds} and C, the inductance is found to be $L = \frac{R_L}{p_1} = 33nH$.

With the dominant pole and zero cancelled with each other, the resultant transfer function is a typical second-order lowpass system whose bandwidth solely depends on its Q value (Quality factor). For maximum flat response, the bandwidth is nearly equal to $1.5\omega_0$, which can be calculated based on the given parameters, that is,

$$f_{-3dB} = \frac{1.5}{2\pi}\sqrt{\frac{C + C_L R_L (g_m + \frac{1}{r_{ds}}) + \frac{CR_L}{r_{ds}}}{CC_L L}} = 10.5GHz$$

Fig. 3-9 shows the magnitude responses obtained from the simulation when the inductor L is absent. A bandwidth of 2 GHz is observed and agrees well with the analysis. To further verify that the dominant pole indeed comes from the internal node and determines the bandwidth, a dummy parasitic capacitance (0.1 pf) is added to the source of M9 and M10, respectively. It can be clearly seen in Fig. 3-9, the bandwidth is reduced. This implies that the bandwidth of the multiplier is determined by the dominant pole originated from the internal node (source of M9 and M10). Simulation is also done for different inductance values. At the optimum value of 30 nH, the maximum bandwidth of 10 GHz is achieved, a 5-time improvement from the original 2 GHz shown in Fig. 3-10.

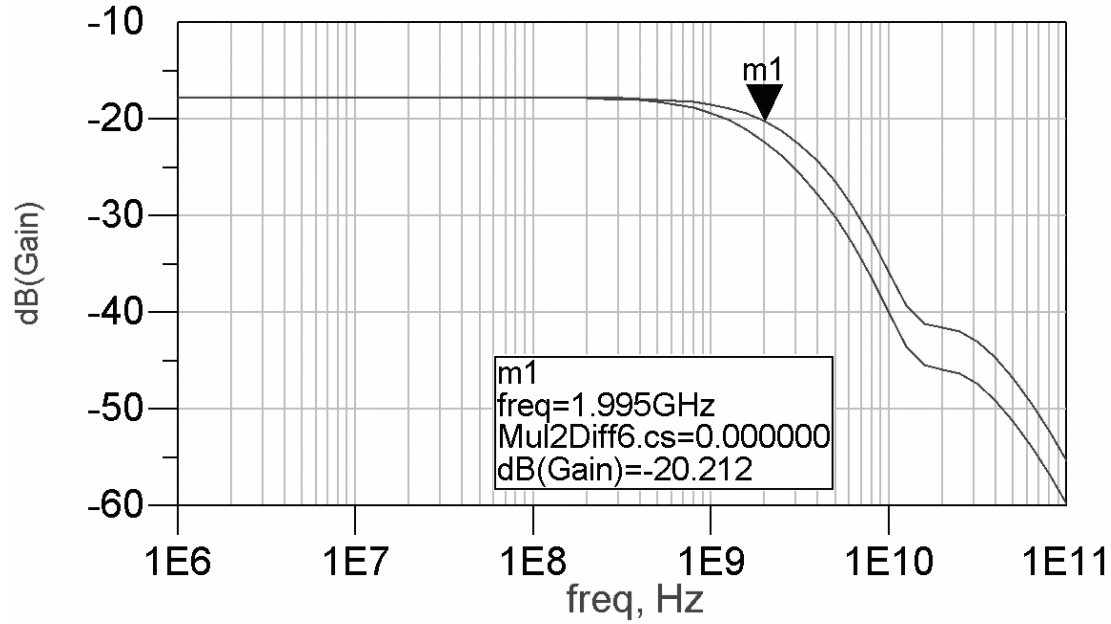


Fig. 3-9 Magnitude response analysis on determining the dominant pole.

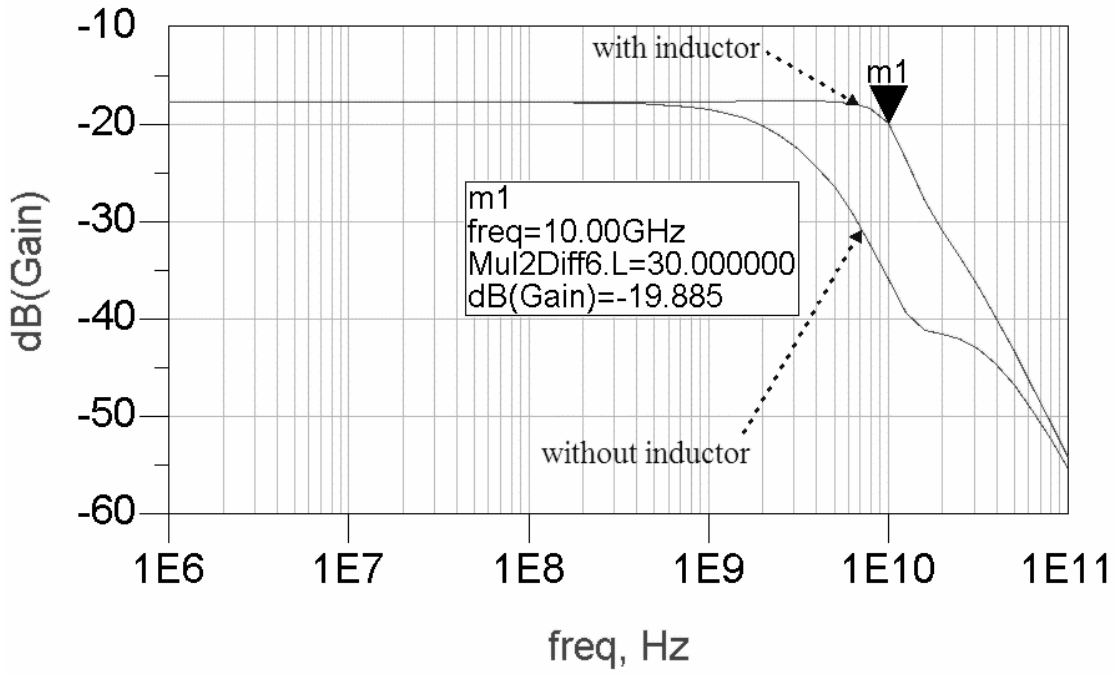


Fig. 3-10 Magnitude response of the multiplier (with and without bandwidth boosting inductor).

3.1.3 Nonlinearity analysis

The linearity is another important factor needs to be considered in a multiplier design. As we all know, CMOS is a square-law device, in which current is non-linear to the

voltage input. To improve the linearity of the device, a non-linearity scheme must be used in the design. A traditional way to cancel the higher polynomial items generated by the non-linear device is to adopt the differential structure. Single-end signal is not preferred because of the uncompleted cancellation of even-order non-linear terms. The linearity can also be improved by the use of triode transistor in this multiplier.

However, the derivation of the multiplication function neglects the second order effect of the transistors, which result in non-linear relationship between output current and input signals. The second order effect of the transistor includes channel length modulation, mobility degradation and mismatch in MOS device. In simple square law model of MOS device, the output current is linear to the input voltage signal $i = g_m v_i$. However, consider the second order effect, the current is expressed as

$$i = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \cdots \tag{1.26}$$

For differential structure, the output current in each branch is given by

$$\begin{aligned} i_1 &= a_1 \frac{v_i}{2} + a_2 (\frac{v_i}{2})^2 + a_3 (\frac{v_i}{2})^3 + a_4 (\frac{v_i}{2})^4 + \cdots \\ i_2 &= a_1 (-\frac{v_i}{2}) + a_2 (-\frac{v_i}{2})^2 + a_3 (-\frac{v_i}{2})^3 + a_4 (-\frac{v_i}{2})^4 + \cdots \end{aligned} \tag{1.27}$$

where v_i is differential voltage input. The total current output is

$$i = i_1 - i_2 = a_1 v_i + \frac{1}{4} a_3 v_i^3 + \cdots \tag{1.28}$$

The current of the single end circuit is the same as Equation (1.26). Therefore, the differential structure not only cancels even-order distortion components, but also reduces the third order coefficient to one fourth of the single end one. Thus, the differential structure is preferred due to improved linearity.

- **Channel length modulation**

The channel length modulation can only be improved by using long channel length devices. However, the minimal channel length transistors provide better performance in high frequency application and high transconductance, which are two major requirements of the multiplier design. Therefore, in the non-linear analysis, we mainly focus on the influence of mobility degradation and mismatch in transistors.

- **Mobility degradation**

The standard model of the mobility degradation is $K_{eff} = \frac{K}{1+\theta(V_{GS}-V_T)}$ [76], θ is the mobility reduction coefficient. Assume $\theta^4(V_{GS}-V_T)^4 << 1$, K_{eff} can be approximately expressed as a third-order polynomial using Taylor series expansion. Substitute K with K_{eff} in the output current expressions when used to derive the multiplication function

$$I_{a1} = \frac{K}{1+\theta(V_{GSa}+v_a-V_{tn})}(V_{GSa}+v_a-V_{tn}-\frac{V_{dsi}}{2})V_{dsi} \tag{1.29}$$

Then the total output current of the multiplier transconductor is given by

$$I = I_{a1} - I_{a2} + I_{b1} - I_{b2} = 2Kv_b[(1+\theta(V_{GSa}-V_{tn}))^2 v_a + \frac{\theta^2 v_a^3}{4}] \tag{1.30}$$

where v_b is a constant. From Equation (1.30), with a balanced differential signal added at two inputs of the differential pair, the second-order harmonic distortion can be cancelled if all the transistors are matched. In addition, the third-order harmonic is reduced to one fourth compared with unbalanced signals input. The nonlinearity of the multiplier with one signal input while keeping the other signal at a constant difference is defined as $a_3/a_1 = \frac{\theta^2}{4[1+\theta(V_{GSa}-V_{tn})]^2}$, thus the harmonic distortion changes inversely with the common mode voltage. Thus, to improve the linearity of the multiplier, the

bias gate-source voltage needs to increase. Since the lower transistors operate in triode region, the increment of the gate-source voltage also can improve the dynamic range of the multiplier.

3.1.4 Noise analysis

Another performance specification of a multiplier for wireless communication is noise, since the power of the input signal is quite low. The current power density of the thermal noise in CMOS transistor is defined as

$$\begin{aligned} \overline{i_{sat}^2} &= \frac{8}{3} KTg_{ms} df \\ \overline{i_{tri}^2} &= 4KTg_{mt} df \end{aligned} \tag{1.31}$$

g_{ms}, g_{mt} are transconductance of the MOS transistor in saturation region and triode region respectively.

$$\begin{aligned} g_{mt} &= K_t(V_{GSt} - V_T - V_{DSt}) = K_t(V_a - V_T - (V_b - V_T)) = K_t(V_a - V_b) \\ g_{ms} &= \sqrt{2K_s I_s} = \sqrt{2K_s K_t (V_a - V_T - \frac{V_b - V_T}{2})(V_b - V_T)} \end{aligned} \tag{1.32}$$

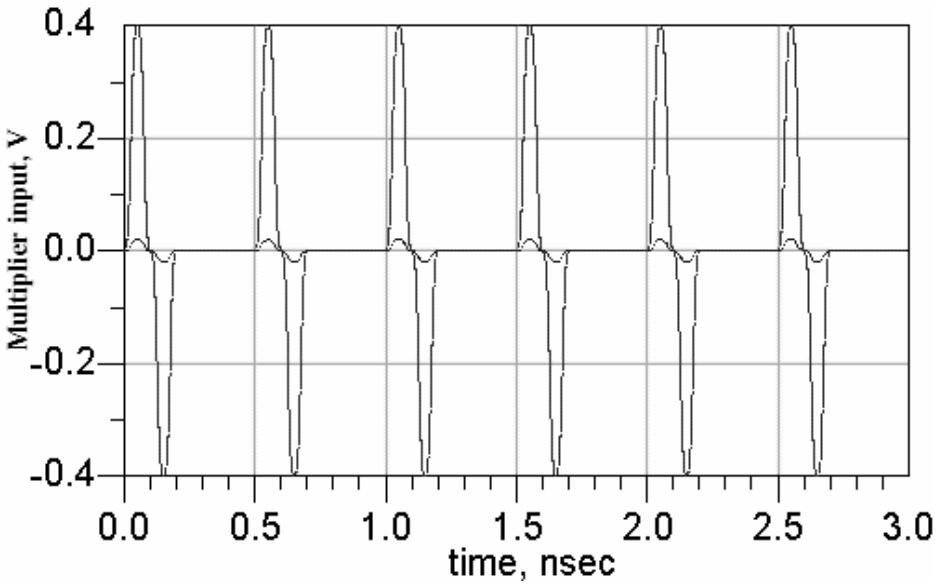
Here, V_a, V_b is the bias voltage at the gate of lower four triode transistors and upper four saturated transistors respectively. K_s and K_t is the conventional notation of the transistor parameter in saturation and triode region. Then the total noise at the output current of the multiplier transconductor is given by

$$\overline{i_n^2} = 4(\overline{i_{sat}^2} + \overline{i_{tri}^2}) = 4(4KTg_{ms} df + \frac{8}{3} KTg_{mt} df) = 16KT(g_{ms} + \frac{2}{3} g_{mt}) df \tag{1.33}$$

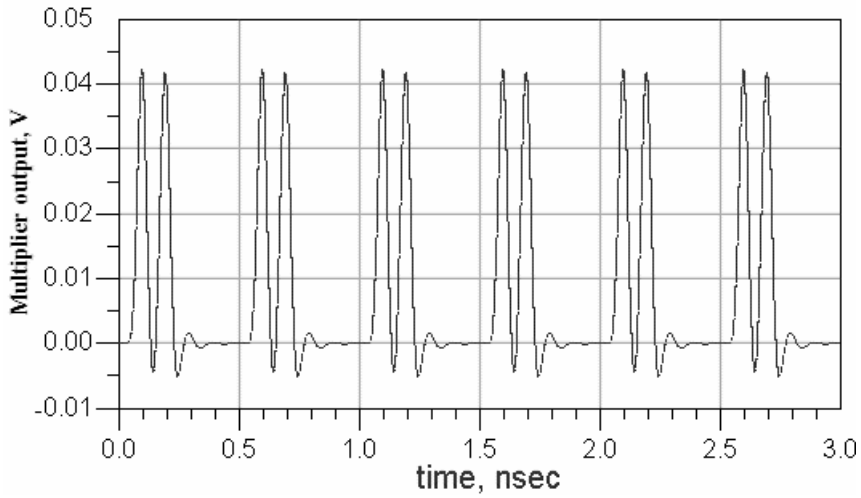
From Equation (1.33), since the transconductance of triode transistor is less than that of the saturation one, the triode transistor multiplier has lower noise floor compared with the saturation structure.

3.1.5 Simulation results of the active multiplier

In order to test the time domain response, two monocycle pulses with same width of 0.2ns, but different amplitudes are used. This is to consider the case in the real correlator where the received signal is weaker than the template signal. The pulse with small amplitude is applied to gates of the lower transistors, while the large pulse is to the upper transistors. The two pulses of 0.2ns are generated by the differentiator from a square wave input. Fig. 3-11 gives the transient simulation result, where (a) shows the two input pulses and (b) the output of the multiplier. Correct output is obtained at the output of the multiplier. It shows that the multiplier has sufficient bandwidth and is able to work with the sub-nano second pulse inputs.



(a)



(b)

Fig. 3-11 The multiplication of two synchronized narrow pulses in time domain.

The linearity of the multiplier is tested in a conventional way in which the DC transfer characteristic with respect to input to the lower transistors (M1-M4) is observed, while the input to the upper transistors (M5-M8) is used as a parameter. The results are shown in Fig. 3-12. Each curve represents a 100 mV step from -300mV to 300mV. A good linearity is obtained. In practice, the amplitude of the input signal is much smaller than 150mV and thus the linearity of the multiplier will be better than what is observed for the large input range.

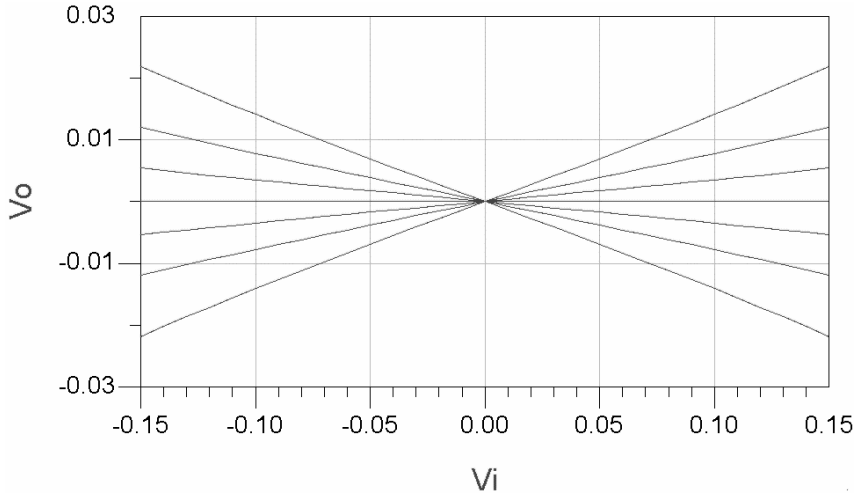


Fig. 3-12 Multiplier DC transfer characteristic.

3.2 Passive Multiplier Design

3.2.1 Passive multiplier

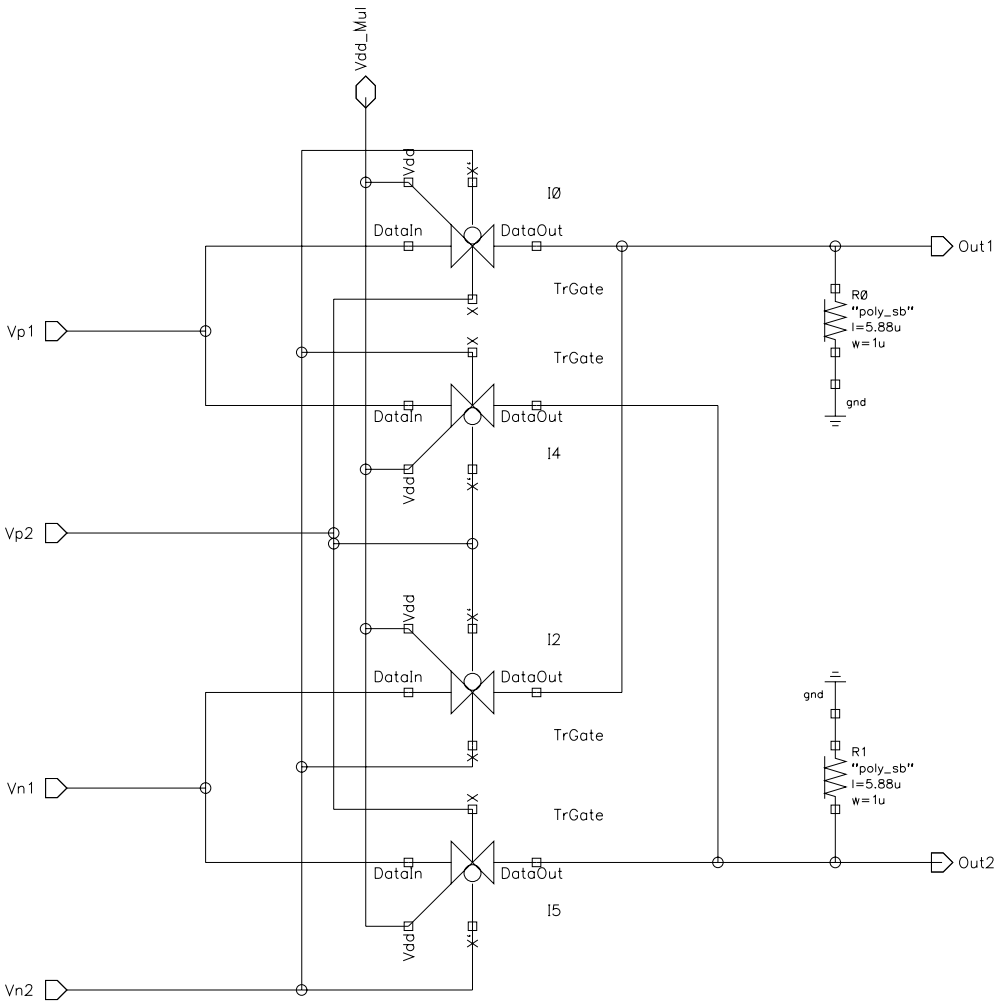


Fig. 3-13 Schematic of Passive multiplier.

This passive multiplier, shown in Fig. 3-13, has a simple and symmetric architecture. It has the advantages of wide bandwidth, high port-to-port isolation, small chip area and low power dissipation. This passive multiplier consists of four pairs of transmission gates, I0-I3, as in Fig. 3-13. The transmission gate is composed of a NMOS and a PMOS transistor. Considering the different mobilities of NMOS and PMOS transistors, the channel width of PMOS is chosen to be about 3 times larger than that of NMOS.

The transmission gate is controlled by a differential pulse signal. In a modulator, the gate-controlled pulse signals are generated from the baseband, which symbolize the data transmitted. V_1 is differential voltage of two input UWB pulse signals (normally the pulse's width is less than 500ps and the period of the pulse is around 10ns). When the transmitted signal is '1', I0 and I5 open, I2 and I4 close, thus $V_1/2$ passes through I0 and $-V_1/2$ passes through I5. Otherwise, when the transmitted signal is '0', I0 and I5 close, I2 and I4 open, then $V_1/2$ passes through I4 and $-V_1/2$ passes through I2 to make an invert output. This scheme of modulation is called BPSK. The multiplication function of the multiplier is $V_o = V_1 \times V_2$ (V_2=±1).

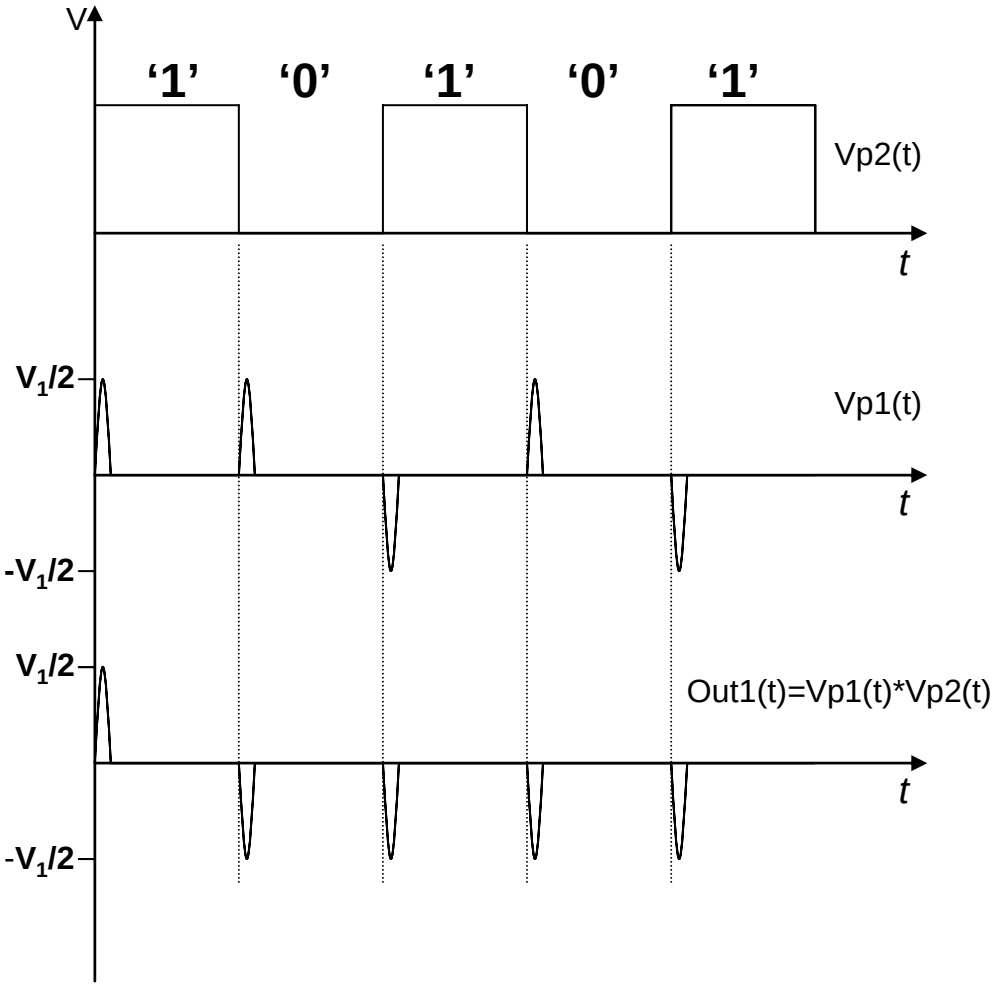


Fig. 3-14 Passive multiplier function as a modulator.

3.2.2 Simulation results

Fig. 3-15 shows the simulation result of the modulator using BPSK in ADS analog environment. Fig. 3-15(a) shows differential input pulse after pulse shaping circuit, which limits the bandwidth of the pulse to 2GHz from 1GHz to 3GHz. Fig. 3-15(c) simulates a modulated code. High level is corresponding to '1' and low level, to '0'. (Vn2 is complement with Vp2 and not shown here). Vp_m and Vp_p is a zoom-in view to the wide bandwidth pulse in one period (10ns) in Fig. 3-15(b). From the output signal Vm_p in Fig. 3-15(d), the signal is modulated quite well because the pulse in the first period is different from the pulse in the second period by 180^o in

phase. The two plots in Fig. 3-15 (e,f) show the frequency spectrum of the input pulse and output modulated pulse. From the comparison in the power spectrum, the power of the output modulated signal is -60dB, which is close to that of the input pulse signal. Therefore the passive multiplier exhibits an excellent frequency response to wideband pulses with high repetition rate.

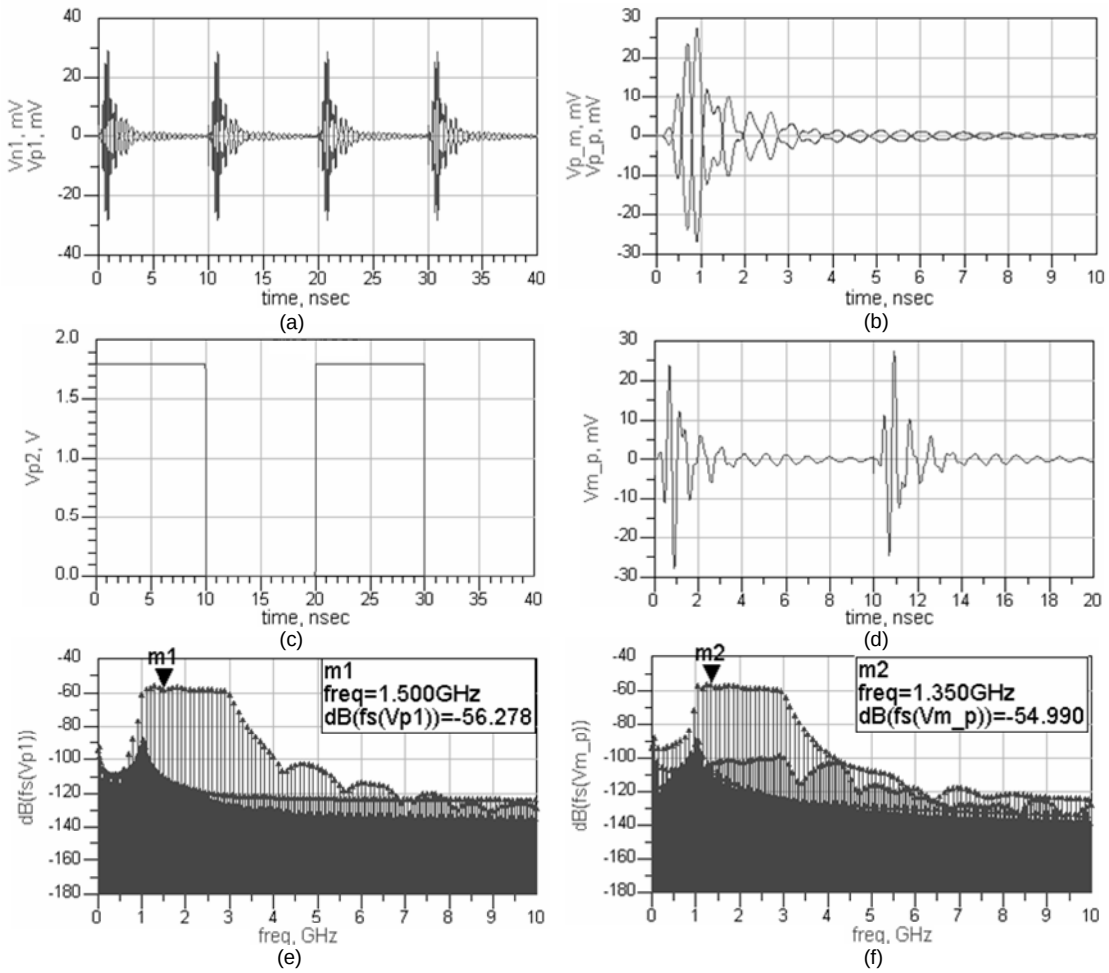


Fig. 3-15 Simulation result of the BPSK modulator
(a) differential pulse input (b) one period zoom in of input differential pulse (c) modulated code (d) modulator output (e) input pulse's spectrum (f) output modulated signal's spectrum.

3.3 Integrator Design

A critical component of the UWB transceiver system is the integrator at the heart of the time-integrating correlator. It must have both sufficient bandwidth to integrate a pulse of 1 ns and be able to hold the integrated signal over a period of 10 ns. These two requirements can not be met at the same time. This is because the charge and discharge of an integrating capacitor is normally determined by the same time constant. In order to hold the signal on the integrating capacitor, it must be disconnected from the integrator, disconnecting from the discharging path. The holding of the signal is thus only dependent on the leakage current that is normally quite small. Alternatively, relatively larger capacitance can be employed to increase the holding time. In the case of large integrating capacitor, the integrating speed can be increased by reducing the equivalent *R*, which also means to increase the charging current.

3.3.1 Transconductor-C integrator

The transconductor-C integrator is designed based on an inverter [77], as shown in Fig. 3-16. K_1 K_2 are two switches. The function of K_1 is to break down the auto discharging path. When the integrator works, K_1 is close to inject current into the capacitor. In order to hold the integrated voltage at the side of the capacitor, K_1 is open after integration. K_2 is a discharging switch to reset the integrator after one period for next operation. The output current of the transconductor $I_0 = I_1 - I_2$, where

$$I_1 = \frac{\beta_n}{2}(V_C - V_{ss} - V_{TN})^2$$
$$I_2 = \frac{\beta_p}{2}(V_{dd} - V_C - |V_{TP}|)^2 \quad (1.34)$$

Here, square law models for MOS devices are assumed. β_n, β_p are transistor parameters and V_{TN}, V_{TP} are threshold voltage of MOS transistors. V_C is the bias voltage at the input. Also, all devices are in saturation mode. Assume NMOS and PMOS transistors are selected in such a way that for $V_{in}=V_C$ ($v_{in}=0$), $I_0=0$, thus we get

$$\frac{\beta_n}{2}(V_C - V_{ss} - V_{TN})^2 = \frac{\beta_p}{2}(V_{dd} - V_C - |V_{TP}|)^2 \quad (1.35)$$

When $v_{in} \neq 0$, that is $V_{in}=V_C+v_{in}$

Now the output current can be derived from Equations (1.35).

$$I_0 = I_1 - I_2$$
$$= \frac{\beta_n}{2}(V_C - V_{ss} - V_{TN})^2 - \frac{\beta_p}{2}(V_{dd} - V_C - |V_{TP}|)^2 \quad (1.36)$$
$$= \frac{\beta_N - \beta_P}{2}v_{in}^2 + [\beta_N(V_C - V_{ss} - V_{TN}) + \beta_P(V_{dd} - V_C - |V_{TP}|)]v_{in}$$

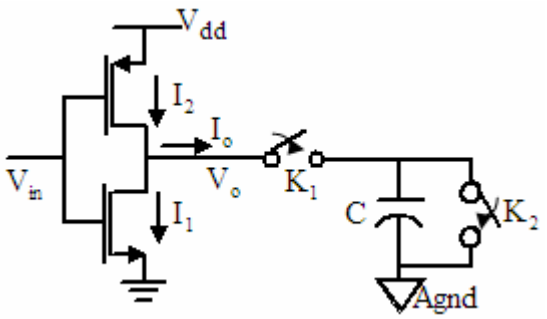


Fig. 3-16 Transconductance integrator with a pair of switches.

In the ideal case, if $\beta_N \approx \beta_P = \beta$, the transconductance is

$$g_m = \frac{I_0}{v_{in}} = \beta(V_{dd} - |V_{TP}| - V_{ss} - V_{TN}) \quad (1.37)$$

From the equation, the linear relationship of input voltage and output current can be seen. The transfer function of this circuit is(C is the capacitance of the integrating capacitor):

$$\frac{V_0}{V_{in}}(s) = \frac{g_m}{sC} \tag{1.38}$$

Due to the existence of output resistance *R*, the practical transfer function is given below

$$\frac{V_0}{V_{in}}(s) = \frac{g_m}{\frac{1}{R} + sC} \tag{1.39}$$

In order to make the integrator close to an ideal one, the output resistance of the transconductor needs to be as large as possible.

Fig. 3-16 shows the circuit for the inverter based integrator where only half of the differential structure is shown. Each transconductor consumes a supply current of 1.98mA. The transconductance is 13.2mS with a broad flat bandwidth up to 10GHz to reduce the excess phase shift and obtain a near-ideal integrator response. Given a constant g_m with a second pole over 10GHz, the transfer function of the circuit can be expressed by $V_o / V_{in}(s) = g_m /(sC + 1/R)$ (R is the output resistor of the transconductor). Switch K_1 is added to the output of the transconductor to increase the output resistance so as to hold the voltage on the capacitor during the holding period. The other set of complementary switches K_2, controlled by a non-overlapping clock with respective to K_1, allows the integration capacitors to be rapidly discharged.

Two factors need to be considered in designing an integrator:

A. DC Enhancement

Normally, an ideal integrator transfer function is difficult to obtain. One often seeks the first-order system with a frequency response close to an ideal one. An ideal

integrator should have an infinite gain at DC frequency. Because the gain bandwidth is constant, to maximize the gain means to reduce the bandwidth of the first-order circuit. Since the bandwidth is decided mainly by parasitic capacitance and resistor, increasing the value of parasitic capacitor or resistor can limit the bandwidth either. However, in UWB transceiver, the integrator is required to have a fast response within 1ns, thus the capacitor cannot be chosen large. Therefore, the only way to enhance the DC gain is to maximize the output resistance of the transconductor. A DC gain enhancement scheme is adopt in an improved version.

B. Bandwidth extension

In integrator design, cut-off frequency is another important parameter needed to be considered, which determines the time of integration process. The response time of the integrator is controlled by the output integration capacitor. Small capacitance will lead to fast response.

3.3.2 Theory analysis of the new inverter based integrator

This integrator is based on inverter like Gm-C cells. A single Gm-C cell is composed of a pair of PMOS and NMOS like an invertor structure. However, since those two transistors are properly biased in saturation region, the output current is

$$i = i_1 - i_2 = v_{in}(V_{dd} - V_{tn} + V_{tp})\sqrt{\beta_n \beta_p} \tag{1.40}$$

Therefore the transconductance of a single Gm-C cell g_m is $(V_{dd} - V_{tn} + V_{tp})\sqrt{\beta_n \beta_p}$.

Before the analysis of the integrator, a negative resistor network is introduced in Fig. 3-17. This network exhibits different resistance with differential and common mode signals. To quickly get the conception of the negative resistance, we use unit voltage to be added at both nodes of the network. Since the two nodes are symmetric, consider node 1 as an example. For differential signal input in Fig. 3-17(a), node 1 is added with a unit voltage and node 2 with a minus unit voltage. Then the conductance can be simplified to be equal to the output current *i*. Since $i_1=g_{ma}$ and $i_2=g_{mb,}$ the input resistance is

$$R_{neg-diff} = 1/G = 1/i = 1/(i_1 + i_2) = 1/(g_{mb} - g_{ma}) \tag{1.41}$$

Similarly, for common mode signal input, the input resistance of such a network is

$$R_{neg-comm} = 1/G = 1/i = 1/(i_1 + i_2) = -1/(g_{mb} + g_{ma}) \tag{1.42}$$

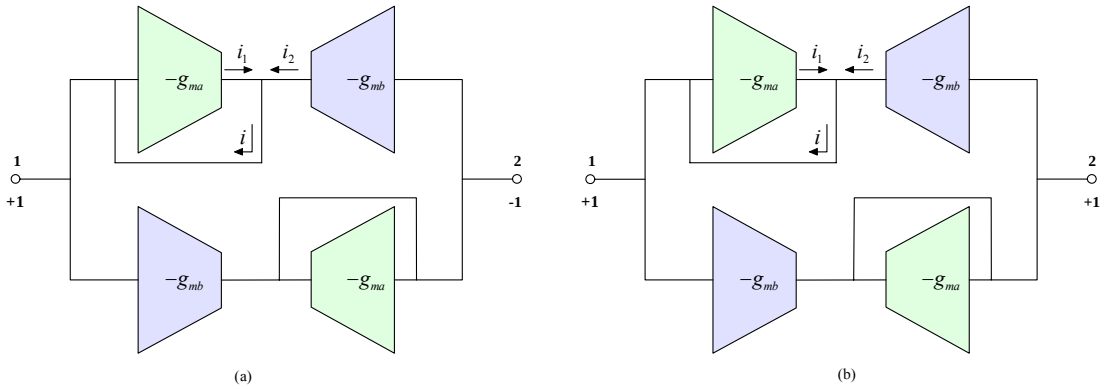


Fig. 3-17 Negative resistor network (a) differential mode and (b) common mode.

Now, let us come back to analyze the circuit in Fig. 3-18.

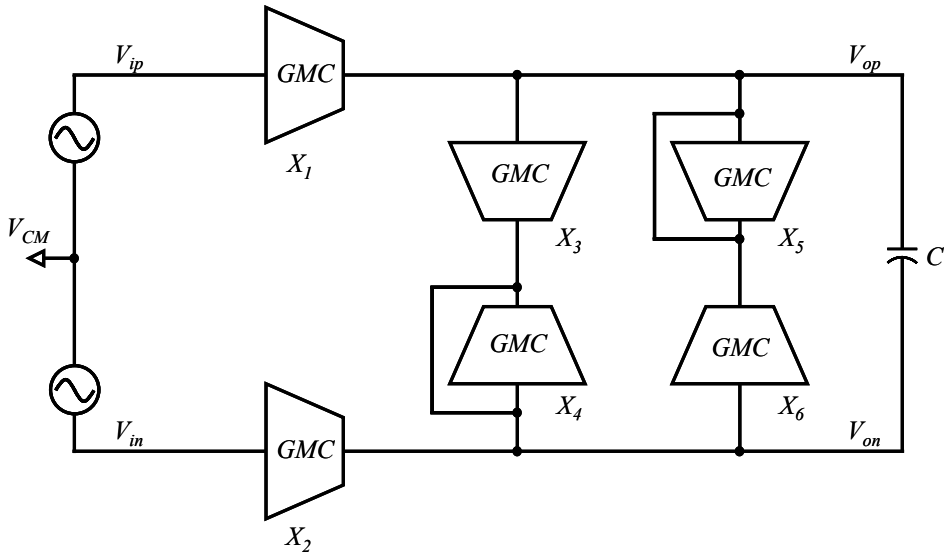


Fig. 3-18 Nauta's transconductance integrator top view.

The common mode and differential signal of the output are controlled by the four transconductor X3-X6, which form a negative resistance network. The result for common mode output signals is that node V_{op} is virtually loaded with a resistance $1/(g_{m5}+g_{m6})$ and node V_{on} is virtually loaded with a resistance $1/(g_{m3}+g_{m4})$, respectively. For differential signals input, node V_{op} is virtually loaded with a resistance $1/(g_{m5}-g_{m6})$ and node V_{on} with a resistance $1/(g_{m4}+g_{m3})$. If the four inverters have the same supply voltage and are perfectly matched, then all of the transconductance are equal. Therefore, the network provides a low resistance to the common mode signals and a high output resistance to the differential signals. The DC gain of the integrator can be increased by introducing a negative resistor load. By choosing $g_{m3}>g_{m4}$, $g_{m3}=g_{m6}$, $g_{m4}=g_{m5}$, this negative resistance $r_{reg}=\frac{1}{g_{m4}-g_{m3}}=\frac{1}{g_{m5}-g_{m6}}$ is simply implemented without adding extra nodes to the circuit. Thus the supply voltage of X4, X5 can be made lower than that of X3, X6. Ideally, the cancellation network can make the output resistance infinite. However, considering the output

resistance of each inverter, the voltage gain can be increased to 30dB compared with 10dB when there is no negative resistor load. Therefore, a significant improvement of the integrator DC gain is achieved without affecting the bandwidth. This is mainly because the negative load network dismisses the contact relationship of DC gain and bandwidth by adjusting the output resistor and capacitor separately.

3.3.3 Simulation result of integrator

A. Integrator DC gain enhancement

Fig. 3-19 is the frequency response of the integrator with DC gain enhancement. Varying the supply voltage of X4 and X5 changes the negative resistance to cancel the output impedance of the three transconductor. From the simulation result, the DC gain changes with the variation of supply voltage on X4 and X5. Because the DC gain is $g_m R_{out}$ (g_m is constant), the output resistance reaches the maximum value at a certain voltage (1.56V), which matches the analysis of the DC gain enhancement quite well.

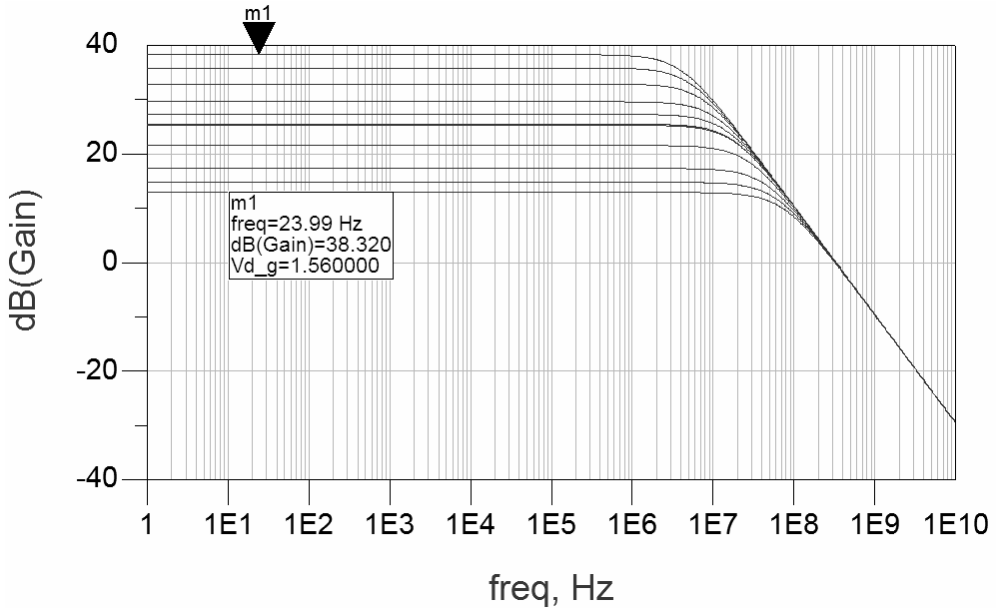


Fig. 3-19 Gain enhancement by adjusting the value of the negative resistor load.

B. Transient simulation result

Once chosen a supply voltage which is optimized for maximum DC gain, the transient simulation is conducted to verify the function of integrator in time domain. Fig. 3-20 shows the input signal pulse and output of the integrator respectively. In time domain, the input 0.2V differential pulses can be integrated to a voltage enough high (0.9V). The output signal can trace the variation of input signal quickly, which means the integrator has a fast response to narrow pulse signal. At the end of a period, the reset signal comes to discharge the information stored in the both side of the integration capacitor. The discharging period is very fast for the next integration process.

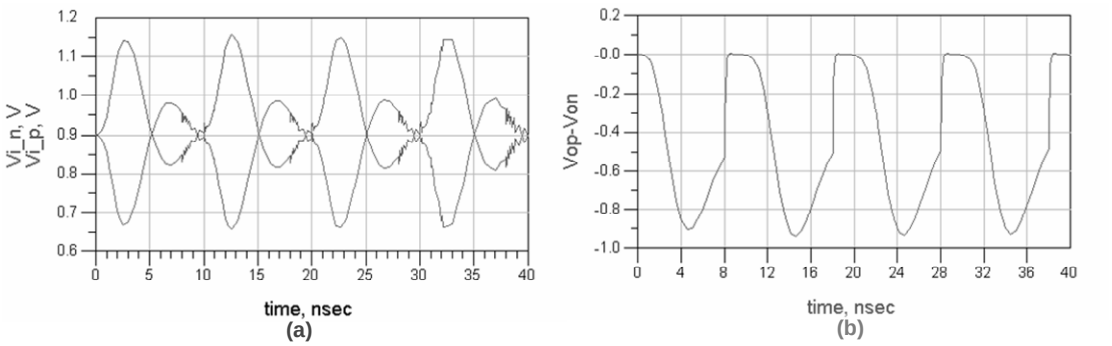


Fig. 3-20 Simulation results of Nauta's transconductance integrator (a) input differential pulse (b) differential output.

3.4 Layout Consideration and Post Layout Simulation

3.4.1 Layout technique

All the layout are drawn using 0.18-um CMOS technology under Cadence environment. In order to obtain better matching, the differential transistors are placed in close proximity in the layout and the large finger transistors are designed using cross-coupled structure. The interconnections are made as short as possible to reduce

the parasitic effect. Octagon-shaped inductors are self designed to obtain a constant inductance in the frequency range from 3GHz to 10GHz. To reduce the parasitic capacitance of the inductor at high frequency, Metal 5 is used to implement the inductor instead of normal top metal layer, because the width of line and spacing in metal 5 can be made smaller than that of top metal. Another advantage is the reduced area of inductor with large value. Since the inductor series with a resistor, there is no critical requirement on the Q factor.

3.4.2 Post layout simulation

Since the multiplier operates with two wideband input pulse signals, the most critical problem in the test is the parasitic in the signal path. Therefore, in the post layout simulation, a detailed channel model for the input and output signal path should be included. In this channel model, the transmission line of different metal layers in the layout is considered. Since the differential input and output structure doubles the number of pins, which exceed the maximum port supported by probe station, a Chip-On-Board (COB) packaging is taken as an alternative to the on-wafer test. The disadvantage of this measurement method is the deterioration of the measurement result due to the additional parasitic effect of the bonding wire and PCB board. Thus a post layout simulation with consideration of these effects is necessary to ensure the first-time success.

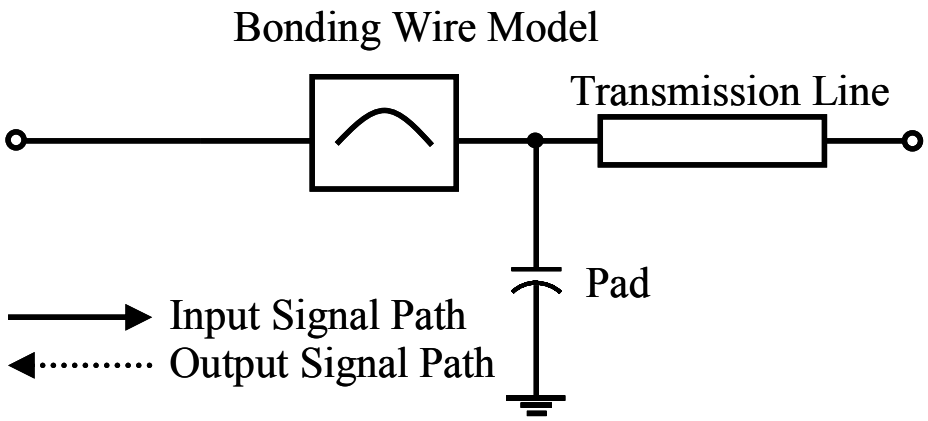


Fig. 3-21 Signal path model from signal source to the input pin.

One complete input signal path in the post layout simulation is explained in Fig. 3-21. First, a 50Ω resistor load is added after the ideal signal source to simulate the signal generator. The transmission line on PCB board as a connection to outside is omitted in this channel model because the wire is placed on PCB design to match 50Ω. This simplifies the complexity in the post layout simulation and reduces the simulation time. A bonding wire model is used to emulate the real gold wire connecting the die to the PCB pad, follower by the pad capacitor. Before the signal enters into the core of the multiplier, a transmission line model is inserted to include the parasitic effect of different metals. Another important thing in the post layout simulation is to see the effect of the load of the multiplier on the frequency response. In the correlator, the multiplier is directly followed by an integrator, which provides high input impedance. While in the testing, the device under test is often connected to a 50-Ω matching load or from the test instrument, which may greatly reduce the gain of the multiplier. To avoid this problem, a buffer can be added. Through the post layout simulation, we find the length of the interconnection between multiplier and voltage buffer is quite

critical to the bandwidth of the multiplier. This is shown in Fig. 3-22. To reduce the effect of the interconnection on the bandwidth, the length of the wire in the layout is made as short as possible. This is because the multiplier has relatively high output load in order to achieve high gain. The large parasitic capacitance at its output could make the dominant pole to shift to the output node, and thus make the bandwidth enhancement technique less effective. In designing a wideband buffer, a trade off is made between the bandwidth and gain.

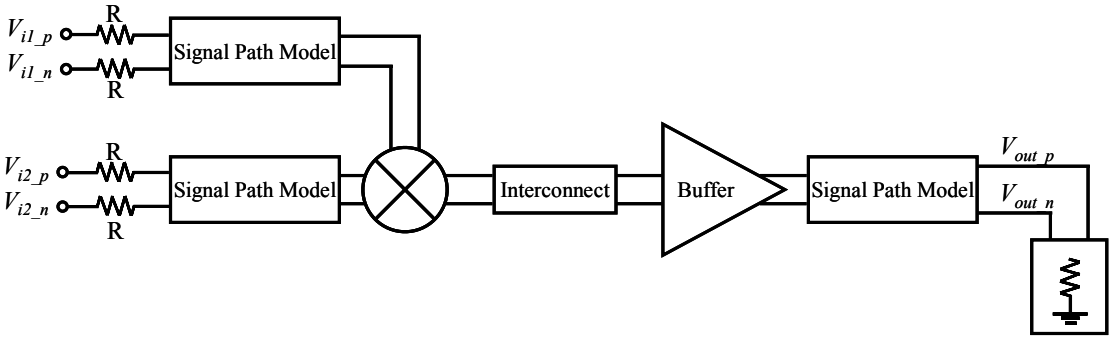


Fig. 3-22 Post layout simulation environment.

The block diagram of the complete correlator is shown in Fig. 3-23. The output buffer of the multiplier is used to isolate the loading effect from the integrator. A level shifter is inserted after the buffer to provide the required DC bias to the integrator. The output buffer of the correlator is added to drive the 50-Ω input impedance of the test instrument.

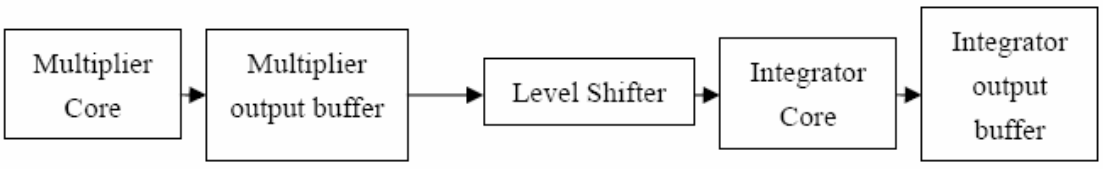


Fig. 3-23 Block diagram of the tapeout correlator for testing.

CHAPTER 4 TEST AND MEASUREMENT RESULT

4.1 Test Preparation

4.1.1 PCB design

Since the multiplier and correlator operate at very high frequency, the material of the PCB is Rogers, a common material used for high frequency printed circuit board. In the PCB layout design, all RF signals have fixed width and clearance to ground plan, which is calculated with coplanar transmission line model by Agilent AppCAD software. Power and ground are maximized to reduce the parasitic resistance. Vias are placed in the free areas of ground plan to lower the potential to the real 'zero'. All the RF signal ports use 50Ω SMA connectors, which are semi-precision, subminiature units that provide excellent electrical performance from DC to 18 GHz. These high-performance connectors are compact in size and mechanically have outstanding durability. Three decoupling capacitors of different values are connected between power and ground filter out the noise in the power supply.

4.1.2 Test setup

Fig. 4-1 shows the test setup, where signal generated by an impulse sources are differential and applied to one input port with a pair of bias tee. DC bias voltage is added to the other input of the bias tee. The pattern generator provides two group control signals. One group signal contains a pair of complementary digital signals. When finish set up the input signal, a high frequency oscilloscope with the sampling

rate at 6GHz is needed to probe the output signals of the designed chip. To measure the frequency response, a 26GHz network analyzer is necessary. Spectrum analyzer is also prepared to verify the function of multiplier in frequency domain. DC blocks are connected at the output to filter out DC. This is to avoid the large DC level being directly at the spectrum analyzer.

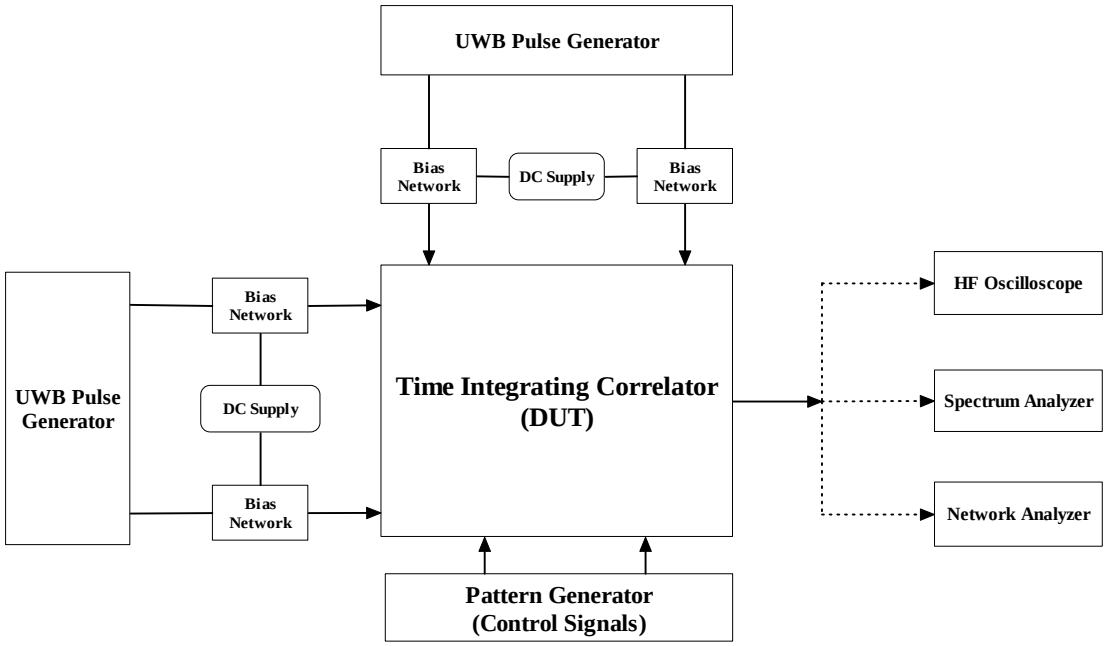


Fig. 4-1 Test platform of the time integrating correlator.

To generate differential input pulse signals, both positive and negative channel of the UWB pulse generator are used. Because the positive and negative channel are not in phase, which leads to one channel lags the other channel of about 200ps, cords are inserted to the lead channel as delay line to synchronize the output signals of the pulse generator. Since the multiplier has two inputs, it is hard to use the normal way to test the frequency response. Therefore, refer to the measurement method in Section 3.1.2, which is defined by setting one input of the multiplier to a fixed offset (delta x), then measuring the forward transmission parameter of the other input to the output of

multiplier. In this setup, the multiplier works as a fixed gain differential amplifier, therefore it is easier to measure the frequency response. In the measurement setup, since a power splitter with a frequency range from 3GHz to 10GHz is not available, we have to terminate one input port and also one output port with 50 Ohm to make the circuit balance, and then measure the S21 parameter of the other input and output port using network analyzer. Therefore, the frequency response of the multiplier can be evaluated. The simulation results under the same setup are also conducted to compare with the measurement results.

The equipment used in the measurement is listed in Table 4-1.

	Model	Manufacture
UWB Pulse Generator	TFP1001	Multispectral Solutions, Inc
Oscilloscope	DSO80804A	Agilent
Spectrum Analyzer	FSQ26	Rohde&Schwarz
Network Analyzer	HP8720D	Agilent
Data Pattern Generator	DG2030	Tektronix

Table 4-1 Equipment used in the measurement

4.2 Measurement Result

The correlator chip fabricated in a 0.18μm CMOS technology and chip microphotograph is shown in Fig. 4-2. For simplicity, other circuits' layout and die photos are listed in Appendix A for layout and Appendix B for fabricated chip separately. Because the best/worst case performance simulations are not executed, the best test results are selected to be reported here.

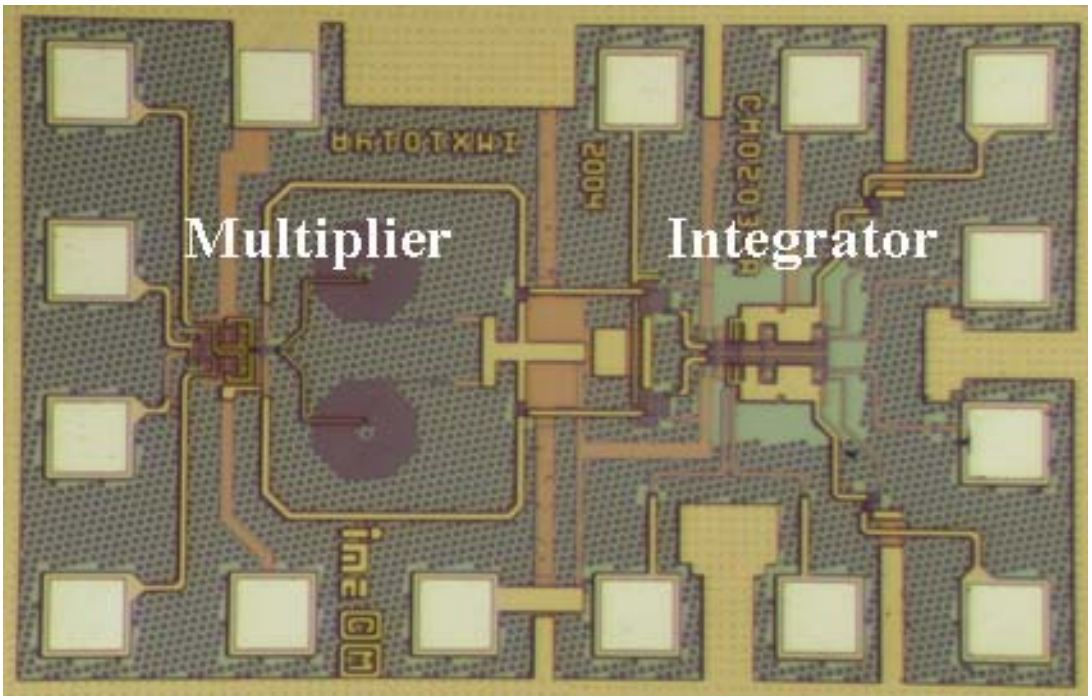


Fig. 4-2 Micrograph of the correlator (die size 0.6x0.9mm^2).

4.2.1 Multiplier

A. Wideband multiplier

The S-parameter of inductance is measured using coplanar ground-signal-ground (GSG) probes and an open test structure for calibration on a 26GHz network analyzer. The fabricated inductor test structures are listed in Appendix B for reference. The inductance is extracted from the measured S-parameter. In Fig. 4-3, we note that the measured inductance match the 10nH value used in the simulation at 3GHz. At 10GHz, the inductance rises up to 12nH due to parasitic capacitance. This is acceptable as the post layout simulation shows a 20% error in the inductance up to 10GHz can be tolerated. The series resistance of the shunt-peaking inductor with less parasitic capacitance contributes to improve the gain of the multiplier as a part of the load resistor. By using metal 4 and metal 5 instead of the top metal (metal 6), the area

of the inductor with large value can be greatly reduced, as shown in Fig. 4-2. The Q factor of the inductor is not important since large Q can be voided by the output load resistor connected in series with the inductor.

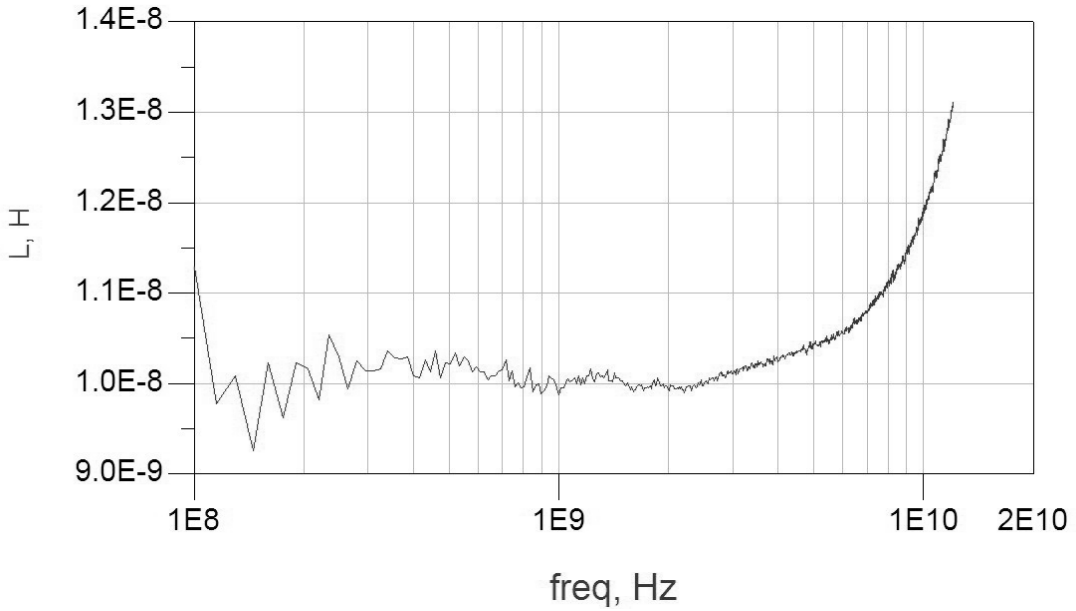
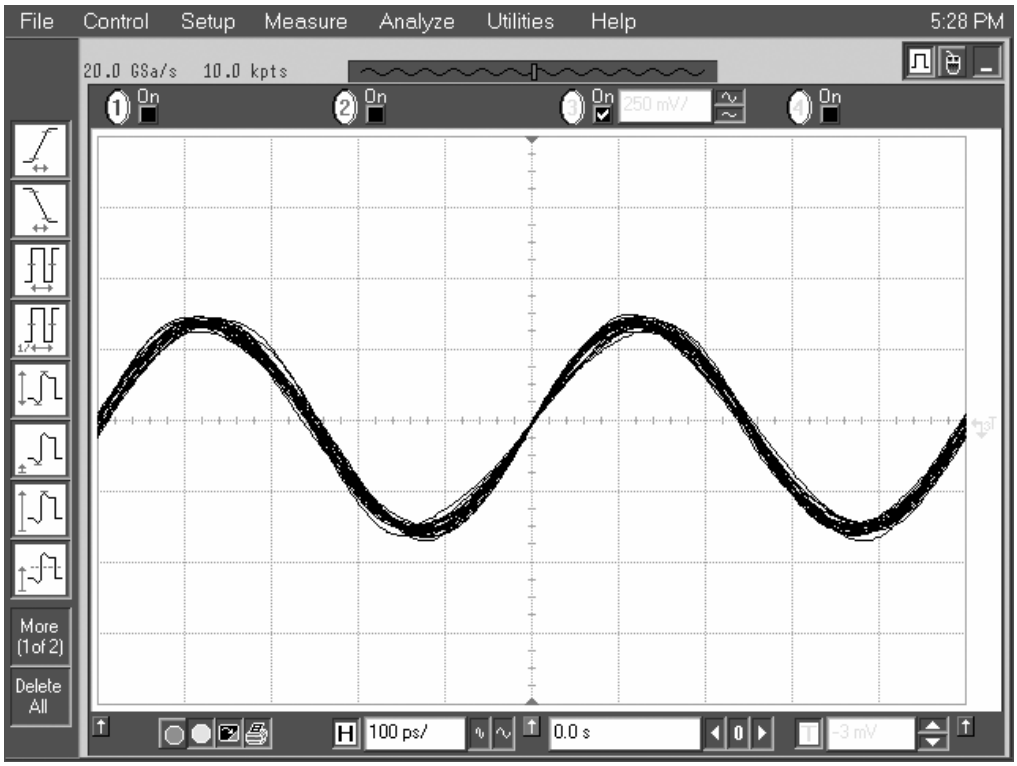
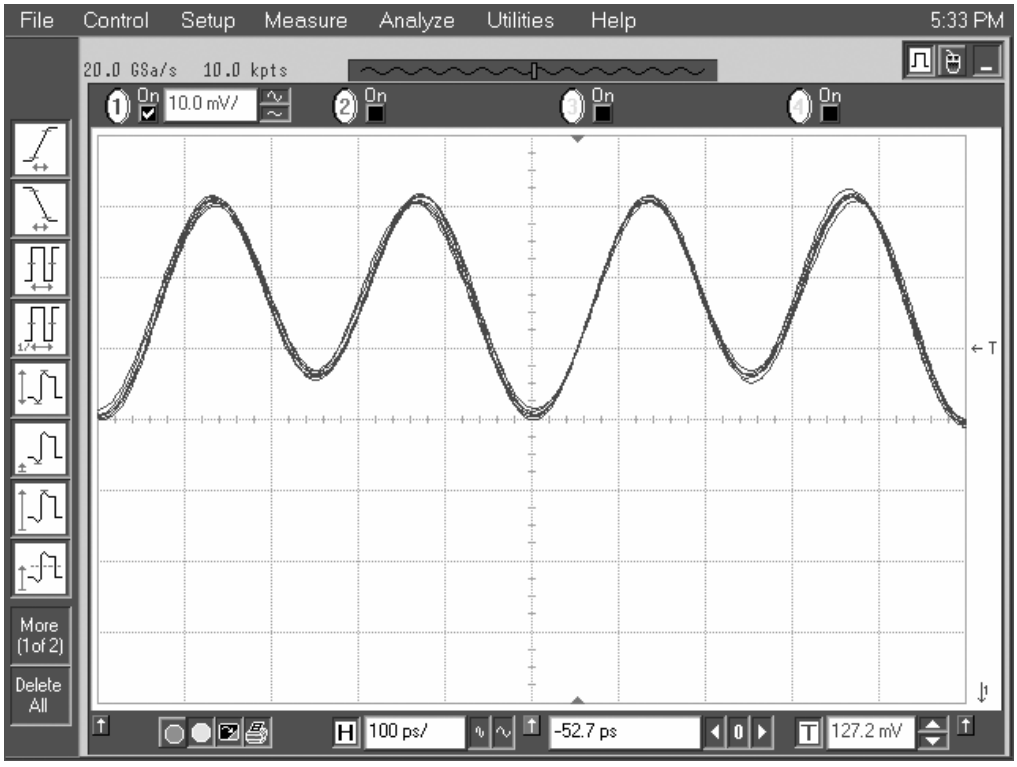


Fig. 4-3 Measured inductance value.

Fig. 4-4 shows the test result of the multiplier. The two input signals to the multiplier are the sinusoidal waves with the same frequency of 2GHz, but different amplitudes of 100mv and 50mv, respectively. Larger signal is injected at LO port in Fig. 3-2, because the power of local template can be made larger compared with the received one. The output shows the multiplication of two synchronized sine waves, where the output is also a sinusoidal signal with twice of the input frequency and positive amplitude.



(a)

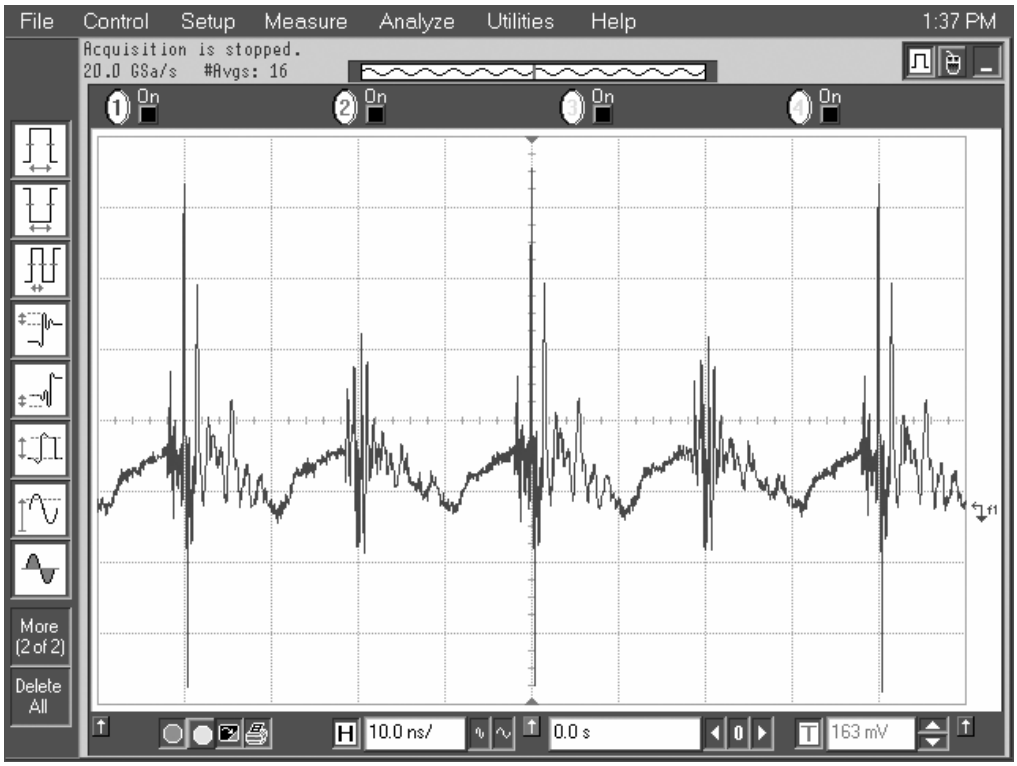


(b)

Fig. 4-4 Output from the multiplier tested with two 2-GHz sine wave inputs (a) one input sine wave at 2GHz (b) output of the multiplier with two peaks in 5ns.

The multiplier is also tested using a monocycle pulse and a template. Fig. 4-5(a) shows the two input Gaussian pulses. The two pulse signals are derived from a single pulse generator with one being inverted and the repetition frequency is controlled by a data generator. The pulse generated is a doubly-exponential pulse with extremely fast rise time and the pulse width is 500ps. The frequency of the UWB pulse is 50MHz and that of the template is 25MHz. Fig. 4-5(b) shows the output of the multiplier. It can be seen that the incoming pulses are correctly detected. The slightly noisy output is due to the small phase difference between the "differential signals", which is generated by inverting the input signal using an inverting amplifier.

(a)



(b)

Fig. 4-5 Output of the multiplier tested with UWB pulses (a) input UWB pulses, upper one is 2 times faster than the lower one (b) differential output result.

The magnitude frequency response of the multiplier is measured by biasing the LO input to a constant value and measuring the forward transmission parameter from RF to the output. There are two main factors contributing to the bandwidth degradation. First, the multiplier is loaded with a non-ideal buffer with gain loss to trade off wide bandwidth and second the inductance fabricated in the chip is 10nH, instead of 30nH as required by simulation, which is shown in Fig. 4-6. This is because of the difficulty to fabricate such a large inductor with constant inductance of 30nH over the wide frequency range in the state-of-art process. Therefore, low inductor causes the mismatch of pole and zero location, which leads to the gain drop within these two

frequency points. Since the chip is mounted on PCB using chip-on-board technology, the additional parasitic capacitance on the PCB also loads the output of the multiplier.

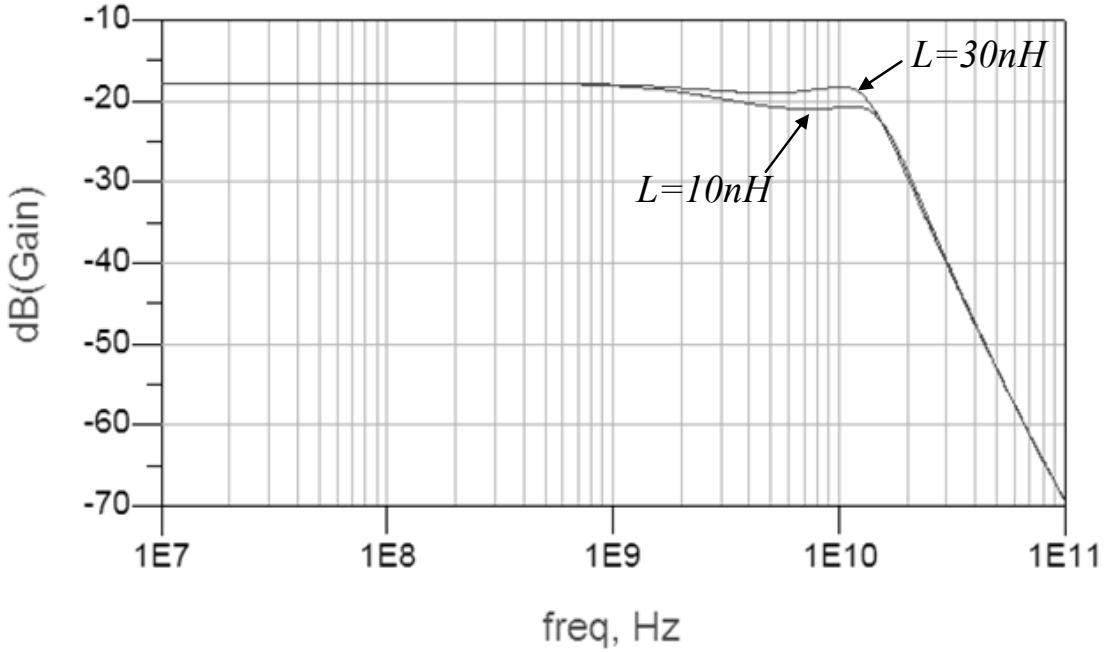


Fig. 4-6 Lower inductance reduces the bandwidth of the multiplier.

Fig. 4-7 is the scattering parameter (S21) extracted from the measured data on a 26-GHz network analyzer. For comparison, a post-layout simulation result with the non-ideal buffer mentioned above is also included in Fig. 4-7. Although the pre-layout simulation is close to the post-layout simulation result except for high frequency band, the post-layout one is more suitable for a realistic comparison. As for the reasons described above, the measured multiplier -3dB bandwidth is 5.3 GHz, which is less than 7.1 GHz obtained in the post layout simulation.

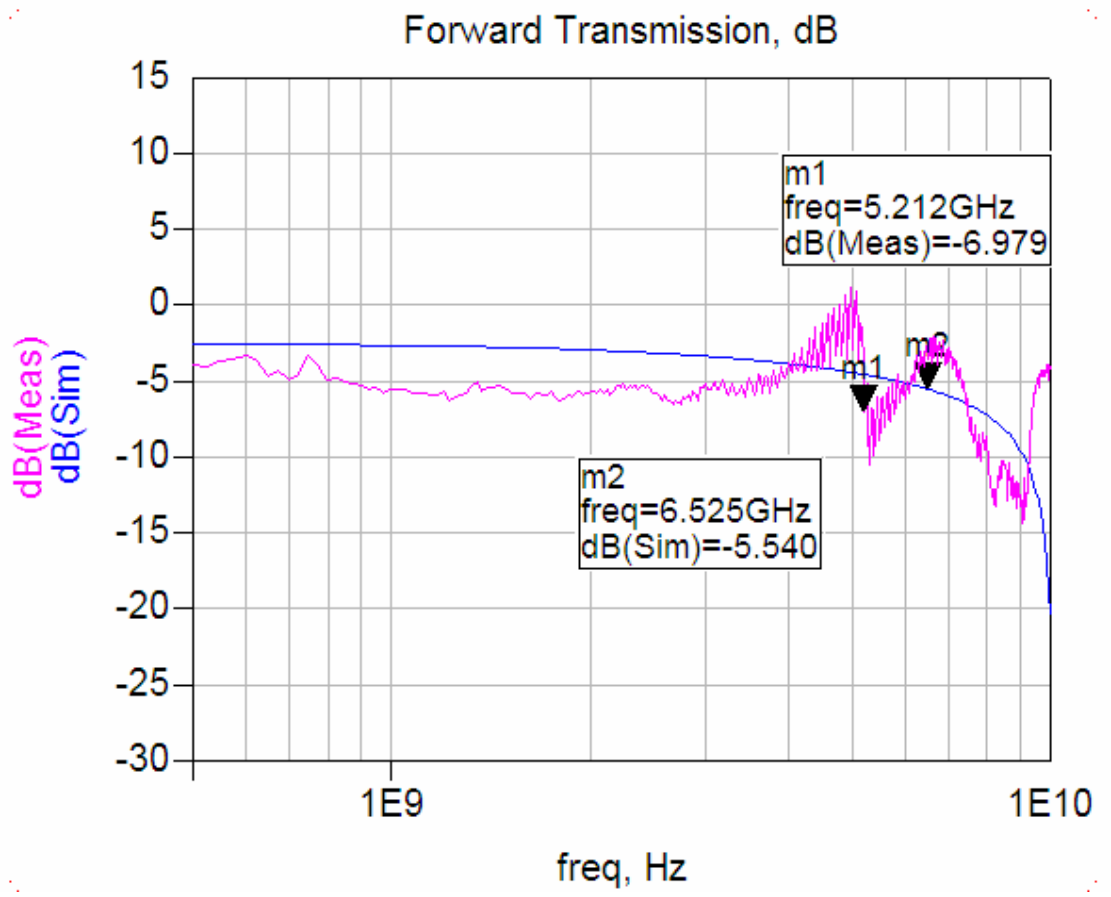


Fig. 4-7 Measured multiplier frequency response compared with the post-layout simulation result

The oscillatory behavior of the frequency response at high frequency is believed to be caused by the transmission line and measurement setup. A smooth curve of the measured results is drawn in Fig. 4-8 to remove the oscillation points with 4-th order degree polynomial curve fitting. From Fig. 4-8, the post layout simulation result shows a similar response to the measured one, except that the gain is about 3-dB higher. The gain, which is 20dB lower than the result in Fig. 4-7, is due to the insertion of additional buffer for measurement, which causes the DC gain of the multiplier drop.

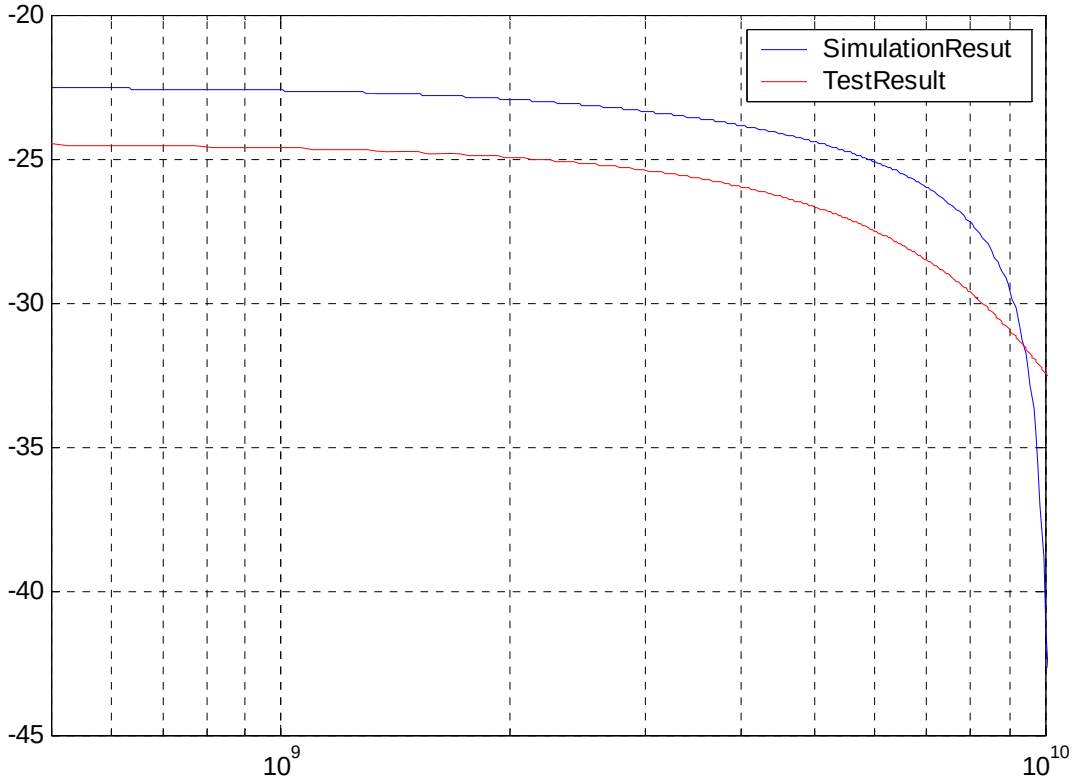


Fig. 4-8 Comparison of simulation and measured result after curve fitting.

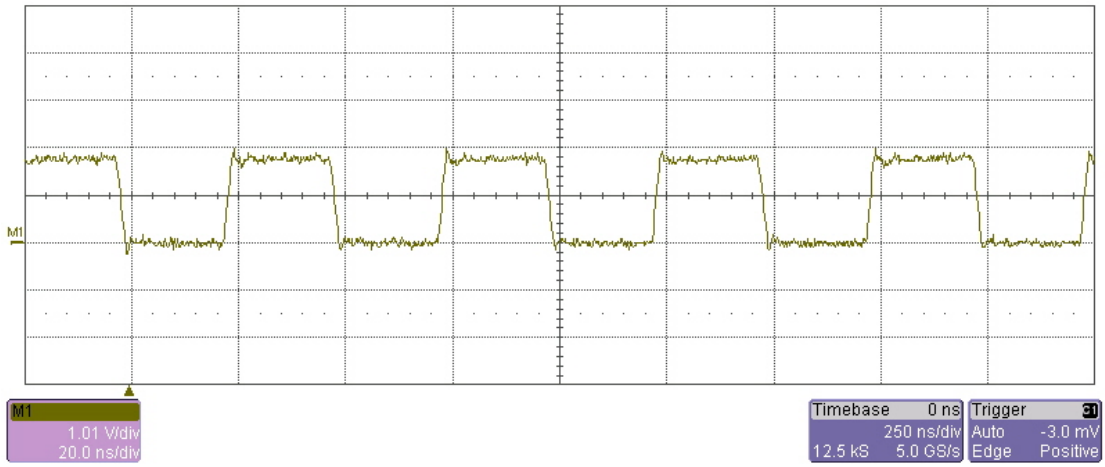
The performance of this wideband multiplier is summarized in Table 4-2.

PARAMETER	VALUE
Technology	0.18 um
Voltage Supply	1.8 V
Bandwidth	
(3-dB without the load)	10 GHz
(3-dB with the output buffer)	7 GHz
(3-dB in measurement)	5.3 GHz
Voltage Conversion Gain	14 dB
Linear input range	± 0.15 V
Power Consumption	3.6 mW
Die Area	0.2 x 0.24 mm^2

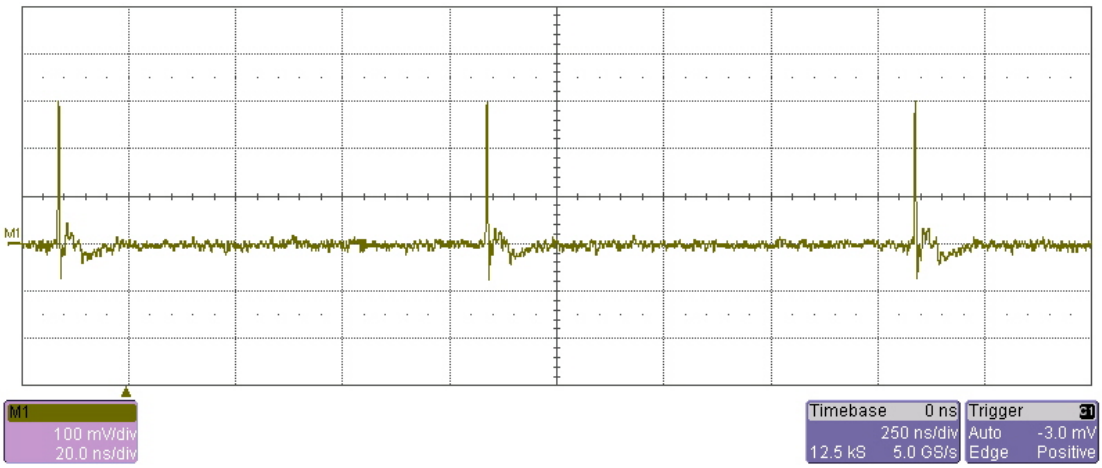
Table 4-2 Performance of the multiplier.

B. Passive multiplier

Fig. 4-9 shows the multiplication of one square wave signal and a UWB pulse signal. The data are captured from the digital oscilloscope (Leroy WaveRunner 6100A). The upper two plots are input signals, which are synchronized in phase. The lowest one is the output signal of the passive multiplier, which lags the input signal due to the time offset of different channel used in the oscilloscope. All these three plots have a time base of 250ns/div. A 2-MHz square wave signal is used to control the switches. The other input signal UWB narrow pulse with frequency of 1 MHz. Both input signals are differential. The measurement result shows that the width of the output pulse is nearly the same as that of the input one, which shows the passive multiplier has sufficient bandwidth. However, from the vertical voltage value of each plot, we can see that a 300mV pulse signal will reduce to 40mV after multiplication. Therefore, this is an significant drawback of the passive multiplier, which limits its application in the UWB receiver design.



(a)



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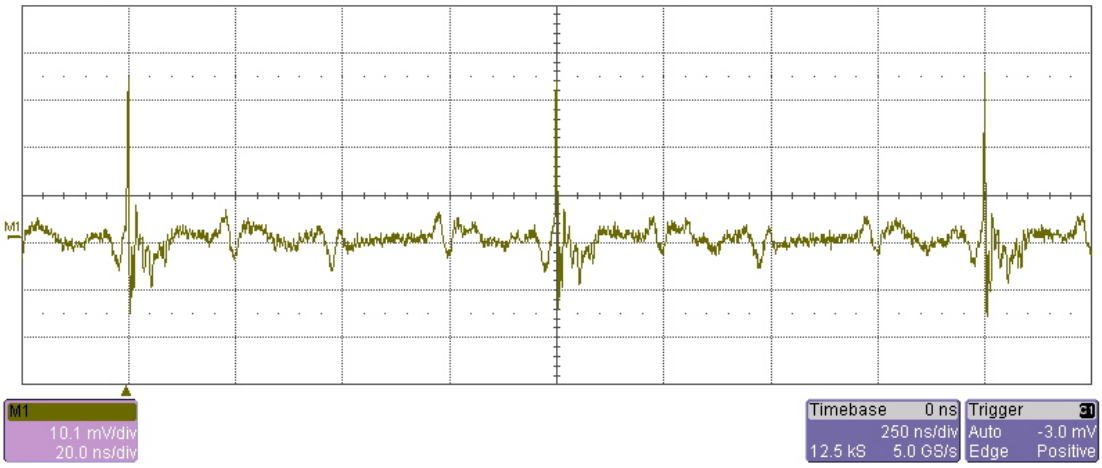

(c)

Fig. 4-9 Output waveform of passive multiplier with one UWB- pulse input signal. (a) input 2-MHz square wave signal (b) input UWB-pulse signal with 1MHz PRF (c) output signal of the passive multiplier

4.2.2 Integrator

The integrator is tested with the ideal pulse and the result is given in Fig. 4-10. The period of the input is 20ns and duty circle 25%. The square wave on the top is the control signal that starts the integration. The bottom is the output signal from the integrator under test, which indicates the correct integrated output. In order to avoid overlaps between control integrating signal and reset signal, we increased the time interval of those two control pulses from ideal 0ns to 5ns. Fig. 4-10 shows that the

pulse signal is correctly integrated. The slight delay between the real output pulse and the signal displayed in the oscilloscope is due to the 1-meter transmission line between the output signal to the input of the oscilloscope.

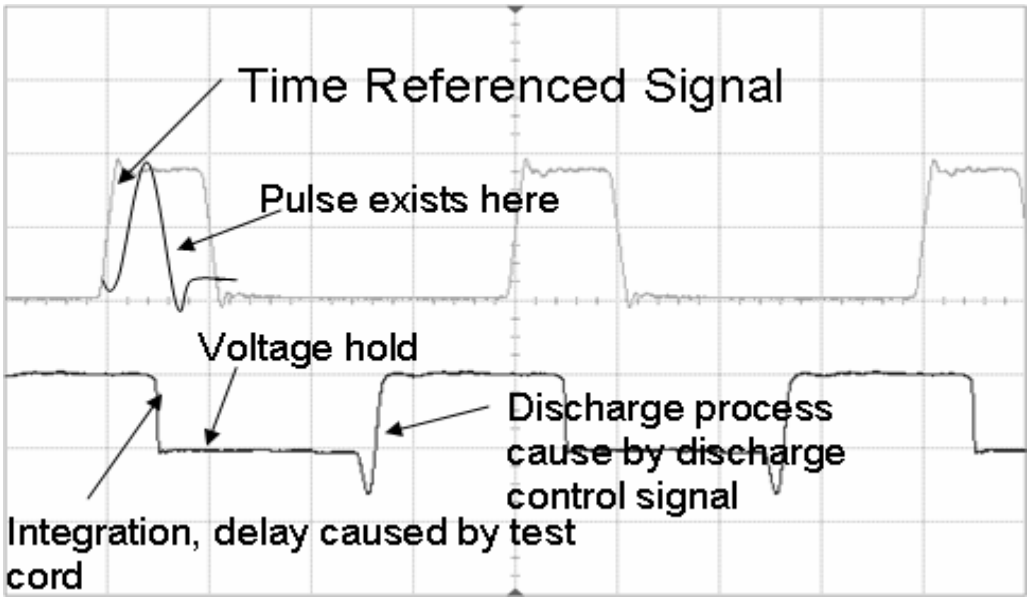

Fig. 4-10 Measured result of integrator with pulse signal.

4.2.3 Correlator

The test result of the complete correlator (multiplier + integrator) is shown in Fig. 4-11. The input signals are two synchronized monocycle pulses with the same repetition frequency of 50MHz. The control signals of the integrator are adjusted to match the operation of the multiplier. The test result is measured with a 50Ω load from the instrument. Since there is an on-chip buffer added to the output of the correlator, this configuration only reduces the output signal amplitude to 30% compared with a high impedance load. The falling edge in the output waveform indicates the integration of the multiplier output. The integrated output voltage is held for a period of time before the integrator is discharged. The frequency of the input

pulse is up to 50MHz which is limited by the pulse generator. The power consumption of the correlator is 13.6 mW under a single 1.8-V supply.

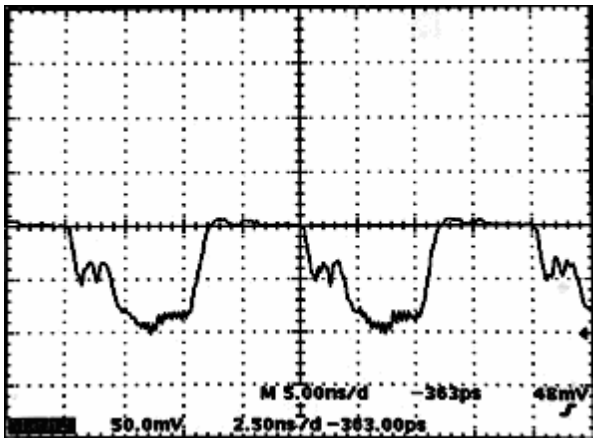

Fig. 4-11 Output waveform of correlator with two UWB- pulse input signal.

The reason that measured correlator works at 50MHz is because of the limitation of the maximum frequency of the pulse generator, which is 100MHz. If 100MHz are used as input signals, the input pulses will have many sub harmonic components, which are correlated to the output by the correlator. Therefore, the waveform of the correlated result has many high order harmonics, which cannot be sampled by the oscilloscope. According to UWB specification, there are variable rate of data communication from 28M, 55M, 110M to 1320M bit/sec. Therefore the designed correlator is still suitable for UWB application.

CHAPTER 5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

The design of an analog correlator for UWB transceiver has been described. The correlator consists of a wideband multiplier and an integrator. The structure of the multiplier is based on programmable linear transconductors. A pole-zero cancellation technique is proposed to enhance the bandwidth. A simple analytical expression for determining the inductance value according to the parameters extracted from the models simplifies the optimization process in the design. The simulation has shown that the multiplier has a flat frequency response up to 10GHz without the load. The wide bandwidth is achieved by canceling the dominant pole at the internal node with the zero introduced by the gain boasting inductor at the output. This has been proved in the simulation which shows that the bandwidth can be increased as much as 5 times. The multiplier is operated under a 1.8-V supply and suitable for implementing the correlator in UWB transceivers. A high speed integrator was designed and analyzed based on Nauta's inverter transconductor. Such an integrator has a feature of high DC gain (over 30dB) and a long holding time.

The wideband CMOS time-integrating correlator is fabricated in a 0.18um CMOS technology. The correlator chip has been tested with a 0.2-ns simulated UWB pulse signal and produces a correctly detected output signal. The correlator consumes 13.6mW under a 1.8-V single supply.

5.2 Future Work

Since testing of the circuits operating at high frequency is restrict to the unpredicted parasitic parameters caused by transmission lines as a connection from inside chip to outside device, an on-wafer testing is preferred to minimize the number of output pins. However, a differential structure is proved to have better performance to cancel even order effects and bias condition than single wing. Thus, they are very commonly used in high frequency design. This means more interface connectors are needed, which makes it impossible to conduct on-wafer measurement. A more accurate scheme, in which a differential on-chip balun is designed for both input and output, is required to minimize the high frequency effects caused by additional measurement equipments and components. Also a stable and accurate DC voltage bias circuit can be inserted to simplify the outside testing circuits in the future design.

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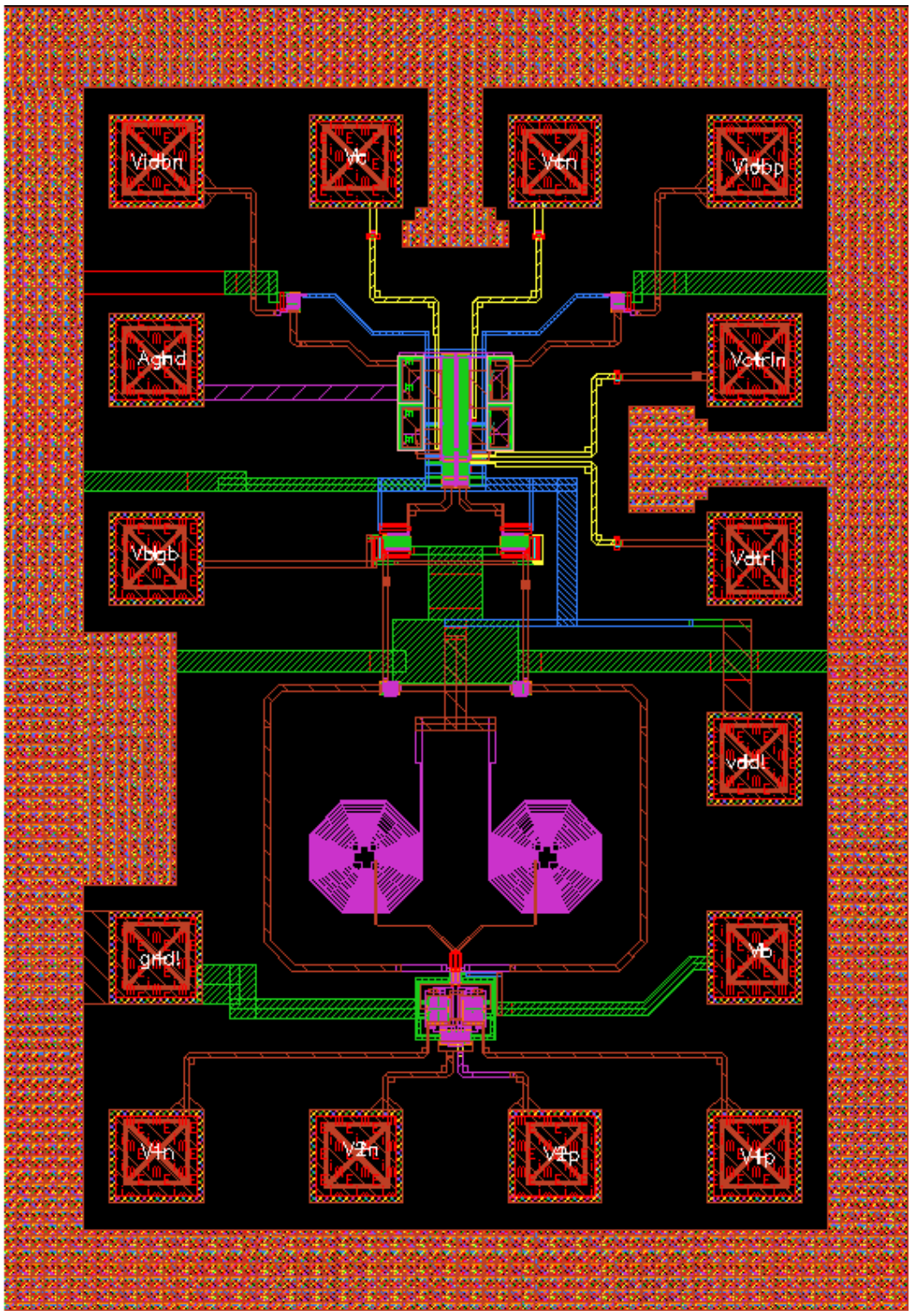
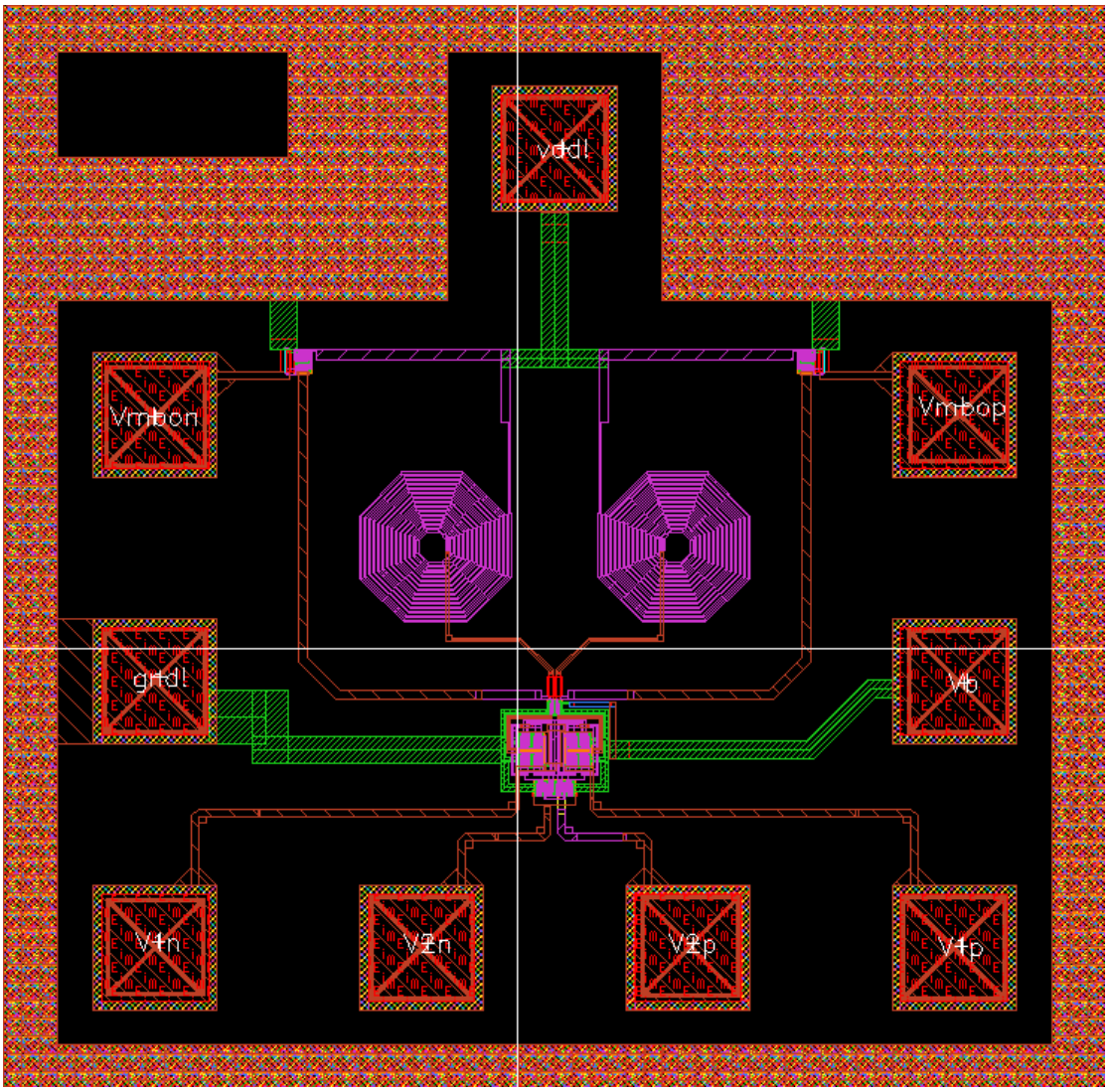
APPENDIX A

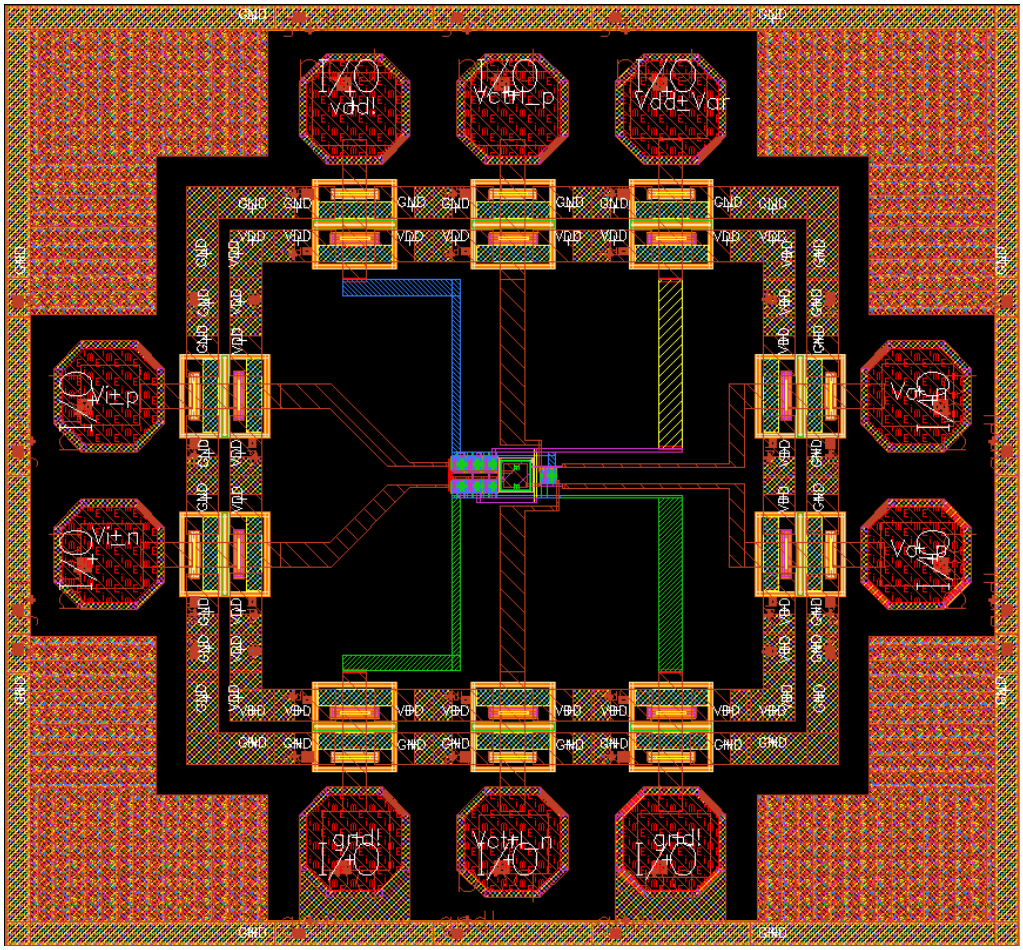
Layout of the Time-Integrating Correlator



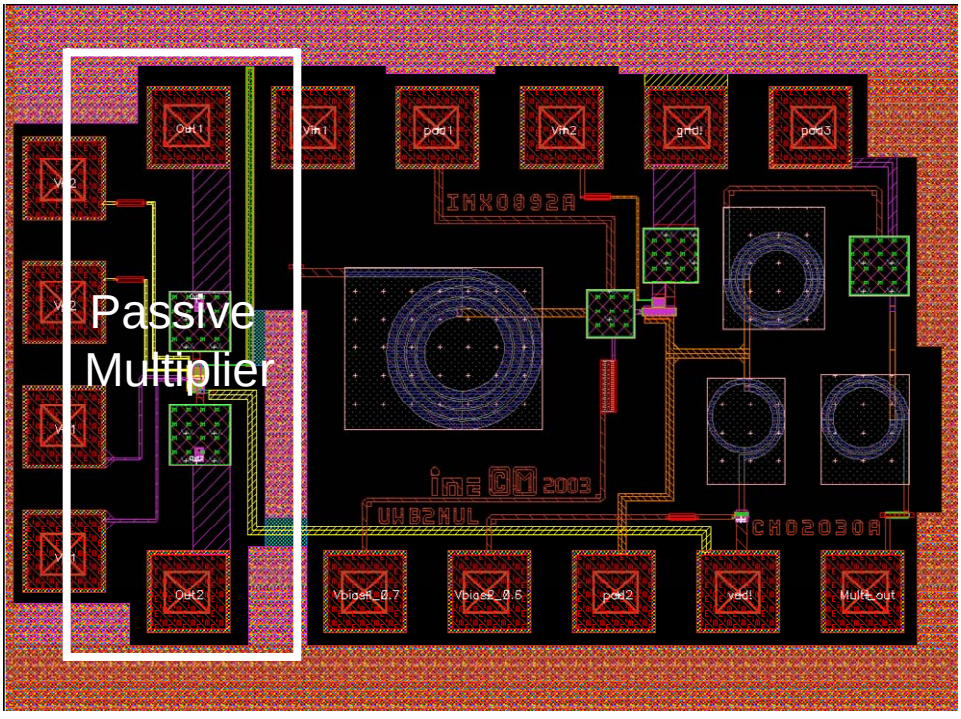
Layout of the Wideband Multiplier



Layout of the Integrator – Nauta's Version

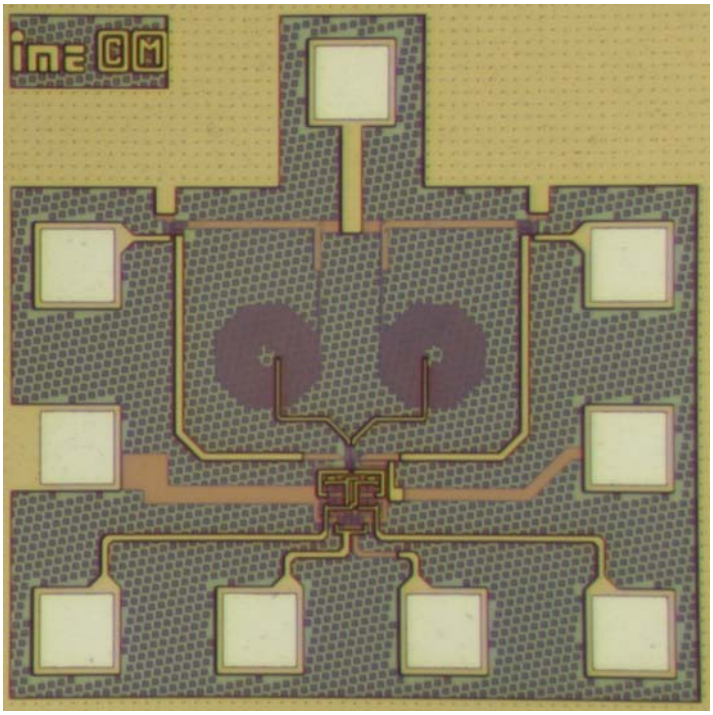


Layout of the Passive Multiplier

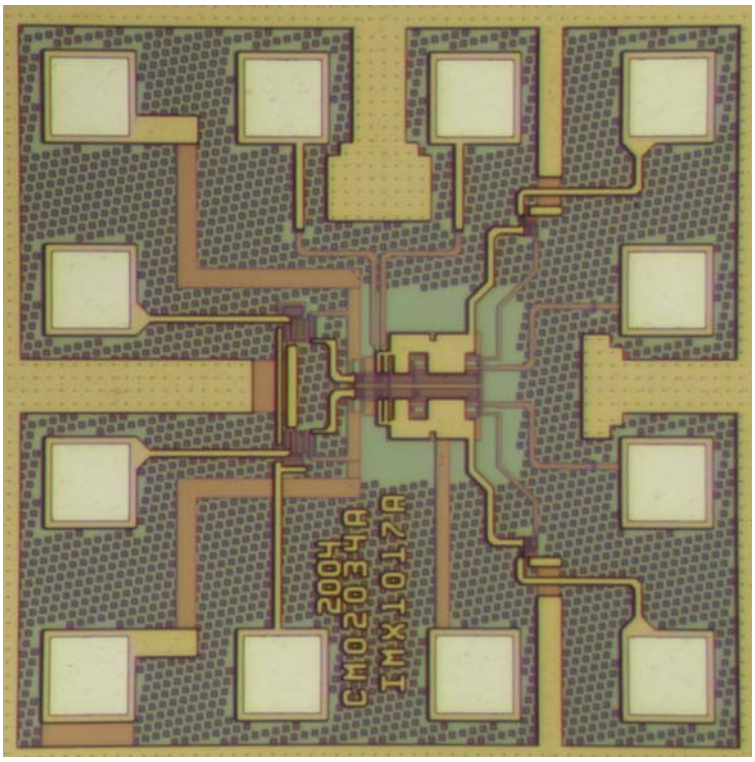


APPENDIX B

Die Photo of Active Multiplier



Die Photo of Integrator



Die Photo of Inductor Test Structure