ALTERNATIVE GATE DIELECTRICS AND APPLICATION IN NANOCRYSTAL MEMORY

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Summary

Nanocrystal memory has attracted much attention because it has better scalability than the conventional floating gate Flash memory. In this work, the performance of germanium (Ge) nanocrystal memory structures, employing high dielectric constant (high-κ) materials to replace the tunnel oxide and capping oxide (control oxide) layers, was investigated. It was found that faster charging rate and better charge retention performance could be obtained with a high-κ tunnel dielectric layer of equivalent oxide thickness (EOT) to that of silicon dioxide. Even at an EOT of 1.9 nm, the high-κ layer is still physically thick enough to prevent Ge penetration into the substrate during high temperature annealing. If Ge penetration were to occur, Ge nanocrystals will not be able to form and the device will not show any charge storage effect. The replacement of the capping oxide layer with a high-κ material of similar physical thickness as that of a silicon dioxide capping layer will result in better gate electric field coupling. The effect of gate electric field coupling on the conductance-voltage (G-V) characteristics of different trilayer nanocrystal memory structures was also investigated. It was found that the distinctive G-V characteristics due to nanocrystals could be separated and identified from the interface traps provided the memory structure has sufficiently high electric field coupling from the gate applied voltage. A method for calculating the density of nanocrystals based on the G-V data was also discussed. Finally, investigation of trap energy levels in Ge nanocrystal memory structures and their effect on the device charging and discharging kinetics were also carried out by monitoring the transient drain current characteristics.

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Chapter 1: Introduction

1.1 Background

The floating gate (FG) memory device is the most widely used design in nonvolatile semiconductor memory (NVSM) implementation. However, there are numerous difficulties in the scaling down of the FG NVSM device, especially decreasing the tunnel oxide thickness to meet conflicting operational requirements. On one hand, the tunnel oxide has to be thin to allow low-voltage, fast program and erase. On the other hand, the tunnel oxide has to be thick to provide superior isolation under charge retention condition in order to maintain information integrity of up to 10 years. As a result of these contradicting demands, Flash memory manufacturers have settled on a compromise for tunnel oxide thickness with values in the range 9 to 11 nm [1].

Storing charge on a single node (i.e. the FG node) makes the conventional Flash memory structure particularly prone to failure of the FG isolation (i.e., tunnel oxide). One weak spot in the tunnel oxide is sufficient to create a fatal discharge path, compromising long-term nonvolatility. One way to overcome this is to rely on distributed charge storage with charge storage nodes isolated from each other. The most popular types are polysilicon-oxide-nitride-oxide-silicon (SONOS) or nanocrystal memories. The main disadvantage for SONOS memory devices is that the traps are distributed randomly in the nitride charge storage layer [2]-[3]. Nanocrystal NVM offers greater control of the charge storage spatial location, especially if a templated self assembly method is used to order the nanocrystals [4].

In a nanocrystal NVM device, the charge is not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots, typically made of semiconductor material [5]–[59]. Each dot will typically store only a single charge; collectively the charges stored in these dots control the channel-conductivity of the memory transistor. Compared to FG NVM, nanocrystal charge-storage offers several advantages; the main one being the potential to use a thinner tunnel oxide without sacrificing nonvolatility. Hence this will lead to lower operating voltages and higher program and erase speeds. Due to the distributed nature of charge storage, the charge storage device is more robust and fault tolerant to charge loss. This will also lead to improved endurance write/erase performance as compared to FG NVM.

1.2 Motivation

A nanocrystal memory device typically consists of three layers of gate material deposited on the Si-substrate. These layers are namely, the tunnel oxide layer, the germanium (Ge) nanocrystal (charge storage) layer and the capping oxide layer. Although a thin tunnel oxide is highly-desirable for fast programming speed, one inherent issue would be the penetration of Ge through the thin tunnel oxide into the silicon (Si) substrate during high temperature annealing to form the Ge nanocrystals, resulting in a complete loss of charge storage capability [10]. This penetration issue imposes a lower bound (~5nm) to the scaling of the tunnel dielectric layer [11].

In this project, we intend to address the Ge penetration issue as well as to further reduce the tunnel dielectric electrical thickness by using an alternative material with a

higher permittivity (κ) value. The high-κ material is able to provide a sufficiently thick physical layer to prevent the Ge from penetrating through the tunnel dielectric while at the same time, providing a much lower equivalent oxide thickness (EOT) for device operation.

In order to obtain a fast programming speed, the electric field across the tunnel oxide needs to be high so that charge carriers can tunnel rapidly from the Si substrate into the Ge nanocrystals. This high electric field could be achieved by simply applying a high voltage at the gate electrode but this approach is counter to low voltage operation. Application of a high gate voltage is also likely to induce unnecessary degradation on the tunnel oxide during Fowler-Nordheim tunneling of the charge carriers. Alternatively, the high electric field across the tunnel oxide could be achieved by decreasing the Ge layer thickness (i.e., nanocrystal size) or the capping oxide thickness. As there is a limit to decreasing the Ge layer thickness, a more viable approach would hence be to decrease the capping oxide thickness. Similar to the tunnel dielectric layer, there also exists a lower bound to the scaling of the capping oxide thickness as the Ge could out-diffuse from the middle Ge layer into the environment during the high temperature annealing to form the Ge nanocrystals if the capping oxide is too thin. It would be interesting to determine the lower bound limit for the SiO_2 cap layer thickness to ensure proper device functioning as well as to further reduce this layer electrically by replacing it with a high-κ material. A high-κ capping oxide layer would also result in better electric field coupling of the gate voltage to the tunnel oxide.

1.3 Research Objectives

The aim of this research is to explore the possibility of replacing the silicon dioxide (SiO_2) components (tunnel oxide layer and capping layer) in a trilayer gate structure nanocrystal memory device with a high-κ material. The performance of the device with the high-κ layers will be compared with the control device with conventional SiO_2 layers. To obtain a better understanding of the role of each replaced layer and its effect on device performance, the individual layers will be changed one at a time and its characteristics studied.

During the initial phase of this project, the suitability of several high-κ materials (e.g., zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2) and hafnium aluminum oxide (HfAlO)) as a replacement material for SiO_2 will first be investigated before deciding on a suitable material. Charge storage capability, charging and discharging speeds as well as charge retention studies will be carried out and compared on nanocrystal capacitor memory devices with 5nm (EOT) of high-κ tunnel dielectric and on device with the same thickness (5nm) of conventional RTO.

As the conventional RTO thickness has a lower limit at 5nm, below which Ge penetration would result in complete loss of charge storage capability, we attempt to address this penetration issue and also further reduce this 5nm EOT limit by replacing the conventional RTO with a suitable high-κ material.

As the down-scaling of the capping layer (physical and electrical thickness) is beneficial to the programming/erasing speed of the device, the possibility of reducing the thickness of 50nm SiO_2 cap layer [8] -[11], as well as replacing this layer with a suitable high-κ material would also be investigated.

Electrical characterizations such as capacitance–voltage (C-V), current-voltage (I-V) and charge retention time studies will be performed on these devices. The more sensitive conductance-voltage (G-V) measurement method will also be used to characterize the devices to obtain further insights into the nanocrystal memory device operation. A methodology for extracting the nanocrystal density based on the G-V data will be discussed.

Upon the fabrication of the nanocrystal memory capacitors, a full-scale nanocrystal memory transistor with high-κ as the tunnel dielectric material will be fabricated and characterized. An experiment for extraction of the nanocrystal trap energy level (E-trap) based on the study of drain current (during the discharging of trapped charge) with respect to temperature will be carried out [12]. An alternative method for extraction of E-trap levels will be proposed and discussed. Finally, the possibility of engineering the E-trap levels in the Ge nanocrystals by varying the surrounding matrix will be investigated.

1.4 Organization of Thesis

The thesis is arranged in a way to address the objectives set out for this research. Chapter 2 is devoted to cover the key findings in the literature survey on high-κ materials as well as provide an overview of the theory of FG flash memory and nanocrystal memory structures. Chapter 3 describes the work carried out on fabrication and characterization of several high-κ materials, namely ZrO_2, HfO_2 and HfAlO, to identify suitable high-κ materials for the nanocrystal memory. Chapter 4 examines the performance of the nanocrystal memory device with high-κ HfO_2 and HfAlO materials as

the tunnel dielectric material. Chapter 5 studies the possibility of employing the high-κ HfAlO material as the capping layer for enhanced electric field coupling. The results of conductance-voltage (G-V) measurements performed on the nanocrystal memory capacitor devices will be shown in this chapter. A method for estimating the nanocrystal density based on the G-V data will also be discussed. Chapter 6 describes the electrical characterization of the transistor-based nanocrystal memory structures with high-κ HfAlO material as the tunnel dielectric. The extraction of the nanocrystal trap energy level based on the study of drain current (during the discharging of trapped charge) with respect to temperature will be presented in this chapter. An alternative method to extract the energy trap level will be compared and discussed.

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Chapter 2: Literature Review on High Dielectric Constant (High-κ) Materials and Nanocrystal Memory

In this chapter, the literature reviews on high dielectric constant (high-κ) materials will first be presented, followed by an overview of current memory devices and their limitations during device downscaling. From the literature reviews, the nanocrystal memory device seems to offer a promising solution to address the issues faced by current memory devices. To further enhance the performance of nanocrystal memory devices, the possibility of utilizing high-κ materials to replace the conventional SiO_2 components in such a device will be discussed.

2.1 Literature Review on High Dielectric Constant (high-κ) Materials

Silicon dioxide (SiO_2) has been used as the main-stream gate dielectric material in Metal-Insulator-Silicon (MIS) devices for many years. However limitations start to arise with device downscaling. In this section, some of the issues experienced by SiO_2 during device downscaling will be mentioned and an explanation on how a high dielectric constant (high-κ) material could provide a solution to these issues will be provided. Some considerations to look into for the choice of an ideal alternative gate dielectric material will also be highlighted.

2.1.1 Limitations of Silicon Dioxide (SiO_2) as Gate Dielectric Material

In recent years, the gate oxide has been aggressively scaled as part of device miniaturization. In the very near future, the leakage current will increase to unacceptably high level and the boron penetration problem will be severely aggravated. In addition, it

will be more difficult to control the uniformity and reproducibility of ultra-thin oxide growth processes. The extrapolated gate oxide scaling targets based on published data from recent Intel technologies [1] predicts that by the year 2008, the physical gate oxide thickness needs to be as thin as 8Å at the 60nm technology node and the solution to this problem is yet unknown. The technology node refers to the smallest polysilicon (poly-Si) gate length which can be defined by photolithography and roughly corresponds to the minimum channel length for a given process technology. A more complete list of projected transistor parameters is given in Table 2.1. The predictions are based on extrapolations of published state-of-the-art 180nm technologies assuming channel length, supply voltage, and gate oxide thickness scaling factors of 0.7, 0.8, and 0.8, respectively [2]-[4]. These projections, representative of the current targets for high-performance logic technology, aggressively outpace those compiled earlier in the year 2000 update of the International Technology Roadmap for Semiconductors (ITRS).

Table 2.1: List of projected transistor parameter requirements for future devices [2]-[4].

Generation (nm)	**180**	**130**	**100**	**70**	**Scaling Factor**
L_{gate} (nm)	100	70	50	35	0.7x
V_{dd} (V)	1.5	1.2	1.0	0.8	0.8x
T_{ox}, electrical (Å)	31	25	20	16	0.8x
T_{ox}, physical (Å)	21	15	10	6	0.8x
I_{off} at 25°C (nA/µm)	20	40	80	160	2x

Year **Technology Node**	**1999** **180nm**	**2001** **130nm**	**2004** **90nm**	**2008** **60nm**	**2011** **40nm**	**2014** **30nm**
L_{gate} (nm)	120	90	70	45	32	22
T_{ox}, physical (Å)	19-25	15-19	12-15	8-12	6-8	5-6
Gate leakage at 100°C (nA/µm)	7	10	16	40	80	160
				No solutions yet		

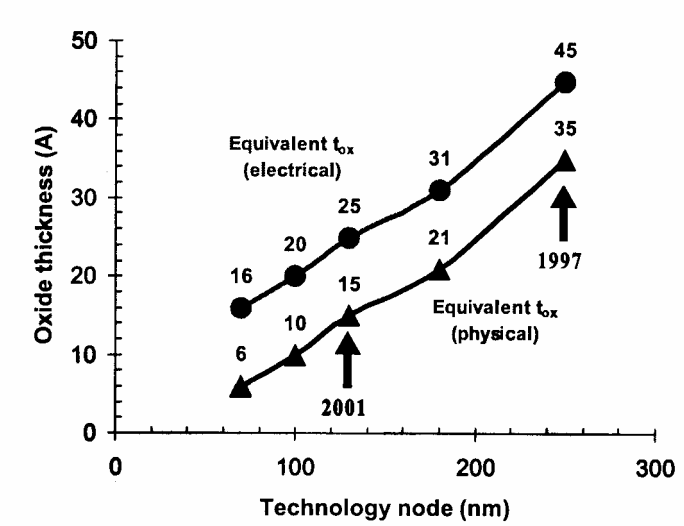

Figure 2.1: Extrapolated gate oxide scaling trend for recent CMOS technologies [2]-[4].

The two data sets in Fig. 2.1 refer to the equivalent electrical and physical thickness of the gate oxide. The equivalent oxide thickness (EOT) refers to how thin a pure silicon dioxide (SiO_2) layer would need to be in order to meet the gate capacitance requirements of a given technology. In a modern MOSFET device, the gate oxide could behave electrically as if it were 8-10Å thicker than its physical thickness due to polysilicon depletion and quantum mechanical effects. From Fig. 2.1, it is clear that the physical thickness of the gate oxide is rapidly approaching atomic dimensions. The 250nm technology, which entered volume production in 1997, used a SiO_2 layer with approximately 40Å physical t_{ox}, corresponding to approximately 20 monolayers of SiO_2. In contrast, the 100nm and 70nm technologies, scheduled for production in the next 5 to 10 years, will require gate capacitance values achievable only with SiO_2 layers as thin as 10Å and 7Å, respectively, to guarantee proper device operation. A 10Å film consists of only three to four monolayers of SiO_2.

2.1.3 Employment of High Dielectric Constant Material as a Solution to Limitations of Silicon Dioxide (SiO_2)

An approach to address the limitations of the conventional SiO_2 gate insulator is to employ a physically thicker, higher permittivity gate dielectric in place of SiO_2, and/or silicon oxynitride, to meet the same gate capacitance requirements. In the following paragraphs, a brief explanation on the operation of the MOSFET followed by how the high dielectric constant material could be employed in such a device will be given.

A MOSFET ideally acts as a three-terminal switch, either connecting or isolating the drain (D) and source (S) terminals based on the voltage applied to the controlling gate (G) terminal. In practice, this switching action is achieved through the use of a gate capacitor. Depending on the polarity of the voltage applied to the gate terminal, either positive or negative charge is induced in the channel region. The channel charge either connects or isolates the drain and source nodes depending on the type of carriers contained in the channel region.

The operation of the MOSFET depends critically on several properties of the gate dielectric material SiO_2. The wide insulating bandgap ($E_g \sim 9eV$) of SiO_2 electrically isolates charges in the gate and channel regions, so that the controlling gate terminal does not interfere with the flow of the current in the channel regions. Also, the interface between SiO_2 and the underlying Si substrate is electrically of very high quality, allowing electric field originating at the gate electrode to penetrate into the channel region to accumulate or invert the surface charge. Prior to the development of the Si/SiO_2 system, attempts to realize a field-effect transistor (FET) were hampered by the abundance of electrically active defects at the dielectric/semiconductor interface.

The amount of charge (Q) induced in the channel region is given by the product of the gate oxide capacitance per unit area (C_{ox}) and the voltage drop across the gate capacitor (V),

$$Q = C_{ox}V \tag{2.1}$$

Since C_{ox} can be modeled as a parallel-plate capacitor, its value is given by

$$C_{ox} = \frac{k_{ox}\varepsilon_o}{t_{ox}} \tag{2.2}$$

where k_{ox} is the relative dielectric constant, ε_o is the permittivity of free space, and t_{ox} is the physical thickness of the dielectric material. Based on these relations, the drain-source current for a long-channel MOSFET operating in the saturation region can be expressed as

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \tag{2.3}$$

where μ is the channel mobility, W and L are width and length of the channel region respectively. V_{gs} is the gate-source potential, and V_t is the threshold voltage. Equations (2.2) and (2.3) reveal that reducing the lateral (L) and vertical (t_{ox}) dimensions of the device increases the current flow between the drain and source. Intuitively, this is because reducing t_{ox} increases C_{ox} and hence the amount of channel charge, and reducing L decreases the distance the channel charge must travel to conduct a current. Reducing the gate oxide thickness (t_{ox}) along with the channel length (L) also helps to maintain the gate potential to modulate more channel charge and is especially important as the supply voltage scales down. From equation (2.2), it can also be seen that the gate oxide

capacitance (and hence the drain current) can be increased by reducing the oxide thickness or by using a gate dielectric material with a higher dielectric constant (κ) value. The larger capacitance value that could be obtained from a high-κ material is given by equation (2.4) as follows:

$$C_{high-k} = \frac{k_{high-k}\varepsilon_0}{t_{high-k}} \tag{2.4}$$

where $k_{high-\kappa}$ and $t_{high-\kappa}$ are the relative dielectric constant and physical thickness of the high-κ material.

In this way, the introduction of a high-κ material is able to ensure a reasonable flow of drain current, with minimal direct tunneling gate current leakage, as the gate oxide thickness reduces. This approach using the high-κ material to replace conventional SiO_2 as the gate insulator seems to provide a viable solution to satisfy future technological needs.

2.1.4 Criteria for Selection of Alternative Gate Dielectrics and Potential Candidates

In the event that an alternative gate dielectric were to be used, other issues concerning the gate material and processing compatibility may arise. Therefore, research on the gate stack as a whole, i.e., considering the high-κ dielectric and the gate material together with process integration issues, is critical to the continuation of device scaling. The required properties of the high-κ materials can be summarized as follows [5]-[8]:

(1) Thermodynamically stable in direct contact with silicon and poly-Si for single layer dielectrics, or in multi-layer dielectric stack on Si surface.

(2) Relative dielectric constant larger than 3.9.

(3) Low diffusion constant for dopant atoms in poly-Si.

(4) Large bandgap with > 1eV tunneling barrier for both electron and hole carriers (conduction and valence band offsets).

(5) Low interface trap defect density, $D_{it} \sim 10^{10} cm^{-2} eV^{-1}$, that is comparable to Si/SiO_2 system.

(6) Low trap density within the bulk oxide layer, i.e., low oxide fixed charge, oxide trapped charge, and mobile ionic charge defects.

(7) Preferable to have a stable amorphous phase to avoid grain boundary leakage problem

(8) Minimal change from existing oxide fabrication process.

The properties of some potential high-κ dielectric materials are summarized in Table 2.2.

Table 2.2: Characteristics and properties of some potential high-κ dielectric material. SiO_2 is also listed for comparison [5].

High-κ Dielectric	Relative Dielectric constant, κ	Bandgap, E_g (eV)	Conduction band offset to Si, ΔE_c(eV)	Crystal structure
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal, cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetragonal (rutile, anatase)
HfO_2	25	5.7	1.5	Monoclinic, tetragonal, cubic
ZrO_2	25	7.8	1.4	Monoclinic, tetragonal, cubic

Due to the reason that one can only obtain either large bandgap or permittivity, but not both, a dielectric with relative permittivity κ > 25 is not necessarily required to replace SiO_2. The more relevant consideration is whether the desired device performance and reliability can be obtained without producing unacceptable current leakage. The guideline is to identify a dielectric that provides only a moderate increase in κ, but is able

to produce a sufficiently large tunneling barrier and high-quality interface to Si. For example, if a single layer could be used, even a material with a κ value of 12 could result in a physical dielectric thickness of 35-50Å, with an equivalent oxide thickness (EOT) of 11-16Å, that meets the requirements for 0.1μm CMOS and beyond. By comparing hafnium dioxide (HfO_2) and zirconium dioxide (ZrO_2) with SiO_2, HfO_2 and ZrO_2 seem to have a slight edge over the rest, because the materials have a relatively high κ value of 25 and a large bandgap of 5.7-7.8eV. However, the effects of leakage would need to be considered, as the conduction band offset of HfO_2 and ZrO_2 (~1.5eV) is much lower than that of SiO_2 (3.2eV) [8].

Many high-κ materials have poor stability when in contact with the Si surfaces, these include Ta_2O_5 [9]-[12] and TiO_2 [13]. They tend to react with Si to form an undesirable interfacial layer that will lower the overall EOT. These materials require a barrier layer to prevent the reaction at the surfaces. Those that are able to deposit on Si with good thermodynamic stability include ZrO_2, HfO_2, Y_2O_3, Al_2O_3 [14] and La_2O_3 [15]-[16]. SiO_2 is naturally grown on Si and has no stability problem on Si. Therefore, the new high-κ material must have a similar stability with Si.

From the literature survey, it has been found that the ZrO_2 [17] and HfO_2 [18]-[23] are the more promising candidates as alternative gate dielectric materials for the near term replacement of SiO_2.

2.2 Introduction to Current Nonvolatile Memory Devices and their Limitations

The first non-volatile memory was proposed by Kahng and Sze in 1967 [24]. In their work, the memory structure was made from a conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) with an embedded metal floating gate. This floating gate served as the storage site for electrons that were injected from the substrate across the tunnel oxide during the programming phase. Storage of these charges changed the threshold voltage of the MOSFET and allows the transistor to electrically alter between the "ON" and "OFF" states to represent the "0" and "1" logic.
In 1970, Frohman-Bentchkowsky demonstrated a floating polysilicon gate transistor. Electrons were injected by hot electron injection across a thick gate oxide to the floating polysilicon gate and removed via ultraviolet (UV) irradiation. This UV-erasable Electrically Programmable Read-Only Memory (EPROM) and its derivatives have steadily evolved to become a major memory technology.

The Floating Gate Tunnel Oxide (FLOTOX) technology proposed by Intel utilizes two transistors (a select transistor and a memory transistor) to achieve selective bits programming through Fowler-Nordheim (F-N) tunneling [25]. The cross sectional structure of a FLOTOX EEPROM cell is shown in Fig. 2.2. This consists of a floating gate transistor with a thin oxide grown over the drain region. The floating polysilicon gate is surrounded completely by high quality silicon dioxide, giving it superior data retention characteristics. Writing of the memory cell (i.e., increasing the threshold voltage) is accomplished by applying a positive voltage to the control gate with the source, drain and substrate grounded. Electrons are injected into the floating gate from

the drain through the thin tunnel oxide and this increases the threshold voltage, as measured on the control gate, to a more positive value. This causes the transistor not to conduct channel current during a subsequent read operation. Erasing of the memory cell is accomplished by applying a positive voltage to the drain with the source floating and the substrate and control gate grounded. Electrons are removed from the floating gate to the drain, reducing the threshold voltage and the channel current will flow during a subsequent read operation.

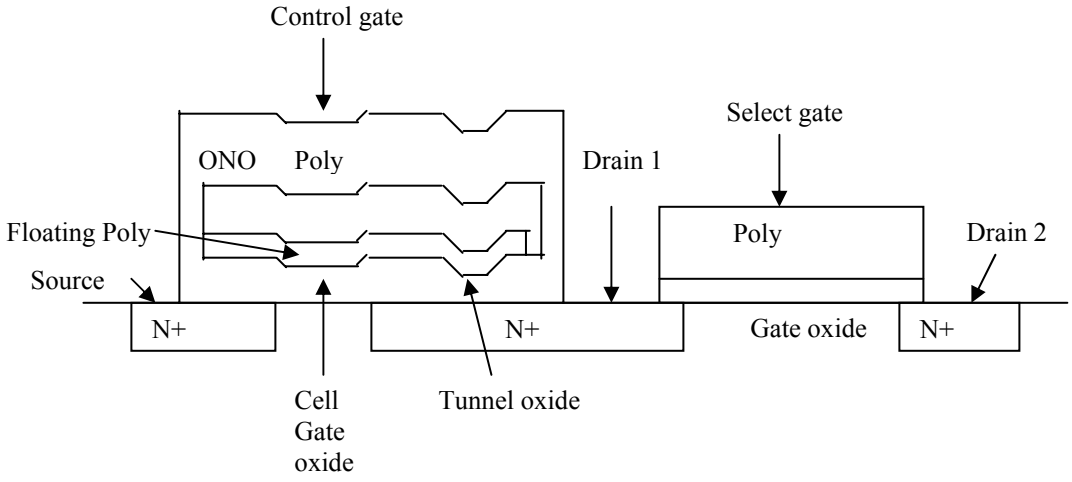

Figure 2.2: Schematic figure of a FLOTOX EEPROM cell.

Since the program and erase coupling conditions are different, they have different design considerations. Electron transfer typically occurs through the F-N tunneling mechanism under oxide electric fields higher than 10MV/cm. The bipolarity F-N tunneling write/erase method has been found to increase data retention time due to a decreasing gate oxide leakage current. The current-voltage (I-V) slope of tunneling is so steep that there is insignificant tunneling under normal read condition, in which the read

voltage is less than the F-N tunneling voltage. In order for the memory cell to function properly and to be addressed individually in an array, it has to be isolated by a select transistor as shown in Fig. 2.2. The floating gate Flash memory structure is similar to the FLOTOX EEPROM except for absence of the select transistor.

2.2.1 Basic Programming Mechanisms in Non-Volatile Memory Devices

In the floating gate Flash memory, the charge needed to program the device has to be injected into the floating gate. In order to change the charge or data content of the NVM, two major mechanisms have been shown to be viable: F-N tunneling through thin oxides (< 12 nm) [26] and channel hot-electron injection [27].

2.2.1.1 Programming by Fowler-Nordheim (F-N) Tunneling

One of the most common injection mechanisms used in NVMs is F-N tunneling. When a large voltage V_{cg} is applied at the control gate during programming, its energy band structure will be influenced as shown in Fig. 2.3.

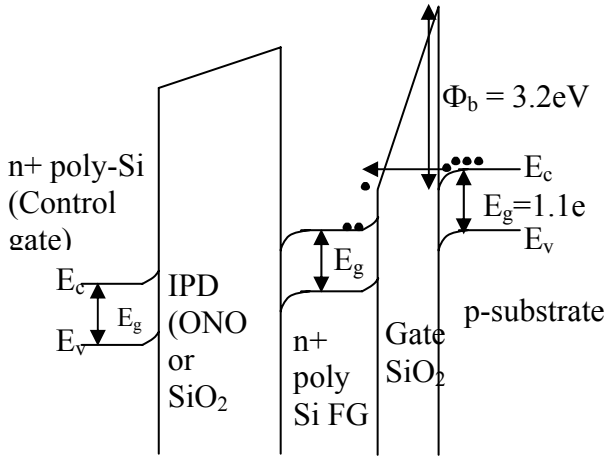

Figure 2.3: Energy band diagram of a floating gate memory during programming by F-N tunneling.

In Fig. 2.3, E_c and E_v are the conduction and valence bands respectively, E_g is the energy band gap (1.1eV for silicon), Φ_b is the Si-SiO_2 energy barrier (Φ_b is 3.2eV for electrons and 4.7eV for holes). The applied V_{cg} results in a thinner barrier for F-N tunneling of electrons from the substrate to the n+ poly-Si floating gate. The bending of the energy bands of the inter-polysilicon dielectric (IPD) and the gate oxide are different due to the thickness differences between them. The IPD, which can be SiO_2 or oxide-nitride-oxide (ONO), ranges from 25 nm to 45 nm while the gate oxide ranges from 5 nm to 12 nm. Figure 2.4 shows a cross-section of a NVM with electrons tunneling uniformly with V_{cg} at a positive potential while the source (V_s), the drain (V_d), and the substrate (V_{sub}) are at ground potential.

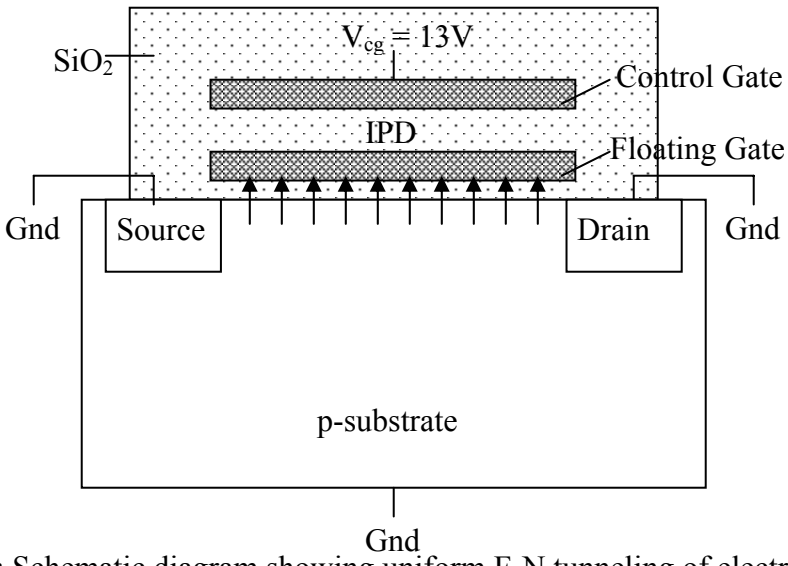

Figure 2.4: Schematic diagram showing uniform F-N tunneling of electrons from the substrate to the floating gate during programming of a Flash memory.

2.2.1.2 Programming by Hot-carrier Injection

Nonvolatile memories can also be programmed by hot-carrier injection (HCI). The method of programming is by hot-electron injection for n-channel NVMs built on p-substrates and by hot hole injection for p-channel NVMs built on n-substrates. Hot-hole injection is typically more difficult due to the larger $Si\text{-}SiO_2$ energy barrier of 4.7 eV for holes (as compared to 3.2eV for electrons), which is why most NVMs manufactured today are n-channel on p-substrates. The memory cell is programmed by charging the floating gate via the injection of hot electrons from the drain pinch-off region. The hot electrons get their energy from the voltage applied to the drain (V_d) of the memory cell. They are then accelerated by the lateral electric field (E_{lat}) along the channel into even higher fields surrounding the drain depletion region. Once these electrons gain sufficient energy, they surmount the energy barrier of 3.2 eV between the silicon substrate and the silicon dielectric layer or gate oxide. With positive V_d and channel voltages, electrons injected into the oxide of an n-channel memory cells return to the substrate unless a high positive V_{cg} is applied to pull the electrons toward the floating gate. The energy band structure for NVM programming by hot-electron injection is shown in Fig. 2.5.

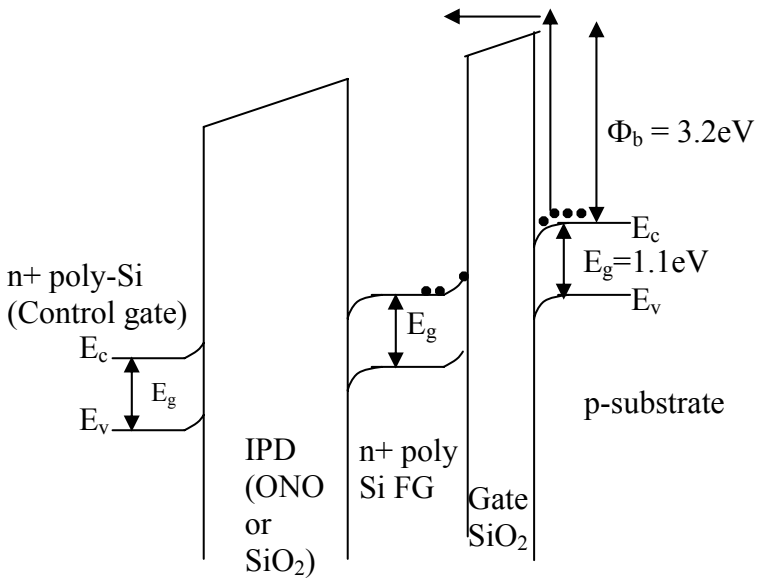

Figure 2.5: Energy band diagram of a floating gate memory during programming by hot-electron injection.

As the floating gate becomes fully charged, the gate current (I_g) is reduced to almost zero because the oxide electric field (E_{ox}) (in the beginning of the injection process, E_{ox} was attractive to the electrons) is now repulsive to the electrons. In general, to the first order, V_{cg} increases the charge on the floating gate while V_d affects the programming speed. Figure 2.6 shows a cross-section schematic of a NVM during hot-electron injection programming. V_{cg} and V_d are at positive potential of 15 V and 10 V, respectively, while V_s and V_{sub} are at ground potential.

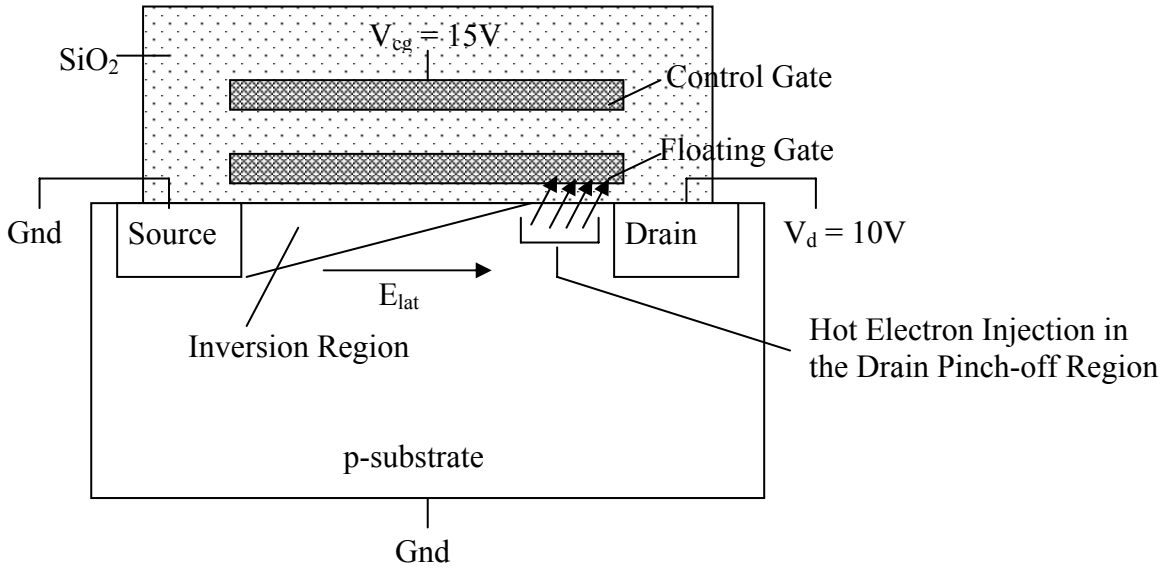

Figure 2.6: Schematic diagram showing hot-electron injection mechanism for programming in a NVM.

2.2.2 Basic Erasing Mechanisms Non-Volatile Memory Devices

In order to reprogram an NVM, it first has to be erased. This section will cover the erasing schemes commonly employed in the industry. The electrons that are injected into the floating gate are trapped by the high gate to oxide energy barrier of 3.2eV. Since the potential-energy barrier at the oxide-silicon interface is greater than 3.0eV, the rate of spontaneous emission of electrons from the oxide over this barrier is negligibly small. The net negative charge which remains on the floating gate shifts the threshold voltage V_T to a positive value. There are two methods of erasing or removing charges from the floating, namely, ultra-violet (CV) radiation and F-N tunneling.

2.2.2.1 Erasing by UV radiation

The stored charge could be removed by subjecting the memory device to UV radiation. The charge removal process is described by the band diagram in Fig. 2.7. After being exposed to the UV radiation, the electrons gain enough energy to surmount the energy barrier from the floating gate to either the control gate or to the substrate, which reduces the V_T. The typical time it takes to change the V_T from the programmed state to the neutral or erased state is 10 minutes.

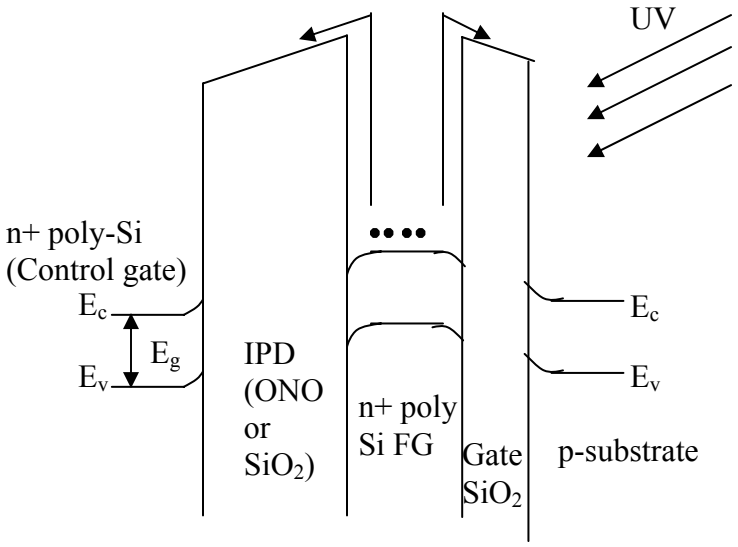

Figure 2.7: Band diagram describing the erasure of stored charge by UV radiation.

2.2.2.2 Erasing by F-N Tunneling

F-N tunneling can also be used to erase a NVM. One of the methods is by applying a large negative voltage at the control gate. The energy band structure will be influenced as shown in Fig. 2.8. The applied V_{cg} causes F-N tunneling of stored electrons from the floating gate to the substrate through the thin gate oxide.

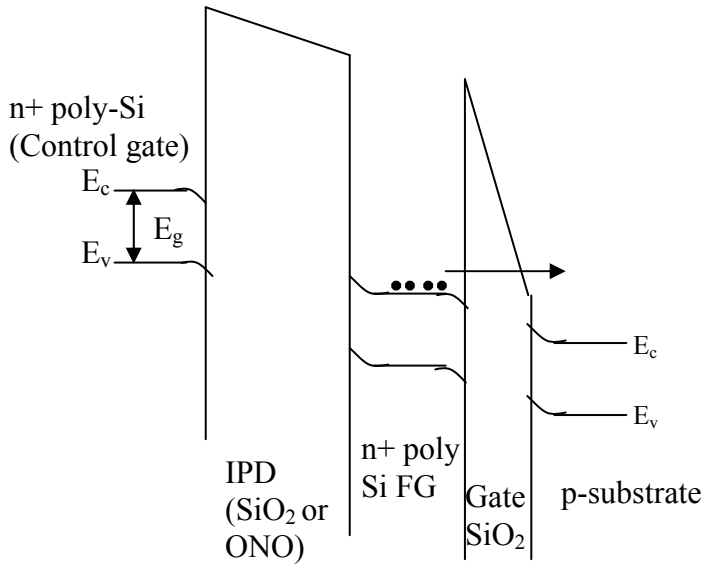

Figure 2.8: Energy band diagram of a floating gate memory during erasing by F-N tunneling.

Figure 2.9a and 2.9b show two methods to erase a Flash EEPROM. For uniform F-N tunneling erase, a large negative V_{cg} is applied while for drain-side tunneling erase method, both a negative V_{cg} and a positive V_d are applied.

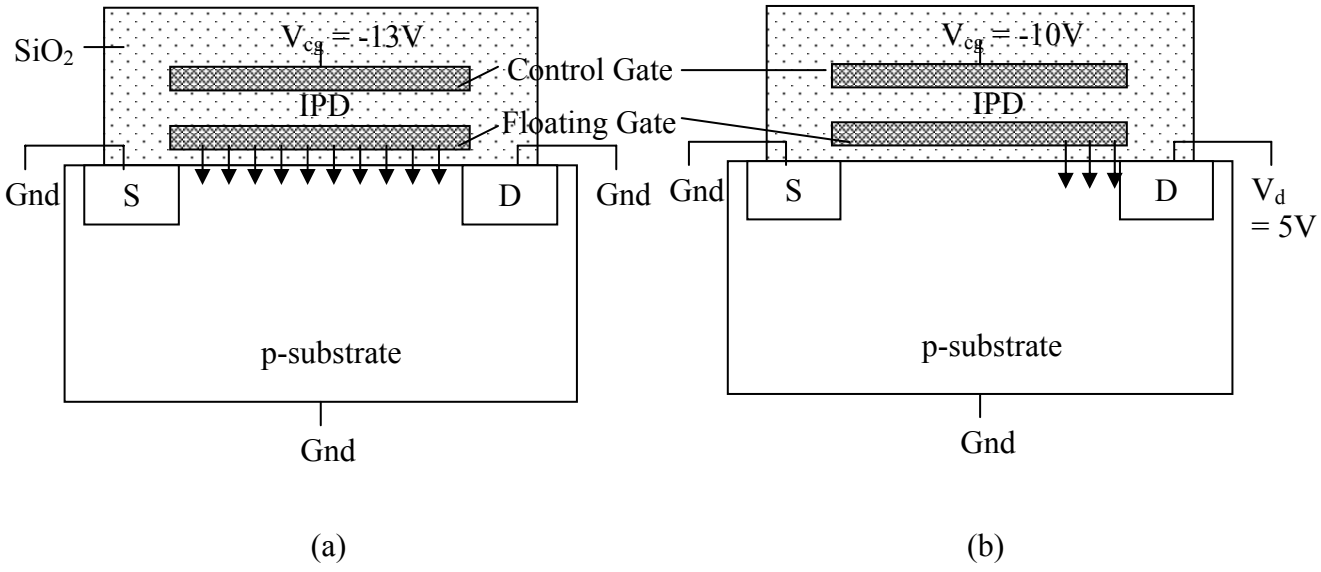

Figure 2.9: Schematic diagrams showing two methods to erase a Flash EEPROM: (a) uniform F-N tunneling erase and (b) drain-side tunneling erase.

In general, uniform tunneling erase is slower that drain-side tunneling erase, but, drain-side tunneling tends to cause reliability issues. The reliability issue is the gate oxide damage that occurs near the drain since a small area is bombarded by electrons and that the tunneling current density as a result of a smaller area is higher.

The dominant failure mechanism for FLOTOX EEPROMs and Flash is the degradation of the tunnel oxide due to defects generated under high field stress during write/erase cycles, resulting in a leaky oxide. Besides, the large area requirement due to the use of two transistors in FLOTOX EEPROM, and the relatively high operating voltage (15 to 20 V) required to operate the cell, due to the thick (8 to 10nm) tunnel oxide used, limit the further downscaling of the EEPROM device [28]. Even though the FLOTOX EEPROM and Flash memory have been a dominant technology for the past two decades, the minimum gate dielectric requirement (for acceptable charge leakage from the storage layer back to the Si substrate) somewhat limits the scalability of the minimum dimension of the memory cell.

2.3 Candidates to Address the Limitations of FLOTOX/Flash Memory Devices

Other forms of non-volatile memories have evolved in the past few decades to address the above issue. Some of the more promising candidates are the Metal-Nitride-Oxide-Semiconductor (MNOS), polySilicon-Oxide-Nitride-Oxide-Silicon (SONOS) and nanocrystal memory structure.

2.3.1 MNOS Memory

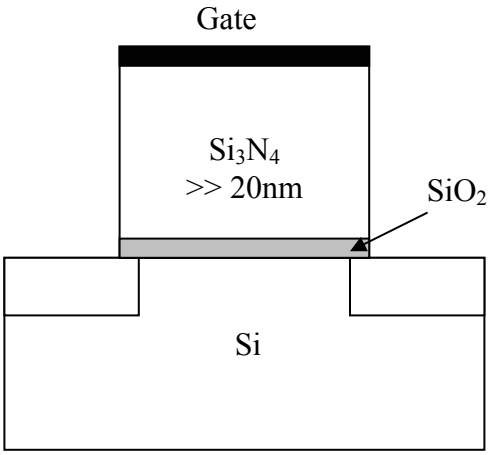

Figure 2.10: Schematic diagram of a MNOS memory structure

The schematic diagram of a MNOS memory structure is shown in Fig. 2.10. In the MNOS system, a gate dielectric containing a thin gate oxide layer and a deposited nitride layer is used [29]. The charge storage occurs in the deep traps within the nitride layer. However, limitations to scale the nitride layer below 200 Å exist due to the significant tunneling from the gate [30]. To overcome this drawback, the SONOS structure was introduced.

2.3.2 SONOS Memory

The SONOS memory structure is similar to the MNOS structure except that an oxide layer is included in between the nitride storage layer and the polysilicon gate. This oxide layer acts as a barrier to carriers injecting into the nitride through the top gate and is useful in reducing the nitride thickness in conventional MNOS systems [31]. The schematic diagram of a SONOS memory structure is shown in Fig. 2.11.

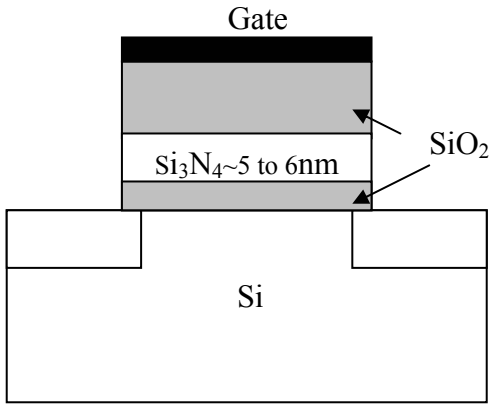

Figure 2.11: Schematic diagram of a SONOS memory structure.

State-of-the-art SONOS devices have nitride thickness in the range of 5 to 6 nm [32]-[33]. SONOS programming occurs through modified F-N tunneling or direct tunneling in the low voltage region and F-N tunneling in the high voltage region. In the case of modified F-N tunneling, the electron tunnels through the tunnel oxide and part of the nitride charge storage layer. In both direct tunneling and F-N regimes, the electron tunnels through just the tunnel oxide layer. In all three cases, increasing the electric field across the tunnel oxide will lead to faster programming. By reducing the charge storage layer thickness to nanocrystal dimensions (< 5 nm), the voltage drop across the charge storage layer will decrease for a given programming voltage. Hence the voltage drop across the tunnel oxide layer will increase, leading to lower programming voltage. The derivation for the coupling factor, or the fraction of the applied voltage to the control gate that appears at the tunnel oxide, is shown in Fig. 2.12.

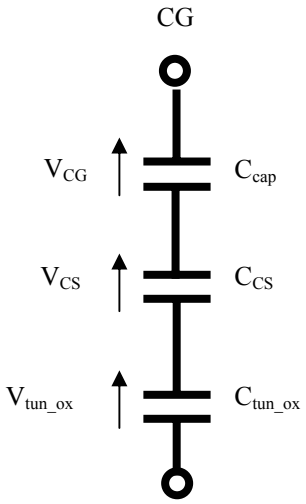

Figure 2.12: Capacitive model of the gate dielectric stack for SONOS-type device. CG denotes the control gate, "cap" denotes the capping (control) oxide layer, CS denotes the charge storage layer and tun_ox denotes the tunnel oxide.

The gate coupling factor for F-N mode program and erase is

$$\frac{V_{tun\_ox}}{V_{tun\_ox}+V_{CS}+V_{CG}} = \frac{1}{1+\frac{C_{tun\_ox}}{C_{CS}}+\frac{C_{tun\_ox}}{C_{CG}}} \tag{2.5}$$

From Eq. (2.5), it is seen that increasing the charge storage capacitance (C_{CS}) or the capping oxide capacitance (C_{cap}) will lead to an increase in the gate coupling factor. This can be achieved by using a dielectric material of higher κ value or reducing the charge storage layer thickness.

Although the nitride storage layer could be reduced in a SONOS memory structure, the main disadvantage associated with SONOS memory devices is that the traps are distributed randomly in the nitride charge storage layer [34]-[35]. In this aspect, the nanocrystal nonvolatile memory (NVM) structure becomes the more ideal candidate as it is able to offer greater control of the spatial location of the charge storage sites and,

at the same time, possesses the advantage of SONOS (due to its similar structure to SONOS).

2.3.3 Nanocrystal Memory Devices

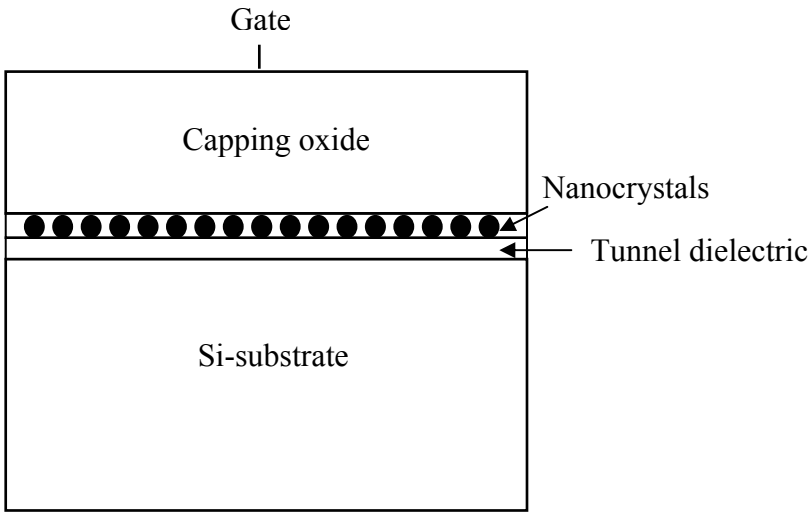

Figure 2.13: Schematic diagram of a nanocrystal memory structure.

A schematic diagram of a nanocrystal memory device is shown in Fig. 2.13. In the nanocrystal NVM structure, charges are stored in isolated nanocrystal nodes [36]-[48]. This storage mode is slightly different from the SONOS device as the charges in a SONOS device are stored randomly in the continuous nitride layer. As the nanocrystals are physically separated from each other by the surrounding oxide dielectric, this enables multi-bit (2 bits or more per-cell) operation [49]-[50]. The physical separation improves the retention time in multi-bit per-cell devices by suppressing the lateral flow of charge [49]. For SONOS memory, minimizing lateral charge redistribution requires careful optimization of the nitride layer. This is a much easier task in nanocrystal

memories through the control of the nanocrystal size and spacing. Nanocrystal memory also offers the possibility to implement nanoscale structures without lithography [49]. Ultra-low power few-electron memories are also possible through the Coulomb blockade effect [51].

2.3.3.1 Methods to Fabricate Nanocrystal Memory Devices

A multitude of techniques have been explored to synthesize nanocrystals. These techniques include plasma enhanced chemical vapor deposition (PECVD) [52], ion-implantation [53], hydrogen (H_2) or silicon reduction of metastable $Si_{1-x}Ge_xO_y$ [54]-[57], deposition (by electron beam evaporation) of Ge layer onto a SiO_2 tunnel dielectric layer, followed by oxidation at 800^{o}C to 1000^{o}C [58] and sputtering plus high temperature annealing [59].

In the work by Iacona *et al*. [52], a parallel-plate plasma enhanced chemical vapor deposition (PECVD) system, consisting of an ultra-high-vacuum chamber (base pressure 1×10^{-9} Torr) and a rf generator (13.56 MHz), connected through a matching network to the top electrode of the reactor, was used to prepare a substoichiometric (SiO_x) thin film using a power of 50W at a temperature of 300^{o}C. The source gases used were high-purity (99.99% or higher) SiH_4 and N_2O with the flow ratio N_2O/ SiH_4 varied between 6 and 15, while keeping the total gas flow rate constant at a value of about 140 sccm. The total pressure during deposition processes was maintained constant at a value of about 6×10^{-2}Torr. After deposition, the SiO_x films were then annealed for 1h at temperatures between 1000 and 1300°C in an ultra pure nitrogen atmosphere to form Si nanocrystals. This method has a disadvantage of long annealing time at high temperature.

In the ion-implantation method used by Fukuda *et al*. [53], a SiO_2 film was first grown on Si in dry oxygen ambient at 900 °C for 15 minutes using a quartz furnace tube, followed by implantation of germanium (Ge) ions into the SiO_2 film, at an ion energy of 25 keV and a dosage of $1x10^{14}$ ions/cm^2. After the ion implantation, the device was then subjected to annealing at 500–1000°C for 1 h in a quartz furnace in N_2 ambient to form Ge nanocrystals. This ion implantation method has the disadvantage of causing a non-uniform location of the nanocrystals along the channel length of the device as well as introduction of damages due to the impact from high energy implantation.

Besides ion implantation, several research groups have also created Ge nanocrystals in SiO_2 via H_2 or Si reduction of metastable $Si_{1-x}Ge_xO_y$ [54]-[57]. An attractive feature of this approach is high wafer throughput. This is due to the ability to process a batch of wafers in parallel, compared to the serial processing required for many other techniques. In addition, in contrast to ion implantation which creates Gaussian-shaped nanocrystal density depth profiles, H_2 or Si reduction of metastable $Si_{1-x}Ge_xO_2$ creates sharp step profiles. An explanation of the reduction process is given as follows:

When Si is in contact with GeO_2, the following reduction reaction occurs:

$$GeO_2 + Si \longrightarrow SiO_2 + Ge \qquad (2.6)$$

yielding a much lower free-energy state. This reaction can occur if the SiGe-oxide film is in contact with a Si or SiGe substrate. At the interface between the materials, Si from the substrate is available for the reduction reaction. Since the diffusivity of Si in oxide is quite small, Si can only be supplied to the oxide in close proximity (<10 nm) to the

unoxidized film and, hence, Ge precipitates only at the interface and not throughout the entire mixed oxide.

The other reduction pathway for GeO_2 is the reaction of the oxide with hydrogen at elevated temperatures:

$$GeO_2 + H_2 \longrightarrow Ge+H_2O \qquad (2.7)$$

At first glance, it would seem to be a simple reduction mechanism, but the actual kinetics can be somewhat complicated which may in turn complicate the prediction and control of nanocrystal size distribution [57].

In the oxidation process adopted by Kobayashi *et al*. [58] a 4-nm-thick tunnel SiO_2 film was first grown on the Si substrate, followed by the deposition of a 10nm-thick Ge film using electron-beam evaporation at a substrate temperature of 60 °C and a base pressure of 2×10^{-7} Torr. The Ge layer was then annealed a temperature between 800 and 1000°C for 1 h in a dry O_2 ambient. Due to the rapid diffusion of O_2 molecules through the Ge grain boundaries, the Ge became crystallized and embedded in the SiO_2 during high temperature oxidation.

In the work by Teo *et al.* [59], the Ge nanocrystal memory devices were fabricated by sputtering a layer of Ge onto the SiO_2 tunnel dielectric followed by sputtering a layer of SiO_2 to form the capping oxide. The trilayer structure was then annealed at 1000^oC for 5 minutes to form Ge nanocrystals. The advantages of this method are: (1) no requirement for complicated equipment, (2) very short process time and (3) the size of the nanocrystals can be controlled by the thickness of the deposited Ge layer. A summary of the various nanocrystal fabrication methods is given in Table 2.3

Table 2.3: A summary of the various nanocrystal fabrication techniques.

Group	Material used as nanocrystal/ host matrix	Method to form nanocrystals	Remarks
F. Iacona *et al.* [52]	Si/SiO_2	PECVD	Long annealing time (1hr) at high temperature (1000^oC to 1300^oC) to form nanocrystals.
Fukudal *et al.* [53]	Ge/SiO_2	Ion implantation	Gaussian profile. Variation in threshold voltage along channel within device.
Taraschi *et al*. [57]	Ge/SiO_2	H_2 reduction of metastable $Si_{1-x}Ge_xO_2$.	Nanocrystalline Ge formation via metastable $Si_{1-x}Ge_xO_y$ reduction is kinetically complex which may in turn complicate the prediction and control of nanocrystal size distribution.
Kobayashi *et al*. [58]	Ge/SiO_2	Deposition of Ge film on SiO_2 layer followed by 1h oxidation at a temperature between 800^oC and 1000^oC.	Oxidation at high temperature required. Undesirable for retention characteristic if high-κ material is used as host matrix.
Teo *et al.* [59]	Ge/SiO_2	Sputter then anneal	Quick and easy process, nanocrystal size can be controlled by thickness of sputtered middle layer.

2.3.4 Other Emerging Memory Devices

Besides MNOS, SONOS and nanocrystal memory devices, other replacements for non-volatile memory are actively researched. These include research on new materials and mechanisms in phase change memory and Magnetic Random Access Memory (MRAM) and Ferroelectric Random Access Memory (FeRAM).

The Phase Change Memory (PCM), also called Ovonic Unified Memory (OUM), structure typically comprises of a transistor and a resistor. The resistor is made from chalcogenide material alloys that are used in rewritable compact disks. During operation, electrical energy is used to convert the phase of the material between crystalline (conductive) and amorphous (resistive) phases. This change of phase in the material in turn changes the electrical resistivity of the material. Figure 2.14 shows the schematic of a typical OUM.

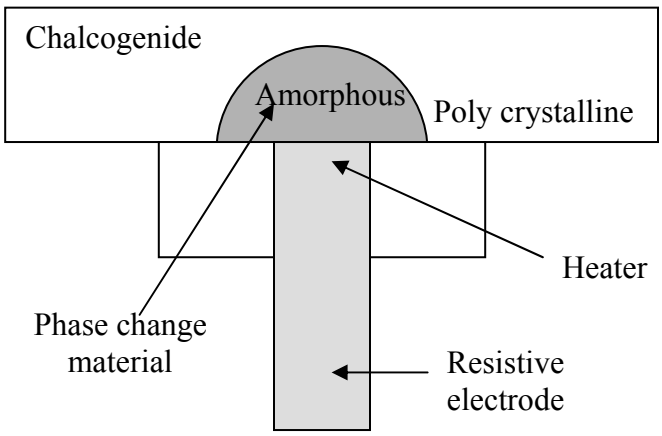

Figure 2.14: Schematic diagram of a Ovonic Unified Memory (OUM) device.

The small volume of active media in Figure 2.14 works as a programmable resistor that can reversibly change its resistance by greater than 40 times. During operation, a MOSFET is used to apply a varying magnitude current pulse to change the

memory cell into a high or low resistance state and the stored data is read by measuring the resistance changes in the cell. Multi-state operations can also be achieved by programming the cell to intermediate resistance values. Another advantage of the OUM is that the cell size determines the energy required for the phase transformation. As a result, the write current scales with the cell size, hence facilitating memory scaling. OUM devices therefore exhibit fast access time (<100 ns), long endurance (>10^{12} cycles), and good data retention (>10 years). However, in order to achieve high packing density, OUM devices need to reduce the programming current to match the minimum transistor drive current capability. One of the lowest programming current reported is 0.1 to 0.2mA/device [60]. The high current places a limit on the minimum width of the transistor used to supply this current, thus resulting in a larger cell size.

In the case of MRAM, the data is stored as the spin state in a magnetic material. During operation, an electrical current is used to switch the magnetic polarity, and the change of the magnetic polarity is sensed as the change of resistance. Advantages of the MRAM includes its fast (<50 ns) write and erase speed, low power and low voltage operation, and unlimited write and erase cycles. However, similar to OUM and FeRAM, MRAM also faces the challenge of integration with mainstream CMOS process.

Among the emerging memory devices, the nanocrystal memory structure is the most promising near-term solution to industry requirement as it could be easily integrated into the mainstream CMOS process, provides good charge retention without the requirement for a thick tunnel dielectric and uses only small voltages for device operation. A brief description on the structure and methods to further enhance the performance of the nanocrystal memory device will be given in the next section.

2.4 Approaches to Improve the Performance of Nanocrystal Memory

The nanocrystal memory structure consists of three layers, namely, the tunnel dielectric, the nanocrystal charge storage layer and the capping oxide. During device operation, charges are injected from the Si substrate through the tunnel dielectric and stored in the nanocrystals. The presence of the capping oxide prevents the charge leakage from the nanocrystal nodes to the gate terminal. The following sections describe the possibilities of introducing some changes to the tunnel dielectric and capping oxide for better device performances.

2.4.1 Tunnel Oxide Thickness Reduction and its Related Issues

During programming, charge carriers tunnel from the Si substrate across the tunnel oxide into the charge storage nodes. In this case, a thin tunnel oxide is desirable to achieve a fast programming speed. A thin tunnel oxide also allows direct tunneling to be used during programming and this programming mode results in less device degradation compared to F-N tunneling.

Although a thin tunnel dielectric is desirable for fast programming speed, the stored charges may tunnel back into the Si substrate easily if a minimum physical thickness has not been met. Hence, a trade-off exists between programming speed and charge retention capability.

Besides acting as a physical barrier between the nanocrystal charge storage nodes and the Si substrate, the tunnel dielectric also plays the important role of providing a platform for the formation of nanocrystals. The formation of nanocrystals is critical in determining the charge storage capability of the memory device. In the case when the

tunnel dielectric is not sufficiently thick in germanium (Ge) nanocrystal memory, Ge may penetrate through the thin tunnel dielectric during high temperature annealing to form the nanocrystals, and short itself with the Si substrate. The absence of nanocrystals in the middle layer would result in a loss of charge storage capability. Together with the charge retention requirement, the Ge penetration issue also sets a lower bound to the physical thickness of the tunnel oxide.

2.4.1.1 Approach to Address Limitations of Thin Tunnel Oxide

It is therefore proposed to replace the tunnel oxide with a high dielectric constant (high-κ) material (for example, hafnium dioxide (HfO_2)), whose larger physical thickness can overcome the limitations mentioned above. The physical thickness of the high-κ tunnel dielectric can be selected to give the same equivalent oxide thickness (EOT) of an ultrathin tunnel oxide, so that the advantages of a small EOT can be maintained. The leakage current of the HfO_2 film is also several orders of magnitude smaller than silicon dioxide (SiO_2) for the same EOT, resulting in superior data retention time. On the other hand, HfO_2 can provide a larger tunneling current than SiO_2 during program operation, due to the lower electron barrier height of HfO_2 (1.4 eV) as compared to SiO_2 (3.1 eV).

2.4.2 Electric Field Coupling Enhancement

The following sections discuss the introduction of changes to the capping oxide for better device performance. To achieve better electric field coupling or gate coupling, the cap oxide thickness could be reduced or replaced with a high- κ material.

2.4.2.1 Capping Layer Thickness Reduction

A primary approach to improving the nanocrystal device performance would be to ensure that a large portion of the applied gate voltage appears across the tunnel oxide layer. This could be achieved by reducing the capping oxide thickness. A thinner capping oxide would also require smaller gate voltages to be applied during writing and erasing. This is essential to satisfy the requirements of low voltage operation. However, similar to issues encountered by a thin tunnel oxide, a lower-bound limit also exists for the capping oxide thickness reduction. The capping oxide must be sufficiently thick to prevent the out-diffusion of Ge into the ambient during annealing to form the Ge nanocrystals. Besides, the out-diffusion issue, this layer must also be sufficiently thick to prevent the leakage of charge from the storage nodes into the gate electrode.

2.4.2.2 High-κ Material as Alternative Capping Material

Similar to the approach adopted to alleviate the issue encountered by a thin tunnel dielectric, a high-κ material could be used to replace the capping oxide. Due to its high dielectric constant value, a thick layer of material could be used to prevent the out-diffusion of Ge during annealing. At the same time, the high-κ capping oxide is

electrically thin to ensure that a large portion of the applied gate voltage appears across the tunnel dielectric layer for better gate or electric field coupling.

2.5 Summary

In the downscaling of transistor devices, the introduction of high-κ materials appears to offer a promising solution to address most of the limitations encountered by the conventional SiO_2 gate dielectric. The main criteria of an ideal high-κ material are: high relative dielectric constant value, compatibility with current CMOS process, good thermodynamic stability on Si, low defect density as well as large conduction and valence band offsets for low gate leakage current characteristics. Among the alternative gate dielctric materials studied in the literature reviews, HfO_2 and ZrO_2 emerge as the more suitable candidates to replace SiO_2.

In the downscaling of memory devices, the dimension reduction of conventional FLOTOX EEPROM and Flash memory has arrived at a saturation stage. The scalability of the memory cell is mainly limited by the minimum gate dielectric thickness requirement to ensure acceptable charge leakage from the storage layer back to the Si substrate. Other forms of non-volatile memories, such as MNOS, SONOS and nanocrystal memory structure, have since evolved to address the above issue. Among these devices, the nanocrystal memory structure is one of the more promising near-term solutions to industry requirement as it has the following advantages. It could be easily integrated into the mainstream CMOS process, provides good charge retention without the requirement for a thick tunnel dielectric and uses only small voltages for device operation.

High-κ materials could be integrated into the nanocrystal memory structure for better device performances. When the high-κ material is used as the tunnel dielectric, faster programming is likely be achieved due to its lower electron tunneling barrier while at the same time, better charge retention could be expected due to its physically thick layer. When the high-κ material is used as the capping layer, better gate electric field coupling factor could be obtained. The improvement in the gate electric field coupling factor would ensure that a large portion of the voltage applied at the gate electrode appears at the tunnel dielectric layer for more efficient device operation.

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Chapter 3: Fabrication and Characterization of High-Dielectric Constant Materials for Potential Applications in Nanocrystal Memory Devices

As discussed in the Chapter 2, the utilization of a high dielectric constant (high-κ) material as a replacement for SiO_2 offers much promise for the performance enhancement of the nanocrystal memory device. Preliminary work involving the fabrication and characterization of high-κ films was first carried out before employing the high-κ material in the nanocrystal memory device. The results of such work are presented in this chapter.

3.1 Fabrication and Characterization of Zirconium Dioxide (ZrO_2)

High-κ dielectric films of zirconium dioxide (ZrO_2) were fabricated and their structural and electrical properties were characterized. The charge transport mechanisms in the ZrO_2 films were also analyzed and discussed.

3.1.1 Device Fabrication

MIS capacitors with ZrO_2 dielectric and Al gate were fabricated on n-type (100) silicon wafers with resistivity of 4-8 Ω-cm. Prior to ZrO_2 deposition, the wafers were cleaned in RCA I and II solutions, dipped in 10% hydrofluoric acid, rinsed in de-ionized water and then dried. ZrO_2 was reactively sputtered in a sputtered-up configured system with a base pressure of 2.5×10^{-6}Torr. The sputtering was performed in argon and oxygen ($Ar+O_2$) ambient with flow rates of 4 sccm and 80 sccm, respectively, under a total pressure of 40mTorr. Sputtering power of 200W and 320W were investigated and it was found that higher sputtering power generally results in sputter damage. The wafer

substrate temperature was kept between 300°C to 400°C during reactive sputtering. Aluminum metallization was performed for the substrate (400nm thick Al) and gate (800nm thick Al to allow for electrical probing) contacts to form Al/ZrO_2/n-Si MIS capacitors. The devices were then annealed at 400°C in nitrogen ambient for 5 minutes. The annealing temperature was kept low to minimize crystallization in the ZrO_2 film, which would lead to increased current leakage, while still obtaining a respectable reduction of the hysteresis in the C-V curves.

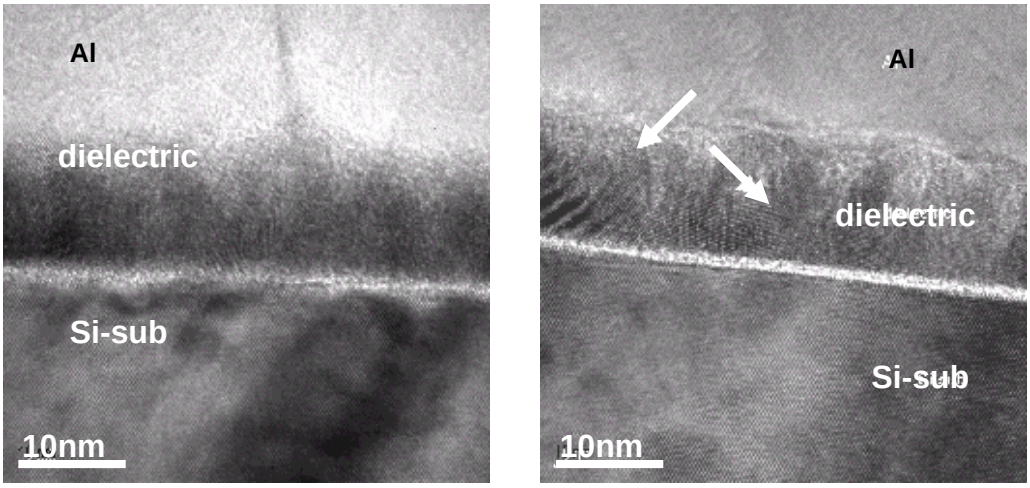
3.1.2 Device Characterization

Upon the completion of device fabrication, structural and electrical characterizations were performed on the devices. The structural characterization includes transmission electron microscopy (TEM) analysis, x-ray photoelectron spectroscopy (XPS) and x-ray diffraction (XRD). Current–voltage (I-V) and capacitance-voltage (C-V) measurements were performed for electrical characterization.

3.1.2.1 Structural Characterization

TEM analysis showed that the sputter-deposited high-κ film consists of a ~1.7 nm thick interfacial layer (possibly zirconium silicate, $ZrSi_xO_y$ [1]) and a ~13 nm thick bulk ZrO_2 layer. Figures 3.1(a) and 3.1(b) show the TEM images of typical low leakage and high leakage sites respectively, on the wafer. More obvious lattice fringes are present in the ZrO_2 layer for the high leakage device. Some of these crystalline grains form a conductive path linking the Al electrode and silicon substrate (Si-sub), as indicated by the arrows in Fig. 3.1(b), resulting in increased current leakage. The difference in the

electrical performance of low leakage and high leakage devices is due to the different degrees of crystallization of the bulk ZrO_2 layer.



(a) (b)

Figure 3.1: TEM images of the fabricated Al/ZrO_2/n-Si MIS devices at (a) a low leakage site and (b) a high leakage site.

The XRD result in Fig. 3.2(a) shows that the crystallization in the ZrO_2 film is not severe for a wafer substrate temperature of 300^{o}C during reactive sputtering, as seen from the absence of a sharp ZrO_2 crystallization peak at a 2-theta angle value of 30^o. The crystallization in the ZrO_2 film is greater at a higher substrate temperature of 400^{o}C, as seen from the appearance of a more prominent broad hump at 2-theta angle values of around 30^o; however, this is still acceptable as most devices fabricated at such a temperature showed good leakage current characteristics. The XPS plots of the Zr3*d* and O1*s* peaks are shown in Figs. 3.2(b) and 3.2(c). The Zr content of the deposited high-κ film, which affects the electrical characteristics of the device, was estimated to be between 23 to 25 atomic (at.) %. Wilk *et al.* [1] have found that films with high Zr content of greater than 30 at. % showed poor electrical properties.

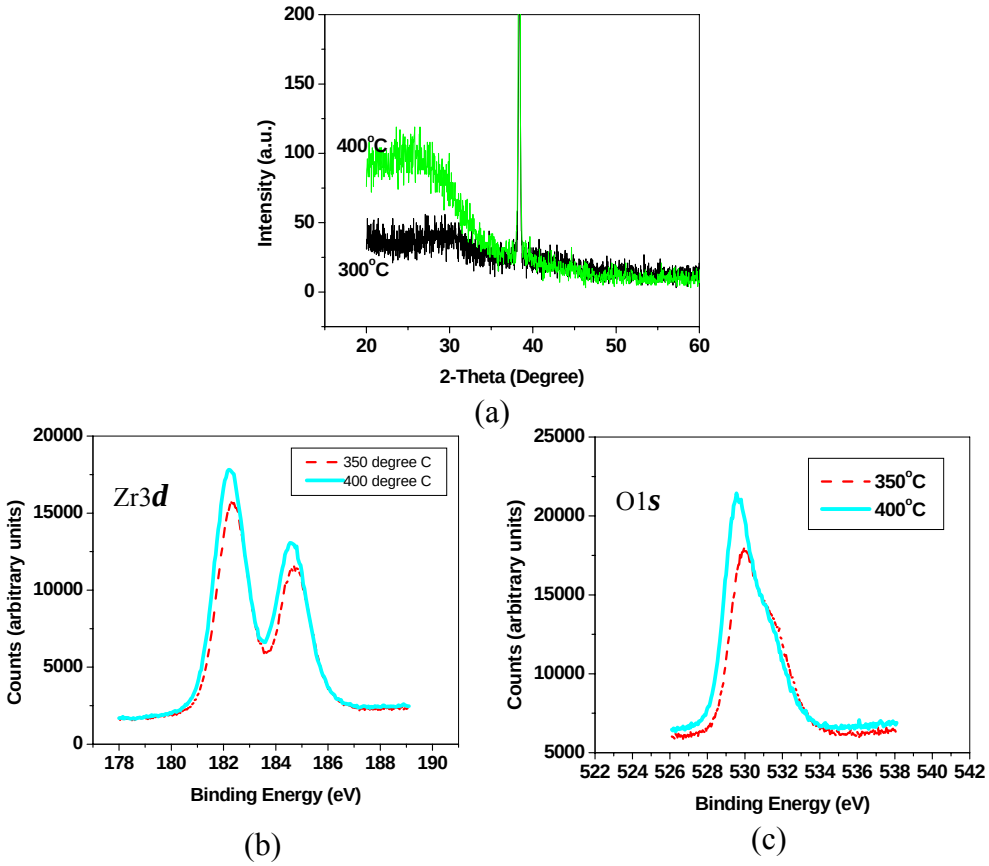
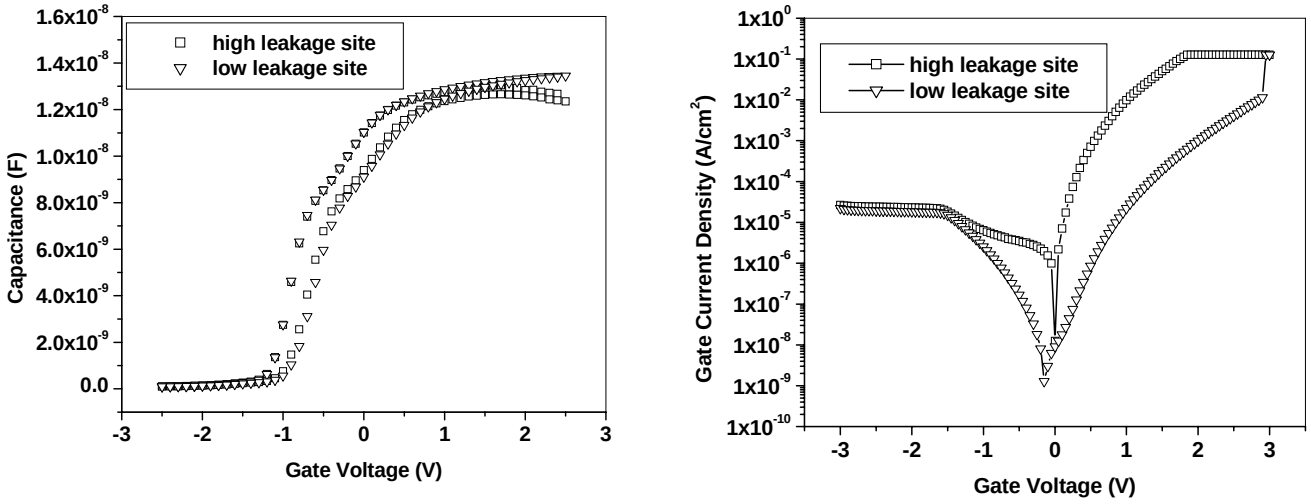


Figure 3.2: Structural characteristics of the fabricated Al/ZrO_2/n-Si MIS devices: (a) The XRD spectra of the ZrO_2 film for wafer substrate temperatures of 300°C and 400°C during sputtering. The (b) Zr3*d* and (c) O1*s* XPS spectra of the ZrO_2 film for wafer substrate temperatures of 350°C and 400°C during reactive sputtering.

3.1.2.2 Electrical Characterization

The high-frequency C-V and gate current density versus gate voltage (J_g-V_g) characteristics of typical low and high leakage devices are shown in Figs. 3.3(a) and 3.3(b), respectively. The sense of the hysteresis is clockwise in the C-V curves of Fig. 3.3(a). In Fig. 3.3(b), the current density of a typical low leakage site is less than 2 x 10^{-5} A/cm^2 at 1 V accumulation bias, with 60% of the tested devices having such low leakage currents. This is lower than devices with silicon dioxide as a gate dielectric of similar equivalent oxide thickness (EOT).



(a) (b)

Figure 3.3: Electrical characteristics of the Al/ZrO_2/n-Si MIS devices: (a) C-V and (b) I-V characteristics for high leakage and low leakage devices.

Figures 3.4(a) and 3.4(b) show the two-frequency (100 and 400 kHz) corrected (measured) C-V curve [2] and the simulated (with quantum-mechanical (Q-M) confinement effects) C-V curve for the low leakage and high leakage Al/ZrO_2/n-Si MIS devices. As the physical thickness of the interfacial layer (~1.7 nm) is rather small, the electric field in this layer is reasonably high (in the region of several MV/cm). This will give rise to a large electric field at the silicon surface which is expected to result in carrier quantization effects that have to be corrected for. The correction of the C-V data for Q-M quantization effects is actually the calculation of a theoretical C-V curve to match the experimental measured C-V data. This theoretical calculation was carried out by solving the one-dimensional Schrödinger equation and the Poisson equation self-consistently using an in-house developed code [3], following the same approach as that used by the UC Berkeley Device Group for an MOS structure [4]. More details on the Q-M simulation is provided in the next section. The Q-M simulated C-V curve, obtained for

zero insulator fixed charge density (N_f) and zero interface state density (D_{it}) and with the Al/n-Si work function difference taken into account, was found to fit the measured C-V curve for the minimum (inversion) and maximum (accumulation) capacitances if relative dielectric constant (κ) values of 15 and 25 were used for the interfacial and bulk ZrO_2 layers. The high κ value found for the interfacial layer again suggests indirectly that this layer is probably not SiO_2 but zirconium silicate ($ZrSi_xO_y$) instead. The amount of flat-band voltage shift of the measured C-V curve as compared to the simulated C-V curve ($N_f = 0$) was used to estimate N_f. For a typical low leakage device, N_f was found to be slightly lower (5.2×10^{12} cm^{-2}) than that of a typical high leakage device (6.1×10^{12} cm^{-2}), although this difference is not very significant. The mid-gap D_{it} was extracted using Terman's method [5], by comparing the C-V curve obtained from measurements with that from Q-M simulation. For typical low and high leakage devices, the extracted mid-gap D_{it} was found to be ~7×10^{12} cm^{-2} eV^{-1} and ~3×10^{12} cm^{-2} eV^{-1}, respectively. There seems to be no direct correlation between the interface state density and the dc leakage current of the Al/ZrO_2/n-Si MIS devices in our work, which is somewhat expected. This could possibly be because of the relatively large physical thickness of the high-κ film which makes the interfacial region less important than the bulk insulator properties (e.g., degree of crystallization) in determining the leakage performance of the devices.

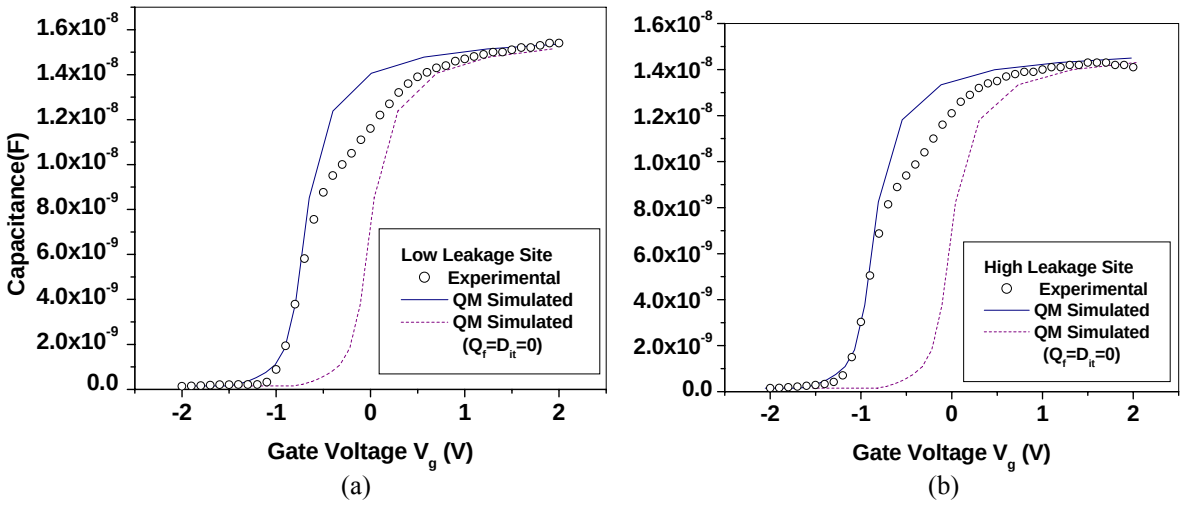


Figure 3.4: Quantum-mechanical C-V modeling (solid and dotted lines) of typical (a) low leakage and (b) high leakage devices compared with experimental measurements (open circles)

3.1.2.3 Quantum-Mechanical Simulation of C-V Curves

The details of the quantum mechanical simulation of the C-V curve is given in this section. In the simulation model [6], electrons are confined in the narrow potential well existing at the insulator-silicon interface and quantized in the direction normal to the tunnel insulator–Si interface. The quantization effect becomes significant with higher substrate doping and a larger surface electric field that results from a smaller gate insulator thickness. Within the potential well, the electrons are quantum-mechanically confined as a two-dimensional (2D) charge sheet and behave like a 2D electron gas. The behavior of electrons in the potential well deviates substantially from classical theory and requires more rigorous Q-M calculations to describe them. The one-dimensional (1D) Poisson and Schrödinger equations are solved self-consistently to find the bounded solution for energy states and the potential. The 1D Poisson equation is

self-approximated using the finite difference method for three adjacent mesh nodes as follows:

$$\frac{V_{j-1} - 2V_j + V_{j+1}}{(\Delta x_j)^2} = -\frac{\rho_j}{\varepsilon_{Si}} \tag{3.1}$$

where x is the direction normal to the insulator–Si interface, ε_{Si} is the permittivity of silicon, and V_j and ρ_j are the respective potential and charge density of the jth mesh node. Δx_j is the size of the jth mesh, and $\Delta x_j = \Delta x$ for all values of j for a uniform mesh size. The calculation begins with the estimation of potential V_j of the various mesh nodes from the matrix form of the 1D Poisson equation given in Eq. (3.2), where j = 2, ..., n-1, and n is the total number of mesh nodes. V_1 and V_n are determined by the specified boundary conditions, where V_1 is the potential of the first mesh node (equal to the input gate

$$\begin{pmatrix} -2 & 1 & & & & & \\ 1 & -2 & 1 & & & & \\ & 1 & -2 & 1 & & & \\ & & & & & & \\ & & & 1 & -2 & 1 & \\ & & & & 1 & -2 & \end{pmatrix} \begin{pmatrix} V_2 \\ V_3 \\ V_4 \\ \\ V_{n-2} \\ V_{n-1} \end{pmatrix} = \frac{-(\Delta x)^2}{\varepsilon_{Si}} \begin{pmatrix} \rho_2 - \frac{\varepsilon_{Si}}{(\Delta x)^2} V_1 \\ \rho_3 \\ \rho_4 \\ \vdots \\ \rho_{n-2} \\ \rho_{n-1} - \frac{\varepsilon_{Si}}{(\Delta x)^2} V_n \end{pmatrix} \tag{3.2}$$

voltage) while V_n is the potential of the last mesh node, which is deep in the quasineutral silicon bulk.

Using the calculated potential of the various mesh nodes from Eq. (3.2), the 1D Schrödinger equation in Eq. (3.3) is solved to obtain the wave functions and eigenenergies, as follows:

$$[-\frac{\hbar}{2m^*}\frac{d^2}{dx^2} + V(x)]\psi_{i,v}(x) = E_{i,v}\psi_{i,v}(x) \tag{3.3}$$

where $\hbar$ is the reduced Planck's constant, m^* is the effective mass of the electron along the x direction, $\psi_{i,v}$ and $E_{i,v}$ are the respective wave function and eigenenergy of the ith quantized energy level in the vth valley. In finite-difference form, the 1D Schrödinger equation for three adjacent mesh nodes is given as

$$-\frac{\hbar^2}{2m^*}\{\frac{1}{(\Delta x)^2}\psi_{i,v(j-1)} - [\frac{2}{(\Delta x)^2} + \frac{2m^*}{\hbar^2}V_j]\psi_{i,v(j)} + \frac{1}{(\Delta x)^2}\psi_{i,v(j+1)}\} = E_{i,v}\psi_{i,v(j)} \tag{3.4}$$

Combining all mesh nodes, the matrix form of the 1D Schrödinger equation is

$$-\frac{\hbar^2}{2m^*}H\Psi = E\Psi \tag{3.5}$$

where H is the Hamiltonian matrix.

In the self-consistent calculation, the six ellipsoidal D valleys of the conduction band and both light-hole and heavy-hole valence bands in the bulk-silicon band structure are considered. It is assumed that the structure is under equilibrium condition and all the bands are described within the parabolic approximation [7]. The following values of effective masses are used: the longitudinal mass $m_l^* = 0.92m_0$ and the transverse mass $m_t^* = 0.19m_0$ for electrons, the heavy-hole mass $m_{hh}^* = 0.49m_0$ and the light-hole mass $m_{lh}^* = 0.16m_0$, where m_0 is the free electron mass [8]. With the eigenfunctions obtained from the solution of Schrödinger equation, the charge densities for different energy bands are calculated and substituted into the Poisson equation to obtain the updated potential. The iterative process continues until self-consistency of the potential is obtained. Although the self-consistent QM simulator can take into account wave function penetration, this was ignored in the simulation since the EOT of the multilayered dielectric stack

structures in this work are larger than 1 nm (ranges from 2.5 to 5 nm). The wave function penetration effect was found to be significant only when the EOT approaches 1 nm or smaller [9].

The self-consistent quantization calculation is then repeated with a small change in the input gate voltage, dV_g, in order to calculate the gate capacitance per unit area, C_g, as follows:

$$C_g = \frac{dQ_g}{dV_g} \tag{3.6}$$

where dQ_g is the change in gate charge density resulting from dV_g . Q_g can be found by summing all the charges at and close to the silicon surface by the following equation:

$$Q_g = -q\{\sum_j [N_{sub} + \sum_v (-N_{e,v} + N_{h,v})]\Delta x_j\} \tag{3.7}$$

where q is the electronic charge, N_{sub} is the substrate concentration (positive for n-type silicon and negative for p-type silicon), $N_{e,v}$ and $N_{h,v}$ are the respective electron and hole concentrations of the vth valley. The electron and hole concentrations can be obtained by summing the carrier density from all available energy levels and valleys. The carrier density of the vth valley is given as

$$N_v = \sum_j \sum_i |\psi_{i,v(j)}|^2 \frac{k_B T}{\Delta x_j \pi \hbar^2} g_v m_v^* \ln[1 + \exp(\frac{E_F - E_{i,v}}{kT})] \tag{3.8}$$

where k is the Boltzmann constant, T is the temperature, E_F is the Fermi energy level of the silicon substrate, g_v is the valley degeneracy, and m_v^* is the density of state mass of the carrier for the vth valley.

The voltage drops across the various layers of the MIS device are considered as follows. The voltage drop in the oxide, or insulator layer of the MIS device, is found by assuming that the insulator electric field is constant and there is negligible trapped charge in the insulator layer. The amount of barrier lowering resulting from the image force effect was not considered as this is lower in high-*k* materials and is also reduced by the Q-M repulsion of both bound and unbound carriers [10]. The voltage drop resulting from the charge quantization effect is calculated by finding the mean position, or dc centroid, of the inversion charge. King *et al.* has performed a detailed analysis of the charge quantization effect [11]. The dc centroid of the inversion charge, X_{dc}, is defined as follows:

$$x_{dc} = \frac{\int \rho_{inv}(x).xdx}{\int \rho_{inv}(x)dx} \tag{3.9}$$

where $\rho_{\mathrm{inv}}(x)$ is the inversion charge density at the local position x. The equivalent-oxide thickness of the insulator, which takes into account the charge quantization effect, is calculated as follows:

$$EOT = T_{ox} + x_{dc}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \tag{3.10}$$

where T_{ox} is the physical thickness of the oxide or insulator and $\varepsilon_{\mathrm{ox}}$ is the permittivity of the oxide.

The voltage drop resulting from charge quantization effects, or the dc centroid of the inversion charge, can be obtained as

$$V_{QM} = F_{ox} x_{dc} \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \tag{3.11}$$

where F_{ox} is the oxide electric field.

For a multilayered dielectric stack structure, additional voltage drops across the various insulator layers of the gate dielectric stack are included in the gate voltage calculation. The overall gate voltage is given as

$$V_g = V_{surface} + V_{fb} + V_{ins\_1} + V_{ins\_2} + ... + V_{ins\_n} \tag{3.12}$$

where $V_{surface}$ is the voltage drop at the silicon surface resulting from surface band bending taking into account V_{QM} , V_{fb} is the flatband voltage, and V_{ins_1} , V_{ins_2} , and V_{ins_n} are the respective voltage drops across layers 1, 2, and *n* of the multilayered dielectric stack.

3.1.3 Charge Transport Mechanisms

In this section, the current transport mechanisms in the ZrO_2 MIS devices were investigated. The study is based on the comparison of the experimental data with the simulation results. The EOT of the Al/ZrO_2/n-Si MIS devices was estimated to be ~2.5 nm from the C-V measurements. The average dielectric constant of the ZrO_2 high-κ film was estimated to be ~21 by dividing the total physical thickness of the high-κ film (from the TEM measurements) with the extracted electrical thickness (i.e., EOT). The electrical

thickness was extracted from the corrected accumulation capacitance using a two-frequency C-V measurement method [2], after accounting for Q-M effects.

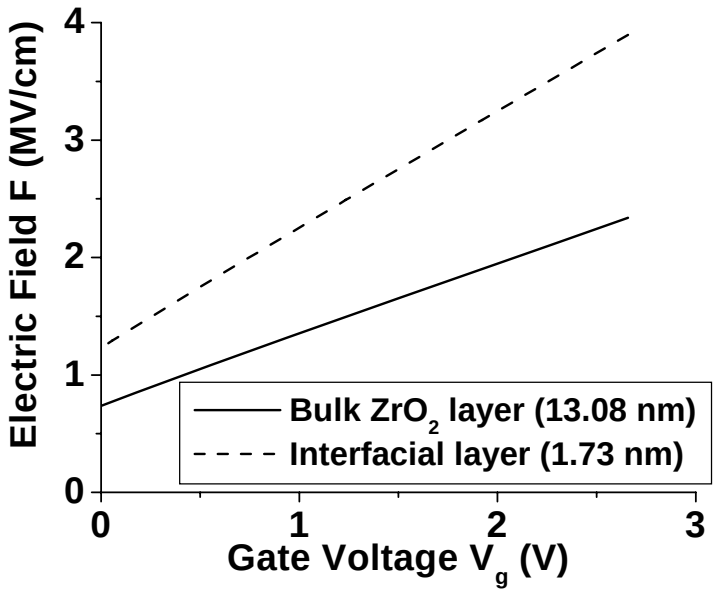


Figure 3.5: Plot showing the electric fields in both the bulk ZrO_2 and interfacial layer at the various gate voltages.

The current transport mechanisms in the Al/ZrO_2/n-Si MIS devices were investigated by fitting the measured gate current density versus gate voltage (J_g-V_g) characteristics under low V_g accumulation bias to Schottky emission and Frenkel-Poole (F-P) emission mechanisms. For the investigation, V_g was first converted to electric field in either the interfacial or bulk ZrO_2 layers as shown in Fig. 3.5.

The electric field (F) in Fig. 3.5, was calculated from equations (3.13) and (3.14) using the Q-M simulation program described above by obtaining the potential drops

across the interfacial and bulk ZrO_2 layers for each value of V_g from the program and dividing these by the respective physical thickness, d, of the layer.

$$\begin{aligned} V_g &= V_{surface} + V_{fb} + V_{interfacial} + V_{ZrO_2} \\ &= V_{surface} + V_{fb} + F_{interfacial} d_{interfacial} + F_{ZrO_2} d_{ZrO_2} \end{aligned} \tag{3.13}$$

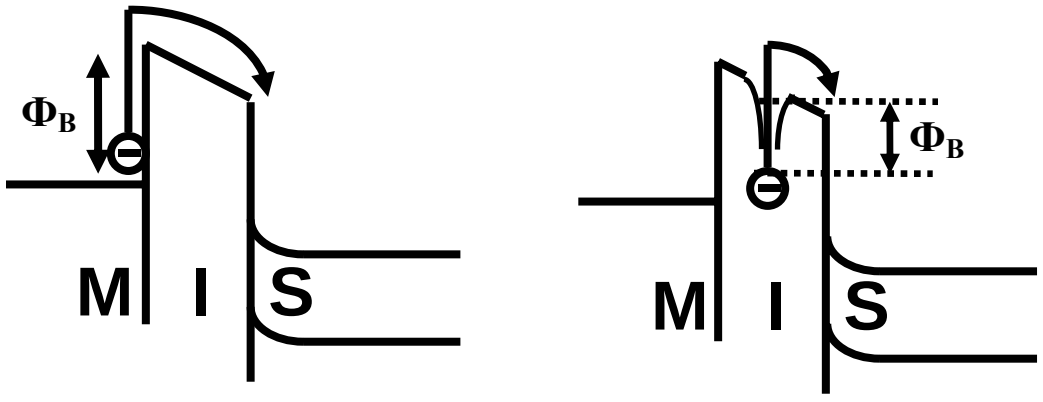
According to Gauss' Law, the electric displacement field through a material, D, is directly related to the electric field, F, via a material-dependent permittivity, ε; that is, D = εF. When a voltage is applied on the two materials, continuity of the electric field displacement across the two mediums must be observed. Mathematically, it can be represented as:

$$\varepsilon_{interfacial} \vec{F}_{interfacial} = \varepsilon_{ZrO_2} \vec{F}_{ZrO_2} \tag{3.14}$$

By solving for equations (3.13) and (3.14) using the Q-M simulation program, the plot of electric field across the interfacial layer and the bulk ZrO_2, shown in Fig. 3.5, could be obtained.

The band diagrams describing the Schottky emission mechanism and the F-P emission mechanism are given in Fig. 3.6 (a) and Fig. 3.6 (b) respectively. The Schottky emission mechanism is an electrode-limited conduction and occurs at low voltages at which electrons at the surface of the injecting electrode (the silicon substrate in this case under positive gate bias) transit above the potential barrier. The F-P emission mechanism is due to the field-enhanced thermal excitation of trapped electrons into the insulator

conduction band. Both F-P and Schottky emissions result from the Coulomb lowering of the potential barrier under an applied electric field.



(a) (b)

Figure 3.6: Band diagrams describing the current conduction processes in Metal-Insulator-Semiconductor devices. (a) shows the Schottky emission mechanism and (b) shows the F-P emission mechanism.

The expressions for F-P emission and Schottky emissions are given as [12]:

F-P emission: $$J_g = B\,F\,exp\left[\frac{q}{kT}\sqrt{\frac{qF}{\pi\varepsilon}} - \frac{q\Phi_t}{k_B T}\right] \quad (3.15)$$

Schottky emission: $$J_g = A\,T^2\,exp\left[\frac{q}{kT}\sqrt{\frac{qF}{4\pi\varepsilon}} - \frac{q\Phi_B}{k_B T}\right] \quad (3.16)$$

where A and B are constants, ε ($=\kappa\varepsilon_o$) and F are the dielectric constant and electric field of either the interfacial or bulk ZrO_2 layer, ε_o is the permittivity of free space, q is the electronic charge, k is Boltzmann constant and T is the temperature in Kelvin. Φ_B is the barrier height seen by the injecting electrons for the Schottky emission mechanism, while

Φ_t is the barrier seen by the trapped electrons for the F-P emission mechanism (equivalent to the depth of the potential well at the trapping site).

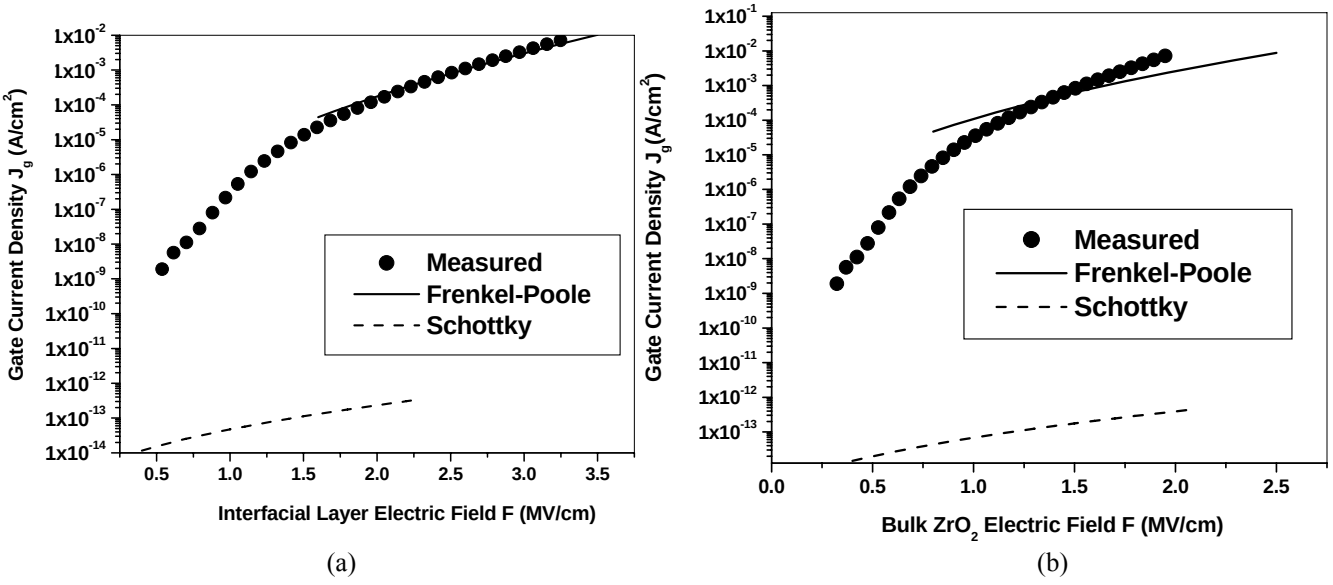


Figure 3.7: The measured and calculated (fitted) J_g-F characteristics, for values of F in the (a) interfacial layer and (b) bulk ZrO_2 of a typical low leakage Al/ZrO_2/n-Si MIS device in the low gate bias region.

Figures 3.7(a) and 3.7(b) show the measured and calculated (fitted) J_g-F characteristics, for values of F in the interfacial layer and bulk ZrO_2, respectively, of a typical low leakage Al/ZrO_2/n-Si MIS device in the low gate bias region. The calculated J_g-F characteristics were obtained with T = 295 K, κ = 15 (interfacial layer) or 25 (bulk ZrO_2), Φ_t = 1 eV (interfacial layer) or 0.9 eV (bulk ZrO_2), Φ_B = 1.4 eV, A = 120 A cm^{-2} K^{-2} (the free-electron Richardson constant was assumed, as the effective Richardson constant was not known, for both the interfacial layer and bulk ZrO_2), and B = 25.95 A cm^{-1} V^{-1} (interfacial layer) or 667 A cm^{-1} V^{-1} (bulk ZrO_2). Values of κ used in the fitting were taken from the Q-M C-V simulation. The electric fields in the interfacial layer and

bulk ZrO_2 corresponding to each gate voltage (see Fig. 3.5) were obtained from the Q-M C-V simulation as explained above. It is seen from Fig. 3.7(a) that only the F-P emission mechanism fit the measured J_g-V_g data between electric fields of 2.0 and 3.2 MV/cm in the interfacial layer (corresponding to $0.7 < V_g < 2$ V). The Schottky emission mechanism, however, does not fit the measured J_g-V_g data at all. For the bulk ZrO_2 layer, both Schottky and F-P emission mechanisms do not fit the measured J_g-V_g data over electric fields in the bulk ZrO_2 from 0.7 to 1.9 MV/cm (corresponding to $0 < V_g < 2$ V). This could possibly be due to the polycrystalline structure of the bulk ZrO_2, making it difficult to fit basic conduction mechanisms like Schottky and F-P emission to the experimental measurements, as also reported by Chaneliere *et al*. [13] for crystalline tantalum pentoxide films. The above results therefore indicate that the interfacial layer plays an important role in determining the conduction mechanism through the high-κ MIS structure. The electric field in the interfacial layer is generally larger than that in the bulk ZrO_2. The injecting field at the cathode or the n-type silicon substrate in this case, depends on the electric field in the interfacial layer as this is directly in contact with the silicon substrate.

3.2 Fabrication and Characterization of Hafnium Dioxide

Besides ZrO_2, hafnium dioxide (HfO_2) is also another high-κ material which has been extensively researched upon [14]-[19]. Many groups have found that both Zr and hafnium (Hf) posses almost identical characteristics. This similarity in properties arises from both elements having the same chemical bonding and similar electronic configuration [20], [21]. In this project, HfO_2 films were also fabricated and characterized. The following sections show some of the results obtained from the fabricated HfO_2 films.

3.2.1 Fabrication of HfO_2 Film

Fabrication of the HfO_2 film was performed on n-type, 4-8 Ω-cm (100) silicon wafers. Prior to HfO_2 deposition, the wafers were cleaned in RCA I and II solutions, dipped in 10% hydrofluoric acid, rinsed in de-ionized water and then dried. HfO_2 was reactively sputtered in a system with base pressure of 9.4×10^{-6} Torr. The sputtering was performed in an ambient of 95% argon and 5% oxygen ($Ar+O_2$), under a total pressure of 40 mTorr. A sputtering power of 100W was used for the high-κ tunnel dielectric fabrication. The wafer substrate temperature was maintained at 360°C during reactive sputtering. The film was then annealed at 400°C in nitrogen ambient for 5 minutes. The TEM picture of the fabricated high-κ film is shown in Fig. 3.8.

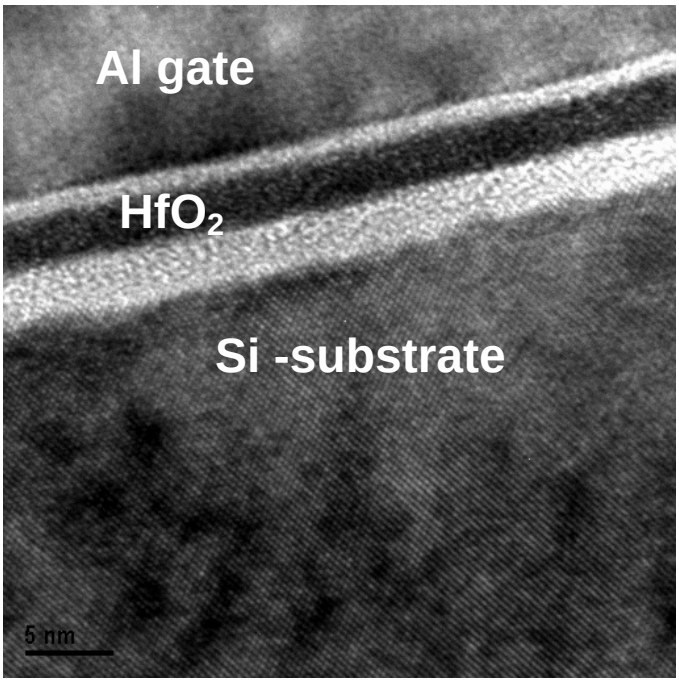
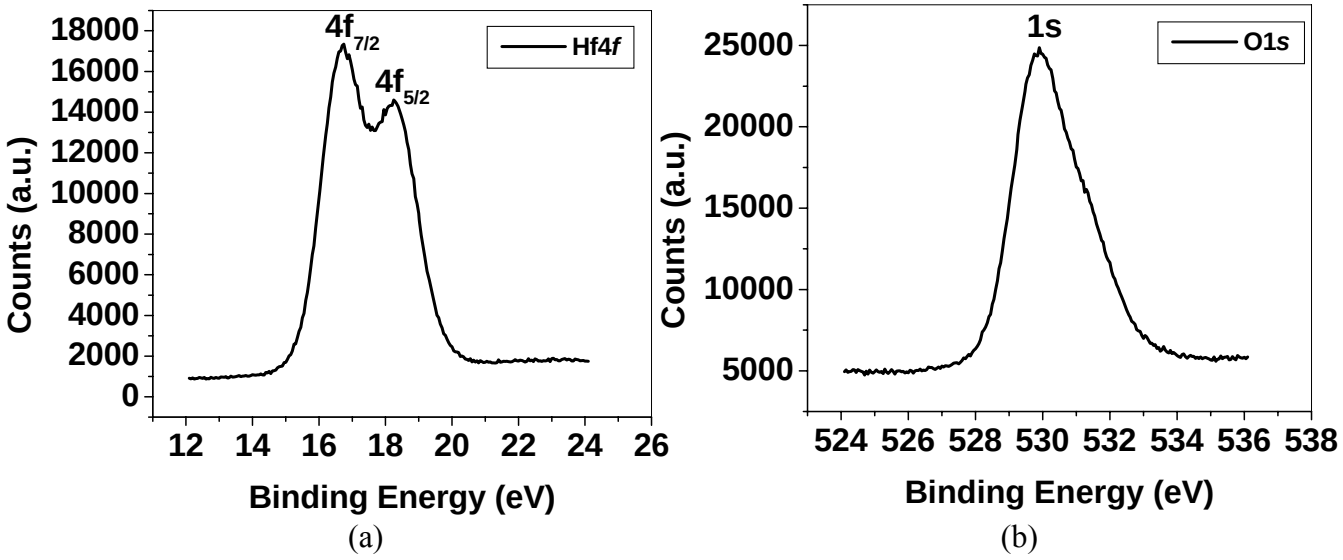


Figure 3.8: TEM picture of the high-κ (HfO_2) film.

3.2.2 XPS Characterization of HfO_2 Film

XPS was used to analyze the percentage composition of the respective elements in the deposited HfO_2 film. The XPS spectra of the Hf4*f* and O1*s* peaks are shown in Figs. 3.9(a) and 3.9(b), respectively. Based on the area enclosed by the peak for each of the two elements and their relative sensitivity factor [22], the ratio of hafnium to oxygen composition was determined to be 19.1 at. % to 80.9 at. %. The percentage composition plays an important role in determining the electrical performance of the dielectric layer. A high-κ metallic content of greater than 30 at. % generally results in poor electrical properties, especially poor gate leakage [1].



(a) (b)

Figure 3.9: (a) Hf4*f* and (b) O*1s* XPS spectra of the deposited and annealed HfO_2 film.

3.2.3 Electrical Characterization of the HfO_2 Film

A typical high frequency capacitance-voltage (C-V) characteristic of the above MIS device, with HfO_2 as the insulator layer, is shown in Fig. 3.10. For a gate voltage sweep range of –4V to 2V, the high-κ MIS device shows a clockwise hysteresis of 110mV. Based on a capacitor area of 1.1 x 10^{-2} cm^2, the EOT of the high-κ layer, extracted from the C-V measurement in Fig. 3.10(a), is 4.8nm. In Fig. 3.10(b), the device shows a leakage current density of 3.6 x 10^{-6} A/cm^2 at 1 V accumulation bias. This leakage current density is several orders lower than SiO_2 of similar electrical thickness.

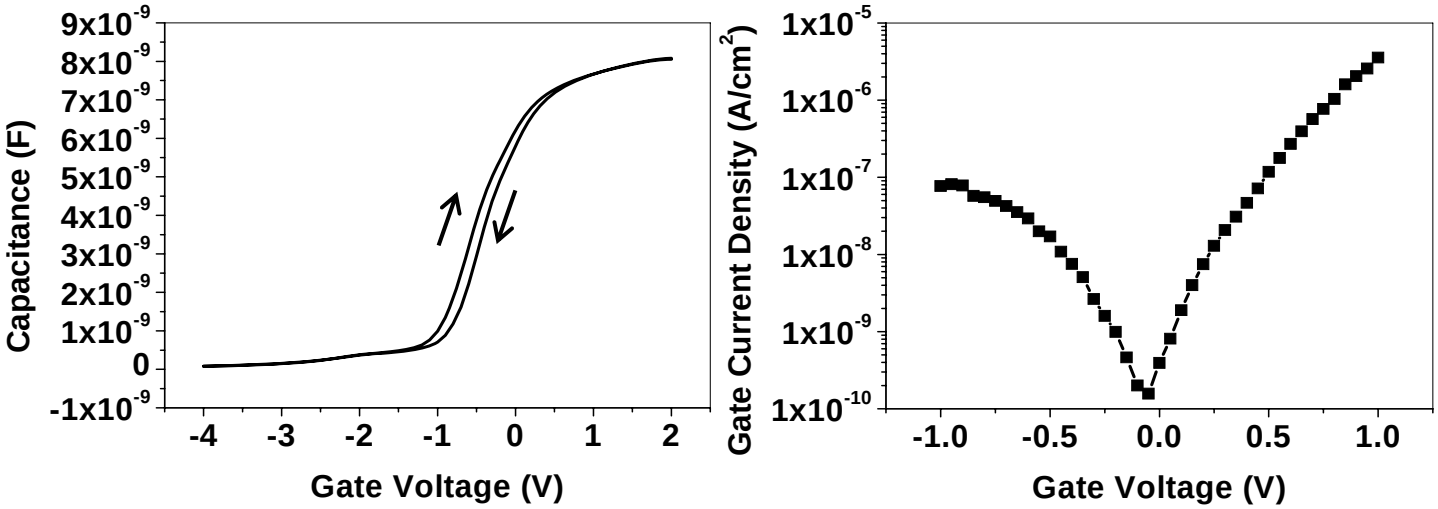


Figure 3.10: (a) C-V and (b) I-V characteristics of a typical MIS device with HfO_2 as the insulator layer.

3.3 Investigation of Crystallization Temperature of Hafnium Dioxide and Hafnium Aluminum Oxide

The leakage current within a high-κ gate dielectric film is typically associated with the crystallization of the high-κ material during high temperature annealing treatment. During device operation, when a voltage is applied at the gate terminal, stray current might start to flow from the gate electrode to the Si substrate via the grain boundaries in the crystallized dielectric film, resulting in the formation of a leakage current path. Despite this crystallization issue encountered in the high-κ material, the gate leakage performance is typically still better than SiO_2 with similar EOT. The gate leakage characteristics of a high-κ material could be further improved if the temperature at which crystallization occurs could be raised.

Both Zr and hafnium (Hf) have almost identical characteristics. This similarity in properties arises from both elements having the same chemical bonding and similar electronic configuration [20], [21]. Besides having the good characteristics associated

with ZrO_2, pure HfO_2 has the additional advantage of having a higher crystallization temperature than pure ZrO_2 [23]. This temperature could be further increased with the introduction of suitable dopants such as aluminum (Al) [24]-[26]. In this aspect, HfO_2 is a slightly better candidate than ZrO_2 as it could preserve the advantage associated with ZrO_2 and yet has the additional potential of having its gate leakage current lowered (due to the delayed occurrence of crystallization).

An experiment, involving the fabrication of two dielectric films, has been carried out to investigate the effect of Al doping on the crystallization temperature of HfO_2. The first film consists of pure HfO_2 obtained by sputtering the Hf target in argon and oxygen ($Ar+O_2$) ambient. The second film consists of HfO_2 doped with Al obtained by co-sputtering Hf and Al targets in the same environment. During sputtering, the Ar and O_2 flow rates were set at 23 sccm and 2 sccm, respectively, and the process was carried out under an operating pressure of 3mTorr. A sputtering power of 200 W (with RF power of 10W) was used. The wafer substrate temperature was set at 350^oC during reactive sputtering followed by post deposition annealing at 400^oC in nitrogen ambient for 5 minutes.

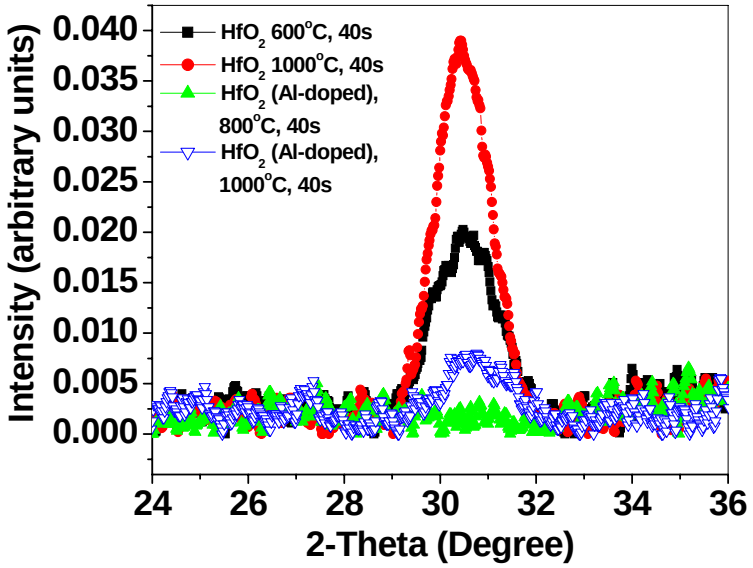


Figure 3.11: XRD spectra of pure HfO_2 after annealing at 600°C and 1000°C and HfO_2 doped with Al after annealing at 800°C and 1000°C. The crystallization temperature of HfO_2 could be raised to 1000°C when it is doped with Al.

Upon the completion of film fabrication, the films were then subjected to high temperature annealing at 600°C, 800°C and 1000°C for 40s. The degree of crystallization was then investigated by XRD after each temperature treatment. From Fig. 3.11, it is observed that when HfO_2 is doped with Al, no crystallization is observed even after 800°C anneal and only a minor trace of crystallization starts to appear after a high temperature anneal of 1000°C. In comparison, for the pure HfO_2 film, crystallization has already taken place at a temperature of 600°C. From this experiment, it can be seen that a 10% incorporation of Al into HfO_2 is an effective way to raise the crystallization temperature up to 1000°C.

3.4 Summary

Structural and electrical characterizations have been performed on the Al/ZrO_2/n-Si MIS devices with EOT of ~2.5 nm. About 60% of the devices fabricated with the optimized process conditions showed leakage current density of less than 2 x 10^{-5} A/cm^2 at 1 V accumulation bias. TEM analysis showed a ~1.7 nm thick interfacial layer (possibly zirconium silicate) and a ~13 nm thick bulk ZrO_2 layer. The difference in the electrical performance of low leakage and high leakage devices is due to the different degrees of crystallization of the bulk ZrO_2 layer. It was found that there was no direct correlation between the interface state density and the leakage current of the Al/ZrO_2/n-Si MIS devices. This could possibly be due to the large physical thickness of the high-κ film which makes the interfacial region less important than the bulk insulator properties in determining the leakage performance of the devices. It was found that only the F-P emission mechanism fit the measured J_g-V_g data between electric fields of 2.0 and 3.2 MV/cm in the interfacial layer (corresponding to $0.7 < V_g < 2$ V). The Schottky emission mechanism, however, does not fit the measured J_g-V_g data at all. For the bulk ZrO_2 layer, both Schottky and F-P emission mechanisms do not fit the measured J_g-V_g data over electric fields in the bulk ZrO_2 from 0.7 to 1.9 MV/cm (corresponding to $0 < V_g < 2$ V).

Capacitor device with another type of high-κ material, HfO_2, has also been fabricated and studied. HfO_2 is also found to be a promising candidate as an alternative gate dielectric material. The crystallization temperature of HfO_2 could be further raised to 1000^{o}C when it is doped with Al to form HfAlO.

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Chapter 4: Nanocrystal Memory Devices with High Dielectric Constant Material as Tunnel Dielectric

The introduction of a high dielectric constant (high-κ) material such as HfO_2 is necessary to address the limitations currently encountered by conventional SiO_2 as the gate dielectric material [1]-[3]. The replacement of SiO_2 in the tunnel dielectric layer and capping oxide (of a nanocrystal memory device) with a high-κ material also seems to provide a viable solution for improved nanocrystal memory device performance. In this chapter, the actual integration of the high-κ material into the nanocrystal memory device will be investigated. The performance of the device with ~5nm (EOT) thick high-κ HfO_2 tunnel dielectric is first compared with a similar device structure with 5nm thick SiO_2 tunnel dielectric. In the subsequent section, the HfO_2 tunnel dielectric is further reduced to an EOT of 1.9nm, a thickness well below the 2.5nm lower bound limit possible for conventional SiO_2 in the Ge nanocrystal memory. A significant improvement in device performance could be observed in both cases.

4.2 Fabrication and Characterization of Nanocrystal Memory with Hafnium Dioxide as Tunnel Dielectric (EOT = 4.8nm)

In this section, the performance of the nanocrystal capacitor device with ~5nm (EOT) thick high-κ hafnium dioxide (HfO_2) tunnel dielectric is first compared with a similar device with 5nm thick SiO_2 tunnel dielectric. For this purpose, the 4.8nm (EOT) thick HfO_2 tunnel dielectric film (fabricated and characterized earlier in Section 3.2) is then subjected to further processing for actual nanocrystal memory capacitor device implementation.

The following processing steps were further carried out to fabricate the trilayer insulator structure. A thin layer (4nm) of Ge was sputter-deposited (at a power of 50W and at an operating pressure of $3.3x10^{-3}$Torr) on top of the 4.8nm (EOT) thick HfO_2 tunnel dielectric film, followed by the deposition of a 50nm thick SiO_2 cap layer. The device was then rapid thermal annealed at 1000^oC for the formation of Ge nanocrystals in the middle layer [4]-[7]. A cap layer thickness of 50nm was used to ensure Ge out-difussion was completely minimized during annealing, so that the charge storage capability of the device could be preserved. Table 4.1 describes the structure of this trilayer device (HK4-8) as well as the control device (RTO5) used for comparison of device performance.

Table 4.1: The configurations of the trilayer structures used for comparison of device performance.

Device	**Layer 1**	**Layer 2**	**Layer 3**
RTO5	5nm RTO	4nm Ge	50nm SiO_2
HK4-8	4.8nm (EOT) HfO_2	4nm Ge	50nm SiO_2

A high-resolution transmission electron microscope (HRTEM) was used to obtain the cross-sectional TEM images of the completed nanocrystal memory devices. The HRTEM micrograph in Fig. 4.1 shows that the sputter-deposited and annealed high-κ film consists of a ~2.3 nm thick interfacial layer and a ~2.9 nm thick bulk HfO_2 layer. From Fig. 4.1, it could be seen that the nanocrystals are very well-formed on the HfO_2 layer and there is no significant penetration of the Ge nanocrystals into the silicon substrate.

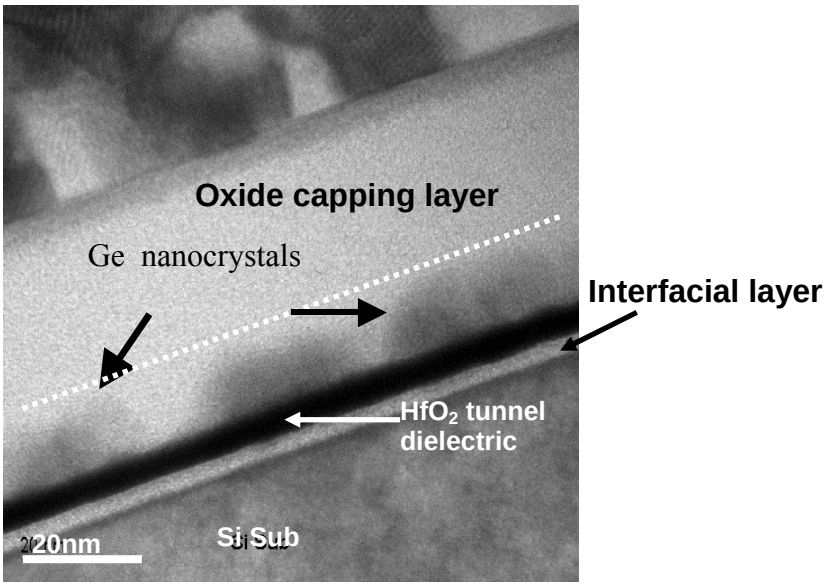


Figure 4.1: Cross-sectional HRTEM image of the nanocrystal memory device HK4-8.

4.1.1 Charge Storage Studies

The charge storage capability of the nanocrystal device is determined by studying the difference in the C-V curves before and after charging [8]. High frequency (100 kHz) forward and reverse sweep C-V measurements were carried out using a HP4284 impedance analyzer. The device was first held at a gate voltage of -2V until saturation of positive charge storage has been reached, followed by a gate voltage sweep from –2V to +2V. At the end of this forward sweep, the device was held at a gate voltage of +2V until saturation of negative charge storage has been reached and then followed by a reverse gate voltage sweep from +2V to –2V. In this way, the gate voltage (V_g) sweep range was gradually increased from $-2V<V_g<2V$ to $-16V<V_g<16V$.

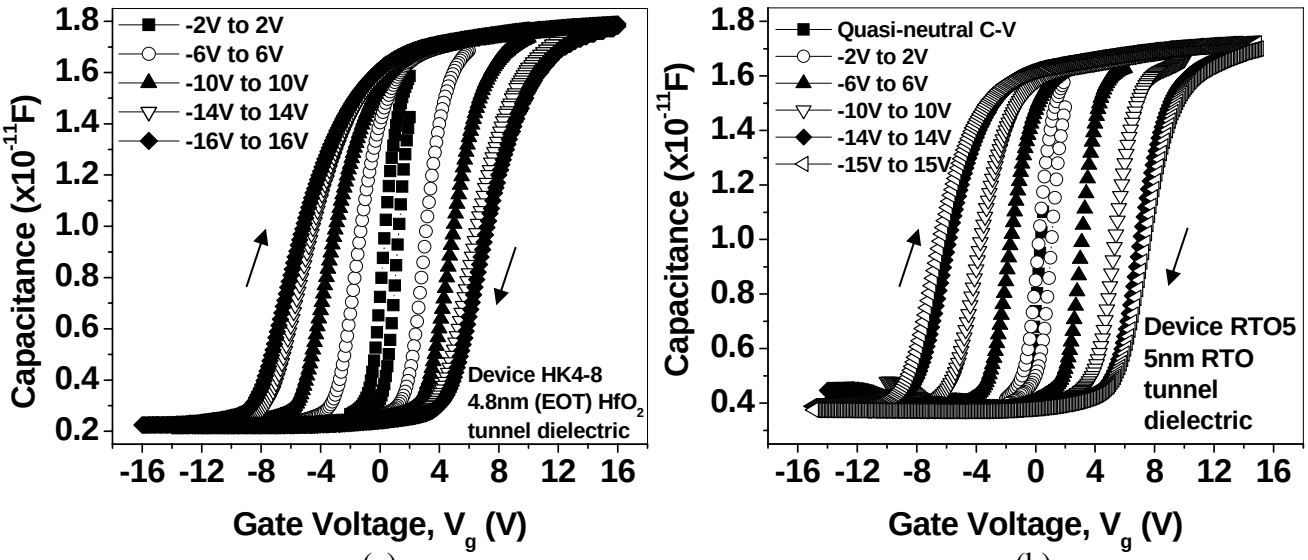


Figure 4.2: C-V characteristics of (a) Device HK4-8 and (b) Device RTO5 showing clock-wise hysteresis. The gate voltage sweep range was gradually increased from $-2V<V_g<2V$ to $-16<V_g<16V$.

The C-V curves of these sweeps are shown in Fig. 4.2. The C-V characteristics of the trilayer device with 4.8nm (EOT) thick HfO_2 tunnel dielectric (Device HK4-8) and device with 5nm conventional RTO as tunnel dielectric (Device RTO5) are shown in Fig. 4.2(a) and (b), respectively. A clockwise hysteresis is observed in the C-V curves of the n-substrate devices, thus indicating charge storage or memory effect in the nanocrystal devices. A plot summarizing the charge storage capability with respect to the gate voltage sweep range is shown in Fig. 4.3. As evident from the almost identical data plots in Fig. 4.3, the charge storage capability is not compromised when the RTO tunnel layer is replaced by the high-κ (HfO_2) material.

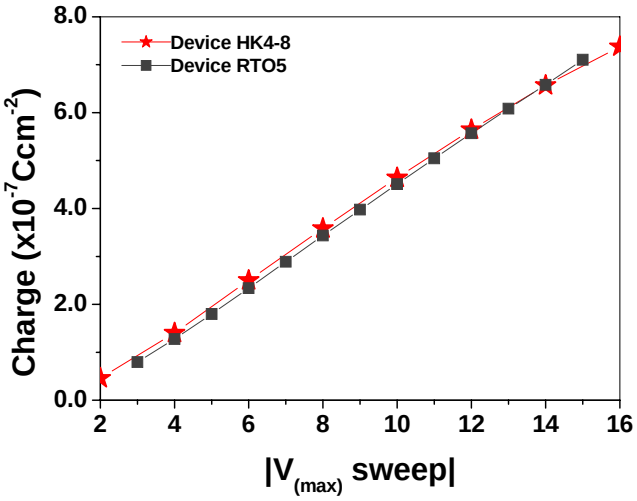


Figure 4.3: A plot summarizing the charge storage capability with respect to the gate voltage sweep range for Device RTO5 and Device HK4_8.

Further tests were carried out on the trilayer device with 4.8nm (EOT) thick HfO_2 tunnel dielectric (Device HK4-8). The gate voltage sweep range was gradually increased to investigate the onset of charge storage saturation, until the occurrence of device breakdown. Breakdown occurs when the C-V sweep range is increased beyond the $-26<V_g<26V$ range. Figure 4.4(b) shows the concentration of extracted negative and positive trapped charges with respect to gate bias. The concentration of the trapped charges is estimated from the change of flat band (ΔV_{FB}) with respect to its uncharged state (i.e., the quasi-neutral C-V condition, which is described further below), multiplied by C_i/q, where C_i is the insulator capacitance measured in accumulation and q is the elementary charge. It is observed that saturation of the charge storage occurs for a gate sweep magnitude of about 20 V, as seen from the occurrence of the first step or plateau in Fig. 4.4(b). However, onset of the second step or plateau in the charge storage versus gate voltage curve (which would indicate Coulomb Blockade) was not observed as the device broke down at $V_g = 26V$.

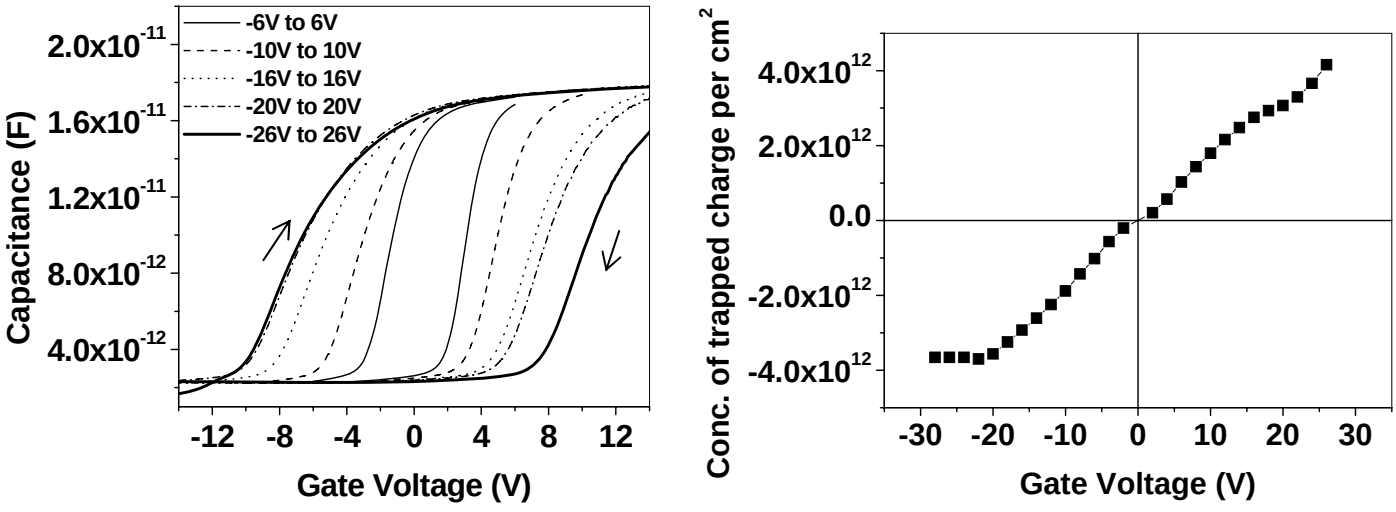
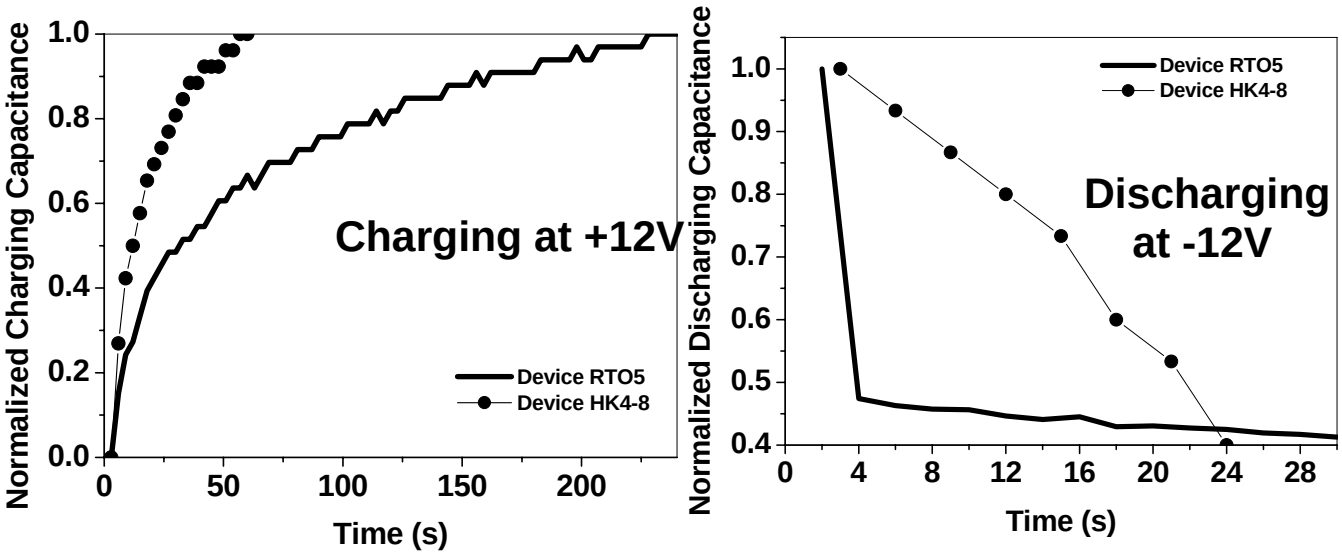


Figure 4.4: (a) C-V characteristics of device HK4-8. The gate voltage sweep range was gradually increased till the occurrence of device breakdown (beyond the $-26<V_g<26V$ sweep range). (b) Concentration of negative and positive trapped charges versus gate bias for device HK4-8.

4.1.2 Charging and Discharging Time Studies

The charging rate of the nanocrystal capacitor memory device with 4.8nm (EOT) thick HfO_2 tunnel dielectric (Device HK4-8) was compared with the device with 5nm of conventional RTO tunnel dielectric (Device RTO5). During charging, a voltage of +12V is applied at the gate terminal. It was found that Device HK4-8 took less than 60s to reach saturation in the capacitance value whereas Device RTO5 took about 240s to reach saturation. The faster charging rate of Device HK4-8 could be attributed to the lower barrier height of the high-κ HfO_2 material with silicon, as compared to SiO_2 with silicon [8].



(a) (b)

Figure 4.5: Study of Charging and discharging rate of the two devices. (a) shows the charging characteristics of the devices when a gate voltage of +12V is applied (b) shows the discharging characteristics when the gate voltage is abruptly switched to –12V after charging.

After fully charging the device at +12V, the gate voltage was abruptly switched to -12V with the discharge capacitance monitored against elapsed time. From Fig. 4.5(b), it could be seen that Device RTO5 took about 4s to lose half of its initial capacitance value whereas Device HK4-8 took about 22s to reach half its initial capacitance value. From this result, it could be inferred that Device HK4-8 is able to retain its charge better than Device RTO5.

4.1.3 Charge Retention Studies

For evaluating the charge retention performance, the devices were first fully charged up at a fixed positive gate voltage until saturation in the gate capacitance was observed, followed by switching abruptly to a constant negative discharging voltage. Similar to the *C-t* results presented by Kim *et al.* [10], the normalized capacitance in our

C-t plot was calculated based on the formula $\frac{C(t)-C_{sat}}{C(t=0)-C_{sat}}$, where C_{sat} is the saturation capacitance taken at the end of the *C-t* discharging experiment while $C(t = 0)$ is the initial capacitance at the start of the discharging experiment. The retention time is defined as the time for the normalized capacitance to decrease to 50% of its initial value at time $t = 0$.

In our charge retention capability study, the devices were first fully charged up at 12V until a saturation in capacitance value has been reached. After which the bias voltage was switched abruptly to the discharging voltage, the latter ranging from -12 V to -2 V. With C(t=0) being defined as the initial capacitance at the start of the discharging experiment, the retention time was defined as the time for the normalized capacitance to decrease to 50% of C(t=0).

Figures 4.6 shows the retention characteristics (retention time plotted against discharging voltage) of the trilayer insulator structure nanocrystal memory device with different types of tunnel dielectric. Both HfO_2 and SiO_2 tunnel dielectric have the same equivalent-oxide-thickness of ~5nm and similar middle layer and cap layer thickness. It is observed that the device with HfO_2 as the tunnel dielectric has a longer peak retention time of 300 s as compared to 148 s for the device with silicon dioxide as the tunnel dielectric.

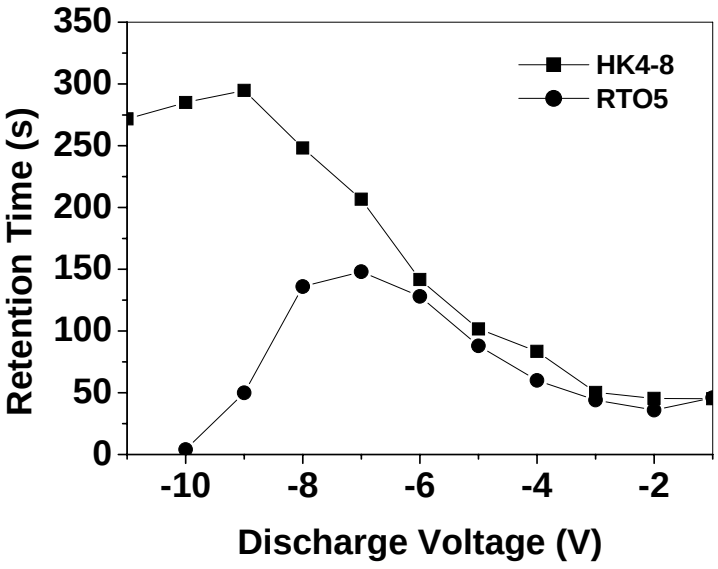


Figure 4.6: Retention characteristics of trilayer insulator structure nanocrystal memory devices for different types of tunnel dielectric. Both HfO_2 and SiO_2 tunnel dielectric have the same equivalent-oxide-thickness of 5nm. The middle and cap layer thickness of both devices are the same.

4.2 Further Scaling of Hafnium Dioxide Tunnel Dielectric to EOT of 1.9nm and Performance Characterization

From the above sections, it could be seen that when the SiO_2 tunnel dielectric is replaced with a high-κ material, no compromise in total charge storage resulted, a faster charging speed could be achieved due to the lower barrier height of the high-κ material with silicon and a better charge retention could be attained due to the physically thicker high-κ layer. In this section, the thickness of the high-κ HfO_2 tunnel dielectric will be further reduced from an EOT of 4.8nm to 1.9nm (Device HK1-9) and studied. This thickness is well below the 2.5nm lower bound limit for conventional SiO_2 in the Ge nanocrystal memory below which Ge penetration would have occurred and no proper charge storage could be obtained.

4.2.1 Structural Characterization

The cross-sectional TEM images of Device RTO2-5 (with 2.5nm thick SiO_2 tunnel dielectric grown by rapid thermal oxidation or RTO) and Device HK1-9 (device with 1.9nm (EOT) thick high-κ HfO_2/SiO_xN_y tunnel dielectric) are shown in Fig. 4.7.

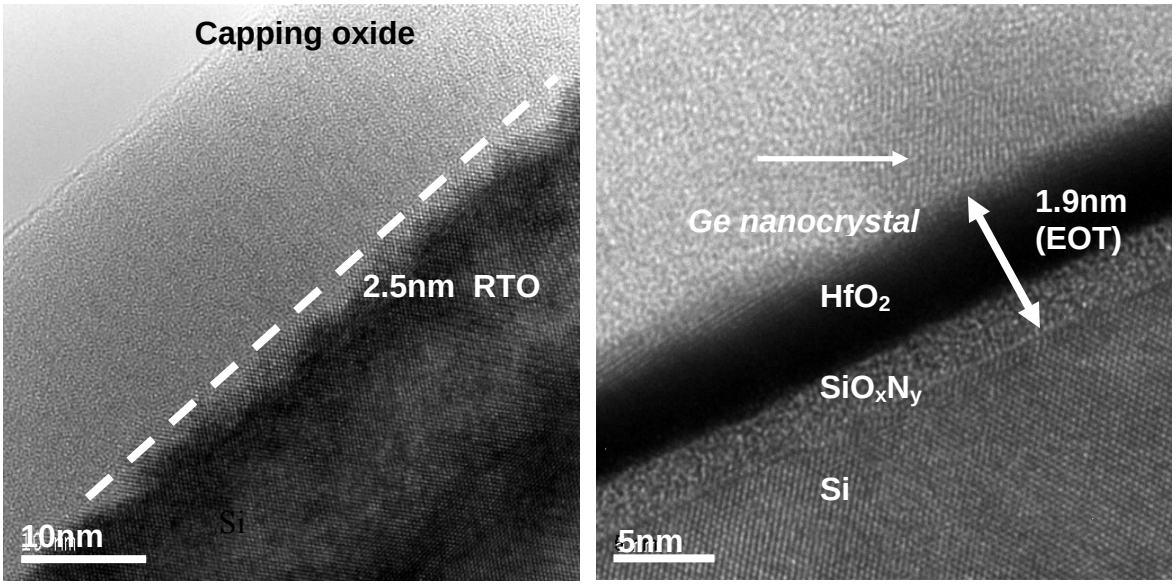


Figure 4.7: Cross-sectional TEM image of (a) device RTO2-5 and (b) device HK1-9. Note the absence of Ge nanocrytals and the uneven RTO-Si interface caused by the Ge penetration in device RTO2-5.

For Device HK1-9, the surface nitridation was preformed at 700^{o}C for 1 minute in an NH_3 ambient while the HfO_2 film was prepared by MOCVD at 400^{o}C using $Hf(OC(CH_3)_3)_4$ precursor contained in a bubbler system, which was bubbled and delivered by Ar.

Figure 4.7(a) shows the TEM image of device RTO2-5, where the formation of Ge nanocrystals is not successful due to the penetration and diffusion of Ge through the thin 2.5nm thick SiO_2 layer during the 1000 °C rapid thermal anneal (RTA) step. The

original pure Ge layer has disappeared after the RTA step and no nanocrystals could be detected in the device. The RTO-Si interface also appears to be rather uneven. Due to the steep Ge concentration gradient between the middle layer and the Si substrate and the thin RTO barrier for diffusion, it is likely that most of the Ge may have diffused into the Si substrate (through the 2.5nm thick RTO) during RTA at 1000 °C [6]. Consequently, no (or very few) nanocrystals were formed in the MIS structure. The uneven RTO-Si interface may be due to the pronounced diffusion of Ge from the middle layer to the Si substrate. The absence of nanocrystals would result in the inability of the structure to store charge as the charge storage capability is generally dependent on the nanocrystal density. Figure 4.7(b) shows the TEM image of well-formed Ge nanocrystal in device HK1-9. The high-κ tunnel dielectric stack of HfO_2/SiO_xN_y is effective in preventing the Ge penetration due to its larger physical thickness, although it has a much smaller EOT than device RTO2-5. The ability of high-κ material to prevent Ge penetration is further confirmed by the SIMS result in Fig. 4.8.

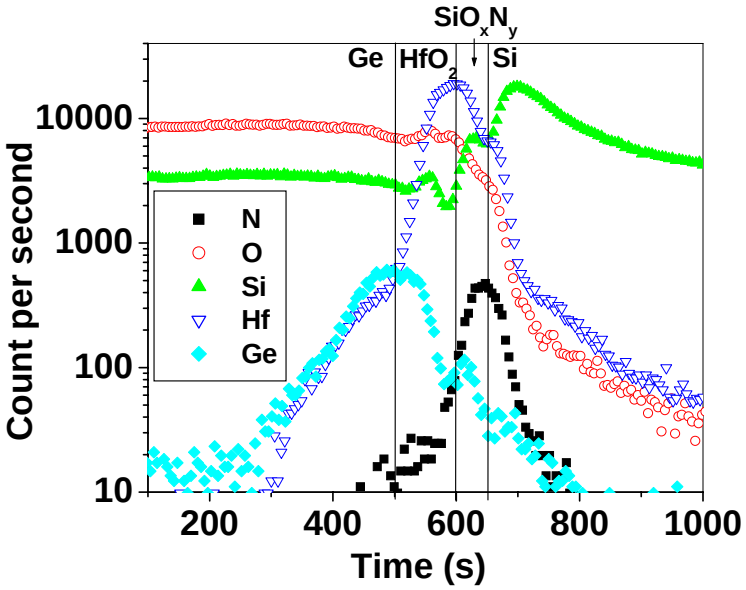


Figure 4.8: SIMS result (of device HK1-9) showing that Ge does not penetrate and diffuse significantly into the silicon substrate. The HfO_2 layer provides a good blocking platform for the formation of Ge nanocrystals.

The performance of the device with reduced tunnel dielectric electrical thickness was then studied. Table 4.2 shows the configurations of the various trilayer structures (with different tunnel dielectric thickness) used for comparison of device performance in the study.

Table 4.2: The configurations of the trilayer structures (with tunnel dielectric thickness further reduced) used for comparison of device performance.

Device	**Layer 1**	**Layer 2**	**Layer 3**	**Remarks**
RTO2-5	2.5nm RTO	4nm Ge	50nm SiO_2	Cannot be used for device performance comparison as no Ge crystals were formed.
RTO5	5nm RTO	4nm Ge	50nm SiO_2	Used in place of RTO2-5 for performance studies.
HK1-9	1.9nm (EOT) HfO_2	4nm Ge	50nm SiO_2	High-κ device with tunnel dielectric reduced from 4.8nm to 1.9nm (EOT).

4.2.2 Charge Storage

A typical high frequency C-V characteristic of device HK1-9 (1.9nm EOT HfO_2) is shown in Fig. 4.9(a). The gate voltage sweep magnitude was gradually increased from 1 V to 3.4 V, in steps of 0.2 V. A holding time of 120 s was applied before commencing each *C-V* sweep. This is to ensure that the charging and discharging processes in the devices have reached a steady state (i.e., the flat-band voltage shift has saturated). In the –3.4 V to 3.4 V gate voltage sweep range, the n-substrate device shows a clockwise C-V hysteresis with a width of ~2.76 V, corresponding to a hysteresis area of 1.74 x 10^{-7} C cm^{-2} and an estimated nanocrystal density of 5.44 x 10^{11} cm^{-2} [5]. This indicates that a significant amount of charge storage could already be obtained over such a small gate voltage sweep range.

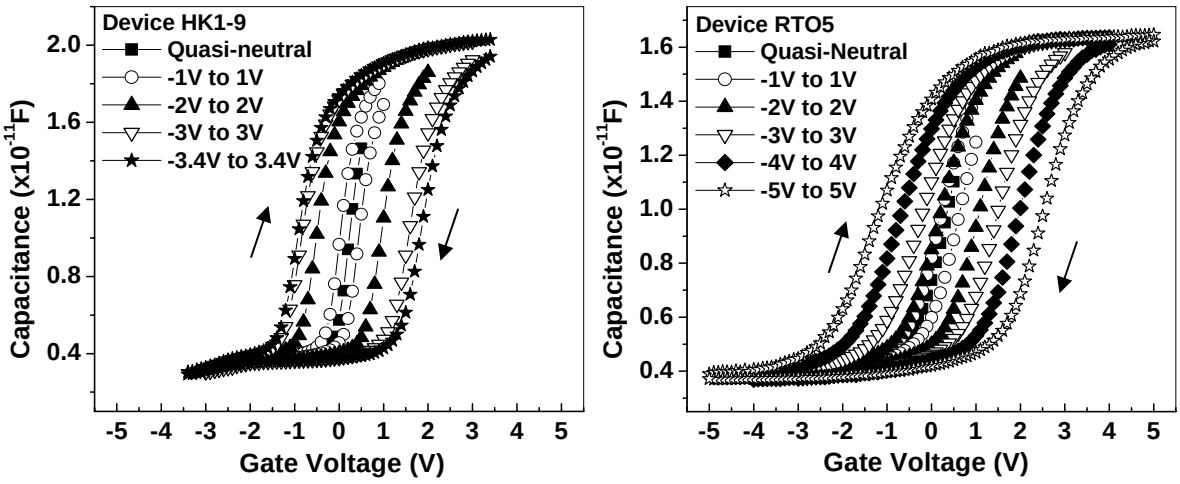


Figure 4.9: High frequency *C-V* characteristics of (a) device HK1-9 and (b) device RTO5. The quasi-neutral *C-V* curves for the respective devices were obtained by restricting the gate bias to a very narrow range to minimize charging up of the Ge nanocrystals.

In performing subsequent electrical characterizations, our focus will be on this lower gate voltage regime as nanocrystal memory devices, unlike conventional floating gate tunnel oxide memory devices, would typically be operated with smaller program and erase voltages.

The charge storage capability of devices with RTO and high-κ tunnel dielectric layers is compared in Fig. 4.9. As the device with a 2.5-nm thick RTO layer (device RTO2-5) does not exhibit significant charge storage capability because of the Ge penetration effect, comparison of charge storage and retention of the high-κ device HK1-9 is thus performed with a 5-nm thick RTO layer device (device RTO5). The physical thickness of the tunnel dielectric layer of device RTO5 is comparable to that of high-κ device HK1-9, and device RTO5 also shows good charge storage characteristics (see Fig. 4.9(b)). For device RTO5, when the gate voltage is swept from –5 V to +5 V, the area enclosed by the hysteresis loop is 1.80×10^{-7} C cm^{-2} and the corresponding nanocrystal density was estimated to be 5.63×10^{11} cm^{-2}. It would be worthwhile to note that a similar amount of charge storage could be obtained from device HK1-9 (see previous paragraph) over a smaller gate voltage sweep range of –3.4 V to +3.4 V. This is due to the smaller EOT of device HK1-9 and the lower barrier height (as compared to SiO_2) of the high-κ layer which allows easier tunneling of charge carriers from the substrate into the nanocrystals.

4.2.3 Charge Retention Studies

It should be noted that the total amount of charge storage for device HK1-9 over the gate voltage sweep range of –3.4 V to +3.4 V is similar to that for device RTO5 over the gate voltage sweep range of –5 V to 5 V. Hence, in the charge retention time studies, device HK1-9 was first charged at +3 V and then discharged at voltages ranging from –3 V to 0 V. For device RTO5, the sample was charged at +5 V followed by discharging at voltages ranging from –5 V to 0 V. It is seen from Fig. 4.10 that device HK1-9 shows better charge retention performance, with generally longer charge retention times, than device RTO5.

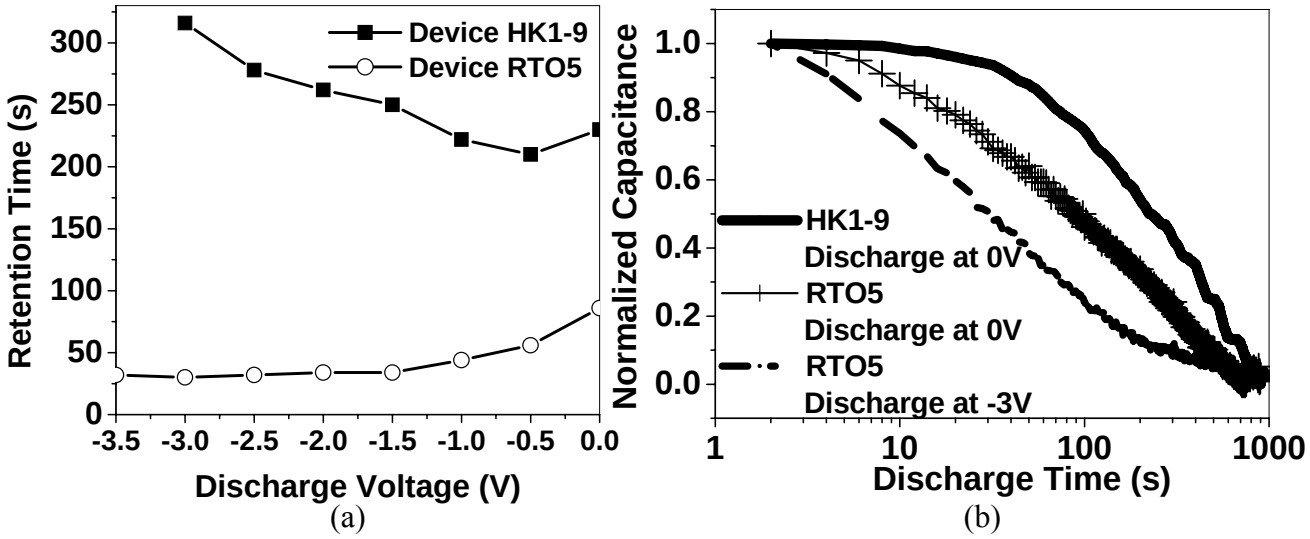


Figure 4.10: Retention characteristics of devices RTO5 and HK1-9: (a) Comparison of retention time versus discharge bias of both devices and (b) Some representative normalized *C*-*t* curves during discharge of devices RTO5 and HK1-9 at a constant discharge voltage of either 0 V or –3 V as indicated.

4.3 Summary

From the experiments performed in this chapter, it was seen that when the nanocrystal memory device with 5nm thick SiO_2 tunnel dielectric was replaced with a high-κ HfO_2 material of equivalent electrical thickness, no compromise in total charge storage was resulted, a faster charging speed could be achieved due to the lower barrier height of HfO_2 with silicon and better charge retention characteristics could be attained due to the physically thicker HfO_2 layer.

The EOT of the HfO_2 dielectric was further reduced from ~5nm to 1.9nm (Device HK1-9) and studied. This thickness is well below the 2.5nm lower bound limit for conventional SiO_2 below which Ge penetration would have occurred and no proper charge storage could be obtained. For the nanocrystal memory device with HfO_2 of 1.9nm EOT as the tunnel dielectric, better charge storage capability (in terms of a lower program voltage) could be obtained, due to the smaller EOT and lower barrier height (as compared to SiO_2) of the high-κ HfO_2 layer, allowing easier tunneling of charge carriers from the substrate into the nanocrystals. The high-κ trilayer structure also shows better charge retention performance than the RTO (SiO_2) trilayer structure even though the EOT of the high-κ tunnel dielectric is smaller than that of the RTO tunnel dielectric.

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Chapter 5: High Dielectric Constant Material as Capping Layer for Improved Electric Field Coupling in Nanocrystal Memory Devices

As presented in Chapter 4, the replacement of SiO_2 with a high-κ material for the tunnel dielectric results in no compromise in charge storage capability, improvement in charging rate and better charge retention characteristics. In this chapter, further investigations on the possibility of device performance enhancement by replacing the capping layer with high-κ material are carried out. In our earlier work, devices with 50nm thick capping SiO_2 were typically used to ensure Ge out-difussion was completely minimized with charge storage capability safely preserved. However, higher programming voltage is required as a result of the thick SiO_2 capping layer. Better gate coupling factor (and hence lower programming voltage) could be achieved either by using a physically thinner SiO_2 capping layer or using a high-κ capping material to replace the conventional SiO_2.

5.1 Experimental Details

To investigate the role of the gate coupling factor, three different capacitor devices have been fabricated. Device A is fabricated with conventional SiO_2 as the capping layer but with thickness reduced from 50nm to 20nm. It would be interesting to investigate if such a thin layer of SiO_2 is able to prevent Ge out-diffusion effectively. Device B is fabricated with 20nm of high-κ hafnium aluminum oxide (HfAlO) as the capping layer. Device C is similar to Device B but with the HfAlO capping layer further reduced from 20nm to 10nm. A summary of the configurations of the trilayer structures

with different capping material/thickness, used in this section for comparison of device performance, is given in Table 5.1

Table 5.1: The configurations of the trilayer structures (with different capping material/thickness) used for comparison of device performance.

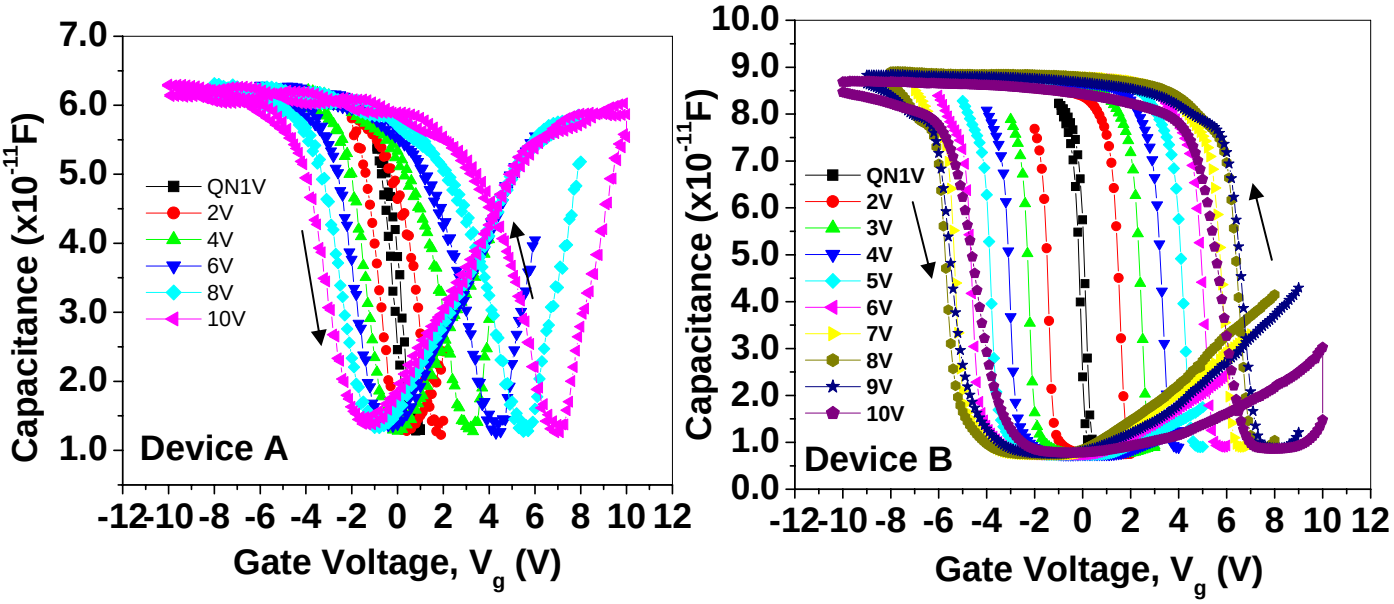
Device	Layer 1	Layer 2	Layer 3	Remarks
A	2nm (EOT) HfAlO	4nm Ge	20nm SiO_2	Good electric field coupling
B	2nm (EOT) HfAlO	4nm Ge	20nm HfAlO	Best electric field coupling
C	2nm (EOT) HfAlO	4nm Ge	10nm HfAlO	Cap layer too thin. No charge storage

5.2 Comparison of Performance for Devices with Different Types of Capping Layer

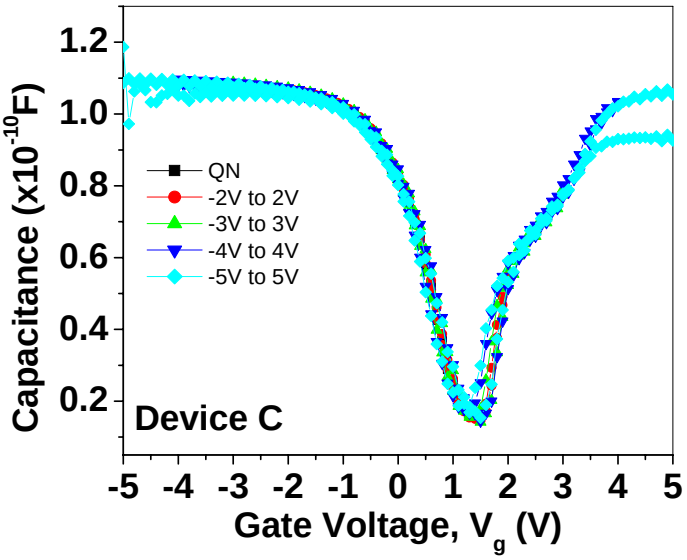
After device fabrication, capacitance-voltage (C-V) measurements followed by retention time studies were then performed on the devices. The performance of these devices (with reduced capping thickness) will also be compared with some of the devices reported in the earlier chapters.

5.2.1 Charge Storage Analysis

In the charge storage capability study, high frequency (100kHz) C-V measurements were conducted on the three devices. The device was first held at a gate voltage of -1V for 240s to allow saturation of positive charge storage, followed by a gate voltage sweep from –1 V to +1V. At the end of this forward sweep, the device was held at a gate voltage of +1 V for 240 s to allow saturation of negative charge storage and then followed by a reverse gate voltage sweep from +1V to -1V. The gate voltage sweep range was then increased from $-1V<V_g< 1V$ to $-10V<V_g<10V$ in steps of 1V. The C-V characteristics of the three devices are shown in Fig. 5.1.



(a) (b)



(c)

Figure 5.1: Forward/reverse C-V characteristics of the three devices for various sweep ranges. C-V Characteristics of (a) Device A (device with 20nm SiO_2 capping layer), (b) Device B (device with 20nm HfAlO capping layer) and (c) Device C (device with 10nm HfAlO capping layer). The capacitor area is $4x10^{-4}cm^2$ for the three devices. A holding time of 240s is applied before the commencement of each gate voltage sweep.

The rising C-V characteristic in the inversion bias region (somewhat similar to a low frequency C-V response) is due to an ample supply of minority carriers (electrons) being able to respond to the applied high frequency AC signal. This is because the capacitors are located on the same wafer as the transistors and the capacitor devices are also exposed to source/drain n^+ implantation which provided the source of minority carriers.

From Fig. 5.1(a), it could be seen that Device A exhibits an anti-clockwise hysteresis, as well as gradual increase of C-V hysteresis width with respect to increased gate voltage sweep range. The anti-clockwise hysteresis for a p-substrate device indicates charge storage and hence suggests the presence of nanocrystals, similar to what was repeated previously in the earlier chapters. It could hence be inferred that 20nm of SiO_2 is sufficient to prevent the out-diffusion of Ge into the ambient during high temperature (1000^oC) rapid thermal annealing (RTA) to form the Ge nanocrystals. From Fig. 5.1(b), it could be seen that Device B (with 20nm of HfAlO as capping layer) is able to provide a larger hysteresis width (compared to Device A) for a similar gate voltage sweep range. This could be attributed to the higher gate coupling factor introduced to the tunnel oxide layer when HfAlO (a higher-κ material than SiO_2) is used as the capping layer. The high-κ capping layer also reduces the overall gate capacitance of the trilayer structure. From Fig. 5.1(c), it is seen that no C-V hysteresis could be obtained for Device C. This suggests that a physical thickness of 10nm HfAlO is too thin to prevent the out-diffusion of Ge during RTA. No charge storage could be obtained for Device C due to the absence of Ge nanocrystals or charges leaking away rapidly the moment it is stored during the C-V sweep.

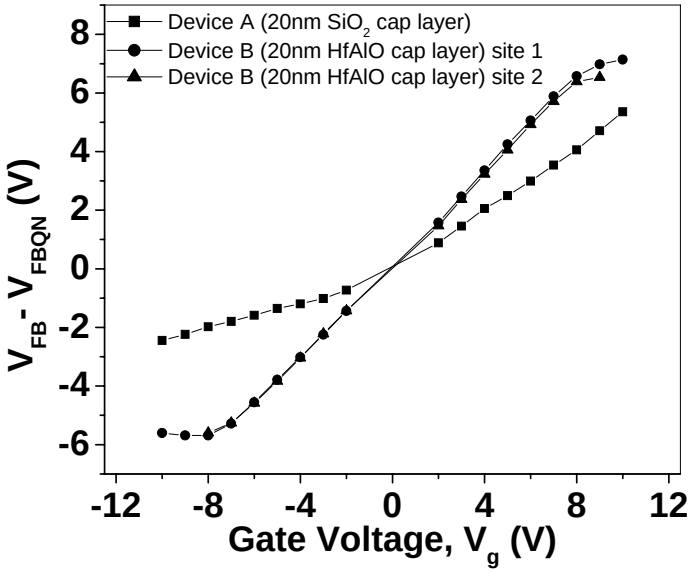


Figure 5.2: Plot of flatband voltage shift with respect to the gate voltage sweep range for Device A and Device B. The area of the device is $4x10^{-4}cm^2$. V_{FB} and V_{FBQN} denote the flatband voltages of the charged and uncharged (quasi-neutral) device, respectively.

The flatband voltage shift with respect to the gate voltage sweep range is summarized in Fig. 5.2. It could be seen that Device B (device with HfAlO as the capping layer) provides the highest amount of flatband voltage shift at a given gate voltage sweep range. The two curves obtained from two different sites on Device B also shows that Device B has good repeatability over a wide range of gate voltage sweep range.

An analysis has also been carried out to investigate the charge storage capability of the devices. The results are shown in Figure 5.3. It could be seen that at a given gate voltage sweep range, the charge storage of Device B (device with 20nm of HfAlO as capping layer) outperforms that of the Device A (device with 20nm of SiO_2 as capping layer) by approximately 2.6 times. A linear increase of charge storage with respect to gate voltage sweep range could also be observed before saturation of charge storage sets in at higher sweep voltages.

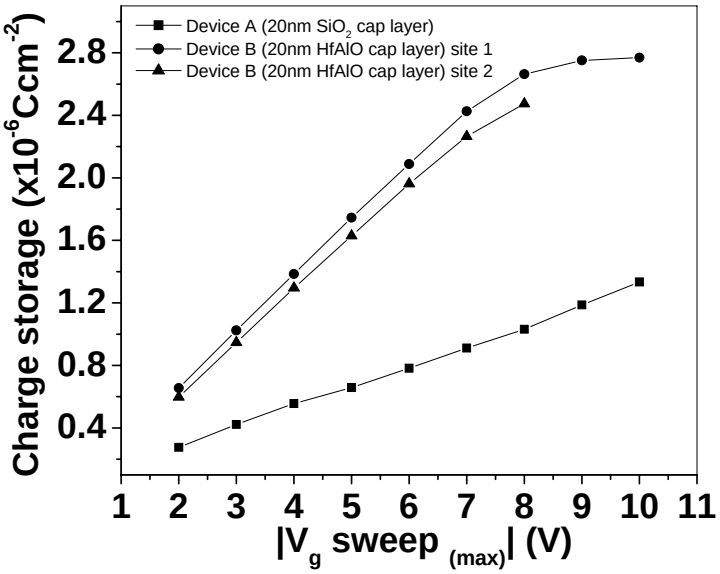


Figure 5.3: Plot of charge storage with respect to the gate voltage sweep range for Device A and Device B.

An attempt has also been made to compare the charge storage capability of Devices A and B with some of the devices (Device HK4-8 and Device HK1-9) reported previously in Chapter 4. Table 5.2 summarizes the comparison of charge storage capability of the different devices.

Table 5.2: A summary of the structures of the fabricated devices and comparison of their charge storage capability.

Device	**Layer 1 High-κ material**	**Layer 2**	**Layer3**	**Ranking in terms of charge storage capability**
HK4-8	4.8nm (EOT)	4nm pure Ge	50nm SiO2	4 (moderate)
HK1-9	1.9nm (EOT)	4nm pure Ge	50nm SiO2	3 (good)
A	2nm (EOT)	4nm pure Ge	20nm SiO2	2 (better)
B	2nm (EOT)	4nm pure Ge	20nm HfAlO	1 (best)
C	2nm (EOT)	4nm pure Ge	10nm HfAlO	Not applicable.

The plot of charge storage with respect to gate voltage sweep range for these devices is shown in Fig. 5.4. Both Device HK4-8 and Device HK1-9 in the earlier work have 50nm thick SiO_2 as capping layer but with tunnel dielectric thickness of 4.8nm (EOT) and 1.9nm (EOT), respectively. For devices HK4-8 and HK1-9, a marginal improvement in charge storage (at a given sweep voltage range) is observed when the tunnel dielectric thickness is reduced from 4.8nm to 1.9nm. This improvement is due to the ease of tunneling of charge carriers from the Si substrate into the Ge nanocrystals associated with reduced tunnel dielectric thickness.

With the tunnel dielectric thickness maintained at ~2nm (EOT), but with the SiO_2 capping oxide reduced from 50nm (Device HK1-9) to 20nm (Device A), a significant charge storage improvement could be obtained. Finally, when the 20nm SiO_2 (Device A) capping layer is replaced with 20nm of HfAlO (Device B), an even more pronounced charge storage enhancement could be seen.

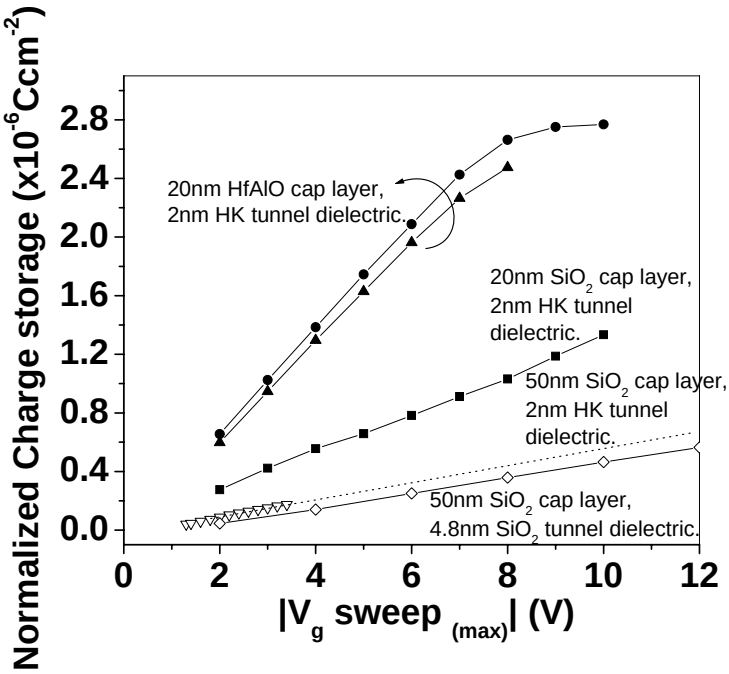


Figure 5.4: Plot of charge storage with respect to the gate voltage sweep range for Device A and Device B as well as devices fabricated in our earlier work (Device HK4-8 and Device HK1-9).

In summary, when the electric field coupling factor is improved by replacing the 20nm thick SiO_2 capping layer with 20nm of HfAlO, a very significant charge storage improvement could be obtained.

5.2.2 Charge Retention Capability Studies

A charge retention capability study has also been carried out on Device A (device with 20nm of SiO_2 capping layer) and Device B (device with 20nm of HfAlO capping layer). The devices were first fully charged up at 5V for 240s, as manifested by the saturated capacitance value in the C-t charging curve. After this, the bias voltage was switched abruptly to the discharging voltage, the latter ranging from -5 V to 0.5V. With C_{max} being defined as the initial capacitance at the start of the discharging experiment, the retention time was defined as the time for the normalized capacitance to decrease to 50% of C_{max}. The normalized discharging characteristics for Devices A and B are shown in Fig 5.5.

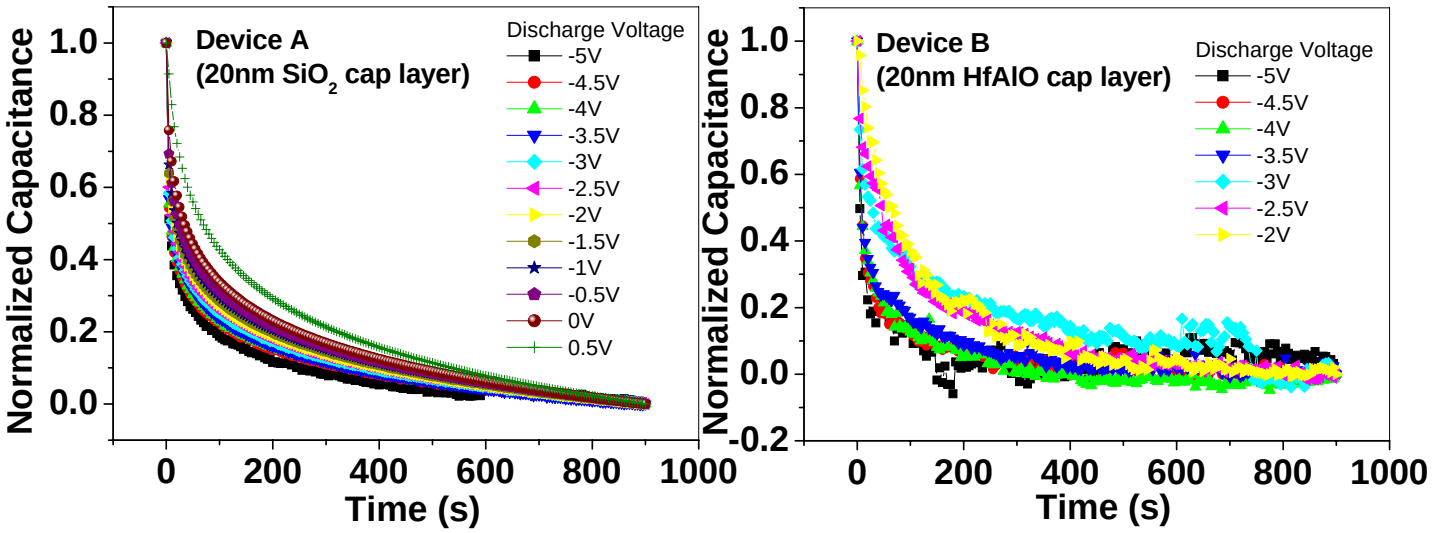


Figure 5.5: Charge retention characteristics of Device A (device with 20nm SiO_2 capping layer) and Device B (device with 20nm HfAlO capping layer). Discharge characteristics of (a) Device A and (b) Device B.

Figure 5.6 shows the retention characteristics (retention time plotted against discharging voltage) of the trilayer insulator structure nanocrystal memory device with two different types of capping layer. Both HfAlO and SiO_2 capping layers have the same physcial thickness of 20nm and similar middle (Ge) layer and tunnel dielectric thickness have been used for both structures. It is observed from Fig. 5.6 that the device with HfAlO as the capping oxide layer (Device B) has a better charge retention capability as compared to the device with silicon dioxide as the capping oxide (Device A) for discharge voltage >-3.5V.

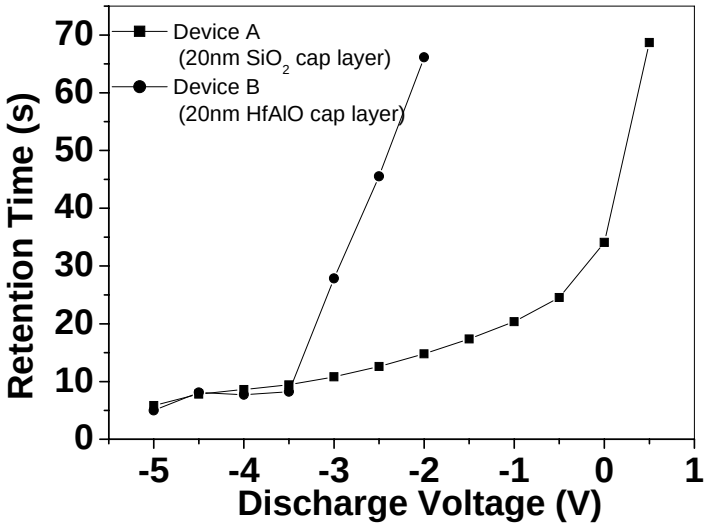


Figure 5.6: Plot of retention time over the discharge voltage range for Device A and Device B.

The reason for better retention characteristics in the smaller negative gate voltage (-2V to –3.5V) seen in Device B could be due to the inherent polarization effect in the high-κ capping material. When Device B is initially charged at +5V for 240s, the electrons from the substrate are attracted into the Ge nanocrystals (as represented by the shaded dots in Fig. 5.7). At the same time, the high-κ capping layer is polarized in a

direction as shown in Fig, 5.7(a). At the end of 240s, when the gate voltage is abruptly switched to a negative voltage (for example V_g = -3V) for discharging, the mildly polarized high-κ capping layer is unable to return to equilibrium immediately and the positive charges in the dipoles of the polarized material would help to prevent some of the electrons (previously stored in the nanocrystals) from tunneling back to the Si substrate easily (as represented by the shaded nanocrystal dots remaining in Fig. 5.7(b)). This polarization effect results in a slightly smaller discharge electric field being seen by the Ge nanocrystals (as shown in Fig. 5.7(b)). The influence from the positive charges in the high-κ capping layer would also cause the number of electrons to fluctuate during the discharge from the nanocrystals to the Si substrate, resulting in a less smooth discharging characteristic for Device B than Device A. This effect is evident from the discharge capacitance curves previously shown in Fig. 5.5.

On the other hand, for Device A, as the amorphous SiO_2 does not exhibit this polarization effect, there would be no opposing field to offset the discharging voltage, causing the nanocrystals to lose charge more smoothly and rapidly. As the apparent discharge electric field seen by the nanocrystals in Device B is smaller, the retention time for Device B would hence be better than Device A.

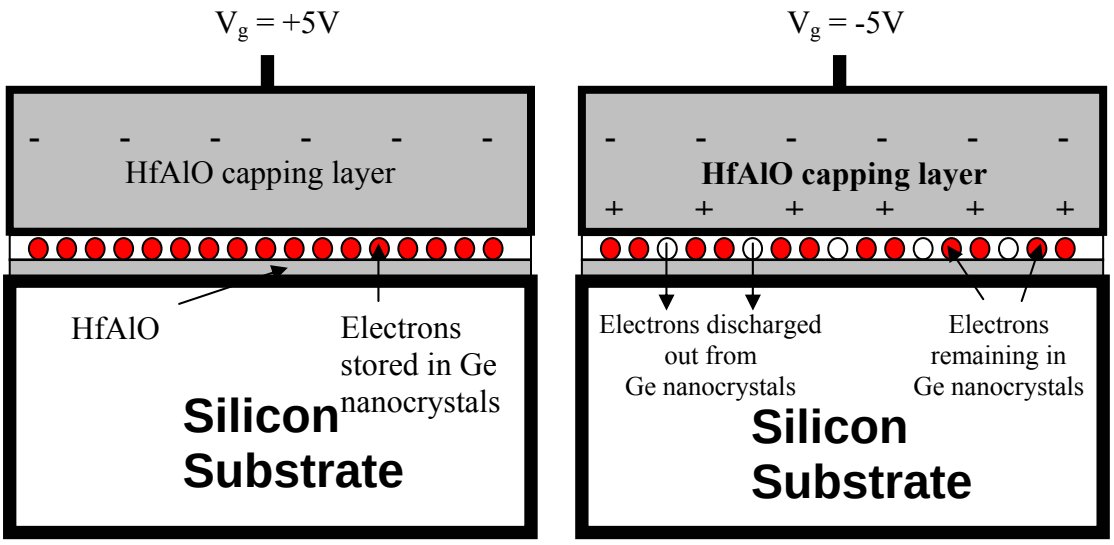


Figure 5.7: Schematic diagram describing the polarization effect in the high-κ capping layer during charging. (a) shows the polarization of the high-κ material when +5V is applied to the gate during charging. (b) shows the positive charge in the dipole of the polarized high-κ material preventing some electrons (stored in the nanocrystals) from tunneling back to the Si substrate easily, when the gate voltage is abruptly switched to -5V during discharging. The nanocrystals that are still stored with electrons are represented by the shaded nanocrystals in (b).

It is also observed that in the more negative gate discharge voltage range from -5V to -3.5V, both devices have almost similar charge retention characteristic. This is because in the slightly more negative voltage regime, the polarization effect from the high-κ capping layer may be too mild to offset the larger discharging voltage in the more negative range. This results in both devices having almost similar retention characteristics over this range.

5.4 Conductance Measurement

Capacitance-voltage (C-V) measurement has conventionally been a preferred method of obtaining device characteristics due to the ease of equipment setup and data analysis. On the other hand, although the conductance-voltage (G-V) measurement requires more elaborate analysis of the experimental data, it is a relatively sensitive method and can provide further insights into the electrical operation of devices [1]-[3]. The G-V method is able to provide information directly related to the energy loss, in response to the applied AC signal, during the capture and emission of carriers by interface traps [4]. Recently, Huang *et al.* have also reported similar energy loss by nanocrystals in response to the AC signal source during the capture and emission of carriers [5]. According to Huang *et al.*, small signal energy loss results when the nanocrystal dots or interface traps cannot respond to the AC signal immediately. This small signal energy loss is directly related to the equivalent parallel conductance, G_p.

5.4.1 Motivation for Applying Conductance Measurement to the Study of Nanocrystal Devices

Currently, few research groups have made use of G-V to study the newer type of device structure. It would be interesting to obtain a better understanding of the electrical characteristics of nanocrystal memory devices using such a technique. In Huang *et al.*'s work, the metal-insulator-semiconductor (MIS) nanocrystal samples used have been carefully fabricated to ensure a negligible concentration of interface traps so that the measured G-V characteristics is predominantly due to the effects of the nanocrystals. In this work, an attempt has been made to show that the effects of interface traps and

nanocrystals on the G-V characteristics could be identified and separated even if the tunnel dielectric were made of a material with poorer interfacial quality, in this case a high dielectric constant (high-κ) material, provided the electric field coupling from the applied gate voltage to the tunnel dielectric layer is high. This would mean that the G-V measurements need not be applicable only to MIS nanocrystal structures with good interfacial quality. In this part of the project, nanocrystal capacitor devices with different capping materials have been used for the study of their G-V characteristics. A calculation has also been made to derive the Ge nanocrystal density from the G-V data and the result is in agreement with that obtained by analyzing the C-V hysteresis width of the Ge nanocrystal memory structures [6].

5.3.2 Theory and Model of Conductance Measurement

Nicollian has explained that the conductance characteristic observed in a conventional MOS capacitor device is due to the energy loss from trap levels that are not able to respond to the AC signal immediately [4]. An illustration of the phenomenon is explained by the energy band diagram in the following way. Figure 5.8(a) shows the energy band diagram at equilibrium when no AC signal is applied to the gate electrode. In the positive half of an AC signal applied at the gate electrode (Fig. 5.8(b)), the Si conduction band move instantaneously towards the Fermi level at the Si surface. Interface traps do not respond immediately but lag behind this sudden change in AC gate voltage, resulting in some empty traps below the Fermi level in the Si. These empty states try to capture electrons from the Si substrate. Energy is lost when electrons at a

higher energy level in the Si conduction band are captured by interface traps at lower average energy.

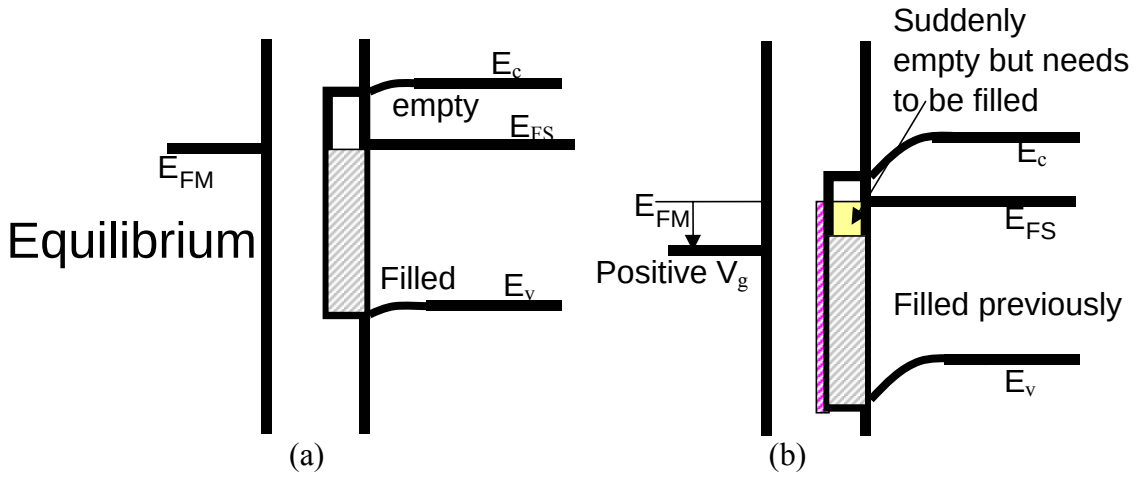
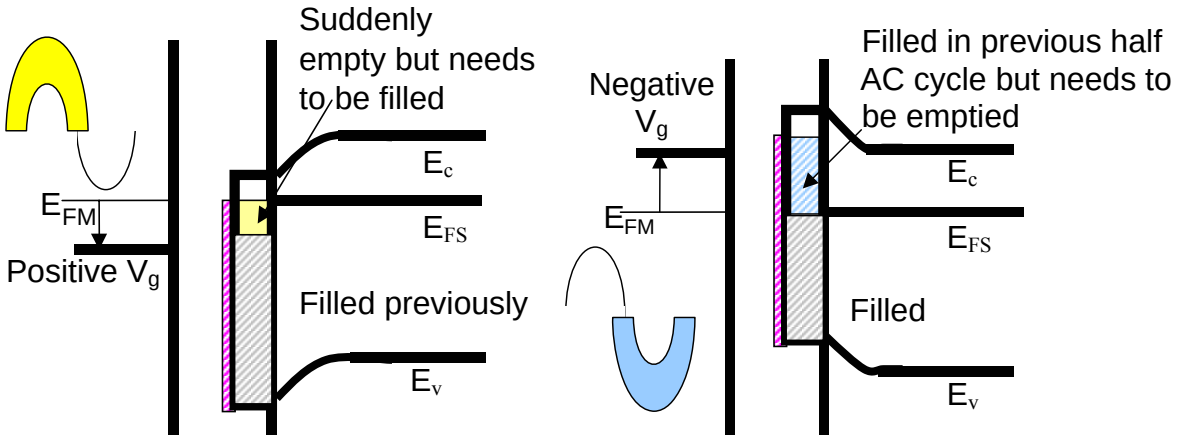


Figure 5.8: Energy band diagram showing the interface traps (a) at equilibrium and (b) in the positive half cycle of the AC signal applied at the gate electrode.

Similarly, when the AC signal suddenly goes from the positive half cycle (shown in Fig. 5.9(a)) to the negative half cycle (shown in Fig. 5.9(b)), the conduction band moves instantaneously away from the Fermi level at the Si surface. The interface traps cannot respond immediately again. Some previously filled interface traps above the Fermi level need to emit their electrons into the Si substrate. As electrons are emitted from interface traps into the Si conduction band, energy is lost again. This energy loss, resulting from interface traps not being able to respond immediately to signal change, can be extracted as an equivalent parallel conductance value, G_p, from G-V measurement.



(a) (b)

Figure 5.9: Energy band diagram showing the interface traps (a) at the positive half cycle of the AC signal and (b) immediately followed by negative half of the AC signal.

The schematic diagram explaining the derivation of the conductance parameters is shown in Fig. 5.10. According to Nicollian and Brews [4], the raw G-V data is first obtained by setting the LCR meter into the parallel Capacitance-Conductance (C-G) mode. From the measured raw data (represented in Fig. 5.10(a)), the device parameters such as interface trap capacitance (C_{it}), silicon surface capacitance (C_s),oxide capacitance (C_{ox}), series resistance (R_s) and equivalent parallel conductance (G_p) can be extracted from the conductance model (represented by Fig. 5.10(b)). G_p is a direct result from AC energy loss and this energy loss is mainly due to interface traps when they fail to respond immediately to the AC gate voltage.

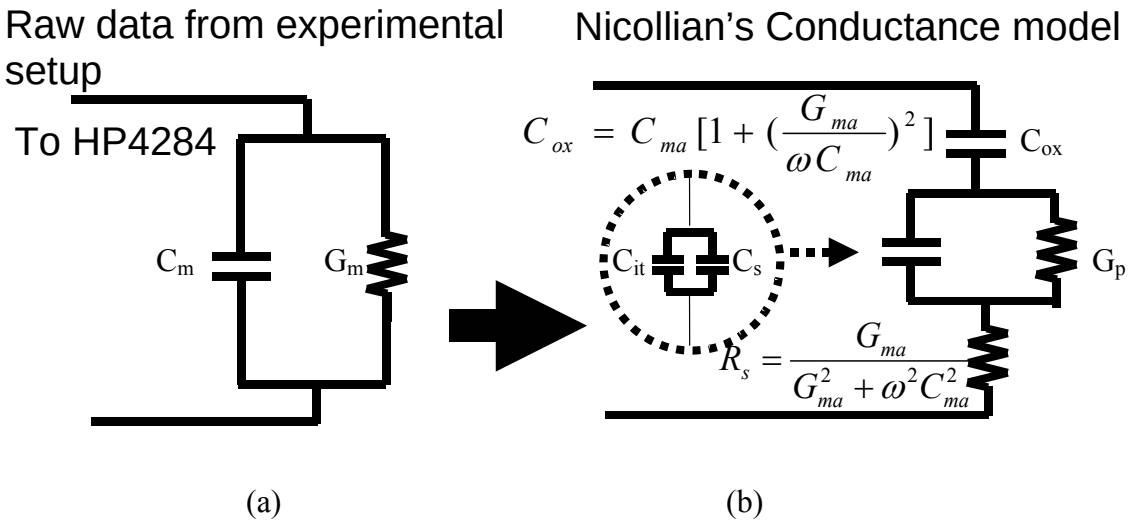


Figure 5.10: Schematic diagram explaining the derivation of the conductance parameters. (a) shows the experimental setup for a typical LCR meter to acquire the capacitance and conductance data and (b) shows the schematic for obtaining the parameters for Nicollian's conductance model.

There are three important sources of AC energy loss in a MOS capacitor: (i) changes in the interface trap level occupancy, (ii) changes in the occupancy of bulk trap levels and (iii) series resistance. If the factor due to series resistance is dominant, the measured equivalent parallel conductance will not go through a peak as a function of gate bias because the loss due to this process is independent of band bending. Both capacitance and conductance measurements can be affected by series resistance, particularly at higher frequencies.

The value of R_s can be found by biasing the MOS capacitor into strong accumulation. In accumulation, the silicon surface capacitance, $C_s = C_a$ where C_a (the accumulation layer capacitance) is large, thus shunting Y_{it} ($=C_{it} + G_p$) (refer to Fig. 5.11(a)). Since $C_a >> C_{ox}$, the circuit in Fig. 5.11(a) is further simplified to Fig. 5.11(b).

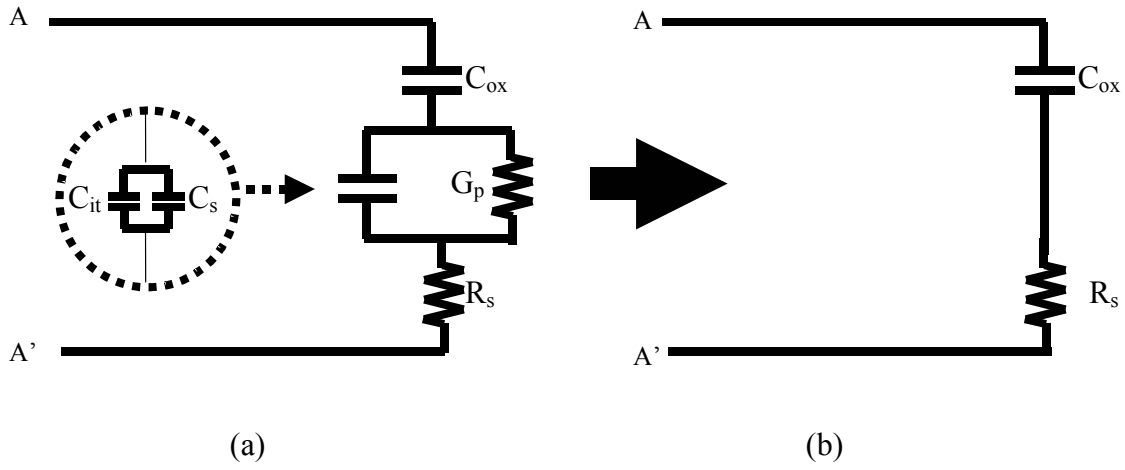


Figure 5.11: Schematic diagrams illustrating the procedure for correction of series resistance. (a) shows the original schematic representation whereas (b) shows the simplified diagram when the MOS capacitor is biased into the strong accumulation region.

The admittance measured across A-A' in strong accumulation is

$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{5.1}$$

where G_{ma} and C_{ma} are the measured conductance and capacitance, respectively, in strong accumulation. R_s is found from the real part of $Z_{ma} = 1/Y_{ma}$ or

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{5.2}$$

C_{ox} can be calculated using the formula as

$$C_{ox} = C_{ma}[1 + (\frac{G_{ma}}{\omega C_{ma}})^2] \tag{5.3}$$

The corrected capacitance, C_c, and conductance, G_c, at any frequency are

$$C_c = \frac{(G_{pm}^2 + \omega^2 C_{pm}^2)C_{pm}}{a^2 + \omega^2 C_{pm}^2} \tag{5.4}$$

and

$$G_c = \frac{(G_{pm}^2 + \omega^2 C_{pm}^2)a}{a^2 + \omega^2 C_{pm}^2} \tag{5.5}$$

respectively, where a = G_{pm}-(G^2_{pm} + $\omega^2C^2_{pm}$)R_s and C_{pm} and G_{pm} are the respective measured capacitance and conductance in the parallel mode across the terminals of the MOS capacitor (shown earlier in Fig. 5.10a).

After series resistance correction, the conductance peak can be obtained. C_{ox} can be found from Eq. (5.3) or from the C_c value in accumulation [Eq. (5.4)]. This value is used to correct for the oxide capacitance included in the measured admittance, $Y_m = C_{pm} + G_{pm}$ (Fig. 5.10a across A-A') to obtain the interface trap admittance, $Y_{it} = C_{it} + G_p$. This is done by converting Y_m into impedance, subtracting $1/j\omega C_{ox}$ and then converting it back into admittance. The real part of the admittance, Y_{it}, is

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_{pm}}{G_{pm}^2 + \omega^2 (C_{ox} - C_{pm})^2} \tag{5.6}$$

Recently, Huang *et al.* have fabricated some Si nanocrystal memory capacitors and conducted some G-V studies [5]. According to Huang *et al.*, for a capacitor memory device with Si-nanocrystals (nc-Si) embedded in a SiO_2 matrix, the conductance characteristics can also be related to the energy loss provided by the AC signal source during the capture and emission of carriers by nc-Si dots. They have conducted a G-V measurement and found a prominent conductance peak (related to maximum energy loss due to nanocrystal) at the flatband-midgap region as shown in Fig. 5.12. The following is their explanation of the conductance peak observed in a nanocrystal memory capacitor device. In the accumulation state, the majority carrier density is very large near the Si-tunnel dielectric interface. The Ge nanocrystal dot capture rates are very rapid compared to the AC voltage and hence no energy loss occurs. Therefore, low conductance value and no peak is observed in the accumulation region. In the depletion state, the majority carrier density at the Si-tunnel dielectric interface is reduced. Capture rates slow down and Si nanocrystal dot levels cannot keep pace with the AC voltage. Therefore, energy loss starts to occur and the conductance value starts to rise. Further in the depletion state (near midgap), the majority carrier density becomes so low that Si nanocrystal dot levels hardly respond. The capture rate is so slow that almost no carriers are exchanged between nanocrystal-dot and the Si substrate. Hence, maximum loss occurs and this gives rise to a conductance peak.

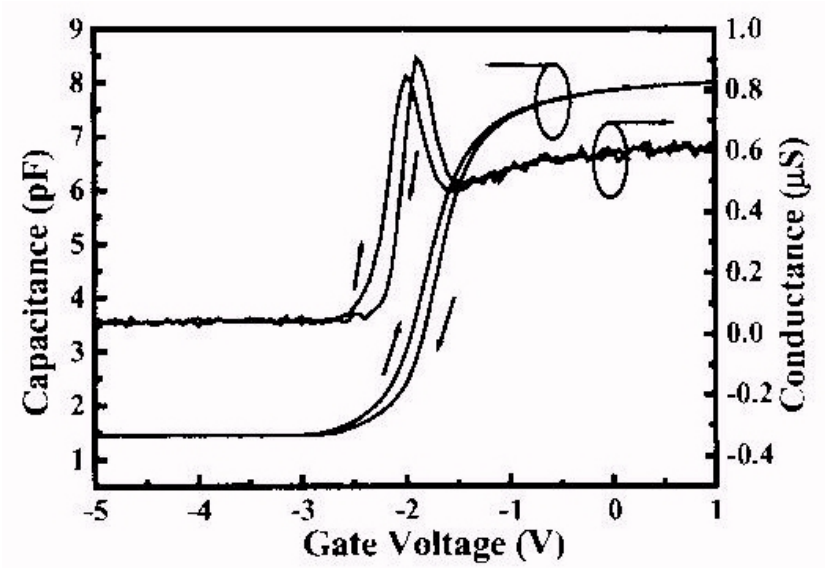


Figure 5.12: Typical C-V and G-V characteristics obtained by sweeping gate voltage back and forth between -5V and 1V. The peak position in the G-V characteristics is around the flatband condition [5].

5.3.3 Correlation between Conductance Peak Location and Flatband Voltage

An experiment was first conducted to investigate the gate voltage location of the conductance peak in the G-V plot of the trilayer structure nanocrystal memory devices. Only results for device B (structures of device A and B have previously been described in Table 5.1) will be shown in Fig. 5.13 but the general conclusion also applies to device A. Device B was first held at a gate voltage of -1 V for 240 s to allow saturation of positive charge storage, followed by a gate voltage sweep from –1 V to 1 V. At the end of this forward sweep, the device was held at a gate voltage of 1 V for 240 s to allow saturation of negative charge storage and then followed by a reverse gate voltage sweep from 1 V to -1 V. The gate voltage sweep range was then increased from -1 V < V_g < 1 V to -10 V < V_g < 10 V in steps of 2 V. During the forward and reverse gate voltage sweeps, both C-V and G-V curves were measured. From the C-V plot in Fig. 5.13(a), the flatband voltage

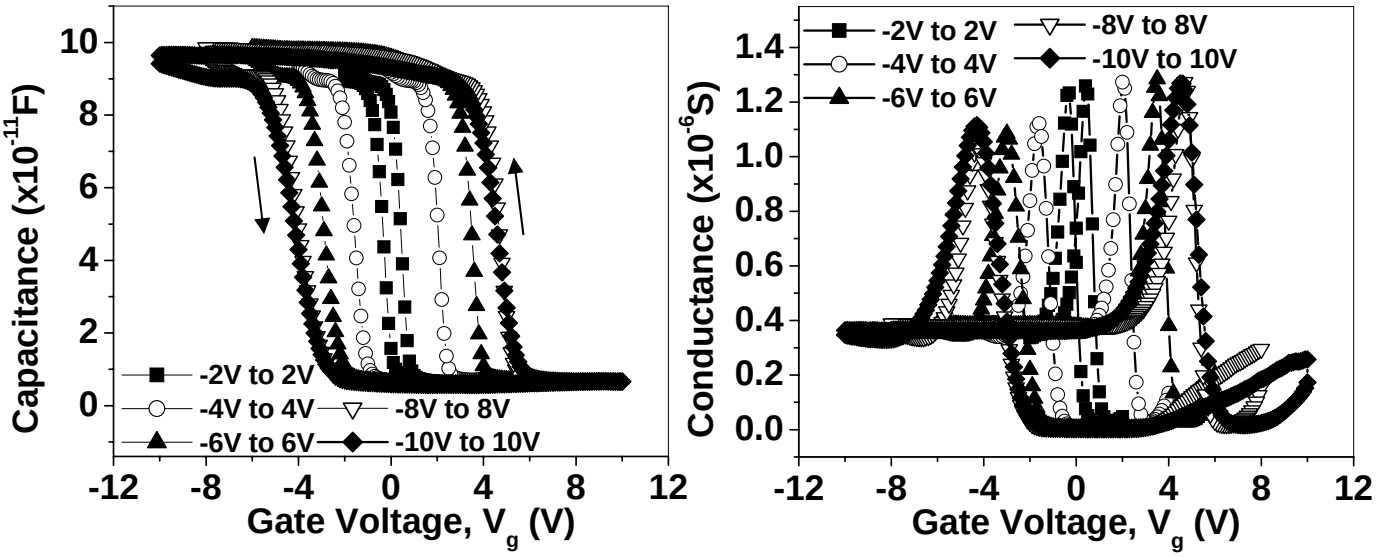
V_{FB} is determined for each C-V curve from the flatband capacitance (C_{FB}) value of 3.267 x 10^{-11} F and compared with the gate voltage location (i.e., V_{PEAK}) where the peak conductance value occurs in the G-V plot in Fig. 5.13(b). The flatband capacitance is obtained from

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_s}} \tag{5.7}$$

where C_{ox} is the oxide capacitance, ε_s is the permittivity of silicon, and L_D is the Debye length, given by

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_{sub}}} \tag{5.8}$$

and N_{sub} is the substrate doping concentration.



(a) (b)

Figure 5.13: High frequency C-V and G-V characteristics of the trilayer structure nanocrystal memory device B. (a) Forward and reverse sweeps C-V curves showing counter-clockwise hysteresis with the gate voltage (V_g) sweep increasing from –2 V < V_g < 2 V to -10 V < V_g < 10 V. (b) The corresponding G-V characteristics during the respective gate voltage sweep.

A plot correlating the V_{FB} and V_{PEAK} (of Fig. 5.13) is shown in Fig. 5.14. It is seen that V_{FB} tracks V_{PEAK} closely, that is the conductance peak occurs close to flatband and in the depletion bias regime. This is because at depletion, the majority carrier density at the silicon-tunnel dielectric interface is reduced. As a result, carrier capture rates slow down and the Ge nanocrystals cannot keep pace with the AC gate voltage, resulting in energy loss. Hence, energy loss is highest, and the conductance between the gate and silicon (Si) substrate peaks, at a gate bias close to V_{FB}.

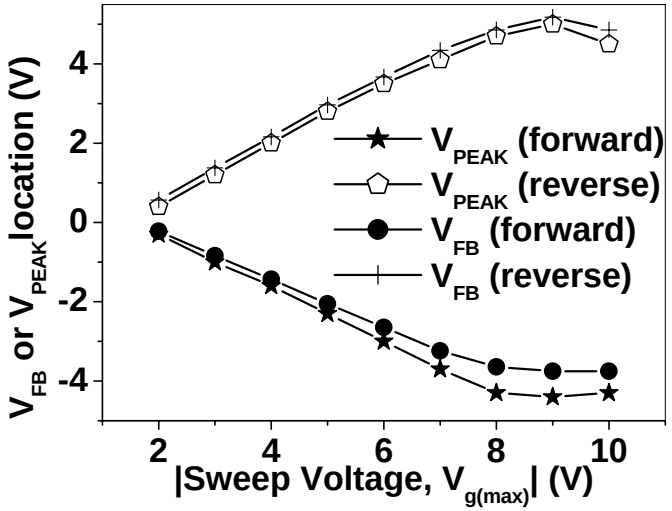


Figure 5.14: Plot of the gate voltage corresponding to the conductance peak (V_{PEAK}) and flatband voltage V_{FB} (from C-V plot) versus the gate voltage sweep range.

By postulating from the theory of Nicollian and Brews [4] and Huang *et al.*'s findings [5], the energy loss in our nanocrystal capacitor memory structure could be attributed to both the interface trap and/or nanocrystals not being able to respond to the AC signal immediately. The conductance model of Nicollian and Brews (previously discussed and shown in Fig. 5.10) could hence be used to take into consideration the effects from both sources of energy losses. The original conductance model could be

broken down into two branches with one branch contributed by energy loss due to interface traps and the other branch, by energy loss due to Ge nanocrystals. A schematic diagram showing the division of the original G_p branch into two sub-branches is shown in Fig.5.15. Based on the model in Fig.5.15 (b), the effects from nanocrystals or interface traps on the conductance characteristics were then studied.

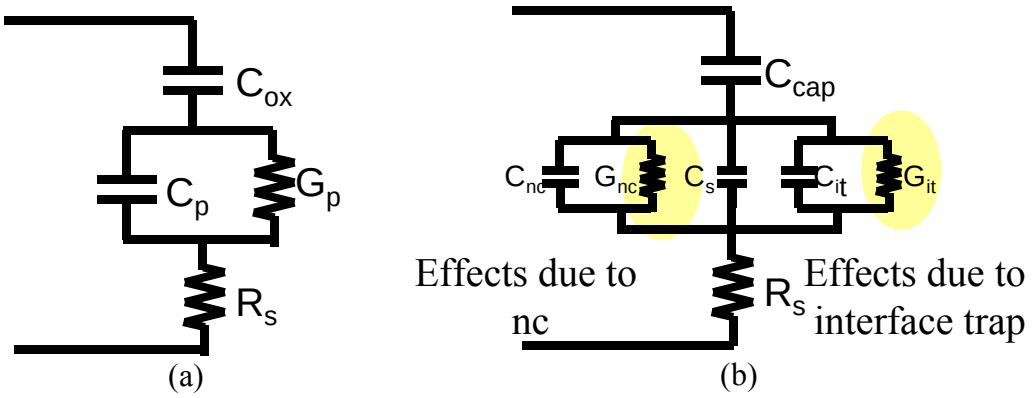


Figure 5.15: Schematic diagram showing the components for the extracted parallel conductance. (a) shows the extracted parallel conductance, G_p, which is contributed by (b) the nanocrystal conductance G_{nc} branch, and the interface trap G_{it} branch.

5.3.4 Conductance Measurement on Nanocrystal Capacitor Devices with Different Types of Capping Layer

Three types of devices (Devices CONTROL, A and B) were used for the study of G-V characteristics. The three devices were simple trilayer capacitors consisting of 4nm HfAlO (with 1nm of surface nitridation) as the tunnel dielectric, followed by a 4nm Ge layer and a capping layer of 20nm thickness. Device CONTROL is intentionally fabricated with no Ge nanocrystals in the middle layer followed by 20nm of SiO_2 capping layer. The G-V characteristics of Device CONTROL would hence be solely due to

interface traps. Device A is a memory capacitor device with Ge nanocrystals present in the middle layer and 20nm of SiO_2 cap layer. The 20nm of SiO_2 cap layer provides moderate electrical coupling from the gate electrode to the nanocrystals. The G-V characteristics obtained from Device A would hence be contributed by a combination of both the interface traps and the nanocrystals. Device B is similar to Device A except that the capping layer used is 20nm of HfAlO. The 20nm HfAlO layer provides the highest amount of electric field coupling (42.8% better than Device A) from the gate electrode to the nanocrystals and the effects on the G-V characteristics would be contributed mainly by the nanocrystals. A description of the three devices used for G-V study is given in Table 5.3

Table 5.3: Description of the devices used for G-V study.

Device	**Layer 1**	**Layer 2**	**Layer 3**	**Remarks**
CONTROL	2nm (EOT) HfAlO	None	20nm SiO_2	Control device without nanocrystals
A	2nm (EOT) HfAlO	4nm Ge	20nm SiO_2	Moderate electric field coupling
B	2nm (EOT) HfAlO	4nm Ge	20nm HfAlO	Best electric field coupling

Frequency dependent G-V measurements, with frequency (*f*) ranging from 50 kHz to 1 MHz, were then carried out on devices CONTROL, A and B. The devices were first held at a gate voltage of -5 V for 240 s to allow saturation of positive charge storage, followed by a gate voltage sweep from –5 V to 5 V. At the end of this forward sweep, the devices were held at a gate voltage of 5 V for 240 s to allow saturation of negative charge storage and then followed by a reverse gate voltage sweep from 5 V to -5 V. During the gate voltage sweep, both the capacitance and conductance values were monitored. The

parallel conductance value (G_p), normalized with angular frequency ($\omega = 2\pi f$) and gate area (A), was extracted based on the model by Nicollian and Brews, and plotted against gate voltage in Fig. 5.16 for the three devices.

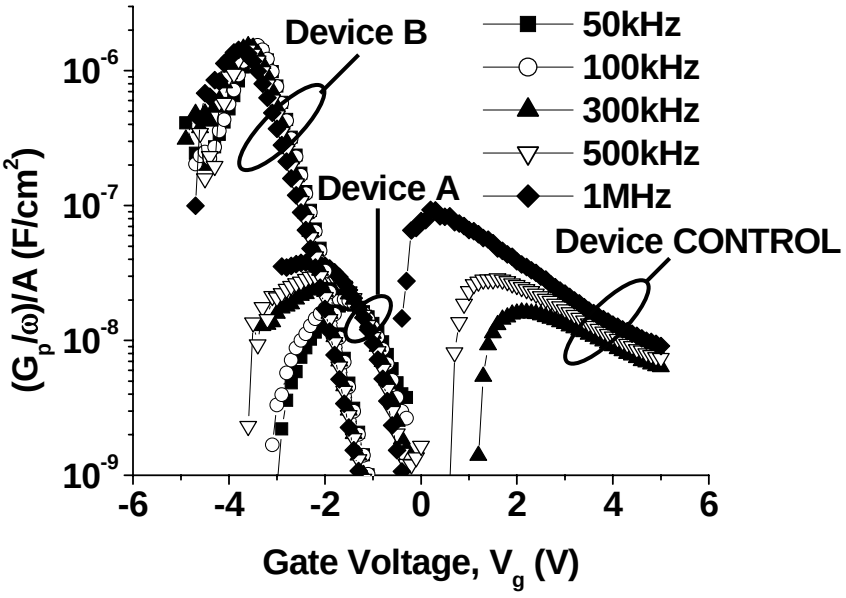


Figure 5.16: Parallel conductance characteristics, $(G_p/\omega)/A$ on a log scale plotted against gate voltage during forward (increasing) gate voltage sweep after biasing at a gate voltage of -5 V for 240 s, for the three devices: Device Control (without nanocrystals), Nanocrystal memory device A (with 20-nm thick SiO_2 cap layer) and Nanocrystal memory device B (with 20-nm thick HfAlO cap layer). Note that the 50 kHz and 100 kHz $(G_p/\omega)/A$ data for device A are smaller than 10^{-9} F cm^2 and are not shown on the plot.

It is seen the conductance peak of the control device (without nanocrystals) has the largest variation with frequency and this is a typical response from the interface traps [4]-[7]. The conductance peak (where energy loss is at a maximum) increases with frequency because at higher frequencies, more interface traps could not respond to the AC signal change and this results in greater energy loss (i.e., increase in the $G_p/(\omega A)$ peak magnitude with frequency). Device A (20-nm thick SiO_2 cap layer) has a much smaller

C-V hysteresis than device B and shows a moderate variation of conductance peak with frequency. This is due to the moderate capacitative coupling provided by the low permittivity SiO_2 cap layer from the applied gate electric field. The moderate frequency dependence of the $G_p/(\omega A)$ peak is indicative of the combined effects from both interface traps and nanocrystals. Device B (20-nm thick HfAlO cap layer) has the largest C-V hysteresis of the three devices and a large $G_p/(\omega A)$ peak magnitude that is frequency independent. This is explained by the larger gate capacitive coupling factor (42.8 % higher than device A) resulting from the higher dielectric constant (high-κ) HfAlO cap layer. Since a higher electric field is channeled to the nanocrystals from the applied gate bias, this results in more nanocrystals being active in the conduction process. Device B shows the highest conductance peak (highest energy loss) magnitude among the three devices. This high energy loss may be due to the high density of nanocrystals not being able to respond to the AC signal immediately. The carriers that are captured and emitted by the nanocrystals have to tunnel through the tunnel dielectric to reach the traps in nanocrystals, or tunnel across the tunnel dielectric layer to land in the conduction band of Ge and then fall into traps in the nanocrystals subsequently [8]-[11]. The response time of the nanocrystal devices is thus much slower compared to the control device where capture and emission of carriers occur only through the interface traps. This is because interface traps are nearer to the Si substrate and hence take a shorter time to reach equilibrium with the substrate as compared to the nanocrystals. The slower response time of the nanocrystal devices suggests a greater energy loss and this results in a higher G_p or $G_p/(\omega A)$ value. This slow response time of the nanocrystals also results in the conductance peak having negligible variation with frequency in device B as the

nanocrystals could not respond immediately to the AC signal for frequencies greater than 50 kHz.

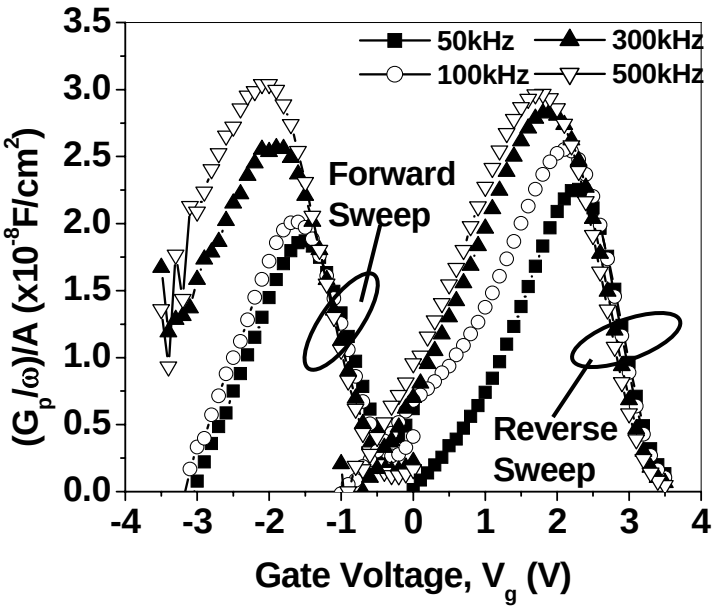


Figure 5.17: Frequency dependent parallel conductance characteristics, $(G_p/\omega)/A$ plotted on a linear scale against gate voltage, of nanocrystal memory device A (with 20-nm thick SiO_2 cap layer): (a) During forward (increasing) gate voltage sweep after biasing at a gate voltage of -5 V for 240 s, and (b) During reverse (decreasing) gate voltage sweep after biasing at a gate voltage of 5 V for 240 s.

Figure 5.17 shows the forward and reverse sweep G-V characteristics of the nanocrystal memory device A, for which the electric field coupling is moderate and both interface traps and nanocrystals affect the G-V characteristics. It is seen that for frequencies greater than 100 kHz, there is less frequency dispersion in the conductance plot for the reverse sweep characteristics as compared to the forward sweep characteristics. The $G_p/(\omega A)$ peak magnitude is also slightly larger at frequencies of 500 kHz and below for the reverse sweep as compared to that for the forward sweep. This could possibly be explained by the slightly larger electric field across the gate structure

during the reverse sweep. During the forward sweep, when the device is held and swept from a negative gate bias, positive charges are stored in the nanocrystals, while during the reverse sweep, electrons or negative charges are stored in the nanocrystals. This would mean that under the assumption of equal number of positive and negative stored charges and for similar surface depletion condition (at the bias corresponding to the conductance peak) for the p-type silicon in the two situations, the magnitude of the gate charge (and resultant electric field) would be larger for the device under reverse sweep than that under forward sweep.

5.3.5 Estimation of Nanocrystal Density Based on Conductance-Voltage (G-V) Data

An attempt has also been made to calculate the nanocrystal density using the extracted parallel conductance data. For nanocrystal capacitor memory devices A and B, the conductance characteristics is contributed by two main branches, namely, the nanocrystal branch and the interface trap branch. However, when the effect from the nanocrystals is more dominant, as in the case where a high-κ capping oxide is used (device B), the nanocrystal branch becomes more dominant over the interface trap branch and the conductance model on the left of Fig. 5.18 could then be simplified to that shown on the right of Fig. 5.18.

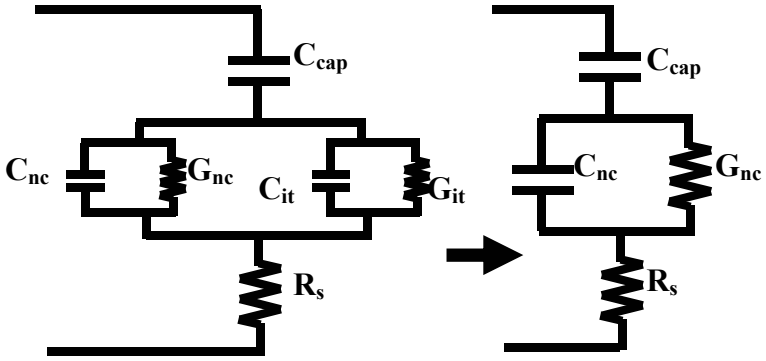


Figure 5.18: Schematic diagram of the conductance model for a typical nanocrystal memory device structure. When the effect of nanocrystals is more dominant than that of interface traps, the model on the left could be further simplified to that on the right.

For device CONTROL without any nanocrystals, the interface density (D_{it}) is given by [4].

$$D_{it} = qC_{it} = \frac{(\frac{G_p}{\omega})_{peak}}{qAf_D} \tag{5.8}$$

where C_{it} is the interface trap capacitance, $(\frac{G_p}{\omega})_{peak}$ is the extracted conductance peak, q is the electronic charge, f_D is the universal function of variance of band bending and A is the area of the device. Similarly, in the nanocrystal memory device B where the electric field coupling is very high and the interface trap effect on the conductance characteristics is negligible, the density (N_{NC}) of nanocrystals can be calculated from the circuit model on the right side of Fig. 5.18. A schematic diagram explaining the approach for the calculation of nanocrystal density is given in Fig 5.19.

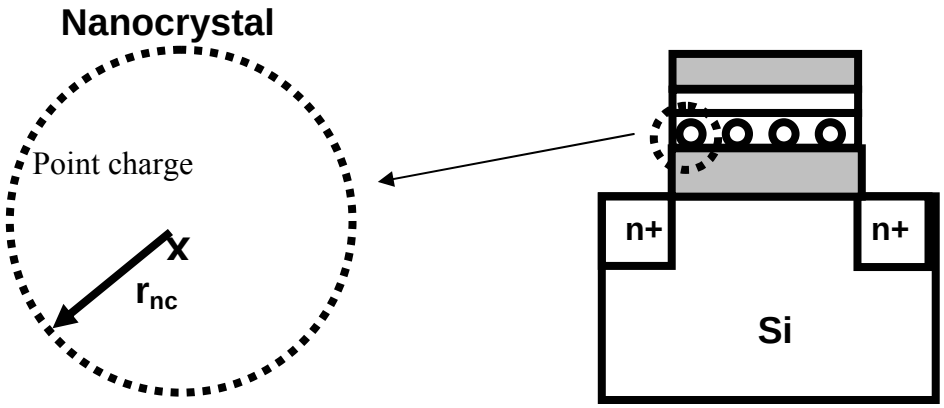


Figure 5.19: Schematic diagram illustrating the approach for the calculation of nanocrystal density.

The charge stored in a nanocrystal is assumed to be a point charge as shown in Fig. 5.19. The electric field at the surface of the nanocrystal can be given as

$$E = \frac{q}{4\pi\varepsilon_o\varepsilon_{Ge}r_{nc}^2} \tag{5.9}$$

where q is the electronic charge, ε_0 is the permitivity of free space, ε_{Ge} is the permitivity of germanium and r_{nc} is the radius of each nanocrystal.

The corresponding potential (V) of each nanocrystal can be obtained by integrating Eq. (5.9) with respect to the radial distance, giving

$$V = \frac{q}{4\pi\varepsilon_o\varepsilon_{Ge}r_{nc}} \tag{5.10}$$

The charge stored in one nanocrystal (q_{nc}) can be expressed as the product of the capacitance of each nanocrystal (C_{nc}) with its potential (V).

$$q_{nc} = C_{nc} \times V \tag{5.11}$$

The total amount of charge of charge, Q, stored in all the nanocrystals can be expressed as

$$\begin{aligned} Q &= N_{NC} \times q_{nc} \\ &= N_{NC} \times C_{nc} \times V \\ &= C_{NC} \times V \end{aligned} \tag{5.12}$$

where N_{NC} is the total number of nanocrystals per unit area, C_{nc} is the capacitance of each individual nanocrystal and C_{NC} is the total capacitance of all the nanocrystals, i.e. $C_{NC} = N_{NC} \times C_{nc}$.

In ref. [6], it was found that one nanocrystal stores one charge, either an electron or a hole. Hence it is assumed that $q_{nc} = q$.

The total number of nanocrystals per unit area can then be derived using Eqs. (5.12) and (5.10) with $q_{nc} = q$ as

$$\begin{aligned} N_{NC} &= C_{NC} \times \frac{q}{q 4\pi\varepsilon_o \varepsilon_{Ge} r_{nc}} \\ &= \frac{C_{NC}}{4\pi\varepsilon_o \varepsilon_{Ge} r_{nc}} \end{aligned} \tag{5.13}$$

C_{NC}, is related to the parallel conductance (G_p) by

$$C_{NC} = \frac{(\frac{G_p}{\omega})_{peak}}{Af_D} \tag{5.14}$$

Using Eqs. (5.13) and (5.14), the density of Ge nanocrystals is estimated to be 4.96 x 10^{12} cm^{-2}, which is in good agreement with the value of 5.0 x 10^{12} cm^{-2} obtained by analyzing the C-V hysteresis width of the Ge nanocrystal memory structures by assuming that one nanocrystal stores one charge (electron or hole) [6].

5.5 Summary

In this chapter, the possibility of achieving enhancement in device performance by means of an increased gate electric field coupling factor has been investigated. The electric field coupling factor could be improved by either reducing the thickness of the SiO_2 capping layer or replacing the capping layer with a high-κ material. The thickness of the SiO_2 cap layer was first reduced from the original 50nm to 20nm. Results show that SiO_2 cap layer with a reduced thickness of 20nm was able to result in better charge storage capability. At the same time, this reduced cap layer thickness was sufficient to prevent Ge outdiffusion into the ambient during high temperature annealing to form the Ge nanocrystals. The gate coupling factor was also increased by replacing the capping layer with a high-κ material. Significant enhancement in device performance in terms of charge storage as well as charge retention capabilities could be attained.

The effect of different cap layers, affecting the electric field coupling from the applied gate bias, on the conductance characteristics of nanocrystal memory devices was also studied. It was found that the frequency dispersion of the conductance peak is most significant when the effect from interface traps is dominant, as in a device structure

without nanocrystals. In structures where the effect from nanocrystals is dominant, the conductance characteristics show negligible frequency dispersion. It was also shown that G-V measurements could also provide a good estimate of the nanocrystal density in structures where the electric field coupling is high.

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Chapter 6: Investigation of Charge Storage Mechanism in Germanium Nanocrystals Using Nanocrystal Transistor Devices

In the earlier chapters, trilayer nanocrystal capacitor devices have been fabricated to study the effects of the high-κ tunnel dielectric and capping oxide layers on device performance. However, more precise parameters such as the threshold voltage, programming speed, retention and endurance characteristics can only be obtained from a complete transistor device. Based on the experience from the fabrication of capacitor devices, a set of transistor devices has been fabricated and their characteristics studied.

Besides characterizing the performance of our devices, the charge storage mechanisms will also be investigated. An overview of previous work conducted by other research groups on the extraction of trap energy level will first be introduced, followed by the extraction of the Ge trap energy levels from our nanocrystal memory transistor device. An alternative method to extract the trap energy level, based on the study of the change in drain current compared to its initial state during the discharging process, will be discussed. This alternative method has a physical basis and the advantage of not requiring a fit of experimental data to an assumed analytical discharge expression. The origin of the traps responsible for the charge storage of our devices will be discussed and the possibility of engineering the trap level, for better charge retention capability, by changing the host matrix surrounding the Ge nanocrystals will also be investigated.

6.1 Fabrication Procedure of Nanocrystal Memory Transistor

The fabrication procedure of the nanocrystal memory transistor is described by the schematic diagram in Fig. 6.1. The substrate used was 4-8 Ω-cm (100) p-type silicon. A high-κ tunnel dielectric stack consisting of 1nm SiO_xN_y and 4nm of HfAlO was first deposited on the Si substrate by MOCVD. The surface nitridation was performed at 700^{o}C for 1 minute in an NH_3 ambient. The HfAlO film was then deposited at 450^{o}C using $HfAl(MMP)_2(OiPr)_5$ as the deposition source. Since the precursor, which is a liquid at room temperature, has extremely low vapor pressure of about 6.4 x 10^{-5} Torr, a liquid delivery system (LDS) was adopted for the delivery of the precursor into the chamber. This precursor was first introduced into a vaporizer chamber by a push gas (argon) and its flow rate was controlled by liquid mass flow controller (LMFC). Another gas line of argon, called argon carrier gas, was used to vaporize the liquid precursor in the vaporizer chamber and to carry the vaporized precursor into the process chamber. After the deposition of the high-κ dielectric, post-deposition annealing (PDA) was performed at 700^{o}C for 1 minute in a N_2 ambient. The tunnel dielectric gate stack has an equivalent oxide thickness of 2nm. A thin layer (4nm) of Ge was sputter-deposited (at a power of 100W and an operating pressure of 0.3kPa) on top of the 2nm (EOT) thick HfAlO tunnel dielectric film, followed by sputter-deposition of a 20nm thick SiO_2 cap layer. The trilayer gate stack was then subjected to rapid thermal annealing at 1000^{o}C for a duration of 300s to synthesize the Ge nanocrystals in the middle charge storage layer. TaN (~150 nm) gate electrode was fabricated by dc sputtering of Ta target in Ar + N_2 ambient. The gate was patterned by photolithography followed by dry etching. N^+ source/ drain

implant was carried out at 100keV, 7^{o} tilt and an As^{+} ion dose of $10^{15}cm^{-2}$, followed by source/ drain activation anneal at 950^{o}C for 30s.

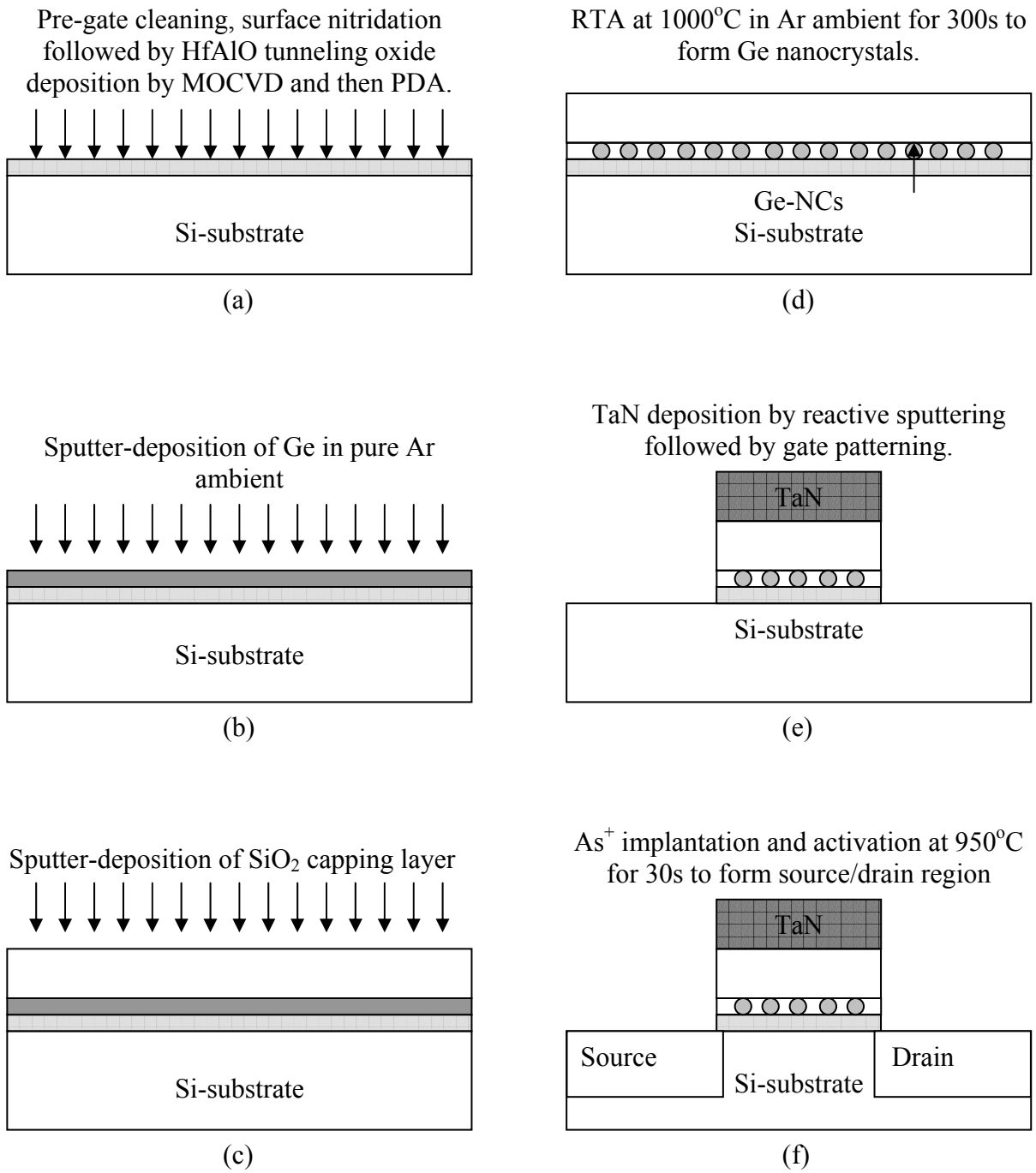

Figure 6.1: Schematic diagram of the process flow for Ge nanocrystal memory transistor device fabrication.

The HRTEM image of the completed HfAlO/nc-Ge/SiO_2 transistor memory structure is shown in Fig. 6.2. The transistors used in our experiments have gate width/ gate length dimensions of W/L = 100/10 μm.

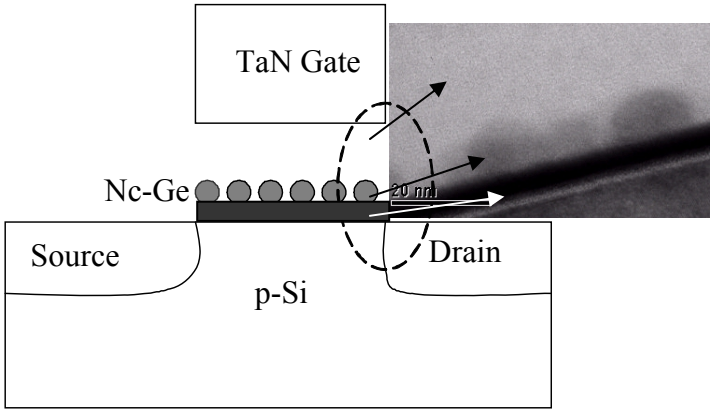

Figure 6.2: Schematic cross-sectional structure of fabricated device and HRTEM image of the HfAlO/nc-Ge/SiO_2 transistor memory structure.

6.2 Electrical Characterization of Nanocrystal Memory Transistor

Following the fabrication of the memory transistors, electrical characterizations were performed on these devices. Figure 6.3 (a) and (b) show the I_d-V_d and I_d-V_g characteristics, respectively. The transconductance (g_m) curve is obtained by differentiating the drain current (I_d) with respect to the gate voltage (V_g). A tangent on the I_d curve is drawn at a gate voltage location for which the maximum transconductance (g_m) value occurs. The threshold voltage (V_{th}) is approximately given by the intersection of the tangent with the gate voltage axis [1]. From Fig. 6.3(b), the threshold voltage is approximately 2.7V and the corresponding drain current at the threshold condition is about 5μA. The threshold voltage shift in our subsequent experiments was monitored based on observing the change in the gate voltage at this constant drain current level of 5μA.

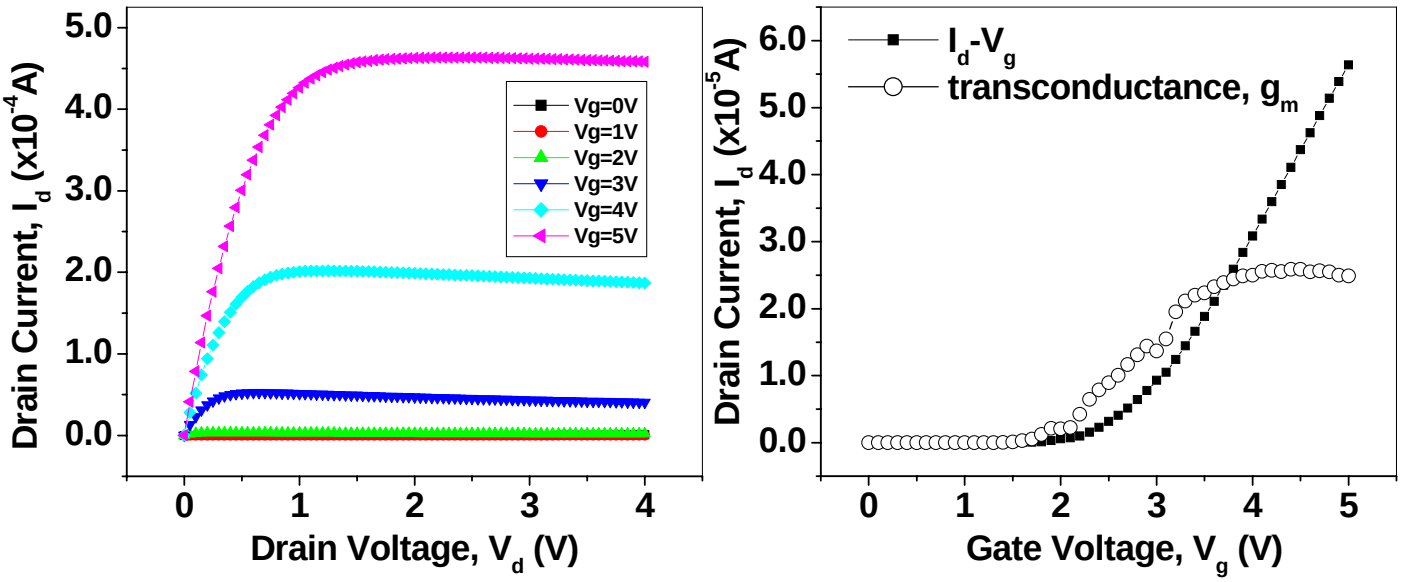

Figure 6.3: Electrical characteristics of the transistor memory device: (a) I_d-V_d and (b) I_d-V_g characteristics. The threshold voltage is about 2.7V.

Following the basic electrical measurements, an experiment is carried out to verify the charge storage capability of the nanocrystal transistor memory device. The drain current of the device is measured while the gate voltage sweep is swept in the forward direction from 0V to 5V, followed immediately by a reverse sweep of 5V to 0V. This experiment is repeated up to a gate voltage sweep range of $0V<V_g<15V$. The I_d-V_g characteristics are shown in Fig. 6.4. The presence of a hysteresis loop is indicative of charge storage in the transistor memory device. During the forward sweep, as the gate voltage increases to a more positive value, electrons are attracted from the Si-substrate into the nanocrystals resulting in a higher threshold voltage. Subsequently, during the reverse sweep, this higher threshold voltage value causes the I_d-V_g curve to shift towards more positive gate voltage. The width of the hysteresis loop increases with the gate voltage sweep range as more electrons would be attracted into the nanocrystals during the forward sweep process, resulting in greater threshold voltage shift.

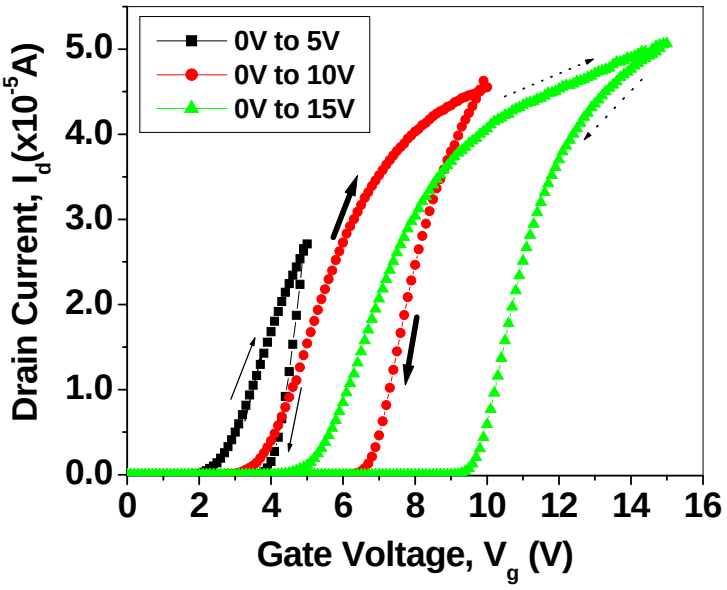

Figure 6.4: I_d-V_g characteristics of the nanocrystal transistor memory device obtained by first sweeping the gate voltage positively in the forward direction followed by a reverse sweep direction. The hysteresis loop formed by each pair of forward/reverse curves is indicative of the charge storage capability of the device.

Following these preliminary measurements, further experiments such as transient programming/erasing characterization, write/erase endurance and charge retention studies were then carried out on these transistor devices and the results will be discussed in the following sections.

6.2.1 Transient Characteristics of the Transistor Based Nanocrystal Memory Structures

The basic function of the non-volatile Flash memory is based on the storing and removing of charges on the floating gate or the floating nodes formed by the nanocrystals. This charging and discharging will affect the threshold voltage (V_{th}) of the memory structure. It is desirable that the charging and discharging are performed at low voltage for a write and erase duration that is as short as possible. However, there is a compromise between the speed and the applied voltage during programming (write) and discharge (erase). The transient programming and erasing characteristics of the memory results in shifting of the threshold voltage as a function of time during the programming or discharging phase. The knowledge gathered from the transient measurement can be used to determine the required programming and erasing voltages, and the time needed to achieve a reasonable threshold voltage window (i.e., difference between programmed and erased state threshold voltage) during the write/erase cycle.

The transient programming measurements can be performed in two ways [2]. In the first approach, programming is done by applying a pulse of fixed amplitude and then measuring the eventual threshold voltage. The device is then erased to its initial threshold voltage and another longer programming pulse is applied at the same amplitude. This process would then be repeated with longer duration programming pulses each time. The main drawback of this technique is that there is an assumption that either the charging or erasing would not introduce defects in the oxide. Another practical difficulty is to accurately bring the system back to its initial condition before charging is performed again.

In the second method, the transient programming characteristics considers the effect of superposition by relating the total programming time as the summation of the durations of the total number of short pulses that are applied. During measurement, voltage pulses of short duration are applied and the threshold voltage is measured after every pulse. The advantage of this method is that it eliminates the need to bring the memory structure back to its initial discharged state. In our characterization, the second method was chosen to investigate the transient programming characteristics of our n-MOSFET devices. The HP8114A pulse generator is used to apply pulses, of selected amplitude and duration. In these experiments, the pulse width is set at 100μs and the pulse period at 500μs. In addition, two pulse amplitudes (8V and 10V) are used for each run. A HP E5250A switch matrix is used to toggle between application of programming or erasing pulses and the measurement of the I_d-V_g curve to extract the threshold voltage, V_{th}, after each run. The V_{th} of the fresh n-MOSFET device is first extracted and subsequently, the V_{th} of the programmed or erased device after 1, 5, 13, 19, 59, 139, 199, 799, 1399, 1999, 3999, 7999, 9999, 11999, 13999, 19997 pulses are obtained using a constant threshold current method.

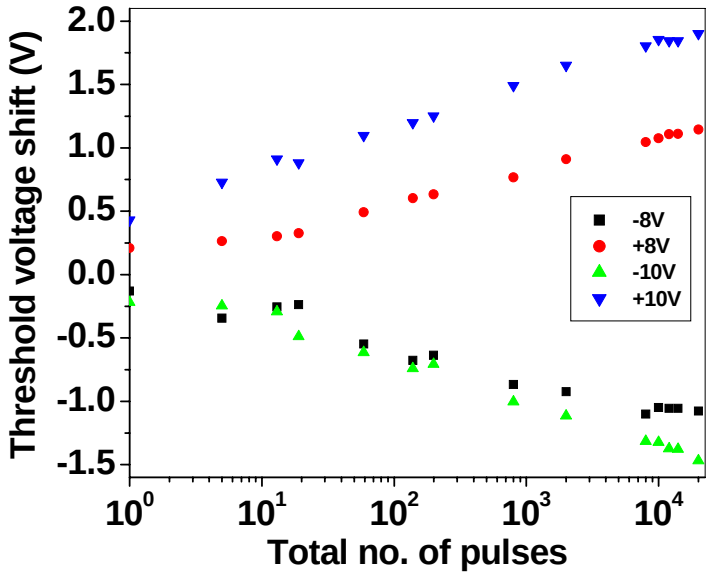

Figure 6.5: A plot of the threshold voltage shift with respect to the total number of pulses. It takes about 59 pulses of 10V to result in a threshold voltage shift of 1V.

From Fig. 6.5, it could be seen that a total of 59 pulses of 10V are required to achieve a significant V_{th} shift of approximately 1V. Assuming that the superposition principle holds, this would correspond to applying a single 10V pulse with pulse width of 5.9ms (i.e., 100µs × 59 pulses). As a form of verification, a V_{th} shift close to 1V was obtained when a single 10V pulse of 5.9ms duration was applied to the gate electrode after the experiment.

6.2.2 Endurance Characteristics

The reliability testing for the nanocrystal memory devices is sub-divided into two parts. Firstly, the endurance characteristics of the devices are investigated. The memory cell is subjected to numerous write/erase (W/E) cycles to observe if there is any significant closure in the threshold voltage window, due to trapped charges that change the injection field and the amount of charges transferred to and from the charge storage

layer during programming. Following that, the retention characteristics of the devices are also measured to give an indication of the required time for the memory to lose its "information" after it has been programmed.

6.2.2.1 Write/Erase Endurance Testing

In the endurance testing, a write pulse of +10V and pulse width of 100ms is applied to the transistor gate followed by a similar duration erase pulse of –10V. The transistor memory device is subjected to a total of 10^4 W/E cycles with its threshold voltage monitored at selected intervals. From Fig 6.6, it could be seen that no observable collapse of the threshold voltage window has occurred after 10^4 W/E cycles. This suggests that there is negligible degradation of the tunnel dielectric after the W/E endurance test.

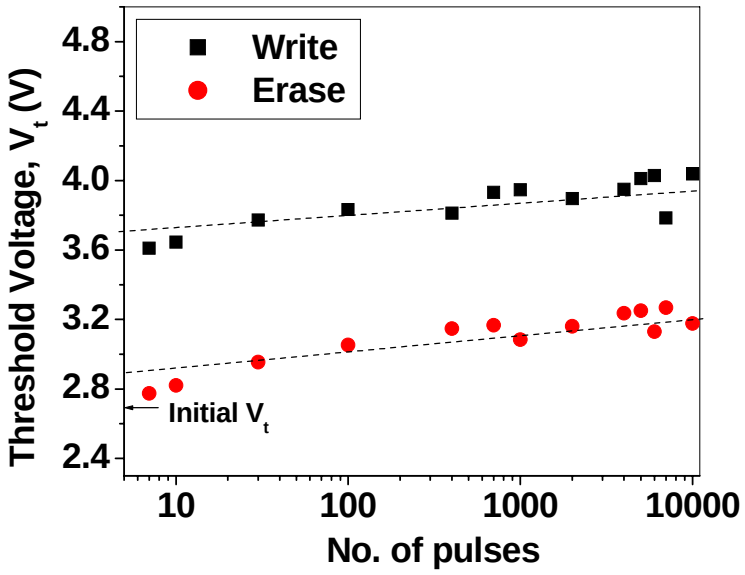

Figure 6.6: Data endurance characteristics. ±10V, 100ms pulses are applied for write/erase cycling of the nanocrystal transistor memory device. Write and erase conditions were (10V, 100ms) and (–10V, 100ms), respectively.

6.2.2.2 Charge Retention Testing

The data retention characteristic was obtained by monitoring the change of the device V_{th} with time after an initial programming or erasing pulse. The device gate was grounded during the charge retention test. Figure 6.7 shows a typical result of the drain current (I_d) versus gate voltage (V_g) plot at the specified time duration after a programming pulse of 10V for 200ms was applied. It is noted that the nanocrystal transistor memory device gradually "loses" its programmed data as observed from the leftwards shift of the I_d-V_g curves as time elapsed during the retention test increases.

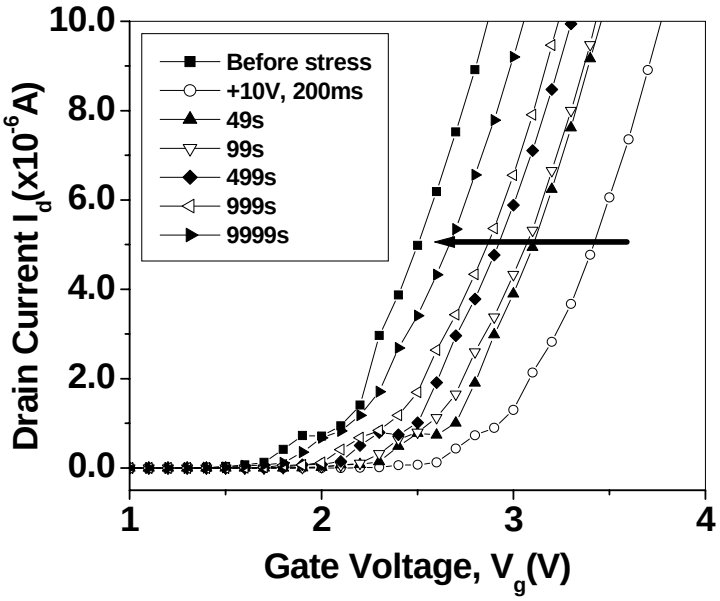

Figure 6.7: Various I_d versus V_g characteristics of the transistor memory device at the specified time durations after application of a write pulse of 10V for 200ms.

A summary of the V_{th} shift with respect to the elapsed time after the application of a gate voltage is shown in Fig. 6.8. The experiment is carried out for three sets of positive gate voltages (8V, 9V and 10V for programming) as well as three sets of negative gate voltages (-8V, -9V and -10V for erasing).

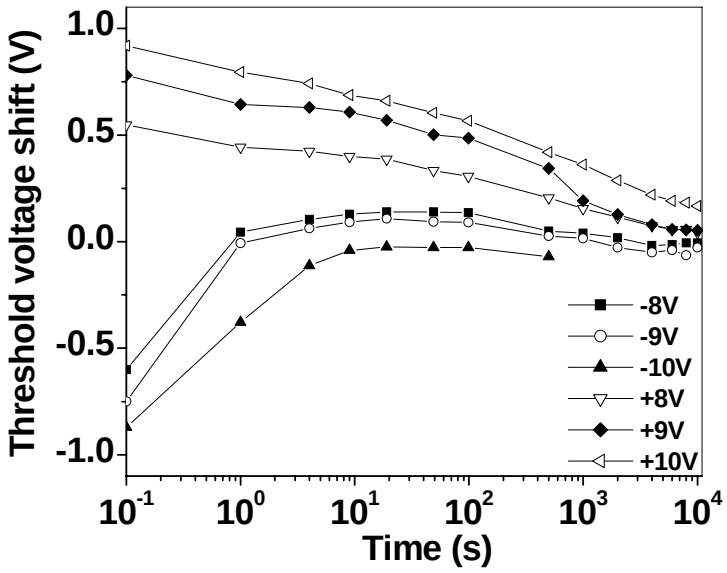

Figure 6.8: Room temperature charge retention characteristics of the nanocrystal transistor memory after Write and Erase pulses of (8V, 9V and 10V for 200ms) and (-8V, -9V and -10V for 200ms), respectively.

A slight difference in the discharge slope is observed for the positive gate pulse and negative pulse. Difference in the time for the threshold voltage shift to reach a constant value (saturation) is also observed for write and erase. It is seen that the device loses its initial stored charge at a slightly faster rate for the case when a negative pulse is applied compared to the case when a positive pulse is applied. This could be due to the slightly asymmetrical nature of the conduction and valence band offsets between the Ge nanocrystal with the HfAlO tunnel dielectric. The conduction and valence band offset between the Ge and HfAlO tunnel dielectric is 2.15eV and 3.19eV [3]-[4], respectively.

When a negative pulse is applied to the gate electrode, holes first tunnel from the valence band of the Si substrate to the valence band of the Ge nanocrystal. When the gate voltage is subsequently held at ground during retention, the holes will start to tunnel from the Ge nanocrystal valence band back to the Si substrate valence band. At the same

time, as the conduction band offset between the Ge nanocrystal and HfAlO tunnel dielectric is only 2.15eV, electrons may also tunnel from the Si conduction band to the Ge nanocrystal conduction band easily, reducing the net positive charge stored in the quantum well at a more rapid rate.

For the case when a positive pulse is applied to the gate electrode, electrons first tunneled from the conduction band of the Si substrate to the conduction band of the Ge nanocrystal. When the gate voltage is subsequently held at ground during retention, the electrons will start to tunnel from the Ge nanocrystal conduction band back to the Si substrate conduction band. Different from the earlier case, the probability of holes also tunneling from the valence band of Si substrate to the valence band of the Ge nanocrystal is lower because of the slightly larger valence band offset. The heavier effective mass of holes also makes such charge transport more difficult. In this case, the net negative charge stored in the quantum well will decay at a slightly slower rate.

6.3 Charge Storage and Discharge Mechanisms in Nanocrystal Flash Memories

Besides obtaining the electrical characteristics of the nanocrystal memory transistor with high-κ as the tunnel dielectric, it would be interesting to obtain some insights on the charge storage mechanism within such a structure. In this section, a review of previous work by other research groups on the extraction of trap energy level will first be presented, followed by the extraction of trap energy from our Ge nanocrystal devices.

6.3.1 Review of Previous Work on Extraction of Trap Energy Level

The charge storage mechanism in nanocrystal Flash memory devices has remained uncertain despite the considerable amount of effort devoted by many research groups. Interfacial defects of the nanocrystals seem to play a role in charge storage in recent studies [5]-[6], although storage in the nanocrystal conduction band by quantum confinement has been reported earlier [7]-[8]. As we have not observed definitive quantum confinement effects in the charge storage characteristics of our Ge nanocrystal memory structures, it is likely that charges are stored in trap energy levels within or at the surface of the Ge nanocrystals. The interface of bulk Ge and SiO_2 has been reported to have surface defect densities on the order of 10^{12} cm^{-2} [9]. Though the defect density is low on a nanocrystal (one defect per nc-Ge of 5 nm in diameter), the highly strained surface of each nanocrystal induces large surface stress which increases its defect density.

Figure 6.9 illustrates the discharging model based on deep level charge storage caused by trap levels at the interface of the nc-Ge. The model could be described by two discharging mechanisms with the first portrayed by paths A and B. The first charge decaying mechanism involves the emission of trapped electrons from the occupancy state to the conduction band of the nc-Ge (path A) followed by band-to-band tunneling into the Si substrate (path B). This mechanism has substantial dependence on temperature as the probability for the emission of trapped electrons to the conductance band would increase with thermal excitation. The second decaying mechanism, depicted by path C which has lower temperature dependence, is trap-to-trap tunneling of electrons from the occupancy state to the Si substrate/tunnel dielectric interface states.

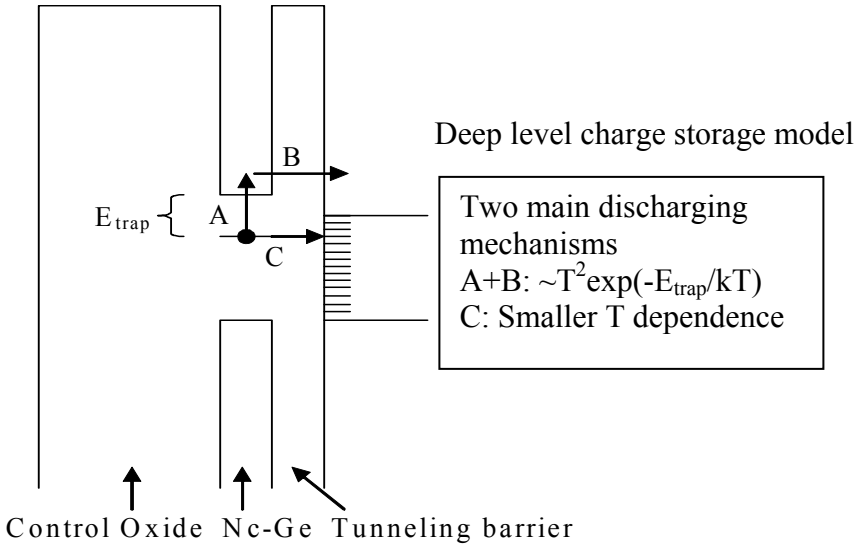

Figure 6.9: Model of deep level charge storage and discharging mechanisms [5].

By postulating this model, Baik *et al*. [5] have proposed the following method to extract the trap energy level responsible for charge storage in silicon nanocrystals. This method is based on the study of the discharging time constant (τ_E), determined at 90% of steady state of the transient drain current characteristics, at a particular read voltage after writing, conducted over a range of temperature. The drain current transient typically exhibits a monotonically increasing curve which is due to the discharging of stored electrons in the nanocrystal array. This discharging kinetics can be understood as a collective effect of individual nanocrystals discharging. The lifetime of an electron stored in a quantum dot or nanocrystal follows an exponential distribution [10]. The drain current (I_D) transient is represented as a step function $u(t-t_i)$, where t_i is the lifetime of the stored electron in each nanocrystal. The probability distribution function of t_i with mean λ can be expressed as follows [5]:

$$f(t = t_i) = 1- \exp(-\lambda t_i) \qquad (6.1)$$

In the nanocrystal memory structure, electrons are stored in many nanocrystals, each with its own individual lifetime t_i. Thus, the I_D transient can be represented as follows:

$$g(t) = \sum_{i=1}^{n} u(t - t_i) \tag{6.2}$$

where a total of *n* nanocrystal charging sites is assumed.

When an electron is released from the nanocrystal at $t = t_i$, a step increase in the drain current would result. The I_D transient curve can be represented by a summation of the step increases over the elapsed time. Pictorially, this explanation is illustrated by the schematic diagram in Fig. 6.10.

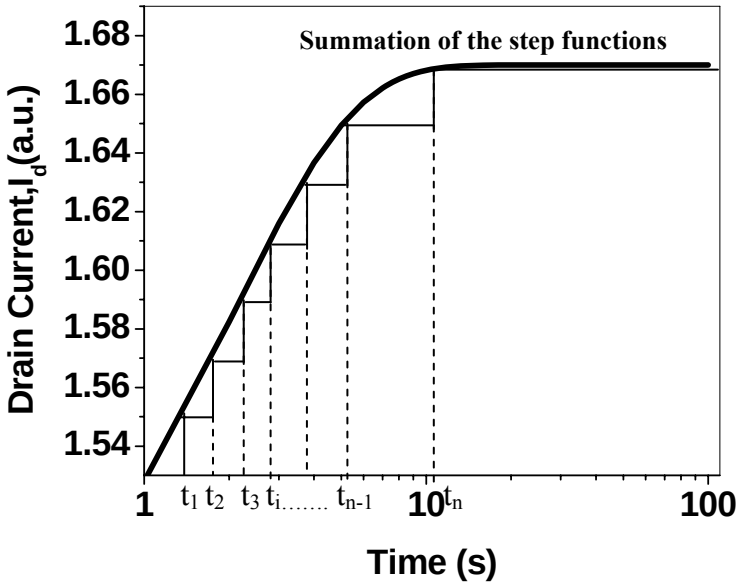

Figure 6.10: Pictorial explanation of the formation of the transient drain current during the discharging process. A step increase in the drain current is resulted when an electron is de-trapped from a nanocrystal into the Si substrate at time $t=t_i$. The drain current transient curve could be represented by a summation of these step functions over the elapsed time throughout the discharging process.

To obtain the envelope of g(t), the expected value of g(t) could be used because the function contains a random variable t_i. The probability for g(t) to be equal to *k* is

$$P(g(t)=k)=\binom{n}{k}(1-\exp(-\lambda t))^{k}(\exp(-\lambda t))^{n-k} \tag{6.3}$$

where *k* represents the total number of electrons released from the nanocrystals during the discharge phase.

Then, the expected value of g(t) is

$$E(g(t))=\sum_{j=1}^{n} j\binom{n}{j}(1-\exp(-\lambda t))^{j}\times(\exp(-\lambda t))^{n-j}=n(1-\exp(-\lambda t)) \tag{6.4}$$

The I_D transient shows a similar curve as predicted by Eq. (6.4), although it does not exactly coincide with the equation. However, this model approximately describes the collective feature of the discharging phenomena, namely monotonic increase with a certain asymptotic value. In addition, the extension of this model is possible using multiple λ's, if there is more than one dominant discharging mechanism.

In general, if there are two dominant discharging mechanisms, then

$$E(g(t))=n_1(1-\exp(-\lambda_1 t))+n_2(1-\exp(-\lambda_2 t)) \tag{6.5}$$

where $n_1+n_2 = n$. λ_1 and λ_2, represent two different discharging mechanisms.

In Baik *et al.*'s work [5], the drain current transients (obtained at three different temperature of 260K, 373K and 423K) with read voltage (V_R) of 3 V after writing at 4V

for 10s are shown in Fig. 611. Each curve was fitted according to Eq. (6.5) and the discharging time constant (τ_E) was determined at 90% of the I_D at steady state. The inverse of τ_E is directly proportional to the discharging current if we assume that the injected charge is almost constant for temperature (T).

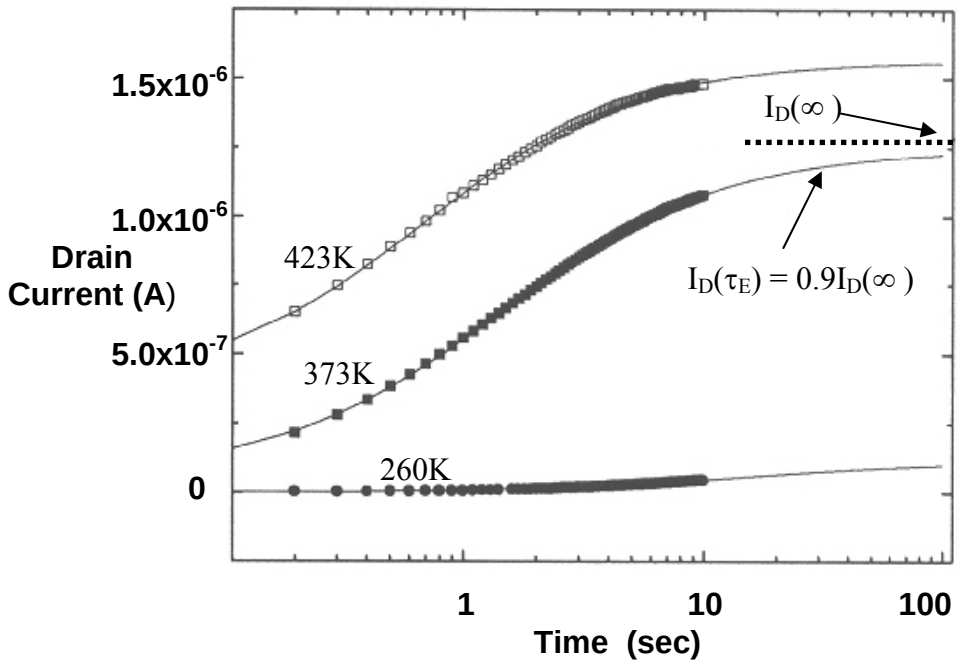

Figure 6.11: Drain current (I_D) transient at the read voltage (V_R) of 3 V after writing at 4V. Symbols represent measured data and the lines are fitted data [5].

Figure 6.12 shows the $1/\tau_E T^2$ versus 1/T at several read conditions. The indicated activation energy can be interpreted as the position of the energy level of deep trap level electron storage as well as the presence of two main discharging mechanisms [11]: thermal activation (T^2 plus exponential dependence) and direct tunneling (independent of temperature T) to the silicon channel conduction band, and direct tunneling to the interface states in-between the tunnel oxide and the Si channel.

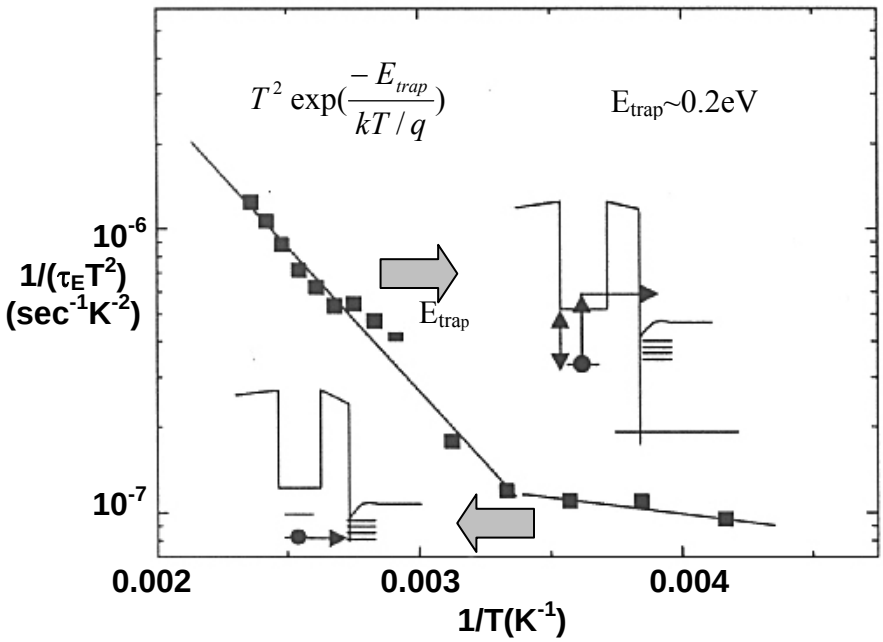

Figure 6.12: Inverse of the discharging time constant divided by squared temperature (T) at various read voltage and temperature T [5].

Based on this method, an activation energy of 0.2eV was extracted for Si nanocrystal in Baik *et al.*'s work [5]. The extracted value is quite reasonable considering the deep levels of Si nanocrystal [12]. On the other hand, at lower temperatures the temperature dependence is absolutely smaller than E_{trap} and in this region the direct tunneling from the deep trap level to the interface states in between the SiO_2 and the channel Si is the dominant discharging process.

6.3.2 Extraction of Trap Energy Level from Germanium Nanocrystal Transistors

The trap energy level of our Ge nanocrystal memory transistors with high-κ HfAlO as the tunnel dielectric is then extracted based on the method discussed in Section 6.3.1. A write pulse of 8V is first applied for 60s followed by a read voltage (V_B). The discharging time constant is obtained by measuring the drain current (I_D) transient during the application of V_R. Figure 6.13 shows the I_D transients at various temperatures with V_R of 4V after writing at 8V for 60 s. Each transient exhibits a monotonically increasing curve due to the discharging of stored electrons in the nc-Ge. The increase in I_D for higher temperatures could be explained by the larger carrier mobility and the higher intrinsic carrier concentration of the substrate. The increased intrinsic carrier concentration reduces the Fermi level (ϕ_F) of the substrate. This causes the voltage drop at the substrate (~$2\phi_F$) during inversion to reduce which would then enhance the vertical electric field across the gate stack oxide.

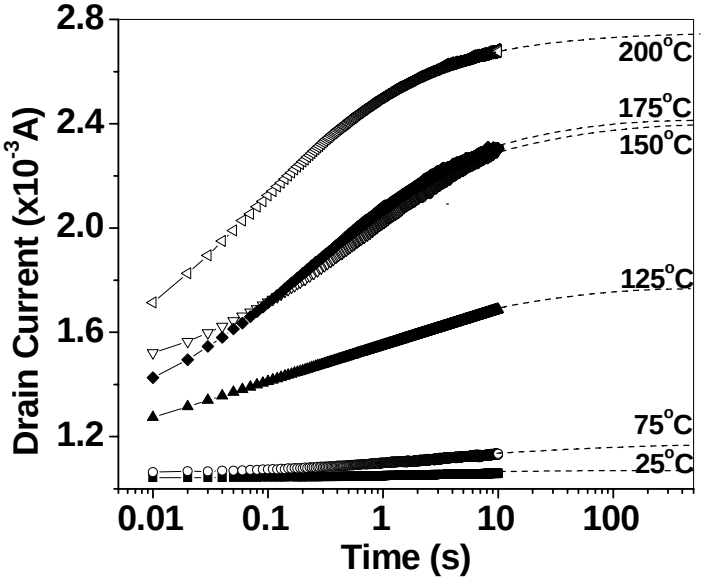

Figure 6.13: The drain current transient during the application of the read voltage at 4V, after the application of a write voltage of 8V for 60s.

The discharging time constant (τ_E) was determined to be the time corresponding to 90 % of I_D at steady state. The inverse of τ_E is directly proportional to the thermal equilibrium emission constant (e_n). Using the approach by Shockley, Read and Hall, the rate of emission (R_e) of electrons from traps in the nc-Ge is proportional to the number of occupied electron traps with the proportionality constant being the emission constant (e_n) [13],[14]:

$$R_e = e_n N_t f_t \tag{6.7}$$

where N_t is the total number of electron traps (cm^{-3}) and f_t is trap occupation probability which is given by the Fermi-Dirac distribution function.

The thermal equilibrium emission constant (e_n) can be simplified [15], yielding:

$$e_n(E_{trap}) = AT^2 \exp\left[-E_{trap}q \Big/ kT\right] \tag{6.8}$$

where E_{trap} is the trap energy level measured from the conduction band of the nc-Ge, A is a non-temperature-dependent constant, k is Boltzmann's constant and T is absolute temperature.

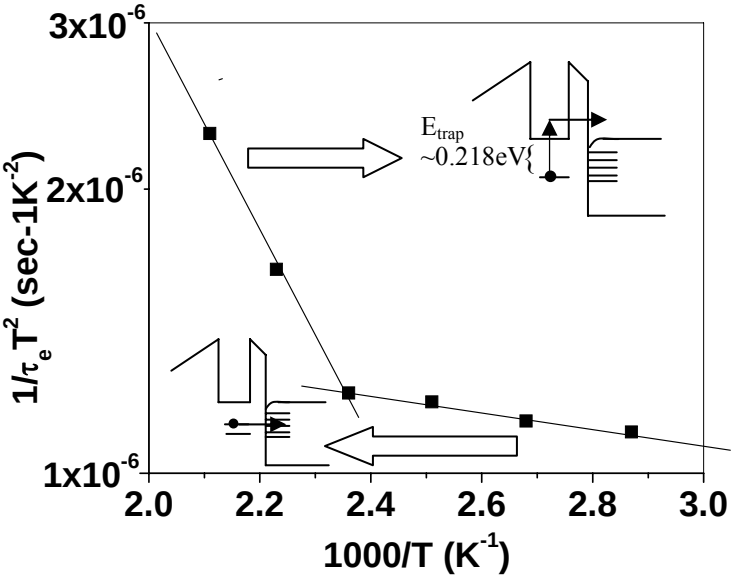

Figure 6.14: Inverse of the discharging time constant divided by squared temperature (T) versus the inverse of T for germanium nanocrystal memory transistors.

Figure 6.14 shows the $1/(\tau_E T^2)$ versus $1/T$ characteristics of the Ge nanocrystal transistors, where the extracted E_{trap} (0.218eV) is indicated by the gradient of the slope at high temperatures. At lower temperatures, the temperature dependence is very much smaller (can be assumed to be temperature independent) and this region indicates the dominance of direct tunneling of electrons from deep level traps to the interface states at the Si/high-κ tunnel electric interface.

6.3.3 Possible Origin of the Extracted Trap Level

The origin of traps in Ge has been investigated by many researchers. Among these, the vacancy-oxygen (VO) complex (*A* center) trap is more commonly known and such a trap or defect is usually induced by irradiation with high-energy particles in oxygen-rich Si and Ge nanocrystals. Recently, several papers have been published in which the vacancy-oxygen (VO) center in Ge was studied by means of high-resolution infrared absorption spectroscopy and deep-level transient spectroscopy (DLTS) measurements [16]-[20]. Markevich *et al.* have proposed the existence of doubly negative (VO^{2-}), singly negative (VO^{-}) and neutral (VO^{0}) charge states in Ge nanocrystals with two corresponding energy levels in the Ge bandgap at about (E_C - (0.20-0.23)eV) and (E_V + 0.27 eV) [20].

In another experiment, Haesslein *et al*. identified the mono-vacancy and self-interstitial in Ge using perturbed angular correlation spectroscopy (PACS) and DLTS [21]. The authors found a donor level lying (0.04 ± 0.02)eV below the conduction band edge. However, da Silva *et al*. [22] suggested that the PACS data in Haesslein *et al*. [21] should be reinterpreted in terms of a donor level at (E_V + 0.31 eV) which is 0.12 eV below the conduction band edge and an acceptor level between 0.11 and 0.16 eV. In such a self-interstitial induced trap level, the source and location of self-interstitial defects is typically introduced by the highly strained/stressed surface of each nanocrystal.

The experimentally extracted trap energy level of 0.218eV from this work lies near to the predicted trap energy due to vacancy-oxygen (VO) complex (*A* center) defects in Ge. This suggests that the VO complex (A center) defects in the Ge nanocrystals may possibly be responsible for the charge storage in our Ge nanocrystal devices. These VO

defects may be introduced as a result from the physical impact during sputter-deposition of the Ge layer and the SiO_2 capping layer. As the Ge nanocrystals are covered by the SiO_2 surrounding, the oxygen-rich SiO_2 host matrix is likely to provide favorable condition for the formation of VO trap defects.

6.4 Alternative Method for Extraction of Trap Energy Level

In section 6.3, the extraction of the trap energy level is based on the study of the transient drain current during device discharging. The retention time is proportional to the depth of the trap level in the Ge nanocrystal and inversely proportional to temperature. If the trap level is deep, it would be more difficult for the trapped charges to be completely released from the trap sites, resulting in the transient drain current taking a longer time to rise and arrive at a steady state condition during the discharge process. The rate of discharge is gauged by the time for the transient to reach 90% of the steady state condition. Similar to the method discussed in Section 6.3, an alternative approach to extract the trap energy level of the Ge nanocrystals would be proposed. This method is based on the study of the difference in the drain current with its initial state (during the discharge process) and will be described as follows.

The linear drain current of a transistor can be approximated by [23]:

$$I_{D(lin)} = \mu \frac{W}{L} C_{ox}(V_G - V_{th})V_D \tag{6.9}$$

where the $0.5V_D^2$ term is neglected for small V_D, μ is the mobility of the minority charge carrier in the inversion channel, W/L is the channel width to channel length ratio, C_{ox} is the oxide capacitance, V_G is the gate voltage, V_{th} is the threshold voltage and V_D is the drain voltage of the transistor device.

After some re-arrangements, Eq. (6.9) could be rewritten as:

$$C_{ox}(V_G - V_{th}) = \frac{I_D}{\mu \frac{W}{L} V_D} = K_1 I_D \tag{6.10}$$

where K_1 is a constant for a fixed V_D.

The threshold voltage of a transistor is given by [23]:

$$V_{th} = V_{FB} + \gamma \sqrt{\phi_S} + \phi_S \tag{6.11}$$

where γ is the body effect parameter and ϕ_S ($=2\phi_F$) is the surface potential.

In a MOS system, the charge in the gate (Q_G) would be balanced by the oxide trap charge (Q_{ot}) as well as the charge in silicon (Q_s).

$$Q_G(t) = -Q_{ot}(t) - Q_s(t) \tag{6.12}$$

Since the gate voltage is fixed during the discharge experiment, $Q_G(t)$ is independent of time, that is,

$$Q_G(t) = Q_G \tag{6.13}$$

At time t = 0,

$$Q_G = -Q_{ot}(0) - Q_s(0) \tag{6.14}$$

At time t = *t*,

$$Q_G = -Q_{ot}(t) - Q_s(t) \tag{6.15}$$

By equating Eq. (6.14) and Eq. (6.15), the expression in Eq. (6.16) could be obtained.

$$Q_{ot}(0) - Q_{ot}(t) = Q_s(t) - Q_s(0) \tag{6.16}$$

where

$$Q_{ot}(0) = qn_o \tag{6.17a}$$

$$Q_{ot}(t) = qn_o \exp(-e_n t) \tag{6.17b}$$

The time-dependent silicon charge $Q_s(t)$ can be obtained from Eq. (6.10) as

$$Q_s(t) = C_{ox}[(V_G - V_{th}(t)] = K_1 I_D(t) \tag{6.18}$$

where V_G is time independent because it is fixed during the experiment. The threshold voltage $V_{th}(t)$ changes with time due to the detrapping of charges from the nanocrystals.

Using Eqs. (6.17a), (6.17b) and (6.18), Eq. (6.16) can be expressed as

$$qn_o[1-\exp(-e_n t)] = K_1[I_D(t) - I_D(0)] \tag{6.19}$$

If the argument in the exponential term in Eq. (6.19) is small (i.e., $e_n t << 1$), the following

$$\exp(-e_n t) \approx 1 - e_n t \tag{6.20}$$

Hence Eq. (6.16) can be simplified to

$$K_1[I_D(t) - I_D(0)] \approx e_n t \tag{6.21}$$

where $e_n = AT^2 \exp(-\frac{E_{trap}}{kT})$

After some mathematical re-arrangements, Eq. (6.21) can be simplified to Eq. (6.22):

$$\ln[\frac{I_D(t)-I_D(0)}{T^2}] = \ln K_2 - \frac{E_{trap}}{kT} \tag{6.22}$$

Using this approach, the E_{trap} level could be extracted based on the analysis of the change in the drain current at time t with respect to the initial state, instead of finding the discharging time constant corresponding to the point for the drain current to reach 90% of the steady-state.

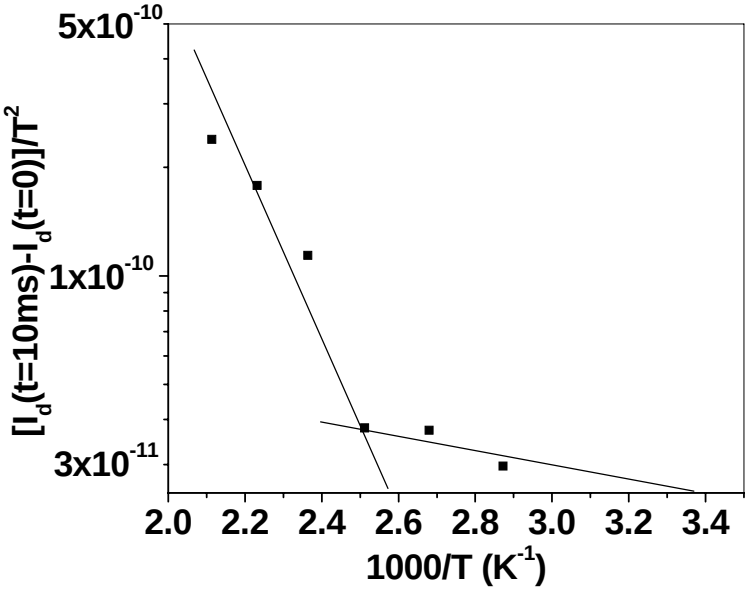

Figure 6.15: Drain current difference during discharging divided by squared temperature (T) versus the inverse of T.

From the gradient obtained in the plot shown in Fig. 6.15, an energy level of 0.25eV is extracted based on this alternative method. This value is very close to the value of 0.22eV obtained by finding the discharging time corresponding to the point for the drain current to reach 90% of the steady-state. Data points of t= 10ms, 20ms, 30ms and 40ms have been used for the extraction of the trap energy level. It is generally found

that a smaller value of t would result in a more accurate extracted value. This is due to Eq. (6.18) where the approximation used in the series expansion requires the time, t, to be small.

6.5 Trap Level Enginnering

Several methods can be introduced to increase the charge retention time. The most convenient method is to increase the tunnel barrier thickness to prevent the charges stored in the nanocrystals from leaking into the Si-substrate easily. However, this method would result in a longer write and erase time for the same write and erase voltages. Another method is to utilize a novel tunnel barrier structure which would increase the barrier thickness but not compromising on the write and erase time [24],[25]. The third method is to introduce deeper trap levels into the Ge bandgap so that charges could not be easily released during charge storage. The calculated range of the discharge time constant for nanocrystalline silicon memory can vary up to an order of 10^9 times when the trap level is shifted from the conduction band edge to midgap [5]. One way to introduce deep traps in the Ge bandgap would be to change the surrounding host matrix of the Ge nanocrystals. This is based on the assumption that trap sites in the nanocrystals responsible for charge storage are related to the interfacial defects between the nanocrystal and its surrounding matrix.

Two basic capacitor structures with nc-Ge embedded within the dielectric of similar tunnel but with different capping materials have been fabricated for proof of concept of the change in charge retention time due to different trap energy levels associated with different host matrix. In the first device, to implement a partial high-κ

host matrix surrounding the nanocrystals, only the tunnel dielectric layer is composed of the high-κ material whereas the capping layer remains as the conventional SiO_2. In the second device, to implement a full high-κ host matrix surrounding the nanocrystals, HfAlO is used for both the tunnel dielectric layer as well as the capping layer. Both devices have similar tunnel dielectric consisting of 5nm of high-κ material (1nm SiO_xN_y and 4nm HfAlO). The capping layer for one device is made up of 20nm of SiO_2 while the capping layer for the other device is 20nm of HfAlO. Temperature dependent capacitance-time (C-*t*) measurements were then carried out on these two capacitor structures. The retention time for the device at various temperatures is defined by the time taken for the capacitance to decrease to a normalized capacitance value of 0.5. The Arrhenius plot of retention time in Fig. 6.16 shows the temperature dependence of the charge retention time in Ge nanocrystal structures with different capping layers. Nanocrystalline-Ge embedded in full HfAlO host matrix shows higher temperature dependence than that of partial (SiO_2/HfAlO) host matrix indicating different activation energies for discharge of the stored electrons. The difference in activation energy of the two cases suggests that the nc-Ge embedded in full HfAlO host matrix could possibly generate deeper trap levels than the nc-Ge embedded in partial (SiO_2/ HfAlO) matrix. It is unlikely that the different temperature dependence of the retention time in Fig. 6.16 is due to a difference in the current transport mechanism through the capping layer during discharge. This is because the HfAlO capping layer is expected to experience a much smaller electric field across it as compared to the SiO_2 capping layer of similar physical thickness because of the larger dielectric constant of the HfAlO. This would mean that the charge transport across the HfAlO layer would tend towards the direct tunneling

regime. The large temperature dependence of the HfAlO capping oxide device in Fig. 6.16 rules out direct tunneling as such a mechanism is independent of temperature. The larger temperature dependence of the HfAlO capping oxide device has to be explained by other reasons, for example the deeper trap energy level in the nc-Ge.

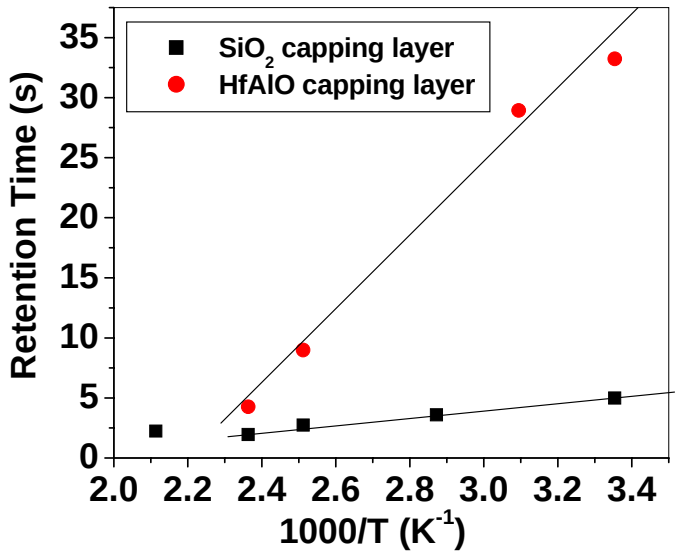

Figure 6.16: Temperature dependence of retention time for nc-Ge capacitors with SiO_2 capping layer and HfAlO capping layer.

6.6 Summary

In this chapter, the electrical characteristics of the nanocrystal memory transistor device with high-κ as the tunnel dielectric have been investigated. In the transient programming study, it was found that the device requires pulse amplitude of 10V for about 6ms to result in a threshold voltage shift of 1V. In the write/erase endurance studies, no significant collapse of the threshold window is observed after 10^4 W/E cycles. This suggests that there is negligible tunnel dielectric degradation during W/E endurance. In the discharge experiments, conducted over a range of temperature ranging from 25^{o}C

to 200^{o}C, a trap energy level of 0.218eV has been extracted based on the study of the discharging time constant at a read voltage of 4V after the device has been charged (programmed) at 8V for 60s. This trap energy value suggests that the VO complex (A center) defects in the Ge nanocrystals may be responsible for the charge storage in our devices. An alternative method to extract the Ge trap energy level has been proposed. This method is based on the study of the change in drain current compared to its initial state during the discharging process. The trap energy level obtained by the alternative method has a value of 0.25eV, which is close to the value derived using Baik *et al.*'s method [5]. The proposed alternative method has a physical basis and the advantage of not requiring a fit of experimental data to an assumed analytical discharge expression. It was also found that the trap energy level could be engineered by modifying the host matrix of the Ge nanocrystals. Better charge retention and greater temperature dependence of the retention time (indicative of deeper traps) could be achieved by employing a full high-κ host matrix consisting of HfAlO as the tunnel and capping dielectric as compared to a device with only HfAlO as the tunnel dielectric but SiO_2 as the capping layer.

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Chapter 7: Conclusion

7.1 Summary

In the downscaling of transistor devices, the introduction of high-κ materials offers a promising solution to address most of the limitations encountered by the conventional SiO_2 gate dielectric. Among the alternative gate dielectric materials studied in the literature reviews, ZrO_2 and HfO_2 emerge as the more suitable candidates to replace SiO_2.

In the initial stage of the project, MIS capacitor devices with high-κ ZrO_2 as the dielectric material were first fabricated and characterized. It was found that the gate leakage current is more related to the degree of the crystallization of the dielectric than the interface state density between the dielectric layer and Si substrate. This could possibly be due to the relatively large physical thickness of the high-κ film which makes the interfacial region less important than the bulk insulator properties in determining the leakage performance of the devices. In the charge transport mechanism study, it was found that only the F-P emission mechanism fit the measured J_g-V_g data between electric fields of 2.0 and 3.2 MV/cm in the interfacial layer (corresponding to $0.7 < V_g < 2$ V). The Schottky emission mechanism, however, does not fit the measured J_g-V_g data at all. For the bulk ZrO_2 layer, both Schottky and F-P emission mechanisms do not fit the measured J_g-V_g data over electric fields in the bulk ZrO_2 from 0.7 to 1.9 MV/cm (corresponding to $0 < V_g < 2$ V).

MIS capacitor devices with another high-κ dielectric material, HfO_2, have also been fabricated and studied. HfO_2 was also found to be a promising candidate as an alternative gate dielectric material. The crystallization temperature of HfO_2 could be further raised to 1000^oC when it was doped with Al to form HfAlO.

In the fabrication of nanocrystal memory device with high-κ as the tunnel dielectric, an experiment was first carried out to determine if the high-κ HfO_2 material provides a suitable platform for the growth of Ge nancorystals. It was seen that when the nanocrystal memory device with 5nm thick SiO_2 tunnel dielectric was replaced with a high-κ HfO_2 material of equivalent electrical thickness, no compromise in total charge storage was observed, a faster charging speed could be achieved due to the lower barrier height of HfO_2 with silicon and better charge retention characteristics could be attained due to the physically thicker HfO_2 layer.

The EOT of the HfO_2 dielectric was then further reduced from ~5nm to 1.9nm and studied. This thickness was well below the 2.5nm lower bound limit for conventional SiO_2 below which Ge penetration would have occurred and no proper charge storage could be obtained. For the nanocrystal memory device with HfO_2 of 1.9nm EOT as the tunnel dielectric, better charge storage capability (in terms of a lower program voltage) could be obtained, due to the smaller EOT and lower barrier height (as compared to SiO_2) of the high-κ HfO_2 layer, allowing easier tunneling of charge carriers from the substrate into the nanocrystals. The high-κ trilayer structure also showed better charge retention performance than the RTO (SiO_2) trilayer structure even though the EOT of the high-κ tunnel dielectric was smaller than that of the RTO tunnel dielectric.

The possibility of achieving enhancement in device performance by means of an increased gate electric field coupling factor has been investigated. The increase in electric field coupling factor was achieved by (1) reducing the thickness of the SiO_2 capping layer and (2) replacing the capping layer with a high-κ material. The thickness of the SiO_2 capping layer was first reduced from the original 50nm to 20nm. Results showed that SiO_2 capping layer with a reduced thickness of 20nm was able to result in better charge storage capability. At the same time, this reduced capping layer thickness was sufficient to prevent Ge outdiffusion into the ambient during high temperature annealing so that the Ge nanocrystals can be synthesized. The gate coupling factor was also increased by replacing the capping layer with a high-κ material. Significant enhancement in device performance in terms of charge storage as well as charge retention capabilities was attained.

The effect of different capping layers, affecting the electric field coupling from the applied gate bias, on the conductance characteristics of nanocrystal memory devices was also studied. It was found that the frequency dispersion of the conductance peak was most significant when the effect from interface traps was dominant, as in a device structure without nanocrystals. In structures where the effect from nanocrystals was dominant, the conductance characteristics show negligible frequency dispersion. It was also shown that G-V measurements could also provide a good estimate of the nanocrystal density in structures where the electric field coupling was high.

In the discharge experiments, conducted over a range of temperature ranging from 25^{o}C to 200^{o}C, a trap energy level of 0.22eV has been extracted based on the study of the discharging time constant at a read voltage of 4V after the device has been charged

(programmed) at 8V for 60s. This trap energy value suggests that the VO complex (A center) defects in the Ge nanocrystals may possibly be responsible for the charge storage in our devices. An alternative method to extract the Ge trap energy level has been proposed. This method is based on the study of the change in drain current compared to its initial state during the discharging process. The trap energy level obtained by the alternative method has a value of 0.25eV, which is close to the value derived using Baik *et al.*'s method [5]. The proposed alternative method has a physical basis and the advantage of not requiring a fit of experimental data to an assumed analytical discharge expression. It was also found that the trap energy level could be engineered by modifying the host matrix of the Ge nanocrystals. Better charge retention and greater temperature dependence of the retention time (indicative of deeper traps) could be achieved by employing a full high-κ host matrix consisting of HfAlO as the tunnel and capping dielectric as compared to a device with only HfAlO as the tunnel dielectric but SiO_2 as the capping layer.

7.3 Technology Perspective

The Ge nanocrystal memory structure, together with the employment of a high-κ HfAlO material as the host matrix, provides a promising solution to address the near-term industry requirements. In terms of financial considerations, minimal increase in the production cost is expected during the implementation of such a nanocrystal-based memory. No additional cost will be introduced as conventional CMOS processes can be utilized for its mass production. This results in easy integration of semiconductor nanocrystals into a mature mainstream CMOS process flow.

From the device performance perspective, the employment of a nanocrystal memory structure would result in better charge storage capability due to the absence of lateral leakage of charges. Besides being more robust to stress-induced leakage current, the drain-induced barrier-lowering effect on such a structure is also less severe compared to conventional floating gate devices as smaller operating voltages are involved. In this aspect, improvements in write/erase endurance and punch-through characteristics could be achieved.

7.3 Recommendation for Future Work

Although the nanocrystal memory structure seems to be a viable alternative to extend the limits of conventional floating gate memories, further research work is still necessary to fine-tune its performance. The following are some of the suggestions.

Due to the spread of dot size and density, fluctuation in electrical characteristics such as variation in the threshold voltage along the channel could result. Better control in the size and spatial distribution of nanocrystals is necessary to minimize such a fluctuation. This could be achieved by using an anodic alumina membrane template to ensure the orderly growth of the nanocrystals during the high temperature annealing stage [2]. However, due to its inherent physical dimension, the introduction of such a template would usually impose a ceiling on the amount of nanocrystals which could be grown. Research on increasing the nanocrystal density using such a template should be carried out.

Besides using a semiconductor material such as Si or Ge as the nanocrystal material, metallic elements could also be considered [3]-[6]. The main advantage of metal nanocrystals is its wide range of available work functions [7]. This provides one more

degree of design freedom to engineer the tradeoff between write/erase and charge retention because the work function of nanocrystals affects both the depth of the potential well at the storage node and the density of states available for tunneling in the substrate. By aligning the nanocrystal Fermi level to be within the Si band gap during retention operation and above the conduction band edge during erase operation, a large erase-current/retention-current ratio can be achieved even for very thin tunnel oxides. Since writing is performed by electrons tunneling from the Si substrate into the nanocrystals and the available states for the electrons to tunnel into can be readily found, fast write/erase and long retention time can be achieved simultaneously in metal nanocrystal memories.

In addition, metal nanocrystal memories have higher density of states around the Fermi level [7]. Hence more electrons can be stored per nanocrystal compared to dielectric or semiconductor materials. Metal nanocrystals also provide a great degree of scalability for the nanocrystal size [7]. To enable single-electron or few-electron memories based on the Coulomb blockade effect, smaller nanocrystals are preferred. However, for semiconductor and possibly dielectric nanocrystals, the band-gap of nanocrystals is widened in comparison with that of the bulk materials due to the multi-dimensional carrier confinement, which reduces the effective depth of the potential well and compromises the retention time. This effect is much smaller in a metal nanocrystal device because there are thousands of conduction-band electrons in a nanocrystal even in charge neutral state. As a result, the increase of Fermi level is minimal for metal nanocrystals of nanometer size. Some experimental works on the treatment of indium–tin oxide (ITO) by thin Pt films have indicated that the work

function of metal thin-films does not deviate from their bulk value dramatically down to about 0.4 nm in thickness [8]. The Coulomb blockade effect can be better exploited with metal nanocrystals to achieve ultra low-power memories without compromising the retention time from quantum mechanical confinement effects.

Despite the above advantages, the main disadvantage of metal nanocrystals is possible metal contamination. The metal materials considered so far are Ag [3], Pd [4], Au and Pt [5] and W [9]. If the metal diffuse through the thin tunnel oxide and contaminate the silicon substrate, deep level defects will be produced. This will seriously degrade the carrier mobility of the memory transistor. For example, Au introduces two deep level defects, an acceptor level (E_C - 0.55 eV) and a donor level (E_v + 0.34 eV) into the band gap of silicon [10]. Pt introduces deep level defects at E_C –0.23 eV and E_v +0.34 eV [11] while Pd introduces a defect at E_C –0.23 eV [11]. The Ag defect levels are at E_C –0.593 eV and E_v +0.405 eV [12] and those of W are at E_v+0.22 eV, E_v+0.33 eV, and E_C–0.59 eV [13]. The metal nanocrystal fabrication process would also need dedicated front-end equipment to avoid possible metal contamination to subsequent processing stages. Although metallic nanocrystal is an alternative worth consideration, its side-effects need to be addressed before this method becomes truly viable.

It has been shown in this project that the performance of a nanocrystal memory structure could be enhanced by replacing the conventional SiO_2 tunnel dielectric and capping layer with high-κ HfAlO material. Other high-κ materials, such as La_2O_3 [14]-[17]and Y_2O_3 [18]-[20], could also be investigated. The trap energy level in Ge nanocrystals, which is responsible for the charge retention capability in the memory

device, can be engineered and further improved upon through the selection of other suitable high-κ materials as host matrices.

A direct way to achieve low programming voltage with good charge retention performance is to make use of a tunnel dielectric with a small conduction band offset and with a sufficiently large physical thickness to limit the direct tunneling current leakage. Such properties of the tunnel dielectric can be obtained from a suitable high-κ material. Another way to achieve the above goals is to make use of a tunnel dielectric stack where the potential maximum is not at the dielectric-silicon interface but somewhere in the middle of the tunnel dielectric thickness. Such a potential barrier in the tunnel dielectric is termed as a crested barrier [21]. A tunnel dielectric stack with such a crested barrier can be formed from a sandwich of three dielectric material layers, a thin high-κ layer followed by a thin silicon dioxide as the middle layer and another thin high-κ layer as the third layer. The crested barrier has several advantages. The barrier to electron injection, and consequently the programming voltage, is not determined by the potential maximum but by the conduction band offset at the silicon-dielectric interface, which is much lower than 3.15eV (typically 1.5eV for a suitable high-κ material). However, the charge retention performance is determined by the potential maximum, or the maximum barrier seen by the tunneling electrons (typically 3.2eV), and the physical thickness of the dielectric stack, which is another advantage. The nanocrystal memory structure could adopt such a combination of materials for its tunnel dielectric layer for better device performance.

In the formation of the high-κ tunnel dielectric, a surface nitridation step is usually necessary prior to the deposition of the actual high-κ tunnel dielectric to prevent

the growth of interfacial oxide during post-deposition steps involving high temperature [22]-[23]. Although this surface nitridation step is necessary to maintain a constant EOT, a trade-off in carrier mobility of the resultant transistor device is resulted. In more recent studies, it has been found that hafnium nitride (HfN) is an excellent barrier against oxygen diffusion [24]-[27]. When used as the gate electrode material, HfN is able to prevent the growth of interfacial oxide without the need for surface nitridation prior to tunnel dielectric deposition. From the fabrication point of view, this would result in the elimination of one process step while from the device performance point of view, a faster operation speed could be achieved as the mobility of charge carriers in the channel would not be compromised. It is hence recommended that HfN be used as the gate electrode material in future fabrication of high-κ nanocrystal memory devices.

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