Hf-BASED HIGH-K GATE DIELECTRIC AND METAL GATE STACK FOR ADVANCED CMOS DEVICES

JOO MOON SIG

NATIONAL UNIVERSITY OF SINGAPORE

2006

Founded 1905

Hf-BASED HIGH-K GATE DIELECTRIC AND METAL GATE STACK FOR ADVANCED CMOS DEVICES

JOO MOON SIG

A THESIS SUBMITTED FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

NATIONAL UNIVERSITY OF SINGAPORE

2006

ACKNOWLEDGMENTS

First and foremost, my deepest gratitude to my supervisor, Associate Professor Cho Byung-Jin, who provided me the opportunity to join Silicon Nano Device Lab (SNDL) and has given me guidance with God's love during my graduate study at NUS. Without his guidance, it would be difficult for me to have completed this thesis.

I would also like to take this opportunity to express my sincere thanks to my co-supervisors, Professor Kwong Dim-Lee and Dr. N. Balasubramanian in Institute of Microelectronics (IME). Without their support and advice, much of this thesis would have been impossible. Especially, I could not forget the moment when Prof. Kwong was encouraging me.

My gratitude also to the other advisors and teaching staffs in SNDL; Professor Li Ming Fu, Dr. Zhu Chunxiang, Professor Albert Chin, Associate Professor Yoo Won-Jong, Associate Professor Ganesh Samudar, Dr. Yeo Yee Chia, and Dr. Lee Sungjoo for their valuable pieces of comment and advice on my research work during internal meetings and seminars. My special gratitude to Prof. Daniel Chan who also provided me the opportunity to join SNDL.

I would like to greatly acknowledge Dr. Low WY, Kim SJ, and Yeo CC for the useful technical discussions. Many thanks to technical staffs and my fellows; Yong YF, Patrick Tang, O Yan WL, Lau BT, Park CS, Whang SJ, Hwang WS, Wu Nan, Chen JH, Debora Poon, Wang XP, Gao Fei, Ren Chi, Shen Chen, Dr. Samanta, Andy Lim, Tan YN, Zhang QC, and Yu XF. It was a joyful experience working with all of them.

Special gratitude to Deacon Park Eun-Bae who has prayed for my family and eagerly helped us in many ways.

Last but not least, my deepest love and gratitude go to my wife, Ju Kyoung-Ja, whose prayer and sacrifice throughout my study have made this work possible.

SUMMARY

With the continuous scaling of complimentary metal-oxide semiconductor (CMOS) devices, the high-K gate dielectric and metal gate stack is required for future CMOS devices with 65 nm technology node and beyond. The scope of this thesis includes studies on the high-K gate dielectric and metal gate stack for the future CMOS device application.

In this thesis, a new process for Al incorporation into HfO_2 is studied, and interactions between high-k dielectrics and metal gates are investigated. Firstly, a high quality HfAlO dielectric film using a single cocktail liquid source $HfAl(MMP)_2(OiPr)_5$ in Metal Organic Chemical Vapor Deposition (MOCVD) system as a new high-K fabrication method is demonstrated. A wide range of composition controllability between HfO_2 and Al_2O_3 in HfAlO is obtained by controlling deposition temperature. Higher temperature deposition introduces more hafnium into the film but there is a turn-around point of the composition ratio at the deposition temperature of 450ºC where the HfO_2 percentage is maximum of around 90% (Al_2O_3 10%). The HfAlO film with 90% HfO_2 (10% Al_2O_3), which has minimum sacrifice of K value (around 19), shows a great improvement in thermal stability and significant reduction of interfacial layer growth during subsequent thermal processes, leading to the reduction in leakage current by around 2 orders of magnitude compared to pure HfO_2 film. The HfAlO film with 90% HfO_2 also shows good compatibility with TaN metal gate electrode, under high temperature annealing process.

Secondly, thermal instability of effective work function ($\Phi_{m,eff}$) and its material dependence on metal/high-K gate stack are investigated. After high temperature rapid-thermal-annealing (RTA), change in $\Phi_{m,eff}$ value is observed and the phenomenon is attributed to the generation of substantial amount of extrinsic interface states at the

metal/dielectric interface. It is found that Si atoms at the interface play a critical role in the thermal instability of $\Phi_{m,eff}$. The behavior of $\Phi_{m,eff}$ can be explained with the types and locations of extrinsic interface states which are generated by silicon-metal bond during high temperature annealing.

Thirdly, a new approach to analyze and predict the behavior of $\Phi_{m,eff}$ in fully silicided (FUSI) gate/high-K dielectric stack and its interface configuration is proposed, using the combination of semi-empirical approach and metal-induced-gap-states (MIGS) theory. It is found that FUSI gate has effectively MSi_2 configuration at the gate dielectric interface. FUSI gate on high-K dielectric is evaluated to have much weaker Fermi-level pinning compared to polysilicon gate on high-K.

Lastly, new findings on the Fermi-level pinning phenomenon in FUSI gate/high-K dielectric stack are discussed. It is found that there is a critical composition ratio (C_{crit}) of Ni to Si in Ni-FUSI gate which starts to show a strong Fermi-level pinning and the C_{crit} is dependent on the underlying gate dielectric material.

CONTENTS

ACKNOWLEDGEMENTS **i**

SUMMARY **ii**

CONTENTS **iv**

LIST OF FIGURES **viii**

LIST OF TABLES **xiii**

LIST OF SYMBOLS **xiv**

LIST OF ACRONYMS **xvi**

CHAPTER 1 INTRODUCTION

1.1 MOSFET Scaling 1

1.1.1 Overview of MOSFET Scaling 1

1.1.2 Scaling of Current Gate Dielectrics and its Limits 3

1.1.2.1 Gate Leakage by Direct Tunneling 4

1.1.2.2 Impact on Device Operation 5

1.2 Motivation and Purpose of Thesis 7

1.3 Thesis Outline and Original Research Contributions 8

References 10

CHAPTER 2 LITERATURE AND TECHNOLOGY REVIEW

2.1 High-K Dielectric as an Alternative to SiO_2 13

2.1.1 Overview of High-K Dielectric 13

2.1.2 Figures of Hf-based High-K Dielectric 15

2.2 Issues with Hf-based High-K Dielectric 17

2.2.1 Thermal Stability 17

2.2.2 Interfacial Layer Growth and its Quality 18

2.2.3 Channel Mobility Related Issues 21

2.2.4 Threshold Voltage Related Issues 23

2.3 Metal Gate Electrode as an Alternative to Polysilicon Gate 25

2.3.1 Limitations of Polysilicon Gate ... 25
2.3.2 Metal Gate Technology ... 27
2.3.3 FUSI Gate Technology ... 30
References ... 32

CHAPTER 3 FORMATION OF HfAlO GATE DIELECTRIC USING SINGLE COCKTAIL LIQUID SOURCE IN MOCVD PROCESS

3.1 Introduction ... 41
3.2 Experimental ... 43
3.2.1 HfAlO Deposition using a Single Cocktail Source ... 43
3.2.2 Fabrication Procedures of MOS Capacitor and Transistor ... 44
3.2.3 Experimental Setup ... 45
3.3 Results and Discussion ... 47
3.3.1 Composition Ratio Control of HfAlO Film by Process Variation ... 47
3.3.2 Thermal Stability of HfAlO ... 51
3.3.3 Wet Chemistry of HfAlO ... 54
3.3.4 Interfacial Layer Growth ... 56
3.3.5 MOS Capacitors with TaN/HfAlO Gate Stack ... 57
3.3.6 MOSFETs with TaN/HfAlO Gate Stack ... 63
3.4 Summary ... 64
References ... 66

CHAPTER 4 THERMAL INSTABILITY OF EFFECTIVE WORK FUNCTION IN METAL/HIGH-K STACK AND ITS MATERIAL DEPENDENCE

4.1 Introduction ... 70
4.2 Theoretical Background of Metal-Dielectric Interface ... 71
4.2.1 Metal-Semiconductor Interface ... 71
4.2.2 Intrinsic States or Metal-Induced Gap States (MIGS) of Metal-Semiconductor Interface ... 72
4.2.3 Extrinsic States of Metal- or Polysilicon-Semiconductor Interface ... 74
4.3 Experimental ... 76
4.4 Results and Discussion ... 77
4.4.1 Intrinsic Properties of Metal/High-K Stack ... 77

4.4.2 Thermal Instability of Effective Work Function 80
4.4.3 Observed Phenomenon 85
4.4.4 Further Confirmation on the Effect of Si 87
4.4.5 Proposed Model...89
4.5 Summary 91
References...92

CHAPTER 5 THE INTERFACE CONFIGURATION AND FERMI-LEVEL PINNING OF FULLY SILICIDED (FUSI) GATE AND HIGH-K DIELECTRIC STACK

5.1 Introduction...96
5.2 Experimental 97
5.2.1 MOS Capacitor Fabrication and Experimental Set-up 97
5.2.2 FUSI Gate Formation Procedures 98
5.3 Theoretical Background: Semiempirical Approach..98
5.4 Results and Discussion 100
5.4.1 Interface Configuration of FUSI Gate/Gate Dielectric Stack................100
5.4.2 Implementation of MIGS theory on FUSI Gate/High-k Dielectric Stack 104
5.4.3 Fermi-level Pinning of FUSI Gate/High-k Dielectric Stack 105
5.5 Summary 107
References...108

CHAPTER 6 STOICHIOMETRY DEPENDENCE OF FERMI-LEVEL PINNING IN FULLY SILICIDED (FUSI) NiSi GATE ON HIGH-K DIELECTRIC

6.1 Introduction...111
6.2 Experimental 112
6.2.1 MOS Capacitor Formation Procedures 112
6.2.2 Experimental Set-up 113
6.2 Results and Discussion 113
6.3.1 Fermi-level Pinning Phenomenon in FUSI Gate/High-K Dielectric Stack 113
6.3.2 The Composition Ratio of Ni-FUSI Samples...115

6.3.3 Gate Dielectric Dependence of Fermi-level Pinning....117
6.3.4 Proposed Model....119
6.4 Summary....120
References....122

CHAPTER 7 CONCLUSIOINS
7.1 Conclusions....125

APPENDIX – LIST OF PUBLICATIONS 128

LIST OF FIGURES

Fig. 1.1 Illustration of Moore's law: number of transistors integrated in the different generations of Intel's microprocessors versus the production year of these circuits. 2

Fig. 1.2 The low voltage oxide conduction follows the theory of Direct-Tunneling where subtle change in barrier change from triangular to trapezoidal explains the leakage current significantly larger than those predicted by the Fowler-Nordheim theory. 5

Fig. 1.3 Power consumption and gate leakage current density for a chip that has a 15 Å thick SiO_2 gate dielectric compared to the potential reduction in leakage current by an alternate dielectric exhibiting the same equivalent oxide thickness. Assumes at total gate area of 0.1 cm^2. 6

Fig. 2.1 XPS spectra of ZrO_2 and polysilicon interface. ZrO_2 is decomposited after 950℃ annealing. 16

Fig. 2.2 XPS analysis of (a) Hf 4f, (b) O 1s, and (c) Si 2p of HfO_2 gate stack deposited on clean Si(100) at 450°C for 2 min followed by N_2 annealing at 800°C for 1min, poly-Si deposition at 600°C and N_2 annealing at 900°C and 950°C for 30sec. 16

Fig. 2.3 Hf ratio and k as a function of distance from Si substrate. Due to fitting (inset) with experimental EOT (diamonds) and estimated EOT (solid curve), SiO_2 of 4 Å thickness seems to exist. 20

Fig. 2.4 Schematic model of fixed charge centers and electron trap charge centers in HfSiO/SiO_2 dielectric stack. The electron trap charge centers that are located at the HfSiO/SiO_2 interface are probably responsible for the mobility reduction. 22

Fig. 2.5 Flat-band voltage versus number of HfO_2 ALD cycle. The V_{fb}'s for n+ and p+ gates converge as the number of ALD cycles is increased. (Inset: ΔV_{fb} versus number of HfO_2 ALD cycles). 25

Fig. 2.6 Required EOT for each gate electrode with different poly doping concentration versus technology node, where hp stands for the industry's most aggressive half-pitch target. 27

Fig. 2.7 C-V curves of nMOS transistors with W/L=50 μm/0.4 μm. Co-FUSI gate suppresses poly-depletion and induces a V_{fb} shift. 31

Fig. 3.1 The chemistry of the single cocktail liquid source: $HfAl(MMP)_2(OiPr)_5$ 44

Fig. 3.2 Dependence of composition ratio on process parameters such as (a) Ar carrier flow rate, (b) O_2 flow rate, and (c) Liquid precursor flow rate. Deposition temperature is 400ºC. The composition ratio is not much affected by the flow rate. 48

Fig. 3.3 XPS depth profiles of HfAlO films deposited at (a) 350ºC, (b) 450ºC, and (c) 600ºC. The 350ºC sample exhibits Al-rich property while the 450ºC and 600ºC samples exhibit Hf-rich property. 49

Fig. 3.4 Temperature dependence on deposition rate and composition ratio of HfAlO. The composition ratio changes over a wide range and shows a very strong correlation with the deposition rate. 50

Fig. 3.5 XTEM images of HfO_2 and HfAlO after 700ºC in-situ PDA treatment. HfAlO layer remains amorphous while HfO_2 is crystallized. Both films were deposited at 400ºC without surface nitridation. 51

Fig. 3.6 XRD spectra of (a) HfO_2, (b) HfAlO-400, and (c) HfAlO-450 after annealing at different temperatures. As-deposited HfO_2 is already crystallized while HfAlO remains amorphous up to 800ºC. 53

Fig. 3.7 The dependence of etch rate at a dilute 1% HF (1:100 DHF) solution of HfO_2 and HfAlO films on deposition and RTA temperature. The dashed line that is the etch rate of conventional thermal oxide (SiO_2) is a guide for the eyes. 55

Fig. 3.8 Increment of interfacial layer (I.L.) of HfO_2 and HfAlO before and after high temperature RTA at 950ºC for 30 second. The thickness of interfacial layer was measured using spectroellipsometry. While HfO_2 with surface nitridation (SN) shows the interfacial layer increase of around 4.5 Å, HfAlO with SN has little change in interfacial layer thickness from the fact that the increase of interfacial layer is less than 1 Å. 57

Fig. 3.9 Normalized C-V curves for HfO_2 and HfAlO films deposited at different temperature. The V_{fb} values of all HfAlO samples show slight positive shifts. 58

Fig. 3.10 (a) *K*-values of HfO_2 and HfAlO films. HfAlO deposited at 450ºC shows acceptable *K* value of 19. (b) Evaluation of K value of HfAlO-450 film after high temperature RTA at 950°C for 30 sec. The K value of around 20 is maintained after high temperature RTA. 60

Fig. 3.11 (a) Leakage currents of 40 Å HfAlO and HfO_2 before and after 950ºC RTA. RTA was done before the formation of TaN electrode. (b) I_g vs. EOT of HfAlO and HfO_2 before (▲,Δ) and after (●,○) 950ºC RTA treatment. Solid symbols represent the HfAlO and open symbols represent the HfO_2, respectively. The leakage current was measured at the gate voltage of $-1V + V_{fb}$ ($Ig@-1V+V_{fb}$). 62

Fig. 3.12 Leakage currents of 40Å HfAlO and HfO_2 before and after 950ºC RTA. RTA was done after the formation of TaN electrode. HfAlO shows better compatibility with TaN gate electrode. 63

Fig. 3.13 Transconductance (G_m) and drain current (I_d) characteristics of TaN metal gate NMOSFETs with HfAlO (solid lines) or HfO_2 (dotted lines) gate dielectrics. 64

Fig. 4.1 Energy band diagram (left) and charging character of interface states (right) for the metal-dielectric interface, where the Fermi level ($E_{F,m}$) is above the charge neutrality level in the dielectric ($E_{CNL,d}$). In general, the character of interface states becomes more acceptor- (donor-) like toward the conduction (valence) band, as indicated by the solid (dashed) line. 74

Fig. 4.2 Change of flat-band potential vs HfO_2 film thickness, showing tendency for potentials to converge around 0.3 eV below CB edge. 76

Fig. 4.3 V_{fb} versus EOT for HfAlO film under three metal nitrides. Initial charges in HfAlO films are the same for three different metal electrodes. 79

Fig. 4.4 $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ for various gate dielectrics. HfAlO and HfO_2 show higher $\Phi_{m,eff}$ values than SiO_2 does. 79

Fig. 4.5 V_{fb} versus EOT for (a) HfN, (b) TaN and (c) TaSiN on HfAlO after annealing at different temperatures. Both HfN and TaN show the change of dielectric charge whereas TaSiN on HfAlO shows the change of work function after high temperature anneal. 81

Fig. 4.6 The behavior of $\Phi_{m,eff}$ before and after high temperature RTA at several temperatures for the gate stacks of (a) HfN or TaN on high-K dielectric (b) TaSiN on high-K dielectric. 83

Fig. 4.7 $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ on HfAlO after annealing at different temperatures. The result indicates that MIGS theory with intrinsic interface states is not applicable after annealing. 84

Fig. 4.8 The behavior of $\Phi_{m,eff}$ before and after high temperature RTA at several temperatures for the gate stacks of metal nitride on pure silicon dioxide stacks. 84

Fig. 4.9 Observed phenomena in the modification of $\Phi_{m,eff}$ of gate stacks in three different combinations of metal nitride/gate dielectric stacks after high temperature annealing. It is observed that the modification of $\Phi_{m,eff}$ after annealing happens only when "silicon" is present at the metal/dielectric interface. 86

Fig. 4.10 Si 2p core-level spectra at two different take-off angles of (a) 15° and (b) 90°. Compared to HfAlO without SP, Si-passivated HfAlO 88

sample shows strong peak at around 102.3 eV, which indicates Hf silicate bond (Hf-O-Si).

Fig. 4.11 Thermal instability of $\Phi_{m,eff}$ of HfAlO sample with SP. $\Phi_{m,eff}$ value approaches around 4.8 eV as RTA temperature increases. 89

Fig. 4.12 Schematic drawing of charging characteristics of interface states at the metal-dielectric interface. The extrinsic interface states cause a shift of $E_{CNL,d}$ toward (a) E_C and (b) E_V to compensate the additional dipole charge (+q' and –q") generated by Si-M and M-Si bond, respectively. 90

Fig. 5.1 Barrier height between silicide and n-silicon plotted against calculated silicide workfunction assuming (metal) Si_4 stoichiometry. 100

Fig. 5.2 $\Phi_{m,eff}$ versus Φ_{MSix} of four metal silicides on SiO_2. The Φ_{MSix} value is calculated by taking the geometric mean of Φ_M and Φ_{Si} with various stoichiometries (X) between metal and silicon. 101

Fig. 5.3 The S parameter and the charge neutrality level $\Phi_{CNL,d}$ on SiO_2 as a function of X at MSix. 103

Fig. 5.4 $\Phi_{m,eff}$ versus Φ_{MSix} of MSi_2 on SiO_2 and HfAlON. The S value of HfAlON is nearly identical to the calculated S value of around 0.63 obtained from Eq. 5.3. 104

Fig. 5.5 Comparison of S value of various gate electrodes on high-K gate dielectrics. HfAlON with FUSI gate shows weak Fermi-level pinning, even though Si atoms are present at the interface of FUSI gate/HfAlON stack. 106

Fig. 6.1 V_{fb} of MOS capacitor versus EOT of gate dielectric for Ni-FUSI gate stacks with two different thickness ratios (R_{Ni}) on both SiO_2 and HfAlON dielectric. Significant shift in $q\Phi_{m,eff}$ is observed for Ni-FUSI gate with R_{Ni}=1.25 on HfAlON. 114

Fig. 6.2 $q\Phi_{m,eff}$ versus thickness ratio of Ni to polysilicon for Ni-FUSI gate on both SiO_2 and HfAlON. A strong Fermi-level pinning is observed in Ni-FUSI films on HfAlON when R_{Ni} is low. 115

Fig. 6.3 RBS spectrum of Ni-FUSI film with R_{Ni}=2.5. The composition ratio of Ni to Si is estimated to be 3, which means Ni_3Si phase. 116

Fig. 6.4 Composition ratio of Ni to Si as function of R_{Ni}. The composition ratio of Ni to Si is estimated by RBS analysis. 117

Fig. 6.5 The relative difference of $q\Phi_{m,eff}$ ($\Delta q\Phi_{m,eff}$), taking Ni_3Si phase Ni-FUSI sample as a reference, for Ni-FUSI gates with different composition ratios on three different types of gate dielectrics. Data for Ni-FUSI gate on HfSiON were taken from [6.9]. 118

Fig. 6.6 Schematic drawing of the interface configuration between high-K dielectric and Ni-FUSI gate with extrinsic interface states induced by Hf-Si bond. In case the extrinsic interface states are dominant, $E_{CNL,d}$ shifts near to the $E_{Hf\text{-}Si}$, resulting in the strong Fermi-level pinning near to E_C of silicon. 120

LIST OF TABLES

Table 1.1	Gate Dielectric Technology Requirements – selected data from latest ITRS-2004 update, where hp and EOT stand for the industry's most aggressive half-pitch target and equivalent physical oxide thickness, respectively.	4
Table 2.1	Comparison of relevant properties for high-K candidates including SiO_2 and Si_3N_4.	14
Table 2.2	Summary of some possible metal gate materials reported in the literature.	29
Table 3.1	Fabrication process for MOS capacitor and NMOS Transistor.	46
Table 4.1	Comparison of theoretical and experimental slope parameter *S* and $\Phi_{CNL,d}$ under three metal nitride gate electrodes.	80
Table 5.1	Comparison of $\Phi_{m,eff}$ and Φ_{MSi2} of each FUSI gate on SiO_2. The Φ_{MSi2} values are obtained from the equation of $\Phi_{MSix} = (\Phi_M \Phi_{Si}^{x})^{1/x+1}$ where x = 2.	103
Table 5.2	Comparison of S value and $\Phi_{CNL,d}$ of four kinds of gate stacks. The FUSI gate/HfAlON stack shows a slightly smaller S value compared to MN/HfAlO stack.	106

LIST OF SYMBOLS

Symbol	Description
C_{crit}	Critical composition ratio
CET_{inv}	Capacitor equivalent thickness in inversion
D_{it}	Interface-state density
E_c, CB	Silicon conduction band edge
$E_{CNL,d}$	Charge neutrality level in the dielectric
$E_{F,m}$	Fermi level of metal electrode
E_G	Silicon bandgap
$E_{Hf\text{-}Si}$	Energy level of Hf-Si bond at the interface
E_{vac}	Vacuum energy level
E_v, VB	Silicon valence band edge
G_m	Transconductance
hp	Industry's most aggressive half-pitch target
I_g	Gate leakage current
I.L.	Interfacial layer
I_d	Drain current
J_g	Gate leakage current density
K	Dielectric permittivity constant
L	Channel length
MSi_x	Metal silicide with arbitrary composition
n	Refractive index
N_{fix}	Density of fixed charge
q	Electronic charge of electron
Q	Charge density
+q'	Additional positive dipole charge
-q"	Additional negative dipole charge
R_{Ni}	Thickness ratio of Ni to polysilicon
S	Slope parameter
t_{eq}	Equivalent oxide thickness
T_{Ni}	Thickness of Ni film
T_{Si}	Thickness of polysilicon
TOA	Take-off angle
V_d	Drain voltage

V_{fb}	Flat-band voltage
V_g	Gate voltage
V_t, V_{th}	Threshold voltage
W	Channel width
W	Electric power
X	Stoichiometry between metal and silicon
χ_s	Electron affinity of the semiconductor
ΔE_C	Electron barrier to Si
ε_∞	Electronics part of the dielectric constant
Φ_{Bn}	Schottky barrier height for the electrons
$\Phi_{CNL,d}$	Charge neutrality level in the dielectric
Φ_M	Metal work function
$\Phi_{m,eff}$	Effective work function of metal electrode
Φ_{ms}	Work function difference between metal electrode and silicon substrate
Φ_{MSix}	Vacuum work function of metal silicide
$\Phi_{m,vac}$	Vacuum work function of metal electrode
Φ_{Si}	Silicon work function
$\mu_{Coulomb}$	Mobility limited by Coulomb scattering
μ_{eff}	Effective mobility
μ_{RCS}	RCS-limited mobility
μ_{univ}	Universal mobility

LIST OF ACRONYMS

ALD	Atomic Layer Deposition
CET	Capacitor equivalent thickness
CGS	Complete gate silicidation
CMOS	Complimentary metal oxide semiconductor
CNL	Charge neutrality level
C-V, CV	Capacitance versus Voltage
CVD	Chemical Vapor Deposition
DHF	Diluted HF
EELS	Electron energy loss spectroscopy
EOT	Equivalent oxide thickness
FDSOI	Fully-depleted silicon on insulator
FET	Field effect transistor
F-N	Fowler-Nordheim
FUSI	Fully silicided
ITRS	International Technology Roadmap of Semiconductors
JVD	Jet Vapor Deposition
LDS	Liquid Delivery System
LMFC	Liquid Mass Flow Controller
LPCVD	Low pressure chemical vapor deposition
MIGS	Metal induced gap states
MOCVD	Metal Organic Chemical Vapor Deposition
MOSFET	Metal-oxide-semiconductor field effect transistor
MPU	Microprocessor unit
nMOSFET	n-channel MOSFET
PDA	Post deposition anneal
PDE	Poly-depletion effect
PMA	Post metallization annealing
pMOSFET	p-channel MOSFET
PVD	Physical Vapor Deposition
QM	Quantum mechanical
RBS	Rutherford backscattering spectrometry

RCS	Remote coulomb scattering
RPS	Remote phonon scattering
RTA	Rapid thermal annealing
SIMS	Secondary ion mass spectroscopy
SN	Surface nitridation
SP	Silicon passivation
VGS	Virtual gap states
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XTEM	Cross-sectional transmission electron microscopy

CHAPTER 1

INTRODUCTION

1.1 MOSFET SCALING

1.1.1 OVERVIEW OF MOSFET SCALING

The pervasiveness of the silicon based microelectronics revolution has continued for the past 40 years, with IC density quadrupling every three-four years, in conjunction with improved transistor performance. This has been accomplished by reducing the dimensions of the key component of these circuits: the MOSFET (metal-oxide-semiconductor field effect transistor). Indeed, the reduction of device dimensions allows the integration of a higher number of transistors on a chip, enabling higher speed and reduced costs. The scaling behavior has followed the well known Moore's law, which predicts that the number of transistors per integrated circuit would double every ~ 18 months [1.1]. This law is illustrated in Fig. 1.1, where the number of devices integrated in the different generations of Intel's microprocessors is presented as a function of the production year of these circuits [1.2]. Over the past 30 years from 1971 to 2002, the minimum feature size in a typical MOS transistor has been reduced by a factor of around 70 – from 10 um to 0.13 um – and the number of integrated transistors and clock frequency have been increased by more than 20,000

times [1.3]. In the meantime, cost per function has decreased at an average rate of ~ 25-30% per year per function [1.4].

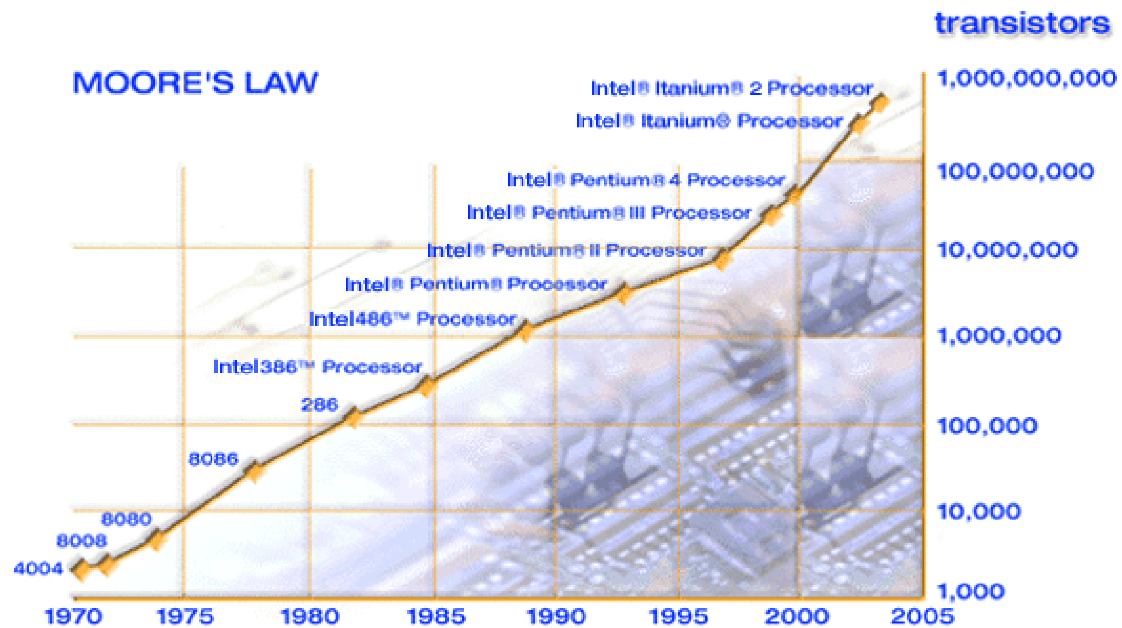


Fig. 1.1 Illustration of Moore's law: number of transistors integrated in the different generations of Intel's microprocessors versus the production year of these circuits [1.2].

The scaling methodology (i.e., scaling in design rules without compromising the current-voltage characteristics) was introduced by Dennard *et al*. in 1974 [1.5] and established the paradigm by which scaling has progressed. The original scaling methodology, based on constant electric field scaling principles, was generalized in 1984 to allow the voltage to be scaled less rapidly than the dimensions by increasing the electrical field with its own scaling factor [1.6]. The physical gate length, gate dielectric thickness and extension junction depth are the critical transistor scaling elements.

1.1.2 SCALING OF CURRENT GATE DIELECTRICS AND ITS LIMIT

One of the key elements that allowed the successful scaling of silicon based MOSFETs is certainly the excellent physical and electrical properties of the gate dielectric so far used in these devices: SiO_2. The thickness of SiO_2 has decreased from the range of 50-100 nm for the 4K NMOSFET DRAM to 1.2-1.5 nm equivalent oxide thickness (EOT) or less for leading edge microprocessor units (MPU) [1.7]. Silicon dioxide is also the smallest dimensional element in the MOSFET and yet has to withstand the highest electrical field. Additionally, SiO_2 exhibits low D_{it} ($\leq 5 \times 10^{10}$ states/cm^2-eV), low fixed charge density ($\leq 5 \times 10^{10}$ charges/cm^2), minimal low-frequency CV hysteresis and frequency dispersion ($\leq$ 10 mV), reasonably high mobility as well as exhibit sufficient reliability after years of high-field stressing (~10 years). In addition, SiO_2 is thermally, chemically and mechanically compatible with the other materials and the manufacturing processes used in IC fabrication. These attributes of SiO_2 have helped the continued use of SiO_2 for the past several decades in complimentary metal-oxide-semiconductor (CMOS) technology. As each generation was scaled, this gate oxide also had to be made progressively thinner. According to the latest International Technology Roadmap of Semiconductors: *ITRS-2004 update* [1.8] as shown in Table 1.1, for the most advanced CMOS technologies being fabricated in 2010 with 45 nm technology node, the gate oxides will have to have thicknesses of 0.7 nm for high-performance application and 0.9 nm for low operating power device.

With the rapid downscaling of SiO_2 gate insulators, several limits will become inevitable, such as gate leakage current issue by direct tunneling [1.9] and poly-depletion-effect issue [1.10] when polysilicon electrode is used as a gate electrode. The direct tunneling associated with ultrathin SiO_2 will be described in the next section and the poly-depletion-effect concerns will be covered in Chapter 2.

Table 1.1 Gate Dielectric Technology Requirements – selected data from latest ITRS- 2004 update [1.8], where *hp* and EOT stand for the industry's most aggressive half-pitch target and equivalent physical oxide thickness, respectively.

Year of Production	***2004***	***2007***	***2010***	***2013***	***2016***
Technology node	*hp90*	*hp65*	*hp45*	*hp32*	*hp22*
Physical gate length for MPU (nm)	37	25	18	13	9
Physical gate length for low-operating-power (nm)	53	32	22	16	11
Physical gate length for low-standby-power (nm)	65	37	25	18	13
EOT for high-performance (nm)	1.2	0.9	0.7	0.6	0.5
EOT for low-operating-power (nm)	1.5	1.2	0.9	0.8	0.7
EOT for low-standby-power (nm)	2.1	1.6	1.3	1.1	1.0
Gate leakage at 100°C for high-performance (nA/μm)	170	230	330	1000	1670
Gate leakage at 100°C for low-operating-power (nA/μm)	1	1.67	2.33	3.33	10
Gate leakage at 100°C for low-standby-power (pA/μm)	3	8	20	27	33

1.1.2.1 Gate Leakage by Direct Tunneling

As gate oxide aggressively scaled below 35 Å, the gate oxide leakage current will be dominated by the direct tunneling of charge carriers through a trapezoidal energy barrier of gate oxide rather than by Fowler-Nordheim (F-N) tunneling through a triangular energy barrier, resulting in gate leakage which is significantly higher at low field and relatively insensitive to field effect. Figure 1.2 shows the dramatic increase in the leakage current at low field due to the direct tunneling when gate oxide

is reduced below 35 Å [1.9]. In the direct tunneling thickness regime, a slight decrease in gate oxide thickness results in order of magnitude increase in the leakage current.

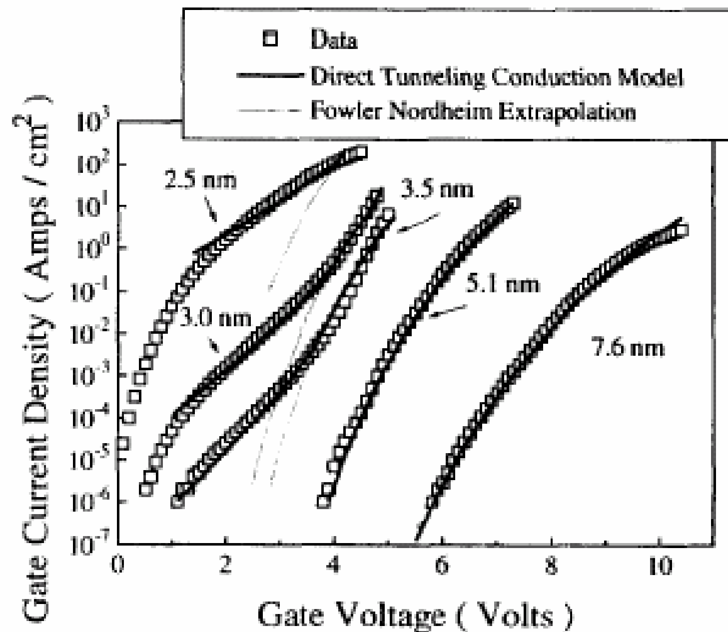


Fig. 1.2 The low voltage oxide conduction follows the theory of Direct-Tunneling where subtle change in barrier change from triangular to trapezoidal explains the leakage current significantly larger than those predicted by the Fowler-Nordheim theory [1.9].

1.1.2.2 Impact on Device Operation

The rapid increase in leakage current with the decrease of the gate dielectric thickness will pose serious concerns to the operation of CMOS devices. One concern is that the direct tunneling current of ultrathin gate oxide becomes large enough that it removes carriers faster than they can be supplied from source/drain of the device. In such cases an inversion layer is kept from forming in an MOS capacitor, resulting in no further gains in transistor drive current when scaling the SiO_2 thickness thinner than

about 10-12 Å [1.11]. Therefore, the SiO_2 thickness of 10 Å or less could serve as a practical limit for the scaling of high-performance MOSFET device.

The other concern is the substantially high standby power dissipation due to high gate leakage in low standby power MOSFET device. The gate leakage current density and standby power consumption are plotted as a function of gate voltage in Fig. 1.3. The curve for 15 Å oxide is based on measured values, but the curve for a high-k film is meant to show the potential reduction in leakage current for a high-k dielectric with the same equivalent oxide thickness (EOT or t_{eq}) value. It is clear that a gate dielectric with a permittivity higher than of SiO_2 is required to meet low-power application requirement [1.12].

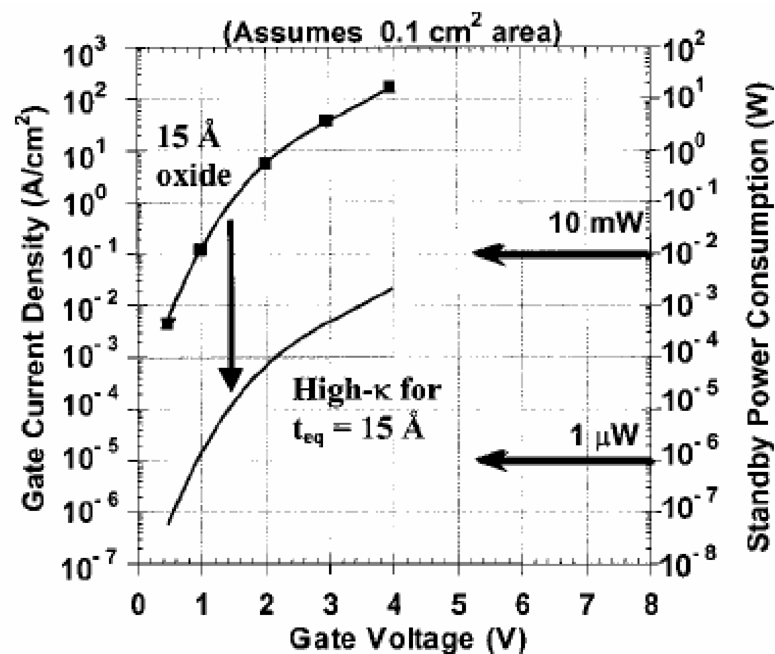


Fig. 1.3 Power consumption and gate leakage current density for a chip that has a 15 Å thick SiO_2 gate dielectric compared to the potential reduction in leakage current by an alternate dielectric exhibiting the same equivalent oxide thickness. Assumes at total gate area of 0.1 cm^2 [1.12].

1.2 MOTIVATION AND PURPOSE OF THESIS

As discussed in the previous section, device performance degradation and/or increased power consumption due to gate leakage current would be the major limitation factors for further device scaling. To overcome these limitations, replacement of SiO_2 with a high-K gate dielectric has been suggested because they can provide physically thicker films at the same EOT, which eventually reduces the tunneling current due to the increased physical thickness [1.12]. Among the various candidates of high-k dielectrics, the HfO_2 has been extensively studied due to both its thermodynamical stability with silicon substrate and relatively good compatibility with polysilicon gate electrode compared to other high-K dielectrics [1.12]-[1.14].

However, the successful implementation of HfO_2 into the advanced CMOS device still remains a challenge. Current issues of HfO_2 will be briefly discussed in Chapter 2. One of the issues with HfO_2 is the poor thermal stability of the film and the interfacial layer growth during subsequent thermal processes. To improve the thermal stability of HfO_2 film and to retard the oxygen diffusion through high-k film, incorporation of Al into HfO_2 film has been attempted [1.15],[1.16]. In addition, the acceptably high dielectric constant value and the band offset values of HfAlO alloy make the film one of the most promising candidates for high-K gate dielectric application [1.15]-[1.18]. However, the valuable work has scarcely been reported using MOCVD (Metal-Organic Chemical Vapor Deposition) system that is considered as one of strong candidates for high-k deposition system. The reason is probably because the process using two precursors in MOCVD is much more complicated and difficult than that in Jet Vapor Deposition (JVD) [1.15], Atomic Layer Deposition (ALD) [1.16],[1.17], or Physical Vapor Deposition (PVD) [1.18]. This thesis attempts to demonstrate the successful deposition of a high quality HfAlO film with a wide range

of composition ratio controllability between HfO_2 and Al_2O_3 in HfAlO using a single cocktail liquid source in a MOCVD system, which is a suitable technique for mass production in terms of process simplicity and reproducibility. The effect of the composition ratio on the electrical properties of HfAlO is studied, too.

The other issue is the poor V_t controllability of MOSFETs due to the interactions between high-K dielectric and gate electrode. It has been reported that polysilicon/high-K gate dielectric devices show the significant V_t shift compared to that of polysilicon/SiO_2 control devices, which is mainly attributed to the interaction between polysilicon/high-K gate dielectric [1.19],[1.20]. A study on the interaction between high-K dielectric and metal gate, including fully silicided (FUSI) gate [1.21], is also focused in this thesis because of the increasing demand of metal gate electrode on high-K dielectric. The possible interaction between metal gate and high-K gate dielectric during their fabrications and/or following thermal processing has been investigated and its effect on the effective work function in metal gate/high-K dielectric stack has also been studied.

1.3 THESIS OUTLINE AND ORIGINAL RESEARCH CONTRIBUTIONS

This thesis is organized as follows; Chapter 1 describes the MOSFET scaling and the accompanying issues. A review on literature and recent gate technology trends and issues are presented in Chapter 2.

In Chapter 3, a high quality MOCVD HfAlO dielectric film with a wide range of composition controllability between HfO_2 and Al_2O_3 in HfAlO using a single cocktail liquid source $HfAl(MMP)_2(OiPr)_5$ as the new high-K fabrication method is

demonstrated and the effect of the composition ratio on the electrical properties of HfAlO is also presented.

The investigation on the thermal instability of effective work function ($\Phi_{m,eff}$) and its material dependence on metal gate/high-K dielectric stack is presented in Chapter 4. Thermal instability of $\Phi_{m,eff}$ after high temperature RTA is investigated. It is found that this phenomenon is attributed to the generation of substantial amount of extrinsic interface states at the metal/dielectric interface. The role of Si atoms at the interface is identified.

In Chapter 5, a new approach to analyze and predict the behavior of $\Phi_{m,eff}$ in FUSI gate/high-K dielectric stack and its interface configuration is proposed using the combination of semi-empirical approach and MIGS theory. It is found that FUSI gate has effectively MSi_2 configuration at the interface between gate dielectric and FUSI gate. In addition, the strength of Fermi-level pinning of FUSI gate on high-K dielectric is compared to that of polysilicon gate on high-K dielectric.

New findings on the Fermi-level pinning phenomenon in FUSI gate/high-K dielectric stack, focusing on process condition and material composition dependence of Fermi-level pinning, are presented in Chapter 6. It has been found that there is a critical composition ratio (C_{crit}) of Ni to Si in Ni-FUSI gate which starts to show a strong Fermi-level pinning. The C_{crit} is also found to be dependent on the underlying gate dielectric material.

Finally, the thesis is completed with summary and conclusions in Chapter 7.

References

[1.1] G. E. Moore, "Progress in digital integrated circuits," in *IEDM Tech. Dig*., pp. 11-13, 1975.

[1.2] "*Moore's Law*", http://www.intel.com/research/silicon/mooreslaw.htm.

[1.3] M. Houssa, *High-K Gate Dielectric*, Bristol and Philadelphia: Institute of Physics Publishing, 2004.

[1.4] Semiconductor Industry Association (SIA), "*International Technology Roadmap for Semiconductors, 2001 Edition*", http://public.itrs.net/Files/2001ITRS/Home.htm.

[1.5] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFETs with very small physics dimensions", *IEEE J. Solid.-State Circuits*, vol 9, pp. 256-268, 1974.

[1.6] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to 1/4 micron MOSFET design", *IEEE Trans. Electron Devices*, vol 31, pp. 452-462, 1984.

[1.7] H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G.A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner and R. W. Murto, "Integration of high-k gate stacks into planar scaled CMOS integrated circuits" in *Nano and Giga Challenges in Microelectronics (2002)*, 2002.

[1.8] Semiconductor Industry Association (SIA), "*International Technology Roadmap for Semiconductors*, *2004 Update*", http://www.itrs.net/Common/2004Update/2004Update.htm.

[1.9] K. F. Schuegraf, D. Park, and C. Hu, "Reliability of thin SiO_2 at direct tunneling voltages," in *IEDM Tech. Dig*., pp. 609-612, 1994.

[1.10] S.-H. Lo, D. A. Buchanan, Y. Taur, L.-K. Han, and E. Wu, "Modeling and Characterization of n+-and p+-polysilicon-gated ultra thin oxides (21-26 Å)" in *Symp. on VLSI Tech*., pp. 149-150, 1997.

[1.11] G. Timp, A. Agarwal, F. H. Baumamn, T. Boone, M. Buonanno, R, Cirelli, V. Donnelly, M, Foad, D, Grant, M. Green. H. Gossmann, S. Hillenius, J, Jackson, D. Jacobson, R. Kleiman, A, Kornblit, F. Klemens, J. T-C Lee, W. Mansfield, S. Moccio, A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. W. Tai, D. Tennant, H. Vuong, and B. Weir, "Low leakage, ultra-thin gate oxides for extremely high performance sub-100nm nMOSFETs," in *IEDM Tech. Dig*., pp. 930-932, 1997.

[1.12] G. D. Wilk, R. M. Wallace, J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations", *J. Appl. Phys.*, vol 89, pp. 5243-5275, May 2001.

[1.13] P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, and J. G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)", *J. Appl. Phys.*, vol 91, pp. 4353-4363, April 2002.

[1.14] Y. Kim, *et al*., "Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-K gate dielectrics with polysilicon gate electrode", in *IEDM Tech. Dig*., 20-02, 2001.

[1.15] W. Zhu, T. P. Ma, T. Tamagawa, and Y. Di, "HfO_2 and HfAlO for CMOS: Thermal stability and current transport," in *IEDM Tech. Dig*., pp. 463-466, 2001.

[1.16] H. Y. Yu, N. Wu, M. F. Li, C. X. Zhu, B. J. Cho, D. L. Kwong, C. H. Tung, J. S. Pan, J. W. Chai, W. D. Wang, D. Z. Chi, C. H. Ang, J. Z. Zheng, "Thermal Stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si," *Applied Physics Letters*, vol 81, pp. 3618-3620, 2002.

[1.17] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D. L. Kwong, J. S. Oan, C. H. Ang, J.Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Applied Physics Lett.,* vol 81, pp. 376-378, 2002.

[1.18] L. Manchanda, M. D. Morris, M. L. Green, R. B. van Dover, F. Klemens, T. W. Sorsch, P. J. Silverman, G. Wilk, B. Busch, S. Aravamudhan, "Multi-component high-*K* gate dielectrics for the silicon industry," *Microelectronic Engineering*, vol 59, pp. 351-359, 2001.

[1.19] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi Level Pinning at the PolySi/Metal Oxide Interface," in *Symp. VLSI Tech. Dig.,* 2003, pp. 9-10.

[1.20] K. Xiong, P. W. Peacock, and J. Robertson, "Fermi-level pinning and Hf-Si bonds at HfO_2: Polycrystalline silicon gate electrode interfaces," *Appl. Phys. Lett.*, vol. 86, 012904, 2005.

[1.21] B. Tavel, T. Skotnicki, G. Pares, N. Carrière, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally silicided ($CoSi_2$) polysilicon: a novel approach to very low-resistive gate (~2Ω/□) without metal CMP nor etching," in *IEDM Tech. Dig.,* pp. 825-828, 2001.

CHAPTER 2

LITERATURE AND TECHNOLOGY REVIEW

2.1 HIGH-K DIELECTRIC AS ALTERNATIVE TO SiO_2

2.1.1 OVERVIEW OF HIGH-K DIELECTRIC

As an alternative to SiO_2 or SiO_xN_y, much research has been done on high-K metal oxides as a means to provide a substantially thicker (in physical thickness) dielectric for reduced leakage current while improving the gate capacitance. A list of possible candidate materials is given in Table 2.1 [2.1]-[2.4], together with their relative dielectric constants, bandgap energy (E_G), and electron barrier to Si (ΔE_C).

Among these candidates, some materials such as Ta_2O_5 [2.5],[2.6], TiO_2 [2.2], $SrTiO_3$ [2.7], and Al_2O_3 [2.8],[2.9] were initially chosen as potential alternative gate dielectric candidates, inspired by memory capacitor applications and the resultant semiconductor manufacturing tool development infrastructure [2.1]. With the exception of aluminum oxide (Al_2O_3), however, these materials are not thermodynamically stable in direct contact with Si. In particular, interfacial reaction has been observed for the cases of Ta_2O_5 and TiO_2 on Si. For this reason, these metal oxides need an additional barrier layer that may add process complexity and impose thickness scaling limit. On the other hand, Al_2O_3 appears to be one of the popular candidates due to its favorable properties such as high bandgap, good thermal stability

on Si substrate and remains amorphous under high annealing temperature. Nevertheless, its large threshold voltage and moderately low permittivity of 9-11 make it a relatively short-term solution [2.1].

It is desirable to use a metal oxide, with reasonably high permittivity, which is stable on Si and exhibits an interface quality comparable to that of SiO_2. This would avoid the need for a thick interfacial layer and at the same time, the high permittivity value could be fully utilized.

Table 2.1 Comparison of relevant properties for high-K candidates including SiO_2 and Si_3N_4 [2.1]-[2.4].

Materials	Dielectric Constant (K)	Band Gap E_G (eV)	ΔE_C (eV) to Si
SiO_2	3.9	8.9	3.15
Si_3N_4	7.8	5.1	2.1
Al_2O_3	9	8.7	2.8
Ta_2O_5	26	4.5	1 - 1.5
TiO_2	80	3.0-3.5	1.2
$SrTiO_3$	200	-	-
$Zr_xSi_{1-x}O_y$	3.9 – 25, 12[a]	~6	~1.5
ZrO_2	25	5.5 - 5.8	1.4
$Hf_xSi_{1-x}O_y$	3.9 – 26, 11[a]	~6	~1.5
HfO_2	25	5.7	1.5

[a] Typical values for Hf and Zr silicates corresponding to x = 0.35

2.1.2 FIGURES OF Hf-BASED HIGH-K DIELECTRIC

Zirconium oxide (ZrO_2), hafnium oxide (HfO_2) and their silicates have received considerable attention since they are predicted to be thermodynamically stable in contact with Si and have reasonable high-K value (~25) [2.10]-[2.17]. Among them, HfO_2 has more desirable properties than ZrO_2. Since the Gibbs energy of formation for HfO_2 is more negative than ZrO_2 (-1088 kJ/mol vs -1040 kJ/mol) [2.11], HfO_2 could be more stable when in contact with Si. Additionally, HfO_2 has been shown to be compatible with a polysilicon gate whereas ZrO_2 has been reported to show gross incompatibilities. Polysilicon deposition at higher temperatures (620ºC) results in the reduction of ZrO_2 to form a Zr-silicide or SiO_2 layer at poly-Si/ZrO_2 interface, leading to very high leakage current [2.12],[2.13]. Figure 2.1 shows the X-ray Photoelectron Spectroscopy (XPS) spectra of ZrO_2 and poly-Si interface. It has been observed that ZrO_2 decomposition into Zr metal compounds occurs when a polysilicon on ZrO_2 sample is annealed in UHV N_2 at 950℃. These reactions would significantly increase leakage current of MOS capacitor. On the contrary, CVD HfO_2 films remain stable after poly-Si deposition and annealing in UHV N_2 ambient up to 950℃ and show no evidence of the formation of undesirable Hf metal or Hf-silicide phases as shown in Fig. 2.2 [2.14]. Due to these properties, thin HfO_2 film or Hf-based high-K dielectric has been extensively studied in recent years as a strong candidate for the next generation gate dielectric material.

Although the reduction of leakage current by orders of magnitude and the good transistor performance of CMOSFET have been demonstrated by HfO_2 [2.15], successful integration of HfO_2 into the conventional CMOS process remains a challenge. In the next section, we will study in detail the issues related to Hf-based dielectric and their effects on device performance.

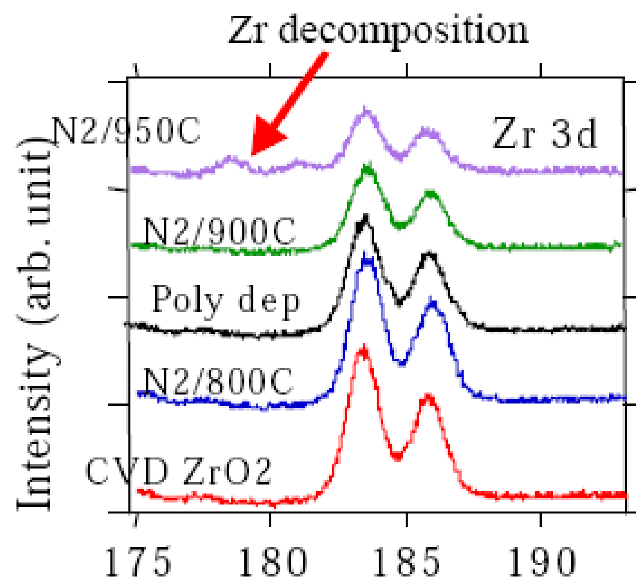


Fig. 2.1 XPS spectra of ZrO_2 and polysilicon interface. ZrO_2 is decomposited after 950℃ annealing [2.12].

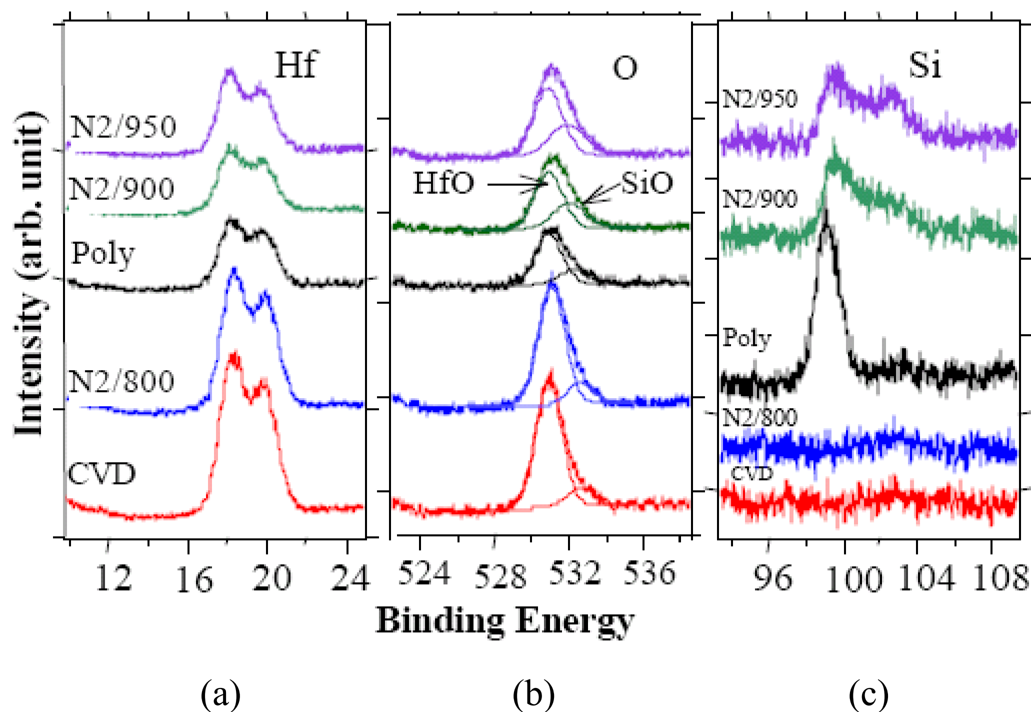


Fig. 2.2 XPS analysis of (a) Hf 4f, (b) O 1s, and (c) Si 2p of HfO_2 gate stack deposited on clean Si(100) at 450°C for 2 min followed by N_2 annealing at 800°C for 1min, poly-Si deposition at 600°C and N_2 annealing at 900°C and 950°C for 30sec [2.14].

2.2 ISSUES WITH HF-BASED HIGH-K DIELECTRIC

2.2.1 THERMAL STABILITY

Most of the advanced gate dielectrics except Al_2O_3 studied to date are either polycrystalline or single crystal films. HfO_2, like most of other metal oxide films, tends to be crystallized either during deposition or following thermal processing. The film is easily crystallized at a temperature as low as 400ºC [2.18] and the crystallization temperature of the film depends on the deposition condition and/or film thickness.

Polycrystalline gate dielectric may be problematic because grain boundaries could induce the defects and serve the diffusion path of impurities such as oxidant [2.19]. In addition, it could also induce the interfacial roughness arising from potential faceted interfaces. The defects throughout the high-K films and interfacial roughness can cause the increase of gate leakage. In addition, grain size and orientation changes throughout a polycrystalline film can cause significant variations in K and V_t, leading to irreproducible properties [2.1]. Yamaguchi *et al.* in his recent report indicates that crystallize HfO_2 portion in the Hf-silicates degrades the electron mobility due to additional Coulomb scattering other than the substrate impurity scattering [2.20]. Furthermore, Liu *et al.*'s modeling results clearly indicate that boron can diffuse through a thin HfO_2 polycrystalline film via grain boundary diffusion, but not by bulk diffusion [2.21]. This finding emphasizes the further need for amorphous film to reduce impurity diffusion.

Nevertheless, there are indeed some encouraging electrical properties reported even though the high-K film has already crystallized. Kim *et al.* have claimed that crystallization of HfO_2 shows almost no effect on the gate leakage current and the additional trap states introduced by formation of grain boundaries have negligible

contribution to conduction [2.22]. Perkin *et al.* show that the leakage current for crystallized ZrO_2 is comparable or lower than those reported for amorphous high-K dielectric for comparable equivalent oxide thickness (EOT) [2.23]. However, it should be noted that for both studies the interfacial SiO_2 layer with the Si substrate is at least 15Å which in turn will limit the down scaling of EOT. Therefore, the effect of crystallization of high-k film on the leakage current is still a controversial issue.

Recently, several research groups [2.18],[2.24],[2.25] have reported that incorporation of Al, Si or nitrogen into HfO_2 film helps to improve the thermal stability of HfO_2 film. The thermal stability properties and their effects on the electrical properties of $HfAl_xO_y$ alloy films (hereafter HfAlO) with various composition ratios prepared by Atomic Layer Deposition (ALD) have been reported by Yu *et al.* [2.26] and Joo *et al.* [2.27]. The HfAlO with 67% composition of HfO_2, $(HfO_2)_{0.67}(Al_2O_3)_{0.33}$, shows a good thermal stability comparable to Al_2O_3 film and a significant reduction in leakage current of 67%-HfO_2 film compared to that of pure HfO_2 film, which is attributed to the improved thermal stability.

Choi *et al.* have reported that the as-grown HfO_2 is crystallized while HfO_xN_y remained amorphous even after 900°C annealing [2.19]. The change of EOT and leakage current as a function of different annealing temperature also indicates that HfO_xN_y shows less increase in EOT and leakage current than HfO_2. This is attributed to the fact that N incorporation allows the film to remain amorphous after high temperature annealing, and therefore reduces the oxygen diffusion through the film as well as the leakage current.

2.2.2 Interfacial Layer Growth and Its Quality

Most of the high-k gate dielectrics have unstable interfaces with Si substrate, leading to undesirable interfacial layer formation. The formation of interfacial oxides, silicates, and silicides has often been observed during the film deposition or the subsequent rapid thermal annealing [2.1],[2.10],[2.11]. These kinds of interfacial layer reduce the overall permittivity of the final gate stack, resulting in increase of EOT. Therefore, the thermodynamic stability of high-K metal oxide in contact with silicon is a critical issue for the application of alternative gate dielectrics in silicon-based devices. Harada *et al.* have investigated the interfacial layer growth between HfO_2 and Si substrate during post deposition anneal (PDA) at 800℃ for 30sec using Secondary Ion Mass Spectroscopy (SIMS), cross-sectional TEM (XTEM), and electrical analysis [2.28]. They have found that there are two interfaces in the transition layer as shown in Fig. 2.3. One is the stoichiometric interface due to a Si out-diffusion from substrate during PDA, which is located at about 12 Å from Si substrate. The other is the K-transition interface defined by dielectric constant transition which is formed by a diffusion mechanism of Si into HfO_2. The K-transition interface is located at approximately 20 Å from Si substrate.

Thus, many research groups tend to employ NH_3 surface nitridation prior to deposition to serve as a barrier against interfacial layer growth and to reduce the extent of Si out-diffusion from the substrate. Interfacial nitride acts as a barrier to silicon, metal and boron diffusion as well as silicate formation. Kirsch *et al*. have reported that, with the nitrided interface, leakage current decreases by two orders of magnitude and capacitance increases by 15% [2.11]. Quantification of the XPS results shows that less interfacial silicate forms with SiN_x. N−(Si≡)$_3$ bonding at the Si/dielectric interface may reduce the amount of available to form $HfSi_xO_y$. However, Cho *et al*. have reported that the interfacial nitride induces the large hysteresis and interface trap

density [2.29]. The poor interface affects the device performance in which the mobility of the carriers in the Si channel is degraded. Therefore, careful interface engineering is necessary to optimize the process so that EOT may maintain even after high thermal process while device performance may not be degraded.

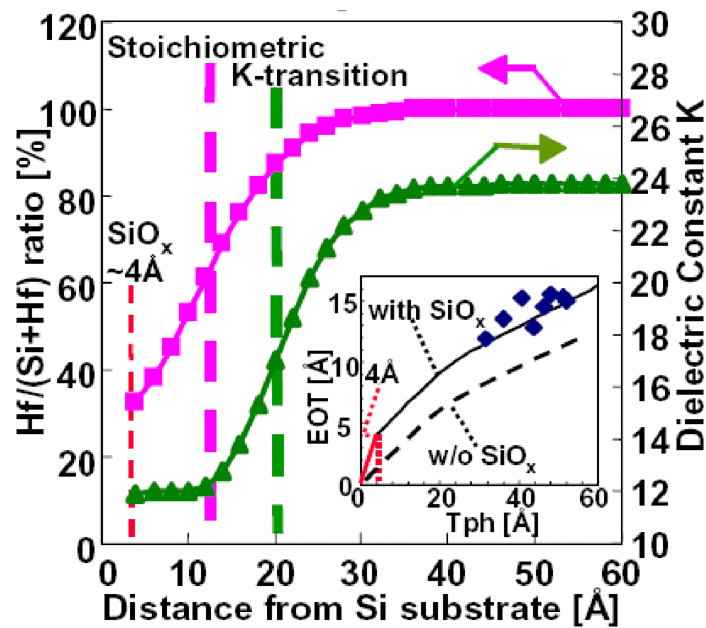


Fig. 2.3 Hf ratio and k as a function of distance from Si substrate. Due to fitting (inset) with experimental EOT (diamonds) and estimated EOT (solid curve), SiO_2 of 4 Å thickness seems to exist [2.28].

On the other hand, Yu *et al*. have demonstrated the successful scaling down to less than 10 Å of EOT in HfN/HfO_2 gate stack even after 1000℃ RTA without using surface nitridation prior to HfO_2 deposition [2.30]. They claim that the good EOT stability up to 1000℃ is attributed to the excellent oxygen barrier of HfN materials as well as thermal stability of HfN/HfO_2 interface. They have observed negligible change in the physical thickness of interfacial layer after 1000℃ RTA. Therefore,

implementation of oxygen diffusion barrier layer on top of high-K dielectric is also important to minimize interfacial layer growth.

2.2.3 CHANNEL MOBILITY RELATED ISSUES

Mobility is a critical parameter to evaluate a high-K dielectric as an alternative to SiO_2 and it is desired to maintain the mobility of MOSFET with high-K dielectric close to that of MOSFET with SiO_2 to ensure the comparable device performance. Recently, however, many research groups have reported that drain current of MOSFET with high-K gate dielectric is lower than that of SiO_2 gate insulator MOSFET mainly due to channel mobility degradation [2.20],[2.31]-[2.34]. The effective mobility (μ_{eff}) of high-K MOSFETs is limited to much smaller than the universal one. The degradation mechanism of effective mobility has been worked by several research groups.

Morioka *et al*. [2.31] and S. Saito *et al*.[2.32] claim that the main reason of mobility degradation is remote coulomb scattering (RCS). They suggest that electron trap centers at the HfSiO/SiO_2 interface and the fixed charges located at the Al_2O_3/SiO_2 interface are probably responsible for the mobility reduction, respectively. The schematic model of electron trap centers in HfSiO/SiO_2 stack is shown in Fig. 2.4. The RCS-limited mobility (μ_{RCS}) is calculated on the assumption that a fixed charge with a density of N_{fix} is located at the high-K/SiO_2 interface. Here, μ_{RCS} is inversely proportional to N_{fix}. In general, the universal mobility (μ_{uinv}) is determined by the scattering from phonons and surface roughness [2.33]. Thus, they add the contributions of μ_{RCS} and conventional Coulomb scattering ($\mu_{Coulomb}$) from interface traps and substrate impurities to the universal mobility according to Matthiessen's rule as shown in Eq. 2.1.

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{univ}} + \frac{1}{\mu_{Coulomb}} + \frac{1}{\mu_{RCS}} \quad \text{-------- (2.1)}$$

They have found that the RCS suppresses the effective mobility in particular at the region of low effective field and the effective mobility of MOSFET with HfSiO could be improved up to 95% of the universal mobility by reducing the RCS effect.

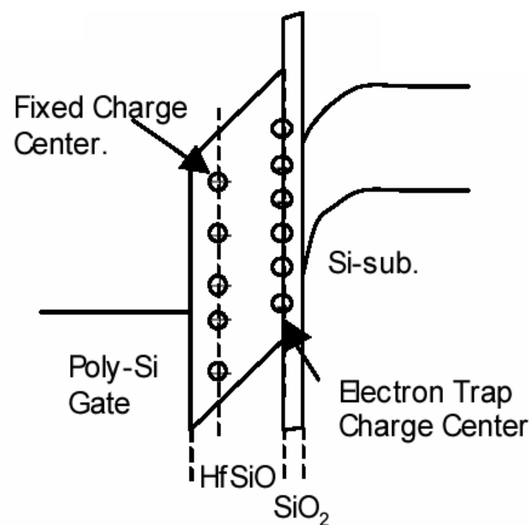


Fig. 2.4 Schematic model of fixed charge centers and electron trap charge centers in $HfSiO/SiO_2$ dielectric stack. The electron trap charge centers that are located at the $HfSiO/SiO_2$ interface are probably responsible for the mobility reduction [2.31].

On the other hand, Han *et al.* [2.34] have proposed that a large amount of interface states in MOSFETs with HfO_2 gate dielectric degrades the channel mobility and the asymmetric energy distribution of interface traps in n- and p-MOSFETs with HfO_2 gate dielectric causes more degradation in n-channel mobility than in p-channel mobility compared to those of conventional MOSFET with SiO_2 or SiON as gate dielectric. It has been found that the density of interface traps in the lower half of bandgap is small whereas that in the upper half of bandgap is high. They claim that

this gross asymmetry of the D_{it} distribution in high-K gated MOSFETs is partially responsible for the frequent observation that the channel mobility in nMOSFETs tends to degrade more severely than in pMOSFETs with high-K gate dielectrics, because the electrons in the n-channel interact with interface traps in the upper half of the bandgap, while holes in the p-channel interact with interface traps in the lower half of the bandgap.

Fischetti *et al*. [2.35] attribute the effective electron mobility degradation to remote phonon scattering (RPS). The high dielectric constant of high-K dielectrics is due to their large ionic polarizability, which is usually accompanied by the presence of soft optical phonons. Associated with "soft" are low-energy lattice oscillations (phonons). They claim that the coupling of low-energy surface optical phonon modes arising from the polarization of the high-K dielectric, while small in the case of SiO_2, to the inversion channel charge carriers causes a reduction of the effective electron mobility.

Although the origin of channel mobility degradation by high-K dielectric is still controversial, it is clear that a viable high-K gate dielectric on Si must at least have a low density of interface traps and oxide charges either in high-K dielectric or at its interface with the interfacial layer in order to realize an acceptable transconductance for advanced CMOS technology. Recently, encouraging results have been reported that the metal gate electrode is effective in screening the high-K's surface optical phonon from coupling to the channel under inversion conditions, resulting in improved channel electron mobility [2.36].

2.2.4 THRESHOLD VOLTAGE RELATED ISSUES

Another critical parameter to realize the high-K dielectric as an alternative to SiO_2 is the precise control of the threshold voltage (V_t) of MOSFETs. Many research groups have reported the significant V_t shift in poly-Si/high-K dielectric devices compared to poly-Si/SiO_2 control devices [2.31],[2.37],[2.38]. Hobbs *et al*. [2.37] have reported that Fermi-level pinning is a fundamental characteristic of the poly-Si/Metal oxide interface that causes high V_t in MOSFET devices. For Hf-based materials, the interfacial Si-Hf bonds create dipoles, resulting in pinning the Fermi level just below the poly-Si conduction band edge. For Al_2O_3 gate dielectrics, the Si-O-Al bonds pin the Fermi-level just above the Si valence band edge. This Fermi-level pining may induce the positive and negative flat-band voltage (V_{fb}) shift for the gate stack of n+Poly-Si and p+Poly-Si with HfO_2 on SiO_2, respectively, causing high V_t for MOSFET. Fig. 2.5 shows that the V_{fb}'s for n+polysilicon and p+polysilicon converge as the number of ALD cycles is increased. The initial region represents the change in V_{fb} for increasing surface coverage of the submonolayer HfO_2. Once complete surface coverage has occurred, ΔV_{fb} becomes constant. The ΔV_{fb} saturation value seems to depend on the bond number ratio of Si-Hf to Si-O-Hf. The high V_t of MOSFET, especially pMOSFET, due to Fermi-level pinning would be a major drawback for using polysilicon on high-K dielectric.

On the other hand, it has been reported that work function of metal gate/high-K dielectric device is also changed after high temperature anneal, which may cause the thermal instability of V_t of MOSFET. Schaeffer *et al.* have reported that the work functions of metal gates such as TaSi and TaSiN on HfO_2 shift with post-gate anneal [2.39]. A larger work function shift is observed when the thermal budget is increased. It has been postulated that the reaction at the metal-dielectric interface could have caused the aforementioned variations. Interfacial reaction, interdiffusion, or formation

of extrinsic states can manifest as thermal instability of work function or the threshold voltage of transistor.

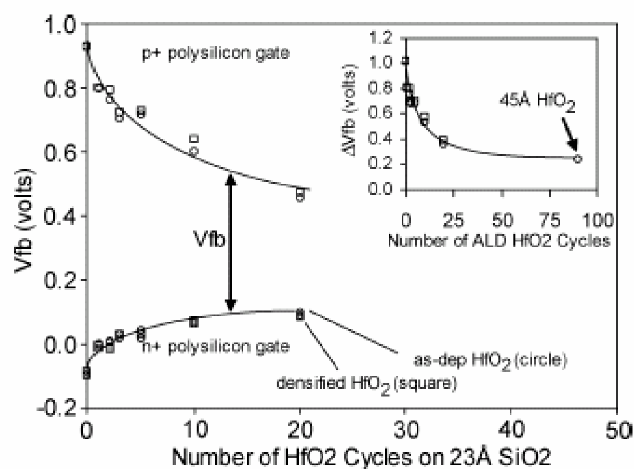


Fig. 2.5 Flat-band voltage versus number of HfO_2 ALD cycle. The V_{fb}'s for n+ and p+ gates converge as the number of ALD cycles is increased. (Inset: ΔV_{fb} versus number of HfO_2 ALD cycles) [2.37].

2.3 METAL GATE ELECTRODE AS AN ALTERNATIVE TO POLYSILICON GATE

2.3.1 LIMITATIONS OF POLYSILICON GATE

In a standard CMOS device, heavily doped polysilicon is used as the gate electrode. The use of polysilicon clearly has a lot of advantages in the CMOS application. However, the severe disadvantage of a polysilicon gate appears with thinner dielectrics and might limit the further scaling of the CMOS device. The first limitation is so-called the poly-depletion effect (PDE). Though heavily doped, the

polysilicon still lacks sufficient charge carriers and shows depletion at the dielectric interface when the transistor channel is in inversion. A high inversion capacitance or lower CET_{inv} (capacitor equivalent thickness in inversion) is required for high-current transistor operation where inversion charge in the channel is the key parameter. The depletion in the polysilicon gate limits the capacitance in inversion. The contribution of the polysilicon depletion in the inversion capacitance reduction depends both on the doping concentration of polysilicon and on thickness of gate dielectric [2.40]. To achieve the target CET_{inv} as required by the latest International Technology Roadmap of Semiconductors [2.41], the dielectric with a polysilicon gate should be additionally scaled down to compensate the EOT increment caused by polysilicon depletion compared to that with a depletion-free gate electrode such as metal gate. Figure 2.6 shows the required EOT to achieve the target CET_{inv} for each gate electrode with different poly doping concentration versus technology node [2.41]. For example, at polysilicon doping of 1×10^{20} and 2×10^{20} cm^3 for *hp*45 technology node, the dielectric thickness should be scaled down by 0.7 nm and 0.4 nm, respectively, due to PDE. To minimize the PDE, the doping range of polysilicon should be much higher than 3×10^{20} cm^3. However, these high doping level values might be hard to achieve. Hence, one solution would be to replace the polysilicon gate with PDE-free materials such as metal gate, including fully silicided gate, which will be discussed in Sections 2.3.2 and 2.3.3.

In addition, the dopant penetration such as boron from p+poly gate electrode through gate dielectrics leads to the uncontrolled V_t shift of the transistor [2.42]. This issue might be more significant for the device with high-K dielectric compared to that with SiO_2, as most of the high-K materials become crystalline during PDA or the source/drain annealing process [2.43].

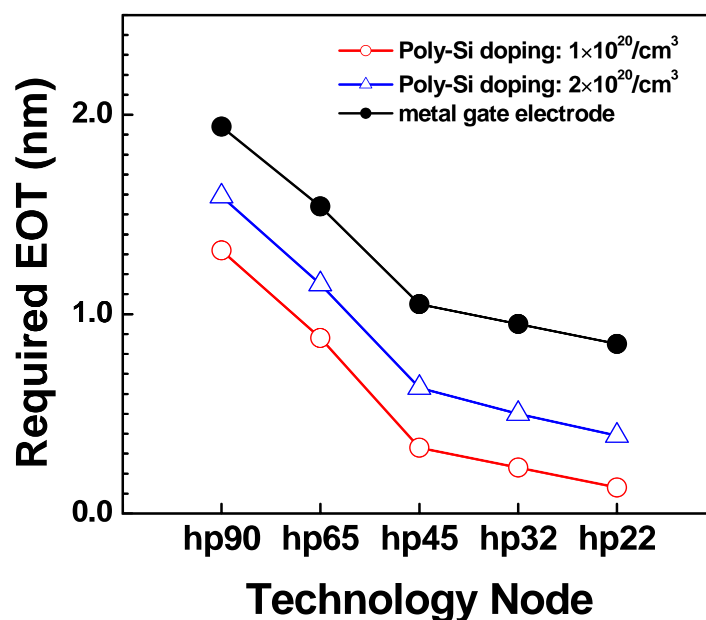


Fig. 2.6 Required EOT for each gate electrode with different poly doping concentration versus technology node, where *hp* stands for the industry's most aggressive half-pitch target [2.41].

2.3.2 Metal Gate Technology

The motivations for using metal gates as an alternative to polysilicon gate are to eliminate the gate depletion and dopant penetration. In addition, they greatly reduce the gate sheet resistance. However, there are strict requirements that the metals must satisfy in order to be useful for CMOS technology. The main requirements for metal-gate integration are to find a material and/or process that enables work-function modulation but is also compatible with CMOS processing. For planar bulk CMOS devices, the metal gates must have work functions that are similar to n+ doped (4.2 eV) and p+ doped polysilicon (5.1 eV) in order to maintain threshold voltages compatible with today's operating voltage [2.44],[2.45]. Moreover, the metal gate

electrodes must be thermally and chemically compatible with the underlying gate dielectrics. They must have good adhesion, and they could be controllably patterned. Work-function modulation is required in order to achieve the correct V_t for the transistors. Some researchers have proposed the use of a single midgap metal (the work function is at the midgap of the silicon bandgap), which is straightforward and is a low-cost integration method. However, this approach requires lower substrate doping to lower V_t, leading to significant short-channel effects, and hence limits its device application such as fully-depleted silicon on insulator (FDSOI) CMOS [2.45],[2.46].

Table 2.2 presents some of the possible candidate materials to be used as a metal gate electrode. They include pure metal with high melting temperature, metal alloy, conductive metal oxide, metal nitride, and metal silicide. For planar bulk CMOS devices requiring dual work functions, a simple and direct way is to use metal gate electrodes with two distinct work functions. In this integration approach, one replaces p+ doped and the other replaces n+ doped polysilicon. Although the successful CMOS integration with dual-metal gate electrodes on high-K dielectric using metal nitrides such as TaSiN for NMOS and TiN for PMOS has been reported [2.47], this approach requires critical etch and strip step to remove the first metal without damaging the gate dielectric. Moreover, the thermal stability of metal gate/dielectric stack is another issue [2.45].

Another integration approach for dual work function operation is to tune the metal work function for either n-MOS or p-MOS by varying the alloy composition or by doping. It has been reported that nitrogen implantation into Mo could tune the work function of metal electrode [2.48]. Here, the approach would be to deposit Mo for the NMOS and implant nitrogen into the Mo layer over the PMOS devices to

increase the work function. RuTa alloy has also been able to meet both the requirement of p-MOSFETs (when Ta < 20%) and that of n-MOSFETs (when 40% < Ta < 54%) [2.49]. However, this approach might also have integration issues such as the thermal stability of metal gate/dielectric stack. In addition, satisfying V_t requirements depends on range of work functions achieved with metal-metal alloy system or influence of dopant [2.45].

The next approach for work function modulation is to use fully silicided (FUSI) gates. The work function of metal silicide can also be tuned by the doping the polysilicon before silicidation anneal. The details of FUSI process will be discussed in the next section.

Table 2.2 Summary of some possible metal gate materials reported in the literature [2.45],[2.47]-[2.58].

Type of Device	Materials under consideration
NMOS	Ta, TaSiN, TaN, TaC, Ti, Mo, HfSi, NiSi+As doping, NiSi+Sb doping, etc.
PMOS	Ru, TiN, MoN, Ni, RuO_2, PtSi, NiSi+B doping, NiSi+In doping, etc.
Midgap metal device	HfN, TiN, NiSi, etc.

2.3.3 FUSI GATE PROCESS

Among the various recent metal gate candidates, fully silicided (FUSI) metal gates or metal gates by complete gate silicidation (CGS) have been demonstrated on the extension of existing self-aligned silicide (Salicide) technology [2.51]-[2.55]. FUSI gates offer several advantages over conventional metal gate processes such as easier integration and no PVD damage. In addition, FUSI process requires no high temperature post-gate step, which avoids the integration issue on the thermal stability of the metal gate/dielectric interface.

Successful integration of FUSI gates on MOSFET has been demonstrated by Tavel *et al.* [2.51] using $CoSi_2$ gates on SiON for the first time. $CoSi_2$ FUSI gate (hereafter Co-FUSI) is obtained by total polysilicon gate silicidation after source/drain activation anneal with only one additional CMP step. It is shown that Co-FUSI gate suppresses PDE and provides low gate resistivity, leading to improvement of device performance. Figure 2.7 shows the C-V curves of nMOS transistors. It clearly shows that Co-FUSI gate suppresses PDE and induces a V_{fb} shift. The V_{fb} shift by Co-FUSI gate process is mainly due to the work function change during full silicidation of polysilicon. Devices with nickel silicide [2.52]-[2.55], titanium silicide [2.56], hafnium silicide [2.57], and platinum silicide gates [2.58] have been reported subsequently.

Qin *et al*. [2.59] are the first to demonstrate that the presence of dopant in polysilicon can affect gate work function upon full silicidation. They have obtained three different work functions from n^+-doped, p^+-doped, and undoped polysilicon electrodes silicided with nickel. The obtained values of work functions are 4.6, 4.9, and 5.0 eV for n^+-doped, undoped, and p^+doped polysilicon, respectively.

Later, Kedzierski *et al.* [2.60] have demonstrated the successful integration of FUSI gate with dual work functions in CMOSFET. They achieve the dual work functions of nickel-FUSI gate using implantation of common dopants. They show that As, P as well as B are capable to set threshold voltages useful to NMOS and PMOS transistors. However, these FUSI processes may still have the integration issues such as the interaction between FUSI gate and gate dielectric.

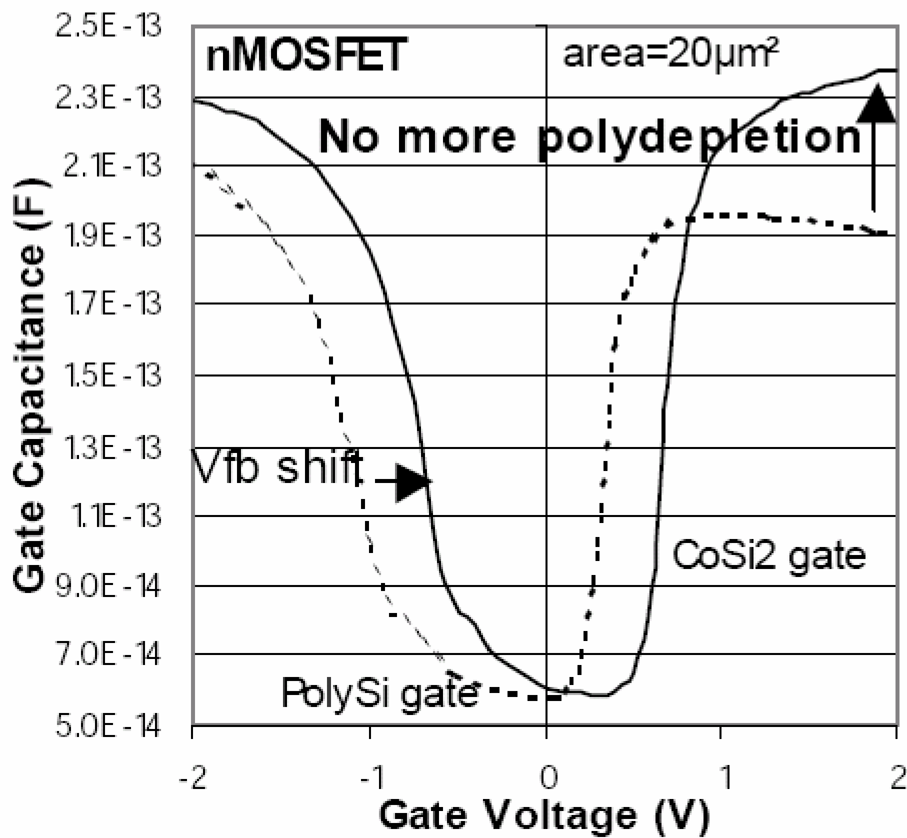


Fig. 2.7 C-V curves of nMOS transistors with W/L=50 µm/0.4 µm. Co-FUSI gate suppresses poly-depletion and induces a V_{fb} shift [2.51].

References

[2.1] G. D. Wilk, R. M. Wallace, J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations", *J. Appl. Phys.*, vol 89, pp. 5243-5275, 2001.

[2.2] S. A. Campbell, D. C. Gilmer, X.-C. Wang, M.-T. H. H.-S. Kim, W. L. Gladfelter, and J. Yan, "MOSFET transistors fabricated with high permittivity TiO_2 Dielectrics", *IEEE Trans. Electron Devices*, vol 44, pp. 104-109, 1997.

[2.3] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices", *J. Vac. Sci. Technol. B*, vol 18, pp. 1785-1791, 2000.

[2.4] M. Houssa, *High-K Gate Dielectric,* Bristol and Philadelphia: Institute of Physics Publishing, 2004.

[2.5] A. Chatterjee, R. A. Chapman, K. Joyner, *et al*., "CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator" in *IEDM Tech. Dig*., pp. 777-780, 1998.

[2.6] C. Chaneliere, J. L. Autran, R. A. B. Devine, B. Balland, "Tantalum pentoxide (Ta_2O_5) thin films for advanced dielectric applications", *Materials Science and Engineering*, R22, pp. 269-322, 1998.

[2.7] K. Eisenbeiser, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopad, W. J. Ooms, L. Salem, S. Bradshaw, and C. D. Overgaard, "Field effect transistors with $SrTiO_3$ gate dielectric on Si", *Appl. Phys. Lett.*, vol 76, pp. 1324-1326, 2000.

[2.8] L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. Brown, C. J. Case, R. C. Keller, Y. O. Kim, E. J. Laskowski, M. D. Morris, R. L. Opila, P. J. Silverman, T. W. Sorsch, and G. R. Weber, "Gate quality doped high K films for CMOS beyond 100 nm: 3 – 10nm Al_2O_3 with low leakage and low interface states", in *IEDM Tech. Dig.*, pp. 605-608, 1998.

[2.9] D.-G. Park, H.-J. Cho, K.-Y. Lim, C. Lim. I.-S. Yeo, J.-S. Roh, and J. W. Park, "Characteristics of n^+polycrystalline-Si/Al_2O_3/Si metal-oxide-semiconductor structures prepared by atomic layer chemical vapor deposition using $Al(CH_3)_3$ and H_2O vapor", *J. Appl. Phys.*, vol 89, pp. 6275-6280, 2001.

[2.10] M. Copel, M. Gribelyuk, and E. Gusev, "Structure and stability of ultrathin zirconium oxide layers on Si(001)", *Appl. Phys. Lett.*, vol 76, pp. 24-27, 2000.

[2.11] P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, and J. G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)", *J. Appl. Phys.*, vol 91, pp. 4353-4363, 2002.

[2.12] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS characteristics of ultra thin rapid thermal CVD ZrO_2 and Zr silicate gate dielectrics", in *IEDM Tech. Dig.*, pp. 27-30, 2000.

[2.13] Y. Kim, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres, J. Lim, B. Foran, F. Shaapur, A. Agarwal, P. Lysaght, G. A. Brown, C. Young, S. Borthakur, H.-J. Li, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R. W. Murto, A. Hou, H. R. Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanec, and C. Werkhoven, "Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-K gate dielectrics with polysilicon gate electrode", in *IEDM Tech. Dig.*, 20-02, 2001.

[2.14] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with polysilicon gate electrode", in *IEDM Tech. Dig*., 02-04, 2000.

[2.15] B. Tavel, X. Garros, T. Skotnicki, *et al*., "High performance 40 nm nMOSFETs with HfO_2 gate dielectric and polysilicon damascene gate", in *IEDM Tech. Dig*., pp. 429-432, 2002.

[2.16] H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G.A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner and R. W. Murto, "Integration of high-k gate stacks into planar scaled CMOS integrated circuits" in *Nano and Giga Challenges in Microelectronics (2002)*, 2002.

[2.17] G. D. Wilk, R. M. Wallace, J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics", *J. Appl. Phys.*, vol 87, pp. 484-492, 2000.

[2.18] W. Zhu, T. P. Ma, T. Tamagawa, and Y. Di, "HfO_2 and HfAlO for CMOS: Thermal stability and current transport," in *IEDM Tech. Dig*., pp. 463-466, 2001.

[2.19] C. H. Choi, S. J. Rhee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong, "Thermally stable CVD HfO_xN_y Advanced Gate Dielectrics with Polysilicon Gate Electrode" in *IEDM Tech. Dig*., 34-03, 2002.

[2.20] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake and N. Fukushima, "Additional scattering effects for mobility degradation in Hf-silicate gate MISFETs" in *IEDM Tech. Dig*., 26-03, 2002.

[2.21] Chun-Li Liu, Z. X. Jiang, R. I. Hedge, D. D. Sieloff, R. S. Rai, D. C. Gilmer, C. C. Hobbs, P. J. Tobin and Shifeng Lu, "Theoretical and experimental

investigation of boron diffusion in polycrystalline HfO_2 films," *Appl. Phys. Lett*., vol 81, pp. 1441-1443, 2002.

[2.22] H. Kim, P. C. McIntyre and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition," *Appl. Phys. Lett.,* vol 82, pp. 106-108, 2003.

[2.23] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Sarawat, S. Haukka and M. Tuominen, "Electrical and materials properties of ZrO_2 gate dielectrics grown by atomic layer chemical vapor deposition," *Appl. Phys. Lett*., vol 78, pp. 2357-2359, 2001.

[2.24] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D. L. Kwong, J. S. Oan, C. H. Ang, J.Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Applied Physics Lett.,* vol 81, pp. 376-378, 2002.

[2.25] L. Manchanda, M. D. Morris, M. L. Green, R. B. van Dover, F. Klemens, T. W. Sorsch, P. J. Silverman, G. Wilk, B. Busch, S. Aravamudhan, "Multi-component high-*K* gate dielectrics for the silicon industry," *Microelectronic Engineering*, vol 59, pp. 351-359, 2001.

[2.26] H. Y. Yu, N. Wu, M. F. Li, C. X. Zhu, B. J. Cho, D. L. Kwong, C. H. Tung, J. S. Pan, J. W. Chai, W. D. Wang, D. Z. Chi, C. H. Ang, J. Z. Zheng, "Thermal Stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si," *Applied Physics Letters*, vol 81, pp. 3618-3620, 2002.

[2.27] M. S. Joo, B. J. Cho, C. C. Yeo, N. Wu, H. Y. Yu, C. X. Zhu, M. F. Li, D. -L. Kwong, N. Balasubramanian, "Dependence of Chemical Composition Ratio

on Electrical Properties of HfO_2-Al_2O_3 Gate Dielectric," *Jpn. J. Applied Physics*, vol 42, pp. L220-L222, 2003.

[2.28] Y. Harada, M. Niwa, S. J. Lee and D.-L. Kwong, "Specific structural factors influencing on reliability of CVD-HfO_2," in *Symp. on VLSI Tech. Dig*., T03P3, 2002.

[2.29] H. J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, and J. C. Lee, "Novel nitrogen profile engineering for improved TaN/HfO_2/Si MOSFET performance" in *IEDM Tech. Dig*., 30-02, 2001.

[2.30] H. Y. Yu, J. F. Kang, J.D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du, and D.-L. Kwong, "Thermally robust high quality HfN/HfO_2 gate stack for advanced CMOS devices," in *IEDM Tech. Dig.,* pp. 99-102, 2003.

[2.31] A. Morioka, H. Watanabe, M. Miyamura, T. Tatsumi, M. Saitoh, T. Ogura, T. Iwamoto, T. Ikarashi, Y. Saito, Y. Okada, H. Watanabe, Y. Mochiduki, and T. Mogami, "High mobility MISFET with low trapped charge in HfSiO films" in *Symp. on VLSI Tech*., 12A-4, 2003.

[2.32] S. Saito, Y. Shimamoto, K. Torii, Y. Manabe, M. Caymax, J. W. Maes, M. Hiratani, and S. Kimura, "Mobility reduction due to remote charge scattering in Al_2O_3/SiO_2 gate-stacked MISFETs" in *Extended Abstracts of SSDM 2002*., pp. 704-705, 2002.

[2.33] S. Takagi, A. Toriumi, M. Iwase, H. Tango, "On the universality of inversion layer mobility in Si MOSFET's" *IEEE Trans. Electron Devices*, vol. 41, pp. 2357-2368, 1994.

[2.34] J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle, "Asymmetric energy distribution of interface traps in n- and p-MOSFETs with HfO_2 gate dielectric on ultrathin SiON buffer layer", *IEEE Electron Device Letters*, vol 25, pp. 126-128, March 2004.

[2.35] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-k insulator: The role of remote phonon scattering" *J. Appl. Phys.*, vol. 90, pp. 4587-4608, 2001.

[2.36] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-K/metal-gate stack and its MOSFET characteristics", *IEEE Electron Device Letters*, vol 25, pp. 408-410, 2004.

[2.37] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface" in *Symp. on VLSI Tech.*, 2-1, 2003.

[2.38] C. W. Yang, Y. K. Fang, C. H. Chen, S. F. Chen, C. Y. Lin, M. F. Wang, Y. M. Lin, T. H. Hou, C. H. Chen, L. G. Yao, S. C. Chen, and M. S. Liang, "Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metal-oxide-semiconductor field-effect transistors for high-K-HfO_2 dielectric" *Applied Physics Letters*, vol 83, pp. 308-310, 2003.

[2.39] J. K. Schaeffer, *et al.*, "Physical and electrical properties of metal gate electrodes on HfO2 gate dielectrics," *J. Vacuum Science Technology B*, vol. 21, no.1, pp. 11-17, 2003.

[2.40] S.-H. Lo, D. A. Buchanan, Y. Taur, L.-K. Han, and E. Wu, "Modeling and Characterization of n+-and p+-polysilicon-gated ultra thin oxides (21-26 Å)" in *Symp. on VLSI Tech.*, pp. 149-150, 1997.

[2.41] Semiconductor Industry Association (SIA), "*International Technology Roadmap for Semiconductors*, *2004 Update"*, http://www.itrs.net/Common/2004Update/2004Update.htm.

[2.42] J. R. Pfiester, F. K. Baker, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, J. W. Miller, C. D. Gunderson, and L. C. Parrillo, "The effects of boron penetration on p+polysilicon gated PMOS devices," *IEEE Trans. Electron Devices*, vol. 37, pp. 1842-1851, 1990.

[2.43] M. A. Quevedo-Lopez, M. R. Visokay, J. J. Chambers, M. J. Bevan, A. LiFatou, L. Colombo, M. J. Kim, B. E. Gnade, and R. M. Wallace, "Dopant penetration studies through Hf silicate," *J. Appl. Phys.*, vol 97, 043508, 2005.

[2.44] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate workfunction on device performance at the 50 nm technology node," *Solid-State Electro.*, vol 44, pp. 1077-1080, 2000.

[2.45] K. Henson and M. Jurczak, "Metal-gate integration challenges," *Semiconductor Fabtech*, 25th Edition, pp. 76-79, also available on http://www.fabtech.org.

[2.46] B. Cheng, B. Mariti, S. Samavedam, J. Grant, B. Taylor, P. Tobin, and J. Mogab, "Metal gates for advanced sub-80-nm SOI CMOS technology," *IEEE Int. SOI, Conf.*, pp. 91-92, 2001.

[2.47] S. B. Samavedam, *et al.*, "Metal gate MOSFETs with HfO_2 gate dielectric" in *Symp. on VLSI Tech.*, 3-2, 2002.

[2.48] R. Lin, Q. Lu, P. Ranade, T.-J. King, and C. Hu, "An adjustable work function technology using Mo gate for CMOS devices", *IEEE Electron Device Letters*, vol 23, pp. 49-51, 2002.

[2.49] H. Zhong, S. Hong, Y. Suh, H. Lazar, G. Heuss, and V. Misra, "Properties of Ru-Ta alloys as gate electrodes for NMOS and PMOS silicon devices," in *IEDM Tech. Dig.,* pp. 467-470, 2001.

[2.50] H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, C. X. Zhu, D. L. Kwong, C. H. Tung, K. L. Bera, and C. J. Leo, "Robust HfN metal gate electrode for advanced MOS devices application" in *Symp. on VLSI Tech.*, pp. 151-152, 2003.

[2.51] B. Tavel, T. Skotnicki, G. Pares, N. Carrière, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally silicided ($CoSi_2$) polysilicon: a novel approach to very low-resistive gate (~2Ω/□) without metal CMP nor etching," in *IEDM Tech. Dig.,* pp. 825-828, 2001.

[2.52] W. P. Maszara, Z. Krivokapic, P. King, J.-S. Goo, and M.-R. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates," in *IEDM Tech. Dig.,* pp. 367-370, 2002.

[2.53] J. Kedzierski, D. Boyd, C. Cabral, Jr., P. Ronsheim, S. Zafar, P. M. Kozlowski, J. A. Ott, and M. Ieong, "Threshold voltage control in NiSi-gated MOSFETs through SIIS," *IEEE Trans. Electron Devices*, vol. 52, pp. 39-46, 2005.

[2.54] D. Aimé, B. Froment, F. Cacho, V. Carron, S. Descombes, Y. Morand, N. Emonet, F. Wacquant, T. Farjot, S. Jullian, C. Laviron, M. Juhel, R. Pantel, R. Molins, D. Delille, A. Halimaoui, D. Bensahel, and A. Souifi, "Work function

tuning through dopant scanning and related effects in Ni fully silicided gate for sub-45nm nodes CMOS," in *IEDM Tech. Dig.,* pp. 87-90, 2004.

[2.55] J. Kedzierski, M. Ieong, T. Kanarsky, Y. Zhang, and H.-S. P. Wong, "Fabrication of metal gated FinFETs through complete gate silicidation with Ni," *IEEE Trans. Electron Devices*, vol. 51, pp. 2115-2120, 2004.

[2.56] P. Xuan and J. Bokor, "Investigation of NiSi and TiSi as CMOS gate materials," *IEEE Electron Device Letters*, vol 24, pp. 634-636, 2003.

[2.57] C. S. Park, B. J. Cho, and D.-L. Kwong, "Thermally stable fully silicided Hf-silicide metal-gate electrode," *IEEE Electron Device Letters*, vol 25, pp. 372-374, 2004.

[2.58] T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita, M. Ohno, H. Ota, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake, and A. Toriumi, "Partial silicides technology for tunable work function electrodes on high-K gate dielectrics-Fermi level pinning controlled $PtSi_x$ for $HfO_x(N)$ pMOSFET-," in *IEDM Tech. Dig.,* pp. 83-86, 2004.

[2.59] M. Qin, V. M. C. Poon, and S. C. H. Ho, "Investigation of polysilicon nickel silicide films as a gate material," *J. The Electrochemical Society*, vol 148, G271-G274, 2001.

[2.60] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K.-L. Lee, B. A. Rainey, D. fried, P. Cottrell, H.-S. Philip Wong, M. Ieong, and W. Haensch, "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," in *IEDM Tech. Dig.,* pp. 247-250, 2002.

CHAPTER 3

FORMATION OF HfAlO GATE DIELECTRIC USING SINGLE COCKTAIL LIQUID SOURCE IN MOCVD PROCESS

3.1 INTRODUCTION

Thin hafnium-oxide film (HfO_2) has been extensively studied among various metal oxides in recent years as a strong candidate for the next generation gate dielectric material because of its reasonably high dielectric constant value, thermodynamical stability in contact with Si, potential compatibility with polysilicon gate process and relatively low amount of fixed charge at the interface [3.1]-[3.6]. As discussed in Chapter 2, however, the HfO_2 film has shown a poor thermal stability, which results in the increase of leakage current after subsequent thermal processes and the interfacial layer growth during following thermal processing. The film is easily crystallized at a temperature as low as 400 ºC [3.7], forming grain boundaries which serve as leakage current paths and diffusion paths of impurities such as oxidant [3.8]. Therefore, high temperature processing causes the increase of the leakage current of HfO_2 as well as the increment of equivalent oxide thickness (EOT) due to the

additional growth of interfacial layer. This can pose a serious limitation to further scaling of HfO_2 into the regime of EOT of 10 Å and below.

Recently, several research groups [3.7],[3.9],[3.10] have reported that incorporation of Al into HfO_2 film helps to improve the thermal stability of HfO_2 film and retard the oxygen diffusion through the film. The retardation of oxygen diffusion is probably attributed to both reduced oxygen diffusion coefficient through the bulk of the film and reduced the grain boundary paths due to the enhanced thermal stability [3.11]. In addition, the acceptably high dielectric constant value and band offset value of $HfAl_xO_y$ (hereafter HfAlO) alloy make the film one of the most promising candidates for high-K gate dielectric application.

Until now, HfAlO has been formed by using two separate metal precursors such as $HfCl_4$ and $Al(CH_3)_3$ with H_2O as oxygen source in Atomic Layer Deposition (ALD) [3.9]-[3.12], or by using two sputtering targets of Hf and Al in Jet Vapor Deposition (JVD) [3.7] or Physical Vapor Deposition (PVD) [3.13]. However, little work has been reported on the valuable result using Metal Organic Chemical Vapor Deposition (MOCVD) system that is considered as one of useful high-k deposition system. The reason is probably because the process using two precursors in MOCVD is much more complicated and difficult than that in ALD. In this chapter, the successful deposition of high quality HfAlO film with a wide range of composition ratio controllability between HfO_2 and Al_2O_3 in HfAlO is demonstrated using a single cocktail liquid source in a MOCVD system, which is a suitable techniques for mass production in terms of process simplicity and reproducibility. In addition, the effect of the composition ratio on the electrical properties of HfAlO is also studied.

3.2 EXPERIMENTAL

3.2.1 HfAlO DEPOSITION USING A SINGLE COCKTAIL SOURCE

MOCVD HfAlO films were deposited using a multi-chamber cluster tool, so that all the processes including surface nitridation (SN), HfAlO deposition, and post deposition annealing (PDA) were carried out without breaking the vacuum. Surface nitridation (SN) were preformed at 700ºC for 1 minute in an NH_3 ambient. HfAlO films were then deposited at 350ºC ~ 600ºC using a single cocktail source, $HfAl(MMP)_2(OiPr)_5$.

Figure 3.1 shows the chemistry of the single cocktail source. It consists of two central atoms of Hf and Al and two kinds of ligands that are OR: Oi-C_3H_7 (OiPr) and OR': $OC(CH_3)_2CH_2OCH_3$ (MMP). By decomposition of this precursor in the chamber at a raised temperature, HfAlO film can be obtained. The composition ratio between Hf and Al in HfAlO film might be dependent on the process condition such as deposition temperature, liquid precursor flow rate, carrier gas flow rate, and so on.

Since the precursor which is a liquid at room temperature has extremely low vapor pressure of about 6.4×10^{-5} Torr, a Liquid Delivery System (LDS) was adopted for the delivery of the precursor into the chamber. This precursor is first introduced into a vaporizer chamber by a push gas (argon) and its flow rate is controlled by Liquid Mass Flow Controller (LMFC). Another gas line of argon, called argon carrier gas, is used to vaporize the liquid precursor in the vaporizer chamber and carries the vaporized precursor into the process chamber. After deposition of high-K dielectric, PDA was performed at 700ºC for 1 minute in a N_2 ambient to remove the H- and/or C-containing bonds in the film and densify the film [3.2],[3.14].

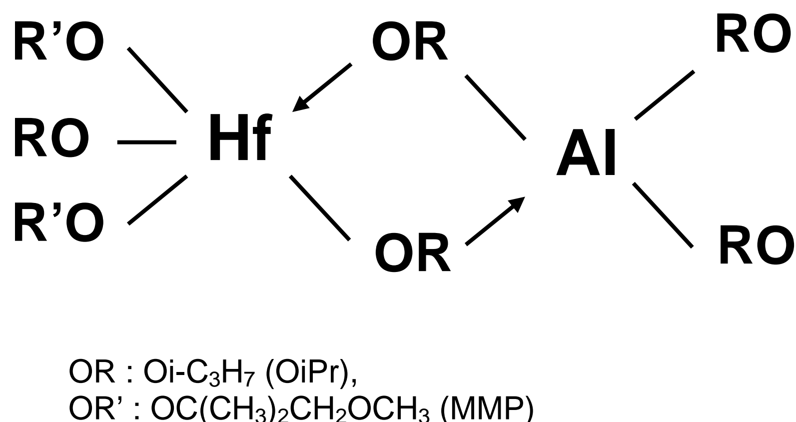


Fig. 3.1 The chemistry of the single cocktail liquid source: $HfAl(MMP)_2(OiPr)_5$

3.2.2 FABRICATION PROCEDURES OF MOS CAPACITOR AND TRANSISTOR

The fabrication of metal-oxide-silicon (MOS) capacitors started with field oxide isolation on p-type Si (100) substrate (4-8 Ω·cm resistivity) and active region patterning. The fabrication of NMOS transistor started with p-well formation on p-type Si (100) substrate (4-8 Ω·cm resistivity) using well implantation followed by a rapid thermal annealing (RTA). After the standard pre-gate clean and a final dilute 1% HF dip, the wafers were inserted into a 3-chamber MOCVD cluster tool. Surface nitridation technique has been employed to passivate the substrate prior to HfO_2 deposition to minimize the interfacial layer growth [3.15]. After surface nitridation, HfAlO films were deposited. For comparison, pure HfO_2 samples were also prepared by MOCVD at 400ºC using $Hf(OC(CH_3)_3)_4$ precursor contained in a bubbler system, which can be bubbled and delivered by argon. TaN was deposited for gate electrode using reactive sputtering. For investigation of thermal stability of the high-K films, RTA at 950ºC for 30 sec was added either before or after TaN deposition. For NMOS

transistor fabrication, a RTA for source/drain activation was performed at 900ºC for 30 sec after TaN gate electrode patterning and source/drain implantation. All devices were subjected to a forming gas anneal at 420ºC for 10 minutes after metallization. Table 3.1 shows the complete fabrication process flows for MOS capacitor and NMOS transistor.

3.2.3 EXPERIMENTAL SETUP

Thick HfO_2 and HfAlO films with a thickness of around 200 Å were also prepared for X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) analysis. The crystallinity properties of HfAlO and HfO_2 were checked by XRD and composition ratio of HfAlO films were evaluated by XPS depth profile. The capacitance versus voltage (C-V) and the current versus voltage (J_g – V) measurements were conducted using HP 4284A precision LCR meter and HP4156A precision semiconductor parameter analyzer for MOS capacitors. The frequency used for C-V measurement was 100 kHz. The EOT of each gate dielectric was extracted taking quantum mechanical (QM) effect into consideration using a simulator developed by UC Berkeley [3.16]. The V_{fb} value of each sample is calculated from the comparison of its C-V curve with the C-V curve simulated by the aforementioned simulator. The transistor performances were evaluated using HP 4155B semiconductor parameter analyzer for NMOS transistor.

Table 3.1 Fabrication process for MOS capacitor and NMOS Transistor.

➢ **MOS Capacitor Fabrication**	➢ **NMOS Tr. Fabrication**
• Field oxidation and active patterning	• P-well Formation
• RCA cleaning and DHF (1:100) dip	• RCA cleaning and DHF (1:100) dip
• Surface nitridation: NH_3, 700°C, 60sec, 50 torr	• Surface nitridation: NH_3, 700°C, 60sec, 50 torr
• **High-k deposition in MOCVD cluster tool**	• **High-k deposition in MOCVD cluster tool**
a. HfAlO Dep. at 350~600ºC using $HfAl(MMP)_2(OiPr)_5$	c. HfAlO Dep. at 450ºC using $HfAl(MMP)_2(OiPr)_5$
b. HfO_2 Dep. at 400ºC using $Hf(OC(CH_3)_3)_4$	d. HfO_2 Dep. at 400ºC using $Hf(OC(CH_3)_3)_4$
• Post deposition annealing (PDA): N_2, 700°C, 60sec, 200Torr	• Post deposition annealing (PDA): N_2, 700°C, 60sec, 200Torr
• RTA: 950°C, N_2, 30 sec (or skip)	• TaN deposition: 3mT, 400W
• TaN deposition: 3mT, 400W	• Gate patterning using Single Tr. Mask
• Gate patterning	• S/D formation
• RTA: 950°C, N_2, 30 sec (or skip)	• RTA: 900°C, N_2, 30 sec
• Forming gas anneal: 420°C, 10 min in a H_2/N_2 ambient	• Forming gas anneal: 420°C, 10 min in a H_2/N_2 ambient

3.3 RESULTS AND DISCUSSION

3.3.1 COMPOSITION RATIO CONTROL OF HfAlO FILM BY PROCESS VARIATION

For HfAlO films, there exists an optimum ratio between Hf and Al for achieving the best electrical properties. Therefore, the major concern in using a single source for the MOCVD HfAlO process is how to control the composition ratio between Hf and Al in HfAlO film. Variations of process conditions were attempted to obtain the acceptably wide range of composition ratio variation.

First, the effects of flow rates of argon carrier gas, oxygen reaction gas, and liquid precursor were investigated. The deposition temperature and deposition pressure were fixed at 400ºC and 400 mTorr, respectively. Figure 3.2 shows the dependence of the composition ratio on the flow rate variations of (a) argon carrier gas, (b) oxygen reaction gas, and (c) liquid precursor. As seen in Fig. 3.2, the composition ratio is not much affected and the controllable range by flow rate variations is between 70 ~ 80 % of HfO_2 in HfAlO. It is interesting to note that HfAlO film can successfully be obtained even without O_2 flow and the composition ratio of the sample without O_2 flow is not much different from those of the samples deposited with O_2 flow of 50 sccm and 100 sccm, as shown in Fig. 3.2 (b). This result indicates that O_2 flow has little effect in the deposition of HfAlO when the precursor $HfAl(MMP)_2(OiPr)_5$ is used. This is probably due to the fact that oxygen can be supplied from the precursor itself through thermal decomposition process in the chamber.

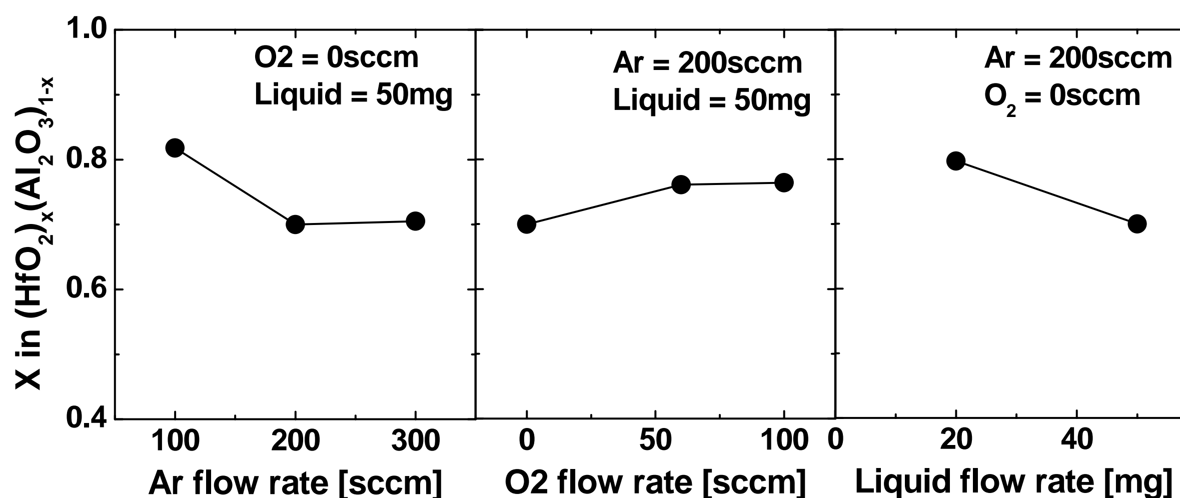
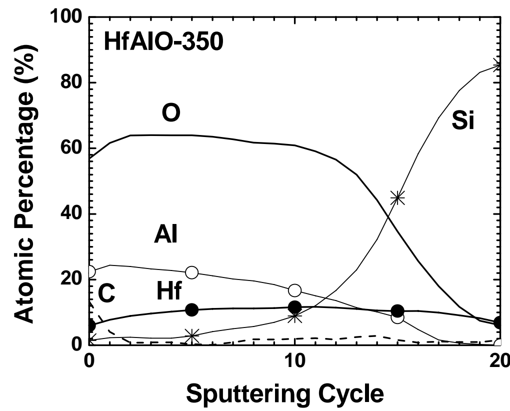


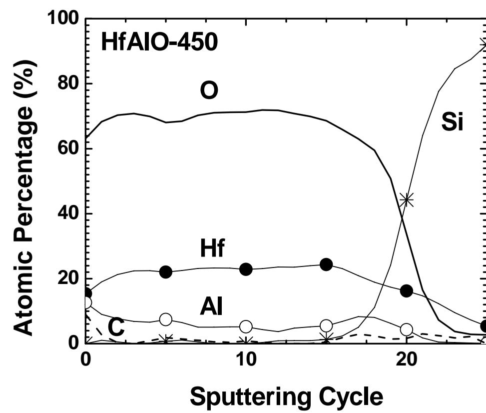
Fig. 3.2 Dependence of composition ratio on process parameters such as (a) Ar carrier flow rate, (b) O_2 flow rate, and (c) Liquid precursor flow rate. Deposition temperature is 400ºC. The composition ratio is not much affected by the flow rate.

Next, the effect of deposition temperature was investigated. Figure 3.3 shows the XPS depth profiles of HfAlO films deposited at three different deposition temperatures of 350ºC, 450ºC, and 600ºC. The three samples are denoted as HfAlO-350, HfAlO-450, and HfAlO-600, respectively. The thicknesses of HfAlO-450 and HfAlO-600 samples were around 200 Å, while that of HfAlO-350 was around 70 Å because of very low deposition rate at 350°C. It is observed that the carbon concentration in the film decreases with the increase of deposition temperature. However, the carbon concentrations in the film bulks are all reasonably low even at HfAlO-350 sample, so it is expected that the carbon concentration may not play a decisive role in electrical properties of HfAlO films in our experiments. The HfAlO-350 sample shows more Al incorporation than Hf incorporation in the film, whereas HfAlO-450 and HfAlO-600 samples show more Hf incorporation. The relatively broadened depth profile of HfAlO-350 compared to those of other samples is due to

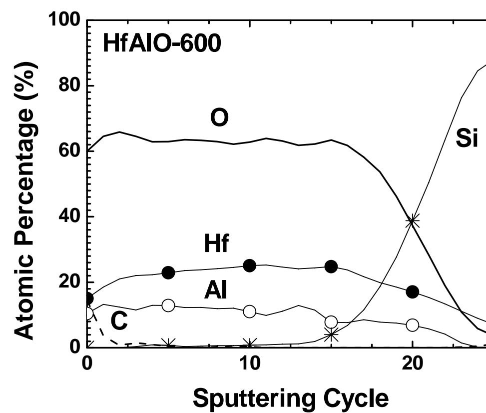
lower sputtering rate during XPS measurement, as the film is much thinner than the other two.



(a)



(b)



(c)

Fig. 3.3 XPS depth profiles of HfAlO films deposited at (a) 350ºC, (b) 450ºC, and (c) 600ºC. The 350ºC sample exhibits Al-rich property while the 450ºC and 600ºC samples exhibit Hf-rich property.

The composition ratio between HfO_2 and Al_2O_3 for each HfAlO sample was evaluated, taking the values at the middle portion of the high-K film in XPS depth profile. The temperature dependences of deposition rate and composition ratio are shown in Fig. 3.4. As shown in the figure, a wide range of composition ratio between 45 to 90 % of HfO_2 in HfAlO is achieved by varying the deposition temperature. Higher temperature deposition introduces more hafnium into the film but there is a turn-around point of the composition ratio at the deposition temperature of 450ºC where the HfO_2 percentage is maximum of around 90% (Al_2O_3 10%). From the results in Figs. 3.3 and 3.4, it is found that the deposition temperature plays a major role in the composition ratio control. Comparing the deposition rate and composition ratio shown in Fig. 3.4, it is interesting to note that the composition ratio has a very strong correlation with the deposition rate. Higher deposition rate causes the higher Hf incorporation into the film. Study of detailed mechanism for this behavior would be interesting.

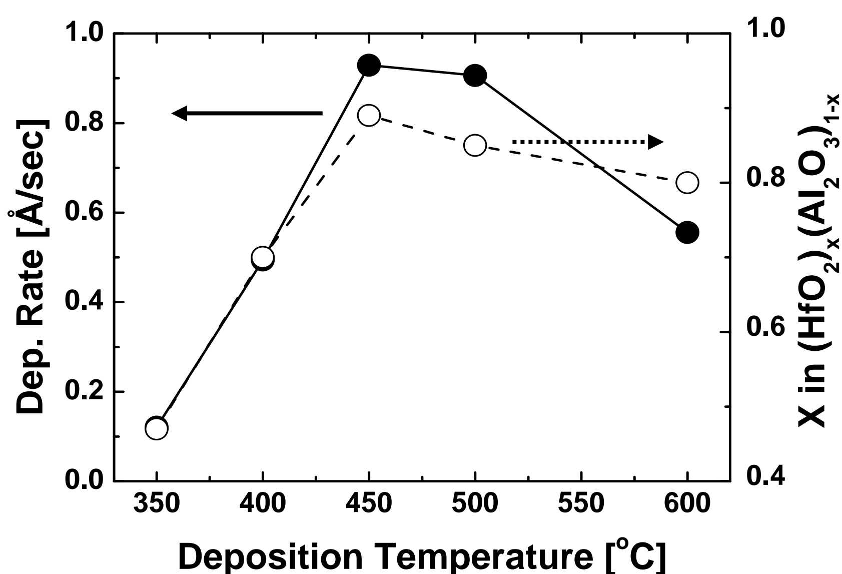
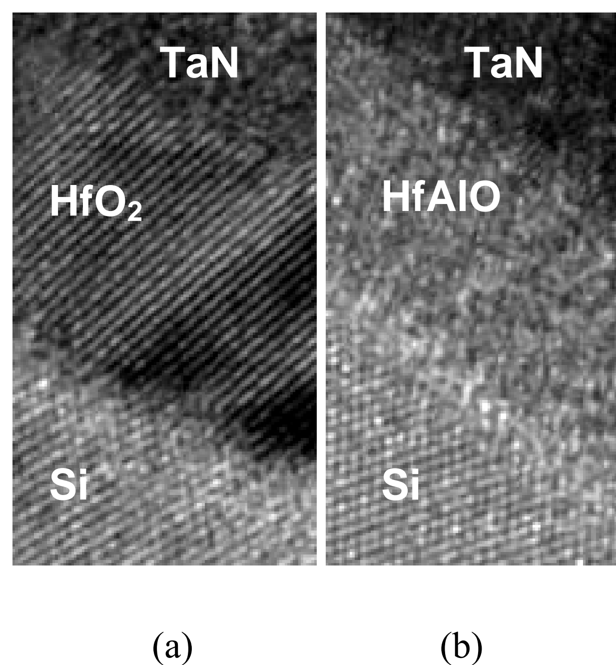


Fig. 3.4 Temperature dependence on deposition rate and composition ratio of HfAlO. The composition ratio changes over a wide range and shows a very strong correlation with the deposition rate.

3.3.2 THERMAL STABILITY OF HfAlO

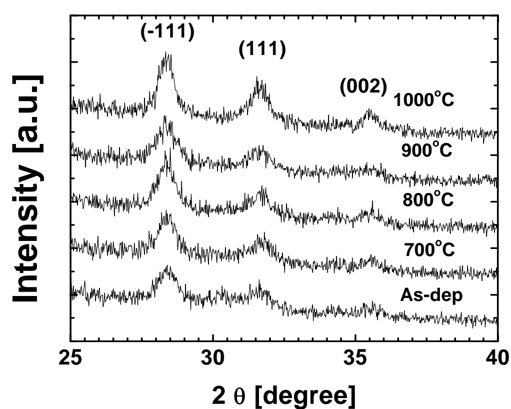
Most of high-K dielectric films are apt to be crystallized during deposition or subsequent high temperature process. Poly-crystallization of thin films generates grain boundaries in thin dielectric films which act as leakage current path, resulting in high leakage current. Therefore, to remain amorphous after thermal process is important to achieve the lower leakage current. Figure 3.5 shows the images taken by high-resolution cross-sectional transmission electron microscopy (XTEM) of HfO_2 and HfAlO with TaN gate electrode. Both films were deposited at the same temperature of 400ºC and went through the same PDA condition of 700ºC for 1 minute. It is clearly seen that HfAlO film remains amorphous after PDA at 700ºC while HfO_2 is crystallized.



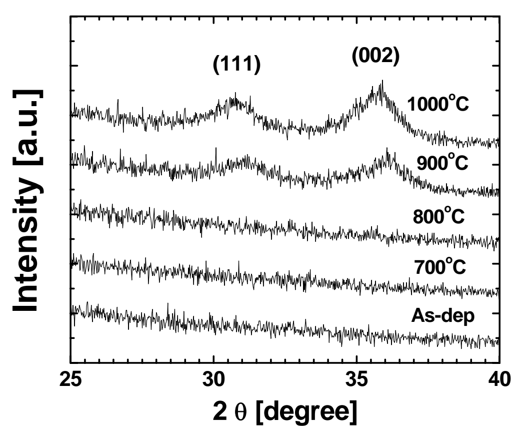
(a) (b)

Fig. 3.5 XTEM images of HfO_2 and HfAlO after 700ºC in-situ PDA treatment. HfAlO layer remains amorphous while HfO_2 is crystallized. Both films were deposited at 400ºC without surface nitridation.

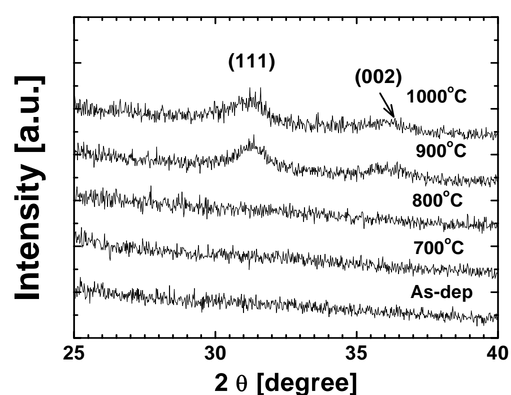
The same trend is also found in X-ray diffraction (XRD) measurement. Figure 3.6 shows the XRD spectra of HfO_2, HfAlO-400, and HfAlO-450 after annealing at different temperature. The thicknesses of HfO_2 and two HfAlO samples deposited at 400ºC and 450ºC were around 200 Å. The result shows that the as-deposited HfO_2 film is already crystallized, showing three crystalline peaks related with HfO_2 (-111), (111), and (002), which is well matched with result in the literature [3.8]. However, two HfAlO samples remain amorphous up to 800ºC for 20 second annealing. And both samples do not show the strong crystalline peak of HfO_2 (-111) even after the annealing at 1000°C, indicating the significant improvement in thermal stability by adding Al into HfO_2. It is interesting to observe that HfAlO-450 film dose not show the strong (002) peak unlike HfAlO-400. It is not clear at the moment why HfAlO-450 film shows less crystallization than HfAlO-400 even though HfAlO-450 contains less amount of Al_2O_3 fraction in the film. The important point to be noted is that thermal stability of HfAlO could be improved by incorporation of Al_2O_3 of as low as 10%. Lower fraction of Al_2O_3 in HfAlO will have advantage of less reduction of dielectric constant, as the K value of Al_2O_3 is much smaller than that of HfO_2.



(a)



(b)



(c)

Fig. 3.6 XRD spectra of **(a)** HfO_2, **(b)** HfAlO-400, and **(c)** HfAlO-450 after annealing at different temperatures. As-deposited HfO_2 is already crystallized while HfAlO remains amorphous up to 800ºC.

3.3.3 WET CHEMISTRY OF HfAlO

One of the critical challenges for the implementation of high-K dielectric into a standard CMOS flow is the complete removal of high-k dielectric on the active regions, especially in source/drain region, before source/drain implantation and its activation anneal. The residue of high-K dielectric may cause the knock-on metal into the source/drain regions and create an obstacle to silicidation of the source/drain regions [3.17]. A wet chemistry to etch high-K dielectrics would be advantageous to avoid plasma damage and overetching to Si substrate during a dry etch. It has been reported that HfO_2 after high temperature annealing is hardly etched by a dilute HF solution at room temperature [3.17],[3.18] and its etch rate is also dependent on the degree of crystallization [3.19]. In this section, we investigate the effect of Al incorporation into HfO_2 film on wet chemistry.

Figure 3.7 shows the etch rate at 1:100 DHF solution of HfO_2 and three kinds of HfAlO films. The initial thicknesses of all high-K films are around 200 Å. While the etch rate of as-deposited HfO_2 film is close to that of SiO_2, those of all the as-deposited HfAlO films are much higher. It is interesting to note that as-deposited HfAlO-450 sample shows lower etch rate than HfAlO-400 and HfAlO-500 films. This is probably due to lower Al incorporation into HfO_2. This result indicates that the etch rate of HfAlO film is strongly dependent on Al composition ratio. After 700℃ PDA, the etch rate of HfO_2 film is substantially reduced due to densification and crystallization of film. On the contrary, HfAlO-450 film can still be etched away because it remains amorphous and the etch rate is two times higher than that of SiO_2, which is around 0.5 Å/sec. As the RTA temperature increases, the etch rate of HfAlO-450 film continues to decrease until 900ºC due to the densification of the film. Once the film starts to crystallize above 900ºC, its etch rate tends to saturate. However, the

etch rate of around 0.5 Å/sec is still high enough to etch away the whole film within an acceptable dipping time. On the contrary, HfAlO-400 film becomes hardly etched by a DHF solution after 900ºC RTA probably due to the higher degree of crystallization compared to HfAlO-450 film as discussed in Fig. 3.6. This result indicates that the etch rate of HfAlO film is also dependent on the degree of crystallization and the HfAlO-450 film can be etched away by a DHF solution even after high temperature anneal owing to the low degree of crystallization. This result shows that HfAlO has clear advantage over HfO_2 for the implementation into a standard CMOS flow in terms of the easy removal of high-k dielectric on the active regions.

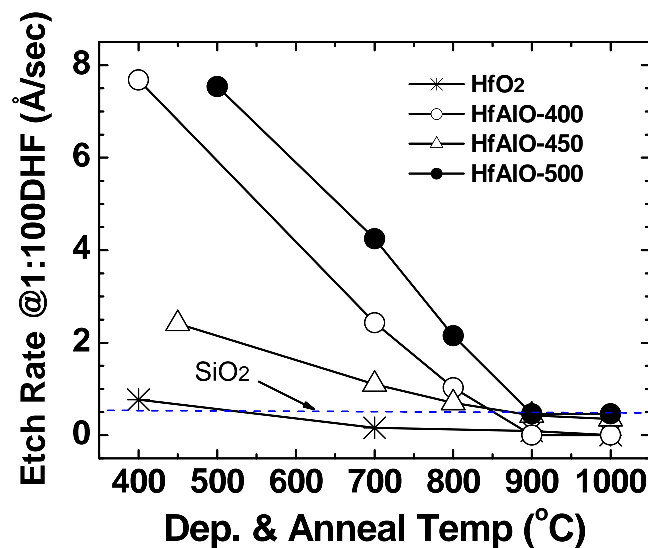


Fig. 3.7 The dependence of etch rate at a dilute 1% HF (1:100 DHF) solution of HfO_2 and HfAlO films on deposition and RTA temperature. The dashed line that is the etch rate of thermal oxide (SiO_2) is a guide for the eyes.

3.3.4 INTERFACIAL LAYER GROWTH

HfO_2 has been known to be transparent to the oxygen diffusion [3.20]. Annealing in an oxygen-rich ambient will lead to fast diffusion of oxygen through the HfO_2, causing the growth of uncontrolled low-k interfacial layer. The uncontrolled low-k layer poses a serious limitation to the scaling of EOT for HfO_2 gate dielectrics. It has been demonstrated that alloying HfO_2 with Al using atomic layer deposition (ALD) system results in the reduction of interfacial layer growth as well as the retardation of crystallization of HfO_2 films [3.11]. In addition, the interfacial layer growth becomes smaller with more Al incorporated into HfO_2. However, the HfAlO film by alloying HfO_2 with Al using MOCVD system shows somewhat different properties from ALD HfAlO films in terms of the interfacial layer growth.

Figure 3.8 shows the increment of interfacial layer thickness of MOCVD HfAlO and HfO_2 samples before and after high temperature RTA at 950ºC, where the thickness of interfacial layer was measured using spectroellipsometry. While HfO_2 with surface nitridation (SN) shows the interfacial layer thickness increase of around 4.5 Å, HfAlO with surface nitridation has little change in interfacial layer thickness. This is attributed to retarded oxygen diffusion by incorporation of Al into HfO_2 [3.11]. In addition, the increment of interfacial layer shows little dependence on HfAlO deposition temperature. Therefore, 10% Al_2O_3 incorporation into the film is enough to prevent the oxygen diffusion through the high-K film. It is interesting to note that the Al_2O_3 composition ratio in MOCVD HfAlO film plays little role in the resistance to oxygen diffusion, unlike ALD HfAlO film.

It is well expected that the increment of interfacial layer may cause the increase of EOT of MOS capacitor with high-K film. The increment of EOT of HfO_2 due to the increment of interfacial layer is around 5 Å, which will be shown in Fig. 3.11 (b).

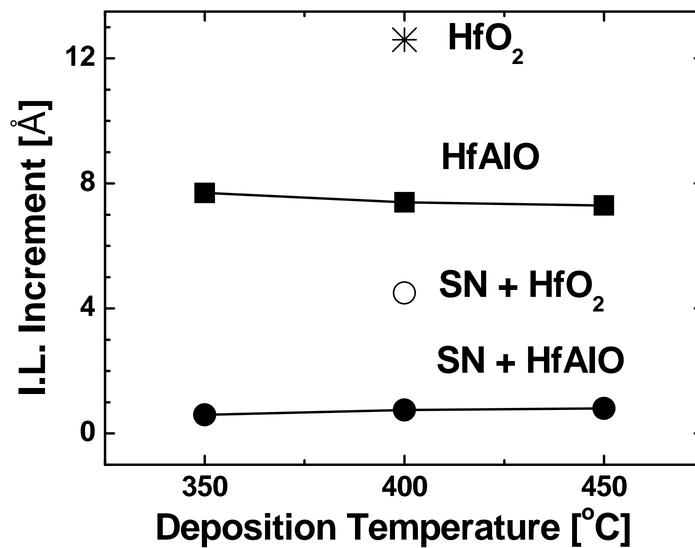


Fig. 3.8 Increment of interfacial layer (I.L.) of HfO_2 and HfAlO before and after high temperature RTA at 950ºC for 30 second. The thickness of I.L. was measured using spectroellipsometry. While HfO_2 with surface nitridation (SN) shows the interfacial layer increase of around 4.5 Å, HfAlO with SN has little change in interfacial layer thickness from the fact that the increase of I.L. is less than 1 Å.

3.3.5 MOS Capacitors with TaN/HfAlO Gate Stack

Figure 3.9 shows the C-V characteristics of HfO_2 and HfAlO films deposited at different temperatures. The frequency used for C-V measurement was 100 kHz. The flat-band voltages (V_{fb}) of all HfAlO samples slightly shift in positive direction due to incorporation of Al into HfO_2 but no strong dependence on HfAlO deposition temperature is observed. This result is somewhat different with other result obtained by ALD [3.21], which shows that flat-band voltage of HfAlO is strongly dependent on

the composition ratio. This weak dependence of flat-band voltage shift on composition ratio of HfAlO deposited by MOCVD will have an advantage in tighter threshold voltage (V_t) control of MOSFET compared to the case of HfAlO deposited by ALD.

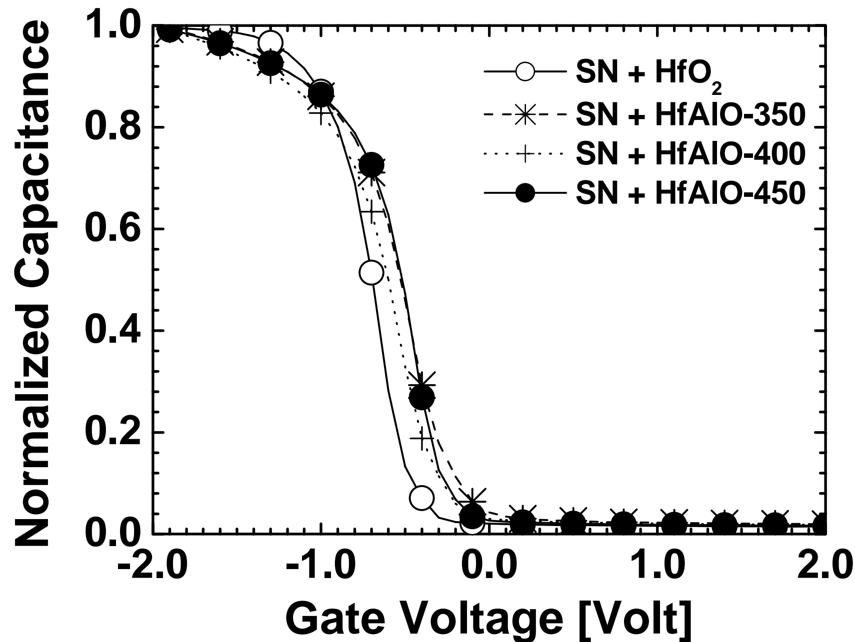
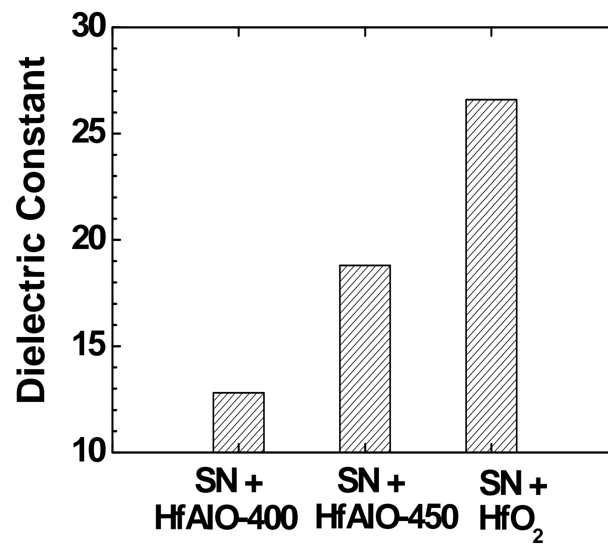


Fig. 3.9 Normalized C-V curves for HfO_2 and HfAlO films deposited at different temperature. The V_{fb} values of all HfAlO samples show slight positive shifts.

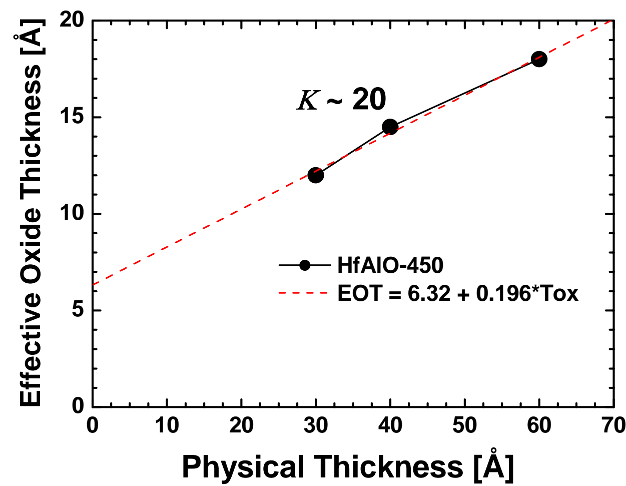
However, dielectric constant value exhibits a very strong dependence on composition ratio of HfAlO, as shown in Fig. 3.10 (a). The dielectric constant value was calculated from EOT and physical thickness of each HfAlO or HfO_2 samples. All samples had no additional RTA treatment after TaN deposition to minimize possible reaction with TaN gate electrode during high temperature process. As expected, higher amount of Al incorporation significantly decreases dielectric constant. HfAlO film deposited at 450ºC, which contains 10% of Al_2O_3, shows the dielectric constant of

19. However, the dielectric constant value is significantly reduced to 13 once the Al_2O_3 fraction is increased to 53%. This trend is well matched with the other result reported by L. Manchanda, *et al*., [3.13], which used the sputtered HfAlO.

The effect of subsequent high temperature process on the dielectric constant of the film is also investigated. HfAlO films deposited at 450°C with three different thicknesses of 30 Å, 40 Å, and 60 Å went through a high temperature RTA at 950°C for 30 sec. The K value extracted from the relationship between EOT and physical thickness is around 20, as shown in Fig. 3.10 (b), which is similar to that of HfAlO-450 in Fig. 3.10 (a). The result indicates that this acceptably high K value of HfAlO-450 is well maintained after high temperature RTA at 950ºC. The figure also shows the interfacial layer thickness is around 6 Å even after high temperature RTA. This thin interfacial layer is attributed to improved diffusion barrier properties against oxidant, which will be one of main advantages of HfAlO over HfO_2 for the application where very thin EOT is required.



(a)

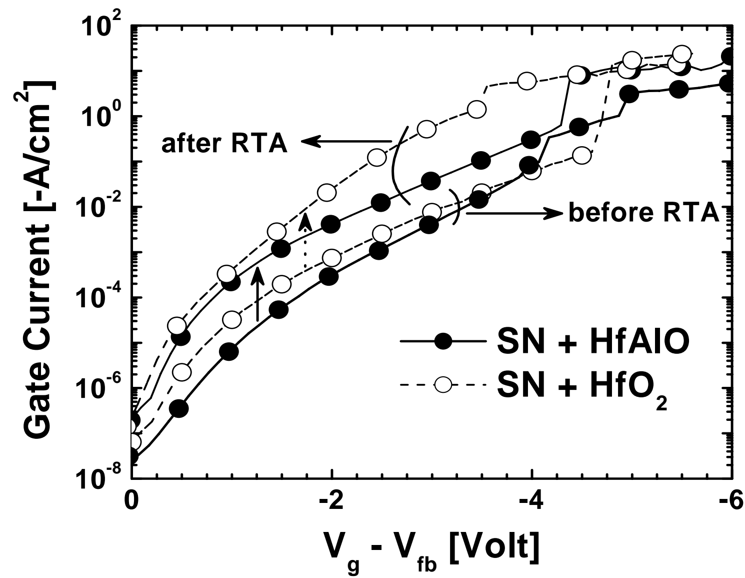


(b)

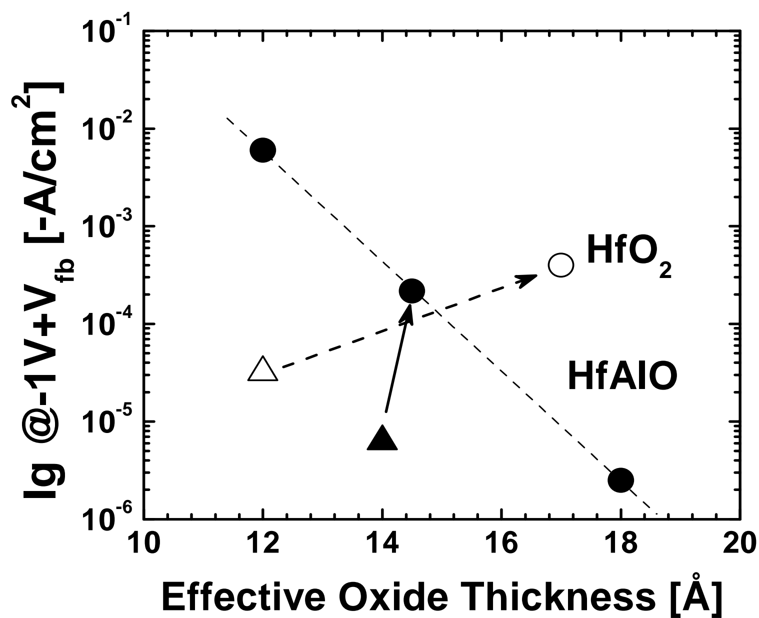
Fig. 3.10 **(a)** *K*-values of HfO_2 and HfAlO films. HfAlO deposited at 450ºC shows acceptable *K* value of 19. **(b)** Evaluation of K value of HfAlO-450 film after high temperature RTA at 950°C for 30 sec. The K value of around 20 is maintained after high temperature RTA.

Since the HfAlO deposited at 450ºC shows relatively high dielectric constant value and still shows similar level of thermal stability and electrical properties compared to other HfAlO samples with higher Al_2O_3 fraction, it can be regarded as the best condition in our work. The results in Figs. 3.11 – 3.13 were obtained from HfAlO films deposited at 450ºC. Fig. 3.11 (a) shows the leakage currents, before and after RTA at 950ºC for 30 sec, of HfO_2 and HfAlO with a thickness of around 40 Å. For both HfO_2 and HfAlO samples, the leakage currents increase after RTA. The reason for increment of leakage current is attributed to the formation or enlargement of grain boundary and/or defects such as pinhole. As can be seen, HfAlO shows lower leakage current for both before and after RTA compared to HfO_2 due to the improved thermal stability and larger band offset [3.9]. However, the leakage current difference at low voltages between HfO_2 and HfAlO after RTA looks to be not that much from the figure. The reason for relatively smaller difference in leakage current after RTA is due to the large increment of interfacial layer of HfO_2 sample, resulting in the increment of final EOT of HfO_2 which helps to lower the leakage current. Figure 3.11 (b) shows the trend more clearly. It shows leakage current versus EOT of HfAlO and HfO_2 before and after 950℃ RTA treatment. If the leakage currents of HfO_2 and HfAlO at the same EOT are compared, however, HfAlO shows much lower leakage current by around 2 orders of magnitude compared with HfO_2.

Thermal stability with top metal electrode was also investigated and the result is shown in Fig. 3.12. In this case, the RTA at 950ºC was done after the formation of TaN electrode. The pure HfO_2 shows tremendous increase in leakage current after RTA, which indicate that HfO_2 is degraded by the reaction of TaN during high temperature processing. On the contrary, HfAlO shows much smaller increase, which indicates better compatibility with TaN metal electrode relative to HfO_2.



(a)



(b)

Fig. 3.11 **(a)** Leakage currents of 40 Å HfAlO and HfO_2 before and after 950ºC RTA. RTA was done before the formation of TaN electrode. **(b)** I_g vs. EOT of HfAlO and HfO_2 before (▲,Δ) and after (●,○) 950ºC RTA treatment. Solid symbols represent the HfAlO and open symbols represent the HfO_2, respectively. The leakage current was measured at the gate voltage of –1V + V_{fb} (I_g@-1V+V_{fb}).

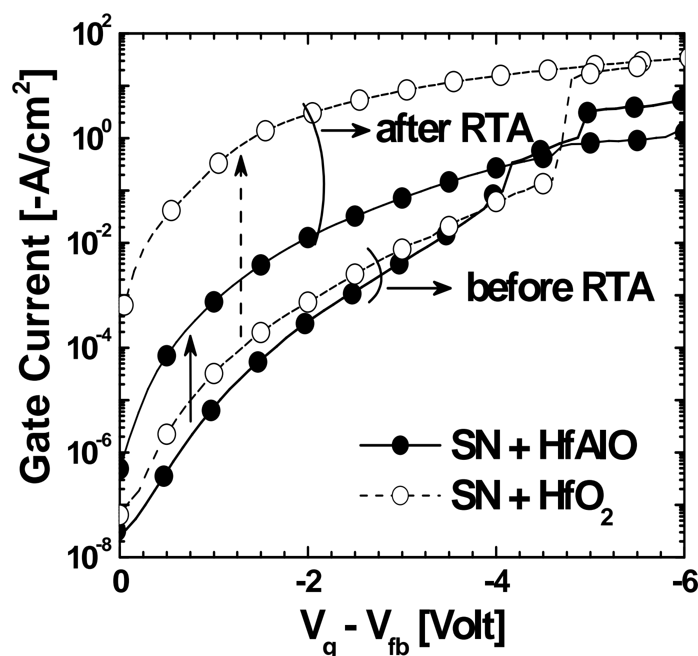


Fig. 3.12 Leakage currents of 40Å HfAlO and HfO_2 before and after 950ºC RTA. RTA was done after the formation of TaN electrode. HfAlO shows better compatibility with TaN gate electrode.

3.3.6 MOSFETs with TaN/HfAlO Gate Stack

NMOSFET's transconductance (G_m) and drain current (I_d) characteristics of HfAlO and HfO_2 with TaN gate electrode are shown in Fig. 3.13. The EOT values of HfAlO and HfO_2 are 17.0 Å and 17.5 Å, respectively. Drain saturation currents (at $V_g - V_t = 1.5$ V and $V_d = 1.5$ V) are 15.7 μA/μm and 27.6 μA/μm for HfO_2 gate device and HfAlO gate device, respectively. While the device with HfAlO gate dielectric shows the well-behaved G_m-V_g and I_d-V_g characteristics, the device with HfO_2 gate dielectric shows the degraded G_m-V_g and I_d-V_g characteristics due to the large gate leakage current possibly by the reaction with TaN electrode during source/drain implantation annealing step, as discussed in Fig. 3.12. This result indicates that the

compatibility of high-K gate dielectric with gate electrode is also important to achieve the well-behaved device performance.

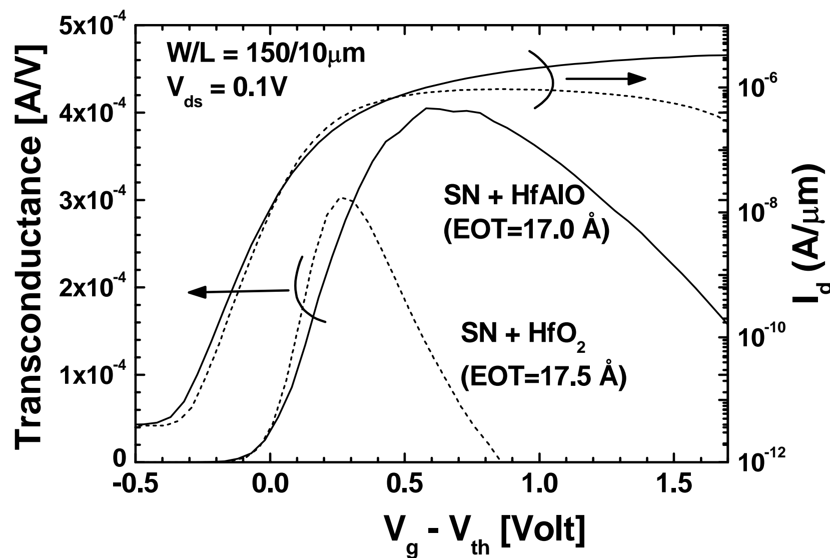


Fig. 3.13 Transconductance (G_m) and drain current (I_d) characteristics of TaN metal gate NMOSFETs with HfAlO (solid lines) or HfO_2 (dotted lines) gate dielectrics.

3.4 SUMMARY

It is demonstrated that a high quality MOCVD HfAlO dielectric film can successfully be deposited with a wide range of composition controllability between HfO_2 and Al_2O_3 in HfAlO using a single cocktail liquid source $HfAl(MMP)_2(OiPr)_5$. A composition ratio between 45 to 90 % of HfO_2 in HfAlO is achieved by controlling

deposition process parameters. It is found that the deposition temperature plays a major role in the composition ratio control. Higher temperature deposition introduces more hafnium into the film but there is a turn-around point of the composition ratio at the deposition temperature of 450ºC where the HfO_2 percentage is maximum of around 90% (Al_2O_3 10%). The effect of the composition ratio between HfO_2 and Al_2O_3 on the electrical properties of the film is also investigated. The HfAlO film with 90% HfO_2 (10% Al_2O_3), which has minimum sacrifice of K value (around 19), shows a great improvement in thermal stability and significant reduction of interfacial layer growth during subsequent thermal processes, leading to the reduction in leakage current by around 2 orders of magnitude compared to pure HfO_2 film. The HfAlO film also shows good compatibility with TaN metal gate electrode, under high temperature annealing process. In addition, the higher etch rate in DHF solution of HfAlO than that of HfO_2 owing to the improved thermal stability and lower degree of crystallization will give the clear advantage to HfAlO over HfO_2 for the implementation into a standard CMOS flow in terms of the complete removal of high-k dielectric on the active regions.

References

[3.1] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," in *IEDM Tech. Dig*., pp. 133-136, 1999.

[3.2] S. J. Lee, H. F. Luan, W. P. Bai, C.H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with Poly-Si gate electrode," in *IEDM Tech. Dig*., pp. 31-34, 2000.

[3.3] Y. Harada, M. Niwa, S. Lee, and D. L. Kwong, "Specific structural factors influencing on reliability of CVD-HfO_2," in *Symp. on VLSI Tech. Dig*., pp. 26-27, 2002.

[3.4] S. J. Lee, C. H. Lee, C. H. Choi, and D. L. Kwong, "Time-dependent dielectric breakdown in Poly-Si CVD HfO_2 gate stack," in *40th Annual International Reliability Physics Symposium*, pp. 409-412, 2002.

[3.5] P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, and J. G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)", *J. Appl. Phys.*, vol 91, pp. 4353-4363, April 2002.

[3.6] B. Tavel, X. Garros, T. Skotnicki, *et al.*, "High performance 40 nm nMOSFETs with HfO_2 gate dielectric and polysilicon damascene gate", in *IEDM Tech. Dig*., pp. 429-432, 2002.

[3.7] W. Zhu, T. P. Ma, T. Tamagawa, and Y. Di, "HfO_2 and HfAlO for CMOS: Thermal stability and current transport," in *IEDM Tech. Dig*., pp. 463-466, 2001.

[3.8] C. H. Choi, S. J. Rhee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong, "Thermally stable CVD HfOxNy Advanced Gate Dielectrics with Poly-Si Gate Electrode" in *IEDM Tech. Dig*., pp. pp. 857-860, 2002.

[3.9] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D. L. Kwong, J. S. Oan, C. H. Ang, J.Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO2)_x(Al2O3)_{1-x}$ on (100) Si," *Applied Physics Letters,* vol 81, pp. 376-378, 2002.

[3.10] J. H. Lee, Y. S. Kim, H. S. Jung, J. H. Lee, N. I. Lee, H. K. Kang, J. H. Ku, H. S. Kang, Y. K. Kim, K. H. Cho, and K. P.Suh, "Poly-Si gate CMOSFETs with HfO_2-Al_2O_3 laminate gate dielectric for low power applications," in *Symp. on VLSI Tech. Dig*., pp. 84-85 , 2002.

[3.11] H. Y. Yu, N. Wu, M. F. Li, C. X. Zhu, B. J. Cho, D. L. Kwong, C. H. Tung, J. S. Pan, J. W. Chai, W. D. Wang, D. Z. Chi, C. H. Ang, J. Z. Zheng, "Thermal Stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si," *Applied Physics Letters*, vol 81, pp. 3618-3620, 2002.

[3.12] G. D. Wilk, M. L. Green, M. –Y. Ho, B. W. Busch, T. W. Sorsch, F. P. Klemens, B. Brijs, R. B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, J. M. Hergenrother, "Improved film growth and flatband voltage control of ALD HfO_2 and Hf-Al-O with n+poly-Si gates using chemical oxides and optimized post-annealing," in *Symp. on VLSI Tech. Dig*., pp. 88-89, 2002.

[3.13] L. Manchanda, M. D. Morris, M. L. Green, R. B. van Dover, F. Klemens, T. W. Sorsch, P. J. Silverman, G. Wilk, B. Busch, S. Aravamudhan, "Multi-

component high-*K* gate dielectrics for the silicon industry," *Microelectronic Engineering*, vol 59, pp. 351-359, 2001.

[3.14] S. Horri, M. Asai, H. Miya, K. Yamamoto, and M. Niwa, "Improvement of electrical properties for high-k dielectrics grown by MOCVD via cyclic remote plasma oxidation" in *Extended Abstracts of SSDM 2002*, pp. 172-173, 2002.

[3.15] R. Choi, C. S. Chang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan and J. C. Lee, "High quality ultra-thin HfO_2 gate dielectric MOSFETs with TaN electrode and nitridation surface preparation," in *Symp. on VLSI Tech. Dig*., pp. 15-16, 2001.

[3.16] C. A. Richter, A. R. Hefner, and E. M. Vogel, "A comparison of Quantum-Mechanical Capacitance-Voltage Simulators", *IEEE Electron Device Letters*, vol 22, pp. 35-37, 2001.

[3.17] J. J. Chamber, A. L. P. Rotondaro, M. J. Bevan, M. R. Visokay, and L. Colombo, "Effect of composition and post-deposition annealing on the etch rate of hafnium and zirconium silicates in diluted HF," in *2001 ECS/ISE Joint Meeting*, Abst. #1434, 2001.

[3.18] J. Chen, W. J. Yoo, D. S. H. Chan, and D.-L. Kwong, "Effects of annealing and Ar ion bombardment on the removal of HfO_2 gate dielectric", *Electrochemical and Solid-State Letters*, vol 7, pp. F18-F20, 2004.

[3.19] C. C. Yeo, M. S. Joo, B. J. Cho, and S. J. Whang, "Effects of annealing on the composition and structure of HfO_2 and nitrogen-incorporated HfO_2", *Thin Solid Films*, vol 462-463, pp. 90-95, 2004.

[3.20] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “Hafnium and zirconium silicates for advanced gate dielectrics,” *J. Appl. Phys.,* vol 87, pp. 484-492, 2000.

[3.21] M. S. Joo, B. J. Cho, C. C. Yeo, N. Wu, H. Y. Yu, C. X. Zhu, M. F. Li, D. -L. Kwong, N. Balasubramanian, “Dependence of Chemical Composition Ratio on Electrical Properties of HfO_2-Al_2O_3 Gate Dielectric,” *Jpn. J. Applied Physics,* vol 42, pp. L220-L222, 2003.

CHAPTER 4

THERMAL INSTABILITY OF EFFECTIVE WORK FUNCTION IN METAL/HIGH-K STACK AND ITS MATERIAL DEPENDENCE

4.1 INTRODUCTION

Aggressive scaling of CMOS devices requires the metal gate electrode on high-K dielectrics for nanoscale CMOS devices because of low gate leakage current and poly-depletion-free feature. In selecting metal gate materials for device integration, the effective work functions ($\Phi_{m,eff}$) of metal gates is an important consideration because it directly affects the threshold voltage and the performance of a transistor. However, the $\Phi_{m,eff}$ values of metal gates on gate dielectrics are reported to be different from their vacuum work functions ($\Phi_{m,vac}$) and dependent on the underlying gate dielectric [4.1]. This phenomenon was explained either by metal-induced gap states (MIGS) theory [4.1]-[4.4] or by chemical bonding theory [4.5]-[4.7]. In MIGS theory, charging of interface states at the metal/dielectric interface creates a dipole that tends to drive the band lineup toward a position that would give zero dipole charge. For pure metals which have not experienced high temperature thermal processes, the experimental data appear to be in good agreement with the MIGS theory [4.1].

However, the behavior of $\Phi_{m,eff}$ of metal nitrides on high-K dielectric, which is a promising gate stack structure for near future CMOS device, has still been poorly understood, especially under high temperature thermal processes which are required for actual CMOS device fabrication.

In this chapter, the new findings on the thermal instability of $\Phi_{m,eff}$ of metal/high-K stack and its material dependence will be discussed and a model to explain the phenomenon of the thermal instability of $\Phi_{m,eff}$ and its material dependence will be proposed.

4.2 THEORETICAL BACKGROUND OF METAL-DIELECTRIC INTERFACE

4.2.1 METAL-SEMICONDUCTOR INTERFACE

The requirement that Fermi levels match up results in potential barrier to charge transfer between a metal and a semiconductor. Such a barrier, commonly referred to as a Schottky barrier, arises because the work functions of the metal and the semiconductor are different. Ideally we can calculate the difference and predict the behaviour of the metal on a semiconductor structure. When there is no charge transfer across the metal-semiconductor interface, the Schottky barrier height for the electrons (Φ_{Bn}) is given by the difference between the work function of the metal in vacuum ($\Phi_{m,vac}$) and the electron affinity of the semiconductor (χ_s), that is,

$$\Phi_{Bn} = \Phi_{m,\,vac} - \chi_s \,. \qquad (4\text{-}1)$$

However, it has been observed experimentally that Eq. (4-1) is not generally obeyed. Bardeen proposed a Surface State model to explain this observation [4.8]. Bardeen's model postulates a high density of surface states of the order of 1 per surface atom at a well-defined energy relative to the conduction band edge of the semiconductor, and these states act to pin the metal Fermi-level. However, later Heine pointed out that the high density of surface states did not exist in the fundamental gap for most metal-semiconductor interfaces and suggested another model, the virtual gap states model [4.9], to explain that observation, which will be discussed in detail in Section 4.2.2.

4.2.2 INTRINSIC STATES OR METAL-INDUCED GAP STATES (MIGS) OF METAL-SEMICONDUCTOR INTERFACE

The virtual gap states (VGS) model, which was introduced by Heine [4.9], assumes that within the band gap of the semiconductor the wave functions of the metal electrons are tailing into the virtual gap states of the complex band structure of the semiconductor. Later, these states in the band gap have been called as metal-induced gap states (MIGS) or simply intrinsic states [4.1],[4.2]. Recently, using electron energy loss spectroscopy (EELS), MIGS have been experimentally observed by Muller *et al.* for MgO/Cu interfaces [4.10].

The continua of MIGS have branch points where the character of these states changes from mostly valance-band- or donorlike to predominantly conduction-band- or acceptorlike. If the Fermi level is above, coincide with, and drops to below the branch point, the net charge density in interface-induced gap states is negative, vanishes, and becomes positive, respectively. Therefore, these branch points are intuitively called

the charge neutrality levels (CNL) of the MIGS [4.11]. The CNL is like a Fermi level for interface states; it is the energy near midgap to which the interface states are filled in a neutral surface. Charge transfer generally occurs across the interface due to the presence of intrinsic interface states. Charging of these interface states creates a dipole that tends to drive the band lineup toward a position that would give zero dipole charge.

Figure 4.1 illustrates the distribution of MIGS at the metal-dielectric interface and charging character of interface state for the case where the Fermi level ($E_{F,m}$) is above the charge neutrality level in the dielectric ($E_{CNL,d}$). For this case, a negatively charged dipole is created on the dielectric side. This interface dipole drives the band alignment so that $E_{F,m}$ goes toward $E_{CNL,d}$, and hence the $\Phi_{m,eff}$ value would differ from the $\Phi_{m,vac}$ value. The work function change is proportional to the difference between $\Phi_{m,vac}$ and $\Phi_{CNL,d}$ [$=(E_{vac}-E_{CNL,d})/q$] and the relationship between $\Phi_{m,eff}$ and $\Phi_{m,vac}$ is given by the following equation [4.1],

$$\Phi_{m,eff} = \Phi_{CNL,d} + S(\Phi_{m,vac} - \Phi_{CNL,d}) . \quad (4\text{-}2)$$

The parameter S in Eq. (4-2) is a slope parameter or dimensionless pinning factor, which describes if the barrier is “pinned” or not. S varies between the limits S=1 for unpinned Schottky barrier, to S=0 for Bardeen barriers, which are pinned by a high density of interface states. Materials with a smaller S tend to pin the metal Fermi level more effectively to $E_{CNL,d}$. It is now known that S depends on the electronics part of the dielectric constant ε_∞ [4.11],[4.12], which can be obtained using the experimental value of refractive index, $\varepsilon_\infty=n^2$ [4.3]. The slope parameter S obeys an empirical relationship given by

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}. \tag{4-3}$$

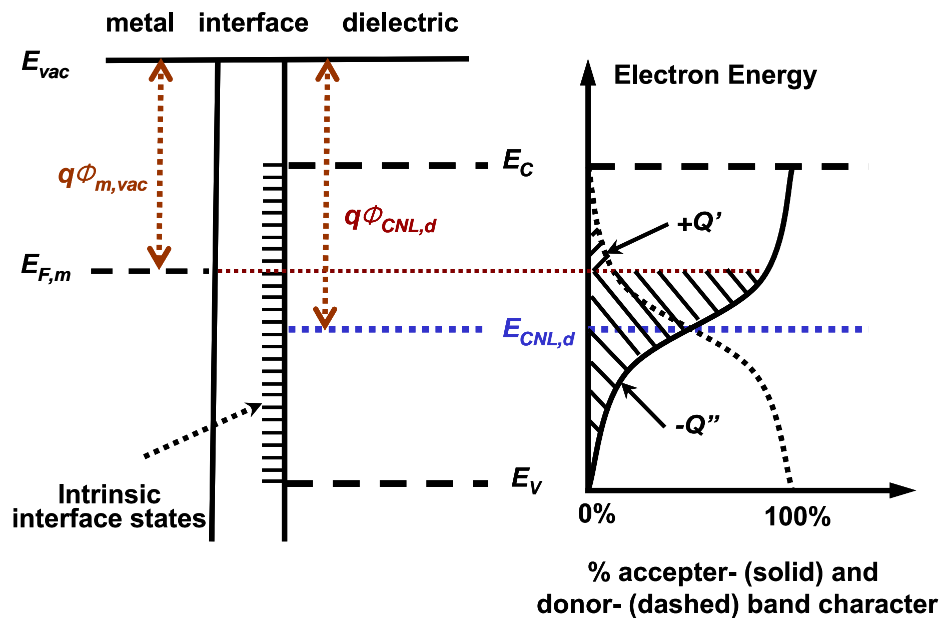


Fig. 4.1 Energy band diagram (left) and charging character of interface states (right) for the metal-dielectric interface, where the Fermi level ($E_{F,m}$) is above the charge neutrality level in the dielectric ($E_{CNL,d}$). In general, the character of interface states becomes more acceptor- (donor-) like toward the conduction (valence) band, as indicated by the solid (dashed) line.

4.2.3 Extrinsic States of Metal- or Polysilicon-Semiconductor Interface

The MIGS model which explains the dependence of $\Phi_{m,eff}$ on gate dielectric material has been particularly successful for metal-dielectric interfaces where there is minimal interaction or where intrinsic states or MIGS dominate. In addition, this model can be applicable for the interface of the heavily doped polysilicon and gate dielectric where there is minimal interaction between polysilicon and gate dielectric.

However, in addition to the dependency on the gate dielectric material, the metal gate work function has been observed to be dependent on process conditions. Schaeffer *et al.* [4.13] have reported that the work functions of the TaN, TaSi, and TaSiN metal gates on HfO_2 change with post-gate anneal. A larger work function shift is observed when the thermal budget is increased. It is postulated that the reaction at the metal-dielectric interface could cause the aforementioned variations. Interfacial reaction or formation of extrinsic states can manifest as thermal instability of work function or the threshold voltage of transistor. In addition, extrinsic states at the metal-dielectric interface or polysilicon-dielectric interface could drive Fermi-level pinning and convergence of work function to a pinning level.

Recently, a serious problem has emerged in field effect transistors (FETs) with HfO_2 gate oxide and polysilicon gate electrodes, where large shifts in the gate threshold voltages are seen compared to their values in FETs with SiO_2 [4.14]. For HfO_2 layers on 2.3 nm of underlying thermal SiO_2 oxide, it is observed the flat-band voltages (V_{fb}) are shifted by about +0.2 V and -0.5 V compared to those of SiO_2 for n-doped polysilicon and p-doped polysilicon gates, respectively. These values can be converted into an energy band diagram as shown in Fig. 4.2. In this diagram, doped polysilicon on SiO_2 is able to move the Fermi level up to the Si conduction band (CB) edge and down to the valence band (VB) edge, but on an increasingly thick layer of HfO_2 it can only move E_F to within 0.2 eV of CB and down to 0.5 eV of VB. This inability to fully shift the Fermi level across the Si gap has been attributed to a “pinning” of the Fermi-level at the oxide polysilicon interface [4.15]. This effect has now been reproduced by various groups [4.16]-[4.19] and it has been generally concluded that the effect is due to Si-Hf bond formation by the interaction between the

polysilicon and the HfO_2 layer causing a Fermi-level pinning at the energy at ~0.3 eV below CB.

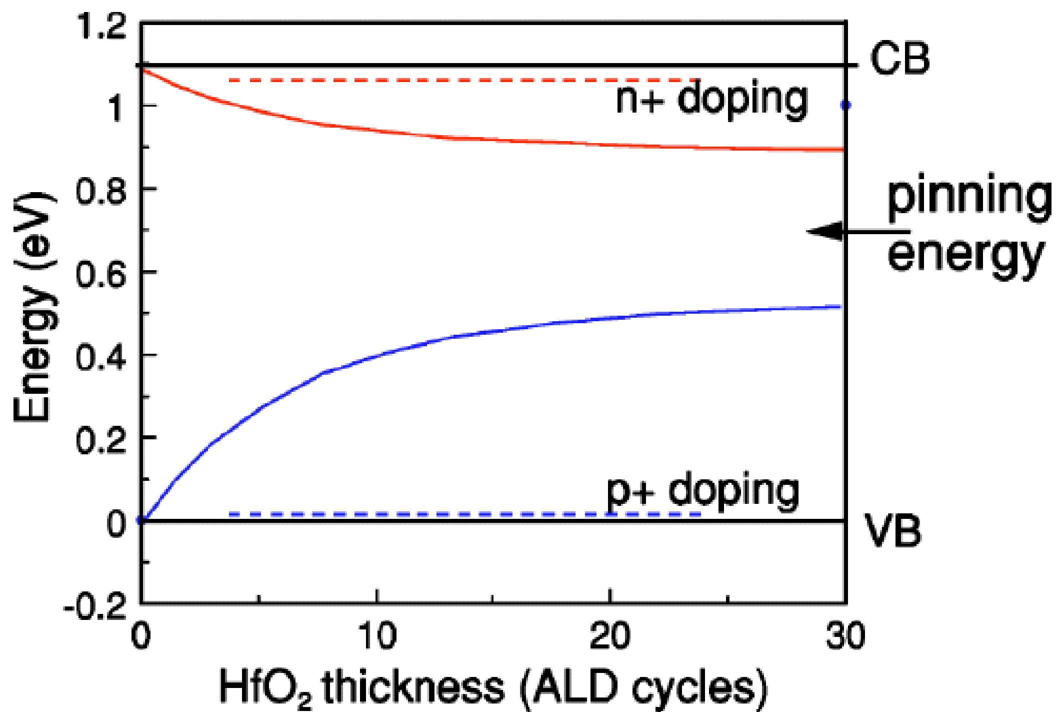


Fig. 4.2 Change of flat-band potential vs HfO_2 film thickness, showing tendency for potentials to converge around 0.3 eV below CB edge [4.15].

4.3 EXPERIMENTAL

The fabrication of metal-oxide-silicon (MOS) capacitors started with field oxide isolation on p-type Si (100) substrate (4-8 Ω cm resistivity) and active region patterning. MOCVD HfAlO dielectric films [4.20] with physical thicknesses of 40

~90 Å were deposited on the DHF-cleaned Si-substrate, followed by post deposition annealing (PDA) at 700ºC for 1 min. The details of film fabrication can be found in Chapter 3. Three metal nitride electrodes, HfN, TaN, and TaSiN, were deposited for gate electrode using reactive sputtering. To prevent the possible oxidant diffusion through a gate electrode during high temperature thermal process, HfN/TaN stack was deposited as a capping layer using reactive sputtering [4.21]. For thermal stability study of $\Phi_{m,eff}$, rapid-thermal-annealing's (RTA's) at 700 ~ 950ºC for 30 sec were done after gate pattering in a N_2 ambient. Post metallization annealing (PMA) in a forming gas ambient (N_2/H_2) at 420℃ was done to all devices.

The capacitance versus voltage (C-V) measurements was conducted using HP 4284A precision LCR meter analyzer for MOS capacitors. The frequency used for C-V measurement was 100 kHz. The equivalent oxide thickness (EOT) was extracted using simulation program taking quantum mechanical effect into consideration. The V_{fb} value of each sample is calculated from the comparison of its C-V curve with simulated C-V curve. The $\Phi_{m,eff}$ values of metal gates on gate dielectric were extracted from plots of V_{fb} versus the EOT of gate dielectric. X-ray photoelectron spectroscopy (XPS) analysis was performed to confirm the Si incorporation into the HfAlO.

4.4 RESULTS AND DISCUSSION

4.4.1 INTRINSIC PROPERTIES OF METAL/HIGH-K STACK

Figure 4.3 shows a plot of V_{fb} versus EOT for three different metal nitrides of HfN, TaN, and TaSiN on HfAlO dielectric before high temperature RTA. All lines are parallel, indicating that initial charges in HfAlO are the same for all three electrodes. The $\Phi_{m,eff}$ value for each metal nitride was calculated using the intercept of its extrapolated line with *y*-axis. Figure 4.4 shows $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ for several metals on HfAlO, HfO_2, and SiO_2. The $\Phi_{m,eff}$ value of each metal gate on gate dielectric was also extracted from plots of V_{fb} versus the EOT of gate dielectric. The experimental slope parameter S and the charge neutrality level Φ_{CNL} of each dielectric can be estimated from values of the gradient and *y*-axis intercept of each line in Fig. 4.4 and Eq. 4.2, respectively. S and Φ_{CNL} values of each dielectric are summarized in Table 1. S and Φ_{CNL} values of HfAlO film are 0.77 and 4.8 eV, respectively, and lie in between those of SiO_2 and HfO_2, which indicates weaker Fermi-level pinning compared to HfO_2. The values obtained are comparable to the theoretical ones predicted by metal-induced gap states (MIGS) theory [4.1]-[4.4]. These values were obtained from the samples without any high temperature process except PMA, which therefore can be considered as an intrinsic property of the materials. However, in actual CMOS devices which require high temperature annealings in the fabrication procedure, these values are not applicable in prediction of V_t because of thermal instability of $\Phi_{m,eff}$ on high-K. The behavior of $\Phi_{m,eff}$ of metal nitrides on HfAlO after annealing will be discussed in Section 4.4.2.

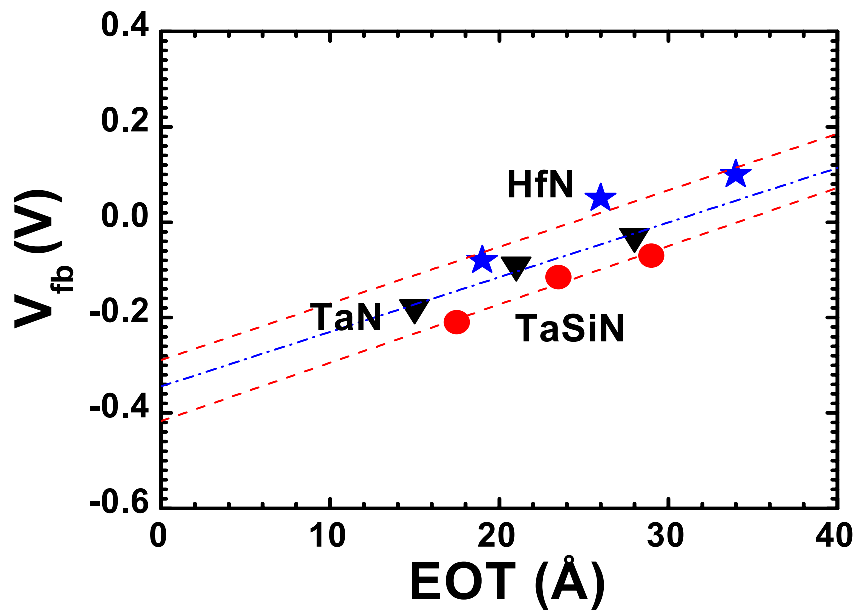


Fig. 4.3 V_{fb} versus EOT for HfAlO film under three metal nitrides. Initial charges in HfAlO films are the same for three different metal electrodes.

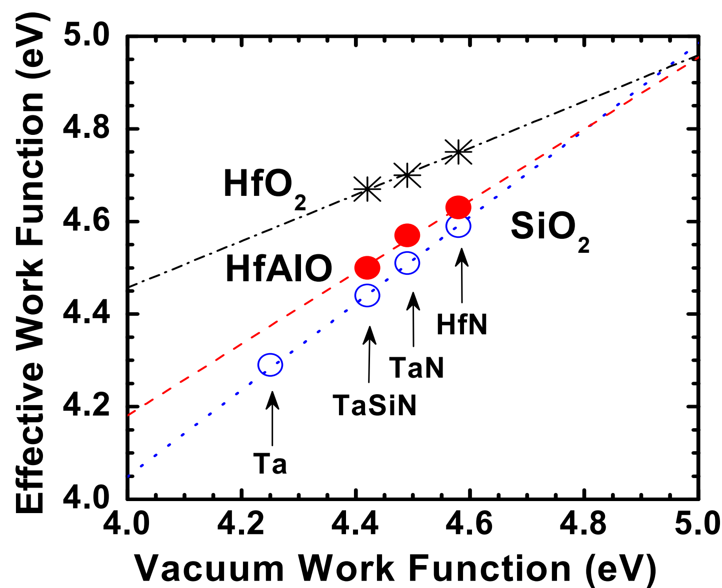


Fig. 4.4 $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ for various gate dielectrics. HfAlO and HfO_2 show higher $\Phi_{m,eff}$ values than SiO_2 does.

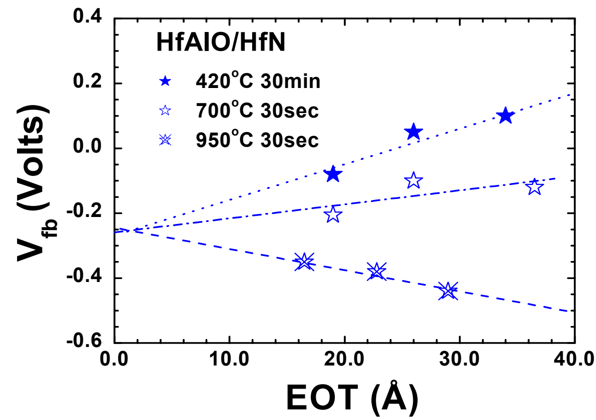
Table 4.1 Comparison of theoretical and experimental slope parameter *S* and $\Phi_{CNL,d}$ under three metal nitride gate electrodes.

Dielectric	$\Phi_{CNL,d}$ (eV)	S (This work)	S (MIGS)
SiO_2	4.7	0.95[a]	0.86
HfO_2	4.9	0.50	0.53
HfAlO	4.8	0.77	0.63

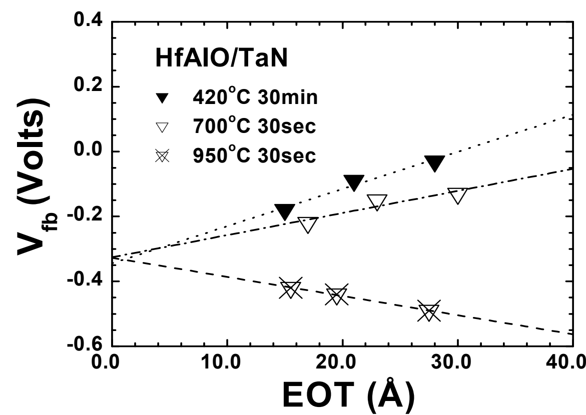
[a]Taken from Ref.[4.1]

4.4.2 THERMAL INSTABILITY OF EFFECTIVE WORK FUNCTION

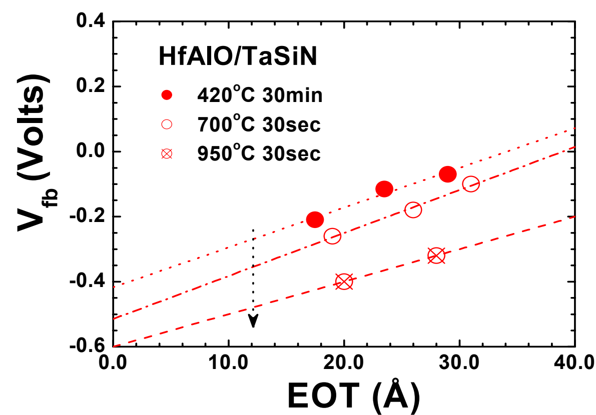
Figure 4.5 shows the V_{fb} of MOS capacitor versus EOT for the gate stacks with three different metal nitrides on HfAlON after high temperature RTA. The RTA process was done at 700℃ and 950℃ for 30 sec. For HfN and TaN on HfAlO, the charge in the HfAlO changes from negative to positive as the annealing temperature increases, but the extrapolated lines are merging to almost a single point, indicating that there is no obvious change in $\Phi_{m,eff}$ as shown in Figs. 4.5 (a) and (b). For TaSiN, however, the dielectric charges are maintained almost the same but intercept value $\Phi_{m,eff}$ significantly decreases towards E_C level of silicon as the annealing temperature increases as shown in Fig. 4.5 (c). These results indicate that $\Phi_{m,eff}$ are strongly depending on electrode materials.



(a)



(b)

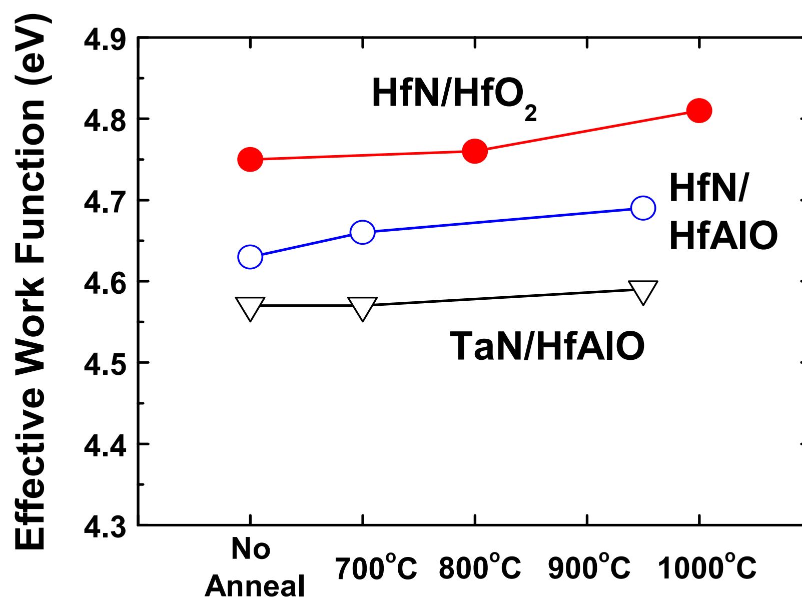


(c)

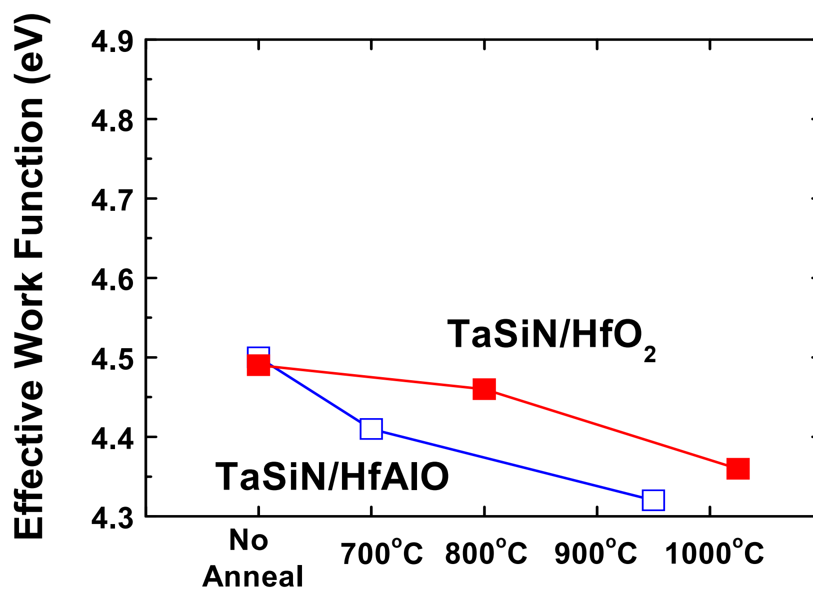
Fig. 4.5 V_{fb} versus EOT for (a) HfN, (b) TaN and (c) TaSiN on HfAlO after annealing at different temperatures. Both HfN and TaN show the change of dielectric charge whereas TaSiN on HfAlO shows the change of work function after high temperature anneal.

Figure 4.6 shows the behaviors of $\Phi_{m,eff}$ of several metal nitrides on two kinds of high-K dielectric, including HfAlO and HfO_2 after high temperature RTA. Data for TaSiN/HfO_2 and HfN/HfO_2 were taken from Ref. [4.13] and [4.21], respectively. In Fig. 4.6 (a), HfN and TaN on high-K dielectric show no obvious modification of $\Phi_{m,eff}$ after high temperature RTA. On the contrary, $\Phi_{m,eff}$ of TaSiN on high-K dielectric is significantly changed approaching towards E_C level of silicon as the annealing temperature increases as shown in Fig. 4.6 (b). Because of this strong dependence of $\Phi_{m,eff}$ on electrode materials after annealing, the data points in the plot of $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ do not fall on a straight line for both 700℃ RTA and 950℃ RTA cases as shown in Fig. 4.7. This result indicates that MIGS theory with intrinsic interface states is not applicable after annealing. This is believed to be due to the generation of substantial amount of extrinsic interface states at the metal/dielectric interface.

The modification of $\Phi_{m,eff}$ after annealing is found not only on high-K but also on SiO_2, too. Figure 4.8 shows the behaviors of $\Phi_{m,eff}$ of several metal nitrides on SiO_2 after high temperature RTA. Data for TaN/SiO_2 were taken from Ref. [4.22]. The $\Phi_{m,eff}$ values are increasing with RTA temperature, which is the opposite trend to the case of TaSiN on HfAlO.



(a)



(b)

Fig. 4.6 The behavior of $\Phi_{m,eff}$ before and after high temperature RTA at several temperatures for the gate stacks of (a) HfN or TaN on high-K dielectric (b) TaSiN on high-K dielectric.

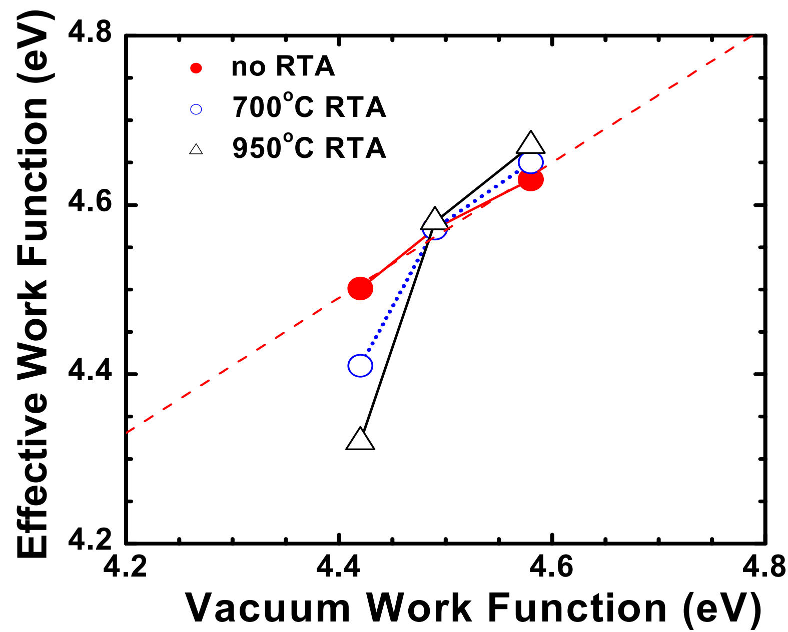


Fig. 4.7 $\Phi_{m,eff}$ versus $\Phi_{m,vac}$ on HfAlO after annealing at different temperatures. The result indicates that MIGS theory with intrinsic interface states is not applicable after annealing.

.

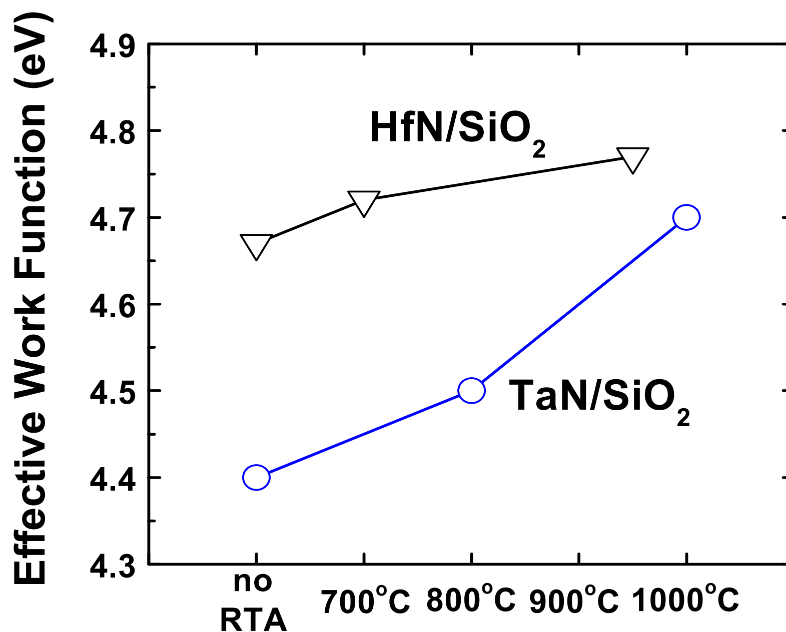


Fig. 4.8 The behavior of $\Phi_{m,eff}$ before and after high temperature RTA at several temperatures for the gate stacks of metal nitride on pure silicon dioxide stacks.

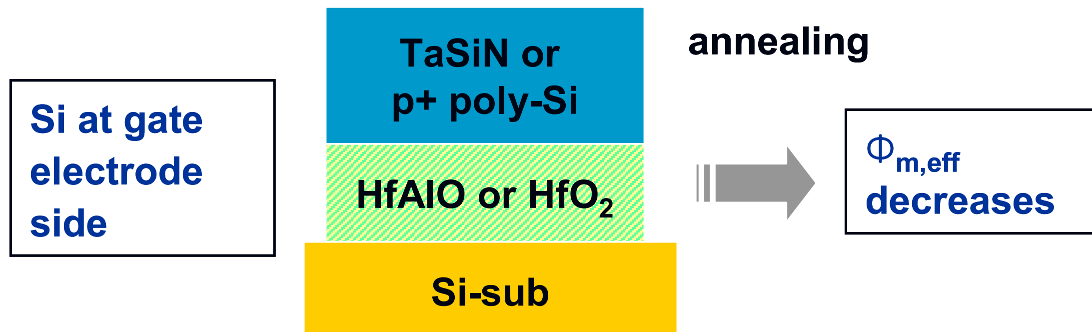
4.4.3 OBSERVED PHENOMENON

A very interesting phenomenon can be found if the data in Fig. 4.5-4.8 in Section 4.4.2 are carefully examined. The modification of $\Phi_{m,eff}$ by annealing is obvious when "silicon" is present at the metal/dielectric interface, no matter where silicon is, either in dielectric or in gate material. But the direction of $\Phi_{m,eff}$ change seems to be depending on the location of silicon. Figure 4.9 illustrates the observed phenomena in the modification of $\Phi_{m,eff}$ of gate stacks in three different combinations of metal nitride/gate dielectric stacks after high temperature annealing.

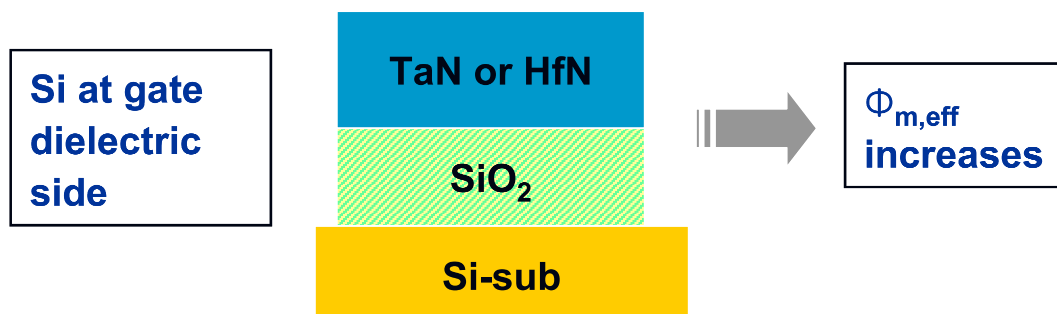
In the combination (I), silicon is present at the gate electrode side (in the case of TaSiN/HfO_2 and TaSiN/HfAlO stacks) and $\Phi_{m,eff}$ values are decreasing with annealing temperature and finally merged to 4.3 ~ 4.4 eV as shown in Fig. 4.6 (b). The similar trend, where the Fermi level is pinned near E_C, was also reported in polysilicon/HfO_2 stack [4.14], which can be considered as an example of the above mentioned case, as silicon is present at the gate electrode side and the device underwent high temperature process for dopant activation in polysilicon.

On the contrary, silicon is present at dielectric side (in the case of HfN/SiO_2 and TaN/SiO_2 stacks) in the combination (II) and $\Phi_{m,eff}$ values are increasing with annealing temperature and finally merged to 4.7 ~ 4.8 eV as shown in Fig. 4.8. However, for the case combination (III) of no silicon at the interface (in the case of HfN/HfO_2, HfN/HfAlO and TaN/HfAlO stacks), there is no obvious modification of $\Phi_{m,eff}$ after annealing as shown in Fig. 4.6 (a).

Combination (I)



Combination (II)



Combination (III)

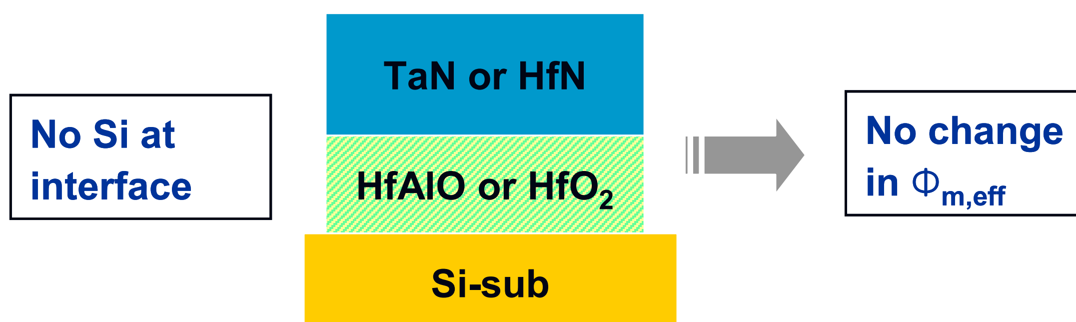
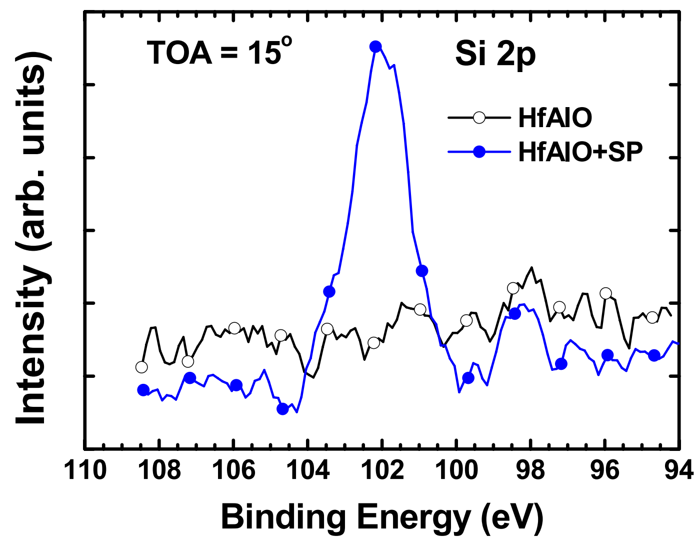


Fig. 4.9 Observed phenomena in the modification of $\Phi_{m,eff}$ of gate stacks in three different combinations of metal nitride/gate dielectric stacks after high temperature annealing. It is observed that the modification of $\Phi_{m,eff}$ after annealing happens only when "silicon" is present at the metal/dielectric interface.

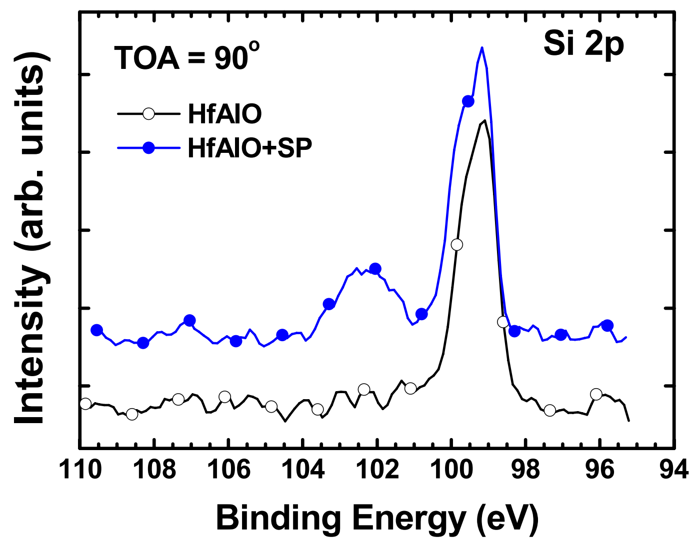
4.4.4 FURTHER CONFIRMATION ON THE EFFECT OF SI

In order to have further confirmation on the effect of silicon on the thermal behaviors of $\Phi_{m,eff}$, silicon atoms are intentionally incorporated at the interface of TaN/HfAlO stack and the behavior of $\Phi_{m,eff}$ is monitored after annealing. Silicon incorporation onto the top surface of HfAlO was implemented by silicon passivation (SP) technique [4.23] using SiH_4 gas flow. After deposition of HfAlO, the wafers were transferred to a constant-temperature process chamber without breaking the vacuum and subjected to SP treatment in SiH_4+N_2 ambient at 5 Torr at 450ºC for 1 minute. The silicon incorporation into HfAlO was confirmed by XPS analysis as shown in Fig. 4.10, which shows Si 2p core-level spectra at two different take-off angles of (a) 5° and (b) 90°, respectively. Compared to HfAlO without SP (HfAlO), Si-passivated HfAlO sample (HfAlO+SP) shows strong peak at around 102.3 eV, which indicates Hf silicate bond (Hf-O-Si) [4.24].

Figure 4.11 shows the behavior of $\Phi_{m,eff}$ of TaN/silicon-passivated HfAlO stack after annealing. The $\Phi_{m,eff}$ obviously increases after annealing, which is not observed in TaN/HfAlO without SP. The $\Phi_{m,eff}$ value is merged to around 4.8 eV, similar to the cases of HfN/SiO_2 and TaN/SiO_2 stacks. This result clearly verifies the role of silicon to the instability of $\Phi_{m,eff}$ during high temperature annealing.



(a)



(b)

Fig. 4.10 Si 2p core-level spectra at two different take-off angles of (a) 15° and (b) 90°. Compared to HfAlO without SP, Si-passivated HfAlO sample shows strong peak at around 102.3 eV, which indicates Hf silicate bond (Hf-O-Si).

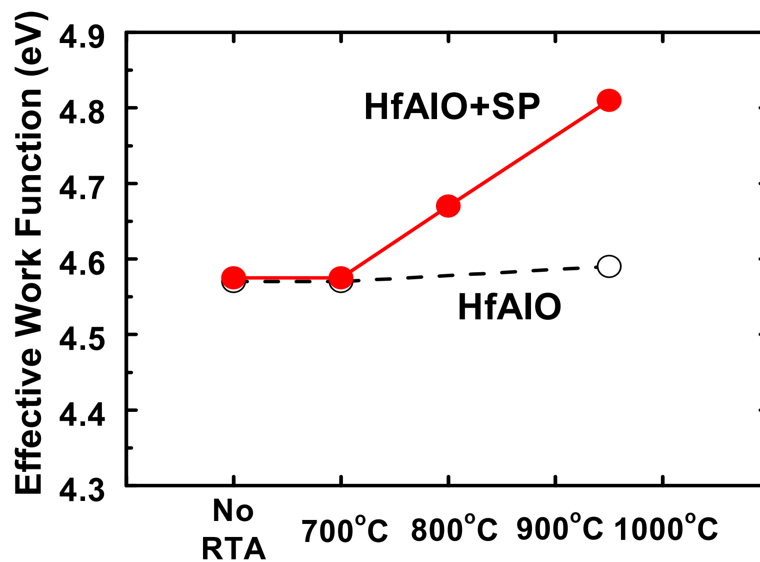
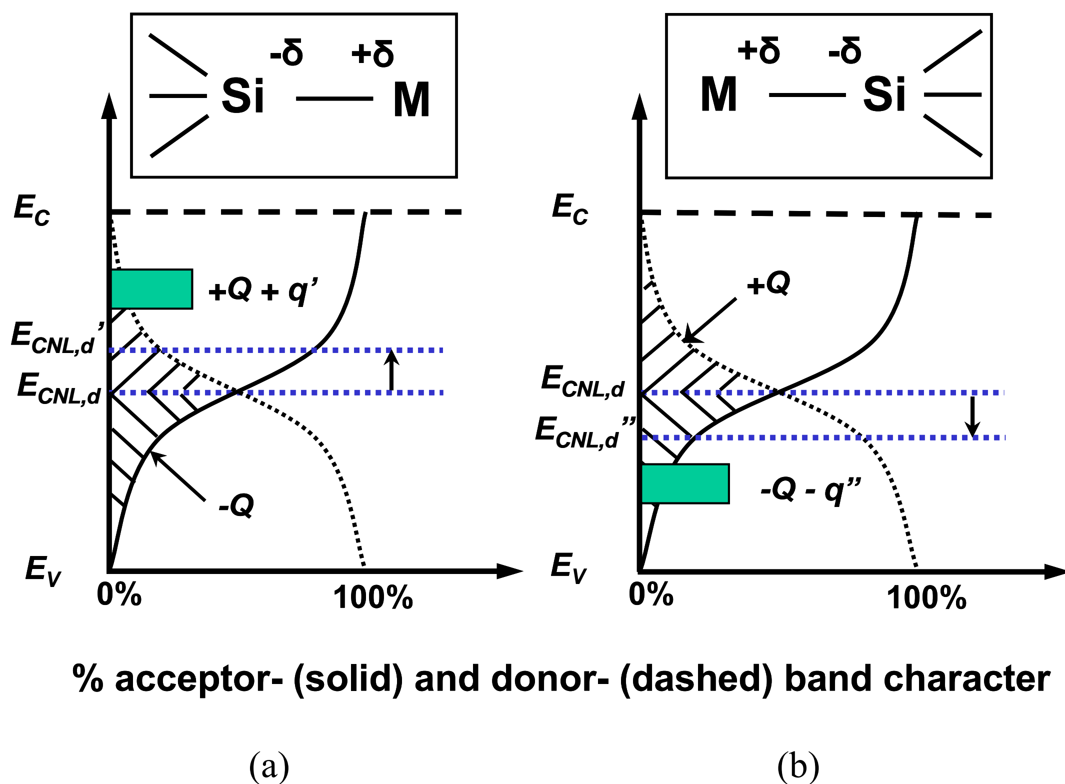


Fig. 4.11 Thermal instability of $\Phi_{m,eff}$ of HfAlO sample with SP. $\Phi_{m,eff}$ value approaches around 4.8 eV as RTA temperature increases.

4.4.5 Proposed Model

Figure 4.12 shows a schematic drawing which illustrates how silicon incorporation at the metal/dielectric interface affects thermal instability of $\Phi_{m,eff}$. In the figure, $E_{CNL,d}$ denotes the charge neutrality level of the dielectric taking account of the intrinsic interface states. However, the presence of silicon at the interface induces additional interface states which can be called extrinsic interface states. When silicon is at the electrode side, Si-Metal (Metallic element in high-K dielectric) bonds generate the additional dipoles. From the fact that the electronegativity of silicon atom is larger than that of Hf atom used in this experiment (1.9 *vs.* 1.3) [4.25], these dipoles are positively charged at the dielectric side and the extrinsic interface states should be donor-like, located near E_C as illustrated in Fig. 4.12 (a). These additional donor-like

interface states result in a shift of $E_{CNL,d}$ toward E_C, causing the decrease of $\Phi_{m,eff}$. On the contrary, when silicon is at the dielectric side, Metal-Si bonds induce the negative dipoles which generate the acceptor-like extrinsic interface states located near E_V. This causes a shift of $E_{CNL,d}$ toward to E_V and increases $\Phi_{m,eff}$, as illustrated in Fig. 4.12 (b). As the annealing temperature increases, more Si-M or M-Si bonds are created, causing a further shift and eventual pinning of $\Phi_{m,eff}$ to 4.3 ~ 4.4 eV or 4.7 ~ 4.8 eV, depending on the location of silicon. The possibility of effective work function shift by the dipole formation at the interface is in line with chemical bonding theory [4.5]-[4.7], which explained the Fermi-level pinning phenomenon by the formation of the polarized chemical bonds at metal-semiconductor interfaces.



(a) (b)

Fig. 4.12 Schematic drawing of charging characteristics of interface states at the metal-dielectric interface. The extrinsic interface states cause a shift of $E_{CNL,d}$ toward (a) E_C and (b) E_V to compensate the additional dipole charge (+q' and –q'') generated by Si-M and M-Si bond, respectively.

4.5 SUMMARY

Thermal instability of $\Phi_{m,eff}$ and its material dependence on metal/high-K gate stack is investigated. Before high temperature process except PMA the MIGS theory with intrinsic interface states is found to be applicable to predict the $\Phi_{m,eff}$ value of metal nitride/HfAlO gate stack. However, after high temperature RTA, this theory is not applicable due to thermal instability of $\Phi_{m,eff}$ owing to the generation of substantial amount of extrinsic interface states at the metal/dielectric interface.

It is also found that thermal instability of $\Phi_{m,eff}$ of metal electrode on gate dielectric is strongly dependent on both gate electrode and dielectric material. The presence of silicon and its location at the interface play a major role in the modification of $\Phi_{m,eff}$ after annealing. The behavior of $\Phi_{m,eff}$ has been explained with the types and locations of extrinsic interface states which are generated by silicon-metal bond during high temperature annealing. When silicon is at the electrode side, additional dipoles generated by Si-Metal bonds induce the additional donor-like interface states, causing the decrease of $\Phi_{m,eff}$. On the contrary, when silicon is at the dielectric side, additional dipoles generated by Metal-Si bonds induce the additional acceptor-like interface states, causing the increase of $\Phi_{m,eff}$.

References

[4.1] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *J. Appl. Phys.*, vol. 92, pp. 7266-7271, 2002.

[4.2] Steven G. Louie and Marvin L. Cohen, "Electronic structure of a metal-semiconductor interface," *Physical Review B*, vol. 13, pp. 2461-2469, 1976.

[4.3] P. W. Peacock and J. Robertson, "Band offsets and Schottky barrier heights of high dielectric constant oxides," *Journal of Applied Physics*, vol. 92, pp. 4712-4721, 2002.

[4.4] Y.–C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of high-K gate dielectric materials on metal and silicon gate workfunctions," *IEEE Electron Device Letters*, vol. 23, pp. 342-344, 2002.

[4.5] Raymond T. Tung, "Chemical bonding and Fermi level pinning at metal-semiconductor interfaces," *Physical Review Letters*, vol. 84, pp. 6078-6081, 2000.

[4.6] Raymond T. Tung, "Formation of an electric dipole at metal-semiconductor interfaces," *Physical Review B*, vol. 64, 205310, 2001.

[4.7] R. A. McKee, F. J. Walker, M. Buongiorno Nardelli, W. A. Shelton, and G. M. Stocks, "The interface phase and the Schottky barrier for a crystalline dielectric on silicon," *Science*, vol. 300, pp. 1726-1730, 2003.

[4.8] J. Bardeen, "Surface states and rectification at a metal semi-conductor contact," *Phys. Rev.*, vol. 71, pp. 717-727, 1947.

[4.9] V. Heine, “Theory of surface state,” *Phys. Rev.*, vol. 138, pp. A1689-A1696, 1965.

[4.10] D. A. Muller, D. A. Shashkov, R. Benedek, L. H. Yang, J. Silcox, and D. N. Seidman, “Atomic scale observations of metal-induced gap states at {222} MgO/Cu interfaces ,” *Phys. Rev. Lett.*, vol. 80, pp. 4741-4744, 1998.

[4.11] W. Mönch, “Electronic properties of ideal and interface-modified metal-semiconductor interfaces,” *J. Vacuum Science Technology B*, vol. 14, pp. 2985-2993, 1996.

[4.12] W. Mönch, “Role of virtual gap states and defects in metal-semiconductor contacts,” *Phys. Rev. Lett.*, vol. 58, pp. 1260-1263, 1987.

[4.13] J. K. Schaeffer, *et al.*, “Physical and electrical properties of metal gate electrodes on HfO_2 gate dielectrics,” *J. Vacuum Science Technology B*, vol. 21, pp. 11-17, 2003.

[4.14] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, “Fermi Level Pinning at the PolySi/Metal Oxide Interface,” in *Symp. VLSI Tech. Dig.,* 2003, pp. 9-10.

[4.15] K. Xiong, P. W. Peacock, and J. Robertson, “Fermi-level pinning and Hf-Si bonds at HfO_2: Polycrystalline silicon gate electrode interfaces,” *Appl. Phys. Lett.*, vol. 86, 012904, 2005.

[4.16] C. W. Yang, Y. K. Fang, C. H. Chen, S. F. Chen, C. Y. Lin, M. F. Wang, Y. M. Lin, T. H. Hou, C. H. Chen, L. G. Yao, S. C. Chen, and M. S. Liang, “Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metal-oxide-semiconductor field-effect transistors

for high-K-HfO_2 dielectric" *Applied Physics Letters*, vol 83, pp. 308-310, 2003.

[4.17] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hedge, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part I," and "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *IEEE Trans. Electron Dev*., vol. 51, pp. 971-984, 2004.

[4.18] L. Pantisano, P. J. Chen, V. Afanas'ev, L.-Å. Ragnarsson, G. Pourtois, and G. Groeseneken, "Direct measurement of barrier height at the HfO_2/poly-Si interface: band structure and local effects," in *Symp. VLSI Tech. Dig.,* 2004, pp. 122-123.

[4.19] E. Cartier, V. Narayanan, E. P. Gusev, P. Jamison, B. Linder, M. Steen, K. K. Chan, M. Frank, N. Bojarczuk, M. Copel, S. A. Cohen, S. Zafar, A. Callegari, M. Gribelyuk, M. P. Chudzik, C. Cabral Jr., R. Carruthers, C. D'Emic, J. Newbery, D. Lacey, S. Guha, and R. Jammy, "Systematic study of pFET V_t with Hf-based gate stacks with poly-Si and FUSI gates," in *Symp. VLSI Tech. Dig.,* 2004, pp. 44-45.

[4.20] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whoang, S. Mathew, L. K. Bera, N. Balasubramanian, and D.-L. Kwong, "Formation of Hafnium-Aluminum-Oxide gate dielectric using single cocktail liquid source in MOCVD process", *IEEE Trans. Electron Dev*., vol. 50, pp. 2088-2094, 2003.

[4.21] H. Y. Yu, J. F. Kang, J.D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du, and D. -L. Kwong, "Thermally robust high quality HfN/HfO_2 gate stack for advanced CMOS devices," in *IEDM Tech. Dig.,* 2003, pp. 99-102.

[4.22] C. Ren, H. Y. Yu, J. F. Kang, Y. T. Hou, M. F. Li, W. D. Wang, D. S. H. Chan, and D. -L. Kwong, "Fermi level pinning induced thermal instability in the effective work function of TaN in TaN/SiO_2 gate stack," *IEEE Electron Device Letters*, vol. 25, pp. 123-125, 2004.

[4.23] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, N. Balasubramanian, A. Chin, and D.-L. Kwong, "Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-K gate dielectric" *Applied Physics Letters*, vol. 85, pp. 4127-4129, 2004.

[4.24] O. Renault, D. Samour, J.-F. Damlencourt, D. Blin, F. Martin, and S. Marthon, N. T. Barrett, and P. Besson, "HfO_2/SiO_2 interface chemistry studied by synchrotron radiation x-ray photoelectron spectroscopy" *Applied Physics Letters*, vol. 81, pp. 3627-3629, 2002.

[4.25] Electronegativity value of each element available on http://en.wikipedia.org/wiki/Electronegativity

CHAPTER 5

INTERFACE CONFIGURATION AND FERMI-LEVEL PINNING OF FULLY SILICIDED (FUSI) GATE AND HIGH-K DIELECTRIC STACK

5.1 INTRODUCTION

Metal gate and high-K dielectric stack is an obvious trend in nanoscale Complementary Metal-Oxide-Semiconductor (CMOS) devices because of its low gate leakage current and polysilicon-depletion-free feature. Among them, fully silicided gates (FUSI gate) appear increasingly attractive due to minimal modification of conventional CMOS process flow and easy work function engineering by pre-doping of gate polysilicon [5.1]-[5.4]. On the other hand, Fermi-level pinning phenomenon becomes a critical issue when high-K gate dielectric is employed [5.5],[5.6]. Metal-induced gap states (MIGS) theory, which has been discussed in Chapter 4, is most widely used to analyze and predict the behavior of effective work function ($\Phi_{m,eff}$) in metal gate/high-K dielectric stack [5.7],[5.8]. Up to date, however, the application of MIGS theory to FUSI gate/high-K dielectric stack has not been attempted because of lack of information on vacuum work function of metal silicide (Φ_{MSix}) on high-K gate

dielectric which is affected by stoichiometry of metal silicide at the high-K dielectric interface.

In this chapter, we suggest a semi-empirical approach for the application of MIGS theory to FUSI gate and provide a quantitative analysis on Fermi-level pinning of FUSI gate on high-K dielectrics.

5.2 EXPERIMENTAL

5.2.1 MOS CAPACITOR FABRICATION AND EXPERIMENTAL SET-UP

The MOS capacitors with SiO_2 and HfAlON gate dielectrics were fabricated on p-type (100) Si substrates. SiO_2 dielectric films were formed by conventional thermal oxidation in a furnace and HfAlON dielectric films were formed by thermal nitridation of HfAlO films in an NH_3 ambient at 800℃, which was deposited on diluted HF-cleaned silicon surface by metal-organic chemical vapor deposition (MOCVD) [5.9]. Four kinds of FUSI gate using Ni-, Pt-, Hf-, and Ti-silicide were formed on the gate dielectrics. The details of each FUSI gate formation will be described in next section. Finally, post metallization annealing (PMA) in a forming gas ambient at 420℃ was done to all devices.

The capacitance versus voltage (C-V) measurements was conducted using HP 4284A precision LCR meter analyzer for MOS capacitors. The frequency used for C-V measurement was 100 kHz. The equivalent oxide thickness (EOT) was extracted using simulation program taking quantum mechanical effect into consideration. The V_{fb} value of each sample is calculated from the comparison of its C-V curve with

simulated C-V curve. The $\Phi_{m,eff}$ values of metal gates on gate dielectric were extracted from plots of V_{fb} versus the EOT of gate dielectric.

5.2.2 FUSI GATE FORMATION PROCEDURES

Polysilicon with a thickness range of 40-50 nm was deposited on the gate dielectric using a low pressure chemical vapor deposition (LPCVD) furnace, followed by the deposition of various metal films using sputtering. Before metal film deposition, all wafers were subjected to dip into a dilute 1% HF (DHF) solution to ensure the removal of native oxide on the polysilicon surface.

For FUSI gate using Ni-silicide (hereafter Ni-FUSI gate), 120 nm thick Ni films were deposited and annealed in a rapid thermal annealing (RTA) chamber at 550℃ for 1 min in a N_2 ambient at an atmospheric pressure. For Platinum-FUSI gate, 200 nm thick Pt films were deposited and annealed in a furnace tube at 420℃ for 30 min at a low pressure with a N_2 gas flow. For Pt silicide formation, Ti capping layer was used on top of Pt to prevent oxygen diffusion along grain boundaries in polycrystalline Pt film [5.10]. For Titanium-FUSI and Hafnium-FUSI [5.11] gates, 60 nm thick Ti and 80 nm thick Hf films were deposited and annealed in a RTA chamber at 600℃ for 1 min in a N_2 ambient at an atmospheric pressure, respectively. For the each FUSI gate process, the thickness of metal film was selected to be thick enough to ensure full silicidation.

5.3 THEORETICAL BACKGROUND: SEMI-EMPIRICAL APPROACH

For the successful implementation of MIGS theory on FUSI process, the information on $\Phi_{m,eff}$ and the Φ_{MSix} on the particular gate dielectric is necessary. The values of $\Phi_{m,eff}$ can experimentally be obtained from the relationship between flat-band voltage (V_{fb}) and EOT. However, it is pretty difficult to obtain the Φ_{MSix} value of the metal silicide due to the feature of easily oxidized surface of metal silicide and also the possible difference of the stoichiometry of metal silicide between the bulk film and the interface contacting the gate dielectric. On the other hand, Freeouf [5.12],[5.13] obtained the calculated work functions (Φ_{MSix}) of metal silicide on silicon substrate using a semi-empirical approach. He assumed a silicon-silicide interface with an arbitrary composition of MSi_x (x= 4) and then calculated the work function of this interfacial layer as a weighted average of the metal (Φ_M) and silicon work functions (Φ_{Si}), that is,

$$\Phi_{MSix} = (\Phi_M \Phi_{Si}^{x})^{1/x+1} \quad . \tag{5.1}$$

Assuming the same interface stoichiometry of MSi_4 for the several silicides, he found that the most of observed barrier heights are consistent with the Schottky picture as shown in Fig. 5.1 and the enhancement in silicon concentration at the interface.

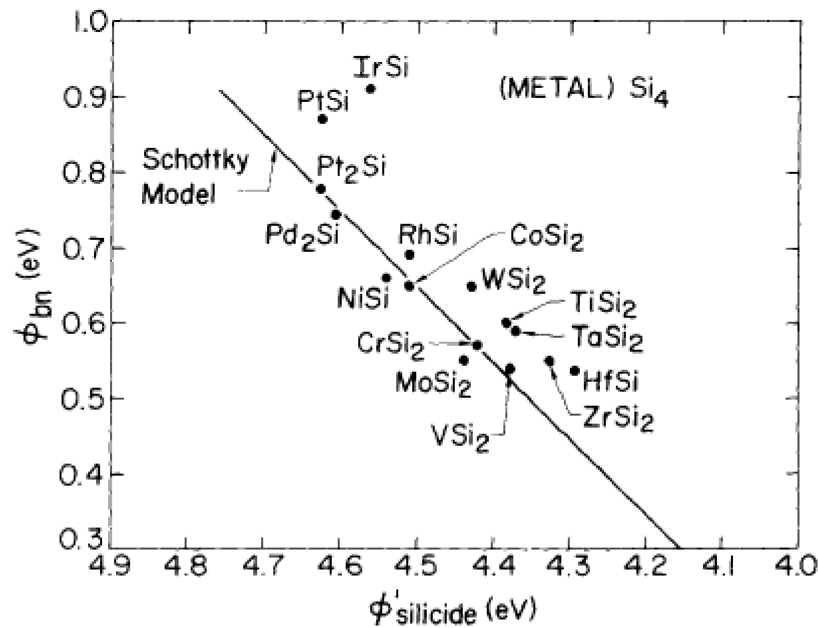


Fig. 5.1 Barrier height between silicide and n-silicon plotted against calculated silicide workfunction assuming (metal) Si_4 stoichiometry [5.12].

5.4 RESULTS AND DISCUSSION

5.4.1 INTERFACE CONFIGURATION OF FUSI GATE/GATE DIELECTRIC STACK

The semi-empirical approach discussed in the previous section is adopted here to obtain the Φ_{MSix} value of the FUSI gate on gate dielectrics. Combining this approach and MIGS theory, the Φ_{MSix} value of the FUSI gate on gate dielectric can be obtained semi-empirically. We applied this technique to FUSI gate on silicon dioxide (SiO_2) film first, as SiO_2 has negligible Fermi level pinning effect. The results for four different FUSI gates on SiO_2 are shown in Fig. 5.2, which shows $\Phi_{m,eff}$ versus Φ_{MSix} of

four metal silicides on SiO_2. The values of Φ_{MSix} are calculated by taking the geometric mean of Φ_M and Φ_{Si} with various stoichiometries (X) between metal and silicon as discussed in Eq. 5.1. For work function calculation of each FUSI gate, Φ_{Hf} = 3.90 eV, Φ_{Ti} = 4.33 eV, Φ_{Ni} = 5.15 eV, and Φ_{Pt} = 5.65 eV are used [5.14],[5.15] and Φ_{Si} = 4.61 eV for undoped polysilicon are assumed.

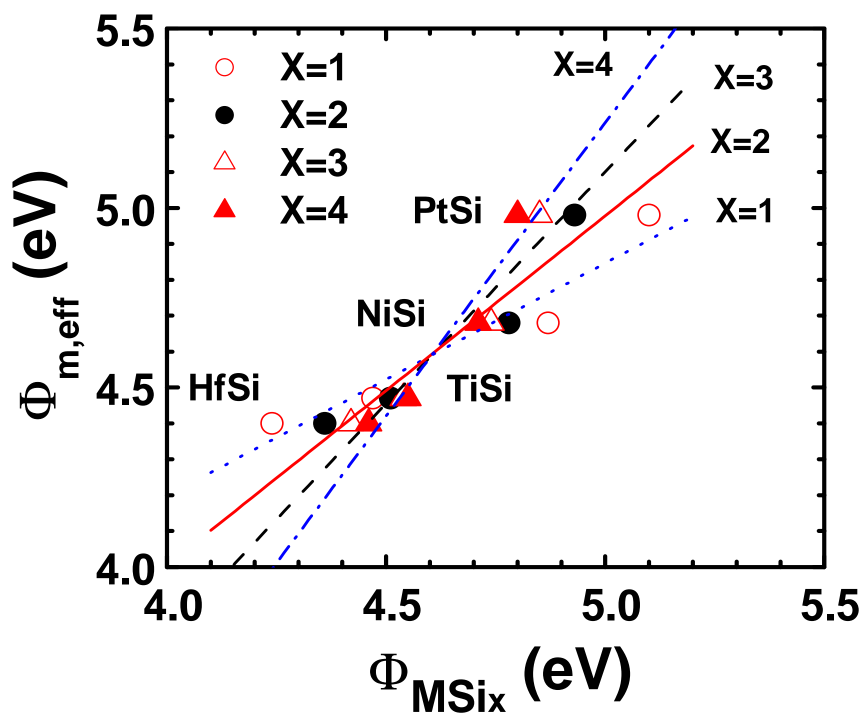


Fig. 5.2 $\Phi_{m,eff}$ versus Φ_{MSix} of four metal silicides on SiO_2. The Φ_{MSix} value is calculated by taking the geometric mean of Φ_M and Φ_{Si} with various stoichiometries (X) between metal and silicon.

Two important parameters of MIGS theory, the slope parameter S and the charge neutrality level ($\Phi_{CNL,d}$), are obtained for the FUSI gates/SiO_2 structure by a least-squares fit method using the data in Fig. 5.2 and Eq. (5-2) in the next page [5.7],[5.8]

$$\Phi_{m,eff} = \Phi_{CNL,d} + S(\Phi_{MSix} - \Phi_{CNL,d})\,. \qquad (5\text{-}2)$$

Figure 5.3 shows the slope parameter S and the charge neutrality level $\Phi_{CNL,d}$ for FUSI gates on SiO_2 as a function of X in MSi_x. The slope parameter S is a dimensionless pinning factor with a range between 0 to 1, which describes the strength of Fermi level pinning and depends on the electronic part of the dielectric constant ε_∞ [5.8] as discussed in Chapter 4. As the X in MSi_x increases from 1 to 4, the S value increases from around 0.6 to 1.6 whereas the $\Phi_{CNL,d}$ value remains nearly fixed at around 4.6 eV. It is interesting to note that for the case of X=2, the S value of 0.93 is nearly identical to the experimental value of 0.95 for SiO_2 [5.7] directly obtained from other pure metal gates on SiO_2. However, other X values (for X=1 or X=3 and 4) shows unreasonably low or high S values. Since SiO_2 has negligible Fermi-level pinning, the S value obtained from FUSI gate must be similar to the one obtained from pure metal gate. From the above analysis, therefore, we can conclude that, at the dielectric interface, the stoichiometry of FUSI gate is MSi_2 or at least we can say that FUSI gates have effectively MSi_2 structure at the interface for the analysis of work function behavior. The values of $\Phi_{m,eff}$ and semi-empirically obtained Φ_{MSix} of each FUSI gate on SiO_2 are summarized in Table 5.1. Note that the values of $\Phi_{m,eff}$ and Φ_{MSi2} of each FUSI gate are within 0.1 eV each other, as the Fermi level pinning on SiO_2 is negligible.

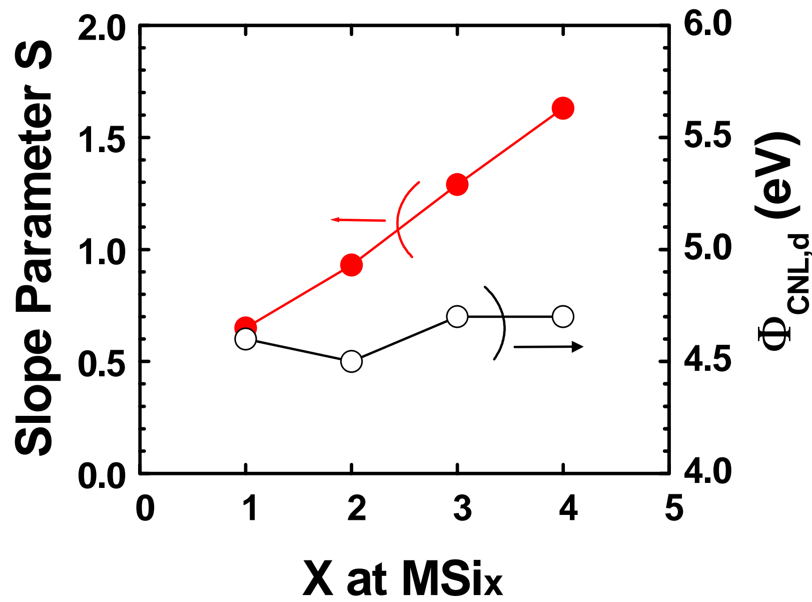


Fig. 5.3 The slope parameter S and the charge neutrality level $\Phi_{CNL,d}$ on SiO_2 as a function of X at MSix.

Table 5.1 Comparison of $\Phi_{m,eff}$ and Φ_{MSi2} of each FUSI gate on SiO_2. The Φ_{MSi2} values are obtained from the equation of $\Phi_{MSix} = (\Phi_M \Phi_{Si}^{x})^{1/x+1}$ where x = 2.

FUSI gate	Φ_{MSi2} (eV)	$\Phi_{m,eff}$ (eV)
HfSi	4.36	4.40
TiSi	4.51	4.47
NiSi	4.78	4.68
PtSi	4.93	4.98

5.4.2 IMPLEMENTATION OF MIGS THEORY ON FUSI GATE/HIGH-K DIELECTRIC STACK

The information of vacuum work function values (Φ_{MSix}) of FUSI gate obtained above now enables us to analyze the Fermi-level pinning on high-K gate dielectrics using MIGS theory. Figure 5.4 shows the $\Phi_{m,eff}$ versus Φ_{MSix} of MSi_2 on SiO_2 and HfAlON. From the results, we can obtain the values of S and $\Phi_{CNL,d}$ of FUSI gate electrode on HfAlON high-K dielectric, which are around 0.67 and 4.8 eV, respectively. This S value is nearly identical to the S value of around 0.63, calculated using the empirical equation of S,

$$S=[1+0.1(\varepsilon_\infty-1)^2]^{-1}, \tag{5.3}$$

which indicates that HfAlON with FUSI gate obeys the MIGS theory well.

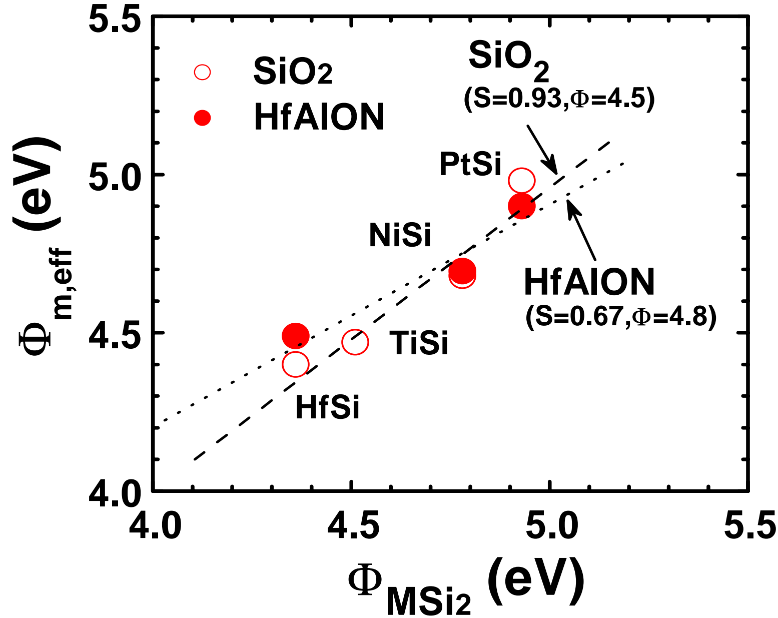


Fig. 5.4 $\Phi_{m,eff}$ versus Φ_{MSiX} of MSi_2 on SiO_2 and HfAlON. The S value of HfAlON is nearly identical to the calculated S value of around 0.63 obtained from Eq. 5.3.

5.4.3 FERMI-LEVEL PINNING OF FUSI GATE/HIGH-K DIELECTRIC STACK

From the data we obtained in Fig. 5.4, we can compare the strength of Fermi-level pinning for the FUSI gate/HfAlON stack with those of other gate stacks. Figure 5.5 shows the comparison between the S value of HfAlON and those of other gate electrode/high-K stacks. In this comparison, HfAlO and HfO_2 with metal nitrides (MN) [5.6] and polysilicon/HfO_2 stack [5.5] were used. The values of S and $\Phi_{CNL,d}$ of each gate stack are summarized in Table 5.2. While polysilicon/HfO_2 stack has much lower S value compared to MN/HfO_2 stack, FUSI gate/HfAlON stack shows only a slightly smaller S value compared to MN/HfAlO stack. It has been known that the extremely low S value of polysilicon/HfO_2 stack is due to strong Fermi-level pinning by Si-Hf bond formation at the interface [5.5]. The above result indicates that Fermi-level pinning for FUSI gate/HfAlON stack is not strong, even under the presence of Si atoms at the interface between FUSI gate and HfAlON dielectric, providing that metal film is sufficiently thick compared to polysilicon before silicidation anneal. This is another important advantage of FUSI process when it is used together with high-K gate dielectrics. However, if the metal film thickness is not sufficiently thick, the strong Fermi-level pinning for FUSI gate/high-K stack might happen due to the presence of Si atoms at the interface between FUSI gate and high-K dielectric. The dependence of Fermi-level pinning strength on metal film thickness will be discussed in the next chapter.

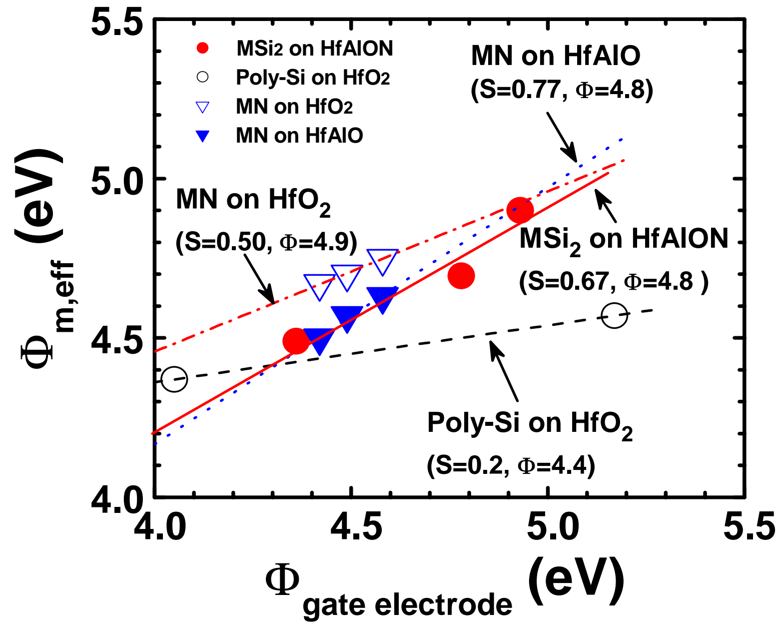


Fig. 5.5 Comparison of S value of various gate electrodes on high-K gate dielectrics. HfAlON with FUSI gate shows weak Fermi-level pinning, even though Si atoms are present at the interface of FUSI gate/HfAlON stack.

Table 5.2 Comparison of S value and $\Phi_{CNL,d}$ of four kinds of gate stacks. The FUSI gate/HfAlON stack shows a slightly smaller S value compared to MN/HfAlO stack.

Gate stack	S	$\Phi_{CNL,d}$ (eV)
FUSI gate on HfAlON	0.67	4.8
MN on HfAlO	0.77	4.8
MN on HfO_2	0.50	4.9
Poly-Si on HfO_2	0.20	4.4

5.5 SUMMARY

A new approach to analyze and predict the behavior of effective work function in FUSI gate/high-K dielectric stack and its interface configuration is proposed using the combination of semi-empirical approach and MIGS theory. It is found that FUSI gate has effectively MSi_2 configuration at the gate dielectric interface. The vacuum work function values of several FUSI gates have been obtained through the analysis, and it is also found that the Fermi-level pinning behavior of FUSI gate on high-K dielectric follows MIGS theory well. FUSI gate on high-K dielectric is evaluated to have much weaker Fermi-level pinning compared to polysilicon gate on high-K, providing that metal film is sufficiently thick compared to polysilicon before silicidation anneal.

References

[5.1] B. Tavel, T. Skotnicki, G. Pares, N. Carrière, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally silicided ($CoSi_2$) polysilicon: a novel approach to very low-resistive gate (~2Ω/□) without metal CMP nor etching," in *IEDM Tech. Dig.,* pp. 825-828, 2001.

[5.2] W. P. Maszara, Z. Krivokapic, P. King, J.-S. Goo, and M.-R. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates," in *IEDM Tech. Dig.,* pp. 367-370, 2002.

[5.3] J. Kedzierski, D. Boyd, C. Cabral, Jr., P. Ronsheim, S. Zafar, P. M. Kozlowski, J. A. Ott, and M. Ieong, "Threshold voltage control in NiSi-gated MOSFETs through SIIS," *IEEE Trans. Electron Devices*, vol. 52, pp. 39-46, 2005.

[5.4] D. Aimé, B. Froment, F. Cacho, V. Carron, S. Descombes, Y. Morand, N. Emonet, F. Wacquant, T. Farjot, S. Jullian, C. Laviron, M. Juhel, R. Pantel, R. Molins, D. Delille, A. Halimaoui, D. Bensahel, and A. Souifi, "Work function tuning through dopant scanning and related effects in Ni fully silicided gate for sub-45nm nodes CMOS," in *IEDM Tech. Dig.,* pp. 87-90, 2004.

[5.5] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hedge, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part I," and "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *IEEE Trans. Electron Dev.*, vol. 51, pp. 971-984, 2004.

[5.6] M. S. Joo, B. J. Cho, N. Balasubramanian, and D.-L. Kwong, "Thermal instability of effective work function in metal/high-K stack and its material dependence," *IEEE Electron Device Lett.*, vol. 25, pp. 716-718, 2004.

[5.7] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *J. Appl. Phys.*, vol. 92, pp. 7266-7271, 2002.

[5.8] P. W. Peacock and J. Robertson, "Band offsets and Schottky barrier heights of high dielectric constant oxides," *Journal of Applied Physics*, vol. 92, pp. 4712-4721, 2002.

[5.9] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whoang, S. Mathew, L. K. Bera, N. Balasubramanian, and D.-L. Kwong, "Formation of Hafnium-Aluminum-Oxide gate dielectric using single cocktail liquid source in MOCVD process", *IEEE Trans. Electron Dev.*, vol. 50, pp. 2088-2094, 2003.

[5.10] C. S. Park, B. J. Cho, W. S. Hwang, W. Y. Loh, L. J. Tang, and D.-L. Kwong, "Dual metal gate process by metal substitution of dopant-free polysilicon on high-K dielectric" in *Symp. on VLSI Tech.*, pp. 48-49, 2005.

[5.11] C. S. Park, B. J. Cho, and D. L. Kwong, "Thermally stable fully silicided Hf-silicide metal-gate electrode", *IEEE Trans. Electron Dev.*, vol. 25, pp. 372-374, 2004.

[5.12] J. L. Freeouf, "Silicide Schottky barriers: an elemental description", *Solid State Communications*, vol. 33, pp. 1059-1061, 1980.

[5.13] J. L. Freeouf, "Silicide interface stoichiometry", *J. Vac. Sci. Technol.*, vol. 18, pp. 910-916, 1981.

[5.14] D. R. Lide, *Handbood of Chemistry and Physics*, 84th edition (CRC Press, 2003-2004).

[5.15] Electron work function of each element available on http://environmentalchemistry.com/yogi/periodic/

CHAPTER 6

STOICHIOMETRY DEPENDENCE OF FERMI-LEVEL PINNING IN FULLY SILICIDED (FUSI) NiSi GATE ON HIGH-K DIELECTRIC

6.1 INTRODUCTION

As an alternative gate electrode material to polysilicon, fully silicided gate (so called, FUSI gate) stack is recently investigated because of its polysilicon-depletion-free feature and capability of work function modulation by pre-doping of polysilicon [6.1],[6.2]. Although its implementation on high-K dielectric has been demonstrated, the precise control of threshold voltage of MOSFETs still remains a concern due to Fermi-level pinning phenomenon [6.3]-[6.6]. The recent reports on Fermi-level pinning in FUSI gate/high-K stack have not been consistent. Some research groups reported weak or negligible Fermi-level pinning in FUSI gate/high-K stack [6.3],[6.7]. In Chapter 5, we have also shown the weak or negligible Fermi-level pinning in FUSI gate/high-K stack, where metal film is sufficiently thick compared to polysilicon before silicidation anneal. On the contrary, other groups reported the strong Fermi-level pinning in FUSI gate/high-K stack [6.4],[6.5],[6.8],[6.9]. Such inconsistency may

suggest that the degree of Fermi-level pinning in FUSI gate/high-K stack depends on the process conditions in FUSI gate fabrication process.

In this chapter, new findings on the Fermi-level pinning phenomenon in FUSI gate/high-K dielectric stack will be reported, focusing on process condition and material composition dependence of Fermi-level pinning which is essential information for the successful implementation of FUSI gate on high-K gate dielectrics.

6.2 EXPERIMENTAL

6.2.1 MOS CAPACITOR FORMATION PROCEDURES

The MOS capacitors with SiO_2 and HfAlON with various thicknesses were fabricated on the DHF-cleaned p-type (100) Si substrates. SiO_2 dielectric films were formed by conventional thermal oxidation in a furnace and HfAlON dielectric films were formed using thermal nitridation of metal-organic chemical vapor deposition (MOCVD) HfAlO films [6.10] in an NH_3 ambient at 800℃. Polysilicon with a thickness range of 40-50 nm was deposited on the gate dielectric using a low pressure chemical vapor deposition (LPCVD) furnace, followed by the deposition of various metal films using sputtering. Before metal film deposition, all the wafers were subjected to dip into a dilute 1% HF (DHF) solution to ensure the removal of native oxide on the polysilicon surface. For FUSI gate using Ni-silicide (hereafter Ni-FUSI gate), Ni film was deposited and followed by rapid thermal anneal (RTA) at 550°C for 1 min. In this chapter, the ratio of original film thickness before the silicidation anneal is defined by $R_{Ni} = \frac{\text{thickness of Ni}}{\text{thickness of polysilicon}}$. Three different R_{Ni} of 2.5, 1.25, and

0.70 are used in this experiment. After silicidation, unreacted Ni film was removed using a H_2O_2 : H_2SO_4 solution.

6.2.2 EXPERIMENTAL SET-UP

For the investigation of the composition ratio between metal and silicon of FUSI gate films, Rutherford Backscattering Spectrometry (RBS) was used. For the investigation of effective work function ($q\Phi_{m,eff}$) values of MOS capacitor, the capacitance versus voltage (C-V) measurements was conducted using HP 4284A precision LCR meter analyzer. The frequency used for C-V measurement was 100 kHz. The equivalent oxide thickness (EOT) was extracted using simulation program taking quantum mechanical effect into consideration. The effective work function ($q\Phi_{m,eff}$) values of metal gates on gate dielectric were extracted from plots of flat-band voltage (V_{fb}) versus the EOT of gate dielectric.

6.3 RESULTS AND DISCUSSION

6.3.2 FERMI-LEVEL PINNING PHENOMENON IN FUSI GATE/HIGH-K DIELECTRIC STACK

Figure 6.1 shows V_{fb} of MOS capacitor versus the EOT of gate dielectric for Ni-FUSI gate stacks with R_{Ni}=2.5 and 1.25 on both SiO_2 and HfAlON. The intercepts at *y* axis indicate work function difference ($q\Phi_{ms}$) between effective work function of the metal gate ($q\Phi_{m,eff}$) and Fermi-level of silicon substrate ($q\Phi_{Si}$). For Ni-FUSI gate stacks on SiO_2, there is no difference in $q\Phi_{m,eff}$ between the samples with R_{Ni} = 1.25

and R_{Ni} = 2.5. However, for Ni-FUSI gate stack on HfAlON, there is a significant difference in $q\Phi_{m,eff}$ between them.

Figure 6.2 shows the plot of $q\Phi_{m,eff}$ as a function of the thickness ratio of Ni to polysilicon on both SiO_2 and HfAlON. When initial metal thickness is thick enough compared to polysilicon, the $q\Phi_{m,eff}$ values of SiO_2 and HfAlON are almost the same, which means almost no Fermi-level pinning in FUSI/high-K gate stack. However, as R_{Ni} becomes thinner, $q\Phi_{m,eff}$ is significantly reduced and finally fixed at around 4.33 eV, which is quite similar to the Fermi-level pinning point of polysilicon/HfO_2 stack [6.6].

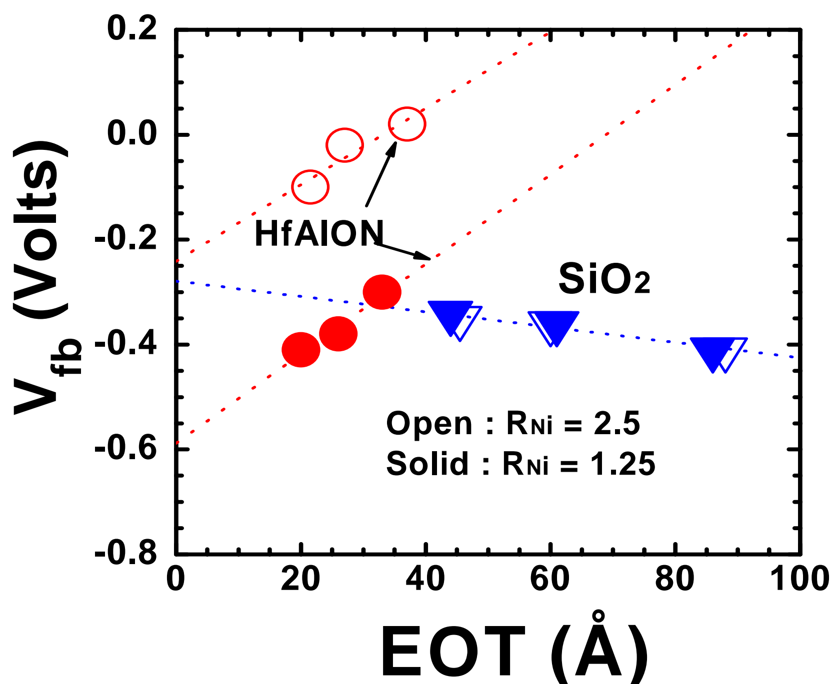


Fig. 6.1 V_{fb} of MOS capacitor versus EOT of gate dielectric for Ni-FUSI gate stacks with two different thickness ratios (R_{Ni}) on both SiO_2 and HfAlON dielectric. Significant shift in $q\Phi_{m,eff}$ is observed for Ni-FUSI gate with R_{Ni}=1.25 on HfAlON.

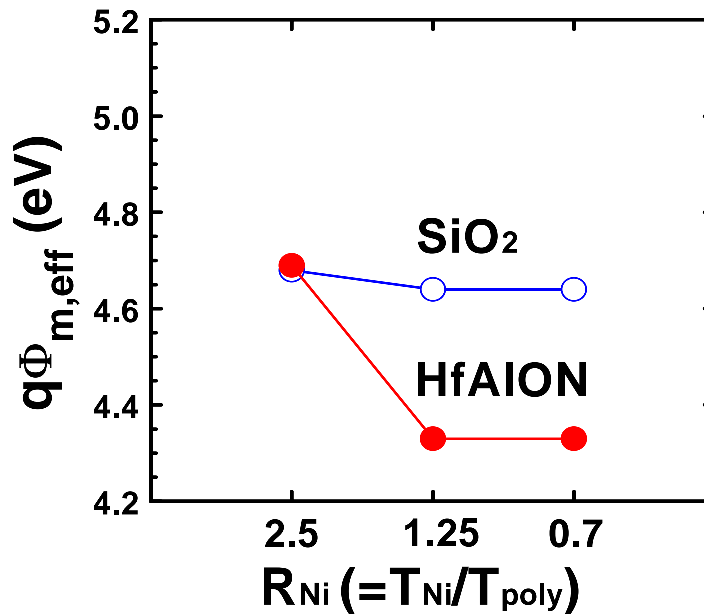


Fig. 6.2 $q\Phi_{m,eff}$ versus thickness ratio of Ni to polysilicon for Ni-FUSI gate on both SiO_2 and HfAlON. A strong Fermi-level pinning is observed in Ni-FUSI films on HfAlON when R_{Ni} is low.

6.3.2 The Composition Ratio of Ni-FUSI Samples

The composition ratio of Ni to Si of each Ni-FUSI sample is investigated using the RBS analysis by the bombardment of He ions with 2 MeV energy. Figure 6.3 shows the RBS spectra for Ni-FUSI sample with R_{Ni}=2.5 on HfAlON. The composition ratio is estimated to be around 3.0, which means the stoichiometry of this Ni-FUSI sample is Ni_3Si. The composition ratios for other Ni-FUSI samples are also estimated from RBS spectra. Figure 6.4 shows the plot of atomic ratio of Ni to Si as a function of the thickness ratio of Ni to polysilicon. As shown in Fig. 6.4, the samples with the composition ratios of R_{Ni}=1.25 and 0.7 are estimated to be 1.9 and 1.0, respectively. This result indicates that the stoichiometries for the Ni-FUSI samples

with R_{Ni}=2.5, 1.25, and 0.7 are approximately Ni_3Si, Ni_2Si, and NiSi, respectively. A similar trend can also be found in Ref. [6.9].

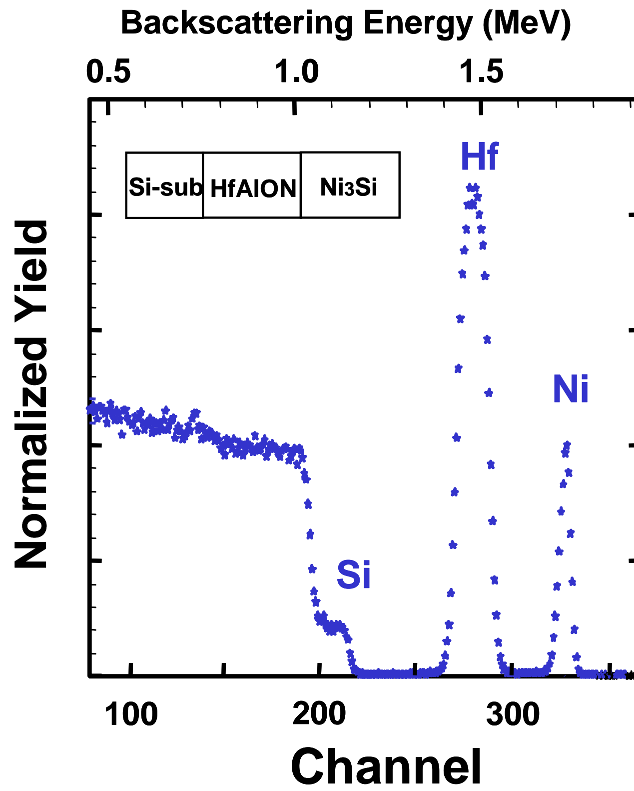


Fig. 6.3 RBS spectrum of Ni-FUSI film with R_{Ni}=2.5. The composition ratio of Ni to Si is estimated to be 3, which means Ni_3Si phase.

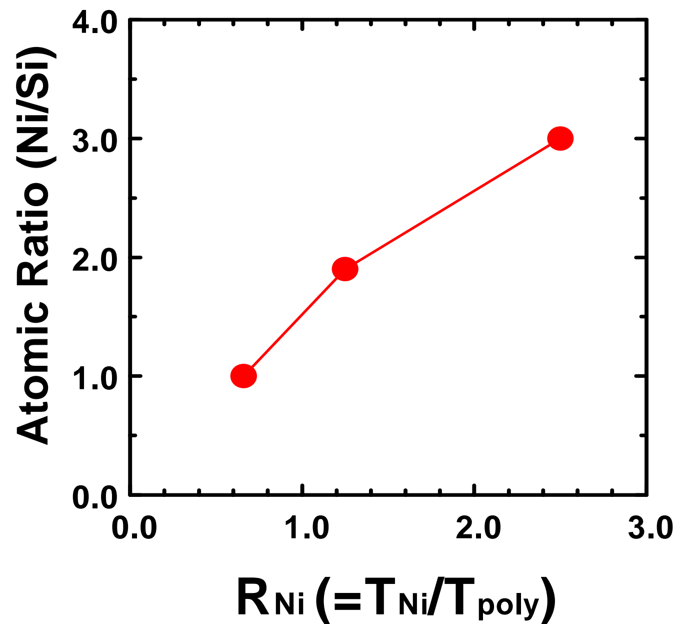


Fig. 6.4 Composition ratio of Ni to Si as function of R_{Ni}. The composition ratio of Ni to Si is estimated by RBS analysis.

6.3.3 GATE DIELECTRIC DEPENDENCE OF FERMI-LEVEL PINNING

The dependence of Fermi-level pinning strength on gate dielectric is investigated. Figure 6.5 shows the relative difference of $q\Phi_{m,eff}$ ($\Delta q\Phi_{m,eff}$), taking Ni_3Si phase Ni-FUSI sample as a reference, for Ni-FUSI gates with different composition ratios on three different types of gate dielectrics. The $\Delta q\Phi_{m,eff}$ values of Ni-FUSI/HfSiON stack are taken from Ref. [6.9]. It is interesting to note that when Ni concentration is decreased, the $\Delta q\Phi_{m,eff}$ of Ni-FUSI/High-K gate stack becomes more negative but eventually merges at about -0.36 eV even for different types of high-K. The final merging point corresponds to 0.28 eV below the silicon conduction band

edge, which is quite similar to the predicted Fermi-level pinning point of ~0.3 eV by Hf-Si bond at polysilicon/HfO_2 interface [6.6],[6.11]. Since the $q\Phi_{m,eff}$ does not decrease after this point, we define it as "strong Fermi-level pinning". The result in Fig. 6.5 suggests that there is a critical composition ratio (C_{crit}) of Ni to Si which starts to show the strong Fermi-level pinning and the C_{crit} depends on underlying gate dielectric materials. The C_{crit} is 0.5 (Si-rich phase, $NiSi_2$) on HfSiON dielectric, but it is 2 (Ni-rich phase, Ni_2Si) when the gate dielectric is HfAlON. The silicon incorporation into HfO_2 dielectric requires more Si in Ni-FUSI gate for strong Fermi-level pinning. Such behaviors of $q\Phi_{m,eff}$ and composition ratio dependence can be explained with the MIGS (metal-induced-gap-state) theory [6.12] with the extrinsic interface states introduced by Hf-Si bond [6.13] at FUSI gate/high-K dielectric interface, which will be discussed in Section 6.3.4.

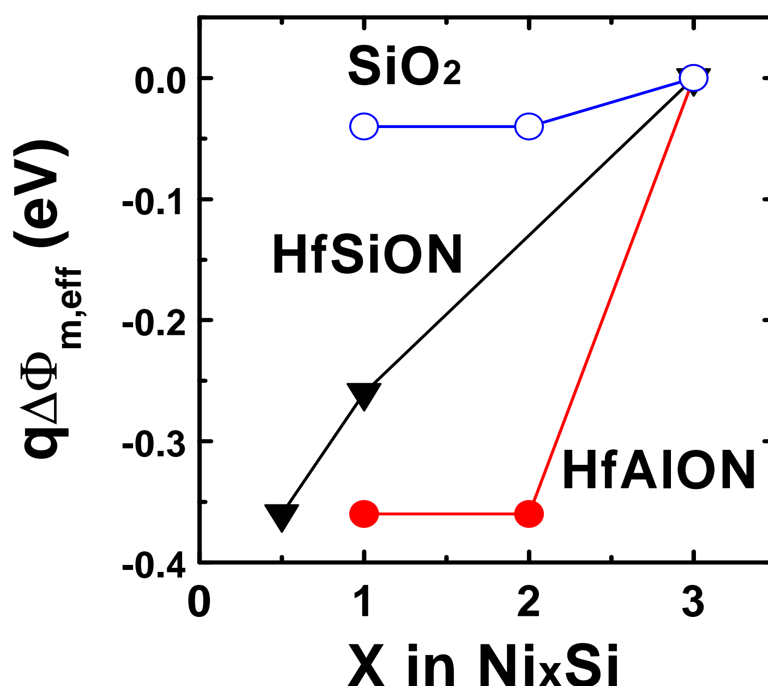


Fig. 6.5 The relative difference of $q\Phi_{m,eff}$ ($\Delta q\Phi_{m,eff}$), taking Ni_3Si phase Ni-FUSI sample as a reference, for Ni-FUSI gates with different composition ratios on three different types of gate dielectrics. Data for Ni-FUSI gate on HfSiON were taken from [6.9].

6.3.4 PROPOSED MODEL

Figure 6.6 shows the schematic drawing of the interface configuration between high-K dielectric and Ni-FUSI gate with extrinsic interface states induced by Hf-Si bond. When Hf-Si bond formation occurs at the interface, it generates the additional dipoles or the extrinsic interface states [6.13]. The electronegativity values of Hf and Si are 1.3 and 1.9, respectively, and Hf is at the dielectric side while Si is at the electrode side. Therefore these dipoles are positively charged at the dielectric side and then the extrinsic interface states should be donor-like, located near E_C [6.13]. In case the extrinsic interface states are dominant, $E_{CNL,d}$ shifts near to the $E_{Hf\text{-}Si}$ in order to balance out the additional positive charges. Based on the observation from the result in Fig. 6.5, $E_{Hf\text{-}Si}$ may lie at around 0.3 eV below the silicon conduction band edge (E_C). Since the change of $E_{CNL,d}$ is due to the formation of Hf-Si bond, the amount of Si at the interface is a critical factor. As Si atoms in Hf-Si bond which causes extrinsic interface states are from gate electrode materials, higher concentration of Si in FUSI gate will cause stronger Fermi-level pinning as observed in the results in Figs. 6.1-6.4. In case that Si is incorporated into high-K dielectric side, like HfSiON gate dielectric, the Hf in the gate dielectric would have less chance to form Hf-Si bond with the Si atoms from gate electrode side, which in turn results in less Fermi-level pinning.

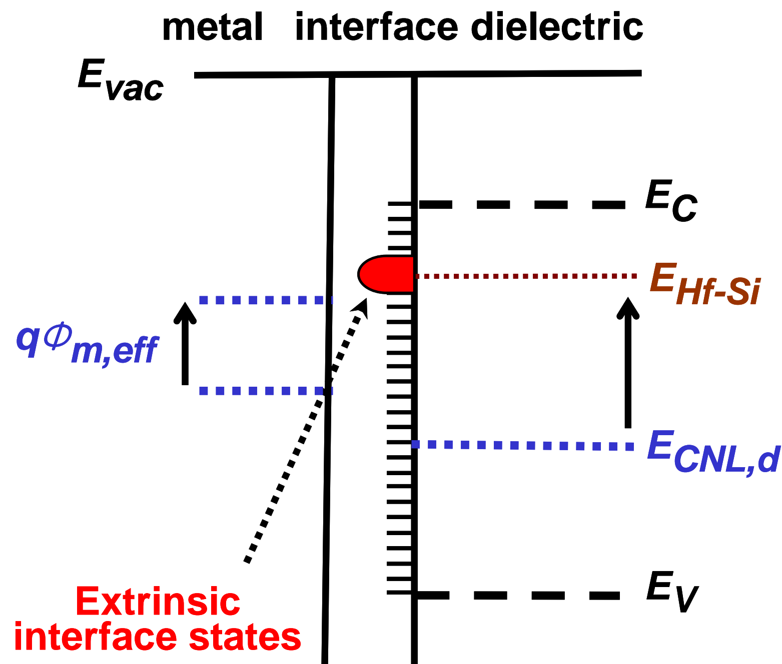


Fig. 6.6 Schematic drawing of the interface configuration between high-K dielectric and Ni-FUSI gate with extrinsic interface states induced by Hf-Si bond. In case the extrinsic interface states are dominant, $E_{CNL,d}$ shifts near to the $E_{Hf\text{-}Si}$, resulting in the strong Fermi-level pinning near to E_C of silicon.

6.5 SUMMARY

Stoichiometry Dependence of Fermi-level pinning in Fully Silicided (FUSI) NiSi gate on high-K dielectric is investigated. Higher composition ratio of Si in NiSi shows higher degree of Fermi-level pinning. It has also been found that there is a critical composition ratio (C_{crit}) of Ni to Si in Ni-FUSI gate which starts to show a strong Fermi-level pinning. The C_{crit} is also found to be dependent on the underlying gate dielectric material. Since such behavior is believed to be due to the Hf-Si

formation at the interface, the control of the amount of Si at the interface is a critical factor for the successful implementation of FUSI gate on high-K gate dielectric.

References

[6.1] B. Tavel, T. Skotnicki, G. Pares, N. Carrière, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, “Totally silicided ($CoSi_2$) polysilicon: a novel approach to very low-resistive gate (~2Ω/□) without metal CMP nor etching,” in *IEDM Tech. Dig.,* pp. 825-828, 2001.

[6.2] J. Kedzierski, D. Boyd, C. Cabral, Jr., P. Ronsheim, S. Zafar, P. M. Kozlowski, J. A. Ott, and M. Ieong, “Threshold voltage control in NiSi-gated MOSFETs through SIIS,” *IEEE Trans. Electron Devices*, vol. 52, pp. 39-46, 2005.

[6.3] K. G. Anil, A. Veloso, S. Kubicek, T. Schram, E. Augendre, J.-F. de Marneffe, K. Devriendt, S. Brus, K. Henson, and S. Biesemans, “Demonstration of fully Ni-silicided metal gates on HfO_2 based high-K gate dielectrics as a candidate for low power application,” in *Symp. on VLSI Tech.*, pp. 190-191, 2004.

[6.4] T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita, M. Ohno, H. Ota, N. Yasuda, A. Ogawa, K. Tominaga, H, Satake, and A. Toriumi, “Partial silicides technology for tunable work function electrodes on high-K gate dielectrics -Fermi level pinning controlled $PtSi_x$ for $HfO_x(N)$ pMOSFET-,” in *IEDM Tech. Dig.,* pp. 83-86, 2004.

[6.5] A. Veloso, K. G. Anil, L. Witters, S. Brus, S. Kubicek, J.-F. de Marneffe, B. Sijmus, K. Devriendt, A. Lauwers, T. Kauerauf, M. Jurczak, and S. Biesemans, “Work function engineering by FUSI and its impact on the performance and reliability of oxynitride and Hf-silicate based MOSETs,” in *IEDM Tech. Dig.,* pp. 855-858, 2004.

[6.6] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hedge, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part I," and "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *IEEE Trans. Electron Dev*., vol. 51, pp. 971-984, June. 2004.

[6.7] C. S. Park, B. J. Cho, W. S. Hwang, W. Y. Loh, L. J. Tang, and D.-L. Kwong, "Dual metal gate process by metal substitution of dopant-free polysilicon on high-K dielectric" in *Symp. on VLSI Tech*., 4A-4, 2005.

[6.8] E. Cartier, V. Narayanan, E. P. Gusev, P. Jamison, B. Linder, M. Steen, K. K. Chan, M. Frank, N. Bojarczuk, M. Copel, S. A. Cohen, S. Zafar, A. Callegari, M. Gribelyuk, M. P. Chudzik, C. Cabral Jr., R. Carruthers, C. D'Emic, J. Newbury, D. Lacey, S. Guha, and R. Jammy, "Systematic study of pFET Vt with Hf-based gate stacks with poly-Si and FUSI gates," in *Symp. on VLSI Tech*., pp. 44-45, 2004.

[6.9] K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki, "Dual workfunction Ni-silicide/HfSiON gate stacks by phase-controlled full-silicidation (PC-FUSI) technique for 45 nm-node LSTP and LOP devices," in *IEDM Tech. Dig.,* pp. 91-94, 2004.

[6.10] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whoang, S. Mathew, L. K. Bera, N. Balasubramanian, and D.-L. Kwong, "Formation of Hafnium-Aluminum-Oxide gate dielectric using single cocktail liquid source in

MOCVD process", *IEEE Trans. Electron Dev*., vol. 50, no.10, pp. 2088-2094, Oct. 2003.

[6.11] K. Xiong, P. W. Peacock, and J. Robertson, "Fermi-level pinning and Hf-Si bonds at HfO2: Polycrystalline silicon gate electrode interfaces," *Appl. Phys. Lett.*, vol. 86, 012904, 2005.

[6.12] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *J. Appl. Phys.*, vol. 92, pp. 7266-7271, Dec. 2002.

[6.13] M. S. Joo, B. J. Cho, N. Balasubramanian, and D.-L. Kwong, "Thermal instability of effective work function in metal/high-K stack and its material dependence," *IEEE Electron Device Lett.*, vol. 25, pp. 716-718, 2004.

CHAPTER 7

CONCLUSIONS

7.1 SUMMARY AND CONCLUSIONS

With the continuous scaling of complimentary metal-oxide semiconductor (CMOS) devices, the high-K gate dielectric and metal gate stack is required for future CMOS devices with 65 nm technology node and beyond. Among the various high-K gate dielectric candidates, Hf-based high-K gate dielectrics have been extensively studied as the alternatives to SiO_2 or SiON. HfO_2 itself may cause several issues for the implementation in the advanced CMOS device due to the poor thermal stability of the film and the interfacial layer growth during subsequent thermal processes. The incorporation of foreign atoms into HfO_2 film such as Al, Si, N, etc. has been attempted to alleviate these issues in this decade. In addition, the interaction between high-k dielectric and gate electrode may cause the poor threshold voltage (V_t) control of MOSFETs. In this thesis, a new process method for Al incorporation into HfO_2 as one of the suitable techniques for mass production in terms of process simplicity and reproducibility is demonstrated and the interactions between high-k dielectrics and metal gates are investigated.

As the new process method, HfAlO film deposition by metal-organic chemical vapor deposition (MOCVD) using a single cocktail liquid source $HfAl(MMP)_2(OiPr)_5$

is demonstrated in Chapter 3. A wide range of composition controllability between HfO_2 and Al_2O_3 in HfAlO is obtained using this method. It is found that the deposition temperature plays a major role in the composition ratio control. Higher temperature deposition introduces more hafnium into the film but there is a turn-around point of the composition ratio at the deposition temperature of 450ºC where the HfO_2 percentage is maximum of around 90% (Al_2O_3 10%). The effect of the composition ratio between HfO_2 and Al_2O_3 on the electrical properties of the film is also investigated. The HfAlO film with 90% HfO_2 (10% Al_2O_3), which has minimum sacrifice of K value (around 19), shows a great improvement in thermal stability and significant reduction of interfacial layer growth during subsequent thermal processes, leading to the reduction in leakage current by around 2 orders of magnitude compared to pure HfO_2 film. The HfAlO film with 90% HfO_2 also shows good compatibility with TaN metal gate electrode, under high temperature annealing process.

The various interactions between high-k dielectrics and metal gates are described in Chapter 4, 5, and 6. In Chapter 4, thermal instability of effective work function ($\Phi_{m,eff}$) and its material dependence on metal gate/high-K dielectric stack are investigated. Although the MIGS theory with intrinsic interface states is applicable to predict the $\Phi_{m,eff}$ value of metal nitride/HfAlO gate stack before high temperature process, this theory is not applicable due to thermal instability of $\Phi_{m,eff}$ owing to the generation of substantial amount of extrinsic interface states at the metal/dielectric interface after high temperature RTA. It is found that the presence of silicon and its location at the interface plays a major role in the modification of $\Phi_{m,eff}$ after annealing. The behavior of $\Phi_{m,eff}$ has been explained with the types and locations of extrinsic interface states which are generated by silicon-metal bonds during high temperature annealing.

In Chapter 5, a new approach to analyze and predict the behavior of $\Phi_{m,eff}$ in fully silicided (FUSI) gate/high-K dielectric stack and its interface configuration is proposed, using the combination of semi-empirical approach and MIGS theory. It is found that FUSI gate has effectively MSi_2 configuration at the gate dielectric interface. FUSI gate on high-K dielectric is evaluated to have much weaker Fermi-level pinning compared to polysilicon gate on high-K, providing that metal film is sufficiently thick compared to polysilicon before silicidation anneal.

New findings on the Fermi-level pinning phenomenon in FUSI gate/high-K dielectric stack are discussed in Chapter 6, focusing on process condition and material composition dependence of Fermi-level pinning which is essential information for the successful implementation of FUSI gate on high-K gate dielectrics. It has been found that there is a critical composition ratio (C_{crit}) of Ni to Si in Ni-FUSI gate which starts to show a strong Fermi-level pinning. The C_{crit} is also found to be dependent on the underlying gate dielectric material. Since such behavior is believed to be due to the Hf-Si formation at the interface, the control of the amount of Si at the interface is a critical factor for the successful implementation of FUSI gate on high-K gate dielectric.

APPENDIX – List of Publications

Journal Papers

1. **M. S. Joo**, B. J. Cho, C. S. Park, N. Balasubramanian, and D.-L. Kwong, "Interface configuration and Fermi-level pinning of fully silicided (FUSI) gate and high-K dielectric stack," *J. Vacuum Science Technology B*, Vol. 24, No. 3, pp. 1341-1343, 2006.

2. Y. N. Tan, W. K. Chim, W. K. Choi, **M. S. Joo**, B. J. Cho, "Hafnium Aluminum Oxide as Charge Storage and Blocking-Oxide Layers in SONOS-Type Nonvolatile Memory for High-Speed Operation," *IEEE Transactions on Electron Devices*, Vol. 53, No. 4, pp. 654-662, 2006.

3. **M. S. Joo**, B. J. Cho, N. Balasubramanian, and D.-L. Kwong, "Stoichiometry dependence of Fermi-level pinning in fully silicided (FUSI) NiSi gate on high-K dielectric," *IEEE Electron Device Letters*, Vol. 26, No. 12, pp. 882-884, 2005.

4. W. Y. Loh, B. J. Cho, **M. S. Joo**, M. F. Li, S. Matthew, D. S. H. Chan, D. L. Kwong, "Charge trapping and breakdown mechanism in HfAlO/TaN gate stack analyzed using carrier separation," *IEEE Dev. Material Reliab.,* Vol. 4, No. 4, pp.696-703, 2005.

5. **M. S. Joo**, B. J. Cho, N. Balasubramanian, D.-L. Kwong, "Thermal instability of effective work function in metal/high-k stack and its material dependence," *IEEE Electron Device Letters*, Vol. 25, No. 11, pp. 716-718, 2004.

6. C. C. Yeo, **M. S. Joo**, B. J. Cho, and S. J. Whoang, "Effect of annealing on the composition and structure of HfO_2 and nitrogen-incorporated HfO_2," *Thin solid films,* Vol. 462-463, pp. 90-95, 2004.

7. S. Mathew, L. K. Bera, N. Balasubramanian, **M. S. Joo**, B. J. Cho, "Channel mobility degradation and charge trapping in high-k/metal gate NMOSFETs," *Thin solid films,* Vol. 462-463, pp. 11-14, 2004.

8. N. Balasubramanian, L. K. Bera, S. Mathew, N. Balasubramanian, V. Lim, **M. S. Joo**, B. J. Cho, "Wet etching characteristics and surface morphology evaluation of MOCVD grown HfO_2 film," *Thin solid films,* Vol. 462-463, pp. 101-105, 2004.

9. **M. S. Joo**, B. J. Cho, C. C. Yeo, D. S. H. Chan, W. S. Jin, S. Mathew, L. K. Bera, N. Balasubramanian, D.-L. Kwong, "Formation of Hafnium-Aluminum-Oxide gate dielectric

using single cocktail liquid source in MOCVD process," *IEEE Transactions on Electron Devices*, Vol. 50, No. 10, pp. 2088-2094, 2003.

10. C. C. Yeo, B. J. Cho, **M. S. Joo**, S. J. Whoang, D. L. Kwong, L. K. Bera, S. Mathew, and N. Balasubramanian, "Improvement of electrical properties of MOCVD HfO_2 by multi-step deposition process," *Electrochemical and Solid-State Letters*, Vol. 6, No. 11, pp. F42-F44, November 2003.

11. **M. S. Joo**, B. J. Cho, C. C. Yeo, N. Wu, H. Y. Yu, C. X. Zhu, M. F. Li, D.-L. Kwong, "Dependence of chemical composition ratio on electrical properties of HfO_2-Al_2O_3 gate dielectric," *Japanese Journal of Applied Physics*, vol. 42, pp. L220-L222, March 2003.

12. H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, **M. S. Joo**, D.-L. Kwong, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si", *Applied Physics Letters*, Vol. 81, No. 2, pp. 376, July 2002.

Conference Papers

1. **M. S. Joo**, B. J. Cho, N. Balasubramanrian, and D.-L Kwong, "Role of Si in Fermi-level pinning phenomena in metal/high-K gate stack," *Int. Conf. on Materials for Advanced Technologies (ICMAT-2005)*, MRS, Singapore, 2005.

2. **M. S. Joo**, B. J. Cho, D. Z. Chi, N. Balasubramanrian, and D.-L Kwong, "Behavior of effective work function in metal/high-K gate stack under high temperature process," *Int. Conference on Solid State Devices & Materials (SSDM)*, Tokyo, Japan, pp. 202-203, Sept, 2004.

3. Y. N. Tan, W. K. Chim, W. K. Choi, **M. S. Joo**, T. H, Ng, and B. J. Cho, "High-k HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation," *IEDM Tech. Dig*., pp. 889-892, 2004.

4. W. Y. Loh, B. J. Cho, **M. S. Joo**, M. F. Li, S. Matthew, D. S. H. Chan, D.-L. Kwong, "Analysis of charge trapping and breakdown mechanism in high-K dielectrics with metal gate electrode using carrier separation", *IEDM Tech. Dig*., 2003.

5. **M. S. Joo**, B. J. Cho, C. C. Yeo, Y. L. Ching, W. Y. Loh, S. J. Whoang, S. Mathew, L. K. Bera, N. Balasubramanian, and D. L. Kwong, "Physical and electrical properties of

MOCVD $HfAl_xO_y$ gate dielectric and their composition ratio dependence," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

6. C. C. Yeo, **M. S. Joo**, B. J. Cho, S. J. Whang, D. L. Kwong, L. K. Bera, S. Mathew, N. Balasubramanian, "MOCVD HfO_2 gate dielectric deposited by liquid delivery system and bubbler system using multi-step deposition technique," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

7. H. Y. Yu, N. Wu, C. Yeo, **M. S. Joo**, M. F. Li, C. Zhu, B. J. Cho, D. L. Kwong, "ALD $(HfO_2)_x(Al_2O_3)_{1-x}$ high-K gate dielectrics for advanced MOS devices application," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

8. S. Mathew, L. K. Bera, N. Balasubramanian, **M. S. Joo**, and B. J. Cho, "Channel mobility behaviour in high-K/metal gate NMOSFETs," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

9. M. Balasubramanian, L. K. Bera, S. Mathew, V. Lim, **M. S. Joo**, and B. J. Cho, "Wet etching characteristics and surface morphology evaluation of MOCVD grown HfO_2 film," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

10. N. Wu, C. X. Zhu, N. Balasubramanian, C. C. Yeo, **M. S. Joo**, H. Y. Yu, Q. C. Zhang, L. K. Bera, B. J. Cho, M. F. Li, S. J. Whoang, "Electrical and Physical Properties of $Si_{1-x}Ge_x/HfO_2/Si$ MOS capacitors," *2nd International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 2003.

11. **M. S. Joo**, B. J. Cho, C. C. Yeo, S. J. Whoang, S. Matthew , L. K. Bera, N. Balasubramanian, D.-L. Kwong, "MOCVD $HfAl_xO_y$ Gate Dielectrics Deposited Using Single Cocktail Liquid Source," *Int. Conference on Solid State Devices & Materials (SSDM)*, Tokyo, Japan, Sept, 2003.

12. C. C. Yeo, B. J. Cho, **M. S. Joo**, S. J. Whoang, D.-L. Kwong, L. K. Bera, S. Mathew, and N. Balasubramanian, "Improving Electrical Properties of CVD HfO_2 by Multi-Step Deposition and Annealing in a Gate Cluster Tool," *2003 Int. Conference on Solid State Devices & Materials (SSDM)*, Tokyo, Japan, Sept, 2003.

13. C. S. Fong, V. L. S. Wei, R. G. Krishnam, A. Trigg, L. K. Bera, S. Mathew, N. Balasubramanian, **M. S. Joo**, C. C. Yeo, and B. J. Cho, "Growth and characterization of

hafnium oxide thin films prepared by MOCVD," *2003 International conference on Characterisation and Metrology for ULSI technology*, Austin, USA, March 2003.

14. W. Y. Loh, B. J. Cho, M. F. Li, C. M. Lek, Y. F. Yong and **M. S. Joo**, "Correlation between interface traps and gate leakage in ultra-thin silicon dioxide (20A)" *Proceedings of 9th IPFA*, pp. 246, July 2002, Singapore.