FORMATION OF ADVANCED GATE STACKS AND THEIR APPLICATION TO NANO STRUCTURE DEVICES

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Abstract

It has been forecasted that continuous scaling down of complementary metal-oxide semiconductor (CMOS) devices and nonvolatile memory (NVM) devices will meet significant challenges soon, especially in gate stack scaling. If these devices are to be still fabricated on planar substrates, it is very likely that a gate stack structure consisting of high-K dielectric and metallic conductor will be required. In this thesis, physical and chemical mechanisms on the formation of advanced gate stacks for the future nano-scale planar CMOS and NVM devices are explored.

Plasma etching and wet removal properties of Hf based high-K gate dielectrics including HfO_2, $(HfO_2)_x(Al_2O_3)_{1-x}$, HfO_xN_y and $Hf_xSi_{1-x}O_2$ were investigated. It was found that the crystallized HfO_2 phase is the main reason for the rapid decrease of the wet etch rate of Hf based high-K dielectrics after anneal. Plasma treatment with low ion energy of several hundred eV can destroy the crystalline structure, resulting in a large increase of etch rate. The plasma etch rate varied depending on the chemical components in the Hf based high-K dielectrics. The composition of the residue was confirmed by x-ray photoelectron spectroscopy (XPS) and time-of-fight secondary ion mass spectroscopy (TOF-SIMS) and the amount of residue was consistent with the volatile points of the etch by-products. High temperature was effective in reducing the amount of etch residues of Hf based high-K dielectrics.

Plasma etching properties of advanced gate materials including poly-SiGe was studied using inductively coupled plasma of $HBr/Cl_2/O_2$. Results show that etch rate of these materials increases rapidly with increasing ion density and energy. Improvement of etch selectivity can be achieved by adding a small amount of O_2, reducing ion energy and increasing pressure. Notching can be controlled by varying the etching process parameters of inductive power, rf bias power, and pressure, as

well as by varying the Ge concentration in poly-SiGe. Optical emissions in various wavelength bands from poly-SiGe etch byproducts were identified, providing sharp etch end point signal.

Formation of Ge nanocrystals (NCs) embedded in HfAlO high-K dielectric was studied for NVM applications. Thermodynamics of the formation mechanism was revealed by XPS analysis. Physical characterization shows a good thermal stability of Ge-NCs in HfAlO. A self-assembly technique of Al_2O_3 nanodots (NDs) on SiO_2 has also been developed by employing a two-step controlled annealing method to suppress lateral migration of electrons via Frenkel-Poole tunneling. Two novel NVM structures and corresponding CMOS compatible process have been realized based on the techniques developed above. Electrical characterization shows that low voltage programming and reliable multi-bit storage can be achieved by the NVM devices using Ge NCs embedded in HfAlO high-K dielectric and Al_2O_3 NDs embedded in SiO_2, respectively.

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Chapter 1

Introduction

1.1 The Challenge of Moore's Law

Nowadays, electronic products have become key elements in human society. Look around, computers, cell phones and internet are influencing every aspect of our life significantly. At the same time, electronic technologies are supporting the progress in other traditional industries and new technologies aggressively. All these cannot occur without the consistently improving and more and more cost effective Very Large Scaled Integrated (VLSI) circuits made of silicon devices.

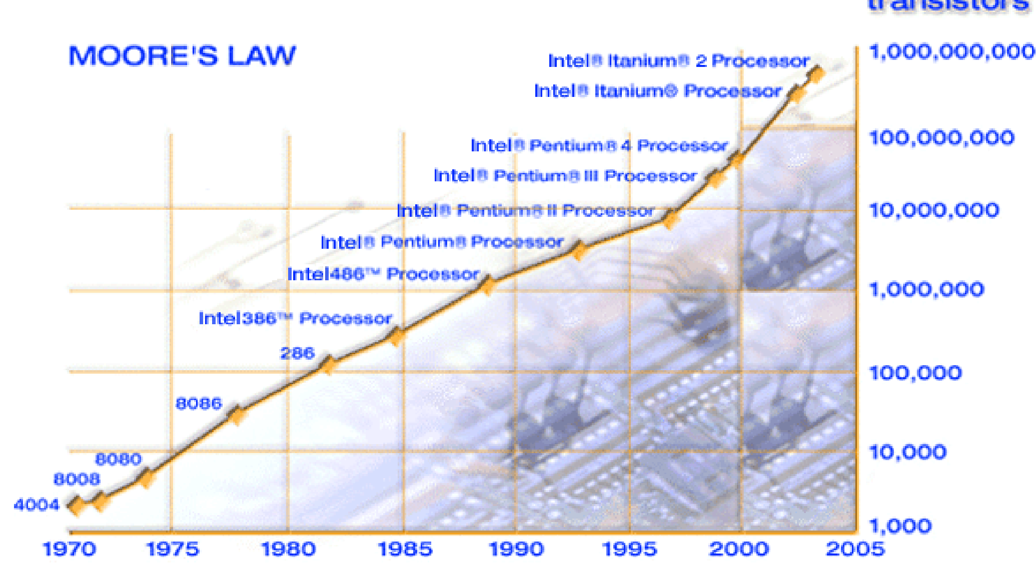


Fig. 1.1 Moore's law in the past 20 years: the number of the transistors on a chip as the function of year. Source: *http://www.intel.com/research/silicon/mooreslaw.htm*.

The improvement of performance and reduction of the price for silicon devices are accomplished by scaling the feature size of devices, following the well

known Moore's law [1.1], which predicts that the number of transistors per integrated circuit would double every 18 months, as shown in Fig. 1.1.

Metal Oxide Semiconductor Field effect Transistors (MOSFETs) (shown in Fig. 1.2) are elemental devices in logical circuits. Its gate length after gate stack etching is regarded as the feature size of the device.

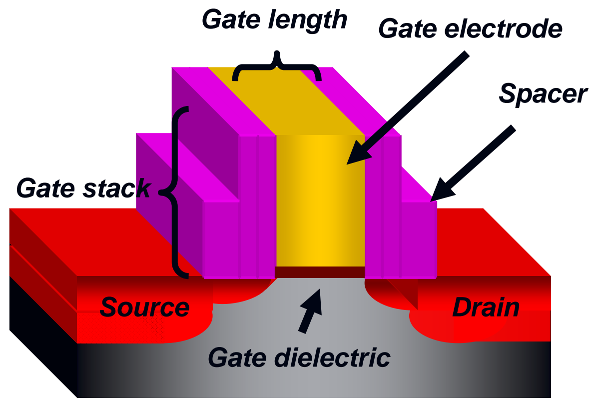


Fig. 1.2 Schematic of a MOSFET.

For high performance MOSFETs, gate length is also regarded as the technology node representing the generation of the VLSI technologies. In 1972, the technology node was about 8 μm; today, MOSFETs with 90 nm (0.09 μm) feature size [1.2, 1.3], which is about one in a thousandth of the human hair, have been in mass production in the leading-edge industries. This has resulted in both the reduction in t price per function and thousands times increase in speed!

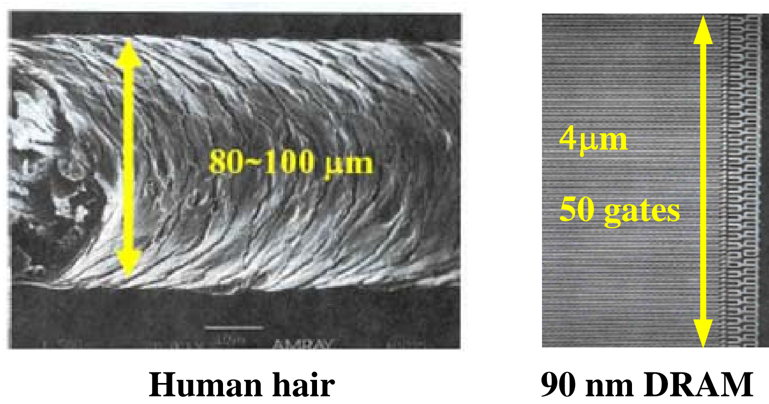


Fig. 1.3 Local images of a human hair and a DRAM of 90 nm technology.

Other silicon devices, such as dynamic random access memory (DRAM) and non-volatile memory (NVM), which is mainly flash electrically erasable programmable read-only memories (flash EEPROMs or flash memories) are scaling at about the same speed as MOSFETs [1.2, 1.3]. Previously, the technology node of flash memories was always delayed for one or half generation behind comparing with high performance MOSFETs because of process issues and the maturity of market. Recently, their scaling speeds have almost been synchronous with the MOSFETs because of the tremendous increase of the demand from mobile applications and digital cameras. This has resulted in the drastic increase of memory density and the reduction of cost per bit in the past few years.

However, the further scaling down of MOSFETs and flash memories introduces new challenges, as indicated in the International Technology Roadmap for Semiconductors (ITRS) 2003-2004 update [1.2, 1.3].

For MOSFETs, the challenges mainly come from large gate leakage current, as shown in Fig. 1.4, high contact resistance and reliability of low-k interconnect dielectrics. Among these challenges, *"in no area is this issue more clear or urgent than in the MOSFET gate stack"* [1.2]. When gate length is scaled, the gate dielectric thickness must be reduced consequently to maintain the performance of transistors, as shown in Fig. 1.4. When the gate length is 65 nm, *i.e.* the technology node of 2007, the gate dielectric thickness will be about 0.9 nm, which is about the thickness of 2-3 SiO_2 molecule layers [1.4]. With this thickness, SiO_2 will meet the physical limitation in electrical insulation, the high direct tunneling current. This is because high direct tunneling current is not able to meet the requirement of MOSFETs for some applications [1.2, 1.3].

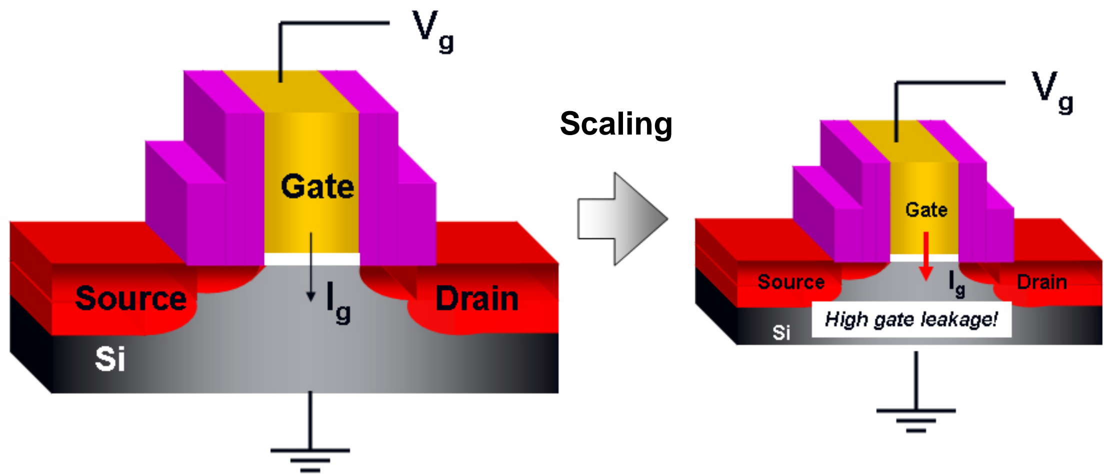


Fig. 1.4 Illustration of scaling of MOSFETs.

For flash memories, scaling down of the devices also requires continuous reduction of thickness of both the tunneling dielectric layer and control dielectric layer (interpoly oxide) in the gate stack to improve the program/erase performance and reduce the operation voltage. But, both dielectric layers must be thick enough to ensure the required charge retention of 10 years as the requirement of nonvolatile flash memories. The current technologies, mainly based on thermal and chemical vapor deposited oxynitrides/nitride for both dielectrics, are not expected to satisfy the aforementioned dielectric scaling needs, thus the implementation of new technologies or new materials is required [1.2, 1.3, 1.5].

In summary, from the angle of front-end process, the gate stack scaling is the main issue in the scaling of both MOSFETs and flash memories.

1.2 Scaling Gate Stacks of MOSFETs: Approaches and Challenges

1.2.1 Approaches of scaling MOSFETs' gate stack and improving performances

Scaling of MOSFETs can increase the transistor density on the chip and reduce the cost per function. In 1970's, in the initial stage of scaling MOSFETs, a scaling strategy was proposed by Dennard *et. al.* [1.6]. This scaling approach is illustrated in Fig. 1.5, where the scaling factor is α. It can be found that in this approach, the dimension, doping, and voltages were scaled in the same proportion, hence the electrical field is constant. This strategy is called "Constant-Electrical Field Scaling".

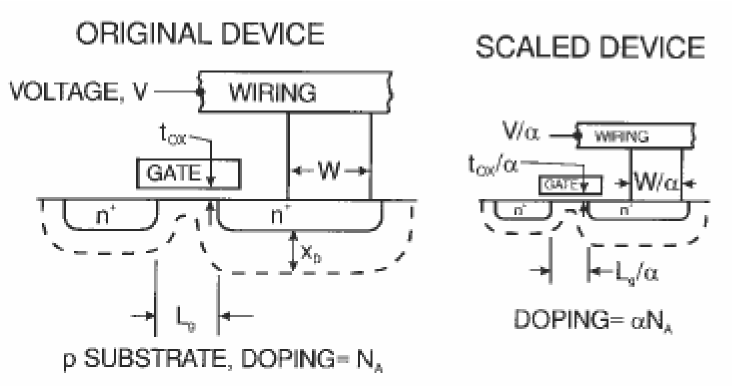


Fig. 1.5 Schematic illustration of the scaling of silicon technology by a factor *α* [1.6].

However, the performance, such as built-in potentials and subthreshold slope which are determined by the inherent properties of materials, does not change or improve using this approach. At the same time, the on-current is more and more

close to the off-current because of the continuous scaling of the voltage. To solve the small on-current problem, an additional scaling factor ε (ε>1) is applied to the scaling voltages. Consequently the doping concentration must be increased by ε times to maintain the same depletion regions, resulting in higher allowed voltage. This scaling strategy is called as "Generalized Scaling". A disadvantage of this strategy is that the electrical field is increased with the scaling, resulting in reliability concern.

Table 1.1 Scaling parameters for Constant-Electrical Field Scaling, Generalized Scaling and Generalized Selective Scaling.

MOSFET's Device and Circuit parameters	Constant-Electrical Field Scaling	Generalized Scaling	Generalized Selective Scaling
Channel Length, Gate Dielectric Thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring Width, Channel Width	$1/\alpha$	1	$1/\alpha_w$
Electric Field	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
Doping	α	$\varepsilon\alpha$	α_d
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate Delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power Dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^3/\alpha_w\alpha_d$
Power Density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

(α_d is the Gate Length and Vertical Scaling Factor, α_w is Gate Length and Wiring Scaling Factor and ε is Electrical Factor)

Actually, the scaling of the gate length and wiring (gate width) of devices can be dependent on different factors, α_d and α_w, summarized as "Generalized Selective scaling". In the Table 1.1 the scaling parameters for Constant-Electrical Field Scaling, Generalized Scaling and Generalized Selective Scaling are summarized. With Generalized Selective Scaling, the MOSFETs can be scaled more aggressively.

It can be found that in Table. 1, gate dielectric thickness must be correspondingly scaled down with the gate length. This is for maintaining the effectiveness of the gate in device operation.

Besides the increase of transistor density, another advantage brought by scaling is the improvement of transistor performance. Pursuing a higher drive current (I_D) (drain current) is one of the key aspects for improving the performance of MOSFETs, because a higher speed requires a higher I_D. A simple model of the drive current can be written using the gradual channel approximation as [1.7]:

$$I_D = (W/L_g)\,\mu\, C_{inv}\,(V_G - V_{th} - V_D/2)V_D \qquad (1\text{-}1)$$

where W is the width of the transistor channel, L_g is the channel length, μ is the channel carrier mobility; we assume that it is a constant here; C_{inv} is the capacitance density when the channel is biased in the inversion region; V_D and V_G are the voltages applied to the gate and drain of the MOSFETs, respectively; and the threshold voltage is given by V_{th}.

This equation is valid in the region of V_D, of which is smaller than $V_G - V_{th}$, where V_{th} is threshold voltage. When V_D exceeds $V_G - V_{th}$, I_D will saturate, expressed as:

$$I_D = (W/L_g)\,\mu\, C_{inv}\,(V_G - V_{th})^2/2 \qquad (1\text{-}2)$$

It can be found that a higher I_D can be acquired by a larger W, C_{inv}, and V_G or smaller L_g and V_{th}. The width W cannot be increased too much, as a larger W will result in a larger transistor area; L_g is limited by the lithography, of which the smallest is the technology node. The mobility μ is mainly determined by the properties of substrate materials; V_G cannot be too large, as a high V_G will induce a high electrical field across the gate dielectric, resulting in reliability problem and it is very hard to reduce the V_{th} down to 200 mV, as electrons' energy is 25 mV at room temperature [1.8].

Hence, to have a higher C_{inv} is very important to get a high I_D. Basically, C_{inv} consists of C_{ox} and C_{dep}, which are the gate dielectric capacitance density and Si substrate capacitance density, respectively. C_{dep} is mainly determined by the doping concentration of substrate. C_{ox} expressed as:

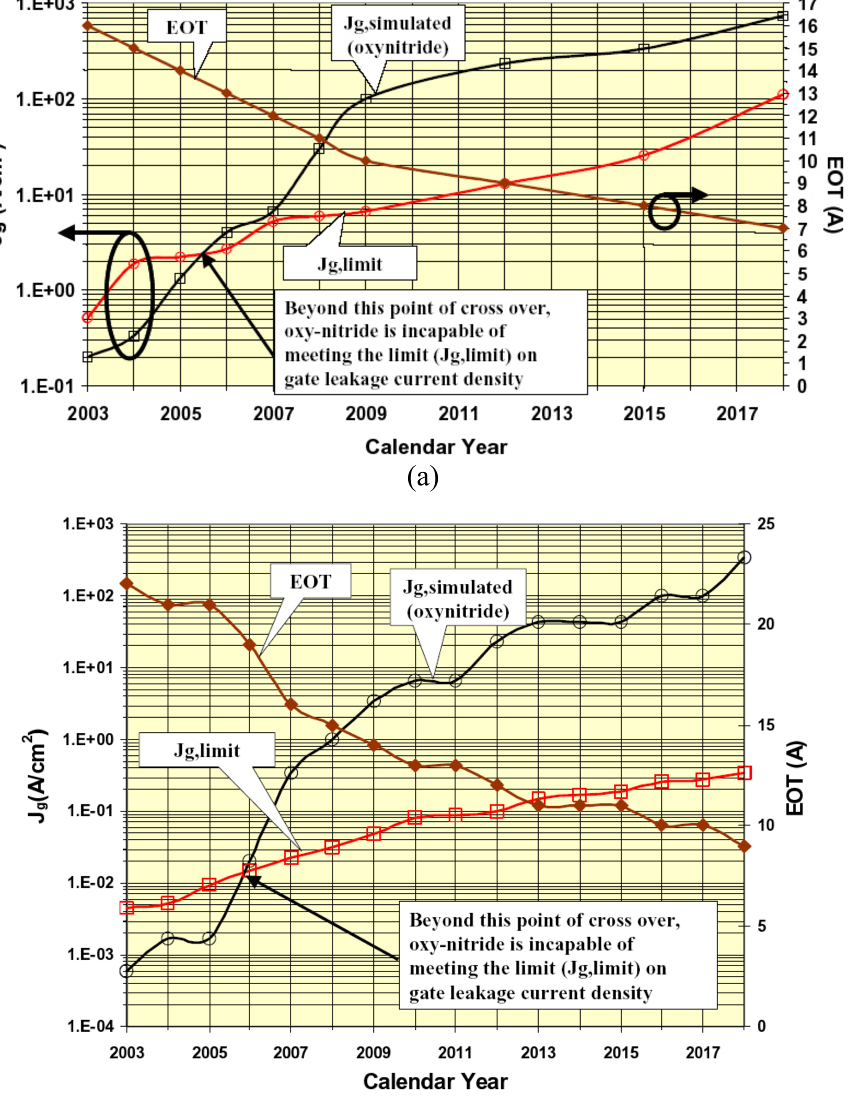
$$C_{ox} = \mathrm{K}\varepsilon_o/t_{ox} \qquad (1\text{-}3)$$

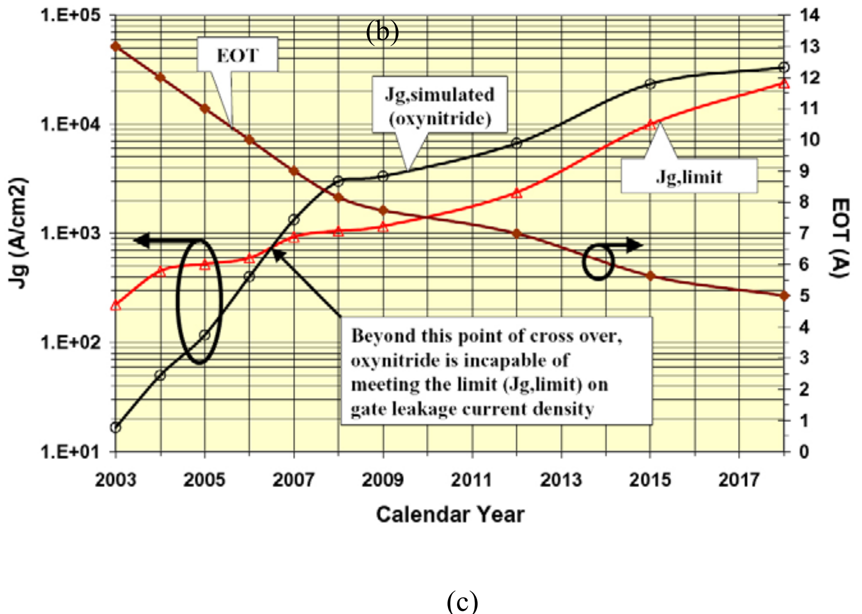
where K is the dielectric constant (the relative permittivity) of the gate dielectric, ε_o is the permittivity of free space (8.85 10-23 fF/ µm). It is obvious that increasing K or reducing t_{ox} can increase C_{ox}.

1.2.2 Limitation of SiO_2 and Si oxynitride as gate dielectric

Although many different oxides have been available for IC application, thermal grown SiO_2 and nitrided SiO_2 (Si oxynitride or SiO_xN_y) have been the most used gate dielectrics for MOSFETs in the past 30 years. This is because they satisfy most requirements of gate dielectrics such as thermal stability, good electrical performances, simple and cheap process. In 1979, the typical gate oxide thickness

was 25 nm; nowadays, 1.3 nm thickness gate oxide is in production. According to ITRS 2004, 0.9 nm equivalent oxide thickness (EOT: for a gate dielectric of thickness T_d and relative dielectric constant K, EOT is defined by EOT = T_d / (K / 3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. [1.3])) is needed for 65 nm technology node and operating gate leakage of less than 9.3×10^2 A/cm^2 is required at the same time. However, the simulation result shows that the direct tunneling current through SiO_xN_y with such thickness has already exceeded the requirement of gate leakage of low operating power (LOP) devices, and subsequently, as well as low standby power (LSTP) devices and high performance (HP) devices one by one, as shown in Fig. 1.6.





(c)

Fig. 1.6 (a) LOP, (b) LSTP and (c) HP logic device scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling (*Source: ITRS 2004 update* [1.3]).

Improving N concentration in SiO_xN_y can increase the K value of SiO_xN_y, resulting in a larger allowed physical thickness and a lower leakage [1.4]. If Si is fully nitrided, *i.e.* Si_3N_4 (the K value is ~ 7.8), the scaling limits of its physical thickness is estimated to be ~ 1.2 nm [1.9], of which EOT is ~ 0.6 nm, considering the smaller band gap compared with SiO_2. Hence, further scaling of gate dielectrics will require new gate dielectrics with higher K values as long as current scaling strategy doesn't change.

1.2.3 High-K gate dielectrics: selection guidelines, candidate materials and integration issues

A. *Selection guidelines*

In the past few years, much work has been done to identify potential candidates, which can replace SiO_2 and SiO_xN_y with a substantially thicker dielectric to maintain a low leakage current while reducing the EOT. The primary objective is to find dielectric materials with a higher K value than SiO_2.

In addition to the dielectric constant, other properties of high-K dielectric films must be considered such as band gap, thermal stability, electrical leakage, and interface property. Table 1.2 shows some primary physical data of several main high-K materials, which are relative to the selection of high-K candidates [1.10].

Table 1.2 Comparison of relevant properties for high-K candidates [1.10].

Dielectric	Dielectric constant (K)	Gap energy (eV)	Electron barrier to Si (eV)
SiO_2	3.9	8.8	3.15
Si_3N_4	7.8	5.1	2.1
Al_2O_3	8 – 11.5	~6.5 - 8.7	~2.4 - 2.8
ZrO_2	22 – 28	~5.5 - 5.8	~1.4 - 2
$ZrSiO_4$	10 – 12	~6	1.5
HfO_2	25 – 30	~5.25 - 5.7	~1.5 - 1.9
$HfSiO_4$	~10	~6	1.5
TiO_2	~80	3.5	~1.2
Ta_2O_5	~25	~5	~0.3 - 0.5

B. Candidate materials

In the early days, aluminum oxide (Al_2O_3), titanium (TiO_2) and tantalum oxide (Ta_2O_5) were found to be the candidates. Al_2O_3 has favorable properties such as high conductance band offset with Si substrate, good thermal stability on Si substrate and retention of amorphous properties under high temperature annealing. But Al_2O_3 can only be a short-term solution because of its middle permittivity in the range of 8~11. In addition, it is reported that the diffusion of boron and phosphorous in Al_2O_3 is undesirably fast [1.4].

TiO_2 and Ta_2O_5 have also been studied widely because of their larger permittivity (TiO_2: ~80 and Ta_2O_5: ~26). But the low conductance band offset to Si substrate and thermal instability on silicon nullify the advantages of high permittivity. Many other materials, such as Y_2O_3 La_2O_3 Pr_2O_3, have also been discussed. But most of them are left out because of the considerations above [1.4].

Recently, hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) have drawn significant attention [1.4, 1.11-1.13] because of their high permittivity of ~25 and acceptable band gap, especially good thermal stability on Si substrate. Reduction of leakage current by orders of magnitude has been demonstrated using HfO_2 and ZrO_2. Currently, many studies are focusing on the improvement in the physical and electrical properties such as the thermal stability and the further reduction of gate leakage. The further comparison shows that HfO_2 seems more promising than $ZrO_{2,}$ mainly because of its better thermal stability on Si. After the further improvement of HfO_2, Hf based dielectric films such as Hf silicate [1.14-1.16], Hf oxynitride [1.17, 1.18], $(HfO_2)_x(Al_2O_3)_{1-x}$ (HfAlO) [1.19] and nitrided Hf silicate (HfSiON) [1.20,

121] have been developed and become the most promising candidates for future MOSFET's applications.

C. Integration Issues

Integration issues must be addressed to implement of high-K gate dielectrics. Crystallization of gate dielectrics can induce the degradation of film uniformity and result in reliability issues; hence it is desirable that the gate dielectric remains amorphous throughout the complementary metal oxide semiconductor transistor (CMOS) processing [1.4]. Interfacial layers between high-K gate dielectric and Si substrate as well as gate electrode are also important considerations. The presence of thick interfacial layers increases the EOT significantly. Gate dielectric must have low interface states density (D_{it}) as well as low bulk trap density.

In the past few years, these issues have been widely discussed [8, 11-19]; many approaches have been reported to improve the electrical performance of high-K dielectric. As mentioned before, Hf based high-K dielectrics have been recently identified as the leading candidates, because of their relevant high K values, good thermal stabilities and so on [1.14-1.21], as shown in Fig. 1.7.

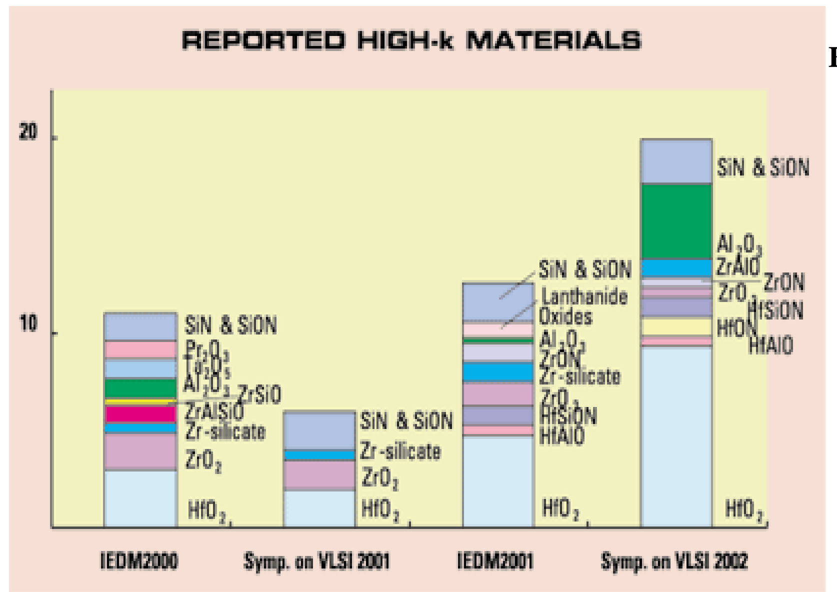


Fig. 1. 7 Comparison of numbers of research articles published on various high-K films in major conference on Si process technologies. Source: Solid State Technologies.

Although film methodology of Hf based high-K dielectrics have been discussed widely, there are few reports on the process integration issues of high-K dielectrics. This is partially because the electrical performance of high-K dielectrics available has not met the requirement of industry. Most recently, rapid scaling down of CMOS devices has pushed the SiO_2 and SiO_xN_y thickness down to the physical limitation of maintaining gate dielectric functions [1.2, 1.3], confirming the urgency of the needs for high-K dielectrics.

Etching processes including wet cleaning and plasma etching of high-K films, especially for Hf based high-K materials are largely unknown. In Fig. 1.8, the integration issues from the process step of gate stack etching to silicidation of gate stacks with Hf based high-K gate dielectrics are summarized.

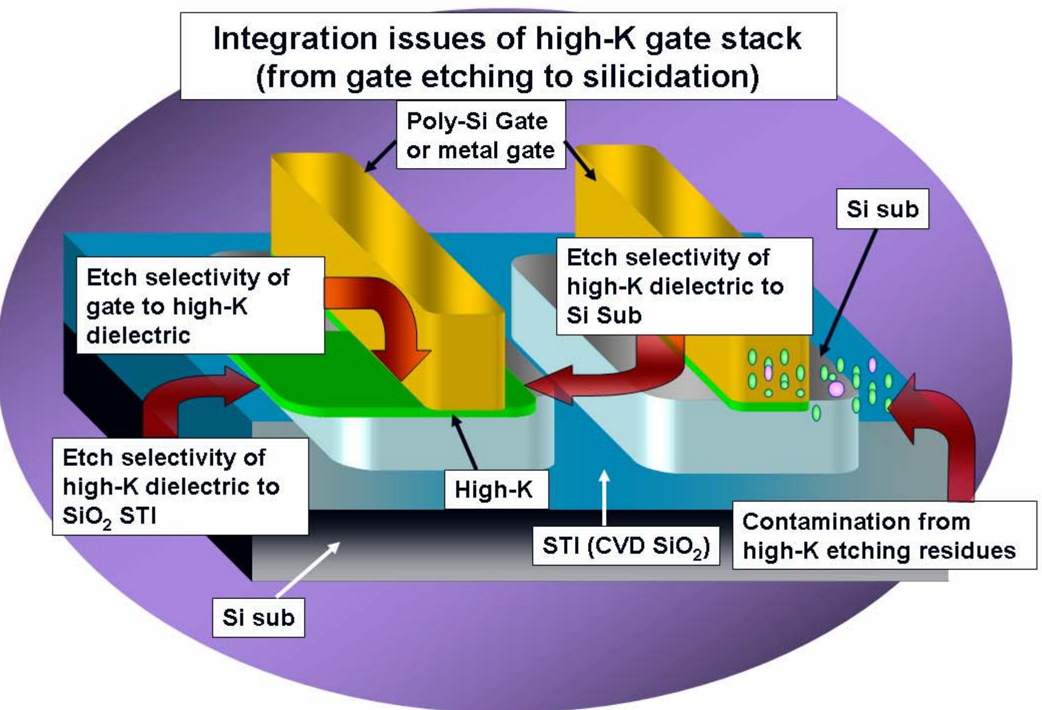


Fig. 1.8 Integration issues from gate stack etching to silicidation of gate stacks with Hf based high-K gate dielectrics.

At the same time, the data available of chemistry of Hf inorganic compounds is very limited because Hf has not been well studied extensively from the chemistry point of view, increasing the difficulty of development of suitable process. In the current front-end process, gate stack etching and cleaning recipes have been elaborately designed based on the poly-Si and SiO_xN_y stack, thus the implement of a new materials could change the whole process significantly. Therefore, implementing high-K gate dielectrics, especially Hf based high-K gate dielectrics, using conventional CMOS compatible process is a very big challenge.

1.2.4 Limitation of polycrystalline Si gate

When polycrystalline (poly-Si) is used for the gate electrodes of MOSFETs, the poly-Si depletion (many cases, simply called poly depletion) effect occurs when gate electrode is biased in inversion region [1.3, 1.22, 1.23], and as shown in Fig. 1.9 (a), this increases the EOT, resulting in the decrease of gate capacitance, as shown in Fig. 1.9 (b).

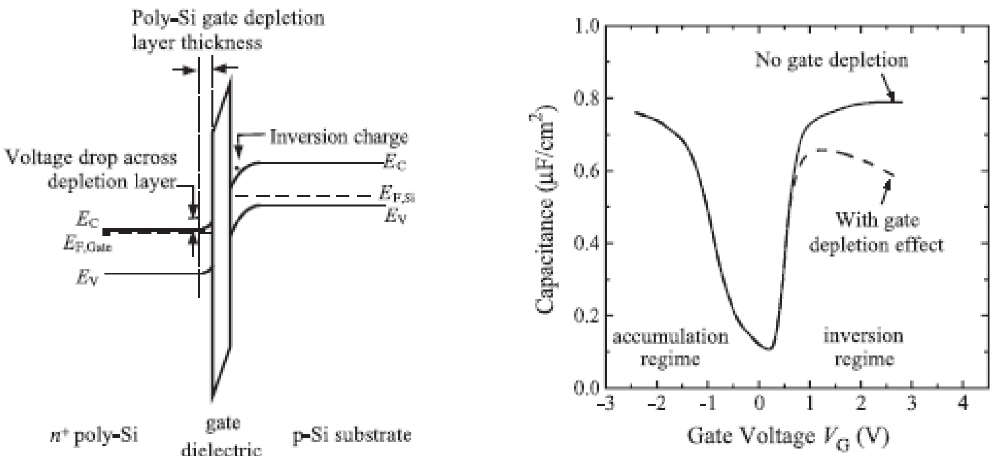


Fig. 1. 9 (a) An energy band diagram of a gate stack of an NMOS device in inversion region and (b) degradation of gate capacitance because of the poly depletion effect [1.22].

With the aggressive scaling of the gate dielectric thickness, the poly-Si depletion effect becomes much more significant [1.2, 1.3]. An increase of gate dielectric EOT of 4-6 Å due to the poly depletion effect is anticipated for any technology node. Considering that requirement of EOT is less than 1 nm for sub-45 nm technology nodes, it is obvious that the increase of EOT due to the poly depletion effect is very serious [1.3].

Increasing the doping concentration of the poly-Si gate can reduce the poly depletion effect. However, this is limited by the saturation of dopant density in *p*+ or *n*+ poly-Si [1.24]. On the other hand, increasing doping concentration worsens the dopant penetration problem [1.25]. Hence, metallic gate electrode materials, such as metals and metal silicides are needed to replace poly-Si.

1.2.5 Selection guidelines for new gate materials, candidate materials and integration issues

A. Selection guidelines

For various applications, the requirements of work functions are always the first priority. Metallic gate work functions of the *n*+ and *p*+ poly-Si close to the conduction band and valence band edges of Si (work functions are around 5.1 eV and 4.0 eV respectively) are preferred for the optimal design of bulk NMOS and PMOS devices, respectively [1.26]. It is also known that thin body fully depleted silicon on insulation (FD-SOI) and fin field effect transistor (FinFET) typed devices need gate electrodes with work function of ~ 4.5 to make low channel doping viable

to eliminate channel mobility degradation and minimize the V_{th} variation [1.27].

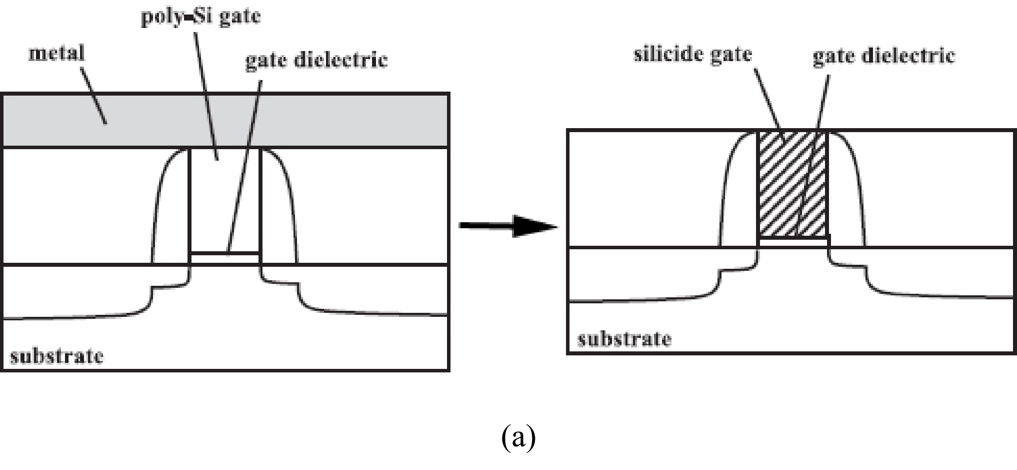
New gate must be thermally stable during device fabrication process. This means that materials of metal gate should not chemically change in the process environment. Furthermore, the reaction and diffusion of materials of metal gate materials with other materials in device, which are in directly contact with gate electrode, need to be minimized. The reaction between metal gate and gate dielectrics is one of the most serious concerns. The most common result of reaction of metal gate and gate dielectrics is the increase of the EOT.

In addition to the electrical requirements, new gate materials must have good adhesion onto gate dielectrics, and must be patternable using conventional lithography and etching process.

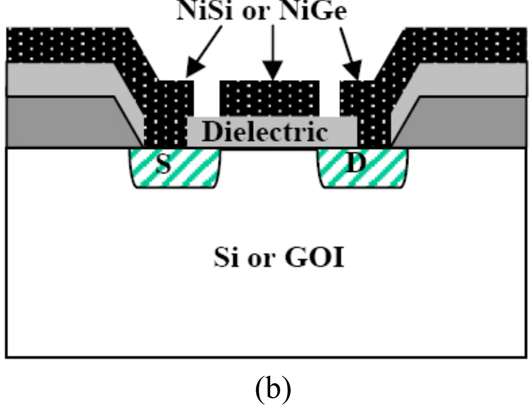
B. Candidate materials

Polycrystalline silicon germanium alloy (hereafter poly-SiGe) was found to have several advantages as a suitable gate electrode material to replace poly-Si [1.28]. In early years, poly-SiGe gates have been found to be effective in reducing poly depletion and boron penetration effects, and to provide controlled work functions by adjusting Ge concentrations.[1.29]. Recently, researchers found the further advantage using poly-SiGe: the thickness of interfacial layer between gate and gate dielectric can be significant suppressed compared with the case of using common poly-Si gate [1.30] when poly-SiGe is integrated with one of the main stream high-K dielectrics, *e.g.* HfO_2. In addition, poly-SiGe has been found to form notch gate more easily than poly-Si via plasma etching, and this can be another approach to scale down the gate length.

However, poly-SiGe may be only a short-term solution because poly depletion effect cannot be completely removed from poly-SiGe gates. Despite this, poly-SiGe still draws significant attention because the poly-SiGe process is almost compatible with the conventional CMOS process. Hence poly-SiGe still can be the choice material if other materials suitable for metal gates are unavailable. On the other hand, in fully silicided or germanided metal gate process, poly-Si, poly-Ge or poly-SiGe is still needed [1.31], the process flow of which is shown in Fig. 1.10 (a) and (b) [1.22]. Note that the fully silicided or germanided metal gate process is almost CMOS process compatible.



(a)



(b)

Fig. 1.10 (a) Main steps to form fully silicided metal gate metal deposition after formation of poly-Si (or poly-SiGe) gate and anneal to form silicide gate [1.22]. (b) Fully germanided NiGe gate [1.31].

Besides poly-SiGe, various metal gates materials and integration schemes are now being developed for the future CMOS devices [1.31-1.39]. As mentioned before, two gate electrodes of different work functions are needed for CMOS devices consisting of PMOS and NMOS, with work functions of around 5.1 eV and 4.0 eV [1.26, 1.34]. The work functions of some pure metals are around these two values. But most n-type metals (with work function of around 4.0 eV) are not suitable for being gates of MOS devices, because of their thermal instability or undesirable oxidation. P-type metals (with work function of around 5.1 eV) such as platinum and ruthenium are very stable, but not suitable for integrating into CMOS process because they are chemically too inert to process.

Among the metal nitrides, it was reported that some refractory metal nitrides such as TaN [1.36], TiN [1.37, 1.38], ZrN and HfN [1.39] might be suitable for microelectronic applications [1.40]. But none of them have been confirmed to be suitable as PMOS or NMOS gate because their work functions are thermally instable on SiO_2 or high-K dielectrics. After annealing, work functions of most of them shift to ~ 4.5 eV, which may be generally suitable only for FD-SOI and FinFET typed devices. Mo and MoN were reported as PMOS and NMOS gates respectively, and have been successfully demonstrated with several high-K materials including HfO_2, but their thermal stabilities were also not good enough [1.41].

As mentioned before, fully silicided metals used for dual metal gates have drawn attention due to their compatibility with conventional CMOS process. By incorporating some metals into poly-Si or poly-Ge, the poly depletion effect can be reduced or removed. Meanwhile, the work functions of these silicides can be tuned close to the values required for PMOS and NMOS by doping and alloying. However,

the tuning of work functions is not sufficiently large for dual-gate bulk CMOS application at this moment [1.41, 1.42].

Until now, no solution has been identified as suitable and stable metal gate materials for CMOS devices and process; therefore, continuous development and research of metal gate materials are needed.

C. *Integration Issues*

Similar to the progress of high-K gate dielectrics, the studies of new metal gate materials have mainly been focused on the selection of materials with proper work functions on dielectrics and film methodology. As the rapid scaling down of CMOS device, it was considered that metal gate electrodes will be required for 45 nm technology node, *i. e.*, year 2007 [1.2, 1.3]. It was reported that high-K gate dielectrics are preferred to couple with metal gates [1.43]; hence, integration studies should be performed simultaneously with the progress of selection of metal gate materials.

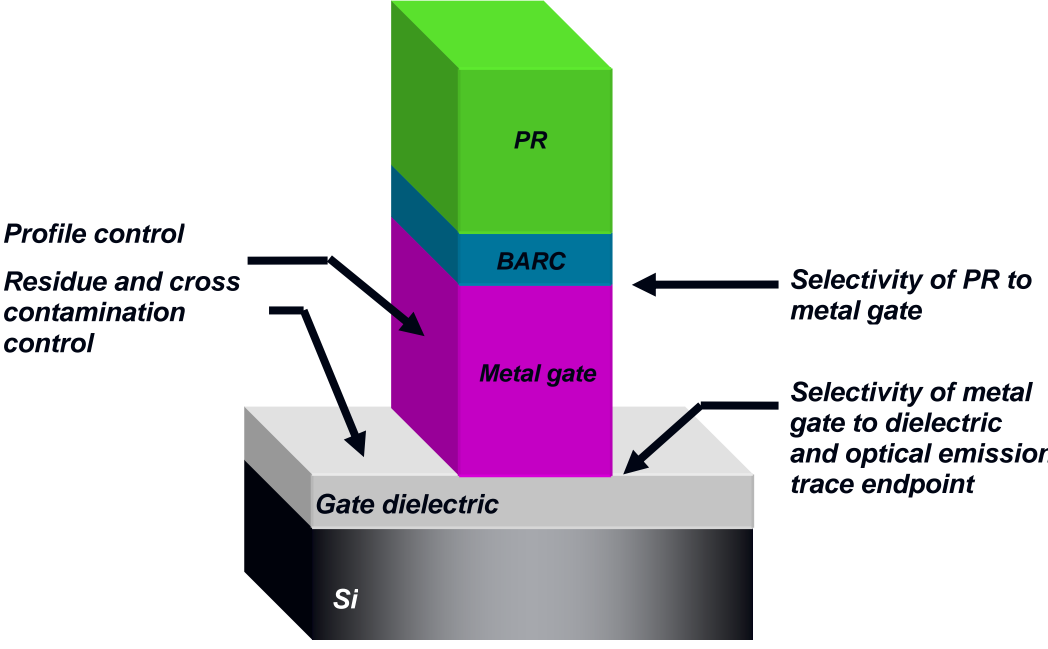


Fig. 1.11 Illustration of summary of integration issues of metal gates. (PR: Photoresist and BARC: bottom anti-reflection coating).

The challenges of etching new gate materials in CMOS device come from the extremely rigorous requirement of nano-scale process including critical dimension (CD) control, profile control, selectivity control, and capture of optical emission trace endpoint, as summarized in Fig. 1.11.

1.3 Scaling Gate Stacks of Flash Memory Devices: Approaches and Challenges

1.3.1 Architecture, device structure and operation of NOR and NAND arrays

Floating gate (FG) flash memories are now the biggest and the fastest growing segment in nonvolatile semiconductor memory area. In Fig. 1.12, a sketch of a typical FG transistor is shown, in which FG is fully insolated by surrounding oxide. Exchanging electrons between FG and channel and control gate takes place through tunneling and interpoly oxides, respectively.

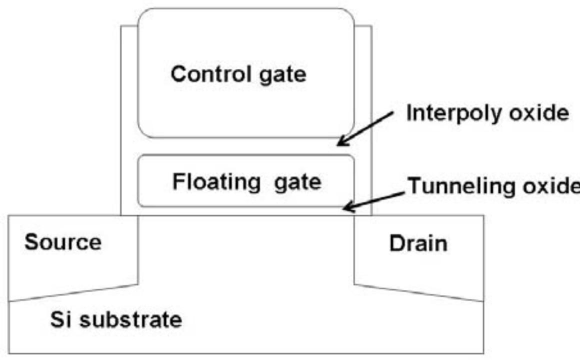


Fig. 1.12 A sketch of a typical FG flash memory transistor

A. Architecture of arrays

In FG flash memory segment, NAND and NOR are the two main types of array. NOR type flash memory is originated from erasable programmable read-only memory (EPROM) array [1.44], which is designed for fast random accessing each memory cell. The device structure of NOR flash memory is the same as that of the FG devices in the EEPROM cells, but the area of flash memory cell is about half of

EEPROM cell because block erase is used in flash memory arrays, hence that access transistor is saved; “flash” here means block rewritable [1.44].

In Fig. 1.13, the NOR array structure is shown. It can be observed that each FG transistor can be accessed directly. Hence random access time of each memory cell is quite short, favoring code reading.

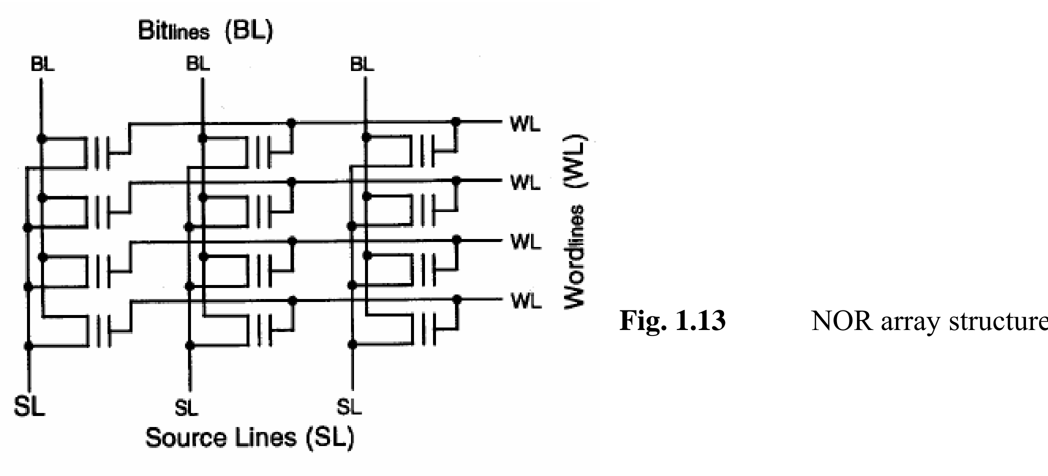


Fig. 1.13 NOR array structure

Generally, in devices such as basic cellular phones and personal digital assistant where code size is relatively small or where there is no performance requirement beyond what can be achieved with direct code execution, NOR flash memories are selected for its high random access speed (within 100 ns). However, due to the high cost and the large cell area, NOR flash memory is typically used with no requirement for storing large amounts of data.

NAND flash was developed a few years after the introduction of NOR. Its design of array emphasizes increased write performance (~10 times of NOR), higher density, and lower cost. Write performance improvements are achieved through a sector-oriented management of the flash and smaller size erase blocks compared with NOR arrays. Higher densities can be attained by using a smaller flash cell size. The scaled back cell size and the reduced pin count of NAND’s I/O interface contribute to a lower manufacturing cost. In Fig. 1.14, the NAND array structure is

shown. It can be found that the FG transistor must be only accessed one by one. Hence random access time of each memory cell is ~10 times longer than that of NOR arrays. However, in NAND arrays, the transistors are directly connected with each other with sources and drains, hence the contact area is saved, resulting in more compact structure than NOR arrays, reducing the cost per bit.

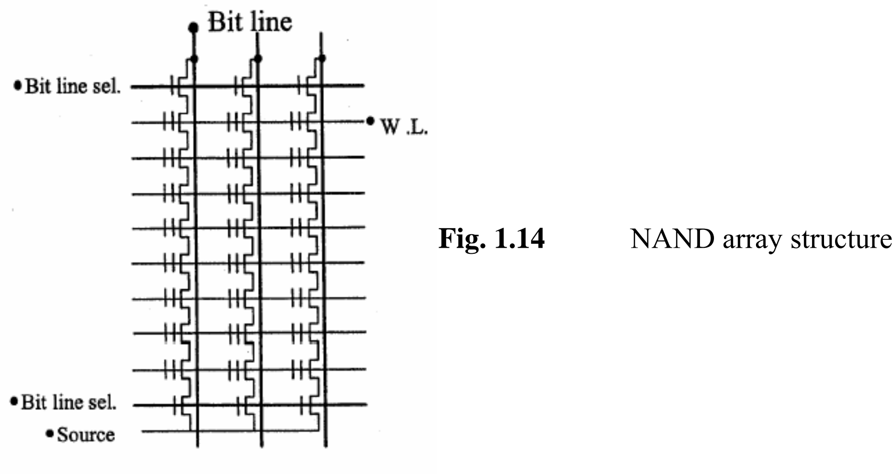


Fig. 1.14 NAND array structure.

B. Operation

The operation scheme depends on the architecture. In NOR array, because of the direct access of the memory cells, FG transistor can be programmed by hot carrier injection (HCI) method. A typical programming and erasing scheme as shown in Fig. 1.15 (a) and (b), respectively.

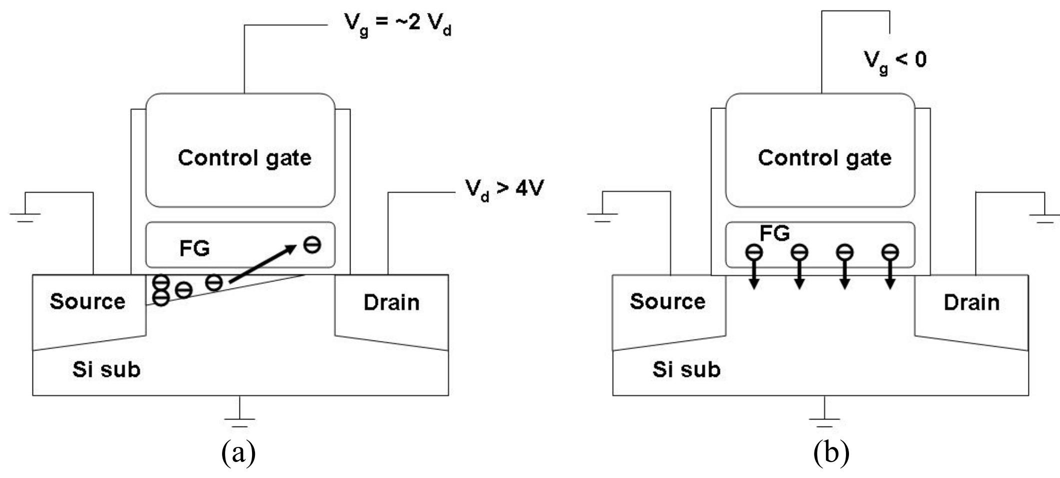


Fig. 1.15 A typical operation scheme of (a) hot carrier programming and (b) F-N erasing of a NOR memory cell.

In programming operation, considering that the barrier height of SiO_2 to Si is 3.1 eV and sheet resistance of the transistor, at least a drain voltage of 4 V is needed to produce enough "hot" electrons to overcome the barriers [1.45]. The momentum of some "lucky electrons" is towards the FG after collision with the lattice. With the help of the gate voltage, these hot electrons can be injected to the FG as described by the "Luck electron model" [1.46]. In Fig. 1.16, an energy band diagram of the gate stack in programming region is shown.

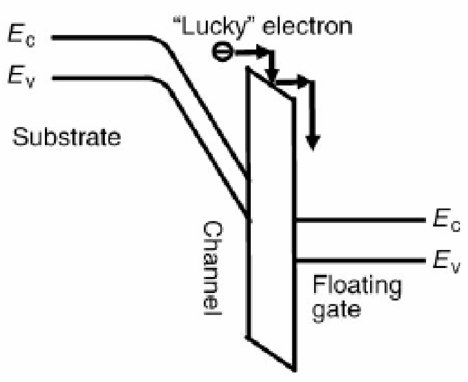


Fig. 1.16 Energy band diagram of the gate stack of a NOR memory transistor biased in programming region [1.45].

In the erase operation, a negative voltage is applied to the control gate, biasing the gate stack into the in Frenkel-Poole (F-N) tunneling region, erasing electrons from FG, as shown in Fig. 1.17.

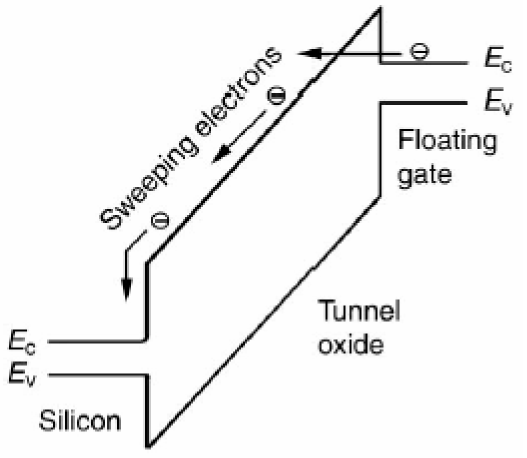


Fig. 1.17 Energy band diagram of the gate stack of a NOR memory transistor biased in F-N tunneling erasing region [1.45].

In NAND arrays, access can only be performed one by one along the bit line direction, FG transistors cannot be programmed by HCI method because a large drain voltage goes through all transistors during HCI operation. Thus both programming and erasing are performed by F-N tunneling, as shown in Fig. 1.18 (a) and (b), respectively.

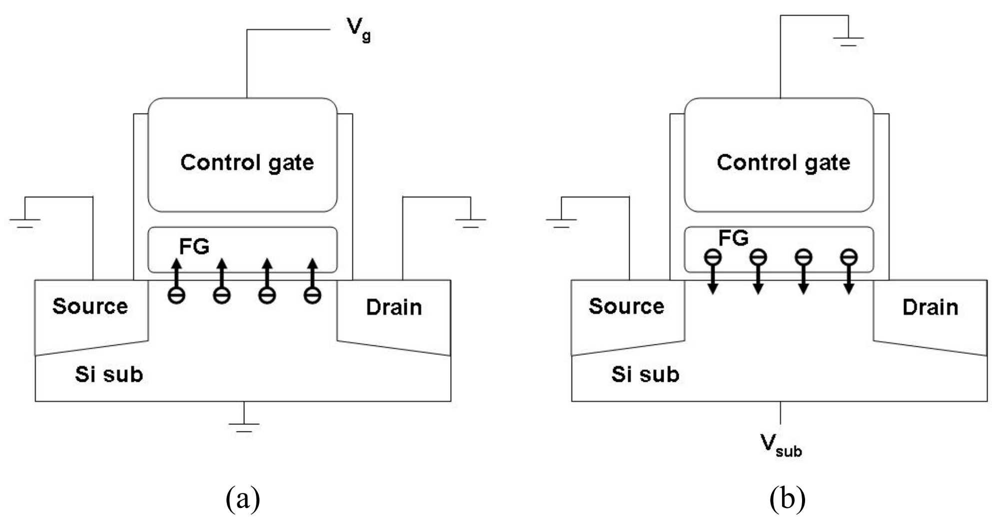


Fig. 1.18 A typical operation scheme of (a) F-N programming and (b) F-N erasing of a NAND memory cell.

In a programming operation, a large gate voltage is applied to bias the tunneling oxide into the F-N tunneling region, as shown in Fig. 1.19. In erasing operation, a negative voltage is applied to the substrate, bias gate stack in F-N tunneling region, erasing electrons from FG, which is the same with NOR arrays.

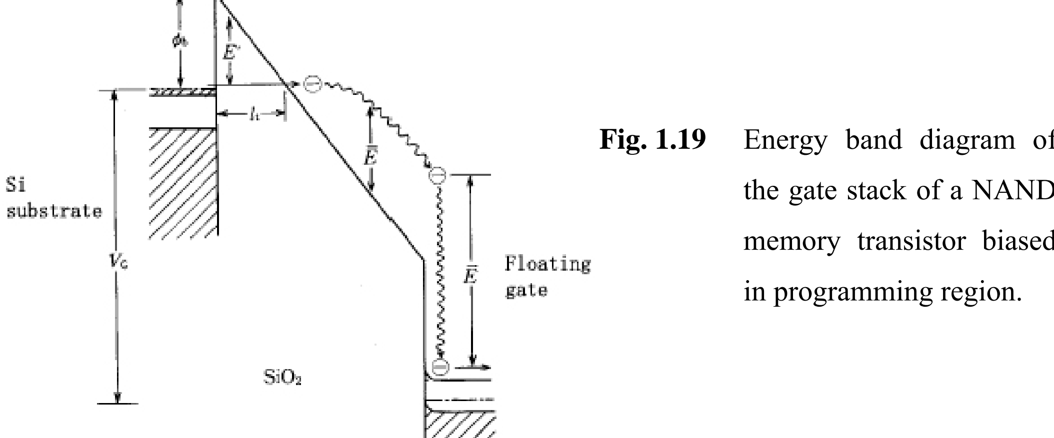


Fig. 1.19 Energy band diagram of the gate stack of a NAND memory transistor biased in programming region.

1.3.2 Scaling approaches and challenges of flash memory cell

A. Advantage of high-K dielectrics

The scaling approaches of flash memory devices are generally the same with MOSFET. However, the scaling approaches of some detailed sizes depend on the structure of arrays, device and operation scheme. Both NOR and NAND requirement of retention need thick tunneling and interpoly oxides. Hence oxide cannot not be scaled too much in these devices. To meet the retention of 10 years, a physical thickness of tunneling oxide of 7 nm is needed for mass production [1.3].

In NOR arrays, because a large drain voltage is needed to produce “hot” electrons, heavy doping of drain and large EOT of tunneling and interpoly oxides make gate length hard to scale down aggressively. Thus, even though the feature size of NOR flash memory device follows the technology node of VLSI technology, the gate length is hard to scale below to 0.2 μm, as shown by an example of a NOR flash memory array fabricated using 0.13 μm (Fig. 1.20).

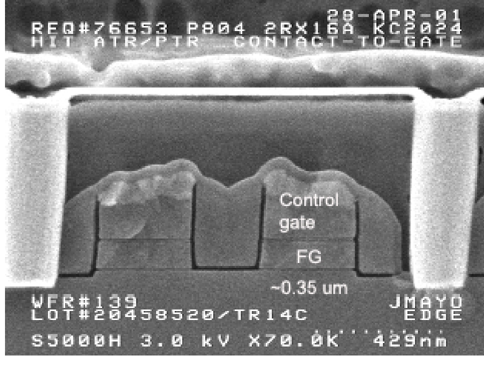


Fig. 1.20 A cross-sectional SEM image of NOR flash memory array along the gate length direction. The chip is manufactured by 0.13 μm technology node, but the gate length is ~0.35 μm. [1.47]

Hence in NOR arrays, the gate length is almost unscalable, and this results in a much slower scaling rate of cell area than other devices. If device structure remains unchanged, further scaling down of memory cells requires the use of high-K dielectrics. By using a high-K tunneling oxide, the barrier height of tunneling oxide

can be reduced and EOT can be reduced, bringing the advantages of low drain programming voltage and a shorter allowed gate length.

In NAND arrays, all dimensions follow the scaling speed of feature size, except the physical thickness of tunneling and interpoly oxides, as shown in Fig. 1.21. By using high-K tunneling and interpoly oxides, because of the smaller EOT and larger physical thickness compared with SiO_2, the further scaling down becomes feasible. In addition to scalable EOT, the use of a high-K tunneling oxide leads to lower programming voltage and better retention performance because of the smaller conduction band offset between Si substrate and high-K dielectric and larger physical thickness of high-K dielectric, respectively [1.48, 1.49].

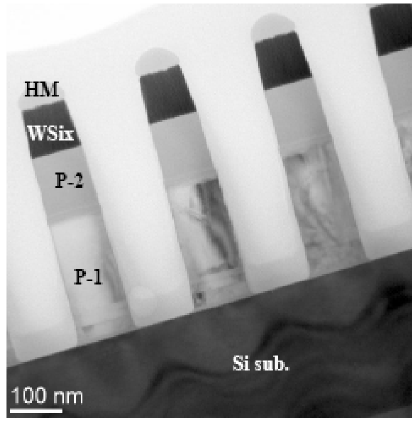


Fig. 1.21 A cross-sectional SEM image of NAND flash memory array along the gate length direction. The chip is manufactured by 0.1 μm technology node, and the gate length is also ~0.1 μm. P-1 is the FG, and P-2 is control gate.

When high-K dielectric is used as the control oxide of FG memory devices of both NOR and NAND arrays, control gate voltage coupling ratio can be increased because of the smaller EOT of the control oxide, resulting in a lower programming voltage and a larger memory window [1.50]. Furthermore, the larger physical thickness of high-K control and tunnel oxides helps the charge retention in low field regions (< 1MV/cm) [1.49, 1.51].

B. Advantage of discrete charge storage

Recently, discrete charge storage resulting from nanocrystals (NCs) [1.52] and Polysilicon-Oxide-Nitride-Oxide-Silicon (SONOS) type [1.53, 1.54] memories has received significant attention because the discreteness of charge storage suppresses lateral migration of charges; hence stored charges are less vulnerable to local oxide defects compared with conventional continuous floating gate memories [1.49, 1.52-1.54]. This results in better retention of memory using discrete charge storage when the same tunneling and interpoly oxides (commonly is called block oxide in memory using discrete charge) thickness are used. Thus a thinner oxide can be employed, bringing about advantages on scaling and operations.

In NCs memories, charges are stored in NCs formed using Si, Ge, or metallic materials, which are embedded in various dielectric materials such as SiO_2, HfO_2 and HfAlO [1.49, 1.52, 1.55-1.57]. Charges migrate laterally via direct tunneling (DT) and trap assisted tunneling (F-P) tunneling. Optimization of the device structure based on the properties of these materials could improve the performance of flash memories further. In SONOS-type memories, charges are dispersed in the sandwiched trappy dielectric layers. Beside the conventional Si_3N_4, high-K materials have been proposed as a trapping layer to achieve better charge retention properties [1.58].

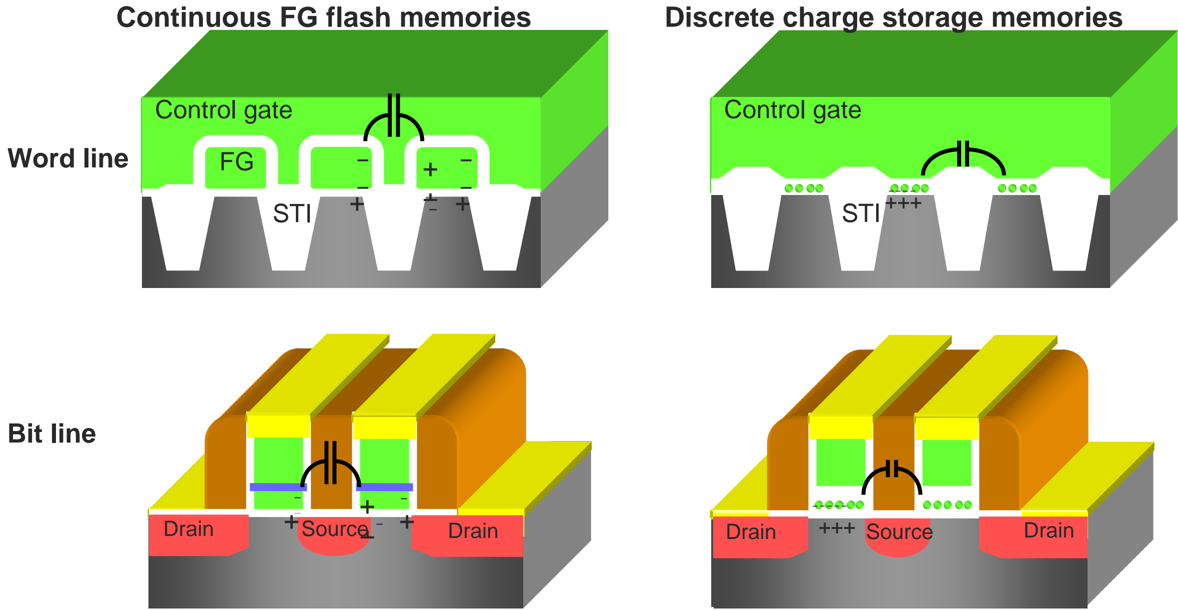


Fig. 1.22 Comparison of capacitive coupling of neighboring cells between continuous FG flash memories and discrete charge storage memories shown by a NOR array.

In addition to the advantages of scaling and operation, discrete charge storage brings about the advantage of immunity of coupling between adjacent cells because discrete charge storage reduces the capacitor between adjacent floating gate, as shown in Fig. 1.22. This is especially important in future highly compact arrays [1.45].

1.4 Organization of Thesis

The focus of this thesis is to study on the formation of advanced gate stack for future nano MOSFET and flash memory application. In particular, in the gate stack of nano MOSFET part, the integration issues of an advanced gate material, poly-SiGe and high-K dielectrics are studied, and for flash memories, the design and formation of two novel memories gate stack involving high-K materials are studied. Results can be usefully applied to the further scaling of MOSFETs and flash memories.

It has been reported that Hf based high-K dielectrics are promising candidate materials for both MOSFET and flash memories. From chapter 2 to 4, the removal and integration process of Hf based high-K dielectrics are studied in detail. Scientific mechanisms in removal process were revealed, and based on these findings, some novel processes were developed.

Because the understanding of inorganic chemistry of Hf based compounds is very limited, the basic Hf inorganic wet chemistry is investigated first in chapter 2. Because the area of this thesis is microelectronics, the microstructure and CMOS process relative properties are the focus. Wet etching properties of Hf based high-K dielectrics including HfO_2, $(HfO_2)_x(Al_2O_3)_{1-x}$, Hf oxynitride and Hf silicate were investigated. Various chemicals for conventional CMOS processing were used. Experimental results show that the conversion to the fluorides is important to dissolve Hf and HfO_2 in acids. Various materials characterization results show that the crystalline phase of HfO_2 is the main reason for the low etch rate and high etch resistance of Hf based high-K materials in HF and the etching of Hf based high-K

dielectrics always occurs through the weak points in the films such as amorphous HfO_2, Hf-N, Al-O and Si-O bonds.

In chapter 3, the effects of plasma treatment using Ar, N_2 and O_2 inductively coupled plasmas on removal properties of crystallized HfO_2 films in dilute HF solution, damage in source and drain regions, and recess in isolation regions are studied. Two novel removal processes using Ar and N_2 plasma treatments for removal of Hf based high-K dielectrics are introduced. The mechanisms responsible for these processes were revealed by x-ray photoelectron spectroscopy and simulation using SRIM Monte Carlo code.

In chapter 4, a study on plasma etching properties of Hf based high-*k* dielectric using inductively coupled plasmas is presented. The aspects of etch rate, etching mechanisms, selectivity, and the effects of elements added in of Hf based high-K dielectric and etch residues were addressed. The results from this study can be used to understand the plasma etching mechanisms of Hf based high-K dielectrics and to develop high-K gate stacks etching recipes.

In chapter 5, the plasma etching properties of poly-SiGe and a novel poly-SiGe/HfO_2 gate stack are studied. The profile, selectivity control and optical emission endpoint are investigated.

In chapter 6, the techniques to form the structure of Ge NCs embedded in HfAlO are introduced. It was found that Ge-NCs can form in HfAlO via phase separation. Electrical characterizations were performed to the memory device using Ge-NCs as floating gates is performed. Results from this study show that it is a promising candidate device structure for the future scaling down of flash memories.

In chapter 7, a novel high-K Al_2O_3 nano-dots flash memory device and a novel two step controlled anneal process are introduced for the formation of Al_2O_3 NDs on SiO_2. Results show that the conglomeration of Al is impeded by oxygen and the size and density of Al_2O_3 NDs can be controlled by the initial Al film thickness and annealing temperature. Memory devices with Al_2O_3 NDs fabricated using this technique show improved retention properties compared to those with Al_2O_3 continuous films. A comparison of temperature dependency shows that the good retention property originates from the suppression of lateral migration of electrons via F-N tunneling.

In chapter 8, at first, conclusions were drawn based on the findings and processes developed from this study. Finally, suggestions on the future works are made.

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Chapter 2

Investigation of Wet Etching Mechanisms of Hf based High-K Dielectrics and Effects of Annealing

2.1 Introduction

In the Chapter 1, we have introduced that due to the aggressive downscaling of the feature size of Complementary-Metal-Oxide-Semiconductor (CMOS) devices, large gate leakage has emerged as one of major challenges for sub 45 nm technology [1]. High dielectric constant (high-K) materials have received significant attention as gate dielectrics because they enable larger physical thicknesses for the same equivalent oxide (SiO_2) thickness (EOT) compared with conventional gate dielectrics of SiO_2 and SiO_xN_y, leading to much lower gate leakages [2.1, 2.2]. Recently, Hf based high-K dielectrics such as HfO_2 [2.3, 2.4], $(HfO_2)_x(Al_2O_3)_{1-x}$ (HfAlO) [2.5-2.7], Hf oxynitride (HfON) [2.8, 2.9], Hf silicate ($Hf_xSi_{1-x}O_2$) [2.10, 2.12] and its nitride [2.13, 2.14] have been considered as the most promising alternative gate dielectrics for future CMOS devices due to their good thermal stability, strong immunity to boron penetration, low degradation of carrier mobility or relatively low gate leakage compared with other candidates.

From the point of process integration, implementation of Hf based high-K dielectrics is a great challenge, especially in the removal (cleaning) process after plasma etching of the gate electrode. In current CMOS process, dilute hydrofluoric

acid (DHF) is widely used to remove the remaining gate dielectric after gate patterning to open source and drain regions for the silicidation process [2.15] because it can selectively remove SiO_2 and SiO_xN_y without attacking the Si substrate and the polycrystalline Si gate. However, many reports have shown that the etch rates of HfO_2 and $Hf_xSi_{1-x}O_2$ decrease very sharply in HF solutions especially in those samples with history of more thermal treatment [2.16-2.22], although Hf is dissoluble in aqueous HF [2.23]. This is very similar to the etching of Ta_2O_5 in aqueous HF [2.24, 2.25].

If post deposition anneal (PDA) can be avoided or performed after gate etching, Hf based high-K dielectrics can be easily integrated into conventional CMOS process in terms of dielectric removal as they can be selectively removed by DHF before thermal treatment. However, PDA is indispensable for acquiring high quality high-K dielectrics as it can remove impurities such as carbon and hydrogen and densify films, resulting in good electrical properties [2.3-2.14]. Furthermore, PDA, as its name suggests, must be performed just after deposition. This is to avoid undesirable reactions in subsequent processes. Therefore, high-K dielectric removal process must be carried out after anneal. It was suggested that crystallization and densification due to the anneal could be the main reasons responsible for the enhancement of wet etching resistance of HfO_2 and $Hf_xSi_{1-x}O_2$, but this is yet to be proven by experiments. Meanwhile, it has been reported that Hf based high-K dielectrics can be dry etched by halogen based plasmas [2.26-2.28]. However, the removal of etch residues, the attainment of high etch selectivity and high uniformity are difficult in this process [2.27, 2.29], especially when considering very strict

requirements for sub 45 nm technology nodes and large wafer sizes with the diameter of 300 mm [2.1].

Until now, no promising process has been demonstrated for the selective removal of Hf based high-K dielectrics on Si substrate. In addition, the lack of understanding in the chemistry of Hf based inorganic materials in CMOS processing poses a further barrier to the development of a suitable process.

In this paper, we studied the effects of anneal on the microstructure of thin Hf based high-K dielectric films with the aim of understanding the wet etch mechanism of each film, using aqueous chemicals for conventional CMOS process: HNO_3, H_2SO_4, HCl, H_3PO_4 and NH_4OH-H_2O_2 (SC1). Various material characterization techniques including inductively coupled plasma optical emission spectroscopy (ICP-OES), transmission electron microscopy (TEM), atomic force microscopy (AFM) and x-ray photoelectron spectroscopy (XPS) were employed to reveal the etching mechanisms as well as the microstructure of the films.

2.2 Experimental Setup

In this work, all films were deposited on *p*-type Si (100) wafers using either a sputtering (also known as physical vapor deposition (PVD)) system at room temperature or a chemical vapor deposition (CVD) system. All anneal processes were performed in a rapid thermal process chamber. HfO_2 films were deposited by either CVD or reactive PVD. In CVD process, HfO_2 films were deposited at 320ºC, using O_2 and a bubbler precursor source, $Hf(OC(CH_3)_3)_4$ carried by Ar [2.18, 2.27]. In PVD process, HfO_2 films were deposited using a Hf target in Ar/O_2 ambient at 3

mTorr [2.27]. $Hf_xSi_{1-x}O_2$ and HfON films were deposited by PVD using Hf single target (or Hf + Si dual targets for $Hf_xSi_{1-x}O_2$) in Ar/O_2 or $Ar/O_2/N_2$ ambient at 3 mTorr. The atomic concentration of N in HfON films was around 10%. Recently, there has been an increasing interest in engineering $Hf_xSi_{1-x}O_2$ films to balance the performance of high-K dielectrics in terms of electron mobility, gate leakage and thermal stability [2.8-2.12]. In this work, the composition of $Hf_xSi_{1-x}O_2$ films was controlled with x approximately equal to 0.3, 0.5 and 0.7 by applying different powers to the Hf and Si targets. HfAlO films were deposited using an atomic layer CVD, where precursors of $HfCl_4$, $Al(CH_3)_3$ and reactant were used and the atomic ratio of Hf : Al was controlled at 7 : 3 by controlling the number of $HfCl_4$ and $Al(CH_3)_3$ cycles. Hf and Hf nitride (HfN) films were also prepared using PVD for the study of the etching properties of Hf inorganic compounds. HfN films were deposited using Hf target in an ambient of Ar/N_2. The atomic ratio of Hf to N in HfN was about 1 : 1, according to the reference 2.30.

In this work, all the thickness of transparent films was measured by a multi-wavelength ellipsometer whereas the thickness of opaque Hf and HfN films was measured by a surface profiler. The analysis of the XPS results was based on the cited references [2.31, 2.32]. The saturated solubility of HfF_4 in aqueous solutions was determined by an ICP-OES, with a detection limit of 1 ppm.

2.3 Results and Discussion

2.3.1 Study of etching mechanisms of Hf inorganic compounds

Table 2.1 shows the etch rate of Hf films, HfO_2 films deposited by PVD and CVD in aqueous chemicals used in conventional CMOS process including 1% DHF, H_2SO_4 (80%), HNO_3 (20%), H_3PO_4 (85%), HCl (15%) and SC1 (NH_4OH : H_2O_2 : H_2O = 0.25 : 1 : 5) at room temperature.

Table 2.1 Etch rates of Hf, PVD HfO_2 and CVD HfO_2 in various chemicals used in conventional CMOS process.

Chemicals		DHF	HF	H_2SO_4
Volume concentration		1%	10%	80%
Etch rate (Å/min)	Hf	~ 1000	>>3000*	~ 800**
	PVD HfO_2	150	~300	< 10
	CVD HfO_2	60	~160	~ 0
Remark		* 3000Å was removed in ~ 15 s. ** Samples were dipped in 1 % HF for 5 s.		

Table 1 cont'd

Chemicals		HNO_3	HCl	H_3PO_4	SC1
Volume concentration		20%	15%	85%	Standar d
Etch rate (Å/min)	Hf	~ 800**	~ 800**	~500**	~ 0
	PVD HfO_2	< 20	< 25	< 10	0
	CVD HfO_2	~ 0	~ 0	~ 0	~ 0
Remark		* 3000Å was removed in ~ 15 s. ** Samples were dipped in 1 % HF for 5 s.			

The concentration of each chemical was determined according to its purpose in conventional CMOS cleaning process, *i. e.* H_2SO_4 is used in SPM (H_2SO_4 : H_2O_2 = 4 : 1), HCl is used in SC2 (HCl : H_2O_2 : H_2O = 1: 1 : 5) and concentrated H_3PO_4 (85%) is used for silicon nitride etching. Since Hf is hard to etch by acids after oxidation, the oxidizing reagent, H_2O_2 was removed from SPM and SC2 while the acid concentration was maintained to understand the role of acidity in etching.

It is found that HF solution shows the strongest etching ability on Hf among the various acid solutions whereas SC1 is unable to etch both Hf and HfO_2. For PVD HfO_2, all the acid solutions are able to etch the film but the etch rates in HF solution are significantly higher than that in other solutions, regardless of the difference of the concentration; however, for CVD HfO_2, only HF solution is able to etch the film. Generally, except HF, other chemicals show very weak or no ability to etch HfO_2.

In all the reactions between the acid solutions studied and Hf, a colorless gas, which was identified as hydrogen using an ATMI® hydrogen detector, was generated. This indicates that displacement reactions occur between acids and Hf. However, it is interesting that although Hf can react with aqueous H_2SO_4, HNO_3, H_3PO_4 and HCl, etching is hard to perform without first dipping the samples in HF solutions. This may be because the oxide on the surface can effectively blocks the etching in these solutions. Another observation is that except HF, reactions between Hf and acid solutions can last for only ~ 20s. Hf is known to dissolve to a certain extent in some of these solutions, such as aqueous HCl [2.23], which implies that the solubility is not the reason for the diminished reactions. Considering that some HF remains on the surface of Hf films after the removal of the oxide, the diminished reactions may be due to the consumption of fluoride. This suggests that the presence

of H^+ is not a sufficient condition for displacement reaction to take place between Hf and aqueous acids; fluorides play an important role in dissolving Hf as well as HfO_2 in acids. Since very dilute HF can etch Hf and HfO_2 effectively, the generation of F^-, HF_2^- ionic species and HF, H_2F_2 molecular species can be responsible for the etching [2.33, 2.34].

From Table 2.1, we also observe that when the concentration of HF solutions increases, the etch rate of Hf and HfO_2 increases. In concentrated HF, the equilibrium of H^+, F^-, HF, HF_2^- and H_2F_2 in HF solutions shifts to the HF_2^- and H_2F_2 rich end [2.33, 2.34]. Hence, it is understood that H_2F_2 and/or HF_2^- can be the main species to etch Hf and HfO_2. This is similar with HF etching of Si and SiO_2 [2.34-2.37]. The XPS signal of F*1s* electron from the surface of HfO_2 after DHF etching is shown in Fig. 2.1 (a).

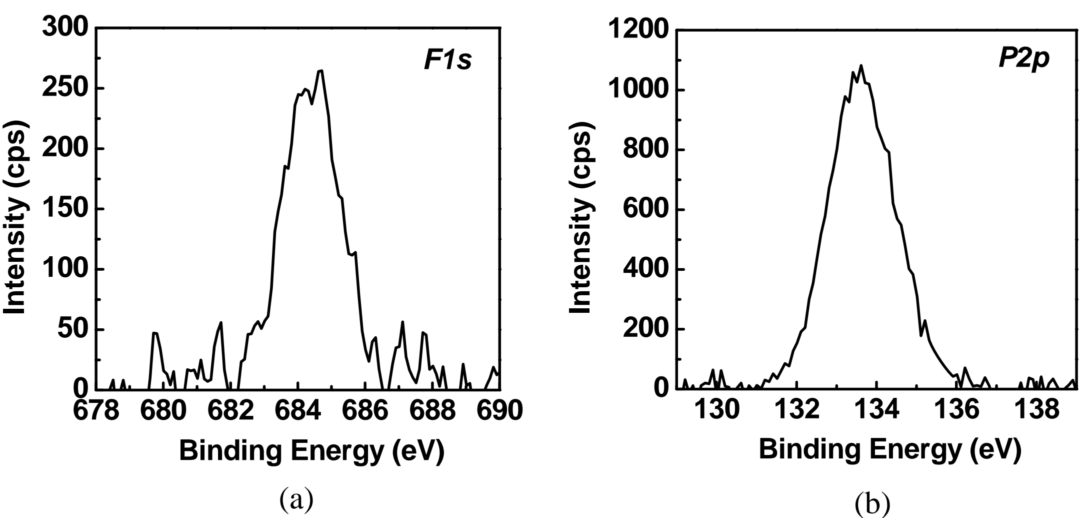


Fig. 2.1 XPS taken from surface of (a) F*1s* peak from 1% DHF etched HfO_2 film at room temperature and (b) P2*p* peak from 85 % H_3PO_4 etched HfO_2 film at 98 °C.

It is known that binding energy in the range of 682 to 686 eV for F*1s* represents inorganic fluoride. Hence the F should bond with Hf, not with O in these fluorides. A detection angle of 90 ^{o} is used in XPS so that signals emerging ~6 nm from the sample surface can be collected. From the Hf*4f* signal intensity of ~ 3000 count per second, the fluoride layer thickness is estimated to be ~ 0.3 nm fluorides, which is equivalent to about one single molecular layer. Hence it is very likely that these fluorides are not thick residue but some F atoms terminated on Hf atoms. This means that although the chemical species inducing the etching of Hf, HfO_2, Si and SiO_2 are similar, the reacting routes may be very different, *i.e.* etching species can directly react with Hf and HfO_2 without a process of eliminating OH^- group that is found in the HF etching of Si and SiO_2 [2.34, 2.35, 2.37, 2.38].

Since the vapor points of H_2SO_4 and H_3PO_4 are relatively high at 338 ^{o}C and 213 ^{o}C respectively, we studied the etch properties of Hf and HfO_2 in H_2SO_4 (20%) and H_3PO_4 (85%) at 98 ^{o}C which is similar to the process temperature used in conventional CMOS process [2.15]. We found that hot H_2SO_4 and H_3PO_4 still cannot etch HfO_2; however, after the removal of oxide using DHF, Hf with thickness of ~ 6000 Å can be etched by either hot H_2SO_4 or H_3PO_4 in a few minutes (the accurate etch rate is hard to acquire perhaps due to the nonuniformity of film property). This means that Hf can dissolve in H_2SO_4 and H_3PO_4; however, the activation energy of the reactions in H_2SO_4 and H_3PO_4 is higher than that in HF.

After dipping in the various chemicals, all the HfO_2 and Hf films were analyzed by XPS. No etchant containing residue can be found on the Hf or HfO_2 surface except for the cases of HF and hot H_3PO_4 etching, as shown in Fig. 2.1 (b). Binding energy in the range of 132 to 136 eV for P*2p* is known to represent

phosphate. Considering that the XPS atomic sensitivity factor is 0.39 for P2*p* and 1 for F*1s*, the amount of phosphate is ten times higher than that of fluoride and it is equivalent to 3 nm. This result suggests that some Hf phosphates may be insoluble.

Figure 2.2 shows the saturation solubility of HfF_4 in aqueous solutions with various pH values measured using ICP-OES. HCl and NH_4OH are used to prepare solutions with pH value lower and higher than 7, respectively. It can be found that the solubility of HfF_4 increases at lower pH value. This same trend is reported from the theoretical calculation of the dissolution of HfO_2 in HF solutions by Lowalekar *et. al.* [2.39].

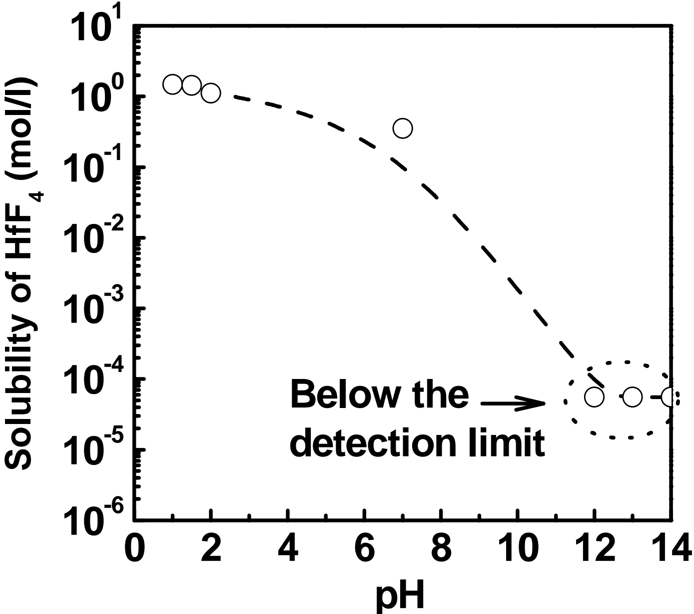


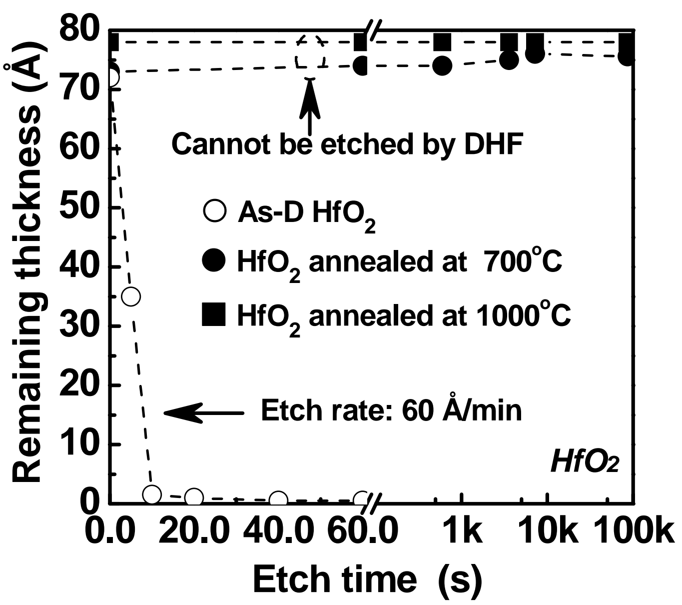
Fig. 2.2 Solubility of HfF_4 in solutions with various pH value. HF and NH_4OH were used to acquire various pH values.

However, it should be noted that the absolute dissolvability of HfF_4 is much higher compared with calculated results [2.39]. At room temperature, HfF_4 is highly soluble in water or acids. This shows that HF can be a good chemical for Hf based

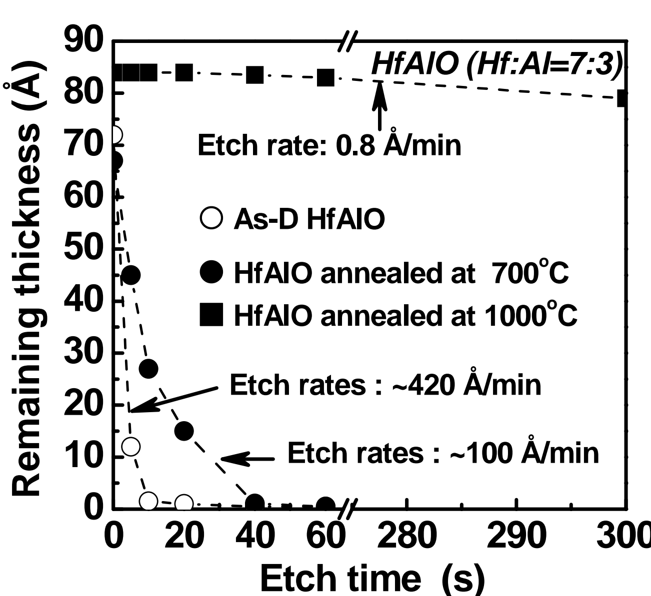
high-K dielectrics etching, and suggests that the fluorides may contain some fluorine atoms terminated on HfO_2 and Hf surface, different from normal residues. The saturation solubility of HfF_4 in aqueous HfCl (20%), H_3PO_4 (85%) and H_2SO_4 (80%) solutions was measured using ICP-OES, to be 8.68×10^{-7} mol/l, 4.72×10^{-8} mol/l and 2.15×10^{-7} mol/l, respectively. HfF_4 has the lowest saturation solubility in H_3PO_4, supporting the XPS result from the Hf surface etched by hot H_3PO_4. In the characterization of solutions with pH value lower than 7, H_3BO_3 is used for consuming fluorine to protect the quartz chamber of ICP-OES machine, hence the measured saturation solubility can be lower than the true values.

2.3.2 Effects of anneal and compositions

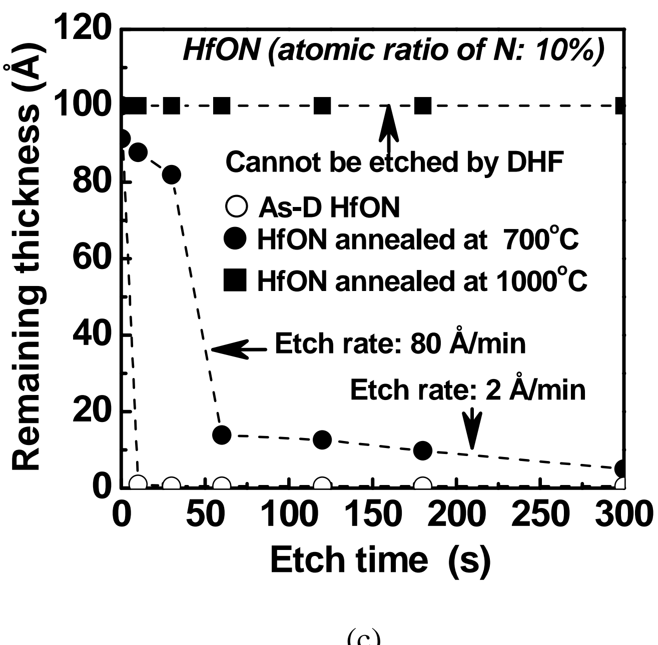
As HF solutions have been investigated widely for etching HfO_2, we choose them to study the effect of anneal and composition on the wet etching properties of Hf based high-K dielectrics.



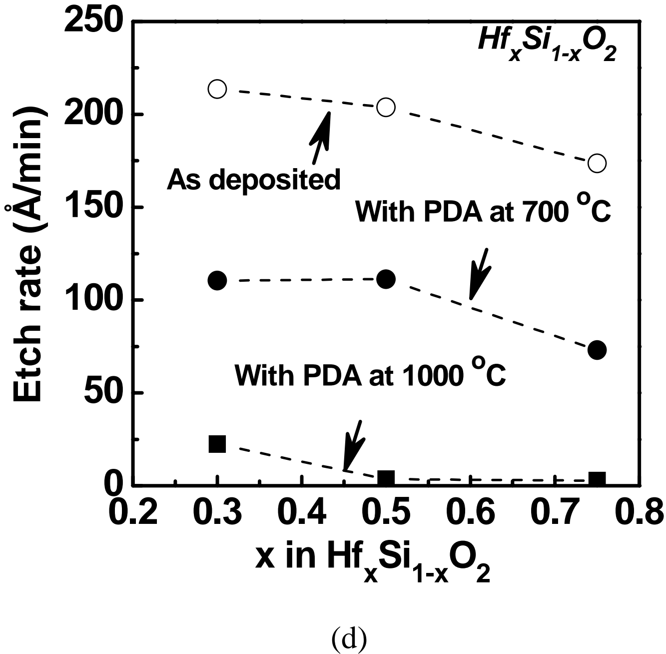
(a)



(b)



(c)



(d)

Fig 2.3 Wet etching properties of as deposited and annealed Hf based high-K dielectrics (a) HfO_2 (b) HfAlO (c) HfON and (d) $Hf_xSi_{1-x}O_2$ (x = 0.3, 0.5 and 0.75) in 1% DHF. All anneals were performed for 1 min in N_2

Figure 2.3 shows the etching rates of as deposited and annealed HfO_2, HfAlO, $Hf_xSi_{1-x}O_2$ and HfON films in 1% DHF. Experimental results show that all the as deposited films with thickness from 70 Å-100 Å can be removed by 1% DHF in 10 s. After anneal at 700 ^oC, etch rates of all the Hf based high-K films drop by different extents. 70 Å thick HfAlO film can be removed in 10 s. For 100 Å thick HfON films, the initial etching rate is very low. After dipping in DHF for 40 s, the etch rate increases rapidly, but the etching rate drops again when the remaining thickness becomes ~13 Å. The remaining film can ultimately be etched by DHF at a slow rate. For HfO_2 with thickness of ~70 Å that has undergone anneal at 700 ^oC or 1000 ^oC, the film cannot be etched in 1% DHF etching. Even after 24 hours in DHF, the film thickness does not decrease. After anneal at 1000 ^oC, the etch rate of HfAlO and HfON is much slower compared with the etch rate after anneal at 700 ^oC. The etch rate of HfAlO drops from hundreds of Å/min to 0.8 Å/min whereas HfON is no longer etched like the HfO_2 films after annealing at 700 ^oC and above. Etch rate of $Hf_xSi_{1-x}O_2$ films decreases with increasing Hf concentration. For the films after anneal, the etch rate drops significantly after anneal, similar to the observation for other Hf based high-K dielectric films.

Figure 2.4 shows cross-sectional transmission electron microscopy (TEM) images of as deposited HfO_2 film ($AsDHfO_2$), HfO_2 films with PDA at 700 ^oC ($HfO_2$700) and 1000 ^oC ($HfO_2$1000) in N_2. It can be found that the as $AsDHfO_2$ film is amorphous, indicating that amorphous HfO_2 can be etched by DHF easily. After PDA at 700 ^oC, the HfO_2 film becomes a mixture of crystallized HfO_2 and amorphous HfO_2. The lateral structure of this film is a series of crystal grains with amorphous filling, and vertical structure is either fully crystallized or amorphous

HfO_2. After PDA at 1000 ^oC, the film is fully crystallized, and no amorphous HfO_2 is observed between crystal grains.

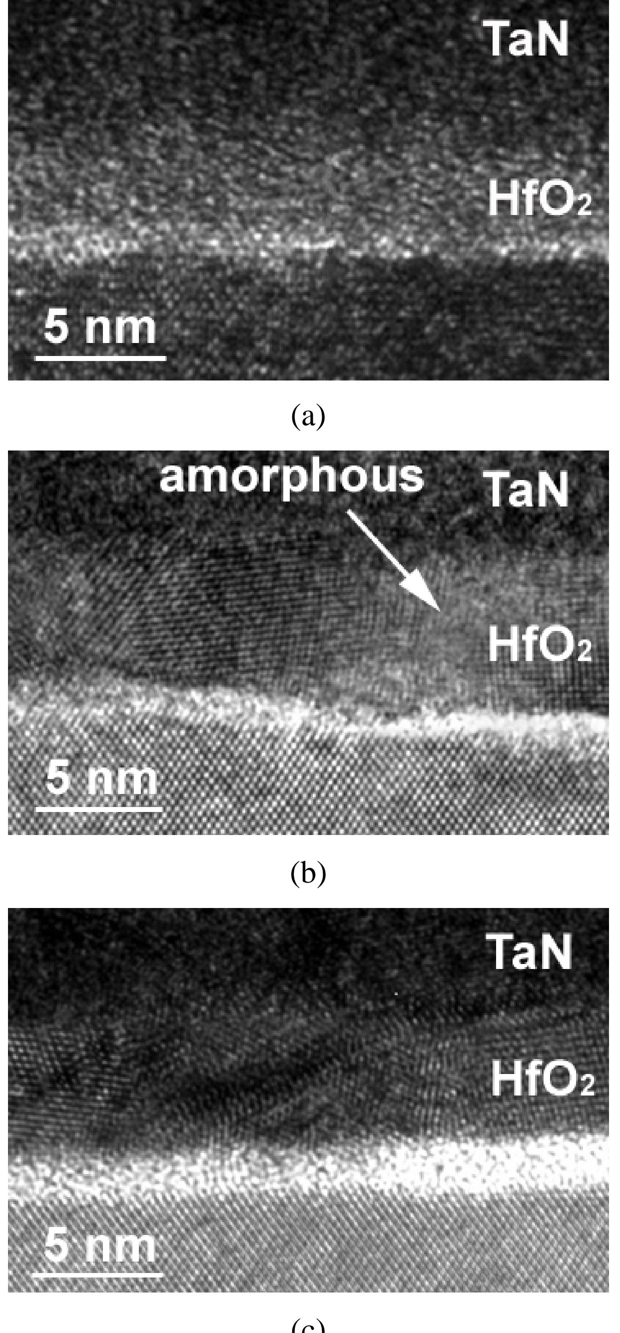


Fig. 2.4 Cross-sectional TEM images of (a) as deposited HfO_2 film (b) HfO_2 film annealed at 700 ^oC for 1 min in N_2 and (c) HfO_2 film annealed at 1000 ^oC for 1 min in N_2. All HfO_2 films were capped by TaN before TEM analysis.

After etching in 10% HF for 1 min, the topographies of as AsDHfO_2, $HfO_2$700 and $HfO_2$1000 films are analyzed by atomic force microscopy (AFM), as shown in Fig. 2.5.

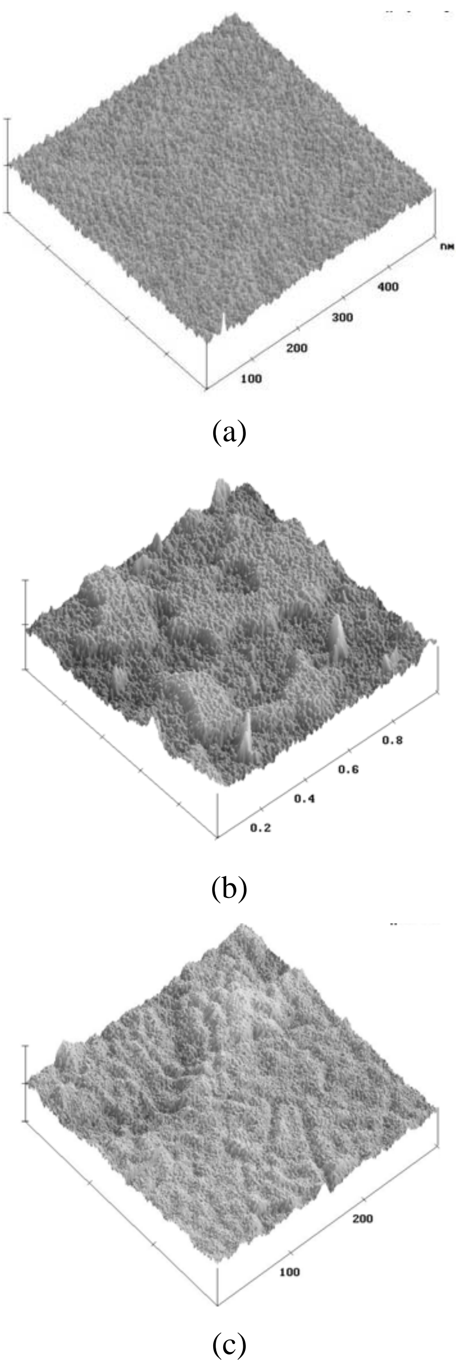


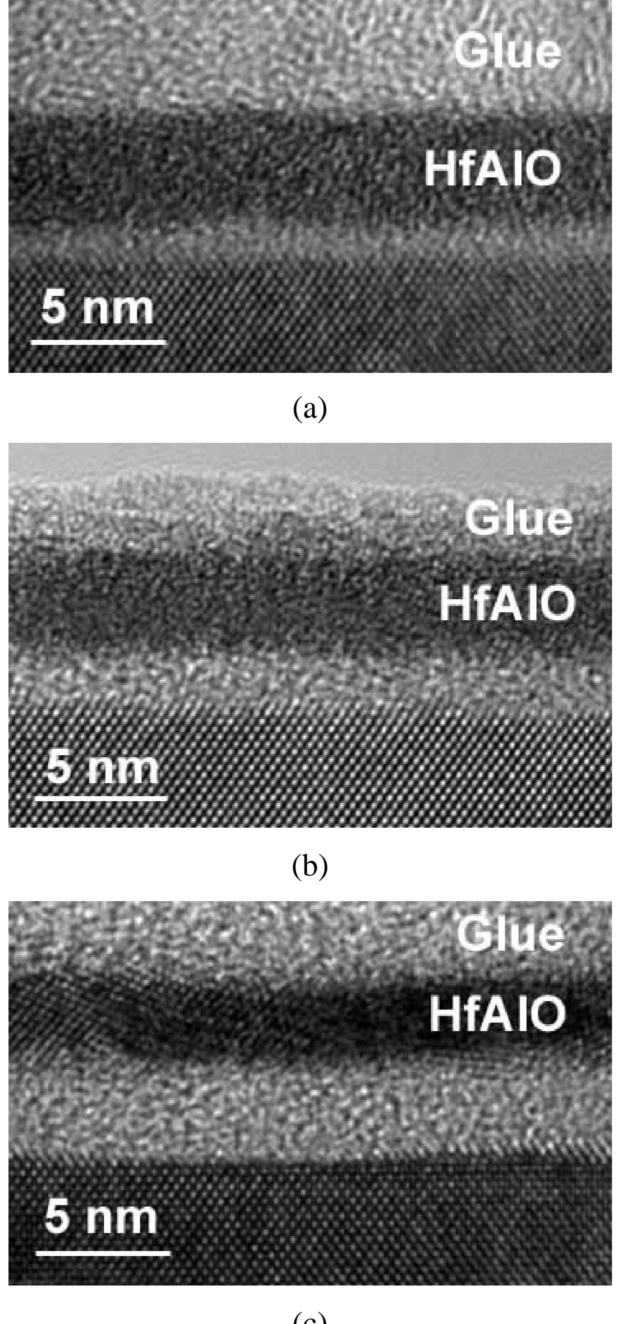
Fig. 2.5 After etching in 10% HF for 1 min, AFM analysis of the HfO_2 surfaces of (a) as deposited film (b) after PDA at 700 ^oC for 1 min in N_2 (c) after PDA at 1000 ^oC for 1 min in N_2.

It is interesting to observe the island and groove structures from the surface of $HfO_2$700 and $HfO_2$1000 films, respectively, whereas no special structure can be observed from the surface of As$DHfO_2$ film. Since amorphous HfO_2 can be etched by DHF, it is very likely that the recess regions observed in Fig. 2.5 (b) consist of the amorphous HfO_2 observed in Fig. 2.4 (b); whereas the islands observed in Fig. 2.5 (b) could be the crystal grains observed in Fig. 2.4 (b). This assumption is supported by another observation that the typical grain size of crystal HfO_2 in Fig. 2.4 (b) is around 100 - 200 Å, which is the similar to the size of the islands observed in Fig. 2.5 (b). The formation of groove like structures observed in Fig. 2.5 (c) can be explained by concentrated HF etching along the grain boundaries when HfO_2 film is fully crystallized, because the dangling bonds at the grain boundaries can favor the wet etching. Therefore, crystallization is considered to be the primary reason for the etch resistance of the annealed HfO_2 in 1 % DHF, although densification occurs by annealing for HfO_2 and $Hf_xSi_{1-x}O_2$ films [2.17, 2.18].

It has been predicted that the presence of dislocations and stress and strain of the bonds between atoms can enhance the dissolution rate of crystals in aqueous solutions significantly, despite no significant change in thermodynamic property [2.40, 2.41]. Such theory has been proven by Casey *et. al.* in the study of the effect of crystal defects on the dissolution kinetics of rutile (polycrystalline TiO_2) [2.42] as another high-K material, where the metallic cation belongs to the same group as Hf in the periodic table. In amorphous HfO_2 films, there is no long range order. Numerous dislocations as well as the stress and strain of the bonds between Hf and O atoms create weak points in the aqueous HF etching process, resulting in the

breaking of Hf-O bonds; however, in crystallized HfO_2 film, well ordered Hf-O periodic structure can help the Hf-O bonds to resist the etching effectively.

Cross-sectional TEM images of as deposited HfAlO film, HfAlO films with PDA at 700 ^{o}C and 1000 ^{o}C in N_2 for 1 min are shown in Fig. 2.6.



(a)

(b)

(c)

Fig. 2.6 Cross-sectional TEM of (a) as deposited HfAlO film (b) HfAlO film annealed at 700 ^{o}C for 1 minute in N_2 and (c) HfAlO film annealed at 1000 ^{o}C for 1 min in N_2 .

It has been reported that the incorporation of Al_2O_3 into HfO_2 can suppress crystallization significantly. By incorporating 15 % Al_2O_3 into HfO_2 film, the film can remain amorphous up to 900 °C [2.43]. Figure 2.6 (b) shows that the HfAlO film remains amorphous even after PDA at 700 ^{o}C. Since Al_2O_3 is chemically soluble in HF [2.23], HfAlO film can be etched easily both before and after PDA at 700 ^{o}C, although densification has occurred after annealing at 700 ^{o}C, as shown in Figs. 2.6 (a) and (b). It is found that after 1000 ^{o}C anneal, the HfAlO film becomes fully crystallized and etch rate drops significantly. As suggested above, crystallization should be mainly responsible for the significant decrease in etch rate. However, unlike the HfO_2 after anneal at 700 ^{o}C and above, the HfAlO film after PDA at 1000 ^{o}C can be steadily etched with an etch rate of 0.8 Å/min until the film is completely removed.

It has been reported that the X-ray diffraction (XRD) spectra are different for HfO_2 and HfAlO crystals [2.44]. Also, the peak positions with the same miller indices and peak broadness are different for HfO_2 and HfAlO crystals [2.44, 2.45]. This implies that Al_2O_3 may fully merge into the crystalline structure of HfO_2, inducing dislocation, highly strained and stressed bonds, favoring the dissolution process where pitting occurs first in the Al_2O_3 rich regions.

The XPS depth profile of the atomic ratio of O, N, Hf and Si of ~10 nm thick HfON film on Si substrate before and after PDA at 700 ^{o}C is shown in Fig. 2.7. It can be found after PDA, the surface of the HfON film is more oxygen rich compared with the as deposited film. This can be induced by the thermal oxidation by O impurities during PDA in N_2. As its surface becomes stable HfO_2 after PDA at 700 ^{o}C, HfO_2 can crystallize, forming an etch-resistive layer in DHF solution. After PDA

at 1000 ^{o}C, an even thicker crystallized HfO_2 layer can form. This can explain the low initial etching rate of HfON in 1% DHF after anneal at 700 ^{o}C and the high etch resistance of HfON after anneal at 1000 ^{o}C.

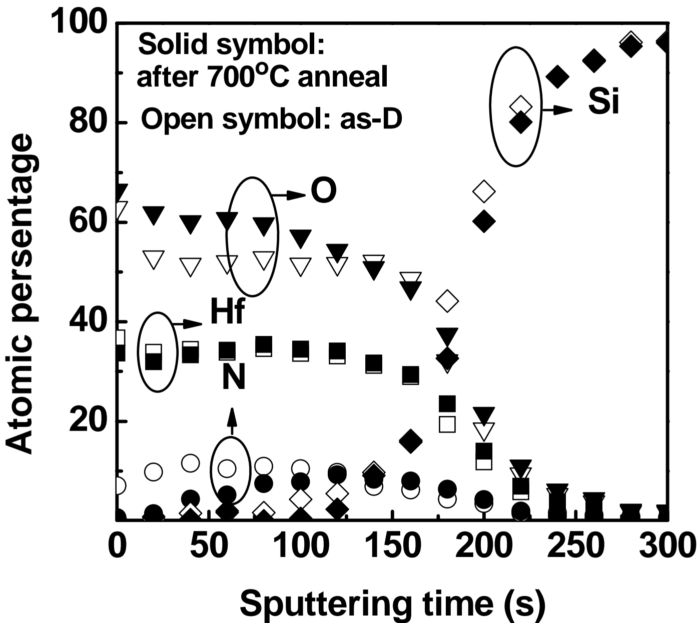


Fig. 2.7 Depth profile of atomic percentages of O, N, Hf and Si of as deposited and annealed HfON films with thickness of ~100 Å on Si substrate. The results were obtained by monitoring O*1s*, N*1s*, Hf*4f* and Si*2p* peaks of XPS. The anneal was performed at 700 ^{o}C for 1 min in N_2.

It is observed that HfN can be etched in 1% DHF easily. Although the etch rate drops after PDA at 700 ^{o}C, it is still very high at 150 Å/min as shown in Fig. 2.8. Both as deposited and annealed HfN films are crystallized [2.30], and this indicates that the Hf-N bond is highly soluble in DHF regardless of crystallization. It has been reported that the incorporation of 10% N into HfO_2 can help the film to remain amorphous up to 1000 ^{o}C [2.8, 2.9]. From Fig. 2.7, it can be found that the bulk of HfON film after PDA at 700 ^{o}C is still incorporated with nitrogen with atomic ratio

of around 10% after anneal. Hence, rapid increase of wet etching rate of HfON film in 1% DHF after 40 s dipping can be attributed to the amorphous HfO_2 phase and highly HF soluble Hf-N bonds.

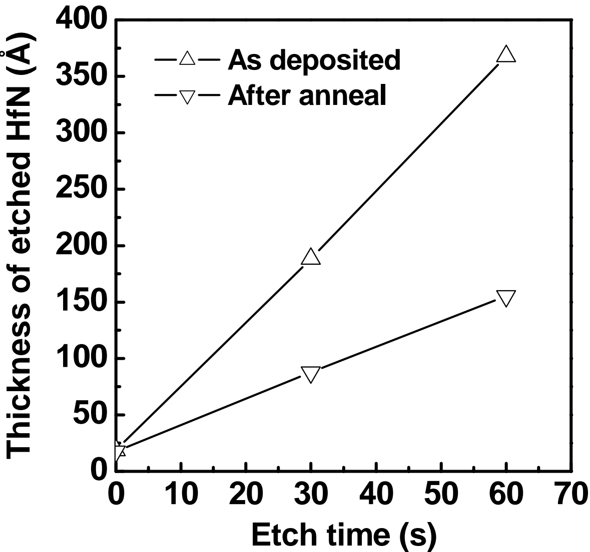


Fig. 2.8 Amount of etched thickness of HfN deposited at room temperature in the reactive sputtering and annealed at 700 ^{o}C for 1 min in N_2 in 1% DHF as function of time. HfN has been etched by plasma etching before dipping into DHF in the case where oxide is formed on the surface.

The reason for the slowing down of the etching rate when the remaining thickness is ~13 Å is unclear. It has been reported that after high temperature anneal, the interfacial layer between HfON and Si can contain Hf-Si [2.8] and Si-N bonds [2.9], and for HfO_2 on Si, $Hf_xSi_{1-x}O_2$ and SiO_2 can form [2.45]. $HfSi_2$ can dissolve in HF [2.46], but Si_3N_4 dissolves very slowly in HF [2.47]. As $Hf_xSi_{1-x}O_2$ after PDA at 700°C can be etched in DHF easily as shown in Fig. 2.3 (d), it is likely that the formation of Si-N bonds is responsible for the drop in etching rate.

Researchers have reported that the etch rate of $Hf_xSi_{1-x}O_2$ drops rapidly after anneal [2.17, 2.22]. This effect is enhanced with a higher concentration of Hf in $Hf_xSi_{1-x}O_2$ [2.22]. The same trend is observed in Fig. 2.3. Figure 2.9 shows AFM images on $Hf_xSi_{1-x}O_2$ films with various Hf/Si ratios that have undergone PDA at 700 ^oC and 1000 ^oC followed by DHF dipping for 1 min.

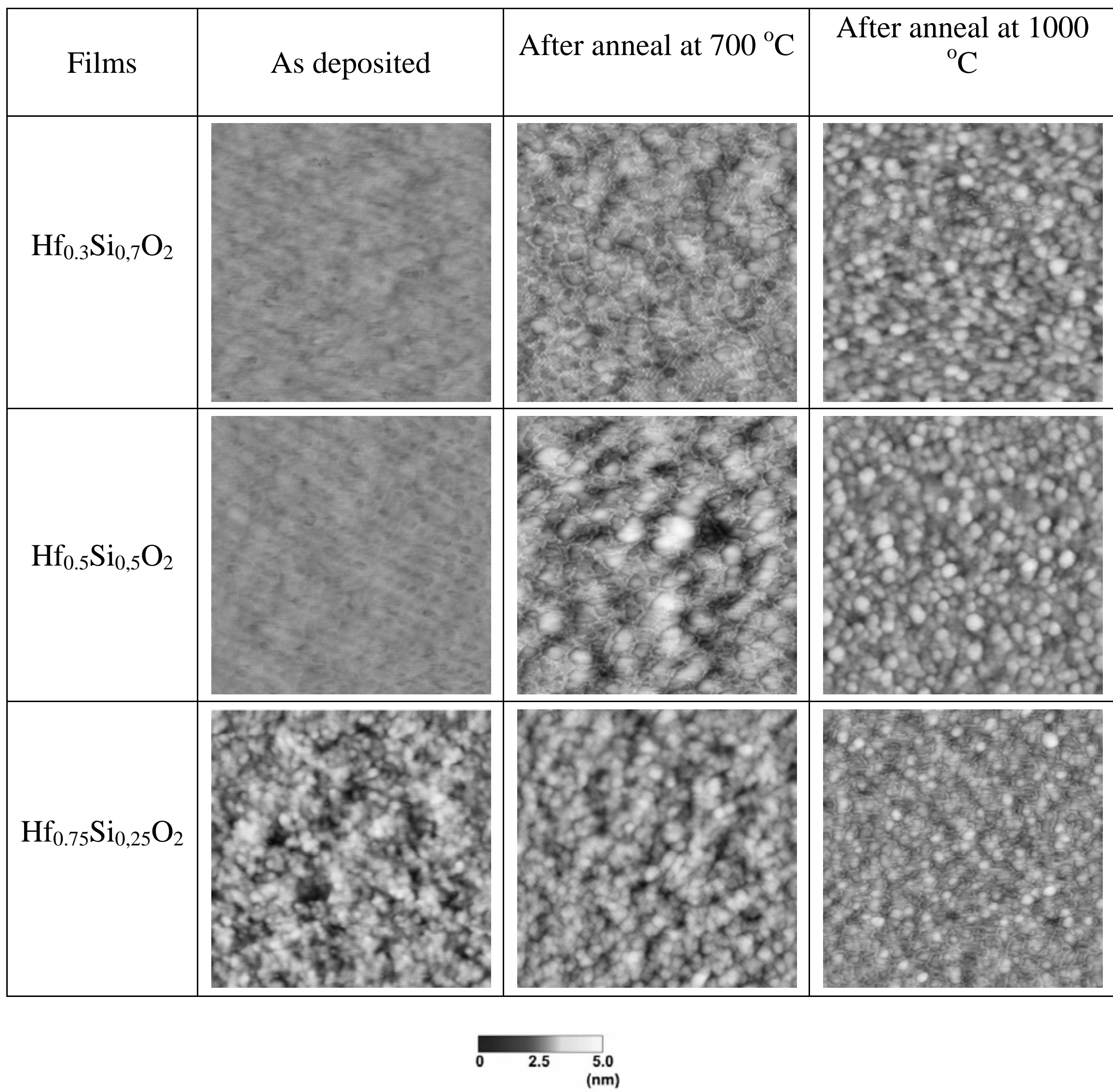


Fig. 2.9 AFM analysis of surfaces of $Hf_xSi_{1-x}O_2$ films with various composition and thermal history, after etching in 1% HF for 1 min.

It can be found that as deposited films of $Hf_xSi_{1-x}O_2$ with x = 0.5 and 0.3 are etched uniformly; however, nano sized island-shaped topography is observed on the surface of as deposited films of $Hf_xSi_{1-x}O_2$ with x = 0.7 and all the annealed $Hf_xSi_{1-x}O_2$ films. Island-shaped topography becomes clearer at higher PDA temperature.

Table 2.2 Atomic ratios reflecting materials composition of Hf based high-K dielectric films after DHF dipping. The results were obtained by XPS with detection angles of 90° and 10°.

Films		HfAlO		HfON	
Elements analyzed		Hf : Al		O : N	
Film history before DHF etching		As-D	PDA	As-D	PDA
Mole ratio	Detection angle of 90°	64 : 36	67 : 33	80 :20	81 : 19
	Detection angle of 10°	63 : 37	68 :32	79 :21	88 : 11

Table 2 cont'd

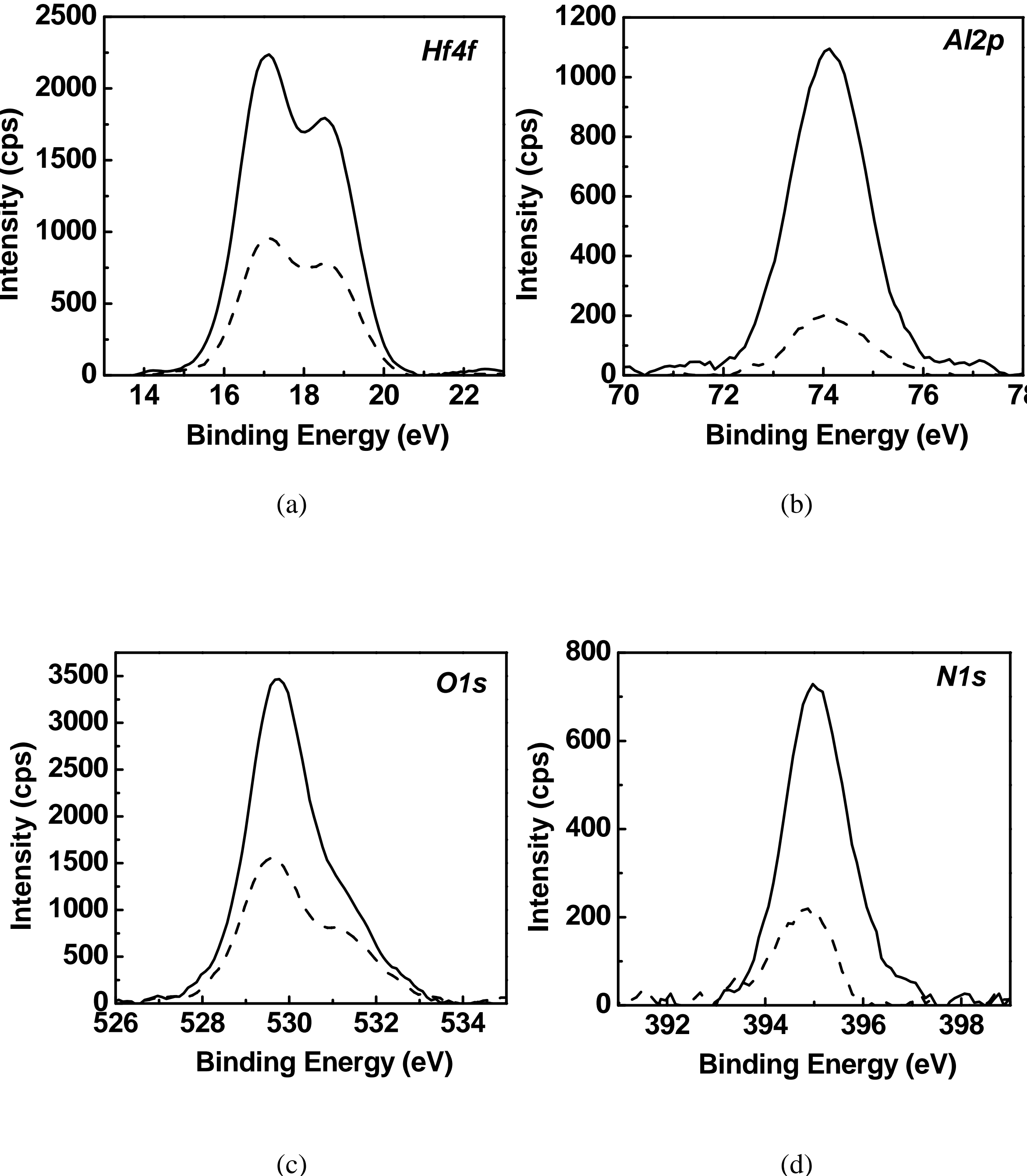
Films		HfSiO1		HfSiO2		HfSiO3	
Elements analyzed		Hf : Si		Hf : Si		Hf : Si	
Film history before DHF etching		As-D	PDA	As-D	PDA	As-D	PDA
Mole ratio	Detection angle of 90°	30 : 70	32 : 68	48 : 52	49 : 51	76 : 24	80 : 20
	Detection angle of 10°	28 : 72	43 : 56	49 : 51	60 : 40	74 : 26	87 : 13

It is known that after high temperature anneal, $Hf_xSi_{1-x}O_2$ separates into amorphous silica and polycrystalline HfO_2 [2.48, 2.49]. Hence it is very likely that island-shaped grains are crystallized HfO_2. Angle resolved XPS results support this assumption. Table 2.2 shows atomic ratios reflecting material composition of Hf based high-K dielectric films after DHF dip. XPS detection angles of 90° and 10° are used to reveal the different composition of the film near the surface and in the bulk. It can be found after DHF dipping, the compositions of the film near the surface and in the bulk of all as deposited $Hf_xSi_{1-x}O_2$ films are very close each other, however, after anneal, the composition of films near the surface becomes Hf rich, indicating that the chemical composition of island-shaped grains is HfO_2.

In Table 2.2, the same trend has been also observed in the etching of HfAlO and HfON, although phase separation via anneal has not been evidenced from these films. This and previous findings from various Hf based high-K dielectric films indicate that etching of Hf based high-K dielectric films by DHF always occurs via their weak points. The weak points include amorphous HfO_2, Al_2O_3, Hf-N bonds, amorphous Hf silicate and SiO_2.

Angle resolved XPS spectra (after 1% DHF dip) of characteristic elements reflecting the composition of the annealed Hf based high-K films are shown in Fig. 2.10. It is observed that, except for N in HfON, there is no change in the chemical states of elements in the films near the surface or in the bulk film, although the composition of the film near the etch front changes. In HfON films, N can bind with either Hf or O. If N binds with O, the binding energy of N*1s* electron will be higher than other normal nitrides as O is more electronegative. Fig. 2.10 (d) shows that after DHF etching, high binding energy signal of N*1s* diminishes when the detection

angle is 10°. This indicates that O-N bonds in HfON are more soluble in DHF compared with Hf-N bonds..



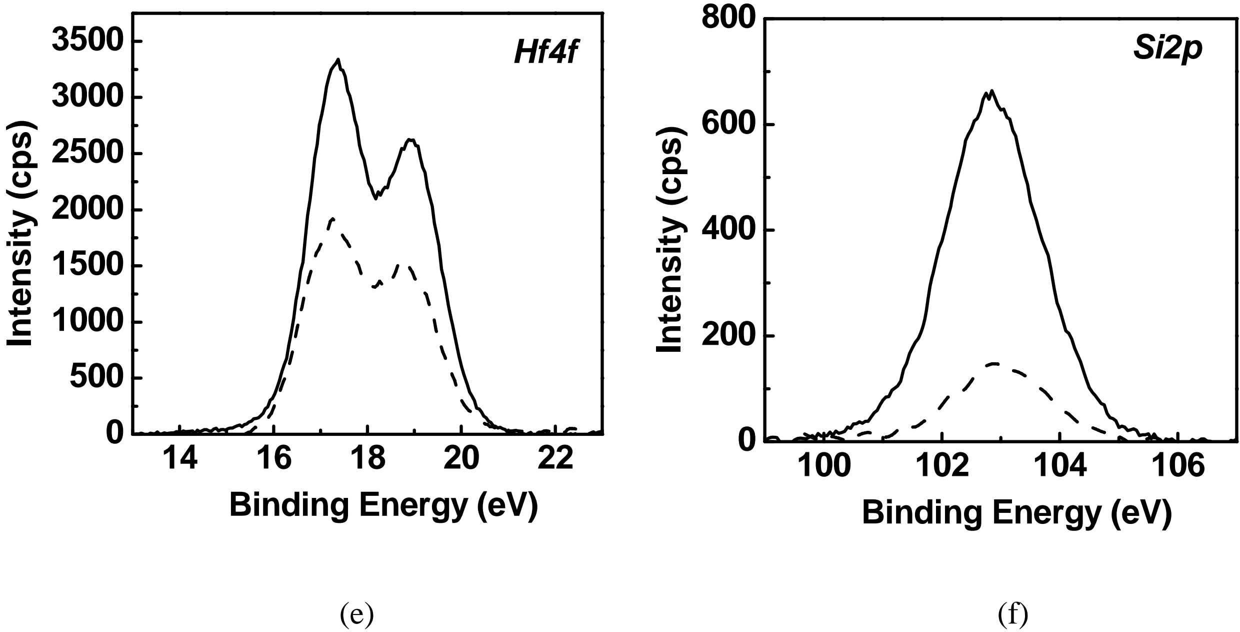


Fig. 2.10 Angle resolved XPS signals from major elements of Hf based high-K dielectric films after DHF etching. XPS signals obtained from detection angle of 90° and 10° are in solid and dashed line, respectively. All films were annealed at 700 ^{o}C for 1 min in N_2.

3.4 Conclusions

The wet etching properties of Hf and HfO_2 in chemicals used for conventional CMOS processing were investigated. HF solutions were found to be the most effective in removing Hf and HfO_2 because of the low activation energy and high solubility of etch byproducts in HF. Generally, the solubility of HfF_4 increases as pH value is reduced. At room temperature, HfF_4 is highly soluble in HF and HCl, but less soluble in concentrated H_2SO_4 and H_3PO_4 and almost insoluble in other solvent solutions. Like SiO_2 etching, HF_2^- and/or H_2F_2 could be the main etching species responsible for etching HfO_2. However, it was found that after HF etching, the Hf and HfO_2 surface becomes terminated by F atoms. This hints that their etching mechanism may be different from that of Si and SiO_2 using aqueous HF.

The etching of Hf based high-K dielectrics in HF and the associated material characterizations of the Hf based high-K dielectrics were performed on as deposited and annealed Hf based high-K films of HfO_2, HfAlO, HfON and $Hf_xSi_{1-x}O_2$. Results show that the etch properties of various Hf based high-K materials are different depending on the annealing treatment. The crystalline phase of HfO_2 is always the main reason for the decrease in the etching rate of all Hf based high-K materials. Etching of Hf based high-K materials using HF occurs via weak points such as amorphous HfO_2, Al_2O_3, Hf-N bonds, amorphous Hf silicate and SiO_2.

In this work, experiments using high temperature HF solutions could not be performed due to the limitation of the wet bench at our facility. Norasetthekul *et. al.* reported that the HF etch rate of HfO_2 film deposited at low temperature increases

with increasing temperature [50]. The ability of high temperature HF solutions to remove crystallized HfO_2 requires further investigation.

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Chapter 3

Effects of N_2, O_2 and Ar Plasma Treatments on Removal of Crystallized HfO_2 Film

3.1 Introduction

In Chapter 1 we have introduced that if Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) continue to be fabricated on planar bulk Si substrates, it is very likely that current polycrystalline Si (poly-Si)/Si oxynitride (SiO_xN_y) gate stacks will be replaced by metallic gate electrode/high-K dielectric gate stacks for sub 45 nm technology nodes [3.1-3.3]. This is to deal with the increased gate leakage density with reduced feature size. By using high-K dielectrics, a larger physical thickness with the same equivalent oxide (SiO_2) thickness (EOT) can be achieved [3.2]. However, the introduction of high-K dielectrics brings significant challenges to the integration of Complementary-Metal-Oxide-Semiconductor (CMOS) process, *e.g.,* gate dielectric removal process after gate electrode patterning [3.4].

According to our previous results [3.5], among the wet chemicals for conventional CMOS process, HF solutions are the most effective for removing Hf based high-K dielectric films. However, after post deposition anneal (PDA) which is necessary right after high-K deposition, the crystallization has the effect to reduce the etch rate of these high-K dielectrics in HF solutions significantly or even to

make them totally insoluble [3.5, 3.6]. Hence, the wet etching alone may be insufficient for the removal process of Hf based high-K gate dielectrics for future CMOS technologies.

Alternative approaches for removing annealed HfO_2 films have been proposed by many researchers. Plasma etching has been proven to etch Hf based high-K materials, regardless of annealing history [3.7-3.11]. However, as plasma etching of Hf based high-K materials is predominated by ion bombardment [3.7, 3.8] and overetching of Si can be accompanied by the reaction with plasma species, it is likely that the plasma etching alone induces recess in source and drain regions, resulting in a large sheet resistance. In addition, most of the etch byproducts of Hf based high-K materials generated from halogen plasmas have low volatility in normal process conditions [9, 10], resulting in a large amount of etch residue remaining on wafer surface. . This makes the cleaning process very challenging [3.9, 3.12].]. Other approaches proposed for the removal of Hf based high-K dielectrics involve wet etching after plasma pre-treatment and ion implantation. It has been reported that the etch rate of crystallized HfO_2 in HF solutions can be enhanced after Ar or O_2 plasma treatment [3.13, 3.14] or ion implantation [3.15].

With regards to ion implantation enhanced wet etching, researchers found that after Ar, As, Si or Ge implantation with a dosage of $10^{15}/cm^2$, the wet etching rate of HfO_2 film annealed at 550 ^oC is around 1.5 - 2 Å/min in 1: 15 HF [3.15]. This is still too low to remove 20 - 30 Å (EOT = ~7 Å) thick HfO_2 for the 45 nm technology node [3.1]. Long time etching in HF solution is undesirable, because some isolation regions, *e.g.* shallow trench insulation (STI), can be significantly eroded due to the nonuniformity in thickness of the remaining high-K layer. Note

that the amount of damage generated by ion implantation with common dose for source and drain formation cannot enhance the wet etch rate of crystallized HfO_2. The dose is a parameter to be adjusted not to meet the requirement of removal process but to accurately control the electrical property of P-N junctions formed around source and drain regions.

In high density Ar and O_2 plasma treatment processes for enhancing the wet etch rate of crystallized HfO_2 [3.13, 3.14], the penetration of ions into Si can be significantly suppressed due to the low ion energy, hence these processes do not change the electrical performance of P-N junctions at source and drain. Furthermore, the damage in high-K layer can be adjusted by ion energy and process time to meet the requirement of etching rate in dilute HF (DHF) [3.13, 3.14].

Nonetheless, there are still some considerations in implementing this technique into CMOS process. In Fig. 1, the main steps of the proposed plasma treatment to enhance the DHF wet etching of high-K dielectric are illustrated. The CMOS gate stack structure before plasma etching is shown in Fig. 1 (a). The SiO_2 isolation region, *e.g.,* shallow trench isolation (STI), tends to be slightly higher to compensate for the oxide loss in cleaning processes. Since the high-K gate dielectric film is directly deposited on Si substrate and SiO_2, etching selectivity of high-K to both Si and SiO_2 must be taken into account. It is known that recesses at the isolation region will cause threshold voltage instability and degradation of the sub threshold slope [3.16]. Recesses at source and drain regions are also known to decrease drive current, causing reduction in the operation speed of the circuit.

Due to the non-uniform removal of gate dielectric during the over etch step of gate etching, the high-K film can be very thin in some areas as shown in Fig. 3.1

(b During the plasma treatment, some ions can penetrate these areas to damage the underlying Si substrate and SiO_2 isolation regions. This results in recesses in these regions due to the faster etching rate in the subsequent DHF, as shown in Figs. 3.1 (c) and (d). Therefore, recesses induced by plasma treatment for enhancing the wet etching rate of high-K dielectrics must be minimized.

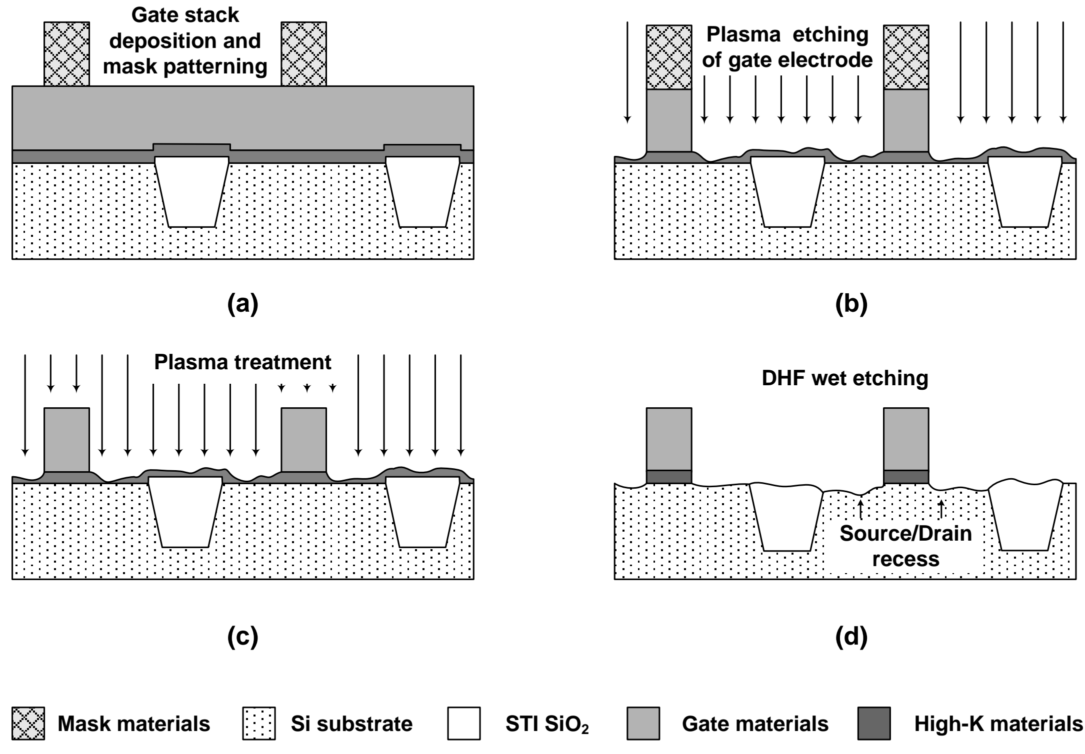


Fig. 3.1 Illustrations of the etching steps of a high-K gate stack including plasma treatment enhanced wet etching using DHF: (a) Surface topography of each film of the gate stack before gate etching; (b) surface topography and thickness non-uniformity of high-K gate dielectric layer after gate electrode etching; (c) plasma treatment to change the wet etching properties of high-K gate dielectric layer and (d) possible surface topographies of Si substrate and STI SiO_2 after plasma treatment enhanced wet etching of high-K dielectric in DHF.

In the Chapter 2, we have found that the etch rate of Hf based high-K dielectrics in HF solutions can be increased by introducing "weak points" to the films, such as metallic HfO_x ($x < 2$), amorphous HfO_2, Hf-N, Al-O and Si-O bonds [3.5, 3.13].

In this Chapter, we will introduce metallic HfO_x, amorphous HfO_2 and Hf-N bonds to crystallized HfO_2 films using various plasma treatment and nitridation methods such including Ar plasma treatment, annealing in the NH_3 ambient and N_2 plasma treatment. The damage induced in source, drain, SiO_2 isolation regions, and the efficiency of increasing the etch rate of crystallized HfO_2 in DHF by N_2, O_2 and Ar plasma treatments were evaluated and compared. We also attempt to reveal the change in materials properties due to the plasma treatment processes by x-ray photoelectron spectroscopy (XPS) and simulation. Transmission electron microscopy (TEM), scanning electron microscopy, X-ray diffraction (XRD) and atomic force microscopy (AFM) were also used for materials characterization and evaluation of procecss.

3.2 Experimental Setup

In this work, HfO_2 films were deposited on *p*-type Si (100) wafers using an atomic layer chemical vapor deposition (ALCVD) system or a metal organic chemical vapor deposition (MOCVD) system at a substrate temperature of 300 ^oC. In ALCVD process, precursors of $HfCl_4$ and H_2O reactant were used. In MOCVD process, the precursor of $Hf(OC(CH_3)_3)_4$ precursor was used and carried by Ar at a pressure of 400mTorr with an O_2 flow rate of 50sccm.

PDAs at 700 ^oC and 1000 ^oC were performed in N_2 ambient for 60 s using a rapid thermal process system. Silicon-on-isolator (SOI) wafers were used to evaluate the damage of the Si substrate as the Si loss can be easily measured by ellipsometry using SOI wafer. In this work, all the thicknesses were measured using a multi-wavelength ellipsometer. Plasma treatments using N_2, O_2 and Ar were performed in an inductively coupled plasma (ICP) system (Manufactured by Korean Vacuum Technologies, type: KVT 2000) at room temperature. A schematic of the ICP system is shown in Fig. 3.2. In this ICP system, wafers are hold using step height on the electrode and gravity of the wafer, a 5.75 turns inductive coils was used to generate plasma, and a capacitive electrode was used to provide bombardment energy of ion gas inlet is on the sidewall of the chamber.

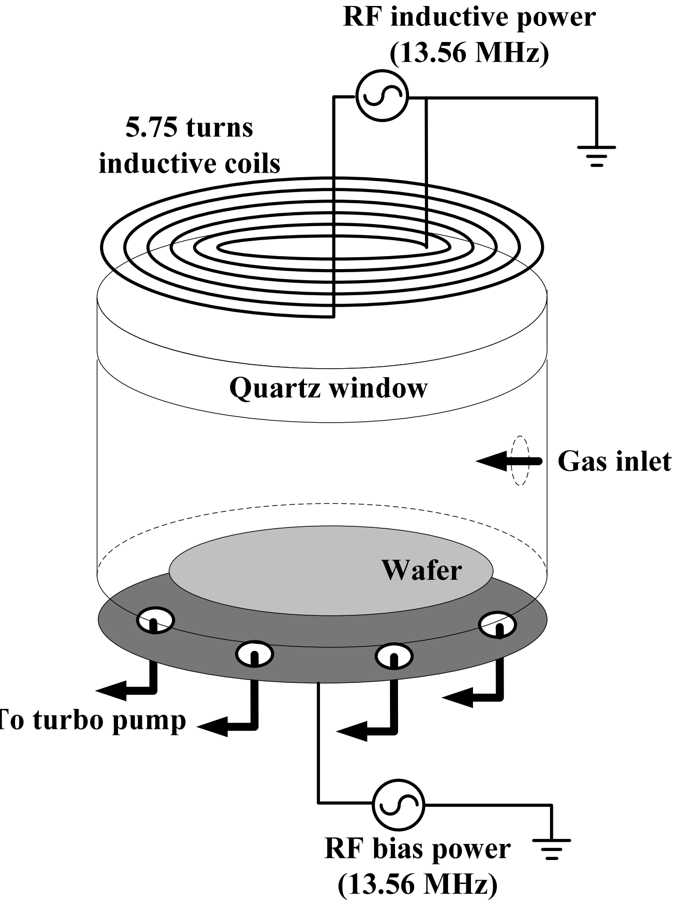


Fig. 3.2 Schematic of ICP system used in the work of chapter 3

In ICP systems, plasma is generated by the inductive power and ion bombardment is provided by the RF bias power and ion energy is depend the DC bias voltage in RF bias power. Although due to applying RF bias power, plasma density increases, we can assume that it doest not influence the plasma density because its efficiency of generating plasma is much lower (1-2 orders) than inductive power. At the same time, to increase the plasma density by increasing inductive power, wafers are not bombarded because of the induction electric field is along the direction of plane parallel to the wafer surface, as shown in Fig. 3.3. Therefore, the ion density and ion energy can be controlled separately. This can help to understand different effect of ion density and ion energy in the plasma treatment process.

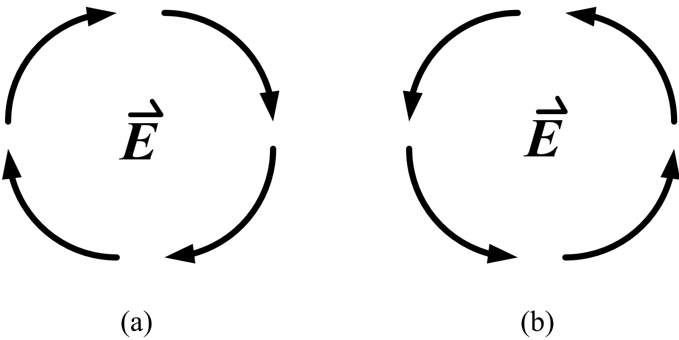


Fig. 3.3 Top view of induction electric field vectors in (a) the first half cycle and (b) the second half cycle of RF inductive power of the ICP system

In the plasma treatment process, the inductive power, gas flow and pressure were fixed at 200 W, 30 sccm and 10 mTorr respectively unless indicated otherwise.

To evaluate the extent of damage due to plasma treatment on isolation regions, chemical vapor deposited SiO_2 films on Si were prepared using tetraethyl orthosilicate source at 800^oC in a furnace tube. The injection depths of N_2, O_2 and

Ar ions in HfO_2 and its underlayer were calculated by the simulation using the Stopping and Range of Ions in Matter (SRIM) - 2003 Monte Carlo code [3.17, 3.18]. The analysis of the XPS results was based on the cited references [3.19, 3.20].

3.3 Results and Discussion

3.3.1 Effects of Ar plasma treatment on the HF removal of crystallized HfO_2

To increase etch rates of annealed HfO_2 in dilute HF, we used ICP using Ar that can effectively induce ion bombardment onto the surface of the HfO_2 films. After the Ar bombardment, the etch rates in HF for HfO_2 annealed both at 700°C and 1000°C increased significantly. By adjusting bias power and process time for ICP, the annealed HfO_2 was completely removed in the subsequent HF etch process at the rates of up to 90 Å/min, even after anneal at 1000°C.: see Fig. 3.4.

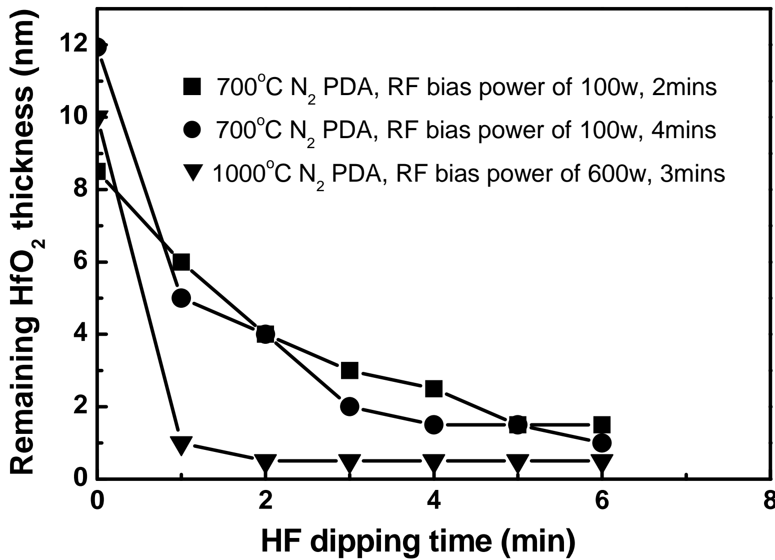


Fig. 3.4 Remaining thicknesses of HfO_2 after Ar plasma treatment and 10% HF wet etching. The other ICP parameters are fixed at a source power of 300W, a pressure of 10mTorr, and an Ar gas flow of 60sccm.

It can be found that with increased RF bias power and plasma treatment time, the etch rate of HfO_2 increases and increasing RF bias power is more efficient than increasing plasma treatment time. We suggest that this could be because that the ICP is a high density plasma source, with fixed RF bias power, it can induce a large amount of damage in HfO_2. In Fig. 3.4, it can be found that after plasma treatment, all films can be etched in 2 mins, and in the first min, the etch rate can achieve 90 Å/min, supporting this suggestion.

3.3.2 Effects of thermal nitridation and plasma nitridation on the HF removal properties of crystallized HfO_2

Thermal nitridation and plasma nitridation were applied to HfO_2 films after PDA at 700 °C. We found that after thermal nitridation at 700 °C or 900 °C in a NH_3 ambient, both 1 % DHF and 49 % concentrated HF cannot etch HfO_2. This could be due to the very stable Hf-O bonds formed after PDA. The standard heat of formation of Hf-N bond is 536 KJ/mol, whereas that of Hf-O bond of 801 KJ/mol [3.21]. This may explain that it is difficult to break the stable Hf-O bonds and to replace them by Hf-N bonds, via annealing in NH_3 ambient.

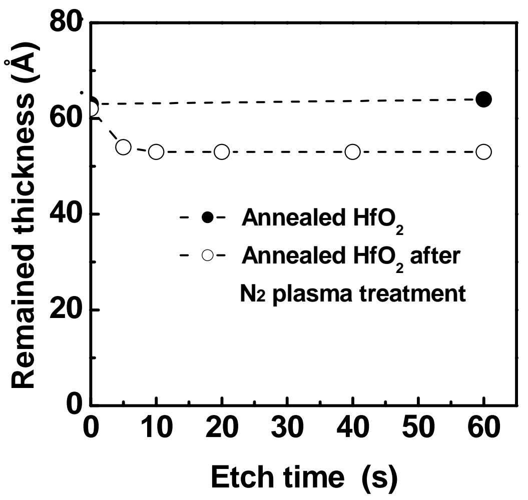
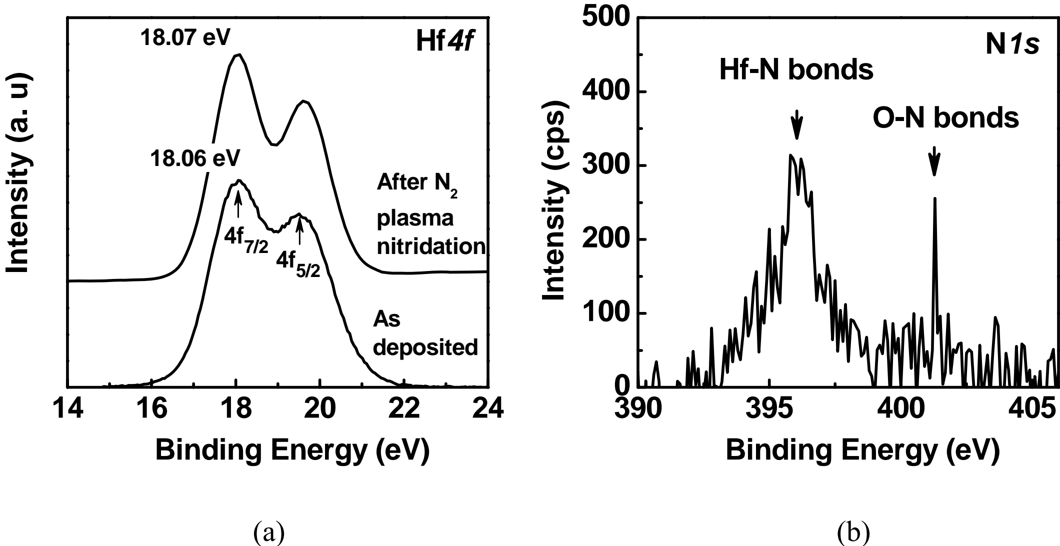


Fig. 3.5 Comparison of remaining thickness of HfO_2 as a function of etching time in 1% DHF with and without N_2 plasma nitridation. Thickness of HfO_2 is ~60Å, right after annealing at 700°C.

Plasma nitridation was also performed on 60 Å thick HfO_2 films using ICP without applying bias voltage. In nitridation process, N_2 gas flow, pressure, inductive power and treatment time were 30 sccm, 10 mTorr, 200 W, and 1 min, respectively. In Fig. 3.5, the remaining thickness of HfO_2 films before and after plasma nitridation as a function of wet etching time is shown.

It can be observed that ~10 Å thick film can be removed in 5 s by 1 % DHF after plasma nitridation, but the film cannot be etched further. Hf*4f* signals from the HfO_2 surfaces before and after N_2 plasma nitridation and N*1s* signal from the HfO_2 surface were scanned using XPS after N_2 plasma nitridation are shown in Figs. 3.6 (a) and (b).



(a) (b)

Fig. 3.6 ((a) Hf*4f* signal of XPS taken from the HfO_2 dielectric surfaces before and after N_2 plasma nitridation and (b) N*1s* signal of XPS taken from the HfO_2 dielectric surfaces after N_2 plasma nitridation without bias voltage.

It can be observed that after plasma nitridation, the Hf*4f* peak did not change significantly although N can be detected. This implies that the extent of nitridation is

very insignificant. Plasma nitridation with higher inductive power (up to 600 W) and longer treatment time (up to 5 mins) was conducted on the annealed HfO_2 films, but no further enhancement in the wet etching of HfO_2 in DHF was observed. This indicates that plasma nitridation using the above conditions only helps to lower the wet etching resistance of crystallized HfO_2 within 10 Å from the surface. It can be anticipated that at least 20 - 30 Å thick HfO_2 need to be formed considering the presence of the interfacial layer and the K value (around 24) of HfO_2 [3.1-3.2]. That is common nitridation techniques do not seem to be feasible for removal process of crystallized HfO_2 film.

3.3.3 Effects of N_2 plasma treatment on the HF removal properties of crystallized HfO_2

We found that applying bias voltage in plasma nitridation helps to lower the wet etching resistance of thicker crystallized HfO_2 film in DHF solution. 100 Å thick HfO_2 films were subjected to N_2, O_2 and Ar plasma treatment after PDA at 700 ^oC. In Fig. 3.7, the remaining thickness of crystallized HfO_2 as the function dipping time in 1% DHF after plasma treatment with various bias powers is shown. Similar to Ar plasma treatment, with increased RF bias power, the wet etch rate of HfO_2 in DHF increases.

It can be found that after applying bias power of 300 W to 600 W, much thicker crystallized HfO_2 becomes dissoluble in HF, compared with plasma nitridation with out bias power. In ICP process, DC component in RF bias power provides ion energy, this is reason why nitrogen ion can penetrate thick HfO_2 film. Since plasma treatment using ICP can provide very high damage density because of

the high density of ICP, ion energy is a key factor influencing the dissoluble thickness of HfO_2. In the next section, we will study the effect of ion energy on the removal of HfO_2, as well as the damage of the substrate.

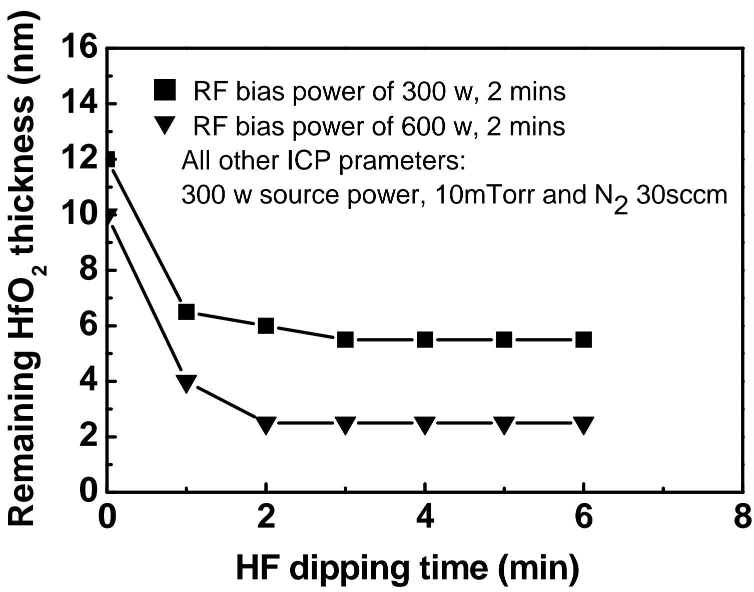


Fig. 3.7 Remaining thicknesses of HfO_2 after N_2 plasma treatment and 1% DHF wet etching.

3.3.4 Comparison of N_2, O_2 and Ar plasma treatments on the removal on crystallized HfO_2, and recess in Si and SiO_2

Figure 3.8 (a) shows the thickness of dissoluble HfO_2 in wet etching after plasma treatment as a function of ion energy. The wet etching time required for DHF process is only 30 s after plasma treatment for 1 min, showing that plasma treatment can substantial damage in HfO_2 in a short time. With increasing ion energy via increasing bias voltage during N_2 and Ar plasma treatment, the soluble thickness of crystallized HfO_2 in DHF solution increases linearly. With the same ion energy, N_2 plasma is more effective in reducing the wet etching resistance of

crystallized HfO_2 compared with Ar plasma. Unlike Ar ions, which provide only physical bombardment, N ions can chemically react with HfO_2 to form Hf-N bonds, further enhancing the removal rate of crystallized HfO_2 in HF [3.5].

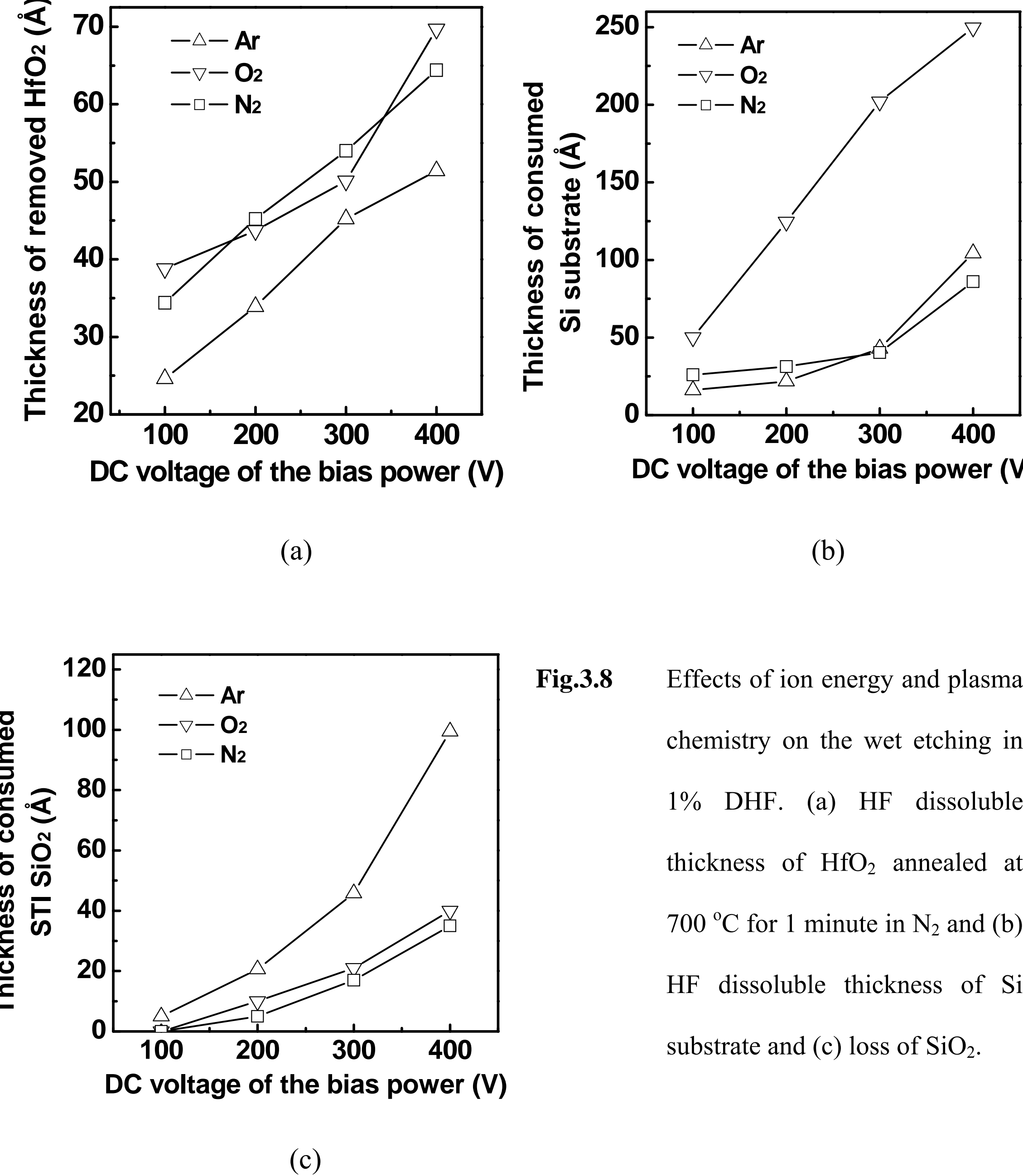


Fig.3.8 Effects of ion energy and plasma chemistry on the wet etching in 1% DHF. (a) HF dissoluble thickness of HfO_2 annealed at 700 ^{o}C for 1 minute in N_2 and (b) HF dissoluble thickness of Si substrate and (c) loss of SiO_2.

The dependence of the dissoluble thickness of crystallized HfO_2 in 1% DHF on ion energy using O_2 plasma treatment is different from that using Ar and N_2

plasma treatment. As the ion energy increases, the wet etching rate increases faster than that using N_2 or Ar plasma treatment. Donnelly *et al.* [3.22] and Vallier *et al.* [3.23] reported that Si oxide grows under the thin gate oxide during the over etch step of poly-Si gate etching process. Vitale *et al.* have found that oxidation occurs easily if O ions penetrate SiO_2, with an activation energy as small as 0.02 eV [3.24]. Although the penetration mechanism of O ions in HfO_2 is unknown, oxidation of Si substrate under thin HfO_2 film has already been observed [3.25]. Oxidation of Si results in volume expansion [3.16], which can affect the integrity of the HfO_2 film. SiO_2 formed can be easily etched by DHF. Once the SiO_2 underlayer is etched by DHF, neighboring area of HfO_2 film can also be removed although crystallized HfO_2 is insoluble. This may explain that, O_2 plasma treatment can lower the wet etching resistance of crystallized HfO_2 in HF solution more compared with the plasma treatment using Ar or N_2, when ion energy is high, *e.g.* ~ 400 eV. However, the oxidation of Si consumes Si substrate significantly to result in deep recess after DHF etching, although it can lead to the faster removal of HfO_2 film.

Figure 3.8 (b) shows the dissoluble thickness of Si on SOI wafers in 1% DHF after the N_2, O_2 or Ar plasma treatment under the same condition used in Fig. 3.4 (a). It can be observed that, with increasing ion energy, the DHF dissoluble thickness increases significantly after O_2 plasma treatment whereas a less significant increase is observed after N_2 or Ar plasma treatment. Since Ar is chemically inert, Ar plasma treatment cannot change the chemical composition of the Si substrate. Considering that it is very difficult to etch single crystal Si by 1% DHF [3.16], it is understood that the small consumption of Si substrate after Ar plasma treatment and DHF dipping is due to the damage induced by Ar ion bombardment. Although N_2

plasma can also damage Si substrate, the damage induced by N_2 plasma treatment could be much smaller as the mass of N ions is much smaller compared with Ar ions. But the N_2 plasma can cause nitridation of the Si surface, forming Si nitrides. These nitrides formed at room temperature are not well bonded, thus they can also be etched by DHF. Hence a combination of damage and nitridation in N_2 plasma treatment results in a similar soluble thickness after Ar plasma treatment. The large loss of Si thickness resulting from O_2 plasma treatment could be due to the growth of SiO_2.

Figure 3.8 (c) shows the SiO_2 damage induced by N_2, O_2 and Ar plasma treatments. Unlike Si and HfO_2, the difference in SiO_2 thicknesses before and after ion bombardment was used to show the extent of damage to SiO_2. DHF dipping process is no longer used in this experiment because HF can etch SiO_2 easily [3.16]. It can be observed that for the same ion energy, O and N ions induce less damage than Ar ions. This could be due to the loss in SiO_2 thickness resulted from sputtering, where Ar ion is more effective than N_2 and O_2 due to its large mass. Since Ar is chemically inert, it neither reoxidizes nor nitridizes etch by products, but results in redeposition.

In current CMOS process, the loss of SiO_2 in isolation (*e. g.* STI) regions can be recovered by increasing the remaining oxide thickness after planarization using chemical mechanical polishing [3.26]. Hence the loss of SiO_2 in STI regions due to plasma treatment process may not be as serious as the recess in source and drain regions. Nevertheless, it can be found from Fig. 3.4 that, N_2 plasma treatment with few hundred eV induces the least damage in source, drain and SiO_2 regions among

the three different types of plasma treatments studied in this work, being the most desirable for the removal of crystallized HfO_2.

In table 3.1, we summarized the surface roughness induced by N_2, O_2 and Ar plasma treatments with an ion energy of 400 eV for 1 min followed by 1% DHF etching for 30 s. It was observed that all the three types of plasma treatment do not induce significant increase of surface roughness, especially for the O_2 and N_2 plasma treatments.

Table. 3.1 Summary of surface roughness denoted by Root Mean Square (RMS) of Si substrate after plasma treatments using Ar, N_2 and O_2 with DC bias voltage of 400 V for 2 minutes, followed by 1% DHF etching for 1 min. The surface roughness of bare Si is ~9 Å.

Plasma chemistry	Ar	N_2	O_2
RMS (nm) after plasma treatment	2.68	0.96	0.93
RMS (nm) after wet etching in 1% DHF for 1 min	2.03	0.69	1.04

N_2 plasma treatment (DC bias voltage of 200 V for 1 min) was performed on a 40 Å remaining HfO_2 film after the etching of a TaN/HfO_2 gate stack with original HfO_2 thickness of 60 Å. After plasma treatment, the wafer was then cleaned using 1 % DHF for 30 s. After the water rinsing for 5 mins, the cleanliness of Si surface was evaluated by XPS analysis, as shown in Figs. 3.9. No Hf can be detected from the surface. It resembles a typical Si surface with native oxide, and this confirms that a very clean surface can be obtained.

(a)

(b)

(c)

Fig. 3.9 Evaluation of the surface cleanliness of Si substrate by scanning ranges of electron binding energy of (a) Hf*4f*, (b) Si*2p* and (c) O*1s* of XPS. Cleaning process was performed to a remaining HfO_2 film with a thickness of 40 Å after PDA at 700 ^{o}C for 1 minute in N_2 on Si substrate using 1% DHF cleaning for 30 s. Before DHF cleaning, N_2 plasma treatment with DC bias voltage of 200 V was performed for 1 min.

In Fig. 3.10, a cross-sectional scanning electron microscopy image shows that there is no measurable recess in open area.

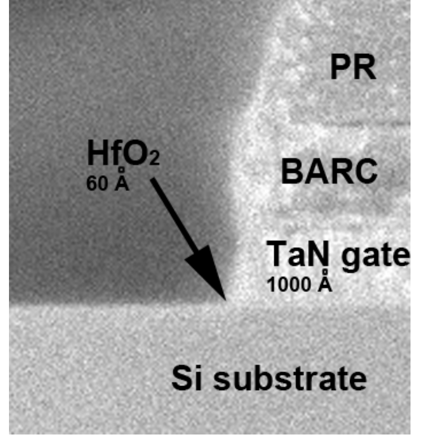
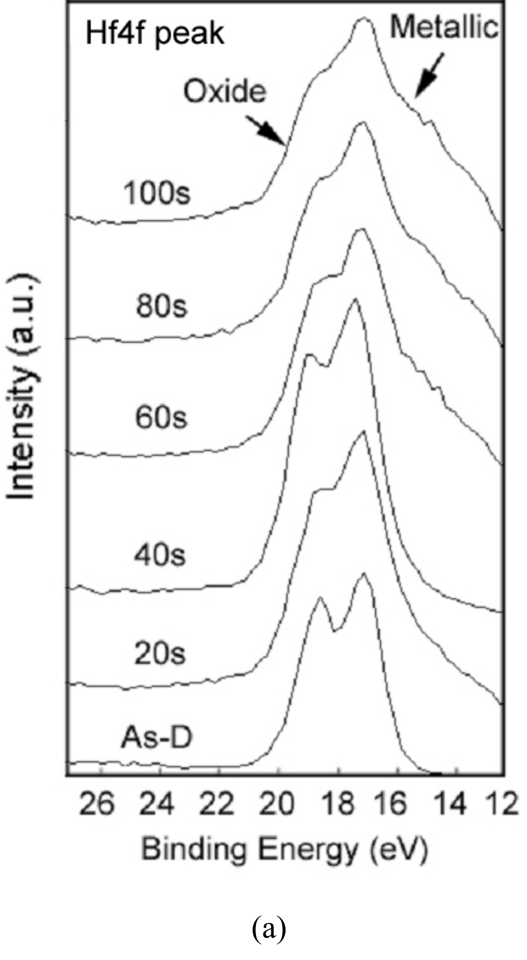


Fig. 3.10 Cross-sectional SEM of TaN/HfO_2 gate after removal process used in Fig. 3.8 (BARC: bottom antireflective coating, PR: photoresist).

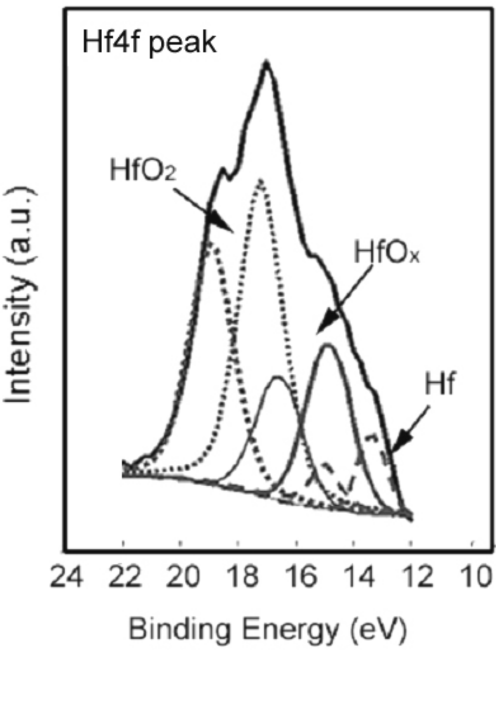
3.3.5 Investigation of mechanisms of plasma treatment process of HfO_2/Si stack using XPS

The extent of the etch rate enhancement of crystallized HfO_2 is different for N_2, O_2 and Ar plasma treatments, thus mechanisms responsible for this difference need to be understood. Furthermore, since the damage in source and drain region is critical to electrical performance but difficult to avoid, it is necessary to understand phenomena occurring to the Si underlayer during the plasma treatment processes.

A. Ar plasma treatment



(a)



(b)

Fig. 3.11 (a) Hf*4f* peaks from XPS for Ar bombarded HfO_2 (b) Fitting curve of Hf*4f* peak from HfO_2 after Ar plasma treatment for 70 s. Ion energy was fixed at 100 eV.

In Fig. 3.11, the change in the chemical state of Hf in 60 Å thick crystallized HfO_2 after Ar plasma treatment was shown by the Hf*4f* XPS signal. It can be found that Hf*4f* peak becomes broader after the Ar ion bombardment, implying the formation of Hf and HfO_x ($x < 2$). The strongest Hf peak in XPS can be obtained from the binding energy of Hf4f. The energy range of Hf*4f* is from 14 - 18 eV for Hf and from 16 - 22 eV for HfO_2. According to the fitting results in Fig. 4 (b), at least three Hf related peaks are detected after the Ar ion bombardment: HfO_2, HfO_x and Hf. This can be attributed to the preferential sputtering of O to Hf by Ar ions due to differences in binding energies and masses between Hf and O in HfO_2 [3.27, 3.28]. The XPS results in Fig. 3.11 shows that many Hf-O bonds may have broken after the Ar ion bombardment. Breaking Hf-O results the change of microstructure of HfO_2 film from crystal phase changing to amorphous phase. The structural change of HfO_2 during ion beam assisted deposition was reported by Alvisi *et al.* [19], in which the HfO_2 phase was transformed from the monoclinic structure, via the amorphous structure, to the cubic structure with increasing ion energy. Our results also showed transformation of the HfO_2 phase from the monoclinic structure (XRD peaks at 28.3^o and 31.6^o) to the amorphous structure. The HF etching of the amorphized HfO_x after the Ar ion bombardment became faster. There were reports on the increase of etch rates in dilute HF after ion implantation onto HfO_2 [15], Al_2O_3 [29], Si_3N_4 [30], and SiC [31]. However, their work used high ion energy in the range of 10 - 360 keV for films in the thickness range of 100 - 1000Å, whereas our work used low ion energy below ~ 400 eV for thin HfO_2 films of ~100 Å. In summary, the mechanism of enhancement of wet removal rate of crystallized HfO_2 after Ar plasma treatment is the formation of metallic HfO_x and amorphous HfO_2

B. N_2 and O_2 plasma treatment

In Fig. 3.12 (a) and (b), the change in the chemical state of Hf in 60 Å thick crystallized HfO_2 films after N_2 and O_2 plasma treatment was shown by the Hf*4f* XPS signal.

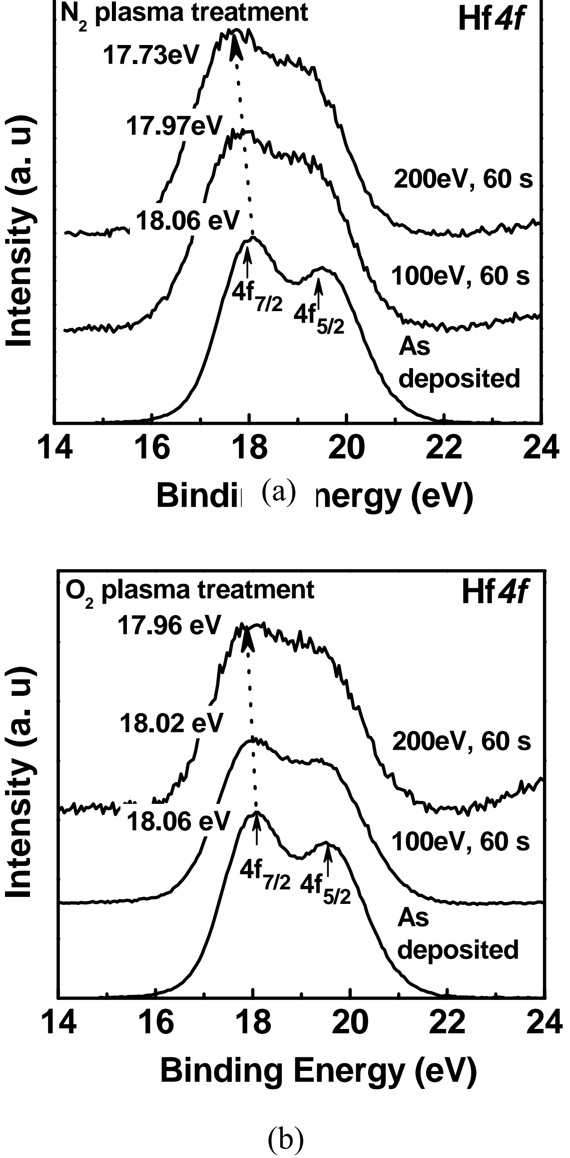


Fig. 3.12 Hf*4f* signals of XPS taken from HfO_2 films with thickness of 60 Å after (a) N_2 plasma treatment and (b) O_2 plasma treatment with ion energies of 100 eV and 200 eV. The Hf*4f* signal of XPS taken from a HfO_2 film before plasma treatment is shown in each figure as a reference.

Unlike N_2 plasma nitridation without bias voltage, both $4f_{7/2}$ and $4f_{5/2}$ of Hf*4f* signal shift to lower binding energy from the binding energy of Hf*4f* electrons in HfO_2. This shift increases with increasing ion energy. The splitting becomes unclear after plasma treatments, indicating that the HfO_2 film is no longer pure HfO_2. Beside HfO_2, some other Hf compounds, in which Hf atoms are bonded to less O atoms or less electronegative species compared with O atoms, have formed [3.13]. Considering that ion bombardment can break Hf-O bonds and preferentially sputter O atoms because of the different masses between Hf and O [3.13, 3.27], Hf metallic bonds, *i. e*. HfO_x, ($x<2$), should form. Breaking of Hf-O bonds can also change the crystallized HfO_2 film to an amorphous state.

In Fig. 3.13 (a), XPS signal of N*1s* electrons is acquired from the surface of 60 Å thick HfO_2 films after N_2 plasma treatment. Obvious N*1s* signal is detected, implying that N has been incorporated into HfO_2 to form Hf-N bonds. We have reported that amorphous HfO_2, Hf metallic bonds and Hf-N bonds can be etched by HF solutions easily [5], therefore the mechanism responsible for the enhancement of etch rate of crystallized HfO_2 using N_2 plasma treatment is the formation of HF dissoluble species including metallic HfO_x, amorphous HfO_2 and Hf-N bonds.

Compared with N_2 plasma treatment with the same ion energy, the shift from O_2 plasma treatment is smaller, as shown in Fig. 3.12 (b). This can be explained in the way that, although energetic O ions can break Hf-O bonds and sputter O atoms from HfO_2 films, injected O ions can also take up some broken Hf-O bonds, which is different from the formation of Hf-N bonds after N_2 plasma treatment. Therefore we consider that the etch rate enhancement of crystallized HfO_2 using O_2 plasma

treatment is originated from the formation of amorphous HfO_2 and oxygen-deficient HfO_x.

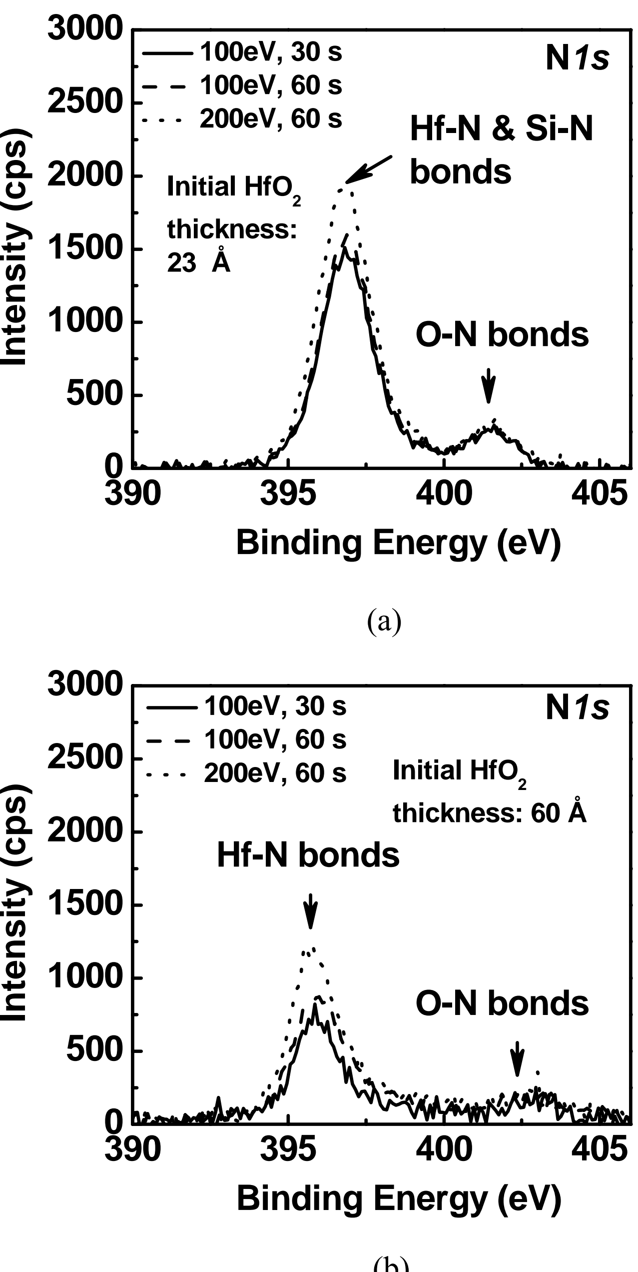


Fig. 3.13 N*1s* signals of XPS taken from (a) 60 Å thick HfO_2 film and (b) 23 Å thick HfO_2 film after N_2 plasma treatment, with various ion energy and treatment time.

In Figs. 3.13 (a) and (b), the chemical state of nitrides detected from the thick (60 Å) and thin (23 Å) crystallized HfO_2 films after N_2 plasma treatment with

various ion energy and treatment time is shown. In both films, ionic and covalent N bonds are found. Considering that only Hf, O can Si can bond to N, it is interpreted that covalent bonds may be O-N bonds and ionic bonds may be Hf-N bonds, Si-N bonds or their combination. The extent of nitridation increases with increasing ion energy but saturates when the treatment time is longer than 30 s.

It is interesting that the binding energy of N*1s* electrons detected from thin HfO_2 films is higher than that from thick HfO_2 films. Since Si is more electronegative than Hf [3.21], the binding energy of N*1s* electron in Si-N bonds is higher than that in Hf-N bonds. Therefore, we consider that N*1s* signals from thin HfO_2 films originate from both Hf-N and Si-N bonds whereas signals from thick HfO_2 films originate only from Hf-N bonds. This is because N ions can penetrate thin HfO_2 films and react with the Si underlayer and interfacial oxide, forming Si nitride or oxynitride, whereas N ions cannot penetrate thick HfO_2 films. Another interesting finding is that the intensity of N*1s* signals detected from thin HfO_2 films is higher than from thick HfO_2 films, when the ion energy and duration of plasma treatment on both films are the same. This indicates that plasma nitridation occurs more easily on Si and SiO_2 than on HfO_2.

Figures 3.14 (a) and (b) show the chemical change on the Si substrate covered by 60 Å thick HfO_2 films after N_2 and O_2 plasma treatments, respectively. . Si*2p* signals are taken from films before plasma treatment and after plasma treatment with 100 eV and 200 eV ion energy for 60 s.

It can be observed from Fig. 3.9 (b) that when ion energy higher than 200 eV, oxide peak of Si*2p* signal increases significantly, indicating that O ions can penetrate 60 Å thick HfO_2 and oxidize Si substrate with this high ion energy. After

N_2 plasma treatment with ion energy of either 100 or 200 eV, the Si*2p* signals are almost the same with the signal taken before treatment, showing that compared with O_2 plasma treatment, N_2 plasma treatment affects Si substrate much less when it's covered with 60 Å thick HfO_2. This also proves that the ionic N bonds found in Fig. 3.7 (a) are primarily Hf-N bonds. Hence, we can propose that N_2 plasma treatment is a better choice than O_2 plasma treatment in minimizing the substrate damage as well as in lowering the etch resistance of thick crystallized HfO_2 films.

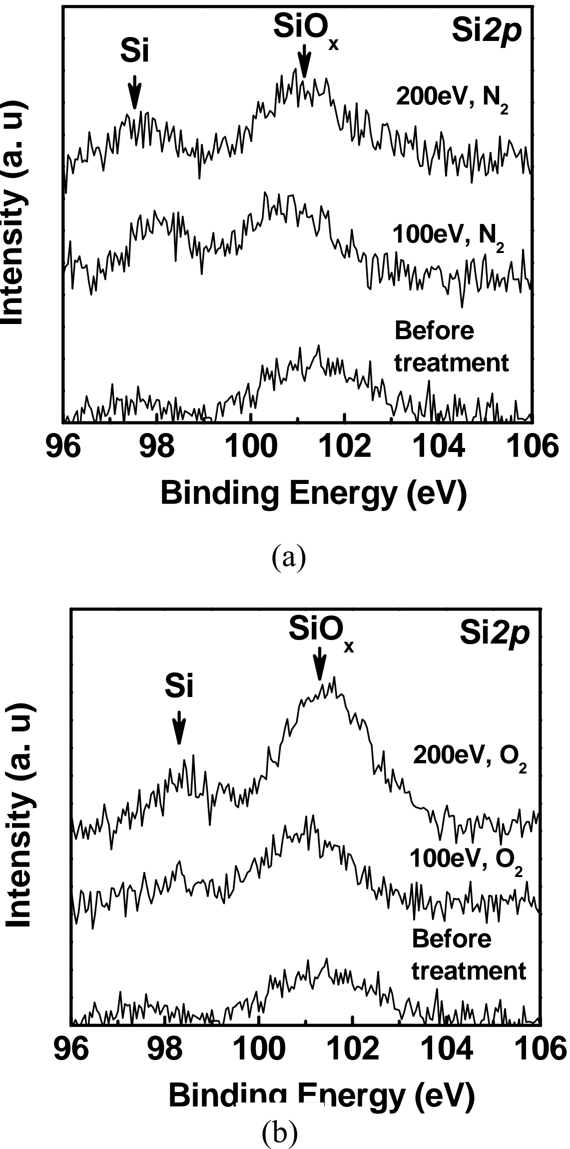


Fig. 3.14 Si*1s* signals of XPS taken from 60 Å thick HfO_2 film after (a) N_2 plasma treatment and (b) O_2 plasma treatment, with ion energies of 100 eV and 200 eV.

Figures 3.15 (a) and (b) show the chemical change of the Si substrate under 23 Å thick HfO_2 films after N_2 and O_2 plasma treatments with various treatment time and ion energy.

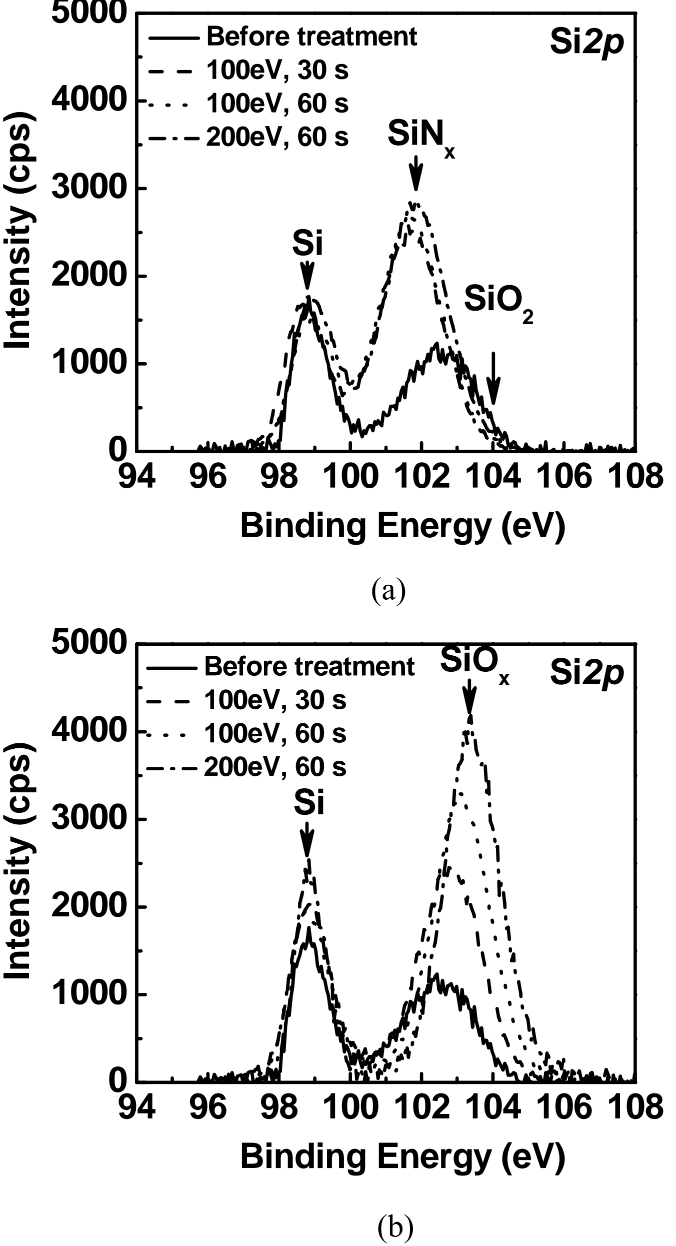


Fig. 3.15 Si2*p* signals of XPS taken from HfO_2 films before plasma treatment and HfO_2 films with (a) N_2 plasma treatment and (b) O_2 plasma treatment with ion energies of 100 eV for 30 s and 60 s, and 200 eV for 60 s.

It can be observed that with increased treatment time and ion energy, the amount of Si nitrides does not increase significantly but saturates after some time. With increasing treatment time and ion energy, the amount of Si oxides keeps increasing and the binding energy of the oxide component of Si*2p* keeps shifting to higher energy, indicating that the extent of oxidation of Si keeps increasing. This result again shows that N_2 plasma treatment is also a better choice than O_2 plasma treatment in lowering the etch resistance of thin crystallized HfO_2 films, because of much less nitridation than oxidation.

The mechanism of the Si recess induced by Ar plasma treatment is hard to investigate using XPS because of the inert chemical nature of Ar. Considering the additional nitridation effect in N_2 plasma treatment process, experimental results in Fig. 3.8 (b) showing that Si recesses induced by Ar and N_2 plasma treatment are similar each other indicate that the physical damage induced by Ar plasma treatment is more than N_2 plasma treatment.

3.3.6 SRIM Monte Carlo simulation of the effects of plasma treatment on HfO_2 and Si

Since plasma treatment using ICP can induce sufficient damage in HfO_2 films to result in highly soluble HfO_2 films in DHF, the solubility of HfO_2 films depends on the depth of ion injection. Experimental results from Fig. 8 (a) shows that the increase of HfO_2 etch depth in DHF using N_2 and O_2 plasma treatment is larger than that using Ar plasma treatment in the energy range of 100 - 400 eV This generally agrees with the 2-D simulation results shown in Figs. 3.16 (a): in HfO_2

films, the injection range of N and O ions is longer than Ar ions with the same ion energy when ion energy is in the energy range of 150 - 400 eV.

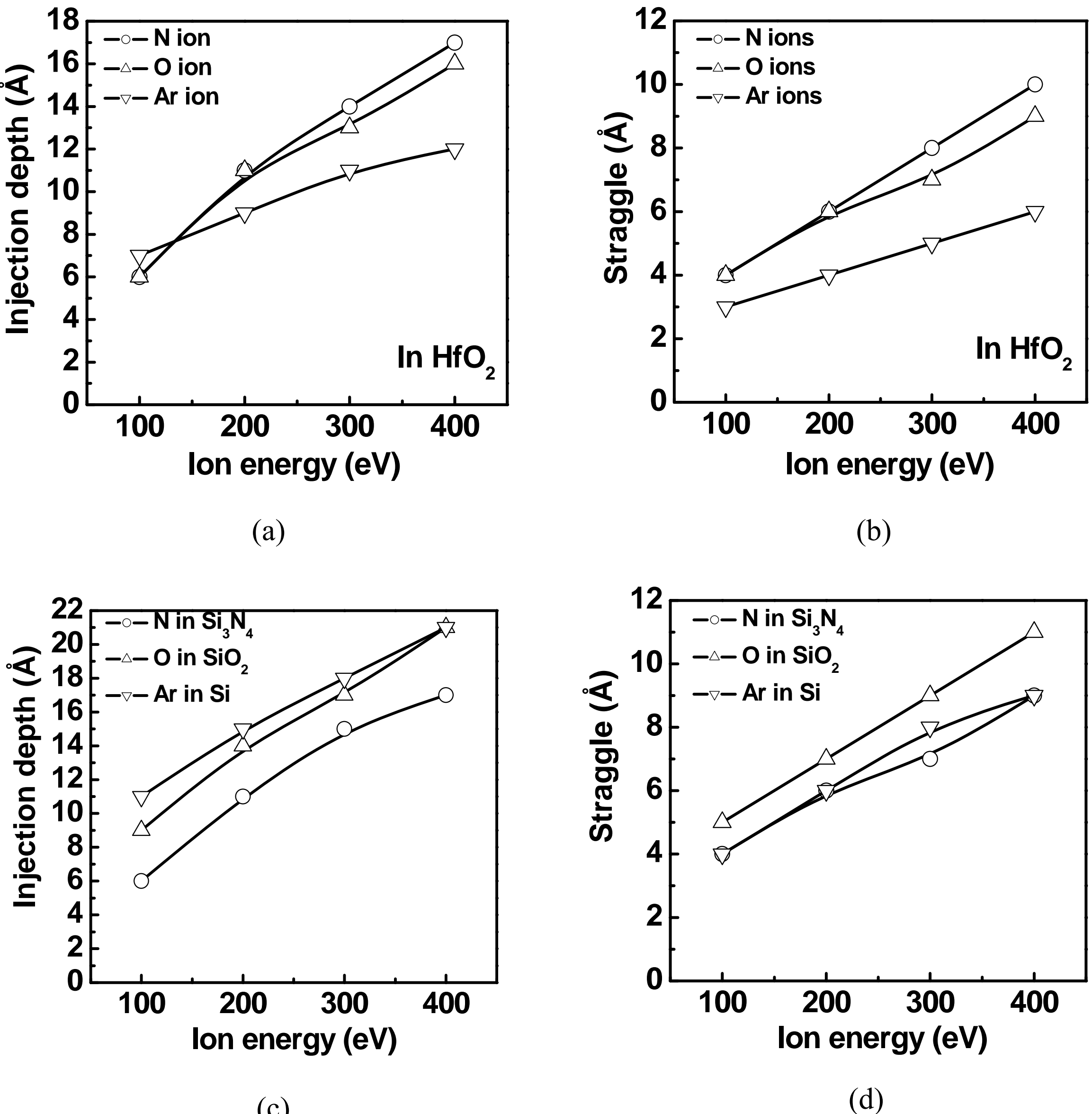


Fig. 3.16 2-D simulation results of (a) injection depth and (b) straggles of N, O and Ar ions with various ion energies in HfO_2, and (c) injection depth and (b) straggles of N, O and Ar with various ion energies in Si_3N_4, SiO_2 and Si substrates, respectively.

Figure 3.16 (b) shows that straggles of N and O ions are also larger than that of Ar ion in this energy range, suggesting another reason why N_2 plasma is more effective to enhance the etch rate of crystallized HfO_2, as shown in Fig. 3.8 (a). An ion number of 5000 was used in all simulations. Injection depth is defined by the peak position of injected ion number and the straggle is defined as $[(\sum_i x_i^2)/N-R_p^2]^{1/2}$, where x_i is the deviation of the injection depth and R_p is the injection depth [18].

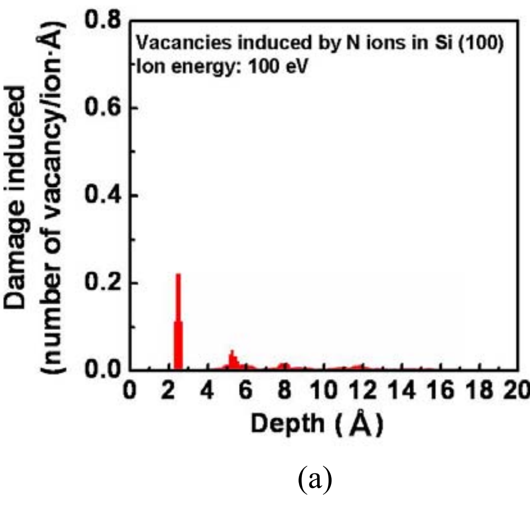
The reason why the injection range and straggle of O and N ions are larger than that of Ar ions could be due to that the masses of N and O ions are smaller than that of Ar ions, hence, when the ion energy is the same, N and O ions can have higher speed and the energy loss in each collision between ions and HfO_2 lattice is smaller.

Since XPS analysis reveals that Si nitrides form during the N_2 plasma treatment and Si oxides form during the O_2 plasma treatment under thin HfO_2 films, the recess on the substrate, either by nitridation or oxidation depends on the injection depth of N and O ions in corresponding Si compounds. In Ar plasma treatment which does not involve chemical reaction with Si, the recess depends on the amount of damage on the substrate. It is, however, hard to evaluate the effect of Ar induced damage on the enhancement of etch rate of Si in HF solutions using simulation because the change of the chemical properties of Si cannot be simulated using SRIM.

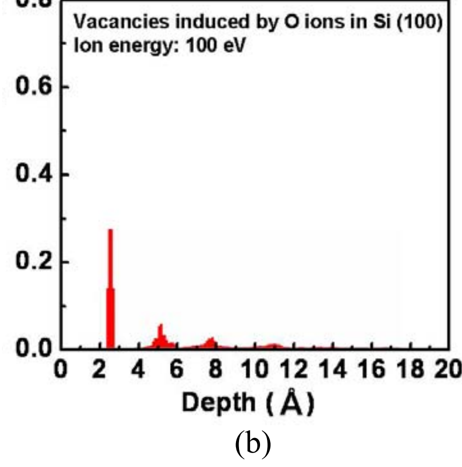
In Figs. 3.16 (c) and (d), the simulation results of injection depth and straggle of N ions in Si_3N_4, O ions in SiO_2 and Ar ion in Si are compared. It can be observed that injection depth and straggle of N ions in Si_3N_4 are the shortest. This can be understood in the way that, although the speed of N ions is higher than O and Ar ions, the density of Si_3N_4 (3.20 kg/m^3) is ~ 1.5 times higher than that of Si (2.33

kg/m^3) or SiO_2 (2.53 kg/m^3) [3.21], thus the effects of energy loss and scattering of N ions can be much faster and more significant in Si_3N_4 than O ion in SiO_2 and Ar in Si. This can explain why the saturation of nitridation with fixed ion energy can easily occur in N_2 plasma treatment process.

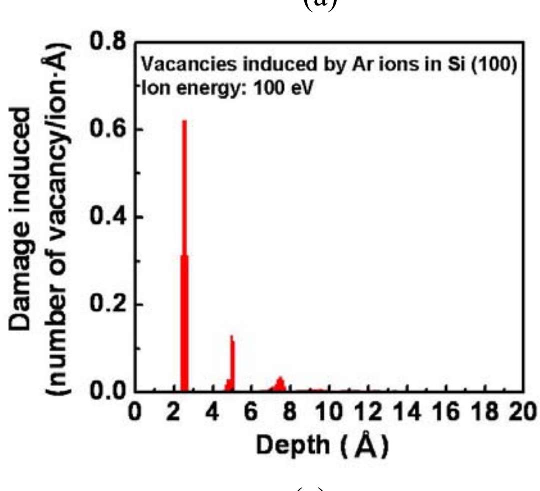
In Fig. 3.17, simulation results of the vacancies produced by N, O and Ar ion with an ion energy of 100 - 400eV are shown. It can be observed that with the same amount of ions, the density of vacancies induced by Ar ions is much higher than that by N and O ions. This result can help us to understand why Ar ions can enhance the etch rate of Si in HF solutions to a similar extent to that of N ions despite no chemical reaction with Si.



(a)



(b)



(c)

Fig. 3.17 2-D simulation of vacancies produced by (a) N, (b) O and (c) Ar ions with an energy of 100 eV in Si substrate. An ion number of 5000 was used.

3.4 Conclusions

It was found that plasma treatment using N_2 or Ar plasma with ion energy of several hundred eV can lower the wet etch resistance of crystallized HfO_2 films via the generation of Hf-N bonds, metallic HfO_x and amorphous HfO_2. However, thermal nitridation or plasma nitridation without bias power cannot introduce sufficient nitrogen to the crystallized HfO_2 films to enhance the wet rate significantly.

Effects of plasma treatment using Ar, N_2 and O_2 to enhance wet removal rate of crystallized HfO_2, SiO_2 and Si were studied using the XPS analysis and the Monte-Carlo simulation on ion injection. The mechanism responsible for the enhancement of etch rate of crystallized HfO_2 using Ar plasma treatment was the formation of HF dissoluble species including metallic HfO_x and amorphous HfO_2; that using N_2 plasma treatment was the formation of HF dissoluble species including metallic HfO_x, amorphous HfO_2 and Hf-N bonds, whereas the mechanism using O_2 plasma treatment was the formation of HF dissoluble species including metallic HfO_x, amorphous HfO_2 and disturbed crystallized HfO_2 resulted from the oxidation of Si substrate.

Among the plasmas studied in this work, N_2 plasma treatment was the most effective to enhance the etch rate of crystallized HfO_2 in HF solution and to minimize recess in the substrate structure because of (1) the largest injection depth in HfO_2, (2) the formation of highly HF dissoluble Hf-N bonds, and (3) the small injection depth of N ions in Si nitrides formed by N_2 plasma treatment. It was found that O_2 plasma treatment can induce a large recess on the Si substrate due to the oxidation effect.

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Chapter 4

Investigation of Etching Properties of Hf Based High-K dielectrics Using Inductively Coupled Plasmas

4.1 Introduction

In chapter 1 of this thesis, we have introduced that to achieve higher and higher speed and density of complementary metal-oxide-semiconductor (CMOS) devices, the physical thickness of silicon oxynitride (SiON) gate dielectric is being scaled down to the sub nanometer regime [4.1, 4.2]. When the thickness of SiON or SiO_2 is less than 15Å, those dielectrics cannot meet the requirements of CMOS devices beyond 45 nm technology node, due to the high gate leakage current [4.1-4.4]. This necessitates the introduction of high-K gate dielectrics [4.1, 4.2]. The comparison of the properties of high-K dielectrics with regards to the requirements and performance of Si devices has shown that hafnium (Hf) based dielectric films such as Hf aluminum dioxide (HfO_2), Hf aluminum oxide (HfAlO), Hf oxynitride (HfON), Hf silicate (HfSiO) and nitrided Hf silicate (HfSiON), are the most promising candidates for future CMOS applications [4.1, 4.5-4.9]. Many reports have shown that adding Al, Si, or N can improve the thermal stability of HfO_2 significantly [4.6-9]. Moreover, various aspects of the performances of CMOS devices such as lower gate leakage current [4.6, 4.7], enhancement of carrier

mobility in the channel [4.9] and reduction of boron penetration [4.7] can be achieved by incorporating those elements into HfO_2. The Hf based dielectrics are also being considered for application in dynamic random access memory (DRAM) capacitors and metal-insulator-metal (MIM) capacitors of RF and mixed signal IC applications [4.10, 4.11].

For successful integration of the Hf based gate dielectrics to conventional VLSI process flow, there are critical process challenges to overcome, *e.g.* plasma etching process [4.12]. In the current front-end process, gate stack etching recipes have been elaborately designed based on the polycrystalline silicon (poly-Si) and silicon oxynitride (SiON) stack. However, the data available for the etching of Hf based dielectrics is very limited. Recently, inductively coupled plasma (ICP) etching of HfO_2 deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD) as a gate dielectric was studied [4.13, 4.14]. Results show that HfO_2 can be etched by various plasmas. For example, etch rates of HfO_2 strongly depend on ion energy as well as ion density, and in HBr plasma, selectivity of poly-Si over HfO_2 can be controlled by pressure, rf bias power and the amount of O_2 [4.14]. However, the etch mechanisms of the other Hf based dielectrics are unclear, and they need to be studied for further process integration.

Hf is a transition metal, and its compounds are usually complex due to the various chemical states, as indicated by various products generated during the plasma etching process [4.15, 4.16]. The etch residues of Hf based dielectrics may not be volatile in the low temperature etching environment due to the high vapor points of Hf compounds [4.16-4.18]. The current etching process of gate stacks involving poly-Si, WSi, and bottom anti-reflection coating (BARC) layer is mostly conducted at relatively low temperature in the range of 20-70^oC using HBr, Cl_2, O_2,

C_xF_y, SF_6, NF_3. Table 4.1 summarizes the melting and boiling points of the main etch by-products of Si, Al, and Hf at atmospheric pressure [4.15, 4.16].

Table 4.1. Melting and boiling points of etch by-products at 1 atm.

Etch by-products	Melting point (^oC)	Boiling point (^oC)
$SiCl_4$	-69	58
$SiBr_4$	5.4	154
SiF_4	-90	-86
$HfCl_4$	319	432
$HfBr_4$	425	420
HfF_4	970	-
$AlCl_3$	192.6	180
$AlBr_3$	97.5	255
AlF_3	1290	1275

This data indicates that the possibility of having non-volatile residues in the etching of Hf based dielectrics is much higher than that in the etching of SiO based dielectrics. Of course, when the pressure is reduced, the vapor points of Hf compounds will decrease [4.17]. For example, the vapor point of $HfCl_4$ is around 140^oC at 100mTorr and it decreases to 100^oC at 5mTorr. Britten *et al.* reported a significant amount of residues formed on the sidewalls after etching HfO_2 using $CHF_3/Ar/O_2$ plasmas [4.18], and they reported that the residues are sputtered fluorinated Hf compounds, as shown in Fig. 4.1.

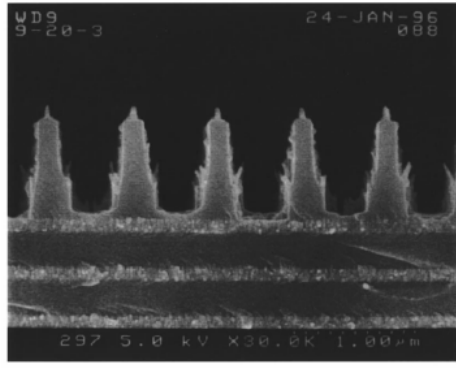


Fig. 4. 1 SEM image of a multilayer dielectric grating with 0.67 μm pitch grating etched by RIE through 750 nm of evaporated SiO_2 to a HfO_2 etch-stop layer. Note the growth of columnar structures on the sidewall and top are believed to be sputtered fluorinated Hf compounds [Ref. 4.18]

In this chapter, we study the properties of etch by-products to understand the etch mechanism and to develop the etching process applicable to devices using Hf based high-K dielectrics. In the work introduced in this chapter, ICP etching of various Hf based high-K dielectrics will be studied using different plasma chemistries. Plasmas of HBr, Cl_2 and their respective mixtures with small amount of O_2 are investigated for etching of high-K films due to their universality in current gate etching technologies. To investigate the etch residues of the Hf based dielectrics generated by HBr/Cl_2/CHF_3/CF_4 plasmas, analysis on the dielectrics was performed using x-ray photoelectron spectroscopy (XPS) and time-of-fight secondary ion mass spectroscopy (TOF-SIMS).

4.2 Experimental Setup

All the films used were deposited on 6-inch Si (100) wafers. The Hf based dielectric films used in this chapter include HfO_2, HfAlO deposited by CVD (hereafter CVD HfO_2, CVD HfAlO), and HfO_2, HfON, HfSiO deposited by PVD (hereafter PVD HfO_2, PVD HfON, PVD HfSiO). CVD HfO_2 was prepared using the same equipment and recipes as our previous work [4.14]. CVD HfAlO was deposited at 420ºC using a single cocktail precursor $HfAl(MMP)_2(OiPr)_5$ (MMP: $OC(CH_3)_2CH_2OCH_3$, OiPr: isopropoxide) which was carried by Ar in the same CVD module used for depositing HfO_2. After deposition, annealing at 700°C for 1 min in N_2 ambient was performed to remove the impurities such as unreacted organic compounds. PVD HfON, PVD HfSiO and PVD HfO_2 were prepared by reactive sputtering at room temperature using either single Hf target or both Hf and Si targets. The thickness of the high-K films deposited by CVD is around 400Å, and that by

PVD is above 2000Å. The atomic or molecular ratio of the added elements was estimated by XPS. The molecular ratio of Al_2O_3 to HfO_2 in HfAlO was 1:10 and the atomic ratio of Si to Hf in HfSiO was 6:7. The amount of N in HfON was found to be around 10%, after light sputtering for removing organic contaminants.

All the samples were etched by two ICP modules, TCP 9400SE (ICP1) manufactured by Lam Research Co. and another module (ICP2). The configuration and difference between these two modules were elaborated in our previous work [4.14]. As the limitation of the gases available in each etcher, the etching using $HBr/Cl_2/O_2/CHF_3$ plasmas was performed using ICP1 and etching by CF_4 plasma was performed using ICP2. All etch rates were determined by measuring the etching time and the thickness of the film removed. Photoresist was removed after etching by acetone in an ultrasonic cleaner. The thickness of the film removed by etching was determined by a surface profiler with a resolution of 5Å.

To understand the properties of etch by-products, various Hf based dielectric surfaces etched by HBr, Cl_2 and CF_4 were analyzed by *ex-situ* XPS. For XPS analysis, monochromatized Al-α x-ray was used. The x-ray source is perpendicular to the surface of the sample. The electron analyzer is installed 45° to the incident x-ray and the energy coordinate was calibrated by the C1s peak. The detection limit of the XPS used is in the order of one part per million. Before the analysis, a light Ar ion sputtering was conducted to remove surface contaminants. To study the effect of temperature on the residues, the XPS analysis was also performed for the HfO_2 samples etched by HBr, Cl_2, CF_4 and CHF_3, after a post heating treatment at 250^oC for 10 min in a vacuum chamber purged by N_2. The analysis of the XPS results is based on the cited references [4.19, 4.20].

The Hf based dielectric samples were also analyzed by TOF-SIMS to

determine the chemical composition of the residues. In TOF-SIMS, Ga ions were used to bombard surfaces, and the chemical composition of the sputtered particles was determined by the mass to charge ratio. Except aluminum fluorides, the chemical composition of all the other particles was confirmed by the isotope spectra of Hf, Br or Cl. As both Al and F have no isotopes, a light ion bombardment prior to the TOF-SIMS analysis was conducted until no carbon was detected. This process ensured complete removal of organic contaminants with the same mass to charge ratio as aluminum fluorides, *e.g.* AlF^+ or AlF_2^+. The detection limit of our TOF-SIMS is in the order of one part per billion. Considering the possibilities of the change of chemical compositions of the residues induced by the exposal to the air, the samples for analysis of XPS and TOF-SIMS were kept in vacuum or N_2 ambient in the transportation.

In ICP1, all residue analysis was done for the etch processes with fixed parameters of 400W of inductive power, 150W of bias power, 10mTorr of pressure and 30sec of etching time. Because of the difference of the chambers and inductive coils between ICP1 and ICP2, it is hard to make the exactly same plasma conditions between the two etchers. Since the volumes of two chambers are similar, when the pressure, gas flux and inductive power are same, it can be estimated that the plasma densities in two chambers are similar. Hence, for comparing the etch residues using CF_4 with other plasma chemistries, in ICP2, other ICP parameters engaged are same with the ones in ICP1. The highest temperature of the wafer surface was determined by the colorific thermal dots mounted on the surface of the samples.

4.3 Experimental Results

4.3.1 Etch rates of Hf based dielectrics

Figures 1 and 2 show the etch rates of CVD HfO_2, PVD HfO_2, CVD HfAlO, PVD HfON and PVD HfSiO obtained by varying the rf bias power in HBr plasma and Cl_2 plasma and their respective mixture.

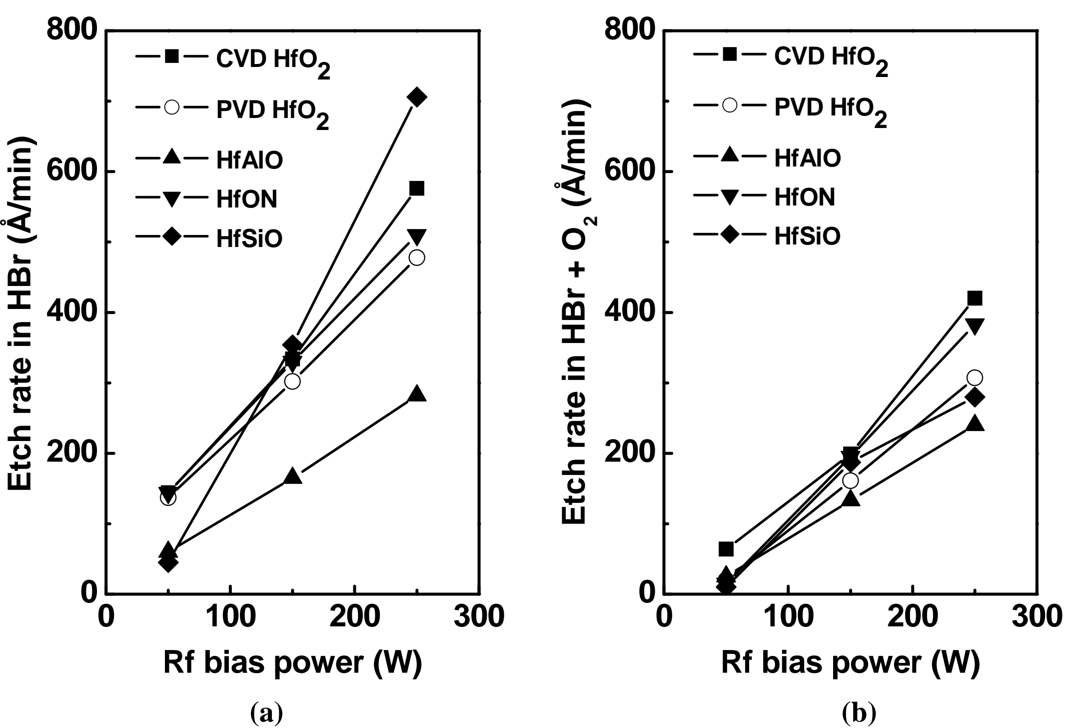


Fig. 4.2 The etch rates of Hf based dielectrics as a function of rf bias power (a) in HBr plasma and (b) in HBr/O_2 plasma (Parameters are fixed otherwise at inductive power of 400W, pressure of 10mTorr, HBr flow of 200sccm, and O_2 flow of 4sccm).

From Figs. 4.2 (a) and (b), the etch rates of all the Hf based dielectrics increase almost linearly with increasing rf bias power in HBr or HBr/O_2 mixture, and their etch rates drop after adding 4sccm of O_2 to 200sccm HBr. In pure HBr plasma, the etch rates of PVD HfSiO show the strongest dependence on rf bias

power. When the rf bias power is larger than 150W, the etch rates of the films in decreasing order is PVD HfSiO > CVD HfO_2 > PVD HfON > PVD HfO_2 > CVD HfAlO. At lower rf bias power, the etch rate of PVD HfSiO drops rapidly. When rf bias power is reduced to 50W, the etch rate of PVD HfSiO is even lower than that of CVD HfAlO. Upon the addition of O_2 to HBr, the etch rates of PVD HfO_2 and PVD HfON drop by half on average of bias powers, and CVD HfAlO, CVD HfO_2 and HfSiO drop by 31%, 41% and 62% on average for different bias powers respectively; on the other hand, the dependence of etch rates of all the other high-K films on the rf bias power remain unchanged, except the etch rate of PVD HfSiO which shows a weaker dependence on rf bias power. Adding O_2 to HBr tends to be more effective in reducing the etch rate of PVD HfSiO than the other films. With the addition of O_2, the etch rates of the films in decreasing order is CVD HfO_2 > PVD HfON > PVD HfO_2 > PVD HfSiO > CVD HfAlO. Generally, the etch rate of CVD HfO_2 is higher than that of PVD HfO_2.

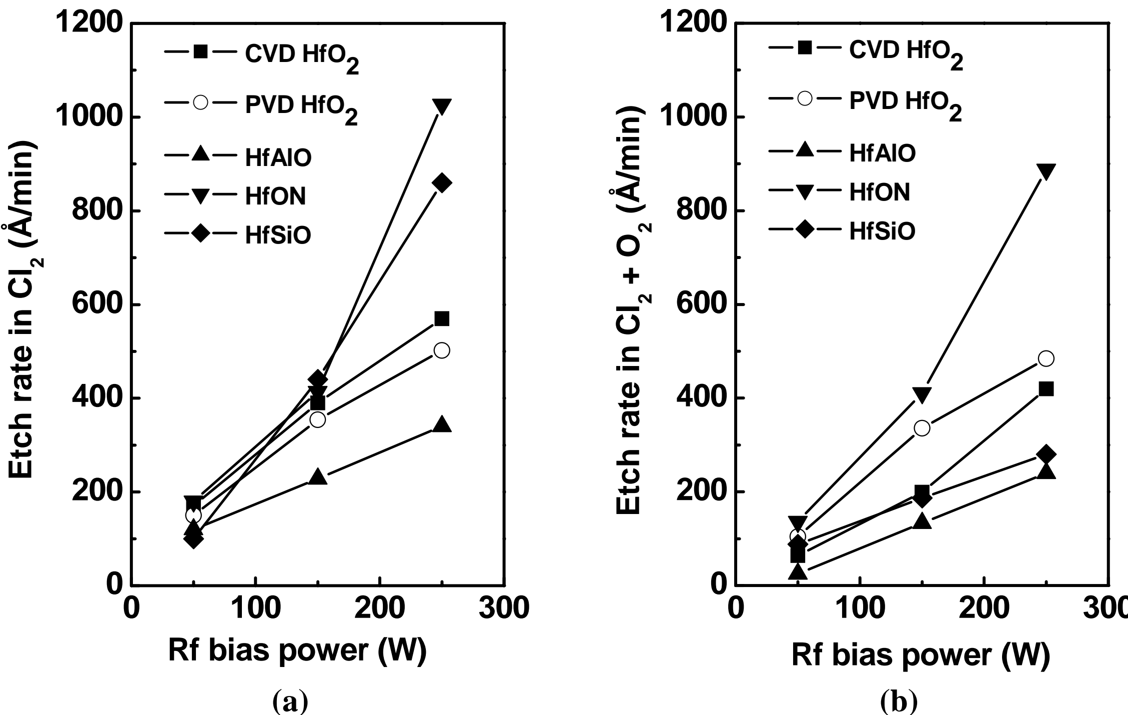
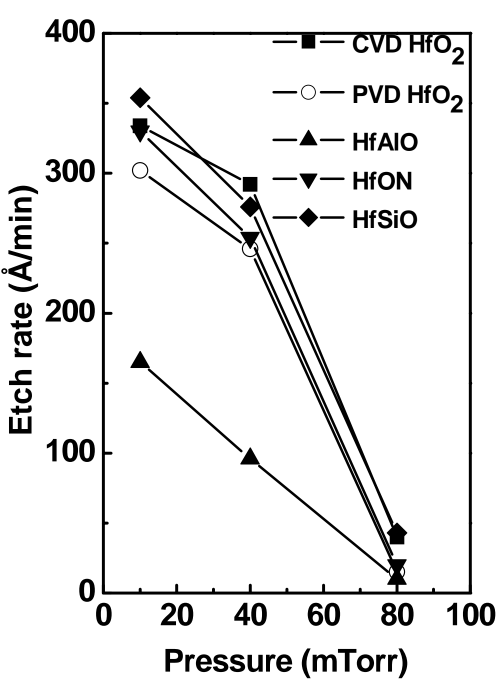


Fig. 4.3 The etch rates of Hf based dielectrics as a function of rf bias power (a) in Cl_2 plasma and (b) in Cl_2/O_2 plasma (Parameters are fixed otherwise at inductive power of 400W, pressure of 10mTorr, Cl_2 flow of 200sccm, and O_2 flow of 4sccm).

From Figs. 4.3 (a) and (b) obtained from Cl_2 and Cl_2/O_2, the etch rates of all the films increase with increasing rf bias power, and their etch rates decrease after adding 4 sccm of O_2 into 200sccm Cl_2, similar to Figs 4.2 (a) and (b) of HBr and HBr/O_2. The etch rates in Cl_2 and Cl_2/O_2 are faster than the ones in HBr and HBr/O_2, respectively. In Cl_2 plasma of Fig. 4.3 (a), when the rf bias power is larger than 150W, the order of etch rates is PVD HfON > PVD HfSiO > CVD HfO_2 > PVD HfO_2 > CVD HfAlO. But in Cl_2/O_2 plasma of Fig. 4.3 (b), the order of etch rates changes to PVD HfON > PVD HfO_2 > CVD HfO_2 > PVD HfSiO > CVD HfAlO. Upon the addition of O_2 to Cl_2, for different bias powers, the etch rates of CVD HfO_2, CVD HfAlO and PVD HfSiO drop by half on average, and PVD HfO_2 and PVD HfON drop by 18% and 13% respectively.

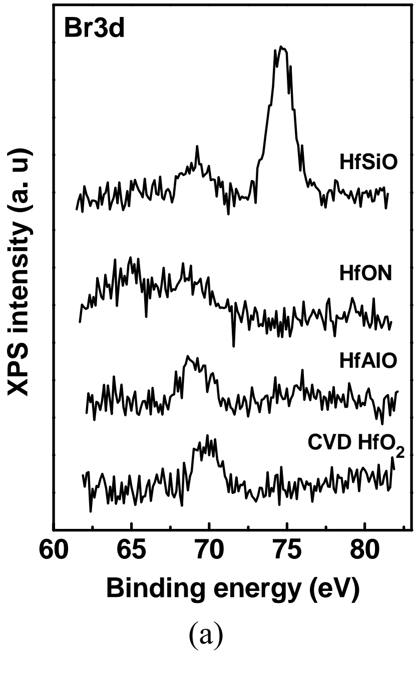
In Fig. 4.4, the etch rates of the Hf based high-K materials are shown as a function of pressure from the HBr plasma. It can be found that the etch rates decrease rapidly with increasing pressure. However, when 4sccm of O_2 is added to 200sccm HBr at 80mTorr, the etch rates are very low within an error range of thickness measurement.

Fig. 4. 4 Etch rates of Hf based dielectrics as a function of pressure (Parameters are fixed otherwise at inductive power of 400W, rf bias power of 150W, HBr flow of 200sccm).

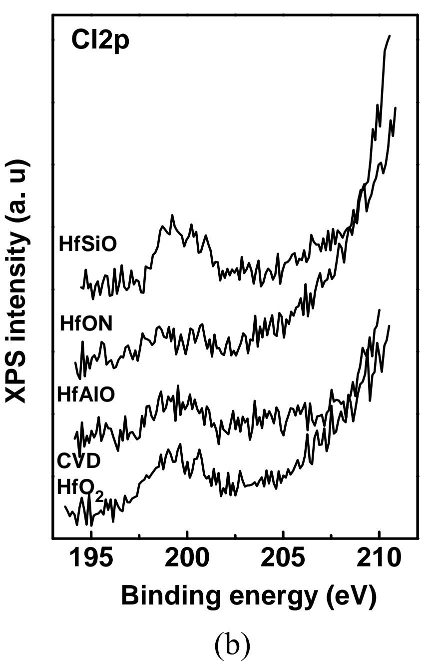


4.3.2 Residue analysis by XPS and TOF-SIMS

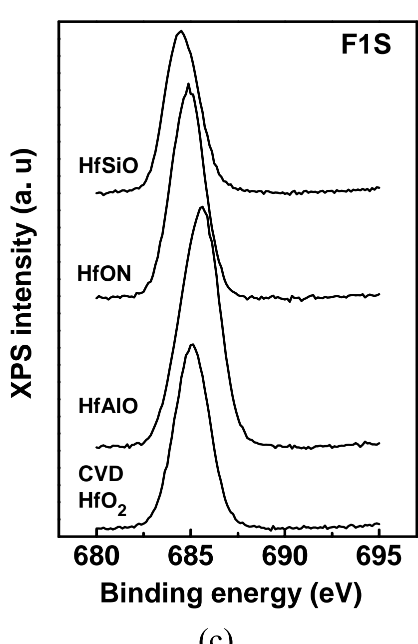
CVD HfO_2, CVD HfAlO, PVD HfON and PVD HfSiO etched by HBr, Cl_2 and CF_4 were analyzed by XPS, as shown in Figs. 4.5 (a)-(c) respectively. The atomic percentages of Cl, Br, and F on the etched surface of the various films are summarized in Table 2. The colorific thermal dot shows that the highest temperature reached by the wafer surface in the etching process is in the range of 100°C to 120°C.



(a)



(b)



(c)

Fig. 4.5 (a) Br*3d* XPS peaks from the Hf based dielectric surface after HBr etching (b) Cl*2p* XPS peaks from the Hf based dielectric surface after Cl_2 etching (c) F*1s* XPS peaks from the Hf based dielectric surface after CF_4 etching

Table 4. 2 Amounts of halogens detected on surfaces by XPS

Samples	**Etchants**	**Atomic % of halogens (Cl, Br or F) detected on etched surfaces**
CVD HfO_2	Cl_2	1.6
HfAlO		1.1
HfON		1.0
HfSiO		2.2
CVD HfO_2	HBr	1.1
HfAlO		1.6
HfON		0
HfSiO		1.7
CVD HfO_2	CF_4	32.1
HfAlO		31.7
HfON		37.8
HfSiO		20.9

Figure 4.5 (a) shows that, various bromides are detected on the surface of the dielectric samples after HBr plasma etching, although they exist in small amounts. The binding energy of Br3d state from 68eV to 72eV was detected on all the surfaces of Hf based dielectrics, indicating that covalent bromine bonds are present (Binding energy of typical Br3d ranges from 68eV to 69eV. [4.20].). A high intensity of binding energy at 75eV for Br3d generated from more electronegative Br is found on the surface of the HfSiO samples, implying that compounds with covalent Br bonds are formed on the surface of HfSiO.

Figure 4.5 (b) shows various chlorides detected on the etched samples. Similar to the HBr etching, the amount of chlorides is very small. Binding energy of Cl2p in chlorides is known to range from 198eV to 210eV [4.20]. In our results, the energy range of Cl2p from 197eV to 202eV is detected with a peak around at 200eV. Typically, binding energy of Cl2p in chlorides with ionic Cl bonds is below 200eV,

and higher binding energy represents chlorides with covalent Cl bonds. Therefore, the chlorides detected on the surface of high-K films are considered to be a mixture of chlorides with ionic and covalent Cl bonds. For binding energy higher than 205eV, it is difficult to identify Cl2p signals as they overlap with strong Hf4d signals from the high-K substrate. In Table 2, only signals from 197eV to 202eV are considered in the calculation of the atomic percentage of Cl.

We notice that the signal of the bromide or chloride based residues on HfON is the weakest among the dielectrics studied in this work. It is likely that the presence of N suppresses the formation of the residues.

Binding energy of F1s detected from the surface is shown in Fig. 4.5 (c). A significant amount of fluorides is detected on the samples etched by CF_4. Typically, binding energy of F1s ranges from 683eV to 689eV, but binding energy of fluorides with ionic F bonds is below 686eV. Higher binding energy is considered to originate from the covalent F bonds. Except from HfAlO, the F1s binding energy from all the other samples is around at 685eV, implying that F is bonded with a metallic element. Binding energy of F1s detected from the HfAlO surface shifts to 686eV.

The Hf4f signal from the HfO_2 surface etched by CF_4 is shown in Fig. 4.6. It is clear that HfO_2 is no longer pure oxide, in that the intensity ratio between the curve-fitted peaks of solid line is reversed from the original peaks and the signal of Hf4f broadens compared with the one from pure HfO_2. After the curve fitting, it can be deduced that HfO_2 and HfO_xF_y were formed with more electropositive Hf in HfO_xF_y as shown from shift of binding energy to the higher energies.

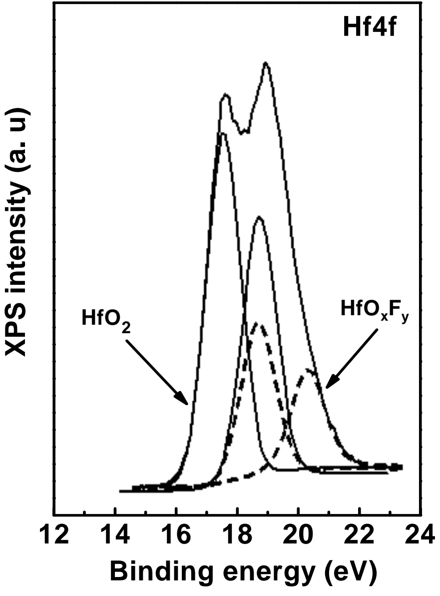
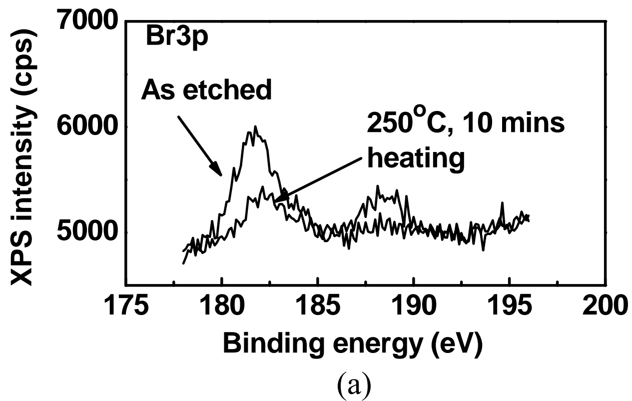
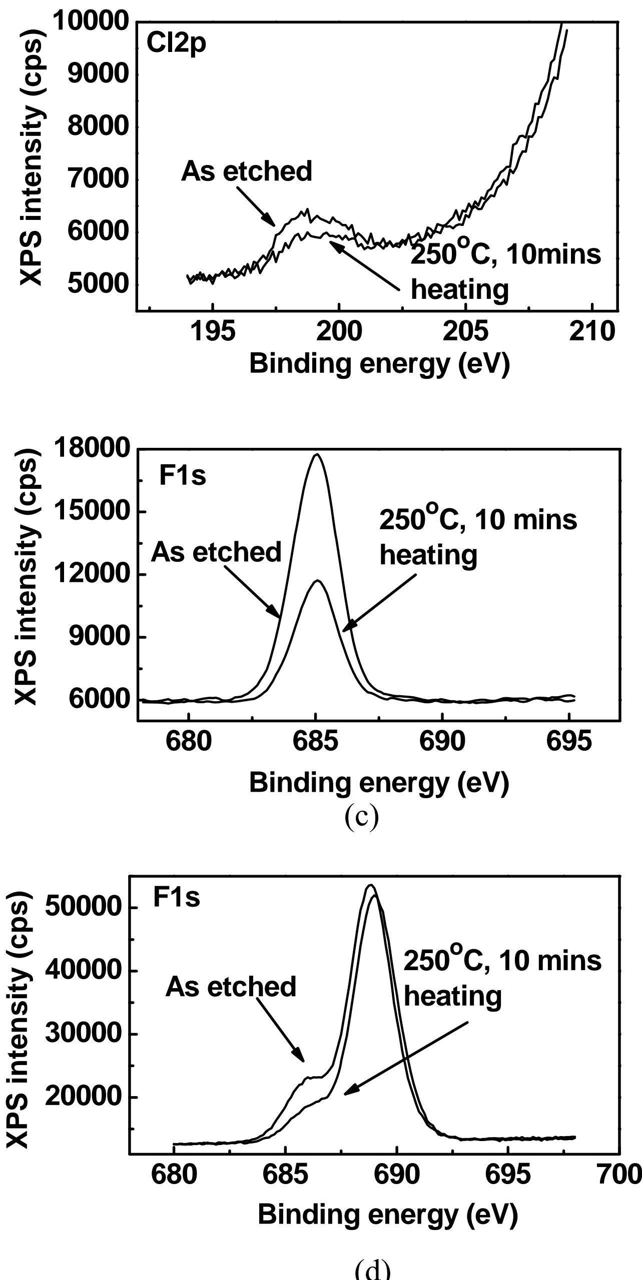


Fig. 4.6 Hf4f XPS peaks from HfO_2 surface after CF_4 etching (Original strong peaks were analyzed as combination of HfO_2 (two peaks of solid line) and HfO_xF_y (two peaks of dotted line))

For CVD HfO_2 films etched by HBr, Cl_2, CF_4 and CHF_3, XPS analysis was performed before and after the thermal treatment at 250°C for 10min in a vacuum environment. The results are shown in Figs. 4.7 (a)-(d). After heating, the signal intensity from Br (Fig. 4.7 (a)), Cl (Fig. 4.7 (b)), and F (Fig. 4.7 (c)) etched by HBr, Cl_2 and CF_4 respectively, decreases about by half. For the HfO_2 surface etched by CHF_3, the XPS analysis results show that fluoride residues are more complex than those by CF_4. Besides 685eV, a high intensity peak at 689eV is detected. It is known that 689eV represents F1s from C-F bonds [4.21]. After heating, signal intensity at 685eV decreases by approximately half, similar to the case of CF_4 etching. Signal intensity at 689eV, however, does not change.



(a)



(d)

Fig. 4. 7 XPS on the surfaces of as-etched HfO_2 samples and the surfaces post heat-treated for 10 minutes in vacuum (10mTorr) (a) Br3p peaks after HBr etching (b) Cl2p peaks after Cl_2 etching (c) F1s peaks after CHF_3 etching (d) F1s peaks after CF_4 etching.

The chemical compositions of the residues are confirmed by TOF-SIMS. The results are summarized in Table 4.3. In TOF-SIMS, precise quantitative analysis cannot be performed, as it requires calibration for all the high-K samples. But the

quantitative trend can be obtained. From the isotope spectra, we found that except for Hf, surface residues on the samples are very different depending on the etching plasmas. From the Br and Cl_2 plasma etching, the amount of bromates, bromides, chlorates or chlorides is very small, and the amount of inorganic bromides or chlorides such as Hf bromides, Hf chlorides, Al bromides and Al chlorides is even smaller. After the CF_4 plasma etching, the particle count from Hf fluorides and oxyfluorides is about 10 times higher than that of residues after the Cl_2 and HBr etching. In the case of CHF_3 plasma etching of HfO_2, a large amount of carbon containing residues was detected from the surface and it was much more than the amount of Hf fluorides.

Table 4. 3 Surface residues detected by TOF-SIMS from Hf based dielectric films etched using HBr, Cl_2, CF_4 and CHF_3.

Films	Etchants	Particles detected from surfaces	Particles detected uniquely from a film
CVD HfO_2	Cl_2	Hf^+, HfO^+, HfO_3H^-, HfO_2H^+, $HfO_2H_2^+$, $HfCl^+$, ClO^-, Cl^- and $ClOH^-$	-
HfAlO			$AlCl^+$
HfON			-
HfSiO			$SiClO_2^-$
CVD HfO_2	HBr	Hf^+, HfO^+, $HfBr^-$, HfO_3H^-, BrO^-, Br^- and $BrOH^-$	-
HfAlO			$AlBr^+$
HfON			-
HfSiO			$SiBrO_2^-$
CVD HfO_2	CF_4	Hf^+, HfO^+, HfF^+, HfF_2^+, $HfFOH^+$, $HfO_2H_3^+$, $HfOH^+$ and HfO_2H^+	-
HfAlO			AlF^+ and AlF_2^+
HfON			-
HfSiO			-
CVD HfO_2	CHF_3	Hf^+, HfO^+, HfO_3H^-, HfF^+, HfF_2^+, $HfFOH^+$, CF^-, $C_3F_3^-$, $C_5F_3^-$ and $C_3F_5^-$	-

4.4 Discussion

4.4.1 Effects of added components and deposition methods on etch rates

1. HfON, HfAlO, and HfO_2

In Fig. 4.2, the etch rates of PVD HfON is higher than those of PVD HfO_2 in both Cl_2 and HBr plasmas. This is especially so in the Cl_2 plasma at high rf bias power. The only difference in the deposition between PVD HfO_2 and PVD HfON is that, the Hf target was sputtered in Ar/O_2 for HfO_2 deposition, whereas it was sputtered in $Ar/O_2/N_2$ for HfON deposition. The XPS analysis shows that our HfON film is mainly a mixture of HfO_2 and HfN. According to the etching results of HfN (Hf:N=1:1 determined by XPS) deposited in the same sputtering conditions, the etch rate is very high at 4000Å/min, at inductive power of 400W, rf bias power of 150W, pressure of 10mTorr and Cl_2 gas flow of 200sccm. It is much higher than the etch rate of PVD HfO_2 at 354Å /min or CVD HfO_2 at 390Å /min. It is known that the enthalpy of the Hf-O bond is 801.7kJ/mol, while the enthalpy of the Hf-N bond is 536kJ/mol [4.21]. This means that the Hf-N bonds can be easier to break than the Hf-O bonds during etching. We suggest that the difference in bond enthalpies may be the reason why the etch rate of PVD HfON is higher than that of PVD HfO_2.

CVD HfAlO always has the lowest etch rate among all the Hf based dielectric films tested. According to the XPS analysis on HfAlO before etching, neither existence of Hf-Al bonds nor distortion of both the HfO_2 and Al_2O_3 signals can be observed.. This means that our HfAlO is a mixture of HfO_2 and Al_2O_3, which is the same as the other reports on the properties of the CVD HfAlO or atomic layer

deposited (ALD) HfAlO [4.6, 4.22]. It is well known that it is very difficult to achieve a high etch rate of Al_2O_3 using Cl_2 without BCl_3 [4.23]. Therefore, the low etch rate of HfAlO is explained by the presence of Al_2O_3.

2. HfSiO vs other Hf based dielectrics

The etch rate of HfSiO shows a very strong dependence on rf bias power and the addition of a small amount of O_2 in the plasma. In the XPS analysis of HfSiO films before etching, we observe a Hf4f signal of low binding energy. This indicates that our HfSiO is not a simple mixture of HfO_2 and SiO_2. Rather, it is considered to be a Hf silicate compound. It has been reported that the structure of Hf silicate is very different from other Hf based dielectrics such as HfO_2 or HfAlO where Hf exists as HfO_2. In Hf silicate, Hf, Si and O tend to form a ternary network structure. The development of this structure enhanced after high temperature annealing [4.24-4.26].

The Si etch by-products are more volatile than the Hf etch by-products [4.15, 4.16], and this may also have contributed to high etch rates of HfSiO in the high rf bias power regime. In the TOF-SIMS analysis, Si chlorates and Si bromates are detected from the surface of HfSiO samples etched by Cl_2 and HBr plasmas respectively. Formation of inorganic passivating polymers such as $SiBr_xO_y$ can also be promoted in the presence of Si in the low rf power regime [4.27, 4.28], causing a sharper decrease in the etch rate of HfSiO.

3. CVD HfO_2 vs. PVD HfO_2

It is observed that the etch rates of CVD HfO_2 and PVD HfO_2 are different. Most cases except for Cl_2/O_2, the etch rates of CVD HfO_2 are higher than those of PVD HfO_2. The CVD HfO_2 samples are prepared using MOCVD whereas the PVD HfO_2 samples are prepared using reactive sputtering. In MOCVD of high-K films,

the precursor may dissociate incompletely, and this results in the incorporation of some impurities such as C, H and additional O into the films (A similar phenomenon was reported from CVD of ZrO_2 [4.29].). Even after post-deposition annealing (PDA) has been performed, some impurities can remain in the high-K films. The impurities disturb the film structures and therefore increase etch rates of the films.

4.4.2 Effects of ICP parameters on etch rate

As shown in Figs. 4.2 to 4.4, reducing rf bias power or increasing pressure can reduce the etch rates of all Hf based high-K materials significantly. The strong dependence of the etch rates on ion bombardment is clearly shown. Meanwhile, reoxidation of Hf etch by-products with the addition of O_2 can explain why the etch rates decrease further. The O_2 effect on the etch rates of Hf based dielectrics is similar to that of SiO_2 or SiON [4.30]. This implies that most Hf based high-K films can be a good etch stop layer during highly selective gate stack etching and therefore the conventional SiO based etching recipes can be used without major modification unless metal gates replace poly-Si gates as conducting electrodes.

4.4.3 Analysis of residues and etch by-products

The results from both XPS and SIMS reinforce each other. This enables conclusive deductions on the amount and chemical composition of the etch residues. In Table 4.4, we summarize the volatility and amount of etch by-products of Hf based dielectrics processed in Cl_2, HBr, CF_4, and CHF_3 plasmas. An assumption made in Table 4.4 is that the compounds detected either in XPS or TOF-SIMS analysis are non-volatile. Also, very little residues of $HfCl_4$, $HfBr_4$, $AlCl_3$, $AlBr_3$, $SiCl_4$, $SiBr_4$, $AlCl_3$, $SiCl_4$ and $SiBr_4$ are observed because they are volatile by-

products [4.31-4.33]. The species noted without (*) are considered to be main and volatile by-products, or to be non-main and non-volatile by-products. Meanwhile, the species noted with (*) are considered to be main but non-volatile by-products. Table 4.4 shows that the non-volatile and main by-products are generated from the etching in F containing plasmas.

Table 4.4 Properties of etch by-products of Hf based dielectric films etched by Cl_2, HBr, CF_4 or CHF_3 plasmas. The uncertain species are marked as "U".

Etchants	**Etch by-products**	**Volatile or not at 100°C & 10mTorr**	**Main by-products or not**
Cl_2	$HfCl_4$	Yes	Yes
	HfCl	No	No
	$U(ClO)_x$	No	No
	$AlCl_3$	Yes	Yes
	$AlCl_3$	No	No
	$SiCl_4$	Yes	Yes
	$USiClO_2$	No	No
Br_2	$HfBr_4$	Yes	Yes
	HfBr	No	No
	$U(BrO)_x$	No	No
	$AlBr_3$	Yes	Yes
	AlCl	No	No
	$SiCl_4$	Yes	Yes
	$USiBrO_2$	No	No
CF_4	HfF_x(X=1, 2) (*)	No	Yes
	HfF_xO_y (*)	No	Yes
CHF_3	C_xF_y (*)	No	Yes
	HfF_xO_y (*)	No	Yes
	C_xF_y (*)	No	Yes
From the air or in plasmas	$HfO_2(H_2O)_x$	No	No
	Hf	No	No

The effect of temperature on the residue shown in Figs. 4.7 (a)-(d) reveals that the amount of etch residues decreases by post high temperature process at 250°C. Dissociation of bromates, chlorates and oxyfluorides may result in the

formation of halides which can be volatile at high temperature, and this can explain the reduction in the residues. However, for the CHF_3 etching, the amount of C fluoride residues was not reduced even after heating and this may be attributed to their relatively high thermal stability.

From the viewpoint of process integration, these residues can be deleterious. If the residues are deposited on the sidewall of gates, they can provide an additional current path which will lead to higher gate leakage. If the residues are deposited on the wafer surface, they can hinder the formation of silicides, and this can result in higher contact resistance. Furthermore, these residues can induce the cross contamination of the wafers and process chambers.

4.5 Conclusions

Experimental results show that the etching of HfON, HfAlO, and HfSiO is strongly dependent on etching properties of each phase in the makeup of the films, *e.g.* HfO_2, HfN, Al_2O_3, and $HfSiO_4$. Inductively coupled plasma using $HBr/Cl_2/O_2$ for poly-Si/SiO_2 gate stack etching can also be applied to the etching of poly-Si / Hf based dielectric gate stacks. The incorporation of N, Al, Si into HfO_2 changes surface residues, and the etch rates of the Hf based dielectric films appear to depend on etch properties of each phase in the films. In the low pressure ICP etching of Hf based dielectrics using HBr or Cl_2 plasmas, the amount of non-volatile residues is small, and high temperature post-treatment helps to further reduce the amount of residues. Fluorine containing plasmas are undesirable for etching of Hf based high-K films because of the generation of a significantly larger amount of non-volatile residues, compared to the plasmas containing bromine or chlorine.

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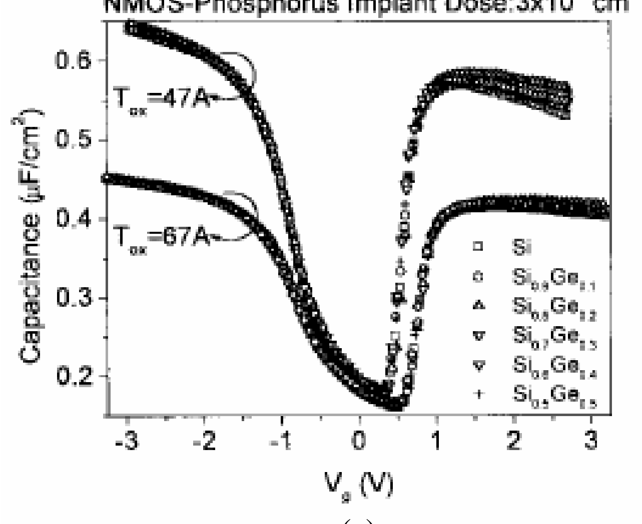
Chapter 5

Formation of Poly-SiGe/HfO_2 Gate Stack Using Inductively Coupled Plasma

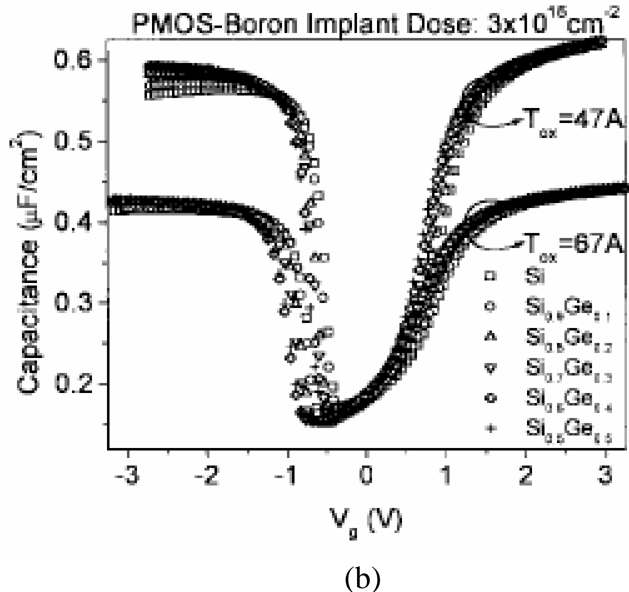
5.1 Introduction

In chapter 1, we have explained that if MOSFETs are kept fabricating on planar bulk Si substrates, it is very likely that not only gate oxide of SiO_2/SiO_xN_y will be replaced by high-K dielectrics, but also poly-Si will be replaced by advanced gate materials nodes [5.1, 5.2].

Polycrystalline silicon germanium (Poly-SiGe) has been is found to have several advantages as a suitable gate conducting material to replace poly-Si. Poly-SiGe gates have been found to be useful in reducing poly depletion effects for both NMOS and PMOS [5.3], as shown in Fig. 5.1. With adjusted Ge concentrations, poly SiGe can provide different work functions suitable for a *p*-channel device [5.4, 5.5].



(a)



(b)

Fig. 5. 1 Comparison of measured quasi-static C-V for (a) NMOS and (b) PMOS with poly-$Si_{1-x}Ge_x$ gate stack [5.3].

At the same time, it has been reported that the interfacial layer between poly-SiGe gate and HfO_2, one the leading high-K gate dielectrics, can be suppressed compared with poly-Si and HfO_2 [5.6], as shown in Fig. 5.2.

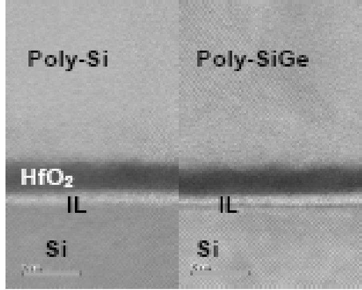


Fig. 5. 2 Cross-sectional TEM images of poly-Si/HfO_2 and poly-SiGe gate stacks after anneal. In poly-SiGe / HfO_2 gate stack, interfacial layers above and under HfO_2 films are thinner than in poly-Si /HfO_2 gate stack [5.6].

Reports have been made regarding the etching of poly-SiGe material using reactive ion etching (RIE) techniques [5.7-5.10]. The common finding in these cases is that the etch rate of poly-SiGe increases with Ge concentration. Oehrlein *et. al.* [5.11] reported that the experimental etch rates were greater than those from their proposed models and gave a thorough discussion to explain this phenomenon. They

reported that the increase in the etch rate could not be accounted for by the greater gasification of Ge atoms alone, but that the presence of Ge atoms in the SiGe alloy increased the rate of the Si etch products formation. Several reasons were proposed. They believed that the availability of electrons at the surface is important in explaining the increased etch rate, and this is similar to the "doping effect" in Si where the etch rate changes with the type and amount of dopants used. Furthermore the surface of SiGe was found to become richer in Ge when using CF_4, while on the other hand, it became richer in Si when using CF_2Cl_2 or HBr. Cheung *et. al.* [5.12] reported that the etch rate and etch profile of $Si_{0.75}Ge_{0.25}$ were strongly influenced by the substrate temperature and the oxygen content in the SF_6/O_2/He gas mixture. There was also a report [5.8] indicating that the difference in the enrichment was highly dependent on ion bombardment, and preferential sputtering was cited as the most plausible mechanism.

Etching of semiconductor materials has moved from the conventional RIE system to a system using a higher plasma density. In a study of etching SiGe in high density plasmas, Vallon *et. al.* [5.13] showed that the recipe previously developed for the etching of Si was unsuitable for etching SiGe, with the etch profile being affected when a helicon source was used. This effect also depended significantly on the Ge concentration in SiGe. A surface study on SiGe using XPS was also performed by them in another work [5.14]. Etching of SiGe using an electron cyclotron resonance (ECR) source [5.8] was also investigated to determine the effect of ion bombardment on surface stoichiometry as mentioned previously. In our work, the dependence of etch profiles and etch rates on process parameters is studied to understand etching mechanisms of poly-SiGe when using an ICP source.

After completing the dry etching process of the poly-SiGe gate conductor, the underlying thin gate dielectric is usually removed by diluted HF, since wet etching of dielectric films using concentrated HF results in significant undercutting. According to recent reports [5.15, 5.16], wet etch rates of high-K films as gate dielectrics are extremely low, particularly after they have been annealed. Exploiting the difficulty for HfO_2 to form volatile products during plasma etching, there have been reports [5.17, 5.18] of using the HfO_2 film as an etch-stop layer. Recently, Norasetthekul *et. al.* [5.19] reported on the etching of HfO_2 films in an ICP etcher using Cl_2 and SF_6.

In this chapter, we report on results obtained from ICP etching of poly-SiGe and HfO_2 with the aim of forming poly-SiGe / HfO_2 gate stacks using industry compatible etching equipment. We also demonstrate the formation of controlled notches from the poly-SiGe sidewall as a step towards the development of short channel devices with a technology node smaller than 65nm and high selectivity plasma etching of poly-SiGe to HfO_2.

5.2 Experimental Setup

The samples used in this work were prepared by a gate cluster system manufactured by Jusung Engineering Co. The system consists of three processing chambers for MOCVD of high-K dielectrics, CVD of poly-SiGe deposition, and post deposition annealing (PDA), respectively. In the gate cluster system, these processing steps are carried out in sequence without breaking the vacuum. All the poly-Si and poly-SiGe films were deposited by CVD using SiH_4 and GeH_4 at a temperature of 550 °C and a pressure of 5 Torr. The SiH_4 flow rate was fixed at 60sccm, but the GeH_4 flow rate was varied from 0 to 200 sccm to obtain various Ge

concentrations in poly-SiGe. The Ge concentrations of poly-SiGe samples used in this study were 15%, 23% 32% and 46 %, and these were determined using Rutherford backscattering spectrometry (RBS). The poly-Si and poly-SiGe films in the thickness range from 500 to 3000 Å were deposited either on SiO_2 thermally grown from an oxidation furnace or on 60 Å thick HfO_2 grown from the MOCVD module of the gate cluster system. The 400 Å thick HfO_2 films were also prepared for the measurement of the etch rates of HfO_2 and the etching selectivities of poly-SiGe over HfO_2. The SiO_2 films were grown on 6-inch Si wafers at a temperature of 1030 ^oC with O_2 at atmospheric pressure. The HfO_2 films were deposited on 6-inch Si wafers using the $Hf(OC(CH_3)_3)_4$ precursor at 400ºC with 50sccm O_2 and 100sccm Ar. The deposition pressure was fixed at 400mTorr. After the deposition, the annealing process was carried out at 700ºC for 1 min in an N_2 ambient.

Thicknesses of blanket films were determined by an ellipsometer. Etch rates and selectivities were determined by measuring the etching times and etched thicknesses. The etched thicknesses of the films patterned by a 0.6µm gate mask were determined by a surface profiler. The etch rates obtained from the patterned films were about the same within the error range. The 0.6um gate patterns were also used for cross sectional SEM observations of poly-SiGe and a test patterns of 0.13µm were used for investigating the etched profile of gate stacks of gate length below 0.1µm by TEM.

All the poly-Si, poly-SiGe and TMNs samples were etched using the ICP etching module (TCP 9400SE manufactured by Lam Research Co.). The wafer is electrostatically clamped to the bottom rf electrode and cooled by He flowing through the grooved electrode. The temperature of the wafer electrode and the chamber wall was maintained at 60 °C. Reactant feed gases were introduced into the

chamber from the bottom. In this study, various gas combinations of $HBr/Cl_2/O_2$ were used for each of the following three etching steps for the gate stack: main-etching of poly-SiGe, over-etching of poly-SiGe, and etching of HfO_2. Studies on the etching of HfO_2 with $HBr/Cl_2/O_2$ plasmas were performed using the TCP9400SE, whereas studies on the HfO_2 etching with CF_4 plasmas were performed using another etcher (ICP2, used in chapter 3). Configuration of TCP9400SE is similar to ICP2. Differences of the TCP9400SE from ICP2 the are as follows: (1) ICP2 holds a wafer using step height on the electrode and gravity of the wafer, whereas TCP9400SE uses electrostatic chuck, and (2) ICP2 has 5.75 coil turns and sidewall gas inlets whereas TCP9400SE has 4 coil turns and bottom gas inlets. To investigate the etching characteristics at various conditions, the parameters of inductive power, rf bias power and pressure were varied. The inductive power was varied in the range from 200 to 550 W, the rf bias power was varied in the range from 0 to 360 W, and the pressure was varied in the range from 10 to 80mTorr.

Optical emission was monitored to investigate the property of the plasma species during the etching of the poly-SiGe / HfO_2 gate stack on the Si substrate. Optical emission spectra in the wavelength range of 200 to 800nm were collected using a CCD spectrograph via an optical fiber fixed on the sidewall of the reactor.

5.3 Experimental Results

5.3.1 ICP etching of poly-SiGe

Figures 5.3 (a), (b) and (c) summarize the etch rates obtained by varying in turn the inductive power, rf bias power and pressure, using the baseline recipe of an inductive power of 550 W, an rf bias power of 200 W, a pressure of 10 mTorr and a HBr flow of 200 sccm.

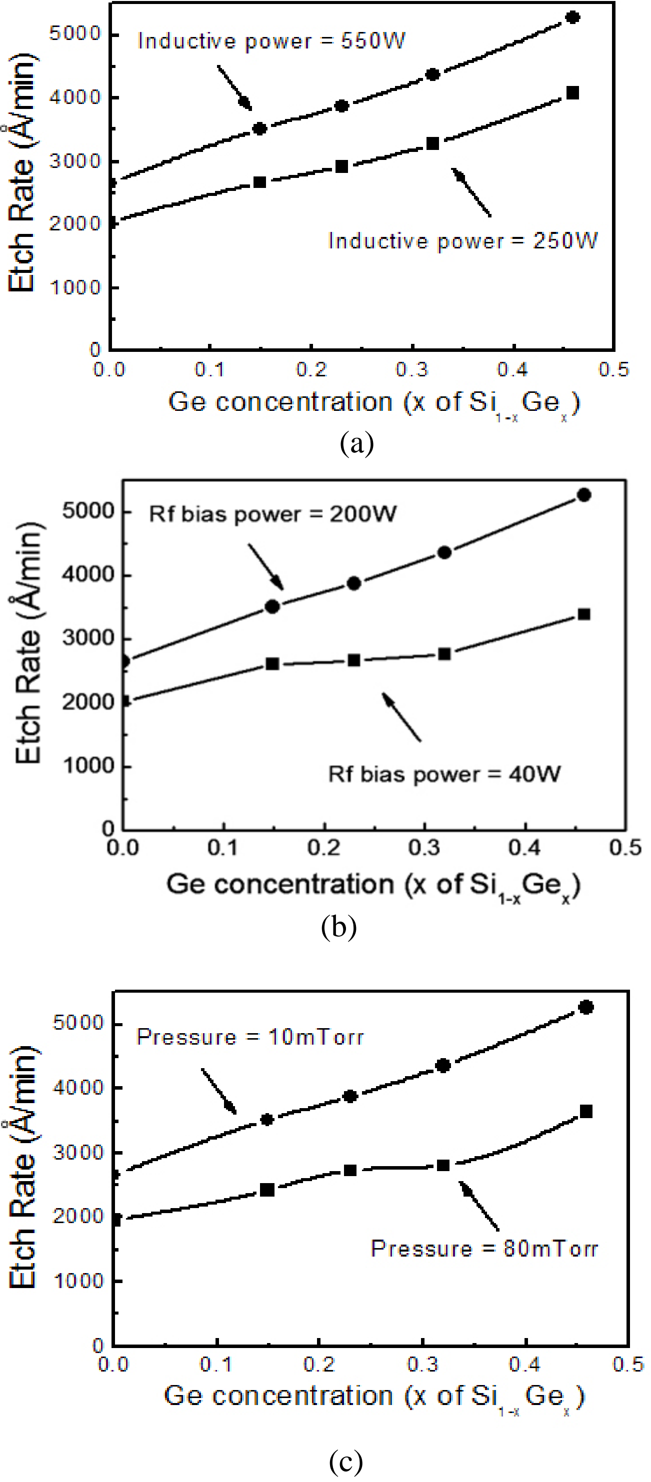


Fig. 5.3 Poly-SiGe etch rates as a function of Ge concentration at the different (a) inductively powers, (b) rf bias powers, and (c) pressures (Parameters are fixed otherwise at inductive power of 550W, rf bias power of 200W, pressure of 10mTorr, and HBr flow of 200sccm.).

From the baseline condition, we obtained the etch rates of 2660 Å/min for poly-Si and 5270 Å/min for Poly-$Si_{0.54}Ge_{0.46}$. From Fig. 5.3, it can be observed that the etch rate of poly-SiGe increases approximately linearly with increasing Ge concentration, although the slight deviation towards the high etch rate was observed at 46% Ge. Models were suggested by Oherlein *et. al.* in RIE [5.10] to explain the deviation from the linear relation, but their experimental results did not quite agree with their models. As shown in Fig 1, the etch rates were affected by changing the following process parameters: 2040 Å/min - 4080 Å/min for the 250W inductive power, 2030 Å/min - 3390 Å/min for the 40 W rf bias power, and 1960 Å/min - 3640 Å/min for the 80mTorr pressure. However, the trend of the linear increase of etching rates with increasing Ge concentration remained unchanged.

Figure 5.4 shows etch rates as a function of pressure from 10 mTorr to 80 mTorr for different Ge concentrations. A peak value for the poly-SiGe etch rates is observed at around 20 mTorr. A similar trend was reported in RIE by Zhang *et. al* [7], but the peak was observed at around 75 mTorr in their work. The trend is more obvious for samples with the larger Ge concentration.

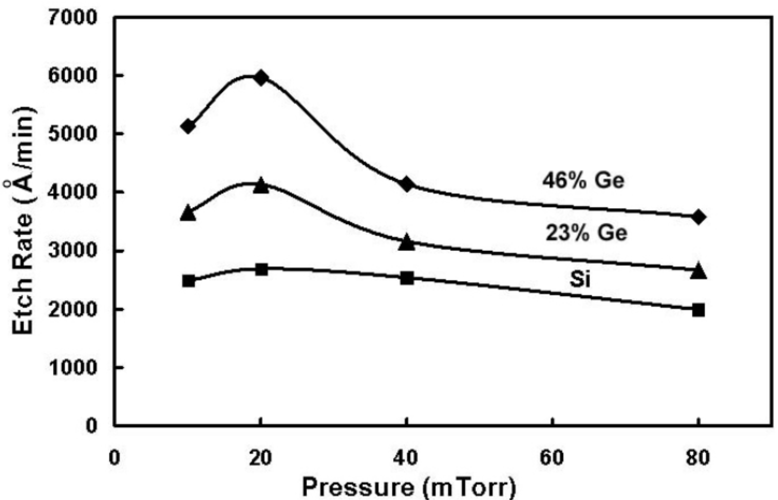


Fig. 5.4 Etch rates of poly-Si, poly-$Si_{0.77}Ge_{0.23}$, and poly-$Si_{0.54}Ge_{0.46}$ as a function of pressure (inductive power: 550W, rf bias power: 200W, and gas flow: HBr 200sccm).

Figures 5.5 (a) and (b) show the etch rates as a function of rf bias power at 10 mTorr and 80 mTorr for poly-SiGe samples for various Ge concentrations. It was found that, as the rf bias power increased, the etch rates increased more rapidly at 80 mTorr than at 10mTorr. The difference between 10 mTorr and 80 mTorr was more pronounced for the higher Ge concentrations.

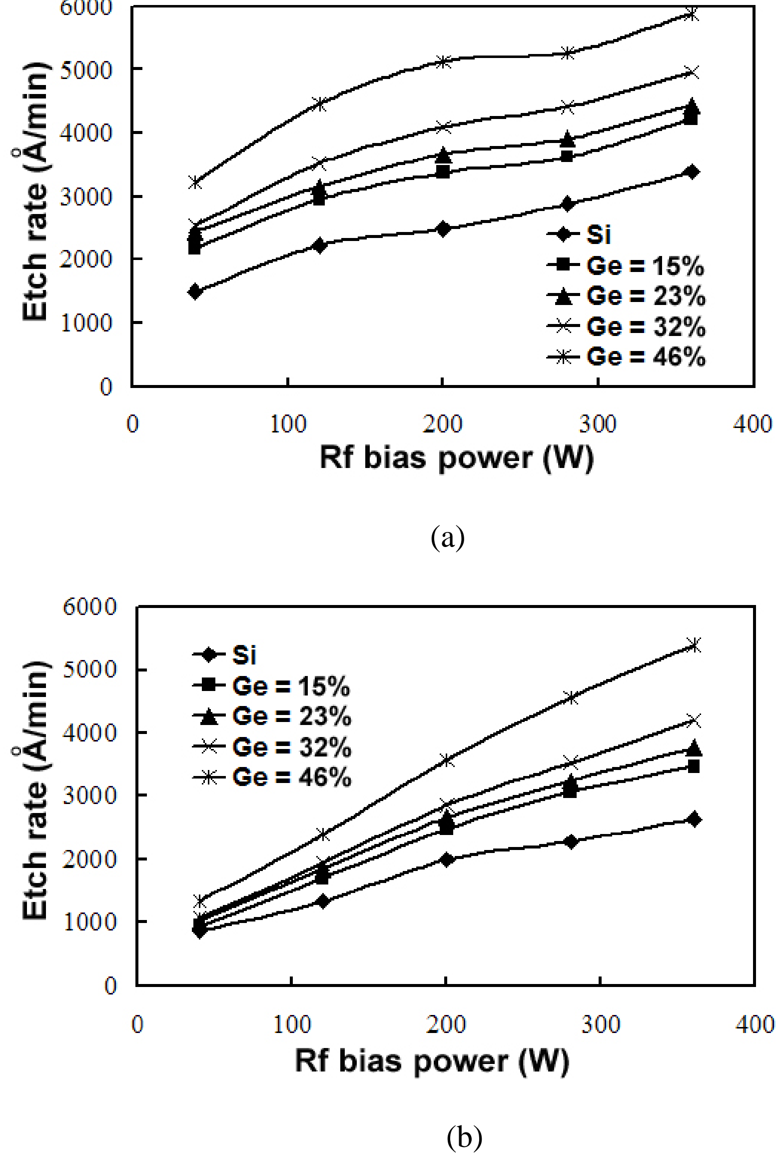
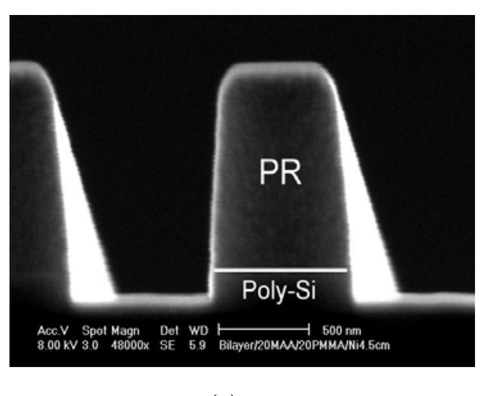


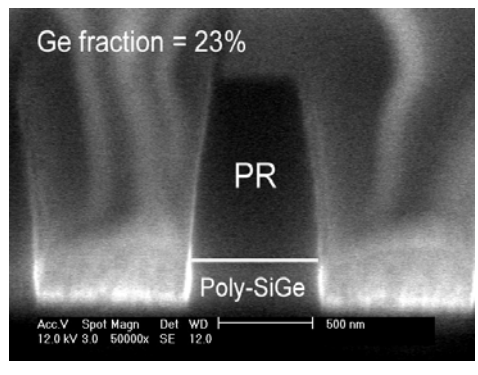
Fig. 5.5 Poly-SiGe etch rates as a function of rf bias power at (a) 10mTorr and (b) 80 mTorr.

Figures 5.6 (a)-(h) show the vertical profiles of the poly-SiGe gates for the

various Ge concentrations and the various process parameters for ICP etching. As shown in Figs. 5.4 (c) and (d), when the Ge concentration was above 30%, notching was observed. Almost no notching was observed in Figs. 5.4 (a) to (c) for the poly-Si gate and the poly-SiGe gates with the Ge concentration below 30%. More notching was visible with increasing Ge concentration (Figs. 5.6(a) to (d)), increasing pressure (Figs. 5.6 (e) and (d)), decreasing rf bias (Figs. 6 (d) to (f)), and increasing inductive power (Figs. 5.6, (g) and (h)).

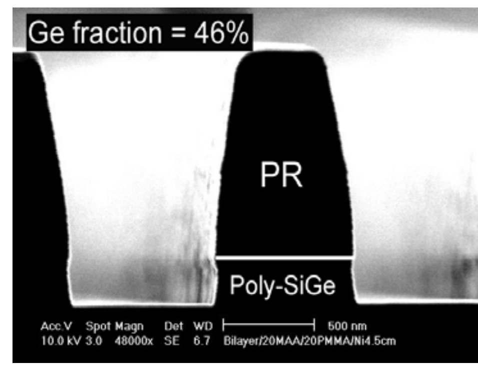


(a)



(b)

(c)



(d)

(e)

(f)

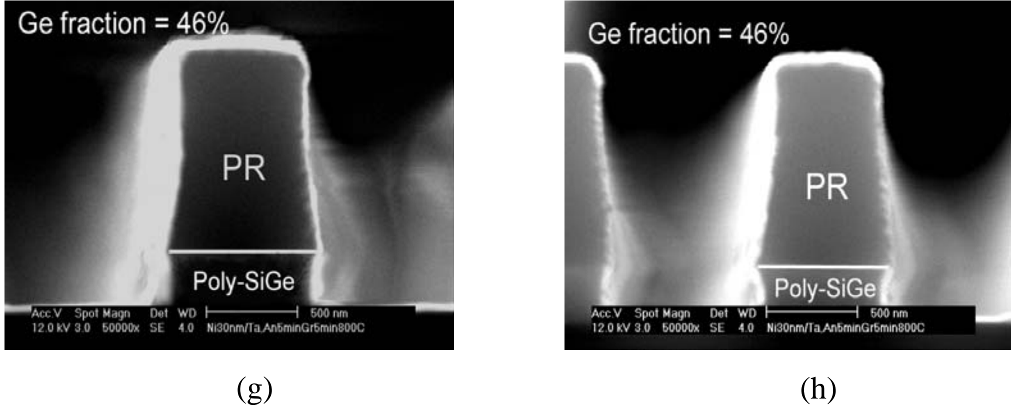


Fig. 5.6 SEM of etching profiles for (a) poly Si, (b) poly $Si_{0.77}Ge_{0.23}$, (c) poly $Si_{0.68}Ge_{0.32}$, (d) poly $Si_{0.54}Ge_{0.46}$, (e) poly $Si_{0.54}Ge_{0.46}$ (pressure: 10mTorr), (f) poly $Si_{0.54}Ge_{0.46}$ (rf bias power: 280 W), (g) poly $Si_{0.54}Ge_{0.46}$ (inductive power: 250 W), and (h) poly $Si_{0.54}Ge_{0.46}$ (inductive power: 550 W). ((a)-(f): parameters are fixed at inductive power of 550 W, rf bias power of 200 W, pressure of 20 mTorr, HBr of 200 sccm, etching time of 30 sec; (g)-(h): parameters are fixed at rf bias power of 200 W, pressure of 80 mTorr, HBr of 200 sccm, and etch time of 150 sec).

Figure 5.7 shows TEM pictures of the double layered poly-Si / poly-SiGe gate stack of the 100nm gate line after etching at a condition identical to those in Fig. 5.6.

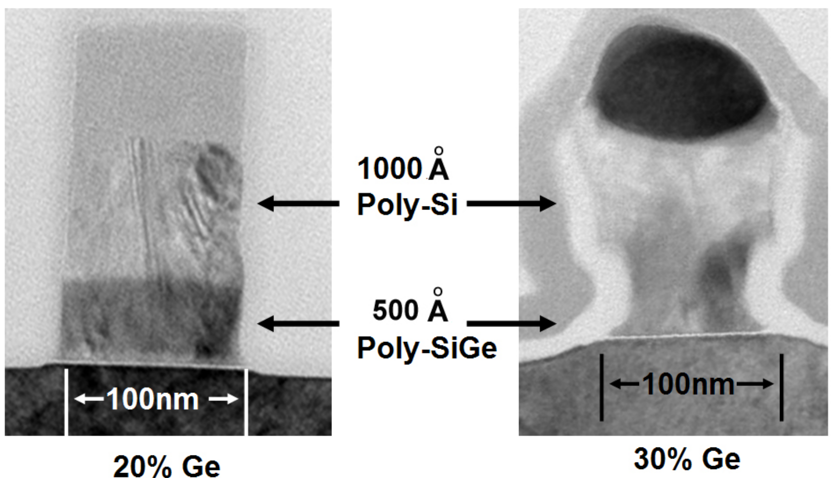


Fig. 5.7 TEM images of etching profiles for gates with a line width of 100 nm with Ge concentrations of 20% and 30%. Thickness is 50nm for poly-SiGe and 100nm for poly-Si.

The notching depth of 50nm was obtained from poly-SiGe of 30% Ge after the etching for the same period as that for the single layered poly-Si. The clear

difference in poly-SiGe gate stack profiles was observed between 20% and 30% Ge.

5.3.2 ICP etching of Poly SiGe/HfO_2 gate stacks

Etching selectivities of poly-SiGe over HfO_2 as a function of rf bias power at 10mTorr and 80mTorr are shown in Figs. 5.8 (a) and 5.8 (b), respectively. At 10mTorr, the etching selectivity decreased as the rf bias power increased (see Fig. 5.8 (a)). This was originated from that the etch rate of HfO_2 increased faster than that of poly-SiGe with increasing the rf bias power. However, the etching selectivities were relatively constant at 80mTorr (see Fig. 5.8 (b)).

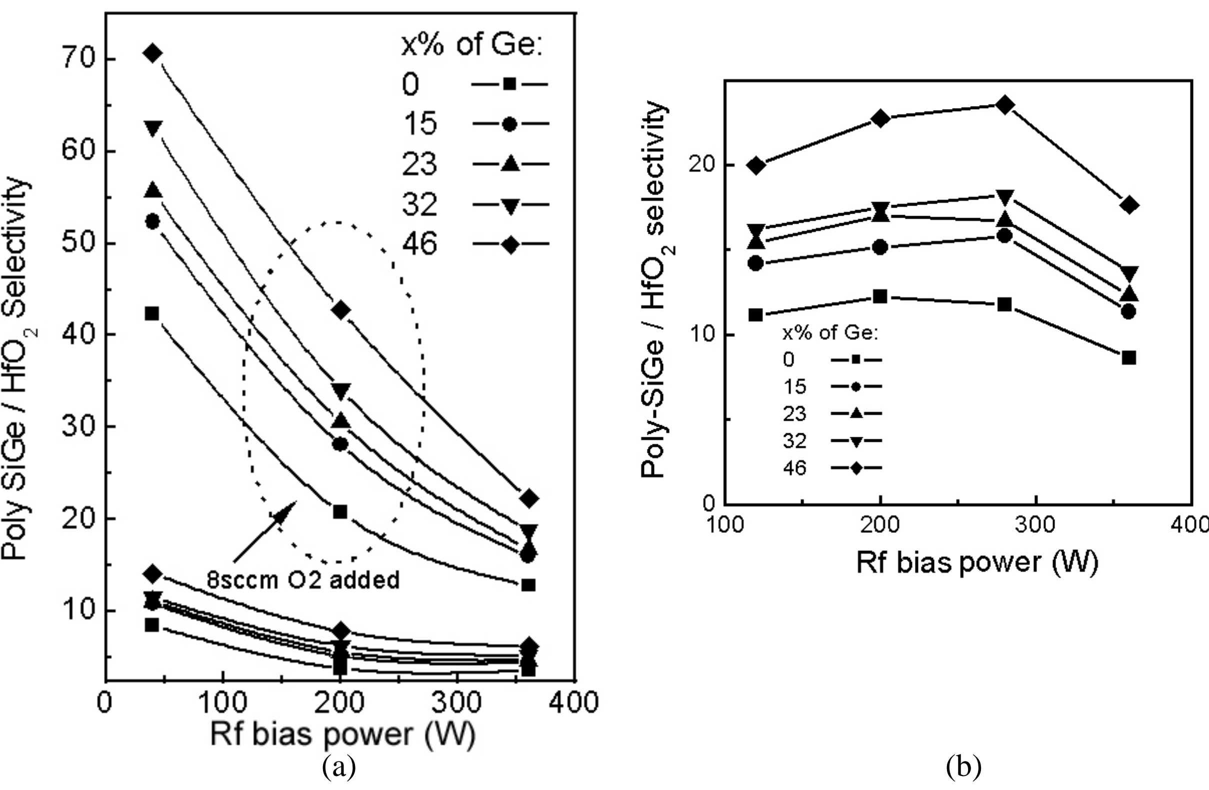


Fig. 5.8 Poly-SiGe / HfO_2 selectivities as a function of rf bias power when pure HBr is used and 8 sccm O_2 is added to HBr at (a) 10 mTorr and (b) 80mTorr.

When 8sccm O_2 was added to 200sccm HBr at 10mTorr, the etching selectivity of poly-SiGe to HfO_2 increased significantly due to the lowered etch rate

of HfO_2 films. When 8sccm O_2 was added at 80 mTorr, at the low bias power the etch rate of HfO_2 films was lowered down to almost 0, and furthermore, at the high bias power a significant amount of etching by-products was deposited to result in net deposition. The occurrence of net deposition was observed by removing the photoresist mask using acetone and by subsequently measuring step heights between masked areas and unmasked areas of HfO_2 films. The net deposition rate was in the range of 0 - 40 Å/min.

Figure 5.9 shows optical emission spectra collected during HBr etching of poly-SiGe. The optical emissions from Si and Ge were detected clearly at the wavelengths of 251.0 nm and 264.5 nm, respectively. We were not able to detect optical emissions generated from Hf etch products, e.g. 307.3 nm, 340.0 nm, 368.2nm, etc [5.20]. Furthermore, the optical emission from the wavelengths of 251nm (Si) and 264.5 nm (Ge) were used to analyze temporal change in the etch products generated during ICP etching of the poly-SiGe / HfO_2 / Si gate stack in the HBr/Cl_2 plasmas.

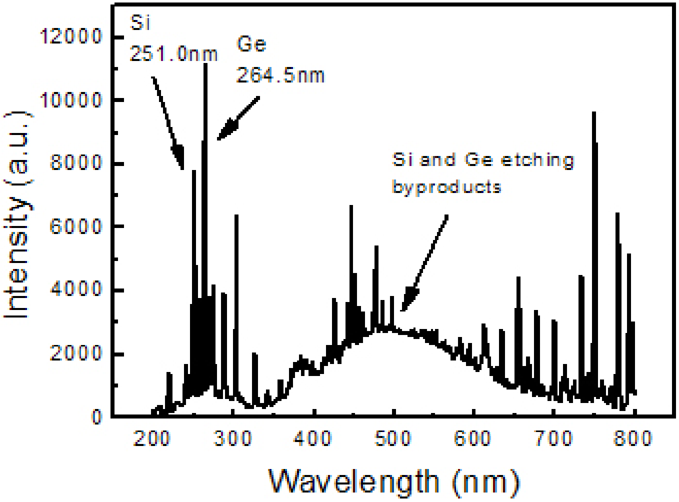
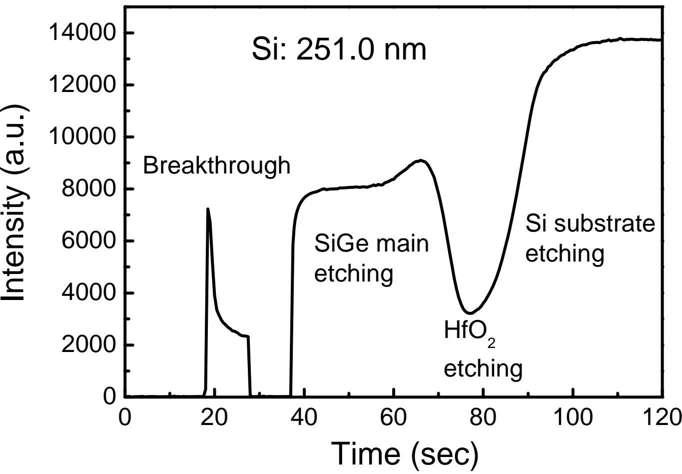
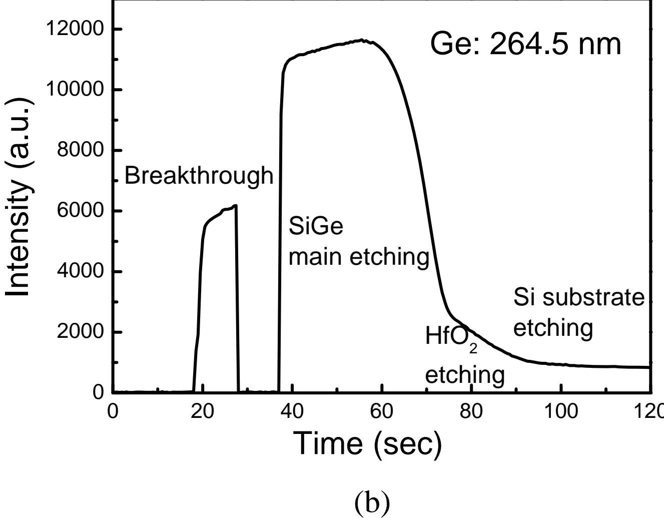


Fig. 5.9 Optical emission spectra during ICP etching of poly-$Si_{0.54}Ge_{0.46}$ using HBr. Optical emission peaks from Si at 251.0nm and Ge at 264.5nm and various etch products from 420nm to 500nm are indicated.

In Figs. 5.10 (a) and (b). A multi-step etching process was applied to the poly-SiGe / HfO_2 / Si gate stack. The oxide breakthrough was performed at the condition of 60 sccm Cl_2, 350 W inductive power, 150 W bias power and 10mTorr for 10 sec. The main etching was performed at the condition of 200sccm HBr, 350W inductive power, 135 W bias power and 10 mTorr. Gas flow and pressure were stabilized before each processing step. The result in Fig. 5.10 (a) shows the rapid increase of the Si optical emission peak after etching the gate stack for 80 sec, proving that the HfO_2 layer was removed from the Si substrate. Optical emission results of Ge from 264.5 nm (Fig. 5.10 (b)) show that the intensity began to drop to noise level after HfO_2 was removed. It is interesting to observe from the decrease of the Si peak (Fig. 5.10 (a)) and the increase of the Ge peak (Fig. 5.10 (b)) during the breakthrough period, that the Si/Ge ratio in the native oxide of poly-SiGe is higher than that in the bulk of poly-SiGe.



(a)



(b)

Fig. 5.10 Optical emission intensity with time during ICP etching of poly-$Si_{0.54}Ge_{0.46}$ / HfO_2 / Si-substrate gate stack using HBr, for (a) Si: wavelength 251.0 nm and (b) Ge: wavelength 264.5 nm.

5.4 Discussion

5.4.1 Profile control in ICP etching of poly-SiGe gate

It is interesting to be able to control the amount of the notching from the poly-SiGe gate sidewall by adjusting the etching process parameters. Oehrlein *et al.* [5.11, 5.21] reported that the surface of the poly-SiGe gate structure becomes either Si-rich in HBr plasmas or Ge-rich in CF_4 and Cl_2 plasmas. According to their observation, the SiGe surface resulting from the HBr experiments is expected to be Si-rich, and the local disturbance of the Si/Ge ratio at the surface is expected to result in more structural defects and thereby more available electrons. This can explain the development of the notching observed when Ge concentration increases. In addition, deeper notches were obtained from processing conditions where ion energy was reduced, that is, with higher pressure, higher inductive power, and lower

rf bias power (See Fig. 5.6). Here we propose the theory that notching of poly-SiGe gates develops when ion energy is insufficient to form a proper passivation layer on the sidewall in HBr plasmas. Foucher *et. al.* [5.22] reported that the sidewall is passivated by the SiO_x-based layer during poly-Si gate etching in HBr/O_2 plasmas. If the same mechanism is applied to SiGe etching, the etch products are likely to be chemically sputtered by ions and can be the main components of the sidewall passivation layers. Therefore it is plausible that experimental conditions of higher ion energy can result in thicker passivation layers and the less notching. Notch gates are currently being studied by some researchers [5.22-5.24] to develop short channel devices of gate channel length below 65nm.

There have been other notching studies in which "footing" was observed as an undesirable phenomenon originating from the conductivity of doped silicon [5.25, 5.26]. In these reports, the notching occurred during over-etching of the poly-Si against the dielectric underlayer when high selectivity between them could be attained. The notching was localized sharply at the interface between the doped poly-Si and the underlying dielectric layer. However, in our observations of Figs 4 and 5, the controlled notch from poly-SiGe is observed all across the depth of sidewalls, and is similar to "bowing". Considering that the currently studied SiGe gate stack requires a double layer composed of poly-Si on poly-SiGe [5.11, 5.27], the notching across the poly-SiGe sidewall may be used for the formation of a T-shaped short channel gate structure.

5.4.2 Etching selectivity control in ICP etching of poly-SiGe / HfO_2 gate stacks

According to previous observations of high-K dielectrics such as HfO_2, ZrO_2, Al_2O_3, $Ba_{0.5}Sr_{0.5}TiO_3$ and inert electrodes such as Pt as potential semiconductor materials [5.19, 5.28-5.33], the etch rates are strongly dependent on ion energy as well as ion density. In ICP etching using inductive power below 1000W and bias power below 500W, etch rates were mostly lower than 1000 Å/min, implying that their etching mechanism is predominantly dependent on sputtering by ion bombardment. The universal model for ion bombardment induced etching processes was suggested by Steinbruchel [5.34],

$$Y(E) \approx A(E^{1/2} - E_{th}{}^{1/2})$$

where *Y(E)* is the sputtering yield at ion energy *E,* and E_{th} is the threshold ion energy for sputtering. This model successfully predicted the relationship between the etch rate and the ion energy for sputtering dominant etching processes. In Fig. 8 (b), we found an approximately linear relation of the etch rates vs rf bias power during HfO_2 etching. But, we were not able to measure dc bias voltages, because this required a significant modification of our etch system (TCP9400SE). S. Norasetthekul *et al.* [5.19] reported that the etching of the sputtered HfO_2 films was not only ion-enhanced but also chemically-enhanced, showing deviation from the Steinbruchel model. Using another ICP etcher, further studies on the effects of the dc bias voltage are in progress to explore the etching mechanism for various HfO_2 films of different annealing and deposition conditions.

Since we can control the etch rates of HfO_2 from both the CF_4 and HBr plasmas, this will be an important method to control the etching selectivity of poly-

SiGe with respect to HfO$_2$. The minimum selectivity requirement of the film to the substrate, $S_{min,}$ is given by [5.35]

$$S_{\min} = \frac{t_{f,ave}}{t_{u,\max}} \left[\frac{(1+\alpha)(1+\delta)}{(1-\beta)} - \frac{(1-\alpha)}{(1+\beta)} \right]$$

where $t_{f\ ave}$ is average film thickness, $t_{u\ max}$ is maximum allowable consumption of the underlayer, α is the uniformity of film thickness, β is the uniformity of etch rate, and δ is the overetching amount. As an example, the advanced gate stack in the 100nm technology node could consist of a 1500Å thick poly-SiGe (thickness uniformity of 3%) film and a 30Å thick HfO$_2$ underlayer. If overetching up to 50% is allowed in the ICP equipment (with an etch rate uniformity of 3%), we will need to achieve a selectivity of 33 or higher in order to form an advanced gate stack by ICP etching. Considering that the removal rate of the remaining HfO$_2$ by diluted HF is extremely low, it can be important to remove most of the underlying HfO$_2$ by plasma etching without consumption of Si substrate. This can be done if the selectivity could be very precisely controlled in the neighborhood of 33 as a minimum.

There have been reports on effects of O$_2$ addition on etching selectivities of poly-Si to SiO$_2$ [5.36, 5.37]. The results from HBr/O$_2$ plasmas [5.36] showed that the poly-Si surface could be extensively oxidized with O$_2$ less than 2%, and expected that the poly-Si etching rates and thereby the etching selectivity could be lowered accordingly. On the other hand, the results from Cl$_2$/O$_2$ plasmas [5.37] showed that, the O$_2$ addition almost unaffected the poly-Si etch rates but lowered the SiO$_2$ etch rates via etch-deposition competition, and this resulted in the higher etching selectivity. In our results of Fig 7, the etching selectivity of poly-SiGe to HfO$_2$ increased significantly with the introduction of 3.8% O$_2$ in HBr. The results

from Fig. 9 (a) demonstrate that the etching selectivity could be sensitively controlled by changing the rf bias power in the presence of small amount of oxygen. We noticed from our preliminary XPS analysis that the change in the selectivity might be mainly due to the change in the film property of the HfO_2 underlayer. When O_2 is added to HBr, it dissociates quickly in the plasma to react with nonvolatile Hf or Hf etch products to form HfO_x or HfO_xBr_y, nullifying the etching of HfO_2 by HBr. We propose that, as the etching is carried out, the surface of the HfO_2 film becomes richer in Hf by a selective etching process for O, but it can quickly return to HfO_x when a certain amount of reactive O is available from the plasma. The precise addition of O_2 is critical in controlling removal rates of HfO_2 and thereby etching selectivities. According to this model, the processing window can be determined by competition between low selectivity from high etch rates of HfO_2 without O_2 and high selectivity from *in-situ* re-formation of HfO_2 withO_2.

5.5 Summary

A novel poly-SiGe/HfO_2 gate stack was formed by ICP etching. We were able to control the amount of notching that was formed by ICP etching of poly-SiGe, and to form a notch gate that can be used for short channel devices of gate length smaller than 65nm. Notching was controlled by varying the etching process parameters of inductive power, rf bias power, and pressure, as well as by varying the Ge concentration in poly-SiGe. Notching became more pronounced in the conditions where ion energy was reduced. Etching of HfO_2 was strongly dependent on the sputtering by ion bombardment. By controlling the etching selectivity of poly-SiGe to HfO_2 with the change in the rf bias power in the presence of a small amount of O

in HBr plasmas, we were able to demonstrate the processing feasibility of the formation of a poly-SiGe / HfO_2 gate stack using ICP etching. Optical emission by monitoring Si and Ge etch by products can provide sharp and obvious endpoint signals.

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Chapter 6

Formation of Novel Gate Stack of Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High-K Dielectric

6.1 Introduction

In chapter 1, we have introduced that to scale the oxide thickness, flash memory devices using nanocrystals (NCs) as floating gate (FG) have received considerable attention because of its excellent memory performance and high scalability [6.1, 6.2]. In NCs flash memory devices, charges are stored in discrete NCs instead of a continuous poly-Si FG. Hence, the devices can be less sensitive to local oxide defects, as shown in Fig. 6.1. Thinner tunneling oxide can be used without significant degradation in retention performance. As a result, the programming voltage can be reduced and the programming speed can be improved significantly [6.1].

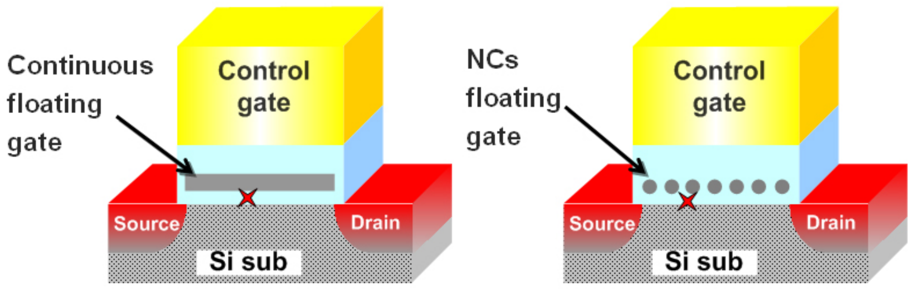


Fig. 6.1 Schematics of nonvolatile flash memory device using continuous floating gate and NCs floating gate.

From the viewpoint of production, the NCs flash memory process is similar to the silicon-oxide-nitride-oxide-silicon (SONOS) memory process, offering a reduced number of masks compared with the existing FG flash memory process [6.3], and leading to a corresponding reduction in cost for system-on-a-chip application employing such devices.

Table 6.1 Process steps of logic with embedded nonvolatile flash memories. Source: Motorola Embedded Memory Center.

Process Step	Logic Only	Embedded Floating Gate Nonvolatile flash memories	Embedded nanocrystals or SONOS type nonvolatile flash memories
Isolation Formation	♦	♦	♦
High Voltage Wells		2 masks	Saved
High Voltage Wells		1 mask	1 mask
Tunnel Oxidation		♦	Saved
Floating Gate Deposition/Patterning		1mask	Saved
ONO Deposition/Patterning		1mask	1 mask
Low Voltage Wells	♦	♦	♦
DGO Wells	♦	♦	♦
High Voltage Oxidation/Patterning		1 mask	1 mask
DGO Oxidation/Patterning	♦	♦	♦
Low Voltage Oxide Growth	♦	♦	♦
Gate Deposition	♦	♦	♦
NVM Stack Patterning		1 mask	Saved
NVM Source Halo Implant		1 mask	Saved
NVM Drain Implant		1 mask	1 mask
Gate Patterning	♦	♦	♦
High Voltage LDD Implants		2 mask	Saved
DGO LDD Implants	♦	♦	♦
S/D and Backend Processing	♦	♦	♦
Masking Step Adder	-	+11	+4

In Table. 6.1, process steps of a typical process flow of a SOC product, which includes logic device and nonvolatile flash memories is show. Number of

added process steps and masks for fabricating FG and discrete charge storage nonvolatile flash memories are compared. It can be found that with discrete charge storage, the process steps and number of masks can be significant reduced compared with conventional FG flash memories process.

The first NCs flash memory device was demonstrated using Si-NCs embedded in SiO_2 [6.4]. Since then, various materials such as Ge and metals have been used to form NCs FG on SiO_2 [6.5-6.7] and various storage mechanisms have been proposed. In semiconductor NCs flash memory devices, electrons can be stored either in the traps or the conduction band of NCs. There are evidences that electrons should be stored in interface states or bulk traps, rather than the conduction band, resulting in good retention property [6.8, 6.9].

Compared with Si, Ge has a narrower band gap and a similar electron affinity [6.10]. It has been reported that flash memory devices employing Ge-NCs instead of Si-NCs may have superior retention properties [6.8, 6.11, 6.12]. Ge-NCs flash memory devices using very thin SiO_2 tunneling oxide were demonstrated a few years ago and good retention performance was observed [6.5, 6.6].

In the chapter 1 of this thesis, we have introduced that to improve the electrical performance of flash memory devices, efforts are also made to replace the SiO_2 tunneling oxide and the $SiO_2/Si_3N_4/SiO_2$ control (interpoly) oxide of FG memory devices with high dielectric constant (high-K) materials. By using a high-k tunneling oxide, both lower programming voltage and better retention performance can be achieved because of the smaller conduction band offset between Si substrate and high-K dielectric and larger physical thickness of high-K dielectric, respectively [6.12, 6.13].

The control gate coupling ratio is given by $\alpha_g = C_{cg} / (C_{cg} + C_{mos} + C_{fs} + C_{fd})$, where C_{cg} is the capacitance between the control gate and the floating gate, C_{mos} is the capacitance between the floating gate and the channel, C_{fs} is the capacitance between the floating gate and the source, and C_{fd} is the capacitance between the floating gate and the drain. In Fig. 6.2, the equivalent capacitor circuit of a floating gate flash memory device is shown. C_{gs} and C_{gd} are the capacitance between control gate and source and drain. They can be neglected because of the thick spacers.

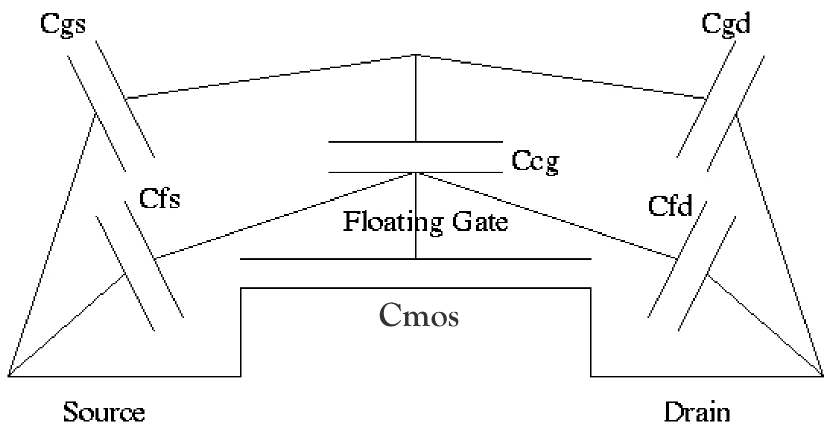


Fig. 6.2 Equivalent capacitor circuit of a floating gate flash memory device.

When high-K dielectric is used as the control oxide of FG memory devices, α_g can be increased because of the smaller equivalent oxide thickness (EOT) of the control oxide. This enables the control gate voltage to couple to the tunneling oxide more effectively, resulting in lower programming voltage; at the same time, the memory window can be enlarged [6.14]. Furthermore, the larger physical thickness of high-k control and tunnel oxides helps the charge retention. Such advantages have been identified recently in NCs FG memory devices and SONOS memory devices [6.12, 6.13-15]. The Hf based high-K materials were chosen in these studies

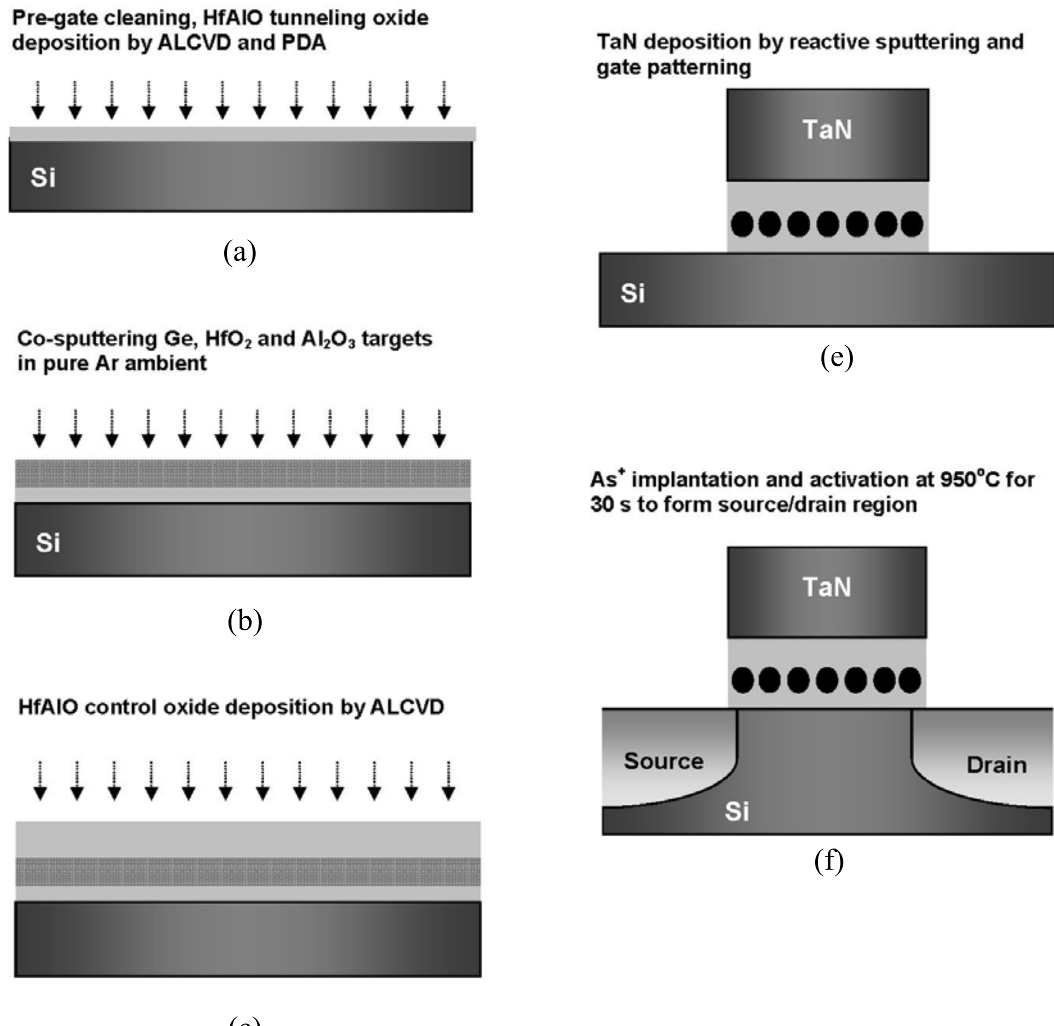
because they have been recognized as the most promising alternative gate dielectrics for future complementary metal-oxide-semiconductor (CMOS) devices. Therefore, considering the advantages of Ge-NCs, integrating Hf based high-K tunneling and control oxides with Ge-NCs could be a promising way to further improve the performance of NCs flash memory devices.

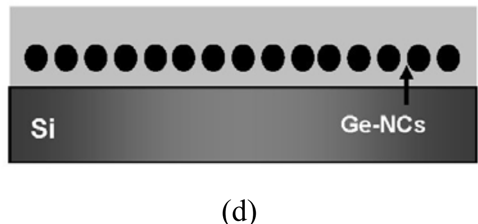
Besides the good electrical performance, we anticipated that a structure of Ge-NCs embedded in Hf based high-k materials could have process integration advantages. The change in Gibbs free energy (ΔG) of formation (at 298.15 K) of GeO_2 (-111.8 kcal / mol) is much smaller than those of the Hf based high-k materials such as HfO_2 (-260.1 kcal / mol), Al_2O_3 (-378.2 kcal / mol), and SiO_2 (-204.75 kcal / mol) [6.16]. This indicates that Ge is less likely to react with O than Hf, Al and Si during the thermal cycles of a CMOS process, leading to a reliable process and a stable structure [6.17]. In this work, we fabricate nonvolatile flash memory devices employing Ge-NCs embedded in HfAlO dielectrics, and investigate their memory properties, including writing, charge retention and endurance.

6.2 Experimental Setup

The devices were fabricated on p-type (100) Si wafers with boron doping concentration of 2×10^{15} cm^{-3}. HfAlO was chosen as the tunneling and control oxide because it showed good thermal stability [6.18], and TaN was chosen as the

control gate because it showed good process compatibility with high-k dielectrics [6.19]. The key process steps including the formation of Ge-NCs in HfAlO are shown in Figs. 6.3 (a) – (f).





(d)

Fig. 6.3 Process flow for device fabrication.

After the pre-gate cleaning in 1% dilute HF, a 5 nm (optical thickness measured by an ellipsometer) HfAlO (HfO_2-Al_2O_3 laminated structure with an atomic ratio of Hf : Al = 1 : 1) tunneling oxide was deposited at 320 ^oC by an atomic layer chemical vapor deposition (ALCVD) using $HfCl_4$ (Hf source) and trimethyl aluminum (Al source) precursors, and H_2O (Fig. 6.3 (a)). A post-deposition-anneal (PDA) was performed in N_2 ambient at 700 ºC for 30 s. The Ge-NCs layer was formed on the tunneling oxide by a co-sputtering and an anneal process [6.17]: (1) at first, around 10 nm thick film was deposited by sputtering Ge, HfO_2 and Al_2O_3 targets together (Ge : HfO_2 : Al_2O_3 = 1 : 3 : 1 by volume) in a pure Ar ambient (Fig. 6.3 (b)); (2) a 8 nm HfAlO control oxide (the atomic ratio of Hf : Al = 1 : 1) was then deposited using ALCVD (Fig. 6.1 (c)); and (3) an anneal at 700 ^oC in N_2 ambient for 30 min was performed to form the Ge-NCs (Fig. 6.3 (d)). After the deposition of TaN and the gate patterning of a 20 μm channel length (Fig. 6.3 (e)), source/drain regions were formed by an As^+ ion implantation followed by an activation anneal at 950 ºC for 30 s in N_2 ambient (Fig. 6.3 (f)).

6.3 Experimental Results

6.3.1 Formation of Ge-NCs in HfAlO

Figure 6.4 shows the bright field transmission electron microscope (TEM) image taken from the gate stack after step (f) in Fig. 6.3. A high resolution image of one typical Ge-NC is inserted for revealing the geometrical characteristics of the Ge-NCs. Energy dispersive x-ray diffraction analysis shows that the dark dots between the two HfAlO layers are pure Ge. After several thermal processing steps including

source/drain anneal, we found that the HfAlO in the tunneling oxide, control oxide and co-sputtered layers remained amorphous.

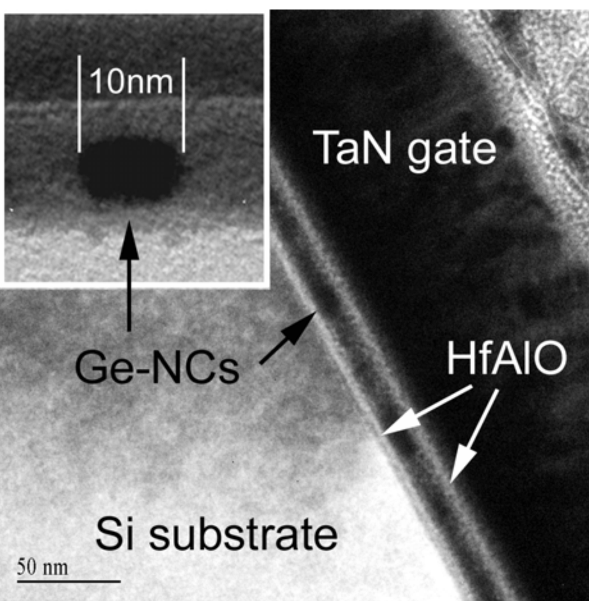


Fig. 6.4 A cross-sectional TEM image of the gate stack fabricated in this work. The dark regions are induced by strong Bragg dispersion by Ge-NCs, and the inset picture shows the details of the Ge-NCs.

The structure of Ge-NCs embedded in HfAlO is clearly observed in Fig. 6.4, and the distinct interface between Ge-NCs and HfAlO indicates that no interfacial layer is formed. A typical Ge-NC shows an elliptic shape with a diameter and a height of 10 nm and 7 nm, respectively.

At the same time, x-ray diffraction spectrum shows that in the as deposited film, Ge is in amorphous phase, and after anneal, Ge is in crystal phase, as shown in Fig. 6.5. This supported that the dark dots observed in Fig. 6.4 is Ge-NCs. This is because it is very clear that the matrix is in amorphous phase, crystal signal should come from dark dots, where the strong Bragg diffraction occurs.

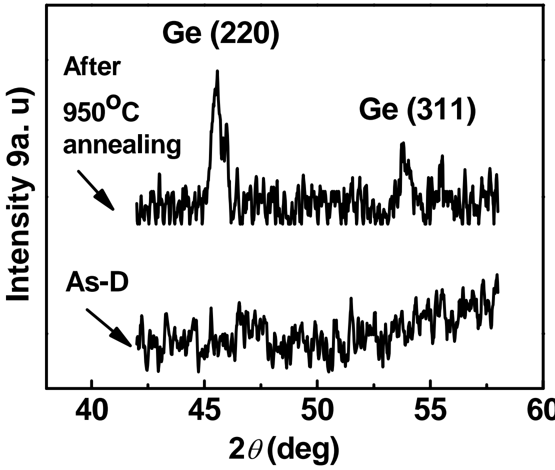


Fig. 6.5 XRD spectra of Ge in HfAlO before and after anneal.

In the co-sputtering process, as the Ge, Al_2O_3 and HfO_2 targets were sputtered in the pure Ar ambient and the base pressure of the process chamber was 10^{-7} Torr, the amount of oxygen in the co-sputtered layer is expected to be just enough to oxidize Al and Hf. Since ΔG of the formation of GeO_2 (-111.8 kcal/mol) is much larger than that of HfO_2 (-260.1 kcal/mol) and Al_2O_3 (-378.2 kcal/mol), and the difference of ΔG between the formation of elemental Ge, Hf and Al can be neglected, in both solid reactions of $GeO_2 + Hf \rightarrow HfO_2 + Ge$ and $3GeO_2 + 4Al \rightarrow 2Al_2O_3 + 3Ge$, ΔG is negative. Hence, the mixture of HfO_2, Al_2O_3 and Ge has the lowest Gibbs free energy in the co-sputtered film. After anneal, all O atoms were consumed to oxidize Al and Hf, leaving Ge atoms to agglomerate in the HfAlO matrix. This results in the formation of Ge-NCs embedded in HfAlO.

This process is experimental reveal by an materials analysis using x-ray photoelectron spectroscopy (XPS). Fig. 6.6 shows the XPS spectra obtained from the co-sputtered film, revealing the presence of HfO_2, Al_2O_3, Ge, GeO_2 and Hf in the as-deposited film.

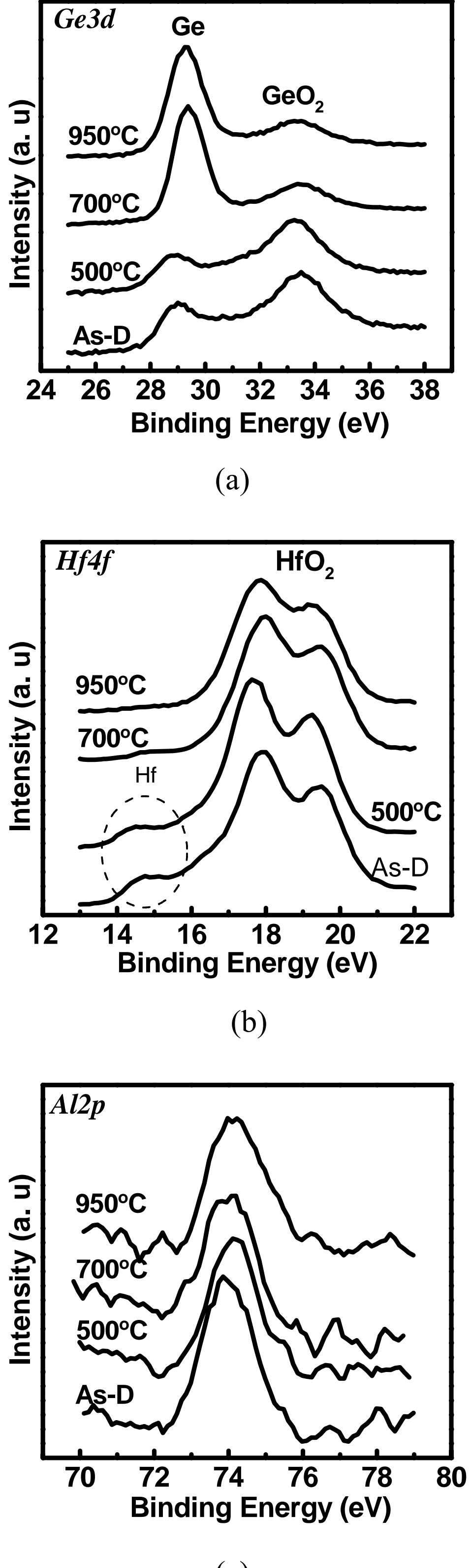


Fig. 6.6 XPS spectra of (a) Hf*4f*, (b) Ge*3d* and (c) Al*2p* from the HfO_2, Al_2O_3 and Ge co-sputtered films as deposited and annealed at different temperatures.

Hf in the as-deposited film comes from the HfO_2 particles, from which oxygen atoms are sputtered away. As a result, GeO_2 is formed. The Al*2p* peak shifts slightly towards higher energy upon annealing, suggesting that some Al atoms that are not fully oxidized in the as-deposited film are substantially oxidized in the followed annealing process. At the same time, Hf is oxidized and a substantial amount of GeO_2 is reduced. GeO_2 was reduced to Ge in the oxidation process of Hf or Al, as anticipated in the introduction of this chapter.

Despite the increase of the annealing temperature from 700ºC to 950ºC, no changes in XPS peaks corresponding to Hf*4f*, Ge*3d* and Al*2p* were observed. This also indicates that no Hf or Al germanide or germanite is formed.

In NCs flash memories, the size of NCs is an important factor that affects electrical performance. She *et al*. [6.20] reported that the size of Ge-NCs embedded in SiO_2 should not be scaled below 5 nm, because the quantum confinement effect becomes very significant for such small Ge-NCs [6.21]. Large quantum confinement leads to the conduction band in the nanocrystal being much higher than that of the Si substrate resulting in enhanced leakage from NCs and shorter retention time. This is especially true for the Ge-NCs embedded in HfAlO due to the smaller conduction band offset. On the other hand, the size of NCs also should not be too large. For a given density of NCs, a larger NC size reduces the inter-NCs spacing and increases charge loss, resulting in poor retention. According to the simulation result, the optimum NC size is about 5 nm for flash memory devices using Ge-NCs embedded in SiO_2 [6.20]. For Ge-NCs embedded in HfAlO, the optimum size should be a little larger as the barrier height is lower. In this work, the typical size of Ge-NCs obtained is in the range of 7 nm to 10 nm, indicating that Ge-NCs formation in HfAlO by phase separation could be a promising way to achieve the

ideal NC size for Ge-NCs high-k flash memory devices. We also found that the Ge-NCs were chemically inert in HfAlO as indicated by the thermodynamic properties, and TEM analysis shows no obvious interfacial layer even when the process temperature was up to 950 ^{o}C. Hence, the structure demonstrated in this study can be realized in an industrially compatible CMOS processes.

The density of Ge-NCs embedded in HfAlO matrix was estimated to be about 2×10^{11}cm^{-2} by an electrostatic force microscopy (EFM) image taken after annealing (Fig. 6.7). Because of the difference in the dielectric constants between Ge and HfAlO, the oscillating phase shift of the EFM probe is different under the electric field. The white dots in the EFM image are the Ge-NCs.

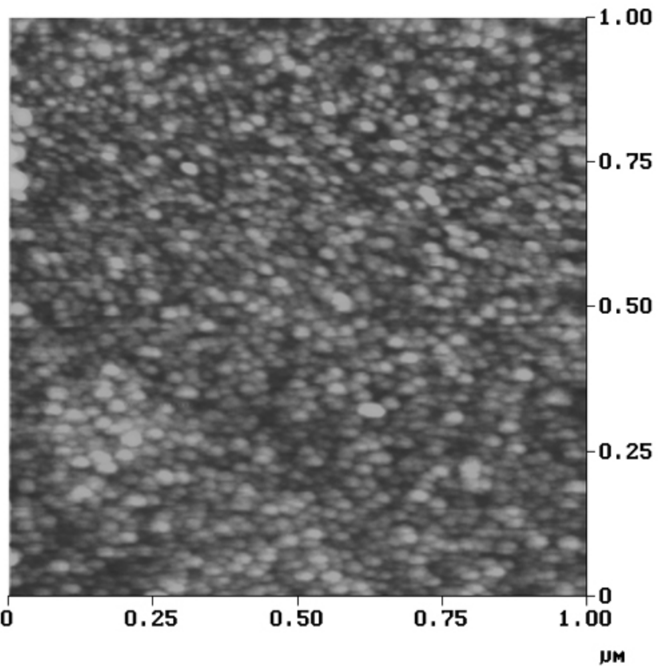


Fig. 6.7 EFM image of Ge-NCs embedded in HfAlO matrix. Tip voltage is 5 V.

Based on this particular EFM image with a nanocrystal density of 2×10^{11} cm^{-2}, the average distance between the centers of adjacent NCs is estimated to be about 22.4 nm, hence the average distance between the two NCs is estimated to be

around 12 nm. This ensures electrical insulation between the Ge-NCs. Note, however, that the density of the Ge-NCs can be increased further, since the inter-NCs distance can be reduced below 12 nm.

To reveal the Ge distribution in the device, secondary ion mass spectroscopy (SIMS) depth profiling analysis on the gate stack was performed, as shown in Fig. 6.8. A very sharp increase in the Ge signal is observed in the middle of the Al trace along the sputtering time axis and the trace of Ge disappears earlier than the ones for Al and Hf. This means that the Ge-NCs are well confined between the two ALCVD HfAlO dielectric layers and no obvious diffusion through the oxide occurs. This is very important because the presence of Ge in the tunneling or control oxides can form the leakage path which degrades retention performance. Furthermore, any Ge presence in the channel can degrade transistor performance [6.22]. The TEM image analysis and the SIMS result suggest that the Ge-NCs embedded in HfAlO show good thermal stability, which is very important for CMOS process integration.

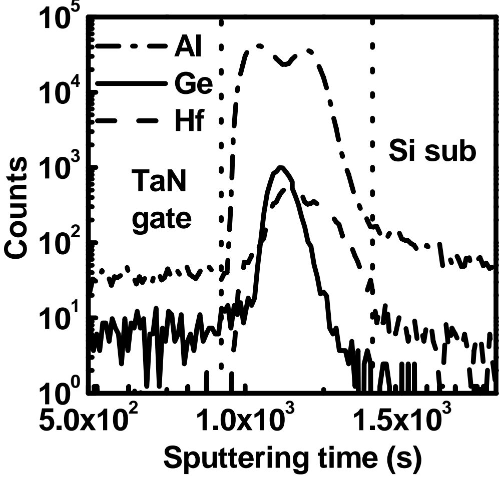


Fig. 6.8 SIMS analysis of Al, Ge and Hf obtained from the gate stack of the device.

6.3.2 Memory Effect of Ge-NCs embedded in HfAlO matrix

In Fig. 6.9, the C-V characteristics of MOS capacitors with HfAlO/Ge-NCs/HfAlO stack are compared to a control sample without Ge NCs. It clearly indicates that the memory effect originates from the Ge-NCs. The V_{fb} shift of 2.2V was attained after stressing the device for 100ms at 12V. At the same time, very little shift was observed from the control sample, of which gate stack is simple TaN/HfAlO/Si stack. The comparison of the *C-V* results between the device and control samples indicated that the memory effects come from Ge-NCs mainly, not the HfAlO matrix.

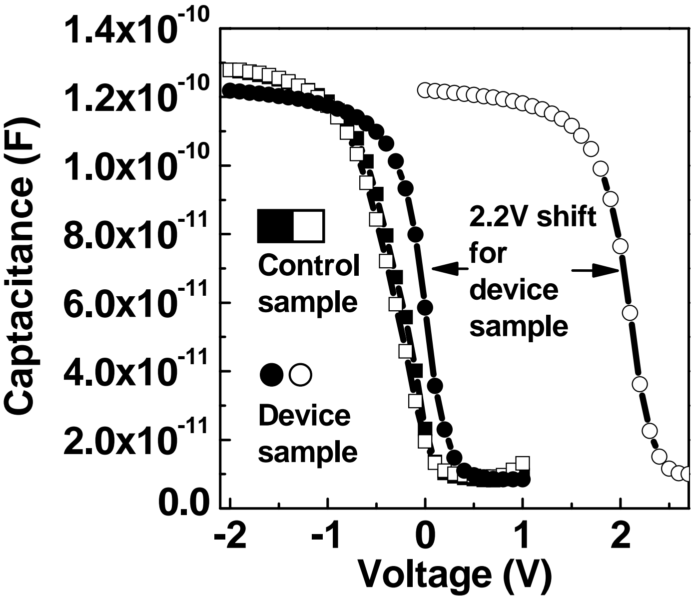
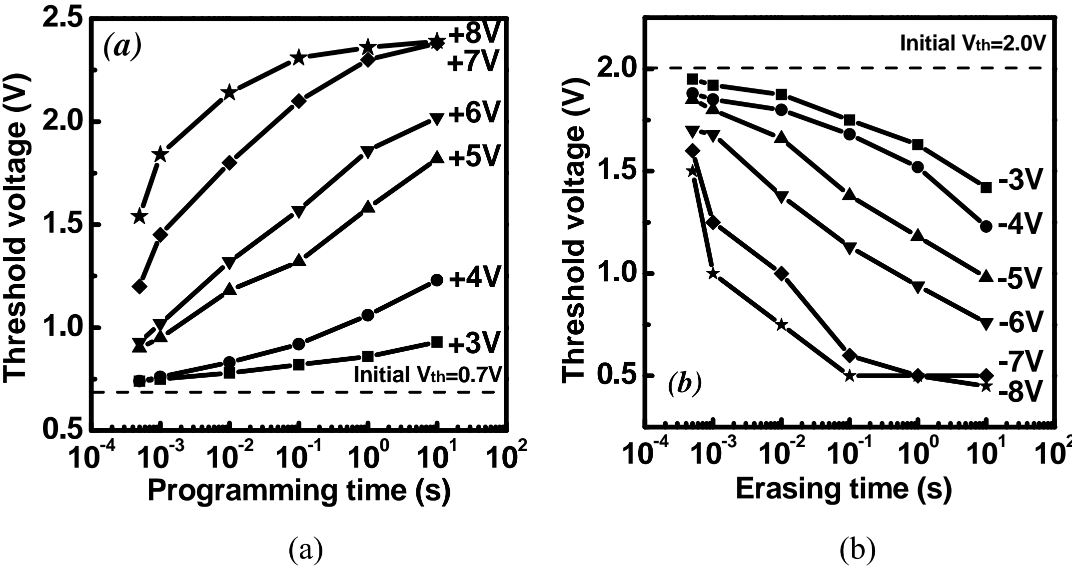


Fig. 6.9 C-V characteristics of the MOS capacitors from control sample and device sample before and after applying 0.1 s, 12V stress.

6.3.3 Programming and erasing characteristics

The typical programming and erasing characteristics as measured from fabricated devices are shown in Figs. 6.10 (a) and (b), respectively. In the measurement of V_{th} in this work, there is a shift of about 0.1 to 0.2 V between forward scan and backward scan in I_d-V_g measurement because of the charge trapping and de-trapping in the HfAlO dielectric. In order to understand memory effects from the Ge-NCs, all the threshold voltages were obtained in the forward scan in this study. In Fig. 6.10 (a), it can be observed that when the programming voltage is increased to about 6 - 7 V, the V_{th} shift increases rapidly, suggesting a change in the programming mechanism.



(a) (b)

Fig. 6.10 Writing transient characteristics during (a) programming and (b) erasing operations for various gate voltages and pulse durations.

The tunneling mechanisms through high-k dielectric materials are still under investigation. Fowler–Nordheim (*F-N*) tunneling, direct tunneling, and Frenkel-Poole tunneling (*F-P*) have been proposed to explain the experimental results at the various voltages [6.23, 6.24]. To understand the programming mechanism in our devices, we perform the following analysis. Considering that the gate length of the measured device is large, the contribution of the capacitance of the FG to source and drain regions can be neglected, the control gate coupling ratio of our device is then estimated to be 0.38. Considering that the conduction band offset between the HfAlO tunneling oxide and the (100) Si substrate is 2.1 eV [6.23], the work functions of TaN on HfO_2 and HfAlO are the same at 4.41 eV [6.25] and the surface potential of Si substrate is 0.6 - 1.0 V in the strong inversion region, the *F-N* tunneling voltage should be around 6.0 - 6.4 V. This is the same as the programming voltage where a steep increase of programming speed was observed. Hence, *F-N* tunneling is likely to be the main mechanism of programming operation at high voltages in our devices. Under this voltage, the control oxide is also in the *F-N* tunneling regime. This is because the control gate coupling ratio is below 0.5 and both the control and tunneling oxides are HfAlO with the same Hf/Al ratio. The voltage applied on the control oxide is higher than that on the tunneling oxide.

Saturation of V_{th} shift is clearly observed at a programming voltage of ~ 7 - 8 V for 1 - 10 sec in Fig. 6.10 (a). This is a universal characteristic of NCs flash memory devices [6.1-6, 6.13]. To understand the effect of replacing Si-NCs with Ge-NCs in flash memory devices with Hf based high-k tunneling and control oxides, we compare the charge storage capabilities between our device and Lee *et al*'s work [6.13]. For a given V_{th} shift, the number of electrons stored in the NCs can be calculated from the distance between the location of the stored charges and the

control gate electrode. However, unlike conventional FG devices, the thickness of control oxide cannot be simply used for the estimation, because the charge distribution in the NCs is unlike the charge distribution in the conventional FG. To estimate the difference in charge storage capabilities between devices with Ge-NCs embedded in HfAlO and Si-NCs embedded in HfO_2, we assume that all charges are stored in the middle of the NCs along the normal of the wafer surface. EOT of the control oxide is 4.6 nm for our device, as determined by fitting the measured *C-V* data with a simulation that takes quantum mechanical effects in the inversion layer into account. Since the EOT of the control oxide in the work by Lee *et al.* [6.13] is 4.5 nm, and the density and size of Si-NCs in that work are similar to this work, the largest amount of electrons that can be stored in each Ge-NC is estimated to be about 3 times of that in Si-NC on the average.

Recently, Compagnoni *et al*. [6.14] proposed a model for program/erase dynamics in the flash memory devices employing Si-NCs embedded in SiO_2. The maximum shift of V_{th} during programming operation is determined by the design of devices as well as the mode of programming. Based on their model, in Figs. 6.11 (b) and (c), the band diagrams of the program mode at low electric field (direct tunneling for tunneling oxide and *F-N* tunneling for control oxide, when V_g = 5.5 V) and high electric field (*F-N* tunneling for both tunneling oxide and control oxide when V_g = 7 V) are illustrated for the device structure of this work. The numerical values of band gap and band offset are taken from the literature [6.12, 6.24, 6.25]. In Figs. 6.11, $I_{e,\ in}$ and $I_{e,\ out}$ represent the injection current through the tunneling oxide and the emission current through the control oxide by electrons, respectively, and $I_{h,out}$ represents the hole current from the NCs to the substrate.

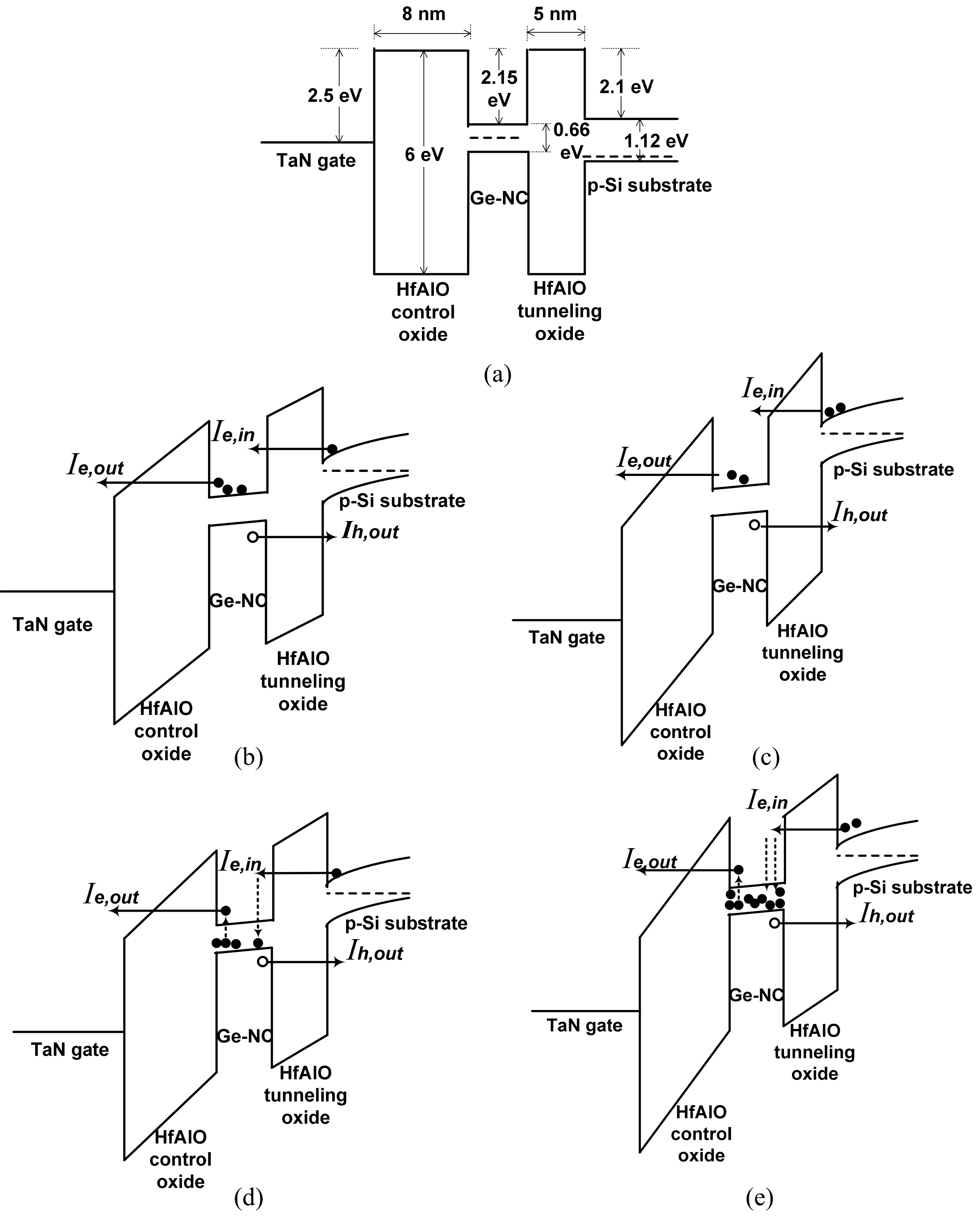


Fig. 6.11 Energy band diagrams of the gate stack (a) at flat band condition; (b) at low and (c) at high electric field programming modes. Traps in Ge-NCs are not taken into account. With traps taken into account, the energy band diagram at (d) low and (e) high electric field programming modes are also shown. Electrons and holes are represented by solid and open circles respectively.

In Compagnoni *et al.*'s model, $I_{h,out}$ is neglected and steady state is achieved when $I_{e,\ in} = I_{e,\ out}$. At low electric fields, the steady state is achieved when the tunneling oxide is in the direct tunneling regime whereas the control oxide is in the *F-N* tunneling regime, hence a large amount of charges can be stored in NCs because of "well separated" oxide fields (Fig. 6.11 (b)). However, at high electric field, NCs can only store very few electrons as nearly the same current flows through both the tunneling and control oxides by the *F-N* tunneling (Fig. 6.11 (c)). Therefore, the maximum memory window is always obtained by low voltage programming, when tunneling oxide is biased in direct tunneling region and control oxide is biased in *F-N* tunneling region [6.14].

If electrons are stored in the conduction band of the Ge-NCs in our device, the phenomena observed in programming operation should be similar to the simulation results in ref. 6.14. However, a very large saturated V_{th} shift is obtained by high voltage programming (both tunneling and control oxides are in *F-N* tunneling region) in our experiments, which cannot be explained by the model in ref. 6.14. In that model, electrons trapped by interface states or bulk defects are not taken into account. In Figs. 6.11 (d) and (e), the band diagrams of the gate stack, where traps have been taken into account in programming operation at low and high fields, are shown respectively. In these cases, after tunneling through the tunneling oxide, a fraction of electrons cannot stay in the conduction band of Ge-NCs and they will be trapped in the interface states between Ge-NCs and HfAlO or bulk defect states in the Ge-NCs. For the electrons in the trap levels, the tunneling from NCs to the gate cannot be simply treated as direct tunneling or *F-N* tunneling. For example, these electrons could emit to the conduction band first, and then tunnel to the gate. As a result, the tunneling probability is lower than that from conduction band to gate.

This allows higher potential of NCs to achieve the steady state ($I_{e,\,in} = I_{e,\,out}$), and therefore more charges can be retained in NCs, compared with the case without traps in programming. This is similar to the phenomenon observed in the metal NCs flash memory devices [6.26], in which a metal with a larger work function (electron stored at a deeper energy level) can provide a larger memory window. It is plausible that a large amount of traps existent in Ge-NCs results in a large memory window at high fields that is observed in our devices.

It is not easy to compare the programming efficiencies between Ge-NCs, SiGe-NCs and Si-NCs flash memory devices using Hf based high-k dielectric at this moment, because the control gate voltage coupling ratios and the thicknesses of tunneling oxides are different in existing publications [6.12, 6.13]. However, a high trap density could be an advantage in improving the programming efficiency because it can provide a high capture cross-section for electron trapping.

The saturation of V_{th} shift is also observed in the positive voltage region for erasing operation, as shown in Fig. 6.10 (b). After full erasure, the V_{th} is still positive and no serious over-erase is found. To further investigate this phenomenon, we performed an additional erasing operation to the already erased devices.

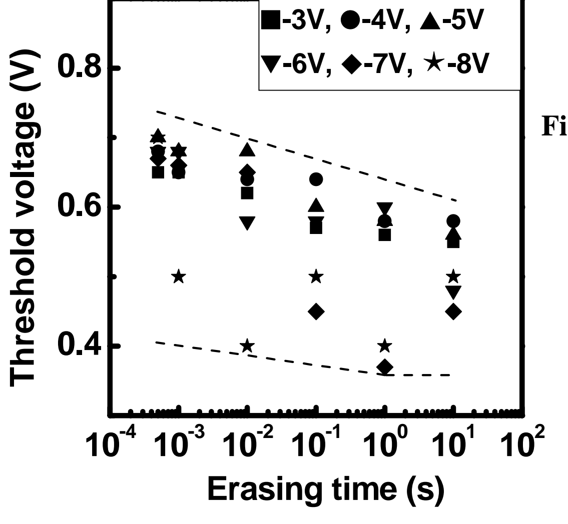


Fig. 6.12 Over-erase characteristics of the devices. Erasing operation is performed for the devices that have already been erased.

In Fig. 6.12, the typical over-erase characteristics are shown. We find that the basic phenomena from the measured devices are quite similar to each other, that is, V_{th} of the device is rarely reduced below to 0.3 V. Some instability of V_{th} after high voltage erase for a long time observed in Fig. 6.9 could be caused by the trapping effect of the HfAlO matrix. Considering that V_{th} of the neutral device is about 0.6 V, it is understood that our device cannot store many holes. However, there are many states available in the valance band in each Ge-NC ($N_v = 5.7 \times 10^{18}/cm^3$ for undoped Ge [6.12]). The valence band offset between HfAlO and Ge-NCs is estimated to be about 3.3 eV [6.12, 6.24], which should also be high enough to store holes. Hence, anti-over-erase characteristic should not be related to the storage capability of holes in the Ge-NCs embedded in HfAlO.

Similar to the programming mode, the final state in the erasing operation is determined by the injection and emission of electrons and holes, as well as the potentials of the NCs with charges stored [6.14]. As the hole tunneling current is 1-2 orders lower than the electron tunneling current through HfAlO dielectric [6.24], electron tunneling dominates the erasing operation, and hole tunneling can be neglected. If the control oxide cannot block electron tunneling effectively, the electron tunneling current through the control oxide will be significant, resulting in a small negative shift from the neutral V_{th} after the complete erasing. This indicates that the anti-over-erase characteristic observed in our device is due to the design of the oxide thicknesses in our device. On the other hand, compared with the programming operation, the small memory window acquired by erasing operation indicates that there are few hole traps available in the Ge-NCs.

6.3.4 Data retention and rewrite endurance properties

Figure 6.13 shows the data retention characteristics at 85°C [6.27], demonstrating that a 0.7 V memory window can be maintained after 10 years. In the retention mode (control gate, source/drain and substrate are all grounded), the FG potential can be obtained by the equation, $Q = \Delta V_{th} C_{cg} = V_{FG} (C_{cg}+C_{mos})$, where Q is the charge stored in the FG, ΔV_{th} is the memory window, and V_{FG} is the FG potential.

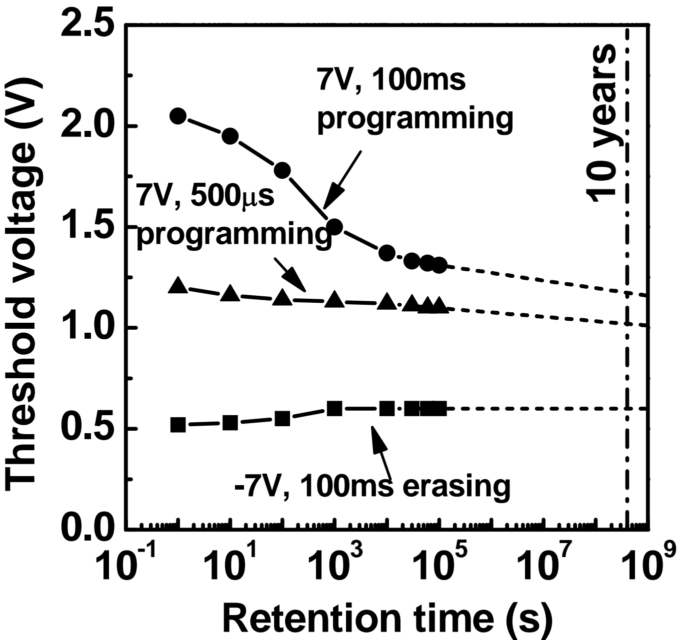


Fig. 6.13 Data retention characteristics of the devices at 85 °C.

For a 1.5 V initial memory window as observed in Fig. 6.10 (using 7 V programming for 100 ms), the FG potential is to be 0.58 V if the FG is assumed to be continuous. Considering that the area coverage of the substrate by NCs FG is 0.16 (calculated by the average size of 10 nm and the center to center distance of 22 nm, as shown in Fig. 6.14) the average electron potential of the NCs FG can be as

high as 3.56 V for ΔV_{th} = 1.5 V. This potential is much higher than the barrier height of the HfAlO control and tunneling oxides, so that the electron loss rate can be very high. This could be the reason for the rapid initial charge loss.

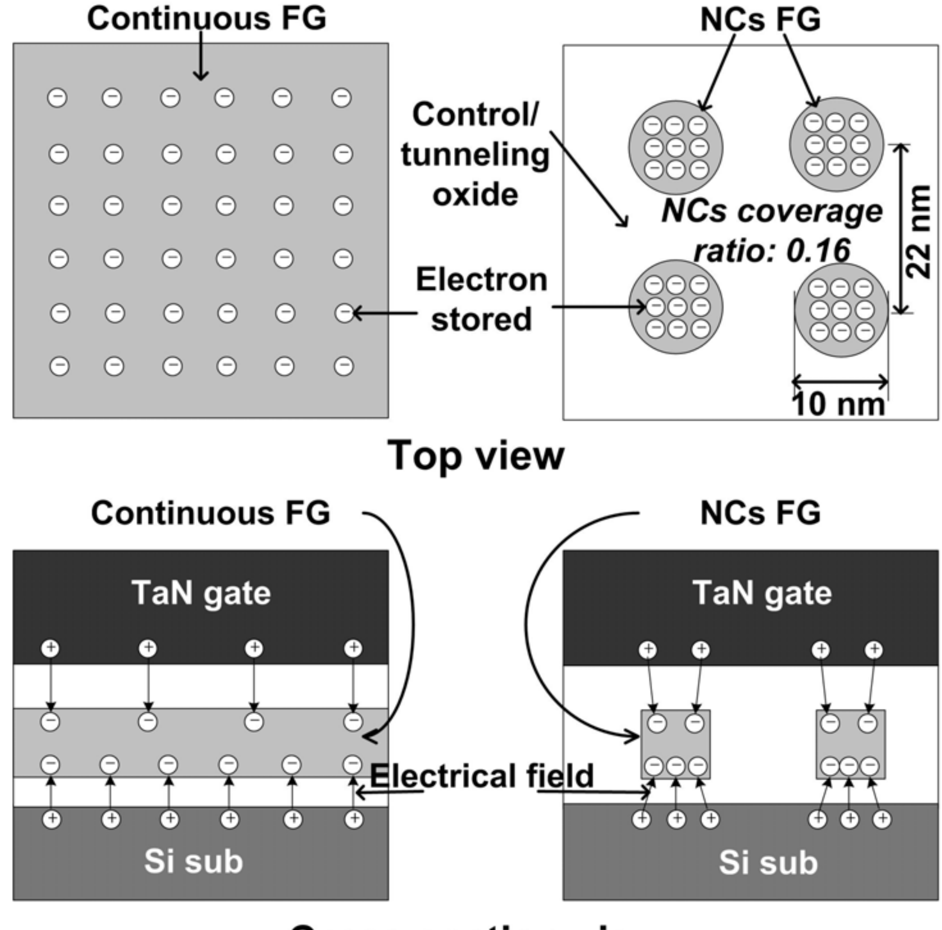


Fig. 6.14 Schematic diagrams of the top view and cross sectional view of electron storage in the continuous FG and NCs FG. The local electron density and potential in NCs are higher than those in a continuous FG for a given stored charge density.

Beyond 10^3 s, ΔV_{th} is reduced to about 0.9 V, and the electron loss rate decreases significantly. We notice that when ΔV_{th} = 0.9 V, the average V_{FG} of NCs

is about 2.14 V which is near the transition point of that average potential of NCs is lower than the barrier height of the HfAlO control and tunneling oxides, and the direct tunneling should become a main mechanism of electron loss. Since the physical oxide thickness used in this work is much smaller than that of the usual FG flash memory devices [6.27], the good retention property should be attributed to the immunity of NCs FG to local defects in the dielectric as well as deep trap levels in Ge-NCs or at interfaces between Ge-NCs and HfAlO.

Figure 6.15 shows the endurance performance for both programmed and erased states. The consistency of the trapping and de-trapping properties of HfAlO is indicated by the error bars. It is found that no obvious V_{th} shift occurs after 10^6 rewrites, and neither significant electron nor hole injection to HfAlO that can accumulate fixed charges occurs. This shows that HfAlO can meet the rewriting operation requirement of flash memory devices [6.27].

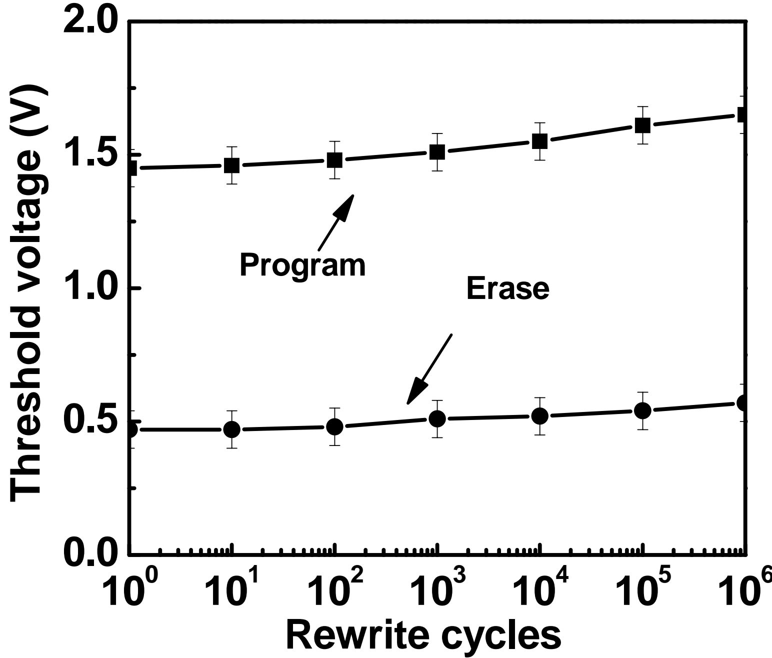


Fig. 6.15 Endurance characteristics of the devices. Pulses of ±5 V for 1 ms are applied. Write and erase conditions for read-out are 5 V for 1 s and -5 V for 1 s, respectively.

6.4 Conclusions

In this work, Ge-NCs were successfully formed in HfAlO high-K dielectric using a phase separation approach with industry compatible CMOS process. We fabricated a nonvolatile flash memory device using Ge nanocrystals (NCs) floating gate (FG) embedded in HfAlO high-K tunneling/control oxides. Results show that Ge-NCs have good thermal stability up to ~1000 ^{o}C in the HfAlO matrix as indicated by the negative Gibbs free energy changes for both reactions of $GeO_2 + Hf \rightarrow HfO_2 + Ge$ and $3GeO_2 + 4Al \rightarrow 2Al_2O_3 + 3Ge$. This thermal stability implies that the fabricated structure can be compatible with the standard CMOS process with ability to sustain source-drain activation anneal temperatures. Compared with Si-NCs embedded in HfO_2, Ge-NCs embedded in HfAlO can provide more electron traps, thereby enlarging the memory window. It is also shown that this structure can achieve low programming voltage of 6 - 7 V for fast programming, long charge retention time of 10 years maintaining a 0.7 V memory window, and good endurance characteristics of up to 10^6 rewrite cycles. This work shows that the Ge-NCs embedded in HfAlO is a promising candidate for further scaling of FG flash memory devices.

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Chapter 7

Formation of Novel Memory Gate Stack Using Al_2O_3 High-K Nano-Dots Embedded in SiO_2

7.1 Introduction

Since the silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory was first introduced in the 1960's [7.1], it has become one of the most attractive candidates for the future scaling of nonvolatile semiconductor memories [7.2, 7.3]. It is reported that lateral migration of electrons can be suppressed because of the discrete nature of charge traps in the sandwiched trapping layer of SONOS-type memories, especially when some high-K dielectric were used as trapping layer [7.2], hence devices are less vulnerable to local oxide defects compared with conventional continuous floating gate nonvolatile memories, bringing about advantages in retention, reliability and scalability [7.2, 7.3].

In chapter 1 and 6, we have introduced that nanocrystal floating gates of discrete charge storage nodes using semiconductor or metallic materials have been extensively studied in recent years for nonvolatile memory applications [7.4-7.6], as an innovative method to suppress lateral migration of electrons in semiconductor memory devices. It is generally known that SiO_2 contains much fewer traps than silicon nitrides or high-K dielectrics [7.7]. If a continuous trapping layer in SONOS-type memories can be replaced by a layer with trappy dielectric nanodots

(NDs) embedded in SiO_2, *e.g.*, nanocrystal floating gates embedded in a dielectric, lateral migration of electrons via *F-P* tunneling can be significantly suppressed, resulting in further improvement in charge retention. In Fig. 7.1, physical mechanisms and its advantages of this idea are illustrated.

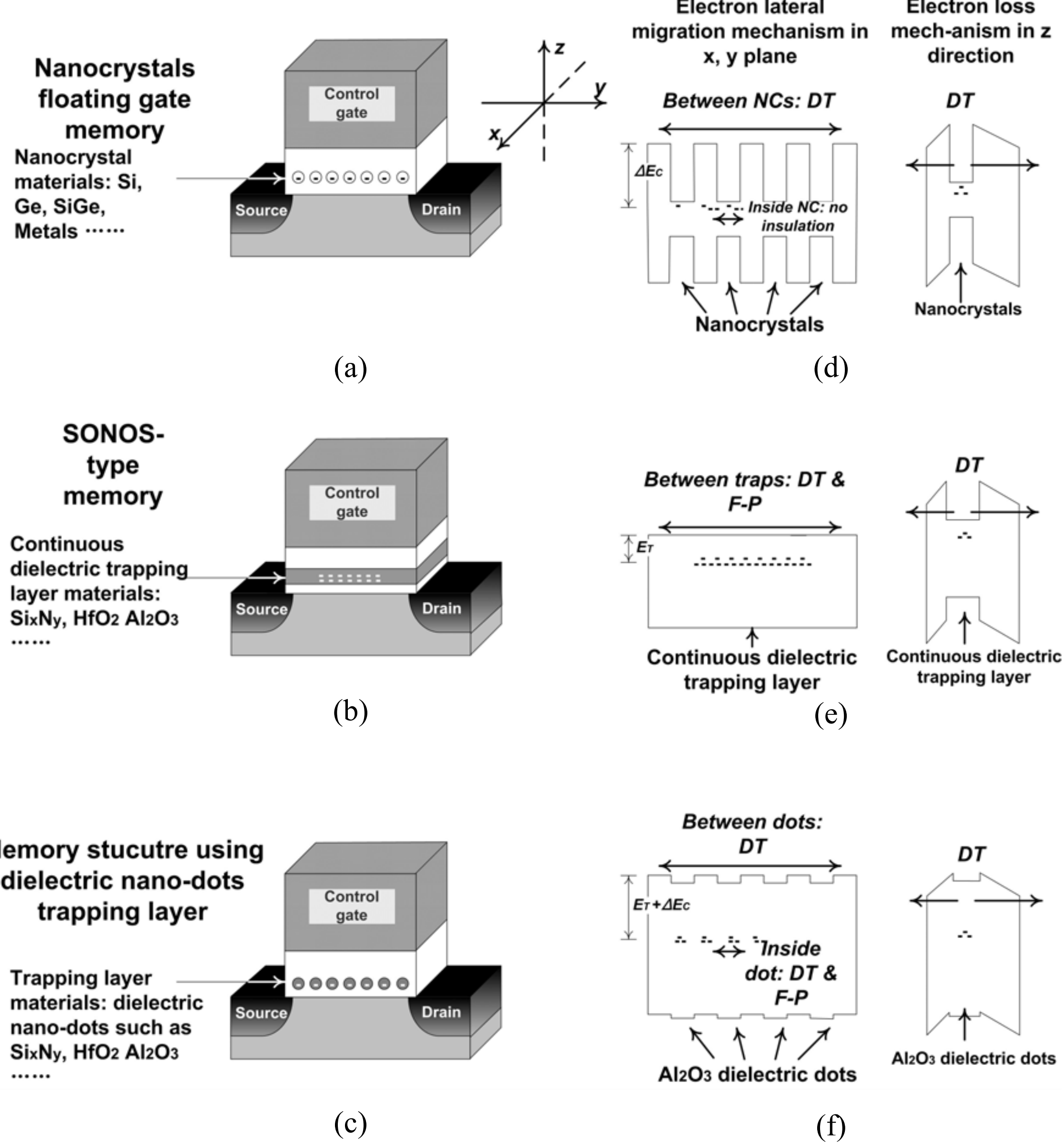


Fig. 7.1 Illustrations of (a) nanocrystals floating gate memory, (b) SONOS-type memory and (c) the memory structure proposed in this work, and their relevant band diagrams and electron loss mechanism (d, e and f) along the wafer plane and vertical direction of the gate stacks. "-" represents electrons stored at the energy levels in each memory structures. Fig. 1 (f) is drawn based on SiO_2/Al_2O_3 nano-dots/SiO_2 structure.

NCs FGs (Fig. 7.1 (a)) and SONOS-type memories (Fig. 7.1 (b)) [7.2, 7.3] have been studied for achieving good retention because of their discrete charge storage capability and lower vulnerability to oxide defects. In NCs memories, electrons in different NCs are insulated by good dielectric materials such as SiO_2, and any electron migration between NCs occurs via direct tunneling (DT), as shown in Fig. 7.1 (d). In SONOS memories, electrons are dispersed in the trappy dielectric, therefore the lateral migration of electrons in SONOS-type nonvolatile memories cannot be inhibited completely, as electrons can migrate laterally via direct tunneling and trap assisted tunneling *F-P* tunneling along the trapping layer as shown in Fig. 7.1 (e), degrading retention properties. In this work, we propose a novel memory structure which combines the advantages of NCs and SONOS memories. Dielectric nano-dots (NDs) are used as charge storage nodes (Fig. 7.1(c)). The memory device structure employs trappy dielectric NDs as charge storage nodes, which are insulated by high quality SiO_2. Compared with the conventional SONOS-type memories, lateral migration via F-P tunneling can be significantly suppressed using this device. Compared with NCs memories, this structure can also provide additional advantage in electrical insulation between charges within each charge storage node, as shown in Fig. 7.1 (f).

Various approaches to form semiconductor or metallic nano-crystals in dielectrics have been made [7.4-7.6, 7.8]; however, there have been very few reports about the formation of dielectric NDs on SiO_2 [7.9].

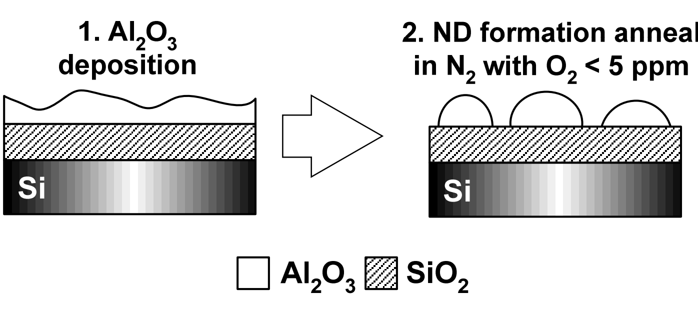
Al_2O_3 is known to have deep trap levels and a high trap density among various high-K materials [7.2, 7.8], indicating possibility of long retention and large memory window. That is, Al_2O_3 can be an ideal trapping layer material for SONOS-type nonvolatile memory devices. However, there is no report of formation

of Al_2O_3 dots on SiO_2 and say nothing of fabrication of Al_2O_3 dots memory with CMOS compatible process. In this chapter, we introduce a novel method to assemble high density Al_2O_3 NDs on SiO_2 using a two-step controlled anneal technique. Based on this technique, we propose a novel memory structure, which combines the advantages of both the NCs and SONOS-type memory structures.

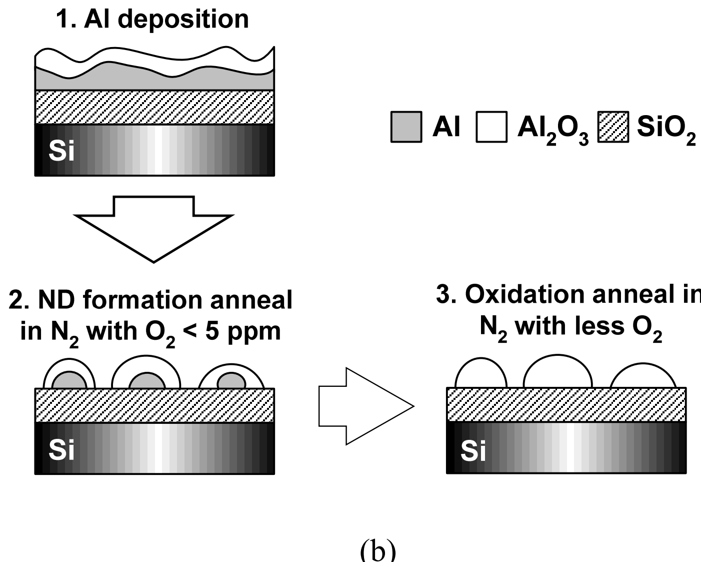
7.2 Process Development of Self-Assembly of Al_2O_3 Nano-Dots on SiO_2

7.2.1 Experimental details

In the study of formation of Al_2O_3 dots on SiO_2, all samples were prepared using *p*-type Si (100) wafers. Bottom SiO_2 were prepared by rapid thermal oxidization at 1000 ^oC. Al and Al_2O_3 thin films were deposited using sputtering in pure Ar ambient or Ar/O_2 ambient. Anneals were performed in a rapid thermal anneal chamber. In Fig. 7.2, two proposed approaches to form Al_2O_3 NDs were illustrated.



(a)



(b)

Fig. 7.2 Illustration of two proposed processes for assembling Al_2O_3 NDs on SiO_2. (a) deposition of thin Al_2O_3 films followed by anneal and (b) deposition of thin Al film followed by anneal and oxidation.

7.2.2 Results and Discussions

A. Formation of Al_2O_3 NDs using proposed process 1

In proposed process 1 (Fig. 7.2 (a)), after a 4.5 nm SiO_2 layer was grown in a pure O_2 ambient at 1000°C, an Al_2O_3 film of 3 nm thickness (as determined by the deposition rate and time) was deposited by sputtering (Step 1: Deposition). Then anneals at 600 °C and 1000 °C for 30 s in a N_2 ambient (O_2 < 5 ppm) was carried out to form Al_2O_3 NDs (Step 2: ND Formation Anneal). After anneal, the surface of the films were analyzed by AFM, the AFM image of the surface of as deposited Al_2O_3 film is also shown as a reference as shown in Fig. 7.3.

It can be found that no dot-shaped topography can be found after anneal at 600 °C and 1000 °C. Anneal at higher temperature is not normal condition for CMOS process. Hence, the proposed process 1 is not feasible. This could because

the melting temperature of Al_2O_3 (2072 ^oC) is much higher than that of Al (660 ^oC) [7.11], resulting in less fluidity. This result also implies that the stress of as deposited Al_2O_3 on SiO_2 is quite low. So-called Stranski-Krastanow (SK) growth, *i. e.* deposition → stress relaxation → island formation, can occur.

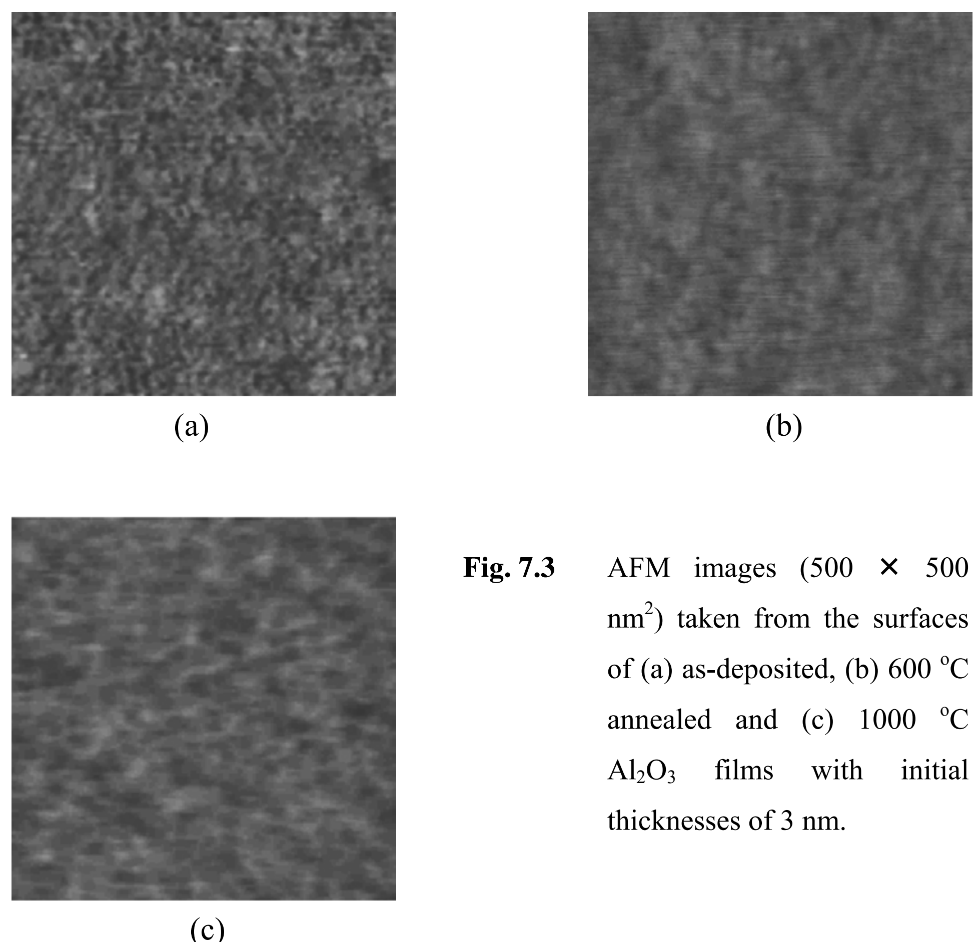


Fig. 7.3 AFM images (500 × 500 nm^2) taken from the surfaces of (a) as-deposited, (b) 600 ^oC annealed and (c) 1000 ^oC Al_2O_3 films with initial thicknesses of 3 nm.

B. Formation of Al_2O_3 NDs using proposed process 2

In proposed process 2, after a 4.5 nm SiO_2 layer was grown in a pure O_2 ambient at 1000^oC, an Al film of 2 nm thickness (as determined by the deposition rate and time) was deposited by sputtering (Step 1: Deposition). Then an anneal at 600 ^oC for 30 s in a N_2 ambient (O_2 < 5 ppm) was carried out to form Al NDs (Step 2: ND Formation Anneal). This is followed by another anneal at 600 ^oC for 30 s in a

N_2 ambient with 5000 ppm O_2 to oxidize the Al NDs to Al_2O_3 NDs (Step 3: Oxidation Anneal). The surface of the films after each step in Fig. 7.2 (b) were analyzed by AFM, as shown in Fig. 7.4.

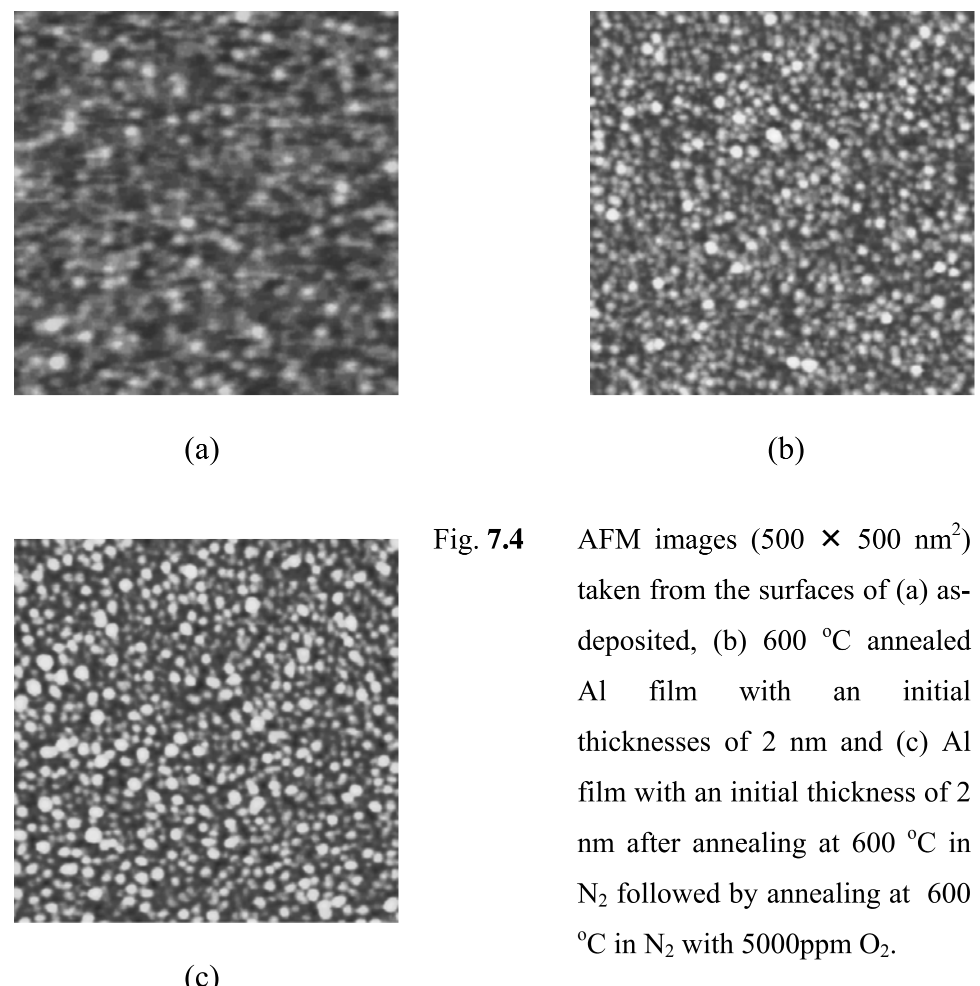


Fig. **7.4** AFM images (500 × 500 nm^2) taken from the surfaces of (a) as-deposited, (b) 600 °C annealed Al film with an initial thicknesses of 2 nm and (c) Al film with an initial thickness of 2 nm after annealing at 600 °C in N_2 followed by annealing at 600 °C in N_2 with 5000ppm O_2.

The AFM images show that the as-deposited Al film was inherently non-uniform (Fig. 7.4 (a)). Dot-shaped topography was observed only after the ND formation anneal (Fig. 7.4 (b)) and this topography remained almost unchanged after the oxidation anneal (Fig. 7.4 (c)). This means that NDs were formed by the ND formation anneal, and the size and density were determined by the same annealing step as well. This is similar to the formation of inert metal nano-crystals on SiO_2 in which stress relaxation of a deposited film by subsequent annealing results in

rupture of the film to end up as islands [7.5]. According to the AFM image after Step 3, a dot (defined by the height > 1nm) density of at least $5\times10^{11}/cm^2$ is obtained.

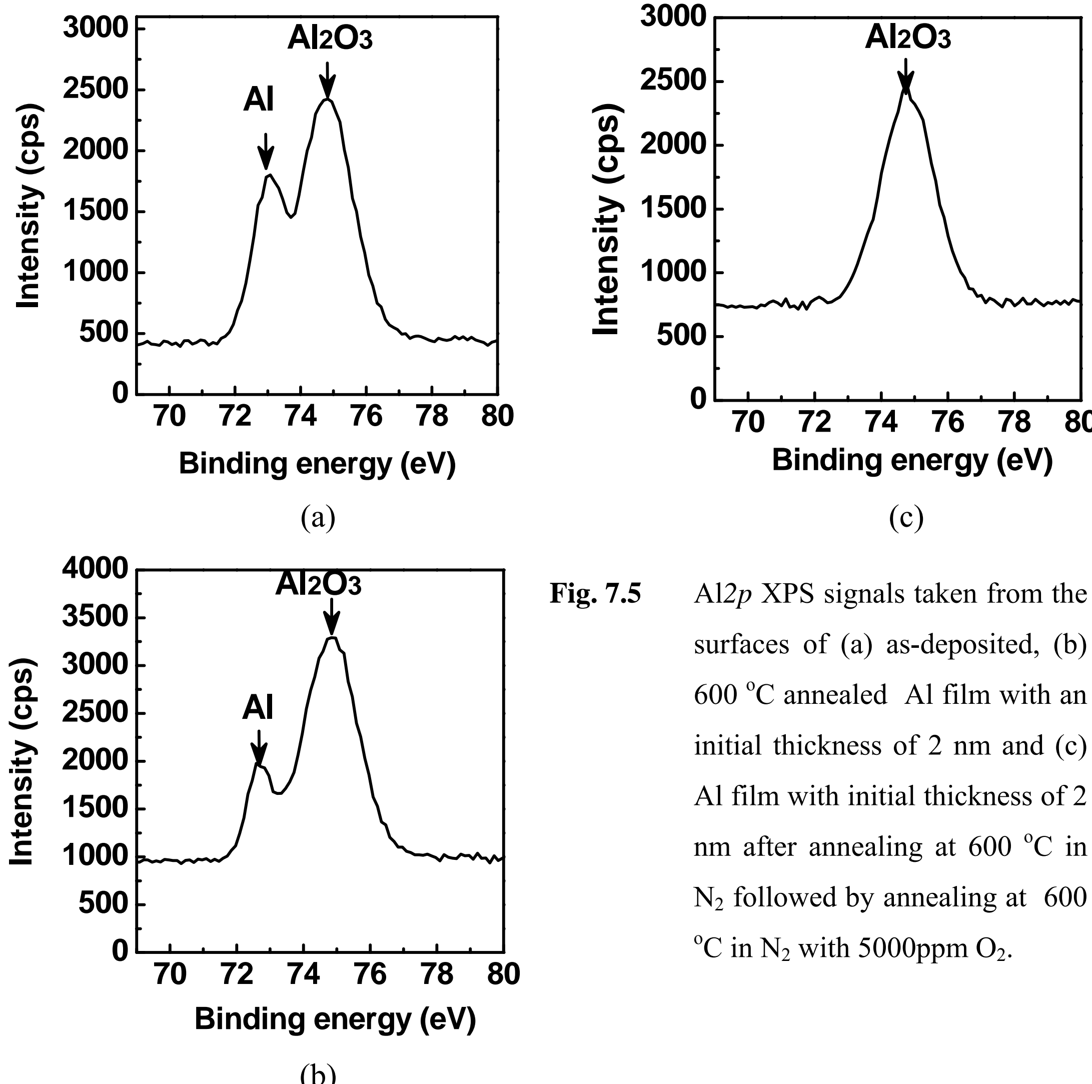


Fig. 7.5 Al2*p* XPS signals taken from the surfaces of (a) as-deposited, (b) 600 ^{o}C annealed Al film with an initial thickness of 2 nm and (c) Al film with initial thickness of 2 nm after annealing at 600 ^{o}C in N_2 followed by annealing at 600 ^{o}C in N_2 with 5000ppm O_2.

The XPS analysis of the films after each step in Fig. 7.2 (b) was shown in Fig. 7.5. It can be found that the initial film of Step 1 contains Al and Al_2O_3 (Fig. 7.5 (a)). This is because the surface of the Al film can be easily oxidized by O_2 present in the atmosphere. Nevertheless, the film still can conglomerate during the ND formation anneal because of the underlying Al layer. The XPS analysis after Step 2 shows that the pure Al phase is still detected (Fig. 7.5 (b)), hence another anneal

with O_2 is performed. The XPS result after Step 3 shows that Al NDs are fully oxidized to Al_2O_3 NDs at 600°C (Fig. 7.5 (c)), indicating that 5000 ppm O_2 in N_2 is sufficient for the oxidation of NDs.

A cross-sectional TEM image on a SONOS-type device with Al_2O_3 NDs of 5-10 nm that is obtained using this controlled two-step annealing method is shown in Fig. 7.6. The TEM and XPS results confirm the formation of Al_2O_3 NDs. At the same time, TEM image shows that there is no further growth of the tunneling oxide in the condition of 5000 ppm O_2 used. Due to the much smaller O_2 partial pressure compared with pure O_2, no measurable increase in the thickness of SiO_2 underlayer (4.5 nm) is observed [7.10] and this enhances feasibility of the process integration.

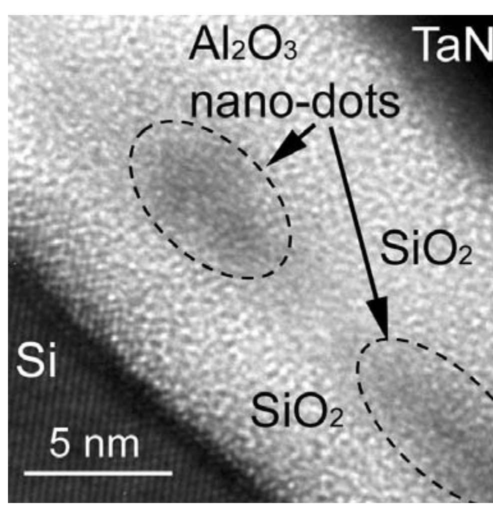


Fig. 7.6 TEM image of Al_2O_3 NDs formed in a memory gate stack of TaN gate/SiO_2/Al_2O_3 NDs /SiO_2/Si using proposed process 1.

C. Control of the size and density of NDs

We found that oxidation level of the Al film, initial Al film thickness and ND formation annealing temperature are very important for the size and density

control of Al_2O_3 NDs. Figure 7.7 summarizes the AFM images associated with these effects.

Initial film	**1 nm Al**	**2 nm Al**	**6 nm Al**
As deposited			
After ND formation anneal at 600 °C			
After ND formation anneal at 700 °C	5.0 (nm) 2.5 0 **Grayscale**		

Fig. 7.7 Comparison of AFM images (500 × 500 nm^2) taken from the surfaces of as-deposited and annealed Al films with initial thicknesses of 1 nm, 2 nm and 6 nm. The ND formation anneals were carried out at 600 °C and 700 °C for 30 s in N_2 ambient with O_2 less than 5 ppm.

It can be found, that if the initial Al film thickness is thin at ~ 1 nm, NDs cannot be formed by the subsequent *ex-situ* anneal. This is probably because the film has been fully oxidized after exposing to the atmosphere. Once the film becomes oxidized, as shown in Fig. 7.3, self-agglomeration is less favorable because of the high melting temperature of Al_2O_3 and small stress of Al_2O_3 on SiO_2 [11].

From Fig. 7.7, it can be also found that thicker initial Al film results in larger NDs. After a systematic comparison, it was found that a 2 nm thick Al film was likely to satisfy the requirement of assembling Al_2O_3 NDs with high area density using the two-step annealing method. An anneal at 700^oC was also carried out for 2 nm and 6 nm thick Al films. The results show that the higher temperature of the ND formation anneal tends to result in the increase of ND size but the decrease of ND density, especially for the thin Al films.

7.3 Fabrication of Nonvolatile Flash Memory Device using Al_2O_3 High-K Nano-Dots Embedded in SiO_2 and Electrical Characterization

7.3.1 Device fabrication

To investigate the effects of Al_2O_3 NDs on the electrical properties of the nonvolatile memories, test devices with Al_2O_3 NDs and control devices with trappy Al_2O_3 continuous layer (CL) were fabricated.

The process flow for device fabrication is shown in Fig. 7.8. Devices with Al_2O_3 NDs and Al_2O_3 CL were fabricated to compare the difference in the topography of the trapping layer. Except for the trapping layer, all the other details of the device structures were the same. After pre-gate cleaning, a 4.5 nm SiO_2 (by rapid thermal oxidization at 1000 ^oC) was used as a tunneling oxide. For the CL device, 3 nm thick Al_2O_3 was deposited by reactive sputtering. For the ND devices, a 2 nm Al film was first deposited on the tunneling SiO_2 by sputtering, then annealed at 600 ^oC for 30 s in N_2 ($O_2 < 5$ppm) to form Al NDs, and followed by a second anneal at 600 ^oC for 30 s in N_2 with 5000 ppm O_2 to oxidize Al NDs to

Al_2O_3 NDs. By employing this process with the above optimized parameters, a dot density of at least $5\times10^{11}/cm^2$ with a size range of 5-10 nm was obtained by an AFM analysis. After the formation of trapping layer, a 7 nm SiO_2 (deposited using TEOS at 675 ^oC) was used as a blocking oxide, and a 150 nm TaN (by reactive sputtering) was used as a gate electrode. TaN gate has been reported to reduce the *F-N* tunneling current through the blocking oxide during erase operation in comparison with n^+ poly-Si gate due to the work function difference [7.13].

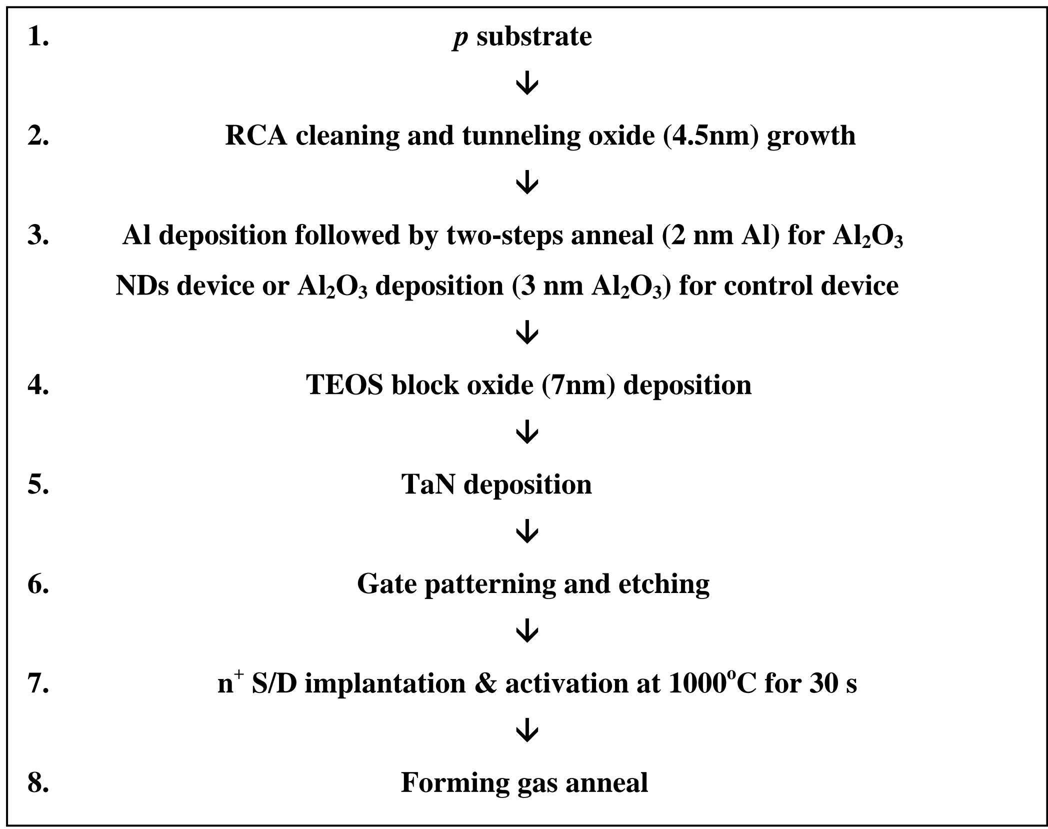


Fig. 7.8 Process flow of the devices fabricated

After gate patterning, source/drain regions were formed by an As^+ implantation followed by activation anneal at 1000 ^oC for 30 s. A forming gas anneal at 420 ^oC was finally performed to improve the quality of SiO_2/Si substrate interface.

In Fig. 7.9, TEM images of the gate stacks and illustrations of the Al_2O_3 ND and CL devices were shown.

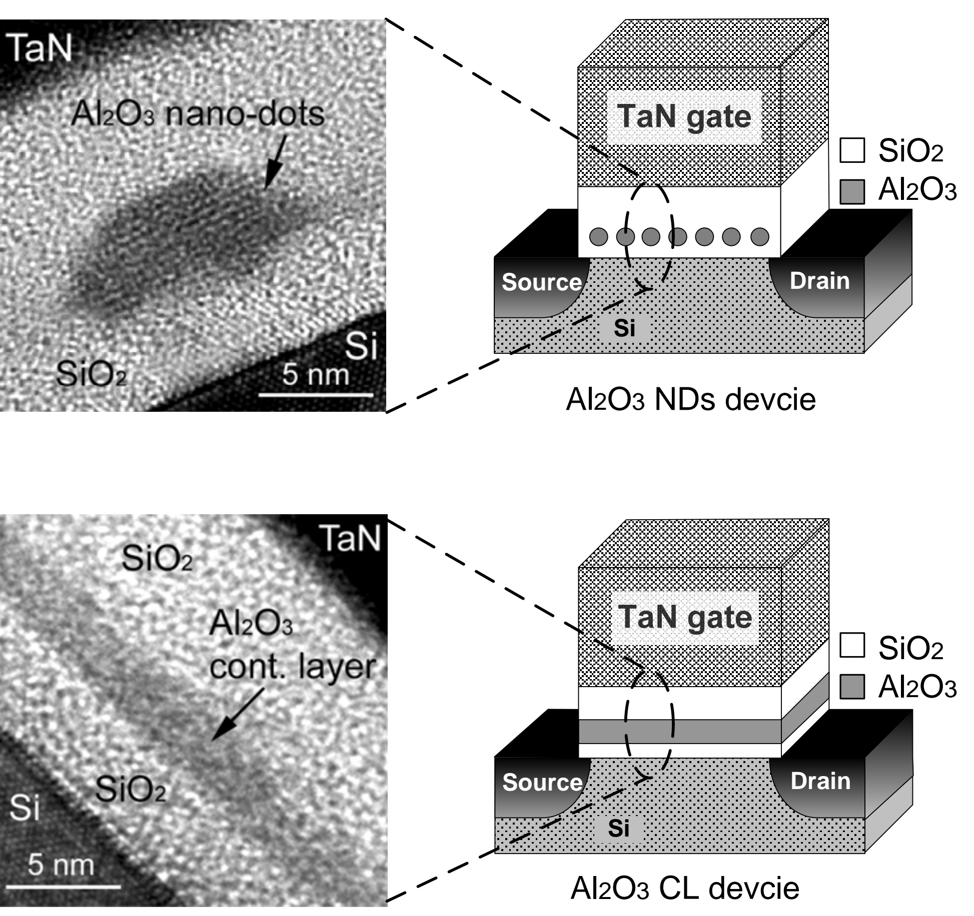


Fig. 7.9 TEM images and illustrations of the Al_2O_3 NDs and CL devices.

It can be found that the SiO_2 thicknesses are the same in both types of devices. According to the density and molar mass of Al_2O_3 and Al [7.12], the volume expansion is in the range of 28% to 45%, when Al is oxidized to form Al_2O_3. Therefore, we can expect that the final Al_2O_3 volume in both the CL and NDs devices is similar.

7.3.2 Electrical characterization and discussion

A. Programming and erasing

Programming and erasing (P/E) efficiencies of the NDs and CL devices are shown in Figs. 7.10 (a) and (b), respectively.

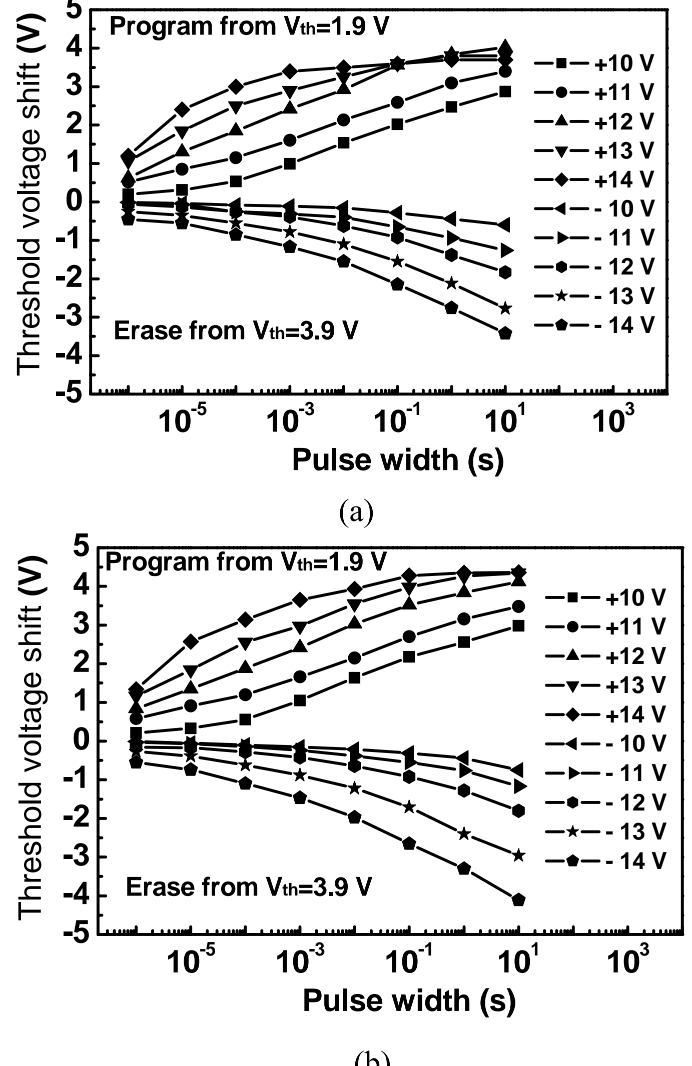


Fig. 7.10
Program and erase characteristics of the (a) Al_2O_3 NDs device and the (b) Al_2O_3 CL device. In programming operation, the source, drain and substrate are grounded, and a programming voltage is applied on the gate. In the erase operation, the source and drain are floating, the substrate is grounded, and an erasing voltage is applied on the gate.

Assuming that the trap density in bulk Al_2O_3 is the same for both devices and that interface trap density is negligible, the theoretical programming speed of the NDs device should be lower than that of the CL device because of the lower trapping layer coverage, resulting in lower capture efficiency of the tunneling

electrons. However, no significant degradation in programming efficiency of NDs device is observed in the fast programming (< 100 μs) region.

According to the calculation of volumes of Al atom ($26.98 gmol^{-1}$ / $2.7 gcm^{-3}$ / $6.02x10^{23}$ atoms/mol = $1.66x10^{-23} cm^3$/atom) and Al_2O_3 molecule ($101.96 gmol^{-1}$ / $3.50 \sim 3.97 gcm^{-3}$ / $6.02x10^{23}$ molecules/mol = $4.27 \sim 4.83x10^{-23} cm^3$/molecule), volume expansion when 2Al is converted to Al_2O_3 is in the range of 28% to 45%. Therefore, we can expect that the final Al_2O_3 volume in both the devices is similar.

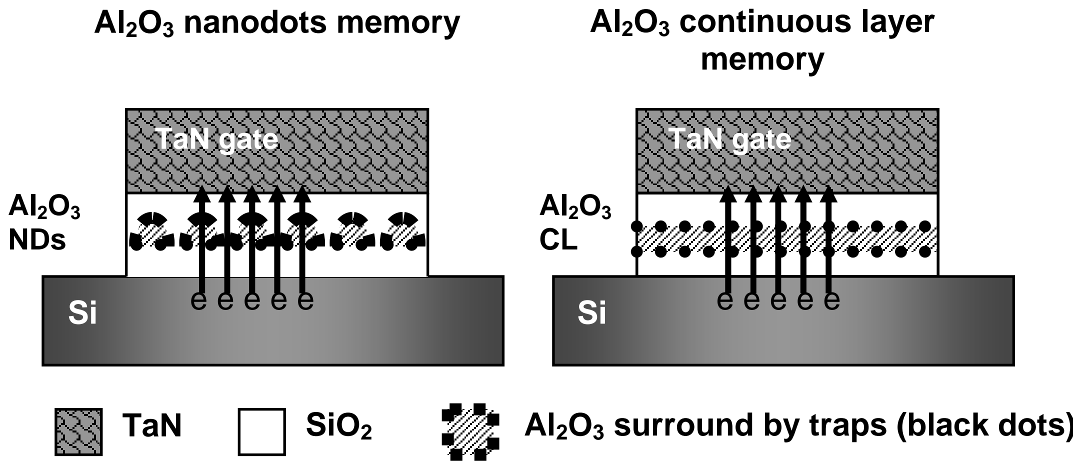


Fig. 7.11 Illustrations of the Al_2O_3 NDs and CL devices.

The same trapping materials volume could be the reason of the same programming speed. This is because when the total volume of trapping materials for both the devices are the same, dots structure has additional interfacial area from the sidewall, generating more interface traps. This can be observed by the Fig. 7.9 that the height of the dots is larger than the thickness of the continuous layer. At the same time, thicker dots can improve the capture efficiency of the electrons, as shown in Fig. 7.11.

In fast programming (less than 10^{-5} s) region, considering the equivalent oxide thickness of each layer, when programming voltage is smaller than ~11 V, the programming mechanism should be direct tunneling and when programming voltage is larger than ~12 V, the programming mechanism should be *F-N* tunneling. This can be also observed in the Fig. 7.10 (a) and (b), that when programming voltage is larger than 12 V, the programming speed increases very fast.

The erase mechanism should be hole injection from channel to the trapping layer. The reason is that erasure speed is much slower than programming speed and trap levels of electron in Al_2O_3 are very deep [7.2]. Considering the tunneling oxide thickness is 4.5 nm, low erasure speed is reasonable. Hole tunneling current is much smaller than that of electron tunneling current. At the same time, as the stored electrons are in deep trap energy level, they are difficult to erase. This is the reason why SONOS type memory using Al_2O_3 trapping layer has very good retention [7.2].

The natural threshold voltages before programming and erasing are V_{th} = 1.9V. This high threshold voltage should be mainly due to the negative charge in Al_2O_3 [7.12]. The fully erased V_{th} is slightly lower than natural V_{th}, as shown in Fig. 7.10, but in common erase time of flash memory (within 10^{-3} s), erase voltage of 14 V can not fully erase all charges if device is fully programmed. This could be due to the deep trap level and band structure of Al_2O_3 [7.13].

B. Charge retention

In Fig 7.12, charge retention characteristics of the Al_2O_3 NDs and CL devices at 24 ^{o}C K and 150 ^{o}C are compared. At 297 K, the electron loss rate of the NDs device is much lower than that of the CL device. Since the materials and

vertical structure of both the devices are the same, this difference must originate from the difference in the lateral dimension. As the conduction band edges of Al_2O_3 and SiO_2 are at about the same level [7.14], their abilities in suppressing electron lateral migration via DT are similar [7.15]; whereas the NDs device is effective in suppressing electron lateral migration via *F-P* tunneling because SiO_2 contains much fewer traps than Al_2O_3. Hence, it is plausible that the reduced F-P tunneling probability results in the better retention of the NDs device. This is supported by the larger difference in charge retention properties of the two types of devices at higher temperature, *e.g.* 150 °C [7.16], as shown in Fig. 7.12.

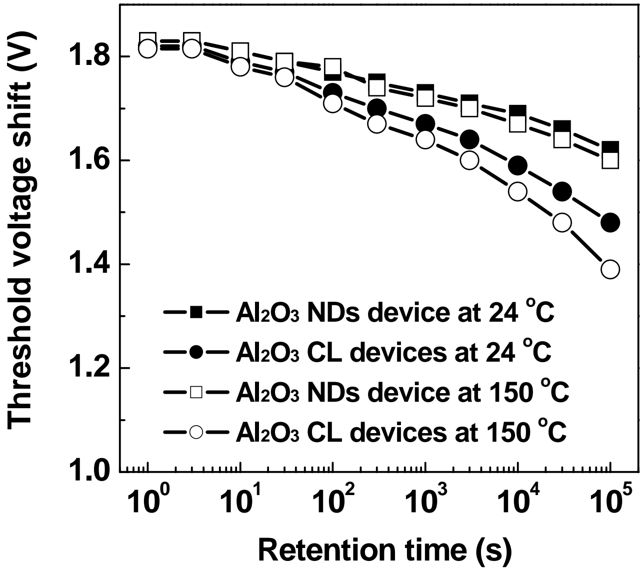


Fig. 7.12 Comparison of data retention (programmed state) between the devices using Al_2O_3 NDs and Al_2O_3 CL at 24 °C and 150 °C.

C. Endurance

The endurance results shown in Fig. 7.13. It can be found that the endurance of Al_2O_3 and CL NDs device are almost the same. This could be because the

accumulation of fixed charge are the same because of the same tunneling oxide, block oxide and volume of Al_2O_3 in for both devices.

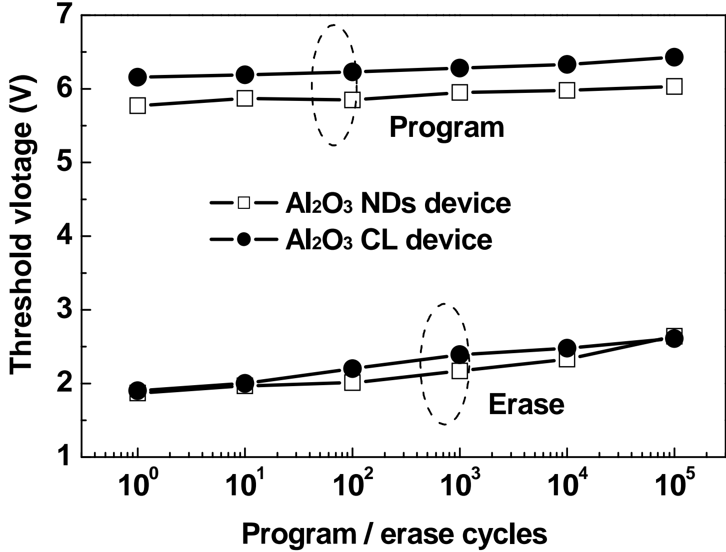


Fig. 7.13 Comparison of endurance characteristics of devices using Al_2O_3 NDs and CL (P/E cycle: 12 V, 10μs program and -14 V, 1 ms erase)

D. Feasibility of multi-level storage

Leveraging on good retention properties demonstrated by the NDs device, we explored its application in multi-level storage. In Fig. 7.14, we demonstrate multi-level storage operation of the NDs and CL devices at room temperature. The erased state near the fresh state is defined as state “11”, and pulses of 11 V for 10 μs, 12 V for 10 μs and 12 V for 100 μs are used to write the memory states of “10”, “01” and “00”, respectively. From the extrapolation of the retention property as shown in Fig. 7.14, the NDs device can achieve 2-bits (four levels) storage with an expected retention time of 10 years if a proper sensing range is provided, because V_{th} of each state is maintained without overlapping with neighboring states.

Meanwhile, in the CL device, the state ("00") merges into the neighboring state ("01") after 10 years, resulting in a memory error.

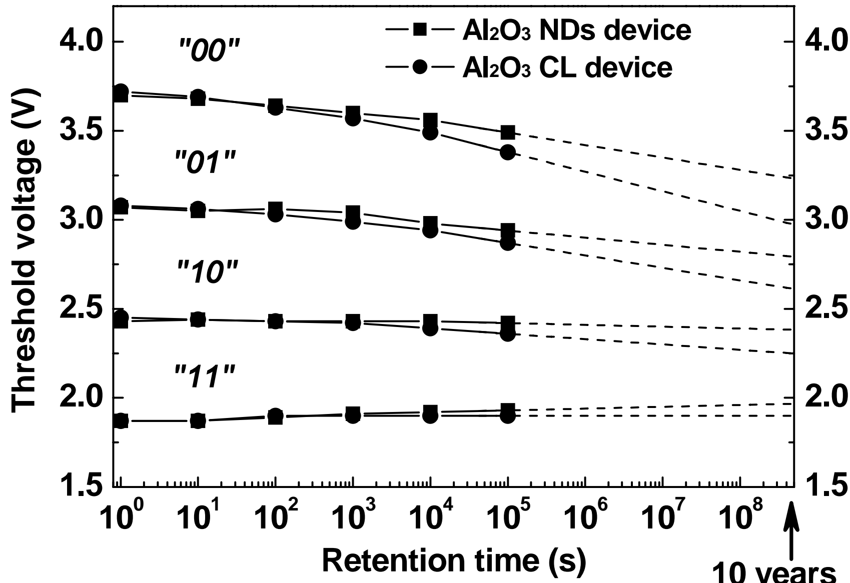


Fig. 7.14 Demonstration of multi-level storage and retention property from the devices with Al_2O_3 NDs and Al_2O_3 CL at room temperature.

7.4 Summary

In conclusion, a two-step controlled anneal process for assembling Al_2O_3 NDs on SiO_2 was demonstrated. It was found that, the size and density of NDs depend on the initial Al film thickness and the annealing temperature, and furthermore the formation of Al_2O_3 NDs strongly depends on the amount of O_2 introduced. Proposed approach is CMOS compatible and the process parameters were optimized to obtain high density sub-10 nm Al_2O_3 NDs on SiO_2.

Novel nonvolatile flash memory devices using Al_2O_3 NDs as charge storage nodes was proposed and fabricated. The Al_2O_3 NDs structure suppresses lateral migration of electrons via *F-P* tunneling that adversely affects retention in Al_2O_3 CL device, thereby improving the retention characteristics. The Al_2O_3 NDs structure has been demonstrated to be a good trapping layer for reliable flash memories and multi-level storage application.

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Chapter 8

Conclusions and Suggestions for Future Work

8.1 Conclusions

In this thesis, the formation of advanced gate stacks of logic CMOS devices and nonvolatile flash memory devices was studied. In the formation of advanced gate stacks of logic CMOS devices, several topics related to process integration, including the wet etching mechanisms of Hf based high-K dielectrics, the effects of annealing on wet etching properties of Hf based high-K dielectrics, the effects of plasma treatment on removal properties of crystallized HfO_2 films, the plasma etching properties of Hf based high-K dielectrics and the formation of advanced poly-SiGe/HfO_2 gate stack using ICP were studied and discussed. In the part of formation of advanced gate stacks of nonvolatile flash memory devices, two novel memory structures and process approaches of Ge NCs embedded in HfAlO high-K dielectric and Al_2O_3 NDs embedded in SiO_2 were introduced and fabricated. The main focuses are on the scientific mechanisms.

With the finding of the scientific mechanisms, several novel CMOS compatible processes and approaches have been developed for the future VLSI application.

8.1.1 Wet etching mechanisms of Hf based high-K dielectrics and effects of annealing

In this work, wet etching properties of Hf based high-K dielectrics including HfO_2, $(HfO_2)_x(Al_2O_3)_{1-x}$, Hf oxynitride and Hf silicate were investigated. Various chemicals for conventional CMOS process were used. Etching mechanisms of Hf and each Hf based high-K dielectric in aqueous HF were explored. Effects of anneal on the microstructure of the films were studied using AFM, TEM and XPS. Major findings are shown as follows:

1. Fluorides species such as F^-, HF_2^- HF and H_2F_2 are very effective for dissolving Hf and HfO_2 using acids.

2. The solubility of Hf increases at lower pH and HfF_4 is highly soluble in HF solution with a solubility of 1.4E-6mol/l, which is much higher than calculated results.

3. It was observed that the etch rates of Hf and HfO_2 increase with higher HF concentration.

4. After HF etching, Hf and HfO_2 surfaces are terminated with F atoms.

5. After anneal, the crystalline phase of HfO_2 is always the main reason for the low etch rate of Hf based high-K materials in HF.

6. Etching of Hf based high-K dielectrics always occurs through the weak points in the films including amorphous HfO_2, Hf-N, Al-O and Si-O bonds.

8.1.2 Effects of annealing effects of N_2, O_2 and Ar Plasma treatment on removal of crystallized HfO_2 Film

In this work, two novel removal processes, DHF etching of crystallized HfO_2 films enhanced by plasma treatments using N_2 or Ar, were developed. Also, effects of plasma treatment using Ar, N_2 and O_2 to enhance wet removal rate of crystallized HfO_2, SiO_2 and Si were studied using the XPS analysis and the Monte-Carlo simulation on ion injection. Major findings are shown as follows:

1. The mechanism responsible for the enhancement of etch rate of crystallized HfO_2 using Ar plasma treatment is the formation of HF dissoluble species including metallic HfO_x and amorphous HfO_2.

2. The mechanism responsible for the enhancement of etch rate of crystallized HfO_2 using N_2 plasma treatment is the formation of HF dissoluble species including metallic HfO_x, amorphous HfO_2 and Hf-N bonds.

3. The mechanism responsible for the enhancement of etch rate of crystallized HfO_2 using O_2 plasma treatment is the formation of HF dissoluble species including metallic HfO_x, amorphous HfO_2 and disturbed crystallized HfO_2 resulted from the oxidation of Si substrate.

4. Among the plasmas studied in this work, N_2 plasma treatment is the most effective to enhance the etch rate of crystallized HfO_2 in HF solution and to minimize recess in the substrate structure because of the largest injection depth in HfO_2, the formation of highly HF dissoluble Hf-N

bonds and the small injection depth of N ions in Si nitrides formed by N_2 plasma treatment.

5. O_2 plasma treatment induces a large recess in the Si substrate due to the oxidation effect.

8.1.3 Inductively coupled plasmas etching properties of Hf based high-K dielectrics

In this work, etching properties of Hf based high-K dielectrics were investigated using ICP. XPS and TOF-SIMS were used to identify the chemical composition of etch by products of Hf based high-K dielectrics in $Cl_2/HBr/C_xF_y/O_2$ plasmas. Major finding are shown as follows:

1. Plasma etching of HfON, HfAlO, and HfSiO is strongly dependent on etching properties of each phase in the makeup of the films, *e.g.* HfO_2, HfN, Al_2O_3, and $HfSiO_4$.

2. Conventional $HBr/Cl_2/O_2$ based plasma gate etching recipes using ICP for poly-Si/SiO_2 gate stack etching can also be applied to the etching of poly-Si / Hf based dielectric gate stacks because of ion sputtering dependent etching properties of Hf based high-K dielectrics.

3. In the low pressure ICP etching of Hf based dielectrics using HBr or Cl_2 plasmas, the amount of non-volatile residues is small, and high temperature post-treatment helps to further reduce the amount of residues.

4. Fluorine containing plasmas are undesirable for etching of Hf based

high-K films because of the generation of a significantly large amount of non-volatile residues, compared to the plasmas containing bromine or chlorine.

5. The chemical composition of main residues has been identified using TOF-SIMS.

8.1.4 Formation of poly-SiGe/HfO_2 gate stack using inductively coupled plasma

In this work, the formation of a novel poly-SiGe/HfO_2 gate stack using ICP was studied. We have also demonstrated the formation of controlled notches from the poly-SiGe sidewall as a step towards the development of short channel devices with a technology node smaller than 65nm, with the help of the high selectivity plasma etching of poly-SiGe to HfO_2. Major findings are shown as follows:

1. Etch rate of poly-SiGe increases with increasing Ge concentration, inductive power, or RF bias power but reducing pressure, in HBr/O_2 plasmas.

2. Etching of HfO_2 was strongly dependent on the sputtering by ion bombardment.

3. Notching of poly-SiGe gate can be controlled by varying the etching process parameters of inductive power, rf bias power, and pressure, as well as by varying the Ge concentration in poly-SiGe.

4. Notching became more pronounced in the conditions where ion energy is reduced.

5. Etching selectivity of poly-SiGe to HfO_2 can be increased by reducing RF bias power in the presence of a small amount of O in HBr plasma or increasing pressure.

6. Optical emission by monitoring Si and Ge etch by products can provide sharp and obvious endpoint signals.

8.1.5 Formation of novel gate stack of nonvolatile flash memory device using Ge nanocrystals embedded in HfAlO High-K dielectric

In this work, Ge-NCs were successfully formed in HfAlO high-K dielectric using a phase separation approach with industry compatible CMOS process. We fabricated a nonvolatile flash memory device using Ge NCs FG embedded in HfAlO high-K tunneling/control oxides and TaN metal gate. Major findings are shown as follows:

1. Ge-NCs can form in HfAlO via phase separation.

2. Ge-NCs have good thermal stability up to ~1000 ^{o}C in the HfAlO matrix as indicated by the negative Gibbs free energy changes for both reactions of $GeO_2 + Hf \rightarrow HfO_2 + Ge$ and $3GeO_2 + 4Al \rightarrow 2Al_2O_3 + 3Ge$.

3. Compared with Si-NCs embedded in HfO_2, Ge-NCs embedded in HfAlO can provide more electron traps, thereby enlarging the memory window.

4. By using the high-K tunneling and control oxide, memory device fabricated can achieve low programming voltage of 6 - 7 V for fast programming, long charge retention time of 10 years maintaining a 0.7 V memory window, and good endurance characteristics of up to 10^6 rewrite cycles.

8.1.6 Formation of novel memory gate stack using Al_2O_3 nanodots embedded in SiO_2

In this work, Al_2O_3 NDs were formed on SiO_2 using a two-step control anneal process. Proposed approach is CMOS compatible and the process parameters have been optimized to obtain high density sub-10 nm Al_2O_3 NDs on SiO_2. Novel nonvolatile flash memory devices using Al_2O_3 NDs as charge storage nodes were proposed and fabricated. Major findings are shown as follows:

1. The size and density of Al_2O_3 NDs depend on the initial Al film thickness and the temperature in the first anneal.

2. Formation of Al NDs strongly depends on the amount of O_2 introduced. More O_2 hinders the formation of the dots.

3. The Al_2O_3 NDs structure suppresses lateral migration of electrons via F-P tunneling, thereby improves the retention properties.

8.2 Suggestions for Future Work

8.2.1 Improvement of removal process of Hf based high-K dielectrics

Although in chapter 3, we have developed two novel removal process of Hf based high-K dielectrics based on the understanding of etch mechanisms of Hf based high-K dielectrics addressed in chapter 2, the overall selectivity of high-K to Si in these processes is lower than that in DHF etching of SiO_2 on Si. Hence this work needs to be explored further. The low selectivity is mainly originated from the low selectivity of plasma treatment. Recently, BCl_3 has been reported to achieve a good selectivity although boron contamination brings about a new challenge [8.1, 8.2]. Hence, more suitable plasma chemistries are expected to improve this process.

However, it is not such an easy task to add a new gas to a well established process line, especially for a toxic gas. Hence, I suggest that once process line can be extended and more gas lines are allowed, we can consider to install new gases, such as BCl_3 to improve high-K removal process.

8.2.2 Study of plasma etching mechanism of new metal gate materials and formation of metal silicides gate

During my Ph. D study, I have also attempted to studied plasma etching properties of some metal nitrides metal gate materials including TaN, TiN and HfN, although it seems that they have not been fully developed for CMOS devices yet.

Results show their etching properties of them are very different with poly-Si or poly-SiGe. It is difficult to improve the etching selectivity of metal gate to HfO_2 by conventional approaches, *i.e.* increasing process pressure and adding small amount O_2. Of course, it may be not an issue at this moment, since the right candidates of metal gate have not been identified clearly.. However, the needs for metal gate are very pressing because of the aggressive scaling of CMOS device [8.3]. Hence the plasma etching process should be developed urgently to meet the requirement of the materials to be used in the near future. At the same time, the etching mechanisms need to be investigated to guide process development and solve the problem in process.

In the case that fully silicided/germanided metal gate is used, plasma etching poly-Si, poly-Ge or poly-SiGe needs to be elaborately developed for sub-45 nm technology node based on the mechanisms explored in this work.

8.2.3 Development of application specific nanocrystals or nanodots flash memories.

Most recently, gate length of the NAND flash memory devices has been scaled down to sub 65 nm [8.4]. With gate length shorter than this dimension, one flash memory cell can contain only a limited numbers of NCs or NDs, *e. g.* several tens. This will result in nonuniform and instable electrical characteristic of flash memory arrays. If the size and density distribution of NCs/NDs cannot be well

controlled, conventional NAND flash memories are expected to dominate the high density flash memory application over NCs/NDs.

However, in some specific areas, *i. e.*, aero space and geological monitoring, where low power consumption, anti radiation and high reliability are required. NCs or NDs flash memory could be the suitable candidates. Hence, development of application specific NCs/NDs flash memory could be promising direction.

8.2.4 High-K dielectrics as interpoly/block oxide of flash memory devices

Although the trapping and mobility degradation issues have not been solved, high-K dielectrics as interpoly oxide of FG flash memory and block oxide of SONOS type flash memory have drawn significant attention [8.5-8.8]. This is because interpoly/block oxide is very thick and it does not affect the carrier mobility in the channel.

Therefore, the development of the novel structures using high-K oxide to replace oxide-nitride-oxide interpoly oxide for FG flash memory and SiO_2 block oxide for SONOS type flash memory, respectively could be very important and promising. However, how to deal with the trapping effects of interpoly oxide is a very challenging work as most of high-K dielectrics are very trappy.

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Appendix

List of Publications Resulting from This Thesis

A. *Journal Publications*

1. **J. H. Chen**, W. J. Yoo, D. S. H. Chan and L.-J. Tang "Self-Assembly of Al_2O_3 Dielectric Nano-Dots on SiO_2 Using Two Step Controlled Annealing Technique for Long Retention Nonvolatile Memories," *Applied Physics Letters*, vol. 86, Feb, 2005.

2. **J. H. Chen**, Y. Q. Wang, W. J. Yoo, Y.-C. Yeo, G. Samudra, D. S. H. Chan, and D.-L. Kwong, "Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High-K Tunneling and Control Oxides: Device Fabrication and Electrical Performance," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp1840-1848, Nov. 2004.

3. **J. Chen**, W. J. Yoo, Z. Y. L Tan, Y. Wang, and D. S. H Chan, "Investigation of Etching Properties of HfO Based High-K Dielectrics Using Inductively Coupled Plasma" *Journal of Vacuum Science and Technology A*, vol. 22, pp1552-1558, 2004.

4. **J. Chen**, W. J. Yoo, D. S. H. Chan and D.-L. Kwong, "Effects of Annealing and Ar Ion Bombardment on the Removal of HfO_2 Gate Dielectric". *Electrochemical and Solid State Letters*. vol. 7, pp18-20, 2004.

5. **J. Chen**, K. M. Tan, N. Wu, W. J. Yoo, and D. S. H. Chan, "Formation of Poly-SiGe / HfO_2 Gate Stack Structure Using Inductively Coupled Plasma Etching". *Journal of Vacuum Science and Technology A*, vol. 21, pp1210-1217, 2003.

6. **J. H. Chen**, W. J. Yoo, D. S. H. Chan and L.-J. Tang "Self-Assembly of Al_2O_3 Dielectric Nano-Dots on SiO_2 Using Two Step Controlled Annealing Technique for Long Retention Nonvolatile Memories," *Journal of Nanoscale Science & Technology*, vol. 11, pp4-6, Feb, 2005.

7. **J. Chen,** W. Y. Yoo, D. S. H. Chan, "Effects of N_2, O_2 and Ar Plasma Treatment on Removal of Crystallized HfO_2 Film", *Journal of Vacuum Science and Technology A,* vol. 24, pp133-138, 2006.

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C. Patent

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