

**ANALYSIS OF COLUMN INTERCONNECTS FOR  
WAFER LEVEL PACKAGES**

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## Summary

Copper column (CuC) interconnect is proposed in the Nano Wafer Level Packaging (NWL) program as a candidate chip-to-substrate interconnect solution and is the focus of investigation in this thesis.

In this thesis, a literature survey on fatigue life correlation models and two important tasks are completed. The two important tasks are:

First, a simulation-based design optimization process is established based on our available software resources, ABAQUS and Minitab. This process integrates finite element analysis (FEA), design of experiment (DoE) technique and numerical optimization, generating a systematic and efficient method that can be used to study the effects of various design parameters on desired system response. The significance of this simulation-based design optimization process lies in its general applicability in various design scenarios where effect of each design parameter on the system response is of interest, investigation of interaction of design parameters is needed and an optimal design parameter setting is required. After the establishment of this optimization process, a case study on CuC interconnect in wafer level packages is detailed. It is found that the substrate coefficient of thermal expansion (CTE) has the largest influence on solder joint fatigue reliability. The chip thickness has the second largest influence with a smaller chip thickness leading to better solder joint reliability. The substrate thickness plays the third

most important role with a thinner substrate thickness giving longer fatigue life. It is also found that increasing CuC height will result in better solder joint fatigue performance. Finally we find that the optimal design combination is: low-level substrate CTE, chip and substrate thickness, and high-level CuC height.

Secondly, two new and novel advanced finite element simulation methodologies, based on simplifying chip/substrate as shells and interconnects as beams, are developed to address the difficulty of modeling the large number of CuC interconnects in a 20mm by 20mm wafer level package with ultra-fine pitch. Although the idea of using shell and beam elements to model substrate/chip and interconnects is not new, previous researchers have not accurately translated the displacement results from the global shell-and-beam-based model to the local model. This thesis describes first-ever the application of the shell-to-solid submodeling and shell-to-solid coupling techniques available in ABAQUS to overcome the above-mentioned difficulty in the context of modeling solder joint fatigue of electronic packages. A feasibility demonstration of the two methodologies is firstly carried out. A great saving of computational resources is realized and results show that good accuracy is achieved. After this, as a case study, the shell-and-beam-submodeling approach is chosen for fatigue life prediction of three different CuC interconnects in 20mm by 20mm wafer level packages with 100 $\mu$ m pitch. By using the shell-to-solid submodeling technique, the stress/strain of the critical solder joint can be derived. Fatigue life prediction can then be



performed based on Solomon's fatigue correlation. It should be noted that the shell-and-beam-submodeling approach can be used not only in the thermo-mechanical but also in drop impact simulation of electronic packages.

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## **CHAPTER 1: Introduction**

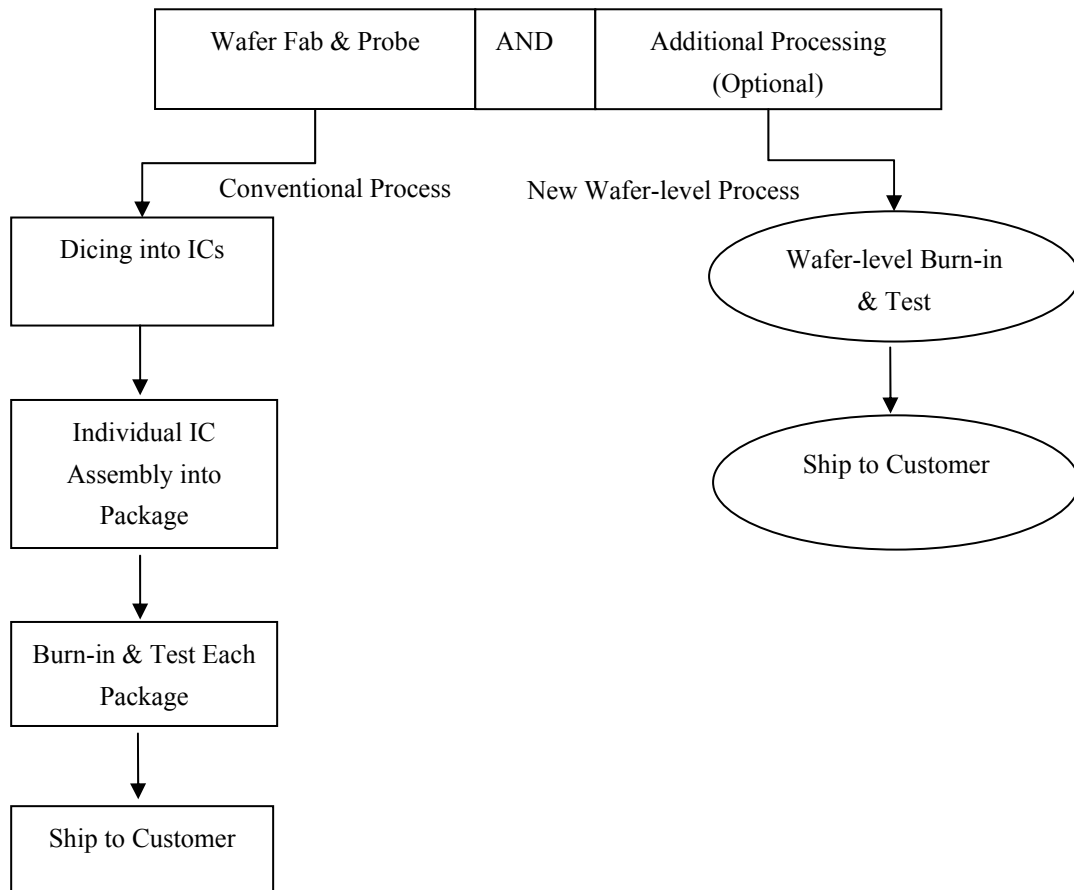
### **1.1 Background**

Since the emergence of Large Scale Integrated-circuit (LSI), the electronic packaging industry has gone through two revolutions [1]. The transition from Pin through Hole (PTH) technology to Surface Mount Technology (SMT) stands for the first revolution. After this revolution Quad Flat Package (QFP) became widely used by the industry to replace the traditional Dual in-line Package (DIP) for denser assembly on Printed Circuit Board (PCB).

The second revolution is typified by the invention of the Ball Grid Array (BGA). The emergence of BGA was driven by the need for integration of larger number of I/Os in the package and relatively coarser interconnect pitch. BGA meets the need for higher I/O number because it adopts an area array interconnect methodology instead of the peripheral array methodology used by QFP. Therefore, with the same I/O number BGA can realize a coarser pitch than QFP, making assembly of BGA much easier.

Currently electronic packaging industry is going through the third revolution. The need for high speed, high power, high number of I/Os, low cost and high performance IC packages calls for new advances in packaging technology. Among all the advances, Wafer Level Packaging (WLP) is the most promising one. In WLP, the package interconnects are fabricated directly on the wafers, the test and

burn-in process are done at the wafer level, and the dies after dicing are directly ready for SMT assembly [2]. A typical WLP process flow is shown in Figure 1.1.



**Figure 1.1 Conventional packaging in comparison with WLP [2]**

As a result of the new process flow, WLP is expected to provide the following advantages [2]:

- Providing the smallest system size, because it is truly a chip size package
- Enabling interconnect continuum from IC to PCB because of thin film processing



- Reduced cost of packaging, because all the interconnects are fabricated at the wafer level
- Reduced cost of testing, because testing is done at the wafer level for all ICs
- Reduced cost of burn-in, because the burn-in is done at the wafer level once
- Elimination of underfill because of compliancy of the leads or other ways to achieve reliability
- Improved electrical performance because of short lead lengths

The two most important momentums driving WLP are size benefits for portable products and cost benefits for all products [2].

## **1.2 Program Motivation**

The International Technology Roadmap for Semiconductors (ITRS) 2003 indicated that the IC feature size is expected to go down to 32 nm and the pitch to 20 $\mu$ m in the year 2013 [3]. Accordingly, in 2002, the NWLP program, an international collaboration among the National University of Singapore, Institute of Microelectronics, and the Packaging Research Center at Georgia Institute of Technology, USA, was initiated with the vision to develop nano-structured interconnect solutions for ultra-fine pitch WLP. The ultimate purpose of this collaboration is to develop interconnect solutions for high speed, high power IC

packages with pitch size of 100 $\mu$ m and explore possible solutions for 20 $\mu$ m pitch using nano-structured materials [4] [5].

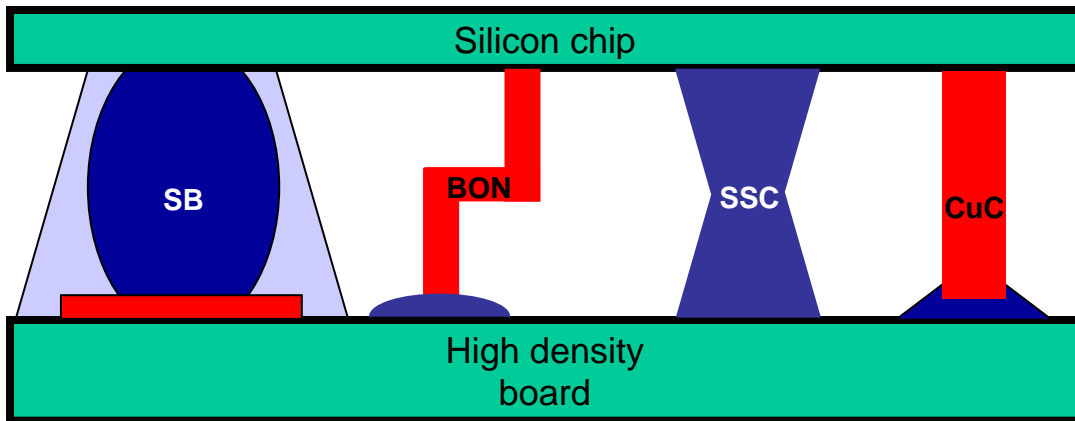
NWLP is actually an advanced version of the WLP because it extends the current WLP technology to ultra-fine interconnect pitch and explore the use of nano-structured materials to WLP for state-of-the-art package performance.

At the initial phase of this program our research focus is, however, to develop interconnect solutions for the next generation WLP with 100 $\mu$ m pitch [4].

Four candidate solutions that extend the current state of the interconnect technology are proposed. They are [5]:

- Solder Ball with No-flow Underfill (SB)
- Bed of Nails (BON)
- Stretched Solder Column (SSC)
- Copper Column Interconnect (CuC)

Figure 1.2 is a schematic picture of the four interconnects and Table 1.1 lists the main design parameters.



**Figure 1.2 Proposed 100µm pitch interconnects**

**Table 1.1 Main design parameters of the proposed interconnects**

Size of Chip	20mm by 20mm
Pitch of Interconnect	100µm
Number of I/Os	10,000 per cm <sup>2</sup>
Temperature Cycling Range	-40 °C to 125 °C
Thermal Cycle Fatigue Life	1000 cycles (target)

The SB interconnect is basically an extension of current technology down to 100µm pitch with no-flow underfill. It is a rigid interconnect. The BON interconnect consists of three segments of electroplated copper in a Z-shaped structure and is expected to be joined to the substrate using solder. It is a compliant interconnect. The SSC interconnect is fabricated by stretching molten high-lead solder bump to an hourglass shape. After that it is joined to the substrate with lead-free or eutectic solder. It is supposed to be a semi-compliant interconnect [4]. The CuC interconnect is actually a simplified version of the BON interconnect. In this interconnect technology a copper column with circular cross section is formed by

electroplating and joined to the substrate with solder. Therefore, the CuC interconnect is much easier to process than the BON interconnect. CuC interconnect is also a compliant interconnect.

CuC interconnect will be the focus of this thesis.

### **1.3 Motivation and Scope of This Work**

As far as long-term reliability of IC packages is concerned, the integrity of solder joints under cyclic temperature changes, known as thermo-mechanical reliability, must be guaranteed. This thermo-mechanical reliability concern arises from the CTE mismatch between silicon chip and substrate. As IC packages experience cyclic temperature changes, i.e. power on and off, the chip and substrate expand or shrink differently due to CTE difference. This difference of expansion or shrinkage make the solder joints between the chip and substrate undergo cyclic load and eventually cause low cycle fatigue failure.

The solder joint thermo-mechanical reliability is already a major concern for current electronic packages and is expected to be critical in view of the proposed chip size of 20mm by 20mm and pitch of 100 $\mu$ m in the NWLP program. Before any physical prototypes are made and experiments carried out, it is often of interest to 1) do a design optimization study to find out the effects of various design parameters on solder joint reliability and find out an optimal set of design

parameters combination that leads to maximum solder joint fatigue life; 2) conduct FEA to estimate the solder joint fatigue life of the critical interconnect.

To do a design optimization analysis of CuC interconnect, a 2D plane strain finite element model is an adequate and efficient. However, when accurate modeling of solder joint fatigue is required, the 2D finite element model is not adequate due to its underlying inaccurate assumption. Full 3D finite element modeling is necessary. But in light of the large package size and ultra-fine interconnect pitch coupled with the requirement for full area array, modeling of solder joint fatigue is a challenge for the current computational resources. Therefore, one of the aims of this thesis is to develop efficient and accurate modeling method to address the challenge.

To sum up, the objectives of this work are to:

- Do a design optimization study to find out the effects of changes of various design parameters on solder joint reliability and determine an optimal parameter combination.
- Develop an efficient and accurate modeling method to address the challenge of modeling solder joint fatigue.
- Use the developed modeling methodology to estimate the solder joint fatigue life of the critical corner interconnect of some CuC packages.

## **1.4 Organization of This Thesis**

This thesis consists of four chapters. Chapter 1 serves as an introduction which describes the industry background, the motivation of the NWLP program, and the motivation and scope of the current work. Chapter 2 is a review of the popular fatigue models including both strain and energy-based models. Chapter 3 contains the simulation-based design optimization process establishment procedures and a case study. Chapter 4 provides the details the newly developed simulation methodologies that can be used to efficiently address the simulation difficulty of CuC interconnect in 20mm by 20mm wafer level package with 100 $\mu$ m pitch.

## **CHAPTER 2: Brief Literature Survey on Fatigue Models**

### **2.1 Introduction**

The eutectic Pb-Sn solder is widely used in the electronic packaging industry because its low melting point allows solder joint to be formed at temperatures low enough to prevent device failure. As far as long-term reliability is concerned, the solder joint sustainability under cyclic temperature changes is vital. This is because during service life the package will experience power on and off as well as ambient temperature changes, causing the solder joints to experience cyclic loadings and eventually failures occur. The primary failure mechanism of eutectic Pb-Sn solder joint under thermal cycling is fatigue. Fatigue occurs when material undergoes repetitive loading. The repetitive loading causes damage to material. Unlike some biomaterials, this damage is cumulative and unrecoverable [6]. When this damage cumulates to a certain level, crack initiates and propagates across the material and failure occurs. There are two types of fatigue, namely high cycle fatigue and low cycle fatigue. The definitions and characteristics of these two types of fatigue are shown in Table 2.1 [6]. According to Table 2.1, solder joint fatigue in electronic packaging is categorized as low cycle fatigue. This is true because solder joints are often stressed beyond their yielding point during thermal cycling and the number of cycles to failure is much lower than  $10^4$ .

**Table 2.1 Category of fatigue [6]**

Low cycle fatigue	<ul style="list-style-type: none"> <li>• Significant plastic strain in each cycle</li> <li>• High load</li> <li>• Low number of cycles to failure, from 1 to <math>10^4</math> or <math>10^5</math> cycles</li> </ul>
High cycle fatigue	<ul style="list-style-type: none"> <li>• Largely confined to elastic range</li> <li>• Low load</li> <li>• Long life, greater than <math>10^4</math> or <math>10^5</math> cycles</li> </ul>

Since solder joints electrically and mechanically connect the chip and substrate, their integrities are important to ensure the package's long-term functionality. Therefore, there is a great interest in evaluating and predicting the solder joint fatigue life under thermal cycling. A cost-effective way for fatigue life prediction is to use finite element analysis coupled with fatigue models.

There are many fatigue models derived by different researchers using different methods. According to the different damage indicators used, the majority of those models can be categorized as strain-based and energy-based [7] [8]. Other less popular ones include crack-based, stress-based and entropy-based [9]. In current literature survey, only two most popular ones which are the strain-based and energy-based fatigue models will be reviewed. Since only eutectic Pb-Sn solder will be used in this work, emphasis will be put on eutectic and near-eutectic solders.



## 2.2 Strain-Based Fatigue Models

The most widely used fatigue models are strain based. Some of them are based on plastic strain, some on creep strain, and others on total strain.

### 2.2.1 Models Based on Plastic Strain

Some of the fatigue models, based on plastic strain only account for plastic strain (i.e. the fatigue is only related to plastic strain range) and thus is categorized as Coffin-Manson type fatigue models. Others may also take into account the cyclic frequency, cyclic temperature range, mean temperature, dwell times, dwell temperatures and loading rates, and thus categorized as Modified Coffin-Manson type fatigue models [7] [8].

#### Coffin-Manson Type

Coffin [10] and Manson [11] reported that the total number of cycles to failure,  $N_f$ , is related to plastic strain range,  $\Delta\gamma_p$ . This relation is expressed in Equation (2.1).

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_f' (2N_f)^c \quad (2.1)$$

The fatigue ductility coefficient,  $\varepsilon_f'$ , is approximately equal to the true fracture ductility,  $\varepsilon_f$ . The fatigue ductility exponent,  $c$ , is a material constant that varies between -0.5 and -0.7 [12]. Either fatigue experiments or FEA modeling can be adopted to derive the plastic strain range,  $\Delta\varepsilon_p$ , for fatigue life prediction. This Coffin-Manson fatigue model is widely used due to its simplicity. However, the

Coffin-Manson fatigue model assumes that the fatigue failure is strictly due to plastic deformation and that elastic strain plays a minor role in fatigue failure. When elastic strain is not negligible and must be taken into consideration, Basquin's fatigue model should be used in conjunction with Coffin-Manson model for fatigue prediction [6]. Basquin's equation relates the total number of cycles to failure,  $N_f$ , to the elastic strain range, and the relation is expressed as Equation (2.2) [7],

$$\frac{\Delta\varepsilon_{elastic}}{2} = \frac{\sigma_f'}{E} (2N_f)^b \quad (2.2)$$

where  $\Delta\varepsilon_{elastic}$  is the elastic strain range,  $\sigma_f'$  is the fatigue strength coefficient,  $E$  is the elastic modulus and  $b$  is the fatigue strength exponent. When both elastic and plastic strains must be considered as contributors to fatigue failure, Equation (2.1) and Equation (2.2) should be combined for fatigue life prediction [6] [13].

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f'}{E} (2N_f)^b + \varepsilon_f' (2N_f)^c \quad (2.3)$$

$\Delta\varepsilon$  is the total strain or is the sum of  $\Delta\varepsilon_p$  and  $\Delta\varepsilon_{elastic}$ . From the above three equations, we can see that for large strains or short fatigue life, plastic strain component predominant and Equation (2.1) is adequate to describe fatigue behavior. For small strains or long fatigue life, elastic strain component predominant and Equation (2.2) is adequate to describe fatigue behavior. If both

elastic and plastic strains have to be taken into account, Equation (2.3) should be used.

Another Coffin-Manson type fatigue model was proposed by Solomon [14]. In his research pure shear tests were performed and the following fatigue model was obtained.

$$\Delta\gamma_p N_f^\alpha = \theta \quad (2.4)$$

$\Delta\gamma_p$  is the plastic shear strain range,  $\theta$  is the inverse of the fatigue ductility coefficient, and  $\alpha$  is a material constant. If the strain state is much more complex than the state in a pure shear test, i.e. the strain is multi-dimensional, accumulated equivalent plastic strain should be used [15]. The definition of accumulated equivalent plastic strain is as follows:

$$\Delta\epsilon_{eq}^{pl} = \frac{\sqrt{2}}{3} \sqrt{(\Delta\epsilon_{xx}^{pl} - \Delta\epsilon_{yy}^{pl})^2 + (\Delta\epsilon_{yy}^{pl} - \Delta\epsilon_{zz}^{pl})^2 + (\Delta\epsilon_{xx}^{pl} - \Delta\epsilon_{zz}^{pl})^2 + \frac{3}{2} [(\Delta\gamma_{xy}^{pl})^2 + (\Delta\gamma_{yz}^{pl})^2 + (\Delta\gamma_{xz}^{pl})^2]} \quad (2.5)$$

where  $\Delta\epsilon_{xx}^{pl}$ ,  $\Delta\epsilon_{yy}^{pl}$ ,  $\Delta\epsilon_{zz}^{pl}$ ,  $\Delta\gamma_{xy}^{pl}$ ,  $\Delta\gamma_{yz}^{pl}$  and  $\Delta\gamma_{xz}^{pl}$  are the incremental plastic strain components acting on the solder. Equation (2.5) may also be expressed in terms of principal strain values:

$$\Delta\epsilon_{eq}^{pl} = \frac{\sqrt{2}}{3} \sqrt{(\Delta\epsilon_1^{pl} - \Delta\epsilon_2^{pl})^2 + (\Delta\epsilon_1^{pl} - \Delta\epsilon_3^{pl})^2 + (\Delta\epsilon_2^{pl} - \Delta\epsilon_3^{pl})^2} \quad (2.6)$$

The accumulated equivalent plastic strain may be defined as:

$$\varepsilon_{eq}^{pl} = \sum \Delta \varepsilon_{eq}^{pl} \quad (2.7)$$

In addition to the equivalent plastic strain, some other strain values may also be used for fatigue life prediction where multi-axial fatigue situations are expected. Cortez et al [15] [16] have investigated the use of maximum principal plastic strain and the maximum plastic shear strain as correlation parameters. Smith, Watson and Tooper [17] relation extended by Sochie [18] for multi-axial fatigue uses maximum principal stress and the maximum principal strain amplitude. Other correlation parameters used are normal stress on the maximum shear planes and the maximum shear strain by Brown and Miller [19], Lohr and Ellison [20].

### **Modified Coffin-Manson Type**

All the above Coffin-Manson type fatigue model equations are simple, so it may be reasonable to assume that their applications are likewise simple. Actually, the above Coffin-Manson type fatigue models are derived based on isothermal fatigue tests, i.e. they only define the fatigue behavior at the temperatures at which the tests were performed. Other factors that may affect the fatigue behavior of solders were not considered.

Coffin [21] [22] found that decreasing the cyclic frequency by increasing the cycle period generally reduces the number of cycles to failure. He described the effect of cyclic frequency on fatigue behavior using a frequency-modified version of the Coffin-Manson equation, i.e., by

$$\left(N_f \nu^{(K-1)}\right)^\alpha \Delta\gamma_p = \theta \quad (2.8)$$

where  $K$  is determined at different temperatures, which defines the effect of cyclic frequency. If  $K = 1$ , the cyclic frequency has no effect on fatigue behavior; if  $K = 0$ , the time to failure,  $t_f$ , is a constant for constant plastic strain ( $N_f / \nu = t_f$ ). Generally  $K$  is between 1 and 0.

The hold time and ramp rate also have effect on solder joint fatigue behavior. Vaynman and Fine [23] found that the number of cycles to failure  $N_f$  is given by

$$N_f = \left(C + D(t_{ht} + t_{hc})\right) / (2t_r + t_{ht} + t_{hc}) \quad (2.9)$$

where  $C$  and  $D$  are constants and  $t_{ht}$ ,  $t_{hc}$  and  $t_r$  are the tensile hold time, compressive hold time, and the ramp time, respectively. This approach requires experiments to determine  $C$  and  $D$ .

Engelmaier [24] proposed a fatigue model based on data from [25] that takes into account effects of both frequency and temperature. According to his fatigue model, the total number of cycles to failure is related to the total shear strain range  $\Delta\gamma_t$ .

The relation is shown in Equation (2.10),

$$N_f = \frac{1}{2} \left( \frac{\Delta\gamma_t}{2\varepsilon_f} \right)^{1/c} \quad (2.10)$$

where  $c = -0.442 - 6 \times 10^{-4} \bar{T}_s + 1.74 \times 10^{-2} \ln(1 + f)$ .  $\bar{T}_s$  is the mean cyclic solder joint temperature in  $^\circ C$ , and  $f$  is the cyclic frequency in cycles/day.

### 2.2.2 Models Based on Creep Strain

As far as solder joints are concerned, their fatigue failure due to creep has been found to be related to two creep mechanisms, namely grain boundary sliding and matrix creep [7].

Knecht and Fox [26] have developed a fatigue life prediction model based on the amount of matrix creep generated during thermal cycling. This model uses a similar form as the Coffin-Manson fatigue model. This equation is:

$$N_f = \frac{C}{\gamma_{mc}} \quad (2.11)$$

The number of cycles to failure,  $N_f$ , is related to a constant  $C$ , which is independent on failure criteria and solder microstructure.  $\gamma_{mc}$  is the matrix creep strain and defined as:

$$\gamma_{mc} = \int C \left( \tau / \tau_0 \right)^{n_{mc}} dt \quad (2.12)$$

where  $n_{mc}$  and  $\tau_0$  is a constant, and  $\tau$  is the shear stress as a function of time.

Syed [27-29] proposed a fatigue model that includes the other creep mechanism, grain boundary sliding, with matrix creep. In this model, creep strain is partitioned into two parts as shown in Equation (2.13):

$$N_f = \left( 0.022 D_{gbs} + 0.063 D_{mc} \right)^{-1} \quad (2.13)$$

where  $D_{gbs}$  and  $D_{mc}$  are the accumulated equivalent creep strain per cycle for grain boundary sliding and matrix creep, respectively.

### 2.2.3 Combination of Plastic and Creep Strain

#### Miner's Rule

Miner's linear superposition rule can be used to combine the effects of both plastic and creep strains in a fatigue model. A typical application of this rule is the combination of Equation (2.1) and Equation (2.11) into Equation (2.14) [30],

$$\frac{1}{N_f} = \frac{1}{N_p} + \frac{1}{N_c} \quad (2.14)$$

where  $N_p$  is the number of cycles to failure due to plastic strain in Equation (2.1) and  $N_c$  is the number of cycles to failure due to creep strain in Equation (2.11).

#### Strain Range Partitioning

Manson [31-33] used strain range partitioning (SRP) to predict fatigue life. The underlying assumption of SRP is that a typical hysteresis loop may be partitioned into four components: the plastic strain in tension and compression (PP), the creep strain in tension and compression (CC), the creep strain in tension and plastic strain in compression (CP), as well as the plastic strain in tension and creep strain in compression (PC). The fatigue life is determined using Equation (2.15):

$$\frac{1}{N_f} = \frac{F_{pp}}{N_{pp}} + \frac{F_{cc}}{N_{cc}} + \frac{F_{cp}}{N_{cp}} + \frac{F_{pc}}{N_{pc}} \quad (2.15)$$

where  $F_{ij}$  the fraction of the total inelastic strain range of the hysteresis loop. The contribution from each part is determined from other fatigue models and from cyclic stress-strain tests.

## 2.3 Energy-Based Fatigue Models

The fatigue failure of materials normally goes through two stages, namely crack initiation and crack propagation. Among the energy based fatigue models, some of them only calculate the number of cycles to crack initiation while others predict the overall fatigue life from a combination of crack initiation and propagation.

### 2.3.1 Non Crack-Propagation-Included Models

#### Energy Partitioning

Energy-based fatigue models were developed later than the strain-based ones, but they are becoming increasingly popular. These models use hysteresis energy or volume-weighted average stress-strain history to predict fatigue life.

Dasgupta [34] proposed the use of total strain energy derived from stress-strain history as an indicator of fatigue life. This strain energy includes both elastic strain energy and inelastic work dissipated during each thermal cycle. A detailed stress-strain analysis is required to determine the elastic strain energy density  $U_e$ , plastic energy dissipation  $W_p$ , and creep strain energy dissipation  $W_c$  within a typical thermal cycle. The relation between fatigue life and the above energy components is expressed in Equation (2.16),

$$U = U_e + W_p + W_c = U_{e0} N_{fe}^{b'} + W_{p0} N_{fp}^{c'} + W_{c0} N_{fc}^{d'} \quad (2.16)$$

where the coefficients  $U_{e0}$ ,  $W_{p0}$  and  $W_{c0}$  represent the intercepts of the elastic, plastic and creep energy density versus fatigue life curves on a log-log plot, while



the exponents  $b'$ ,  $c'$ , and  $d'$  are their corresponding slopes. The variables  $N_{fe}$ ,  $N_{fp}$ , and  $N_{fc}$  represent the cycles to failure due to elastic, plastic and creep deformations, respectively. Similar to Equation (2.14), the total damage is computed by summing the inverse of  $N_{fe}$ ,  $N_{fp}$ , and  $N_{fc}$ .

$$D_{total} = \frac{1}{N_{fe}} + \frac{1}{N_{fp}} + \frac{1}{N_{fc}} \quad (2.17)$$

It is obvious that the above fatigue model uses an energy partitioning approach. When multiple damage mechanisms need to be taken into account, Equation (2.17) is used to compute the total damage from each damage mechanism.

### **Models Based on Total Energy**

Morrow [35] was one of the first modern fatigue researchers to show that fatigue life could be correlated with the mechanical energy of hysteresis loop. His energy based fatigue model is shown in Equation (2.18),

$$N_f^m W = \theta_E \quad (2.18)$$

where  $m$  and  $\theta_E$  are constants.

Akay [36] proposed that the volume-weighted average total strain energy dissipated in a stabilized response cycle can be related to the mean cycles to failure,  $N_f$ , using the following equation,

$$N_f = \left( \frac{\Delta W_{total}}{W_0} \right)^{1/k} \quad (2.19)$$

where  $\Delta W_{total}$  is the total strain energy calculated from the volume-weighted averages over a stabilized cycle,  $W_0$  and  $k$  are load-independent material constants. Successful applications of this fatigue model on LLCC leaded packages were reported by Akay [36]. Based on his studies the values of  $W_0$  and  $k$  were determined to be  $W_0 = 0.1573$  and  $k = -0.6342$  for the leaded joints tested.

Liang et al [37] have developed a fatigue model that takes into account the geometry of solder joint based on elastic and creep analyses. This model is expressed in Equation (2.20),

$$N_f = C(W_{ss})^{-m} \quad (2.20)$$

where  $W_{ss}$  is the stress-strain hysteresis energy density.  $C$  and  $m$  are temperature-dependent material constants determined from experiments. Successful application of this model was reported by Liang in BGA packages.

### **2.3.2 Models Which Include Crack-Propagation**

All the above energy-based fatigue models do not account for crack propagation, i.e. they only predict the number of cycles to crack initiation. Prediction of the overall time to failure needs to include crack propagation.

Gustafsson [38] has proposed a fatigue model that combines the crack initiation and propagation based on the findings from Darveaux. This fatigue model is shown in Equation (2.21).

$$N_{aw} = N_{0s} + \frac{a - (N_{0s} - N_{0p}) \frac{da_p}{dN}}{\frac{da_s}{dN} + \frac{da_p}{dN}} \quad (2.21)$$

For either crack initiation or propagation, it is considered that there are primary and secondary cracks, denoted by the subscripts  $p$  and  $s$ , respectively. The primary and secondary cracks are considered to initiate and propagate towards each other at different rates.  $N_{aw}$  is the total number of cycles to failure, and  $a$  is the total possible crack length.  $N_{0p}$  and  $N_{0s}$  are the primary and secondary crack initiation energy terms, respectively. They can be calculated by Equation (2.22) [38],

$$N_{0p}, N_{0s} = 54.2 \Delta W^{-1.00} \quad (2.22)$$

where  $\Delta W$  is energy density calculated from the hysteresis curves in an analysis. Finite element results reported by Gustafsson were based on the leadless RF-transistor solder joints.

The crack propagation terms,  $da/dN$ , are dependent on the corresponding values of  $\Delta W$ , as shown in Equation (2.23) [38].

$$\frac{da}{dN} = 3.49 \times 10^{-7} \Delta W^{1.13} \quad (2.23)$$

## 2.4 Conclusion

Various fatigue models for solder joint fatigue life prediction are available in the literature. The damage indicators they use range from popular ones like strain range and energy density to less popular ones including stochastic crack, stress and

entropy. Among all the solder joint fatigue models, the strain-based and energy-based ones constitute the majority. This chapter has reviewed some of the most popular strain-based and energy-based fatigue models. For more details on each of the fatigue models described in this chapter, the readers are encouraged to read the corresponding reference papers.

It should be noticed that each of the fatigue models was developed for a certain type of electronic package. Therefore, when one wants to make accurate fatigue life prediction using a fatigue model he or she should always use the most relevant one, i.e. for a BGA package, use a fatigue model developed for BGA packages rather than another fatigue model developed for leaded packages.

One of the purposes of this work is to carry out solder joint fatigue life prediction for CuC interconnect in WLP. However, the CuC interconnect is a new type of interconnect and no available fatigue models in the literature have been developed specially for solder joint fatigue life prediction of this interconnect/package. Furthermore, this kind of interconnect is still in the development stage and no dummy packages or physical prototypes are readily available for experimentally determining the fatigue life prediction model.

To move forward, this thesis will use Solomon's fatigue correlation,

$$\Delta\gamma_p N_f^{0.51} = 1.14 \quad (2.24)$$

where  $\Delta\gamma_p$  is the cyclic shear strain range. This correlation is chosen based on its ease of use.

## **CHAPTER 3: Simulation-based Design Optimization on CuC**

### **3.1 Introduction**

Traditionally, a product development process from conceptual design to final large-volume manufacturing usually contains the following two typical procedures.

1) The design engineers do the initial design to meet the functional requirements for the product. Some simple analytical calculations are needed to design against potential product failures. 2) After the design procedure, some physical prototypes must be made. Test engineers have those prototypes undergo actual service conditions or sometimes accelerated testing conditions to see whether reliability requirements are met. If, fortunately, those requirements are met, the product may be manufactured in large volume and put into the market. Unfortunately, however, in most cases, not all the reliability requirements are met and re-design, re-prototyping and re-testing have to be carried out. The design, prototyping and testing procedures loop until all the reliability requirements are met. This approach for product design is called the trial-and-error method. It is clear that this design approach is quite time-consuming and the final product cost can be very high due to the fact that many loops may have been done until all the reliability requirements are met. Physical prototyping is also expensive.

Recently product development has been speeded up and cost is reduced by the extensive use of computer simulation techniques, which greatly reduce or even in some occasions eliminate the need for physical prototyping. This design approach

using computer simulation is often called virtual prototyping. Virtual prototyping means that the prototype is modeled in computer simulations and potential reliability issues are foreseen and reduced as much as possible before physical prototypes are fabricated. By using the virtual prototyping approach, in many cases, physical prototyping and testing are only needed to verify the results of computer simulation. Another benefit that virtual prototyping provides is its ability to gain an insight into the effect that changes in design parameters (i.e. geometry or material properties) have on product reliability and hence give some indications on how to improve the design. The investigation of changes in design parameters on reliability is called parametric study.

More recently engineers have found that although virtual prototyping combined with parametric study provides critical data and insight into the effects of changes in design parameters such approach can be very time-consuming because each simulation run may require a long time to complete with the presence of nonlinearities in geometry, material properties and boundary conditions. Also, the parametric study cannot investigate two parameters simultaneously and very important interaction effects are likely to be missed in such an analysis. Besides, this approach cannot give enough information on how to arrive at an optimal design within the design constraints. To overcome these drawbacks design of experiments (DoE) technique, Surrogate Modeling technique and numerical optimization technique, together with virtual prototyping have been integrated to

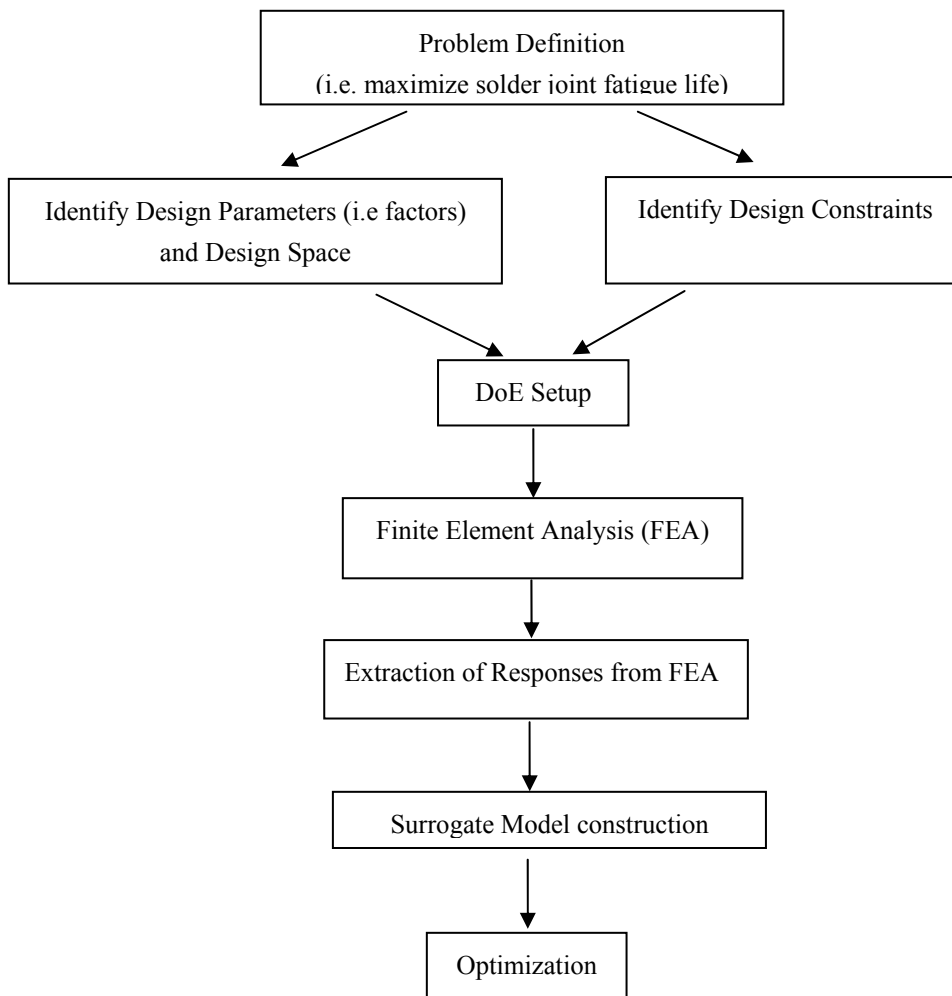
form a new design approach called Simulation-based Design Optimization. This new approach not only has the capability to study the effects of changes of different design parameters but also provides a systematic method on how to combine different design parameters within various design constraints to arrive at an optimal parameter combination that leads to optimal reliability.

In the context of solder joint thermo-mechanical reliability design, many researchers have applied the Simulation-based Design Optimization approach to optimize the solder joint fatigue life by finding the optimal or near-optimal set of design parameters (Mertol [39-41]; Dasgupta et al [42]; Zhang [43]; Stoyanov [44]; Vandeveldel et al [45-46]; Driel et al [47] [48]; Jagarkal et al [49]; Yang et al [50]; Lee et al [51]).

A typical flow chart for the solder joint thermo-mechanical reliability design using Simulation-based Design Optimization approach is show in Figure 3.1.

Those steps involved in the above flow chart will be explained in detail in the next section.





**Figure 3.1 Typical flow chart for Simulation-based Design Optimization**

## **3.2 Steps of Simulation-based Design Optimization**

### **3.2.1 Problem Definition**

In the current context of solder joint thermo-mechanical reliability design, the problem is solder joint fatigue and the objective is to find an optimal set of design parameters to maximize solder joint fatigue life.

### **3.2.2 Identification of Design Factors, Space and Constraints**

Design factors are independent design parameters, i.e. changing one factor will not involve changing the other factors. The design space is typically a multi-dimensional hypercube defined by the upper and lower bounds of each design factor over some region of interest. The upper and lower bounds of a factor are a special type of constraint. Another type of constraint is the one put on the system response (i.e. the output of an input of design factors combination). An example of this constraint is that while the solder joint fatigue life needs to be maximized, the stress in the chip should not exceed a certain value to avoid die cracking.

### **3.2.3 DoE Setup**

There are actually numerous design points across the design space. To find the optimal design point, obtaining the system responses at all the design points is definitely impractical. Design of experiments (DoE) method is a systematic sampling method used to optimize the selection of design points for subsequent surrogate modeling. There are many types of DoE methods, including the classical ones and new ones developed with the emergence of computer simulation. The classical DoE methods were originally developed for planning physical experiments where random variations cannot be eliminated. Those methods include full factorial design, central composite design (CCD), Box-Behnken design, and their variants [52]. Since the wide use of computer simulation, new data sampling methods known as design and analysis of computer experiments (DACE)

have been developed. These methods include Monte Carlo sampling, Latin Hypercube sampling, and orthogonal array sampling [52].

In the realm of electronic packaging, various researchers have used different DoE methods to sample the design space. Mertol [39-41] applied the orthogonal array sampling method in chip scale package design. Dasgupta et al [42] developed a generic computational optimization methodology based on orthogonal array sampling method. Zhang et al [43] reported Philips' strategy of virtual thermo-mechanical prototyping developed based on Latin Hypercube sampling. Vandeveldel et al [45] [46] and Driel et al [47] [48] also used the Latin Hypercube sampling method to do the optimization work for thermo-mechanical reliability optimization of chip scale package and nonlinear packaging stress, respectively. Stoyanov et al [44] did a design optimization study using the orthogonal array method for solder joint thermo-mechanical reliability in flip chip package with no-flow underfill. Jagakal and his colleagues [49] used ANSYS software and its integral optimization module to optimize the solder joint reliability in a board-level electronic package. They used sub-approximation method, full factorial method and CCD method to conduct the optimization study and found that the optimal solution derived based on the full factorial method is best among the three for that specific case. Yang et al [50] did an optimization study for solder joint reliability in a lead-free flip chip on board (FCOBO) package using CCD method. Lee et al

[51] performed a full factorial study on the solder joint reliability of a double-layer wafer level package.

From the above literature survey, it seems that the full factorial, orthogonal array and Latin Hypercube methods are more popular than others.

### **3.2.4 Finite Element Analysis**

After the DoE method is chosen, many finite element models will be built according to the different factor combinations or design points sampled from the design space by the selected DoE method and sent to a finite element code for analysis. Usually a finite element analysis of one model is called a trial.

### **3.2.5 Responses Extraction**

After all the trials are done, the desired system responses must be extracted for surrogate modeling in the next step.

### **3.2.6 Surrogate Model Construction**

Surrogate model construction, also known as surface fitting, metamodeling or response surface approximation, is widely used in engineering design applications to provide an insight into the trends exhibited by system responses with respect to changes in values of design factors. Once all the system responses at the sampled design points are derived from finite element simulation, it is ready for us to set up a surrogate model. The purpose of surrogate model construction is to derive a closed-form mathematical model to approximate the relationship between design

factors and the system response. If such a surrogate model is established, system responses for other design factor combinations or design points can be determined using this model and thus eliminate the need for further expensive and time-consuming finite element simulations.

There are several types of surrogate model construction methods, including quadratic polynomial model, first-order Taylor series expansion, Kriging spatial interpolation model, stochastic layered perception artificial neural networks, and multivariate adaptive regression splines. All of these surrogate model construction methods can be used to design applications with arbitrary numbers of design factors.

Among all the surrogate model construction methods, the quadratic polynomial is most frequently used due to its computational simplicity and convenient algebraic form [52]. In the design optimization studies for electronic packaging, the popularity of quadratic polynomial can be seen in the works of Mertol [39-41], Dasgupta et al [42], Zhang et al [43], Stoyanov [44], Vandeveldel et al [45] [46], Driel et al [47] [48], Jagarkal et al [49], Yang et al [50] and Lee et al [51]. However, surrogate model constructed using the quadratic polynomial method does not always meet the accuracy requirement. If intolerable discrepancy is found between the predicted system response from the surrogate model and true values

from computational simulation, more reliable and complex methods, such as Kriging model may be used for surrogate model construction [47].

Typically, a surrogate model constructed using the quadratic polynomial method takes on the form of a fully quadratic polynomial with cross-terms [50] [52].

$$\hat{y} = C_0 + \sum_{i=1}^m C_i x_i + \sum_{i=1}^m \sum_{j=1}^m C_{ij} x_i x_j + \varepsilon \quad (3.1)$$

In Equation (3.1),  $\hat{y}$  is the response value of the system,  $m$  is the number of design factors,  $x_i (i=1-m)$  are the design factors,  $\varepsilon$  is the residual error term,  $C_0$  is the constant term of the approximation model,  $C_i (i=1-m)$  are the coefficients of linear terms and  $C_{ij} (i, j=1-m)$  are the coefficients of the quadratic terms.

### 3.2.7 Optimization

Once the response surface approximation model is derived and specified accuracy criteria satisfied, various types of design optimization can be carried out efficiently. If an optimal design parameters combination is derived and this combination is not a trial in the original DoE setup, an extra simulation run based on this optimal parameter setting should be performed as verification.

### 3.2.8 Conclusion

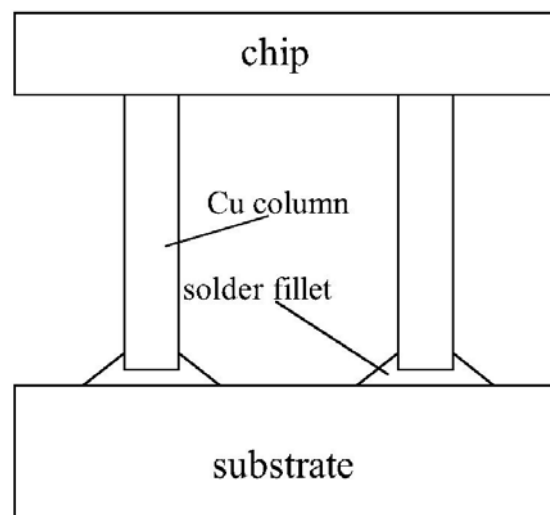
Some commercially available software packages, such as iSIGHT, Modelcenter, Modelfrontier, DAKOTA, Optimus, VisualDoC, can integrate the above design optimization procedures and run those procedures in an integrated and automated

manner. But those software tools are not available in our program. To move forward, ABAQUS FEA software, together with statistical software, Minitab and S-Plus, will be used for the current design optimization study and the optimization procedures will be conducted manually.

### 3.3 Optimization Study on the CuC Interconnect

#### 3.3.1 A Brief Note on the CuC Interconnect

The CuC interconnect is actually a simplified version of the BON interconnect. In this interconnect a copper column with circular cross section is formed by electroplating and joined to the substrate using solder. Therefore, the CuC interconnect is much easier to process than the BON interconnect. The CuC interconnect is supposed to be a compliant interconnect. Figure 3.2 shows a schematic picture of the CuC interconnect.



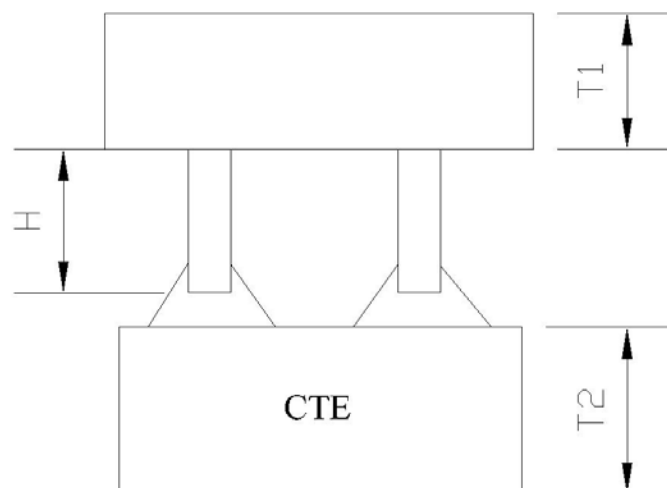
**Figure 3.2 Schematic picture of the CuC interconnect**

### 3.3.2 Problem Definition

As far as long-term reliability of electronic package is concerned, solder joint integrity under temperature cycling is vital. The purpose of the current design optimization study on the CuC interconnect is to find an optimized set of design parameters that leads to optimized solder joint thermo-mechanical reliability. In this study, maximization of solder joint fatigue life, i.e. minimization of the fatigue damage indicator at the outermost (critical) interconnect, will serve as the optimization objective.

### 3.3.3 Identification of Design Factors and Space

Based on the inputs from process people, the design factors identified for the current design optimization study are illustrated in Figure 3.3 and listed in Table 3.1.



**Figure 3.3 Illustrations of Design Factors**



**Table 3.1 Design factors and their variations**

Symbol	Design factors	Variations
T1	Chip thickness ( $\mu\text{m}$ )	250 ~ 640
T2	Substrate thickness ( $\mu\text{m}$ )	800 ~ 1200
H	CuC height ( $\mu\text{m}$ )	100 ~ 150
CTE	Substrate CTE (ppm/K)	8 ~ 10

### 3.3.4 DoE Study Setup

Given the design factors and design space, the next step would be the selection of an appropriate DoE method to sample the design space. For the current study, the 2-level full factorial DoE method will be adopted. Since there are four design factors, the number of simulation runs required would be:

$$k^n = 2^4 = 16 \quad (3.2)$$

where  $k$  is the number of levels for each design factor, and  $n$  is the total number of design factors.

After the DoE method is selected, the design table is built and shown in Table 3.2.

**Table 3.2 DoE design table**

Trial No.	T1 ( $\mu\text{m}$ )	T2 ( $\mu\text{m}$ )	H ( $\mu\text{m}$ )	CTE (ppm/K)
1	250	800	100	8
2	640	800	100	8
3	250	1200	100	8
4	640	1200	100	8
5	250	800	150	8
6	640	800	150	8
7	250	1200	150	8
8	640	1200	150	8
9	250	800	100	10
10	640	800	100	10
11	250	1200	100	10
12	640	1200	100	10
13	250	800	150	10
14	640	800	150	10
15	250	1200	150	10
16	640	1200	150	10

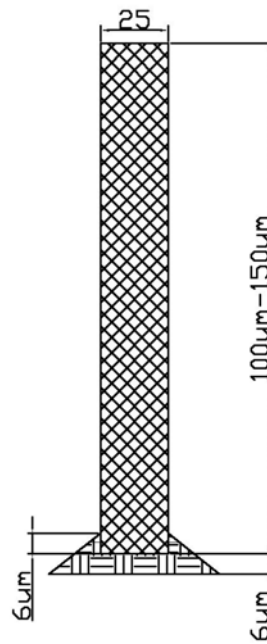
### 3.3.5 Finite Element Analysis

#### Geometry and Mesh

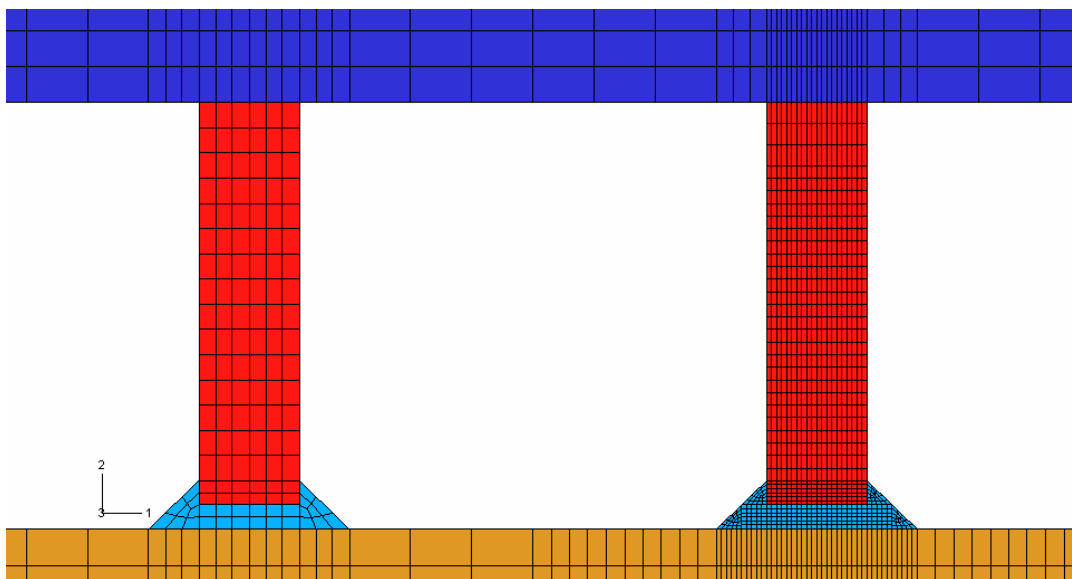
The detailed modeling parameters for the electronic package under investigation are shown in Table 3.3 and Figure 3.4. Those data are based on Table 3.1 and inputs from process group. Based on previous study in [9], the hysteresis loop of stress-strain will converge after five cycles. So five temperature cycles will be simulated in the current analyses.

**Table 3.3 Details of modeling parameters**

Chip thickness	250 ~ 640 $\mu$ m
Substrate thickness	800 ~ 1200 $\mu$ m
Substrate CTE	8 ~ 10ppm/K
Solder gap	6 $\mu$ m
Column wetting height	6 $\mu$ m
Solder pad diameter	50 $\mu$ m
CuC radius	25 $\mu$ m
CuC height variation	100 ~ 150 $\mu$ m
Interconnect pitch	100 $\mu$ m
Chip size	20mm by 20mm
Temperature extremes	125°C to -40°C
Number of cycles modeled	5



**Figure 3.4 Dimensions of the CuC interconnect**



**Figure 3.5 2D mesh of the electronic package under investigation  
(a close-up view of the corner part)**

2D plane strain model is used for the finite element analysis in the current design optimization study. Although the 2D plane strain model adopts an inaccurate underlying assumption, it is well suitable for design optimization study where

accurate prediction of solder joint fatigue life is not a necessity [53] and only the trend is of more importance. In the current analyses, CPE4 plane strain element in ABAQUS is adopted.

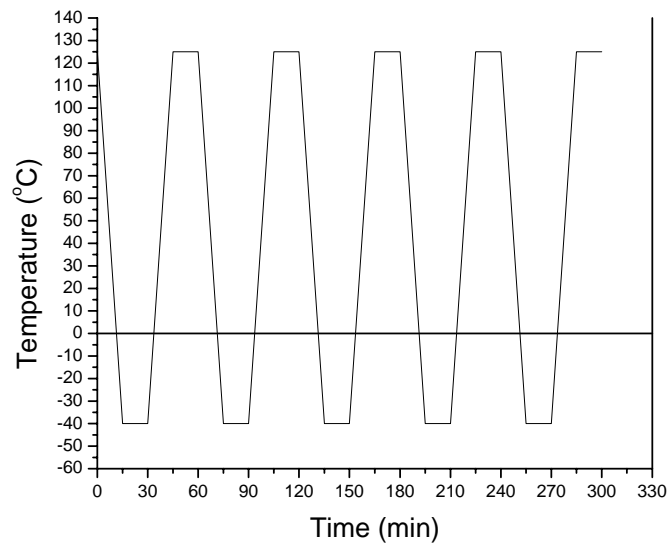
A typical mesh of the package under investigation is shown in Figure 3.5.

### **Loading and Boundary Conditions**

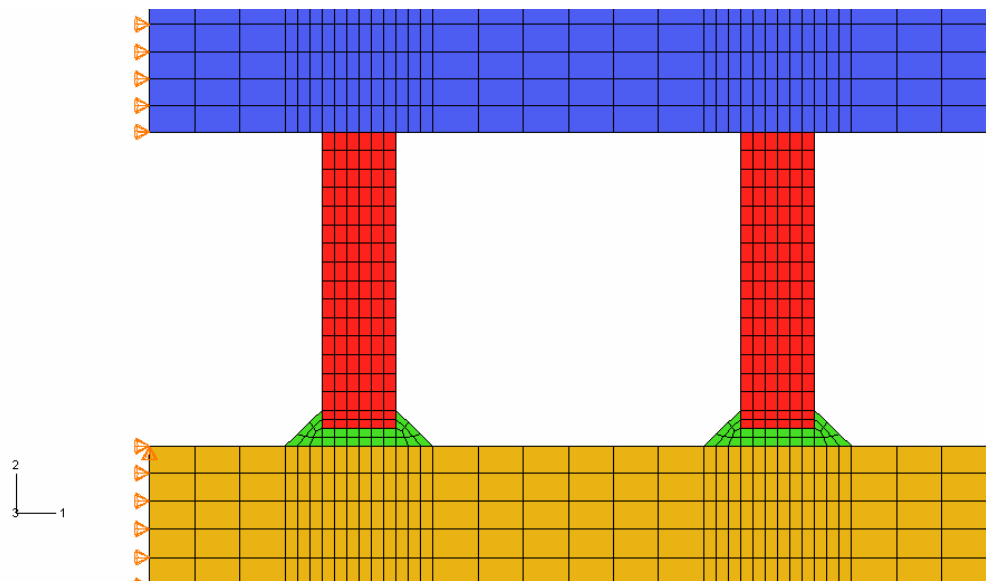
When doing the analysis of solder joint thermo-mechanical reliability, we assume that the only loading acting on the electronic package is the cyclic temperature change. In the most rigorous way of solder joint fatigue modeling, initial temperatures are specified for all parts of the package and a thermal analysis is first conducted to obtain the temperature field within the package, then this temperature field is used as an input for subsequent stress analysis [53]. The above analysis is known as sequentially coupled temperature-displacement analysis. However, in most cases, the temperature field is assumed to be uniform in all the parts of the package as the temperature cycles between its extremes [53]. This assumption eliminates the need for a thermal analysis.

In this study, the above mentioned assumption is adopted. The temperature cycling profile is shown in Figure 3.6. The stress-free state is assumed to be at 125°C.

The boundary condition for the finite element model is shown in Figure 3.7. The package neutral line is required only to be able to move along y-direction and a point is fixed to prevent rigid body motion.



**Figure 3.6 Temperature cycling profile**



**Figure 3.7 Boundary conditions of the 2D finite element model**

### Material Properties

Modeling of solder joint fatigue requires accurate material properties for all the materials in the electronic package. Although such data is extensively available,

they are derived from bulk specimens rather than very small-scaled ones. It should be noted that material properties derived from bulk material tests could be quite different from material properties when the characteristic size of the material is down to less than  $100\mu\text{m}$  [54] [55]. Moreover, material properties are also known to be dependent on the preparation procedure of specimens [56]. Due to the lack of appropriate material properties, however, the current study will use the data available in the literature to move forward. Both chip and substrate are modeled as temperature-independent linear elastic materials whose properties are listed in Table 3.4. Copper is assumed to be a temperature-independent elastic-plastic material with properties stated in Table 3.5. Eutectic tin-lead solder is modeled as a temperature-dependent elastic-plastic material whose properties are detailed in Table 3.6 [9] [57]. Due to the prohibitive computational resources required, creep property of solder is not modeled [57].

**Table 3.4 Material properties for chip and FR4 board**

	Chip	Substrate
Young's modulus( GPa ), E	131	22
Poisson's ratio, $\nu$	0.23	0.28
CTE(ppm/K)	2.8	8 ~ 10

**Table 3.5 Material properties for copper**

Young's modulus(GPa ), E	35.7
Poisson's ratio, $\nu$	0.34
CTE(ppm/K )	16.7
Yield stress(GPa ), $\sigma_y$	100
Plastic strain at stress=125 MPa	0.0016
Plastic strain at stress=150 MPa	0.0028
Plastic strain at stress=175 MPa	0.0043
Plastic strain at stress=200 MPa	0.0075
Plastic strain at stress=212.5 MPa	0.0099
Plastic strain at stress=225 MPa	0.0139
Plastic strain at stress=231.7 MPa	0.0186
Plastic strain at stress=238 MPa	0.0301



**Table 3.6 Material properties for solder**

Temperature(K)	233	273	303	333	363	393	423
Young's modulus(GPa ), E	40.554	34.474	29.914	25.354	20.794	16.234	11.674
Poisson's ratio, $\nu$	0.35						
CTE(ppm/K)	22.4						
Yield stress(GPa ), $\sigma_y$	38	31	25.6	20.3	14.9	9.6	4.2
Stress( MPa ) at plastic strain=0.002	46.4	39.1	32.2	25.5	17.9	10.1	4.5
Stress( MPa ) at plastic strain=0.005	50.2	42.3	34.8	27.4	19.3	10.5	4.7
Stress( MPa ) at plastic strain=0.01	53	44.5	36.4	28.4	20	10.8	4.8
Stress( MPa ) at plastic strain=0.02	56.6	46.7	37.8	29.5	20.7	11.1	4.9
Stress( MPa ) at plastic strain=0.05	60.3	49.6	40	30.9	21.4	11.5	5.0
Stress( MPa ) at plastic strain=0.1	63.4	51.7	41.6	31.9	22.0	11.8	5.1
Stress( MPa ) at plastic strain=0.2	66.8	53.9	43.2	33.1	22.7	12	5.2
Stress( MPa ) at plastic strain=0.5	71.9	57.2	45.6	34.9	23.3	12.3	5.35

### 3.3.6 Responses Extraction

In the current study, incremental equivalent plastic strain defined in Equation (2.5), (2.6) and (2.7) will be used as the indicator of fatigue life. It should be noted that the copper/solder and the solder/substrate interfaces usually involve abrupt geometrical changes which will cause singular stress/strain responses. Since

nonlinear material properties are taken into account, such stress/strain concentration is alleviated. Techniques are needed to characterize the strain response around the singularity point. It is also known that the strain value near the concentration area is very sensitive to mesh density. To solve all the above problems and to make fair comparisons among the results from different models, a volume-weighted technique is adopted to average the strain values derived. The volume-weighted technique is expressed in Equation (3.3) [58],

$$\Delta\varepsilon_{avg} = \frac{\sum_{e=1}^n \Delta\varepsilon_e \times V_e}{\sum_{e=1}^n V_e} \quad (3.3)$$

where  $\Delta\varepsilon_e$  is the incremental equivalent plastic strain of the e-th element and  $V_e$  is the volume of the e-th element. In the current study the incremental equivalent plastic strain is averaged over the entire solder volume.

According to the design table shown in Table 3.2, sixteen finite element models for all the sixteen design factors combinations are constructed. The responses for all the sixteen models are extracted and listed in Table 3.7.

**Table 3.7 Responses of all the sixteen finite element models**

Trial No.	T1 ( $\mu\text{m}$ )	T2 ( $\mu\text{m}$ )	H ( $\mu\text{m}$ )	CTE (ppm/K)	$\Delta\mathcal{E}_{avg}$	Surrogate Model predictions
1	250	800	100	8	0.0066	0.006388
2	640	800	100	8	0.0087	0.008888
3	250	1200	100	8	0.0080	0.008088
4	640	1200	100	8	0.0093	0.009238
5	250	800	150	8	0.0061	0.006013
6	640	800	150	8	0.0078	0.007913
7	250	1200	150	8	0.0074	0.007613
8	640	1200	150	8	0.0084	0.008163
9	250	800	100	10	0.0086	0.008837
10	640	800	100	10	0.0139	0.01369
11	250	1200	100	10	0.0120	0.01189
12	640	1200	100	10	0.0153	0.01539
13	250	800	150	10	0.0076	0.007662
14	640	800	150	10	0.0120	0.01191
15	250	1200	150	10	0.0108	0.01061
16	640	1200	150	10	0.0133	0.01351

### 3.3.7 Surrogate Model Construction

After all the responses for the sixteen design points are extracted, the next step is to construct a surrogate model to approximate the relationship between the system response and the design factors and interactions. In this study the system response is the volume-weighted incremental equivalent plastic strain.

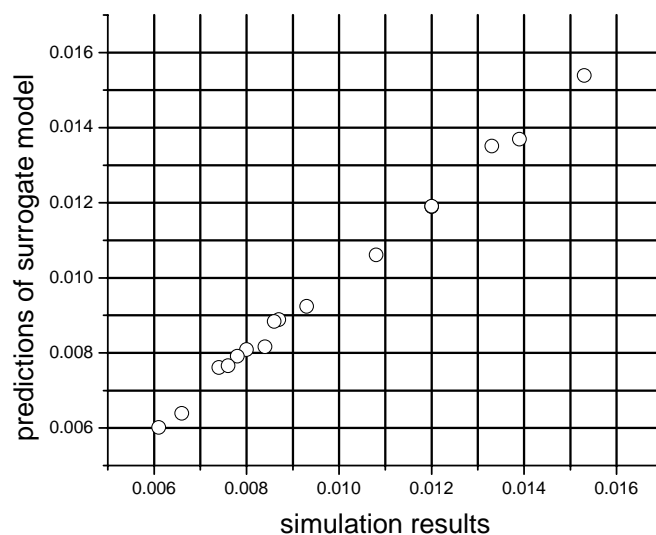
Various surrogate models may be used for the approximation. In current study, quadratic polynomial model that takes on the form in Equation (3.1) will be adopted. The coefficients in the polynomial equation are determined by fitting the system response data using the least squares approach and is derived using Minitab software. The following quadratic polynomial shown in Equation (3.4) is found to be the approximation between the volume-weighted incremental equivalent plastic strain  $\Delta\epsilon_{avg}$  and the four design parameter, T1, T2, H and CTE:

$$\begin{aligned} \Delta\epsilon_{avg} (T1(\text{mm}), T2(\text{mm}), H(\text{mm}), \text{CTE}(\text{ppm/K})) \\ = -0.000139423076922915 - 7.69230769230764e-006 \times T1 \\ - 6.5865385113284e-006 \times T2 + 6.81923096999526e-005 \times H \\ - 7.82051283749752e-005 \times \text{CTE} - 8.65384587086737e-009 \times T1 \times T2 \\ - 3.07692307978868e-008 \times T1 \times H + 3.01282061263919e-006 \times T1 \times \text{CTE} \\ - 4.99999987368938e-009 \times T2 \times H + 1.68750004377216e-006 \times T2 \times \text{CTE} \\ - 7.999999797903e-006 \times H \times \text{CTE} \end{aligned}$$

(3.4)

After the above surrogate model is derived, its accuracy must be evaluated. Several statistical methods which are based on Residual Analysis, Analysis of Variance, and statistical efficiency measures, can be used to judge the quality of the

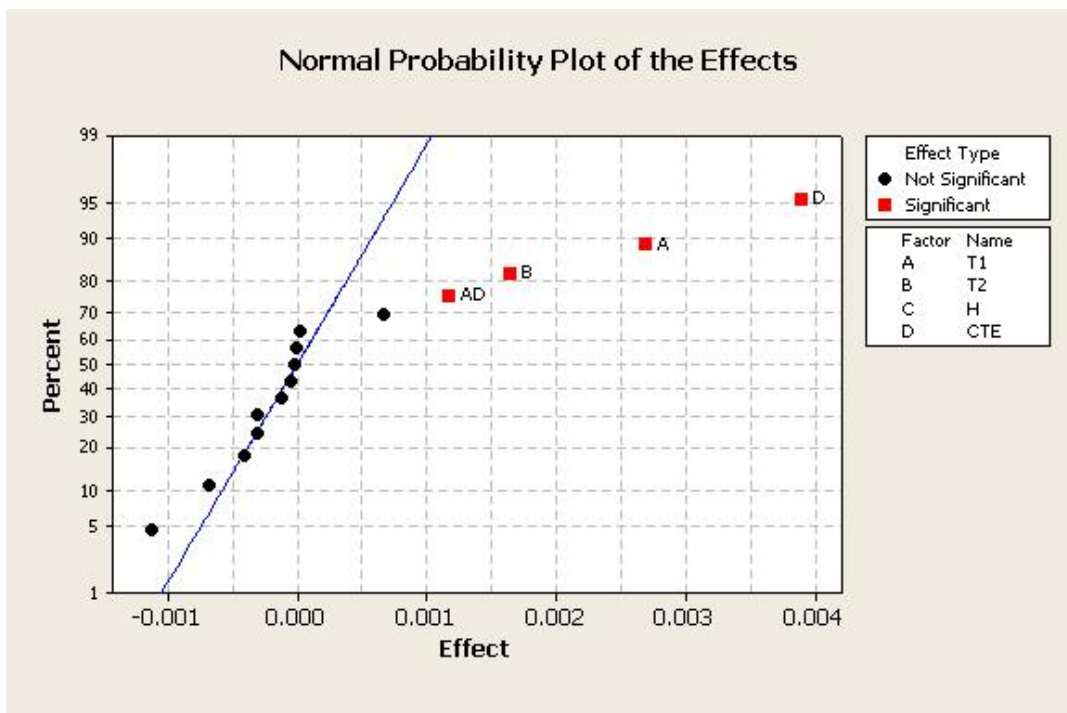
generated quadratic polynomial approximation. These methods have shown that the above polynomial approximation provides a good fit. In Figure 3.8 the volume-weighted incremental equivalent plastic strain values predicted by Equation (3.4) are plotted against the actual values from simulation results. Clearly we can see that the quadratic polynomial approximation gives acceptable accuracy. The coefficient of determination,  $R^2$ , is also a measure of the accuracy of the surrogate model fit. When the surrogate model is a perfect fit,  $R^2$  is equal to one. The  $R^2$  value for the above derived quadratic polynomial surrogate model is 0.989, showing a good fit between the surrogate model and the simulation results at all the design points.



**Figure 3.8 Predicted values VS simulation results**

The normal probability plot in Figure 3.9 shows us the effects of various factors and helps us to identify the significant main effects and interactions. This plot

illustrates estimates of the factor effects on a normal probability paper. The x-coordinate of the paper represents the slope of the line joining the two values of system responses at the two levels of a factor. The y-coordinate represents the probability of a data point being less than or equal to a particular value. This is based on the cumulative normal distribution [42]. The unimportant factor effects tend to lie along a straight line while the significant effects will lie away from the straight line. From Figure 3.9 clearly we can see that the CTE, T1, T2, and T1×CTE effects are significant. Figure 3.10 also serve as a proof of the above conclusion.



**Figure 3.9 Normal probability plot of factor effects**

One of the benefits of a surrogate model is that it can be used to perform sensitivity analysis. The sensitivities of all the design factors and their interactions are shown

in Figure 3.10. The Pareto plot is an ordered bar chart of the normalized coefficients in the quadratic polynomial surrogate model. To obtain normalized coefficients, the coefficients in the original polynomial model are first scaled. Scaling is performed so that the contributions of design factors can be compared more fairly since both the magnitude of the factors and the amount they are varied affect the data used in constructing the surrogate model. To obtain the scaled coefficients, the factor values are scaled to range from -1 to 1 and least squares fit is performed on this data. The scaled coefficients are listed in Table 3.8. After this, the normalized coefficients can be calculated using Equation (3.5),

$$N_i = \frac{S_i}{\sum_{i=1}^j |S_i|} \times 100\% \quad (3.5)$$

where  $N_i$  is the normalized coefficient of the  $i$ -th term in Table 3.8,  $S_i$  is the scaled coefficient of the  $i$ -th term in Table 3.8 and  $j$  is the total number of terms in the polynomial model.

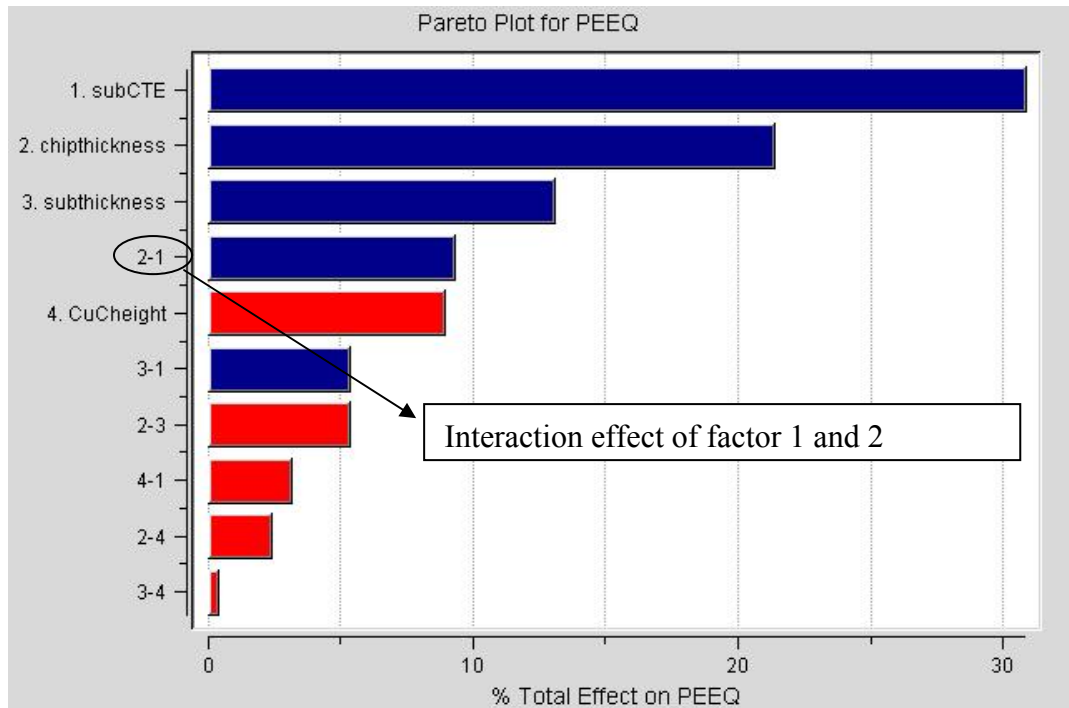
Those bars in Figure 3.10 represent the % total effect on the system response, which is  $\Delta\varepsilon_{avg}$  in the current context. Therefore, the Pareto plot gives a quantitative characterization of the factor effects and interactions on the value of  $\Delta\varepsilon_{avg}$ . From Figure 3.10 we can also identify that the significant effects are from substrate CTE, chip thickness (T1), substrate thickness (T2), and interaction of substrate CTE and chip thickness. It can be seen that increasing the substrate CTE, chip thickness,

substrate thickness will increase  $\Delta\varepsilon_{avg}$ , i.e. decrease the solder joint fatigue life, whereas increasing the CuC height will tend to decrease the value of  $\Delta\varepsilon_{avg}$  or increase the solder joint fatigue life.

**Table 3.8 List of unscaled and scaled coefficients**

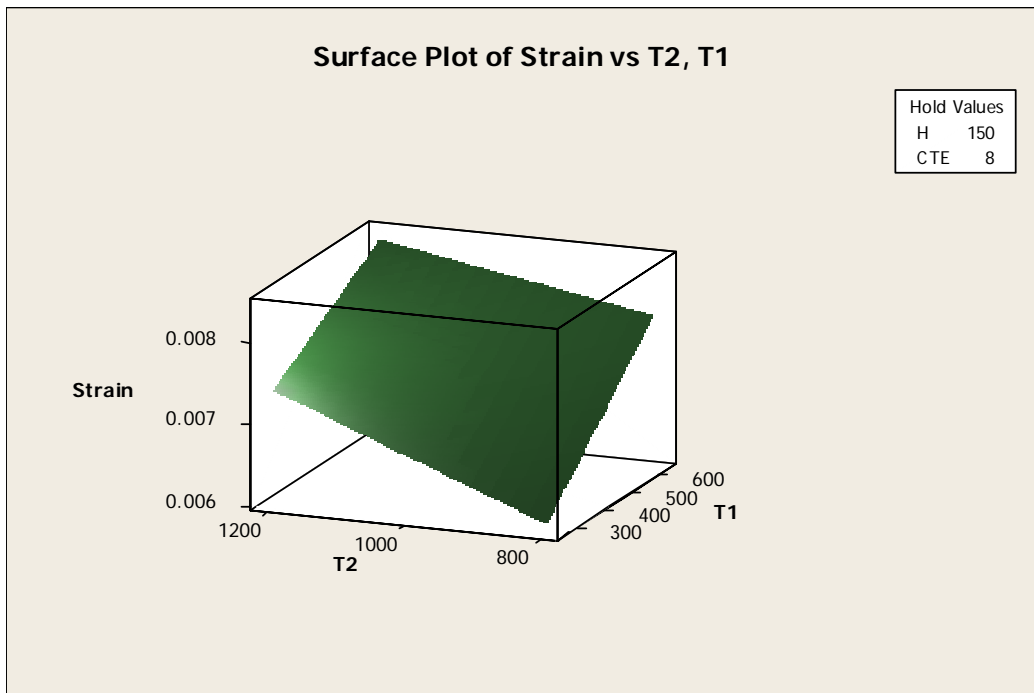
i	Factor	Coefficients	Scaled
1	constant	-0.000139423076922915	0.0097375
2	T1	-7.69230769230764e-006	0.00135
3	T2	-6.5865385113284e-006	0.000824999995529652
4	H	6.81923096999526e-005	-0.000562499975785613
5	CTE	-7.82051283749752e-005	0.00194999994710088
6	T1×T2	-8.65384587086737e-009	-0.0003375
7	T1×H	-3.07692307978868e-008	-0.00015
8	T1×CTE	3.01282061263919e-006	0.0005875
9	T2×H	-4.99999987368938e-009	-2.49999993684469e-005
10	T2×CTE	1.68750004377216e-006	0.000337500008754432
11	H×CTE	-7.999999797903e-006	-0.000199999994947575



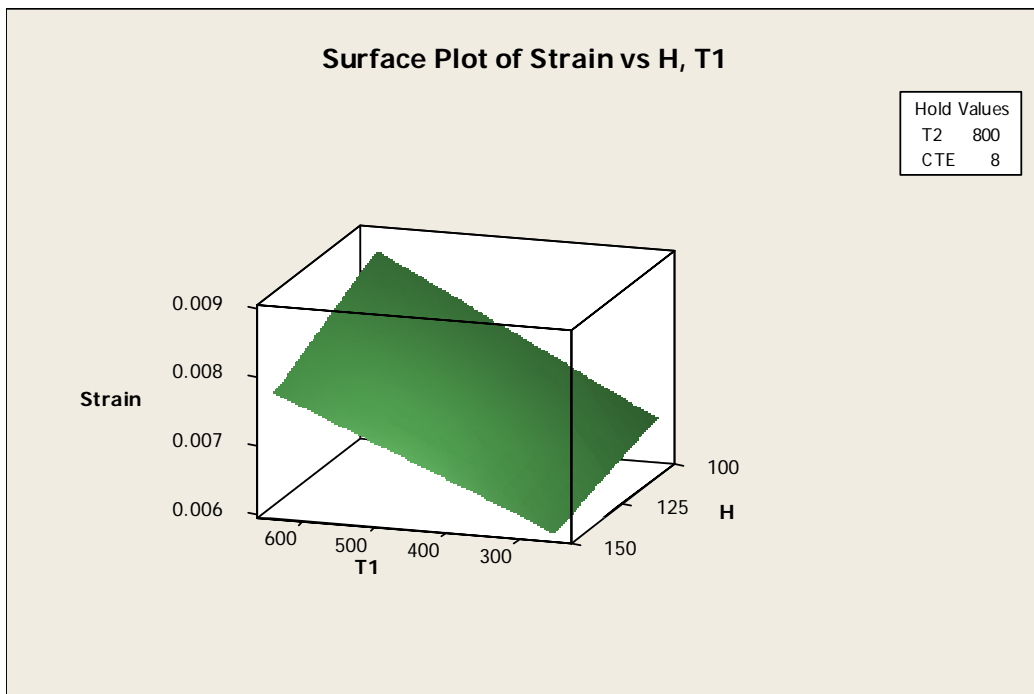


**Figure 3.10 Influences of design factors and interactions on  $\Delta\varepsilon_{avg}$  value**

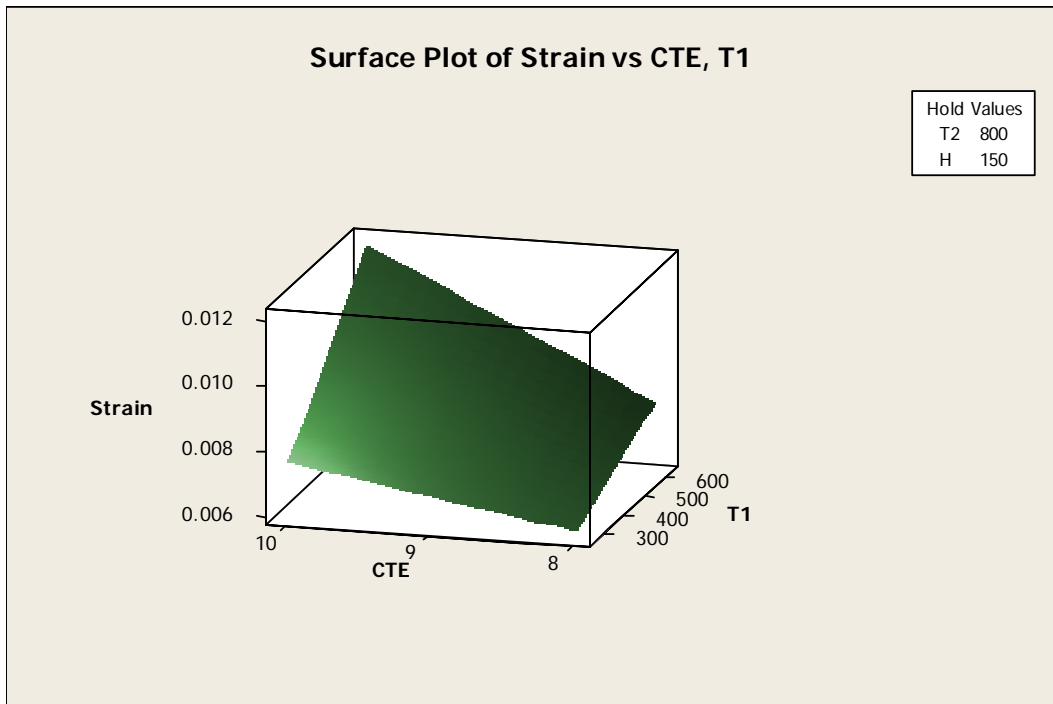
Figure 3.11 from (a) to (f) illustrate the response surface plots between incremental equivalent plastic strain  $\Delta\varepsilon_{avg}$  and any two of the four design factors (while the other two factors are held at their optimal values). From the above response surface plots and Figure 3.10, it is not difficult to find that increase of chip thickness, substrate thickness and substrate CTE will increase the value of  $\Delta\varepsilon_{avg}$  and thus decrease the solder joint fatigue life and increase of the CuC height will decrease  $\Delta\varepsilon_{avg}$  and thus increase solder joint fatigue life. Both the above finding and the optimization result from Minitab show that the optimal design factor combination should be low-level chip thickness, substrate thickness, substrate CTE and high-level CuC height.



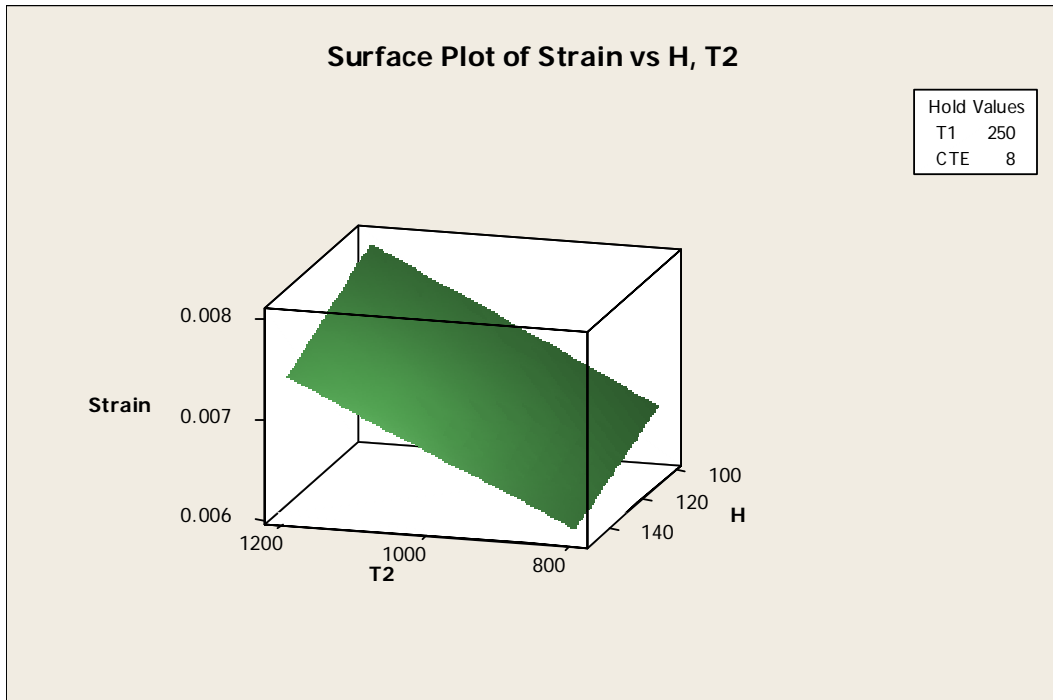
**Figure 3.11(a) Response surface plot of  $\Delta\epsilon_{avg}$  vs. chip thickness and substrate thickness**



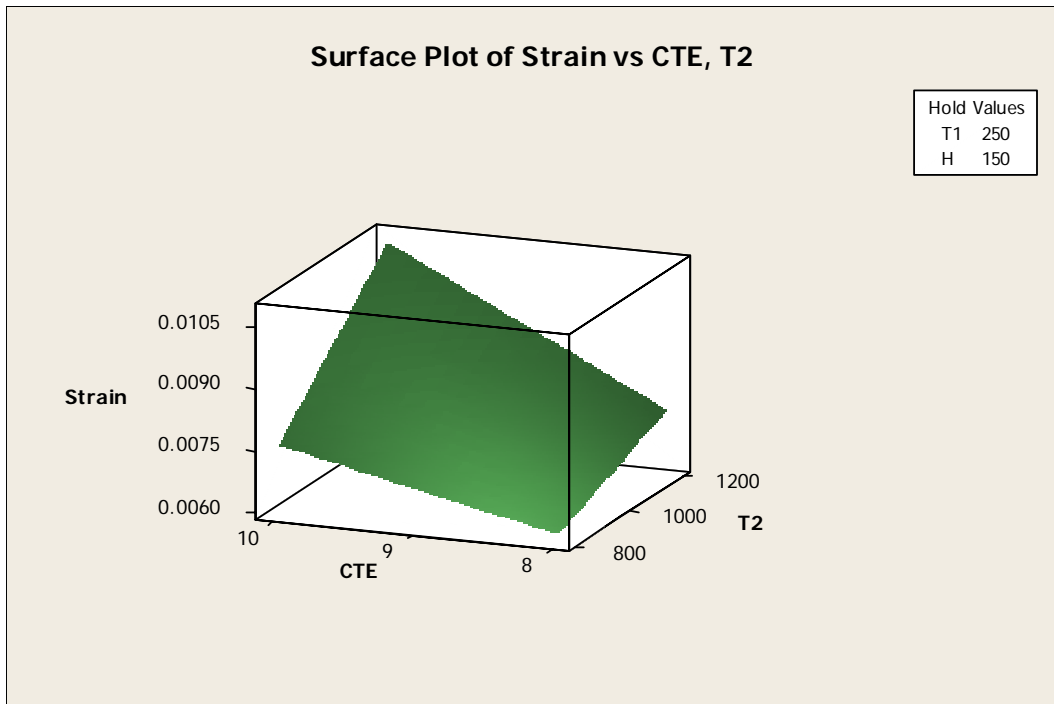
**Figure 3.11(b) Response surface plot of  $\Delta\epsilon_{avg}$  vs. chip thickness and CuC height**



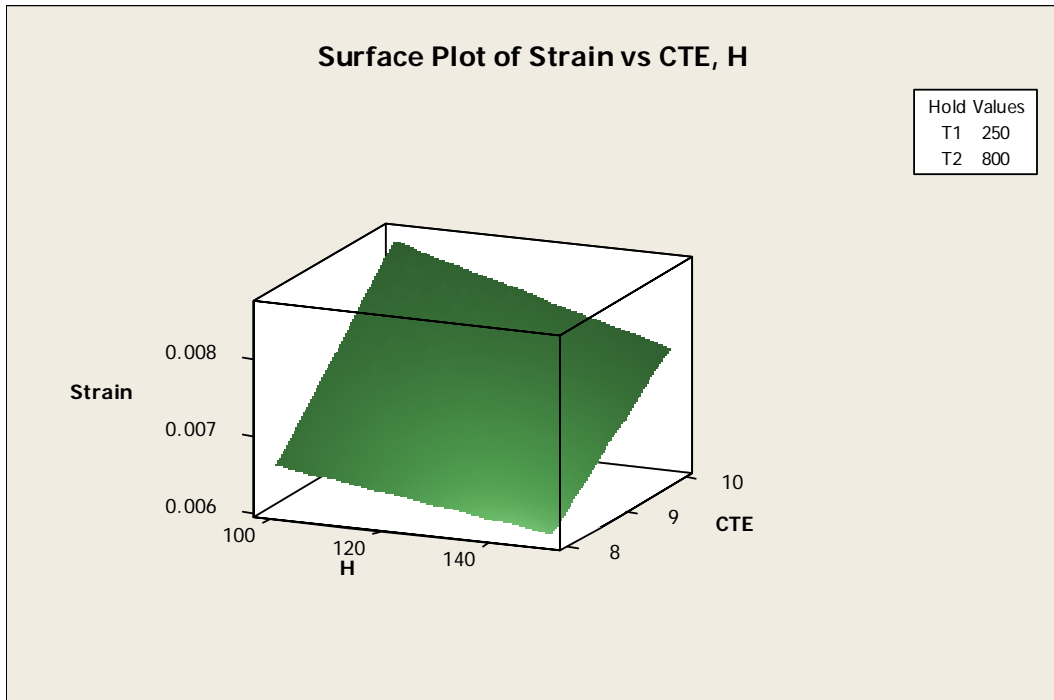
**Figure 3.11(c) Response surface plot of  $\Delta\varepsilon_{avg}$  vs. chip thickness and substrate CTE**



**Figure 3.11(d) Response surface plot of  $\Delta\varepsilon_{avg}$  vs. substrate thickness and CuC height**



**Figure 3.11(e) Response surface plot of  $\Delta\varepsilon_{avg}$  vs. substrate CTE and substrate thickness**



**Figure 3.11(f) Response surface plot of  $\Delta\varepsilon_{avg}$  vs. CuC height and substrate CTE**

### **3.4 Summary and Conclusion**

In this chapter, we briefly talked about the difference between the traditional design process and the current state-of-the-art Simulation-based Design Optimization process. The detailed steps on how to conduct simulation-based design optimization are explained and a brief literature survey in the context of solder joint reliability of electronic package is done for each of the steps. The simulation-based design optimization is adopted in our work to investigate the CuC interconnect. The purposes are to: 1) study the effect of each design factor and 2) find the optimal set of design factors that leads to optimal solder joint fatigue reliability. It is found that the substrate CTE has the largest influence on the solder joint fatigue reliability as the CTE mismatch between chip and substrate is the dominant force that drives solder joint fatigue failure. The chip thickness has the second largest influence on solder joint fatigue life and a smaller chip thickness leads to better solder joint fatigue reliability. The substrate thickness plays the third important role in determining solder joint fatigue life and a thinner substrate thickness gives longer fatigue life. It is also found that increasing CuC height will result in better solder joint fatigue performance. Finally we find that the optimal set of design factors is: low-level substrate CTE, chip and substrate thickness, and high-level CuC height.

## **CHAPTER 4: Fatigue Life Estimation of CuC Interconnect**

### **4.1 Finite Element Modeling**

#### **4.1.1 Introduction**

CuC interconnect as illustrated in Figure 1.2 and 3.2 is a candidate interconnect solution to the 100 $\mu$ m pitch wafer level packaging in our Nano Wafer Level Packaging program. In this interconnect technology electroplated CuC is soldered to the solder pad on the substrate. Thermo-mechanical reliability concern arises because the difference of CTE between the chip and substrate causes the solder joint to experience cyclic strain changes resulting in low cycle fatigue failure during temperature cycling.

In chapter 3, we have done a Simulation-based Design Optimization study on CuC interconnect. Effects of various design factors have been characterized and the optimal parameter setting has been identified. The emphasis of this chapter will be put on the fatigue life estimation of the CuC interconnect in a 20mm by 20mm wafer level package with 100 $\mu$ m pitch. The motivation of this work comes from the interest of conducting FEA to evaluate the fatigue life of this new interconnect before any physical prototype is made and experiments carried out.

#### **4.1.2 Difficulty in FEA**

The immediate difficulty of fatigue life estimation of the CuC interconnect is the lack of efficient and accurate finite element modeling methodology. With the

proposed chip size of 20mm by 20mm and pitch of 100 $\mu$ m, a fully populated package with 40000 interconnects has to be modeled in our finite element simulation. 2D plane strain, plane stress and axisymmetric elements can be used to simplify the original 3D problem into a 2D problem. However, it is well-known that this simplification introduces errors in the predicted results due to the difference between the underlying assumption of plane stress, plane strain and axisymmetric problems and the boundary and loading conditions the package actually undergoes [59]. For example, with the assumption of 2D modeling, the thermal stress and deformation of the chip are independent of the substrate size [59]. This is clearly not the case in real 3D models. Although 2D elements are ideal for occasions such as design optimization where qualitative analysis is good enough, they are not suitable for accurate fatigue life estimation where accurate stress/strain results are desirable. Therefore, 2D elements will not be used in the solder joint fatigue life estimation of the CuC interconnect in this chapter.

3D models constructed using solid elements is favored. Given the symmetry condition, reduction of a full 3D model can be achieved by modeling only one quarter or one eighth of the package. However, the large difference between chip/substrate and interconnect size and nonlinearity of material properties still result in a prohibitively large finite element model. Although the strip model and sector model used by some researchers can further reduce the 3D model size, this reduction is quite limited in the light of our chip and pitch size; the model size is

still computationally prohibitive [9]. Besides, the sector model and the strip model use inaccurate boundary conditions for the simulation analysis and will inevitably introduce errors in the results.

#### **4.1.3 Shell-and-Beam Model**

Since the traditional finite element model using solid elements is not feasible in analyzing our package, we have to turn to other ways. Given the geometrical parameters of the package, we find that for the chip and substrate their in-plane dimension is much greater than their out-of-plane dimension, which means we can model the chip and substrate as shell structures. Moreover, in view of the high aspect ratio of the CuC interconnects, we can probably model them as beams. Since a shell-and-beam model can only provide global deformation results of the entire package, not the detailed stress/strain results at the solder joint of the critical interconnect, a macro-micro modeling approach needs to be adopted.

The idea of using shell and beam elements to model the global deformation of the entire electronic package and a detailed micro model to analyze the critical interconnect is not new. Corbin [60] is the first researcher who used shell-and-beam model to model the global deformation of a C<sup>4</sup> technology electronic package. In his model, the equivalent beams representing the original C<sup>4</sup> solder balls are connected to the mid-plane of the chip and substrate which are modeled with shell elements. Clearly, however, this is not the real case where solder balls



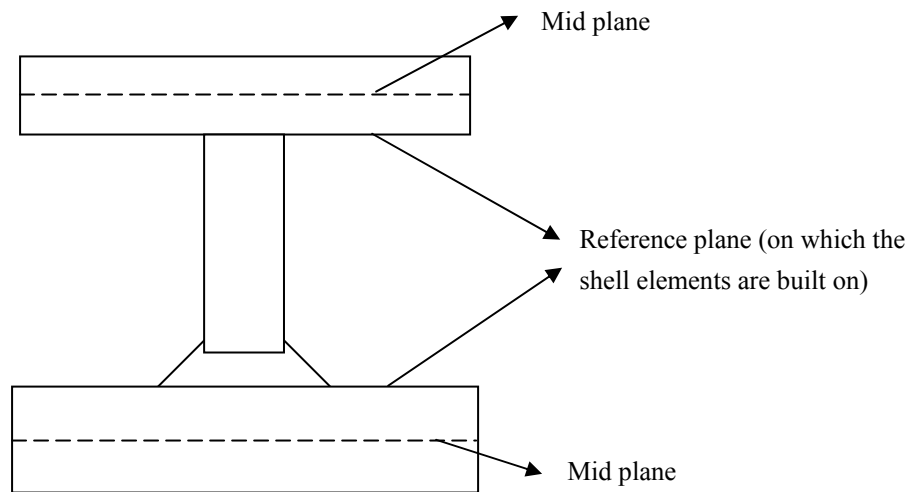
are actually connected to the lower surface of chip and the upper surface of substrate. Moreover, in his work when the micro model of the critical interconnect is analyzed, it is not clear how the deformation results from the global shell-and-beam model are extracted and applied as the boundary conditions of the micro model. Despite this Corbin's methodology has been used by Ju et al [61] and Chan [62] in their research work. Cheng et al [63] improved Corbin's modeling methodology and provided the details of deriving an equivalent beam for the solder ball. In his work, a three-section beam was used as the equivalent beam. The length of the beam was derived using beam theory. Other geometrical parameters of the beam and material properties were derived using Design of Experiment based optimization and the force-displacement curves at different temperatures from the original solder ball. Yuan [64] further improved the equivalent beam derivation method. In his work, the equivalent beam has the same height as the original solder ball and the two ends of the beam have the same diameter as the chip-side and substrate-side pads. However, Yuan did not simply the chip and substrate as shell structures. Instead, the chip and substrate are still modeled using 3D solid elements and the equivalent beams are connected to them using multi-point constraint (MPC) technique. In our analysis, due to the shear number of interconnects to be modeled, it is impossible to construct the chip and substrate using 3D solid elements and use MPC method to connect them.

In our Nano Wafer Level Packaging program, Chng [9] developed a new and convenient method to derive the equivalent beam in her analyses of BON and SSC interconnects. The main advantages of her method over the original Corbin's method are [9]:

- The force-displacement behavior of the original interconnect is estimated under the combined influence of displacement and temperature loadings. This eliminates the need to estimate the force-displacement behaviors at different temperatures.
- The equivalent beam only varies the geometry but not the material properties. In contrast, Corbin's method is much more involved because both the geometry and material properties of the equivalent beam are derived based on complex optimization method.

Therefore, in the current work of fatigue life estimation of the CuC interconnect, Chng's equivalent beam derivation method will be used.

In the micro model analysis of the critical interconnect, unlike the other researchers who included part of the chip and substrate in their micro model, Chng used a micro model that only contained the interconnect itself. This is consistent with the fact that in Chng's global shell-and-beam model the reference surface of the shell elements is offset to the interfaces of interconnect/chip and interconnect/substrate (see Figure 4.1).



**Figure 4.1 Schematic picture of the reference plane of the shell elements**

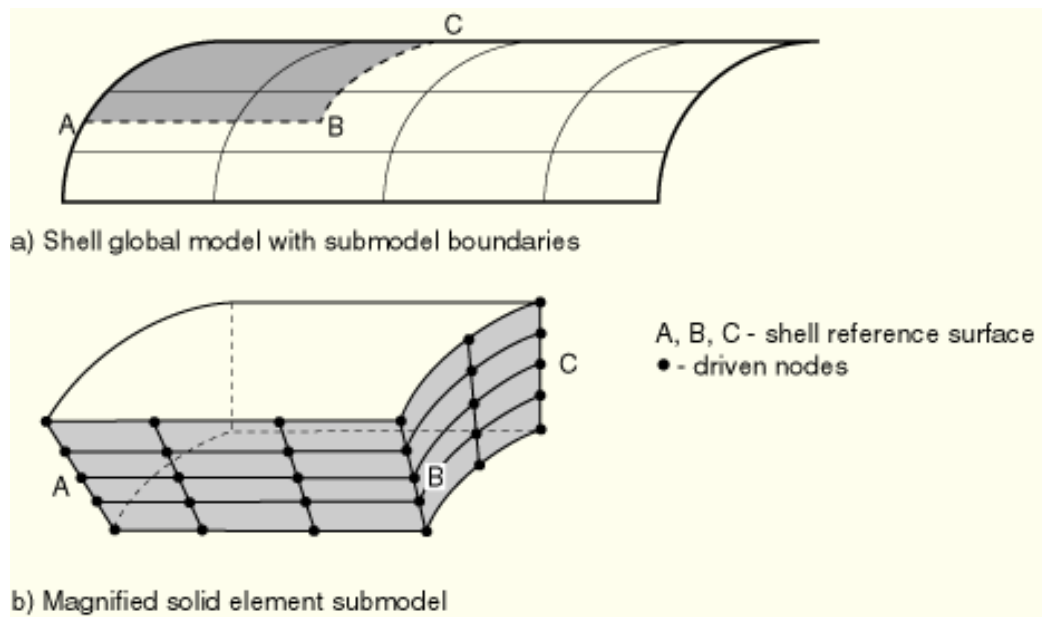
Since the micro model only includes the interconnect itself, the immediate drawback is that the local mismatch effect at the chip/interconnect and substrate/interconnect interfaces cannot be accounted for. Another drawback in Chng's micro model analysis is that the displacement results from the global shell-and-beam model are difficult to be transferred onto the micro model. To overcome this, Chng assumed that the top surface of the interconnect can only move parallelly like a rigid surface with respect to the bottom surface [9]. With this assumption, the nodal displacement results of the equivalent beam in the global model may be easily transferred to the 3D micro model. However, this assumption is not tenable since the top surface of the interconnect may not always move parallelly to the bottom surface during thermal cycling.

In this work, two new modeling techniques, namely shell-to-solid submodeling and shell-to-solid coupling [65], currently available in ABAQUS are adopted to overcome the above disadvantages of Chng's micro modeling method.

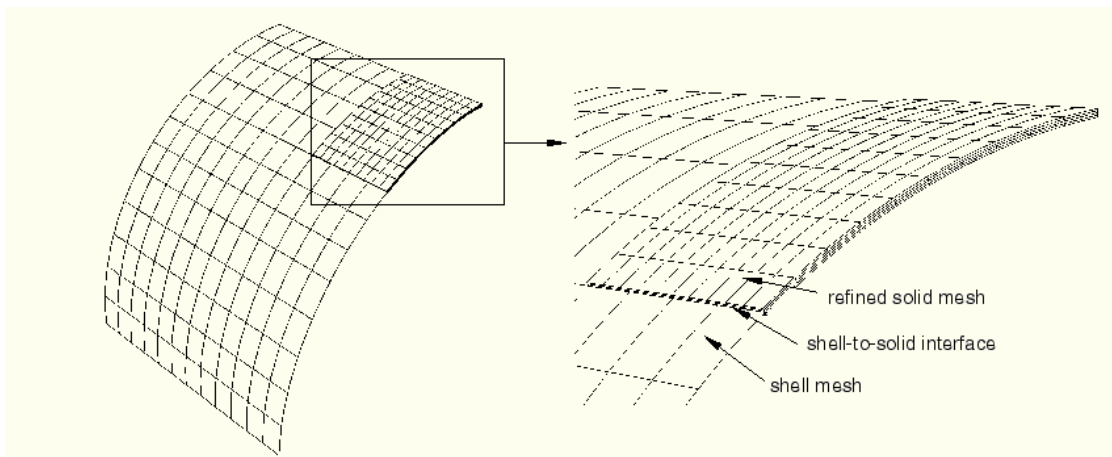
#### **4.1.4 Shell-to-Solid Submodeling and Coupling**

In ABAQUS, submodeling technique is used to investigate a local part of a model with a refined mesh based on interpolation of the solution from an initial, relatively coarse, global model. By specifying the driven nodes in the submodel of the critical CuC interconnect, ABAQUS will automatically search the global shell-and-beam model in the vicinity of the submodel for the necessary displacement results and interpolate those results onto the nodes on the appropriate parts of the boundary of the submodel. Thus, the response at the boundary of the submodel is defined by the solution for the global shell-and-beam model [65]. The driven nodes and any loads applied to the submodel determine the solution in the submodel. Figure 4.2 illustrates the relationship between global model and submodel.

Shell-to-solid coupling technique, however, does not require a separate analysis of the submodel. This technique allows for a transition from shell element modeling to solid element modeling and is most useful when local modeling should need a full three-dimensional analysis but other parts of the structure can be modeled as shells [65]. A typical shell-to-solid coupling finite element mesh is shown in Figure 4.3



**Figure 4.2 Shell-to-solid submodeling [65]**



**Figure 4.3 Shell-to-solid coupling [65]**

## 4.2 Feasibility Analysis

### 4.2.1 Modeling Methodologies

Based on the discussion in section 4.1, the modeling methodologies that will be used in this work are described as follows:

The chip and substrate are simply modeled as shell structures and interconnects as beams by taking advantage of their geometrical characteristics. Since the shell-and-beam model can only provide good global deformation results not the detailed stress-strain results, shell-to-solid submodeling or shell-to-solid coupling will be adopted to obtain the detailed stress-strain results. In the modeling methodology using shell-to-solid submodeling technique, a global shell-and-beam model for the entire package based on the above mentioned simplification is first analyzed. Then a detailed submodel analysis of the critical interconnect is conducted using the shell-to-solid submodeling capability in ABAQUS to obtain a detailed stress/strain solution at the solder joint. In the modeling methodology that uses shell-to-solid coupling technique, the corner part of the package which includes the critical interconnect is modeling using 3D solid elements and other parts of the package will still be modeled using shell elements and beam elements. The transition from shell elements to solid elements are implemented using shell-to-solid coupling capability in ABAQUS. To differentiate the methodology using shell-to-solid submodeling technique and the one using shell-to-solid coupling technique, those two modeling methodologies are named shell-and-beam-submodeling and shell-and-beam-coupling, respectively.

Before the application of those two modeling approaches on our package, a smaller dummy package is modeled and studied to demonstrate the feasibility and accuracy of those two proposed modeling approaches. A small package is chosen

because a full 3D finite element model is still feasible to analyze the package. In this demonstration, a full 3D model is built up using 3D solid elements. Results from the full 3D model are used as the benchmark to testify the results obtained from shell-and-beam-submodeling and shell-and-beam-coupling models.

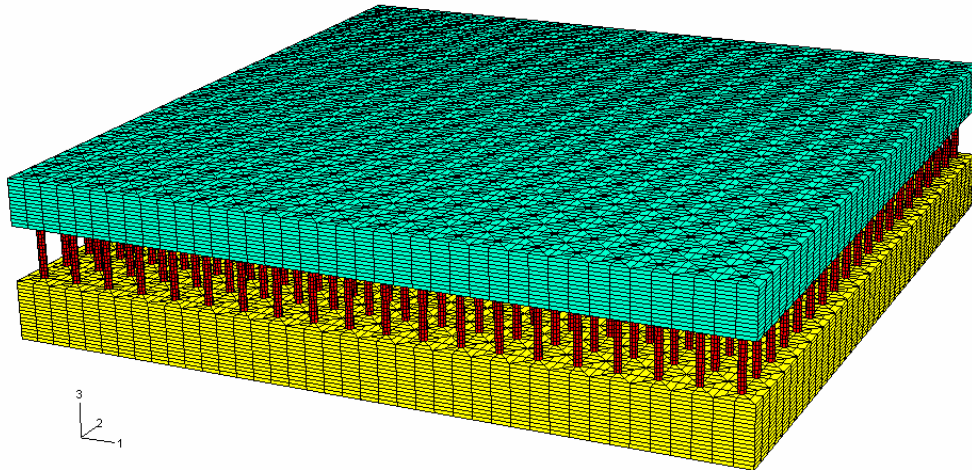
### **4.2.2 The Dummy Package**

#### **Full 3D Model**

In this study, a small dummy package is investigated. The package is made to be small to make sure current computation resources are adequate to analyze the 3D finite element model built with 3D solid elements. Details of the geometrical parameters of the dummy package in the feasibility analysis are listed in Table 4.1. The chip thickness and substrate thickness are shrunk to be equal to one-fifth of the original size in the 20mm by 20mm package. This to make sure that the simplification of chip and substrate as shell structures is still tenable. The 3D mesh of the package is shown in Figure 4.4. Due to symmetry, only one quarter of the entire package is modeled. In all the finite element models using 3D solid elements, C3D8 first-order element in ABAQUS is used. The loading is a temperature drop from 125 °C to -40 °C. The boundary conditions are prescribed according to the symmetry condition such that the nodes on the quarter-symmetry plane cannot move out-of-plane. In order to prevent rigid body motion of the package a node at the neutral line is fixed.

**Table 4.1 Geometrical parameters of the dummy package**

Package size (mm)	4mm by 4mm
Interconnect pitch ( $\mu\text{m}$ )	100
Chip thickness ( $\mu\text{m}$ )	128
Substrate thickness ( $\mu\text{m}$ )	160
CuC height ( $\mu\text{m}$ )	150
CuC diameter ( $\mu\text{m}$ )	20
Substrate CTE (ppm/K)	10

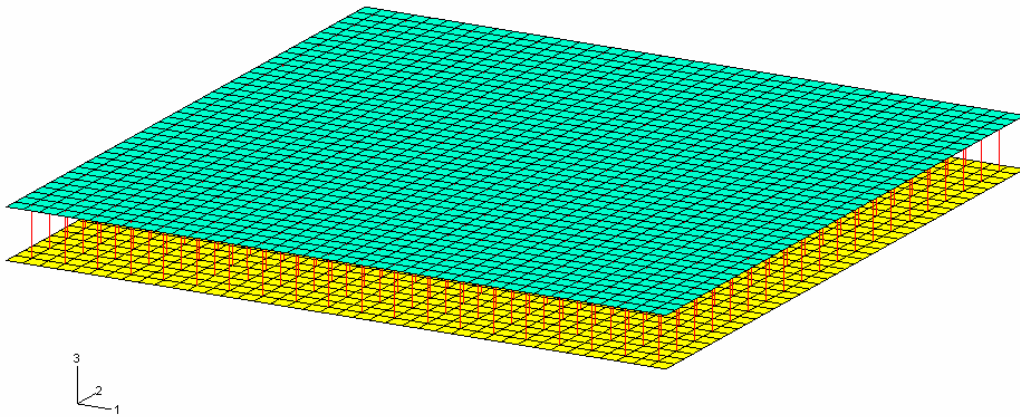
**Figure 4.4 Finite element mesh of the dummy package**

### Shell-and-Beam-Submodeling

In the shell-and-beam-submodeling approach, a global shell-and-beam model representing the entire dummy package is firstly built, then a submodel analysis of the critical interconnect is performed using ABAQUS shell-to-solid submodeling capability.



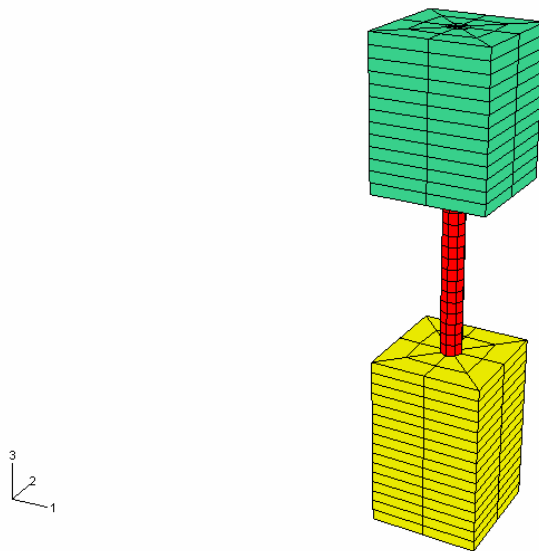
The global shell-and-beam finite element model is shown in Figure 4.5. The chip and substrate are modeled using S4R shell elements in ABAQUS, with reference planes offset away from their mid-planes as shown in Figure 4.1. The CuC interconnects are modeled using B32 Timoshenko beam elements with the length and diameter as prescribed in Table 4.1. The loading is a temperature drop from 125 °C to -40 °C. The boundary conditions of the shell-and-beam model are similar with the full 3D model. The nodes on the quarter-symmetry plane cannot move out-of-plane. In order to prevent the rigid body motion of the package a node at the neutral line is fixed.



**Figure 4.5 Finite element mesh of the global shell-and-beam model**

After the global shell-and-beam model analysis, the submodel for the critical interconnect must be analyzed to obtain the detailed stress-strain solution of the solder joint. The mesh of the submodel of the critical interconnect is shown in Figure 4.6. C3D8 first-order continuum solid element in ABAQUS is used for the

finite element model construction. The boundary condition of the submodel is applied by specifying the driven nodes in this submodel. Then ABAQUS will automatically search the global shell-and-beam model in the vicinity of the submodel for the necessary displacement results and interpolate those results onto the driven nodes of the submodel. Therefore, the response at the boundary of the submodel is defined by the solution for the global shell-and-beam model. The driven nodes and any loads applied to the submodel determine the solution in the submodel.

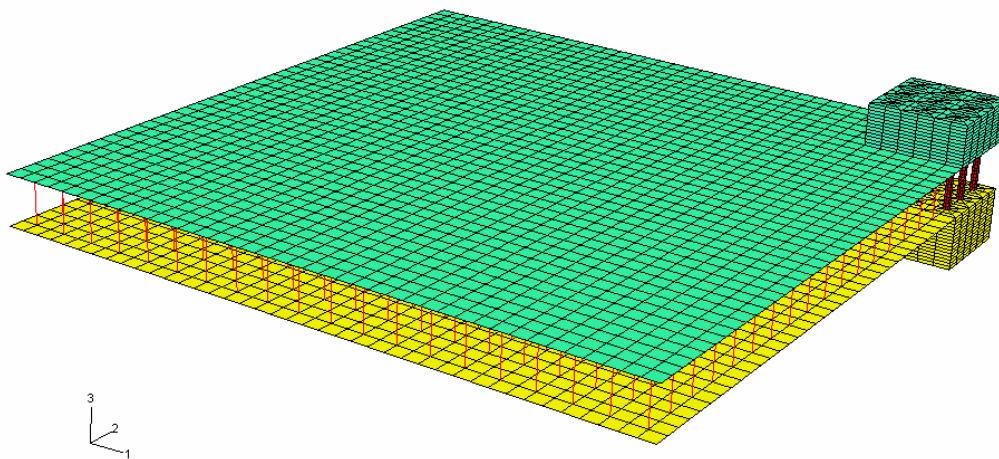


**Figure 4.6 Finite element mesh of the submodel of the critical interconnect**

### **Shell-and-Beam-Coupling**

In shell-and-beam-coupling model, the simplification of chip and substrate as shell structures is still used. However, the corner part of the package which contains the critical interconnect is modeled with details using 3D solid elements (C3D8 first-order continuum solid element in ABAQUS). The shell part and the corner part are

coupled using shell-to-solid coupling technique in ABAQUS. Same as the full 3D model, the loading of the shell-and-beam coupling model is a temperature drop from 125 °C to -40 °C and the boundary conditions are prescribed according to the symmetry condition such that the nodes on the quarter-symmetry plane cannot move out-of-plane. In order to prevent rigid body motion of the package a node at the neutral line is fixed.



**Figure 4.7** Finite element mesh of the shell-and-beam-coupling model

### **Results and Discussion**

Figure 4.8-4.10 shows the displacement contour plots of the chip in our three different finite element models, the full 3D model, the global shell-and-beam model for submodel analysis, and the shell-to-solid-coupling model, respectively. We can see that the global shell-and-beam model and shell-to-solid-coupling model provide good agreement with the full 3D model in terms of package

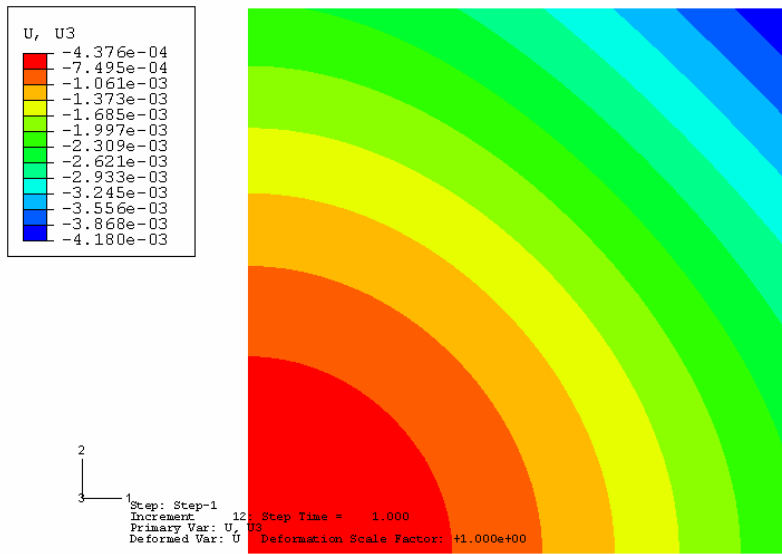
deformation. Table 4.2 further lists the maximum displacement values of the three models. We can see that the global shell-and-beam model gives better package deformation results than the shell-to-solid-coupling model and both of them produce an error of about 13%, which is acceptable. Figure 4.11 shows us the displacement results along the package diagonal from the center of package to the critical interconnect (corner of package). We can see that the global shell-and-beam model yields almost the same deformation results as the shell-to-solid-coupling model. It is also clear that the discrepancy of displacement results between the simplified models and the full 3D model increases as the distance from the center of package increases. But the maximum discrepancy is only 13.2%, yielded by the shell-to-solid-coupling model. Furthermore, for shell-to-solid submodeling approach the time history deformation results of the global shell-and-beam model must be accurate in order to drive the submodel analysis. Figure 4.12 shows the time history deformation results of the global shell-and-beam model and the full 3D model. We can see that the global shell-and-beam model does yield accurate deformation results that can be used to drive subsequent submodel analysis.

No matter which finite element model we use, the final purpose of the thermo-mechanical analysis is to obtain accurate stress/strain information at the critical (corner) interconnect so that fatigue life prediction can be made based on that information. The above discussion has already shown that the shell-and-beam-

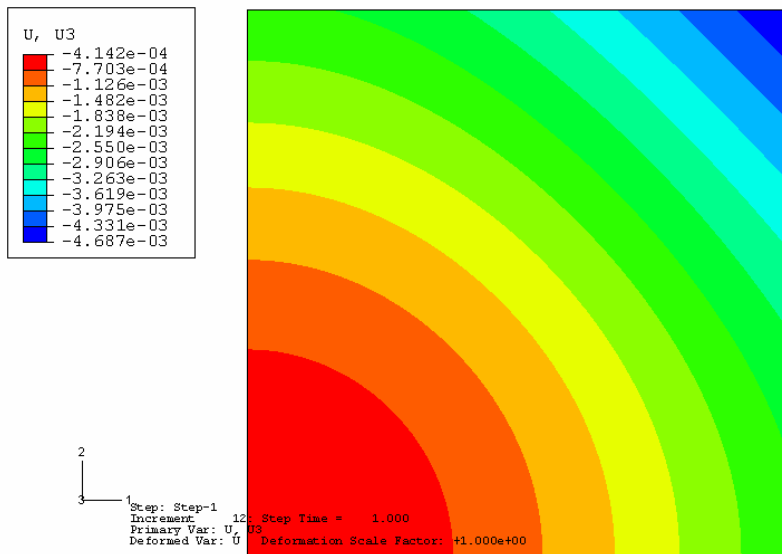
submodeling model and shell-and-beam-coupling model can produce good deformation results. So the next step is to see whether those two simplified models can also produce good agreement with the full 3D model in terms of detailed stress/strain results at the critical interconnect. Figures 4.13 to 4.16 show us the Mises stress distribution contours of the full 3D model, shell-and-beam-submodeling model, shell-and-beam-coupling model, and Chng's micro modeling model, respectively. We can see that the stress contours from the shell-and-beam-submodeling and shell-and-beam-coupling are almost the same as the one from the full 3D model, which means this two simplified model can give very good stress distribution results. In view of the maximum Mises stress, the two simplified model also provide very accurate results. As can be seen from Table 4.3, compared with the full 3D model, the maximum Mises stress values from the shell-and-beam-submodeling and shell-and-beam-coupling only produce an error percentage of 2.4% and 1.1%, respectively, showing that accurate stress/strain results can be expected despite the fact that the two models are very simplified. However, when we compare the stress contours of Figure 4.16 and Figure 4.13, we find that the result derived using original Chng's micro modeling approach is not in good agreement with the one derived using the full 3D model. Especially in the stress concentration areas near the two ends of the CuC interconnect, the stress distribution from micro modeling approach is not comparable with that from the full 3D model. In terms of maximum Mises stress, the micro modeling approach

predicts a much higher value than the full 3D model, producing an error percentage of 15.1% which is much higher than the shell-and-beam-submodeling and shell-and-beam-coupling models.

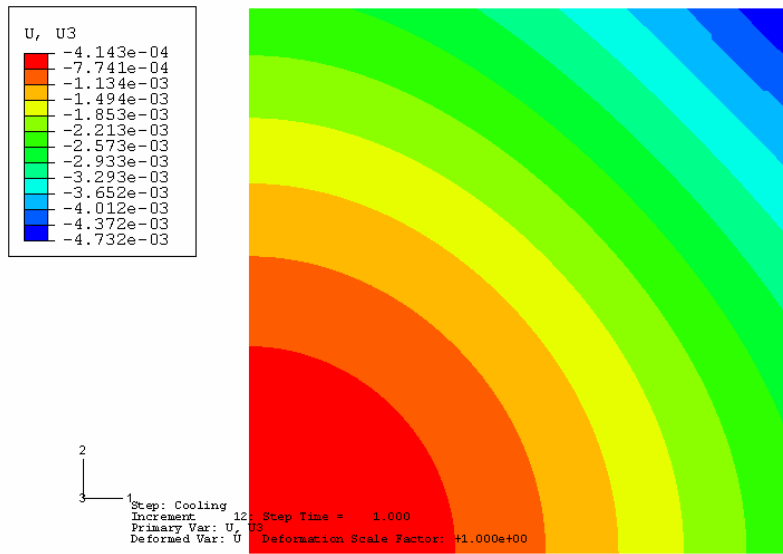
Table 4.4 shows us the computational requirements of various models. We can see that a great saving of computational resources is yielded by the two simplified models compared with the full 3D model, despite the above-mentioned very small errors generated. As can be seen from Table 4.4, the computation time of the shell-and-beam-coupling model is only 1.4% of the time required by the full 3D model. The shell-and-beam-submodeling approach takes even less computation time than the shell-and-beam-coupling approach, which is only 0.27% of the time used by the full 3D model. Similar great savings can also be seen in terms of required memory for computation. The required memories of shell-and-beam-coupling method and shell-and-beam-submodeling method are only 4.6% and 3.3%, respectively, of that needed by the full 3D model.



**Figure 4.8 Displacement (Z-direction) contour of the chip in full 3D model**



**Figure 4.9 Displacement (Z-direction) contour of the chip in global shell-and-beam model**

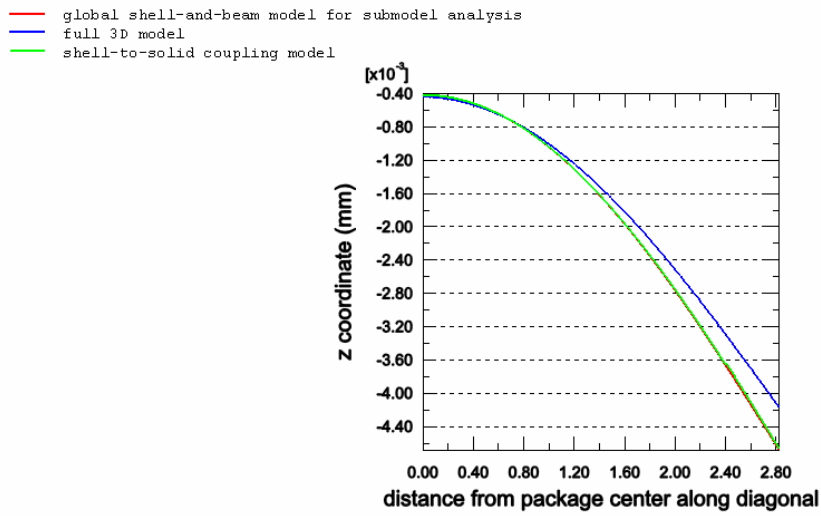


**Figure 4.10 Displacement (Z-direction) contour of the chip in shell-to-solid-coupling model**

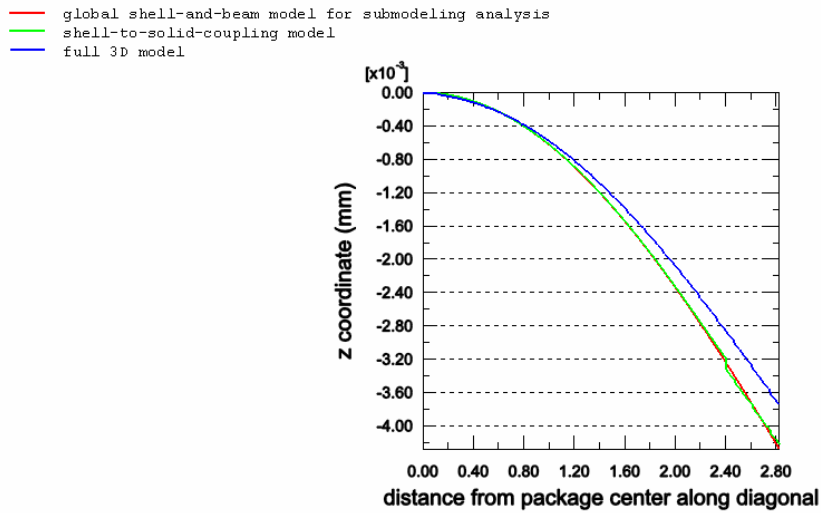
**Table 4.2 Displacement result comparison between the three models**

Model name	Max displacement ( $\mu\text{m}$ )	Error (percentage)
Full 3D model	4.180	N.A.
Global shell-and-beam model	4.687	12.1%
Shell-to-solid coupling model	4.732	13.2%



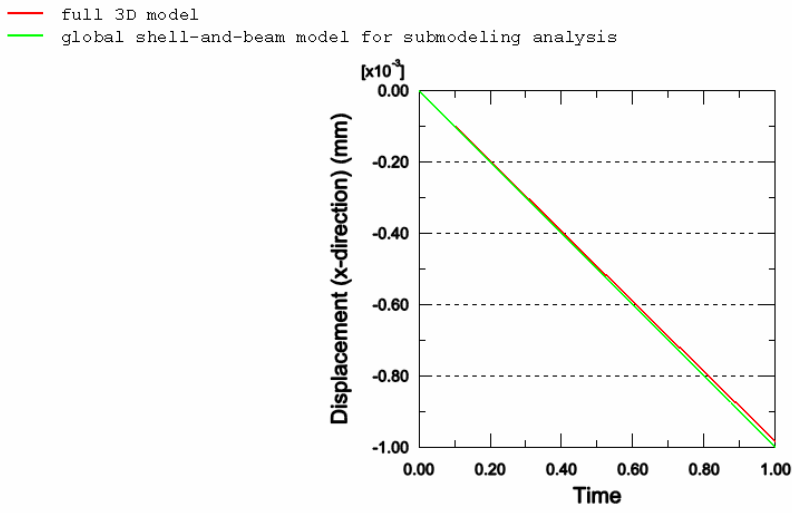


(a)

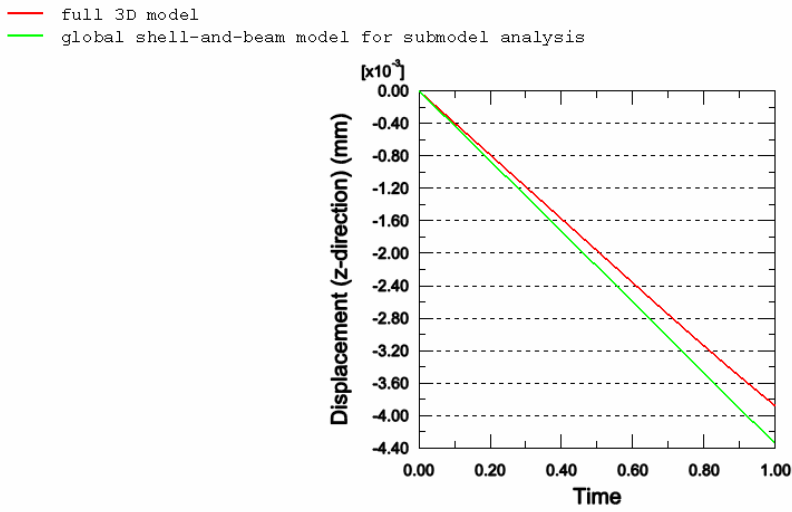


(b)

**Figure 4.11 Comparison of deformed shape of the 4mm by 4mm package after temperature drop from 125 °C to -40 °C. (a) Top of interconnect, and (b) bottom of interconnect**

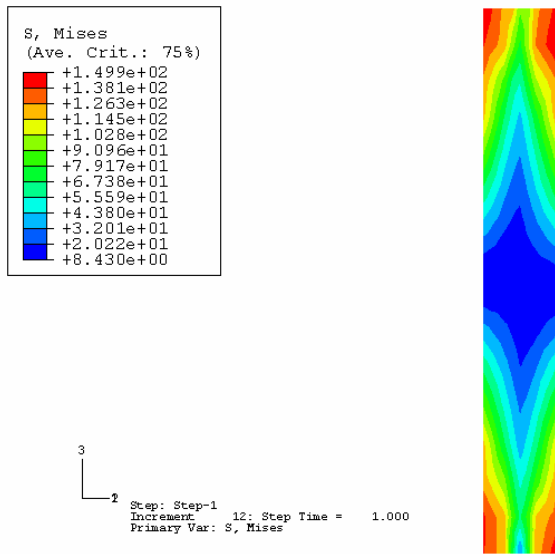


(a)

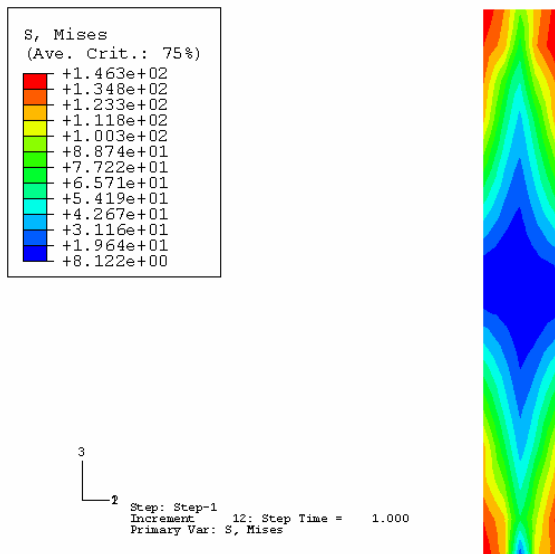


(b)

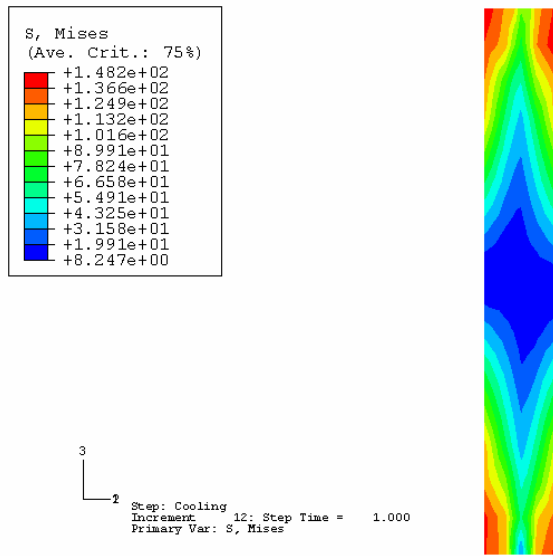
**Figure 4.12 Time history deformation of the global shell-and-beam model and full 3D model**



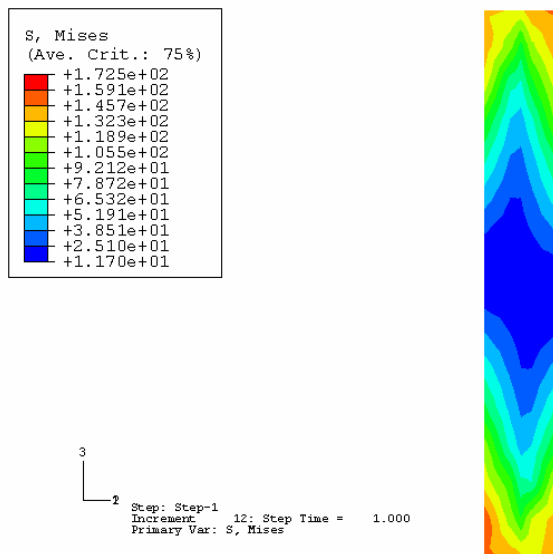
**Figure 4.13 Stress contour plot for the corner CuC interconnect in the full 3D model**



**Figure 4.14 Stress contour plot for the corner CuC interconnect using the shell-to-solid-submodeling approach**



**Figure 4.15** Stress contour plot for the corner CuC interconnect using the shell-to-solid-coupling approach



**Figure 4.16** Stress contour plot for the corner CuC interconnect using the original Chng's micro modeling approach (Chng, 2003)

**Table 4.3 Mises stress result comparison between the four models**

Model name	Max Mises stress (MPa)	Error (percentage)
Full 3D model	149.9	N.A.
Shell-and-beam-submodeling	146.3	2.4%
Shell-and-beam-coupling	148.2	1.1%
Chng's micro modelling	172.5	15.1%

**Table 4.4 Requirements of various models in analyzing a 4mm by 4mm dummy package**

	Case 1	Case2	Case3
Package size	4mm by 4mm		
Number of interconnects modeled	400 (fully populated)		
CuC Interconnect pitch	100 $\mu$ m		
Interconnect size	150 $\mu$ m (height) 20 $\mu$ m (diameter)		
Chip thickness	128 $\mu$ m		
Substrate thickness	160 $\mu$ m		
Stress-free temperature	125 °C		
Temperature changed to	-40 °C		
Analysis type	Elastic-plastic		
Portion of package simulated	One fourth		
Type of elements used	3D solid	3D solid, shell and beam	Shell and beam
Total number of nodes in model	444911	15237	4962 (global model) 1261 (submodel)
CPU time required (second)	39644	559.60	82.47 (global model) 25.52 (submodel)
Memory required (MB)	1190	55.23	24.21 (global model) 16.02 (submodel)

### **4.2.3 Summary and Conclusion**

In section 4.2 various previously used finite element models are reviewed and brief explanations are given why they cannot be used in the current analysis of our wafer level packages. After that a decision is made that shell-and-beam model should be adopted to address the difficulty of modeling our package. Both the origin and progressive development of the shell-and-beam model are reviewed. Since the shell-and-beam model does not provide detailed information of the stress/strain at the critical interconnect, a global-local or macro-micro modeling approach must be used. Subsequently a brief review is given to micro modeling of the critical interconnect. However, those previous micro modeling methods are either inaccurate or infeasible for the current analysis of our wafer level packages. Therefore, two new methodologies that can be used to obtain the detailed stress/strain solution of the critical interconnect are proposed by this thesis. They are named shell-and-beam-submodeling and shell-and-beam-coupling.

A small dummy package is investigated to verify the accuracy the two proposed modeling methodologies. In this verification study, full 3D model, shell-and-beam-submodeling model, shell-and-beam-coupling model and Chng's micro modeling approach are used analyze the dummy packages. Based on this study, the following conclusions can be drawn:

1. Both the global shell-and-beam model and shell-and-beam-coupling model can predict good package deformation under the specified loading condition. Both of them tend to overestimate the package warpage by 13%.
2. The global shell-and-beam model and shell-and-beam-coupling model produce almost the same package deformation results.
3. The discrepancy of deformation results between the simplified models and the full 3D model increases as the distance from package center to package corner increases.
4. Both the shell-and-beam-submodeling and shell-and-beam-coupling approaches give very accurate stress/strain results at the critical interconnect compared to the full 3D model. Chng's micro modeling approach tends to give a less accurate result, producing an error percentage of 15.1%
5. It is feasible to adopt the proposed shell-and-beam-submodeling and shell-and-beam-coupling methodologies in the current thermo-mechanical fatigue life prediction of CuC interconnect in our wafer level packages.
6. The two simplified model give a great saving of computational resources and can be used to analyze large packages at affordable turnaround time.

### **4.3 Fatigue Life Estimation of CuC Interconnect**

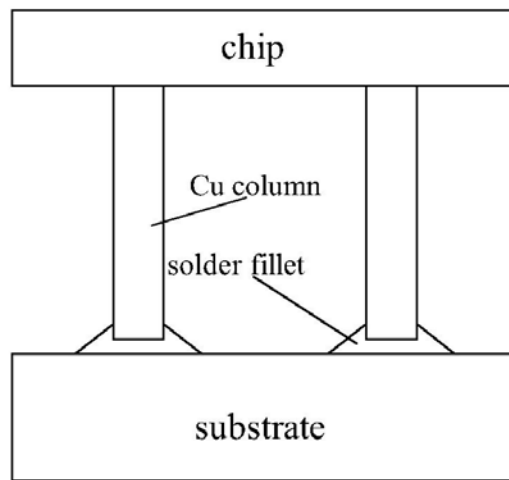
So far, the finite element modeling methodologies for predicting the solder joint fatigue life of CuC interconnect in wafer level package have been proposed and their feasibilities testified. The next stage will be to apply the established modeling methodology in our real wafer level package for solder joint fatigue life estimation. In section 4.1 and 4.2, we have actually developed two modeling methodologies. One is the shell-and-beam-submodeling technology which includes a global shell-and-beam model and a subsequent submodel analysis of the critical interconnect; the other one is the shell-and-beam-coupling method in which the area of interest is modeled using 3D solid elements and the rest is modeled using shell and beam elements. Although both of the two simplified modeling methodologies exhibit good feasibilities in the fatigue life estimation of CuC interconnect, only the shell-and-beam-submodeling will be applied in the next work. This is because the two methodologies generate almost the same results based on section 4.1 to 4.2 and the model set-up time for shell-and-beam-coupling methodology is longer than shell-and-beam-submodeling methodology. Therefore, only the shell-and-beam-submodeling methodology will be adopted in the fatigue life estimation of CuC interconnect in wafer level packages.

#### **4.3.1 The CuC Interconnect and Package under Investigation**

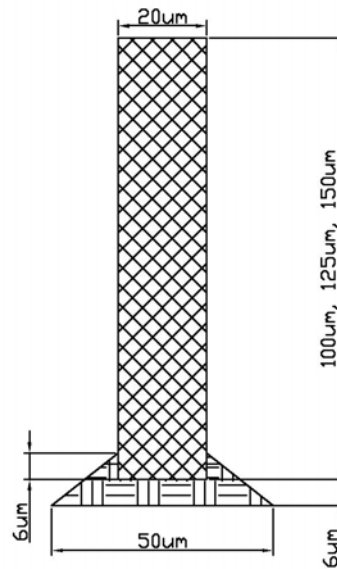
CuC interconnect (Figure 4.17) is a compliant interconnect with one end directly bonded to the chip and the other connected to substrate by eutectic tin-lead solder



joint. The geometrical parameters of the CuC to be investigated currently for solder joint fatigue life estimation are illustrated in Figure 4.18. Chip and substrate are not sketched for clarity. Their detailed dimensions can be found in Table 4.5. The chip size in this package is 20mm by 20mm and is fully populated by CuC interconnects at 100 $\mu$ m pitch, i.e. 40000 CuCs are in one package.



**Figure 4.17 Schematic picture of the CuC interconnect**



**Figure 4.18 Dimensions of CuC interconnect**

**Table 4.5 Details of modeling parameters**

Chip thickness	640 $\mu\text{m}$
Substrate thickness	800 $\mu\text{m}$
Substrate CTE	10ppm/K
Solder gap	6 $\mu\text{m}$
Column wetting height	6 $\mu\text{m}$
Solder pad diameter	50 $\mu\text{m}$
CuC radius	20 $\mu\text{m}$
CuC height variation	100, 125, 150 $\mu\text{m}$
Interconnect pitch	100 $\mu\text{m}$
Chip size	20mm by 20mm

### 4.3.2 Solder Joint Shape Prediction

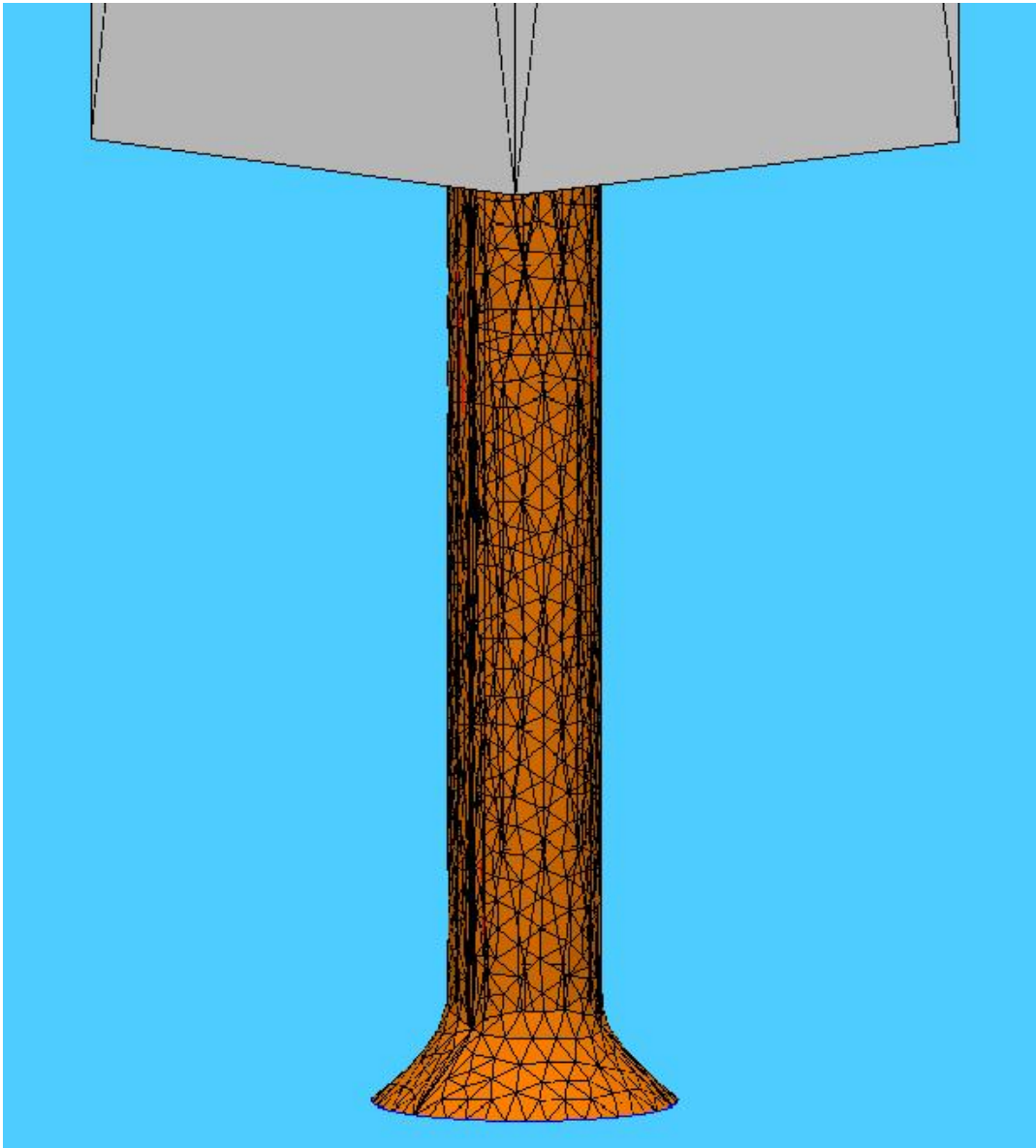
There are various solder joint shape prediction methods in the literature. Those methods can be classified into two categories, analytical methods and numerical methods. For the analytical methods, some of them are geometry-based, others are force-based. The simplest and easiest geometry-based method is proposed by Goldmann [66]. In his method, the solder joint is assumed to be a truncated sphere. Heinrich et al [67] developed a popular force-based analytical method. This method assumes that the solder joint shape is described as a revolution surface whose generating meridian is a circular arc. Although the above-mentioned analytical methods and other analytical methods are useful, they cannot be used in

our solder joint shape prediction of CuC interconnect due to the fact that the CuC interconnect is much more complex than a single solder bump and the fact that those analytical methods are primarily developed for simple solder bump shape prediction. Therefore, numerical methods will be sought for the solder joint shape prediction of CuC interconnect.

Surface Evolver is a software tool based on numerical method that can be used for arbitrary solder shape prediction. It was developed by Ken Brakke as part of the Geometry Supercomputing Project and has been extensively used by various researchers in the electronic packaging realm for solder joint shape prediction. Surface Evolver discretizes an arbitrary surface with area elements, and subsequently minimizes the surface energy. The energy terms to be considered may be determined by the user. Since Surface Evolver has the advantage of being able to predict complex solder shape, it will be used in our solder joint shape prediction of CuC interconnect.

The parameters needed for Surface Evolver to predict the solder joint shape of CuC interconnect are listed in Table 4.6. Based on Table 4.6 and the CuC interconnect dimensions listed in Table 4.5, the solder joint shape predicted by Surface Evolver is shown in Figure 4.19. Note that the chip and CuC are also shown in Figure 4.19. Figure 4.19 shows that the edge of the solder fillet is

slightly curved. However, for ease of modeling, the fillet is assumed to have straight edges as shown in Figure 4.17 and 4.18.



**Figure 4.19 Predicted solder joint shape by Surface Evolver**

**Table 4.6 Parameters used for solder shape prediction by Surface Evolver**

Surface tension of solder	0.49 J/m <sup>2</sup>
Surface energy of copper/solder interface	-0.688 J/m <sup>2</sup>
Density of solder	9280 kg/m <sup>3</sup>
Density of copper	8900 kg/m <sup>3</sup>
Density of chip	2330 kg/m <sup>3</sup>
Volume of solder	1.08×10 <sup>-14</sup> m <sup>3</sup>
Solder pad diameter	50 μm
Chip size	20 mm by 20 mm

### 4.3.3 Equivalent Beam Representation

In a shell-and-beam based model of the electronic package, the CuC interconnect is represented by a beam. However, a beam structure can hardly behave exactly the same under all loading conditions as the original interconnect, i.e. CuC interconnect or traditional truncated sphere solder joint, which is much more complex than a single beam. Therefore, the beam in the shell-and-beam model is only required to represent the original interconnect under certain loading conditions. Such a beam is termed an equivalent beam. In Section 4.1.3 we reviewed and discussed the equivalent beam derivation methods developed by various researchers. For the current work, the equivalent beam derivation method proposed by Chng [9] will be adopted.

In the context of our CuC interconnect, since it is impossible for an equivalent beam to fully represent the behavior of a CuC interconnect, i.e., the responses of an equivalent beam and that of a CuC interconnect cannot always be the same to different loading conditions, the equivalent beam is only required to behave similarly with the CuC interconnect under two major loading conditions: shear loading and axial loading, based on the understanding that CuC interconnect may be subjected to shear in the X direction and is likely to be in tension [9].

The procedures of obtaining such equivalent beams for the three CuC interconnects are the same as the procedures detailed elsewhere [9] and therefore omitted in current work.

Under the combined loading of a temperature decrease from 125 °C to -40 °C and a displacement loading along the X and Z direction, two “force-displacement” characteristics with respect to X and Z directions can be obtained from finite element analyses of the micro model of the CuC interconnect shown in Figure 4.20.

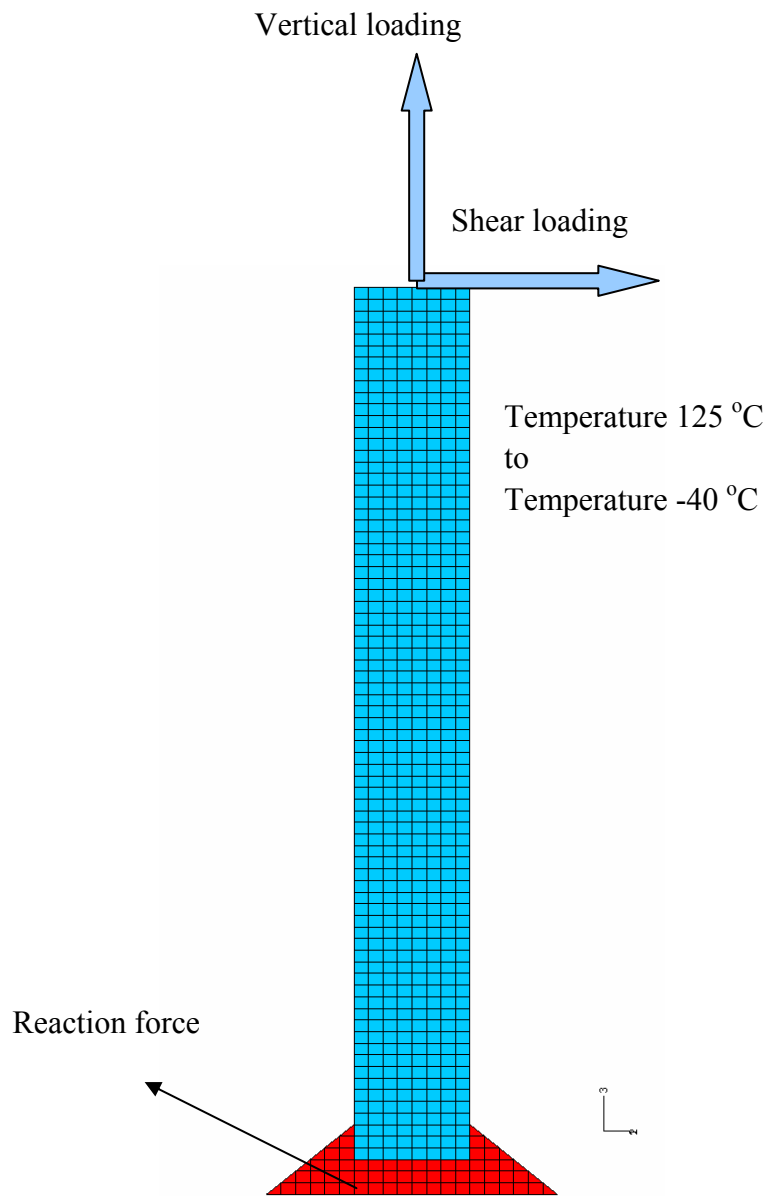
The resulting force-displacement characteristics are shown in Figure 4.21

**Table 4.7 Equivalent beams (EBs) for CuC interconnects**

	D20H100	D20H125	D20H150
EB height	106µm	131µm	156µm
EB diameter	20µm	20µm	20µm

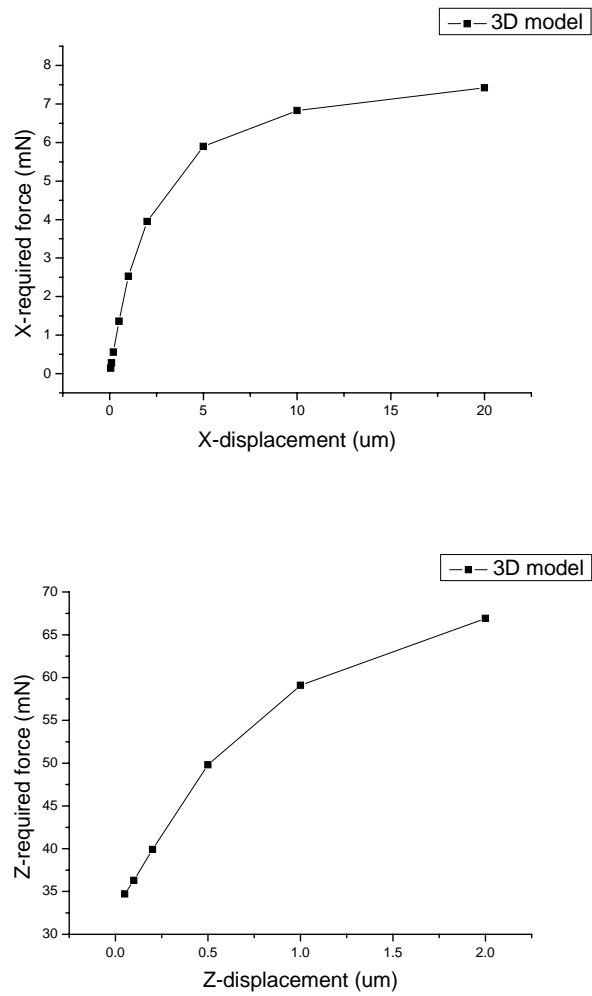
The equivalent beams are chosen to have the same material properties of copper and the same height as the CuC interconnect given by the height of the CuC and the solder layer below it. Table 4.7 shows the details of equivalent beams for three CuC interconnects under investigation.

The force-displacement characteristics of the 3D finite element model for D20H100 and that of the equivalent beam are compared in Figure 4.22 and 4.23.

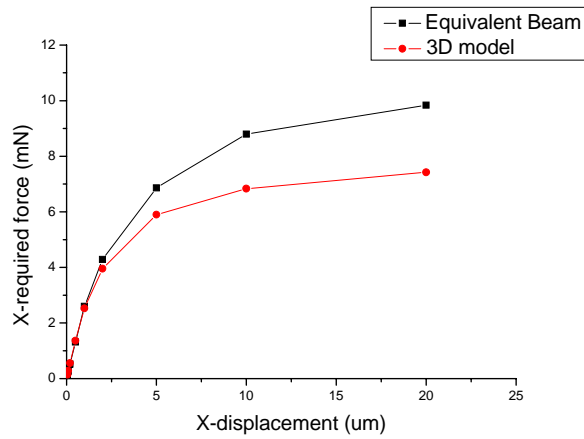


**Figure 4.20** Micro model of CuC interconnect

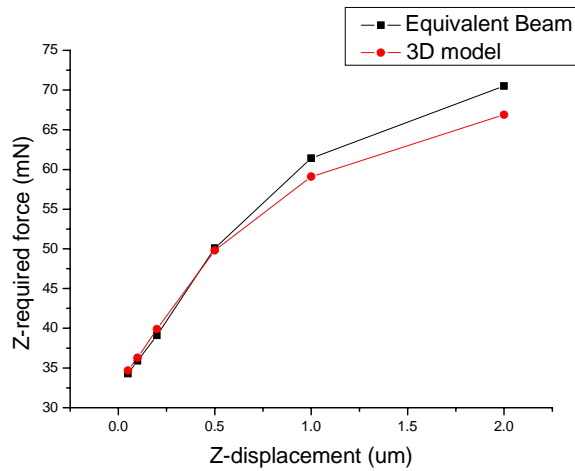




**Figure 4.21 Force-displacement characteristics of micro model**



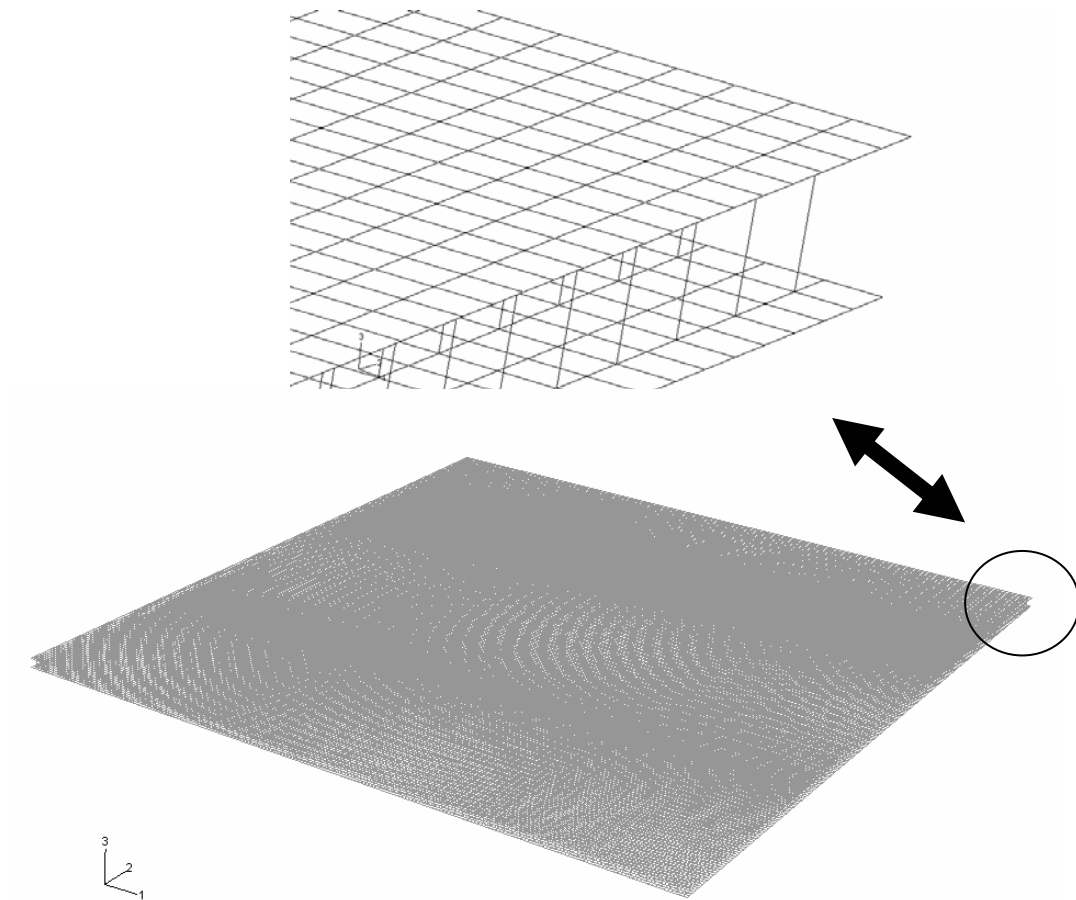
**Figure 4.22 Comparison of X-displacement of equivalent beam**



**Figure 4.23 Comparison of Z-displacement of equivalent beam**

#### 4.3.4 Global shell-and-beam model

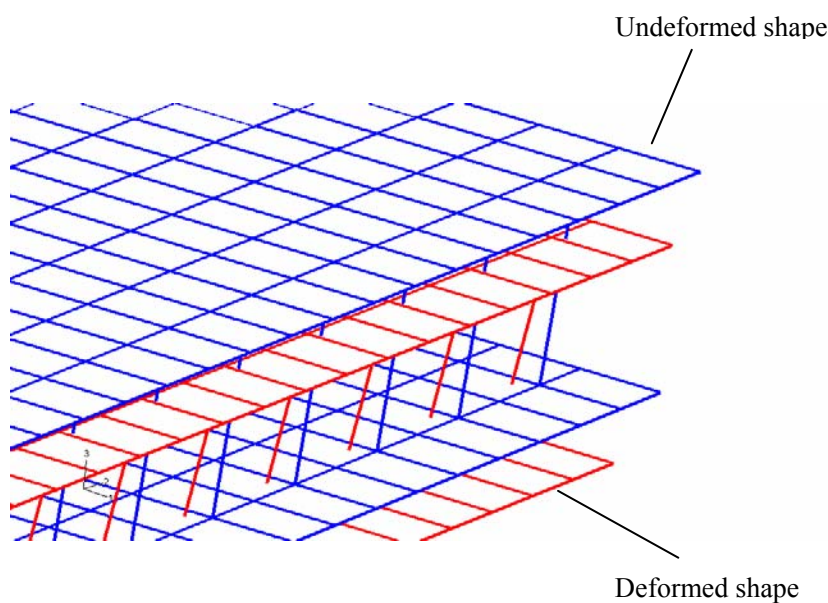
For chip/substrate, their length/width is much larger than the thickness. So in a global model they are modeled as shell structures using S4R conventional shell elements (see Figure 4.24).



**Figure 4.24 Global shell-and-beam model and local zoom-in view**

After equivalent beams are derived, they are used in a global shell-and-beam model (as illustrated in Fig. 4.24) to obtain the necessary displacement results to drive a submodel analysis. It is apparent that this shell-and-beam model saves a lot of computational resources compared to a full 3D solid element model. Only one quarter of the package is modeled because package has the requisite planes of symmetry. It should be noted that although the package also has the feature of octant symmetry, one-eighth model is not adopted. This is because of the difficulty of dividing a beam element into two separate parts along the octant symmetry

plane. The central node on the substrate is fixed, preventing rigid body motion. Five thermal cycles with temperature extremes of 125 °C and -40 °C are simulated, with the initial stress-free temperature at 125 °C. The relevant material properties are listed in Table 3.4, Table 3.5, and Table 3.6 of Chapter 3. A typical deformation of a global shell-and-beam model can be seen in Figure 4.25

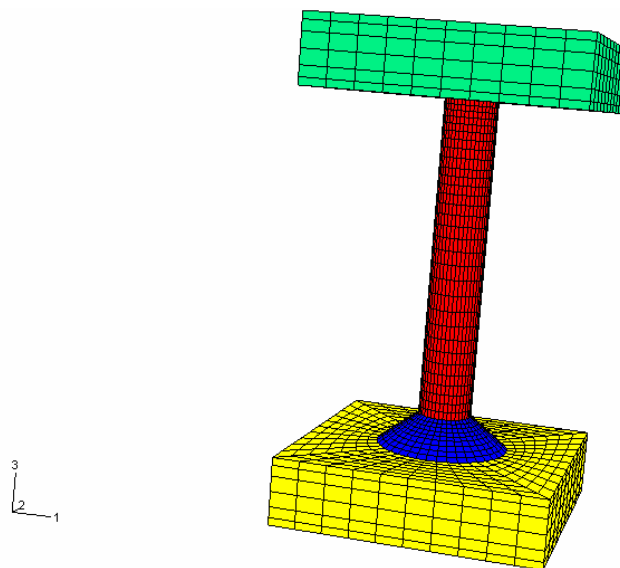


**Figure 4.25 Deformation of global model at -40oC (first cycle)**

#### **4.3.5 Shell-to-solid submodeling**

As stated earlier, the global shell-and-beam model can only yield accurate deformation results of the package, not the stress/strain results. A submodel (as illustrated in Figure 4.26) should be built and analyzed to obtain the detailed stress/strain results in the solder joint of the critical CuC interconnect.

In ABAQUS, submodeling technique is used to investigate a local part of a model with a refined mesh based on interpolation of the solution from an initial, relatively coarse, global model. By specifying the driven nodes in the submodel of the critical CuC interconnect, ABAQUS will automatically search the global shell-and-beam model in the vicinity of the submodel for the necessary displacement results and interpolate those results onto the nodes on the appropriate parts of the boundary of the submodel. Thus, the response at the boundary of the submodel is defined by the solution for the global shell-and-beam model. The driven nodes and any loads applied to the submodel determine the solution in the submodel. Figure 4.2 illustrates the relationship between global model and submodel.



**Figure 4.26 Submodel of critical CuC interconnect**

After the submodel analysis, maximum inelastic shear strain range  $\Delta\gamma_p$  is extracted for estimation of fatigue life. However, this value is not readily available in ABAQUS output. Some simple calculations are needed to obtain it.

The maximum shear strain at a certain node in the solder joint is given by

$$\Delta\gamma_p = \text{IE}_{\text{max.principal}} - \text{IE}_{\text{min.principal}} \quad (4.1)$$

where IE is inelastic strain. Maximum inelastic shear strain range is evaluated based on the last temperature cycle. In order to alleviate the mesh sensitivity of this value, a portion rather than a single node is used for estimation. This portion of the model is selected by identifying the elements which share the node that has the maximum inelastic shear strain range. Then the desired maximum inelastic shear strain range is averaged over those identified elements at element centroids.

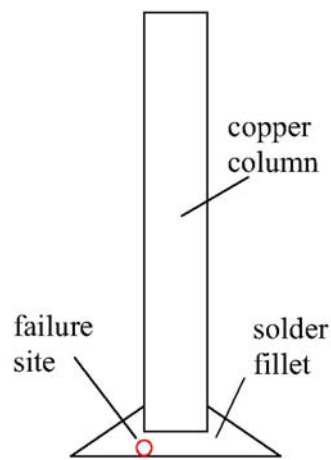
Maximum inelastic shear strain range is substituted into Solomon’s correlation to estimate the fatigue lives of three CuC interconnects. The fatigue lives estimated are shown in Table 4.8.

**Table 4.8 Fatigue lives of the three CuC interconnects**

	D20H100	D20H125	D20H150
Fatigue life ( $N_f$ )	20	27	29

The failure sites identified for the three CuC interconnects are illustrated in Figure 4.28. Note that same failure sites are identified for all of the three interconnects. Analyses are also conducted on D15, D25, and D30 with the same CuC height variation. The same failure sites as illustrated in Figure 4.28 are consistently identified for all the CuC interconnects.

Submodel analyses are also conducted using the original micro model illustrated in Figure 4.20. In this case, relative displacement results between the two ends of the critical interconnect (equivalent beam) need to be derived and applied as the boundary conditions of the micro model. However, it was found that the location of the failure site varied from case to case, as illustrated in Figure 4.29.



**Figure 4.27 Failure site identified using the modified macro-micro modeling approach**



\*On the symmetry plane or one element layer away from it.

**Figure 4.28 Failure sites identified using the original macro-micro modeling approach**

### **4.3.6 Discussion**

Advantages of the shell-and-beam-submodeling approach over the original Chng's macro-micro modeling approach

- No transformation or calculation is needed to derive the relative displacement results of the two ends of the equivalent beam. ABAQUS will automatically interpolate the solution from the global model onto the submodel boundary to perform the submodel analysis.
- By incorporating the chip and substrate in a submodel analysis, the local mismatch at the chip/interconnect and substrate/interconnect interfaces are accounted for.
- The loading condition on the submodel is closer to the real loading condition compared to the loading assumption used in the original macro-micro modeling approach. Hence, consistent failure sites have been identified for different CuC interconnects due to their similarity in structure and loading conditions.

The disadvantage of the shell-and-beam-submodeling approach is that a submodel different from the micro model used to derive the equivalent beam has to be set up.

### **4.3.7 Conclusions**

The following conclusions may be drawn.



- Despite the difference of geometrical parameters of different CuC interconnects, the location of the expected failure site remained the same.
- An increase of CuC height has a positive effect on the solder joint fatigue life. This is consistent with the result as shown in Chapter 3.
- Fatigue life of this interconnect is low based on Solomon's correlation.

## **CHAPTER 5: Conclusions of the Current Thesis**

The current thesis completed a literature survey on fatigue life correlation models and two important tasks. The two important tasks are:

First, a simulation-based design optimization process is established based on our available software resources, ABAQUS and Minitab. This process integrates FEA, DoE technique and numerical optimization, generating a systematic and efficient method that can be used to study the effects of various design parameters on desired system response. The significance of this simulation-based design optimization process lies in its general applicability in various design scenarios where effect of each design parameter on the system response is of interest, investigation of interaction of design parameters is needed and an optimal design parameter setting is required. After the establishment of this optimization process, a case study on CuC interconnect in wafer level packages is detailed. It is found that the substrate CTE has the largest influence on solder joint fatigue reliability. The chip thickness has the second largest influence with a smaller chip thickness leading to better solder joint reliability. The substrate thickness plays the third most important role with a thinner substrate thickness giving longer fatigue life. It is also found that increasing CuC height will result in better solder joint fatigue performance. Finally we find that the optimal design combination is: low-level substrate CTE, chip and substrate thickness, and high-level CuC height.

Secondly, two new and novel advanced finite element simulation methodologies, based on simplifying chip/substrate as shells and interconnects as beams, are developed to address the difficulty of modeling the large number of CuC interconnects in a 20mm by 20mm wafer level package with ultra-fine pitch. Although the idea of using shell and beam elements to model substrate/chip and interconnects is not new, previous researchers have not accurately translated the displacement results from the global shell-and-beam-based model to the local model. This thesis describes first-ever the application of the shell-to-solid submodeling and shell-to-solid coupling techniques available in ABAQUS to overcome the above-mentioned difficulty in the context of modeling solder joint fatigue of electronic packages. A feasibility demonstration of the two methodologies is firstly carried out. A great saving of computational resources is realized and results show that good accuracy is achieved. After this, as a case study, the shell-and-beam-submodeling approach is chosen for fatigue life prediction of three different CuC interconnects in 20mm by 20mm wafer level packages with 100 $\mu$ m pitch. By using the shell-to-solid submodeling technique, the stress/strain of the critical solder joint can be derived. Fatigue life prediction can then be performed based on Solomon's fatigue correlation. Some advantages of the shell-and-beam-submodeling approach over the original Chng's macro-micro modeling approach are: 1) No transformation or calculation is needed to derive the relative displacement results of the two ends of the equivalent beam. ABAQUS will

automatically interpolate the solution from the global model onto the submodel boundary to perform the submodel analysis. 2) By incorporating the chip and substrate in a submodel analysis, the local mismatch at the chip/interconnect and substrate/interconnect interfaces are accounted for. 3) The loading condition on the submodel is closer to the real loading condition compared to the loading assumption used in the original macro-micro modeling approach. Hence, consistent failure sites have been identified for different CuC interconnects due to their similarity in structure and loading conditions. Lastly, the following conclusions may be drawn: 1) Despite the difference of geometrical parameters of different CuC interconnects, the location of the expected failure site remained the same. 2) An increase of CuC height has a positive effect on the solder joint fatigue life. This is consistent with the result as shown in Chapter 3. 3) Fatigue life of this interconnect is low based on Solomon's correlation.

## References

- [1] Minbo Tian, Electronic Packaging Technology, pp. 86-99, China: Tsing Hua University Press. 2003
- [2] Rao R. Tummala (ed), Fundamentals of Microsystems Packaging, pp. 400-404, Singapore: McGraw-Hill. 2001
- [3] <http://public.itrs.net/>
- [4] Andrew. A. O. Tay, Challenges of Thermomechanical Design and Modeling of Ultra Fine-Pitch Wafer Level Packages, Proc. EuroSimE 2004, May 2004, Brussels, Belgium, pp. 601-606.
- [5] Nano Wafer Level Packaging brochure 2002.
- [6] Lecture notes of Fracture and Fatigue of Materials (ME5513), NUS
- [7] W. W. Lee, L. T. Nguyen, G. S. Selvaduray, Solder Joint Fatigue Models: Review and Applicability to Chip Scale Packages, Microelectronics Reliability, 40 (2004), pp. 231-234
- [8] D. R. Frear et al. (ed), The Mechanics of Solder Alloy Interconnects, New York: Van Nostrand Reinhold. 1994.
- [9] Audrey C. K. Chng, Modeling Fatigue Life of Solder Joints in Wafer Level Packages, Master Thesis, National University of Singapore, 2003
- [10] L. F. Coffin Jr., A Study of the Effects of Cyclic Thermal Stresses on a Ductile Metal, ASME Transactions, 76 (1954), pp. 931-950

- [11] S. S. Manson, Fatigue: a complex subject – some simple approximations, *Explorations in Mechanics*, 5 (1965), pp. 193-226
- [12] GE Dieter, In: *Mechanical Metallurgy*, pp. 391, New York: McGraw-Hill. 1986
- [13] T. J. Kilinski, J. R. Lesniak, B. I. Sandor, Modern Approaches to Fatigue Life Prediction of SMT Solder Joints, In: J. H. Lau (ed), *Solder Joint Reliability Theory and Applications*, New York: Van Nostrand Reinhold. 1991 (Chapter 13)
- [14] H. D. Solomon, Fatigue of 60/40 Solder, *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, 9(4), pp. 423-432, 1986
- [15] R. Cortez, E. C. Cutiongco, M. E. Fine, D. A. Jeannotte, *Proc 42nd ECTC*, pp. 354-359
- [16] R. Cortez, M. E. Fine, I. M. Daniel, D. A. Jeannotte, *Materials Developments in Microelectronic Packaging Conference Proceedings (1991)*, ASM International, pp. 147
- [17] K. N. Smith, P. Watson and T. H. Topper, *Journal of Materials*, 1970(5), pp. 767
- [18] D. F. Sochie and J. A Bannantine, 1989, *Materials and Engineering Design: The Next Decade*, ed. E. F. Dyson and D. R. Hayhurst, London: The London Institute of Metals, pp. 301
- [19] M. W. Brown and K. J. Miller, *Proc. Inst. of Mech. Eng.*, 187:745

- [20] R. D. Lohr and E. G. Ellison, 1980, *Fatigue of Engineering Materials and Structures*, 3:1
- [21] L. F. Coffin Jr., 1971, *Met. Trans*, 2: 3105
- [22] L. F. Coffin Jr., 1973, *ASTM STP-520*, pp. 112
- [23] S. Vaynman and M. E. Fine, 1991, *Mat. Res. Soc. Proc.* (3), pp. 226
- [24] W. Engelmaier, *Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling*, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 6(3), pp. 232-237, 1983
- [25] R. N. Wild, *Properties of Some Low Melt Fusible Solder Alloys*, IBM Technical Report No. 71Z000408, October 1971
- [26] S. Knecht and L. Fox, *Integrated Matrix Creep: Application to Accelerated Testing and Lifetime Prediction*, in: J. H. Lau (ed), *Solder Joint Reliability Theory and Applications*, New York: Van Nostrand Reinhold 1991
- [27] A. R. Syed, *Factors Affecting Creep-Fatigue Interaction in Eutectic Sn/Pb Solder Joints*, *Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference INTERpack'97*, vol. 2 (1997), pp. 1535-1542
- [28] A. R. Syed, *Thermal Fatigue Reliability Enhancement of Plastic Ball Grid Array (PBGA) Packages*, *Electronic Components and Technology Conference 1996*, pp. 1211-1216

- [29] A. R. Syed, T. Panczak, R. Darveaux, S. Lee, C. Lee, J. Partridge, Solder Joint Reliability of Chip Array BGA, Pan Pacific Microelectronics Symposium, Maui, 1998
- [30] J. H. L. Pang, T. Tan, S. K. Sitaraman, Thermo-mechanical Analysis of Solder Joint Fatigue and Creep in a Flip Chip on Board Package Subjected to Temperature Cycling Loading, Electronic Components and Technology Conference, 1998, pp. 878-883
- [31] S. S. Manson, G. R. Halford, and H. M. Hirshberg, 1971, Design for Elevated Temperature Environment, ASME, pp. 25
- [32] S. S. Manson, 1975, Time Dependent Fatigue of Structural Alloy, ORNL-5073, pp. 155
- [33] G. R. Halford and S. S. Manson, 1976, ASTM STP 612, pp. 239
- [34] A. Dasgupta, C. Oyan, D. Barker, M. Pecht, Solder Creep-Fatigue Analysis by an Energy-Partitioning Approach, Journal of Electronic Packaging, 1992 (114), pp. 52-60
- [35] J. Morrow, 1965, ASTM STP-378, pp45
- [36] H. Akay, H. Zhang, N. Paydar, Experimental Correlations of an Energy-based Fatigue Life Prediction Method for Solder Joints. In: Advances in Electronic Packaging, Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference INTERpack'97, vol.2, pp1567-74



- [37] J. Liang, N. Gollhardt, PS Lee, S. Heinrich, S Schroeder, An Integrated Fatigue Life Prediction Methodology for Optimum Design and Reliability Assessment of Solder Interconnections. In: Advances in Electronic Packaging, Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference INTERpack'97, vol.2, pp1583-92
- [38] G. Gustafsson, Solder Joint Reliability of a Leadless RF-transistor, Electronic Components and Technology Conference, June, 1998, pp. 87-91
- [39] A. Mertol, Application of the Taguchi Method on the Robust Design of Molded 225 Plastic Ball Grid Array Packages, IEEE Trans. Comp. Packag., Manufact. Technol. B, vol. 18, pp. 734-743, Nov. 1995
- [40] A. Mertol, Optimization of High Pin Count Cavity-up Enhanced Plastic Ball Grid Array (EPBGA) Packages for Robust Design, IEEE Trans. Comp. Packag., Manufact. Technol. B, vol. 20, pp. 376-388, Nov. 1997
- [41] A. Mertol, Application of the Taguchi Method to Chip Scale Package (CSP) Design, IEEE Trans. Adv. Packag., vol. 23, 2000, pp. 266-276
- [42] A. Dasgupta, M. G. Pecht, B. Mathieu, Design-of-experiment Methods for Computational Parametric Studies in Electronic Packaging, Finite Element in Analysis and Design, 30 (1998), pp.125-146
- [43] G. Q. Zhang, J. H. J. Janssen, L. J. Ernst, J. Bisschop, Z. N. Liang, F. Kuper, and R. L. Schravendeel, Virtual Thermo-Mechanical Prototyping of Electronic Packaging Using Philips' Optimization Strategy, IMAPS2000, USA

- [44] S. Stoyanov, C. Balley and M. Cross, Optimization Modeling for Flip Chip Solder Joint Reliability, *Soldering & Surface Mount Technology*, 14/1, 2002, pp. 49-58
- [45] B. Vandeveld, E. Beyne, G. Q. Zhang, Jo F. J. M. Caers, D. Vandepitte and M. Baelmans, Solder Parameter Sensitivity for CSP Life-Time Prediction Using Simulation-Based Optimization Method, *IEEE trans. on Electronics Packag. Manufact.*, vol. 25, 4, October 2002
- [46] B. Vandeveld, E. Beyne, G. Q. Zhang, Jo Caers, D. Vandepitte, M. Baelmans, Parameterized Modeling of Thermo-mechanical Reliability for CSP Assemblies, *Journal of Electronic Packaging*, vol. 125, December 2003
- [47] W. D. van Driel, G. Q. Zhang, J. H. J. Janssen, L. J. Ernst, Reponse Surface Modeling for Nonlinear Packaging Stresses, *Journal of Electronic Packaging*, vol. 125, December 2003
- [48] W. D. van Driel, G. Q. Zhang, J. W. C. de Vries, M. Jansen, L. J. Ernst, Virtual Prototyping and Qualification of Board Level Assembly, *Proceedings of EPTC2003*, December 2003
- [49] S. G. Jagarkal, M. M. Hossain, D. Agonafer, M. Lulu, S. Reh, Design Optimization and Reliability of PWD Level Electronic Package, *Proceedings of ITherm'04*, June, 2004 Las Vegas, USA

- [50] D. G. Yang, J. S. Liang, Q. Y. Li, L. J. Ernst, G. Q. Zhang, Parametric Study on Flip Chip Package with Lead-free Solder Joints by Using the Probabilistic Designing Approach, *Microelectronics Reliability*, 44, 2004, pp. 1947-55
- [51] C. C. Lee, S. M. Chang, K. N. Chiang, Design of Double Layer WLCSP Using DOE with Factorial Analysis Technology, *Proceedings of EPTC2004*, December 2004
- [52] A. A. Giunta, Use of Data Sampling, Surrogate Models, and Numerical Optimization in Engineering Design, AIAA 2002-0538, American Institute of Aeronautics and Astronautics
- [53] H. S. Morgan, Thermo-mechanical Modeling of Solder Joints-Numerical Considerations, In: *The Mechanics of Solder Alloy Interconnects*, ed by D. R. Frear, S. N. Burchett, H. S. Morgan, J. H. Lau, pp. 314-330, New York: Van Nostrand Reinhold. 1993
- [54] N. R. Bonda, I. C. Noyan, Effect of the Specimen Size in Predicting the Mechanical Properties of PbSn Solder Alloys, *IEEE Transactions on Components, Packaging and Manufacturing Technology-Part A*, 19(2), pp. 208-212, 1996
- [55] M. Klein, A. Hadrboletz, B. Weiss, G. Khatibi, The 'Size Effect' on the Stress-Strain, Fatigue and Fracture Properties of Thin Metallic Foils, *Materials Science and Engineering A*, 319-321, pp. 924-928, 2001

- [56] Z. Guo, H. Conrad, Effect of Microstructure Size on Deformation Kinetics and Thermo-mechanical Fatigue of 63Sn37Pb Solder Joints, *Journal of Electronic Packaging*, 118, pp. 49-54, 1996
- [57] Audrey C Chng, A. A. O. Tay, K. M. Lim, Fatigue Life Estimation of a Bed-of-Nails Ultra-Fine-Pitch Wafer Level Package Using the Macro-Micro Modeling Approach, *Proceedings of EPTC2003*, December 2003
- [58] Y. T. Lin, C. T. Peng, K. N. Chiang, Parametric Design and Reliability Analysis of Wire Interconnect Technology Wafer Level Packaging, *Journal of Electronic Packaging*, vol. 124, September 2003
- [59] Q. Yao, J. Qu, Three-Dimensional Versus Two-Dimensional Finite Element Modeling of Flip-Chip Packages, *Journal of Electronic Packaging*, 121, pp. 196-201, 1999
- [60] J. S. Corbin, Finite Element Analysis for Solder Ball Connect (SBC) Structural Design Optimization, *IBM Journal of Research and Development*, 37(5), pp. 585-596, 1993
- [61] T. H. Ju, Y. W. Chan, S. A. Hareb, Y. C. Lee, An Integrated Model for Ball Grid Array Solder Joint Reliability, *Structural Analysis in Microelectronic and Fiber Optic Systems ASME* 1995, vol. 12, pp. 83-89
- [62] Y. W. Chan, T. H. Ju, S. A. Hareb, Y. C. Lee, Reliability Modeling for Ball Grid Array Assembly with a Large Number of Warpage Affected Solder Joints, *Journal of Electronic Packaging*, vol. 124, September 2002

- [63] H. C. Cheng, K. N. Chiang, M. H. Lee, An Effective Approach for Three-Dimensional Finite Element Analysis of Ball Grid Array Typed Packages, *Journal of Electronic Packaging*, vol. 120, June 1998
- [64] C. A. Yuan and K. N. Chiang, Micro to Macro Thermo-Mechanical Simulation of Wafer Level Packaging, *Journal of Electronic Packaging*, vol. 125, December 2003
- [65] ABAQUS inc., ABAQUS Analysis User's Manual for Version 6.4
- [66] L. S. Goldmann, Geometric Optimization of Controlled Collapse Interconnects, *IBM Journal of Research and Development*, pp. 251-265, May 1969
- [67] S. M. Heinrich, M. Schaefer, S. A. Schroeder, P. S. Lee, Prediction of Solder Joint Geometries in Array-Type Interconnects, *Journal of Electronic Packaging*, vol. 118(3), pp. 114-121, 1996