METAL GATE WITH HIGH-K DIELECTRIC IN Si CMOS PROCESSING

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TABLE OF CONTENTS

Title ..... **i**

Acknowledgements ..... **ii**

Table of Contents ..... **iv**

Summary ..... **vii**

List of Tables ..... **ix**

List of Figures ..... **x**

List of Symbols ..... **xviii**

Bibliography ..... **xix**

CHAPTER 1 Introduction **1**

1.1 MOSFET Scaling Overview 1

1.2 High-K Dielectric 6

1.2.1 Limitation of Conventional Gate Oxides 6

1.2.2 Candidates of High-K Dielectric 9

1.2.3 Scaling Challenges in High-K Dielectric 9

1.2.4 Carrier Mobility 9

1.2.5 Threshold Voltage Instability 10

1.2.6 Thermal Stability of High-K Dielectrics 10

1.3 Metal Gate Technology 12

1.3.1 Limitations of Polysilicon Gate 12

1.3.2 Material Consideration for Metal Gate 13

1.3.3 Metal Candidates 14

1.3.4 Work Function 16

1.3.5 Work Function Determination 16

1.3.6 Work Function Consideration 17

1.3.7 Effect of Surface Doping Concentration 18

1.3.8 Work Function Variation with High-K Dielectric 21

1.3.9 Process Integration of Dual Metal Gate 21

1.4 Objectives 26

1.5 Significance and Organizations 27

References 29

CHAPTER 2 Dual Metal Gate Integration using AlN Buffer Layer 37
2.1 Introduction.....38
2.2 Experiment.....39
2.3 Results and Discussion.....42
2.3.1 Analysis of AlN Film as a Buffer Layer.....42
2.3.2 Chemical Resistance of AlN Film as a Buffer Layer.....45
2.3.3 XPS Study at Interface between AlN and Metals (Ta, Hf).....47
2.3.4 AlN Consumption.....50
2.3.5 Work Function.....54
2.3.6 I-V Characteristics.....58
2.4 Summary.....61
References.....62

CHAPTER 3 Fully Silicided Hf-Silicide Metal Gates 65
3.1 Introduction.....66
3.2 Experiment.....67
3.3 Results and Discussion.....69
3.4 Summary.....80
References.....81

CHAPTER 4 Substituted Al Metal Gate for Low Work Function and Fermi Level Pinning Free.....84
4.1 Introduction.....85
4.2 Background of Al substitution.....86
4.2.1 Reaction of Al with Si.....86
4.2.2 Applications using Al substitution.....87
4.3 Experiment.....87
4.4 Results and Discussion.....89
4.4.1 Substitution of Al for polysilicon.....89
4.4.2 C-V characteristics.....93
4.4.3 Work function of Substituted Al Gate and Fermi level pinning.....100
4.4.4 I-V characteristics.....103
4.5 Summary.....107
References.....108

CHAPTER 5 Pt Rich PtxSi Gate with High-K Dielectric for High Work Function and Reduced Fermi Level Pinning 111

5.1 Introduction 112

5.2 Experiment 113

5.3 Results and Discussion 114

5.3.1 Effect of Ti capping 114

5.3.2 Characteristics of Pt-rich Pt-silicide gated MOS characteristics 121

5.3.3 Dual metal gate integration 125

5.4 Summary 127

References 128

CHAPTER 6 Top Surface Aluminized and Nitrided HfAlON/HfO_2 Stack using AlN/HfO_2 130

6.1 Introduction 131

6.2 Experiment 132

6.3 Results and Discussion 135

6.3.1 Feasibility of AlN consumption 135

6.3.2 EOT reduction by AlN 138

6.3.3 Chemical composition of synthesized layer 140

6.3.4 Flat-band voltage shift 142

6.3.5 Gate leakage current characteristics 145

6.3.6 Improved mobility 147

6.4 Summary 148

References 149

CHAPTER 7 Conclusion 153

7.1 Approaches for integration of dual metal gates 153

7.1.1 AlN Buffer Layer 153

7.1.2 Fully Silicided Hf-Silicide 154

7.1.3 Substituted Al (SA) for nMOSFET 155

7.1.4 Pt-rich Pt_xSi Gate for pMOSFET 156

7.2 A proposal for integration of dual metal gates with high-K 157

7.3 HfAlON/HfO_2 stack fro advanced high-K dielectric 159

References 160

SUMMARY

As CMOS devices continue to be scaled down continuously, conventional gate dielectrics will encounter the limitation of scaling because thinner gate dielectric leads to much higher tunneling current, resulting in high power consumption and degradation in reliability. As gate size decreases, conventional polysilicon gate will encounter problems such as poly depletion, high resistivity and dopant penetration. High-K dielectrics and metal gate have been studied widely to solve the above problems. However, the introduction of high-K dielectric to Si CMOS technology generates new problems such as non-compatibility with polysilicon gate and carrier mobility degradation. In addition, the integration of metal gates for CMOS technology is still a big challenge.

The aim of this study was firstly to evaluate the feasibility of new approaches for integrating dual metal gates and their compatibility with the conventional Si CMOS process, and secondly to improve the carrier mobility using HfAlON/HfO_2 stack.

Thin AlN layer was used to form HfAlON on HfO_2 layer. AlN buffer layer included at the interface between metal and dielectric, full Hf silicidation of polysilicon, and full Al substitution for polysilicon were investigated for integration of dual metal gates. It was found that gate leakage current and carrier mobility were significantly improved as Al and N were successfully incorporated on the top layer of HfO_2. The absence of adverse effect on the flat-band voltage and the significant improvement in mobility indicated that both Al and N were certainly localized near the top of HfO_2. The result that top incorporation of Al and N were successfully achieved using AlN/HfN stack

suggests a good combination of AlN and HfN. Three different new methods for integrating metal gates, namely, new metal alloy using thin AlN buffer layer, FUSI HfSi gate, substituted Al (SA), and FUSI Pt-rich Pt_xSi gate were proposed and demonstrated. About 4.4 eV of Hf-AlN and 4.9 eV of Ta-AlN alloy metal gates were successfully achieved using a thin AlN as a buffer layer. This also suggested that a wet etching process can be used for metal gate integration using the AlN layer. Although a wider range of work function was obtained using FUSI HfSi gate on SiO_2, more study HfSi gate on high-K dielectric is required. The work functions of SA and Pt_xSi gate were determined to be 4.25 and 4.9 eV with free and reduced Fermi level pinning, respectively. Since both gates can be implemented with Ti capping at the same temperature, the integration of dual metal gate using both gates may offer a feasible method for adjusting work function of metal gates. As an alternative way, fully substituted Al metal gate was also demonstrated for a low work function of metal.

HfAlON/HfO_2 with HfN metal gate may be a promising gate stack for fabricating advanced CMOS devices. Results of the integration of dual metal gates also suggest that the full-replacement of polysilicon with full-silicided or full-substituted metal may eliminate a Fermi level pinning problem observed at the interface between various gate electrodes and high-K dielectrics.

List of Tables

Table 2.1 Etching rates of various films. For HPM, 1:1:50 ($HF:H_2O_2:H_2O$) volume ratio was used at room temperature. For SPM solution, 1:4 ($H_2O_2:H_2SO_4$) volume ratio was used at 120 ^oC for etching those films. Sputtered Hf, AlN and thermally grown silicon oxide were used. 46

List of Figures

Fig. 1.1 Projection of physical gate length and gate oxide thickness for high performance logic application [1.2] 2

Fig. 1.2 Gate and channel length versus effective oxide thickness. L_{GATE} and L_E are gate length and channel length, respectively [1.3] 2

Fig. 1.3 Potential solutions for Low Operatiing Power (LOP), Low Standdy Power (LSTP) and High Performance (HP) logic applications. Solid, gray and white bars denote the status of research required, development underway, and qualification for pre-production, respectively [1.2] 5

Fig. 1.4 Gate leakage versus gate voltage for various oxide thicknesses [1.20].....6

Fig. 1.5 High-performance logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling [1.2]. 7

Fig. 1.6 LSTP logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling.....8

Fig. 1.7 Poly depletion increases the EOT of gate dielectric when the channel is in inversion. The added thickness is equivalent to $W_{d, poly}$. 12

Fig. 1.8 Two considerations of selecting a metal for gate electrode.....15

Fig. 1.9 Energy diagrams of threshold voltages for nMOS and pMOS devices for (a) midgap metal gate and (b) dual metal gate. 17

Fig. 1.10 Threshold voltage vs. gate work function for both n and p-channel devices with different surface concentration superimposed. 19

Fig. 1.11 Threshold voltage vs. gate work function for SOI devices [1.51].....20

Fig. 1.12 Threshold voltage vs. gate work function for thin body devices [1.16].....20

Fig. 1.13 Dual metal gate process using wet etching. Mo and Ti were used for gate electrode of pMOS and nMOS, respectively. TiN/Ti stack was removed away by SC1 chemical. 22

Fig. 1.14 Dual metal gate process using nitrogen implantation. Mo and N implanted Mo (MoN_x) were used for gate electrode of pMOS and nMOS, respectively. 23

Fig. 1.15 Dual metal gate process using metal interdiffusion. Ni (metal 2) and Ti (metal 1) were used for gate electrode of pMOS and nMOS, respectively. Ni was located on top of gate dielectric through diffusion. 24

Fig. 1.16 Dual metal gate process using full silicidation (FUSI). Ni-silicided B-doped polysilicon and Ni-silicided As (or P)-doped polysilicon were used for gate electrode of pMOS and nMOS, respectively. 25

Fig. 2.1 The schematic shows a proposed dual gates fabrication process flow; (a) deposition of first metal for nMOSFET on top of a reactive sputtered AlN buffer layer, (b) wet chemical etching the first metal from the pMOSFET region, (c) deposition of second metal for p-MOSFET, and (d) gate patterning and annealing to consume AlN buffer layer and form new metal alloy films. 41

Fig. 2.2 Sputtering rate for AlN deposition with plasma power. 43

Fig. 2.3 Plot of CET vs. physical thickness of AlN/SiO_2 stack gate dielectric. 43

Fig. 2.4 (a) The XPS depth profile of AlN film. (b) Dependence of composition ratio of AlNx on the process gas flow rate during AlN formation sputtering. 44

Fig. 2.5 The C-V measurement results on Pt/SiO_2 and $Pt/AlN/SiO_2$ capacitors after annealing at 420ºC in a forming gas ambient. The 0.3 nm increase in EOT is observed by introducing AlN. One of $Pt/AlN/SiO_2$ capacitors underwent deposition of Hf followed by wet chemical stripping before Pt deposition. No noticeable difference is found, indicating that AlN has sufficient chemical resistance during wet etching of the first metal. 46

Fig. 2.6 N 1*s* (a), Al 2*p* (b), and Ta 4*f* (c) XPS spectra at Ta/AlN interface before and after annealing at 420°C and 950°C. Binding energy shift after annealing indicates the reaction of AlN with Ta. 48

Fig. 2.7 N 1*s* (a) and Al 2*p* (b) XPS spectra at Hf/AlN interface before and after annealing at 420°C and 950°C. Binding energy shift after annealing indicates the reaction of AlN with Hf. 49

Fig. 2.8 C-V measurement results of $Ta/AlN/SiO_2$ before and after anneal at 420 ºC in a forming gas ambient. 50

Fig. 2.9 C-V measurement results of $Hf/AlN/SiO_2$ before and after anneal at 420 ºC in a forming gas ambient. 51

Fig. 2.10 HRXTEM images confirm the consumption of AlN buffer layer by subsequent annealing at 420^{o}C. The initial thickness of SiO_2 is 3.5nm. 52

Fig. 2.11 (a) EOT variation with various temperatures for two different thicknesses of AlN buffer layers. EOT in y-axis denotes the EOT difference between before and after annealing. (b) EOT variation of Ta- and Hf-AlN/SiO_2 capacitors with annealing condition. For both capacitors there is no change in EOT after AlN consumption. 53

Fig. 2.12 The normalized C-V curves of (a) Ta/SiO_2 capacitor and (b) $Ta/AlN/SiO_2$ capacitor, before and after anneal at 420^{o}C. A significant shift of V_{fb} is observed for $Ta/AlN/SiO_2$ while there is no change in V_{fb} for Ta/SiO_2. 55

Fig. 2.13 The C-V curves of Hf- and Ta-AlN/SiO_2 after anneal at 420^{o}C (a) and 420°C followed by 600°C (b) show 0.5V of V_{fb} difference. (T_{ox} = 48nm, area = $4x10^{-4}Cm^2$). ..56

Fig. 2.14(a) V_{fb} plotted against gate oxide thickness for the extraction of work function of Ta-AlN and Hf-AlN gates on p-type substrate. (b) The work function of Ta-AlN and Hf-AlN gates after annealing at 420°C and 600°C. 57

Fig. 2.15 The J-V characteristics of Hf-AlN and Ta-AlN gates on p-sub after anneal at 420 ^{o}C (a) and anneal at 420°C and 600°C. 58

Fig. 2.16 (a) Extracted barrier height (Φ_B) of both gates with SiO_2. (b) The J-V characteristics of Hf-AlN and Ta-AlN gates on p-sub after anneal at 420 ^{o}C. The J-V characteristic of $TaSi_xN_y$ gate with about 4.3eV workfunction is shown, which shows similar characteristics with that of Hf-AlN gate with about 4.4eV work function. 60

Fig. 3.1 AES depth profile of tungsten capped Hf-silicide formed through RTA at 650 ^{o}C. Negligible interdiffusion between W and Hf is observed after RTA at 650^{o}C. 68

Fig. 3.2 (a) The consumption of polysilicon by silicidation at different annealing temperature. (b) Sheet resistance of Hf/polysilicon stack layers after annealing at different temperatures. Sheet resistance was measured before unreacted metal strip. The initial polysilicon thickness is 200 nm. RTA was done at the temperature range of 600^{o}C - 750^{o}C for 1 min. For 420^{o}C, the annealing was done in a furnace tube for 1 hour.....70

Fig. 3.3 (a) XPS depth profile of Hf-silicide formed on undoped polysilicon after RTA at 600 ^{o}C for 1 min. The initial thickness of Hf and polysilicon is 200 nm and 100 nm, respectively. About 55 nm of polysilicon was consumed for silicidation. Sputtering rate was 11.9 nm/min. (b) RBS spectrum of Hf silicide formed through RTA at 600°C. Mostly the composition is estimated to be 0.9, which is very close to HfSi. 71

Fig. 3.4 The quasi-static C-V curve of Hf-silicide gated MOS capacitors. The Hf-silicide was formed by RTA at 600^{o}C for 1 min. The sample went through another annealing at 750^{o}C for 30 sec after removal of unreacted. The thickness of SiO_2 gate dielectric is 7.6nm and the area of MOS capacitors is 1.0×10^{-4} cm^2. 72

Fig. 3.5 AES depth profile of fully silicided Hf-silicide through RTA at 600^{o}C for 1min. Hf (80 nm)/phosphorous doped polysilicon (40nm) film stack was used for silicidation. After RTA, both capping and unreacted metals were removed away using wet chemical solutions. 73

Fig. 3.6 C-V curves of Hf-silicide gated MOS capacitor with thin SiO_2. The initial thickness of gate oxide is 3.55 nm and the area of capacitors is 1.0×10^{-4} cm^2. 74

Fig. 3.7 HRXTEM of $HfSi/SiO_2$ gate stack and its focused image. 75

Fig. 3.8 Flat-band voltage vs. gate oxide thickness. Work function difference of about 0.64 eV is obtained between Hf-silicided n+ polysilicon and Hf-silicided p^+ polysilicon. 75

Fig. 3.9 Tunable range of work function in Hf-silicide and Ni-silicide by controlling dopants in polysilicon. The work function of n-HfSi is nearer to that n^+, while the work

function of Ni-silicide is nearer to that of p^+ polysilicon, respectively. •, ■ : this work, ◘ : taken from Ref. [3.6] 76

Fig. 3.10 Variation of equivalent oxide thickness and flat-band voltage of FUSI HfSi gate MOS capacitors before and after annealing at different temperatures. The TaN capping layer was used on top of HfSi. Excellent thermal stability up to 950 ^oC is observed. 77

Fig. 3.11 I-V characteristics of TaN/HfSi/SiO_2 MOS capacitors with annealing temperature. Hf-silicide was formed through RTA at 600^oC for 1 min. TaN was capped right after unreacted Hf was removed away. The thickness of gate oxide was 3.5 nm. ...78

Fig. 3.12 High frequency C-V curve of FUSI HfSi gate nMOSFET with 3.2 nm thick gate oxide. Source/drain was grounded during measurement. No polysilicon depletion is observed. 79

Fig. 3.13 I_d-V_d characteristics of nMOSFET with FUSI n-HfSi gate. Neither p-well implantation nor V_{th} adjustment implantation was done. 79

Fig. 4.1 (a) the surface of Al/polysilicon stack on thermal oxide after anneal (b) the surface of Al/polysilicon after anneal followed by Al removal using wet chemical solutions. Annealing was done in a furnace at 450°C for 30 min. Noted that orange spots are Si and light blue colors are Al in (a) while black colors are oxide in (b), indicating non-uniform reaction of Al and polysilicon. Removal of Al exposed oxide layer. 90

Fig. 4.2 HRXTEM images; (a) polysilicon on HfAlON before Al substitution, (b) after annealing of Ti/Al/polySi on HfAlON for Al substitution. It is observed that polysilicon is fully substituted with Al and diffused towards Ti, forming Ti-silicide. (c) Focused image of the interface of substituted-Al and HfAlON. The substitution of Al was done by annealing at 450°C in a furnace. 91

Fig. 4.3 AES depth profiles of Ti/Al/polysilicon on HfAlON (a) before and (b) after Al substitution with polysilicon. Silicon is diffused towards Ti and reacted with Ti, resulting in TiSi formation. 92

Fig. 4.4 C-V curves of MOS capacitors with SA or FUSI NiSi of undoped polysilicon on SiO_2. Both Al substitution and FUSI silicidation shows identical EOT, indicating the full substitution of undoped polysilicon. 93

Fig. 4.5 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA), and FUSI NiSi of n^+ polysilicon (n-NiSi) on SiO_2. Both gates show V_{fb} shift and EOT reduction after SA and FUSI processes. 94

Fig. 4.6 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA), and FUSI NiSi of n^+ polysilicon (n-NiSi) on Si_3N_4. Both gates show V_{fb} shift and EOT reduction after SA and FUSI processes. 95

Fig. 4.7 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA) on Al_2O_3. Al_2O_3 was deposited by ALD CVD.

High positive V_{fb} shift of n^+ polysilicon is due to Fermi level pinning at the interface between Al_2O_3 and polysilicon. Negative V_{fb} shift and EOT reduction is observed after Al substitution. 96

Fig. 4.8 C-V curves of MOS capacitors with substituted Al and FUSI NiSi of undoped polysilicon on HfAlON. Identical EOT and 0.44 V of V_{fb} difference are observed after SA and FUSI processes. 97

Fig. 4.9. C-V curves of MOS capacitors with substituted Al and FUSI NiSi of n^+ polysilicon on HfAlON. Compared to n^+ polysilicon, lower V_{fb} is observed in SA gate and larger V_{fb} is observed in FUSI n-NiSi gate. 97

Fig. 4.10 C-V curves of MOS capacitors with SA gates formed using n^+ polysilicon (n-SA), p+ polysilicon (p-SA), and undoped polysilicon (SA).The negligible difference in V_{fb} indicates that the work-function value of SA on high-K does not depend on polysilicon pre-doping. 99

Fig. 4.11. High frequency C-V curves of substituted Al gate measured on nMOSFET. Source and drain were grounded for measurement. No polysilicon depletion is observed after substitution of Al. 99

Fig. 4.12 Plots of EOT vs. flat-band voltage for n^+ polysilicon gate on SiO_2 and HfAlON. 100

Fig. 4.13 Characteristics of I_d-V_g for n+polysilicon gated SiO_2 and HfAlON nMOSFETs. About 0.35 V of V_{th} difference is observed. 101

Fig. 4.14 Plots of EOT vs. flat-band voltage for SA gates on SiO_2 and HfAlON. 102

Fig. 4.15 Plots of EOT vs. flat-band voltage for n-type FUSI NiSi gate on SiO_2 and HfAlON. 102

Fig. 4.16 Leakage current characteristics of n-SA and FUSI n-NiSi gate on reoxidized CVD Si_3N_4. Comparable leakage currents are observed between SA and FUSI gates. 104

Fig. 4.17 Leakage current characteristics of n-SA and FUSI n-NiSi gate on HfAlON high-K dielectrics. Comparable leakage currents are observed between SA and FUSI gates. 104

Fig. 4.18 Plots of leakage current vs. EOT for Si_3N_4. Benchmarked data are also compared. The SA gate on high-K shows slightly lower leakage current than n^+ polysilicon gate on high-K and comparable to FUSI NiSi gate on high-K. The results denoted by * (n^+polySi/SiO_2) and + (FUSI n-NiSi/SiON) are quoted from ref. [4.16] and [4.8], respectively. 105

Fig. 4.19 Plots of leakage current vs. EOT for HfAlON dielectric. Benchmarked data are also compared. The SA gate on high-K shows slightly lower leakage current than n^+ polysilicon gate on high-K and comparable to FUSI NiSi gate on high-K. The results denoted by * (n^+polySi/SiO_2) and + (FUSI n-NiSi/HfSiON) are quoted from ref.[4.16] and [4.8], respectively. 105

Fig. 4.20 Cumulative plot of leakage current distribution measured at V_{fb}-1V of (a) n^+ polysilicon, n-SA, and FUSI n-NiSi gates on HfAlON dielectric. 106

Fig. 4.21 Cumulative plot of leakage current distribution measured at V_{fb}-1V of SA gates on HfAlON with different EOTs and on Si_3N_4 gate dielectrics. 106

Fig. 5.1 Wet etching rates of Pt and Pt-rich Pt-silicide.....114

Fig. 5.2 (a) Visual inspection and SEM-EDX analysis of surface after wet etching of Ti capped Pt/Pt_xSi. Clean gate patterns are observed. No Pt is detected on field oxide surface. 115

Fig. 5.2 (b) Visual inspection and SEM-EDX analysis of surface after wet etching of Pt/Pt_xSi stacks. Wet etch Pt-silicide residues are observed on field oxide. 116

Fig. 5.3 (a) C-V curves of Pt_xSi/HfAlON capacitors formed with and w/o Ti capping. (b) Gate leakage currents of Pt_xSi gates with HfAlON formed with and w/o Ti capping....117

Fig. 5.4 XPS depth profile of Pt rich Pt-silicide gate on HfAlON.....118

Fig. 5.5 Oxygen distribution in Pt/Pt_xSi layer for Ti capped and without Ti capping....119

Fig. 5.6 HRXTEM of Pt_xSi on HfAlON. No damage to HfAlON dielectric is observed. 120

Fig. 5.7 Plots of EOT vs. V_{fb} for Pt-silicide and n^+ polysilicon gates on SiO_2. 121

Fig.5.8 C-V curves of SA and Pt_xSi gates with HfAlON on p-Si substrate. Both gates were formed using P-doped polysilicon and undoped polysilicon for p-Si substrate and n-Si substrate, respectively.....122

Fig. 5.9 Comparison of effective work functions. No pinning is observed for SA while less pinning for Pt_xSi. SA data were taken from [5.12]. 123

Fig. 5.10 Comparison of gate leakage current characteristics of various gates on HfAlON. 124

Fig. 5.11 Comparison of V_{fb} s of various gates on Hf-based high-K dielectrics. No pre-doping was used for this work while B doping was used for benchmarked data. 124

Fig. 5.12. Symmetric C-V curves of SA and Pt_xSi gated HfAlON MOS capacitors on p- and n-Si substrate, respectively. No pre-doping of polysilicon was used. 125

Fig. 5.13 Gate leakage currents of SA and Pt_xSi gated HfAlON MOS capacitors on p- and n-Si substrate, respectively. Both measurements were done under accumulation. No pre-doping of polysilicon was used. 126

Fig. 6.1. Schematic diagram of process flow for top located HfAlON formation on HfO_2 using synthesis of AlN/HfO_2. 132

Fig. 6.2. (a) XTEM images of $HfN/AlN/HfO_2$ stack as–deposited and after RTA at 950^{o}C. (b) High frequency C-V curves of HfO_2 and AlN/HfO_2 MOS capacitors before and after RTA at 950°C. For HfO_2 MOS capacitor, PDA was done at 700°C for 1 min immediately after HfO_2 deposition. For AlN/HfO_2 stack capacitor, PDA was skipped after HfO_2 deposition. The area of capacitors is $50 \times 50\ \mu m^2$. 133

Fig. 6.3 High frequency C-V curves of HfO_2 MOS capacitor. PDA was done at 700 ^{o}C for 1 min right after HfO_2 deposition. No AlN was deposited on top of HfO_2. Increase in EOT due to IL growth is observed.....136

Fig. 6.4 High frequency C-V curves of $AlN(1.0\ nm)/HfO_2$ MOS capacitors. 137

Fig. 6.5 C-V curves of $AlN(2.0\ nm)/HfO_2$. PDA was skipped after HfO_2 deposition. Final EOTs of synthesized $HfAlON/HfO_2$ stacks are identical regardless of initial AlN thickness, indicating complete consumption of AlN during RTA. It is observed that final EOT of synthesized $HfAlON/HfO_2$ stack is thinner than that of conventional HfO_2 even though the additional layer AlN is added. 138

Fig. 6.6 EOT reduction is found when AlN is used. The amount of EOT reduction depends of the process sequence. Thicker HfO_2 (4.8 nm) is used in this case. 139

Fig. 6.7 The change in thickness of HfO_2 on silicon substrate between before and after PDA. Thickness of HfO_2 films was measured by Spectroscopy Ellipsometer. For all the HfO_2 films, PDA was done at 700C in a N2 ambient for 1 min. 139

Fig. 6.8 XPS spectra on various films; (a) Al 2*p* peaks are observed near 74.3 eV (Al-O) and 73.8 eV (Al-N). (b) The shift of Hf 4*f* peak is observed after RTA, which is attributed to N incorporation. For AlN/HfO_2 stack, no PDA was done prior to AlN deposition. The annealing was done without HfN gate for XPS measurement. 141

Fig. 6.9 Nitrogen profile obtained from SIMS analysis. For the SIMS measurement, a platinum layer is used as a capping layer instead of HfN gate for better contrast of N profile. 141

Fig. 6.10 The hysteresis of the synthesized $HfAlON/HfO_2$ stack MOS capacitor after 950^{o}C RTA.....142

Fig. 6.11 The flat-band voltage with various $AlN/(AlN+HfO_2)$. HfAlO shows positive Vfb shift due to Al at the interface while the surface nitrided HfO_2 shows negative Vfb shift due to increased fixed charge. The $HfAlON/HfO_2$ shows no change in Vfb. 143

Fig. 6.12 Al and Si atomic concentration of $HfAlON/HfO_2$ stack obtained by Angle Resolved XPS. Most of Al atoms exist near top surface of HfO_2 after RTA. For the AlN/HfO_2 stack films, Al concentration becomes lower while for HfAlO it is not much changed with angle. 144

Fig. 6.13 Leakage current characteristics of synthesized $HfAlON/HfO_2$ stack formed using $AlN(1.0nm)/thick\text{-}HfO_2$. For the synthesized $HfAlON/HfO_2$ stack samples, PDA was skipped. For all the samples, RTA at 950^{o}C for 30s was conducted. 145

Fig. 6.14 Leakage current characteristics of synthesized HfAlON/HfO_2 stack formed using AlN(1.0~2.0nm)/thin-HfO_2. For the synthesized HfAlON/HfO_2 stack samples, PDA was skipped. For all the samples, RTA at 950^oC for 30s was conducted.....146

Fig. 6.15 EOT versus leakage current. the HfAlON/HfO_2 stack show significantly improved leakage current, compared to conventional HfO_2 + PDA process. 146

Fig. 6.16 Comparison of effective electron mobility of HfAlON/HfO_2 stack sand HfO_2 with surface nitridation. For both nMOSFETs, EOT is 1.15 nm.....147

Fig. 7.1 Proposed process scheme for dual metal gate integration using SA and Pt_xSi for nMOSFET and pMOSET. 158

List of Symbols

L_g (L_{GATE})	Physical Gate Length
L_E	Channel Length
K	Dielectric Constant
V_{th}	Threshold Voltage
E_c	Conduction Band Edge of Silicon
E_v	Valence Band Edge of Silicon
E_i	Intrinsic Energy Level of Silicon
E_{fn}	Fermi Level of n-type Silicon
E_{fp}	Fermi Level of p-type Silicon
$W_{d,\ poly}$	Polysilicon Depletion Width
V_{fb}	Flat-band Voltage
Φ_{MS}	Work Function Difference
Φ_M	Work Function of Metal
Φ_{Si}	Work Function of Silicon
Q_f	Fixed Oxide Charge
Φ_B	Barrier Height

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Chapter 1

Introduction

1.1 MOSFET Scaling Overview

MOS device technology has experienced downscaling for high density and better performance by following Moore's Law for over forty years [1.1]. The IC industry has rapidly and consistently scaled the design rules, increased the chip and wafer size, and improved the design of devices and circuits. As the scaling of devices proceeds rapidly and continuously, the devices will encounter physical limitations and problems while technological improvements in device performance such as faster speed and lower power consumption are required. However, such rapid scaling will be more difficult unless new breakthroughs including new materials are found. A challenge is the scaling of gate length (L_g) in the MOSFETs, which has been a key factor driving both the overall MOSFET scaling and performance. This gate length scaling involves the reduction of gate oxide thickness and channel length as seen in Fig. 1.1. Hence, the scalability of gate length will determine if MOS devices can be scaled into the next generation.

Above all, gate oxide thickness scaling has been instrumental in controlling short channel effects in downscaled MOSFETs. Gate oxide thickness has been reduced nearly in proportion to the channel length to have good short channel behavior as seen Fig. 1.2. The device with the thinner oxide has a smaller channel depletion layer and hence improved short channel characteristics. Therefore, for continued MOS scaling, the gate dielectric thickness must continue to be scaled. However, there exists the thickness limit for SiO_2 due to its physical limitation. Fig. 1.2 also shows that the limitation of SiO_2 thickness will also determine the limitation of channel length. In addition, when the gate oxide thickness becomes thinner and closer to the thickness limitation, the gate oxide is

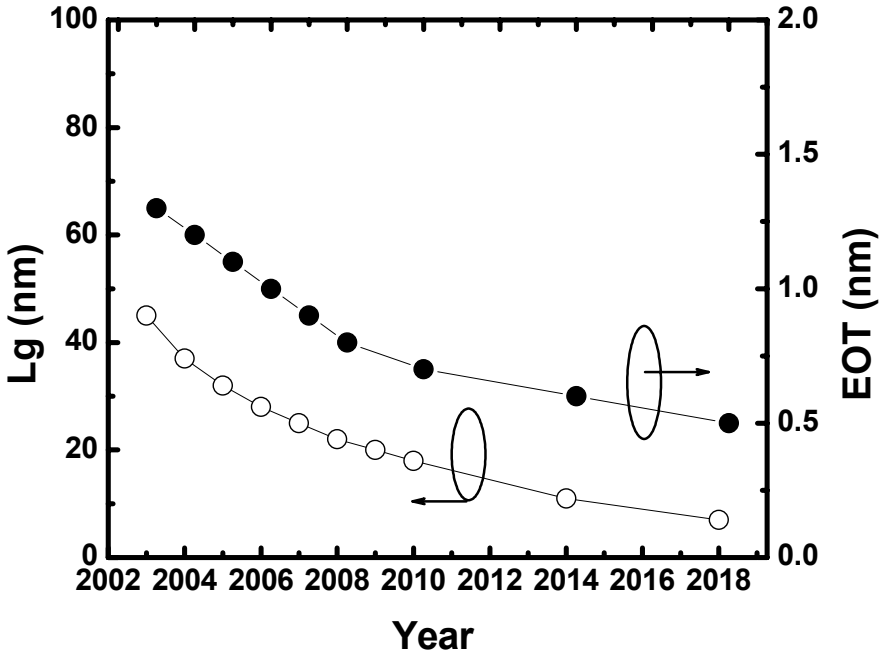

Fig. 1.1 Projection of physical gate length and gate oxide thickness for high performance logic application [1.2].

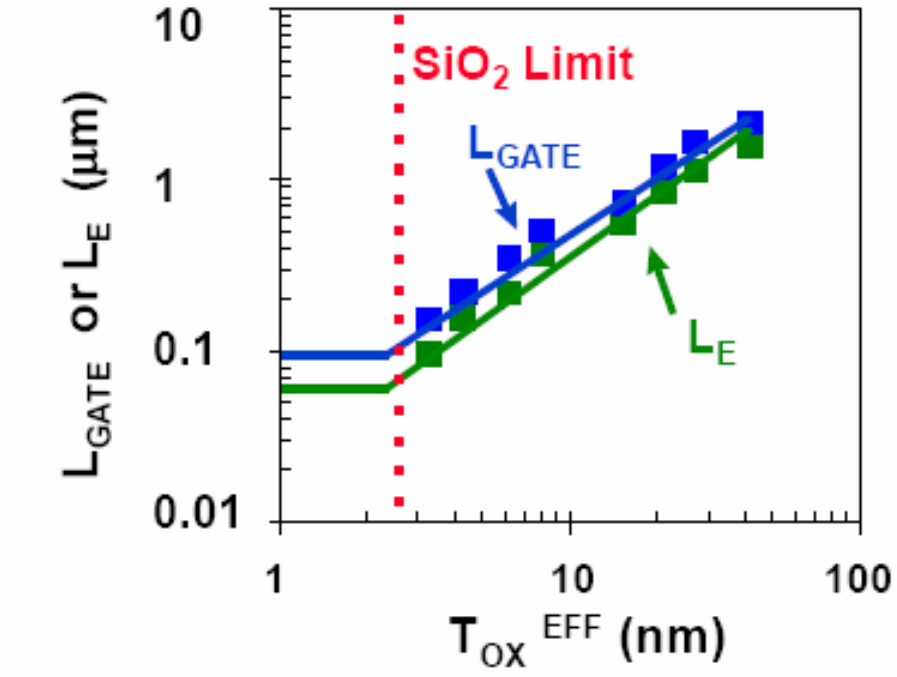

Fig. 1.2 Gate and channel length versus effective oxide thickness. L_{GATE} and L_E are gate length and channel length, respectively [1.3].

subject to direct tunneling, causing extremely high gate leakage current. The gate leakage current through such a thin oxide layer increases exponentially as the oxide thickness is scaled down. This direct tunneling gate leakage current will contribute to a huge increase of standby power consumption in a device. Accordingly, the allowable power consumption will limit the further scaling of gate oxide thickness in the CMOS devices. High dielectric constant (high-K) materials have been considered as alternative dielectrics to continue further MOSFET scaling. With these materials, thicker dielectric layers can be used but the same inversion layer characteristics can be maintained. These thicker layers result in smaller gate leakage current, and they allow further scaling of the effective oxide thickness.

Downscaled device dimension will also lead to smaller polysilicon gate dimension, causing several problems such as high sheet resistance, polysilicon depletion and boron penetration. Although the sheet resistance has been improved by incorporating silicides on top of the polysilicon, it does not provide sufficiently low resistivity for advanced gate stack. Polysilicon depletion, caused by insufficient activation of dopant within the gate, also affects device performance [1.4, 1.5]. As the polysilicon is driven into depletion, part of the applied voltage is dropped across the gate electrode, reducing the field at the Si/SiO_2 interface and decreasing channel carrier concentration. Gate capacitance is reduced due to the polysilicon depletion, indicating that the equivalent-oxide thickness of the total gate capacitance at inversion is thicker. The effect of polysilicon depletion on device performance becomes worse with the decrease of gate oxide thickness. The penetration of boron into gate dielectrics is another critical matter for MOSFETs [1.6, 1.7]. Boron penetration through thin oxide becomes more serious as the gate oxide thickness decreases below 2.0 nm. The increase of doping concentration is also restricted due to the limitation of solid solubility, and the restricted doping will also result in high resistivity. Therefore, metal gate electrode has been

widely studied because of no polysilicon depletion, low resistivity, no boron penetration, and better compatibility with high-K dielectric.

On the other hand, carrier mobility in a MOSFET channel is significantly reduced with gate oxide thickness [1.8]. As the channel length becomes shorter, improved carrier mobility in the inversion layer is also needed for the transistor performance. Moreover, serious mobility degradation due to high-K gate dielectric becomes a hot issue [1.9]. Strained-Si has been extensively investigated and shown a significant improvement for both n- and p-channel MOSFETs [1.10, 1.11]. Ge substrate can be another candidate to improve mobility [1.12, 1.13]. Extremely scaled MOSFET will also increase extrinsic parasitic resistances and capacitances. The introduction of new device structures to reduce the parasitic resistances and capacitances also becomes important. Fully Depleted Thin Body SOI technology has resulted in substantial reduction in the parasitic junction capacitances [1.14 – 1.19]. A double gate structure implemented with FinFET has been demonstrated as an alternative MOSFET structure [1.17-1.19], which has shown reduced short-channel effects and an enhanced carrier transport behavior [1.17, 1.18].

As predicted by International Technology Roadmap for Semiconductor (ITRS) [1.2], MOSFET scaling will continue further despite of problems mentioned above. As seen in Fig. 1.3, high-K gate dielectric and metal gate electrode were projected to be introduced into production by 2007, in order to effectively prevent polysilicon depletion and hence allow acceptable scaling down of the equivalent electrical oxide thickness. Ultra Thin Body SOI technology will also be utilized but a device designed by new architecture is still far from the present.

New process schemes and materials associated gate stacks will be the main focus of this thesis. In the following sections, demonstrated results and issues on high-K gate dielectric and metal gate technology will be explored.

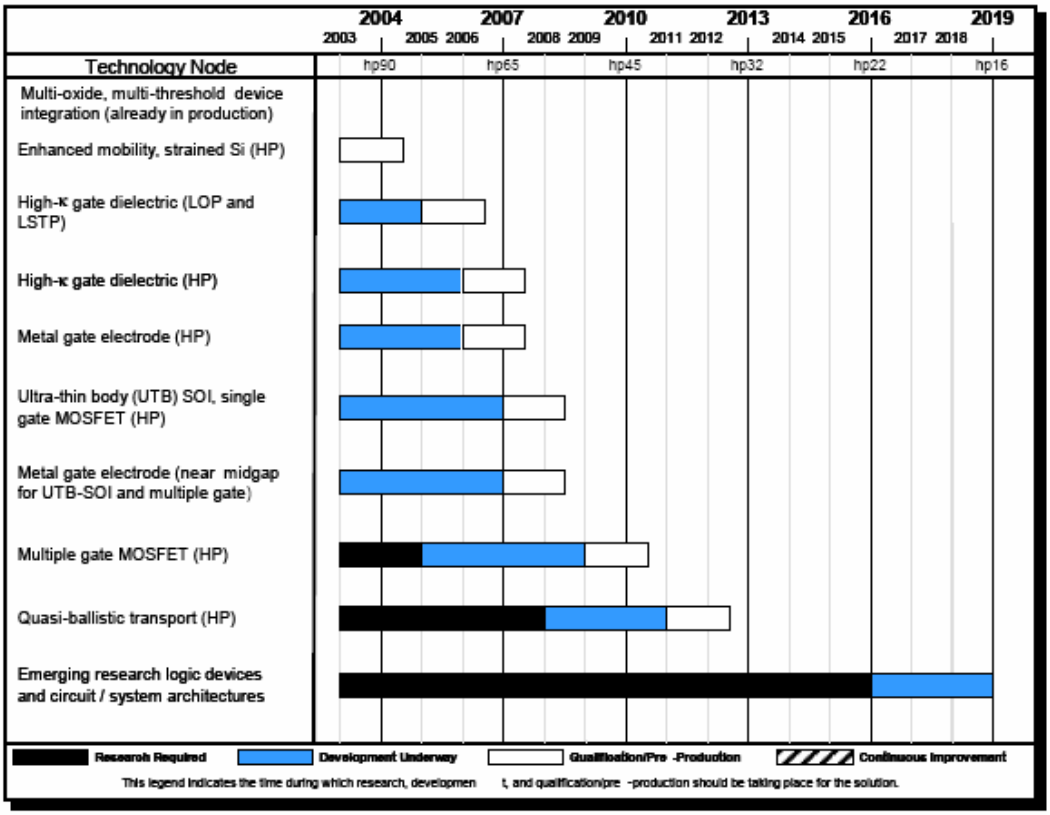

Fig. 1.3 Potential solutions for Low Operatiing Power (LOP), Low Standdy Power (LSTP) and High Performance (HP) logic applications. Solid, gray and white bars denote the status of research required, development underway, and qualification for pre-production, respectively [1.2].

1.2 High-K Dielectric

1.2.1 Limitation of Conventional Gate Oxides

As briefly discussed earlier, one of the key elements that has allowed the successful scaling of Si-based MOSFETs is the excellent material and electrical properties of SiO_2 as a gate dielectric. However, further scaling of the SiO_2 thickness below 2.0 nm is problematic due to the rising gate leakage current [1.20, 1.21] as seen in Fig. 1.4. This exponential increase in gate leakage current has caused significant concerns regarding to the operation of CMOS devices, particularly standby power dissipation, reliability, and lifetime.

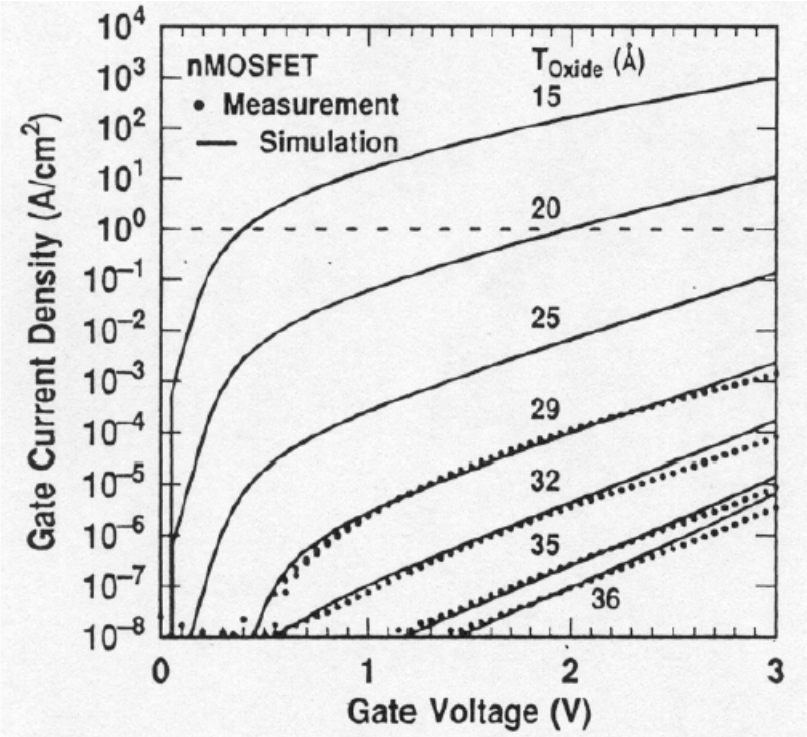

Fig. 1.4 Gate leakage versus gate voltage for various oxide thicknesses [1.20].

Nitrided silicon oxides (silicon oxynitrides, SiO_xN_y) have extended the limit of oxide thickness a little further as it has been shown to be beneficial for reduction of the leakage current, reliability enhancement, and suppression of B penetration [1.22, 1.23]. Although an extension of oxynitride to less than 1 nm may satisfy the device reliability requirement for high performance applications, it will no longer meet the strict leakage current requirement in high performance logic applications as well as low standby power applications as seen in Fig. 1.5 and 1.6.

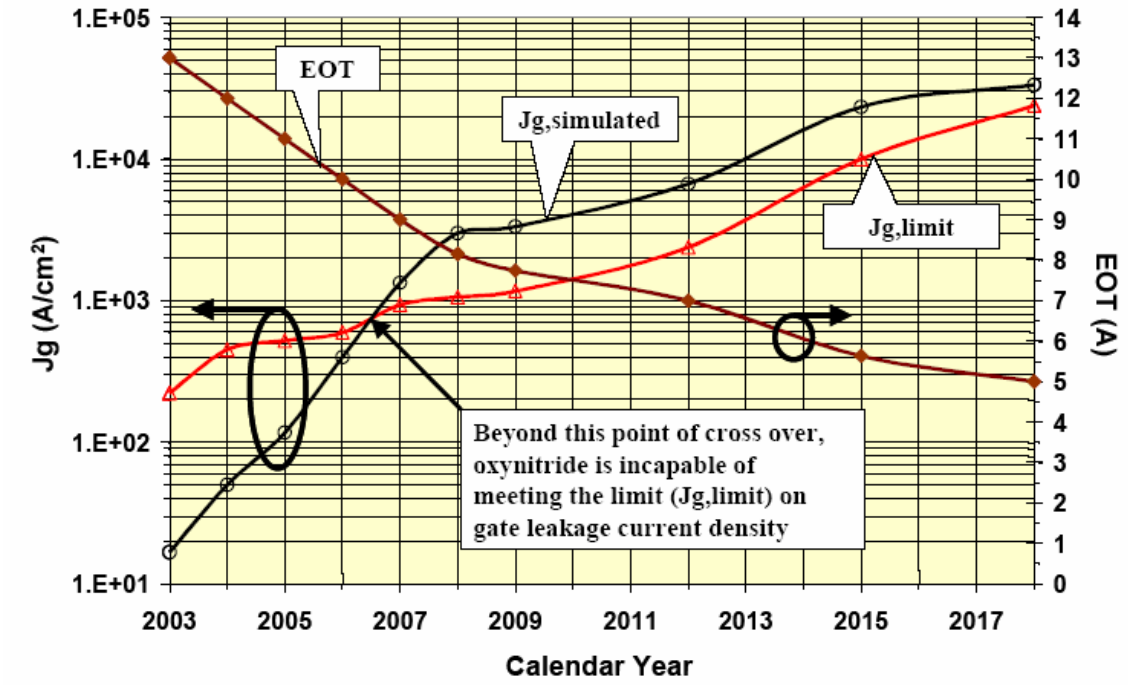

Fig. 1.5 High-performance logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling [1.2].

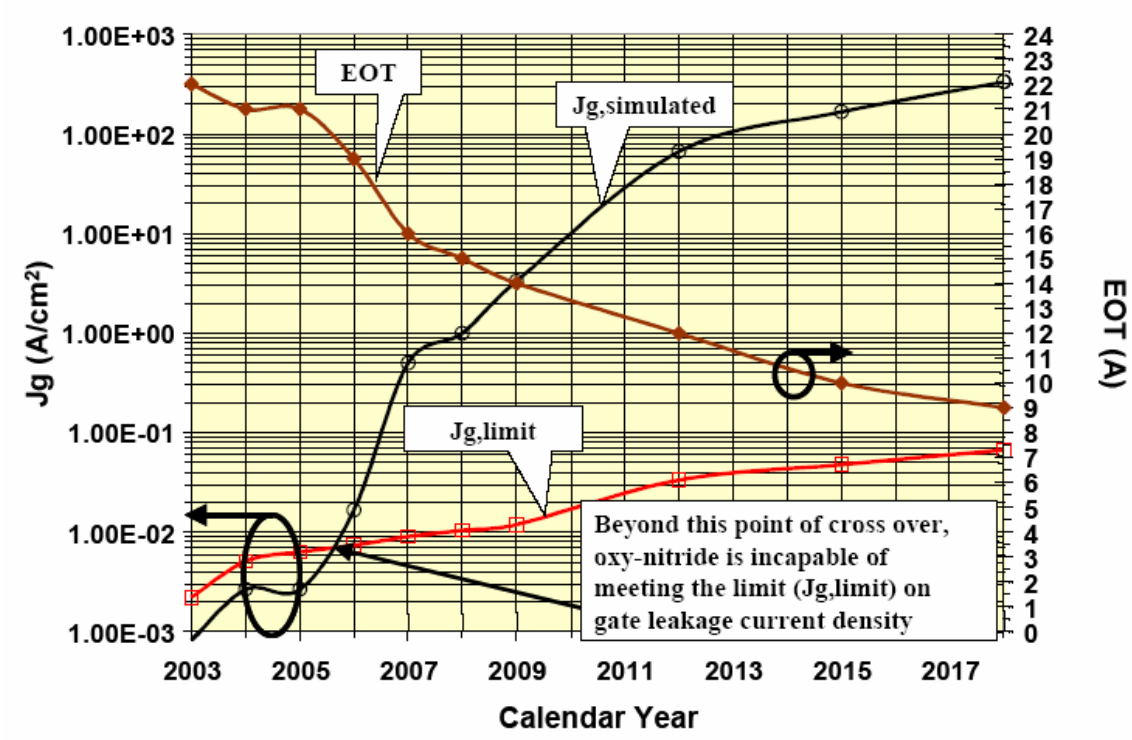

Fig. 1.6 LSTP logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling [1.2].

Practical solutions to reduce the gate tunneling current have been proposed and demonstrated through introduction of high dielectric constant (high K) gate dielectrics. The use of high-K gate dielectrics allows to use physically thicker film to reduce direct tunneling current while maintains the same EOT (equivalent oxide thickness), which is given by

$$t_{EOT} = \frac{k_{OX}}{k_{high-k}} t_{high-k} \quad \text{..... (1.1)}$$

where k_{ox} and k_{high-k} are the dielectric constant of thermally grown SiO_2 and high-K dielectric material, and t_{EOT} and t_{high-k} are the equivalent oxide thickness and the physical oxide thickness of high-K dielectric material. Hence, high-K dielectric material is a potential solution to solve the problem of high gate leakage current density.

1.2.2 Candidates of High-K Dielectric

Initially, Al_2O_3 has been widely studied as a high-K dielectric, whose k value is 9 - 11 [1.24]. However, when Al_2O_3 is used, the threshold voltage is high due to the large negative fixed charge incorporated in the film [1.25, 1.26]. HfO_2, its silicate and aluminate, and their nitrogen incorporation have been widely investigated and practically demonstrated. Although the silicate and aluminate and N incorporated films show relatively lower dielectric constant than the corresponding value for their pure oxide, the resulting values, k ≈ 12-20 appear to be sufficient for the transistor performance.

1.2.3 Scaling Challenges in High-K Dielectric

There are several factors that affect EOTs of high-k gate dielectrics. These include bulk material properties, deposition and post deposition annealing conditions, interfacial interactions due to subsequent thermal processing between the high-K gate dielectric and the silicon substrate as well as between the high-k material and the gate electrode. Surface chemistry is important as both the thickness of interface layer and the quality of surface can be determined. HF cleaning followed by NH_3 treatment is very effective for reducing EOT. However, mobility degradation can occur due to N incorporation at the bottom interface [1.27]. Chemical oxide growth on the Si surface may have better mobility than the NH_3 pretreated surfaces [1.28] but will limit further scaling of EOT. Post deposition annealing conditions also affect interfacial layer thickness, hence EOT.

1.2.4 Carrier Mobility

Mobility is also a key parameter influencing transistor performance. In general, it has been observed that mobility increases with decreasing high-K thickness due to

reduced total coulomb scattering, which is attributed to charges in the high-k. As shortly discussed above, mobility can be somewhat controlled by the interfacial layer thickness because the screening effect can be enhanced with the interfacial oxide [1.28]. More effectively, it is improved by the replacement of polysilicon gate with metal gate electrode [1.8, 1.47].

1.2.5 Threshold Voltage Instability

Another key issue associate with the high-k gate dielectric is threshold voltage control. An asymmetric threshold voltage shift has been observed for all high-k dielectrics with polysilicon gate electrodes. Recent report has addressed Fermi level pinning due to metal-Si bonding at the upper interface [1.29]. Dopant penetration, particularly boron penetration into high-K dielectric also causes an uncontrollable shift in threshold voltage. Adding a relatively small amount of nitrogen to the high-k dielectric is expected to suppress the boron diffusion through the dielectric [1.30], as has been generally effective with current SiO_xN_y applications [1.22]. A possible solution to both of these issues is the implementation of metal gate electrodes although the metal gates also have Fermi level pinning.

1.2.5 Thermal Stability of High-K Dielectrics

It appears that most of high-K dielectric films are amorphous when as-deposited. However, during the subsequent thermal process, the films may become crystallized. Polycrystalline phase of dielectric films can result in increase of thickness non-uniformity due to the formation of grains and increase of leakage current through the grain boundary. The critical temperature for crystallization can vary according to the film composition, film thickness, and incorporation of additional impurities into high-K dielectric. For Hf-based high-K dielectrics, N, Al, and Si have been used to be

incorporated into the high-K dielectrics to improve their thermal stability. The thermal stability of dielectric films depends on the concentration of each impurity in high-K dielectric. However, since too high concentration of impurity may decrease K value of dielectric, the incorporation level should be controlled carefully. Besides, non-uniform distribution of impurity in high-K dielectric film may lead to adverse effect on device performance because impurities diffused into the bottom interface may cause carrier mobility degradation and V_{th} instability [1.31].

1.3 Metal Gate Technology

1.3.1 Limitations of Polysilicon Gate

Polysilicon is currently the most widely used gate material for MOSFETs because it has an excellent compatibility with Si CMOS process and can be easily formed for dual gates. The use of dual n^+/p^+ polysilicon gates sets a symmetric and the most suitable threshold voltages for both p- and n-channel bulk MOSFETs. However, when the active carrier concentration in the polysilicon is not sufficient, the band bending in the polysilicon becomes voltage-dependent. As the device is biased such that the Si substrate is inverted and a channel is formed, the polysilicon gate becomes depleted of free carriers and a significant voltage fraction is dropped across the gate electrode, which is caused by polysilicon depletion as shown in Fig. 1.7.

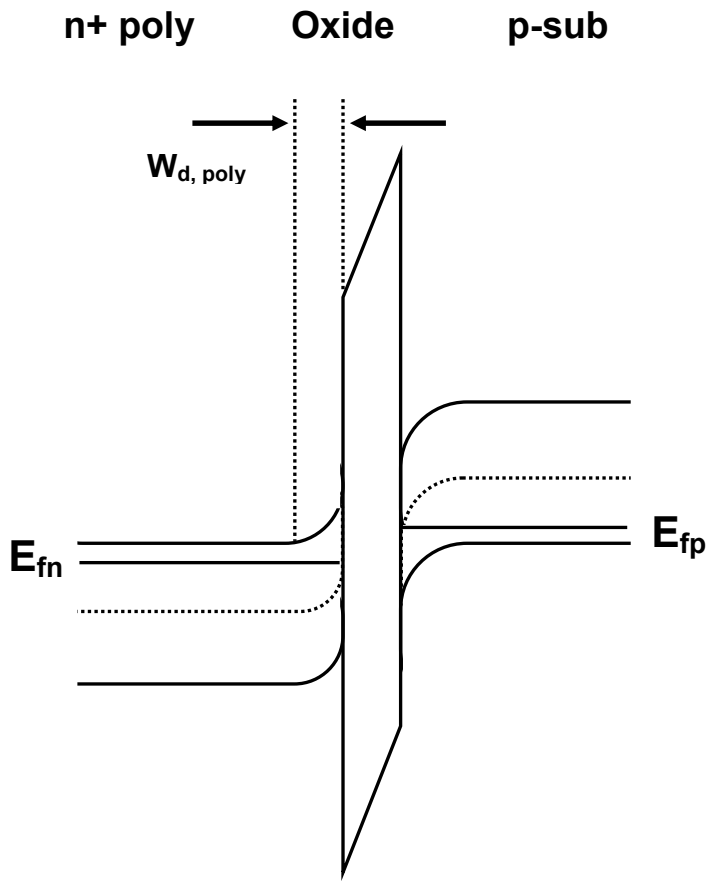

Fig. 1.7 Polysilicon depletion increases the EOT of gate dielectric when the channel is in inversion. The added thickness is equivalent to $W_{d,\,poly}$.

Gate capacitance is reduced due to the polysilicon depletion, indicating the increase of equivalent-oxide thickness at inversion. Considering the fact that an equivalent gate oxide of less than 1.5 nm at inversion is required for the coming technology nodes, this impact of polysilicon depletion is very critical. Although polysilicon is still considered as the best gate electrode, polysilicon depletion and dopant penetration are still challenges as devices become smaller.

Another concern on polysilicon gate is an issue on the compatibility of polysilicon gate with high-K dielectric, which has been widely studied recently. The introduction of high-K dielectrics for gate dielectric brings about a new problem, which is an interfacial reaction of high-K film and polysilicon during subsequent thermal processing. This reaction will change the effective work function of polysilicon due to Fermi level pinning effect [1.32, 1.33].

However, the insertion of metal gate electrodes may also bring about other problems in terms of device reliability, process integration and new types of defect generation and detection. Therefore, careful consideration of metals for gate electrode is needed. The following section describes the required material properties for metal gate electrode and the need of work function engineering. Proposed methods for integrating dual metal gates are shown and the results are also discussed.

1.3.2 Material Consideration for Metal Gate

The metal for the gate electrode application must have a right work function and a low resistivity and also should possess all the good characteristics of polysilicon that are qualified for the gate application. It should be stable with the gate oxide, have low mechanical stress to stand up the high processing temperature without mechanical failure and not be oxidized during the process. The thermodynamic stability of metal/dielectric interface at processing temperatures is an important issue. Electrically, it should be free

of mobile charge, have low surface states, and satisfactory breakdown strength. In addition, the more subtle issues of electrical properties are flat band voltage stability, which becomes ultimately threshold voltage stability and charge trapping characteristics. Interface control between metal and gate oxide is also a determining factor.

In terms of fabrication process, metal etching and metal gate patterning by RIE and stopping of the ion channeling during source-drain ion implantation are required. To meet those requirements, refractory metals and their silicides are natural candidates because of their high temperature stability. Refractory metal silicides in general are not as attractive as refractory metals for two reasons. First, their resistivity is in general higher than metals' resistivity. Secondly, they have high stress and poor adhesion to the oxide. More details on candidates are discussed in the following subsections.

1.3.3 Metal Candidates

Many refractory metals are good choices for this application primarily on account of their high melting points, which allow them to be used at the high temperatures necessary for source/drain activation. Some metals such as W and Mo have been studied [1.34, 1.35]. However, the use of refractory metals introduces the additional complexity of etching, especially for dual metal gates, such as selectivity and suitable masking procedures to selectively deposit metals over different areas of the same wafer, as seen in Fig. 1.8. In addition, since most of the refractory metals have the work function close to the mid-gap of the silicon, work function tuning for dual metal gates is difficult.

Some of nitrides including TiN, TaN, TaSiN, TiAlN and HfN are distinguished from the others by their exceptional mechanical and electrical properties [1.36-1.40]. These compounds are frequently called refractory metal nitrides due to their extremely

high melting points. The excellent high temperature stability, hardness, relatively low resistivity and corrosion resistance are attractive to many applications.

Full silicidation (FUSI) has widely been demonstrated. The FUSI process has been considered to be an alternative way for dual metal gate in CMOS processing because of compatibility with conventional processing. Recently FUSI Ni-silicide and Co-silicide have been proposed for gate application [1.41, 1.42]. Since it has been reported that the work function of Ni-silicide has a dependence on dopant in polysilicon, Ni-silicide have been considered as a promising candidate for dual metal gate process [1.43-1.45]. However, the compatibility with high-K dielectric is still concern because unstable interface between polysilicon and high-K dielectric can also affect the interface between silicide and dielectric after silicidation [1.46]. In addition, it may not be free from Fermi level pinning problem [1.47].

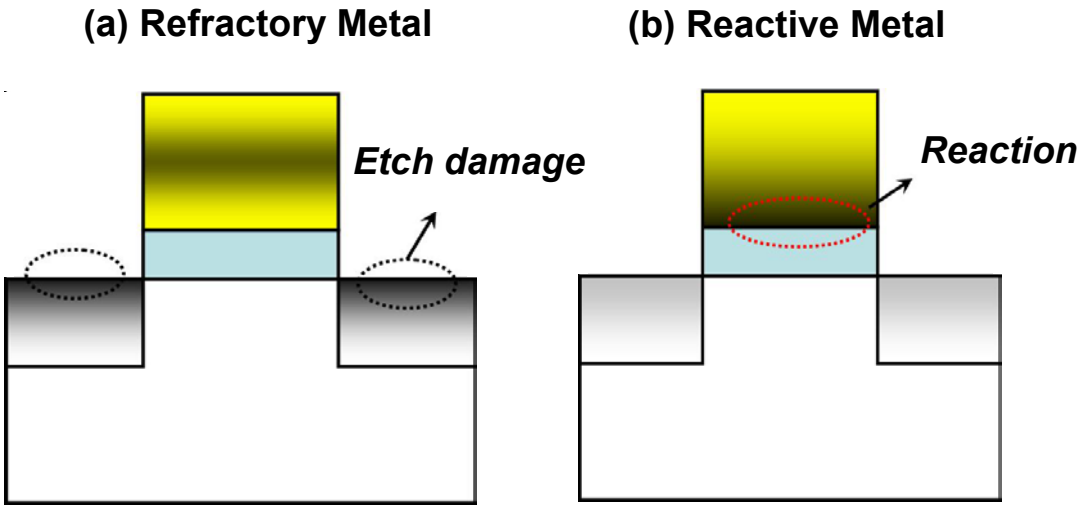

Fig. 1.8 Two considerations of selecting a metal for gate electrode.

1.3.4 Work Function

The most direct impact of the gate electrode on the operation of a MOSFET is through its control of the device threshold voltage (V_{th}). The voltage required for the onset of inversion in MOSFET channel can be determined by the work function of the gate electrode. In MOSFET, the threshold voltage of a surface channel device can be expressed as:

$$V_{th} = V_{FB} + 2\phi_B \pm \gamma\sqrt{\phi_B} \qquad (1.1)$$

where ϕ_B is surface potential at strong inversion, which is equivalent to $2\phi_f$. γ is body effect factor depending on doping concentration in Si substrate, which is given by

$$\gamma = \frac{\sqrt{2\varepsilon_S qN}}{C_{ox}} \qquad (1.2)$$

where ε_S is permittivity of Si and N is the doping concentration in Si substrate.

V_{fb} is the flat band voltage across the MOS stack. V_{fb} is given by the following expression:

$$V_{fb} = \Phi_{MS} - \frac{Q_f}{C_{ox}} \qquad (1.3)$$

where Φ_{MS} denotes the work function difference between the metal gate and the Si substrate and Q_f the magnitude of fixed charge in the dielectric film. The threshold voltage of MOSFET is thus directly controlled by the gate electrode through the work function difference between the gate and the substrate.

1.3.5 Work Function Determination

A practical way to estimate the work function of gate electrode is using a plot of V_{fb} versus gate oxide thickness [1.48]. The V_{fb} for the capacitors with various gate electrodes can be determined from high-frequency C-V measurements, and plotted as a

function of gate oxide thickness (T_{ox} or EOT for high-K dielectric). Φ_{MS} can be extrapolated from the flat-band voltage data according to equation (1.3).

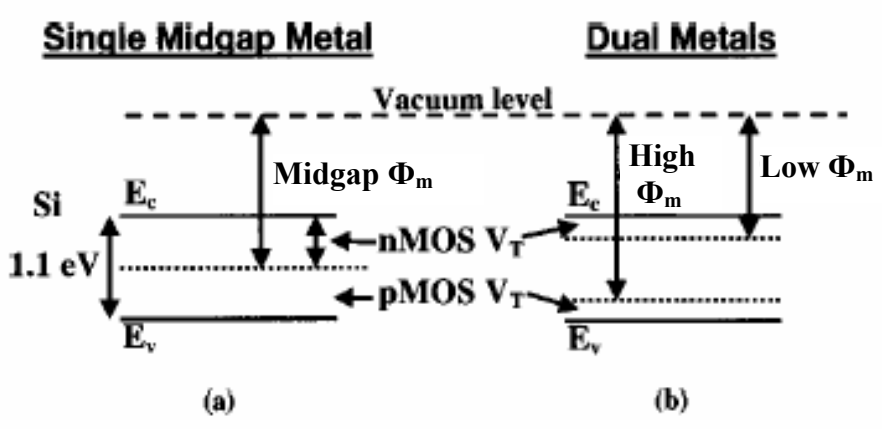

Fig. 1.9 Energy diagrams of threshold voltages for nMOS and pMOS devices for (a) midgap metal gate and (b) dual metal gate.

1.3.6 Work Function Consideration

Single mid-gap metal gate and dual metal gate are two approaches in achieving surface channel operation for both types of devices in the CMOS technology. Figure 1.9 shows that for a single gate, the work function of gate metal should be near midgap of Si while both metals should be near band edges of Si for dual gates. Midgap metal gate can provide CMOS devices with symmetric threshold voltages (V_{th}) for nMOS and pMOS, and have advantage of simple process integration. However, the V_{th} limits of both n- and p-MOS for midgap metal have been known to be about 0.5 V. Since 0.5 V of V_{th} may be too large for 0.1 um technology and beyond, channel engineering such as counter doping should be considered to adjust and obtain a proper V_{th} for device operation [1.49].

When using dual metal gates: n-type metal for n-channel devices, and p-type metal for p-channel devices, the overall process will be more complicated. However, in

order to obtain low and symmetrical threshold voltages in nMOS and pMOS devices and minimize short channel effects, proper work functions separated by roughly the band gap of Si for nMOS and pMOS devices are required. A simulation indicates that for an optimum combination of short channel performance and device drive current, gate work functions for bulk-Si CMOS transistors should be between ± 0.2 V of E_c (E_v) for nMOS (pMOS) [1.50].

1.3.7 Effect of Surface Doping Concentration

When using a single mid-gap gate material, the surface doping level required for surface channel operation is lower as shown in Fig. 1.10. Thus, the field is reduced and the electron mobility is increased compared to that of dual gate devices. When the surface concentration of surface channel devices is too low, the short channel effect will become worse. Scaled bulk-Si MOSFETs typically need high dopant concentrations in the channel regions to prevent the drain depletion region from penetrating excessively in the channel, leading to poor short-channel performance. However, high level channel doping typically degrades carrier mobility in the channel. Bulk-Si and Partially Depleted SOI devices need work functions near band edges of Si while midgap work functions may be suitable for Fully Depleted SOI devices [1.51] as shown in Fig. 1.11. Ultra-thin body FETs and vertical transistor structures that use a double gate structure such as FinFET typically use undoped Si channels since the thin Si body automatically enhances the short channel performance of the device by eliminating subsurface leakage paths between the source and the drain.

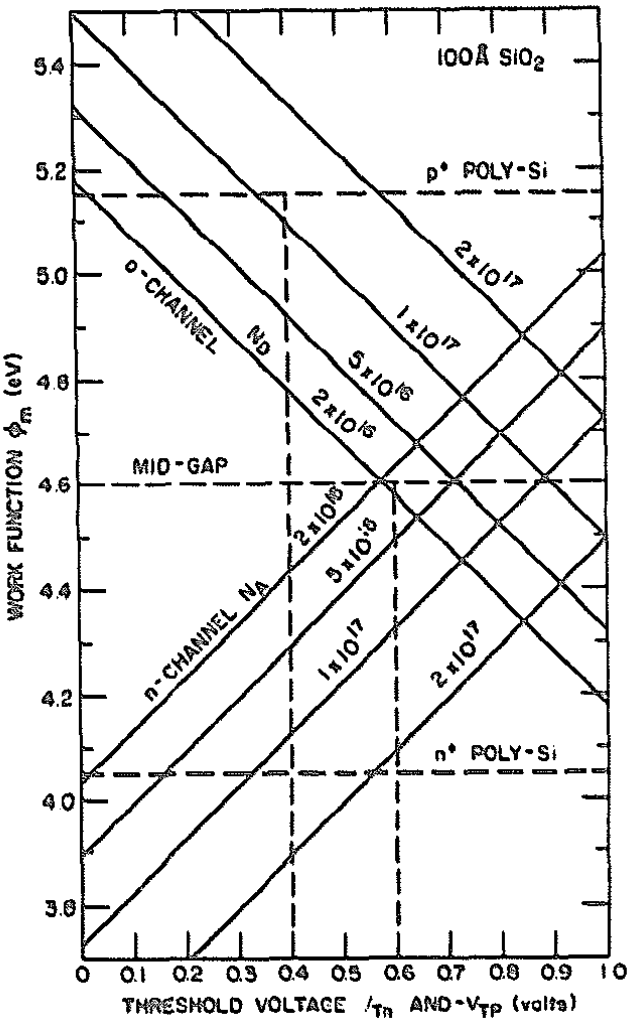

Fig. 1.10 Threshold voltage vs. gate work function for both n and p-channel devices with different surface concentration superimposed.

For such advanced device structures using fully depleted Si channels, the gate work functions on the n and pMOS devices need to be closely centered near the intrinsic Si Fermi level ± 0.2 V of E_i i.e. 4.4 V and 4.9 V for n and pMOS devices, respectively [1.16] as seen in Fig. 1.12.

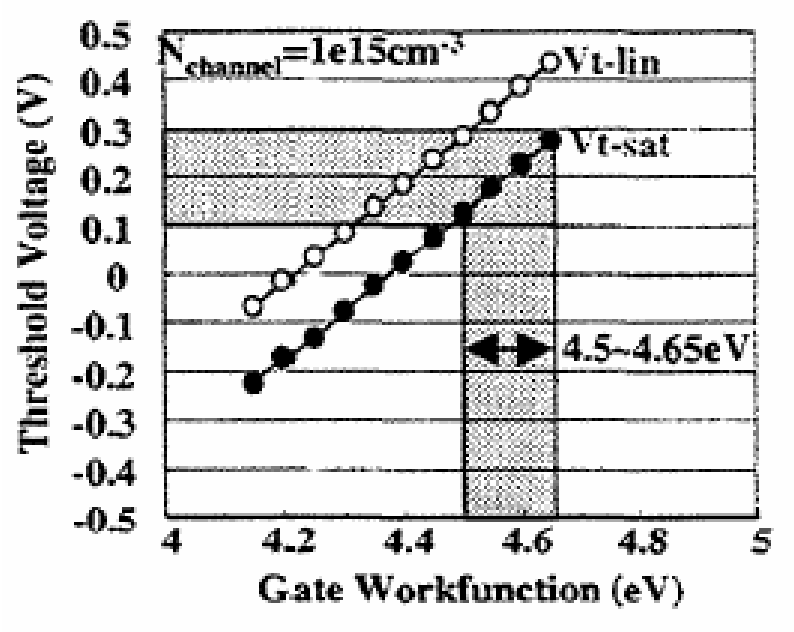

Fig. 1.11 Threshold voltage vs. gate work function for SOI devices [1.51].

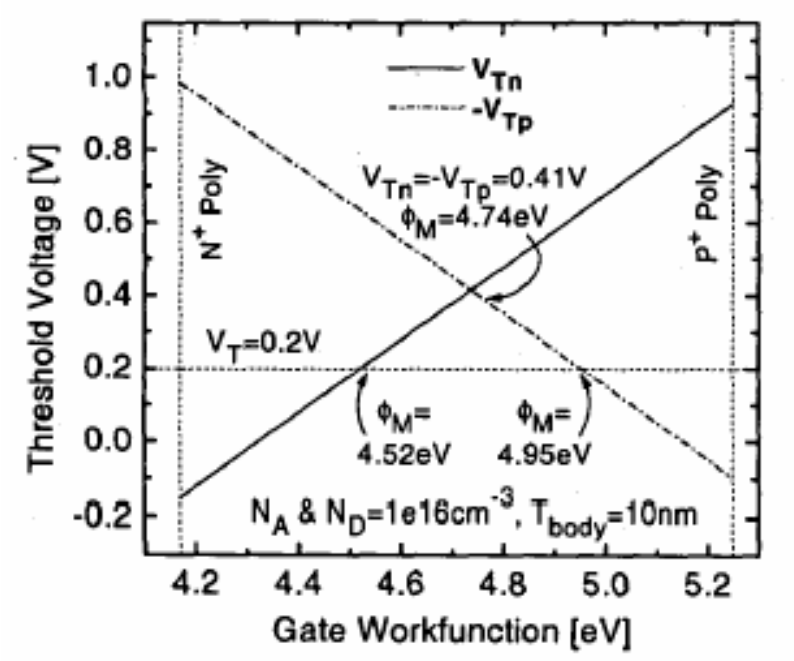

Fig. 1.12 Threshold voltage vs. gate work function for thin body devices [1.16].

1.3.8 Work Function Variation with High-K Dielectric

Instability of polysilicon on high-K has been observed at the interface due to reaction of polysilicon and high-K dielectric. Metal gates have been attempted with high-K gate dielectrics to overcome the reaction problem at the gate interface. However, another important consideration in the selection of metal gate electrodes is the work function modulation when contacted to high-K dielectrics. In general, the work function of a metal at a dielectric interface is different from that in vacuum. The dependence of the metal work function on several gate dielectrics has been explained using experimental data in conjunction with interface dipole theory [1.52]. The work function of polysilicon gates on high-K, especially Hf-based high-K dielectrics is not consistent with that on SiO_2, which is due to Fermi level pinning. It is attributed to metal-Si, especially Hf-Si, bonds at the interface of high-K dielectric and gate electrode [1.47].

1.3.9 Process Integration of Dual Metal Gate

As discussed above, symmetric and lower threshold voltages (V_{th}) for both n and pMOS can also be achieved by dual metal gates because the control of Vth can be controlled by work functions of gates. Accordingly, dual metal gates need two different work functions of metals, one for pMOS and the other for nMOS devices. Two metals should be chosen by their work functions so that Fermi levels of metals line up favorably with the conduction and valence bands of Si, respectively. Several methods of integrating dual metal gates have been proposed.

One is to use wet etching to remove a part of a metal deposited before another metal deposition. Fig. 1.13 shows that an integration of dual metal gates using selectively etched TiN and subsequently deposited Mo on the gate oxide that TiN is removed was demonstrated [1.53]. Although it may be the easiest way and most compatible with Si

processing, a specific chemical etching process without causing damage to gate dielectrics is required. Once a dielectric is exposed to the wet chemical after metal is removed, the quality of gate dielectric may be degraded because the chemical may react with the dielectric and a residue from the chemical may be left on the gate dielectric. In addition, there has been no study on how to prevent the gate dielectric from being exposed to chemical.

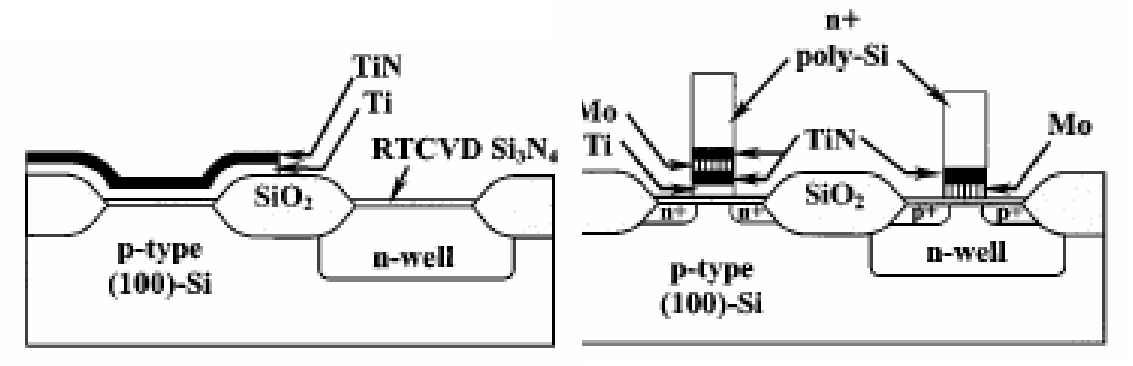

Fig. 1.13 Dual metal gate process using wet etching. Mo and Ti were used for gate electrode of pMOS and nMOS, respectively. TiN/Ti stack was removed away by SC1 chemical.

Another way for dual metal gate is to employ selective implantation to adjust the work function of a metal, as illustrated in Fig. 1.14. As dual metal gates implemented using N implantation, TiN and Nitrogen (N) implanted TiN_x [1.54] and Mo and N implanted MoN_x [1.55] have been reported. It has been suggested that a work function of a metal can be tuned by incorporating N into the metal. However, the range of change in the work function by N incorporation was not wide enough for bulk Si MOSFET although it may be suitable for Thin-Body MOSFET or FDSOI MOSFET [1.16, 1.51]. In addition, the implantation process may cause damage to gate dielectric.

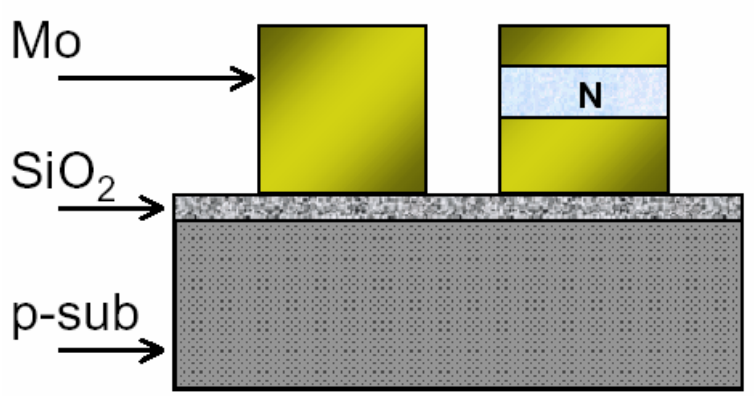

Fig. 1.14 Dual metal gate process using nitrogen implantation. Mo and N implanted Mo (MoN_x) were used for gate electrode of pMOS and nMOS, respectively.

The use of interdiffusion between two metals [1.56] and the reaction of both metals [1.57] was also proposed. Fig. 1.15 shows a process using interdiffusion of metals. Interdiffusion of two metals may offer a good solution for integrating dual metal gates but it is applicable only to the gate last process in which thermal stability of the metal gate is not an issue. This indicates that the use of interdiffusion for the conventional process may not be feasible because thermally stable metals are required for subsequent thermal processing. Another group proposed that two different metal gates can be obtained by the reaction of two different metal stacks at high temperature [1.57]. However, an actual demonstration for dual metal gates was not done successfully. In addition, a low work function of metal using the reaction of metals was not obtained by this reaction process.

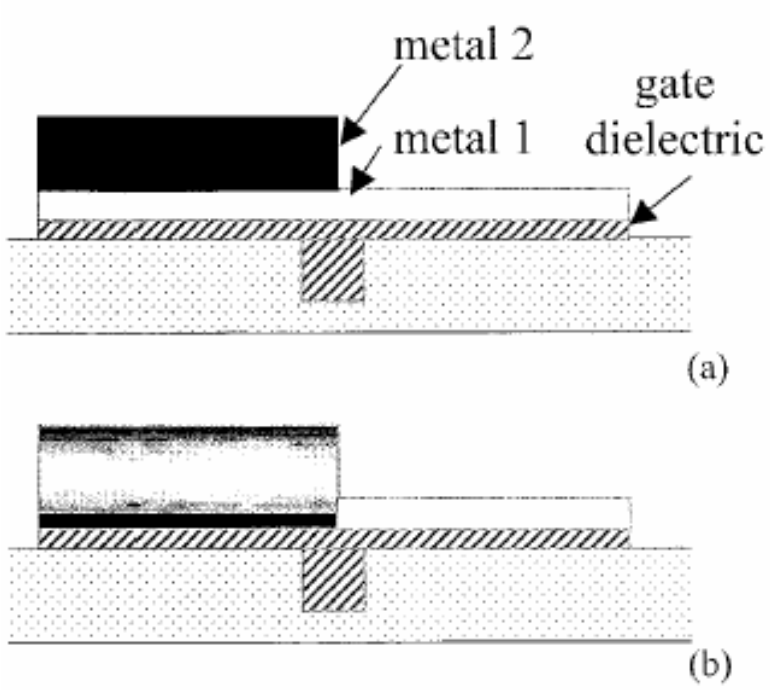

Fig. 1.15 Dual metal gate process using metal interdiffusion. Ni (metal 2) and Ti (metal 1) were used for gate electrode of pMOS and nMOS, respectively. Ni was located on top of gate dielectric through diffusion.

Lastly, fully silicided (FUSI) silicide gates such as $CoSi_2$ and NiSi have recently been proposed [1.41 – 1.45]. Both FUSI gates have been demonstrated for implementing dual gates as seen in Fig. 1.16. FUSI process has been very attractive for CMOS device fabrication because of its compatibility with conventional Si processing. The fabrication sequence using FUSI NiSi is almost the same as the conventional process. A wide range of work functions was also achieved using pre-doping of polysilicon. However, FUSI gates may not be thermally stable because of the diffusion of metal impurities into gate dielectric during subsequent thermal processing, and there has been little study on the thermal stability of FUSI gates. In addition, it is expected that FUSI process may not go well with high-K dielectrics due to the reaction of high-K and silicide [1.46].

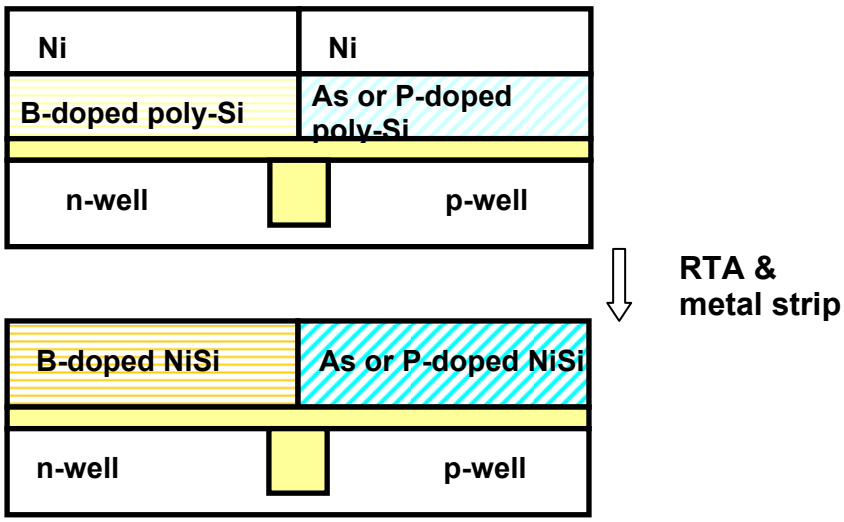

Fig. 1.16 Dual metal gate process using full silicidation (FUSI). Ni-silicided B-doped polysilicon and Ni-silicided As (or P)-doped polysilicon were used for gate electrode of pMOS and nMOS, respectively.

1.4 Objectives

The challenging issues on the device scaling have accelerated innovative works on material properties related with gate dielectrics and gate electrodes. For the metal gate, especially, the integration of dual metal gates is becoming more critical as projected in ITRS roadmap [1.2]. However, not many proposals have been made and no promising way of dual metal gates integration has been reported. For the high-K dielectrics, one challenge is a matter of how to improve the thermal stability of high-K dielectric. Although some approaches using N and Al incorporation into high-K dielectric have been proposed, problems such as EOT increase and mobility degradation may occur because of the diffusion of Al and N to the bottom interface. Thus the objectives of this thesis are to propose and demonstrate possible solutions for the issues described above.

For the metal gate study, this thesis describes the results of several new approaches for the integration of dual metal gates. A novel way of integrating dual metal gates using a very thin AlN buffer layer will be discussed. A discussion of how the thin AlN layer can be used for dual metal gate integration is included. This thesis also presents a full silicided Hf-silicide metal gate capable of implementing dual metal gates. A wide range of work functions obtained using this approach will be discussed. The substitution of Al with polysilicon will be described as another approach. In addition, a new phenomenon observed at the interfaces between various gates and high-K dielectrics will be discussed.

Additionally, this thesis describes if a thin AlN layer can be used to incorporate Al and N into HfO_2 gate dielectric, forming HfAlON/HfO_2 stack. Furthermore, the thesis will deal with the implementation of HfAlON/HfO_2 stack dielectric using a thin AlN

layer and discuss the thermal stability, the electrical properties and the adverse effects such as mobility degradation of the new gate dielectric stack.

1.5 Significance and Organizations

As described, MOSFET scaling will accelerate the utilization of metal and high-K material as gate stack. Especially, aggressively scaled CMOS devices will be in the need of dual metal gate although dual metal gate integration is still a challenge today. At present, therefore, the investigation of high-K dielectric and metal gate may be very appropriate and timely for the development of advanced CMOS technology.

In this thesis, novel approaches for integration of dual metal gate will be the main focus. Additionally, a new method to improve thermal stability of HfO_2 high-K dielectric will also be discussed. The thesis is organized as follows. Chapter 2 will discuss gate work function engineering using aluminum nitride (AlN) buffer layer and cover experimental results of modified work functions of new metal alloys. Through electrical and physical characterization, a role of buffer layer for work function engineering and insight into the mechanisms behind the observed results will be discussed. In Chapter 3, the application of fully silicided Hf-silicide for NMOS will be reported and possible way for dual metal gates using HfSi is proposed. Chapter 4 will discuss MOS characteristics of substituted Al metal gate on HfAlON high-K dielectric. The results demonstrate low work function and no Fermi level pinning through substitution of Al for polysilicon, and a possible process scheme for dual metal gate integration will be proposed in Chapter 4. Chapter 5 will cover MOS characteristics of Pt rich Pt-silicide metal gate. High work function required for pMOSFET and less Fermi level pinning will be discussed. Chapter

6 will discuss the other application of AlN on high-K gate dielectric is discussed. Finally, conclusion and recommendations will be addressed in Chapter 7.

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Chapter 2

Dual Metal Gate Integration using AlN Buffer Layer

In this chapter, a new approach for dual metal gate CMOS process integration is discussed. This new way was successfully demonstrated using an ultra thin aluminum nitride (AlN) buffer layer between metal gate and gate dielectric. The buffer layer prevented the gate oxide from being exposed to a metal etching process and played a key role in determining the work functions at the metal/dielectric interface. During annealing, this buffer layer was completely consumed through the reaction with metal gate and converted into a new metal alloy, resulting in no increase of EOT. The work functions of the original gate metals were modified as a result of this reaction, making this approach attractive for dual metal gate CMOS applications.

2.1 Introduction

Some approaches for dual metal gates fabrication such as ion implantation, selective etching and metal interdiffusion have been proposed [2.1 - 2.7]. However, process integration of dual metal gate technology still faces several challenges. Firstly when it comes to wet etching process, especially selective removing of the first metal from either the nMOS or pMOS regions will expose the thin gate dielectric to etching chemical. It inevitably results in gate dielectric loss during metal etching and/or contaminants adsorption onto gate dielectric from the chemical solution, which may cause gate dielectric reliability problems. Secondly, ion implantation into a metal has been tried to achieve dual work function. In this case, an impact to dielectric can be encountered due to ion implantation to gate electrodes as reported previously [2.8], leading to gate dielectric degradation. Additionally, there are other reported issues such as metallic contamination to the gate dielectric due to metal diffusion and not sufficient range of work function shown in fully silicided metal-silicide gates [2.9, 2.10]. Nevertheless, most promising way is still to use wet etching process for removing one part of metal gate electrode as it is compatible with the conventional CMOS processing. In order to mitigate the damage or loss of gate dielectric during the wet etching of one part of metal electrode on top of gate dielectric, a thin buffer layer can be stacked between gate metal and dielectric to protect the gate dielectric during metal etching. Since AlN has a strong chemical resistance [2.11], it can be used as a protection layer of gate dielectric during gate metal etching. In this study, we evaluate the feasibility of thin AlN as a buffer layer for dual metal gates process and also study the behavior of work function through the reaction of AlN and metal, which may introduce a possible way to integrate dual metal gate CMOS.

In this chapter, a novel technique for dual metal gate process using an ultra-thin, consumable dielectric buffer layer between gate dielectric and metals is proposed and demonstrated. This is integratable and compatible with standard CMOS process.

2.2 Experiment

Figure 2.1 shows the process sequence of the proposed dual metal gate process using a dielectric buffer layer between gate dielectric and metal electrodes. The requirements for this buffer layer are: (1) it must have a high chemical resistance in order to protect the underlying gate dielectric from being exposed to first metal etching; (2) it must be consumed and converted into metal alloy through reactions with metal gate electrodes during subsequent annealing so that the introduction of the buffer layer must not increase the final EOT; and (3) the work functions of resulting gate electrodes after annealing must be suitable for dual metal gate CMOS. It was identified and demonstrated that ultra thin aluminum nitride (AlN) film can successfully meet these requirements. Furthermore, it can be converted into metal alloy when reacting with metals that have electronegativity below 1.34, such as Ti (1.32), Hf (1.23) and Ta (1.33) [2.12], and therefore modifies the work function of these metals. An ultra thin (~1.0 nm) layer of AlN is deposited first, followed by deposition of the first metal for nMOSFET. The first metal is then selectively removed from pMOSFET region, followed by the second metal deposition for pMOSFET. The sequence of the deposition of two metal films can be swapped depending on the ease of removal of the first metal. The AlN buffer layer prevents the gate dielectric from being exposed during the first metal etching. After gate patterning, an annealing is performed to consume the ultra thin AlN buffer layer as well as react it with first and second metal electrodes, forming metal alloy films with suitable work functions for n and pMOSFETs, respectively.

The MOS capacitors with SiO_2 of several thicknesses were fabricated on p-type (100) Si substrates. AlN was deposited on top of SiO_2, followed by Ta or Hf deposition. An annealing was performed at 420°C for 30 min in a forming gas ambient. Since platinum (Pt) does not react with AlN due to higher electronegativity than 1.34, Pt gate was also prepared to evaluate the property of AlN as a dielectric. Thicker AlN films were also prepared to investigate allowable thickness of AlN as a buffer layer. For some of samples, RTA was done at 600°C followed by annealing at 420°C.

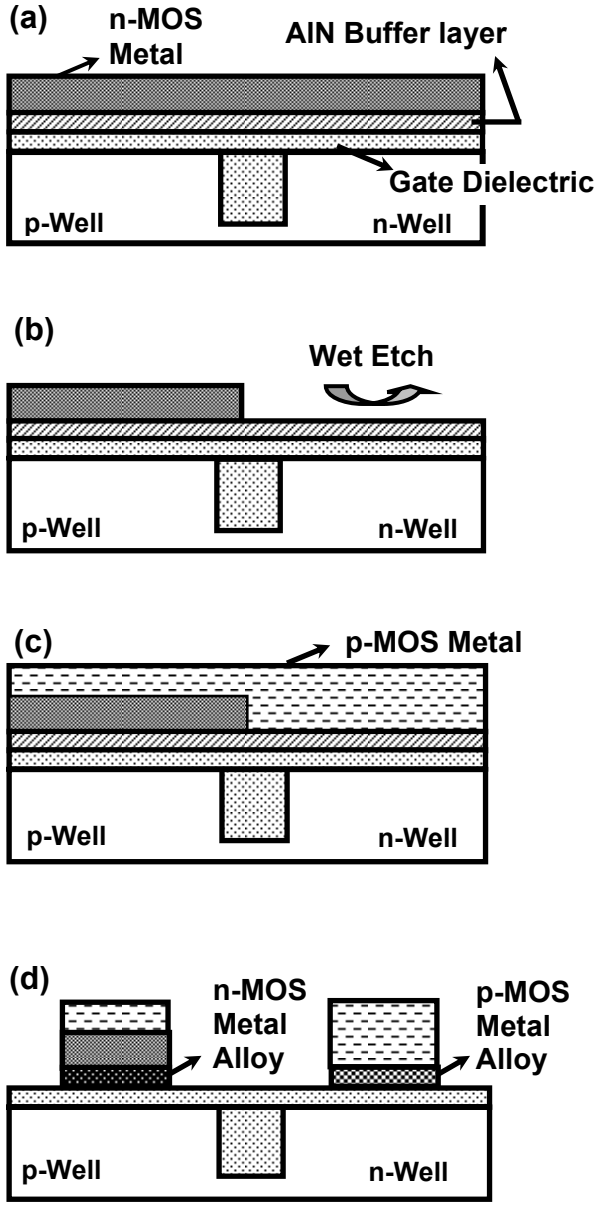

Fig. 2.1 The schematic shows a proposed dual gates fabrication process flow; (a) deposition of first metal for nMOSFET on top of a reactive sputtered AlN buffer layer, (b) wet chemical etching the first metal from the p-MOSFET region, (c) deposition of second metal for pMOSFET, and (d) gate patterning and annealing to consume AlN buffer layer and form new metal alloy films.

2.3 Results and Discussion

2.3.1 Analysis of AlN Film as a Buffer Layer

The AlN deposition rate in this experiment was 1.5 nm/min. The sputtering was done for 30 seconds under 3×10^{-7} Torr of base pressure in order to deposit thin AlN film with thickness of 0.7 to 0.8 nm. The sputtering time was long enough to obtain the thin AlN deposited by reactive sputtering. As seen Fig. 2.2, the lower deposition rate was obtained at low power of sputtering, indicating a wide process window for thin AlN deposition.

The dielectric constant of sputtered AlN was also determined so that EOT of AlN buffer layer can be estimated. To determine the dielectric constant of AlN, Ta/AlN/SiO_2 stacks of MOS capacitors were simply fabricated using shadow mask. From the plot of physical thickness of AlN/SiO2 vs. capacitance equivalent thickness as shown in Fig. 2.2, the dielectric constant of AlN, κ_{AlN}, can be calculated using (2.1),

$$t_{EOT} = \frac{\kappa_{OX}}{\kappa_{AlN}} t_{AlN} + t_{\text{interface}} \qquad (2.1)$$

where κ_{ox} is the dielectric constant of SiO_2, which is known to be 3.9, and $t_{\text{int}\,erface}$ is t_{SiO_2} since the gate stack of the capacitor is AlN/SiO_2. The calculated thickness of SiO_2 from the plot in Fig. 2.3 is consistent with the measured thickness of SiO_2 prior to AlN deposition. The value of dielectric constant obtained form the plot was determined to be about 10, which is consistent with reported data [2.13 - 2.15].

Sputtered AlN film showed a good reproducibility. Figure 2.4 (a) shows the composition of AlN measured by XPS, and the value of x is estimated to be about 1.0. In this study, the value of x was estimated to be about 1.0. The composition ratio of AlN with various flow rate ratio of N_2 and the mixture of N_2 and Ar gases was also examined

by Auger and XPS analysis. The value of x for each flow rate ratio was estimated to be about 1.0 ~ 1.02 in the range of 17% to 35% in $N_2/(N_2+Ar)$ flow rate ratio as seen in Fig. 2.4 (b).

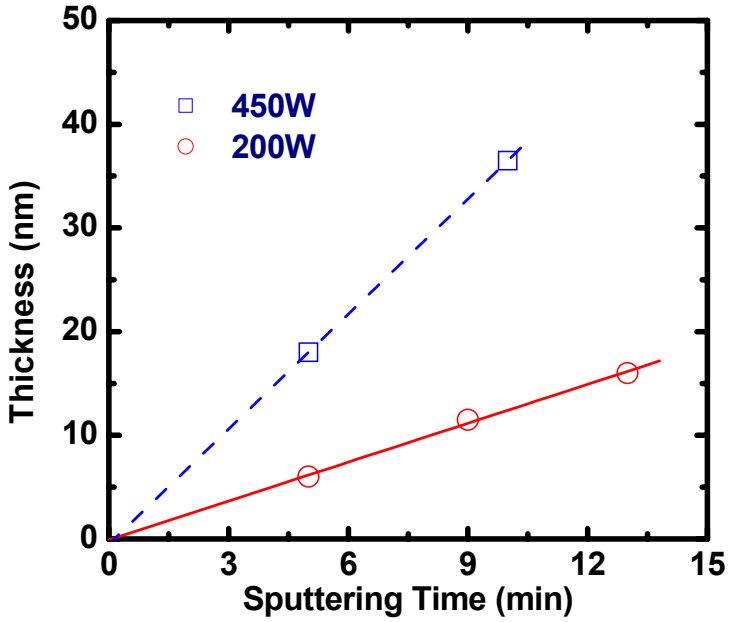

Fig. 2.2 Sputtering rate for AlN deposition with plasma power.

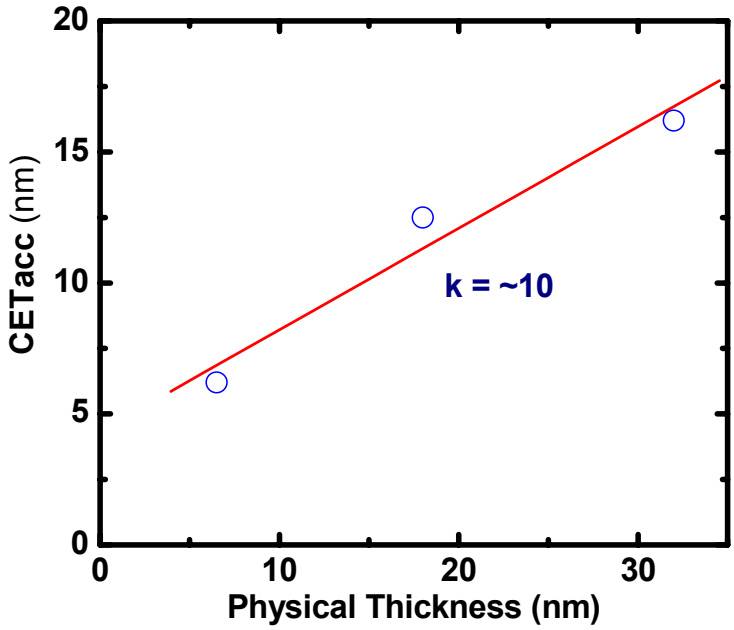

Fig. 2.3 Plot of CET vs. physical thickness of AlN/SiO2 stack gate dielectric.

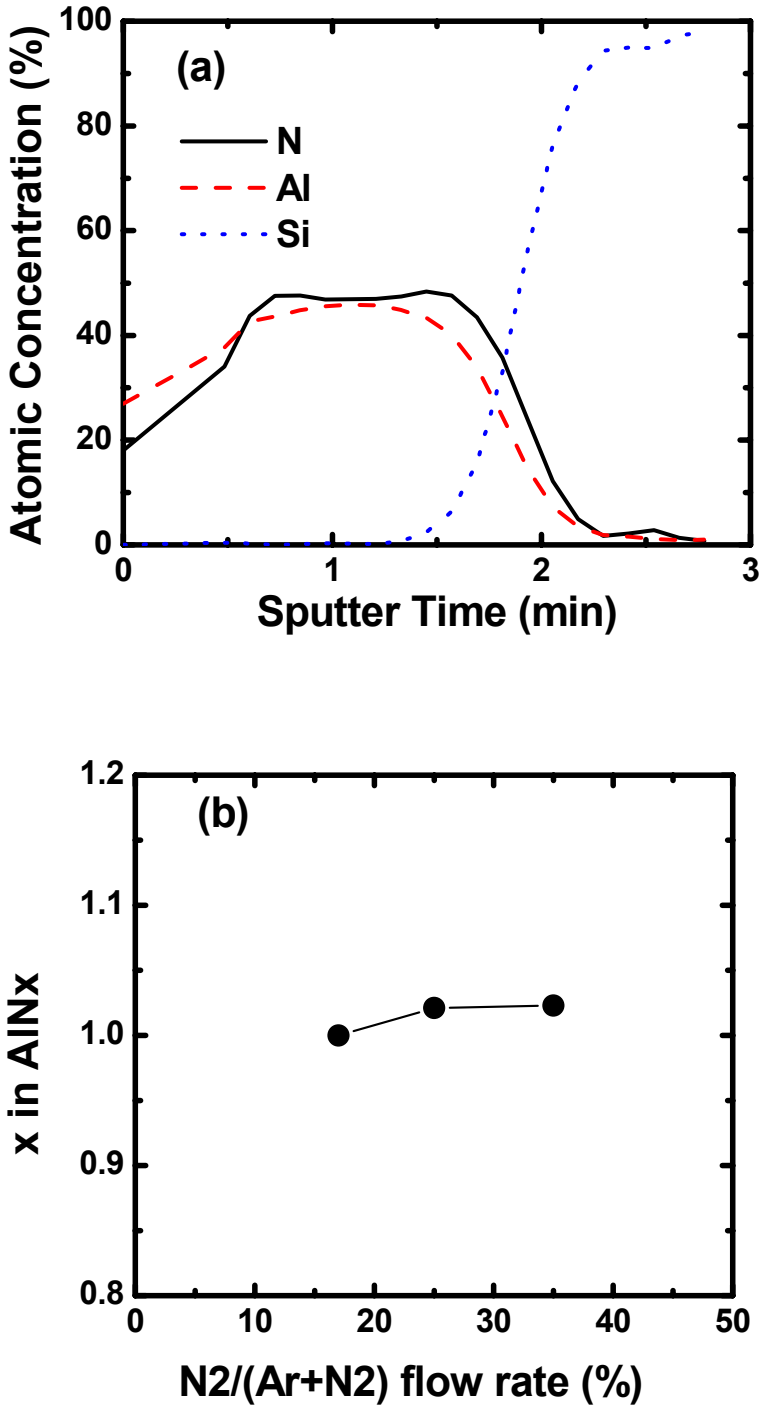

Fig. 2.4 (a) The XPS depth profile of AlN film. (b) Dependence of composition ratio of AlN_x on the process gas flow rate during AlN formation sputtering.

2.3.2 Chemical Resistance of AlN Film as a Buffer Layer

AlN has a very high chemical resistance against chemical etching [2.11]. The etching rates of various films including AlN are summarized in Table 2.1. As seen in the table, AlN shows excellent chemical resistance in both HPM (HF, H_2O_2) and SPM (H_2SO_4, H_2O_2) solutions.

Figure 2.5 shows C-V of Pt/SiO_2 and Pt/AlN/SiO_2 capacitors with 0.7~0.8 nm AlN. Since Pt does not react with AlN due to its high electronegativity, the accumulation capacitance difference between Pt/SiO_2 and Pt/AlN/SiO_2 capacitors is due to the presence of AlN, indicating that the AlN plays a role of dielectric. The EOT difference of 0.3 nm in Fig. 2.5 is consistent with the physical thickness of AlN, considering its dielectric constant (~9.0 to 11.0). The capacitance difference is equivalent to 0.3 nm of EOT, indicating the presence of AlN layer as a dielectric. The two curves for Pt/AlN/SiO_2 capacitors in Fig. 2.5 were from two capacitors with different process histories; one with Pt deposition without interruption, but the other with Pt deposition after intentional deposition and stripping of Hafnium using HF/H_2O_2 mixture solution. These two capacitors show identical C-V, V_{fb}, and leakage current, clearly demonstrating the ability of AlN film as a protection buffer layer during the first metal etching.

Table 2.1 Etching rates of various films. For HPM, 1:1:50 ($HF:H_2O_2:H_2O$) volume ratio was used at room temperature. For SPM solution, 1:4 ($H_2O_2:H_2SO_4$) volume ratio was used at 120 ^oC for etching those films. Sputtered Hf, AlN and thermally grown silicon oxide were used.

(unit: nm/min)

	Hf	AlN	SiO_2
HPM ($HF+H_2O_2+H_2O$)	82	<0.1	6.0
SPM ($H_2SO_4+H_2O_2$)	>100	0	0

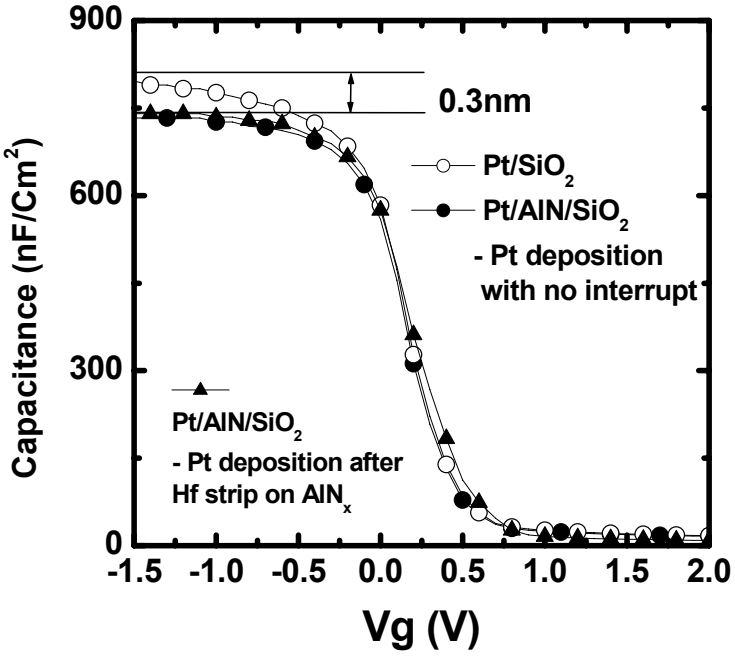

Fig. 2.5 The C-V measurement results on Pt/SiO_2 and $Pt/AlN/SiO_2$ capacitors after annealing at 420ºC in a forming gas ambient. The 0.3 nm increase in EOT is observed by introducing AlN. One of $Pt/AlN/SiO_2$ capacitors underwent deposition of Hf followed by wet chemical stripping before Pt deposition. No noticeable difference is found, indicating that AlN has sufficient chemical resistance during wet etching of the first metal.

2.3.3 XPS Study at Interface between AlN and Metals (Ta, Hf)

The formation of new alloy was analyzed using x-ray photoelectron spectroscopy (XPS). Figure 2.6 shows the XPS spectra of N 1*s*, Al 2*p* and Ta 4*f* at the Ta/AlN interfaces with annealing temperature. For the as-deposited sample, the peak at 397 eV is in excellent agreement with the N 1*s* binding energy of AlN (397.1 eV). With increasing the annealing temperature, the peak is shifted to higher binding energy. The peak of Al 2*p* at 74 eV, which is consistent with the Al 2p binding energy in AlN (73.8 eV), is observed for as-deposited sample. The subsequent annealing leads to the shift of Al 2*p* peak. The Ta 4*f* spectra in Fig. 2.4 (c) also show the similar feature to the N 1*s* and Al 2*p* spectra shown in Fig. 2.6 (a) and (b), which indicates the existence of the Ta-Al-N phase resulted from annealing. The same features of the N 1*s* and Al 2*p* spectra at the Hf/AlN interfaces are also observed in Fig. 2.7, indicating the formation of new alloy layer (Hf-AlN) through annealing.

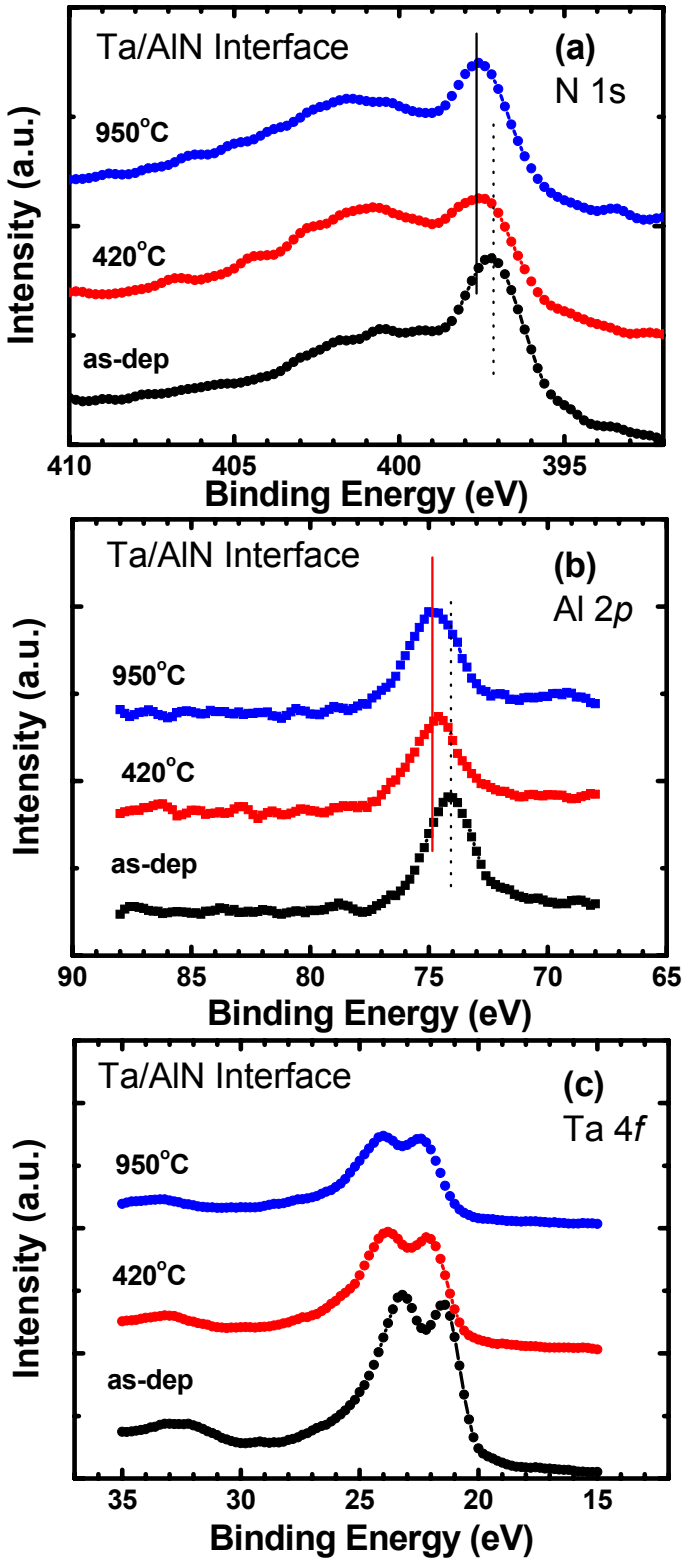

Fig. 2.6 N 1*s* (a), Al 2*p* (b), and Ta 4*f* (c) XPS spectra at Ta/AlN interface before and after annealing at 420°C and 950°C. Binding energy shift after annealing indicates the reaction of AlN with Ta.

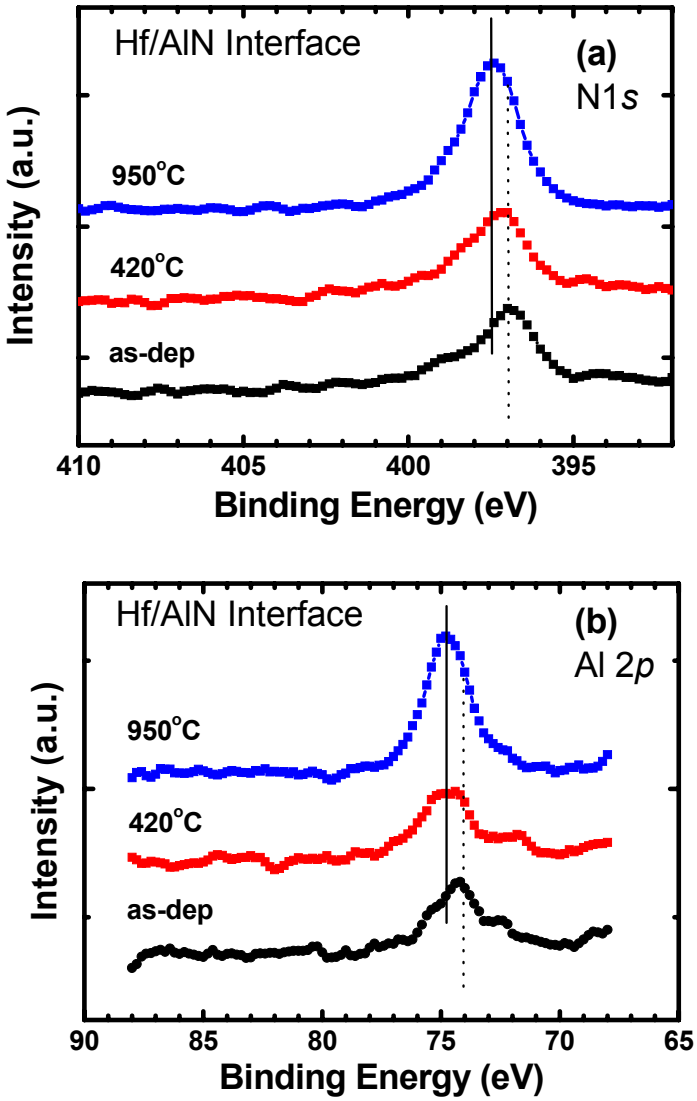

Fig. 2.7 N 1*s* (a) and Al 2*p* (b) XPS spectra at Hf/AlN interface before and after annealing at 420°C and 950°C. Binding energy shift after annealing indicates the reaction of AlN with Hf.

2.3.4 AlN Consumption

In fact, for dual metal gate applications, this ultra thin AlN must be completely consumed through reaction with metals during annealing, otherwise it would cause final EOT increase. C-V properties of Ta/AlN/SiO_2 before and after forming gas annealing at 420°C are shown in Fig. 2.8. After annealing, the accumulation capacitance is increased and the increment corresponds to 0.3 nm of reduction in EOT, confirming complete consumption of AlN.

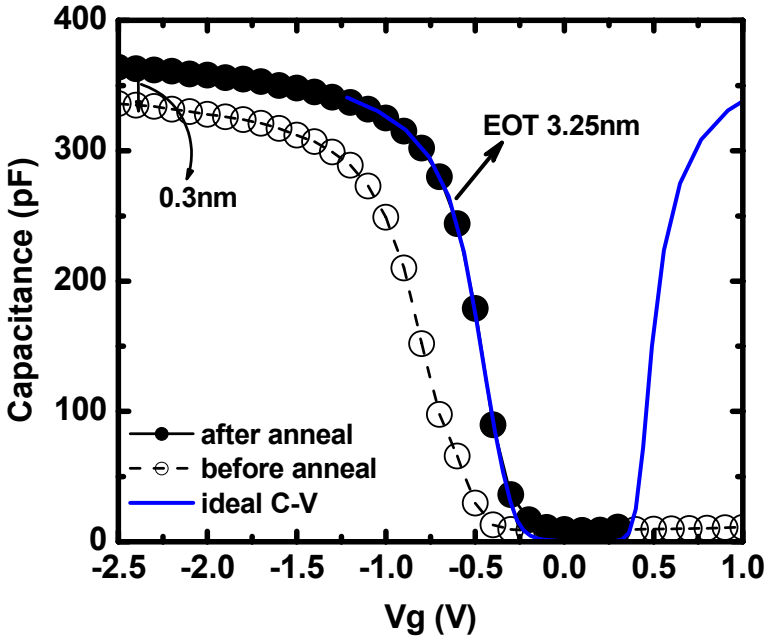

Fig. 2.8 C-V measurement results of Ta/AlN/SiO_2 before and after anneal at 420 ºC in a forming gas ambient.

Figure 2.9 shows similar C-V characteristics of Hf/AlN/SiO_2 before and after forming gas annealing at 420°C. As observed in the C-V curves of Ta/AlN/SiO_2, the accumulation capacitance was increased after annealing, and the increment corresponds to 0.3 nm of decrease in EOT. This amount of EOT reduction corresponds to the physical thickness of AlN, confirming that AlN layer is completely consumed during

annealing and thus makes no contribution to EOT. This is further supported by the perfect match observed between the simulated C-V curve with SiO_2 only thickness and the experimental C-V curve after annealing.

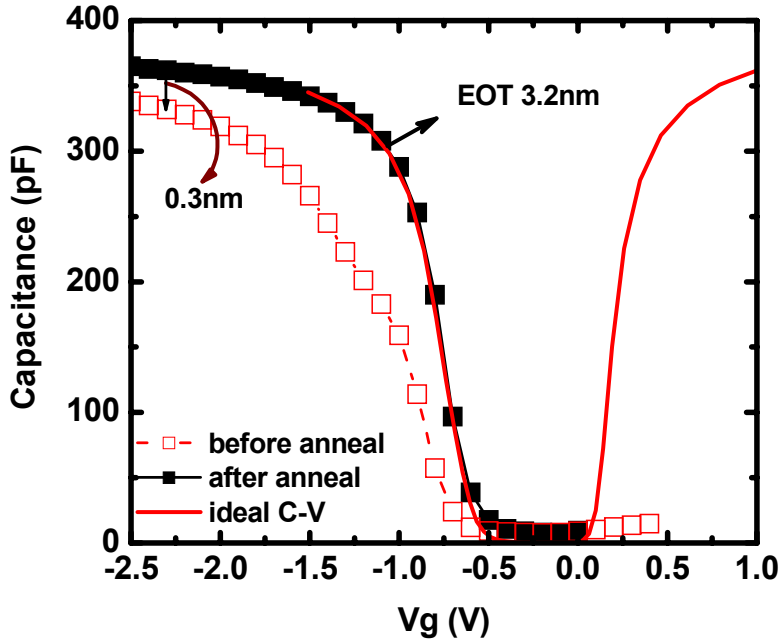

Fig. 2.9 C-V measurement results of Hf/AlN/SiO_2 before and after anneal at 420 ºC in a forming gas ambient.

HRXTEM shown in Fig. 2.10 also confirms the consumption of 0.7-0.8 nm AlN buffer layer by subsequent annealing.

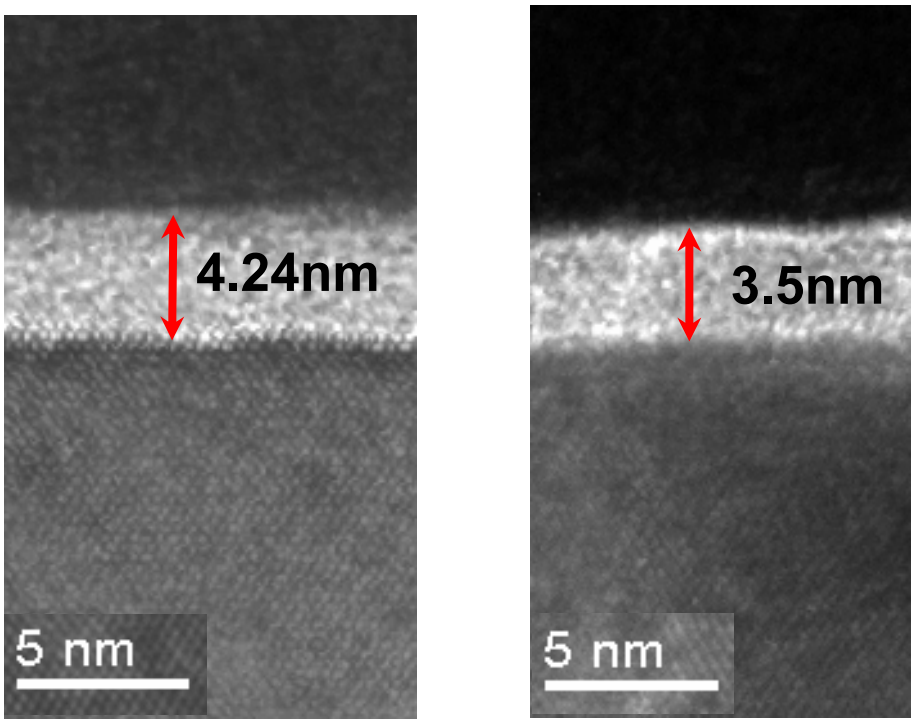

Fig. 2.10 HRXTEM images confirm the consumption of AlN buffer layer by subsequent annealing at 420°C. The initial thickness of SiO_2 is 3.5nm.

Figure 2.11 shows EOT variation depending on thickness of AlN as well as subsequent annealing temperature, providing an allowed thickness of AlN as a buffer layer. It indicates that once the thin AlN is completely consumed, there is no further change in EOT during the subsequent annealing. It is also expected that there will be a process window for AlN thickness. If it is too thin, it may not be effective for protection, whereas if is too thick, it will not be completely consumed during the annealing.

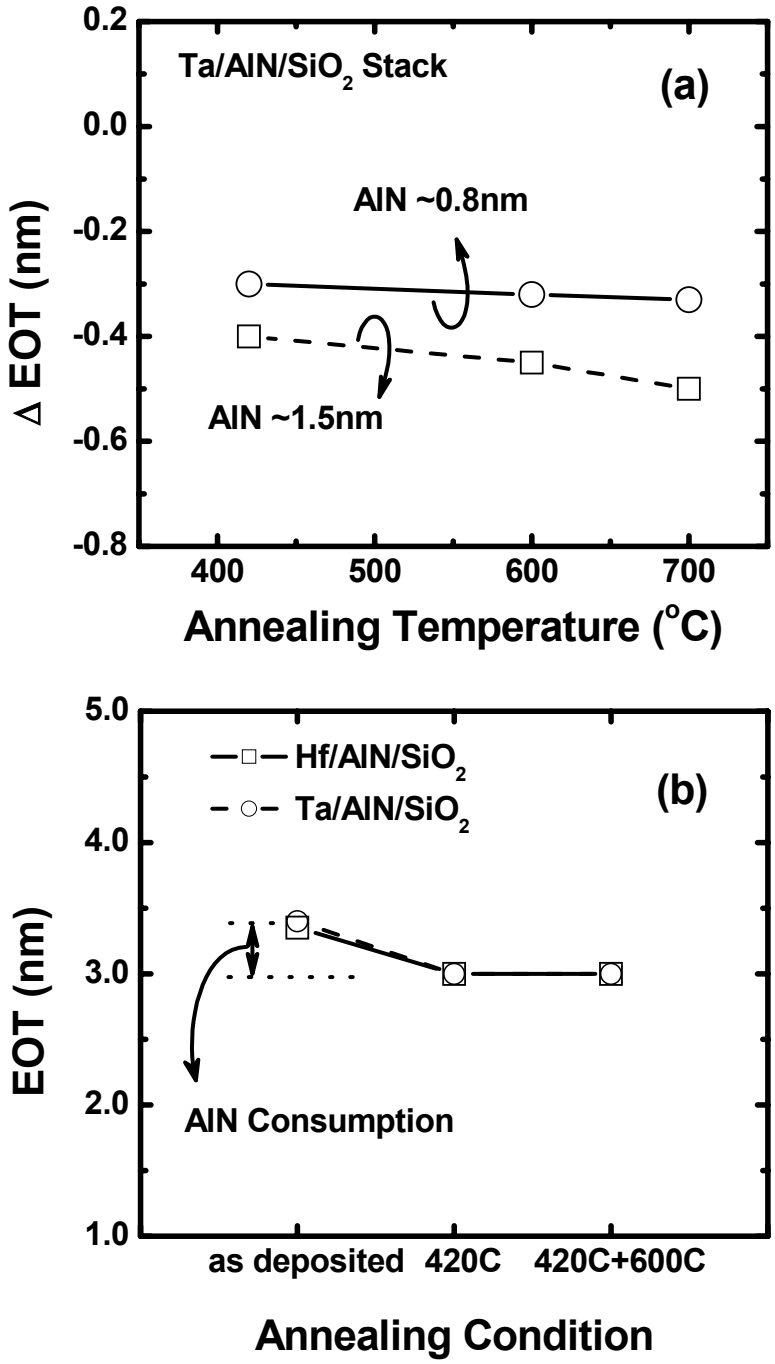

Fig. 2.11 (a) EOT variation with various temperatures for two different thicknesses of AlN buffer layers. ∇EOT in y-axis denotes the EOT difference between before and after annealing. (b) EOT variation of Ta- and Hf-AlN/SiO_2 capacitors with annealing condition. For both capacitors there is no change in EOT after AlN consumption.

2.3.5 Work Function

It was discussed that this ultra thin AlN should be completely consumed when reacted with metals deposited initially, causing no increase in final EOT. Moreover, for the integration of dual metal gates, this reaction should result in formation of metal alloys with suitable work functions so that those alloys can be employed for dual metal gates. Firstly, the flat-band voltage shift is observed due to the reaction of metal and AlN. The normalized C-V curves of Ta/SiO_2 and Ta/AlN/SiO_2 capacitors in Fig. 2.12 (a) and (b) show a significant difference in flat-band voltage (V_{fb}) before and after annealing at 420^{o}C. The flat-band voltage (V_{fb}) of Ta gated SiO_2 capacitor is not changed after annealing while that of Ta/AlN/SiO_2 capacitor is shifted significantly. In both C-V curves of Ta- and Hf-AlN/SiO_2 shown previously, it should be noted that the consumption of AlN is accompanied by a large shift in V_{fb}, which implies the formation of thin ternary metal nitride or aluminide alloy at the metal/SiO_2 interface, which are Ta-AlN and Hf-AlN.

Figure 2.13 shows the V_{fb} difference of 0.5 V obtained between Hf-AlN and Ta-AlN alloy gated capacitors. The result indicates that the work function of metal gates can be modified through the consumption of AlN with initial metal gates (Ta and Hf). The work function was determined by the plot of V_{fb} and gate oxide thickness [2.16]. The work function of Ta on SiO_2 gate dielectric was estimated to be about 4.6 eV, which is in a good agreement with the reported result [2.17] whereas that of Ta-AlN on SiO_2 was about 4.9 eV. The work function difference of both metal gates is consistent with the V_{fb} difference observed in the C-V curves. The plots of V_{fb} as a function of gate oxide thickness in Fig. 2.14 (a) show about 0.5eV of work function difference between Ta-AlN and Hf-AlN alloy gates.

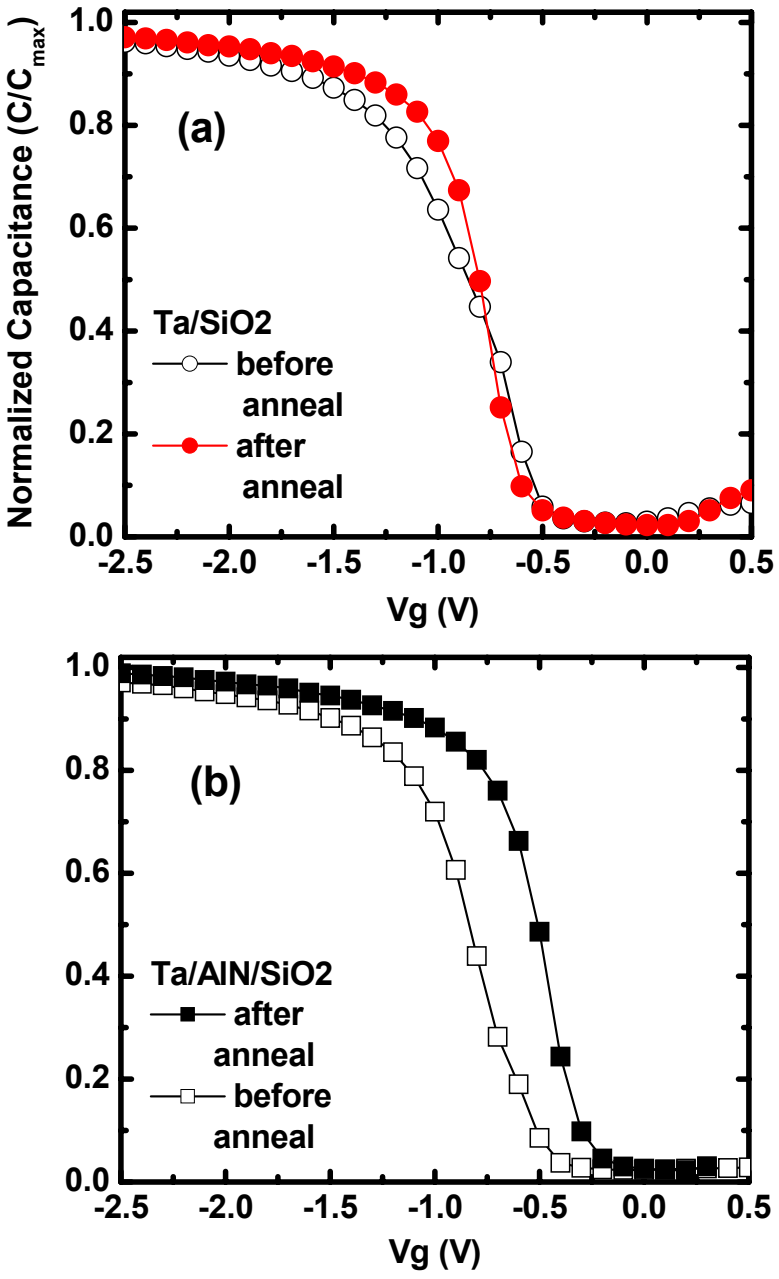

Fig. 2.12 The normalized C-V curves of (a) Ta/SiO_2 capacitor and (b) $Ta/AlN/SiO_2$ capacitor, before and after anneal at 420°C. A significant shift of V_{fb} is observed for $Ta/AlN/SiO_2$ while there is no change in V_{fb} for Ta/SiO_2.

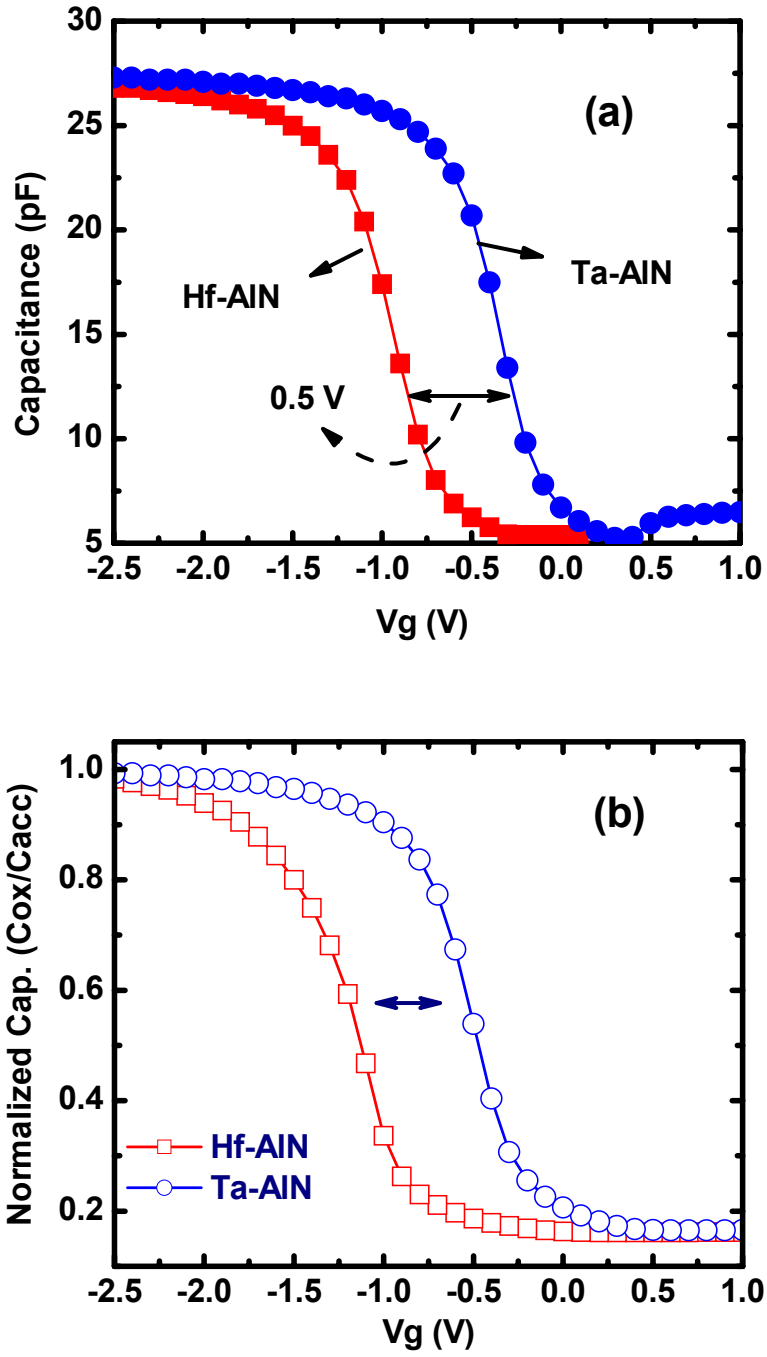

Fig. 2.13 The C-V curves of Hf- and Ta-AlN/SiO_2 after anneal at 420°C (a) and 420°C followed by 600°C (b) show 0.5V of V_{fb} difference. (T_{ox} = 48nm, area = $4x10^{-4}Cm^2$).

Additionally, it shows the work function change with the different $N_2/(Ar+N_2)$ flow rate ratios. For the AlN film sputtered at 25% of gas flow rate ratio, the work functions of both alloys are determined to be about 4.9 eV and 4.4 eV, respectively. The work functions of the new alloys, Ta-AlN and Hf-AlN, are slightly dependent upon the ratio of Al to N, indicating a possibility of modifying work function using N concentration.

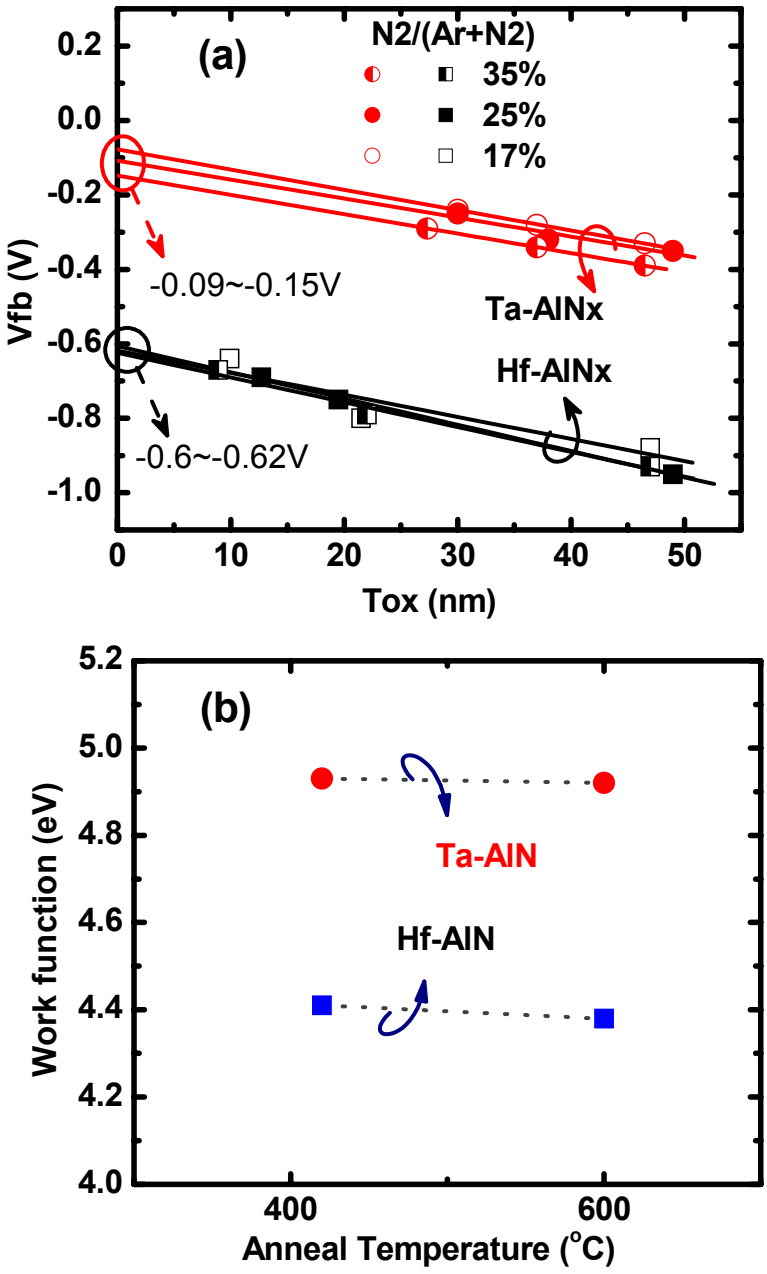

Fig. 2.14(a) V_{fb} plotted against gate oxide thickness for the extraction of work function of Ta-AlN and Hf-AlN gates on p-type substrate. (b) The work function of Ta-AlN and Hf-AlN gates after annealing at 420°C and 600°C.

In Fig. 2.14 (b), the work functions of those alloys are obtained not much differently after annealing at 400°C and 600°C, indicating both alloys are stable to 600°C.

2.3.6 I-V Characteristics

The gate leakage characteristics of both metal alloy gates with thin SiO_2 were also investigated as shown in Fig. 2.15. The leakage current characteristics were slightly degraded after subsequent annealing was done at 600°C.

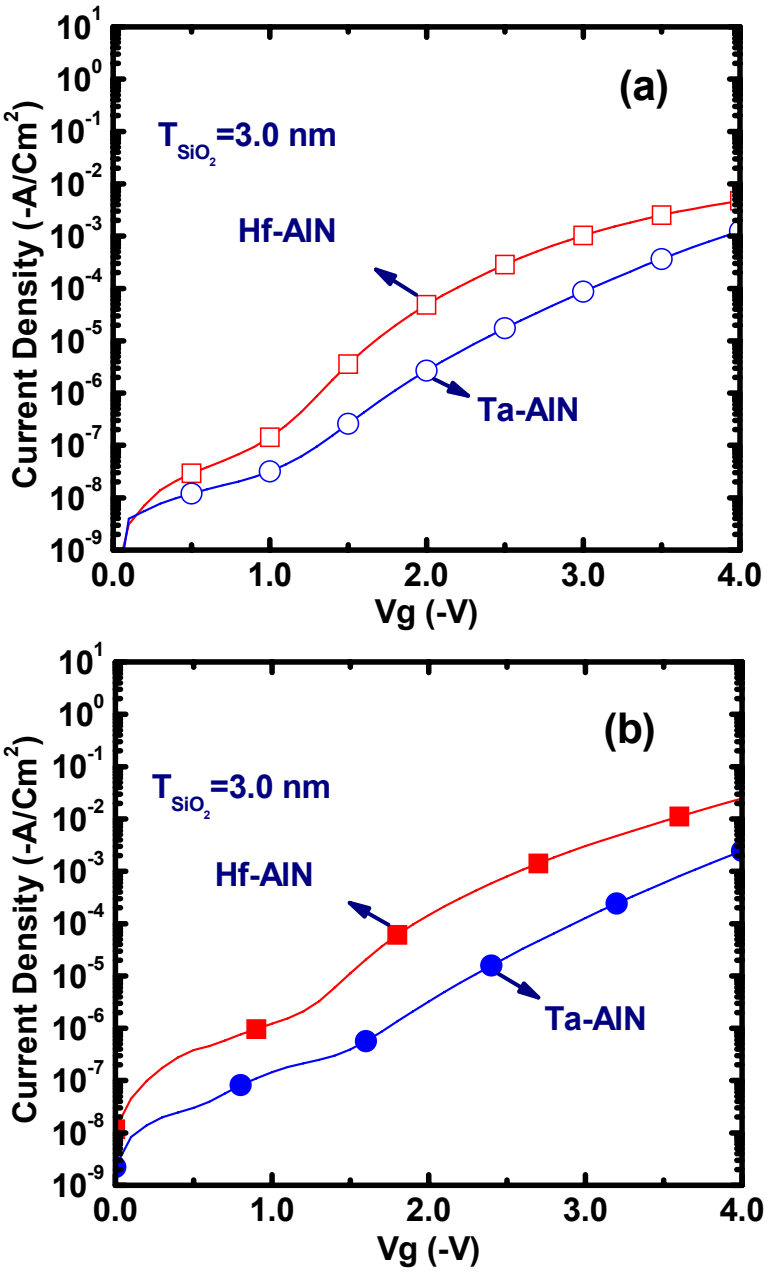

Fig. 2.15 The J-V characteristics of Hf-AlN and Ta-AlN gates on p-sub after anneal at 420 °C (a) and anneal at 420°C and 600°C.

However, the consistent difference in leakage current for both gate electrodes is attributed to the work function difference between both electrodes.

The work function extracted from the plot of V_{fb} and oxide thickness was also confirmed by the barrier height determined from Fowler-Nordheim tunneling equation. Provided with an electron effective mass of $m^* = 0.5m$ for the oxide [2.18], the amount of work function difference is similar to that of the barrier height difference shown in Fig. 2.16 (a). It shows that the gate leakage current for Hf-AlN gate with 4.4 eV of work function is consistent with the J-V characteristics of $TaSi_xN_y$ metal gate with about 4.3 eV as shown in the published results [2.2]. The higher leakage current of Hf-AlN device compared to Ta-AlN is attributed to its lower barrier height due to its lower work function. The work function of Hf-AlN is determined to be about 4.4 eV, which is suitable for nMOS gate metal for thin body SOI or FinFET application [2.19-2.20].

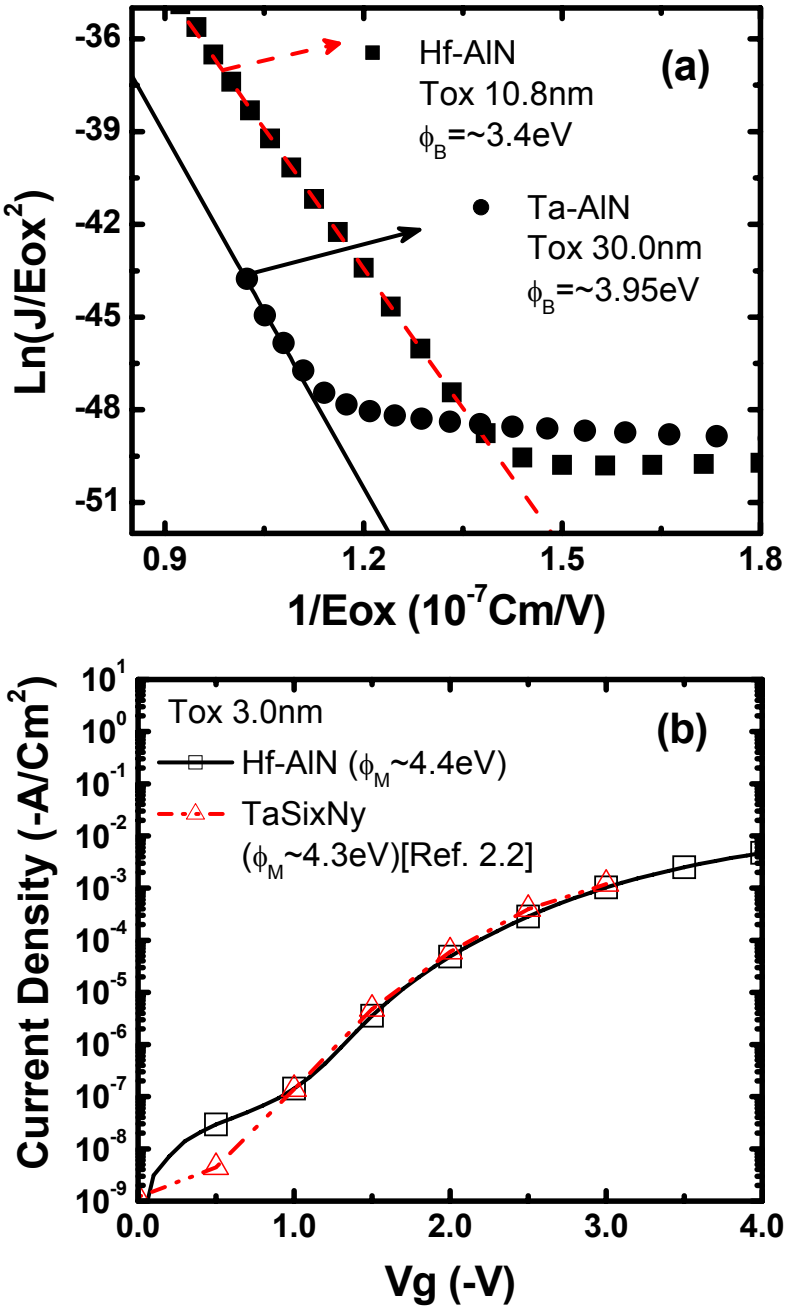

Fig. 2.16 (a) Extracted barrier height (Φ_B) of both gates with SiO_2. (b) The J-V characteristics of Hf-AlN and Ta-AlN gates on p-sub after anneal at 420 °C. The J-V characteristic of $TaSi_xN_y$ gate with about 4.3eV workfunction is shown, which shows similar characteristics with that of Hf-AlN gate with about 4.4eV work function.

2.4 Summary

In this chapter, a novel approach for dual metal gate CMOS process integration through the use of a very thin aluminum nitride (AlN) buffer layer was described. This buffer layer prevented the gate oxide from being exposed to a metal etching process and was completely consumed upon annealing through the reaction with metal gate. The work function of the original gate metal was modified as a result of its reaction with AlN. This approach can offer attractive engineering method for adjusting the work function for dual metal gate process. However, it is applicable as a gate last process because it did not show a sufficient thermal stability for a conventional CMOS fabrication.

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Chapter 3

Fully Silicided Hf-silicide Metal Gates

In this chapter, fully silicided (FUSI) Ni-silicide and Hf-silicide metal gates on SiO_2 are presented. Fully silicided Hf-silicide gate electrode using n^+ polysilicon shows a work function of 4.23 eV, which is very close to that of n^+ polysilicon. No polysilicon depletion effect and excellent thermal stability with negligible change in equivalent oxide thickness (EOT) and flat-band voltage even after high temperature annealing at 950^{o}C are demonstrated. These results indicate that FUSI Hf-silicide is a promising candidate both for nMOSFET metal gate electrode and for dual metal CMOS process. A wide range (4.23 ~ 4.87 eV) of work function with doping of polysilicon is observed.

3.1 Introduction

Many refractory metals as well as refractory metal nitrides have been investigated as candidates for metal gate electrode material [3.1 - 3.3]. However, most of thermally stable metals available for CMOS processing have work functions near midgap or the valance band of silicon. Since the metals with low work functions are inherently unstable and reactive, searching a suitable metal for n-MOSFET gate electrode with thermal stability compatible with CMOS front-end process is a challenge.

Si-based gate materials are desirable because dopant implantation conditions can control the threshold voltage V_{th} for both nMOS and pMOS, and the process integration schemes are well established in actual fabrication process. Refractory metal silicides such as WSi_2, $MoSi_2$, and $TaSi_2$ have been studied for this purpose since silicide and self-aligned silicidation process (SALICIDE) were widely used to reduce the source, drain, and gate resistance of sub-micrometer MOS devices [3.4]. Recently, fully silicided metal silicides such as NiSi and $CoSi_2$ for dual metal gates have drawn considerable attention due to their CMOS compatibility and no process-induced damage to the gate dielectric [3.5 - 3.9]. However, no silicide material suitable for nMOSFET has been reported. In this study, we demonstrate for the first time that Hf-silicide can be used as a gate electrode material for nMOSFETs with a work function of 4.2 eV and excellent thermal stability up to 950^{o}C. This study is based on the fact that the work function of metal-silicide is close to that of the initial metal for silicidation [3.2, 3.6] and the work function of hafnium is as low as around 4.0 eV [3.10]. The basic material studies on Hf-silicide have been reported [3.11 - 3.14] and in our study they are applied for nMOS metal gate electrode in CMOS applications.

3.2 Experimental

The MOS capacitors with SiO_2 gate dielectric were fabricated on p-type (100) Si substrates. *In-situ* phosphorous doped polysilicon films with a thickness range of 40 – 200 nm were deposited in a LPCVD furnace and annealed at 900^{o}C. Hafnium (Hf) metal films with thicknesses ranging from 80nm – 200nm were deposited on polysilicon by sputtering at 450 Watt of power under a base pressure of 10^{-7} torr, immediately after the removal of native oxides from the surface of polysilicon. About 40nm thick Tungsten (W) capping layer was subsequently deposited on top of hafnium layer. The tungsten capping layer is to prevent hafnium from being oxidized during its silicidation and will be removed together with unreacted hafnium after silicidation. As seen in Fig. 4.2.1, the tungsten capping layer does not react with hafnium even at 750°C. Silicidation was done by furnace annealing at 420°C or rapid thermal annealing (RTA) at different temperatures ranging from 600 to 750°C for 1 min. Sputtered tungsten can easily be removed in H_2O_2 solution [3.15], and oxidized tungsten layer can be etched away by hydroxide solution such as tetra-methyl ammonium hydroxide (TMAH) and NH_4OH solutions [3.16]. Sputtered hafnium film is removed using the mixture of H_2SO_4 and H_2O_2 (SPM). After silicidation, tungsten and unreacted hafnium films were removed by H_2O_2 and SC1 solution, followed by SPM. For the evaluation of thermal stability of the Hf-silicide, the samples were annealed in a RTA chamber at 750 to 950°C for 30 sec. Finally, all the samples were annealed in a forming gas ambient at 420°C for 30 min.

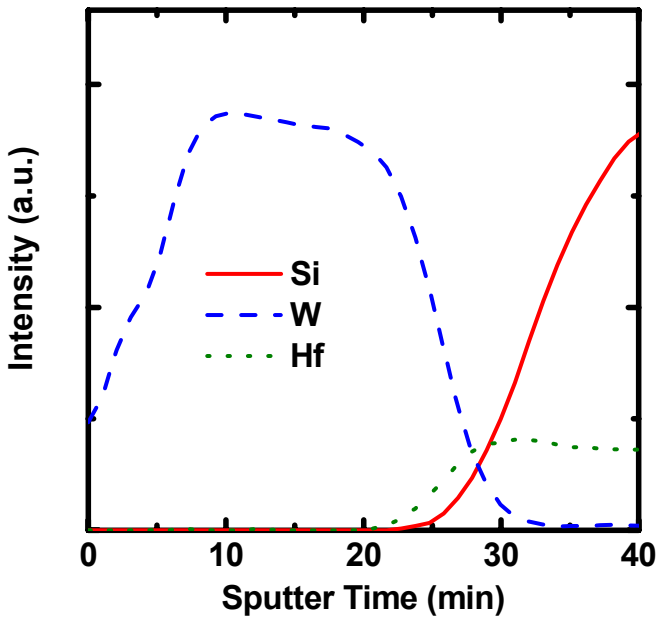

Fig. 3.1 AES depth profile of tungsten capped Hf-silicide formed through RTA at 650 ^{o}C. Negligible interdiffusion between W and Hf is observed after RTA at 650^{o}C.

3.3 Results and Discussion

Figure 3.2 (a) shows the amount of silicon consumption by silicidation at different temperatures, which was determined by etching Hf-silicide films in buffered hydrofluoric acid and measuring the thickness of the remaining polysilicon. Figure 3.2 (b) shows the sheet resistance values after silicidation at different temperatures. The decrease of sheet resistance with the increase of silicidation temperature indicates the increase of Hf-silicide layer, which is consistent with the results in Fig. 3.2 (a) and the report in [3.14]. In this experiment, there was no significant difference in the amount of silicon consumption between undoped and phosphorous doped polysilicon. Figure 3.3 (a) shows XPS depth profile of Hf-silicide formed through RTA at 600°C for 1 min. Before RTA, the thickness of Hf and undoped polysilicon was around 200 nm and 100 nm, respectively. About 55 nm of polysilicon film was silicided at this temperature, which is consistent with the result in Fig. 3.2 (a). The composition of Hf-silicide formed through RTA at 600°C is analyzed using RBS. As seen in Fig. 3.3 (b), the composition ratio of Hf to Si is estimated to be 0.9, which is close to HfSi. Based on these results, 40 nm thick polysilicon, 80 nm thick hafnium, and RTA at 600°C for 1 min were chosen so that polysilicon can be fully silicided for MOS capacitor fabrication and electrical performance evaluation.

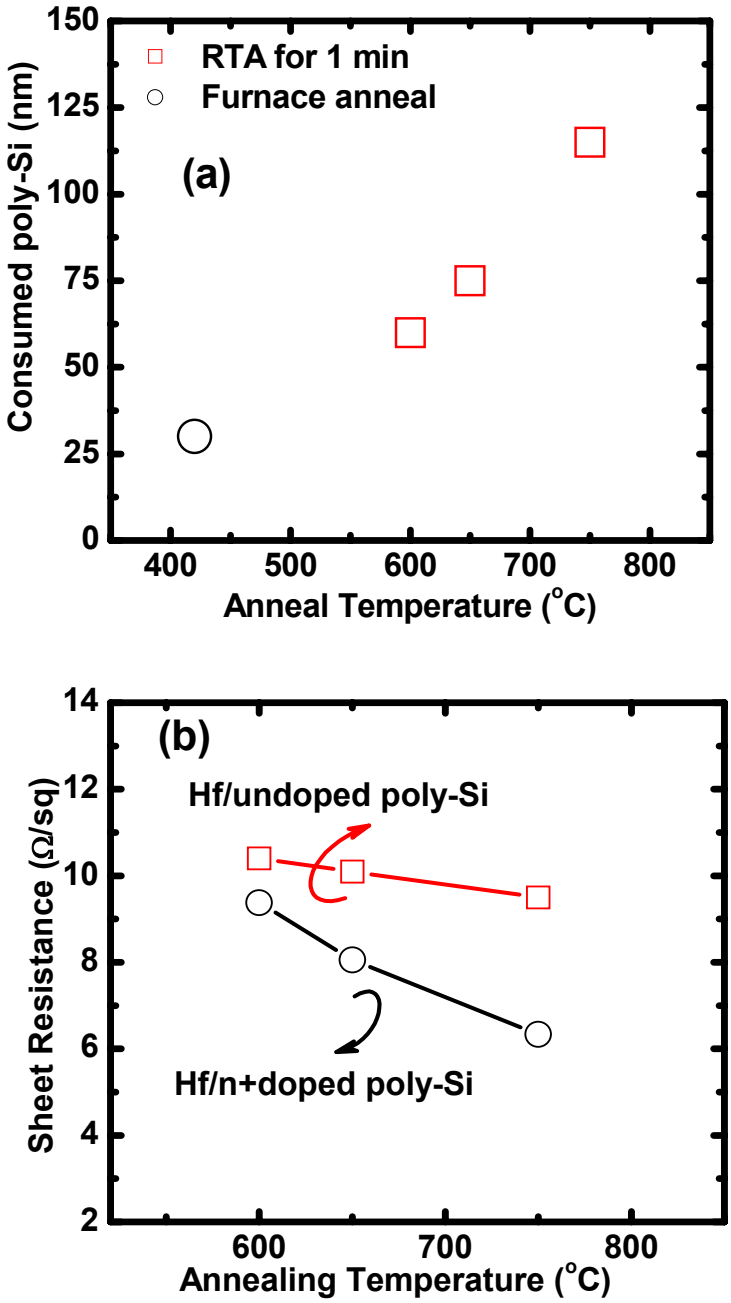

Fig. 3.2 (a) The consumption of polysilicon by silicidation at different annealing temperature. (b) Sheet resistance of Hf/polysilicon stack layers after annealing at different temperatures. Sheet resistance was measured before unreacted metal strip. The initial polysilicon thickness is 200 nm. RTA was done at the temperature range of 600°C - 750°C for 1 min. For 420°C, the annealing was done in a furnace tube for 1 hour.

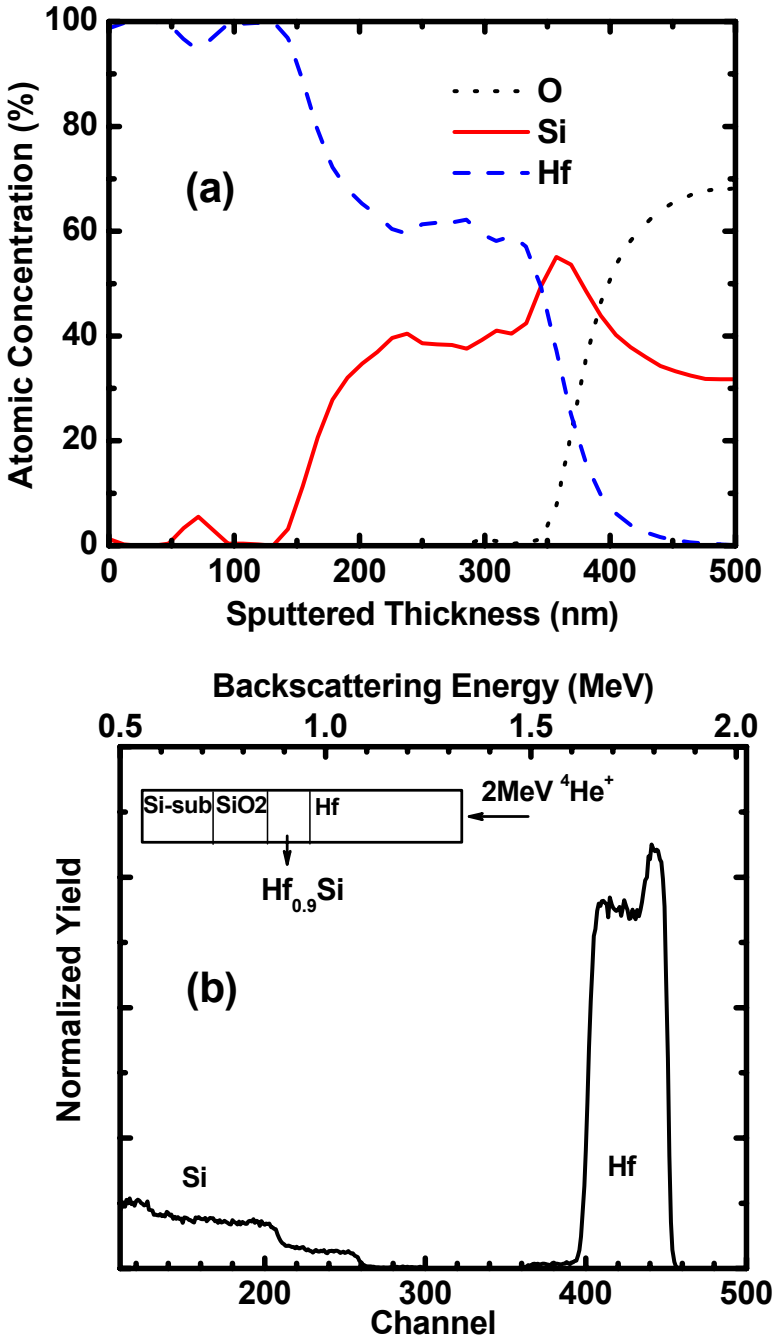

Fig. 3.3 (a) XPS depth profile of Hf-silicide formed on undoped polysilicon after RTA at 600 °C for 1 min. The initial thickness of Hf and polysilicon is 200 nm and 100 nm, respectively. About 55 nm of polysilicon was consumed for silicidation. Sputtering rate was 11.9 nm/min. (b) RBS spectrum of Hf silicide formed through RTA at 600°C. Mostly the composition is estimated to be 0.9, which is very close to HfSi.

Fully silicided Hf-silicide is confirmed with the quasi-static C-V curve of MOS capacitor fabricated using Hf-silicide gate formed by RTA at 600°C for 1min. As can be seen in Fig. 3.4, it fits very well with the theoretical C-V curve, with complete elimination of polysilicon depletion. Equivalent oxide thickness (EOT) of 76 Å is also well matched with the original thickness of SiO_2, indicating that SiO_2 dielectric is intact. Full silicidation with no remaining polysilicon on top of SiO_2 was confirmed again with a depth profile of Hf-silicide layer analyzed by Auger Electron Spectroscopy as seen in Fig. 3.5.

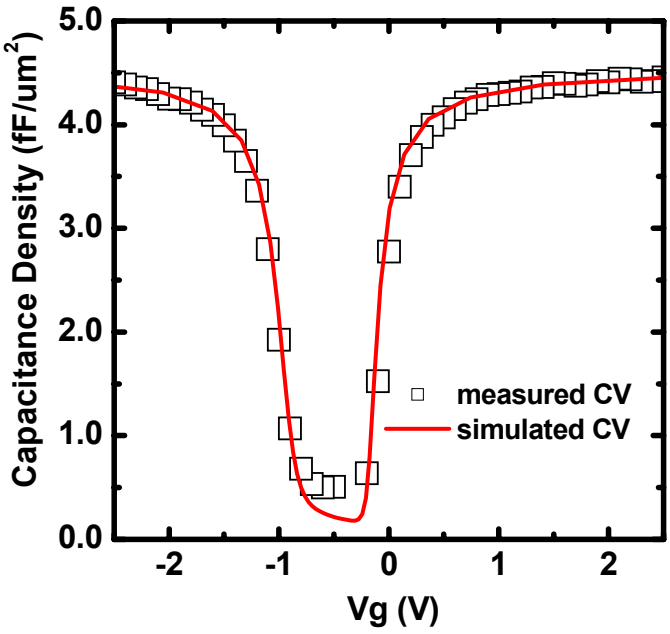

Fig. 3.4 The quasi-static C-V curve of Hf-silicide gated MOS capacitors. The Hf-silicide was formed by RTA at 600°C for 1 min. The sample went through another annealing at 750°C for 30 sec after removal of unreacted. The thickness of SiO_2 gate dielectric is 7.6nm and the area of MOS capacitors is 1.0×10^{-4} cm^2.

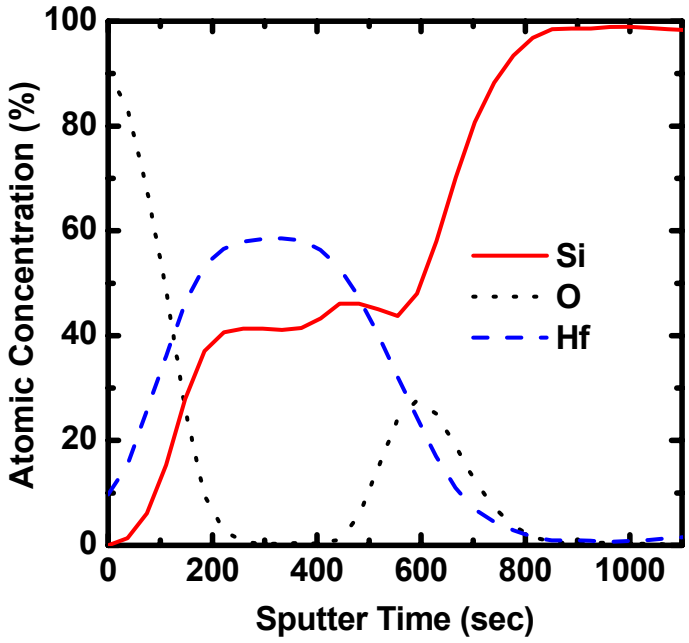

Fig. 3.5 AES depth profile of fully silicided Hf-silicide through RTA at 600°C for 1min. Hf (80 nm)/phosphorous doped polysilicon (40nm) film stack was used for silicidation. After RTA, both capping and unreacted metals were removed away using wet chemical solutions.

Figure 3.6 shows the C-V curve of HfSi gated SiO_2 MOS capacitor. It fits well with the QM-simulated C-V curve suggesting that there are little interface traps. The EOT determined by the theoretical C-V curve which took into account the quantum mechanical effect [3.20] is 3.55 nm, which is consistent with the physical thickness obtained from HRTEM image as seen in Fig. 3.7.

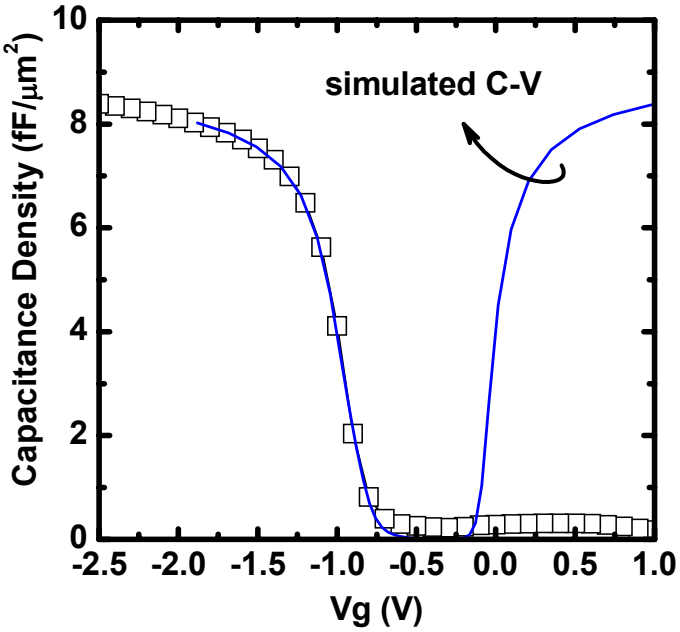

Fig. 3.6 C-V curves of Hf-silicide gated MOS capacitor with thin SiO_2. The initial thickness of gate oxide is 3.55 nm and the area of capacitors is 1.0×10^{-4} cm^2.

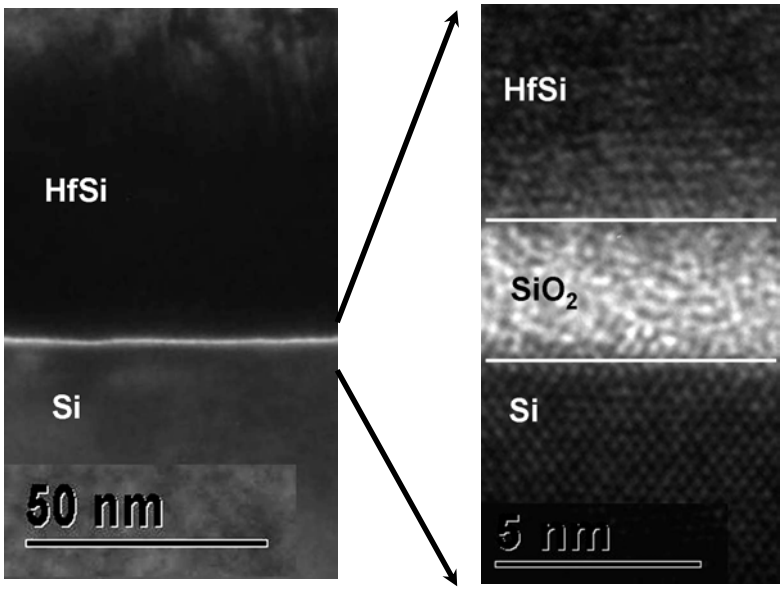

Fig. 3.7 HRXTEM of $HfSi/SiO_2$ gate stack and its focused image.

Flat band voltages versus gate oxide thickness for FUSI Hf-silicide gates with various dopings in the initial polysilicon are shown in Fig. 3.8. The intercepts at y-axis indicate workfunction difference (Φ_{ms}) between the gate materials and silicon substrate. The work function of FUSI HfSi of n^+-polysilicon (n-HfSi) is estimated to be about 4.23 eV, which is very close to that of n^+- polysilicon. When p^+-polysilicon is used, the work function of FUSI HfSi of p^+-polysilicon (p-HfSi) is about 4.87 eV. Dopant dependence of work function in FUSI gate is found in other silicide gate as well, like FUSI Ni-silicide, and it is attributed to dopant impurity segregation to the interface of gate oxide [3.17]. As seen in Fig. 3. 9, the work function difference between n-HfSi and p-HfSi is 0.64 eV, which is larger than 0.5 eV observed in FUSI NiSi gates [3.18-3.19]. The lowest work function of FUSI n-NiSi is about 4.6 eV, which is still not low enough for nMOSFET. The wider range of work function modulation and very low minimum work function value in FUSI HfSi make the process more attractive for gate electrode application.

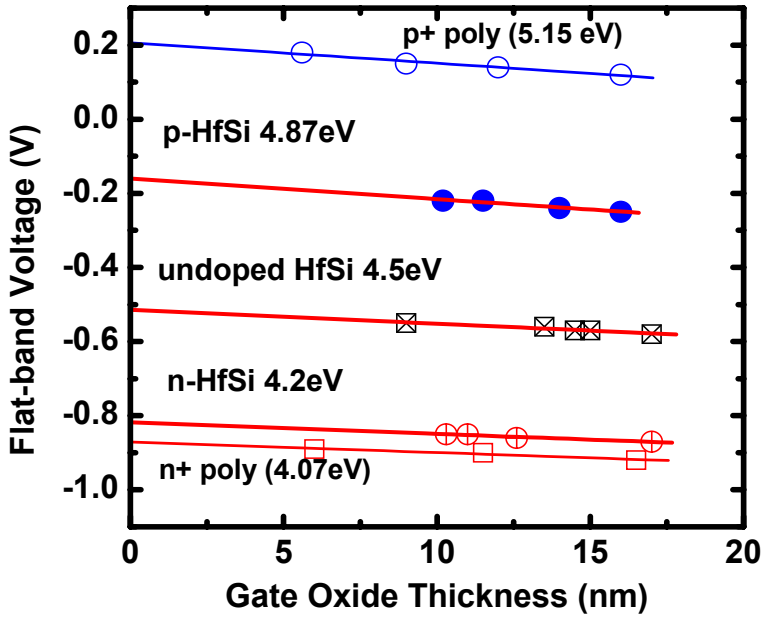

Fig. 3.8 Flat-band voltage vs. gate oxide thickness. Work function difference of about 0.64 eV is obtained between Hf-silicided n^+ polysilicon and Hf-silicided p^+ polysilicon.

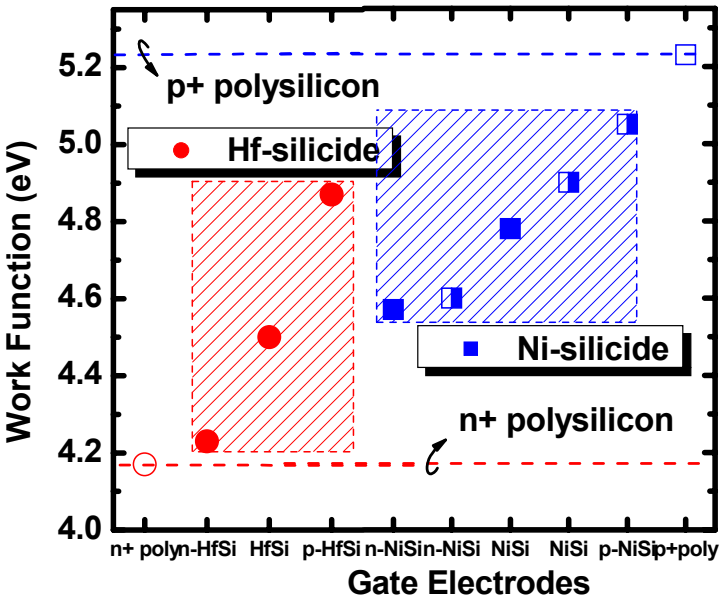

Fig. 3.9 Tunable range of work function in Hf-silicide and Ni-silicide by controlling dopants in polysilicon. The work function of n-HfSi is nearer to that n^+, while the work function of Ni-silicide is nearer to that of p^+ polysilicon, respectively. ●,■ : this work, ◨: taken from Ref. [3.6].

The thermal stability of Hf-silicide gate is further investigated by RTA up to 950°C which is the temperature required for source/drain implantation annealing. In this case, 40 nm thick TaN capping layer is used on top of Hf-silicide to suppress oxidation of Hf-silicide and reduce gate resistance. The previous capping layer, W, was chosen because of ease of etching by wet chemical, as the unreacted Hf must be removed after silicidation. However, it is observed that tungsten is oxidized even during forming gas annealing in a furnace tube. For such reasons, TaN is chosen here as a capping layer for the final structure of the silicided gate. Since the oxidation of silicide films and grain boundary grooving during subsequent annealing can degrade the sheet resistance, the use of nitrided metal capping layer on top of silicide can overcome such problems [3.15].

In this experiment, the TaN film successfully played a role of capping layer, showing no degradation of sheet resistance even after a high temperature annealing at

950°C. After annealing at 950°C, the sheet resistance of 40nm thick TaN capped Hf-silicide stack gate was measured to be about 20 ohms/square. Further reduction of sheet resistance can be achieved by increasing the TaN thickness. Consistent C-V curves of TaN capped Hf-silicide gate capacitors with 3.5 nm thick SiO_2 were observed before and after annealing at various temperatures. Figure 3.10 shows negligible change in accumulation capacitance, indicating no noticeable difference in EOT and negligible amount of shift in flat-band voltage (V_{fb}) even after annealing at 950ºC. Gate oxide leakage current also showed no significant difference between before and after annealing at 950ºC as shown in Fig. 3.12. The results demonstrate the excellent thermal stability of TaN capped fully Hf-silicided gate, demonstrating its potential use as the gate electrode material for n-MOSFETs.

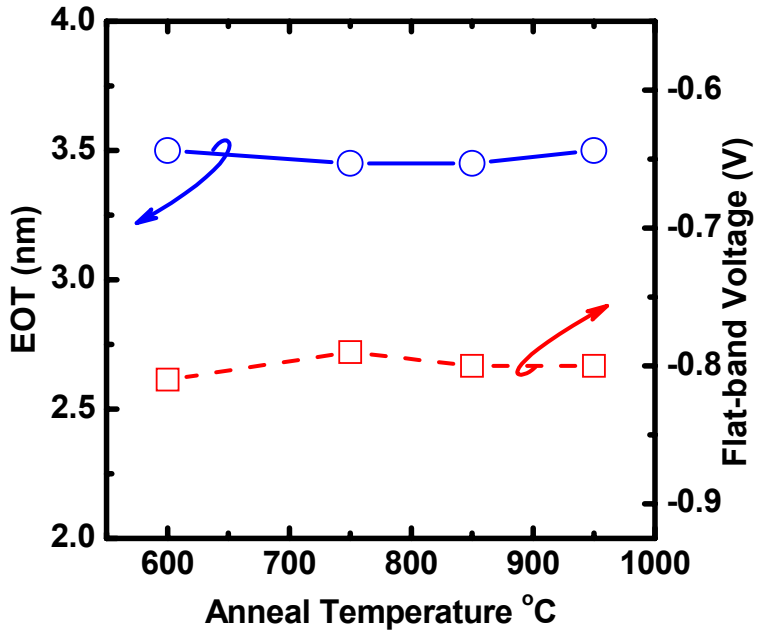

Fig. 3.10 Variation of equivalent oxide thickness and flat-band voltage of FUSI HfSi gate MOS capacitors before and after annealing at different temperatures. The TaN capping layer was used on top of HfSi. Excellent thermal stability up to 950 °C is observed.

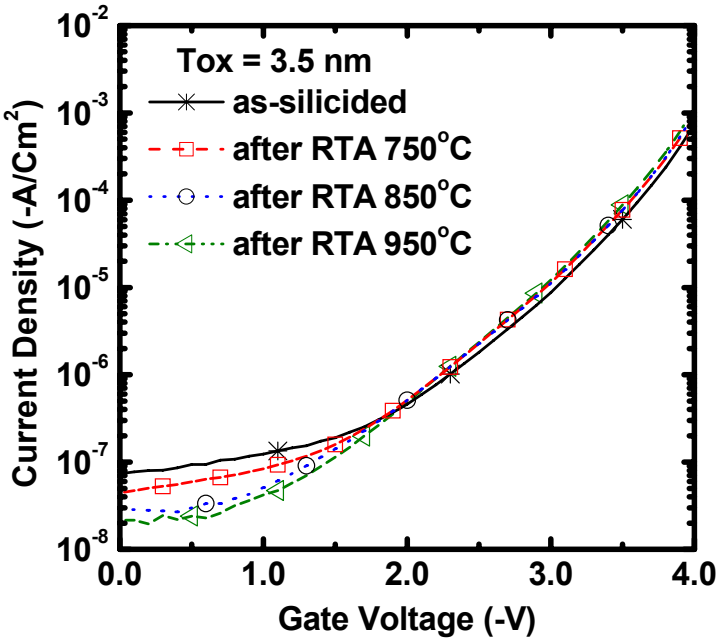

Fig. 3.11 I-V characteristics of TaN/HfSi/SiO_2 MOS capacitors with annealing temperature. Hf-silicide was formed through RTA at 600°C for 1 min. TaN was capped right after unreacted Hf was removed away. The thickness of gate oxide was 3.5 nm.

nMOSFET with FUSI n-HfSi gate electrode is successfully demonstrated. Figure 3.12 shows the high frequency C-V curve and I_d-V_d characteristics of FUSI n-HfSi gate nMOSFET. In C-V curve measurement, source and drain were grounded. The measured C-V curve is compared to the theoretical C-V curve which took into account the quantum mechanical effect [3.20]. Fig. 3.13 shows demonstrates no polysilicon depletion effect under inversion and well behaved transistor with FUSI n-HfSi gate.

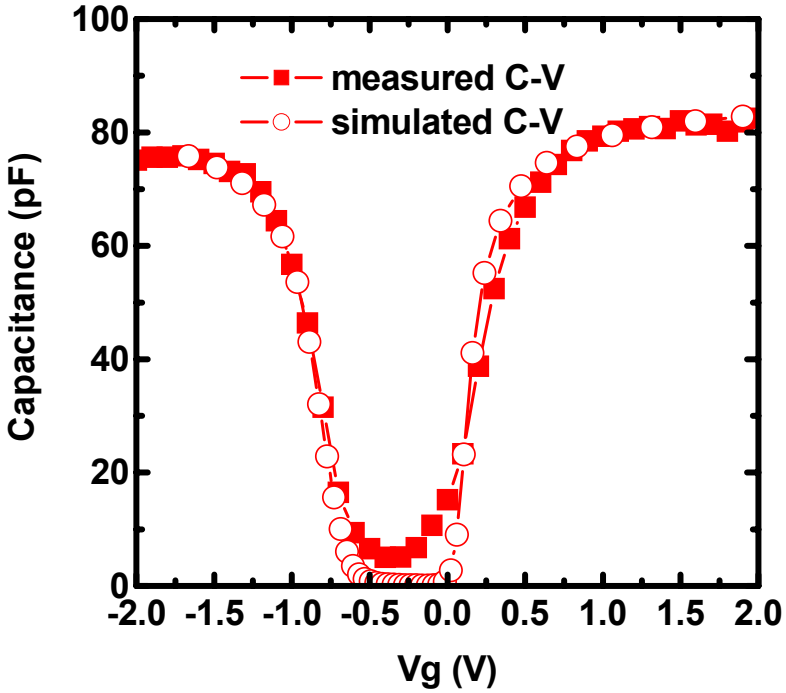

Fig. 3.12 High frequency C-V curve of FUSI HfSi gate nMOSFET with 3.2 nm thick gate oxide. Source/drain was grounded during measurement. No polysilicon depletion is observed.

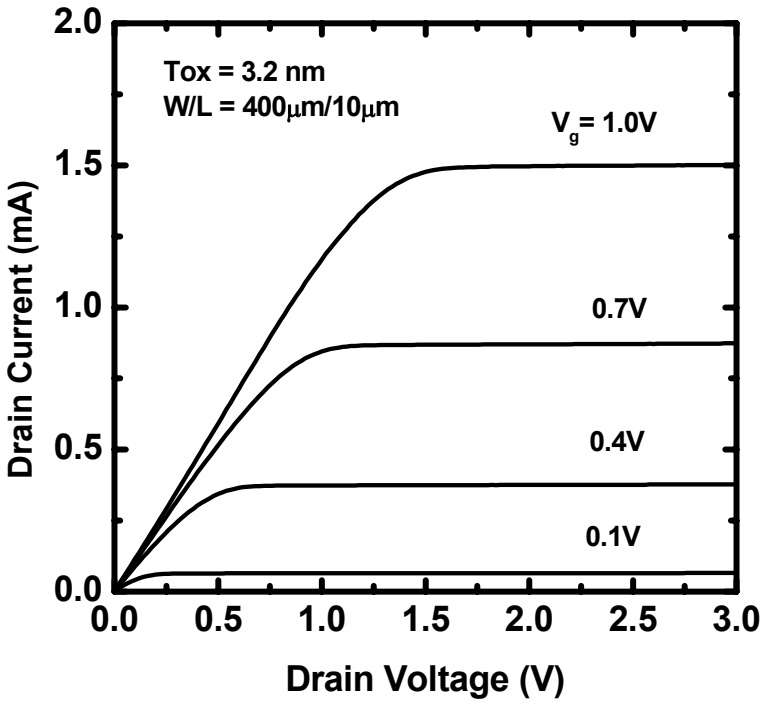

Fig. 3.13 I_d-V_d characteristics of nMOSFET with FUSI n-HfSi gate. Neither p-well implantation nor V_{th} adjustment implantation was done.

3.4 Summary

Fully silicided (FUSI) HfSi as a metal gate material for nMOSFETs (work function ~4.2 eV) was demonstrated, which is compatible with CMOS processing. Full silicidation and no polysilicon depletion were observed from the quasi-static frequency C-V curve of Hf-silicide gate capacitor. Negligible change in flat-band voltage and EOT were observed even after annealed at 950°C, demonstrating its excellent thermal stability. Wide range (4.23 ~ 4.87 eV) of work function with doping is observed.

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Chapter 4

Substituted Al Metal Gate for Low Work Function and Fermi Level Pinning Free

In this chapter, substituted aluminum (SA) gate MOS characteristics are discussed. SA gates were successfully demonstrated on various gate dielectrics such as SiO_2, re-oxidized Si_3N_4, Al_2O_3, and HfAlON high-K dielectric. Full substitution of polysilicon with Al was achieved for a Ti/Al/polysilicon/HfAlON gate structure by a low temperature annealing at 450°C. The SA gate on HfAlON dielectric shows a very low work function of 4.25 eV, which is well suitable for bulk nMOSFETs. The SA process was free from Fermi level pinning problem. In addition, the SA process also shows improved uniformity in leakage current distribution compared to fully silicided (FUSI) metal gate.

4.1 Introduction

Metal gate is imperative in nano-scale CMOS devices, especially with high-K gate dielectrics because of the interface instability between polysilicon and high-K materials. For bulk CMOS devices, the dual metal gate scheme requires work functions of gate metals to be within 0.2 eV of the E_C and E_V of Si for n- and p-MOSFET, respectively [4.1]. However, the achievement of such work functions on high-K dielectric is still a challenge because of Fermi level pinning and thermal instability of the interface as well as the metal film itself, especially for the metals with low work function [4.2-4.5]. Although a wide work function difference between n- and p-type of metals can be achieved, the integration of dual metal gates is still a big challenge.

Although FUSI (Fully silicided) metal gate has advantages of better thermal stability, capability of work function tuning by pre-doping of polysilicon, and less Fermi level pinning effect, it is not still easy to achieve proper work functions for both n and pMOSFET using pre-doping of polysilicon on high-K dielectrics because FUSI gate process is not completely free from Fermi level pinning problem. The Si-Hf reaction at the interface between polysilicon and Hf-based dielectric may still complicate the work function adjustment in FUSI gate [4.6].

Reaction of Al with polysilicon can be also used as a replacing polysilicon gate. Substituted Aluminum (SA) gate, which can be obtained through the reaction of Al with polysilicon can be used as an alternative metal gate. Like FUSI process, for this SA process, no damage to gate dielectric and no thermal instability related issue would be expected as it can be implemented after all the high temperature processes were done with polysilicon gate. Additionally, Si can be removed from the interface of gate and high-K dielectric, leading to Fermi level pinning free.

For both polysilicon gate and FUSI gate, their work function tuning is not easy due to Fermi level pinning effect. Since the cause of Fermi level pinning could be mostly due to Si bonding at the interface of gate and dielectric, substituted metal gate may offer a practical solution of work function tuning as Si bonding can be removed from the interface.

4.2 Background of Al substitution

The reaction of silicon with aluminum is not new. In this section, historical backgrounds of Al substitution process are reviewed and related mechanism to Al substitution for polysilicon and reported application of Al substitution are discussed.

4.2.1 Reaction of Al with Si

The reaction of Al with silicon results in contact migration. Contact migration refers to the diffusion of the metal atoms of a contact such as Al or an alloy into the silicon substrate. This phenomenon is due to the occurrence of interdiffusion between two different interdiffusible materials in contact with each other, which are Al and Si in this case. This interdiffusion occurs in both ways, i.e., Al diffuses into Si and Si diffuses into Al. Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. This Al spike has shortened the junction, damaging the device. The reverse case, where the Si atoms have entirely penetrated the Al layer above, may also happen and can result in an open circuit as a result of voids in the metal contact. This junction spiking problem has been usually reduced by doping the Al with Si (Al-Si) or Cu (Al-Cu) or both (Al-Si-Cu), forming an alloy that is more resistant to

Al-Si interdiffusion. A barrier metal such as Ti or Ti/TiN has also been used between the Al layer and the silicon substrate to suppress their interdiffusion.

Silicon re-growth has been observed in Al film on Al overlying Silicon due to substitution and it has been reported that the reaction between Al and polysilicon occurs below 577°C [4.7, 4.8]. Once the reaction of Al with silicon starts, it depends on the solubility of Si in Al. The solubility of Si in Al film increases with temperature. Si dissolves in Al and Al moves to fill the void created by Si. It has also been reported that solid phase reaction of polysilicon with Al is mainly dominated by the silicon solubility and the dissolved silicon diffusion in Al. In addition, it has been investigated that the reaction preferably proceeds along the polycrystalline silicon grain boundary. In this case, non-uniform reaction may occur.

4.2.1 Applications using Al substitution

Uniform reaction of Al with polysilicon has been obtained in Ti capped Al/polysilicon stack structure. It has been reported that Ti on top of Al enhanced moving of Si to Al, leading to uniform reaction [4.9]. Substituted Al plugging for polysilicon has been developed [4.9], and as another application of Al substitution, substituted Al gated MOSFET was demonstrated on SiON recently [4.10].

4.3 Experiment

The SA process is a type of gate last process with no etching or removal of gate polysilicon. After fabrication of MOSFETs with polysilicon gate using a conventional CMOS process flow, the interlayer dielectric is polished down until the gate polysilicon is exposed. Then, aluminum is deposited on top of the polysilicon. Titanium capping

layer on top of aluminum is used to enhance the replacement process. During low temperature annealing (as low as 450°C), the polysilicon is replaced with aluminum and a Ti/Ti-silicide/Al/high-K gate structure is formed. Polysilicon can fully be replaced with Al under the presence of Ti on top of Al. Without the Ti capping layer, the replacement takes place only partially and in a very non-uniform manner [4.7, 4.8].

In this experiment, HfAlON dielectric is used as the high-K gate dielectric. HfAlON films were formed using thermal nitridation of MOCVD HfAlO films in a NH_3 ambient at 800°C. XPS analysis showed that the concentration ratio of Hf and Al in the bulk HfAlON was estimated to be 4:1 and about 10 % of N was incorporated. For comparison, thermal SiO_2 and re-oxidized CVD nitride (Si_3N_4) gate dielectrics were also prepared. Reoxidation of nitride was done by RTO at 950°C. For the FUSI NiSi and Al substitution processes, 30-40 nm thick amorphous silicon films were deposited in a LPCVD furnace. Doping of polysilicon was done by either in-situ phosphorus doping or boron implantation, followed by furnace annealing at 900°C for 30 min for dopant activation. For boron implantation, BF_2 ions were implanted with an energy of 10 keV and a dose of 1×10^{15} cm^{-2}. For in-situ phosphorous-doped n^+ polysilicon, the sheet resistance of 40 nm thick polysilicon was about 800 Ω/sq. Approximately 200 nm of Al was sputtered on top of the polysilicon right after DHF cleaning, followed by sputter deposition of Ti with a thickness of 100 nm. In this experiment, Al thickness was chosen to be thicker than polysilicon thickness to ensure the full substitution [4.13]. Both FUSI NiSi and Al substitution were implemented at the same temperature of 450°C for 30 min in a furnace tube.

4.4 Results and Discussion

4.4.1 Substitution of Al for polysilicon

There was a significant effect of Ti capping layer on the substitution of Al for polysilicon. For pure Al/polysilicon stack without Ti capping, the reaction of polysilicon with Al occurred non-uniformly as seen in Fig. 4.1. Fig. 4.1 (a) shows the surface of Al/polysilicon stack on thermal oxide after annealing at 450°C. It appears that island types of polysilicon grains exist in Al layer. When Al layer is removed, polysilicon grains can be observed clearly. Fig. 4.2 (b) shows the surface of annealed Al/polysilicon stack after Al is removed. Al was removed using wet chemical solution, which is SPM (Sulfuric Peroxide Mixture), after annealing at 450°C. SiO_2 layer is exposed while unreacted polysilicons are left as SPM selectively removes Al only. However, for Ti /Al/polysilicon stack, a clean SiO_2 surface was observed after Ti/$TiSi_x$/Al is removed, suggesting uniform reaction of polysilicon with Al.

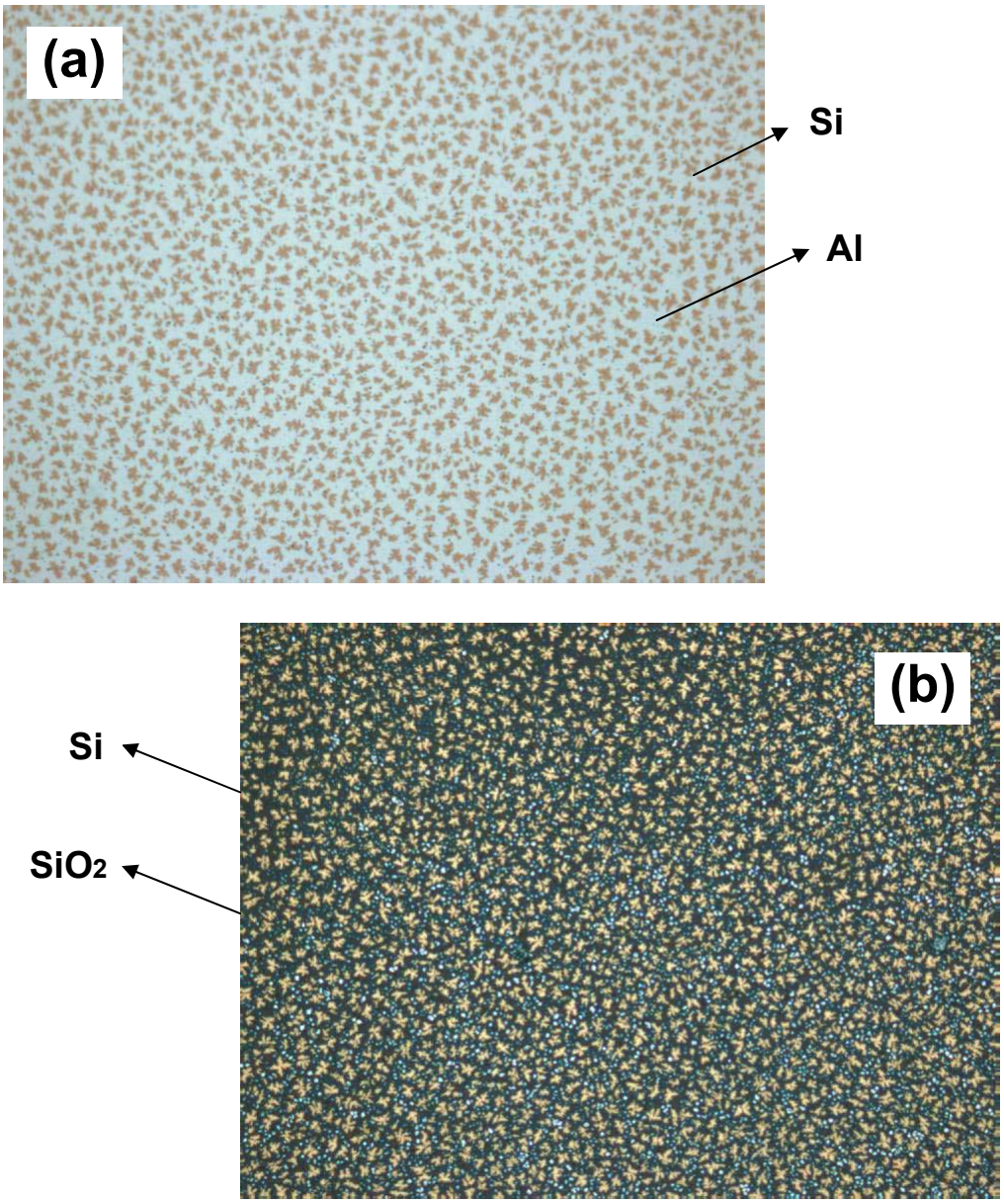

Fig. 4.1 (a) the surface of Al/polysilicon stack on thermal oxide after anneal (b) the surface of Al/polysilicon after anneal followed by Al removal using wet chemical solutions. Annealing was done in a furnace at 450°C for 30 min. Noted that orange spots are Si and light blue colors are Al in (a) while black colors are oxide in (b), indicating non-uniform reaction of Al and polysilicon. Removal of Al exposed oxide layer.

HRXTEM images show a full substitution of aluminum (Al) for polysilicon when Ti/Al/polysilicon structure is used, as seen in Fig. 4.2. Fig. 4.2 (a) shows crystalline polysilicon on thin HfAlON film before a stack of Ti/Al/polysilicon/HfAlON/Si-substrate was annealed. After the stack was annealed at 450°C in a furnace, polysilicon moved to Ti layer and then Ti-silicide was formed while Al was re-located to the position where polysilicon existed initially as seen in Fig. 4.2 (b) and (c). Additionally, focused images of the interfaces between gate and HfAlON gate dielectric show a crystalline phase of Al. No defect on HfAlON gate dielectric was observed, indicating that the HfAlON gate dielectric is not damaged by Al substitution.

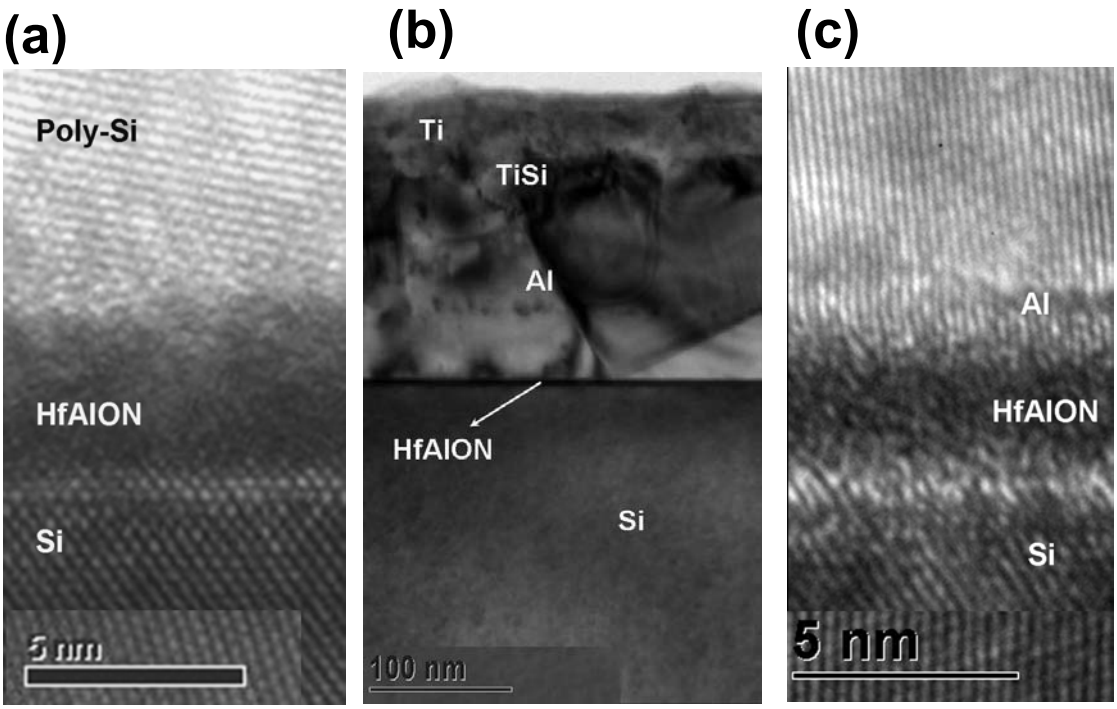

Fig. 4.2 HRXTEM images; (a) polysilicon on HfAlON before Al substitution, (b) after annealing of Ti/Al/polySi on HfAlON for Al substitution. It is observed that polysilicon is fully substituted with Al and diffused towards Ti, forming Ti-silicide. (c) Focused image of the interface of substituted-Al and HfAlON. The substitution of Al was done by annealing at 450°C in a furnace.

Depth profiles of Ti/Al/polysilicon/HfAlON/Si-substrate stack before and after annealing at 450C were examined using AES analysis. Figure 4.3 clearly shows that Si moved to Ti layer and then reacted with Ti, forming Ti-silicide. Most Al atoms were found on the top of HfAlON. Both TEM and AES results confirm that Al is completely substituted for polysilicon through annealing at 450°C.

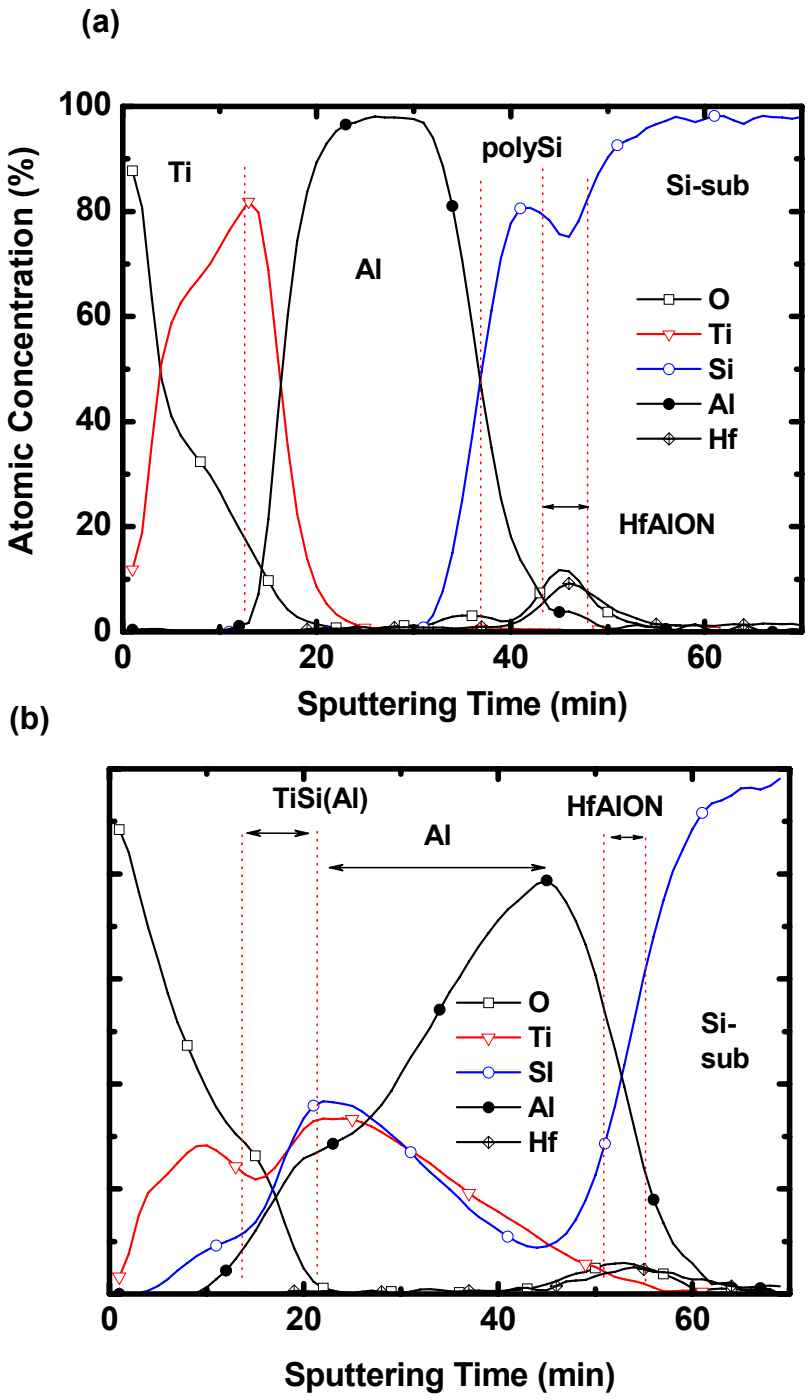

Fig. 4.3 AES depth profiles of Ti/Al/polysilicon on HfAlON (a) before and (b) after Al substitution with polysilicon. Silicon is diffused towards Ti and reacted with Ti, resulting in TiSi formation.

4.4.2 C-V characteristics

In order to investigate the property of substituted Al (SA) as a gate electrode, the C-V characteristics of substituted Al gated MOS capacitors were investigated with various gate dielectrics. Figure 4.4 and 4.5 show high frequency C-V curves of SA and FUSI NiSi gated MOS capacitors with SiO_2 dielectric. No matter whether polysilicon is doped before both Al substitution and Ni silicidation, the accumulation capacitances of both substituted Al and Ni silicided gates were identical, indicating there is little difference in the EOT values of two gates.

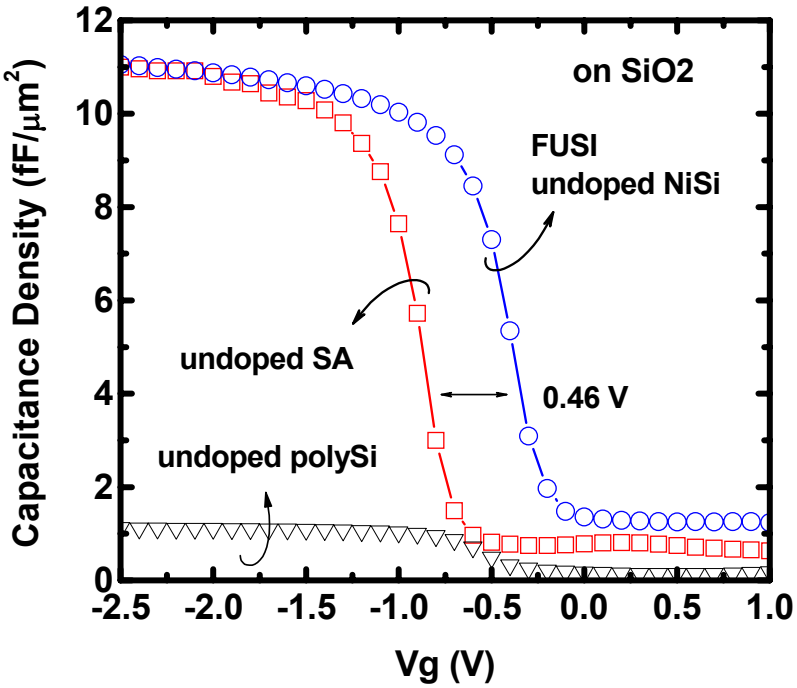

Fig. 4.4 C-V curves of MOS capacitors with SA or FUSI NiSi of undoped polysilicon on SiO_2. Both Al substitution and FUSI silicidation shows identical EOT, indicating the full substitution of undoped polysilicon

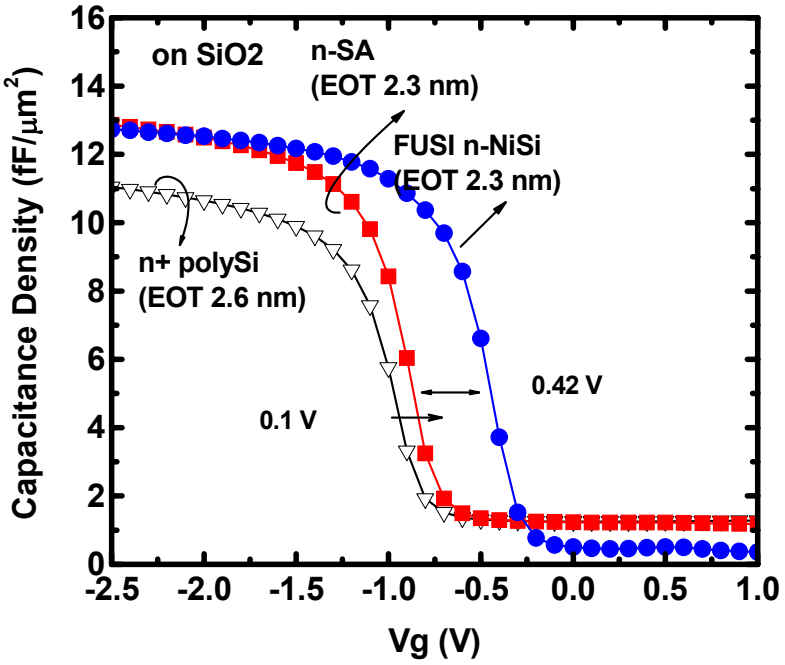

Fig. 4.5 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA), and FUSI NiSi of n^+ polysilicon (n-NiSi) on SiO_2. Both gates show V_{fb} shift and EOT reduction after SA and FUSI processes.

The flat-band voltage (V_{fb}) of substituted Al for undoped polysilicon (undoped SA) was lower than that of fully Ni-silicided undoped polysilicon (undoped NiSi), and about 0.5V of V_{fb} difference was obtained. About + 0.1 V and + 0.5 V of V_{fb} shifts were observed for substituted Al for n^+ polysilicon (n-SA) and fully Ni-silicided n^+ polysilicon (n-NiSi), respectively, compared to that of n^+ polysilicon gate on SiO_2. The V_{fb} difference between n-SA and n-NiSi was about 0.4 V, which is lower than the V_{fb} difference between SA and NiSi. These results suggest that the work function of SA is much lower than that of n-NiSi. The lower V_{fb} of n-NiSi gate than that of NiSi gate may be due to n-type dopant segregation at the interface between n-NiSi and gate dielectric [4.14].

Fig. 4.6 and 4.7 show the C-V characteristics of both gates on re-oxidized Si_3N_4 and ALD Al_2O_3 gate dielectrics. EOT reduction was observed for both gates on re-oxidized Si_3N_4 gate dielectrics. Similar findings were also observed for SA gate on Al_2O_3 dielectric. However, after Al was substituted for n^+ polysilicon on re-oxidized Si_3N_4 (or SiO_2) and Al_2O_3, a V_{fb} shift in the opposite direction was observed. About 0.15 V of positive V_{fb} shift was observed for SA gated Si_3N_4 (about + 0.1V for SA gated SiO2) compared to that of n^+ polysilicon gate while about 0.3 V of negative V_{fb} shift was found for SA gated Al_2O_3. Since the V_{fb} of n+ polysilicon gate depends on gate dielectrics, the value of V_{fb} is also affected even after both Al substitution and Ni silicidation.

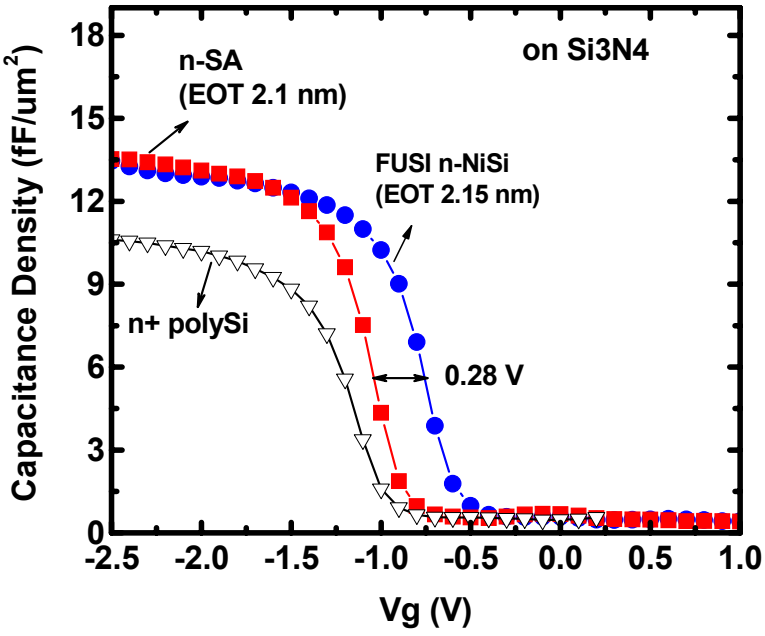

Fig. 4.6 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA), and FUSI NiSi of n^+ polysilicon (n-NiSi) on Si_3N_4. Both gates show V_{fb} shift and EOT reduction after SA and FUSI processes.

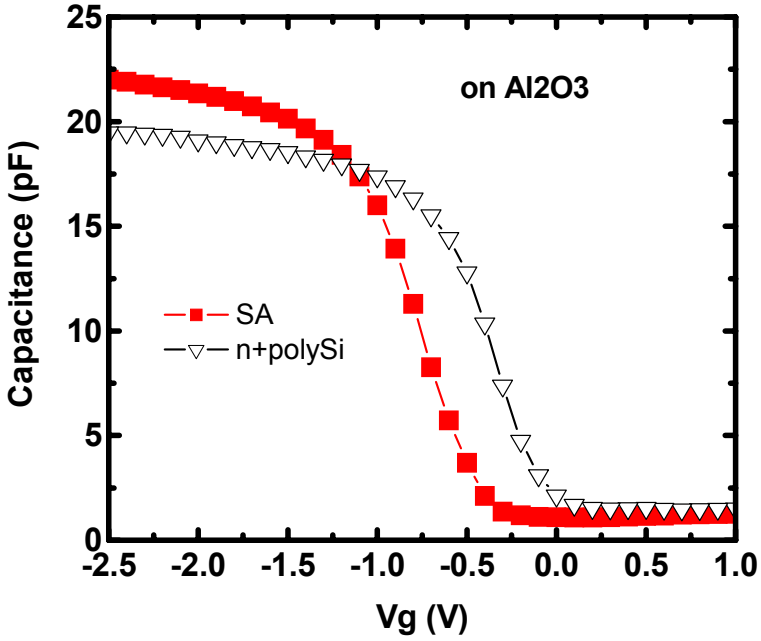

Fig. 4.7 C-V curves of MOS capacitors with phosphorus doped n^+ polysilicon, substituted Al of n^+ polysilicon (n-SA) on Al_2O_3. Al_2O_3 was deposited by ALD CVD. High positive V_{fb} shift of n^+ polysilicon is due to Fermi level pinning at the interface between Al_2O_3 and polysilicon. Negative V_{fb} shift and EOT reduction is observed after Al substitution.

This shows a dependence of gate dielectric on V_{fb} of n^+ polysilicon gate, which may be due to fixed oxide charges of dielectric and pinned Fermi level at the interfaces between n+ polysilicon and gate dielectric. For n^+ polysilicon gate, negative fixed oxide charges of Al_2O_3 gate dielectric lead to the positive V_{fb} shift. In addition, Al-O-Si chemical bonds found at the interface between polysilicon and Al_2O_3 may lead to Fermi level pinning below the valence band (E_v) of silicon [4.2].

The C-V characteristics of SA gate on high-K dielectric were also investigated. Fig. 4.8 and 4.9 show the C-V curves of SA, n-SA, NiSi and n-NiSi on HfAlON gate dielectric. Identical EOT was observed for both SA gates and FUSI NiSi gates on HfAlON, which indicates that Al on HfAlON is substituted completely for both n^+ and undoped polysilicon. The amount of V_{fb} differences between SA gates and NiSi gates

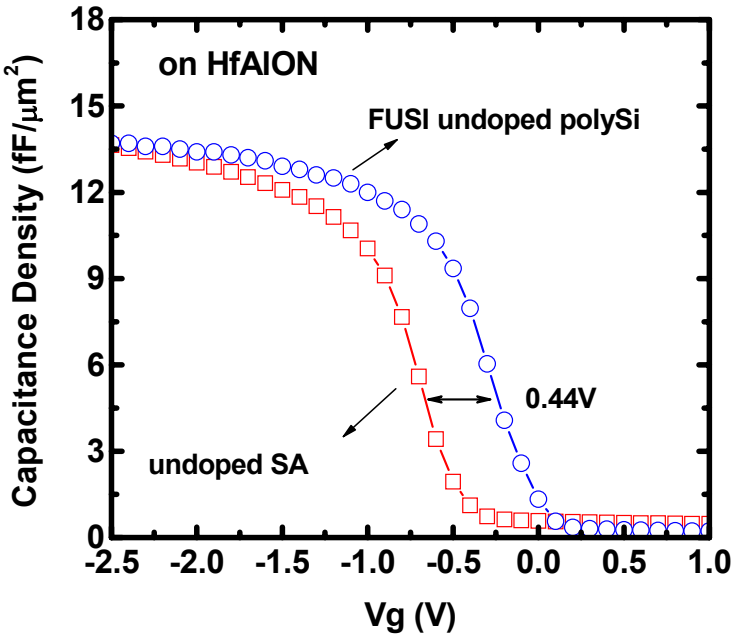

Fig. 4.8 C-V curves of MOS capacitors with substituted Al and FUSI NiSi of undoped polysilicon on HfAlON. Identical EOT and 0.44 V of V_{fb} difference are observed after SA and FUSI processes.

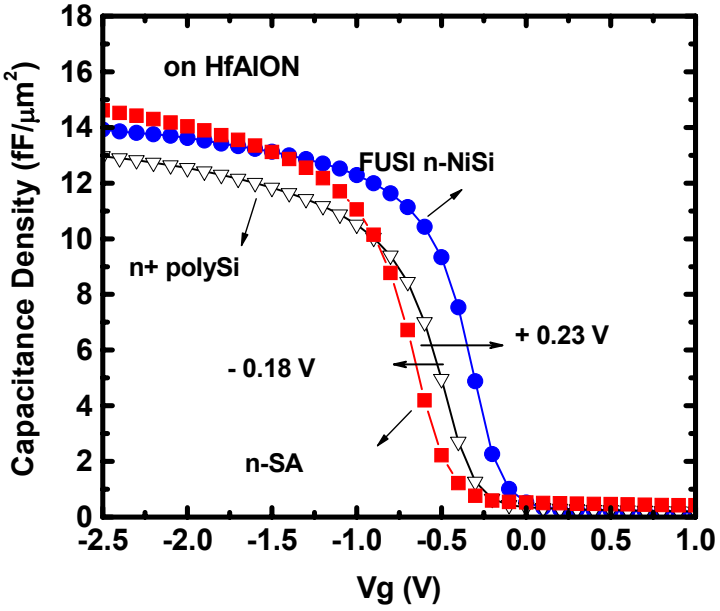

Fig. 4.9. C-V curves of MOS capacitors with substituted Al and FUSI NiSi of n^+ polysilicon on HfAlON. Compared to n^+ polysilicon, lower V_{fb} is observed in SA gate and larger V_{fb} is observed in FUSI n-NiSi gate.

on HfAlON were very close to the differences between both gates on SiO_2. The V_{fb} of SA gated HfAlON capacitor was shifted negatively, which is similar to that of SA gated Al_2O_3 capacitor as described above. However, these two capacitors differed in the amount of V_{fb} shift. For HfAlON, it was smaller than that for Al_2O_3. This difference could be attributed to different fixed oxide charges of Al_2O_3 and HfAlON, and fewer Al-O-Si bonds in HfAlON than in Al_2O_3 due to Hf in HfAlON film.

Figure 4.10 shows the C-V characteristics of SA gates prepared using different doping types of gate polysilicon. The V_{fb} of SA gate shows no dependence on doping of polysilicon, which implies that dopant segregation at the top interface of high-K during SA process is negligible. The C-V curve measured on SA gated nMOSFET as shown in Fig. 4.11 confirms there was no polysilicon depletion indicating full substitution of n^+ polysilicon with Al. The EOT reduction phenomenon was also observed in SA process and the amount of EOT reduction was identical for both processes, which is consistent with the result that FUSI process has shown EOT reduction compared to n^+ polysilicon gate [4.2]. The reduced EOT was 0.3 nm for SiO_2 and HfAlON, but 0.5 nm for re-oxidized Si_3N_4 dielectric. It appears that the amount of EOT reduction depends on dielectric.

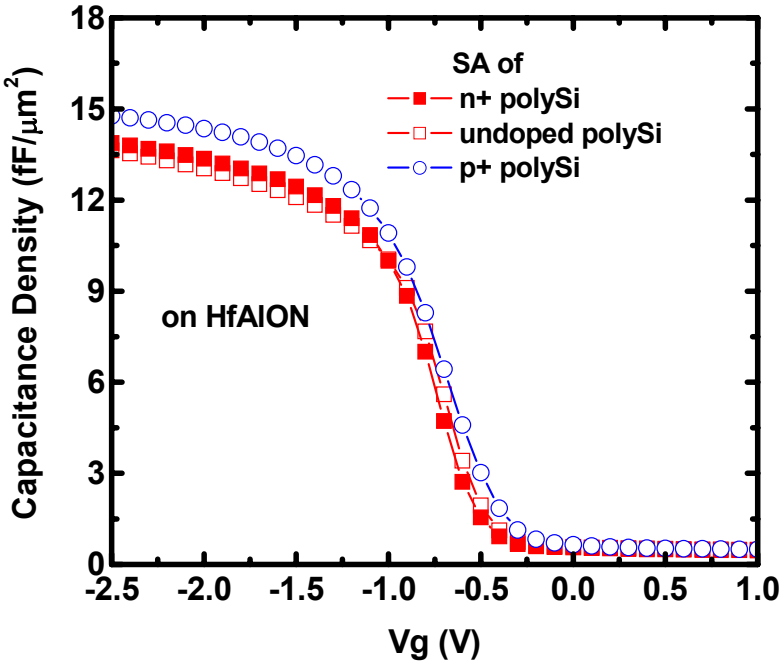

Fig. 4.10 C-V curves of MOS capacitors with SA gates formed using n^+ polysilicon (n-SA), p^+ polysilicon (p-SA), and undoped polysilicon (SA).The negligible difference in V_{fb} indicates that the work function value of SA on high-K does not depend on polysilicon pre-doping.

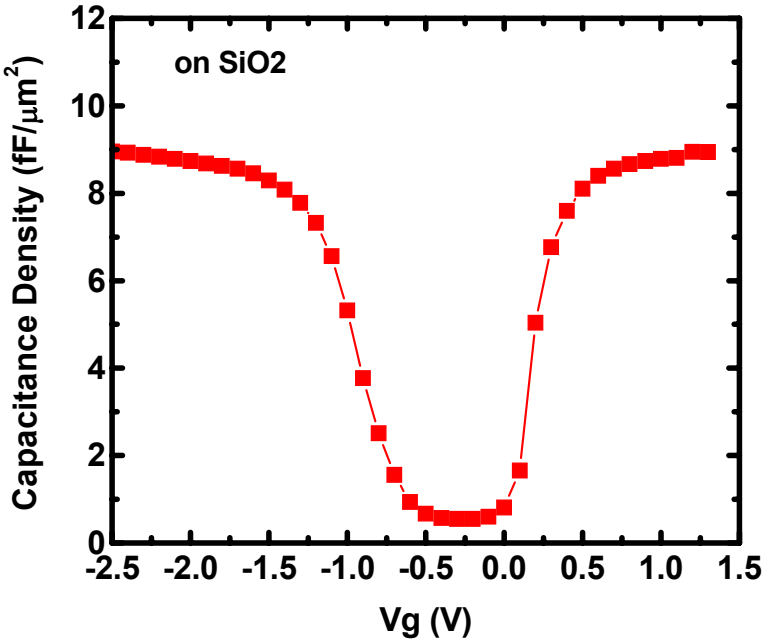

Fig. 4.11. High frequency C-V curves of substituted Al gate measured on nMOSFET. Source and drain were grounded for measurement. No polysilicon depletion is observed after substitution of Al.

4.4.3 Work function of Substituted Al Gate and Fermi level pinning

Work function difference of n+ polysilicon gate on SiO_2 and HfAlON was similar to V_{th} difference of n+ polysilicon gated SiO_2 and HfAlON nMOSFETs as shown in Fig. 4.12 and 4.13. This work function difference has been understood to be due to Fermi level pinning, which may be attributed to Hf-Si and Si-Al-O bonding [4.2]. Figure 4.14 and 4.15 show that work function difference of n-NiSi was determined to be about 0.1 V whereas that of SA was almost zero. This suggests that there is no Fermi level pinning for SA gate, which could be due to Si free at the interface between SA gate and HfAlON gate dielectric. It has been understood that Fermi level pinning on high-K could be due to chemical bonding at the interface between gate and high-K dielectric and also due to high temperature annealing [4.4, 4.5].

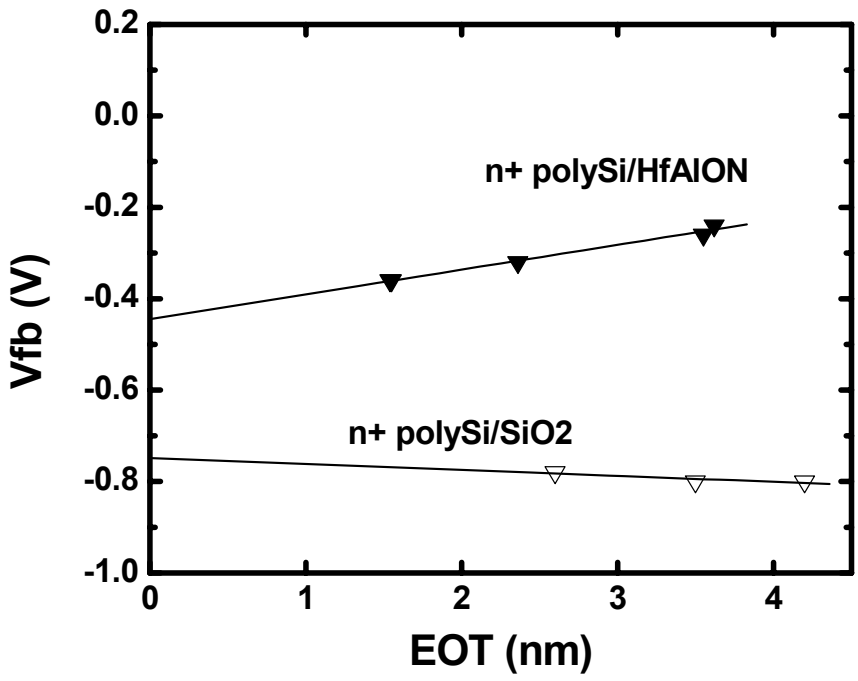

Fig. 4.12 Plots of EOT vs. flat-band voltage for n+ polysilicon gate on SiO_2 and HfAlON.

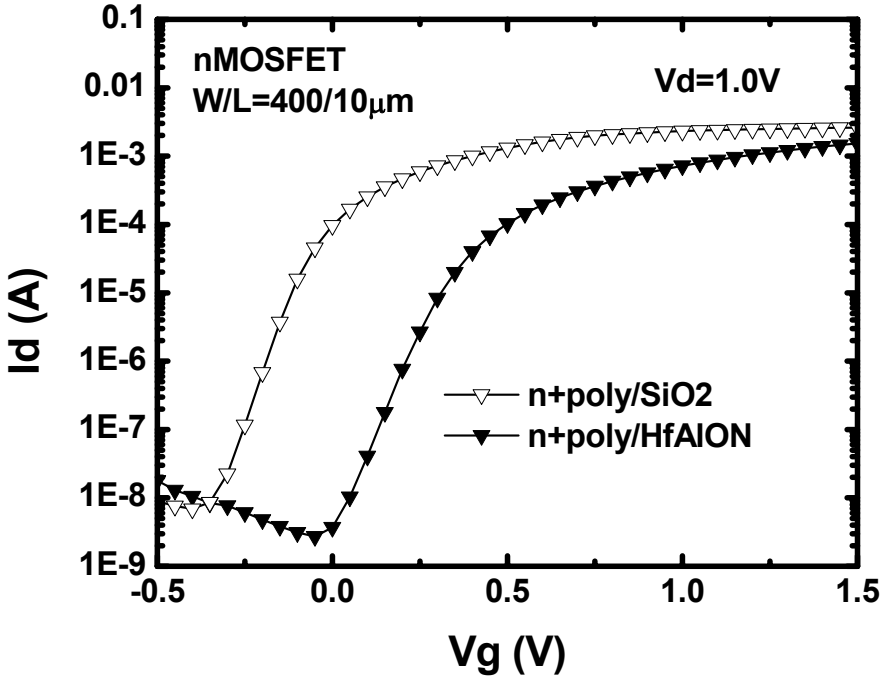

Fig. 4.13 Characteristics of I_d-V_g for n+polysilicon gated SiO_2 and HfAlON nMOSFETs. About 0.35 V of V_{th} difference is observed.

As observed in TEM and AES depth profile of SA gate, Al substitution removed Si from the interface, leading to few Si bonding at the interface. In addition, the implementation of SA gate was done by a low temperature thermal process, suggesting that SA was not annealed at high temperature. However, NiSi gate still includes Si bonding at the interface between NiSi gate and HfAlON gate dielectric. Although FUSI process had not undergone by a high temperature annealing, it still has Si chemical bonding at the interface, which may be another factor to give rise to Fermi level pinning. This can be evidenced by the work function difference of NiSi gate on SiO_2 and HfAlON as seen in Fig. 4.15.

Therefore, the substitution of Al for polysilicon may be a possible practical way to overcome Vth instability which may be attributed to Fermi level pinning problem.

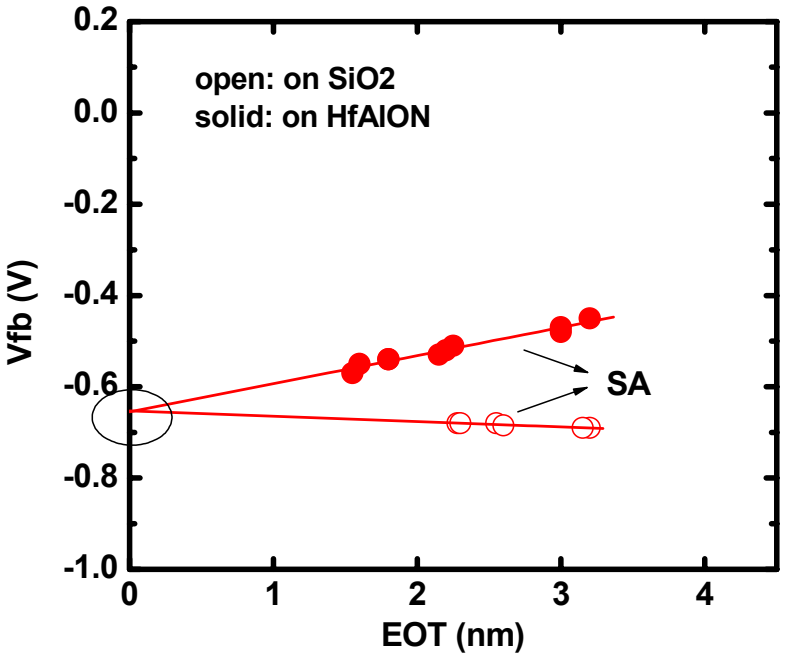

Fig. 4.14 Plots of EOT vs. flat-band voltage for SA gates on SiO_2 and HfAlON.

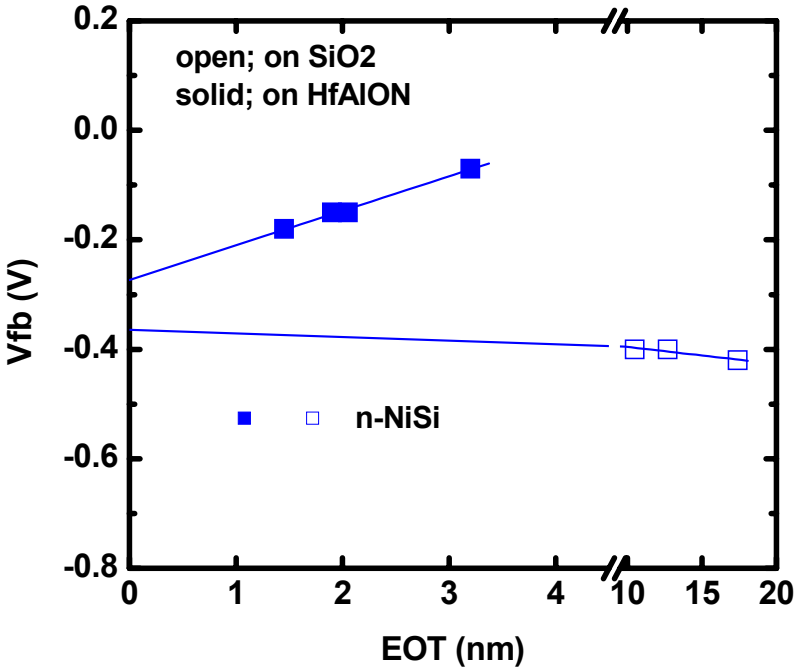

Fig. 4.15 Plots of EOT vs. flat-band voltage for n-type FUSI NiSi gate on SiO_2 and HfAlON.

4.4.4 I-V characteristics

The representative leakage current characteristics of re-oxidized Si_3N_4 and HfAlON gate dielectric with n-SA, FUSI, and n^+ polysilicon gates are compared in Fig. 4. 16 and Fig. 4.17. A lower leakage current of n^+ polysilicon gate is due to its thicker EOT. After silicidation and Al substitution of n^+ polysilicon, EOTs of both gates are reduced, leading to slightly high leakage current. However, when the leakage currents of these gates are compared through the plot of EOT versus gate leakage current as seen in Fig. 4.18 and 4.19, SA process did not affect gate leakage current characteristics. The SA gate on high-K dielectric shows slightly lower leakage current than n^+ polysilicon gate on high-K dielectric and comparable to FUSI NiSi gate on high-K. Cumulative plots of leakage current distribution in Fig. 13 also show that the SA gate on HfAlON has much better uniformity in leakage current distribution compared to n^+ polysilicon or FUSI on HfAlON, indicating that SA has better process stability than both FUSI and n^+ polysilicon gates.

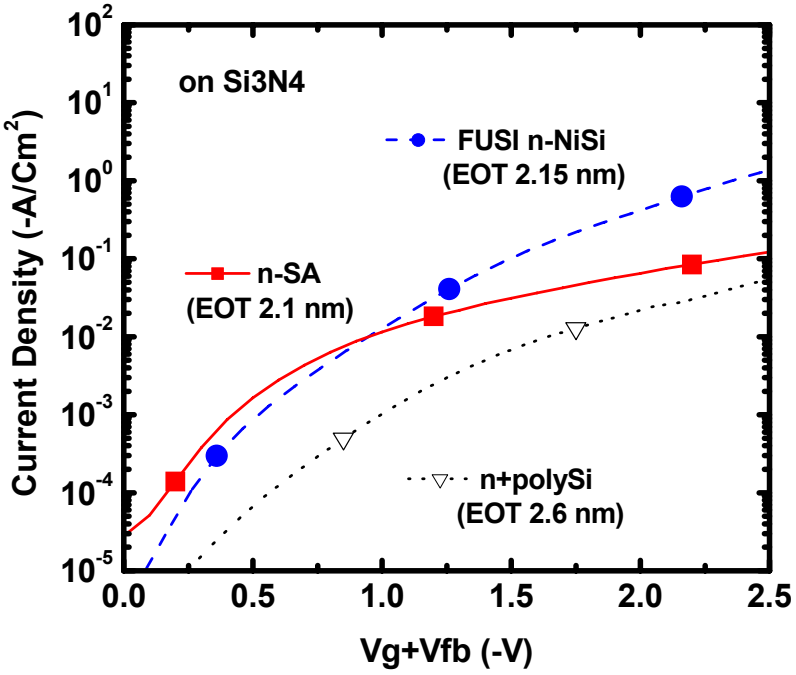

Fig. 4.16 Leakage current characteristics of n-SA and FUSI n-NiSi gate on reoxidized CVD Si_3N_4. Comparable leakage currents are observed between SA and FUSI gates.

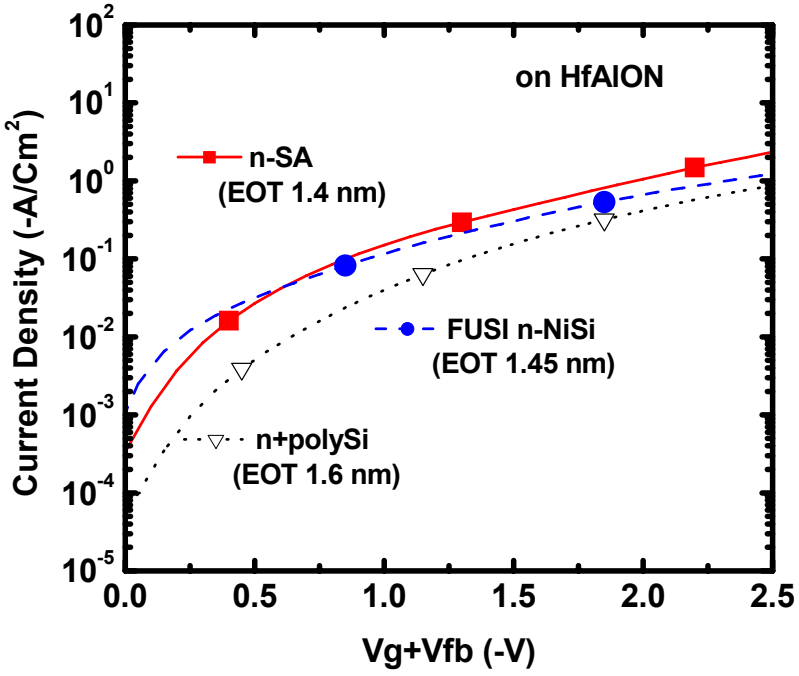

Fig. 4.17 Leakage current characteristics of n-SA and FUSI n-NiSi gate on HfAlON high-K dielectrics. Comparable leakage currents are observed between SA and FUSI gates.

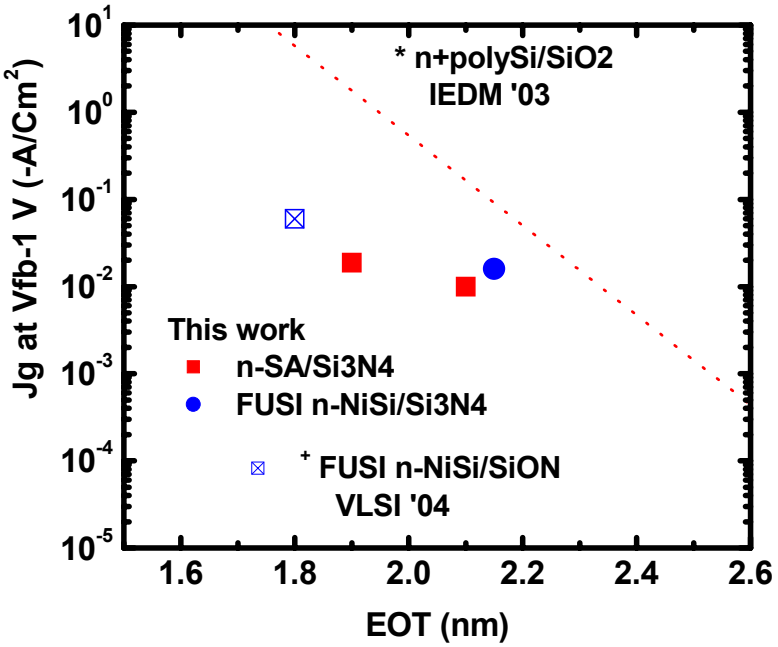

Fig. 4.18 Plots of leakage current vs. EOT for Si_3N_4. Benchmarked data are also compared. The SA gate on high-K shows slightly lower leakage current than n^+ polysilicon gate on high-K and comparable to FUSI NiSi gate on high-K. The results denoted by * (n^+polySi/SiO_2) and + (FUSI n-NiSi/SiON) are quoted from ref. [4.13] and [4.14], respectively.

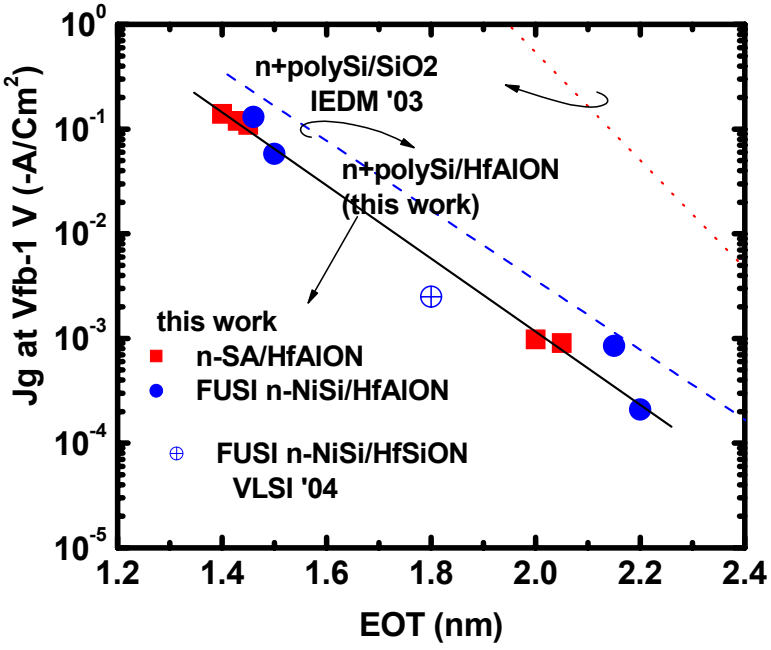

Fig. 4.19 Plots of leakage current vs. EOT for HfAlON dielectric. Benchmarked data are also compared. The SA gate on high-K shows slightly lower leakage current than n^+ polysilicon gate on high-K and comparable to FUSI NiSi gate on high-K. The results denoted by * (n^+polySi/SiO_2) and + (FUSI n-NiSi/HfSiON) are quoted from ref.[4.13] and [4.14], respectively.

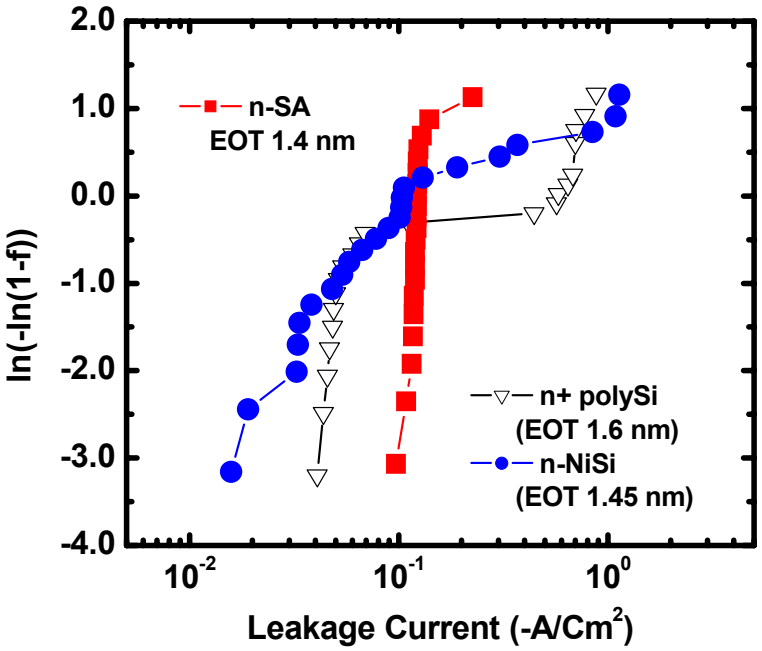

Fig. 4.20 Cumulative plot of leakage current distribution measured at V_{fb}-1V of (a) n^+ polysilicon, n-SA, and FUSI n-NiSi gates on HfAlON dielectric.

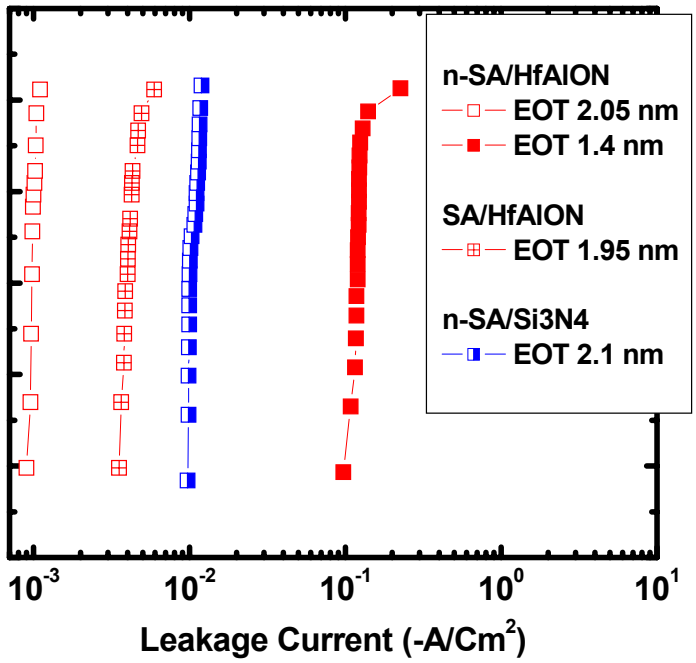

Fig. 4.21 Cumulative plot of leakage current distribution measured at V_{fb}-1V of SA gates on HfAlON with different EOTs and on Si_3N_4 gate dielectrics.

4.5 Summary

Substituted Al (SA) gate is successfully demonstrated on SiO_2, Si_3N_4 and HfAlON high-K dielectric. The work function of substituted Al gate is determined to be about 4.25 eV. Polysiliocn depletion and Fermi level pinning are completely eliminated by Al substitution of polysilicon. It is free from thermal instability issue as Al substitution is implemented after all the high temperature processes. No damage or reaction at metal gate/high-K interface in SA gate process resulted in improved leakage current distribution. Since the SA process can be done as low as 450°C which is also the suitable temperature for FUSI NiSi process [4.11, 4.12], it can provide a possible integration scheme for dual metal gate on high-K dielectric, with FUSI NiSi for pMOSFET and SA for nMOSFET.

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Chapter 5

Pt Rich Pt_xSi Metal Gate on High-K Dielectric for High Work Function and Reduced Fermi Level Pinning

In this chapter, high work function of Pt_xSi gate, which is suitable for pMOSFET, is presented. Without pre-doping of polysilicon, Pt_xSi allows much higher positive V_{FB} shift on high-K dielectric and also reduces Fermi level pinning problem on high-K dielectric. This may be due to high concentration of Pt in Pt_xSi, leading to less Si bonds at the interface of Pt_xSi gate and high-K dielectric. When Pt_xSi is combined with substituted Al (SA), a wide range of work function difference (0.65 eV) is achieved, which can be utilized for dual metal gate process scheme.

5.1 Introduction

Downscaled MOSFETs need metal gate since it enables MOSFET to scale down further. It becomes more imperative especially with high-K dielectric because there has been a concern about the interface instability of polysilicon gate and high-K dielectric. Moreover, dual metal gated CMOS devices are required to be ready in the near future as projected in recent ITRS road map [5.1]. For bulk CMOS devices, the work functions of metals for integrating dual gate should be within 0.2 eV of the E_C and E_V of Si for n and pMOSFET, respectively [5.2]. The achievement of such work functions on high-K dielectric is still a challenge because of Fermi level pinning and thermal instability of the gate/dielectric interface [5.3 – 5.6]. As one of dual metal gate process schemes to achieve such a wide range of work function, Fully Silicided (FUSI) metal silicide gate process has drawn attention as it has shown a potential capability of work function modulation using pre-doping of polysilicon [5.7]. However, phosphorous (P) or arsenic (As) doping in polysilicon on high-K dielectric caused excessive leakage current through high-K dielectric, demanding a careful doping process [5.8]. Boron (B) penetration problem due to high diffusivity of B in Hf-based high-K dielectric has also been addressed [5.9, 5.10]. In addition, the Fermi level pinning on high-K dielectric may not be eliminated by FUSI process, which may be due to Si-Hf bonds at the interface between metal silicide gate and Hf-based dielectric [5.11].

Substituted Al (SA) gate described in previous chapter has shown 4.25 eV of work function, which is suitable for nMOSFET. SA gate on high-K dielectric did not have Fermi level pinning problems. However, similar approach for pMOSFET without B pre-doping of polysilicon on high-K has not been identified yet.

Although Pt is not substituted when it is in contact with polysilicon, it may have a similar effect of substitution if Pt concentration is high enough in platinum silicide

(Pt_xSi). In this study, we propose and demonstrate that Pt with Ti capping layer can achieve high work function without pre-doping of polysilicon, which is suitable for pMOSFET. The Ti/Pt process can be used together with SA process for complete dual metal gate CMOS process.

5.2 Experiment

MOS devices with HfAlON dielectric were fabricated. HfAlON high-K gate dielectric was formed by deposition of MOCVD HfAlO films followed by annealing in an NH_3 ambient at 800°C. For comparison, thermally grown SiO_2 gate oxides were also prepared. Undoped or *in-situ* P-doped polysilicon was deposited on top of gate dielectric and annealed at 900°C for 30 min. For all processes, 40 nm of polysilicon was used. For Al substitution process, about 200 nm of Al was sputtered on top of polysilicon right after DHF cleaning, followed by about 100 nm of Ti deposition using PVD. For Pt_xSi formation, 200 nm of Pt was sputtered. For some Pt samples, Ti sputtering was also done sequentially without being exposed to air for the purpose of capping. For NiSi formation, about 50 nm of Ni was also prepared without Ti capping. Ti/Al/polySi/HfAlON structure was used for n-MOSFET, while Ti/Pt/polySi/HfAlON structure for pMOSFET. FUSI NiSi was also prepared for comparison. All NiSi, Ti/Pt, and Al substitution were done at the same temperature of 450°C in a furnace tube.

5.3 Results and Discussion

5.3.1 Effect of Ti capping

In order to successfully integrate dual metal using substitution of silicon, a metal that has high work function and can be fully substituted with silicon is needed. As a low work function of Al was the one for nMOSFET, a few metals such as W, Ni, Ru and Pt can be candidates for pMOSFET because the work functions of these metals are higher than the midgap of Si. Unlike Al, most of such metals tend to form silicide with silicon rather than being substituted. However, Pt can form Pt-silicide (Pt_xSi) whose Pt concentration is high enough in Pt_xSi, which may have a similar effect of metal substitution observed in SA gate. To form Pt_xSi with such high x, silicon movement in Pt should be as easy as possible and Pt should be thick enough compared to polysilicon. It was found that Ti capping layer on top of Pt during Pt_xSi formation plays a critical role in process control as well as work function modulation.

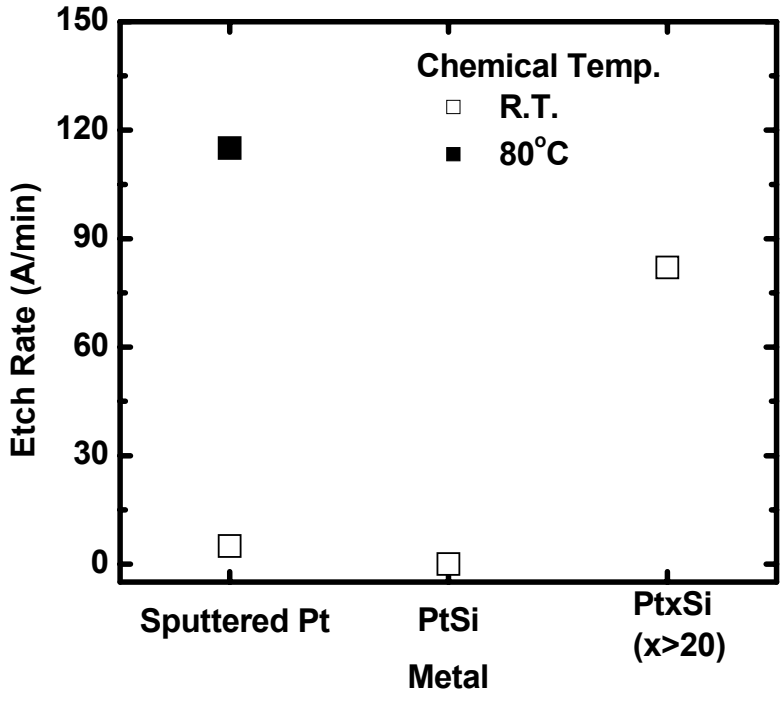

Fig. 5.1 Wet etching rates of Pt and Pt-rich Pt-silicide

Figure 5.1 shows that it was hard to etch PtSi (x=1.0) using wet chemical solution even at high temperature but Pt_xSi was easily etched by the same solution at room temperature when Pt concentration is high. In addition, as observed by a visual inspection in Fig. 5.2 (a) and (b), when Pt_xSi is formed without Ti capping layer, a lot of wet etching residues were found on field oxide after Pt_xSi is formed and removed sequentially. This indicates that the Pt_xSi formation is not uniform and x in Pt_xSi is low. This was also confirmed from SEM/EDX analysis on the residue, which shows a large amount of Si in Pt_xSi. When Ti capping layer is used, such residue is not observed, indicating uniformly high concentration of Pt in Pt_xSi.

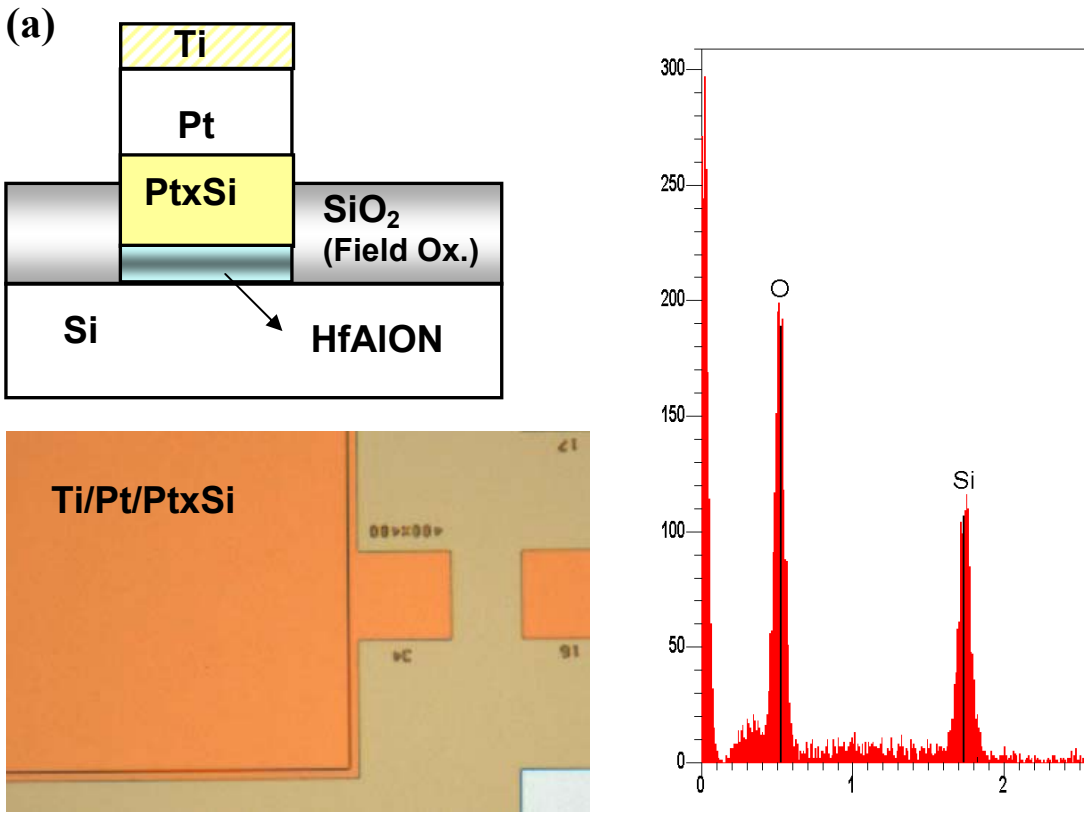

Fig. 5.2 (a) Visual inspection and SEM-EDX analysis of surface after wet etching of Ti capped Pt/Pt_xSi. Clean gate patterns are observed. No Pt is detected on field oxide surface.

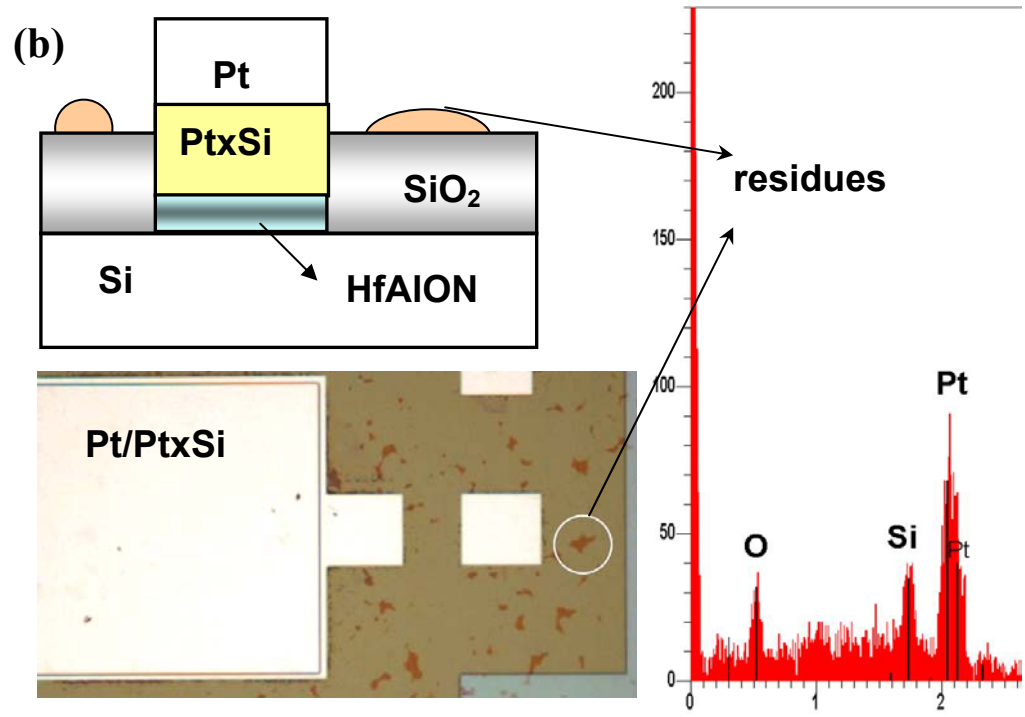

Fig. 5.2 (b) Visual inspection and SEM-EDX analysis of surface after wet etching of Pt/Pt_xSi stacks. Wet etch Pt-silicide residues are observed on field oxide.

Interestingly, Pt_xSi on HfAlON, formed with Ti capping layer, shows thinner EOT and higher V_{fb} compared to the case of without Ti capping layer as shown in Fig. 5.3 (a). Figure 5.3 (b) also shows that gate leakage current is also reduced when Ti capping layer is used, even though EOT becomes thinner. All these results are probably due to different amount of oxygen in Pt_xSi when Ti capping layer is present. Oxygen (O) can diffuse preferably along grain boundaries in polycrystalline Pt film [4.13] and then suppress the movement of Si along the grain boundaries of Pt, resulting in high concentration of Si in Pt_xSi.

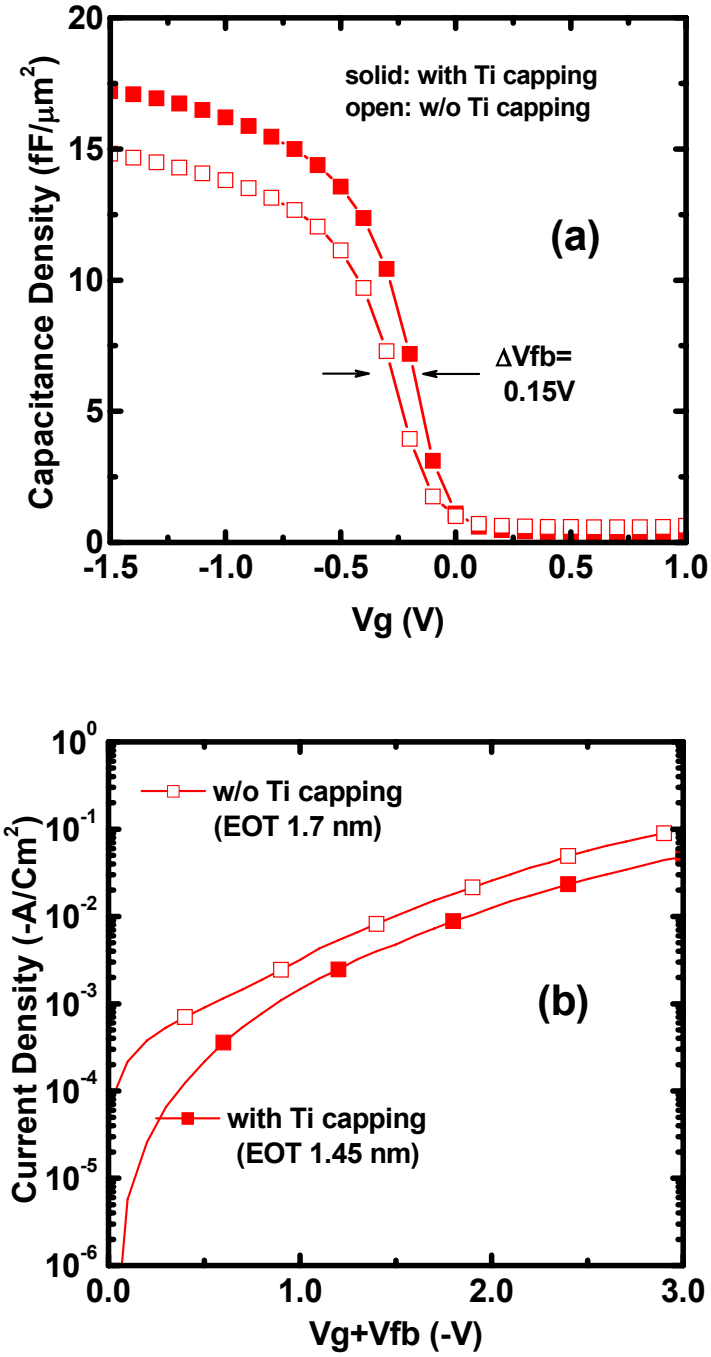

Fig. 5.3 (a) C-V curves of Pt_xSi/HfAlON capacitors formed with and w/o Ti capping. (b) Gate leakage currents of Pt_xSi gates with HfAlON formed with and without Ti capping.

The XPS depth profile in Fig. 5.4 also confirms that there is no Ti diffusion into Pt and Pt concentration near the gate dielectric interface is clearly higher when Ti capping is used.

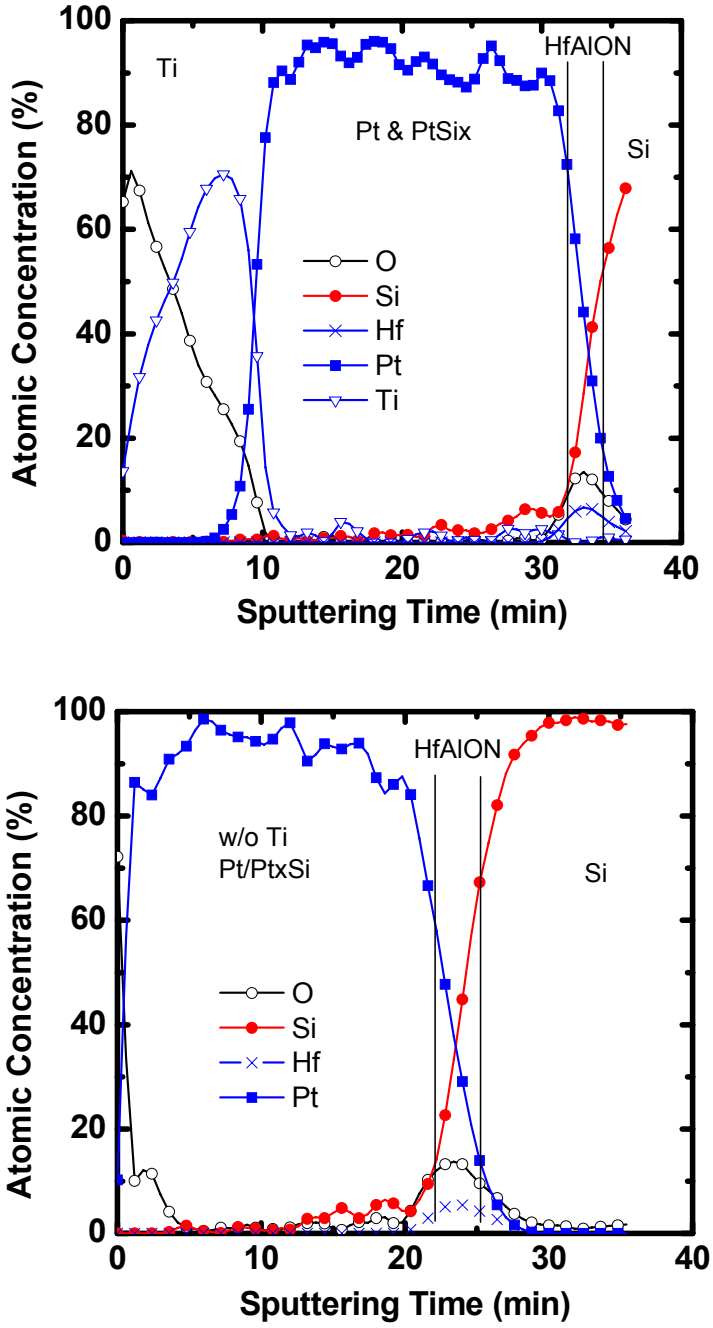

Fig. 5.4 XPS depth profile of Pt rich Pt-silicide gate on HfAlON

Fig. 5.5 shows that the amount of O in Ti capped Pt_xSi stack was almost at noise level while a fairly large amount of O is observed in Pt_xSi stack without Ti capping. TEM images of Ti/Pt/Pt_xSi/HfAlON stack confirm the polycrystalline structure of Pt and Pt_xSi, and a very low amount of Si atoms in Pt_xSi were also observed by TEM/EDX analysis as shown in Fig. 5.6. HfAlON gate dielectric is quite intact after Pt_xSi formation process.

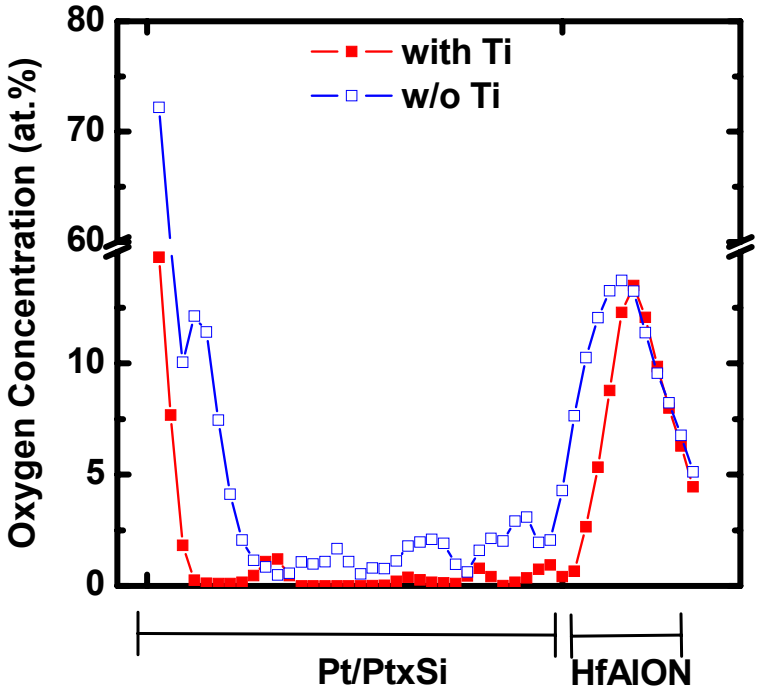

Fig. 5.5 Oxygen distribution in Pt/Pt_xSi layer for Ti capped and without Ti capping

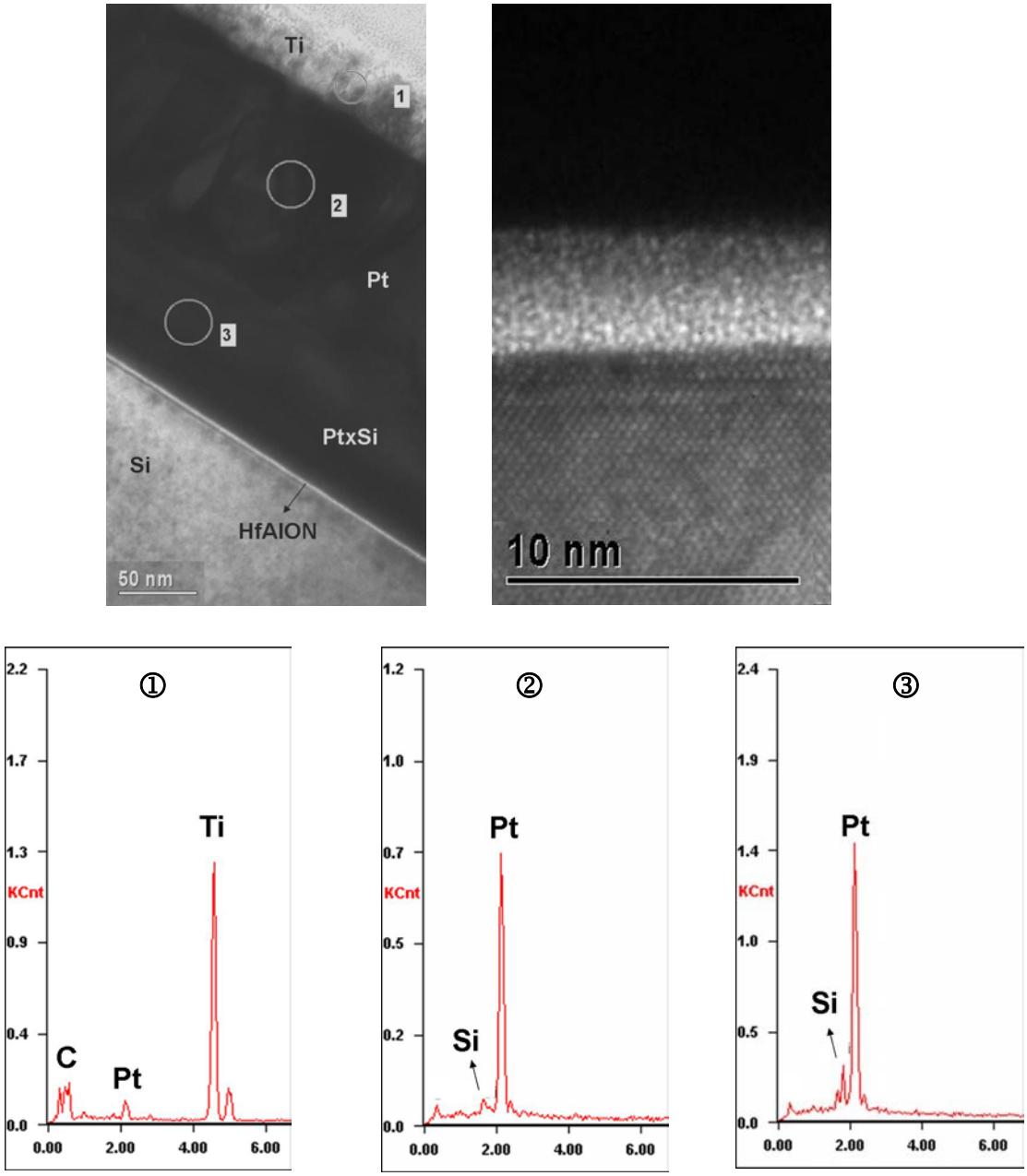

Fig. 5.6 HRXTEM of Pt_xSi on HfAlON. No damage to HfAlON dielectric is observed.

5.3.2 Characteristics of Pt-rich Pt-silicide gated MOS characteristics

The work functions of Pt_xSi were also affected by the presence of Ti capping layer, as seen in Fig. 5.7 (a) and (b). Extracted work function values of Pt_xSi on SiO_2 and high-K are 4.98 eV and 4.9 eV respectively for the case of with Ti capping layer, and 4.92 eV and 4.75 eV for without Ti capping layer. Ti capped Pt_xSi gate shows higher work function closer to E_V of Si. The work function difference between Pt_xSi on SiO_2 and HfAlON was also reduced when Ti capping was used, suggesting reduced Fermi level pinning. Both higher work function and reduced Fermi level pinning is attributed to higher Pt and lower Si concentrations in Pt_xSi by Ti capping as reported that the presence of Si at metal-dielectric interface worsens Fermi level pinning [5.3].

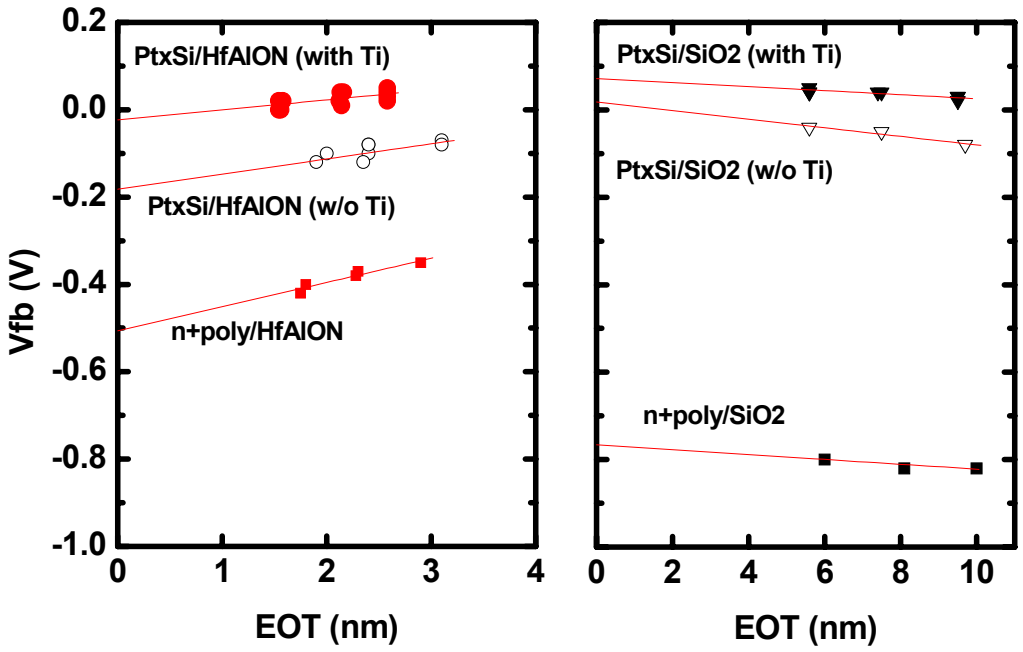

Fig. 5.7 Plots of EOT vs. V_{fb} for Pt-silicide and n^+ polysilicon gates on SiO_2.

Figure 5.8 shows the C-V curves of various gates with and without pre-doping of polysilicon on high-K dielectric. The V_{fb} difference of 0.65 V between SA and Pt_xSi

gates is maintained regardless of pre-doping. Since the work function of SA gate is not affected by pre-doping of polysilicon [5.12], indicating that the work function of Pt_xSi

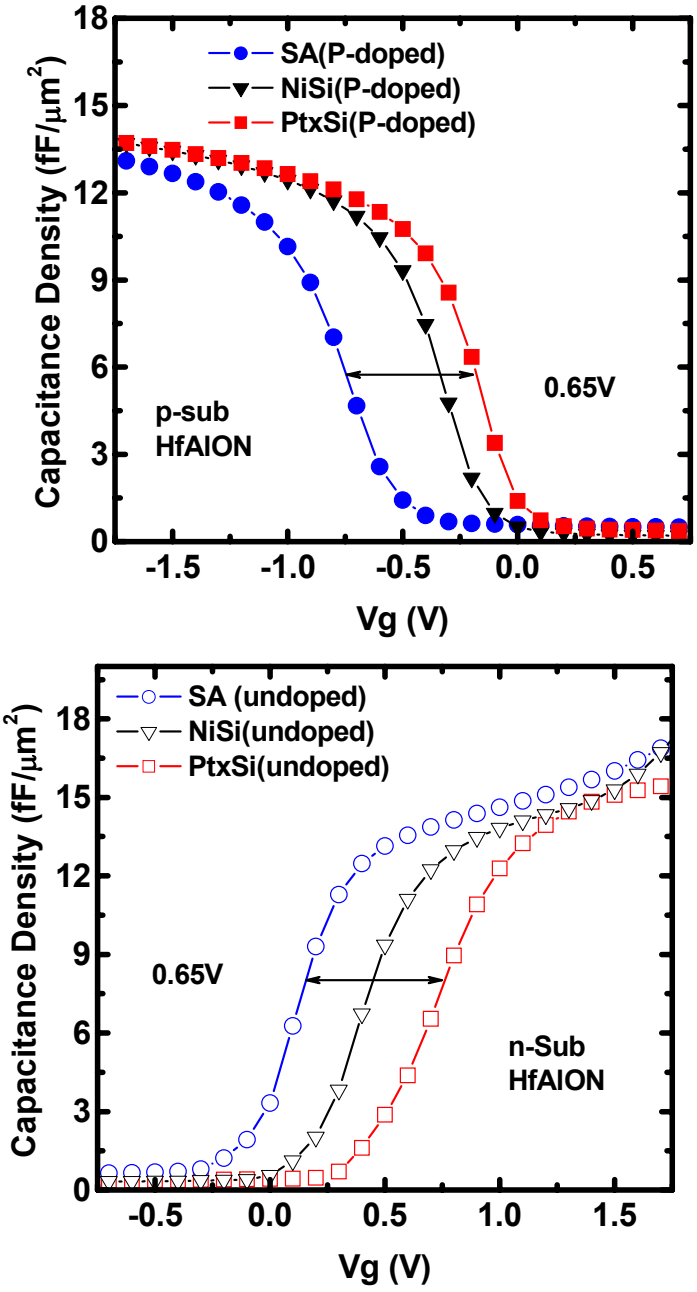

Fig.5.8 C-V curves of SA and Pt_xSi gates with HfAlON on p-Si substrate. Both gates were formed using P-doped polysilicon and undoped polysilicon for p-Si substrate and n-Si substrate, respectively

with Ti capping has no effect on polysilicon pre-doping. The V_{FB} difference is also consistent with the work function difference between SA (4.25eV) and Pt_xSi (4.9eV) gates. Work functions of various gate electrodes on SiO_2 and HfAlON are summarized in Fig. 5.9.

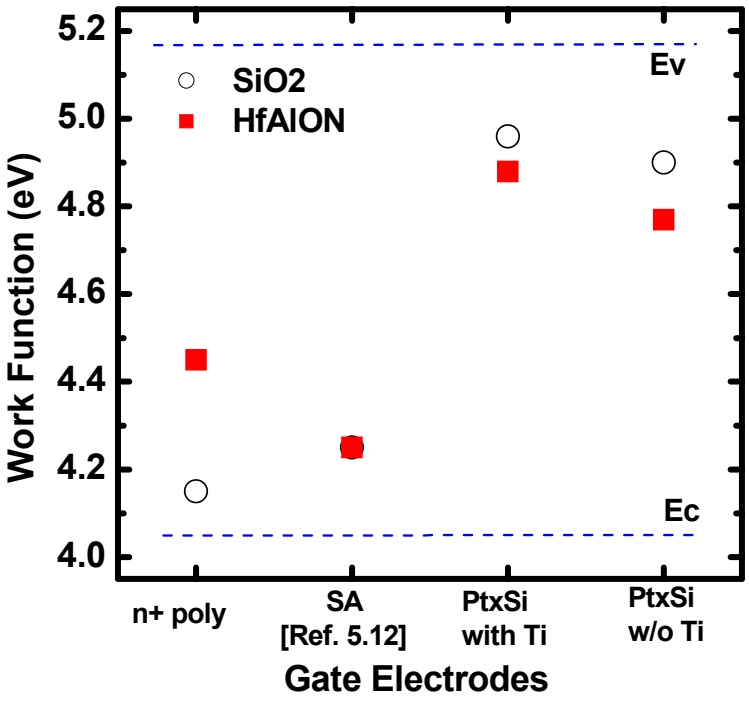

Fig. 5.9 Comparison of effective work functions. No pinning is observed for SA while less pinning for Pt_xSi. SA data were taken from [5.12].

Combination of SA and Pt_xSi gates is suitable for dual metal gate for bulk Si CMOS as both work functions are within or very near 0.2 eV of E_c and E_v of Si. Fig. 5.10 shows much lower gate leakage current of Pt_xSi compared to FUSI NiSi. This is attributed to higher barrier height of Pt_xSi gate. V_{FB} comparison in Fig. 5.11 shows that regardless of no pre-doping in polysilicon, Pt_xSi allows much higher positive V_{FB} shift

on high-K dielectric compared to B pre-doped FUSI NiSi and polysilicon, implying much reduced Fermi level pinning.

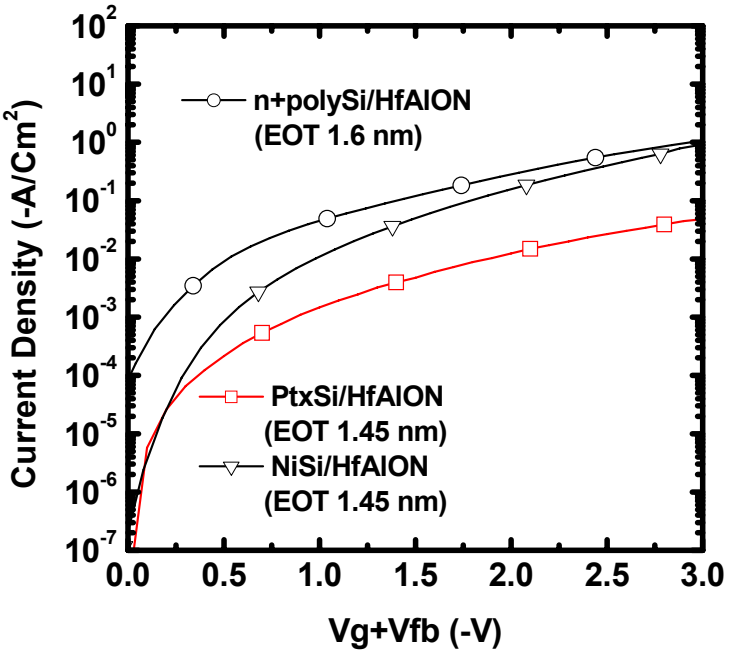

Fig. 5.10 Comparison of gate leakage current characteristics of various gates on HfAlON

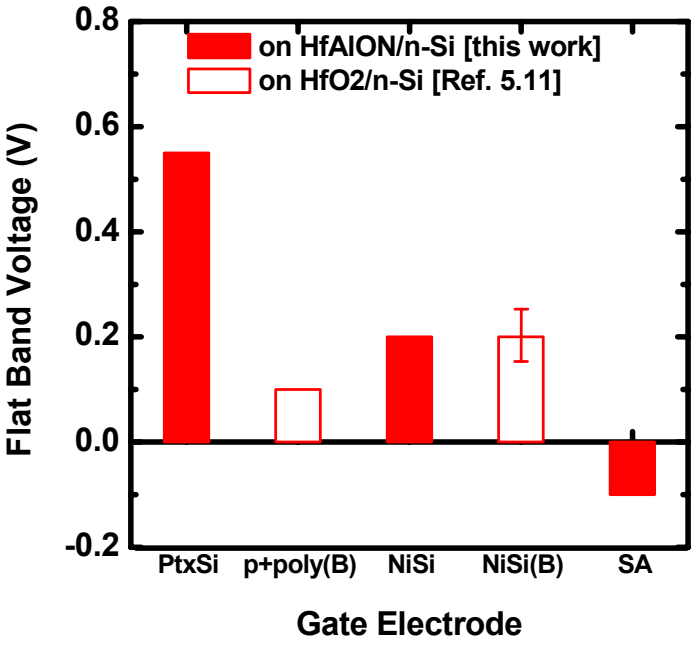

Fig. 5.11 Comparison of V_{FB} s of various gates on Hf-based high-K dielectrics. No pre-doping was used for this work while B doping was used for benchmarked data.

5.3.3 Dual metal gate integration

Fig. 5.12 shows symmetrical C-V curves of SA/HfAlON on p-Si substrate and Pt_xSi/HfAlON on n-Si substrate. The V_{fb}s of both gates were determined to be about -0.55eV and +0.55eV, suggesting low and symmetric V_{th}. Comparable gate leakage currents of both gates were also obtained as seen Fig. 5.13.

Thus, a possible process scheme of dual metal gate is suggested. Undoped polysilicon can be used in this process, and both SA and Pt_xSi gates are formed through annealing at 450°C. Ti capping is necessary for achieving a wide range of work function difference between SA and Pt_xSi because it enhances full substitution of Al for polysilicon for SA gate [5.12] and also prevents oxygen from diffusing through Pt film during annealing for Pt-silicide formation, leading to higher work function of Pt_xSi gate.

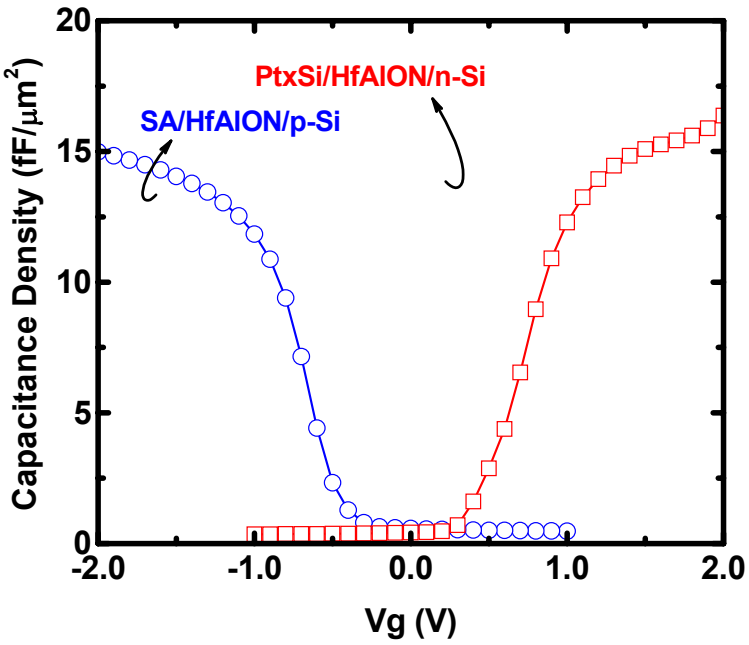

Fig. 5.12. Symmetric C-V curves of SA and Pt_xSi gated HfAlON MOS capacitors on p- and n-Si substrate, respectively. No pre-doping of polysilicon was used.

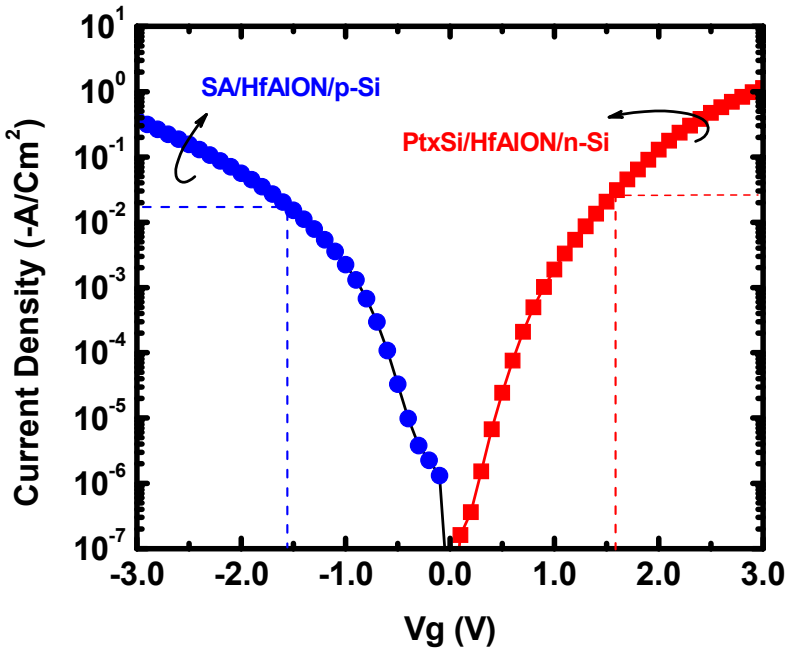

Fig. 5.13 Gate leakage currents of SA and Pt_xSi gated HfAlON MOS capacitors on p- and n-Si substrate, respectively. Both measurements were done under accumulation. No pre-doping of polysilicon was used.

5.4 Summary

For pMOSFET, Pt_xSi gate without boron pre-doping of polysilicon on high-K was demonstrated. Its work function on high-K dielectric was 4.9 eV which is suitable for pMOSFET. It also reduced Fermi level pinning, which may be due to high Pt concentration in Pt_xSi and low thermal process of Pt_xSi formation. SA and Pt_xSi with Ti capping and without pre-doping can be implemented together for complete dual metal gate CMOS process. This process enabled to achieve a wide range of work function difference (0.65 eV) and almost free Fermi level pinning for both n and pMOSFETs.

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Chapter 6

Top Surface Aluminized and Nitrided HfAlON/HfO_2 Stack using AlN/HfO_2

As an another application of using thin AlN layer, a new approach to incorporate Al and N into only top area of HfO_2 was proposed, using synthesis of ultra thin aluminum nitride (AlN) and HfO_2. The reaction of AlN with HfO_2 during subsequent annealing synthesized HfAlON near top surface of HfO_2, forming HfAlON/HfO_2 stack structure. The approach suppressed interfacial layer growth and improved thermal stability, resulted in significant improvement in leakage current, and showed no adverse effects caused by N and Al incorporation at the bottom interface.

6.1 Introduction

MOSFET devices have been aggressively scaled down to improve their performance, but corresponding reduction of device feature size is limited by some of the physical properties of the current material. The technology roadmap shows that SiO_2 will encounter soon the limitation of such a scaling because very thin SiO_2 increase tunneling current, resulting in high power consumption and degradation in reliability. HfO_2 has been evaluated to replace SiO_2 as one of gate dielectric materials since it has relatively high dielectric constant and bandgap. Since HfO_2 crystallizes even at low temperatures less than 500°C [6.1-6.3], inevitably it leads to the formation of grain boundaries to play a role of the paths for oxygen or dopants diffusion into gate dielectric, causing interfacial layer growth, threshold voltage instability and defect generation. For this reason, recently Hf-based high-K dielectrics doped with aluminum (Al) and nitrogen (N) have been proposed as promising gate dielectrics because of good thermal stability and immunity to impurity penetration [6.1-6.8]. Incorporation of N into high-K dielectric can improve thermal stability of the gate dielectric, enhancing its sufficient immunity to impurity diffusion during the subsequent thermal process [6.9, 6.10]. Nitridation of the Si surface using NH_3 prior to a deposition of high-K dielectric has been shown to be effective in achieving low EOT and preventing boron penetration [6.11, 6.12]. However, this technique results in higher interface charges [6.13], which lead to higher hysteresis and reduced channel mobility. An additional adverse effect of this NH_3 treated surface is the presence of hydrogen known to increase the electron trapping rates [6.14]. Besides, Al incorporation at the bottom interface of high-K causes degradation of the interface quality such as introduction of negative fixed charge due to Al [6.2], and mobility degradation due to the fixed-charge-induced Coulomb scattering [6.15]. In this study, a new approach to form Hafnium-Aluminum-Oxynitride (HfAlON) is demonstrated, using

synthesis of ultra thin AlN and HfO_2, in which only the top surface of HfO_2 film is aluminized and nitrided.

6.2 Experiment

Figures 6.1 and 6.2 show the basic idea of the proposed process and corresponding TEM images. The results clearly demonstrate that HfAlON on top of HfO_2 is successfully formed. AlN is completely consumed by the reaction with HfO_2 during RTA at 950^{o}C. HfAlON layer is in amorphous state even after 950°C RTA. The thin HfO_2 near the bottom interface remains unreacted, indicating that Al and N are incorporated only at the top portion of HfO_2 film. The HfO_2 layer near the bottom is crystallized. Thickness reduction of high-K due to densification during annealing also can be seen in the TEM images.

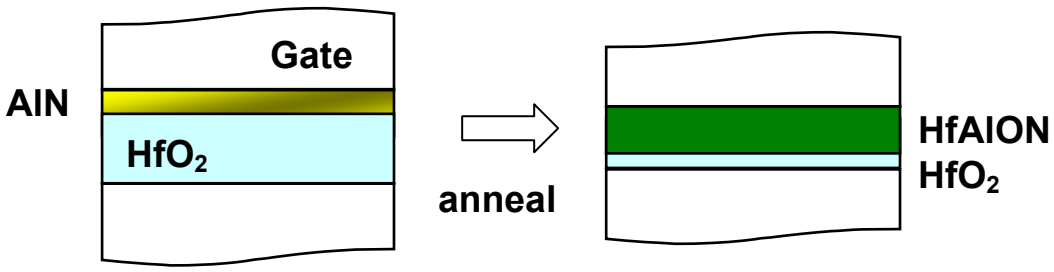

Fig. 6.1. Schematic diagram of process flow for top located HfAlON formation on HfO_2 using synthesis of AlN/HfO_2.

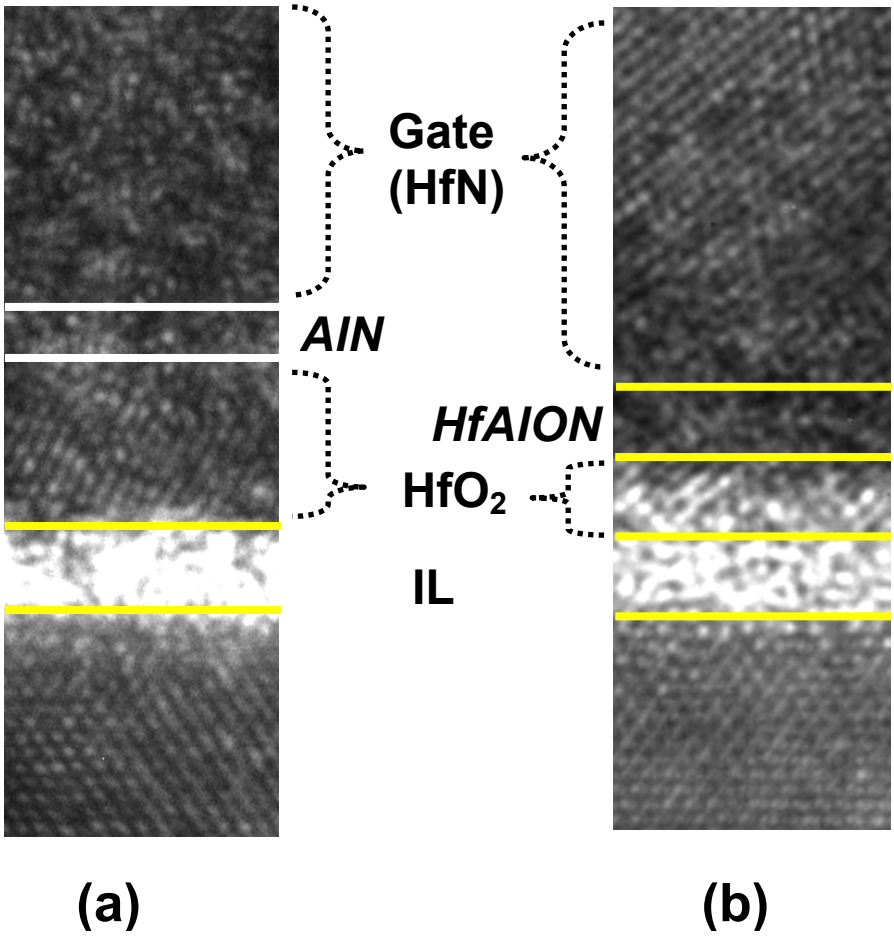

Fig. 6.2. (a) XTEM images of HfN/AlN/HfO_2 stack as–deposited and after RTA at 950^{o}C. (b) High frequency C-V curves of HfO_2 and AlN/HfO_2 MOS capacitors before and after RTA at 950°C. For HfO_2 MOS capacitor, PDA was done at 700°C for 1 min immediately after HfO_2 deposition. For AlN/HfO_2 stack capacitor, PDA was skipped after HfO_2 deposition. The area of capacitors is 50 × 50 μm^2.

The MOS capacitors with HfO_2 gate dielectric were fabricated on (100) p-type silicon substrates. The HfO_2 dielectric films were deposited on the silicon substrates by metalorganic chemical vapor deposition (MOCVD) using t-butoxy hafnium precursor at 400°C right after pre-gate cleaning is done. For the pure HfO_2, post deposition anneal (PDA) is done, prior to metal gate formation, at 700°C for 1 min at 200 Torr in a N_2 ambient. However, for the samples with AlN, no annealing is done before AlN and metal gate deposition. Thin AlN film with a thickness range of 1 ~ 2 nm is deposited on top of HfO_2 film using reactive sputtering. The same sputtering condition as discussed in the experiment section of Chapter 2 was used for AlN deposition. The ratio of Al to N in the as-deposited AlN film was also estimated to be about 1.0 as also described in Chapter 2, which was obtained in the range of 16% to 35% of $N_2/(N_2+Ar)$ flow rate ratio for sputtering, indicating wide range of process window. HfN/TaN stack and n^+ polysilicon were used for the gate electrode. For n^+ polysilicon, *in-situ* phosphorous doped amorphous silicon was deposited. The synthesis of AlN and HfO_2 was made through RTA at 950°C for 30s, which was required for S/D annealing. Finally, post metallization annealing was done in a forming gas ambient at 420°C. For comparison, both HfAlO prepared by single cocktail source MOCVD [6.3] and HfAlON by NH_3 thermal nitridation of HfAlO were also prepared.

6.3 Results and Discussion

6.3.1 Feasibility of AlN consumption

AlN is one of dielectric materials and its dielectric constant has been known to be around 9 ~ 10 [6.20], which was also similar to the value obtained in the previous experiment as shown in Chapter 2. Therefore, the AlN sputtered on top of HfO_2 initially exists as a dielectric, reducing the total capacitance of dielectric. However, if it is fully reacted with HfO_2 during subsequent annealing, the capacitance of MOS capacitor will be changed, causing the variation of final EOT. Firstly, it is investigated how the thin AlN introduced onto the top of HfO_2 affects HfO_2, which is the original dielectric. As seen in Fig. 6.3, EOT variation is evaluated using high frequency C-V measurements. For single HfO_2 without introducing AlN, the increase in EOT is observed due to interfacial layer (IL) growth after RTA at 950°C. For AlN on HfO_2 before RTA at 950°C, EOT becomes larger because the AlN is a dielectric layer. However, after RTA, the EOT is reduced back to that of HfO_2 before RTA. The final EOT of synthesized HfAlON/HfO_2 stack is thinner than that of conventional HfO_2 even though additional AlN layer is added. This indicates that when AlN is used, the IL growth during RTA is negligible due to the excellent oxygen barrier property of AlN. Interestingly, it is also observed that for both 1 nm and 2 nm of AlN films on HfO_2, the final EOTs are almost identical. This shows that AlN film of up to 2 nm thickness is completely consumed through RTA at 950°C. The sequence of PDA, AlN and HfN depositions, and RTA also affects the final EOT, because the final EOT is the result of competing processes between IL growth and HfO_2 densification. The thinnest EOT is achieved when PDA is skipped and RTA is done after deposition of both AlN and HfN layers. In this case, the IL growth is negligible because of double diffusion barriers (both AlN and HfN), and only densification is reflected to the final EOT change.

HfN is chemically and thermally a very stable material [6.19]. However, HfO_2 is much easier to have reaction with aluminum and nitrogen. TEM figure does not show any change at the bottom of electrode. Additionally, if the AlN is reacted with HfN electrode instead of reacting with HfO_2, the work function of electrode must be changed, resulting in V_{fb} shift too. However, no so significant change in V_{fb} was observed. If AlN reacts with HfN and if no change in HfO_2, there will be no reason for such a great improvement in leakage current for thinner EOT.

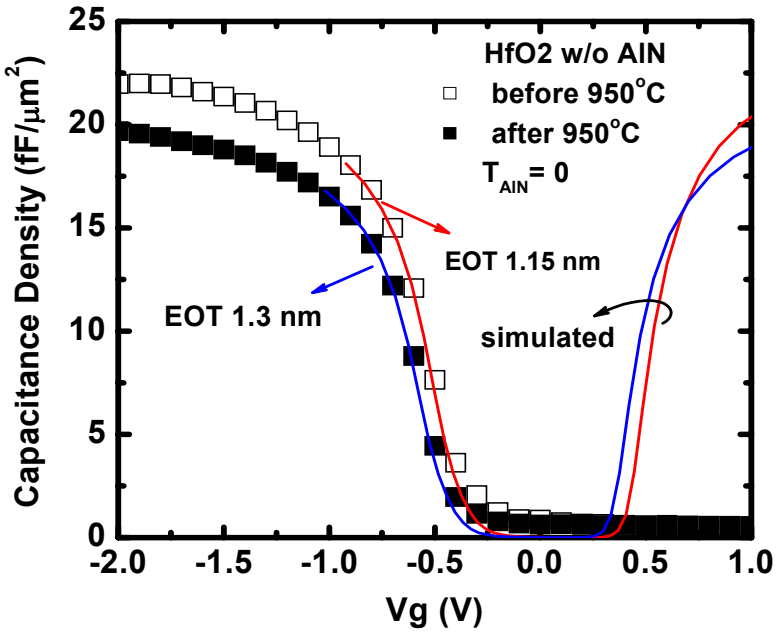

Fig. 6.3 High frequency C-V curves of HfO_2 MOS capacitor. PDA was done at 700 °C for 1 min right after HfO_2 deposition. No AlN was deposited on top of HfO_2. Increase in EOT due to IL growth is observed.

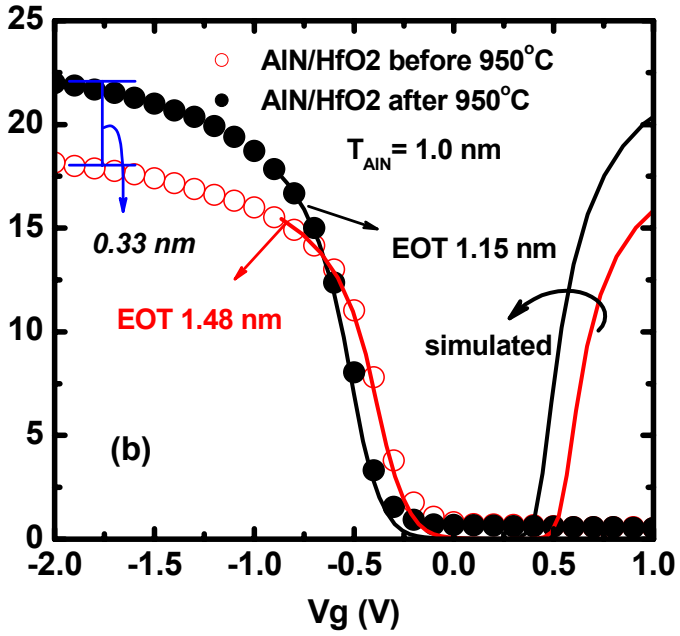

Fig. 6.4 High frequency C-V curves of AlN(1.0 nm)/HfO_2 MOS capacitors.

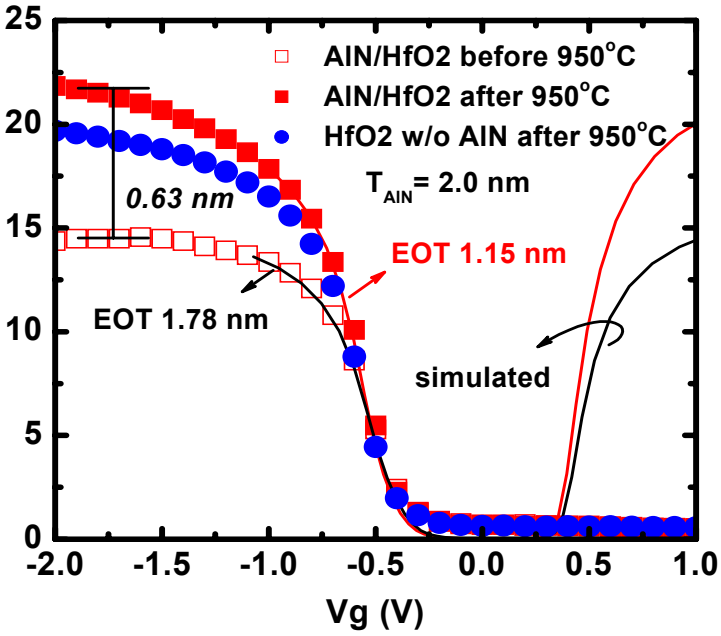

Fig. 6.5 C-V curves of AlN(2.0 nm)/HfO_2. PDA was skipped after HfO_2 deposition. Final EOTs of synthesized HfAlON/HfO_2 stacks are identical regardless of initial AlN thickness, indicating complete consumption of AlN during RTA. It is observed that final EOT of synthesized HfAlON/HfO_2 stack is thinner than that of conventional HfO_2 even though the additional layer AlN is added.

6.3.2 EOT reduction by AlN

As seen in Fig. 6.4, the final EOT of synthesized HfAlON/HfO_2 stack is thinner than that of conventional HfO_2 even though additional layer AlN was added. This indicates that when AlN is used, the IL growth during RTA is negligible due to the excellent oxygen barrier property of AlN [6.21]. The sequence of PDA, AlN and HfN depositions, and RTA also affects the final EOT as observed in Fig. 6.6, because the final EOT is the result of competing process between IL growth and HfO_2 densification. The thinnest EOT is found when PDA is skipped and RTA is done after deposition of both AlN and HfN layers. In this case, the IL growth is negligible because of double diffusion barriers (both AlN and HfN) and only densification is reflected to the final EOT change. Additionally, the change of thickness monitored using Spectroscopy Elliposmeter as shown in Fig. 6.7 shows that the optical thickness of HfO_2 is reduced after PDA, confirming its densification.

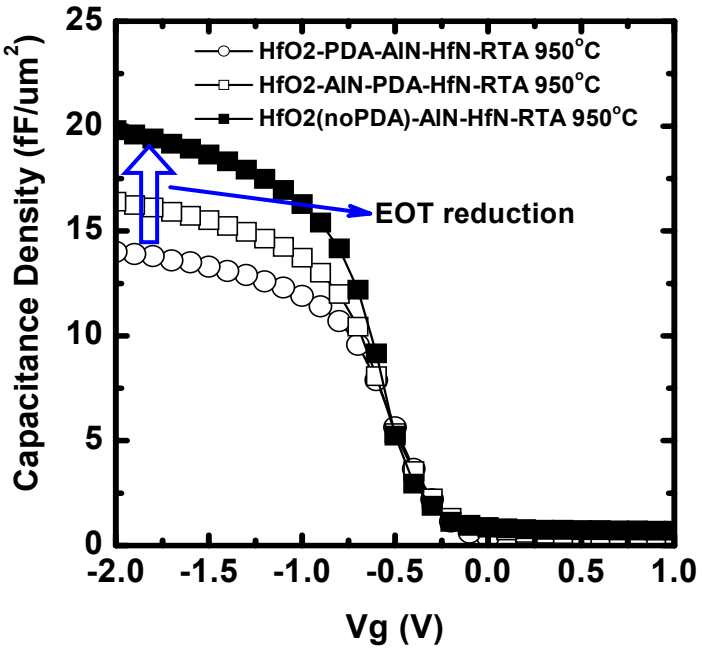

Fig. 6.6 EOT reduction is found when AlN is used. The amount of EOT reduction depends of the process sequence. Thicker HfO_2 (4.8 nm) is used in this case.

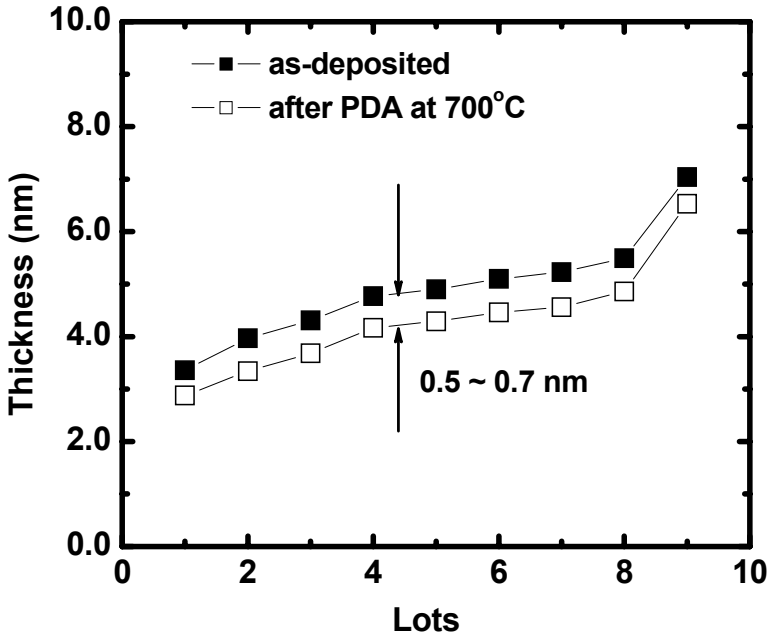

Fig. 6.7 The change in thickness of HfO2 on silicon substrate between before and after PDA. Thickness of HfO2 films was measured by Spectroscopy Ellipsometer. For all the HfO2 films, PDA was done at 700C in a N2 ambient for 1 min.

6.3.3 Chemical composition of synthesized layer

In order to verify Al and N incorporation in the synthesized film, XPS and SIMS analysis were made. Figure 6.8 shows the XPS spectra of Al 2*p* and Hf 4*f* obtained from various films. The spectra of MOCVD HfAlO and HfAlON obtained by NH_3 annealing of HfAlO were also investigated in order to compare with those of synthesized HfAlON. As-deposited AlN/HfO_2 stack shows the Al-N bonding due to AlN on top of HfO_2. After RTA, Al-N peak intensity is slightly attenuated and the peak has shifted towards Al-O peak. The Hf 4*f* peak does not shift much even after RTA. It is attributed to the fact that the shift to a higher binding energy caused by annealing and densification of as-deposited HfO_2 compensates the shift to a lower binding energy caused by the Hf-N bond formation in HfO_2. As for the shift of Hf 4f peak, there can be two mechanisms to make the shift of the peak. Annealing and densification of as-deposited HfO_2 causes a shift to a higher binding energy. This has been confirmed at both MOCVD and sputtered HfO_2 [6.6, 6.7], as also can be seen in comparison between before and after PDA in Fig. 6.8. Introduction of Hf-N bond in HfO_2 makes a shift to a lower binding energy [6.18]. For the AlN/HfO_2 sample which PDA as well as RTA does not undergo, the HfO_2 in AlN/HfO_2 is the same as as-deposited HfO_2. This may explain the finding that the AlN/HfO_2 had a similar binding energy as the HfO_2 without PDA, as seen in Fig. 6.8. After RTA, if there is no AlN, it should shift to higher energy. However, it still remains at lower energy of Hf peak because of the formation of Hf-N bond during RTA. Fig. 6.9 shows N profiles before and after RTA.

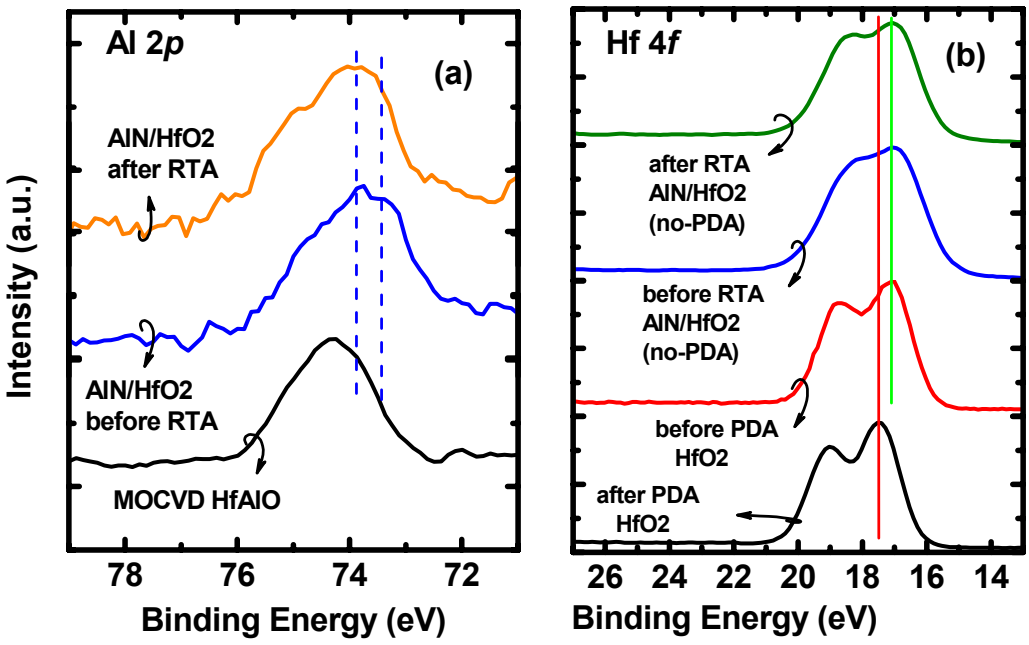

Fig. 6.8 XPS spectra on various films; (a) Al 2*p* peaks are observed near 74.3 eV (Al-O) and 73.8 eV (Al-N). (b) The shift of Hf 4*f* peak is observed after RTA, which is attributed to N incorporation. For AlN/HfO_2 stack, no PDA was done prior to AlN deposition. The annealing was done without HfN gate for XPS measurement.

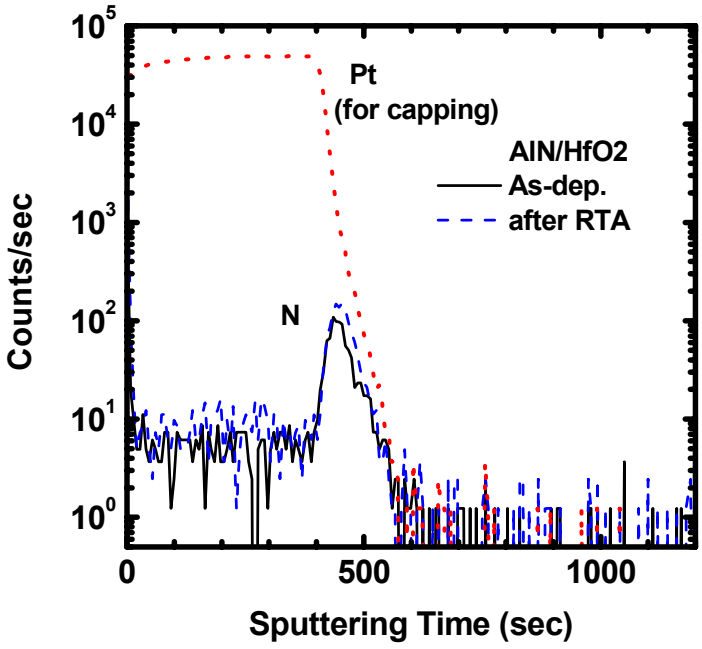

Fig. 6.9 Nitrogen profile obtained from SIMS analysis. For the SIMS measurement, a platinum layer is used as a capping layer instead of HfN gate for better contrast of N profile.

6.3.4 Flat-band voltage shift

Degradation in hysteresis due to N incorporation [6.18], which is usually found in N-incorporated HfO_2 is not found in the synthesized HfAlON/HfO_2 stack. The hysteresis of the synthesized HfAlON/HfO_2 stack with an EOT of 1.15nm is measured to be about 18 mV, under the sweep range of -2.0 to +1.0 V as shown in Fig. 6.10. This is significantly lower compared to the typical range of hysteresis (~ 200 mV) for HfO_2 with nitrogen incorporation at the bottom interface, measured under the similar sweep range [6.24]. Fig. 6.11 also shows that the synthesis process does not change V_{fb}, indicating that the high-K at the bottom interface is still HfO_2. However, MOCVD HfAlO shows positive V_{fb} shift due to the negative fixed charge induced by Al, and HfO_2 with surface nitridation shows negative V_{fb} shift due to enhanced positive charges induced by N.

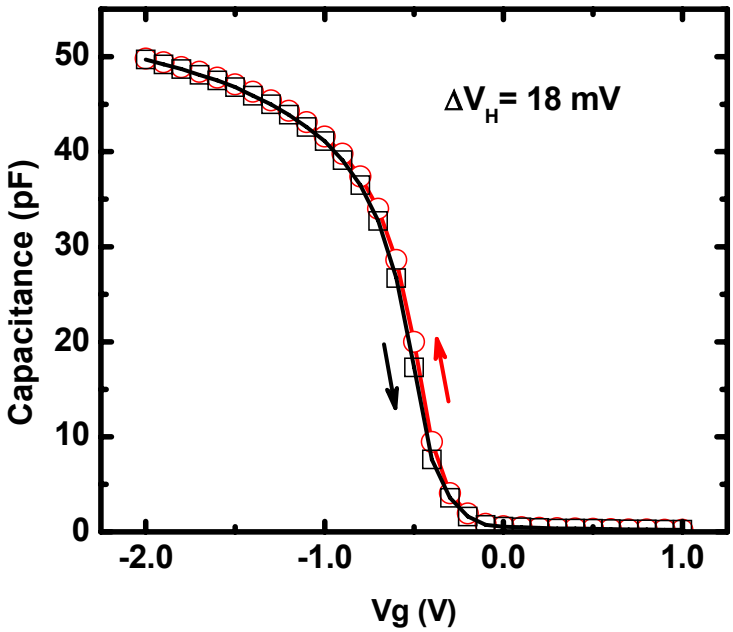

Fig. 6.10 The hysteresis of the synthesized HfAlON/HfO_2 stack MOS capacitor after 950°C RTA.

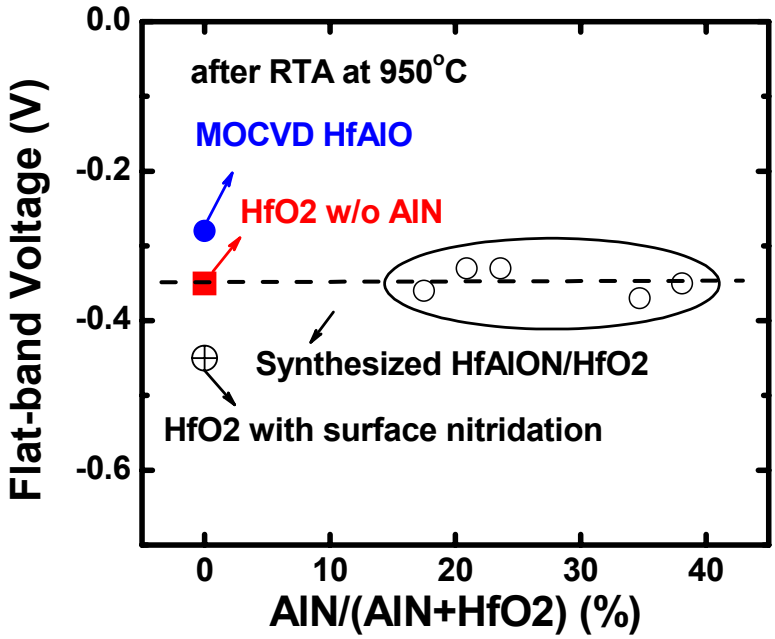

Fig. 6.11 The flat-band voltage with various AlN/(AlN+HfO_2). HfAlO shows positive V_{fb} shift due to Al at the interface while the surface nitrided HfO_2 shows negative V_{fb} shift due to increased fixed charge. The HfAlON/HfO_2 shows no change in V_{fb}.

Al incorporation from the top surface is also evidenced by Angle Resolved XPS results as shown in Fig. 6.12, which confirm that most of Al atoms exist near top surface of HfO_2 after RTA. Al is almost uniformly distributed throughout the HfAlO film whereas for synthesized HfAlON/HfO_2 stack, the Al concentration is decreasing with the increase of the tilt of angle. This suggests that most of Al exist near the top of HfO_2.

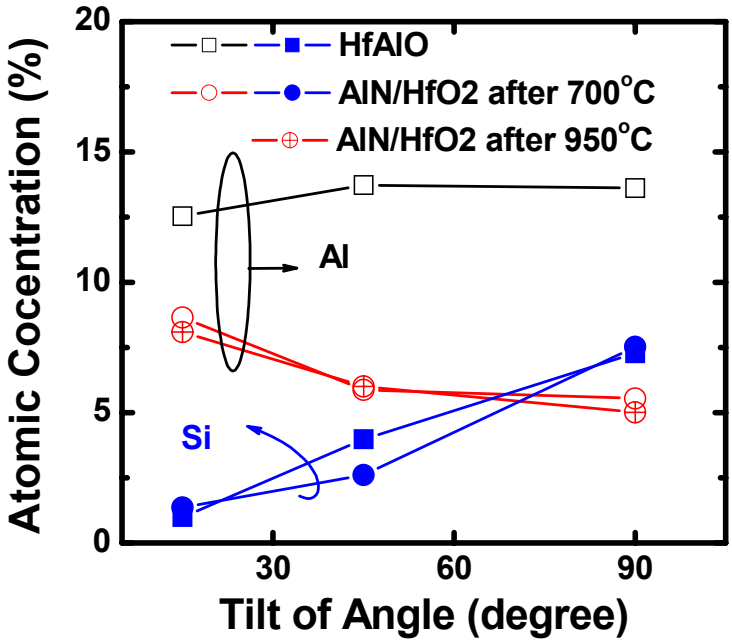

Fig. 6.12 Al and Si atomic concentration of HfAlON/HfO_2 stack obtained by Angle Resolved XPS. Most of Al atoms exist near top surface of HfO_2 after RTA. For the AlN/HfO_2 stack films, Al concentration becomes lower while for HfAlO it is not much changed with angle.

6.3.5 Gate leakage current characteristics

Figure 6.13 shows a significant improvement in gate leakage current for synthesized HfAlON/HfO_2 stacks, compared to conventional HfO_2 + PDA process. It is attributed to improved thermal stability and film quality by incorporation of Al and N [6.1-6.6]. For the synthesized HfAlON/HfO_2 stack formed on top of HfO_2 that PDA is skipped, more than 3 order reduction of leakage current is achieved. However, once PDA is done prior to AlN deposition, the leakage current improvement is less because the HfO_2 is already partially crystallized during PDA. Fig. 6.14 shows gate leakage current characteristics of synthesized HfAlON/HfO_2 stack formed using AlN(1.0~2.0nm)/thin-HfO_2. Excellent gate leakage characteristics are achieved and confirmed with benchmarked data as shown in Fig. 6.15.

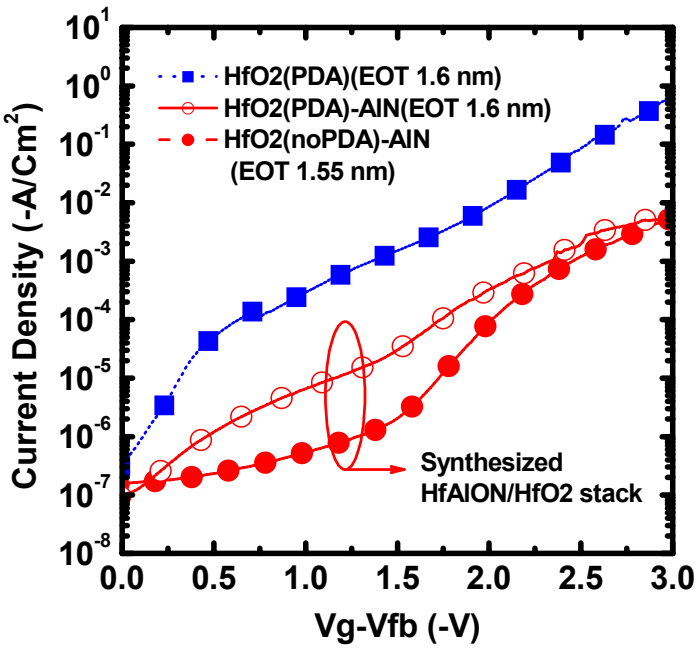

Fig. 6.13 Leakage current characteristics of synthesized HfAlON/HfO_2 stack formed using AlN(1.0nm)/thick-HfO_2. For the synthesized HfAlON/HfO_2 stack samples, PDA was skipped. For all the samples, RTA at 950°C for 30s was conducted.

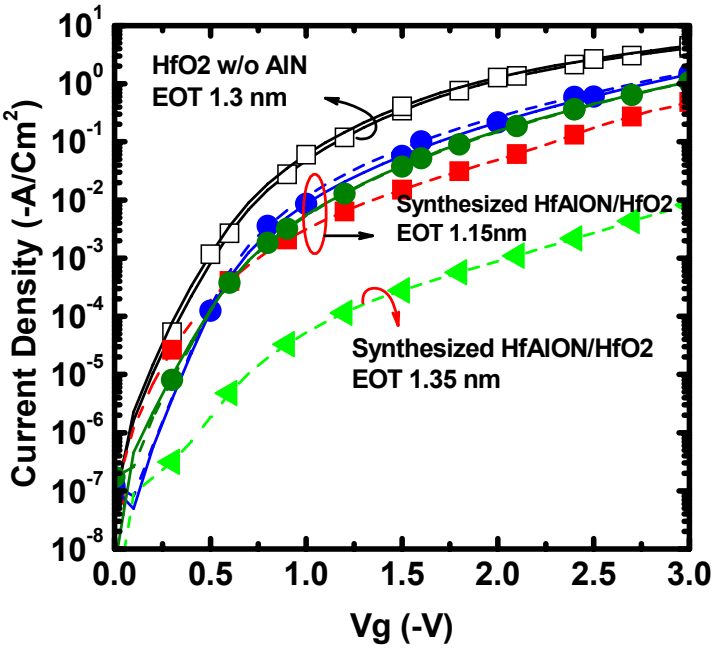

Fig. 6.14 Leakage current characteristics of synthesized HfAlON/HfO_2 stack formed using AlN(1.0~2.0nm)/thin-HfO_2. For the synthesized HfAlON/HfO_2 stack samples, PDA was skipped. For all the samples, RTA at 950°C for 30s was conducted.

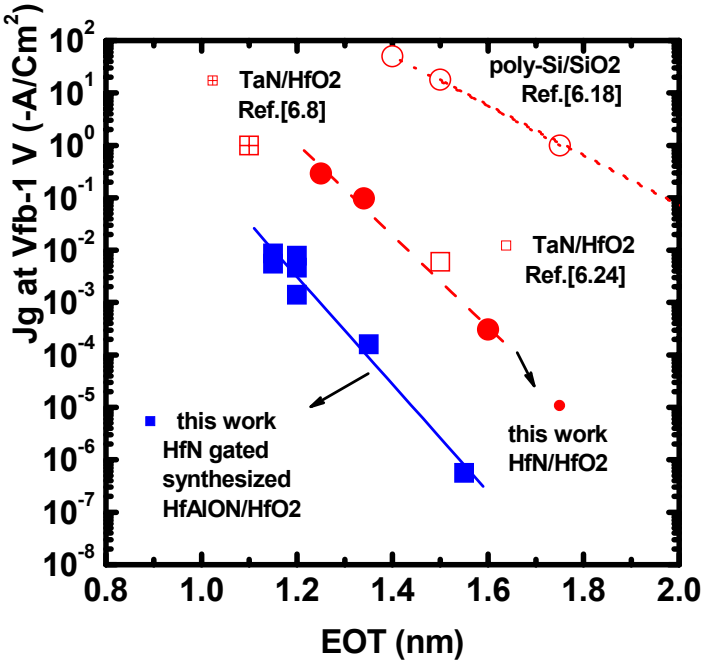

Fig. 6.15 EOT versus leakage current. the HfAlON/HfO_2 stack show significantly improved leakage current, compared to conventional HfO_2 + PDA process

6.3.6 Improved mobility

Compared to HfO_2 with surface nitridation, improved mobility is obtained for n-MOSFET with synthesized HfAlON/HfO_2 stack, due to less fixed charge at the interface compared to HfO_2 with surface nitridation, as shown in Fig. 6.16. It may also support that Al and N is incorporated on the top area of HfO_2 and do not go down to bottom interface.

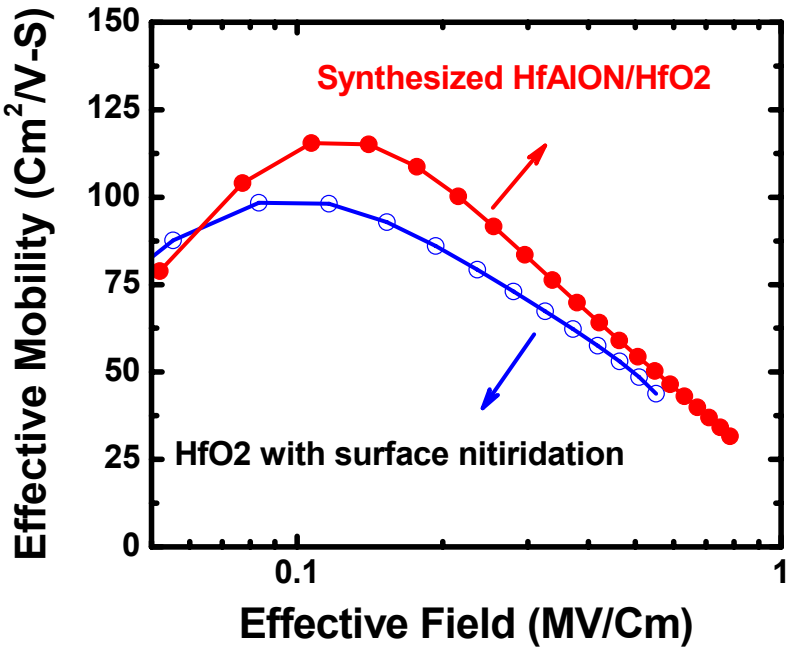

Fig. 6.16 Comparison of effective electron mobility of HfAlON/HfO_2 stack sand HfO_2 with surface nitridation. For both nMOSFETs, EOT is 1.15 nm.

6.4 Summary

In this chapter, HfAlON/HfO_2 stack high-K gate dielectric using the synthesis of AlN/HfO_2 was demonstrated. Through the subsequent high temperature annealing (RTA at 950°C, 30s), thin AlN on top of HfO2 was reacted with HfO_2 and consumed completely, resulted in HfAlON on the surface of HfO_2. The introduction of AlN suppressed additional interfacial layer growth. There was no significant change in the flat-band voltage between single HfO_2 and synthesized HfAlON/HfO_2 stack. The top incorporation of Al and N on the surface only of HfO_2 improved thermal stability, resulting in the improvement of leakage current and mobility. This work should be interesting to the semiconductor industry as this approach can be easily implemented. However, one drawback can be that this approach may increase the process complexity since additional dielectric layer deposition step is required.

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Chapter 7

Conclusion

7.1 Approaches for integration of dual metal gates

7.1.1 AlN Buffer Layer

A novel way for integration of dual metal gates using a conventional wet etching process was demonstrated. The use of a very thin aluminum nitride (AlN) buffer layer was a key for demonstration of this method. This buffer layer prevented the gate oxide from being exposed to a metal etching process and was completely consumed through the reaction with metal gate during subsequent annealing. This study suggests that the use of buffer layer is also an effective method for tuning work functions of two metal gates as about 4.4 and 4.9 eV of work functions were obtained. However, although an integration of dual metal gates can be done using a thin AlN buffer layer, it may not be suitable for highly scaled devices because it will be difficult to define a narrow gate line width using wet etching process. Defining of gate pattern by wet etching can cause the degradation of the gate pattern due to isotropic etching property of wet chemical solution. In addition, new alloy gates formed through the reaction of AlN and gate metals have to follow the gate last process flow for CMOS device fabrication because these alloy gates may be thermally stable up to 750°C. Since these experiments were carried out with SiO_2 gate dielectric only, a similar experiment should be done with high-K dielectric.

Nonetheless, as the work functions of the original gate metals are modified as a result of their reaction with AlN, this approach would be still attractive for engineering the work function for dual metal gate process.

7.1.2 Fully Silicided Hf-Silicide

Fully silicided Hf-silicide as a metal gate material for n-MOSFETs was demonstrated as a FUSI process. The range of work function of the HfSi gate was estimated to be between 4.25 and 4.8 eV. Full silicidation and no polysilicon depletion were observed from the C-V curve of Hf-silicide gate nMOSFET. Hf-silicide gate was also excellent in terms of its thermal stability. A higher work function, which is needed for pMOSFET was not obtained for HfSi gate although about 4.85 eV of work function was achieved by boron pre-doping. Since the work function of Hf is very low, it may be difficult to achieve a higher work function. Thus, to integrate dual metal gates of bulk CMOS using FUSI HfSi, a FUSI gate using another metal that has a higher work function may be needed. However, this will make it even harder to integrate dual metal gates as another metal deposition process needs to be added to device fabrication. In addition, full silicidation may lead to the volume expansion of gate electrode because silicidation indicates incorporation of metal into silicon. On a specific structure which is required for formation of FUSI gate, this volume expansion not only forms an unnecessary and ugly silicide layer on top of the gate but also induces a stress on gate dielectric. This stress may degrade the electrical property of gate dielectric. Therefore, it should be verified whether there is any stress induced by silicidation and if silicidation induces stress on the gate dielectric, the effect of the electrical property of FUSI gate on this stress should be investigated. This study suggests that FUSI HfSi gate is better than FUSI NiSi gate as a wider range of work function can be obtained using FUSI HfSi. It

may be applicable for FDSOI MOSFET and thin-body MOSFET that need about 0.4 eV of work function difference between n and pMOSFETs. Further study on FUSI gate with high-K dielectric is also recommended for future application because high-K dielectric will replace current gate dielectric.

7.1.3 Substituted Al (SA) for nMOSFET

As an alternative way of forming a metal gate with a low work function, substituted Al (SA) gate was proposed and demonstrated. This can provide a practical solution for achieving a low work function on a high-K dielectric. The SA process was free from thermal instability related issues as it was implemented after all the high temperature processes were completed. The work function of substituted Al gate was determined to be about 0.25 eV. This value was identical no matter what the dielectric film was, suggesting that Fermi level pinning is eliminated. Fermi level pinning may occur due to Hf-Si bond at the interface. In this case, a reason why Fermi level pinning is eliminated is that Si elements are completely removed from the interface between substituted Al and HfAlON through the full substitution of Al for polysilicon. The work function of substituted Al gate was low enough for nMOSFET but it was not affected by pre-doping of polysilicon. Therefore, another metal which can be substituted for polysilicon and has a higher work function for pMOSFET is required for CMOS device. The fact that substituted Al gate can eliminate Fermi level pinning is very interesting and of considerable importance because it has been reported that Fermi level pinning leads to Vth instability. However, how the pinning problem was solved by Al substitution was not clearly understood. A systematic study for investigating the cause of the elimination of Fermi level pinning is recommended for future research. Further study on Fermi level pinning problem and its cause will offer a practical solution for V_{th} instability issue.

7.1.4 Pt-rich Pt_xSi Gate for pMOSFET

Substituted Al (SA) gate using undoped polysilicon had a work function, which is suitable for nMOSFET, and the SA gate on high-K dielectric did not have Fermi level pinning problems. However, similar approach for pMOSFET without boron pre-doping of polysilicon on high-K has not been known yet. Hence, for pMOSFET, fully silicided Pt-rich Pt_xSi gate was demonstrated. Although Pt was not substituted when it is in contact with polysilicon, it had a similar effect of substitution when Pt concentration was high enough in platinum silicide (Pt_xSi). The work function of Pt_xSi gate on HfAlON high-K dielectric was determined to be about 4.9 eV, which was very close to the work function determined on SiO_2 gate dielectric. This suggested much reduced Fermi level pinning though the pinning was not fully eliminated. The reduced Fermi level pinning was probably due to two factors; less Si at the interface of HfAlON and Pt_xSi and no interfacial reaction of HfAlON and Pt_xSi because no further high temperature process was undergone. Ti capping layer on the top of Pt film was very useful in this process because it prevented oxygen from diffusing into Pt and Pt_xSi gate, resulted in high concentration of Pt in Pt_xSi. In addition, Pt_xSi gate did not show a dependence of pre-doping on its work function. This may provide a practical solution for achieving a high work function on a high-K dielectric. Without pre-doping of polysilicon, this Ti/Pt process can be used together with SA process for complete dual metal gate CMOS process.

7.2 A proposal for integration of dual metal gates with high-K dielectric.

For bulk CMOS devices, the work functions of metals for integrating dual gate should be within 0.2 eV of the E_C and E_V of Si for n and pMOSFET, respectively. [7.1]. However, a promising way of dual metal gate process on high-K dielectric, which should have a wide range of work function and must not have the Fermi level pinning problem, has not been identified yet. Although FUSI process has a potential capability of work function modulation using pre-doping of polysilicon, pre-doping in polysilicon on high-K dielectric may cause excessive leakage current and dopant penetration problem [7.2 – 7.4]. In addition, the Fermi level pinning on high-K dielectric has not been solved through FUSI process [7.5, 7.6].

On the basis of the results demonstrated, a possible process scheme of dual metal gate is presented as described in Fig. 7.1. Undoped polysilicon is used in this process, as pre-doping does not affect the gate work function. Both SA and Pt_xSi gates are formed through annealing at 450°C. Ti capping is done to achieve free or less Si at the interface of SA (or Pt_xSi) and high-K dielectric, leading to a wide range of work function and free (or reduced) Fermi level pinning.

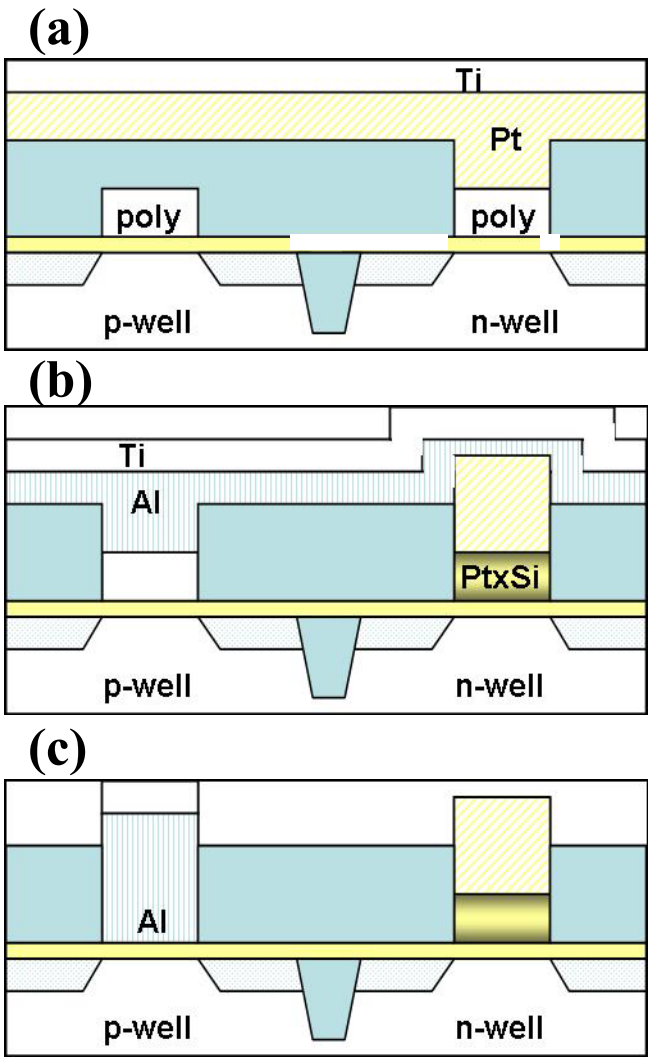

Fig. 7.1 Proposed process scheme for dual metal gate integration using SA and Pt_xSi for nMOSFET and pMOSET.

7.3 HfAlON/HfO_2 stack for advanced high-K dielectric

HfAlON high-K gate dielectric using the synthesis of AlN/HfO_2, which is aluminized and nitrided HfO_2 on the top of HfO_2 was demonstrated. The introduction of AlN suppressed additional interfacial layer growth, resulting in thinner EOT. Improved thermal stability and significant reduction in leakage current were achieved, without adverse effects arsing from N and Al incorporation. These results are most likely due to incorporation of N and Al near the surface of dielectric. This study suggests that top nitridation and aluminization of high-K gate dielectric can be done easily by sputtering a thin AlN layer onto gate dielectric. Since the evaluation of HfAlON/HfO_2 stack was done only with HfN gate, it is necessary to examine whether HfAlON can be formed with the conventional polysilicon gate and other metal gates. In addition, if HfAlON can be formed, it should also be investigated whether HfAlON is compatible with the polysilicon and metal gates since the polysilicon gate is used currently but will be replaced with a metal gate. This work may provide the industry with a promising way for high-K gate dielectric not only because of good electrical property of HfAlON but also because of easy implementation for top surface nitridation.

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