LOW NOISE AMPLIFIER DESIGN AND NOISE CANCELLATION FOR WIRELESS HEARING AIDS

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NATIONAL UNIVERSITY OF SINGAPORE

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Summary

Wireless technology is one of the most promising approaches for future hearing aids research. Compared to the conventional hearing aids, wireless hearing aids provide a clearer voice, longer operation time, easy communication with other audio devices, and so on. Although the advantages of the wireless hearing aids, noise cancellation and power consumption are still the key issues in research, which require more efficient noise cancellation method and lower power consumption circuit design.

Receiving the processed audio signal within the power budget of the wireless hearing aid earpiece is one of the inherent design challenges. Low noise amplifier (LNA) is the first stage to receive the signal, which is embedded in the earpiece of a wireless hearing aid. There has been not much attempts to implement a CMOS receiver for the earpiece of wireless hearing aid systems. As an attempt towards its CMOS implementation, an integrated single-ended CMOS LNA with inductive degeneration at the source is presented. The power consumption is the key issue to concern in this design. Because the earpiece and the body unit for hearing aid device are separated within about one meter, the noise figure and gain is not as important as power consumption. With the small power consumption, the LNA should have good linearity also. According to the normal hearing aid battery capacity, the total power consumption of an earpiece, where receiver is the most power hungry block, should be as low as possible but below 3.0 mW [1]. The recently reported 0.9 GHz CMOS receiver consumes 2.2 mW, out of which LNA alone consumes 1.44 mW [2]. Reducing LNA power consumption will extend the battery life. A single ended low voltage and low power LNA was implemented in CSM 0.18 μm

CMOS technology. The LNA is powered at 1.0 V supply and drains only 0.95 mA. The LNA provides a forward gain of 11.91 dB with a noise figure of only 2.41 dB operating in the 0.9 GHz band. The IIP3 is 0.7 dBm and the P1dB is -12 dBm. The proposed design also meets requirements on noise, linearity and gain for 0.9 GHz low power applications, specifically suitable for CMOS wireless hearing aids.

Another consideration in this research work is about canceling the environmental noise. Normally, an input to hearing aids is often associated with the environmental noise. For instance, due to the environmental noise, a hearing-impaired person not only feels severe hearing loss but also is unable to perceive desired speech from the noisy environment. Thus, the noise cancellation is a primary concern, particularly for hearing impaired. In this thesis, a modified two-element beamforming method for noise cancellation is introduced, which helps reduce the surrounding environment noise. This method needs to be verified before physical implementation. So, the behavior model for this method is also presented, which shows a better noise cancellation performance. In addition, the whole wireless hearing aid system is simulated using the proposed noise canceling model. The simulation satisfies the proposed method.

Nomenclatures

ADC: Analog-to-Digital Converter

ADS: Advance Design System

BSIM: Berkeley Short-channel IGFET Model

BSIM3: third generation BSIM

CAD: Computer Aided Design

CIC: Completely In Canal hearing aid

CMOS: Complimentary Metal Oxide Semiconductor

CSM: Charted Semiconductor Manufacturer

DC: Direct Current

DAC: Digital-to-Analog Converter

DRC: Design Rule Check

DSP: Digital Signal Processing

DUT: Device Under Test

EDA: Electronics Design Automation

HA: Hearing Aid

IEEE: Institute of Electrical and Electronic Engineer

IIP3: Input-referred third-order Intercept Point

IME: Institute of Microelectronics, Singapore

ITC: In The Canal hearing aid

LNA: Low Noise Amplifier

LPLV: Low Power consumption Low Voltage

MIM: Metal Insulator Metal

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor

NF: Noise Figure

NMOSFET: Negative Channel MOSFET

NQS: Non-Quasi-Static

PMOSFET: Positive Channel MOSFET

P1dB: 1 dB compressor Point

QPFSK: Quadrature Phase-Shift Keying

RF: Radio Frequency

SMA: SubMiniature version A

SNR: Signal to Noise Ratio

SPICE: Simulation Program for Integrated Circuits Emphasis

SPL: Sound Pressure Level

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Chapter 1 Introduction

1.1 Introduction

Keeping in view the global population of hearing impaired people in the world, there is a huge market demand on hearing aid devices. Thanks to the microelectronics development, it attracts more and more the interest of industries attempting to exploit the micro-technologies for hearing aids devices [3].

A hearing aid is an electronic, battery-operated device that amplifies and changes sound to allow for improved communication. Hearing aids receive sound through a microphone, which then converts the sound waves into electrical signals. The amplifier increases the loudness of the signals and then sends the sound to the ear through a speaker. Every conventional electrical hearing aid has mainly three parts [4] :

(1) A microphone used to collect the sound and convert into electrical impulses. Thus, reproduces the rise and fall of pitch of the sound (high or low) and the intensity (loudness measured in decibels).

(2) An amplifier, modulates the electrical impulses, makes sounds louder. It has an integrated circuit comprising of several transistors or a combination of integrated circuits.

(3) A speaker (earphone) converts the amplified signal into sounds and feeds them into the ear.

Hearing aids have been developed for a long time since the year 1800 [4], [5]. The Greeks used shells and Romans had bronze funnels, but it was only in the 1800's that the first ear horns or trumpets were developed. In 1800's London F C Rein company

established itself as the first company to manufacture hearing aids on a commercial basis. In 1892 the first hearing aid, a carbon hearing aid, was produced at the Pilitzer Clinic in Vienna. It consists of an earphone connected to a carbon microphone fastened onto a battery box. Alexander Graham Bell is also credited as the first to build an earphone which amplifies sound for the hearing impaired. In 1901 the first commercial aid was the Akoulallion 1899, but this carbon ball invented in 1901 led to an increase in the quality and reliability of electrical hearing aids. An electrical hearing aid was used by the English Queen Alexandra for her coronation of 1902. In 1934, the first vacuum tube aid was developed in England, consisting of a microphone, an earphone, an amplifier and two batteries. Vacuum tube technology rapidly became the hearing aid standard. However, the new vacuum aid requires two large batteries which usually last one day only. The transistor was invented by Bell laboratories in 1947 and in 1953 transistor hearing instruments were fabricated to make them smaller, cheaper and more effective. The transistors allow behind-the-ear aids to develop. Other head worn aids are often attached to hair with a clip. In 1970 hybrid hearing aids combined both digital and analog circuitry. These were the first to include a digital chip and were a fraction of the size of previous hearing aids. Leading up to the 70's, behind the ear aids (BTE) almost fit behind the ear. In-the-ear aids (ITE) became popular in the late 70's, which are more reliable and smaller. In the 1980's, the first programmable hearing aids were developed. First digital hearing aid circuits are similar to those in personal computers. Programmable aids allow user to control hearing in different situation. In 1990's the first automatic aids without volume control were made available. Moreover, the first fully digital hearing aid came out in 1997. The first completely digital CIC was also announced around the same time. The

CIC hearing aids now are smaller than ever before allowing truly “invisible” hearing for all. In 2001, with the RF technology and IC design development a kind of wireless hearing aid was invented [1]. At present, the wireless hearing aids are the research focus which would bring many advantages over the traditional hearing aids. The CMOS technology seems the most promising to provide high performance.

Hearing aid manufacturing is a highly technical and delicate task. Most of the hearing impaired persons’ hearing losses are different from each other’s hearing loss, so each hearing instrument has to be customized to match the user's exact needs. The elements which go into making a hearing aid should not be compared to a pair of spectacles, which have mass-produced frames and lenses, but are actually closer to that of a sophisticated piece of specialist hi-fi equipment. As every customer's hearing loss is unique, so every hearing aid is different. The type of hearing aid best suited to a customer depends largely on their type of hearing loss, in addition to the physical and cosmetic considerations [6]. In Fig. 1.1 a few sample of the range of styles and sizes of hearing instrument available in the market are depicted [7].

Fig. 1.1 Some conventional hearing aids

Behind the ear hearing aids (BTE) are usually cheaper, easier to adjust than other devices. It is fairly visible and usually more powerful, thus fewest number of problems with wax or infections. Completely in the canal hearing aid (CIC) cannot be seen and require tight fit. It is hard to adjust and remove. CIC aid is so small that it is invisible. However, the battery capacity is limited, so the user needs to change the battery more frequently. Behind the ear hearing aids are bigger in size than CIC aids. Hence more circuits can be built in with more functions, such as clearer voice. In the ear hearing aid (ITE) is less visible, harder to put in and adjust compared to the CIC aid. In the canal

hearing aid (ITC) is even less visible and consumes less power than ITE. As a result, hearing-impaired patients with tremor or poor eyesight are not good candidates for ITC/CIC aids. Cochlear implant hearing aids are more advanced, mostly recommended to patients with profound loss/deaf [7]. First, sound is picked up by a directional microphone and sent from the microphone to the speech processor. Then the speech processor analyzes and digitizes the sound into coded signals. Third, coded signals are sent to the transmitter via radio frequency. The transmitter sends the code across the skin to the internal implant. Fourth, the internal implant converts the code to electrical signals. The signals are sent to the electrodes to stimulate the corresponding hearing nerve fibers. Finally, the signals are recognized as sounds by the brain, thus produce a hearing sense.

Fig. 1.2 An analog hearing aid system

For simplicity, among the above mentioned hearing aids, from circuit point of view hearing aids can be categorized mainly of two kinds: (i) the conventional hearing aids and (ii) wireless hearing aids. Wireless hearing aids using wireless technology are under investigations [1]. From the circuit operation and signal processing point of view, the conventional hearing aids are generally of two types: (i) analog hearing aid (Fig. 1.2) and (ii) digital hearing aid (Fig. 1.3) [5], [7]. Analogue hearing aids use microphone to convert sounds into an electric signal which is modified in a miniature amplifier and converted back into sound by a receiver. That sound passes into the ear and is heard by

the patient. After 1996, with the rapid growth in digital communications, the first digital hearing aid was fabricated. The digital hearing aid uses the microphone to get the electrical signal. Then after A/D conversion, the digital signal processing (DSP) is performed to get rid of the noise and modulate the signal. Finally, the digital signal is converted to analog signal which is heard by the user. Hearing aids with digital technology contain a very advanced degree of signal processing that can provide better accuracy, sound quality, perception of loudness and environmental noise reduction [5], [8]. At the same time, digital hearing aids can have many separate amplifier channels. Most digital models are programmable using personal computers and can offer a high degree of flexibility and precision. Moreover, the digital hearing aid, which is so small as to be practically invisible out of canal, could be compared to a contact lens.

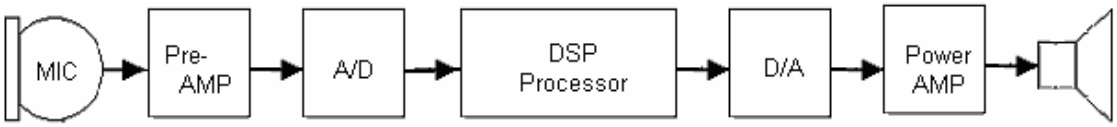


Fig. 1.3 A digital hearing aid system

Because of the advantages of the digital hearing aid, many researchers focus on the digital hearing aid. The major concerns in the hearing aid design are noise and echo cancellation by DSP and the whole system power consumption budget. However, taking into account the limited size and battery supply in hearing aid devices, putting DSP chip in the earpieces perhaps is intuitively not the best choice. For traditional hearing aids, the battery capacity is limited, such as one kind of 600 mAh battery in the market [9], because of the small size of hearing aids. It is difficult to build complex circuits for the hearing aids, because of the limited power supply, especially for the CIC. For example, some good noise cancellation performance method can not be built in the hearing aid

(HA), which needs more circuits to be implemented. Usually, conventional hearing aids use the filter banks to cancel the noise, so the noise cancellation performance is limited. To solve this problem, some manufactures use bipolar technology in their hearing products, because the bipolar technology consumes less power to get the similar performance compared to the CMOS technology. However, the hearing aids built with bipolar technology are more expensive than those with the CMOS technology.

The size of the hearing aid is small, such as CIC, so it is not practical to design a hearing aid in only one part with the trade off in size, power consumption, and efficiency. It faces challenges to improve the hearing aids performances further.

The integrated circuits design has been scaled down to deep submicron (DSM) technology. Analog, digital, mixed signals and radio frequency signals processing circuits can be built into one chip. Digital signal processing methods are more advanced than before, better noise canceling circuits can be implemented in a DSP chip. Considering recent evolutions, the wireless hearing aids having multi-microphones, analog, digital and mixed signals and radio frequency signals processing circuits, DSP and programmable unit seem to be promising to provide enhanced performance [1], [10].

A typical wireless hearing aid scheme is shown in Fig. 1.4. It has a body unit and an earpiece [1]. The earpiece communicates with the body unit by a RF link. The earpiece receives the audio signal and converts it into an electrical signal. After A/D conversion, the signal processing is done in the body unit and transmits back into the earpiece using RF link. The earpiece converts the RF signal into audio signal and feeds it into the patient's ear. This kind of wireless hearing aid has several characteristics. It gives better noise cancellation, easy trade off in hearing aid earpiece power consumption and size etc.

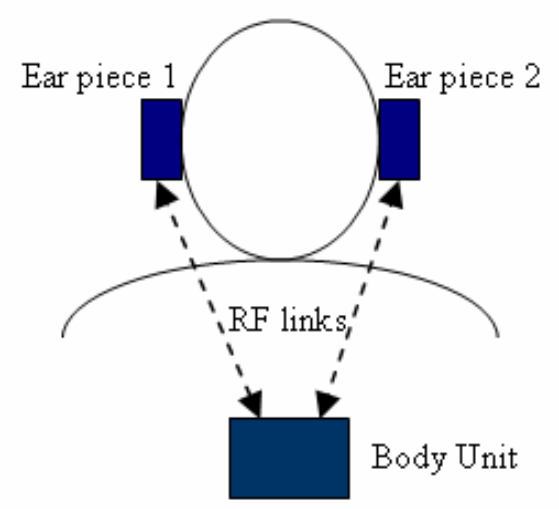


Fig. 1.4 Typical wireless hearing aid principle

Based on the concept of RF link as shown in Fig. 1.5 [1], a typical wireless hearing aid can be configured as shown in Fig. 1.5. In this architecture, the wireless hearing aid has two separate parts, a body unit and an earpiece with RF wireless links connecting between them. The voice sound is received by the microphones in the earpiece. In order to get a clearer voice, only one microphone is not enough [5]. So, in the wireless hearing aids, there are two omni-directional microphones built in the body unit, which not only provide a good noise cancellation performance, but also help the users locate the sound. The microphone outputs are amplified to feed forward into the following AD converter. After AD conversion, the data are transmitted into a RF receiver in the body unit. The DSP block following the RF receiver lies in the body unit and functions to eliminate unwanted surrounding noise, reverberations and echo. Various DSP algorithms are implanted to realize complex functions [11], [12]. The noise cancellation output is transmitted between earpiece and body unit via RF wireless link. Modulation methods are optimized for a tradeoff between size, complexity and power. After the RF receiver receives the RF signal from RF transmitter in the body unit, the signal is down converted

to low frequency signal. Then the digital signal is converted to analog signal by D/A converter to drive the earpiece speaker.

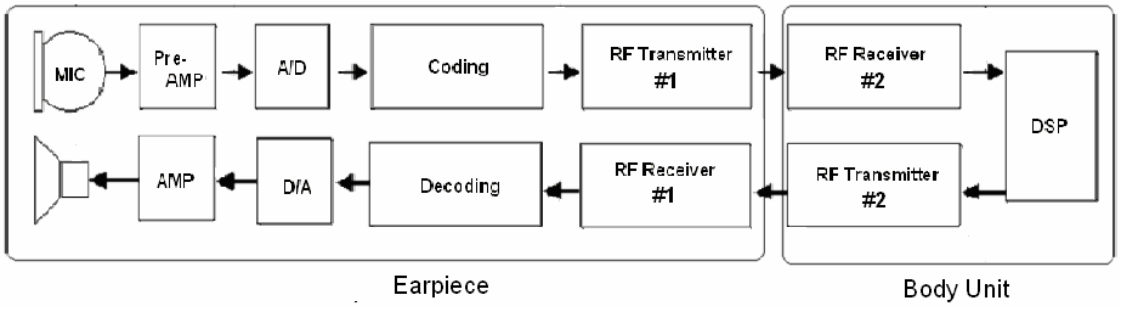


Fig. 1.5 Typical wireless hearing aids system construction

Some characteristics of a wireless hearing aid, compared to the conventional hearing aids, as discussed below:

(1) Wireless hearing aids primarily have two parts, body unit and earpiece, connected by a RF link. The body unit size is bigger than conventional hearing aid size. The bigger battery with higher capacity is used in the body unit. The power hungry circuits for hearing aids can be built in body unit. As a result, the earpiece can be built with less power consumption circuits and of the smaller size.

(2) Better noise cancellation method is implemented in DSP part in the body unit for clear voice. There are several good noise cancellation performance methods based on adaptive signal processing, which are built in the DSP block. Moreover, two microphone inputs and binaural configuration also help noise cancellation and sound localization.

(3) In order to be compatible with other audio device, these functions can be realized in DSP block inside body unit. As is a trend to be all-in-one, the features of the body unit can be embedded with other audio devices, such as mobile phone, MP3 player, FM receiver and other handheld audio devices.

(4) HA circuit noise is one of the most stringent problems for the HA users, if the circuit noise is so large that makes the useful signal distortion. It is possible to design more compensation circuits for less noise in body unit, because of more power capacity and larger size of body unit.

Keeping above in view, wireless hearing aids seem quite promising, which are currently under research and investigations.

1.2 Design Challenges of Hearing Aid Device

For a long time, hearing impairment has been an inevitable severe problem in the medical community. However with technological evolutions, attempts have been made to provide hearing aids. With the increase of IC technology development, currently available hearing aid devices, such as analog hearing aids, though help the patients up to certain extent, have the severe problems related with noise and echo. They do not satisfy users' need. With time, technology has been further advanced and it has opened a wider window to overcome such problems. More and more researchers [1], [3] show their interests in the study of advanced hearing aid devices which give more benefit to the hearing impaired. Many of them focused on the issue of digital signal processing (DSP) method for noise cancellation, speech quality improvement, ultra low power consumption and lower price, etc. However, there are a number of design challenges to bring the technology to the end user. It includes issues related with minimum power consumption, noise cancellation, size and portability, etc.

1.2.1 Size and Power Consumption

A hearing aid system invisible to other people like CIC or ITC hearing device is more acceptable to the impaired nowadays. However, the limited size of hearing devices is not able to hold current complex functions, which needs more complicated circuits and power consumption.

The problem is how to realize a tiny hearing aid with complex function. While highly integrated circuit is needed to realize complex functions, separating redundant components from ear-piece to a body unit can be a choice [10].

Battery life is a crucial characteristic of hearing aid devices. Worn by the patients throughout the day, hearing devices are expected to maintain a longer working life. Some researches [13] focus on developing long-lasting batteries which are out of the scope of this thesis. Another way is using rechargeable battery that is recharged when it has no power. In the market, there are different kinds of batteries for hearing aids. Unfortunately, the power capacity of battery for hearing aid is limited, even for BTE hearing aids. In Table 1.1, some hearing aids battery capacities are shown [9]. At the one side, investigations are needed to enhance the battery capacity, at the other side, circuit design researches are focused on reducing power consumption of the hearing aid systems.

Table 1.1 Hearing aid battery capacity in the market

Battery model number	H.A. type	Capacity / mAH
A675	BTE	600
A13	BTE/ITE	260
A312	ITE/ITC	150
A10	ITC/CIC	80
A675P	Cochlear	520

The present hearing aids are built using microchip and other electronic components. Obviously, the microchip power consumption should be reduced. In the conventional

hearing aids, especially digital hearing aids, noise cancellation method is implemented in the chip. Since the complexity of noise cancellation algorithm should be increased for improved noise cancellation performance, so as the power consumption. With the development of semiconductor technology, especially submicron technology, the circuits can be built with much less power consumption to realize same function. To further reduce the circuit power consumption, the number of off-chip components should be reduced. The system power cost is greatly reduced to a much lower level by integrating components to one silicon chip. Current technique on semiconductor has been used in hearing aid device to reduce both its size and power consumption. However, even with these methods to reduce circuit power consumption, it is still difficult to get a better noise cancellation in with limited power budget.

Many researchers have shown their interests in monolithic hearing aid design with technology of 0.6 μm CMOS [3] and 0.8 μm BiCMOS [1] in the past 3 years. However, these have inherent limitations. Normally, the price for implementing circuits in BiCMOS technology is higher than implementing circuits in CMOS technology. Hence, wireless hearing aid implemented in CMOS technology may be a more economic solution.

Digital circuits are designed in CMOS technology, such as DSP chip, because of the higher speed and lower power consumption. At present, the CMOS technology has already reached the 0.18 μm. In some situations, the analog circuit and RF circuit can be implemented in CMOS technology with the similar performance compared to the one with bipolar technology. In the wireless hearing aid design, it includes not only digital circuit part but also analog circuit, RF circuit part. So when the chip, which includes

digital circuit, analog circuit and RF circuit, is designed using the BiCMOS technology, it faces the drawbacks of the BiCMOS technology. The CMOS technology is preferable in hearing aid devices since CMOS technology is more suitable for mix-signal IC design compared to other silicon techniques strongly backs up this preference. That means digital circuits and analog circuits can be fabricated in one chip with CMOS technology in order to be cheap enough. The complexity in digital circuits is increased to compensate the disadvantages in the analog circuits and RF circuits when built in CMOS technology. The recent improvement in the CMOS technology promises a more miniaturized and lower-power consuming circuit, which will benefit to hearing aid design.

The RF receiver is the main part of earpiece in wireless hearing aid. There are several fundamental topologies for RF receiver design. One of the typical RF receiver topologies is shown in Fig. 1.6.

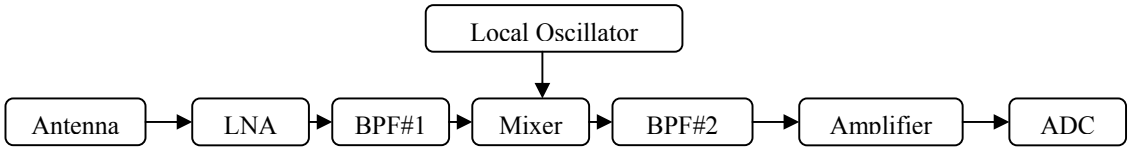


Fig. 1.6 Typical RF receiver architecture

The receiver function is transferring RF signal to base band signal. There are some fundamental blocks in the receiver. LNA is the first block in the receiver. It amplifies the weak RF signal adding as less noise as possible. Band pass filter #1 rejects the imaginary RF signal and passes the desired RF signal. Mixers are used to down convert the high frequency signal to low frequency signal. Local oscillator provides high frequency signal for mixer to down convert the desired RF signal. Band pass filter #2 only passes the desired signal. Amplifier is working at base band frequency to provide suitable amplitude for the following AD converter. After AD conversion, the base band analog signal

becomes to digital signal. The further digital signal processing can be implemented. LNA design is important in the whole receiver design. It should amplify the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding as little noise as possible, handle large (unwanted) signal along with some very weak signal. For example, noise figure is a very important parameter in receiver design, which is the ratio of input SNR to the output SNR. If the LNA noise figure is too high, the noise figure of the whole receiver is not acceptable, because normally the total noise figure is mainly determined by the LNA noise figure. That means the signal is affected by the noise, if the receiver noise figure is too high.

The literature search shows that by far there is no CMOS LNA design for wireless hearing aids, especially in very low voltage and low power operation. It is not easy to trade off among power gain, noise figure, linearity and matching in such low voltage and low power consumption. Designing LPLV LNA circuit is one of the major challenging problems involved in the design of CMOS wireless hearing aids.

1.2.2 Background Noise and Echo Cancellation

With the advancements in integrated circuits technology the performance improvements of audio device, such as hearing aid devices, has been more beneficial to the end users e.g. hearing impaired. However, an input to such device is often associated with the environmental noise. For instance, even for a hearing-impaired person with a HA, due to environmental noise, a hearing-impaired person not only feels severe hearing loss but is also unable to discern desired speech from the environment noise sometime.

Environmental noise, also termed as reverberations, is the main noises that make a hearing-impaired person unable not discern desired speech.

When a hearing-impaired person is in a noisy environment, even with a HA, the surrounding noise may interfere the desired voice that makes the hearing-impaired person to have the difficulty in discerning the desired speech. So the hearing aid should only amplify what the hearing-impaired person need to hear and reduce what hearing-impaired person does not want to hear. Thus, even in the noisy environment, the HA should be able to cancel all surrounding noise and selects only desired speech.

The conventional hearing aids which are merely amplifying all inputs or doing simple filtering have been proved to be insufficient. The speech enhancement which includes noise cancellation and echo reduction is needed. With the help of DSP technique, today's hearing aid devices start to develop their ability on speech enhancement.

A simple design in many current commercial hearing devices is using a single directional microphone for voice pick-up. By inhibiting background noise, SNR is increased (Siemens Hearing, Unitron Hearing, etc). Many DSP algorithms are presented for such single microphone setup and most of them are based on frequency spectrum analysis [14] or wavelet transforms [15].

Due to the fact that interference often overlaps in the frequency domain with the desired speech, the single microphone setup is not sufficient [5]. Current researches are focusing on using more than one microphone, especially on dual-microphone setups. The principle is by using more than one microphone, the system obtains more information on both the desired speech and noise [16], [17]. Thus, it is possible to extract the desired signal from the inputs. Adaptive filtering [18], [19], [20] is used as the fundamental

method in these studies. Some researchers also use an estimator to estimate the noise then cancel the noise from the original signal [1]. However, the result seems not satisfactory enough. Currently, there are few commercial products implementing a mature multi-inputs signal processing technology.

As an example, Fig. 1.7 shows a noise cancellation application situation for hearing aids users.

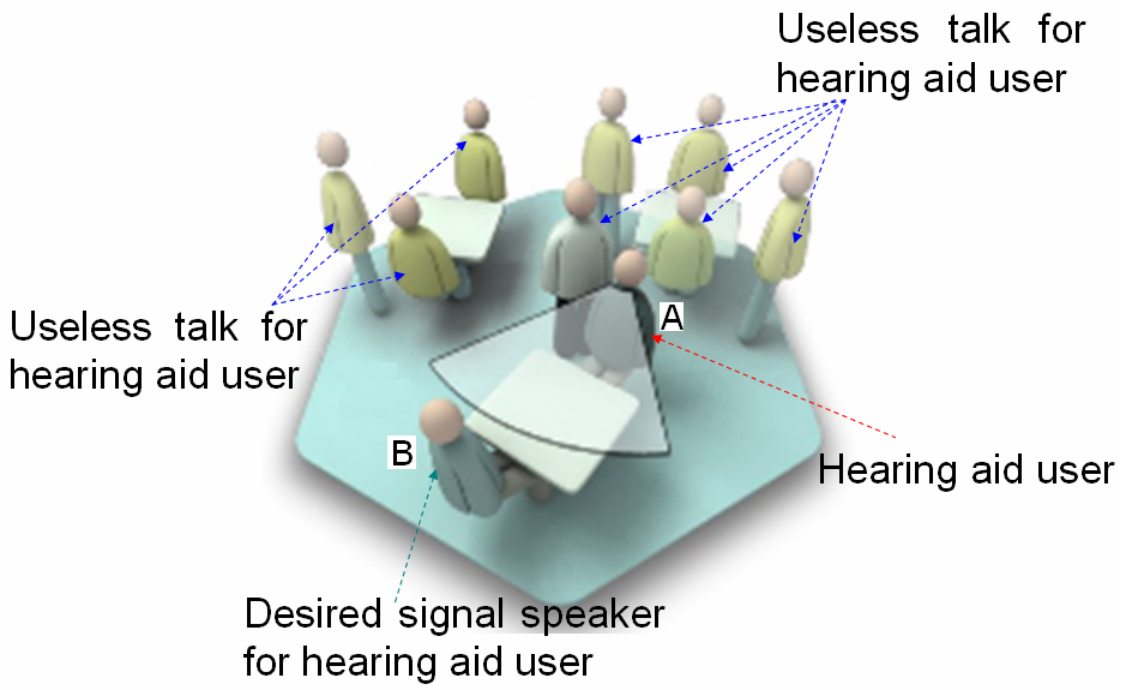


Fig. 1.7 Example for noise cancellation application situation in hearing aids design

Person A, a hearing aid user, is in a noisy environment as some people are standing besides him and talking. However, person A does not care about other people's talking. The hearing aid user only wants to perceive the voice from the person B.

The noise, undesired voice, and the desired signal are both in audio frequency band. The normal filter bank method is difficult to get rid of the noise. Adaptive signal

processing method can be used in this situation. However, the two-element beamforming method has some limitations.

Since noise cancellation is very important for users, further investigations are required to get a clear voice. Many researchers are focusing on further investigation for improving the noise cancellation schemes [12], [21].

1.3 Objective and Scope of Thesis

The research work reported in this thesis aims mainly for two aspects concerning wireless hearing aids:

(i) Low power low voltage design and development of CMOS low noise amplifier circuit. Under this, the scope of work includes design and test of a CMOS LNA operated at 1.0 V, keeping in view the wireless hearing requirements.

(ii) Background noise cancellation method with beamforming method for wireless hearing aids. Investigating the improved noise canceling method and its application in wireless hearing aids system simulation is included within the scope of the work.

1.4 Organization of Thesis

The thesis is divided into five chapters. It begins with the hearing aids introduction in Chapter 1. Chapter 2 provides the details of design and optimization techniques of the CMOS LNA circuit with low voltage and low power consumption for wireless hearing aids. Measurement results and discussion of CMOS LPLV LNA are presented in Chapter 3. Noise cancellation method, modified two-element beamforming, for wireless hearing

aids is described in Chapter 4. Conclusions, together with some suggestions for future work, are included in Chapter 5.

Chapter 2 Low Noise Amplifier Design and Optimization

2.1 Introduction

Receiving the processed audio signal within the power budget of an earpiece in wireless hearing aids is one of the inherent design challenges [1]. Low noise amplifier is the first stage to receive the RF signal, which is embedded in the earpiece of a wireless hearing aid. Literature survey shows that there has been not much attempts to implement a CMOS receiver for the earpiece of wireless hearing aid systems, especially on LVLP LNA design. Towards CMOS implementation, in this thesis, a low power consumption low voltage monolithic single-ended CMOS low noise amplifier with cascode source inductive degeneration at the source is presented. The LNA design targets, topology and optimization are also described.

2.2 RF Models for LNA Design

Because MOSFETs, spiral inductors and capacitors are often used in LNA circuit, the accurate RF models are very important to predict the silicon performance of gigahertz circuits. The characteristic of transistor in low frequency is different from the one in high frequency. The parasitic effects of transistor should be considered in circuit design, which are not included in the low frequency circuit design. So the transistor model for low frequency design is quite different with the model for high frequency design. Moreover, in high frequency, the inductance and Q value varies with the operating frequency, and capacitor also has parasitic effects. So Inductor and capacitor models should also be

studied carefully for correct design. Otherwise, the difference between simulation results and testing results are unacceptable.

2.2.1 MOSFET RF Models

MOSFET models, especially the RF MOSFET models are required to predict the silicon performance accurately, such as sub-circuit short channel MOSFET models for RFIC designs. In the sub-circuit models, MOSFET is divided into two parts, an intrinsic part and an extrinsic part. The intrinsic part represents the main active part of the device, which can be any compact model, such as Berkeley Short-Channel IGFET Model (BSIM). BSIM3 Model is a physics-based, accurate, scalable, robotics and predictive MOSFET SPICE model for circuit simulation and CMOS technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. This model has already been accepted and verified. However, the extrinsic part consists of most of the parasitic elements, including all the terminal access series resistance, gate resistance, overlap and junction capacitance, and substrate network. One of such NMOSFET model is shown in Fig. 2.1, which is used for RF circuit design. The transistor symbol in the figure is the BSIM3 model. The resistors, inductors and capacitors in the Fig. 2.1 are all ideal components. This charge-based model takes into account short channel effects and Non-Quasi-Static (NQS) effect. It is valid in all regions of operation, from strong inversion to weak inversion, and in all of DC, small-signal AC and large-signal analysis up to 10 GHz.

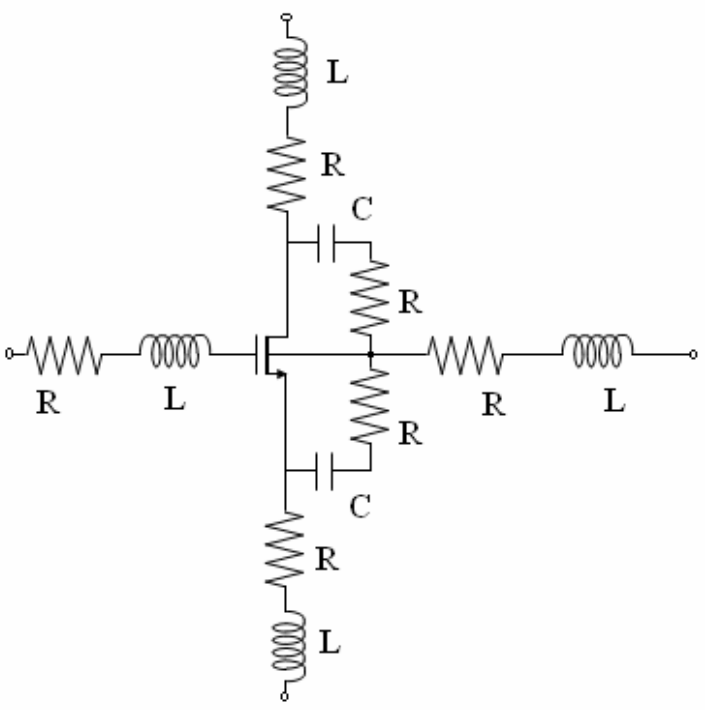


Fig. 2.1 NMOSFET model for RF circuit design

As the MOSFET models include main noise sources, i.e. channel thermal noise, flick noise, terminal resistances thermal noise, substrate resistances thermal noise and induced gate noise, they work well for the noise performance prediction of short channel devices, which is critical for low noise RFIC designs.

2.2.2 Inductors RF Models

Spiral inductors with reasonable Q and self-resonant frequency are widely used in the RFIC designs, such as fully integrated LNA, oscillator and impedance matching network. They are proved to be most difficult passive components to be implemented on chip. Fig. 2.2 shows the layout of a circular spiral inductor, which is defined by their geometry sizes. For example, a circular square spiral inductor is defined by side length, wire width, wire space and number of turns.

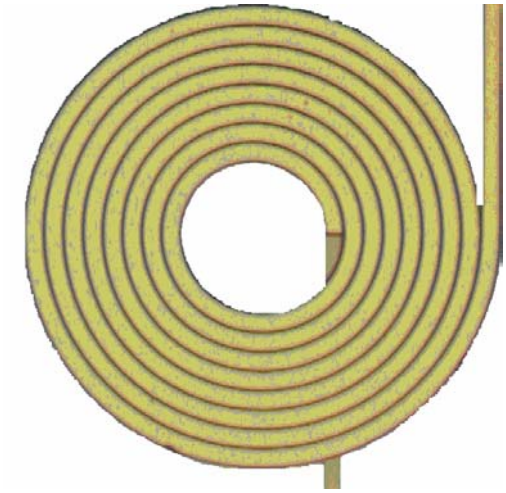


Fig. 2.2 Layout of circular spiral inductors

A typical spiral inductor consists of several series or/and parallel metal segments. Each segment is modeled as two-port lumped components as shown in Fig. 2.3, which is used for RF circuits design. Therefore the spiral inductor becomes a finite-lumped-element circuit of series and parallel connection of lumped segments. Solving the circuit equations in the model, we can compute the inductance matrix and capacitance matrix, then find the final characteristics of spiral inductors.

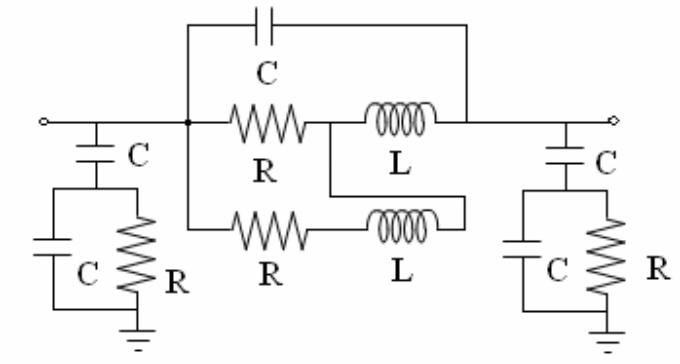


Fig. 2.3 Circular spiral inductor model

Although the model helps the designers to predict the silicon performance, the design of higher performance spiral inductors with smaller area remains a very challenge task due to the electrical coupling, relatively high metal resistance and substrate loss in

CMOS process. Some novel techniques compatible with standard CMOS process have been reported. They include higher conductivity metal layers or multi-shunted metal layers with increased effective thickness to reduce the metal loss [22], thick oxide, floating inductors or ground shields to reduce the substrate loss [22], tapered shape to optimized performance from energy point of view [23], miniature 3-D structure to reduce the area [24].

2.2.3 Capacitors RF Models

Capacitors are another important passive components widely used in RF circuit design, such as impedance matching and DC block. Fig. 2.4 shows a typical MIM capacitor layout structure in RF circuit design, which uses two metal layers as their top and bottom plates. Normally, the metals used to constructed capacitor are the high layer metals. For example, sixth layer metal can be as top plate and first layer metal can be as bottom plate in 0.18 μm technology design. Thus, the capacitor parasitic effects are smaller.

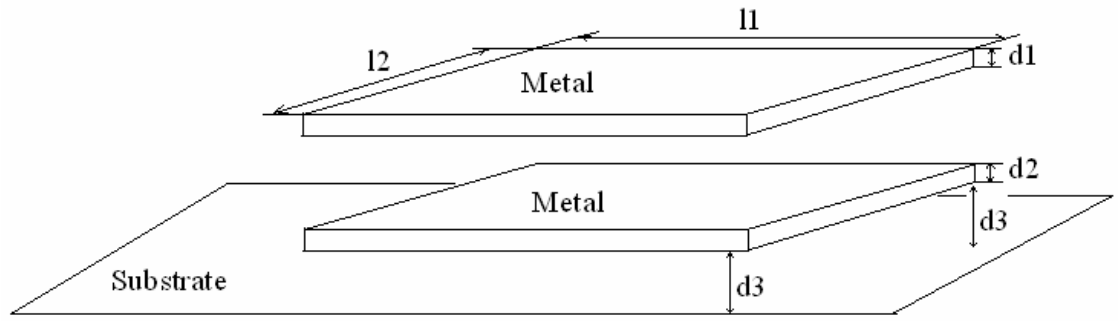


Fig. 2.4 Layout of MIM capacitors

Similar with inductor models, the MIM capacitor models is made up of a finite-lumped-element passive network by connection of ideal resistors, inductors and capacitors. Fig. 2.5 shows a typical MIM capacitor model used for RF circuits design.

Solving the circuit equations in the model, the characteristics of MIM capacitors can be got.

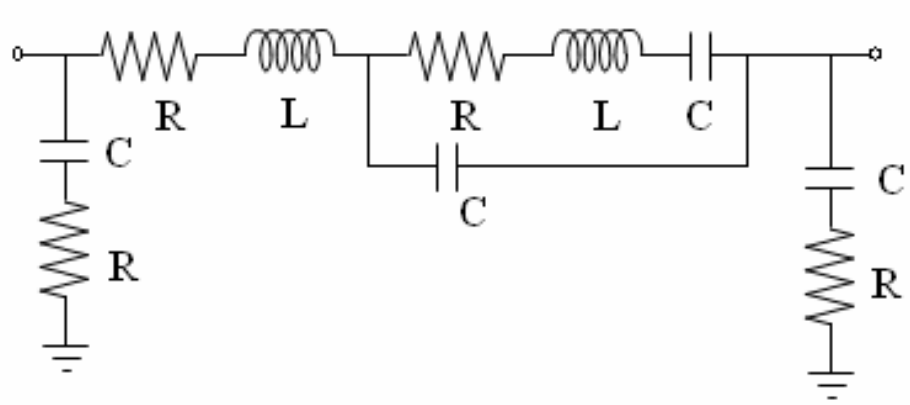


Fig. 2.5 MIM capacitor model

2.3 LNA Design Topologies

Low noise amplifier is the first stage in the receiver design. Because the operating frequency of LNA is in RF frequency band, the circuit should be as simplified as possible, especially for the RF path. Otherwise the circuit noise becomes too high. Moreover, if the circuit is complicated, the parasitic effects may distort the amplified signal.

Hence, there are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration, which are shown in Fig. 2.6.

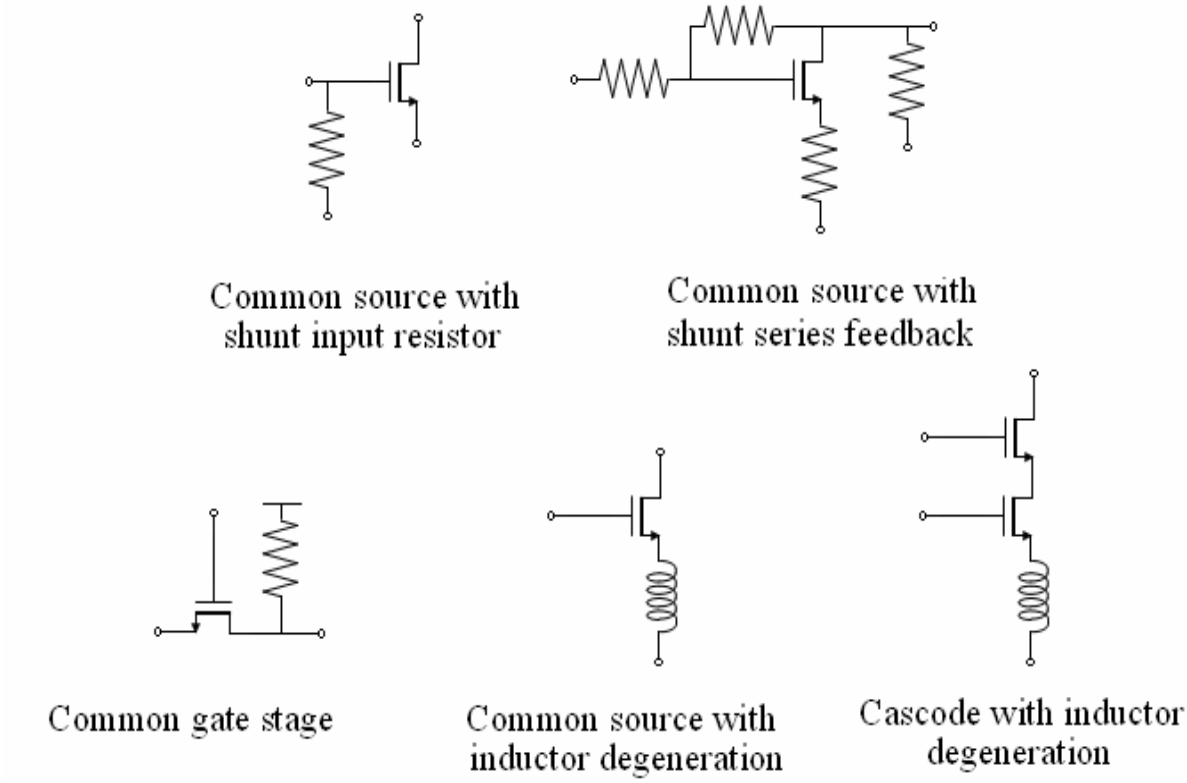


Fig. 2.6 Different LNA topologies

Out of the several topologies for narrow band single ended LNA design, an appropriate topology should be selected for low power and low voltage optimized LNA design. For common gate topology, the gain is less than 10.0 dB in very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among gain, small noise figure and better input/output matching in very low power consumption. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology, which can get the similar low noise amplifier performance in very low power consumption. Above all, the cascode inductor source degeneration topology is selected for this design. The

advantages and disadvantages of these different kinds of LNA topologies are shown as below Table 2.1.

Table 2.1 Advantages and disadvantages of LNA topologies

Type	Advantages	Disadvantages
Resistive termination common source	Broad band amplifier	Adding the noise from the resistor
Common gate	The input impendence is equal to $1/g_m$. It is practical to get 50 Ω.	The impedance varies with the bias current.
Shunt series feedback common source	Broad band amplifier	Adding the noise from resistor
Inductive degeneration common source	The source and gate inductors make the input impendence 50 Ω. Not adding noise from the input.	The inductor is off chip at low frequency and low isolation.
Cascode inductor source degeneration	Isolation of input and output is good, higher gain, lower noise figure.	The inductor is off chip at low frequency.

2.4 Specification Freezing and Design Target

The LNA is the first stage of receiver in the earpiece, which is powered by a battery. So, the power consumption is the key issue to concern in this design. Reducing LNA consumption will improve the battery life. Because the earpiece and the body unit for hearing aid device are separated within about one meter, the noise figure and gain is not as important as power consumption.

According to normal hearing aid battery capacity, the total power consumption of an earpiece, where receiver is the most power hungry block, should be as low as possible but below 3 mW [1]. The recently reported 0.9 GHz CMOS receiver consumes only 2.2 mW, out of which LNA alone consumes 1.44 mW [2]. In this low noise amplifier design, the voltage is power by 1.0 V, and the aim for power consumption is less than 1.0 mW.

With the small power consumption, the LNA should amply the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding as little noise as possible, handle large (unwanted) signal along with some very weak signal. LNA is the first stage in receiver design, and normally each block of receiver is matched. From noise figure equation [25], the receiver total noise figure is mainly determined by the LNA noise figure, if the gain of LNA is large enough. So the gain should large enough, at the same time the noise should be as less as possible. However, the gain of LNA should not be too high, otherwise the following stage, mixer, is saturated. Noise figure should be less than 3.0 dB and the gain should be more than 10 dB. Moreover, LNA should present specific impedance at the input, e.g. 50 Ω, especially interface with the filter or antenna. This is shown in S-parameter chart.

Keeping in view the wireless hearing aid design requirements, efforts were needed to freeze the specifications for LNA design application specific to these requirements. Based on the preliminary studies about hearing aids and the batteries, the low voltage and low power low noise amplifier design target are defined as shown in the Table 2.2.

Table 2.2 LNA specifications design target

noise figure	<3.0 dB
power gain	>10 dB
IIP3	>-5.0 dBm
power supply	1.0 V
current	<1 mA
S11	<-10 dB
S22	<-10 dB
P1dB	>-15 dBm
RF frequency	0.9 GHz
technology	CMOS 0.18 μm

2.5 Low Noise Amplifier Design

The design and optimization steps followed in the design of presented LNA are mentioned below. For each step, the design flow is given in Appendix A.

Step1. Specification freezing: The design specifications of the DC voltage, DC current, power gain, noise figure, S11, S22, isolation, IIP3 and P1dB are defined keeping in view the earpiece requirements for wireless hearing aids based on the literature search [1]. For example, the DC voltage is determined by the battery voltage in the earpiece. The receiver noise performance is determined by the LNA noise figure, so the LNA noise figure should be not too high, normally less than 3.0 dB.

Step2. Design simulation and optimization-stage I: the five kinds of low noise amplifiers, which are resistive termination common source topology, common gate topology, shunt series feedback common source topology, inductive degeneration common source topology and cascode inductor source degeneration topology, are considered and tried to satisfy the design requirements. If some specifications are not satisfied, the iterations are started till they are satisfied. That means that the transistor sizes, inductor values, capacitor values and resistor values are changed to match the design requirements. If the design requirements can not be satisfied no matter how to change the component sizes, the simulation for this specific low noise amplifier design should be paused. For those topologies that match the design requirements, the design specifications are further trade-off to get the best results for the design.

Step3. Topology selection step: each satisfied topology which can meet the design target in the previous design step is compared. The best LNA topology is selected for further design.

Step4. LNA design simulation and optimization–stage II: In this step, the design optimization is carried out on the selected topology to meet the design targets. The design step can be described as follows. From theoretical analysis and the preliminary simulation studies for various topologies, the CMOS LNA circuit shown in Fig. 2.7 is selected for the targeted specification. This topology seems the best suitable for a CMOS wireless hearing aid earpiece. It is based on the cascode inductor source degeneration topology.

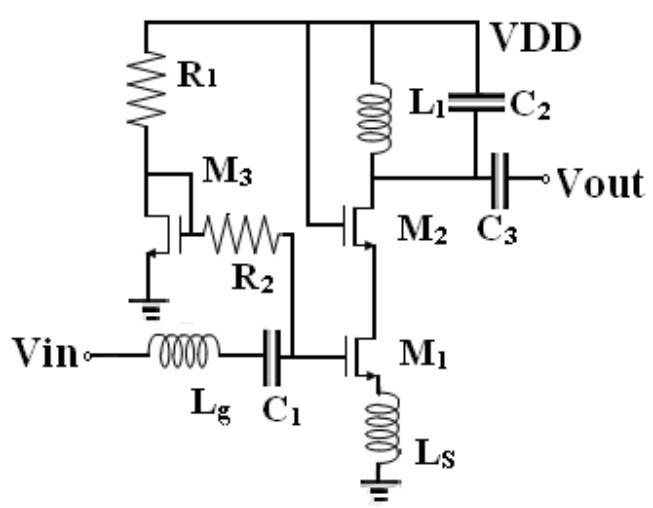


Fig. 2.7 LNA circuit schematic

It is difficult to trade off between noise performance and power consumption at the same time. Classical noise matching only considers the noise performance, so the power consumption is quite high sometimes. That means one cannot obtain both input matching and minimum NF simultaneously. Low noise circuit design starts as follows [48]: firstly, select the transistor and operation point to meet the circuit noise requirements by the preliminary noise analysis; secondly, a circuit configuration or feedback can be determined to meet the gain, bandwidth and impedance requirements; thirdly, some modification should be done to meet all specifications, such as more stages, additional

feedback or increasing the bias current of the input transistor; finally, the noise can be recalculated to see if it is still within the specifications. This iterative procedure ensures satisfactory noise performance and prevents locking in on a high-noise condition at the very beginning of the design. However, this methodology does not consider more on power consumptions. Sometimes, this methodology uses more power to meet the noise performance requirements. In the earpiece blocks design for wireless HA, power consumption is more important than noise requirement, because of the limited HA battery capacity.

For cascode inductor source degeneration topology, power-constrained noise optimization method is provided in the reference [25] and [27] by Thomas H. Lee. It was found that, for the small amount of power dissipation, there exists an optimum transistor size that provides a minimum NF while satisfying input matching [25]. However, the achievable minimum NF is a little higher than of the common-source transistor. This power-constrained noise optimization method is suitable for this LNA design for wireless hearing aid.

The proposed CMOS LNA circuit can be matched to the 50 Ω output impedance of the antenna. Moreover, the input and output impedance matching of the amplifier can be done individually. By selecting the suitable inductance, the real part of the impedance can meet the matching requirements. The input impedance of the circuit at the resonance frequency ω_0 is $R_{in} = g_m \times L_s / C_{gs}$, where g_m is the transconductance of the transistor M_1, C_{gs} is the gate source capacitance. L_s and L_g are selected to satisfy the resonant conditions for the input circuit. The value of L_s is optimized as 0.45 nH in this design according to

this input matching requirement. A cascode transistor is used to isolate the local oscillator reverse leaking to the antenna from the LNA.

A useful measure of noise performance of a system is the noise factor, which is usually denoted *F*. Noise figure is the logarithm of noise factor [25]. In Fig. 2.8, a two port driven by a source that has an admittance Y_s and an equivalent shunt noise current $\bar{i}_s$. Symbol $\bar{e}_n$ and $\bar{i}_n$ are the total noises appearing as inputs to the noiseless network.

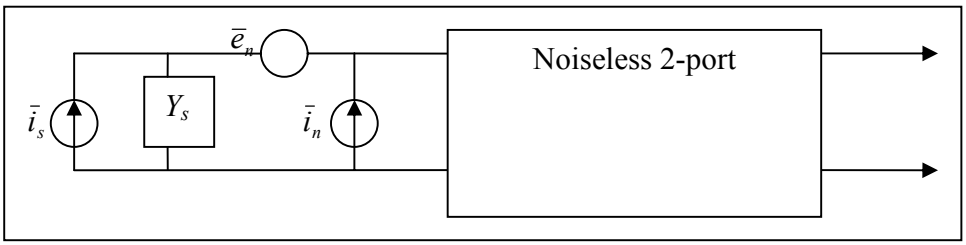


Fig. 2.8 Noisy two ports network driven by noisy source

The noise factor can be expressed as

$$F = \frac{\overline{i_s^2} + \overline{\left|i_n + Y_s e_n\right|^2}}{i_s^2} \tag{2.1}$$

In order to accommodate the possibility of correlations between e_n and i_n, express i_n as the sum of two components. i_c is correlated with e_n, and i_u is not correlated with e_n. The relation between i_c and e_n is $i_c = Y_c e_n$. The noise factor can be expressed as

$$F = 1 + \frac{\overline{i_u^2} + \left|Y_c + Y_s\right|^2 \overline{e_n^2}}{i_s^2} \tag{2.2}$$

In equation 2.2, the independent noise can be treated as an equivalent resistance or conductance. Assuming $R_n = \frac{\overline{e_n^2}}{4KT\Delta f}$, $G_u = \frac{\overline{i_u^2}}{4KT\Delta f}$ and $G_s = \frac{i_s^2}{4KT\Delta f}$, where K is Boltzmann's constant, T is the absolute temperature in Kelvin, and Δf is the noise

bandwidth in hertz over which the measurement is made. Noise factor can be expressed as

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \tag{2.3}$$

In equation 2.3, the admittance *Ys* can be expressed as $Y_s=G_s+jB_s$, and the admittance Y_c can be expressed as $Y_c=G_c+jB_c$.

The noise figure can be expressed as

$$NF = NF_{\min} + \frac{R_n}{G_s}(G_s - G_{opt})^2 \tag{2.4}$$

where $G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2}$, $NF_{\min} = 1 + 2R_n(G_{opt} + G_c)$

In this LNA topology, the small equivalent circuit for CMOS LNA is shown in Fig. 2.9. $R_n = \frac{\gamma g_{d0}}{g_m^2}$, $G_u = \frac{\delta\omega^2 C_{gs}^2(1-|c|^2)}{5g_{d0}}$ and $G_c \approx 0$, where c is the correlation coefficient defined as $c = \frac{\overline{i_{ng} \times i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \times \sqrt{\overline{i_{nd}^2}}}$. i_{nd} is the drain current noise, and i_{ng} is the gate current noise; γ is the coefficient of channel thermal noise; g_{d0} is the drain-source conductance at zero drain source bias voltage; g_m is the transconductance of transistor; δ is the gate noise coefficient; C_{gs} is the gate source capacitance; ω can be expressed as $\omega = 2\pi f$, f is the frequency.

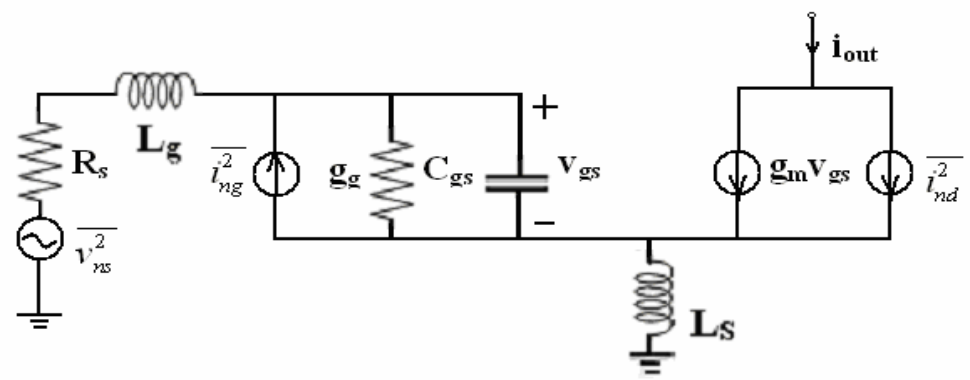


Fig.2.9 Small equivalent circuit for CMOS LNA

In this topology, combining low-noise operation with low power consumption requires the use of a low V_{gs}-V_T value, allowing a high g_m at low current levels, where V_{gs} is the voltage between gate and source of the transistor and V_T is the transistor threshold voltage. Yet, as low V_{gs}-V_T values mean wide transistors. Assuming $Q_{opt} = \frac{G_{opt}}{\omega C_{gs}} = \alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2}$ and $Q_s = \frac{1}{\omega C_{gs} R_s}$, where $\alpha = \frac{g_m}{g_{d0}}$, and Rs is the source resistance, the width of the optimum device width M_1 is determined by the equation from [25]:

$$W_{opt} = 1/3\omega L C_{ox} R_s \tag{2.5}$$

where L is the length of transistor, C_{ox} is the gate unit capacitance of transistor,. The width of the optimum device width M_1 is 300 μm in this design. This value expresses noise optimization in a way that takes power consumption explicitly into account. Moreover, the larger gate to source capacitor helps reducing current consumption [26]. In addition, the width of transistor M_3 and the value R_1 are optimized to control the gate voltage of transistor M_1.

The LNA noise figure is primarily due to the transistor M_1. The noise figure relation is expressed as equation 2.4 [27].

With the width of W_{opt}, the noise figure obtained within the power constrained is

$$F_{\min} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left[\frac{\omega}{\omega_T} \right] \tag{2.6}$$

where $\varpi_T = \frac{g_m}{C_{gs}}$.

The thermal noise from the resistor R_2 should also be considered, because it affects the input signal from the transistor M_1 gate. The R_2 value is selected large enough, such as 50 kΩ, to give as less noise as possible to the whole circuit noise figure. The transistor M_2 contributes more on IIP3 of LNA than transistor M1 does. Increasing the DC bias of M_2 improves IIP3. Since, the power consumption is the most critical for this design. The DC bias of M_2 can be optimized in terms of its gate width, while keeping the DC bias voltage of M_1 as low as possible to reduce the power consumption of the circuit. The width of transistor M_2 is optimized to be 300 μm in this design.

From the analysis and iterative simulations, the components values of LNA are optimized and summarized in Table 2.3.

Table 2.3 Component values of LNA

Component	Values	Functionality
M_1, M_2	60×(5 μm/0.18 μm)	Amplify the RF signal
M_3	8×(5 μm/0.18 μm)	DC bias current mirror
L_g	35 nH (off chip)	Input matching
L_s	0.45 nH	Input matching
L_1	14.7 nH	Output matching
C_1	8 pF	Input matching
C_2	0.5 pF	Output matching
C_3	1.0 pF	Output matching
R_1	4.8 kΩ	DC bias
R_2	50 kΩ	Reduce the input noise from DC bias circuit

2.6 LNA Simulation Results

The simulation is done in the EDA software ADS [28]. The RF transistor models, inductor models, capacitor models and resistor models are provided by CSM in CMOS 0.18 μm technology, which are mentioned in the above section. The simulation also uses the package model and pad model available in IME in-house central library. The pad model and package model are both passive networks composed of ideal resistors, capacitors and inductors. All these resistors, capacitors and inductors values are extracted from the actual wafer and PCB testing results. When the simulation includes all these models, the simulation results are more similar with the testing results. However, some parasitic, such as PCB parasitic effect, can not be fully included in the simulation, because it is more difficult to build a model for these kinds of parasitic effects. The only way to deal with these parasitic is the careful layout on PCB, such as wire width, wire length, component location, etc. Thus, these parasitic can be reduced further.

The simulation includes DC simulation, S-parameter simulation and harmonic balance simulation in ADS. From DC simulation the power consumption is got. The transistors operation points are optimized from DC simulation. It is important to give the larger gain for LNA design with the optimum operation point. S-parameter simulation considers the microwave effects, such as wave reflection and gives parameters of S11, S22, S21 and S12. From these parameters, S-parameter simulation provides input/output matching, noise figure and power gain. Harmonic balance simulation provides linearity analysis, including P1 dB analysis and IIP3 analysis. HB is a powerful frequency domain analysis technique including simulations of inter-modulation frequencies, harmonics and

frequency conversion between harmonics. It is well-suited for the predication of steady-state behavior in nonlinear circuits and systems, especially in the RF regions.

The simulation predicts a forward gain (S21) of 13.0 dB with a noise figure of 2.19 dB while drawing 0.95 mA from a 1.0 V power supply. The simulated curves of noise figure, input/output matching, and gain for S-parameters are shown in Fig. 2.10, Fig.2.11 and Fig. 2.12.

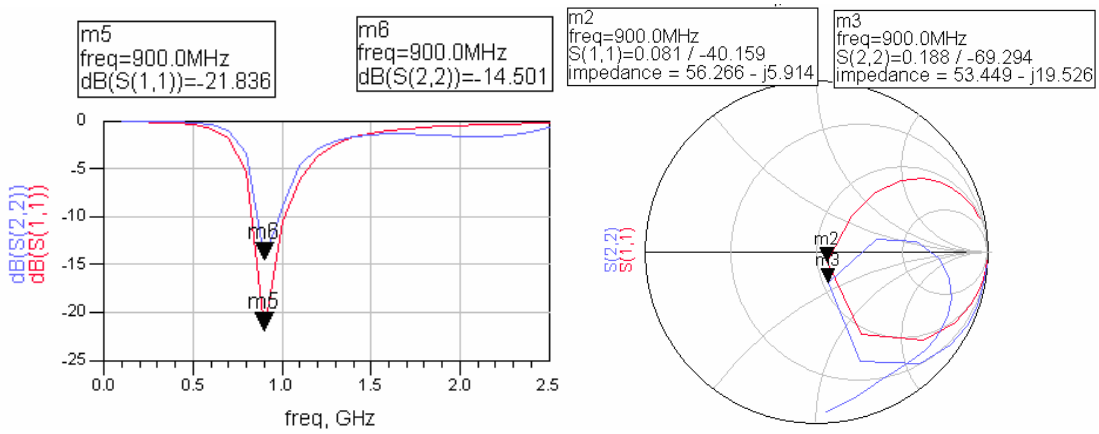


Fig. 2.10 S-parameter input and output matching simulation results

In the left figure of Fig. 2.10, S11 and S22 have the minim values at frequency 0.9 GHz. The minim values are less than -10 dB. That means the input and output power matching is good enough. The value of S11 and S22 is less than 0 dB from 0 Hz to 2.5 GHz. That means the input and output are quite sable from 0 dB to 2.5 GHz. And in the right figure of Fig 2.10, the impedances of S11 and S22 at 0.9 GHz frequency are close to 50 Ω, which is for the impedance matching.

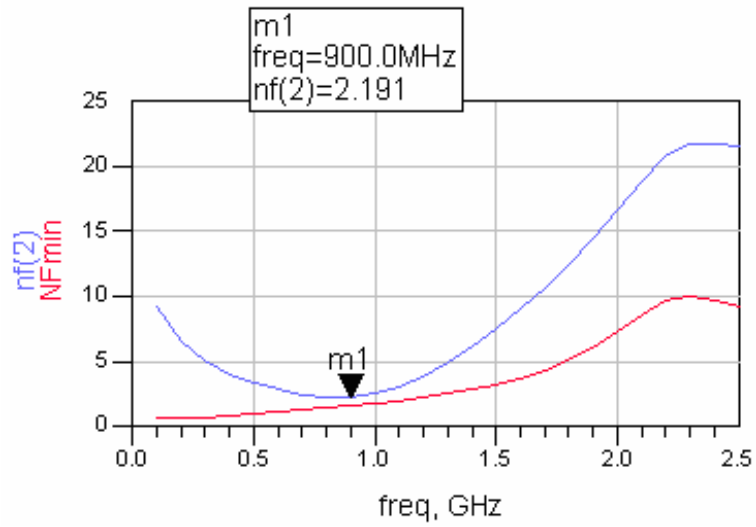


Fig. 2.11 S-parameter noise figure simulation results

In Fig. 2.11 the noise figure is 2.19 dB at 0.9 GHz frequency. The noise figure is high in low frequency and high frequency. In low frequency, the flick noise dominates the noise performance, which characteristic is proportional to 1/f. However in high frequency, with the distortion of the circuit gain, the noise performance degrades.

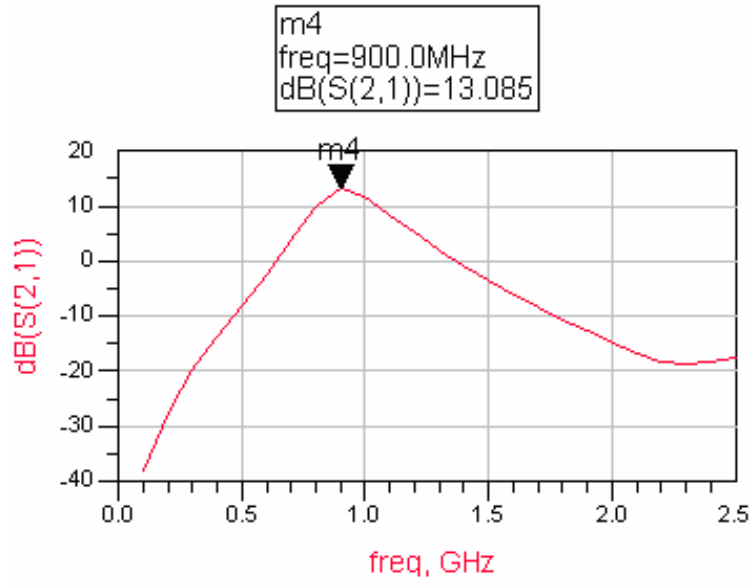


Fig. 2.12 S-parameter power gain simulation results

In Fig. 2.12, the power gain of this low power consumption low voltage LNA is 13.08 dB at 0.9 GHz frequency, which is about the maxim value in the simulation frequency band.

The various simulation iterations are performed on the proposed LNA circuit to meet design requirements. It is simulated for the whole process variation from slow corner to the fast corner. The threshold voltages for the slow, typical and fast process corners are 0.49 V, 0.41 V and 0.32 V respectively. The simulation results achieved at the typical process are summarized in the Table 2.4.

Table 2.4 Proposed LNA simulation performance summary

	Design Target	Simulation Results
noise figure	<3.0dB	2.19 dB
RF frequency	0.9 GHz	0.9 GHz
power gain	>10dB	13. 08dB
IIP3	>-5dBm	7.5dBm
power supply	1.0V	1.0V
current	<1mA	0.95mA
S11	<-10dB	-21.8dB
S22	<-10dB	-14.5dB
P1dB	>-15dBm	-14.0dBm
technology	CMOS 0.18 μm	CMOS 0.18 μm

2.7 Conclusions

LPLV LNA for wireless hearing aids was designed and described in this chapter according to the design target. In order to select the most suitable topology, five different LNA topologies are simulated and compared. The cascode inductor source degeneration topology was selected for the required design. The circuit was implemented using RF transistor, inductor and capacitor models. The simulation results show the satisfaction with the design target. The simulation predicts a forward gain (S21) of 13.08 dB with a

noise figure of 2.19 dB while drawing 0.95 mW from a 1.0 V power supply. The simulated IIP3 and P1dB are 7.5 dBm and -14.0 dBm.

Chapter 3 Low Noise Amplifier Measurement and Discussions

3.1 Introduction

Normally, in RF circuit design, there are parasitic effects which are difficult to include in simulation. These parasitic effects reduce the whole circuit performance. Hence, the RF circuit measurement is very important. The RF circuit simulation results are verified by the measurement results. After the RF circuit simulation, the circuit layout development is done. Then the circuit design is converted into the GDS format file and sent to foundry for fabrication. When the wafer is back from foundry, it is covered with package for testing. To test this LNA, the chip is soldered on the PCB with other off-chip components, such as resistors, capacitors and inductors. The LNA test includes DC test, S-parameter test, noise figure test and linearity test. Form these measurements, the LNA performances, such as power consumption, noise figure, power gain, linearity, are gotten.

3.2 LNA Chip Layout Development

Layout of RF circuits is a critical issue to determine their final performance in silicon. Several key points in the RF layout design are discussed in this section.

All the circular spiral conductors have the optimized geometry of width, radius and spacing. They are made of two shunted top metal layers (Metal 5 and Metal 6 in CMOS 0.18 μm technology) to reduce the metal loss and substrate loss. Moreover, the layout method of placing gate contacts on each end of the device can reduce the poly-gate resistance further, by half. In the transistors' layout, the multi-fingered folded structure is also used to improve the Q of parasitic capacitors C_{gs}, C_{gd}, C_{gb}, C_{db}. The number of

fingers should be chosen properly to minimize the total parasitic capacitance. Proper floor plan and routing technique are required for reducing the parasitic inductance and capacitance.

General layout design rules and considerations are still valid in RF layout designs. Sufficient number of contacts for substrate/n-well diffusion and well-placed guard rings must be placed for the high IC reliability. Around the portions flowing radio frequency signals, some additional empirical RF design rules are applied to reduce the magnetic field effects upon these components. First, because of the interference of inductor is very strong, the distance between inductor and other components should big enough to reduce the interference, such as about 50μm minimum spacing between spiral inductors and other components, self-guard-ring for each RF component. Second, this LNA is a single ended design, so the AC ground, including DC ground and voltage supply, is very important. It affects the whole performance badly if we do not consider it fully. More care should be given to the AC ground layout. Third, guard rings prevent the transistors from noise. Fourth, the RF path should be as short as possible, at the same time, use direct path as possible. Fifth, the metal for RF path should use high layer metal, such as sixth layer metal, to reduce the capacitance effect between the metal layer and the substrate.

According to these above rules, the LNA layout is developed in the Cadence design environment using CSM CMOS 0.18 um process design rules. The total silicon area required is 535 μm × 653 μm. The Design Rule Check (DRC) is made over the developed layout and the layout was ensured meeting all design rules provided by the foundry, before release for fabrication.

The test chip has 8 total pads including 2 power supply pads, 2 RF signal pads, 1 bias voltage pad and 3 ground pads.

The LNA chip bonding diagram is shown in Fig. 3.1. The chip package is QPF24 model provided by IME, which has 24 pins. However, only 8 pins were used in this design, other left pins were NC (not connected).

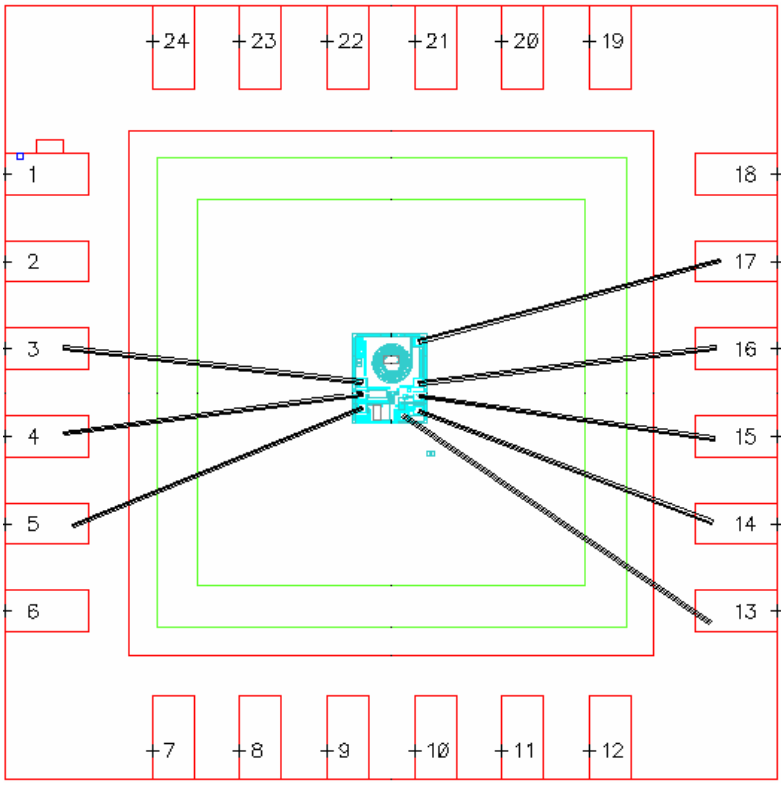


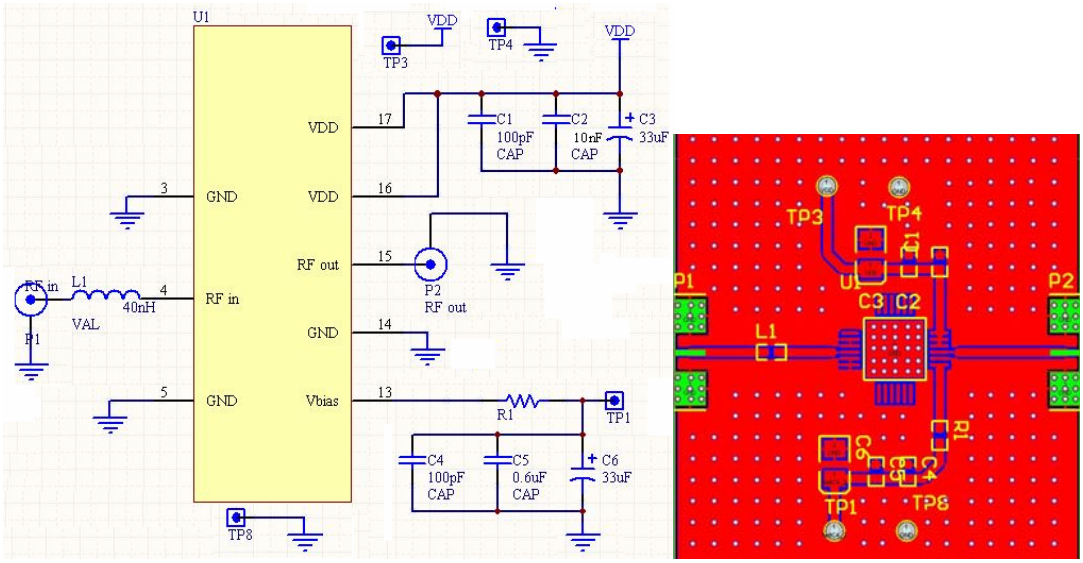
Fig. 3.1 LNA chip bounding diagram

The bonding wire is made up of low resistance metal, which gives low parasitic effects on the whole circuit performance.

3.3 LNA PCB Layouts

The PCB layout is developed using EDA tool Protel [29]. The PCB description for LNA testing is shown in Fig. 3.2. The PCB material is FR4, which is suitable for this

operation frequency. The PCB size is 1911.00 × 2189.00 mil^2. The on-board capacitors are used to filter out the noise from power supply and affect the RF signal as less as possible. Testing points TP4 and TP8 are ground. Testing point TP3 is VDD and TP1 is bias voltage in Fig. 3.2.



a b

Fig. 3.2 PCB description for LNA testing
a. PCB schematic b. PCB layout

The PIN description is given in Table 3.1.

Table 3.1 Pin description of the LNA test chip

Pin No.	Pin Name	Pin Description
3	GND	Common power ground
4	RFin	RF signal input
5	GND	Common power ground
13	Vbias	DC bias voltage input
14	GND	Common power ground
15	RFout	RF signal output
16	VDD	Power supply
17	VDD	Power supply
1,2,6,7,8,9,10,11,12,18,19,20 ,21,22,23,24	NC	Not connected

It should be noticed that the PCB design for high frequency applications looks much different from that for applications at low frequencies. The main reasons include: the impedance of PCB traces or wires has frequency-dependent characteristics of being primarily resistive at low frequency and becomes inductive at high frequency; and the PCB transmission line effect becomes one limiting factor for proper circuit operation at high frequencies.

Transmission line is a material medium or structure suitable for efficiently directing the transmission of energy between two terminals. The simplest transmission line can be formed when a PCB trace is routed adjacent to a reference plane. Its characteristic impedance is identified by Z_0:

$$Z_0 = \sqrt{\frac{L_0}{C_0}} = \frac{V(x)}{I(x)} \tag{3.1}$$

When a transmission line having impedance of Z_0 is terminated with an arbitrary load Z_L (Fig. 3.3), from microwave theories, the impedance Z_{in} seen looking into the transmission line terminated with Z_L is expressed in terms of hyperbolic functions as follows [30]:

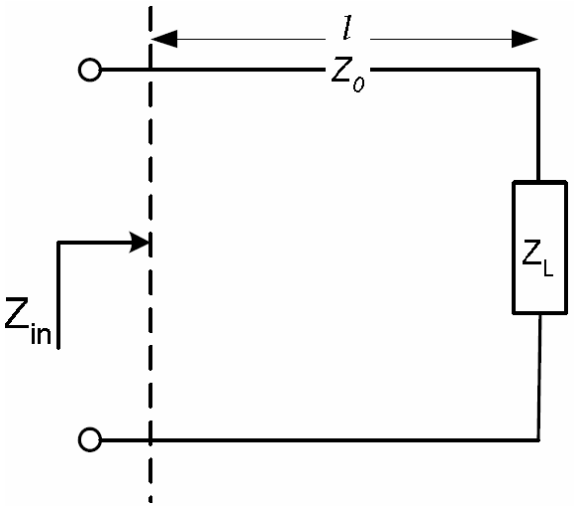


Fig.3.3 Transmission line Z_0 terminated with Z_L

$$Z_{in} = Z_0\left(\frac{Z_L\cosh(\gamma l)+Z_0\sinh(\gamma l)}{Z_0\cosh(\gamma l)+Z_L\sinh(\gamma l)}\right) \tag{3.2}$$

$\gamma = j\frac{2\pi}{\lambda}$, λ is the wavelength, l is the length of transmission line. It implies that Z_{in} is no longer the function of γ and l when Z_0 is chosen to be identical to Z_L. The condition is so called impedance match. As a part of the matching network, the transmission lines connecting RF signal pin and the SMA connector should be designed to have the same 50 impedance as the input impedance of RF equipment Z_L. The physical transmission line type of symmetric coplanar waveguide with ground as illustrated in Fig. 3.4 is commonly used in RF signal tracks. According to the theories in [30] and the material parameters, the optimal W (trace width) and G (spacing to the adjacent ground plane) of 50 transmission line can be calculated. This calculation can be done in Agilent AppCAD [31], a personal RF & Microwave design assistant. Typically, a 50 PCB trace has 5% tolerance in the fabrication.

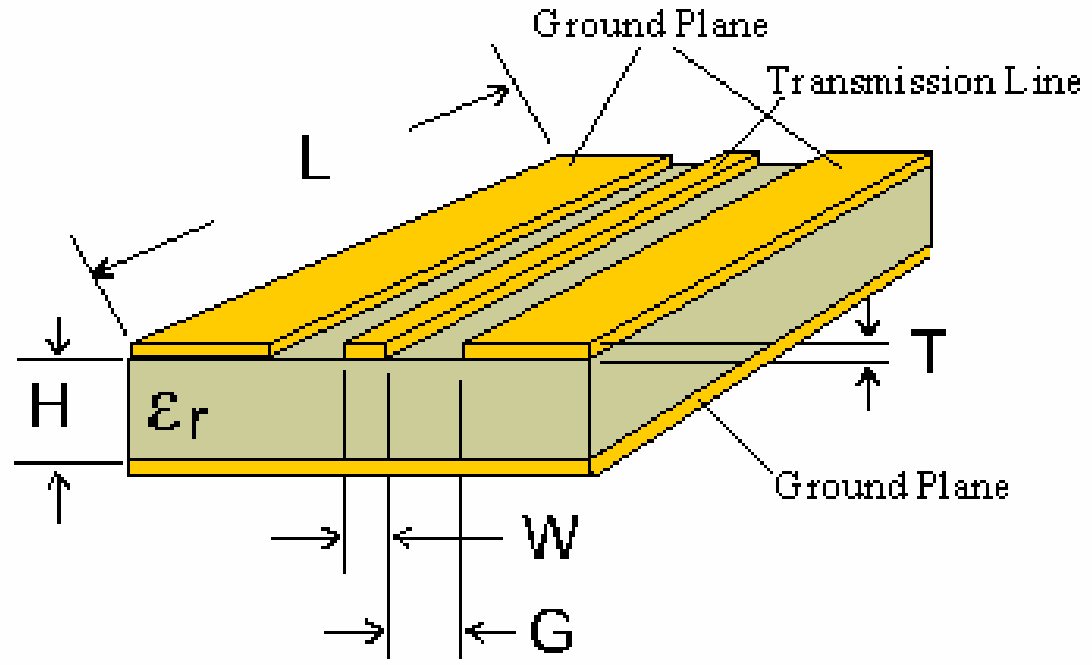


Fig. 3.4 Cross-section of symmetric coplanar waveguide with ground plane

Standard FR-4 is a commonly used material in PCB fabrication. It is suitable for the RF applications at the 0.9 GHz ISM band. Using the parameters of the double-sided FR-4 PCB given in Table 3.2, the optimal dimension of the 50 transmission line is W= 40 *mil* and G =11.4 *mil*.

Table 3.2 Double-Sided FR-4 PCB parameters

Material	FR4
Dielectric Thickness	0.8 mm
Number of Layers	2
Size	1911.00 mil by 2189.00 mil
Min Hole Size	12 mil
Min Track Width	40 mil
Min Track to Track Spacing	11.4 mil
Copper Thickness	1 oz
Finishing	Golden Flush

In this PCB layout, each RF signal track is designed as a 50Ω transmission line with optimal size. An external matching network is added over the transmission line to compensate the impedance mismatch introduced by the bond-wires in the package. The component sizes in the matching network can be calculated by using Smith Chart. During the calculation, the bond-wire can be simply represented by an inductor with 1nH/mm unit length inductance.

This PCB design requires the use of multipoint ground strategy with ground planes to minimize the impedance of RF ground loops as most high frequency PCB designs do. The main part of PCB bottom layer is used as a ground plane that links up all of the defined ground areas to improve the grounding of the test chip. The via-fences around the transmission lines can isolate the RF signals further.

All the component sizes in this PCB design are listed in Table 3.3. Several decoupling capacitors (C_1-C_6) at the power supply and voltage bias inputs are also incorporated to suppress supply noise.

Table 3.3 Component sizes in the LNA test PCB design

Name	Description	Value
C_1	DC regulation capacitor	10 nF
C_2	DC regulation capacitor	100 pF
C_3	DC regulation capacitor	33 μF
C_4	DC regulation capacitor	10 nF
C_5	DC regulation capacitor	100 pF
C_6	DC regulation capacitor	33 μF
L_1	Input matching inductor	10 nH
R_1	Biasing resistor	3 KΩ
P_1, P_2	SMA	-
U_1	Chip	-
TP_1	Testing Point	-
TP_3	Testing Point	-
TP_4	Testing Point	-
TP_8	Testing Point	-

3.4 LNA Measurement Setup and Testing

LNA test is RF test, so it is different with low frequency test. The connection between different RF equipments and LNA PCB should use 50 Ω cables with shield metal. LNA test includes DC test, S-parameter test, noise figure test and linearity test. The fundamental RF equipments are noise figure analyzer, network analyzer, spectrum analyzer, signal generator, etc.

DC testing

The current consumed by the LNA is measured by connecting multimeter between the DUT (LNA) and the power supply. Supply voltage is set as 1.0 V. The measurement equipments are shown in Table 3.4. The DC measurement setup is shown in Fig. 3.5. The measurement current can be read from the DC power supply.

Table 3.4 DC measurement equipment list

Number	Measurement Equipment
1×	Digital multimeter
2×	Dynamic measurement DC source (Agilent 66312A)

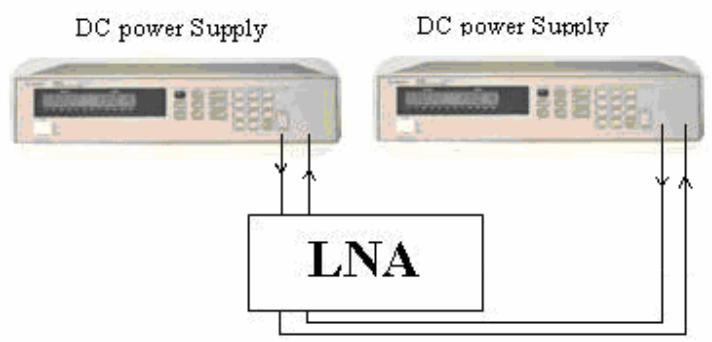


Fig. 3.5 DC measurement setup

S-parameter testing

The S-parameters of LNA (S11, S22, S12 and S21) are measured by connecting the DUT to the network analyzer, shown in Fig. 3.6. Before testing LNA, calibration should be done for network analyzer. The power supply should be switched on during the measurement. The measurement equipments are shown in Table 3.5.

Table 3.5 S-parameters measurement equipment list

Number	Measurement Equipment
1×	Network Analyzer (Agilent 8720D)
2×	Dynamic measurement DC source (Agilent 66312A)
2×	50 ohm termination cable

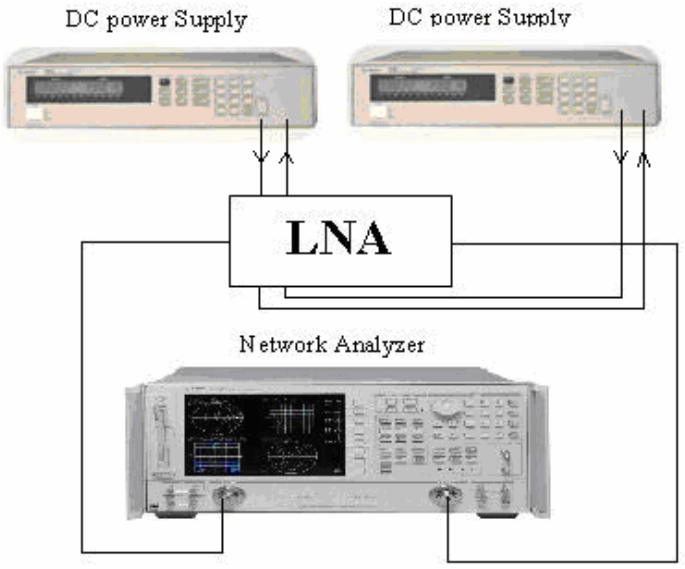


Fig. 3.6 S-parameters measurement setup

Noise figure testing

The noise figure test should be done in the shielding room, because there are so many different frequencies electronic noises have the possibility to couple into the LNA circuit. Shielding room can prevent these noise couple into the circuit from the open air. Moreover, in shielding room, each electronic device is specially designed, so it interferes on the LNA circuit quite small enough. Before testing noise figure of LNA, calibration should be done. This step is critical for noise figure test. Otherwise, the testing results are not believable. Then, noise figure can be measured when the DUT is connected between the noise source and noise figure analyzer, shown in Fig. 3.7. The measurement equipments are shown in Table 3.6.

Table 3.6 Noise figure measurement equipment list

Number	Measurement Equipment
1×	Noise Figure Analyzer (Agilent 8975A)
1×	Noise Source (Agilent N4002A)
2×	Dynamic measurement DC source (Agilent 66312A)
1×	50 ohm termination cable

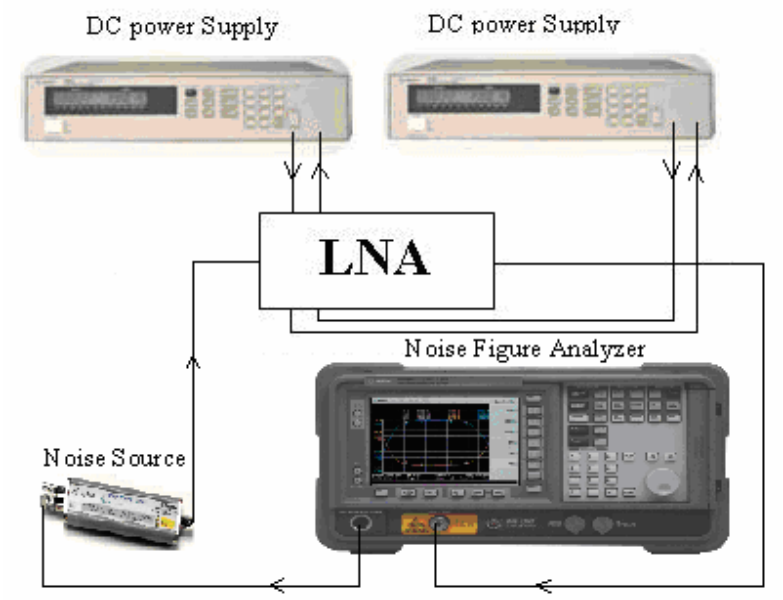


Fig. 3.7 Noise figure measurement setup

Linearity testing

To measure the linearity, two signal generators, a combiner and a spectrum analyzer are required, shown in Fig. 3.8. To test P1dB, one signal generator is turned off and other generator is swept from -60 dBm to 0 dBm. The output power level of the DUT is measured by the signal analyzer. However, when measuring the IIP3 of the LNA, two signal generators are required. The output power level of both signal generators should be set to the same level before taking the measured value at the signal analyzer. The measurement equipments are shown in Table 3.7.

Table 3.7 Linearity measurement equipment list

Number	Measurement Equipment
2×	Signal generator (Agilent E8247C)
1×	Signal analyzer (RS FSIQ26)
1×	Power divider (HP1163A)
2×	Dynamic measurement DC source (Agilent 66312A)
4×	50 ohm termination cable

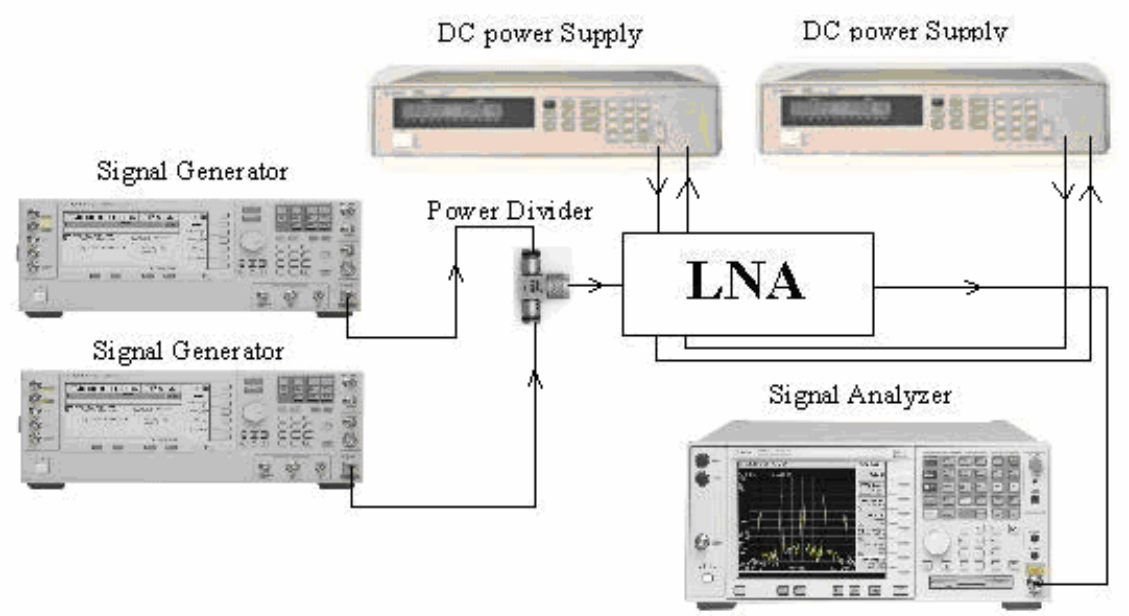


Fig. 3.8 Linearity measurement setup

3.5 LNA Measurement Results and Discussion

After chip tapeout, the chip was tested. The chip is functional and no ESD failure is encountered so far. All board level test results have been tabulated and put into the following figures.

For noise figure testing, the low noise amplifier is measured from 0.5 GHz to 1.3 GHz. The noise figure measurement results are shown in Fig. 3.9. The testing curve is very similar with the simulation results. At 0.9 GHz, the noise figure is about 2.41 dB, which is a little higher than the simulation results, 2.19 dB.

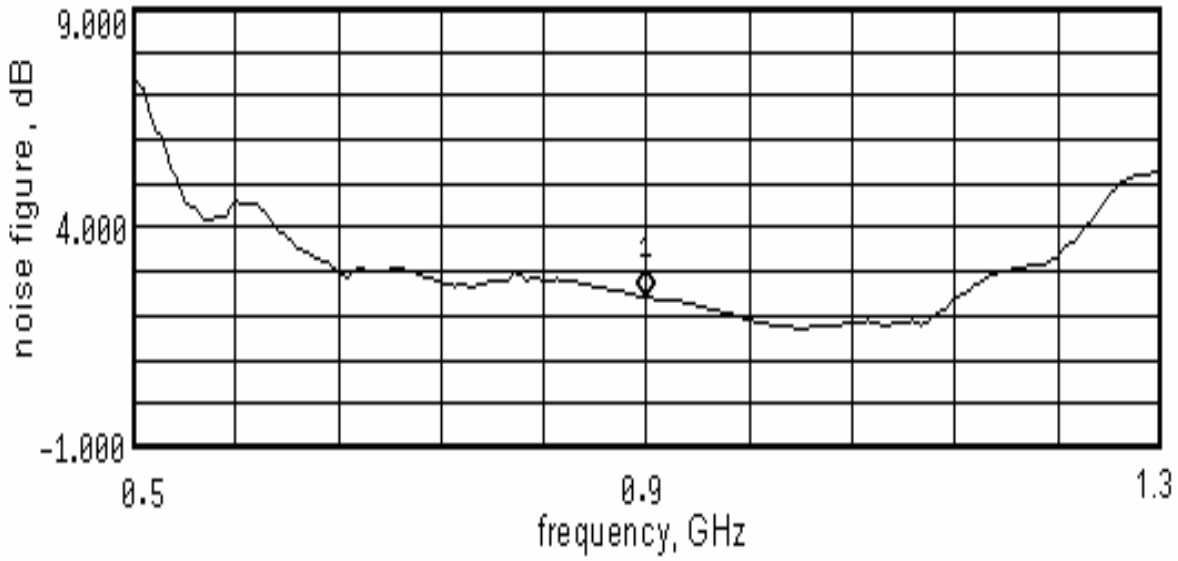


Fig. 3.9 CMOS LNA noise figure measured results

For power gain testing, the low noise amplifier is measured from 0.5 GHz to 1.3 GHz. The power gain measurement result is shown in Fig. 3.10, which is similar with the simulation result. At 0.9 GHz, the power gain is 11.91 dB. The tested value is a little lower than the simulation result.

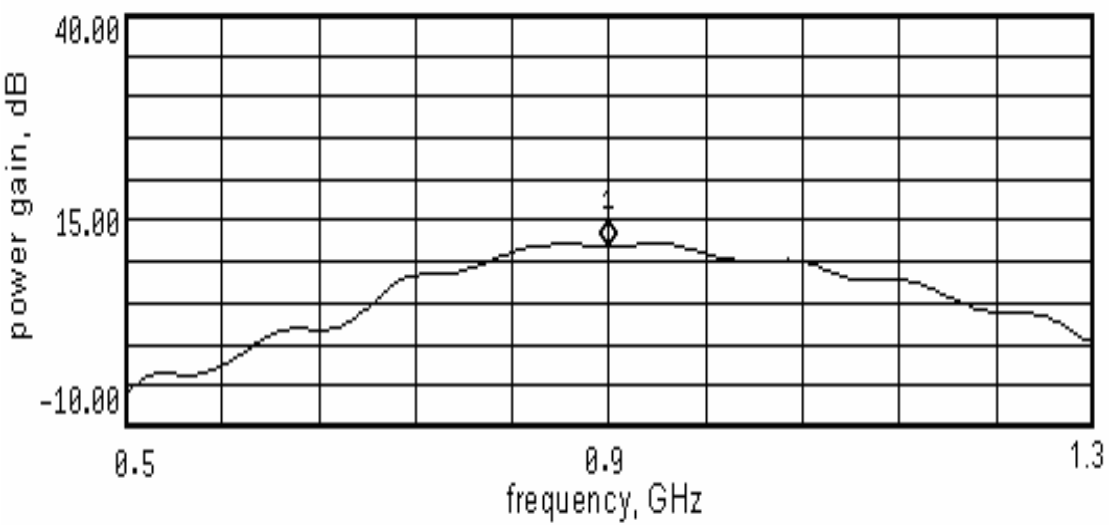


Fig. 3.10 CMOS LNA gain measured results

For P1 dB testing, low noise amplifier was measured from -60 dBm to 0 dBm at 0.9 GHz. The P1 dB measured results are also shown in Fig. 3.11. The linearity region is about from -60 dBm to -10dBm. From the test curve, the P1 dB value can be calculated and it is about -12 dBm.

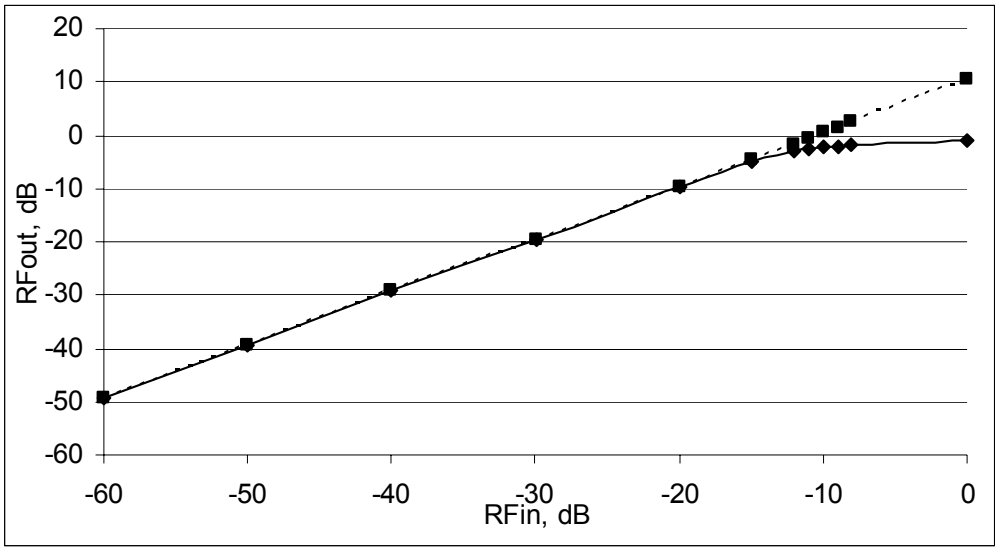


Fig. 3.11 CMOS LNA P1dB measured results
——— Tested LNA – – – – Ideal response

The input matching and output matching are also tested using a Network Analyzer. The measured data are showed in Fig. 3.12. The measured input matching S11 is -3.5 dB.

The output matching S22 is -11 dB. The deviation in tested value of S11 at 0.9GHz seems mainly because the fact that in simulation the Q and L values considered are as per the data sheet of the off chip inductor available for 2.4GHz.

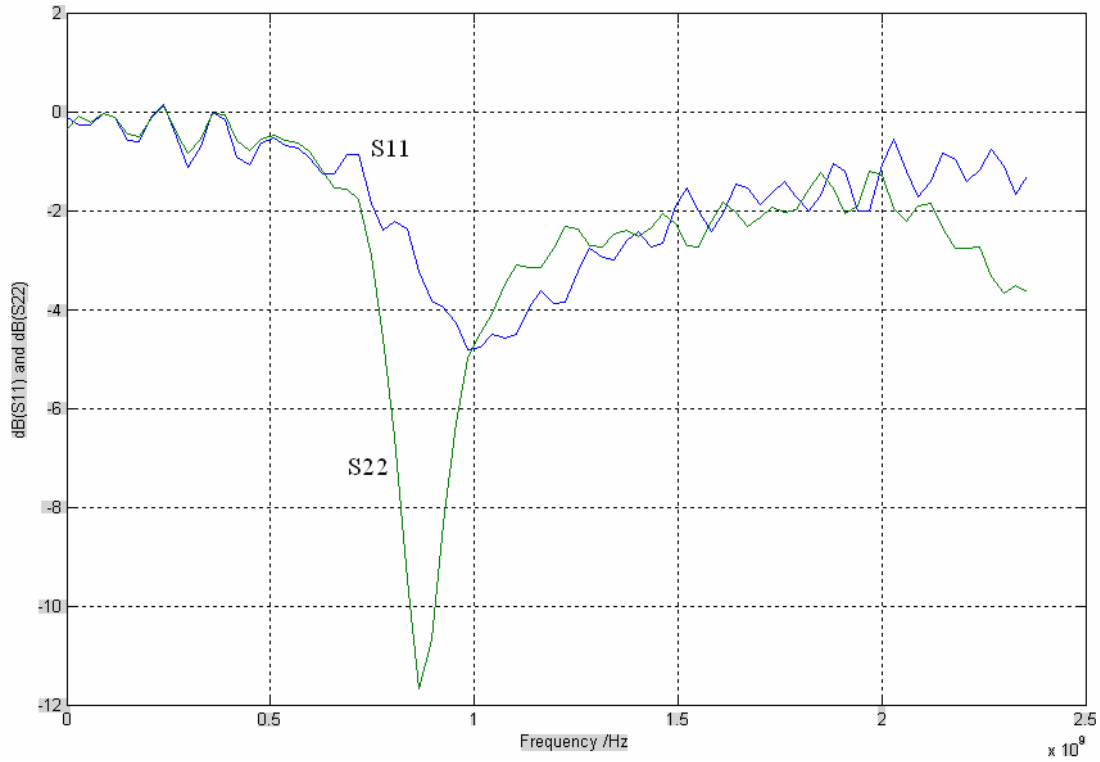


Fig. 3.12 CMOS LNA input and output matching measured results

The LNA chip microphotograph is shown in Fig. 3.13. The total silicon area used is 535 μm × 653 μm. The total power consumption is only 0.95 mW from a 1.0 V power supply, including the biasing power consumption.

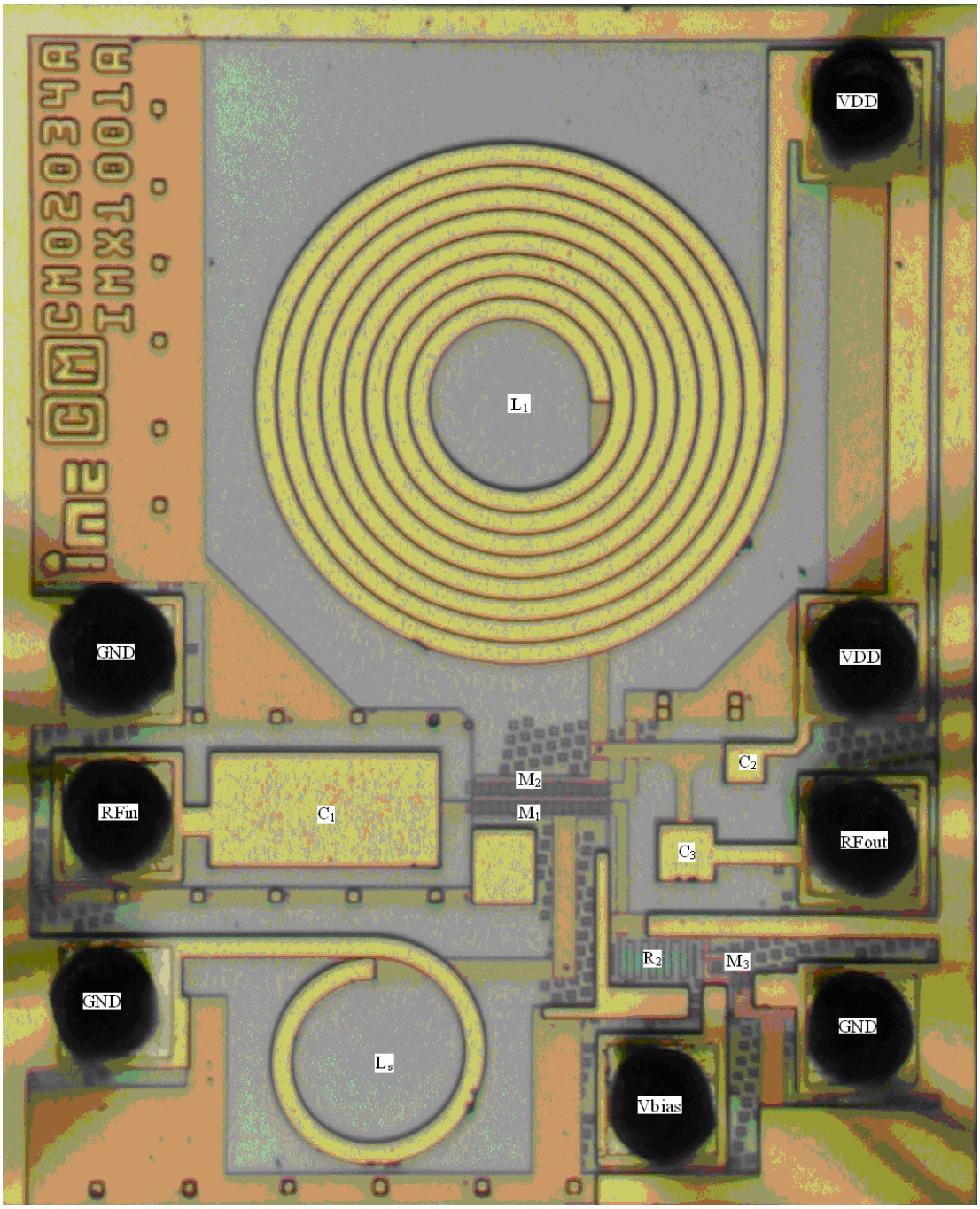


Fig. 3.13 LNA chip microphotograph

All the CMOS LPLV LNA measurement data can be summarized as Table 3.8. The testing results are similar with the simulation results.

Table 3.8 LNA measurement summary

	Simulation Results	Tested Results
noise figure	2.19 dB	2.41 dB
gain	13. 0 dB	11.91 dB
IIP3	7.5 dBm	0.72 dBm
power supply	1.0 V	1.0 V
current	0.95 mA	0.95 mA
S11	-21.8 dB	-3.5 dB
S22	-14.5 dB	-11 dB
P1dB	-14.0 dBm	-12 dBm
RF frequency	0.9 GHz	0.9 GHz
technology	CMOS 0.18 μm	CMOS 0.18 μm

There are some variations between the testing results and the simulation results. Some discussion about this follows.

DC measurement

The current consumption is the same as the simulated level.

S-parameters measurement

The measured S22 of LNA shows that the output port is matched. And the measured S11 of LNA shows the input port is a little mismatch. The isolation is about 30 dB for LNA. In term of log magnitude curve, S11 is above -10 dB at 0.9 GHz, however, the output port S22 is below -10dB at 0.9 GHz. Though the measured values meet the specification but there are still several dB lower compared to the simulated results.

There are several reasons which maybe cause the matching problems. First, the process of the passive components, such as inductors and MIM capacitors has variation. Normally, although the transistor can be built on the chip accurate, the variation of inductor and capacitor is about 20%. The circuit performance degrades if the inductance and capacitance change. This can be verified by the simulation. Second, the unknown PCB parasitic effects also degrade the performance. In the PCB design, although the

matching is design for 50 Ω, there are many parasitic effects which are difficult to model in the simulation. Such as parasitic effects from the filter capacitors for DC power supply and the connection between each component on the PCB. Third, transistor simulation model has some approximation. With the IC technology improvement, the length of transistor is very small compared to long channel transistor. So the physics of transistor is a little different. The model for long channel transistor is not suitable for short channel transistor. Moreover some parameters of the model, which describe the transistor physics, are not clear enough, such as γ for short channel transistor. Normally these parameters are got from the measurement.

The S11 value in simulation is different from the one in test. This LNA has only one off-chip component, inductor connected with the gate of transistor M1. So the inductance can be changed to change the input matching. In the simulation, the model for inductor is not accurate enough. The inductance value and the quality factor used in simulation are taken from the available data sheet which corresponds to a frequency of 2.45 GHz i.e different from 0.9 GHz. So this is believed a major possible reason in deviations between the simulation one and the test one for inductor. Moreover the simulation can not include all the parasitic effects in the PCB test, which has already been discussed above. In LNA test these parasitic effects make the input matching more complicated, such as introducing more capacitance in the input matching network. Hence in the LNA test the input matching $|S_{11}|$ is not as good as in the simulation. However, selecting a more appropriate inductor for 0.9GHz with similar Q and L values may help.

Linearity measurement

The testing P1dB is better than the simulation result. The reason is believed that the testing gain is less than the simulation result. So the testing P1dB result is better than the simulation result.

Noise figure measurement

From the testing results, noise figure is 2.41 dB. The measured data is about 0.2 dB higher than the simulated results. There maybe several reasons which can cause this noise performance degradation. First, the substrate noise is a factor. The chip substrate is silicon, which conducts noise into the circuit. This parasitic effect is very difficult to model. In simulation this effect is not easy to include. Second, the unknown PCB parasitic effects also degrade the performance. Third, transistor simulation model has some approximation.

Above all, a low voltage and low power consumption LNA for wireless hearing aid device has been implemented in CSM CMOS 0.18 μm technology. In the measurement, all the LNA designs are functional. However, the measured data show that there are some deviations between measurement and simulation. Most of the data miss the specification by a narrow margin, which is the prime suspect from other uncontrolled effects, such as bonding parasitic effects, substrate noise etc.

3.6 LNA Performance Comparison with Others Works

Table 3.9 summarizes the low voltage and low power consumption CMOS LNA designs from 0.95 GHz to 5.35 GHz applications in recent years. They were implemented in CMOS technologies, from 0.18 μm to 0.6 μm. Some applications are used special process to get the better performance. As we can see, it is a challenge to satisfy low noise

figure, low power consumption and good linearity at the same time in low noise amplifier design.

Table 3.9 A comparison of recent LVLP CMOS LNA designs

Process	Voltage	Power Consumption	Noise Figure	Gain	IIP3	P1dB	Layout Area	Frequency	Reference /Year
0.18 µm	1.0 V	0.95 mW	2.41 dB	11.9 dB	0.7 dBm	-12 dBm	535×653 mm^2	0.9 GHz	This work
0.35 µm	1.5 V	6.5 mW	1.4 dB	21 dB	-37 dBm	NA	0.51×0.25 mm^2	1.9 GHZ	[32] 1999
0.6 µm AMS	1.5 V	7.1 mW	1.8 dB	13 dB	NA	NA	NA	0.95 GHz	[33] 2001
0.18 µm	1.0 V	3.8 mW	1.8 dB	11 dB	NA	NA	0.15×0.05 mm^2	2.0 GHz	[34] 2003
0.18 µm	1.2 V	7.76 mW	2.77 dB	15.1 dB	1.18 dBm	-8.7 dBm	NA	2.4 GHz	[35] 2002
0.25 µm SOI	1.0 V	4.5 mW	3.0 dB	13.4 dB	0 dBm	-15 dBm	NA	2.5 GHz	[36] 2001
0.18 µm	1.0 V	14.2 mW	2.3 dB	11.6 dB	NA	-7.9 dBm	NA	2.4 GHz	[37] 2003
0.18 µm	1.0 V	9.8 mW	3.22 dB	15 dB	-1 dBm	NA	NA	2.4 GHz	[38] 2001
0.35 µm	1.2 V	1.44 mW	2.85 dB	21 dB	9.4 dBm	NA	NA	0.9 GHz	[2] 2002
0.25 µm	1.25 V	2.0 mW	1.35 dB	12 dB	-4 dBm	NA	NA	0.9 GHz	[26] 2004
0.18 µm	1.8 V	10.44 mW	2.3 dB	15.4 dB	-4.3 dBm	-13.6 dBm	0.83×0.83 mm^2	5.35 GHz	[39] 2004
0.18µm	1.2 V	12.5 mW	1.6 dB	17 dB	-8.8 dBm	NA	0.9×0.5 mm^2	5.3 GHz	[40] 2004

N.A: Not Available

Table 3.9 provides comparative results with recent CMOS LPLV low noise amplifier designs. Most of the designs used cascode inductor source degeneration topology, especially for the low power consumption design. This coincides with the previous low noise amplifier topology analysis. As we can see, the proposed LPLV LNA consumes less power while meeting the specification for an earpiece. It could be the suitable LNA design, drawing very small current, for a CMOS earpiece of a wireless hearing aid system.

Above comparison shows that the overall performance of the proposed LNA for wireless hearing aid device stays among the state-of-the-art in the current CMOS RFIC evolutions.

3.7 Conclusions

A 0.95mW single-ended cascode inductor source degeneration LNA design has been fabricated in CSM CMOS 0.18 μm technology. The tested results show a forward gain (S21) of 11.9 dB with a noise figure of 2.41 dB while drawing 0.95 mW from a 1.0 V power supply. The IIP3 and P1dB of LNA are 0.7 dBm and -12 dBm, which predict a good linearity. This tested LNA has very low power consumption, compared to other CMOS LPLV LNA designs, which can be built in the wireless hearing aid earpiece.

Chapter 4 Noise Cancellation in Wireless Hearing Aid device

4.1 Introduction to Background Noise Cancellation

When a hearing-impaired person is in a noisy environment, even with a HA, the surrounding noise may interfere the desired voice that makes the hearing-impaired person has difficulty to discern what he needs. So the hearing aid should only amplify what the hearing-impaired person need to hear and reduce what hearing-impaired person not want to hear. Normal background noise cancellation has its limitation on noise performance, so further better noise cancellation needs to be studied.

Because of the noise problem degrades the quality of hearing aids performance, the noise cancellation is a primary concern to do the speech enhancement. Noise cancellation study has been carried on for many years.

Filters are the most common blocks to cancel the noise for many years. Filter bank design [14], shown in Fig. 4.1, and comb filter design [41] are two mainly filter design for noise cancellation.

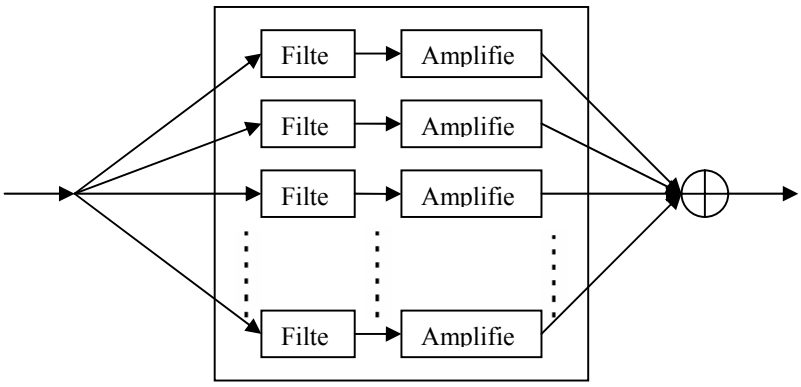


Fig. 4.1 Filter bank for noise cancellation

Filter bank uses many band pass filters parallel together. These filters' pass bands cove the whole system band, but each filter's pass band dose not cross cover. Each filter has its own gain, which can be set by designers. There are two advantages for this kind filter banks. On one hand, if the specific noise frequencies are known, then the noise can be filtered out. On the other hand, the gain of each filter in the filter bank can be set with different value in order to give the maxim gain of signal frequency band and the minimum gain of noise frequency band. However, there are also some disadvantages of this method. For example, the noise property should be known in advance. Then the parameters of the filter bank can be determined. But it is not practical, because the real situation for hearing aid device is unknown to designers. In the similar way, the comb filter method should first detect the noise fundamental frequency, and then filter the noise from the input voice signal [42]. Another limitation is that if the noise frequency band is the same with the desired voice frequency band, it is not easy to get rid of noise from the hearing aid input.

Wavelets analysis is another method used in noise cancellation [15]. The wavelet filter is designed to cancel the noise as follows. Firstly, a fundamental wavelet, such as Daubechies Wavelet or Meyer Wavelet, is selected. Secondly, use this selected fundamental wavelet to analyze the received audio signal. Finally, filter out the noise from the received signal. However, this method has its disadvantages. How to select the wavelet for different hearing-impaired persons to cancel the noise is a problem. Different wavelet has different cancellation effect and they are under the research.

Fuzzy math can be also used in hearing aid for noise cancellation [43]. It has its own advantages. It gives more flexibility to determine the parameters of HA, which can

improve the HA performance. However, the membership functions for each fuzzy variable are more difficult to be determined, because each hearing-impaired person's situation is different. Normally, the functions are simplified by just selecting triangle wave functions. Sometimes, this kind of function is not exact to reflect the real change of fuzzy variable. Moreover, how to determine the boundary of each fuzzy variable at different fuzzy zone is another problem. All these problems need practical experience on each case for different hearing aid users.

The concept of adaptive noise canceling was proposed by Widrow. Basically, the idea is to subtract out a filtered version of some signals, known to be correlated with noise, from the noise corrupted desired signal. The filter is continuously modified by some algorithm so as to optimize some performance criterion on the resulting signal. A generalization of the work of Widrow in the context of multichannel noise canceling was carried out by Griffiths [44]. Beamforming method is one of the adaptive noise cancellation methods [12], [21]. Shown in Fig. 4.2, *s(n)* is the wanted signal and *v(n)* is the interference/noise. Device A and B are omni-direction microphones without loss. Voice signal and interference come to the microphones with different directions. The angel of signal is zero. The angel between voice signal and interference is θ. Voice signal and interference are both band limited signals with the assumption that their center frequencies are the same. If the phase shifter is chosen suitably, the interference can be cancelled. On the other hand, the beamformer output *e(n)* is nonzero. The envelope of output still holds the signal information. This beamformer allows the signal to pass, while cancels the interference at the same time. In addition, by increasing the number of elements in the array, better approximations to the desired beam pattern can be achieved.

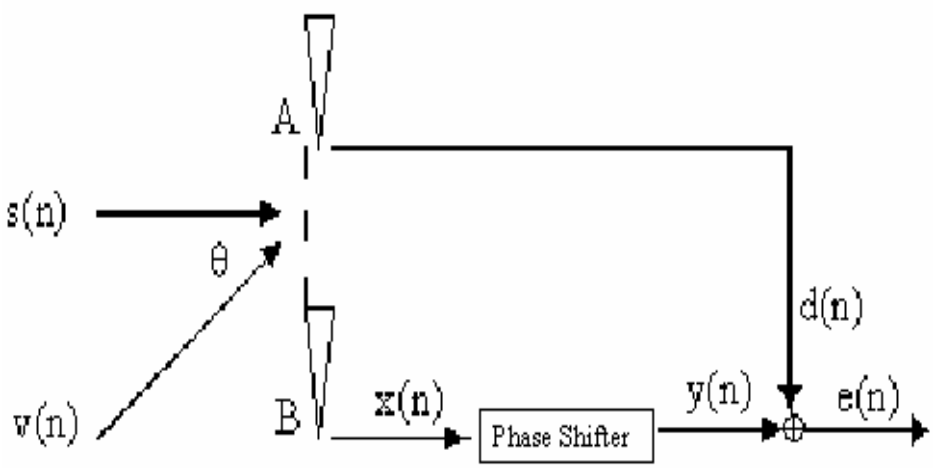


Fig. 4.2 Two-element beamformer

Beamforming method uses multimicrophones not only to cancel the noise but also to locate the sound. So beamforming method is a more efficient method for noise cancellation in hearing aid device [12], [21], which is based on the constrained adaptive beamformer of Grifliths and Jim [44]. A two-element microphone array beamformer is shown in Fig. 4.3 [12].

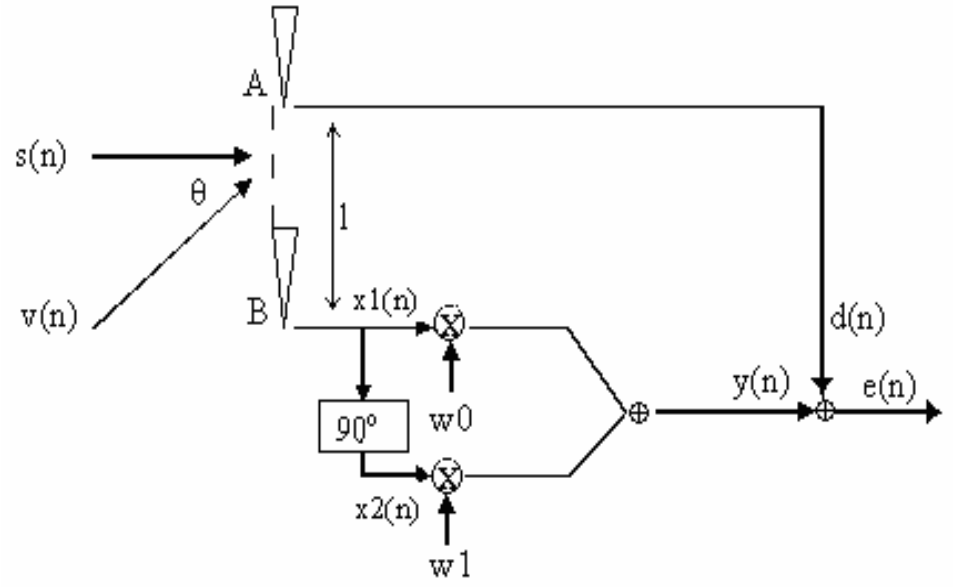


Fig4.3 A two-element microphone array beamformer

In Fig. 4.3, s(n) is the voice signal and v(n) is the noise. Device A and B are two omni-direction microphones without loss. The voice signal and the noise come to the microphones with various directions. The direction angel of voice signal is zero. The direction angel between voice signal and noise is θ. x1(n), x2(n), y(n) and d(n) are random signals combined audio signal and noise. w_0 and w_1 are two coefficients which are determined by output e(n) from solving Wiener-Hope Equation [45]. From the theoretic calculation, with all the equations [12], the signal-to-noise power spectral density ratio at the noise canceller output is equal to the inverse of the signal-to-noise power spectral density ratio at the reference input. This means that if the signal-to-noise power density ratio at the reference input is low, then a good cancellation of the noise at the output can be expected. However, the maximum gain of signal with different direction angle passing through this beamformer is not at the point of direction angle with zero degree in some cases. The proof is shown in Appendix B, which shows that the maxim or minim value is not at direction angle with zero degree.

As an example, in MATLAB, the voice and noise are all band limited signal. Using only one beamforming path as shown in Fig. 4.3, the simulated plot is shown in Fig. 4.4 for a set of input parameters such as the direction angle difference between noise and arrival signal, variance coefficients of signal and noise and centre frequency etc. The signal source direction angle is fixed at 0° and the noise source direction angle is varied from 0° to 360° by a step of 1°. The curve in Fig. 4.4 shows the directivity pattern of two-element beamformer. In Fig. 4.4, the gain at zero degree is the signal gain, and the gain at other degrees is the noise gain. It is observed that the signal gain is less than noise gain, when input noise direction angle is between the range of about 20° to 160° and the

signal gain is more than noise gain when input signal direction angle is between the range of about 0° to 20° or 160° to 180°. So when the signal and noise are received together from a difference in direction angles, the amplification in signal and reduction in noise is observed. However, as shown in Fig. 4.4 the noise cancellation performance is not good enough for the noise direction angles from 180° to 360°. It has a maxim value from 270° to 360°, which is about at 340° in Fig. 4.4. That means if noise comes from 340°, noise has the possibility to be amplified and the strength of noise is larger than the strength of signal. The noise can make a heavy distortion on the signal.

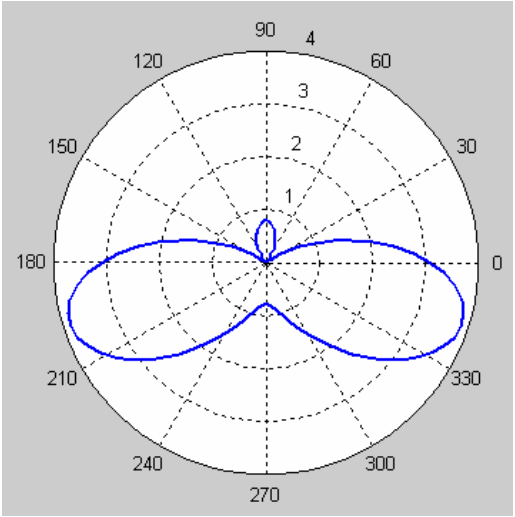


Fig. 4.4 Directivity pattern of two-element beamformer

As an attempt to handle such case in a better way, a modified two-element beamformer is provided in Fig. 4.5. In the similar as in Fig. 4.3, s(n) is the voice signal and v(n) is the noise. Device A and B are two omni direction microphones without loss. The arrival direction angel between voice signal and noise is θ. x(n), $\tilde{x}(n)$, y(n), $\tilde{y}(n)$, z1(n), z2(n), d1(n) and d2(n) are random signals combined audio signal and noise. w_0, w_1, w_2 and w_3 and are four coefficients which are determined by output before compared from solving Wiener-Hope Equation.

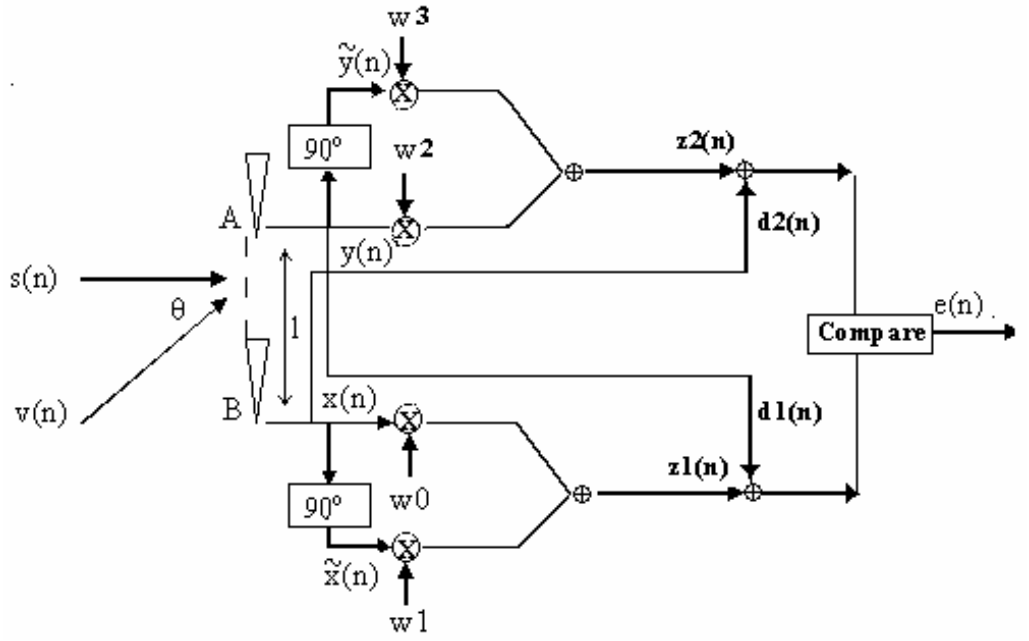


Fig. 4.5 A modified two-element beamformer

Shown in Fig. 4.5, two independent beamforming paths are used and then their outputs are compared to select the better one. The new beamforming path is very similar with the old one. They are symmetric. The comparison of two beamforming path is to select the output with smaller output power. It, thus, enable the maxim gain occurs only when the signal with zero degree arrival direction angle passing through this beamformer. This promises better noise cancellation performance than that in the case of Fig. 4.3.

As an example, the modified two-element beamforming method as shown in Fig. 4.5 is used and the achieved simulated plot using enhanced method of beamforming is shown in Fig. 4.6. The signal source direction angle is fixed at 0° and the noise source direction angle is varied from 0° to 360° by a step of 1°. The curve in Fig. 4.6 shows the directivity pattern of modified two-element beamformer. In Fig. 4.6, the gain at zero degree is the signal gain, and the gain at other degrees is the noise gain. The noise cancellation performance is symmetrical and promises better than that as shown in Fig. 4.4. The noise and signal sources used in MATLAB simulation are defined as random

signals i.e. the magnitude and frequency is varied with time. As shown in the Fig. 4.6, this modified two-element beamformer overcomes the shortcoming of only one path beamforming. For instance in Fig. 4.4, the gain at 330°, which is the noise gain, is more than 3. The gain at 0°, which is the voice gain, is about 3. So there is no noise cancellation. However, in Fig. 4.6, the gain at 330°, which is the noise gain, is less 3. The gain at 0°, which is voice gain, is still about 3. The noise cancellation works. So noise cancellation performance is better than the previous one.

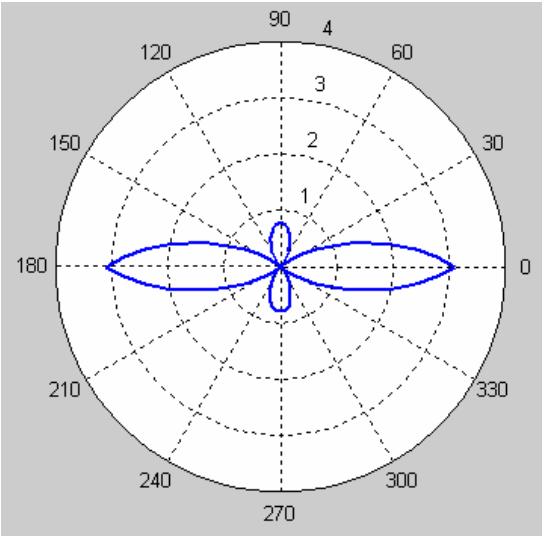


Fig. 4.6 Directivity pattern of modified two-element beamformer

In Fig. 4.6, the gain has its maxim value only in 0° or 180°, which is the voice signal direction angle. Thus, the surrounding noise can be reduced and the voice signal can be amplified when they pass from this noise cancellation system.

4.2 Behavior Model Development

While having better ways of canceling the noise, it needs to be verified before physical implementation for wireless hearing aids. The behavior modeling has been a

conventional method to verify the functionality of the systems during the design and implementation phase.

As a case study, the model is constructed to be amenable with hearing aid devices. The front end of which is shown in Fig. 4.7.

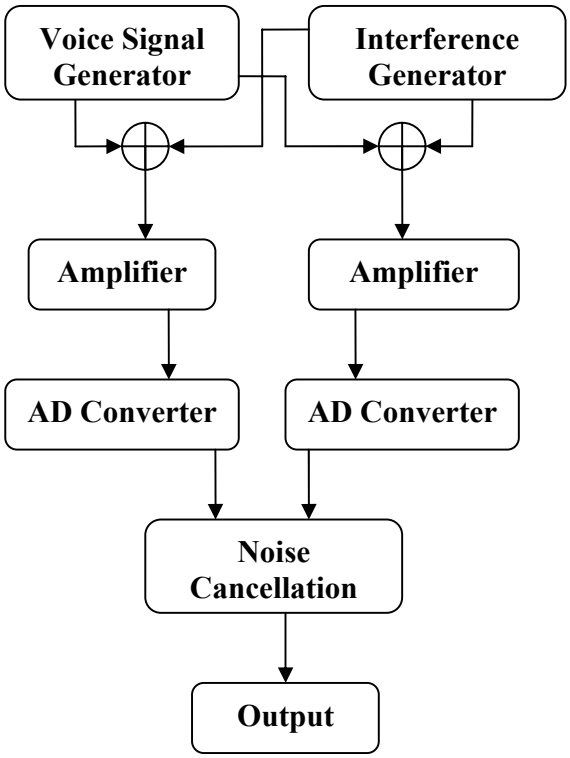


Fig. 4.7 A typical system using noise cancellation in an audio device

For instance, a typical hearing aid system has its front stage consisting of (i) signal receivers i.e. microphones (ii) amplifiers (iii) A/D converters and (iv) noise cancellation block. Its CAD compatible model enabling behavioral simulation is constructed as follow. It includes following steps: (i) The voice signal generator and interference generator are used to model the received voice and noise respectively, where both sources are defined as random signals in the frequency band of 0 kHz to 6 kHz which falls under audio range. (ii) The voice signal and the noise are combined and then transmitted after amplification

into A/D converter to get the digital signals. (iii) The noise cancellation unit is used to process the digital signals using modified two-element beamforming method.

To develop the behavioral model for noise cancellation, for the modified two-element beamforming method as shown in Fig. 4.5, compatible to MATLAB and ADS, the only one independent beamforming path bock diagram of the modified two-element beamforming method is shown in Fig. 4.8.

The gain of the amplifier in the behavior model is considered programmable. For simulation purpose, the sampling frequency of the 8 bit A/D converter used is taken as 100 kHz, which is higher enough than the maxim frequency of the voice signal, and the reference voltage for behavior model of AD converter is defined as 1.0 V.

In MATLAB, the behavior model is realized by programming the corresponding equations [12]. While in ADS, the behavior model is built using the modeling features of the software of ADS Agilent Ptolemy in behavior level [46]. All the functional blocks such as addition, multiplier and expectation are defined in ADS Agilent Ptolemy using equivalent models in ADS library.

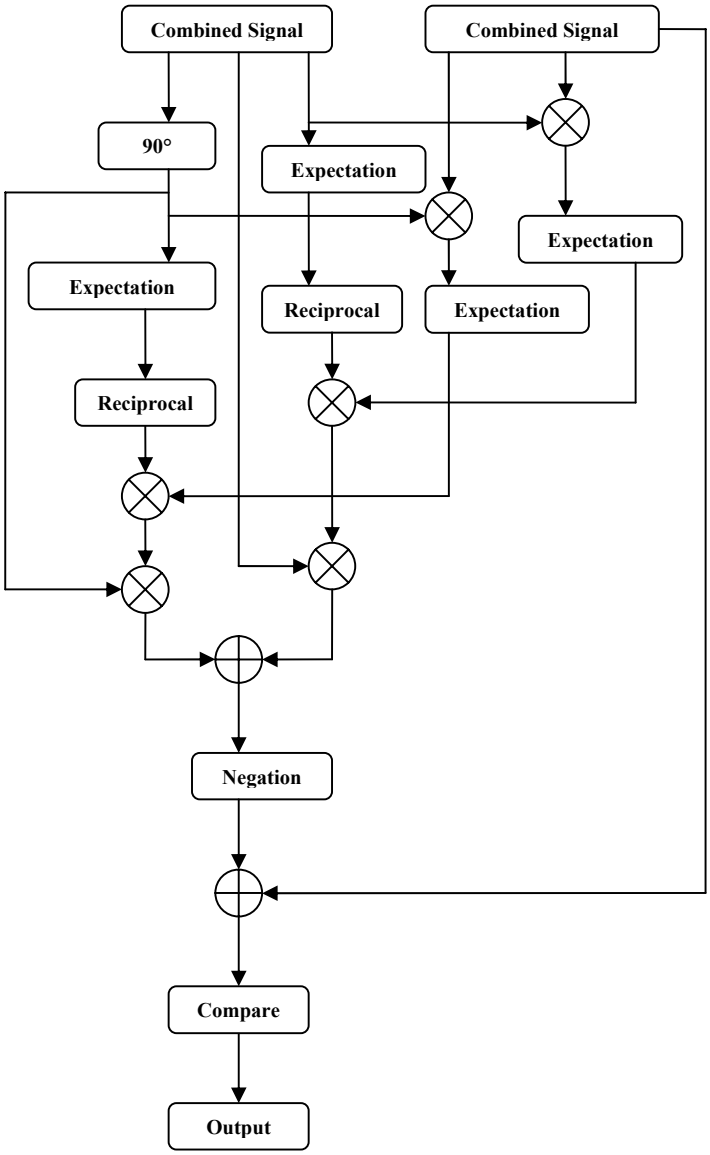


Fig. 4.8 Extended block diagram of single path beamforming

The EDA software ADS has the feature for behavior models and circuit model building [46]. The above discussed behavioral models are also made ADS compatible which are found suitable for simulating audio devices consisting of RF, analog and/or digital blocks e.g. wireless hearing aid.

4.3 Behavioral Simulation and Model Validation

4.3.1 MATLAB Simulation Results

The modified two-element beamformer can do the noise cancellation. In this behavior model, when the angle between voice and noise θ_0 which is for constructing model, input SNR, variance of signal σ_α and variance of noise σ_β or central frequency of signal and noise changes, the noise cancellation effects are different. For further study on behavior model for wireless hearing aids, the parameters in the model need to be changed in order to optimize the noise cancellation effects.

4.3.1.1 Changing the direction angle between noise and voice signal θ_0 which is for constructing model

The direction angle between noise and voice signal θ_0 for constructing model is selected as 10°, 30°, 45°, 60°, 75° and 90° in the simulation. Because of the symmetry, the beamforming results of other θ_0 values, such as -60°, -30°, are similar with previous θ_0 values, such as 60°, 30°. The simulation results are shown in Fig. 4.9. The simulation results are provided with typical parameter values. That is to say, the sampling frequency is 100 kHz; the central frequency of signal and noise is 3 kHz; the variance of the desired signal σ_α is 0.01; the variance of the noise σ_β is 1.0; the input SNR is -4.59dB.

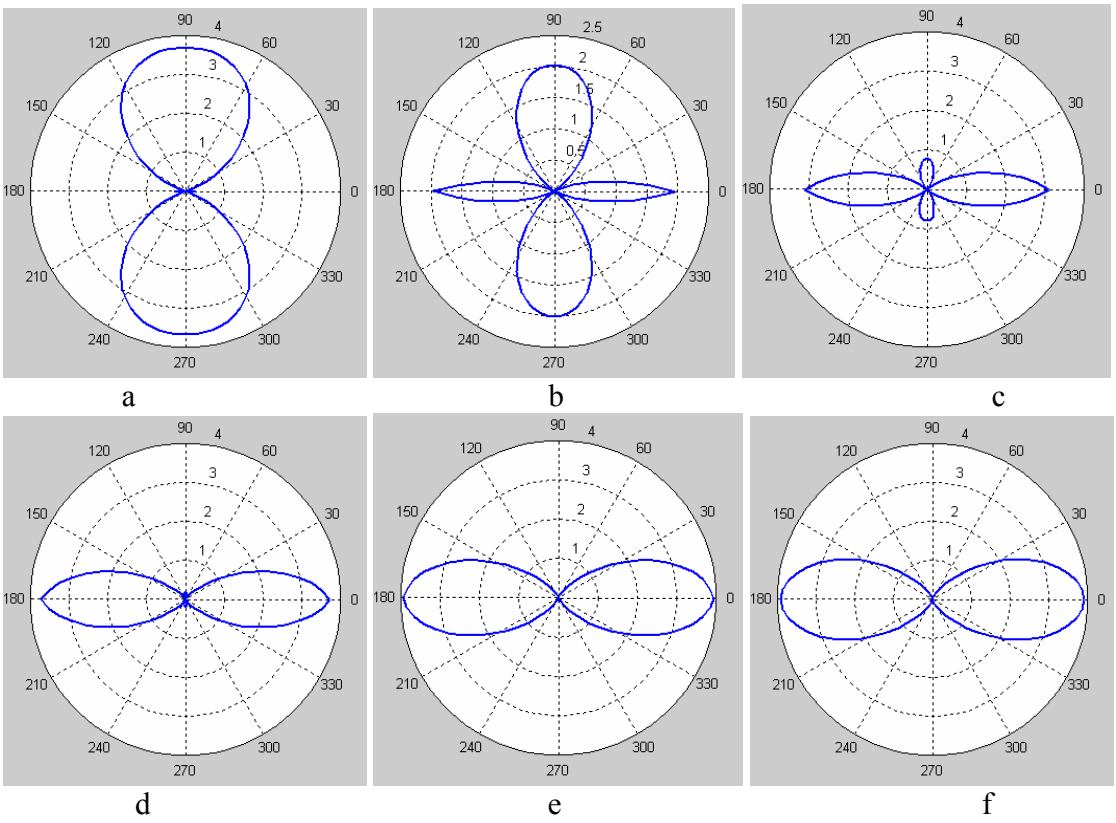


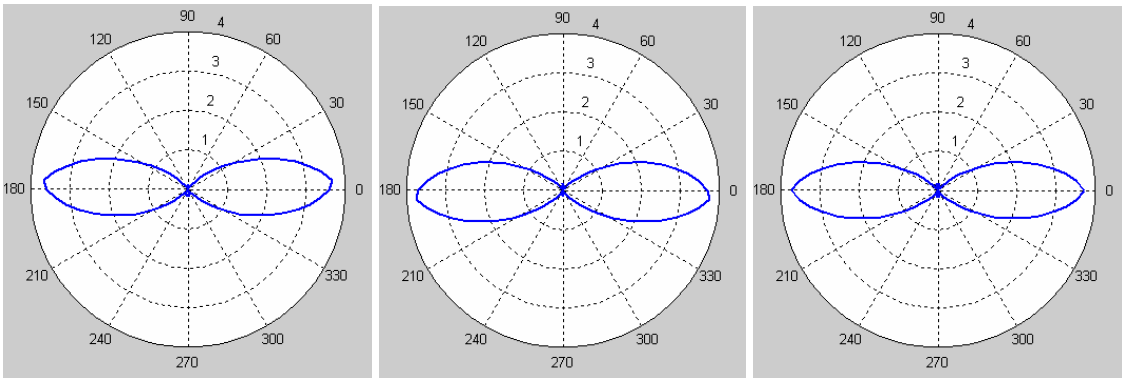
Fig.4.9 Directivity pattern of modified two-element beamformer with different direction angle between noise and voice signal θ_0 which is for constructing model
a. θ_0=10° b. θ_0=30° c. θ_0=45° d. θ_0=60° e. θ_0=75° f. θ_0=90°

As shown in the above figures, when the angle θ_0 is very small, i.e. θ_0=10°, this beamformer can not detect the desired signal, which comes from 0°. On the contrary, the noise is amplified, which is not we want. When the angle θ_0 increases, i.e. θ_0=30°, this modified two-element beamformer can detect the desired signal from noise. However, if the noise comes from 60° to 120°, the noise strength can not be reduced. When the angle θ_0 becomes larger, the simulation curve becomes wider. That means when θ_0=60° the desired signal can come from -30° to 30° to get a better noise cancellation performance; when θ_0=90°, the desired signal can come from -45° to 45° to get a better noise cancellation performance. At the same time, the strength of noise coming from 90° through the modified two-element beamformer when θ_0 set as 90° is smaller than the

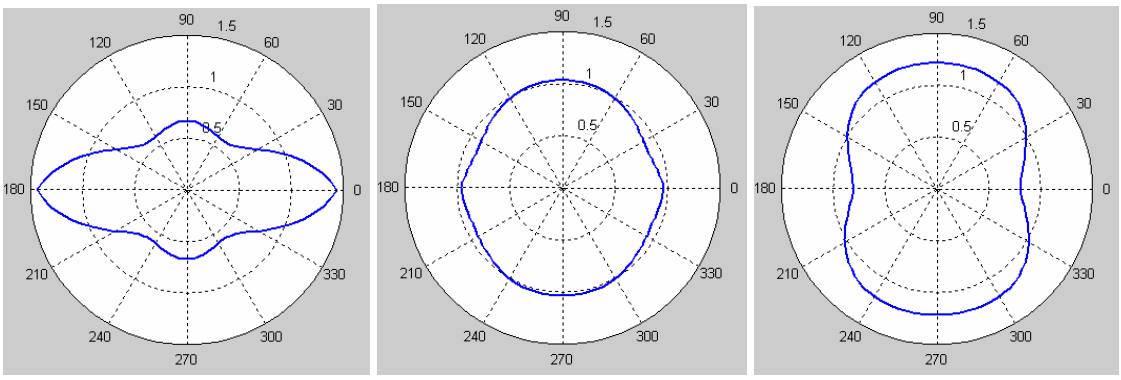
strength of noise coming from same direction when θ_0 set as 60°. So it is a trade-off when selecting θ_0. If the small coming angle variance of desired signal is needed, θ_0 can be set with a small value, such as 45°. Otherwise, θ_0 can be set with a large value, such as 90°. From the simulation results, this parameter is quite critical. Normally θ_0 can be selected as 60°.

4.3.1.2 Changing the input SNR

Hearing aids will be used in different environment, especially used in a noisy environment. Sometime, the hearing aids are used in a quiet environment. The input SNR is more than 0 dB. On the contrary, if the hearing aids are used in a noise environment, in this kind of situation, the input SNR is perhaps less than 0. So the noise cancellation performances need study when changing the input SNR. The simulation results are shown in Fig. 4.10. The AD converter sampling frequency is fixed as 100 kHz. The central frequency of signal and noise is 3 kHz. The variance of the desired signal σ_α is 0.01. The variance of the noise σ_β is 1.0. The direction angle between signal and noise for constructing model θ_0 is set as 60°.



a b c



d e f

Fig. 4.10 Directivity pattern of modified two-element beamformer with different input SNR

a. SNR=-9.2185dB b. SNR=-7.8148dB c. SNR=-4.6028dB d. SNR=-1.3445dB
e. SNR=0.0165dB f. SNR= 4.6184dB

As shown in the above figures, if the magnitude of noise is higher than the magnitude of voice signal, that is to say the input SNR less than 0dB, the noise cancellation can improve the SNR. It is a verification of the theoretic calculation [12]. However, if the magnitude of noise is higher than the magnitude of voice signal, i.e. input SNR is greater than 0dB, the cancellation result is not good. So a detection to decide whether or not to use this noise cancellation is needed before the noise cancellation for the proposed wireless hearing aids.

4.3.1.3 Changing the variances of signal σ_α and the variances of noise σ_β

Voice signal and noise are both random in audio frequency band. The variances of signal σ_α and the variances of noise σ_β are random also. So it is expected to get the better noise cancellation with the different variances of signal σ_α and the variances of noise σ_β. The simulation results are shown in Fig. 4.11. The sampling frequency is still as 100 kHz. The central frequency of signal and noise is 3 kHz. The input SNR is less than 0 dB. The direction angle between signal and noise for constructing model θ_0 is fixed as 60°.

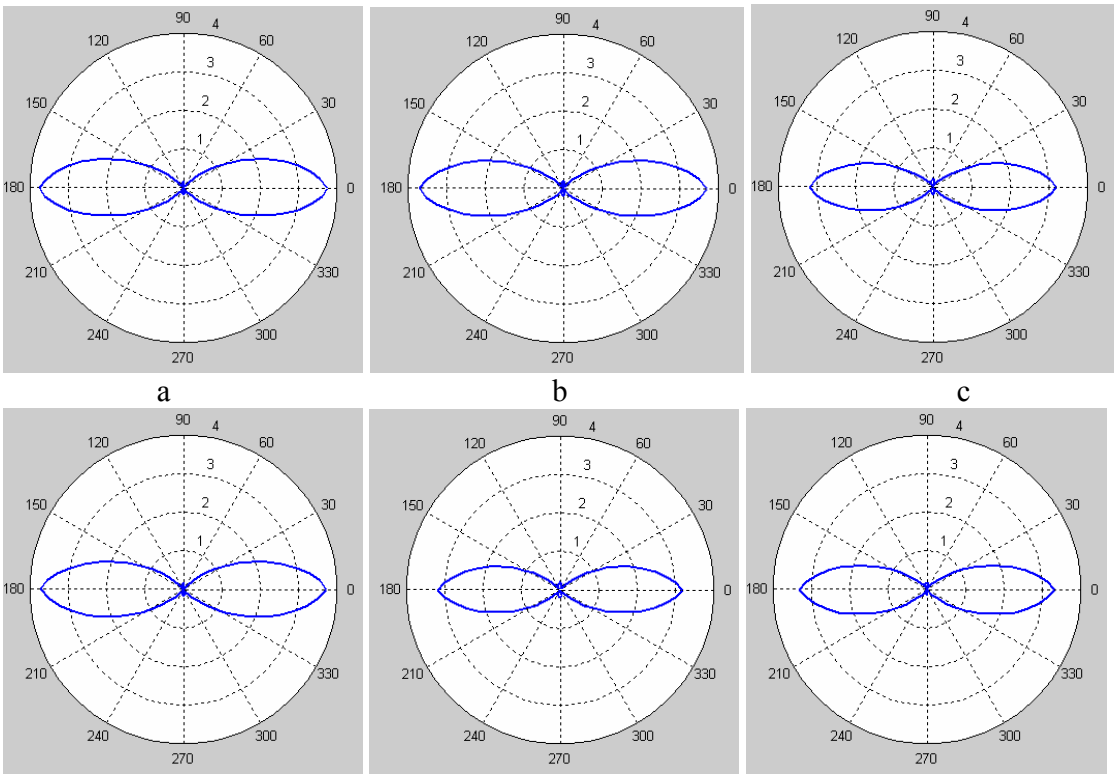


Fig. 4.11 Directivity pattern of modified two-element beamformer with different variances of signal σ_α and different variances of noise σ_β

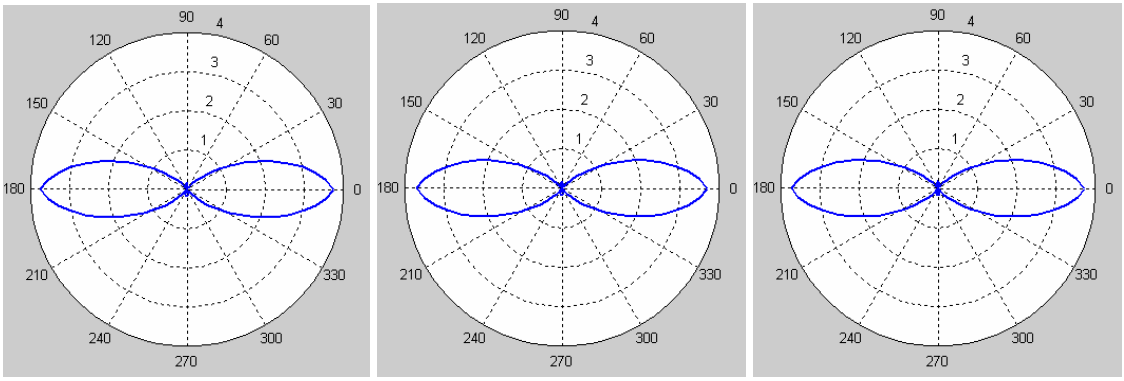
a. σ_α=0.01, σ_β=1.0 b. σ_α=0.01, σ_β=0.1 c. σ_α=0.01, σ_β=0.01
d. σ_α=0.1, σ_β=1.0 e. σ_α=0.1, σ_β=0.1 f. σ_α=0.1, σ_β=0.01

As shown in the above figures, the variances of signal σ_α and the variances of noise σ_β have little effect on the performance of noise cancellation for typical values. That means that the noise cancellation can be done in variant variances of signal and noise situations. This is an advantage for this noise cancellation method.

4.3.1.4 Changing the center frequency of signal and noise

Because audio signal and noise are both band limited random in audio frequency band, we can assume that the center frequencies of audio signal and noise are same. The center frequency of signal and noise can be selected as the middle value of the minim and maxim audio signal or noise frequency. The simulation results are shown in Fig. 4.12.

The center frequency of signal and noise is selected simplified same in the simulation. The sampling frequency is 100 kHz. The variance of the desired signal σ_α is 0.01. The variance of the noise σ_β is 1.0. The angle between signal and noise for constructing model θ_0 is 60°. The input SNR is less than 0 dB.



a b c

Fig. 4.12 Directivity pattern of modified two-element beamformer with different center frequency of signal and noise

a. Central frequency is 3 kHz b. Central frequency is 5 kHz

c. Central frequency is 10 kHz

As shown in the above figures, the central frequencies of signal and noise have little effect on the performance of noise cancellation, as long as the sampling frequency is satisfied with the sampling theory. It, thus, makes not too difficult for the AD converter design in the proposed wireless hearing aids.

4.3.2 ADS Simulation Results

The simulation of modified two-element beamformer method is performed also in ADS as well keeping in view that the ADS is a better choice for the whole system simulations, in general. The advantage of behavior model building in ADS is the co-simulation in ADS with other circuit level blocks of hearing aid devices. This advantage

of building modified two-element beamformer behavior model in ADS will be shown in the following session later.

The proof of this behavior model has been given in MATLAB. Hence in ADS, only the determined voice signal and noise are selected to simulate and test the behavior model in ADS for simplification.

In ADS, the voice signal and the noise are single tone sinusoidal signals. The frequency of noise is fixed. The frequency of voice signal can be changed. At the same time the magnitudes of voice signal and the noise can also be changed. The noise signal frequency is taken as 1 kHz. The voice signal frequency and magnitude can be changed. θ_0 is set as 45° and central frequencies of desired signal and noise are 3 kHz.

Some results are given in Fig. 4.13 and Fig. 4.14, which show the differences in output and input SNR with respect to the variation in input signal frequency and input SNR respectively.

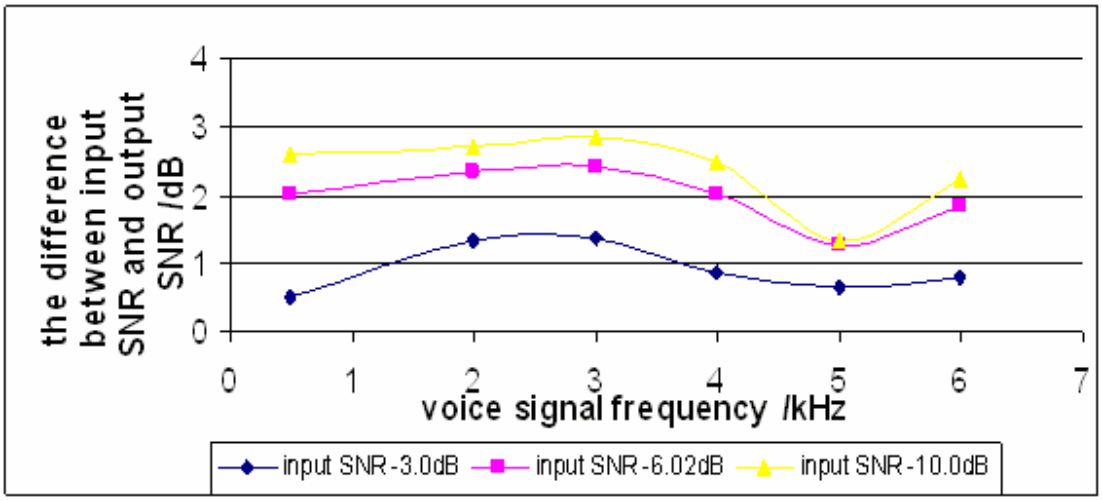


Fig. 4.13 Difference between input SNR and output SNR of modified two-element beamformer for different frequency

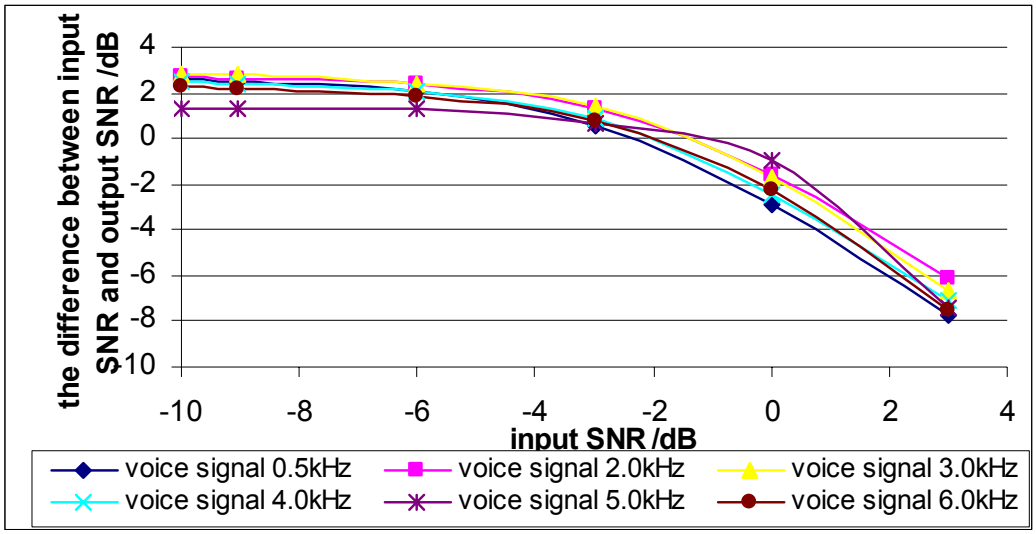


Fig. 4.14 Difference between input SNR and output SNR of modified two-element beamformer for different input SNR (noise frequency is at 1 kKHz)

Fig. 4.13 reflects that the difference between input SNR and output SNR changes not too much with the variance of frequency. Fig. 4.14 reflects that the difference between input SNR and output SNR decreases with increase in the input SNR. It may, however, be noted from the above results that there is an improvement in output SNR when input SNR is less than certain limit i.e. in this case about -2 dB. This value is a little difference compared the simulation results in MATLAB. In MATLAB simulation, the voice signal and noise are both random and their correlation is zero. However in ADS, voice signal and noise are determined and their correlation in none zero. So there is a little difference in simulation results.

These results are observed in compliances with the modified method of noise cancellation as discussed above and also with the results achieved using MATLAB. Some useful results can be got from the simulation results.

(1) In audio frequency band, this modified two-element beamformer can do the noise cancellation.

(2) This modified two-element beamformer for noise cancellation can be used only when noise strength is higher than voice signal strength.

(3) In this modified two-element beamformer, the angle between voice and noise θ_0 which is for constructing model and input SNR affects the noise cancellation performance. However, the variance of signal σ_α and variance of noise σ_β or central frequency of signal and noise has little effect on noise cancellation performance.

4.4 Noise Cancellation Simulation in Wireless Hearing Aids

In the above section, the behavior model simulation results for noise cancellation are discussed. However, what we concern more is how the noise cancellation effect is when building in the typical wireless hearing aid using the proposed method of noise cancellation. So the behavior model simulation with other circuit level block is needed. The whole wireless hearing aid construction is one kind of typical hearing aids, as shown in Fig. 1.5.

Nowadays, most researchers use PSPICE or MATLAB for behavioral modeling and system simulation. However, due to the complexity lying in our system, neither of them fits our requirements. The SIMULINK tool in MATLAB is a powerful simulation tool for DSP and behavioral modeling, whereas it does not provide adequate help in IC design and high frequency RF communication. Some researchers chose PSPICE for circuit system simulation, which is good at analog circuit analysis but helps little in incorporating digital signal processing and RF wireless communication into our system.

Most difficulties are solved in ADS, which is a powerful electronic design automation software system [46]. The Agilent Ptolemy provided by ADS can include co-

simulation of DSP blocks with the RF and analog simulators within the same schematic. The Ptolemy signal processing simulator has its roots at the University of California at Berkeley and it modifies the proven Synchronous Dataflow domain to include timed components. This Timed Synchronous Dataflow domain enables fast RF simulation, integration with signal processing simulation, and co-simulation with Agilent circuit simulators.

With the help of Agilent Ptolemy, the system simulation between different domains becomes easy and straightforward. Also, any IC block design can replace the corresponding behavioral models and test its applicability and performance within the entire system.

Voice signal and noise can the same as the previous used in ADS. Behavioral modeling of electric-acoustic transducers such as microphone and speaker is built using data from actual measurement. Frequency responses of microphone and speaker are collected from real measurement on receiver model BK1600 and microphone model EK3024 [47] and stored in an external data file. EDA software ADS provides Data Access Component model which can set the parameter of the specified component according to external data files [46].

Generic models of RF system are available in ADS library [46]. A super-heterodyne receiver structure is used, along with QPSK modulation scheme. The model simplifies communication channel, assuming it is ideal within 1 meter's range. One of the block in RF transceiver, LNA, is implemented in circuit level with transistors, resistors, inductors and capacitors. The design descriptions are presented in the next chapter.

The Ptolemy simulation requires a small simulation time step for good accuracy. However, the sampling rate of AD converter is around 30K Hz. The inconsistency brings problem with the parameter setup of AD converter. To solve the problem, a Down-sampler model is added after the AD Converter, which reduces initial AD sampling rate of 1/Time step, to desirable 32 KHz [46] .

DSP noise cancellation algorithm is first realized in MATLAB, and then transplanted to ADS using functional blocks provided by ADS library.

The noise cancellation simulation results are shown in Fig. 4.15 and Fig. 4.16. During simulation, the input signal comprises both signal and interfering noise. Noise cancellation is evaluated by comparison between system input and output. To better examine the SNR improvement with input SNR, a series of simulation are processed using different input SNR.

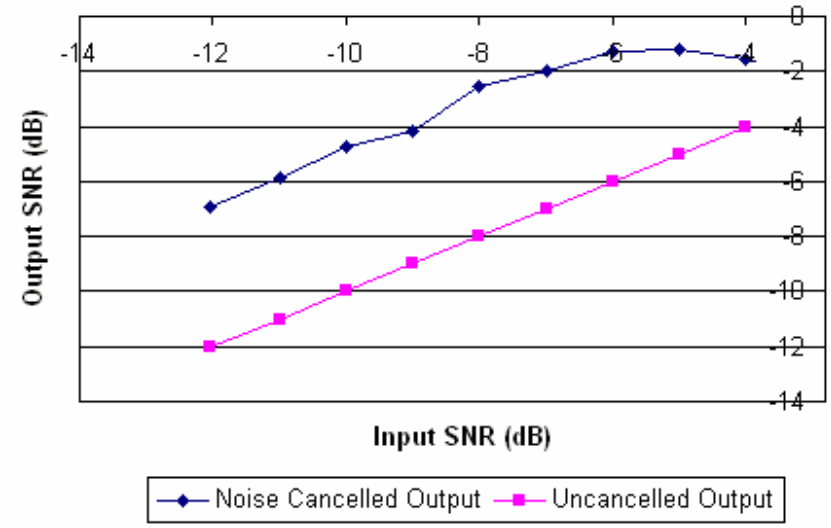


Fig. 4.15 Output SNR versus input SNR for typical wireless hearing aids

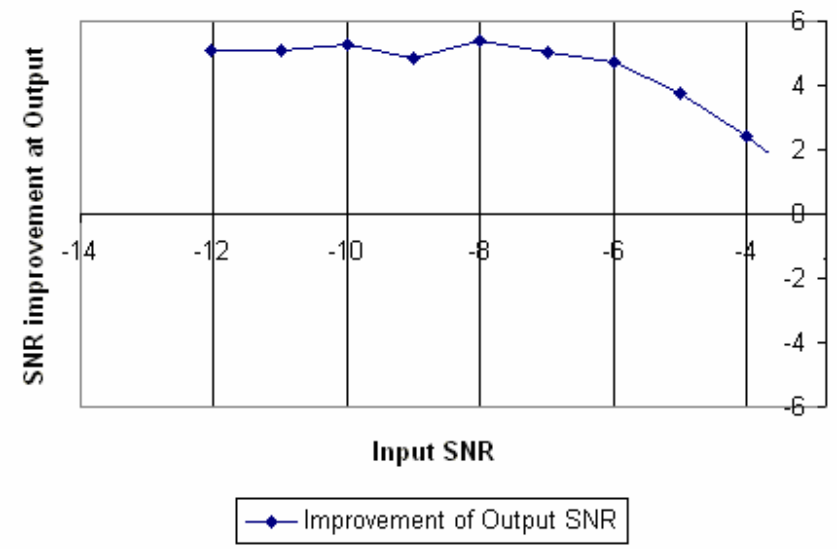


Fig. 4.16 Output SNR improvement for typical wireless hearing aids

By comparing the two curves in Fig. 4.15, one can easily tell that SNR is improved when the input noise strength is higher than the desired signal strength. Moreover, Fig. 4.16 shows the improvement of SNR (difference between input SNR and output SNR) increases when input SNR decreases.

4.5 Conclusion

A modified two-element beamformer method for noise cancellation is proposed, which can overcome the limitation of two-element beamforming method [12] . It is supported with a behavior model for noise cancellation in audio devices such as wireless hearing aid. Equivalent behavioral models are generated for carrying out simulation in MATLAB and ADS. The simulation results show the enhancement in the noise cancellation using the proposed scheme for noise cancellation. The proposed noise cancellation method functions properly for the hearing aid device. It can suppress the noise from certain angels. Noise cancellation is mainly required when noise strength is

higher than voice signal strength. The input SNR, variances of signal and noise, sampling frequency, the directional angle between signal and noise for construction model affect the noise cancellation performance. The direction angle between voice signal and noise θ_0 should be selected greater than 30°, otherwise the noise cancellation is not effective enough.

An ADS set-up whole wireless hearing aid system simulation is also developed in this thesis. Using the set-up, system behavioral checks are made. The simulation results show this modified two-element beamforming method can be implemented in wireless hearing aids.

Chapter 5 Conclusions and Future Works

5.1 New Development

The followings are the main two novelties in this research:

1. A single ended low voltage and low power consumption LNA was implemented in CSM 0.18 μm CMOS technology packed and tested on printed circuit board. The designed LNA provides state-of-art performance. It operates at 1.0 V supply and drains 0.95 mA only. The LNA provides a forward gain of 11.91 dB with a noise figure of only 2.41 dB operating in the 0.9 GHz band. The IIP3 is 0.7 dBm and the P1dB is -12 dBm.

2. A modified two-element beamforming method for the background noise cancellation is provided and applied. The noise cancellation performance of the two-element beamforming method is not good enough for the noise direction angles from 180° to 360°. That means if noise comes from certain angle, such as 340°, noise has the possibility to be amplified and the strength of noise is larger than the strength of signal. The noise makes a heavy distortion on the signal. However, the proposed modified two-element beamforming method overcomes the above limitation. The desired signal can get the maximum gain, which arrives with 0° direction angle. It is shown that with proposed method, the noise gain is less than the desired signal gain.

5.2 Main Conclusions

The LPLV LNA was designed and tested. This LNA consumes very small power consumption compared to other CMOS LNA designs keeping in view frequency and NF. The design also meets requirements on noise, linearity and gain for 0.9 GHz low power

applications, specifically for CMOS wireless hearing aids. The tested LNA performance is promising be embedded in earpiece of wireless hearing aids.

Modified two-element beamforming method for noise cancellation is discussed, which can reduce the surrounding environment noise. The verification of this method is implemented in EDA software with behavior model. It is used when the noise strength is higher than the desired signal strength. The input SNR, variances of signal and noise, sampling frequency, the directional angle between signal and noise for construction model affect the noise cancellation performance. The noise cancellation method can be used in wireless hearing aid to get a better performance.

5.3 Future Works

The LPLV LNA was designed and tested. The input matching is not good enough. In order to improve the input matching, more parasitic effects should be considered in the simulation, such as PCB parasitic effects, off-chip components parasitic effects.

Although the noise cancellation method is discussed, the implementation of this method in digital circuit is needed for future works.

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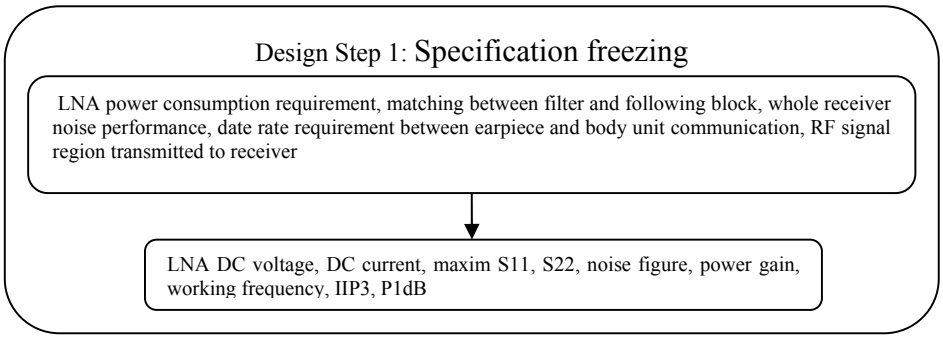
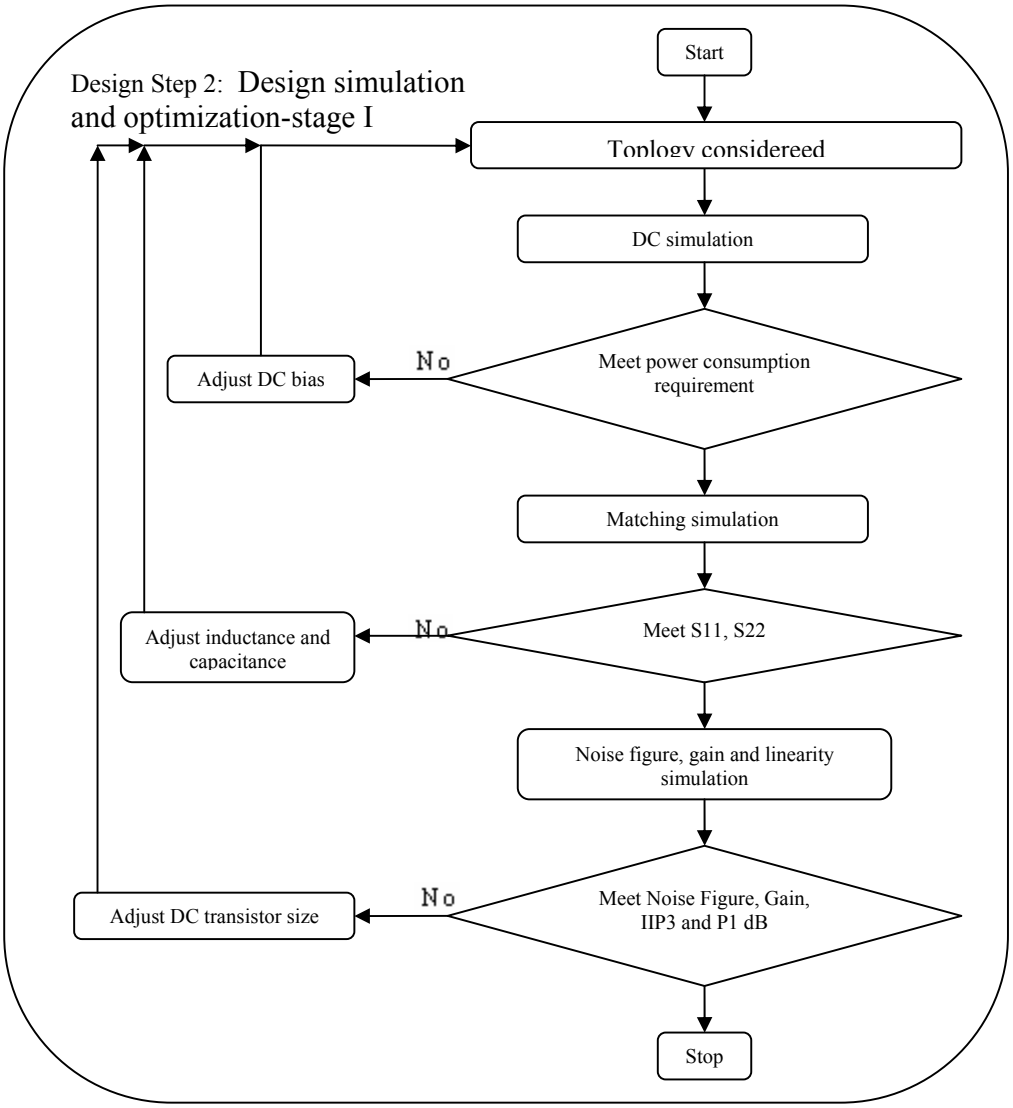
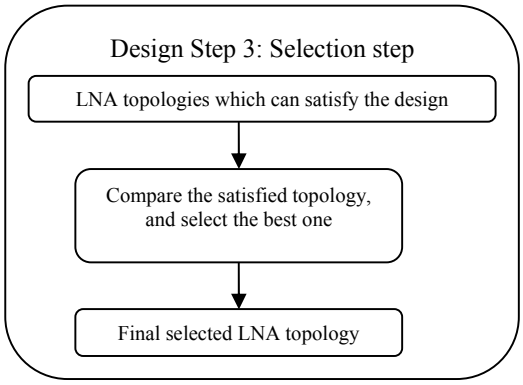
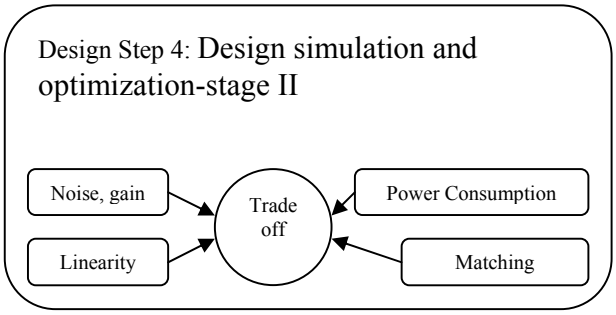
Appendices

A. LPLV LNA Design and Optimization Steps




Design Step 2: Design simulation and optimization-stage I
Start
Toplogy considereed
DC simulation
Meet power consumption requirement
No
Adjust DC bias
Matching simulation
Meet S11, S22
No
Adjust inductance and capacitance
Noise figure, gain and linearity simulation
Meet Noise Figure, Gain, IIP3 and P1 dB
No
Adjust DC transistor size
Stop


Design Step 3: Selection step
LNA topologies which can satisfy the design
Compare the satisfied topology, and select the best one
Final selected LNA topology


Design Step 4: Design simulation and optimization-stage II
Noise, gain
Linearity
Trade off
Power Consumption
Matching

B. Proof of Two-element Microphone Array Beamformer Limitation

Assumes voice signal $s(n) = \alpha(n)\cos n\omega_0$, noise $v(n) = \beta(n)\cos n\omega_0$, where ω_0 is the central frequency of the voice signal *s(n)* and noise *v(n)*, $\alpha(n)$ and $\beta(n)$ are random amplitude of narrow-band signals. Phase shift $\phi_0 = \frac{l\sin\theta_0\omega_c}{c}$, where l is the distance between two microphones, ω_c is the continuous carrier frequency, c is the propagation speed, θ_0 is the direction angle between the voice signal *s(n)* and noise *v(n)* [12].

From Wiener-Hopf equation [45] , the coefficients can be determined as follows:

$w_0 = \frac{\sigma_\alpha^2 + \sigma_\beta^2\cos\phi_0}{\sigma_\alpha^2 + \sigma_\beta^2}$, $w_1 = \frac{\sigma_\beta^2\sin\phi_0}{\sigma_\alpha^2 + \sigma_\beta^2}$, where σ_α and σ_β are the variances of voice signal *s(n)* and noise *v(n)*.

Assumes signal $x(n) = \gamma(n)\cos n\omega_0$ is arriving at an angle θ. When θ is 0°, it is voice signal; otherwise, it is the noise. Then the output can be expressed as [12]

$$e(n) = \gamma(n)[(\cos(\pi\sin\theta) - w_0)\cos n\varpi_0 + (\sin(\pi\sin\theta) - w_1)\sin n\varpi_0]$$

$$= a(\theta)\gamma(n)\sin(n\varpi_0 + \varphi(\theta)),$$

where $a(\theta) = \sqrt{(\cos(\pi\sin\theta) - w_0)^2 + (\sin(\pi\sin\theta) - w_1)^2}$

and $\varphi(\theta) = \tan^{-1}(\frac{\cos(\pi\sin\theta) - w_0}{\sin(\pi\sin\theta) - w_1})$.

For the function *a(θ)*, its derivative can be calculated to get the maxim and minim values of function *a(θ)*. Because of *a(θ)* > 0, the maxim and minim values of function $a^2(\theta)$ is the same of function *a(θ)*. So in the simplified way, the derivative of $a^2(\theta)$ is calculated.

$a^2(\theta) = (\cos(\pi \sin\theta) - w_0)^2 + (\sin(\pi \sin\theta) - w_1)^2$. The derivative of $a^2(\theta)$ is $b(\theta) = [2\sin(2\pi \sin\theta) - w_0 \sin(\pi \sin\theta) - w_1 \cos(\pi \sin\theta)]\pi \cos\theta$.

Assumes when $\theta = 0$, then $b(\theta) = -\pi w_1 \neq 0$.

Normally, when $0 < \theta_0 < \pi/2$, $w_1 > 0$. Moreover, $a^2(\theta)$ and *b(θ)* are continuous functions, so $a^2(\theta)$ can not get the maxim or minim value at $\theta = 0$, because $b(\theta) \neq 0$.

Thus, it is easy to verify that when $\theta=0$, $b(\theta) \neq 0$. That means that when $\theta=0$, $a^2(\theta)$ can not get its maxim value.

This equation is not easy to get the exact solution for $b(\theta)=0$. However, where the maxim or minim value occurs can be clarified according to the property of function continuity and derivative.

(1) ∵ When $\theta = \pi/2 \; and \; 3\pi/2$, $b(\theta) = 0$

∴ $a^2(\theta)$ has the maxim or minim value at $\theta = \pi/2 \; and \; 3\pi/2$.

(2) Assumes θ is very close to $-\pi/2$ and $\theta > -\pi/2$, then $b(\theta) \approx w_1 > 0$ when $0 < \theta_0 < \pi/2$. And we also know that when $\theta=0$ and $0 < \theta_0 < \pi/2$, $b(\theta) = -\pi w_1 < 0$

∵ $a^2(\theta)$ and *b(θ)* are continuous functions, ∴ *b(θ)* should cross 0 at least once when $\theta \in$

$(-\pi/2, 0]$. That means that $a^2(\theta)$ should have at least one maxim or minim value when $\theta \in (-\pi/2, 0]$.

(3) In the similar way, $a^2(\theta)$ should have at least one maxim or minim value each when $\theta \in (-\pi, -\pi/2], \theta \in (0, \pi/2)$ and $\theta \in (\pi/2, \pi)$.

C. MATLAB Simulation Program for Noise Cancellation

```
% programm for noise cancellation in hearing aid, including AD converter and DSP part

% set the original parameters for noise cancellation simulation
% itn, thetao, sigma_a, sigma_b, Misad, gap_length, T1, analog_frequency and
noise_angle can be changed
   itn=10000;                    % cycle times / first sampling discrete signal length
   thetao=-45.0;                 % angle difference (degree)
   thetao=pi*thetao/180;         % angle difference convert to rad
   deltao=pi*sin(thetao);        % another conversion  (rad)

   sigma_a=0.01;                 % Variance of the desired signal
   sigma_b=1.0;                  % Variance of jammer signal or noise

   Misad=0.1;
   traceR=2*(0.5*sigma_a+0.5*sigma_b);
   mu=Misad/traceR;

   gap_length=0;                 % gap length of signal and noise for second sampling
   T1=1.0/(100.0*1000.0);
   % first sampling period / the first sampling frequency is 1MHz
   T2=T1*(gap_length+1);
   % The real sampling period got from first and second sampling
   analog_frequency=3.0*1000;          % analog signal central frequency (Hz)
   omegao_c=2*pi*analog_frequency;     % analog signal central frequency (rad/s)
   omegao=omegao_c*T2;                 % digital signal central frequency (rad)

% generate the first sampling signal and noise
   aa=1.0*sqrt(sigma_a)*randn(itn,1);     % the random amplitude for signal
   bb=1.0*sqrt(sigma_b)*randn(itn,1);     % the random amplitude for noise
   theta_a=2*pi*rand;                     % rand orignal phase of signal;
   theta_b=2*pi*rand;                     % rand orginal phase of noise;

   ss=aa.*cos([1:itn]'*omegao+theta_a);   % generated first sampling signal
   rr=bb.*cos([1:itn]'*omegao+theta_b);
   % generated first sampling noise

 % second sampling for signal and noise
   n=1;
   m=1;                                   % temperate second sampling cycle number

   while (n+(n-1)*gap_length)<=itn
      s(m)=ss(n+(n-1)*gap_length);        % signal after second sampling
      r(m)=rr(n+(n-1)*gap_length);        % noise after second sampling
```

```
      a(m)=aa(n+(n-1)*gap_length);        % processed second sampling signal
      b(m)=bb(n+(n-1)*gap_length);        % processed second sampling signal
      n=n+1;
      m=m+1;
   end
   digital_length=m-1;      % the length of signal and noise for second sampling

  % let the no use element to zero for second sampling (amplitudes, signal and noise)
   for n=digital_length:itn
      s(n)=0;
      r(n)=0;
      a(n)=0;
      b(n)=0;
   end

 % calculate the input first sampling SNR
   power_s=0;
   power_r=0;
  for n=1:digital_length
     power_s=power_s+s(n)^2;
     power_r=power_r+r(n)^2;
  end
  snr=log(power_s/power_r);

% generate the real signal and noise into two microphones
   xp_beforeAD=(a.*cos([1:itn]*omegao+theta_a)+b.*cos([1:itn]*omegao-
deltao+theta_b))/5.0;
   x1_beforeAD=(a.*cos([1:itn]*omegao+theta_a)+b.*cos([1:itn]*omegao+theta_b))/5.0;

xq_beforeAD=(a.*cos([1:itn]*omegao++theta_a)+b.*cos([1:itn]*omegao+deltao+theta_b
))/5.0;

%add the phase shifter 90 degree for x1_beforeAD
   x2_beforeAD=(a.*sin([1:itn]*omegao+theta_a)+b.*sin([1:itn]*omegao+theta_b))/5.0;

 %  AD converter programm
   y1= uencode(xp_beforeAD,8,1,'signed');
   y2= uencode(x1_beforeAD,8,1,'signed');
   y3= uencode(x2_beforeAD,8,1,'signed');
   y4= uencode(xq_beforeAD,8,1,'signed');
   % data convertion to double format
   xp=double(y1)/(2^8);
   x1=double(y2)/(2^8);
   x2=double(y3)/(2^8);
   xq=double(y4)/(2^8);
```

```
% noise cancellation core / LMS solution for Winer-Hope equation
  xi_p=zeros(itn,1);
  xi_q=zeros(itn,1);
  wp=[0 0]';
  wq=[0 0]';
  for n=1:digital_length
     xtdl=[x1(n);x2(n)];
     ep(n)=xp(n)-wp'*xtdl;
     eq(n)=xq(n)-wq'*xtdl;
     wp=wp+2*mu*ep(n)*xtdl;
     wq=wq+2*mu*eq(n)*xtdl;
     xi_p(n)=xi_p(n)+ep(n)^2;
     xi_q(n)=xi_q(n)+eq(n)^2;
  end

% calculate the onput signal SNR
  power_ep=0;
  power_eq=0;
 for n=1:digital_length
    power_ep=power_ep+ep(n)^2;
    power_eq=power_eq+eq(n)^2;
 end

% input a temp signal to get the gain for different angles
  sigma_c=0.01;
  % Variance of the temp desired signal
  cc=1.0*sqrt(sigma_a)*randn(digital_length,1);
% the temp random amplitude for signal
% when the signal is too large, the AD will satruation, but when the signal is too small,
%what is result?

  analog_frequency_temp=3.0*1000;    % analog temp signal central frquncy (Hz)
  omegao_c_temp=2*pi*analog_frequency_temp;
   % analog temp signal central frquency (rad/s)
  omegao_temp=omegao_c_temp*T2;    % digital signal central frquency (rad)

  theta_c=2*pi*rand;                        % rand orignal phase of temp signal;
  temp=cc.*cos([1:digital_length]'*omegao_temp+theta_c);
   % generated first temp sampling signal / x(n)
  temp_shift=cc.*sin([1:digital_length]'*omegao_temp+theta_c);
  % generated first shift temp sampling signal / x~(n)

  y_temp= uencode(temp,8,1,'signed');                % AD conversion for temp signal
  y_temp=double(y_temp)/(2^8);                        % data conversion
  y_temp_shift= uencode(temp_shift,8,1,'signed'); % AD conversion for temp shift signal
  y_temp_shift=double(y_temp_shift)/(2^8);        % data conversion
```

```
  m=1;
  for angle_c=0:2*pi*0.01:2*pi
     deltao_c=pi*sin(angle_c);        % change the temp signal angel to orientation
     temp_d_p=cc.*cos([1:digital_length]'*omegao_temp-deltao_c+theta_c);
     % temp signal with pashe delay
     temp_d_q=cc.*cos([1:digital_length]'*omegao_temp+deltao_c+theta_c);
     y_temp_d_p= uencode(temp_d_p,8,1,'signed');
     % AD convertion for temp signal with phase delay
     y_temp_d_q= uencode(temp_d_p,8,1,'signed');
     y_temp_d_p=double(y_temp_d_p)/(2^8);
     % data convertion
     y_temp_d_q=double(y_temp_d_q)/(2^8);
     y_temp_out_p=y_temp_d_p-(y_temp.*wp(1)+y_temp_shift.*wp(2));
     % output of temp signal
     y_temp_out_q=y_temp_d_q-(y_temp.*wq(1)+y_temp_shift.*wq(2));

  %calculation the SNR for temp signal with different input angle
     power_temp=0;
     power_tempout_p=0;
     power_tempout_q=0;
     for n=1:digital_length
        power_temp=power_temp+y_temp(n)^2;
        power_tempout_p=power_tempout_p+y_temp_out_p(n)^2;
        power_tempout_q=power_tempout_q+y_temp_out_q(n)^2;
     end
     if (power_tempout_p<power_tempout_q)
        snr_temp(m)=log(power_tempout_p/power_temp);
     else
        snr_temp(m)=log(power_tempout_q/power_temp);
     end
     m=m+1;
  end


% plot the polar figure for gain
  m=1;
  for angle_c=0:2*pi*0.01:2*pi
     exp_temppolar(m)=exp(snr_temp(m));
     m=m+1;
  end
  figure(3)
  f=polar(theta,exp_temppolar);
  set(f,'LineWidth',1.5)

  % display the other useful parameters
```

```
disp(' Input SNR (dB) = ' )
disp(snr)

disp('gap length of signal and noise for second sampling = ')
disp(gap_length)

disp(' Sampling frequency (kHz) = ')
disp(1.0/(T2*1000))
```

D. Author's Related Publications

1. Ram Singh Rana, Garg Hari Krishna, **ZhangLiang** and Tang Bin "Hearing Aid Devices A Few Selected Research Issues", *the 8th World Multi-Conference on Systemic, Cybernetics and Informatics*, July 18-21, 2004, Orlando, Florida, USA, pp. 80-84
2. Ram Singh Rana, **Zhang Liang**, Tang Bin and Garg Hari Krishna, "An Enhanced Method and Behavioral Model for Noise Cancellation in Audio Devices" *IEEE International Workshop on Biomedical Circuits & Systems*, 1-3 December 2004, Singapore, pp. S2.6-11-S2.6-14
3. Ram Singh Rana, **Zhang Liang** and Garg Hari Krishna, "Sub-mA Single Ended CMOS Low Noise Amplifier with 2.41 dB Noise Figure", *IEEE Journal of Analog Integrated Circuits and Signal Processing*, (reviewed and revised)
4. Ram Singh Rana, Tang Bin, **Zhang Liang**, Garg Hari Krishna, Wang De Yun and Lim Hsueh Yee, "Reverberation Canceling Wireless Aid for Hearing Impaired", *IEEE Transaction on Neural Systems and Rehabilitation Engineering*, under review
5. Garg Hari Krishna, Ram Singh Rana, Tang Bin and **Zhang Liang**, "System Simulation on Wireless Hearing Aids Using ADS", Asilomar Conference 2005, USA, (presented).
6. Ram Singh Rana, Tang Bin, **Zhang Liang**, Garg Hari Krishna and Wang De Yun, "Wireless Hearing Aid System Simulations using Advanced Design System A Behavioral Modeling Approach," *the 27th Annual International Conference of the IEEE Engineering in Medicine and Biology*, pp. 5.3.1-6, Sept.2005, Shanghai, China.