SELECTED TOPICS ON ADVANCED ELECTRON DEVICES AND THEIR CIRCUIT APPLICATIONS

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Summary

In this thesis, selected topics on advanced modern electron devices have been studied, including both active devices and passive devices. Their applications in different kinds of circuit applications are also discussed.

In part I, a systematic study of Negative Bias Temperature Instability (NBTI) in p-MOSFETs with ultra-thin SiON gate dielectric is reported. The study shows that the conventional measurement methods which have been used over the past years seriously underestimate N_{it} due to passivation of N_{it} during measurement. By using the fast pulsed method, a fast Dynamic NBTI (DNBTI) component is distinguished from the conventional slow one for the first time. Evidence has been shown that this component is due to trapping and de-trapping of hole traps N_{ot} in SiON. The accumulative degradation increases with increasing stress frequency. A model describing the phenomenon has been developed and the model simulations are in excellent agreement with all the experiments. The impact of fast DNBTI on device lifetime and circuit applications has been re-evaluated in the light of this new finding.

In part II, researches have been done on proton implanted high quality inductor as well as high-κ MIM capacitor, showing promising characteristics for future ULSI application. RF and analog circuits using advanced passive devices are also designed and the simulation results show improved circuit performance.

Part I

A systematic study on Negative Bias

Temperature Instability (NBTI) in p-MOSFETs

with ultra-thin SiON gate dielectrics

Chapter One

Introduction

1.1 MOSFET scaling and issues with gate dielectric scaling down

The modern Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) was successfully demonstrated in the 1960's, when the silicon technology was mature enough to realize MOS gate stacks based on the thermal SiO_2-Si framework. Large-scaled commercialization of MOS technology took place from then on. In 1963, the complementary MOSFET (CMOS) was proposed [1]. It soon emerged ast the work-horse in the semiconductor industry due to its low power consumption and high packing density. It still prevails as the technology of choice for today's ultra-large-scale-integration (ULSI) applications.

For the goals of reducing gate delay, increasing operating frequency, increasing transistor density and reducing power dissipation, the modern MOSFETs has been continuously downsized based on a set of guidelines established over the past four decades. The basic scaling parameters include channel length L, power supply voltage V_{dd}, threshold voltage V_{th}, and gate oxide thickness t_{ox}. According to Moore's law [2], for every three years, the device dimension is reduced by approximately $1/\sqrt{2}$, the chip size is increased by about 1.5 times, and the number of transistors in a chip is increased by a factor of four. By reducing the device dimensions, in particular the

transistor gate length the amount of current supplied by a transistor is increased. Higher current allows the circuits to switch more quickly, leading to faster computations. In addition, the reduction in transistor size also allows more transistors to be integrated on a single chip. Consequently the complexity and functionality of ICs can be increased while keeping the cost of the circuit fabrication low. This in turn constantly expands the realm of possible applications of semiconductor products.

On the other hand, with the reduction in gate length, gate is losing its control over the channel because of a channel control competition from the drain side. To keep the pace with drive current demands and the better gate control over channel, the gate dielectric thickness must also be scaled down in accordance with the gate length. As can be seen from Fig. 1.1, gate dielectric thickness continues to shrink aggressively to offer higher drive current and gate capacitance required by scaled MOSFETs.
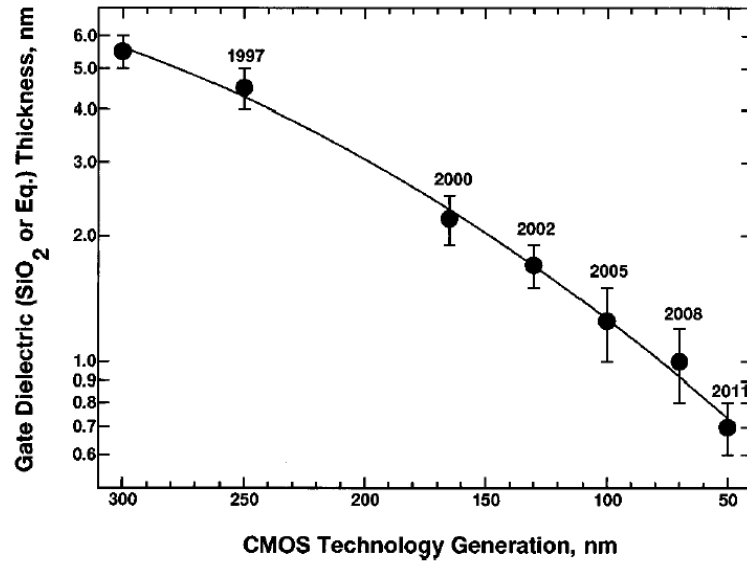

Fig.1-1 Decrease in gate EOT with device scaling. (Extracted from ITRS [3]).

Though promising for high performance MOSFETs, ultra-thin gate dielectric layer leads to critical issues in the following areas, namely: (i) Direct tunneling current (DT); (ii) Boron penetration and gate poly-silicon depletion; (iii) Quantum mechanical

effects; (iv) Integration issue and manufacturability; and, (v) Oxide reliability. These issues pose serious challenges for device engineering and could become significant hurdles for further MOSFET scaling.

1.2 Oxide reliability and motivation

Oxide reliability is one of the most important issues introduced by gate dielectric scaling down. It has received increasing attention since it causes degradation and failures in advanced ULSI devices, and therefore, is a serious challenge to the downscaling trend of oxide thickness and MOSFET size.

A critical reliability issue that is associated with dielectric scaling is negative bias temperature instability (NBTI). In recent years, it has been widely recognized that NBTI is the most serious reliability issue in the ultra-thin SiO_2 or SiON gate dielectric p-channel MOSFETs (p-MOSFETs) [4] [5]. It could increase the amplitude of the threshold voltage (ΔV_{th}) by as much as $50 - 100mV$ in a p-MOSFET over a period ranging from months to years, depending on the operating condition. As a result, it would be more difficult to turn on the p-MOSFET, causing a significant reduction in circuit speed and even logical mal-function. With these concerns, the reliability of ultra-thin gate dielectrics has become one of the limiting factors for future ULSI development.

As a result of the NBTI issue in the p-MOSFET, an evolutionary change in the lifetime limiting factor for CMOS technology has occurred in the past few years. Traditionally, for 0.35μm technology and above, hot-carrier injection (HCI) induced degradation of n-channel MOSFETs limits the lifetime of CMOS circuitry, and

therefore considerable work has been carried out to understand the mechanism responsible for defect generation in n-MOSFETs under HCI stress. However, with aggressive scaling of the thickness of gate oxide film into the direct-tunneling regime, NBTI degradation in p-MOSFETs, instead of the HCI degradation in n-MOSFETs, limits the CMOS lifetime [5]. Therefore, investigation into NBTI issue becomes paramount especially when the gate dielectric thickness is reduced to barely a few atomic layers.

Another challenge is that the NBTI reliability physics of ultra-thin gate dielectric becomes more complicated when continued scaling requires material-based modification like incorporation of nitrogen into the thin SiO_2 film to form silicon oxynitride (SiON) or even totally change the SiO_2 based dielectric material to high-κ material, for instance, HfO_2. Many existing NBTI models for thick pure SiO_2 might then be challenged [6]. Hence, it is essential that a systematic study on this topic could be carried out as soon as possible.

Significantly, G. Chen et al. [7] reported a recovery effect of NBTI stress which prolongs the device lifetime in real application. A debate on what is the origin of this recovery effect was then raised. G. Chen et al. [7] and also some other groups claimed that the V_{th} recovery in the passivation phase is due to the passivation of SiO_2/Si interface traps [8]-[12]. On the contrary, V. Huard et al. [13] argued that the transient recovery of V_{th} in the passivation phase is due to de-trapping of hole traps in the dielectric. To clarify this conflict is demanded not only for physics study, but also has important implications for real IC application and further studies on high-κ dielectric MOSFETs.

All the above factors form the major motivation of this research work, which addresses the issue of NBTI in the ultra-thin gate dielectric MOSFETs.

1.3 Review of previous studies on NBTI in p-MOSFETs

Researches on NBTI can be traced back to the very early days of MOS device development. In 1967, Deal et al. [14] found that both the interface trap density N_{it} and oxide charge density N_{ox} increased after negative bias stress. The rates of increase of both N_{it} and N_{ox} were very similar. In 1973, Goetzberger et al. reported the same observation using metal gate devices with 100 nm thick oxides, stressed at –106V/cm at 300°C [15]. Later on, many other research groups confirmed the observation that there is an equal growth of oxide charge (reflected by V_{th} shift) and surface trap density, which are independent of the NBTI stress field and temperature. Another common observation is that the generation of interface trap and positive oxide charge follow a power-law time dependence with the exponent having values in the range of 0.20 ~ 0.25 [16]-[20]. To explain the interface trap generation, many researchers adopted the Si-H dissociation mechanism, which is a two-reaction model involving atomic hydrogen dimerization and hydrogen-interface reactions [21]. At that time, it is commonly acknowledged that the threshold voltage shift is only because of interface trap generation. Since the dielectric layer was so thick that no direct tunneling or FN tunneling could occur, no one took the bulk trap into consideration.

Recently, Dynamic NBTI stress test is widely used to predict the device lifetime and to study the physical mechanisms of BTI degradation since it is more similar to the real device operation conditions. In the year of 2002, G. Chen et al. applied an AC stress on the gate to simulate an inverter's operation conditions: switch on and off [22]. Consequently, they found that the Dynamic NBTI effect significantly prolongs the lifetime of p-MOSFETs operating in a digital circuit. As shown in Fig.1-2 [22], the

projected 10-year lifetime operating voltage V_{10Y} is 1.2V for Dynamic NBTI stress, and is 0.9V for Static NBTI stress, which overestimates the degradation in real digital circuit operation.
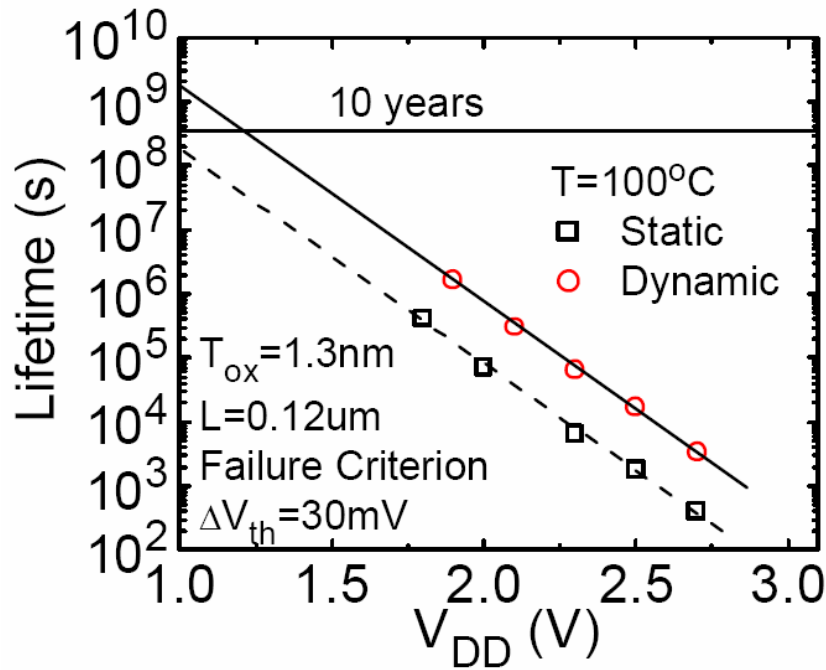

Fig.1-2 SNBTI and DNBTI lifetime projections for p-MOSFETs. The SNBTI stress overestimates the degradation in real digital operation.

From then on, many groups started trying to do more researches on this DNBTI effect [23]-[26], not only on pure SiO_2 dielectrics, but also other materials such as HfO_2 based high-κ dielectric, Si_3N_4 etc..

With the advent of high-κ dielectric, more advanced measurement technologies [6] [27] are now being used in BTI research, especially for measuring the fast V_{th} shift. The V_{th} shift can no longer be ascribed to only the interface traps, but the charge trapping and de-trapping in the bulk dielectric layer [6], [27] also contributes to it. Fig.1-3 gives a comparison on ΔV_{th} measured by fast and conventional DC methods on both n- and p-MOSFETs respectively, showing significant difference.
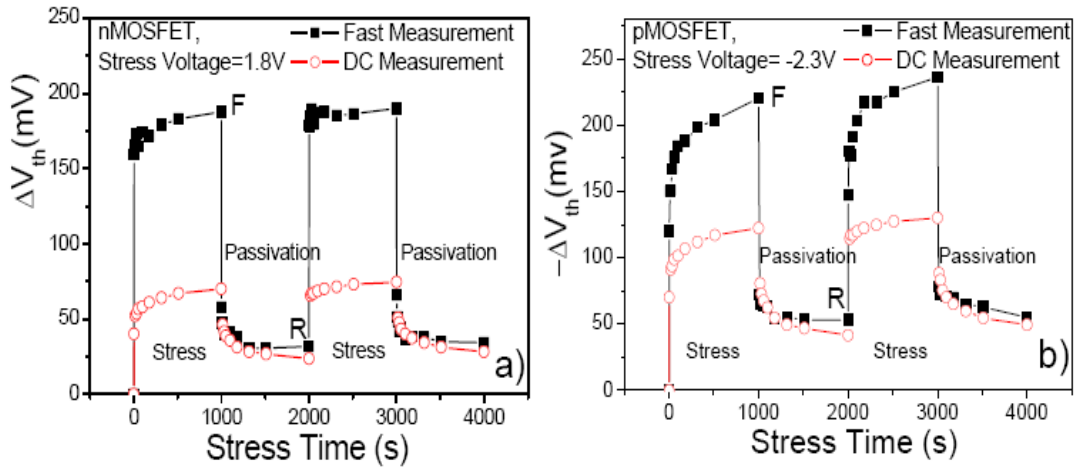
Fig.1-3 Comparison of measured ΔV_{th} under DNBTI stress by fast and conventional DC methods on both n- and p-MOSFETs.

A new reaction-diffusion model was proposed by M. A. Alam [8] to study the physics of frequency-dependent shift in transistor parameters due to NBTI. C. Shen et al. also made a frequency dependent model and explained the BTI frequency dependence of the slow traps by the –U property of these traps [6].

However, there has been no research work using the fast measurement method to study on SiON dielectrics, which is widely be used in present day CMOS technology. Does SiON also have fast traps? If so, does it affect the circuit performance and device lifetime? These questions are to be discussed based on the experimental result.

1.4 Major contribution of this work

The followings are the major contributions of this work.

1.   For the first time, a systematic study on the impact of N_{it} measurement on N_{it} and V_{th} recovery has been done.

2.   The recent debate in the slow DNBTI component measured by conventional DC method has been clarified.

3.   The fast DNBTI component measured by fast measurement method has been demonstrated and analyzed for the first time. Device lifetime has been re-evaluated based on the new results and its impact on circuit application has also been studied.

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Chapter Two

Measurement methods for NBTI

Characterization

2.1 Introduction of the conventional DC technique for V_{th}

characterization

The NBTI degradation of CMOS devices with conventional gate dielectrics is commonly studied using static (DC) measurement techniques. The I_d-V_g curves are monitored by measure-stress-measure cycles with DC parametric measurement tools such as the HP4156 semiconductor parameter analyzer. The linear extrapolation (LE) method is widely used to extract threshold voltage (V_{th}) from measured I_d-V_g curves. From the extracted ΔV_{th} as stress time curves, the device stability degradation is investigated.

Fig.2-1 illustrates the typical DC measurement waveform applied to the gate when interrupting the stress for measurement. Stress is stopped at time t_1. Since parameter analyzer needs time to set up the measurement parameters, the measurement is actually started after a delay (t_2-t_1). At time t_2, the gate voltage starts to scan from 0V to the device operation voltage (usually smaller than the stress voltage) and at the same time, the analyzer captures the I_d-V_g information. This measurement period takes around

0.5sec or more. Then, also after a small delay, the stress is resumed at time t_4. The whole measurement cycle from stopping stress to resuming stress takes around 1~2sec.
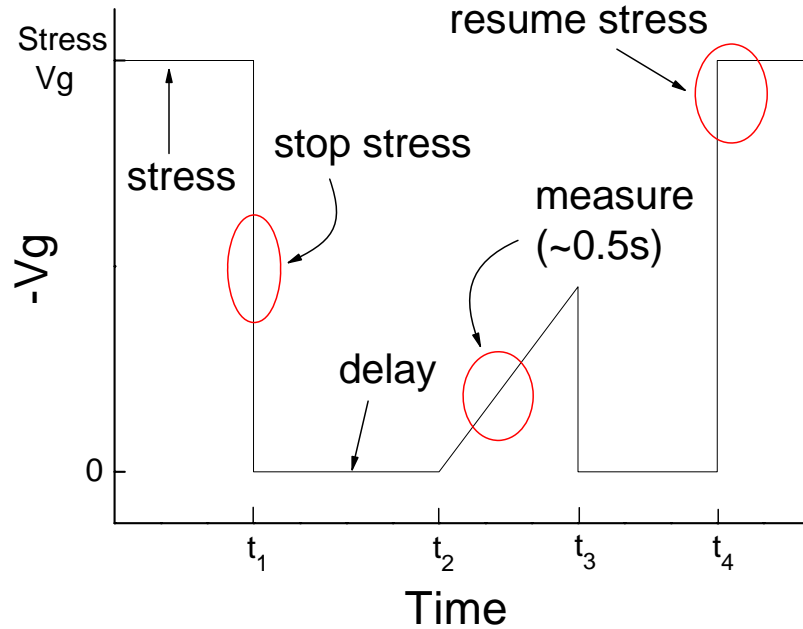

Fig.2-1 Illustration of the conventional DC NBTI measurement cycle.

However, since there is always a time delay, which is typically in the order of 0.1−1 second, between the end of stress and the I_d−V_g measurement for V_{th} extraction, using this method to extract the ΔV_{th} characteristic is only able to observe the slow component in NBTI degradation.

2.2 An advanced fast technique for V_{th} characterization

Since the aggressive scaling of CMOS devices, the pure SiO_2 gate dielectric is being driven to its physical limits. Alternative gate dielectrics, such as SiON and HfO_2 based materials, are currently being investigated extensively as a replacement for SiO_2 as a gate insulator. With the equivalent oxide thickness (EOT) scaling down, charge

trapping / de-trapping in these alternative gate dielectrics makes degradation and recovery in V_{th} significant even within a 1ms delay [1]–[4]. The conventional measurement method greatly underestimates the real V_{th} NBTI degradation. Though the V_{th} recovery during the short delay in conventional DC measurement method has long been thought negligible in devices with SiO_2 as the gate dielectric, it must be taken into consideration in the investigation of SiON gate dielectric devices. Therefore, a fast technique is necessary to be developed in order to give more accurate analysis in SiON gate dielectric investigation.

The measurement method developed by Kerber et al. has been widely used to evaluate the fast charging trapping in high-κ dielectrics [1]. The method setup is shown in Fig.2-2.
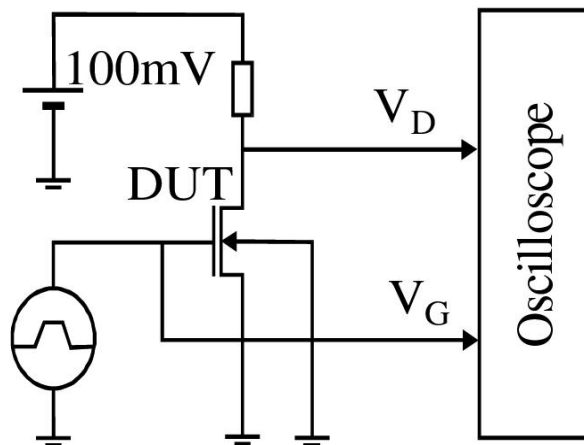

Fig.2-2 Schematic drawing of measurement setup used for pulsed Id-Vg experiments in the μs range.

A pulse generator is used to apply the gate voltage to the MOSFET. The oscilloscope monitors the gate voltage, and measures the voltage drop across the sense resistor R at the drain, from which one is able to extract the drain current by the following equation:

$$I_d = \frac{100mV}{V_d} \cdot (\frac{100mV - V_d}{R_L}) \ , \qquad\qquad 2.1$$

where R_L is the load of the inverter circuit. The pulsed I_d-V_g measurement technique enables drive current measurements down to less than millisecond. More importantly, the time delay between stressing and sensing is significantly shrunk.

However, this method brings some constraints for ultra-fast measurement. In this method, the drain voltage of the MOSFET under test is not a constant, but changes with the change of drain current. The parasitic capacitor C_0 and C_{gd} are charged or discharged since the change of gate or drain voltage during the measurement, and this charging current distorts the measured drain current. To circumvent this problem, an improved pulsed I_d–V_g measurement technique was developed by C. Shen et al [6], as shown in Fig.2-3.
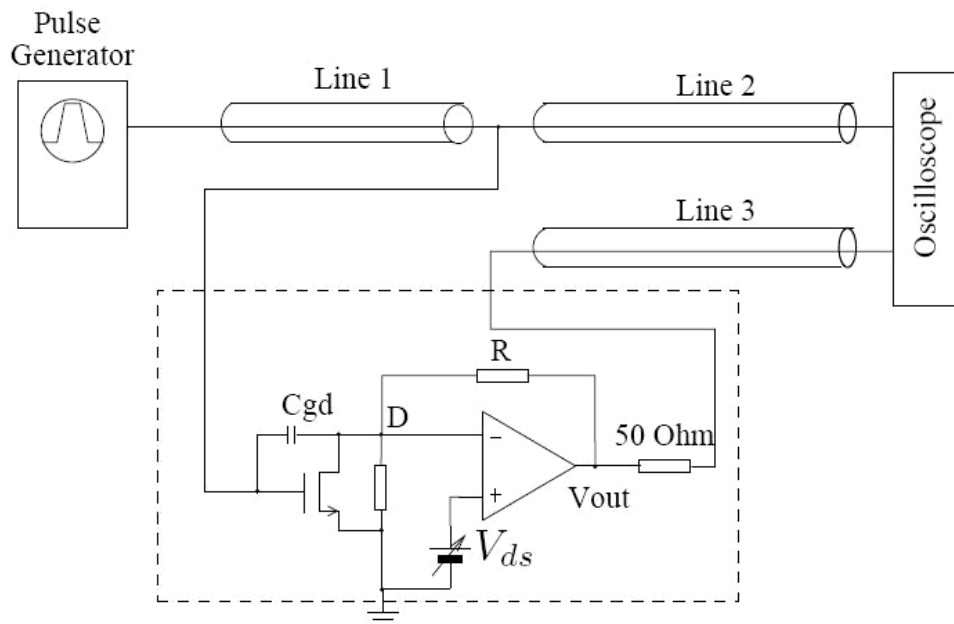

Fig.2-3 Schematic diagram of the setup used for improved pulsed I_d-V_g measurement technique

In this setup, an Op-Amp is inserted between the drain and source/substrate. Since the virtual short circuit property of Op-Amp (the two input terminals are forced to be

equal), the drain voltage of the MOSFET is fixed at V_{ds} supplied by the voltage source. Therefore, there is no charging or discharging current flows through C_0. A high-speed Op-Amp (OPA655) with 400MHz unity gain bandwidth is used to achieve fast measurement.

As samples are measured in probe station environment, the Op-Amp circuit (enclosed by the dashed line in Fig.2-3) is mounted immediately above the probe holder. Probe holders are modified to make the wire connection from voltage source to the transistor source and drain terminal less than 10cm, so that the parasitic effects are minimized. All the transmission lines are 50Ω co-axial cables, and cable 2 and 3 have the same length to minimize the difference in cable delay. The drain current is measured by the sense resistor R. Resistor $R_0 = R$ is used to ensure circuit stability when the MOSFET is off. The output voltage measured at the oscilloscope is related to the MOSFET drain current by:

$$V_{out} = (I_d - I_{gd}) \cdot R + V_{ds} ,$$
2.2

where R is the sense resistance, V_{ds} is the drain voltage, and I_{gd} is the current from gate to drain through the parasitic capacitor C_{gd}. The current I_{gd} is caused by the fast transient at the gate and is given by:

$$I_{gd} = C_{gd} \cdot \frac{dV_{gd}}{dt} = C_{gd} \cdot \frac{dV_{gs}}{dt} .$$
2.3

In the measurement, the MOSFET is biased in linear region in $I_d - V_g$ measurements, and C_{gd} is given by:

$$C_{gd} = C_{overlap,d} + \frac{1}{2} C_{inv} ,$$
2.4

where $C_{overlap,d}$ and C_{inv} are the capacitance of the drain overlap region and the inversion capacitance, respectively.
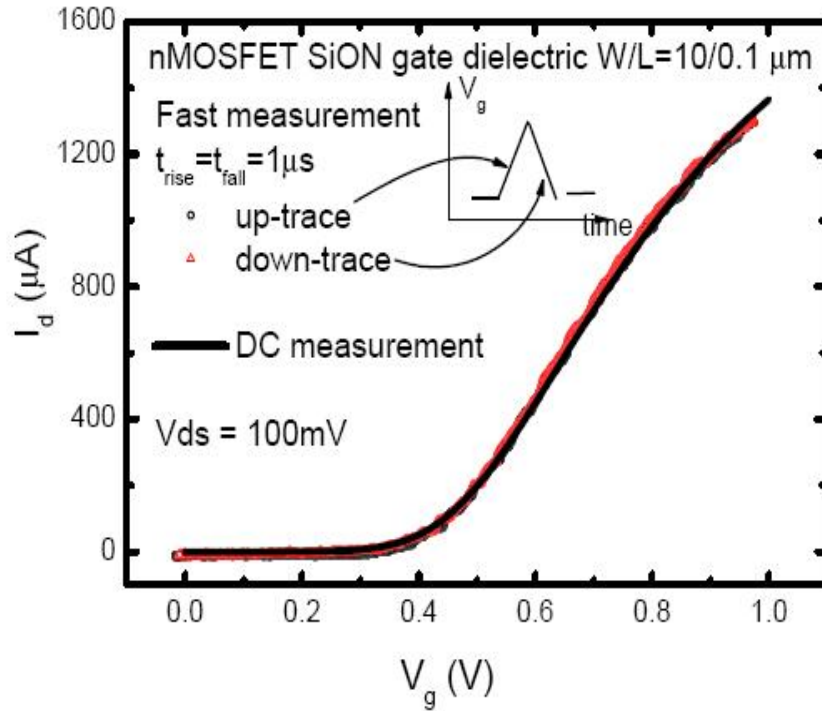
Fig.2-4 I_d-V_g characteristics measured from a short-channel nMOSFET with SiON
gate dielectric, with the V_g waveform shown in the inset.

For short-channel devices, since C_{gd} is small, the corresponding I_{gd} is much smaller than the drain current, and therefore the charging current through C_{gd} can be ignored. When a symmetric triangular pulse is applied at the gate as shown in the inset of Fig.2-4, I_d-V_g curve can be measured at both the up-trace and down-trace of the pulse. In the two cases, dV_g/dt are of the same magnitude but of opposite polarity. For nMOSFET with short channel length L = 0.1μm, the I_d-V_g curves measured in the up-trace and down-trace (1μs measurement time) of V_{gs} both coincide with that from DC measurement, as shown in Fig.2-4, which indicates that the effect of charging current through C_{gd} with a measurement time down to 1μs is negligible.

This improved pulsed I_d-V_g measurement method is used to evaluate the charge trapping in ultra-thin SiON gate dielectric devices. It distinguishes the fast and slow NBTI component in SiON [4]. The 1μs measurement time is shown to be fast enough

for this particular application. Results of the fast measurement will be discussed in Chapter 4.

2.3 Improved Charge Pumping and DCIV techniques for N_{it} characterization on thin gate dielectric

The charge-pumping (CP) technique is a well-known experimental approach for assessing the interface-state density of MOSFET's [5] [6]. Using this technique, it has been possible to measure the spatial variation of hot carrier induced D_{it} near the drain [7]-[9]. The pulses applied to the gate of the MOSFET can be square, triangular or sawtooth waves. The basic arrangement for the conventional CP measurements is presented in Fig.2-5.
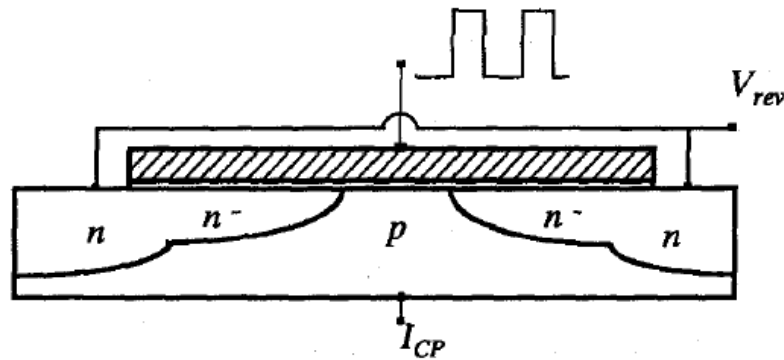

Fig.2-5 Schematic diagram for Charge Pumping measurement setup

An HP8110 pulse generator is used to supply the gate pulses, and a small reverse bias is applied to the source and drain of the MOSFET. The substrate current of the device can be measured by an HP4156 parameter analyzer with varying pulse base level to drive the silicon surface from accumulation to inversion, while the amplitude of the pulses is kept constant.

Fig.2-6 shows the measurement result on a long channel device with a thick EOT around 20nm [10]. The pulses added on gate were trapezoidal in shaped, and three different rise and fall times of the pulse were used in the measurements. As shown in this figure, the leakage gate current is very low during the measurement even when the amplitude of gate voltage exceeds 6V, hence it is generally thought to be accurate when measuring the devices with EOT>30Å.
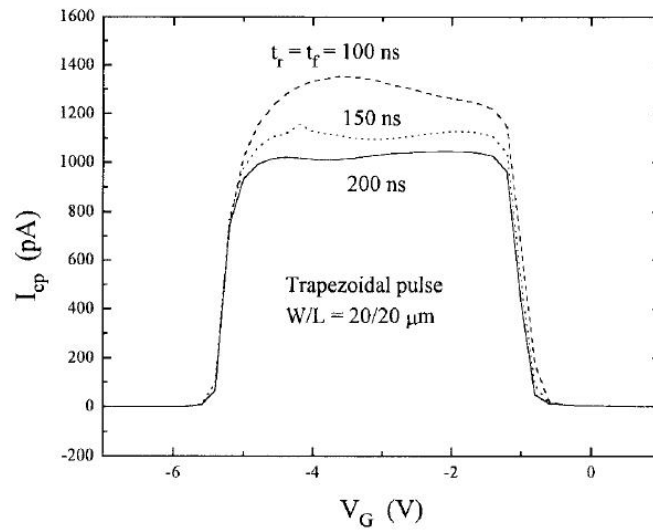

Fig.2-6 Measured I_{cp} on a long channel thick dielectric device by the conventional Charge-Pumping measurement.

However, scaling of sub-l00nm device nowadays needs a t_{ox} in the range of 10-15Å, and as predicted from the roadmap, this thickness is even reaching the range of <10Å in the next couple of years. It is well known that two pronounced effects occur as a result of the gate oxide scaling below 30Å, i.e., direct tunneling gate leakage and the quantum mechanical effect [11] [12]. Since large gate leakage current occurs during the measurement, this conventional Charge-Pumping measurement becomes inaccurate for the t_{ox}<2nm. With the gate leakage current becoming dominant for t_{ox}<1.3nm, it is even impossible to observe the peak I_{cp} by the conventional Charge-

Pumping method. Then one faces a severe problem on how to measure the oxide quality with thickness below 20Å, in particular the interface traps N_{it}.

An improved method – high-low frequency CP method, derived from the conventional charge pumping method was demonstrated by S. S. Chung et al. [13] for accurate determination of the interface traps in ultra-thin dielectric devices.
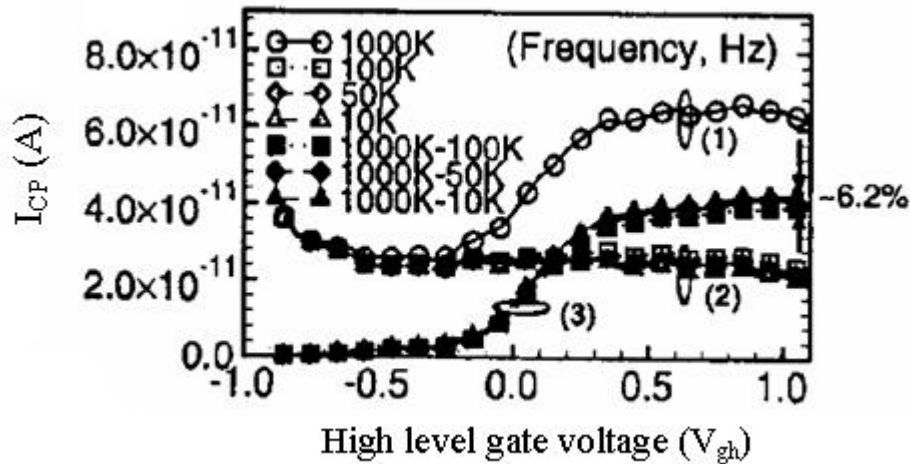

Fig.2-7 I_{cp} measured by high-low frequency CP method.

High-low frequency CP method is shown in Fig.2-7. First, the I_{cp} for various frequencies was measured. Curve (1) was measured by a high frequency, while group (2) curves were measured by several low frequencies and are considered as the leakage current. Using curve (1) subtract group (2) curves can have the correct I_{cp} (group 3) without leakage component. Since the charge pumping current is proportional to the measurement frequency, one is now able to extract the N_{it} parameter from the I_{cp} curves after low frequency calibration.

Another method commonly used to characterize N_{it} is direct-current current–voltage (DCIV) technique [14].

Fig.2-8 illustrates the DCIV measurement set-up for a p-MOSFET. The drain p$^+$, n$^-$ well and p$^-$ substrate form a vertical BJT transistor. Since the base current I_b comes

from the recombination current at the interface traps generated during operation, it is directly proportional to N_{it}. Therefore, by measuring I_b, one is able to get the information of N_{it} in the channel. Adjust V_g until the interface trap energy in the middle of the Si energy gap becomes coincident with the Fermi energy; a peak value of I_{DCIV} can then be observed, and this peak amplitude is actually proportional to the effective number of interface traps N_{it}.
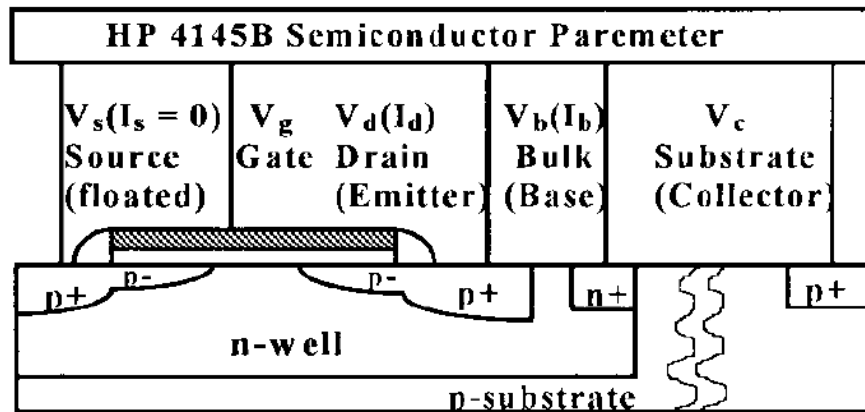

Fig.2-8 Cross-sectional schematic of a PMOS and the DCIV measurement set-up.

However, this method also suffers from the high leakage current with dielectric scaling down. G. Chen et al. [15] proposed an improved DCIV method to monitor the interface traps in MOSFETs with gate oxide thicknesses down to 1.3 nm by proper biasing and signal processing. By measuring I_b under bias $V_e>0$ and $V_e=0$, respectively, one finds the difference ($I_{b(Ve)} - I_{b(0)}$) is exactly the DCIV current combined with background recombination current (from drain to n-well) and thermal-trap-tunneling current at s/d extension, which are both independent of the N_{it}. Since BTI characterization usually only concentrates on the increase or recovery in N_{it} during stress or passivation, using the difference ($I_{b(Ve)} - I_{b(0)}$), one is able to eliminate the influence from the gate leakage current.

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Chapter Three

A detailed analysis on conventional DC measurements

3.1 Debate on the origin of NBTI recovery effect in p-MOSFET with SiON gate dielectric by DC method

It is commonly known that under static NBTI stress, the p-MOSFET shows a significant negative threshold voltage shift. By adding a passivation phase (applying a positive or zero gate bias) after the NBTI stress, recovery of NBTI degradation can be observed. Recently, several studies on the origin of this NBTI recovery effect have been reported [1-7]. G. Chen et al. [1], by using DCIV method [8], found that the V_{th} recovery in the passivation phase is due to the passivation of SiO_2/Si interface traps, which is consistent with some other works [2-4, 9, 10]. On the contrary, V. Huard et al. [5] using the charge pumping method (CP) [11], and inferred that the interface trap density remains as a constant during the passivation phase, and the transient recovery of V_{th} in the passivation phase is due to de-trapping of hole traps in the dielectric. In this chapter, the contradicting views on the V_{th} recovery mechanism in the passivation phase will be clarified. The NBTI degradation and recovery effects observed by the conventional DC measurement method is mainly due to the creation and dissipation of

interface traps at the SiON/Si interface by releasing and retracting hydrogen-related species, rather than trapping/de-trapping of the pre-existing hole traps in SiON bulk.

3.2 Experimental results and discussion

Transistors were fabricated using CSM 0.11μm CMOS technology. The gate dielectric with two equivalent oxide thicknesses (EOT), 1.3nm and 4.5nm, were grown by thermal oxidation followed by decoupled plasma nitridation (DPN) and post-deposition thermal annealing. An HP4155C parameter analyzer was used to measure the device characteristics. CP pulse was generated by HP41501B pulse generator. For N_{it} measurement of p-MOSFET with EOT=1.3nm, the improved DCIV method and the improved CP method as illustrated in Chapter 2.3 were used.

For the NBTI characterization, devices with EOT=1.3nm were stressed under a constant negative gate voltage followed by a passivation phase (V_g=0V), while the source, drain and bulk were grounded. Stress in the stress phase was intermittently interrupted for V_{th} and N_{it} measurement. During each interruption, both V_{th} (extracted by I_d-V_g measurement) and N_{it} (extracted by DCIV measurement) were measured by two characterization approaches: in the first approach, V_{th} was measured first, followed by N_{it} measurement; in the second one, N_{it} was measured first, followed by V_{th} measurement. NBTI stress was conducted under a wide range of gate voltage.

From the I_{DCIV} curves as shown in Fig.3-1, one can observe an unambiguous ΔN_{it} generation and recovery. No doubt, interface traps do have recovery effect. Fig.3-2 plots both measured ΔV_{th} and ΔN_{it} data by two approaches.
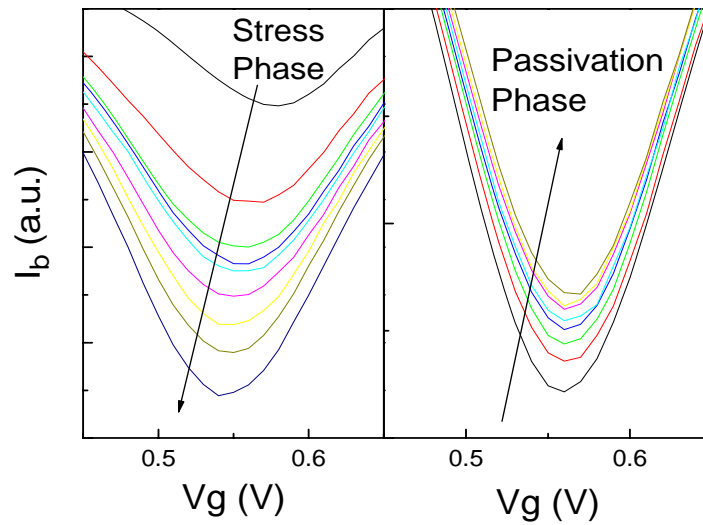
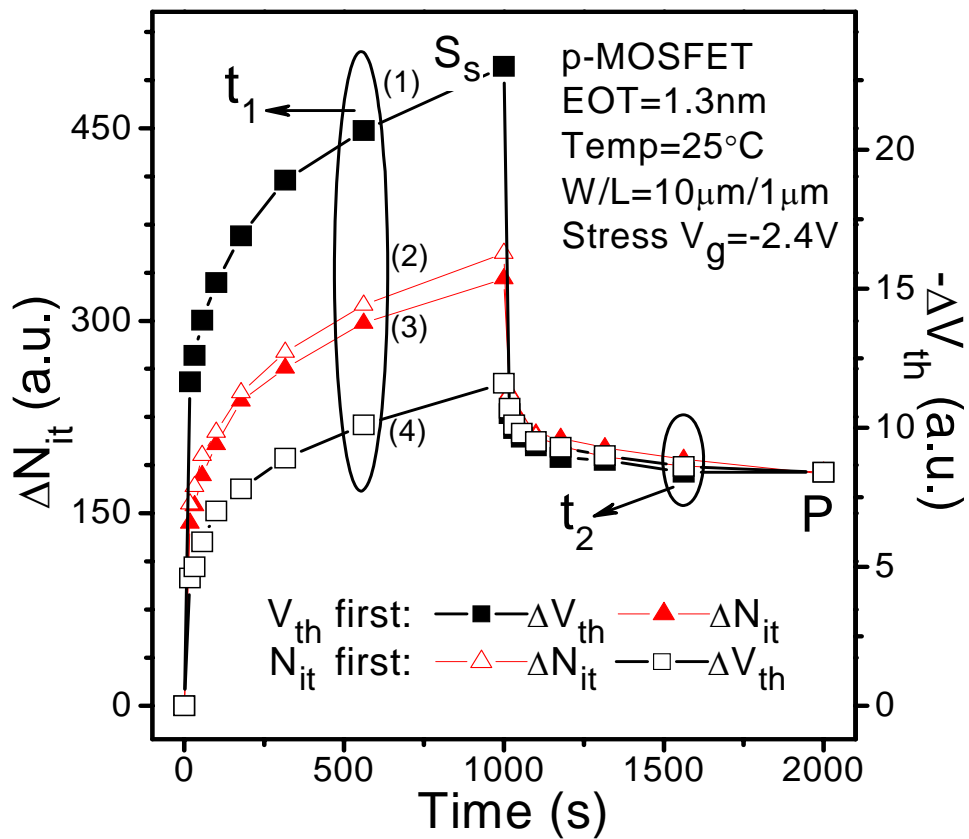Fig.3-1 Measured DCIV curves in both stress and passivation phases.

Fig.3-2 NBTI degradation of pMOSFET characterized by ΔV_{th} and ΔN_{it} under a stress phase (t=0 to 1000s) and a passivation phase (t=1000 to 2000s).

At a first glance, the four curves in Fig.3-2 do not look consistent. For further understanding the result, Fig.3-2 illustrates what really happens when measuring by two different approaches in both stress and passivation phases.
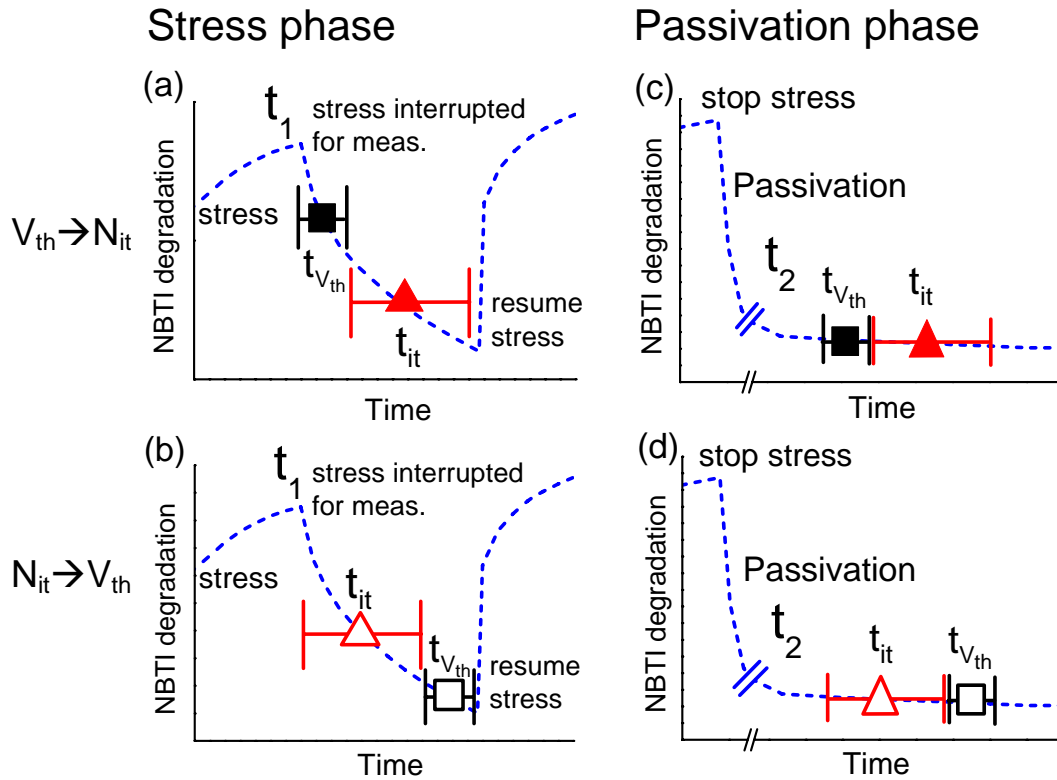

Fig.3-3 Illustration of the NBTI degradation in both stress and passivation phases using two approaches.

In the stress phase, as shown in Fig.3-3(a) and (b), once the stress is interrupted for measurement, the NBTI degradation starts to recover with a trend shown as the dash curves. After the measurement is finished, the stress is resumed, and the NBTI degradation goes up rapidly. If one measures V_{th} first, followed by N_{it}, the V_{th} value (square symbol) will be extracted at a higher NBTI degradation level, and N_{it} (triangle symbol) at a lower level; if measures N_{it} first followed by V_{th}, then the N_{it} value is extracted at a higher level, and V_{th} the lower. However, in the passivation phase, as shown in Fig.3-3(c) and (d), once the stress is stopped for passivation, the NBTI

degradation recovery starts. Until the time point to do the measurement, the recovery rate is already very slow. Therefore, no matter measuring V_{th} first or N_{it} first, the extracted data are taken at almost the same degradation level.
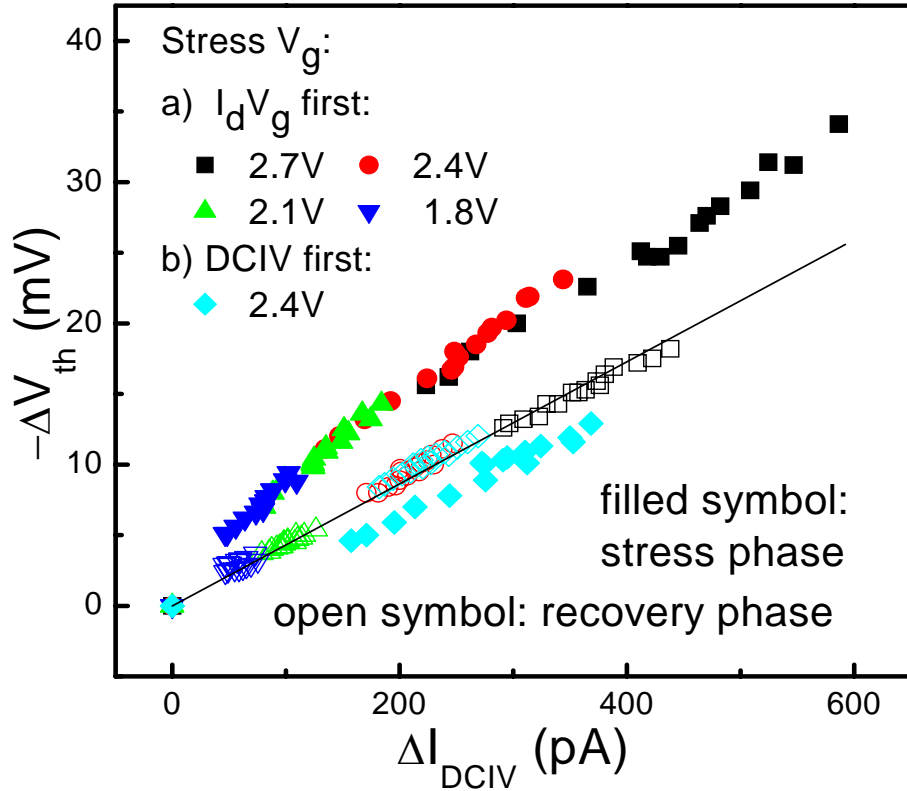

Fig.3-4 The correlation of ΔV_{th} and ΔN_{it} for NBTI stress under various stress voltage, in the stress and passivation phases, using both measurement approaches.

Fig.3-4 gives further proof on this explanation. It shows the correlation of ΔV_{th} and ΔN_{it} for NBTI stress under various stress voltage, in stress and passivation phases, using two measurement approaches. In the stress phase, the two measurement approaches (I_d-V_g first or DCIV first) yield different correlation (different slopes in ΔV_{th}-ΔN_{it} plot). However, in the passivation phase, two approaches yield the same correlation. The real correlation between ΔV_{th} and ΔN_{it} is shown in the passivation phase because of no interface traps passivation during measurement. Therefore, the

normalization of the four curves should be made at the end of passivation phase (point *P*).

Before alignment of the four curves together, ΔV_{th} curves and ΔN_{it} curves were plotted separately first. Plotting first (solid squares) and second measured ΔV_{th} (open squares) together in one figure gets Fig.3-5(a); and plotting first measured ΔN_{it} (solid cycles) and second measured ΔN_{it} (open cycles) together gets Fig.3-5(b).
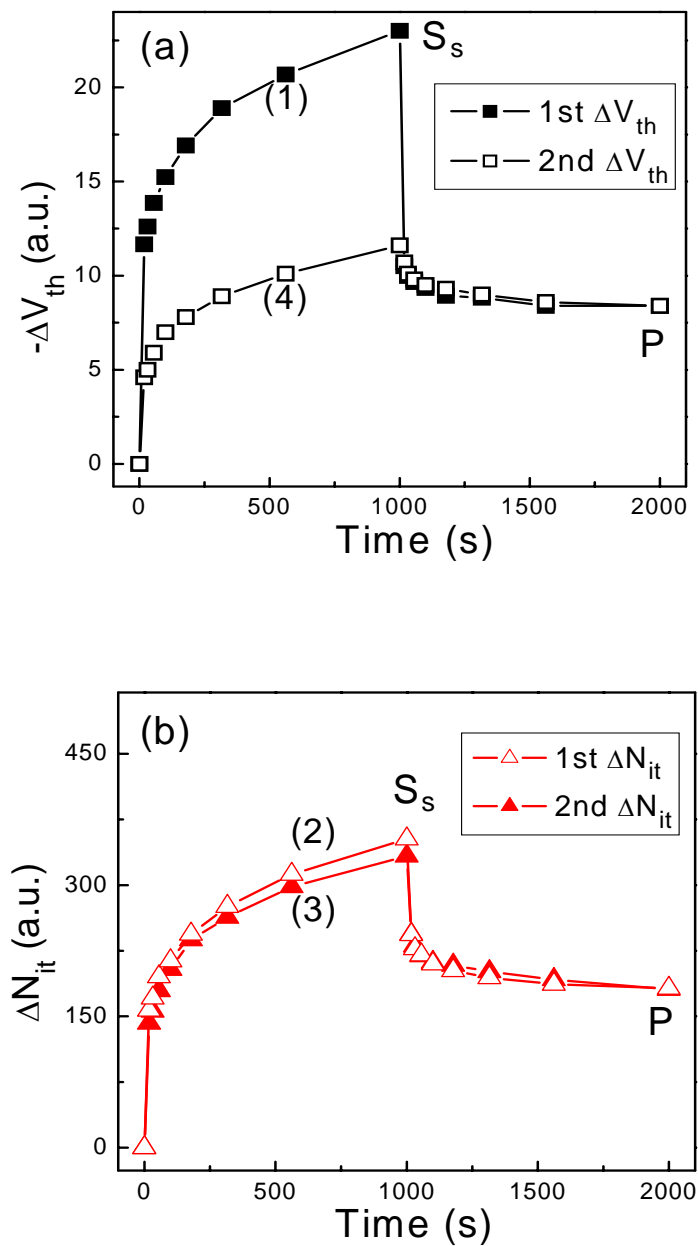

Fig.3-5 Measured (a) ΔV_{th} and (b) ΔN_{it} by two measurement approaches.

Both figures show obvious bifurcation in the stress phase, which is because of N_{it} recovery during the other measurement, while both ΔV_{th} and ΔN_{it} overlap in the passivation phase, showing no influence of the measurement approaches. Normally, it takes different time for V_{th} and N_{it} measurements. Define the time for a V_{th} measurement as t_{Vth} and the time for a N_{it} measurement as t_{it}. Since the DCIV current is several orders smaller than the drain current, usually it takes longer time for N_{it} measurement than for V_{th}, and therefore, $t_{it} > t_{Vth}$, so the gap in the stress phase shown by the two ΔV_{th} curves is much greater than that shown by ΔN_{it} curves. Therefore, when plotting four curves together in one figure, it reasonably gets Fig.3-2.

3.3 Impact of N_{it} measurement on NBTI recovery

Further experiments are designed to illustrate the interface trap passivation effect and show a significant impact of N_{it} measurement on NBTI recovery.

For each fresh device in Fig.3-6, the V_{th} and N_{it} were first measured, giving the initial threshold voltage $V_{th,0}$ and the initial interface trap density $N_{it,0}$. A stress ($V_g = -$2.4V for EOT=1.3nm devices, -4.5V for EOT=4.5nm devices) was then applied for 500sec. Threshold voltage shift $\Delta V_{th1,S}$ was measured at the end of the stress (point S_S as indicated in Fig.3-2), followed by a measurement of the change in interface trap density $\Delta N_{it,S}$ using CP or DCIV method, and another measurement of the threshold voltage shift $\Delta V_{th2,S}$ was followed. After a 500ses lapse in the passivation phase ($V_g = $0V), $\Delta V_{th1,P}$, $\Delta N_{it,P}$, and $\Delta V_{th2,P}$ were measured sequentially again at the end of passivation phase (point P as indicated in Fig.3-2). In Fig.3-6 (b), ΔN_{it} and ΔV_{th} data are normalized at point P because little passivation of N_{it} occurs at P.
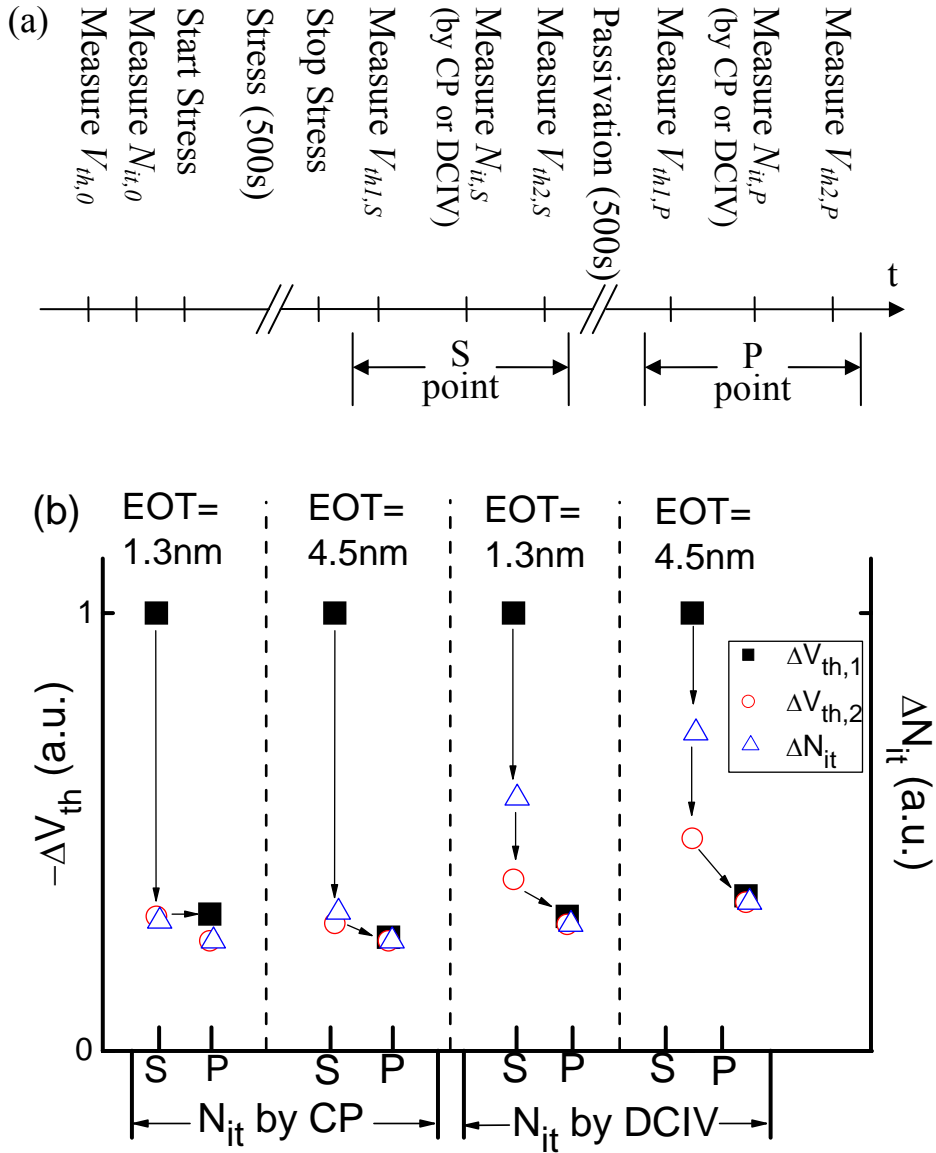
(a) Measure $V_{th,0}$ | Measure $N_{it,0}$ | Start Stress | Stress (500s) | Stop Stress | Measure $V_{th1,S}$ | Measure $N_{it,S}$ (by CP or DCIV) | Measure $N_{it,S}$ | Measure $V_{th2,S}$ | Passivation (500s) | Measure $V_{th1,P}$ | Measure $N_{it,P}$ (by CP or DCIV) | Measure $V_{th2,P}$

(b) EOT= 1.3nm | EOT= 4.5nm | EOT= 1.3nm | EOT= 4.5nm

$-\Delta V_{th}$ (a.u.)

ΔN_{it} (a.u.)

$\blacksquare$ $\Delta V_{th,1}$
$\circ$ $\Delta V_{th,2}$
$\triangle$ ΔN_{it}

S P | S P | S P | S P

$\leftarrow N_{it}$ by CP $\rightarrow$ | $\leftarrow N_{it}$ by DCIV $\rightarrow$

Fig.3-6 (a): Measurement sequences at both *S* and *P* points (indicated in Fig.1)
(b): Measured ΔV_{th1}, ΔN_{it}, and ΔV_{th2} data at points *S* and *P*. ΔN_{it} and ΔV_{th2} data are normalized at point *P*.

All data from devices with thin (EOT=1.3nm) and thick (EOT=4.5nm) gate dielectrics show the same trend: at point *S*, ΔV_{th2} after the N_{it} measurement is much smaller than ΔV_{th1} before the N_{it} measurement. For the thick dielectric with EOT=4.5nm, the measured FN tunneling current at gate rises significantly only when $|V_g|$ is above 5V. Therefore at a stress voltage of -4.5V, the measured gate current is

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negligible and no charge trapping/de-trapping in the dielectric. All variation of V_{th} is due to variation of N_{it} (generation and passivation). The reduction of ΔV_{th} is due to the passivation of interface traps. The N_{it} measurement accelerates the reduction of ΔV_{th} due to the positive gate bias applied to the device during N_{it} measurement. Fig.3-6 (b) also clearly shows that no obvious recovery of ΔN_{it} can be observed in the passivation phase using CP measurement [5], because most of the interface traps have already been passivated during the CP measurement. Since the thin dielectric device has the same trend as the thick dielectric device, it is believed that the V_{th} recovery is dominated by N_{it} passivation [1] rather than N_{ot} de-trapping [5].
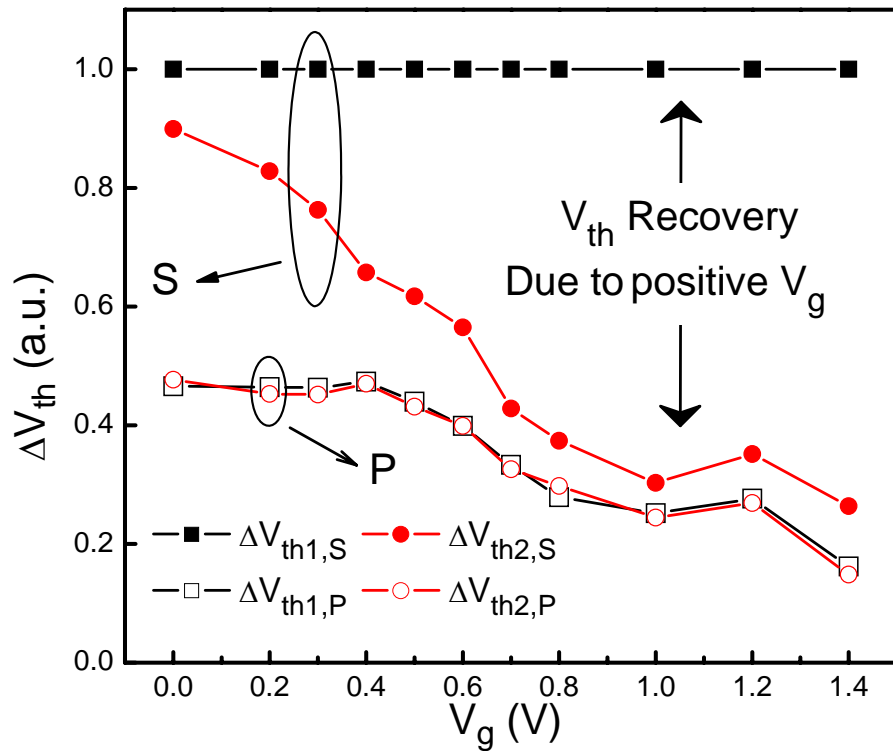
Fig.3-7 In the measurement sequence of Fig.3-6(a), the measurement of N_{it} is replaced by a 0.5 s positive gate bias stress V_g (for both points S and P). Plot $\Delta V_{th,2}$ as a function of different V_g, normalized by $\Delta V_{th,1}$ at point S.

Fig.3-7 illustrates the acceleration effect of interface trap passivation under a positive gate bias. The same measurement sequence as that in Fig.3-6 was used, however the measurement of N_{it} was replaced by a 0.5s positive gate bias stress V_g (for both points S and P). Fig.3-7 plots $\Delta V_{th,2}$ as a function of different positive V_g, normalized by $\Delta V_{th,1}$ at point *S*. The results show clearly that the positive bias accelerates ΔV_{th} passivation. This explains the different results obtained by DCIV and CP measurements in Fig.3-6 (b). In DCIV measurement, a recombination current I_{DCIV} through the interface traps shows a peak when the Fermi level coincides with the Si mid gap at surface [13]. In our measurement, the maximum V_g applied to the device to show the peak is around +0.5~0.6V. In the stress phase measurement, the interface traps have already passivated to some extend before reaching the I_{DCIV} peak gate voltage (Fig.3-7 data measured at point *S*), so the result is always underestimated. However after a time period of passivation in the passivation phase at point *P*, the passivation rate is almost zero (Fig.3-7 data measured at point *P*) and therefore DCIV method measures the real interface trap density.

The underestimation is more serious when using Charge Pumping (CP) technique. In CP measurement, the device changes from inversion to accumulation to pump the electrons between conduction/valence bands through the interface states [11]. Therefore, comparing to the DCIV measurement, a larger positive V_g should be applied. In our CP measurement, the maximum positive V_g applied to the device is +1.2V. In addition, CP measurement uses longer time than DCIV measurement. This explains why $\Delta V_{th,2,s}$ and ΔN_{it} measured by CP is smaller than that measured by DCIV as indicated in Fig.3-6(b), that is, more interface traps are passivated during the CP measurement.
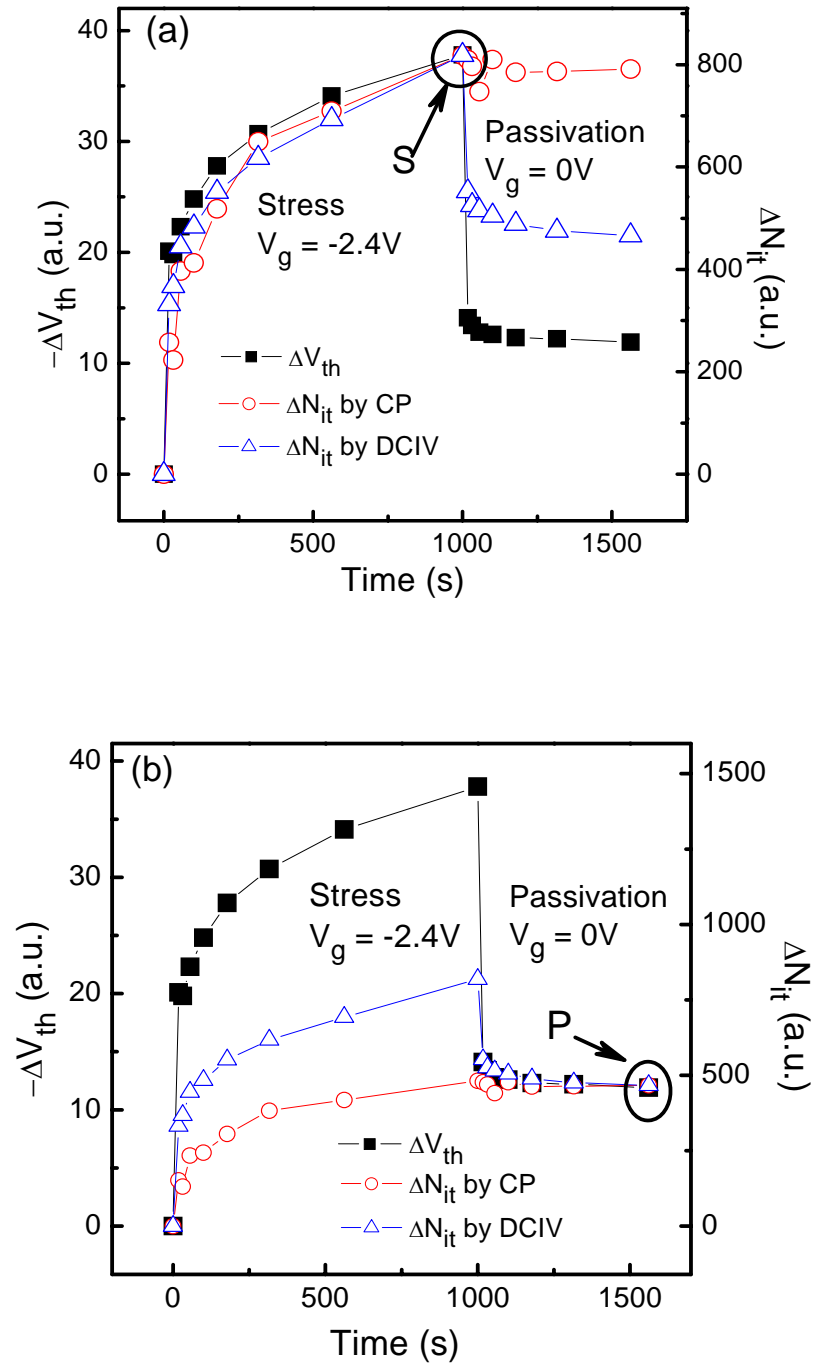
Fig.3-8 The data of ΔV_{th} and ΔN_{it} measured by both CP and DCIV, plotted versus stress and passivation time: (a) all data aligned at point S [5]; (b) all data aligned at P point (this work).

According to the discussion in [5], all curves are aligned at point S in Fig.3-8(a).

However, this alignment is misleading because the measured N_{it} is underestimated

during the stress phase. Due to this incorrect alignment, N_{it} is lifted up at the passivation phase. N_{it} is lifted more by using CP measurement, consistent with Fig.1 of [5], even looks like no interface trap recovery. Thus, the contradiction between two different interpretations of the V_{th} recovery phenomena in the passivation phase is clarified.

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Chapter Four

Fast NBTI components in p-MOSFET with SiON gate dielectric and its impact on circuit applications

4.1 Introduction

As discussed in the previous chapters, using the conventional DC measurement method to characterize the NBTI degradation, time delay between the stopping of the stress and actual measurement is typically in the order of 1 second. Since the NBTI V_{th} degradation starts to recover as soon as the stress voltage is removed, this time delay leads to underestimation of V_{th} degradation which has already been found to be significant in thin high-κ dielectrics [1][2]. Therefore a fast measurement method is necessary to minimize the V_{th} recovery effect prior to measurement. In this chapter, the fast pulsed measurement method as introduced in Chapter 2.4 is used for the DNBTI study of ultra-thin SiON gate dielectrics. By using the fast pulsed measurement method, a distinctive fast trapping / de-trapping transient component that is responsible for large V_{th} shifts has been found, in addition to the widely-reported slower DNBTI degradation component. The frequency and voltage dependencies of the fast DNBTI

component are also investigated. A model for charge trapping is developed, and the impact of the fast DNBTI component is analyzed.

4.2 Experimental results and discussion

Transistors were fabricated using CSM 0.11 μm CMOS technology. The gate dielectric has an equivalent oxide thickness (EOT) of 1.3 nm and was grown by thermal oxidation followed by decoupled plasma nitridation (DPN) and post-deposition thermal annealing. Both NBTI and DNBTI stress were performed using the fast pulsed I_d-V_g measurement technique as described in Chapter 2.4 to examine the fast component of the de-trapping charge as stress progresses.
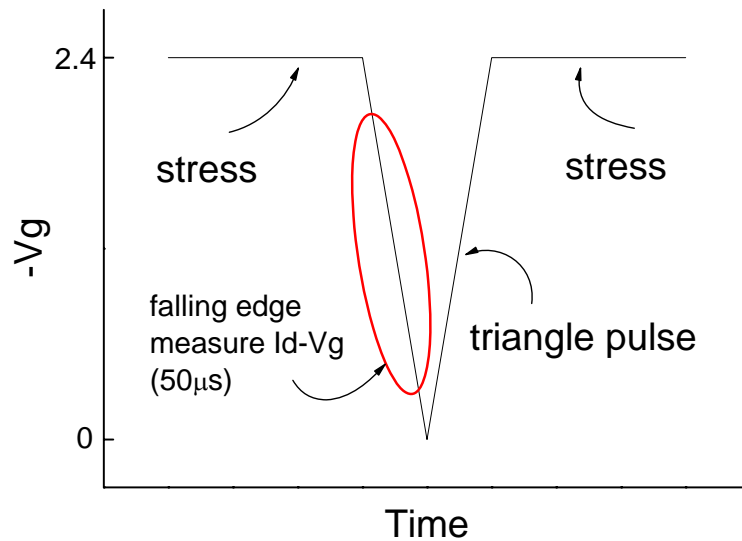
Fig.4-1 Pulsed waveform for NBTI characterization in static stress phase.

For NBTI stress, short triangular voltage pulses (from stress voltage to 0V and back to stress voltage) are inserted in the constant gate voltage stress to intermittently monitor the I_d-V_g characteristics, as illustrated in Fig.4-1. The I_d-V_g curves are derived

from the falling edge (from stress voltage to 0V) or rising edge (from 0V to stress voltage) of the triangular voltage pulses. For DNBTI stress, dynamic stress voltage with a square waveform is applied on the gate with different frequencies, and the I_d-V_g characteristics are measured at both rising (R) and falling (F) edges of the square wave during stress, as illustrated in Fig.4-2. For both NBTI and DNBTI stresses, the measurement time t_m can be adjusted by changing the rising or falling time of the pulses, and therefore the delay between stress and measurement can be minimized. As long as t_m is short enough, the extracted transistor threshold voltage is negligibly affected by the V_{th} recovery effect.
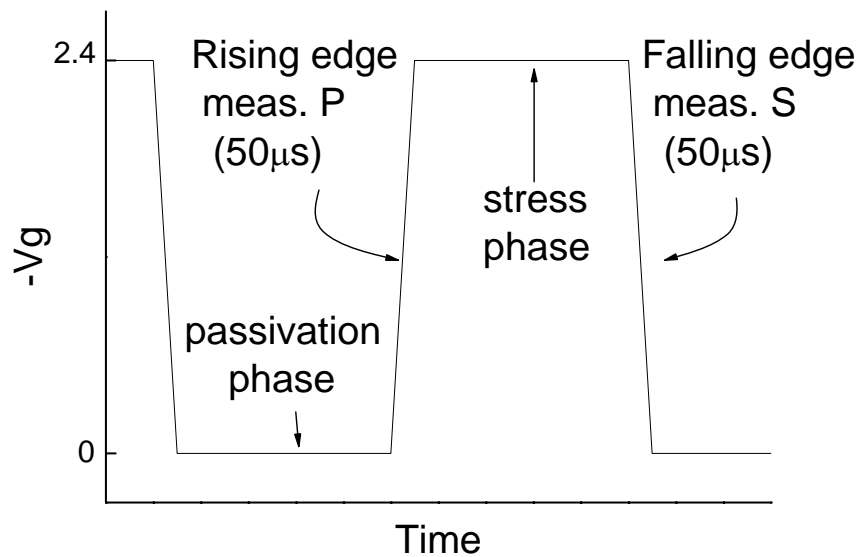
Fig.4-2 Waveform for DNBTI characterization by the fast pulsed measurement.

Fig.4-3 shows an example of measured I_d−V_g curves. The waveform applied on the gate is shown in the inset. First, a triangle pulse was applied on the gate, and the falling edge of the pulse was used to derive I_d−V_g curve of a fresh device; then after a 1 second stress, the falling edge of the stress was monitored to derive the I_d−V_g after stress. From the result, one can see an obvious V_{th} shift.
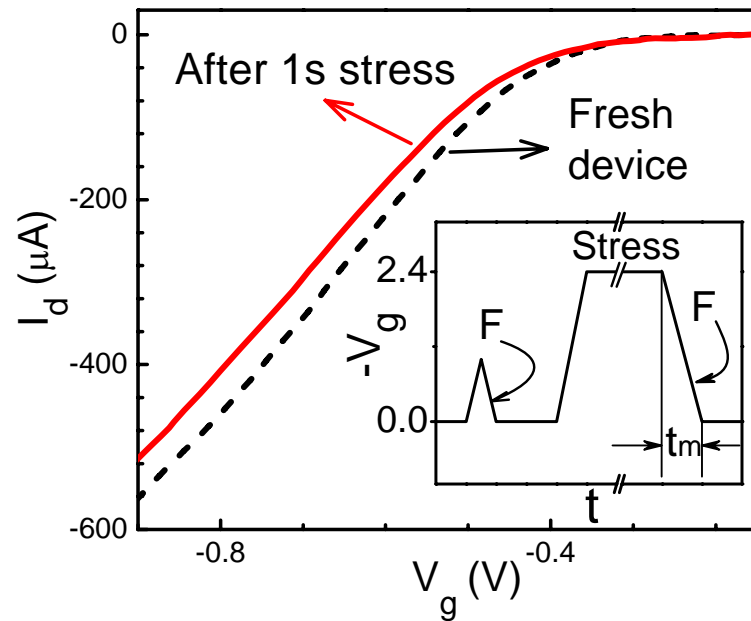
Fig.4-3 $I_d - V_g$ curves measured by fast pulsed measurement.
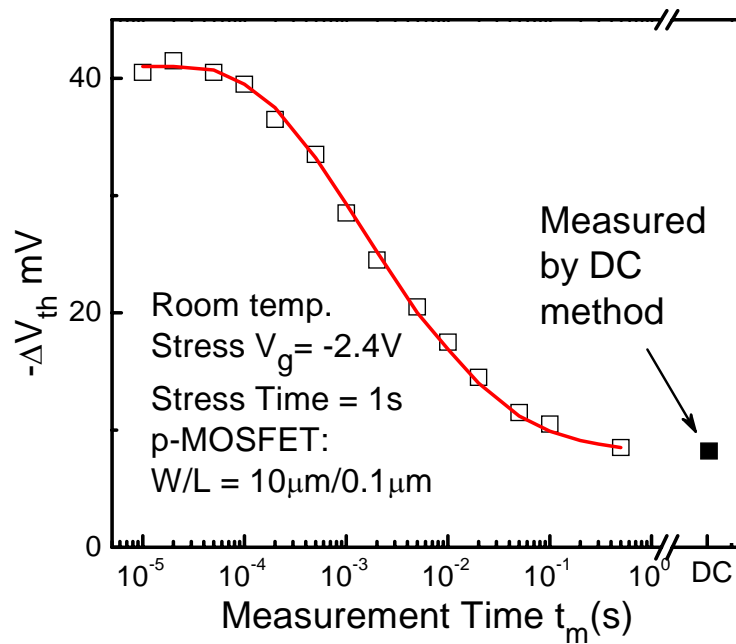
Fig.4-4 ΔV_{th} as measured using different measurement time t_m (Fig.4-3 inset), after 1sec stress. ΔVth measured using a conventional DC method is also shown.

Since result shows the measured V_{th} shift depends on the measurement time, different t_m was used to repeat the above experiment. As shown in Fig.4-4, when t_m is

increased above 100μs, the measured ΔV_{th} decreases dramatically due to V_{th} recovery during the measurement. It is also seen from Fig.4-4 that the ΔV_{th} measured by the fast pulsed method approaches the value obtained by the conventional DC method when t_m is longer than 0.5s, which means that the result of pulsed and DC methods are consistent with each other. On the other hand, when t_m is kept below 100μs, the measured ΔV_{th} is almost independent of t_m, indicating that recovery of ΔV_{th} during that time period is negligible.
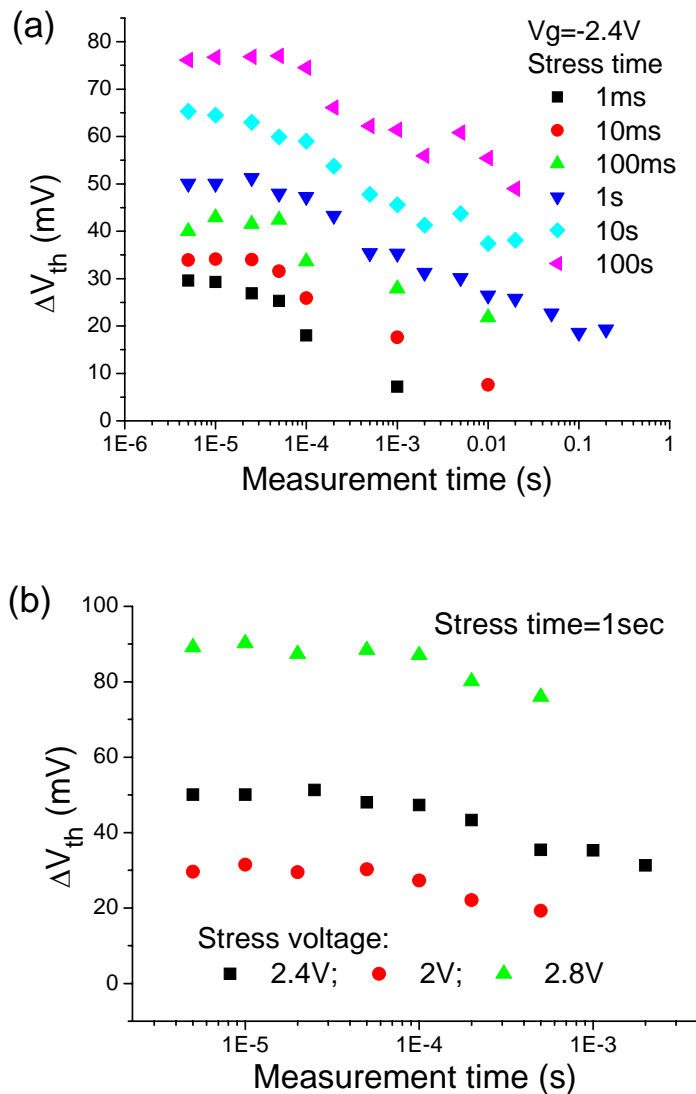
Fig.4-5 ΔV_{th} as measured using different measurement time t_m (Fig.4-3 inset), after: (a) different stress time with same stress voltage; (b) different stress voltage with fixed stress time.

In addition, different samples with different stress voltage V_g and different stress time ranging from 1ms to 100s were measured, and all the results (Fig.4-5) show a saturation ΔV_{th} at $t_m \sim 100\mu s$. Therefore $t_m = 50\mu s$ is fast enough for the specific devices used in this experiment, and it is employed for all the fast NBTI measurements in this work.
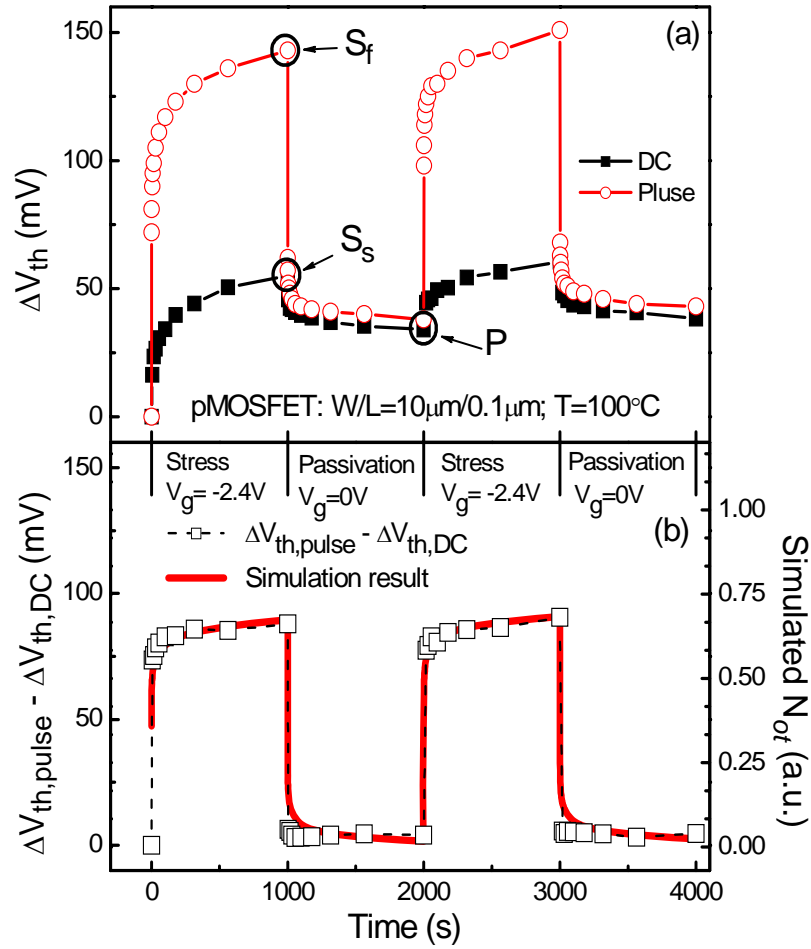
Fig.4-6 (a) ΔV_{th} under dynamic stress as measured by fast pulsed and DC methods for frequency of 0.0005Hz; (b) ΔV_{th} due to fast component.

Fig.4-6 shows the ΔV_{th} evolution measured on a p-MOSFET under DNBTI stress at a very low frequency (0.0005Hz), using both fast pulsed measurement described above and the conventional DC method. S_f and S_s are the points of the end of stress

phase measured by fast pulsed and DC method respectively; *P* is the end of the passivation phase.

The result shows that during stress phase, ΔV_{th} measured by fast pulsed measurement is much higher than that by DC method (about 100mV larger for -2.4V stress at 100°C for 1000s). On the other hand, during passivation phase, the difference in V_{th} shift between fast pulsed measurement and DC measurement diminishes quickly. This indicates that there is a distinctive fast component in the observed NBTI result. From Fig.4-4, one can estimate that the recovery time constant of this fast component is less than 0.1s. The pulsed measurement method captures both the fast and slow components, while the slow DC measurement measures only the slow component since its inevitable delay between stress and measurement, which is much greater than 0.1s. Therefore, the difference between V_{th} shift measured by fast pulsed method and DC method ($\Delta V_{th,pulse}$-$\Delta V_{th,DC}$) can be used as an estimation of the fast component, as shown in Fig.4-6(b).
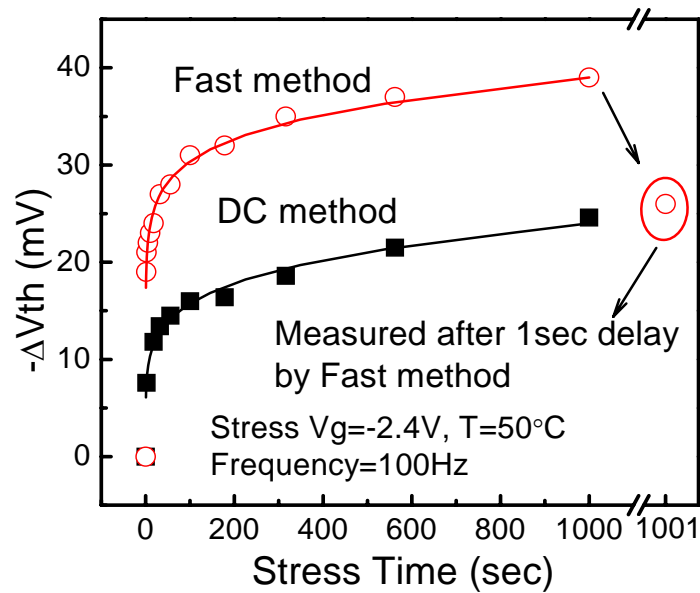
Fig.4-7 Measured ΔV_{th} due to DNBTI using DC method and fast pulsed method (using R edge to measure the accumulation degradation at P).

Using rising edge to measure the accumulation degradation at point *P* by a 100Hz DNBTI stress got Fig.4-7. The point in the circle is the result of fast pulsed measurement stop at 1000s and measured after 1s delay. The charge accumulated in N_{ot} in the stress phase is not completely de-trapped in the passivation phase. Hence, there is a net charge accumulation and N_{ot} contributes to an additional DNBTI degradation.

Fig.4-8 explores the frequency dependence of ΔV_{th} as measured using the fast pulsed method at the end of the stress phase (point S_f) and at the end of the passivation phase (point *P*). As shown in Fig.4-8(a), ΔV_{th} at S_f (open symbols) and *P* (solid symbols) were measured at the falling and rising edges, respectively. Stress-passivation cycles determined by the frequencies are repeated so as to get total stress time of 1000s. At point *P* of each stress cycle, a net charge accumulation which increases with increasing stress time can be observed. This also proves that the charge cumulated in N_{ot} in the stress phase is not completely de-trapped in the passivation phase and N_{ot} contributes to an additional DNBTI. The V_{th} degradation due to the fast component is also a cumulative process.
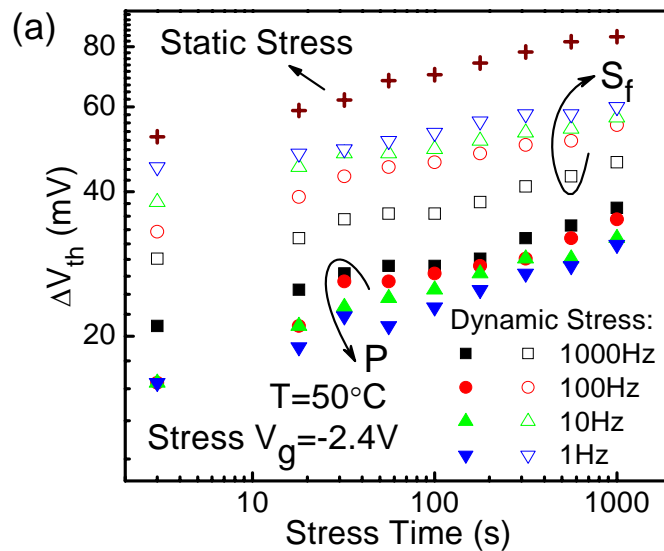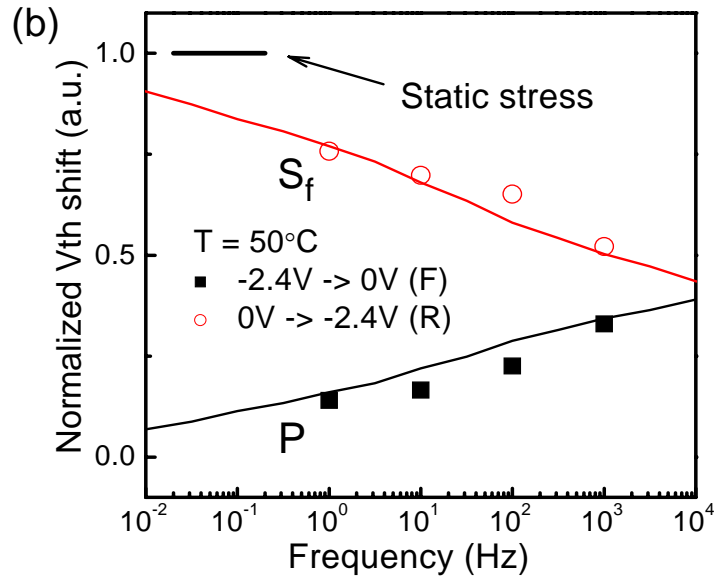
Fig.4-8 (a) Stress pulse frequency dependence of ΔV_{th} due to DNBTI as measured by fast pulsed method. (b) Stress pulse frequency dependence of the fast DNBTI component. The difference between S_f point and P point represents the transient amplitude of ΔV_{th} indicated in Fig.4-6(a).

Fig.4-8(b) shows that the transient amplitude ($\Delta V_{th, Sf}$-$\Delta V_{th, P}$) under dynamic stress is reduced and approaches zero when the frequency is increased. This implies that if the device is working under a very high frequency, little transient effect is expected. On the other hand, DNBTI measured by DC method shows frequency independent behavior as reported in [3]. The same experiment was repeated in SiON samples in this experiment and same conclusion can be drawn from the result. This implies that the fast component and the slow component in NBTI or DNBTI have different origins. According to different results from this frequent dependence experiment, slow component can be attribute to the generation and passivation of interface traps as proposed in [6]-[8], which fits well with the reaction-diffusion model and shows frequency independent; while the fast DNBTI component can be attributed to the trapping and de-trapping at hole traps in SiON dielectric [4].

Measured ΔV_{th} under dynamic and static stresses by fast pulsed and DC methods is shown in Fig.4-9. After 5×10^5s stress, the measured V_{th} shift is around 130mV, still no degradation enhancement or saturation was observed. However, the experiment fit data of $\Delta V_{th,pulse}$ - $\Delta V_{th,slow}$, shown as the "X" symbols, shows a saturation tendency at long stress time, implying the fast component might lose its dominance at very long stress time.
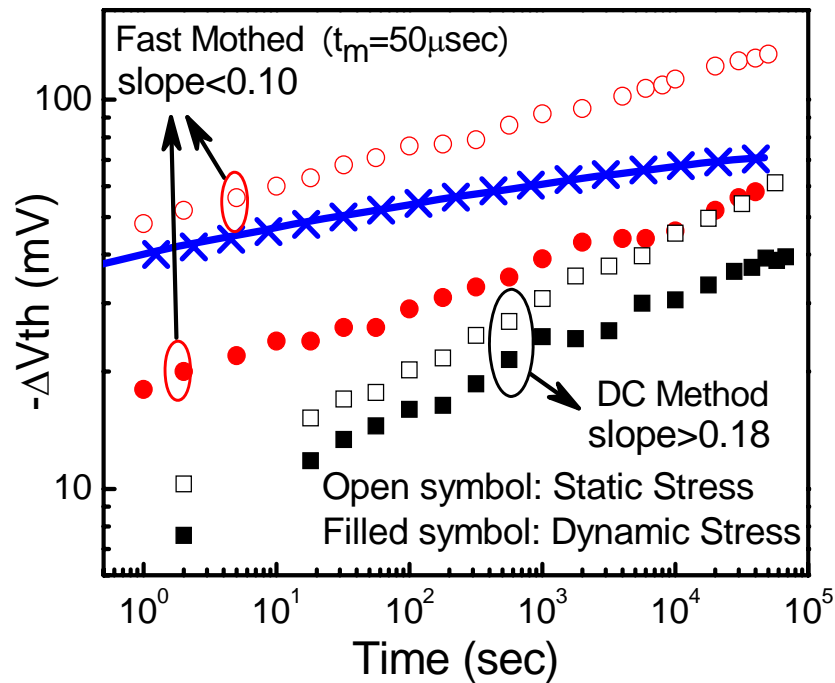

Fig.4-9 Measured ΔV_{th} under dynamic and static stresses by fast pulsed and DC methods as stress time.

Temperature dependence measured by fast pulsed and DC methods under dynamic stress is shown in Fig.4-10. The slow component shows an activation energy (E_a) of 0.11eV, while that of the fast component is only 0.05eV, much less temperature dependent. In addition, at very high temperature, the slow component can be even more significant than the fast component as shown in Fig.4-10.
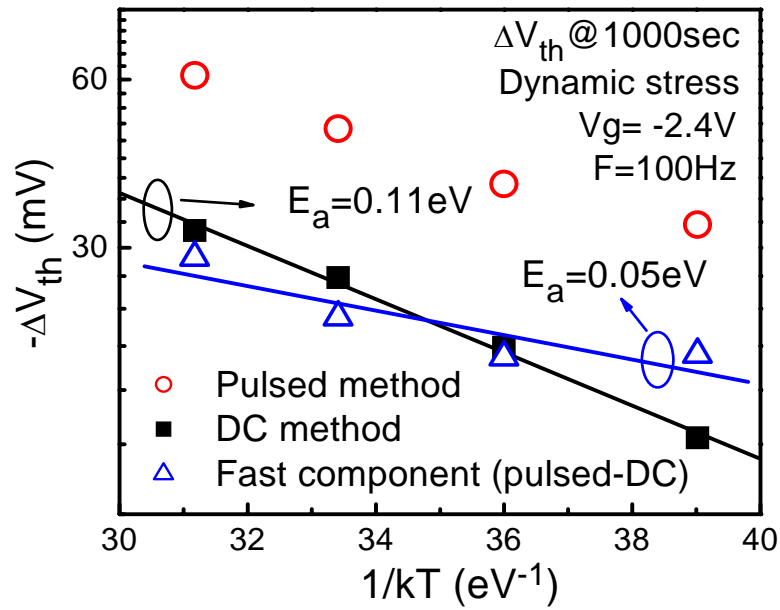
Fig.4-10 Temperature dependence by fast pulsed and DC methods under dynamic stress (measured at P).
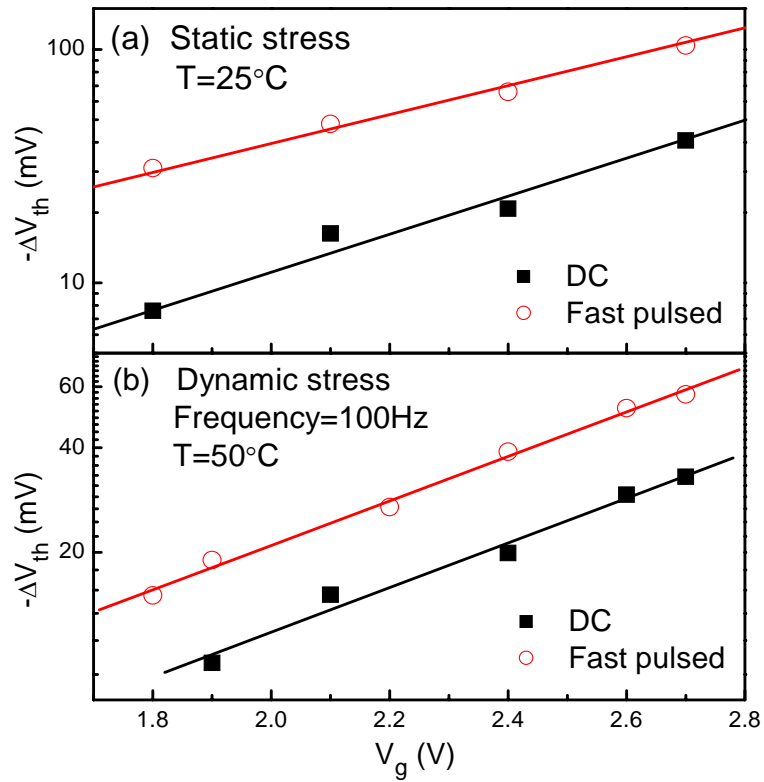

Fig.4-11 ΔV_{th} of p-MOSFET as different stress V_g as measured by both fast pulsed method and DC method under: (a) static and (b) dynamic NBTI stress.

The stress voltage dependence is shown in Fig.4-11. Both static and dynamic NBTI stresses with different stress V_g were applied in the experiment. ΔV_{th} measured by both DC and fast pulsed methods shows exponential dependence on stress V_g.

4.3 Modeling of fast DNBTI component in SiON gate dielectric

The fast DNBTI component in SiON gate dielectric can be simulated using the following equations of trapping and de-trapping of the pre-existing hole traps N_{ot} [11] in bulk gate dielectric:

$$\frac{dp}{dt} = \frac{1}{\tau_C}(N_{ot} - p) - \frac{1}{\tau_{E1}}p \qquad (1)$$

$$\frac{dp}{dt} = -\frac{1}{\tau_{E2}}p \qquad (2)$$

where p is the trapped hole concentration; N_{ot} is the trap concentration, which has a wide distribution over trapping and de-trapping time constants τ_C and τ_E as shown in the inset of Fig.4-12.

Using (1) & (2), the simulated time evolutions of fast NBTI degradation are fitted to the experimental data. Fig.4-12 shows the frequency dependence of the fast DNBTI component ($\Delta V_{th,pulse}$ - $\Delta V_{th,DC}$ after 1000s stress) re-plotted on a normalized scale. Simulated results are plotted using solid lines, which are also in good agreement with the experimental data. The inset of Fig.4-12 shows the spectrum of trap concentration probability distribution function (PDF) over trapping and de-trapping time constants τ_C and τ_E employed in eq. (1) and (2). The continuous distribution of PDF is proposed to explain the power law of time evolution of NBTI degradation [9].
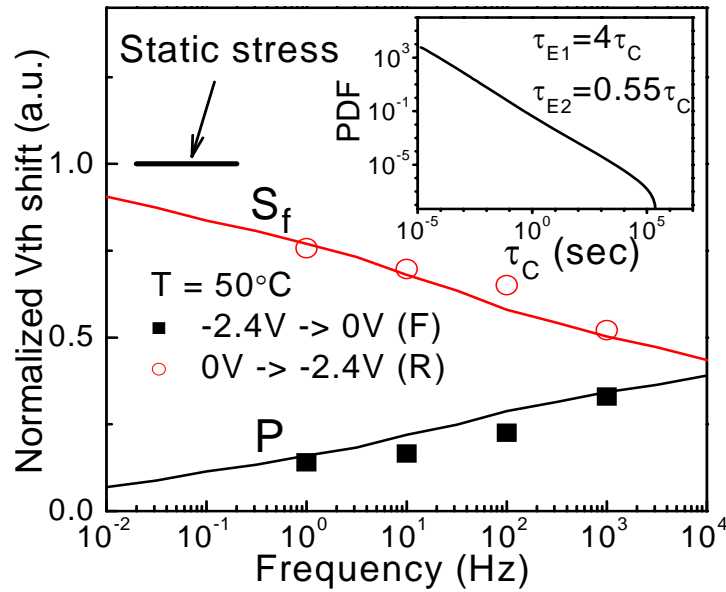
Fig.4-12 ΔV_{th} of p-MOSFET under static and dynamic NBTI stress (measured at *P*) as measured by both fast pulsed method and DC method.

The simulated time evolution of the fast components ($\Delta V_{th,pulse}$-$\Delta V_{th,DC}$) is also plotted in Fig.4-8(b) and Fig.4-9 using solid lines. The measured ΔV_{th} trend agrees well with simulated N_{ot}.

4.4 Impact of the fast NBTI components on circuit applications

Fig.4-8 shows that the transient amplitude of ΔV_{th} under dynamic stress is reduced and approaches zero when the frequency is increased. Therefore no transient effect is expected in the fast digital circuit applications.

For analog applications, a good example is shown in Fig.4-13. Device was stressed under an ultra-low frequency sine wave signal, and ΔV_{th} was measured using the fast pulsed method every few seconds. Since the exponential ΔV_{th}-V_g relationship, the

measured ΔV_{th} is no longer a sine function. This would induce a non-linear signal distortion in ultra-low frequency large signal analog applications.
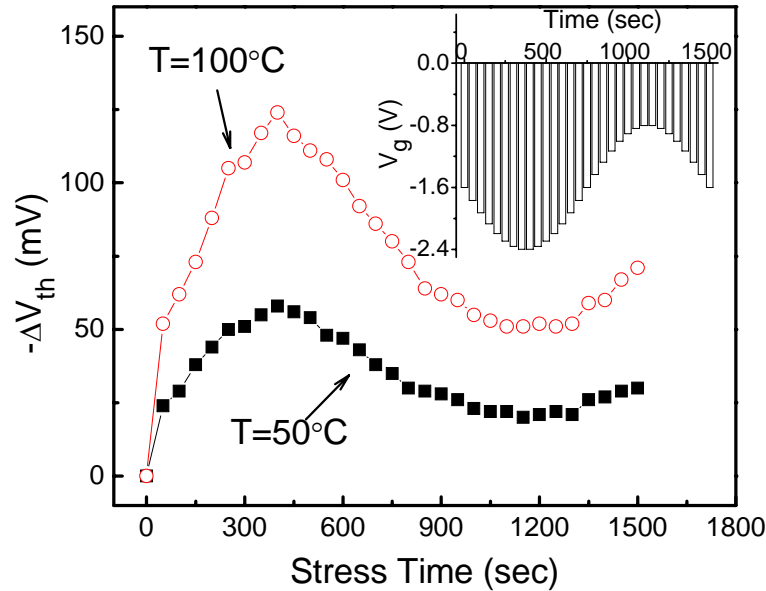

Fig.4-13 ΔV_{th} under a sine wave V_g stress, measured ΔV_{th} is not a sine function of time.

As for the device lifetime, if the charge accumulated in N_{ot} in the stress phase is completely de-trapped in the passivation phase, there is no net accumulation and no effect on the DNBTI device life time. Otherwise there is a net charge accumulation and N_{ot} will contribute to additional DNBTI degradation. Fig.4-7 clearly shows that the later case is true.

Choosing ΔV_{th}=30mV as the failure criterion, the device lifetime is re-estimated under dynamic NBTI stress. Both fast pulsed method and conventional DC method were used, and the result is plotted in Fig.4-14. The DC method overestimates the device lifetime at high stress voltage V_g. However, with stress V_g decreasing and stress time increasing, the slow DNBTI component becomes more significant. Therefore, when doing the lifetime extrapolation to 10 years' time, the DC method is still valid to predict the device lifetime.
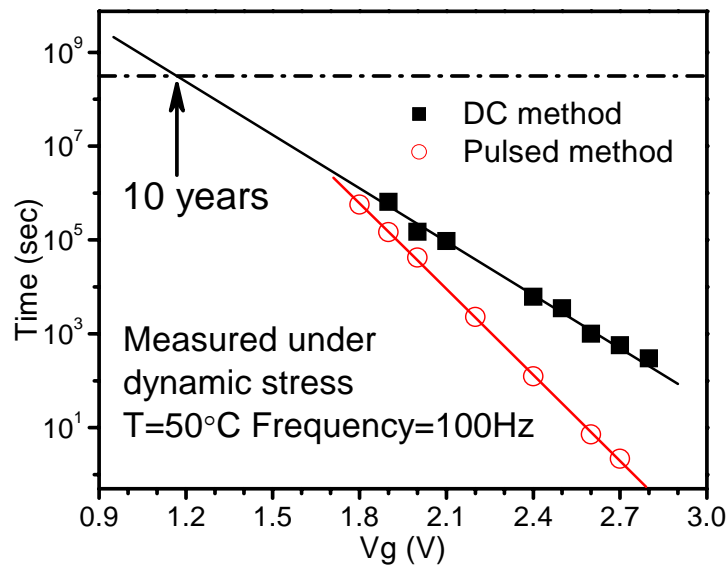
Fig.4-14 Device lifetime re-evaluated under dynamic stress. The fast DNBTI
component affects the device lifetime at high voltage.

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Part II

Advanced passive devices and their application

in circuits

Chapter Five

Proton implanted high-Q inductors

5.1 Introduction

The on-chip inductors are one of the most important components for implementation of RF circuits in CMOS. Due to the lossy nature of Si substrate, the quality factor of CMOS on-chip inductors is low, which has become one of the fundamental barriers of Si VLSI [1]-[6]. There are many techniques reported in the literature to enhance the quality factor of the inductors. These include (i) use of high resistivity silicon substrate, (ii) removal of silicon substrate by micromachining techniques, (iii) use of very thick dielectric layers below the spiral inductors, and (iv) use of high energy proton implantations as a post processing add-on step[4]-[9].

In this chapter, the role of proton implantation in enhancing the Q-factor of inductors has been investigated. The DC resistance of the inductor spirals has been measured for the spirals without proton implantation as well those had undergone the proton implantation. Open pads have been modeled to investigate the influence of proton implantation on the bulk silicon resistivity. The inductors in two cases are both modeled. The improved inductor quality factor results are interpreted in terms of enhanced substrate resistivity by proton implantation.

5.2 Experiments

Circular spiral inductors having turns from 1 to 8 and with two internal diameters of 75μm and 100μm were used in this study. The width of the spiral was 6μm and 10μm respectively in the two cases. A small piece of wafer with the inductors was implanted with high energy protons. The DC resistance of the inductors with and without proton implantation was measured.

For RF characterization, Scattering Parameters (or S-parameters) are essential for practical system characterization in RF regime. S-parameters, which are the reflection and transmission coefficients between the incident and reflection waves, describe completely the behavior of a device under linear conditions at microwave frequency range. Each parameter is typically characterized by magnitude, decibel and phase. The wave functions used to define S-parameters are shown in Fig.5-1 [10] [11].
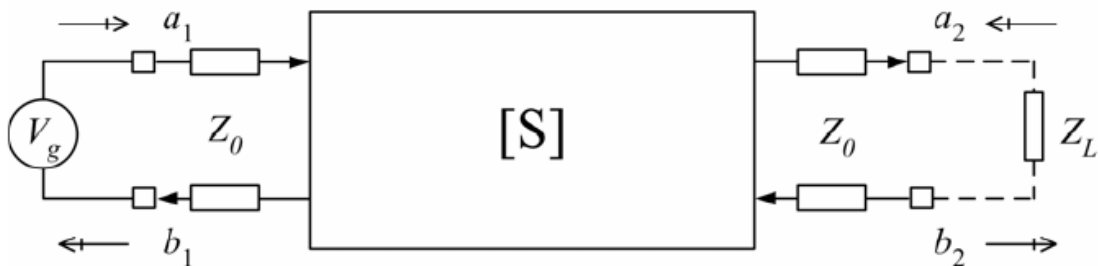
Fig.5-1   Wave functions used to define S-parameters for a two-port network.

Here a_n and b_n (n = 1, 2) are the normalized incident and reflected power waves. The definition equations of S-parameter as shown below:

$$\begin{Bmatrix} b_1 \\ b_2 \end{Bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{Bmatrix} a_1 \\ a_2 \end{Bmatrix} \qquad\qquad 5.1$$

$$\text{where, } \begin{cases} a_n = (1/2\sqrt{Z_0}) \times (V_n + Z_0 I_n) \\ b_n = (1/2\sqrt{Z_0}) \times (V_n - Z_0 I_n) \end{cases} \qquad 5.2$$

For a two port network using matched loads $Z_0 = Z_L = 50\Omega$, S_{11} is the reflection coefficient of the input, S_{22} is the reflection coefficient of the output, S_{21} is the forward transmission gain, and S_{12} is the reverse transmission gain (from output to input).

One-port S-parameters of open pads were modeled using the equivalent circuit shown in Fig.5-2. The equivalent circuit shown in Fig.5-3 was used to model the inductors. In this experiment, S-parameters of the inductors together with the open pads were measured from 50 MHz to 10 GHz using HP 8510C network analyzer with the GGB's air coplanar probes (ACP) for ground-signal-ground (GSG) configuration.
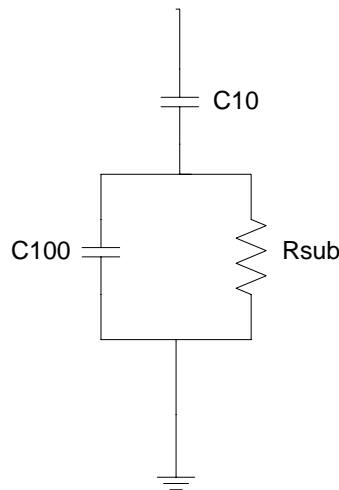
Fig.5-2   Equivalent RF modeling circuit of the open pad.
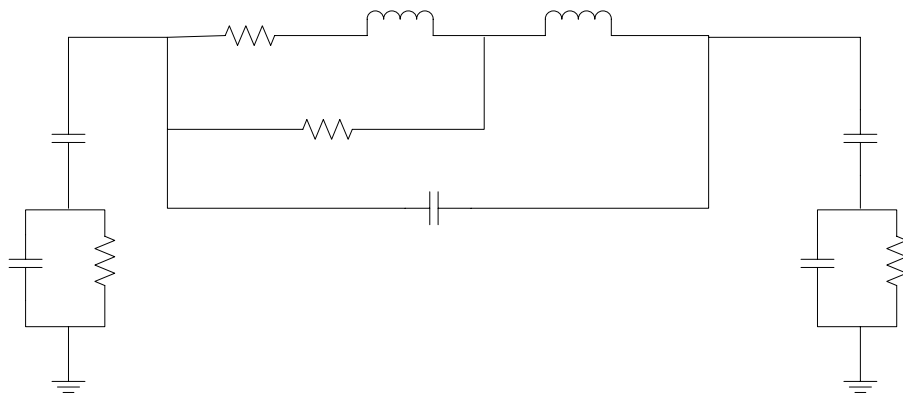
Fig.5-3   Equivalent RF modeling circuit of the inductor.

5.3 Results and discussion on the impact of proton implantation

Fig.5-4 plots the Q values of the inductors as a function of frequency for a 5 and a half turns inductor for the two cases, namely, (i) without proton implantation and (ii) with proton implantation. There is significant improvement in the Q values in case (ii).
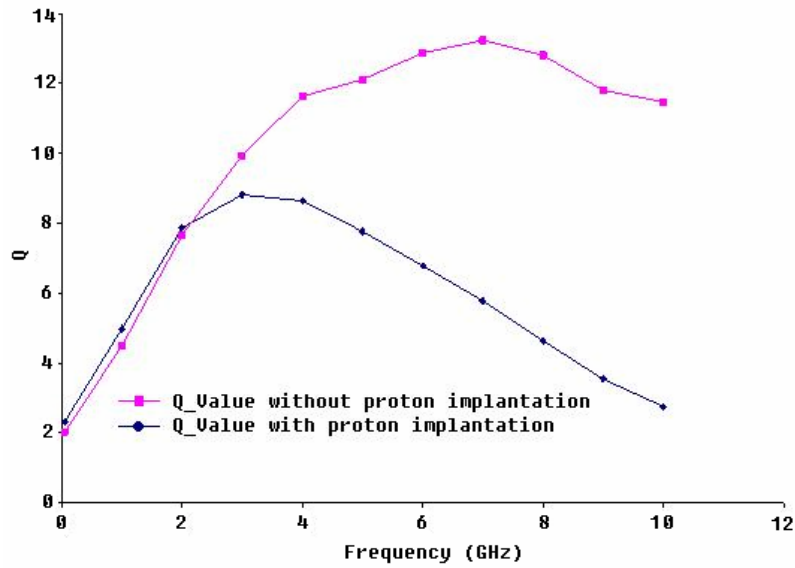

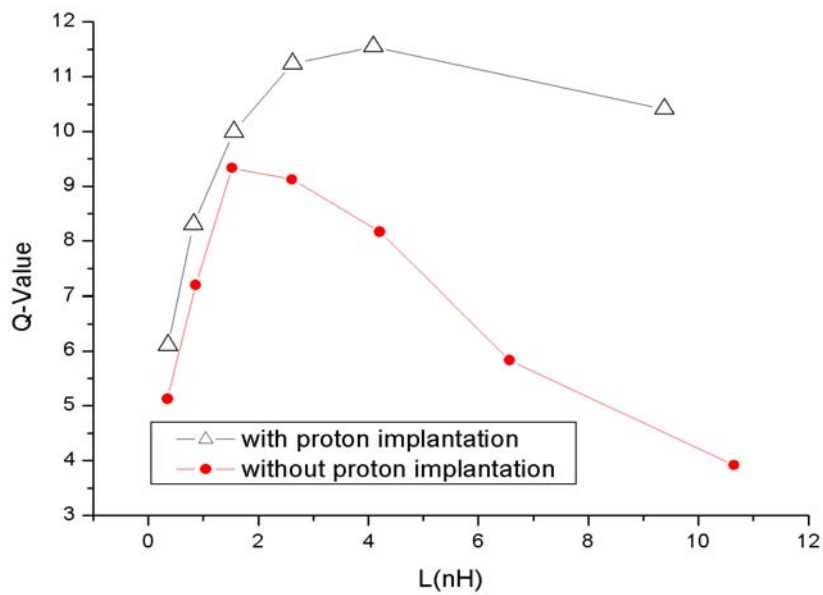Fig.5-4 Q-Value w/ and w/o proton implantation over frequency (c75n5p5)

Fig.5-5 Q-Value w/ and w/o proton implantation @5GHz

Fig.5-5 shows the Q-value with and without proton implantation as a function of inductance values. One observes more improvement in quality factor for larger inductance values. Fig.5-6 shows the improvement ΔQ as a function of number of turns. More improvement was achieved with larger number of turns, or inductors with larger area.
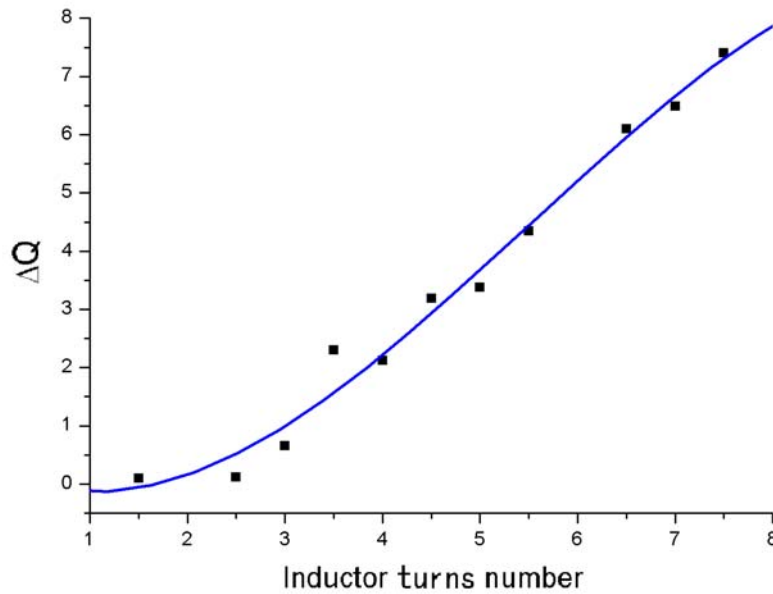
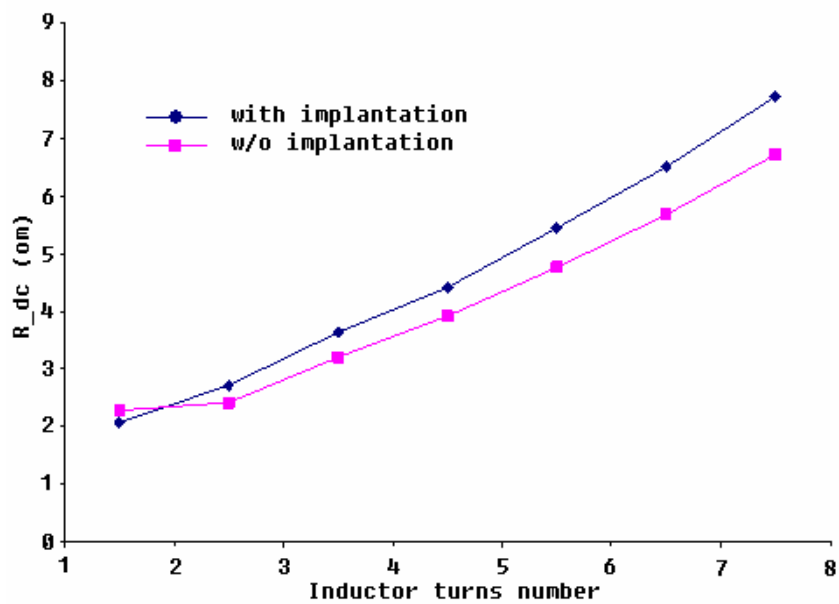Fig.5-6 ΔQ enhanced by post proton implantation on different scales @5GHz

Fig.5-7 DC resistance of the metal spirals w/ and w/o post proton implantation

To investigate the influence of proton implantation on the resistance of metal spirals, the DC resistance of the coils was measured through IV characteristics. Fig.5-6 shows the results. There is no significant change in the DC resistance of the coils as a result of proton implantation.

To investigate the influence on the substrate, one-port S-parameters of open pads were modeled by the equivalent circuit shown in Fig.5-2. The extracted value of substrate resistance – before and after implantation – is indicative of the effect of proton implantation. The substrate resistivity appears to be improved by almost one order of magnitude after proton implantation, while the parasitic capacitors were remained almost the same (as shown in Table. 1-1).

	w/o Imp	w Imp
C10	110fF	100fF
C100	40fF	34fF
Rsub	210Ω	2310Ω

Table.5-1 Substrate parameters of the inductors w/ and w/o post proton implantation

For inductors with small area, the increased substrate resistance does not have very large influence; however, for the larger inductors, this increment is very significant since the substrate loss plays a more significant role in quality factor degradation.

In conclusion, post fabricated proton implantation can increase the substrate resistance significantly, resulting in enhanced Q-value of inductor. This enhancement is significant for the inductors whose value is greater than 2nH and which occupies larger silicon area.

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Chapter Six

High-κ dielectric MIM capacitors

6.1 Introduction

Metal-insulator-metal (MIM) capacitors in silicon integrated circuits have attracted great attention due to their high conductive electrodes and low parasitic capacitance. MIM capacitors are needed for applications including de-coupling of integrated circuits from power supplies, analog functions for RF/wireless applications and termination of transmission lines. Circuit designers need MIM capacitors with good capacitance-voltage linearity, low leakage, high capacitance, a high Q (quality) factor, good device matching, low dielectric loss and 100,000 hours of power-on (POH) reliability with low failure rates.

With device scaling down, the capacitance density of conventional MIM capacitors using silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) is not high enough to meet the requirement predicted by ITRS [1]. Therefore, high-κ material is demanded for the dielectric to obtain greater capacitance on smaller area.

HfO_2 based high-κ dielectrics are able to achieve higher capacitance and to further reduce the parasitic in the MIM capacitors. They are needed to replace silicon nitride and silicon dioxide (SiO_2) in passives and CMOS devices to curb the current leakage that occurs when thin dielectrics are used for device scaling. Continued thickness

reduction of SiO_2 also results in reliability degradation. High-κ dielectrics can be made thicker than conventional dielectric materials, with the same equivalent capacitance, and thereby reducing leakage.

In this chapter, researches have been done on high-κ MIM capacitors using HfO2 based dielectrics. Extensive electrical characterization was conducted to evaluate these high-κ MIM capacitors. DC properties in terms of leakage, voltage coefficients, reliability etc, have been analyzed. In addition, a well behaved RF high-κ MIM model was extracted showing a stable dielectric constants of HfO_2 based dielectrics in wide range of frequency.

6.2 Device fabrication and experimental results

The MIM capacitors with RF test structures were fabricated on standard p-type Si substrates with a resistivity of 4-8Ω·cm. Before defining the bottom electrode of the HfO_2 MIM capacitors, 500nm SiO_2 was deposited on silicon substrate for isolation. The bottom electrode of Ta/TaN was formed by sputtering. Ta was used to reduce the parasitic resistance of the electrode and TaN was acted as an oxidation-resistant barrier layer [2]. Laminated dielectrics with alternate Al_2O_3 (1nm) and HfO_2 (5nm) layers were deposited using Atomic-Layer-Deposition (ALD) technique, as illustrated in Fig.6-1.
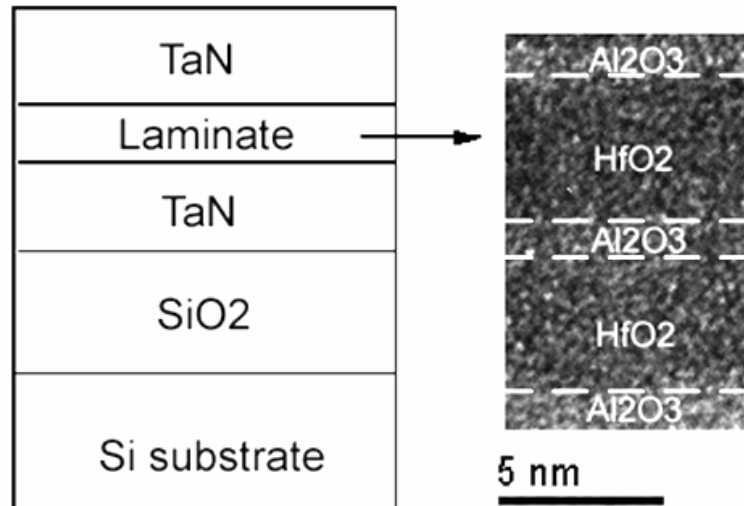
Fig.6-1   TEM cross section of 13 nm HfO$_2$-Al$_2$O$_3$ laminated dielectric.

The beginning and end layers were both Al$_2$O$_3$, which were used to improve the metal/dielectric interface quality [4]. Three thicknesses of laminated dielectrics (i.e. 13, 31 and 43nm) were deposited for electrical evaluation. TaN was then sputtered as the top electrode, followed by the post deposition annealing in N2 at 420°C for 30min. At last, a photolithography step and dry etching were used to define the MIM capacitors. Fig.6-2 illustrates major fabrication steps and schematic top views of MIM capacitor structure for RF characterization. The open dummy device was used to de-embed the parasitic from the bond-pads and transmission lines [5] [6]. In consideration of RF characterization, the coplanar transmission lines were fabricated, which also served as the top and bottom electrodes. Al was used as contact pads after TaN top electrode formation.

(a) Mask 1: Transmission line patterning after bottom electrode deposition

(b) Mask 2: Contact hole etching after high-κ HfO2 deposition
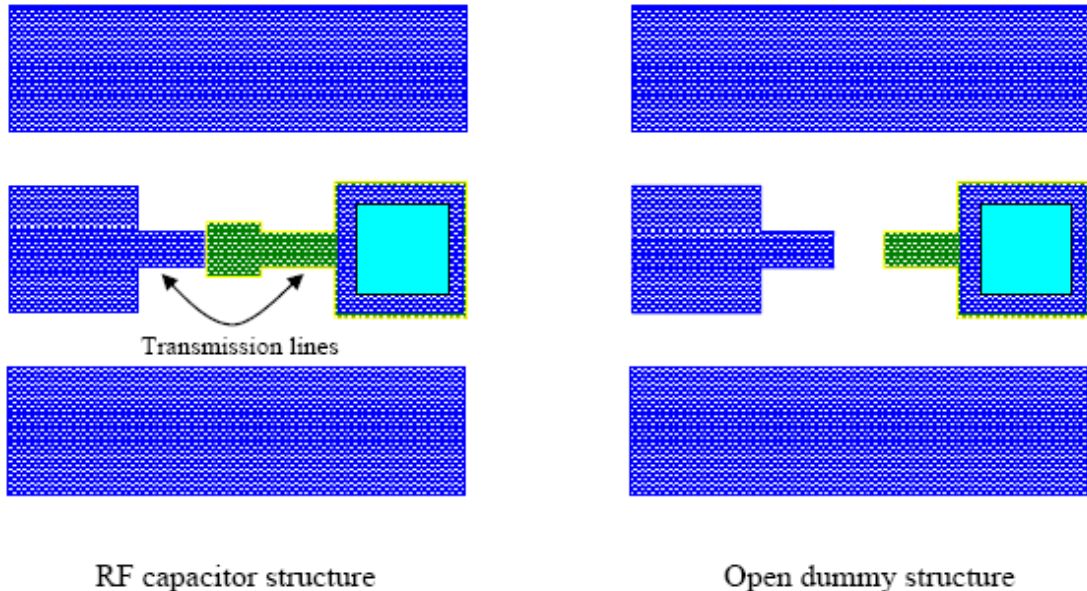
RF capacitor structure   Open dummy structure

(c) Mask 3: RF MIM structures patterning after top electrode deposition

Fig.6-2 Major fabrication steps and schematic top views of RF HfO$_2$ MIM capacitor and open dummy structure.

Leakage current of the MIM capacitors was measured by an HP4156A semiconductor parameter analyzer. The capacitance voltage characteristics were acquired with the help of HP4284A precision LCR meter with frequency ranging from 10kHz to 1MHz. On-wafer S-parameters were measured by HP 8510C network analyzer with the GGB's air coplanar probes (ACP) in ground-signal-ground (GSG) configuration for RF characterization, and a precise calibration procedure including open, short, through, 50Ω load has been implemented using impedance standard substrate before extracting device characterization.

Fig.6-3 shows the dependence of leakage current density (J) on biasing voltage at 125°C for MIM capacitors with different thicknesses of laminate. From the result, the

leakage current density decreases with the increase of the laminate thickness at the same voltage. However, the 13nm HfO$_2$-Al$_2$O$_3$ laminated MIM capacitor can provide much smaller leakage current than previous reported MIM capacitors [7] [8] while maintaining similar capacitance density.
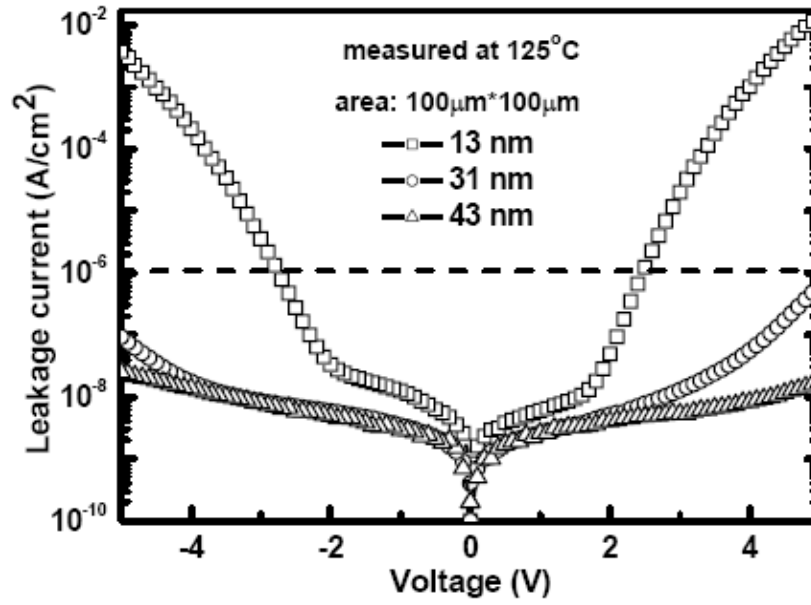

Fig.6-3 Leakage current as bias voltage measured on samples with different dielectric thickness.

Voltage coefficients of capacitance (VCCs) were analyzed by fitting the measured data with the second order polynomial equation:

$$C(V) = C_0(\alpha V^2 + \beta V + 1),$$
(1)

where C_0 is the zero-biased capacitance, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Fig.6-4 shows bias-dependent normalized capacitance ($\Delta C/C_0$) fitted by equation (1). Obviously, α decreases with increasing the laminate thickness. In the case of the 13nm laminated MIM capacitor, β is equal to 211ppm/V at 1MHz, which can easily meet RF capacitor requirement (1000 ppm/V) [1].
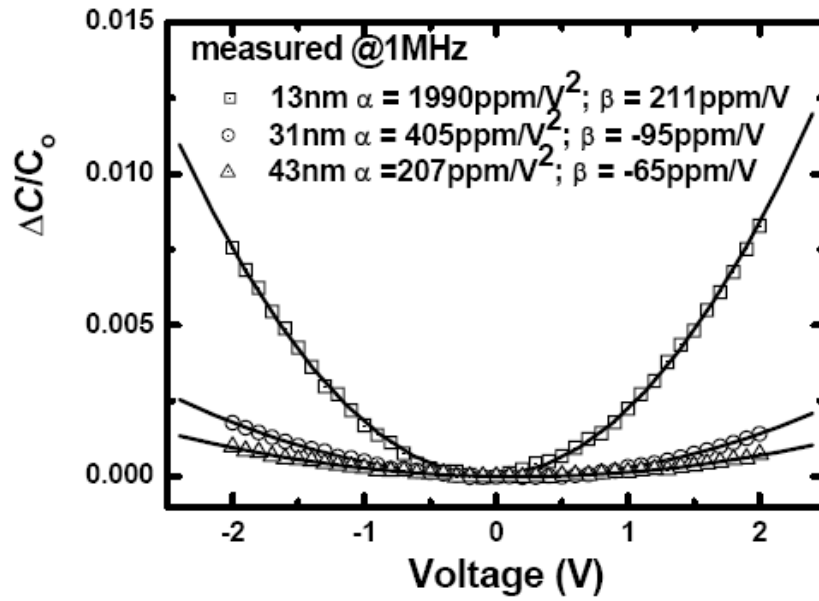
Fig.6-4   The voltage-dependent normalized capacitance (*ΔC/C0*) at 1MHz for 13, 31 and 43 nm laminated capacitors, fitted by a second order polynomial equation

6.3 RF modeling on high-κ MIM capacitors

To investigate the capacitance characteristics of HfO_2 based high-κ MIM capacitors in RF regime, a π network based equivalent circuit model was used as shown in Fig.6-5 [2].
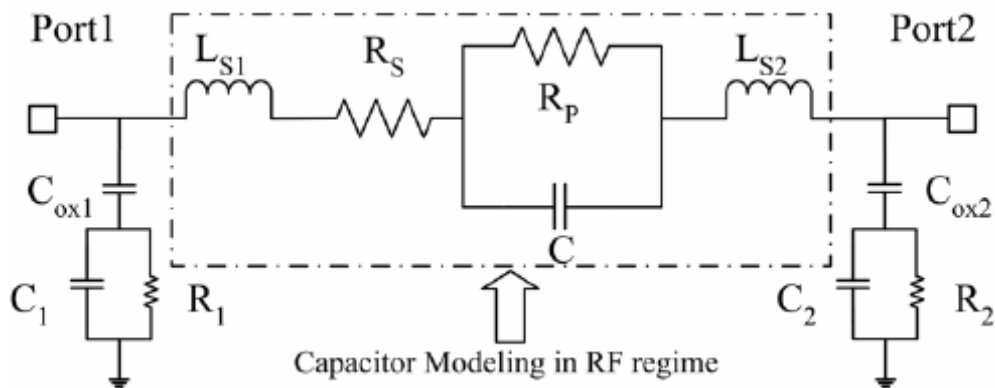

Fig.6-5 The equivalent circuit model for capacitor simulation at RF regime.

The R_p and C describe the basic electrical capacitor model. R_s, L_{s1} and L_{s2} represent the parasitic resistance and inductance from the coplanar transmission lines used for RF measurements. The elements (C_{ox1}, R_1, C_1 and C_{ox2}, R_2, C_2) in the shunt branches represent the coupling from the top and bottom electrodes to ground through SiO_2 and Si substrate. Standard procedures were used to de-embed the parasitic from the probe-pads [9].
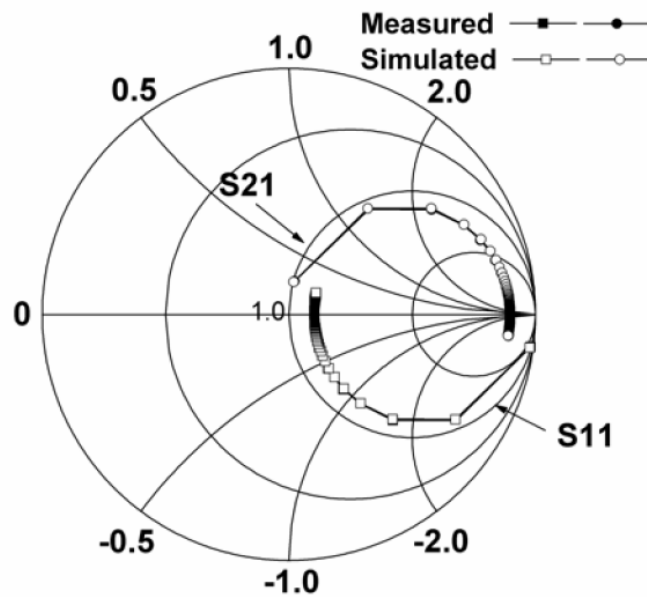
Fig.6-6 Measured and simulated S-parameters for laminated MIM capacitors

The measured two-port S parameters (S_{11} and S_{21}) after de-embedding shunt elements are shown in Fig.6-6. To make the comparison, two-port S parameters simulated by the equivalent circuit (shown in Fig.6-5) are also shown here. It can be found that the measured and simulated data over the entire frequency range from 50MHz to 20GHz are in excellent agreement, suggesting this model is suitable and reliable.

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[2]   Hang Hu, Shi-Jin Ding, H. F. Lim, C. X. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, Subhash C Rustagi, M. B. Yu, C. H. Tung, Anyan Du, Doan My, PD Foo, Albert Chin, and Dim-Lee Kwong, "High Performance ALD HfO2-Al2O3 Laminate MIM Capacitors for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, pp. 15.6.1- 15.6.4, 2003.

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[8]   S. J. Kim, B. J. Cho, M. F. Li, C. Zhu, A. Chin, and D.-L. Kwong, "HfO2 and lanthanide-doped HfO2 MIM capacitors for RF/mixed IC applications," in *Proc. Symp. VLSI Technology,* pp.77-78, 2003.

[9]   C. Chaneliere, J. L. Autran, R. A. B. Devine, and B. Balland, "Tantalum pentoxide (Ta2O5) thin films for advanced dielectric applications," *Materials Science and Engineering*, R22., pp. 269-322 1998.

Chapter Seven

RF and analog circuits using advanced passive devices

7.1 5GHz low noise amplifier (LNA) using high-Q inductors

With the growing of 5GHz wireless LAN (WLAN), high-Q inductors is now essential for the front-end transceiver, i.e. the 5GHz low noise amplifier (LNA). Higher signal gain, lower noise figure (NF) and nice input/output impedance matching (50Ω) at the demanded frequency regime are required to achieve a well performed LNA. In this section, two LNAs were designed using the proton implanted inductors and simulated by CSM 0.18 technology. Circuit characteristics before and after post proton implantation were studied and compared. Simulation results show that the post proton implantation is able to improve the overall characteristic of the RF circuit.

7.1.1 One stage LNA design

Schematic of the one stage LNA is shown in Fig.7-1. Three inductors are used to meet the input/output matching requirement and reach the highest signal gain at 5GHz.
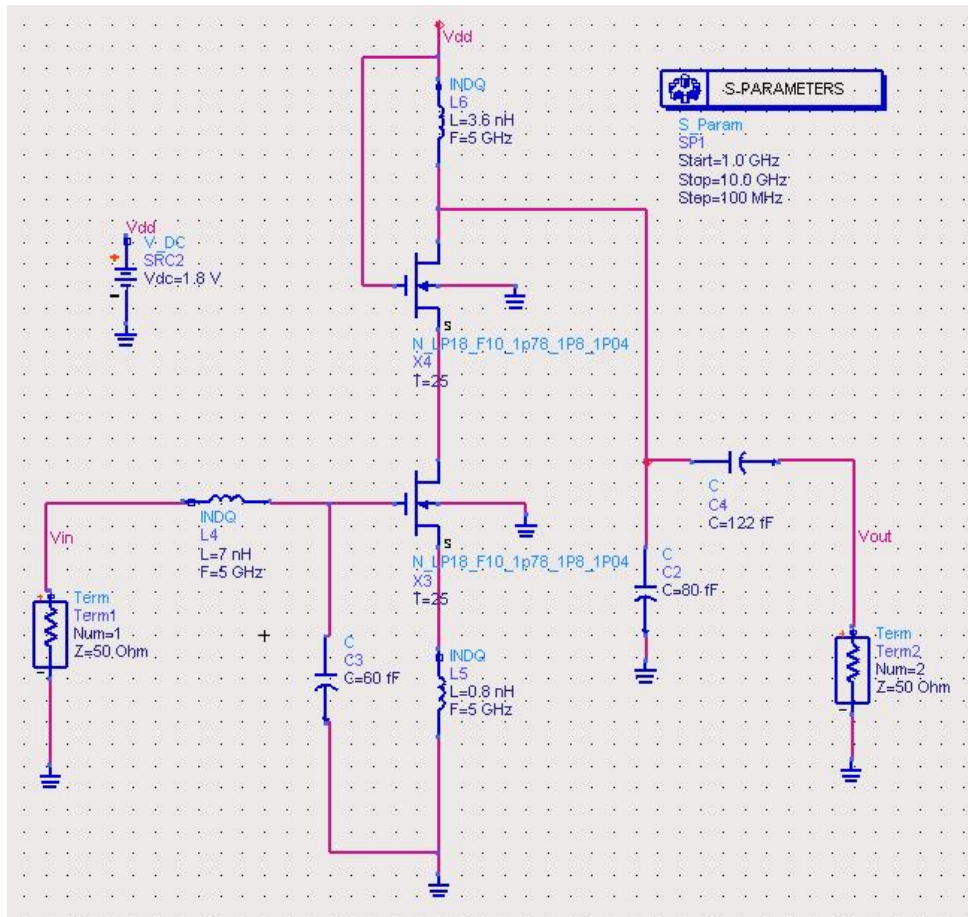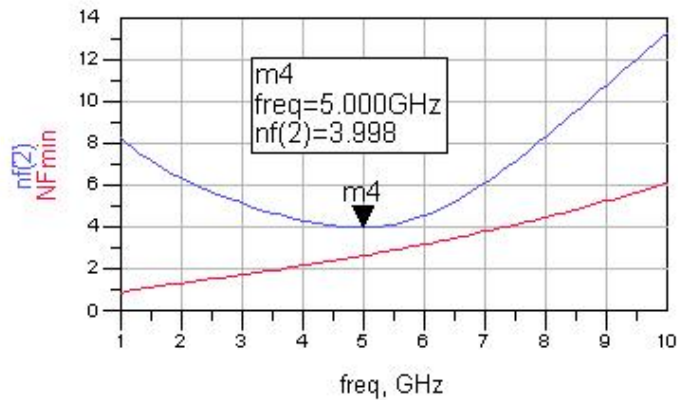
Fig.7-1   Schematic of one-stage LNA.

The circuit was first simulated under frequencies ranging from 50MHz to 10GHz with a standard spiral inductor model without proton implantation. The results are shown in Fig.7-2. The S_{21} parameter, which presents the signal gain of the LNA, is 8.5dB at 5GHz, while the noise figure (NF) is 4.0dB at 5GHz.
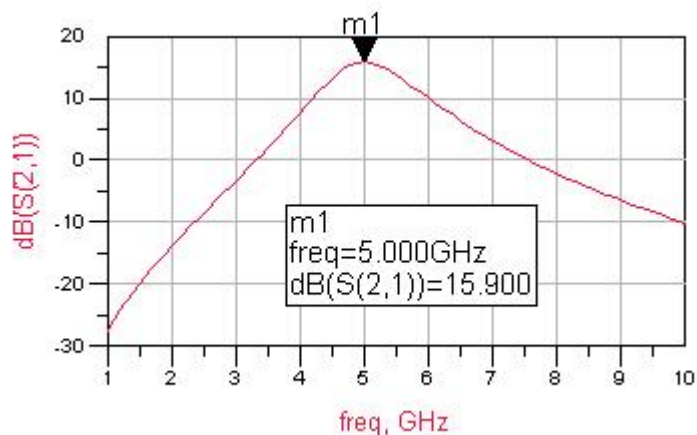

m1
freq=5.000GHz
dB(S(2,1))=8.548
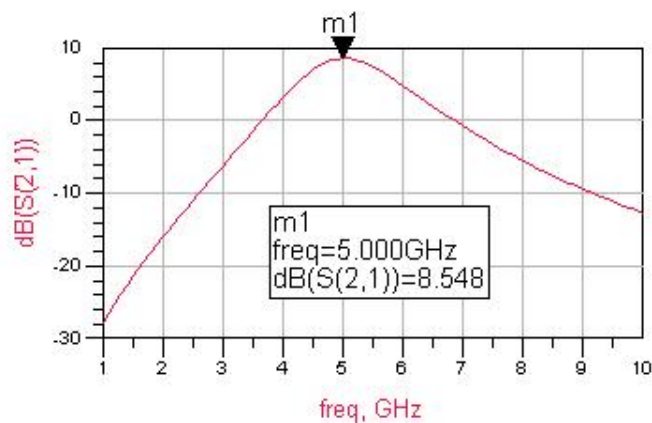
(a)

(b)

Fig.7-2   Simulated results of one-stage LNA w/o proton implantation on
(a) S_{21} parameter; (b) Noise figure.

Simulation was also done with the model of proton implanted inductor (as shown in Fig.7-3). The S_{21} parameter is then increased by 86%, having a value of 15.9dB at 5GHz and the noise figure is suppressed to 2.0dB. Fig.7-4 shows the Smith-Chart of simulation results on input/output impedance (S_{11} and S_{22} parameters), implying very nice input and output matching at 5GHz.

From the simulation results on one-stage LNA circuit, the step of post proton implantation is able to improve the overall performance.

(a)

(b)
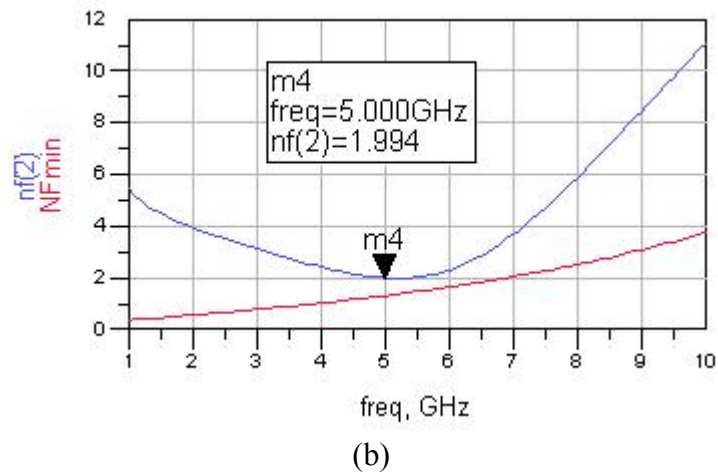
Fig.7-3   Simulated results of one-stage LNA with proton implantation on
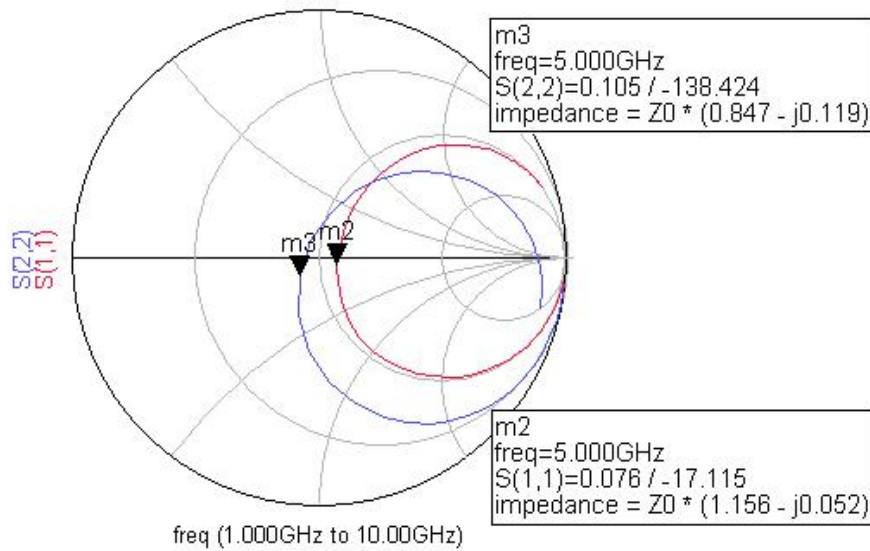(a) S_{21} parameter; (b) Noise figure.

Fig.7-4 S_{11} and S_{22} parameters on Smith Chart of a one-stage LNA after proton
implantation

7.1.2 Two stage LNA design

Schematic of the one stage LNA is shown in Fig.7-5.

The simulation results without and with post proton implantation are shown in Fig.7-6 and Fig.7-7 respectively. The S_{21} parameter was increased by about 50% using proton implanted inductor model, while also suppress the noise figure.
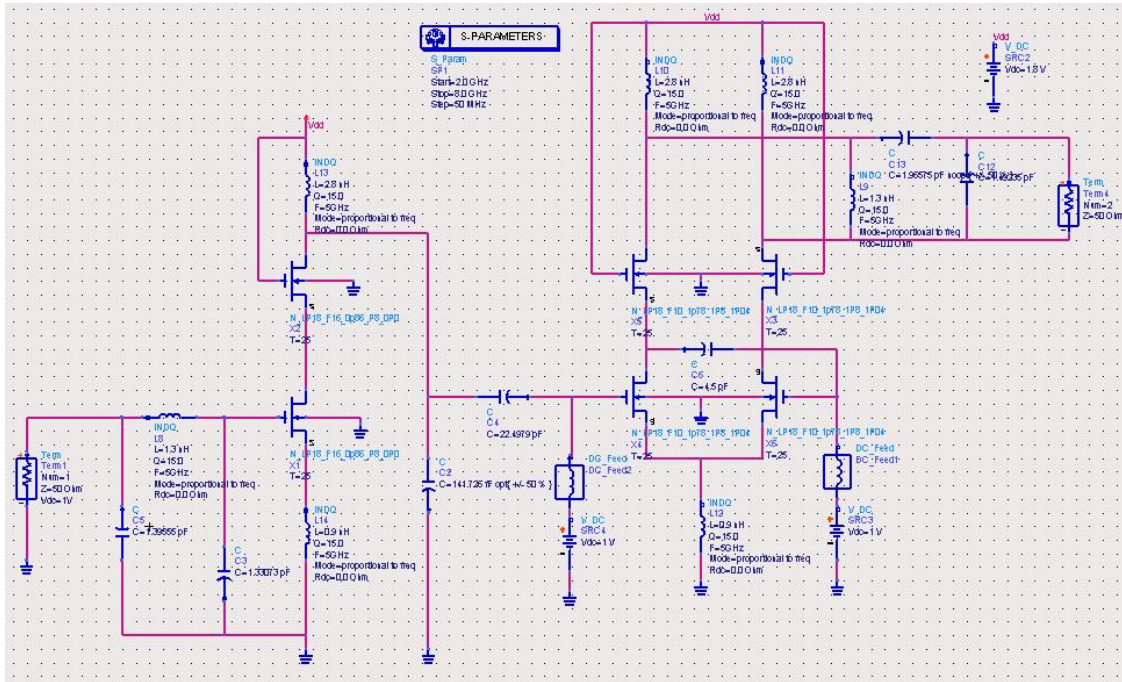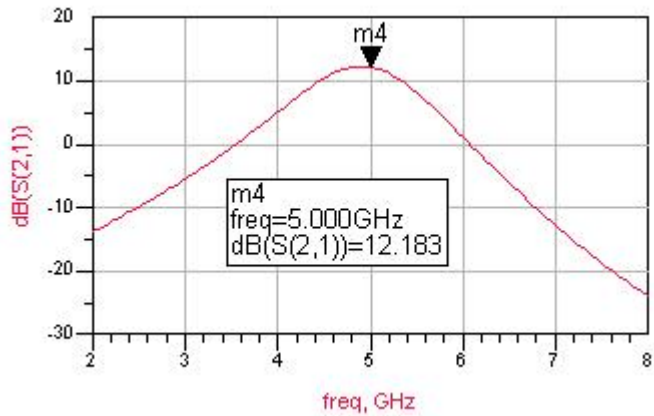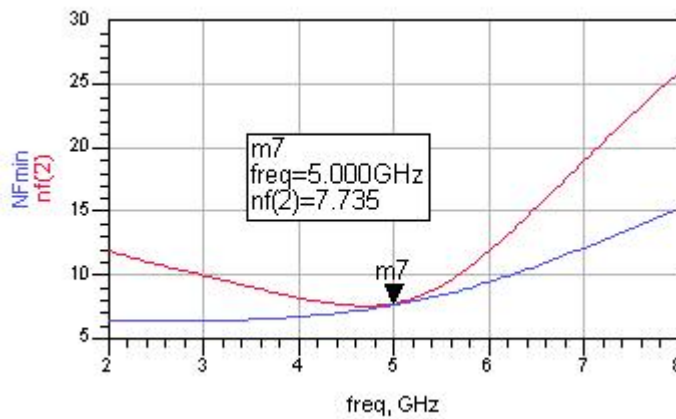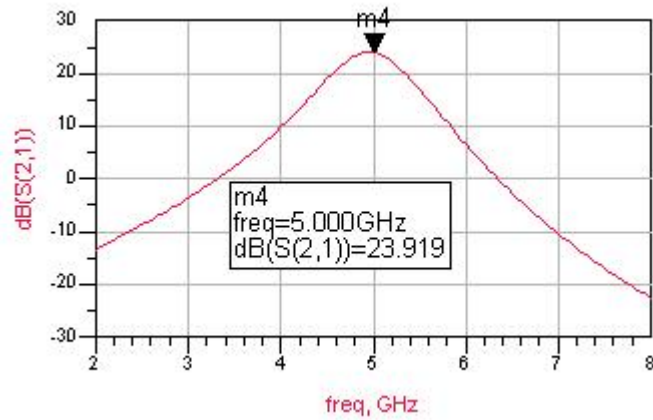
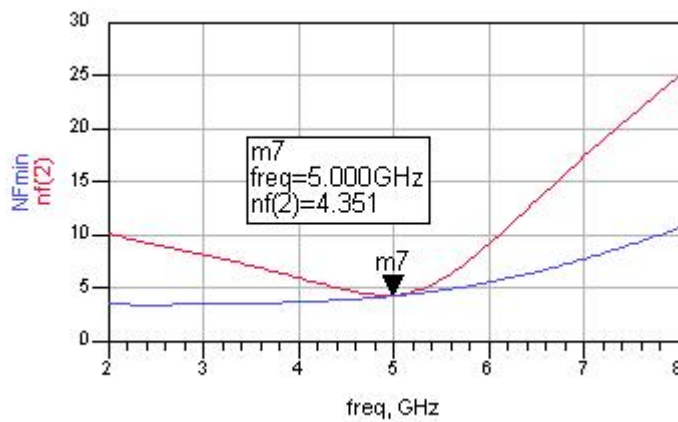Fig.7-5   Schematic of a two-stage LNA.

(a)

(b)

Fig.7-6   Simulated results of two-stage LNA w/o proton implantation on
(a) S_{21} parameter; (b) Noise figure.

(a)

(b)

Fig.7-7   Simulated results of two-stage LNA with proton implantation on
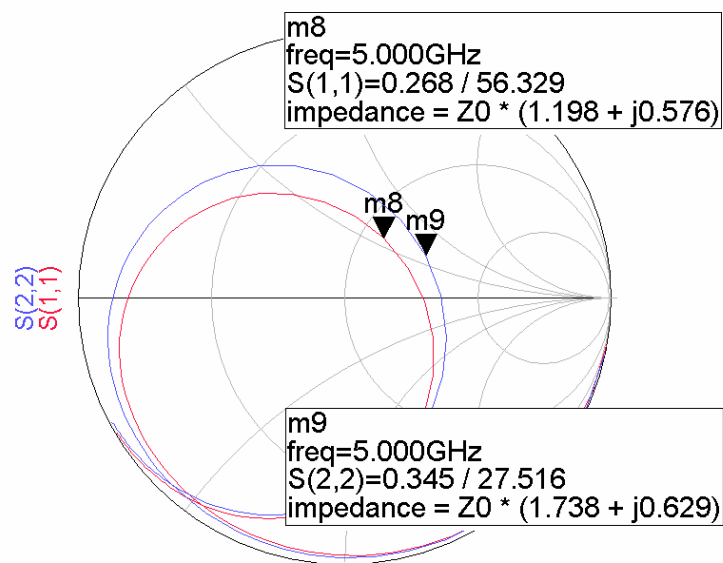(a) Noise figure; (b) S_{21} parameter.

Fig.7-8 S_{11} and S_{22} parameters of two-stage LNA after proton implantation

However, the input/output matching is worse after the implantation as shown in Fig.7-8. It implies that the improvement of Q-factor can sometimes also change the input/output impedance matching. Therefore, if using this technology to design complicated circuits, these issues need to be under consideration carefully.

7.1.3 Conclusions

Table 7-1 summarized the parameters of both one-stage and two-stage LNA with and without post proton implantation upon simulation result. As can be seen from the table, all parameters of one-stage LNA are improved after implantation, while the two-stage one has impedance matching degradation.

	One-stage w/o Imp	One-stage w/ Imp	Two-stage w/o Imp	Two-stage w/ Imp
S_{11}	-11.431	-22.377	-30.540	-11.438
S_{22}	-10.521	-19.574	-25.390	-9.238
S_{21}	8.548	15.900	12.183	23.919
NF	3.998	1.994	7.735	4.351

Table 7-1 Summary of circuit parameters w/ & w/o post proton implantation

7.2 8-bit successive approximation ADC using high-κ MIM capacitor array

In modern CMOS technology, with shrinking of chip size, the area occupied by passive device is becoming a major issue in area scaling down for some circuits, such as charge redistribution based successive approximation analog to digital converter (ADC). Fig.7-9 shows a chip photograph of a 9-bit successive approximation ADC

using conventional passive devices [3]. As show in the figure, more than half of the chip area is occupied by the capacitor array. Therefore, high density MIM capacitors are demanded to decrease the total area of the chip.
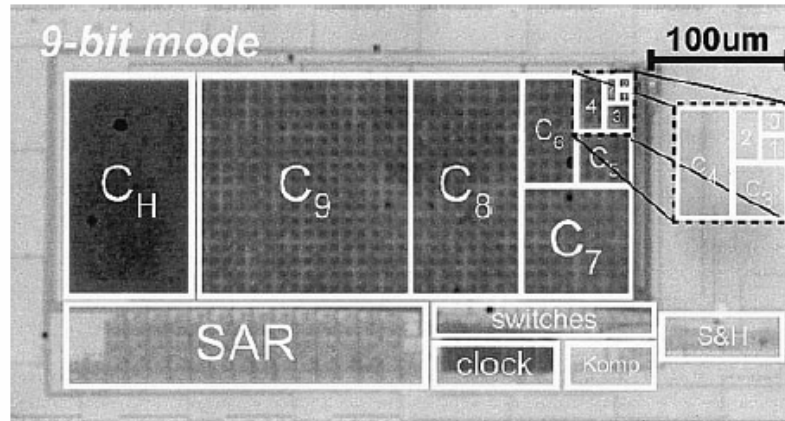

Fig.7-9 Chip photograph of a successive approximation ADC using conventional MIM capacitor

In Fig.7-10, a converter based on a charge redistribution principle is depicted. The converter consists of an S&H stage, a comparator, a successive approximation register (SAR), and a capacitor-based DAC.
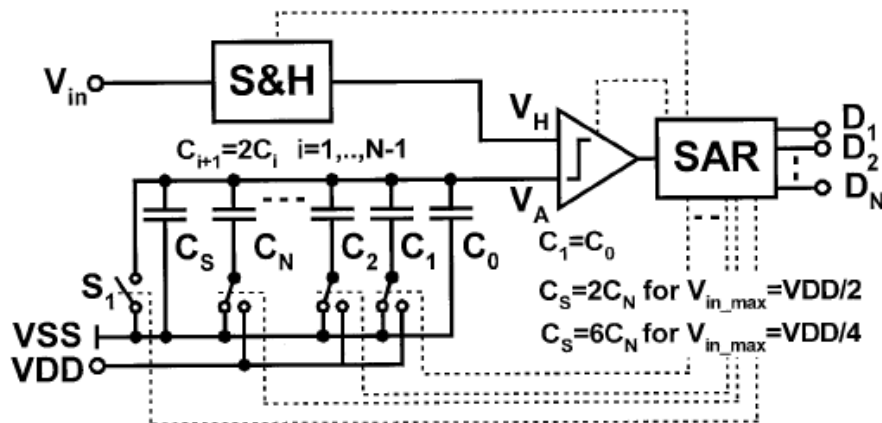

Fig.7-10 Successive approximation architecture based on a charge redistribution principle.

The S&H circuit block diagram is given in Fig.7-11(a). The sampling clock f_s provided by the SAR is divided by two and a non-overlapping two-phase clock is

generated. Both signals are provided in complementary form to control the NMOS switches and the related NMOS dummy switch devices. The sampling capacitors C_{H1} and C_{H2}, which are also integrated on-chip here, are alternately operated in sample and in hold operation. Fig.7-11(b) and (c) show the schematic and layout of the S&H circuit respectively.

(a)

(b)

(c)
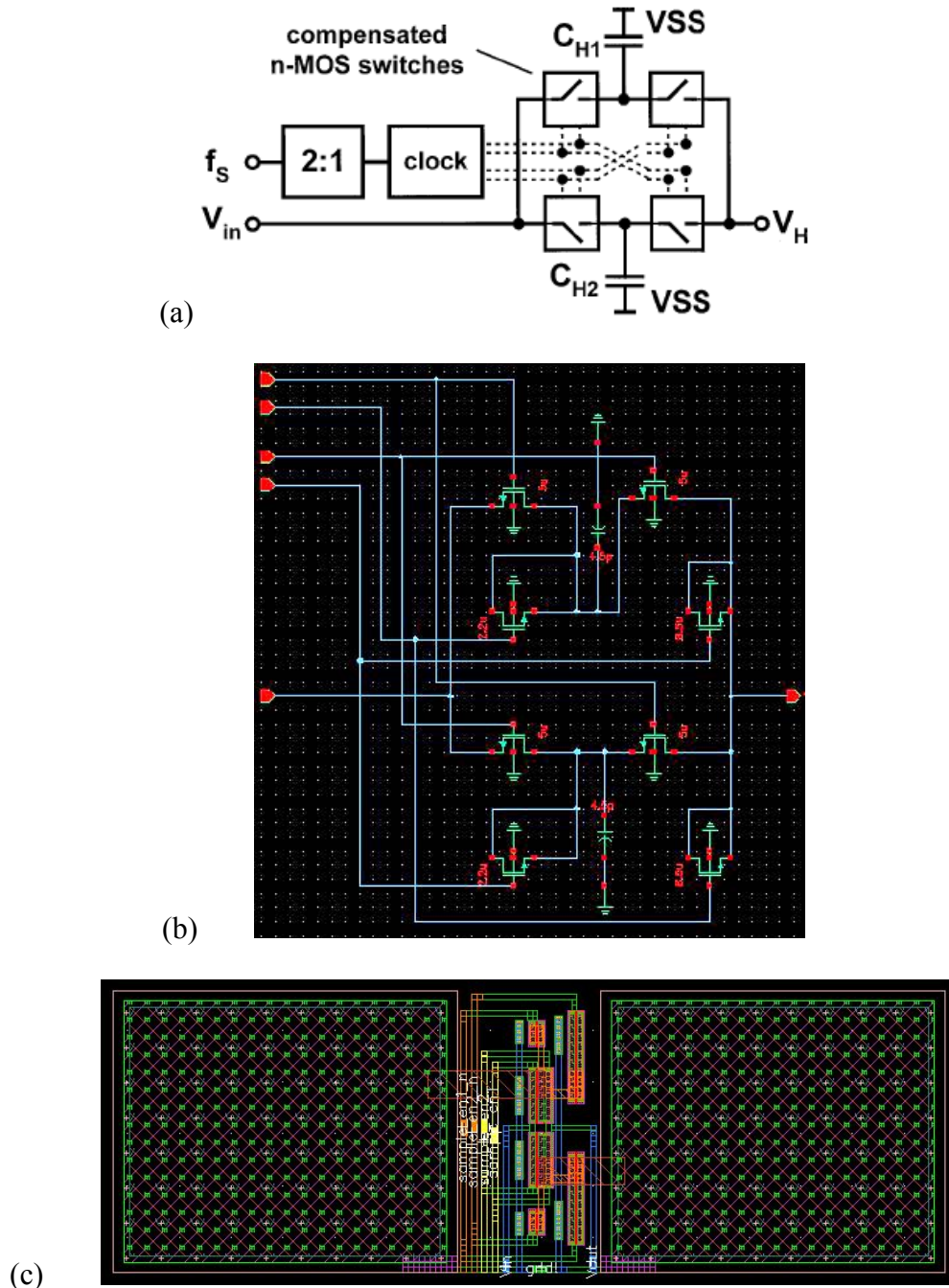
Fig.7-11   S&H circuit: (a) block diagram; (b) schematic; (c) layout.

A two-stage latch-up amplifier is used as the comparator. The circuit schematic is shown in Fig.7-12.

(a)

(b)

Fig.7-12　Comparator circuit: (a) schematic; (b) layout.

Fig.7-13　Layout of the capacitor array.

The capacitors C_0–C_N in Fig.7-10 are realized as multiples of a unit capacitor of 20fF. The layout is shown in Fig.7-13.

Table 7-3 summarizes the area consumption of each circuit block and whole ADC using high-κ MIM capacitors and conventional MIM capacitors respectively. From the comparison, the advantage of using the high-κ MIM capacitors is obvious. It significantly shrinks the whole chip area by almost a half, even with the sampling capacitors integrated on-chip. The simulation result shows good INL and DNL parameters.

	S&H	Comp	SAR	Cap array	Whole chip
High-κ MIM	80×28	45×35	55×110	165×100	175×195
Conventional MIM	80×25	60×25	60×260	150×400	250×400

Table 7-3 Comparison of area of ADC using high-κ MIM and the conventional circuit. (Unit: μm^2)

Reference:

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Chapter Eight

Conclusions

Studies have been done on both active and passive devices in this work. The important findings and conclusions obtained in the course of the studies can be summarized as the following:

In Part One, different measurement techniques used for monitoring the NBTI degradation have been studied thoroughly. The debate on the slow DNBTI component has been clarified. The ΔV_{th} recovery in passivation phase is mainly due to passivation of interface traps N_{it}, rather than N_{ot} de-trapping. Due to passivation of N_{it} during measurement, the conventional CP and DCIV methods seriously underestimate N_{it}.

In addition, a fast DNBTI component due to trapping and de-trapping of hole traps in SiON is distinguished from the slow one for the first time. The fast DNBTI component affects the device lifetime at high voltage and introduces a non-linear distortion in large signal ultra-low frequency analog applications.

In Part Two, proton implanted high quality inductor and high-κ MIM capacitor have been investigated. Simulation results on both analog and RF circuits show improved circuit performance by using these advanced passive devices.

List of publications

[1] T. Yang, M. F. Li, C. Shen, C. H. Ang, C. X. Zhu, Y. C. Yeo, G. Samudra, Subhash C. Rustagi, M. B. Yu, and D. L. Kwong, "Fast and Slow Dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application," in *Symp. on VLSI Tech. Dig.*, pp. 92-93, 2005.

[2] T. Yang, C. Shen, M. F. Li, C. H. Ang, C. X. Zhu, Y.-C. Yeo, G. Samudra, and D. L. Kwong, "Interface trap passivation effect in NBTI measurement for p-MOSFET with SiON gate dielectric," *IEEE Electron Device Letter*, accepted for publication.

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[4] T. Yang, M. F. Li, C. Shen, C. H. Ang, C. X. Zhu, Y. C. Yeo, G. Samudra, Subhash C. Rustagi, M. B. Yu, and D. L. Kwong, "Fast Dynamic NBTI components in p-MOSFET with SiON dielectric," submitted to *IEEE Electron Device Letter*.

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