BED OF NAILS (BON) – 100 MICRONS PITCH WAFER LEVEL OFF-CHIP INTERCONNECTS FOR MICROELECTRONIC PACKAGING APPLICATIONS

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NATIONAL UNIVERSITY OF SINGAPORE
2005

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SUMMARY

The demand for interconnection density both on integrated circuit (IC) and packages increases tremendously as microsystems continue to move towards high speed and microminiaturization technologies. In order to meet the silicon device performance, number of I/Os needs to increase by 15% every year and the cost per pin needs to decrease by 10% every year to match the silicon productivity and cost. In the near future, the necessity for higher I/O count, 10,000 per IC chip requiring fine pitch of <100µm would increase as the IC technology shift towards the nano ICs with feature size of <90nm. In current approaches for chip-to-package interconnections at fine pitch solder interconnects number of limitations was observed. The main failure in these solder interconnects are due to the CTE mismatch between the Si chip and substrate. Especially in fine pitches, assembly yield and process costs are found to be higher due to the low stand off height and less solder volume. Thus, the present interconnection technologies cannot meet the essential requirements of reliability, cost, performance and manufacturability. Hence, in this present work, a new technology namely Bed of Nails (BoN) interconnections was conceived, designed, fabricated and tested to meet the above requirements. The fabrication uses conventional wafer level process, hence it is convenient to mass produce these interconnects. This work also highlights the challenges in high aspect ratio lithography process (50µm diameter and 100-130µm height) and electroplating of copper nails.

The test chips were designed and fabricated based on the optimized process developed. Two different test chips of 10 mm × 10 mm and 20 mm × 200 mm sizes were fabricated. The fabricated test chip with BoN interconnects was assembled on

conventional test board using Karl-Suss flip chip bonder (FC-150). This interconnects were subjected to thermal cycle test as per the JEDEC standards. Results obtained clearly showed that BoN interconnects are at least better by a factor two compared to the conventional solder interconnects. Failure modes of the samples were analyzed using scanning electron microscopy and major failures were observed in the bulk solder. These failures can be further reduced by using solder of better properties. The wafer level interconnects Bed of Nails developed in this study can be implemented for fine pitch interconnect schemes between Si chip and substrate.

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CHAPTER 1

INTRODUCTION

The rapid advances in IC design and fabrication continue to challenge electronic packaging technology, in terms of fine pitch, high performance, low cost and better reliability. In the near future, the demands for higher I/O count per integrated circuit (IC) chip increases as IC technology shifts towards the nano ICs with a feature size less than 90nm. According to Rent's rule the I/O counts will increase to around 10,000 by 2014 [1]. The demand for packages with increased I/O counts and decreased die size will result in the requirement for fine pitch I/Os.

The International Technology Roadmap for Semiconductors (ITRS) sponsored by the Semiconductors Industry Association (SIA) has given the future I/Os pitch requirements according to the IC technology advancements. Table 1.1 shows the ITRS 2003 I/O requirements for advanced IC assembly and packaging [2]. The minimum feature size in IC component will reach 45nm by 2010, requiring an area array chip-to-substrate interconnect pitch of less than 100µm. As microsystems continue to move towards high speed and microminiaturization technologies, the stringent electrical and mechanical properties are required. Current chip-to-substrate interconnects cannot meet the above requirements. This bottleneck in the packaging industry will potentially limit the future progress in IC technology.

In the past four decades, various types of microelectronics packaging technologies have been developed to accommodate the decreasing feature size and increasing I/O density of ICs, which are discussed in the next chapter. It is very important for the chip-

to-next level substrate interconnect technology to accommodate to these trends in the development of microelectronic packaging. Thus the main focus of this research is on interconnects between chip-to-next level substrate for IC packaging which is also addressed as first-level or off-chip interconnect.

Table 1.1 ITRS 2003 for Assembly and Packaging [ITRS 2003]

Year of production	2004	2005	2007	2010	2013	2016
DRAM ½ Pitch (nm)	90	80	65	45	32	22
MPU Physical Gate Length (nm)	37	32	25	18	13	9
Chip Interconnect Pitch (μm)						
Flip Chip area array	150	130	120	90	90	80
Peripheral flip chip	60	40	30	20	20	15

The main criteria involved in the development of the first level interconnect technology are:

- High count I/Os
- Good electrical performance
- Better thermo-mechanical reliability
- Good manufacturability
- Low cost

In the current electronic packaging industry, the three most widely used off-chip interconnect technologies are wire bonding, tape automated bonding (TAB) and solder bump joints for flip chip (FC) packaging. Solder bump interconnects serve to meet the

requirements of high performance ICs due to the area array capabilities of solder bumps because it meets the requirements of increased I/O density and also provides shorter leads, lower inductance, higher frequency, small device footprint, and lower profile when compared to wire bonding and TAB.

As stated in Table 1.1 earlier, the pitch of area-array flip chip packages will reach 80µm by 2016. Electroplating solder balls could result in a pitch of 80µm, but this small pitch and the short standoff height of interconnects would decrease the thermo-mechanical reliability. The predominant failure mode in flip-chip technology was the thermo-mechanical fatigue of solder joints which eventually resulted in decreased reliability. The reason for this failure was attributed to the mismatch in the coefficient of thermal expansion (CTE) between IC and organic substrate, and the geometrical constraints of the package coupled with temperature excursions during assembly and operation [3].

To improve this reliability, the use of underfill material in the gap between the IC and substrate was suggested [1]. But the use of underfill added cost to the assembly and has moisture related reliability issues. Hence the packaging industry, particularly the consumer product industry prefers packages with no underfill, as one process step was eliminated with reworkability [4]. Moreover, as the pitch size between solder bumps reduces, the height of the solder bumps, and thus the gap between the chip and the substrate, is also reduced. Therefore the cost and the difficulties of underfill dispensing and solder reflow and attaching increases [5].

The potential solutions for the above problems can be summarized as follows

- develop flexible interconnect structure that can withstand the strain energy and thus reduce interconnect failures
- use low CTE boards
- underfill free interconnects
- increase the stand-off of the solder joints

In order to meet some of the above requirements, nano packaging is the only solution offered. Nano packaging comes at two levels namely wafer level and board level packaging. The nano wafer level packaging group, a collaboration project in Singapore, has proposed various wafer level interconnect schemes to develop 100µm pitch interconnects at wafer level. The Bed of Nails (BoN) interconnect technology is one of the schemes proposed. The main objective of this research is to develop the fabrication process of the above off-chip interconnect at 100µm pitch and to assess its reliability

In chapter 2, a literature survey of microelectronic packaging, wafer level packaging and compliant interconnects is presented followed by experimental details in chapter 3. BoN interconnects conceptual design and fabrication process development are discussed in chapter 4 followed by test chip demonstrator design and its fabrication process in chapter 5. Test board design, assembly process and reliability results of BoN interconnects are reported in chapter 6. Finally the thesis ends with main conclusions and a few recommendations for future work in chapter 7.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction to Microelectronics Packaging

Microelectronics is stated as the first and foremost important technology wave in microsystems technologies. It started with the invention of the transistor instead of vacuum tubes. Microelectronics typically, refers to those micro devices, such as integrated circuits (ICs), which are fabricated in sub-micron dimensions and which form the basis of all electronic products. Integrated circuits are defined as a miniature or microelectronic device that integrates elements such as transistors, resistors dielectrics and capacitors into an electrical circuit possessing a specific function [1]. Packaging can be defined as the bridge that interconnects the ICs and other components into a system-level board to form electronic products. Packaging of microelectronics (ICs) is referred to as microelectronics packaging.

Packaging is essential because IC devices cannot function without proper packaging, even though transistors act as brains of IC. The essential functions of the conventional IC packaging are listed as follows:

- To protect IC chips from the external environment.
- To facilitate the packaging and handling of IC chips.
- To dissipate heat generated by IC chips for proper operation of transistors and interconnects.
- To protect the electrical characteristics of the IC.

- To provide paths to distribute signals between chips and to supply voltage and current to the circuits within a chip, as well as to other ICs in a given system, for their operation.

Continuous advances in reducing the size of the transistors allowed the progressive integration of tens, hundreds, to thousands of transistors on a single IC in technologies called small, medium and large scale integration (SSI, MSI and LSI) which evolved into an era of very large or ultra scale integration (VLSI or ULSI) that consists of millions of transistors in a single IC.

In general, IC packages can be classified into two categories namely, Through-Hole and Surface Mount Packages. If the packages have pins that can be inserted into holes in the printed wiring board (PWB), they are called through–hole packaging. If the packages are not inserted into the PWB, but are mounted on the surface of the PWB, they are called surface mount packages. The three most important parameters for packaging ICs as listed in the IC roadmap are given as follows [1]:

(1) I/O which controls the pitch of the IC package and the wiring needs at system level.

(2) Size of the IC which controls the reliability of the IC to package connection.

(3) Power which controls heat dissipation properties of IC and system-level packaging.

Microelectronics packaging and interconnection technologies have undergone both evolutionary and revolutionary changes to serve the trend towards miniaturization in electronic equipment, which is presently evident in military, telecommunications, industrial and consumer applications. The trend has been driven by various forces

including specialist requirements for size and weight as well as cost and aesthetics, which have led to various innovative developments in packaging of integrated circuits and in connectivity on electronics substrates and circuit boards [6].

2.2 Hierarchies of IC packaging

Packaging hierarchy can be divided into different levels in terms of its integration level as shown in Figure 2.1.

At the IC level, packaging involves interconnecting, powering, cooling and protecting ICs. A piece of IC die is generally attached to a chip carrier and the I/O pads on the IC connected to a lead frame by wire bonding. The assembly is then encapsulated. This is referred to as Level 1 in the packaging hierarchy.

Packaging a single IC does not generally lead to a complete system since a typical system requires a number of different active and passive devices. System–level packaging involves interconnection of all these packaged IC chips and components to be assembled on the system level board (PCB) by either through-hole or surface mount technology. The conductor traces on PCB works as communication paths between different IC chips and components by connecting every component so as to form one interconnected system. This is referred to as Level 2 in the packaging hierarchy.

A single system-level board may not carry all the components (ICs) necessary to form some total systems such as mainframes and supercomputers as they require a very large number of ICs. In this case, the several boards necessary to make up the entire system are typically connected through connectors, sockets and cables. This is referred to as Level 3 in the packaging hierarchy.

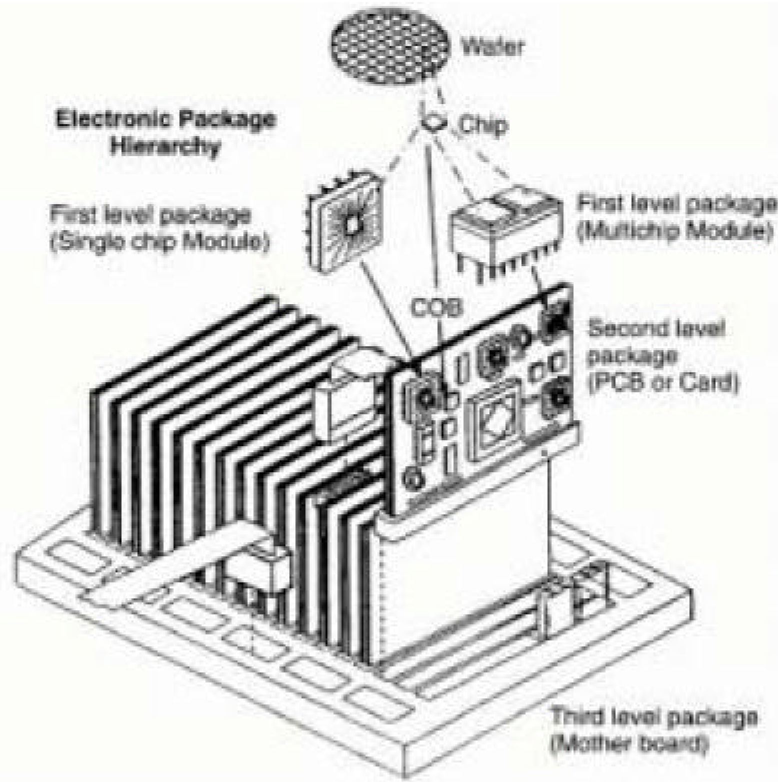


Figure 2.1 Hierarchy of electronic packaging [1]

2.3 Historical development of packaging technology

With increasing integration and higher speed ICs and with the miniaturization of electronic equipment, newer packaging systems have been requested by the industry which incorporates the following functions to the above stated functions [7]:

- Multi-pin I/O.
- Ultra-miniature packages.
- Packages suited for high density ICs.
- Improved heat resistance for use with reflow soldering techniques.
- High throughput speed.
- Improved heat dissipation.

- Lower cost per pin.

To resolve these requirements, a great number of packaging schemes are evolved in the market and used for various applications. These technologies have been developed which varies in their structure, materials, fabrication methodology, bonding technologies, package size and thickness, number of I/O connections, heat removal capability, electrical performance, reliability and cost.

As shown in Figure 2.2, packages have been evolving into smaller size and higher pin count to be compatible with the ever increasing density and complexity demand of ICs. The first development in the packaging technology is the dual-in-line packages (DIP) which gained most popularity in 1970's and 1980's. DIP is through-hole package type, in which, I/Os, or the pins are distributed along the sides of the package. Though many packages have been developed, DIP is used for four decades (after its first introduction), because of its low cost and high reliability. Shrink DIP (SH-DIP), skinny DIP (SK-DIP), slim DIP (SL-DIP), ceramic DIP (CER-DIP) are the different types of DIPs with different number of pins. Since DIPs have upper limitation of the number of I/Os or pins as 64, to achieve higher I/O connections, DIPs have given way to pin grid arrays (PGA) which is also a through-hole package, where the pins are distributed in an area array fashion underneath the package surface.

Through-hole packages are inherently limited in some application due to their big size or inefficient use of the PCB estate, and thus the solution comes with the emergence of surface mount packages in 1980's. Surface mount packages occupy only one side of the PCB estate and thus significantly increase the second level packaging density compared with through-hole packages. Elimination of drilling holes for through-hole

packages also means that smaller pins with smaller pitches can be obtained. In the surface mount packages, the small outline package (SO or SOP) is the first package and most widely used package in modern memory for low I/O applications because of its extremely low cost. Another technology, the Quad flat package (QFP) is an extension of the SOP with larger I/O connections. Both the SOP and QFP have leads that can be attached to the PWB whereas further technology development has led to the evolution of leadless chip packages such as leadless chip carrier (LCC), plastic lead chip carrier (PLCC) and SOJ. In the late 1980's, packages with solder balls are developed as an alternative to packages with leads. The solder balls can be placed underneath the surface of the package in an array and can significantly increase the I/O count of the surface mount packages, for example, ball grid array (BGA) and flip chip packages. It should be noted that some packages, like flip chip packaging, are different from others such as SOP in the manner of connection between IC dies and carriers.

As the name implies, in flip chip technology the die is flipped upside down with the active side connected to the carriers by solder balls, which is in sharp contrast with DIP devices where the die is wire-bonded to the carrier. Flip chip devices are electrically superior to conventional dual-in-line (DIP) and pin grid array (PGA) packages since electrical parasitic associated with long bonding wires and lead frame pins are effectively eliminated. Although reliability concern and cost issues are still to be resolved before flip chip technology finally replaces wire bonding technology [8]. It is gradually accepted that flip chip technology is the right direction especially for high pin count devices. Furthermore, by properly applying underfill material between chip and carrier, reliability

of flip chip packages can be enhanced by a factor of ten [9]. Solder or gold bumps are used in flip chip technology, and the correct choice is application dependent [10-11].

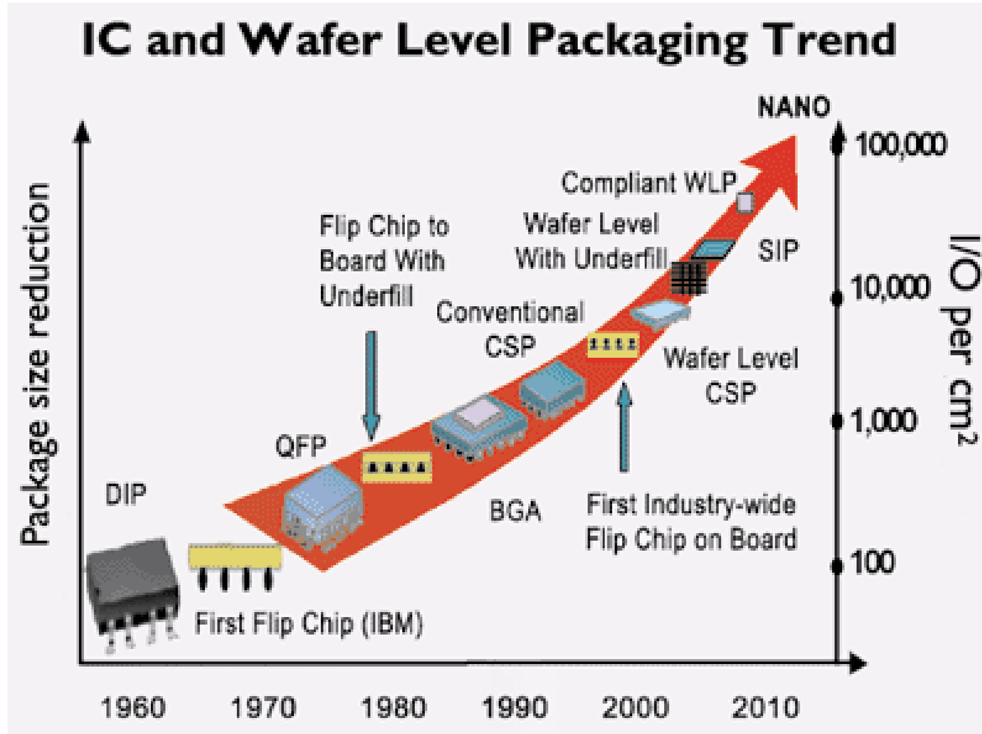


Figure 2.2 Packaging trends [12]

The Chip scale package (CSP) has been developed to address the demands of modern electronics, like portable and hand held products, which require smaller, thinner and lighter packages. A CSP is defined as package whose area is less than 1.2 times the area of the IC package. Generally, CSP devices have solder ball interconnects with a diameter of 0.3mm and a pitch of 0.5mm and CSP package may come as small as 5x5mm^2 and 1 mm thick. Various CSP manufacturing methodologies have been developed by major semiconductor companies such as National semiconductor, Motorola and Fujitsu etc. Typical CSPs can be divided into lead frame, rigid and flexible substrate with flip chip and ceramics substrate with wire bond and flip chip types, but they still

follow the conventional packaging process, i.e., die singulation before packaging. On the other hand, wafer level packaging (WLP) technology such as wafer level CSP (WL-CSP) attracted greater interest from industry because it is cost effective, easy to test and has a small footprint and low profile. The unique feature of the wafer level approach is that the package is completed directly on the wafer then singulated by dicing for the assembly in a flip chip fashion. All WL-CSPs are real chip-size rather than chip-scale due to the wafer level processing. The industry may finally move to direct chip attach (DCA) technology that eliminates the first level package and thus further reduce cost, but the current infrastructure is still more suitable to CSPs and CSP devices which are easier to handle, assemble, test at higher speed and rework when compared to DCA.

With the decreasing feature size of ICs and packages, the RC delay and crosstalk effect might result in the serious problem that the signal integrity cannot be obtained with the packaging technologies mentioned above. Therefore, alternative packaging approaches have been proposed, including optical packaging, RF packaging and 3-D stack packaging [13-14]. Both on-chip and off-chip data transmissions are expected to improve with the enhancement in packaging density [15].

2.4 Challenges in microelectronics packaging

The microelectronics packaging industry continues to face technical challenges as long as market demands for modern electronics, like more portable and hand held, light weight, and high performance products. As a guide for research direction in the packaging field, the International Technology Roadmap for Semiconductors (ITRS) clearly indicates the technical challenges that could be roughly categorized as Printed Circuit Board (PCB) related, materials related, and design and simulation challenges [16].

With the increasing complexity and integration of semiconductor technology, PCB fabrication has become a bottle-neck for IC development. On-chip Input/Output pin (I/Os) numbers increases with increasing the number of transistors according to Rent's rule, while chip size keeps falling. As a result more stringent requirements are imposed on the corresponding metal pads on PCBs in terms of their size and pitch. To realize the fine-pitch board-level interconnects, micro via and soldering technologies need to be further improved for fabrication of reliable, multi-layer PCBs. PCB research is still focused on organic substrates due to their cost consideration. Advanced organic substrates must have higher glass transition temperature (Tg) to be compatible with the high temperature processing of Pb-free solder, increased wireability at low cost, improved planarity and low warpage at higher process temperatures, low moisture adsorption, low cost, increased via density in substrate core, low cost embedded passives. Electrically, the substrates must have improved impedance control and lower dielectric loss to support higher frequency applications.

Drastic improvements in materials properties will be required to support the technology nodes driven by projected semiconductor requirements in power, frequency and I/O, and as well as market requirements in cost, size, weight, and environment. Major material challenges are placed on underfill, copper/ low-k dielectrics, and Pb-free solders. Underfill is a liquid polymer-based composite that is dispensed and flowed between the flipped chip and underneath PCB to relieve the high strain in the chip-to-board interconnects. The current underfill materials must be improved in terms of their adhesion, lowering moisture absorption, and broadening the operating temperature range. Advanced underfill materials under development include pre-dispensed underfills,

reworkable underfills [17], and snap cure underfills. Underfill void and adhesion in the reduced solder bump gap and spacing between the bumps will pose additional difficult material challenges. Advanced underfills must easily dispense in narrowing solder bump gaps and in between higher density bumps. Low modulus underfill materials and molding compound materials may become needed for the chip dielectric and copper interconnects will be robust under thermo-mechanical stress.

Copper metallization and low-k dielectrics have been introduced into electronic packaging for the sake of lower signal delay and thus higher signal integrity required by next generation IC products. By the introduction of copper/low-k materials, the on-die dielectric stiffness will be approaching in stiffness to the materials on the package side such as the molding compound or underfill materials. However, mechanical problem results from higher mismatch in coefficient of temperature expansion (CTE) and poor interfacial strength between the low modulus (low-k) dielectric and metallization traces. Major efforts have been underway to address environmental concerns such as materials and surface finishes for lead-free solder assembly and development and implementation for halogen free materials. Pb-free solders are mandated not only to relieve the environmental concerns but also to reduce radiation-induced soft errors. The most significant emission of alpha particles comes from decay of ^{210}Pb, an unstable isotope of lead in the solder [18]. Tin-based alloys are the most promising lead-free solder candidates, including Sn-3.5Ag, CuSbAgSn and Sn-3.4Ag-4.8Bi etc.

Other material challenges are, due to the rapid reduction in wire bond pitch, the reduction in wire size, capillary, and solutions for wire sweep electrical signal integrity and bond pad designs, which will require significant materials improvement, and

materials process innovation than the currently used processes. Material properties such as dielectric constant, dielectric loss, and thermal conductivity will be very significant to meet higher frequency and higher power demands. Materials research and development will be needed to meet thermal management challenges such as for thermal interface materials, heat spreaders, and external solutions. Knowledge of packaging materials properties are critically needed for modelling and simulation of electrical, thermal and reliability performance for package design release and new package development. Methods for accurate characterization of materials properties and materials interface properties for packaging materials in their use environment will be needed.

2.5 Wafer level packaging technology

Wafer level packaging (WLP) entered the microelectronics industry's lexicon in the late 1990's. WLP is an advanced packaging technology in which the die interconnects bumping, assembly, packaging, test and burn-in all are processed at the wafer level prior to singulation for the system level assembly either as a flip chip or directly as a surface mount device. Compared with conventional packaging technologies where silicon wafers are first singulated into dies and then each die sequentially go through assembly, packaging, and test and burn-in steps, wherein WLP all these steps are done on IC dies when they are still in wafer form and thus it is a true chip-size package. WLP technology offered a number of advantages includes, size miniaturization, lowest cost, elimination of underfill materials and enhancement of electrical performance because of short interconnects [1].

All wafer level packages usually use area-array solder balls as chip-to-next level interconnection whereas WLP technologies differ according to the process steps for area-

array distribution of solder balls. WLP technologies can be classified as Redistribution WLP, Encapsulated WLP and Flex/tape WLP. Many commercial WLPs which have been introduced into the market by different companies are compared with respect to their process features in Table 2.1 [19].

Redistribution WLP generally involves the deposition of thin-film polymer dielectrics, such as BCB or Polyimide, which acts as a secondary passivation layer and metallization Cu or Al to reroute the typical peripheral pads to an area-array configuration. Electroplated or electroless Ni/Au are used as under bump metallurgy (UBM). UBM is critical and necessary to minimize the metallurgical reactions like diffusion of Sn from solders into the redistribution layer and provide highly reliable interconnections. Finally solder balls are formed by solder past screen printing directly on the wafer and reflowed. Examples of redistribution WLPs include IZM-Berlin's S^3-Diepack, FCT's Ultra CSP and Fujitsu's Super CSP etc. The cross section of Fujitsu's Super CSP is shown in Figure 2.3.

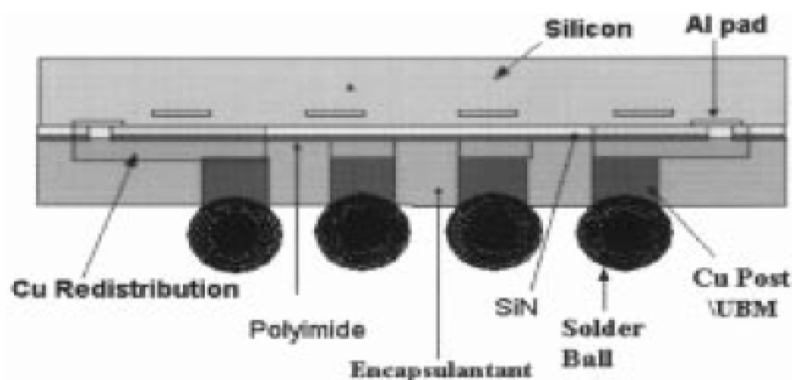


Figure 2.3 Cross sectional view of Fujitsu's Super CSP [19]

Table 2.1 Comparison of Commercial Wafer-Level package technologies

Company	Technology	Feature	UBM	Dielectric	Solder Bump Ball dia/Pitch (mm)
Amkor	wsCSP™	WB connection Cu/PI film	N/A	PI film	0.3-0.5/0.5-0.8
FCT	UltraCSP™	Redistribution	Al/NiV/Cu	BCB	0.35-0.5/0.5-0.8
FormFactor	MOST™	WB “Spring”	N/A	N/A	N/A
Fujitsu	SuperCSP™	Encapsulated 0.1 mm Cu posts	Ti/Ni/Cu	PI	0.35-0.5/0.5-0.8
IZM Berlin	S^3-diepack	Cu redistribution	TiW/Cu/Ni/Au	BCB	0.3
Intarsia	MicroSMT™	Epoxy Si/glass encapsulation	Ti/Cu/Ni/Au	Proprietary	0.3
Oki	-	CMP encapsulated Cu posts	-	PI	-
Shellcase	Shell BGA™	Glass encapsulation	Ni/Au	BCB epoxy	0.3
Tessera	WAVE™	Cu/PI film, low modulus encapsulant		PI film	
Unitive	-	Redistribution	Al/Ti/Cr-Cu	BCB	Plated bumps 0.125-0.25

Encapsulated WLP technology seals the wafer which contains the active devices between the glass wafers. First, the peripheral pads on the die are extended into the dicing streets. The face of the wafer is then glued to a glass wafer and the back side of the wafer is thinned down to 100µm thickness. The backside of the wafer is sealed in glass and

sawn to expose the extended pads. Metallization and UBM layers are deposited and patterned respectively. Finally, solder bumps are attached and reflowed. Examples of Encapsulated WLPs are Shellcase's Shell CSP and Intarsia- Micro SMT. The cross-section of a glass encapsulated Shell CSP WLP is shown in Figure 2.4.

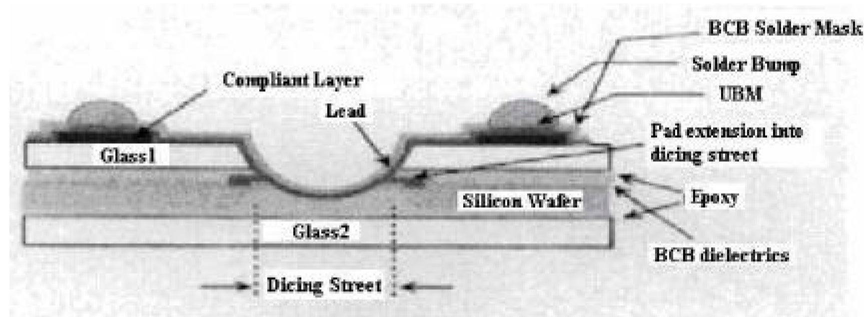


Figure 2.4 Cross sectional view of the Shellcase WL-CSP [19]

Flex tape WLP technologies redistribution structure is different from previous technologies. In this, a redistribution pattern is formed on the Cu/Polyimide flex tape and the patterned tape is attached to the wafer with adhesive. Then the chip is connected by wire bonds from the chip pads to the tape. Liquid encapsulant is used to protect the wire bonds and bond pads. Finally, eutectic solder bumps are attached and reflowed. The examples of Flex tape WLPs include Amkor Anam's wsCSP^{TM}, Tessera's μBGA and FormFactor's MOST^{TM} technology. The cross-section of the wsCSP^{TM} flex tape WLP is shown in Figure 2.5.

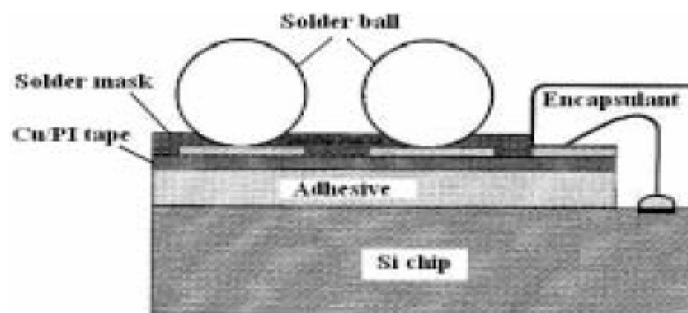


Figure 2.5 Cross sectional view of Amkor ws -CSP package [19]

Inspite of many advantages when compared to conventional packaging, wafer level packaging technology has many challenges must still be solved, including reliability of larger die sizes and developing testing strategies. Other key challenges remaining include wafer-level burn-in and test, in addition to thermal management. Presently, wafer bumping and WLP technologies are relatively using 8inch or smaller wafers. But transistion is being made to 300mm, which challenges all the current technology in this scale-up migration. Major challenges include 300mm sputtering, full-field exposure and across-wafer resistance-drop for electroplating. While transistion from 200mm to 300mm has become a major project for the large IC manufacturers, it is even more challenging from bump foundries.

2.6 Compliant wafer level interconnects

Earlier investigations reported that flipped chips are bonded with PCBs using solder bumps or gold bumps. Solder bumps offers better advantages in terms of self-aligning property over gold during the solder reflow process with better planarity in bump height. However, problems arise when this solder ball interconnects are subjected to thermal loading; failure occurs due to thermal fatigue caused by the large CTE mismatch between the Si die (~2.3ppm/^{0}C) and organic PCB substrate (18ppm/^{0}C), inducing high strain in solder joints. In case of eutectic 63Sn/37Pb solder, which is preferred due to the low melting point of 183^{0}C, creep deformation can occur even at room temperature. Thus, it is evident that solder joints are the most frequently observed failure sites in flip chip devices. The above problems can be overcome with the application of underfill material, which is a pre-dispensed liquid injected into the gap between the flipped chip and PCB substrate and is then cured. Due to this the solder joint

reliability is substantially improved because the thermal deformation is evenly distributed through out the underfill material and solder joints. However, this improved reliability is obtained at the expense of cost and electrical performance degradation of the underfill material [20]. Apart from these drawbacks, cracking or interfacial delamination during thermal cycling can also occur in underfill materials. The other limitations of the solder bumps include the difficulty to reflow and attach solder and to dispense underfill as the pitch size is reduced [21]. Coupled with this, the reliability also drops down. Compliant interconnects with both vertical and horizontal compliance is found to offer better solutions to the above mentioned problems, especially for wafer level packaging, in which the vertical compliance facilitates wafer-level test and interconnection, and the lateral compliance has helped to reduce strain accumulated in solder joints. Few compliant interconnects for wafer-level packaging, which are either available in market or under development in laboratory are discussed as follows.

2.6.1 Tessera's μBGA and WAVE™ packaging technologies

Tessera had developed μBGA technology in the early 1990's for a unique multiple chip module (MCM), with vertical compliance that facilitate reliable contact during electrical testing. Tessera μBGA technology is the first qualified CSP technology for Rambus memory (RDRAM) and flash memory devices [22]. Although some companies including Amkor and Hitachi, got licenses of the μBGA technology with many modifications, the fundamental elements are presented in Figure 2.6. The compliant layer or buffer layer, which is made of low modulus silicon elastomer with thickness of 75-150μm, enables to provide the required compliances. Since the compliant layer is in direct contact with the active side of IC, it must be free of alpha particle. The flexible

links between IC pads and the chip to next level interconnects such as solder balls are provided by using redistribution layer. Another feature is that the notched leads remain attached to the carrier films until the moment of bonding. In Tessera µBGA packages, the structure incorporates compliancy that solves the reliability issues with thermal expansion mismatch between silicon die and PCB. Compliancy provides high on-board reliability that requires no underfill, allowing the device to be easily reworked. Other features of µBGA technology include its face-down structure enabling enhanced electrical and thermal performance, short signal paths resulting in reduced parasitics, and an exposed back surface of the die allowing for efficient heat dissipation. µBGA packages shows good electrical parasitics due to its short signal paths and excellent board level reliability, with a life of over 2876 cycles under thermal cycling between -60 to 150^{0}C [23]. Tessera also demonstrated over 1200 cycles without failure under -40 to 125^{0}C test condition with TV-46 µBGA package [24].

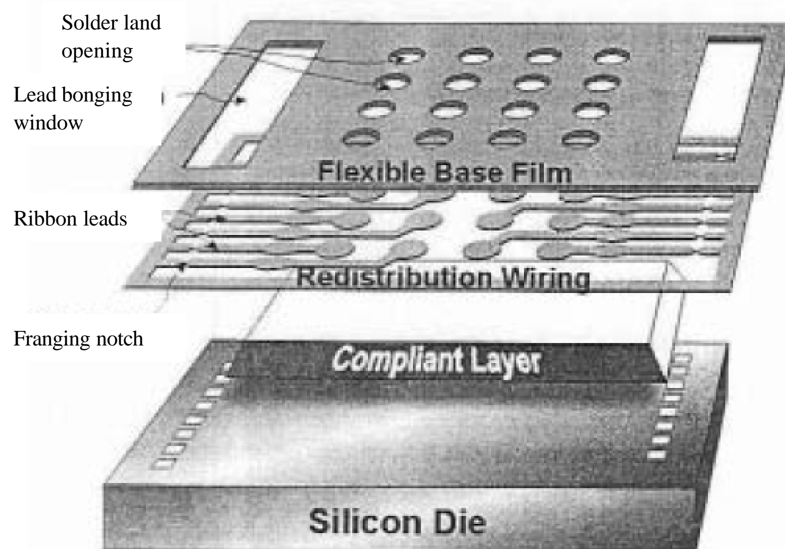


Figure 2.6 Schematic representation of fundamental components of µBGA package by Tessera [25]

Tessera's second generations of compliant packages are μZ™ (Zinger™) and WAVE™ (Wide Area Vertical Expansion) technologies. The WAVE package incorporates a compliant layer formation process that expands vertically along the surface of the die or the entire wafer as shown in Figure 2.7. In WAVE™ technology, more flexible interconnections between the die and package can integrate and the first level bonding of all die pads to substrate can be done simultaneously. The WAVE packages integrate the silicon die with a stress decouple layer made of low modulus encapsulate and a copper intrachip wiring layer with two metal/polyimide substrates. The gap between the die and the substrate is filled and expanded to a height of 100 to 150μm by injection of low modulus encapsulant. WAVE package has a much higher potential than μBGA package for high performance and high reliability package application. The board level reliable tests of WAVE package with a gap distance 150μm demonstrated over 1500 cycles between -40 and 125^{0}C without fail and can be improved by optimization of lead type, lead orientation and gap distance [26-28].

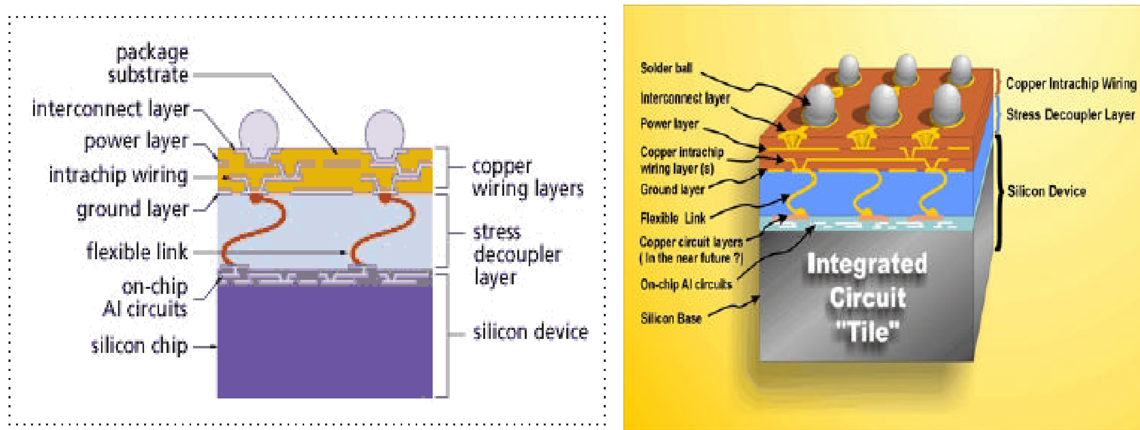


Figure 2.7 Schematic representation of cross section and 3-D view of WAVE™ package [26]

These packaging technologies which include μBGA, WAVE^{TM} and μZ^{TM} are engineered to enable the semiconductor industry to meet the growing demand for small form factor, high performance and cost effective electronics. These technologies are well suited for wireless and memory semiconductors devices including, DRAM (Dynamic Random Access Memory), ASIC (Application Specific Integrated Circuits) and RFIC (Radio Frequency Integrated Circuits) application which requires light weight, small foot print, thin profile and high performance [29].

2.6.2 FormFactor Microspring^{TM} Contacts

In 1998, FormFactor introduced the industry's first integrated wafer level back-end process. This core technology involves the fabrication of Microspring^{TM} contacts on the wafer using wire bonding technology. By using these microspring contacts as chip to next level interconnects, FormFactor introduced the industry's first integrated wafer level CSP (Chip Scale Package) called as Microspring^{TM} Contact on Silicon Technology (MOST^{TM}) package [30-32]. These Microspring contacts as shown in Figure 2.8, de-couples the CTE mismatch between the Si IC chip and PCB substrate and thus improves reliability because of its controlled shape and inherent spring characteristics. Unlike, solder ball based CSP approaches, MOST^{TM} process is unique in that the package leads (Microspring contacts) are also the compliant interface to the test and burn-in equipment and enables whole-wafer burn-in and test at the wafer level. Assembly methods to attach MOST leads to PCBs are conventional solder attach, self socketing die and using conductive epoxies developed by FormFactor and its partners. Advantages of MOST^{TM} includes, low cost due to usage of conventional materials and equipment, elimination of underfill due to Microspring compliant leads structure and thus enables easy repair, and

soft errors rate also reduced due to the distance between the solder and the IC, compared to CSPs that apply solder balls directly on the die surface and this error is even totally removed in case of self-socketing die assembly and die attach using conductive epoxies where solder is not used for connection. Reliability test shows a life of over 1000 cycles under thermal cycling in the range of -55 to 125^{0}C. MOST^{TM} interconnects demonstrates low inductance and low stay capacitance compared to many solder-ball based interconnects. Despite having many advantages, MOST^{TM} process has certain draw backs because they are fabricated one after other using wire bonding, which is an inefficient process which eventually leads to increased cost.

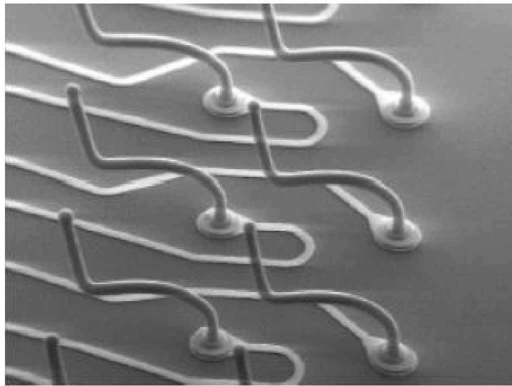


Figure 2.8 SEM micrograph showing microspring contacts or interconnects (MOST^{TM}) array by FormFactor[33]

2.6.3 Sea-of-Leads (SoL) interconnects

Sea of Leads (SoL) is a novel ultra-high-density I/O interconnection technology developed at Georgia Institute of Technology to meet future chip-to-module interconnection needs, which includes giga scale off-chip communication in System on Chip (SoC) packages and electrical performance [34-36]. It is an extension of the concepts and processes that are developed by Patel et al. [37-38]. The important feature of SoL interconnection technology includes high density more than 10^4 leads per cm^2, x-

y-z compliance, high power and high electrical band width, and low electrical parasitics [39]. SoL is fabricated at the wafer level to extend the economic benefits of semiconductor front-end and back-end wafer level batch fabrication to include chip I/O interconnects, packaging, and wafer level testing and burn-in [40]. The SoL processing steps starts with fabrication of die pads on the wafer using photolithography and metal etching followed by applying and patterning of polymer using photolithography to expose the die pads. Compliant metal interconnects extending from the die pad to the solder bump are fabricated by depositing a metal seed layer and electroplating with Cu to final interconnect thickness. The seed layer is then removed and the Cu interconnects are covered with second polymer layer followed by exposure of Cu interconnect end. Again a new seed layer is deposited and the solder bump is electroplated followed by finally removing the seed layer to form the complete SoL interconnects as shown in Figure 2.9. The advantages of SoL interconnects are that it enables high out-of-plane and in-plane compliances, low electrical parasitics and cross-talk by selecting the polymer with low Young's modulus and dielectric constant.

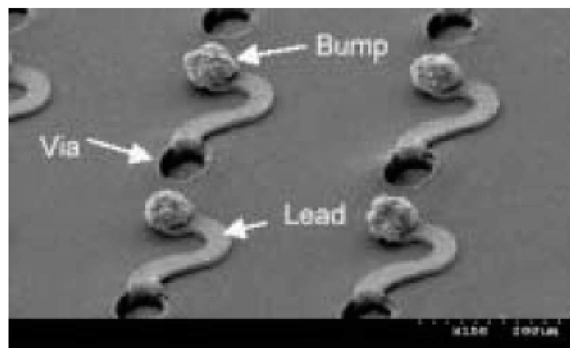


Figure 2.9 SEM micrograph of SoL interconnects [38]

The SoL packaging technology has made continuous improvements to enhance the electrical performance and mechanical compliance. Embedded air-gaps are

introduced in SoL interconnects by processing a polynorbornene (PNB) sacrificial polymer (Unity^{TM} 400) layer, which is thermally decomposed at 400-425^{0}C, to increase the effective out-of-plane (Z-axis) compliance of the package for probe contact and other movements, to mitigate problems in thermal expansion between chip and printed wiring board, and also to reduce the dielectric constant of the interconnect dielectric materials [41]. Furthermore, optical waveguides are proposed to be incorporated within next generation SoL packages, in which the embedded air gaps are used as the upper cladding for optical waveguides. The SoL design is compatible with board-level optical signal distribution via waveguides and also the insertion loss of ground signal propagation into and out of SoL package is less than 1.2dB at 45GHz [42]. Advantages of the next-generation SoL packages includes enhanced predictability of global clock signals, higher heat removal and power supply capabilities that is especially important for hybrid electrical/optical systems packaging.

2.6.4 Cantilevered spring interconnects

To address the compliant ultra fine pitch and high density I/O interconnects requirement for next generation packaging, micro-spring interconnects [43-46], J-Spring interconnects [47], and highly compliant cantilevered nanospring interconnects [48-50] have been introduced by Georgia Institute of Technology in collaboration with Xerox Palo Alto Research Center and Nanonexus Inc. All these technologies are based on stress induced sputtered metal thin film technology in which intrinsic stress in sputtered metal films leads to bending after the film is released from the substrate. The desired uniform bi-axial stress gradient across the film thickness, which determines the radius of curvature of the released compliant interconnect oriented in up or down directions to an

expected extent, can be controlled by the manipulation of the argon pressure in the sputtering chamber. In nanospring technology, 80% Mo/20%Cr (by weight) alloy is chosen to make cantilever-type interconnects, in which the metal is first sputtered onto a substrate at low argon pressure to build compressive stress in thin metal layer. By gradually increasing the argon pressure in sputtering chamber, the film intrinsic stress is changed from compressive to tensile at the end of the sputtering deposition, which is required to bend up after the film is released from substrate. The stress-engineered thin film is patterned into springs and coated with a highly conductive metal layer such as gold to improve its electrical conductivity and the released layer under the thin film is etched away. The released springs curl up due to its intrinsic stress gradient to form spring interconnects as shown in Figure 2.10.

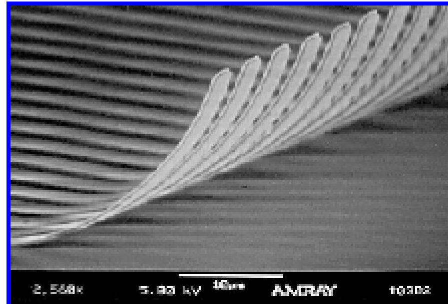


Figure 2.10 SEM micrograph of Ultra-fine pitch nanospring interconnects [50]

The advantage of these compliant spring interconnects is that it meets the requirements of ultra fine-pitch interconnects as small as 6μm. This technology is also found to be highly yielding and inexpensive. Compared to other compliant interconnects, spring interconnects posses very high compliance, i.e. tens of millimeters per Newton in X and Y directions, and over 10,000mm/N in Z direction. Another unique advantage of this technology is that it enables the no-soldering contact between the spring and the board pad. The drawback of this technology is that only some specific metals can be

used to fabricate the nanospring interconnects. Another coiled Microspring contact technology has been studied using thermal expansion coefficient of thin metal films [51].

2.6.5 Helix – type interconnects

Recently another novel compliant off-chip interconnects, namely one-turn Helix and ß-Helix have been developed as an underfill-free interconnects at Georgia Institute of Technology based on conventional photolithography and electroplating technologies [52-55]. The fabrication of Helix-type interconnects starts with the completion of die pads by using etching process on given wafer. A thick photoresist is initially spun, soft baked, UV patterned, post-exposure baked and developed. The bottom copper post is electroplated with seed layer. Again a new seed layer is sputtered and a thinner photoresist is applied, patterned and arc beam electroplated. This sequential process of photolithography and electroplating is repeated to fabricate the five-layer ß-Helix structure. After completion of all these steps, the surrounding photoresist and the seed layers are etched sequentially layer by layer. Thus the free-standing wafer-level 200µm pitch ß-Helix interconnects are fabricated as shown in Figure 2.11. Simulation results demonstrated that, the ß-Helix interconnects had good mechanical compliance in the three orthogonal directions. Besides the good mechanical and thermo-mechanical performance, ß-Helix interconnect also has comparative electrical parasitics with conventional solder bump interconnect. It is also a cost-effective process, especially when the I/O count is high because the fabrication of the above interconnects can be integrated into wafer-level processing as a batch process [55]. Research is still being carried at Georgia Institute of Technology, to develop an alternative geometry design like G-Helix to meet all of the electrical and the mechanical requirements without the need for relaxing for some of the values [56].

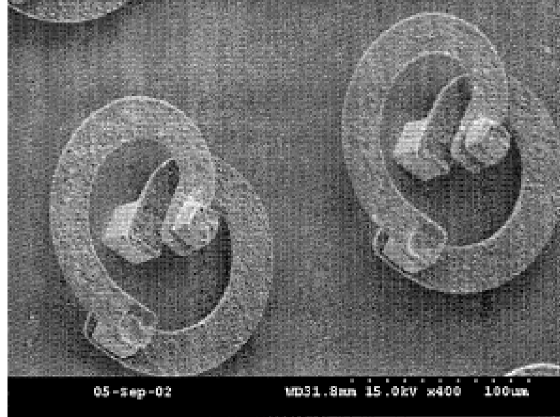


Figure 2.11 SEM micrographs of ß-Helix interconnects [55]

2.7 Challenges in wafer level packages

In the microelectronic packaging industry wire bond interconnections are still in use because of its low cost and easy processing method. Flip chip package interconnections fabrication process generally involved more number of process steps and costly photoresist and polymer materials hence found to be costly than wire bond interconnections. Apart from this, there are number of challenges faced by the existing interconnections technologies which are summarized in detail as follows:

- More number of processing steps are involved in interconnects fabrication thereby increasing the time of fabrication which resulted in reduced mass production.
- Usage of expensive proprietary polymers in processing techniques resulted in high cost. Hence the cost per I/O pin is increased.
- Most of the technologies fabricated interconnects at pitch size of 200-500µm. which limits the interconnection density and the packaging technologies for next generation microelectronics.

- Due to difficult shapes involved, special assembly equipments are required. Apart from this assembly yield and quality are also biggest challenges faced.
- Process recipes should be compatible for mass production fabrication.
- Current technologies are using the polymers as encapsulates and underfill materials to obtain compliancy effect but these materials induces moisture issues in the package thereby degradation of their thermo-mechanical reliability.

2.8 Scope of the project

The present packaging technologies are using solder balls as the interconnections between the chip and substrate, at the pitch size of 300-400µm. But the investigations found that these solder balls are the main failure sites in the package during the thermo-mechanical fatigue caused due to the CTE mismatch between the chip and organic substrate. Hence underfill material is dispensed around the solder bumps in between chip and substrate to improve the fatigue life. According to ITRS-2003, next generation packaging technologies will require interconnections technologies at lower pitch size, where solder balls cannot meet the reliability requirements because of its small size and short stand-off height at that fine pitch and underfill dispensing would also found to be a bottleneck issue at that fine pitch. Hence packaging industry needs cost effective underfill-free interconnections technologies to meet the reliability requirements at fine pitch. The present study was done on the fabrication of underfill-free Bed of Nails (BoN) interconnects. The fabrication of the BoN interconnects was based on photolithography and electroplating techniques. This fabrication was carried out at wafer level hence it enables mass manufacturing and realizes a cost effective package. The main tasks of this project includes optimization of thick photoresist process for mold fabrication, copper

and solder electroplating, solder reflow process and assembly process. Thermo-mechanical reliability of the above interconnects was done to test the feasibility and failure analysis to identify the possible failure modes.

CHAPTER 3

EXPERIMENTAL DETAILS

3.1 Materials

The future packaging demands on high I/O density and high mechanical and electrical reliability necessitate copper as a prominent material for interconnects. As an electrical off-chip connector, copper has lower electrical resistance that not only leads to improved power distribution and device performance but also helps to reduce cross-talk by providing a better control over the tight interconnect pitch. Furthermore, with good electromigration stability, copper can conduct high current density. From a cost point of view, copper is cheap and can be easily electroplated. Therefore, in the current study, copper was electroplated during the fabrication of the BoN interconnect. To fabricate the electroplated copper BoN interconnects the following materials were used in the process:

1. The p-type silicon (100) wafers of 200mm diameter with thin electrical insulating film of 1000A° SiO_2 were used for the fabrication of test chip demonstrator.
2. Sputtered Ti/NiV/Au layers were used as pads and UBMs with daisy chains. It also was used as the seed layer for electrical contact during the electroplating of copper interconnects.
3. AD AP3000 primer solution for promoting adhesion of the BCB with the wafer.
4. BCB dielectric material was used to passivate the daisy chains and to define the pads for copper interconnects.
5. Wet etchant chemicals for selective etching of Ti, NiV, Au and Cu layers.

6. PFI 26A (+ve), PLA 900 (+ve), AZ P4620 (+ve), SU-8 (-ve) and JSR (-ve) photoresist materials were used to get the patterned thick layer for selective plating of copper interconnects.
7. Electroplated eutectic Tin-Lead was used as a solder material.
8. Developer and stripper solutions for the above resist materials.
9. Piranha solution (H_2SO_4 + H_2O_2) for wafer cleaning. Ratio of H_2SO_4 to H_2O_2 was 5 : 1.
10. Acetone and PI for cleaning of wafers to reclaim the photoresist coated wafers.

3.2 Equipments

3.2.1 Sputtering machine

The seed layers for electroplating were deposited using Balzers LLS 502, load lock sputtering system. Ti layer was coated on the wafer prior to deposition of Cu or Au seed layer films to promote the adhesion. The Cu or Au target was used as the cathode with 99.9999 % purity. The sputtering conditions used were 4 x 10^{-6} base pressure; 3 x 10^{-1} working pressure; 4KW, 6KW and 1KW sputter power for Ti, Cu and Au respectively. The sputtering chamber was baked for about 20hrs by wiring with a couple of heaters to remove the moisture from the chamber wall very efficiently. High Purity Argon gas was used to maintain inert atmosphere. Seed layers were deposited by DC magnetron sputtering on the Si (100) substrate. The substrate was mainatined at a distance of 70mm from the target. From thickness measurements of all the films, the deposition rate of the film was estimated to be 2.15nm/s.

3.2.2 Spin coater track

SVG 90 series spin coater track was used to coat, soft bake, post exposure bake and to develop the photoresist material. This track accepted only 8inch diameter wafers and contained 18 stations, which included “2” wafer sender/receivers, “2” vapor primers at 150^{0} C, coating, 4 hot plates, 6 chill plates, and 2 developing stations. In this spin coater, wafer flow could be defined according to the process flow, in such a way that wafer started from wafer sender to vapor primer at 150^{0}C and then to chill plate to cool the wafer to room temperature. After cooling, the wafer is moved to the coating station where the resist spun onto the wafer according to the coating cycle which was already programmed. Finally the wafer was moved to the hot plate where a defined temperature was maintained for pre-defined time to soft bake the photoresist. All this process could be performed automatically for 25 wafers lot continuously by selecting automatic mode. Even the single step process such as coating or baking could be performed by selecting the manual mode. The thickness of the photoresist can be controlled by changing the spin speed and spin time.

3.2.3 Mask aligner

EVG 640 mask aligner was used to expose the photo sensitive layers through soda lime or chrome masks and to align the subsequent masks in the lithography processes. This was a UV light (365-405nm) exposure aligner and was compatible with 5, 7 and 9 inch masks. The capabilities of the above aligner were as follows.

- Single and double side alignment
- Proximity, hard and soft contact modes

- ± 1µm alignment accuracy
- Alignment for embossing and wafer bonding

3.2.4 Copper electroplating tool

Copper electroplating was carried out using RENA 8” wafer electroplating tool, which was fountain type (Cup type) in which Sperolyte $CuSO_4$ based solution (Atotech Pte. Ltd) was used as electrolyte solution. The principle of this plating tool was that the wafer was loaded in chuck as cathode placed upside down at the top of the plating tool as shown in Figure 3.1 and the soluble copper anode was positioned at the bottom in cup shaped electrolyte chamber. The electrolyte was fountained from the bottom to the wafer surface through the diffusers. The concentration uniformity of the electrolyte solution also would be maintained due to this fountain type electrolyte flow and thereby improved the plating efficiency. The plating process was carried out in two steps. In first step, the chuck loaded with the wafer was rotated at high speed with high flow rate of electrolyte to improve the wettability of the wafer whereas in the second step , the flow rate was maintained constant with the rotating speed of the chuck being reduced to obtain uniform copper plating in the entire wafer. Hence the plating thickness could be controlled by optimizing the current density and platting time and uniformity could be controlled by optimizing the the flow rate of electrolyte. The plating process was carried out at room temperature.

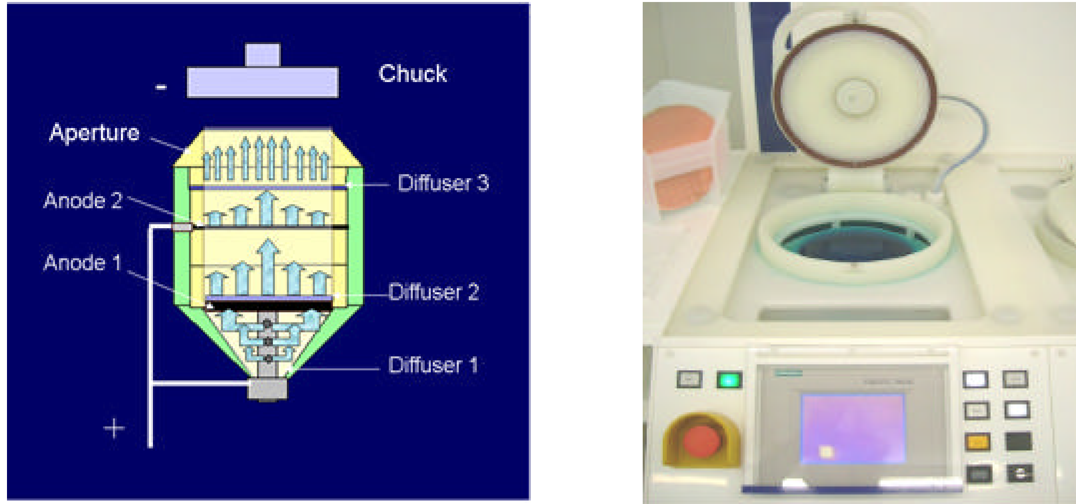


Figure 3.1 (a) Schematic diagram of principle of electroplating (b) photograph of 8 inch wafer fountain type for Cu plating tool

3.2.5 Solder plating tool

The eutectic tin-lead solder was plated at the tip of the copper interconnects using RENA 8” wafer electroplating tool, which was a rack type in which sperolyte solution (Atotech Pte. Ltd) was used as electrolyte solution and tin-lead pellets were used as anode. Here the principle of plating was that the wafer was loaded in the chuck and the chuck was positioned parallel to the anode as shown in the Figure 3.2. Solder thickness, uniformity and solder shape at the tip of the BoN interconnects were controlled by optimizing the current density, flow rate of electrolyte and plating time.

Figure 3.2 (a) and (b) Photographs of rack type solder plating tool for 8inch wafer

3.2.6 Scanning electron microscope (SEM)

JEOL 5600LV scanning electron microscope (SEM) was used to view the cross-section of the vias in the photoresist thick layers, electroplated copper interconnects and as well as to analyze the failure mechanisms of the packaged interconnects after thermal cycle testing. The samples were mounted on the sample stud by means of double–sided adhesive tapes. The SEM measurement was performed at an accelerating voltage of 15kV.

3.2.7 Convection heating Oven

BCB soft curing and hard curing at 210^0C and 250^0C for 40min and 60min respectively were carried out under N_2 atmosphere in a convection heating oven. In this oven, required temperature and holding time along with heating and cooling rate could be programmed.

3.2.8 Wet bench

This contains temperature controlled etch tanks, DI water rinse tanks, solvent tanks and ultrasonic cleaning tank. It was used for the wafer cleaning, photoresist stripping in the resist stripper solvent at 65^0C and DI water rinsing.

3.2.9 Spin rinse dryer

It was used to dry the wafer after cleaning and DI water rinse. Wafers were spun dry at 1300rpm for 5min. This drying process was carried out with N_2 gas purging.

3.2.10 Plasma thermo etching system or Reactive Ion Etching system (RIE)

Thin residues of BCB and photoresists after litho process was removed using O_2 plus CF_4 gases and O_2 plasma descum process by RIE etching system. BCB descum was carried out using gas mixture of 16sccm O_2 and 4sccm CF_4 at 300watts power for 1min. Photoresist descum was carried out using 20sccm O_2 plasma gas at 300watts power for 3-5min. This O_2 plasma process was also used to activate the photoresist surface for electroplating of copper.

3.2.11 Solder reflow oven

The eutectic Tin-Lead solder at the tip of the BoN interconnects was reflowed after stripping of the resist, in N_2 atmosphere using 6-zone reflow oven. Solder reflowed at above the liquidus temperature of eutectic tin-lead solder (235^0C) for about 80seconds were used to form the solder bump at the tip of BoN interconnects.

3.2.12 Dicing machine

After fabrication of BoN interconnects on the silicon wafer, the wafer was diced into individual dies using dicing machine. Diamond tip wheel was used for cutting.

3.2.13 Flip-Chip bonder

The diced individual chip was assembled on the Printed Circuit Board (PCB) to perform the thermal cycle test using Karl-Suss Flip-Chip bonder (FC-150). It was a fully automated device bonding system, used to level, align and package components down to 200µm with ± 0.1µm accuracy. In this bonder, flux could be applied on the solder automatically using rotating ball in the liquid flux bath and solder could be reflowed (in-situ reflow) in the bonder during the assembly by heating the chip holder chuck and PCB holder. Force could be applied in the Z-direction on the chip during the assembly to control the solder shape. Different types of chuck sizes can be used to accommodate all device sizes. The FC150 could be equipped with tooling enabling all known bonding processes (i.e. Thermo compression, Adhesives, Reflow...) to perform wafer-to-wafer bonding, with wafer sizes up to 100mm diameter at + 1µm post-bonding accuracy.

Figure 3.3 Photograph of Karl-Suss flip chip bonder

3.2.14 X-ray system

X-ray screening was performed on the assembled packages to inspect the voids in the bonded solder and to know whether any two daisy chains were short circuited or not using Dage XD 6500 X-ray system. The minimum feature size recognition in this system was 2μm. X-ray tube voltage of 30-160KV was used.

Figure 3.4 Photograph of Dage X-ray system

3.2.15 Thermal cycling furnace

The board level reliability of the assembled packages was performed in Weiss temperature system. The thermal cycling test of the assembled packages was performed under the temperature cycling at the range -40^{0}C to 100^{0}C. The dual time per one cycle was 1hour. The resistance of the daisy chains was measured for every 100 cycles to assess the failure of the assembled package.

3.2.16 Bump shear tester

The bump shear test was one of the most commonly used methods for evaluating bonding strength of bumps. It can give a quick assessment of the strength of the bond between bump and substrate. Bump shear tests were carried out on the Model BT24 Dage

Ball Shear Tester. The schematic diagram of the bump shear tester is shown in Figure 3.5 [57]. Shear height and shear speed were the main parameters in the shear test. Generally shear height have to be maintained at 10-20 percentage of the total bump height.

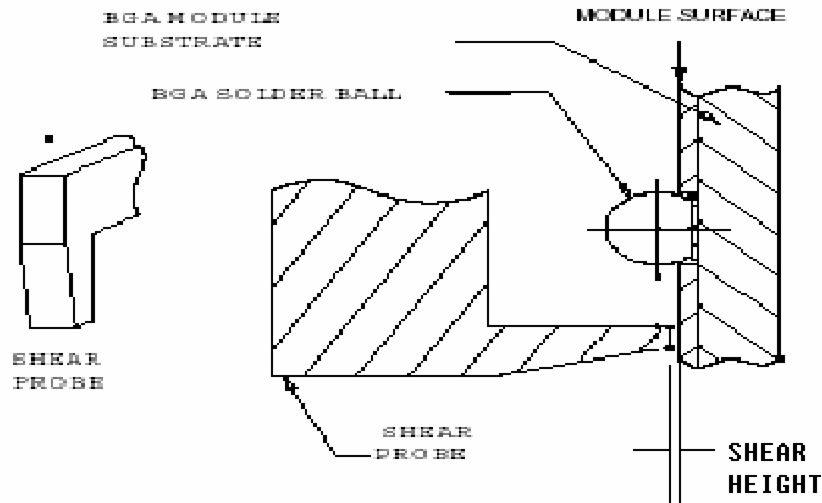


Figure 3.5 Schematic diagram of bump shear test [57]

3.2.17 Die shear tester

Die shear test was used for evaluating the bonding strength of assembled test dies. It can give a quick assessment of the strength of the bond between the test die and substrate. Die tests were carried out on the Dage Series 4000 bond tester. Schematic diagram of die shear tester was also similar to the above ball shear tester but the shear probe used in the die shear test was flat surfaced whereas pointed surface was used in ball shear tester. The width of the shear probe used in die shear test was equal to the die width. Shear height and shear speed were the main parameters in the shear test. Generally shear height have to be maintained at the total bump height.

CHAPTER 4

BED OF NAILS (BoN) INTERCONNECTS CONCEPTUAL DESIGN AND FABRICATION PROCESS DEVELOPMENT

4.1 Conceptual Design

As mentioned earlier, with the continued reduction in IC feature size, microelectronic packaging continues demanding for smaller size, better performance, lower cost and higher reliability. Currently, underfill dispensed around the solder bumps was found to be the solution for the CTE mismatch and enhanced thermo-mechanical reliability, but in future technologies high density I /Os will be required in smaller chip size resulting in fine pitch sizes. Dispensing of underfill at this fine pitch interconnection would be difficult. Hence accommodation of CTE mismatch without underfill would be one of the key challenges from thermo-mechanical point of view. A notable innovation that could resolve these challenges was the use of compliant off-chip interconnects. In this work, a new interconnect named, Bed of Nails, an underfill free off-chip interconnect, has been designed, fabricated and analyzed. Conceptual design is the first but the most important step throughout the development of a new technology.

4.2 Design Concerns

4.2.1 Functional concerns

The main function of off-chip interconnects was to provide reliable electrical and mechanical connection between the Integrated Circuits (IC) and the next-level substrate. In which, providing the electrical connection was an important objective which was made feasible only through mechanical linking. Hence it was required that any packaging

concept should yield an interconnect design capable of meeting the thermo-mechanical compliancy between IC chip and substrate [58]. Electronic packages generally undergo thermal expansion and contractions in their real use conditions. Hence, tensile and compressive stresses were induced due to relative movements because of the CTE mismatch in various parts. Mechanical and functional failures were also resulted due to the plastic deformation which was caused because of the strains induced due to CTE mismatch, exceeding the elastic limits of interconnect material. Therefore, underfill material was frequently dispensed around the solder bump to reduce the shear strain in the solder bump. In case of complaint interconnects, due to its in-plane compliancy it easily accommodates the differential displacements induced due to the CTE mismatch between the chip and substrates. Apart from this, it also reduces the force on the bond pads thereby preventing crack or delamination in low-k dielectrics in chip.

For future microelectronic packaging systems, maintaining signal integrity becomes one of the major bottle neck issues for enabling reliable systems. This is due to the increase in speed; reduction in voltage, increase in power and the integration of mixed signal functions which in turn imposes number of challenges for electrical design in off-chip interconnects. Due to the fast transition of digital signals, the analog behavior of these signals becomes very important. Issues such as cross talk, reflection, switch noise; eye patterns and delay therefore have to be addressed for the design of systems. High power supply and high signal speed in fine pitch off-chip interconnections results in electromigration and thermal effects which highly affects the interconnect reliability. Due to this increased power dissipation and reduced chip size, the temperature of interconnects will be increased resulting in the degradation of device performance and

decreased interconnect reliability due to electromigration induced failure mechanisms. Hence electrical design and the interconnect temperature have to be maintained at optimum level to have better device performance.

4.2.2 Material concerns

Presently, solder bumps were widely used as off-chip interconnects in the microelectronics packaging. As the pitch size reduces, and signal speed and power supply increase, the solder bumps will face electromigration and cross-talk problems. Apart from this, solder bumps thermo-mechanical reliability will degrade at such a fine pitch sizes due to their poor strength. Hence it was very essential to choose an alternative metal to accommodate next generation packaging.

Due to the inherent low resistivity and good electro-migration stability, copper was chosen as a potential candidate to meet the above challenges [59]. This low electrical resistivity of the copper not only leads to improve power distribution and device performance but also reduce the cross-talk by providing better control over the high I/O density. Copper can also carry high current density due to its good electromigration stability. As a mechanical chip to substrate connector, copper has high strength than solder material while with moderate elastic modulus. In addition, from the fabrication point of view copper plating was considered as the most popular and cost-effective technology compared to other metal-deposition processes.

The biggest challenge in the fabrication of interconnect was to meet the high density at fine pitch by reducing the size of interconnect. To attain this requirement, lithography seems to be the best option. Compatibility was also considered as other important criteria because interconnects were fabricated on top of the foundry-processed

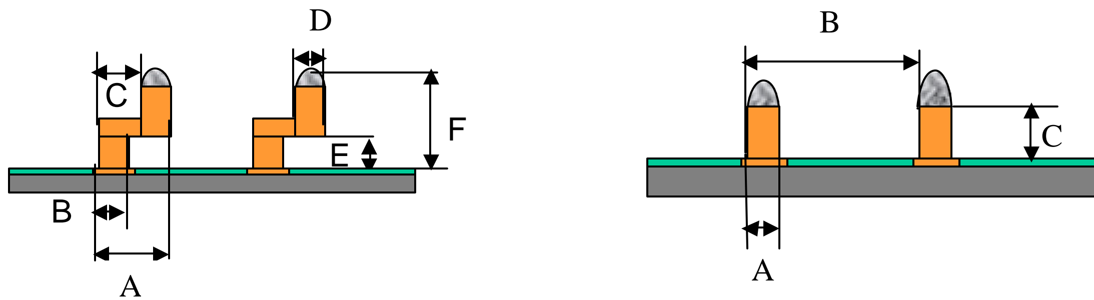
silicon wafer with integrated circuit devices. Hence the interconnect fabrication process and the material used in fabrication should be compatible with standard IC fabrication technology.

Considering all the above requirements, BoN interconnects have been designed and developed, the fabrication of which is compatible with conventional IC fabrication process.

4.3 Design of BoN interconnect

Driving factors behind the design and development of Bed of nails (BoN) off-chip interconnects was to improve the mechanical compliance, electrical performance, manufacturability, cost-effective fabrication process, fine pitch interconnection needs, wafer level and easy processing similar to conventional semiconductor processing steps. Two different types of Bed of Nails interconnections, namely, three layers BoN interconnects and single layer or single copper column BoN interconnects as shown in Figure 4.1 (a) and 4.1 (b), were designed to obtain mechanically and electrically reliable and high performance interconnections to meet the next generation packaging needs. The BoN interconnects designed in three layers provides better compliancy because of its flexible structure and hence better reliability could be obtained. Even the single copper column BoN interconnects could also result in better reliability because of the high aspect ratio obtained due to increased stand-off height of the copper column. However, BoN interconnects with single layer have low electrical parasitics due to its shorter interconnections between chip and substrate compared to three layer BoN interconnects. The structures dimensional details of the above BoN interconnects were shown in Table 4.1. In this project, the study was focused mainly on the fabrication and reliability of

single copper column BoN interconnects along with the demonstration of design and fabrication process of three-layer BoN interconnects. The reason for focusing mainly on the single layer interconnects is because of the few limitations in the fabrication of three layer BoN interconnects, which involves process difficulties and poor yielding due to more number of process steps and cost. The details of which will be discussed in the section 4.5.



(a) Three layer Bed of Nails interconnect (b) Single layer Bed of Nails interconnect

Figure 4.1 Geometric representation of Bed of Nails interconnects

Table 4.1 Dimensions of Bed of Nails interconnect structures

(a) Three layer Bed of Nails interconnect

	Dimensions in Microns
A	50,60,70
B	20,30
C	30
D	20,30
E	20,50
F	50,80

(b) Single layer Bed of Nails interconnect

	Dimensions in Microns
A	50
B	100
C	50,100

4.4 Fabrication process development

Thick metallic microstructures were of interest for many applications in the micro-electronic industry. Hence, fabrication of thick metallic microstructures with high aspect ratio was required. Therefore, in past years many process developments have been

made to fabricate taller and larger electroplated 3-D structures. LIGA process was the first and most widely used technique to fabricate very tall (100µm-1mm) structures without sacrificing the accuracy of the lateral dimensions [60]. The LIGA process starts with the deposition of thick layer of X-ray sensitive photoresist, usually polymethylmethacrylate (PMMA) based resist, on a metal coated substrate followed by the exposure through an X-ray mask, using a high energy X-ray radiation source, which was produced by synchrotron. The use of synchrotron based lithography allows exposure of vertical sidewalls through the thickness of photoresist. If the negative photoresist is used, the resist in the unexposed region is then developed, revealing regions of underlying metal seed layer. The patterned thick photoresist now acts as a mold for metallic structure material deposition using electroplating. Once the deposition has been completed, the photoresist was removed, yielding the released electroplated metal structure. This LIGA technology has great capabilities but was very expensive as it requires costly X-rays, mask fabrication process and synchrotron exposure facilities which may not be available in many laboratories. The lack of access to a synchrotron source have motivated the development of cheaper and easier process, similar to LIGA process based on UV photolithography and it became more and more popular to fabricate free standing high aspect ratio metallic structures in recent years. In this process, near UV light sensible photo resist materials were exposed through soda lime or chrome mask using conventional UV-light source. This process was called as UV-LIGA or LIGA like process. Different UV or near UV sensitive positive and negative thick photoresists were commercially available. The details of which were discussed in the later session.

BoN off-chip interconnects was fabricated based on LIGA like process. In this process, both positive and negative photoresist materials were tried to obtain required structure with good side wall verticality and easy processibility which was compatible to mass production.

4.4.1 BoN Wafer Level Interconnects Fabrication Process

The fabrication process of BoN interconnects was based on photolithography and electroplating process which was compatible to the conventional integrated circuit (IC) fabrication and was integrated into wafer-level processing as batch processes. Therefore, cost can be reduced especially when I/O count is high.

4.4.1(a) Single layer BoN Wafer Level Interconnects Fabrication Process Flow

The fabrication process of the wafer-level single layer BoN interconnects was schematically illustrated step-by-step in Figure 4.2. Additional masks were not needed to fabricate the single column BoN interconnects as UBM mask can be used to pattern the photoresist for copper column deposition. Thus this BoN interconnect fabrication was cost effective especially when I/O count was high as this fabrication was carried out at wafer-level. On a given clean wafer, Ti/Ni/Au metal layer was first deposited by sputtering. The photoresist was then applied and patterned to form metal pads with daisy chains by etching Ti/Ni/Au layers one by one followed by resist removal. Secondly, BCB dielectric polyimide was spun to passivate the daisy chains and pattern the dielectric layer using UV lithography to open the pads. Next Ti/Cu or Ti/Au seed layer was sputtered in which the bottom Ti layer was applied to improve the adhesion between dielectric and Cu or Au. Then a thick photoresist was spun, soft baked, UV patterned, and developed, followed by electroplating of copper post. Then the solder was electroplated at the tip of

the copper post for bump formation. Thick photoresist was then removed and Ti/Cu or Ti/Au seed layer was etched away to complete the interconnect structure. Finally, solder was reflowed.

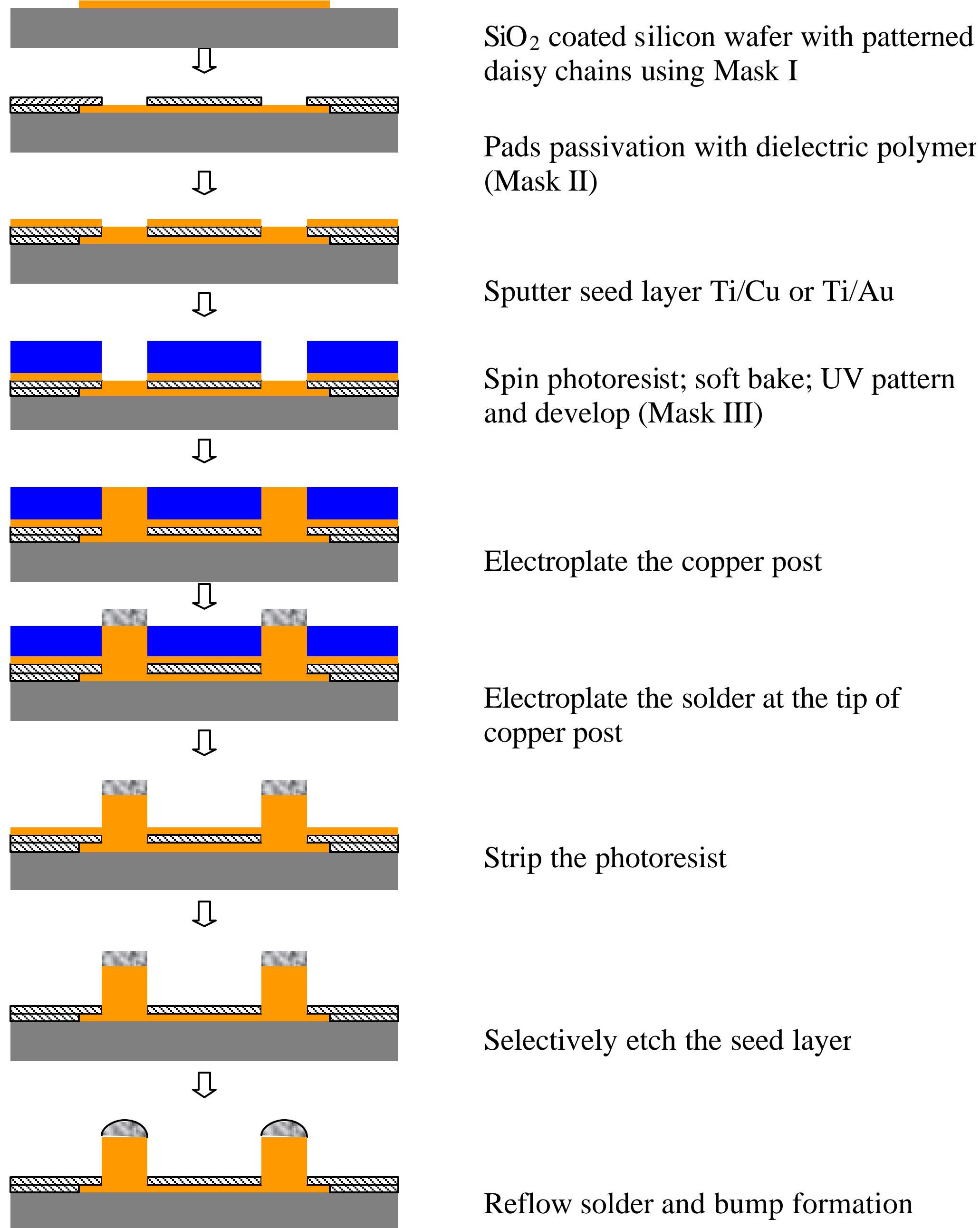


Figure 4.2 Fabrication process flow chart of single layer BoN wafer level interconnections

4.4.1 (b) Three layer BoN Wafer Level Interconnects Fabrication Process Flow

Three layer wafer-level BoN interconnects fabrication process was schematically illustrated step-by-step in Figure 4.3. This process requires two extra masks to complete the free standing three layers BoN interconnects fabrication compared to conventional solder bumps fabrication. On a given clean wafer, Ti/Ni/Au metal layer was first deposited by sputtering. The photoresist was then applied and patterned to form metal pads with daisy chains by etching Ti/Ni/Au layer one by one followed by resist removal. Secondly, BCB dielectric polyimide was spun to passivate the daisy chains and pattern the dielectric layer using UV lithography to open the pads. Next Ti/Cu or Ti/Au seed layer was sputtered in which the bottom Ti layer was applied to improve the adhesion between dielectric and Cu or Au. Then a thick photoresist was spun, soft baked, UV patterned, and developed, followed by electroplating the bottom copper post. After electroplating, a second Ti/Cu or Ti/Au seed layer was sputtered and a thick photoresist was again spun. The sequential process of photolithography and electroplating was repeated to create the three layer BoN structure. After completion of BoN structure, solder was then electroplated at the tip of the BoN interconnects for bump formation. Once the steps were completed, the surrounding photoresist and the seed layers were etched sequentially layer by layer. Finally solder was reflowed to form the bump. Thus the free standing wafer-level BoN interconnects was fabricated.

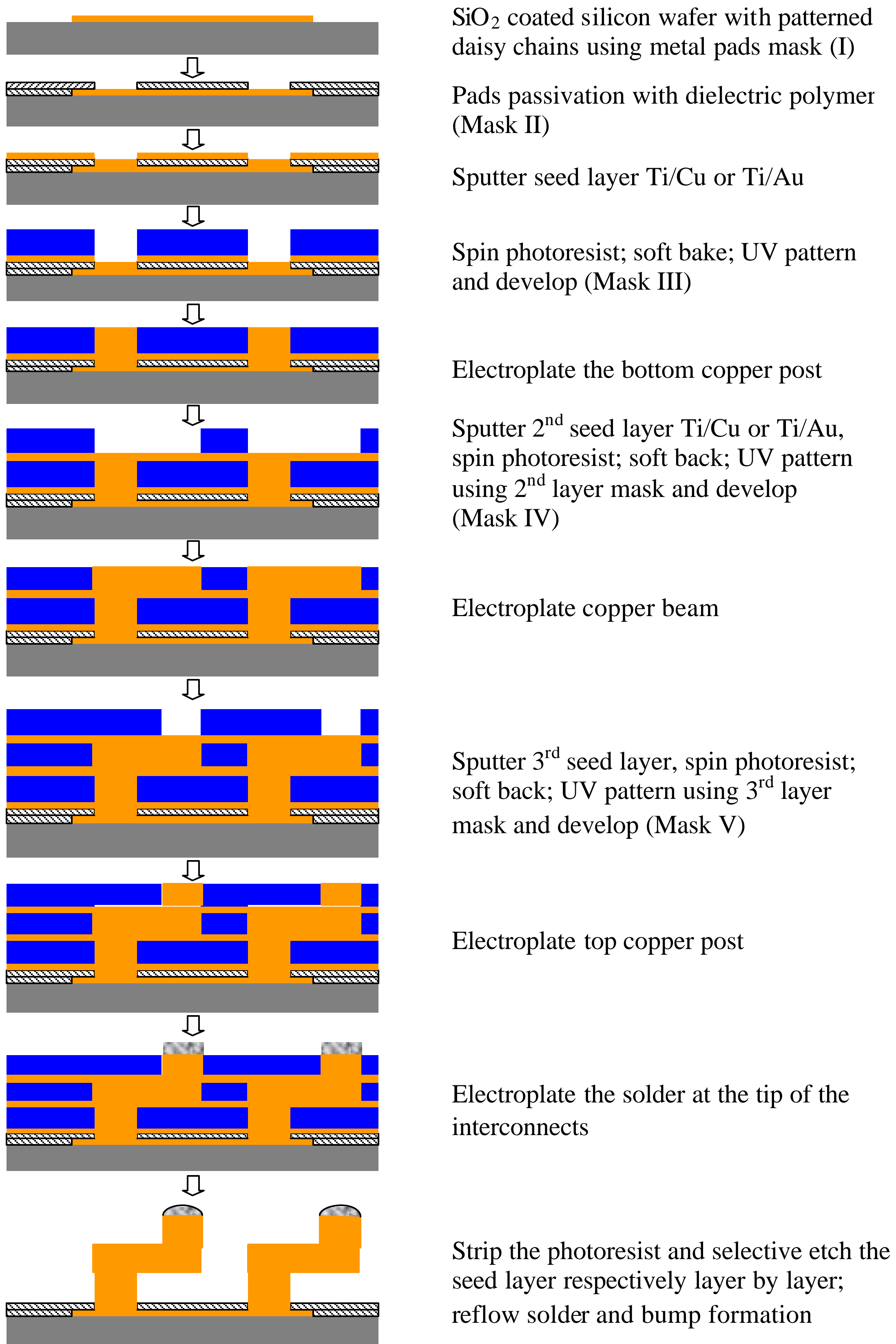


Figure 4.3 Fabrication process flow chart three-layer BoN wafer level interconnections

4.5 Selection criteria for interconnect design

The important criteria considered for the interconnect design selection for the fabrication of BoN interconnect are listed as follows:

1. Cost
2. Mechanical properties
3. Electrical properties
4. Processibility
5. Yield
6. Environmental Susceptibility
7. Reproducibility

4.5.1 Cost

The first and foremost criteria essential for the fabrication of BoN interconnects is the cost of the materials used. The BoN interconnect fabrication cost mainly depends on the photoresist material and electroplating process involved. In single layer BoN interconnects, the fabrication cost involved is comparatively less than 3-layer interconnects. This is because, in single layer, the photoresist is coated once, whereas in three layer process the coating has to be done for three times. In photoresist spin coating process, 80% of the resist material will be wasted during spinning. Hence the wastage of the photoresist material in 3-layer BoN interconnect fabrication is found to be much higher than single layer BoN interconnects. Similarly in the electroplating process, copper have to be plated three times to complete the fabrication of 3-layer BoN interconnects thus resulting in high plating cost.

4.5.2 Mechanical properties

The most important mechanical requirement of the interconnect structure is the compliancy as it improves the thermo-mechanical reliability/fatigue life of interconnects and packages. Strength is also considered as an important parameter, because it is necessary to accommodate the strain induced due to the CTE mismatch between the chip and substrate. Earlier studies estimated the fatigue life of single column and three layer BoN interconnects using simulation, which revealed that the fatigue life of 3-layer BoN interconnects was superior due to its better compliancy offered by its flexible structure. Table 4.2 shows the simulated fatigue life data of the single and three layered interconnects of 20µm diameter and 100µm height [61, 62].

Table 4.2 Simulated fatigue life data of the single and three layers BoN interconnects

Parameters	Single column	Three-layer
Chip thickness(µm)	640	640
Board CTE(ppm/°C)	10	10
Fatigue life (f_n)	20	348

4.5.3 Electrical properties

The main parameters studied for electrical properties are inductance, resistance and capacitance. As reported earlier, the simulated results showed that single layer BoN interconnects exhibit better electrical properties than 3-layer interconnects due to their short interconnection between chip and substrate. Table 4.3 shows the simulated electrical properties of three layered interconnect [62].

Table 4.3 Simulated electrical properties of three layers BoN interconnect

Properties	Three-layer
Inductance (pH)	46
Resistance (mO)	28
Capacitance (fF)	18

4.5.4 Processibility

Single layer BoN interconnection fabrication process is found to be easy compared to three layer BoN interconnects. This is because in the single layer BoN fabrication process only one extra mask process is involved whereas three layer BoN interconnect fabrication involves three masks processes thereby increasing the number of process steps involved with more processing time. Apart from this, misalignment of the successive mask processes, seed layer sputtering on photoresist material and resist stripping are also found to be the other difficult steps involved in 3-layer BoN interconnects.

4.5.5 Yield

The most essential criteria for the microelectronic packaging is the yield of the interconnect fabrication process. In single layer BoN interconnect process, yield is found to be higher than 3-layer interconnects because of the less mask process steps, which reduced the misalignment and other process problems. In addition to high yield, the fabrication of single layer BoN interconnects is found to be compatible for mass production because of its less processing steps and thus less processing time.

4.5.6 Environmental susceptibility

Currently high lead and eutectic tin-lead solder balls are used as interconnects in most of the packages. The potential health hazards involved in using the lead material results in disorders of the nervous and reproductive systems and also can affect the neurological and physical development. Hence necessary steps have been taken to eliminate or reduce the use of lead in packages. In present study, BoN interconnect fabrication process involves usage of copper and less volume of eutectic tin-lead solder thereby reducing the lead content in package thus making BoN interconnects environmental friendly.

4.5.7 Reworkability

Currently, under-fill materials are used in the packages to improve reliability. Usage of this under-fill material makes reproducibility to be difficult. In case of BoN interconnects, no under-fill material is used thus making this process highly reproducible. Table 4.4 shows the overall comparisons between single layer and three layers BoN interconnects.

Table 4.4 Overall comparisons between Single layer and three layers BoN interconnects

Properties/process	Single layer process	Three-layer process
Cost	Low	Comparatively high
Mechanical properties	Moderate	Good
Electrical properties	Good	Moderate
Yield	Better	Comparatively poor
Processibility	Less process steps	More process steps

Assessing the merits and demerits of three-layer and single layer BoN structure, which have been discussed above, the nano wafer level packaging project team decided to pursue the single layer structure only, in its review meeting. A detailed study on the single layer BoN interconnects in terms of different column height and diameters was carried out to asses its implementation as a 100µm pitch wafer level interconnects. More details on the fabrication, assembly and reliability will be discussed in the following Chapters.

CHAPTER 5

TEST CHIP DEMONSTRATOR DESIGN AND FABRICATION

5.1 BoN test chip and mask layout Design

To fabricate the BoN test chips on wafer level, the test chip layout design was required to design the complete mask layout from which the fabrication of the photo mask was facilitated. Cadence software was used to design the mask. The factors to be considered while designing the mask included the process flow, type of materials, alignment of different layers, dark field or bright field of the mask type, and functions of every pattern etc. But the above design consideration had certain drawbacks. Hence in order to optimize this design, simulation or some trial and error methods were ought to be performed.

To fabricate the single column BoN interconnects at 100μm pitch, 3 soda lime masks namely metal pads patterning mask, metal pads passivation or BCB opening mask and copper column mask to pattern the photoresist for copper interconnect plating were designed with 10mmX10mm size chips with 3332 I/Os in 17 depopulated rows as shown in Figure 5.1 and 4356 I/Os in a fully populated manner. In addition, 20mmX20mm size chips were also designed with 2256 I/Os in 3-depopulated rows as shown in Figure 5.2 and 36481 I/Os in a fully populated manner as evident in Figure 5.3. Three different patterns were present on three different masks to complete the test chips fabrication with single column BoN interconnects. In each test chip die alignment marks were designed on the metal pads patterning mask at the lower left corner and upper right corner. These alignment marks can be used to align the test die with the next level substrate during

assembly. These test chip designs were used for the complete designing of masks as evident in Figure 5. 4. Two alignment marks were designed on each mask at the distance of 62-68mm from the center of the 7inch mask on left and right sides. These alignment marks can be used to align the subsequent mask processes. For three layer BoN interconnects at 100μm pitch, 5 masks namely metal pads patterning, metal pad passivation and photoresist patterning for 1st, 2nd, and 3rd copper plating respectively, were designed with test chip design of 10mmX10mm as well as 20mmx20mm sizes by using cadence software. By using this design masks were fabricated.

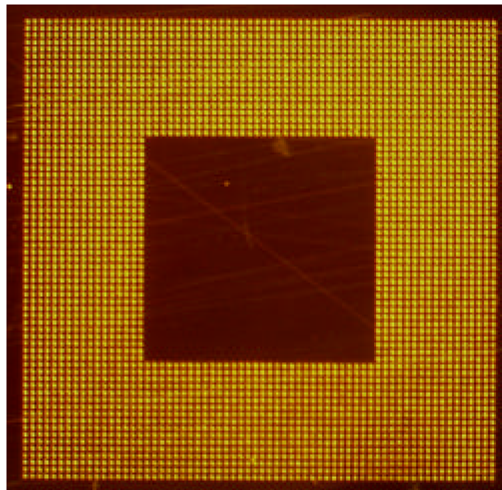


Figure 5.1 Chip design of 10 mm × 10 mm size with 3332 I/Os in 17 depopulated rows

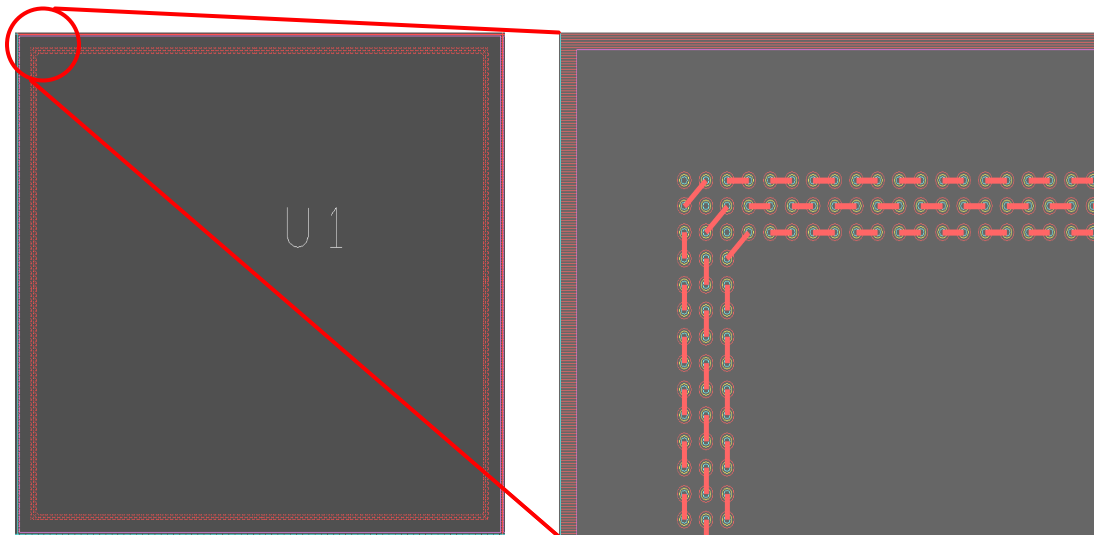


Figure 5.2 Chip design of 20 mm × 20 mm size with 2256 I/Os in 3 depopulated rows

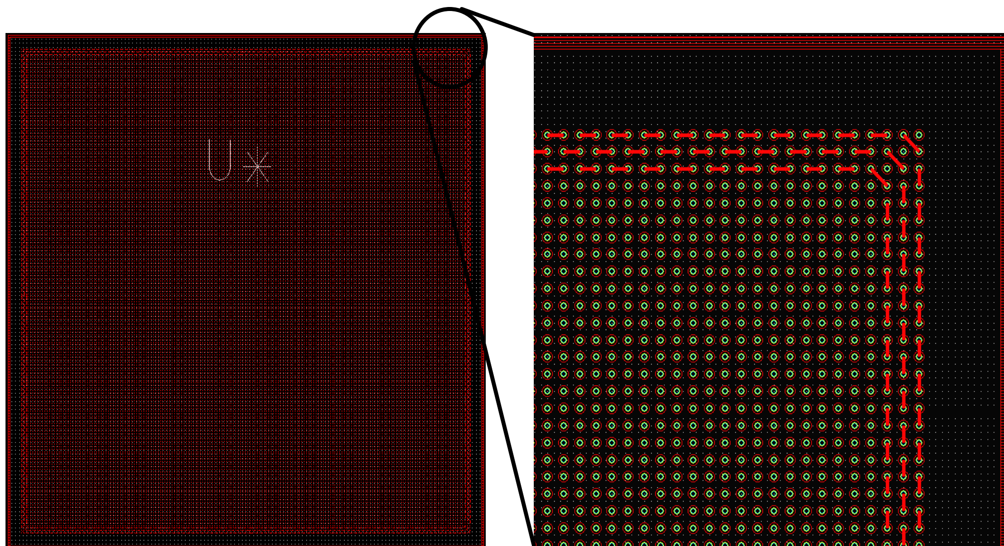


Figure 5.3 Chip design of 20 mm × 20 mm size with 36481 I/Os as fully populated

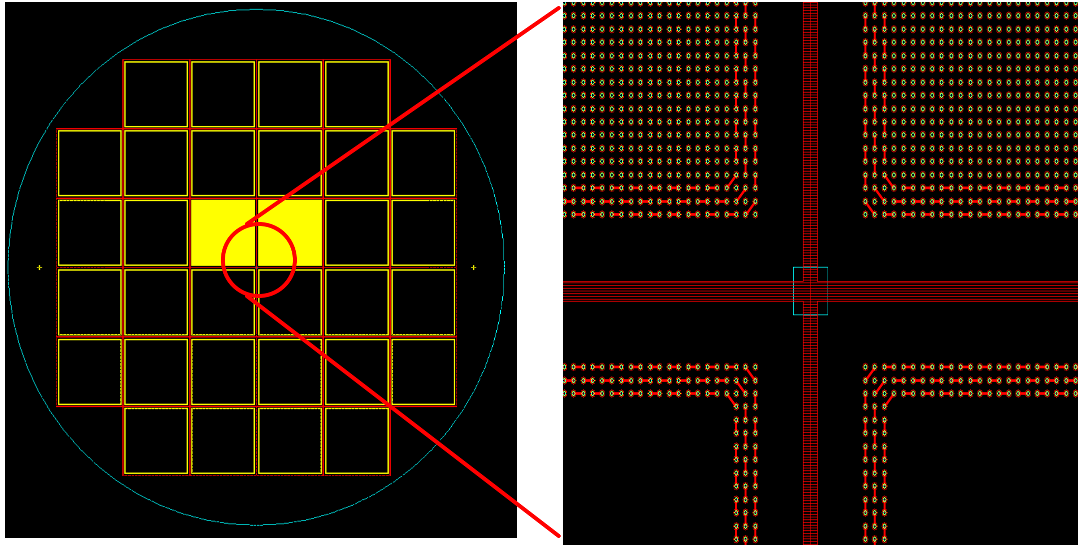


Figure 5.4 Layout design of complete mask (7”) with 20 mm × 20 mm chip design

5.2 Test chip fabrication

5.2.1 Metal pads patterning and their passivation

The test chip fabrication started with the 1000A° Ti/2000A° NiV/ 500A° Au metal layer sputter deposition on a given clean 8inch wafer using Balzer DC magnetron sputtering system. The bottom Ti layer was applied to improve the adhesion between SiO_2 deposited Si wafer and seed layers. The PFI 26A (+ve) photoresist of 2µm thick was then spun, soft baked and UV patterned through metal pad mask (Mask 1), then post exposure baked followed by developing using MF 319 developer and finally hot baked to pattern the above metal layer for metal pads with daisy chains which were used for electrical testing. The conditions used in the above process are shown in Table 5.1.

Table 5.1 Lithography conditions for 2µm thick PFI 26A photoresist process

Spin Speed/ spin time (rpm/ sec)	Soft bake (^{0}C/Sec)	Exposure energy (mJ/Cm^2)	Post-exposure bake (^{0}C/Sec)	Developing time (sec)	Hot bake (^{0}C/Sec)
1200/60	100/60	140	115/60	150	115/60

After patterning, the metal layers were selectively etched one by one using the wet etching process. The etching rate depends on the concentration of etchant and agitation process. The chemical etchants and etching conditions for individual metals were shown in Table 5.2. The etching process was carried out at room temperature and the etching time was optimized to control the under cut of the metal layers. Then the photoresist was stripped using PRS 3000 stripper solution (Shipley corp.) at 65^0C. Optical micrograph of the patterned metal pads with daisy chains was shown in the Figure 5.5.

Table 5.2 List of selective etchant chemicals and etching time for different metals

Metal	Thickness (A^0)	Etchant solution (composition)	Etching time (sec)
Ti	1000	Ethylene glycol : 10% HF (3:1)	20
Ni	2000	HNO_3 : H_2O (1:4)	300
Au	500	Entreat 100 Au etchant : H_2O (1:12)	180

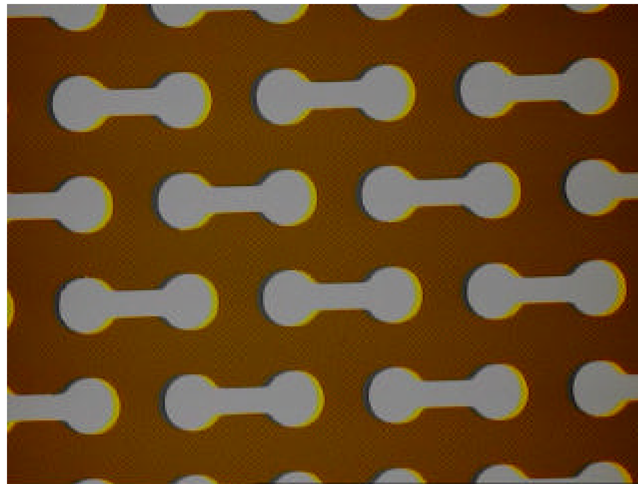


Figure 5.5 Optical micrograph of the patterned metal pads with daisy chains

These daisy chains were passivated using BCB dielectric material. The BCB dielectric material was spun on the wafer using spin coating cycle as shown in Figure 5.6, to obtain 5μm thick layer using SVG 90 series spin track system and soft baked. AP3000 primer was coated on the wafer before BCB coating to improve the adhesion of BCB dielectric material which was then UV-patterned through BCB mask (Mask 2) to open the pads and developed in DS2100 developer solution using lithography conditions as shown in Table 5.3. This patterned BCB dielectric layer was cured in two steps (soft curing and hard curing) to remove the solvent completely in convection heating oven under N_2 atmosphere. The BCB curing profiles in this work were shown in Figure 5.7.

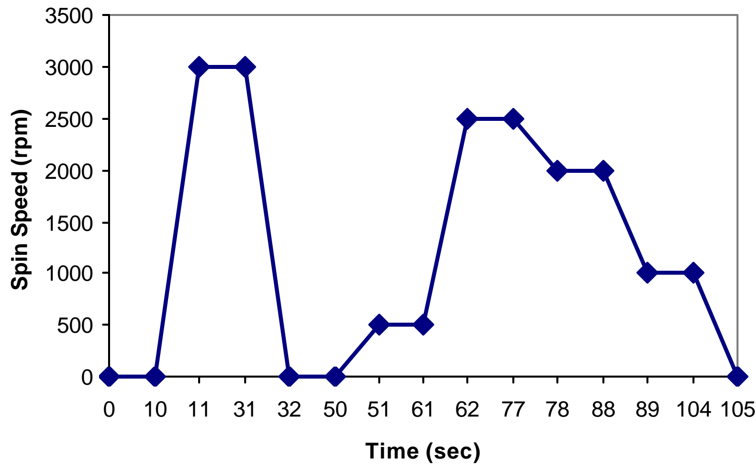


Figure 5.6 AP3000 primer and BCB dielectric material coating cycle

Table 5.3 Lithography conditions for BCB dielectric patterning

Soft bake (^{0}C/Sec)	Exposure energy (mJ/Cm^2)	Post-exposure bake (^{0}C/Sec)	Developing time (sec)	Post develop bake (^{0}C/Sec)
80/90	185	80/30	60	80/60

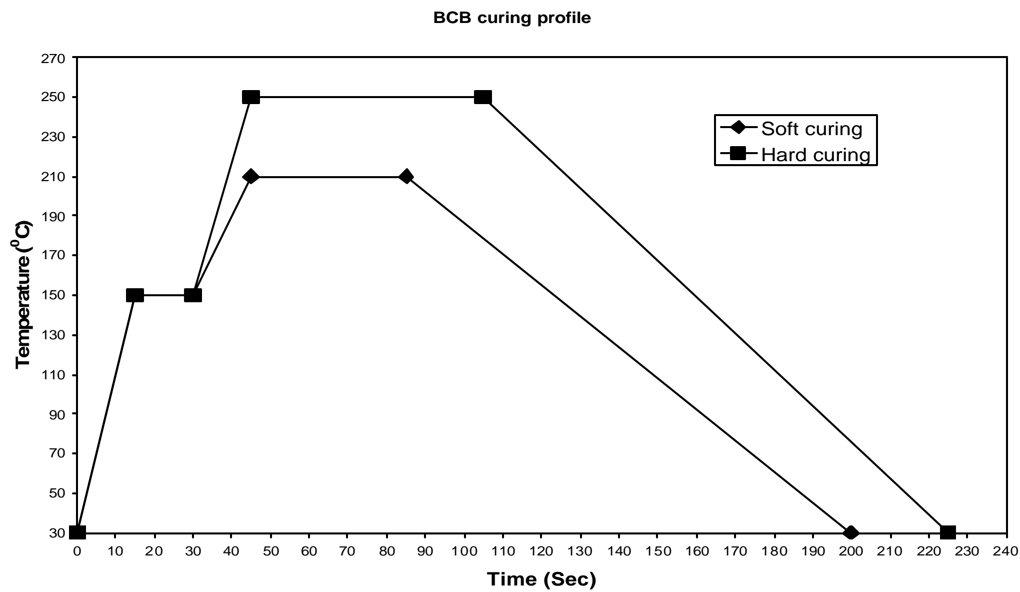


Figure 5.7 BCB soft and hard curing profiles

After hard curing a thin BCB residue layer was observed at the bottom of the pad openings as shown in Figure 5.8. This residue was removed using a descum process by plasmatherm system using BCB, 16sccm O_2 and 4sccm CF_4 gas mixture at 50mbar pressure and 300watts power for 60sec. After the descum process, the residues were completely removed from the BCB opening on the pads as shown in Figure 5.9. The etching rate in this descum process was 400nm per min. Next, sputtering of Ti/Cu or Ti/Au seed layer was done for electrical contact during the electroplating of copper interconnects. The bottom Ti layer was applied to improve the adhesion between dielectric and Cu or Au.

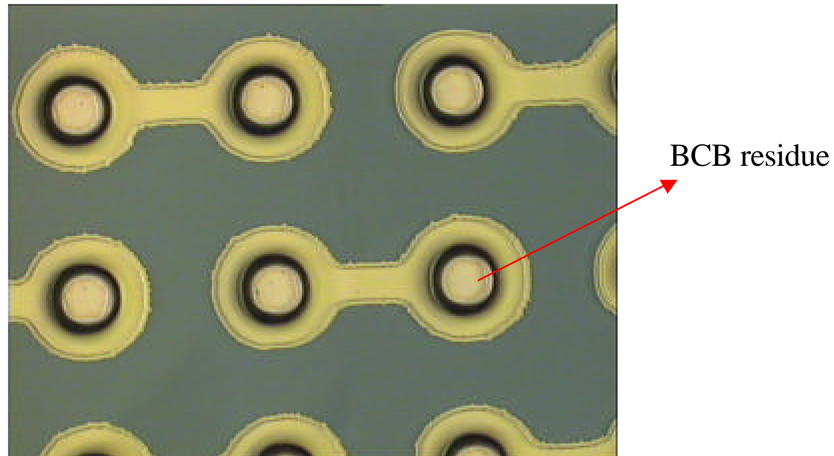


Figure 5.8 Optical micrograph of patterned BCB before descum

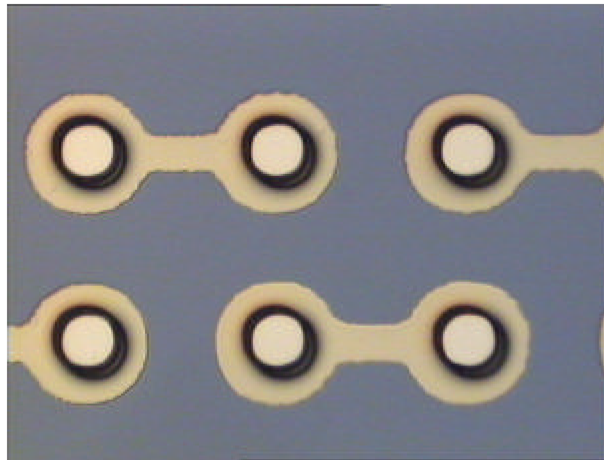


Figure 5.9 Optical micrograph of patterned BCB after descum

5.2.2 Thick resist process for single Column BoN interconnects fabrication

In order to fabricate the single column BoN interconnects; thick photoresist moulds were required initially for copper interconnects electroplating. Initially, positive type photoresist were selected to develop the thick resist molds for electroplating of BoN interconnects because of its compatibility with IC chip fabrication and easy striping after electroplating. The principle of the positive photoresist involves the degradation of photoresist material exposed to the UV-light which dissolves in the liquid developer without affecting the unexposed resist material in the developing process. Hence, dark field and clear featured soda-lime masks were fabricated based on the design to carry out

the process with positive photoresist. Two different types of positive photoresist materials namely, PLA 900 and AZ P 4620 were tried to obtain required thick molds for electroplating. Results revealed that this positive resist materials showed poor side wall verticality with thickness of maximum 20µm in single coating which was not suitable to meet the BoN interconnect dimensions. Hence negative type photoresist materials were selected to develop the 50µm and 100µm thick photoresist process for mould fabrication required for electroplating of copper column BoN interconnects. The principle of this negative photoresist involves physical and chemical changes, when exposed to UV light that renders it insoluble in the liquid developer with the unexposed areas (under the dark area of the photo mask) being removed without expensive effect on the hardened or exposed area in developing process. Hence clear field and dark feature soda-lime masks were fabricated based on the design discussed earlier in Section (5.1) to carry out the process on a contact aligner. Experiments were carried out with two different types of negative photoresist materials namely SU-8 (MicroChem Corp.) and JSR (JSR Corp.) and the details of these photoresist were discussed as follows.

5.2.2 (a) SU-8 Photoresist

First SU-8 2050 negative photoresist was selected for use because it had very high optical transparency which made it suitable for imaging near vertical sidewalls using near UV (350-400nm) lithography in very thick films. Resist thickness of 50µm to 165µm could also be achieved with single spin coat process. Besides, it had excellent chemical resistance that made it suitable for a variety of electrolytic plating bath chemistries. Other advantages include improved coating properties like uniformity and lower surface tension and faster drying of the films [63]. Initially, SU-8 was tested to optimize the process for

50µm thick film with 50µm diameter openings. Many factors affect the resolution limit of above photolithography process, such as spin speed, softbake time and temperature, exposure energy, post exposure temperature and time, and development time. The spin speed acted as important criteria as it controlled the thickness of the resist film. Coating conditions for 50µm thick film was optimized by varying the spin speed using SVG 90 series coating track. The optimized spin coating cycle for 50µm thick film was shown in Figure 5.10.

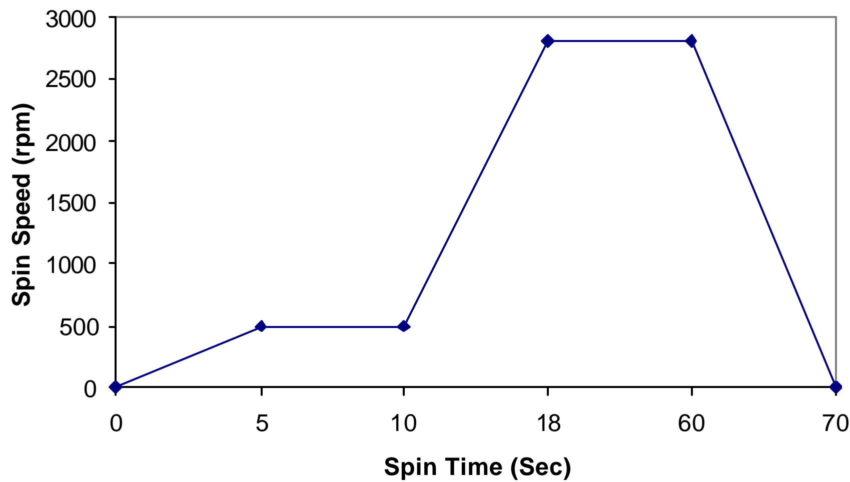


Figure 5.10 Spin cycle for 50µm thick SU-8 resist coating

The above coated thick resist film was patterned through Mask 3 using EVG 640 aligner. In order to obtain near vertical side wall profile, the other parameters excluding the spin speed were considered critical and experiments were carried out using trial and error method to optimize them. The optimized parameters for 50µm diameter openings at 100µm pitch in 50µm thick film were shown in Table 5.4. SU-8 was virtually transparent and insensitive above 400nm but has high atomic absorption below 350nm. Hence near UV i-line (365nm) was used for exposure. The exposure energy for 50µm thick resist

film was optimized using EVG 640 aligner and the exposed resist was developed in the MicroChem's SU-8 developer.

Table 5.4 Lithography conditions for 50μm thick SU-8 photoresist process

Spin Speed/ spin time (rpm/ sec)	Soft bake (^{0}C/min)	Exposure energy (mJ/Cm^2)	Post-exposure bake (^{0}C/min)	Developing time (min)
2800/60	95/5	750	95/4	15

Though straight and near vertical side walls were obtained with SU-8 resist as shown in Figure 5.11, experimental results revealed that SU-8 photoresist had poor adhesion with copper and gold substrates and after the developing process, micro cracks were observed at the edges of the vias as shown in Figure 5.12. Earlier investigations also reported similar observations [64-65]. This cracking might be due to the fact that SU-8 photoresist gets readily cross-linked and resulted in a highly stressed film during the exposure and post exposure backing steps. This cracking caused by the stress can be overcome to a certain extent by increasing the exposure dose and/or increasing post exposure bake (PEB) time and by avoiding the rapid cooling rate after PEB. Due to this above problem, experiments were not conducted for 100μm thick resist film optimization process with SU-8 photoresist.

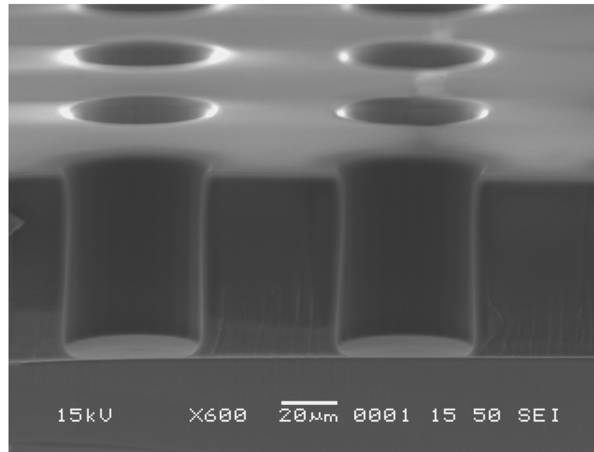


Figure 5.11 SEM micrograph of planar view of 50µm thick patterned SU-8 photoresist with 50µm diameter holes

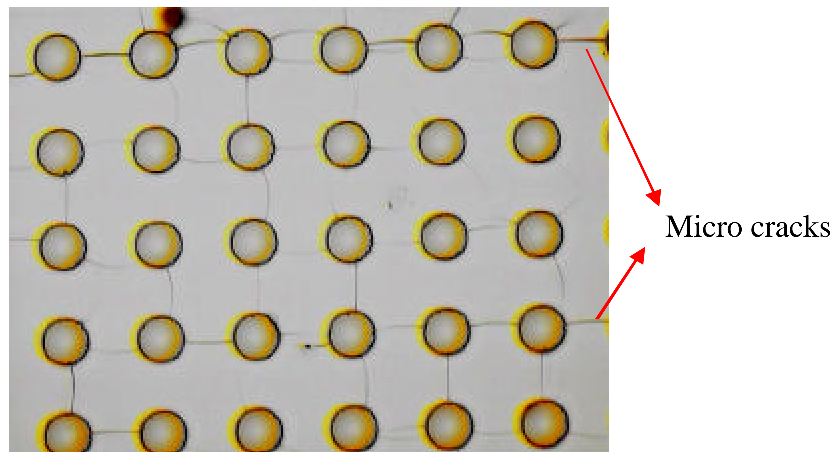


Figure 5.12 Optical micrograph of patterned SU-8 resist with micro cracks

5.2.2 (b) JSR Photoresist

JSR THB-151N photoresist was also selected for the fabrication of thick moulds for electroplating of single column BoN interconnects because it also offered high resolution, high sensitivity to near UV (350-400nm) light, faster drying of the films, excellent plating resistance and resolution strip. Resist thickness of 35µm to 70µm could be achieved with single spin coat process. According to the JSR process sheet the maximum thickness that could be obtained using JSR photoresist in single spin coating

was 70µm at 1000rpm on a 6inch wafer [66]. In this study, first experiments were carried out to optimize the lithography process for 65µm thick film on 8inch wafer. Resist thickness of 65µm was obtained by changing the main spin speed and spin time according to the speed. The thickness of 65µm was obtained at an optimum speed of 700rpm. If the spin speed was maintained below 700rpm along with the corresponding spin time, the thickness obtained was 65µm and was not found to be uniform. The reason for the same thickness of 65µm was because it depends on the solid content in the resist and the non-uniformity was due to the resist material not spreading uniformly throughout the wafer with in the required time. If the spin time was increased further the thickness of the film tends to reduce. The reason for this problem was attributed to the high viscosity of thick resist materials. The optimized spin coating cycle for 65µm thickness was shown in Figure 5.13 and the plot between thickness vs. spin speed was shown in the Figure 5.14.

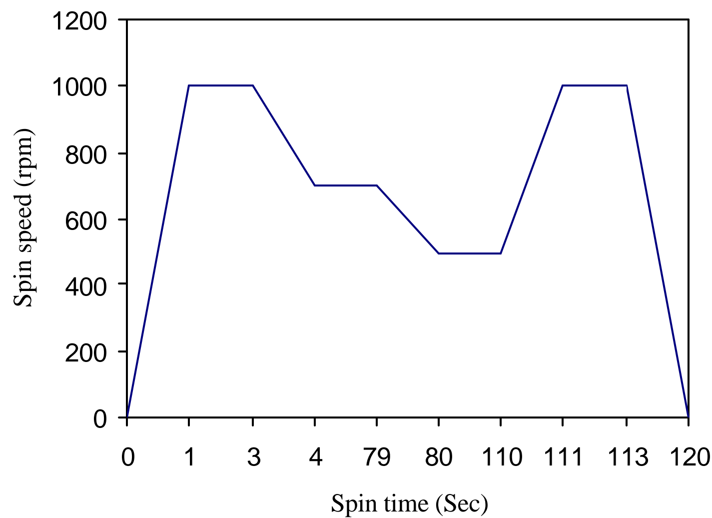


Figure 5.13 Spin cycle for 65µm thick JSR resist coating on 8 inch wafer

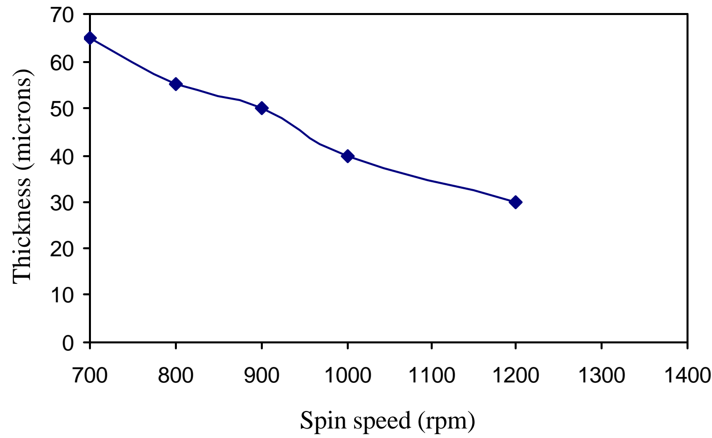


Figure 5.14 Graph of Spin speed vs. thickness for JSR 151N resist on 8 inch wafer

The exposure energy was optimized using EVG 640 contact aligner and the exposed resist was developed in the PD535 developer (supplied by JSR Corp.). The optimized lithography conditions for 50µm diameter vias in 65µm thick film with near vertical sidewalls were shown in Table 5.5. The experimental results obtained revealed good vertical side walls in 65µm thick resist film as evident in Figure 5.15.

Table 5.5 Lithography conditions for 65µm thick JSR photoresist process

Spin Speed/ spin time (rpm/ sec)	Soft bake (^{0}C/min)	Exposure energy (mJ/Cm^2)	Developing time (min)
700/75	120/5	700	6

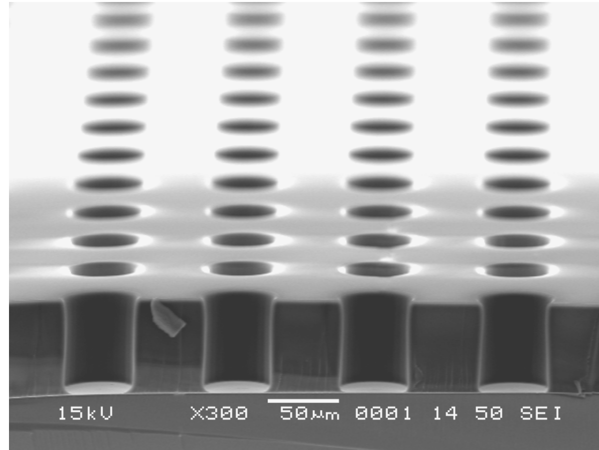


Figure 5.15 SEM micrograph of planar view of 65µm thick pattrned JSR-151N photoresist with 50µm diameter holes

Besides this, a double coating process was optimized for the resist thickness of above 100µm (130µm) film. In this double coat process, the first 65µm thick film was coated using above optimized spin coat cycle and was baked for a short time before applying second layer at lower temperature. After this short soft bake, the second resist layer was coated with the same spin coat cycle and then the total resist film was again subjected to final soft bake. The total resist thickness obtained after two coats was measured to be 130µm. The optimized soft bake, exposure and developing conditions for the double coat process were shown in Table 5.6. The experimental results obtained in the double coat process exhibited near vertical side walls in 130µm thick resist film as shown in Figure 5.16. In addition to the near vertical side wall profile, JSR also had good adhesion to copper and gold substrates compared to SU-8 resist.

Table 5.6 Lithography conditions for 130µm thick JSR photoresist using double coat process

Layer	Spin Speed/ spin time (rpm/ sec)	Soft bake (^{0}C/min)	Exposure energy (mJ/Cm^2)	Developing time (min)
1st layer	700/75	110/3	-	-
2nd layer	700/75	120/9	1200	10

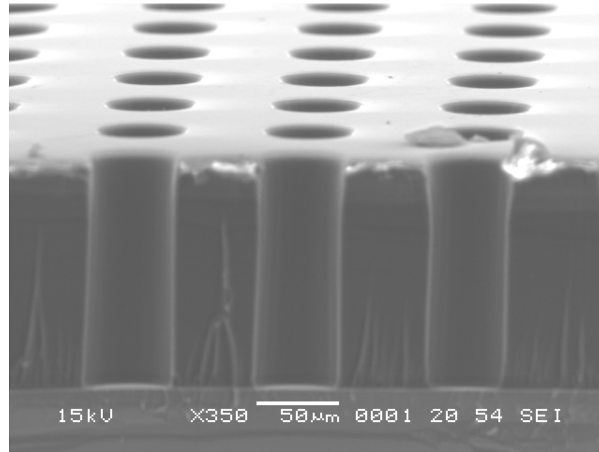


Figure 5.16 SEM micrograph of planar view of 130µm thick patterned JSR-151N photoresist with 50µm diameter holes

Earlier investigations reported that various positive photoresist materials used for fabrication resulted in more number of coating layers, higher exposure energy, longer baking time, increased cost and more number of process steps. JSR photoresist was found to have better properties with more advantageous compared to the other photoresist materials used so far. Thus JSR serves to be the potential photoresist for further use. Comparisons of JSR with other photoresist materials are presented in Table 5.7.

Table 5.7 Comparison of JSR resist with other photoresist materials

Photoresist material	Max Thickness (μm) / no. of layers	Final backing time (min)	Exposure energy (mJ/cm^2)
AZ 4562 [67]	75/4	150 @ 90^0C	8400
AZ 9260 [67]	81/4	150 @ 90^0C	3360
SPR 220-7 [68]	54/3	150 @ 90^0C	12600 (900 Sec)
AZ 4562 [69]	80/2	150 @ 90^0C	4750
JSR	65/1	5 @ 90^0C	750
JSR	130/2	10 @ 120^0C	1200

5.2.3 Copper and solder plating

The photoresist material was spun and patterned on the processed wafer for test chip fabrication in the session 5.2.1 using above optimized lithography conditions. The wafer with photoresist patterned molds was O_2 plasma descumed for 5min using plasmatherm etching system to remove the thin residue film at the bottom of the vias and to activate the resist surface for electroplating process. First, copper was grown in the patterned vias with sputtered Ti/Au seed layer using electroplating. This electroplating was carried out using REENA 8 inch wafer electroplating tool, which was a fountain type (Cup type) in which Sperolyte $CuSO_4$ based solution (Atotech Pte. Ltd) was used as the electrolyte solution. The patterned wafer was loaded into the electroplating tool as stated earlier in Section 3.2.4. The electroplated copper quality and uniformity throughout the wafer depends on the current density, electrolyte flow rate, agitation and additives composition including inhibitors and accelerators like, levelers, brighteners and wetting agents. The other variable taken into consideration during electroplating was the exposed

surface area of the wafer for plating because the current density of the wafer interface determines the deposition characteristics which include the deposition rate and morphology of electroplated copper. Hence the total developed area of the open molds was estimated for 10 mm × 10 mm and 20 mm × 20mm test chip designs on 8inch diameter wafer as 1000mm^2 and 300mm^2 based on the copper column mask layouts respectively.

The optimum plating conditions were obtained by varying the current and flow rate with the addition of Cupracid HL leveler and brightener (Atotech Pte. Ltd). The wettability of the electrolyte was improved by rotating the wafer at higher speed for 2min and the rotation speed was reduced to get the good plating properties such as uniformity and morphology of electroplated copper. The uniformity of the electroplated copper was improved using higher electrolyte flow rate along with lower rotation speed of the wafer chuck. During the deposition, wafer was rotated in a clockwise and then in anticlockwise direction for 2min alternatively in order to prevent the non uniformity in the thickness of plated BoN interconnects. The required plating thickness was obtained by controlling the current and plating time. The optimum plating conditions used to electroplate the copper in the vias of photoresist for 10 mm × 10 mm and 20 mm × 20 mm size test chip wafers were presented in Table 5.8 and 5.9. The current density used in this optimized process was 30mA/cm^2. The copper deposition rate with the above optimized plating conditions was 0.5µm/min and the total electroplating time to deposit a 50µm height copper post of BoN interconnect was around 100 min.

The cross-section analysis revealed that the electroplated copper column was vertical, uniform at the top surface of the copper column and free of void as shown in

Figure 5.17. Careful observation was very essential during the end of the plating process to avoid over plating or under plating. Hence the wafer was removed from the plating bath frequently water rinsed and dried. Then the wafer was examined by the profilometer to check the surface profile at the plating areas. If the surface in the molding area is lower than the mold edge, plating should be continued to get a proper thickness. Before placing this wafer back into plating bath, preventive measures must be taken to remove the oxidation of the copper due to the long time exposure to the atmosphere by immersing it into 10% dilute sulphuric acid for 2-3 min.

Once plating was completed, the above wafer was rinsed, dried and made ready for next process. After copper plating, the eutectic Tin-Lead solder was plated at the tip of the copper column using RENA 8inch wafer electroplating tool, which was rack type in which Sperolyte Sn-Pb based solution (Atotech Pte. Ltd) was used as electrolyte solution and tin-lead pellets were used as anode. The solder thickness and uniformity was controlled by varying current density, electrolyte flow rate and plating time. The optimum electroplating conditions as shown in the Table 5.8 and 5.9 were used to plate the solder for 10 mm × 10 mm and 20 mm × 20 mm size test-chip wafers, respectively. The current density used in this optimized process was $15 mA/cm^2$. The solder deposition rate with the above optimized plating conditions was 0.8µm/min and the total electroplating time to deposit a 15µm height solder at the tip of copper column was around 20 min.

This solder plating was formed as a mushroom shape at the tip of the copper column as shown in Figure 5.18. If the solder plating was increased beyond a certain limit, the mushroom shaped interconnects would club with the adjacent interconnects. In

order to avoid this problem, the vias are filled with copper up to 50μm and solder was filled in the remaining 15μm. If the plating was increased more than the vias, again the above mentioned problem occurred. Current density and the plating time were optimized to solve the above problem.

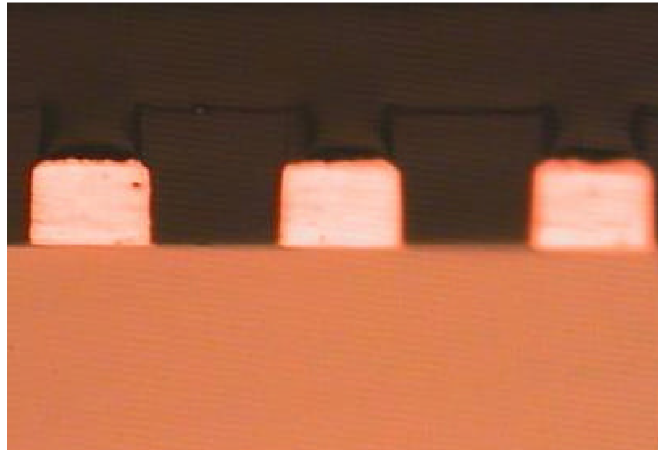


Figure 5.17 Cross sectional view of copper filled vias in photoresist

Table 5.8 Plating conditions for copper and solder electroplating of 10mmx10mm size test chip wafer

Plating metal	Thickness (μm)	Flow rate (lt/min)	Current (mA)	Temperature (^{0}C)	Time (min)
Copper	50	24	300	25	100
Solder	15	10	150	25	20

Table 5.9 Plating conditions for copper and solder electroplating of 20mmx20mm size test chip wafer

Plating metal	Thickness (μm)	Flow rate (lt/min)	Current (mA)	Temperature (^{0}C)	Time (min)
Copper	50	24	100	25	100
Solder	15	10	50	25	20

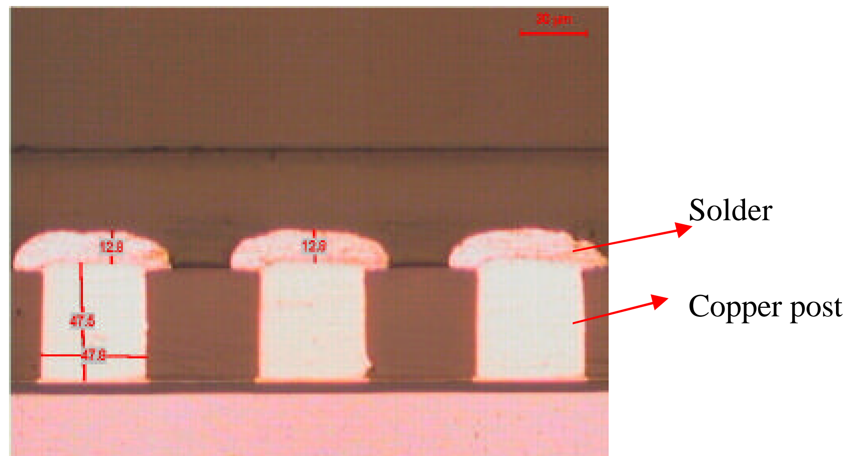


Figure 5.18 Cross sectional view of 100μm pitch BoN interconnects in photoresist

5.2.4 Thick photoresist stripping

5.2.4 (a) SU-8 resist stripping

After copper and solder electroplating, the thick SU-8 photoresist film was stripped with MicroChem's Remover PG at 80^{0}C temperature. The results revealed that the stripping of SU-8 resist after copper and solder plating was difficult using remover. This may be due to the highly cross-linked property of the SU-8 resist after exposure and hard baking at 95^{0}C which resulted in difficult stripping. Even after a long striping process, the SU-8 residues were observed in between interconnects at the bottom at the above temperature. SU-8 residues after stripping were evident in Figure 5.19. Earlier reports also observed that SU-8 removal after post-exposure bake and developing was difficult using solvent based stripper solutions.

Figure 5.19 Optical micrograph of SU-8 residues in between the BoN interconnects after stripping

SU-8 photoresist can be removed using plasma etching with a combination of oxygen and fluorine plasma, but this process was quite time consuming and expensive. In addition to problems like poor adhesion and cracking at the edges of vias, the difficulty in stripping was also an added issue in SU-8 resist. Hence experiments were not conducted for the 100µm thick resist film optimization process with SU-8 photoresist and efforts were focused on another thick negative type JSR resist.

5.2.4 (b) JSR resist stripping

After copper and solder electroplating in the patterned JSR resist, the resist was stripped using THB-S1 stripper solution supplied by JSR Corp. at 60^0C. JSR resist was found to completely dissolve into the stripper within 20 minutes but residues at certain areas were observed. These residues were removed with some small agitation during the stripping process. The dissolution rate was also improved due to agitation. The final result revealed that JSR stripping was easy compared to SU-8 resist and free of residues in between interconnects. Figure 5.20 shows the BoN interconnects after JSR resist stripping.

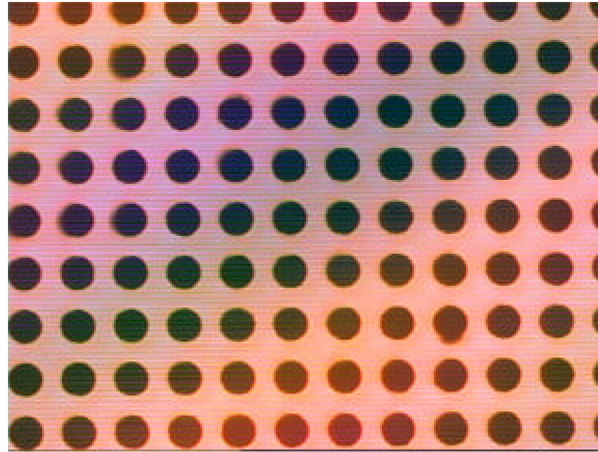


Figure 5.20 Optical micrograph of BoN interconnects after JSR resist stripping

After stripping the photoresist, the Ti/Au seed layer was selectively etched using same conditions discussed earlier in session 5.2.1

5.2.5 Solder reflow

After stripping the photoresist and seed layer etching, the electroplated eutectic Sn-Pb solder was reflowed in 6-zone reflow oven in N_2 atmosphere using reflow profile as shown in Figure 5.21. In this reflow profile, solder was reflowed at above the liquidus temperature of eutectic tin-lead solder (235^0C) for about 80seconds to form the solder bump at the tip of BoN interconnects. Figure 5.22 shows the planar view of BoN interconnects before reflow. After reflowing once, the results revealed that the solder bump shape was not spherical as shown in Figure 5.23. To obtain a good spherical bump shape, the wafer was reflowed twice at the same profile. The reason for the improper bump shape during the initial reflow was because the solder was not melted properly whereas when reflowed again using flux proper melting of solder took place resulting in spherical bump. Results revealed spherical shaped bump and uniform bump height.

Figure 5.24 shows the planar view of the BoN interconnects after solder reflow using flux.

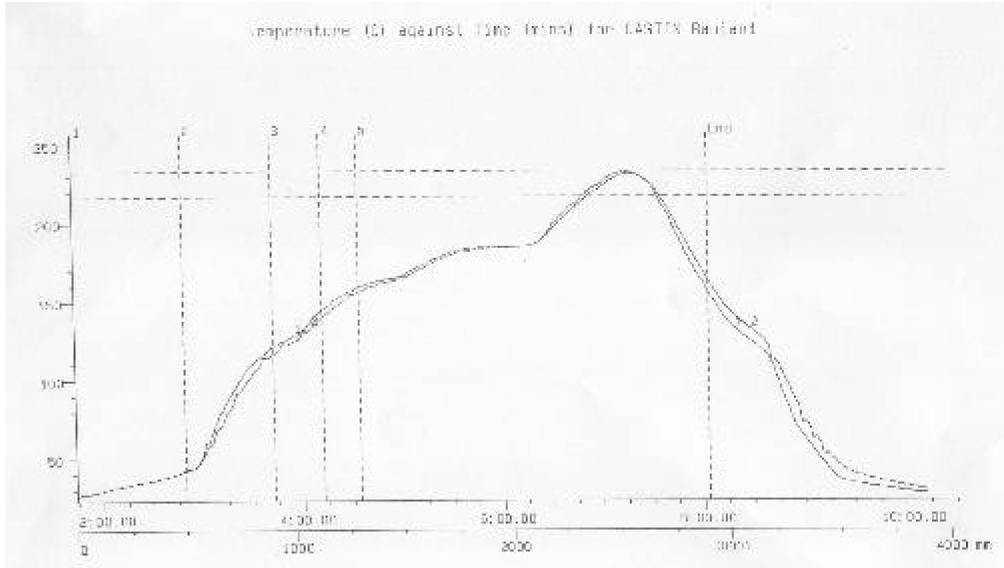


Figure 5.21 Eutectic tin-lead solder reflow profile

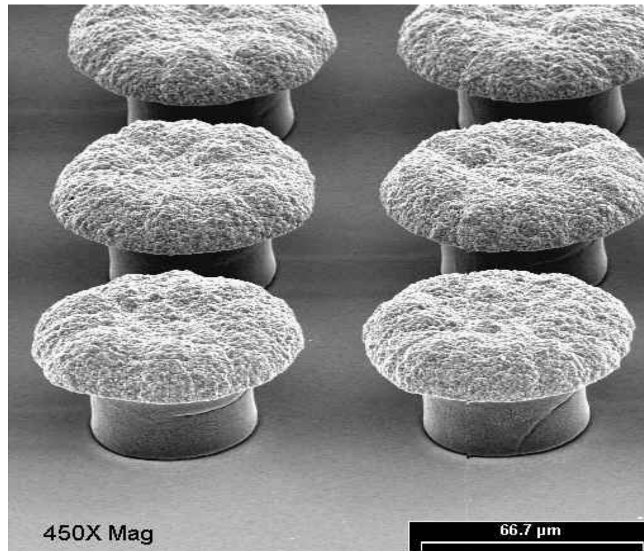


Figure 5.22 Planar view of BoN interconnects before solder reflow

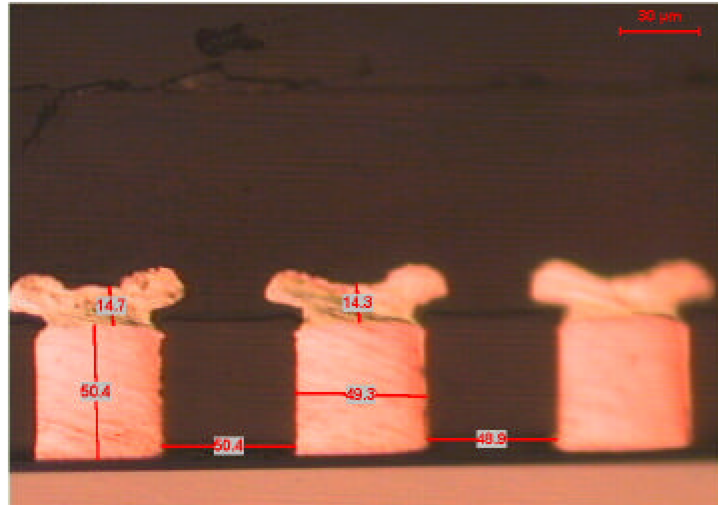


Figure 5.23 Cross-sectional view of BoN interconnects after one time solder reflow

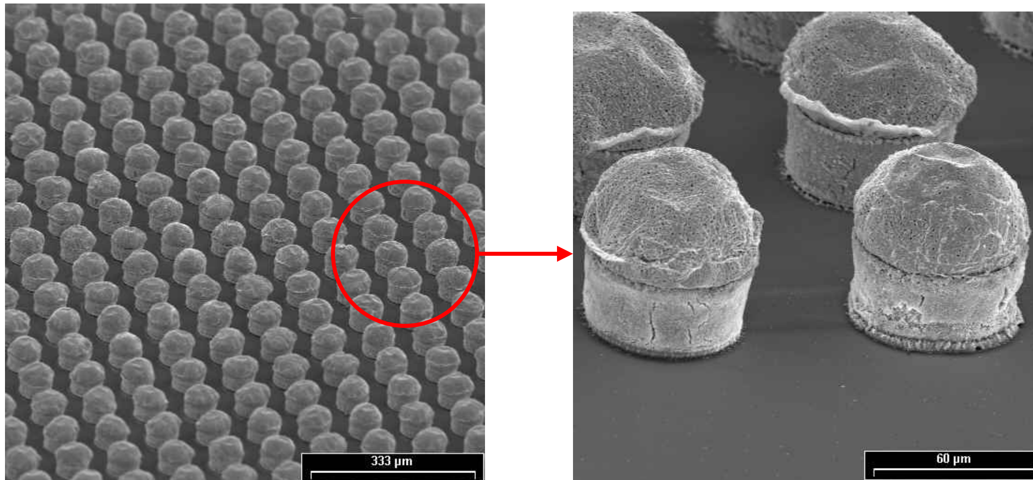


Figure 5.24 Planar view of BoN interconnects after solder reflow using flux

Once the BoN interconnects were fabricated on the wafer, they were ready for bonding to next level substrate. Hence, the wafer with BoN interconnects was diced into individual dies using a dicing machine. The above optimized conditions were used for the fabrication of 10 mm × 10 mm and 20 mm × 20 mm test chips. Figure 5.25 shows the SEM micrograph of area array of the BoN interconnects in 20 mm × 20 mm test chip.

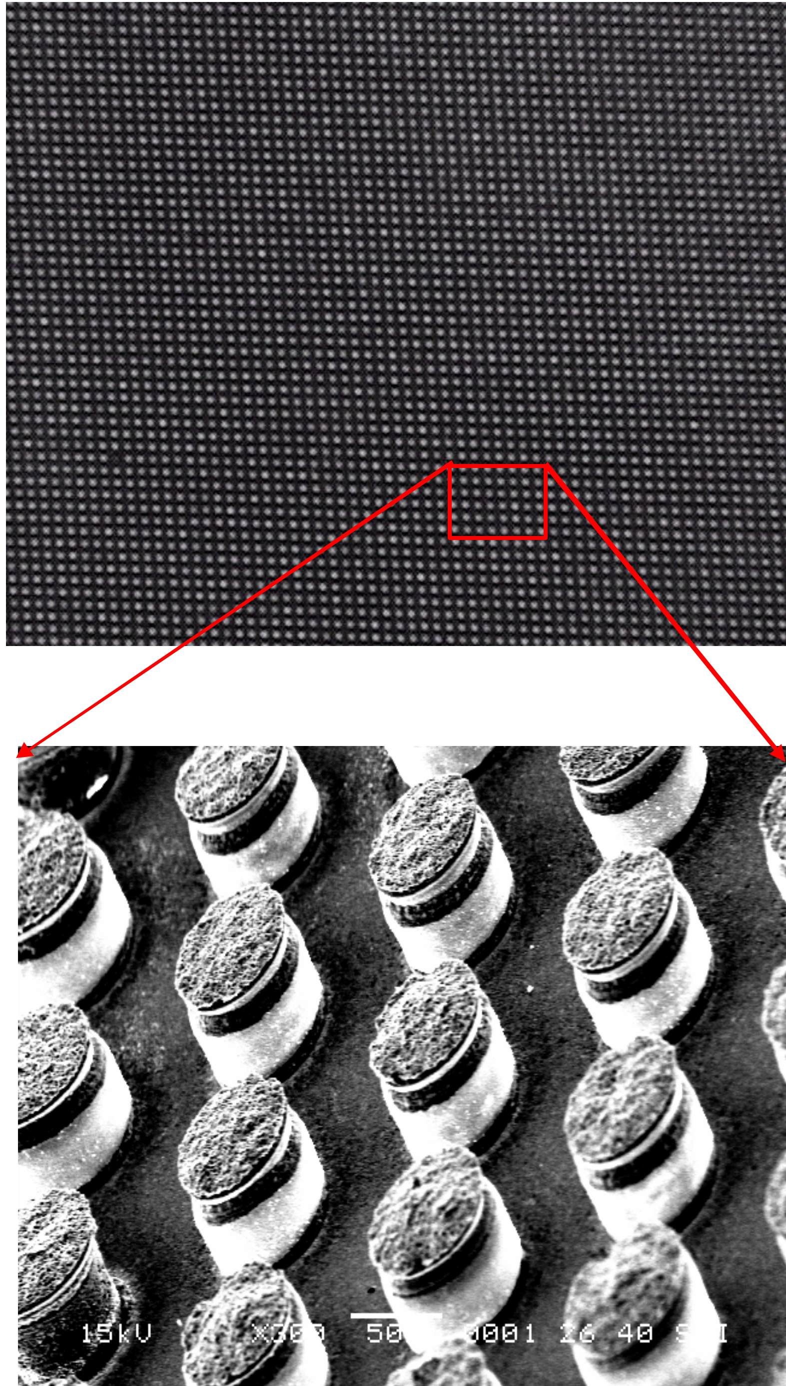


Figure 5.25 SEM micrograph of area array of BoN interconnects on 20 mm × 20 mm test chip

5.3 Solder bump fabrication

In order to make comparisons, eutectic Sn/Pb solder bumps at the same pitch were fabricated using the same process. Masks of 20 mm × 20 mm size test chip design were used for this solder bump fabrication. The process steps involve electroplating of the solder in the patterned resist vias completely. The solder plating was carried out using the earlier optimized conditions shown in Table 5.9 in session 5.2.3. Figure 5.26 shows optical 3D micrograph of the electroplated eutectic tin-lead solder bumps at 100µm pitch before and after reflow.

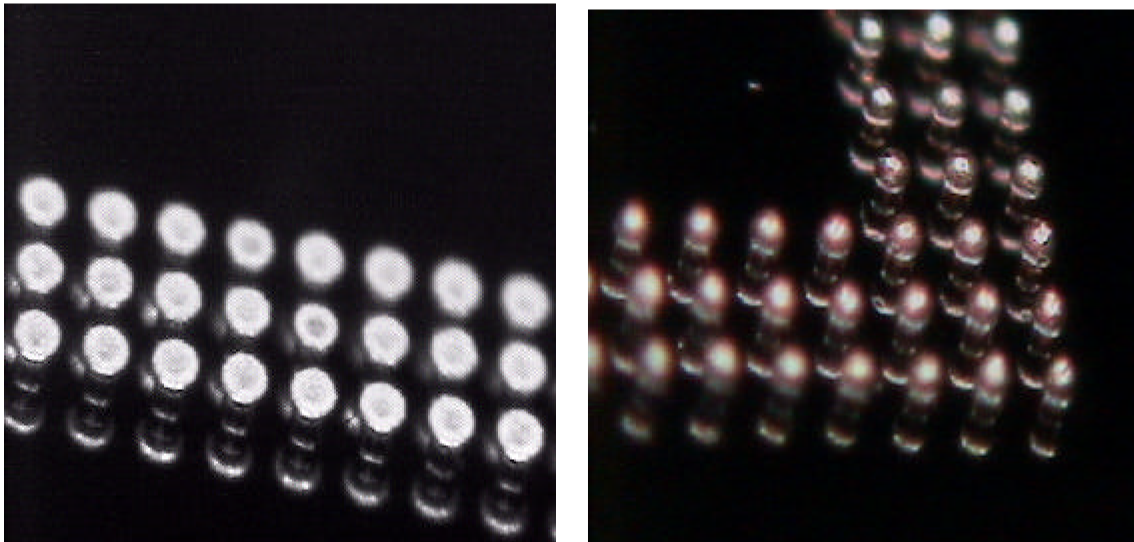


Figure 5.26 Electroplated eutectic tin-lead solder bumps before and after reflow

5.4 Bump shear test

The bump shear test was done to the above fabricated BoN bumps to evaluate the shear strength and to investigate the failure mode of bumps. Bump shear tests were carried out on the Model BT24 Dage Ball Shear Tester. Table 5.10 shows the parameters used in the bump shear test. Bump shear tests were carried out at different bump shear

height and shear speed. For each case, at least 20 bumps were tested. For comparison, shear tests of electroplated eutectic solder bumps of the same size were also tested.

Table 5.10 Bump shear test parameters

Shear speed(mm/s)	0.05, 0.2, 0.5	Shearing Height (µm)	5, 10, 15
Fallback	80%	Bump Diameter (µm)	50
Landing speed (mm/s)	0.2000	Pad shape	circle
Over travel (µm)	50	Pad diameter (µm)	50

The results showed little variation in the average shear force with increasing shear height at all shear speeds as shown in Figure 5.27. There was not much change on the average shearing force with shear speed at the same shear height. Thus the shear height of 10µm, 15% of the total bump height and shear speed of 200µm/sec was taken into consideration. The shear test for eutectic solder bumps also were done at shear height of 10µm. The average shear force of BoN was measured as 26.7 grams at shear height of 10µm and shear speed of 200µm/Sec whereas the average shear force of eutectic Sn/Pb solder tested at the same conditions was 17.6 grams.

SEM and EDX analysis were conducted on the sheared bump pads to investigate the failure mode of BoN interconnect. Analysis revealed that all failures occurred at the edges of copper column and seed layer interface whereas at the centre of the copper column the failure mode was observed to be ductile shear. The above failure modes analyzed by SEM and EDX were evident in Figure 5.28 and 5.29. The bump edge failure mode may be attributed to the small interface area between the copper column and the seed layer.

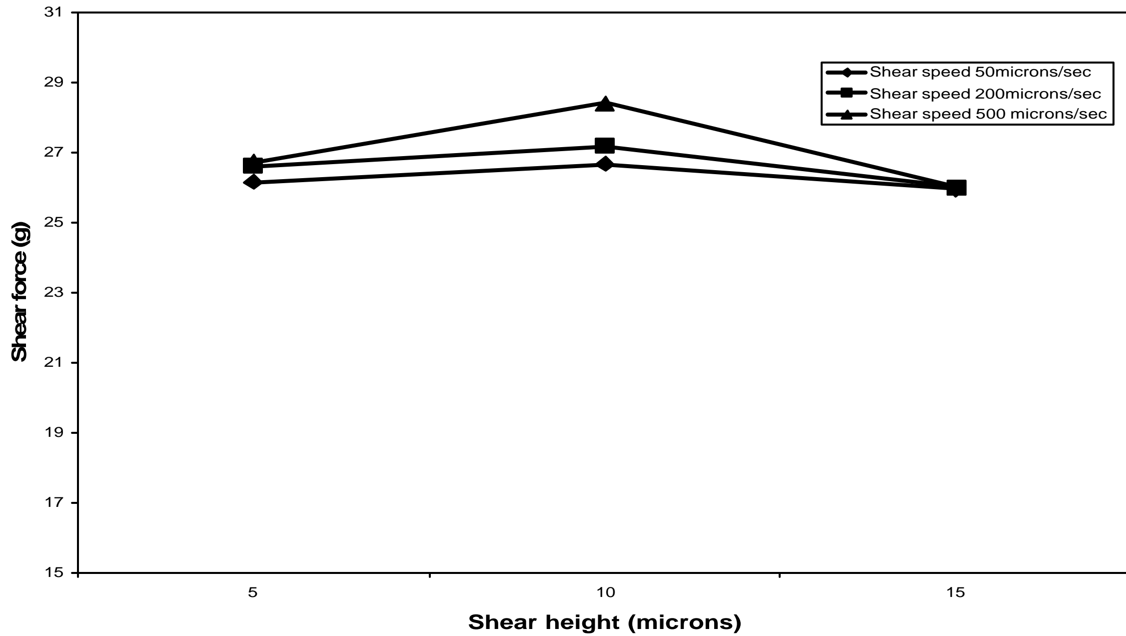


Figure 5.27 Graph of shear force vs. shear height at constant shear speed

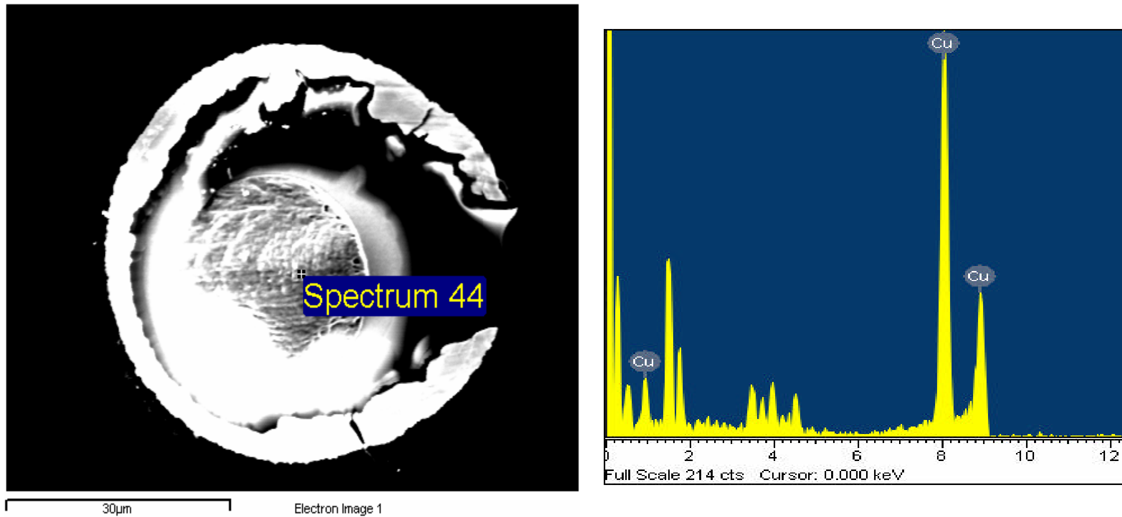


Figure 5.28 SEM micrograph of sheared bump pad and EDX graph at the center of sheared bump pad

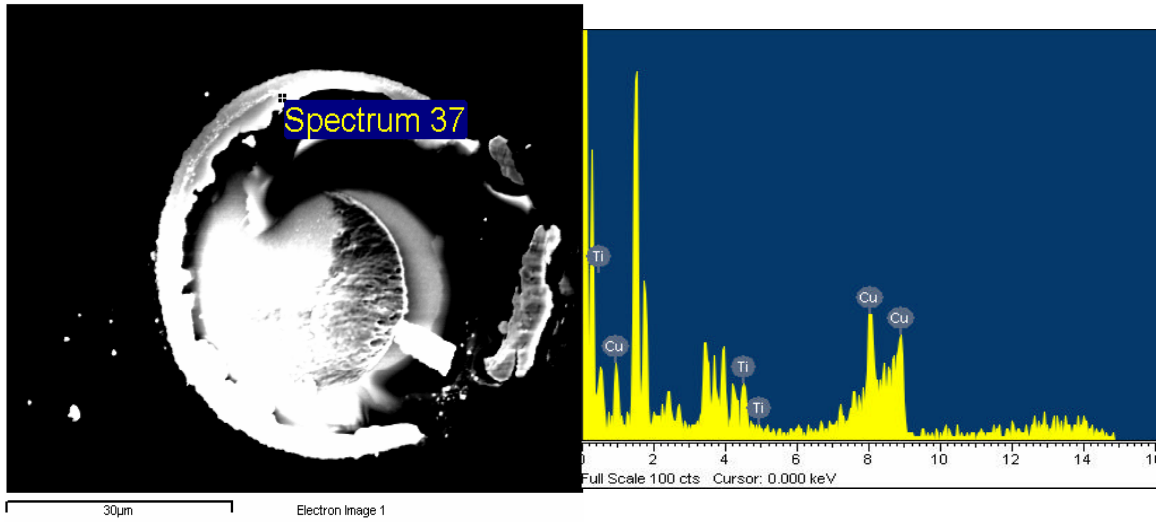


Figure 5.29 SEM micrograph of sheared bump pad and EDX graph at the edge of sheared bump pad

CHAPTER 6

ASSEMBLY, RELIABILITY AND FAILURE ANALYSIS

6.1 Introduction

To assess the fatigue life of BoN interconnects, testing the fabricated test chips with BoN interconnects were necessary. For the above testing, the required test vehicles were designed and fabricated for two different test chips of 10 mm × 10 mm and 20 mm × 20 mm sizes. The test chip assembly process was optimized and the fabricated test chip was assembled on the test boards using the optimized process. These assembled test dies was subjected to thermal cycling test as per the JEDEC standards. In general solder interconnects were widely using in packaging technologies. Hence, the reliability results of the BoN interconnects obtained was compared with 200µm pitch solder bump interconnects. Shear strength of the BoN interconnects was also estimated using the die shear test on assembled test die. After thermal cycling test, possible failure modes were analyzed using SEM cross-sectional analysis. Finally, the recommendation to improve the reliability of the BoN interconnects was also suggested in this chapter.

6.2 Test board design

Test boards with daisy chains were essential to assemble the BoN interconnect test chips in order to asses the reliability of BoN interconnects. The test boards were designed for 10 mm × 10 mm and 20 mm × 20 mm size test chips corresponding to the test chip designs. The specifications of daisy chain test dies and test boards of 10 mm × 10 mm and 20 mm × 20 mm are listed in Table 6.1 and 6.2, respectively. The test boards for 10 mm × 10 mm test die were fabricated using standard FR-4 board material of

18ppm/^{0}C CTE with non-solder mask defined (NSMD) flip chip bond pads of electroless nickel and immersion gold surface finish and it consists of 4 flip chip attachment sites as shown in Figure 6.1. Each flip chip attachment site design consisted of 20 daisy chains by connecting the outer and center interconnects, as shown in Figure 6.1.

Table 6.1 Specifications of test dies

Test die size (mm)	10 mm × 10 mm	20 mm × 20 mm
Number of bumps	3338	2252
Bump layout	Depopulated in outer 17 rows	Depopulated in outer 3 rows
Bump type	Electroplated eutectic Sn/Pb at the tip of electroplated copper column	
Bump pitch	100µm	
Bump height	65µm	
Bump diameter	50µm	
Passivation	Benzocyclobutene (BCB)	

Table 6.2 Test board specifications for test dies

Test Board	10 mm × 10 mm	20 mm × 20 mm
Material	FR-4 (~18ppm/^{0}C)	High T_g FR-4 ((~10ppm/^{0}C)
Pad finish	Cu/Electroless Ni/Au	Cu/Electroless Ni/Au
Board dimension (mm)	150 X 125 X 1	40 X 50 X 1
Pad diameter	70µm	
Pad pitch	100µm	
Solder mask design	NSMD	SMD/SMD with eutectic Sn/Pb solder finish
No. of Flip chips mounting on test board	4	1

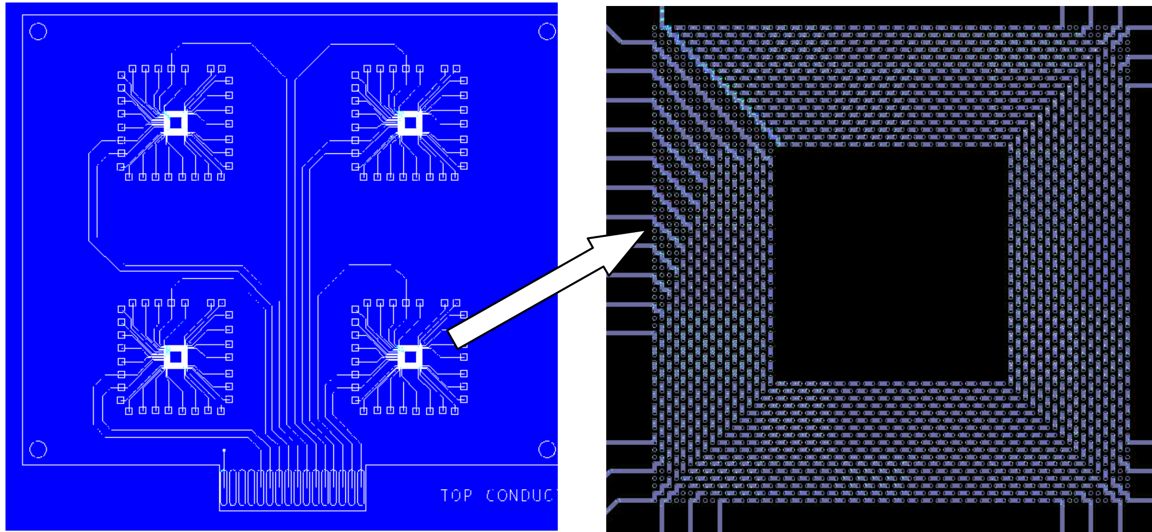


Figure 6.1 Test board design for 10 mm × 10 mm test die

The test boards for 20 mm × 20 mm test die were fabricated using standard FR-4 board material of ~10ppm/^{0}C CTE with solder mask defined flip chip bond pads of electroless nickel and immersion gold surface finish. Test boards with eutectic Sn/Pb solder finish were also fabricated. Each test die design consisted of 11 long daisy chains by connecting the outer and center interconnects, as shown in Figure 6.2. These 11 daisy chains were again divided into 30 small chains by connecting corners and sides of the test die to trace out the exact failure sites.

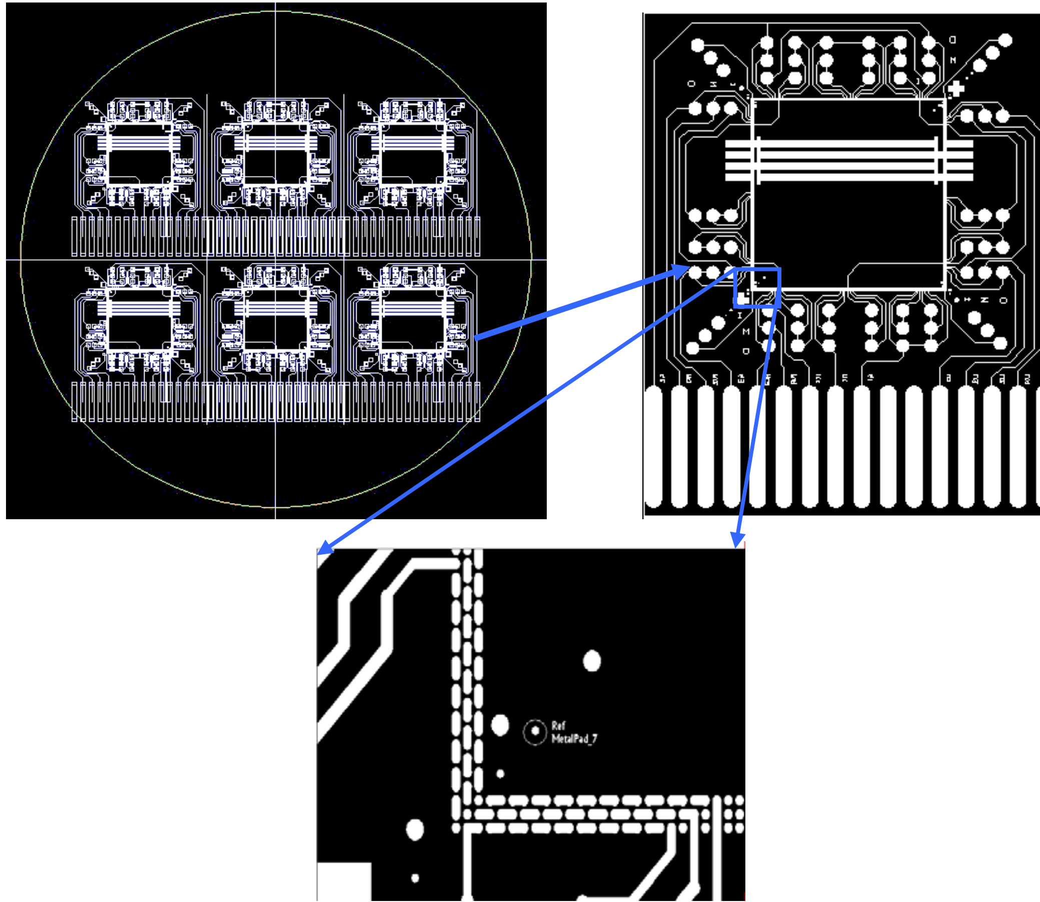


Figure 6.2 Test board design for 20 mm × 20 mm test die

6.3 Assembly process

The test chip with 50μm diameter, 65μm height BoN interconnects at 100μm pitch fabricated earlier (discussed in chapter 5) was assembled on the conventional test board with the non-solder mask defined pads using Karl-Suss flip chip bonder (FC-150). This assembly process was carried out without underfill. Kester 6521C and Kester 1865 liquid fluxes were applied to the interconnect bumps for proper melting of solder during

the assembly. The schematic representation of the assembly method is shown in Figure 6.3.

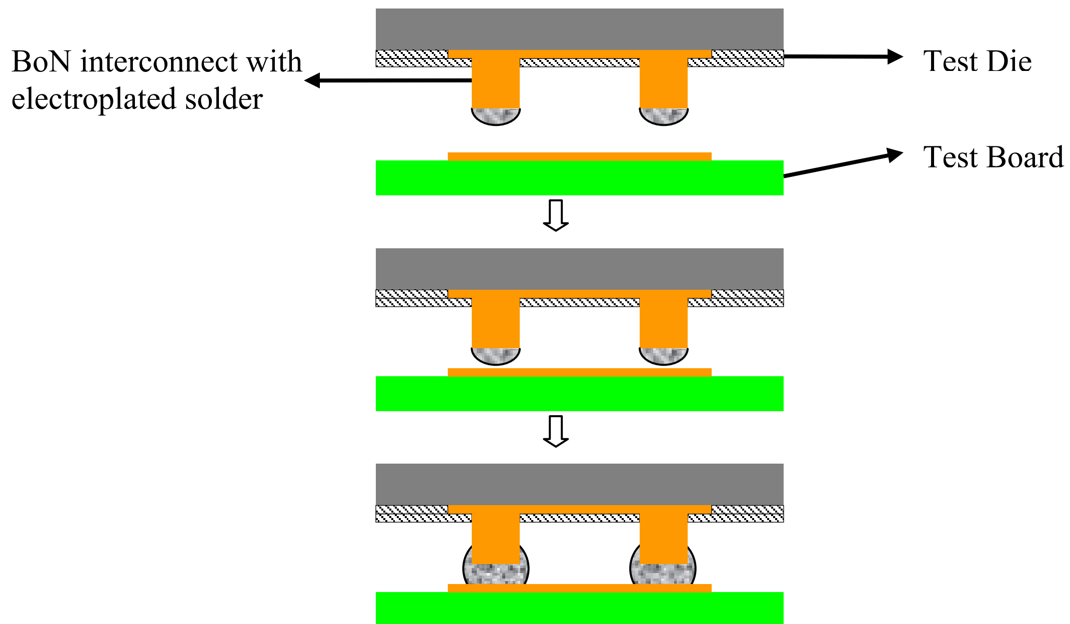


Figure 6.3 Schematic diagram of BoN off-Chip interconnect assembly process

6.3.1 Assembly process optimization for 10mmx10mm test chip

The assembly process optimization was concentrated on various parameters which included the bond force, in-situ reflow temperature, alignment temperature, cooling time, bonding time, and Z-direction force control. Initially experiment were carried out with 1kg bonding force, 235^0C insitu reflow temperature and 70^0C alignment temperature. The bonding profile is shown in Figure 6.4.

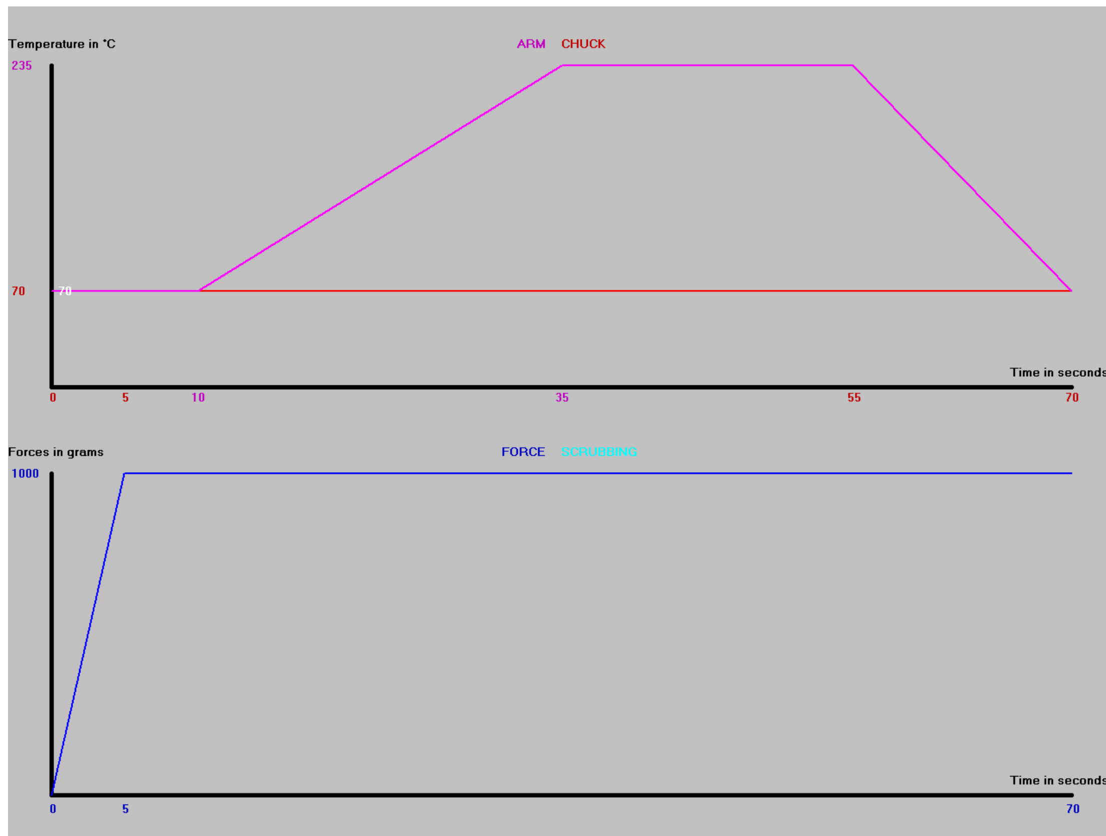


Figure 6.4 Flip chip bonding profile with bonding force for 10 mm × 10 mm test chip assembly

The X-ray scanning was done on the assembled test chip to check whether any two daisy chains were short circuited or not. Results revealed that a few daisy chains were short circuited as evident in Figure 6.5 along with the solder being spread on the bond pad traces as shown in Figure 6.6. The cross sectional analysis revealed that a solder bridge was formed in between the two interconnects on the pads. This problem was considered severe because the bridging resulted in the formation of additional solder column in between interconnects as shown in Figure 6.7. The reason for this bridging may be attributed to the high bonding force on the chip and easy solder wettability on the metal pads as there is no solder mask. Daisy chain resistances were also measured to

asses the connectivity of chains. Results obtained revealed that all chains are open which may be due to the short circuit in daisy chains.

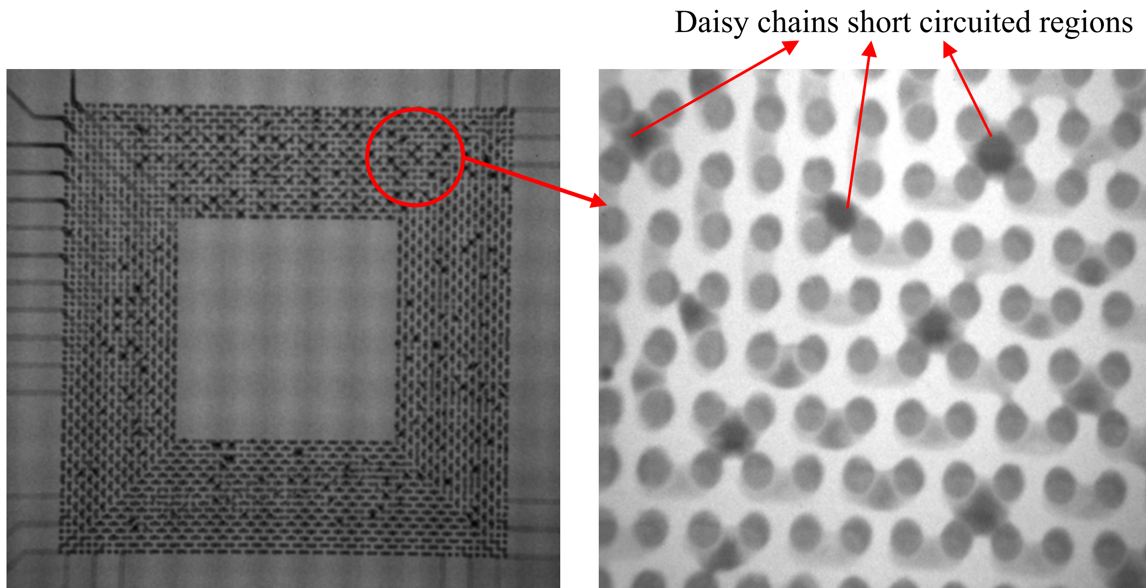


Figure 6.5 X-ray scanning micrograph of assembled 10 mm × 10 mm test chip with daisy chain short circuits

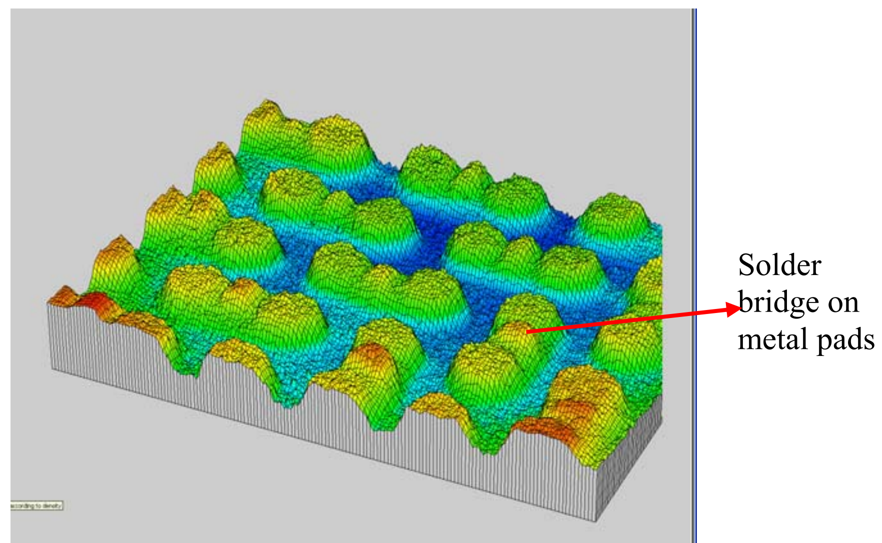


Figure 6.6 X-ray scanning of assembled package in 3-D view

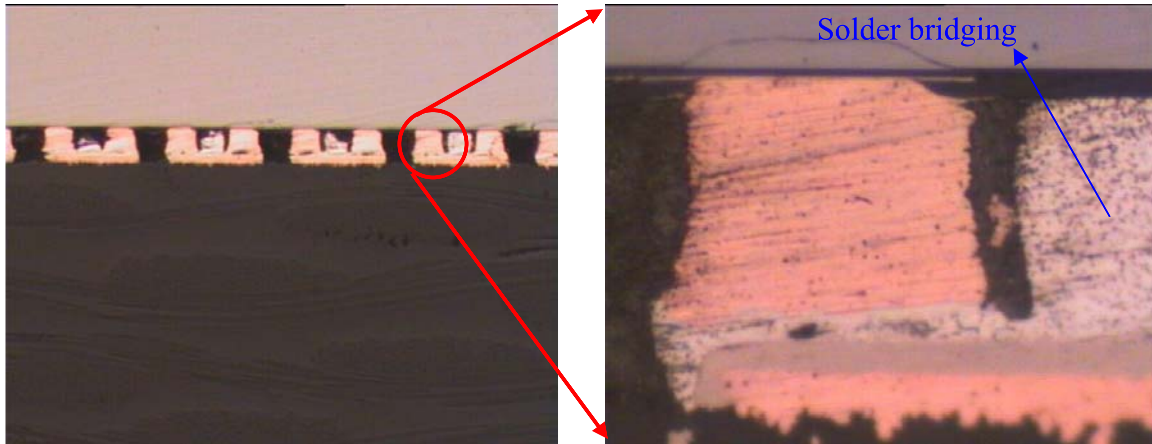


Figure 6.7 Cross-sectional view of assembled 10 mm × 10 mm test chip

To overcome the above problems a number of assemblies were fabricated by varying bond force, alignment temperature, cooling time, and bonding time. Finally daisy chain short circuiting problem was overcome using the assembly profile shown in Figure 6.8. This assembly was carried out without bond force and here chip weight itself acts as bond force. X-ray screening of assembled package shows that there is no short circuit between two daisy chain pads as shown in Figure 6.9. Though daisy chains were not short circuited, solder spread along the daisy chain traces were observed as shown in Figure 6.10. The cross-sectional analysis of packages revealed that the solder bridge was formed in between the two interconnects on the pads but the severity was less when compared to the previous assembly process using force because the solder was formed as a small layer in between interconnects. Yet, the formation of solder bridge was found to be a problem because the solder volume between copper column and substrate was reduced due to the spreading of solder.

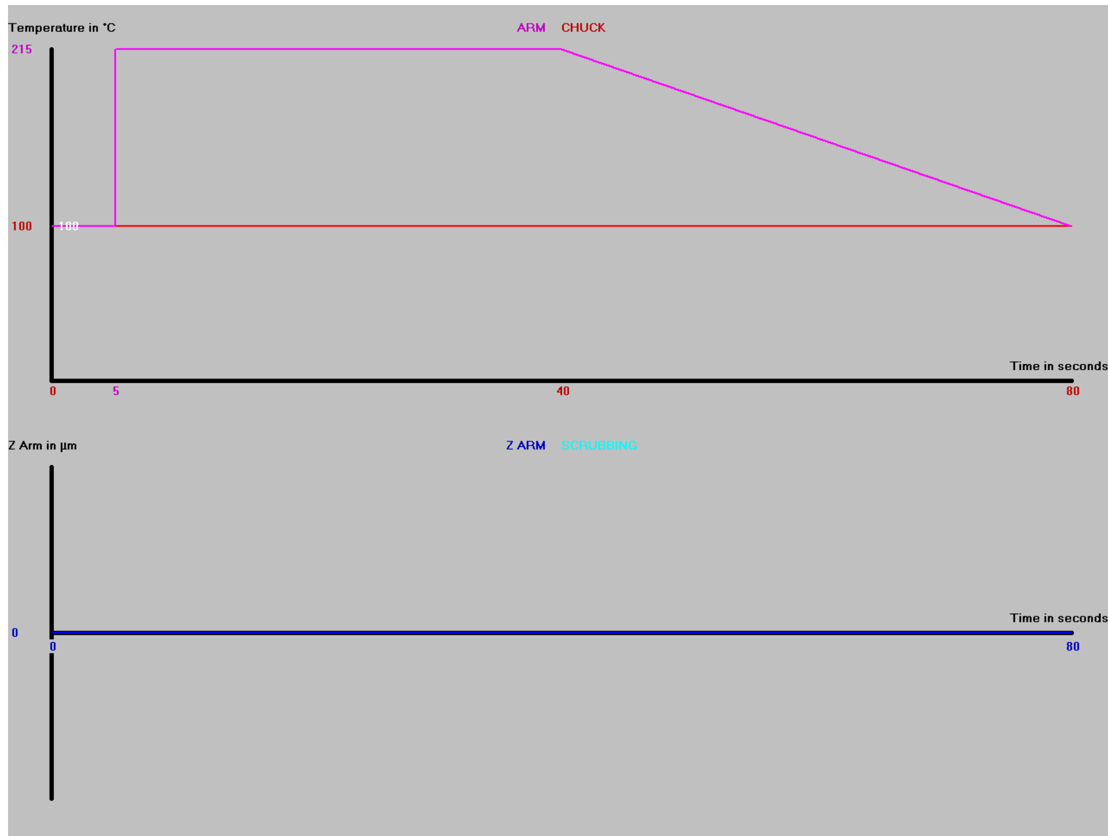


Figure 6.8 Flip chip bonding profile without bond force for 10 mm × 10 mm test chip assembly

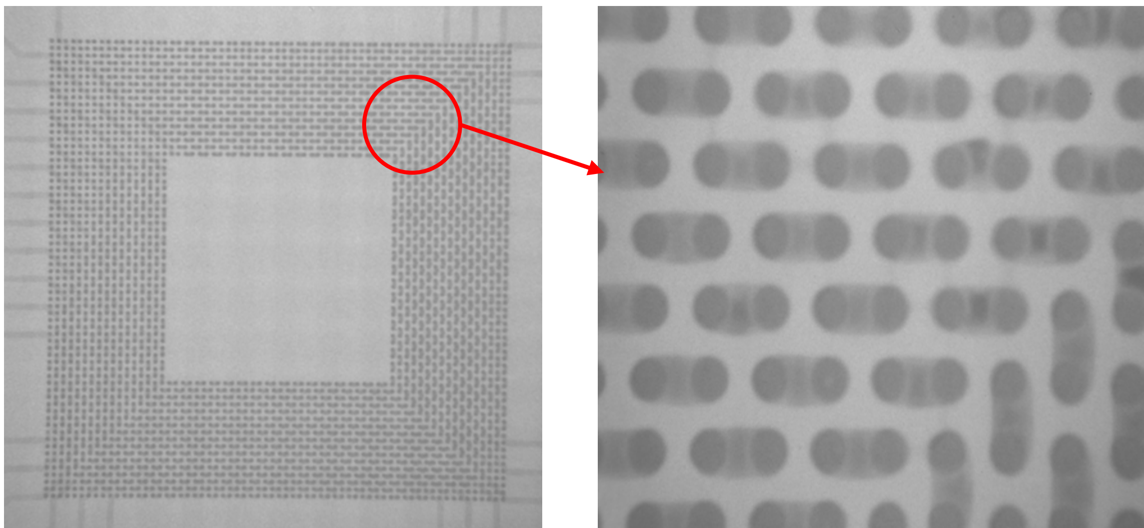


Figure 6.9 X-ray scanning micrograph of assembled 10 mm × 10 mm test chip without daisy chain short circuits

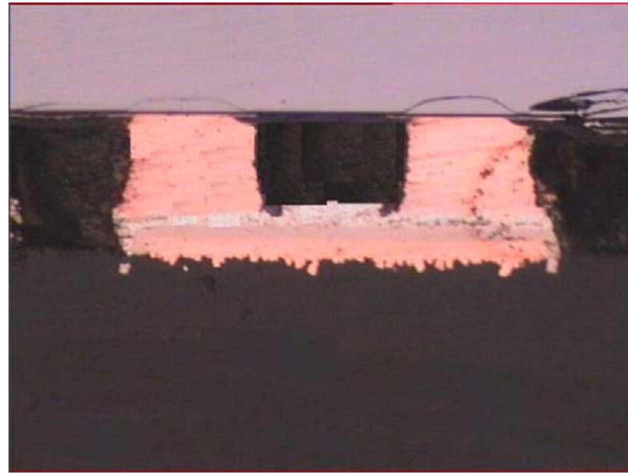


Figure 6.10 Cross sectional view of assembled 10 mm × 10 mm test chip without bond force

This solder bridging problem was overcome to some extent using Z-control. The optimized flip chip bonding profile with Z-control was shown in Figure 6.11. Results revealed that solder wettability was observed along the non-solder-mask-defined test board pads and few daisy chains were opened due to the force applied in the Z-direction to the solder in the liquid state. Hence the assembly process was carried out with previous conditions without bond force. This solder wettability along the pad traces can only be avoided completely by using solder mask defined test board pads. Figure 6.12 shows the BoN test demonstration on conventional board of CTE 18ppm/^{0}C. Because of the above problem test board for 20 mm × 20 mm dies were fabricated with solder mask defined test board pads.

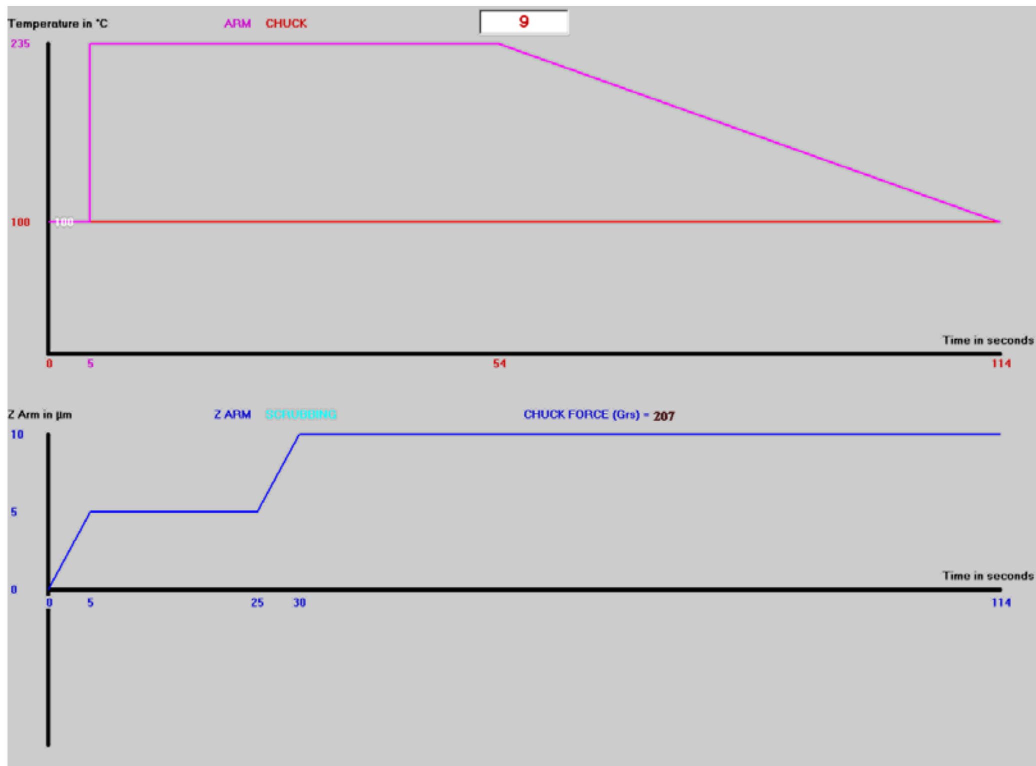


Figure 6.11 Flip chip bonding profile with z-control for 10 mm × 10 mm test chip assembly

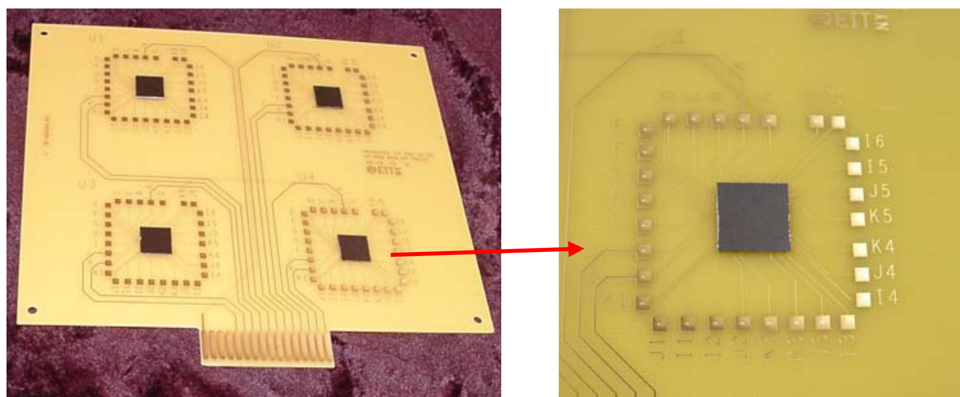


Figure 6.12 Bed of Nails test demonstration on conventional board (CTE 18ppm/ºC)

6.3.2 Assembly process optimization for 20 mm × 20 mm test chip

Similar to 10 mm × 10 mm test chip assembly, 20mmx20mm test chip with BoN interconnects were also assembled on test boards with solder mask defined (SMD) metal pads. Using the same optimization condition with force, assembly was carried at 235°C bonding temperature with 1 kg bonding force. The assembly profile is shown in Figure 6.13. X-ray scanning was used to check the quality of the assembled chip, which revealed that there was no short circuit in daisy chains along with no solder bridging between two interconnects. Figure 6.14 shows the X-ray micrograph of assembled test chip. The advantage of this 20 mm × 20 mm assembly when compared to 10mmx10mm assembly was that there was no solder bridge between two interconnects due to SMD metal pads. Figure 6.15 shows the 20 mm × 20 mm test demonstration on conventional board of CTE 10ppm/^{0}C.

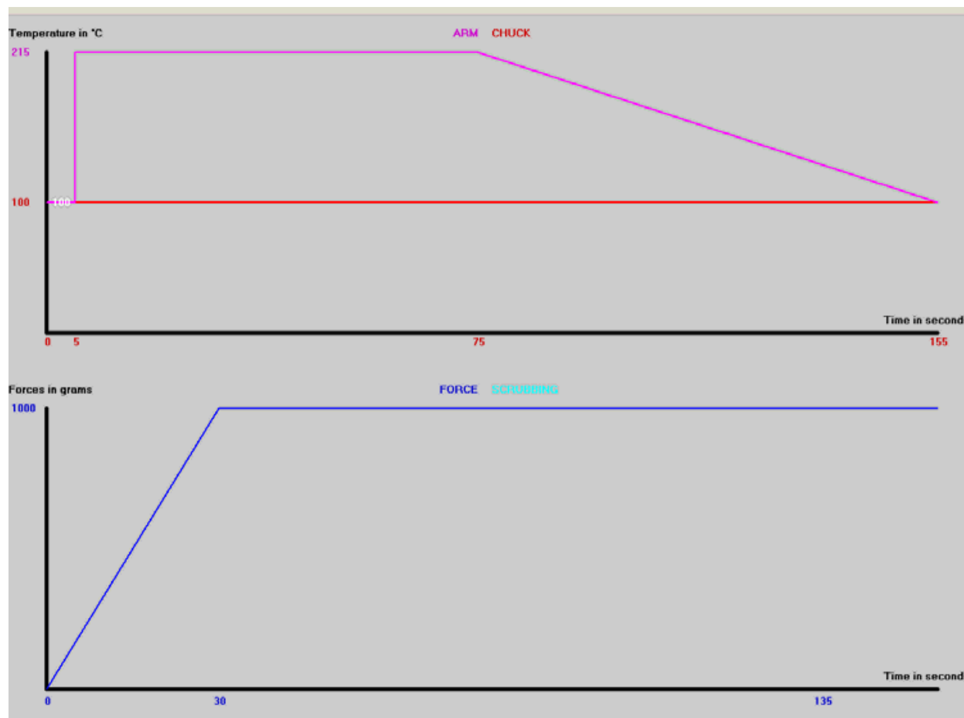


Figure 6.13 Flip chip bonding profile with bonding force for 20 mm × 20 mm test chip assembly

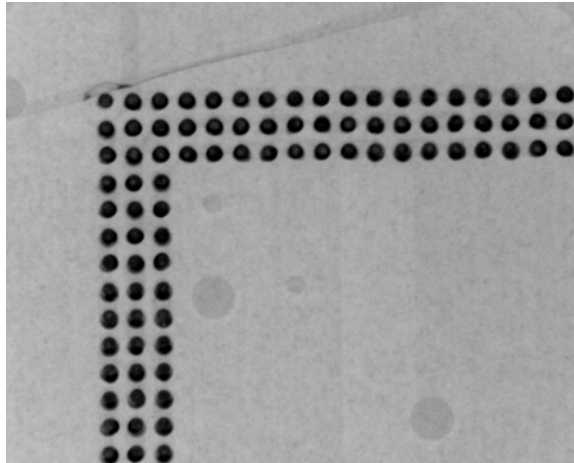


Figure 6.14 X-ray scanning micrograph of assembled 20 mm × 20 mm test chip without daisy chain short circuits and solder bridging

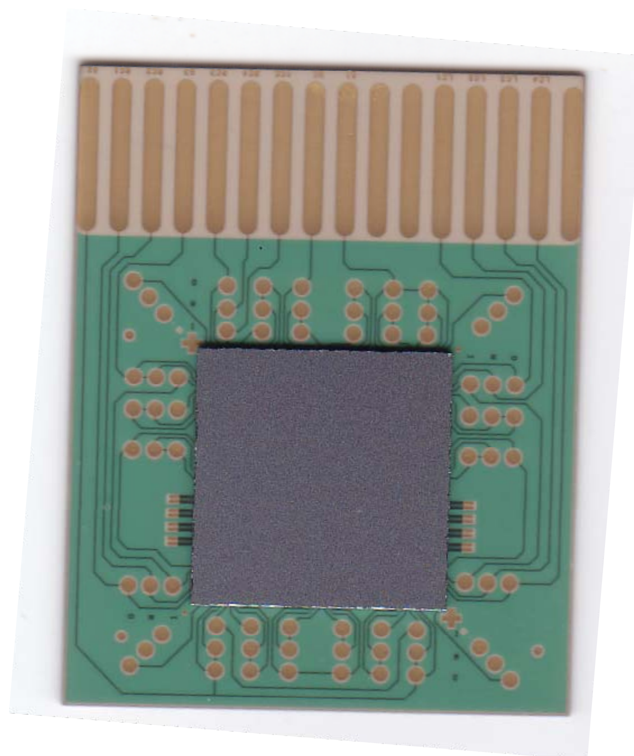


Figure 6.15 20 mm × 20 mm test chip demonstration on conventional board (CTE 10ppm/ºC)

6.4 Die shear test

The die shear test was done to the above assembled 10mmx10mm test dies to evaluate the shear strength and to investigate the wettability of the solder on the bond pads. Die shear tests were carried out on the Dage Series 4000 bond tester. Shear tests were carried out at 50µm shear height and 100µm/sec shear speed. Table 6.3 shows the parameters used in the die shear test. The average shear strength of 5 dies was 63 kg. Figure 6.16 shows the plot between shear force vs. time. The sheared surface revealed good solder wettability on the bond pads of PCB board and failure was observed in the solder region.

Table 6.3 Die shear test parameters

Cartridge	DS100Kg	Shearing Height (µm)	65
Shear speed(µm/s)	100	Die size (mmxmm)	10x10
Landing speed (µm/s)	180	Die shape	squire
Fallback	80%	Test load (Kg)	100

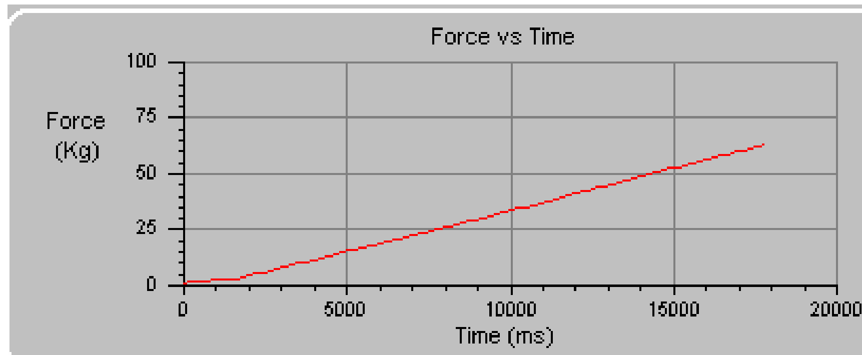


Figure 6.16 Die shear test result

6.5 Reliability

Thermal Cycling tests for the above filp chips on boards without underfill were done under temperature cycling at -40^{0}C to 100^{0}C. Figure 6.17 shows the temperature profile for TC test. Daisy-chain resistance measurements are taken at every 100 cycles to assess the reliability of interconnects. Any daisy-chain with resistance greater than 3 times the theoretical resistance value of that daisy-chain and/or open is considered as a failure. The theoretical resistance of each daisy chain was calculated using the following formula.

$$\text{Resistance } R = \frac{\rho L}{A}$$

ρ = Resistivity
L= Longitudinal length
A= Cross sectional area

The resistivity of the metals used in the calculation are 17.1, 69.3 and 150 mΩ-µm for copper, nickel and solder respectively.

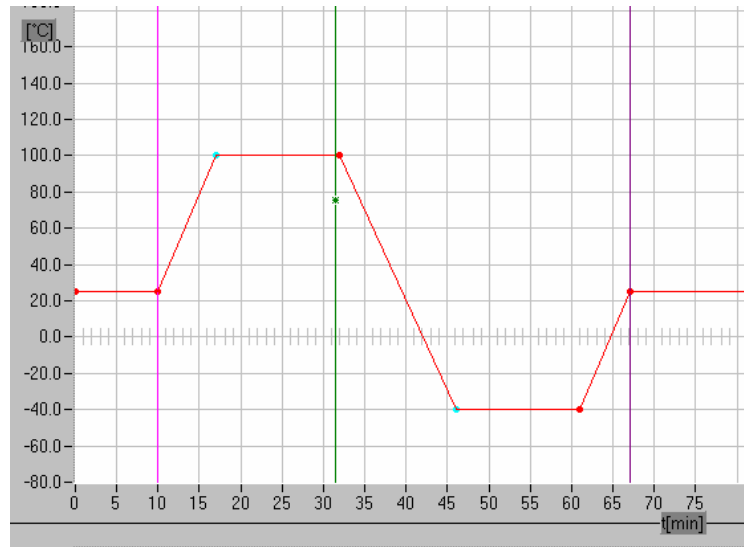


Figure 6.17 Temperature profile for thermal cycle test

In general, the solder interconnects were widely used in advanced packaging. Hence, the test vehicles were bench-marked with a 200μm pitch solder ball test vehicles of similar die size without underfill. It was observed the test vehicles with solder ball showed initial failures as early as 100-200 cycles whereas in the case of Bed of Nails interconnects, initial failures were observed at between 500-600 cycles. Table 6.4 shows the TC results obtained during thermal cycle testing. Results reveal that the BoN interconnects test vehicles are 2 times more reliable than solder ball test vehicles of similar die size without underfill.

Table 6.4 TC reliability test results

	100	**200**	**300**	**400**	**500**	**600**	**700**
No. of failures in solder ball with out underfill (200 μm pitch)	0/10	3/10	10/10	-	-	-	-
No. of failures in Bed of Nails with out underfill (100 μm pitch)	0/10	0/10	0/10	0/10	0/10	2/10	10/10

However, according to the JEDEC standards for the high performance devices packages, the interconnects required to pass 1000 cycles, but in some applications such as hand held devices only 600 cycles are needed [70]. Thus it was evident that the BoN interconnects were more reliable than the conventional solder interconnects.

6.5.1 Failure analysis

In order to understand the failure mechanisms, cross-sectional analysis was done using scanning electron microscopy (SEM). The cross sectional analysis of the failed interconnects revealed that most of the failures occurred due to the cracking in the bulk solder as evident in Figure 6.18. This is because the bulk solder is the weak region in the

BoN interconnect and it also may be due to the lesser solder volume between copper column and board because of the spreading of solder over the bond pads of test board. In a few other cases, the failures was observed due to the crack initiation in copper column at the BCB opening near chip side and BCB delamination on the chip side.

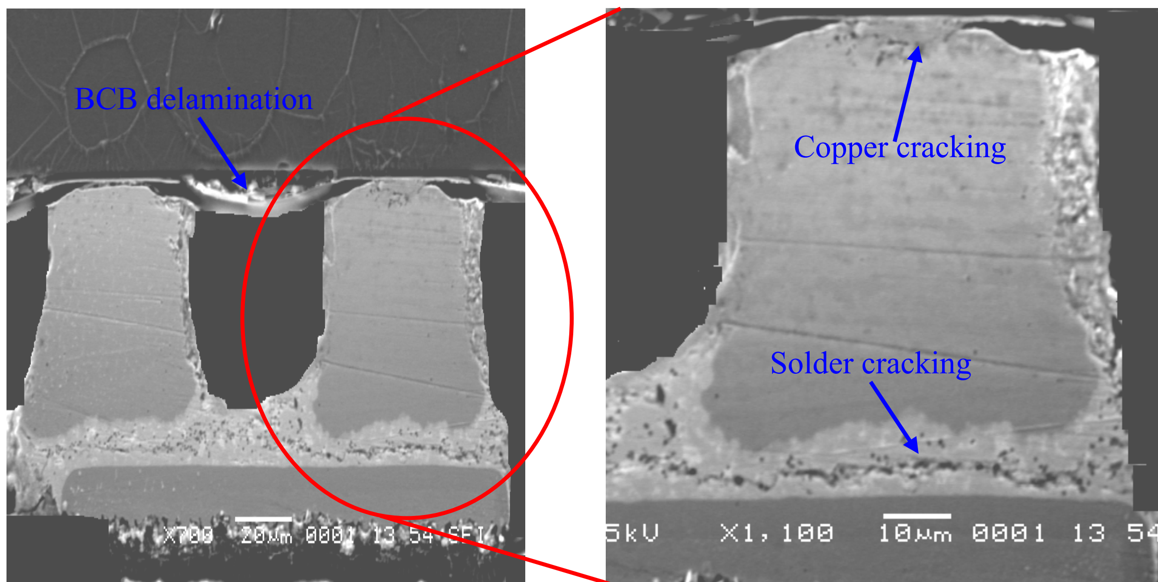


Figure 6.18 SEM photograph of Cross section of failed interconnect after TC test

The reliability of the BoN interconnects can be further improved to meet the JEDEC reliability standards by the following modifications.

1. The solder region failure can be controlled by using solder of better properties, the higher solder volume and by avoiding the solder spreading along the bond pads of test board using solder mask defined metal pad boards. Hence the strain on the solder will reduce and it will enhance fatigue life of interconnects.
2. Further increasing the copper column height to 100-120µm to reduce the strain on the solder region.

According to the fatigue life predictions using strain-based methods, thermal fatigue life is directly proportional to the creep strain range per cycle ($\Delta\varepsilon_{crp}$) as shown in the following Equation 1 [71].

$$N_f = \theta\ (\Delta\varepsilon_{crp})^{-\eta} \qquad (6.1)$$

Based on the modified strian relationship for interconnects applications, the strain on the interconnect is inversely proportional to the height of the interconnect as shown in the following Equation 2 [72].

$$\Delta\varepsilon = DNP * (\alpha_s - \alpha_c) * \Delta T / H \qquad (6.2)$$

where, $\Delta\varepsilon$ is strain on the interconnect, α is co-efficient of thermal expansion (ppm/ °C), ΔT is 140 °C (thermal cycling between -40 °C to 100 °C), H is interconnect stand-off height and DNP is maximum distance to the neutral point.

From Equations 6.1 and 6.2, it is understood that the fatigue life is proportional to interconnect stand-off height. Hence, further increasing the column height to 100-120µm will reduce the strain on the solder region and as well as will improve the reliability.

3. Thinning of the die.

In this work, conventional wafers of 720 µm thickness were used. Reducing the silicon die thickness will make the die more flexible to bear the stress and enhance the fatigue life. Therefore a die thickness of 300 µm is proposed and the process for the same can be carried out using a mechanical backgrinding.

4. Using low CTE boards.

According to Equation 6.2, the CTE difference between silicon die and board is directly proportional to the strain in the interconnects. From Equations 6.1 and 6.2, it is understood that the fatigue life is inversly proportional to CTE difference. Hence usage of low CTE boards can enhance the fatigue life. The CTE of the boards can be reduced to 10-12 ppm/^{0}C from the conventional 14-18 ppm/^{0}C by using advanced materials.

CHAPTER 7

CONCLUSION

The following are the conclusions of this study:

- A new technology named, Bed of nails (BoN) off-chip interconnects technology has been developed to meet the next-generation microelectronic packaging needs in terms of electrical, mechanical, assembly, environmental and cost requirements.
- BoN interconnect scheme was successfully demonstrated using a 10mm x 10mm test chip assembled on a conventional test boards.
- BoN interconnects fabrication process, which was based on photolithography and electroplating process, has been optimized and fabricated at a pitch of 100µm. This fabrication process was compatible to the conventional integrated circuit (IC) fabrication.
- Thick photoresist process to fabricate high aspect ratio (more than 2) BoN interconnect, has been optimized using JSR negative tone photoresist and the results showed near vertical sidewall profile with good reproducibility.
- Copper plating process was optimized to fill the 50µm diameter and 65µm depth vias and yield obtained was found to be high.
- Test chip with 50µm diameter, 65µm height and 100µm pitch BoN interconnects was assembled on PCB test board without underfill and reliability test showed promising results.

- This low cost BoN interconnects can be a potential candidate to meet some of the off-chip interconnect requirements of the next-generation microelectronic packaging.
- The process has been implemented on 8 inch wafer for mass fabrication using conventional wafer level process.

The following are recommendations for future work:

- To assess the reliability of 100µm height BoN interconnects, the test chips of 20 mm × 20 mm size with 100µm height BoN interconnects can be fabricated, assembled and subjected to thermal cycle testing.
- Test chip of 20 mm × 20 mm size with 36481 number of interconnects of 100µm height BoN interconnects in fully populated manner can be fabricated to improve the reliability.
- To assess the electrical performance, electrical testing is needed to be done to understand the electrical performance of Bed of Nails (BoN) interconnects.
- Bed of Nails (BoN) off-chip interconnects with different heights can be fabricated to obtain better reliability and to study the BoN height effect on their thermo-mechanical reliability.
- To avoid the problems faced during the copper plating, various plating techniques with different chemical additives can be studied for higher aspect ratios.
- Thinning of the wafer can be carried out using backgrinding to improve the reliability.
- Different types of materials can be used to improve the performance and thermo-mechanical reliability of the off-chip BoN interconnects.

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