DYNAMIC PERFORMANCE IMPROVEMENT IN BOOST AND BUCK-BOOST-DERIVED POWER ELECTRONIC CONVERTERS

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Summary

Classical boost and buck-boost converters and their derivatives are used in dc-dc switch-mode power supplies and in single-phase ac-dc power factor correction (PFC) applications. In dc-dc applications, the small-signal dynamic performance of these converters operating in continuous-conduction mode is slow due to the presence of a right-half plane (RHP) zero in their control-to-output transfer function. Their large-signal dynamic performance is also sluggish, a prime reason being the linear nature of controllers commonly used with these converters. The focus of this thesis is to analyze and propose solutions for mitigating and overcoming these dynamic performance problems.

The proposed solutions are obtained in the following two ways.

1. By enhancing the converter design and by modifications in the employed controller
2. By modifying the converter topology.

Among the solutions related to the first approach, to begin with, it is shown that the small-signal dynamic performance problem of a boost converter is mitigated by appropriate selection of boost inductance. The pros and cons of the proposed design are discussed.

Following the first approach, the performance of boost converter is investigated with linear-PI controller, gain-scheduled PI controller (GSPI), and fuzzy logic controller (FLC). Linear-PI controller offers a better small-signal performance at the designed operating point than those offered by GSPI and FLC. For large-signal transients, FLC offers a dynamic performance better than that offered by the linear-PI controller. For explaining this transient response offered by FLC, the structure of

several FLCs used in power-converter-control-applications (PCCA) in the past are analyzed. It is shown that most of these FLCs can be approximated by a single-input-single-output nonlinearity. The resulting 'Non-linear Function Controller' (NLFC) explains the rationale behind the good large-signal performance offered by FLCs. Besides, the design of NLFC (and indeed FLCs) to obtain good small-signal performance becomes logical. The proposed NLFC can replace FLCs in PCCA. A Non-Linear PI Controller (type of NLFC) is designed and tested with a boost converter to verify the advantages offered by NLFCs.

Another solution to dynamic response problem that falls under the second category relates to the novel 'tri-state' class of boost and buck-boost-derived converters proposed and analyzed in detail in this thesis. These converters have an extra-degree of control-freedom in the form of an 'inductor-free-wheeling' interval, using which the dynamic response problem due to RHP zero is avoided. Excellent improvement in dynamic performance over those of the classical counterparts is verified experimentally.

The additional control-freedom of tri-state boost converter is exploited by three novel control methods, namely,

1. 'Constant-D_o' control method
2. Direct dual-mode control (DDMC) method
3. Indirect dual-mode control (IDMC) method.

While the 'constant-D_o' control method focuses primarily on improving the dynamic performance, the multi-variable IDMC and DDMC schemes improve both the dynamic and steady-state (i.e. operating efficiency) performances of the converter.

A procedure for designing power and control components of a tri-state boost converter employing DMC scheme is also given.

Tri-state converters, due to their additional control-freedom constitute potential candidates for application as PFC rectifiers that have to meet multiple objectives, namely, drawing a sinusoidal input current at unity power factor, delivering a well-regulated dc voltage, and ensuring fast dynamic response. A study on the application of tri-state converters in PFC applications is presented. A simple 'dual-mode' control method for a PFC rectifier employing cascade buck-boost (CBB) converter (a tri-state converter) is proposed. This control method exploits the extra control-freedom in meeting the PFC goals. The anticipated good transient and steady-state performances are verified experimentally. A qualitative comparison of CBB-PFC with popular PFC converters is also given.

The report concludes with an identification of future work related to the tri-state class of power converters.

Keywords: boost, buck-boost, cascade buck-boost, controller, fuzzy logic controller non-linear function controller, non-linear PI-controller, power converter, Tri-state.

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CHAPTER 1

INTRODUCTION

1.0 Background

Power electronic converters are used to control and condition the flow of electrical energy between two systems. The insertion of a power electronic converter between the two systems becomes essential to achieve compatibility between them and to achieve important performance objectives. For example, the up-stream system could be the ac mains power supply that requires the load to draw a current of low harmonic content in phase with the ac voltage. On the other hand, the down-stream system or load may require a well-regulated supply voltage having fast-dynamic response characteristics to meet sudden fluctuations in power demand. The power electronic converter inserted in such a case aims at meeting both the load-side and the line-side requirements.

From microchips requiring a few milli-watts of power to Maglev (magnetic levitation) trains and high-voltage dc-transmission (HVDC) systems where several gigawatts of power is processed, power electronic converters find applications in almost all areas of utilization of electrical energy. Historically, these converters have been classified depending on the nature of the systems interconnected by them. The broad classification is as below.

1. Dc-dc converters.
2. Ac-dc converters
3. Dc-ac converters
4. Ac-ac converters

In the past, dc-dc converters, popularly known as ‘choppers’ were broadly classified based on the quadrants of operation on load voltage-current plane. These choppers are used in high power applications e.g. electric traction. A class of dc-dc converters used in power levels below 1 kW is Switch-Mode Power Supplies (SMPS). Being the backbone of many consumer electronic products, SMPS constitute a multiple-billion-dollar industry. Considering the importance of SMPS, in this thesis, certain important problems associated with popular SMPS are investigated.

The ac-dc converters popularly known as ‘rectifiers’ are primarily used as front-end converters. They can be built using uncontrolled (diodes), fully-controlled (MOSFETs, IGBTs) or semi-controlled (thyristors) switches. In the later part of this thesis, a member belonging to this class of power converters is described in detail.

The ‘dc-ac’ converters, popularly known as ‘inverters’ find applications in uninterrupted power supplies (UPS), high-performance ac drives, and in line-commutated converters as in HVDC transmissions. In this thesis, this class of power converters is not considered for investigation.

Applications of ac-ac converters are limited to ac-voltage controllers used in lamp dimmers and cyclo-converters used in high power drives. In this thesis, this class of power converters is also not considered for investigation.

1.1 Importance and Requirements of DC-DC Converters

Many a time, dc-dc converters as SMPS have an unregulated input voltage. Depending on the requirements of the load, the SMPS may either step-up or step-down the input voltage to produce a well-regulated load voltage. Based on the

relative magnitudes of supply and load voltages, SMPS primarily fall under three broad categories listed below.

- *Step-up* converter in which magnitude of load voltage is always more than that of the supply voltage
- *Step-down* converter in which magnitude of load voltage is always less than that of the supply voltage
- *Step-up/down* converter in which magnitude of load voltage may be either higher or lower than that of the supply voltage.

Some popular dc-dc converters [2] and their classifications are given below.

Buck and buck^2 converters – step-down

Boost converter – step-up

Buck-boost and Cuk converters- step-up/down (with polarity reversal)

Cascade buck-boost and Sepic converters – step-up/down

In some applications, where galvanic isolation of line and load sides is essential, isolated versions of the above three categories of converters are used. Forward and flyback converters are popular examples.

The design of SMPS is dictated by both steady-state and transient-state requirements of the load. This can be explained as follows.

The most important steady-state requirement in any power electronic converter is that the converter should have a high operating efficiency. Primarily, the parasitic elements in the converter are responsible for loss of power. Converters having low operating efficiencies need large heat sinks. Thus, operating efficiency of the converter has implications on both the size and operating cost of the converter.

Another important steady-state requirement is the load voltage regulation. In most of the cases, the load requires a well-regulated voltage of desired magnitude. Besides, the switching ripple in the load voltage is desired to be kept low. In some applications such as in a SMPS feeding a mother board in the PC, extremely tight steady-state regulation of load voltage is essential. This requirement reflects in the selection of appropriate converter topology, size and rating of filter components, and control method employed.

One more steady-state specification that is gaining ground is related to electro-magnetic interference (EMI). Due to switching nature of the power converter, the current drawn from the supply has large ripple content. The high frequency content of the current interferes with the nearby communication channels. Several international standards restrict the level of high frequency current drawn by the SMPS from the mains. Many times, to meet the standards, additional EMI filters and components are added making the converter bulkier and more expensive.

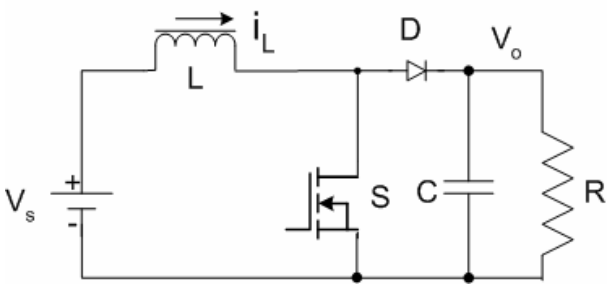
Among the several transient-state load requirements, permissible overshoots and dips in the converter states (inductor current, output voltage), time taken by the load voltage to recover after a sudden disturbance, and hold-up time after a failure in the supply voltage (of SMPS) are of prime importance. Device voltage stress and current stress limits and saturation of magnetic components are important reasons behind specifications limiting the voltage and current overshoots. Another important transient-state consideration is the recovery time of the load voltage after a step disturbance. Most of the applications demand a fast recovery of load voltage. The dynamics of the converter and hence the recovery of output voltage once again

depends on the selected converter topology, size and count of filter components employed, and control methods employed.

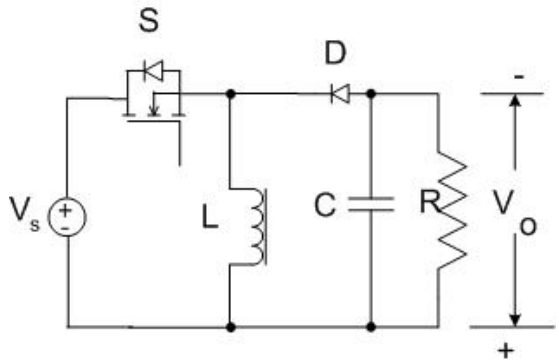
From the above discussion, the importance of SMPS and the associated design challenges may be obvious. Thus, in this thesis, certain converters belonging to step-up and step-up/down category of SMPS are considered for investigation.

1.2 Boost and Buck-Boost-Derived DC-DC Converters

Single-switch boost and buck-boost converters shown in Fig. 1.1 belong to step-up and step-up/down category of non-isolated dc-dc converters [1], [2]. These converters find applications in on-board power supplies.



(a)



(b)

Fig. 1.1 Circuit diagrams (a) Classical single-switch boost converter (b) Classical single-switch buck-boost converter

The voltage gains of the boost and buck-boost converters are given below.

$$\textit{For boost (step-up) converter: Voltage gain} = \frac{V_o}{V_s} = \frac{1}{1-\mathrm{D}} \qquad (1.1)$$

$$\textit{For buck-boost (Step-up/down) converter: Voltage gain} = -\frac{\mathrm{D}}{1-\mathrm{D}} \qquad (1.2)$$

In (1.1) and (1.2), V_o is the load voltage, V_s is the supply voltage and D represents the duty ratio of the switch S employed in the converter.

Several books on power electronics [1], [2] discuss the basic operation and design of these converters and they may be referred to understanding the operation, if necessary. The prime objective of this thesis is to study the various transient-response problems associated with these converters and their derived versions (e.g. flyback, cascade buck-boost converter). This section introduces the dynamic response problems associated with these converters when used in dc-dc applications.

1.2.1 Small-signal Dynamic Response Problem due to Right-Half-Plane (RHP) Zero

Boost, buck-boost, flyback, cascade-buck-boost converters, and their quasi-resonant versions are non-minimal phase systems. Systems with small-signal transfer functions having a pole and/or zero on the right-half of the complex frequency plane are called non-minimal phase systems [91]. The small-signal control-to-output transfer function of these converters when operating in continuous-conduction mode (CCM) presents a characteristic right-half-plane (RHP) zero, which poses a great challenge to designers in obtaining a good small-signal bandwidth. For example, the control-to-output transfer-function of a classical single-switch boost converter shown in Fig. 1.1(a) (obtained by state-space averaging and linearization [3]) is given by

$$\frac{V_o(s)}{D(s)} = \frac{\mathrm{V_s}}{(1-D)^2} \frac{\left(1 - s\frac{L}{R(1-D)^2}\right)}{1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}}, \qquad (1.3)$$

In (1.3) L is the boost inductance, C is the output capacitance, and R is the load resistance. From (1.3), it may be seen that the location of RHP zero is not fixed but changes with changes in operating point i.e. with input voltage and load resistance. This movement of RHP zero in the complex s-plane complicates the task of designing a good controller. Typically, the overall closed-loop bandwidth is reduced to values as low as $1/30^{th}$ of the switching frequency [12]. As a result, the small-signal dynamic response of the converter is sluggish.

It must be noted that the presence of RHP zero in the small-signal control-to-output transfer function is not limited to boost and buck-boost family of converters alone. Even Cuk converter has a double complex-right-half-plane zero in its control transfer function. However, the problem in Cuk converter is not investigated in this thesis.

1.2.2 Large-Signal Dynamic Response Problem

Another problem that is often faced not only in boost and buck-boost-derived converters but also in many other converters is related to the large-signal dynamic response of the converter. During large-signal transients i.e. when the converter undergoes a major change in operating point on account of a change in the load or in the input voltage, the settling time to reach the desired state depends primarily on two factors, namely

1. Size of energy storage elements and
2. Control technique employed.

The size of energy storage elements is generally dictated by the rated operating conditions of the converter. The larger the size of the elements, the more sluggish is the response.

Often, the control method employed compounds the large-signal dynamic response problem of the converter. This can be explained as follows. Dc-dc power converters are non-linear in nature. Traditionally, the design of controller for such a system is based on small-signal frequency domain analysis. In order to design a controller for a non-linear plant like a power converter, to begin with, a mathematical model of the power converter is obtained. Many papers [3]-[11] found in literature explain several ways of getting the mathematical model of switching converters. Among them, state-space averaging and linearization technique [3] is widely used in obtaining a linear-time-invariant (LTI) model of the plant. The model obtained so is a small-signal model, whose applicability is limited to a small region around the converter's operating point. This is due to linearization at the operating point during the modeling process. As a result, the model parameters vary significantly when the operating point shifts.

In general, after obtaining the mathematical model, classical control tools like Bode plots and Nyquist plot are used to design a controller that optimizes the dynamic performance of the converter at the selected operating point. The controller designed accordingly will generally offer a reasonably good small-signal response (measured in terms of settling time and transient overshoot) at the designed operating point. However, for large disturbances, the response of the converter with the controller will be sluggish, often associated with large overshoots or undershoots due to the inability of controller in handling large-signal transient response efficiently.

1.3 Focus of the Thesis

The focus of this thesis is to investigate into the dynamic response problems associated with boost and buck-boost converters and topologies derived from them. Solutions to overcome or mitigate these problems are proposed. The proposed solutions broadly fall under two categories, namely

1. Mitigation of dynamic response problems by enhancements in converter design and control techniques
2. Modification of the existing converter topology to overcome the problem.

The issues considered for investigation and contributions of the thesis are explained in the following sub-sections.

1.3.1 Issues Studied

The following issues were investigated in this dissertation.

1. Mitigation of dynamic performance problems by enhancements in converter design and control techniques:

a. Mitigation of small-signal dynamic response problem by enhanced design of converter

Mitigation of small-signal dynamic response problem due to RHP zero occurring in the control transfer function of a classical boost converter operating in continuous-conduction mode (CCM) by appropriate selection of filter elements was investigated. The pros and cons of such a design were brought out.

b. Mitigation of small-signal dynamic response problem by enhanced design of controllers

With an aim to achieve marginal improvement, the small-signal performance of the boost converter was investigated with several control techniques namely

linear-PI controller, gain-scheduled PI controller, and fuzzy logic controller (FLC).The advantages and disadvantages of each of these methods were brought out.

c. Mitigation of large-signal dynamic response problem by enhanced design of controllers

An in-depth analysis of large-signal performance improvement in boost and buck-boost-based converters using fuzzy logic controller (FLC) was carried out. Based on the analysis, a simple and inexpensive Non-linear Function Controller (NLFC) that replaces two-input FLCs of the type used typically in power-converter-control applications was proposed.

2. Modification of the existing converter topology to overcome the dynamic response problem:

A new class of dc-dc converters named as '**tri-state family of converters,**' derived from the boost and buck-boost family of dc-dc converters was proposed. The tri-state converter avoids the RHP zero in its control transfer function resulting in improvement in dynamic performance. The 'tri-state' converters were studied in detail for improvement in steady-state and dynamic performance.

Large-signal dynamic response of tri-state class of power converters for disturbances of varying magnitudes was also studied.

Application of 'tri-state concept' in single-phase ac-dc power factor correction (PFC) rectifiers:

One of the key applications of boost and buck-boost-derived converters is in single-phase ac-dc PFC rectifiers. A few members belonging to the 'tri-state'

family of converters introduced in this thesis were investigated for applications as PFC rectifiers.

1.3.2 Thesis Contributions

The major contributions of the thesis are as follows.

1. Aimed at achieving a marginal improvement, the dynamic response problem in dc-dc boost power converter has been investigated with locally-optimized PI controllers, gain-scheduled PI controller (GSPI), and two-input fuzzy-logic controllers (FLCs). The pros and cons of each of these control techniques are clearly brought out.

2. A simple and inexpensive non-linear function controller (NLFC) that approximates complex two-input fuzzy logic controllers (FLCs) of the type commonly used in power-converter-control applications is proposed. Besides explaining the good large-signal transient response that is typically obtained using FLCs in power converters, the NLFC helps in understanding and designing FLCs to offer good small-signal transients. A stability analysis of the proposed NLFC is also presented. This simplification of two-input FLC into NLFC is used to question the very need of FLCs in power converter control applications.

3. A novel ‘tri-state’ class of boost and buck-boost-derived converters with an additional degree of control-freedom in the form of an ‘inductor-free-wheeling interval’ is proposed. The additional degree of control-freedom helps in avoiding the small-signal dynamic response problem due to the presence of RHP zero in the control transfer function of the converter.

4. Three different control methods that effectively exploit the control freedom offered by 'tri-state' boost converter to achieve good steady-state and transient performance are proposed. They are

   a. Constant-D_o control method

   b. Direct dual-mode control method

   c. Indirect dual-mode control method.

   In (a), D_o refers to the duty ratio of the interval during which the output capacitor of the converter is charged.

5. A novel dual-mode control method that meets the contradictory multiple-steady-state goals of achieving sinusoidal input current while providing a tightly regulated output voltage in a single-phase ac-dc PFC rectifier employing cascade-buck-boost converter is proposed. The dual-mode control method uses the 'Tri-state' concept proposed in this thesis in achieving the multiple goals. The control method also de-couples the output voltage control loop from the often-slow input-current-reference generator, resulting in excellent output voltage dynamic response.

1.4 Thesis Organization

The thesis consists of five major divisions, namely div. 1-5.

Div. 1: Literature survey

Chapter 2 falls under this division. This chapter explains in detail the dynamic response problem in boost and buck-boost-derived dc-dc and converters. A literature

survey on the techniques available to overcome or mitigate these problems is also given.

Div. 2: Mitigation of dynamic response problem by enhanced converter design

A part of **Chapter 3** falls under this division. In this chapter, mitigation of small-signal dynamic response problem in boost dc-dc converter by choosing appropriate value of boost inductance is discussed.

Div. 3: Mitigation of dynamic response problem by enhanced controller design

Chapters 3 and 4 come under this division. Dynamic performance offered in a dc-dc boost power converter by several controllers such as PI-controller, fuzzy logic controller, non-linear function controller (NLFC), non-linear PI controller (NPIC), and gain-scheduled PI controller is investigated in these chapters. The strengths and drawbacks of the various control techniques are clearly brought out.

Div. 4: Tri-state class of converters

Chapters 5 to 7 come under this division. **Chapter 5** introduces and discusses in detail the novel 'tri-state' class of boost and buck-boost-derived converters that has an extra degree of control-freedom. Simulation and experimental results demonstrating the steady-state and dynamic performances of tri-state boost and tri-state flyback converters (both implementing a simple 'constant-D_o' control method) are presented. Comparison with classical boost and classical flyback converter is also done.

Chapter 6 introduces the need for implementing multi-variable control techniques with tri-state class of converters and proposes two variations of a multi-variable 'Dual-Mode Control (DMC)' scheme. These schemes aim to improve the

steady-state (operating efficiency) and dynamic-state performance of tri-state class of converters by properly exploiting their extra degree of control-freedom. Simulation and experimental results demonstrating the excellent dynamic and steady-state characteristics of the tri-state boost converter under DMC schemes over those under 'constant-D_o' control scheme are presented and discussed.

The dynamic and steady-state performances of the tri-state converters under DMC schemes are closely inter-related and in turn decide the size and rating of power components and also the design of feedback controllers. **Chapter 7** investigates in greater detail the trade-offs involved in the design of DMC-based tri-state boost converter and presents a systematic design procedure for selecting the power and control components of the converter. An example design is presented and the design is validated through simulations and experiments.

Div. 5: Application of tri-state class of converters in single-phase ac-dc power factor correction (PFC)

Chapter 8 falls under this division. In this chapter, the application of tri-state converters in PFC is investigated. A simple and effective 'dual-mode' control method that achieves the control goals of unity-power-factor rectifiers based on cascade buck-boost (CBB) converter is proposed. The theoretical analysis, choice of circuit elements, and the applicable range of operating conditions of the proposed control scheme are presented. Excellent steady-state and transient performance of the converter are demonstrated through simulation and experimental results.

Chapter 9 presents the thesis conclusions.

CHAPTER 2

LITERATURE SURVEY OF SOLUTIONS TO DYNAMIC RESPONSE PROBLEMS OF BOOST AND BUCK-BOOST-DERIVED DC-DC POWER CONVERTERS

2.0 Introduction

In this chapter, the dynamic problems associated with boost and buck-boost-derived power converters that were introduced in Chapter 1 are explained in detail. A detailed literature survey on the solutions available to these problems is also presented. The pros and cons of the various solutions are briefly discussed. A literature survey on single-phase power factor correction, one of the popular applications of boost and buck-boost converter has also been done. As the prime focus of this thesis is to propose solutions to dynamic response problems of boost and buck-boost converters in dc-dc applications, the literature survey on single-phase ac-dc converters is included in appendix D.

2.1 Small-Signal Dynamic Response Problem due to RHP Zero

As mentioned in Chapter 1, the small-signal control-to-output transfer function of boost, buck-boost, and flyback converters and their quasi-resonant versions (operating in CCM) present a RHP zero. The presence of RHP zero prevents achievement of good closed-loop bandwidth resulting in slow dynamic response. In this section, the dynamic response problem due to the presence of RHP zero is

explained in detail. Following this, a few solutions available in literature are discussed. For the sake of simplicity, the problem is explained taking the dc-dc boost converter as an example. Similar arguments can be made for buck-boost converter and its derived versions.

2.1.1 Presence of RHP Zero and its Effect on Frequency and Time Domain Response of the Converter

The small-signal control-to-output transfer functions of single-switch boost (repetition of (1.3)) and buck-boost converters (operating in continuous-conduction mode CCM) obtained by state-space averaging and linearization method [3] are given below.

$$\textit{Boost converter: } \frac{V_o(s)}{D(s)} = \frac{\mathrm{V_s}}{(1-D)^2} \frac{\left(1 - s\dfrac{L}{R(1-D)^2}\right)}{1 + s\dfrac{L}{R(1-D)^2} + s^2\dfrac{LC}{(1-D)^2}} \tag{2.1}$$

$$\textit{Buck-boost converter: } \frac{V_o(s)}{D(s)} = -\frac{\mathrm{V_s}}{(1-D)^2} \frac{\left(1 - sD\dfrac{L}{R(1-D)^2}\right)}{1 + s\dfrac{L}{R(1-D)^2} + s^2\dfrac{LC}{(1-D)^2}} \tag{2.2}$$

Here V_s is the supply voltage, D is the operating duty ratio, V_o is the average output voltage, L is the filter inductance, C is the output capacitance, and R is the load resistance. As mentioned in Chapter 1, it may be noticed from (2.1) and (2.2) that the location of RHP zero on the complex s-plane varies with changes in operating point of the converter, thereby complicating the design of controllers. In this sub-section, the time-domain and frequency-domain effects of RHP zero in the boost converter operating in CCM are explained in detail. For the purpose of explanation, let us consider an ideal boost converter (Fig. 1.1) having the following specifications:

L = 278 μH, C = 540 μF, V_s = 12.5 V, V_o = 25 V, R = 12.5 Ω, F_s = 50 kHz, where F_s is the switching frequency.

For the boost converter under consideration, at the above-specified operating conditions, the value of D can be verified to be 0.5 using (1.1). The control-to-output transfer function obtained by state-space averaging and linearization can be written using (2.1). The corresponding Bode plot is shown in Fig. 2.1.

From Fig. 2.1, it may be seen that at a frequency of about 205 Hz, the boost converter has a set of complex poles which results in the phase rolling down from 0 degrees to -180 degrees and the slope of the magnitude (gain) changing from 0 dB/decade to -40 dB/decade. The presence of RHP zero at about 1789 Hz may be understood by the slope of gain increasing from -40 dB/decade to -20 dB/decade and the phase rolling down towards -270 degrees.

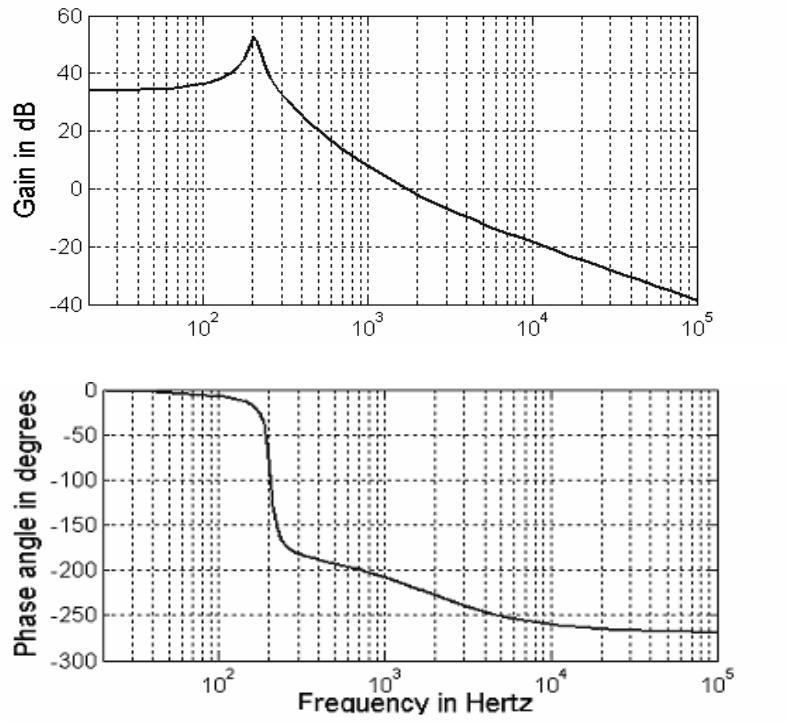


Fig. 2.1. Bode plot of Control-to-output transfer function of a classical boost converter at V_s = 12.5 V, V_o = 25 V, and R = 12.5 Ω.

The presence of RHP zero makes it difficult to realize a compensator that can ensure a positive phase margin while achieving a small-signal bandwidth above the RHP-zero frequency. Although an LHP zero provided by the compensator at frequencies higher than the RHP zero's frequency improves the phase response, it makes the gain slope flat (0 dB/decade), which is undesirable. Any LHP pole provided by the compensator worsens the phase margin besides reducing the slope of the gain to -40 dB/decade. Unlike an LHP zero, the RHP zero cannot be compensated by using a RHP pole as it may lead to an unstable system. Thus, in general, the closed-loop bandwidth is limited to frequencies less than the RHP-zero frequency.

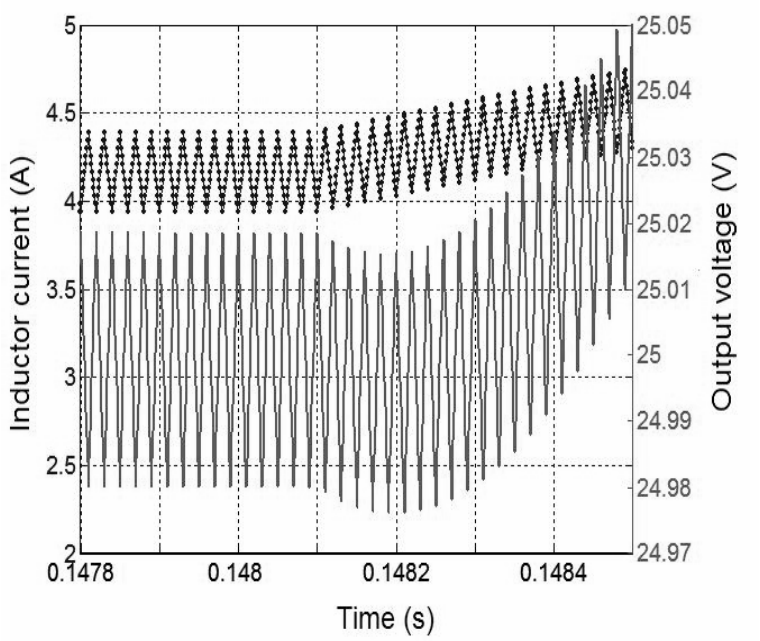


Fig. 2.2. Inductor current (upper) and output voltage (lower) waveforms of classical boost converter for a step increase in duty ratio from D = 0.5 to 0.51 at V_s = 12.5 V, V_o = 25 V, I_o = 2 A.

The effect due to the RHP zero can be explained in time domain as follows. An increase in control input (duty ratio of S in Fig. 1.1) initiated by a dip in the output voltage causes an increased output-capacitor-discharge-time. This results in the output voltage dipping even further until the inductor current builds up to recharge the

capacitor. This is demonstrated in Fig.2.2 which shows the response of the boost converter for a step change in duty ratio. The initial dip observed in the output voltage shows the presence of RHP zero. Although this voltage dip is not an important concern, the control complexity that this (RHP zero) introduces is the real problem. Any attempt to speed up the control by a significant increase in the closed-loop bandwidth will affect the system stability.

2.1.2 Solutions Available in Literature for RHP Zero Problem

Operating the boost (or buck-boost) converter in DCM is often suggested as a popular solution for 'eliminating' the RHP zero effect. In DCM, one of the two system poles is shifted to a high frequency. As a result, the system essentially behaves as a first order system exhibiting fast dynamic response. However, operations in DCM will increase the peak and ripple currents in the components. This in turn will increase the current ratings of the devices which has an impact on the cost of the converter. Besides this, the increased RMS current will also result in higher losses due to system parasitics and will result in a low overall efficiency. It is interesting to know that references [6] and [15] explain that in DCM operation, the RHP zero is not eliminated but shifted to a much higher frequency closer to the switching frequency of the converter. As the closed-loop bandwidth realized in most cases is below the Nyquist frequency (half the switching frequency), the presence of RHP zero at high frequencies has negligible effect on the system dynamics.

The method proposed in [12] shows that leading-edge modulation of output voltage can eliminate this RHP zero, provided the ESR (Equivalent Series Resistance) of the output capacitor is above a minimum value. Such a large ESR value will lead to

high ripple voltage, which is an important consideration. Additional series resistance may even have to be added to satisfy the ESR condition. Furthermore, the compensation requires accurate knowledge of the ESR value, which is temperature sensitive and hence difficult to measure.

Reference [13] suggests three techniques - reducing the inductor value, reducing the switching frequency, and operating in the discontinuous-conduction mode (DCM). Reducing the inductor value does not eliminate the RHP zero but pushes it farther into the right-half-plane, thus reducing its effect on the system response. With a decrease either in the inductor value or in the switching frequency, the ripple and peak currents in the components will increase considerably, thereby increasing the output filter requirement. The disadvantages of operating in DCM have been explained earlier. This does not address the RHP zero problem in the CCM operation.

Reference [14] models the RHP zero as a time delay and utilizes a 'predictor', which is designed such that when operated with the boost converter the RHP zero is eliminated. However the work does not address the practical problems in implementing such a scheme. For example, the predictor model used is based on small-signal modeling and may not be able to compensate fully the actual boost operation.

2.2 Large-Signal Dynamic Response Problem

The large-signal dynamic response problem in boost and buck-boost power converters has been explained briefly in Chapter 1. Chapter 1 mentioned two reasons that are primarily responsible for sluggish large-signal dynamic operation. Among them, sluggish large-signal dynamic operation on account of size of filter elements

employed is not considered for investigation in this thesis. The reason is that the size of the filter elements is dictated by rated operating conditions of the converter and other design specifications such as hold-up time. Any reduction in the filter elements in an attempt to get faster dynamic will increase the device stresses and may also violate the design specifications. Thus, in this section, the compounding of dynamic response problem by controllers employed is alone studied. Following this, popular control techniques available in literature for improving the large-signal dynamic response are discussed.

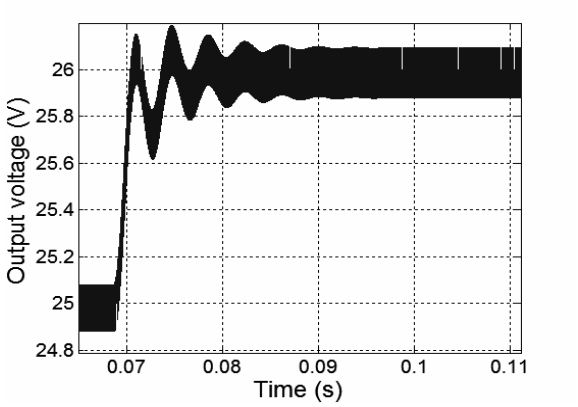
2.2.1 Problems with Classical Controllers in Handling Transient Disturbances

It was mentioned in Chapter 1 that classical linear controllers are strongly dependent on the converter model. This dependency results in two limitations of the controllers listed below.

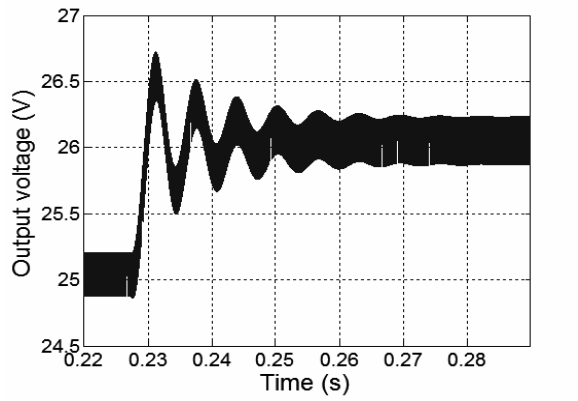
1. The controller does not offer good small-signal transient at an operating point different from the design operating point.
2. The controller does not offer a good large-signal transient.

As the converter's model (parameters) changes significantly with changes in operating point (2.1), a linear controller which is design-optimized for small-signal transients at one operating point many times does not offer the desired small-signal performance at a different operating point. Fig 2.3 shows the simulated responses of a boost converter ($L = 275\ \mu H$, $C = 540\ \mu F$, *ESR of* $L = 0.15\ \Omega$, *ESR of* $C = 0.05\ \Omega$, and $R = 25\ \Omega$) for a small step change in reference voltage from 25 V to 26 V at two different input voltages, namely $V_s = 15\ V$ (Fig. 2.3 (a)) and $V_s = 10\ V$ (Fig. 2.3(b)). Fig. 2.3(c) shows the response at a different operating point when reference voltage is

changed from 30 V to 31 V. A PI controller designed at V_s= *15 V* and R= *25 Ω* has been used in all the cases. The transient response corresponding to V_s = *15 V* (Fig. 2.3 (a)) is faster and has smaller overshoot when compared to the transient responses in the other two cases. This clearly demonstrates the local scope of linear controllers.



(a)



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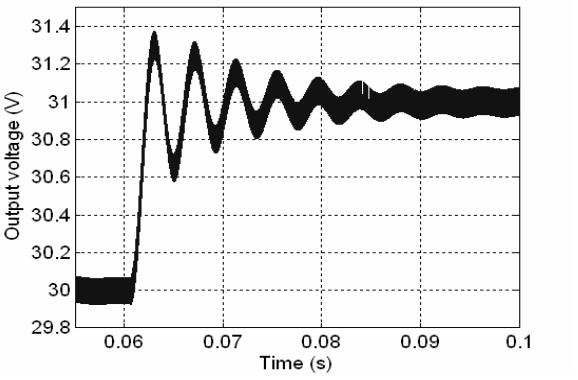


(c)

Fig. 2.3. Demonstration of model-dependent nature of linear controllers- Simulation results (a) Transient response at design operating point V_s=*15 V* , R = 25 Ω, V_o transient from 25 V to 26 V(b) Transient response at a different operating point V_s=*10 V* , R = 25 Ω, V_o transient from 25 V to 26 V (c) Transient response at a different operating point V_s=*15 V* , R = 25 Ω, V_o transient from 30 V to 31 V.

The non-optimum small-signal transient offered by the linear controller at an operating point different from the design-operating point also suggests that the converter dynamics for large disturbances will not be optimum. This is due to the fact that during large-signal transients, the converter parameters undergo a significant change and the dynamic response is highly-non-linear in nature. In many cases, even the linear controllers hit their saturation limits and are no longer 'linear' in nature. Fig. 2.4 shows the large-signal disturbance response of the converter with the same linear controller that has been used in obtaining the small-signal transients shown in Fig. 2.3. Here, the input voltage of the converter undergoes a large change i.e. from 15 V to 10 V. The poor large-signal transient response is demonstrated by the oscillatory nature of the output voltage and the long settling time.

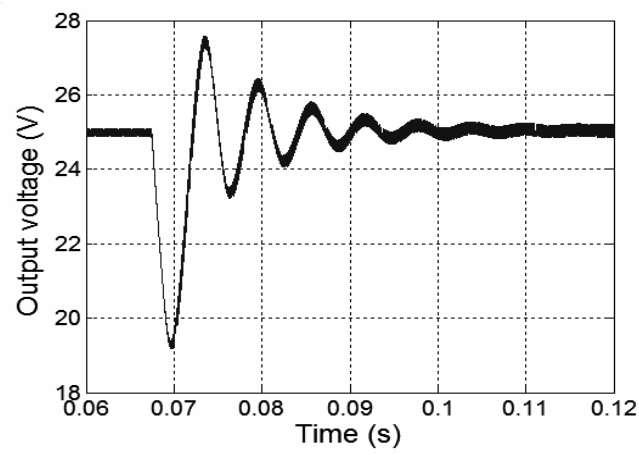


Fig. 2.4. Large-signal transient response offered by linear controller for a step change in V_s (from 15 V to 10 V) at V_o = 25 V and I_o = 1 A.

2.2.2 Solutions to Dynamic Response Problem on Account of Model-Dependent Nature of Controllers

During large-signal transients, as the dynamic response is highly non-linear in nature, several researchers [24], [25], [28] have suggested non-linear controllers as

better alternatives to linear controllers to handle these transients efficiently. A popular way of handling large disturbances or parameter variations efficiently is to employ controllers that posses one among the characteristics listed below.

1. Controller adapts itself to the operating conditions (e.g. Adaptive controllers),
2. Controller is totally independent of the converter model (e.g. Controllers based on Fuzzy logic, and Artificial Neural Networks (ANNs)), and
3. Controller does not need an accurate model of the converter (e.g. Sliding-mode controller (SMC)).

It must be noted that some controllers e.g. controllers employing Artificial Neural Networks (ANNs) may fall under more than one of the above-listed categories. In addition, most of the controllers that possess any one of the above three characteristics are by-and-large non-linear in nature. This non-linear nature, as mentioned before, is believed to be the reason behind the good large-disturbance-handling capability of these controllers.

A. Adaptive Controllers

Some of the popular controllers that fall under this category are adaptive-PID (or linear) controller [16], adaptive-model-reference controller [80], and other types of adaptive controllers [79]. In general, controllers falling under this category will ensure a good small-signal transient response in the converter irrespective of the operating point.

Reference [79] presents an average current-mode control (CMC) scheme for a flyback converter in which the slope of the compensating ramp is adaptively tuned as per the operating point. Slope tuning is achieved by adding a term dependent on the

output voltage and inductor current to the equation defining the constant slope compensation. As a result of tuning, a small-signal transient response better than that obtained with a classical CMC scheme (with slope compensation) has been reported. However, the proposed method of slope tuning does not improve the large-signal dynamics offered by the converter appreciably.

Reference [88] presents a non-linear current-mode control scheme (NCMC) for boost converter that makes the dc gain of the control-to-output transfer function of the boost converter insensitive to changes in load of the converter. The control scheme also reduces the output impedance of the converter. A non-linear term containing information about the input voltage, load current, and output voltage is appended to the original current programming command of the current-mode control scheme in achieving the afore-mentioned advantages. On the downside, the method requires sensing of input voltage and load current.

Many adaptive controllers are implemented using microcontrollers or digital-signal processors (DSPs). This increases the system cost and complexity as peripheral units such as analog-to-digital converters (ADC) are needed. Analog implementations often require several OPAMPs as in [80] and expensive ICs for implementing special functions (e.g. multiplication, division, logarithmic operation etc.). In some implementations involving model reference adaptive controllers, sensing of all the state variables of the converter is needed. This becomes a problem, especially in high-order converters.

B. Controllers that are Independent of Converter Model

Non-linear controllers employing computationally intelligent (CI) techniques such as fuzzy logic [19]-[25] and ANN are popular members of this category.

Fig. 2.5 shows a typical fuzzy logic controlled (FLC) power converter. As shown, most of the FLCs take as inputs the converter's output voltage error and its rate-of-change and compute the incremental duty ratio. References [19]-[23] present such control schemes for buck, boost, and Cuk converters. The non-linear nature of FLCs is believed to improve the large-signal dynamic response of power converters. Such an improvement in dynamic response has been reported in [19], [22], [24], [25].

FLCs are independent of the converter model parameters. This is evident from [19]-[23] in which the converter model has not been used in the development of the control scheme. Variations in converter parameters on account of change in operating point or due to ageing need not be considered when employing fuzzy logic controllers. The ability of fuzzy logic to handle uncertain and imprecise inputs is the reason behind this independency of the controller upon the converter model.

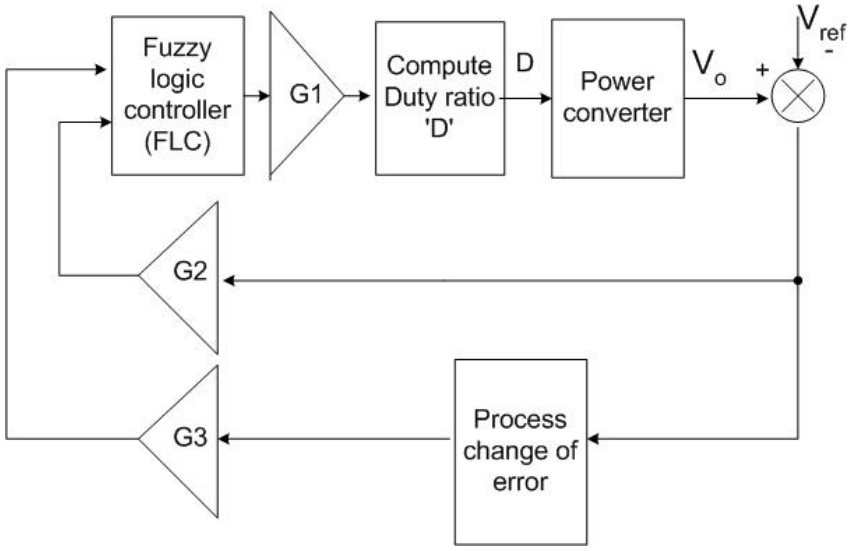


Fig. 2.5. Fuzzy logic controlled (FLC) power electronic converter

In the later part of this thesis, structures of several FLCs used with power converters and reported in literature are analyzed in detail. Logical reason behind the excellent large-signal handling capabilities of these controllers is brought out. The

analysis will also raise questions about the strengths claimed often with FLCs and the very need of FLCs for controlling power electronic converters.

ANNs constitute another group of controllers that are independent of converter model. Fig. 2.6 shows two popular ANN-based control schemes [17] [18] for power converters. In both the schemes, the ANN controller takes as inputs the past m-samples of the controller and converter outputs and computes the operating duty ratio.

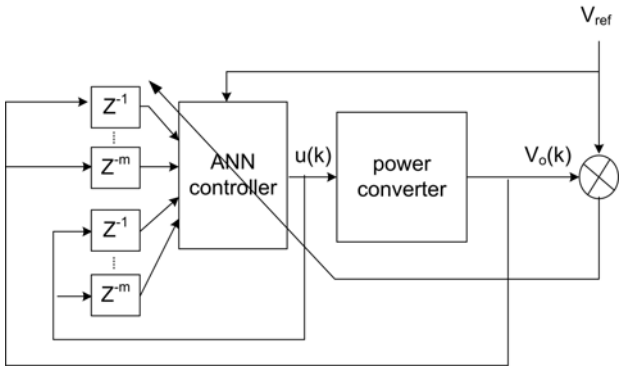
In direct control scheme [17] (refer Fig. 2.6(a)), the converter's output voltage error alone is known. For Back-propagation (BP) algorithm-based weight-adjustment [27], the error at the output of the controller (control-input error to the converter) needs also to be known. This error may be estimated using

$$\in (k) = e(k+1)\frac{\partial y(k+1)}{\partial u(k)}, \tag{2.3}$$

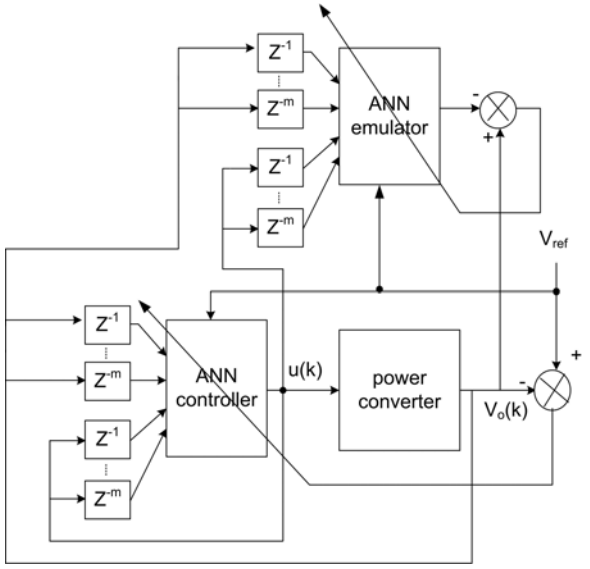
where k represents the sample instant, $\in(k)$ is the estimate of the error at the output of the ANN controller, $e(k+1)$ is the error at the output of the plant and $\partial y(k+1)/\partial u(k)$ is the Jacobian of the plant. Thus, this scheme requires knowledge of the Jacobian of the plant. The above equation assumes that the control input $u(k)$ in the k^{th} instant results in an output $y(k+1)$ at the $(k+1)^{th}$ instant. Based on this assumption, the control error of k^{th} instant is calculated from the output error at the $(k+1)^{th}$ instant using the linear relation in (2.3). However, this assumption may not be true for plants of higher orders and complex non-linearity.

Fig. 2.6(b) shows the indirect control scheme employing ANNs. This method is popular and is applicable even if the plant is ill-defined, as computation of Jacobian of the plant is not needed. The scheme employs two ANNs, namely an ANN emulator

and an ANN controller. The ANN emulator adaptively learns and mimics the converter dynamics on account of its excellent non-linear function matching characteristics. The output voltage error of the plant is back-propagated through the ANN-based emulator to find the error at the output of the ANN controller (control-input error to the converter) for BP-based weight-adjustment. References [17], [18], [26] present such controllers applied to boost dc-dc converter. Reference [26] expresses mathematically the converter output voltage at any instant as a non-linear function of its output voltage and duty ratio in the previous sample instants and constructs a non-parametric model that can be used for getting an ANN-based emulator for the boost converter considered.



(a)



(b)

Fig. 2.6. ANN controllers for power converters (a) Direct control (b) Indirect control using emulator.

It must be noted that in spite of model-independent nature and demonstration of good large-signal dynamic response in power converters by controllers employing CI techniques, due to increased cost and control complexity, these techniques have not been adopted widely by power supply industry. Besides, absence of systematic design and analysis procedure makes these controllers less attractive. In the later part of the thesis, a simple and inexpensive analog alternative of FLC namely, the non-linear function controller (NLFC) is proposed for a boost converter. Systematic analysis and design methods for NLFC are also proposed.

C. Controllers that do not Need an Accurate Model of the Converter

Sliding mode controller (SMC) [28], [29] and H^{∞} controllers [69], [81] are some popular members of this category. Among them, SLMC does not need an accurate mathematical model of the controller but requires the knowledge of parameter variations for reachability and stabilizability as stated in [19]. Reference [19] demonstrates the superior dynamic performance of SLMC over PI controller in a buck converter for large variations in load resistance and supply voltage changes occurring. However the performance of SLMC is reported to be inferior to that of the Mamdani-type FLC discussed in [19].

Although SLMC is known for its robustness, the need for sensing all the state variables increases the control complexity. Besides, variable frequency of operation and associated chattering problems make this controller less attractive. Methods of avoiding chattering problem add to the control complexity and realization of the controller.

References [69] and [81] report H^{∞} controller-based schemes for classical boost converter. The design of these controllers is based on small-signal model of the converter at the operating point. Variations in the model are integrated in the design procedure as disturbances in line and load conditions. The designed controllers maximize the closed-loop bandwidth of the nominal small-signal model assumed for the plant. It must be noted that although robustness to parameter variations is possible using these controllers, sensing of input voltage may be needed as in [81]. Besides, the small-signal closed-loop bandwidth is limited by RHP zero of the converter's control transfer function even in this case.

Reference [78] presents a modified current-mode control configuration for a dc-dc buck converter in which an additional controller that is designed based on the inverse model of the nominal power-stage transfer function (approximated) is used. It is claimed that this additional part helps in achieving robustness for variations in line and load conditions and converter parameters (*L, C* etc.). Besides, improvement in large-signal transient response when compared to a conventional average current-mode control is also reported. However, such a control scheme cannot be used for boost and buck-boost converters as the RHP zero in the actual model becomes RHP pole in the inverse model resulting in instability.

2.3 Chapter Conclusions

In this chapter, a detailed literature survey on the dynamic response problems of boost and buck-boost-derived dc-dc power converters has been presented. A literature search on boost and buck-boost-derived converters in single-phase ac-dc PFC applications has also been done and is given in the appendix D.

Based on the literature survey, it may be concluded that there is a need to come up with simpler solutions for the dynamic response problems in boost and buck-boost-derived converters. Accordingly, the rest of the thesis focuses on investigation and improvement of existing solutions and proposal of novel solutions to the dynamic response problem. The proposed solutions fall broadly under two categories namely,

1. Mitigation of dynamic response problem by enhancement in design of converter and employed controllers.
2. Improvement in dynamic performance by modifications of converter topology- Novel 'Tri-state' class of converters.

Among the above two approaches, the first approach aims only at achieving a marginal improvement in the dynamic performance of the converters. The second of the above-listed approaches is aimed at achieving a significant improvement in dynamic response of the converter at the cost of addition circuit components

CHAPTER 3

DYNAMIC PERFORMANCE IMPROVEMENT BY ENHANCEMENT IN DESIGN AND CONTROL TECHNIQUES

3.0 Introduction

Chapters 1 and 2 explained in detail the dynamic response problems occurring in boost and buck-boost converters. The presence of RHP zero in the control-transfer function of these converters results in sluggish small-signal transient responses. The small-signal dynamic response problem is further compounded by the changes in operating point and converter parameters. It was pointed out that an efficient way of getting good small-signal transient response irrespective of changes in operating point is to employ adaptive controllers.

Chapters 1 and 2 also pointed out that the prime reason behind the sluggish large-signal transient responses offered by boost and buck-boost converters is attributed to the linear nature of the employed controllers. It was suggested that for an improvement in the large-signal dynamic performance of these converters, non-linear controllers be used.

Following the above discussion, in this chapter, investigation of dynamic performance of a boost converter (specifications are given in Table 3.1) with the following controllers is carried out.

1. Gain-scheduled PI-controller (GSPI)
2. Two-input fuzzy logic controller (FLC)

TABLE 3.1. DC-DC BOOST CONVERTERS' SPECIFICATIONS

Input voltage	Output voltage	Rated output power	Switching frequency	L	C
10 to 20 V	25 V	50 W	50 kHz	267 µH	540 µF

The reasons behind considering the above two controllers for investigation are as follows. Both FLC and GSPI controller are non-linear in nature. Thus, they form potential members for handling large-disturbances. Besides, the GSPI controller is also adaptive in nature. Due to this, it appears to have the capability of delivering good small-signal transient response irrespective of changes in the operating point.

The dynamic performance offered in the boost converter by FLC and GSPI controllers are investigated and compared with benchmark PI controllers that are design-optimized at different test operating points. Prior to this investigation, an in-depth analysis into the mitigation of small-signal dynamic response problem due to RHP zero through refinement in the converter's design approach is described. The pros and cons of the design approach are brought out.

It must be noted that this approach of improving the dynamic response of converter through enhanced design of converter/control techniques is aimed at achieving only a marginal improvement in dynamic performance. Significant improvement in small-signal transient response is difficult as the closed-loop bandwidth is limited by RHP zero. It must also be noted that the GSPI controller considered in this chapter is strongly dependent on the small-signal model of the boost converter.

Section 3.1 discusses the mitigation of RHP zero problem in boost converter through refining the design approach. Section 3.2 investigates the performance of the boost converter with locally-optimized PI controller, fuzzy logic controller, and gain-

scheduled PI controller. Simulations and experimental results and dynamic performance comparison with locally-optimized PI controller are presented.

3.1 Mitigation of RHP Zero Problem by Refining the Design Approach

The dynamic response problem due to RHP zero can be minimized by shifting the zero farther in the right-half plane. A popular way of avoiding this problem would be to operate the converter in Discontinuous Conduction Mode (DCM).

As described in Chapter 2, the presence of RHP zero in time domain response is indicated by an initial under-shoot (overshoot) in output voltage for a small-step increase (decrease) in duty ratio due to decreased (increased) output current. The reason for this is demonstrated in Fig 3.1 that shows the output charge (indicated by areas A_1 and A_2) transferred before and after a small-step increase in duty ratio ($\hat{d}$). In general, the area A_2 is less than A_1 due to which an initial dip in output voltage is observed. This dip may be avoided under the conditions when A_2 is more than A_1. The conditions under which A_2 will become greater than A_1 can be derived as below.

The average output currents I_{o1} and I_{o2} before and after the step change in duty ratio are given by (3.1) and (3.2) respectively.

$$I_{o1} = \frac{I_1 + I_1^{'}}{2}(1-D) = \left(I_1 + \frac{V_s}{2L} DT \right)(1-D) \tag{3.1}$$

$$I_{o2} = \frac{I_2{}'' + I_2^{'}}{2}\left(1-D-\hat{d}\right) = \left(I_1^{'} + \frac{V_s}{L}\hat{d}T + \frac{V_s - V_o}{2L}\left(1-D-\hat{d}\right)T \right)\left(1-D-\hat{d}\right) \tag{3.2}$$

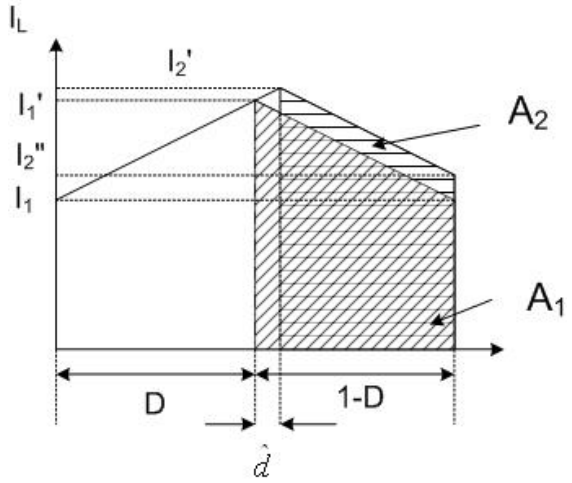


Fig. 3.1. Mitigation of RHP zero problem

The problem with RHP zero may be reduced under conditions when A_2 becomes more than A_1. i.e when

$$I_{o2} \geq I_{o1} \tag{3.3}$$

Let us assume that the output voltage does not change appreciably immediately after the small-step change in duty ratio. Substituting (3.1) and (3.2) in (3.3) and rearranging (neglecting the non-linear terms involving $\hat{d}^2$), the resulting expression can be simplified as below.

$$\begin{aligned} &\hat{d}\left(I_1 + \frac{V_s}{L} DT - \frac{V_s}{L} T \right) \leq 0 \\ &\Rightarrow \left(I_1 + \frac{V_s}{L} DT - \frac{V_s}{L} T \right) \leq 0 \text{ as } \hat{d} > 0 \end{aligned} \tag{3.4}$$

The above equation can be re-written as

$$\left(I_1 + \frac{V_s}{L} DT \right) \leq \frac{V_s}{L} T \tag{3.5}$$

In CCM, the current I_1 can be written in terms of the average inductor (input) current I_L as

$$\left(I_L - \frac{V_s}{2L} DT + \frac{V_s}{L} DT \right) \leq \frac{V_s}{L} T \tag{3.6}$$

$$\left(I_L + \frac{V_s}{2L}DT\right) \le \frac{V_s}{L}T \Rightarrow \frac{V_o I_o}{V_s} + \frac{V_s}{2L}DT \le \frac{V_s}{L}T$$
$$\Rightarrow L \le \frac{V_s^2 T}{V_o I_o}\left(1 - \frac{D}{2}\right) \tag{3.7}$$

At this value of L, the control-to-output transfer function (1.3) of the converter obtained by state-space averaging and linearization can be re-written as follows.

$$\frac{V_o(s)}{D(s)} = \frac{\mathrm{V_s}}{(1-D)^2} \frac{\left(1 - sT\left(1 - \frac{D}{2}\right)\right)}{1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}} \tag{3.8}$$

Equation (3.8) shows that the location of RHP zero is shifted to frequencies between $1/(2\pi T)$ Hz (calculated at *D=0*) and $1/(\pi T)$ (calculated at *D=1)*. As closed-loop bandwidth realized with power converters are generally less than $1/(2\pi T)$ Hz, the effect of RHP zero in the dynamic performance of the converter is reduced significantly. This also simplifies the controller design.

Although the effect of RHP zero is made negligible, the boost inductance calculated using (3.7) will result in higher ripple current. For example, at an operating point V_s*=10 V,* V_o *= 25 V,* I_o *= 2 A*, T = 20 μs, and *D = 0.6*, the boost inductance calculated using (3.8) is about 28 μH. The RHP zero is located at 71428 rad/s. The inductor average and peak-to-peak ripple currents are respectively 5 A and 4.2 A. Such a high ripple current is not desired.

As mentioned in Chapter 2, operation in DCM is a popular solution of reducing the effect of RHP zero. This reduction in the effect of RHP zero is also evident from (3.5) wherein I_1 becomes zero and the condition is always satisfied.

3.2 Investigation of Dynamic Performance Improvement by Enhanced Design of Controllers

In this section, the dynamic performance improvement in boost converter using GSPI and FLC are studied. The observed dynamic performances offered by these controllers are compared with those offered by benchmark PI controllers that were design-optimized using MATLAB-SIMULINK [63] at different test operating points.

3.2.1 Gain-Scheduled-PI (GSPI)-Based Scheme

As demonstrated in Chapter 2, a single PI-controller designed-optimized by frequency-domain methods (Bode plots) to offer good small-signal transient at an operating point may not give a satisfactory transient performance when the operating point changes. An obvious way to ensure good small-signal transient at any operating point is to get the optimal sets of proportional (K_p) and integral (K_i) gains of the PI controller $\lfloor K_p + K_i / s \rfloor$ at several operating points and then tune them appropriately with changes in operating point.

In this sub-section, the dynamic performance of boost converter with one such Gain-Scheduled-PI controller (GSPI) is studied. To begin with, the optimal PI-controllers at several operating points are obtained using computer simulations. The near-functional relation between the PI-controller's parameters and the operating point are determined. These functional relations are used for tuning the PI controller's parameters when the operating point changes. Following this, simulation results demonstrating the performance of converter with GSPI are presented.

A. **Development of GSPI Controller**

Using MATLAB-SIMULINK, the dc-dc boost converter (with parasitics[1]) has been simulated with thousands of combinations of proportional (K_p) and integral (K_i) gains. The sets of K_p and K_i that offered minimum settling time for a step change in reference voltage from 25 V to 27 V at various operating points are listed in Table 3.2.

TABLE 3.2. 'BRUTE-FORCE' OPTIMIZED (**BENCHMARK**) PI- CONTROLLERS

Input voltage (V)	Load resistance (Ω)	K_i	K_p	Location of zero of the controller	Settling time (s)
10	12.5	9	0.03	300	0.006057
10	25	11	0.022	500	0.002738
10	37.5	10.5	0.021	500	0.002625
10	50	11	0.01833	600	0.002591
12.5	12.5	15	0.01875	800	0.002698
12.5	25	14.5	0.0145	1000	0.002459
12.5	37.5	14.5	0.01318	1100	0.002399
12.5	50	14.5	0.01318	1100	0.002351
15	12.5	18	0.012	1500	0.002447
15	25	17	0.0081	2100	0.002418
15	37.5	16	0.00727	2200	0.002504
15	50	16	0.00667	2400	0.002478
17.5	12.5	39	0.04875	800	0.003333
17.5	25	42.5	0.05313	800	0.00304
17.5	37.5	44	0.055	800	0.002947
17.5	50	50	0.0625	800	0.002962
20	12.5	46	0.04182	1100	0.003087
20	25	47.5	0.04318	1100	0.002923
20	37.5	48	0.04364	1100	0.002874
20	50	38	0.03455	1100	0.003216

From Table 3.2, it may be seen that the integral gain has an almost linear relationship with the input voltage and is more or less independent of the load. The approximate relation of integral gain to input voltage has been found to be

$$K_i = 10 + 2*(10 - V_s) \tag{3.9}$$

where V_s is the input voltage.

[1] The circuit parasitics considered in this case are different from the one used in section 3.3. They are ESR of C = 0.15 ohms, ESR of L = 0.4 ohms.

However, the proportional gain K_p and hence the location of zero of the controller transfer function is not seen to follow any known functional relation. Due to non-availability of a definite functional relation between operating point and K_p, following the discussions in [77], the actual value of K_p has been made dependent on the output-voltage error. The relation is as follows.

$$Kp(t) = K_{p\max} - (K_{p\max} - K_{p\min}) \exp^{(-a|e(t)|)} \tag{3.10}$$

where, the factor '*a*' decides the rate at which the value of K_p rises from K_{pmin} to K_{pmax}. Values of K_{pmax} (=0.04364) and K_{pmin} (=0.00667) are extracted from Table 3.2. The value of '*a*' has been chosen to be 128 using computer simulations.

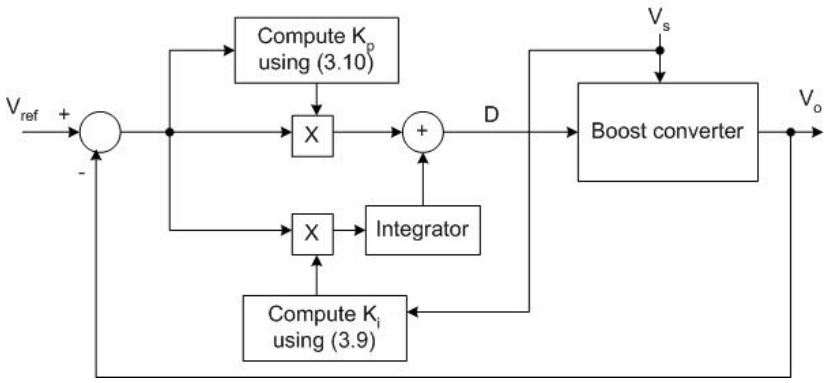


Fig. 3.2. Gain-scheduled-PI (GSPI) controller-boost converter: Schematic.

B. Simulation Results and Discussions

The GSPI controller-boost converter scheme is shown in Fig. 3.2. The scheme has been simulated using MATLAB-SIMULINK. Fig. 3.3 compares the simulated response of the boost converter (considering the effect of parasitics) with GSPI and optimized-PI controller (taken from table 3.2) at a certain operating point. As the simulations were carried out on a large-signal averaged model of the converter (refer appendix B), switching effect is not seen in the responses. The settling time with optimal-PI is shorter than that with GSPI controller.

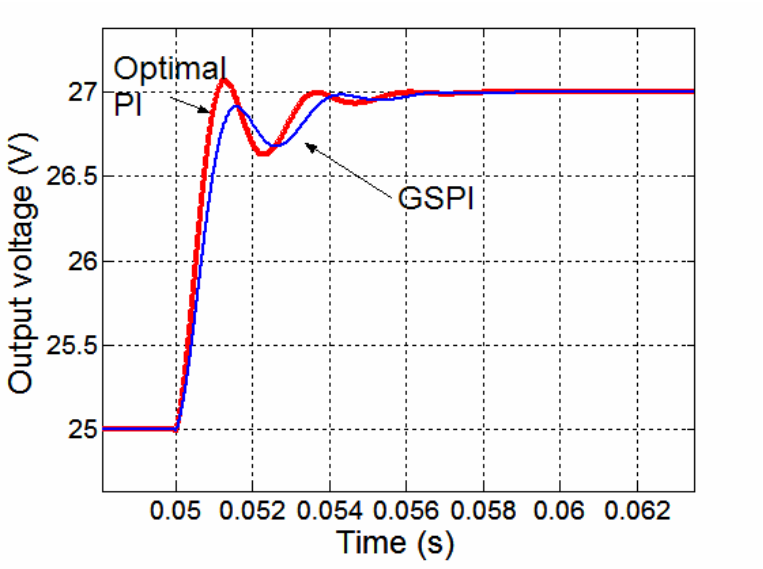


Fig. 3.3. Performance comparison of GSPI and PI for step change in reference voltage from 25 V to 27 V at 0.05 s at V_s = 20 V, R = 50 Ω.

Table 3.3 shows a comparison of simulated small-signal transients offered by the GSPI and benchmark PI controllers (Table 3.2) at various operating points. Here, the settling time refers to the time taken by the output voltage to reach and stay within 5% of the step change in reference voltage. It may be noticed that under high line conditions, the performance offered by GSPI controller is almost comparable to that offered by the benchmark optimized-PI. Nevertheless, it is clear that the approximations made to K_i (3.9) and the implemented control law for K_p (3.10) do not help in offering a performance better than that offered by the optimized-PI controllers.

Table 3.4 summarizes the comparison of large-signal transients offered by GSPI and benchmark-PI controller. While in two cases (1 and 3) the performance offered by GSPI controller is better than that offered by benchmark-PI controller, in the rest of the cases, the responses with benchmark-PI controllers are better than those due to the GSPI controller. The reason for this could also be attributed to the approximations made to the gains of GSPI. However, unlike the small-signal transient responses listed

in Table 3.3, GSPI offers large-signal transient responses comparable to those offered by the locally-optimized PI controllers.

TABLE 3.3. GSPI VERSUS PI- CONTROLLER: SMALL-SIGNAL STEP RESPONSE

Input voltage (V)	Load current (A)	Reference voltage step		Settling time (ms)		Percentage overshoot (%)	
		From	To	GSPI	Benchmark PI	GSPI	Benchmark PI
10	2	25	27	19	< 7	10	2.9
10	0.5	25	27	6.25	2.6	0	3.5
15	1	25	27	4.75	2.4	0	4.2
20	2	25	27	3.8	3	0	12
20	0.5	25	27	3.62	3.2	0	3.5

TABLE 3.4. GSPI VERSUS PI- CONTROLLER: LARGE-SIGNAL STEP RESPONSE

Case	V_s (V)	I_o (A)	Reference voltage step change (V)		step response			
					Settling time (within 5% of the reference step) (ms)		% Overshoot/ undershoot	
			From	To	GSPI	PI	GSPI	PI
1	11	2	24.9	20.9	8	13	0	0
2	10	0.5	21	25	7.25	6.25	0	0
3	15	1	21	25	5	5.2	0	0
4	20	2	21	25	4.2	3.1	0	0
5	20	0.5	20.7	24.9	4.68	4.55	0	0

One obvious disadvantage of the GSPI method is that the input voltage has to be sensed (Fig. 3.2). Besides, the analog implementation of control law (3.10) needs the use of multiplier and logarithmic ICs which are expensive. Digital implementations also need expensive DSPs for implementing the complex law. Even with an inexpensive microcontroller, the implementation is complex due to the additional interfacing and protection circuitry needed. Besides, such an implementation may also force a compromise either in the switching frequency of the converter or in the

sampling frequency of the variables due to the associated time-consuming calculations. On account of these practical issues, hardware implementation of the controller has not been attempted.

3.2.2 Fuzzy Logic-Based Approach

Recently, there have been several publications which apply fuzzy logic controllers (FLCs) to control power electronic converters [19]-[25], [54]-[61]. In general, these non-linear controllers have been shown to offer excellent dynamic response in power converters [19], [22]-[25], with references [22] and [25] demonstrating in particular, the excellent large-signal dynamic response characteristics offered by FLCs.

To study the dynamic performance of the boost converter under consideration with an FLC, a Sugeno-type FLC has been simulated, built, and tested. This sub-section presents the details of the FLC developed and the results (simulation and experimental) comparing the performance of FLC with benchmark PI-controllers. Prior to this, the benchmark PI- controllers are re-designed for reasons mentioned in the following sub-section.

A. Re-design of Benchmark PI Controllers

The benchmark-PI controllers designed in Table 3.2 are based on brute-force techniques and the effect of converter parasitics have been taken into account in the arriving at the controller parameters. As circuit parasitics vary from one converter to another, the benchmark PI controllers were re-designed based on the small-signal control-to-output transfer function (without parasitics) of the boost converter under consideration at the design operating points. Bode plots were used for the design.

Table 3.5 summarizes the different operating points considered, the designed PI controllers, and the phase margins offered by these controllers at the design operating point.

TABLE 3.5. LOCAL LINEAR-PI CONTROLLERS

Input voltage (V)	**Load current (A)**	**Output voltage (V)**	**Benchmark PI controller**	**Phase margin (degrees) (theoretical)**	**Gain crossover frequency (rad/s) (theoretical)**	**Benchmark Controller realized in the hardware setup**
10	2	25	$17.25\frac{\frac{s}{853}+1}{s}$	46.489	461.39	$16.94\frac{\frac{s}{1000}+1}{s}$
10	0.5	25	$17.25\frac{\frac{s}{1004}+1}{s}$	45.3	981	$16.94\frac{\frac{s}{1000}+1}{s}$
15	1	25	$16.5\frac{\frac{s}{1517}+1}{s}$	80.96	943	$16.9\frac{\frac{s}{1470}+1}{s}$
20	0.5	25	$20\frac{\frac{s}{2058}+1}{s}$	99.23	731	$20\frac{\frac{s}{2127}+1}{s}$
20	2	25	$22\frac{\frac{s}{2027}+1}{s}$	96.46	781	$22\frac{\frac{s}{2127}+1}{s}$

It must be noted that the zeros of these PI-controllers in Table 3.5 are located at the corner frequency of the converter's control transfer function (without parasitics), with an aim to increase the closed-loop bandwidth at the given operating point. As changes in load do not affect the location of poles in the control transfer function appreciably, it may be noticed that the location of zero of the controllers designed for a particular input voltage is nearly constant. This also explains the reason behind the nearly-fixed location of zeros of the 'brute-force' benchmark controllers (Table. 3.2) at a constant input voltage.

The gains of the controllers in Table 3.5 have been tuned through computer simulations in order to optimize the settling time of the output voltage for a two volt step change in reference voltage.

An experimental prototype of boost converter has been built and tested. Implementation details are given in Appendix C. Table 3.5 also lists the benchmark PI-controllers realized in the hardware set up. It may be noticed that the gain and zero of the controllers realized in the hardware set up are slightly different from the designed values. This discrepancy is due to limited choice of practical capacitor and resistor values. Fig. 3.4 shows the experimental step response of the converter (fitted with a locally-optimized PI controller) for a small change in reference voltage at a certain operating point. The settling time is about 7 ms.

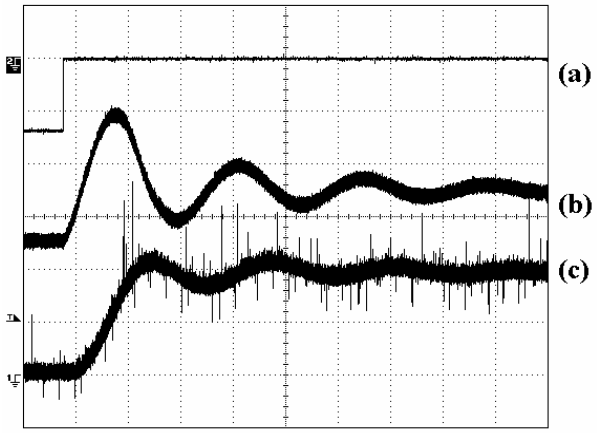


Fig. 3.4. Experimental step response of the boost converter with PI controller for a step change in reference voltage from V_{ref}= 22 V to V_{ref}= 24 V, at R = 12 Ω, V_s = 10 V (a) Step- marks the instant when the reference voltage changes (b) Inductor current (c) Output voltage (channel in ac coupling mode); Scale: voltage: 1 V/div, current: 1 A/div, time: 2ms/div

Table 3.6 summarizes the settling times (obtained by simulations and experiments on a hardware prototype) offered by the various re-designed benchmark PI-controllers for a step change in reference voltage at their corresponding design operating points. Here also, the settling time refers to the time taken by the output

voltage to reach and stay within 5% of the step change in reference voltage. Although the design of controllers did not consider the effect of system parasitics, the simulation results tabulated here do consider the effect of circuit parasitics namely, ESR of inductor (= 0.15 Ω) and ESR of capacitor '*C*' (= 0.1 Ω). The differences observed between the simulated and experimental settling times and transient overshoots is believed to be attributed to the non-exact modeling of system parasitics. The results obtained with these benchmark controllers will be compared with those obtained with fuzzy logic controller discussed in the following section.

TABLE 3.6. PI- CONTROLLER: SMALL-SIGNAL STEP RESPONSE

Input voltage (V)	Load current (A)	Reference voltage step		Simulation results		Experimental results	
		From	To	Settling time (ms)	Percentage overshoot	Settling time (ms)	Percentage overshoot
10	2	22	24	7	2	7	10 (approx.)
10	0.5	24	26	10	1.92	11.4	10 (approx.)
15	1	25	27	6	0.185	8	5(approx.)
20	2	25	27	7	0.37	7	0
20	0.5	25	27	7.5	0.29	7	0

B. Fuzzy Logic Controller- Implementation Details

A two-input Sugeno-type FLC similar to the one in [21] has been simulated, built, and tested with the boost converter whose specifications are given in Table 3.1. The overall schematic is shown by Fig. 3.5. The details of the FLC [22] developed are as below.

FLC Inputs and Output- Description

The inputs to the Sugeno-type FLC are

1. The voltage error (e) (reference voltage subtracted from actual voltage.)

2. The change of the voltage error (ce) ($ce = V_o([k+1]T) - V_o([k]T)$, where T is the period of sampling (and switching)).

As shown in Fig. 3.5, prior to fuzzification, the inputs are multiplied by gains G_2 (=1/15.15) and G_3 (=1). The range of each of the input sets is divided into five fuzzy sets with 50% overlap (refer Fig. 3.6).

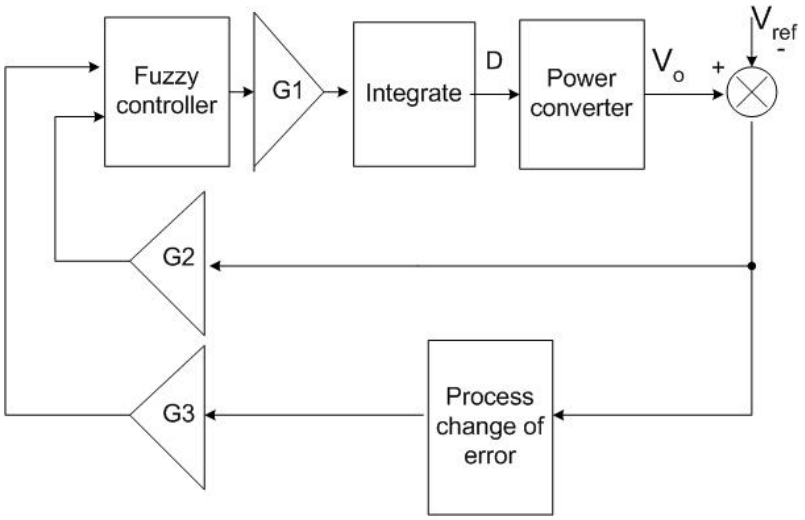


Fig. 3.5. FLC-based control of dc-dc boost power electronic converter

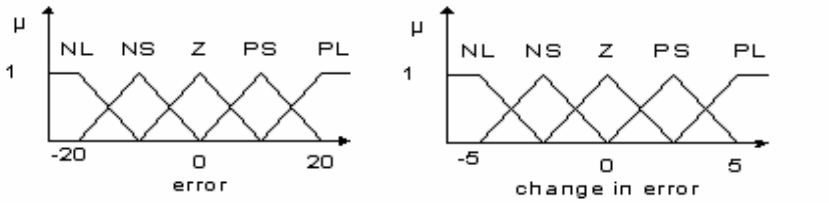


Fig. 3.6 Membership functions for inputs

The FLC is a PI-type FLC, in which the output of the controller is the incremental control action i.e. the incremental duty ratio. This is integrated further to get the actual control action. The universe of discourse of output memberships is spanned by 17 singletons taking values between -1 to 1. They are -1, -0.65, -0.5, -0.45, -0.35, -0.3, -0.2, -0.1, 0, 0.1, 0.2, 0.3, 0.35, 0.45, 0.5, 0.65, 1.

FLC Rule Base

The rules connecting the inputs and the output singletons are based on the understanding of the system. The rules have an *if...then…* structure with the inputs being combined by AND operator. The rule base (Table 3.7) used in [21] has been retained. The development of the rule base is based on understanding of the system. A few rules to mention are as below.

1. When the output voltage is away from the reference and is moving away from at a much fast rate, large-change in control input to bring it towards the set point is essential.
2. When the output voltage is far from the reference and approaching at a very fast rate (NL or PL), small change in incremental control input is given.

The selection of rule base and its tuning are cumbersome and are based on computer simulation. In the next chapter, an in-depth analysis of rule bases of several FLCs are carried out and a simple way of obtaining the rule base is explained.

TABLE 3.7. RULE TABLE OF SUGENO-TYPE FLC USED FOR CONTROLLING DC-DC BOOST CONVERTER

e / ce	NL	NS	Z	PS	PL
NL	1	0.5	0.2	0	-0.3
NS	0.65	0.35	0.1	-0.1	-0.35
Z	0.45	0.2	0	-0.2	-0.45
PS	0.35	0.1	-0.1	-0.35	-0.65
PL	0.3	0	-0.2	-0.5	-1

De-fuzzification Method

Among the several de-fuzzification methods, the popular centre of gravity method [65] (3.11) has been used. The de-fuzzified value (output of FLC) is multiplied by a gain G_1 (=0.0113) (Fig. 3.5) to yield the incremental control action.

$$Z_o = \frac{\sum_{i=1}^{N} c_i * w_i}{\sum_{i=1}^{N} w_i} \tag{3.11}$$

where w_i is the membership value of the output set i, c_i is the corresponding singleton value, N is the number of output singletons, and Z_o is the defuzzified value.

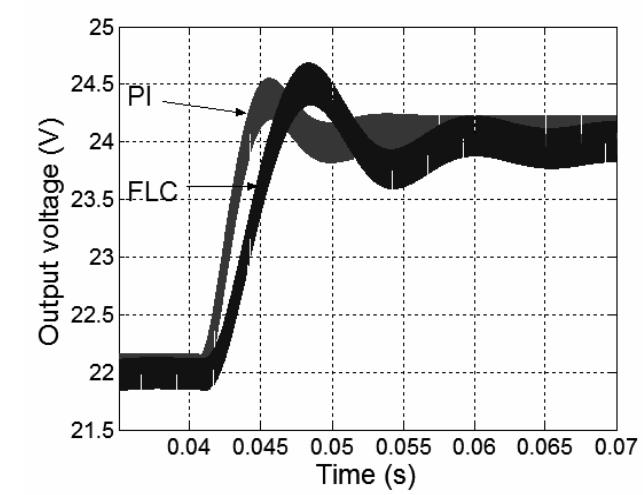
C. Simulation and Experimental Results and Comparison of Performance with Linear-PI Controller

The FLC described in the previous sub-section has been simulated using MATLAB-SIMULINK. Besides, hardware realization of the controller has been achieved using a MSK243 [75] starter kit employing TMS320F243 [76] digital signal processor (DSP). This sub-section discusses the simulated and experimental results.

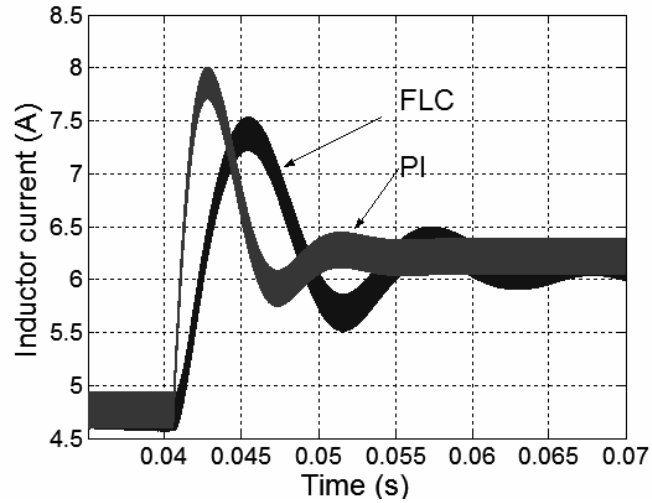
Simulated Results and Comparison

Fig. 3.7 compares the simulated reference-voltage-step responses of the boost converter offered by FLC and by locally-optimized PI controller (discussed in section 3.2.2 (A)) at a certain operating point. For this small-step change in reference voltage, the transient response offered by locally-optimized PI controller is much better than that offered by FLC.

Table 3.8 compares the settling times and transient overshoots offered by the controllers for a small-step change in reference voltage at different operating points. It may be seen that in most of the cases, the transient response offered by the locally-optimized PI controller is much better than that offered by the FLC.



(a)



(b)

Fig. 3.7. Simulated reference-voltage-step-up transients offered by FLC and PI controllers at V_s = 10V, I_o = 2A, step of V_{ref} from 22 V to 24 V (a) output voltage (b) inductor current.

TABLE 3.8. SIMULATED STEP RESPONSE – COMPARISON BETWEEN FLC AND LINEAR-PI CONTROLLER

Case	V_s (V)	I_o (A)	Step response (V)		Settling time (within 5% of the step) (ms)		% Overshoot	
			From	To	Fuzzy	PI	Fuzzy	PI
1	10	2	22	24	13	7	3.04	2
2	10	0.5	24	26	40	10	2.88	1.92
3	15	1	25	27	8.5	6	0.55	0.185
4	20	2	25	27	5.5	7	0.148	0.37
5	20	0.5	25	27	7	7.5	0	0.29

Experimental Results and Comparison

Fig. 3.8 shows the experimental step response of the converter with FLC for a large step-change in reference voltage. Fig. 3.9 shows the corresponding response of the converter fitted with a locally-optimized PI controller. The response offered by the PI controller is more oscillatory than that offered by the FLC. Besides, the settling time with FLC is smaller than that with the PI controller.

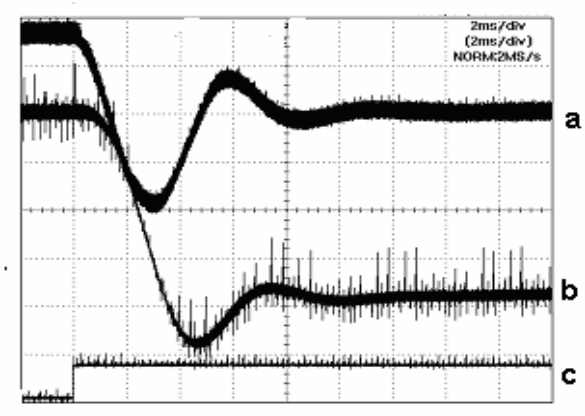


Fig. 3.8. Experimental step response of the classical boost converter with FLC for a large step-change in reference voltage V_{ref} at V_s = 11 V, I_o = 2.1 A (when V_o = 24.9 V) (a) Inductor current (b) V_{ref} step change from 24.9 V to 20.9 V (c) Step V_{ref} (inverted); Scale: voltage: 1 V/div, current: 1A/div, time: 2ms/div.

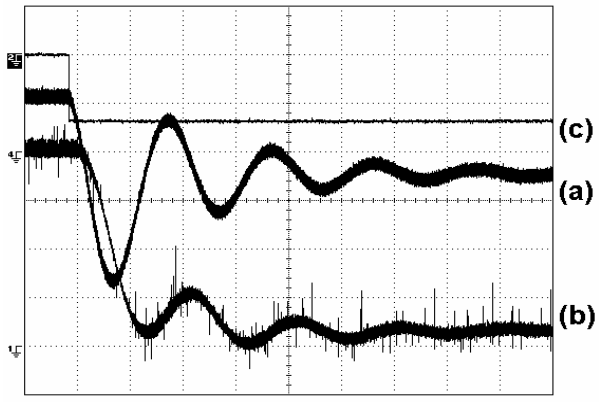


Fig. 3.9. Experimental step response of the classical boost converter with PI controller for a large-step change in V_{ref} at V_s = 11 V, I_o = 2.0 A (when V_o = 24.9 V) (a) Inductor current (b) V_{ref} step from 24.69 V to 20.77 V (c) Step V_{ref}; Scale: voltage: 1 V/div, current: 1A/div, time: 2 ms/div.

Table 3.9 compares the experimental small-step and large-step reference-voltage-change transient responses offered by FLC and linear-PI controllers at various operating points. It may be seen that for large-signal transients (case 1 and 3), the response with FLC is much better than with PI controller in one case (case 1) and is almost comparable to that offered by the PI in other case (case 3). For small-signal transients (case 2 and 4) the response with PI is only marginally better than that offered by FLC.

TABLE 3.9. COMPARISON OF EXPERIMENTAL RESULTS: FLC VERSUS PI-CONTROLLER

Case	V_s (V)	I_o (A)	step response (V)		step response			
					settling time (within 5% of the reference step) (ms)		% Overshoot/ undershoot	
			From	To	fuzzy	PI	fuzzy	PI
1	11	2	24.9	20.9	6	12	25	10
2	11	2	23.3	24.9	8	7	12.5	26
3	20	0.5	20.7	24.9	8	8	4.7	6.66
4	20	0.5	23.5	25.1	6	6	13.3	0

Discussions

Simulation results (Table 3.8) demonstrate the fact that by and large, the locally-optimized PI controller gives a better small-signal transient than the FLC. However, with cases 4 & 5 (Table 3.8), the converter's small-signal transient response with FLC is better than that offered by the converter with local-PI controller.

In the experimental results (Table 3.9, case 2 and 4), the advantage offered by locally-optimized PI controller is only marginal over FLC. Besides in case 3 of Table 3.9, the large-signal transient offered by PI is better than that offered by FLC. The following discussion explains the discrepancy observed in the large-signal transient response.

The FLC has been implemented using a DSP and the PI controller has been realized using analog circuitry. The quantization errors occurring on account of the limited word length of DSP often affect the performance of the realized controller. Besides, with a controller having small gain terms (as in the present case in which gain $G_1 = 0.0113$ in FLC) implemented on a fixed point processor (TMS320F243), the rounding-off errors may become significant, if not handled properly. The truncation and rounding-offs errors may slow down the rate of change of control action. In other words, the system damping is increased. This is believed to be one of the reasons behind the large-signal transient of PI being better than that of the FLC in case 3 (Table 3.9).

Although the above discussion answers the question of large-signal response (experimental) of PI controller being better than that of FLC, it does not explain the reason behind the good small-signal transient (obtained by simulations) offered by FLC over local-PI controller in cases 4 & 5 (Table 3.8). Thus, a blind comparison of transients offered by the controllers without addressing the following issues will be of not much use.

1. The reason behind FLC offering good large-signal transient in most cases.
2. The reason behind FLC offering small-signal transient response comparable to that offered by the localized-PI controller in some cases.
3. The systematic design procedure of getting an FLC that offers good small-signal transient response in the power converter.

For answering the above questions, in the next chapter, the structure of several FLCs implemented with power converters is analyzed in detail based on which, the

transient response offered by FLC is also explained. Design of FLCs to offer good small-signal transient response is also explained.

Due to complexity of control algorithm and expensive realizations, FLCs have not become popular in the control of power converters. To overcome this drawback, in the next chapter, a fast and inexpensive alternative of FLC namely, the non-linear function controller (NLFC) that has the potential to be used in future power supplies is also proposed.

3.3 A Note on Other Linear Compensators

In many applications a compensator realized using two zeros and two/three poles (3.12) is used [93], [94]. The zeros Z1 and Z2 are chosen to compensate for the system/converter poles. The pole at the origin ensures zero steady-state error. The pole P1 is placed above the cross-over frequency to ensure that the gain slope does not become positive on account of RHP zero and zero introduced by ESR of the filter capacitor. The pole P2 is a high frequency pole that ensures high frequency roll-off at -20 dB/dec.

$$P_C = G\frac{\left(1+\frac{s}{Z1}\right)\left(1+\frac{s}{Z2}\right)}{s\left(1+\frac{s}{P1}\right)\left(1+\frac{s}{P2}\right)} \tag{3.12}$$

With such a compensator, the gain-crossover frequency will be better that that realized using simple PI controllers. A re-designed controller corresponding to the operating conditions given by $V_s = 15\ V$, $V_o = 25\ V$, and $R = 25\ \Omega$ is given below.

$$P_C = 25\frac{\left(1+\frac{s}{625}\right)\left(1+\frac{s}{714}\right)}{s\left(1+\frac{s}{62500}\right)\left(1+\frac{s}{153846}\right)} \tag{3.13}$$

As mentioned before, the pole at the origin ensures zero steady state error. The two closely placed zeros compensate the system (converter) poles and provide differential action. Fig. 3.10 shows the frequency response of the loop gain when the converter is at the design operating of $V_s = 15\ V$, $V_o = 25\ V$, and $R = 25\ \Omega$. The effect of parasitics in the converter is neglected. The RHP zero of the control transfer function is located at 32374 rad/sec. The system poles are located at 1593.5 rad/sec. With the above compensator, the gain crossover frequency is about 6470 rad/sec which is much higher than that realized using PI controller (refer table 3.5). It must be noticed that even in this case, the bandwidth realized is significantly less than the RHP zero location.

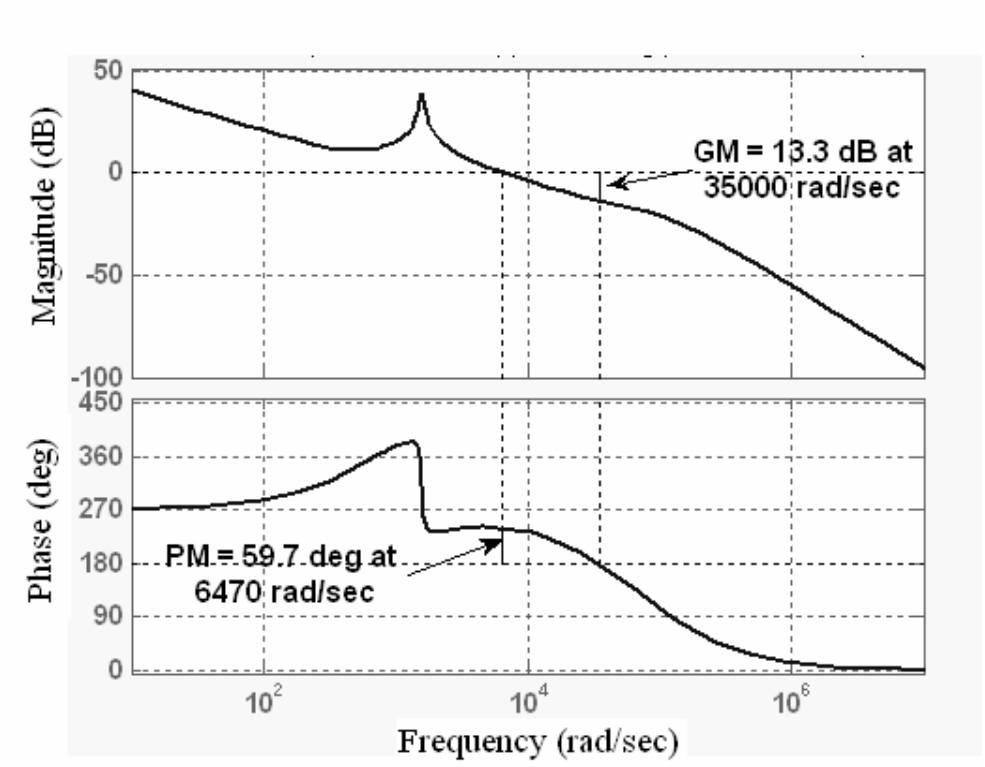


Fig. 3.10. Frequency response plot with re-designed controller.

Fig. 3.11 shows the simulated response with the re-designed controller for a step change in reference voltage from 25 V to 27 V. Here also the effect of system parasitics is neglected. The settling time of the output to reach within 5% of the final value is about 3 ms. An important point to be noted is that even for this small step transient, the boost inductor current is increased to a large value (5.7 A). This is due to the differential action introduced by the zeros of the controller. This high transient inductor current will require the inductor size to be increased besides increasing the device stresses.

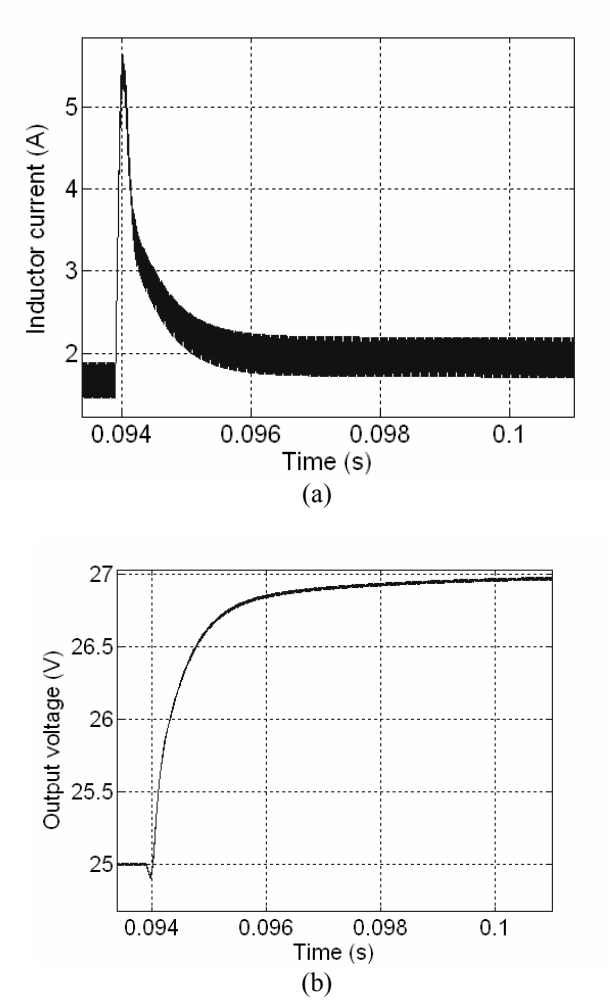


Fig. 3.11. Simulated reference-voltage-step-up transients offered by redesigned controller at V_s = 15V, I_o = 1A, step of V_{ref} from 25 V to 27 V (a) output voltage (b) inductor current

The re-designed controller is a third order controller. The transient response will be dependent on the state of these energy elements and their rates of changes. In general, due to the higher number of energy elements, a high order controller/system will be more sensitive to changes in operating point than a relatively lower order controller/system. Thus in the rest of the thesis, the investigation is carried out with PI controller as benchmark for boost converter.

3.4 Discussions and Conclusions

The following conclusions can be drawn from the discussions in this chapter.

1. Small-signal dynamic response problem due to RHP zero in a boost converter operating in CCM can be mitigated by appropriately selecting the boost inductor value. However, the resulting inductor current will have a high ripple which is an important consideration.
2. Linear-PI controller designed at an operating point offers the nearly best transient response possible at the operating point in the case of boost converters. However, it must be noted that the response is still slow as the closed-loop bandwidth is limited by the presence of RHP zero in the control-to-output transfer function of the converter. Unless the RHP zero is avoided or pushed farther in the right-half of the complex-s-plane, an improvement in closed-loop bandwidth is difficult. In this chapter, the best possible transient that can be obtained through modifications in control techniques has been explored. The other alternative to achieve an even fast transient response (by avoiding the RHP zero) is to modify the converter topology itself. Such a modified topology that introduces one more operating interval in the

converter is carried out in Chapter 5. The later part of the thesis will focus on this 'tri-state' class of converters.

3. The integral gain of an adaptive PI controller need not be changed for getting an optimum transient when the load alone changes. It has been observed that the integral gain has an almost-linear relation with input voltage. On the other hand, the proportional gain does not hold any well-defined functional relation with the operating point.

4. In spite of implementation complexities of two-input FLC and GSPI controllers, not much advantage in terms of small-signal transient response over the locally-optimized PI controller is observed. However, the two-input FLC offers good large-signal transient, the reason for which will become obvious in the next chapter.

CHAPTER 4

NON-LINEAR FUNCTION CONTROLLER: A SIMPLE AND COST-EFFECTIVE ALTERNATIVE TO FLC

4.0 Introduction

In the previous chapter, dynamic response problem in boost converter has been investigated using fuzzy logic controller (FLC). Typically, FLCs are realized using microcontrollers or digital signal processors (DSPs) [21]. Due to FLC's complex algorithm, the computational overhead on the processor is high. Also, with an increased preference to operate power converters at high switching frequencies, there is a significant reduction in the computational time available for implementing the control logic. Thus, expensive high-speed processors will be required to implement an FLC for a high frequency power converter.

FLC realizations using inexpensive microcontrollers [20], [23] require that either the sampling frequency or the converter's switching frequency be reduced, forcing a compromise on the dynamic response performance of the converter. In addition, as mentioned in Chapter 3, high quantization and rounding-off errors add to performance degradation and sometimes may even result in limit cycles when employing low-priced microcontrollers with limited word length and PWM resolution [66].

Many problems related to digital implementation do not arise in an analog realization of FLC [56]. However, such an analog implementation employs a large number of components for fuzzification, rule-base, and de-fuzzification. Hence the

overall controller occupies a large physical space. In addition, any attempt to increase the number of fuzzy sets for increasing the granularity will be cumbersome as this would also increase the size of rule base and also the number of operational amplifiers (op-amp) used in the realization.

In this chapter, based on an investigation on the input sets and rule bases, it is shown that the rule table of most of the FLCs typically utilized in the control of power electronic converters in other publications [19]-[25], [54]-[61] (including the one that has been discussed in Chapter 3) can be approximated to a single-input-single-output (SISO) non-linear function. This simplifies very greatly the analysis and realization of the controller. With this simplification in place it would be more appropriate to call the implemented controller as 'Non-Linear Function Controller (NLFC)' than as 'Fuzzy Logic Controller (FLC).' This simplified structure can be realized with a simple non-linear analog circuit using minimum number of components. Even with digital implementation, the computational overhead of the processor will be significantly reduced. **The simplified structure also makes it easier to explain the excellent large-signal performance of FLCs (reported in the previous chapter) over linear controllers. In addition, the process of designing NLFCs (and indeed FLCs) to yield good small-signal dynamics similar to linear controllers becomes logical.** The motivation behind the simplification of FLC into NLFC comes from [61], in which the reduction of a two-input FLC with a skew-symmetric type of rule table typically used in control of power converters into a single-input FLC is described.

In this chapter, reduction of an FLC rule table of the type typically used in power converter control applications into an NLFC is first described. It is seen that in several power converter control applications, the FLCs take error and change-in-error

of the output variable as inputs and compute the incremental control action which is integrated to get the actual control input. The simplification of such a PI-type FLC turns out to be a Non-linear PI Controller (NPIC), as will be explained and investigated in greater detail in this chapter. Such an NPIC is proposed, developed, and tested on a classical single-switch dc-dc boost converter. While the NPIC behaves as a linear-PI controller delivering excellent transient performance for small disturbances around the steady-state operating point, its non-linearity helps in achieving excellent large disturbance response. Experimental results are presented to demonstrate this aspect clearly. Simulation results are also presented to show that the response of NPIC is almost identical to that of an FLC. The simplification of PI-FLC to NPIC has also been used to predict the gain margin of the system beyond which the system breaks into limit cycle oscillations. The predicted stability limits are then verified experimentally.

Section 4.1 analyses the structure of several FLCs used in power converter control applications. Based on this, section 4.2 establishes and explains the approximation of two-input FLCs into a simple non-linearity, the NLFC. Sections 4.3 and 4.4 present analog circuit realization of NLFC. Section 4.5 verifies the equivalence of NLFC and FLC. Section 4.6 analyzes the similarity between NPIC (reduced form of PI-FLC) and linear-PI controllers. It also suggests design methods that can help in achieving good transient response with NPICs in power converters. Section 4.7 describes the design of NPIC with an example. The PI-FLC equivalent to NPIC described in section 4.7 is developed in section 4.8. Section 4.9 discusses the experimental results comparing the transient response performances offered by NPIC and linear-PI controllers. Section 4.10 describes and presents the stability analysis based on describing function method. Section 4.11 concludes the chapter.

4.1 Analysis of FLC Structure in Power Converter Control

In this section, the structure of several FLCs that have been used to control power converters in the past are investigated, based on which, a simple non-linearity that approximates the rule table is discussed. Furthermore, the FLC itself is replaced by a simple analog circuit.

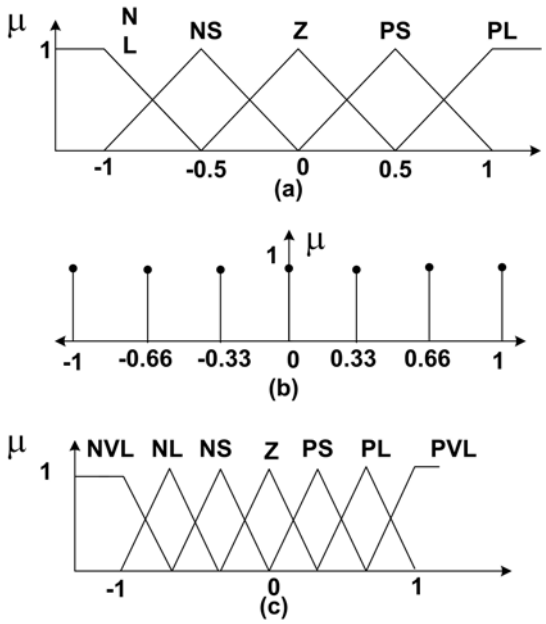


Fig. 4.1. Membership functions- shapes (a) input (Sugeno and Mamdani) (b) output singletons (Sugeno) (c) output (Mamdani)

4.1.1 Shape of Input and output Membership Functions

The first stage in all FLCs is the fuzzification of the inputs. The FLCs proposed in [19]-[23], [25], [54]-[59], take error and change in error of output state variable as inputs. Reference [24] proposes an FLC for buck-boost and Sepic converters, in which the inputs are the output voltage error and the inductor current error. In all the above cases, the shape of all the input membership functions other than those at the extreme ends of the range are triangular (refer Fig. 4.1(a)) and have a 50% overlap.

The triangular membership functions are symmetric in [20]-[21], [23], [24], [25], [59] and asymmetric in [19], [54], [57].

The output membership functions are either singletons as in Sugeno-type FLCs (Fig. 4.1(b)) [21]-[23], [56] or triangular/trapezoidal with 50% overlap (Fig. 4.1 (c)) as in Mamdani-type FLCs [19], [20], [54], [24], [25], [57], [58]. The membership functions are asymmetric triangles in [54] and [57].

The membership grades of the output membership functions are generally determined either by Mamdani's minimum fuzzy implication or by Larsen's product implication [65]. Among the several defuzzification methods [65], centroid method is widely used [19]-[23], [55], [57].

Considering an FLC with triangular (symmetric/asymmetric) input and output membership functions having 50% overlap, the input-output relation can be expressed as a fuzzy associative memory (FAM). Irrespective of the different fuzzy operators and implications, FLCs having the same FAM will give the same output for the same inputs at which rules are defined in the FAM (rule table). This fact is used in the proposed simplification.

4.1.2 Rule Base Structure

The heart of FLC is the rule/knowledge base. In this sub-section, the rule bases of several FLCs implemented with power converters are examined. It is seen that in most cases, the rule base has a Toeplitz [64] structure i.e the output membership functions along the diagonal and off-diagonal elements are same as in Table 4.1. Even in cases where it is seen to deviate, upon a greater examination, the structure is found to be near-Toeplitz. Such a Topelitz structure of the rule base is the basis for

simplification of FLC that is dealt in greater detail in the rest of this chapter. It is also seen that a large number of FLC rule tables are also skew-symmetric.

Table 4.1 shows a Toeplitz rule base with output membership functions constant along each (top-left to lower-right) diagonal. Here 'x_1' and 'x_2'are the inputs to the FLC. The membership functions on the leading diagonal are zero (Z) and those on either side of the leading diagonal take opposite signs as well. Such an exact Toeplitz rule base has been used in [19], [20], [25], [54]-[58].

TABLE 4.1. TOEPLITZ RULE TABLE

x_2 \ x_1	PL	PS	Z	NS	NL
NL	Z	NS	NL	NVL	NVL
NS	PS	Z	NS	NL	NVL
Z	PL	PS	Z	NS	NL
PS	PVL	PL	PS	Z	NS
PL	PVL	PVL	PL	PS	Z

The rule tables in [59] and [60] have zeros along their diagonal and have near-Toeplitz structure with only 4 violations out of 49 rules. Information about the rule table structure in [23] is not available.

The rule tables of fuzzy-P and fuzzy-I controllers in [24] is near-Toeplitz with violations at the extreme ends when the magnitude of output voltage error becomes too large (PL or NL).

The rule base of Sugeno-type FLC used in [21] and [22] is shown in Table 4.2. It must be noted that this rule table is the same as that of the FLC developed in section 3.3. It looks as if it does not have a Toeplitz-matrix structure. However, Table 4.3, which has been derived by linear interpolation of Table 4.2, by extending the range of change-in-error 'ce' input (by two times), and by increasing the granularity of error 'e' input, has a near-Toeplitz structure. The 14 elements (out of 81) that violate the

property are marked in bold letters. The magnitude of terms that make the matrix deviate from having an exact Toeplitz structure is insignificant in most of the cases. It should be noted that the rule base is not only near-Toeplitz, but also near-skew-symmetric.

TABLE 4.2[1]. SUGENO-TYPE FLC RULE TABLE [21]

e[1] / ce	NL	NS	Z	PS	PL
PL	0.3	0	-0.2	-0.5	-1
PS	0.35	0.1	-0.1	-0.35	-0.65
Z	0.45	0.2	0	-0.2	-0.45
NS	0.65	0.35	0.1	-0.1	-0.35
NL	1	0.5	0.2	0	-0.3

TABLE 4.3. EXTENDED SUGENO-TYPE FLC RULE TABLE

e / ce	NL	***NM***	NS	***NVS***	Z	***PVS***	PS	***PM***	PL
PVVL	0	-0.1	-0.2	-0.35	-0.5	-0.75	-1	-1	-1
PVL	0.1	0	-0.1	-0.2	-0.35	-0.5	-0.75	-1	-1
PL	**0.2 + 0.1**	**0.1 + 0.05**	0	-0.1	-0.2	-0.35	-0.5	-0.75	-1
PS	0.35	**0.2 + 0.025**	0.1	0	-0.1	**-0.2-0.025**	-0.35	-0.5	**-0.75 + 0.1**
Z	**0.5-0.05**	**0.35-0.025**	0.2	0.1	0	-0.1	-0.2	**-0.35-0.025**	**-0.5 + 0.05**
NS	**0.75-0.1**	0.5	0.35	**0.2 + 0.025**	0.1	0	-0.1	**-0.2-0.025**	-0.35
NL	1	0.75	0.5	0.35	0.2	0.1	0	**-0.1-0.05**	**-0.2-0.1**
NVL	1	1	0.75	0.5	0.35	0.2	0.1	0	-0.1
NVVL	1	1	1	0.75	0.5	0.35	0.2	0.1	0

4.2 Toeplitz Rule Tables and Reduction of Two-input FLC to NLFC

Reference [61] suggests that a two-input FLC rule table having skew-symmetric property can be reduced to a SISO non-linearity. In this sub-section, the rationale

[1] $e = V_o - V_{ref}$; $ce = e(k) - e(k-1)$

behind such a simplification is described. Furthermore, it will be explained that for such a simplification, it is sufficient for the FLC rule table to be a Toeplitz matrix and not the more restrictive skew-symmetric matrix, as assumed in [61].

Let us consider the FLC rule bases given in Table 4.1. Let us assume that the input membership functions are symmetrical and have 50% overlap as in Fig. 4.1(a). Due to zero-diagonal Toeplitz-structure of Table 4.1, the set of inputs that contribute to the same output '*r*' form parallel lines (Fig. 4.2(a)) in the x_1-x_2 plane. The number of parallel lines increases with an increase in granularity of the inputs. With infinite granularity, for getting the output '*r*' corresponding to an input set $u=\{x_1, x_2\}$, a single variable '*d*' that represents the signed distance of the parallel line (in which the set '$u=\{x_1, x_2\}$' lies) from the leading diagonal '*diag*' (4.1) (refer Fig. 4.2(b)) in the x_1-x_2 plane can be used instead of the two-variable input set $u=\{x_1, x_2\}$.

$$\text{diag}: x_2 + \lambda x_1 = 0 \quad (4.1)$$

In (4.1), 'λ' is the magnitude of slope of that diagonal in the x_1-x_2 plane, whose singleton (membership) value in the rule table is zero (Z). The distance 'd_1' of any input $u_1=\{x_{1,1}, x_{2,1}\}$ from the leading diagonal can be obtained as

$$d_1 = \frac{x_{2,1} + \lambda x_{1,1}}{\sqrt{1+\lambda^2}}. \quad (4.2)$$

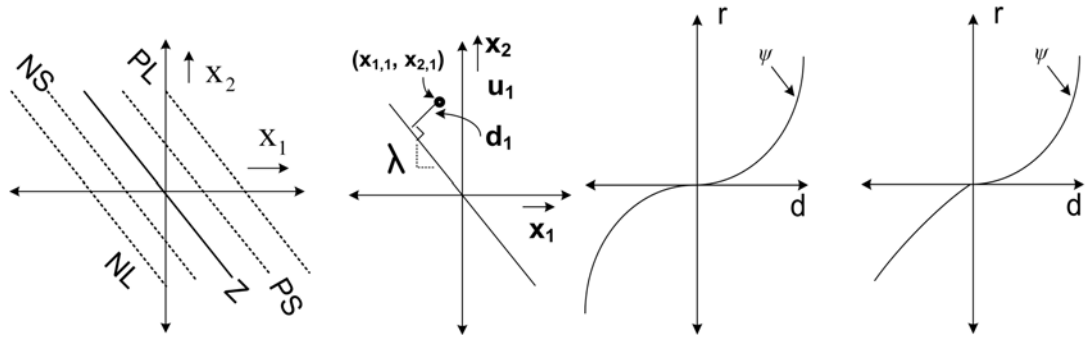
The non-linear property of FLC is preserved by the non-linear function ψ that maps the distance '*d*' in x_1-x_2 plane to its singleton (membership) value *'r'* (refer Fig. 4.2(c)). Consequently, the output of FLC with the assumption of an infinite granularity is given by

$$r = \psi(d) \quad (4.3)$$

Thus, the two-input FLC rule table is reduced to a SISO "**Non-Linear Function Controller (NLFC)**." It must be noted that this reduction is based on linear

interpolations of the output membership functions in the rule table. Hence, it is only an approximation of the FLC rule table with close matches at the vertices (rules) defined in the rule table. However, as FLCs themselves are based on expert knowledge of system that is not quantified, such an approximation is justified.

An odd non-linearity like the one in Fig. 4.2(c) is obtained by reduction of a skew-symmetric rule-table. In cases, when the rule table is not skew-symmetric but is only a Toeplitz matrix (with zero diagonal), simplification of rule-table into SISO non-linearity is still possible. However, the resulting non-linear function will not have an odd symmetry (refer. Fig. 4.2 (d)).



(a) (b) (c) (d)

Fig. 4.2. (a) Output membership functions in x_1-x_2 plane (b) converting inputs from x_1-x_2 plane to d-r plane (c) mapping a skew symmetric rule table in d-r plane (d) mapping of a non-skew symmetric rule table in d-r plane.

4.3 NLFC- The Economical and Fast "FLC" and its Circuit Realization

The reduction of multi-input complex rule table into a single non-linearity 'ψ' simplifies the circuit realization. Even with digital implementation, the computational overhead on the processor is significantly reduced. A simple analog circuit in which

the non-linearity is divided into several piecewise sections with each section realized by two resistors and a diode is shown in Fig. 4.3(a) [62]. Thus, even large FLC rule tables that need more granularities can be realized with the addition of a few components. It should be noted that this circuit realizes *'-ψ.'* The various slopes and threshold voltages are given below.

$$V_1 = -\frac{R_3}{R_4} V_{cc}^{-};\ V'_1 = -\frac{R'_3}{R'_4} V_{cc}^{+} \tag{4.4}$$

$$V_2 = -\frac{R_5}{R_6} V_{cc}^{-};\ V'_2 = -\frac{R'_5}{R'_6} V_{cc}^{+} \tag{4.5}$$

$$G = -\frac{R_2}{R_1}; G_1 = -\left(\frac{R_2}{R_1} + \frac{R_2}{R_3}\right); G_2 = -\left(\frac{R_2}{R_1} + \frac{R_2}{R_3} + \frac{R_2}{R_5}\right) \tag{4.6}$$

$$G'_1 = -\left(\frac{R_2}{R_1} + \frac{R_2}{R'_3}\right); G'_2 = -\left(\frac{R_2}{R_1} + \frac{R_2}{R'_3} + \frac{R_2}{R'_5}\right) \tag{4.7}$$

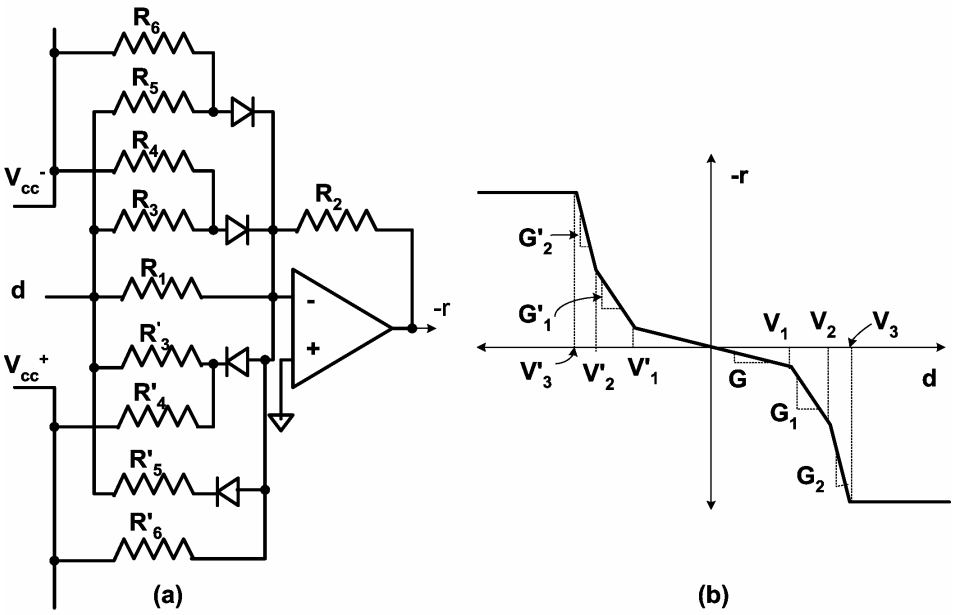


Fig. 4.3. Cheap and Fast "FLC" (a) circuit realization (b) simulated non-linearity '-ψ'.

The circuit in Fig. 4.3(a) realizes an NLFC with the magnitude of slope

increasing with that of '*d*.' To realize a non-linearity with both increasing and decreasing slopes, a combination of circuits in Figs. 4.3 and 4.5 (pre-processing circuit) may be used. Besides being simple and economical, the NLFC implemented using the circuit in Fig. 4.3 will have fast response which is desirable in power converter control applications.

4.4 Handling Asymmetrical Input Membership Functions

In the case of asymmetric triangular input sets [54] as in Fig. 4.4(a), pre-processing of inputs may be needed prior to processing using (4.2) and (4.3). This can be explained with the help of an example. At a normalized value of input '*x = 0.5*,' rules related to *PM* alone are fired in the FLC in Fig. 4.4(a). On the other hand, rules related to both *PS* and *PM* are fired in the FLC with symmetrical input sets for '*x = 0.5*,' (Fig. 4.4(b)). This will result in a large error in the de-fuzzified value, especially when the vertices of the asymmetrical sets are far apart. The error in such cases can be reduced if the set of vertices *{-1, -0.5, -0.2, 0, 0.2, 0.5, 1}* of the asymmetrical sets are mapped to those *{-0.75, -0.5, -0.25, 0, 0.25, 0.5, 0.75}* in the symmetrical sets (refer Fig. 4.4(c)). This 'pre-processing,' although may not be essential in most cases, if unavoidable, may be realized (with a sign inversion) using the circuit in Fig. 4.5 [62]. Here, only the positive half of the mapping is shown. The various slopes and thresholds of this circuit are given by (4.8) and (4.9). It must be noted that if all the inputs of an FLC have similar asymmetric memberships, the pre-processing circuit may be avoided. An example for this will be given in later in this chapter.

$$V''_1 = \frac{R''_3}{R''_4} V_{cc}^{+} \quad ; \quad V''_2 = \frac{R''_5}{R''_6} V_{cc}^{+} \tag{4.8}$$

$$G'' = -\frac{R_2}{R_1}; G''_1 = -\frac{R_2 \parallel R_3}{R_1}; G''_2 = -\frac{R_2 \parallel R_3 \parallel R_5}{R_1} \tag{4.9}$$

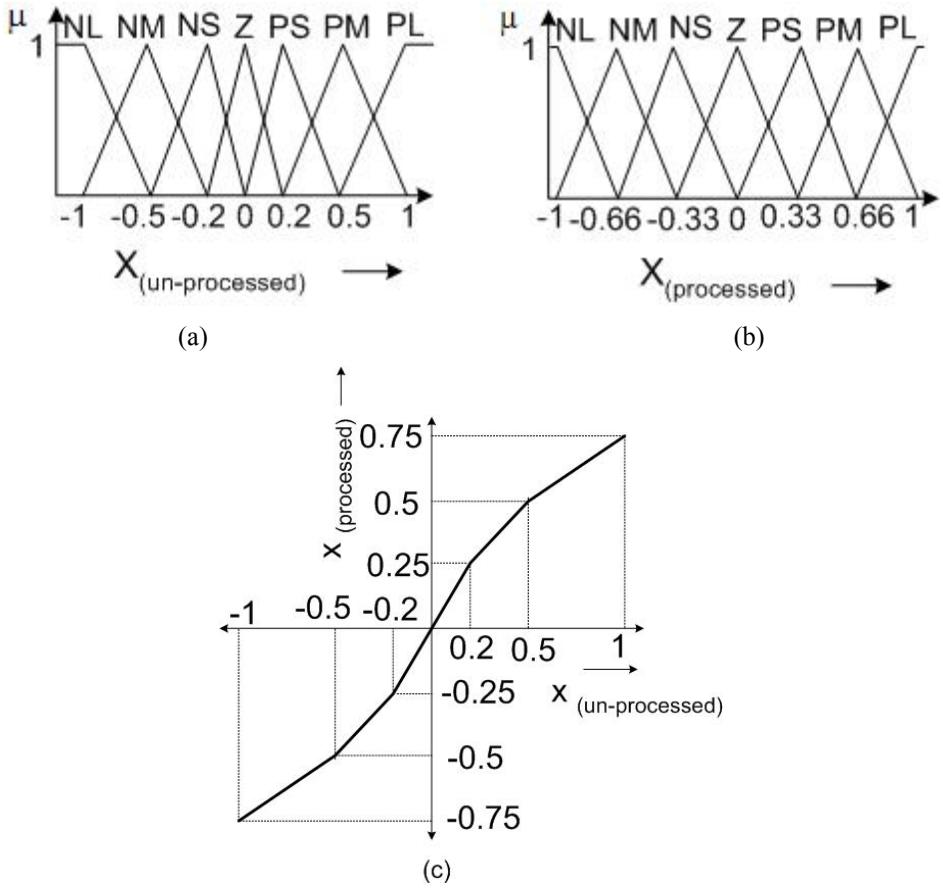


Fig. 4.4. Membership functions (a) asymmetrical (b) symmetrical (c) mapping.

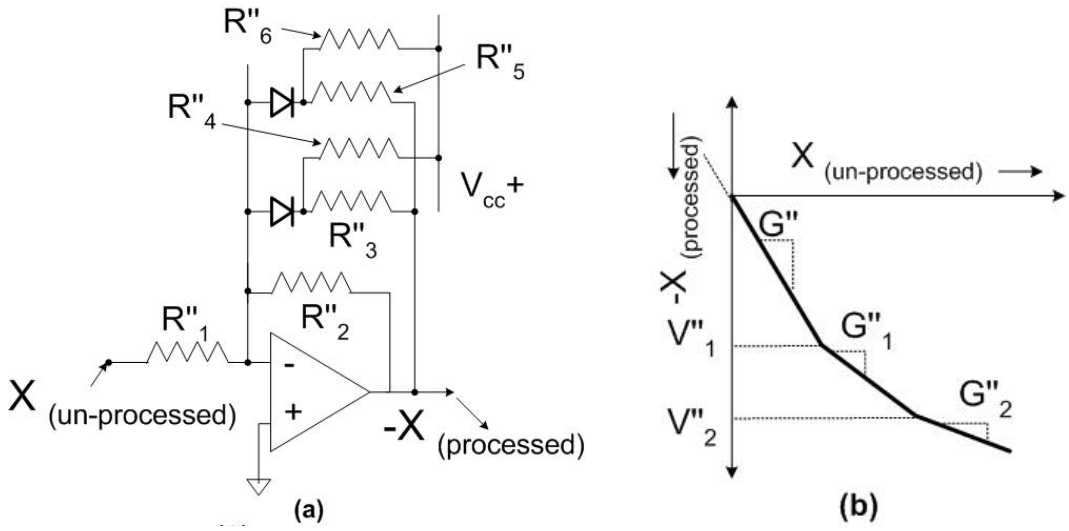


Fig. 4.5. Preprocessing circuit (a) realization (b) mapping.

Fig. 4.6 shows a comparison of a two-input FLC and an NLFC. It may be noticed that the proposed simplification of FLC to NLFC reduces the complexity of FLC algorithm involving fuzzification, inference from rule table, and defuzzification processes.

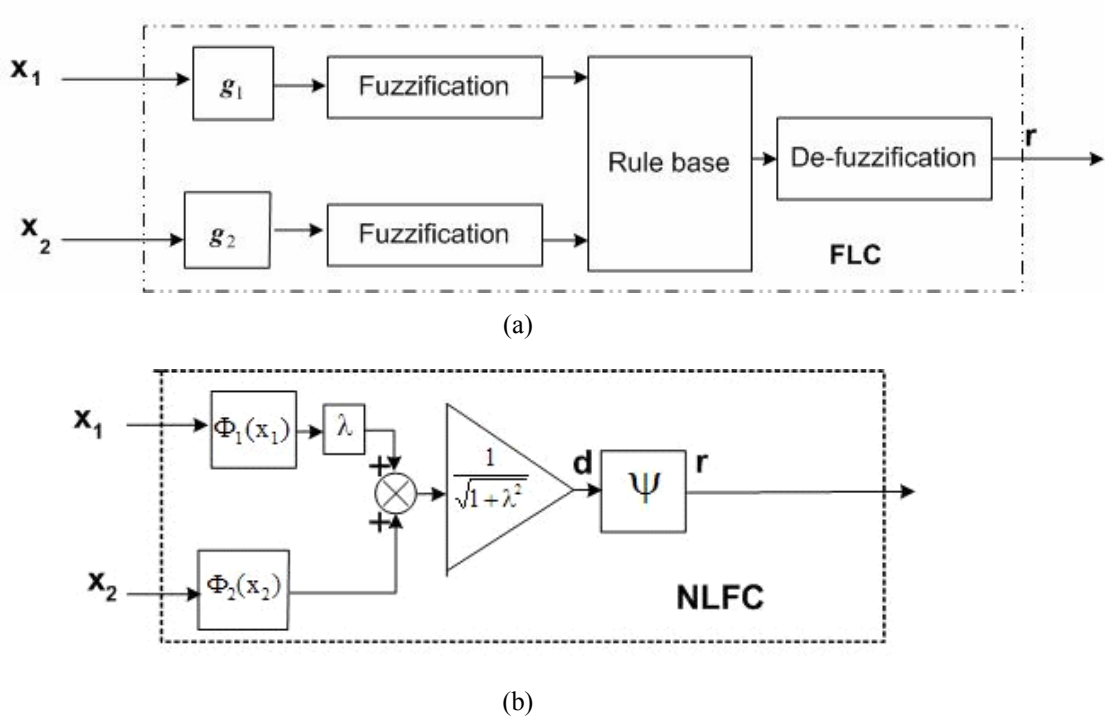


Fig. 4.6. Comparison of FLC to NLFC (a) FLC (b) NLFC.

To summarize, an FLC and its simplified form NLFC will deliver a near-similar output under the following conditions.

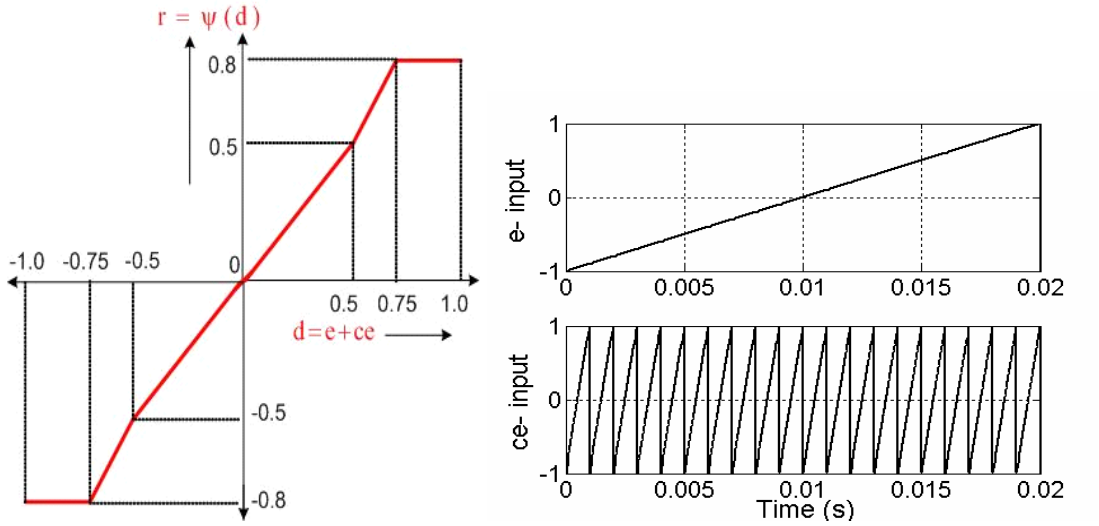
- Input membership functions are symmetrical/asymmetrical triangular with 50% overlap. Preprocessing circuit may be needed to map the asymmetrical inputs to symmetrical ones.
- Output membership functions are symmetrical/asymmetrical triangular with 50% overlap as in Mamdani-type FLCs or singletons as in Sugeno-type FLCs.
- The rule table is a Toeplitz or a near-Toeplitz matrix.

With FLCs satisfying the above three conditions, there will be closer match of the outputs of FLC and NLFC at the points (rules) defined in the rule table. The overall rule surface generated by FLC to that produced by NLFC will be closer with the degree of closeness depending upon the fuzzy operators (AND, OR) and defuzzification (centroid, centre of sums) employed. Investigation of simplification in case of FLCs violating the above conditions is beyond the scope of this thesis, as most of the FLCs implemented with power converters for which details are available [19]-[25], [54]-[61] satisfy the above two conditions.

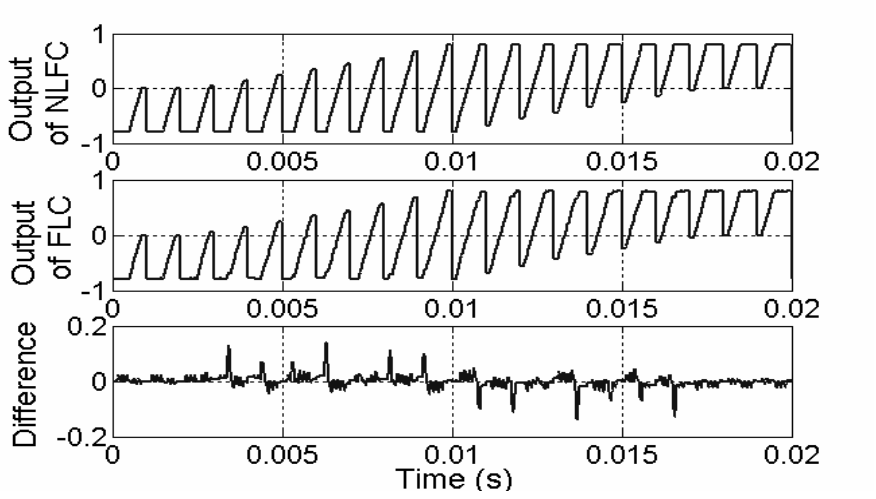
4.5 Verification of Equivalence Between NLFC and FLC

To demonstrate the simplicity of NLFC and its near-similarity to the two-input FLC having a Toeplitz rule-table, the Mandani-type FLC implemented to control a dc-dc boost converter in [20] is considered. Table 4.1 represents rule table with inputs 'x_1' and 'x_2' replaced by output voltage error 'e' and change-in-error 'ce' respectively. The input and output membership functions are symmetrical and are similar to the one represented in Fig. 4.4(b) upon normalization. Hence, pre-processing gains are not needed in the NLFC realized. The processed input 'd' (4.2) of NLFC may be verified to be the addition of 'e' and 'ce' inputs ($\lambda=1$). The non-linear function 'ψ' is shown in Fig. 4.7(a). It must be noted that the gain $1/\sqrt{1+\lambda^2}$ has been integrated with the non-linear function 'ψ.' Up to $|d|=0.5$, the output 'r' follows the input. Due to trapezoidal end-sets (in the output set), the output 'r' is limited to ± 0.8 (when *PL* or *NL* alone is fired). The presence of trapezoidal sets and saturation have been taken into account by a change in the slope of 'ψ' beyond $|d|=0.5$ and by saturation of output 'r' at ± 0.8 for $|d|>0.75$. Fig. 4.7(c) shows the simulated outputs of FLC and NLFC when excited with inputs (Fig. 4.7(b)) spanning the entire *e-ce* plane. By and large, the difference

between the two outputs is negligible, thereby suggesting NLFC as a simple and cost-effective alternative to the two-input FLC.



(a) (b)



(c)

Fig. 4.7. Equivalence of NFLC & FLC (a) NLFC- Function mapping (b) Inputs to NLFC & FLC (c) Outputs of NLFC & FLC and their difference.

4.6 NLFC : Performance Analysis

In this section, the NLFC concept is applied to a large class of FLCs known as PI-FLCs [23]. PI-FLCs are FLCs in which the inputs to the controller are the error '*e*' and change-in-error '*ce*' of the plant's output (state) variable (refer Fig. 4.8(a)). The

simplified from of PI-FLC, when applying the NLFC concept yields the **Non-Linear PI Controller** (NPIC), which is introduced in this section. A discussion on the converter's dynamic-response enhancement follows this. The structure of NPIC is also used explain the rationale behind the excellent large-disturbance handling capabilities of PI-FLCs.

4.6.1 NPIC/PI-FLCs Versus Linear-PI Controllers

In a PI-FLC, the inputs are error 'e' and change-in-error 'ce.'

$$x_1 = e; x_2 = ce \tag{4.10}$$

The above inputs are fed to the FLC block to compute the incremental control action 'Δd,' which is further integrated to get the actual plant control. This integration involved in post-processing imparts the name 'PI-FLC' to the controller.

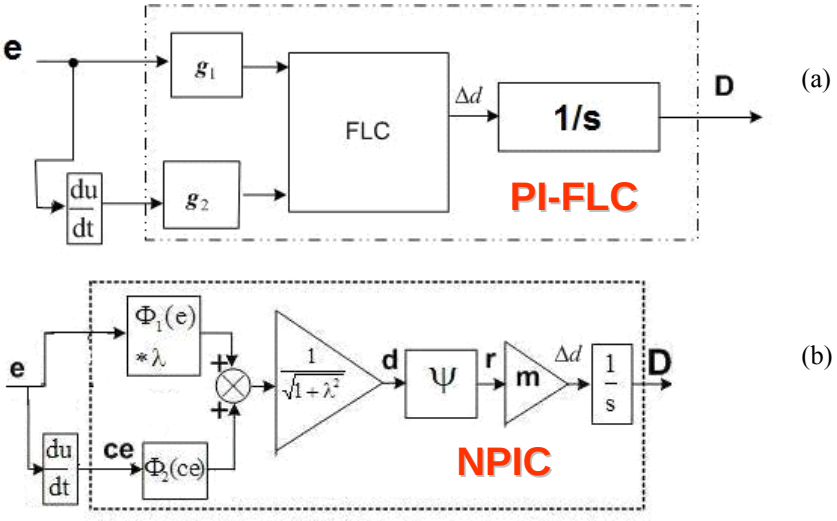


Fig. 4.8. Schematic diagrams (a) PI-FLC (b) NPIC.

The simplified form of such a PI-FLC based on NLFC-concept, namely NPIC is shown (inside the dotted block) in Fig. 4.8(b). The structure of NPIC has been derived from Fig. 4.6(b). The processed input 'd' in NPIC (Fig. 4.8(b)) is obtained using (4.11) (derived from (4.2)) and fed to the non-linearity ψ.

$$d = \frac{\Phi_2(ce) + \lambda\Phi_1(e)}{\sqrt{1+\lambda^2}} \tag{4.11}$$

The output '*r*' of ψ is multiplied by a gain '*m*' and then integrated to get the actual plant control input '*D.*'

Fig. 4.9(a) shows a system schematic in which an NPIC is used to control a power converter. The 'filter' block is used to filter the switching noise of the converter. For the sake of simplicity, let the input membership functions be assumed to be symmetrical with 50% overlap. Hence, $\Phi_1(e)$ and $\Phi_2(ce)$ are replaced by '*e*' and '*ce.*' To show the similarity between NPIC scheme and linear-PI controller, let us consider a linear-PI controller given by

$$T_c(s) = \frac{D(s)}{e(s)} = K_1 \cdot \frac{\frac{s}{K_2}+1}{s} \tag{4.12}$$

$$\Rightarrow D(s) = \left(\frac{s.e(s)}{K_2} + e(s)\right).\frac{K_1}{s} \tag{4.13}$$

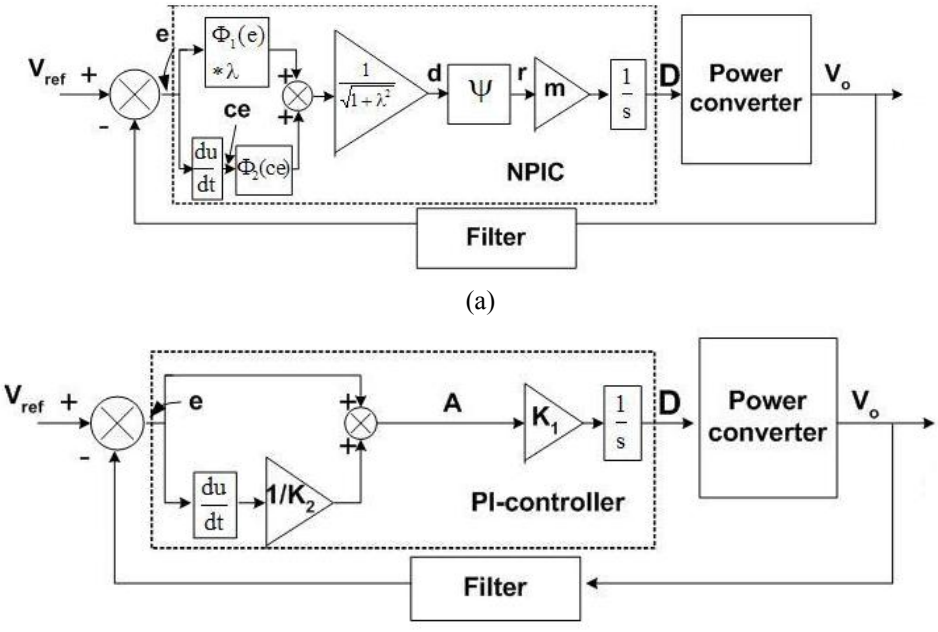


Fig. 4.9. Power converter control schematic (a) with NPIC (b) with linear-PI controller

The first term in (4.13) represents the addition of error and its derivative (change-in-error) with a gain. The system schematic with PI controller in Fig. 4.9(b) has been drawn using (4.13). This scheme is structurally similar to NPIC-based scheme (Fig. 4.9(a)). This structural similarity between NPIC and linear-PI controller is advantageously used in obtaining good small-signal performance. The following section explains the associated design steps.

4.6.2 Transient Performance Improvement in NPIC

Linear-PI controller designed at an operating point generally offers a good small-signal transient performance at the designed operating point. Such a good transient performance can also be achieved using NPIC/PI-FLC, if the NPIC is designed to mimic the PI controller for low values of input *'d.'* This is achieved by

1. setting the parameters 'λ' and 'm' of NPIC as given by (4.14) and (4.15),
2. setting the slope of non-linearity 'ψ' to unity (near the origin)
3. replacing preprocessing gains $\Phi_1(e)$ and $\Phi_2(ce)$ by unity (under the conditions defined in sub-section 4.4).

In many control applications, as the normalizing gain given to change-in-error input is generally small, it may be assumed that $\lambda >> 1$.

$$\lambda >> 1 \Rightarrow \sqrt{1+\lambda^2} \approx \lambda; \lambda/\sqrt{1+\lambda^2} \approx 1; \lambda \approx K_2 \tag{4.14}$$

$$m = K_1 \tag{4.15}$$

For higher values of input *'d,'* i.e for large disturbances, the equivalent gain of NPIC/PI-FLC is set high. This changes the control input to the power converter at a rate faster than that in the linear-PI controller. As a result, NPIC/PI-FLC is capable of delivering good transient performance for large disturbances. Similar to the design of

a two-input FLC, the non-linearity 'ψ' at various values of input *'d'* is determined from knowledge of the system behavior and is corrected using computer simulations.

It should be noted that at an operating point different from the design operating point, similar to a PI controller, the NPIC/PI-FLC also does not guarantee a good small-signal transient response. Adaptive tuning [23] may be needed in such a case.

4.7 Example System and NPIC/PI-FLC Description

Based on a benchmark-PI controller, an NPIC has been designed, simulated and a hardware model has been built and tested on a single-switch dc-dc boost power converter. This sub-section describes the converter and controller specifications.

4.7.1 Boost Converter Specifications

A single-switch dc-dc boost power converter shown in Fig. 1.1 and with the specifications given in Table 3.1 has been considered as an example system. The other parameters of the converter are ESR of *L = 0.2 Ω, ESR of C = 0.15 Ω*, MOSFET ('S') '*ON*' resistance = *0.115 Ω*, and diode forward voltage drop = *0.8 V*.

Neglecting the effect of parasitics, at a given operating point, the small-signal control-to-output-voltage transfer function of the boost converter (operating in continuous conduction mode (CCM)) can be verified as

$$\frac{V_o(s)}{D(s)} = \frac{\mathrm{V_s}}{(1-D)^2} \frac{\left(1 - s\dfrac{L}{R(1-D)^2}\right)}{1 + s\dfrac{L}{R(1-D)^2} + s^2\dfrac{LC}{(1-D)^2}}, \qquad (4.16)$$

where D = duty ratio (control input) at the operating point, V_s = supply voltage, V_o = output voltage, R = load resistance. The transfer function in (4.16) is a repetition of

(2.1). The above transfer function is used in designing a benchmark PI controller that offers a good small-signal response, based on which the NPIC/PI-FLC is derived.

4.7.2 NPIC/PI-FLC Description

A benchmark PI controller that delivers good small-signal transient performance at V_s=*15 V*, and *R=33 Ω*, has been designed. The design of PI controller is based on small-signal model of the boost converter. The controller has been tuned further on the hardware prototype model to offer good small-signal transient performance. The benchmark PI controller obtained accordingly is given by

$$T_c(s) = 3.4 \cdot \frac{\frac{s}{1000} + 1}{s}. \tag{4.17}$$

The parameters of NPIC that has an identical small-signal behavior as that of the benchmark PI controller are obtained using (4.14) and (4.15). They are as follows.

$$\lambda = K_2 = 1000 \tag{4.18}$$

$$m = K_1 = 3.4 \tag{4.19}$$

The cut-off frequency of filters in Figs. 4.9(a) and 4.9(b) is 10 kHz. The differentiator block is approximated by a transfer function with a zero at the origin and a pole at 3500 Hz.

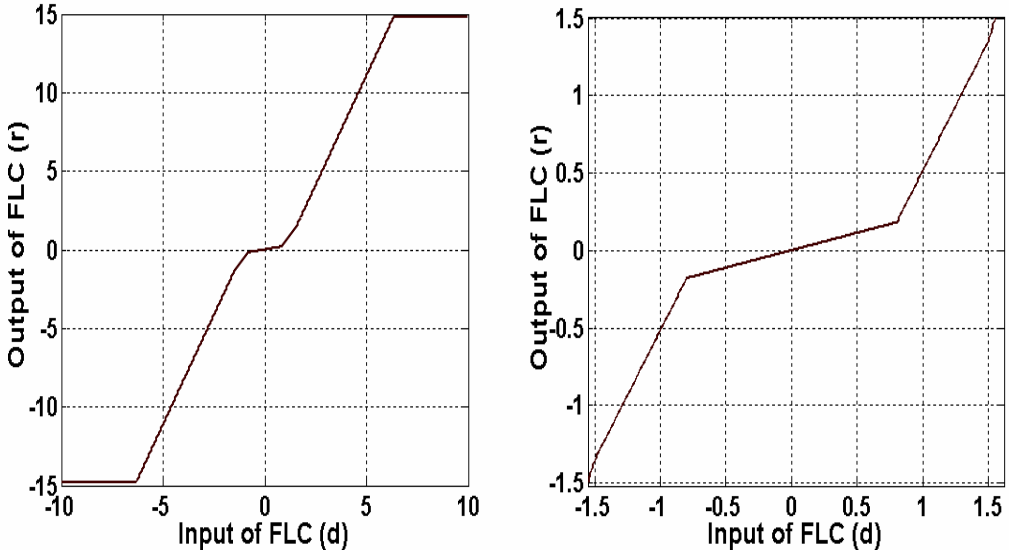
The small-signal model of the system described by (4.16) is valid only for small range of variations '*ΔD*' of the control input '*D*' around the operating point. This range '*ΔD*' decides the input range of the NPIC beyond which the non-linearity '*ψ*' will have a gain higher than unity. Input voltage perturbations that account for a *ΔD* of *0.015* were carried out on the boost converter model with PI controller (Refer Fig. 4.9(b)) using MATLAB-SIMULINK [63]. With such perturbations, the signal at '*A*'

had a maximum variation of *0.8* units. Hence, the non-linearity 'ψ' will have a unity gain until the magnitude of its input *'|d|'* is *0.8 units*. Beyond $|d| = 0.8$, the non-linearity 'ψ' is tuned by simulations on the NPIC-boost converter closed-loop model (see Fig. 4.9(a)) using input voltage perturbations of different magnitudes.

In the hardware implementation, as the gain 'ψ' is high at higher values of inputs, many times, op-amp saturation was found to hinder the realization of the desired non-linearity. To avoid this, the gain of non-linearity has been reduced by a factor (=1/4.44) and appropriately compensated by an increase in the output gain 'm' which is realized in the integrator stage. The corrected value of m is given by

$$m = 4.44 * 3.4 \approx 15.1 \tag{4.20}$$

The non-linear function (ψ) mapping from *'d'* to *'r'* is shown in Fig. 4.10. Here, it can be seen that the gain at origin is no longer unity but is reduced to 0.225 (=1/4.44).



(a) (b)

Fig. 4.10. Non-linear function ψ mapping of SISO-FLC (a) the overall function with saturation (b) the mapping zoomed near the origin.

4.8 Deriving the Equivalent PI-FLC from NPIC

In this section, a PI-FLC that is equivalent to the NPIC designed in the previous section is presented. Simulation results are presented that demonstrate the similarity between the two controllers.

4.8.1 PI-FLC Equivalent to NPIC

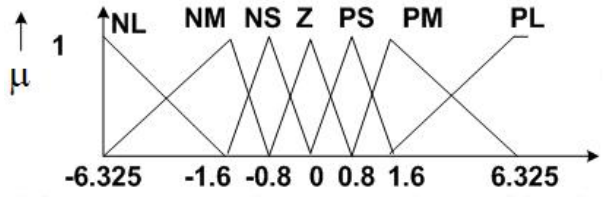
To derive a PI-FLC that approximates the designed NPIC, the input range *('d')* of nonlinearity *'ψ'* of NPIC *(-6.325 to +6.325)* has been divided into 5 piece-wise sections namely *(-6.325 to -1.6, -1.6 to -0.8, -0.8 to 0.8, 0.8 to 1.6, and 1.6 to 6.325).* The inputs to the PI-FLC are the processed error *'e_p' (≈e.)* and processed change-in-error 'ce_p,' *(= $ce/(1+\lambda^2)^{1/2}$, $\lambda = 1000$*).

The range of 'e_p' and 'ce_p' are limited to *±6.325* units. Each of the inputs is divided into seven asymmetrical membership functions as shown in Fig. 4.11(a).

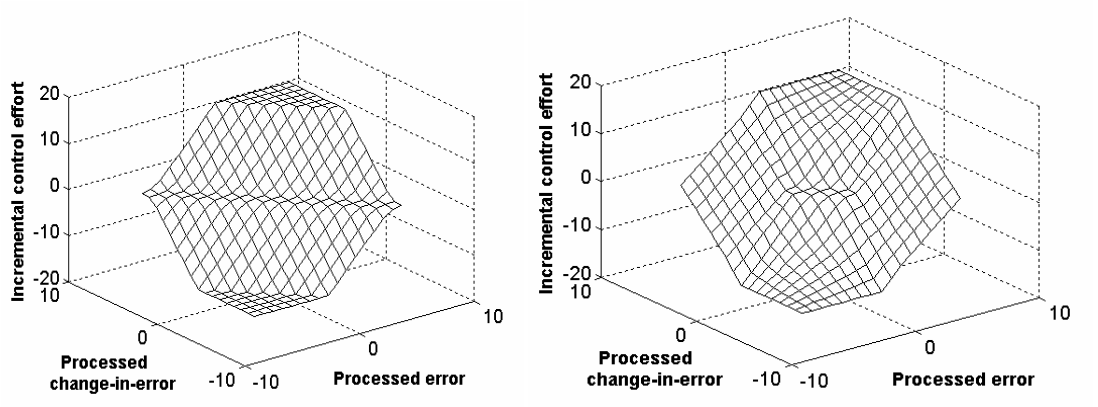
Table 4.4 is the rule table. To generate this table, the value of *'d'* corresponding to different values of inputs e_p and ce_p are found. The singleton value corresponding to the processed inputs e_p and ce_p is the output membership *'r'* in 'ψ' of NPIC corresponding to the computed '*d'* (= $ce_p + e_p$). It must be noted that since the membership functions in the inputs have the same asymmetry, additional pre-processing circuits have been avoided as mentioned in section 4.4.

TABLE 4.4. RULE TABLE OF PI-FLC

e_p / ce_p	NL	NM	NS	Z	PS	PM	PL
PL	0	10.54	12.77	15	15	15	15
PM	-10.54	0	0.18	1.63	3.857	6.085	15
PS	-12.77	-0.18	0	0.18	1.63	3.857	15
Z	-15	-1.63	-0.18	0	0.18	1.63	15
NS	-15	-3.857	-1.63	-0.18	0	0.18	12.77
NM	-15	-6.085	-3.857	-1.63	-0.18	0	10.54
NL	-15	-15	-15	-15	-12.77	-10.54	0



(a)

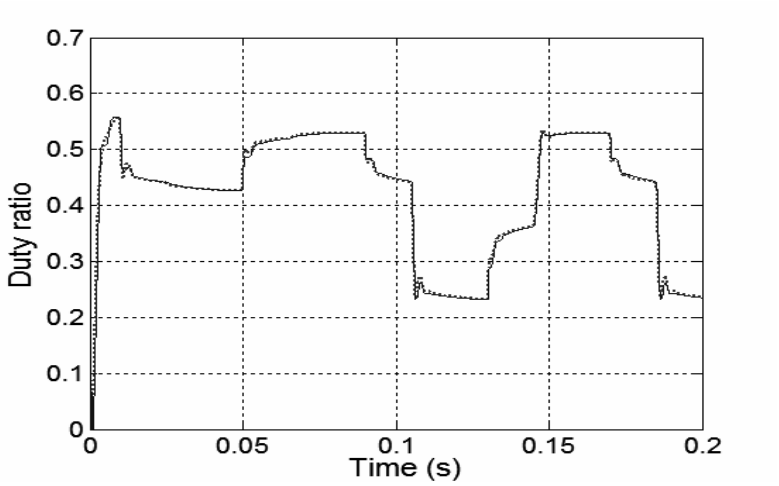


(b) (c)

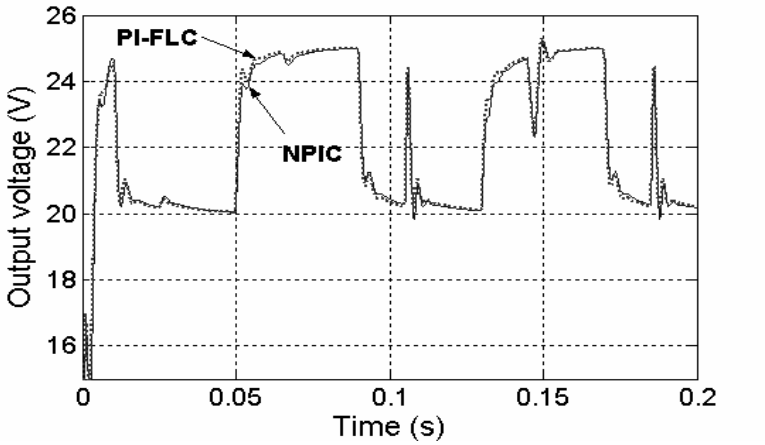
Fig. 4.11. (a) PI-FLC- Input membership functions (b) Input-output relation of NPIC (c) Input-output relation of PI-FLC.

4.8.2 Performance comparison of PI-FLC and NPIC

Figs. 4.11(b) and 4.11(c) show the rule-surfaces of NPIC and PI-FLC. While the output values of the two surfaces are matching at the inputs specified in the rules, at the other values of inputs, the surfaces are reasonably close. To show that the NPIC and PI-FLC offer a nearly equivalent control performance, simulations were carried out on the classical boost converter models controlled by PI-FLC and NPIC for step changes in reference voltage, load resistance, and input voltage. Figs. 4.12(a) and 4.12(b) demonstrate that the transients observed in duty ratio and output voltage are nearly identical in both the cases. Thus it can be concluded that NPIC is a fairly good and simple approximation of PI-FLC.



(a)



(b)

Fig. 4.12. Performance comparison of NPIC and PI-FLC for random disturbances in the power converter; Input voltage transients at 0.025 s, 0.065 s, 0.105 s, 0.145 s, 0.185 s; reference voltage transients at 0.01 s, 0.05 s, 0.09 s, 0.13 s, 0.17 s; load resistance changes at 0.05 s, 0.09 s, 0.13 s, 0.17 s (a) Duty ratio (b) Output voltage legend: '..' PI-FLC, solid line-NPIC.

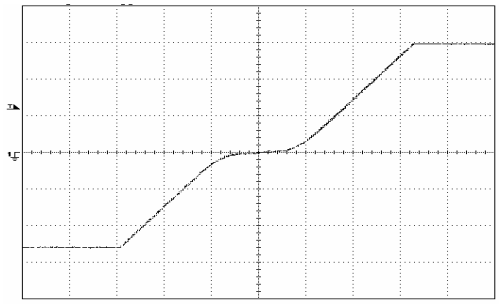
4.9 Experimental Results

In this sub-section, experimental results demonstrating the dynamic performance of NPIC and linear-PI controllers are presented and compared. Figs. 4.13(a) and 4.13(b) show the non-linear function 'ψ' (inverted) of NPIC realized using the circuit in Fig. 4.3(a). Due to diode voltage drops and tolerance of resistors, the break points are not sharp and slightly different from the designed values. However, this does not

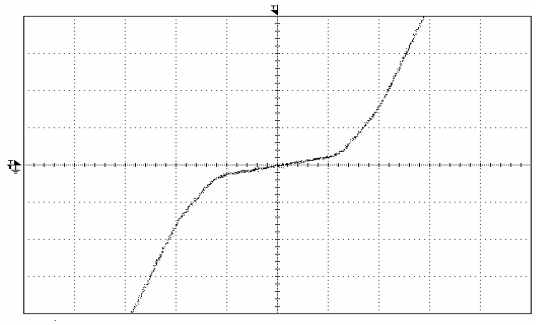
affect the performance of the controller substantially. The values of various components are as below.

$$R_1 = 12\ k\Omega;\ R_2 = 2.7\ k\Omega;\ R_3 = R'_3 = 1.8\ k\Omega$$
$$R_4 = R'_4 = 36\ k\Omega;\ R_5 = R'_5 = 2.2\ k\Omega;\ R_6 = R'_6 = 22\ k\Omega \quad (4.21)$$

The positive and negative saturation levels of the circuit have different magnitudes due to op-amp characteristics. Figs. 4.14 and 4.15 show the experimental responses of the boost converter fitted with NPIC and benchmark-PI controllers respectively for a small step increase in load. Due to the small magnitude of disturbance, as per design, the response is identical in both the cases. Figs. 4.16 and 4.17 show the step responses for a large change in load. The 1% settling time with NPIC is about 6 ms while that with PI controller is about 12.5 ms. This clearly demonstrates the excellent large-disturbance handling capability of NPIC/FLC.



(a)



(b)

Fig. 4.13. Non-linear function ψ - hardware realization; Oscilloscope in xy-mode; (a) overall non-linearity; scale: x-axis (input ‘d’)= 2 V/div, y-axis (output ‘r’) = 5 V/div (b) non-linearity zoomed near the origin; scale: x-axis (input ‘d’)= 1 V/div, y-axis (output ‘r’) = 1 V/div

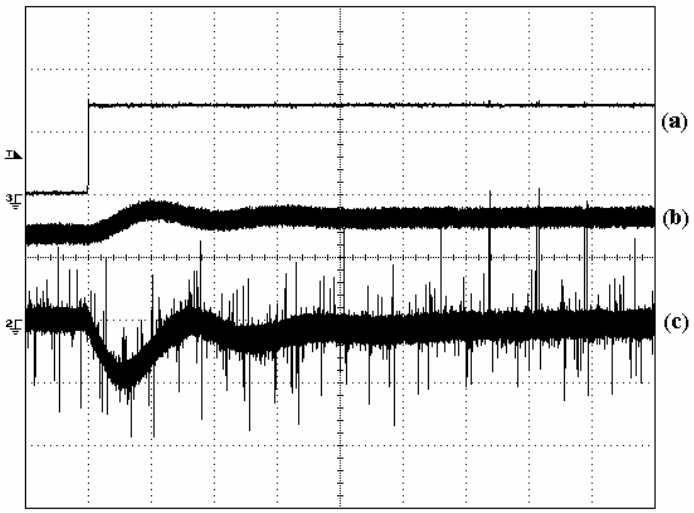


Fig. 4.14. Experimental step response of the converter with NPIC for a step change in load from I_o= 0.75 A to I_o= 0.9 A, at V_s = 15 V, V_o = 25 V (a) Step- marks the instant when the load changes (b) Inductor current (c) Output voltage (oscilloscope channel in ac coupling mode); Scale: voltage: 0.2 V/div, current: 1 A/div, time: 2ms/div.

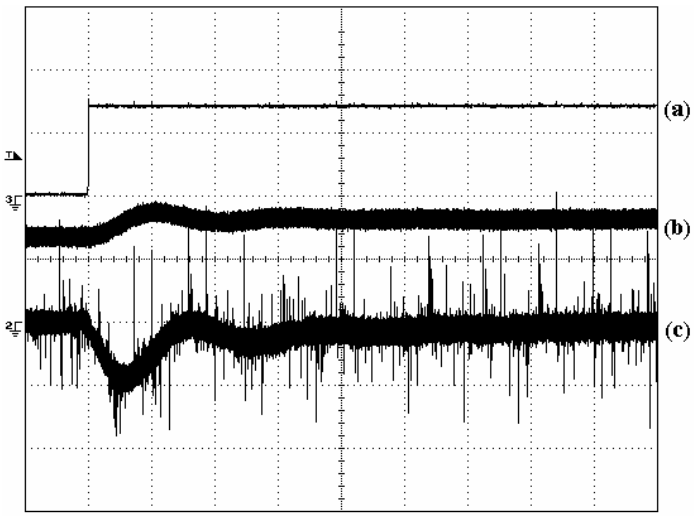


Fig. 4.15. Experimental step response of the converter with PI controller for a step change in load from I_o= 0.75 A to I_o= 0.9 A, at V_s = 15 V, V_o = 25 V (a) Step- marks the instant when the load changes (b) Inductor current (c) Output voltage (channel in ac coupling mode); Scale: voltage: 0.2 V/div, current: 1 A/div, time: 2ms/div.

Figs. 4.18(a) and 4.18(b) show the simulated response of the converter for a large-step change in reference voltage. The response of the converter with PI controller shows a dominant integral action. On the other hand, the response with

NPIC shows a high peak current overshoot. At the expense of high device current stress, the NPIC achieves a settling time smaller than that achieved using the linear-PI controller. Figs. 4.19(a) and 4.19(b) show the corresponding experimental step response. The experimental results agree well with the simulated results.

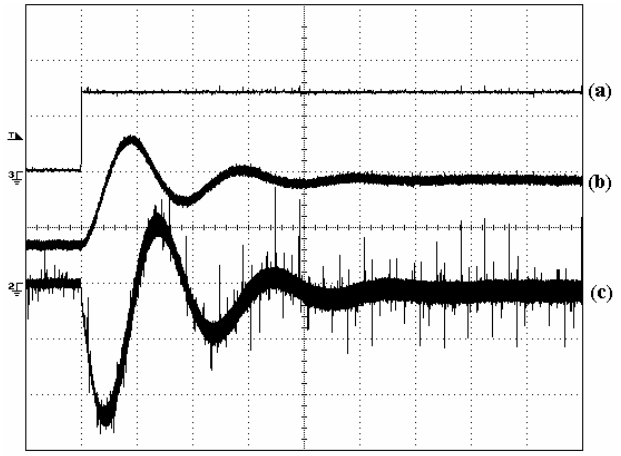


Fig. 4.16. Experimental step response of the converter with NPIC for a step change in load from I_o= 0.75 A to I_o= 2.0 A, at V_s = 15 V, V_o = 25 V (a) Step- marks the instant when the load changes (b) Inductor current (c) Output voltage (oscilloscope channel in ac coupling mode); Scale: voltage: 0.5 V/div, current: 2 A/div, time: 2ms/div.

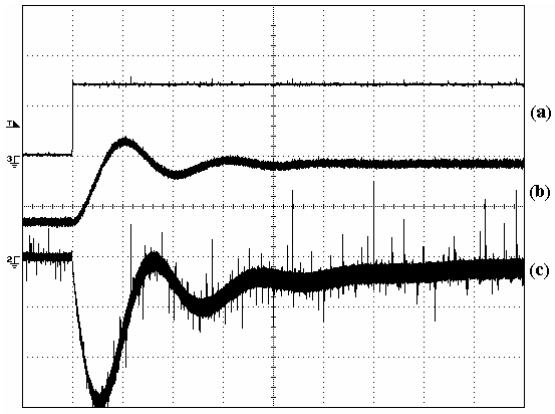
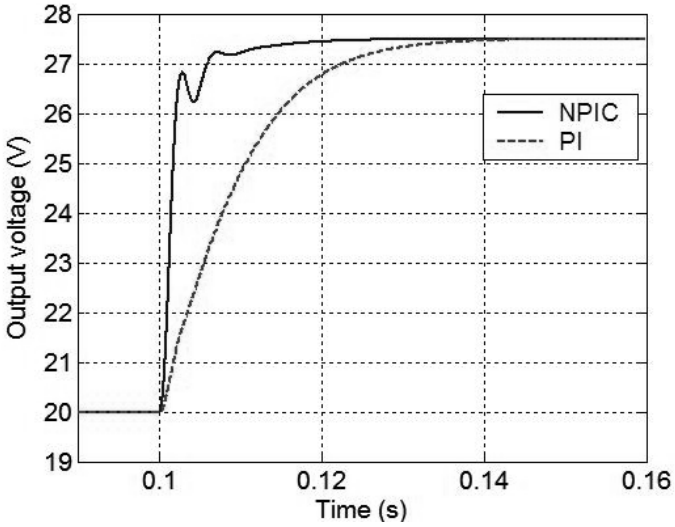
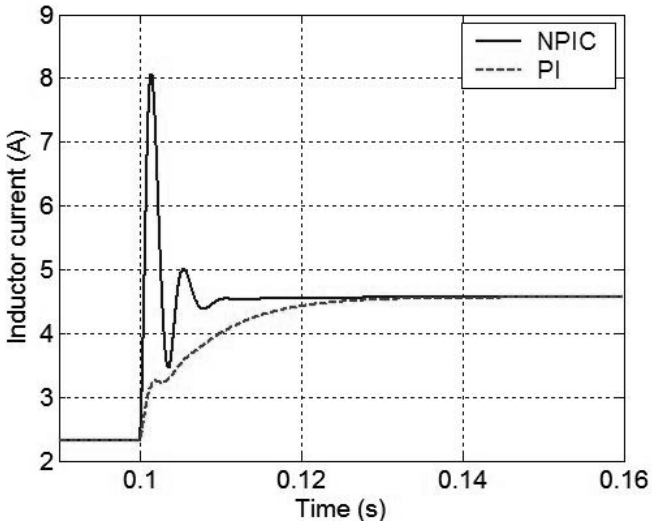


Fig. 4.17. Experimental step response of the converter with PI controller for a step change in load from I_o= 0.75 A to I_o= 2.0 A, at V_s = 15 V, V_o = 25 V (a) Step- marks the instant when the load changes (b) Inductor current (c) Output voltage (oscilloscope channel in ac coupling mode); Scale: voltage: 0.5 V/div, current: 2 A/div, time: 2ms/div.

Figs. 4.20(a) and 4.20(b) show the simulated response of the converter for a step change in input voltage V_s. Once again, the time taken by output voltage to recover back to 25 V in the case of converter with NPIC is smaller than that taken by the converter with PI controller. These results clearly demonstrate the excellent large-disturbance handling capability of NPIC/FLC.

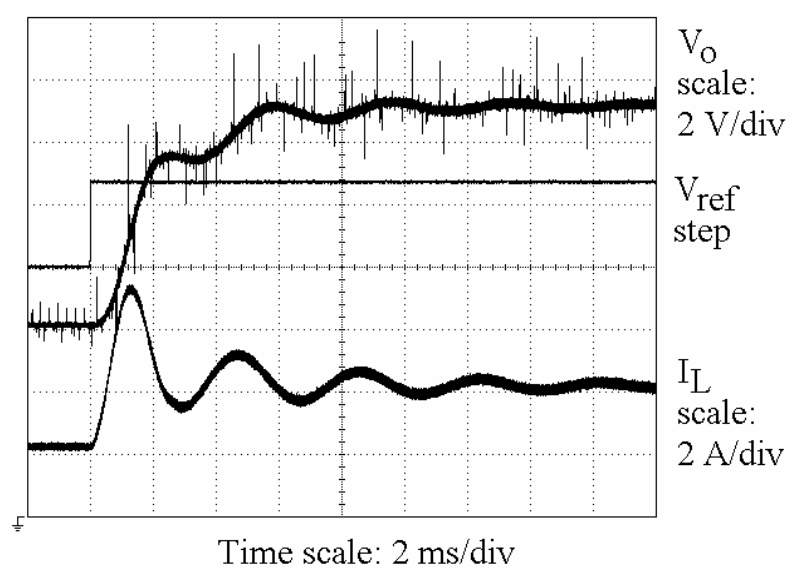


(a)

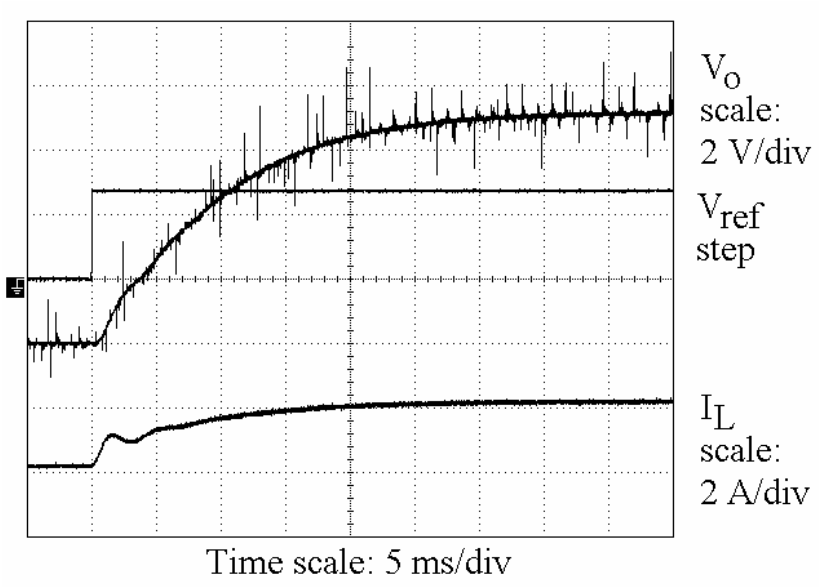


(b)

Fig. 4.18. Simulated step response of the converter with NPIC and PI controllers for a step change in reference voltage from V_{ref} = 20 V to V_{ref} = 27.5 V, at V_s = 15 V, load resistance R = 12.5 Ω (a) output voltage (b) inductor current.

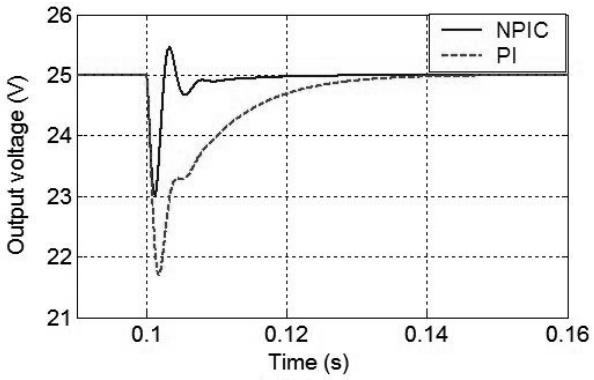


(a)

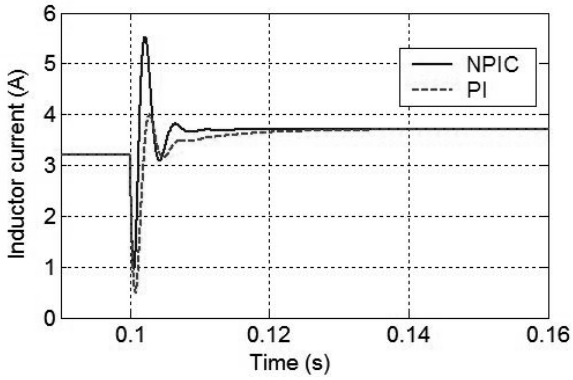


(b)

Fig. 4.19. Experimental step response of the converter with (a) NPIC (b) PI for a step change in reference voltage from V_{ref} = 20 V to 27.5 V, at V_s = 15 V, load resistance R = 12.5 Ω.



(a)



(b)

Fig. 4.20. Simulated step response of the converter with NPIC and PI controllers for a step change in input voltage from V_s = 15 V to V_s = 13 V, at V_{ref} = 25 V, load resistance R = 12.5 Ω (a) output voltage (b) inductor current.

4.10 Stability Analysis of NPIC

Limit cycles have been reported in FLC systems [89] under large transient disturbances. These limit cycles are undesirable sustained oscillations occurring in a system due to the control or state variable hitting its non-linear hard-limits. When limit cycles occur in a power converter, the voltage across the components and device currents are extremely large challenging the life of the power converter. Thus, the study of limit cycles and the conditions under which they are initiated in a converter is essential.

The simplification of PI-FLC to NPIC makes it easy to predict the gain margin *'K'* of the system beyond which limit cycles occur. Such an analysis has been carried out under the maximum loaded conditions ($R = 12.5\ \Omega$, $V_s = 12.5\ V$, and $V_{ref} = 25\ V$) of the boost converter under study and is presented here. In this section, two different aspects of analyzing stability are discussed. The stability analysis presented here is limited to NPICs that don't need input pre-processing.

4.10.1 Gain-Margin without Considering System Non-linearities:

The boost power converter-NPIC system has several non-linearities. The non-linearities in the system include

- Non-linear nature of NPIC including its saturation
- Control input (duty ratio) limitation (from 0 to 0.85)
- Unidirectional inductor current (from 0 to infinity)
- Unidirectional output voltage (from 0 to infinity).

Among the above-mentioned non-linearities, under transient disturbances, the first three non-linearities may become active depending on the magnitude of disturbance. The fourth non-linearity is generally inactive in most cases.

In the present approach of analyzing stability, the non-linearity of NPIC 'ψ' is treated as a simple gain whose value is equal to its slope at the origin of the *d-r* plane. All the non-linearities in the converter and controller are assumed to be inactive and the converter is represented by its small-signal model. Stability analysis is carried out using well-known frequency-domain technique of root locus. The gain margin '*K*' predicted so is valid only for disturbances of infinitesimal magnitude at the operating point considered. For the boost converter-NPIC system under consideration, using

root locus technique, the gain margin '*K*' has been calculated to be equal to 4.9 at the operating point under consideration.

4.10.2 Describing Function Approach- Gain Margin Considering NPIC's Non-linearity

A fairly good prediction of gain margin is expected if the non-linearities listed before are taken into consideration. However, in this sub-section, for the sake of simplicity, the non-linearity of NPIC alone is considered for predicting the gain margin '*K*' at which the system breaks into limit cycles. All the other non-linearities are assumed to be inactive. The NPIC is modeled using describing function method [67], [68]. The describing function '*N(A)*' of NPIC's non-linearity 'ψ' (represented by Fig. 4.10(a)) has been computed using SIMULINK and is shown in Fig. 4.21.

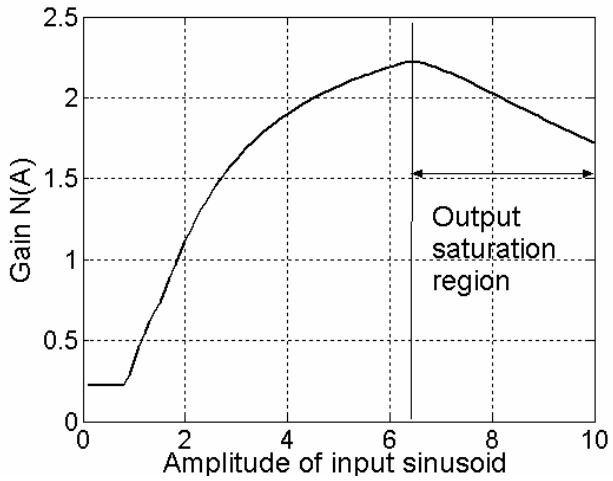


Fig. 4.21. Describing function of NPIC's non-linearity 'ψ' with output saturation.

The Nyquist plot of the rest of the system (*G(s) = converter + filter + preprocessing circuits + other gains*) and negative inverse *(-1/N(A))* of describing function of NPIC are plotted on the same complex frequency plane (refer Fig. 4.22). Any intersection between the two curves predicts the existence of a limit cycle, whose frequency corresponds to the frequency value in the *G(s)* curve. With no intersection

between *G(s)* and *-1/N(A)* curves, the system without any extra gain (*K=1*) is predicted to be stable (Refer curve (b) on Fig. 4.22). Limit cycles at 388 Hz are predicted at a gain '*K=2.3*' at which *G(jw)*K* (curve (a) in Fig. 4.22) touches the *-1/(N(A)* curve.

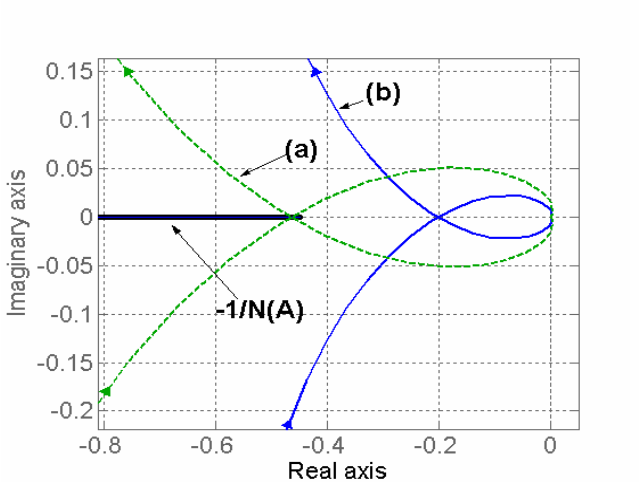


Fig. 4.22. Onset of limit cycles predicted by describing function method; (a) Nyquist plot of G(s)*K (system with the incremental gain 'K') at the verge of instability (b) Nyquist plot of G(s) alone with K=1 (stable).

Although describing function method takes into account the non-linearity of NPIC, it should be noted that the rest of the system (*G(s)*) is assumed to be represented by its small-signal model. Hence, in order to investigate the performance in the actual converter, the gain of NPIC was increased and the converter was switched on. At an extra gain of *3.3*, the converter exhibited limit cycles upon start-up. Fig. 4.23 shows limit cycles observed in the experimental set up. The frequency of limit cycles is about *370 Hz*. It should be seen that while the output of NPIC (incremental control action '*r*') hits its hard limits (op-amp saturations), the other quantities namely the duty ratio, the inductor current, and the output voltage do not hit their corresponding hard-limits.

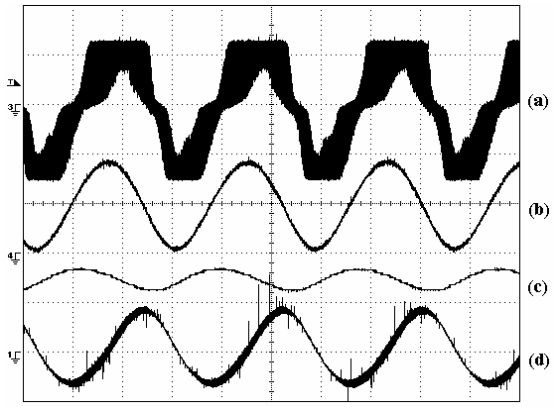


Fig. 4.23. Experimental waveforms showing the converter exhibiting limit cycles at an extra gain of 3.3 (a) Output 'r' of 'ψ' (5 V/div) (b) Inductor current (5 A/div) (c) Duty ratio (0.5 units/div) (d) Output voltage (4 V/div) with channel in ac mode

The discrepancy between gain margin predicted by describing function analysis ($K = 2.3$) and that observed in the experiments ($K = 3.3$) is believed to be attributed to the difference between the small-signal and large-signal models of the converter and to the non-exact modelling of system parasitics. It must be noted that with some disturbances, the other non-linearities in the converter such as duty cycle limits also become active. In such cases, a more detailed analysis may be needed to predict the gain margin.

4.11 Chapter Conclusions

Rule tables of Fuzzy logic controllers (FLCs) of the type typically implemented with power converters have an exact-Toeplitz or near-Topelitz structure. Such an FLC can be reduced to an NLFC which can be realized using fast and inexpensive analog circuitry. NLFC can be easily designed and analyzed when compared to the original two-input FLC. Besides, it also gives an insight into the design of FLCs to offer good dynamic performance in power converters. An example design of NPIC, the simplified form of PI-FLC, from a benchmark-PI controller to offer good transient

response in a classical boost converter has been presented. Experimental results demonstrating the good dynamic performance offered by NPIC have been discussed. A stability analysis to predict the gain margin at which limit cycles occur in the boost converter employing NPIC has been discussed.

With this, the investigation of dynamic performance improvement in boost and buck-boost-derived converters by enhancements in design and control schemes is complete. The rest of the thesis discusses the improvement in dynamic performance by modifications in the converter topology.

CHAPTER 5

NOVEL TRI-STATE CLASS OF BOOST AND BUCK-BOOST-DERIVED CONVERTERS WITH FAST DYNAMICS

5.0 Background

As mentioned in Chapters 1 and 2, classical single-switch boost and buck-boost-derived dc-dc converters operating in CCM suffer from dynamic response problem due to the presence of RHP zero in their small-signal control-to-output transfer-function. The problem is further compounded due to change in operating point which makes the RHP zero move in the complex frequency (s) plane.

Chapters 1 and 2 explained the effect due to the RHP zero in a conventional boost converter in time and frequency domains and the difficulty in achieving good small-signal bandwidth. Designers are generally forced to limit the overall closed-loop bandwidth to a low frequency dictated by the worst-case RHP zero location. Typically the bandwidth is limited to 1/30th of the switching frequency [12].

In this chapter, a novel 'tri-state' class of converters derived from boost and buck-boost-based dc-dc converters is presented. The converters belonging to this tri-state class have an additional degree of control freedom that can be exploited effectively to avoid the dynamic response problem due to the presence of RHP zero occurring in the control-transfer-function of their classical counterparts.

The chapter is organized as follows. The tri-state class of converters will be introduced and the motivation behind the elimination of RHP zero will be explained.

The discussions after this will focus primarily on the tri-state versions of boost and flyback converters. Firstly, the 'tri-state boost' converter and the control freedom offered by the converter are explained. A simple control method that avoids the RHP zero in the control-transfer-function is presented. The steady-state operation and the small-signal model (under the proposed control method) of the converter are also presented. The superior dynamic performance of the converter over the classical boost converter is established through computer simulations and experimental results.

Following the discussions on tri-state boost converter, similar theoretical analysis, and discussions on tri-state flyback converter supported by experimental results are presented.

5.1 Tri-State Class of Converters- Motivation

The time-domain effect of RHP zero in the classical boost converter has been explained in section 2.1. A step increase in duty ratio triggered by a sudden load increase causes the output voltage to dip initially before it starts to rise (Fig. 2.2). This effect of RHP zero can be eliminated and an improvement in the dynamic response of the converter is expected if the 'OFF' interval of the converter is in principle made independent of the 'ON' interval. Such a de-coupling is made possible by introducing an additional 'inductor-free-wheeling interval' in the converter. The class of converters having this additional 'inductor-free-wheeling' interval, on account of the three-state cyclic-steady-state operation (CCM) is named as 'tri-state' class of converters. Fig. 5.1 demonstrates the decoupling of 'capacitor-charging' (OFF) interval from the 'boost' (ON) interval. Any increase in 'boost' interval can be achieved by a corresponding reduction in 'free-wheeling 'interval without having to change the 'capacitor-charging' interval as shown in Fig. 5.1.

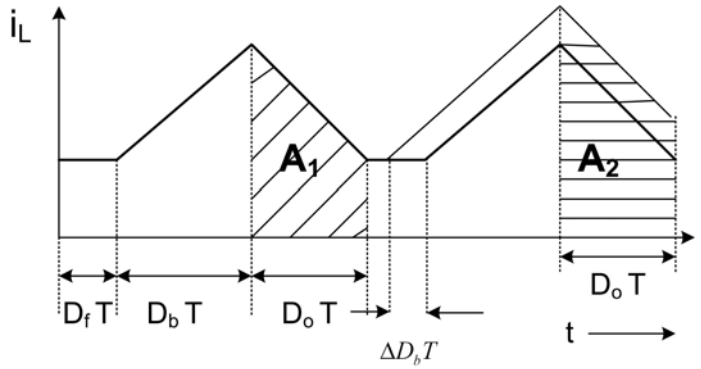


Fig. 5.1 Tri-State class of converters- Motivation

Fig. 5.2 shows the classical versions of popular boost and buck-boost-derived converters and their corresponding 'tri-state' topologies. The additional switch or diode (or both) needed to realize 'tri-state' operation are represented as S_f and D_f .

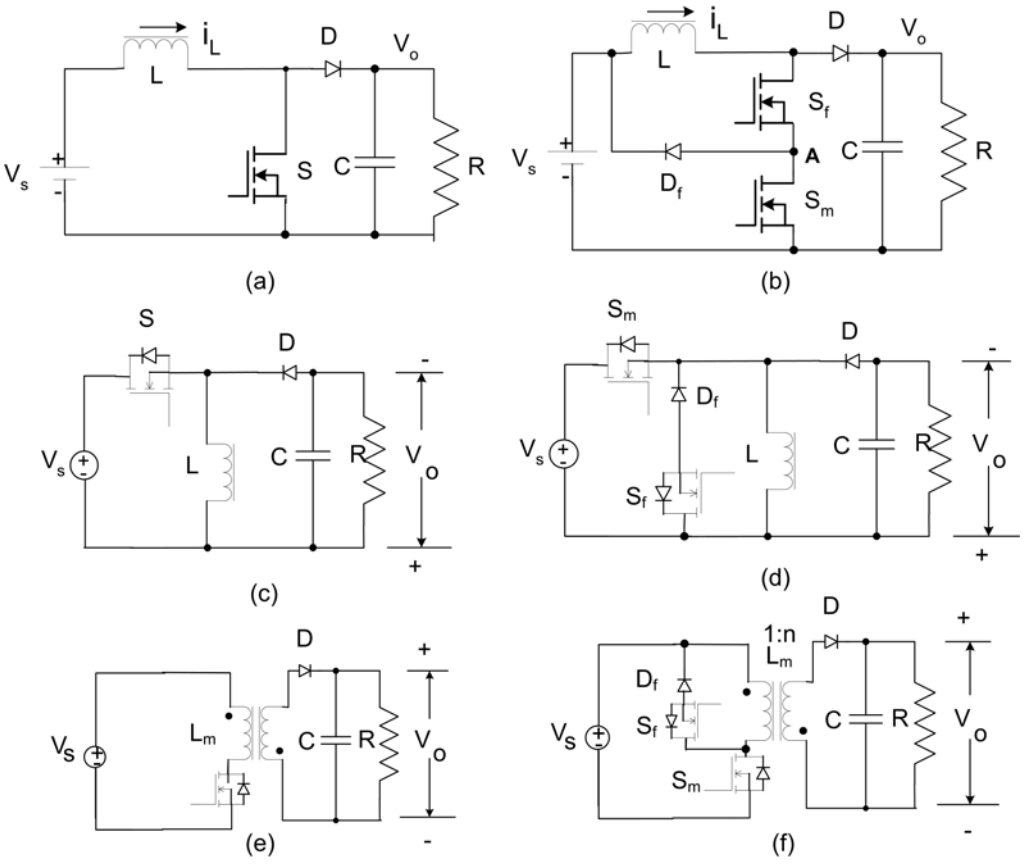


Fig. 5.2 Circuit diagrams of classical and modified tri-state boost and buck-boost-derived power converters (list continues in the next page also. Please refer to the next page for figure captions)

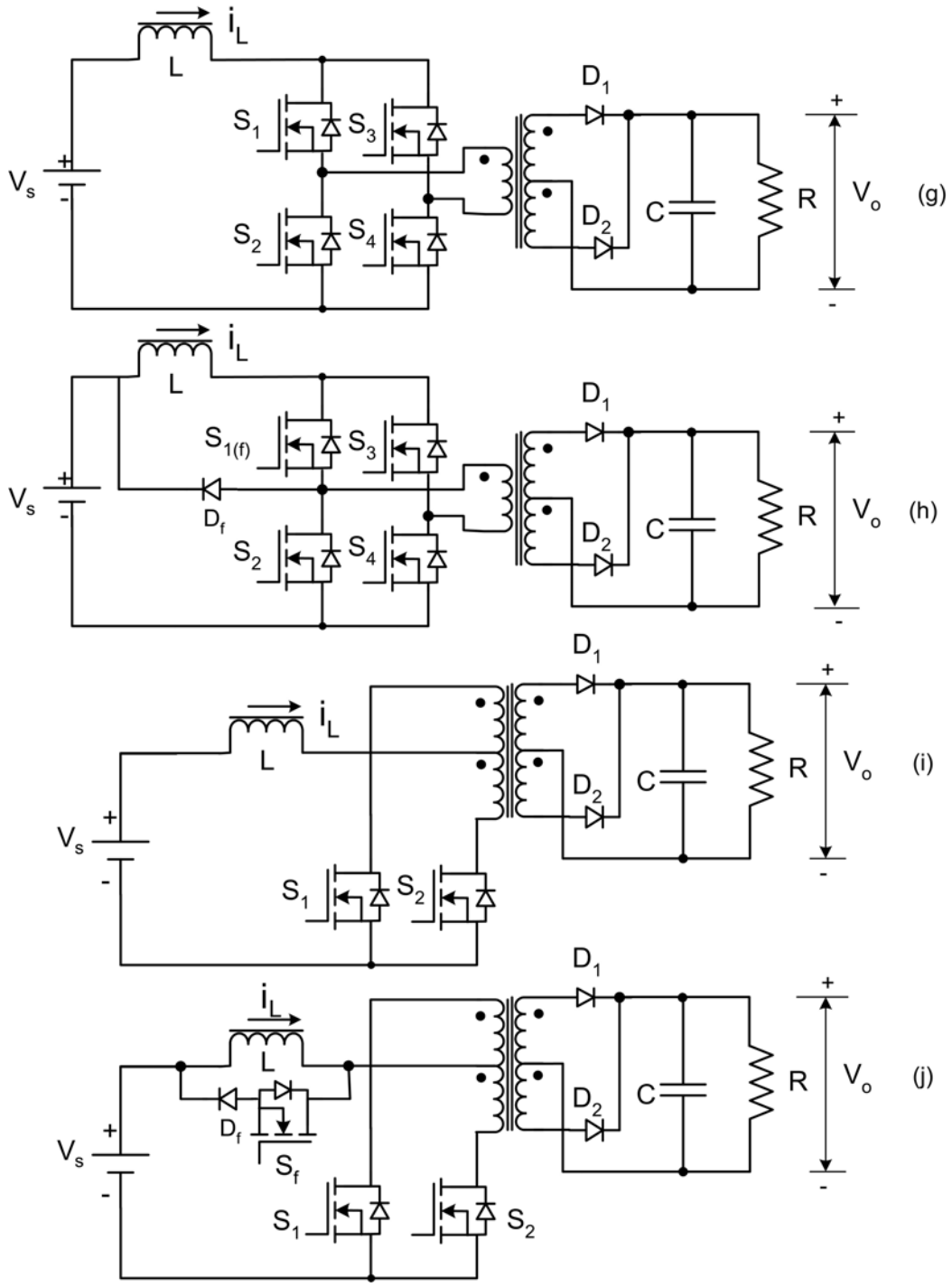


Fig. 5.2 Circuit diagrams of classical and modified tri-state boost and buck-boost-derived power converters (a) Classical boost converter (b) Tri-State boost converter (c) Classical buck-boost converter (d) Tri-state buck-boost converter (e) Classical flyback converter (f) Tri-state flyback converter (g) Classical full-bridge transformer-isolated boost converter (h) Full-bridge transformer-isolated tri-state boost converter (i) Classical push-pull isolated boost converter (i) Push-pull isolated tri-state boost converter.

While the classical versions of boost, push-pull isolated boost, buck-boost, and flyback require both a switch and a diode for realizing tri-state operation, the full-bridge transformer isolated boost converter requires only an additional diode. An existing converter which does not need any additional component is the cascade-buck-boost (CBB) converter (Refer Fig. 5.3), known popularly for its low switch-voltage-stresses. By appropriately controlling the switches S_1 and S_2, an inductor current waveform similar to that in Fig. 5.1 can be obtained. An application of tri-state operation of this converter in single-phase power factor correction will be discussed later in the thesis.

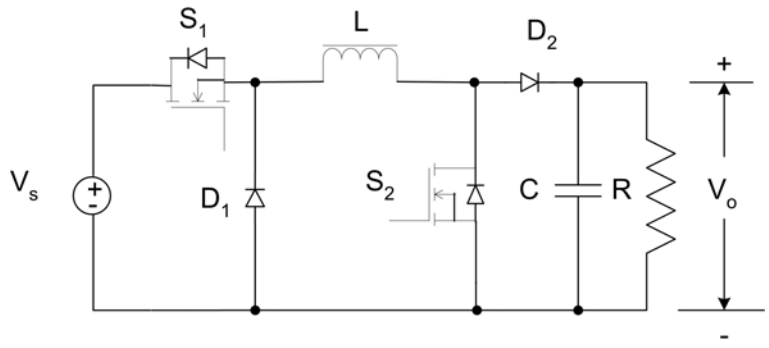


Fig. 5.3 An existing converter with possible tri-state operation- Cascade-buck-boost converter

5.2 Tri-State Boost Converter

In this section, the steady-state operation and small-signal model of tri-state boost converter are presented. Following this, using a simple 'constant-D_o' control scheme, dynamic performance improvement in the converter over classical boost converter is demonstrated through simulation and experimental results.

Fig. 5.4 shows another variation of the proposed tri-state boost converter, different from that in Fig 5.2(b). Though there are differences in the two converters from a practical-implementation point of view, from the control point of view both

converters operate in a similar manner. For example, the switch S_f of the converter shown in Fig.5.4 (Circuit B) carries less current than that of the converter shown in Fig. 5.2(b) (Circuit A). Thus, Circuit-B can be expected to be more efficient. However in Circuit-A, the switches S_f and S_m form a totem-pole arrangement and commercial MOSFET driver ICs can be used to drive them. The discussions in this chapter specifically focus on Circuit-A variation of the converter, though much of the discussion is valid for Circuit-B as well.

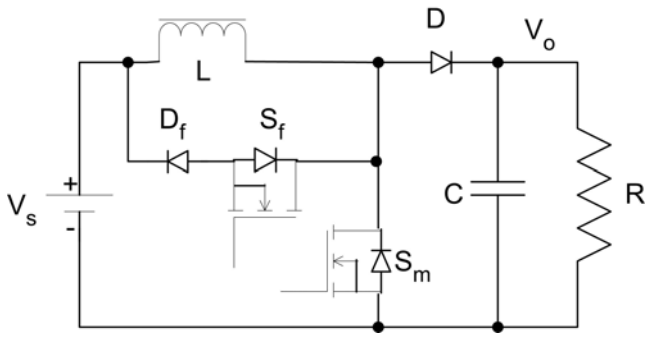


Fig. 5.4. Tri-state boost converter –another alternative (Circuit B)

As mentioned before, the proposed tri-state boost converter shown in Fig. 5.2(b) has three intervals of operation (Fig. 5.5) in cyclic steady-state. They are

1. The '**freewheeling**' interval ($D_f T$): The boost-inductor current is in the freewheeling mode. The switch S_f is ON and S_m is OFF. The diode D is reverse-biased and the capacitor C supplies the load.
2. The '**boost'** interval ($D_b\ T$): Both S_m and S_f are ON and the inductor current builds up. Once again the diode D is reverse-biased and capacitor C takes care of the load.
3. The **'capacitor-charging'** interval ($D_o\ T$): Both S_m and S_f are OFF and the diode D is forward-biased. The inductor current ramps down as the transfer of power to the load side takes place, with the capacitor C being charged.

It may be noted that

$$D_f + D_b + D_o = 1 \tag{5.1}$$

Due to the above constraint (5.1), any two of the three intervals can be controlled independently provided the third interval does not vanish to zero. Thus, unlike in a classical boost converter, the tri-state boost converter allows the boost interval ($D_b\ T$) to be changed at the expense of the freewheeling interval ($D_f\ T$), without having to alter the capacitor-charging interval ($D_o\ T$). This has the capability of avoiding the RHP zero in control transfer function of the tri-state boost converter.

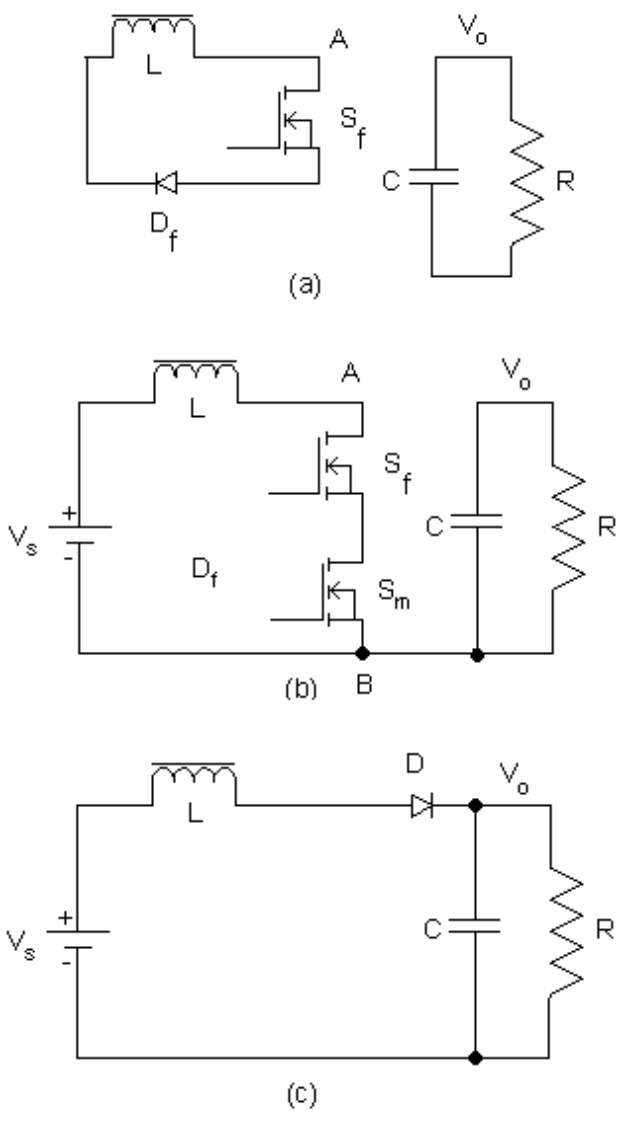


Fig. 5.5. Equivalent circuits under different intervals of operation (a) 'Freewheeling' interval ($D_f T$) (b) 'Boost' interval ($D_b\ T$) (c) Capacitor-charging interval ($D_o\ T$).

The currents and voltages in the switches and diodes can be easily determined from the waveforms shown in Fig. 5.6 for analysis and design purposes. A point to be noted is that during the capacitor-charging interval (D_o T), the MOSFETs, S_m and S_f, are both off. Thus in circuit-A, the drain voltage of S_m is undefined during this interval.

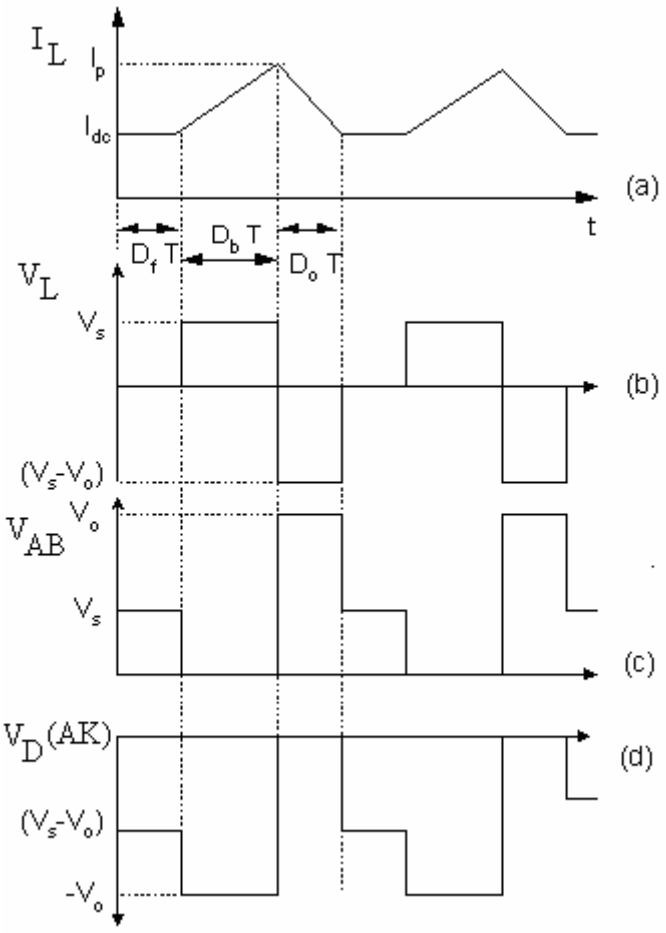


Fig. 5.6. Theoretical steady state waveforms of the tri-state boost converter (a) Boost-inductor current (b) Boost-inductor voltage (c) Voltage across A and B (d) Anode-cathode voltage of Diode D.

Another issue which is of significant importance is the related to the sequence of operation of the intervals. The sequence of the intervals of operation can be different from that in Fig. 5.1 ($D_f \rightarrow D_b \rightarrow D_o$). For example, in Fig. 5.7, the operating sequence is ($D_b \rightarrow D_f \rightarrow D_o$). This latter sequence has the disadvantage of additional losses in

the inductor and in the devices, S_f and D_f, due to higher freewheeling current.

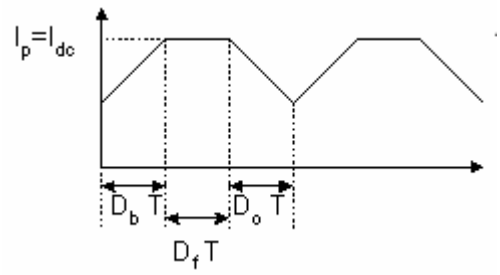


Fig. 5.7. Alternative sequence for converter operation ($D_b \rightarrow D_f \rightarrow D_o$)

5.2.1 DC Analysis

In this sub-section, the dc-analysis of the tri-state boost converter is presented.

A. Boost Voltage Gain

Applying the volt-second balance across the inductor L (Fig. 5.2(b)) and assuming a lossless converter, the dc characteristics of the tri-state boost converter can be shown to be

$$\frac{V_o}{V_s} = \frac{I_s}{I_o} = \frac{(D_b + D_o)}{D_o}, \tag{5.2}$$

where V_o is the dc output voltage, V_s is the dc input voltage, I_o is the dc output current, and I_s is the dc source current. From (5.2), it can be seen that by varying D_b/D_o ratio, the output voltage of the converter can be varied.

B. Inductor Current Ripple (I_{ripple})

The inductor current ripple can be calculated using the following expression.

$$I_{ripple} = \frac{V_s D_b T}{L} \tag{5.3}$$

C. Average Inductor Current (I_L)

Assuming an inductor current sequence of $D_f \rightarrow D_b \rightarrow D_o$ as in Fig. 5.8, the average inductor current is obtained by the following expression.

$$I_L = \frac{V_s D_b T}{2L}(1 - D_f) + I_{dc} \tag{5.4}$$

where, I_{dc} is the free-wheeling current in the inductor.

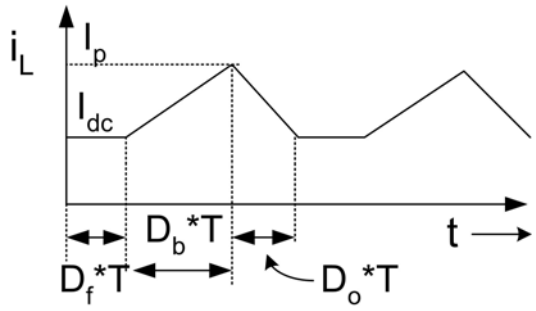


Fig. 5.8. Inductor current waveform with ($D_f \rightarrow D_b \rightarrow D_o$) sequence

D. Peak Inductor Current (I_p)

Assuming an inductor current sequence $D_f \rightarrow D_b \rightarrow D_o$ as in Fig. 5.8, the peak inductor current is obtained by the following expression.

$$I_p = \frac{V_s D_b T}{L} + I_{dc} \tag{5.5}$$

E. Average Input Current

Assuming a lossless transfer of power, the average input current I_s and average output current I_o are related by the following expression.

$$\left(I_{dc} + \frac{V_s D_b T}{2L}\right)(1 - D_f) = I_s = \frac{V_o I_o}{V_s} \tag{5.6}$$

F. Output Voltage Ripple (V_{o_ripple})

With filter capacitor C, cycle time T, and ignoring ESR of the capacitor, the output voltage ripple can be calculated using the following expression.

$$V_{o\_ripple} = \frac{(1 - D_o)TI_o}{C} \tag{5.7}$$

5.2.2 Control Characteristics- A simple 'Constant-D_o' Control Method

The presence of the 'free-wheeling' interval ($D_f T$) introduces one more degree of control-freedom. As a result, there are several ways of controlling the converter. Among them, to start with, a simple control method in which D_b is varied with D_o being fixed is investigated in the rest of this chapter. This simple control method is named 'Constant-D_o' control method.

In the 'constant-D_o' control method, the maximum gain of the converter (V_o/V_s) is reached when $D_b=1-D_o$ (that is $D_f = 0$) and the value of this theoretical maximum gain is $1/D_o$ (see (5.2)). Thus, if a boost gain of 5 is required, the value of D_o should be less than 0.2. Any increase in the energy demand by the load is met by an increase in the boost interval ($D_b T$) and a corresponding decrease in the freewheeling interval ($D_f T$). The instantaneous drop in energy supply to the output side and the resulting output voltage dip experienced in classical boost converter are avoided here as $D_o T$ remains unaffected.

5.2.3 Small-Signal Characteristics

The state equations of the tri-state boost converter during the various intervals are given in (5.8)-(5.10).

$D_f T$ interval:

$$\begin{pmatrix} \frac{di}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ v_o \end{pmatrix} \tag{5.8}$$

$D_b T$ interval:

$$\begin{pmatrix} \frac{di}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ v_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_s \tag{5.9}$$

$D_o T$ interval:

$$\begin{pmatrix} \frac{di}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ v_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_s \tag{5.10}$$

With fixed capacitor-charging time ($D_o T$) and the control input being D_b, using state-space averaging and linearization, the control-to-output (D_b-to-V_o) transfer-function for the tri-state converter can be obtained as

$$\frac{V_o(s)}{D_b(s)} = \frac{V_s}{D_o} \frac{1}{s^2 \frac{LC}{D_o^2} + s\frac{L}{RD_o^2} + 1} \tag{5.11}$$

Detailed derivation of the above expression is given in Appendix A. As expected, (5.11) shows the absence of RHP zero. On the other hand, the control-to-output transfer-function (5.12) [repetition of (2.1)] of the classical boost converter has an RHP zero.

$$\frac{V_o(s)}{D(s)} = \frac{V_s}{(1-D)^2} \frac{\left(1 - s\frac{L}{R(1-D)^2}\right)}{1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}} \tag{5.12}$$

Here D is the duty ratio at the operating point.

For a classical boost converter (5.12), the dc gain and the pole and zero locations vary with operating point due to changes in the duty cycle D. Conversely, in tri-state boost converter (5.11), with the control method fixing D_o, the pole-zero locations are fixed and the dc gain depends only on the input voltage V_s. Thus, the task of designing the controller for the tri-state boost converter under 'constant-D_o' control scheme is further simplified.

Taking the ESR (R_c) of the capacitor also into account, the control-to-output transfer-function of the tri-state boost converter can be shown to be

$$\frac{V_o(s)}{D_b(s)} = G_n \left(\frac{sR_cC+1}{s^2 \dfrac{RLC}{D_o a^2 (R_c + D_o R)} + s \dfrac{L + RR_cD_oC}{aD_o(R_c + D_oR)} + 1} \right), \tag{5.13}$$

where $G_n = \dfrac{V_s R}{a(R_C + RD_o)}$, $a = \dfrac{R}{R + R_c}$.

The left-half plane zero in (5.13) is due to the ESR of the filter capacitor. The input-to-output transfer-function (audio susceptibility) without considering the effect of parasitics is given by the following expression.

$$\frac{V_o(s)}{V_s(s)} = \frac{(D_b + D_o)}{D_o} \frac{1}{S^2 \dfrac{LC}{D_o^2} + S \dfrac{L}{RD_o^2} + 1} \tag{5.14}$$

Under the proposed 'constant- D_o' control scheme, the audio susceptibility depends primarily upon the input voltage.

5.2.4 Simulation and Experimental Verification

A tri-state boost converter and a conventional 'benchmark' boost converter of

same specifications (see Table 5.1) were designed, simulated using MATLAB SIMULINK [63], built, and tested. A comprehensive procedure on the design of these filter components is given in Chapter 7. Details of simulation are given in appendix B. Hardware implementation details are given in appendix C. The output specifications of the converter were 50W/25V and the switching frequency was 50 kHz. This sub-section presents simulation and experimental results, comparison, and discussions.

TABLE 5.1. BOOST CONVERTERS' SPECIFICATIONS

Input voltage	**L**	**C**	**D_o***	**Output voltage**	**R**
10 to 20 V	275 μH	540 μF	0.3	25 V	10 to 100 Ω

* Value needed only for tri-state boost converter

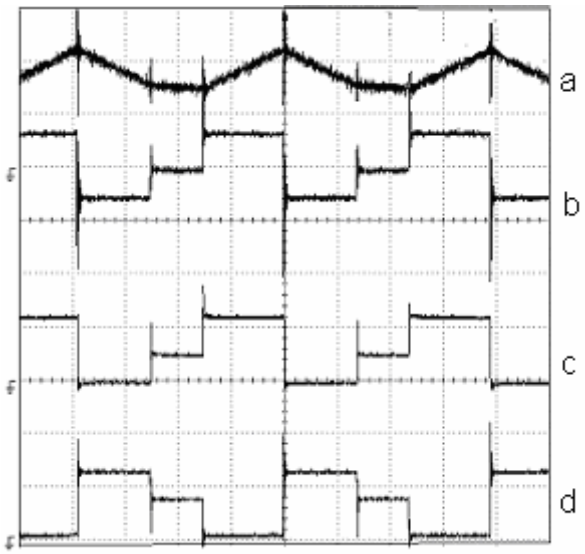


Fig. 5.9. Experimental waveforms of the tri-state boost converter at half load (V_s = 14V and I_o = 1.2 A) (a) inductor current (b) voltage across inductor (c) cathode to anode voltage of diode D (d) voltage across A and B. Scale: current: 0. 5 A/div (ground not shown), voltage: 20 V/div, time: 5μs/div.

Fig. 5.9, a composite plot obtained by combining two different oscilloscope plots, shows the steady-state experimental waveforms of the tri-state boost converter. The experimental waveforms confirm the expected theoretical waveforms of Fig. 5.6.

It is seen that the inductor current shows a small droop during the freewheeling interval primarily because of the conduction losses in the ESR of inductor and in the devices S_f and D_f.

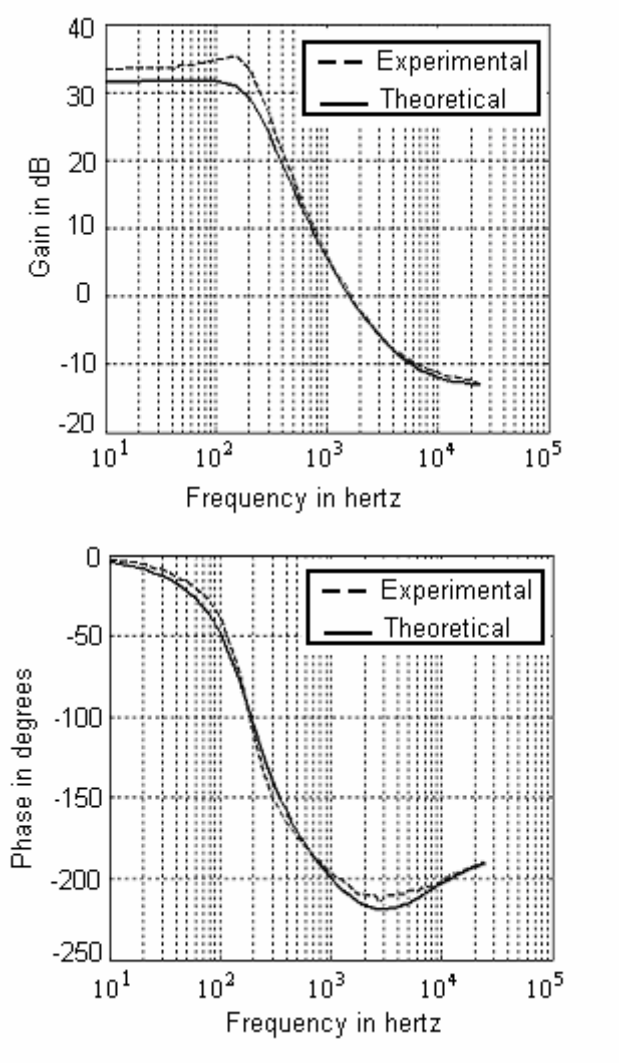


Fig. 5.10. Control-to-output Bode plots under minimum line (10 V) and maximum load (2 A) - Classical boost converter / open-loop operation.

A. Open-Loop Performance

The location of RHP zero of the classical boost converter is closest to the imaginary axis in the complex s-plane under minimum input voltage and maximum load condition. Under this operating condition, the theoretical and experimental

(obtained using HP4194A gain-phase analyzer) Bode plots of the designed classical boost converter are shown in Fig. 5.10. It is seen that due to the presence of complex poles (at a frequency close to 180 Hz) and RHP zero (at a frequency close to 1060 Hz), the phase rolls down towards -270 degrees. However, the ESR of the output-capacitor introduces a zero (at a frequency close to 6000 Hz) which causes the phase to recover to -180 degrees.

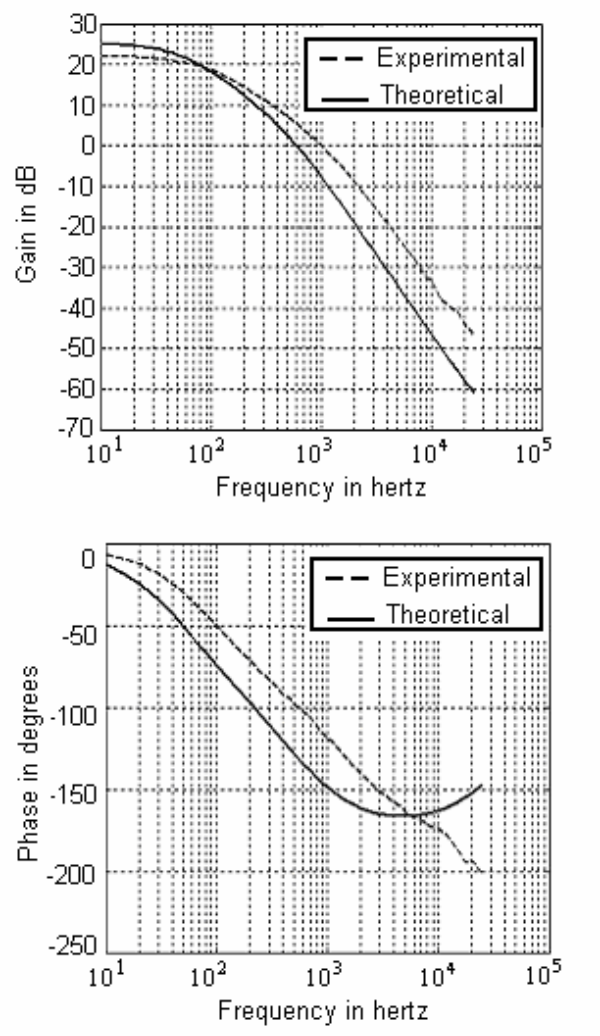


Fig. 5.11. Control-to-output Bode plots under minimum line (10 V) and maximum load (2 A) –Tri-state boost converter / open-loop operation.

Fig. 5.11 shows the corresponding Bode plots of the tri-state converter under the above operating conditions. The experimental Bode plot has a low dc gain, a flatter overall gain curve, and also higher phase compared to the simulated plot which can

perhaps be attributed to the losses in the system. This is because, under low line and high load conditions, the effect of parasitics such as forward voltage drops of diodes and voltage drops in the parasitic resistance of inductor become significant. In the next chapter, a closer match of experimental and theoretical Bode plots taken under conditions of a relatively higher input voltage and lighter (half) load (during which the effect of circuit parasitics is relatively less), will be shown. This will confirm the correctness of the modeling approach. The Bode plots, as theoretically predicted, resemble that of a simple second order system without any RHP zero. At high frequencies, the normal left-half plane zero due to the ESR of the capacitor shows up.

Figs. 5.12 and 5.13 show the simulated variations of inductor current and output voltage for a step change in duty ratio applied to classical and tri-state boost converters respectively. The characteristic initial undershoot seen in the output voltage (Fig. 5.12) of the classical boost converter due to RHP zero is absent in the tri-state converter (Fig. 5.13).

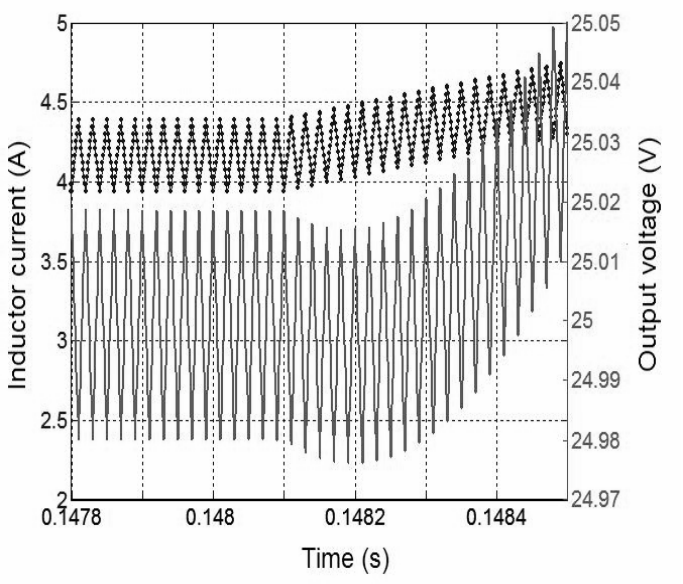


Fig. 5.12. Inductor current (upper) and output voltage (lower) waveforms of classical boost converter for a step increase in duty ratio from D = 0.5 to 0.51 at V_s = 12.5 V, V_o = 25 V, I_o = 2 A

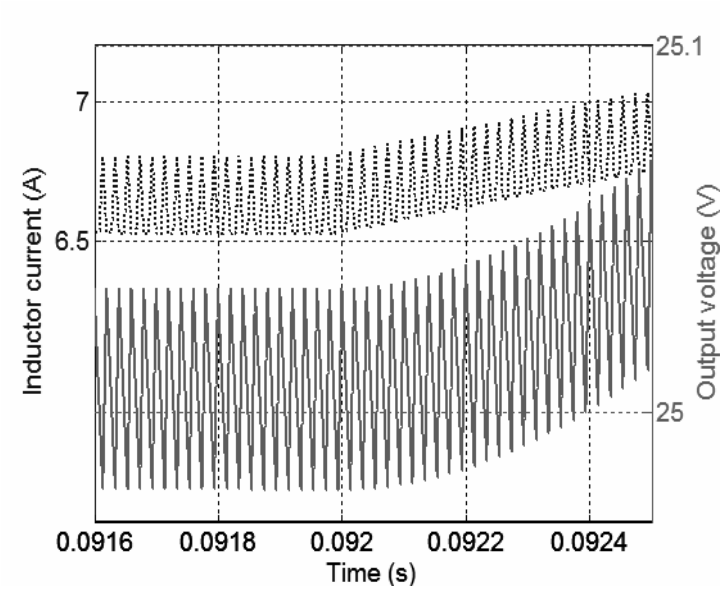


Fig. 5.13. Inductor current (upper) and output voltage (lower) waveforms of tri-state boost converter for a step increase in duty ratio from D = 0.3 to 0.31 at V_s = 12.5 V, V_o = 25 V, I_o = 2 A

B. Closed-Loop Performance

The settling time of the output (to reach and stay within 5% of the steady-state value) for a small step-change in reference voltage and the bandwidth of the loop transfer-function have been used as measures to compare the closed-loop performances of the two converters. The objective of the controller design was to obtain a phase margin of at least 45 degrees and a large bandwidth.

For the classical boost converter, the transfer-function of the controller designed to achieve good performance is given below.

$$T_c(s) = 8.0\frac{\frac{s}{100}+1}{s} \tag{5.15}$$

With the above controller, a cross-over frequency of 270 Hz has been realized. The phase margin achieved is about 48 degrees (Fig. 5.14). Due to the presence of RHP zero, the controller designed can achieve only a low overall bandwidth.

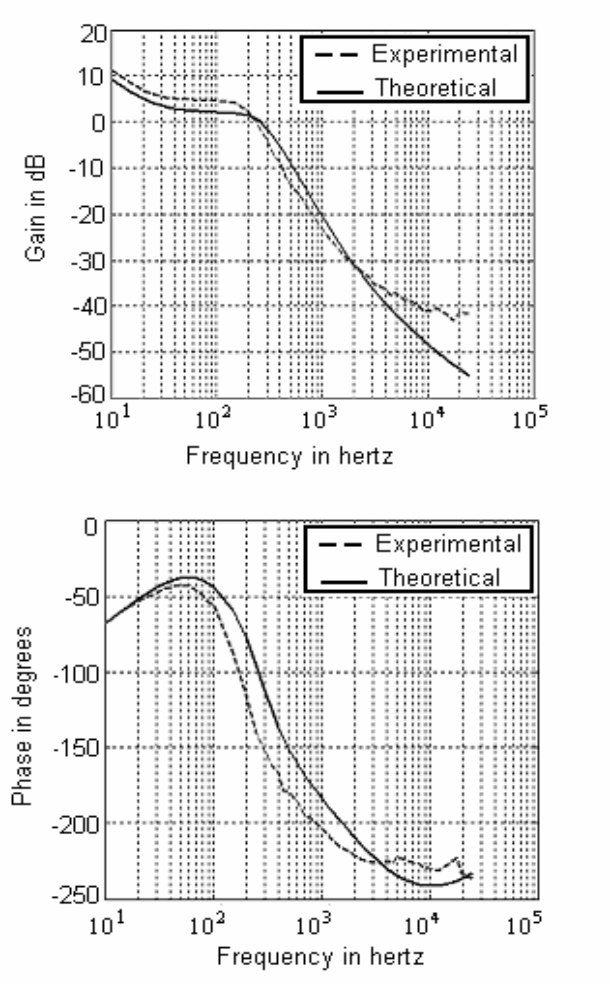


Fig. 5.14. Loop transfer-function Bode plots under minimum line (10 V) and maximum load (2 A)-Classical boost converter

As mentioned earlier, in the case of the tri-state boost converter, the design of controller is simple as the corner frequency of the control transfer function is fixed. This permits obtaining any bandwidth (of course, up to half the switching frequency) with a lead-lag controller having a zero located either at the resonant frequency of the transfer-function or at slightly higher frequencies. A design goal of 5 kHz was set and the transfer-function of the controller designed is given below.

$$T_{ct}(s) = 13.43\frac{\frac{s}{8333}+1}{\frac{s}{31269}+1} \tag{5.16}$$

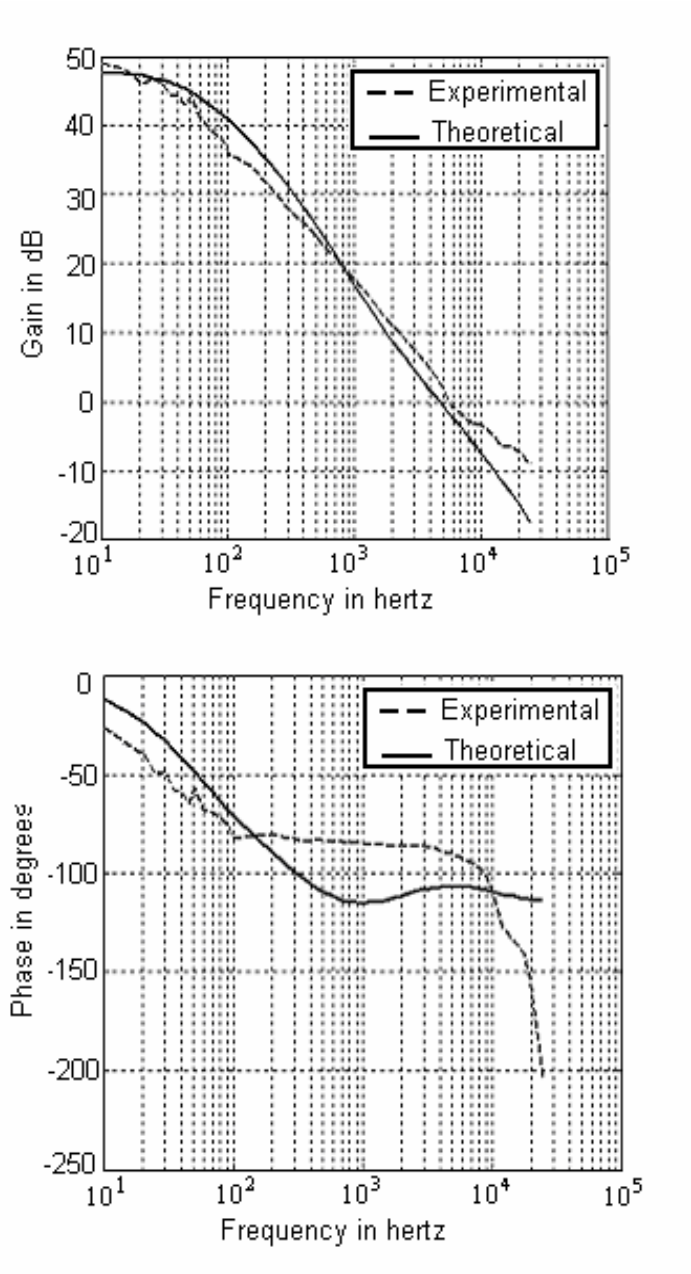


Fig. 5.15. Loop transfer-function Bode plots under minimum line (10 V) and maximum load (2 A)- Tri-state boost converter.

The experimental loop-gain cross-over frequency of the converter is 5.5 kHz and the phase margin is over *90 degrees* (refer Fig. 5.15). It was found that the converter's small-signal response is affected by the losses in the circuit, particularly by the losses in the freewheeling path. It is believed that this accounts for an experimental phase higher than the simulated value (Fig. 5.15). The theoretical gain-

phase curves in Fig. 5.15 have been plotted taking into account several parasitic quantities including the ESR of the capacitor (*0.05 Ω*), the ESR of the filter inductor (*0.15 Ω*), the diode drops and the MOSFET ON-resistance (*0.3 Ω*). In spite of this, there is a mismatch in the Bode plots, particularly in the phase plot. This is perhaps due to the low input voltage (*10 V*) at which these measurements were made.

Figs. 5.16 and 5.17 show the closed-loop response of the two converters for a step change in reference voltage. It is seen that the tri-state converter has a smaller settling time (*700 μs*) as against *40 ms* settling time of the classical boost converter. Table 5.2 summarizes the performance of the two boost converters. As expected, the efficiency of the tri-state boost converter is less than that of the classical boost converter due to the losses in the additional circuit elements. An improvement in efficiency of the tri-state converter by optimizing the inductor current through adjustments in the control input D_o will be presented in the next chapter.

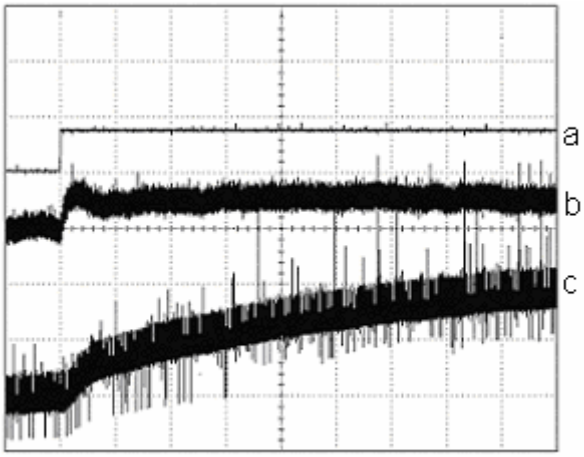


Fig. 5.16. Experimental step response of the classical boost converter for a step change in voltage reference (a) Step reference change (b) Inductor current (from 4.8 A to 5.1 A) (c) Output voltage (from 24.6 V to 25.5 V). Scale: voltage: 0.5 V/div, current: 0.5 A/div, time: 5ms/div

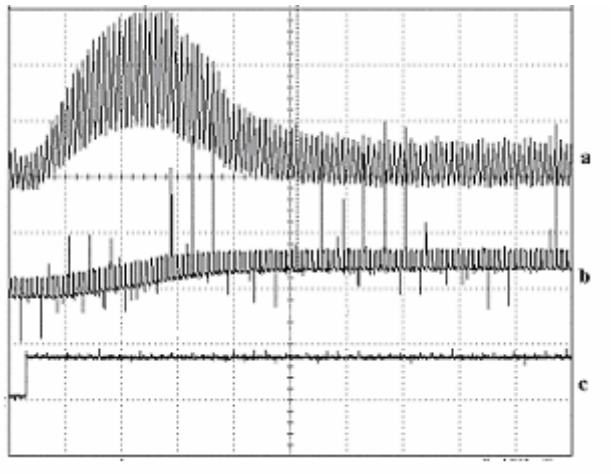


Fig. 5.17. Experimental step response of the Tri-state boost converter for a step change in voltage reference (a) Inductor current (b) Output voltage (from 24.5 V to 25.4 V) (c) Step references change. Scale: voltage: 1 V/div, current: 0.5 A/div, time: 200μs/div

TABLE 5.2. COMPARISON OF EXPERIMENTAL PERFORMANCE OF CONVERTERS

	Crossover frequency	**Phase margin**	**Settling time***	**Full-load efficiency**
Classical boost	270 Hz	48 degrees	>40 ms	84%
Tri-state boost	5500 Hz	>90 deg	0.7 ms	74%

* To reach within 5% of steady-state value

5.3 Tri-State Flyback Converter

Fig. 5.18 shows the tri-state flyback converter. The free-wheeling interval is introduced by the additional switch S_f connected in parallel to the zener diode D_z. The zener diode D_z is used to dissipate the energy trapped in the leakage inductance of the transformer.

In this section, the operation and small-signal model of the tri-state flyback converter is first presented. Following this, simulation and experimental results (under 'constant-D_o' control scheme) demonstrating the dynamic performance improvement are discussed. ***It should be noted that a similar work was reported in [70] in the year 2002 while our work on tri-state family of converters was in progress***. Since similar

results are already published, the tri-state flyback converter is discussed here for the sake of completeness. However, there are differences between the implementation considered here and that discussed in [70]. For example, the inductor current follows a sequence $D_b \rightarrow D_f \rightarrow D_o$ in the implementation reported in [70], whereas it follows $D_b \rightarrow D_o \rightarrow D_f$ here. Besides, in one of the two topologies proposed in [70], the current freewheels through a switch (MOSFET) whose source is connected to the positive rail of the supply. Discussions on the driver IC requirement of this switch are not available.

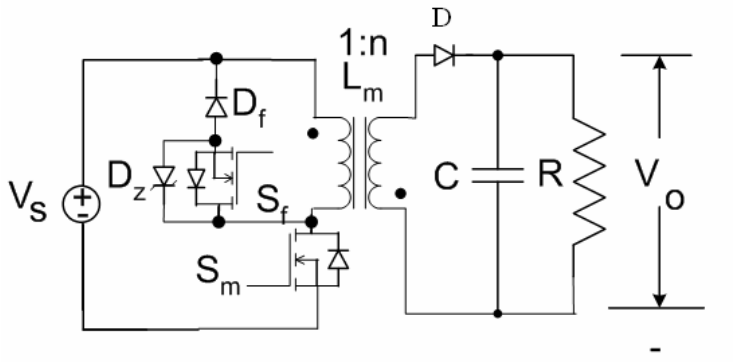


Fig. 5.18. Tri-state flyback converter- circuit diagram.

5.3.1 Tri-State Flyback Converter - Switching Sequence and Theoretical Waveforms

Under cyclic-steady-state tri-state operation, the status of the switches in tri-state flyback converter (Fig. 5.18) is as below.

Boost interval	-	(D_b T) → S_m alone is ON
Capacitor charging interval	-	(D_o T) → D alone is ON
Free-wheeling interval	-	(D_f T) → S_f, D_f - ON

The theoretical waveforms of the various quantities are shown in Fig. 5.19. Here I_m is the equivalent magnetizing current in the coupled inductor. I_{py} is the current in

the primary winding and I_D is the current in the secondary winding.

The steady-state voltage gain of the converter can be obtained by applying volt-second balance across the equivalent inductor. The voltage gain can be verified as

$$\frac{V_o}{V_s} = n\frac{D_b}{D_o} \tag{5.17}$$

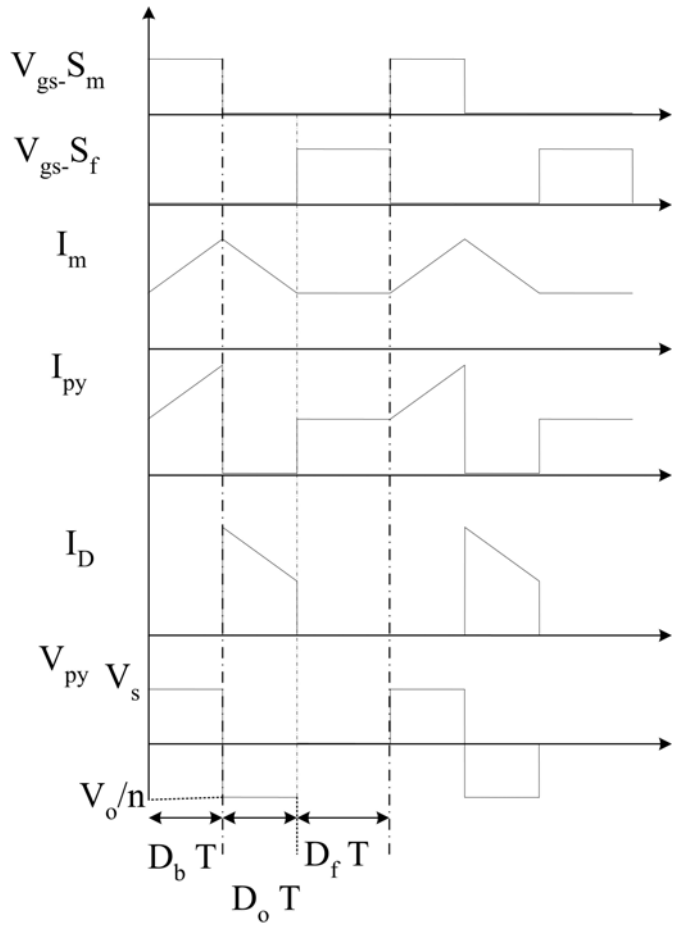


Fig. 5.19. Ideal theoretical steady state waveforms of the tri-state flyback converter (a) Gate-source voltage of switch S_m (b) Gate-source voltage of S_f (c) Magnetizing current in the equivalent inductor (d) Primary winding current (e) Secondary winding current (f) Voltage across the primary winding.

5.3.2 Tri-State Flyback Converter- Small-Signal Characteristics

The state equations of the tri-state flyback converter obtained by neglecting the effect of parasitics, assuming the transformer turns ratio to be unity ($n=1$), and

replacing the coupled inductor by its magnetizing inductance L_m as follows.

$D_f T$ interval:

$$\begin{pmatrix} \frac{di_m}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_m \\ v_o \end{pmatrix} \tag{5.18}$$

$D_b T$ interval:

$$\begin{pmatrix} \frac{di_m}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_m \\ v_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_m} \\ 0 \end{pmatrix} V_s \tag{5.19}$$

$D_o T$ interval:

$$\begin{pmatrix} \frac{di_m}{dt} \\ \frac{dv_o}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L_m} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_m \\ v_o \end{pmatrix} \tag{5.20}$$

With a fixed capacitor-charging time (D_o T) and the control input being D_b, using state-space averaging and linearization, the control-to-output (D_b-to-V_o) transfer-function for the tri-state flyback converter can be obtained as

$$\frac{V_o(s)}{D_b(s)} = \frac{V_s}{D_o} \frac{1}{s^2 \frac{L_m C}{D_o^{\,2}} + s \frac{L_m}{R D_o^{\,2}} + 1} \tag{5.21}$$

The above transfer-function (assuming $n=1$) is exactly same as the one obtained with the tri-state boost converter (5.11) and has the same advantages as those of the tri-state boost converter's control transfer-function discussed in the previous section. The control-to-output transfer-function of the single-switch flyback converter shown in Fig. 5.2(e) (with n=1) has an RHP zero and is given by the following expression.

$$\frac{Vo(s)}{D(s)} = \frac{Vs}{(1-D)^2} \frac{1 - s\frac{DLm}{R(1-D)^2}}{1 + s\frac{Lm}{R(1-D)^2} + s^2 \frac{CLm}{(1-D)^2}} \tag{5.22}$$

In (5.22), D stands for the duty ratio of the switch at the operating point. It may be seen that similar to the case of the classical boost converter, the locations of poles and the RHP zero change dynamically with changes in operating point.

Considering the effect of parasitics namely the diode forward voltage drop V_d, ESR of the capacitor R_c, resistance of the primary winding rp, resistance of the secondary winding rs, and the MOSFET resistance mr, the control-to-output voltage transfer-function of the tri-state flyback converter under 'constant-D_o' control scheme (5.21) gets modified. The modified transfer function can be verified as

$$\frac{V_o(s)}{D_b(s)} = \frac{(V_s + V_d)aD_o}{J} \frac{(1 + R_c Cs)}{s^2 \frac{L_m C}{J} + s\frac{K}{J} + 1} \tag{5.23}$$

where

$$a = \frac{R}{R + R_c};$$

$$\mathrm{J} = \frac{\mathrm{a}}{\mathrm{R}}\left([rp + mr][1 - D_o] + D_o[rs + aR_c]\right) + a^2 D_o{}^2 \tag{5.24}$$

$$K = \frac{L_m a}{R} + C[rp + mr][1 - D_o] + CD_o[rs + aR_c]$$

Once again it may be seen from (5.23) that an LHP zero has been introduced on account of the ESR of the filter capacitor.

5.3.3 Simulation and Experimental Results

A tri-state flyback converter with the specifications given in Table 5.3 has been designed and simulated. A hardware prototype has been built and tested. Simulation models are described in appendix B. Circuit implementation details are given in appendix C. This section presents simulation and experimental results demonstrating the excellent dynamic performance of the converter.

TABLE 5.3. TRI-STATE FLYBACK CONVERTERS' SPECIFICATIONS

Input voltage	L_m	C	D_o *	Output voltage	I_o (rated)	Switching frequency	n	V_z of D_z
20 to 40 V	240 μH	100 μF	0.3	25 V	2 A	100 kHz	1	100V

* Value needed only for tri-state flyback converter

Fig. 5.20, a composite plot obtained by combining two different oscilloscope plots, shows the steady-state experimental waveforms of the tri-state flyback converter under certain load and line conditions. The experimental waveforms confirm the expected theoretical waveforms of Fig. 5.19. The ringing observed in these waveforms is attributed to the leakage inductance of the windings and the parasitic capacitances.

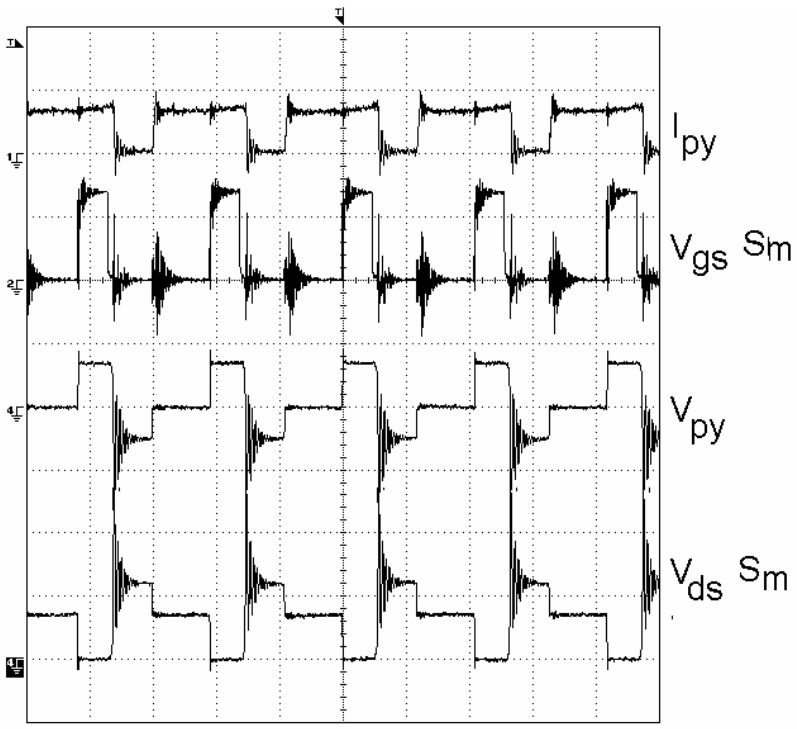


Fig. 5.20. Experimental waveforms of the tri-state flyback converter at half load (V_s = 35V and I_o = 1 A) (I_{py})- Primary current, scale: 5 A/div (V_{gs}-S_m) – Gate-source voltage of S_m, scale: 10 V/div, (V_{py})- Voltage across the primary winding, scale : 50 V/div (V_{ds} S_m)- Drain-source voltage of S_m, scale: 50 V/div, time: 5μs/div.

Fig. 5.21 shows the theoretical (with and without considering the effect of parasitics) and experimental Bode plots (obtained using HP4194A gain-phase

analyzer) of the control-to-output *(Db-to-Vo)* transfer.

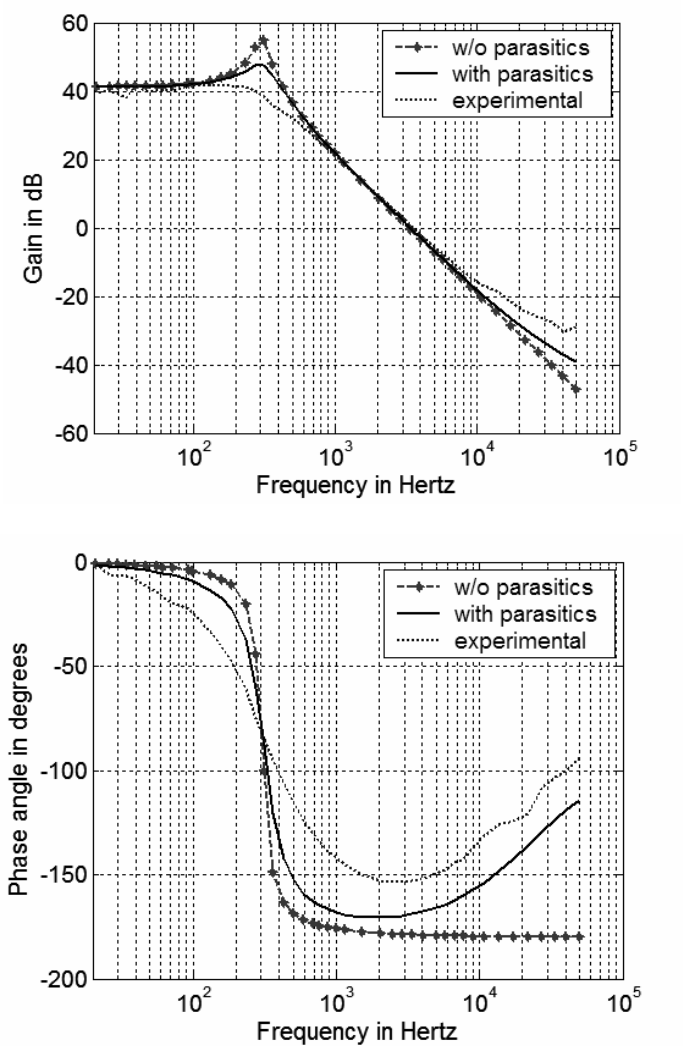


Fig. 5.21. Control-to-output (D_b-*to*-V_o) Bode plots under V_s = 35 V and I_o = 1 A –Tri-state flyback converter.

As the ideal theoretical (without parasitics) and the experimental plots of the converter differ considerably, Bode plots taking into account the converter parasitics have also been plotted. The parasitics of the converter considered are listed below.

ESR of Capacitor *C*	=	0.07 Ω
Diode forward drops V_d	=	0.8 V (approximated)
MOSFET forward resistance *mr*	=	0.075 Ω (from data sheet)
Primary winding resistance *rp*	=	0.059 Ω (measured)

Secondary winding resistance rs = 0.057 Ω (measured)

It may be noticed that with the inclusion of the parasitics, the theoretical predictions are closer to the experimental results (Fig. 5.21). This verifies the correctness of the predicted small-signal model of the converter.

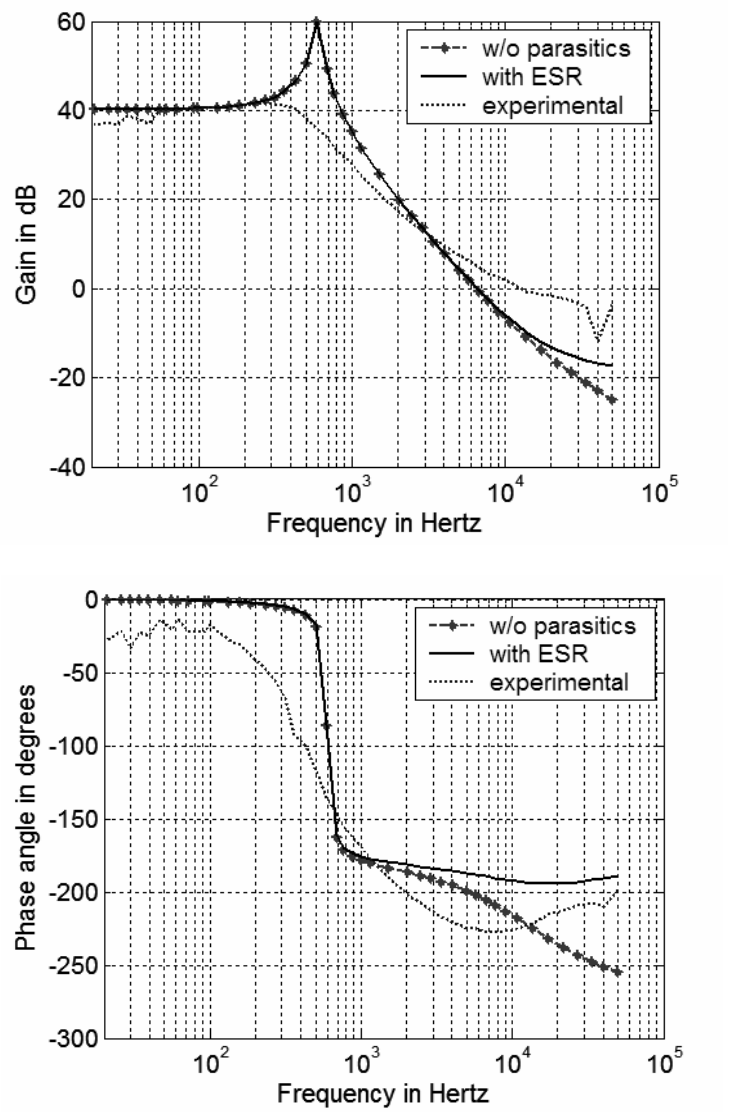


Fig. 5.22. Control-to-output (D-to-V_o) Bode plots under V_s = 35 V and I_o = 1 A –Classical flyback converter.

A classical flyback converter has been realized using the circuit in Fig. 5.18 by simply disabling the gate pulses to S_f. The theoretical (with and without considering ESR of filter capacitor) and experimental (obtained using HP4194A) control-to-

output Bode plots of the classical flyback converter are shown in Fig. 5.22. It may be noticed that due to the presence of RHP zero, the phase plot rolls towards -270 degrees but eventually recovers back indicating the existence of LHP zero due to ESR of the filter capacitor.

5.3.4 Closed-Loop Performance

For closed-loop performance, a design goal of 10 kHz was set for the tri-state flyback converter. A cascaded combination of lead-lag and PI controller (5.16) has been used to achieve the required bandwidth theoretically.

$$T_{ct}(s) = 400\frac{\frac{s}{4900}+1}{\frac{s}{190000}+1}\frac{\frac{s}{600}+1}{s} \tag{5.16}$$

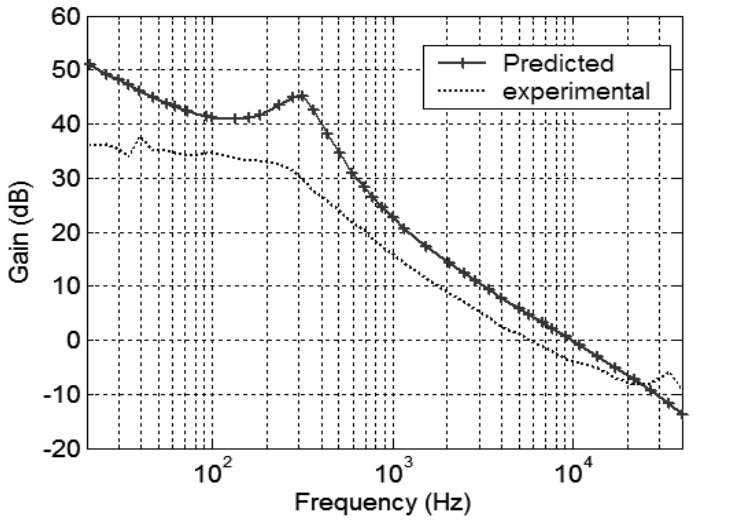


Fig. 5.23. Loop transfer-function Bode plots at V_s = 35 V and I_o = 1 A -Tri-state flyback converter.

Fig. 5.23 shows the experimental and theoretical loop-transfer-functions. While the theoretical bandwidth is 10 kHz, the experimental bandwidth obtained is about 6 kHz. As may be noticed from Fig. 5.23, an increase in the overall gain of the experimental Bode plots will lead to a closer match of experimental and theoretical

Bode plots and also a higher bandwidth close to the design bandwidth of 10 kHz. Perhaps, the non-exact modeling of parasitics in the converter (leakage inductance not considered) and the parasitics of the controller have resulted in a reduction in the experimental bandwidth. Nevertheless, the experimental bandwidth is still better than the bandwidth ($1/30^{th}$ of switching frequency) realized typically with classical flyback converter. A full load efficiency (under minimum line conditions V_s=20V) of 74% has been obtained with the tri-state flyback converter using the 'constant-D_o' control scheme.

5.4 Importance of Tri-state Class of Converters

To establish the importance and need of tri-state class of converters, a literature survey on non-isolated single-stage-single-switch power converters that perform boost action without presenting a RHP zero in the control transfer function has been done. Recently (June 2004), an interesting solution to RHP zero problem has been proposed in [90] for the case of a classical boost converter with an output LC filter. By magnetically coupling the boost inductance and LC filter inductance, RHP zero is eliminated from the control-transfer function. A disadvantage of this scheme is that an additional inductor and capacitor are used which occupy more physical space than a switch and diode that is needed in the case of a tri-state boost converter. Besides, effect of line voltage variations on the frequency response of the converter is not discussed. It is believed that line voltage variations will alter poles of the transfer function significantly and may restrict the closed-loop bandwidth achieved. This is unlike the case of a tri-state boost converter employing 'constant-D_o' control scheme.

A qualitative comparison of tri-state class of converters with popular CUK and SEPIC (Single-ended primary inductance) converters has also been done. One of the

prime advantages of both Cuk and SEPIC converters is that unlike the case of the tri-state converters, both the input and output currents of these converters are smooth resulting in a significant reduction in filter capacitances (both input and output).

On the downside, a major disadvantage of both SEPIC and Cuk converters is that they employ four energy elements and exhibit fourth order response [86]. As a result, the small-signal closed-loop bandwidth realized with these converters is generally much limited. Besides, the control transfer function of the SEPIC converter has an RHP zero at high frequency. However, the small-signal bandwidth is believed to be limited primarily by the fourth order behavior of the converter and not by the RHP zero in this case.

Similar to SEPIC converter, the bandwidth of Cuk converter is also limited by its fourth order behavior. Besides, the control transfer function of the converter has a pair of complex conjugate zeros that shift between right-half and left-half of the complex frequency plane when the load conditions change [87]. This also limits the small-signal bandwidth obtained from the converter.

5.5 Chapter Conclusions

This chapter has proposed tri-state versions of boost and buck-boost-derived converters that avoid the dynamic response problem due to the presence of RHP zero in the control-to-output transfer-function of their corresponding classical versions. The additional degree of control-freedom introduced in the converter in the form of a freewheeling interval has been exploited through a simple 'constant-D_o' control technique to achieve this elimination of RHP zero. Analytical, simulation and experimental results of the tri-state boost and flyback converters have been presented

and compared with those of their classical converter versions. The results clearly demonstrate the superior dynamic performance of the proposed tri-state converters. Similar improvement in dynamic performance is expected in the case of other tri-state converters over their corresponding classical versions. The proposed converters can be used in applications wherever fast-response boost/buck-boost action is needed.

CHAPTER 6

DUAL-MODE CONTROL OF TRI-STATE CONVERTER FOR IMPROVED PERFORMANCE

6.0 Background

Chapter 5 introduced the tri-state class of power converters. A 'constant-D_o' control scheme, in which the 'capacitor-charging' interval of the converter is kept constant was investigated in greater detail. Significant improvement in dynamic performance of the tri-state converter over that offered by its classical counterpart was verified through simulations and experimental results. A key problem with the 'constant-D_o' control scheme is that the resulting inductor current is large especially under high line and load conditions, thereby causing high circuit losses. Improvement in operating efficiency of the converter by optimizing the magnitude of inductor current is the topic of discussion in the present chapter.

To optimize the inductor current and hence to improve the steady-state operating efficiency without much compromise in the dynamic performance, in this chapter two variations of a novel dual-mode control (DMC) scheme, both of which effectively exploit the additional degree of control-freedom offered by the tri-state boost converter are proposed and compared. This proposed DMC schemes aim to meet the multiple objectives of excellent small-signal transient response, large dynamic range of operation, and improved efficiency. Unlike the 'constant-D_o' control scheme, the DMC schemes vary both the 'boost' and the 'capacitor-charging' intervals to achieve the desired transient and steady-state performance objectives.

The chapter presents the complete small-signal transfer function model of the tri-state boost converter. Based on this model, design of controllers for the proposed DMC control methods are carried out using multi-variable control techniques. The superior performance of tri-state boost converter with DMC schemes over the one with 'constant-D_o' scheme and over that of the classical boost converter with PI control is established through simulations and experimental results. The DMC schemes achieve a significant (about 10%) improvement in converter's efficiency for a wide load range over the 'constant-D_o' control scheme. The limitations of the proposed DMC schemes are discussed briefly. A detailed discussion on the limitations of the control scheme and its implications on selecting the power and control components will be discussed in the next chapter.

Although the discussions in this chapter are limited to DMC of tri-state boost converter, it is believed that the proposed control method will also improve the operating performance of the other tri-state converters discussed in Chapter 5.

Section 6.1 describes the limitations of tri-state boost converter employing 'constant-D_o' control scheme. Section 6.2 introduces and describes the DMC scheme. This section also presents the complete small-signal control-to-state transfer function model of the tri-state boost converter. Section 6.3 verifies the small-signal model of the converter experimentally. A comparison of steady-state and dynamic performances offered by classical boost converter and tri-state boost converter under the various control schemes is given. Section 6.4 concludes the chapter.

6.1 Dual-mode control (DMC) scheme- Motivation

In this section, the limitations of tri-state boost converter employing 'constant-D_o' control scheme are discussed. In particular, the upper limit established on the

boost voltage gain and the reason behind the high magnitude of inductor current under high line and load conditions are explained. This brings out the need for the proposed DMC scheme.

6.1.1 'Constant-D_o' Control Scheme- Limit on the Voltage Gain

The tri-state boost converter has one more degree of control-freedom, due to the introduction of the free-wheeling interval. The dc voltage gain of the converter is given by ((5.2) repeated).

$$\frac{V_o}{V_s} = \frac{(D_b + D_o)}{D_o} = \frac{1 - D_f}{D_o}, \tag{6.1}$$

where V_o is the dc output voltage and V_s is the dc source voltage. From (6.1), maximum possible boost-voltage-gain (6.2) is obtained when $D_f = 0$.

$$\left(\frac{V_o}{V_s}\right)_{\max} = \frac{1}{D_o} \tag{6.2}$$

Thus, with D_o held constant in the 'constant-D_o' control scheme, an upper limit is established on the boost voltage gain. A higher boost gain, if needed, can be achieved only by changing D_o.

6.1.2 'Constant-D_o' Control Scheme- Magnitude of Inductor Current

From Table 5.2, it may be noticed that the full load efficiency of tri-state boost converter employing 'constant-D_o' control scheme is about 10% lower than the classical boost converter. This increased power loss may be attributed to the extra circuit elements employed. Another important reason is that the 'constant-D_o' control scheme establishes a large free-wheeling current in the converter that increases the circuit losses significantly. It is this increase in loss due to large free-wheeling current

that is sought to be reduced in the proposed DMC method.

The inductor freewheel current I_{dc} can be shown to be

$$I_{dc} = \frac{I_o}{D_o} - \frac{I_{p-p}}{2} = \frac{I_o}{D_o} - \frac{(V_o - V_s)}{2L} D_o T , \tag{6.3}$$

$$I_{p-p} = I_p - I_{dc} \tag{6.4}$$

where, $I_{p\text{-}p}$ is the peak-to-peak inductor ripple current and I_p is the peak inductor current. Fig. 6.1 shows the variation of free-wheel current with D_o for the tri-state boost converter considered in Chapter 5. When D_o is set at a low value, the free-wheel current is high resulting in increased power loss. Setting a high value of D_o brings down the free-wheeling current and hence the power loss, but reduces the maximum possible boost ratio (6.2). In addition, a high value of D_o also results in a smaller free-wheeling interval ($D_f T$). As the free-wheeling interval acts as an 'energy reservoir,' any reduction in the free-wheeling interval leads to a reduced range of disturbances within which the converter offers fast dynamic response. An in-depth analysis of this aspect will be given in the next chapter, which deals with the design of the converter.

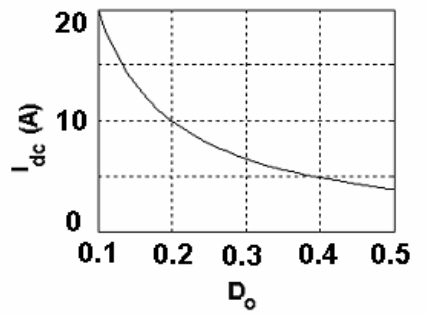


Fig. 6.1. Theoretical variation of free-wheeling current versus D_o at P = 50W, V_s = 15 V, V_o = 25 V, f = 50kHz, and L = 278 μH.

Under near-constant operating line and load conditions, the 'constant D_o' control scheme will be the best choice to attain the multiple-objectives of achieving high efficiency, wide dynamic range of operation, and required boost ratio. However, when

the line and load conditions of the converter vary over a wide-range, the 'capacitor-charging' interval ($D_o\,T$) will also have to be varied in order to achieve the multiple goals desired for the reasons given below.

Let the input voltage of the converter increase under a constant load. Under 'constant-D_o' control scheme, this increases the steady-state inductor current from I_{DC1} to I_{DC2} (refer Fig. 6.2) (as shown by (6.3)). It may be seen that the resulting free-wheeling interval is long indicating large energy storage in the inductor. If, however, interval $D_o\ T$ is increased while still satisfying the boost gain needed (6.1), then the free-wheeling current I_{dc} (6.4) and hence the circuit losses can be brought down as shown in Fig. 6.2. Such a 'dual-mode' control (DMC) scheme having two control inputs namely, D_b and D_o is proposed in this chapter.

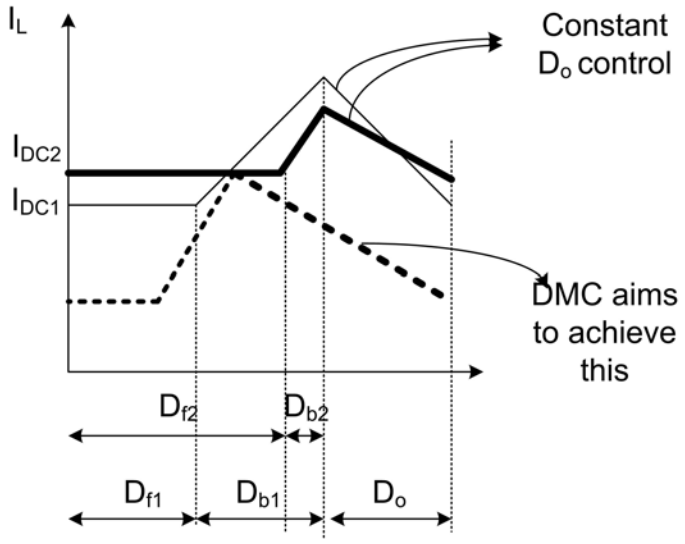


Fig. 6.2. Comparison between inductor currents established by constant-D_o and DMC schemes for an increase in input voltage from $V_o/2$ to ¾ V_o.

6.2 Dual Mode Control (DMC) Approach

In this section, to start with, the tri-state boost converter's small-signal transfer-

function model is presented. A grouping of control-inputs to converter states is then done and on this basis, the DMC scheme is established. Two variations of the DMC scheme are presented and associated controller designs are discussed.

6.2.1 Tri-State Boost Converter- Small-Signal Model

Using state-space averaging and linearization, the control-input-to-converter-state transfer-function matrix *G(s)* of the tri-state boost converter can be obtained as below. Detailed derivations are given in Appendix A.

$$\begin{bmatrix} V_o(s) \\ I_L(s) \end{bmatrix} = G(s) \begin{bmatrix} D_b(s) \\ D_o(s) \end{bmatrix} = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} \begin{bmatrix} D_b(s) \\ D_o(s) \end{bmatrix} \tag{6.5}$$

where I_L is the average inductor current, V_o is the average output voltage, and

$$G(s) = \frac{1}{\left(\frac{LC}{D_o^2}s^2 + \frac{L}{RD_o^2}s + 1\right)} \begin{bmatrix} \frac{V_s}{D_o} & \frac{V_s D_b}{D_o^2}\left(\frac{sL(D_b + D_o)}{RD_b D_o^2} - 1\right) \\ \left(sC + \frac{1}{R}\right)\frac{V_s}{D_o^2} & -\frac{V_s(2D_b + D_o)}{RD_o^3}\left(\frac{sCRD_b}{(2D_b + D_o)} + 1\right) \end{bmatrix} \tag{6.6}$$

From the transfer function matrix (6.6), it can be seen that the D_b-*to*-V_o transfer function ($G_{11}(s)$) does not have an RHP zero. However, the D_o-*to*-V_o ($G_{12}(s)$) transfer function does have an RHP zero that shifts with the converter's operating point. In addition, the D_o-*to*-I_L ($G_{22}(s)$) transfer function has a negative gain that has to be handled appropriately in the control loop.

6.2.2 Grouping of Control Inputs and Converter States

In multi-variable control system involving *N*-inputs and *N*-outputs, there are *N!* ways to form control loops. In such cases, Relative Gain Array (RGA) ([71], [72]) attempts to give the best combination of control inputs and system outputs. The RGA matrix also gives an estimate of the steady-state interaction between the different

loops. Given a transfer function matrix *G(s)*, RGA (*Γ(0)*) is generally obtained from the zero frequency (*s=0*) transfer function gain matrix *G(0)*, given by

$$\Gamma(0) = G(0) \bullet * \left\{ G(0)^{-1} \right\}^{T} \tag{6.7}$$

where operator '●*' represents element-by-element matrix multiplication, superscript *-1* stands for matrix inversion operation and superscript *T* stands for matrix transpose operation. In the RGA, in any i^{th} row

$$\sum_{j=1}^{N} \Gamma_{ij}(0) = 1; \qquad i = 1, 2, 3 \ldots N \tag{6.8}$$

where Γ_{ij} stands for the element in the i^{th} row and j^{th} column and *N* is the row length of the square matrix *Γ(0)*. The element Γ_{ij} represents a measure of the influence of the j^{th} control input on the i^{th} system state. Hence, if in the i^{th} row,

$$\Gamma_{ij}(0) > \Gamma_{ik}(0), \qquad \forall k \neq j \tag{6.9}$$

then the j^{th} control input has a higher influence on the i^{th} system state than the other control inputs. Thus RGA helps us to find the appropriate grouping of the system states and control inputs.

In the tri-state boost converter, from (6.6), the small-signal gains at zero-frequency (*s=0*) are given by

$$G(0) = \frac{V_s}{D_o} \begin{bmatrix} 1 & \dfrac{-D_b}{D_o} \\ \dfrac{1}{RD_o} & \dfrac{-(2D_b + D_o)}{RD_o^2} \end{bmatrix} \tag{6.10}$$

Obtaining the RGA using (6.7) and (6.10),

$$\Gamma(0) = \frac{1}{(D_b + D_o)} \begin{bmatrix} 2D_b + D_o & -D_b \\ -D_b & 2D_b + D_o \end{bmatrix} \tag{6.11}$$

In (6.11), Γ_{11} is always greater than Γ_{12}. This indicates that system state V_o has to be grouped with control input D_b. Similarly, it can be seen that I_L and D_o should be grouped together. In addition, as mentioned before, the D_o-*to*-V_o transfer function has an RHP zero and hence grouping V_o with D_o will complicate the controller design as is the case in a classical single-switch boost converter. Thus, in the DMC scheme, D_b value will be decided by the output voltage error and D_o value by the inductor current error.

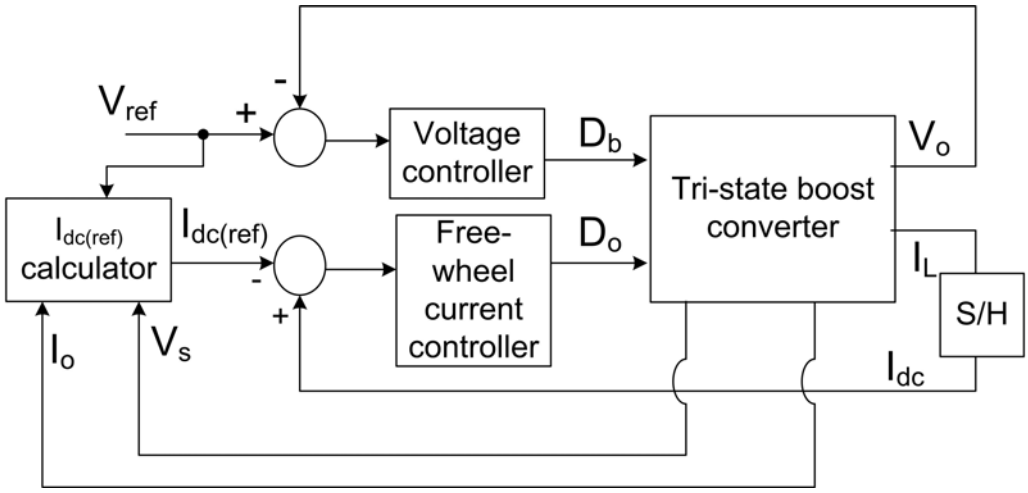


Fig. 6.3. Direct Dual-mode control (DDMC) scheme

6.2.3 Control Method 1- Direct Dual-Mode Control (DDMC)

The first DMC scheme proposed for tri-state boost converter is shown in Fig. 6.3. This scheme, named as 'direct dual-mode control (DDMC) scheme,' employs two controllers, namely a voltage controller that decides D_b from the output voltage error and a free-wheel current controller that decides D_o from the inductor current error. The fast output voltage dynamics of 'constant-D_o' control scheme is preserved by making the rate of change of D_o slower than that of D_b during transients. Hence the output voltage loop is realized as a fast loop whereas the free-wheeling current loop is made relatively slow. Also, when the free-wheeling interval ($D_f T$) vanishes to

zero, D_o will be decided by the inductor current error and D_b will be limited to (1-D_o). If instead, D_o is made dependent on D_b, then the detrimental effect of RHP zero will appear again whenever D_f vanishes as D_o will be forced to change faster with D_b.

The inductor free-wheel current reference signal, $I_{dc(ref)}$ in Fig. 6.3 is set by '$I_{dc(ref)}$ calculator' as follows. Assuming no-loss converter operation, the average input current, I_s can be derived from power equivalence.

$$I_s = \frac{V_{ref} I_o}{V_s} \tag{6.12}$$

For maintaining tri-state operation ($D_f \neq 0$), the average inductor current has to be more than the average input current. The DMC achieves this by fixing the inductor free-wheeling current reference as

$$I_{dc(ref)} = KI_s = K\frac{V_{ref} I_o}{V_s} \tag{6.13}$$

where K is a factor greater than unity. The ***K*-factor** decides the magnitude of the free-wheeling/average inductor current. During start-up, as the output current is zero, the inductor reference current will also be zero as per (6.13). Hence, for proper start-up, a minimum value of D_o (=0.1) overriding the DMC scheme is set.

In general, as the magnitude of inductor current ripple is quite small compared to the free-wheeling current's magnitude over a wide range of operation, either the average inductor current or the free-wheel current in the inductor can be used in the current loop. In the experimental results presented in this chapter, the inductor current has been sampled thus obtaining the free-wheeling current and fed back as I_{dc} (Fig. 6.3). An advantage of the DDMC scheme is that as the currents (inductor current and load current) are sensed directly, current limit protection can be easily implemented.

A. Significance of *K-Factor*

Unlike the case of classical boost converter wherein the selection of power components are generally independent of the parameters of the employed control scheme, in the case of DMC-based scheme, the size and rating of power components are also dependent on the choice of *K-factor*. This can be inferred from (6.13). A low value of *K*-factor results in a small free-wheeling interval and improves the converter's operating efficiency. However, the dynamic operating range of the converter is reduced, due to which the tri-state operation is lost more readily under large-signal dynamic operation. On the other hand, a high value of *K-factor*, although ensuring wider dynamic range of operation, lowers the efficiency. Hence as a compromise, a value of *K-factor* equal to 1.3 has been selected and used to obtain the experimental results that are discussed in the next section. The design aspects of the control scheme including the proper selection of *K*-factor and its implications on the size and rating of the power components will be discussed in the next chapter.

B. Design of Controllers for DDMC

In DMC scheme, the current loop is made one order slower than the voltage loop. Hence the design of output voltage and free-wheel current controllers is done using sequential loop-closing method. The fast voltage loop controller is designed based on $G_{11}(s)$ with the current loop open. For designing the free-wheel current controller, the overall transfer-function between I_L and D_o with the presence of interactions $G_{12}(s)$ and $G_{21}(s)$ and with the voltage loop closed (Fig. 6.4) can be used. This systematic procedure will prevent any instability in the designed loops. Alternatively, the current loop can also be designed based on $G_{22}(s)$ alone neglecting the effect of voltage loop on the current loop as being high speed disturbance

interaction on a slow system. As the current loop is made at least one order slower than the voltage loop, a simple integrator with an integral gain dictated by system stability margins is sufficient for the DDMC scheme.

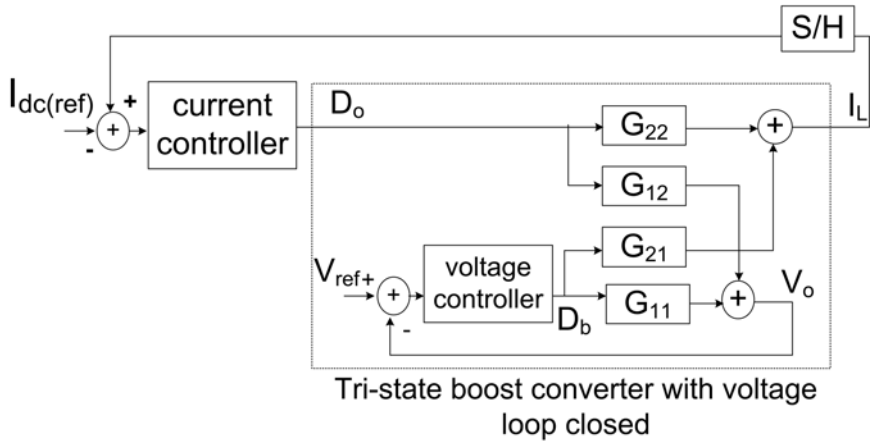


Fig. 6.4. System model with cross-couplings for accurate current controller design (DDMC)

6.2.4 Control Method-II: Indirect Dual-mode Control (IDMC)

Although the DDMC scheme offers excellent transient and steady-state performance as will be demonstrated in section 6.3, it requires sensing of the input voltage and the load current in addition to output voltage and inductor current. The indirect dual-mode control (IDMC) scheme, shown in Fig. 6.5 eliminates most of the sensors of DDMC scheme. Here, the magnitude of the steady-state inductor current is controlled indirectly by fixing the steady-state length of the free-wheeling interval. The motivation for this method comes from the following discussion.

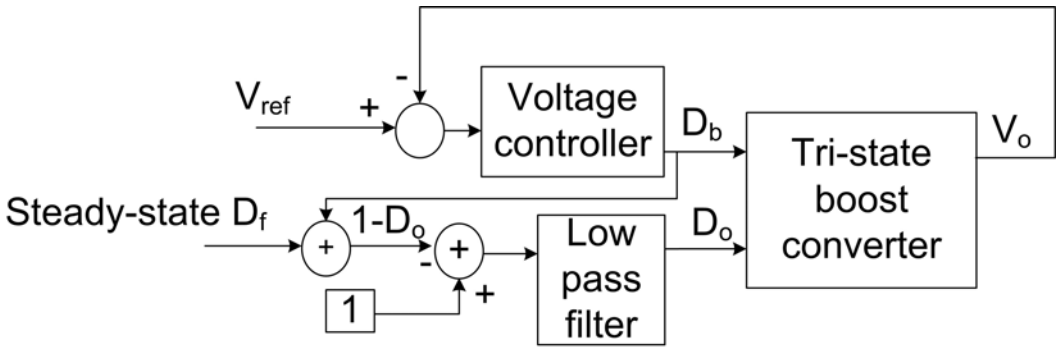


Fig. 6.5. Indirect dual-mode control (IDMC) scheme

Neglecting the ripple current term in (6.3), the inductor free-wheeling current can be written as

$$I_{dc} \approx \frac{I_o}{D_o} \tag{6.14}$$

The reference value of free-wheeling current is given by (6.13). Combining (6.13), (6.14) and (6.3)

$$I_{dc} = K \frac{V_{ref} I_o}{V_s} = \frac{I_o}{D_o} \tag{6.15}$$

$$K = \frac{V_s}{V_{ref} D_o} = \frac{1}{D_b + D_o} = \frac{1}{1 - D_f} \tag{6.16}$$

From (6.16), it can be seen that D_f is constant when *K-factor* is kept constant. The IDMC advantageously uses this relation (6.16) by fixing the steady-state value of D_f and avoids sensing of inductor current, input voltage, and load current. However, unlike DDMC, implementing output current limit protection will require additional current sensor and appropriate circuitry.

The controller design for the IDMC is much simpler than for the DDMC scheme. The voltage controller design is similar to that in the DDMC scheme. The D_o-controller is simply a low pass filter (see Fig. 6.5) with a cut-off frequency (f_c) much lower than the cross-over frequency of the voltage loop. This makes sure that the variations in D_o are much slower than the variations in D_b, thereby preserving the fast dynamic response characteristics of the output voltage (similar to 'constant-D_o' control scheme).

A disadvantage of both DDMC and IDMC schemes is that for large disturbances, the dynamics are slow as they depend on the slow-acting current loops. The fast

dynamic range of the converter is determined by the amount of energy stored in the inductor. A detailed discussion on the range of disturbances within which fast dynamic operation of the converter is preserved will be given in the next chapter.

6.3 Simulation and Experimental Results

A tri-state boost converter and a classical boost converter with the specifications in Table 6.1 (Table 4.1 repeated here) were designed and simulated using MATLAB SIMULINK. The design values of *L* and *C* (described in the next chapter) for both converters were 278μH and 510μF respectively. Hardware prototype models were built and used to verify the theoretical predictions. This section presents certain critical simulation and experimental results. Simulation models are given in appendix B. The hardware circuitry is given in appendix C.

TABLE 6.1. CONVERTERS' SPECIFICATIONS

Input voltage	D_o*	Output voltage	Output power	Switching frequency
10 to 20 V	0.3	25 V	50 W	50 kHz

* Value needed only for tri-state boost converter with constant D_o

6.3.1 Verification of Small-Signal Model

Figs. 6.6 to 6.9 show the theoretical (with and without considering the effect of parasitics) and experimental Bode plots (obtained using HP4194A gain-phase analyzer) of $G_{11}(s)$, $G_{21}(s)$, $G_{12}(s)$, and $G_{22}(s)$ of the $G(s)$ matrix (6.6) under a certain converter operating condition. As the ideal theoretical (without parasitics) and the experimental plots of the tri-state boost converter differ considerably, the transfer function matrix was again derived and plotted taking into account the converter parasitics with ESR of filter capacitor = 0.115 Ω (measured), ESR of boost inductor = 0.4 Ω (measured), MOSFET ON-resistance = 0.27 Ω (from data sheet) and diode

forward voltage drop = 1 V (approximated). The transfer function matrix *G'(s)* with parasitics can be verified as given below (refer Appendix A for detailed derivation).

$$G'(s)=\frac{1}{J*LC*d(s)}\begin{bmatrix}G'_{11} & G'_{12}\\ G'_{21} & G'_{22}\end{bmatrix} \tag{6.17}$$

where

$$G'_{11}=D_o a\left(V_s+V_D-R_M I_L\right)\left(1+sR_cC\right) \tag{6.18}$$

$$G'_{12}=a\left(sI_L L+R_L I_L+R_M I_L\left(1+D_b\right)+V_s D_o-aRD_o^2 I_L\right)\left(1+sR_cC\right) \tag{6.19}$$

$$G'_{21}=\frac{1}{R}\left(V_s+V_D-R_M I_L\right)\left(a+sR_cC\right) \tag{6.20}$$

$$G'_{22}=\frac{1}{R}\{sRC\left(V_s+I_L\left[R_M-a(R_c+RD_o)\right]\right)+aV_s+aI_L\left[R_M-a(R_c+2RD_o)\right]\} \tag{6.21}$$

$$d(s)=\frac{1}{J}s^2+\frac{P}{J}s+1 \tag{6.22}$$

$$J=\frac{1}{RLC}\left(aR_L+aR_M\left[1-D_o+D_b\right]+a^2R_cD_o+a^2D_o^2R\right) \tag{6.23}$$

$$P=\frac{1}{RLC}\left(aL+R_LRC+RCR_M\left[1-D_o+D_b\right]+aR_cD_oRC\right) \tag{6.24}$$

$$I_L=\frac{V_s\left(D_b+D_o\right)-V_D\left(D_f+D_o\right)}{R_L+2D_bR_M+R_MD_f+aR_cD_o+aRD_o^2} \tag{6.25}$$

$$a=\frac{R}{R+R_c} \tag{6.26}$$

where, R_M= MOSFET ON-Resistance, R_L= Inductor ESR, R_c= Capacitor ESR, V_D= Diode Forward voltage drop, I_L= Average inductor current, R = Load resistance. It may be noticed that with the inclusion of the parasitics, the theoretical predictions are closer to the experimental results.

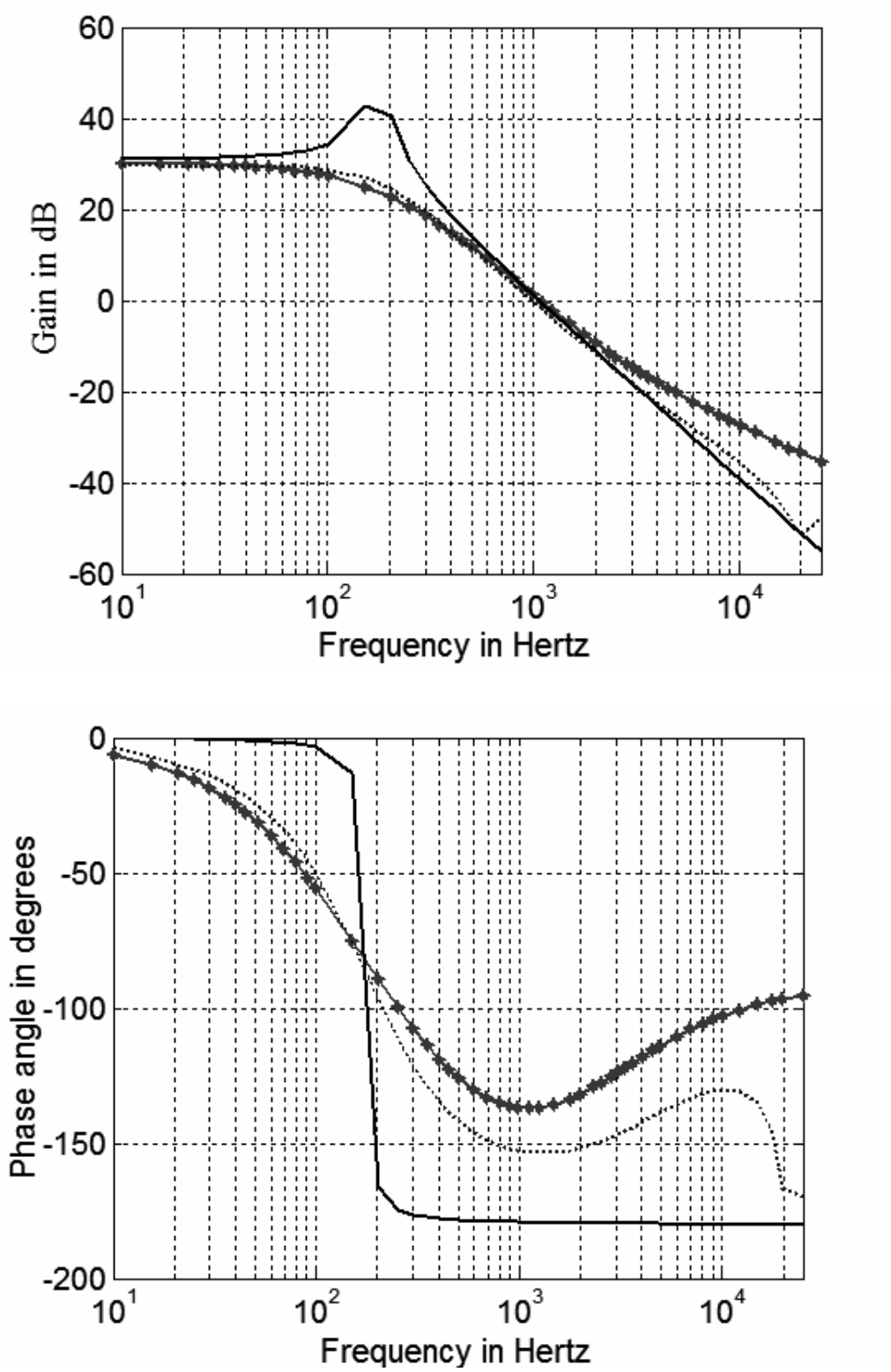


Fig. 6.6. D_b-*to*-V_o Bode plots- Tri-state boost converter/ open-loop operation at V_s = 15V, V_o = 25V, I_o=1A, D_b= 0.3586 and D_o=0.4188; legends: **-theoretical (with parasitics), ..-experimental, _-theoretical (without parasitics).

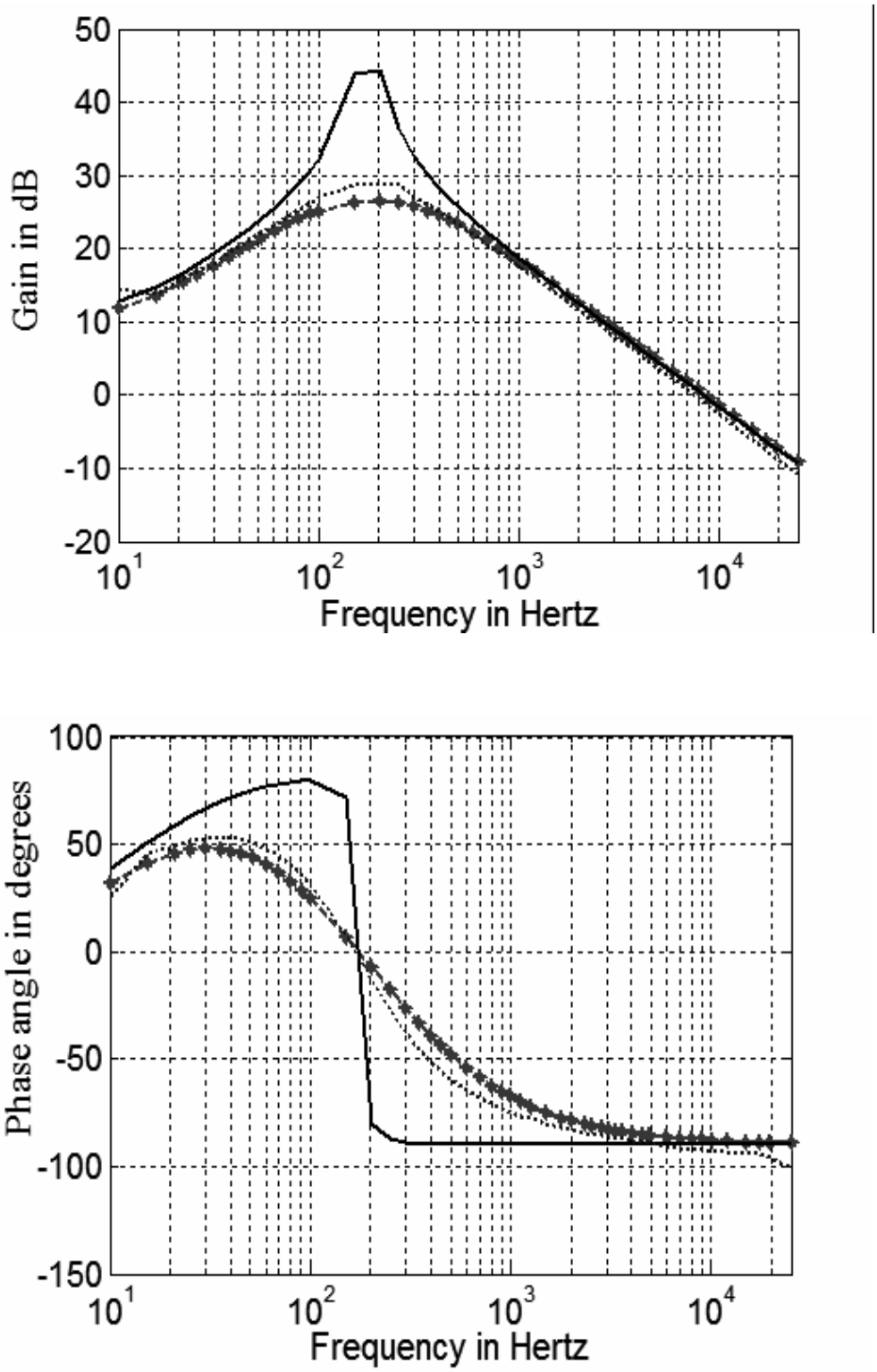


Fig. 6.7. D_b-*to*-I_L Bode plots- Tri-state boost converter/ open-loop operation at V_s = 15V, V_o = 25V, I_o=1A, D_b= 0.3586 and D_o=0.4188; legends: **-theoretical (with parasitics), ..-experimental, _-theoretical (without parasitics).

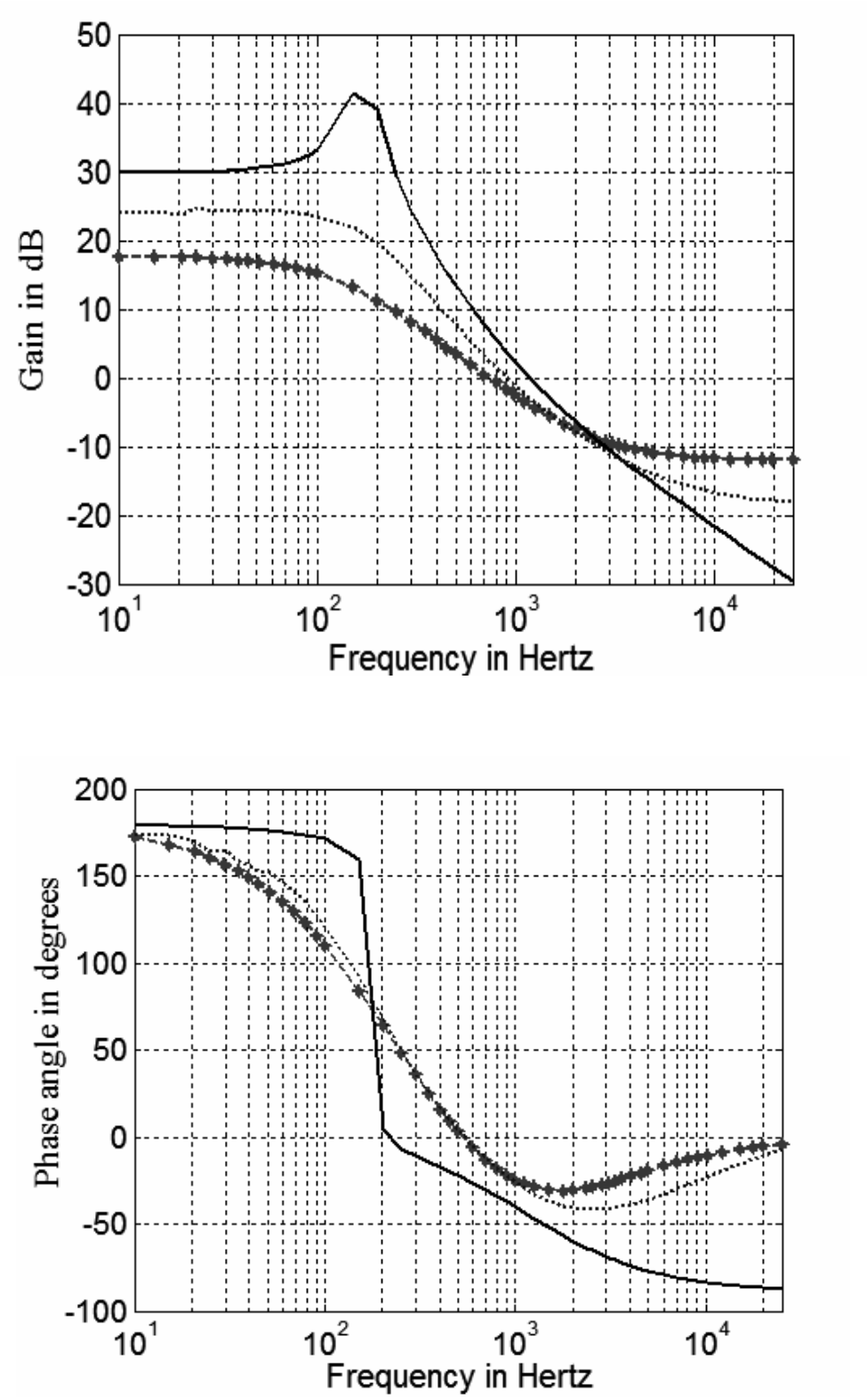


Fig. 6.8. D_o-*to*-V_o Bode plots- Tri-state boost converter/ open-loop operation at V_s = 15V, V_o = 25V, I_o=1A, D_b= 0.3586 and D_o=0.4188; legends: **-theoretical (with parasitics), ..-experimental, _-theoretical (without parasitics).

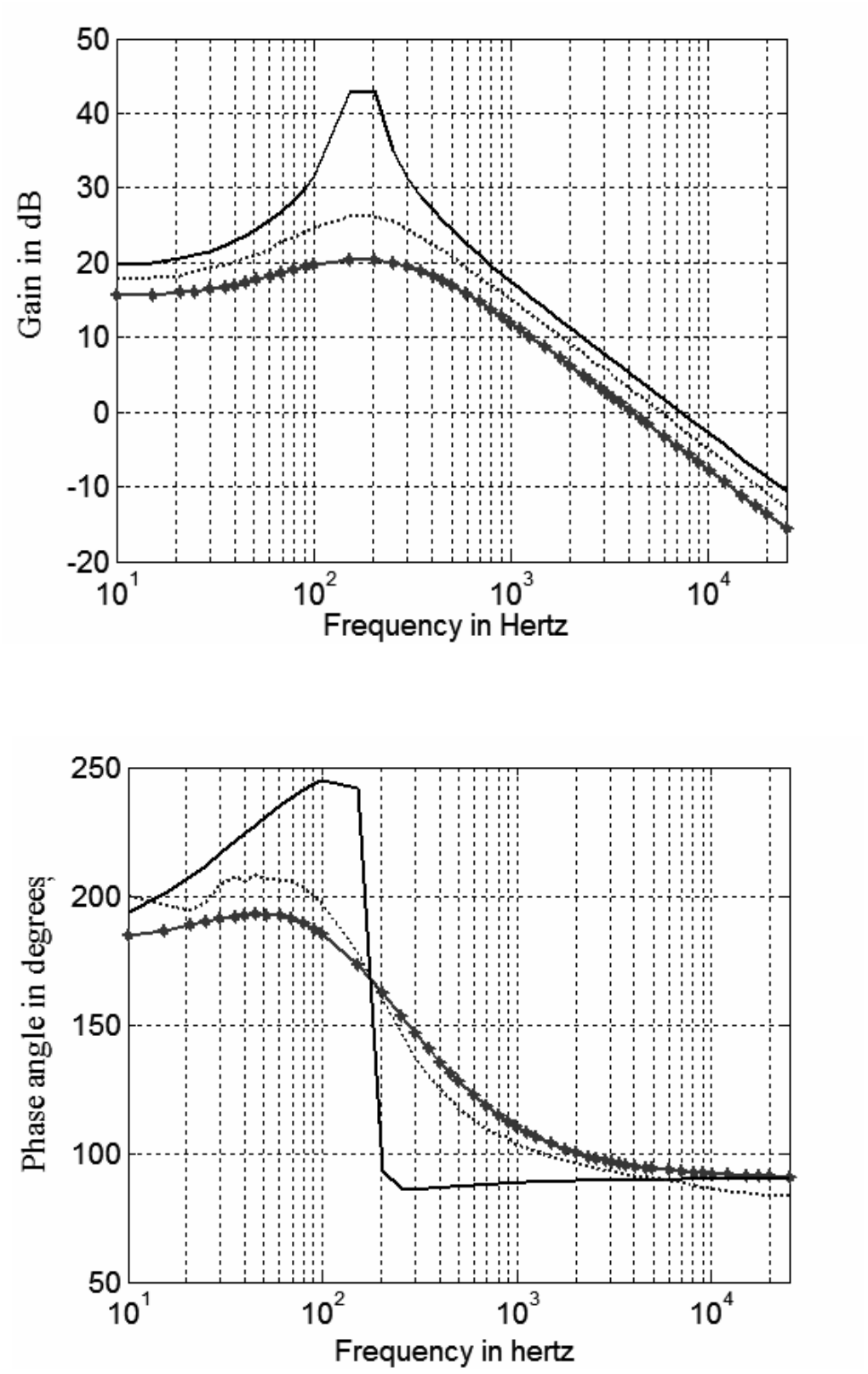


Fig. 6.9. D_o-*to*-I_L Bode plots- Tri-state boost converter/ open-loop operation at V_s = 15V, V_o = 25V, I_o=1A, D_b= 0.3586 and D_o=0.4188; legends: **-theoretical (with parasitics), ..-experimental, _-theoretical (without parasitics).

It may be noticed from Fig. 6.8 the D_o-*to*-V_o transfer function ($G_{12}(s)$) has an RHP zero. The presence of RHP zero results in the phase plot rolling towards -90 degrees before recovering back to 0 degree on account of the presence of LHP zero introduced by the ESR of output capacitor. Besides, it is also seen that the magnitude of $G_{12}(s)$ is more sensitive to system parasitics than those of the other transfer functions. This, once again, suggests that D_o should not be grouped with V_o.

6.3.2 Closed-Loop Performance- Controller Design

The design of controllers for DDMC and IDMC schemes was based on the discussions in section 6.2. The voltage-loop controller designed for both DDMC and IDMC schemes is a cascaded combination of a PI and a lead-lag controller (6.27) that ensures zero steady-state error and a small-signal voltage-loop ($G_{11}(s)*V\_cont(s)$) bandwidth of about *5 kHz* at the designed operating point.

$$V\_cont(s) = 148.8 \cdot \frac{\frac{s}{177}+1}{s} \cdot \frac{\frac{s}{1912}+1}{\frac{s}{36954}+1} \tag{6.27}$$

The above controller was also used in the 'constant-D_o' control scheme. For the DDMC scheme, a small-signal current-loop ($G_{22}(s)*I\_cont(s)$) bandwidth of *500 Hz* was achieved using a simple integrator given by

$$I\_cont(s) = \frac{96.7}{s} \tag{6.28}$$

For the IDMC scheme, the D_o-controller (filter) has a cut-off frequency (f_c) of about *160 Hz* and is given by

$$I\_filter(s) = \frac{1}{\frac{s}{1000}+1} \tag{6.29}$$

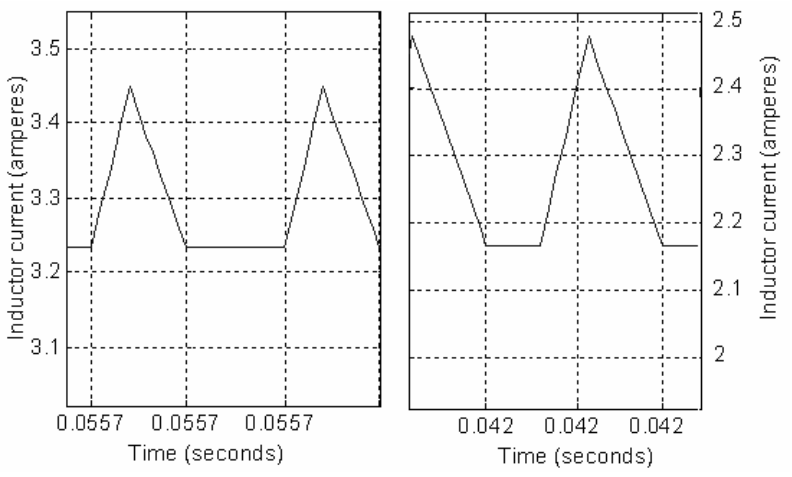
For the classical boost converter, the PI controller designed is based on the discussions in [22] (Table 3.5) and is given by

$$Vboost\_cont(s) = 16.5 \cdot \frac{\frac{s}{1517} + 1}{s} \tag{6.30}$$

6.3.3 Closed-Loop Performance- Simulation and Experimental Results

The closed-loop performances of the various converters/control schemes have been tested through simulations and experiments, under the operating conditions of V_s = 15 V, V_o = 25 V, and I_o = 1 A (R=25 Ω).

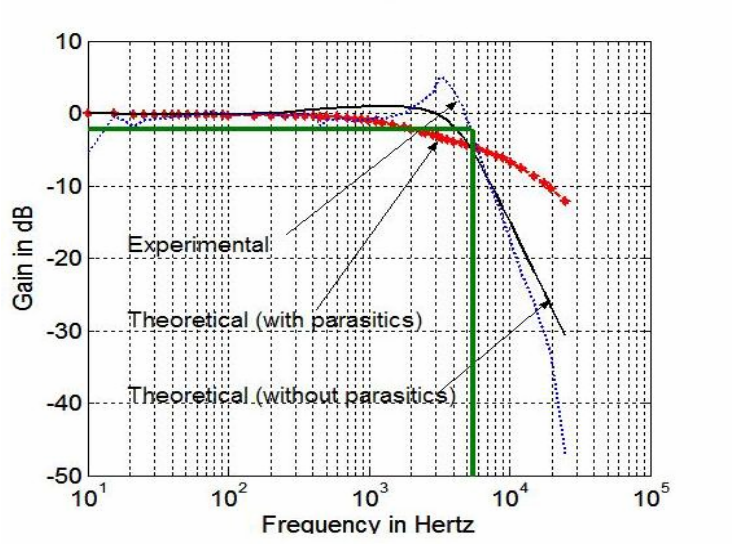
Fig. 6.10 shows a simulated comparison of steady-state inductor currents of the tri-state boost converter under 'constant-D_o' (D_o=0.3) and DDMC schemes (K=1.3). The inductor free-wheel current under the DDMC scheme is about 1.1 amperes less than that under the 'constant-D_o' control scheme. This has the potential to achieve a significant improvement in the converter's operating efficiency under DMC scheme.



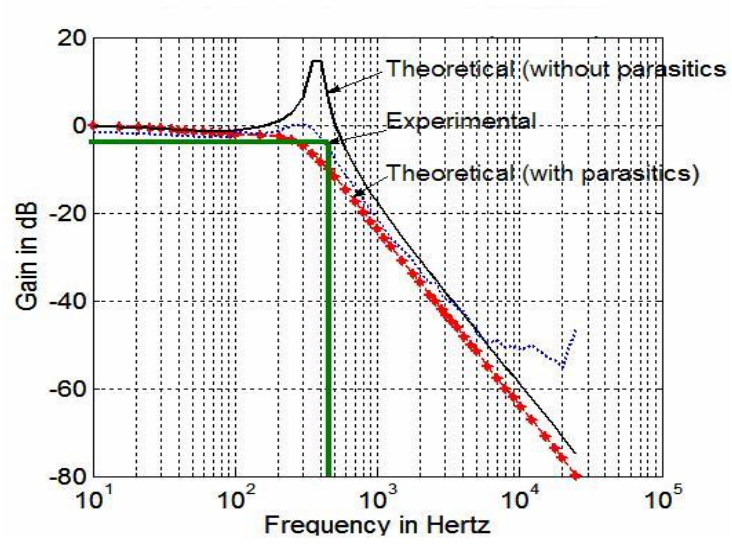
(a) (b)

Fig. 6.10. Simulated steady-state inductor current waveforms of tri-state boost converter (V_s=15 V, V_o= 25 V I_o= 1 A) (a) 'constant-D_o' control scheme (b) DDMC scheme (K=1.3).

Figs. 6.11(a) and 6.11(b) show the theoretical (with and without considering the effect of parasitics) and experimental Bode magnitude plots (obtained using HP4194A gain-phase analyzer) of V_{ref}-*to*-V_o (closed voltage-loop $G_{11}(s)$*$V\_cont(s)$ with D_o held constant) and I_{ref}-*to*-I_L (closed current-loop $G_{22}(s)$*$I\_cont(s)$ with D_b held constant) in DDMC scheme. As per the design, the experimental voltage loop has a closed-loop bandwidth of about 5 kHz. The current-loop bandwidth is nearly 500 Hz. Fig. 6.12 shows that the classical boost converter has an experimental bandwidth of 270 Hz.



(a)



(b)

Fig. 6.11. Closed-loop Bode magnitude plot at V_s = *15V,* V_o = *25V,* I_o=*1A,* D_b= *0.3586* and D_o=*0.4188*; (a) closed voltage loop (b) closed *c*urrent loop.

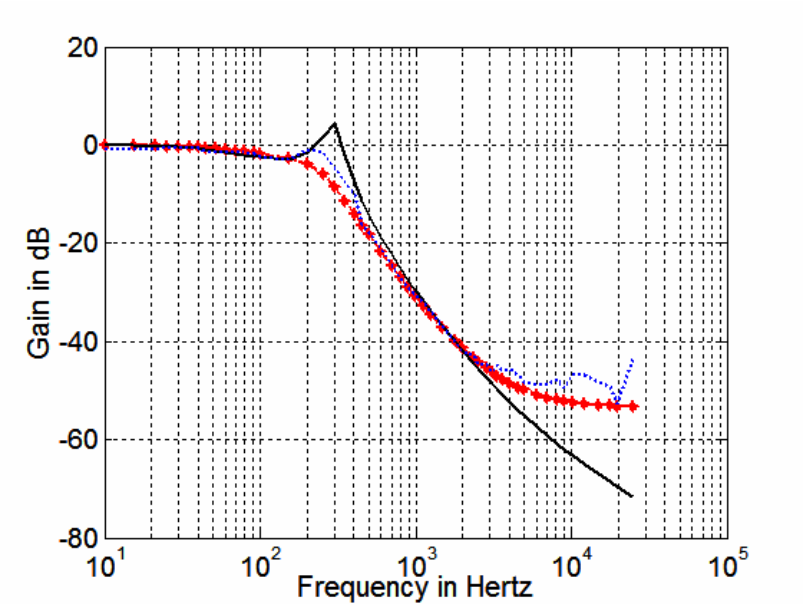


Fig. 6.12. Classical boost converter- closed-loop Bode magnitude plot at V_s = 15V, V_o = 25V, I_o=1A, legends: **-theoretical (with parasitics), ..- experimental, _-theoretical (without parasitics).

Figs. 6.13, 6.14, 6.16, and 6.18 show the experimental reference-voltage step responses of the various converters/control schemes. The excellent dynamic performance of the DMC schemes over the classical boost converter is clearly demonstrated. Moreover, in agreement with the simulation results, the steady-state inductor current (before step transient) under the 'constant-D_o' control scheme is about one ampere more than that under the DMC schemes. Fig. 6.17 shows the slow current loop response (inductor current optimization) under the DDMC and IDMC control schemes. Table 6.2 summarizes the closed–loop bandwidths and settling time of the various converters/control schemes for a reference voltage step-change.

TABLE 6.2. COMPARISON OF EXPERIMENTAL PERFORMANCE OF CONVERTERS

		Bandwidth		settling time	Full load efficiency
		Voltage loop	Current loop		
Classical Boost		270 Hz	--	5.5 ms	86%
Tri-state boost	**Constant D_o**	5 kHz	---	0.7 ms	68%
	DDMC	5 kHz	500 Hz	0.6 ms	79%
	IDMC	5 kHz	f_c=160 Hz	0.6 ms	82%

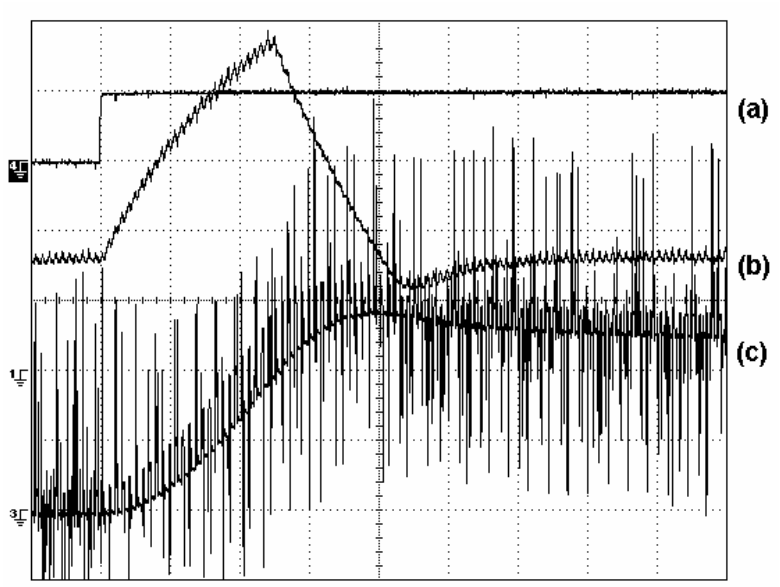


Fig. 6.13. Experimental reference voltage step response of a tri-state boost converter with 'constant-D_o' control scheme (a) step reference change (b) inductor current (ground at -1 div) (c) output voltage from 23.8 V to 25.1 V (oscilloscope in ac mode with ground at -3 div); Scale: voltage: 0.5 V/div, current: 2A/div, time: 200μs/div.

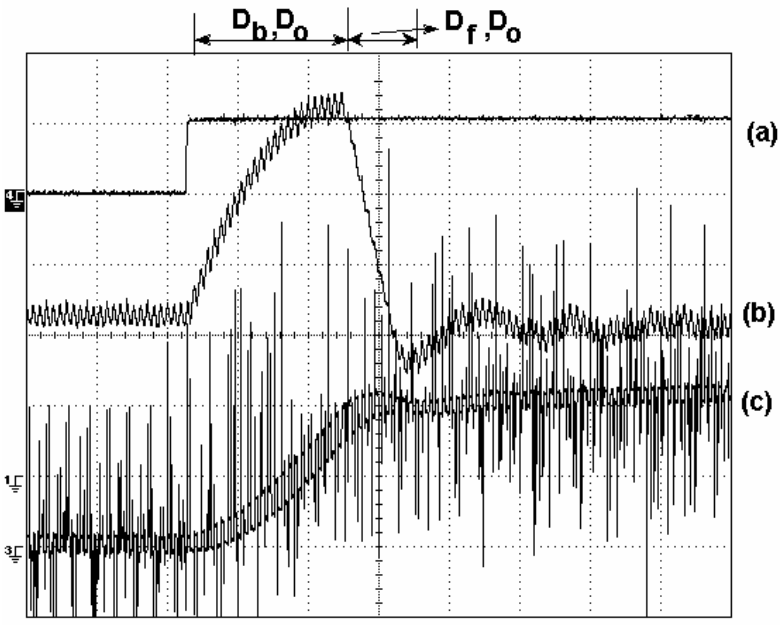


Fig. 6.14. Experimental reference voltage step response of a tri-state boost converter under DDMC scheme; (a) step reference change (b) inductor current (ground at -2 div) (c) output voltage from 24.1 V to 25.1 V ; Scale: voltage: 0.5 V/div, current: 1A/div, time: 200μs/div.

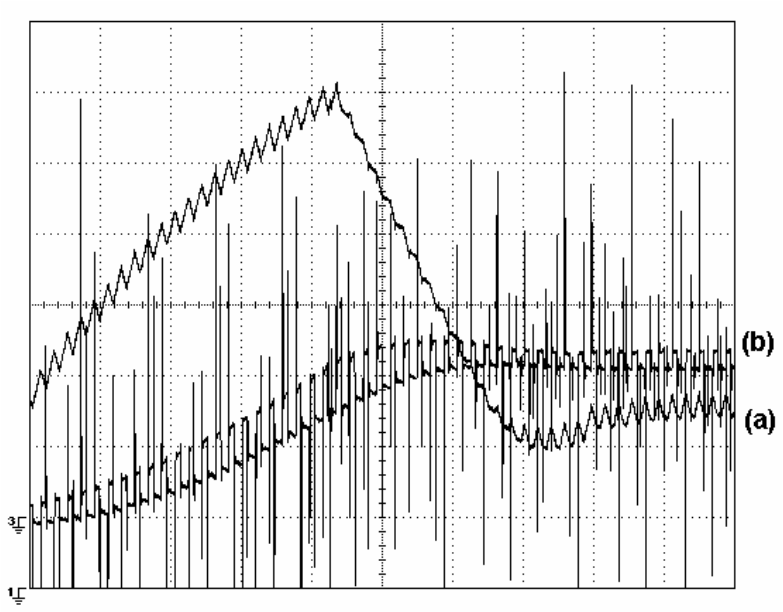


Fig. 6.15. DMC scheme- demonstration of vanishing free-wheeling interval for a step change in reference voltage from 24.1 V to 25.1 V. (a) inductor current (b) output voltage; scale: current: 1A/div, voltage: 0.5 V/div, time: 100μs/div.

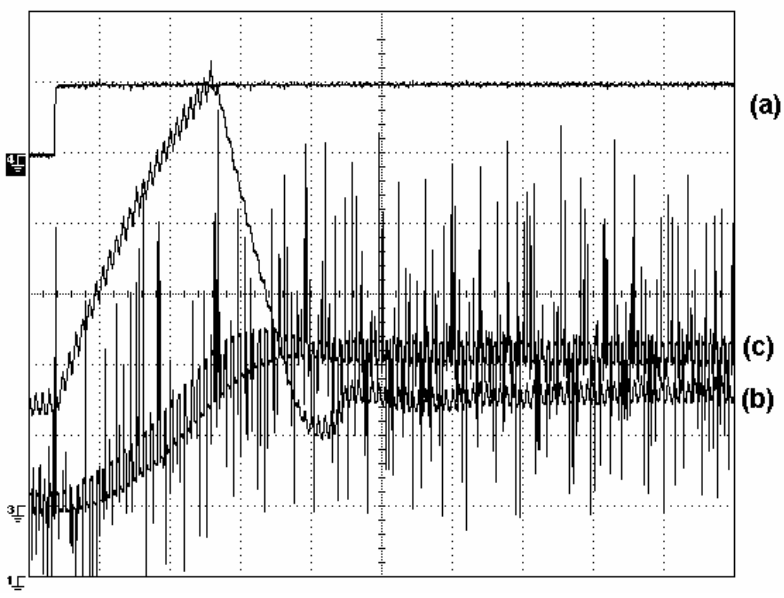
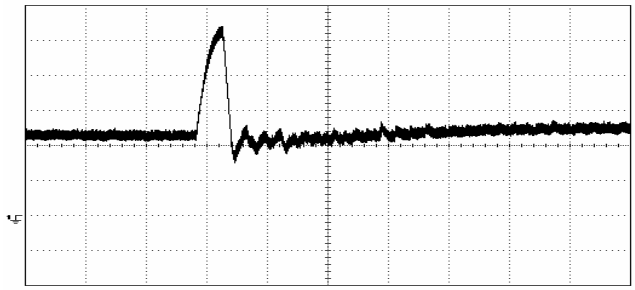
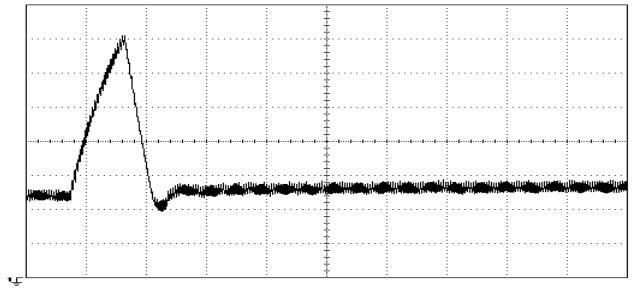


Fig. 6.16. Experimental reference voltage step response of a tri-state boost converter with IDMC scheme; (a) step reference change (b) inductor current (ground at -4 div) (c) output voltage from 24.1 V to 25.1 V (oscilloscope in ac mode with ground at -3 div); Scale: voltage: 0.5 V/div, current: 1A/div, time: 200μs/div.



(a)



(b)

Fig. 6.17. Slow current loop operation for a step change in reference voltage from 24.1 V to 25.1 V (a) DDMC scheme; scale: current: 1A/div, time: 1 ms/div (b) IDMC scheme; scale: current: 1A/div, time: 500 μs/div.

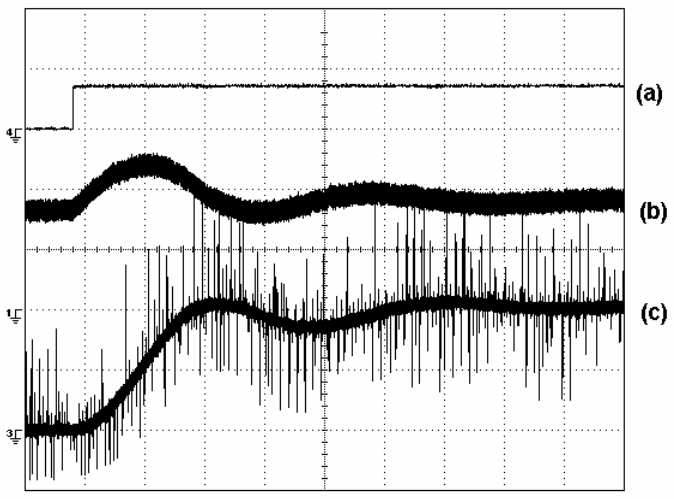


Fig. 6.18. Experimental step response of the classical boost converter for a step change in voltage reference (a) step reference change (b) inductor current (ground at -1 div) (c) output voltage from 24.1 V to 25.1 V (oscilloscope in ac mode with ground at -3 div); Scale: voltage: 0.5V/div, current: 1A/div, time: 1ms/div.

Fig. 6.15 (obtained upon zooming of Fig. 6.14) shows that the free-wheeling interval under DMC (both schemes) vanishes in the first cycle itself after the disturbance thereby boosting up the inductor current. Although the converter shifts to a two-state operation involving D_b and D_o similar to a classical boost converter, it exhibits faster dynamics than the classical boost converter. This is due to the fact that once the converter voltage has reached the reference value, the free-wheeling interval once again appears and the inductor acts as an 'energy reservoir' for the excess energy. Due to lack of such an 'excess energy reservoir' in a classical boost converter, energy oscillations occurring between the boost inductor and output capacitor result in slow dynamics. Fig. 6.15 shows that once the output voltage surpasses the reference voltage, the converter shifts to another two state operation involving D_f and D_o in order to keep the output voltage equal to the reference value.

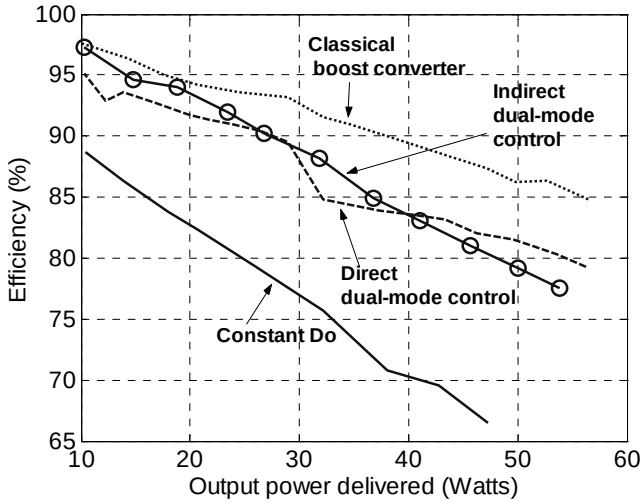


Fig. 6.19. Efficiency versus load power at V_s=20 V and V_o=25 V.

6.3.4 Efficiency Comparison

Fig. 6.19 shows the variation of steady-state efficiencies of the various converters/control schemes with output power for an input voltage of $V_s=20\ V$. The tri-state boost converter with either DDMC or IDMC scheme achieves an

improvement in efficiency of about 10% over that with 'constant-D_o' scheme, although the converter is still about 5% less efficient when compared to the classical boost converter.

Beyond 40 W of delivered power, the IDMC scheme is seen to be less efficient than the DDMC scheme. This is due to the fact that the free-wheeling interval in DDMC becomes less than that in the IDMC scheme which leads to lower free-wheel inductor current. The reason for this can be explained as follows. For a fixed value of *K-factor*, the length of the free-wheeling interval in DDMC scheme becomes smaller with an increase in load. On the other hand, in the case of IDMC scheme, the length of the free-wheeling interval is independent of load. For the same value of *K-factor*, as will be demonstrated later in the next chapter (Fig. 7.2), the length of the free-wheeling interval obtained using DDMC scheme will be higher than that obtained using IDMC scheme. Thus, ideally, the efficiency obtained using DDMC scheme should be less than that obtained using IDMC scheme for a specific load and *K-factor*. In Fig. 6.19, at 40 W of delivered power, the two efficiencies are observed to match. This indicates an equally long free-wheeling interval in both the cases. Assuming a perfect *K-factor* setting in DDMC scheme (*K=1.3*), using the free-wheeling interval, the value of *K-factor* corresponding to IDMC scheme can be calculated to be 1.3563. This 4.3 % deviation in the setting of *K-factor* in the hardware setup is perhaps responsible for the IDMC scheme being less efficient than DDMC scheme beyond 40 W of delivered power. In practice, this may not be a disadvantage as the *K-factor* can be marginally tuned in the case of IDMC scheme to realize higher efficiencies, if necessary.

6.4 Chapter Conclusions

In this chapter, two variations of a novel multi-variable DMC approach to achieve multiple objectives of attaining good steady-state converter efficiency and good transient response in a tri-state boost converter has been proposed and described. The small-signal model of the tri-state boost converter has been verified experimentally. The design of controllers for the proposed DMC schemes has been discussed. The superior dynamic performance of the tri-state boost converter with DMC schemes over classical boost converter has been verified experimentally. An experimental determination of efficiency shows that the tri-state converter with DMC is about 10% more efficient than that with 'constant-D_o' control scheme and is about 5% less efficient than the classical boost converter. Thus, the tri-state boost converter with DMC scheme offers a compromise between the classical boost converter and the tri-state boost converter with simple 'constant-D_o' control scheme. It is believed that such a DMC scheme can also be used in case of tri-state versions of other boost and buck-boost derived converters to offer improvements in efficiency and in dynamic performance. As mentioned earlier, the size and ratings of power components depend on the control settings i.e the choice of *K-Factor* in the DMC schemes. The next chapter presents a systematic design procedure for selecting of power and control components of the tri-state boost converter employing DMC schemes.

CHAPTER 7

DESIGN AND EVALUATION OF TRI-STATE BOOST CONVERTER

7.0 Introduction

Chapter 6 discussed two variations of a multi-variable dual-mode control (DMC) scheme that effectively exploit the control freedom offered by tri-state boost converter with an aim to attain a good compromise between the contradictory multiple-goals of achieving good dynamic performance and high efficiency. As mentioned in the previous chapter, the dynamic and steady-state performances of the converter under DMC schemes are closely inter-related and in turn decide the size and rating of power components and also the design of feedback controllers. The aim of this chapter is to investigate in greater detail the trade-offs involved in the design of DMC based tri-state boost converter and to present a systematic design procedure for both variations of the DMC schemes. The relation between dynamic and steady-state performances is investigated and used appropriately in selecting the power and control components. An example design is presented and the design is validated through simulations and experiments.

Section 7.1 describes the trade-offs involved in the design of DMC-based tri-state boost converter. Section 7.2 explores the disturbance margins of the converter within which fast dynamic response is ensured. Based on the disturbance margins offered by the converter, section 7.3 presents the design algorithm which involves selection of control and power components. Section 7.4 explains an example design. Section 7.5 presents simulation and experimental results investigating the

performance of converter for disturbances of different magnitudes. Section 7.6 concludes the chapter.

7.1 Trade-Off in DMC of Tri-State Boost Converter

As mentioned in the previous chapter, unlike the case of a classical boost converter in which the size of power components are generally independent of the parameters of the controller, in the case of DMC of tri-state boost converter, the choice of control parameters decide the ratings of the power components. In this section, this aspect is brought out through description of the trade-offs involved in the DMC-based control of tri-state boost converter.

The free-wheeling interval $D_f\ T$ in the converter serves as an extra energy 'reservoir,' the length of which decides the magnitudes of free-wheeling current I_{dc} and average inductor current I_L. The relationship between I_{dc}, average input current I_s, average output current I_o, and D_f is given by (5.6) [repeated here again in (7.1)].

$$\left(\mathrm{I_{dc}}+\frac{\mathrm{V_s D_b T}}{2\mathrm{L}}\right)(1-\mathrm{D_f})=\mathrm{I_s}=\frac{\mathrm{V_o I_o}}{\mathrm{V_s}} \tag{7.1}$$

From (7.1), it may be seen that at a given line and load condition, increasing D_f^* in the IDMC scheme (Fig. 6.5) will result in an increase in I_{dc}. Similarly increasing *K-factor* and hence I_{dc}^* (Fig. 6.3) in the DDMC scheme will result in an increase in D_f.

Setting a high D_f^* in IDMC scheme or a high I_{dc}^* in the DDMC scheme will result in high inductor free-wheeling current I_{dc}, high average inductor current I_L, and hence a large storage of energy. This excess storage helps in achieving excellent dynamic response. This is because, when the load demand suddenly increases, the converter, through a reduction in $D_f\ T$ and an increase in boost interval $D_b\ T$ is able to

release the stored energy as well as boost up the input power drawn from the source. As a result, the dynamic performance is improved. However, for certain types of disturbances (to be discussed in the next section), $D_f\ T$ vanishes and the converter enters a slow two-state operation with the slow control input D_o alone being active (D_b saturated to $1\text{-}D_o$). When operating with a long $D_f\ T$, i.e with D_f^* set high in IDMC scheme or with I_{dc}^* set high in DDMC scheme, fast dynamic property is lost only for extremely large disturbances. Although a high D_f^* (or I_{dc}^*) is desirable from dynamic response point of view, due to the resulting high inductor current I_L, the size and ratings of the power components are increased. Besides, the operating efficiency is also reduced due to high inductor current and associated losses in system parasitics.

On the contrary, a small D_f^* (or I_{dc}^*) results in smaller component size and ratings and better efficiency. However, the converter enters the slow two-state operation even for small disturbances.

The above trade-off involved in selecting D_f^* (or I_{dc}^*) is implemented by the '*K-factor*' in the scheme. The *K-factor* is related to $D_f\ T$ and I_{dc} and hence is also a measure of energy in the 'reservoir.' The DDMC scheme directly uses *K-factor* (7.2) [(6.13) repeated] in deciding the control reference I_{dc}^* (Fig. 6.3).

$$I_{dc} = KI_s = K\frac{V_o I_o}{V_s} \tag{7.2}$$

The IDMC scheme (Fig. 6.5) uses *K-factor* indirectly through its control reference D_f^* (7.3) [(6.16) repeated].

$$\mathrm{K} = \frac{1}{1-\mathrm{D_f}} \Rightarrow \mathrm{D_f} = 1 - \frac{1}{\mathrm{K}} \tag{7.3}$$

It must be noted that even in the IDMC scheme, (7.2) is satisfied, if the inductor ripple current is neglected. Thus, the *K-factor* unifies the design of DDMC and IDMC

schemes. The choice of *K-factor* and hence the extra energy in the reservoir are decided by disturbance margins offered by the converter within which fast-dynamic operation of the output voltage is preserved. The following section defines the disturbance margins of the converter that play a critical role in the converter design.

7.2 Converter Disturbance Margins

Three classes of margins (limits) have been identified in the converter operating under DMC schemes, namely transient margin, quasi-steady-state margin, and steady-state margin. They are defined as below.

(1) Transient margin*:* Transient margin is defined as the maximum disturbance that the converter can tolerate by a reduction in $D_f T$ in the first cycle after a disturbance.

(2) Quasi-steady-state (QSS) margin*:* In the DMC schemes, quasi-steady state refers to the intermediate state (after a transient disturbance) in which the output voltage regulation is complete and the inductor current optimization is still in progress. QSS margins are defined under the assumption that the control input D_o remains practically constant until the output voltage reaches the desired state. QSS margin refers to the limit on the magnitude of disturbances in the input or reference voltage, below which output voltage regulation is fast, being independent of the inductor current optimization. For disturbances of magnitude greater than this, the output voltage regulation is slow due to dependency on the slow inductor current loop.

(3) Steady-state margin: These are the limits beyond which the converter will not be able to meet the system objectives. For example, a hard-limit is set on the minimum value of D_o which in turn limits the maximum possible boost voltage gain (6.2). Any attempt to get a higher gain will result in the control inputs D_b and D_o hitting their

respective saturation levels of 0.9 and 0.1 respectively and the output voltage limited to the maximum possible value (=*10*V_s*).

Of the three classes of margins defined above, steady-state margin is primarily used in determining the suitability of the tri-state converter for a specific application. Apart from this, it does not play any active role in determining the component size and design of controllers. On the other hand, the transient and quasi-steady-state margins are directly involved in determining the *K-factor* and hence decide the trade-off between dynamic response and steady-state performance.

In this section, three important disturbance margins belonging to QSS and transient classes of margins that play a critical role in deciding the converter trade-off are defined. These margins will be used in subsequent sections in the design of DMC scheme that can tolerate a definite disturbance.

7.2.1 Output Voltage Margin (V_{o_margin})

This is a QSS margin. V_{o_margin} is defined as the maximum change in the reference voltage V_{ref} that can be realized by the fast output voltage loop at the expense of the free-wheeling interval $D_f T$. For an output voltage (V_o) demand beyond this margin, the dynamics will be slow due to dependency on the slow-D_o control loop. This margin is computed assuming constant input voltage V_s. Under limiting conditions, maximum V_o (=$V_{o(limit)}$) is obtained when $D_f T$ vanishes. Thus, V_{o_margin} can be derived as below.

$$V_{o\_margin} = V_{o(limit)} - V_o = V_s\left(1+\frac{D_f + D_b}{D_o}\right) - V_s\left(1+\frac{D_b}{D_o}\right) \quad (7.4)$$

$$\Rightarrow V_{o\_margin} = V_s \frac{D_f}{D_o}$$

From (7.4), it may be concluded that a long free-wheeling interval ($D_f\ T$) guarantees a large V_{o_margin}.

7.2.2 Input Voltage Margin (V_{s_margin})

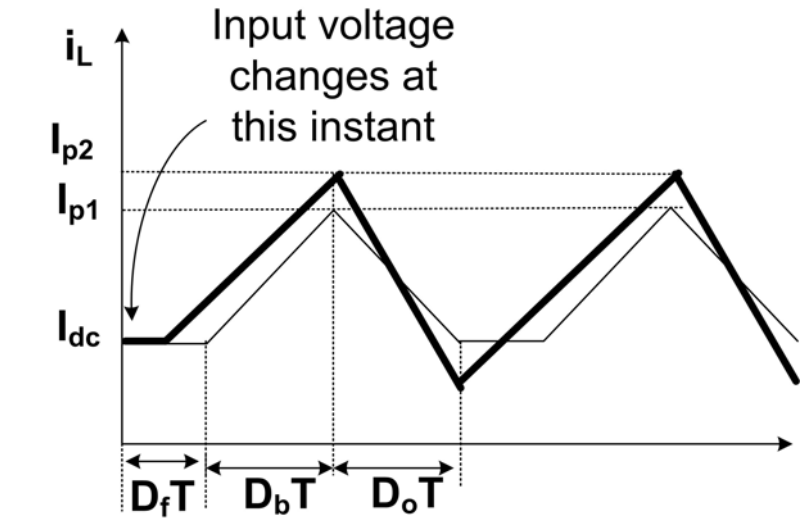
This is also a QSS margin. V_{s_margin} is defined as the maximum dip in V_s that the fast output voltage loop can tolerate at the expense of $D_f\ T$, above which the transient response of output voltage is dependent on the slow-D_o loop. Assuming a constant load current (and voltage) before and after the input voltage disturbance, V_{s_margin} can be derived using (6.1) as follows.

$$\frac{V_o}{V_{s1}} = 1 + \frac{D_b}{D_o}; \qquad \frac{V_o}{V_{s2}} = 1 + \frac{D_f + D_b}{D_o};$$
$$\Rightarrow V_{s\_margin} = V_{s2} - V_{s1} = -V_o \frac{D_o D_f}{D_b + D_o} = -V_{s1} D_f \tag{7.5}$$

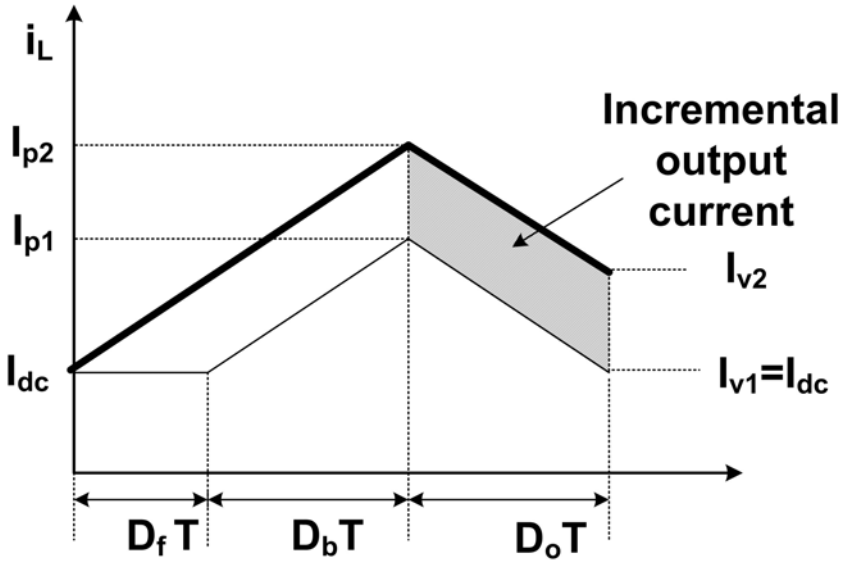
where V_{s1} and V_{s2} signify input voltages before and after the disturbance. From (7.5), it can be seen that an increase in D_f, will permit a large input voltage dip that can be handled by extra energy stored in the inductor itself. This also results in fast dynamic response of the output voltage.

Equation (7.5) also represents the transient-input-voltage margin (i.e. the dip in V_s which the converter can tolerate in the first cycle after disturbance), when an ideal controller is assumed. This can be explained with reference to Fig. 7.1(a). Here, the light and bold waveforms represent the inductor current before and after a dip in V_s (that just hits V_{s_margin}) respectively. The corresponding dip in V_s (transient-input-voltage margin) may be verified to be the same as in (7.5). It must be noted that in practical implementations, analysis of transient-input-voltage margin is of not much use due to its dependency on the controller, which is generally not 'intelligent'

enough to offer a transient as in Fig. 7.1(a). Hence, the simpler QSS margin alone (7.5) is used in the design of the converter.



(a)



(b)

Fig. 7.1. Inductor current waveforms (a) V_s change (b) Load (or V_{ref}) change

7.2.3 Load Current/Power Margin ($(\Delta I_o)_{max}$ [or $(\Delta P_o)_{max}$])

This belongs to the class of transient margins. Load current margin is defined as the maximum incremental load current that the converter can supply in the first cycle after a sudden load (or V_{ref}) increase. In Fig. 7.1(b), the light and bold waveforms

represent the inductor current before and after a load (or V_{ref}) increase that makes $D_f T$ vanish. The shaded area shows the incremental load current.

Let I_{o1} and I_{o2} be the load currents just before and after the load transient. From Fig. 7.1(b), the output current I_{o1} before the load transient can be derived as below.

$$I_{o1} = \left(\frac{I_{p1} + I_{v1}}{2} \right) D_o = \left(\frac{V_s}{L} D_b T + I_{dc} \right) D_o + \frac{\frac{V_s - V_o}{L} D_o T}{2} D_o \tag{7.6}$$

Similarly, the output current I_{o2} after the occurrence of disturbance can be shown to be

$$\begin{aligned} I_{o2} &= \left(\frac{I_{p2} + I_{v2}}{2} \right) D_o \\ &= \frac{I_{p2} + I_{p2} + \frac{V_s - V_o}{L} D_o T}{2} D_o \\ &= \frac{2I_{p2} + \frac{V_s - V_o}{L} D_o T}{2} D_o \\ &= \left(\frac{V_s}{L} (D_b + D_f) T + I_{dc} \right) D_o + \frac{\frac{V_s - V_o}{L} D_o T}{2} D_o \end{aligned} \tag{7.7}$$

From (7.6) and (7.7), the incremental load current can be obtained as follows.

$$\begin{aligned} (\Delta \mathrm{I_o})_{\max} &= I_{o2} - I_{o1} \\ &= \frac{V_s}{L} D_f D_o T \end{aligned} \tag{7.8}$$

This margin is computed assuming that the output voltage V_o does not change appreciably in the first switching cycle after the disturbance. Load power margin $(\Delta P_o)_{max}$ is the product of load current margin $(\Delta I_o)_{max}$ and output voltage V_o. This margin is important as it gives an estimate of the incremental power transferred and hence an indication of the time taken to reach the final state.

It must be noted that for load changes,

$$\begin{aligned} &D_o(final) \approx D_o(initial); \\ &D_b(final) \approx D_b(initial) \\ &\text{Thus, } D_o(final) \le \left(1 - D_b(initial)\right) \end{aligned} \tag{7.9}$$

As a result, for load step changes, the dynamics of V_o is generally independent of the slow-D_o loop. Hence a QSS-class of margin is not defined for load changes.

To summarize, from (7.4), (7.5) and (7.8), it is evident that an increase in energy 'reservoir' interval $D_f T$ in turn increases the dynamic performance range (disturbance margins) of the converter.

7.2.4 Relationships between Disturbance Margins and *K-factor*

In this sub-section, the relationships between *K-factor* and the various defined disturbance margins under IDMC and DDMC schemes are given.

A. IDMC Scheme

In this scheme, the *K-factor* has a straightforward relationship with the control input (reference) D_f^* given by (7.3). Fig. 7.2(b) shows the variation of the wheeling duty-ratio (D_f) with *K-factor*. The converter margins (7.4), (7.5) and (7.8) can be rewritten using (7.3) as below.

$$\begin{aligned} V_{o\_margin} &= \frac{V_s}{D_o}\left(1 - \frac{1}{K}\right) \\ V_{s\_margin} &= -V_s\left(1 - \frac{1}{K}\right) \\ \left(\Delta P_o\right)_{\max} &= V_o * \left(\Delta I_o\right)_{\max} = \frac{1}{K}\left(1 - \frac{1}{K}\right)T\frac{V_s^{\,2}}{L} \end{aligned} \tag{7.10}$$

Equation (7.10) shows that the margins of the converter under IDMC scheme are independent of the power output. Besides, it may be noticed that the load margin

$(\Delta P_o)_{max}$ is dependent on the inductance value L while the other two margins are independent of L.

B. DDMC Scheme

Unlike the IDMC scheme, the disturbance margins offered by the converter in the DDMC scheme do not hold simple relationships with the *K-factor*. Instead the following steps are to be followed to get the disturbance margins.

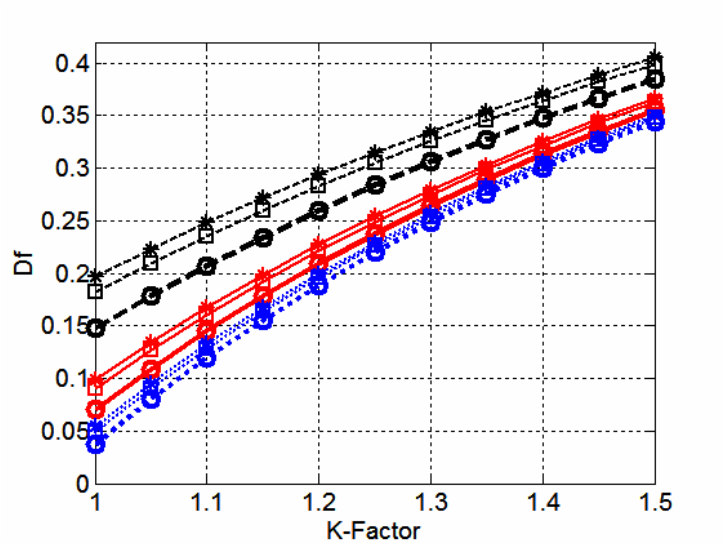
Assuming V_o, I_o, V_s, I_s, L, and *K-factor* to be known, D_o and D_f are needed for finding the disturbance margins (7.4), (7.5), and (7.8). I_o is related to I_{dc} by the following relation.

$$\mathrm{I_o} = \left(\mathrm{I_{dc}} + \frac{\mathrm{V_s D_b T}}{2\mathrm{L}} \right) \mathrm{D_o} \tag{7.11}$$

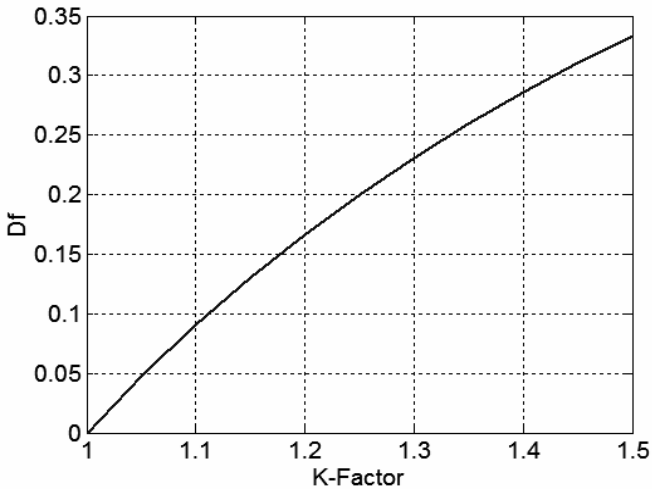
Substituting (5.2) in (7.11) and solving for D_o we get

$$\mathrm{D_o} = \frac{-\mathrm{I_{dc}} + \sqrt{\mathrm{I_{dc}^2} + 4\mathrm{I_o}\left(\mathrm{V_o} - \mathrm{V_s}\right)\mathrm{T}/2\mathrm{L}}}{\mathrm{T}\left(\mathrm{V_o} - \mathrm{V_s}\right)/\mathrm{L}};$$
$$\mathrm{D_b} = \mathrm{D_o}\left(\frac{\mathrm{V_o}}{\mathrm{V_s}} - 1\right); \mathrm{D_f} = 1 - \mathrm{D_b} - \mathrm{D_o} \tag{7.12}$$

where, I_{dc} is directly related to *K-factor* (7.2). Equation (7.12) can be used to find the duty ratios D_f and D_o, using which the disturbance margins offered by the converter can be calculated (7.4), (7.5), and (7.8). Unlike the case of IDMC scheme, in the DDMC scheme, the margins depend both on the inductance value and the power delivered. Fig. 7.2(a) shows the variation of the free-wheeling duty-ratio (D_f) with *K-factor* under DDMC scheme for the tri-state boost converter whose specifications are given in Table 6.1.



(a)



(b)

Fig. 7.2. Variation of free-wheeling interval with *K-factor* (a) *DDMC* scheme (b) IDMC scheme; Legend: square- V_s=20 V, starred- V_s=15 V, circled V_s=10 V, dashed line-P_o=10 W; continuous-P_o=25 W, dotted–P_o=50 W.

7.3 Design of Tri-state Boost Converter

In this section, the design algorithm of DMC based tri-state boost converter is presented. This involves selection of boost inductance L, filter capacitance C, switches (S_m, S_f), and diodes (D_f, D) (refer Fig. 5.2(b)), and controllers used in the scheme. The inputs needed are

1. input voltage range

2. rated load current

3. rated output voltage, and

4. preferred margins of disturbances in reference voltage (V_{o_margin}), input voltage (V_{s_margin}), and load current $(\Delta I_o)_{max}$ [or power $(\Delta P_o)_{max}$].

The preferred margins of disturbance are specific to the application. Choosing high margins will result in high $D_f T$, and hence high inductor current. As mentioned before, this will also affect the efficiency.

7.3.1 Step 1: Disturbance Margins- Selection of *K-Factor*

To start with, the design algorithm assumes an IDMC scheme (even if a DDMC scheme is desired) in which the *K-factor* holds a simple relation with D_f (7.3). As the inductance L is unknown, a plot of V_{o_margin} and V_{s_margin} of converter at different line and load conditions versus *K-factor* is drawn using (7.10). These plots that relate the disturbance margins to the *K-factor* are named as '**disturbance margin curves**.' From the curves, the *K-factor* that gives disturbance margins slightly greater than the design specifications is selected.

7.3.2 Step 2: Selection of Boost Inductance

Assuming nominal operating conditions, with the value of selected *K-factor*, the values of D_f, D_b, and D_o are calculated using (5.1), (5.2), and (7.3). Once *K-factor* is known, I_{dc} is calculated using (7.2). The boost inductance L is calculated on the basis of the percentage (5% to 10%) ripple current under nominal line conditions. At this point, the values of inductance L and free-wheeling current I_{dc} need to be checked. High values of L or I_{dc} result in a large-sized inductor. If such a condition arises, a compromise has to be made on the disturbance margin specifications and the design

has to be started from step 1.

7.3.3 Step 3: Correction of *K-factor*

The output power margin $(\Delta P_o)_{max}$ curves are plotted using (7.10) in the case of IDMC scheme. The value of $(\Delta P_o)_{max}$ at the selected value of *K-factor* is checked to be greater than or equal to the desired margin. If the margin is less than the specification, the value of *K-factor* is increased and the process may be repeated from step 1.

For DDMC scheme, the disturbance margin curves at various line/load conditions (with selected value of L) are plotted using (7.11) and (7.12). Generally, the disturbance margins offered by DDMC scheme are more than those offered by IDMC scheme. This is due to the fact that for the same value of *K-factor*, since the inductor ripple current is neglected in the case of IDMC scheme, the corresponding free-wheeling interval is shorter than that in the case of DDMC. This is also evident from Fig. 7.2. Thus, the selected *K-factor* in DDMC may be reduced appropriately, if needed.

7.3.4 Step 4: Design of Output Capacitor '*C*'

The output capacitor is selected by the well-known methods based either on the hold-up time or on the output voltage ripple constraint.

7.3.5 Step 5: Choice of Switches

The maximum voltage stress across D is V_o and across D_f is V_s. As the potential at point A (Fig. 5.2(a)) cannot be more than $V_s + V_D$ (V_D being the diode drop), the maximum voltage stress across S_m is V_s+V_D and across S_f is V_o. The current rating of

each of the devices is chosen to be at least 1.5 times the inductor peak current I_p under low-line and high-load conditions to allow current overshoots during transients.

7.3.6 Step 6: Design of controllers

The design of controllers is based on the assumption that the variations in D_o are much slower than the variations in D_b. The design uses the small-signal model of the converter (Fig. 7.3) obtained by state-space averaging and linearization given by (7.13), (7.14) [(6.5) and (6.6) repeated].

$$\begin{bmatrix} V_o(s) \\ I_L(s) \end{bmatrix} = G(s) \begin{bmatrix} D_b(s) \\ D_o(s) \end{bmatrix} = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} \begin{bmatrix} D_b(s) \\ D_o(s) \end{bmatrix} \tag{7.13}$$

$$G(s) = \frac{1}{\left(\frac{LC}{D_o^2}s^2 + \frac{L}{RD_o^2}s + 1\right)} \begin{bmatrix} \frac{V_s}{D_o} & \frac{V_s D_b}{D_o^2}\left(\frac{sL(D_b + D_o)}{RD_b D_o^2} - 1\right) \\ \left(sC + \frac{1}{R}\right)\frac{V_s}{D_o^2} & -\frac{V_s(2D_b + D_o)}{RD_o^3}\left(\frac{sCRD_b}{(2D_b + D_o)} + 1\right) \end{bmatrix} \tag{7.14}$$

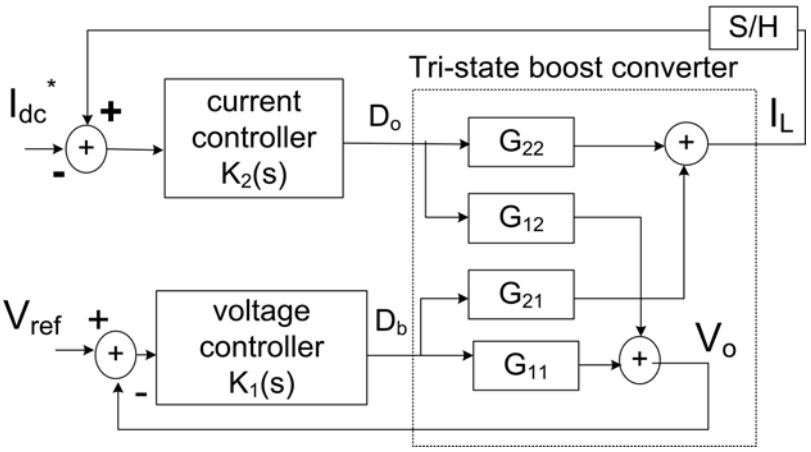
(1) <u>DDMC scheme</u>: The small-signal model of the closed-loop system is shown in Fig. 7.3(a). As mentioned in Chapter 6, since D_o is a slow control variable, the voltage controller $K_1(s)$ (same as *V_cont(s)* (6.27) in Chapter 6) is designed based only on $G_{11}(s)$ (7.14) alone using standard frequency domain techniques such as Bode plots. The slow controller $K_2(s)$ (same as *I_cont(s)* (6.28)) is designed either using $G_{22}(s)$ alone or using the overall transfer function between I_L and D_o (with voltage loop closed) given by (7.15). In both the cases, the effect of sample and hold module is neglected.

$$G_{ddm}(s) = \frac{I_L(s)}{D_o(s)} = G_{22}(s) - \frac{G_{12}(s)G_{21}(s)K_1(s)}{1 + K_1(s)G_{11}(s)} \tag{7.15}$$

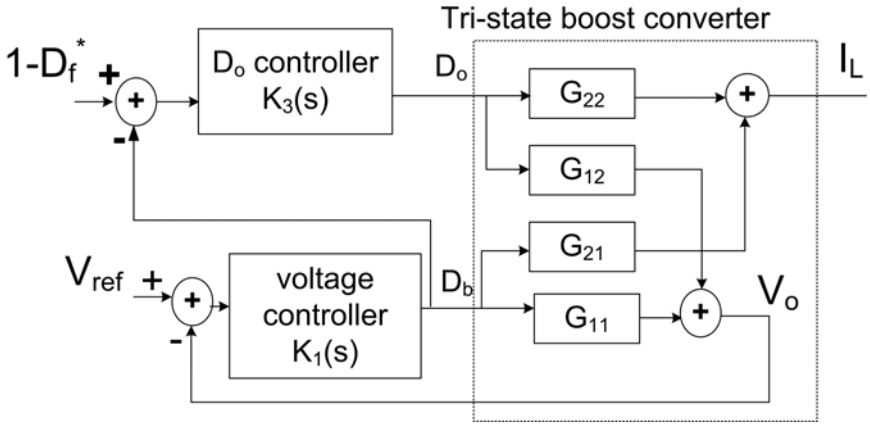
(2) <u>IDMC scheme</u>: The small-signal model is shown in Fig. 7.3(b). The design of $K_1(s)$ is dependent only on $G_{11}(s)$ similar to the case of DDMC scheme. $K_3(s)$ (same

as *I_filter(s)* (6.29)) is a simple filter with a cut-off frequency at most *1/10*th the bandwidth of the voltage loop. The system stability with $K_3(s)$ can be checked using $G_{idm}(s)*K_3(s)$, where $G_{idm}(s)$ is the D_o-*to*-D_b transfer function given by

$$G_{idm}(s) = \frac{D_b(s)}{D_o(s)} = -\frac{G_{12}(s)K_1(s)}{1+K_1(s)G_{11}(s)}. \tag{7.16}$$



(a)



(b)

Fig. 7.3. Small-signal model- (a) DDMC scheme (b) IDMC scheme.

7.4 Design Example

In this section, an example design of a DMC based (DDMC & IDMC) tri-state boost converter of the following specifications is presented.

V_s = 10-20 V, V_o = 25 V, P_o (rated) = 50 W

f_s = 52.3 kHz , V_{s_margin} = -2.5 V , V_{o_margin} = 5V , $(\Delta I_o)_{max}$ =0.05 A [*or* $(\Delta P_o)_{max}$ = 0.05A*25V=1.25 W].

It should be noted that the converter specifications are the same as those of the converter discussed in Chapter 6 (Table 6.2). **The following design steps also verify the selection of power and control components used in Chapters 5 and 6**.

7.4.1 Step 1: Disturbance Margin- Selection of *K-Factor*

To start with, assuming an IDMC control scheme, the variations of V_{o_margin} and V_{s_margin} with *K-factor* under various line and load conditions of the converter are plotted using (7.10) (refer Fig. 7.4). It may be seen that a *K-factor* of *1.2* guarantees a V_{s_margin} of *-2.5 V* (at $V_s \geq 15$ *V*) and a V_{o_margin} of about 5 volts.

At this value of *K-factor*, V_{s_margin} under minimum line conditions (V_s*=10 V*) is only *-1.7 V*, which doesn't meet the specifications. However, as a further dip in the input voltage (at V_s*=10 V*) will trigger the under-voltage protection module, it is sufficient if V_{s_margin} meets the specifications under nominal (V_s *= 15 V*) conditions.

7.4.2 Step 2: Seletion of boost inductance

With the value of *K-factor* set at 1.2*,* under nominal line conditions (V_s*=15 V*), using (5.1), (5.2), and (7.3) it may be verified that

D_f *= 0.1667,* D_b = *0.33333* and D_o = *0.5*.

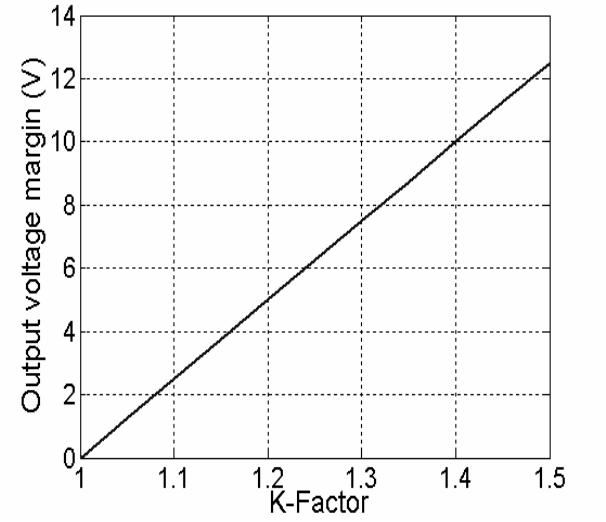
The free-wheeling current 'I_{dc}' is calculated using (7.2) at the maximum loaded condition.

$$\mathrm{I_{dc}} = 1.2 * \frac{25 * 2}{15} = 4\ \mathrm{A}. \qquad (7.17)$$

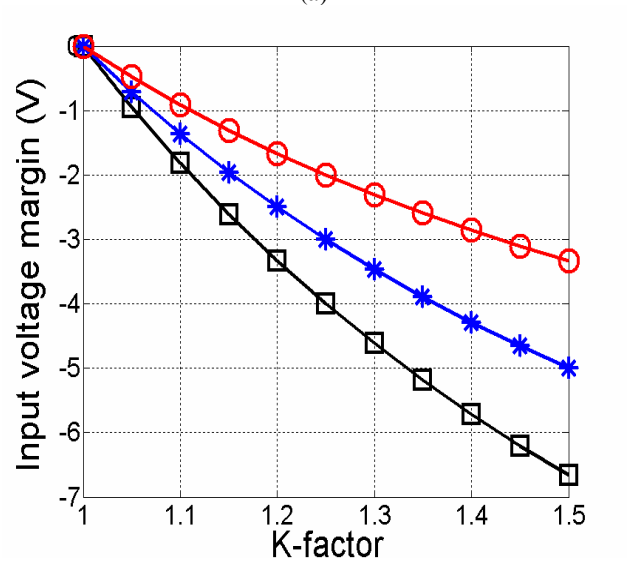
Assuming a *9%* ripple in the inductor current, the inductance can be verified as

$$L = \frac{V_s D_b T}{0.09 * I_{dc}} = \frac{15 * 0.3333 * 19.1e-6}{0.09 * 4} = 265.27\mu H \quad (7.18)$$

(chosen $L = 278\ \mu H$)



(a)



(b)

Fig. 7.4. Variation of disturbance margins with *K-factor* at different load and line conditions (a) V_{o_margin} (b) V_{s_margin}; Legend: square- V_s=20 V, starred- V_s=15 V, circled V_s=10 V.

7.4.3 Step 3: Correction of *K-factor*

The load current margin curves under IDMC scheme are shown in Fig. 7.5. With *K_factor* set at 1.2, the power margin offered by the converter is *1 W* (≈ *0.04 A* * *25 V*) which is less than the specifications (*1.25 W*). Thus, *K-factor* is increased to *1.3*.

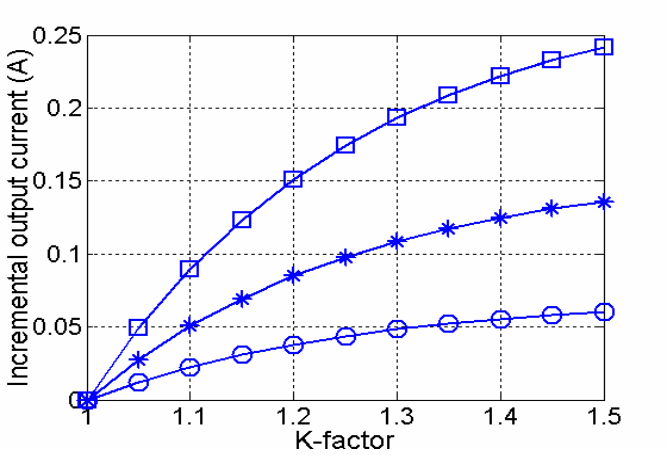


Fig. 7.5. $(\Delta I_o)_{max}$ versus *K-factor*- IDMC scheme (refer Fig. 7.4 for legend).

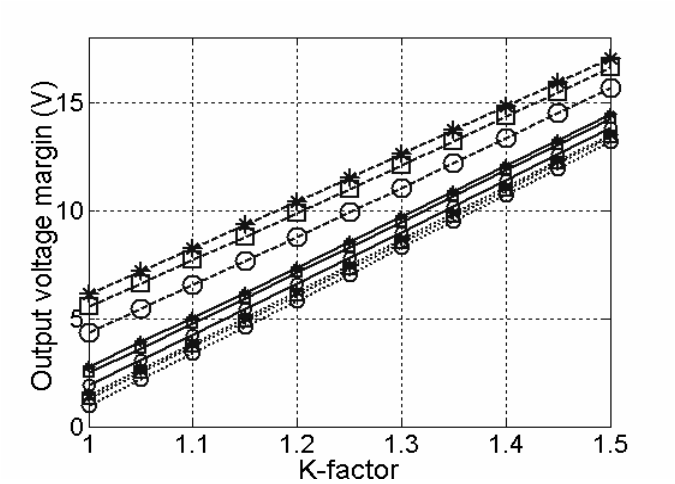
For the DDMC scheme, the disturbance margins are calculated using (7.11), (7.12), (7.4), (7.5), and (7.8). The margin curves are shown in Fig. 7.6. For meeting the margin specifications, the *K-factor* in this case is also set at 1.3. **The above process justifies the selection of *K=1.3* (in both DDMC and IDMC schemes) used in Chapter 6**.

7.4.4 Step 4: Selection of Output Capacitor *C*

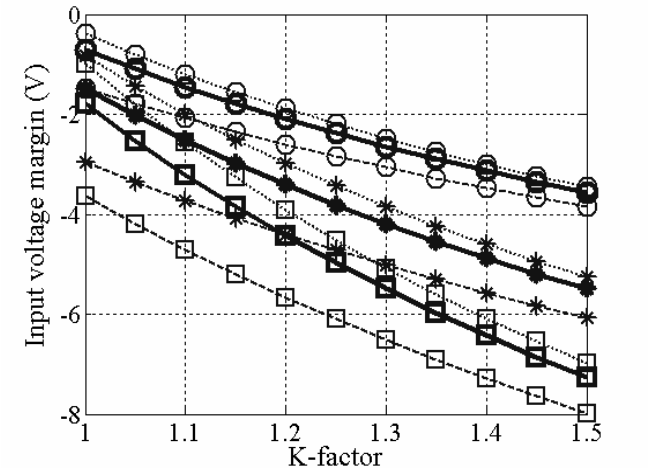
Under minimum-line-maximum-load conditions (V_s*=10 V,* I_o*=2 A,* D_o*= 0.33333*), the output capacitor *C* is selected to limit the ripple in the output voltage to 0.2%.

$$C = \frac{(1 - D_o)TI_o}{V_{o\_ripple}} = \frac{(1 - 0.333) * 19.1e^{-6} * 2}{0.002 * 25} = 509\,\mu F \qquad (7.19)$$

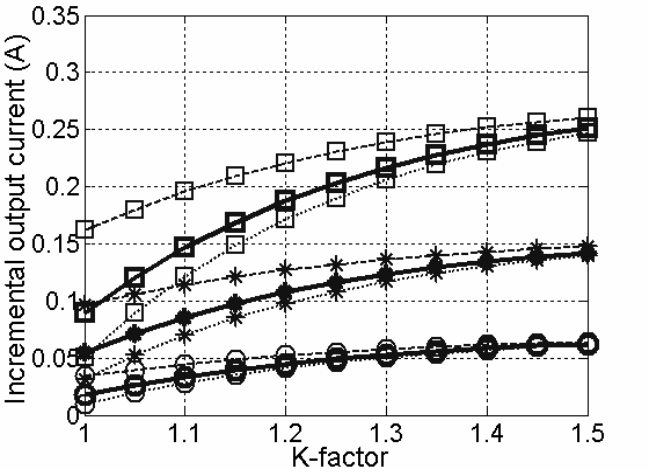
Two electrolytic capacitors whose capacitance sum to *C* = 510 μF have been used in the hardware implementation. (refer Chapters 5 and 6). If necessary, the effect of equivalent series resistance (ESR) of the capacitors upon the voltage ripple can also be considered in the design.



(a)



(b)



(c)

Fig. 7.6. Variation of disturbance margins with *K-factor* (DDMC scheme) (a) V_{o_margin} (b) V_{s_margin} (c) $(\Delta I_o)_{max}$; Legend: square- V_s=20 V, starred- V_s=15 V, circled V_s=10 V, dashed line- P_o=10 W; continuous-P_o=25 W, dotted–P_o=50 W.

7.4.5 Step 5: Design of Controllers

The controller $K_1(s)$ is designed using $G_{11}(s)$ (7.14) to give a small-signal voltage-loop ($G_{11}(s)*K_1(s)$) crossover frequency of about 5 kHz at $V_s = 15V$, $V_o = 25V$, $I_o=1A$. $K_1(s)$ is a cascaded combination of PI and lead-lag controllers given by

$$K_1(s) = 148.8 \cdot \frac{\frac{s}{177}+1}{s} \cdot \frac{\frac{s}{1912}+1}{\frac{s}{36954}+1} \cdot \frac{1}{\frac{s}{2*pi*15000}+1}. \quad (7.20)$$

The last term in (7.20) represents the output voltage filter. It may be noticed that the above equation (excluding the last term) is a repetition of (6.27).

A. Design of Current Controller $K_2(s)$ for DDMC

The current-loop controller is a simple integrator and has been designed by using $G_{22}(s)$ alone. The designed current controller that gave a current-loop ($G_{22}(s)*K_2(s)$) crossover frequency of 500 Hz is given by [(6.28) repeated]

$$K_2(s) = \frac{96.7}{s}. \quad (7.21)$$

B. Design of D_f Controller $K_3(s)$ for IDMC

At $V_s = 15V$, $V_o = 25V$, $I_o=1A$, the selected $K_3(s)$ is given by [(6.29) repeated]

$$K_3(s) = \frac{1}{\frac{s}{1000}+1} \quad (7.22)$$

The transfer function $G_{idm}(s)$ (7.16) was computed. The $G_{idm}(s)*K_3(s)$ loop is theoretically stable up to a filter ($K_3(s)$) cut-off frequency of 6721 rad/s. Hence loop stability is ensured with the filter ($K_3(s)$) selected in (7.22).

7.5 Results and Discussions

A tri-state boost converter with the design specifications, components and controllers designed in section 7.4 has been simulated using MATLAB-SIMULINK. A hardware prototype has also been built and tested. As experimental results demonstrating small-step response with the designed converter and controllers are reported in Chapter 6 (section 6.3), the aim of this section is to investigate the dynamic response of the converter for disturbances that fall within and outside the derived margins. For the purpose of investigation, step disturbances in reference voltage, input voltage, and load current have been investigated.

The definitions of V_{s_margin} and V_{o_margin} are based on the assumption that for disturbances whose magnitude are within the defined margins, the slow control input D_o undergoes only a little change until the output voltage reaches the desired state. It was observed that although the D_o-controllers ($K_2(s)$ (7.21) and $K_3(s)$ (7.22)) make the variations of D_o slower than that of D_b, the rate of change of D_o is not as slow as to verify the slow dynamic performance of the converter when a disturbance violates its defined margin. Thus, in order to carry out such a study, the controllers $K_2(s)$ (7.21) and $K_3(s)$ (7.22) have been re-designed (7.23) to slow down the variations in D_o further.

$$K_2(s) = \frac{9.67}{s};$$
$$K_3(s) = \frac{1}{\frac{s}{21.27}+1} \qquad (7.23)$$

7.5.1 Investigation of Dynamic Performance of Tri-state Boost Converter under IDMC Scheme

In this subsection, the dynamic performance of tri-state boost converter (under IDMC scheme) for disturbances that fall within and outside the defined margins is investigated.

A. Step Changes in Reference Voltage (V_{ref})

Fig. 7.7 shows the experimental response for step-V_{ref} change, the magnitude of which is less than V_{o_margin} (=*7.8 V*). Prior to t_1, the converter is in steady tri-state operation. Between t_1 and t_2, the free-wheeling interval $D_f T$ is zero and the energy in boost inductance L and filter capacitance C is boosted up. At t_2, output voltage V_o is close to V_{ref}. The converter enters another two-state operation involving freewheeling ($D_f T$) and capacitor-charging ($D_o T$) intervals in an attempt to maintain V_o closer to V_{ref}. The desired output voltage V_o is achieved without the intervention of the slow D_o loop. Hence, in spite of the large step disturbance, the response is fast.

Fig. 7.8 shows the experimental step-V_{ref} response, the magnitude of which is greater than V_{o_margin} (= *6.1 V*) at the operating point considered. Between t_1 and t_1', due to the loss of $D_f T$, the initial rate of rise of V_o is high. At t_1', the maximum V_o that can be achieved by making $D_f T$ vanish is reached. Beyond t_1' and up to t_2, the dynamics of V_o are slow due to dependency on the slow- D_o loop. The converter continues to operate in the two-state mode involving $D_b T$ and $D_o T$ until t_2, when the converter enters the two-state operation involving $D_f T$ and $D_o T$ to maintain V_o closer to V_{ref}. At t_3, the converter enters QSS as V_o has settled and I_L optimization is underway.

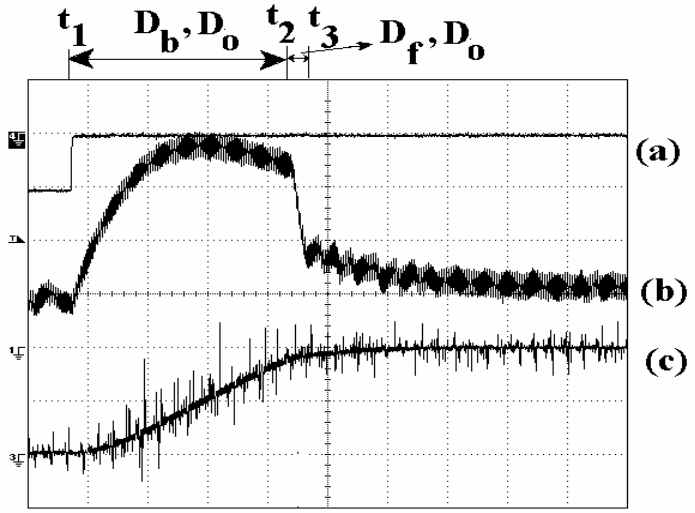


Fig. 7.7. Experimental small-V_{ref} step response (IDMC) at V_s=*15V, R=62.5 Ω*; (a) V_{ref} step (b) i_L (ground at -1 div) (c) V_o from *26 V to 30 V* (oscilloscope in ac mode with ground at -3 div); V_{o_margin}=*7.8 V* scale: voltage: 2 V/div, current: 1A/div, time: 500 μs/div.

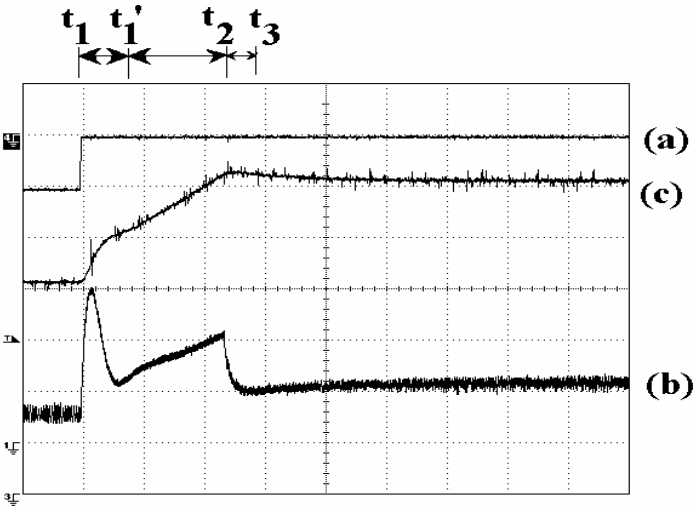


Fig. 7.8. Experimental large-V_{ref} step with IDMC scheme at V_s=*15V, R=62.5 Ω*; (a) V_{ref} step (b) i_L (ground -3 div) (c) V_o from *20.5 V to 30.5 V* (oscilloscope in dc mode with ground at -3 div); V_{o_margin}= *6.1 V*; scale: voltage: 5 V/div, current: 2A/div, time: 5 ms/div.

B. Step Changes in Load Conditions

Figs. 7.9 and 7.10 show the experimental step-load responses. The load current margin ($(\Delta I_o)_{max}$) under these conditions is *0.11 A*. For the small-step-load change, the output voltage dip is practically zero (Fig. 7.9). The V_o dip observed for the large-

step-load change (> $(\Delta I_o)_{max}$) shown in Fig. 7.10 is not only small but the voltage recovery is also fast. The reason for this has been explained in section 7.2.3 (7.9).

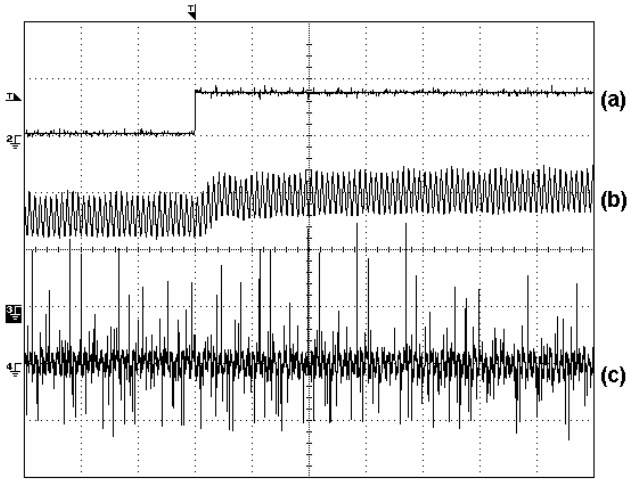


Fig. 7.9. Experimental small-I_o-step (0.4 A to 0.5 A) response at V_o=25 V and V_s=15 V with IDMC scheme (a) step load change (b) i_L (ground at -1 div) (c) V_o (oscilloscope in ac mode with ground at -2 div); $(\Delta I_o)_{max}$ = 0.11 A; scale: voltage: 0.25 V/div, current: 0.5 A/div, time: 200μs/div.

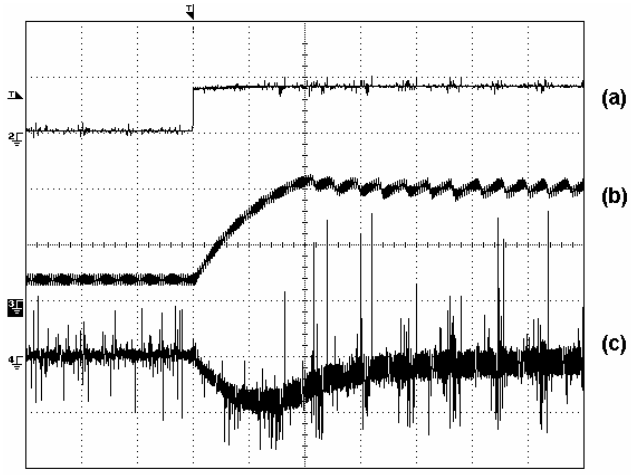


Fig. 7.10. Experimental large-I_o-step (0.4 A to 2 A) response at V_o=25 V and V_s=15 V with IDMC scheme (a) step load change (b) i_L (ground at 0 div) (c) V_o (oscilloscope in ac coupling mode with ground at -1 div); $(\Delta I_o)_{max}$ = 0.11 A; scale: voltage: 0.5 V/div, current: 2 A/div, time: 500μs/div.

C. Step Changes in Input Voltage

Fig. 7.11 shows the simulated response of the converter for a small step change

in input voltage that falls within the defined input voltage margin (V_{s_margin} = *-3.5 V*) at the operating point under consideration. It may be noticed that the output voltage dip is insignificant. As the output voltage error is insignificant, the control effort is also small and as a result, the output voltage recovery is slow. Tri-state operation is not lost during the transient.

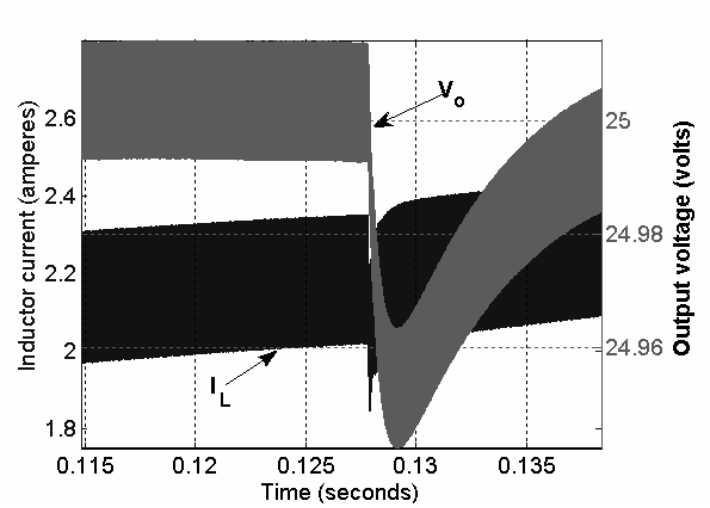


Fig. 7.11. Simulated response (IDMC) for a small dip in input voltage from 15 V to 14 V at V_o=*25 V* and I_o=*1 A*, V_{s_margin} = *-3.5 V*.

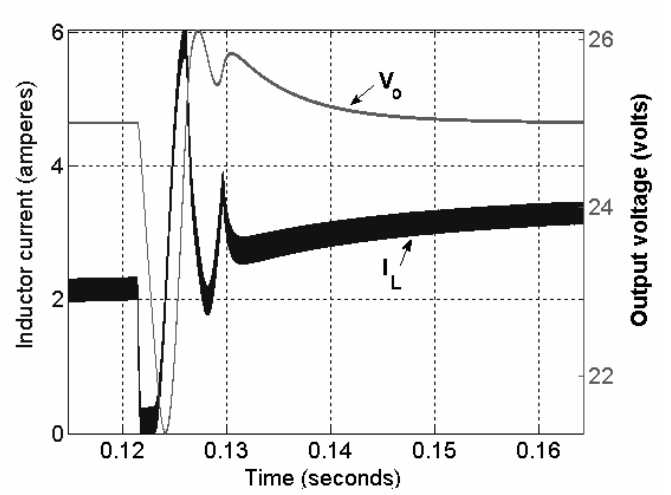


Fig. 7.12. Simulated response (IDMC) for a large dip in input voltage from 15 V to 10 V at V_o=*25 V* and I_o=*1 A*, V_{s_margin} = *-3.5 V*.

Figs. 7.12 shows the simulated response of the converter for a large step change in input voltage that violates the V_{s_margin} (= *-3.5 V*) at the specified operating point. In

this case, the output voltage dip is significant. Besides, the voltage recovery is also dependent on the slow-D_o control loop as may be seen from the transient response.

7.5.2 Investigation of Dynamic Performance of Tri-state Boost Converter under DDMC Scheme

In this subsection, the dynamic performance of tri-state boost converter (under DDMC scheme) for disturbances that fall within and outside the defined margins is investigated.

A. Step Changes in Reference Voltage (V_{ref})

Fig. 7.13 shows the experimental response of the converter for step-V_{ref} change, the magnitude of which is less than V_{o_margin} (= *13.06 V*) Similar to the response observed in the case of IDMC scheme, the two-state operation involving $D_b T$ and $D_o T$ is initially observed followed by the other two-state operation involving $D_f T$ and $D_o T$ to maintain V_o closer to V_{ref}. Once again, the desired V_o is achieved without the intervention of the slow D_o loop and the output voltage dynamics are fast.

Although the response of the converter under DDMC scheme is similar to that obtained with IDMC scheme (Fig. 7.7), it may be noticed that the peak inductor current is higher in the case of DDMC scheme. The difference in inductor currents is mainly attributed to the difference in the steady-state values of D_f under the operating conditions considered (V_s=*15V, R=62.5* Ω). This is also evident from the relatively higher steady-state inductor current observed in the case of DDMC scheme before the occurrence of the disturbance. The steady-state value of D_f under IDMC scheme is 0.23 and under DDMC scheme is 0.32. Due to this large difference in free-wheeling interval, the corresponding inductor current is also boosted up to a large value in the

DDMC scheme when the step disturbance occurs. The higher inductor current has also resulted in a relatively shorter settling time of the output voltage in the case of the DDMC scheme. A reduction in the peak inductor current, if desired, may be achieved by a corresponding reduction in the *K-factor* in DDMC scheme.

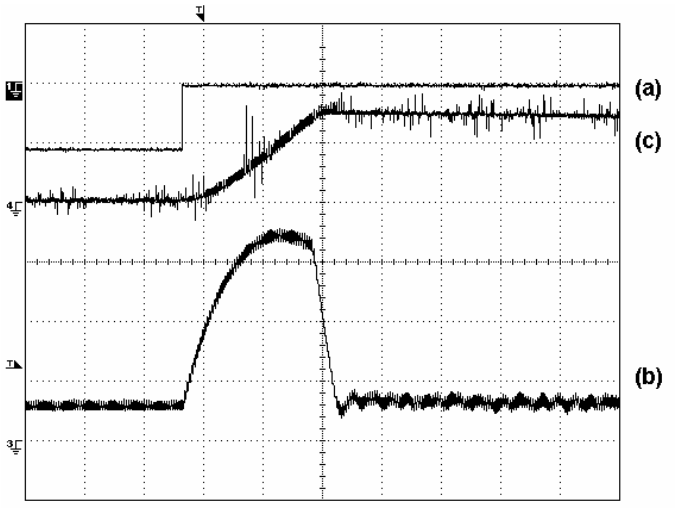


Fig. 7.13. Experimental step response of a tri-state boost converter with DDMC scheme for a large step change in voltage reference at V_s=15V, R=62.5 Ω; (a) V_{ref} step (b) inductor current (ground at -3 div) (c) output voltage from 26 V to 30 V (oscilloscope in ac mode with ground at +1 div); V_{o_margin}= 13.06 V; scale: voltage: 2.5 V/div, current: 2 A/div, time: 500 μs/div.

Fig. 7.14 shows the experimental response of the converter for a large-step change in reference voltage that exceeds the V_{o_margin} (= *9.2 V*) at the specified operating point. It may be noticed that the inductor current in this case rises much faster than that observed in the case of the IDMC scheme (Fig. 7.8). The difference in the rates of rise of inductor current observed in DDMC and IDMC scheme is again attributed to the difference in values of D_f. Given an operating point and a fixed value of *K-factor*, as the free-wheeling interval in the DDMC scheme is longer than that in the IDMC scheme (Fig. 7.2), the initial rate of rise of inductor current due to the vanishing free-wheeling interval is higher in the case of DDMC scheme. Saturation of

inductor is also observed. Due to this, energy is dumped into the output capacitor from the input at a much faster rate resulting in fast dynamic response of output voltage. Thus, the dependency of output voltage dynamics on the inductor current is not very obvious.

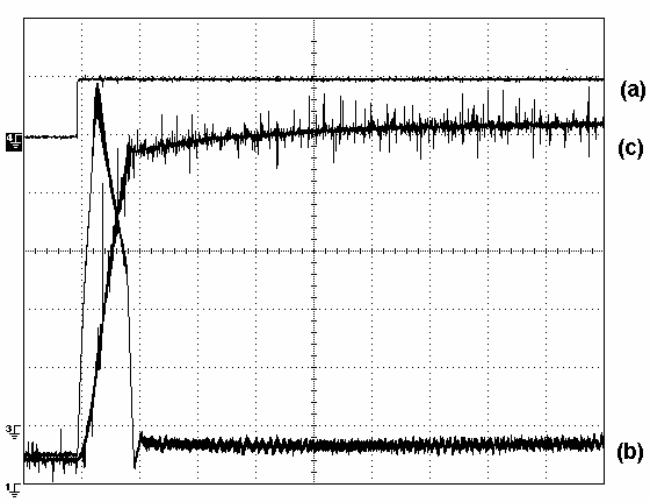
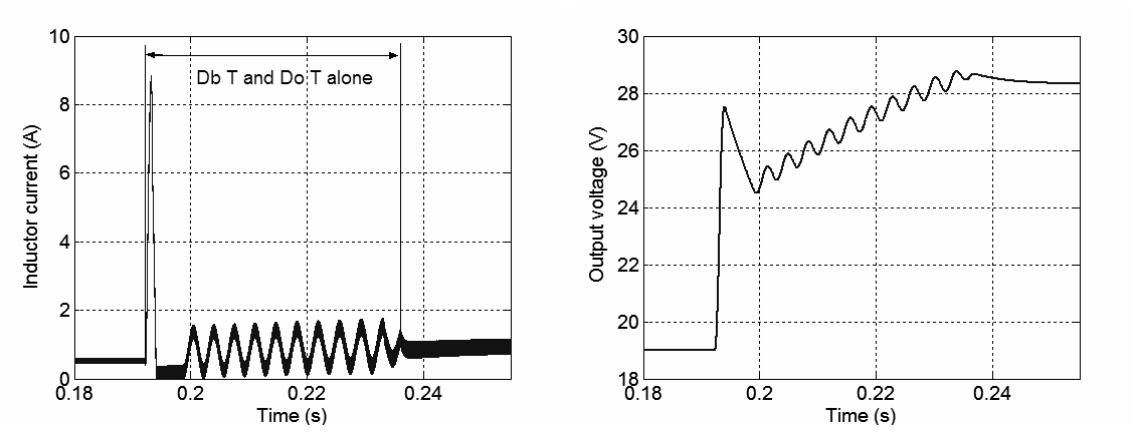


Fig. 7.14. Experimental step response of a tri-state boost converter with DDMC scheme for a large step change in voltage reference at V_s=15V, R=62.5 Ω; (a) step reference change (ground at +2.0 div) (b) inductor current (ground at -4 div) (c) output voltage from 19 V to 30.3 V (oscilloscope in dc mode with -20 V offset and with ground at -3 div); V_{o_margin}= 9.2 V; scale: voltage: 2 V/div, current: 2A/div, time: 1 ms/div.



(a) (b)

Fig. 7.15. Simulated step response of a tri-state boost converter with DDMC scheme for a large step change in voltage reference at V_s=15V, R=62.5 Ω; (a) inductor current (b) output voltage from 19 V to 28.3 V ; V_{o_margin}= 9.2 V.

To show the dependency of output voltage dynamics on the slow-D_o loop in the absence of inductor saturation, simulations using SIMULINK has been carried out. Fig. 7.15 shows the simulated output voltage transients under DDMC scheme without inductor saturation. Here, the dependency of output voltage on the inductor current is clearly observed.

B. Step Changes in Load Conditions

Figs. 7.16 and 7.17 ((i) and (ii)) show the response of the converter under DDMC scheme for step changes in load that fall within and outside the load current margin *($(\Delta I_o)_{max}$ = 0.136 A*). The responses are much similar to those obtained with IDMC scheme (Figs. 7.9 and 7.10). For the small-step load change (Fig. 7.16), the output voltage is practically constant. Even in the case of large-step change in load that violates the load power margin (Fig. 7.17), the voltage dip is almost zero.

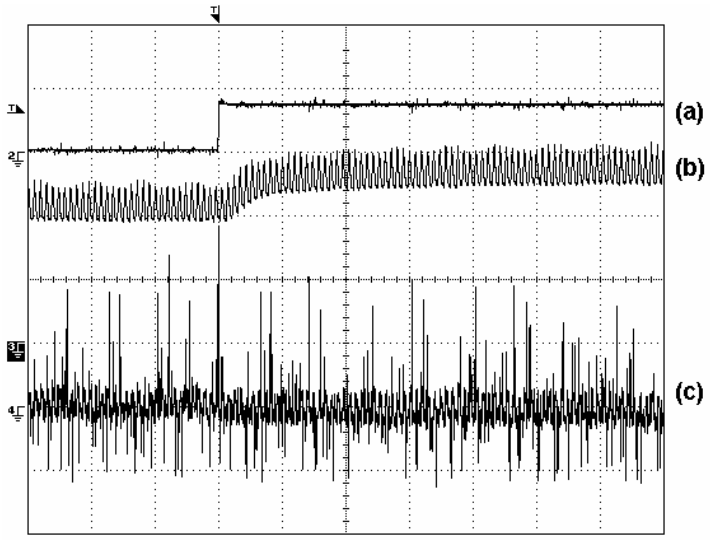
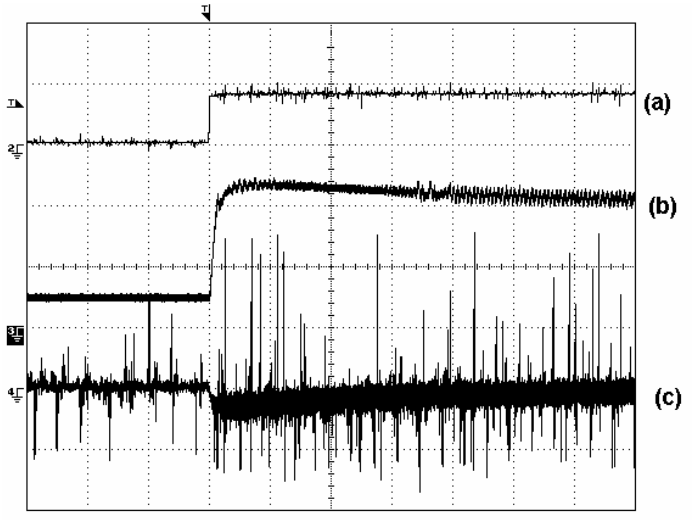
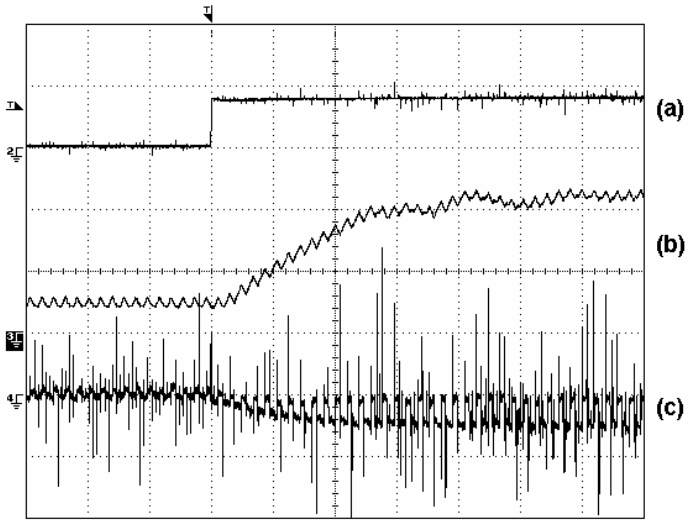


Fig. 7.16. Experimental response for a small step change in load current from 0.4 A to 0.5 A at V_o=25 V and V_s=15 V for DDMC (a) step load change (b) inductor current (ground at -3 div) (c) output voltage (oscilloscope in ac mode with ground at -2 div); scale: voltage: 0.25 V/div, current: 0.5 A/div, time: 200μs/div.



(i)



(ii)

Fig. 7.17. Experimental large-I_o-step (0.4 A to 2 A) response at V_o = 25 V and V_s = 15 V with DDMC scheme (a) step load change (b) inductor current (ground at -1 div) (c) output voltage (oscilloscope in ac mode with ground at -3 div); scale: voltage: 0.5 V/div, current: 2 A/div, (i) time scale : 2 ms/div (ii) time scale: 100 μs/div.

C. Step Changes in Input Voltage

Figs. 7.18 and 7.19 show the simulated step-input voltage (V_s) dip responses under DDMC scheme. Similar to the response observed with IDMC scheme, the output voltage does not change significantly for the small dip (that falls within the defined

V_{s_margin}) in input voltage. The dip in output voltage V_o is high in the other case in which the dip in input voltage violates V_{s_margin} (refer Fig. 7.19). The recovery of output voltage also depends on the slow current loop.

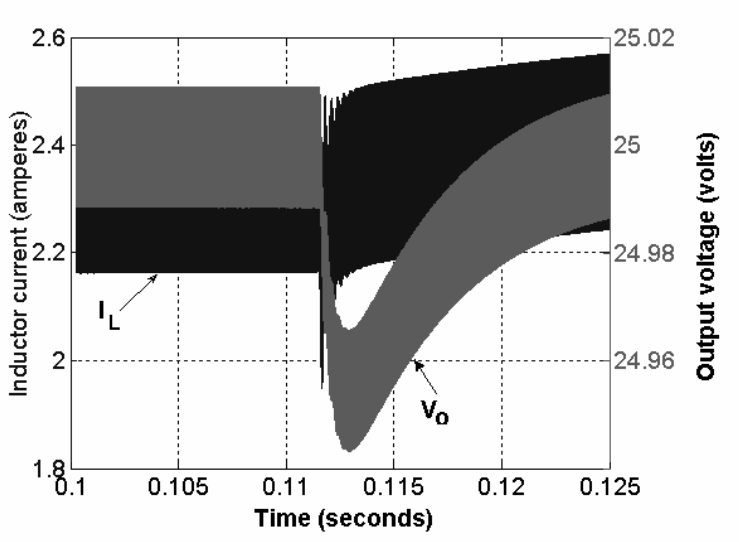


Fig. 7.18. Simulated response (DDMC) for a small dip in input voltage V_s from 15 V to 14 V at V_o=*25 V* and I_o=*1 A*;. V_{s_margin} = -4.2 V.

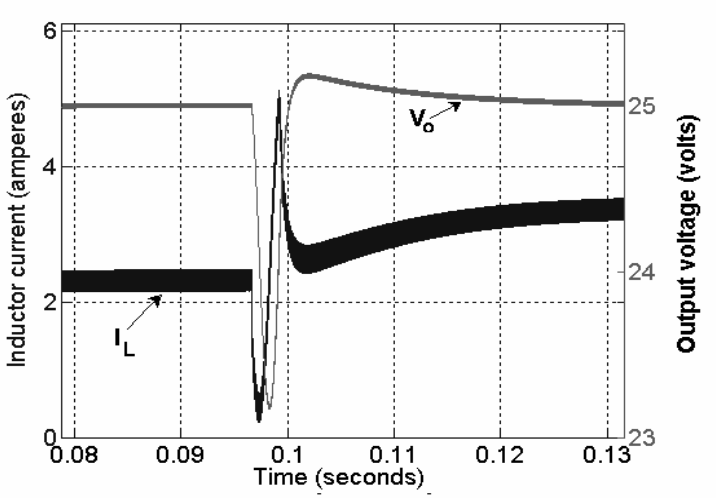


Fig. 7.19. Simulated response (DDMC) for a large dip in input voltage V_s from *15 V* to *10 V* at V_o=*25 V* and I_o=*1 A*. V_{s_margin} = -4.2 V.

7.6 Chapter Conclusions

In this chapter, three disturbance margins that play a critical role in deciding the

trade-off existing between dynamic and steady-state performances of a DMC based tri-state boost converter have been defined. The role of these margins in deciding the size and ratings of the circuit components has been investigated. The systematic design procedure of a DMC based tri-state boost converter has been explained with an example. Simulation and experimental results have been presented to investigate the operation of converter for disturbances which fall within and outside the defined margins. Similar disturbance margins can be defined in the case of other converters belonging to the tri-state family (refer Chapter 5). A similar design approach may be followed for deciding the size and rating of power components. With this, the discussions on dc-dc applications of tri-state class of converters are complete. The next chapter will explore the strengths of tri-state class of converters in single-phase ac-dc power factor correction applications.

CHAPTER 8

APPLICATION OF TRI-STATE CONTROL CONCEPT IN SINGLE-PHASE POWER FACTOR CORRECTION RECTIFIERS

8.0 Introduction

The previous chapters (5, 6, and 7) discussed the dc-dc applications of tri-state class of converters. The discussions were focused primarily on the tri-state boost converter. Boost and buck-boost topologies are also popularly used in single-phase ac-dc power factor correction (PFC) applications. The requirements of power converters to be used in PFC applications are discussed in detail in appendix D. Appendix D also presents a literature survey on popular PFC rectifiers and their associated problems.

The prime objectives of a PFC rectifier are drawing a sinusoidal input current in phase with the ac input voltage, delivering a tightly regulated dc output voltage, and ensuring fast dynamics of operation for sudden changes in line and load conditions. For achieving these goals, as explained in the appendix D, a PFC rectifier should have an additional energy storage element. Besides, two degrees of control freedom are needed for meeting the load-side and line-side demands. Converters belonging to the 'Tri-state' family, on account of the availability of an extra degree of control-freedom, constitute potential candidates for application as PFC rectifiers. Thus, in this chapter, the application of tri-state converters in single-phase PFC is investigated.

To begin with, the suitability of tri-state converters in PFC is described. Following this, a simple and effective control method for unity-power-factor rectifiers

based on cascade buck-boost (CBB) converter, a member of the tri-state class of converters is proposed. The proposed "dual-mode" control method effectively exploits the additional degree of control freedom provided by the CBB converter and achieves sinusoidal input current while providing a tight output voltage regulation. In addition, the control method also de-couples the output voltage control loop from the often-slow input-current-reference generator, resulting in excellent output voltage dynamic response. The theoretical analysis, choice of circuit elements, and the applicable range of operating conditions of the proposed control scheme are also presented. Excellent steady-state and transient performance of the converter are demonstrated through simulation and experimental results. A qualitative comparison of the converter performance with popular PFC converters is also given.

Section 8.1 reviews the goals of a PFC rectifier and the strengths of the tri-state converters in achieving these goals. Section 8.2 investigates the suitability of tri-state boost and tri-state buck-boost-derived converters in PFC application. In section 8.3, a cascade-buck-boost-based PFC rectifier is studied. The dual-mode control scheme for CBB-PFC is proposed and the associated control trade-offs are described. This section also discusses the design of power and control components of the CBB-PFC employing dual-mode control scheme. Simulation and experimental results demonstrating the steady-state and dynamic response characteristics of the converter are presented. A qualitative comparison of DMC-based CBB-PFC with popular single-phase PFC rectifiers is also given in this section. Section 8.4 concludes the paper.

8.1 Achieving Steady-State Goals in a PFC Rectifier

In this section, a possible way of achieving sinusoidal input current and tightly-

regulated output voltage in a single-stage PFC rectifier through storage of second harmonic energy in an inductor is described. These discussions will also form the basis for explaining the suitability of tri-state converters in PFC applications.

Let us consider the PFC rectifier shown in Fig. 8.1. Let the input current ($I_{in}(t)$) be sinusoidal and in-phase with the input voltage $V_{in}(t)$. Neglecting the switching ripple in the input current, the input current and voltage can be written as below.

$$\begin{aligned} I_{in}(t) &= I_m Sin(\omega t) \\ V_{in}(t) &= V_m Sin(\omega t) \end{aligned} \tag{8.1}$$

Here I_m and V_m are the peak ac line current and voltage respectively. The input power ($P_{in}(t)$) is given by

$$P_{in}(t) = V_{in}(t) \bullet I_{in}(t) = V_m I_m \left(\frac{1 - Cos(2\omega t)}{2} \right) \tag{8.2}$$

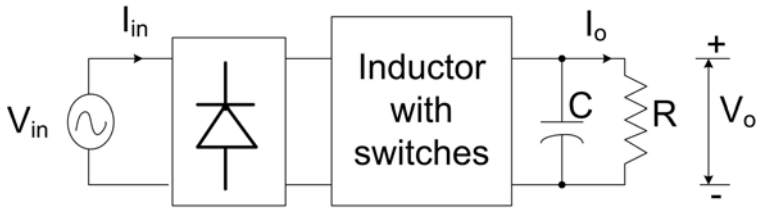


Fig. 8.1. A PFC rectifier with internal inductor energy storage.

It may be noticed from (8.2) that the input power drawn form the utility has a second (line-frequency) harmonic content and a dc content which equals the delivered output power. If the second harmonic energy content reaches the output terminals, the output voltage will have a second harmonic ripple. There are two possible ways to avoid the second harmonic ripple in the output voltage. They are as follows.

1. With an inductor designed to store insignificant energy, a large output capacitor is needed to minimize the second harmonic ripple in the output voltage. This approach is popular and is used in classical boost and buck-boost PFC rectifiers.

2. The inductor with switch network can be used to absorb the second harmonic content of the input power and prevent it from reaching the output terminals. Theoretically, no output capacitor is needed in this case.

Of the above two approaches, generally, the output voltage dynamics of PFC rectifiers adopting the first approach will be poor due to large output capacitor and in many cases, due to the associated control scheme (Details are given in appendix D). The second approach based on inductive energy storage has not been explored much in literature. The following discussions describe the approach.

Let us assume that all the second harmonic content of input power is absorbed by the inductor and switch network itself, so that the output voltage is free from ripple at twice the line frequency. Assuming an ideal converter operation, using (8.2), the instantaneous inductor volt-ampere can be verified to be

$$VA_L(t) = V_m Sin(\omega t) \bullet I_m Sin(\omega t) - \frac{V_m I_m}{2} = -\frac{V_m I_m Cos(2\omega t)}{2}, \qquad (8.3)$$

To find the inductor current and the corresponding voltage across the inductor that will yield this VA (8.3), let us assume that the inductor current $I_L(t)$ has a DC component (I_{dc}) and a variable component($i_L(t)$) given by

$$I_L(t) = I_{dc} + i_L(t) \qquad (8.4)$$

From (8.3) and (8.4),

$$(I_{dc} + i_L(t)) \bullet L\frac{di_L(t)}{dt} = -\frac{V_m I_m Cos(2\omega t)}{2} \qquad (8.5)$$

The following steps are followed to solve for $i_L(t)$.

$$(I_{dc} + i_L(t)) \bullet di_L(t) = -\frac{V_m I_m Cos(2\omega t)}{2L} dt \qquad (8.6)$$

Integrating (8.6), we get

$$I_{dc} i_L(t) + \frac{\left(i_L(t)\right)^2}{2} = -\frac{V_m I_m Sin(2\omega t)}{4L\omega} + {I_R}^2 \quad \text{(integral constant } {I_R}^2\text{)} \qquad (8.7)$$

Solving for $i_L(t)$

$$i_L(t) = \frac{-2I_{dc} \pm \sqrt{4{I_{dc}}^2 - \frac{4V_m I_m Sin(2\omega t)}{2L\omega} + 8{I_R}^2}}{2} \qquad (8.8)$$

$$\begin{aligned} I_L(t) \;=\; I_{dc} + i_L(t) \;&=\; I_{dc} + \frac{-2I_{dc} \pm \sqrt{4{I_{dc}}^2 - \frac{4V_m I_m Sin(2\omega t)}{2L\omega} + 8{I_R}^2}}{2} \\ &= \pm\sqrt{{I_{dc}}^2 - \frac{V_m I_m Sin(2\omega t)}{2L\omega} + {I_M}^2} \end{aligned} \qquad (8.9)$$

Discarding the negative value, the overall inductor current is given by

$$I_L(t) = \sqrt{{I_{dc}}^2 + {I_M}^2 - \frac{V_m I_m}{2L\omega} Sin(2\omega t)} = \sqrt{{I_k}^2 - \frac{V_m I_m}{2L\omega} Sin(2\omega t)} \qquad (8.10)$$

The current component I_M (=8 I_R^2) in (8.10) is an integration constant. The current I_k can be shown to be the rms value of the inductor current as follows.

$$I_L(rms) = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\sqrt{{I_k}^2 - \frac{V_m I_m}{2L\omega} Sin(2\omega t)}\right)^2 d(\omega t)}$$

$$I_L(rms) = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left({I_k}^2 - \frac{V_m I_m}{2L\omega} Sin(2\omega t)\right) d(\omega t)} = I_k \qquad (8.11)$$

Fig. 8.2 shows the waveforms of the various quantities. Ideally, with an inductor current following the relation in (8.10), the PFC rectifier can deliver a well-regulated output voltage while drawing a sinusoidal input current. It should be noted that the current I_k can be set at any value by the designer. However, it should not be less than a certain minimum in order to meet the PFC goals. This point will become obvious later in this chapter.

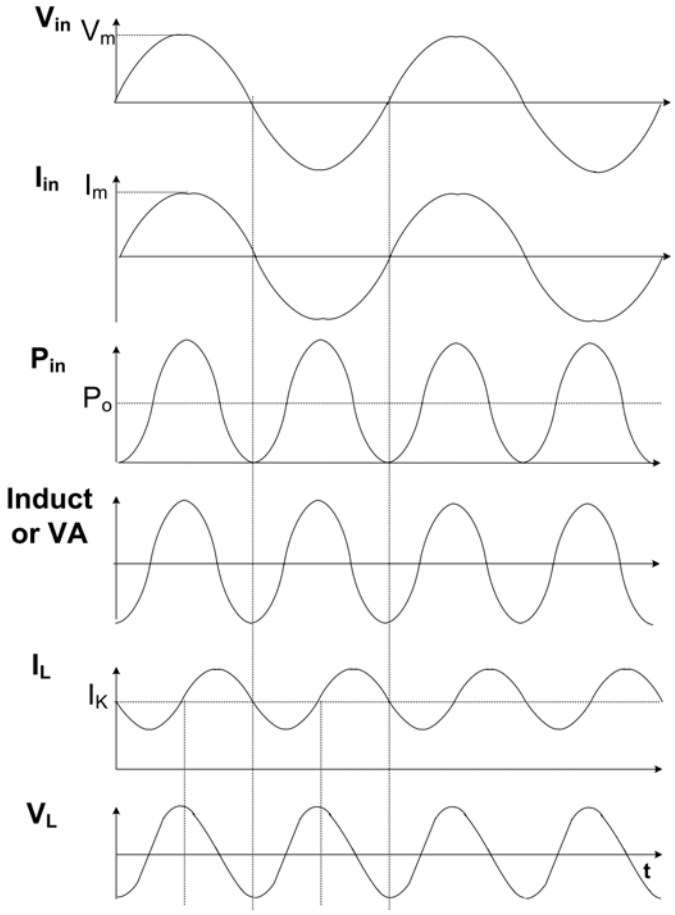


Fig. 8.2. Dual goal achievement- PFC rectifier, V_L-voltage across inductor, I_L- inductor current, VA_L- inductor volt-ampere.

8.2 Suitability of 'Tri-state' Class of Converters in PFC Applications

In this section, the suitability of tri-state boost and tri-state buck-boost-derived converters in PFC applications is investigated. Approaches based on both capacitive and inductive (second-harmonic) energy storage are considered and explained.

8.2.1 Suitability of Tri-state Boost Converter

A prime advantage of tri-state boost PFC rectifier (both inductive and capacitive energy storage) over classical boost PFC rectifier is that by appropriately controlling the switches, it is possible to limit the output voltage overshoots within permissible

limits without boosting up the energy in the inductor. This is not possible in a classical boost PFC rectifier.

The tri-state boost PFC converter with most of the second harmonic energy stored in the output capacitor does not offer much advantage over the classical boost PFC scheme. The reasons are listed as below.

1. The output capacitor needed in the tri-state PFC converter is as large as the one needed in the case of classical boost converter.
2. With negligible energy stored in the inductor, the tri-state operation will be lost in most part of the line frequency cycle and the converter will just function as a simple boost converter with two switches in series. This will result in additional losses in the extra switch. Besides, the losses due to reverse recovery of the diodes (D and D_f) will be higher than that due to reverse recovery of the single diode in boost PFC rectifier. These factors will result in a lower efficiency of tri-state boost PFC rectifier when compared to that of a classical boost PFC rectifier.
3. Fast dynamics of output voltage is also not ensured due to large-size of the filter capacitor. Besides, it is believed that similar to a boost PFC scheme, any attempt to enhance the dynamic response of output voltage in tri-state boost PFC rectifier will result in increased distortion of the input current.

The tri-state boost PFC rectifier with second harmonic energy stored in the boost inductor also does not offer significant advantage over the classical boost PFC scheme. This can be explained as below.

With the inductor storing all the second harmonic energy, the average current in the inductor will be high. Assuming a large inductor, the inductor current 'I_L' can be

considered to be a constant (with negligible ripple). Neglecting the effect of switching, the input and output currents of the scheme can be written as

$$\begin{aligned} I_o(t) &= I_L * D_o(t) \\ \left|I_{in}(t)\right| &= I_L * (D_b(t) + D_o(t)) = I_L * D_b(t) + I_o(t) \end{aligned} \tag{8.12}$$

Under any loaded condition, the average load current I_o will become more than $|I_{in}(t)|$ during some part of the ac cycle (around the zero-cross), during which a solution for '$D_b(t)$' does not exist (refer (8.12)). Any attempt to deliver the desired output current during these conditions (be setting $D_o(t) > 0$) will result in increased input current distortions. On the other hand, if $D_o(t)$ is set to zero under these conditions, second harmonic ripple will start appearing in the output voltage which would demand a large capacitance.

Thus it may be concluded that in spite of the presence of extra degree of control-freedom, the tri-state boost converter with either inductive or capacitive second-harmonic energy storage does not offer much advantage over the classical approach.

8.2.2 Suitability of Tri-state Buck-Boost-Based Converters

Single-phase power factor correction (PFC) using a buck-boost-based converter has a wide output voltage range. Unlike the popular boost-PFC converters, the buck-boost-based PFC converter can even deliver an output voltage lower than the peak ac input voltage, if required.

Tri-state buck-boost-based PFC converters (buck-boost, flyback, and cascade-buck-boost (CBB) converters) with second harmonic energy stored primarily in the output capacitor, do not offer any significant advantage over their corresponding classical counterparts. Thus, in this sub-section, the suitability of these converters

with second harmonic energy stored in the inductor (coupled inductor in the case of flyback converter) in PFC applications is investigated.

With the inductor storing all the second harmonic energy, the average current in the inductor will be high. Assuming a large inductor, the inductor current 'I_L' can be assumed to be a constant (with negligible ripple). Under these conditions, neglecting the effect of switching, the input and output currents can be written as

$$\begin{aligned} I_o(t) &= I_L * D_o(t) \\ \left|I_{in}(t)\right| &= I_L * D_b(t) \end{aligned} \tag{8.13}$$

With a large inductor current, the above two equations can be satisfied under all operating conditions in the buck-boost-based PFC rectifier i.e., a total decoupling of input current control and output voltage control can be achieved. Thus, the extra degree of freedom offered by the tri-state operation in the case of buck-boost-based PFC rectifier can be effectively exploited to achieve both sinusoidal input current and ripple-free output voltage. To demonstrate this, a cascade-buck-boost-based PFC rectifier is explored in detail in the rest of this chapter.

8.3 Cascade-Buck-Boost PFC Converter (CBB-PFC)

In this section, the tri-state operation of CBB-PFC rectifier (Fig. 8.3) with inductive energy storage is explored. A novel control method for the CBB-PFC converter is proposed. The proposed 'dual-mode control (DMC)' method is a modified form of the IDMC scheme discussed in Chapter 6 for the tri-state boost converter. The control method is simple to implement and meets the PFC objectives. As mentioned before, the second harmonic component of input power is absorbed in the converter itself and is prevented from reaching the output terminals, resulting in low output voltage ripple. The proposed control method independently controls the

output voltage and input current. The separation of output voltage control from the input current control makes fast dynamic response of the converter possible for limited range of load step changes. However, for large load changes, the converter offers slow dynamic response.

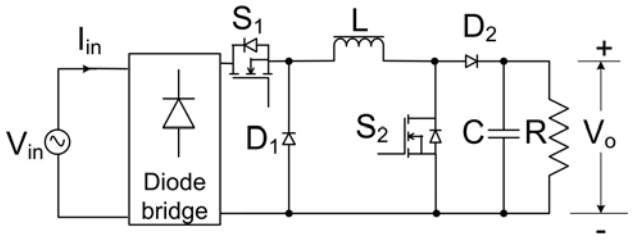


Fig. 8.3. Cascade buck-boost- PFC (CBB-PFC) converter

The important discussions in this section include a brief review of CBB converter operated in tri-state mode, description of the proposed control scheme and its limitations, trade-off between inductor size and efficiency, and selection of inductor and output capacitor. The anticipated good steady-state and transient performance are verified through simulation and experimental results on a prototype converter that was designed and built. A qualitative comparison of the converter performance with the popular single-phase PFC converters is also given.

8.3.1 CBB Converter- Degrees of Control-Freedom

The CBB converter (Fig. 8.3) has four valid operating states corresponding to the status of S_1 and S_2. In the proposed PFC scheme, the converter is operated as a tri-state converter. When operated as a dc-dc converter, the inductor current under cyclic-steady-state has three intervals of operation (refer Fig. 8.4), namely 'boost' interval ($D_b\ T$) {both S_1 and S_2 ON}, 'free-wheel' interval ($D_f\ T$) {S_2 ON and S_1 OFF}, and 'capacitor charge' interval ($D_o\ T$) {both S_1 and S_2 OFF}. The fourth state (S_1 ON and S_2 OFF) is invalid. Also, in any switching cycle,

$$D_b + D_f + D_o = 1. \tag{8.14}$$

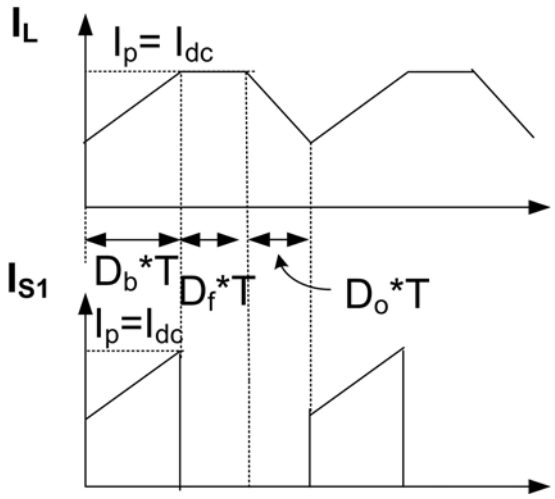


Fig. 8.4. Inductor (I_L) and switch 'S_1' (I_{S1}) waveforms.

The control freedom offered by CBB converter in the form of an inductor-free-wheeling interval can be used to shape the inductor current as in (8.10) and hence meet the steady-state PFC goals. In addition, as mentioned before, this interval also helps in de-coupling the output voltage control from the input current control (8.13). This helps in achieving excellent transient performance as will be demonstrated later in the chapter.

8.3.2 Dual-Mode Control Scheme for CBB-PFC

In this sub-section, the control requirements of CBB-PFC are discussed. The dual-mode control (DMC) scheme for PFC is introduced and described. The control trade-offs are described in detail.

A. Control Requirements and Grouping of Control Inputs of CBB-PFC

Two loops, namely an input current loop for shaping the input current to a sinusoid and an output voltage loop for delivering a well-regulated output voltage are

needed in the control scheme. A third loop is needed to optimize the rms value of inductor current 'I_k,' (8.10). With these three loops in place, the input current is shaped sinusoid, the output voltage is tightly regulated, and the inductor current is also optimized for better performance.

As the CBB-PFC rectifier has two independent (D_b, D_o,) and one dependent control input (D_f) and three control objectives to be met, there is a need to group each of the control inputs to an objective that has to be met. As the input current is drawn only during the boost interval (D_b T), D_b is used for shaping the input current. Similarly, since output capacitor is charged only during the 'capacitor-charging' interval (D_o T), D_o is used to control the output voltage. Neglecting the switching ripple in the inductor current and using (8.10), the average input and output currents can be written as

$$\left|I_{in}(t)\right| = D_b(t) I_L(t) \Rightarrow D_b(t) = \frac{\left|I_m \mathrm{Sin}(\omega t)\right|}{\sqrt{I_k{}^2 - \frac{V_m I_m}{2L\omega}\mathrm{Sin}(2\omega t)}} \tag{8.15}$$

$$I_o(t) = D_o(t) I_L(t) \Rightarrow D_o(t) = \frac{V_o / R}{\sqrt{I_k{}^2 - \frac{V_m I_m}{2L\omega}\mathrm{Sin}(2\omega t)}} \tag{8.16}$$

The above two equations assume that the control inputs D_b and D_o are totally independent. Such an independence is possible only under the conditions when the inductor current is high enough so that

$$D_b(t) + D_o(t) \le 1. \tag{8.17}$$

Condition (8.17) is satisfied by the third (slow) loop that controls I_k. This is done indirectly by adjusting the ac-cycle-averaged steady-state value of free-wheeling duty

ratio (D_f^*). The free-wheeling interval serves as a 'reservoir' of extra energy (similar to a tri-state boost converter). The longer the free-wheeling interval, the higher the current I_k (refer Fig. 8.6), the larger the stored energy, and hence better is condition (8.17) met. The added advantage of having a higher D_f is that for a step change in load, the converter offers good dynamic response as the excess energy in the inductor is readily released by a reduction in the free-wheeling interval, under transient conditions. However, for large load changes, the inductor may lose all its energy and the dynamics will be slow. This will be demonstrated later.

B. Dual-Mode Control (DMC) Scheme

The proposed dual-mode control (DMC) scheme for the CBB-PFC rectifier is shown in Fig. 8.5. As pointed out earlier, the scheme has three control loops, namely

1. A charge control [39], [40] based input current (I_{rect}) shaping loop that decides D_b. As the input current is pulsed, to avoid ringing and oscillations in the sensor circuit, the inductor current is sensed and is integrated during the '$D_b T$' interval to get the input current.
2. A fast output voltage error loop that decides D_o.
3. A slow D_f-error loop that decides the peak value of rectifier current ($I_{rect(pk)}^*$) to get the required inductor current I_k satisfying (8.17).

In the DMC scheme, when the free-wheeling interval vanishes to zero, D_b becomes the 'master' control input with dependency only on the input current error. Control input D_o becomes the 'slave' control input with saturation at 1-D_b. The reason for these choices can be explained as follows. Let us assume instead D_o to be the master and D_b to be the slave control input. When a load (increase) step occurs, the output voltage dips. D_o increases in an attempt to draw more energy from the

inductor for maintaining the output voltage. As a result, D_f is reduced to zero at first followed by a reduction in D_b. With a reduced D_b, the energy input from the ac source is also brought down. This cuts down the energy supply to the inductor and worsens the output voltage dip. The system will not be able to recover from such a transient. To avoid this D_b is given the highest priority, followed by D_o, and then D_f.

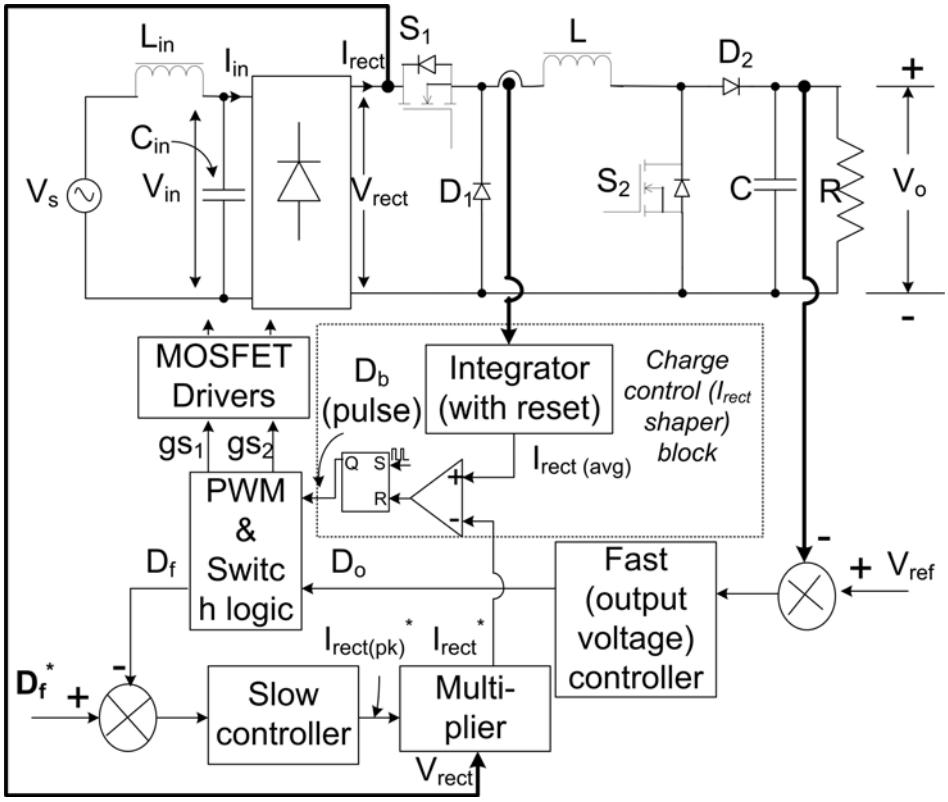


Fig. 8.5. Dual-mode Control scheme for CBB-PFC rectifier

C. DMC of CBB-PFC- Trade-Offs and Limitations

The trade-offs in the CBB-PFC converter will be explained with respect to the converter that was designed, simulated and built. The specifications of the converter are V_s = 85-110V, 60 Hz, V_o = 100 V, and I_o (rated) = 1 A. The component values chosen were L = 13.6 mH, C = 470 µF, L_{in} = 700 µH, and C_{in} = 0.94 µF. For the purpose of analysis, the effect of line filter (L_{in}, C_{in}) is neglected in the sections to come and V_{in} is assumed to be equal to V_s (Fig. 8.5).

The first trade-off in CBB-PFC exists between size of the inductor and operating efficiency of the converter. In the proposed PFC scheme, the second harmonic energy is absorbed in the inductor. If the inductance is low, high losses (due to parasitic resistances) occur in the power converter due to high inductor current. High inductor current also results in high crest factor of the input current causing EMI problems. A reduction in inductor current and crest factor of input current can be achieved by increasing the inductance value. However, this increases the size of the inductor. Increasing the inductor size can be expected to slow down the transient performance of the converter.

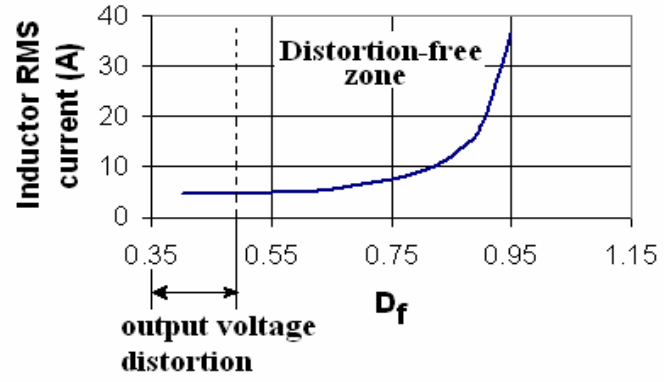


Fig. 8.6. Variation of inductor rms current with D_f^* at V_s= 85 V, P_o=100 W.

The choice of free-wheeling duty reference D_f^* introduces another trade-off between steady-state efficiency and meeting the objectives of PFC rectifier. At an operating point, D_f^* decides the rms value of inductor current I_k. Setting a high value of D_f^* in the control scheme results in a high inductor current and hence a large energy storage (refer Fig. 8.6). Although, this results in excellent steady-state and transient response, on the downside, it increases the component size and ratings and lowers the operating efficiency of the converter. On the other hand, setting a very low value of D_f^* is also not possible as there is a minimum ('limiting') D_f^* corresponding to each operating line and load condition below which second (line frequency) harmonic

distortions will start appearing at first in the output voltage followed by input current distortions.

This 'limiting' D_f^* at each operating condition is obtained by solving the non-linear constrained optimization problem given by (8.18).

$$\begin{aligned} &\text{minimize} \frac{1}{\pi}\int_0^{\pi}\left(D_f(\omega t)\right)d(\omega t) \\ &\text{subject to } D_b(\omega t)+D_o(\omega t)\le 1 \quad \forall \omega t \end{aligned} \tag{8.18}$$

Expanding (8.18) using (8.15)-(8.17)

$$\begin{aligned} &\text{minimize} \quad \frac{1}{\pi}\int_0^{\pi}\left(1-\frac{\left|I_m \sin(wt)\right|+V_o/R}{\sqrt{I_k{}^2-\frac{V_m I_m}{2L\omega}Sin(2\omega t)}}\right)d(\omega t) \\ &\text{subject to} \quad \frac{\left|I_m \sin(wt)\right|+V_o/R}{\sqrt{I_k{}^2-\frac{V_m I_m}{2L\omega}Sin(2\omega t)}}\le 1 \quad \forall\, \omega t \end{aligned} \tag{8.19}$$

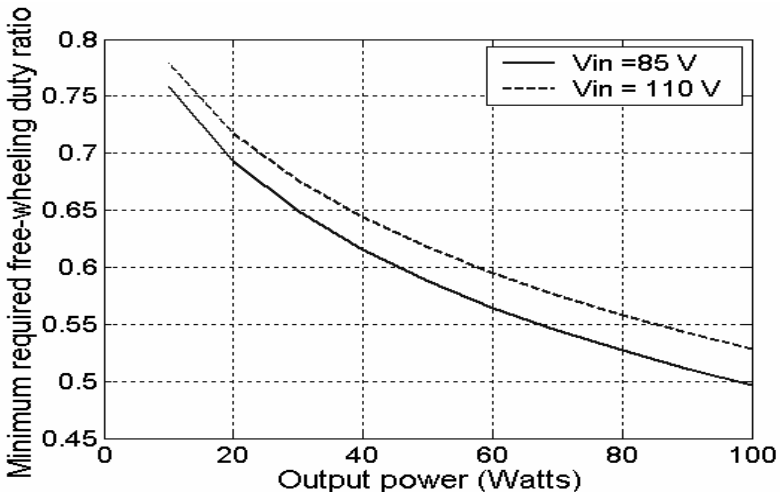


Fig. 8.7. Variation of 'limiting' D_f* with operating conditions, at V_o=100 V

The solution of this optimization problem (8.19) will be the minimum cycle-averaged D_f^* that minimizes the inductor current I_k, while allowing D_b and D_o to vary

freely to achieve sinusoidal input current and tight output voltage regulation (8.17). A plot of this minimum D_f^* at various line/load conditions is shown in Fig. 8.7. It may be noticed that the 'limiting' D_f^* needed at high-line and light-loaded conditions is higher than that needed at low-line and high-loaded conditions.

8.3.3 Selection of Power/Control Circuit Components

Given the ratings of a PFC rectifier, this section describes the selection of power circuit components of the CBB converter. The choice of components of the prototype CBB-PFC converter (V_s=85-110V, 60 Hz, V_o = 100 V, I_o (rated) = 1 A) that was built and tested is presented here as an example.

A. Selection of Inductance '*L*'

Unlike the case of a boost-based PFC wherein the size of power circuit components are generally independent of the control parameters and settings, in the case of CBB-PFC, the reference D_f^* also plays an important role in deciding the inductor size and energy storage and hence the rating of the power switches. The inductor must be chosen in such a way that the minimum of free-wheeling interval in an ac cycle just touches zero, while still satisfying the input/output PFC requirements (8.15)-(8.17). Under such inductor 'optimum storage' conditions

$$\text{maximum}\left(D_b(\omega t) + D_o(\omega t)\right) = 1,\ 0 \le \omega t \le \pi . \tag{8.20}$$

Using (8.15) and (8.16), (8.20) can be rewritten as follows.

$$\text{maximum}\left(\frac{\left|I_m \sin(wt)\right| + V_o/R}{\sqrt{I_k^{\,2} - \frac{V_m I_m}{2L\omega}\text{Sin}(2\omega t)}}\right) = 1, 0 \le \omega t \le \pi \tag{8.21}$$

Given the worst case operating conditions (minimum line and maximum load) and assuming an ideal converter operation (efficiency = 1), the unknowns in the above equation are the inductor current I_k, the inductor value L, and the cycle-instant at which the above relation is maximized. Under 'optimum storage' conditions the maximum of equation (8.21) was found using Mathematica [73]. It was seen that in most cases, the maximum occurred approximately at $\omega t = \pi/4$ radians.

Thus (8.21) can be simplified as

$$\frac{\left|I_m\right|/\sqrt{2} + V_o/R}{\sqrt{I_k^{\,2} - \frac{V_m I_m}{2L\omega}}} \approx 1, \quad \omega t = \frac{\pi}{4}\,\text{rad} \tag{8.22}$$

The above equation relates I_k and L. Table 8.1 shows a comparison between inductor currents I_k at V_o=100V, V_s =85 V, I_o= 1A (for different values of inductance L) calculated using (8.22) and (8.21).

TABLE 8.1. COMPARISON OF INDUCTOR CURRENTS CALCULATED USING EXACT (8.21) AND APPROXIMATE (8.22) RELATIONS

L (mH)	15	13.6	10.8	5.5	2.75
I_k (using (8.22))	4.745	4.940	5.425	7.283	10.06
I_k (using (8.21))	4.735	4.924	5.413	7.277	10.06

Thus, it may be concluded that (8.22) may be sufficient in designing the inductor. The inductor rms current I_k is chosen to be a multiple of the maximum input rms current under minimum line and maximum load conditions. Equation (8.22) is then solved to find the actual inductance value. For the power converter under consideration, at V_s=*85 V* and I_o *(rated) = 1 A*, the input current I_{in} (assuming ideal converter operation and neglecting the effect of line filter) is *1.17 A*. Taking into consideration the reduced operating efficiency and increased input current crest factor

due to high inductor current, the rms value of inductor current I_k is chosen to be about 4.25 times the input current. Thus, with $I_m=1.17*\sqrt{2}$, $R=100\ \Omega$, $I_k=4.25*I_{in}$, the inductance L can be calculated as *13.1 mH* using (8.15). A **laminated iron core inductor** **of *L=13.6 mH*** has been selected in order to keep the size and cost low. Although a laminated iron core inductor has been used, it will be demonstrated through experimental results in section 8.4.4 that the converter performance in terms of efficiency is not affected.

B. Selection of Output Capacitor '*C*'

The output capacitor is selected based on the required hold-up time. Although energy is stored in inductor L as well, the storage is insufficient to meet hold-up time requirements. For the CBB rectifier under consideration, the output capacitor designed (without considering the energy storage in L) to hold the output voltage above 75 V (75% of rated output voltage) for about 10 ms is 457 μF. If the storage in inductor is also considered, the capacitor requirement is reduced to 440 μF. In the hardware implementation, a 470 μF capacitor has been used.

C. Selection of Diodes and Switches

Table 8.2 summarizes the maximum voltage stress across the various devices based on which the switches and diodes may be selected. The maximum current in all the devices listed in Table 8.2 is equal to the peak inductor current. As inductor current limit has been set at 10 A in the experimental set up, the devices have to be rated for a minimum of 10 A.

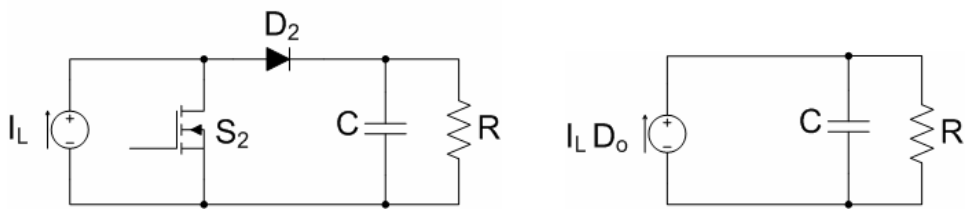
TABLE 8.2. VOLTAGE STRESS ACROSS VARIOUS SWITCHES

S_1	S_2	D_1	D_2	Bridge diodes
V_m(=156 V)	V_o (= 100 V)	V_m	V_o	V_m

D. Controllers and Hard-limits Set in the DMC Scheme

The reference value of free-wheeling interval (D_f^*) in the control scheme (Fig. 8.5) has been set at *0.57*. From Fig. 8.7, it can be seen that with this D_f^*, second (line frequency) harmonic ripple in output voltage and distortions in input current will start appearing when the power delivered falls below 50 W (at V_s = 85 V).

The maximum value of D_b has been limited to 0.75. In addition, D_b is also limited when the inductor current exceeds the current limit which was set at 10 A. This current limit module is not shown in Fig. 8.5 for the sake of simplicity.



(a) (b)

Fig. 8.8. Simplified converter model for design of voltage-loop converter (a) current-fed converter model (b) averaged model with diode D_2 replaced by current source.

Although the DMC scheme is simple, because of the non-linear nature of the converter/control system, system modeling was difficult. A simple design approach for voltage-loop controller is to model the converter as a current source feeding an RC-load as shown in Fig. 8.8. With this approach, the D_o-to-V_o transfer function of the converter can be written as follows.

$$\frac{V_o(s)}{D_o(s)} = \frac{I_L R}{RCs+1} \tag{8.23}$$

Using (8.23), the voltage loop controller was designed to be

$$T_v(s) = 2.36\frac{\frac{s}{7770}+1}{\frac{s}{11223}+1} \cdot \tag{8.24}$$

Due to the lack of a simplified model relating D_f to $I_{rect(pk)}$, the corresponding controller that operates on the D_f error loop to generate $I_{rect(pk)}^{*}$ has been designed based on computer simulations using MATLAB SIMULINK and tuned during experiments in the hardware prototype model. The designed PI-controller is given by

$$T_c(s) = 38.8\frac{\frac{s}{77.6}+1}{s}. \qquad (8.25)$$

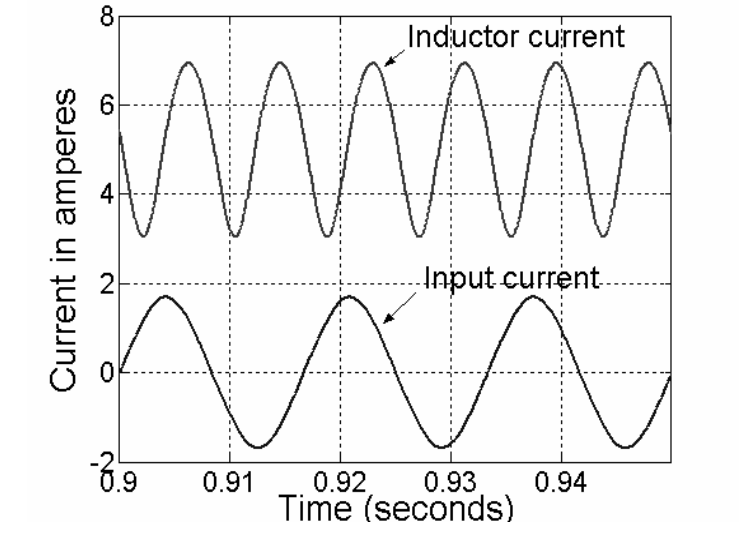
8.3.4 Simulation and Experimental Results

A CBB converter of the specifications mentioned earlier (in section 8.3.2(C)) has been designed, simulated using MATLAB SIMULINK, and a hardware prototype has been built and tested. Simulation models are given in Appendix B. Hardware implementation details are given in Appendix C. Figs. 8.9 and 8.11 show respectively the simulated and experimental waveforms under certain line and load conditions. In both cases, the inductor current is seen to follow the relation (8.10).

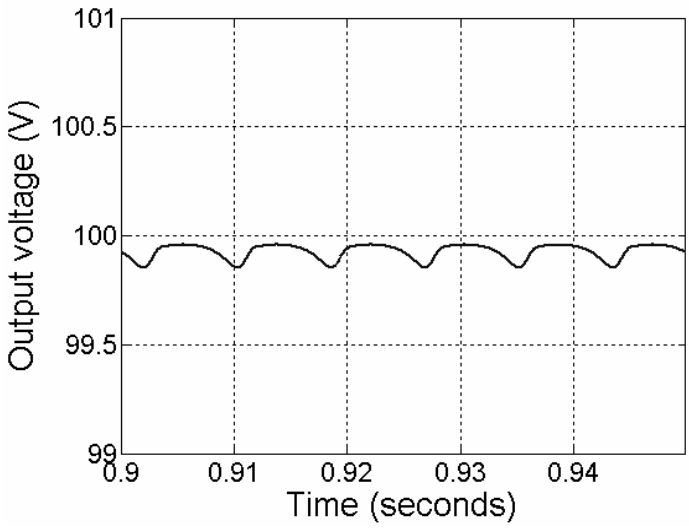
The small (about 0.15 V) second harmonic ripple observed in the output voltage (Fig. 8.9 (b)) is due to the fact that the selected voltage controller (8.24) is not able to vary D_o fast enough to minimize the ripple. To verify this, simulations were carried out using a voltage controller having 10 times the gain of that in (8.24) [poles and zeros remaining the same]. The results are shown in Fig. 8.10. It may be noticed that the output voltage ripple in this case is reduced by almost $1/10^{th}$ of that obtained with the original controller in (8.24). In the experimental set-up, such a high gain on the voltage controller led to noise amplification. A better layout may avoid this problem.

As the second harmonic energy is absorbed in the inductor itself, the output voltage ripple in experimental waveforms (Fig. 8.11) is only about *0.4 %.* Fig. 8.11(e) shows the various frequency components of the input current. The overall THD of the

input current is *3.35 %* . The rms values of various components are $I_{(fundamental\ 60Hz)}=1.46217$ A, $I_{(180Hz)}=0.025$ A, $I_{(300Hz)}=0.025$ A, and $I_{(420Hz)}=0.0224$ A. Thus, from Figs. 8.11(b) and 8.11(e), it may be concluded that the input current is nearly sinusoidal.

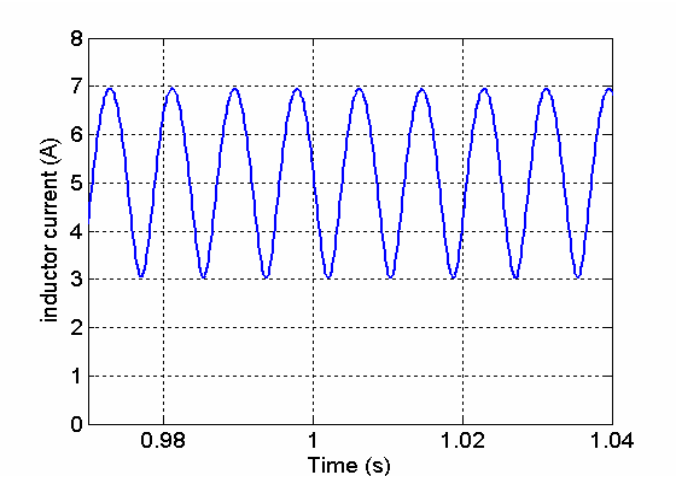


(a)

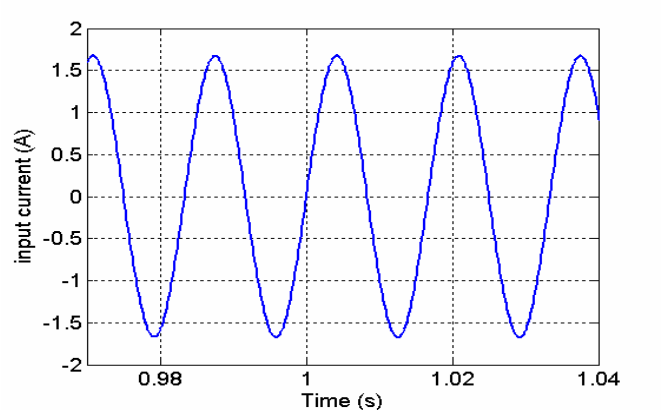


(b)

Fig. 8.9. Steady-state waveforms of DMC based CBB-PFC rectifier at V_s=85 V, V_o=100 V, I_o=1 A, D_f^*=0.57 (a) Input and inductor currents (b) Output voltage.



(a)



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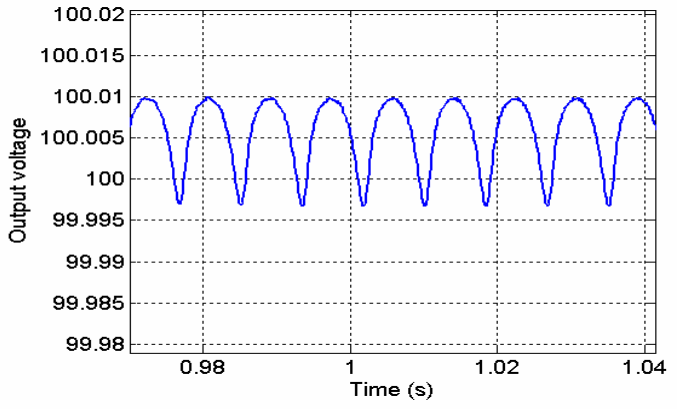


(c)

Fig.8.10. Simulated steady-state waveforms of DMC based CBB-PFC rectifier at V_s=85 V, V_o=100 V, I_o=1 A, D_f^*=0.57- Investigation with increased voltage-loop gain (a) Inductor current (b) input current (c) output voltage.

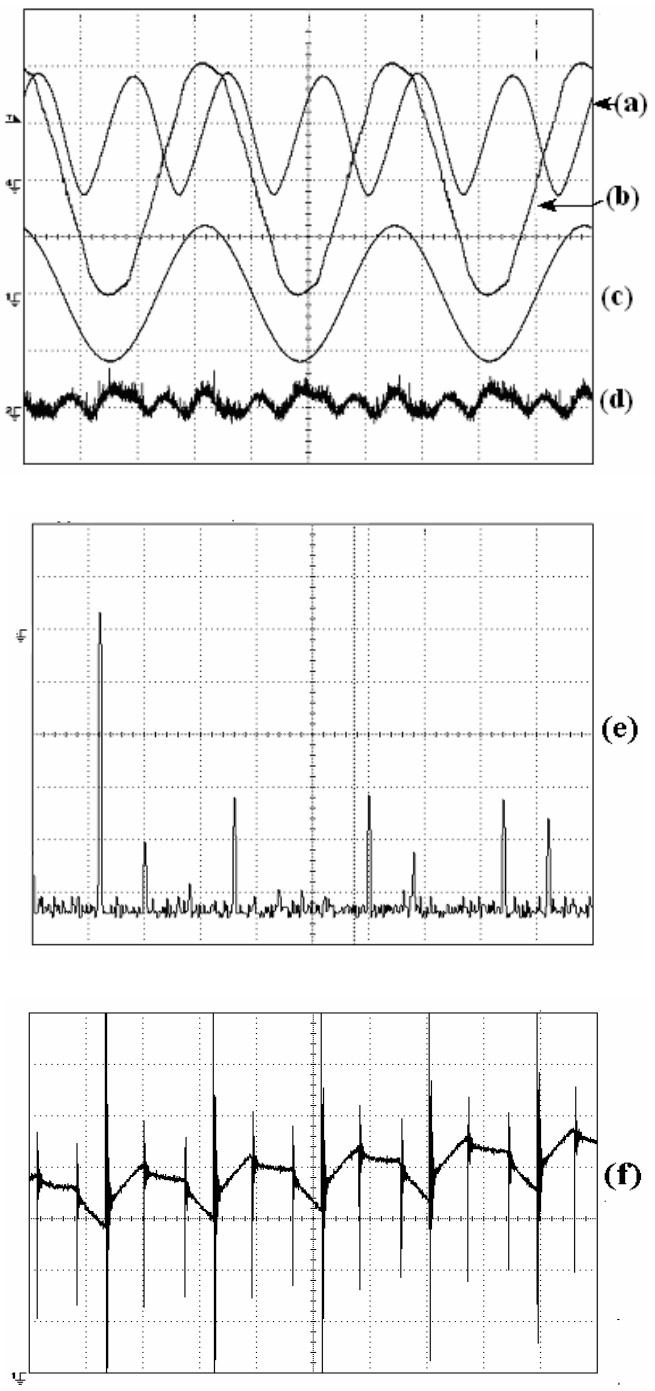


Fig. 8.11. Experimental steady-state waveforms at V_s=85 V, V_o=100 V, I_o=1 A. (a) inductor current (ground at -1 div, scale: 2A/div) (b) input current (scale: 1A/div) (c) input voltage (scale: 100 V/div) (d) output voltage (oscilloscope in ac-coupling mode with ground at -3 div, scale: 1V/div); time scale: 5ms/div (e) Harmonic spectrum of input current; scale: x-axis:50 Hz/div, y-axis: 10dBA/div; GND at +2 div (f) Inductor current (zoomed) showing tri-state operation (scale: 0.1 A/div, waveform has an offset of -2.7 A time: 10 μs/div.

The inductor current in Fig. 8.11(f) demonstrates tri-state operation at switching frequency (50 kHz). The core loss at 50 kHz is believed to be low as the inductor ripple current and the flux variations in the core are much smaller than their corresponding DC and twice-the-line-frequency (120 Hz) components. The jumps observed in the inductor current at the beginning of free-wheeling and boost intervals are believed to be attributed to the parasitic capacitance of the inductor. This can be explained as below.

Fig. 8.12 shows the equivalent model [83]-[85] of laminated iron-core inductor. The equivalent inductance L_{ac} and resistance R_{ac} are frequency dependent quantities. R_{ac} models the skin and proximity effects. The parallel capacitance C_w models the turn-to-turn and turn-to-iron stray capacitances.

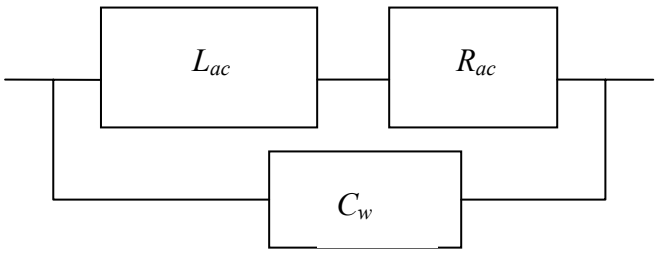


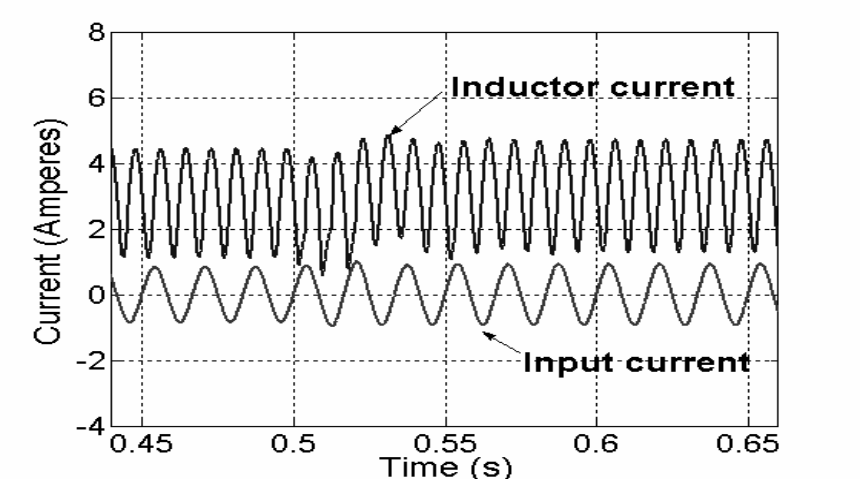
Fig. 8.12. Equivalent model of laminated iron-core inductor

The inductor model in Fig. 8.12 may be used to explain the jumps observed in the inductor current waveform (Fig. 8.11(f)). At the beginning of 'boost' interval (D_b T), when S_1 and S_2 are switched on, the equivalent capacitance C_w, which is initially charged to 100 V (output voltage) discharges and recharges in the opposite polarity to the magnitude of the input voltage. This charging current appears as jumps in the measured inductor current waveforms. Similarly at the beginning of 'free-wheeling' interval (D_f T), the capacitance discharges its stored charge which accounts for the jump encountered in the inductor current observed at the beginning of the interval.

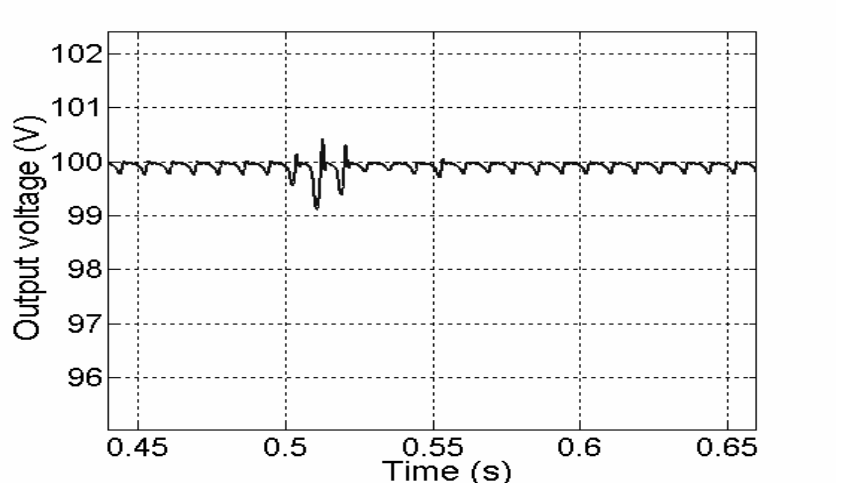
The inductor current jump observed at the beginning of the 'capacitor-charging' interval (D_o T) is on account of the charging of C_w to the output voltage. The maximum change of polarity of voltage across the inductor is experienced at the beginning of the 'boost' interval. As a result, the magnitude of inductor current jump is also higher in this case, as may be observed from Fig. 8.11(f). In spite of the presence of capacitance 'C_w' and its effect on the switching waveforms, the input and output conditions of the PFC rectifier are satisfied suggesting laminated iron core inductors in such energy storage applications. Further investigations needed in this aspect are left for future exploration.

Fig. 8.13 shows the simulated response for a small-step change in load. For this load change, the output voltage recovery is very fast. Figs. 8.14 and 8.15 show respectively the simulated and experimental responses of the converter for a large-step change from half load to full load. As soon as the load step occurs, the output voltage starts dipping and the fast (output voltage) controller increases D_o. As $I_{rect(pk)}^*$ is decided by the slow-D_f loop, the input current does not change much immediately. With little change in energy drawn from the source and increased energy drawn by the load, the inductor loses all its energy. The output voltage dips further and the dip continues until the input current rises up to charge the inductor. Once the inductor current is sufficiently high to meet the demand, the output voltage recovers smartly and reaches its desired state. After this, the inductor current takes several ac cycles to reach its steady-state, during which the output voltage shows little change. This is due to the presence of free-wheeling interval that decouples control of output voltage control from that of the input current. This is unlike the case of a boost-based PFC rectifier in which output voltage and inductor (input) current reach steady-state together.

The voltage dip can be reduced and the transient response can be made faster by increasing the stored energy in the capacitor C, or by increasing the stored energy in the inductor either by increasing D_f^* or by increasing L.

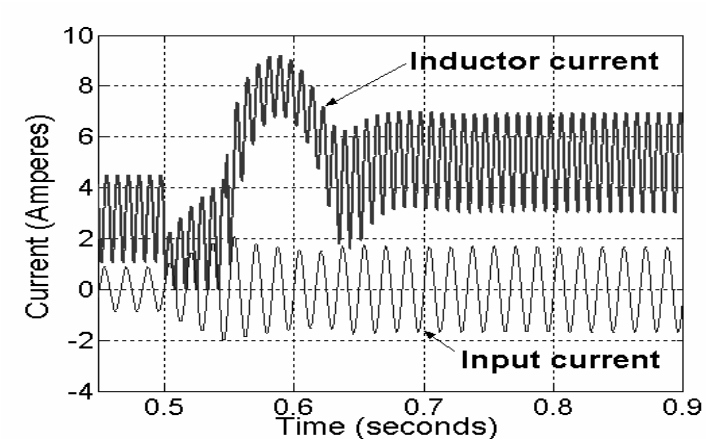


(a)

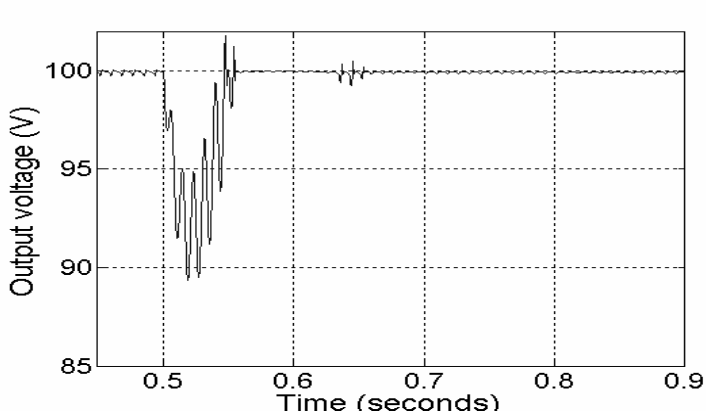


(b)

Fig. 8.13. Simulated step load transient response of the CBB PFC rectifier at V_s=85 V, V_o=100 V, I_o=0.5 A to 0.55 A, D_f^*=0.57. (a) Inductor and input current. (b) Output voltage.



(a)



(b)

Fig. 8.14. Simulated step load transient response of the CBB-PFC rectifier at V_s=85 V, V_o=100 V, I_o=0.5 A to 1 A, D_f^*=0.57. (a) Inductor and input current. (b) Output voltage.

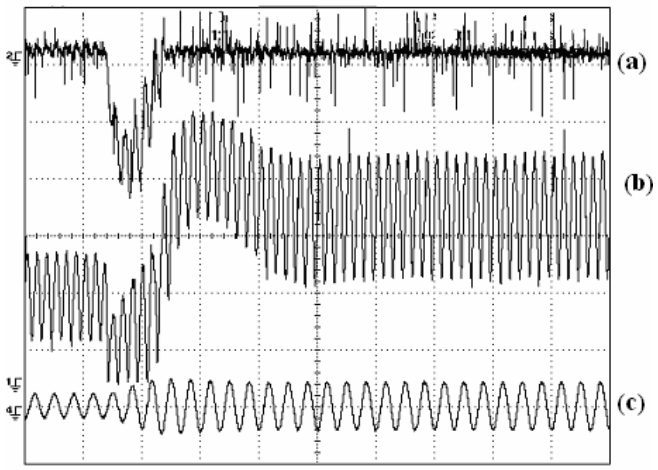


Fig. 8.15. Experimental response for step load change at V_s=85 V, V_o=100 V, I_o=0.5 A to 1 A, D_f^*=0.57; (a) Output voltage (scale: 5 V/div, oscilloscope in ac coupling mode with ground at 3.2 div) (b) Inductor current (ground at -2.5 div, scale: 2A/div) (c) Input current (scale: 5A/div; ground at -3 div) time scale: 50ms/div.

Fig. 8.16 shows the experimental steady-state efficiency of the converter and the total harmonic distortion (THD) of the input current at various line and load conditions. It may be noticed that the THD of input current at light loads is higher than that at high loads. This is due to the choice of D_f^* (refer section 8.3.3(D)). Setting of D_f^* to a constant value in the DMC scheme results in the magnitude of inductor current I_k being reduced under light loads. Due to this, the operating efficiency of the converter is high even under partial loaded conditions. To explain this, the relationship between inductor current I_k ad D_f^* has to be known. The exact relationship between D_f^* with I_k is complex and is given by

$$\frac{1}{\pi}\int_0^{\pi}\left(\frac{\left|I_m \sin(wt)\right| + V_o/R}{\sqrt{I_k{}^2 - \frac{V_m I_m}{2L\omega} Sin(2\omega t)}}\right) d(\omega t) = 1 - D_f{}^* \tag{8.26}$$

For simplicity, if we assume a large inductance, the second term inside the square root in the denominator can be neglected. (However, it must be noted that in practice, the inductor ripple current is significant).

$$\frac{1}{\pi}\int_0^{\pi}\left(\frac{\left|I_m \sin(wt)\right| + V_o/R}{I_k}\right) d(\omega t) = 1 - D_f{}^* \tag{8.27}$$

Solving this, the approximate relation between I_k and D_f^* can be obtained as

$$I_k = \frac{\frac{2I_m}{\pi} + V_o/R}{(1 - D_f{}^*)} \tag{8.28}$$

Thus, with D_f^* held constant, and with a reduction in load, the current I_k is also brought down. Although the above expression neglects the inductor ripple current, it basically gives an indication that the inductor current indeed decreases with a

reduction in load at a constant D_f^*. This explains the high operating efficiency obtained under partial and light load conditions (Fig. 8.16).

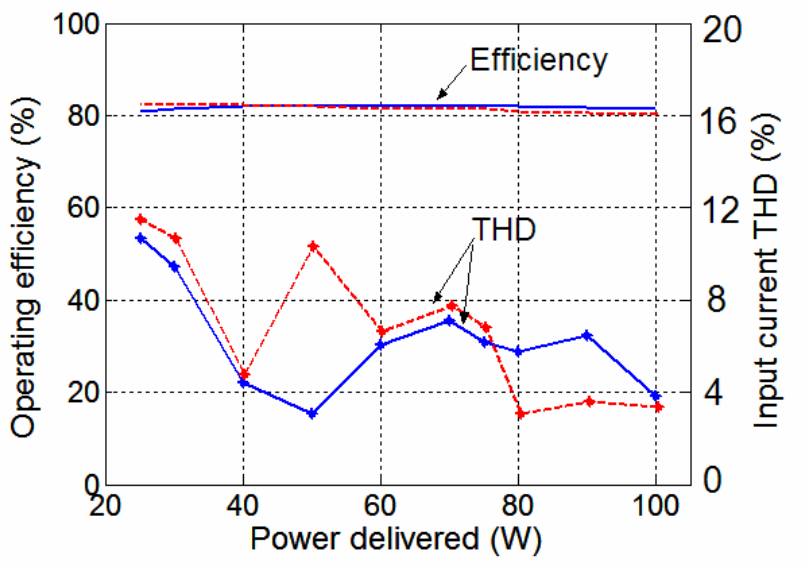


Fig. 8.16 Experimental variation of steady-state efficiency and input current THD (multiplied by 5) with delivered power at extreme line conditions; legends: dotted line -V_s=110 V, solid line – V_s=85 V.

8.3.5 Comparison of CBB-PFC with Popular PFC Rectifiers

In this sub-section, the proposed DMC based CBB-PFC rectifier is qualitatively compared with popular stand-alone boost PFC and cascaded boost-buck PFC converters.

A. CBB-PFC Versus Stand-Alone Boost PFC Rectifier

One of the major advantages of the CBB converter over stand-alone boost-based PFC rectifier is that the output voltage can also be lower than the peak of the input voltage. Thus, the maximum device voltage stress in CBB converter is always lower than that in the boost PFC converter. In addition, the inrush current problem that occurs in the boost PFC at start-up can be avoided in the CBB converter. Besides, the

CBB converter has an additional degree of control freedom that is exploited in preventing the second harmonic energy from reaching the output terminals. The control freedom helps in decoupling the control of output voltage from that of the input current. This also reduces the output filter capacitance, which in the case of a boost-PFC is high, being designed to reduce the output voltage ripple.

On the down side, the CBB converter has an additional switch and an additional diode. The second harmonic energy is stored in the inductor, which results in a high input current crest factor and increased device current ratings. The energy storage in inductor is also likely to result in a lower operating efficiency when compared to the boost-PFC converter. It must be noted that although energy storage in inductor may be considered as a disadvantage of the CBB scheme, an inexpensive laminated core inductor which also has a longer life time when compared to electrolytic capacitors has been used.

B. CBB-PFC Versus Cascaded Boost-Buck PFC Rectifier

The cascaded boost-buck (CaBB) converter is the dual of the CBB converter. As a result, it also has the additional degree of control freedom that helps in decoupling the control of input current from that of the output voltage. The second harmonic energy in CaBB-PFC scheme is stored in the intermediate capacitor which is a more efficient way of energy storage when compared to the inductive energy storage in the CBB converter. However, since energy in CBB converter is processed only once in the inductor, whereas in the CaBB it is processed twice, direct comparison of their operating efficiency is difficult.

As the first stage in the CaBB converter is a boost-stage, the device voltage stress in the scheme is much higher than the corresponding stress in the CBB

converter. In addition, although power loss due to reverse recovery of diodes occurs in both converters, the loss will be relatively lower in the case of CBB converter due to the low voltages involved. An advantage of having a boost front-end stage (in CaBB converter) is the low crest factor of input current. However, the boost-stage cannot limit the inrush current upon start-up which, can be avoided in the CBB converter.

In the CaBB converter, the output voltage is absolutely free from the second harmonic ripple, whereas in the DMC-based CBB converter, it is dependent on the control setting D_f^*, the higher the setting, the lower is the ripple. As mentioned earlier, the setting of D_f^* also affects the operating efficiency and device current ratings.

The output voltage dynamics of CaBB converter is generally good due to high energy storage in the intermediate capacitor. Similar dynamics can be obtained in the CBB converter by increasing the energy storage either in the inductor (by increasing D_f^* or L or both), or in the output capacitor C. However, increasing L/C will increase the size and cost of the converter.

In addition to the line-side LC-filter, the CaBB converter has four energy elements (two inductors and two capacitors), whereas the CBB converter employs only one inductor and one capacitor. As the buck converter acts like a constant power load presenting a negative load resistance characteristics on the boost stage in the CaBB PFC rectifier [74], the controller design for the boost stage is dependent not only on the line side performance but also on the load-side characteristics. Being a single-stage converter, it is believed that the CBB converter does not face this problem.

It needs to be mentioned that, although the DMC-based CBB-PFC rectifier offers several advantages over CaBB PFC rectifier, it is not clear if these advantages make it really superior over the cascaded scheme. Further explorations are needed to clarify this aspect.

C. Dual-Mode Versus Other Control Techniques of CBB-PFC

The CBB-PFC has two switches and hence there are two degrees of control freedom. A chosen control technique can employ one of the following two control approaches.

1. The control technique exploits the control freedom in achieving tight output voltage regulation and shaping the input current to sinusoid
2. The control technique does not exploit the control freedom offered by the converter. The prime control need is to shape the input current to a sinusoid. The output voltage is roughly regulated with a large second harmonic ripple.

Depending upon the nature of control, the filter components of the converter will be different. When approach 1 is employed, as in the present DMC based scheme, second harmonic power drawn from the input is absorbed in the inductor thereby increasing its size.

Converters employing control methods following approach 2 are similar to boost pre-regulators. However, unlike boost pre-regulators, the output voltage can be either lower or higher than the peak input voltage. The size of inductor will be small in this case, although a bulky filter capacitor will be needed in order to reduce the output voltage ripple (on account of second harmonic power reaching the output terminals). The lower the output voltage, the larger will be the capacitor needed. A down-stream converter may be needed if load regulation demands are stringent.

Typically, the voltage loop bandwidth of the pre-regulator is lower than the frequency of the mains resulting in poor dynamic response. This is because, increasing the bandwidth of the voltage loop will introduce distortions in the input current reference and hence, in the actual input current. References [47] and [50] employ control schemes that come under this category. Reference [92] employs a similar scheme to control an interleaved buck-boost converter.

Control methods employed in [48] and [49] fall under approach 1, in which second harmonic energy drawn from the mains is stored in the inductor. Reference [49] uses a control method that exploits the control freedom offered by a two-switch buck-boost converter, a converter much similar to cascade buck-boost converter. However, the paper does not present results discussing the dynamic performance of the control/converter scheme. Besides, the output voltage is controlled indirectly by shaping the inductor current. The circuit parasitics, which have not been taken into account in shaping the inductor current, will result in second harmonic ripple appearing in the output voltage.

Reference [48] employs sliding-mode-based control to shape the input current and regulate the output voltage. The performance goals of this scheme are the same as those of the proposed DMC scheme. The control scheme was designed and simulated for the specifications given in Sec.8.3.3. A brief discussion and evaluation of the control method is given below.

Fig. 8.17 shows the overview of the scheme. This diagram is drawn based on the understanding of the control scheme presented in [48]. Similar to the DMC scheme, here also there are three loops, viz., input current shaping loop, output voltage regulation loop and inductor current loop.

1. Input current shaping loop

The input current is shaped by controlling S_1. The equivalent control is given by

$$u_{1eq} = \frac{KV_{rect}}{i_L}. \tag{8.29}$$

Here i_L is the instantaneous inductor current and V_{rect} is the rectified input voltage. The numerator term represents the input current. The parameter K decides the input-output power balance. The above expression is similar to (8.15) that relates D_b to input current and inductor current.

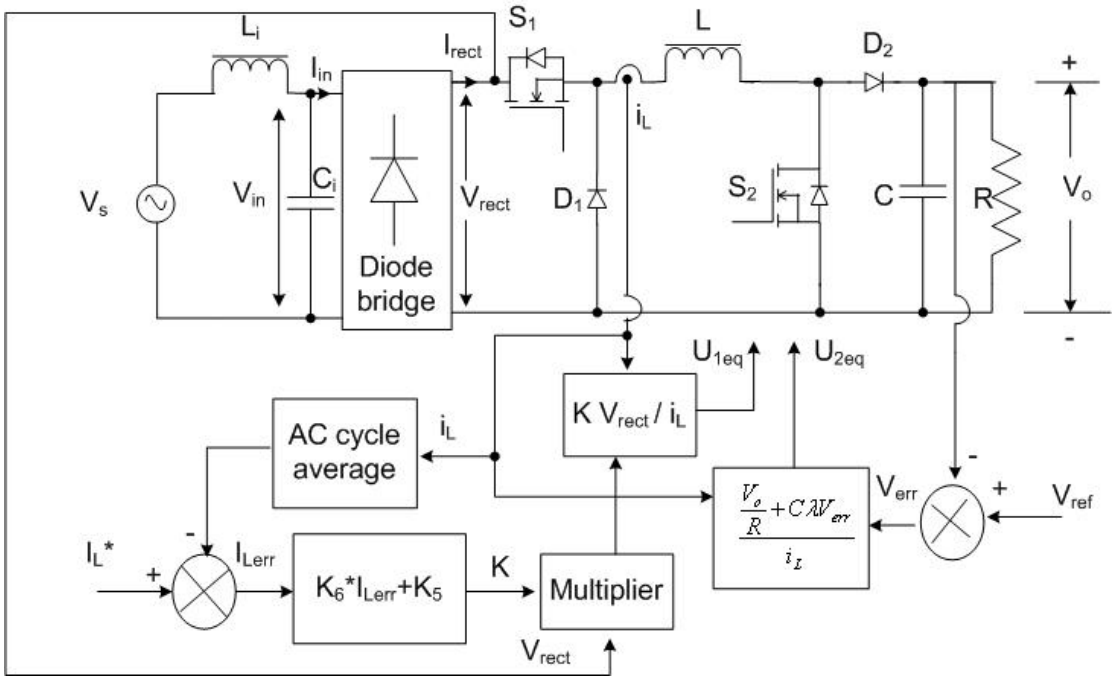


Fig. 8.17 Block schematic diagram of sliding-mode control scheme for CBB-PFC – based on the method in [48]

2. Output voltage regulation loop

The output voltage is regulated by controlling S_2. The equivalent sliding control is given by

$$u_{2eq} = \frac{\frac{V_o}{R} + C\lambda(V_{ref} - V_o)}{i_L}. \qquad (8.30)$$

Here λ is chosen by the designer. Under steady-state, the above expression is similar to (8.16) that relates D_o, output current and inductor current.

3. Inductor current loop

This is the slow loop similar to the D_f-error loop in the DMC scheme. The inductor current error decides the parameter K which in turn ensures power balance. The parameters K_5 and K_6 in Fig. 8.17 are dependent on the load resistance and reference voltage. Details can be obtained from [48].

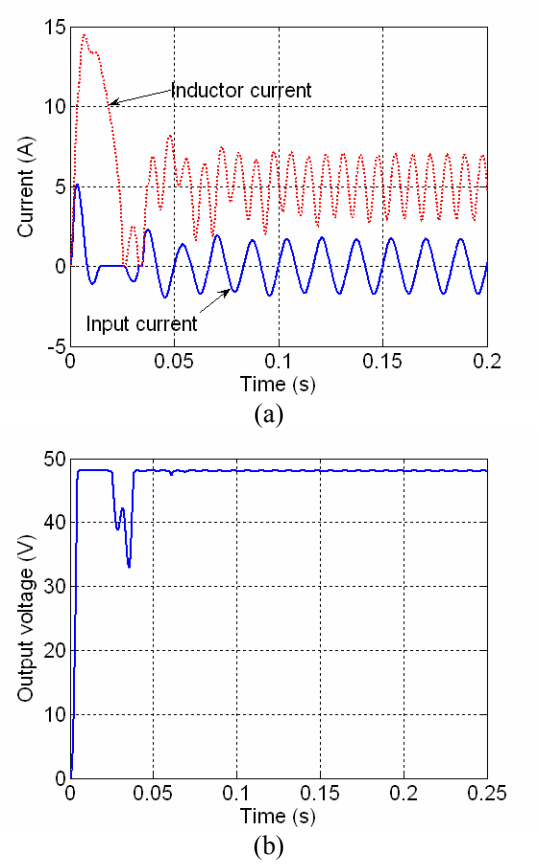


Fig. 8.18 Simulation results demonstrating the performance of control scheme employed in [48] at V_s = 85 V, V_{ref} = 48 V and P_o = 100 W (a) Inductor and input current (b) output voltage.

Excellent steady-state and transient state behavior are obtained when the reference voltage is set low. Fig. 8.18 demonstrates the excellent start-up transient offered by the converter when the reference voltage is set to 48 V and load power is set to 100 W. However, the scheme was found to have the following two drawbacks.

1. Irrespective of the load conditions, the inductor current reference used in the control scheme is the same. Thus, under light load conditions, the converter's efficiency will be low. Unlike the scheme in [48], in the proposed DMC scheme, the inductor current goes down when the load becomes low (8.28) thereby boosting the operating efficiency.
2. In the sliding-mode control scheme, the switch S_1 is used to control the input current and S_2 is used to control the output voltage. These switches are controlled independently. When the output voltage reference is moderately high (for example, 85V DC with a 85 V RMS AC input), the converter operates like a buck rectifier (S_2 switched off) during start-up and the desired output voltage would never be realized. This problem is demonstrated in Fig. 8.19, when the converter input voltage is set at 85V (RMS) and the output voltage reference is set at 100V DC. The operation of the converter in the buck mode and the control scheme's inability to boost the output voltage beyond 80 V are clearly seen. In the proposed DMC scheme, the intervals of the converter are controlled (instead of the individual switches) with the boost interval being the master interval. Thus, such a start-up problem does not arise.

Thus, it may be concluded the proposed DMC scheme for the CBB-PFC is superior to the other control techniques currently available in the literature.

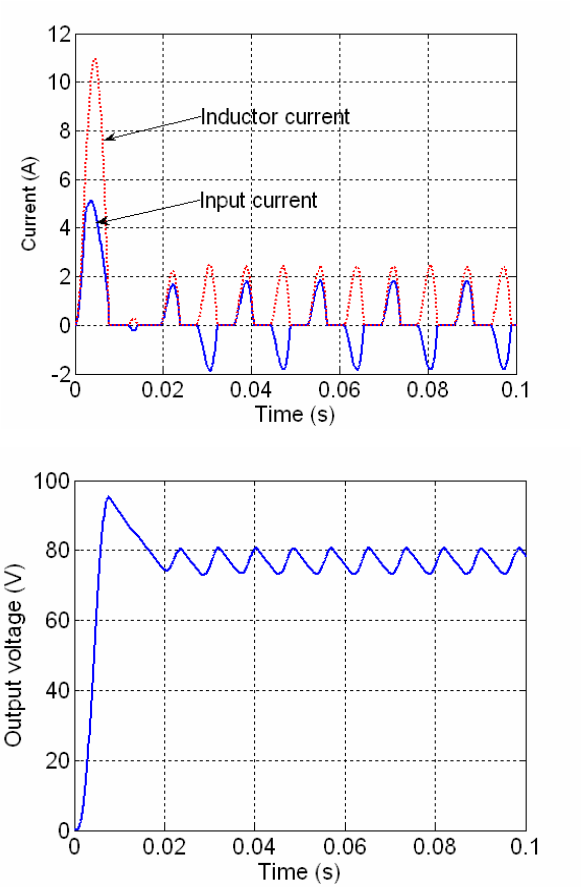


Fig. 8.19 Simulation results demonstrating the drawback of sliding-mode control scheme employed in [48] (a) Inductor and input current (b) output voltage.

8.4 Chapter Conclusions

In this chapter, the application of tri-state converters in single-phase ac-dc PFC rectifiers has been investigated. It has been shown that the tri-state boost PFC converter may not offer significant advantage over the classical boost-PFC. On the other hand, in tri-state versions of buck-boost-derived converters, it is possible to decouple the controls of input current and output voltage. This also results in meeting the multiple-objectives of a PFC rectifier. To demonstrate this multiple-goal-achievement, a cascade-buck-boost PFC converter has been designed, built, and tested. A simple dual-mode control scheme has been proposed for a PFC unit based on CBB converter that exploits the control freedom offered by the converter to achieve

sinusoidal input current and tight output voltage regulation. The control of output voltage and input current are de-coupled thereby resulting in good dynamic response. The limits and trade-offs in the control scheme have been explained. Simulation and experimental results that demonstrate the steady-state and transient performance of the converter with the proposed control scheme have been presented. A qualitative comparison of the proposed PFC scheme with other popular single-phase PFC schemes has been given.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

9.0 Background

Classical single-switch boost and buck-boost power converters and their derivatives are used in dc-dc switch-mode power converters and in ac-dc power factor correction applications. In both the applications, the dynamic performance of the above-mentioned converters for disturbances is generally slow.

In dc-dc applications, although dynamic response problem is encountered in these converters for both small and large disturbances, the reason behind the slow dynamic response is different in either case. For small disturbances, the dynamic response is slow on account of the presence of a characteristic RHP zero in the small-signal control-to-output transfer function of the converter. As the RHP zero also changes its location in the complex frequency plane with changes in operating point, the closed-loop bandwidth is typically limited to frequencies much less than the switching frequency. For large disturbances, an important reason for the sluggish dynamic response is related to the characteristics of linear controllers that are often optimized for small-signal performance at one operating point.

In single-phase ac-dc PFC applications, the absence of an additional degree of control freedom in single-switch boost and buck-boost rectifiers and the prime objective to shape the input current to a sinusoid forces a compromise in the dynamic response offered by the converter. Typically, a closed loop bandwidth much less than the ac line frequency (50/60 Hz) is realized.

In this thesis, several solutions to dynamic response problem in boost and buck-boost-derived converters have been proposed. The solutions fall under the following two categories.

- Mitigation of dynamic response problems by enhancements in converter design and control techniques
- Modification of the existing converter topology to overcome the problem.

9.1 Mitigation of RHP Zero Problem by Refining the Design Approach

Chapter 3 discussed this approach. The aim of this approach was to mitigate the small-signal dynamic response problem due to RHP zero in the classical boost dc-dc converter by appropriate selection of the boost inductance. Through a theoretical analysis it has been proved that even when operating in CCM, the RHP zero in the control transfer function can be shifted farther in the complex frequency plane provided the inductance is below a certain value. However, the resulting inductance is small which will eventually result in an undesirable large ripple current. The analysis has also been extended to explain the well-known fast dynamic response characteristics of the converter when operated in discontinuous conduction mode.

9.2 Dynamic Performance Improvement by Modifications in the Employed Controller

This approach was discussed in Chapters 3 and 4. The aim of this approach was to improve the dynamic performance of the classical boost converter (in dc-dc

applications) by modifications in the controllers employed. The controllers considered for dynamic performance improvement are listed below.

- Locally-optimized Linear-PI controller
- Gain-scheduled-PI (GSPI) controller and
- Fuzzy logic controller (FLC)

It has been observed that linear-PI controller designed at an operating point offers the nearly best transient response possible at the operating point in the case of boost and buck-boost converters. However, it must be noted that the response is still slow as the closed-loop bandwidth is limited by the presence of RHP zero in the control-to-output transfer function of the converter.

GSPI and FLC controllers, in spite of implementation complexities, do not offer much advantage in terms of small-signal transient response over the locally-optimized PI controller. However, for large-signal transients, as pointed out by many researchers, FLC is better than linear-PI controllers. Simulation and experimental results on a 50 W prototype dc-dc boost power converter have been presented to demonstrate the dynamic performances offered by GSPI and FLC.

9.3 Non-linear function controller

An in-depth analysis has been carried out on FLCs used in power converter control applications. It has been shown that the rule table of two-input FLCs of the type typically used in the control of power electronic converters can be replaced by a single-input-single-output non-linearity and the entire FLC can be realized using a fast and inexpensive non-linear analog circuitry. The reduced controller form has been named as Non-linear Function Controller (NLFC). Simulation results showing the

near equivalence of NLFC and multi-input FLC have been presented. A Non-Linear PI Controller (NPIC) (reduced form of PI-FLC) has been developed for a classical boost converter. Although a boost converter has been taken for example, it must be noted that the proposed NLFC/NPIC is relevant to all power converters, in general. The structural similarity of NPIC to linear-PI controller has been used to design an NPIC that offers good small-signal dynamic performance (at an operating point). An example design has been given. Experimental results demonstrating a similar small-signal dynamic performance and an improved large-signal dynamic performance of the converter with NPIC over that obtained with a linear-PI controller have been presented.

It must be noted that although NPIC offers better large-signal response when compared to that offered by PI-controller and good small-signal performance similar to the PI-controller at the design operating point, the NPIC (and hence the original PI-FLC) may not offer good small-signal performance when the operating point changes.

The simplification of two-input FLC to SISO-non-linearity has been advantageously used in predicting the stability margins of the system consisting of the classical dc-dc boost converter and NPIC controller. Describing function analysis has been used for the purpose. The predicted stability limits have been verified using simulation and experimental results.

9.4 Dynamic Performance Improvement by Modifications in the Converter Topology

Although locally-optimized PI controllers offered a better small-signal transient response than the other controllers explored in Chapters 3 and 4, due to reduced

small-signal bandwidth on account of the presence of RHP zero, the transient response was still slow. Unless the RHP zero is avoided or pushed farther in the right-half of the complex-s-plane, an improvement in closed-loop bandwidth was difficult.

Tri-State Class of Converters

To achieve a significant improvement in the dynamic response in boost and buck-boost-derived converters (in dc-dc applications), Chapter 5 explored the other alternative of making modifications in the converter topology itself. An additional degree-of-control-freedom in the form of an 'inductor free-wheeling interval' has been introduced in these converters. The family of converters obtained so has been named as 'tri-state' family of converters. A list of classical boost and buck-boost-derived converters and their tri-state versions has been given.

At the cost of an additional diode or an additional switch or both, the tri-state converters are able to avoid the RHP zero in their control-to-output transfer function. This has resulted in a significant improvement in the dynamic performance of these converters over their classical counterpart. Hardware prototypes of tri-state boost and tri-state flyback converters have been designed, built, and tested. Using a simple 'constant-D_o' control scheme, simulation and experimental results demonstrating the absence of RHP zero and improvement in dynamic performance have been presented. The performance of tri-state boost and tri-state flyback converters has also been compared with those offered by their corresponding classical counterparts. The results clearly indicate the significant improvement in dynamic performance.

Dual-Mode Control Scheme for Tri-State Boost Converter

Although the dynamic performance of the converter with the 'constant-D_o' control scheme discussed in Chapter 5 is good, under high line and load conditions,

the inductor current is excessively high. This results in a reduction in the steady-state operating efficiency of the converter. To optimize the inductor current and thereby improve the efficiency of the converter without much compromise in the dynamic operating range of the converter, two variations of a multivariable dual-mode control (DMC) scheme, namely, direct dual-mode control scheme (DDMC) and indirect dual-mode control (IDMC) scheme have been proposed in Chapter 6. These schemes vary both the 'boost' ($D_b\,T$) and 'capacitor-charging' ($D_o\,T$) intervals to achieve fast output voltage dynamics and relatively slow inductor current optimization. An improvement in efficiency of the converter by about 10% (at full load) over that obtained when using 'constant-D_o' control scheme has been achieved. Experimental results showing an identical small-signal dynamic response of the tri-state boost converter under the various control schemes has also been presented.

Design of Tri-State Boost Converter

The presence of 'free-wheeling' interval in tri-state converter acts as an energy reservoir. This reservoir not only helps in achieving excellent small-signal dynamic operation, but also enables obtaining good large-signal dynamic response for external disturbances of limited magnitude. The length of the free-wheeling interval also decides the size and rating of power components. The relationship between length of the free-wheeling interval and margins offered by the converter for various disturbances within which fast dynamic response of the converter's output voltage is preserved has been presented in Chapter 7. A systematic design procedure for calculating the power and control components of the converter (under DDMC and IDMC schemes) and for getting the pre-defined margins of disturbance has also been given. The dynamic performance of the converter for disturbances whose magnitudes

fall within and outside the defined disturbance margins have been studied through simulation and experimental results.

9.5 Investigation of Tri-state Converters for Performance Improvement in Single-Phase AC-DC PFC Applications

The presence of additional degree of control freedom in tri-state converters make them potential candidates for application in single phase PFC rectifiers, where there is a need to achieve multiple goals namely drawing a sinusoidal input current at unity power factor from the ac mains, delivering a well-regulated output voltage, and offering fast dynamic response for step disturbances. Accordingly, the application of tri-state boost and tri-state buck-boost-derived ac-dc converters in single phase PFC has been investigated in C**hapter 8**. It has been shown that while the tri-state boost PFC rectifier does not offer much advantage over the classical boost-PFC rectifier, the tri-state buck-boost PFC converter and its derivatives are capable of meeting the multiple-PFC objectives. A cascade buck-boost converter, which is a derivative of buck-boost converter, has been taken for detailed investigation in PFC applications. A novel dual-mode control method that aims at achieving the multiple goals in the CBB-PFC has been proposed. The operation of the converter-control scheme has been analyzed in detail. The multiple-goal achievement in PFC has been demonstrated through simulation and experimental results. It has been demonstrated that the converter also offers excellent output voltage dynamic response for step loads below a certain magnitude.

As the second harmonic energy from ac-line is stored in the inductor in the CBB-PFC, a design procedure to select the inductor and other power circuit

components has been given. The associated design trade-offs have been described. The CBB-PFC has been qualitatively compared with single-phase stand-alone boost PFC and cascaded boost-buck converter. It must be noted that although the CBB-PFC offers many advantages over cascaded boost-buck-PFC, it is not clear if these advantages make them really superior to cascaded boost-buck PFC. Further work related to establish the converter as a useful solution for PFC problem is left for future explorations.

9.6 Future work

Some ideas that can be considered in future for implementation are as below.

1. The DMC schemes for tri-state boost converters make the optimization of inductor current at least one order slower than the control of output voltage i.e., control input D_o is made one order slower than control input D_b. Investigations on the best possible rates of change of D_b and D_o that achieve the desired steady-state in the shortest possible time without affecting stability are left for future investigation. The implication of such an optimum change in control inputs on the size and ratings of power components is also left for future investigation.
2. Due to non-availability of a proper model, the controllers of CBB-PFC have been designed based on computer simulations. Development of a model of the converter that will help designers in deciding the controller is a major task that is left for future explorations. Besides, as mentioned in before, detailed investigation and comparison of CBB-PFC with cascaded boost-buck converter with respect to cost, size, and performance is also left for future exploration. These investigations will establish the usefulness of CBB-PFC rectifier.

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1. K.Viswanathan, R. Oruganti, and D.Srinivasan, "Dual-mode control of cascade buck-boost PFC converter," Being revised as per the changes suggested by *IEEE Transaction on Industrial Electronics*.

APPENDIX A

TRI-STATE BOOST CONVERTER: DERIVATION OF COMPLETE SMALL-SIGNAL TRANSFER FUNCTION MODEL

A.0 Background

Chapter 5-7 discuss the tri-state boost converter. The small-signal control-inputs-to-converter-state transfer function of the converter has been used in several places. In this section of the thesis, the complete derivation for the control-input-to-converter-state transfer function taking into account the effect of system parasitics is presented.

A.1 Complete Transfer Function- Derivation

Let us consider the tri-state boost converter (Fig. 5.2(b)). Let us consider the following parasitics in the converter.

R_M = MOSFET ON-Resistance,

R_L = Inductor ESR,

R_c = Capacitor ESR,

V_D = Diode Forward voltage drop.

Let I_L be the average inductor current, V_o be the average output voltage, V be the average voltage across the capacitor, and R be the load resistance. The state equations of the converter can be written as below.

$D_f T$ interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{(R_M + R_L)}{L} & 0 \\ 0 & -\frac{a}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v \end{pmatrix} - \begin{pmatrix} \frac{V_D}{L} \\ 0 \end{pmatrix} \tag{A1}$$

where $a = \frac{R}{R + R_c}$.

$D_b T$ interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{(2R_M + R_L)}{L} & 0 \\ 0 & -\frac{a}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_s \tag{A2}$$

$D_o T$ interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{(aR_C + R_L)}{L} & -\frac{a}{L} \\ \frac{1}{C} - \frac{aR_C}{RC} & -\frac{a}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_s - \begin{pmatrix} \frac{V_D}{L} \\ 0 \end{pmatrix} \tag{A3}$$

The average equation of the converter can be written as below.

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{\left[aR_C D_o + R_L + R_M (1 + D_b - D_o)\right]}{L} & -\frac{a}{L} D_o \\ \left(\frac{1}{C} - \frac{aR_C}{RC}\right) D_o & -\frac{a}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v \end{pmatrix} + \begin{pmatrix} \frac{1}{L}(D_b + D_o) \\ 0 \end{pmatrix} V_s - \begin{pmatrix} \frac{V_D}{L}\left(D_f + D_o\right) \\ 0 \end{pmatrix} \tag{A4}$$

For obtaining the small-signal model, perturbations are introduced in the control inputs D_b and D_o (only one control input is perturbed at a time). As a result, the dynamic variables I_L and V change. Let the perturbed variables be

$$\begin{aligned} v &= V + \hat{v}; \qquad i_L = I_L + \hat{I}_L \\ d_b &= D_b + \hat{D}_b \\ d_o &= D_o + \hat{D}_o \end{aligned} \tag{A5}$$

In the sections to follow, the transfer function between the converter states and each of the control input (the other control input is kept constant) is derived and the transfer-function matrix (6.17) is derived.

A.2 Derivation of D_b-to-State Transfer Functions

In this case, the control input D_o is held constant. **This is similar to the case of transfer functions derived in the case of the 'constant-D_o' control scheme** discussed in chapter 5. Applying the perturbed variables (A5) [other than D_o] to (A4) we get

$$\begin{aligned} \frac{d\left(I_L + \hat{I}_L\right)}{dt} &= -\frac{\left[aR_C D_o + R_L + R_M(1 + D_b + \hat{D}_b - D_o)\right]}{L}\left(I_L + \hat{I}_L\right) \\ &\quad - \frac{a}{L} D_o\left(V + \hat{V}\right) + \frac{1}{L}(D_b + \hat{D}_b + D_o)V_s - \frac{V_D}{L}\left(1 - D_b - \hat{D}_b\right); \\ \frac{d\left(V + \hat{V}\right)}{dt} &= \left(\frac{1}{C} - \frac{aR_C}{RC}\right) D_o\left(I_L + \hat{I}_L\right) - \frac{a}{RC}\left(V + \hat{V}\right) \end{aligned} \tag{A6}$$

The small-signal model can be obtained by removing the dc terms and neglecting the non-linear terms in the above set of equations.

$$\begin{aligned} \frac{d\hat{I}_L}{dt} &= -\frac{\left[aR_C D_o + R_L + R_M(1 + D_b - D_o)\right]}{L}\hat{I}_L - \frac{a}{L} D_o \hat{V} + \frac{V_s + V_D - R_M I_L}{L}\hat{D}_b; \\ \frac{d\hat{V}}{dt} &= \left(\frac{1}{C} - \frac{aR_C}{RC}\right) D_o \hat{I}_L - \frac{a}{RC}\hat{V} \end{aligned} \tag{A7}$$

Taking laplace transforms

$$\begin{aligned} sI_L(s) &= -\frac{\left[aR_C D_o + R_L + R_M(1 + D_b - D_o)\right]}{L} I_L(s) - \frac{a}{L} D_o V(s) + \frac{V_s + V_D - R_M I_L}{L} D_b(s); \\ sV(s) &= \left(\frac{1}{C} - \frac{aR_C}{RC}\right) D_o I_L(s) - \frac{a}{RC} V(s) \end{aligned} \tag{A8}$$

Eliminating *V(s)* form the above set of equations, the D_b-to-I_L transfer function ($G_{21}'(s)$) can be computed as

$$G_{21}'(s) = \frac{I_L(s)}{D_b(s)} = \frac{1}{JLCR} \frac{\left(V_s + V_D - R_M I_L\right)\left(a + sR_cC\right)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1} \tag{A9}$$

Similarly, eliminating $I_L(s)$ from (A7), the D_b-to-V transfer function can be computed as

$$\frac{V(s)}{D_b(s)} = \frac{D_o a}{JLC} \frac{\left(V_s + V_D - R_M I_L\right)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1} \tag{A10}$$

where

$$J = \frac{1}{RLC}\left(aR_L + aR_M\left[1 - D_o + D_b\right] + a^2 R_c D_o + a^2 D_o^2 R\right) \tag{A11}$$

$$P = \frac{1}{RLC}\left(aL + R_L RC + RCR_M\left[1 - D_o + D_b\right] + aR_c D_o RC\right) \tag{A12}$$

$$I_L = \frac{V_s\left(D_b + D_o\right) - V_D\left(D_f + D_o\right)}{R_L + 2D_b R_M + R_M D_f + aR_c D_o + aRD_o^2} \tag{A13}$$

The relation between the output voltage V_o and capacitor voltage V can be shown to be

$$v_o = av + i_L aR_C D_o \tag{A14}$$

Substituting the perturbed variables in (A14),

$$V_o + \hat{V}_o = a\left(V + \hat{V}\right) + \left(I_L + \hat{I}_L\right)aR_C D_o \tag{A15}$$

Neglecting the dc terms in (A15) and taking the Laplace transforms, we get

$$\begin{aligned} &V_o(s) = aV(s) + aR_C D_o I_L(s) \\ &\Rightarrow V_o(s) = aV(s) + aR_C D_o \frac{sRC + a}{R} V(s) \qquad [\text{from (A8)}] \end{aligned} \tag{A16}$$

Rearranging (A16) and substituting for '*a*,' we get

$$V_o(s) = V(s)\left(1 + s\mathrm{R_C C}\right) \tag{A17}$$

Thus, the overall D_b-to-V_o transfer function ($G_{11}'(s)$) can be written as

$$G_{11}'(s)=\frac{V_o(s)}{D_b(s)}=\frac{1}{JLC}\frac{\left(V_s+V_D-R_M I_L\right)\left(1+sR_cC\right)}{\frac{1}{J}s^2+\frac{P}{J}s+1} \tag{A18}$$

A.3 Derivation of D_o-to-State Transfer Functions

In this case, the control input D_b is held constant. Applying the perturbed variables (A5) [other than D_b] to (A4) we get

$$\begin{aligned}\frac{d\left(I_L+\hat{I}_L\right)}{dt}&=-\frac{\left[aR_C\left(D_o+\hat{D}_o\right)+R_L+R_M\left(1+D_b-\hat{D}_o-D_o\right)\right]}{L}\left(I_L+\hat{I}_L\right)\\&\quad-\frac{a}{L}\left(D_o+\hat{D}_o\right)\left(V+\hat{V}\right)+\frac{1}{L}\left(D_b+\hat{D}_o+D_o\right)V_s-\frac{V_D}{L}\left(1-D_b\right);\\\frac{d\left(V+\hat{V}\right)}{dt}&=\left(\frac{1}{C}-\frac{aR_C}{RC}\right)\left(D_o+\hat{D}_o\right)\left(I_L+\hat{I}_L\right)-\frac{a}{RC}\left(V+\hat{V}\right)\end{aligned} \tag{A19}$$

The small-signal model obtained by removing the dc terms and neglecting the non-linear terms is given by

$$\begin{aligned}\frac{d\hat{I}_L}{dt}&=\frac{\left[-aR_C I_L+R_M I_L-aV+V_s\right]}{L}\hat{D}_o-\frac{\left[aR_C D_o+R_L+R_M\left(1+D_b-D_o\right)\right]}{L}\hat{I}_L-\frac{a}{L}D_o\hat{V};\\\frac{d\hat{V}}{dt}&=\left(\frac{1}{C}-\frac{aR_C}{RC}\right)\left(D_o\hat{I}_L+I_L\hat{D}_o\right)-\frac{a}{RC}\hat{V}\end{aligned} \tag{A20}$$

Taking laplace transforms

$$\begin{aligned}sI_L(s)&=\frac{\left[-aR_C I_L+R_M I_L-aV+V_s\right]}{L}D_o(s)-\frac{\left[aR_C D_o+R_L+R_M\left(1+D_b-D_o\right)\right]}{L}I_L(s)-\frac{a}{L}D_o V(s);\\sV(s)&=\left(\frac{1}{C}-\frac{aR_C}{RC}\right)\left(D_o I_L(s)+I_L D_o(s)\right)-\frac{a}{RC}V(s)\end{aligned} \tag{A21}$$

Eliminating *V(s)* form the above set of equations, the D_o-to-I_L transfer function ($G_{22}'(s)$) can be computed as

$$G_{22}'(s)=\frac{I_L(s)}{D_o(s)}=\frac{1}{JLCR}\frac{sRC\left(V_s+I_L\left[R_M-a(R_c+RD_o)\right]\right)+aV_s+aI_L\left[R_M-a(R_c+2RD_o)\right]}{\frac{1}{J}s^2+\frac{P}{J}s+1} \tag{A22}$$

Similarly, eliminating $I_L(s)$ from (A7), the D_b-to-V transfer function can be computed as

$$\frac{V(s)}{D_b(s)} = \frac{a}{JLC}\frac{\left(sI_L L + R_L I_L + R_M I_L(1+D_b) + V_s D_o - aRD_o^2 I_L\right)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1} \tag{A23}$$

The relation between the output voltage V_o and capacitor voltage V is

$$v_o = av + i_L aR_C D_o \tag{A24}$$

Substituting the perturbed variables (A11) in (A24),

$$V_o + \hat{V}_o = a\left(V + \hat{V}\right) + \left(I_L + \hat{I}_L\right)aR_C\left(D_o + \hat{D}_o\right) \tag{A25}$$

Neglecting the DC terms in (A12) and taking the laplace transforms, we get

$$\begin{aligned} &\hat{V}_o = a\hat{V} + \hat{I}_L aR_C D_o + I_L aR_C \hat{D}_o \\ &V_o(s) = aV(s) + aR_C D_o I_L(s) + aR_C I_L D_o(s) \\ &\Rightarrow \frac{V_o(s)}{D_o(s)} = a\frac{V(s)}{D_o(s)} + aR_C D_o \frac{I_L(s)}{D_o(s)} + aR_C I_L \end{aligned} \tag{A26}$$

Using (A21), it can be shown that the above relation reduces to

$$\frac{V_o(s)}{D_o(s)} = \frac{V(s)}{D_o(s)}\left(1 + sR_C C\right) \tag{A27}$$

Thus, the overall D_o-to-V_o transfer function (G_{12}'(s)) can be written as

$$G_{12}'(s) = \frac{V_o(s)}{D_o(s)} = \frac{a}{JLCR}\frac{\left(sI_L L + R_L I_L + R_M I_L(1+D_b) + V_s D_o - aRD_o^2 I_L\right)(1+sR_c C)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1} \tag{A28}$$

It may be noticed that the above transfer function has an RHP zero. This again justifies the control input D_o not being grouped with the output voltage (chapter 6).

A.4 Control-to-State Transfer Functions in the Absence of Parasitics

In the absence of parasitics, the control-to-system state transfer functions ($G_{11}(s)$, $G_{12}(s)$, $G_{21}(s)$, $G_{22}(s)$) can be written from $G_{11}'(s)$, $G_{12}'(s)$, $G_{21}'(s)$, $G_{22}'(s)$ (A9),

(A18), (A22), and (A28) by making $R_L=0$, $R_M=0$, $R_C=0$, $V_D=0$, $a=1$, $J=\frac{D_o^2}{LC}$ and $P=\frac{1}{RC}$.They are as below.

$$G_{11}(s)=\frac{V_o(s)}{D_b(s)}=\frac{1}{D_o{}^2}\frac{V_s}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A29}$$

$$G_{12}(s)=\frac{V_o(s)}{D_o(s)}=\frac{1}{D_o{}^2}\frac{\left(sI_LL+V_sD_o-RD_o^2I_L\right)}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A30}$$

As $I_L=V/(RD_o)=V_s(D_b+D_o)/(RD_o^2)$(steady-state inductor current)

$$G_{12}(s)=\frac{V_o(s)}{D_o(s)}=\frac{V_sD_b}{D_o{}^2}\frac{\left(sL\frac{(D_b+D_o)}{RD_o^2}-1\right)}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A31}$$

$$G_{21}(s)=\frac{I_L(s)}{D_b(s)}=\frac{1}{D_o{}^2R}\frac{V_s}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A32}$$

$$G_{22}(s)=\frac{I_L(s)}{D_o(s)}=\frac{1}{D_o{}^2R}\frac{sRC\left(V_s-I_LRD_o\right)+V_s+I_L\left[-2RD_o\right)]}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A33}$$

once again, as $I_L=V/(RD_o)=V_s(D_b+D_o)/(RD_o^2)$,

$$G_{22}(s)=\frac{I_L(s)}{D_o(s)}=-\frac{V_s(2D_b+D_o)}{RD_o^3}\frac{\left(\frac{sCRD_b}{(2D_b+D_o)}+1\right)}{\frac{LC}{D_o{}^2}s^2+\frac{L}{RD_o{}^2}s+1} \tag{A34}$$

The above transfer functions $G_{11}(s)$, $G_{12}(s)$, $G_{21}(s)$, and $G_{22}(s)$ are the same as those obtained in chapter 6.

APPENDIX B

MATLAB-SIMULINK MODELS OF THE VARIOUS CONVERTER-CONTROLLER SCHEMES

B.0 Tri-State Boost Converter

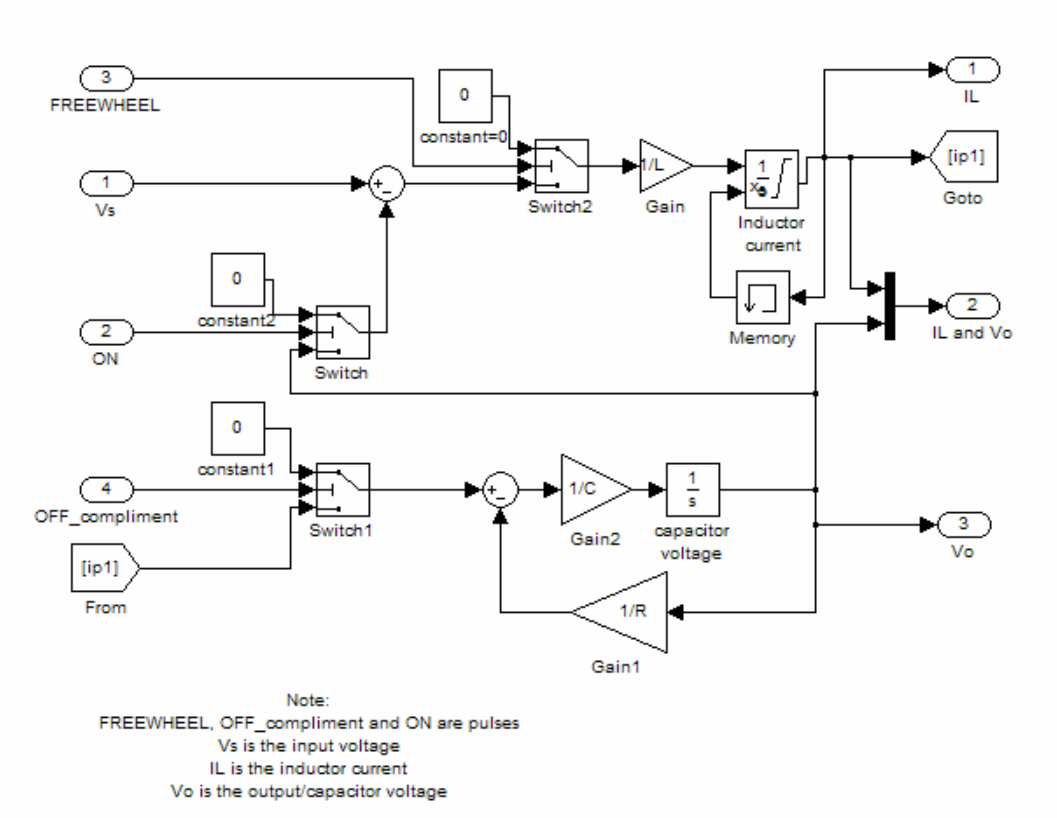


Fig. B.1. Tri-state boost converter- Simulation (SIMULINK) model

The parameters of the converter namely the filter inductance (*L=278 μH*), filter capacitance (*C= 540 μF*), and load resistance, *R* have to be stored in the matlab workspace before executing the model in Fig. B.1. Besides, as the inductor current is unidirectional in the tri-state boost converter, it is essential to limit the current to positive values. This has been achieved by having a non-linear limiter on the integrator 'inductor current.'

B.1 Switch Logic

The model in Fig. B.2 takes as input the D_b and D_o signals and derives the appropriate PWM signals driving the later stages.

Saturation1 (D_o limiter) limit- 0.1 to 1; Saturation (D_b limiter) limit- 0 to 0.9.

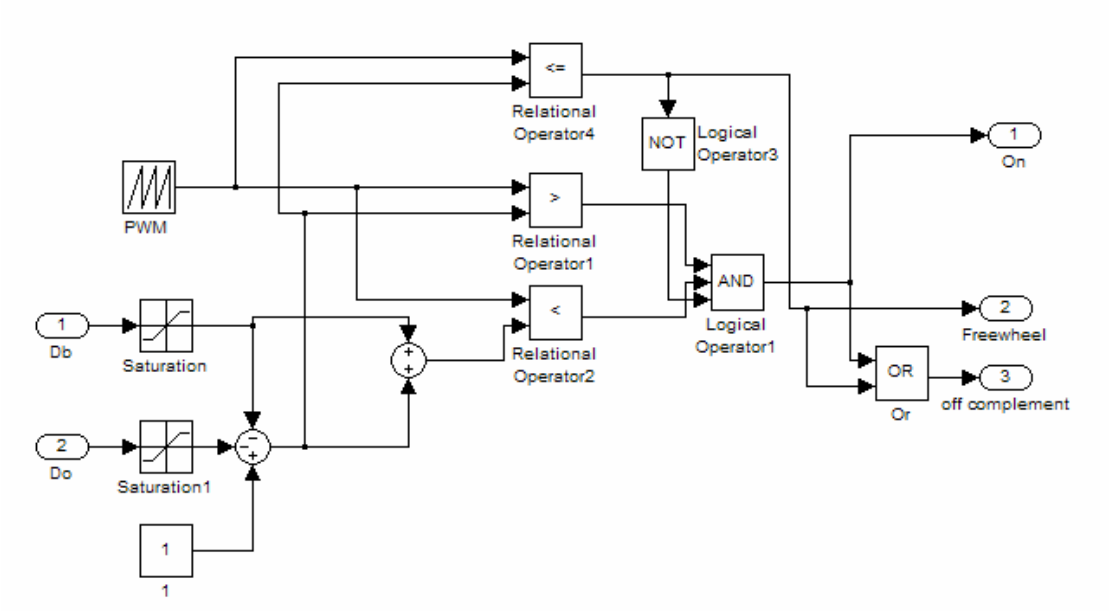


Fig. B.2. Switch logic- Simulink model.

B.2 Tri-State Boost Converter- 'Constant-D_o' Control Scheme

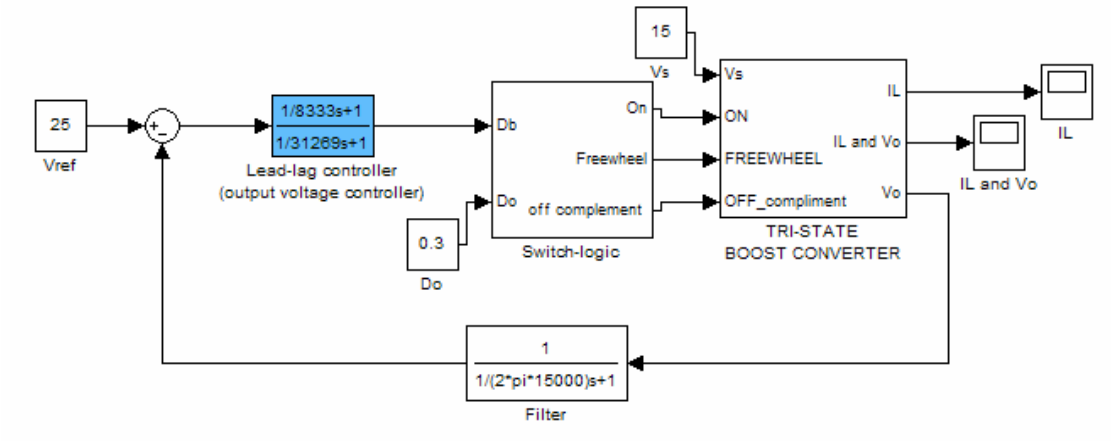


Fig. B.3. Tri-state boost converter- 'Constant-D_o' control scheme- Simulation (SIMULINK) model

B.3 Tri-State Boost Converter- Direct Dual-Model Control (DDMC) Scheme

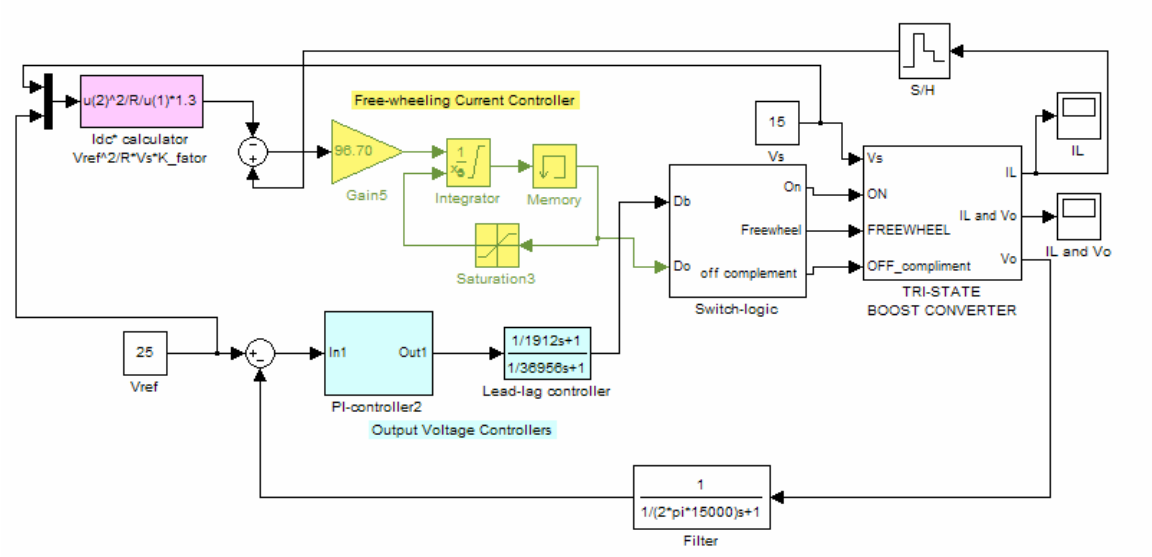


Fig. B.4. Tri-state boost converter- DDMC scheme- Simulation (SIMULINK) model

B.3.1 Subsystem 'PI Controller2'

PI-Controller2 in Fig. B.4.

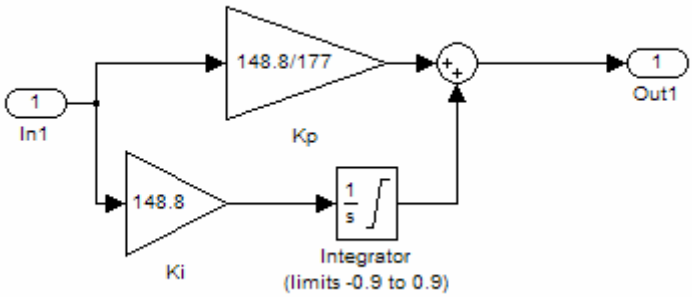


Fig. B.5. PI-controller (voltage-loop) used in DDMC and IDMC schemes- Simulation (SIMULINK) model

B.4 Tri-State Boost Converter- Indirect Dual-Model Control (IDMC) Scheme

Tri-state boost converter shown in Fig. B.1, switch logic shown in Fig. B.2, and PI-controller shown in Fig. B.5 have been used even in the IDMC scheme.

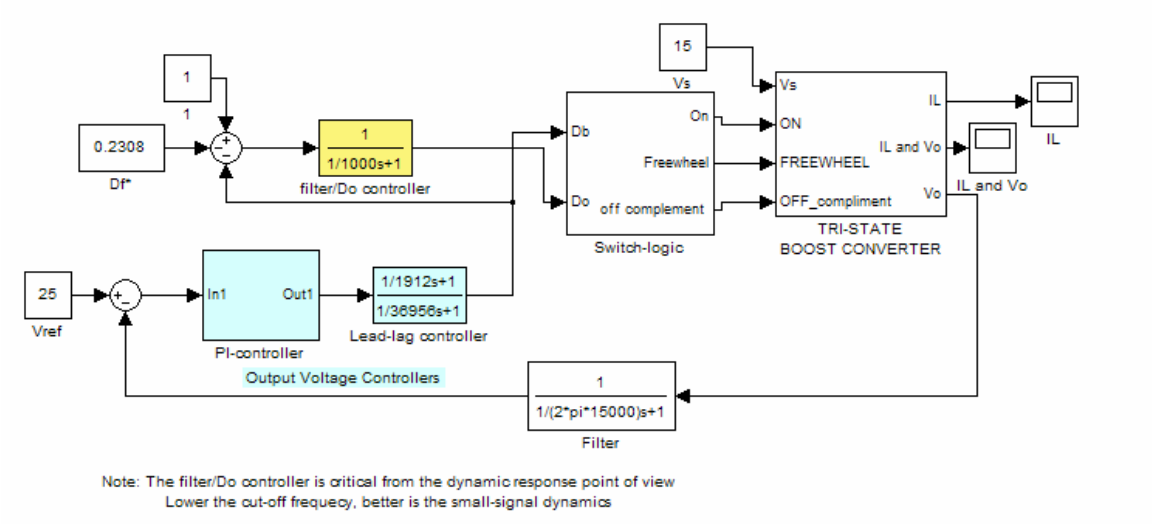


Fig. B.6. Tri-state boost converter- IDMC scheme- Simulation (SIMULINK) model

B.5 Tri-State Flyback Converter- 'Constant-D_o' Control Scheme

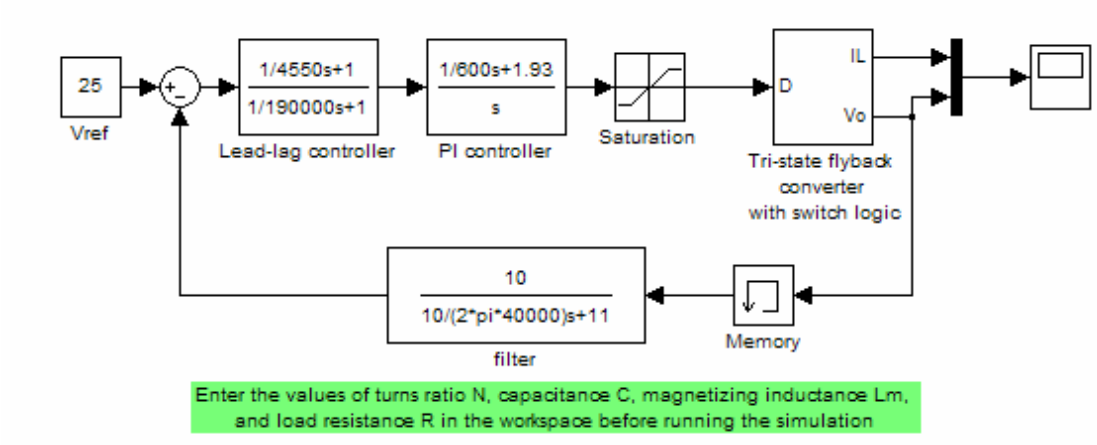


Fig. B.7. Tri-state flyback converter- 'Constant-D_o' control scheme- Simulation (SIMULINK) model

B.5.1 Subsystem 'Tri-state Flyback Converter with Switch Logic'

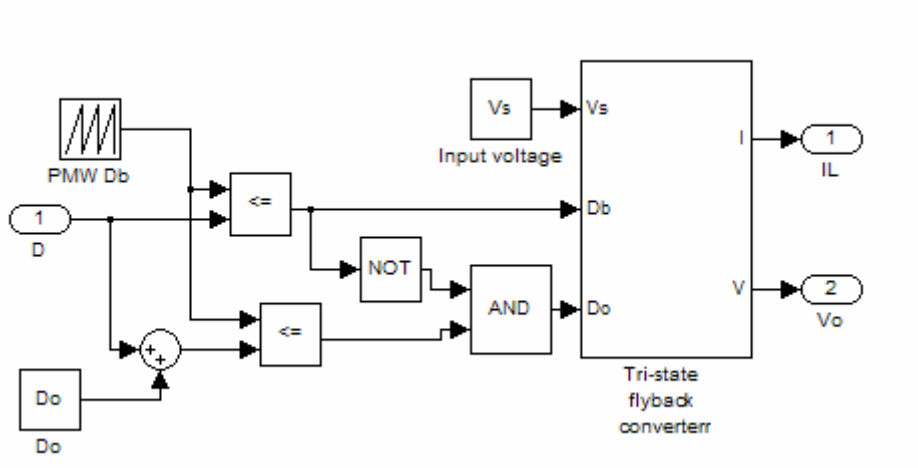


Fig. B.8. Subsystem – 'Tri-state flyback Converter with Switch logic'- Simulation (SIMULINK) model

B.5.2 Subsystem 'Tri-state Flyback Converter'

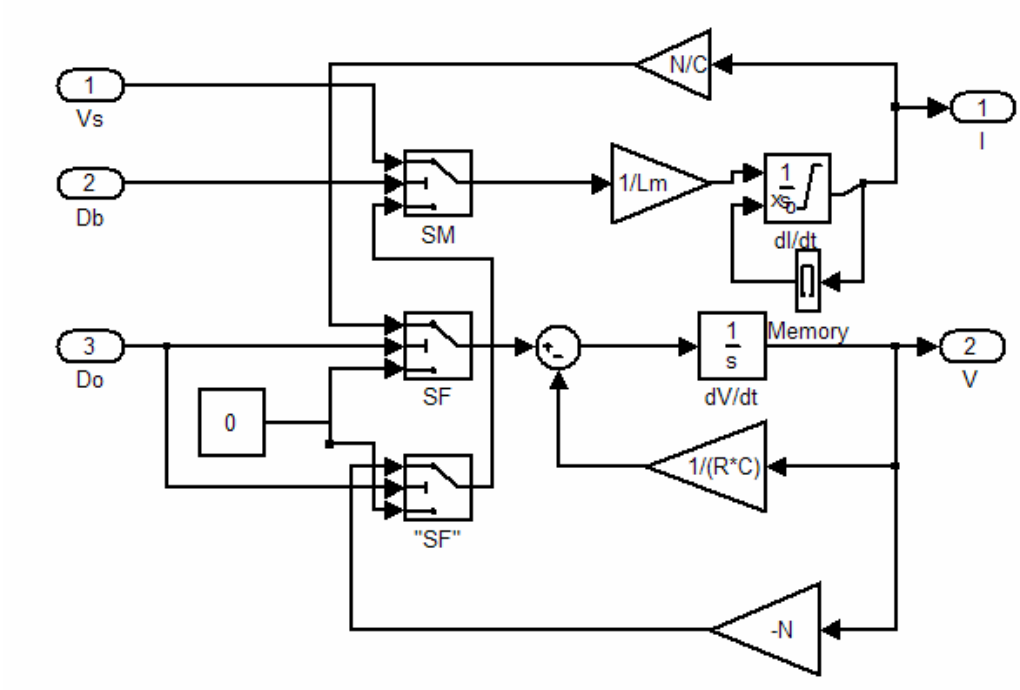


Fig. B.9. Subsystem – 'Tri-state flyback Converter - Simulation (SIMULINK) model

B.6 Dual-mode Control of Cascade Buck-Boost Power Factor Correction (CBB-PFC) Converter

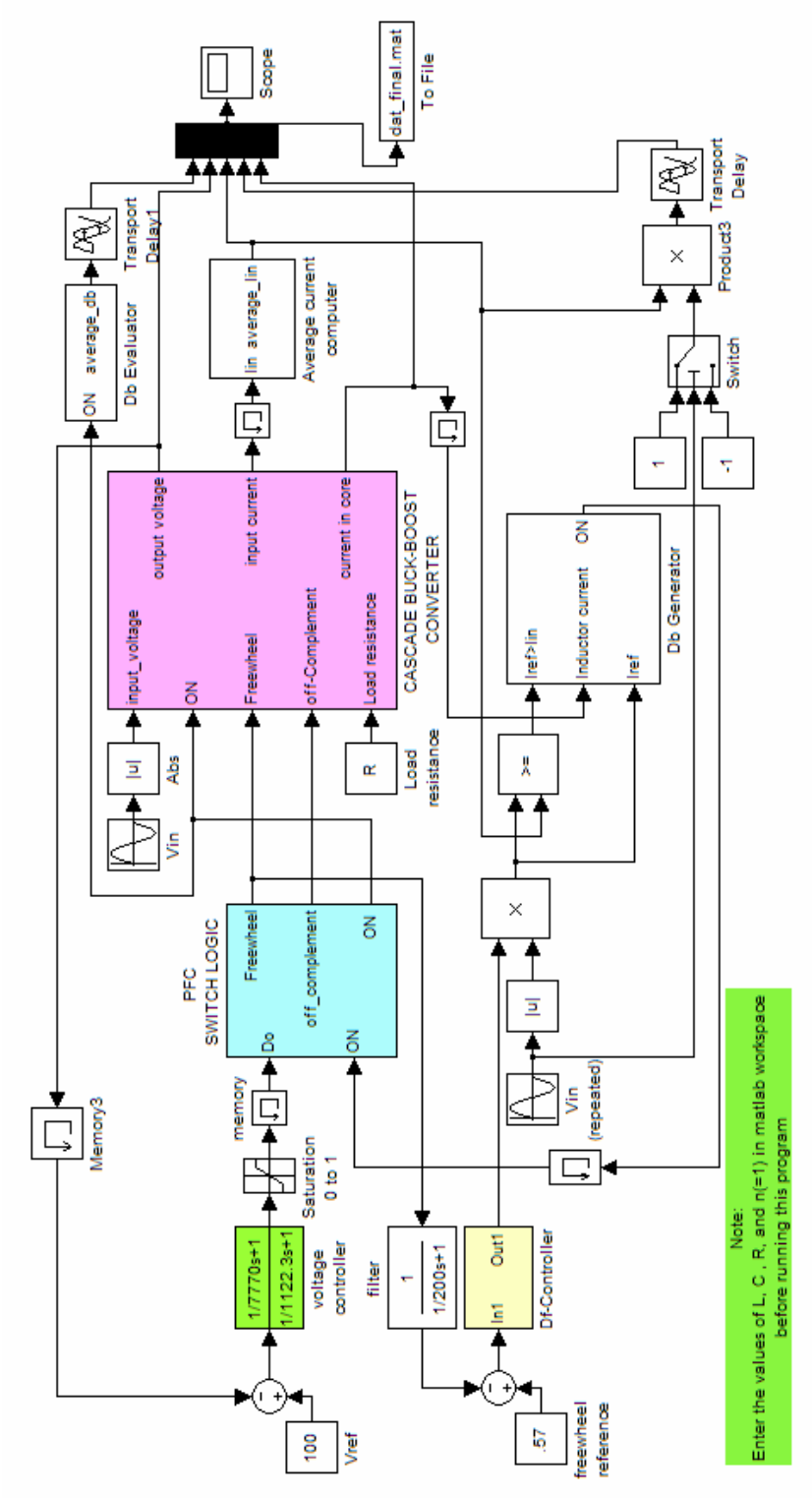


Fig. B.10. Dual-mode control of CBB-PFC- Simulation (SIMULINK) model

B.6.1 Subsystem 'CASCADE BUCK-BOOST CONVERTER'

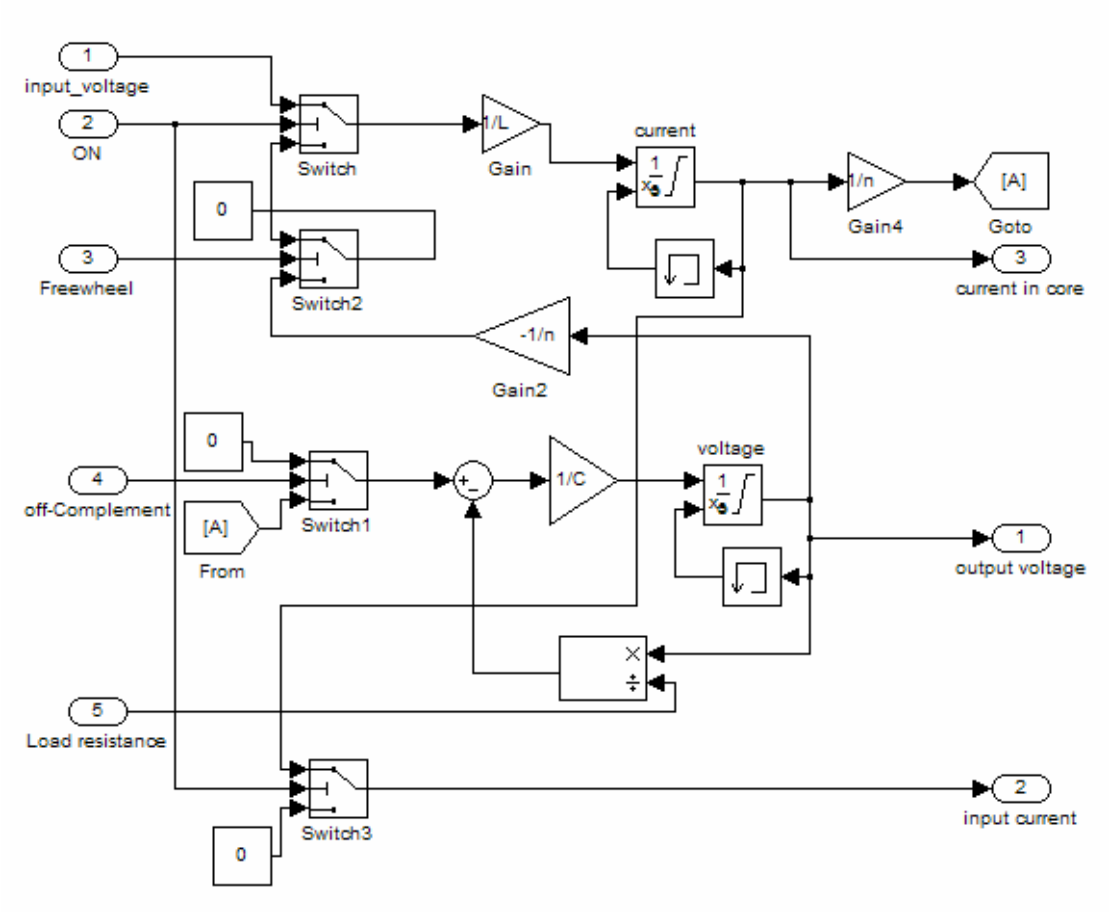


Fig. B.11. Subsystem 'CASCADE BUCK-BOOST CONVERTER'- Simulation (SIMULINK) model.

B.6.2 Subsystem 'AVERAGE CURRENT COMPUTER'

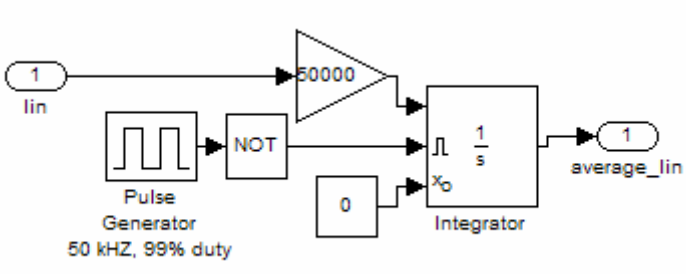


Fig. B.12. Subsystem 'AVERAGE CURRENT COMPUTER'- Simulation (SIMULINK) model

B.6.3 Subsystem ‘PFC SWITCH LOGIC’

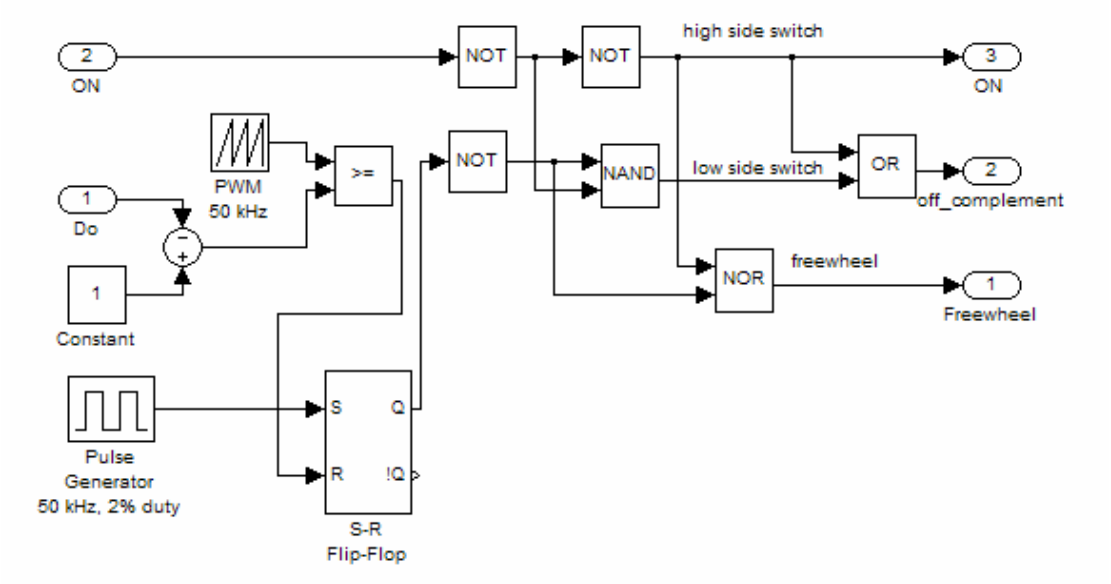


Fig. B.13. Subsystem ‘PFC SWITCH LOGIC’- Simulation (SIMULINK) model

B.6.4 Subsystem ‘Db Evaluator’

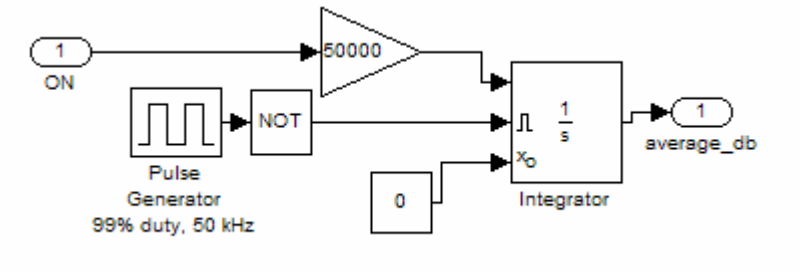


Fig. B.14. Subsystem ‘Db Evaluator’- Simulation (SIMULINK) model

B.6.5 Subsystem ‘Df Controller’

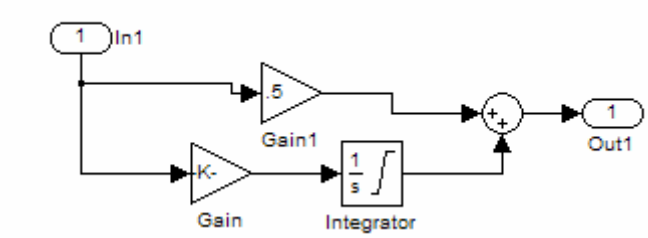


Fig. B.15. Subsystem ‘Df Controller’- Simulation (SIMULINK) model

B.6.6 Subsystem 'Db Generator'

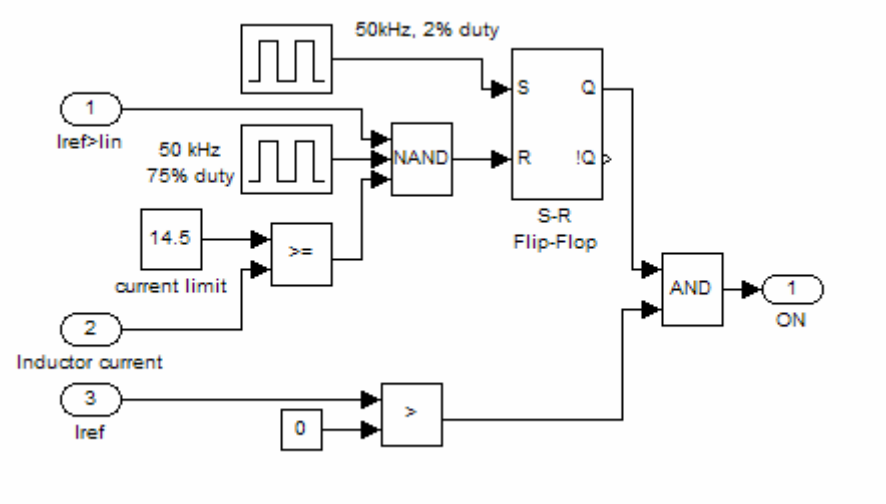


Fig. B.16 Subsystem 'Db Generator'- Simulation (SIMULINK) model

B.7 Classical Boost Converter (Averaged Model) Controlled by Gain-Scheduled PI Controller

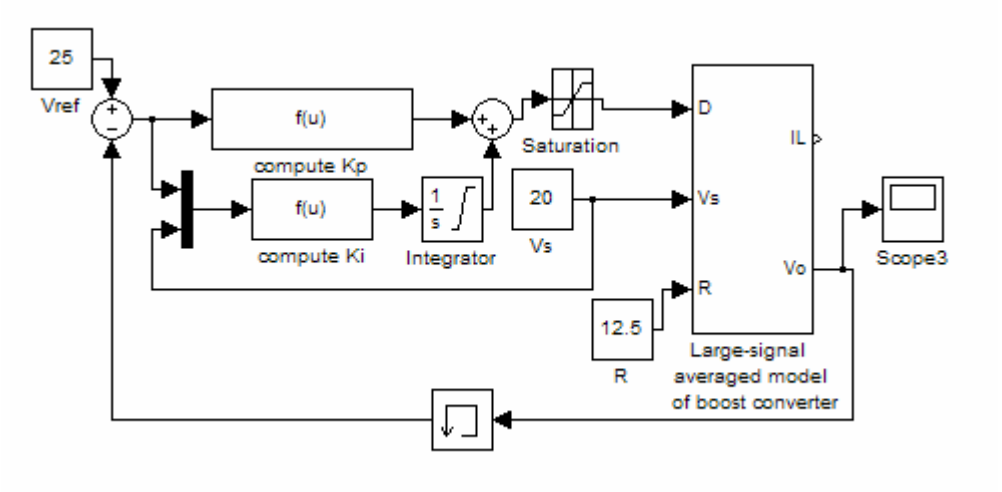


Fig. B.17 Classical boost converter with GSPI controller- Simulation (SIMULINK) model

Compute Kp:

u= Vref- Vo; f(u) = (Kpmax-(Kpmax-Kpmin)*exp(-128*abs(u)))*u

Compute Ki:

u(1)= Vref-Vo; u(2)=Vs; f(u)=u(1)*(10+2*(u(2)-10))

B.7.1 Subsystem ''Large-signal averaged model of boost converter'

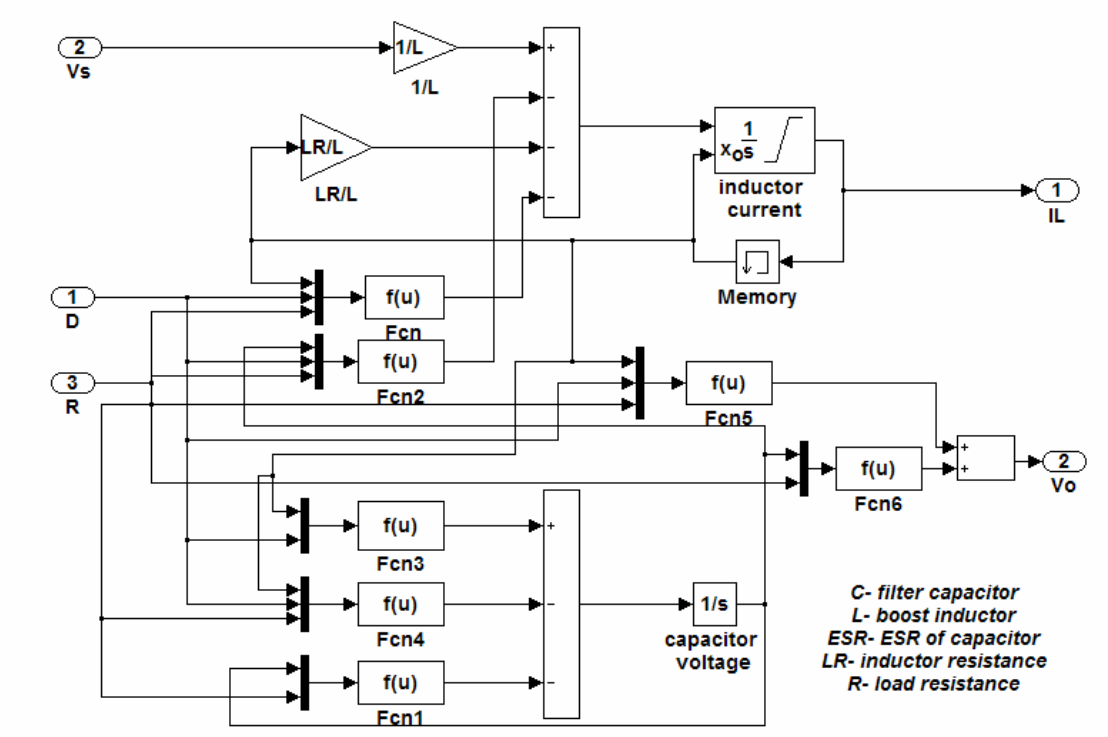


Fig. B.18 Subsystem 'Large-signal averaged model of boost converter'- Simulation (SIMULINK) model

Description of various functions:

I_L = averaged inductor

D = averaged duty ratio

V_c = averaged capacitor current

V_o = averaged output voltage

Fcn: output = I_L*(1-D)*ESR*R/(R+ESR)*1/L

Fcn1: output = V_c*R/(R+ESR)*1/(R*C);

Fcn2: output = V_c*(1-D)*u(3)/(u(3)+ESR)*1/L

Fcn3: output = I_L*(1-D)/C

Fcn4: output = I_L*(1-D)*R*ESR/(R)+ESR)*1/(R*C)

Fcn5: output = I_L*(1-D)*R*ESR/(R+ESR)

Fcn6: output = V_c*R/(R+ESR)

B.8 Classical Boost Converter (Averaged Model) Controlled by Linear-PI Controller

Large-signal averaged model of boost converter in Fig. B.18 has been used.

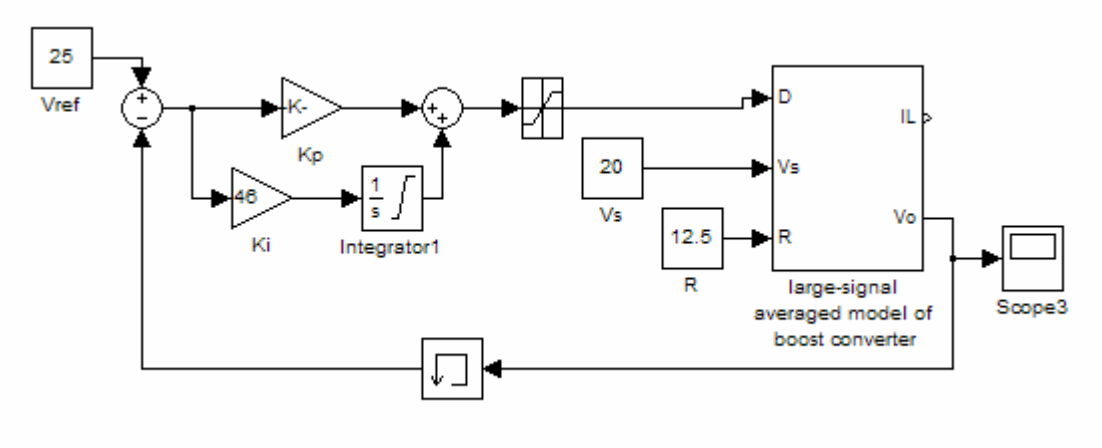


Fig. B.19 Classical boost converter with Linear-PI controller- Simulation (SIMULINK) model

B.9 Classical Boost Converter (Averaged Model) Controlled by PI-FLC and NPIC Controllers:

Refer to chapter 4 for details related to NPIC and PI-FLC blocks. Large-signal averaged model of boost converter in Fig. B.18 has been used.

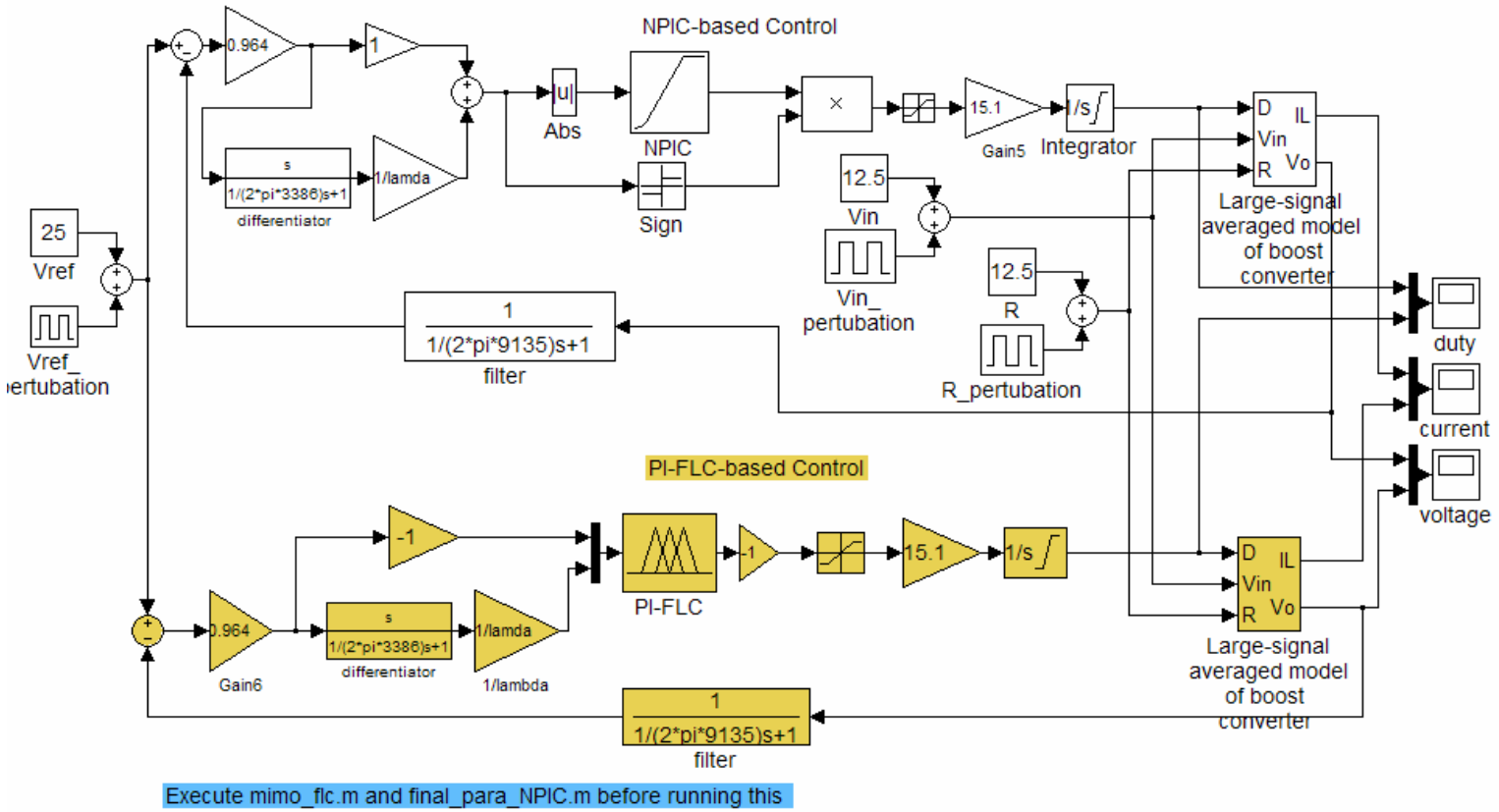


Fig. B.20 Classical boost converter with PI-FLC and NPIC Controllers- Simulation (SIMULINK) model.

APPENDIX C

HARDWARE IMPLEMENTATION DETAILS OF THE VARIOUS CONVERTER/CONTROL SCHEMES

C.0 Tri-state Boost Converter- 'Constant-D_o' Control Scheme

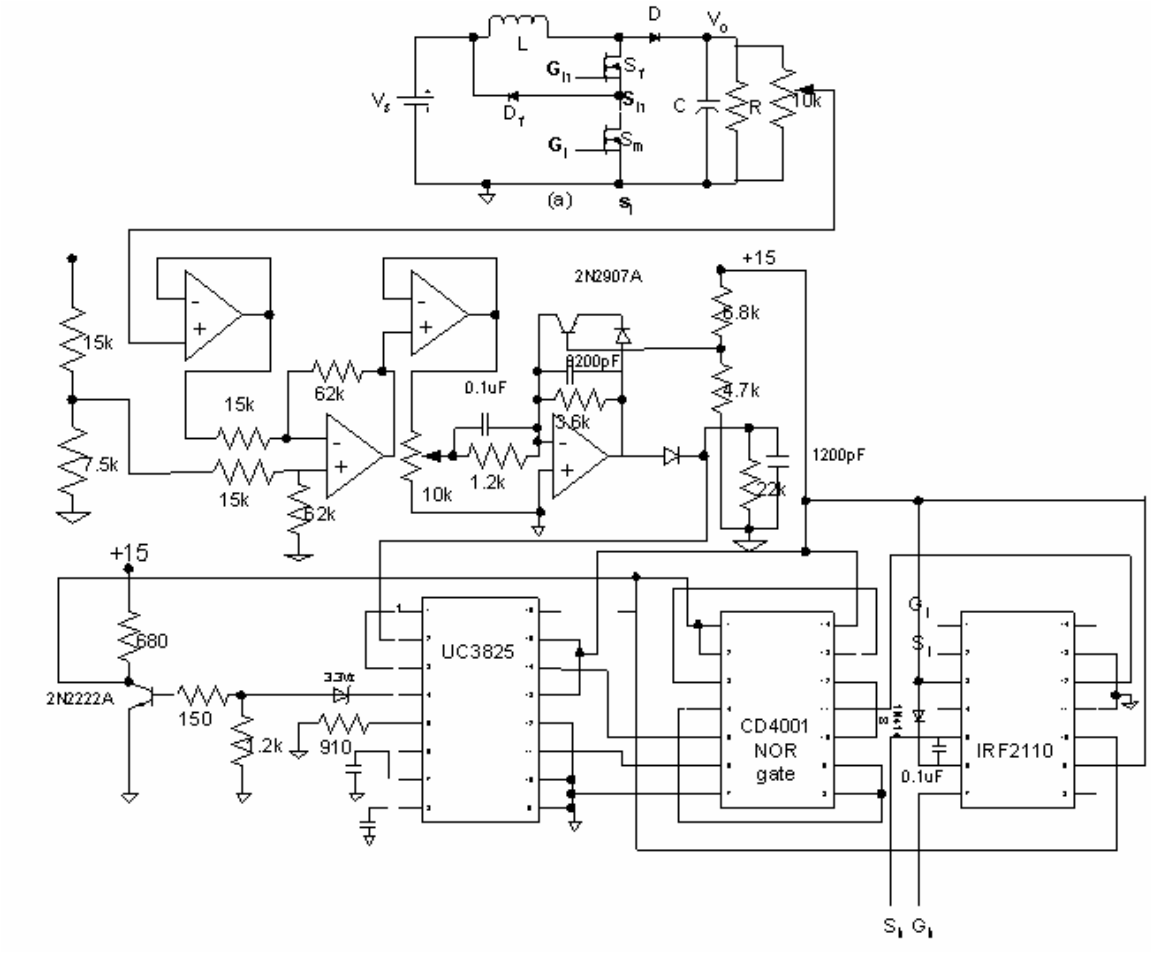


Fig. C.1. Tri-state boost converter- Hardware implementation

C.1 Classical Boost Converter- PI-based Control Scheme

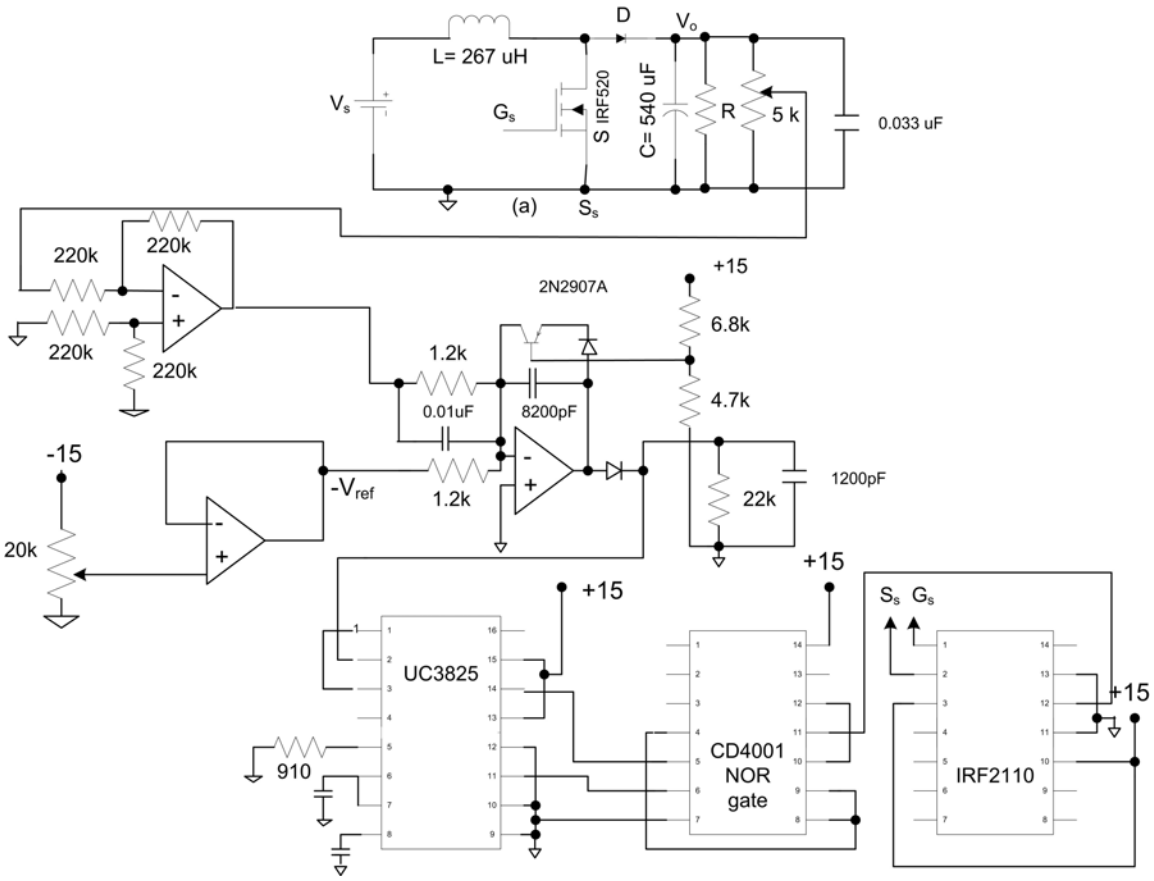


Fig. C.2. Classical boost converter- Hardware implementation

C.2 Tri-State Boost Converter- Direct Dual-Mode Control Scheme

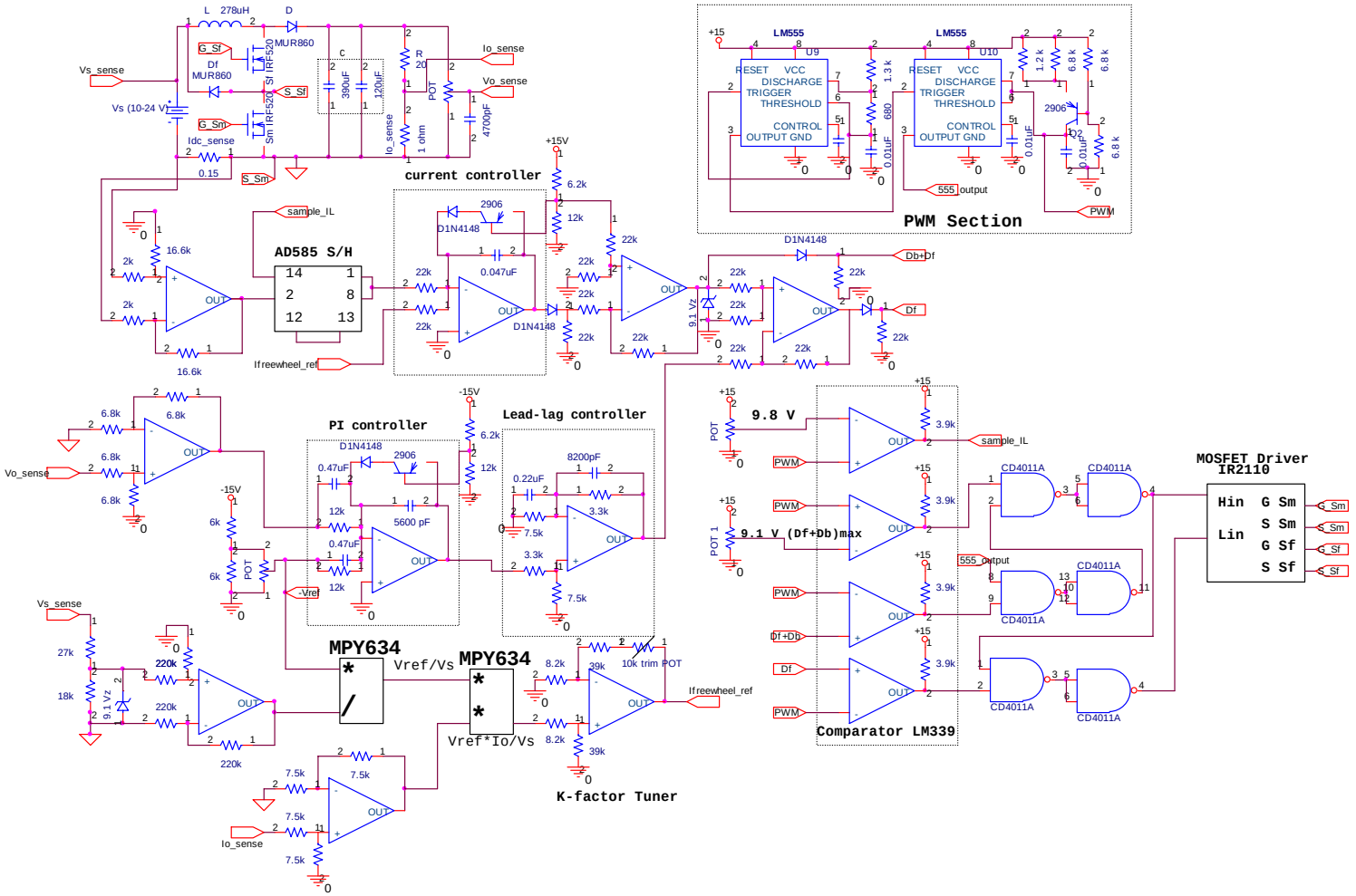


Fig. C.3. Direct Dual-mode control- Implementation

C.3 Tri-State Boost Converter- Indirect Dual-Mode Control Scheme

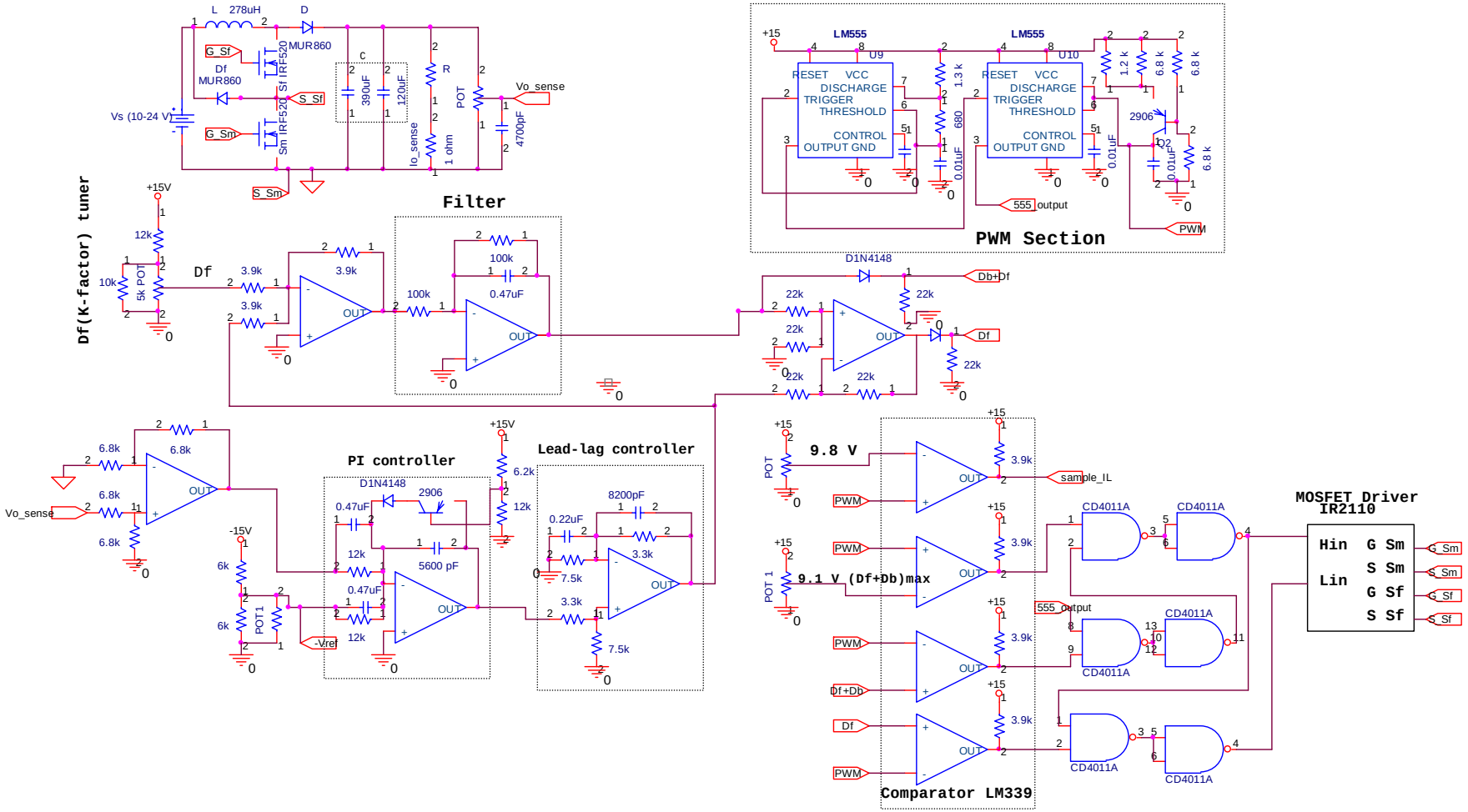


Fig. C.4. Indirect Dual-mode control- Implementation

C.4 Tri-State Flyback Converter- 'Constant-D_o' Control Scheme

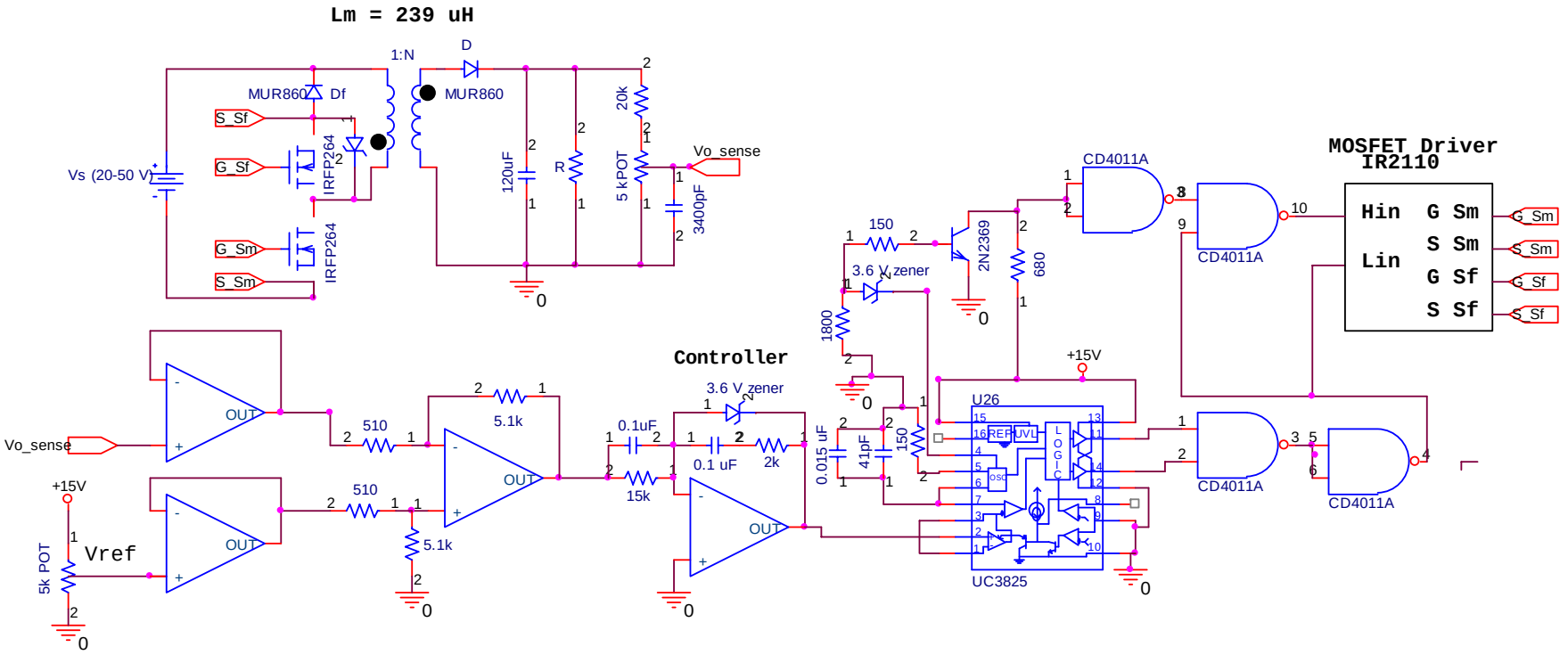


Fig. C.5. Tri-state flyback converter with 'constant-D_o' control scheme- overall schematic

C.5 Dual-Mode Control of Cascade-Buck-Boost PFC Converter- Circuit Schematic

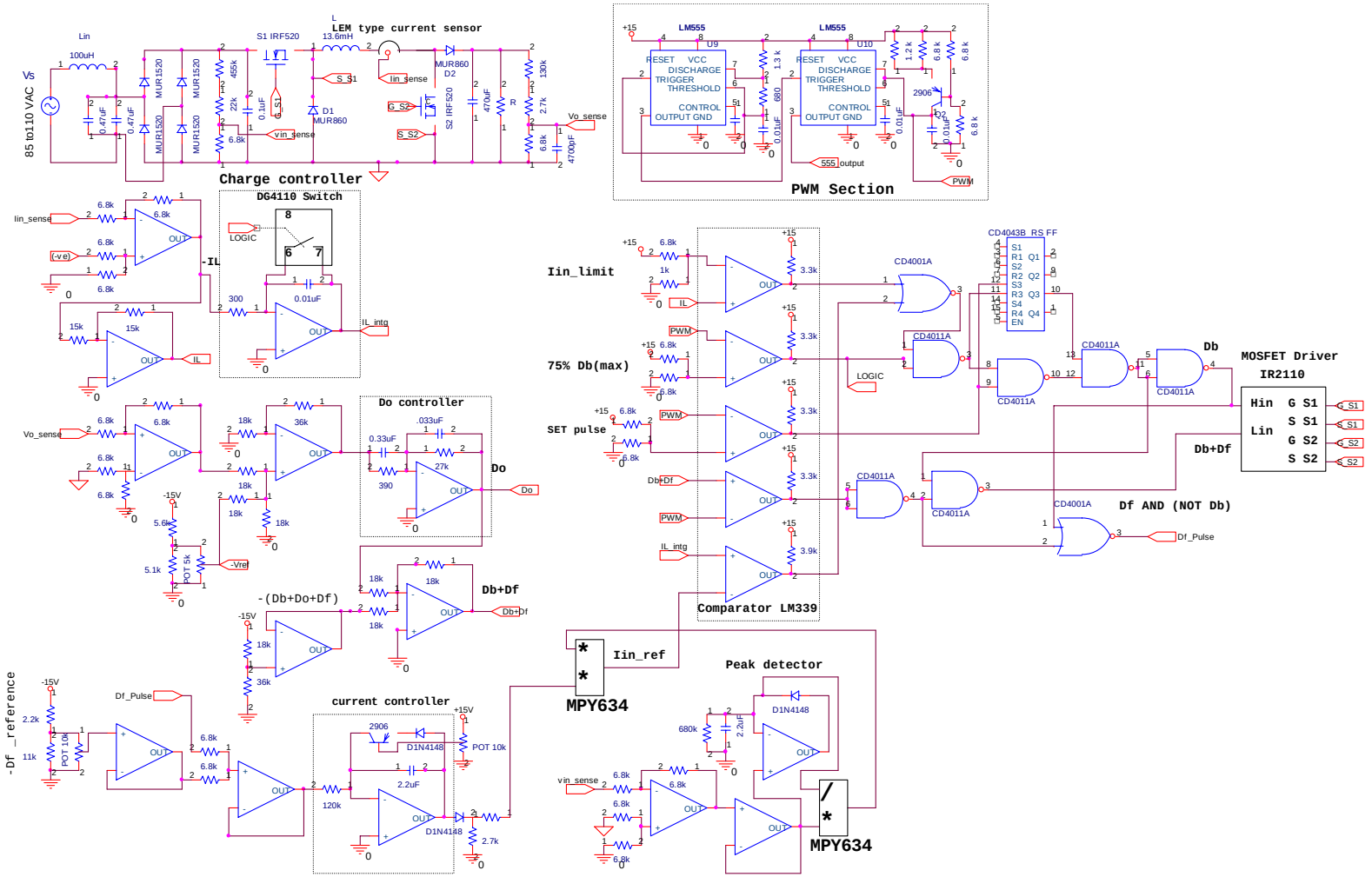


Fig. C.6. Dual-mode control of CBB-PFC- Circuit Implementation

APPENDIX D

SINGLE-PHASE AC-DC POWER FACTOR CORRECTION RECTIFIERS: A SURVEY

D.0 Introduction

One of the key applications of boost and buck-boost-derived converters is in single-phase ac-dc power factor correction (PFC). Traditionally, the front-end of off-line power supplies operating from ac-mains consists of a diode bridge rectifier followed by a bulky capacitor filter. Such an arrangement results in drawing an input current rich in harmonics, which in turn distorts the ac-mains voltage at the point of common coupling and deteriorates the quality of utility power supply. Several international standards and restrictions [82] have been imposed on the harmonic content of the current drawn form the utility. Reducing the harmonic content in the input current (this also implies improvement in input power factor) has been an active topic in power electronics since early 80's. Several PFC circuit topologies aimed at reducing the input current harmonics have emerged over the past decade. Among them, the single-switch boost PFC rectifier is the most popular one, followed by flyback-based PFC schemes. In this appendix, the power factor correction problem is presented to begin with. Following this, a literature survey on the popular PFC techniques is also given.

D.1 Single-Phase AC-DC Rectifiers- Overview of Problems

In the nutshell, the prime objectives of a PFC rectifier can be summarized as below.

1. The input current should be sinusoidal drawn at nearly unity power factor
2. The output voltage should be tightly regulated
3. The dynamic response of the converter has to be fast
4. The voltage and current stress on the switches should be low as they reflect on the cost of the converter.
5. The control scheme has to be simple and
6. The converter should be cost-effective.

Among the above listed objectives, achieving objectives 1, 2, 3, and 6 simultaneously is often a difficult task. This can be explained as below.

Let us consider a PFC rectifier drawing a sinusoidal input current I_{in} form the utility voltage V_{in} and delivering a well-regulated output voltage V_o.

$$I_{in}(t) = I_m \sin(\omega t); \quad V_{in}(t) = V_m \sin(\omega t) \tag{D.1}$$

The input power ($P_{in}(t)$) can be written as follows.

$$P_{in}(t) = V_{in}(t) \bullet I_{in}(t) = V_m I_m \left(\frac{1 - \mathrm{Cos}(2\omega t)}{2} \right) \tag{D.2}$$

The above expression shows that the input power consists of a constant component and a component that varies at twice the line-frequency. Assuming a lossless power processing, the dc-part of the input power will be equal to the output power $P_o(t)$. Thus,

$$P_o(t) = \frac{V_m I_m}{2} \tag{D.3}$$

Fig. D.1 shows the waveforms of the various quantities. With the energy input (from the source) changing at twice the line frequency and with a constant energy

demand by the load, any single-phase PFC scheme needs an extra energy-storage element to store the second harmonic power component (D.2). The extra energy-storage element increases the cost of the converter in many cases. Besides the energy-storage element, PFC converters should have at least two degrees of control-freedom to shape the input current to a sinusoid and to provide a tight output voltage regulation. Converters with less control inputs fail to meet one or more of the PFC objectives. This aspect will become clear in the next section.

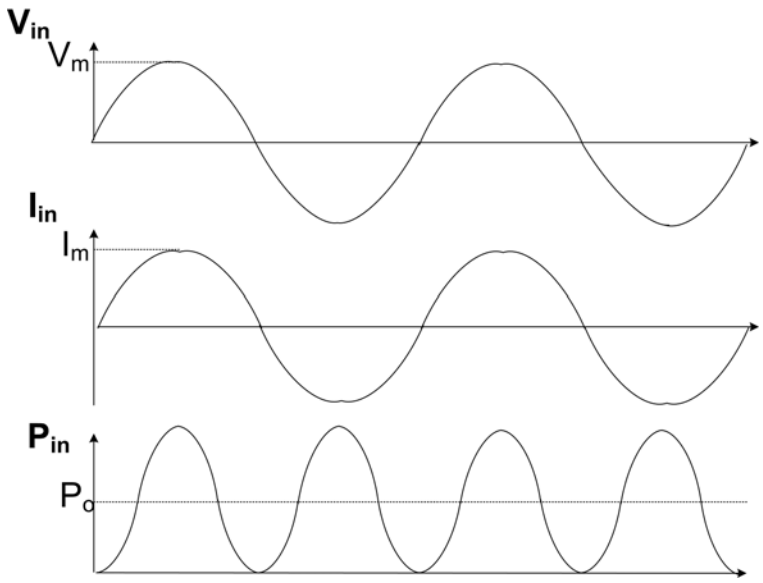


Fig. D.1. Waveforms of an ideal single-phase PFC rectifier (a) Input voltage (b) Input current (c) Input power

In general, the rate at which energy is built and processed in the extra-energy-storage element (‘reservoir’) and the amount of extra-energy stored (size of the ‘reservoir’) decide the dynamic response characteristics of the converter. While the storage-level in the ‘reservoir’ increases with its size, the rate at which energy is built and processed decreases with the increase in size of the storage element. PFC converters with large energy storage show little change in the output voltage for small load disturbances. However, sluggish dynamic response of the converter can be

observed when the load disturbance is large enough to exhaust the extra energy in the 'reservoir.'

In the case of many PFC rectifiers, in addition to the size of storage element, employing fast controllers to enhance the dynamics of output voltage often distorts the input current. Due to this, the bandwidth of output voltage loop is generally limited to below the line frequency. This will also be explained in detail in the next section by considering a boost-PFC rectifier as an example.

D.2 Applications of Boost and Buck-Boost converters in Single-Phase AC-DC Power Factor Correction and Associated Problems

In this section, a survey [30], [31] of solutions available in literature for the PFC problem is presented and discussed. For the sake of simplicity, the survey is presented on the basis of the second-harmonic energy storage available in the converter.

D.2.1 Energy Storage on Load-side Capacitor

Stand-alone boost, buck-boost rectifiers and their derivatives are popular examples that store the second harmonic energy in the output capacitor. In this sub-section, the problems associated with each of these PFC techniques are discussed.

A. Stand-Alone Boost PFC Rectifier

Fig. D.2 shows the boost-PFC rectifier with a commonly used control scheme. This converter has only one control input (duty ratio of the switch '*S*'), that can be used either to shape the input current to a sinusoid or to regulate the output voltage

tightly, but not both. Generally, shaping the input current is given a higher priority, this being a PFC converter. With an input current shaped to a sinusoid and with negligible energy storage in the inductor [2], all the second harmonic energy from the input (D.2) is passed to the filter capacitor *C*. This results in a high second harmonic ripple in the output voltage, which is generally reduced by employing a huge capacitor. On account of this high output voltage ripple, boost-PFC is generally used as a pre-regulator.

The following issues are associated with boost-PFC techniques.

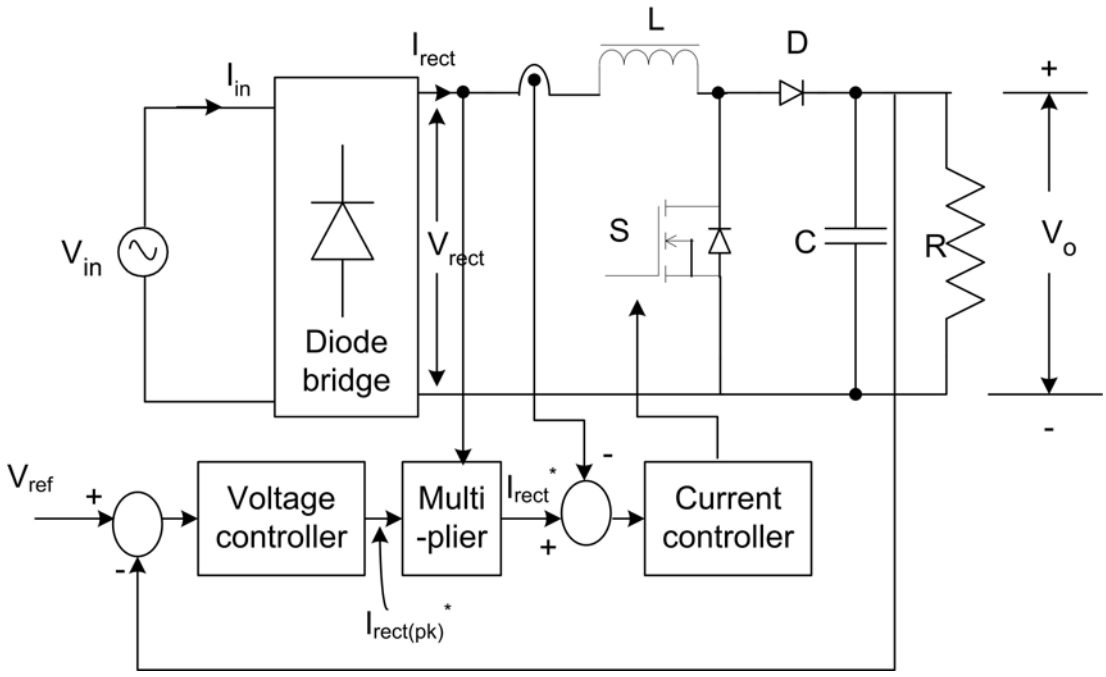


Fig. D.2. Single-phase-single-stage boost PFC rectifier (pre-regulator) - converter and control scheme.

Slow output voltage dynamics

A popular control scheme [32], [38] employed with boost-PFC is given in Fig. D.2. It may be seen that the output voltage error is processed by a voltage controller to yield the peak of the rectifier current $I_{rect(pk)}$. For the input current to have a low THD,

$I_{rect(pk)}$ should ideally be a dc. To achieve this, the second harmonic ripple in the output voltage should be prevented from distorting $I_{rect(pk)}$. This demands the need for the voltage control loop to have a bandwidth less than twice the line frequency (100 Hz or 120 Hz). Typically, a low voltage-loop bandwidth (20 Hz) is realized [32].

One of the ways of improving the voltage-loop bandwidth would be to estimate the voltage ripple and filter it from the sensed output voltage signal. Such a ripple compensation technique has been employed in [33]. A voltage loop bandwidth of 100-200Hz has been reported. Although this is a significant improvement over the bandwidth obtained from a classical control scheme without ripple estimation, the scheme is complex. Reference [34] reports another ripple estimation technique based on adaptive learning. However, here also the scheme is complex as it employs phase-locked loop and requires sensing of the output current.

Reverse recovery loss

Another issue which is of significant importance in boost-PFC circuits is the power loss due to reverse recovery of the output diode. During reverse recovery process (occurs when the main switch turns on), the reverse recovery current of the diode flows through the boost switch. This increases the turn-on losses of the boost switch and causes severe electromagnetic interference problems.

A simple way of reducing the effect of reverse recovery problem is to employ ultra fast recovery diodes. Silicon-carbide (SiC) diodes that have negligible reverse recovery current can avoid this loss. However, besides being expensive, the forward voltage drop of SiC diodes is also high (about 2.5 V).

Another way of alleviating this problem would be to operate the converter in discontinuous-conduction mode (DCM) or in DCM-CCM boundary. However, operation in DCM or at the border of DCM-CCM increases the current stress on the switches. Reference [35] introduces a new branch consisting of a diode and a coupled winding of the boost inductor and alleviates the problem due to reverse recovery of the output diode. A 2% improvement in efficiency of the boost converter has been reported.

Avoiding the input voltage sensor and multiplier/divider in the control scheme

The boost-PFC scheme in Fig. D.2 needs sensing of the input voltage. Besides, the scheme employs multipliers and divisors for modulating the duty ratio to shape the input current to a sinusoid and for input voltage feed-forward. If the input voltage sensor and multiplier circuitry are avoided, significant reduction in component count and cost of the converter will be achieved. Several control schemes that avoid input voltage sensor and multipliers/dividers are available in literature. Reference [36] discusses a technique of avoiding the input voltage sensor in boost and buck-boost based PFC rectifiers. The following discussion describes the underlying motivation.

Under steady-state the input current and input voltage are in phase and the power converter emulates an equivalent resistance R_{eq} given by

$$\langle I_{in} \rangle = \frac{V_{in}}{R_{eq}} \tag{D.4}$$

where $\langle I_{in} \rangle$ is the average input (inductor) current in one switching cycle. The relation between input and output voltages is given by

$$V_o = \frac{V_{in}}{(1-D)} \tag{D.5}$$

Substituting (D.5) in (D.4)

$$\langle I_{in} \rangle = \frac{V_o}{R_{eq}}(1-D) \tag{D.6}$$

In (D.6), the unknown duty *D* can be obtained by comparing the average input current (obtained in the previous switching cycle) with a waveform (refer Fig. D.3) whose time variation in every switching period '*T*' is given by

$$\frac{V_O}{R_{eq}}\left(1-\frac{t}{T}\right) \tag{D.7}$$

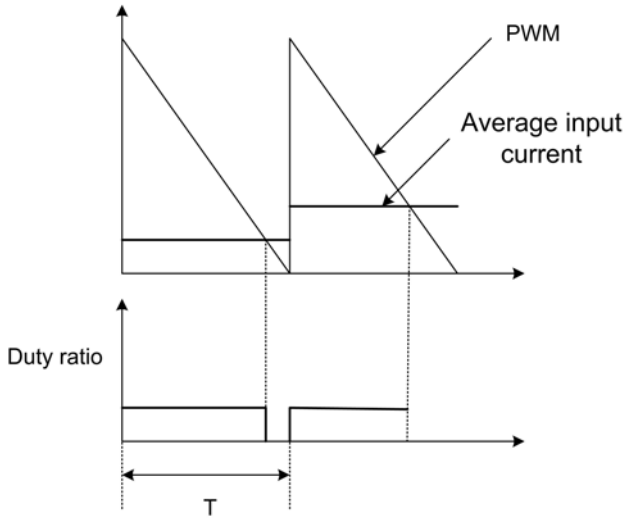


Fig. D.3. Avoiding the input voltage sensor and multipliers

References [37] and [42] discuss similar ways of avoiding the input voltage sensor and multipliers in which the diode current and switch current are respectively sensed and used generate the duty ratio pulse.

Inrush current

Almost all boost-based PFC converters suffer from inrush current problem when powered on as there is no series switch to limit the rising current. This problem in the case of PFC rectifiers attracts significant importance as the magnitude of inrush current depends on the part of the ac cycle at which the circuit is powered on.

Thermistors with negative temperature coefficient limit are generally used to limit the inrush current.

Device voltage stress

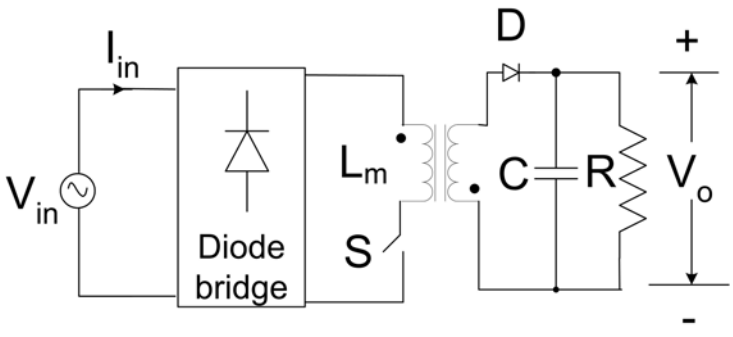
The voltage stress across switches and diodes used in stand-alone boost PFC rectifiers is equal to the output voltage, which is higher than the peak of the line voltage. This, in particular, plays a critical role in deciding the cost of the converter.

B. Single-Switch Buck-Boost/Flyback PFC Rectifier

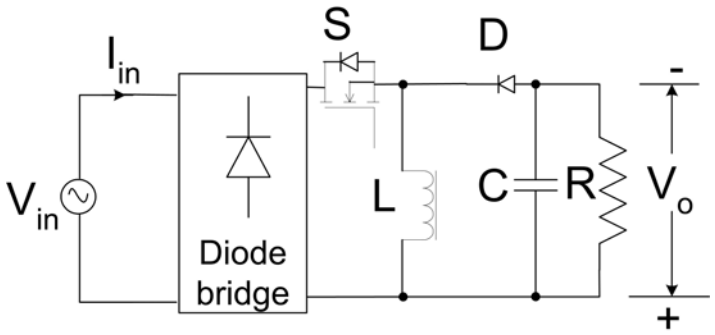
Flyback and buck-boost converters typically use the output capacitor as the extra energy-storing element in PFC applications (refer Fig. D.4). Flyback converters operating in DCM are very popular in small and medium power PFC converters for the following reasons.

1. When operated in DCM with a constant duty ratio, the average input current follows the shape of the input voltage and the additional current loop is avoided.
2. The output voltage can be adjusted to be even lower than the peak of the input voltage, if required.
3. Unlike the boost PFC rectifier, the buck-boost and flyback PFC rectifiers avoid the inrush current problem due to the presence of a series switch.
4. Implementation of galvanic isolation between the input and the output is simple with flyback topology.

Some of the important issues related to flyback/buck-boost-based PFC topology are listed below.



(a)



(b)

Fig. D.4. Circuit diagram (a) Flyback PFC (b) Buck-boost PFC

Input Current and Current Control Loop

Unlike the boost converter, the input current of flyback/buck-boost PFC topology is chopped. This increases the EMI-associated problems and filtering requirements. When operated in DCM, the device current stresses and EMI filtering requirements are much higher than those when operated in CCM.

For flyback and buck-boost PFC converters operating in CCM, the control scheme generally implemented is almost similar to the one implemented with the boost PFC converter (Fig. D.2). However, as the input current is not the same as the inductor current, a charge-control-based [39] input current control is typically implemented with flyback converters [40].

Slow Dynamic Response

Similar to boost-PFC converter, the output voltage dynamics of flyback-PFC operating in CCM is slow. The small-signal bandwidth obtained is generally less than the line frequency (50 or 60 Hz).

Large Filter Requirement

The storage of second-harmonic energy in the output capacitor increases the size of the output capacitor. Unlike the boost-PFC converter, as the output voltage can even be less than the peak value of the line voltage, the size of the capacitor depends on the magnitude of the output voltage, the lower the output voltage, the larger is the capacitance.

Leakage Inductance of the Flyback Transformer

A common problem with flyback converter is the leakage inductance of the primary winding that causes high voltage spikes when the switch is turned-off. The energy trapped in the primary inductance when the flyback converter is operated as a dc-dc converter may be transferred back to the source by using a two-switch topology. However, in PFC application, due to the presence of diode bridge, the energy cannot be pumped back to the source. Reference [41] suggests a two switch flyback converter with regenerative clamping in which the energy trapped in the leakage inductance is transferred to the source.

Device voltage stress

The maximum voltage stress across the (primary-side) switch is very high being the summation of the input voltage peak and the output voltage reflected back to the

primary. The maximum voltage stress across the diode on the secondary side is equal to addition of output voltage and peak of the line voltage transferred to secondary.

Avoiding the input voltage sensor and multiplier/divider in the control scheme

Similar to the case of boost-PFC rectifier control, [36], [43] and [44] present control schemes for flyback/buck-boost PFC rectifier operating in CCM in which the input voltage sensor and multiplier and are avoided. The motivation may be briefly described as below.

Under steady-state, the average input (switch) current is in phase with the input voltage and the converter emulates a resistance R_{eq}.

$$\langle I_{in} \rangle = \frac{V_{in}}{R_{eq}} \tag{D.8}$$

where $\langle I_{in} \rangle$ is the average input (switch) current in one switching cycle. The input and output voltages are related by

$$V_o = n\frac{DV_{in}}{(1-D)} \tag{D.9}$$

where, n is the turns ratio of the transformer. Substituting (D.9) in (D.8)

$$\langle I_{in} \rangle = \frac{1}{T}\int_0^{DT} i_s(t)dt = \frac{V_O}{R_{eq}}\frac{(1-D)}{nD} = \frac{V_O}{nR_{eq}}\frac{T}{t}\left(1-\frac{t}{T}\right) \tag{D.10}$$

In (D.10), the unknown duty *D* can be obtained by comparing the integral of switch current with a non-linear carrier waveform (refer Fig. D.5) whose time variation in every switching period ‘T’ is given by

$$\frac{V_O}{nR_{eq}}\frac{T}{t}\left(1-\frac{t}{T}\right) \tag{D.11}$$

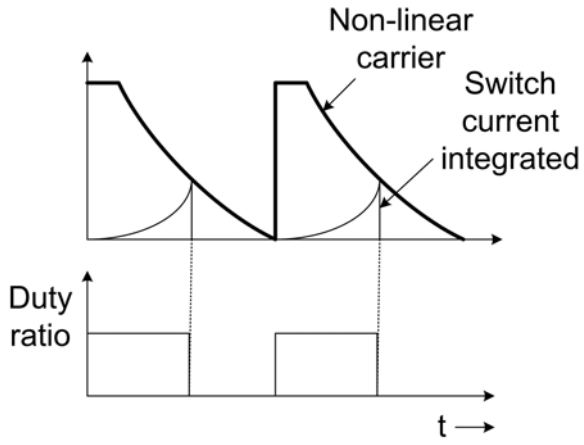


Fig. D.5. Avoiding the input voltage sensor and multipliers

D.2.2 Energy Storage on the Intermediate Bus Capacitor

Cascaded PFC scheme, BIFRED and BIBRED converters and parallel PFC (PPFC) schemes are few examples of PFC schemes that store the second harmonic energy in the intermediate capacitor.

A. Cascaded PFC Scheme

As PFC converters are needed to shape line current to a sinusoid as well as deliver a tightly regulated output voltage, a cascaded boost-buck or boost-forward scheme [30], [31] (Fig. D.6) is commonly used to meet both the load-side and line-side objectives. In such a scheme, the first (boost) stage is controlled to shape the input current to a sinusoid. The load-side converter is controlled to deliver a tightly regulated output voltage. The intermediate bus capacitor stores the second harmonic energy.

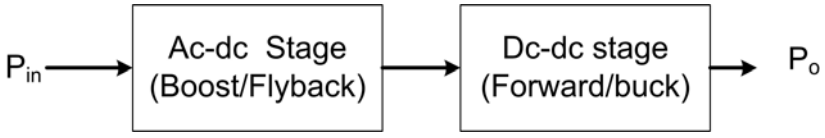


Fig. D.6. Cascaded PFC scheme

The following issues are important in relation to cascaded PFC scheme.

1. The maximum device stress of the devices is equal to the intermediate bus voltage, which is higher than the peak of the input voltage.
2. The scheme has a high component count, weight, and cost.
3. The rated output power P_o is processed twice before being dumped into the load. This reduces the operating efficiency of the scheme.

Nevertheless, the cascaded scheme is still popular as it offers excellent load-side dynamic response (with the energy stored in the intermediate bus capacitor being sufficiently high) and meets very well the line and load side requirements.

B. Single-Stage PFC {S^2PFC} Schemes

S^2PFC schemes are obtained by reduction of cascaded converter schemes in which the cascaded stages share the same electronic switch. BIFRED (Boost integrated with Flyback rectifier/energy storage/dc-dc converter), BIBRED (Boost integrated with Buck rectifier/energy storage/dc-dc converter) [45], and S^2IP^2 (single-stage isolated power factor corrected power supply) schemes discussed in [46] are well-known members belonging to this category. While BIFRED converter has been derived by reducing the cascaded schemes of boost & flyback, BIBRED converter has been obtained from the cascaded combination of boost & forward topologies. The S^2IP^2 in [46] has been derived from the cascaded combination of boost and forward converters.

These converters, like the original cascaded scheme store energy in the intermediate bus capacitor. However, unlike the original cascaded scheme, they have only one switch which is shared between the line side and load-side stages. Thus, the

control freedom is greatly reduced. References [45] and [46] suggest the use of duty ratio variations for regulating output voltage and switching frequency variations for reducing the input current harmonics. A voltage-loop bandwidth of 10 kHz has been reported with the scheme in [45].

One of the disadvantages of S^2PFC schemes is that the boost-stage is generally operated in DCM. This increases the switch current stress. Another disadvantage is that the efficiency of power conversion is generally low similar to the cascaded scheme. Besides, the control complexity is also high.

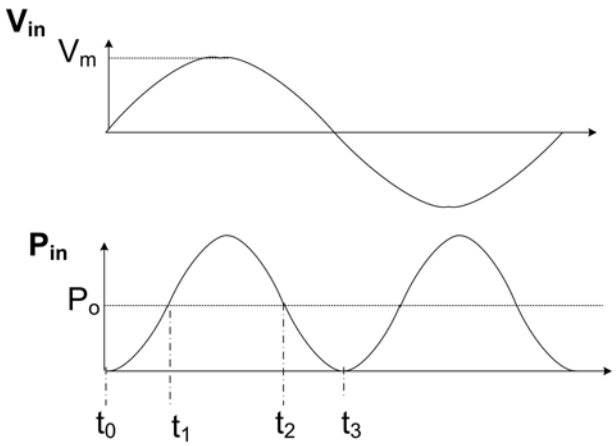


Fig. D.7. Input and output power waveforms to illustrate PPFC concept

C. Parallel PFC Schemes (PPFC)

Fig. D.7 shows the input and output powers of the PFC scheme drawing sinusoidal input current from the ac mains. From t_1 to t_2, the input power drawn is higher than the load power, whereas from t_0 to t_1 and from t_2 to t_3, the output power delivered is higher than the input power. In PPFC schemes, the excess input power between t_1 to t_2 is stored in an additional storage capacitor and is used up during t_0 to t_1 and t_2 to t_3. It may be shown that unlike the cascaded scheme wherein the entire

rated power is processed twice resulting in efficiency degradation, in this case, only 32% of the rated power is processed twice. This results in efficiency improvement.

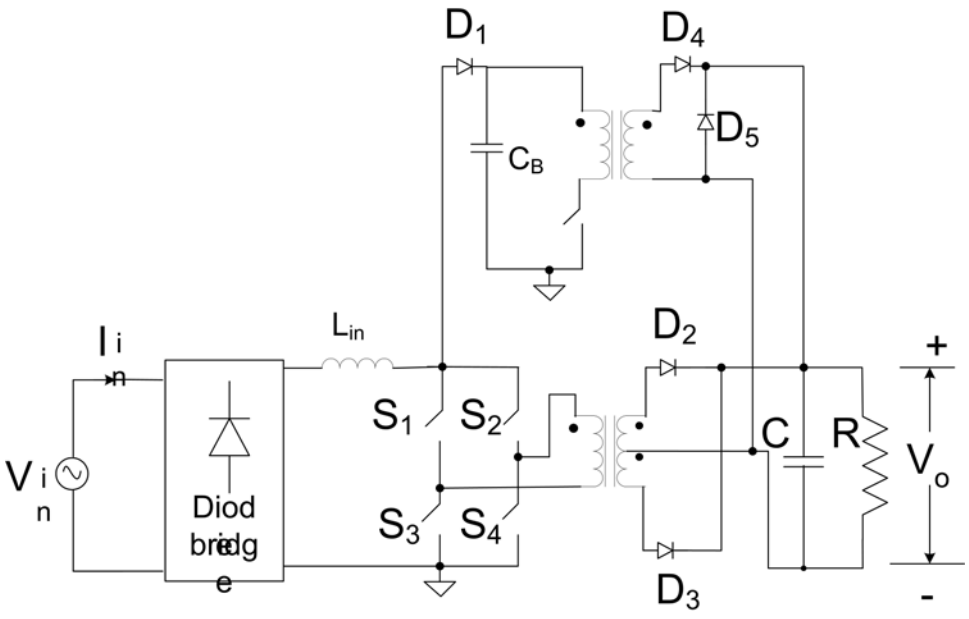


Fig. D.8. Full Bridge Boost Parallel PFC scheme

PPFC schemes have been discussed in [51] and [52]. The scheme in [51] is shown in Fig. D.8. Here, 68% of the rated power flows from the ac mains to the load while the rest 32% is stored in C_B and processed twice by the boost-forward topology. A full-load efficiency of about 90% has been reported. Besides, fast output voltage dynamics is also achieved, although not demonstrated experimentally. Reference [53] presents a systematic approach of deriving PFC converter configuration that achieves tight output regulation. Systematic circuit synthesis aimed at achieving high operating efficiency through a reduction in the redundant power processing is also discussed.

D.2.3 Energy Storage in Cascade Buck-Boost Converter and in Two-Switch Buck-Boost Converter

Fig. D.9 shows a cascade-buck-boost (CBB) PFC rectifier. This converter is the dual of cascaded boost-buck scheme discussed in the previous section. Similar to a

buck-boost/flyback converter, this converter is capable of delivering an output voltage less than the peak of the input voltage, if desired. In addition, the converter has an addition degree of control freedom that can be effectively exploited to achieve sinusoidal input current and tight output voltage regulation. Besides, the converter is also known popularly for low device voltage stresses.

Either the inductor *L* or the capacitor *C* can be used to store the second harmonic energy drawn from the line.

References [47] and [50] employ control schemes that switch the CBB converter operation between buck and boost modes based on the relative magnitudes of the instantaneous input and output voltages. The second harmonic energy in these schemes is stored primarily in the output capacitor. These schemes focus mainly on shaping the input current and do not fully exploit the control freedom (due to the presence of two switches) offered by the converter. As a result, the output voltage contains second (line frequency) harmonic ripple and its dynamic response is slow.

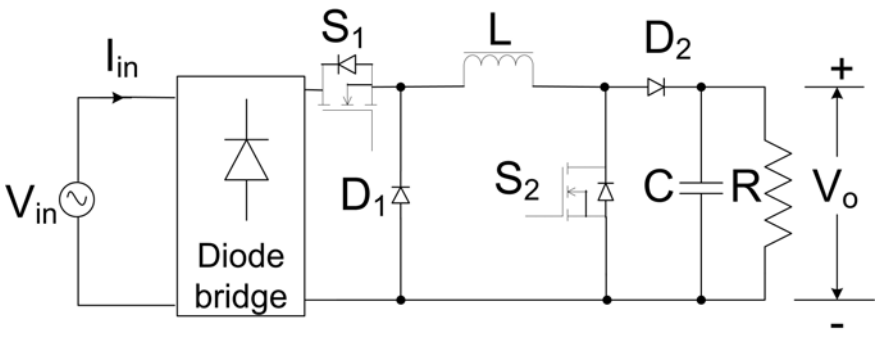


Fig. D.9. Cascade buck-boost PFC scheme

Reference [48] employs a sliding-mode based control scheme which does exploit the control freedom due to the presence of two switches. In the scheme, the second harmonic energy is stored in the inductor. Issues related to selection of

inductor current reference in the control scheme, the magnitude of inductor current under various load and line conditions, and trade-off between inductor size and converter efficiency have not been addressed in the paper.

Reference [49] proposes an inverting two-switch buck-boost PFC converter and a control scheme that under ideal conditions meets the steady-state objectives of the PFC converter by storing the second harmonic energy in the inductor. However, the paper does not present results demonstrating the dynamic behavior of the converter/control scheme. Also, as the output voltage is not directly controlled, but controlled through the shaping of the inductor current, the presence of circuit parasitics which are not taken into account in shaping the inductor current will result in high output voltage ripple.

In chapter 8 of the thesis, a novel dual-mode control scheme for CBB-PFC is presented. The control scheme helps to meet the steady-state objectives of PFC by storing energy in the inductor. Design issues related to the selection of power and control components are discussed in detail with the help of an example. The steady-state and dynamic performance of the converter are demonstrated though simulation and experimental results.