READOUT ELECTRONICS FOR MICROBOLOMETER INFRARED FOCAL PLANE ARRAY

QIAN XINBO

NATIONAL UNIVERSITY OF SINGAPORE

2004

READOUT ELECTRONICS FOR MICROBOLOMETER INFRARED FOCAL PLANE ARRAY

QIAN XINBO
(M. Sc., CAS)

A THESIS SUBMITTED
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING
NATIONAL UNIVERSITY OF SINGAPORE
2004

Acknowledgements

I wish to express my sincere gratitude to my supervisors, A/Prof. Yong Ping Xu and A/Prof. Gamani Karunasiri, for their interest, guidance and support throughout the course of this work. Their profound knowledge and rigorous scientific approach have greatly inspired me in the research. Their advices to me on all matters, not just the professional help, are greatly appreciated and are something I will ever benefit from.

My thankfulness also extends to my senior colleagues Mr. H.-J. Wu, Mr. X.-B. He and Mr. C. Y. Hui. They have greatly helped me in the research. Especially at the initial stages, I got a lot of support and helpful suggestions through the technical discussions with them. I would also thank Ms. Musni Hussain, Mr. Francis Boey and Mr S. M. Teo for their assistance in the experimental set-up. My appreciation also goes to Dr. V. Samper of Institute of Microelectronics (IME) for providing me the microbolometer samples and focal plane arrays.

Many thanks to graduate students in Center for Opto-electronics and VLSI Lab, in particular, Mr. L.-F. Zhou, Ms X.-W. Zhang, Ms. L.-C. Xu and Mr. Rama Krishna MVS for their kind help. I really enjoy and appreciate the time I have spent with them.

Finally, I would like to thank my family for their continuously support and encouragement.

Table of Contents

Summary

Uncooled microbolometer infrared detectors have a number of advantages over other types of detectors. They have showed their commercial potential to realize low-cost, high-performance infrared imagery systems. Microbolometer changes its resistance in response to the infrared radiation. In order to monitor the change of the resistance, microbolometers need to be electrically biased during the operation. Unfortunately, the bias current flowing through the microbolometer generates the heat on the sensor itself. This unavoidable self-heating effect will severely affect the readout circuits, such as the degradation of the dynamic range. The continuing improvement on the performance of the uncooled thermal imagers have driven the motive of developing an effective circuit for self-heating cancellation that can be applied to on-chip readout electronics for the microbolometer focal plane array.

This project looks into a novel technique of self-heating cancellation for microbolometer. Such a cancellation scheme is based on the equivalence between the electrical and thermal systems, and uses a capacitor to mimic the thermal capacitance of the microbolometer. A replica of the bias heating can generated on the capacitor and later used to cancel the self-heating of the bolometer. The concept of using the electrical equivalence of bolometer's thermal parameter to build the replica of self-heating is extended to current-mode readout circuits. A PMOS transistor working in the triode region is used to generate the ramp current to compensate the self-heating effect in a current subtraction circuit. Both voltage- and current-mode self-heating cancellation circuits are realized in silicon and the effectiveness is demonstrated with a single microbolometer.

The voltage- and current-mode ROICs (readout integrated circuits) with the proposed self-heating cancellation circuit have been developed together with on-chip 8-bit fixed pattern noise (FPN) correction circuits. The ROICs were fabricated in a 0.6 μm CMOS technology. The voltage-mode ROIC was evaluated with an external 128 × 128 microbolometer FPA. The test results have shown that the FPN can be corrected to a 7-bit resolution when exclude the pixels with unexpected large FPN from test, and an 8-bit resolution can be attained when tested with a built-in resistor array. The current-mode ROIC has been evaluated with a built-in 8 × 8 resistor array for the performance of FPN correction, since the microbolometer FPA for current-mode ROIC is not available. The measured residual FPN of less than ±2.5 LSB has been achieved. Due to the unavailability of proper microbolomter FPAs, the self-heating cancellation cannot be demonstrated with the on-chip FPN correction in the ROICs.

List of Figures

List of Tables

List of Symbols

Symbol	Description	Unit	Page No.
α	Temperature coefficient of resistance	1/K	6,43,50,53,60 ~ 63, 91,92
ε	Absorptivity coefficient		41
ϕ_e	Spectral incident infrared power	W	5
φ	Input radiation power	W	41
η	Emissivity of the detector material		6
μ_p	Hole mobility	$cm^2/V.s$	92
τ	Thermal time constant	s	41,46~48,58
ω	Angular modulation frequency of incident radiation	rad/s	5, 6
Δf	Noise equivalent bandwidth	Hz	6
ΔT	Temperature difference of the detector	K	48,50~53, 55, 60 ~ 63, 91
ΔT_b	Temperature difference between the target and the background	K	5
$\Re_v$	Responsivity	V/W	5, 6
A	Sensitive area of the detector	cm^2	6
B	Bandwidth	Hz	54
C_{ox}	Gate oxide capacitance per unit area	f/ cm^2	92
C_T	Electrical equivalent of thermal capacitance	f	42,44,46,50
D^*	Specific Detectivity	$cm\sqrt{Hz}/W$	6
G	Thermal conductance	W/K	6,42,41,46,48
H	Thermal capacitance	J/K	6,41,42,48, 61,62,91,92

Symbol	Description	Unit	Page No.
I_S	Saturation current of the bipolar device	A	105
k	Boltzmann's constant	J/K	54,106
P_{bias}	Bias heating power	W	41~45,48,60~62,91
P_{IR}	Infrared power absorbed by detector	W	41~45,52,55,60
q	Electron charge	C	106
R_T	Electrical equivalent of Thermal resistance	Ω	42,44,46,50
T	Temperature	K	41,42,54,105,106
V_{G0}	Bandgap voltage of the silicon at 0 ºK	V	105,106
V_{GS}, V_{DS}	Gate-source and drain-source voltage of transistor, respectively	V	92,98
V_T	Thermal voltage	V	105,106
V_{TH}	Threshold voltage	V	92
W, L	Width and length of the transistor, respectively	μm	67,92

List of Abbreviations

Abbreviation	Expansion	Page No.
ADC, or A/D	Analog to digital converter	31~33,72~74,77,85,87, 96,97,120,133,136,145 ,146,148
AMS	AustriaMicroSystems	72,92
CCBDI	Constant current buffered direct injection	30
CMOS	Complementary Metal-Oxide Semiconductor	7,8,18,28,63,64,92, 105,122,123,151, 153
CTIA	Capacitive transimpedance amplifier	28,29
DAC, or D/A	Digital to analog converter	32,34,72,73,85~88,102 ~105,107,113~117,119 ,121,133, 148,149
DAQ	Data acquisition	132~136,141,146
DI	Direct injection	27~30
DNL	Differential Nonlinearity	102,116,117
FPA	Focal plane array	3,9,11,12,14,17~21, 23,25,30~35,48,56,57, 70~73,76~79,85~ 88,95~99,118,119, 122~125,132~136, 140~147,151~155
FPN	Fixed pattern noise	31,32,36,57,66,72,79, 83~88,96~99,114, 117~122,133~136, 139,141~155
GBW	Gain bandwidth	79,80,83
IC	Integrated circuit	14,35,58,63,70,88
IME	Institute of Microelectronics	132
INL	Integral Nonlinearity	102,117
IR	Infrared	1~5,9,12,14~20,28,31 ~39,48~57,60~63,77, 85,88,91,93~96,118, 119,122,129~134,140, 146,147,152~155
JFET	Junction field effect transistor	25

Abbreviation	**Expansion**	**Page No.**
LSB	Least significant bit	104,107~109,113,119, 121,145,146,149,151, 154
NEP	Noise Equivalent Power	5,7
NETD	Noise Equivalent Temperature Difference	6,17,19,20,85
NMOS	N-channel Metal-Oxide Semiconductor transistor	64,67,71,95,107
PCB	Printed circuit board	129,132,134~138,147
PMOS	P-channel Metal-Oxide Semiconductor transistor	22,64,80,90,92,105, 109~113,121
PTAT	Proportional to absolute temperature	106
RMS	Root mean square	5
ROIC	Readout integrated circuits	9,12,14,19~22,31 ~34,39,70,71,87,95~ 98,122~125,129, 132~136,140~142, 144,146~148,151~155
SEM	Scanning electron microscope	125
SNR, or S/N	Signal-to-noise ratio	5,6,54,124,132,147
SPICE	Simulation program with integrated circuit emphasis	12,42,44~49,56,62, 92,153
SRAM	Static Random Access Memory	135,138,141,147,148
TCR	Temperature coefficient of resistance	6,7,17,43
VCVS	Voltage control voltage source	63
VLSI	Very large scale integration	62,63

Chapter 1. Introduction

1.1. Infrared detector

Infrared (IR), or "beyond the red", is the electromagnetic radiation similar to visible light but with longer wavelengths. The infrared portion of the electromagnetic spectrum lies adjacent to the visible[1]. Its wavelength range extents from 0.7μm, the red end of the visible light, to about 1000μm. While visible light is only emitted by objects at a very high temperature, infrared energy is radiated by all objects when the temperature of the object surface is above absolute zero. For example, at room temperature, the peak of the radiant emittance is about 10 μm which lies in the infrared region[2][3]. Hotter the object, more energy is radiated.

Although infrared radiation is invisible to the naked human eyes, it can be "seen" by infrared detectors. It gives us the possibility of measuring the self-emitted radiant energy from objects. When the infrared radiation is effectively detected, we can see all objects regardless of the darkness of the environment.

An infrared detector is basically a radiation transducer. It senses the incident infrared radiation with the changes in some of its electrical parameters. The infrared detectors can be roughly classified into two groups: photon and thermal detectors. The former absorbs the incident photons, which interact with the charge carriers in the detector and generates a photo-current or voltage, which produce the electrical output directly proportional to the number of input photons. The thermal detector responds to the

infrared power with a change in its temperature, which can be converted to either a voltage or current signal through a temperature sensing device.

The photon detector needs to be cooled down with a cryogenic system for efficient operation. However, most of thermal detectors are “uncooled”, which means that they can operate at room temperature. This enables uncooled detectors to have some advantages over the photon ones, such as affordability and reliability. These attractive characteristics encourage the development of the uncooled IR for a wide range of applications.

Since William Herschel first discovered the infrared energy beyond the visible region, the use of this portion of electromagnetic spectrum has aroused great interest among scientists. Modern infrared imaging system are lighter in weight and easier to use than those used decades ago[4][5]. They can sense the infrared radiant energy and generate useful electrical signal that is proportional to the temperature of the object surface. Therefore, clear thermal images can be produced for visual inspection. Nowadays, infrared technology is being widely adopted in many military, civilian, and scientific applications[6~8].

1.2. Microbolometer IR detector and focal plane array

There have been several types of uncooled IR detectors reported to date. Among them, microbolometer IR detector has been widely adopted in commercial products owing to its low cost and compatible process with silicon integrated circuits.

Microbolometer is a temperature sensor whose resistance is dependent on its temperature. A microbolometer based infrared detector consists of a resistive elements built on a thermally isolated structure, which is also act as infrared absorption layer. The incident infrared radiation is absorbed by the detector, causing its temperature to rise. The temperature change of the detector is sensed by the change in resistance. With the readout circuit, the resistance change is converted to a voltage or current signal as the output of the detector.

When used in the thermal imaging applications, microbolometer detectors are commonly arranged in a two-dimensional detector array, which is called the focal plane array (FPA). A FPA is a detector array placed at the focal plane of an optical system such as a camera, spectrometer or telescope. This detector array is combined with readout circuits or multiplexer which allows the electronic access to each detector cell in the array. Each detector in FPA represents a pixel of the final thermal image.

The operation of a microbolometer imaging system starts from the infrared incident absorption by the microbolometer FPA. Each detector cell senses the infrared energy radiated on it and changes its resistance accordingly. The readout electronics of the IR FPA sequentially addresses the detector cells (pixels) and convert the resistance change to an electrical signal, either in a voltage or a current. The signal from detectors is processed by the pre-amplifier and then analog-to-digital converter. After some imaging process programs such as filtering and enhancement, the digitized thermal image information can be obtained and stored in the video memory. Thus, a complete thermal image with the proper format and frame rate for TV display can be monitored.

The block diagram of a microbolometer IR imaging system is illustrated in the Fig.1.1. An example of a thermal image taken by the microbolometer based infrared camera is shown in the Fig.1.2, where a bright spot corresponds to the high temperature and a dark spot corresponds to the low temperature.

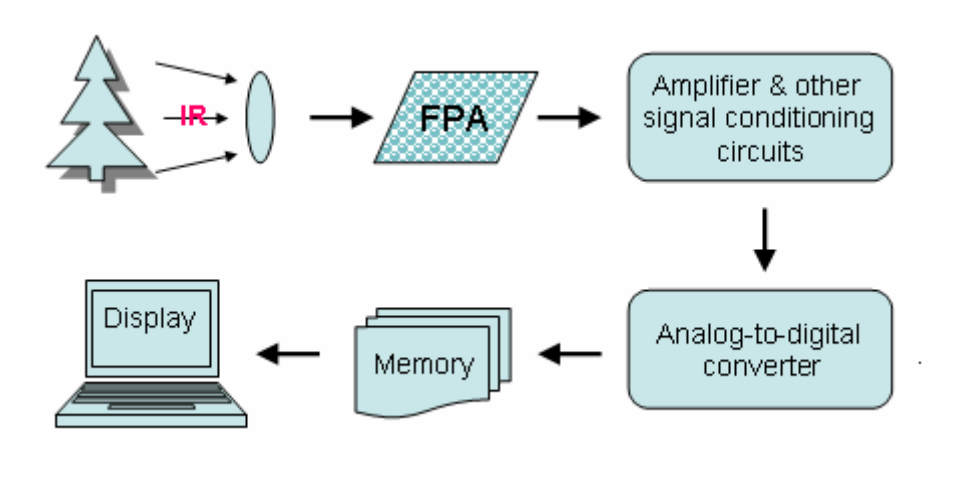


Fig.1.1. Block diagram of a bolometer infrared detection system.

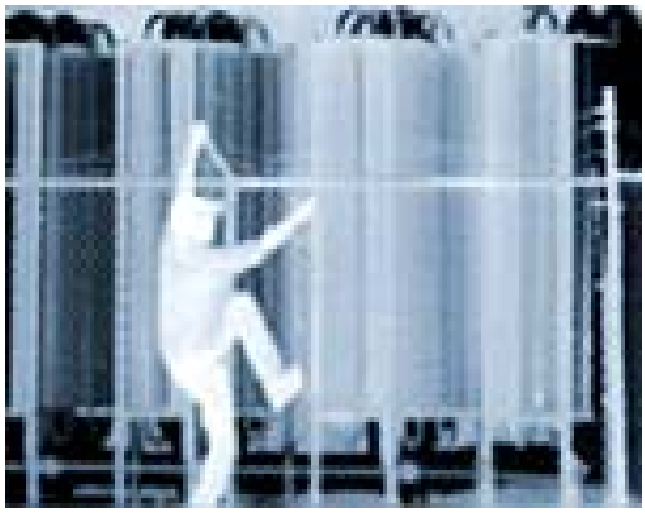


Fig.1.2. Thermal image taken by the uncooled infrared camera LTC550[9].

1.3. Detector characterization

In the study of thermal detector based systems, the following parameters are commonly used for characterizing the detectors.

- Responsivity:

The basic function of a detector is to convert input IR radiant power to an electrical output signal. The responsivity, as a measure of the conversion efficiency, is defined as the output signal per unit input IR power.

$$\Re_v = \frac{V_s}{\phi_e} \tag{1-1}$$

Where V_s is the detector output voltage and ϕ_e is the spectral incident power, which can normally be decomposed into a set of sinusoidal components as

$$\phi_e = \phi_{e,0} e^{j\omega t} \tag{1-2}$$

Ideally, the responsivity of the microbolometer detector is broad and flat with respect to the wavelength of input radiation.

- Noise Equivalent Power (NEP):

NEP is defined as the root mean square (RMS) incident radiant power required to produce an output signal V_s that is equal to the detector noise level V_n.

$$NEP = \frac{\phi_e}{V_s / V_n}. \tag{1-3}$$

In other words, the NEP determines the incident power for the detector to produce a signal-to-noise ratio (SNR) of unity. It is a measure of the ultimate sensitivity of a detector.

- Specific Detectivity (D^*):

The specific detectivity, D^*, which is the sensitivity normalized to the area of 1cm^2 and the noise equivalent bandwidth of 1Hz, is defined as

$$D^* = \frac{\sqrt{A\Delta f}}{NEP}, \tag{1-4}$$

where A is the sensitive area of the detector and Δf is the noise equivalent bandwidth.

- Noise Equivalent Temperature Difference (NETD):

NETD is defined as the smallest temperature difference between target and the background, which produces a signal to noise ratio (SNR) of unity.

$$NETD = \frac{\Delta T_b}{V_s / V_n} \tag{1-5}$$

ΔT_b is the temperature difference between the target and the background.

When a bridge readout circuit is used, the voltage responsivity of microbolometer can be expressed as

$$\Re_v = \frac{\alpha\eta \cdot V_{bias}}{4\left(G^2 + \omega^2 H^2\right)^{1/2}} \tag{1-6}$$

where α is the temperature coefficient of resistance (TCR), η is the emissivity of the detector material, G is the thermal conductance, H is the thermal capacitance of the microbolometer, ω is angular frequency of incident radiation. The TCR is defined as

$$\alpha = \frac{1}{R_d}\frac{dR_d}{dT_d} \tag{1-7}$$

where R_d and T_d are the resistance and temperature of the detector, respectively.

It can be seen from Eq.(1-6) that, to achieve high responsivity, a microbolometer with high TCR, high absorption coefficient and low thermal conductance is desirable. This is also true for obtaining low noise equivalent power (NEP) and high detectivity (D*).

Moreover, the responsivity of the bolometer has a low-pass feature. Although low thermal conductance can increase the responsivity, it reduces the bandwidth of the detector, and hence slows down the response of the microbolometer. Thus, compromise needs to be made in the detector design.

1.4. Structure of micromachined microbolometer

According to the Eq.(1-6) and Eq.(1-7), the thermal isolation between the microbolometer and the substrate is one of the important factors that contributes to high performance of the detector. With the development of silicon micromachining technology, structure with good thermal isolation can be easily realized. The compatibility of silicon micromachining technology with the standard CMOS process offers the possibility of combining the conventional CMOS readout integrated circuits with the microbolometer focal plane array.

There are two main types of micromachining (bulk and surface) commonly used for fabricating microbolometers. The structure of a microbolometer made by bulk micromachining is schematically shown in Fig. 1.3. An infrared absorber layer is formed by the dielectric layers, normally the composite of silicon oxide and silicon nitride. A meandering thin film resistor material is then deposited on the dielectric layer. The silicon under the dielectric membrane is etched away later in the process to form the gap between the microbolometer and substrate in order to reduce the thermal

mass and the thermal conductance. The resulting micromembrane is suspended above the silicon substrate and supported by the two legs connecting the detector to the readout circuits. The absorbed heat can only be dissipated through these two legs to the substrate that acts as a heat-sink.

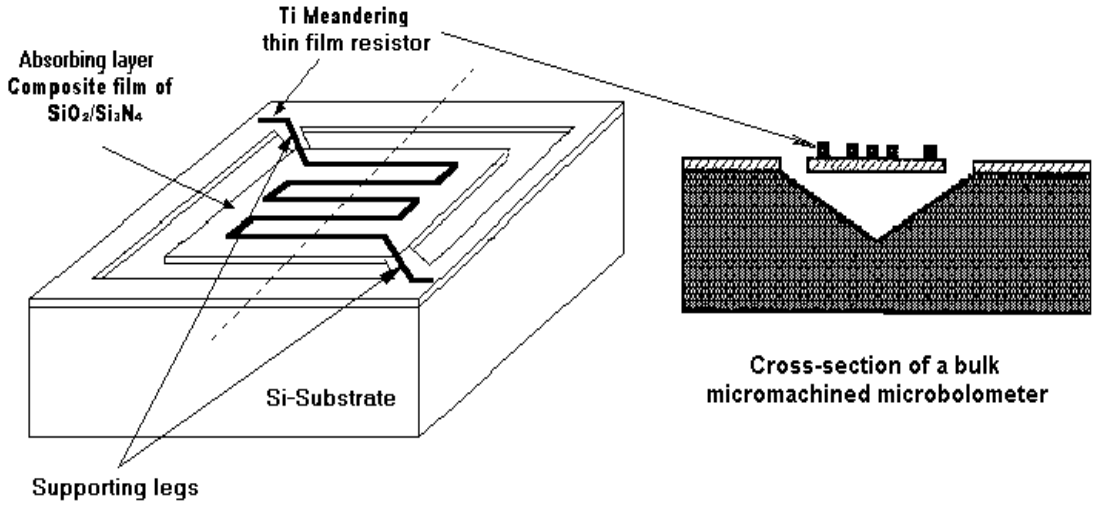


Fig. 1.3. Structure of a bulk micromachined bolometer.

In surface micromachining technology, a sacrificial silicon dioxide layer is deposited at the early stage of the processing. Then the microbolometer thin film is fabricated on the top of the sacrificial layer. The infrared absorbing layer, similar to that of the bulk micromachined structure, is made of Si_3N_4 during the CMOS process. Finally, the oxide sacrificial layer is removed with either wet or dry etching techniques. The free-standing microbolometer structure is then formed, as shown in Fig.1.4. After the sacrificial layer is removed, an air gap of 0.5 μm separates the micromembrane from the silicon substrate. The absorbed heat is dissipated to the substrate through the anchoring contacts.

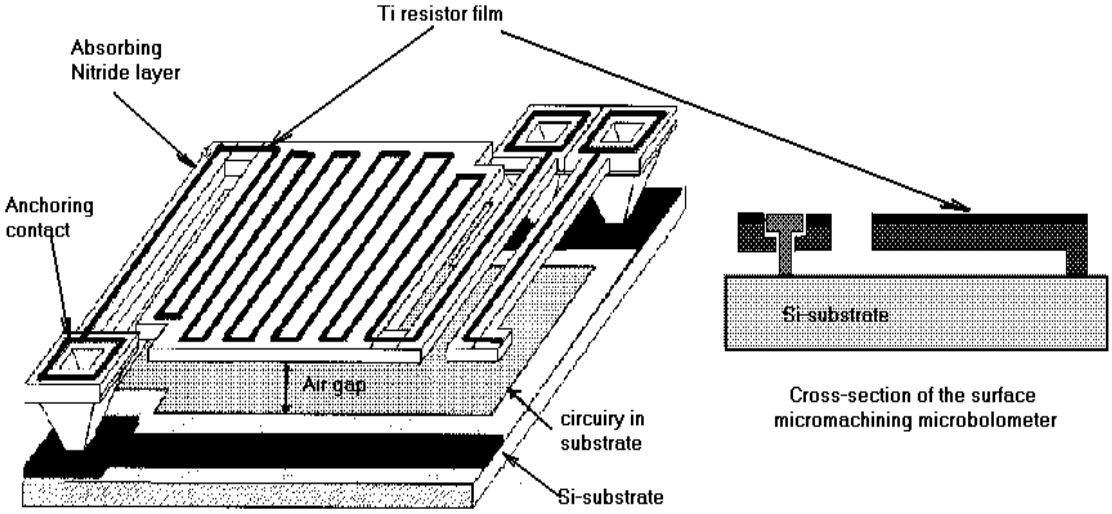


Fig.1.4. Microstructure of the surface micomachined microbolometer.

1.5. Readout circuits and self-heating effect

Besides the microbolometer detector itself, the readout integrated circuit (ROIC) is the next crucial part of the IR imaging system. It is an interface between the IR detector array and the thermal image display, where the signal and imaging process are carried out. The basic configuration of the readout circuit for microbolometer FPA is shown in Fig.1.5, where R_d is the microbolometer which is biased with a constant voltage V_{bias} through a load resistor, R_0. The IR radiation is sensed by R_d and a small voltage change ΔV_d is produced, and subsequently amplified by the preamplifier. The main shortcoming of this configuration is the large pedestal voltage V_d is also amplified such that it overrides the IR signal.

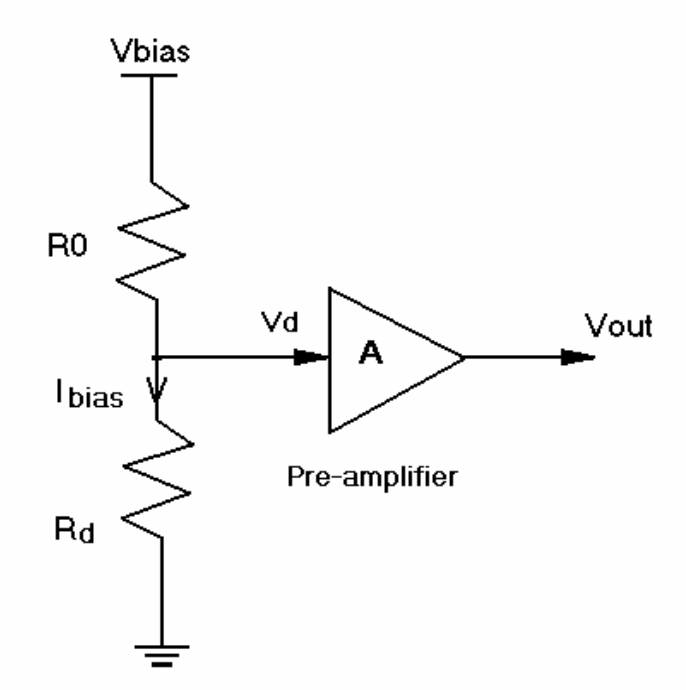


Fig.1.5. Basic readout circuit of the microbolometer.

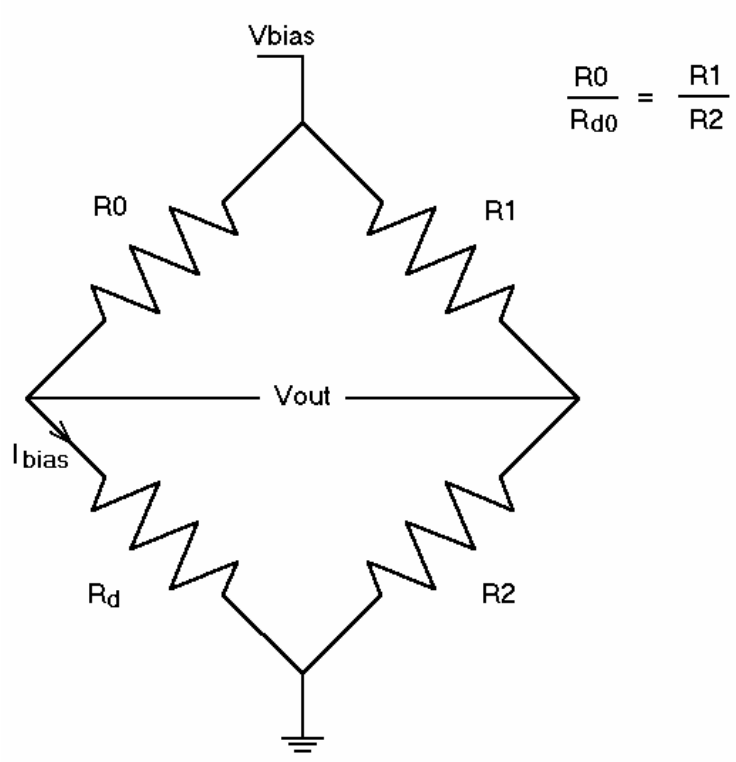


Fig.1.6. Wheatstone bridge readout circuit of the microbolometer.

Most practical readout circuits employ the Wheatstone bridge structure[10], as shown in Fig.1.6. When the ratio of the resistor R_0 over the room temperature resistance of the microbolometer, R_{d0}, is equal to that of resistor R_1 over R_2, the bridge is balanced. Such a bridge structure not only removes the pedestal bias voltage, but also rejects the fluctuation and other noise introduced by the power supply.

However, the Wheatstone readout circuit also has its shortcomings, such as self-heating effect. During the readout, in order to monitor the amount of the resistance change, the microbolometer element must be electrically biased. When there is a current flowing through the bolometer, it generates the Joule heating. As a result, the microbolometer is not only heated by the infrared radiant energy, but also the bias current flowing through. This heating effect due to the bias current is referred to as the self-heating of the microbolometer. Because of the micromachined structure, thermal conductance of the bolometer is greatly reduced. Hence the heat generated by the self-heating effect cannot be quickly dissipated through the thermal conduction to the substrate. This makes the temperature change of the microbolometer due to the self-heating effect much greater than that due to the input infrared radiation. Thus, the self-heating effect must be compensated in the readout circuits.

1.6. Scope and organization of thesis

Several microbolometer based IR focal plane detector arrays have been reported. However, very little information is available on their readout electronics, especially on self-heating cancellation. An in-house microbolometer focal plane array was developed by previous students. However, its performance suffers from the problems

in its ROIC, in particular, the self-heating effect, as it was not dealt with in the ROIC. The scope of this project is to develop a simple and yet effective method or circuit for the self-heating cancellation and employ it in the ROIC for the microbolometer focal plane array made in house. The overall objective was to develop a prototype ROIC for the above mentioned microbolometer focal plane array that can compensate both self-heating and fixed pattern noise.

The organization of the thesis is as follows:

Chapter 2 presents the literature review of the infrared imaging system and readout electronics for microbolometer focal plane array.

In chapter 3, a SPICE Electro-thermal model of the bolometer is introduced. The effectiveness of this model is demonstrated by the comparison between the simulation and the experimental results. The analysis of the thermal behaviours of the microbolometer is studied based on the proposed SPICE model.

In chapter 4, the design of the voltage-mode readout integrated circuits for microbolometer FPA is presented. A new self-heating cancellation scheme is proposed and the detailed description of the circuit operation is given. The proposed self-heating cancellation scheme is employed in a voltage-mode ROIC, in which the fixed pattern noise cancellation circuit is also included. Finally, the simulation results are presented.

Chapter 5 focuses on the design of the current-mode readout electronics for the microbolometer IR focal plane array readout circuit. The self-heating cancellation

scheme described in chapter 4 is extended to the current-mode realization. The design and simulation results are presented.

Chapter 6 deals with test and evaluation of the voltage- and current-mode readout circuits. Finally, chapter 7 gives the conclusions of this research and suggestions for the future work.

Chapter 2. Literature Review

Over a century after the infrared is discovered, the first IR imaging system circa-1930 Evaporagraph [11] was produced. It was a rather insensitive non-scanning system which could not satisfied most tasks. Since then, rapid advances have been made in thermal imaging systems. Today, the sophisticated thermal imaging systems are used in many commercial, industrial and military applications [12][13]. The ever-expanding field of applications of IR imaging systems is a primary motivation for the worldwide efforts in the research and development of infrared technology.

Infrared detectors and readout integrated circuits (ROIC) are the two important aspects of thermal imaging systems. In late 1970s, the first generation IR focal plane arrays incorporating the IC technology were developed [14][15]. The readout integrated circuits for these IR FPA were simple multiplexers and consist of little, if any, signal conditioning circuits. Due to the significant system performance enhancements allowed by the integrated circuits, ROICs for IR imaging systems become more and more complex. The available on-ROIC or on-FPA functionality has increased dramatically. The advance in modern microelectronic technologies has provided the potential to realize cost-effective and high performance IR imaging systems.

2.1. Infrared detectors for thermal imaging

IR detectors are generally classified into two categories, namely, photon and thermal IR detectors. Photon detectors absorb the IR radiation by interaction with electrons within the material. When an electron gains enough energy from the incident IR radiation (or photons), it overcomes the energy gap and becomes a free electron that alters the electrical parameters of the material, such as conductivity. Thus, the responsivity of the photon detector depends on the wavelength of the IR radiation, as the incident photon energy is a function of the wavelength. For a detector material with a fixed energy gap, when the wavelength of the incident IR radiation is beyond certain value, the photon energy will not be high enough to excite the electrons to over the energy band gap. The detector will fail to response. This is often referred to as "long wavelength limit" of the IR photon detectors. The major advantages of the photon detector are its good sensitivity and fast response[16][17]. However, in order to achieve this, the cryogenic cooling operation is required, which makes the semiconductor photon detectors bulky, heavy and inconvenient to use, as well as costly. Thus the applications of the photon IR detectors are mainly in the high-performance thermal imaging system or cameras[18~23].

Thermal IR detectors, on the other hand, absorb the IR radiant power resulting in the change of its temperature. This temperature change is converted to an electrical output through a temperature sensing device. Thermal effects are generally wavelength independent. The spectral band of thermal detectors is normally determined by optics and windows. Thus, a broad or flat spectral response can be expected. Since the room temperature object emits the highest radiant power in 8-14μm range, thermal detectors are generally used as long wavelength IR detector.

In comparison with photon detectors, thermal detectors are characterized by modest sensitivity and slow response. However, the thermal detectors are typically operated at the room temperature, making them low-cost and convenient to use. The thermal IR detectors are often referred to as uncooled IR detectors. Uncooled IR detector technology has advanced rapidly in the past decade and results dramatic improvement in the performance of uncooled thermal imaging systems [24][25]. The crucial technology to fabricate uncooled detectors is the micromachining technology. It enables the realization of miniaturized thermal isolated structure and increases the detector sensitivity and response speed[26~29]. The most common uncooled thermal detectors are microbolometer[30~33] and ferroelectric IR detectors[34~39].

As the microbolometer IR detector will be used in this study, the remaining of this chapter briefly reviews microbolometer IR detectors and its readout electronics.

2.2. Microbolometer

Microbolometer detector is one of the promising thermal IR detectors. When exposed to IR energy, the microbolometer detector heats up and its electrical resistance changes in response to the absorbed IR energy. The resistance change can be measured by applying an electrical bias to the detector and readout the changes in voltage or current.

2.2.1. Microbolometer IR detectors

One of the successful commercialized microbolometer materials is vanadium oxide[40~42], VOx, which was developed originally at Honeywell. It usually has the

high temperature coefficient of resistance (TCR) of above - 2%/K[43]. The measured thermal capacitance of VO_2 detectors is about 10^{-9} J/K corresponding to a thermal time constant of 10 ms. The responsivity of 250 kV/W has been observed with a 50μm-square pixel (detector) in response to 300K blackbody radiation[44][45]. One of the drawbacks of VOx microbolometer is its non-crystalline structure which results in large 1/f noises. Low NETD of 30 mK and D* of about 10^8 $cmHz^{1/2}/W$ have been achieved for micromachined VOx microbolometers[46][47].

Metal film microbolometers, used in this study, have a positive TCR of about 0.3%/K. Such devices normally have the detectivities in the order of 1×10^8 $cmHz^{1/2}/W$ under room temperature operation [14]. They have comparatively low temperature coefficient, but low noise and high lone-term stability in comparison with vanadium oxide detectors[16]. Titanium is one of the metal materials used for microbolometers, and reported to have the NETD of around 0.07K with f/1 optics and the TCR of about 0.25%/K to 0.35%/K [48][49]. Double sacrificial layer surface micromachining technology used to fabricate Ti microbolomerter further improves the fill-factor of the FPA to around 92%[50][51]. The thermal isolation effect can also be enhanced by the technique of supporting the absorbent membrane with a lower layer, which is anchored to the substrate. The detectivity of 2.43×10^9 $cmHz^{1/2}/W$ was reported with Ti microbolometer [50]. In spite of its low TCR, titanium has been successfully employed in commercial IR FPAs.

Amorphous silicon (a-Si) is another high TCR microbolometer material. With resistivity of up to 10^5 Ωcm, the TCR of a-Si:N can be as high as 6%/K. However, high noise is observed. While at low resistivity (10^3 Ωcm), TCR reduces to around

2.5%/K[52]. High performance of the amorphous silicon microbolometer have been achieved in many investigations that show a-Si is becoming an advantageous choice for uncooled IR detector material[53~57].

YBaCuO is a well kown material for superconducting bolometers[58][59]. However, its possible operation at room temperature has been widely studied recently[60][61]. YBaCuO bolometers also demonstrate a low 1/f noise and low power-normalized corner frequency, f_c/I^2R, where f_c corresponds to the point of the frequency spectrum at which the voltage of the current noise equals the voltage of the Johnson noise[60][62]. The detectivity of 1×10^8 $cmHz^{1/2}/W$ was obtained with a thermal time constant of 5 ms.

There are several other bolometer materials that have been studied, such as the polycrystalline Si-Ge[63~65], P-N junction diode[66~68] and single crystal silicon N-well in the standard CMOS process[69][70]. The reported detectivities for these materials are 2.3×10^8 $cmHz^{1/2}/W$[63], 1.2×10^{10} $cmHz^{1/2}/W$[68] and 1.2×10^9 $cmHz^{1/2}/W$[69] respectively.

2.2.2. Microbolometer focal plane array

There are two main architectures used for developing IR focal plane arrays, namely, the hybrid and monolithic, as shown in the Fig.2.1. Hybrid microbolometer FPAs compound the detector arrays with the silicon readout chip via some chip-to-chip bonding techniques, such as indium bumps or loopholes, while in monolithic structure, detector arrays are fabricated on-chip with the readout circuits.

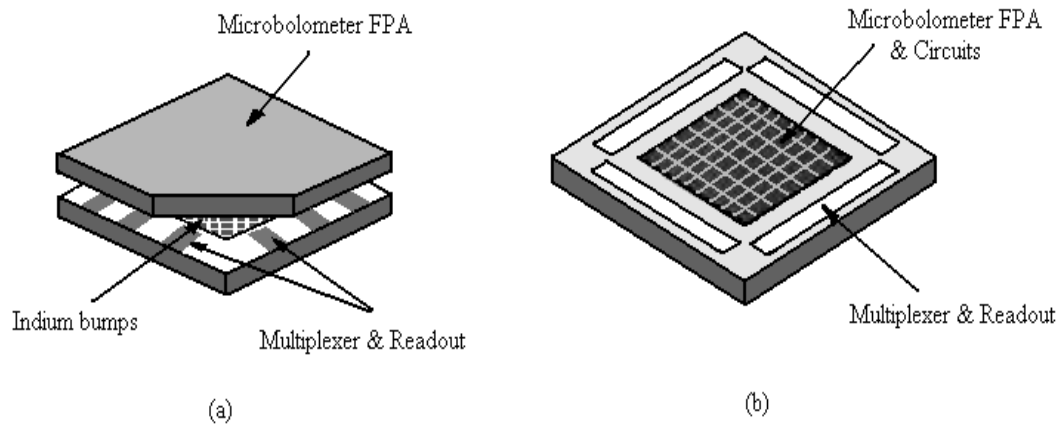


Fig. 2.1. Flip-chip-hybrid (a) and monolithic (b) structures of microbolometer FPA[71]

In the hybrid design, the microbolometer detector FPA and readout circuits are fabricated on different substrates, and bonded together through indium bump or loophole interconnection. The indium columns form both the electrical connection between detector and signal processor, and a thermal conduction path to the silicon. The thermal conduction must be minimized to maximize the temperature differential across the detector and achieve high sensitivity[72][73]. Since the detector array is on a separate chip from the one for the circuits, it can be optimized independently of the readout circuit. A high fill factor near 100% can be achieved[17]. Hybrid structure is used primarily when the processes of detector and ROIC are not compatible or there are some cost issues if fabricated both together. Hybrid uncooled microbolometer FPAs with NETD in the range of 300mK have been reported[74][75].

Modern two-dimenstional microbolometer FPAs employed in IR imaging system usually have large number of pixels so that individual lead-outs from each pixel are impractical. Thus, a monolithic structure with the control circuit fabricated in the underlying silicon has been developed. In the monolithic design, the detectors are fabricated on a thermally isolation structure on the same silicon substrate where the

ROIC is. The monolithic thermal isolation structure typically provides a lower thermal conduction than that of the indium columns in the hybrid FPAs. Monolithic FPAs with the readout circuits on the same chip is the preferred choice for microbolometer infrared FPAs as the direct on-chip electrical connection results in the simplified package, improved performance and high reliability[76~78].

One of early studies of the fully monolithic micromachined bolometer FPA, with simple on-chip readout circuits and preamplifier, was reported in 1993[44]. No signal processing circuit was integrated on this chip. However, because of the improvement of the filling factor and the reliability in the monolithic IR FPA, the monolithic FPA technique has been widely employed and studied in the last decade [79~81]. IR imaging FPAs with various dimensions from 128 × 128 to 640 × 480 pixels have been reported[82~91]. The NETD for most of these FPAs have attained around 100mK, with the best performance being less than 20 mK[84].

2.3. Readout electronics for microbolometer FPAs

The basic functions of the readout electronics for microbolometer FPAs typically include the bias for the microbolometer, front-end amplification and signal conditioning, pixel addressing, digitization, and error correction circuits. The block diagram of a ROIC operated in serial pixel addressing mode is shown in Fig.2.2. The pixels in the array are read out serially through the pixel addressing circuits that consists of the column switches, x (column) and y (row) shifter registers. Clock generator generates all the control and clock signal needed in multiplexer circuits and signal processing circuits. The signal is amplified and further processed by signal

conditioning circuits. The output from the signal conditioning circuit is digitized and sent to the off-chip circuitry for further processing and producing the standard video display.

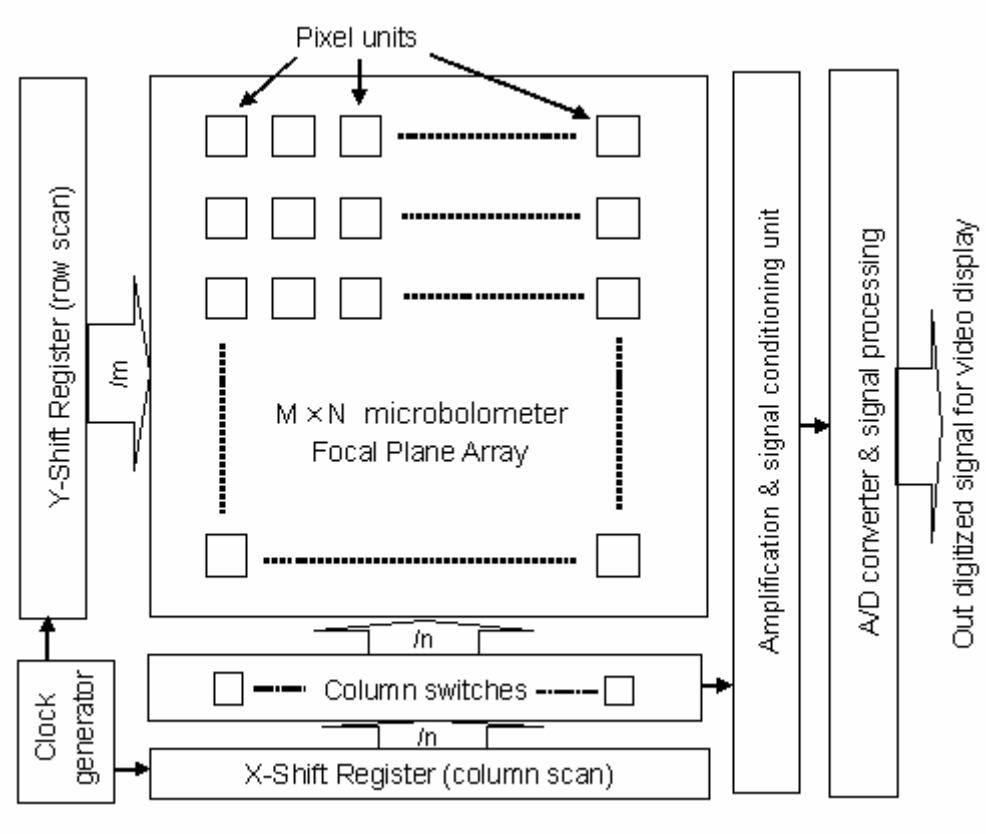


Fig. 2.2. Block diagram of the ROIC for an M × N-pixel microbolometer FPA.

2.3.1. Front-end signal conditioning circuits

The microbolometer is in essence a temperature sensing resistor whose resistance changes with its temperature. The change of the resistance can be read out as a voltage or a current. Thus the front-end signal conditioning circuit can be classified as voltage- or current-mode. Since the signal from the bolometer is normally very

weak, the front-end signal conditioning circuit is critical to the performance of the ROIC.

2.3.1.1. Voltage-mode front-end readout circuits

The simplest voltage-mode readout method is to connect the microbolometer to a bias resistor serially, as shown in Fig. 2.3(a). The problem in this solution is that the bias resistor damps the signal. To avoid this, an active bias scheme with high bias voltage was proposed in [92], as given in Fig. 2.3(b), where the bolometer is connected to the source of a PMOS transistor and the output signal is taken from its drain with the bias resistor as a load. Large PMOS transistor should be used to avoid the significant 1/f noise.

To overcome the problem of high 1/f noise from the active device, a modified the passive biasing circuit with a non-overlapping chopper amplifier was reported in [93], which is shown in the Fig.2.4. The chopping amplifier is worked as modulation circuit, which modulate the signal to a higher frequency band so that the DC and low frequency measurements can be avoided. Hence, the matching requirement between bolometer resistances is eliminated and greatly reduces the 1/f noise. The offset caused by the mismatch among the pixels (also referred to as the fixed pattern noise) can be pre-corrected by providing a suitable chopper reference to each pixel with a digital-to-analog converter, as indicated in the dash line.

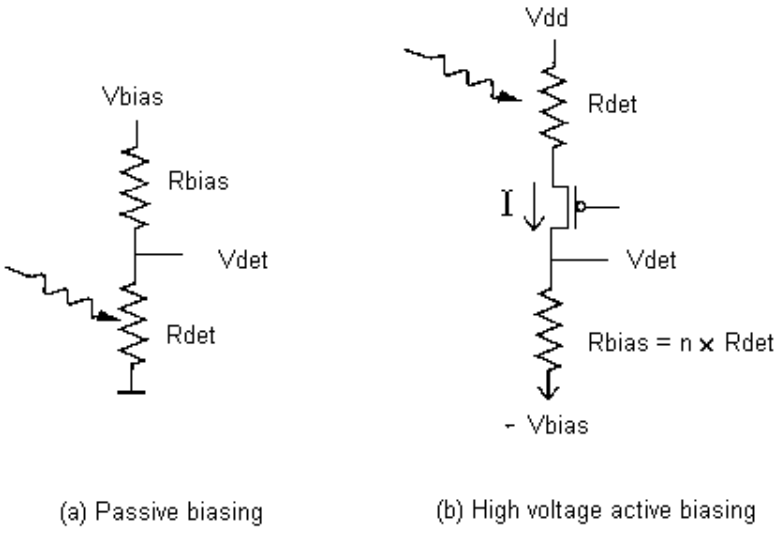


Fig. 2.3. Two simplest voltage-mode readout circuits

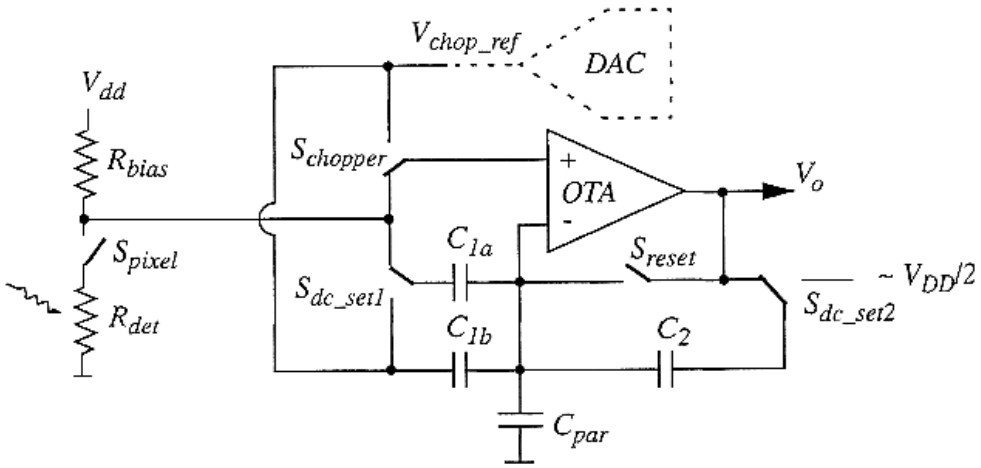


Fig. 2.4. Chopper-amplifier voltage-mode circuit

The Wheatstone bridge structure is the most commonly used voltage-mode readout scheme for microbolometer FPAs[94][95]. The advantage of this readout circuit is that the common-mode signal can be removed by a differential amplifier. Either a constant or pulse bias can be employed.

Fig.2.5 shows a Wheatstone bridge circuit with an AC bias voltage[96][97]. The AC bias can be either a sinusoidal or a square wave voltage with zero DC level. The frequency of the bias voltage is much higher than the thermal rolling-off frequency of the bolometer, $1/2\tau$, to provide a modulated signal for amplification. A lock-in amplifier provides the phase sensitive detection after the output of the bridge circuit is amplified, producing a DC output voltage proportional to the resistance difference between bolometer 1 and 2. If the two bolometers in the bridge are perfectly matched, the 1/f noise from the amplifiers and source-followers are eliminated by the phase sensitive detection.

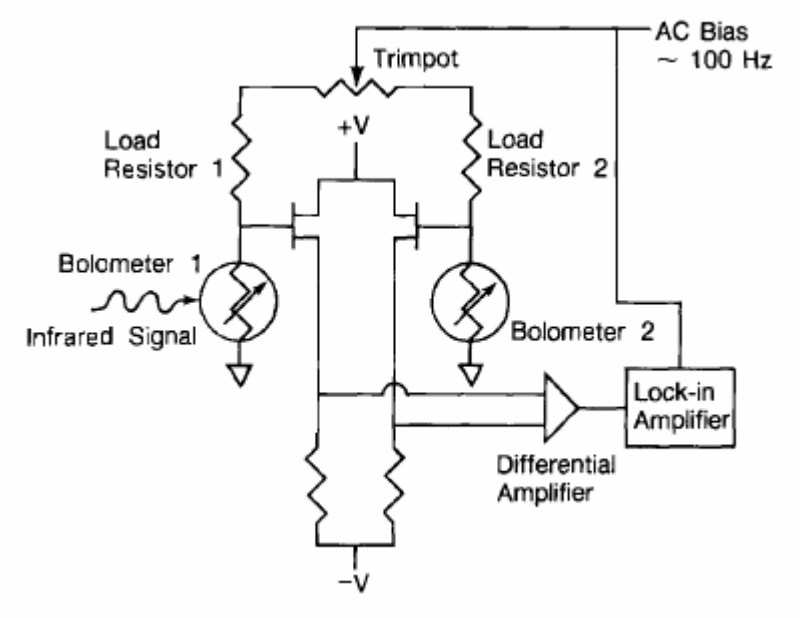


Fig. 2.5. AC-bias bridge readout circuit for bolometer

A bridge readout circuit with a capacitive load shown in Fig. 2.6 was presented in [98]. The load capacitor is polarized by a triangular wave voltage, which produces a square wave current. This triangular voltage is built from the square voltage, which biases the bolometer, through an active integrator using pre-amplifier. The main advantage of this circuit is that the use of capacitive load enables the circuit free of Johnson noise and decreases the spikes form the high frequency bias. The bias

parameters, such as amplitude of the bias voltage, intensity of the bias current and the slope of the bias voltage in each half period etc., are digitally controllable to obtain the best sensitivity and bridge equilibrium. Moreover, the high frequency AC bias separates the signal from the low frequency noise of JFET devices, such as the 1/f noise, through modulation and demodulation.

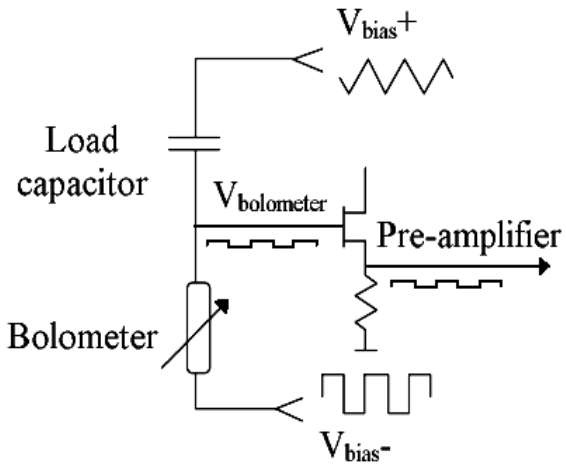


Fig. 2.6. Bridge readout circuit with capacitive load

2.3.1.2. Current-mode front-end readout circuits

In the current mode readout, the output signal is the current from the bolometer. This current is normally integrated and converted to a voltage at the output of the integrator. The integration also removes out-of-band high frequency noise. It is preferred in some applications for its high sensitivity and good noise immunity[99~101]. A simple current-mode readout circuit for titanium bolometer FPA was employed in Ref.[48]. MOS transmission gates are used for pixel select switches to reduce the on resistance, as shown in Fig. 2.7.

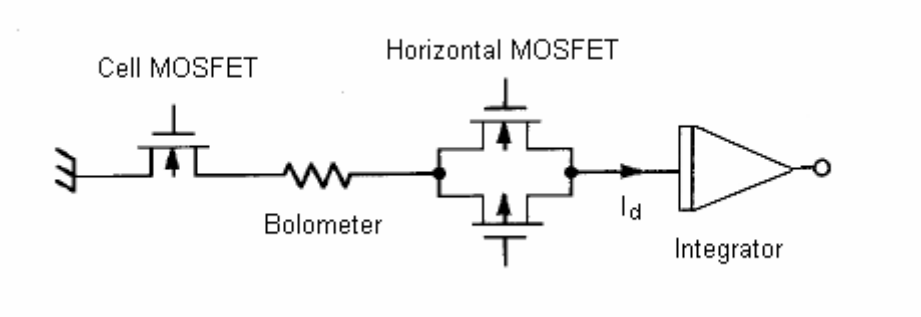


Fig. 2.7. A simple current-mode readout for microbolometer

In another current mode readout scheme[100], a pulse current bias is employed. The bias scheme and the pixel amplifier circuit is shown in the Fig. 2.8. With signal *sel_i*, the bias current is generated from the current source that consists of M_3, M_{bias} and R_{bias}. When signal *selref* is pulse low, the V_{ref} is sampled on C_2 and output of pixel amplifier is given as:

$$V_0 = V_{ref} - |H(0)|(V_{ref} - V_{bol}) \tag{2-1}$$

where $H(0)$ is the DC gain of the pixel amplifier and V_{bol} is the voltage drop across the bolometer. When the signal *selref* is kept to high, signals *phi* and $\overline{phi}$ enable the signal from one pixel be stored on C_2 and act as V_{ref} when readout the next pixel. Thus, the signal difference between two consecutive pixels can be enhanced by the amplifier. With this scheme, the voltage drop on the microbolometer can be continuously measured and a high dynamic range can be achieved. Another advantage of such circuit architecture is that it "allows accommodation of the large signal swings due to the self-heating effect" with the high dynamic range of the circuit.

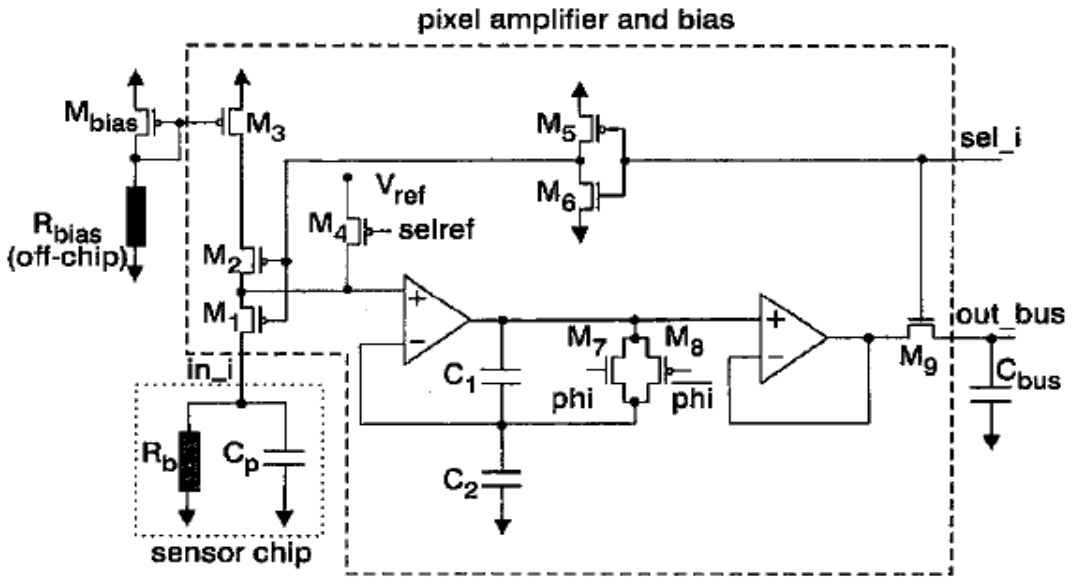


Fig. 2.8. Pixel amplifier and pulse current bias circuits

Another commonly used current-mode readout technique is the direct injection (DI) circuit [102][103], which is illustrated in Fig.2.9. When it is used in the microbolomter readout circuit, the unit cell consists of a direct injection input buffer MOS transistor, M_b, which is used to bias and sense the current from microbolometer, and an output source follower to provides a voltage-mode output [104]. The integration begins with resetting the voltage of the integration capacitor to a bias voltage. Then a current flows from the integration capacitor to bolometer. The voltage drop on capacitor is monitored and amplified. The injection efficiency of a DI readout circuit is defined as the ratio of the current flowing into the readout circuit to the current from microbolometer. Thus, the input resistance of the buffer MOS transistor should be lowered in order to obtain the high injection efficiency and better detectivity.

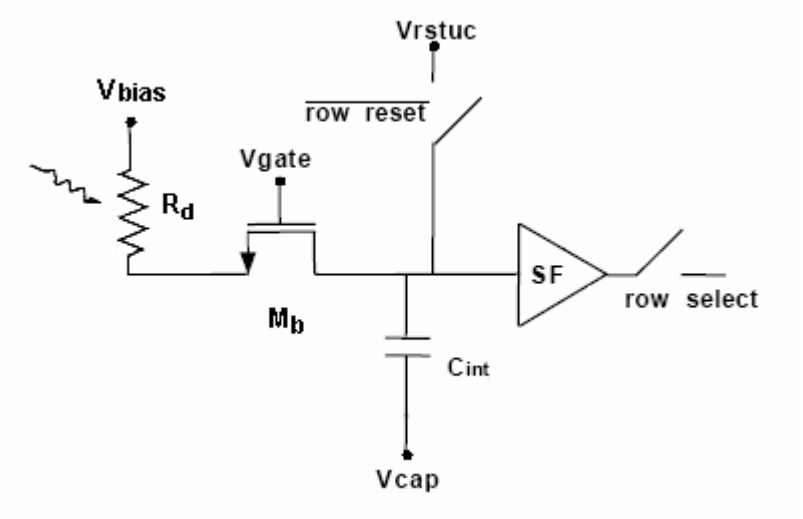


Fig. 2.9. Direct injection circuit

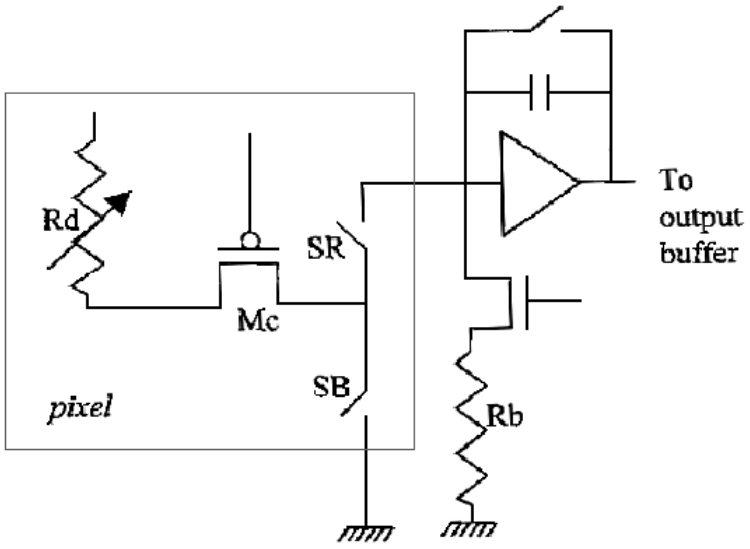


Fig. 2.10. Direct injection circuit with CTIA integrator.

A CMOS readout circuit based on the DI input stage was reported in [54], where a capacitive transimpedance amplifier (CTIA) was used to integrate the current signal, as shown in Fig. 2.10. The readout is performed when switch SR is closed. R_b is a blind bolometer which is not subject to the IR radiation and used to suppress the background current. One R_b is required for each column. Thus, only the IR induced

signal current is integrated by the CTIA. Similar circuit is also implemented using switched capacitor circuit[105].

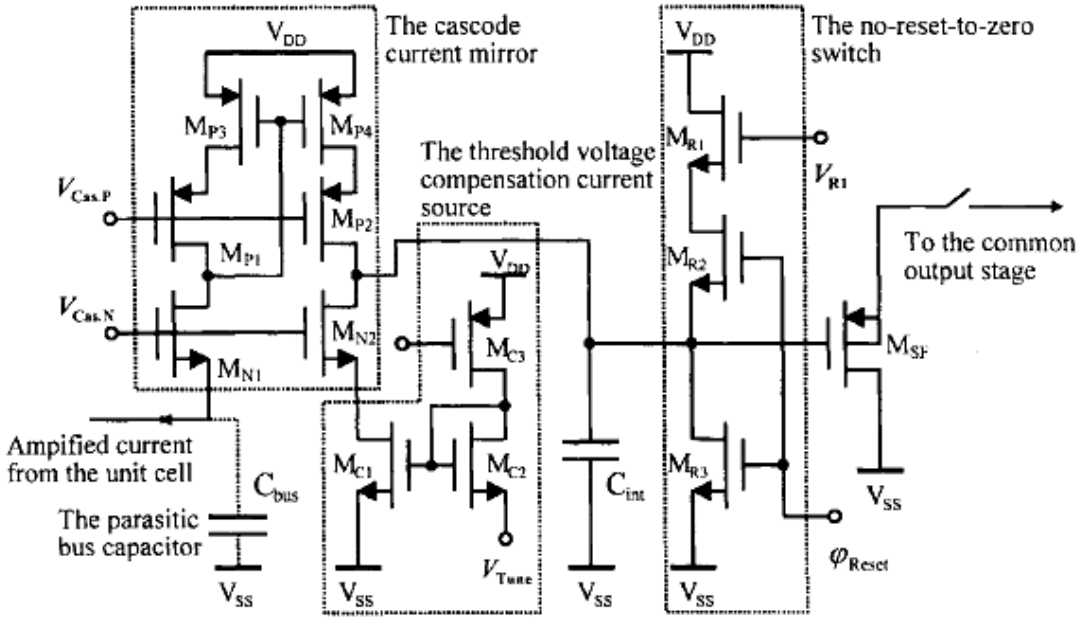


Fig. 2.11. Shared integration cell with current-mode background suppression.

The output current of DI circuits contain the large background current, which is the bias current flowing through the microbolometer. This will significantly degrade the circuit dynamic range and readout performance. More recently, current-mode background suppression circuits, as shown in Fig. 2.11, have been reported[106][107]. The current from unit cell is mirrored through a cascade current mirror. The threshold-voltage compensated current source generates a tunable background current. Thus, current from unit cell is subtracted by a DC background current before it is integrated on the capacitor, C_{int}. When using the small biasing current and large transconductance for transistors M_{C1} and M_{C2}, the drain current of M_{C1} can be nearly independent of MOS threshold voltage[108]. Therefore, the shared-integration cell,

which can be incorporated into DI circuits, provides the background current compensation and good immunity of the threshold-voltage non-uniformity.

A constant current buffered direct injection (CCBDI) readout circuit was demonstrated with a 64 × 64 FPA [99]. The bolometer is biased with a constant current source, I_{cc}. A transconductance amplifier (Gm) is used to transfer the voltage out of the constant-current biasing readout to the current output, and an inverting amplifier connected between the gate of the buffer transistor and the output from the microbolometer detector. The formed negative feedback structure can decrease the input resistance of the buffer transistor by a factor of A, the open-loop gain of the amplifier. The unit cell circuit with the CCBDI readout is plotted in Fig.2.12. The shared-integration background suppression circuit was incorporated to the BDI structure and provided background suppression and the compensation of the threshold-voltage variations. Thus, both linearity and offset of the CCBDI circuit are improved.

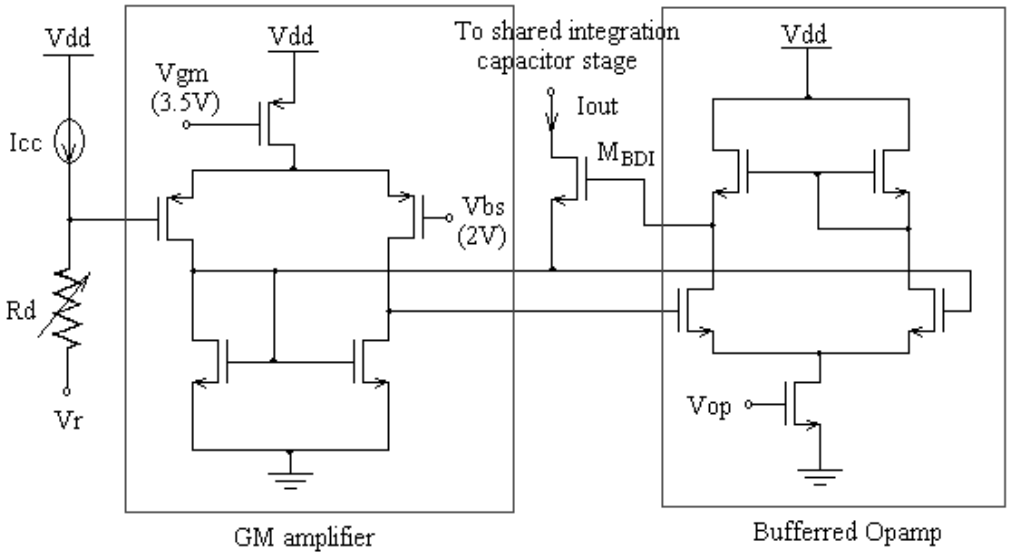


Fig. 2.12. CCBDI readout circuit

2.3.1.3. Other front-end readout circuits

A pixel-wised A/D converter concept was first proposed in [109] and the following research is reported in [110]. The idea is to digitize the signal at early stage and increase the noise immunity. The readout circuit is essentially a RC oscillator with R (R_d) being the microbolometer. The IR induced resistance change of the microbolometer is converted to frequency. Thus, the frequency of the output signal is proportional to the incident IR radiation, and the analog signal from the microbolometer is digitized. The subsequent oscillation frequency detection circuit uses a observing window and counts the number of pulses in the window[111].

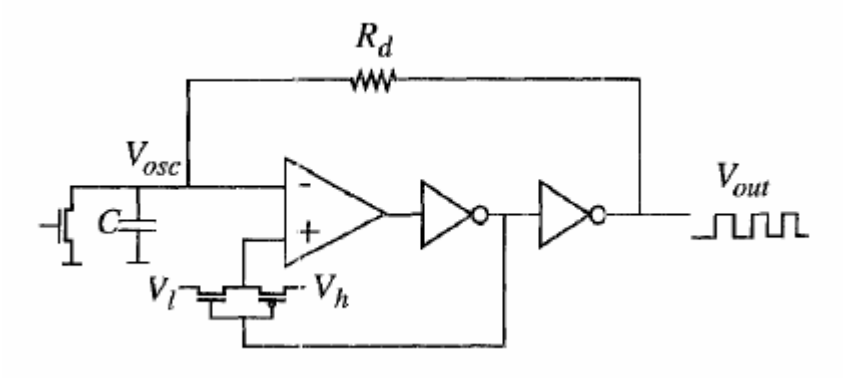


Fig. 2.13. Pixel-wised A/D converter circuit

2.3.2. On-chip non-uniformity correction

Non-uniformity (pixel offset) is one of the important performance limits for the IR FPA ROICs. It may be either due to mask, lithography or other processing variables. In a large focal plane array, the non-uniformity from pixel to pixel, which produces the fixed pattern noise (FPN) in the output thermal images, could be very significant.

The fixed pattern noise correction circuit is therefore an important part of the readout electronics.

The most common FPN cancellation circuit uses the on-chip analog to digital converter (ADC) to digitize the FPN and store the data into some off-chip memories. When in real infrared imaging acquisition operation, the stored FPN data is read by the on-chip digital to analog converters (DAC) and fed back into ROIC. Then ROIC subtracts the FPN from the normal output signal pixel by pixel. Due to the large silicon area required for high order ADC, most of the pixel-by-pixel input offset correction circuits have only 6-bit[112] to 8-bit[113] resolutions. Therefore, the on-chip circuit can only perform coarse correction and an off-chip cancellation is normally required for the fine correction.

The on-chip 6-bit pixel-by-pixel FPN correction circuit with on-chip 14-bit ADC has been reported[112]. The ROIC obtains the measured instantaneous dynamic range of more than 76 dB at a 6.1 MHz output data rate and 60 Hz frame rate. The power consumption is less than 500 mW. Two-point non-uniformity correction is performed by the off-chip electronics.

As far as thermal image quality is concerned, high-accuracy on-chip ADC and DAC are preferred for the on-chip correction of FPNs. Delta-Sigma A/D converter is seen as a candidate to achieve high resolution without much increase in its complexity. A second-order multiplexed oversampling Delta-Sigma A/D converter was proposed for FPN correction in the IR FPAs [114][115]. Results from experiments showed the accuracy better than 12 bits could be achieved in prototype ROICs.

Since the high order Delta-Sigma A/D converter requires the very high sampling rate, a 16-bit on-chip A/D converter with two operation modes is shown in Fig. 2.14 [116]. One 8-bit resetable Delta-Sigma converter used to obtain the most significant bits is combined with one 8-bit conventional successive approximation A/D for residual voltage conversion to achieve 16-bit resolution. High linearity is obtained by the first-order Delta-Sigma converter, while speed and resolution are enhanced by the successive approximation conversion circuit.

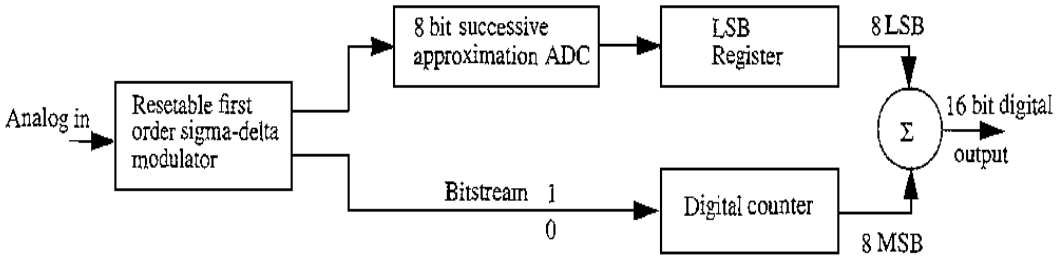


Fig. 2.14. Block diagram of the two-mode 16-bit A/D converter

2.2.3. Other on-chip functions

Besides on-chip offset correction, most uncooled IR FPAs integrate the gain control and temperature stabilizer circuits on ROICs [31,84,117]. On-chip temperature-induced offset compensation schemes using thermally shorted bolometers, as shown in Fig. 2.15, were reported in [118] and [119]. The thermally shorted microbolometers or the "compensation elements" have the same temperature coefficient as the active detectors, but are not thermally isolated or thermally shorted. Thus there is no opaque cover needed for these compensation elements. A supply adjustment configuration to vary the microbolometer bias for different units is

implemented by a digital-to-analog converter that adjusts the source potential of the common gate amplifier. A transimpedance amplifier is used for integration and amplification of the signal.

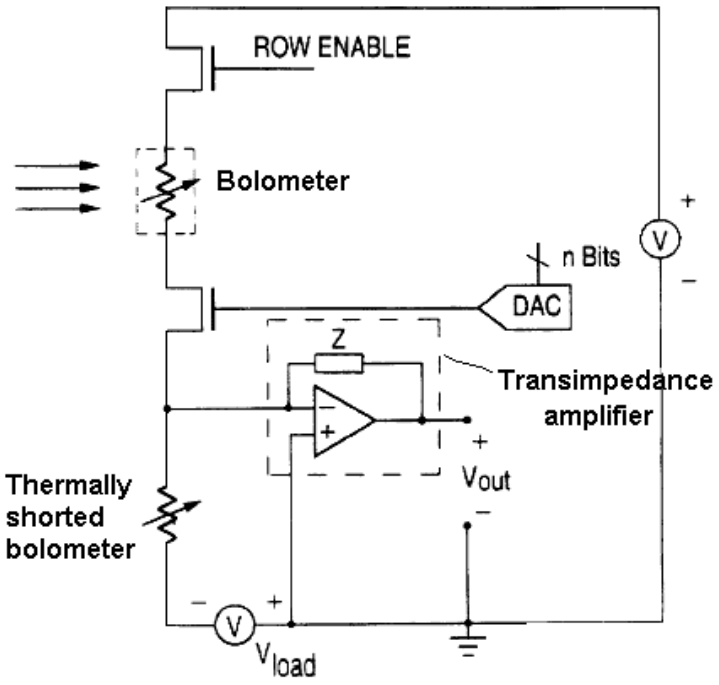


Fig. 2.15. Method for correction for temperature-induced non-uniformities with thermally shorted microbolometer elements

An on-chip bias regulator has been reported to be integrated with uncooled IR FPA, providing the bias drift rejection[120]. It was claimed that the bias regulator can achieve better than 100:1 drift rejection from an external 5.5 V supply.

Another bias equalization method was presented in [121]. It can provide a unique bias to each microbolometer element, so that allows the control of the non-uniformity over a wider range of ROIC substrate temperatures. As shown in the Fig. 2.16, an n-bit DAC supply the bias voltage to the microbolometer through a unit cell enable

switch. Thus, other than a conventional two-point correction, offset and gain correction, a three-point correction process was integrated on-chip for better signal conditioning. This approach was expected to allow the removal of the temperature stabilizer for the microbolometer arrays.

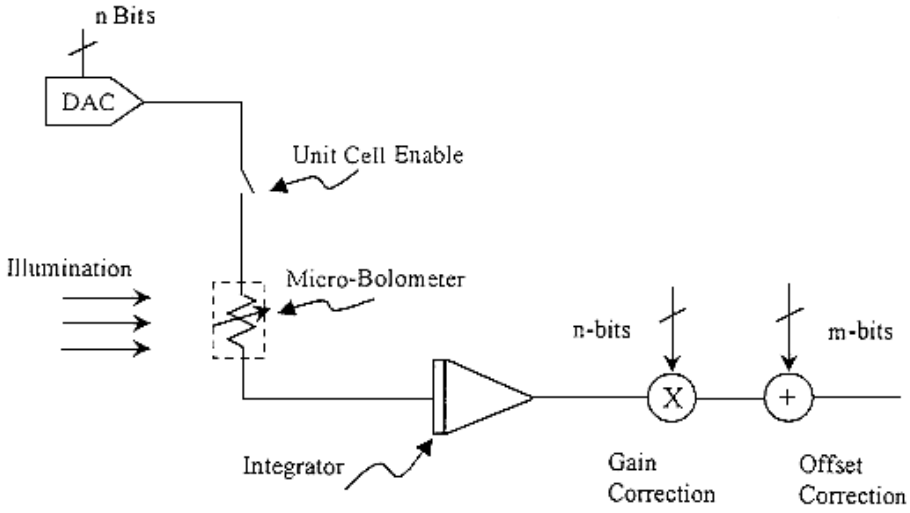


Fig. 2.16. Block diagram of the three-point correction scheme

More recently, smart functions of the FPA readout technologies, such as neural network concept[122], pixel averaging[123], bad pixel substitution[124] and edge enhancement[125][126] have been presented. Neural network mimics the function of biological sensors using silicon IC design. Pixel averaging and bad pixels substitution has been suggested that the bad pixels in the focal plane are replaced with the average value of the surrounded pixels. Edge enhancement and other pattern recognition functions not only improve the IR image quality, but also can extract the user-interested information[127]. These techniques have further enhanced the performance of the uncooled IR focal plane array and have potential to be applied to the uncooled FPAs.

2.4. Self-heating effect and cancellation techniques

In order to sense the resistance change, the microbolometer must be biased by either a voltage or a current source. The current bias current flowing through the bolometer generates the Joule heat which raises the temperature of the bolometer. Thus, the bolometer temperature will depend on both IR incident power and the Joule heat. The Joule heat due to the bias current is normally much higher than the absorbed infrared power and must be in some way compensated before the IR induced signal can be read out. Although studies have shown that the self-heating effect should not degrade the long-term characteristics of microbolometer[128], the readout circuit is required to have large dynamic range to accommodate the self-heating. Several techniques for compensating the self-heating effect have been reported.

One of the methods proposed in [129] treats the self-heating effect as a DC offset similar to the FPN in the focal plane array and cancels it accordingly. However, this method does not allow a subsequent integration to be performed on the readout signal, and hence the signal-to-noise ratio cannot be further improved.

A commonly used compensation technique is to use a "blind" (dummy) bolometer to balance the self-heating power [30][130]. The blind bolometer is a one that is identical to the pixel bolometer, except that it is "blocked" from IR radiation. Thus, it is only subject to the self-heating. The signal from the blind bolometer is subtracted from the output of the normal bolometer, as shown in Fig.2.17. Although in principle, the self-heating can be removed, in practice, it is difficult to construct the blind bolometer that is shielded from the incident IR radiation.

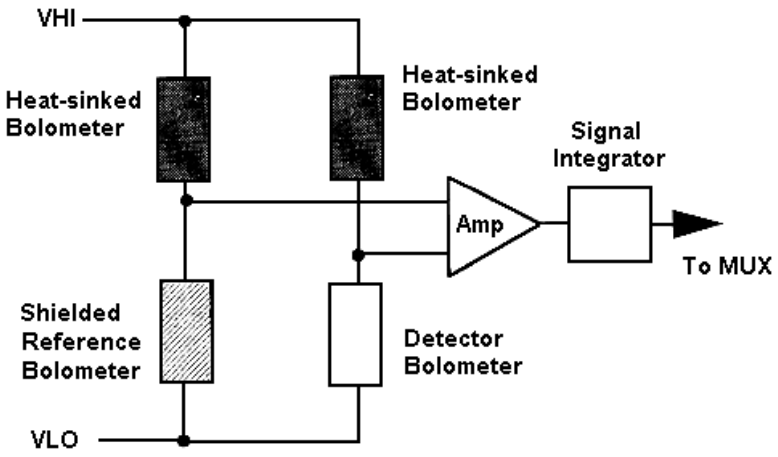


Fig. 2.17. Front-end readout circuit with the self-heating cancellation using blind bolometer

Another self-heating compensation technique based on the dummy bolometer was reported in Ref.[131] and [132]. Being different from the previous ones, the dummy bolometer has the same thermal mass, but higher thermal conductivity than the normal bolometers and no IR shielding is required. The compensation circuit is shown in Fig.2.18. The bolometer is pulse biased.

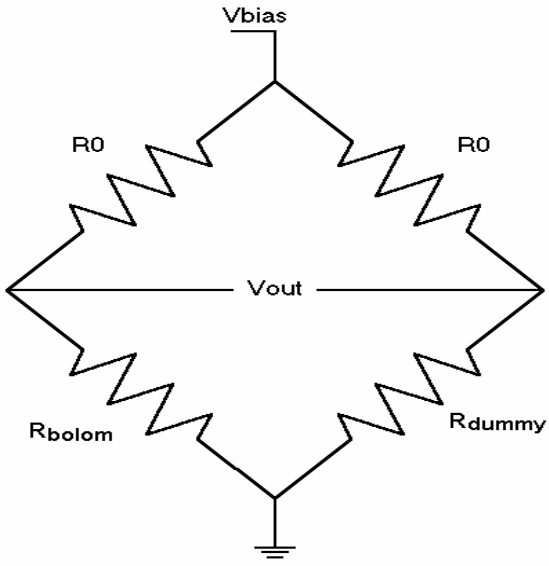


Fig.2.18. Self-heating compensation circuits in [131] [132].

Under the condition that the bias period (t_{bias}) is much smaller than the thermal constant of both dummy and bolometers, the dummy device would have little response to the IR radiation, but its temperature drift due to self-heating is almost same as that of the normal bolometer in a pixel. Thus, the self-heating is effectively cancelled at the output. In this scheme, the cooling rate of dummy devices is required to be much higher than that of the normal bolometer since it needs to be cooled down before next pixel in the same row is read. Therefore, trade-off must be made in selecting the thermal conductance of dummy cells. The high cooling rate requires high thermal conductance; however, if the thermal conductance of dummy devices is too high, the condition $t_{bias} << \tau$ may not be valid.

Two similar off-chip compensation methods, which are using the ramp voltage to cancel the self-heating effect, have been reported for pulse bias heating of microbolometer detectors[133]. One assumed that the detect signal sent to the pre-amplifier was a differential voltage between the detector output and a reference. The other directly compensated the ramp of detector voltage due to self-heating effects. The functional architectures of these two approaches are shown in Fig.2.19.

In these methods, an additional on-chip sensor must be used to sense the resistance value of the microbolometer. The off-chip circuits generate the ramp voltage corresponding to the measured resistance level. The ramp voltage produced by the circuit in Fig.2.19(a) enables the V_{ref} to track the bolometer voltage. Similarly, the compensation ramp in the Fig.2.19(b) is inverted so that the bias heating response of V_d can be cancelled. The on-chip r_{sense} was made by the resistive material with a temperature coefficient identical to that of bolometer, but it was not thermally isolated. Thus, it can track the ambient (substrate) temperature.

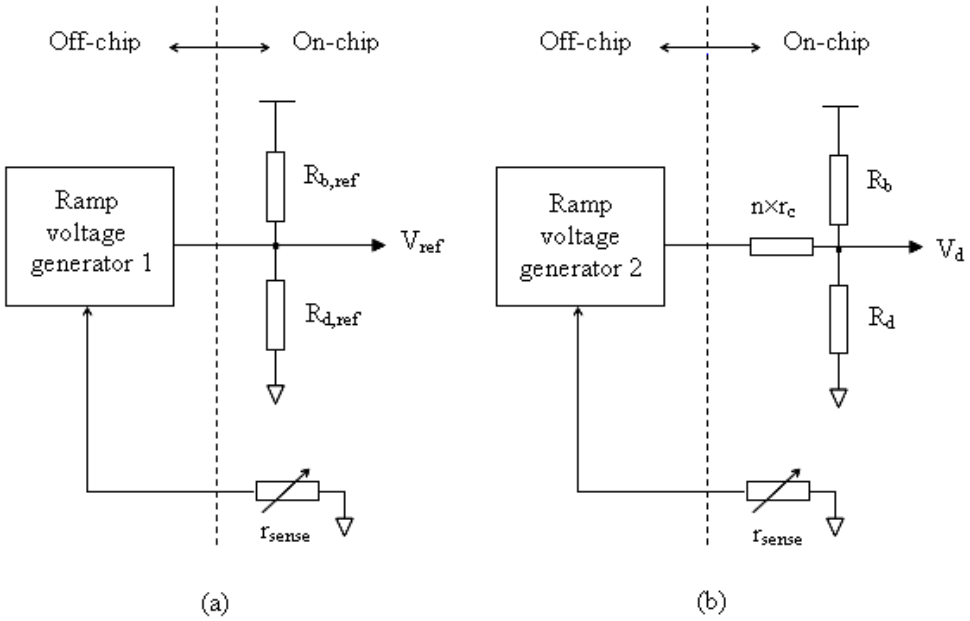


Fig.2.19. Off-chip self-heating compensation schemes
(a)Compensation of the difference of V_{ref} and V_d; (b) Direct compensation of V_d.

2.5. Summary

As the performance of the IR detectors continue to improve, the IR imaging technology is advancing toward uncooled, higher sensitivity, smaller and cheaper systems. Studies have showed that the self-heating noise of the Ti microbolometers significantly affects the signal-to-noise ratio of the readout circuits [131][132]. Although the function filled ROIC today can provide satisfactory performance for some applications, few self-heating techniques have been reported. The effective suppression of the self-heating noise can further improve the performance of readout circuit and hence the IR imaging arrays. At the present, the available on-chip self-heating compensation methods provide only passive cancellation, which cannot be tuned and therefore are not effective. In this project, a simple and effective self-heating cancellation technique is proposed and related on-chip readout circuits are developed.

Chapter 3. Electro-thermal Characteristics of Microbolometer

The microbolometer is essentially a temperature sensor built on thermally isolation structure, which absorbs the infrared radiation. Its operation is similar to that of a simple temperature-sensitive resistor. When receiving the incident infrared radiation, the microbolometer is heated up by the radiant power absorbed, resulting to a change of its resistance. In order to monitor the amount of the resistance change, the microbolometer must be electrically biased. The bias current flowing through the sensor during the readout period also causes the Joule heating (self-heating) of the microbolometer. Even the bias period for each microbolometer unit is very short comparing with the frame period, the temperature increase due to the self-heating is much higher than that due to the room temperature input infrared power. For the purpose of obtaining a measurable change in the bolometer's temperature, which results from a very small input infrared power, a good thermal isolation from the substrate is highly desired. Thus, the heat resulting from the self-heating power cannot be quickly dissipated. As a result, the microbolometer resistance change not only results from the information of infrared input, but also the self-heating effect.

Because of the interactions of the input infrared and the self-heating power, which are associated with the feedback between the microbolometer and its readout circuits, the temperature and resistance change of the microbolometer is no longer as simple as it seems to be. An accurate simulation model based on the detailed understanding of these behaviours is therefore required for the design of the readout electronics. Such

a model is also useful for the study of the self-heating effect and cancellation techniques.

3.1. Thermal characteristics of microbolometer

The thermal behaviour of a microbolometer is mainly determined by its thermal time constant τ, thermal conductance G and the thermal capacitance H. The relationship among the three thermal parameters is defined by

$$\tau = \frac{H}{G} \tag{3 - 1}$$

Normally the thermal time constant ranges from several millisecond to less than 20 ms. Using the parameters defined above, the heat balance equation of microbolometer, including the self-heating effect, can be written as

$$H\frac{dT}{dt} + G(T - T_0) = P_{bias} + \varepsilon \cdot \varphi \tag{3 – 2}$$

where the T_0 is the ambient temperature, T is the bolometer temperature; P_{bias} is the self-heating power, ε is the absorptivity coefficient of the sensor element and φ is the input radiation power.

The last item in the equation (3 - 2), which can be further defined by Eq.(3-3), represents the infrared power the sensor absorbed. It causes the heating up of bolometer elements.

$$P_{IR} = \varepsilon \cdot \varphi \tag{3 - 3}$$

Characterization of the heat propagation by an equivalent RC electrical circuit had

previously been reported by Auerbach *et al* [134]. The resistor R and capacitor C are used to represent the thermal conductance G and the thermal capacitance H, respectively. Thus the thermal behaviour of the sensor and the medium can both be simulated by standard programs, such as SPICE.

Defining the thermal resistance as $R = 1 / G$, and with the help of current generators, the quantities in the equation (3-2) can be well characterized by their electrical equivalents listed in the Table 3.1, where the thermal resistance and capacitance are lumped values, but not cover the nature of the heat distributed in the device.

Table 3.1 Electrical equivalents of the thermal behavior quantities of microbolometer

Thermal Behaviour	**Electrical equivalent**
Sensor Temperature *T (K)*	Voltage *T (V)*
Ambient Temperature T_0 *(K)*	Voltage T_0 *(V)*
Thermal Capacitance *H (J/K)*	Capacitance C_T *(F)*
Thermal Resistance *R (K/W)*	Resistance R_T *(Ω)*
Self-heating Power P_{bias} *(W)*	Current P_{bias} *(A)*
Input Infrared Power P_{IR} *(W)*	Current P_{IR} *(A)*

Now the heat balance equation (3-2) can be rewritten using these equivalents in electrical domain.

$$C_T \frac{dT}{dt} + \frac{(T - T_0)}{R_T} = P_{bias} + P_{IR} \qquad (3-4)$$

3.2. Construction of SPICE electro-thermal model of microbolometer

In order to effectively study the thermal behaviour of the microbolometer, the SPICE

electro-thermal model of the microbolometer is constructed and described in this section.

3.2.1. Elector-thermal model of microbolometer

The sensor material used in this study is titanium. The temperature coefficient of resistance (TCR) for the titanium thin film bolometer can be as high as 0.25% K^{-1}[48]. For the metallic bolometer materials, the resistance has a linear dependence on the temperature according to the first order approximation of TCR. The linear equation relating resistance and temperature change is:

$$R(t) = R_0 + R_0 \cdot \alpha \cdot [T(t) - T_0] \qquad (3-5)$$

where α is the TCR of the sensor material, and R_0 is the bolometer resistance at the room temperature T_0. The resistance, $R(t)$, and the temperature, $T(t)$, of the bolometer are all time dependent.

If $I(t)$ is defined as the bias current applied to the bolometer during readout, the bias power (self-heating power) can be expressed as

$$\begin{aligned} P_{bias} &= I^2(t)R(t) \\ &= \frac{V^2(t)}{R(t)} \\ &= \frac{V^2(t)}{R_0 + R_0 \cdot \alpha \cdot (T(t) - T_0)} \end{aligned} \qquad (3-6)$$

where $V(t)$ is the voltage across the resistive sensor, and

$$\begin{aligned} I(t) &= \frac{V(t)}{R(t)} \\ &= \frac{V(t)}{R_0 + R_0 \cdot \alpha \cdot (T(t) - T_0)} \end{aligned} \qquad (3-7)$$

When there is a bias current flowing through the microbolometer, the microbolometer temperature increases not only due to the presence of P_{IR} but also the effect of P_{bias}. At the same time, the microbolometer resistance increases according to equation (3-5). If the readout circuit uses a stable power supply during readout period, the current flowing through the sensor decreases due to the increase of the resistance. Thus, strictly speaking, *I(t)* should also be a time dependent variable. For the same reason the voltage across the sensor element, *V(t),* also varies in the readout period. All of these should be represented in the electro-thermal model of the microbolometer.

Combining the equation (3-4), (3-5), (3-6) and (3-7), the completed electro-thermal model of the microbolometer can be constructed using SPICE circuit elements. The schematic of the SPICE model is shown in the Fig. 3.1.

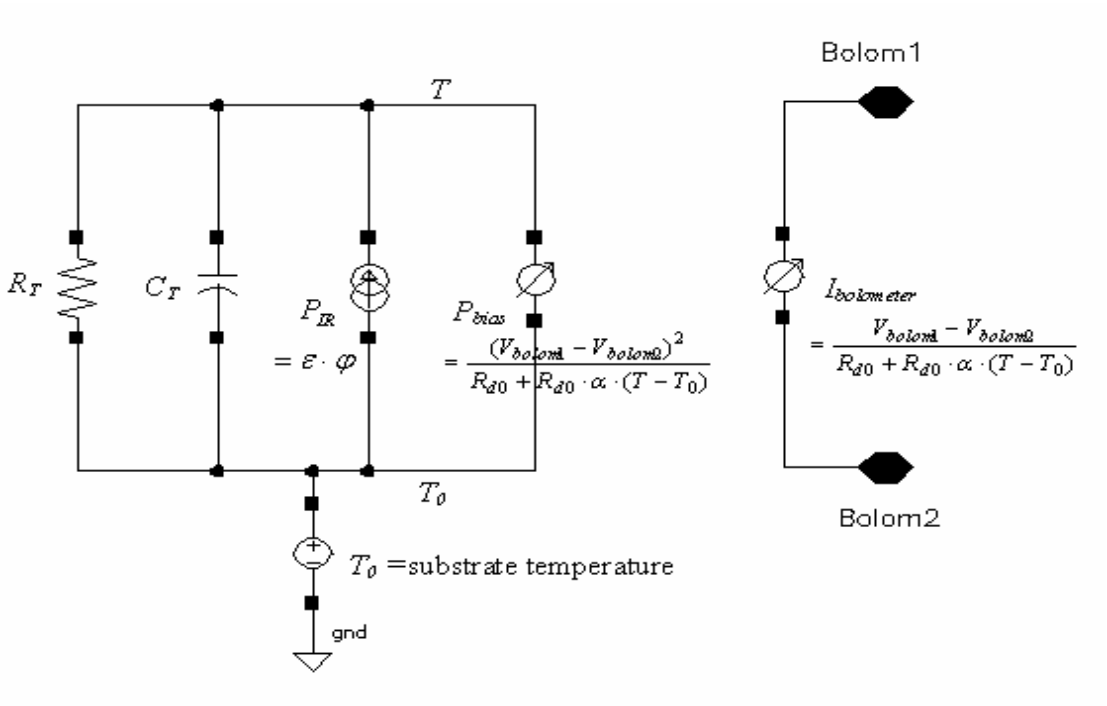


Fig.3.1. Electro-thermal model of microbolometer

In this model, the substrate temperature is implemented by a DC voltage source.

Bolom1 and *Bolom2* are the two terminals of the microbolometer. The equations of two controllable current sources, P_{bias} and $I_{bolometer}(t)$, are defined by Eqs. (3-6) and (3-7), respectively. The current source P_{IR} has a constant current whose value is equal to the input infrared power.

3.2.2. Verification of the SPICE microbolometer model

In order to verify the SPICE model of microbolometer, the experimental data reported in Ref.[95] were used. The circuit configuration of in [95] was a Wheatstone bridge. The experimental set-up including the pulse generator and other measurement equipments is illustrated in the Fig.3.2.

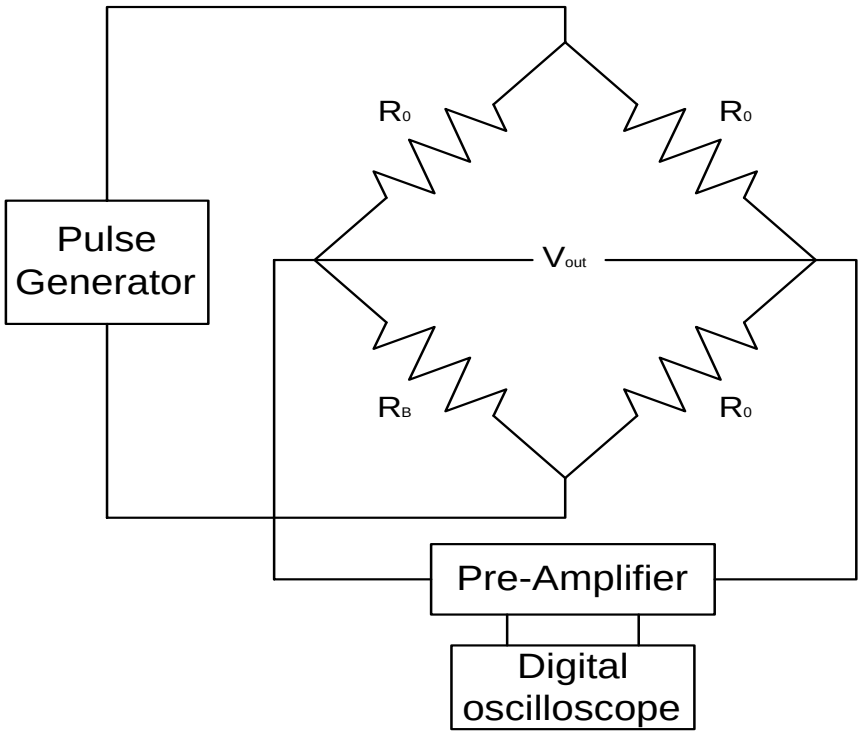


Fig.3.2. Experimental setup in Ref.[95], where R_B is the microbolometer and R_0s are the fixed reference resistors.

In the experiments, the three constant value resistors in the Wheatstone bridge have the very similar value as the room temperature resistance of the tested bolometer. The magnitude of the squared pulse was 1 Volt and the duration was 60 ms. The parameters of two single microbolometers were extracted by measuring the time dependent output voltage of a balanced Wheatstone bridge containing a microbolometer under pulse bias condition. Thermal capacitances and thermal conductances of microbolometer 1 and 2 had been independently obtained using the slope of the linear region and the saturated value of the output voltage, respectively.

To verify the SPICE model of the microbolometer, the similar Wheatstone bridge structure was used in the simulations for the comparison with the experimental results in [95]. The same voltage source and the resistor values reported in [95] have been used in simulation. The equivalent parameters of our SPICE model used in the simulations were also calculated to match those of microbolometers used in [95] at most. The thermal resistance is calculated using the following equation.

$$R_T = \frac{1}{G} \tag{3-8}$$

The thermal capacitance was calculated from

$$C_T = G \times \tau \tag{3-9}$$

The comparison between the simulation results and the experimental data in [95] is done for two microbolometers. The parameters of the two microbolometers used in both simulation and experiment are listed in Table 3.2, respectively. Figure.3.3 shows the simulation results of the output voltage V_{out} together with the experimental data, where the red curves correspond to the simulation results with the proposed SPICE model as detectors and the black curves correspond to the experimental results

reported in Ref.[95]. A good agreement between the simulated and experimental results is obtained, which indicates the correctness of the SPICE electro-thermal model for the microbolometer.

Table 3.2. Parameters of the two bolometers used in the experiments and simulation.

	Microbolometer 1		Microbolometer 2	
	In experiment	In simulation	In experiment	In simulation
Room temperature resistance	3.9 kΩ	3.9 kΩ	3.9 kΩ	3.9 kΩ
Thermal conductance	6.9×10^{-7} W/K		3.6×10^{-6} W/K	
Thermal time constant	8.7ms		2.5ms	
Thermal resistance		1.45 MΩ		278 kΩ
Thermal capacitance		6.0 nf		9.0 nf
TCR of the material	0.25%	0.25%	0.25%	0.25%

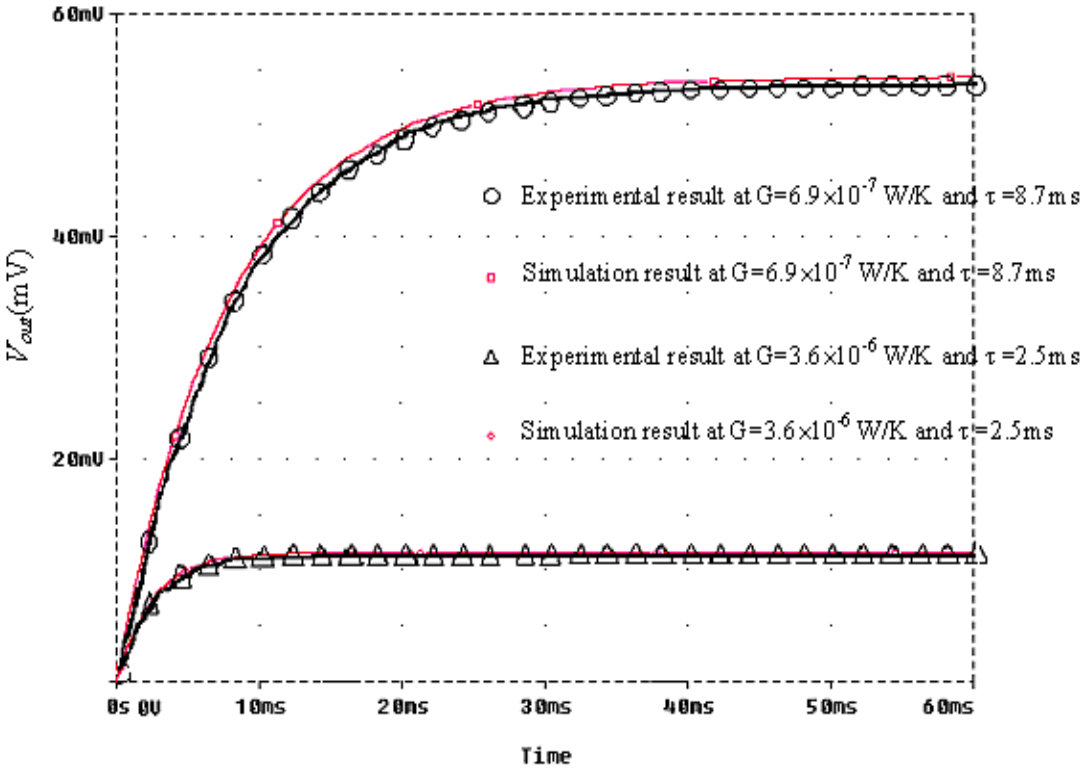


Fig.3.3. Comparison of simulation results using the SPICE model with the experimental data.

3.3. Study of response of the microbolometer to the infrared and self-heating power

Theoretically, the expression of the temperature variation ΔT of microbolometer can be derived from the heat balance equation, Eq.(3-2), provided that the initial conditions are known. When studying the microbolometer self-heating effect in the short bias period, the input IR power can be set to zero. Then the expression of ΔT due to the self-heating as the function of time t can be derived as:

$$\Delta T\big|_{P_{IR}=0} = \frac{P_{bias}}{G}(1 - e^{-\frac{t}{\tau}}) \qquad (3-10)$$

Under normal operation, the readout period, $t_{bias,}$ for each microbolometer in an IR FPA (typically several microseconds) is much shorter than the thermal time constant, τ, of the microbolometer[135]. Thus, the equation (3-10) can be further simplified to

$$\Delta T = \frac{P_{bias}}{G \times \tau} \cdot t = \frac{P_{bias}}{H} t \qquad (t_{bias} << \tau) \qquad (3-11)$$

The Eq.(3-11) indicates that the temperature difference due to the self-heating power is independent of the thermal conductance of the microbolometer under the condition of $t_{bias} << \tau$.

The self-heating behaviours of microbolometer were simulated by using the electro-thermal model in SPICE to represent the microbolometers. In an IR focal plane array (FPA), each bolometer elements acts as one pixel. Pixels are addressed one by one so that the signal of all pixels can be read separately during one frame period. In order to

understand the behaviour of the microbolometer, we first simplify the study by considering a single microbolometer pixel, and studying its self-heating behaviours under Wheatstone bridge readout, constant current bias readout and constant voltage bias readout circuits.

First, the microbolometer model was connected to a Wheatstone bridge readout circuit as shown in Fig.3.4. R_d, the detector, is replaced by its SPICE model in succeeding simulations. R_1 is a normal resistor whose resistance is equal to the room temperature resistance of bolometer, R_{d0}. R_0 and R_2 are also normal resistors whose values are chosen to only one tenth of R_{d0} so that it is possible to fabricate them inside the pixel near micorbolometers to reduce the fixed pattern noise. If there is no bias voltage or current and no infrared incident applied to the bolometer detector, the bolometer resistance would remain as R_{d0}. The output of the Wheatstone bridge is zero. When a pulse voltage is applied to the bridge circuit, the R_d increases due to both the infrared incident and self-heating power, and an output voltage V_{out} across the Wheatstone bridge is thus generated.

A square pulse voltage source is applied to the Wheatstone bridge circuit to provide the necessary bias to the microbolometer detector. The magnitude of the pulse voltage is set to 5 V and the duration is 10 μs. R_{d0} and R_1 are set to 5 kΩ, and R_0 and R_2 are equal to 500 Ω. The parameters of the microbolometer IR detector used in the simulation, which provided by the Ti microbolometer development institute, Institute of Microelectronics, Singapore, are listed in Table 3.3.

The thermal time constant of the microbolometer causes its temperature to rise exponentially with time when the microbolometer is exposed under a constant power

IR radiation. This is analogous to the charging of a capacitor in an RC circuit. The larger the thermal time constant, the slower the response of the microbolometer. The responses of the microbolometer to the different input infrared power have been studied. The infrared powers are set to 3.7 nW, 28.2 nW and 108 nW, respectively.

Table 3.3. Parameters of the microbolometer used in the simulation.

Microbolometer parameters	**Values**
Detector resistance at T_0, R_{d0}	5000 Ω
TCR, α	0.2%
Thermal Resistance, R_T	2.1×10^6 Ω
Thermal Capacitance, C_T	1.7 nf
Ambient temperature, T_0	300°K
Initial temperature difference ΔT_0	0°K

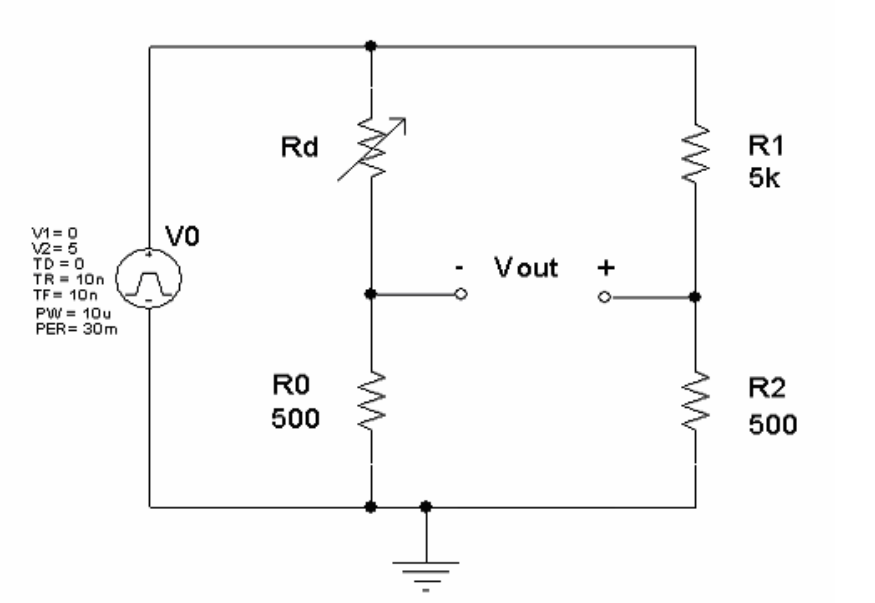


Fig.3.4. Wheatstone bridge readout circuit.

The simulation results shown in the Fig.3.5 illustrate the temperature changes of the microbolometer at the different input powers, while the bias heating power is set to zero. The exponential relationship between ΔT of the microbolometer and time can be

clearly observed. This agrees with what is predicted in Eq. (3-10). The simulation time has been set to long enough to observe the saturation of the temperature difference. It can be seen that ΔT rises to the saturated value after about 30 milliseconds and almost had no change after that even though the input power was continually applied to the sensor. The saturated value reflects the input infrared power and is sensed by the microbolometer. The temperature change of the pixel is converted to a voltage through the microbolometer during the readout.

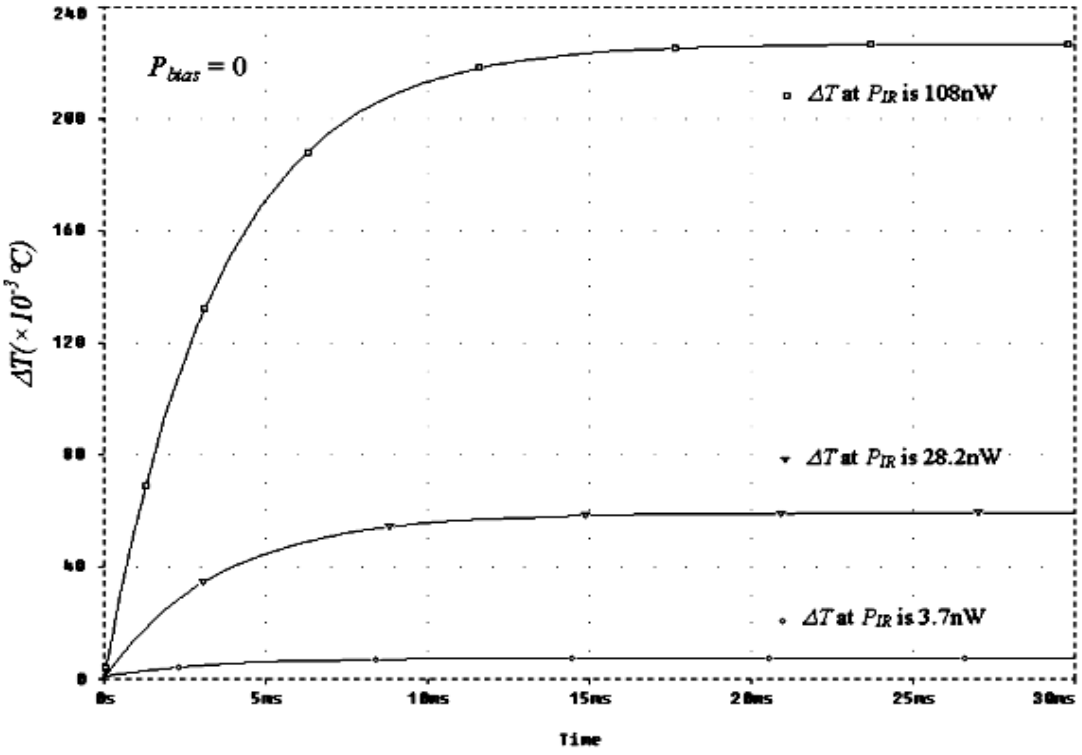


Fig. 3.5. Temperature changes of the microbolometer, ΔT, with different IR powers.

When a thermal image is taken by the infrared imager, the IR incident emitted by the object will first be focused on the infrared detector array by an optical lens. Thus, the detector array is heated up by the input infrared power for a time long enough for sensors to reach the saturated temperature before the readout electronics begins to work. To mimic the real operating condition, a short pulse bias voltage is applied to

the Wheatstone bridge circuit 50 ms after the input infrared power is applied to ensure that the response of the microbolometer to the input power P_{IR} is stabilized. In this way, both self-heating and the IR response of the microbolometer can be observed. The simulation results in the bias period of 10 μs after 50 ms are shown in Fig. 3.6.

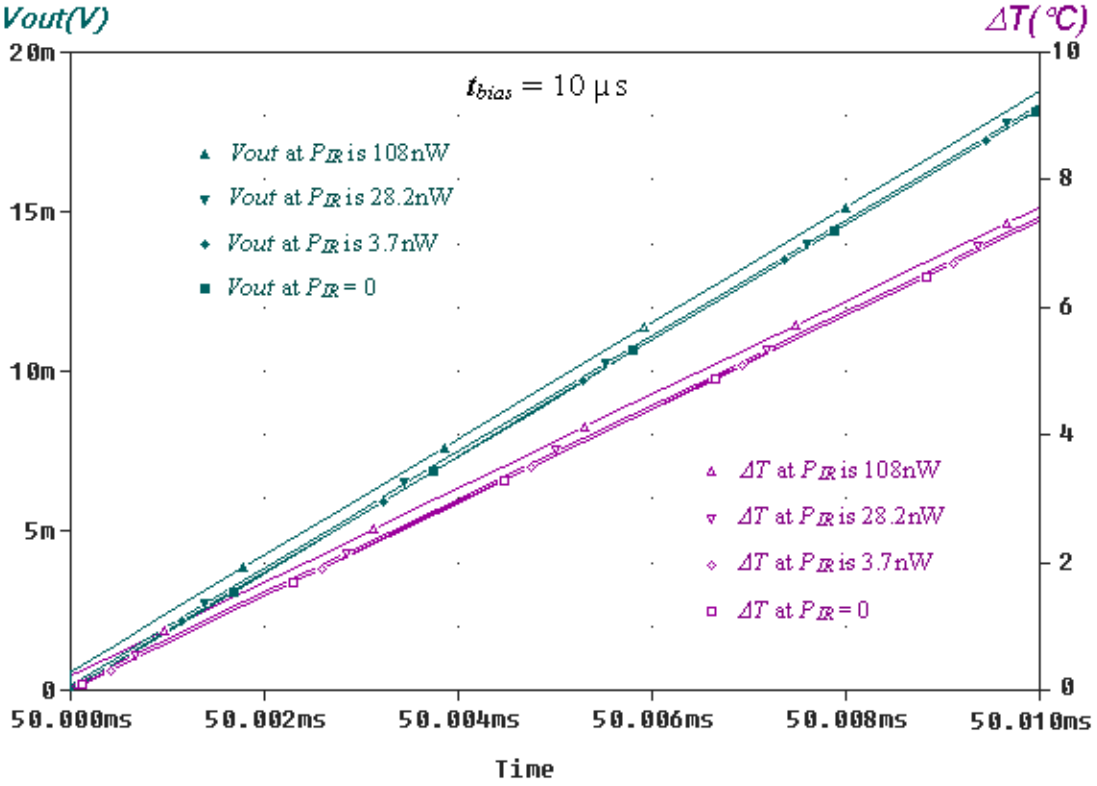


Fig. 3.6. Output voltage (green curves) and the temperature change (pink curves) of the microbolometer with different input IR powers.

It can be see that the in the short bias period, the bridge output and the temperature variation of microbolometer rise almost linearly, which agree with Eq.(3-11). In the simulation, the bolometer is first exposed to the IR radiation and lets its response reach the saturated level before a pulse bias is applied. This is reflected by the small voltage or temperature steps at the beginning of the bias period. The differences between curves represent the response to the incident IR power, while the linear rise of the microbolometer temperature or voltage is due to the self-heating effect.

Normally the infrared power radiated by an object around room temperature and absorbed by the microbolometer in the pixel is below 10 nW. Therefore, from the Fig. 3.6, it can be clearly seen the output generated by the self-heating power is much higher than that due to the input infrared power. For instance, the small step voltage in response to the 3.7 nW infrared input power is only about 8 μV, while the output due to the self-heating can be as high as 18 mV. Even when the infrared input power is increased to 108 nW, the output voltage due to IR power is only about 0.6 mV.

When using Wheatstone bridge readout circuit in Fig. 3.4, assuming the bridge is balanced, the room temperature object (P_{IR} = 3.7 nW) can provide the output voltage change

$$\Delta V_{out} = \frac{\alpha \Delta T \cdot R_{d0} R_0}{(R_{d0} + R_0)(R_{d0} + \alpha \Delta T + R_0)} V_{bias} \approx 0.66 \times 10^{-6} V_{bias}$$

Thus, the bias voltage required for a 3 μV output, which is minimum readable signal, is 4.55 V. If the bias voltage is lower, objects in room temperature would be difficult to be sensed. However, if the bias is too high, there would be large self-heating problem. Since the system supply is 5 V, thus, the bias voltage of 5V is selected.

If the bias is applied for the duration of thermal time constant (~ ms) the temperature of a microbolometer reaches nearly the maximum. This can be relatively large (hundreds of degrees) in particular smaller thermal conductance used in microbolometers. Thus, it is important to minimize the bias time which in turn can increase the noise due to increase in bandwidth. The Johnson noise of a 5000 Ω micbolometer can be expressed as

$$V_{b\_n}{}^2 = 4kTR_bB \qquad (3\text{-}12)$$

where k is the Boltzmann constant that equals to1.38×10^{-23} J/K, B is the bandwidth. According to the Eq. (3-12), to achieve a signal-to-noise (S/N) ratio higher than 1 for a 3 μV IR signal output at 300 °K, the maximum bandwidth can be reached is:

$$B < \frac{(3\mu V)^2}{4kTR_b} = \frac{(3\mu)^2}{4 \times 1.38 \times 10^{-23} \times 300 \times 5000} \approx 108.7\,\text{kHz}$$

Thus, the minimum bias period required for 3 μV signal can be obtained as

$$t_{bias\_\min} = 1/(108.7 \times 10^3) \approx 9.2\mu s$$

In this thesis, the bias time was set to around 10 μs to avoid the over heating problem and satisfy the S/N ratio requirement.

The self-heating effects under constant current and voltage bias readout circuits have also been studied, respectively. Similar to using Wheatstone bridge, the bolometer is first exposed to the IR radiation till saturated then the pulse bias is applied. Fig. 3.7 and 3.8 show the output of the readout circuits and microbolometer temperature changes at constant current (500 μA) and constant voltage (2.5 V) bias, respectively. It is observed that in these two biasing mode, the self-heating effects of the microbolometer are also much higher than the output due to IR signals. In constant current bias, the output voltage in response to the 3.7 nW infrared input power is only about 32 μV, while the output due to the self-heating can be as high as 37.4 mV. Even when the infrared input power is increased to 108 nW, the output voltage due to IR power is only about 2.6 mV. Similar results can be obtained from the Fig. 3.8, the output current due to the self-heating (7.1 μA) is more than 10 times higher than that due to the 108 nW IR input (0.56μA).

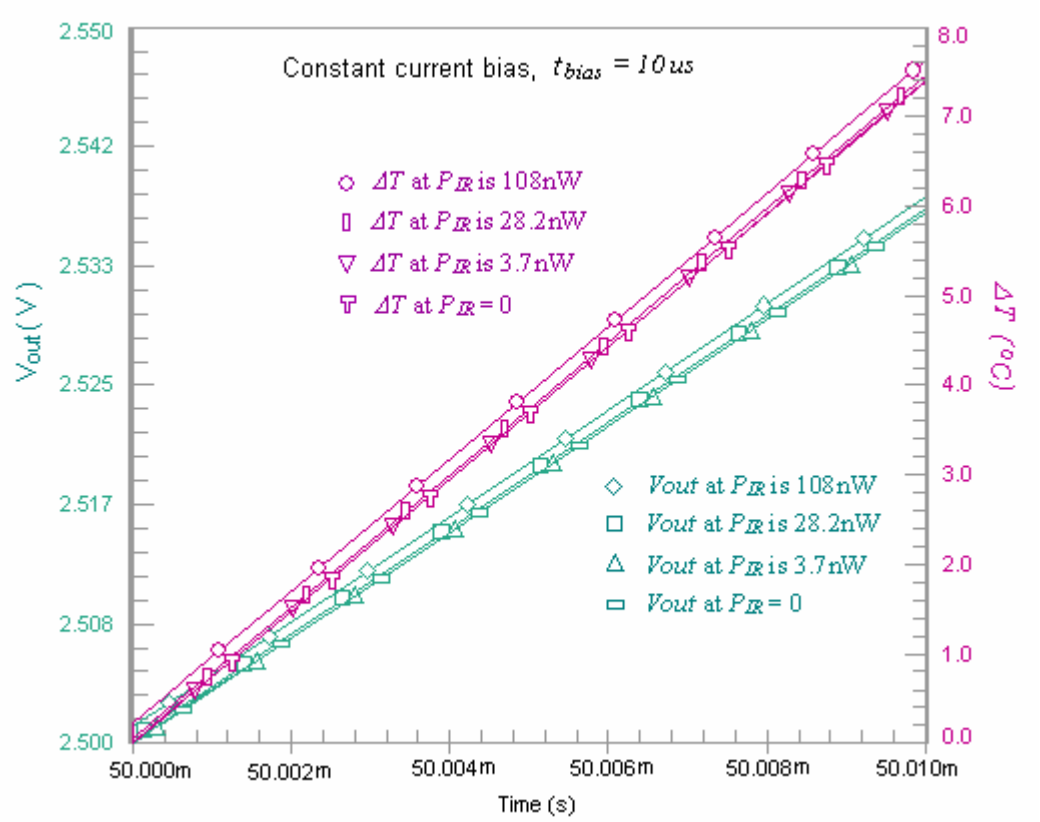


Fig. 3.7. Output voltage (green curves) and the temperature change (pink curves) of the microbolometer with different input IR powers, at constant current bias.

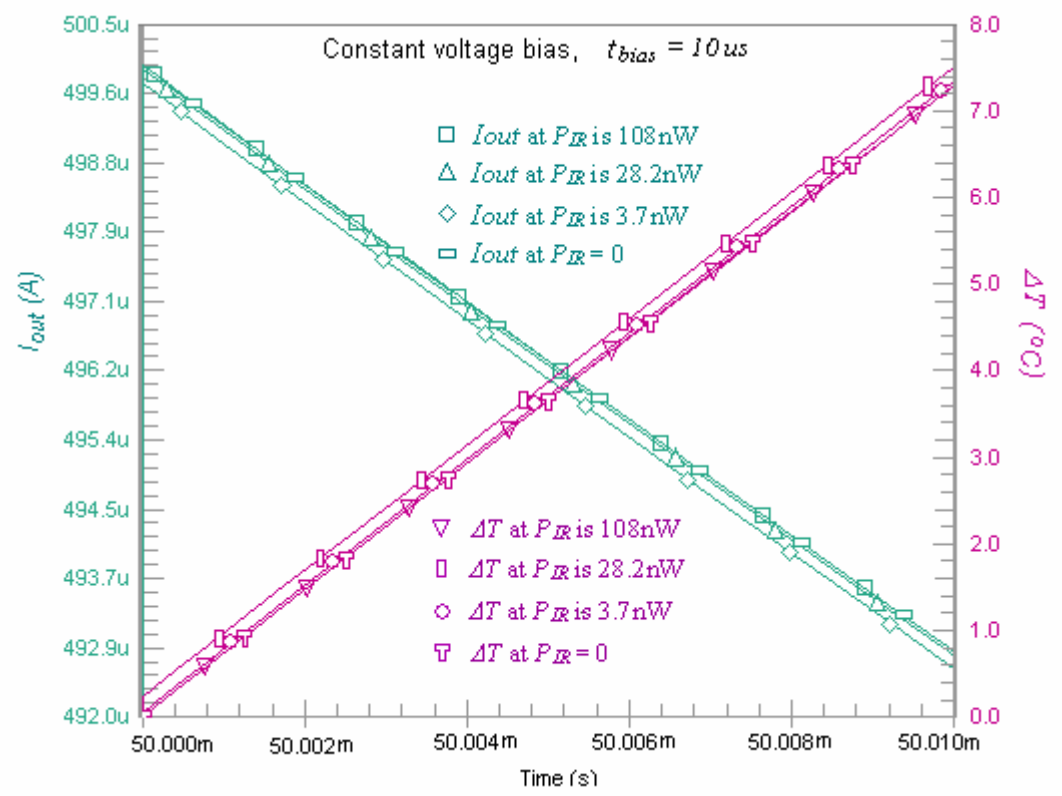


Fig. 3.8. Output current (green curves) and the temperature change (pink curves) of the microbolometer with different input IR powers, at constant voltage bias.

3.4. Summary

In this chapter, a SPICE electro-thermal model of microbolometer is developed based on the equivalence between the thermal and electrical domain. This model was validated by the comparison between the simulation and the experimental results. With the help of the SPICE model, the thermal characteristics of the microbolometer, especially the self-heat effects, have been studied using a Wheatstone bridge readout circuit. The study shows that the self-heating effect of microbolometer is independent of the thermal conductance in short readout period. The simulation results of the Wheatstone bridge, constant current bias and constant voltage bias readout circuits have proven that the response of the microbolometer due to the infrared radiation is much smaller than that of the self-heating. Hence the self-heating cancellation is indispensable for the high-performance readout electronics for the IR FPA.

Chapter 4. Readout IC for Microbolometer with Voltage-mode Self-heating Cancellation

It can be clearly seen from the description in the chapter 3 that the bolometer IR detectors are strongly influenced by the self-heating effect. Such an effect results in a large thermal drift in the circuits and a large portion of the dynamic range of the subsequent pre-amplifier is therefore sacrificed. Thus, an on-chip self-heating cancellation is crucial and necessary for the readout circuits.

Another severe problem for IR FPA application is spatial non-uniformity, which results in a large fixed pattern noise. It will greatly degrade the dynamic range of the readout circuit. In order to improve the performance of the FPA, the FPN must be removed before the signal is further amplified.

In this chapter, a prototype voltage-mode readout circuit with a new on-chip self-heating and FPN cancellation techniques is presented. The self-heating cancellation circuit is based on the equivalence between the electrical and thermal systems and utilizes a capacitor to mimic the thermal capacitance of the bolometer. This enables the bias-heating to be replicated and later used to cancel itself. FPN correction is achieved by first digitally storing the pixel-to-pixel variation under the dark condition to an off-chip memory, and later subtracting them from the signal.

4.1. A new self-heating cancellation method

Since the thermal behaviour of the microbolometer is very similar to the charge and discharge of a capacitor, a new self-heating cancellation circuit based on the equivalence between the electrical and thermal capacitance is presented[136]. The circuit uses a current source and a capacitor to mimic and cancel the self-heating effect. The simulation result shows that the proposed circuit can effectively cancel the self-heating and is suitable for the implementation of monolithic microbolometer-based infrared focal plane arrays.

4.1.1. Self-heating cancellation circuit

It has been shown in the chapter 3 that the self-heating is directly dependent on the thermal capacitance provided that $t_{bias} << \tau$. The smaller the thermal capacitance, the higher the self-heating effect. Based on the equivalence between the electrical and thermal capacitance, a replica of self-heating effect can be generated on an electrical capacitance and used to cancel the self-heating from the microbolometer. A self-heating cancellation circuit based on this concept is therefore designed and schematically shown in Fig.4.1. In this modified bridge circuit, R_d represents bolometer detector and R_2 is the fixed value resistor whose resistance is same as the room temperature resistance of R_d, that is, R_{d0}. The two resistors R_1 and R_3 only have one tenth of the value of R_2 so that R_1 can be fabricated in each pixel cell using the same material as the detector R_d. Thus, ratio of R_{d0}/R_1 can be made near constant within whole readout IC area. The ratio of R_2/R_3 is chosen to be equal to R_{d0}/R_1. The switches are controlled by a two-phase non-overlapping clock whose waveform is shown in Fig. 4.2. The bridge is biased by the constant voltage supply V_{dd}. However the row and column select switches

SW1 and SW2 enable each microbolometer to be pulse biased to avoid overheated.

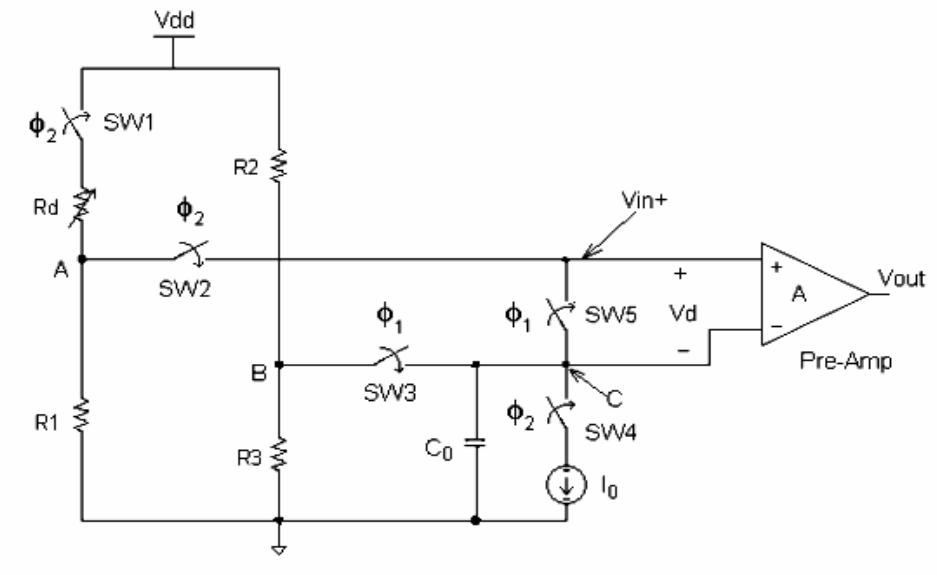


Fig.4.1. Schematics of the self-heating cancelling scheme.

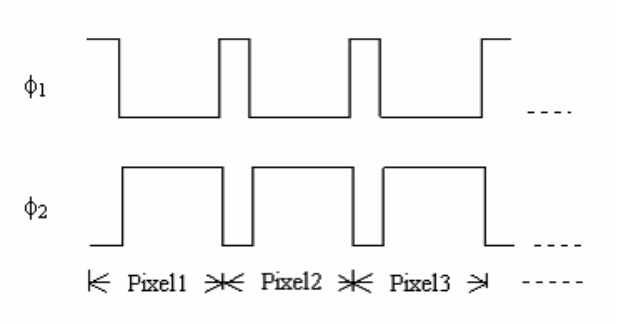


Fig.4.2. Waveforms of the clock signals.

When clock ϕ_1 is high, switch SW3 and SW5 are closed. The capacitor is pre-charged to a voltage equal to that at the point B, V_B. The inputs of the amplifier are shorted together by SW5, making V_d to be zero. When clock ϕ_2 becomes high and ϕ_1 low, switch SW1, SW2 and SW4 are closed, and the microbolometer R_d is biased. At the moment when SW1 turns on, V_A should be equal to V_B, assuming that the Wheatstone bridge is balanced and there is no infrared incident power. As soon as SW3 turns off and SW4 turns on, the capacitor will be discharged through I_0. With correctly chosen

values for C_0 and I_0, a replica of the self-heating can be generated on the capacitor, C_0. This replica can be used to effectively cancel the self-heating from the microbolometer at the input of the pre-amplifier.

4.1.2. Determination of the capacitor and current values

In order to determine values of the I-C pair that imitates the self-heating effect in the readout circuits, the behaviour of V_A in the bias period when the detector is shielded from the IR radiation must be studied. For the purpose of simplification, only the half-bridge structure is considered and the infrared incident power, P_{IR}, is set to zero.

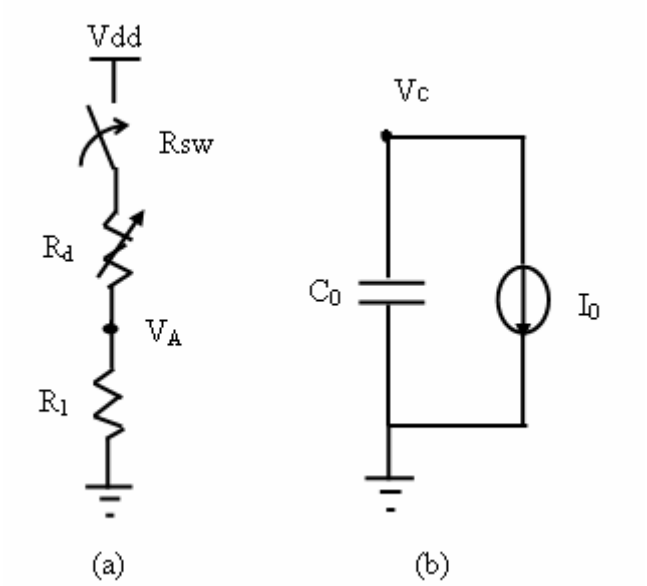


Fig. 4.3.(a) Half circuit of the Wheatstone bridge containing the microbolometer and (b) I-C pair that generates the replica of the self-heating.

From Fig. 4.3(a), the bias heating power of the microbolometer R_d can be obtained as

$$P_{bias} = \frac{V_{dd}{}^2 R_d(t)}{(R_1 + R_{sw} + R_d(t))^2} = \frac{V_{dd}{}^2 R_{d0}(1+\alpha\Delta T)}{(R_1 + R_{sw} + R_{d0}(1+\alpha\Delta T))^2} \quad (4\text{-}1)$$

where V_{dd} is a bias voltage across the Wheatstone bridge and R_{SW} is the On-resistance of the pixel-selecting switch. Since the condition $\alpha\Delta T << 1$ is normally valid for a metallic microbolometer, the bias power can be simplified to:

$$P_{bias} \approx \frac{{V_{dd}}^2 R_{d0}}{(R_1 + R_{sw} + R_{d0})^2} \tag{4-2}$$

Under normal operation, the readout period, $t_{bias,}$ for each microbolometer in an IR focal plane array (typically several microseconds) is much shorter than the thermal time constant, τ, of the microbolometer. Thus, according to Eq.(3-11), the temperature change of the microbolometer is given as the follow,

$$\Delta T(t) = \frac{P_{bias}}{H} t \qquad (t_{bias} << \tau) \tag{4-3}$$

Thus, V_A can be written as

$$\begin{aligned} V_A(t) &= \frac{V_{dd} R_1}{R_1 + R_{SW} + R_d} \\ &= \frac{V_{dd} R_1}{R_1 + R_{SW} + R_d} \cdot \frac{R_1 + R_{SW} + R_d - R_{d0}\alpha\Delta T(t)}{R_1 + R_{SW} + R_{d0}} \\ &= \frac{V_{dd} R_1}{R_1 + R_{SW} + R_{d0}} - \frac{V_{dd} R_1 R_{d0}\alpha\Delta T(t)}{(R_1 + R_{SW} + R_d)(R_1 + R_{SW} + R_{d0})} \\ &\approx \frac{V_{dd} R_1}{R_1 + R_{SW} + R_{d0}} - \frac{V_{dd} R_1 R_{d0}\alpha\Delta T(t)}{(R_1 + R_{SW} + R_{d0})^2} \qquad (R_d \approx R_{d0}, \alpha\Delta T << 1) \\ &= V_A(0) - \frac{V_{dd} R_1 R_{d0}\alpha}{(R_1 + R_{SW} + R_{d0})^2} \cdot \frac{P_{bias}}{H} \cdot t \end{aligned} \tag{4-4}$$

From Fig.4.3(b), Vc is equal to

$$V_c(t) = V_c(0) - \frac{Q(t)}{C_0} = V_c(0) - \frac{I_0}{C_0} \cdot t \tag{4-5}$$

In the self-heating cancellation circuit shown in Fig.4.1, the capacitor C_0 is pre-charged to an initial voltage $Vc(0)$, whose value is equal to $V_{B.}$ Since V_B is equal to

$V_A(0)$ when SW1 turns on, assuming the Wheatstone bridge is balanced. Thus,

$$V_A(0) = V_c(0) \tag{4-6}$$

From Eqs.(4-4), (4-5) and (4-6), it can be seen that to generate a replica of the self-heating on the capacitor, that is to make V_C(t) equal to V_A(t), the following relationship must be satisfied:

$$\frac{I_0}{C_0} = \frac{V_{dd} R_1 R_{d0} \alpha}{(R_1 + R_{SW} + R_{d0})^2} \cdot \frac{P_{bias}}{H} = \frac{\alpha R_{d0}^2 R_1 V_{dd}^3}{H(R_1 + R_{SW} + R_{d0})^4} \tag{4-7}$$

In order to verify the equation (4-7), the two circuits in Fig. 4.3 are simulated using SPICE, where R_1 = 500 Ω; R_{SW} = 500 Ω; R_{d0} = 5 kΩ; V_{dd} = 5 V. Other parameters of the microbolometer were selected according to Table 3.3. The initial voltage at V_C was manually set equal to $V_A(0)$. Substituting the above conditions into Eq.(4-7), the ratio I_0/C_0 should be equal to 7.092×10^2 (*A/F*). Considering the practical realization of the capacitor on a VLSI chip, the capacitance value was selected to be 20pf. Then the current, I_0, was calculated to be 14.2nA.

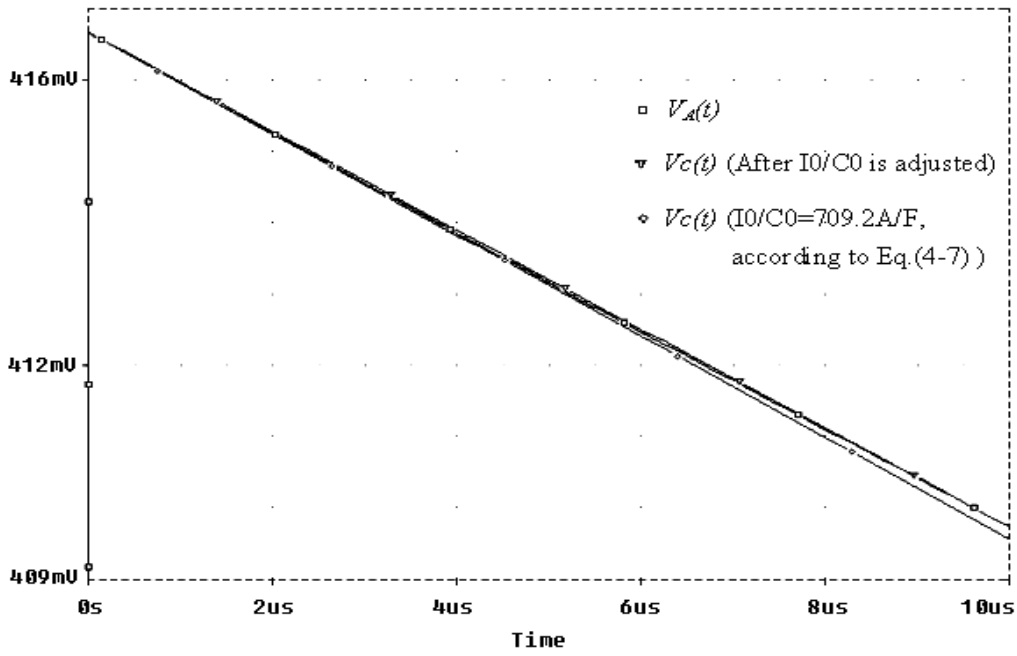


Fig. 4.4. Mimic the self-heating effect using an I-C pair.

The simulation result for $V_A(t)$ and $V_C(t)$ during the bias period are plotted in Fig.4.4. It indicates that a replica of the self-heating effect can be generated using a current source and capacitor pair. There is a small discrepancy between the curve $V_A(t)$ and $V_C(t)$ when I_0/C_0 is selected according to Eq.(4-7). This is due to the assumption, $\alpha\Delta T << 1$, made in the derivation of equation (4-7), while the simulation result is exact. Such discrepancy can be eliminated by slightly tuning the ratio I_0/C_0 by changing the current I_0. After adjusting the ratio ($I_0/C_0 = 6.92\times10^2$ A/F), $V_A(t)$ is perfectly resembled by $V_C(t)$. A replica of the self-heating is therefore generated.

4.1.3. Functional verification

The functionality of the self-heating cancellation circuit shown in Fig. 4.1 is verified by SPICE simulation where the ideal switch model is used for all the switches and a voltage control voltage source (VCVS) for the pre-amplifier. The IR power is set to zero so that the detector output voltage is only dependent on the self-heating effect. The voltage gain of the VCVS is selected to be unity. The values of I_0 and C_0 are selected according to Eq.(4-7) with the proper adjustment. The simulation results shown in the Fig. 4.5 indicate that the self-heating effect in the output, V_{out}, is significantly reduced.

In a large microbolometer focal plane array, there are always mismatches in the resistance and thermal parameters among different pixels. Such mismatch errors may degrade the performance of the self-heating cancellation circuit. Further investigation has shown that for the proposed circuit, ± 5% mismatch in microbolometer resistance

and thermal capacitance can only cause a maximum error of ±1.2 mV and ±0.8 mV in V_{out}, respectively, at the end of the readout period. Thus, compared with results in Fig. 4.5, the self-heating effect is still reduced more than 10 times. Hence, the requirement for the dynamic range of the subsequent circuits can be relaxed.

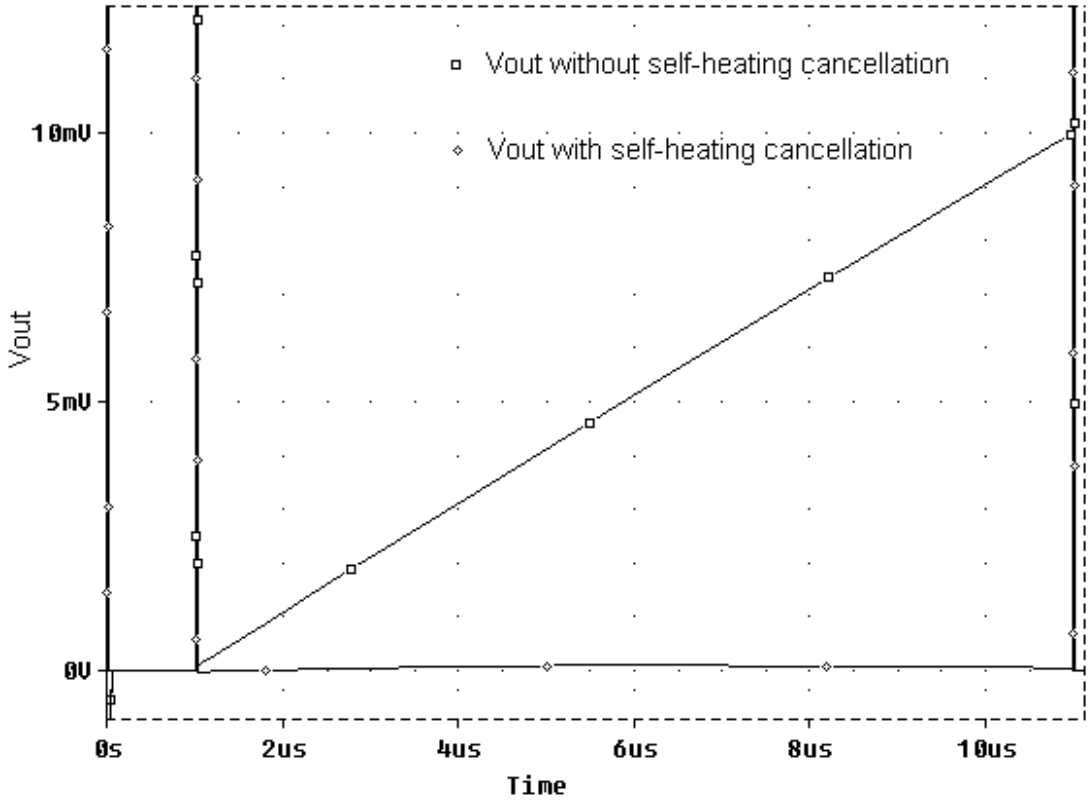


Fig. 4.5. Simulation results for the self-heating cancellation circuit.

4.2. Self-heating Cancellation circuit design

4.2.1. Circuit design

The circuit shown in the Fig.4.1 can be realized using the standard CMOS IC processing technology. The ideal switches can be implemented by MOS transistors. The schematic of the self-heating cancellation circuit is given in the Fig.4.6.

Because the switch M1 is directly connected to the bias voltage source V_{dd}, p-MOS transistor is used to avoid the body effect. Furthermore, in order to balance the ON resistance of the non-ideal switch M1, switch M0 with the same type and aspect ratio as M1 is inserted between R_2 and V_{dd}. All other switches are implemented by n-MOS transistors. A low-noise CMOS operational amplifier is used to implement the pre-amplifier, which will be described in the next section.

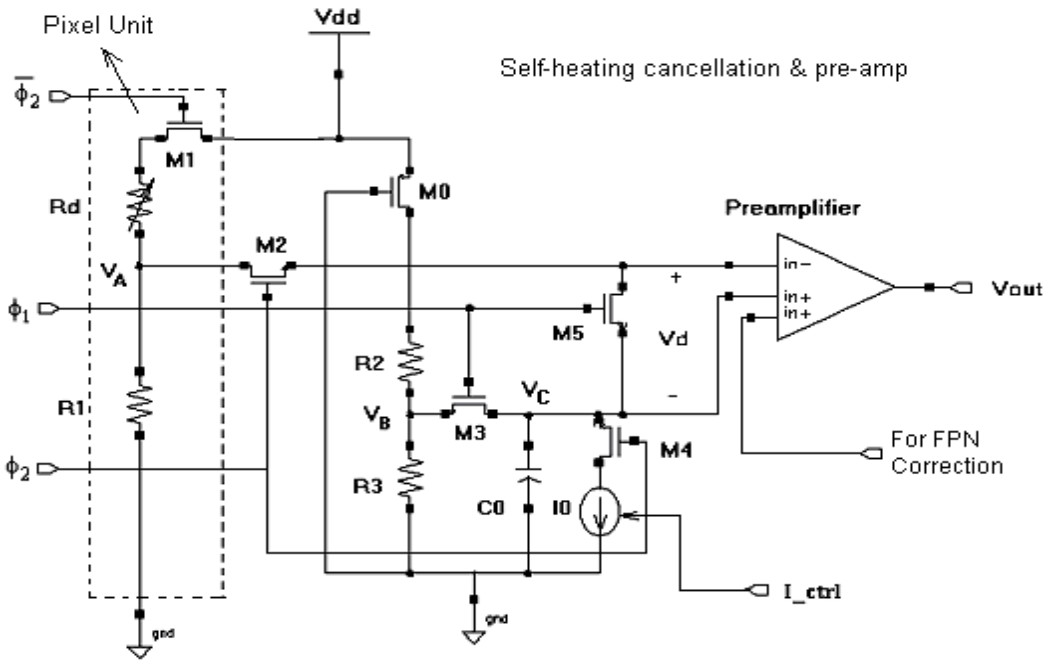


Fig. 4.6. The schematics of the tuneable self-heating cancellation circuit.

The current sink I_0 is implemented by a voltage-controlled cascode current mirror to achieve the high output impedance and accuracy. The cascode current mirror is tuneable through an external pin so that the ratio I_0/C_0 can be easily adjusted to ensure the complete bias-heating cancellation. Thus the discrepancy arising from the approximation made in the derivation of Eq.(4-7) and the accuracy of the thermal parameters is not important.

The output of the self-heating cancellation circuit is shown in the Fig. 4.7 with the gain of the preamplifier is set to be unity and infrared input is set be zero. The signal path from the fixed patter noise (FPN) correction circuit is disconnected. The cancellation of the self-heating can be clearly seen at the output. However, there is a small offset, about -2 mV, appearing at the output of the pre-amplifier. This offset can also be observed at the input of the preamplifier and is found to be caused by the non-ideal switches in the circuit. To achieve good self-heating cancellation, the sizes of these non-ideal switches must be optimized.

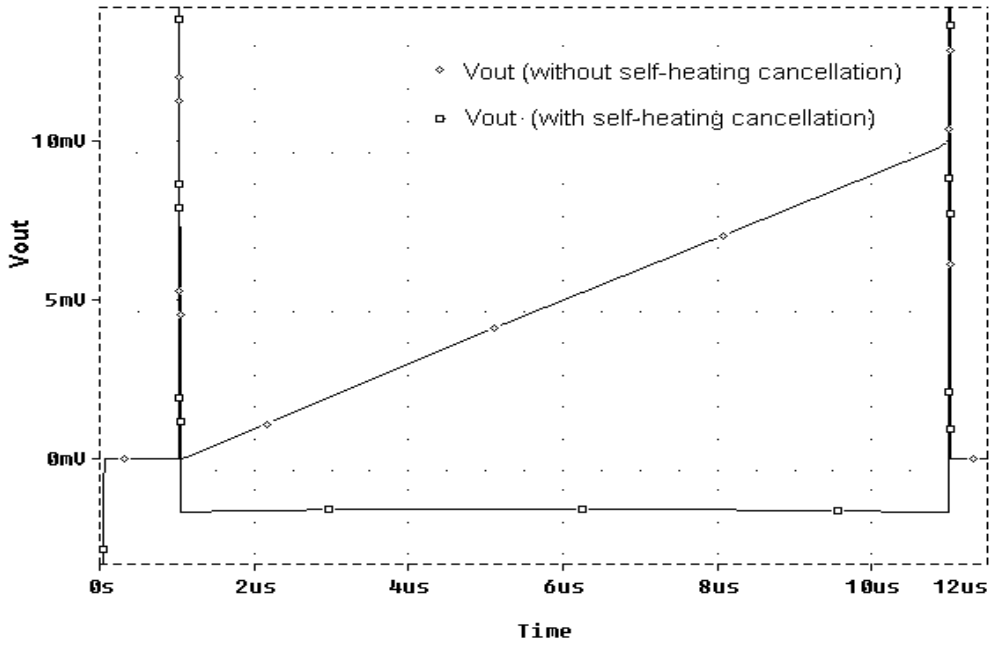


Fig. 4.7. Output of the implemented self-heating cancellation circuit with non-ideal switches.

4.2.2. Charge injection and clock feed-through

As mentioned in the last section, an offset is observed at the input of the preamplifier. Since the gate current of the MOS transistor is zero, there should be no current flow through the switch M2 an M3 to preamplifier. Thus, the offset cannot be due to the unequal resistance of the transistor M2 and M3. The size of M3 does affect the pre-

charging time of C_0. The large switch has a low ON-resistance, hence a small time constant. The post-layout simulation has showed that the pre-charging time will less than 0.1 μs when the NMOS switch M3 has the aspect ratio of as small as 2.6μm/1μm. This would have little effect to the frame rate of the self-heating cancellation circuit.

The other possible error source is the charge injection and clock feed-through since there are several switches connected to the input of the pre-amplifier. By observation, there are two switches, M2 and M5, connected to the inverting input of the preamplifier. They are controlled by the opposite clock signals. Thus, if both transistors have the same size, the clock feed-through and charge injection should be cancelled[137]. At the non-inverting input, there are three switches. M3 and M5 are controlled by a signal opposite to that on the gate of M4. Thus, the charge injection caused by two switches, M3 and M5, to this node is opposite to that of M4. When the size of M4 is approximately equal to the sum of that of M3 and M5, the charge injection should be cancelled.

The above analyses have been proved by the simulation as shown in the Fig. 4.9, where M3 and M5 have same size, while M4 is about twice of the M3 or M5. That is

$$\left(\frac{W}{L}\right)_{M4} = K\left(\frac{W}{L}\right)_{M3,5} \tag{4-8}$$

where $K \approx 2.3$. The charge injection is effectively compensated. In simulation, the infrared input power is set to zero, the aspect ratios of two PMOS switches were set to 20 μm/1μm, and the NMOS switch M2 is chosen to be the same size as M3. The bias period of the microbolometer is set to 10 μs.

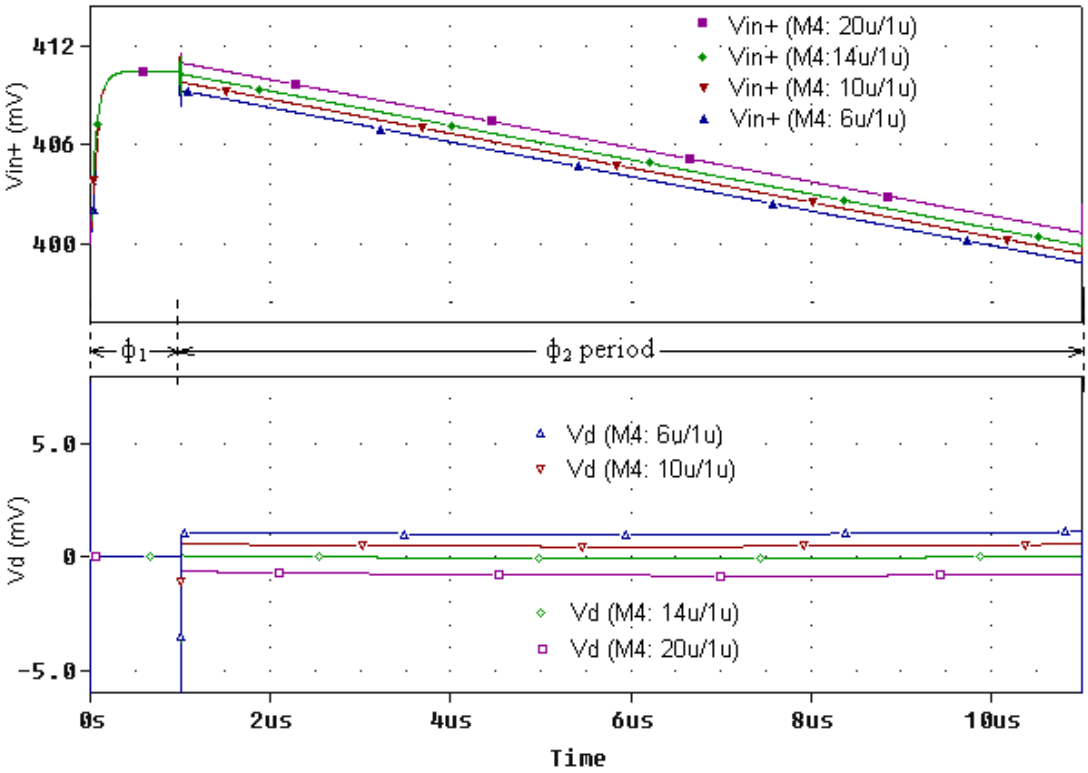


Fig. 4.8. Charge injection vs. different aspect ratio of M4. The upper plot shows non-inverting inputs of the preamplifier, while the lower plot shows differential inputs of the preamplifier, at the different aspect ratio of M4.

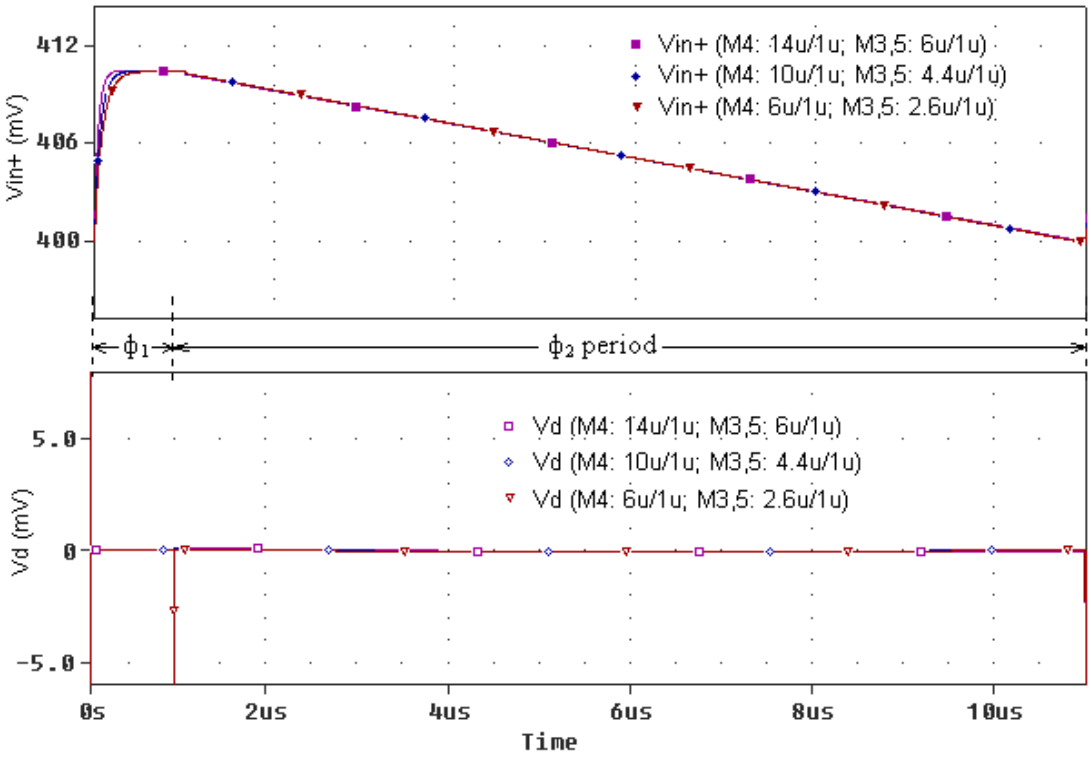


Fig. 4.9. Charge injection after the size of M4 is optimized. The upper plot shows non-inverting inputs of the preamplifier, while the lower plot shows differential inputs of the preamplifier, when size of M4 over M3, M5 are around 2.3.

4.2.3. Final simulation results

The overall self-heating cancellation simulation result is shown in Fig. 4.10. The circuit parameters used in the simulation are given in the Table 4.1. The room temperature resistances of microbolometer are selected according to the available two types of the single bolometers fabricated by Institute of Mircoelectronics, Singapore. The thermal parameters of the microbolometers are those from Table 3.3. The gain of the pre-amplifier is 5. The value of I_0/C_0 is calculated using Eq.(4-7), and slightly adjusted to achieve better self-heating cancellation performance. It can be seen from Fig. 4.10 the self-heating effect can be effectively cancelled and there is no offset.

Table 4.1. The circuit parameters after optimization

Circuit parameters	Values
Room temperature resistance of microbolometer 1	5 kΩ
Room temperature resistance of microbolometer 2	2.6 kΩ
Aspect ratio of M0 and M1	20 μm/1μm
Aspect ratio of M2, M3 and M5	2.6 μm/1μm
Aspect ratio of M4	6 μm/1μm
I_0, for microbolometer1	13.8 nA
I_0, for microbolometer2	29.6 nA
Capacitance C_0	20 pf

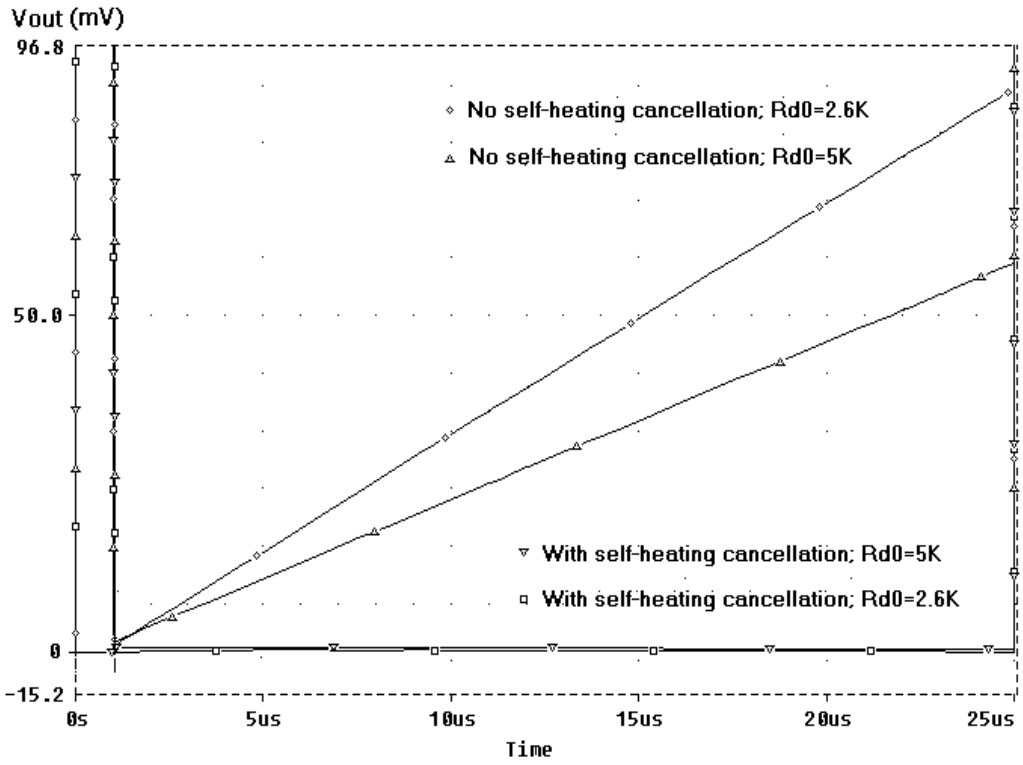


Fig. 4.10. Simulation results of optimized self-heating cancellation circuit.

4.3. Incorporation the voltage-mode self-heating cancellation into ROIC

In order to demonstrate the suitability of the self-heating cancellation scheme for the focal plane array, a readout IC for a 128 × 128 microbolometer FPA is designed. The architecture of the ROIC is shown in Fig. 4.11. Each pixel in the FPA comprises all the elements enclosed by the dash line in Fig. 4.6. Partially parallel readout structure is adopted, in which 16 columns are read out simultaneously to achieve longer signal integration time. A long integration time is essential for the low-noise design. To satisfy the requirement of most commercial applications, the frame rate of the imaging system should be higher than 30 Hz. For the 128 × 128 pixel FPA, the proposed partially parallel readout scheme has a readout duration for each pixel as

long as 16 μs for a 30 Hz frame rate, and 8 μs for 60 Hz frame rate. In the following simulation, the pixel readout duration is set to be 10.8 μs, which gives a frame rate of 45 Hz. All the column switches are implemented by a single-NMOS transistor. The on-chip clock generator provides all the necessary clocks for the ROIC. 128-row digital shift register and partial 16-column shifters are used to generate the pixel addressing signals, which drive the row and column switches, respectively. The frequency of the row select signals is 128 times higher than that of the column select signals so that the pixels in one column can be addressed row by row.

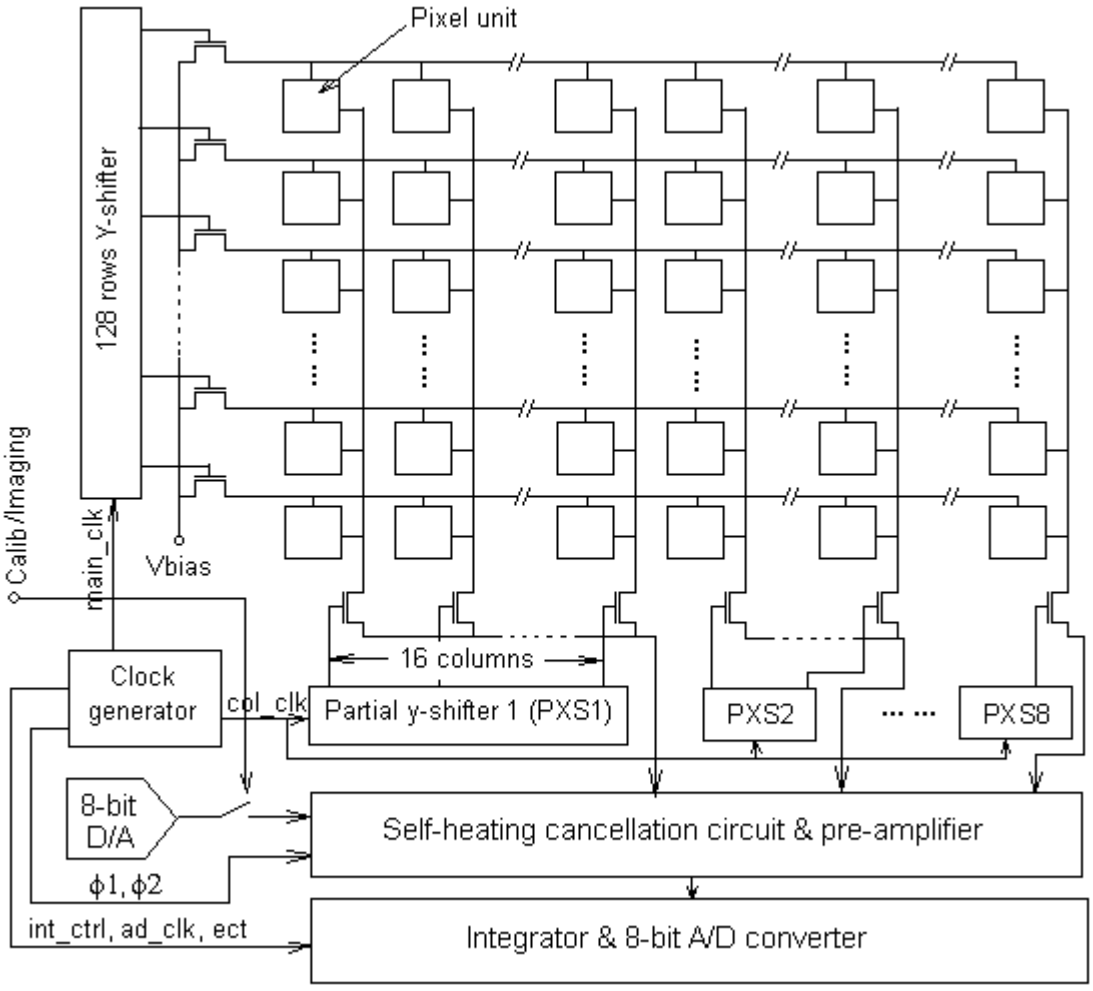


Fig. 4.11. Partially parallel readout architecture of the voltage-mode ROIC.

When a pixel is addressed, its output, generated by both infrared and bias heating, is fed to the inverting input of the differential pre-amplifier, as shown in Fig. 4.12. At the same time, the self-heating cancellation circuit generates a replica of the self-heating voltage which is applied to the non-inverting input under the control of the clock ϕ_1 and ϕ_2. Thus, the self-heating can be cancelled during the readout. In addition, the fixed pattern noise of FPA obtained during the initial calibration period under dark condition is also fed to the non-inverting input of pre-amplifier during readout for FPN cancellation. The output from the pre-amplifier should therefore contain neither self-heating effect nor FPN. The amplified infrared signal is further integrated and digitized by an 8-bit on-chip A/D converter. The on-chip 8-bit A/D and 8-bit D/A converters are selected from AMS (AustriaMicroSystems) analogLib library.

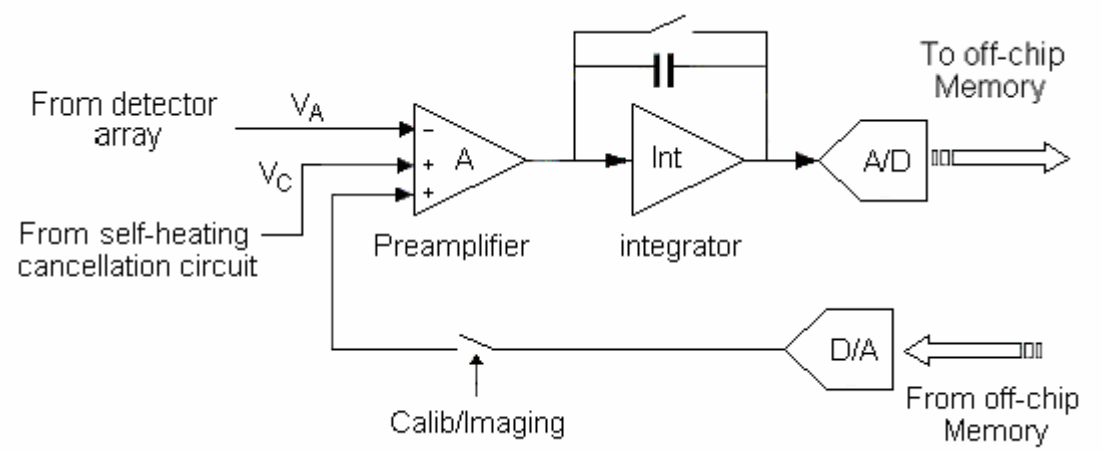


Fig. 4.12. Block diagram of the fixed pattern noise correction circuit.

4.3.1. Clock and control signals generation

All the clock and the control signals are generated on-chip with an external master clock signal. The clock generation circuit provides all the necessary clocks and

control signals for the self-heating cancellation circuit, amplifier, integrator, the on-chip A/D and D/A converters. The block diagram of the clock generation circuit is shown in Fig. 4.13. The *main_clk* generator block generates ϕ_1, ϕ_2, *main_clk* and *int_ctrl* from an external input clock. The *main_clk* is the pixel clock for the FPA. The row and column select clocks are generated by the addressing clock generator, using *main_clk* as the input clock. The addressing clock generator also produces a frame synchronization signal when the last pixel in the array is addressed. This synchronization signal is send to the off-chip circuitry and the imaging acquisition card to synchronize the operation of the entire system. A/D clock generator block generates the *ad_clk* and *ad_start* signals for the on-chip A/D converter.

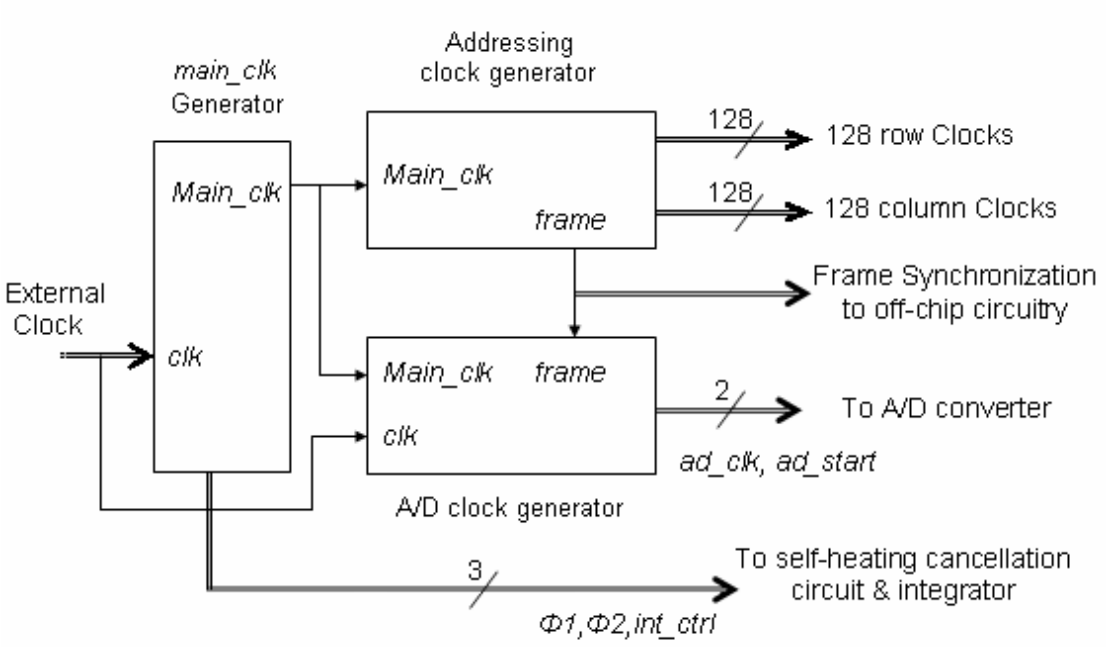


Fig. 4.13. Block diagram of clock and control signal generator.

4.3.1.1. Clock generator for *main_clk* and ϕ_1, ϕ_2

The clock generation circuit is shown in Fig. 4.14, where an external master clock,

clk, is used to derive all the internal clocks. Clock ϕ_1 and ϕ_2 are designed to define the bias and amplification period. This period is one master clock cycle shorter than the *main_clk* cycle so that before the microbolometer detector is biased there is enough time to pre-charge the capacitor C_0 in the self-heating cancellation circuit. The *int_ctrl* clock, which is generated for the on-chip integrator, is designed in such a way that it allows the signal integration to start at half *clk* cycle after the bias period and end at half *clk* cycle before. Hence, the transient noise from ϕ_1 and ϕ_2 can be avoided. The high period of the *int_clk* resets the integrator. An external reset signal is used to reset all the counters, shift registers and flip-flops to '0'. The simulation results are plotted in Fig. 4.15.

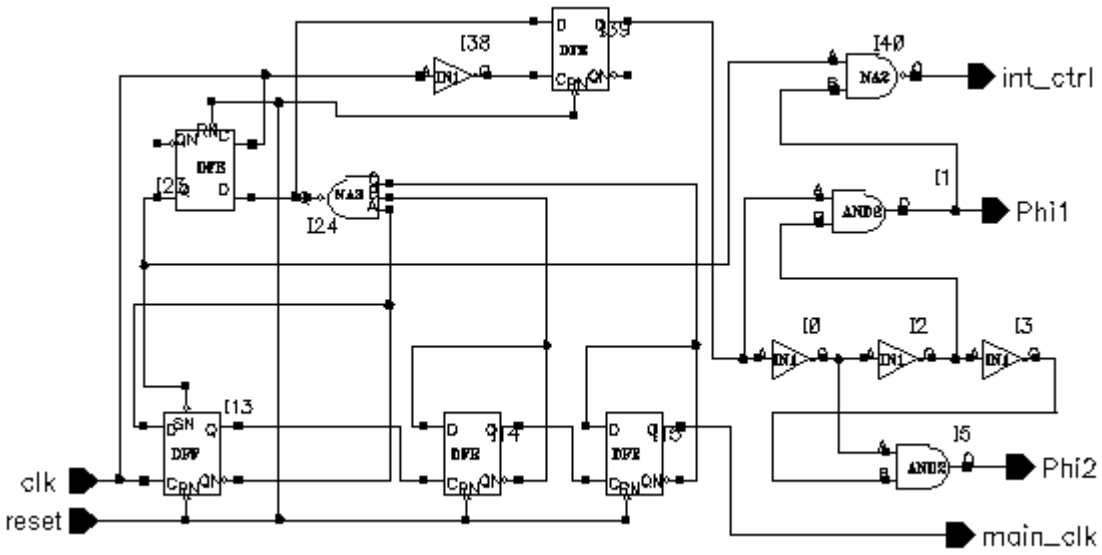


Fig. 4.14. Schematic of the pixel clock and control signal generator.

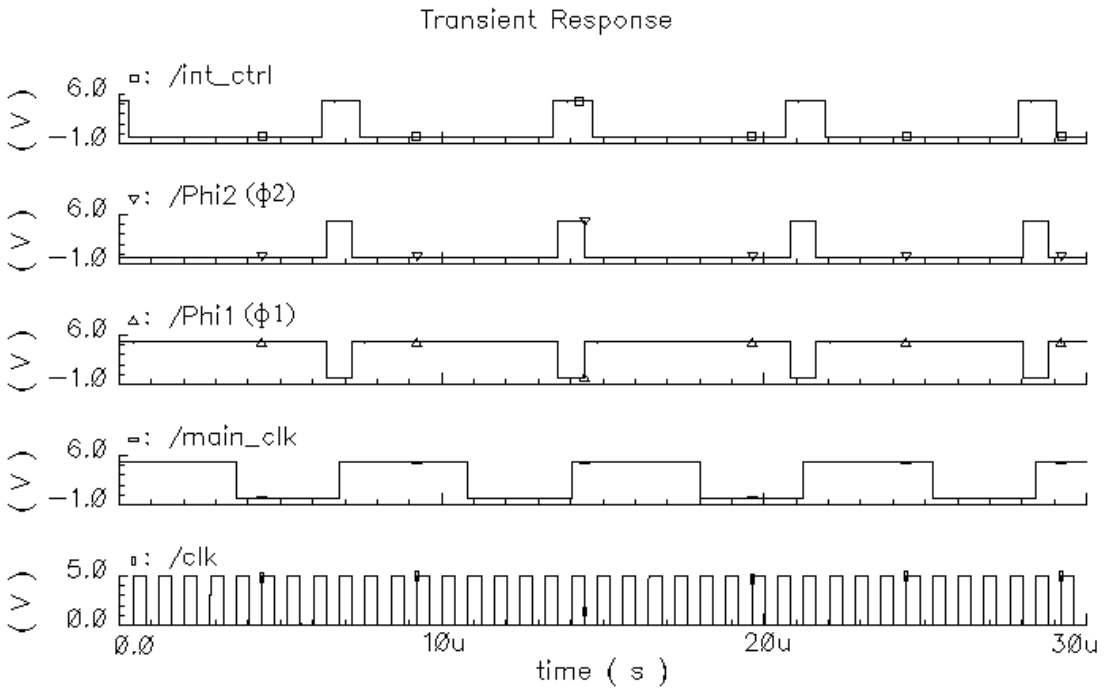


Fig.4.15. Waveforms of *int_ctrl*, ϕ_2, ϕ_1 *main_clk* and *clk*.

4.3.1.2. Clock generator for A/D converter

The A/D converter is controlled by two clock signals, *ad_clk* and *ad_start*. It requires 9 clock cycles to perform one data conversion. Among them, one cycle is for sample and hold, and the other 8 cycles are for converting the signal to 8-bit data. When *ad_start* is low, no conversion occurs. First rising edge of the *ad_clk* after the *ad_start* goes high will reset the ADC. At the second *ad_clk* rising edge, input signal is sampled and held. After the ninth clock cycle, the first data is valid at the output of ADC. Thus, conversion will repeat every 9 cycles while the *ad_start* is high.

The design of the *ad_clk* and *ad_start* signal generators should ensure that the converter is started while the first pixel is read out and the signal should be sampled and held after a considerable period of integration. In the circuit illustrated in Fig.

4.16, the frame signal, which is logic high when the last pixel in FPA is reading, is used to make the *ad_start* active at the start of the seventh cycle after the first frame. The *ad_clk* is obtained by inversing the external input clock, *clk*, so that its second rising edge after *ad_start* will be half cycle before the end of the integration period. Fig. 4.17 shows the timing waveform of the related signals.

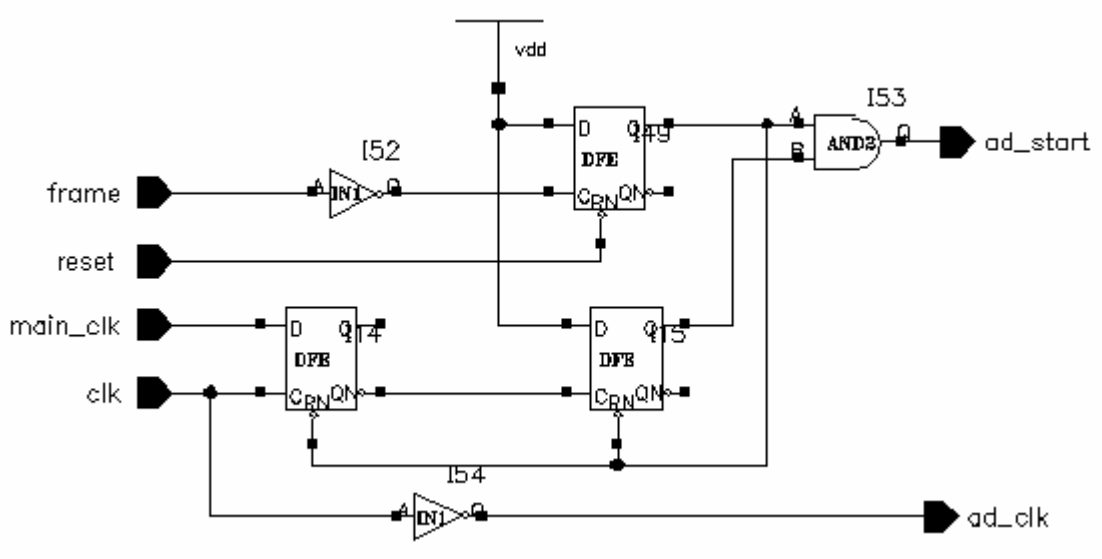


Fig. 4.16. Schematic of the *ad_clk* and *ad_start* signal generator.

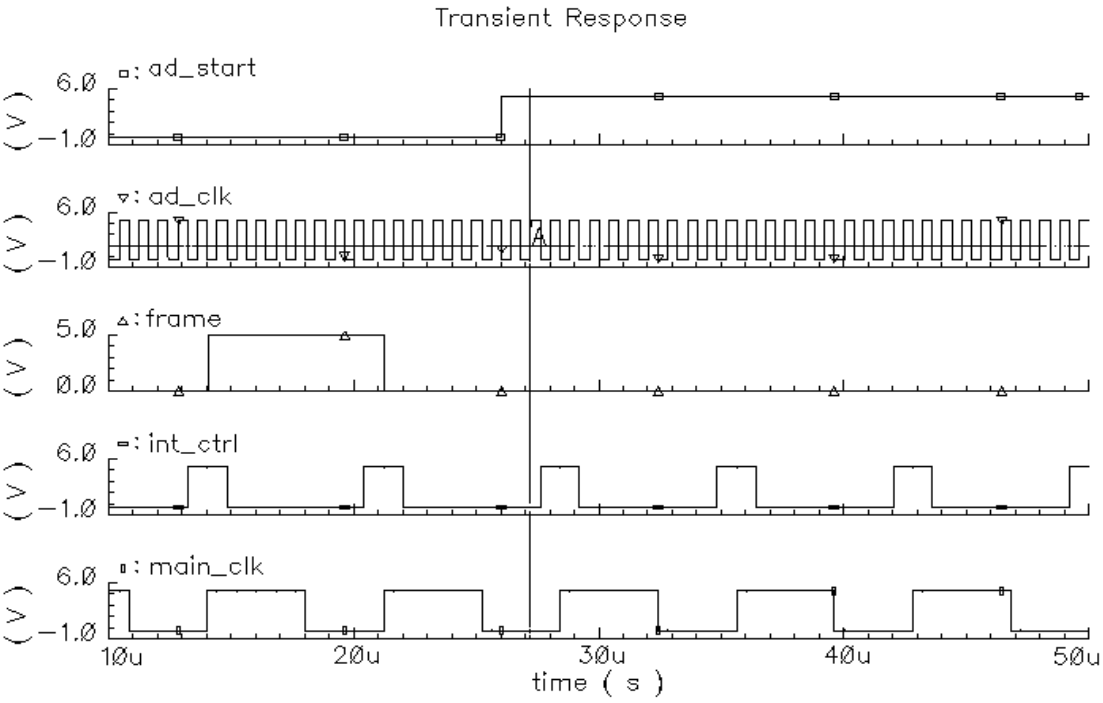


Fig. 4.17. Timing waveforms of *ad_start*, *ad_clk, frame, int_ctrl* and *main_clk.*

4.3.1.3. Pixel addressing signal generation

The pixels in the FPA are addressed by the row and column select signals. The circuit used to generate the addressing clocks is shown in Fig. 4.18. Row addressing is accomplished by a 7-bit cyclic synchronous counter, a 7-input NOR gate and a 128-bit shift register (y-shifter). The output of the NOR7 gate is set to high when all the outputs of the 7-bit counter are low. Thus, for every 128 *main_clk* cycles will output a pulse. The pulse propagates through the y-shifter at every rising edge of the *main_clk* and generates the row select signals.

Column select signals are generated in a similar way as the row select signals. The last bit output of the 7-bit counter, Q6, is inversed and used as the clock of the 4-bit cyclic counter so that the output of NOR4 gate becomes high for 128 *main_clk* cycles and repeats every 2048 *main_clk* cycles (16 cycles for *col_clk*). The 16-bit partial x-shifter shifts the output of the NOR4 gate and generates the column select pulses. Since there are 128 columns in the microbolometer focal plane array, eight same partial x-shifters operate at the same time under the control of the *col_clk* and the output from the NOR4 gate.

The frame pulse is obtained at the end of each frame by ANDing the last row and last column select signals. This signal is used to control the start of the A/D conversion and to synchronize the off-chip circuitry of the overall IR imaging acquisition system.

Fig. 4.19 and 4.20 show the timing waveforms of the first 6 row select signals and 6 column-select signals, respectively.

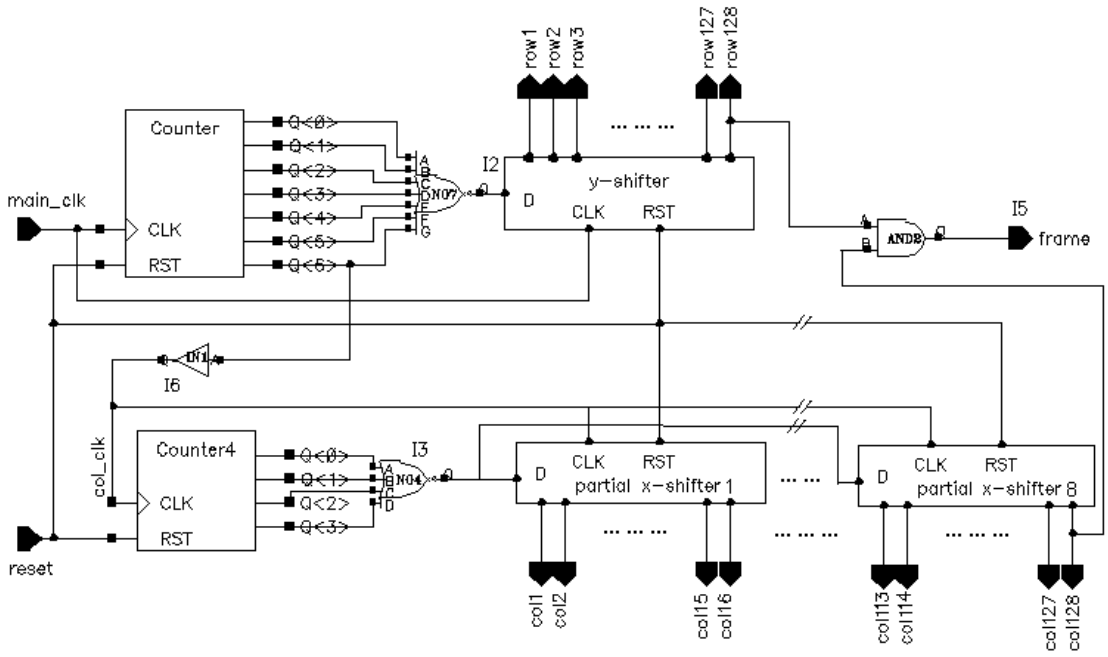


Fig. 4.18. Schematic of the X-Y scanning clock generator.

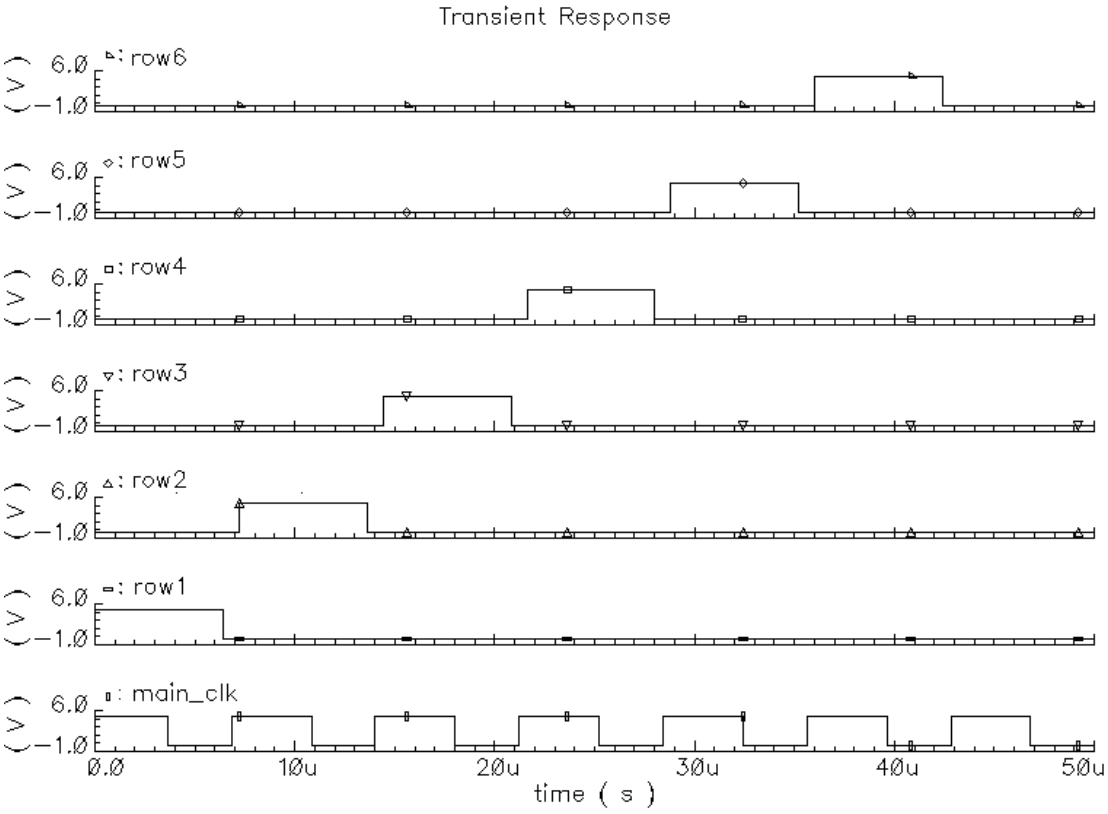


Fig. 4.19. Waveforms of the scanning clocks of the first 6 rows and *main_clk*.

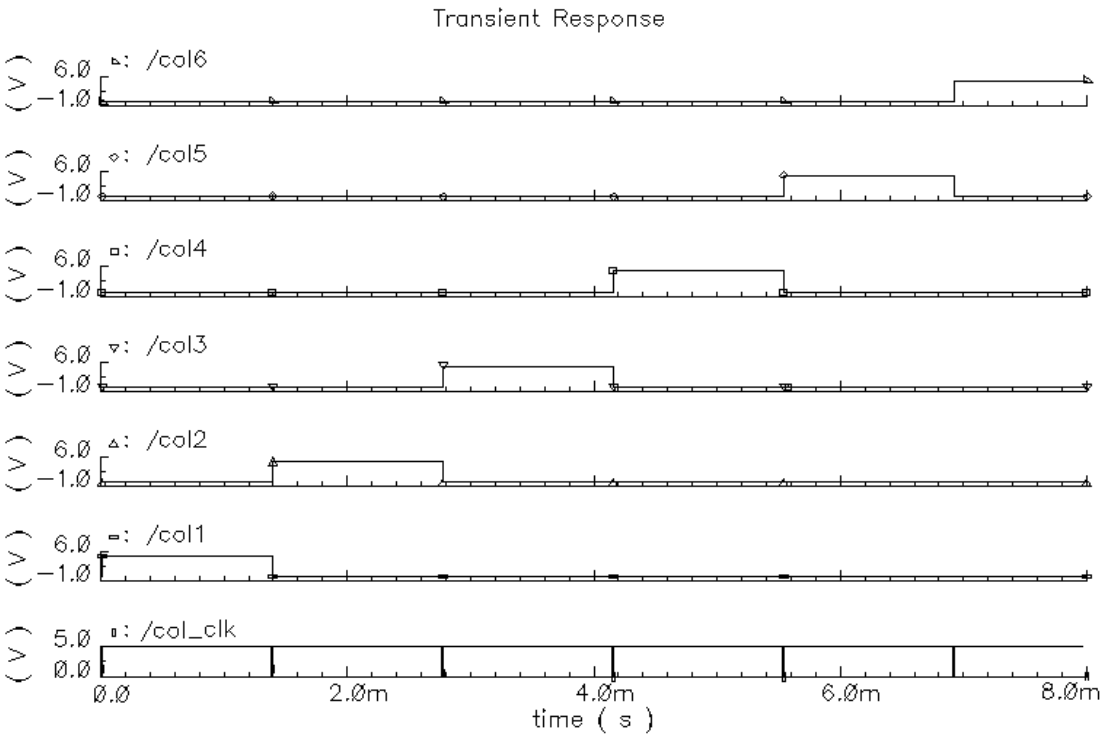


Fig. 4.20. Waveforms of the scanning clocks of the first 6 columns and *col_clk*.

4.3.2. Pre-amplifier design

A typical pre-amplifier for microbolometer readout circuits must amplify the input signal to a required level with very low noise, since the signal from the bolometer can be as low as 3 μV. Furthermore, to satisfy the requirements of the 30 Hz frame rate for a 128 × 128 microbolometer array, the gain bandwidth (GBW) of the preamplifier should be larger than 500 kHz. For the partial parallel readout, the GBW of 100 kHz is accepted. The differential input range of the preamplifier should cover the FPN of the FPA. The FPN, caused by the variation of bolometer resistance, is typically within ± 10% of the nominal value. In our design, the nominal value of microbolometer resistance at the room temperature is 5 kΩ, which leads to the FPN of ± 100mV. The common mode range of the preamplifier can be from 0.3 V to 3.0 V.

The lower limit of the common mode range is critical because the resistors in the lower arms of the Wheatstone bridge could be only one tenth of the microbolometer resistance. The offset is another important parameter for preamplifier. It should be limited to several microvolts level. Since the settling time of switching from one pixel to another must be shorter than the ϕ_1 period, the slew rate of the preamplifier should also be higher than 1 V/μs if the amplifier gain is higher than 2. In summary, the requirements of the preamplifier lead to the following specifications:

1) GBW > 0.8 MHz
2) Differential input range > ± 150 mV
3) Common mode input range from 0.2 to 3.5 V
4) Input referred offset < 10 nV (adjustable)
5) Integrated noise level from DC to 500 kHz < 3 μV;
6) Slew rate > 2 V/μs

The pre-amplifier is a two-stage operational amplifier shown in the Fig. 4.21. In order to satisfy the design specifications, several design considerations have to be taken into account. For the implementation of low-noise preamplifier, PMOS differential input stage is used. Since the PMOS input transistors must be kept in saturation region for a common-mode input level near the ground rail for single power supply operation, the common-mode input range requirement can be easily achieved with a PMOS input stage. The output stage is a common-source high gain stage with low output impedance and high drive current.

To reduce the flicker noise, the gate length of 8 μm is used for the input transistor M0 and M1, and 10 μm for active load M2 and M3. Long channel length also provides

good matching characteristics and hence reduces the input offset. The differential input stage is biased by a current source which consists of M4, M5, M6, M7, and generates around 100 μA current to the tail of the input transistor pair. Two small resistors R1, R2 are added between the sources of M2, M3 and ground, respectively, for external offset adjustment. The values of R1 and R2 are designed to make the systematic DC offset of the amplifier as low as possible. Transistor M8 ~ M12 are added to form the push-pull output stage. The frequency response and the stability of the amplifier are ensured by the Miller capacitor, *Cc,* and the nulling resistor, *Rc*.

Since the offset in operational amplifiers not only comes from the systematic design, but also from the imperfect fabrication of matched devices, careful layout of the matched devices is planed in the design to reduce process-related offset. The common-centroid cross-coupling layout strategy together with double guard rings is adopted for critical devices. All the devices that need to be matched were arranged in close proximity to minimize the effect of spacing-dependent parameter mismatch. These include the input pair, active loads and current mirror sources. The layout of the preamplifier is shown in Fig. 4.22.

The overall post-layout performance of the preamplifier, simulated with 5 V power supply and a 5 pf capacitor load, is summarized in the Table. 4.2. The input referred noise is integrated over the bandwidth of the preamplifier since there is no filter in the readout circuit.

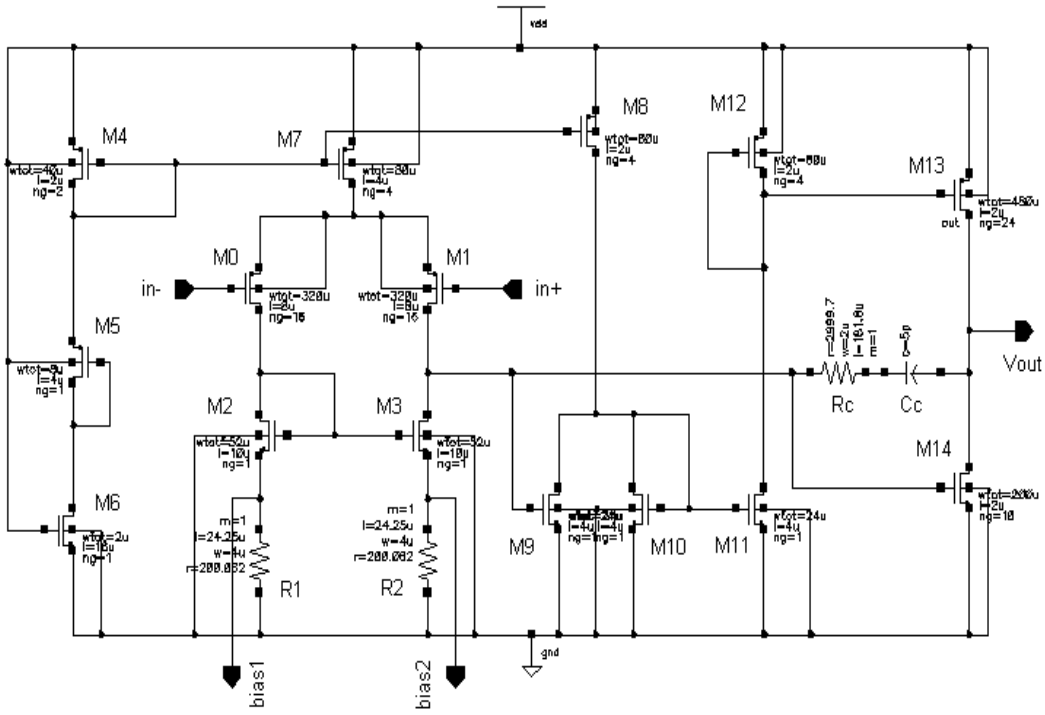


Fig. 4.21. Schematic of the pre-amplifier.

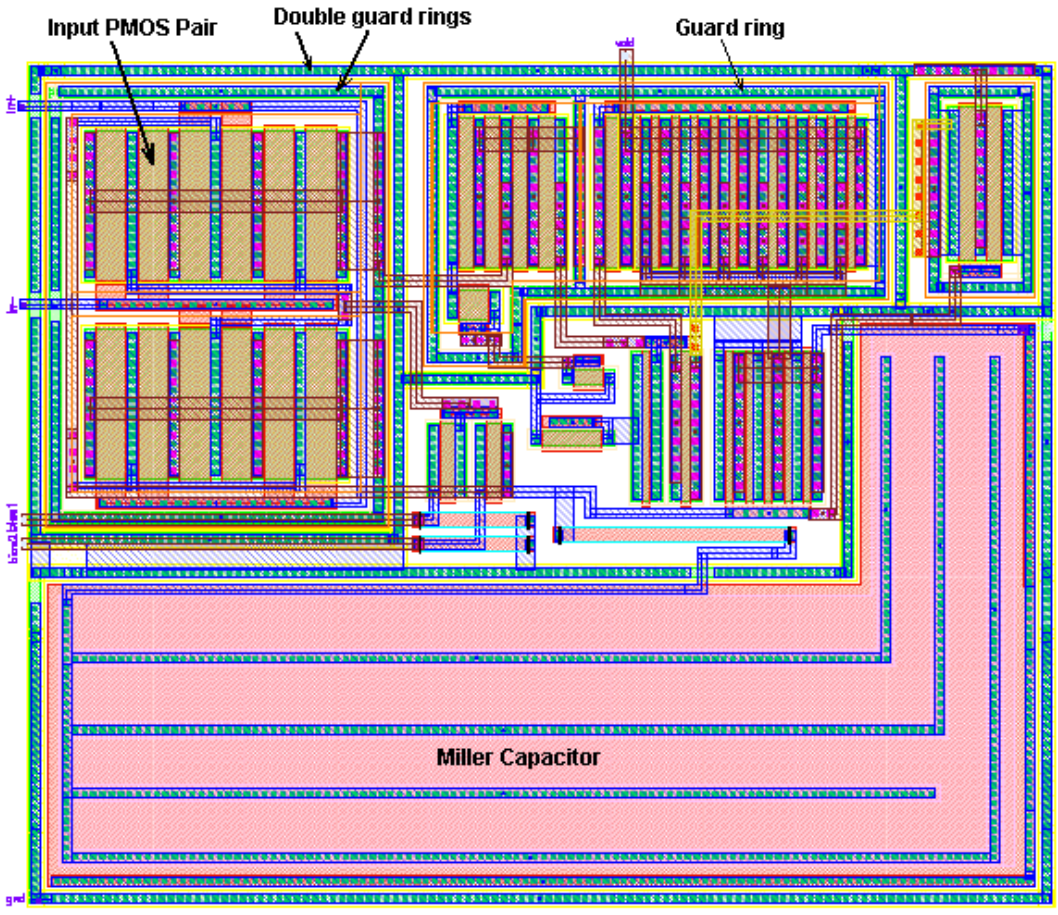


Fig. 4.22. Layout of the preamplifier.

Table 4.2. Post-layout Simulated pre-amplifier parameters

Parameters	Results
DC gain	107.3 dB
GBW	4.6 MHz
Phase margin	82 degree
Input referred offset	5.98 nV
Positive slew rate	6.4 V/μs
Negative slew rate	-6.2 V/μs
Noise @ 1 kHz	32 $nV/\sqrt{Hz}$
Input referred noise integrated @ 1 Hz ~ 4.6 MHz	1.2 μV
Core preamplifier area	112 × 137 μm^2
Power consumption	8 mW

4.3.3. Fixed pattern noise correction

The fixed pattern noise is caused by the spatial non-uniformity in the infrared focal plane array. The existence of the spatial non-uniformity is due to the variation in the fabrication process. In a large focal plane array, the non-uniformity from pixel to pixel can be significantly larger than the signal due to incident infrared. Therefore, it must be corrected in the readout circuit. The schematic of the FPN correction circuit is shown in Fig. 4.23.

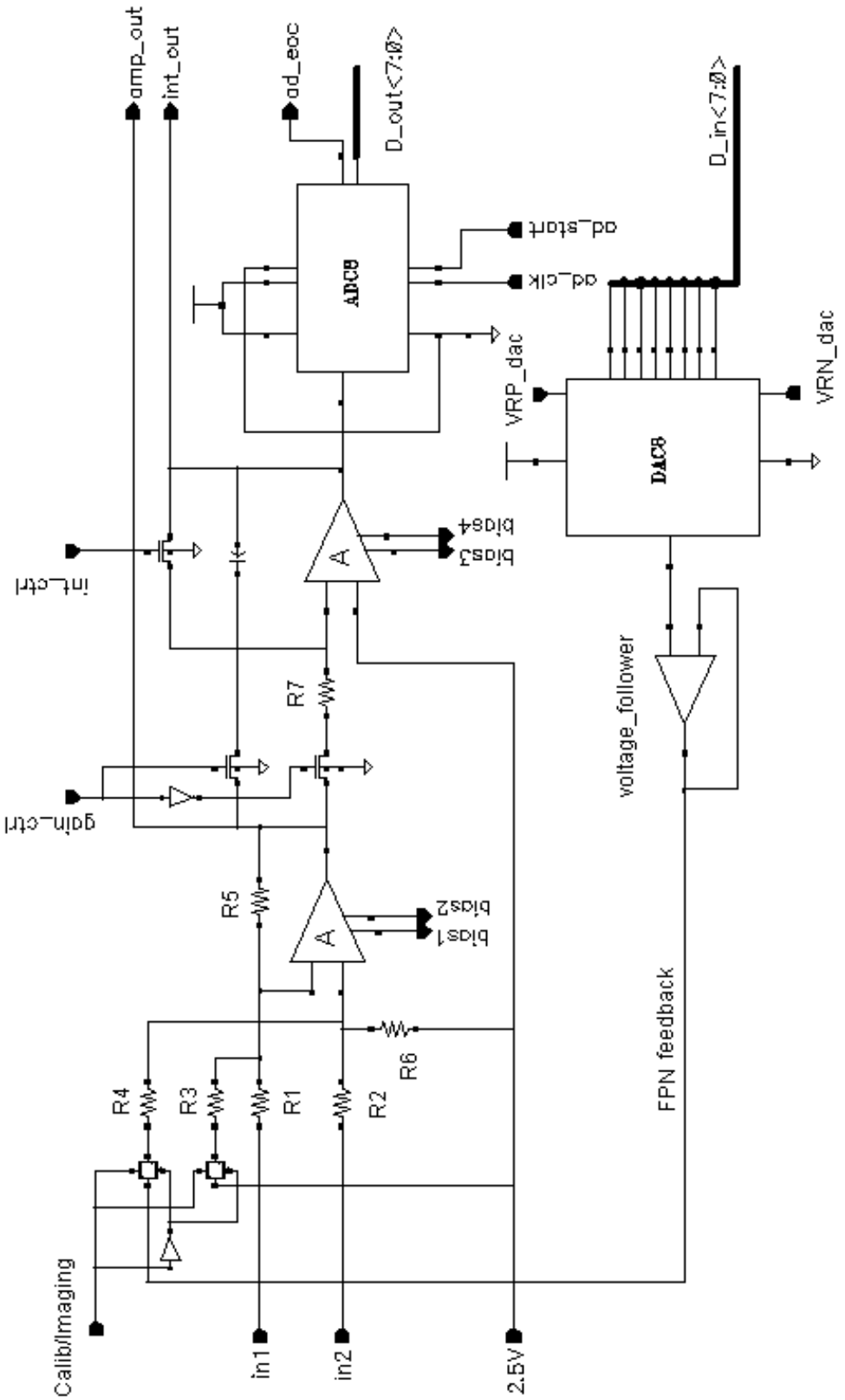


Fig. 4.23. Schematic of the FPN correction circuit.

There are two operation modes in this circuit, namely, the calibration and imaging mode. When in calibration mode, the detector array is shielded from IR incident. The FPN feedback path from the output of D/A converter is disconnected by the transmission gates that is controlled by signal *Calib/Imaging*. The fixed pattern noise of the focal plane array is then read and sent to the inverting input of the preamplifier. At the same time, the replicated the self-heating signal is fed to the non-inverting input of the pre-amplifier. Thus, the self-heating effect is removed and leaves only the FPN at output of the pre-amplifier. The FPN is then integrated, digitized by an on-chip 8-bit A/D converter, and stored in an off-chip memory. During the imaging mode, the transmission gates are open. The 8-bit on-chip D/A converter reads the FPN from the off-chip memory and sends them back to the input of the pre-amplifier. The preamplifier operates similar to a subtracter, subtracting the self-heating noise and fixed pattern noise from the readout signals from the FPA. Thus, both self-heating and FPN can be cancelled at the input of the pre-amplifier. The output signal of the pre-amplifier with a small residual FPN is then digitized for further fine off-chip correction.

To achieve a Noise Equivalent Temperature Difference (NETD) better than 100 mK, the FPN correction with at least 16-bit resolution is needed. In our design, only 8-bit coarse FPN correction circuit is built on chip. The fine correction will be performed off-chip.

The pre-amplifier described in the section 4.3.2 is adopted to implement all amplifiers in the FPN correction circuit. The values of $R_1 \sim R_6$ are selected according to the following equations.

$$\begin{aligned} R_1 &= R_2 \\ R_3 &= R_4 \\ R_5 &= R_6 \\ \frac{R_5}{R_3} &= \frac{1}{\left|Gain_{\text{int}}\right| \times Gain_{ADC} \times Gain_{DAC}} \end{aligned} \tag{4-9}$$

One of the important factors, which must be considered in selection of the resistor values, is that the integrator stage cannot be saturated when circuit is working in the calibration mode. Therefore the ratio $\frac{R_5}{R_1}$ is chosen to around unity.

The external *gain_ctrl* pin controls the time constant of the integrator so that different time constants can be set for the calibration and imaging operation, respectively, and the full dynamic range of the integrator can be utilized for the small signal after FPN correction.

Post-layout simulation of the circuit in Fig. 4.23 had been run with a FPN input between pin *in1* and *in2* fed to the amplifier. Considering the ±100 mV variation, which equivalent to a ± 10% non-uniformity in the microbolometer FPA, and other variation from the circuit fabrication process, the maximum input FPN range is set to ±130 mV. A voltage source is used in simulation to generate the FPN input. The digitized FPN is saved when circuit operates in calibration mode and the FPN feedback from DAC is disconnect. In the imaging mode, the saved FPN data is the input to *Din<7:0>* so that the residual FPN can be observed at the output of the pre-amplifier. The simulation is repeated with the simulated FPN stepped from -130 mV to 130 mV and results are shown in the Fig. 4.24. After the correction, the FPN can be reduced to less than ± 400 μV for the maximum input FPN range of ±130 mV. In the simulation, the self-heating block is disabled.

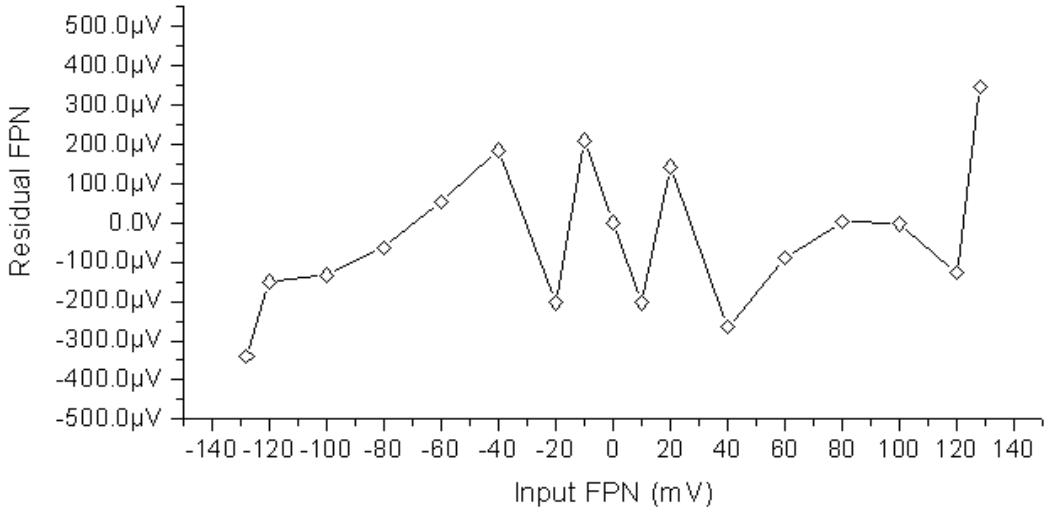


Fig. 4.24. Simulation results of fixed pattern noise correction.

4.4. Summary

A new self-heating cancellation technique for microbolometer readout circuits based on equivalence of thermal capacitance and electrical capacitor is described. With the proper chosen values, a current and capacitor pair can be used to generate a replica of the self-heating. The design equations for determining the value of the current source and capacitor have been derived. The self-heating cancellation circuit is optimized and simulation results show that an effective self-heating cancellation can be achieved. The tuneable feature of the cancellation has also been demonstrated.

A partial parallel voltage readout integrated circuit for microbolometer focal plane array is proposed based on the new self-heating cancellation technique. 8-bit on-chip A/D and D/A converters form the coarse FPN correction circuit. An 8-bit correction has been achieved using the fixed pattern noise correction circuit. Although the ROIC is demonstrated for a 128 × 128 microbolometer FPA, it can be easily extended to a focal plane array with a larger dimension.

Chapter 5. Readout IC for Microbolometer with Current-mode Self-heating Cancellation

In currently available state-of-the-art IR FPA readout circuits, noise requirement is more and more strict so that the system sensitivity can be further enhanced. Comparing with the voltage-mode readout circuit, current-mode circuit shows its good noise immunity. However, there is no self-heating cancellation circuit reported for current-mode microbolometer readout circuits. In this chapter, a current-mode readout circuit with both of self-heating noise cancellation and FPN correction is presented. The concept of using the electrical equivalence of the thermal system to generate the replica of self-heating effect in voltage-mode readout circuits is extended to the current-mode readout circuits. The cancellation of the self-heating is demonstrated by both simulation and experiment. An on-chip 8-bit current-steering D/A converter is designed to perform the coarse correction of the FPN.

5.1. Current-mode self-heating cancellation circuit

The proposed current-mode self-heating cancellation circuit is based on the same concept as that described in the voltage-mode cancellation circuit, that is, the equivalence between electrical and thermal capacitance. The details are described in the following sub-sections.

5.1.1. Current-mode self-heating cancellation scheme

The schematic of the current-mode microbolometer self-heating cancellation circuit for single microbolometer is shown in Fig. 5.1 [138]. R_d represents the microbolometer. R_1 is a fixed-value resistor whose resistance is equal to the room temperature resistance of R_d, R_{d0}. M1 is used to balance the ON-resistance of M0 and is set to always on. Three unity gain cascade current mirrors, (M2 ~ M5), (M6 ~ M9) and (M10 ~ M13) form the current subtraction circuit. The output current of the current mirror (M2 ~ M5) is set by the microbolometer R_d, while the output current of another current mirror (M6 ~ M9), which is completely identical with the current mirror (M2 ~ M5) to obtain the well matched structure, is set by the resistor R_1. The current output from (M10 ~ M13) is equal to current I_d. Assuming the ramp current generator generates the replica of the self-heating effect of I_d, the differential output current should be equal to the difference between I_d and the sum of I_{ref}, the DC current of I_d, and I_{ramp}, the replica of self-heating noise, and contain only infrared signals. The differential current is fed to a subsequent current integrator.

The circuit of the ramp current generator is depicted in Fig. 5.2. The switches are controlled by the two-phase non-overlapping clock ϕ_1 and ϕ_2. When clock ϕ_1 is high and ϕ_2 low, the microbolometer is not biased. At same time, M14 is on and the capacitor C_0 is pre-charged to a voltage, which is equal to the drain voltage of M6, V_{D6}. Controlled by the complementary signal of ϕ_2, M15 is off. Therefore, V_{DS} of M17 is approximately equal to zero. While clock ϕ_2 becomes high and ϕ_1 low, switch M0, M15 and M16 are on, and the bolometer R_d is biased. Under the assumption of a metal-film bolometer, R_d increases due to the self-heating effect, resulting in the decrease of I_d. The operation amplifier in Fig. 5.2 is used to track the voltage on the capacitor C_0 and feed it to the drain of M17. Since M14 is off but M16 on, I_0 is discharging C_0 so that the drain voltage of M17 is linearly decreasing while its source

voltage remains unchanged and is equal to V_{D6}. Note that V_{D6} is mainly determined by I_{ref} since I_{ramp} is very small. The drain source voltage of M17, - $I_0/C_0\,t$, is designed to much lower than the threshold voltage of the PMOS transistor so that M17 is operating in the triode region. With correctly chosen values for C_0 and I_0, the ramp current can have the same gradient as the self-heating current of the microbolometer, I_d. Thus, a current-mode replica of self-heating is obtained.

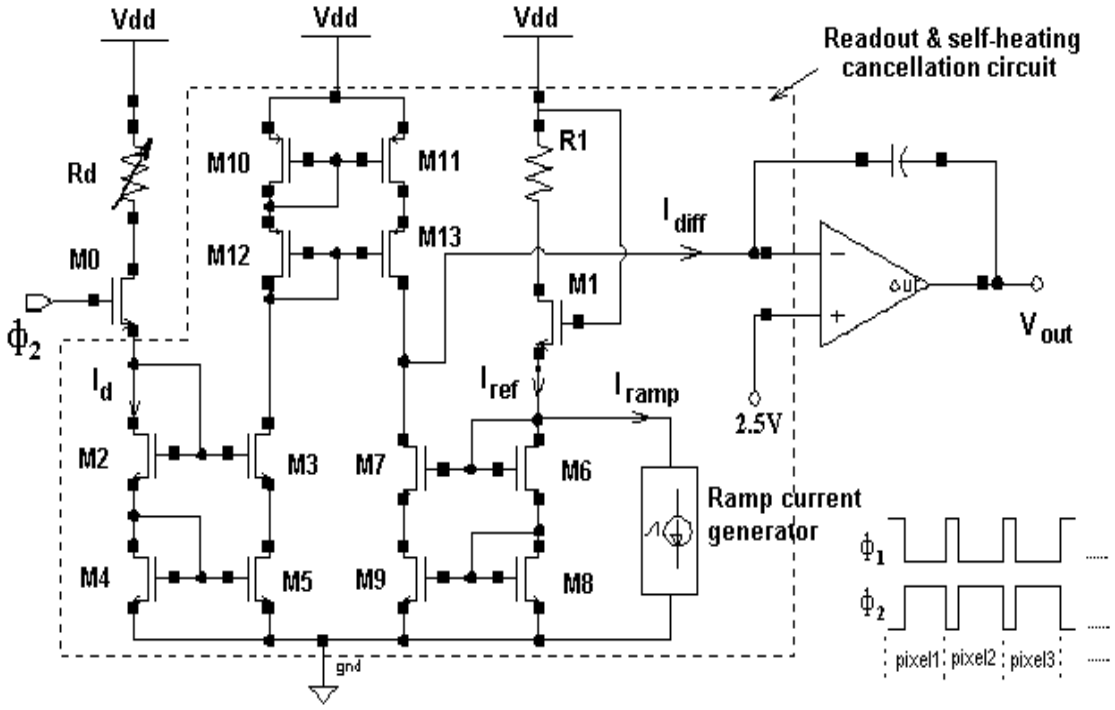


Fig. 5.1. Schematic of the current-mode self-heating cancellation circuit.

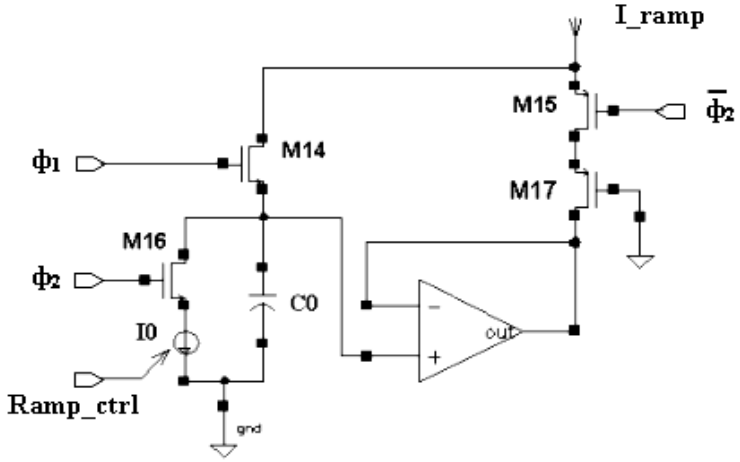


Fig. 5.2. Schematic of the ramp current generator.

5.1.2. Determination of the capacitor and current values

During readout, the resistance change of a metal-film microbolometer is equal to $R_{d0}\alpha\Delta T$. Assuming there is no IR incident input and the ΔT is only caused by the microbolometer's self-heating effect, ΔT can be derived when the bias period is much shorter than the thermal time constant of the microbolometer.

$$\Delta T(t) = \frac{P_{bias}}{H} t \tag{5-1}$$

For the circuit shown in Fig. 5.1, the P_{bias} can approximately be written as

$$P_{bias} = \frac{(V_{dd} - V_{D0})^2}{R_d} = \frac{(V_{dd} - V_{D0})^2}{R_{d0}(1 + \alpha\Delta T)} \tag{5-2}$$

where V_{dd} is bias voltage and V_{D0} is the drain voltage of the M0.

The drain source current of the transistor M2 and M4, I_d can be written as

$$\begin{aligned} I_d(t) &= \frac{V_{dd} - V_{D0}}{R_d} \\ &= \frac{V_{dd} - V_{D0}}{R_d} \cdot \frac{R_d - R_{d0}\alpha\Delta T(t)}{R_{d0}} \\ &= \frac{V_{dd} - V_{D0}}{R_{d0}} - \frac{(V_{dd} - V_{D0})R_{d0}\alpha}{R_d R_{d0}} \cdot \frac{P_{bias}}{H} \cdot t \\ &= \frac{V_{dd} - V_{D0}}{R_{d0}} - \frac{(V_{dd} - V_{D0})^3 R_{d0}\alpha}{H \cdot R_d{}^2 R_{d0}} \cdot t \\ &\approx I_{ref} - \frac{(V_{dd} - V_{D0})^3 \alpha}{H \cdot R_{d0}{}^2} \cdot t \qquad (R_d \approx R_{d0} \text{ since } \alpha\Delta\text{T} << 1) \end{aligned} \tag{5-3}$$

The drain source current of the transistor M6 and M8 is equal to $I_{ref} - I_{ramp}$. Assuming current mirrors are matched, the output current of the current subtracter can be expressed as

$$I_{diff} = I_d - (I_{ref} - I_{ramp}) \tag{5-4}$$

I_{ramp} is the drain current of M17, which linearly depends on its V_{DS} when operating in the triode region and can be written as

$$\begin{aligned} I_{ramp} &= -\mu_p C_{ox}(\frac{W}{L})_{17}\left|V_{GS}-V_{TH}\right|\cdot V_{DS} \\ &= -\mu_p C_{ox}(\frac{W}{L})_{17}\left|V_{GS}-V_{TH}\right|(V_{D6}-\frac{I_0}{C_0}t-V_{D6}) \\ &= \mu_p C_{ox}(\frac{W}{L})_{17}\left|V_{GS}-V_{TH}\right|\frac{I_0}{C_0}t \end{aligned} \tag{5-5}$$

where μ_p is the hole mobility, C_{ox} is the gate oxide capacitance per unit area, $(W/L)_{17}$ is the aspect ratio of M17 and V_{TH} is the threshold voltage. When there is no infrared incident input and if the self-heating is completely cancelled, I_{diff} should be equal to zero. Substituting Eqs. (5-3) and (5-5) into (5-4), and let $I_{diff} = 0$, it yields

$$\frac{I_0}{C_0} = \frac{(V_{dd}-V_{D0})^3\alpha}{H\cdot {R_{d0}}^2}\cdot\frac{1}{\mu_p C_{ox}(\frac{W}{L})_{17}\left|V_{GS}-V_{TH}\right|} \tag{5-6}$$

In other word, if Eq.(5-6) is satisfied, the ramp current can successfully compensate the self-heating effect.

The current source I_0 can be implemented by an adjustable current-sink so that the gradient of the ramp current can be adjusted through an externally voltage-controlled pin. M17 can also be replaced by a resistor, but with an area penalty. The use of PMOS transistor M17 can provide another mean to tune the ramp current if its gate voltage is made adjustable.

5.1.3. Functional verification

The functionality of the current-mode self-heating cancellation circuit has been verified by SPICE programs. In simulation, R_d is replaced with a microbolometer model. The period of the pixel clock is set to 10 μs. The bias period (ϕ_2 period) of

the microboloemeter detector is 9.5 μs in simulations. The results of the simulation show that 0.5 μs is long enough to pre-charge the capacitor C_0. When C_0 is designed to be 10 pf, the ϕ_1 period can be further decreased to around 0.2 μs to increase the bias period of detectors. The IR incident power per pixel is set to zero so that self-heating effect and its cancellation can be clearly observed. The microbolometer related parameters used in simulation are set as in Table 3.3. Process related parameters in Eq.(5-6) are based on the device models from the AMS 0.6-μm CMOS double-poly triple-metal process. Other circuit parameters are listed in Table 5.1. Care should be taken when choosing the sizes of the switch transistors, M14 ~ M16. The charge injection effects similar to that occurred in the voltage-mode self-heating cancellation circuit should be avoided.

Table 5.1. Current-mode self-heating cancellation circuit parameters in simulation

Circuit parameters	Values
R_{d0}, R_1	5000 Ω
Aspect ratios of M2, M3, M6, M7	400.5μ/3μ
Aspect ratios of M4, M5, M8, M9	400μ/3μ
Aspect ratios of M10, M11	800μ/3μ
Aspect ratios of M12, M13	618μ/3μ
Aspect ratio of M14, M16	11.2μ/0.6μ
Aspect ratio of M15	12μ/0.6μ
Aspect ratio of M17	29.6μ/5μ
C_0	10 pf
I_0 (after tunning)	18 nA
V_{dd}	5 V

The simulation results in Fig. 5.3 shows that after proper cancellation, the current I_{diff} is almost zero within whole bias period. The self-heating is effectively cancelled using the proposed current-mode cancellation circuit. The ratio I_0/C_0 can be tuned by

I_0 through the *Ramp_ctrl* pin to achieve complete self-heating cancellation. Fig. 5.4 shows the tuneable feature of the ramp current generator, where I_0 is tuned to be 25.2 nA, 18 nA and 10.8 nA. The slope of I_{ramp} is therefore changed according to I_0. The tuneable feature ensures a good self-heating cancellation since errors from assumptions made in deriving Eq.(5-6) and the variation of the process parameters are tolerable.

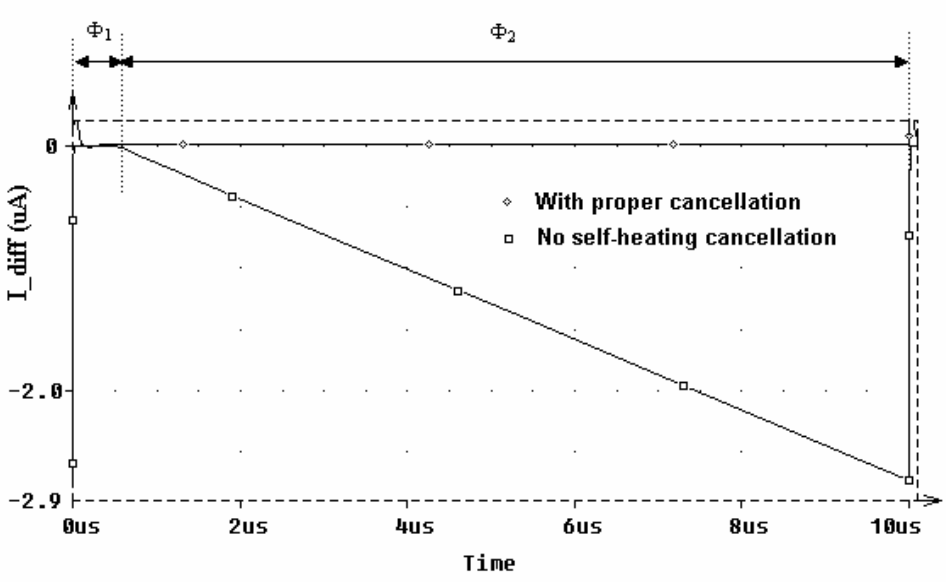


Fig. 5.3. Simulation results for current-mode self-heating cancellation.

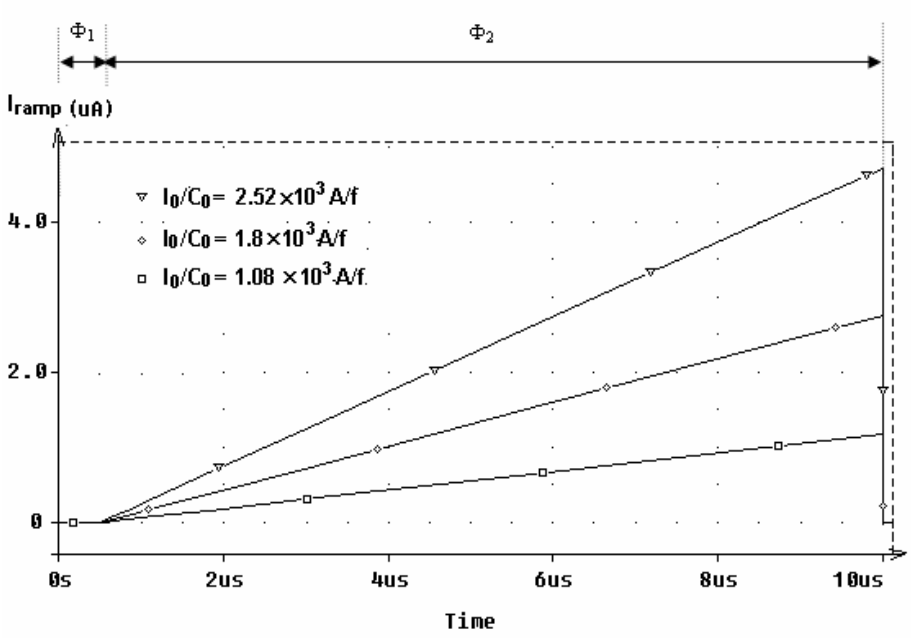


Fig. 5.4. Tuneable feature of the ramp current generator.

5.2. Current-mode ROIC with self-heating cancellation

The readout circuit with the proposed current-mode self-heating cancellation has a simpler structure than the one in voltage-mode when employed in an IR FPA. In current-mode, each pixel contains a microbolometer and a MOS transistor as the *ROW* selective switch. Thus, only three connections (*Row*, V_{bias} and I_{pout}) are needed, compared with that in the voltage-mode where there are four global connections (*Row*, *Vdd, GND* and V_{pout}). This is shown in Fig. 5.5.

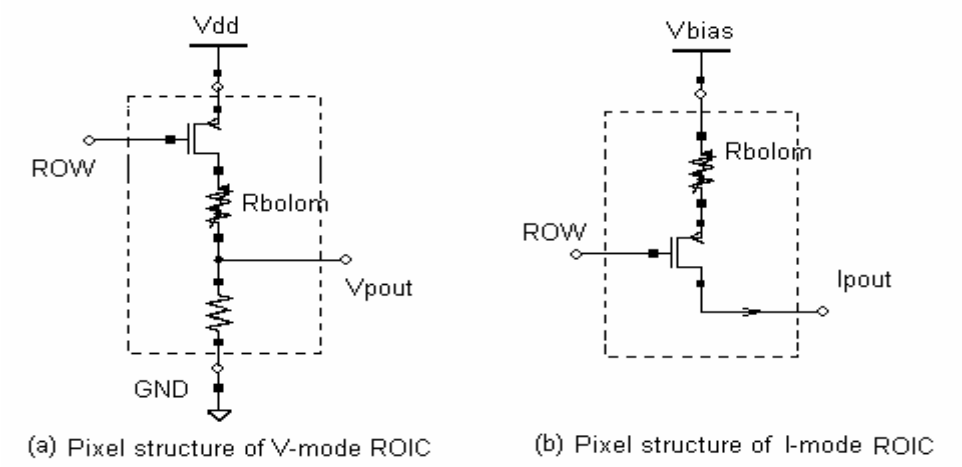


Fig. 5.5. Pixel structure of the voltage-mode(a) and current-mode(b) readout circuit

A current-mode readout circuits for the M × N pixels FPA is shown in Fig. 5.6. The digital circuitry is similar to that in the voltage-mode readout systems. The X-shifter generates the scan control signals for N column-switches, while Y-shifter generates the control signals for M row-switches. These switches are all implemented by the NMOS transistors. Since it is a column-major scanning system, frequency of the clock for Y-shifter should be M times higher than that of the clock for X-shifter. The current output from each pixel is then multiplexed and sent to the current-readout and self-heating cancellation circuits (circuits enclosed by the dash-line in the Fig. 5.1). After the current-subtraction circuits, the output current I_{diff} is integrated and

converted to a voltage signal, which is then, digitized by the on-chip voltage A/D converter and saved in an off-chip memory. The *Calib/Image* switches the ROIC between calibration and imaging mode. When in the calibration mode, the FPA should be shielded from IR radiation. Assuming a perfect self-heating cancellation, the saved digital output, should contain only the fixed pattern noise of the FPA. In the imaging mode, this digitized FPN is converted back in the analog domain, fed to input of the integrator and cancels the FPN. Thus, the final output should only contain the IR signal and small residual FPN.

In addition to the clocks needed by two digital shifters, the on-chip clock generator also provides ϕ_1 and ϕ_2 for readout and self-heating cancellation circuit and all other control signals required by the integrator and A/D converter. Partial parallel readout structure can also be adopted for the current-mode readout scheme in Fig. 5.6 if the microbolometer FPA is a large array, so that the signal integration period longer than 5 μs for each pixel can be guaranteed.

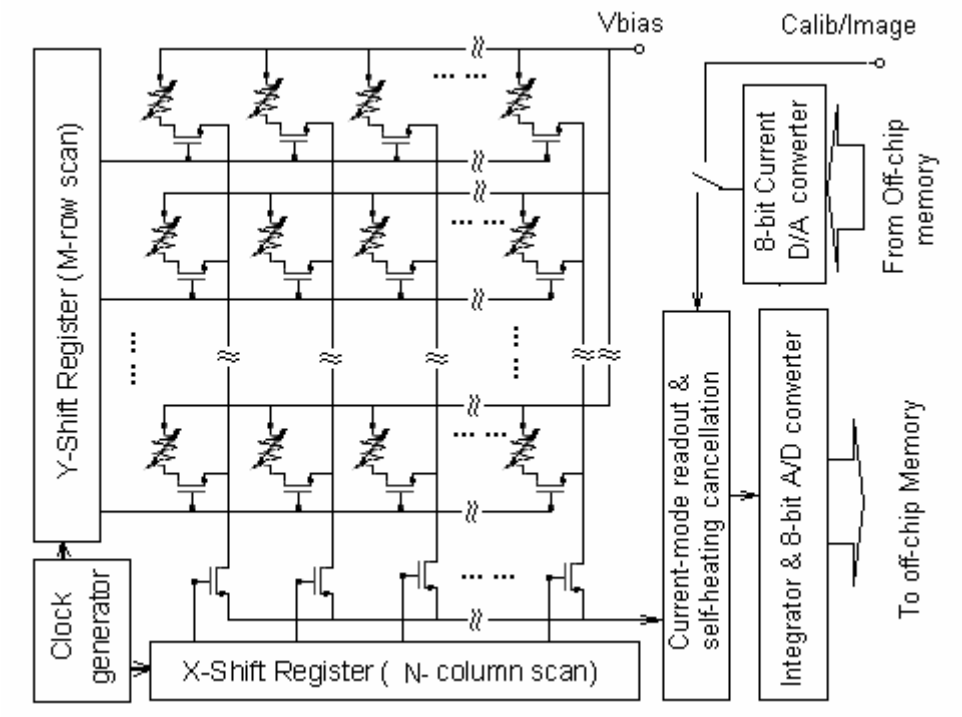


Fig. 5.6. Readout circuit architecture of the current-mode ROIC for an M×N FPA.

5.2.1. Digital circuitry of the current-mode ROIC

The digital blocks are similar to those in the voltage-mode ROIC, which are described in the Chapter 4. The *main_clk* is the pixel clock used as the basic clock to generate the X-Y scanning pulses. The *int_ctrl* signal is the pulse to control the current integrator. When the *int_ctrl* is high, the integrator output is reset to the reference voltage (2.5 V in the designed circuits) and the capacitor is quickly discharged. When *int_ctrl* is low, the current I_{diff} charges the capacitor and generates the voltage signal. The clock generator makes the low period of the *int_crtl* shorter than the bias period of the microbolometer detector by one *clk* cycle so that the transient noise of the ϕ_1, ϕ_2 can be avoided. The X-Y address clock generation circuit is given in Fig. 5.7 where Y-shifter has M bits and X-shifter N bits. The frame signal is the synchronization signal for A/D clock generator and off-chip circuitry, whose falling edge indicates the start of the readout period for the first pixel.

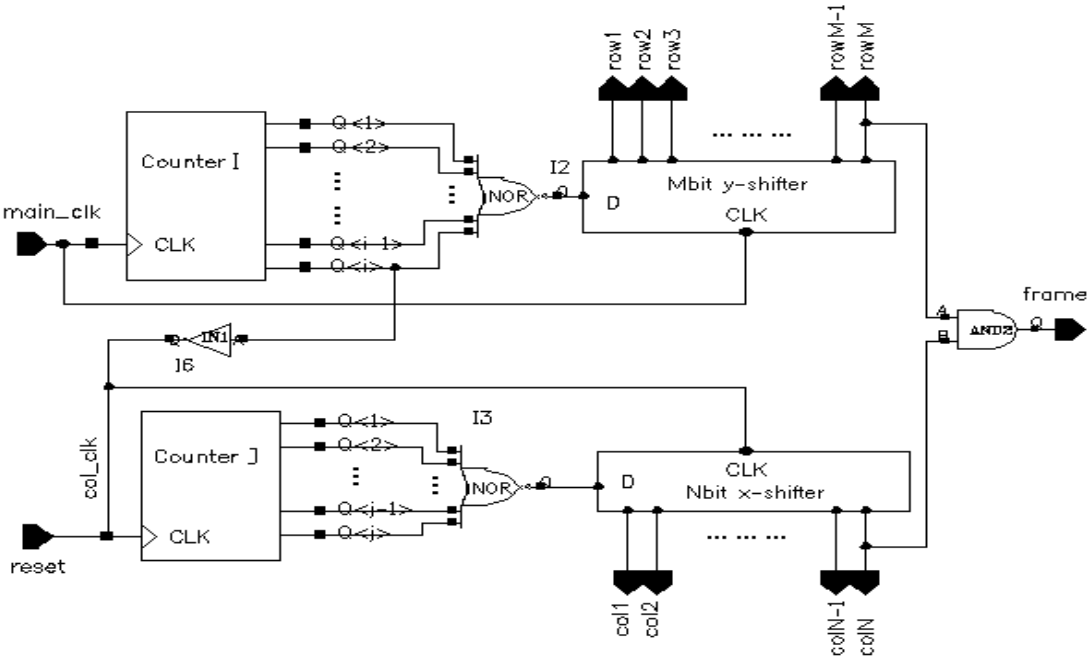


Fig.5.7. X-Y address clock generator for M × N FPA.

5.2.2. Current subtraction circuit

The current subtraction circuit formed by three current mirrors is the most critical part in the current-mode ROIC. In order to reduce the effect of channel length modulation, cascade structure mirror, as shown in Fig. 5.8, is used in current subtraction circuit. To further reduce the error resulting from variation of V_{DS}, the DC operation voltage at the output of the current subtraction circuit is set to be 2.5 V. This is achieved by adjusting the transistors' aspect ratios of each current mirror to make the DC operating points of all mirrors to 2.5 V. Furthermore, the non-inverting input of integrator is tied to 2.5 V to force the circuit operation condition. Although the mismatch or other process variations may cause the drift of the DC operation voltage of the current mirrors and therefore the non-zero of I_{diff}, the drift is much smaller than the fixed pattern noise of the microbolometer array. It would be corrected with the on-chip FPN correcting circuit.

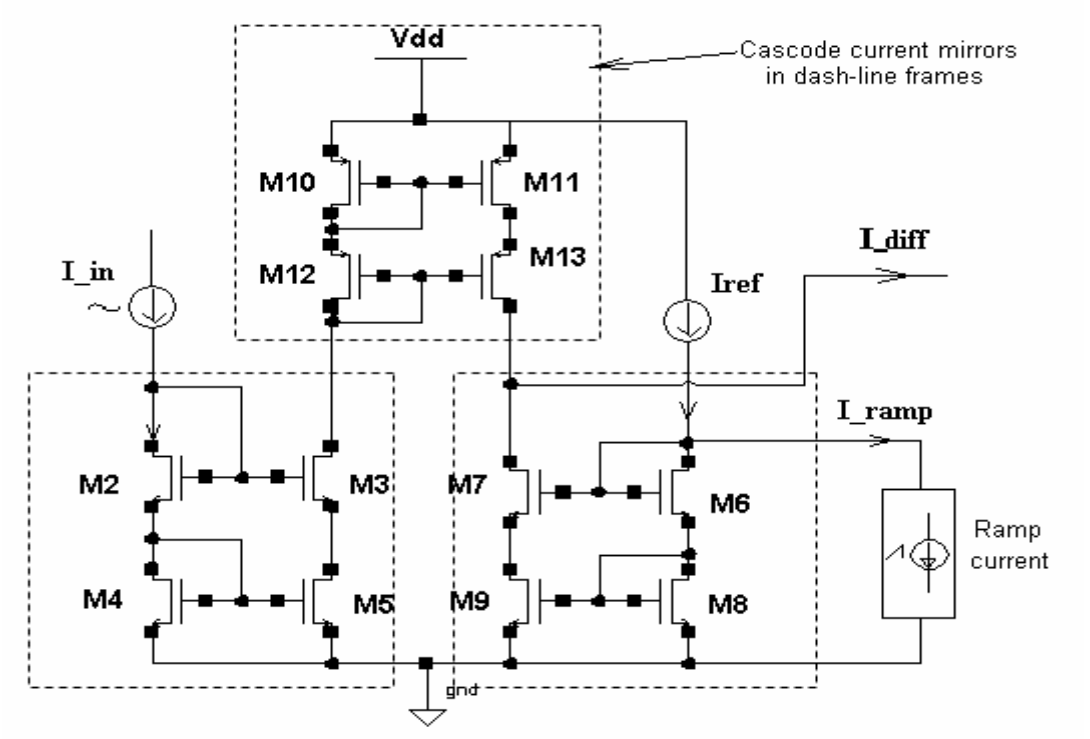


Fig. 5.8. Current subtraction circuit.

Figure 5.9 shows the AC (window 1) and DC sweep (window 2) simulation results of the current subtraction circuit in Fig. 5.8, where the x axis in DC sweep curve is the output voltage swept from 2.25 V to 2.75 V. In the simulation, the ramp current generator is disabled to evaluate the current subtraction circuit independently. The input is an AC current source plus a DC current offset, which equals to I_{ref}. It is observed that the DC offset of I_{diff} is 0.2 nA. The 3 dB bandwidth of the circuit obtained from the AC sweep analysis of the current subtraction circuit is 3 MHz.

In our design, the voltage variation at the output of the drain (or gate) of M6, which is mainly caused by the ramp current generator, is generally smaller than 5 mV. Hence, its effect to the I_{diff} can be ignored. The current-mode readout circuit is designed to handle the large offset current of more than ± 35 μA. Thus, the small offset of 0.2 nA will not affect the dynamic range of circuit and is handled as the noise of FPN. For a 128 × 128 microbolometer FPA, to keep the frame rate higher than 30 frames/sec, the circuit bandwidth of 500 kHz is required for serial readout. For partial parallel readout, the requirement should be even lower. The bandwidth of the current subtraction circuit is enough for the application of the current-mode readout circuits of microbolometer arrays.

Figure. 5.10 shows the noise analysis results of the current subtraction circuit. The equivalent input current noise of the circuit is less than $1.8\,nA/\sqrt{Hz}$, and the referred input noise current integrated from 1 Hz to 1 MHz can be calculated as

$$I_{n\_in} = \frac{\left(\int_{f=1\sim 1M} {I_{n\_out}}^2 df \right)^{\frac{1}{2}}}{Gain} = \frac{\sqrt{230.561\times 10^{-18}}}{1} \approx 15.184nA$$

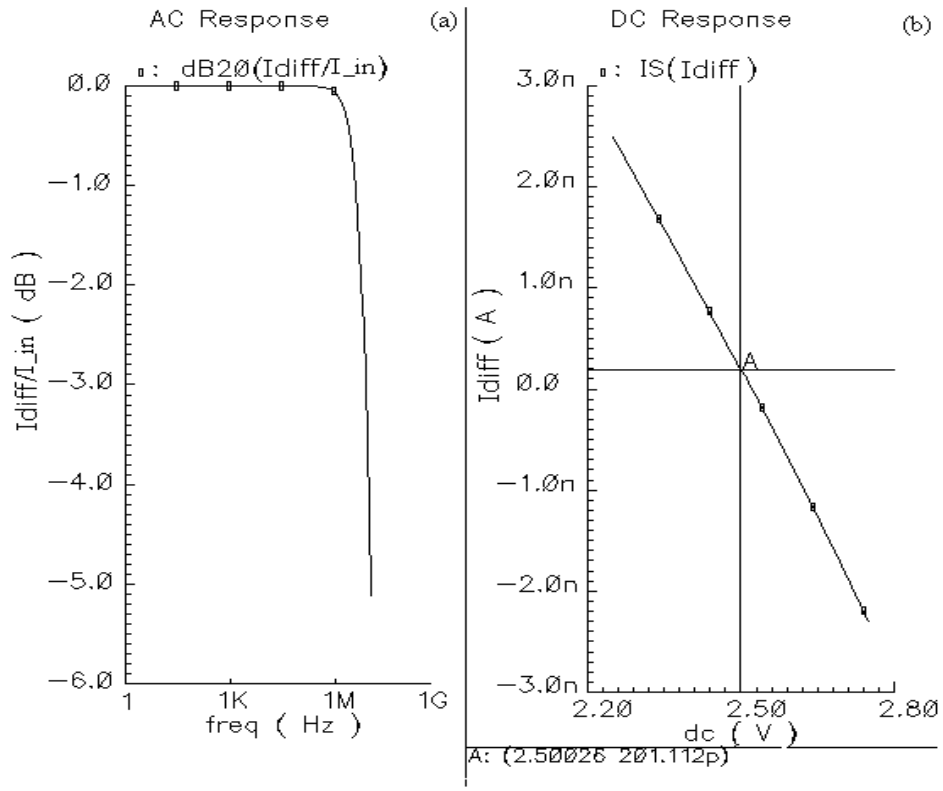


Fig.5.9. (a) AC sweep response and (b) DC sweep of the current subtraction circuit.

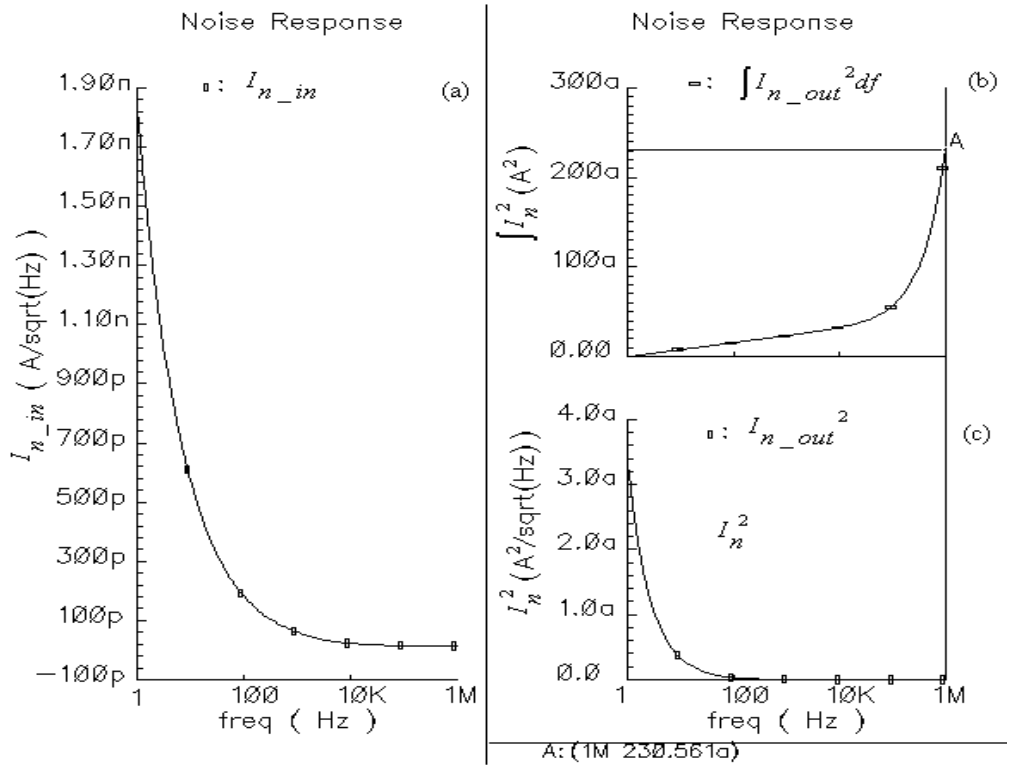


Fig.5.10. Noise analysis of the current subtraction circuit:
(a) Equivalent input current noise density, (b) output noise power density and (c) total noise power in the bandwidth from 1Hz to 1MHz

The input current due to the weak infrared signal normally is around 10 nA. Therefore, the noise of the current-mode readout circuit should be further reduced. By introducing a current gain in the current mirror (M2 ~ M5) and (M6 ~ M9), the noise caused by transistors (M10 ~ M13) can be reduced by a factor of the current gain. Fig. 5.11 shows the noise simulation results of the current subtraction circuit with a gain factor of 4. The equivalent input current noise now is reduced to less than $0.56 nA/\sqrt{Hz}$. The input referred current noise integrated from 1 Hz to 1 MHz is also reduced to

$$I_{n\_in} = \frac{\sqrt{370.036 \times 10^{-18}}}{4} \approx 4.81 nA$$

However, the noise reduction is obtained at the cost of the larger chip area consumed by M3, M5, M7 and M9, whose sizes are 4 times larger than their values in the unit gain current mirrors. The aspect ratios of other transistors may need to be adjusted to maintain the desired DC operation condition.

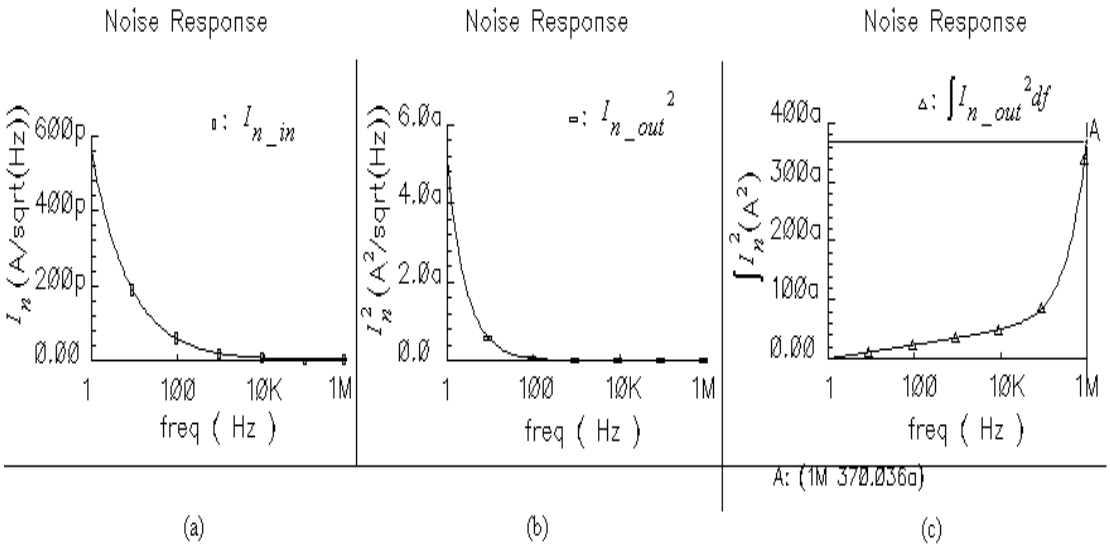


Fig.5.11. (a) Equivalent input current noise density; (b) output current noise power density and (c) total output noise power in the bandwidth from 1 Hz to 1 MHz.

5.2.3. Current steering DAC design

There are three structures which can be employed for current-steering digital-to-analog converters (DAC), namely, binary-weighted, thermometer-coded and segment architecture. For single-ended current output D/A converter, the output current can be described as

$$I_{out} = (b_0 2^0 + b_1 2^1 + \cdots \cdots + b_{n-1} 2^{n-1}) \cdot I_{LSB} \quad (5\text{-}7)$$

Where $b_{0\sim n-1}$ are the n-bit input data, I_{LSB} is the current corresponding to the least significant bit. The output current range is therefore from 0 to $(2^0 + 2^1 + \cdots + 2^{n-1}) \cdot I_{LSB}$. The design of the DAC will be described in the following sub-sections.

5.2.3.1. Selection of the current-steering DAC structure

The simplest current-steering DAC structure is the binary-weighted architecture, which is shown in Fig. 5.12. The input data bits directly control the current mirrors, which are binary-weighted to their corresponding data bits, through the switching latch. In this structure, there is no need for the decoder and the number of the latch and current mirror units are minimized. Thus, the silicon area would be highly reduced. However, the difference in the size of the current mirror makes the mismatching a big problem, especially with the increasing of input data bits. That will cause large INL (Integral Nonlinearity) and DNL (Differential Nonlinearity) errors. Moreover, severe glitches will arise at the code transitions.

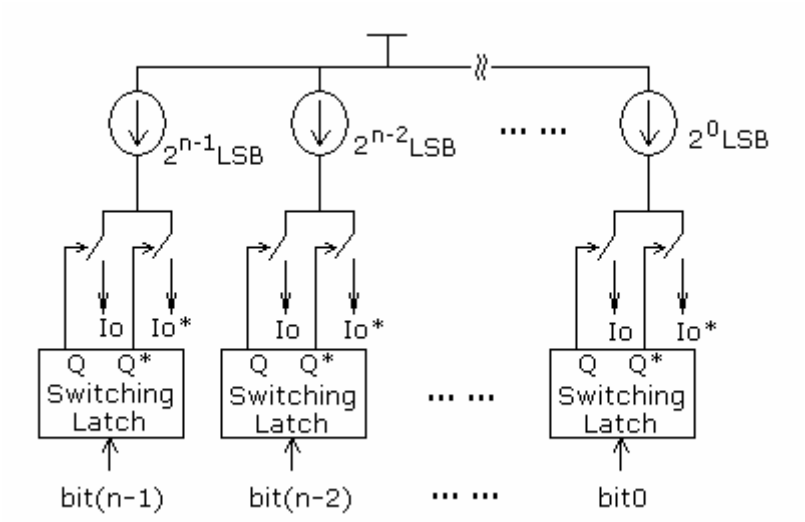


Fig. 5.12. Binary weighted architecture of the current-steering DAC.

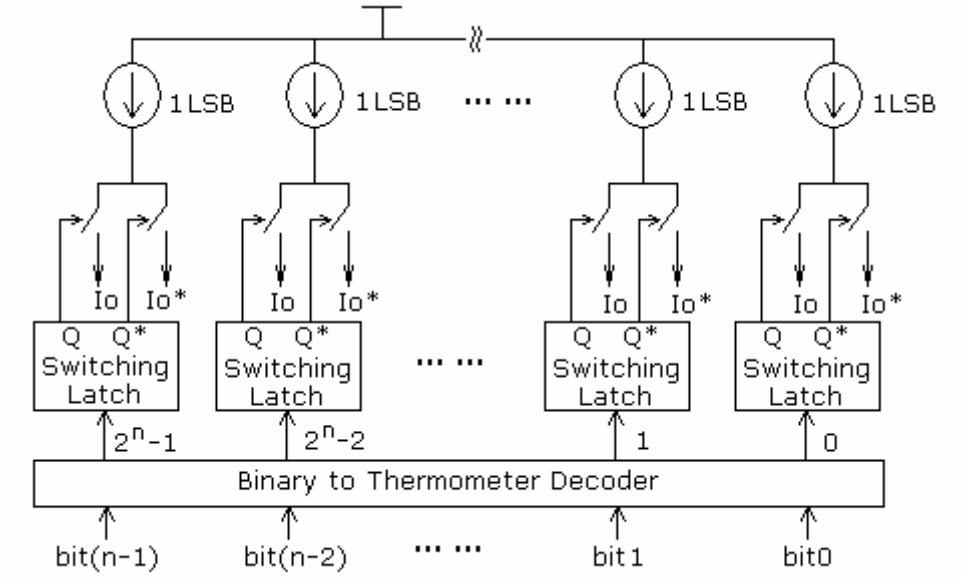


Fig. 5.13. Thermometer coded architecture of the current-steering DAC.

In thermometer-coded architecture, only current sources with the size of one LSB are used so that the requirement on mismatching can be greatly relaxed and glitches at the code transitions are minimized. A binary to thermometer decoder is needed to convert the binary input to 2^n-1 control bits. Moreover, the number of the current sources and latches is increased to 2^n-1 for one n-bit D/A converter. Thus, the complexity of the circuit is increased.

The trade-off between circuit complexity and mismatching results in the segmented DAC architecture, where binary-weighted and thermometer coded structures are combined to obtain an enhanced overall performance. An 8-bit segmented current-steering DAC is shown in Fig. 5.14. In this example, an 8-bit input is partitioned into four segments. Every two input bits are converted to three control bits with a simple binary to thermometer decoder. Four different current sources, representing 1 LSB, 4 LSB, 16 LSB and 64 LSB, respectively, are used. *Bit0* and *bit1* control three current sources with the size of 1 LSB; *Bit 2* and *bit3* control the current sources with size of 4 LSB; and so on. Although thermometer-coded segments are adopted to reduce the number of current sources having different sizes, the segmented structure still maintains the advantages of relatively small size and simple circuit structure. Thus the segmented current steering DAC is chosen for the current-mode readout circuit.

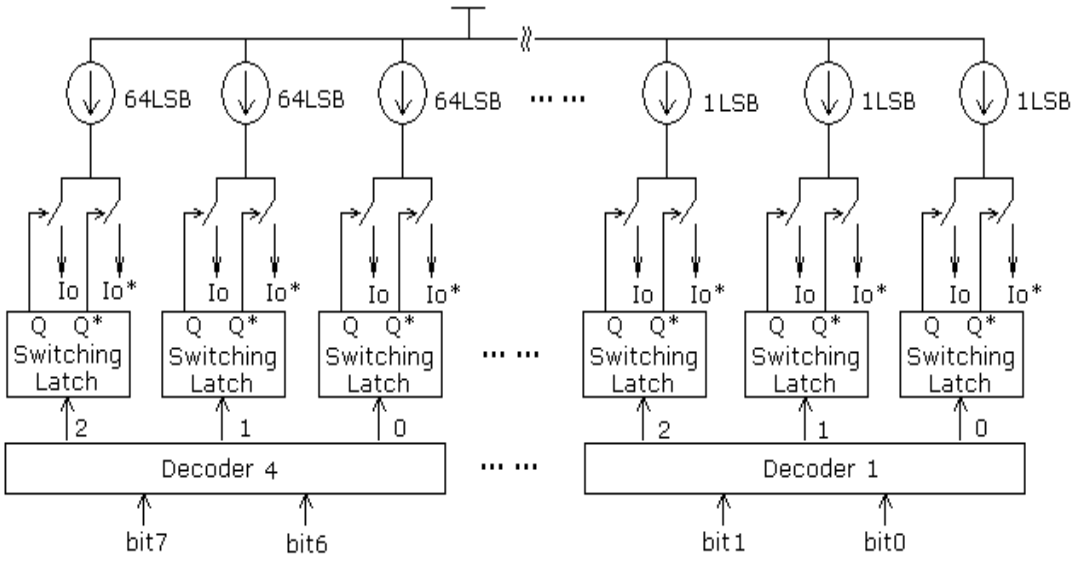


Fig. 5.14. Segmented architecture of the 8-bit current-steering DAC.

5.2.3.2. Current sources and mirrors

In current-steering DAC, a high-precision current reference independent of the CMOS process and temperature variation is required. In this design, a bandgap voltage reference is used to generate the reference current. The schematic of the bandgap reference circuit is shown in Fig. 5.15[139]. The dimensions of the PMOS transistor M0, M1 and M2 are same and their gates are connected to a common node. The operational amplifier is a two-stage amplifier with the PMOS input transistor pair and Miler compensation. The input current of the opamp can be ignored because of the zero gate current of the MOS input stage. Thus, current *I0*, *I1* and *I2* have the same value. The operational amplifier forces the voltage V_A to be equal to the voltage V_B. PNP transistors T0, T1 and T2 are connected as diodes. T0 and T2 have the same base-emitter junction size, while the size of T1 is 8 times larger than T0 or T2.

From Fig. 5.15,

$$V_A = V_{EB0} = V_T \ln\left(\frac{I_0}{I_S}\right) \tag{5-8}$$

$$V_B = V_{EB1} + I_1 R_0 = V_T \ln\left(\frac{I_1}{8 \times I_S}\right) + I_1 R_0 \tag{5-9}$$

where V_T is the thermal voltage and I_S is the saturation current of the bipolar device.

Since $V_A = V_B$ and $I_0 = I_1 = I_2$, then

$$I_1 = \frac{1}{R_0} V_T \ln 8 \tag{5-10}$$

The output bandgap reference voltage can be written as

$$\begin{aligned} V_{bg} &= V_{EB2} + I_2 R_1 \\ &= V_T \ln\left(\frac{I_2}{I_S}\right) + I_2 R_1 \\ &= V_{G0} + V_T\left(\ln(I_2 C) - \gamma \ln T\right) + I_2 R_1 \end{aligned} \tag{5-11}$$

where γ and C are constants.

In order to obtain the zero temperature coefficient of the voltage V_{bg}, the circuit parameters should be selected so that the derivative of V_{bg} with respect to T is held zero at the circuit operation temperature. Since the collector current of T2 in this circuit is a PTAT (Proportional To Absolute Temperature) current, the derivative of V_{bg} will include $\partial I_C / \partial T$. Thus,

$$\begin{aligned}\frac{\partial V_{bg}}{\partial T} &= \frac{\partial V_T}{\partial T}\ln\left((I_C C)-\gamma \ln T\right)+V_T\left(\frac{1}{I_2}\frac{\partial I_2}{\partial T}+\frac{\partial\left(-\gamma \ln T\right)}{\partial T}\right)+R_1\frac{\partial I_2}{\partial T}\\ &= \frac{V_{EB2}-V_{G0}}{T}+V_T\left(\frac{\ln 8}{I_2 R_0}\frac{\partial V_T}{\partial T}-\frac{\gamma}{T}\right)+\frac{R_1 \ln 8}{R_0}\frac{\partial V_T}{T} \qquad (5\text{-}12)\\ &= \frac{V_{EB2}-V_{G0}-\gamma\cdot V_T}{T}+\frac{k}{q}+\frac{R_1 \ln 8}{R_0}\frac{k}{q}\end{aligned}$$

Setting the Eq. (5-12) to zero, the following equation can be obtained.

$$\frac{k}{q}\left(1+\frac{R_1 \ln 8}{R_0}\right)\approx -1.8\times 10^{-3} \qquad (5\text{-}13)$$

where k is Boltzmann's constant (1.38×10^{-23} J/K); q is electron charge.

The ratio R1/R0 is calculated to be

$$\frac{R_1}{R_0}\approx 9.545$$

This ratio has been slightly adjusted, according to the simulation results, to make the temperature coefficient of the output V_{bg} to be zero at 27 ºC. After adjustment, the R1 and R0 are chosen to be 5000 Ω and 550 Ω.

The simulation result of the output bandgap voltage, swept from -40 ºC to 100 ºC, is shown in the Fig. 5.16. The bandgap reference output at 27 ºC is 1.232 V and its temperature coefficient at room temperature is 0. The maximum variation ΔV_{bg} from -40 ºC to 100 ºC is less than 3 mV.

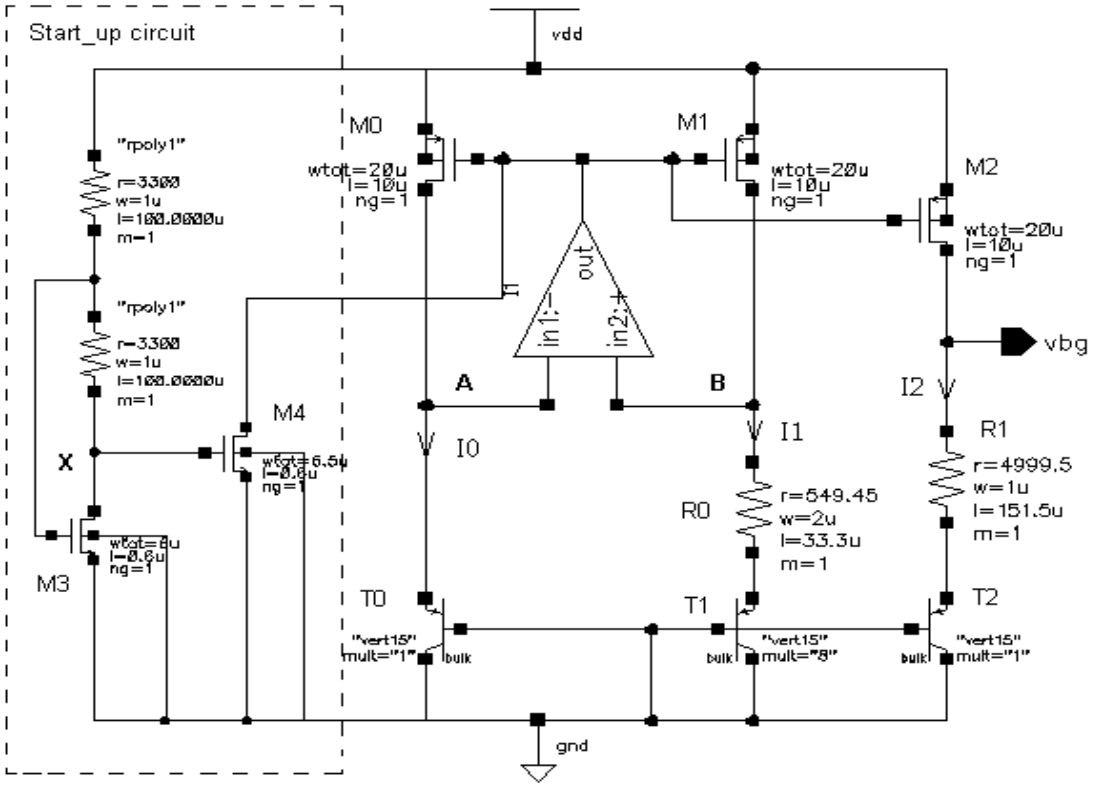


Fig. 5.15. Schematic of the bandgap voltage reference circuit.

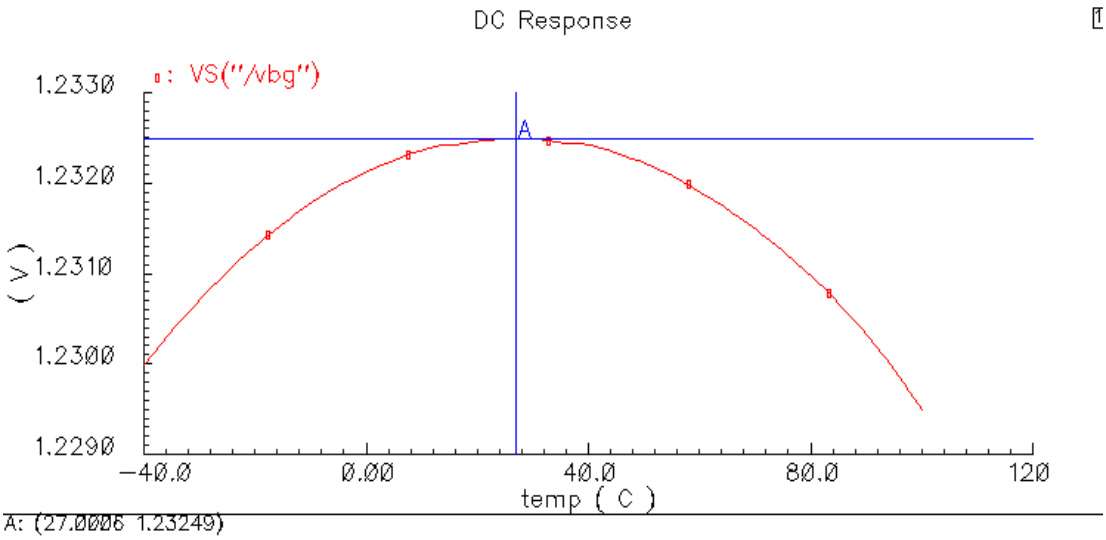


Fig. 5.16. Temperature dependence of the bandgap reference voltage output.

The start-up circuit, which is enclosed in the dash line in the Fig. 5.15, is used to initialize the circuit when the power is switched on. After the power turned on, the

voltage V_X will become smaller than the threshold voltage of the NMOS transistor and then the M4 will be kept off. Thus, the start-up circuit will not affect the normal operation of the bandgap circuit.

The basic current cells of current steering DAC are generated using the above described bandgap voltage as the reference. The voltage-to-current converter circuit is shown in the Fig. 5.17. The bandgap voltage is impressed on a resistor and a NMOS transistor, which is serially connected with the resistor, through an operational amplifier. M5 and M6 are identical and are working in the saturation region. Since the bandgap voltage is determined by the silicon bandgap energy, the generation of the low 1 LSB current will require a very large R_0 if M6 is not used. The current, *1LSB_ref*, is sensed and mirrored by the cascade current mirror M7 ~ M10. Numbers of 1 LSB basic current outputs can be generated by similar current mirrors. Because the bandgap voltage is temperature-insensitive reference, the temperature coefficient of the 1 LSB output current is also comparatively small. The simulation result of the voltage-to-current converter is shown in the Fig. 5.18. In the temperature range of -40 ºC to 100 ºC, the output current variation is less than 60 nA. Since the 1 LSB current is designed to 281.4 nA, the variation is smaller than 21 % of 1 LSB within the operation temperature range, which is acceptable.

The current sources of 4 LSB, 16 LSB and 64 LSB are obtained in a similar way. A DC offset current source of -127.5 LSB is also generated and added to output current. A bipolar current DAC output is therefore obtained.

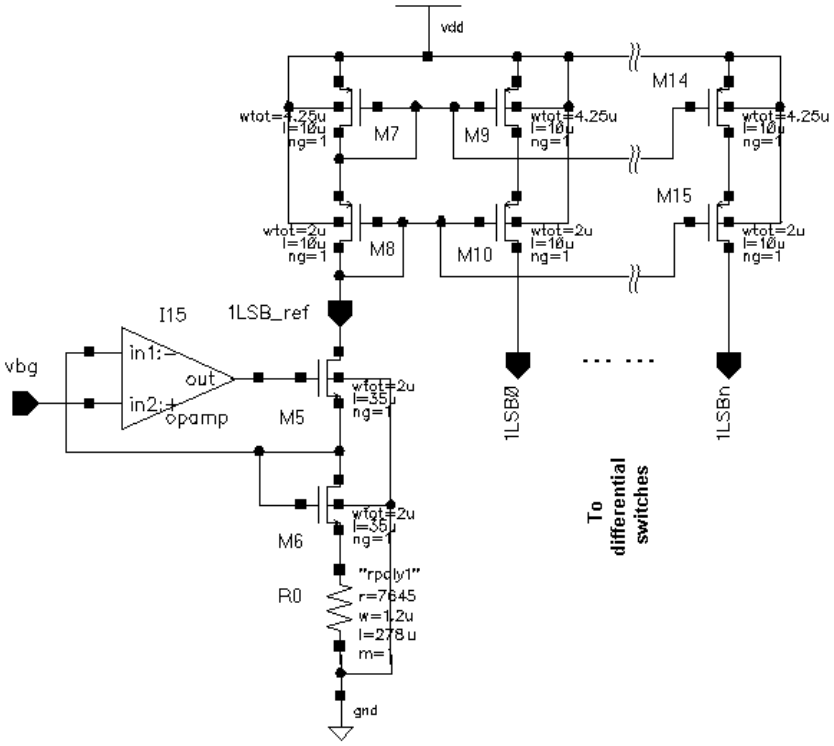


Fig. 5.17. Schematic of the voltage-to-current converter.

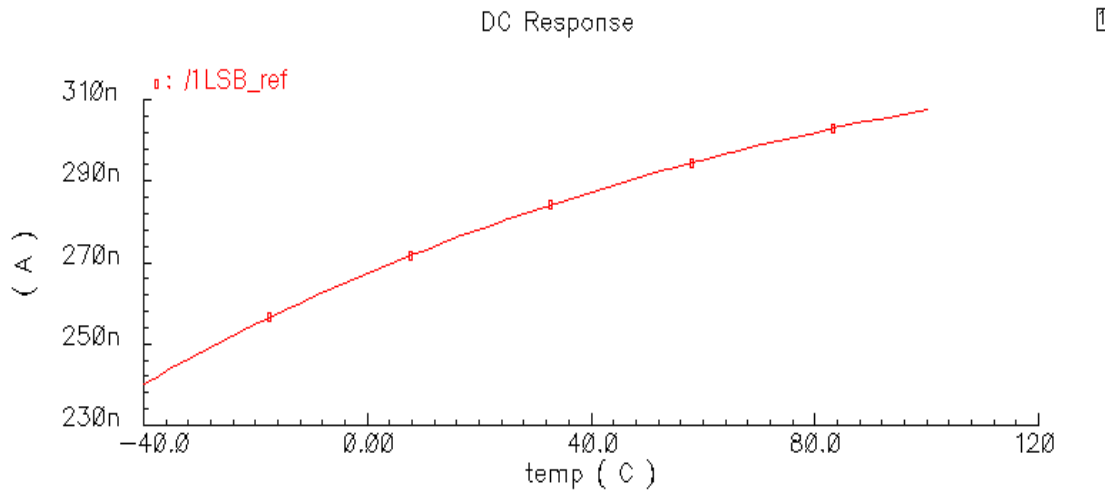


Fig. 5.18. Simulation result of the 1 LSB basic current generator.

5.2.3.3. Decoder logic

The 2-to-3 lines binary to thermometer decoder can be easily realized by simple combinational logic circuits. The truth table of the combinational logic is shown in

Table 5.2. The switches that control the current sources are implemented by using PMOS transistors. The control signal is active low.

Table 5.2. Truth table of the 2-bit binary-to-thermometer decoder.

Inputs		Outputs		
Bit 1(s1)	Bit 0(s0)	Line2	Line1	Line0
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Derived from the truth table, the combinational logic of the decoder can be obtained.

$$\begin{aligned} Line0 &= \overline{(s0 + s1)} \\ Line1 &= \overline{s1} \\ Line2 &= \overline{s0 \bullet s1} \end{aligned} \tag{5-14}$$

The schematic of the decoder with latches is shown in Fig. 5.19 and the waveforms of the decoder outputs are shown in the Fig. 5.20. The maximum propagation delay from input to *Line(i)* control signals is less than 0.7 ns. The outputs of the latch, *Q* and *Qn*, control the differential switches for the current sources.

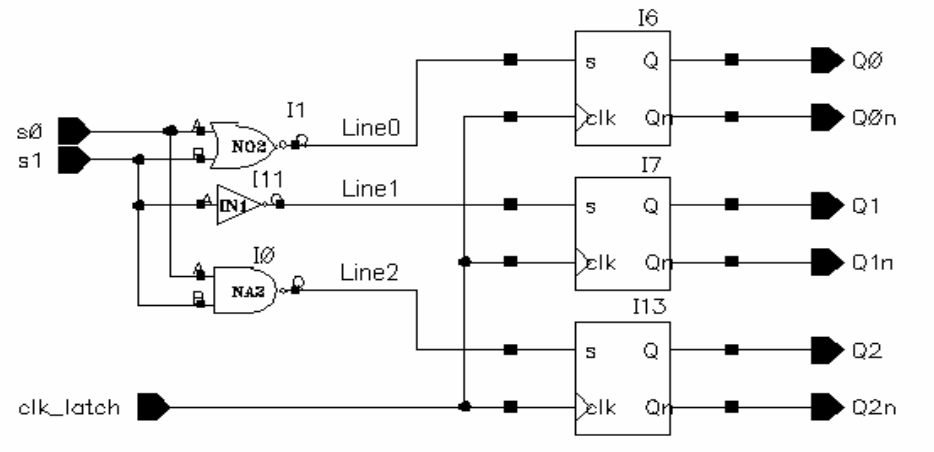


Fig. 5.19. 2-bit binary-to-thermometer decoder circuit and latches.

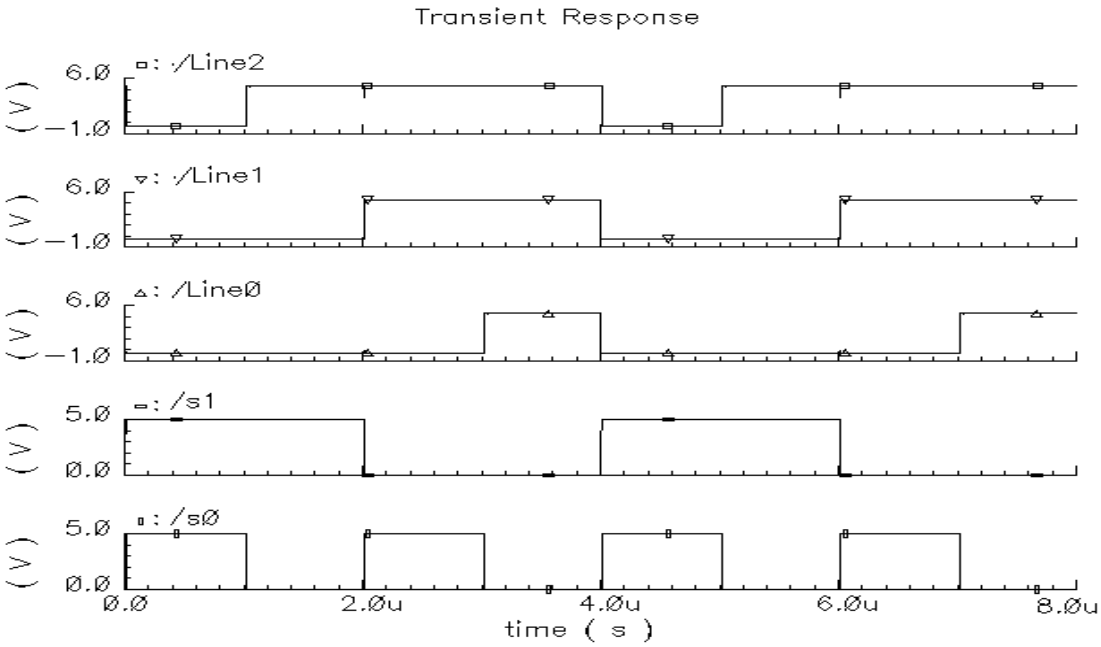


Fig. 5.20. Waveforms of the decoder inputs, *S0*, *S1* and outputs *Line(0-3)*.

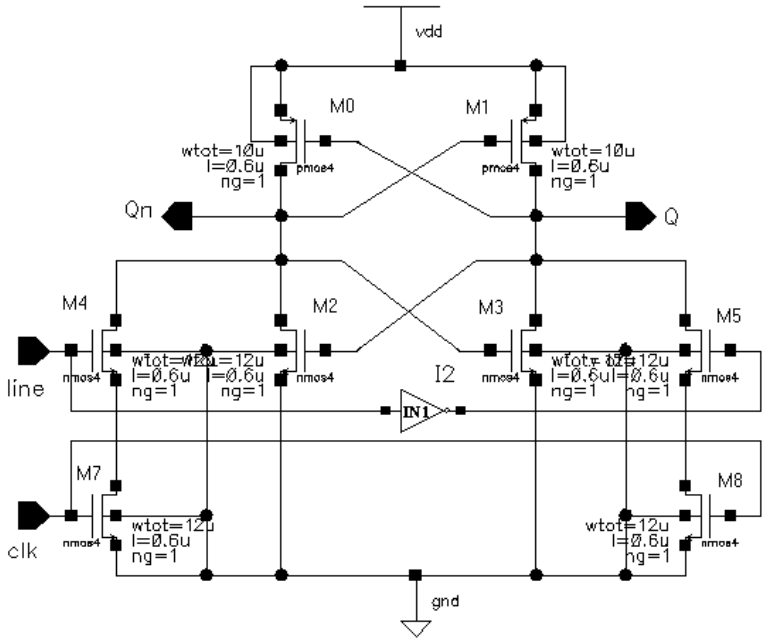


Fig. 5.21. Schematic of the low-crossing latch.

5.2.3.4. Differential switches and low-crossing latch

In order to reduce the glitches in the current output, the differential switches, which are made of PMOS transistors, are used for each current source. The low-crossing latch illustrated in the Fig. 5.21 is employed to generate the control signals for the

differential switches. The crossing point of the two outputs of the latch can be adjusted by the ratio of M0 (M1) to M2 (M4). In this design, the crossing point of the switching signals is set to a value lower than the switching point of the PMOS transistors so that the differential switches will not be turned off simultaneously. Fig. 5.22 shows the transition of the two output of the low-crossing latch. It can be seen that the crossing point of the switching control signals is around 1.4 V.

The clock signal is used to synchronize the timing of switching signals. When the clock signal is low, the outputs are latched, while the clock goes to high, the positive output, *Q*, of the latch follows the input signal and the inverting output is obtained at the negative output. The latch can also operate in the transparent mode, when the clock is set to high, so that the glitches from the clock signal can be avoid.

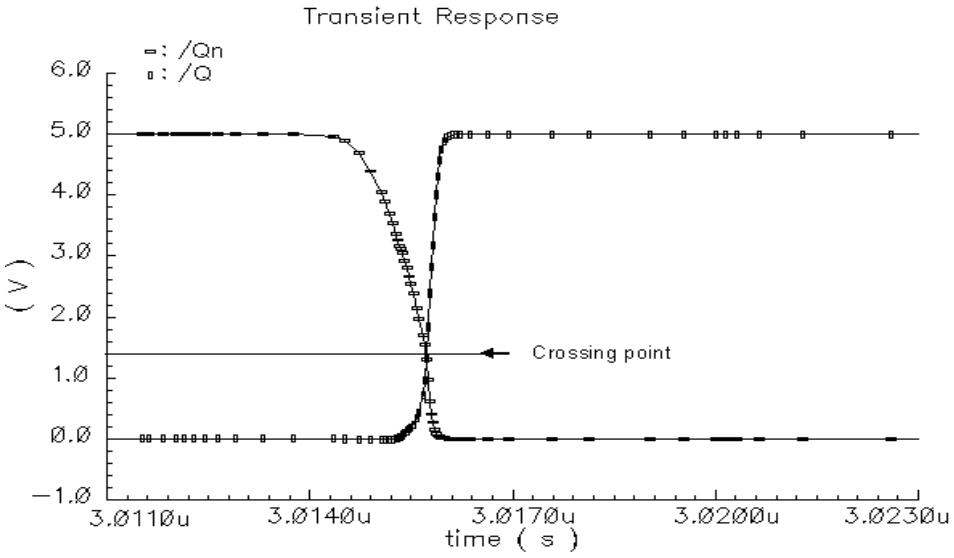


Fig. 5.22. Transient analysis results of the low-crossing latch.

The circuit of differential switches is shown in the Fig. 5.24. PMOS transistor pairs are used. The current is either steered to *i_out* or *i_outn* depending on the output of *Q* or *Qn*. The two extra transistors M3 and M4 are added to isolate the switches from

the output. Therefore, the fluctuations and charge injection due to parasitic capacitance can be reduced and hence the glitches at the output. The low crossing point of 1.4 V avoids both PMOS switches, M1 and M2 in the Fig. 5.23, turning off at the same time.

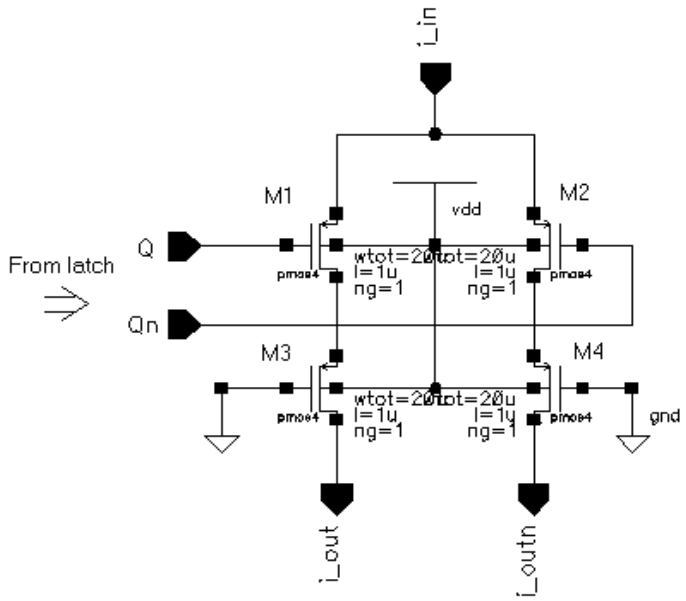


Fig. 5.23. PMOS differential switches of the current outputs.

5.2.3.5. Current-steering DAC circuit and performance

The overall block diagram of the current-steering DAC circuit is shown in Fig.5.24. The bandgap voltage generator and the voltage-to-current converter, Cell **i_ref**, generate the reference currents of 1 LSB, 4 LSB, 16 LSB and 64 LSB, together with the constant current output of 127.5 LSB. Each reference current source is mirrored to three current cells. The digital inputs are first decoded by the 2-3 line binary-to-thermometer decoder then latched to the output control signals *Q(i)* and *Qn(i)*. These signals control the ON or OFF of the differential switches that determine the current output from each current cell flowing to *i_out* or *i_outn*. The output of the DAC can be expressed as

$$I\_out = (D<0>\times 2^0 + D<1>\times 2^1 + \cdots + D<7>\times 2^7)\cdot I_{LSB} - 127.5\times I_{LSB} \quad (5\text{-}15)$$

where I_{LSB} is designed to be 281.4 nA so that the full range of the DAC output current can be utilized to cancel the FPN noise.

Since the output *i_outn* is unused for the microbolometer current-mode readout circuit, it is connected to a 5 kΩ on-chip resistor to ground to ensure the continuous current flow during the operation.

The layout of the DAC is plotted in the Fig. 5.26. The power supplies for digital circuit and the analog circuit are separated in the layout to reduce the crosstalk between the digital and the analog circuits.

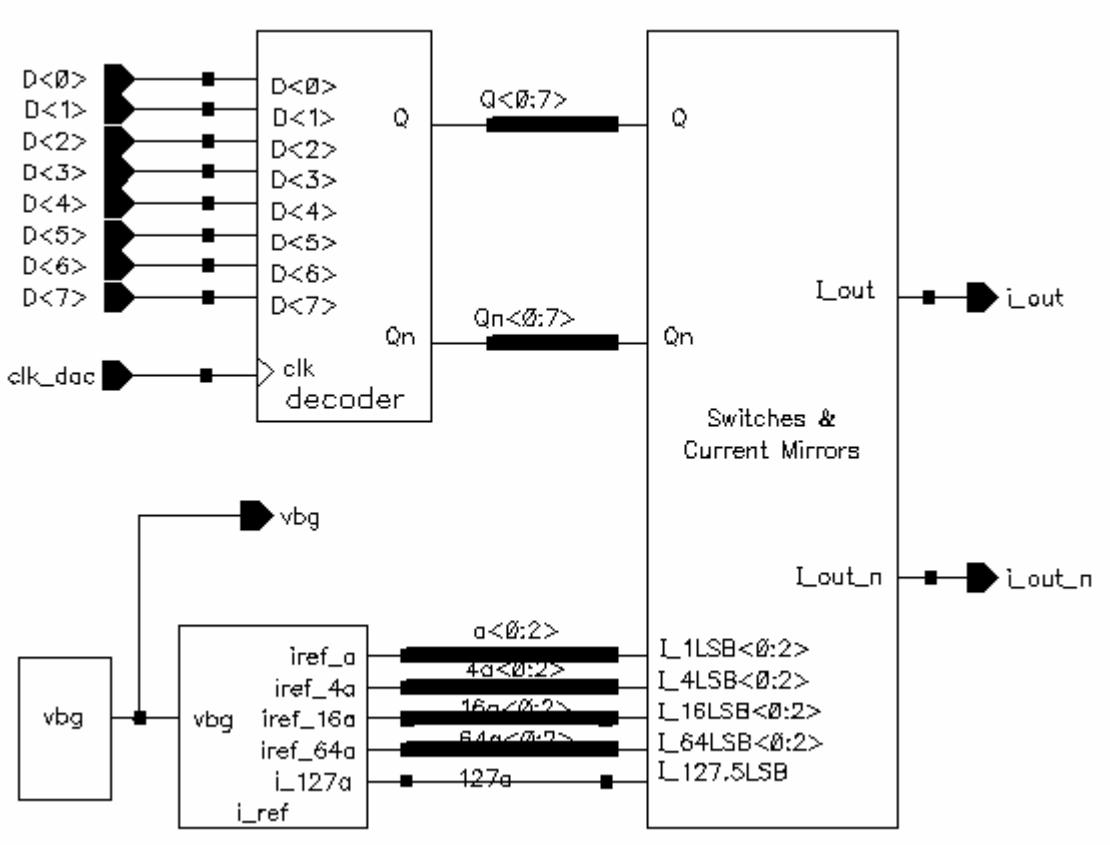


Fig. 5.24. Block diagram of the current-steering DAC.

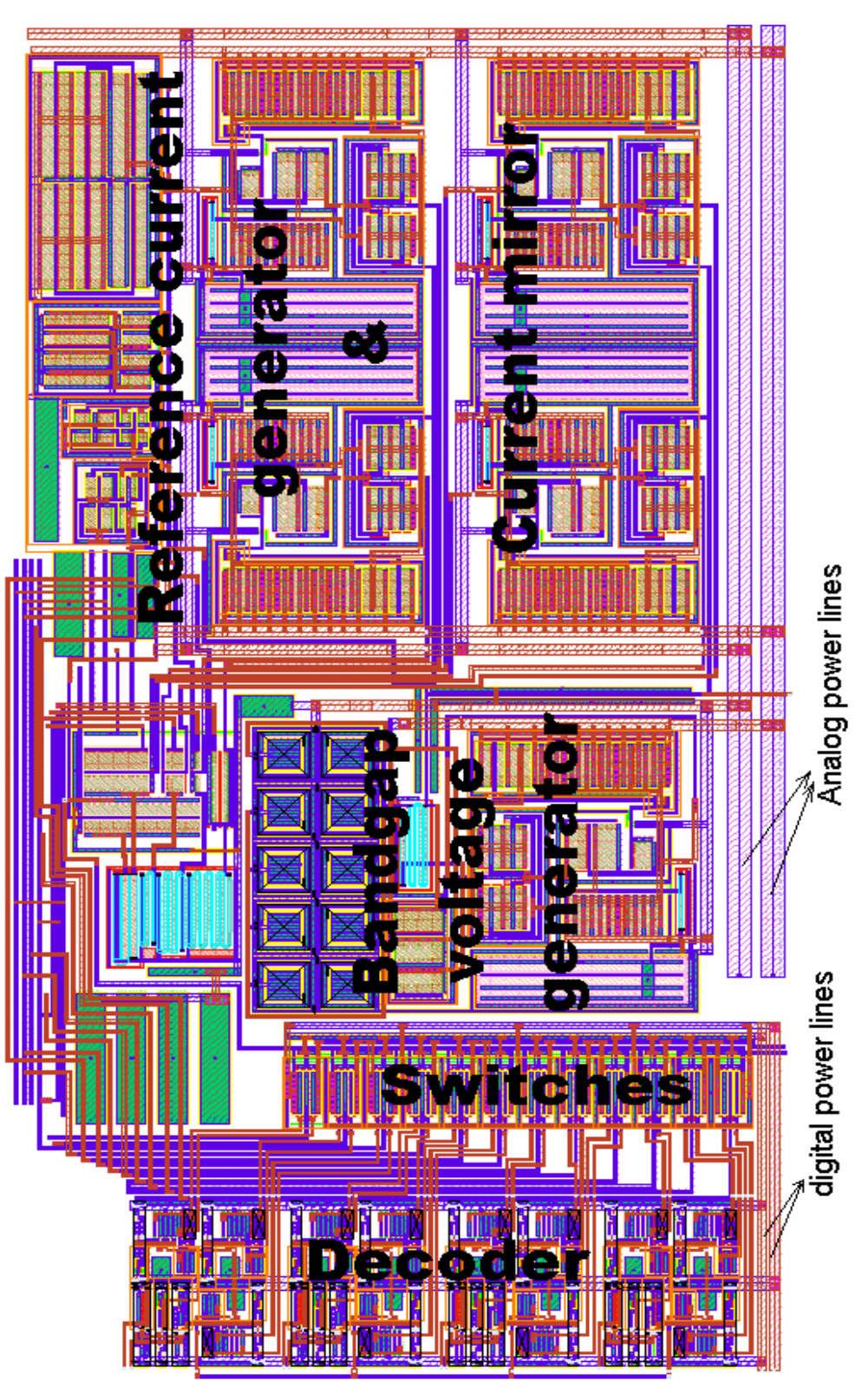


Fig. 5.25. Layout of the current-steering DAC.

The post-layout simulation results of the current-steering DAC, obtained by simulating the netlist extracted with "all cap" option, are shown in the Fig. 5.26. It shows the transient analysis results of the current output, *i_out*, at input digital codes from 0 to 255. The update frequency of the input code is set to 500 kHz, which is applicable for the 128 × 128 microbolometer array operating in 30 Hz frame rate.

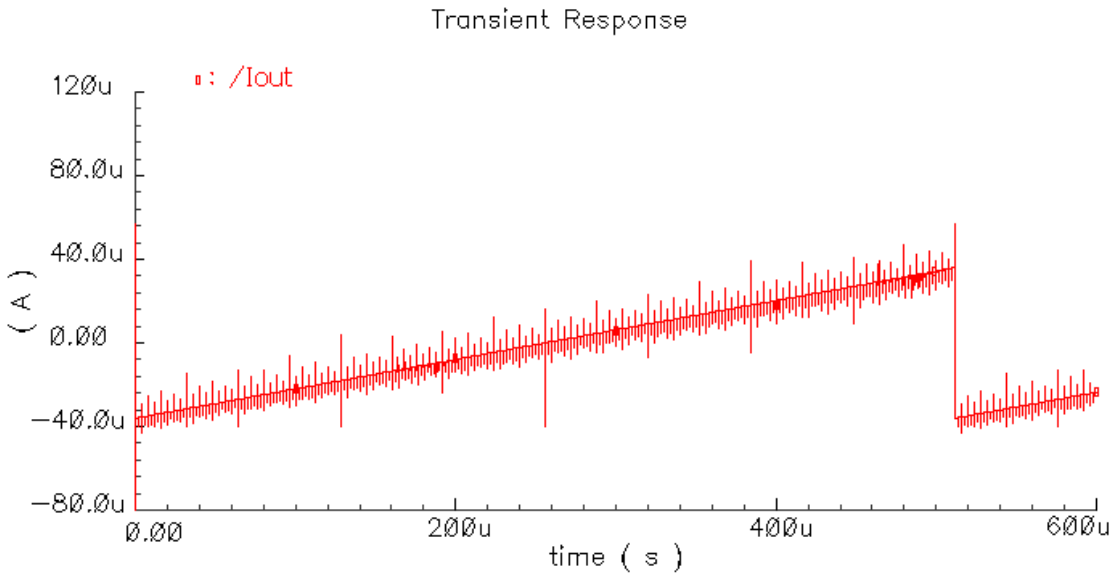


Fig. 5.26. Transient analysis of the current-steering DAC.

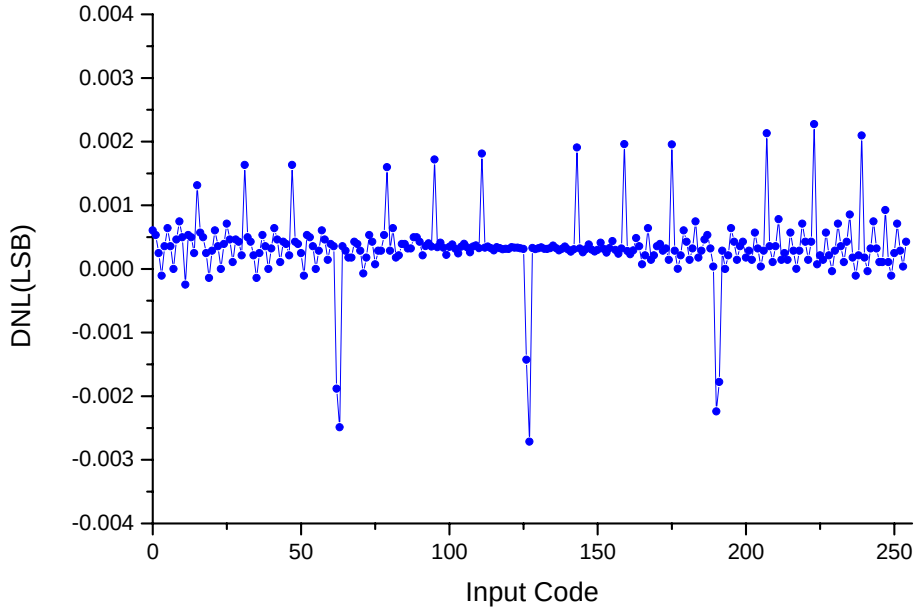


Fig. 5.27. Simulated DNL of the current-steering DAC.

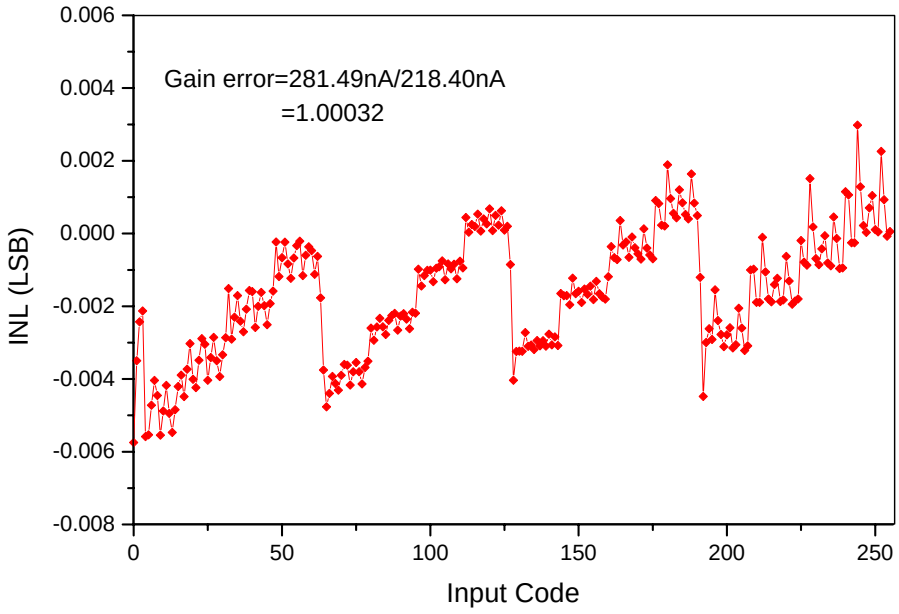


Fig. 5.28. Simulated INL of the current-steering DAC.

The differential non-linearity and integrated non-linearity of the output current are calculated and plotted in the Fig. 5.27 and Fig. 5.28, respectively. It can be seen that the DNL of the designed DAC is less than ± 0.003 LSB. The INL is less than ±0.006 LSB, where the INL is calculated after the gain error correction of the factor of 1.00032.

5.2.4. Current-mode fixed pattern noise cancellation circuit

The schematic of the current-mode FPN correction circuit is shown in Fig. 5.29. Its operation is similar with that in the voltage-mode circuits described in chapter 4. In calibration mode, the DAC output, *i_out*, is disconnected from the input of the integrator by the control signal, *Calib/Imaging*. The input of the integrator, I_{diff}, comes from the current subtraction circuit illustrated in Fig. 5.1. The R_{bolom} in this

circuit represents the selected microbolometer element in the FPA, where the pixel-addressing circuit is not shown in the figure. R_{dummy} is the dummy resistor which has the same resistance as the room temperature resistance of the microbolometer. Since the microbolometer array is shielded from the IR incident, and the self-heating noise is cancelled by the generated ramp current, the integrator integrates the large FPN of the array. The resulting FPN output is digitized and stored in the off-chip memory. When in imaging mode, the microbolometer array is sensing the IR signal and the self-heating cancellation circuit is still activated. The 8-bit FPN data are read back from the off-chip memory and converted to the bipolar current, I_{FPN}, which is fed to the input of the integrator, together with I_{diff}. Thus if the circuit is designed such that the I_{diff} of the pixel (x,y) is equal to I_{FPN} of the pixel (x,y), but in the opposite direction, the fixed pattern noise will be cancelled.

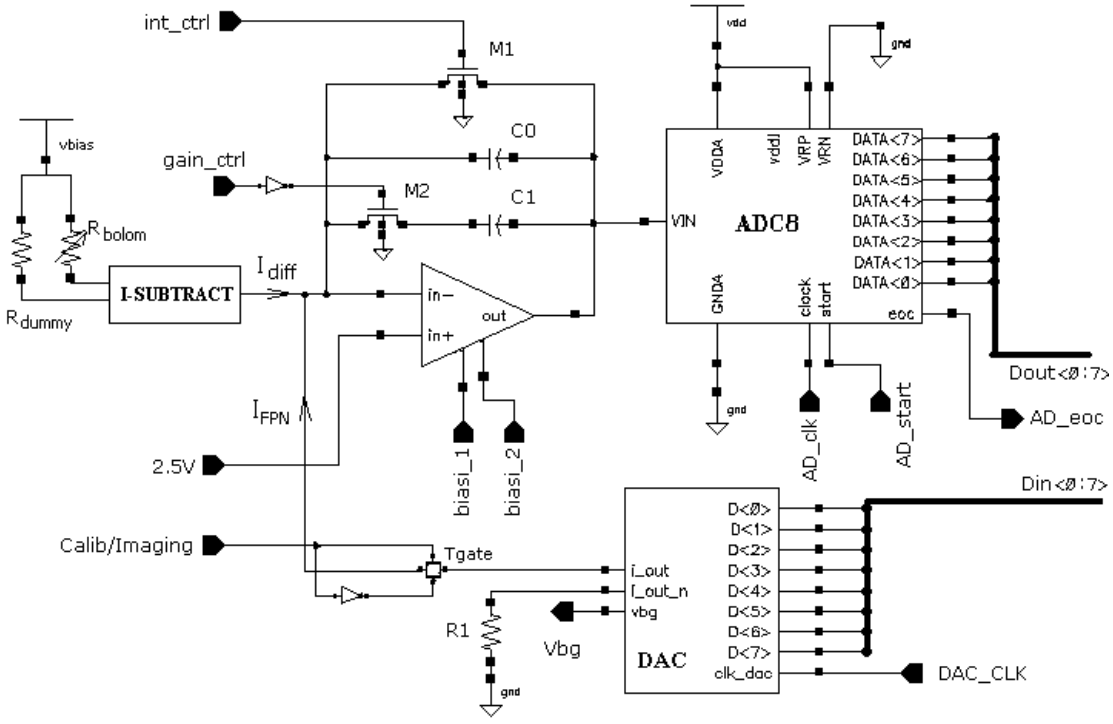


Fig. 5.29 Schematic of the current-mode FPN correction circuit

The *int_ctrl* signal, as described in section 4.3.1.1, makes the integration time shorter than the pixel readout period so that the transient noise from the pixel addressing and the glitches from the current-steering DAC can be avoided. The *gain_ctrl* signal sets the gain of the integrator. In the calibration mode, the *gain_ctrl* signal should be low so the large FPN signal is integrated with the gain of $\frac{I_{diff}}{C_0 + C_1} t_{\text{int}}$, where t_{int} is the integration time, and will not saturate the integrator. While in imaging mode, high integrator gain can be used since the integrated current only contains the IR signal and the small residual fixed pattern noise. The gain of the integrator can be set to a high value by turning off M2. The circuit is Fig. 5.29 can only provide a coarse cancellation (8-bits) of the FPN. The fine cancellation (12-bits) is preformed off-chip.

For evaluation of the fixed pattern circuit, a resistor array of 8 × 8 elements with the resistance values varying within ± 15% of the nominal value, 5000 Ω, is used to simulate the fixed pattern noise in the microbolometer FPA. The R_{dummy} is set to 5000 Ω. The ramp current generator in the current subtraction circuit block is disabled in order to evaluate the FPN correction only. Post-layout simulation results including effects caused by parasitic capacitors are listed in the Table 5.3, where ΔR is the resistance difference between the resistors in the array to simulate the microbolometer and dummy resistor. It is observed from the Table 5.3 that there is a small offset existing in the readout circuit. It may be caused by the mismatch of the current mirrors in the current subtraction circuit. It does not affect the 8-bit current-mode fixed pattern noise correction since the offset is smaller than the 1/3 LSB of the DAC. The residual FPN noise after correction is shown in the Fig. 5.30. It can be seen that the I_{diff} of ±35.9 μA, which is equivalent to the ± 15.3% resistance non-uniformity in the FPA, can be reduced to less than ± 140 nA, which is smaller than ± 0.5 LSB.

Table 5.3. Simulation results of the on-chip current-mode FPN correction circuit

ΔR (Ω)	I_{diff} (μA)	A/D output	I_{diff} (nA) (After correction)	A/D output (After correction)
765	-35.916	11111111	-25.40	10000000
750	-35.263	11111101	64.45	01111111
650	-30.965	11101110	-46.07	10000000
550	-26.434	11011101	-115.38	10000000
450	-21.871	11001101	-56.89	10000000
350	-17.138	10111100	-107.76	10000000
250	-12.381	10101011	-132.01	10000000
150	-7.519	10011010	-59.54	10000000
50	-2.490	10001000	-98.81	10000000
0	0.970	01111111	-43.40	10000000
-50	2.671	01110110	-3.34	01111111
-150	7.620	01100100	-121.96	10000000
-250	12.511	01010011	-16.61	10000000
-350	17.253	01000010	-60.11	10000000
-450	21.968	00110001	-128.28	10000000
-550	26.516	00100001	-89.57	10000000
-650	31.033	00010001	-72.45	10000000
-750	35.320	00000010	8.68	01111111
-765	35.971	00000000	79.48	01111111

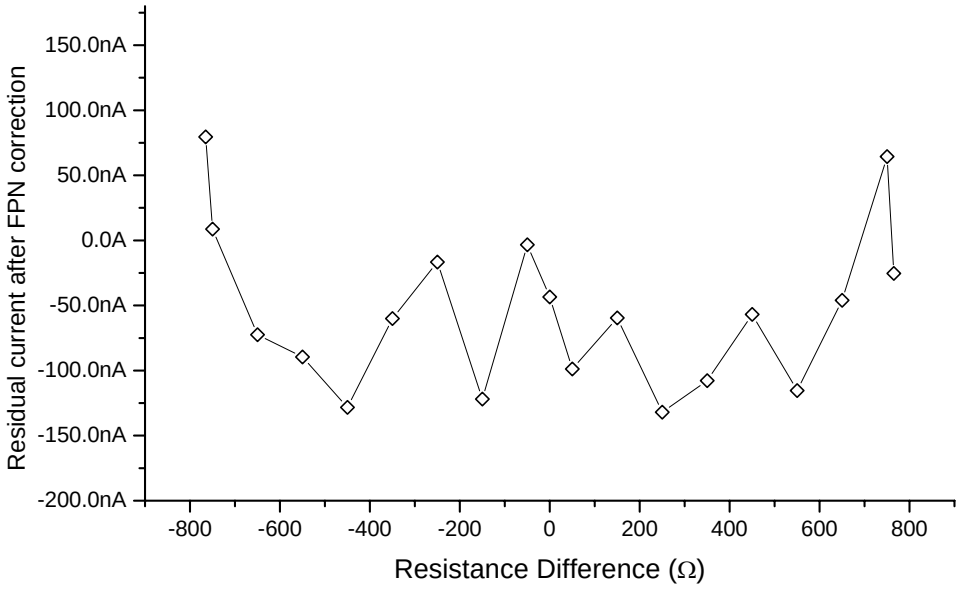


Fig. 5.30. The residual FPN current after current-mode FPN correction

5.3. Summary

A current-mode readout integrated circuit for microbolometer with the self-heating cancellation circuit has been described. The self-heating cancellation is achieved using a ramp current that replicates the self-heating effect. The ramp current is generated with a PMOS transistor operating in the triode region and a capacitor that mimics the thermal capacitance of the microbolometer. Simulation results have shown that with the properly chosen circuit parameters, especially the ratio of I_0/C_0, the self-heating effect can be effectively cancelled. An 8-bit on-chip current-steering DAC is designed for the coarse FPN correction. Post-layout simulation results show that the 8-bit current-mode FPN correction circuit can reduce the FPN current to less than ± 0.5 LSB.

Chapter 6. Experimental Results

The operation of the microbolometer detector is significantly affected by the self-heating effect [132,133,138]. Since the thermal conductance of the microbolometer is necessarily minimized to achieve high sensitivity, the self-heating typically results in a large thermal drift of the detector. Studies in chapter 3 show that the self-heating noise can be much higher than the desired infrared signal. If there is no proper cancellation, a large portion of the dynamic range of the subsequent readout circuits would therefore be sacrificed. Thus, an optimized readout circuit is necessary to remove the noise generated from the self-heating to achieve the high performance.

Based on the proposed self-heating cancellation technique, a prototype ROIC is fabricated in a Double-poly Triple-metal 0.6-μm CMOS process. The chip is packaged in a standard PLCC-84 ceramic package. The microphotograph of the ROIC is illustrated in the Fig. 6.1. Both voltage- and current-mode readout circuits are integrated onto the same chip. In order to evaluate the readout circuit with either the microbolometer FPA or a single microbolometer, the simplified voltage- and current-mode readout circuits, which include the self-heating cancellation but without the FPN correction, are also designed separately on the chip. The test set-ups for single bolometer and FPA measurements are described in this chapter. National Instrument's PCI-6025E data acquisition card is used for final IR image acquisition. An image acquisition software written in LabVIEW is developed for testing the voltage-mode microbolometer FPA readout circuits.

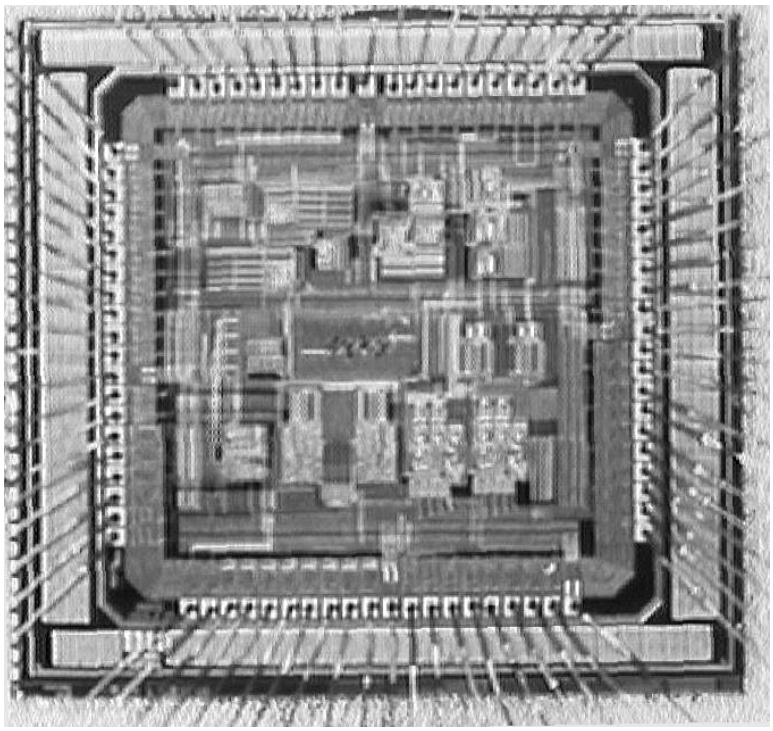


Fig. 6.1. The microphoto of the ROIC.

6.1. Microbolometers used in measurement

The single microbolometer used in the evaluation of self-heating cancellation circuits is a bulk-micromachined titanium bolometer with the diameter of 50 μm × 50 μm. The measured room temperature resistance of the single microbolometer is 2.68 kΩ. Other parameters provided by Institute of Microelectronics, Singapore, are listed in Table 3.3.

The microbolometer FPA used in testing is a 128x128 2-D array, fabricated in a standard CMOS process with the micromachining post-process. Its SEM photo is shown in Fig. 6.2(a). Each microbolometer pixel in the FPA has 50 μm × 50 μm diameter and room temperature resistance of around 5 kΩ. The picture of the FPA mounted inside a 68-pin PLCC socket is shown in Fig 6.2(b). The large grey area in

the centre of this chip is the 128 × 128 microbolometer focal plane array. The FPA consists of Wheatstone bridge readout circuit, pre-amplifier and X-Y scanning multiplexers. The supply voltage for the on-FPA circuit and bias voltage for the bridge are both 5 V. A frame synchronization signal is generated by the on-FPA digital logic circuit. It is a single positive pulse when the last pixel (128, 128) is selected. And the negative edge of the pulse indicates the position of the signal from the first pixel.

However, this only available microbolometer FPA for testing has some drawbacks. The on-chip readout bridge and preamplifier cannot be used for our test because the pre-amplifier is saturated by the large fixed pattern noise of the FPA and offset voltage in the bridge. Thus, the output voltage of the microbolometer was taken from one arm of the bridge and fed to the ROIC, as shown in Fig. 6.2(c). Since the digital ground for multiplexers in FPA chip cannot be separated from the analog ground to the bridge, the output of the FPA could be affected by glitches from the digital circuits in FPA, and consequently reduces the signal-to-noise (S/N) ratio of the readout circuit. On the other hand, the foundry that fabricated Ti microbolometer arrays is no longer available for us and a custom process is beyond the available funding resources. Thus, it is impossible to design and fabricate another FPA. The evaluation of the ROIC is therefore constrained to these pre-fabricated microbolometer arrays that are available at the time of the evaluation.

Both the single bolometer and microbolometer FPA used in measurement were developed by the joint research project [140] and fabricated by Institute of Microelectronics, Singapore.

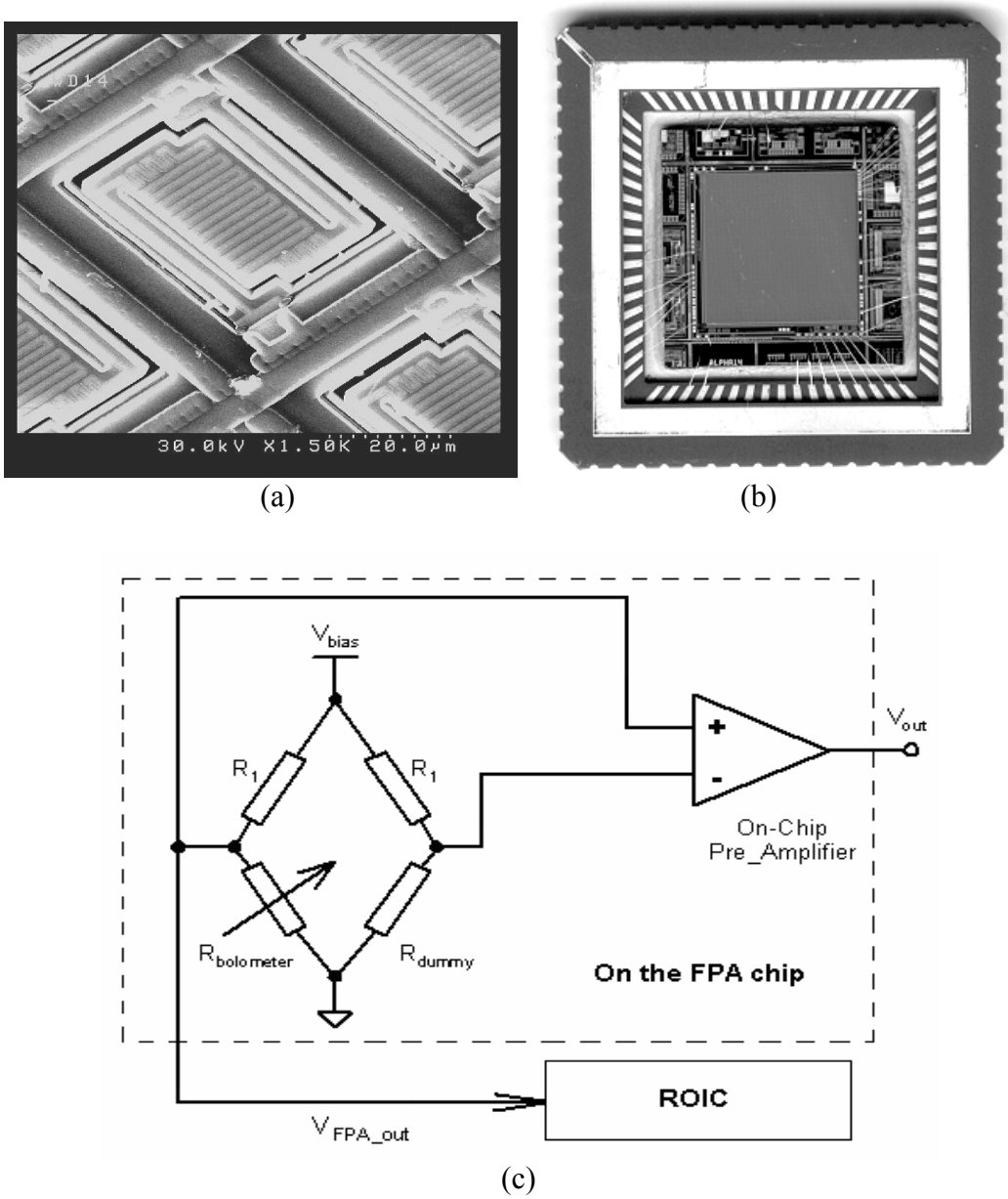


Fig. 6.2. (a) SEM photo of the microbolometer on FPA; (b) The microphotograph of the microbolometer FPA chip; (c) On-FPA readout bridge and the output of FPA to our ROIC.

6.2. Test of the voltage-mode self-heating cancellation circuit with single microbolometer

The single bolometer readout circuit contains only the self-heating cancellation circuit. The test set-up is shown in Fig. 6.3. The microbolometer, R_{bolom}, and the

fixed-value resistor, R_1, are placed in a vacuum chamber to reduce the bolometer's heat dissipation through the air. The air pressure inside the vacuum chamber is kept at less than 10^{-4} Torr. A voltage pulse is generated by a HP Function/Arbitrary Waveform Generator is supplied to the single bolometer and R_1 as the electrical bias. The amplitude of the pulse is 5 Volts high and the duration is 10 μs. However, its read period is set to 30 ms so that the microbolometer has enough time to cool down before the next test cycle. The self-heating cancellation circuit is operated under a 5 V power supply. The gain of the preamplifier is approximately unity. The room temperature resistance of the microbolometer used in testing is 2.68 kΩ.

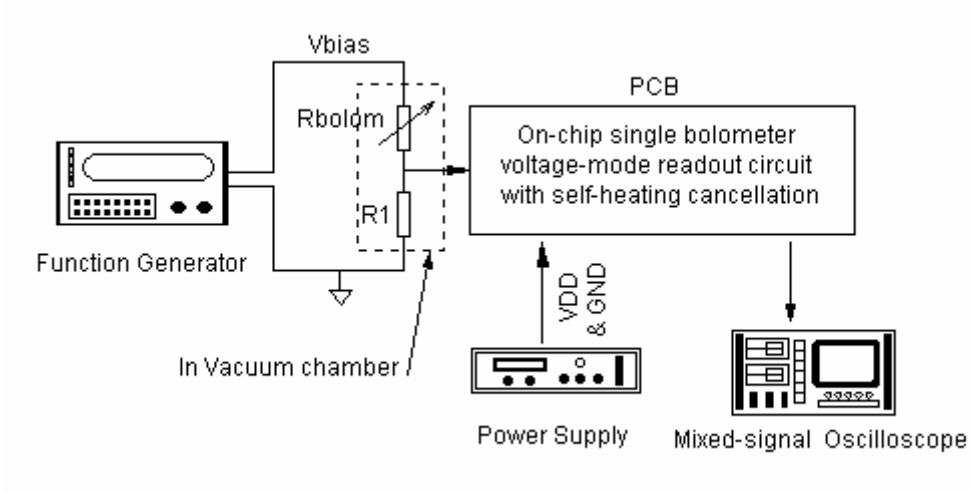


Fig. 6.3. The test set-up of voltage-mode self-heating cancellation circuit for single bolometer.

The output, V_{out}, from the preamplifier with different I_0/C_0 ratios is plotted in Fig. 6.4. The tuneable feature of the self-heating cancellation circuit can be clearly observed. Since the current I_0 can be tuned off-chip, a good self-heating cancellation can be achieved. The large spikes, appearing at the beginning and the end of the bias period, result from the transitions of ϕ_1 and ϕ_2, which does not affect the performance of the readout circuit if the integration time of the sequential integrator is shorter than the

bias period of 10 μs (9 μs in the testing) and is set in such a way that the spikes could be avoided. The outputs of the integrator with and without self-heating cancellation are plotted in the Fig. 6.5. It can be seen that the output would be saturated if no self-heating cancellation is employed. If the time constant of the integrator is increased to avoid saturation, the dynamic range of the circuit would be highly degraded.

To further evaluate the effectiveness of the cancellation, the residue error after the self-heating cancellation is observed, which is shown in Fig. 6.6. The random measurement noise is due to the use of off-chip bolometer in the measurement and can be reduced if the bolometer is integrated with the self-heating cancellation circuit. In most practical readout circuit, an integrator is added after the preamplifier to improve the signal-to-noise ratio. With such an arrangement, the random noise can be further reduced. Thus, in the evaluation of the self-heating cancellation, and the random noise is ignored and a linear fit of the measured data is used. The linear fit analysis shows that the slope of V_{out} after self-heating cancellation is about 14 V/s, which translates to an output voltage drift of 0.126 mV at the end of 9 μs reading period. This compares to a 12.3 mV drift (based on a slope of about 1367 V/s as shown in Fig. 6.4) when no self-heating cancellation is applied. Thus, the self-heating effect is reduced by at least two orders of magnitude with the proposed voltage-mode self-heating cancellation circuit. The small DC offset of the V_{out} results from a slightly unbalance of the bridge readout circuit.

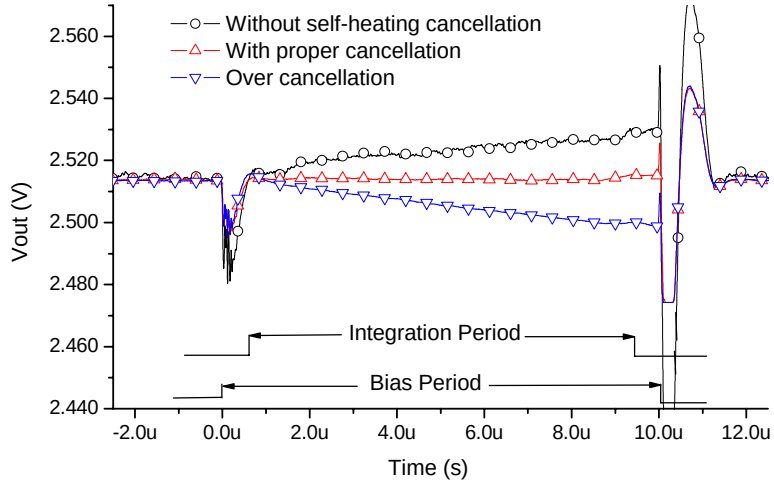


Fig.6.4. Measured output from preamplifier with different I_0/C_0 ratios.

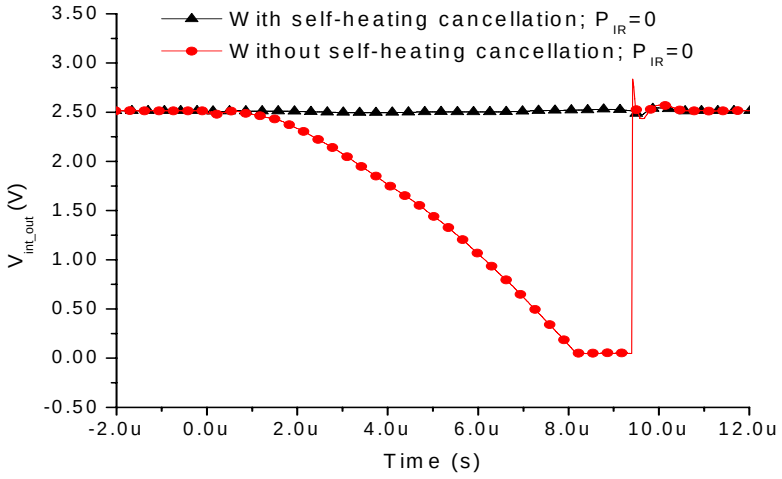


Fig. 6.5. Measured output from integrator with and without self-heating cancellation.

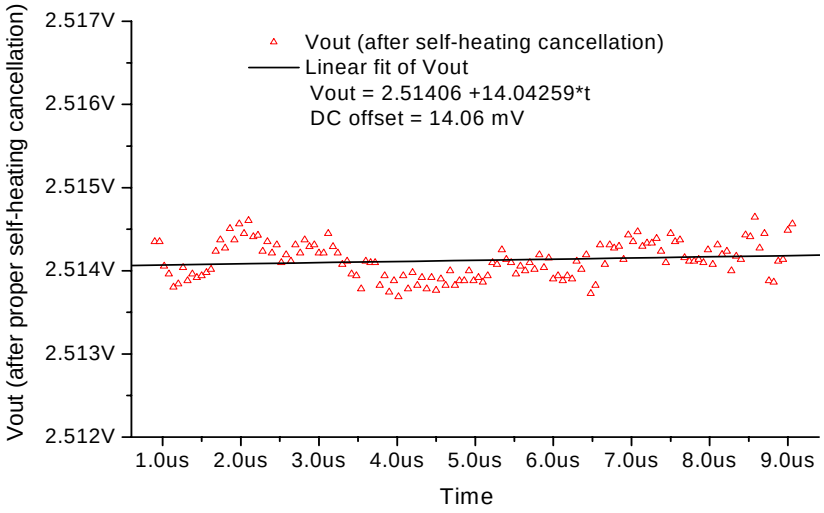


Fig. 6.6. Measured residue error after self-heating cancellation.

6.3. Test of the current-mode self-heating cancellation circuit with single microbolometer

The test set-up for current-mode self-heating cancellation circuit evaluation is shown in Fig. 6.7. The function generator provides bias voltage to supply to one terminal of the microbolometer, while its other terminal is connected to the current-mode self-heating circuits in the ROIC. The pulse voltage bias generates the pulse current through the microbolometer. The current gain of the current-mode self-heating cancellation circuit is unity.

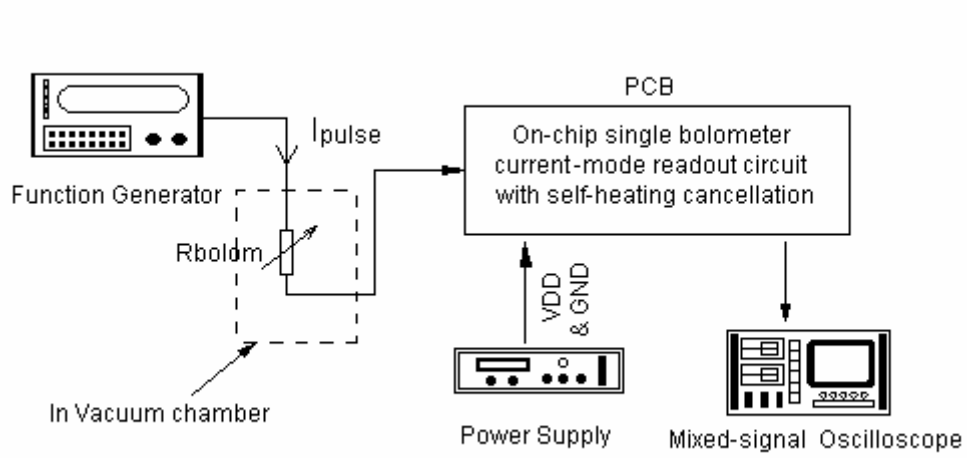


Fig. 6.7. Test set-up of the current-mode self-heat cancellation for single bolometer.

The measured result in Fig. 6.8 shows that the self-heating effect (I_d) is well resembled by its replica (I_{ref} - I_{ramp}), which indicates the good performance of the current-mode self-heating cancellation circuit. Fig. 6.9 shows the output of the I_{diff} integrated by the following integrator when IR input power was set to 175nW. It can be clearly observed that when there is no self-heating cancellation, the output of the integrator is dominated by the self-heating power and quickly becomes saturated. The input infrared signal is corrupted.

Following the same method used for the voltage-mode circuit, the residue error in I_{diff} after self-heating cancellation and its linear fit are obtained and shown in Fig. 6.10. The slope of the linear fit is about 8×10^{-5} A/s. At the end of 9 μs biasing period, I_{diff} only reaches 0.72 nA, compared with -0.56 μA (Fig. 6.7) when there is no self-heating cancellation. The self-heating effect is reduced by more than two orders of magnitude. The positive slope of the linear fit curve of the residual error indicates the cancellation circuit was slightly over tuned. There is also a small DC offset in I_{diff}, which is caused by the mismatch of the current mirrors in the circuit. The tunable feature of the current-mode self-heating cancellation circuit is demonstrated in Fig. 6.11.

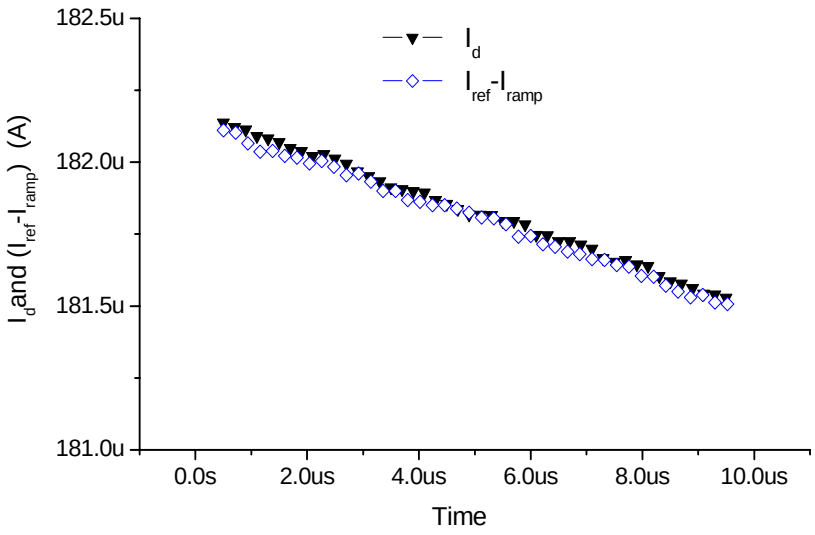


Fig. 6.8. Measured I_d and I_{ref} - $I_{ramp.}$

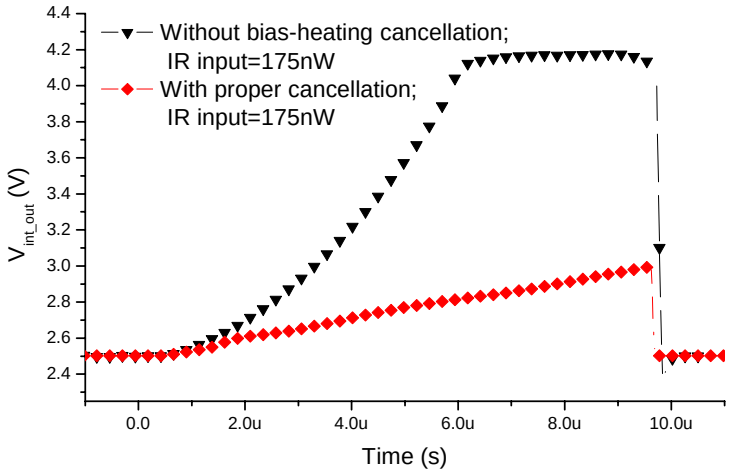


Fig. 6.9. Integrator outputs with and without self-heating cancellation, at input IR power of 175nW.

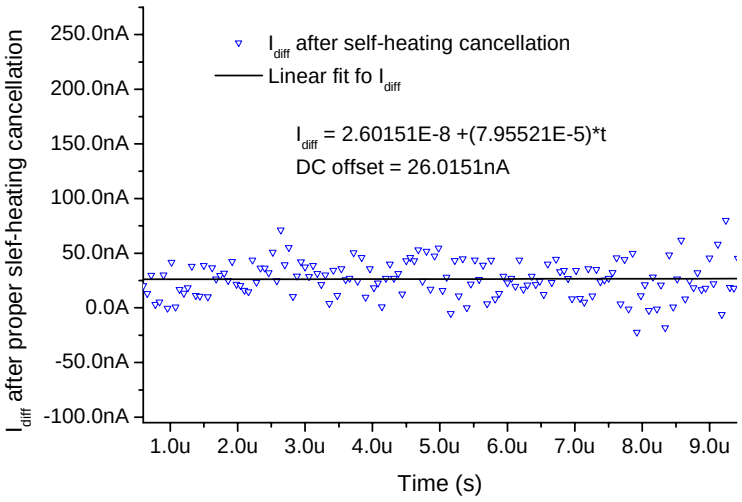


Fig. 6.10. Measured residue error (I_{diff}) after self-heating cancellation.

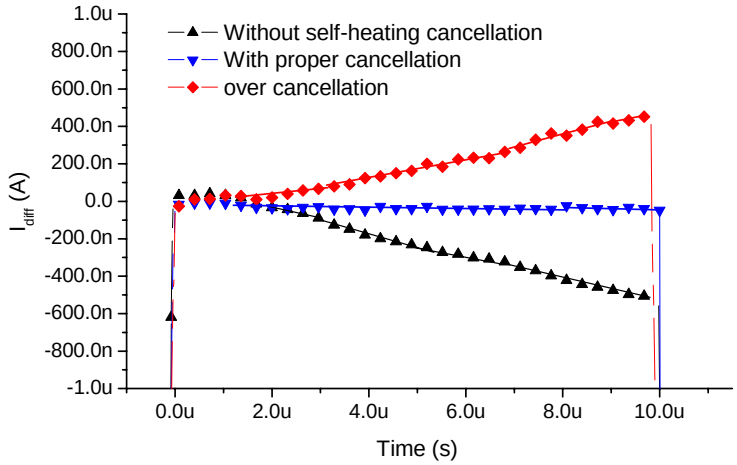


Fig. 6.11. Tunable feature of the current-mode self-heating cancellation circuit.

6.4. Test of the voltage-mode ROIC with an external microbolometer FPA

According to the original research plan, a new two-dimensional Ti microbolometer FPA was to be designed by Institute of Microelectronics (IME) for the ROIC described in this work and the ROIC was to be designed at National University of Singapore based on the specifications of the new FPA given by IME. The two parts will be integrated either in a hybrid or monolithic form and evaluated. However, due to the change of research plan at IME, the design of the new FPA was not carried out. Consequently, the readout circuit can only be tested with the existing mirobolometer FPAs which have different specifications from the originally planed one. As a result, the voltage-mode ROIC was tested with the 128 × 128 two-dimensional titanium microbolometer FPA described in section 6.1. The microbolometer FPA used in the test has a relatively larger fixed pattern noise than originally considered in the ROIC design. The digital ground on FPA cannot be totally separated from the analog ground. This has imposed some restrictions on the evaluation and reduces the signal-to-noise (S/N) ratio of the readout circuit.

6.4.1. Test set-up of the voltage-mode ROIC

The test set-up of the on-chip voltage-mode readout circuit with microbolometer FPA is illustrated in the Fig. 6.12, which consists of the interface printed circuit board with the ROIC chip, the microbolometer FPA chip mounted onto the camera body, and National Instrument PCI-6025E data acquisition (DAQ) card. The regular DC power supply provides the power for PCB and FPA chip. The computer with the DAQ card

generates the signals, which start and control the operation, and performs the image data acquisition. The ROIC performs the voltage-mode readout for the microbolometer FPA with self-heating cancellation and coarse FPN correction.

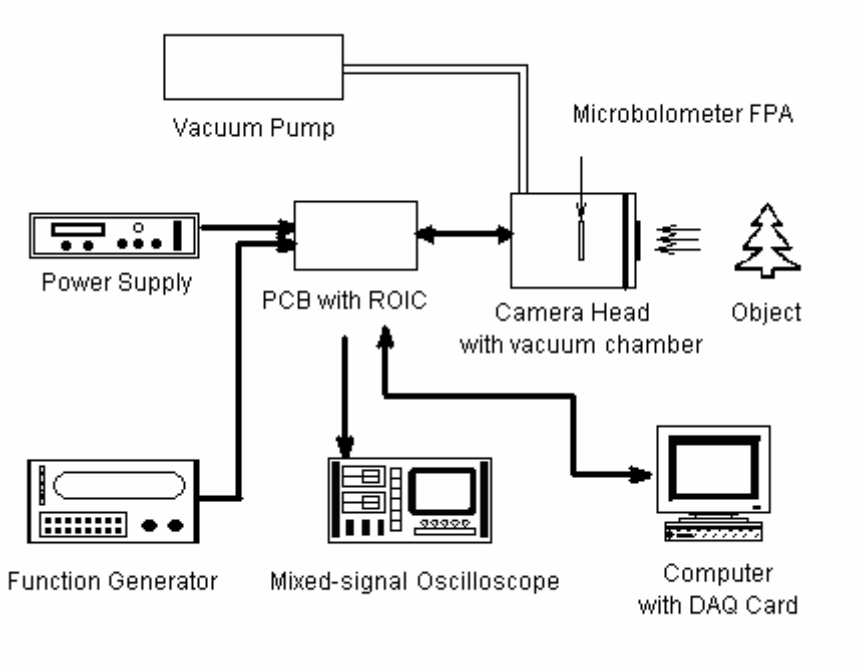


Fig. 6.12. Test set-up for voltage-mode readout circuit.

During the test, the microbolometer FPA chip is attached to a vacuum dewar, a vacuum chamber to prevent the loss of sensitivity due to thermal convection through air. The optical lens of the IR camera head is a germanium lens with focal length of 50 mm, which is used to focus the IR image of the object. A function generator is used to generate the master clock signal, *CLK,* for the ROIC, from which other clock signals are derived. During the readout, each microbolometer is momentarily biased and its output is sent to ROIC. Finally, the analog image signal is acquired by PCI-6025E DAQ card and the digitized image is stored on computer. PCI-6025E has 8 differential analog input channels with 12-bit A/D converter resolution and two 12-bit D/A channels[141]. Its digital I/O unit has bidirectional digital data lines, which can be programmed by users. To programming the DAQ card, the LabVIEW graphic

program language is used. The data acquisition program for testing the voltage-mode readout circuit performs the raw image data acquisition and other processing functions, including fine calibrating, averaging, noise calculation and image display.

6.4.1.1. Hardware interface of the test system

The hardware interfacing between the FPA, ROIC, other circuits on PCB and the DAQ card are shown in Fig. 6.13. The FPA chip required two DC power supplies, *VDD* and *Vbias*. *VDD* is the mian power supply for the on-FPA circuits, while *Vbias* is for the microbolometer bridge. The *main_clk* signal from the ROIC is used as the pixel clock of the FPA. The IR image signal sensed by microbolometer in each pixel is the input signal, *FPA_out* (equivalent to V_A in Fig. 4.1) to the voltage-mode readout circuit. Another output signal from the FPA chip is the frame synchronization signal. When the *main_clk* starts, the scan begins from an arbitrary pixel of the array depending on the status of the horizontal and vertical shift registers. However, a single positive pulse will be generated when the last pixel (128, 128) is selected. Thus, the negative edge of the frame synchronization pulse indicates the position of the signal from the first pixel (1, 1). This signal is used to synchronize the operation of the ROIC and the data acquisition.

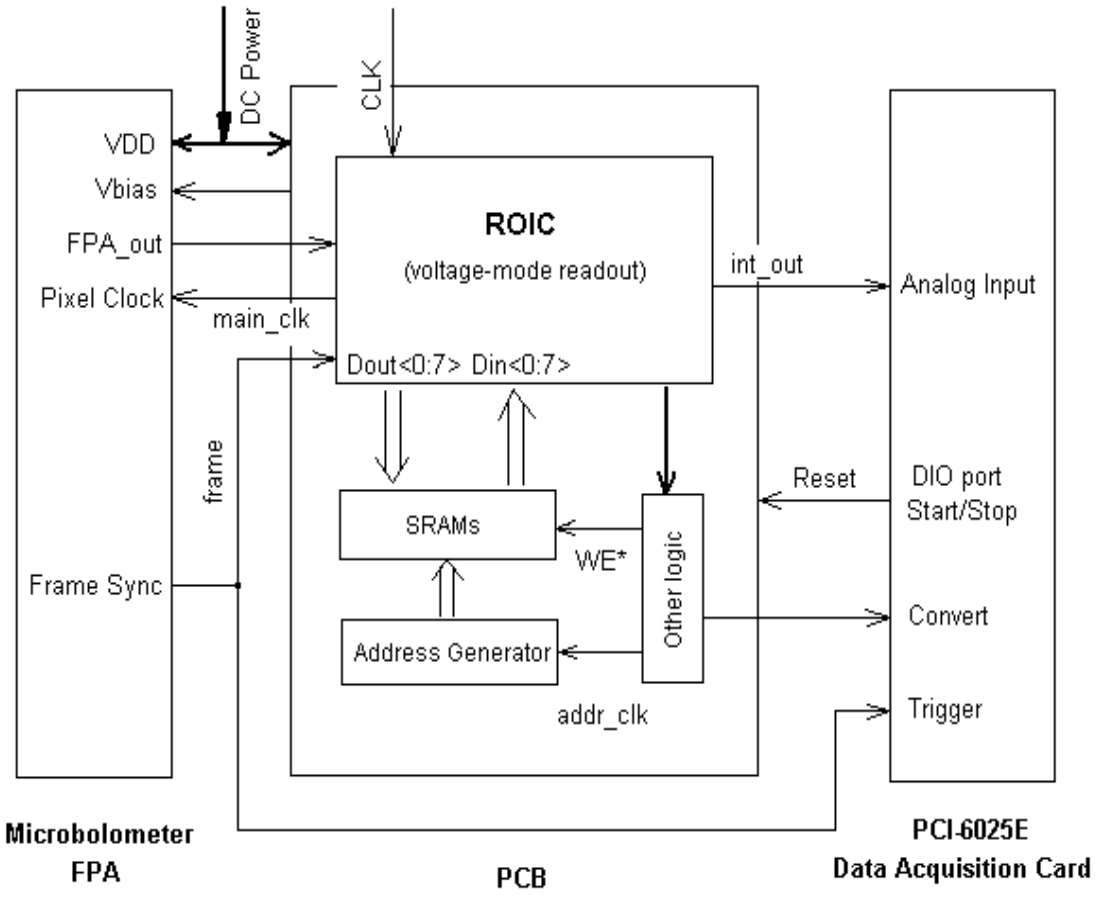


Fig. 6.13. The signal flow diagram of the hardware interface of the test system.

The on-chip voltage-mode readout circuit with the self-heating cancellation and fixed pattern noise correction has been described in the Chapter 4. The ROIC is mounted on the PCB, with the off-chip SRAMs, RAM's address generator and some simple logic circuits. Fig. 6.14 shows the schematic of the digital circuitry on PCB. In calibration operation, the fixed pattern noise data output from the *Dout* port of the ROIC and stored in the off-chip SRAMs. At the mean time, the analog data acquisition unit on the DAQ card is disabled. In imaging operation, the FPN data are read from SRAMs and fed back to the *Din* port of ROIC for the 8-bit coarse FPN correction. The computer data acquisition is also activated and triggered by the frame synchronization signal of the FPA.

The DAQ card sends out a *Start/Stop* signal from its DIO port to control the operation of the whole system. When this signal is low, all the registers and counters in ROIC and on PCB are cleared and no signal is read out. When the *Start/Stop* signal is high, ROIC is enabled and generates the clocks to drive the FPA and other circuits on PCB. Meanwhile the signal from FPA is streamed into ROIC and the coarse FPN correction (calibration mode) or data acquisition of the DAQ card (imaging mode) is carried out. A *Convert** signal is required by the data acquisition unit of the DAQ card as the A/D clock, whose falling edge indicates the occurring of and A/D conversion.

The low period of the *int_clk* is the actual readout period of each microbolometer pixel. In this period, the amplified pixel signal is integrated to minimize the thermal (Johnson) noise. The integrated pixel signal output is pipelined into an analog input channel of the DAQ card and converted into digital image data at the *Convert** falling edge. The *Convert** signal is designed such that its period is same as the *int_clk* so that in every *Convert** cycle only one pixel signal streaming out from the ROIC is sampled and converted to digital data in the DAQ card. However, they are also designed to have different phase and duty cycle so that the time interval from the falling edge of *Convert** to the rising edge of *int_clk* is long enough to satisfy the setup time of the A/D converter. This also minimizes the noise injection due to the clock transition and the switching noise from the ϕ_1 and ϕ_2 pulses on ROIC's self-heating cancellation circuit. The relationship of the *main_clk*, *int_clk* and the *Convert** is sketched in the Fig. 6.15.

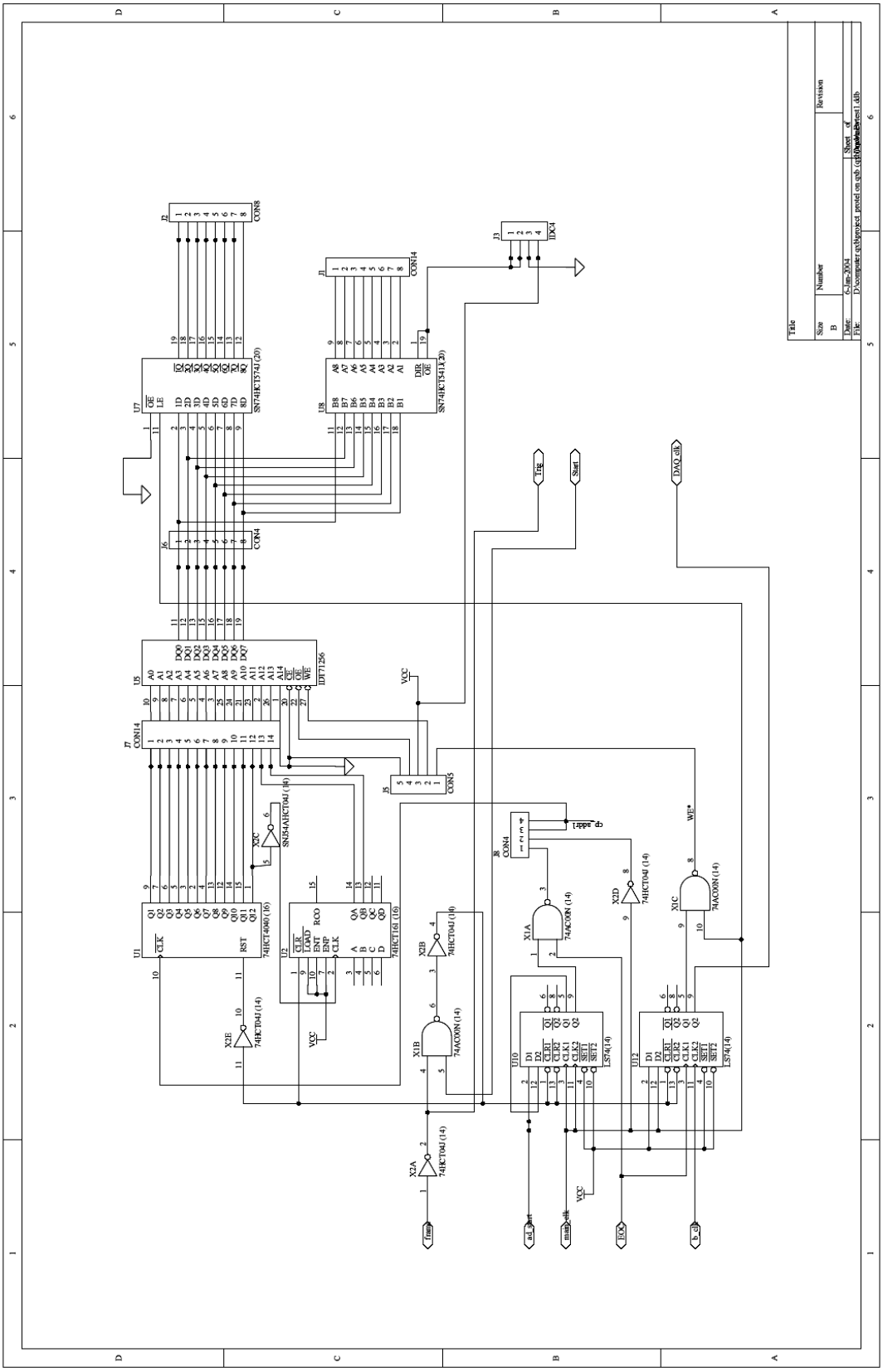


Fig. 6.14. Schematic of the digital circuit on the PCB.

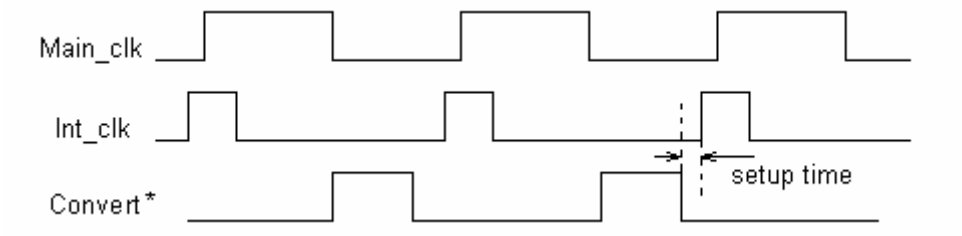


Fig. 6.15. Relationship of *main_clk*, *int_clk* and *Convert**.

The simple logic circuitry on PCB generates the *Convert** signal and other control signals, which are needed by SRAM (IDT71256) and SRAM address generator, such as *WE** for SRAM and the clock of the address counter. The operation of the PCI-6025E Data Acquisition card is programmed and controlled by the image acquisition software, which is described in the next section.

6.4.1.2. Image acquisition software

An image acquisition software was written in LabVIEW [142] to control the operation of the test system.

Normally, image calibration operation was performed before any image is captured. Covering the optical lens completely, several frames were taken and averaged to reduce the random noise of the system. These averaged signals were saved and served as the calibration data for subsequent imaging to provide the one point fine correction of the fixed pattern noise. During imaging process, the acquired frame was subtracted from the calibration frame to remove the FPN and then forms the calibrated image data. Simple noise analysis was performed for both calibration data and the calibrated images.

The real time imaging interface of the image acquisition software is shown in Fig. 6.16. Noise analysis results are shown in the Data Analysis Panel. Two image display windows display the acquired raw image without 1-point FPN correction and the calibrated image after FPN correction respectively.

Fig. 6.17 shows the flow chart of the image acquisition software. The major functions of the image acquisition software are initializing the data acquisition hardware, real time image data acquisition, 2-D frame reconstruction, 1-point FPN calibration, noise measurement, real time image display, save or load calibration file and image file.

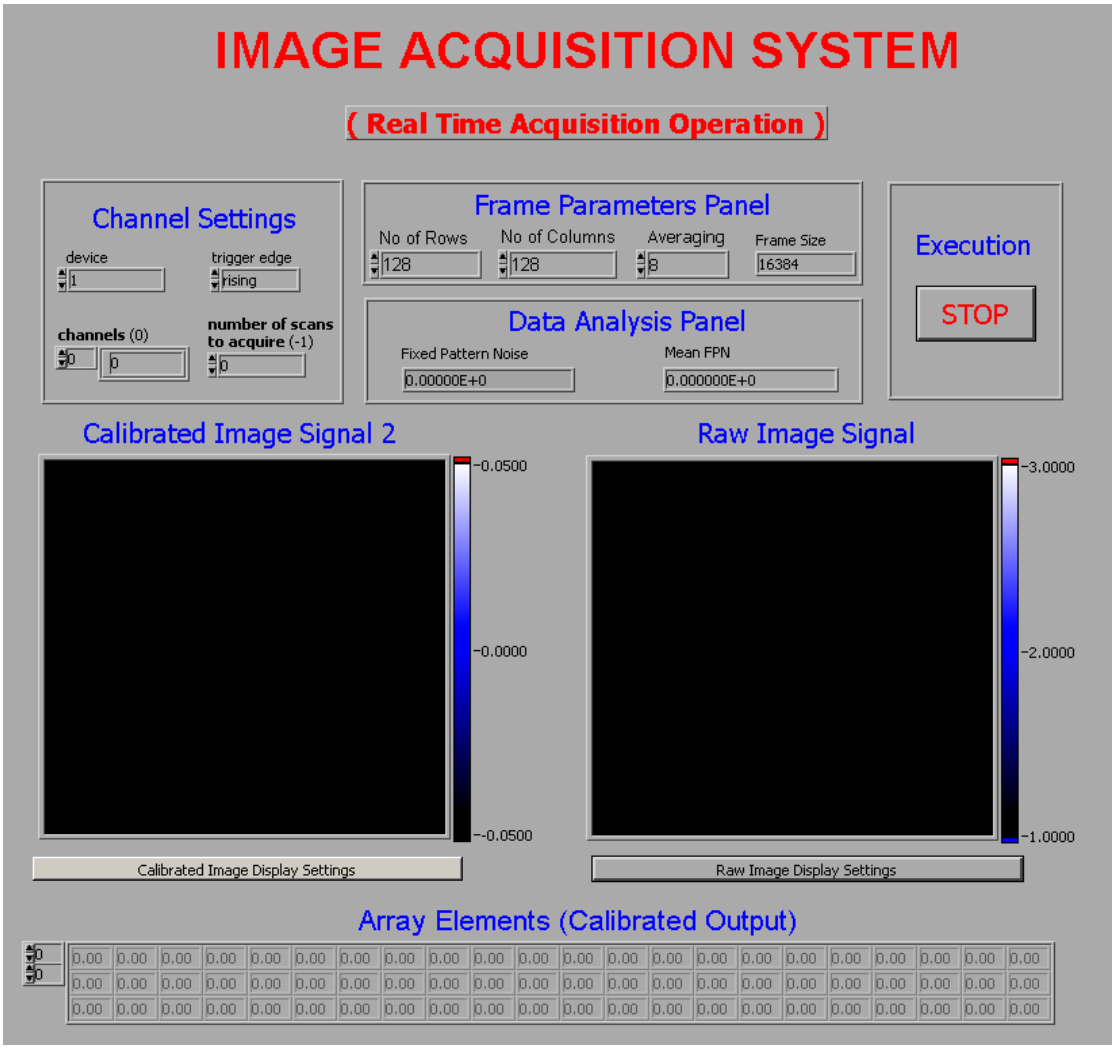


Fig. 6.16. User interface of image acquisition

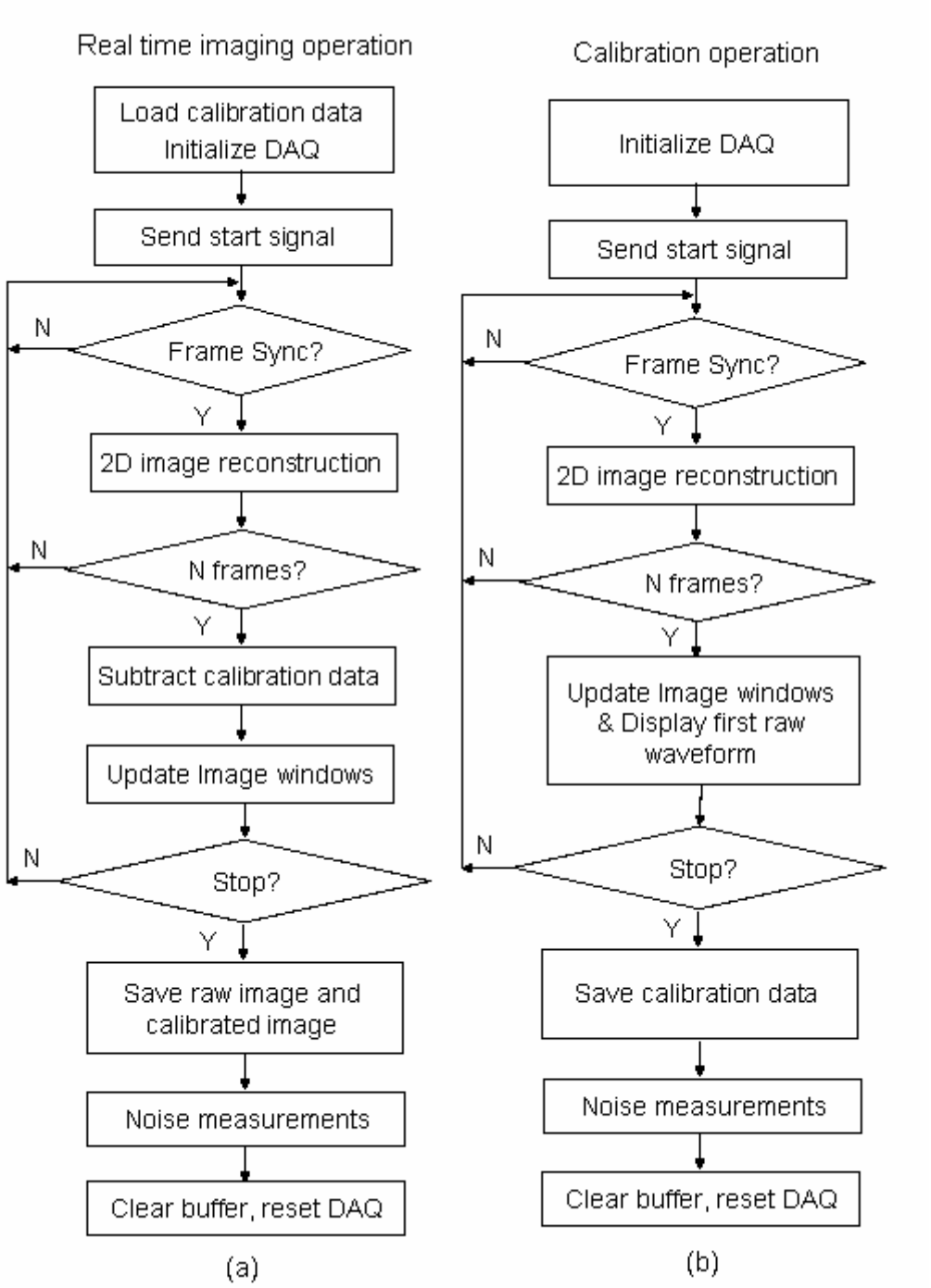


Fig. 6.17. Flow chart of the Image Acquisition LabVIEW programs (a) Real time imaging operation; (b) Calibration operation.

6.4.2. Test results of the voltage-mode ROIC

The voltage-mode ROIC was tested using the external FPA chip, which was mounted inside a vacuum chamber of an IR camera head. The vacuum was kept as low as 10^{-4}

Torr. During the test, the bias period of each microbolometer pixel was set to 10 μs to achieve integration time of about 8.6 μs. The ROIC and microbolometer FPA were operated under 5 V power supplies. The digital circuitry and analog circuitry on ROIC use different power supplies to reduce the crosstalk. The room temperature resistance of the microbolometers in the FPA is around 5 kΩ. The on-chip dummy resistor of the Wheatstone bridge to balance the micrbolometer resistance was designed to 5 kΩ. The gain of preamplifier on the ROIC was approximately set to unity when the circuit is operated in the calibration mode to avoid the saturation due to large FPN.

The calibration process was performed before entering thermal image mode. Several frames were acquired with the optical lens closed and no FPN correction was applied. At the same time, the last frame FPN data was saved in the SRAM, which was later used for on-ROIC FPN correction. With the optical lens was still covered, the system executed the calibration operation program again. However, at this time, the FPN data stored in the SRAM was loaded back to the ROIC. The readout circuit on ROIC now performs self-heating cancellation and on-chip FPN coarse correction. The DAQ card acquired the analog output of the ROIC, and the FPN data before and after 8-bit on-chip coarse correction were displayed and saved.

In the measurement, the FPN data should be first acquired while the optical lens is closed. The FPN data acquired from the first row in the microbolometer FPA is shown in Fig. 6.18, where the x-axis indicates the position indexes of the pixels in the first row and y-axis is the output voltage of the integrator in ROIC. Fig. 6.19 depicts the 2-D intensity graph of the fixed pattern noise before the coarse correction. The x, y axes indicate the position indexes of the pixels in the corresponding rows and columns, respectively. The intensity bar shows the output voltage of the integrator,

which represents the amplified FPN of each pixel. It can be observed that there is considerable variation of signals from different pixels that has been coded into different blue color scale, even though there is no incoming radiation. Furthermore, either from the waveform chart of the first raw signals or the 2-D graph, it can be seen that pixels of the last column have the output of nearly zero. It might be caused by the bad pixels or the faulty multiplexer circuit in the FPA. Thus, this last column is excluded in the measurement. The integrator output from ROIC is adjusted to around 0 ~ 5V in order to fully use the circuit dynamic range.

Fig. 6.18. Output waveform chart of the first row of FPA without FPN correction.

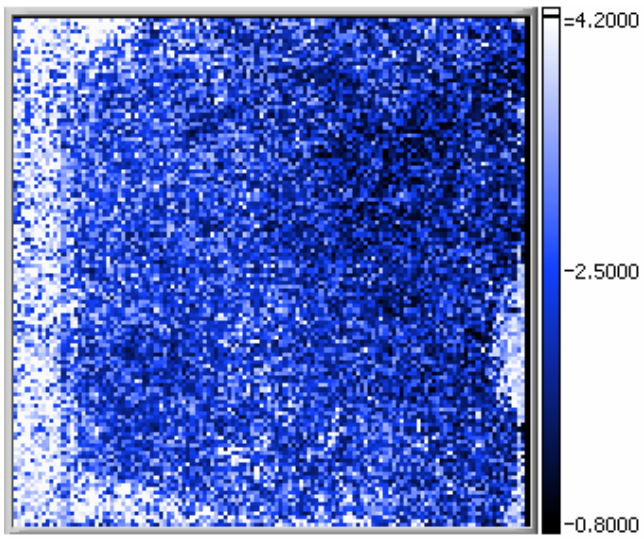


Fig. 6.19. Measured 2-D intensity graph of the FPA without coarse FPN correction.

The same measurements are repeated for the case with the 8-bit on-chip coarse FPN correction applied. The residual FPN outputs of the first raw pixels are shown in Fig. 6.20. It can be seen that the non-uniformity of the FPN outputs are greatly reduced when the 8-bit on-chip fixed pattern noise correction is applied. The effect of coarse FPN correction can be clearly observed from the intensity graph acquired in Fig. 6.21 where (a) uses the same intensity scale as that in Fig. 6.19 and (b) shows a zoom-in version. The first pixel of the frame (at the left-bottom corner) and the pixels in the last column are excluded in the measurement. The former is due to an error in the synchronization, while the latter could be due to the defect in the FPA.

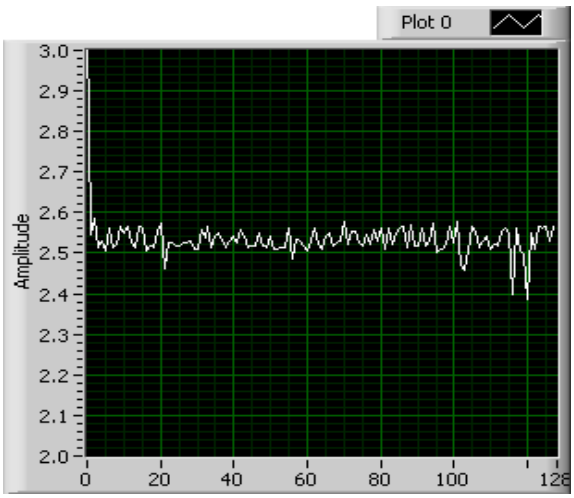
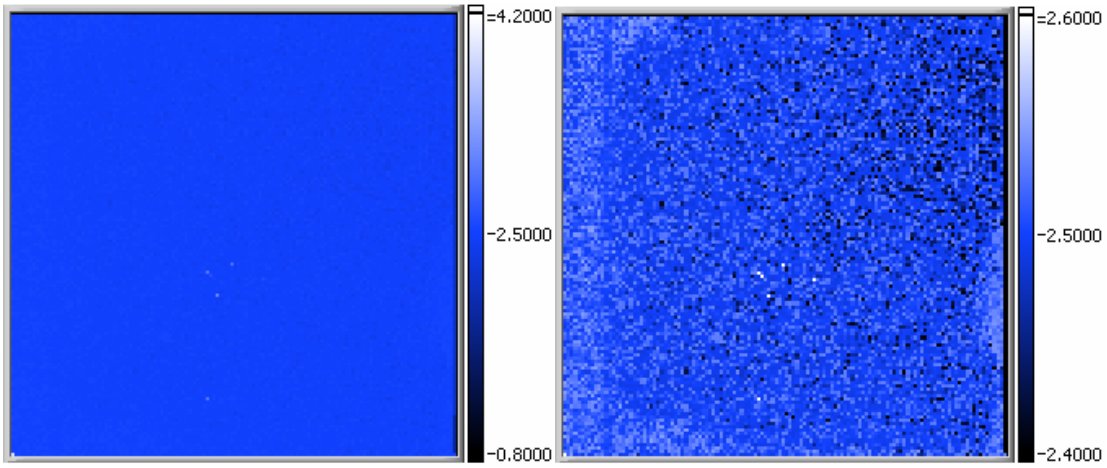


Fig. 6.20. The residual FPN readings of the first raw of FPA.



(a) (b)

Fig. 6.21. The residual fixed pattern of the FPA after on-chip correction: (a) Intensity scale is same as that in Fig.6.19 and (b) Intensity scale is reduced.

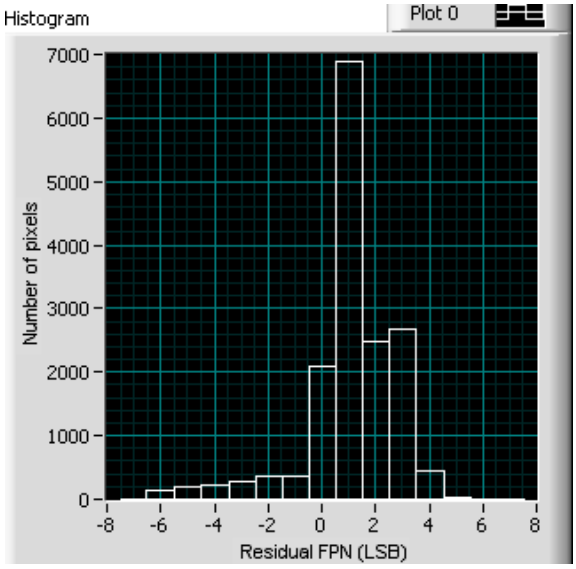


Fig. 6.22. The histogram of the residual FPN.

The noise measurement program gives the maximum and minimum values of residual FPN data, which are 2.5934 V and 2.3702 V, respectively. The mean of the residual FPN is 2.5203 V and the standard deviation (σ) is 0.0342V. The 8-bit on-chip FPN correction circuit is expected to correct the FPN in range of 0 to 5 V to less than ± 1 LSB, or ± 19.6 mV. However, the residual FPN are within the range of -7 LSB to 5 LSB. The histogram in Fig. 6.22 shows the distribution of the residual FPN. Although the on-chip FPN correction can only provides 5½ -bit correction, there are 85.6% pixels are corrected to lower than ±2 LSB and 93.2 % pixels to lower than ±3 LSB.

The slightly large residual FPN might result from the poorly fabricated mcirobolometer FPA which has an unexpectedly large fixed pattern noise measured to be approximately in range of ± 600 mV at the input of ROIC, while the maximum input referred FPN the ROIC can handle is ±130 mV.

If those pixels whose original FPN are out of range of ±130 mV are excluded in the analysis of the residual FPN, better results can be obtained. The maximum and minimum values of residual FPN data become 2.5573 V and 2.4812 V, respectively. The standard deviation is now 0.0180 V. Thus, the residual FPN are in range of -1 LSB to 3 LSB. Thus, the correction to 7-bit resolution is achieved.

In order to properly evaluate the performance of the on-chip FPN correction circuit, an on-chip dummy bolometer array which contains 32-element polysilicon resistors as the pixels was used in the measurement. The resistance values of these resistors are within about ±10% variation of 5 kΩ to mimic the typical non-uniformity observed in microbolometer FPAs. A ±10 % non-uniformity of pixel resistance gives a FPN of ±130 mV in our Wheatstone bridge circuit. The FPN was first digitized and stored in the off-chip memory during the calibration and later used for the correction. After correction, the 8-bit digitized residual offset noise at the output of the A/D converter is shown in the Fig. 6.23.

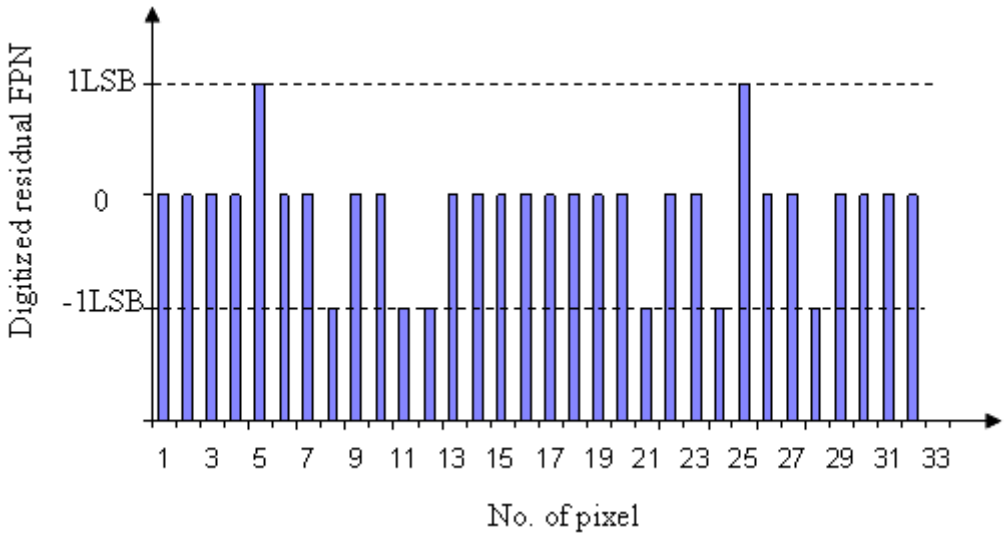


Fig. 6.23. Residual error of FPN correction when tested with a resistor array.

It can be seen that the on-chip FPN correction reduces the offset noise to less than ±1 LSB. After the 8-bit on-chip correction, the input referred residual error is within ±1 mV. The results prove that the designed 8-bit fixed patter noise correction circuit is working properly if the condition of the input signal is within the operation limits.

The second step of the measurement is the software calibration of the residual FPN and the real-time IR image acquisition. With the on-chip FPN correction applied, the gain of the readout circuit can be increased by reducing the time constant of the on-chip integrator. While the lens is closed, the calibration data, which is the residual FPN with the increased gain, are stored in computer for subsequent software fine calibration in real time imaging operation. When real time imaging is carried out, the optical lens is open and the calibration data is loaded. The LabVIEW program carries out the 1-point FPN correction, which is a linear correction by subtracting the stored residual FPN calibration data from the raw image data to produce a 2-D calibrated image.

However, since the available microbolometer focal plane arrays are not well matched with our designed ROIC, the performance of the whole readout system is not satisfied. The real-time IR image could not be clearly observed. One of the possible reasons, as mentioned before, is that the FPN of the microbolometer array under test is too large to be handled by our readout circuit (± 600 mV cf. ± 130 mV). Thus, the performance of the readout circuit is greatly degraded and the IR signal is overwhelmed by the large residue FPN. When the overall gain of the ROIC is reduced to around 400 to accommodate the FPN, the useful IR signal cannot be adequately amplified. Typical IR signals from room temperature objects are of the order of several millivolts. With the gain of 400, the 12-bit ADC on the DAQ card is

unable to resolve such a small signal. Furthermore, the noise introduced by the long wire connections between the FPA in the vacuum dewar and PCB, and by the shared digital and analog ground in FPA will further reduce the S/N (signal-to-noise) ratio. These are the main reasons that make the IR signals unreadable.

6.5. Test of the on-chip current-mode FPN correction

Since the available FPA cannot be used to evaluate the current-mode ROIC (due to the built-in on-chip readout circuit shown in Fig. 6.10), the current-mode readout circuit is only tested with a built-in 8 × 8 resistor array as a dummy FPA since the microbolometer FPA for current-mode output is unavailable. The variation of the resistor values was designed to be within ±10 % of 5 kΩ, which gives a FPN range of ±26.5 μA, similar to the case in the voltage-mode readout circuit.

The test set-up of the current-mode FPN correction circuit is similar to the voltage mode and shown in Fig. 6.24. The ROIC is mounted on a PCB, which includes logic circuits, 2 blocks of SRAM and their address generators. The off-chip SRAM1 is used to store the FPN and calibrated data, while the block SRAM2 is built on PCB to store the calibrated data after the on-chip FPN correction. A function/arbitrary waveform generator is used for *CLK* signal generation. A mixed-signal oscilloscope displays the ROIC output.

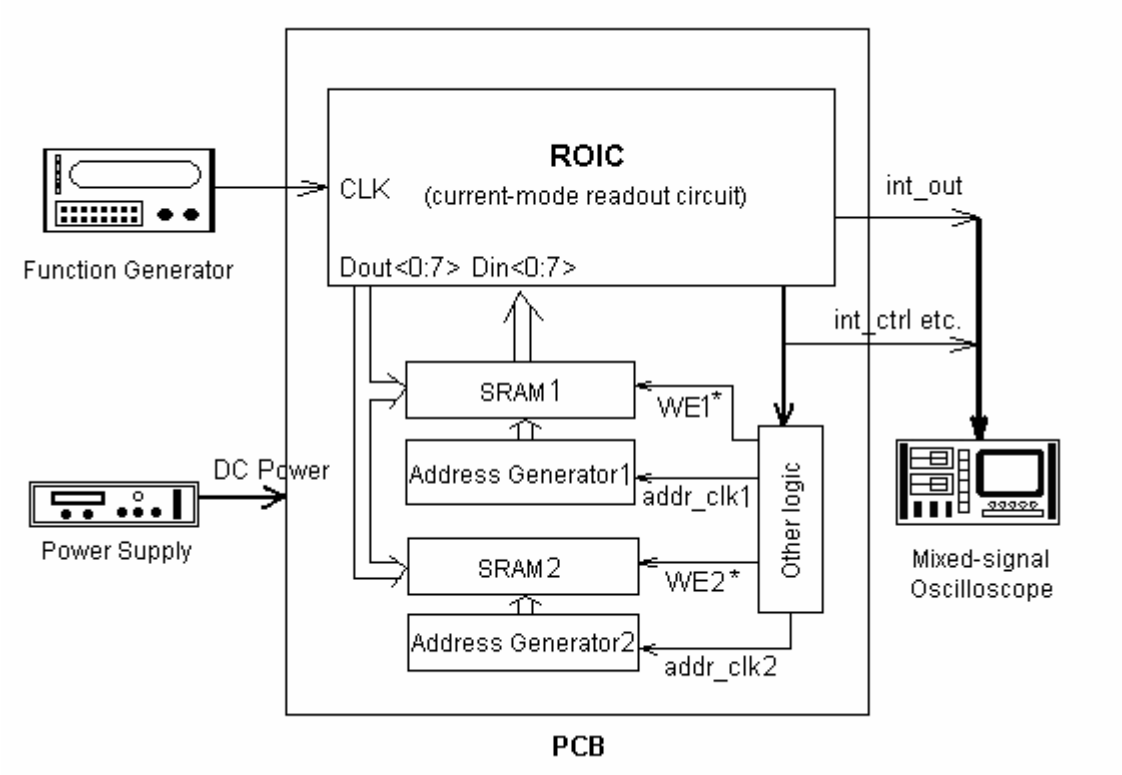


Fig. 6.24. Test set-up for current-mode FPN correction circuit on ROIC.

The first step of the on-chip coarse FPN correction for the current-mode readout circuits is the calibration operation, while the connection between the output of the current-steering DAC and the input of the integrator is disconnected. During the calibration mode, the FPN generated by the resistor array was written into one of the off-chip SRAMs. During imaging operation, the FPN data were read from SRAM and fed back to the output of the current subtraction circuit through the on-chip current DAC. The connection between the DAC and integrator was connected so that the calibration current output from DAC compensates the offset current, I_{diff}. The residual error current was integrated by the integrator and digitized by on-chip ADC again. The data generated in this operation mode was stored in another off-chip SRAM. The on-chip ramp current generator was disabled during the test since the

fixed value resistors used to simulate the microbolometer having no self-heating effect.

The digitized residual FPN after 8-bit on-chip coarse correction is plotted in the Fig. 6.25. It can be seen that the FPN noise is reduced to less than ±2.5 LSB. As the largest FPN handled by the on-chip feedback circuit is 8-bit, the residual fixed pattern noise is within ± 0.98% after FPN cancellation, which is near 7-bit resolution. The results can be made better if the adjustable design for the 1 LSB reference current is adopted for on-chip current-steering DAC. This may be realized by including a tunable voltage reference with bandgap source, and convert it to the adjustable reference current, *1LSB_ref*.

The waveforms of the analog output of the current integrator (for several resistor pixels) before and after FPN correction are shown in the Fig.6.26 (a) and (b), respectively, where trace D7 is *int_ctrl*, which controls the integration time of the current I_{diff} of each pixel.

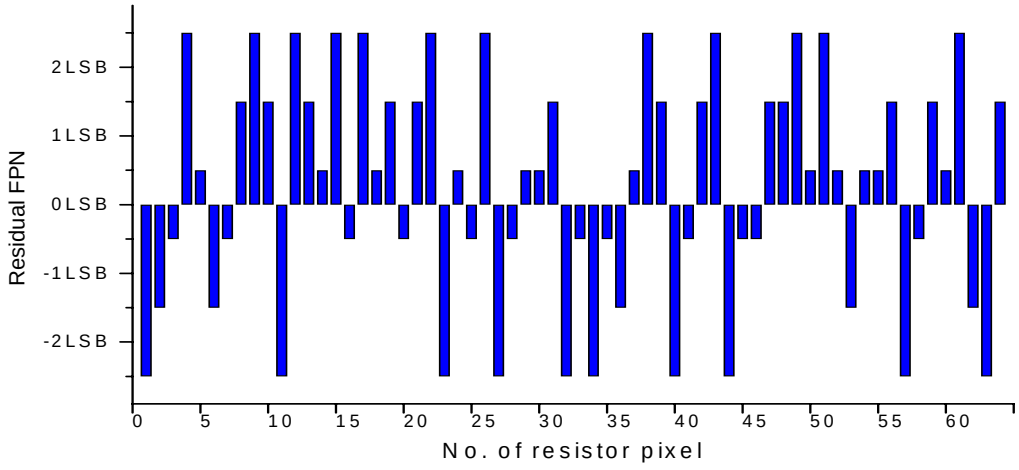
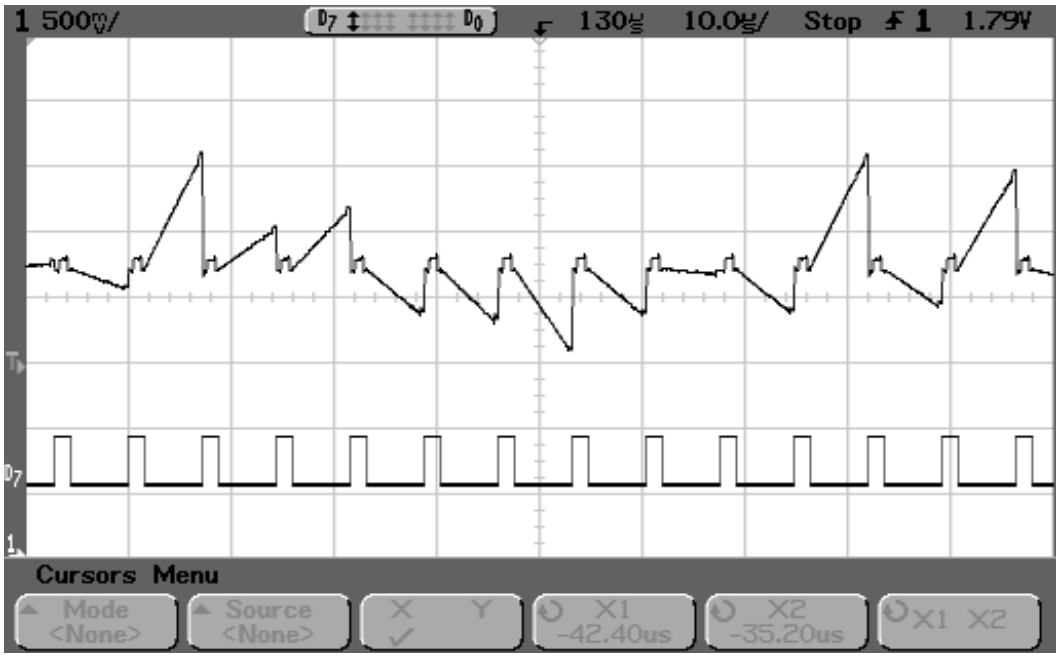
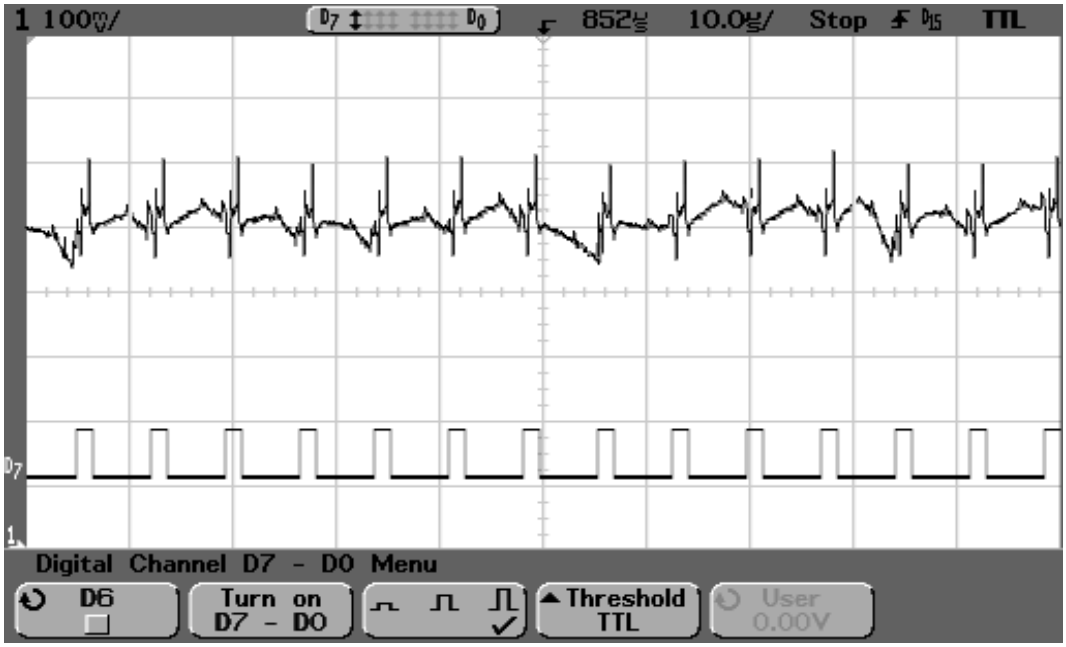


Fig. 6.25. Measured residual error after coarse FPN correction.



(a)



(b)

Fig. 6.26. Output waveform of the on-chip current integrator. (a) before and (b) after coarse FPN correction.

6.6. Summary

Microbolometer ROIC with self-heating cancellation and fixed pattern noise correction circuits in both voltage- and current-modes were fabricated in a 0.6-μm standard CMOS process. The fabricated chips were evaluated with both single bolometer and an external FPA. The effectiveness and tuneable feature of the self-heating cancellation circuits for both voltage- and current-mode readout have been demonstrated. When there is no self-heating cancellation, the measured outputs of the integrator were saturated due to large self-heating noise, which indicates the necessity of the self-heating cancellation circuits in ROIC.

The voltage-mode ROIC has been measured using the external 128×128 microbolometer FPA. The measurement results for the 8-bit on-chip fixed pattern noise correction shows that it is able to provide 5½-bit correction when tested with the microbolometer FPA. The degradation in the performance of the correction with FPA is believed to be caused by the unexpected large non-uniformity of the microbolometer FPA. If the pixels with large FPN were excluded in measurements, the 7-bit resolution can be achieved. The FPN correction circuit attains 8-bit correction when measured with an on-chip resistor array.

Since the existing microbolometer FPA is not suitable for the current mode ROIC, the current-mode FPN correction circuit has been measured with an on-chip resistor array. The results show that the on-chip coarse FPN correction can reduce the FPN to less than ±2.5 LSB.

Since the integration of microbolometer FPA and ROIC could not be carried out, the large FPN and readout circuit in the existing microbolometer FPA have, in some way, prevented the fabricated voltage- and current-mode ROIC from being fully evaluated. The large FPN is believed to be the main reason for which the real-time IR image could not be detected.

Chapter 7. Conclusions

7.1. Conclusions

A new self-heating cancellation technique suitable for microbolometer IR detectors and arrays has been proposed in this thesis. The cancellation is based on the equivalence between the electrical and thermal system, by which the thermal capacitance can be represented by a capacitance in the electrical domain. Therefore the self-heating effect in the thermal domain can be easily generated using a current source and capacitor, which can be later used to cancel the self-heating effect itself.

The newly proposed self-heating cancellation concept has been successfully implemented and demonstrated in a voltage- and a current-mode readout circuit for single microbolometer. The test results of the fabricated chips have shown that the self-heating effect can be reduced by at least two orders of magnitude in both voltage- and current-mode readout circuits.

A SPICE electro-thermal model of microbolometer has been constructed to study the behaviours of the microbolometer and gain better understanding of the self-heating effect. The model has been validated by the experiment data and used in the design of the self-heating cancellation circuits.

The ROIC with the proposed voltage-mode self-heating cancellation circuit has been developed together with an 8-bit FPN correction circuit. The ROIC is fabricated in a 0.6 μm CMOS technology and evaluated with an external 128 × 128 microbolometer

FPA. The test results have shown that the FPN can be corrected to a 5½-bit resolution against the expected design specification of 8 bits. This is attributed to the unexpected large FPN in the IR FPA under test, which is observed during the test. When this factor is excluded from the test, the resolution of the correction is improved to 7 bits. This has also been approved by a test in which the FPA is replaced by a resistor array, whose resistance variation resembles the FPN in the microbolometer FPA. The correction of 8-bit has attained in this case.

The current-mode self-heating cancellation circuit has also been incorporated in a current-mode ROIC with an 8-bit FPN correction. However, since the microbolometer FPA for current-mode ROIC is not available, the fabricated ROIC can only been evaluated with a built-in 8 × 8 resistor array for the performance of FPN correction. The measured residual FPN of less than ±2.5 LSB has been achieved.

7.2. Original contributions

The concept of using the equivalence between the electrical and thermal system for the cancellation of the self-heating in microbolometer is first proposed in this thesis. The voltage- and current-mode self-heating cancellation circuits have been successfully demonstrated and the results are published in [136] and [138]. A Singapore and US Provisional patent have been filed for the voltage- and current-mode self-heating cancellation circuits, respectively. In addition, the proposed concept can be applied to the design of the readout circuits for other types of sensors, where similar problem exists.

7.3. Future work

The evaluation of the ROIC in this thesis is restricted by the availability of the suitable microbolometer FPAs. Thus, to properly evaluate the ROIC with the proposed self-hearing cancellation circuit, the integration of the readout circuit with a microbolometer focal plane array should be further pursued. To reduce the FPN, an option to place the load resistor (in Wheatstone bridge) in the pixel and near the detector using same material as the microbolometer, can be explored. With such an arrangement, the non-uniformity or FPN of the FPA is expected to be greatly reduced. This is because the resistance ratio of the bolometer and its load can be kept at relatively constant. Moreover, the low noise design approach should be adopted in the future implementation of the ROIC to ensure the high signal-to-noise ratio required for IR imaging at room temperature.

References

[1] Schlessinger, M. Infrared Technology Fundamentals. – 2nd edition. pp.1-25, Marcel Dekker Inc. 1995.

[2] Burnay, S.G., T.L. Williams and C.H. Jones. Applications of Thermal Imaging. Adam Hilger, Bristol. 1988.

[3] Rogalski, A. and K. Chrzanowski. Infrared Devices and Techniques, Opto-Electronics Review, *Vol.10(2)*, pp.111–136. 2002.

[4] Dereniak, E. L. and G. D. Boreman. Infrared Detectors and Systems. pp.395-438, John Wiley and Sons, 1996.

[5] P.R. Norton, Infrared Detectors in the next millennium, Proc. SPIE, *Vol.3698*, pp.652–665. 1999.

[6] Kaplan, H. Practical Applications of Infrared Thermal Sensing and Imaging Equipment, SPIE Optical Engineering Press, 1993.

[7] Dempsey, R.J., D.G. Davis, R.G. Jr. Bruice and R.A. Lodder. Biological and Medical Applications of Near Infrared Spectrometry, Applied Spectroscopy, *Vol.50(2)*, pp.18A-34A, 1996.

[8] Kruse, P.W. Uncooled Thermal Imaging Arrays, Systems, and Applications, SPIE Press, 2001.

[9] BAE Systems Information and Electronic Systems Integration Inc., Uncooled imagery, Mar. 2003. URL: http://www.iews.na.baesystems.com/iris/unc-imagery.htm. (Accessed on Apr. 22nd, 2003).

[10] He, X., G. Karunasiri, T. Mei, W. J. Zheng, P. Neuzil and U. Sridhar. Performance of Microbolometer Focal Plane Arrays under Varying Pressure, IEEE Electron Device Letters, *Vol.21*, pp.233-235. 2000.

[11] McDaniel, G. W. and D. Z. Robinson. Thermal Imaging by Means of the Evaporagraph, Appl. Opt., *Vol.1*, pp.311-324. 1962.

[12] Burnay, S. G., T. L. Williams, and C. H. Jones. Applications of Thermal Imaging, Adam Hilger, Bristol. 1988.

[13] Kruse, P. W. Thermal Imagers Move from Military to Marketplace, Photonics Spectra, *Vol. 29*, *No. 3*, p.103. 1995.

[14] Liddiard, K. C. Thin-film Resistance Bolometer IR Detectors, Infrared Physics, *Vol.24*, pp.57-64. 1984.

[15] Pommerenig, D. H., D. D. Enders and T. E. Meinhardt. Hybrid Silicon Focal Plane Array Development: An Update, Proc. Society Pho-Opt. Instrumentation Engineering, *Vol.267*, pp.23–30. 1981.

[16] Rogalski, A. Infrared Detectors. pp.3-152, Gordon and Breach Science Publishers, Amsterdam. 2000.

[17] Rogalski, A. Infrared Detectors: an Overview, Infrared Physics & Technology, *Vol.43*, pp.187 –210. 2002.

[18] Kinch, M. A., S. R. Borrello, D. H. Breazeale and A. Simmons. Geometrical Enhancement of HgCdTe Photoconductive Detectors, Infrared Phys., *Vol.17*, pp.137-145. 1977.

[19] Musca, C. A., J. F. Siliquini, K. A. Fynn, B. D. Nener, L. Faraone and S. J. C. Irvine. MOCVD-grown Wider-bandgap Capping Layers in $Hg_{1-x}Cd_xTe$ Long-

wavelength Infrared Photonconductors, Semicon Sci. Technolo. *Vol.11*, pp.1921-1922. 1996.

[20] Smith, D. L., D. K. Arch, R. A. Wood and M. W. Scott. HgCdTe Heterojunction Contact Photoconductor, J. Appl. phys., *Vol. 45*, pp. 83-85. 1984.

[21] Gunapala, S. D., S. V. Bandara, J. K. Liu, E. M. Luong, S. B. Rafol, J. M. Mumolo, D. Z. Ting, J. J. Bock, M. E. Ressler, M. Levy, N. LeVan, M. A. Fauci. Recent Developments and Applications of Quantum Well Infrared Photodetector Focal Plane Arrays, Opto-Electron. Rev., *Vol. 9*, pp.150 –163. 2001.

[22] Andersson, J. Y., Dark Current Mechanisms and Conditions of Background Radiation Limitation of N-doped AlGaAs/GaAs Quantum-well Infrared Detectors, J. Appl. Phys. *Vol.78*, pp. 6298–6304. 1995.

[23] Piotrowski, J., W. Galus and M. Grudzien. Near Room-temperature Photodetectors, Infrared Phys. *Vol.31*, pp.1-48. 1991.

[24] Butler, N., R. Blackwell, R. Murphy, R. Silva and C. Marshall. Low Cost Uncooled Microbolometer Imaging System for Dual Use, Proc. SPIE, *Vol. 2552*, pp. 583–591. July 1995.

[25] Foote, M. C., E. W. Jones, T. Caillat. Uncooled Thermopile Infrared Detector Linear Arrays with Detectivity Greater than 10^9 $cmHz^{1/2}/W$, IEEE Trans. Electron Devices, *Vol. ED-45*, pp.1896-1902. 1998.

[26] Almasri, M., D. P. Butler, and Z. Çelik-Butler. Self-supporting Infrared Microbolometers with Low Thermal Mass, IEEE/ASME Journal of Microelectromechanical Systems, *Vol. 10*, pp. 469-476. 2001.

[27] Baer, W. G., K. Najafi, K. D. Wise and R. S. Toth. A 32-element Micromachined Thermal Imager with On-chip Multiplexing, Sensors & Actuators A, *Vol. A48*, pp.47-54. 1995.

[28] Lenggenhager, R., H. Baltes and T. Elbel. Thermoelectric Infrared Sensors in CMOS Technology, Sensors & Actuators A, *Vol A37-38*, pp.216-220. 1993.

[29] Parameswaran, M., H. Baltes, L. Ristic, D. Dhaded and A. Robinson. A New Approach for the fabrication of Micromechanical Structures, Sensors & Actuators A, *Vol. 19*, pp.289–307. 1989.

[30] Howard, P. E., C. J. Han, J. E. Clarke, J. C. Stevens, P. A. Ely and E. T. Fitzgibbo. Advances in Microbolometer Focal Plane Technology at Boeing, Proc. SPIE, *Vol. 3379*, pp.47-57. 1998.

[31] Howard, P. E., J. E. Clarke, W. J. Parrish and J. T. Woolaway. Advanced High-Performance 320×249 VO_x Microbolometer Uncooled IR Focal Plane Array, Proc. SPIE, *Vol. 3698*, pp.131-136. 1999.

[32] Radford, W., D. F. Murphy, J. A. Finch, K. Hay, A. Kennedy, M. Ray, A. A. Sayed, J. Wyles, R. Wyles, J. B. Varesi, E. A. Moody and F. Cheung. Sensitivity Improvements in Uncooled Microbolometer FPAs, Proc. of SPIE, *Vol.3698*, pp.119-130. 1999.

[33] Breen, T. B., N. R. Butler, M. Kohin, C. A. Marshall, R. Murphy, T. W. Parker and R. J. Silva. Applications of Uncooled Microbolometer Sensors, Proc. SPIE, *Vol. 3379*, pp.145-156. 1998.

[34] Kohli, M., C. Wuthrich, K. G. Brooks, B. Willing, M. Forster, P. Muralt, N. Setter and P. Ryser, Pyroelectric Thin Film Sensor Array, Sensors & Actuators A, *Vol.60*, pp.147–53. 1997.

[35] Hanson, C. M. Uncooled Thermal Imaging at Texas Instruments, Proc. SPIE, *Vol.2020*, pp.330 –339. 1993.

[36] Noda, M., T. Miyamoto, S. Murakami, T. Nomura, K. Inoue and M. Okuyama. A Dielectric Bolometer Mode of Infrared Sensor Using a New $BaTi_{1-x}Sn_xO_3$ Thin Film with a High Temperature Coefficient of Dielectric Constant, Integrated Ferroelectrics, *Vol.49*, pp.305-314. 2002.

[37] Hashimoto, K., H-P. Xu, T. Mukaigawa, R. Kubo, H. Zhu, M. Noda and M. Okuyama. Si Monolithic Microbolometers of Ferroelectric BST Thin Film Combined with Readout FET for Uncooled Infrared Image Sensor, Sensors & Actuators A, *Vol.88, No.1*, pp.10-19, Jan. 2001.

[38] Anthony, C. J., M. A. Todd, P. P. Donohue, M. A. C. Harper, Z. Huang and J. C. Jones. High Performance PST Thin Films on Polysilicon Sacrificial Layers for Uncooled IR Detectors, Integrated Ferroelectrics, *Vol.* 49, pp.233-243. 2002.

[39] Huang, Z., P. P. Donohue, Q. Zhang, D. J. Williams, C. J. Anthony, R. W. Whatmore and M. A. Todd. Comparative Microstructure and Electrical Property Studies of Lead Scandium Tantalite Thin Films as Prepared by LDCVD, Sol-gel and Sputtering Techniques, J. Phys. D – Appl. Phys., *Vol.36*, pp.270-279. 2003.

[40] Kim, D. H. and H. S. Kwok. Pulsed Laser Deposition of VO_2 Thin Films, Appl. Phys. Lett., *Vol.65*, pp.3188-3190. 1994.

[41] Chen, C.-H., X.-J. Yi, X.-R. Zhao and B.-F. Xiong. Characterizations of VO_2-based Uncooled Microbolometer Linear Array, Sensors & Actuators A, *Vol. 90*, pp.212-214. May 2001.

[42] Jerominek, H., F. Picard and D. Vincent. Vanadium Dioxide Films for Optical Switching and Detection, Opt. Eng., *Vol.32*, pp.2092-2099. 1993.

[43] Kuzma, E. Contribution to the Technology of Critical Temperature Resisters, Electron Technology, *Vol. 26*, pp.129-142. 1993.

[44] Wood, R.A. Micromachined Bolometer Array Achieve Low-cost Imaging, Laser Focus World, *Vol. 29*, pp.101-106. June, 1993.

[45] Wood, R.A. Uncooled Thermal Imaging with Monolithic Silicon Focal Planes, Proc. SPIE, *Vol. 2020*, pp.322-329. 1993.

[46] Jerominek, H., F. Picard, N. R. Swart, M. Renaud, M. Levesque, M. Lehoux, J.-S. Castonguay, M. Pelletier, G. Bilodeau, D. Audet, T. D. Pope and P. Lambert. Micromachined, Uncooled, VO_2-based IR Bolometer Arrays, Proc. SPIE, *Vol. 2746*, pp.60-71. 1996.

[47] Jerominek, H., T. D. Pope, C. Alain, R. Zhang, F. Picard, M. Lehoux, F. Cayer, S. Svard, C. Larouche and C. Grenier, Miniature VO_2-based Bolometric Detectors for High-resolution Uncooled FPAs, Proc. SPIE, *Vol. 4028*, pp. 47-56. 2000.

[48] Tanaka, A., S. Matsumoto, N. Tsukamoto, S. Itoh, K. Chiba, T. Endoh, A. Nakazato, K. Okuyama, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka and N. Teranishi. Infrared Focal Plane Array Incorporationg Silicon IC Process Compatible Bolometer, IEEE Trans. Electron Devices, *Vol.43*, pp.1844-1850. Nov. 1996.

[49] Lambkin, P., B. Lane, I. O'Heifearnan, J. Gillham and R. Watton. Characterization of CMOS Compatible Uncooled Microbolometers, In Proc. IEEE/LEOS Int. Conf. on Optical MEMS, Aug. 2000, Kauai, USA, pp.99-100.

[50] Ju, S-B., Y-J. Yong and S-G. Kim. Design and Fabrication of a High-fill-factor Microbolometer Using Double Sacrificial Layers, Proc. SPIE, *Vol. 3698*, pp.180-189. 1999.

[51] Lee, H.-K., J.-B. Yoon, E. Yoon, S.-B. Ju, Y.-J. Yong, W. Lee and S.-G. Kim. A High Fill−factor Infrared Bolometer Using Micromachined Multilevel Electrothermal Structures, IEEE Trans. Electron. Devices, *Vol.46*, pp.1489–1491. 1999.

[52] Liddiard, K. C., U. Ringh, C. Jansson and O. Reinbold. Progress of Swedish–Australian Research Collaboration on Uncooled Smart IR Sensors, Proc. SPIE, *Vol. 3436*, pp. 578-584, 1998.

[53] Malyarov, V. G., I. A. Khrebtov, Y. V. Kulikov, I. I. Shaganov, V. Y. Zerov, N. A. Feoktistov. Comparative Investigation of Bolometric Properties of Thin-film Structures Based on Vanadium Dioxide and Amorphous Hydrated Silicon, Proc. SPIE, *Vol. 3819*, pp.136-142. June 1999.

[54] Tissot, J.-L., F. Rothan, C. Vedel, M. Vilain and J.-J. Yon. LETI/LIR's Amorphous Silicon Uncooled Microbolometer Development, Proc. SPIE, *Vol.3379*, pp.139-144. 1998.

[55] Ichihara, T., Y. Watabe, Y. Honda and K. Aizawa. A High Performance Amorphous $Si_{1-x}C_x$:H Thermistor Bolometer Based on Micro-machined Structure, In Proc. Int. Conf. on Solid-State Sensors & Actuators (Transducers'97), pp.1253-1256. June 1997.

[56] Mottin, E., J.-L. Martin, J.-L. Ouvried-Buffet, M. Vilain, J.-J. Yon and J.-P. Chatard. 320×240 Microbolometer Uncooled IRFPA, Proc. SPIE, *Vol.4028*, pp.40-46. 2000.

[57] Onokhov, A. P., M. A. Fedorov and N. A. Feoktistov. Photometric Study of Layers of Amorphous Silicon Carbide, Journal of Optical Technology, *Vol. 69* pp.766-768. Oct. 2002.

[58] Rice, J. P., E. N. Grossman and D. A. Rudman. Antenna-coupled High-Tc Air-bridge Microbolometer on Silicon, Appl. Phys. Lett. *Vol.65*, pp.773-775. 1994.

[59] Brasunas, J. C. and B. Lakew. High-Tc Superconductor Bolometer with Record Performance, Appl. Phys. Lett. *Vol.64*, pp.777-779. 1994.

[60] Gray, J., Z. Celik-Butler, D. P. Butler and M. Almasri. Semiconducting YBaCuO as Infrared Detecting Bolometers, Proc. SPIE, *Vol.3436*, pp.555-565. 1998.

[61] Jahanzeb, A., C. M. Travers, Z. Celik-Butler, D. P. Butler, S. G. Tan. A Semiconductor YBaCuO Microbolometer for Room-temperature IR Imaging, IEEE Trans. Electron. Devices, *Vol.44(10)*, pp.1795-1801. 1997.

[62] Almasri, M., D. P. Butler and Z. Celik-Butler. Semiconducting YBCO Bolometers for Uncooled IR Detection, Proc. SPIE, *Vol.4028*, pp.17-26. 2000.

[63] De Moor, P., J. John, S. Sedky and C. Van Hoof. Linear Arrays of Fast Uncooled Poly SiGe Microbolometers for IR Detection, Proc. SPIE, *Vol.4028*, pp.27-35. 2000.

[64] Sedky, S., P. Fiorini, K. Baert, L. Hermans and R. Mertens. Characterization and Optimization of Infrared Poly SiGe Bolometers, IEEE Trans. Electron. Devices, *Vol.46*, pp. 675–682. 1999.

[65] De Moor, P., S. Sedky, D. Sabuncuoglu and C. Van Hoof. Linear Arrays of Uncooled Poly SiGe Microbolometers for IR Detection, Proc. SPIE, *Vol.3876*, pp.256-259. 1999.

[66] Ishikawa, T., M. Ueno, K. Endo, Y. Nakaki, H. Hata, T. Sone, M. Kimata and T. Ozeki. Low-cost 320×240 Uncooled IRFPA Using Conventional Silicon IC Process, Proc. SPIE, *Vol. 3698*, pp.556-564. 1999.

[67] Kim, J. and C. Han. A New Uncooled Thermal Infrared Detector Using Silicon Diode, Sensors & Actuators A, *Vol.89*, pp. 22–27. 2001.

[68] Brasunas, J. C., B. Lakew and R. Fettig. A Comment on Reported Detectivity of a New Uncooled Thermal Infrared Detector, Sensors & Actuators A, *Vol.96*, pp.211–213. 2002.

[69] Tezcan, D. S., F. Koçer and T. Akin. An Uncooled Microbolometer Infrared Detector in Any Standard CMOS Technology, In Proc. 10th Int. Conf. on Solid-State Sensors & Actuators (TRANSDUCERS'99), June, 1999. Sendai, Japan, pp.610-613.

[70] Eminoglu, S., D. S. Tezcan, M. Y. Tanrikulu, T. Akin. Low-cost Uncooled Infrared Detectors in CMOS Process, Sensors & Actuators A, *Vol.109*, pp.102–113. 2003.

[71] Hsieh, C.-C., C.-Y. Wu, F.-W. Jih, and T.-P. Sun. Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems, IEEE Transactions on Circuits and Systems for Video Technology, *Vol.7, No. 4*, pp.594-605 1997.

[72] Balcerak, R. and D. P. Jenkins. Uncooled Infrared Focal Plane Arrays, In Proc. 18th Annual International Conference of the IEEE Engineering in Medical and Biology Society, 1996, Amsterdam, pp.2077-2078.

[73] Nelson, M. D., J. F. Johnson and T. S. Lomheim. General Noise Processes in Hybrid Infrared Focal Plane Arrays, Opt. Eng., *Vol.30, No.11*, pp.1682–1700. 1991.

[74] Agnese, P., C. Buzzi, P. Rey, L. Rodriguez and J.-L. Tissot. New Technological Development for Far-infrared Bolometer Arrays, Proc. SPIE, *Vol.3698*, pp.284-290. 1999.

[75] Kavadias, S., P. De Moor, M. Gastal, N. Hendrikx, F. Wirix and C. A. Van Hoof. Hybrid Long-wavelength IR Sensor Based on a Linear Array of Poly SiGe Uncooled Microbolometers with a CMOS Readout, Proc. SPIE, *Vol. 4169*, pp.348-355. 2001.

[76] Liu, C. C. and C. H. Mastrangelo. A CMOS Uncooled Heat-Balancing Infrared Imager, IEEE J. Solid-State Circuits, *Vol.35(4)*, pp. 527-535. Apr. 2000.

[77] Zerov, V. Y., Y. V. Kulikov, V. G. Malyarov, I. A. Khrebtov, I. I. Shaganov and E. B. Shadrin. Vanadium Oxide Films with Improved Characteristics for IR Microbolometer Devices, Tech. Phys. Lett. *Vol.27*, pp.378-380. 2001.

[78] Infrared Solutions Inc. IR-160 Thermal Imager, 2004, URL: http://www.infraredsolutions.com/html/products/ir160F.shtml. (Last accessed at Feb. 25th, 2004)

[79] Ishikawa, T., M. Ueno, K. Endo, Y. Nakaki, H. Hata, T. Sone and M. Kimata. Low-cost 320×240 Uncooled IRFPA Using Conventional Silicon IC Process, Opto-Electron. Rev. *Vol.7*, pp. 297 –303. 1999.

[80] Radford, W., D. Murphy, M. Ray, S. Propst, A. Kennedy, J. Kojiro, J. Woolaway, K. Sch, R. Coda, G. Lung, E. Moody, D. Gleichman and S. Baur.

320×240 Silicon Microbolometer Uncooled IRFPAs with On-chip Offset Correction, Proc. SPIE, *Vol.2746*, pp.82-92. 1996.

[81] Oda, N., Y. Tanaka, T. Sasaki, A. Ajisawa, A. Kawahara and S. Kurashina. Performance of 320 × 240 Bolometer-type Uncooled Infrared Detector, NEC Research & Developement, *Vol. 44(2)*, pp.170-174. 2003.

[82] Radford, W., D. Murphy, A. Finch, A. Kennedy, J. K. Kojiro, M. Ray, R. Wyles, R. Coda, E. A. Moody and S. T. Baur. Microbolometer Uncooled Infrared Camera with 20-mK NETD, Proc. SPIE. *Vol.3379*, pp22-35, 1998.

[83] Wood, R.A., C. J. Han and P. W. Kruse. Integrated Uncooled Infrared Detector Imaging Arrays, In Technical Digest. IEEE 5th Solid-State Sensor and Actuator Workshop, 22-25 Jun 1992, USA, pp.132 -135.

[84] Radford, W. A., R. Wyles, J. Wyles, J. B. Varesi, M. Ray, D. F. Murphy, A. Kennedy, A. Finch, E. A. Moody, F. Cheung, R. Coda and S. T. Baur. Microbolometer Uncooled Infrared Camera with 20-mK NETD, Proc. SPIE, *Vol. 3436*, pp.636-646. 1998.

[85] Marshall, C. A., N. R. Butler, R. Blackwell, R. Murphy and T. Breen. Uncooled Infrared Sensors with Digital Focal Plane Array, Proc. SPIE, *Vol. 2746*, pp.23-31. 1996.

[86] Radford, W. A., D. Murphy, M. Ray, S. H. Propst, A. Kennedy, Kevin L. Soch, R. Coda, G. Lung, E. A. Moody and D. Gleichman. 320×240 Microbolometer Focal Plane Array for Uncooled Applications, Proc. SPIE, *Vol. 2685*, pp.80-90. 1996.

[87] Meyer, B., R. F. Cannata, A. Stout, A. Gin, P. Taylor, E. Woodbury, J. Deffner and F. Ennerson. Amber's Uncooled Microbolometer LWIR Camera, Proc. SPIE, *Vol.2746*, pp.13-22. 1996.

[88] Murphy, R., M. Kohin, B. S. Backer, N. R. Butler, R. Blackwell and T. Allen. Recent Developments in Uncooled IR Technology, Proc. SPIE, *Vol. 4028*, pp.12-16. 2000.

[89] Murphy, D. F., M. Ray, R. Wyles, J. F. Asbrock, N. A. Lum, J. Wyles,C. Hewitt, A. Kennedy, D. Van Lue, J. S. Anderson, D. Bradley, R. Chin and T. Kostrzewa. High-sensitivity 25-micron Microbolometer FPAs, Proc. SPIE, *Vol. 4721*, pp.99-110. 2002.

[90] Harling, G., R. Zhang, T. Pope, F. Picard and A. Azelman. Non-contacting Temperature Sensing Device, U.S. Patent, No. 6222454. 2001.

[91] Ueno, M., O. Kaneda, T. Ishikawa, K. Yamada, A. Yamada, M. Kimata and M. Nunoshita. Monolithic Uncooled Infrared Image Sensor with 160 by 120 Pixels, Proc. SPIE, *Vol. 2552*, pp.636-643. 1995.

[92] Parrish, W. J., J. T. Woolaway, G. Kincaid, J-L. Heath and J. D. Frank. Low Cost 160×128 Uncooled Infrared Sensor Array, Proc. SPIE, *Vol. 3360*, pp.111-119. 1998.

[93] Jansson, C., U. Ringh, K. C. Liddiard and N. Robinson. FOA/DSTO Uncooled IRFPA Development, Proc. SPIE, *Vol. 3698*, pp.264-275. 1999.

[94] Earth Observatory, NASA, On the Shoulders of Giants, Samuel Langley, URL: http://earthobservatory.nasa.gov/Library/Giants/Langley/langley_2.html. (Last accessed on June 18th, 2004)

[95] X. Gu, G. Karunasiri and G. Chen, Determination of the Thermal Parameters of Microbolometers Using a single Electrical measurement, Applied Physics letters, *Vol.72, No.15*, pp.1881-1883. 1998.

[96] Rieke, F.M., A. E. Lange, J. W. Beeman and E. E. Haller. An AC Bridge Readout for Bolometric Detectors, IEEE Transactions on Nuclear Science, *Vol.36(1)*, pp.946-949. Feb. 1989.

[97] Wilbanks, T. Improved Low Frequency Stability of Bolometric Detectors, IEEE Trans. Nuclear Sci., *Vol. 37(2)*, pp.566-572. 1990.

[98] Gaertner, S., A. Benoit, J. M. Lamarre, M. Giard, J. L. Bret, J. P. Chabaud, F. X. Desert, J. P. Faure, G. Jegoudez, J. Lande, J. Leblanc, J. P. Lepeltier, J. Narbonne, M. Piat, R. Pons, G. Serra and G. Simiand. A New Readout System for Bolometers with Improved Low Frequency Stability, Astronomy & Astrophysics Supplement Series, *Vol.126(1)*, pp.151-160. Nov. 1997.

[99] Yu, T.-H., C.-Y. Wu, P.-Y. Chen, F.-W. Chi, J.-J. Luo, C. D. Chiang and Y.-T. Cheng. A New CMOS Readout Circuit for Uncooled Bolometric Infrared Focal Plane Arrays, In Proc. 2000 IEEE International Symposium on Circuits and Systems(ISCAS 2000), 2000, Geneva, *Vol.2*, pp.493-496.

[100] Kavadias, S., P. De Moor and C. Van Hoof. CMOS Circuit for Readout of Microbolometer Arrays, Electronics Letters, *Vol.37, No.8*, pp.481-482. Apr. 2001.

[101] Chin, Y. L., T. P. Sun, J. C. Chou, Y.-C. Chin, Y. C. Chou, W. Y. Chung and S. K. Hsiung. High-Performance Readout Integrated Circuit for Surface-Micromachined Bolometer Arrays, Proc. SPIE, *Vol. 3899*, pp.124-132.1999.

[102] Chow, K., J. P. Rode, D. H. Seib and J. D. Blackwell. Hybrid Infrared Focal Plane Arrays, IEEE Trans. Electron Devices, *Vol.29, No.1*, pp3-13. 1982.

[103] Doudoumopoulos, N. A., D. J. Gulbransen, J. K. Kojiro, A. E. Cosand, C. G. Whitney, R. Wyles, D. Murphy and S. Black. Infrared Readout Integrated Circuit Technology for Tactical Missile Systems, In Proc. Meeting In Infrared Readout Electronics, Apr. 21-22, 1992, Orlando, USA, pp.201-211.

[104] Wada, H., M. Nagshima, N. Oda, T. Sasaki, A. Kawahara, M. Kanzaki, Y. Tsuruta, T. Mori, S. Matsumoto, T. Shima, M. Hijikawa, N. Tsukamoto and H. Gotoh. Design and Performance of 256×256 Bolometer-type Uncooled Infrared Detector, Proc. SPIE, *Vol.3379*, pp.90-100. 1998.

[105] Brady, J., T. Schimert, D. Ratcliff, R. Gooch, B. Ritchey, P. McCardel, K. Rachels, S. Ropson, M. Wand, M. Weinstein and J. Wynn. Advances in Amorphous Silicon Uncooled IR Systems, Proc. SPIE, *Vol.3698*, pp.161-167. 1999.

[106] Wu, C. Y. and C. C. Hsieh. New Design Techniques for a Complementary Metal-Oxide-Semiconductor Current Readout Integrated-Circuit for Infrared Detector Arrays, Optical Engineering, *Vol.34(1)*, pp.160-168. Jan. 1995.

[107] Hsieh, C.-C., C.-Y. Wu, T.-P. Sun, F.-W. Jih and Y.-T. Cherng. High-Performance CMOS Buffered Gate Modulation Input (BGMI) Readout Circuits for IR FPA, IEEE J. Solid-State Circuits, *Vol.33, No.8*, pp.1188-1198. 1998.

[108] Chin, S. Y. and C. Y. Wu. A 10-bit 125-MHz CMOS Digital-to-analog Converter with Threshold-voltage Compensated Current Sources, IEEE J. Solid-State Circuits, *Vol. 29*, pp.1374–1380. Nov. 1994.

[109] Ringh, U., C. Jansson, C. Svensson and K. Liddiard. CMOS Analog to Digital Conversion for Uncooled Bolometer Infrared Detector Arrays, Proc. SPIE, *Vol.2474*, pp.88-97. May, 1995.

[110] Ringh, U., C. Jansson, C. Svensson and K. Liddiard. CMOS RC-oscillator Technology for Digital Readout from an IR Bolometer Array, In Proc. of the 8th International Conference on Solid-state Sensors and Actuators, and EuroSensors IX, June 25-29, 1995, Sweden, pp.138-141.

[111] Xie, G. Z., L. Deng, T. Wang, J. H. Xu, X. D. Chen, Y. D. Jiang, Z. M. Wu, C. H. Huang and B. C. Yang. Readout Circuit Design for Uncooled Infrared Focal Plane Arrays, In Proc. of IEEE 11th International Symposium on Electrets, Oct. 2002, Australia, pp.349-352.

[112] Marshall, C. A., N. R. Butler, R. Blackwell, R. Murphy and T. Breen. Uncooled Infrared Sensors with Digital Focal Plane Array, Proc. SPIE, *Vol. 2746*, pp.23-31, 1996.

[113] Altman, M. P., B. Backer, M. Kohin, R. Blackwell, N. R. Butler and J. H. Cullen. Lockheed Martin's 640×480 Uncooled Microbolometer Camera, Proc. SPIE, *Vol.3698*, pp.137-143. 1999.

[114] Mandl, W. J. Advances in On-focal-plane A/D with Low-power Optical Readout, Proc. SPIE, *Vol. 3379*, pp.473-482. 1998.

[115] Mandl, W. J., J. J. Kennedy and M. Chu. MOSAD IR Focal Plane per Pixel A/D Development, Proc. SPIE, *Vol. 2745*, pp.90-98. 1996.

[116] Ringh, U., C. Jansson and K. C. Liddiard. Readout Concept Employing a Novel On-chip 16-bit ADC for Smart IR Focal Plane Arrays, Proc. SPIE, *Vol. 2745*, pp.99-110. 1996.

[117] Murphy, D., W. Radford, J. Finch, A. Kennedy, J. Wyles, M. Ray, G. Polchin, N. Hua and C. Peterson. Multi-spectral Uncooled Microbolometer Sensor for Mars 2001 Orbiter THEMIS Instrument, In Proc. 2000 IEEE Aerospace Conference in Big Sky, 2000, Montana, pp.151-163.

[118] Parrish, W. J. and J. T. Woolaway. Methods and Circuirty for Correcting Temperature-induced Errors in Microbolometer Focal Plane Array, U.S. Patent, No. 5756999, 1998.

[119] Parrish, W. J. and J. T. Woolaway. Methods and Circuirty for Correcting Temperature-induced Errors in Microbolometer Focal Plane Array, U.S. Patent, No. 6028309, 2000.

[120] Howard, P. E., J. E. Clarke, A. C. Ionescu, C. C. Li and J. C. Stevens. DRS U6000 640×480 VO_x Uncooled IR Focal Plane, Proc. SPIE, *Vol. 4721*, pp.48-55. 2002.

[121] Parrish, W. J. and J. T. Woolaway. Improvements in Uncooled Systems Using Bias Equalization, Proc. SPIE, *Vol. 3698*, pp.748-755. 1999.

[122] Thodberg, H. H. Review of Bayesian Neural Networks with an Application to Near-infrared Spectroscopy, IEEE Trans. Neural Networks, *Vol.7, No.1*, pp.56–72. 1996.

[123] Panicacci, R., S. Kemeny, L. Matthies, B. Pain and E. R. Fossum. Programmable Multiresolution CMOS Active Pixel Sensor, Proc. SPIE, *Vol. 2654*, pp.72–79. Feb. 1996.

[124] Cannata, R. Introduction to Infrared Focal Plane Electronics, The SPIE Short Course Note, San Diego, CA, July 1993.

[125] Chiu, C. F. and C. Y. Wu. The Design of Rotation-invariant Pattern Recognition Using the Silicon Retina, IEEE J. Solid-State Circuits, *Vol.32*, pp.526–534. Apr. 1997.

[126] Baxter, C. R. and M. A. Massie. On-chip Signal Processing Configurations for Focal Plane Arrays, Proc. SPIE, *Vol. 3698*, pp.726-735. 1999.

[127] Mizaikoff, B. Recent Trends in Mid-infrared Sensing, Proc. SPIE, *Vol.4253*, pp.76-83. 2001.

[128] Tanaka, A., S. Matsumoto, N. Tsukamoto, S. Itoh, K. Chiba, T. Endoh, A. Nakazato, K. Okuyama, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka and N. Teranishi. Influence of Bias-heating on a Titanium Bolometer Infrared Sensor, Proc. SPIE, *Vol. 3061*, pp.198-209. 1997.

[129] Hegel, Jr. R. R., R. A. Wood. Array Uniformity Correction, U.S. Patent, No. 4752694, 1988.

[130] Kaisha, T. K. Non-contacting Thermometer, European Patent, No. EP 0798545A1. 1997.

[131] Gu, X., G. Karunasiri, J. Yu, G. Chen, U. Sridhar and W. J. Zeng. On-chip Compensation of Self-heating Effects in Microbolometer Infrared Detector Arrays, Sensors & Actuators A, *Vol. 69*, pp. 92-96. 1998.

[132] Ramakrishna, M. V. S., G. Karunasiri, P. Neuzil, U. Sridhar and W.J. Zeng. Highly Sensitive Infrared Temperature Sensor Using Self-heating Compensated Microbolometers, Sensors & Actuators: A, *Vol. 79*, pp.122-127. 2000.

[133] Jansson, C., U. Ringh and K. Liddiard. Theoretical Analysis of Pulse Bias Heating of Resistance Bolometer Infrared Detectors and Effectiveness of Bias Compensation, Proc. SPIE, *Vol. 2552*, pp.644-652. 1997.

[134] Auerbach, F. J., G. Meiendres, R. Muller and G. J. E. Scheller. Simulation of the Thermal Behaviour of Thermal Flow Sensors by Equivalent Electrical Circuits, Sensors & Actuators A, *Vol.41-42*, pp.275-278. 1994.

[135] Jakonis, D., C. Svensson and C. Jansson. Readout Architectures for Uncooled IR Detector Arrays, Sensors & Actuators A, *Vol.84*, pp.220-229. 2000.

[136] Xu, Y. P., X. B. Qian and G. Karunasiri. Circuit for microbolometer bias-heating cancellation, Electronics Letters, *Vol. 36*, pp.1993-1994, Nov. 2000.

[137] Gregorian, R. and G. C. Temes. Analog MOS Integrated Circuits for Signal Processing, Chapter 7, John Wiley and Sons, 1986.

[138] Qian, X., Y. P. Xu and G. Karunasiri. Self-heating cancellation circuits for microbolometer, Sensors & Actuators A, *Vol.111*, pp. 196-202. 2004.

[139] Razavi, B. Design of Analog CMOS Integrated Circuits, pp.377-404, McGraw-Hill Higher Education, 2001.

[140] Zeng, W.-J. Infrared Sensors Using Silicon Microstructures, Thesis of Master Engineering, National University of Singapore, 1998.

[141] National Instruments. DAQ 6023E/6024E/6025E User Manual, Dec. 2002.

[142] National Instruments. LabVIEW Function and VI Reference Manual, Jan. 1998.

List of Publications

[1] **Xinbo Qian**, Yong Ping Xu and Gamani Karunasiri. Self-heating cancellation circuits for microbolometer, Sensors & Actuators A, *Vol.111*, pp. 196-202. 2004.

[2] Xu, Y. P., **X. B. Qian** and G. Karunasiri. Circuit for microbolometer bias-heating cancellation, Electronics Letters, *Vol. 36*, pp.1993-1994, Nov. 2000.

[3] **X-B. Qian**., Y. P. Xu and G. Karunasiri. A Prototype ROIC with bias-heating cancellation for microbolometer IR FPA, Technical Digest of 27th international conference on IRMMW, Sept. 2002, San Diego, USA, pp. 259-260.

[4] **X-B. Qian**, Y. P. Xu and G. Karunasiri. A tunable bias heating cancellation circuit for microbolometer readout electronics, Proc. Sensor for Industry Conference (SIcon'01), Nov. 2001, Chicago, USA, pp.264-268.

[5] Yong Ping Xu and **Xinbo Qian**. Current-mode Self-heating Cancellation Circuits for Microbolometers, U.S. Provisional Patent, No. 60498465, Aug. 2003.

Appendix B. LabVIEW Programs

B. 1. Descriptions of sub-VIs used in imaging acquisition programs

: Configures an analog input operation for a specified set of channels.

: Sets the channel and scan clock rates.

: Starts a buffered analog input operation.

: Sets the output logic state of a digital line to high or low on a digital channel.


: Creates an n-dimensional array in which every element is initialized.

: Reads one frame data in the buffer and send the data out as 1-D array.

: Constructs the 2-D image array from the input 1-D data.


: Calculates the array size.


: Changes the dimension of an array, such as changes a 2-D array to 1-D array.


: Displays a dialog box that contains a message and a single button.

: Writes data string of a 2D or 1D array to a spreadsheet file.

: Reads a specified number of lines or rows from a spreadsheet file.

: Clears the analog input task.

: Clears the digital I/O task.

: Generates a color table to set the color of the front panel object.

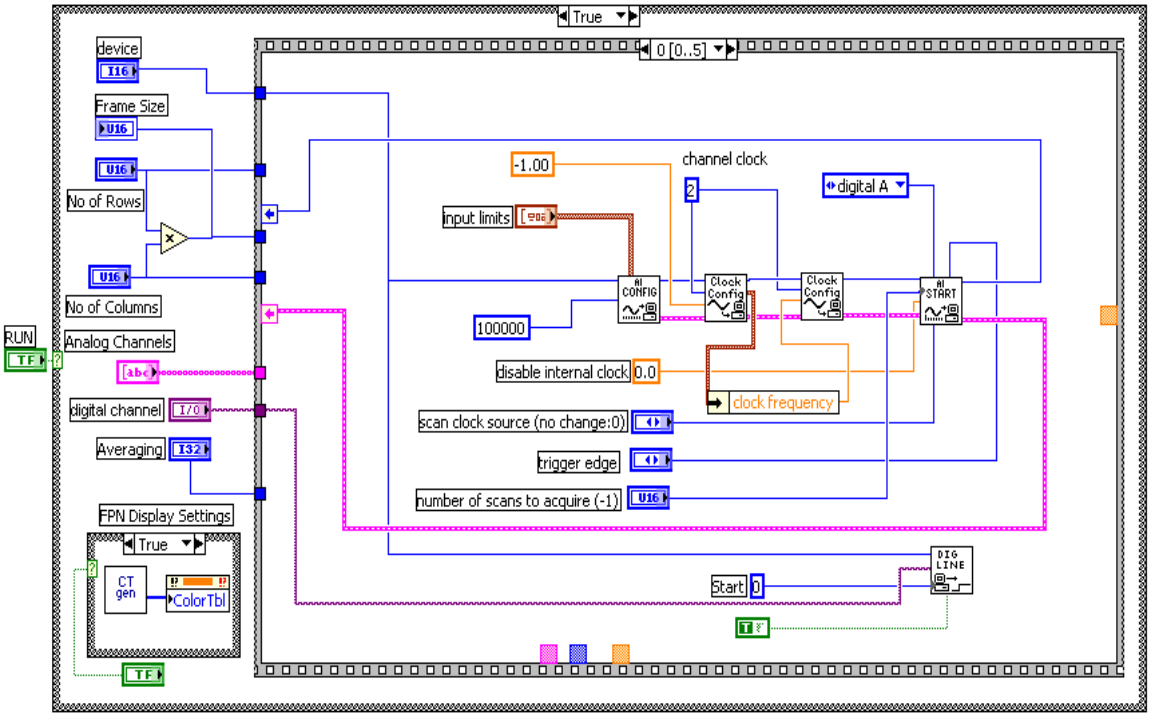

: Computes the mean, standard deviation, and variance of input data sequence.


: Searches for the first maximum and minimum values in numeric array.

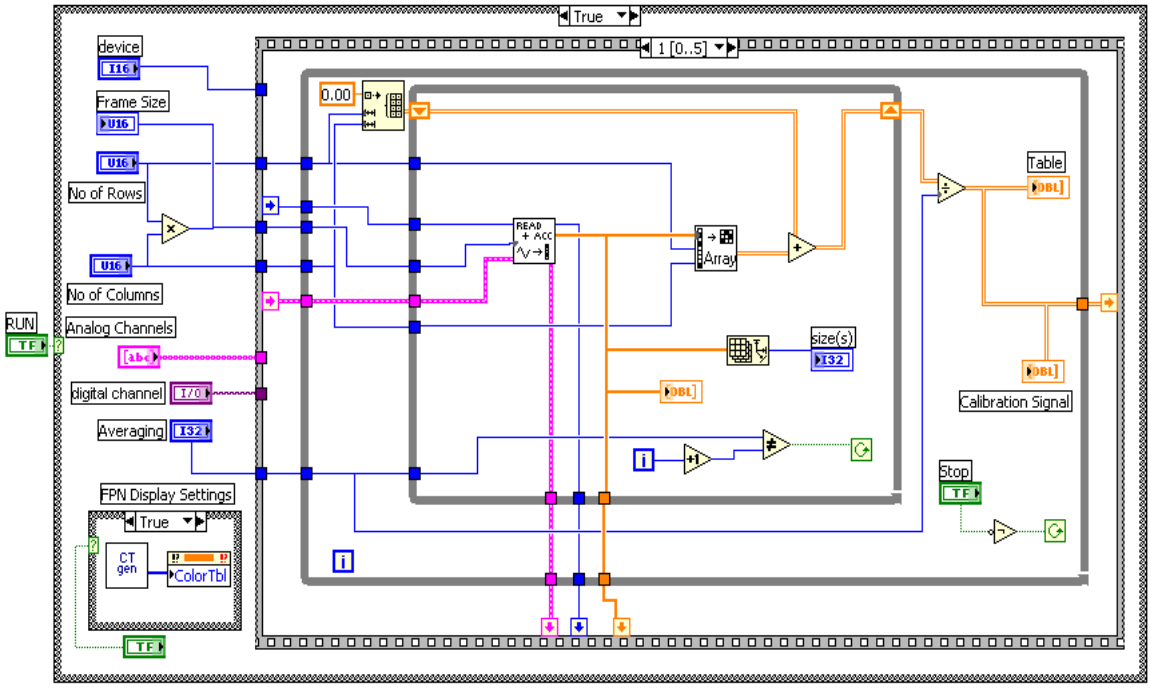
: Finds the discrete histogram of the input data sequence.

B.2. LabIVEW program for calibration operation

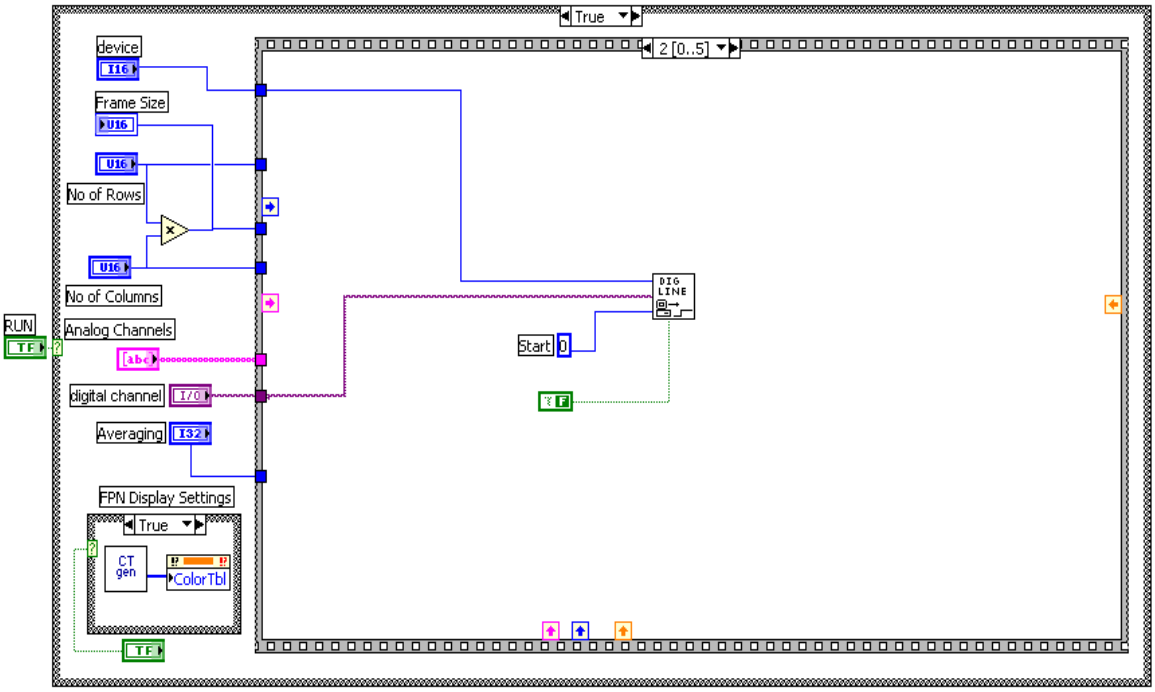
Calibration operation program (Frame 0)



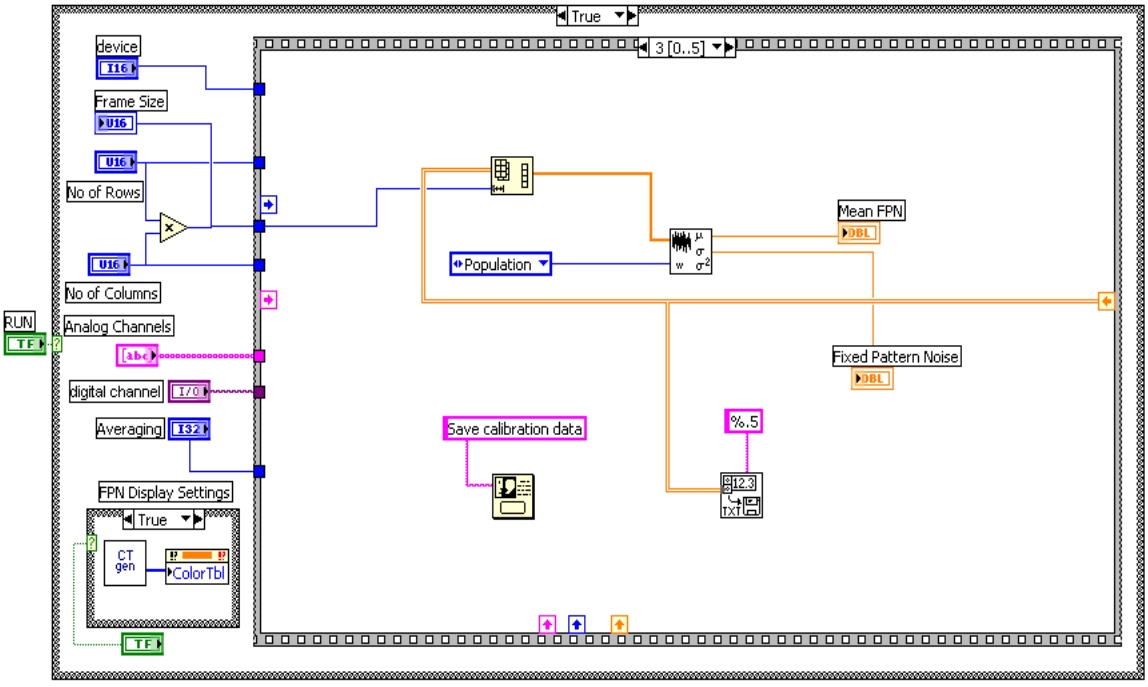
Calibration operation program (Frame 1)



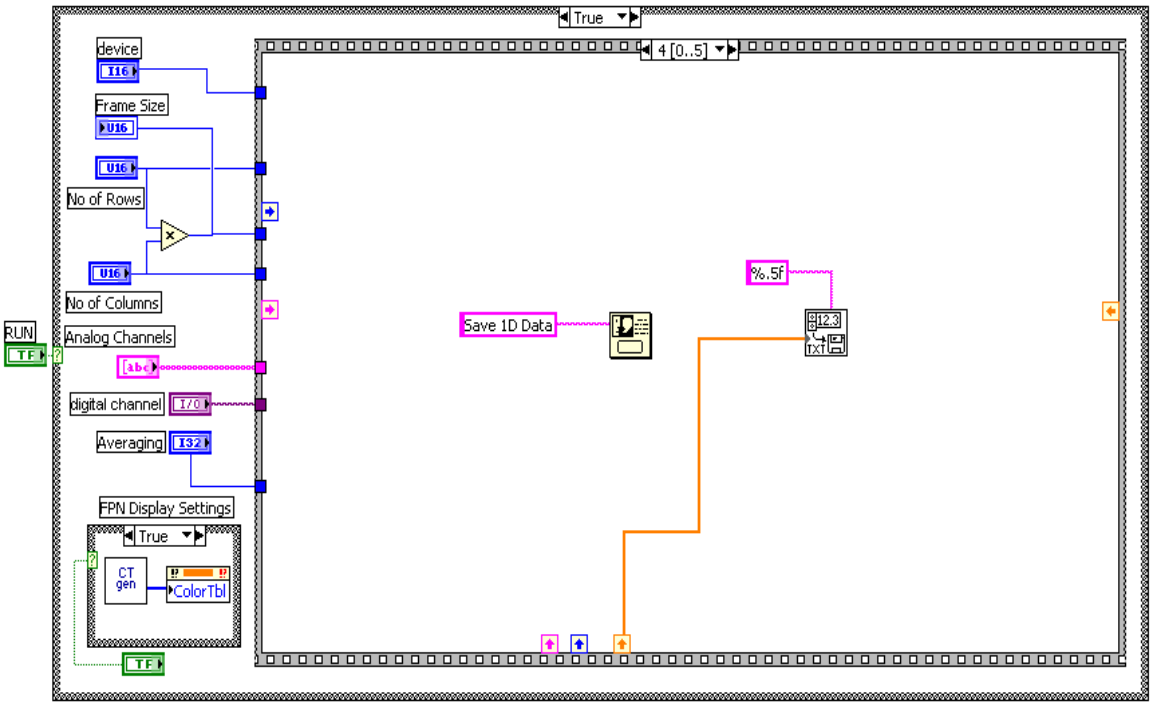
Calibration operation program (Frame 2)



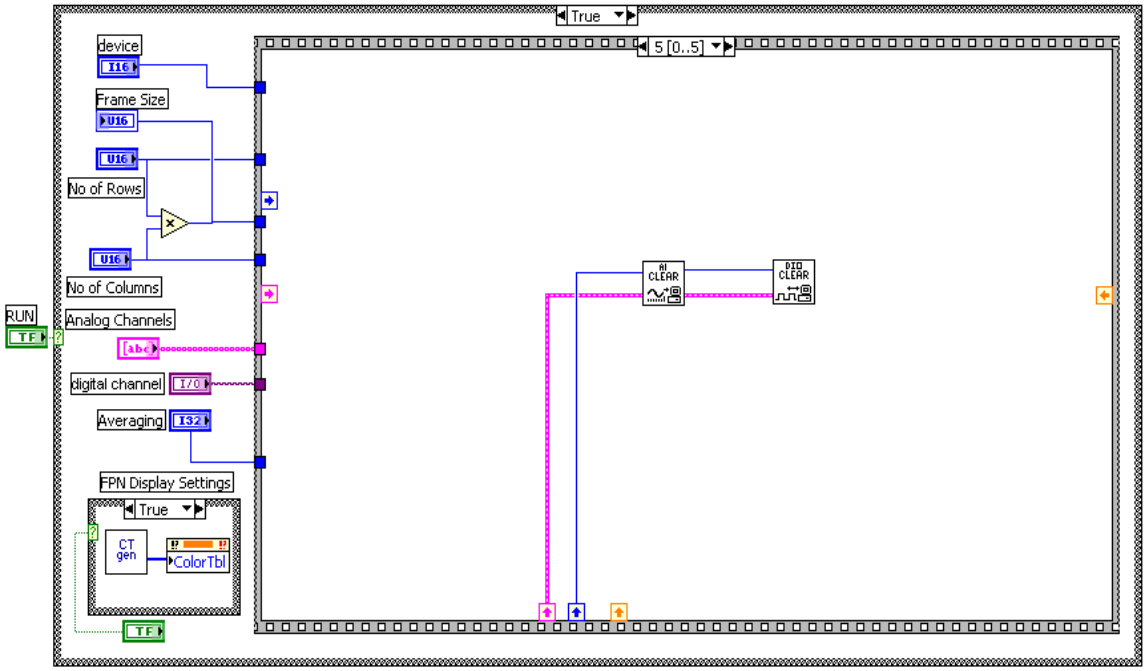
Calibration operation program (Frame 3)



Calibration operation program (Frame 4)

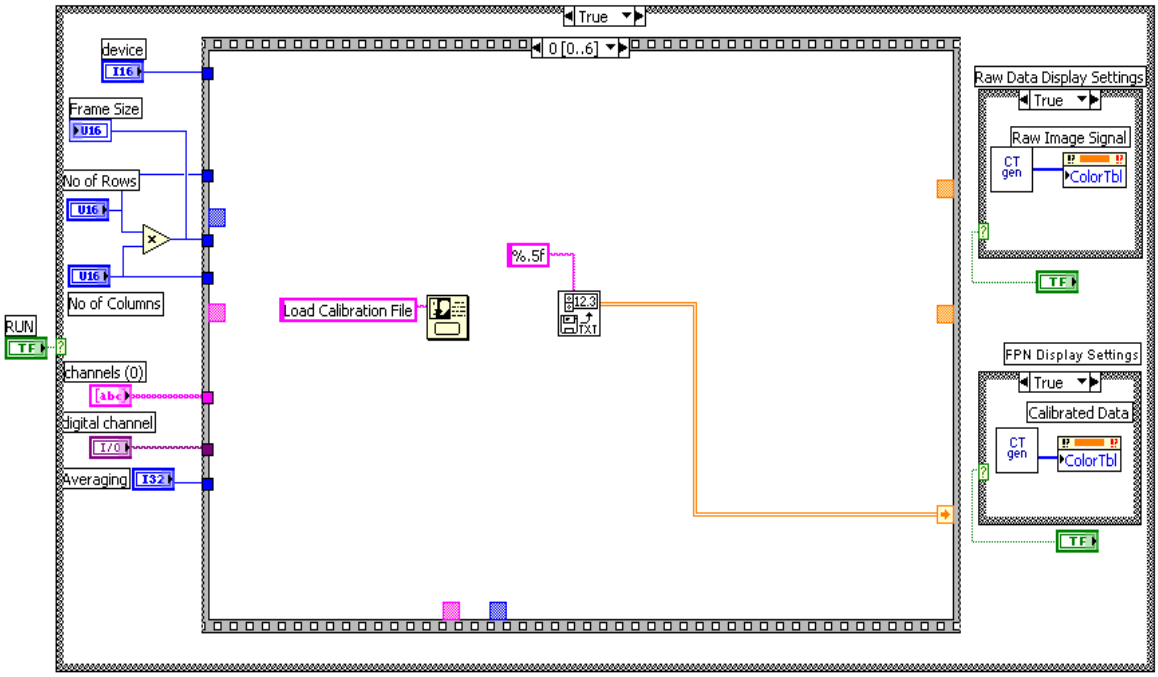


Calibration operation program (Frame 5)

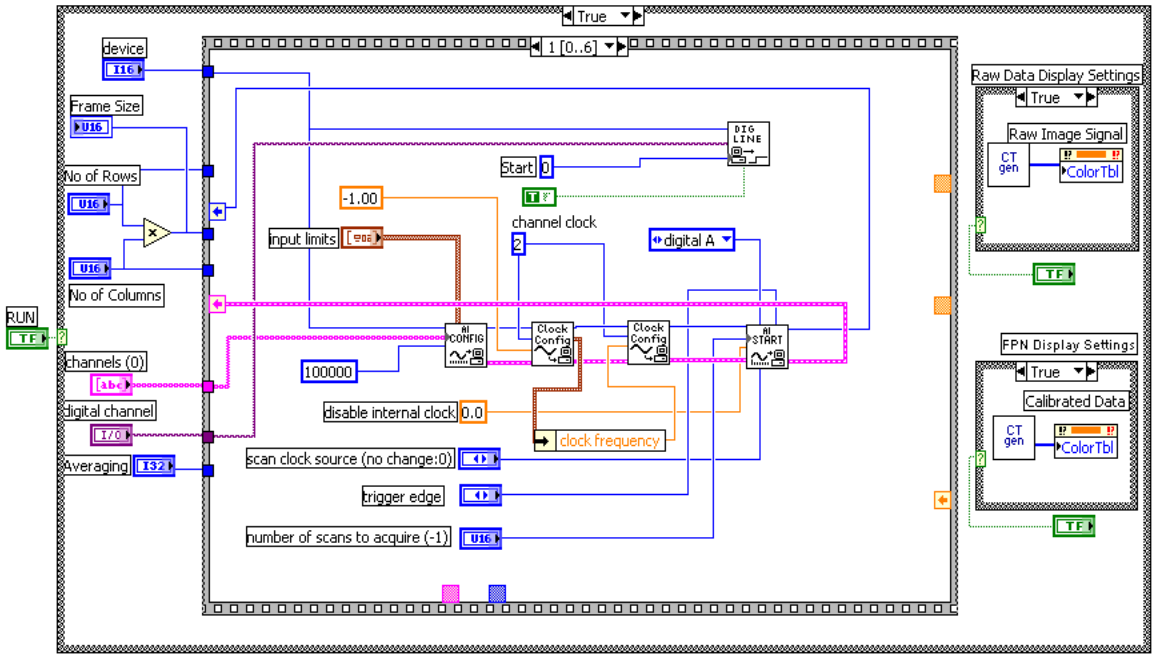


B.3. LabIVEW program for real-time imaging operation (Frame 0)

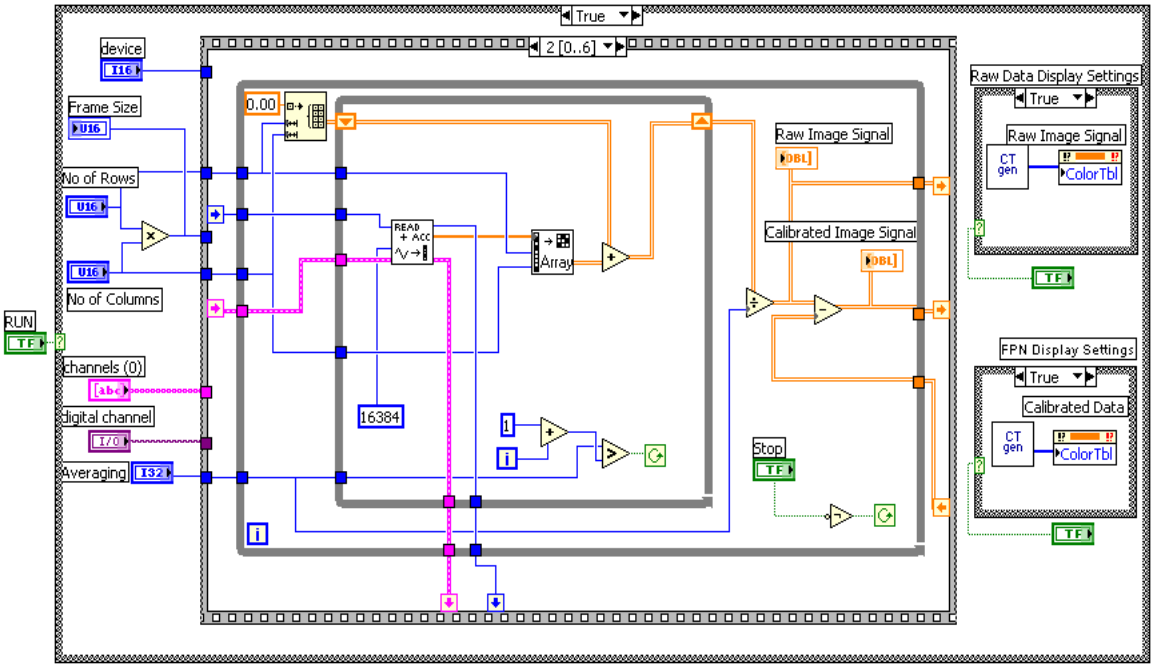
Real-time imaging operation program (Frame 1)



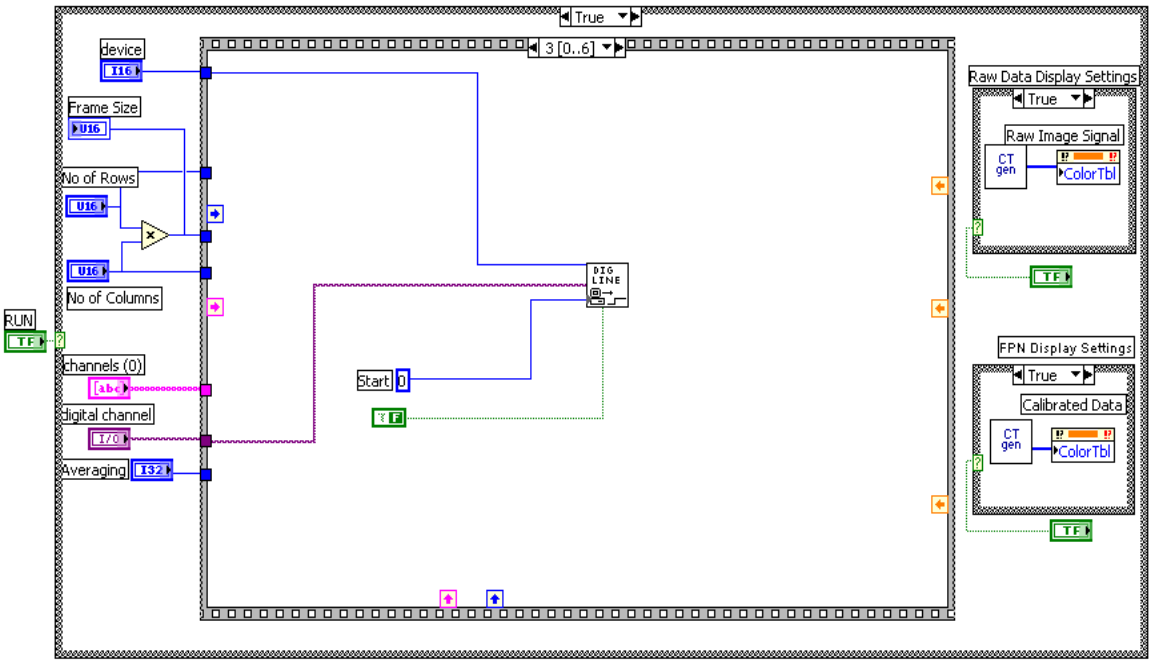
Real-time imaging operation program (Frame 1)



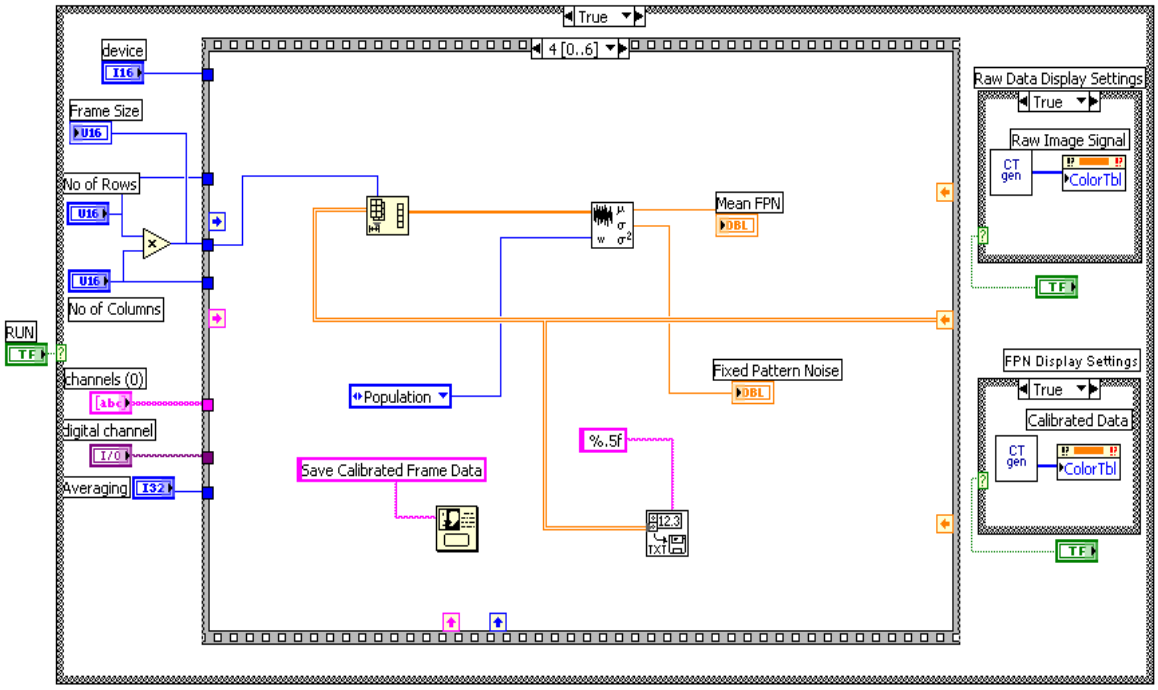
Real-time imaging operation program (Frame 2)



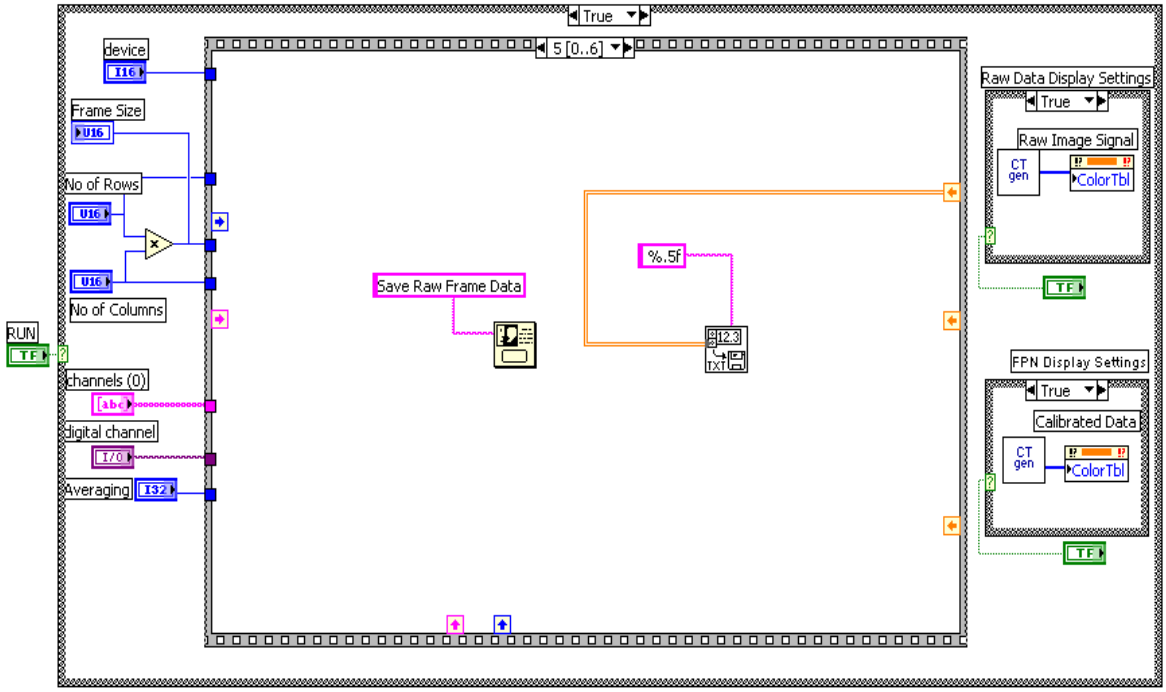
Real-time imaging operation program (Frame 3)



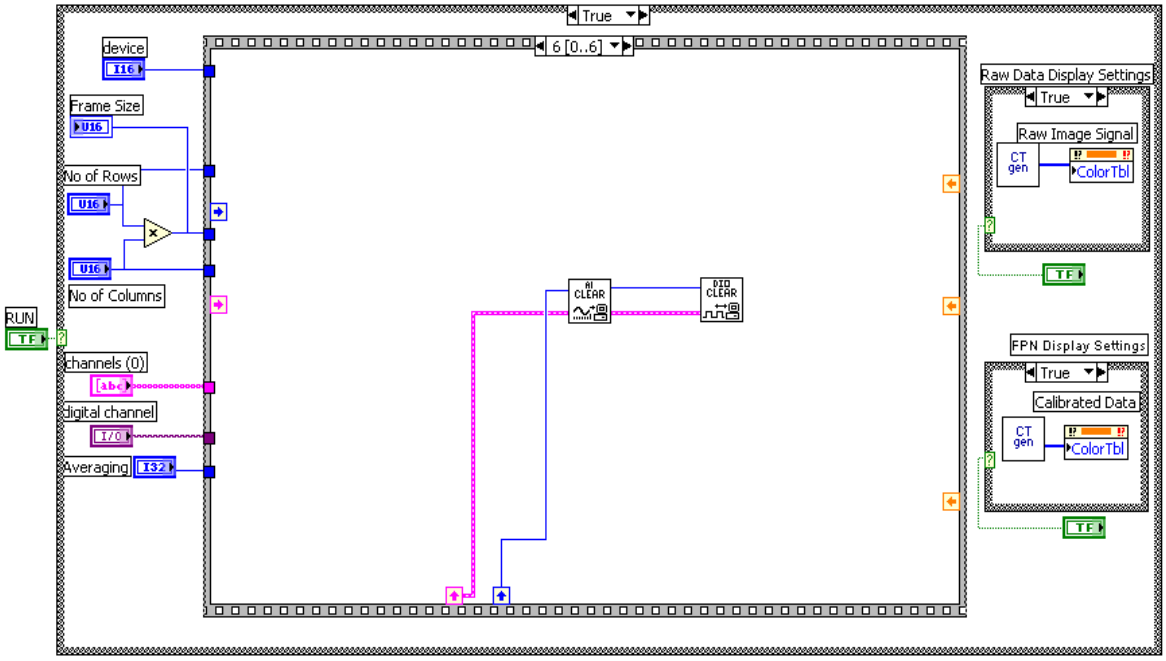
Real-time imaging operation program (Frame 4)



Real-time imaging operation program (Frame 5)



Real-time imaging operation program (Frame 6)



B.4. LabIVEW program for noise measurements