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Temperature Regulation and In-Situ Fault Detection of Wafer Warpage

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2004

Temperature Regulation and In-Situ Fault Detection of Wafer Warpage

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Summary

Wafer warpage is common in microelectronics processing. There are two major stress factors that account for wafer warpage or bow during its processing: (1) Stress from mechanical processing of the wafer surface; (2) Stress from heating. Warped wafers can affect device performance, reliability and line width control in various processing steps. In the exposure step a warped wafer results in a non-uniform gap between the wafer and mask for a contact aligner and different depth-of-focus at different parts of the wafer for a projection exposure system. Warpage may cause the patterning out of design thus makes the electronic elements fail in test.

There are quite a few ways used to test the wafer warpage in industry or laboratory. Current techniques of measuring wafer warpage are mainly based on optical analysis for example Shadow Moiré and pneumatic-electro-mechanical technique. These techniques are off-line methods where the wafer has to be removed from the processing equipment and placed in the metrology tool, which increase processing steps, time and cost. The author proposes in this thesis an in-situ fault detection technique for wafer warpage in lithography. In soft baking process of lithography the measurement of bakeplate temperature are running continuously, and physical analysis shows that the warpage of wafer determines the curve of temperature. By constantly monitoring the baking temperature it is able to detect the defective wafer quickly, but with minimal computational power and few false indications.

This thesis thoroughly analyzes the soft baking process of lithography and builds an accurate model based on the heat transfer equations. A Feedforward control strategy is applied to achieve a steady baking temperature. The optimal Feedforward control signal is found out by Linear programming method. In implementation the signal is truncated with boundaries of input. Simulation shows that the use of advanced process control resulted in a very small temperature disturbance given a flat wafer. With a warped wafer the baking temperature experiences a deviation from the set point. The value of deviation is an observable index of the warpage. The effectiveness of the Feedforward signal is demonstrated by experiment. Simulation and experiment also show that the baking temperature is sensitive to the wafer warpage, which makes the fault detection method feasible. The more the wafer warps, the more the temperature fluctuates. In industry a standard approach to fault detection is to define a threshold based on manufacturing requirements and any violation of the threshold is considered a fault. The experiment is repeated for 9 times and the comparison of results has proved the repeatability of the warpage detection method.

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Nomenclature

A_P surface area of the side of bake plate

A_w Surface area of wafer

c_w Specific heat capacity of wafer

C_P Total heat capacity of bake plate

C_w Total hest capacity of wafer

h Natural convection coefficient

K_a Thermal conductivity of air

K_p Gain constant of PID

l_a Nominal air-gap thickness

l_{pp} Bakeplate proximity pin length

m_w Mass of wafer

$p(t)$ Heater power

R_a Heat transfer resistance of air gap

R_p Heat transfer resistance of bakeplate to the ambient atmosphere

R_w Heat transfer resistance of wafer to the ambient atmosphere

T_i Integrative constant of PID

T_p Bakeplate temperature above the ambient

T_{plate} Bakeplate temperature (K)

T_w Wafer temperature above the ambient

T_∞ , $T_{ambient}$ ambient temperature

λ_{wp} the measure of warpage (average warpage)

ε_w Emittance of wafer

ε_p Emittance of bakeplate

σ Stefan-Boltzmann constant

θ The temperature variance from steady state in baking

U The power variance from steady state

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Chapter 1 Introduction

1.1 Motivation

Wafer warpage is common in microelectronics processing. Over-warped wafers are not acceptable in industry because they cause the final semiconductor products to have serious defects.

Warpage can affect device performance, reliability and linewidth or Critical Dimension (CD) control in various lithographic patterning steps. Figure 1.2 shows a typical lithography sequence [19]. Warpage is one challenge that marking system must cope with. Figure 1.1 illustrates the process of marking. The marking system is the core of lithography equipments. It is in the marking system that the pattern is copied from mask to the wafer surface precisely.

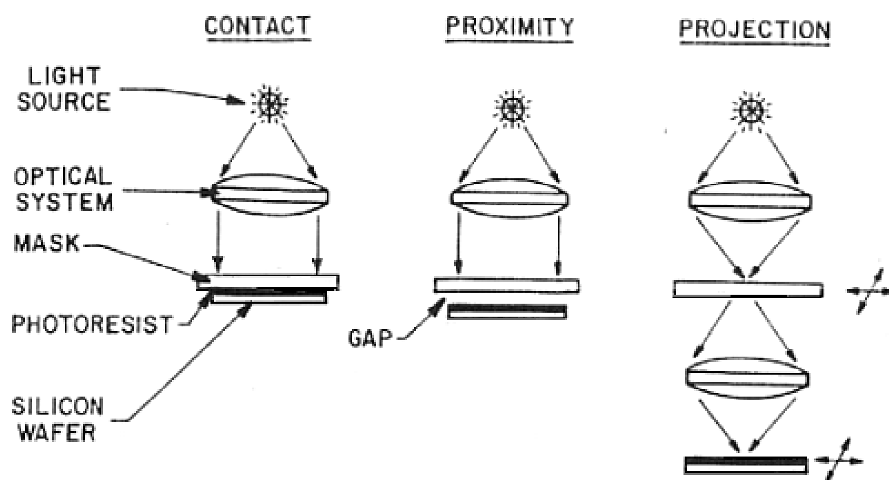


Figure 1.1 Marking Process

Typically, as silicon wafers get thinner and larger, gravity pulls down the center of the silicon wafer. This is a serious problem for laser marking. In the exposure step a warped wafer results in a non-uniform gap between wafer and

mask for a contact aligner and different depth-of-focus at different parts of the wafer for a projection exposure system. The significance of having a wafer of minimal warpage is that it makes possible the reduction of the depth-of-focus to achieve a higher pattern resolution [19]. Warpage may cause the patterning out of design thus makes the electronic elements fail in test. Because of wafer warpage, wafer cracking may happen during the photo-lithography process using the conventional contact-type mask aligner [15].

Warped wafers also affect the various baking steps in the lithography sequence [24] shown in Figure 1.2. Warpage can result in a non-uniform wafer temperature distribution across the wafer. Simulation results show that warpage of less than 50μm can lead to a temperature variation of 1ºC at temperatures between 70ºC and 150ºC.

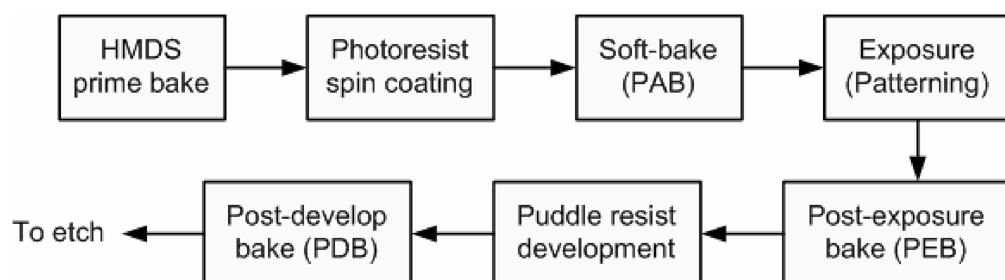


Figure 1.2 Typical steps in the lithography sequence.

Wafer warpage can lead to a high level of stress and generation of defects in dielectric films, degrading device performance of the final IC products.

Warped wafers also result in different processing conditions in other processing steps such as Rapid Thermal Processing [19]. Warpage becomes more problematic for larger wafers and the maximum allowable warpage for a 300 mm wafer is 100 μm from centre to edge [11].

Wafer bow and warp have been shown to generate downstream problems to photolithography, Chemical Mechanical Polishing and backgrinding [13]. Even modest wafer warpage can cause substantial spatial variability in the temperature profile during transients, which will lead to strain accumulation and crack or de-lamination during dicing and the low temperature storage process. Warpage may also impact the repeatability of the production. Chucking problems may be due to wafer warpage. Wafer transport is affected by sag compounded by wafer warpage from previous processes.

In the process of semiconductor manufacturing, most of the stages experience the temperature changing, and some even have the rapid heating and cooling within seconds which result in the temperature difference above several hundred degrees Celsius [5]. The laminated structure of wafer always leads to different physical properties of the substrate and the sandwich film; as a result warpage may be induced by sharp temperature variance. The warpage is increased by the effect of gravity during the loading of the wafer into the wafer boat. The main cause is typically the lack of support provided to the thin wafer where the side wing width is only 3 mm. As a result, a warped wafer cannot be placed into a conventional wafer boat.

There are a few stress factors that account for wafer warpage or bow during its processing [6]:

(1) Stress from mechanical processing of the wafer surface e.g. Chemical Mechanical Polishing or back grinding causes it to bend or fracture. Wafer warps sometimes due to the grinding surface damage. Wafer warpage up to a large amount can occur during wafer thinning. Stress induced during slicing and lapping

of wafers may also lead to warpage.

(2) Stress from heating e.g. Rapid Thermal Processing causes the wafer to bend. The mismatch in the coefficient of thermal expansion among different layers on the silicon substrate induces some distortion on the wafer level. In oxidation process wafers are typically inserted and removed from the tube furnace during the soak period at a given rate (for example, 12" per min). Exceeding this rate can cause the wafer to warp. Wafers are put in a furnace and heated to around 1200°C and various pure gasses are pumped into the furnace. Usually the furnace is started at around half that value and rapidly increased over time because otherwise the thermal gradient across the width of the wafer may vary too sharply, causing it to warp or even break. In the doping process, the furnace temperature profile is of particular importance. A very steep temperature gradient normally occurs between the front of the flat zone and the mouth of the diffusion tube. If the carrier is rapidly pushed or pulled through this portion of the diffusion tube, a large temperature gradient will form across the radius of the sources. If this gradient is too high, the stresses it develops can warp the silicon wafer to a large amount or even break the wafer or the dopant source.

Due to the problems that wafer warpage may induce, wafers that warp above the tolerable limitation should be identified as early as possible. They should be rejected without further processing so as to reduce the cost and increase the yield. Wafer level packaging, which saves a great amount of time in the manufacturing and reduces cost per chip by batch process, has stringent requirements regarding the flatness of the wafer as well as other new technologies like the System On Package. Some new complex device structures such as those in CMP (chemical

mechanical planarization) place stringent requirements on the starting wafer flatness (the front surface of the patterned wafer must be made flat to within tenths of a micron).

There are quite a few ways used to test the wafer warpage in industry or laboratory.

Current techniques of measuring wafer warpage are mainly based on optical analysis. Different measurement equipments are developed by a number of organizations. The techniques include pneumatic-electro-mechanical technique [4], capacitive measurement probe [18] and Shadow Moiré technique [26].

Charles *et al* [1] developed a technique using a broadband white-light source to measure the warpage in microelectronics. The technique forms an interference fringe pattern when observed through Charge Coupling Device camera. The fringe pattern is captured using a videocassette recorder and a digital frame grabber for storage, display and conversion into 3-D color plots.

Tools based on capacitance gauges are widely used today for wafer geometry measurements. Capacitive Sensors are non-contact sensors that use an electric field to measure or gauge geometry of a conductive target with wide bandwidth, accuracy and resolution to nanometers or micro inches. It's also able to measure nonconductors in many applications. A Capacitive Sensor is a combination of a probe and driver electronics.

Currently, the most commonly used method of wafer measurement is the Shadow Moiré technique, which employs a pair of capacitive measuring probes which sample points on the surface of a rotating wafer to obtain the contours of

surface. Many sampling points on the surface are needed for more accurate measurements thus more time for the inspection are required. An alternative for full-field, whole-wafer measurement was developed using a laser light source and the modified Shadow Moiré technique [26]. This method is faster, especially when dealing with wafers with diameter larger than 200 mm (8").

All of the above are off-line methods where the wafer has to be removed from the processing equipment and placed in the metrology tool resulting in increased processing steps, time and cost. For example, the Shadow Moiré components require rearrangement of the process equipment if they are integrated on line. Otherwise the measurement have to be done off line. Both the light source and camera increase the initial expense and maintenance cost as well.

In this thesis, the author proposes an in-situ fault detection technique for wafer warpage using available temperature measurements. Detection of process faults in the shortest time possible is critical to minimize defective wafers and improve product yields for semiconductor manufacturing. There are two traditional ways to detect these faults. One method involves waiting for problems to arise with the end-of-the-line product. This method is slow and tedious and can lead to substantial losses in product. Alternatively, one can monitor wafer-state data collected after each manufacturing process step and look for faulty processing. For example the warpage can be measured by a stress gauge after Reactive Ion Etch process or may be detected in the alignment step when wafer contacted the camera. More recently there has been a move towards fault detection directly on line through monitoring of the process-state data. To enable the in-situ fault detection the system must have the ability to collect a large amount of data in real-

time, which means the system of processing needs to be enhanced to support in-situ performance monitoring. An in-situ system must constantly monitor for faults and any unexpected state changes must be detected very quickly, but with minimal computational power and few false indications. Fortunately, in soft baking process of lithography the measurement of bakeplate temperature is running continuously. At the same time the temperature data is well filtered and processed, hence it is both available and reliable. The more important thing is that the baking temperature varies directly with the warpage of a wafer, with either convex or concave areas on its surface. One important task of this thesis is to find the relationship between the measured temperature and the warpage.

1.2 Background and Contribution

The relationship of bakeplate temperature and warpage is determined by the thermal physics of baking process. There are a number of low temperature thermal processing steps in the lithography sequence [21] as shown in Figure 1.2.

Thermal processing of semiconductor wafers (after coating) is commonly performed by placement of the substrate on a heated bakeplate for a given period of time. The heated bakeplate is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bakeplate near the surface. The wafers are usually placed on proximity pins of the order of 100 to 200 μm high to create an air-gap so that the bakeplate will not contaminate the wafers. As wafers can warp up to 100 μm from centre to edge, the percentage change in the air-gap between the wafer and bakeplate can be substantial (see Figure 2.1) resulting in a non-insignificant variation in the bakeplate temperature. When a wafer at room temperature is placed on the bakeplate, the temperature of the bakeplate drops at first but recovers gradually because of closed-loop control [10] (discussed in the next chapter).

Different air-gap sizes cause different magnitudes of temperature disturbances hence warpage can be detected from the temperature disturbances. Since bakeplate temperature measurements are already available, the proposed method can be implemented without increasing system complexity and equipment cost.

However, in [10], the temperature disturbance used as the signal for warpage computation had a magnitude of more than a degree Celsius. This may not be implementable in practice as the temperature for some baking steps such as the

post-exposure bake has to be controlled to be within ±0.1°C [22]. For commercially available deep ultra violet resist, representative post-exposure bake latitude for Critical Dimension variation is about 5nm/ºC [22]. A number of recent investigations also showed the importance of proper bakeplate operation on line width or CD control [24], [7]–[9]. According to the International Technology Roadmap for Semiconductors [12], the post-exposure bake resist sensitivity to temperature will be more stringent for each new lithography generation. By the year 2010, the post exposure bake resist sensitivity is expected to be 1 nm/ºC, making temperature control even more critical. The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational control and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence.

In this thesis, advanced process control such as Feed Forward control [8] is applied to compensate the temperature drop and reduce it to a tenth of a degree Celsius. The new in-situ method to detect over-warped wafer in microlithography is also simulated and verified by experiments within this thesis.

By investigation of the physical process, a first principle thermal model is built to identify the relationship between wafer warpage and the variance of baking temperature. This relationship is compared with the result of experiments. From the thermal model an optimal Feed Forward control signal is also found to eliminate the disturbance. In implementation this signal is truncated by the input boundary of the heater.

Small temperature disturbance makes the method suitable for industrial implementation. Experiments show that the Feed Forward control method improved the uniformity of temperature by 10 times from that with only feedback control. In industrial practice there is always a limitation on the input power to the baking system, therefore the Feed Forward signal is confined within a high and a low boundary. The optimal computation method is applied to minimize the settling time and the baking temperature deviation.

It is demonstrated that warpage can still be detected and more importantly, there is no loss in sensitivity in the detection algorithm even though the temperature disturbance that provided the signal for detecting warpage is small. Since bakeplate temperature measurements are already available, the proposed method can be implemented without increasing system complexity and equipment cost.

Simulation and experiments show that the relationship between warpage and baking temperature is explicit and stable. The extreme value of temperature gives a noticeable indication to amount of warpage. For a variance of warpage about 50μm the extreme temperature may have a difference more than 0.2ºC.

Compared with the warpage detection methods like Shadow Moiré mentioned in section 1.1, the newly proposed method is much easier to implement but cost much less. The work required to do is building a thermal model for the soft-bake system. Some experiments need to be done so as to set the temperature threshold for the process. Although the precise warpage amount cannot be predicted, warpage fault wafers are able to be identified quickly by observation of the baking temperature curve.

1.3 Scope

Chapter Two describes the mathematical modeling of the soft-baking system used in this project. The model in a specific industrial practice may be built similarly.

Chapter Three explains the temperature control method. The optimal predictive control algorithm is provided and the control signal based on the thermal model in Chapter two is obtained.

Chapter Four describes the experimental system and the results. The respective data are analyzed by table and graph to demonstrate the feasibility the method.

1.4 Conclusion

Warpage is a common problem in wafer-fab processes. Over-warped wafers should be found out as early as possible in industry because they bring serious defects to the final semiconductor products and cause some difficulties to the following process steps. There are different ways in semiconductor industries to measure the wafer warpage, in which the Shadow Moiré technique is widely applied. However, most of them are difficult to implement due to the extra process or equipment demand. An easy feasible way is proposed to detect over-warped wafers in this thesis.

Chapter 2 Thermal model

2.1 Introduction

In this Chapter, we present the model for the baking process which can be used to detect wafer warpage. For our purpose, a one-dimensional analysis will be used to characterize the dynamics of heat transfer for a silicon wafer at room temperature placed on a bakeplate maintained at a steady-state temperature. A similar model was derived in [10].

However, radiation was neglected in [10]. In this thesis heat transfer through radiation is considered to give a more accurate model.

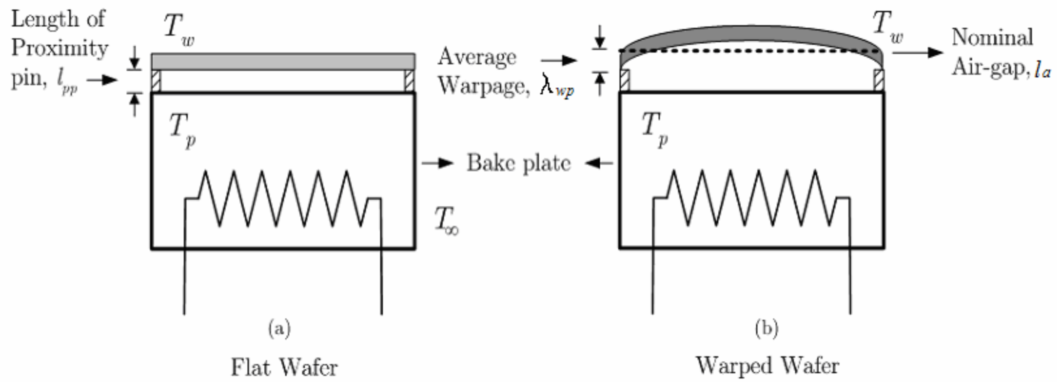


Figure 2.1 Schematic Diagram of Baking Process

The heat transfer of radiation is in the same order of magnitude as that of natural convection. In this thesis the characteristic temperature (at which the thermal properties of materials are determined) is

$$\frac{T_{Plate} + T_{ambient}}{2} = \frac{90 + 273 + 28 + 273}{2} = 332\ K = 59\ ^\circ C$$

At this temperature [16], the heat loss by natural convection may then be calculated:

$$Q_{convection} = h\ (T_{plate} - T_{ambient})$$

$$= (N_u A \frac{\lambda}{l})(T_{plate} - T_{ambient})$$

$$= CA(R_a)^{0.25} \frac{\lambda}{l} (T_{plate} - T_{ambient})$$

$$\approx 0.59A \times \left(9.8 \times \frac{1}{273+28} \times (90-28) \times \frac{0.2^3}{(16 \times 10^{-6})^2} \times 0.7 \right)^{0.25} \times \frac{0.0283}{0.15} \times (90-28)$$

$$= 562A$$

h is the heat transfer coefficient; l is the characteristic length; A is the surface area; R_a is the Rayleigh number; λ is heat conductivity of air; N_u is the Nusselt number; C is a constant.

The heat loss by radiation is:

$$Q_{radiation} = \varepsilon_p \sigma [(T_{plate})^4 - (T_{ambient})^4] A$$
$$= 0.7 \times 5.67 \times 10^{-8} \times [(90 + 273)^4 - (28 + 273)^4] A$$
$$= 363\ A$$

σ is the black body radiation constant; ε_p is the emissivity of steel plate.

It is found that the heat loss through radiation of the plate is not negligible. Thus in the modeling radiation term is kept to represent the baking process more accurately.

2.2 Modeling

A schematic of the system under consideration is shown in Figure 2.1 where 2.1(a) shows the baking of a flat wafer and 2.1(b), the baking of a warped wafer. The system consists of 3 basic sections: the bakeplate, the air-gap and the silicon wafer. The wafer and the bakeplate were assumed to have the same diameter. The temperature distribution within each section is assumed at any instant to be sufficiently uniform such that it can be considered to be a function of time only i.e. "lumped" model approach. Radiative heat transfer between the bakeplate and ambient, and wafer and ambient are considered. Heat transfer between the bakeplate and wafer due to radiation can be neglected safely because the channel is less than 0.3mm, while the size of wafer is 200mm. The heat of radiation is mostly reflected so its effect can be ignored.

The energy variance of wafer, $m_w c_w \dot{T}_w$, should be equal to the difference between the heat it gets from plate ($\frac{k_a A_w}{l_a}(T_p - T_w)$), and the heat it dissipates through convection ($hA_w T_w$) and radiation ($\varepsilon_w A_w \sigma((T_w + T_\infty)^4 - T_\infty^{\ 4})$). The plate gains energy from heater (*p(t)*) and losses heat to wafer ($\frac{k_a A_w}{l_a}(T_p - T_w)$) and ambient (through convection: $hA_p T_p$, through radiation: $\varepsilon_p A_p \sigma((T_p + T_\infty)^4 - T_\infty^{\ 4})$). The energy balance of the wafer and bakeplate are given by:

$$m_w c_w \dot{T}_w = \frac{k_a A_w}{l_a}(T_p - T_w) - hA_w T_w - \varepsilon_w A_w \sigma\left((T_w + T_\infty)^4 - T_\infty^{\ 4}\right) \tag{2.1}$$

$$C_p \dot{T}_p = p(t) - \frac{k_a A_w}{l_a}(T_p - T_w) - hA_p T_p - \varepsilon_p A_p \sigma\left((T_p + T_\infty)^4 - T_\infty^{\ 4}\right) \tag{2.2}$$

Where for the 200 mm wafer and the given bakeplate:

mass of wafer: $m_w = 55.3\,\mathrm{g}$

specific heat capacity of wafer: $c_w = 0.73\,\mathrm{KJ/KgK}$

total heat capacity of bake plate: $C_P = 750\,\mathrm{J/K}$

thermal conductivity of air: $K_a = 0.012\,\mathrm{W/mK}$

natural convection coefficient: $h = 10\,\mathrm{W/m^2K}$

emittance of wafer: $\varepsilon_w = 0.67$

emittance of bakeplate: $\varepsilon_p = 0.65$

Stefan-Boltzmann constant: $\sigma = 5.67 \times 10^{-8}\ \mathrm{W/(m^2K^4)}$

surface area of wafer: $A_w = 0.0314\,\mathrm{m^2}$

surface area of the side of bake plate: $A_P = 0.11\,\mathrm{m^2}$

wafer temperature above the ambient: T_w

bakeplate temperature above the ambient: T_p

ambient temperature: T_∞

heater power: $p(t)$ Watt

nominal air-gap thickness: l_a micron

bakeplate proximity pin length: l_{pp} micron

Most thermo physical properties are temperature dependent. However, for the temperature range of interest from 15ºC to 150ºC, it is reasonable to assume that they remain fairly constant as given in the above. They can be obtained from handbooks [20], [16].

Figure 2.1 shows the nominal air-gap, l_a. Notice that for a flat wafer the nominal air-gap, l_a, is equal to the height of the bakeplate proximity pins, l_{pp}. We next define λ_{wp} as a measure of the degree of warpage where

$$\lambda_{wp} = l_a - l_{pp}$$

The T^4 dependence of radiant heat transfer complicates calculations. Equations (2.1) and (2.2) can be linearized as follows [16].

$$m_w c_w \dot{T}_w = \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - hA_w T_w - \varepsilon_w A_w \sigma\left(\left(T_w + T_\infty\right)^2 + T_\infty^{\ 2}\right)\left(T_w + 2T_\infty\right)T_w$$

$$\approx \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - hA_w T_w - 4\sigma\varepsilon_w A_w T_{mw}^3 T_w$$

$$= \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - \left(h + h_{rw}\right)A_w T_w \qquad (2.3)$$

Where $h_{rw} = 4\sigma\varepsilon_w T_{mw}^{\ 3}$, and T_{mw} is the mean of $T_w + T_\infty$ and T_∞. In the baking process the average value T_{mw} is observed as 353K (80ºC). Then we can find that the linearization introduces an error that is less than 4% to the radiation term (Figure 2.2). This error is further reduced by adding the convection term, which contributes more to the heat loss. Therefore the simplification affects T_p very little

so that it is safe to use it.

For plate:

$$C_p\dot{T}_p = p(t) - \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - hA_pT_p - \varepsilon_p A_p \sigma\left(\left(T_p + T_\infty\right)^2 + T_\infty{}^2\right)\left(T_p + 2T_\infty\right)T_p$$

$$\approx p(t) - \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - hA_pT_p - 4\sigma\varepsilon_p A_p T_{mp}^3 T_p$$

$$= p(t) - \frac{k_a A_w}{l_a}\left(T_p - T_w\right) - \left(h + h_{rp}\right)A_pT_p \tag{2.4}$$

Where $h_{rp} = 4\sigma\varepsilon_p T_{mp}{}^3$, and T_{mp} is the mean of $T_p + T_\infty$ and T_∞. Since T_p varies very little (2%) in the baking process (Figure 2.3), the simplification brings an error less than 1% to the radiation term in equation (2.4). Hence the difference between the models before and after linearization is negligible.

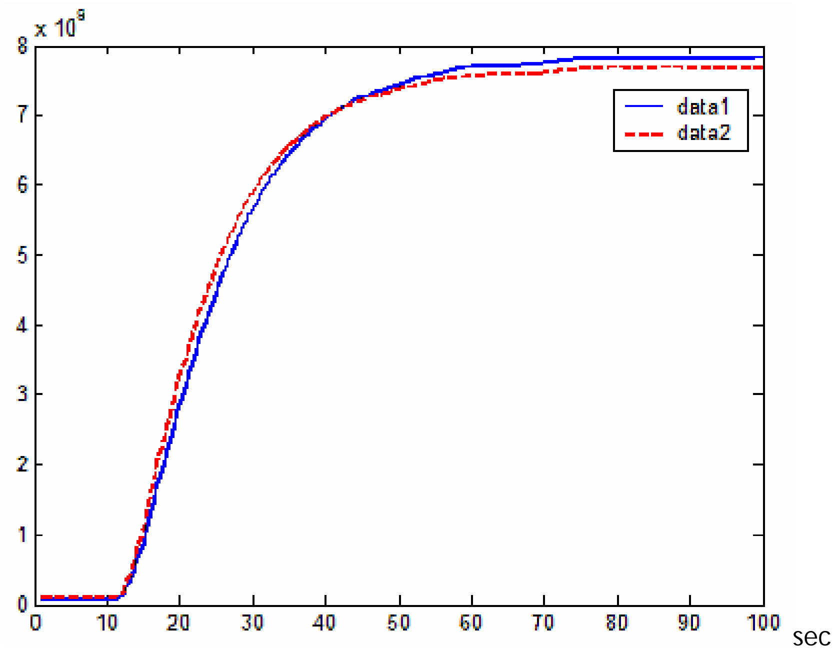
Let

$$R_a = \frac{l_a}{k_a A_w} \tag{2.5}$$

$$C_w = m_w c_w$$

$$R_w = \frac{1}{(h + h_{rw})A_w}$$

$$R_p = \frac{1}{(h + h_{rp})A_p}$$



data 1: Results of $(T_w + T_\infty)^4 - T^4{}_\infty$; Unit: K^4

data 2: Linearized results of $4T^3_{mw}T_w$. Unit: K^4

Figure 2.2 Comparison of Linearised and Unlinearised radiation terms in equation (2.3) on a typical baking process

Equation (2.3) and (2.4) can now be expressed as

$$C_w \dot{T}_w(t) = \frac{1}{R_a}\big(T_p(t) - T_w(t)\big) - \frac{1}{R_w} T_w(t) \tag{2.6}$$

$$C_p \dot{T}_p(t) = p(t) - \frac{1}{R_a}\big(T_p(t) - T_w(t)\big) - \frac{1}{R_p} T_p(t) \tag{2.7}$$

At steady state, $\dot{T}_w(\infty) = \dot{T}_p(\infty) = 0$ and Equations (2.6) and (2.7) give

$$T_w(\infty) = \frac{R_w}{R_w + R_a} T_p(\infty)$$

$$T_p(\infty) = \frac{R_p}{R_p + R_a} T_w(\infty) + \frac{R_p R_a}{R_p + R_a} p(\infty)$$

At the beginning of an experiment (t = 0), a wafer at ambient temperature ($T_w(0)$ = 0) is placed on the bakeplate maintained at a particular steady-state temperature, $T_P(0)$. With a Feedback controller, the bakeplate temperature recovered after the baking process, i.e. $T_p(\infty) = T_P(0)$ (Note in Figure 2.3).

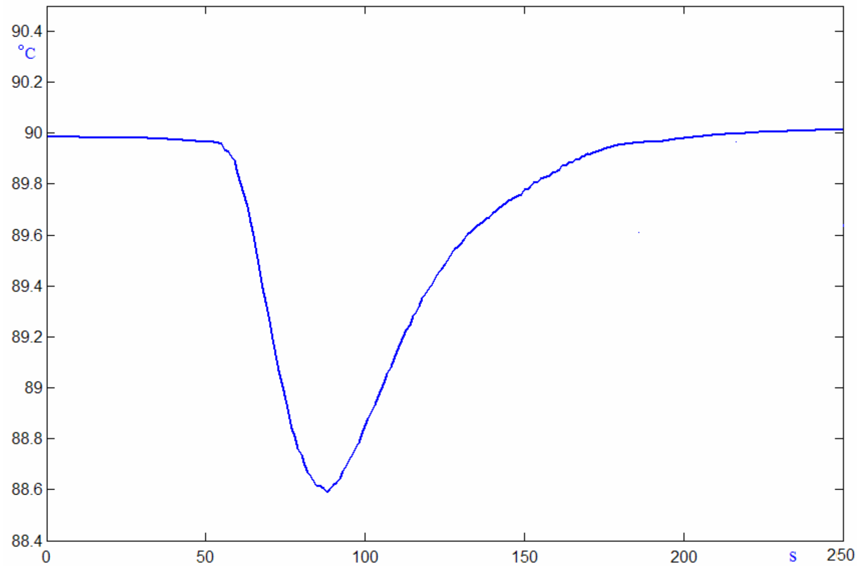


Figure 2.3 Typical variance of plate temperature in baking process

To simplify our analysis, the following new variables are defined.

$$\theta_w(t) = T_w(t) - T_w(\infty) = T_w(t) - \frac{R_w}{R_w + R_a} T_p(\infty)$$

$$\theta_p(t) = T_p(t) - T_p(\infty) = T_p(t) - \frac{R_p}{R_p + R_a} T_w(\infty) - \frac{RR_a}{R_p + R_a} p(\infty)$$

$$U(t) = p(t) - p(\infty)$$

Equation (2.6) and (2.7) can now be expressed as

$$C_w \dot{\theta}_w(t) = \frac{1}{R_a}[\theta_p(t) - \theta_w(t)] - \frac{1}{R_w}\theta_w(t)$$

$$C_p\dot{\theta}_p(t)=U(t)-\frac{1}{R_a}[\theta_p(t)-\theta_w(t)]-\frac{1}{R_p}\theta_p(t)$$

Laplace transformation gives

$$\Theta_w(s)\left(sC_w+\frac{1}{R_a}+\frac{1}{R_w}\right)=C_w\theta_w(0)+\frac{1}{R_a}\Theta_p(s) \tag{2.8}$$

$$\Theta_p(s)\left(sC_p+\frac{1}{R_a}+\frac{1}{R_p}\right)=U(s)+C_p\theta_p(0)-\frac{1}{R_a}\Theta_w(s) \tag{2.9}$$

Where

$$\theta_w(0)=T_w(0)-\frac{R_w}{R_w+R_a}T_p(\infty)$$

$$\theta_p(0)=T_p(0)-T_p(\infty)=0$$

Eliminating $\Theta_w(s)$ in Equations (2.8) and (2.9) gives

$$\Theta_p(s)=\Theta'_p(s)+D(s) \tag{2.10}$$

$$=\frac{B(s)}{A(s)}U(s)+D(s)$$

where $\Theta'_P(s)=\frac{B(s)}{A(s)}U(s)$ is the bakeplate temperature change due to the heat supplied by the heater to the bakeplate and *D(s)* denotes the temperature change resulting from heat removed from the bakeplate by dropping the cold wafer on the bakeplate. Further

$$\frac{B(S)}{A(s)}=\frac{\frac{1}{C_p}\left(s+\frac{1}{C_w}\left(\frac{1}{R_a}+\frac{1}{R_w}\right)\right)}{s^2+s\left(\frac{1}{C_w}+\frac{1}{C_p}\right)\left(\frac{1}{R_a}+\frac{1}{R_w}\right)+\frac{1}{C_wC_p}\left(\frac{1}{R_aR_w}+\frac{1}{R_aR_p}+\frac{1}{R_pR_w}\right)} \quad (2.11)$$

$$D(s)=\frac{\frac{1}{C_PR_a}}{s^2+s\left(\frac{1}{C_w}+\frac{1}{C_p}\right)\left(\frac{1}{R_a}+\frac{1}{R_w}\right)+\frac{1}{C_wC_p}\left(\frac{1}{R_aR_w}+\frac{1}{R_aR_p}+\frac{1}{R_pR_w}\right)}\theta_w(0) \quad (2.12)$$

The block diagram is shown in Figure 2.4, where $G_c(s)$ is the temperature controller.

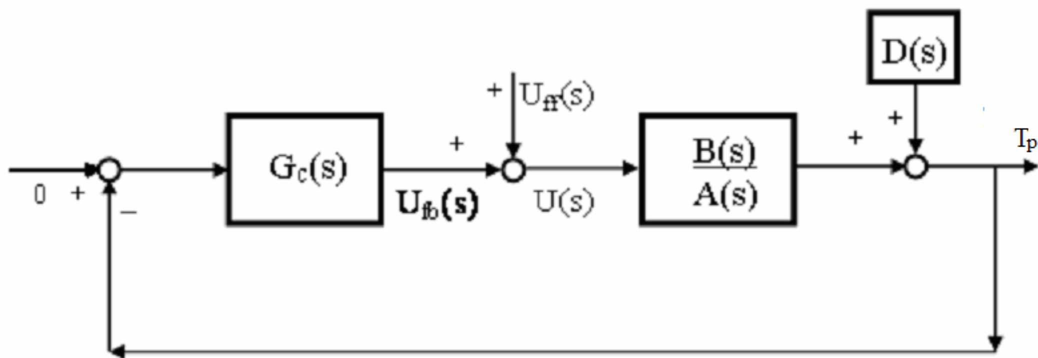


Figure 2.4 Block Diagram of the Baking Process

2.3 Conclusion

The thermal model for the baking process is built for the estimation of wafer warpage. One-dimensional analysis is used to characterize the dynamics of heat transfer for a silicon wafer at room temperature placed on a bakeplate maintained at a steady-state temperature by the Feed Forward and Feedback signals. Radiation is considered in the mathematical model to make it more precise. To simplify the model, radiation terms are linearized. Time domain modeling of the baking-system and disturbance is completed.

Chapter 3 Temperature Control

3.1 Introduction

We now develop the control strategy using linear programming to compensate for the load disturbance induced by the placement of the wafer at room temperature on the hot plate. This approach has been discussed elsewhere in the literature [8] and only the equations necessary for the computation in this thesis are given.

From Equation (2.10), we note that the effect of the disturbance, *D(s)*, on the temperature of the bakeplate, $\Theta_p(s)$, can be eliminated if,

$$\Theta'_p(s) + D(s) = 0$$

In other words, the input energy flux resulting from the heater balances the output energy flux due to the cold substrate. This can be accomplished without feedback control by adjusting the heater power using Equations (2.11) and (2.12)

$$\frac{B(s)}{A(s)} U(s) + D(s) = 0$$

$$U(s) = U_{ff}(s) = -\frac{A(s)}{B(s)} D(s) \tag{3.1}$$

In practice, because of bounds placed on the achievable input power from the heater, the control signal is subjected to saturation within lower and upper bounds, for example $U(t) = u \in [U^{min}, U^{max}]$. In this case,

$$\Theta'_p(s) + D(s) \neq 0$$

if the required input power is outside the achievable bounds. A simple implementation strategy would be to calculate the perfect control move as given by Equation (3.1), and then truncate at the boundaries.

3.2 Linear Programming

In this thesis, for our application we consider the optimal solution. To implement a practical solution, we discretize the problem in sampled data format, denoting the sampling indices as $k \in \{0, 1, ...\}$, and express the goal to minimize the maximum absolute error [2] as represented by the objective function

$$\min_{u(k)\in[0,U^{\max}]} \max_{k\in\{0,1,...N\}} \left|\theta_p{}'(k) + d(k)\right| \tag{3.2}$$

with the condition that the input is within prespecified limits and the desired output temperature remains equal to its initial steady-state condition over a time horizon *N*.

This optimization problem can be solved computationally by the use of the models in Equations (2.10) through (2.12).

Discretizing for computer implementation gives

$$\theta_P(k) = \theta_P'(k) + d(k)$$

$$= \frac{B(q^{-1})}{A(q^{-1})} u(k) + d(k) \tag{3.3}$$

where q^{-1} is the backward shift operator ($q^{-1}y(k) = y(k - 1)$) and

$$A(q^{-1}) = a_0 + a_1 + ... + a_n q^{-n} \tag{3.4}$$

$$B(q^{-1}) = b_0 + b_1 + ... + b_n q^{-n} \tag{3.5}$$

The order of the polynomials, *n*, has been assigned to be equal.

This discrete representation can also be expressed in a convolution model at sample time k,

$$\theta'_P(k) = \sum_{j=0}^{k} c_j q^{-j} u(k)$$

where the coefficients are given by

$$c_j = b_j - \sum_{l=1}^{n} a_l c_{j-l} \tag{3.6}$$

Over a finite interval, N, the input and output signals can be represented as finite–dimensional vectors. The solution between the input and output vectors over the interval N can be expressed as a Toeplitz matrix,

$$\Theta'_P = \Psi U$$

where

$$\Theta'_P = \begin{bmatrix} \theta_p'(0) \\ \theta_p'(1) \\ \vdots \\ \theta_p'(N) \end{bmatrix}, \qquad U = \begin{bmatrix} u(0) \\ u(1) \\ \vdots \\ u(N) \end{bmatrix},$$

$$\Psi = \begin{bmatrix} c_0 & 0 & \cdots & \cdots & 0 \\ c_1 & c_0 & 0 & \cdots & 0 \\ \vdots & & & & \\ c_N & c_{N-1} & \cdots & c_1 & c_0 \end{bmatrix}$$

The optimization problem of Equation (3.3) is equivalent to the following linear programming problem [2]:

Minimize

$$\begin{bmatrix}0 & \dots & 0 & 1\end{bmatrix}\begin{bmatrix}U \\ e\end{bmatrix} \qquad \text{objective function}$$

subject to

$$\begin{bmatrix}\Psi & -1_I \\ -\Psi & -1_I\end{bmatrix}\begin{bmatrix}U \\ e\end{bmatrix} \le \begin{bmatrix}-D \\ D\end{bmatrix} \quad \text{dynamic model}$$

$$U \le U^{\max} \quad \text{upper control signal saturation}$$

$$U \ge U^{\min} \quad \text{lower control signal saturation}$$

$$\Theta'_p(s) + D(s) = 0 \qquad k \in [n_f, \dots, N]$$

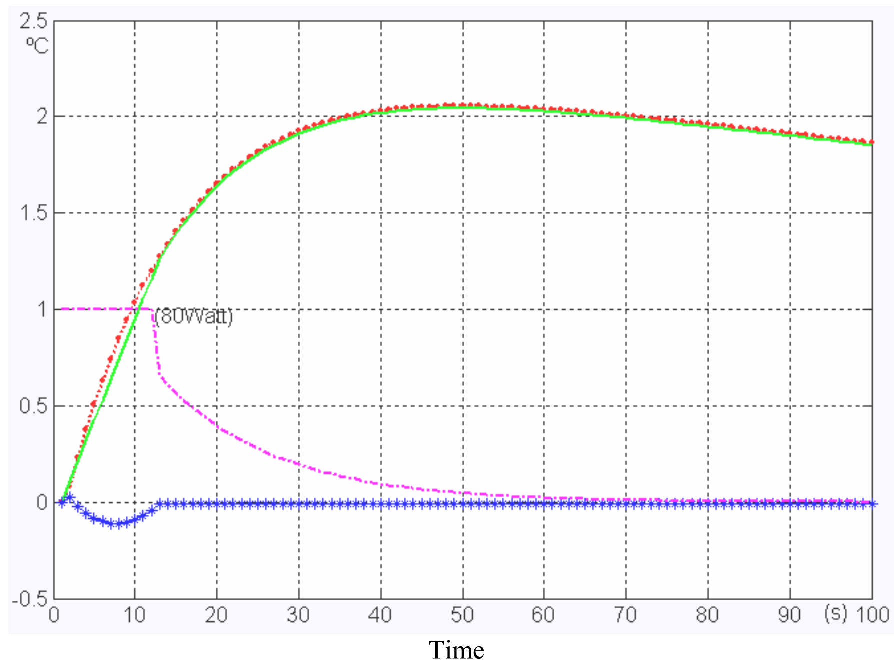
disturbance to be eliminated from n_f to N

where 1_I is a column vector with all I entries equal to one, $e(k) = \theta'_P(k) + d(k)$, and $D = [d(0)\ d(1)\ ...\ d(N)]'$. For vectors U and U^{max}, $U \le U^{max}$ means every entry of U is less than or equal to the corresponding entry of U^{max}. The value of n_f is chosen such that n_f is feasible and n_{f-1} is not. n_f is an integer and is reduced until the Linear program does not give a feasible solution. For instance if n_f=16 does not give a feasible solution then 17 will be chosen. This value is then chosen as the minimum time for eliminating the disturbance.

The detailed calculation is given in Appendix A.

In this thesis parameter $T_P(0) = T_P(\infty) = 62$ºC and $T_w(0) = 0$ºC. The thermal capacitance of the wafer is $C_w = 40.4$ J/K. Wafer heat loss resistance $R_w = 2.3$K/W,

can be computed directly from the handbook data [20]. The proximity pin of the plate is l_{pp} = 165 µm, which gives R_a = 0.43 K/W. C_P = 750 J/K and R_P = 0.59 K/W. Then the Feed Forward signal is obtained as the Dash-dotted line in Figure 3.1 (and Figure 4.2) by Linear Programming. The simulated *θ'(k)* and *e(k), d(k)* are also plotted in Figure 3.1.

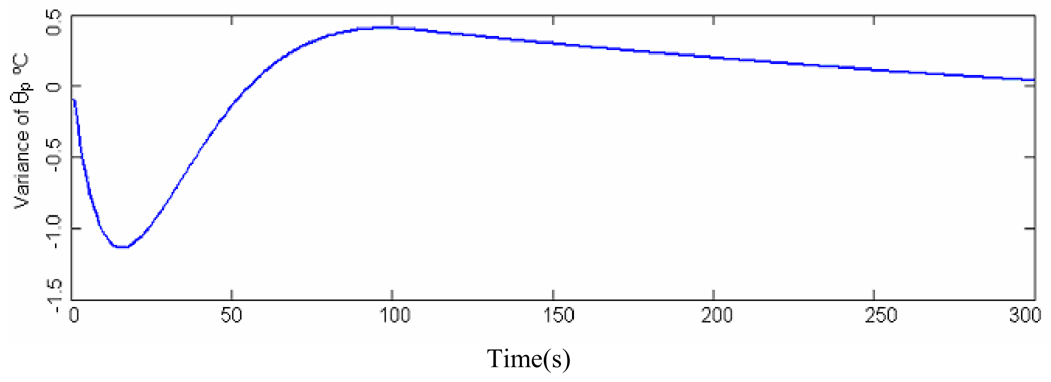


Time

Dotted line: The magnitude of disturbance (-*D*); Asterisk line: The error output of θ_P; Solid line: Response of $G_P(s)$ to $U_{ff}(\theta'_P)$; Dash-dotted line: Feed Forward Power (U_{ff}).

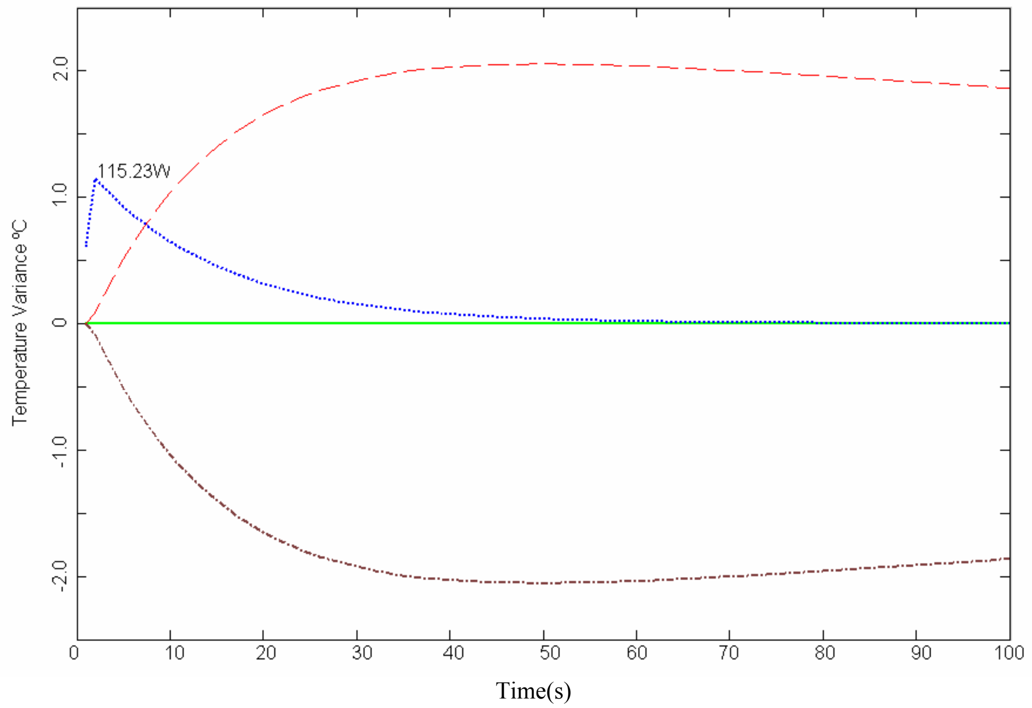
Figure 3.1 Simulation Result by Saturated Feed Forward Signal

Figure 3.1 shows that the error caused by disturbance is now improved to be within 0.15ºC. Comparing with the variance of θ_P without Feed Forward input in Figure 3.2, we can see that the stability of baking temperature is substantially improved. Figure 3.3 gives the simulation result of the Feed Forward signal without boundary. Theoretically the error is zero all through the process，while in Figure 3.1 the error deviates from zero due to the boundary of input.



Time(s)

Figure 3.2 Baking Temperature Deviation with Feedback control only



Time(s)

Solid Line: The error; Dotted Line: Un-saturated Feed Forward (FF) power; Dashed Line:

Simulated output of FF; Dash-dotted Line: Disturbance

Figure 3.3 Simulation results of Un-saturated Feed Forward

3.3 Conclusion

Feedback control is not ideal for eliminating the baking temperature disturbance. Feed Forward control strategy is applied to compensate for the load disturbance induced by the placement of the wafer at room temperature on the hot plate. In practice there is always a boundary on the input power, so optimal control method is used to calculate the Feed Forward (FF) signal. Simulation shows that the magnitude of baking temperature (T_P) variance is reduced 10× times with such a signal. Theoretically T_P can be kept in steady state with un-saturated FF signal.

Chapter 4 Experiment

4.1 Setup and Transfer Functions

Figure 4.1 gives the software implementation of the control strategy in Figure 2.4. The control signal and the output (baking temperature) are monitored with NI-LabVIEW panel on a PC, all the external data (plate and wafer temperature, control signal) are communicating with the LabVIEW through a NI-DAQ card.

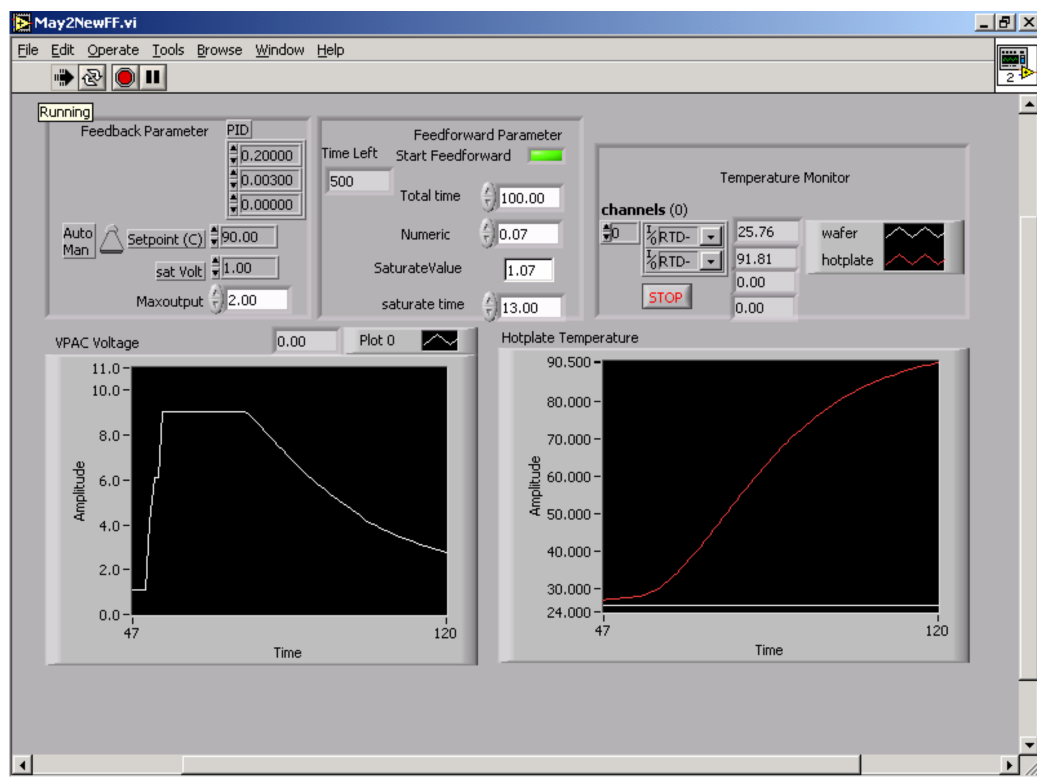


Figure 4.1 LabVIEW program used in experiment

The output voltage of the data acquisition system is 5.000V±2.5mV (after conditioning), and the output noise (0.1-10Hz) is only 4μV. The precision of RTD is 0.02ºC. The data is further filtered with LabVIEW software. Therefore the effect of measurement error is neglected.

The experiments are conducted at $T_P(0) = T_P(\infty) = 90^{\circ}C - 28^{\circ}C = 62^{\circ}C$ and $T_w(0) = 0^{\circ}C$. The thermal capacitance of the wafer, $C_w = 40.4$ J/K, and wafer loss resistance, $R_w = 2.3$K/W, can be computed directly from the handbook data [16]. For the given bakeplate, the proximity pin $l_{pp} = 165$ µm, $C_P = 750$ J/K and $R_P = 0.59$ K/W are expected to be fixed and hence can be determined beforehand. For $l_a = 165$ µm (flat wafer), Equation (2.5) gives $R_a = 0.43$ K/W. Substituting all the parameters into Equation (2.11) and (2.12) gives the transfer functions of hot plate and disturbance below (Refer to Appendix B for details).

$$\Theta_P(s) = \frac{7s + 0.5}{5283s^2 + 384s + 1}U(s) - \frac{866}{5283s^2 + 384s + 1} \tag{4.1}$$

Discretizing with 1 second sampling interval gives Equation (3.3) as

$$\theta_P(k) = \frac{0.0013q^{-1} - 0.0012q^{-2}}{1 - 1.9297q^{-1} + 0.9299q^{-2}}u(k) - 2.44\left(e^{-0.0027k} - e^{-0.07k}\right)$$

Once the model for $\theta_P(k)$ is known, the optimal FeedForward control signal obtained from linear programming with the constraint $-120 \text{ W} \leq u(k) \leq 80 \text{ W} \ \forall k \in \{0, 1, \ldots, N\}$ is computed as Figure 4.2 (Refer to Appendix A).

A Proportional-Integral Controller of the form

$$G_c(s) = K_p\left(1 + \frac{1}{sT_i}\right) = 36\left(1 + \frac{1}{67s}\right)$$

is used in the experiment and its discretization gives

$$G_c(q^{-1}) = \frac{36 - 35.46q^{-1}}{1 - q^{-1}}$$

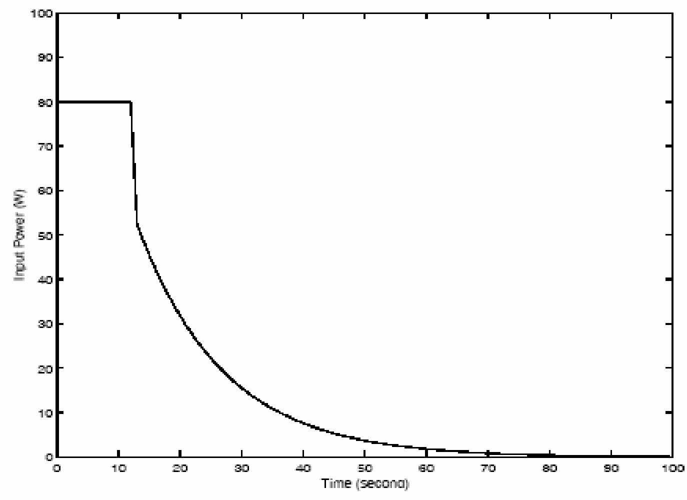


Figure 4.2 Feed Forward Control Signal

Figure 4.3 Hardware

4.2 Results and Discussion

All the parameters in the system block diagram of Figure 2.4 are known; $u_{ff}(k)$ is given in Figure 4.2. With the entire system of Figure 2.4, computer simulation (Simulink) can be run to give the output as shown in Figure 4.5. The maximum drop in temperature is -0.1ºC. By repeating the simulation for different values of l_a (which gives different values of R_a hence different transfer functions by equation (2.5), (2.11) and (2.12)), the maximum drop can be plotted against l_a as shown in Figure 4.6.

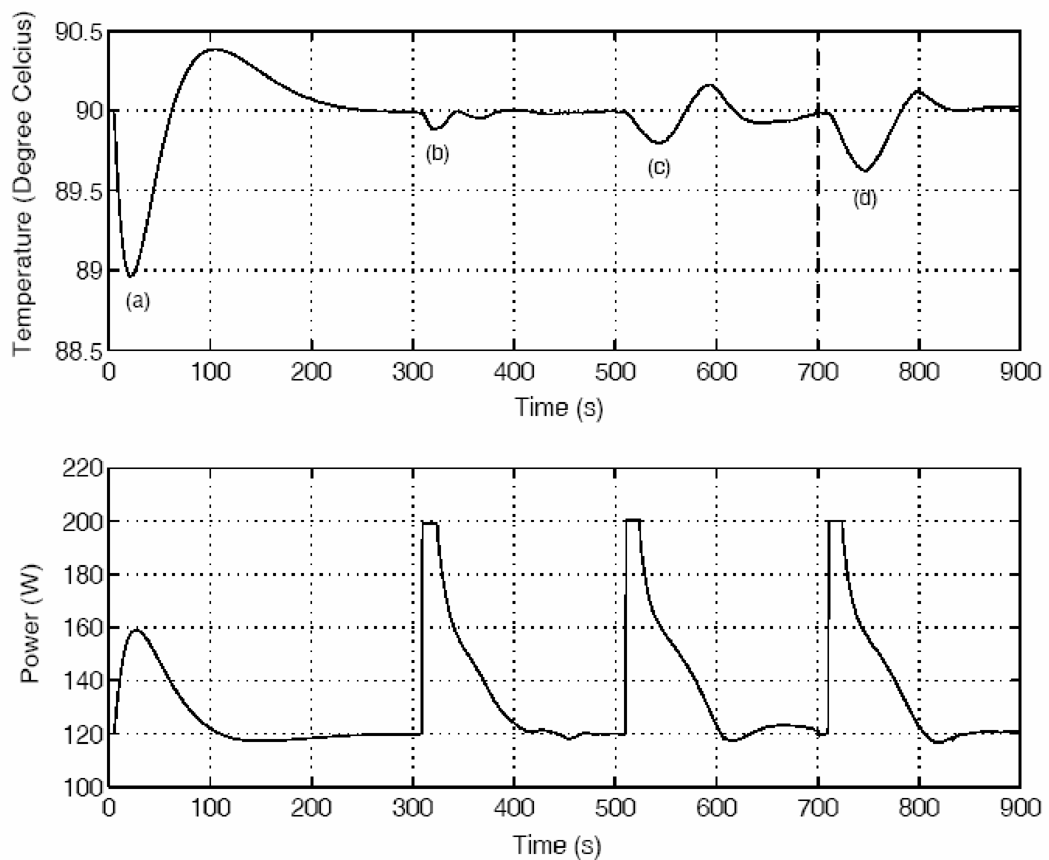


Figure 4.4 Experimental Data

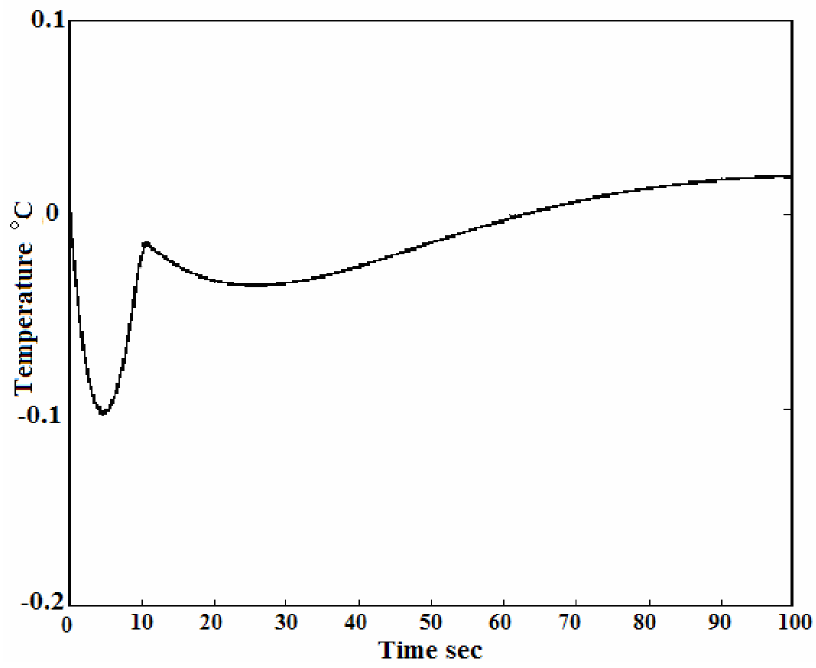


Figure 4.5 Temperature Disturbance Simulation

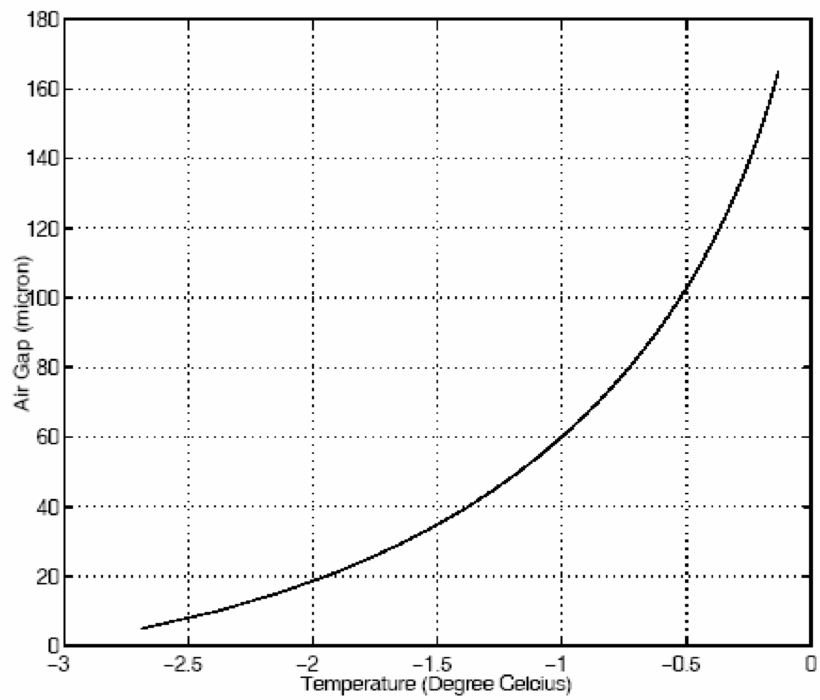
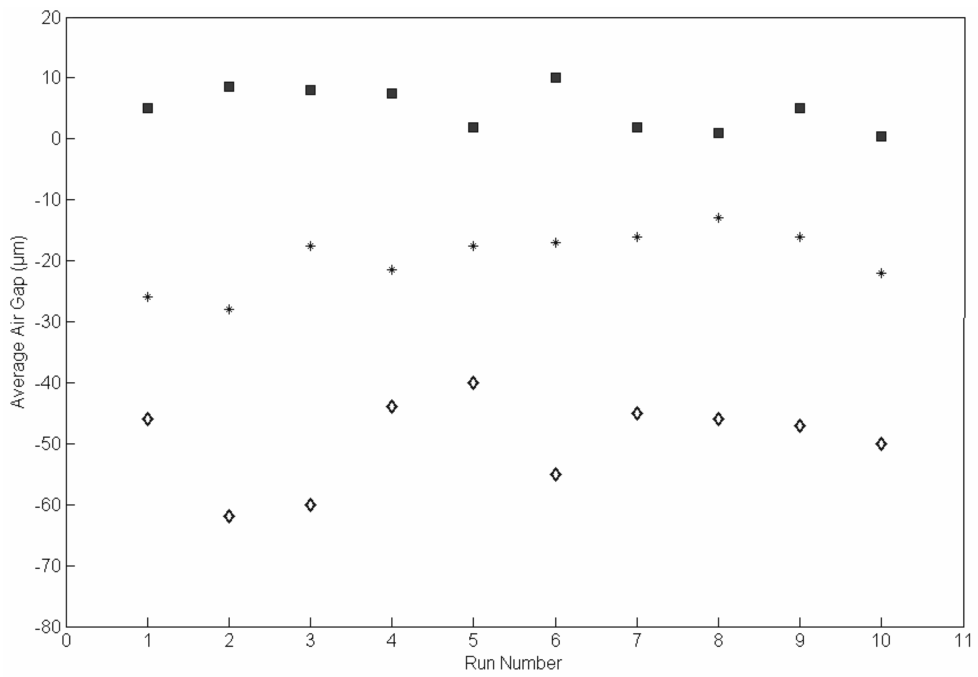
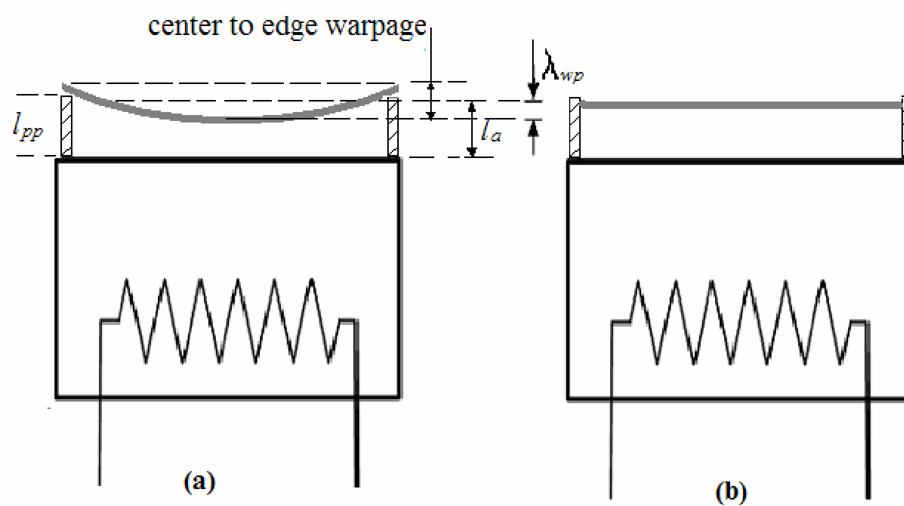


Figure 4.6 Nominal Air-gap, l_a, versus Temperature Drop



Square: run (b) flat wafer; Asterisk: run (c) warped wafer; Diamond: run (d) warped wafer

Figure 4.7 λ_{wp}, Experimental runs for the 3 different conditions outlined in Table 4.1



(a) the warped wafer (b) the equivalent flat wafer with air gap of l_a.

Figure 4.8 Warpage profile

The temperature disturbance with Feedback control only is given in experiment (a) of Figure 4.4. Temperature drop is about -1ºC. The temperature disturbance with Feedback and Feedforward control is given in Experiment (b).

The temperature drop is about -0.1ºC, which agrees well with the simulation result in Figure 4.5. Notice a 10× reduction in the magnitude of the temperature disturbance is achieved when Feedforward control is used. In contrast the temperature disturbance in [10] like Experiment (a) is larger than −1ºC because Feedforward control is not applied making it less suitable for industrial implementation.

Wafers with center-to-edge warpages of 55 µm and 110 µm are used for Experiments (c) and (d) respectively (Figure 4.8 gives the warpage shape). As shown in Figure 4.8, the baking process of a warped wafer is equivalent to the process of heating a flat wafer through a nominal air gap l_a. The results are given in Table 4.1. The deviation of bakeplate temperature are −0.2ºC and −0.38ºC respectively and the corresponding nominal air-gaps read from Figure 4.6 are l_a = 149 µm and l_a = 118 µm. The average warpages are λ_{wp} = −16 µm and λ_{wp} = −47µm respectively.

Table 4.1: Warpage Fault Detection (proximity pin of bakeplate, l_{pp} = 165 µm)

Run No.	Wafer Warpage	Maximum Temperature Drop in θ_p(ºC)	Nominal Air-Gap l_a (µm)	Average Warpage $\lambda_{wp}=l_a-l_{pp}$(µm)
(b)	flat	-0.12	167	2
(c)	Warped (55 µm center-to-edge)	-0.2	149	-16
(d)	Warped (110 µm center-to-edge)	-0.38	118	-47

Consider Experiment runs (b) and (d) in Table 4.1. The nominal air-gap, l_a, changes by about 50 µm from 167 µm to 118 µm while the temperature drop changes by more than 0.25ºC from −0.12ºC to −0.38ºC. In contrast, the sensitivity

in [10] for detecting l_a is lower i.e. 0.1ºC change in temperature for a 50 μm change in l_a. Hence, in this thesis, temperature is more sensitive to change in l_a, which is important for detecting warpage from temperature. The reason for the improvement of sensitivity is the use of Feedforward control signal. The Feedforward signal is computed based on a flat wafer, so when a warped wafer comes, the balance between disturbance and Feedforward power is disrupted. Thus the Feedforward power becomes an extra disturbance, which increases the fluctuation of T_p given a same PID controller.

Since a flat wafer is used for Run (b), l_a is expected to be close to the length of the proximity pin, l_{pp}; and the average warpage $\lambda_{wp} = l_a - l_{pp} = 2$ μm. Note that λ_{wp} is the deviation of the nominal air gap from the proximity pin in a warped wafer (see Figure 4.8) and is a good measure of the extent of warpage. If the deviation is large, then warpage is large. A standard approach to fault detection is to define a threshold based on manufacturing requirements and any violation of the threshold is considered a fault. For instance if the maximum warpage allowed is $100\mu m$, the threshold can be selected as 30~50μm. The optimal value could be determined by practical experience. A curve like Figure 4.6 can be obtained by physical analysis or by experimental identification. Once a T_p out of the range corresponding to l_a=l_{pp}±(30~50μm) is observed, the wafer should be treated as over-warped. The method is able to detect wafers with regular warpage profile. The un-regular ones can be found out by setting the threshold to a relatively lower value.

To verify the repeatability of the method 9 more experiments are conducted for run (b), (c) and (d) in Figure 4.4. The respective minimum θ_p is used to find corresponding nominal air gap through Figure 4.6. The average warpage in each

experiment is plotted in Figure 4.7, which shows that the statistical error of the experiments is acceptably low.

4.3 Conclusion

Experiments demonstrated that it is possible to detect warpage fault from the extreme baking temperature. Baking temperature gives a clear indication of the warpage if other conditions are kept unchanged. The temperature drop with Feedback and FeedForward control is a 10 × reduction in the magnitude compared to that with only Feedback control. And in this situation temperature is more sensitive to the change of air gap (l_a) which is important for detecting warpage from temperature variance. Experiments also prove that the method is repeatable.

Chapter 5 Conclusion

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence. In this thesis, advanced process control reduces temperature disturbance to about a tenth of a degree Celsius, which is a 10× increase of the processing stability from Feedback control only.

It has been demonstrated that warpage can still be detected and more importantly, there is no loss in sensitivity in the detection strategy even though the temperature disturbance that provides the signal for detecting warpage is small.

Experimental results show that baking temperature (T_p) is uniquely determined by average wafer warpage given a certain baking system, which agrees well with the thermal analysis. Conversely, the over-warped wafer can be identified by comparing the extreme baking temperature with the record of known air gap (critical value). Thus this method simplifies the process to distinguish wafers with a warpage out of requirement, even if it is not able to determine the amount of warpage because the warpage form is irregular.

It has been proved by experiments that the method has a positive character of repeatability. The estimated warpage differences from case to case are small enough to be within the threshold.

The method can be extended to the industrial environment from laboratory conditions. It is possible to find stable T_p curves with wafers warped to a certain

amount, given that the ambient conditions are fixed (and this is always the truth in practice). The Feed Forward signal to eliminate the disturbance by an un-warped wafer can be obtained with methods given in Chapter 3. Then the in-line observed data of T_p should be compared with the curves built by experiments.

This thesis has demonstrated that it is possible to detect warpage fault from the minimum temperature. The accuracy is expected to be improved if more sophisticated estimation technique is used. For example, an extension is to consider area under the temperature curve instead of just the minimum point. Yet, an even more elaborate method is to fit the complete temperature trajectory of the bakeplate with the model in the least square sense. These more elaborate techniques can be investigated in future once the concept of relating temperature to warpage is established.

Appendix A

From equation (2.10), (3.3) and (4.1) we can get the [a_0 a_1 a_2] = [1 -1.9297 0.9299] in equation (3.4) and [b_0 b_1 b_2] = [0 0.0013 -0.0012] in equation (3.5).

Then from equation (3.6), the value of c_j can be computed.

With $\theta'_P(0) = 0$,

$$\begin{aligned}\theta'_P(1) &= \frac{B(q^{-1})}{A(q^{-1})}u(1) + \theta'_P(0) \\ &= \frac{b_0 + b_1 q^{-1} + b_2 q^{-2}}{a_0 + a_1 q^{-1} + a_2 q^{-2}}u(1) + 0 \\ \Rightarrow \theta'_P(1) &= 0 + b_1 u(0)\end{aligned}$$

Similarly, integration with equation $\theta'_P(k) = \sum_{j=0}^{k} c_j q^{-j} u(k)$ we can get

$$\begin{aligned}\theta'_P(2) &= b_0 u(2) + b_1 u(1) + (b_2 - a_1 b_1)u(0) \\ &= c_0 u(2) + c_1 u(1) + c_2 u(0)\end{aligned}$$

Thus

$$c_0 = 0;\ c_1 = 0.0013$$

Then from equation (3.6)

$$\begin{aligned}c_2 &= b_2 - \sum_{l=1}^{2} a_l c_{2-l} \\ &= -0.012 - a_1 c_1 - a_2 c_0 \\ &= 0.001309\end{aligned}$$

Continue with the computation we can get the value of c_j for $j \leq N = 100$.

And c_j can also be found by impulse the transfer function of

$$\frac{B(q^{-1})}{A(q^{-1})} = \frac{b_0 + b_1 q^{-1} + b_2 q^{-2}}{a_0 + a_1 q^{-1} + a_2 q^{-2}}$$

The computation results of c_j are given below:

[0.0000000 0.0013242 0.0013224 0.0013205 0.0013184
0.0013163 0.0013141 0.0013118 0.0013095 0.001307
0.0013045 0.0013019 0.0012993 0.0012966 0.0012939
0.0012911 0.0012883 0.0012854 0.0012826 0.0012796
0.0012767 0.0012737 0.0012707 0.0012677 0.0012646
0.0012616 0.0012585 0.0012554 0.0012523 0.0012492
0.0012461 0.001243 0.0012398 0.0012367 0.0012335
0.0012304 0.0012272 0.0012241 0.0012209 0.0012177
0.0012146 0.0012114 0.0012082 0.0012051 0.0012019
0.0011988 0.0011956 0.0011924 0.0011893 0.0011861
0.001183 0.0011799 0.0011767 0.0011736 0.0011705
0.0011674 0.0011643 0.0011611 0.001158 0.001155
0.0011519 0.0011488 0.0011457 0.0011426 0.0011396
0.0011365 0.0011335 0.0011304 0.0011274 0.0011244
0.0011213 0.0011183 0.0011153 0.0011123 0.0011093
0.0011063 0.0011034 0.0011004 0.0010974 0.0010945
0.0010915 0.0010886 0.0010856 0.0010827 0.0010798
0.0010769 0.001074 0.0010711 0.0010682 0.0010653
0.0010624 0.0010596 0.0010567 0.0010539 0.001051
0.0010482 0.0010454 0.0010425 0.0010397 0.0010369]

The disturbance may also be found by equation (4.1), where

$$D(s) = \frac{-866}{5283s^2 + 384s + 1}$$

$$D(q^{-1}) = \frac{-0.0800q^{-1} - 0.0781q^{-2}}{1.0 - 1.9297q^{-1} + 0.9299q^{-2}}$$

Then we get the value of $-D$ used to calculate the Feed Forward signal:

[0.0000 0.08001 0.23249 0.37424 0.50598
0.62839 0.74211 0.84772 0.94577 1.0368
1.1212 1.1995 1.2721 1.3394 1.4017
1.4594 1.5128 1.5621 1.6078 1.6499
1.6888 1.7246 1.7576 1.7880 1.8159
1.8415 1.8650 1.8865 1.9062 1.9241
1.9405 1.9553 1.9687 1.9808 1.9917
2.0015 2.0103 2.0180 2.0249 2.0309
2.0361 2.0405 2.0443 2.0475 2.0500
2.0520 2.0535 2.0545 2.0550 2.0552
2.0549 2.0543 2.0534 2.0522 2.0506
2.0488 2.0468 2.0445 2.0420 2.0393
2.0365 2.0334 2.0302 2.0269 2.0234
2.0198 2.0161 2.0122 2.0083 2.0043
2.0002 1.9960 1.9917 1.9874 1.9830
1.9786 1.9741 1.9696 1.9650 1.9604
1.9558 1.9511 1.9464 1.9417 1.9369
1.9321 1.9273 1.9225 1.9177 1.9129
1.9080 1.9032 1.8983 1.8935 1.8886
1.8837 1.8788 1.8740 1.8691 1.8642]'

Now we get the matrix of Ψ and D, then with Matlab function "lp" we can solve the optimal input power U by minimizing the error. The conditions are:

$$\begin{bmatrix} \Psi & -1_I \\ -\Psi & -1_I \end{bmatrix} \begin{bmatrix} U \\ e \end{bmatrix} \leq \begin{bmatrix} -D \\ D \end{bmatrix}$$

$$U^{\min} \leq U \leq U^{\max} \text{ with } U^{\min} = -120;\ U^{\max} = 80$$

The solution is shown in Figure 3.1 and Figure 4.4.

Appendix B

The calculation of transfer functions of $B(s)/A(s)$ and $D(s)$.

For run (b) in Table 4.1,

l_a= 165μm

$$R_a = \frac{l_a}{k_a A_w} = \frac{165\times 10^{-6}}{0.012\times 0.0314} = 0.43K/W$$

$$\theta_w(0) = -\frac{R_w}{R_w + R_a} T_p(\infty) = \frac{2.3\times 62}{2.3+0.43} = 52.2$$

According to equation (2.11) and (2.12),

$$\frac{B(S)}{A(s)} = \frac{\frac{1}{C_p}\left(s + \frac{1}{C_w}\left(\frac{1}{R_a}+\frac{1}{R_w}\right)\right)}{s^2 + s\left(\frac{1}{C_w}+\frac{1}{C_p}\right)\left(\frac{1}{R_a}+\frac{1}{R_w}\right) + \frac{1}{C_w C_p}\left(\frac{1}{R_a R_w}+\frac{1}{R_a R_p}+\frac{1}{R_p R_w}\right)}$$
$$= \frac{0.00135s + 0.0000923}{s^2 + 0.0727s + 0.000189}$$
$$= \frac{7s+0.5}{5283s^2 + 384s + 1}$$

$$D(s) = \frac{\frac{1}{C_P R_a}}{s^2 + s\left(\frac{1}{C_w}+\frac{1}{C_p}\right)\left(\frac{1}{R_a}+\frac{1}{R_w}\right) + \frac{1}{C_w C_p}\left(\frac{1}{R_a R_w}+\frac{1}{R_a R_p}+\frac{1}{R_p R_w}\right)}\theta_w(0)$$
$$= \frac{0.165}{s^2 + 0.0727s + 0.000189}$$
$$= \frac{866}{5283s^2 + 384s + 1}$$

Similarly for run (c), l_a=137.5μm,

$$\frac{B(S)}{A(s)} = \frac{6.09s + 0.48}{4566.2s^2 + 381.6s + 1}$$

$$D(S) = \frac{892.4}{4566.2s^2 + 381.6s + 1}$$

For run (d), l_a=110μm,

$$\frac{B(S)}{A(s)} = \frac{5.02s + 0.48}{3726.7s^2 + 389.9s + 1}$$

$$D(S) = \frac{939.1}{3726.7s^2 + 389.9s + 1}$$

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