STRESS-INDUCED LEAKAGE CURRENT IN DUAL-GATE CMOSFETS WITH THIN NITRIDED GATE OXIDES

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SUMMARY

Beginning with a brief review of the literature about stress-induced leakage current (SILC), a study of the SILC in the dual-gate CMOSFET with 2.2 nm nitrided gate oxide has been presented, from the observation of the evolution of hole and electron current components.

In the p+/pMOSFET, the hole component of the SILC dominates over the electron component, and such dominance is enhanced continuously during stress. A physical model, featuring two separate energy distributions of oxide traps and favoring hole tunneling in the p+/pMOSFET, is proposed to explain the observed evolution of hole current and electron current components. Oxide trap localization near the substrate valence band is probably responsible for the dominance of hole current. Such a localized trap distribution could be generated by hole injection into the gate oxide. The proposed physical model is consistent with the established TAT framework for SILC

In the n+/nMOSFET, SILC is found to be dominated by the conduction-band electron tunneling, which is attributed to the trap-assisted tunneling (TAT) mechanism facilitated by a heavily one-sided stress-induced trap distribution, localized near the substrate conduction band edge.

Degradation of the ultrathin gate oxide process can be well visualized by the generation and increase of SILC. Before oxide breakdown happens, both p+/pMOS and n+/nMOS demonstrated the partial recovery of degradation after the withdrawal of stress voltage but before the oxide breakdown. A solid correlation exists between degradation rate of the gate oxide and charge injection. The sharp decrease of SILC generation

probability at high charge injection indicates that neutral oxide trap generation tends to saturate at high stress level.

LIST OF FIGURES

LIST OF SYMBOLS

Ec	Energy level of conduction band edge of silicon
Ev	Energy level of valence band edge of silicon
J_g	Gate leakage current density of a MOSFET
J_{sd}	Source-drain current density of a MOSFET in carrier separation measurement
J_{sub}	Substrate current density of a MOSFET in carrier separation measurement
J_{g0}	Initial gate leakage current density
J_{sd0}	Initial source-drain current density
J_{sub0}	Initial substrate current density
ΔJ_g	Gate SILC
ΔJ_{sd}	Change of source-drain current sensed by carrier separation measurement
ΔJ_{sub}	Change of substrate current sensed by carrier separation measurement
L	Channel length of a MOSFET
ΔN_{te}	Change of neutral oxide trap density responsible for electron tunneling
ΔN_{th}	Change of neutral oxide trap density responsible for hole tunneling
N_{te}	Neutral oxide trap density responsible for electron tunneling
N_{th}	Neutral oxide trap density responsible for hole tunneling
P_{gen}	Trap generation probability
Q_{bd}	Charge-to-breakdown
Q_{inj}	Charge injection fluence
T_{ox}	Gate oxide thickness
T_{bd}	Time-to-breakdown

t_s	Cumulative stress time
V_b	Voltage applied the body substrate during substrate hot carrier injection
V_g	Gate voltage of a MOSFET
V_{ox}	Voltage drop across the gate oxide
V_{oe}	Gate voltage at which hole SILC is half of gate SILC
V_{sd}	Source-drain voltage of a MOSFET
V_s	Stress voltage during constant-voltage stress applied to the gate
V_{sub}	Substrate voltage of a MOSFET
V_w	Voltage applied the well during substrate hot carrier injection
W	Channel width of a MOSFET
β	Slope the correlation of hole SILC with electron SILC in double-log scale

NOMENCLATURES

AHI	Anode hole injection
AHR	Anode hydrogen release
CAT	Charge-assisted tunneling
CBE	Conduction-band electron
CHE	Channel hot electron
CMOS	Complementary metal-oxide-semiconductor
CMOSFET	Complementary metal-oxide-semiconductor field-effect transistor
CVS	Constant voltage stress
DT	Direct-tunneling
FNT	Fowler-nordheim tunneling
HBD	Hard-breakdown
HV-SILC	High-voltage SILC
LV-SILC	Low-voltage SILC
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
RTAT	Recombination and trap-assisted tunneling
RTO	Rapid thermal oxidation
SBD	Soft-breakdown
SHCI	Substrate hot carrier injection
SHEI	Substrate hot electron injection
SHHI	Substrate hot hole injection
SILC	Stress-induced leakage current
TAT	Trap-assisted tunneling
TDDB	Time-dependent dielectric breakdown
TDDW	Time-dependent dielectric wearout
THAT	Thermal-assisted tunneling

ULSI	Ultra large scale integration
VBE	Valence-band electron

Chapter 1

Introduction and Literature

1.1 Gate Oxide Scaling and Reliability

The quest for higher packaging density, faster circuit speed and lower power dissipation has been relentlessly driving complementary metal-oxide-semiconductor (CMOS) devices to ever smaller dimensions in the past three decades. For current ultra large scale integration (ULSI) applications, the state-of-art technology is 0.11 μm. It will soon advance to 90 nm or even 65 nm in the very near future. CMOS devices with even smaller channel lengths (50 nm and sub-50 nm) have been successfully fabricated in research laboratories [1] - [7]. According to the International Technology Roadmap for Semiconductor (ITRS), gate length scaling will continue in a two-year cycle until 2007 [8], when the minimum feature size reaches 25 nm.

The scaling of the gate length must be accompanied by a corresponding reduction in the gate oxide thickness [9] [10], in order for the gate voltage to maintain enough control over the channel, thus suppressing the 2-D short channel effects and maintaining a good subthreshold slope. During the past two decades, MOSFET scaling has been primarily, but not exactly, following the constant-field scaling scheme, proposed by Dennard *et al.* [11] [12]. For CMOS logic technology, gate oxide thickness decreases from 20 nm to 1.5 nm, when the gate length reduces from 1 μm to 100 nm, corresponding to a reduction in supply voltages from 5 V to 1.0 V. On the other hand, a reduced oxide thickness is also desirable for non-volatile memory devices, as the programming voltage could then be significantly reduced.

One of the key factors for the success of the MOS technology is the long list of extraordinary thermal and electrical properties of SiO_2 and its excellent scaling and process integration capabilities. However, SiO_2 is not perfect and suffers from some reliability problems. In the conventional MOS devices, the thin oxide layer is subjected to a gate voltage of several volts, resulting in a high oxide field. Continuous scaling of the CMOS technology gradually increases this oxide field, since the operating voltage has been scaled down less aggressively. In state-of-art logic CMOS devices, the oxide field is about 6 MV/cm [13]. At such a high field, the oxide properties gradually degrade, constituting the much-studied time-dependent dielectric breakdown (TDDB) phenomenon. Even though it has been the subject of numerous studies in the past three decades [13] - [15], a complete understanding of oxide degradation is still lacking and its implications on the reliability of devices and circuits remain unclear. Among the many models presented to explain the degradation and breakdown of silicon dioxides under electrical stress, two were widely accepted. They are the Anode Hole Injection (AHI) model [16] and Anode Hydrogen Release (AHR) model [17]. Another widely cited model is the thermochemical model (or *E*-model) [18] [19]. Despite continuing controversy, at least the following agreements have been reached. First, there is a force, such as the voltage, electric field or and/or tunneling current that drives the degradation and breakdown of the silicon dioxide film. Second, defects, including interface traps, bulk oxide traps and trapped charges, are generated, resulting in additional increase in the leakage current. Third, there exists a vital criterion that characterizes the final oxide breakdown, e.g. the hole fluence in the AHI model and the critical defect density in the percolation model.

When oxide thickness is scaled down to the nanometer regime, several new phenomena related to oxide reliability occur: Ballistic and direct tunneling [20], polarity-dependent oxide breakdown (including both time-to-breakdown (T_{bd}) and charge-to-breakdown (Q_{bd})) [21] - [23], decrease in the Weibull slope of the breakdown distribution [24] [25] and soft breakdown (SBD) [26] - [31]. These new phenomena add to the complexity of gate oxide reliability.

For thick oxides ($T_{ox} > 5$ nm), oxide breakdown is characterized by a sudden change in current or voltage during electrical stress, due to the formation of a highly conductive ohmic short between anode and cathode by the propagation of thermal damage (hard

breakdown, HBD). This conductive path has been verified to be localized. Usually, the HBD is followed by immediate device and circuit failure. However, for ultrathin oxides, another mode of oxide failure exists. This failure mode has been termed as soft, quasi, early, nondestructive, electric breakdown, or B-mode SILC, characterized by the creation of a more resistive breakdown path. The latter had been proposed as the dominant mode of failure for ultrathin gate oxides. However, the so-called soft breakdown (SBD) models have been challenged in recent years. Weir *et al*. [32] convincingly showed that devices remained functional even after soft breakdown of ultrathin gate dielectrics. Cheung reported that soft breakdown of the ultrathin gate oxide could probably be an experimental artifact induced by the inability of the device to eliminate the current surge at the moment of the formation of a percolation path [33]. Recently, a novel argument was proposed to account for a unique phenomenon: progressive degradation of ultrathin gate oxides. It was argued that ultrathin gate oxides actually would not breakdown (at least not in the manner of HBD or SBD), but will progressively degrade, as revealed by the progressive increase in the leakage current and/or current noise under constant voltage stress [34] - [36]. Wu *et al.* proposed a new Time-Dependent Dielectric Wearout (TDDW) technique to measure and characterize the degradation of ultrathin gate oxides [37].

Above all, downscaling of gate oxide thickness, has complicated, rather than simplified the gate oxide reliability issues. Established models are continuously challenged. A further understanding of the degradation process and mechanism of ultrathin gate oxides is greatly needed.

1.2 Intrinsic Leakage Currents in Gate Oxides

Current conduction in high-field-stressed oxides consists of two parts: Intrinsic part and stress-induced part. Depending on the oxide thickness and the magnitude of the electric field, one of these two mechanisms, Fowler-Nordheim Tunneling (FNT) and Direct Tunneling (DT), is responsible for the intrinsic leakage current. For oxides thicker than 30 Å, the intrinsic current can be well modeled as FNT. For thinner oxides, DT current dominates the intrinsic current. The difference of these two tunneling

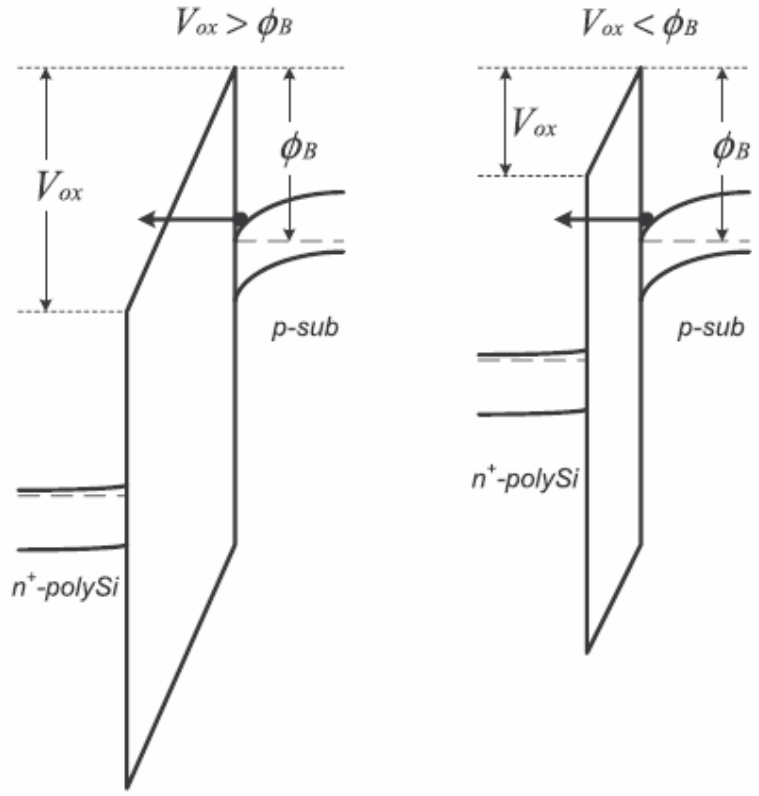

Figure 1.1: Illustration of two major tunneling mechanisms: (left) Fowler-Nordeim Tunneling and (right) Direct Tunneling.

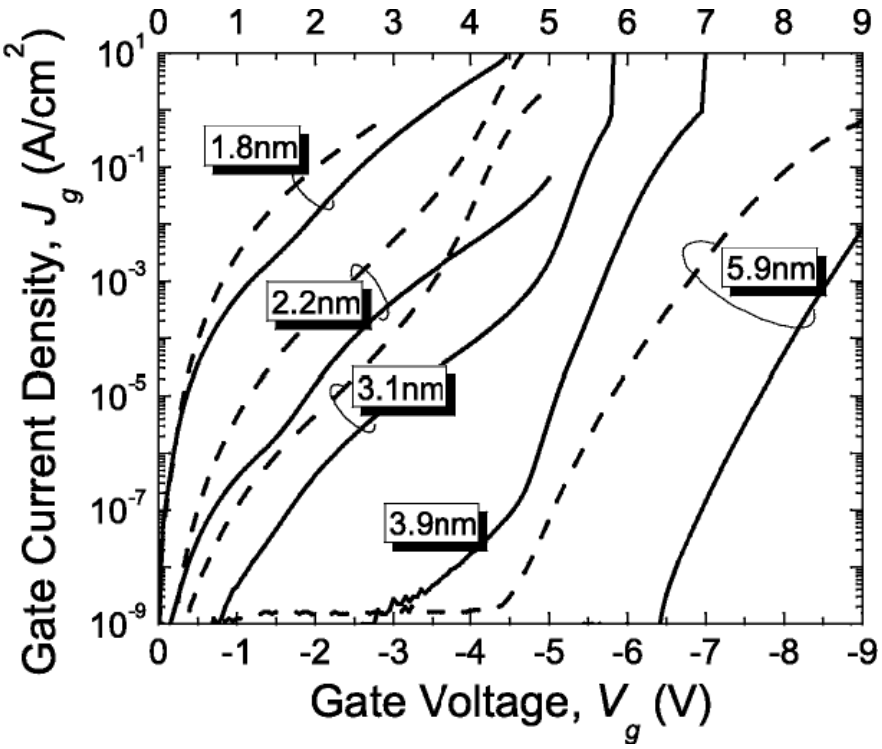

Figure 1.2: Intrinsic gate leakage current in dual-gate CMOSFETs with different oxide thickness. Measurement was done under inversion mode. The characteristics for both p+/pMOS (solid lines) and n+/nMOS (dashed lines) are shown.

mechanisms lies in the tunneling barriers involved, as shown in Figure 1.1. In FNT, the voltage across the oxide (V_{ox}) is larger than the barrier height (ϕ_B), and electrons tunnel through a triangular energy barrier. The current density can be written as

$$J_{\mathrm{FN}} \cong A \cdot E_{\mathrm{ox}}^2 \cdot \exp(-B / E_{\mathrm{ox}}). \tag{1.1}$$

where A and B are constants. The former is related to the doping density and oxide thickness, and the latter is related to the tunneling barrier height. E_{ox} is the oxide electric field.

For DT, however, $V_{\mathrm{ox}} < \phi_{\mathrm{B}}$ and the energy barrier is trapezoidal. One representative model for DT taking into consideration of quantum mechanical effects is given as,

$$J_{\mathrm{DT}} \cong J_{\mathrm{FN}} \cdot 2(1-\frac{V_{\mathrm{ox}}}{2\phi_{\mathrm{B}}}) \cdot (\frac{\phi_{\mathrm{B}}}{V_{\mathrm{ox}}}) \cdot \exp(\frac{\beta(\frac{\phi_{\mathrm{B}}-V_{\mathrm{ox}}}{\phi_{\mathrm{B}}})^{3/2}}{E_{\mathrm{ox}}}). \tag{1.2}$$

The intrinsic gate leakage currents in dual-gate CMOSFETs with oxides of five different thicknesses are plotted in Figure 1.2. The transition from FNT current to DT current is clearly shown. For T_{ox} = 3.1 nm and below, the gate leakage is primarily a DT current, while for T_{ox} = 3.9 nm and T_{ox} = 5.9 nm, the gate leakage is mainly FNT current. As the oxide thickness scales down, the leakage current increases dramatically; at the same time the gate current difference between n+/nMOSFET and p+/pMOSFET becomes smaller. The DT leakage thus imposes a critical limit on the further downscaling of silicon-dioxide-based ULSI devices.

1.3 Stress-Induced Leakage Currents in Gate Oxides

When a high electrical field is applied to the gate oxide, a number of phenomena related to the degradation of oxide properties occur: charge trapping, bulk trap generation, interface state generation and stress-induced leakage current (SILC) increase. These phenomena occur concurrently and may interact with one another. SILC is of

great importance among them. SILC was first reported by Maserjian and Zamani [38] [39]. Initially, it was defined as the excess low field leakage current induced by high-field stress. Physically speaking, SILC is the additional leakage current originating from stress-induced damage in the oxide and/or interfaces. Electrical stress induces charges and traps in the oxide and at the interface, and these defects modify the tunneling leakage current through the oxide. In practice, SILC is directly related to two important reliability issues: stand-by power dissipation of CMOS circuits and data retention time of non-volatile memory devices. Increased leakage current means more stand-by power dissipation for the former, while shorter data retention time for the latter [40]. Following the pioneering work of Maserjian and Zamani, an extensive research on SILC has been done. It has been widely accepted that carrier conduction in SILC is inelastic and defect-assisted. However, two major issues have been under debate for over two decades. First, what kinds of defects are involved (trap charges, bulk oxide traps, or interface states)? Second, how do they facilitate carrier conduction through the gate oxide?

1.3.1. General Physical Characteristics of SILC

A Classical Illustration of SILC

A classical illustration of SILC is given in Figure 1.3 and Figure 1.4. The SILC characteristics are obtained from dual-gate CMOSFET devices with 5.9 nm oxide. In Figure 1.3, the two J_g-V_g curves are measured consecutively. In the first measurement, the voltage ramp was stopped at a high value. The SILC shows itself at low gate voltage in the second curve. This is due to oxide damage induced by the first measurement. A more common way to obtain SILC is to subject the device to a certain type of stress (such as constant current stress, constant voltage stress, ac stress, etc.) and to compare the pre- and post-stress J_g-V_g characteristics. Shown in Figure 1.4 is a group of J_g-V_g curves similar to those in Figure 1.3, but in the former, the devices were subjected to a constant voltage stress (CVS). Note that in both figures, the post-stress gate current at high measurement voltage is actually lower than the

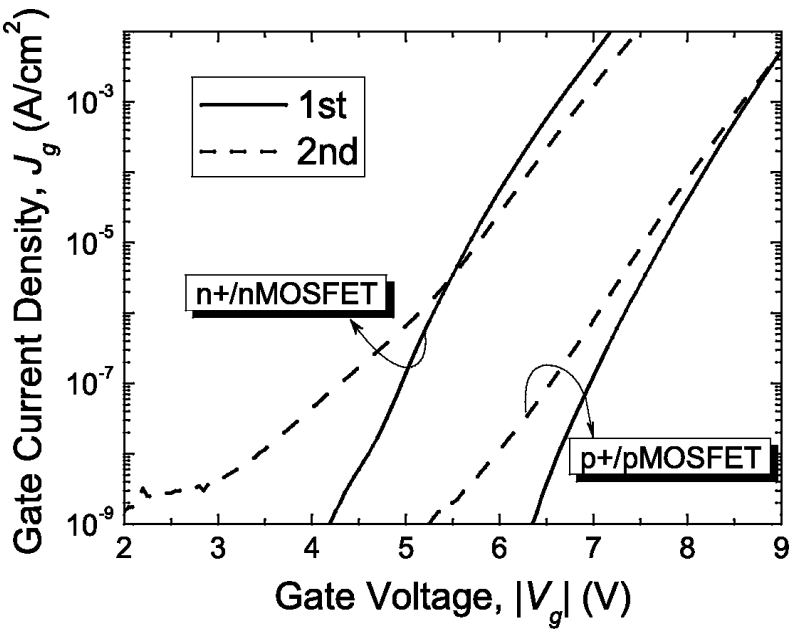

Figure 1.3: SILCs in dual-gate CMOSFETs with 5.9 nm oxide. For each type of device, two J_g-V_g measurements are taken successively, and the excess leakage current appears in the second curve (dashed line). The gate voltage was gradually increased from 0 to as high as 9.0 V (−9.0 V) for n+/nMOSFET (p+/pMOSFET).

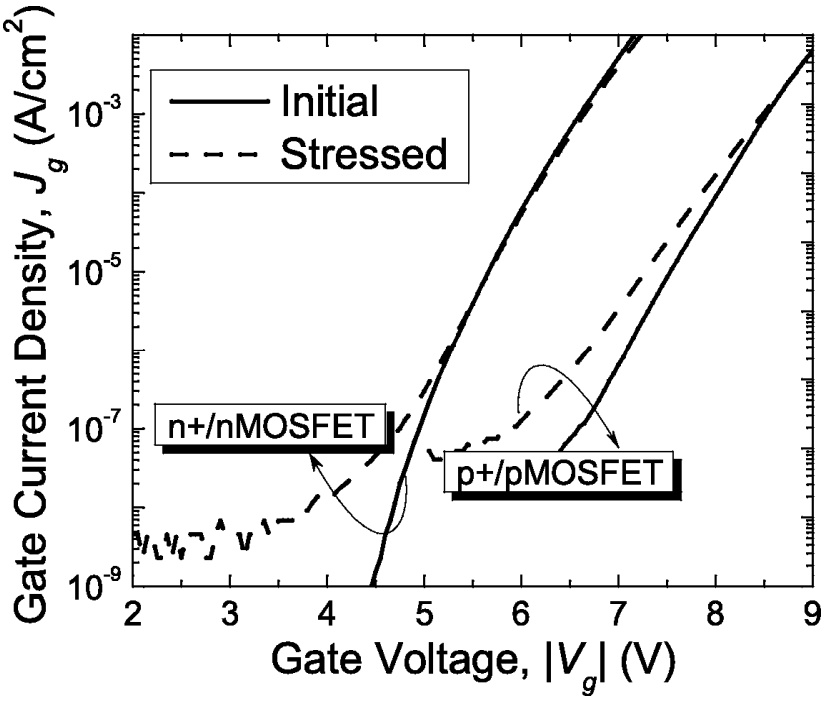

Figure 1.4: SILCs in dual-gate CMOSFETs with 5.9 nm oxide. J_g-V_g measurements are taken before (solid lines) and after (dashed lines) constant voltage stress. The devices are the same as those of Figures 1. The n+/nMOSFET and p+/pMOSFET were stressed at +7 V and −8.5 V respectively, for 100 s.

pre-stress one. This is due to the fact that charge trapped in the oxide lowers the transmission coefficient of tunneling electrons at high voltage [41].

Transient SILCs vs. Steady-state SILCs

SILC is strongly dependent on gate oxide thickness but is rather insensitive to process details. Basically, the components of SILC can be separated into two groups: Transient and steady-state. For oxides thicker than 7.5 nm, transient components tend to dominate the SILC, while steady-state components dominate in thinner oxides [42]. The transient SILC components have been shown to be composed of different sub-components with complex stress/measurement voltage dependence and polarity dependence [43] - [45]. Furthermore, one component can be revealed or concealed by different stress and measurement sequences, and is sensitive to voltage ramp rate [42] [46]. After stress, the current was observed to decay exponentially with time ($J \propto t^{-n}$, with $n \approx 1$) [43], [47] - [49]. This transient behavior originates from charge trapping and detrapping in the oxide [50]. Several models have been proposed to characterize the transient SILCs [51] - [53]. In ultrathin gate oxides, since charge trapping is significantly reduced, transient SILC is practically absent.

Stress Time, Stress Fluence, Temperature and Oxide Thickness Dependence

It has been frequently reported that stress-induced leakage current increases exponentially with stress time, i.e. $J_{\mathrm{SILC}} \propto t_{\mathrm{s}}^{-n}$. The tendency of saturation has been observed at long stress time or large injection fluence at low stress voltages, as well as in small-area devices [54] [55]. In the case of thin oxides, the stress fluence dependence of SILC is similar to the stress time dependence, since the injection charge can be well approximated by an initial injection current multiplied by stress time, i.e. $Q_{\mathrm{inj}} \sim J_0 \cdot t_s$.

The temperature dependence of SILC has been shown to be similar to that for trap creation [56] [57]. SILC, as well as the SILC generation efficiency, increases as the temperature increases.

The oxide thickness dependence of SILC shows a "turn-around" effect. For a fixed stress fluence, SILC increases as oxide thickness decreases and peaks at T_{ox} ~50 Å. Thereafter, SILC decreases as oxide thickness decreases below 50 Å [58] [59]. This "turnaround" effect can be explained by the trap-assisted tunneling (TAT) framework [59] [60]. The turn-around effect may be attributed to the increasing significance of direct tunneling current over TAT current in thinner oxides.

Impact of Nitridation on SILC

By virtue of its ability to suppress boron penetration from the p+ gate, and to improve the hot-carrier reliability, the nitrided gate oxide is widely used in state-of-the-art CMOS technologies. The most popular nitridation method for high-quality gate oxide growth is Rapid Thermal Oxidation in an N_2O ambient [61]. Apart from the well-known advantages that make nitrided oxide a more superior gate dielectric, it has also been reported that nitrided oxide exhibits a greater immunity to SILC generation, as compared to traditional silicon dioxide [62] - [64]. It is believed that the incorporated nitrogen decreases the trap generation rate and density of weak spots [63].

1.3.2. Major Physical Models of SILC

As indicated in the previous sections, SILC is far more than a simple physical phenomenon. In the past two decades, a lot of experimental and theoretical research works have been carried out. Generally, four groups of SILC models can be found in the literature: Charge-Assisted Tunneling (CAT) model [39] [65] [66], Thermally-Assisted Tunneling (THAT) model [56], Trap-Assisted Tunneling (TAT) model [42] [47] [57] [67], and Trap-Assisted Tunneling and Recombination model (TATR) [68] - [70]. The schematic diagrams in Figure 1.5 qualitatively illustrate these four mechanisms. In the CAT model, trapped holes modify the tunneling barrier profile, making it more favorable for electron tunneling. In the THAT model, excess leakage current originates from localized weak spots generated by high-field stress.

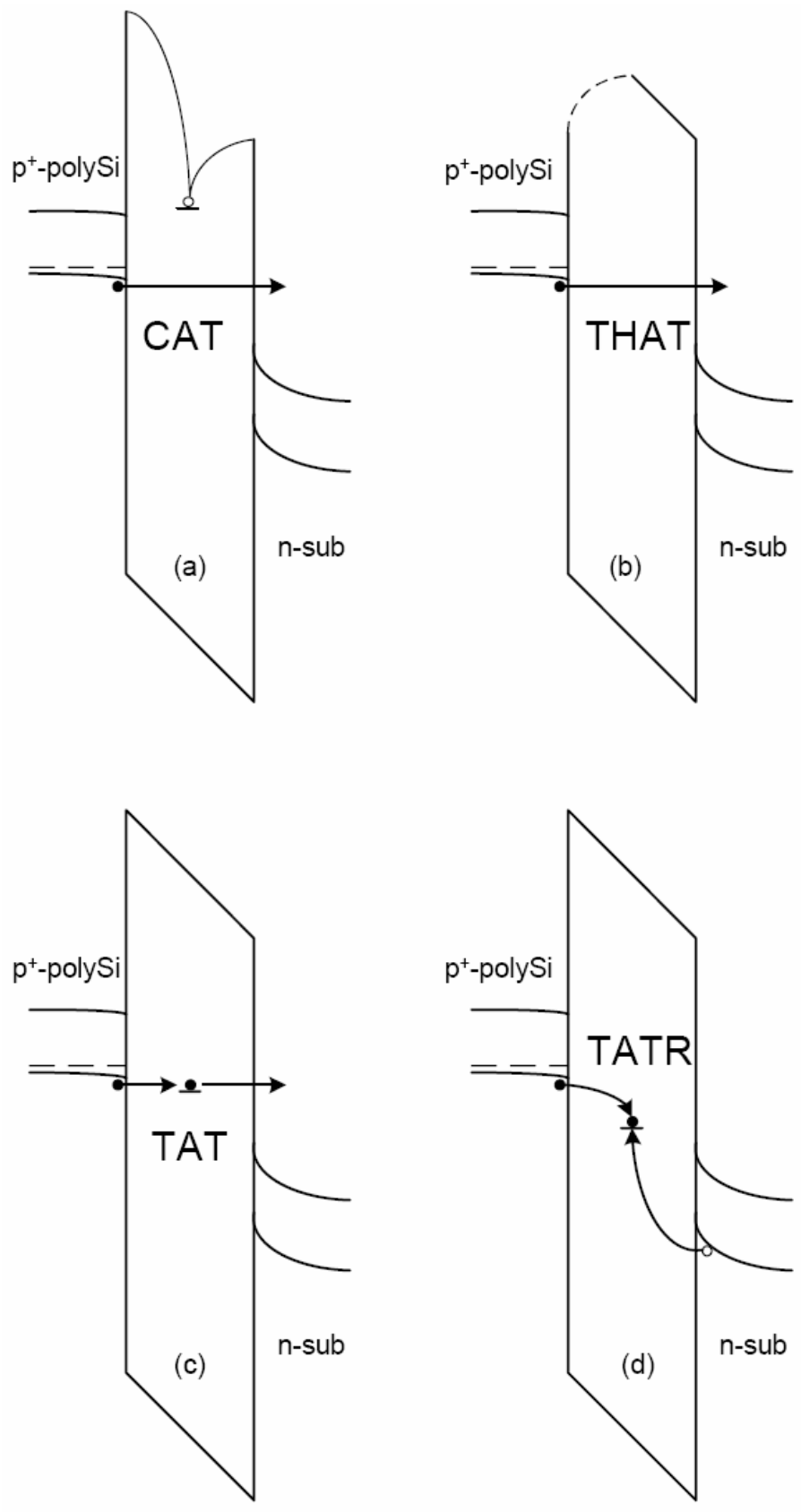

Figure 1.5: Schematic diagrams illustrating four typical tunneling mechanisms that have proposed to explain the SILC.

In the TAT model, oxide traps act as the stepping-stones for excess carrier tunneling. While in the RAT model, the traps act as recombination centers. In this model, it is proposed that a surface channel p+/pMOS structure, holes in the inversion layer actually do not tunnel through the gate oxide; instead, they are captured by the traps in the gate oxide and subsequently recombine with electrons that tunnel from the gate.

Charge-Assisted Tunneling

The increase of leakage current at low voltage was initially attributed to the generation of positive charges in the oxide. This forms the basis of the charge-assisted tunneling (CAT) model, proposed by Maserjian and Zamani [38]. It is proposed that during FN stress, positive oxide charges are generated near the anode, due to the breaking of strained Si-O-Si bonds by hot electrons in the oxide. The trapped holes modify the tunneling barrier profile, thus increasing the electron tunneling efficiency. This model has not gained much support in the literature, even though it is compatible with the AHI model [65] [66]. Recently, the role of positive trapped charge in the stress-induced leakage current is reinvestigated by some groups [53] [71] [72]. It is claimed that the dominant SILC mechanism is Positive Charge-Assisted Tunneling (PCAT), and the transient effect of SILC can be successfully explained by reduction of PCAT current via positive charge detrapping. Furthermore, it has been found that when oxide thickness reduces from 100 Å to 53 Å, the dominant mechanism changes from PCAT to TAT, which will be discussed in detail later in this section.

Thermal-Assisted Tunneling

Olivo *et al.* [56] investigated the dependence of SILC on stress polarity, oxide thickness and measurement temperatures. The excess leakage is modeled as thermal activated electron tunneling through *localized defect-related weak spots*. This constitutes the so-called Thermally-Assisted Tunneling (THAT) model. Furthermore, it is shown that the observed excess leakage can be well described by an FNT-like tunneling current through a heavily reduced barrier height (~0.9 eV) over a wide range of temperatures. Their work has great impact on those of other groups, even though the so-called THAT model for SILC has been abandoned by most groups nowadays. Further research found that the heavily reduced tunneling barrier height is characteristic of

SILC [58]. One example is shown in Figure 1.6, where both virgin gate current and SILC are replotted based on the FNT model, i.e. $\log(J/E_{ox}^2)$ vs.$1/E_{ox}$. Both virgin gate leakage and SILC characteristics can fit the FNT model well. However, it was shown in [63] that for ultrathin gate oxides the low field SILC does not support the FNT model.

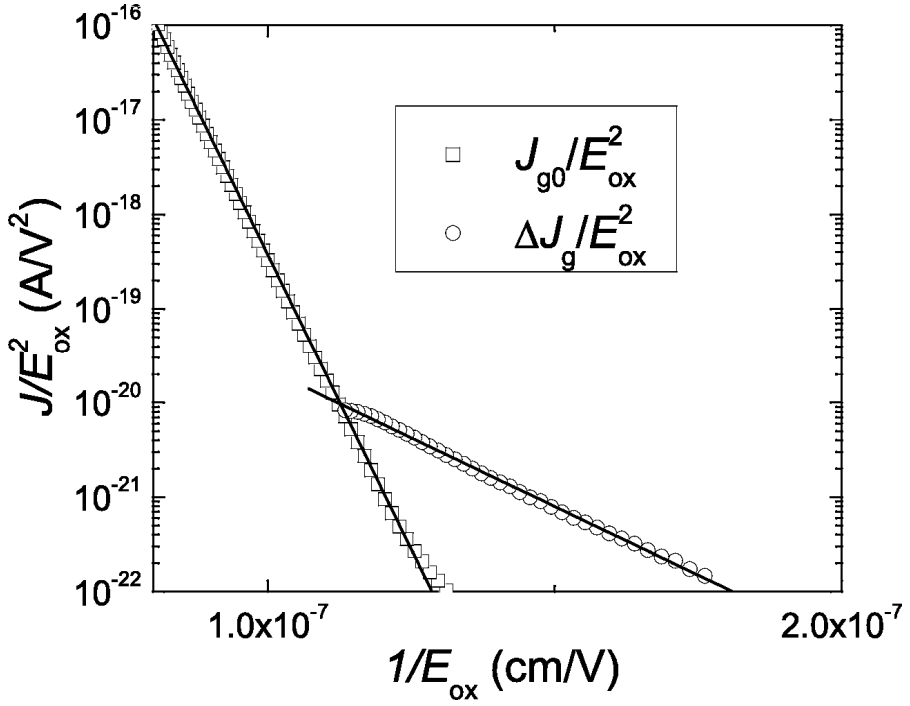

Figure 1.6: FN plots of virgin FNT current and SILC, for an n+/nMOSFET with T_{ox} = 5.9 nm. Device dimensions: W = 20 μm, L = 20 μm, T_{ox} =5.9 nm.

Trap-Assisted Tunneling

The trap-assisted-tunneling (TAT) model became widely accepted in the early 1990s. Actually, the significance of oxide traps in SILC conduction was suggested in late 1980's. Naruke *et al.* [73] investigated the low field excess leakage induced by w/e cycles in FLOTOX EEPROM tunnel oxides with thickness ranging from 40 Å to 100 Å. Consistent with the argument of [56], it was shown that the conduction mechanism of SILC was different from positive charge accumulation in the oxide, since SILC and hole trapping have very different (actually opposite) oxide thickness dependence. However, it seems that the Frenkel-Poole type defect hopping mechanism [74], with a current-field dependence of the form $\log(J/E_{ox}) \propto \sqrt{E_{ox}}$, fits the observed SILC characteristics quite well. A similar behavior was observed by Ann *et al.* [63]. It

should be noted that Frenkel-Poole emission actually can be treated as field-enhanced electron emission from trapping sites [75]. Thus, FP hopping conduction and the TAT mechanism may be largely similar: Low-field conduction in the gate oxides is facilitated by traps, via the formation of intermediate states in the oxide.

Dumin *et al.* [47] quantitatively investigated the relationship between excess leakage current and trap density (N_t). A one-to-one relationship exists between them, strongly suggesting that the conduction of SILC is trap-assisted. Furthermore, the trap density is found to be proportional to the cube root of the injection charge fluence ($N_t \propto Q^{1/3}$) and is independent of the stress polarity. It was observed in [47] that Schottky emission ($\log J \propto \sqrt{V}$), other than Frenkel-Poole emission, also fits the experimental SILC. Patel *et al.* [58] found that there existed a threshold electron energy (~1.7 eV) for the stress voltage, below which no SILC could be observed. It was noted that this threshold value was very close to the trap creation energy in SiO_2 [76].

DiMaria [57] carried out a comprehensive investigation of the dependence of SILC on injected charge fluence, stressing voltage, sensing voltage, oxide thickness, Si-substrate doping, and temperature. SILC was found to exhibit a "universal" dependence on the hot-electron energy. Furthermore, oxide defect generation (trapped holes, trapped electrons, interface states, positive charge trapped near the anode) was investigated as a function of hot-electron energy. By comparing the latter results to the electron energy dependence of SILC, it was concluded that the major cause of SILC was neutral electron traps generated during hot-electron stress.

Other important reports related to the TAT model include [59] [77] - [79]. In [78], and with more detail in [80], experimental evidence is provided showing that trap-assisted tunneling is involved in SILC conduction. During SILC conduction, a "constant energy loss" (~1.5 eV) is verified for electrons injected through the gate oxide into the Si substrate. This is also supported by the simulation results reported by Ghetti *et al.* [81] [82]. Furthermore, it is concluded that process-induced oxide traps and stress-induced oxide traps are essentially different, since tunneling through process-induced oxide traps appears to be elastic [82].

Assuming that the density of process-induced oxide traps is negligible, which is reasonable for state-of-the-art CMOS process, the principles behind the TAT model for

SILC can be summarized below:

1. In post-stress oxide, the leakage current is made up of two parts: Native tunneling leakage current and excess leakage induced by stress. The native leakage can be FNT or DT, while the excess leakage is dominated by TAT.
2. The oxide traps act as stepping-stones for carrier tunneling. Tunneling is facilitated by oxide traps, because their presence substantially lowers the tunneling barrier.
3. TAT is at least a two-step process: A tunneling-in followed by a tunneling-out process.
4. Carriers lose energy when they tunnel through the gate oxide via TAT, i.e. the tunneling is inelastic.
5. Traps involved in TAT are believed to change their states after the TAT process, to compensate the energy loss stated above. The exact mechanism of this change is still not clear.

Based the TAT framework, many successful SILC models have been proposed [51], [83] - [88]. However, there are still uncertainties. The most controversial ones are those concerning the spatial and energy profile of stress-induced oxide traps. For example, it is still not clear whether interface traps or bulk traps, or both, are involved in the TAT process. As early as 1991, Rofan and Hu [67] proposed that SILC was a result of trap-assisted tunneling via interface traps, and this argument was supported by the fact that there was a close correlation between SILC and interface traps sensed by charge pumping current measurement for three cases: Pre-stress, post-stress, and post-stress anneal. This argument was also supported and developed by other groups [64] [89].

It has been reported that high-field generated interface states and oxide traps are actually correlated. From this point of view, the observation that SILC is well correlated to interface trap density is therefore not enough to prove that SILC conduction is dominated by interface-trap assisted tunneling. A similar conclusion applies to bulk oxide traps. Practically, it is sometimes difficult to clearly distinguish interface traps from oxide traps, especially for ultra-thin gate oxides. As gate oxide thickness approaches the critical dimension of a single electron trap, the debate on interface- or bulk-trap assisted tunneling may not be meaningful.

Recombination and Trap-Assisted Tunneling

Although the TAT model has gained great success and wide support in the past years, it has been challenged recently. The lack of direct evidence or detailed knowledge on the TAT process that happens at the oxide traps is the major short-coming for TAT-based models.

Ielmini *et al.* presented a novel model for SILC, which incorporated recombination into the TAT process, namely the recombination and trap-assisted tunneling (RTAT) model [68] - [70]. In this model, the simultaneous observation of hole current and electron current in SILC is attributed to electron-hole recombination at defect states in the oxide (Figure 1.5-d). It was shown that these two components in SILC are highly (almost one-to-one) correlated, in that they share the same stress dose dependence and relaxation time dependence [69]. Specifically, plotting hole SILC vs. electron SILC at different stress levels or relaxation time (after the stress) on log-log scale results in a straight line with slope very close to 1; wherever electron SILC is suppressed, e.g. in p+/pMOS devices, hole SILC is also suppressed.

1.3.3. Stress-Induced Traps in Oxides

The strong correlation between SILC and trap generation has been demonstrated by many SILC models. The properties of the stress-induced oxide traps, the density of the traps, and the energy distribution of the traps are the factors that would most significantly influence SILC. But, how exactly an oxide trap facilitates carrier tunneling is still not clear till these days. The traditional methods for extracting trap density have their limitations. A good understanding on the energy distribution of the traps is lacking either. Specifically, a detailed knowledge of the energy distribution of stress-induced oxide traps is not available.

In the literature, several techniques have been used to measure the trap density. For example, the density of interface states was often measured by the charge pumping technique [64] [67]. The density of bulk oxide traps can be obtained from the discharge current characteristic after removal of high voltage pulse [47] or from the

C-V and I-t characteristics [17]. More recently, a novel method, termed Direct-Current Current-Voltage (DCIV), was used to monitor both the bulk oxide traps and SiO_2/Si interface states [89] [90]. However, it should be noted that all these methods can only sense a portion of the interface/bulk oxide traps. In other words, only the relative change in the trap density can be monitored, not the absolute change.

In order to characterize SILC accurately, the oxide trap distribution must also be known precisely. This includes the spatial and energy profiles of the traps. However, due to lack of insight into the microstructure, a detailed knowledge of the energy profile of the stress-induced oxide traps has never been obtained. A common practice in the literature of SILC modeling is to first introduce the energy level of the traps as a parameter, and later extract an improved value by fitting the SILC model to experimental data [91]. Spinelli *et al.* reported an experimental method to extract the energy distribution of oxide traps [92]. However, this method is not applicable to ultrathin gate oxides, since it makes use of the transient current as the monitor of trap density. In ultrathin gate oxides, the transient current is too small to be a sensitive monitor.

It is still not clear whether the electrical stress-induced oxide damage is localized or is uniformly distributed throughout the gate oxide. In the literature, some group adopted the concept that stress-induced damage is localized [93] on the basis that oxide breakdown (SBD or HBD) is highly localized [13]. However, in using the TAT model, the assumption of a uniform oxide trap distribution is found to fit the experimental SILC data very well [50] [86], indicating that oxide traps responsible for SILC may not be necessarily localized. This challenges the argument that SILC and oxide breakdown are well correlated. Furthermore, some groups postulated that the traps responsible for SILC are different from those responsible for oxide breakdown [94]. In recent years, new experimental findings have shown that there are at least two types of oxide traps created during electrical stress [95] [96]. This casts more doubts on the proposed strong correlation between SILC and oxide breakdown. However, as suggested in [94], and also in [97], the correlation between SILC and oxide breakdown could be indirect. Further research work is needed to clarify their relationship.

1.3.4. Recent Advances in Research

The number of publications on SILC is huge, and recent research work has become more detailed. Chetti *et al.* [82] investigated the physical characteristics of electrical stress-induced traps by quantum yield measurement and simulation [82], and they showed that electron tunneling via stress-induced traps is inelastic, consistent with [80]. Furthermore, it has been shown that electron tunneling via pre-existing traps is elastic. This indicates that pre-existing traps and stress-induced traps are different in nature, which is also shown recently in [98].

Ang *et al.* [99] found that SILC could be annealed out partially by applying a low voltage after high voltage stress, and proposed that the reduction in SILC was linked to annealing of trapped holes. The mechanism of SILC and dielectric breakdown was examined by Alers *et al.* [100] through 1/f noise in the tunneling current of 1.7 - 5 nm oxides. Before breakdown, a linear relationship between SILC and 1/f noise was observed. This behavior was successfully described using the TAT model. A new quantitative model was developed for the 1/f noise, on the basis of TAT current fluctuations. It was shown that the traditional charge-state fluctuation model is inconsistent with the voltage-scaling of the noise. These results also strongly suggest that the conduction mechanisms in the stressed and unstressed oxides are fundamentally different.

Irrera proposed a kinetic model for trap creation in thermal oxides during electrical stress [101]. In this model, creation of additional traps is believed to be controlled by electron scattering by existing defects. The model predicts a square-root dependence of SILC on the stress time. Defect concentrations calculated by this model were used in a TAT model and excellent agreement with low-field conductivity was observed.

Ielmini *et al.* presented a detailed investigation based on Quantum Yield (QY) experiments [102]. Experimental data show that no correlation exists between QY and SILC, and that QY is determined by high-energy oxide traps. Numerical simulation was used, based on a detailed calculation of the oxide defect distribution. It is shown that the leakage current and the excess impact ionization component are due to TAT of electrons through different sets of traps: Deep level traps are responsible for SILC,

while high-energy states determine the impact ionization current. Simulation results were in good agreement with experiments, showing that QY results could not be used to extract the energy loss of the SILC electrons.

Wu *et al.* investigated the validity of SILC as a measure for the critical defect density (N_{BD}) that triggered breakdown [103]. Their finding shows that SILC may not serve as a reliable measure for $N_{BD.}$ This work suggests that a re-evaluation of the breakdown models constructed from SILC-based experiments is required, in particular, their validity in comparison to the statistically accurate breakdown data.

The relation between SILC and hydrogen release (HR) was analyzed by Esseni *et al.* for both channel hot electron (CHE) [104] and FN [105] stress. From the fact that no deuterium isotope effect was observed for SILC, they concluded that there was no causal relation between SILC generation and HR, regardless of whether the SILC was generated by CHE stress or FN stress. In contrast, it was shown that the AHI mechanism is operative even at low gate voltage [106].

Chim *et al.* investigated the SILC generated by impulse stress [107]. An abnormally high density of positive trapped charges was observed in oxides as thin as 4.3 nm. Furthermore, it was found that the transient SILC is larger than steady-state SILC, contrary to observations in DC-stressed thin oxides [42]. These two observations, i.e. abnormally high density of positive trapped charges and large transient SILC, were found to be correlated. Another article by the same team [108] presents a detailed investigation on the SILC conduction mechanism via Conduction Band Electron (CBE) and Valence-Band Electron (VBE) tunneling in thin oxides. An improved SILC model is proposed, which enables reproduction of the experimental SILC over a wide range of oxide field, and extraction of a realistic neutral trap concentration. This improved model also confirms the concept that SILC conduction via neutral traps is accompanied by energy loss. Furthermore, the energy loss is found to be dependent on the origin of tunneling species: ~1.5 eV for CBE, and ~0.8 eV for VBE.

Research on the impact of SILC on Flash memories has been greatly advanced by Ielmini *et al.* In [109], they reported a new experimental technique to evaluate the position of oxide weak spots responsible for SILC in Flash memories. In their report, the position of the leakage spot is determined by the shift in the gate current-voltage (I-V) characteristics, when the oxide field along the channel is modified by varying the

drain bias. Results reveal a strong localization of SILC near the drain junction, as a result of program/erase operations. A statistical model of SILC in Flash arrays is presented in [110], featuring that tunneling assisted by two traps (2TAT) [111] [112], rather than the traditional single-defect TAT, dominates the steady-state SILC in Flash arrays with oxide thickness in the range of 6.5 nm to 9.7 nm. Some recent progress on SILC in nonvolatile memory devices can also be found in [113] [114].

A good understanding of SILC has led to several applications in the characterization of gate oxide reliability and lifetime. SILC increase has been successfully used to predict the lifetime of ultrathin gate oxides by Nigam *et al.* in [115], and the method is found to be fast and simple. However, it should be noted that the measured oxide lifetime is not necessarily associated with breakdown. In some cases, the increase in gate leakage could already limit circuit functionality.

1.4 SILC and Oxide Degradation in Scaled Oxides

As gate oxide thickness scales down, the gate leakage current increases exponentially. The large direct tunneling leakage current has become a major reliability problem for ULSI, and it is believed to be the "show-stopper" of ULSI applications based on the silicon dioxide. Due to the predominance of direct tunneling current, SILC in ultrathin gate oxides is significantly different from that in thick oxides. For thick oxides, at very low voltage regime where initial leakage current is usually not detectable, SILC shows up as obvious increase in the leakage current after high-voltage stress. Instead, the increase in the leakage current is gradual and progressive in the case of ultrathin gate oxides, because the high DT current usually concealed SILC. An example is shown in Figure 1.7. In this figure, the data are obtained for an n+ poly-gated nMOSFET with 2.2 nm gate oxide. The currents have been normalized to the gate area. The pre-stress and post-stress J_g-V_g characteristics are shown for both gate voltage polarities. We can see that the direct tunneling current constitutes a major part of the overall post-stress leakage current.

The dominant direct-tunneling current in ultrathin gate oxide at low voltage implies that different current conduction and degradation mechanism may exist. Takagi

et al. [116] experimentally examined the DT current in unstressed and stressed ultrathin oxides in n+-poly/pMOS devices, and found that a leakage path allowing the flow of holes dominates SILC and overall leakage current after oxide soft-breakdown. This is also confirmed later by H. Guan *et al.* [117]. In [116], it is suggested that leakage paths different from those responsible for TAT are formed inside the SiO_2 layer after stress, and these paths lead to a dominant hole current and SB of the oxide. This implies the possibility that for direct-tunneling oxides, SILC is dominated by hole current, even though it has never been explicitly pointed out yet.

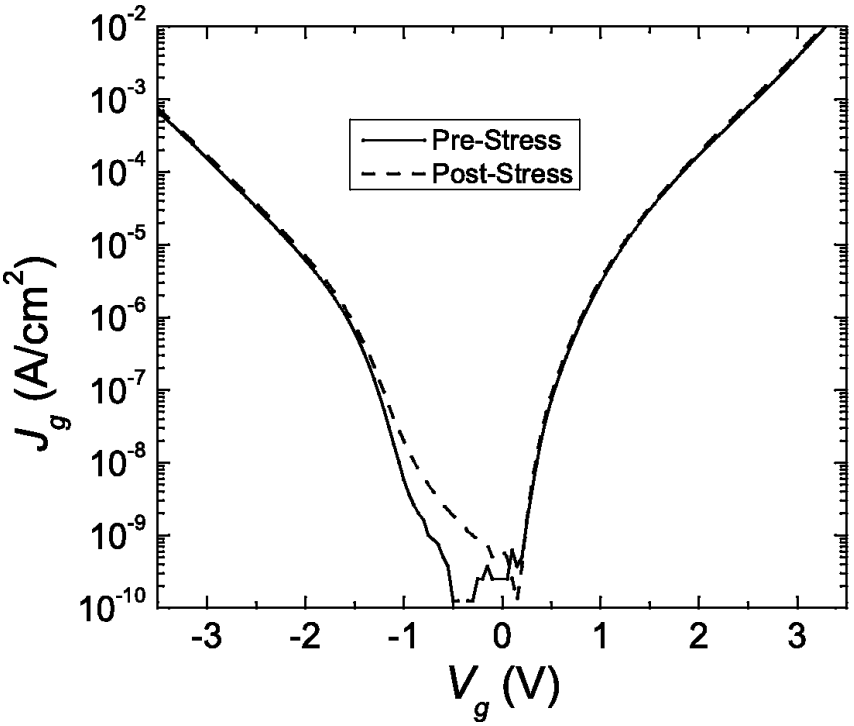

Figure 1.7: J_g-V_g characteristics of an n+/nMOSFET. The *s*olid and dashed lines denote the pre-stress and post-stress characteristics respectively. The gate voltage was swept from negative to positive during measurement. Device dimensions: T_{ox} = 2.2 nm, W = 40 μm, L = 20 μm.

Recently, research on low-voltage SILC (LV-SILC) in ultrathin gate oxides reveals a scenario that is rather different from high-voltage SILC (HV-SILC). This includes the possible sense-voltage dependent SILC mechanism [122] and possible interfacial trap-rated tunneling [122] - [124]. Even though controversy remains [125] [126], these reports demonstrate the possibility that LV-SILC can be an alternative degradation monitor of ultrathin gate oxides, when traditional methods, such as C-V and

charge-pumping, are no longer applicable.

1.5 Motivation of This Work

As has been shown previously, SILC in thick oxides (>3 nm) has been comprehensively investigated, and it has generally been accepted that TAT dominates the SILC conduction. For ultrathin gate oxides, SILC usually is not quantitatively significant compared to the initial DT current. However, this does not mean that SILC in ultrathin gate oxides is not important. It is to be noted that even after more than 30 years of research, the degradation of oxide films under electrical stress is still not completely understood. SILC in ultrathin gate oxides, even though usually concealed by large DT current, may still be a very good indicator of oxide degradation. As a piece of evidence, LV-SILC has been used as monitor of oxide degradation in [125] and [126].

For ultrathin gate oxide case, probably TAT is still the most possible mechanism responsible for SILC [122] - [126]. However, several pieces of information are still missing for better understanding of SILC in ultrathin gate oxides, especially for dual-gate CMOS devices.

1. In p+/pMOSFETs, it is known that the low voltage DT leakage is dominated by hole current. However, it is not clear the significance of hole current in SILC, and how it evolutes during electrical stress. This can be of great importance because it is possible to figure out the distribution of oxide traps responsible for SILC from the evolution of hole SILC and electron SILC [68] - [70].
2. As indicated in the polarity dependence of oxide breakdown [21] - [23], the manner of current injection has different oxide degradation rate. However, it is not clear how the manner of current injection will impact the evolution of hole SILC and electron SILC.
3. It is still not clear whether there is a common scheme, in terms of stress-induced trap generation and distribution, to explain the evolution of hole SILC and electron SILC in both p+/pMOSFET and n+/nMOSFET.

This work demonstrates an attempt to give an illustration of the evolution of hole SILC and electron SILC in dual-gate CMOSFETs with ultrathin gate oxides. Both type of devices (n+/nMOS and p+/pMOS), both stress polarities (inversion and accumulation), and both types of sense voltages (positive and negative) will be considered, to obtain better understanding of the SILC in different type of devices and generated/measured by different conditions.

1.6 Organization of the Thesis

This thesis consists of 6 chapters. Chapter 1 is the introduction chapter, which gives a comprehensive literature survey research on SILC. Chapter 2 provides detailed information about the test vehicles and experimental setup used in this work, as well as the data analysis technique. In Chapter 3, the SILC characteristics of ultrathin gate p+/pMOSFETs, subjected to different stress conditions, are discussed. Chapter 4 presents the SILC characteristics of the n+/nMOSFETs. In Chapter 5, we correlate our experimental SILC data to the defect generation mechanisms proposed for ultrathin gate oxides. Finally, Chapter 6 summarizes the major findings of this research project and makes suitable recommendations for future work.

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Chapter 2

Experimental Techniques

2.1 Device Information

Conventional dual-gate MOS devices were fabricated by state-of-art commercial CMOS technologies. These include nMOSFETs with n+-polysilicon gate (denoted as n+/nMOSFETs) and pMOSFETs with p+-polysilicon gate (denoted as p+/pMOSFETs).

After n-channel implant, gate oxides were grown by partial wet oxidation in 850 °C, and etched into several desired thicknesses. These oxides were nitrided by rapid annealing in an N_2O ambient. Devices with gate oxide thickness ranging from 1.7 nm to 5.9 nm and various gate areas (20×1 μm^2, 20×20 μm^2, 40×20 μm^2) were available. Polysilicon gates were deposited and doped after gate oxide nitridation. Our focus is on devices with thin oxides, and those with thick oxides are only for purpose of comparative study.

2.2 Major Experimental Procedures

In order to investigate the dependence of SILC on stress time, stress fluence, and stress voltage, devices were stressed under various stress voltages, with the stress cycle periodically interrupted to measure the gate leakage characteristics at lower voltages. Thus, a stress/measurement cycling procedure was needed, which is shown in Figure 2.1. This cycling procedure was specially designed for computer-controlled experiments for the characterization of SILC. It ensured that, after each stress, the device *J-V* characteristics were obtained and thus the effect of that duration of stress was

recorded for future analysis. The cycle was repeated until the cumulative stress time exceeded 10^5 s or the oxide broke down (can be soft breakdown or hard breakdown). The maximum gate voltage used in carrier separation measurement was at least 1 V smaller than the stress voltage, ensuring that negligible additional degradation was induced by the measurement steps. This procedure was controlled by a computer program [1] [2]. The time interval between the end of a stressing step and the beginning of the measurement step was about 10 seconds. This was the time needed for the computer program to extract data from the measurement instruments and to configure the next measurement step. Because charge trapping in such thin oxides was negligible for ultrathin gate oxides, transient currents could be safely neglected. Thus, the SILC obtained in this way is a steady-state current.

A stress-time array was used to control the period of each stress cycle. The validity of this procedure was confirmed from observation of the steady and progressive oxide degradation.

A schematic diagram of the experimental setup is shown in Figure 2.2. The source, drain and substrate terminals of the MOSFET were grounded. Stressing and measurement were carried out using the HP 4156A semiconductor parameter analyzer. Triaxial connections were used for optimum low-leakage current measurement. The device under test was situated in an enclosed chamber, evacuated down to a pressure of ~5 mTorr. This experiment configuration enabled accurate measurement of current as low as 1 fA, with high stability and reproducibility.

2.2.1 Carrier Separation Technique

The application of the carrier separation technique in investigating carrier conduction in insulators dates back to the 1970s [3]. In the past years, this technique has been successfully used to characterize the quantum yield of energetic electrons tunneling from the gate of nMOSFET [4]. For MOS devices with ultrathin gate oxides, in which significant direct tunneling happens at very low voltages, the carrier separation technique can be used to distinguish the electron and hole tunneling current components in the overall gate leakage [5].

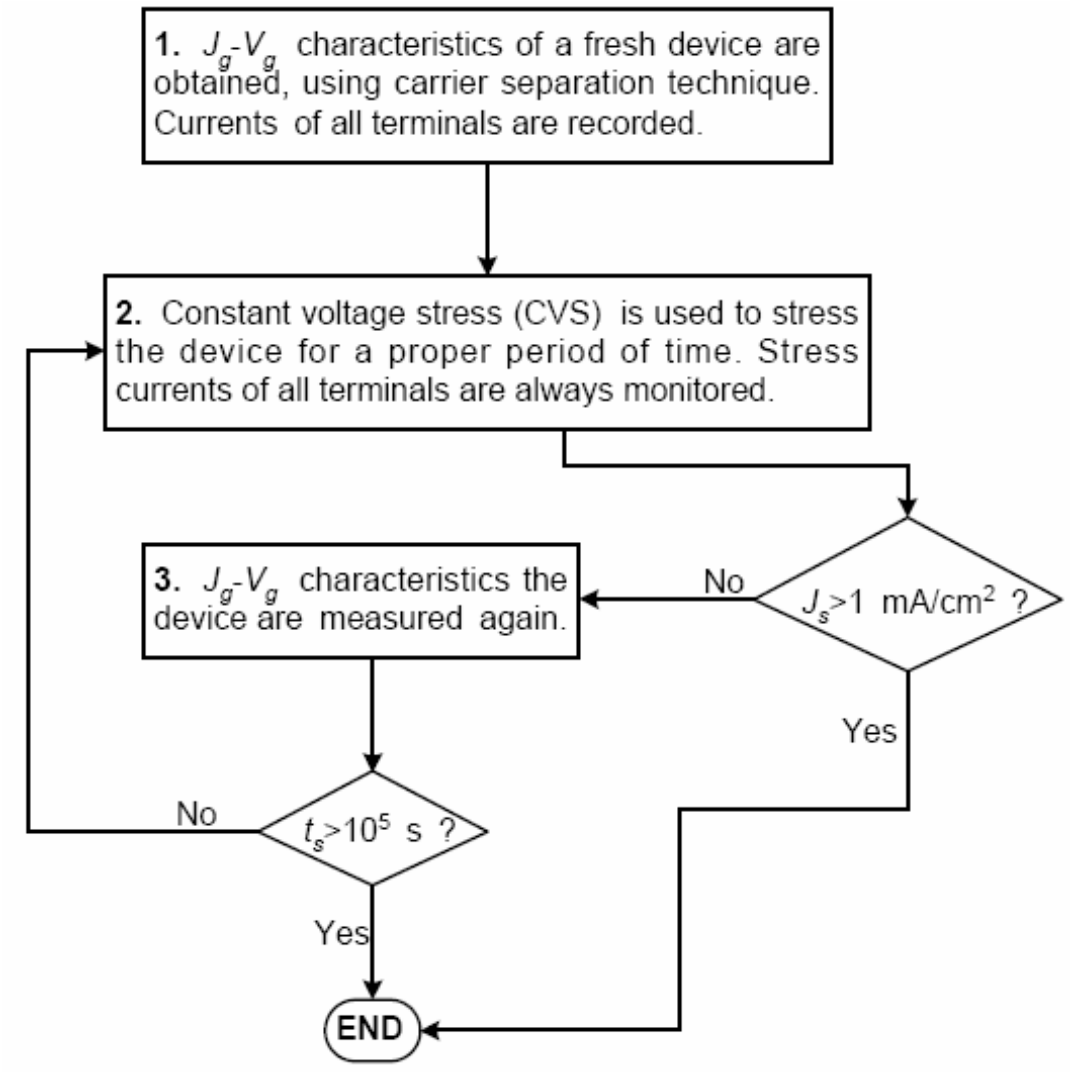

Figure 2.1: A CVS/measurement procedure for characterizing the SILC in ultrathin gate oxides. Note that t_s stands for cumulative stress time and J_s stands for the gate current measured during the stress.

The experimental setup for the carrier separation technique is shown in Figure 2.2. When a negative bias is applied to the gate of the p+/pMOSFET, an inversion layer is formed at the Si-SiO_2 interface. Hole tunneling from the inversion layer to the gate dominates the leakage current at low voltage (-1.5 V$< V_g < 0$), for electron tunneling from the gate valence band to substrate is inhibited due to unavailability of empty states in the band gap [6]. As the gate voltage increases, electron tunneling from the gate also contributes to the gate leakage current and gradually dominates over hole tunneling. The grounded p+ source/drain supply the holes (J_{sd}) needed tunneling to the gate. Electrons that tunnel from the gate are collected as the substrate current (J_{sub}).

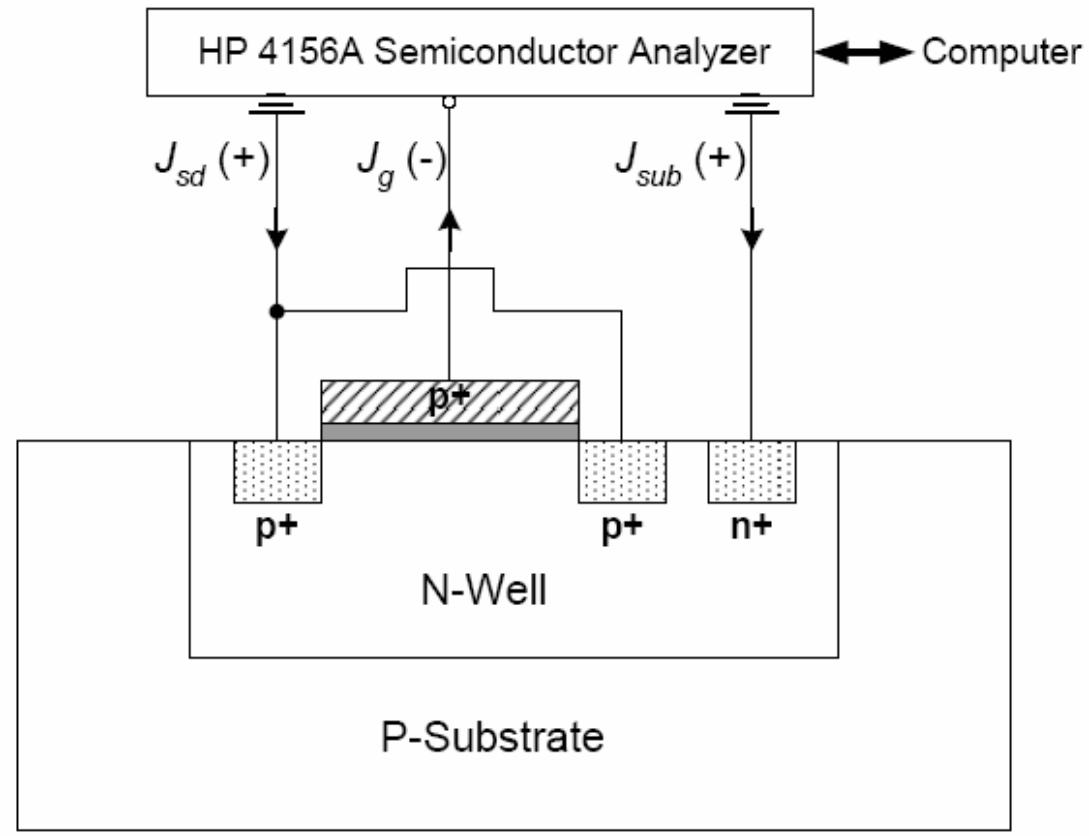

Figure 2.2: A schematic diagram of the experimental configuration used for both constant voltage stress and carrier separation measurement, for a p+/pMOSFET. The cycling procedure is controlled by a computer. In this thesis, currents following into the transistor are always defined as positive, while those flowing out of the transistor are defined as negative.

The experimental configuration shown in Figure 2.2 can also be applied to the n+/nMOSFET. When the channel is biased in inversion, electrons tunnel from the substrate conduction band to the gate. These electrons are provided by the grounded n+ source and drain (J_{sd}). Electrons also tunnel from the substrate valence band and holes left behind are collected as substrate current (J_{sub}). However, within the voltage window of our interest, J_{sub} is only a minor part compared to J_{sd}, and can be safely neglected in total gate leakage current [6].

In Figure 2.3 to Figure 2.6, the carrier separation measurement results of four situations are shown, together with the corresponding energy band diagrams: p+/pMOSFET in inversion, p+/pMOSFET in accumulation, n+/nMOSFET in inversion, and n+/nMOSFET in accumulation.

It should be pointed out that carriers in the gate leakage current can be nicely

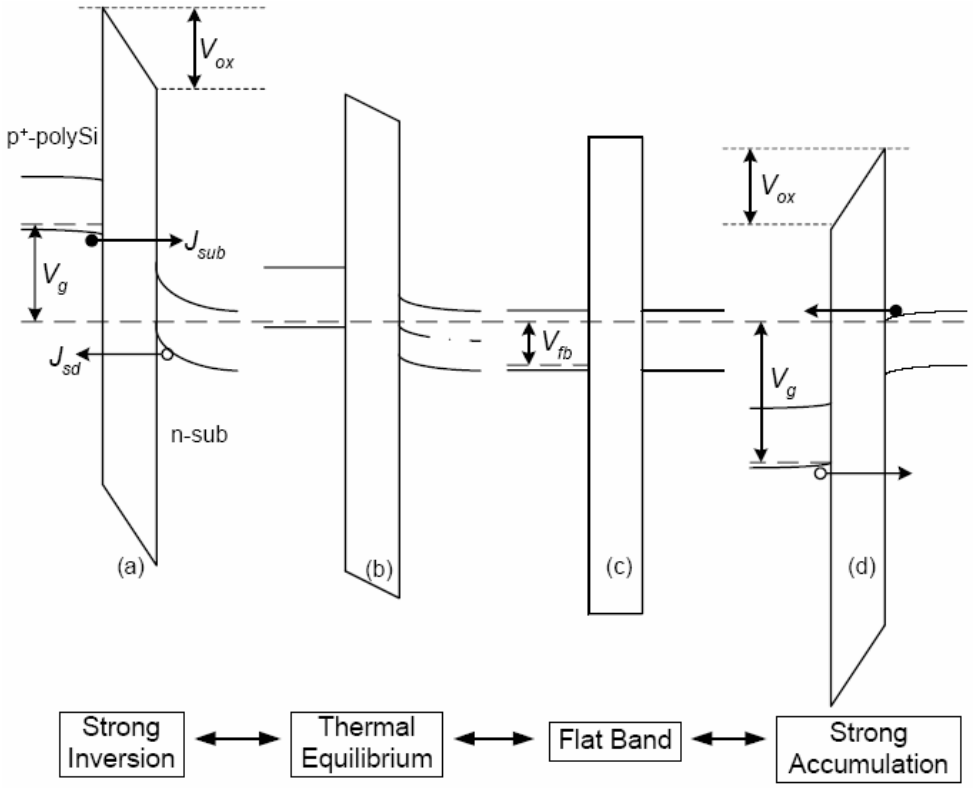

Figure 2.3: Energy band diagrams illustrating the p+/pMOSFET transiting from strong inversion to thermal equilibrium, to flat-band, and to strong accumulation.

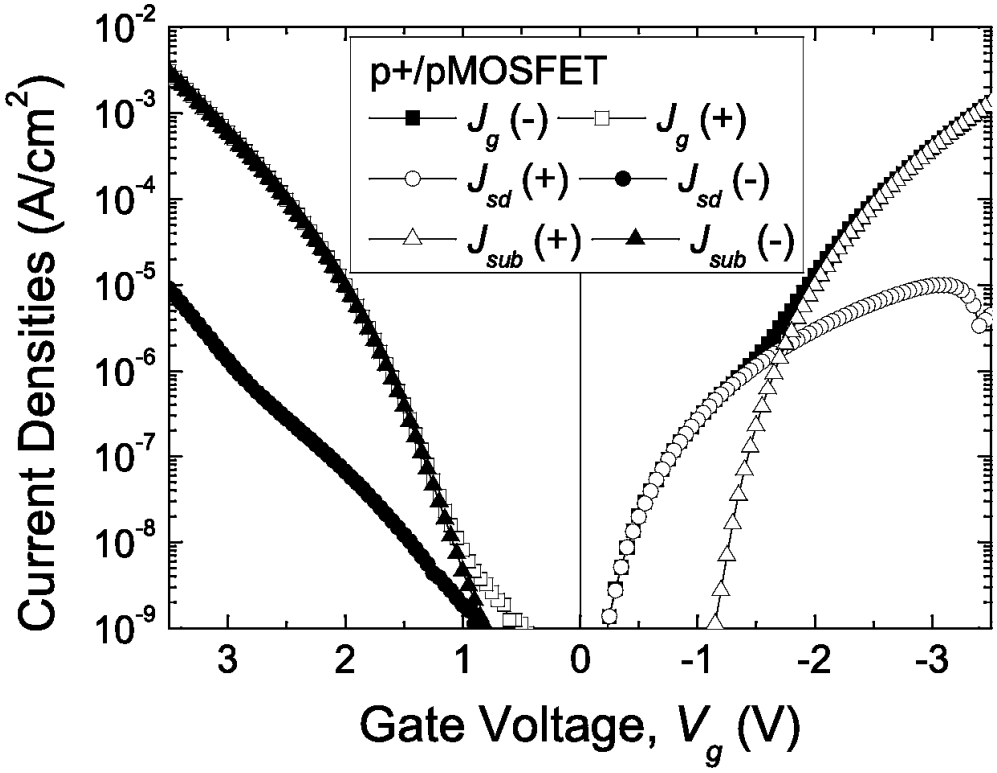

Figure 2.4: Carrier separation measurement results of a p+/pMOSFET. Solid and open symbols denote positive and negative current, respectively. Device dimensions: T_{ox} = 2.2 nm, W = 40 μm, L = 20 μm.

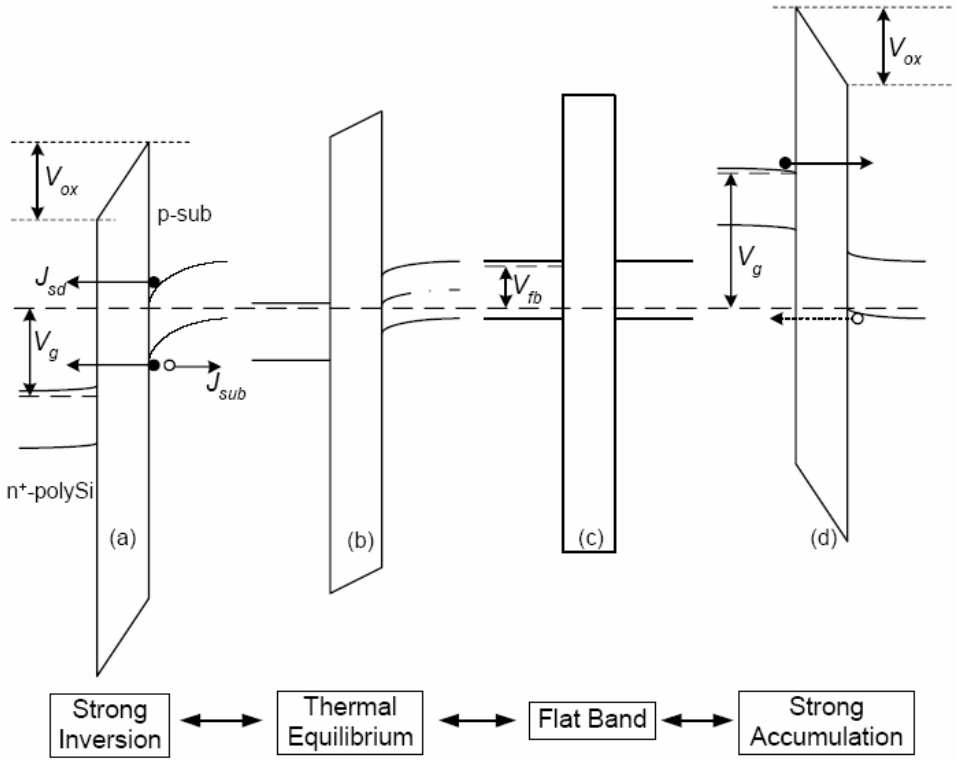

Figure 2.5: Energy diagrams illustrating the n+/nMOSFET transiting from strong inversion to thermal equilibrium, to flat-band, and to strong accumulation.

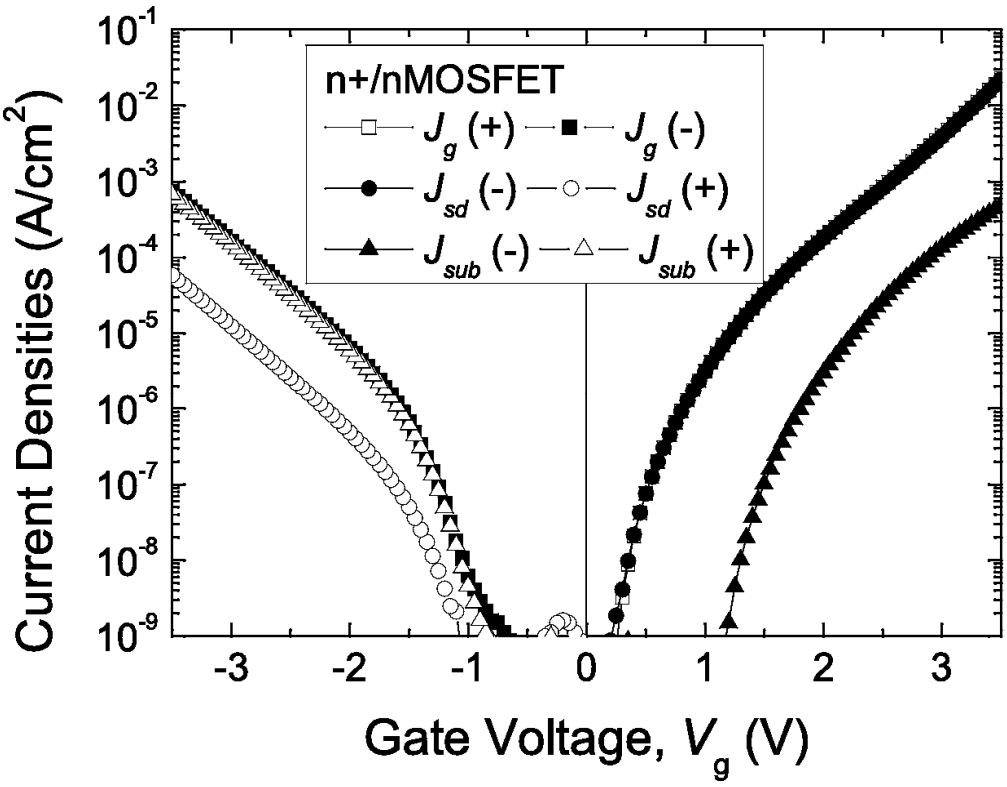

Figure 2.6: Carrier separation measurement results of an n+/nMOSFET. Solid and open symbols denote positive and negative current, respectively. Device dimensions: T_{ox} = 2.2 nm, W = 40 μm, L = 20 μm.

separated only when an inversion layer exists in the channel. When the channel is biased in accumulation, carriers injected from the gate become the minority carriers when they enter the substrate, and some of them are annihilated through recombination with the majority carriers in the substrate. This recombination effect is more severe in MOSFET with longer channel. Since this part of recombination current is not easy to be quantified, the "carrier separation" curves in the channel accumulation regime are shown for qualitative comparison only.

After a certain amount of charges has been injected into the gate oxide (either by CVS or SHCI), oxide properties are degraded. The degradation can be visualized from the shifts of the gate leakage current and it components. By comparing the carrier separation measurement results before and after the stress, not only the gate current change (gate SILC) but also the changes in the respective current components (electron SILC and hole SILC) can be revealed. These changes may convey important information on SILC generation and SILC conduction, as well as trap generation [7] [8].

2.2.2 Constant Voltage Stress

Constant voltage stress is used to generate SILC for most cases of this work. In CVS configuration, the source, drain and substrate are grounded, as shown in Figure 2.2. The stress voltage is applied to the gate. In order to investigate stress magnitude and polarity dependence of SILC, the magnitude of the stress voltage (V_s) is varied, but always ensuring that the magnitude of the stress voltage does not exceed 5 V. This is to avoid early oxide breakdown because it was found that the breakdown voltage (during a ramp-voltage test) of 2.2 nm gate oxides used in our work is only about 5.5 volts. Within the voltage region of V_g<5 V, the carrier transport in the thin oxide can be treated as ballistic [7].

2.2.3 Substrate Hot Carrier Injection

The MOSFETs are also stressed using the substrate hot carrier injection (SHCI) technique [5]. Making use of the vertical NPN or PNP bipolar transistor, during SHCI stress, primarily only the minority carriers is injected into the gate oxide, while the injection of majority carriers is strongly suppressed. Thus, SHCI provides a useful means to investigate oxide degradation due to the injection of one carrier type. Depending on the type of device, substrate hot-electron injection (SHEI) and substrate hot-hole injection (SHHI) stress are performed on nMOSFETs and pMOSFETs, respectively.

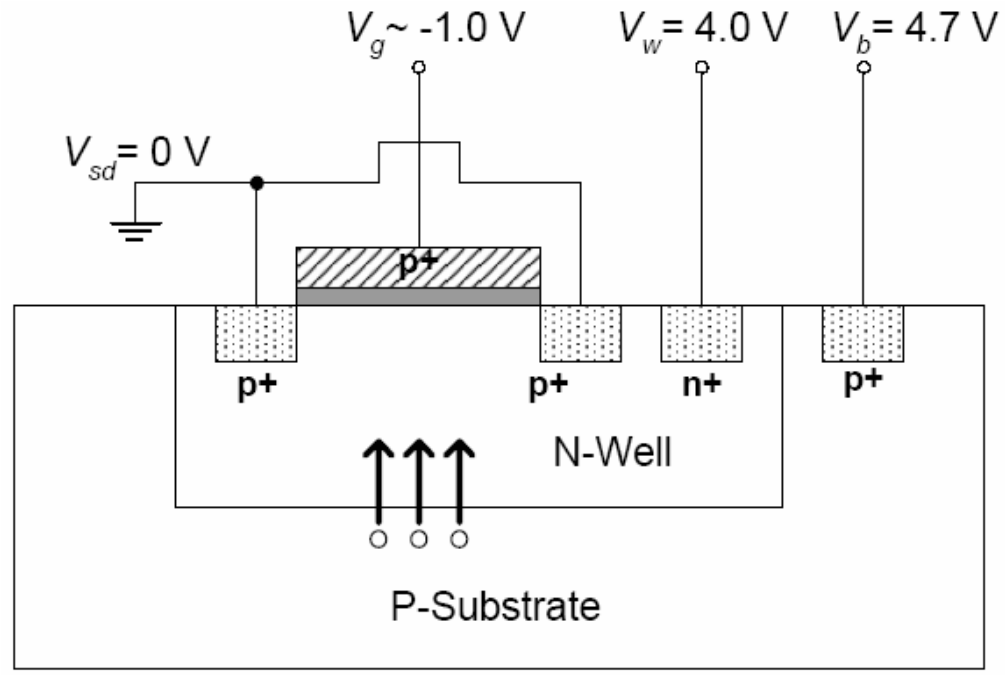

Figure 2.7: Schematic illustration of substrate hot-hole injection. The source and drain are grounded. Both n-well and p-substrate are biased at high positive voltage (V_w and V_b respectively), with the latter 0.7 V higher than the former.

A schematic diagram of SHHI is shown in Figure 2.7. A low negative voltage is applied to the gate, ensuring the substrate surface is strongly inverted but the oxide field is not high enough to induce measurable degradation. A relatively high positive bias is applied to the n-well, and an even higher positive bias is applied to the substrate, maintaining a constant 0.7 V difference between the base and emitter. Holes are injected from the positive-biased PN junction formed by the p-substrate and the n-well,

and accelerated in the depletion region formed by the positive n-well bias. Finally, part of these holes are injected into the gate oxide and collected as gate current. The grounded source/drain serves as a hole "sink". The degradation of gate oxides is purely induced by the injected holes. The n-well bias determines the energy and therefore the degradation efficiency of the injected holes.

2.3 Summary

Major process and dimension parameters of the devices used in this work are listed in this chapter. Detail is given for the main experimental techniques and procedures, including carrier separation measurement, constant voltage stress and substrate hot carrier injection. These techniques ensure a systematic study of SILC in ultrathin gate oxides with good stability and reproducibility.

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Chapter 3

SILC in p+/pMOSFETs with Ultrathin Nitrided Gate Oxides

3.1 Introduction

In modern polysilicon-based CMOSFET applications, a dual-gate configuration is commonly used. In this configuration, n+ poly-gate is used for nMOSFET, and p+-poly gate is used for pMOSFET. The threshold voltages for nMOSFET and pMOSFET are highly symmetrical because of the highly symmetrical MOS structures in the two types of transistors. The use of p+ gate for p-MOSFET results in a surface-channel device. Traditionally, buried channel pMOSFETs are preferred, because they have better hole mobility due to less severe scattering in the channel. However, in a surface channel pMOSFET, a better control of gate to silicon surface is achieved, and short-channel effects are better suppressed compared to a buried channel pMOSFET. As technology advances and the process is continuously improved, a superior oxide/substrate has been achieved, and the hole mobility in surface channel pMOSFET is no longer a serious concern. In this chapter, we will focus on surface channel p+/pMOSFET only.

Previous research works also show that the surface-channel pMOSFET with p+-poly gate is about one order of magnitude less leaky than its nMOS counterpart [1]. This can be attributed to the smaller tunneling probability of holes compared to electrons. Furthermore, it has been identified that in the p+/pMOS structure, the gate tunneling leakage current is “bipolar”. Specifically, both electrons and holes are involved in the tunneling, and dominate gate leakage at high and low gate voltages,

respectively [1] - [4]. Due to the unique features associated with the gate leakage of surface-channel p+/pMOSFET, it can be expected that the stress-induced leakage current (SILC) in p+/pMOSFET with ultrathin gate oxides could behave quite differently from its nMOS counterpart. Even though there are numerous articles on SILC in the literature, the dual-gate case has been considered only recently [5] [6], and a complete description of SILC in dual-gate CMOSFETs with ultrathin gate oxides is not yet available.

In this chapter, the stress-induced leakage current (SILC) in p+/pMOSFET with ultrathin nitrided gate oxides (1.7 nm and 2.2 nm) are measured and characterized, using the experimental procedure shown in the previous chapter. Specifically, the change in the electron current component and hole current component of in the gate leakage are constantly monitored for various stress levels. For a better description of SILC and its components, the traditional SILC is termed as gate SILC, and its hole current component and electron current component are denoted as hole SILC and electron SILC, respectively, in accordance with the work of Ielmini *et al.* [9]. Gate SILC actually is the total stress-induced gate leakage current (ΔJ_g). For p+/pMOSFET in inversion, hole SILC and electron SILC are stress-induced source-drain current (ΔJ_{sd}) and substrate current (ΔJ_{sub}), respectively.

In order to understand the polarity dependence of SILC, both positive and negative stress voltages are used. The magnitude of stress voltages used ranges from 3.5 V to 4.7 V.

3.2 Electrons and Holes in the Gate Leakage Current

Figure 3.1 schematically shows the evolution of the 1-D energy diagram of a fresh p+/pMOS, from strong inversion to strong accumulation. In strong accumulation, where both electrons in the bottom electrode and holes in the top electrode are present in huge number, electron tunneling dominates the gate leakage current because electrons in the accumulation layer face a lower potential barrier (~3.2 eV) than holes in the poly-gate (~4.3 eV). It is noted that in accumulation, there is always a small current hump between 0 to 1 V. In the literature, this current was attributed to the electron tunneling

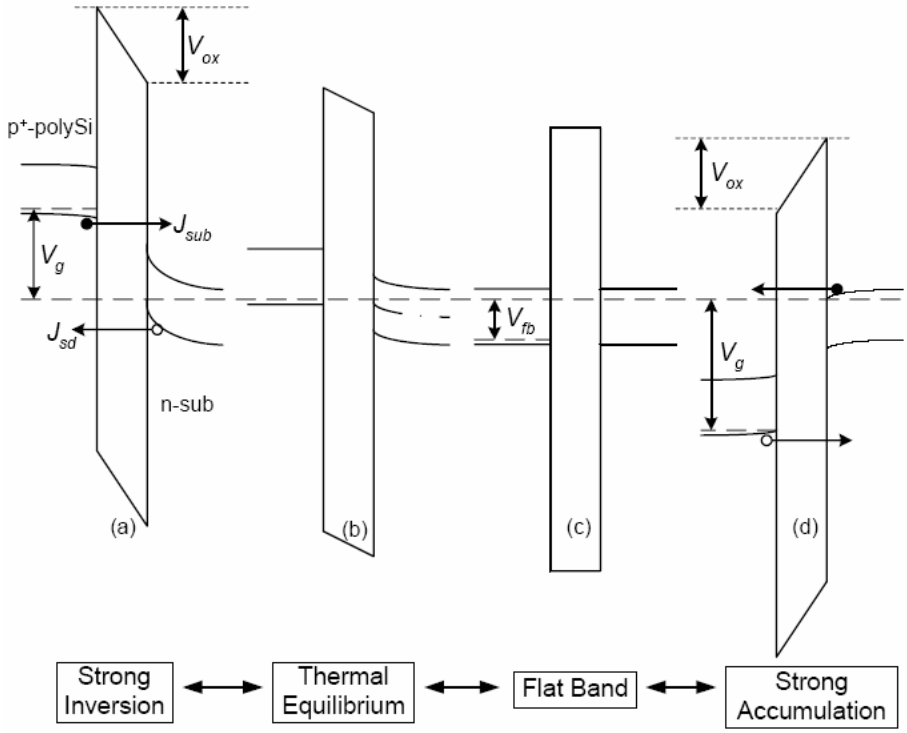

Figure 3.1: Energy band diagrams illustrating the transition from strong inversion to strong accumulation of a p+/pMOS structure.

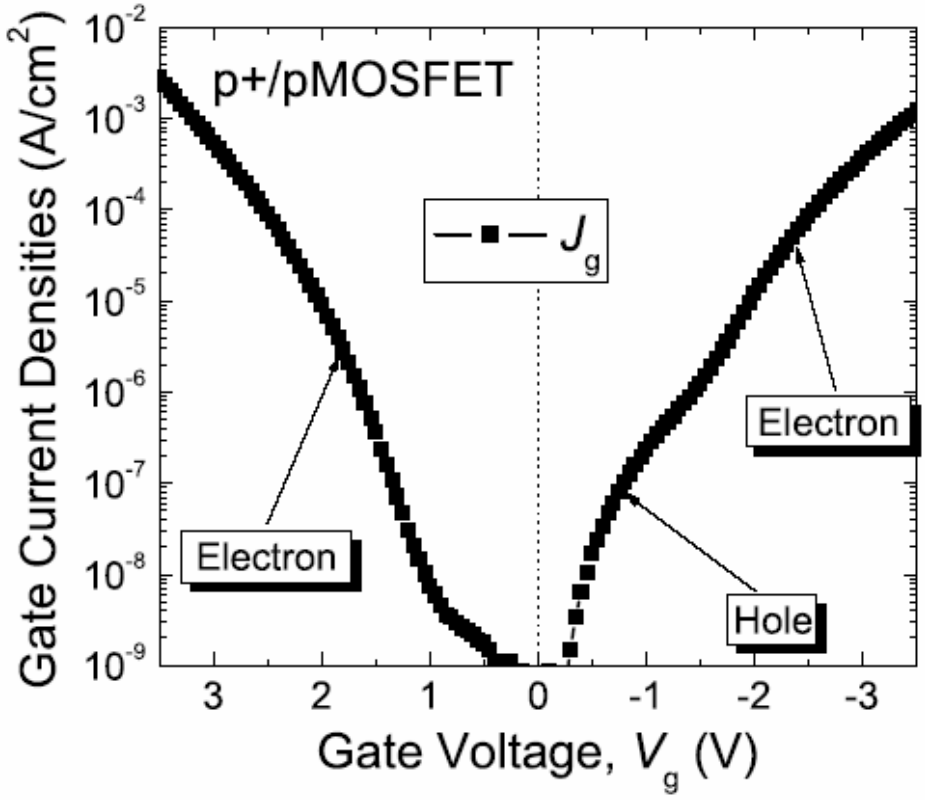

Figure 3.2: Gate tunneling leakage current of a p+/pMOSFET with ultrathin gate oxide as the function of gate voltage, from strong accumulation to strong inversion. Device dimension: W= 40 μm, L = 20 μm, T_{ox} = 2.2 nm.

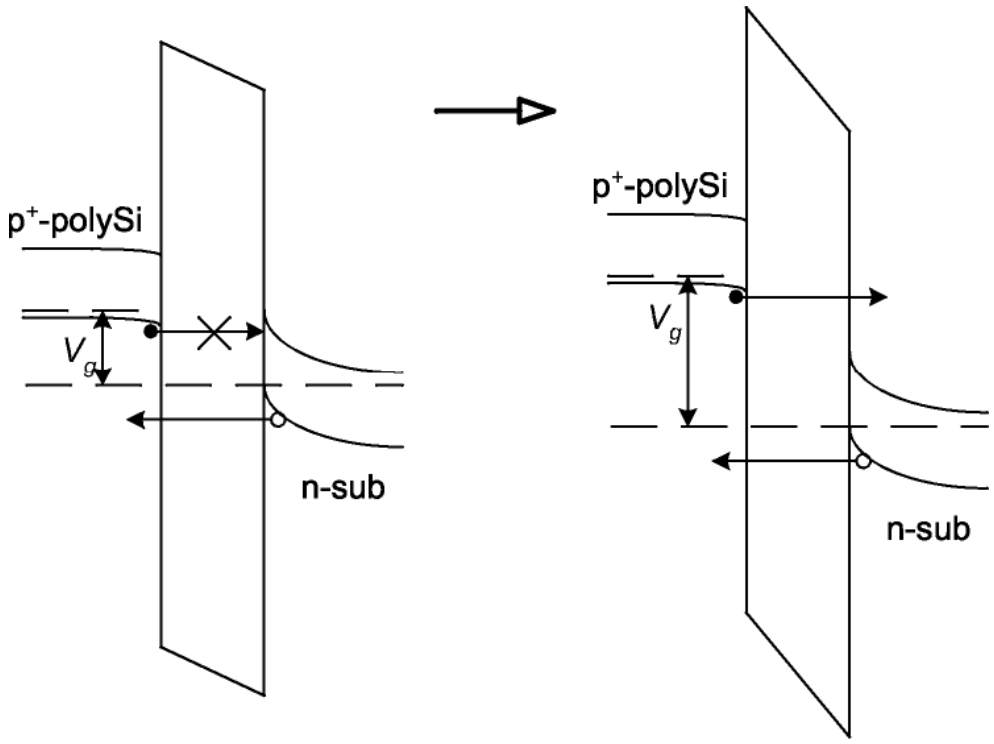

Figure 3.3: Schematic diagrams showing the transition of gate bias from low-negative voltage to impact-ionization region in a p+/pMOS.

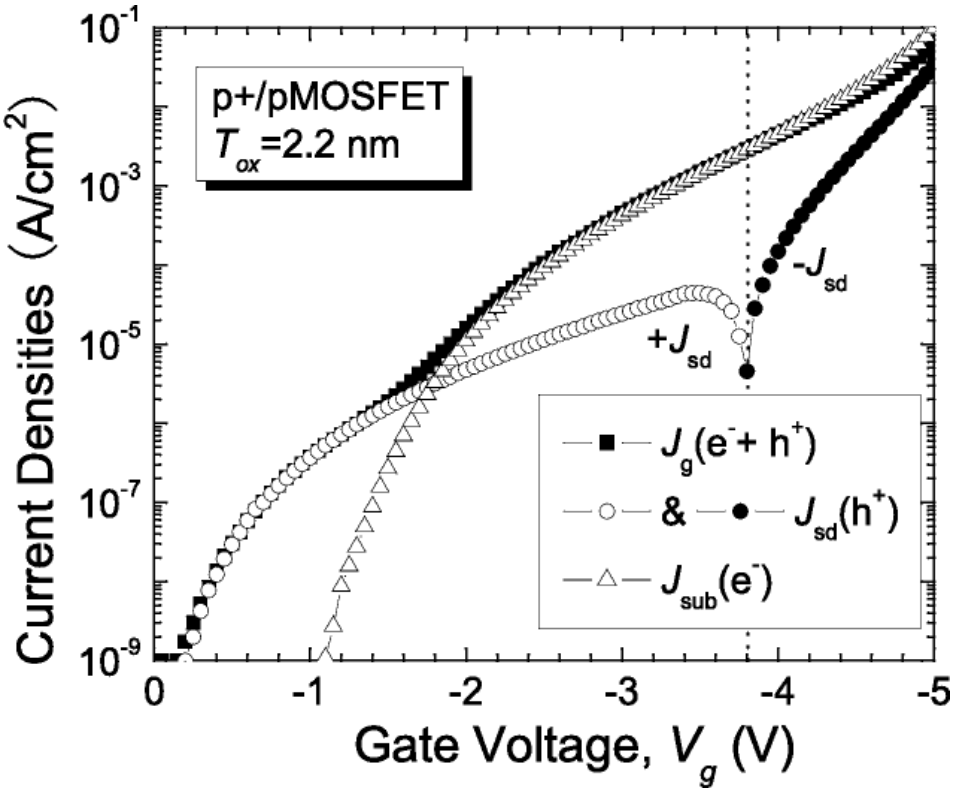

Figure 3.4: Carrier separation curves of a p+/pMOSFET with the gate voltage swept from zero bias to the strong impact ionization regime (in inversion region). Solid and open circles denote positive and negative currents, respectively.

via interface states [10]. While in strong inversion, the potential barrier for electron tunneling from gate to substrate and hole tunneling from channel to gate are comparable (~ 4.3 eV). In this case, dominant tunneling carrier type is determined by the potential difference between gate and substrate.

As has been shown in Section 2.3, as gate voltage increases from zero to a large negative value, the dominant component of gate leakage changes from hole current to electron current. In a p+/pMOS structure, the electron tunneling is from gate to substrate conduction band, and hole tunneling is from substrate valence band to gate valence band. For p+-poly gate, electrons tunnel from its valence band, unless gate bias is high enough to invert the polysilicon. At low negative gate voltage, the valence band edge of the p+ gate is aligned to the band gap of the silicon substrate, thus electron tunneling to substrate conduction band is strongly inhibited, as shown in Figure 3.3. In this case, hole tunneling is the dominant component in the gate leakage current. As gate voltage becomes more negative, the valence band edge of the poly-gate is elevated, and finally goes above the conduction band edge of the substrate. When this happens, electron tunneling from the p+ gate valence band is initiated, and dominates over hole tunneling quickly. This transition process is well demonstrated in Figure 3.4, in which the relationships between gate leakage, electron current, and hole current are shown as a function of gate bias. The curves are obtained simultaneously by the carrier separation technique described in Chapter 2. Such dominance of hole current component in the gate leakage current at low gate voltage is unique in surface p+/pMOSFETs.

We notice that in Figure 3.4, the hole current exhibits a sign change at around $V_g = -3.8$ V. This point indicates that impact ionization in the silicon surface begins to dominate the tunneling current, and the source and drain "sinks" the holes generated by impact ionization. As shown in Figure 3.5, when the gate voltage is high enough, electrons injected into substrate from the gate are energetic enough to generate electron-hole pairs. The generated electrons flow to the substrate and cause J_{sub} to increase, while the generated holes sink to the grounded source and drain terminals. When the flow of these generated holes is large enough, J_{sd} changes from positive to negative, and J_{sub} becomes larger than J_g as shown in Figure 3.4. The point of sign change is found to be dependent on gate oxide thickness. For a 1.8 nm gate oxide, J_{sd} becomes

negative at about $V_g = -3.0$ V. It should be noted that the stress voltages used in our experiments are all in impact-ionization region.

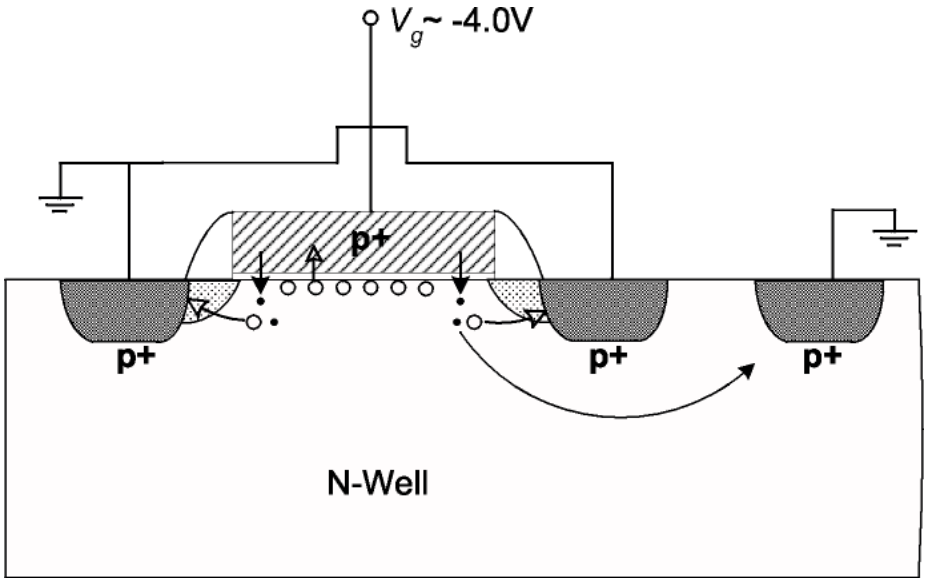

Figure 3.5: Impact ionization in the substrate surface induced by highly energetic electrons, which originated from the valence band of the p+ gate.

3.3 Gate SILC in p+/pMOSFETs

The evolution of gate leakage characteristics during constant-voltage stress is shown in Figure 3.6. A constant voltage of −4.3 V was applied to the gate during stress. The stress was interrupted at pre-defined stress intervals to obtain the gate leakage characteristics by carrier separation measurement. The cumulative stress time (t) ranges from 10^2 to as high as 10^6 seconds. It can be seen that the J_g-V_g curve shifts up as stress time increases. The difference between the pre-stress curve and post-stress curve, as well as the differences between the post-stress curves of different stress times, is subtle, because the pre-stress tunneling leakage current is already very high.

The gate SILC characteristics (ΔJ_g-V_g), which can be obtained by subtracting the pre-stress gate leakage (J_{g0}) from the post-stress J_g, are shown in Figure 3.7. The increase in SILC as stress time increases is clearly shown. The gate SILC strongly depends on the sense voltage (V_g), and increases rapidly and monotonically as $|V_g|$ increases. However, by normalizing the gate SILC with pre-stress gate leakage, the

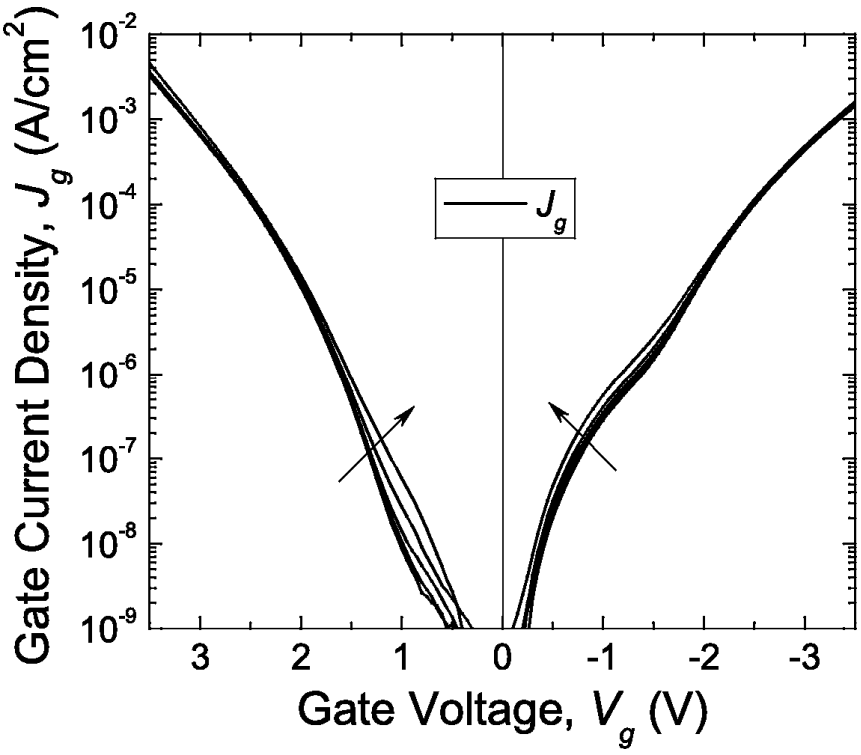

Figure 3.6: Shift in the gate leakage characteristics of a p+/pMOSFET after 4 cumulative stress intervals: 10^2, 10^3, 10^4 and 10^5 seconds (along the direction of the arrows).

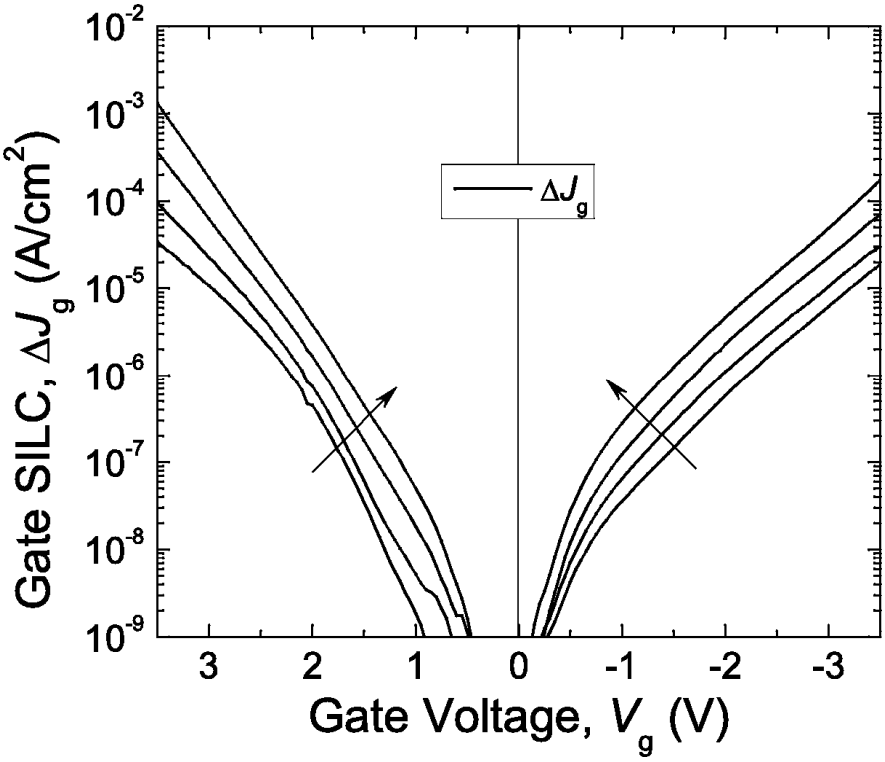

Figure 3.7: Gate SILC of a p+/pMOSFET as a function of the sense voltage, with stress time as the parameter. The SILC is obtained from the J_g-V_g characteristics in Figure 3.6. Cumulative stress time increases along the arrow: 10^2, 10^3, 10^4 and 10^5 seconds.

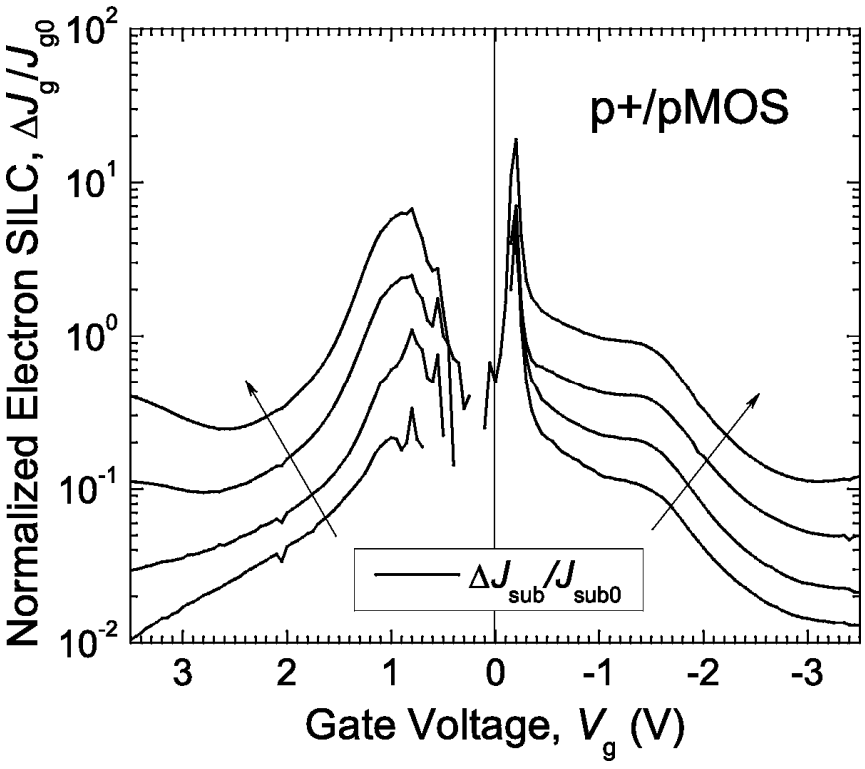

Figure 3.8: Normalized gate SILC of a p+/pMOSFET as a function of the sense voltage, with stress time as the parameter. The normalized SILC is obtained from the J_g-V_g characteristics in Figure 3.6.

gate voltage dependence is greatly suppressed, as shown in Figure 3.8. Furthermore, the relationship between SILC and V_g is no longer a simple monotonic function. At low gate voltage, two peaks can be identified at $V_g = 0.8$ V and $V_g = -0.2$ V, respectively. In the literature, these two low-voltage peaks have been attributed to the electron tunneling through interface traps [10]. However, there is possibility that the second peak is because J_{g0} becomes lower than measurement limitation, i.e. it's an artifact. For short stress time, the normalized SILC decreases as sensing voltage increases ($|V_g| > 1$ V). This indicates that the significance of SILC in the overall gate leakage decreases as gate voltage increases. However, at longer stress time, the normalized SILC tends to increase at high sense voltage ($|V_g| > 3$ V), indicating a possible change in the conduction mechanism.

Classically, SILC depends exponentially on the stress time. Specifically, the gate SILC can be written as [7] [8]

$$\Delta J_g = f(V_g) \cdot t_s^n \tag{3.1}$$

where n is a constant reported to be ~0.5. If n is not dependent on the sense voltage, the ΔJ_g -V_g characteristics at different stress times should be parallel to each other. Assuming that $f(V_g)$ does not change with stress time, then for two different cumulative stress time t_1 and t_2, Equation 3.1 leads to

$$\log \Delta J_{g2} - \log \Delta J_{g1} = n \cdot \log \frac{t_2}{t_1} \tag{3.2}$$

and

$$n(t_1, t_2) = \frac{\log \Delta J_{g2} - \log \Delta J_{g1}}{\log(t_2 / t_1)} \tag{3.3}$$

where ΔJ_{g1} and ΔJ_{g2} are the gate SILC corresponding to t_1 and t_2 respectively.

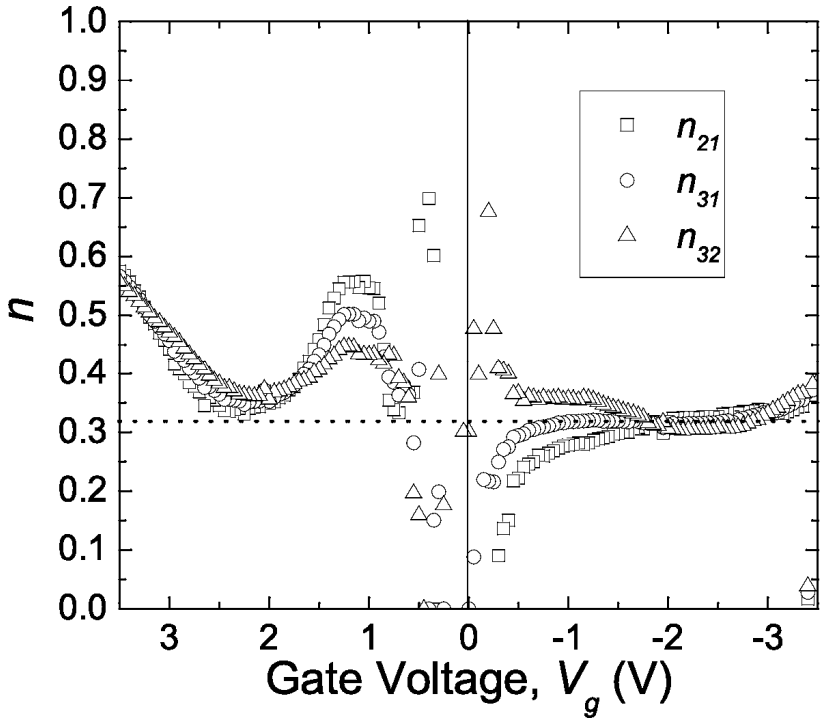

Figure 3.9: Power-law exponent n, where n is as defined in the relation $\Delta J_g = f(V_g) \cdot t^n$, as a function of the sense voltage. Note that $n_{21} = n(t_2,t_1)$, $n_{31} = n(t_3,t_1)$, $n_{32} = n(t_3,t_2)$, with $t_1 = 10^3$ s, $t_2 = 10^4$ s, $t_3 = 10^5$ s.

Using Equation 3.3, the n-V_g relationship can be determined from the difference between the SILC associated with two different stress times. An example is shown in Figure 3.9. In this figure, n is obtained from three stress times: $t_1 = 10^3$ s, $t_2 = 10^4$ s, $t_3 = 10^5$ s. From Figure 3.9, we see that the exponent n is highly dependent on the sense voltage and polarity. For negative gate voltage, especially in the strong inversion

regime ($V_g < -1$ V), the exponent n is quite constant, independent of V_g, and is not sensitive to stress time as well. In this region, n can be well approximated by $n = 0.33$. When the gate voltage is positive, however, we see that n shows strong gate voltage dependence. Furthermore, at low positive voltage ($0 < V_g < 1.5$ V), n also depends on stress time. The polarity dependence of n indicates that the conduction mechanism of SILC may also be polarity dependent. In the next sections, we will focus on SILC in the inversion regime, the usual operating voltage condition for the p+/pMOSFET.

3.4 Hole SILC in p+/pMOSFETs

Corresponding to the gate SILC shown in the last section, the evolution of hole tunneling current characteristics and hole SILC are shown in Figure 3.10 and 3.11 respectively. As expected, the hole leakage current increases steadily with stress time. Furthermore, the voltage at which the hole leakage current changes sign, is continuously pushed to more negative region.

The normalized hole SILC ($\Delta J_{sd}/J_{sd0}$) is shown as a function of the sense voltage in Figure 3.11. The normalized hole SILC is rather insensitive to the sense voltage, ranging from about 0.5 V to 3.0 V. The sharp increase in the normalized SILC at high gate voltage is due to the decrease of J_{sd0}, when V_g is sufficiently large to trigger significant impact ionization in the substrate.

In Figure 3.12, a comparison between the gate SILC and hole SILC is made. Several interesting observations are noted.

1. Similar to initial gate leakage current, the gate SILC is also dominated by hole SILC in the low gate sense voltage regime.
2. As stress time increases, hole SILC in the high gate sense voltage regime approaches the gate SILC.

The first observation is similar to the observed dominance of the hole tunneling current in a fresh sample. It may be explained by the fact that the availability of substrate conduction band states is manipulated by the gate voltage. However, this theory alone could not account for the second observation, *which suggests substantial increase of the hole tunneling leakage component following stress.*

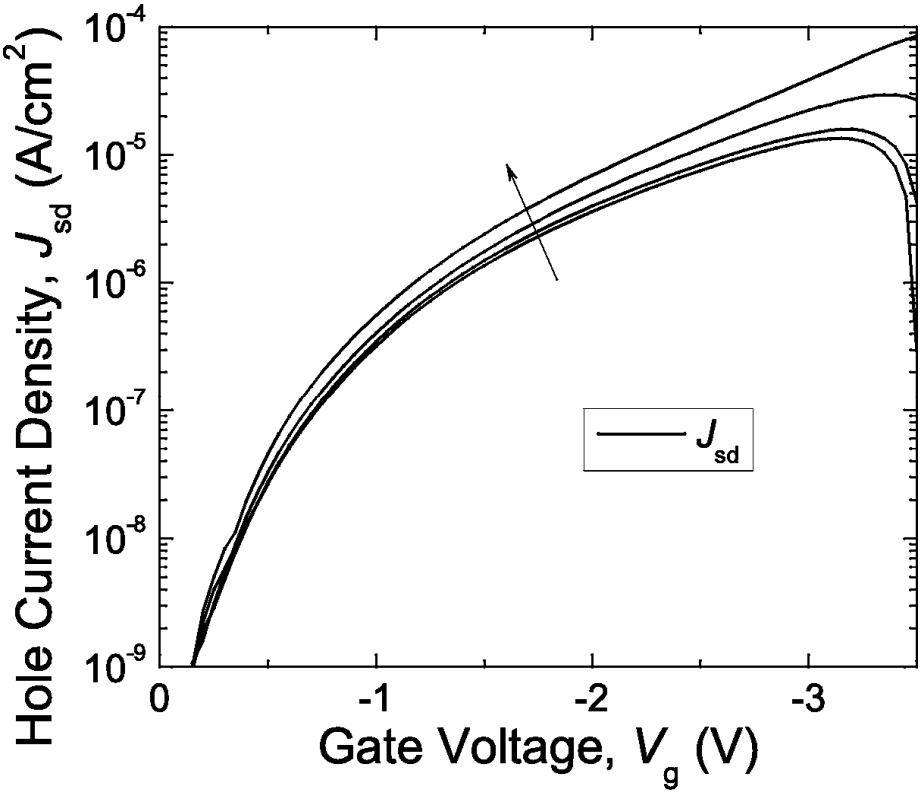

Figure 3.10: Increase in the hole tunneling current in a p+/pMOSFET subjected to constant voltage stress, in respect to the gate SILC shown in Figure 3.7. The stress time increases in the direction of the arrow.

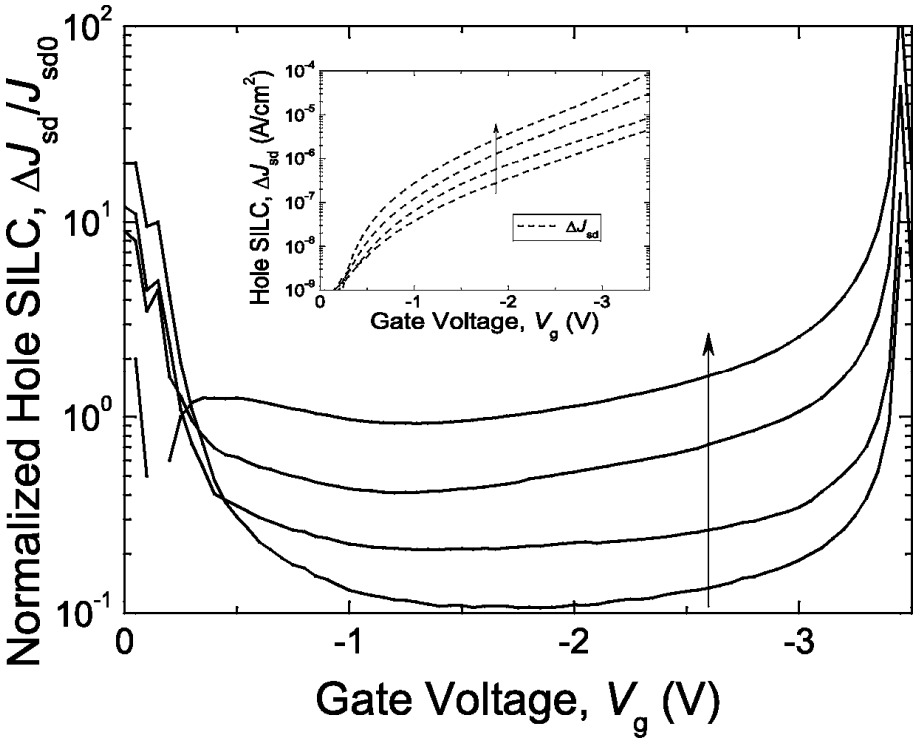

Figure 3.11: Normalized hole SILC in p+/pMOSFET as a function of the gate sense voltage, after different stress intervals. The normalized SILC curves are obtained based on the data in Figure 3.10.

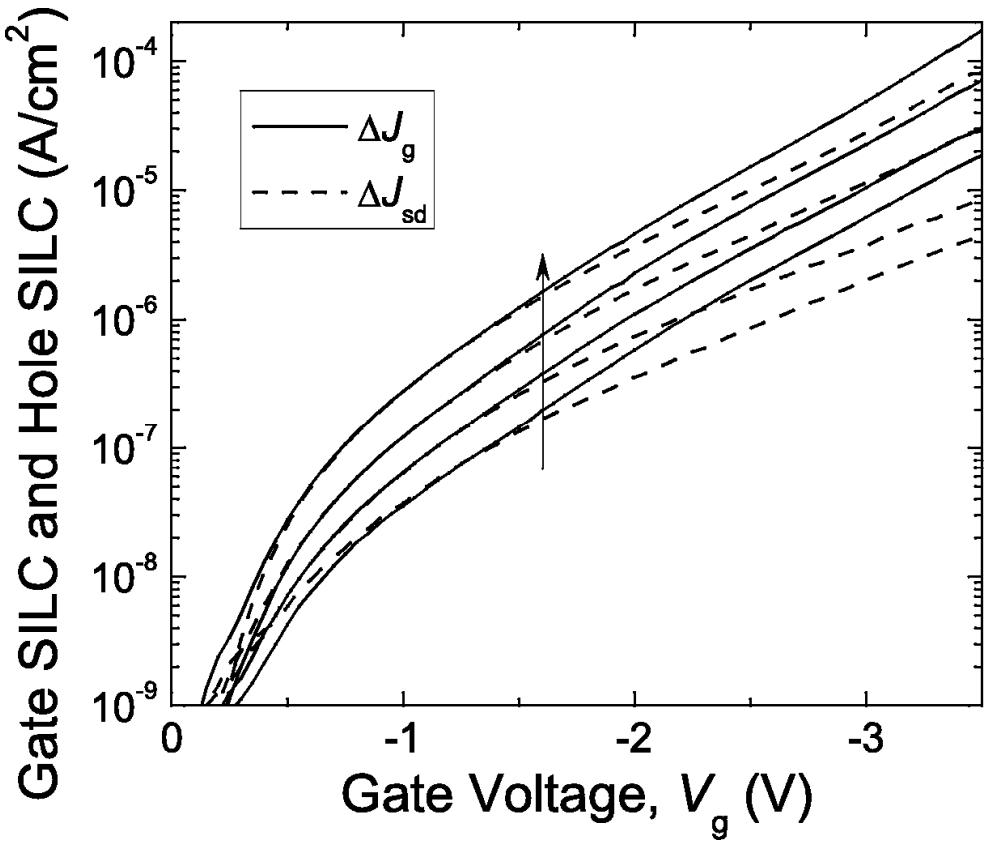

Figure 3.12: Gate and hole SILC as a function of the gate sense voltage with stress time as the parameter.

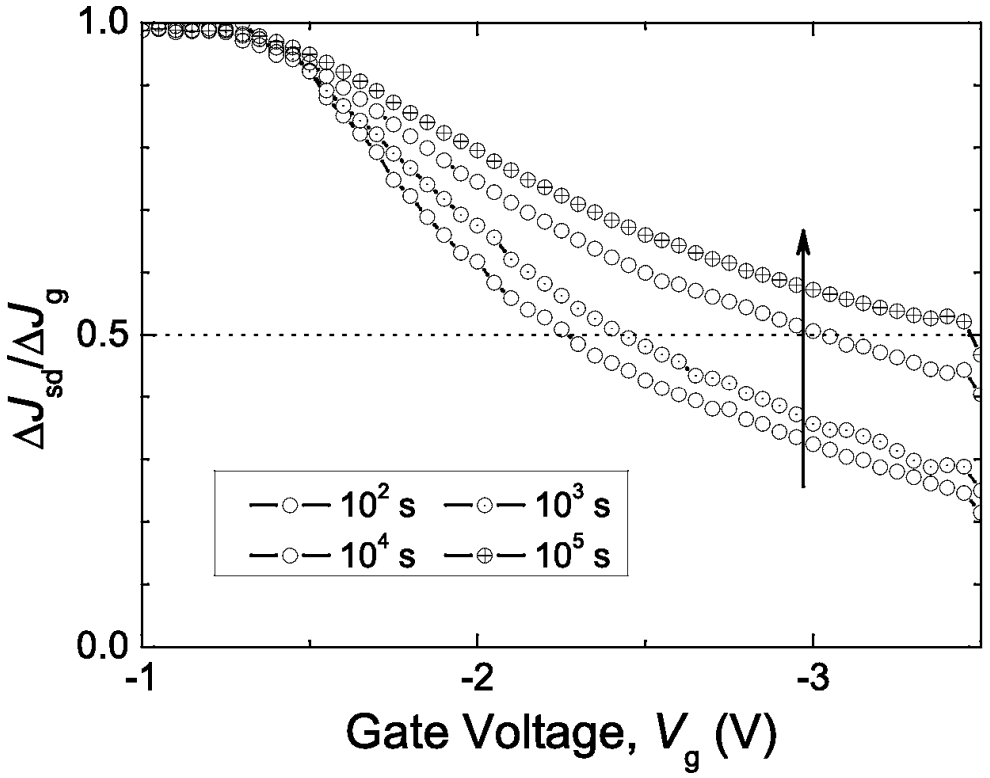

Figure 3.13: The fraction of hole current component in the overall gate SILC ($\Delta J_{sd}/\Delta J_g$) as a function of the gate sense voltage, with stress time as the parameter.

In order to better understand the relationship between hole SILC and gate SILC, the proportion of hole current in the gate SILC, i.e. $\Delta J_{sd}/\Delta J_g$, is plotted as the function of the sense voltage in Figure 3.13, with stress time as the parameter. For $|V_g| < 1.5$ V, $\Delta J_{sd}/\Delta J_g$ approaches 1. As V_g becomes more negative, $\Delta J_{sd}/\Delta J_g$ drops monotonically because of the occurrence of valence band electron tunneling. However, we can clearly see that the $(\Delta J_{sd}/\Delta J_g)$-$V_g$ curve is continuously shifted upward by stress. For convenience, we denote the gate voltage at which $\Delta J_{sd}/\Delta J_g = 0.5$ as V_{oe}. For $t_s = 10^2$ s, $V_{oe} = -2.2$ V. When t is increased to 10^4 s, V_{oe} is increased to as high as -3.0 V. For $t_s = 10^5$ s, the longest stress time shown in Figure 3.13, V_{oe} has already increased beyond -3.5 V, which approximately corresponds to the onset of significant impact ionization by non-SILC electrons. Figure 3.13 strongly indicates the gradual dominance of hole SILC in the gate SILC of p+/pMOSFET with ultrathin gate oxide.

Considering the fact that electrical stress also causes electron SILC to increase, which will be shown in the next section, Figure 3.13 implies that hole SILC increases faster than electron SILC. The relationship between these two components will also be discussed in next session.

3.5 Hole SILC vs. Electron SILC

The electron SILC, measured from ΔJ_{sub}, is shown in Figure 3.14. The measurement covers both the accumulation and inversion regions. Similar to the hole SILC, the electron SILC increases with the cumulative stress time. In the accumulation region, the electron SILC coincides very well with the gate SILC, and the hole current is negligible, as shown in Figure 3.15. In the inversion region, as expected, the electron current is more and more a minor component in gate SILC when stress level increases. In the inversion region, the electron SILC accounts for most of the gate SILC in the early stress stage. However, the proportion of electron SILC to gate SILC gradually decreases as stress progresses.

It will be of interest to compare the hole SILC and the electron SILC in the inversion region, with cumulative stress time as a parameter. Data from Figure 3.11 and Figure 3.14 are plotted in Figure 3.16 showing both ΔJ_{sd}-V_g and ΔJ_{sub}-V_g. It is clearly

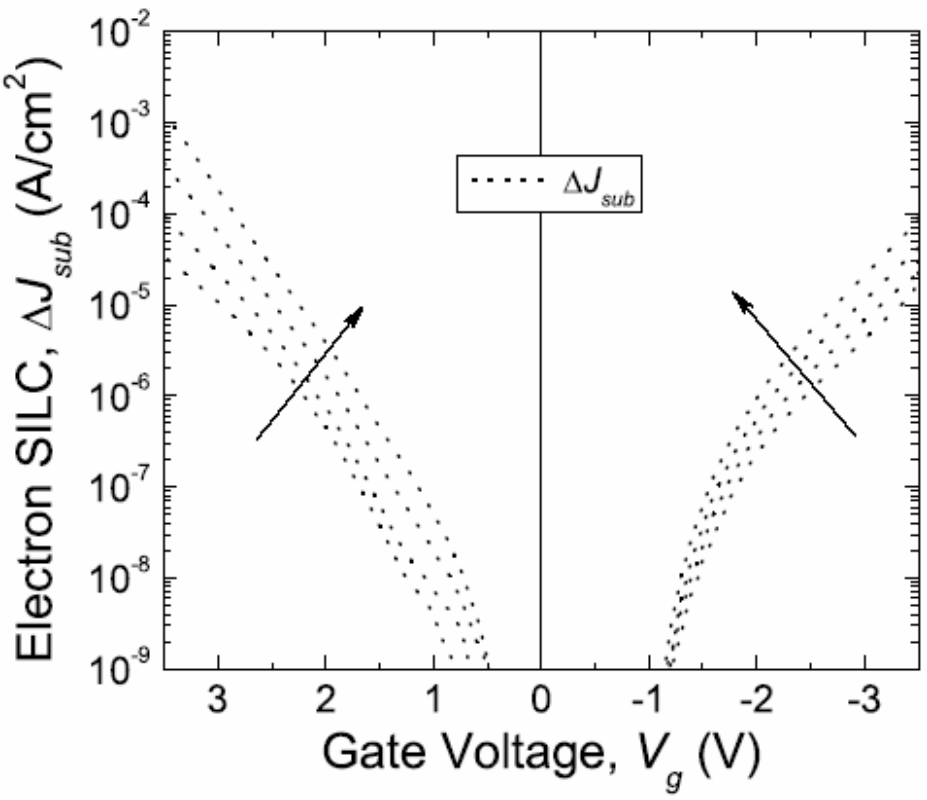

Figure 3.14: Electron SILC as a function of gate sense voltage, for the accumulation and inversion regions. Stress time increases in the direction of the arrow.

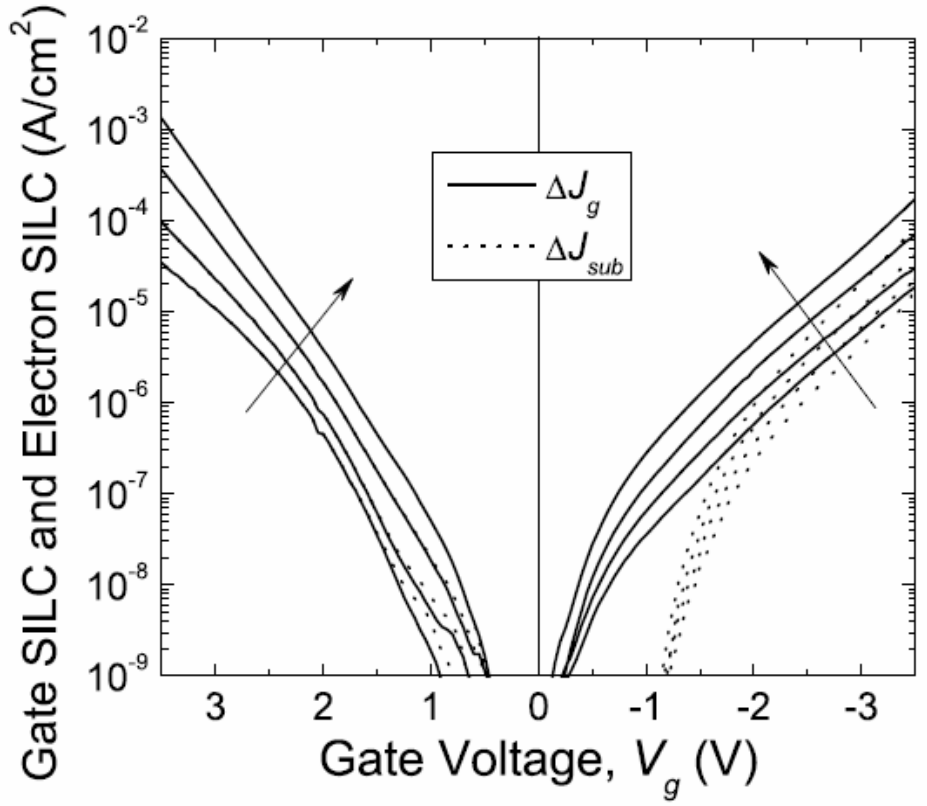

Figure 3.15: A comparison of ΔJ_{sub} and ΔJ_g in the accumulation and inversion regions.

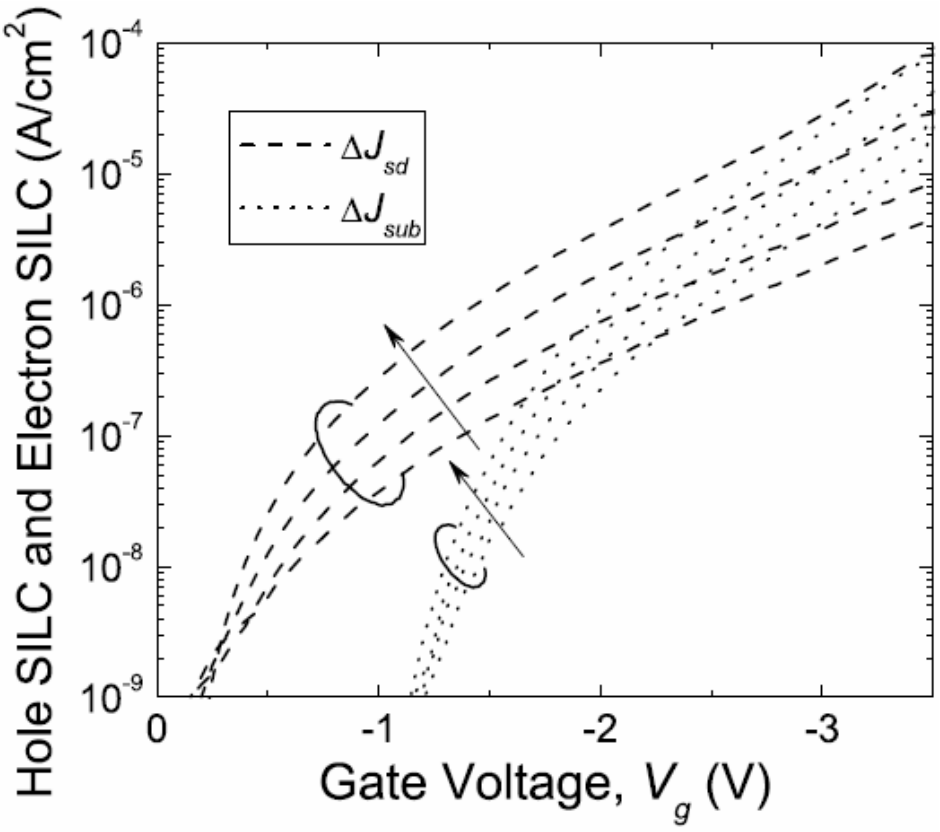

Figure 3.16: A comparison of hole SILC (ΔJ_{sd}) and electron SILC (ΔJ_{sub}) in the inversion region, for different stress time.

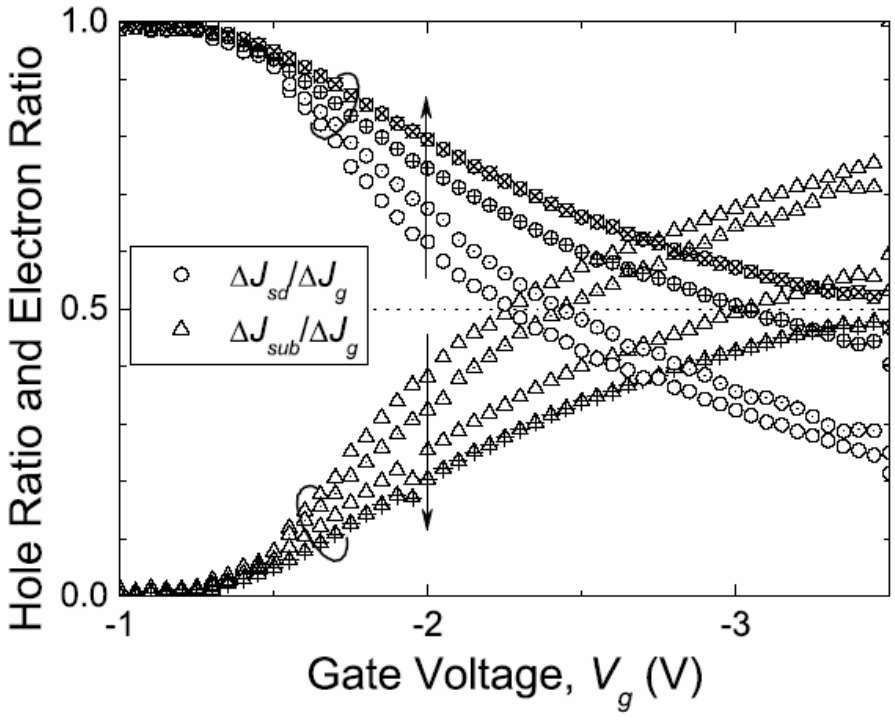

Figure 3.17: Normalized hole SILC (circles) and electron SILC (triangles) characteristics, with the stress time as the parameter.

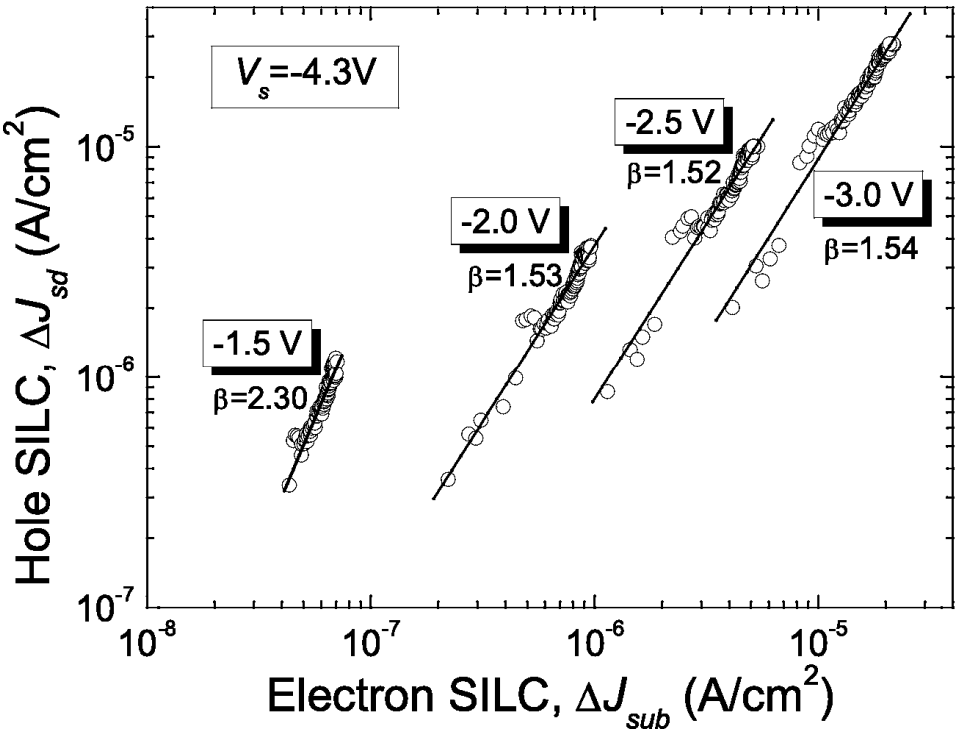

Figure 3.18: The correlation between hole SILC and electron SILC for different gate sense voltages. The relation between these two components can be well described by a power-law expression. The gate sense voltages and the power-law exponents are given in the figure accordingly. Stress voltage $V_s = -4.3$ V.

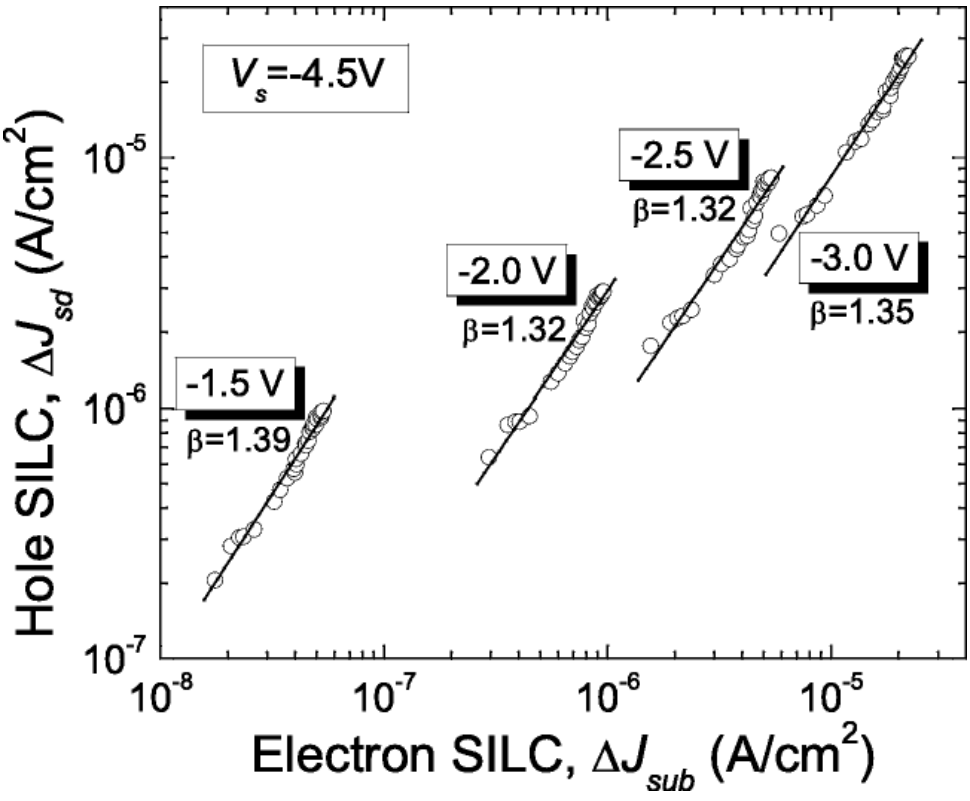

Figure 3.19: Similar to Figure 3.18, except that stress voltage is higher at −4.5 V.

shown that at short stress time, e.g. $t_s = 10^2$ s, electron SILC exceeds electron SILC for $|V_g| > 2.3$ V. Following the longest stress interval, i.e. $t_s = 10^5$ s, the dominant gate leakage component is hole SILC voltage ranging up to the onset of substrate impact ionization. To directly compare the significance of these two components in the gate SILC, we have plotted $(\Delta J_{sub}/\Delta J_g)$-$V_g$ as well as $(\Delta J_{sub}/\Delta J_g)$-$V_g$ in the inversion region in Figure 3.17. The downward shift of $(\Delta J_{sub}/\Delta J_g)$-$V_g$ corresponds well to the upward shift of $(\Delta J_{sd}/\Delta J_g)$-$V_g$. It has been reported that a one-to-one relationship exists between the hole SILC and the electron SILC [9], [14], i.e. for a given gate sense voltage,

$$\log \Delta J_{sd} = \beta \cdot \log \Delta J_{sub} \tag{3.4}$$

where β is a constant (a 1-1 relationship implies $\beta = 1$). In Figure 3.18, we plot ΔJ_{sd} vs. ΔJ_{sub} on log-log scale. A linear relationship exists between these two components. For a given stress voltage, the value of β is insensitive to the gate sense voltage for $|V_g| > 2$ V. However, instead of having a value of 1 as has been reported in [14] [15], β is found to be larger than 1.5 for stress voltage at −4.3 V. Furthermore, β is also dependent on stress voltage. Figure 3.19 is similar to Figure 3.18, except that the stress voltage was 0.2 V higher. We see that β is decreased by about 0.2 compared to that in Figure 3.18. The non-unity β and its dependence on stress voltage indicate a non-recombination SILC conduction mechanism. Figure 3.18 and 3.19 provide clues to explain the dominance of hole current in SILC, and will be discussed in detail in the next section.

3.6 Physical Model for Hole-Dominant SILC

From the previous discussions, we established that in the gate SILC of p+/pMOSFET with ultrathin gate oxide, the hole SILC is the dominant component, and the dominance of this component is continuously increased by stress. This observation can be of great importance for understanding the degradation of ultrathin gate oxides. It is well-known that holes have a larger trap generation efficiency than electrons in the gate oxide. A hole-dominant leakage current means a higher oxide degradation rate than its electron-dominant counterpart. It has been predicted that ultrathin gate oxides

in pMOS devices have a shorter lifetime than those in nMOS devices [18]. Our experimental results indicate that the dominant hole SILC might be responsible for the faster oxide degradation in p+/pMOSFETs than in n+/nMOSFETs. The increased hole current induces more damage (usually by generating more traps) in the gate oxide, which further increases the hole current. Thus a positive feedback loop is formed. However, before we discuss its impact on oxide degradation we need to provide a physical explanation for the observed hole-dominant SILC.

It has been widely accepted that SILC is determined by the neutral traps in the oxide. The density, spatial distribution, and energy distribution of traps play a very important role on on SILC conduction. For ultrathin gate oxides, the spatial trap distribution is no longer a concern, for the oxide thickness is already comparable to the dimension of an oxide trap. In Figure 3.20, two different energy distributions of oxide traps are shown, together with the respective electron and hole tunneling process: two separate trap distributions vs. a single distribution.

The good correlation between hole SILC and electron SILC seems to suggest that a common trap distribution is responsible for both components (Figure 3.20 (a)). Under this assumption, oxide traps responsible for SILC is very deep inside the oxide band gap, in accordance with the finding of [16]. However, for a single trap distribution, we should expect a dominant recombination component in the SILC [14] [15]. As shown in Figure 3.20 (a), when both the electron and hole are tunneling into the same trap distribution, the probability of electron-hole recombination at the trap site should be much larger than the probability of tunneling out. If that is the case, we would expect

1. β to have a value of one.
2. β to be insensitive to the gate sense voltage. Even if there is some dependence on the gate sense voltage, β should be smaller for lower gate sense voltage.
3. β to be independent of the stress voltage.

However, this hypothesis is not borne out by our experimental results. In Figure 3.21, β is plotted as a function of the gate sense voltage, for three different stress voltages: −4.3 V, −4.5 V, and −4.7 V. It seems to be true that β is not very sensitive to sense voltage. However, it is clearly shown that β decreases as stress voltage increases. This observation suggests that for a given oxide thickness, β~1 is only valid for a certain stress voltage, e.g. −4.5 V for 2.2 nm shown in Figure 3.21. These observations tend to

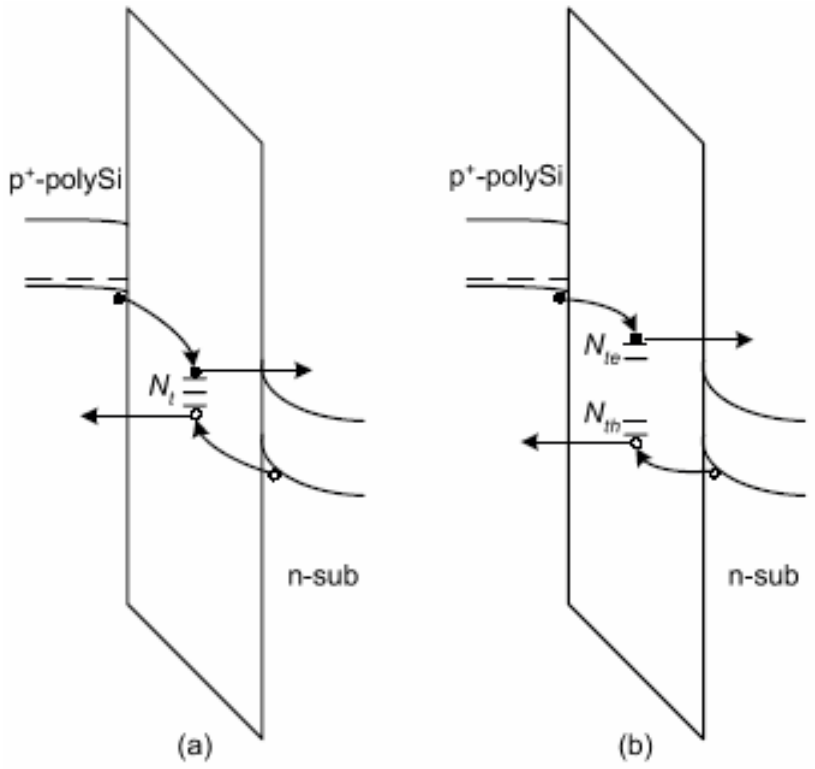

Figure 3.20: Schematic illustration of two TAT conduction mechanisms: electron tunneling and hole tunneling via: (a). a common oxide trap distribution [15]; (b) two separate oxide trap distribution.

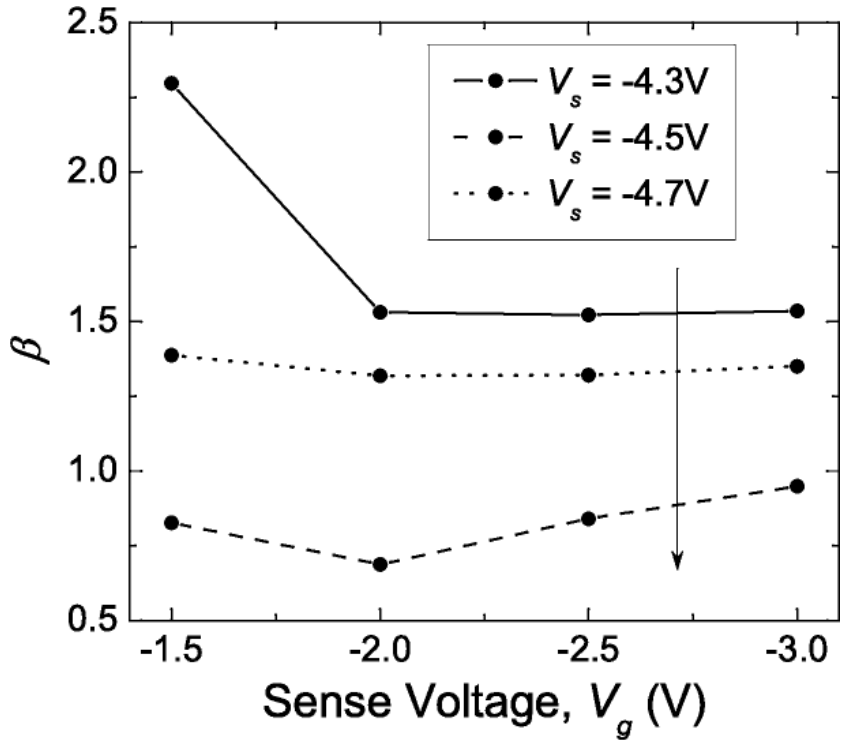

Figure 3.21: β as a function of the gate sense voltage, with stress voltage as the parameter.

exclude the possibility that the electron and hole SILC takes place through the same trap distribution

If electron tunneling and hole tunneling takes place at two separate oxide trap distributions (Figure 3.20 (b)), we have

$$\lg \Delta J_{sd} \propto \Delta N_{th} \quad \& \quad \lg \Delta J_{sub} \propto \Delta N_{te} \tag{3.9}$$

$$\lg \Delta J_{sd} \propto \frac{N_{th}}{N_{te}} \lg \Delta J_{sub} \tag{3.10}$$

where ΔN_{te} and ΔN_{th} are the average trap density facilitating electron tunneling and hole tunneling, respectively. Physically, ΔN_{te} and ΔN_{th} are probably of the same origin, because oxide traps responsible for SILC are neutral, and they can trap electrons as well as holes. ΔN_{te} and ΔN_{th} are dependent on the stress voltage and stress time. Comparing Equation 3.9 and Equation 3.11, we have

$$\beta \propto \frac{\Delta N_{th}}{\Delta N_{te}}. \tag{3.11}$$

In the strong inversion region, the number of electrons in the valence band of the p+-gate and holes in the inversion layer available for tunneling is huge, thus the tunneling probability is determined by the gate sense voltage and trap density. For a fixed gate sense voltage, the ratio $(\lg\Delta J_{sd})/(\lg\Delta J_{sub})$ is determined by ΔN_{th} and ΔN_{te}. As shown in Figure 3.18 and 3.19, for a given gate sense voltage, β is a constant, independent of the stress time, indicating that the ΔN_{th} and ΔN_{te} ratio is not affected by the duration of the stress. Furthermore, as shown in Figure 3.21, β is also insensitive to the gate sense voltage. This is possible only if ΔN_{th} and ΔN_{te} are linearly correlated. Since there are two separate sources of current injection generating oxide traps, it is not clear why the two separate oxide trap distributions are so well correlated. One explanation is that trap creation is mainly determined by the energy of injected carriers. When ultrathin gate oxides are stressed in the direct tunneling regime, the energy of electrons and holes flowing across the oxide is uniquely determined by gate-to-substrate voltage.

Based on Figure 3.20(b), the dominant hole SILC component may be attributed to a larger oxide trap density (ΔN_{th}), near the Si valence band edge. This may be due to trap localization or a broader spread of the trap distribution near the Si valence

band edge. So far, the physical mechanisms behind such a oxide trap distribution favoring hole tunneling it's not well understood, but not electron tunneling, remain elusive. One possible explanation lies in the larger trap generation efficiency of hole compared to electron.

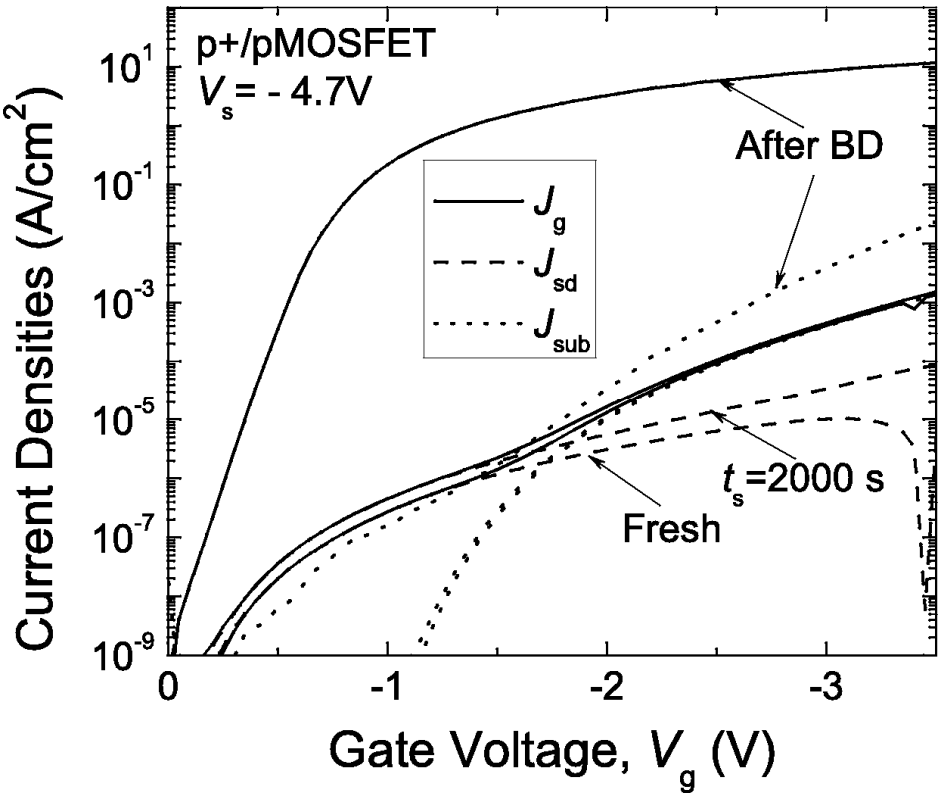

Figure 3.22: Carrier separation curves for p+/pMOSFET after three stress intervals: t_s = 0 (fresh device), t_s = 2000 s and t_s = 2900 s. The stress voltage is at −4.7 V.

Following our argument that the importance of the hole SILC component is continuously increased by stress, it is expected that as the stress time increases, there will be a point at which the gate leakage is totally dominated by hole SILC, and electron SILC becomes negligible within the voltage range of interest. In Figure 3.22, three sets of carrier separation curves are shown for the fresh device, after stress time t_s = 2000 s and after oxide breakdown [17]. The second set of curves (t_s = 2000 s) were obtained at the measurement point nearest to breakdown, which happens after 2.9×10^3 s of stress. A stress voltage higher than those used in previous experiment was chosen to accelerate SILC generation and oxide breakdown. The gate leakage current increases dramatically after oxide breakdown. Furthermore, it

is observed that the gate leakage consists only hole current. The electron current does not change much after oxide breakdown and it is at least three orders smaller than the hole current. Figure 3.22 clearly indicates a nearly 100% hole-dominated gate leakage current after oxide breakdown. More importantly, it implies that oxide breakdown is triggered by those oxide traps responsible for hole SILC, i.e. they are localized near the Si valence band edge.

To verify our hypothesis that two separate oxide trap distributions are responsible for the hole and electron SILC, substrate-hot hole (SHH) injection was used to generate SILC in a p+/pMOSFET having the same dimensions and gate oxide thickness as those used for the CVS experiments. As mentioned in Chapter 2, during SHH injection stress, the gate is biased at a low negative voltage, while the source and drain are tied together and grounded. A high positive voltage is applied to the n-well contact (denoted as V_w), and an even higher positive voltage (V_w + 0.7 V) is applied to the p-substrate contact (denoted as V_b). Under this configuration, a pure stream of hot holes will flow towards the gate oxide. The energy of the hot holes approaching the Si-SiO2 interface is determined by V_w. In other words, by adjusting V_w, we can achieve the desired oxide degradation rate. Carrier separation measurement is carried out before and after the stress to determine the SILC. Figure 3.23 shows the SILC generated by SHH injection stress at $V_g = -1.5$ V, $V_w = 4.0$ V and $V_b = 4.7$ V for 1000 seconds. Interestingly, the gate SILC is observed to consist almost only of the hole SILC, while the electron current component constitutes a very minor component of the gate SILC. This observation supports our hypothesis that the stress-induced oxide trap distribution is highly localized near the Si valence band edge.

Combining the relation between hole SILC and gate SILC generated by CVS and SHH injection stress, we deduce that the type of carrier injected into the oxide and the energy of the injected carrier are the two key factors determining the resultant oxide trap distribution. In CVS, both electrons and holes are injected across the oxide, and the resultant oxide trap distribution is not as highly localized as that resulting from SHH injection stress. As can be seen from Figure 3.16 and 3.17, the electron SILC component is still significant even after the longest stress time. For SHH injection stress, however, mainly hot holes are injected into the gate oxide. The resultant oxide trap distribution is therefore highly skewed towards the Si valence band edge.

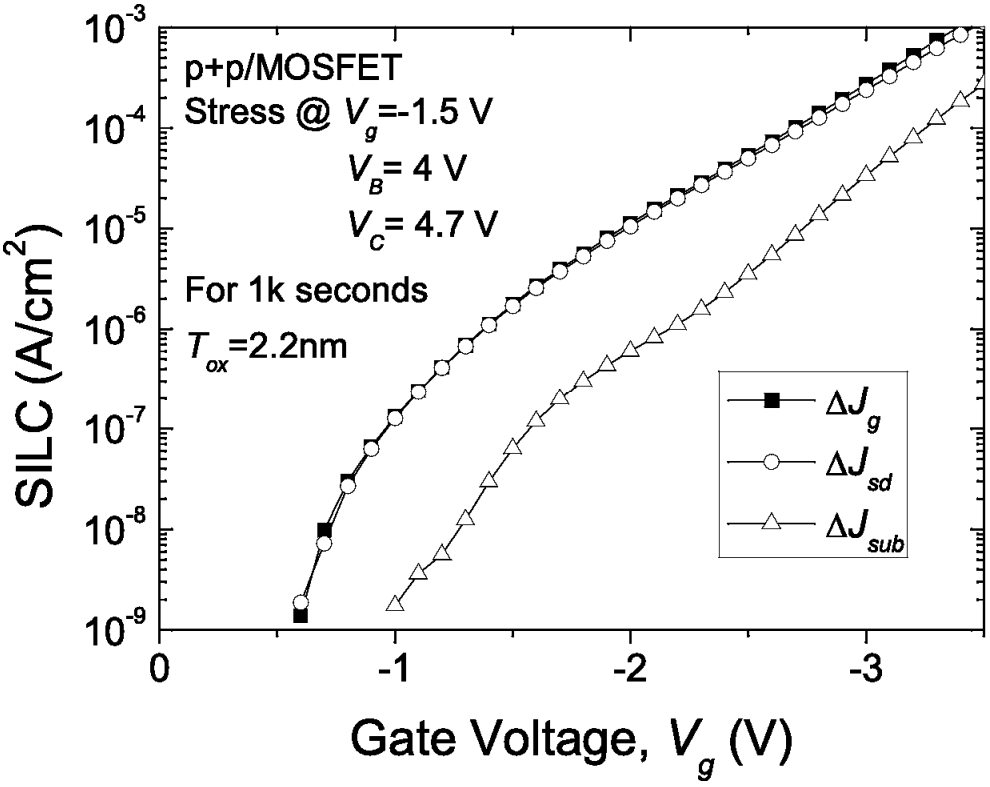

Figure 3.23: Carrier separation curves of a p+/pMOSFET after 1000 seconds of SHH injection. Stress parameters are indicated in this figure.

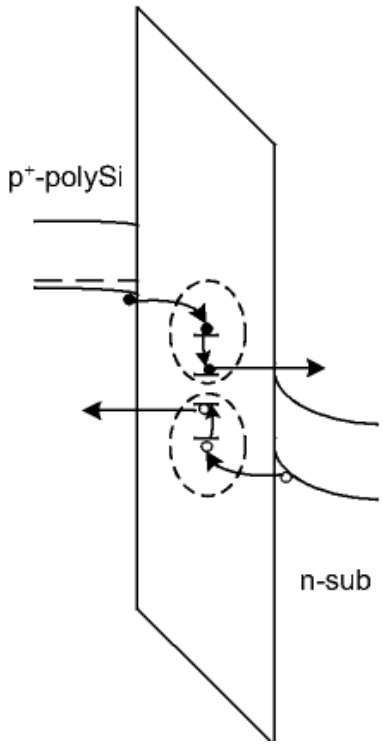

Figure 3.24: TAT process involving multiple steps. An electron (hole) tunnel from a shallow trap to a deep trap before it tunnels out to the conduction (valence) band.

It should be pointed out that Figure 3.20 (b) depicts an extremely simplified physical process. In actual SILC conduction, TAT probably is multi-step. Except for the tunneling in step and the tunneling out step, trapped electrons/holes can interact with the oxide traps, and can tunnel from shallow trap levels to deeper trap levels, as shown in Figure 3.24. Energy is released during the transition from a shallow level to a deep level. This also explains the observation in [16] that SILC tunneling occurs via deep level oxide traps. Electrons/holes tunnel out from deep-level traps, but actually they first tunnel into shallow traps, followed by a transition to deeper traps. Considering these factors, the proposed physical model is compatible with established TAT framework of SILC.

3.7 Summary

SILC in p+/pMOSFET with 2.2 nm nitrided gate oxide, generated by CVS and SHH injection stress has been comprehensively characterized. It is found that hole current component in the gate SILC generated by CVS tends to dominate over the electron counterpart, and the dominance is continuously increased during the stress. In the case of SHH injection stress, the hole current component shows an overwhelming dominance over the electron counterpart. A physical model featuring a localization of oxide traps near the Si valence band is presented to explain the observed evolution of the hole current and electron current components of the gate SILC. This localization of oxide traps near the Si valence band consistently explains the dominance of hole current over its electron counterpart. Such a localized oxide trap distribution is believed to be generated by hole injection into the gate oxide. The presented physical model is consistent with the established TAT framework for SILC.

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Chapter 4

SILC in n+/nMOSFETs with Ultrathin Nitrided Gate Oxides

4.1 Introduction

In the last chapter, SILC in p+/pMOSFETs with ultrathin gate oxide has been comprehensively investigated, from the viewpoint of its electron and hole components. It was found that the hole SILC component dominated the gate SILC in the p+/pMOSFET. A model based on trap-assisted tunneling has been established to explain the dominance of the hole SILC. In this chapter, we will discuss SILC in n+/nMOSFETs with ultrathin gate oxides. SILC in nMOS devices has been the subject of intensive research. However, not much work has been done on gate oxides in direct tunneling region (< 3 nm). In this region, the gate leakage current in a fresh device is already high (for T_{ox} = 2.2 nm at V_g = 1.5 V, $J_g \approx 0.3$ μA/cm^2), and SILC probably will not contribute significant additional leakage. However, since it is widely agreed that SILC is a good indicator of gate oxide degradation, even a relatively low level of this leakage may still convey important information, and thus it merits further study.

We will first discuss the gate leakage current of a fresh n+/nMOS device. Then we present an overview of the gate SILC, and follow up with a detailed investigation from the viewpoint of the evolution of conduction-band electron tunneling and valence-band electron tunneling.

4.2 Gate Leakage Current in Virgin n+/nMOSFETs

When the gate voltage is swept from positive to negative, the n+/nMOS structure experiences inversion, flat band, thermal equilibrium, and accumulation. The 1-D energy band diagrams corresponding to the various surface conditions are schematically shown in Figure 4.1. In strong inversion, electron tunneling from the inversion layer dominates the gate leakage, and depending on the gate voltage, the major contribution will come from either conduction band electron (CBE) tunneling or valence band electron (VBE) tunneling. The gate bias V_g, at which transition from CBE to VBE occurs, is ~5.0 V [1]. When the substrate surface is in accumulation, the number of holes in the accumulation layer should be about the same as that of electrons in the poly-gate, but due to the difference of tunneling barrier, electron tunneling dominates the gate leakage and hole tunneling is negligible. Generally, for n+/nMOS devices, the dominant tunneling carrier is always the electron. This is a big difference between n+/nMOS devices and p+/pMOS devices employing ultrathin gate oxide.

The typical gate leakage characteristics of an n+/nMOSFET with a 2.2 nm gate oxide, biased in the accumulation and inversion modes, are shown in Figure 4.2. The curves were obtained by carrier separation measurement. During measurement in the inversion mode, the source-drain current measures the conduction band electrons tunneling through the gate oxide. As for VBE tunneling, the corresponding holes flow to the substrate, and are measured as J_{sub}. In the inversion region, the CBE component is always almost two orders of magnitude larger than its VBE tunneling counterpart, within the range of gate bias shown in the figure. The gate leakage currents in inversion and in accumulation are plotted in the inset of Figure 4.2. For a certain $|V_g|$, J_g in accumulation is about one order of magnitude smaller than J_g in inversion, due to the effect of the flat band voltage.

4.3 SILC in n+/nMOSFETs

The gate was stressed at a constant voltage of +4.3 V (inversion mode stress). The

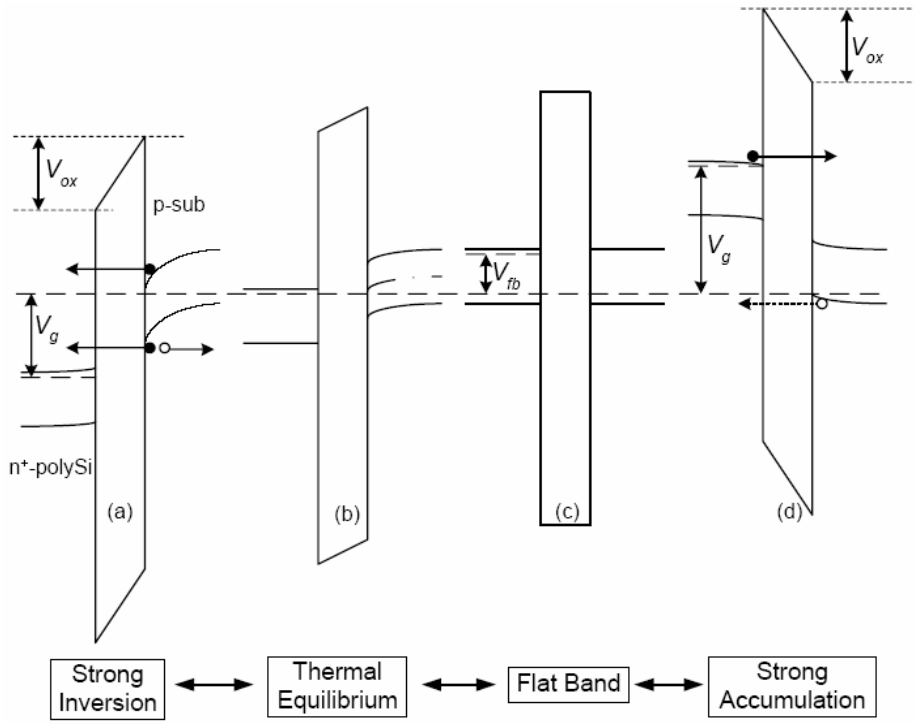

Figure 4.1: Energy band diagrams illustrating the transition from strong inversion to strong accumulation mode of an n+/nMOS device.

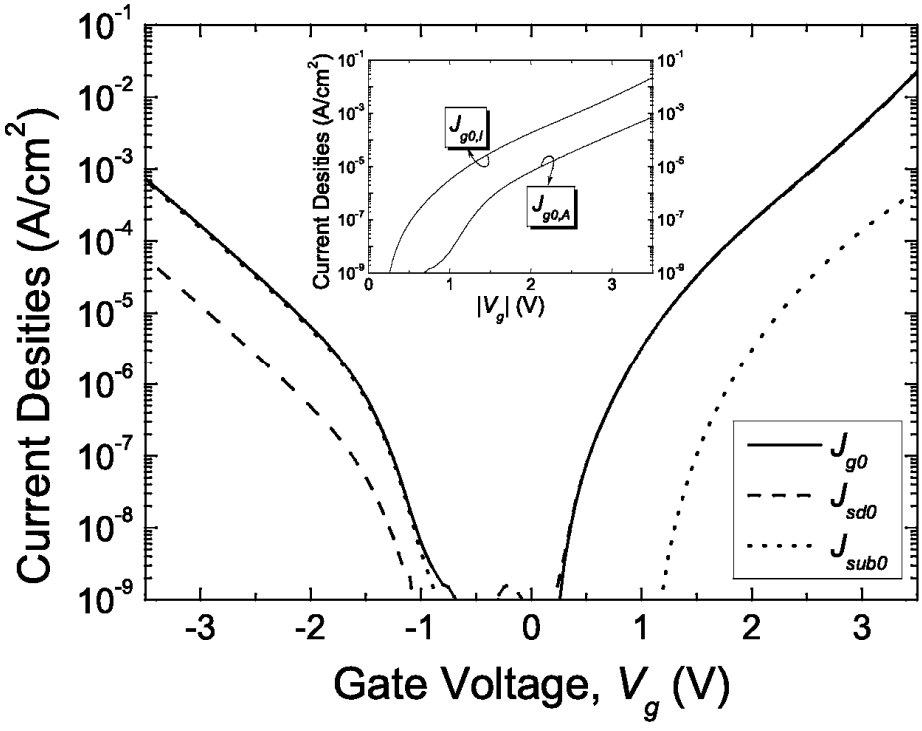

Figure 4.2: Gate leakage current of an n+/nMOSFET with ultrathin gate oxide as a function of gate voltage, from strong accumulation to strong inversion.. In the inset, $J_{g0,I}$ and $J_{g0,A}$ denote gate leakage current in the inversion and accumulation region, respectively. Device dimensions: W = 40 μm, L = 20 μm, T_{ox}= 2.2 nm.

stress was periodically interrupted to measure the gate leakage current. The evolution of the gate leakage current of an n+/nMOSFET with 2.2 nm gate oxide is shown in Figure 4.3 and the corresponding gate SILC is shown in Figure 4.4, for both the accumulation mode and inversion mode. For a certain stress level, the increase of gate leakage current in the accumulation mode is more significant than that in the inversion mode. Furthermore, as the stress time increases, the shape of the J_g-V_g curve in accumulation also changes significantly. At t = 1000 s, the slope of the J_g-V_g curve in accumulation exhibits a distinct change at $V_g \sim -1.0$ V. Note that this is quite close to the value of the flat band voltage of the n+/nMOS device. In other words, this transition point in the gate SILC curve in the accumulation mode can be used as a rough measure of the flat band voltage. The change in the slope happens when the gate voltage sweeps passed the flat band point (Figure 4.1-c), when it increases from zero to negative side. After this point, conduction band electron tunneling from poly-gate to substrate becomes available.

In Figure 4.5, the various components of the gate SILC after t_s = 1000 s stress are shown. In accumulation, the gate SILC mainly comprises the substrate current ΔJ_{sub}, and this is the case even at gate voltage as low as −0.5 V. At such low voltage, electron tunneling from gate to substrate is unlikely to happen since the bottom of the conduction band of the gate poly is aligned with the band gap of the substrate (Figure 4.1-b, c). The only way, by which electron tunneling can happen, is via interface states or oxide traps. Beyond the flat band point, conduction band electron tunneling from poly-gate to substrate dominates. The shift in the slope of $\log(\Delta J_g)$-V_g indicates a change in the conduction mechanism of SILC. This change in the slope was, however, not observed for p+/pMOS devices in the previous chapter.

The change in the slope of the $\log(\Delta J_g)$-V_g curve at $V_g \sim -1$ V becomes more obvious when the normalized gate SILC is plotted against the gate voltage, as shown in Figure 4.6. The gate voltage at which the slope of $\log(\Delta J_g)$-V_g curve changes corresponds well to the peak of the normalized gate SILC. The normalized SILC of p+/pMOS is also shown in the inset of Figure 4.6 for comparison. We see that for both devices, besides the one in the accumulation region ($|V_g| \sim 1.0$ V), there is an additional peak in the weak inversion region at $|V_g| \sim 0.2$ V. The similarity between

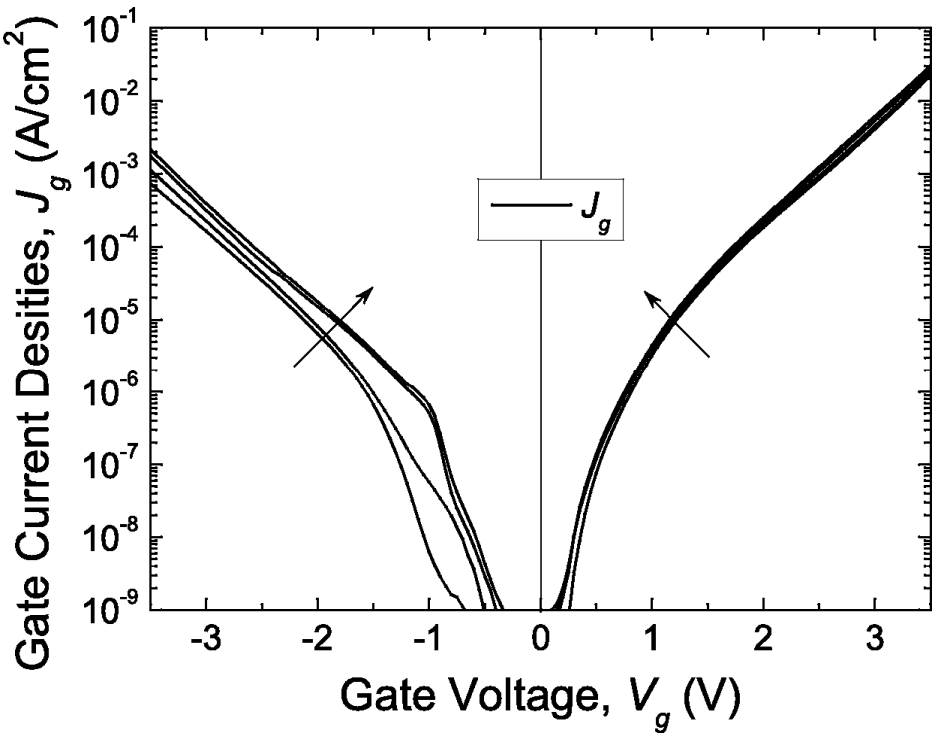

Figure 4.3: Evolution of the gate leakage current in an n+/nMOSFET, after constant voltage stress at V_s = +4.3V. The stress time increases in the direction of the arrow: 0 s (pre-stress), 100 s, 1000 s, and 3000 s.

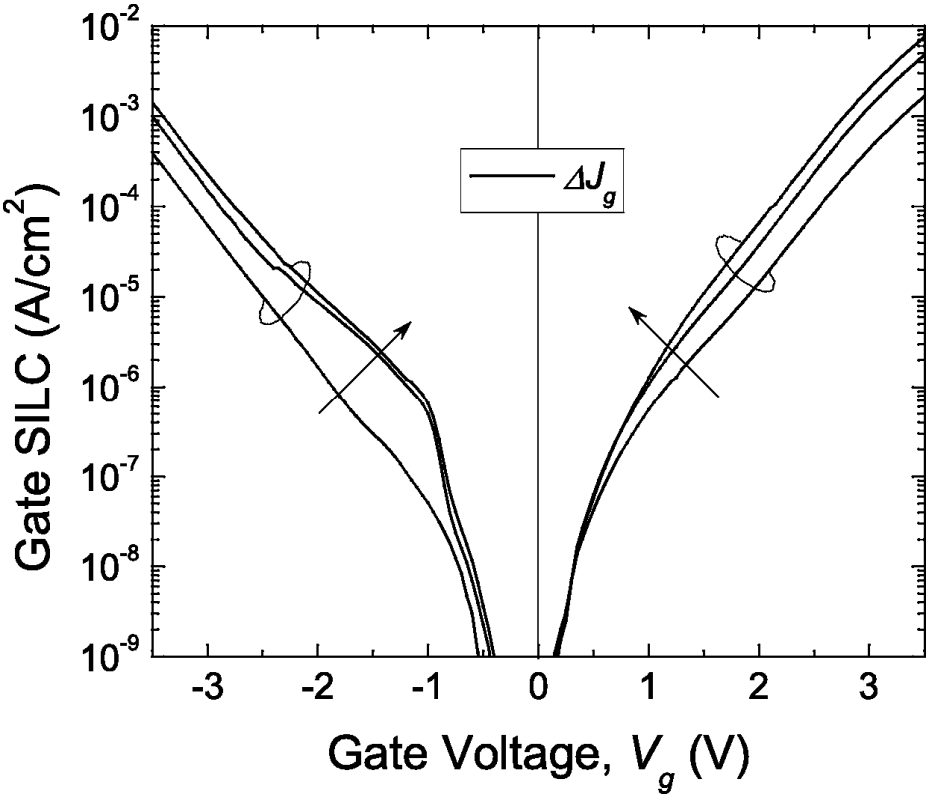

Figure 4.4: Gate SILC of the n+/nMOSFET shown in Figure 4.3, for the accumulation and inversion modes. The stress voltage was +4.3 V. The stress time is 100 s, 1000 s, and 3000 s (same as Figure 4.3) along the direction of the arrow.

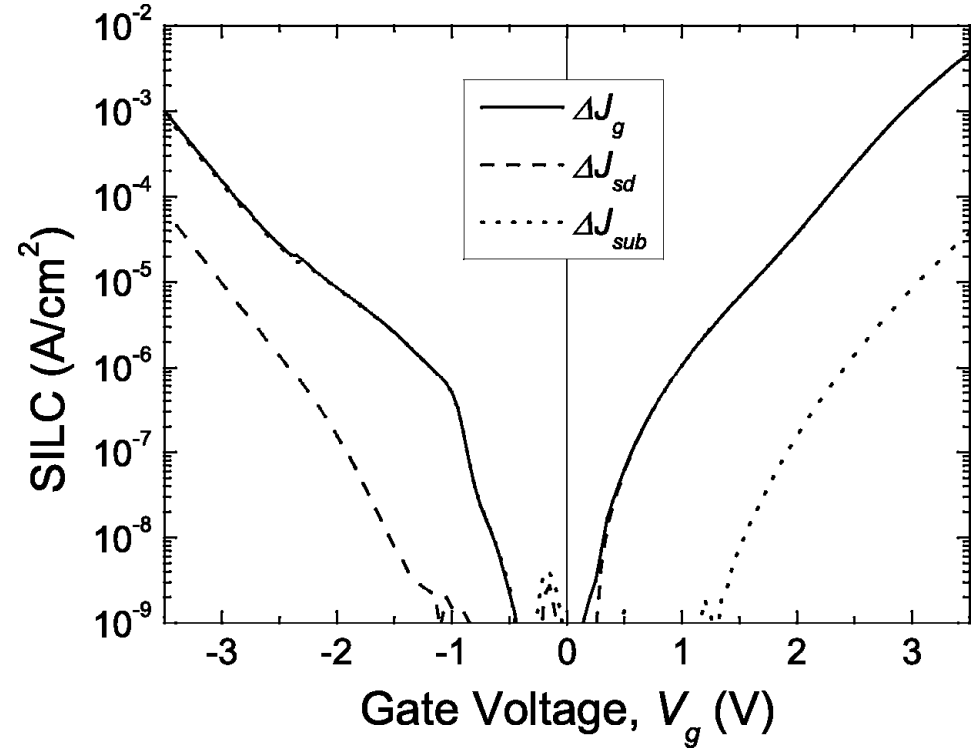

Figure 4.5: Electron and hole SILC characteristics for the accumulation and inversion modes after t = 1000 s stress. The curves are obtained by sweeping the gate voltage from negative to positive.

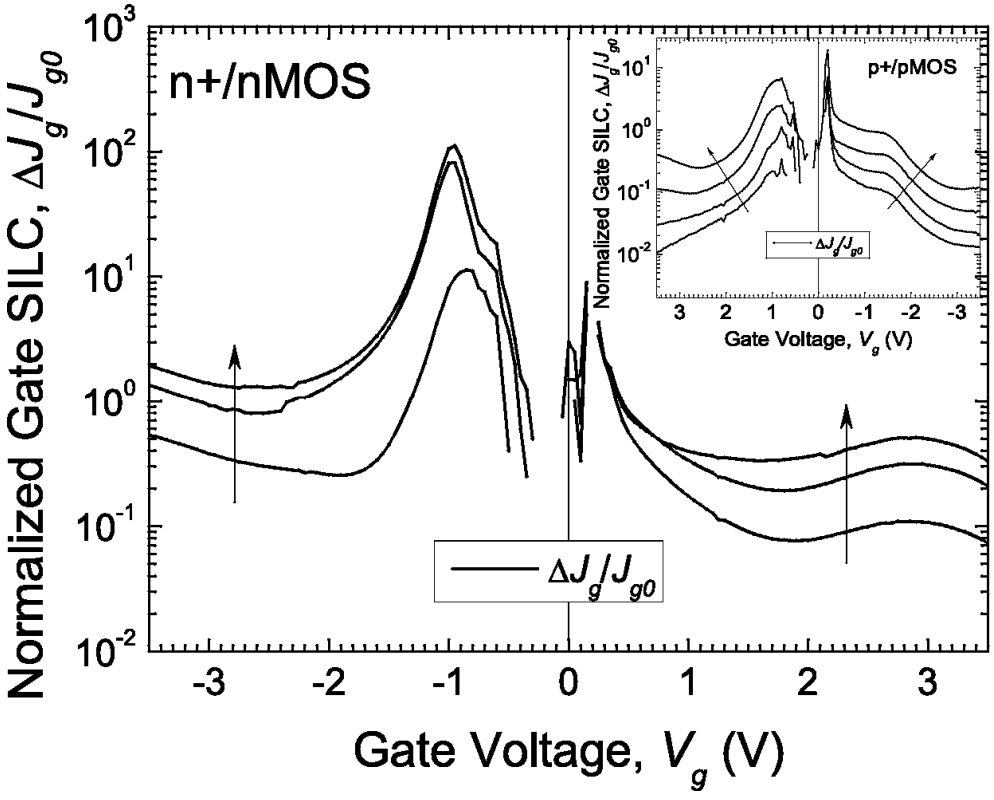

Figure 4.6: Normalized gate SILC as a function of gate voltage, for an n+/nMOSFET following different stress times. J_{g0} denotes the pre-stress gate leakage current, and ΔJ_g denotes the gate SILC. A similar plot for a p+/pMOSFET is also shown in the inset. The stress time increases along the direction of the arrow.

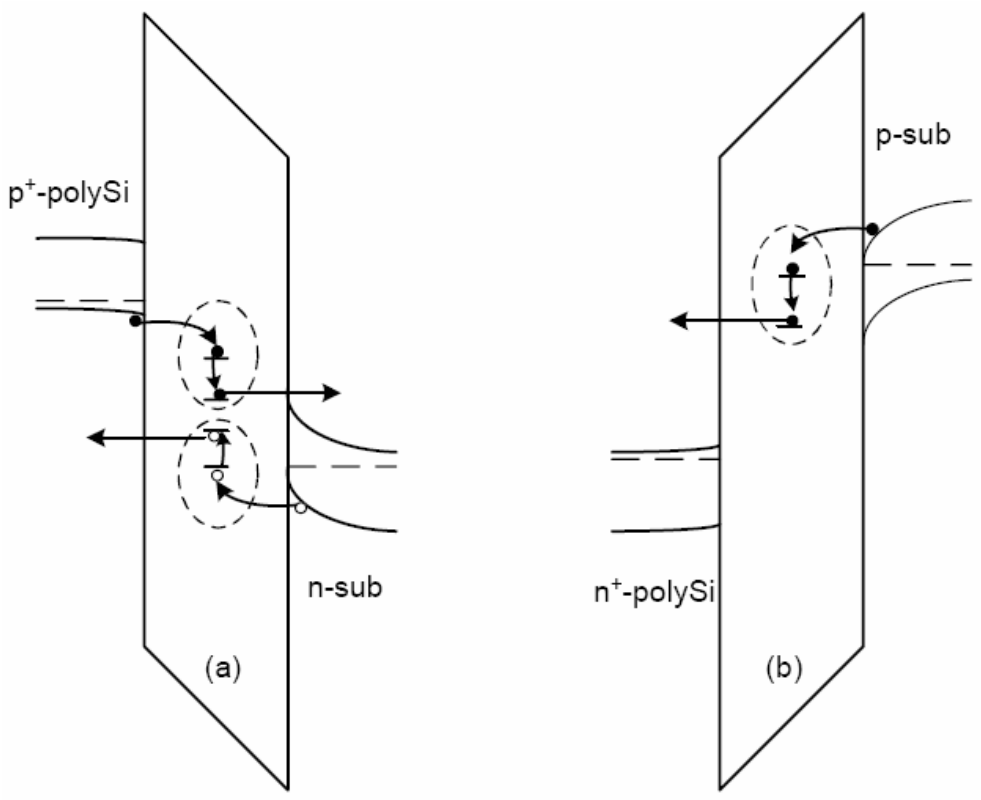

Figure 4.7: Electron and hole TAT process via stress-induced oxide trap (under strong inversion), for (a) p+/pMOS and (b) n+/nMOS, respectively.

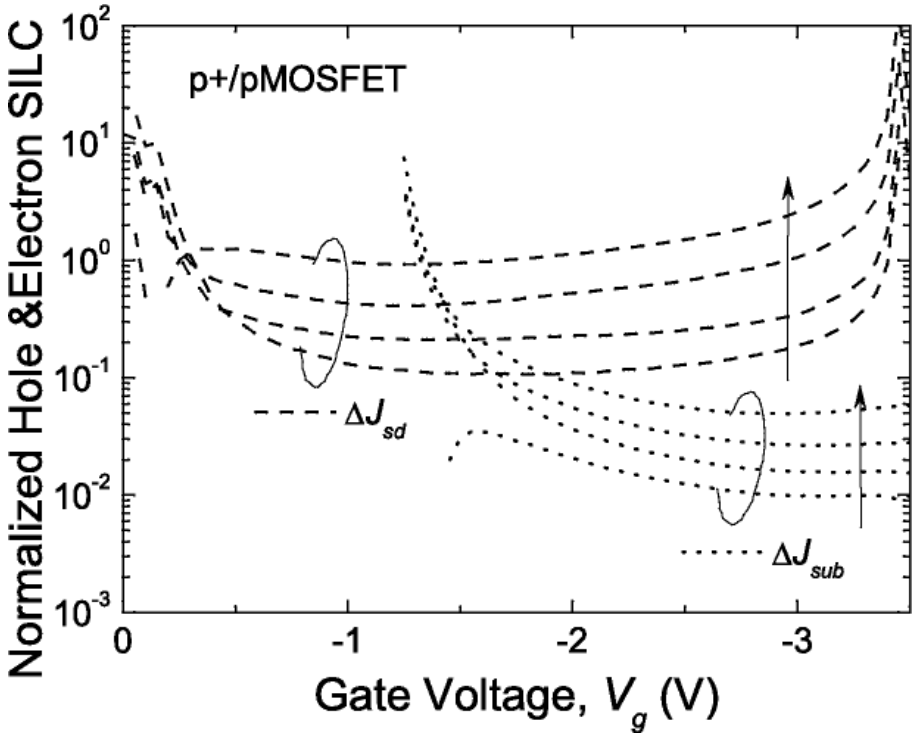

Figure 4.8: Normalized hole SILC and electron SILC in a p+/pMOSFET, for different stress times. The electron SILC in the low gate sense voltage ($|V_g| < 1.2$ V) regime is not shown, for the electron current in this voltage range is negligible. The Cumulative stress time increases along the direction of the arrow.

p+/pMOS and n+/nMOS shown in Figure 4.6 suggests a common mechanism for the ultra-low voltage SILC in these two devices. Further research work is needed to further understand the stress-induced current conduction in this region [2].

Unlike in the accumulation mode, the gate SILC (ΔJ_g-V_g) curve does not display a slope change in the inversion mode. This can be attributed to the fact that carriers involved in the SILC of n+/nMOS in inversion are mainly CBE, with very limited VBE involved. CBE tunneling via a TAT (trap-assisted tunneling) mechanism has been shown to successfully model the SILC in this region [3] - [5]. As shown in Figure 4.6, when the gate voltage is high enough, the ($\Delta J_g/J_{g0}$)-V_g curves for different stress time are parallel to each other. For a given stress level, the normalized gate SILC is rather insensitive to the gate sense voltage, for V_g > 1.5V. In this region, the amount of CBE available for tunneling is huge, and does not limit the tunneling leakage current. The density of stress-induced oxide traps, which is reflected by the normalized SILC, becomes the determining factor. The insensitivity of the normalized SILC to the gate sense voltage in Figure 4.6 indicates that the oxide trap density sensed by SILC at different gate sense voltage is almost identical. This is in contrast to the p+/pMOS case, where the oxide trap density sensed by SILC is highly dependent on the gate sense voltage (inset of Figure 4.6). The difference may have arisen from the different energy distributions of the stress-induced oxide traps of these two devices. In Chapter 3, we propose that for the p+/pMOS devices there are two separate oxide trap distributions responsible for the hole SILC and electron SILC. While for n+/nMOS device, electron SILC is predominant and there is actually negligible hole tunneling current in the gate leakage current. This implies that the energy distribution of stress-induced oxide traps in the n+/nMOS device is one sided, as shown in Figure 4.7-b. A further confirmation of this implication can be found in Figure 4.8, in which the normalized hole SILC and electron SILC of a p+/pMOSFET are plotted together as functions of the gate sense voltage. The normalized hole SILC of a p+/pMOSFET is quite insensitive to the gate sense voltage, similar to the normalized gate SILC of the n+/nMOSFET shown in Figure 4.6. However, the normalized electron SILC decreases significantly as the gate sense voltage increases, which is also responsible for the overall decreasing trend of the normalized gate SILC

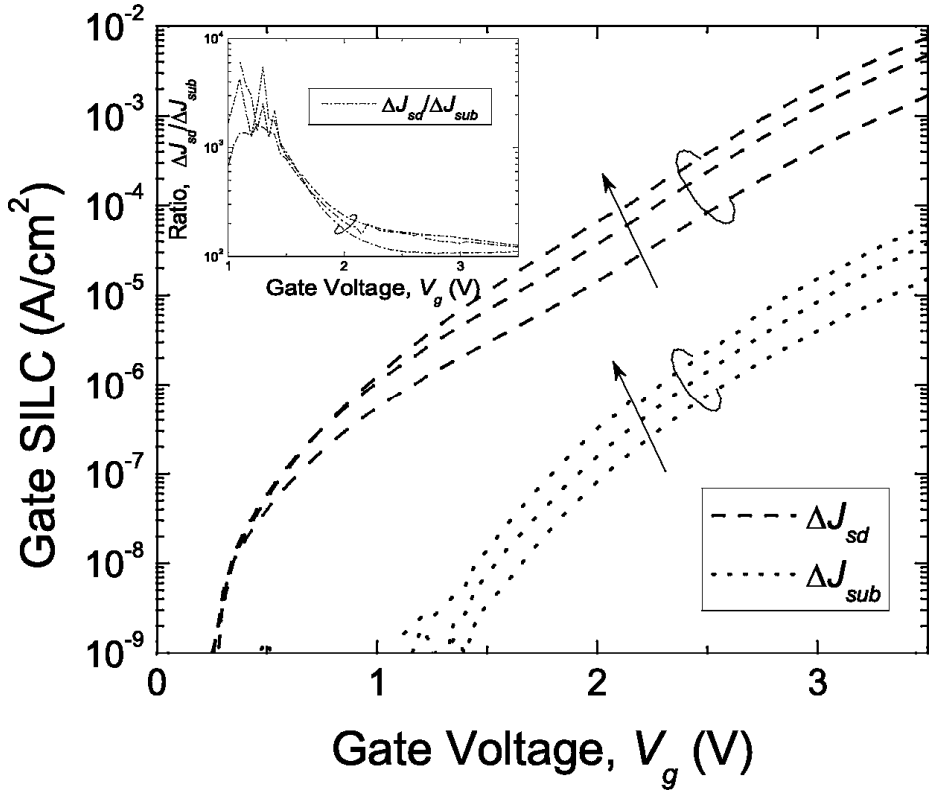

Figure 4.9: Increase in the CBE tunneling current (ΔJ_{sd}, dashed lines) and VBE tunneling (ΔJ_{sub}, doted lines) in of an n+/nMOSFET with 2.2 nm gate oxide.

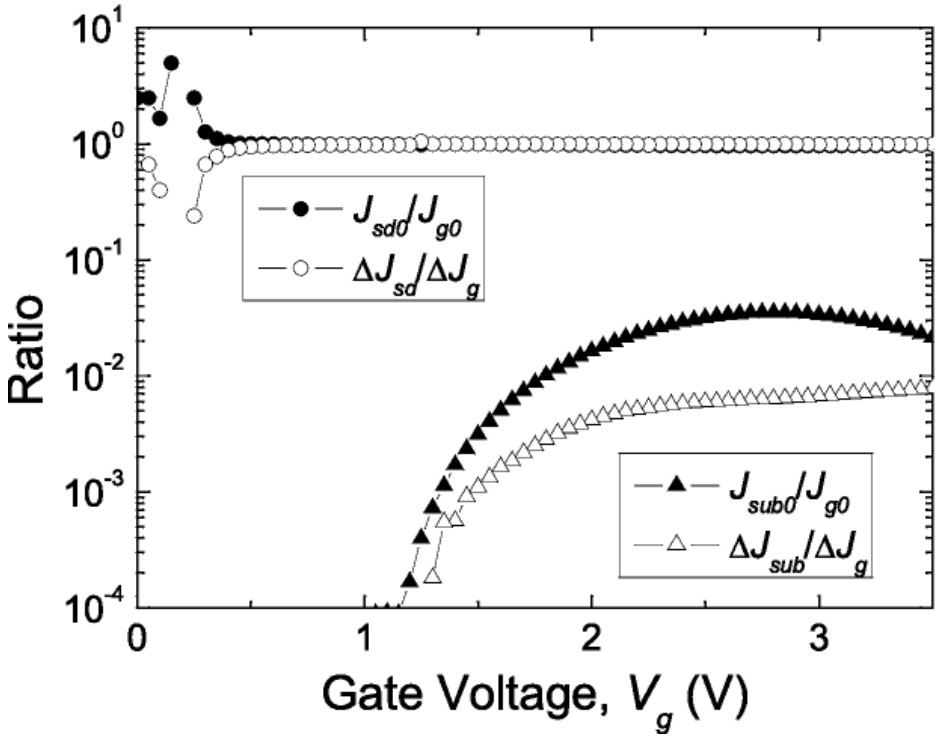

Figure 4.10: The ratio of CBE tunneling current to the gate leakage current of a fresh device (solid circle), and to the in gate SILC of a stressed device (open circle). The corresponding ratios for the VBE tunneling current are also shown. Stress time t = 1000 s.

of the p+/pMOSFET shown in the inset of Figure 4.6.

As indicated in Figure 4.5, SILC in the n+/nMOS device is mainly dominated by the conduction band electron tunneling current, and the contribution of valence-band electrons or holes is negligible. In Figure 4.9 the stress-induced evolution of the CBE tunneling component as well as the VBE tunneling component is shown. We can see that after every stress interval, the CBE tunneling component is as least 2 orders larger than the VBE tunneling component. Moreover, the ratio is not sensitive to stress time. The ratio of CBE (J_{sd0}) tunneling to pre-stress gate leakage (J_{g0}), and of stress-induced CBE (ΔJ_{sd}) tunneling to gate SILC (ΔJ_g), is shown in Figure 4.10. For both cases, the contribution due to CBE tunneling is very close to 100%. But for the VBE tunneling component (J_{sub0}/J_{g0} and $\Delta J_{sub}/\Delta J_g$), also shown in the same figure, the contribution to the gate leakage is typically less than 5%. Furthermore, the contribution is further reduced after stress, i.e. $(\Delta J_{sub}/\Delta J_g) < (J_{sub0}/J_{g0})$. VBE tunneling can, therefore, be neglected over the voltage range of interest. This further indicates that in the n+/nMOS device, the oxide trap distribution is localized near the E_c of the Si band gap.

4.4 Summary

SILC in n+/nMOSFETs with ultrathin nitrided gate oxide (2.2 nm) is characterized and compared to that in the p+/pMOSFETs. It is found that SILC in n+/nMOS devices is dominated by conduction-band electron tunneling. Furthermore, the TAT process in n+/nMOS is probably facilitated by a one-sided stress-induced oxide trap distribution localized near the E_c Si band gap.

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Chapter 5

Degradation of Ultrathin Nitrided Gate Oxides

5.1 Introduction

In the previous two chapters, we discussed the SILC in p+/pMOS and n+/nMOS devices with ultrathin gate oxide, from a viewpoint of evolution of its electron and hole components. p+/pMOS devices were found to display a gate SILC which was progressively dominated by the hole current, as the stress time was increased. On the other hand, for n+/nMOS devices, the gate SILC was always dominated by the conduction-band electron tunneling current.

It is widely accepted that SILC can be correlated to oxide degradation. In the previous chapters, we have shown the shift in the J_g-V_g characteristic induced by stress, without quantifying the increase in the gate leakage current. In this chapter, we will focus on the degradation process of ultrathin gate oxides, by investigating the generation rate of SILC under constant voltage stress.

5.2 Gate Stress Current and Gate Sense Current

As discussed in Chapter 2, a constant voltage stress was used to generate SILC in our experiments, and the stress current was always recorded for quantitative evaluation of the relationship between SILC and charge injection. In Figure 5.1, the recorded gate stress current ($J_{s,g}$) is shown as function of stress time (t_s), for a

p+/pMOSFET. $J_{s,g}$ exhibits a strong oscillatory behavior after each cycle of stress, consistent with an earlier observation [1]. This behavior was explained by the relaxation of trapped positive charges after the stress voltage was withdrawn. The gate sense current $J_{g,-1.5}$, measured at $V_g = -1.5$ V after each cycle of stress, is also shown, displaying a similar increasing trend with stress time. The gate sense current curve exhibits slight perturbations. Both the gate stress current and gate sense current increase dramatically in the initial stage of stress, and tend to saturate at long stress time. The gate sense current shows a peak at about $t_s = 5000$ s, and drops continuously in the next few cycles before it increases again. This again indicates the instability of stress-induced trapped charges and traps in p+/pMOS devices.

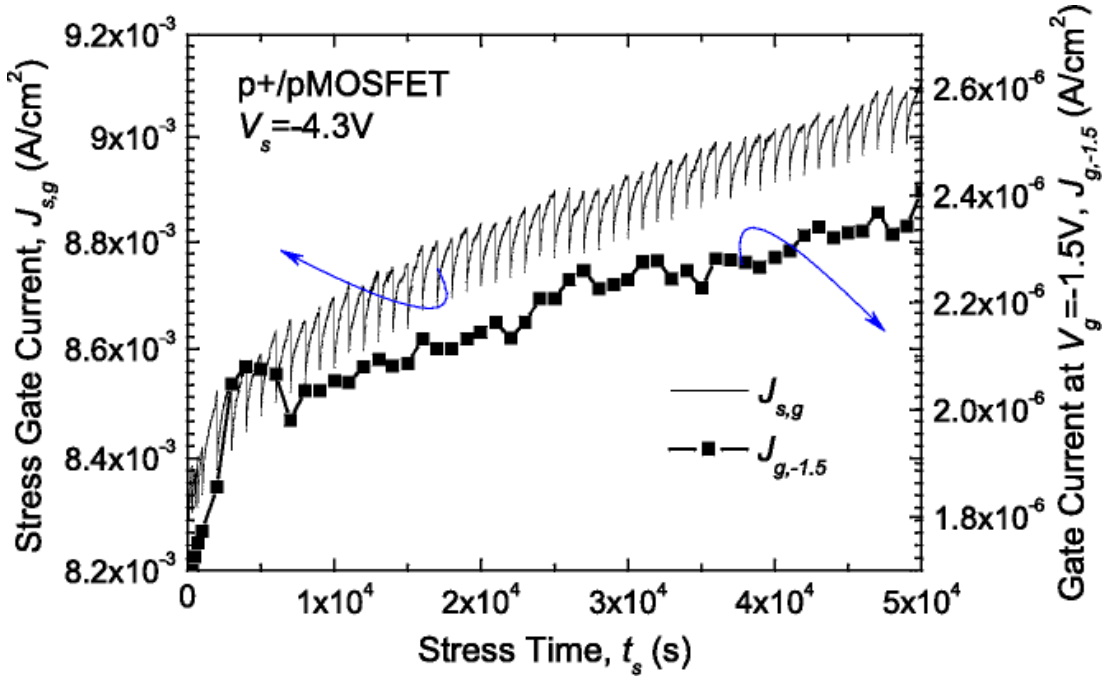

Figure 5.1: Recorded gate current during constant voltage stress and gate sense current after each cycle of stress, for a p+/pMOSFET. Gate area is 40 × 20 μm^2, and the gate oxide thickness is 2.2 nm.

For the case of n+/nMOS device, we observe similar oscillatory characteristics, in Figure 5, for both gate stress current and gate sense current, before oxide breakdown. This indicates that the partial relaxation of stress-induced effects is common to both p+/pMOS and the n+/nMOS devices. In our stress and measurement scheme, the process is repeated until the gate oxide breaks down. Note that for an n+/nMOS device with such thin gate oxide (2.2 nm) and stressed under such high voltage

(+4.3 V), the time-to-breakdown is about 3 x 10^3 s. The p+/pMOS counterpart, stressed under the same voltage (−4.3 V), did not break down even for stress times up to 10^5 seconds. This should be expected since the stress current for n+/nMOS is about two orders larger than that for p+/pMOS.

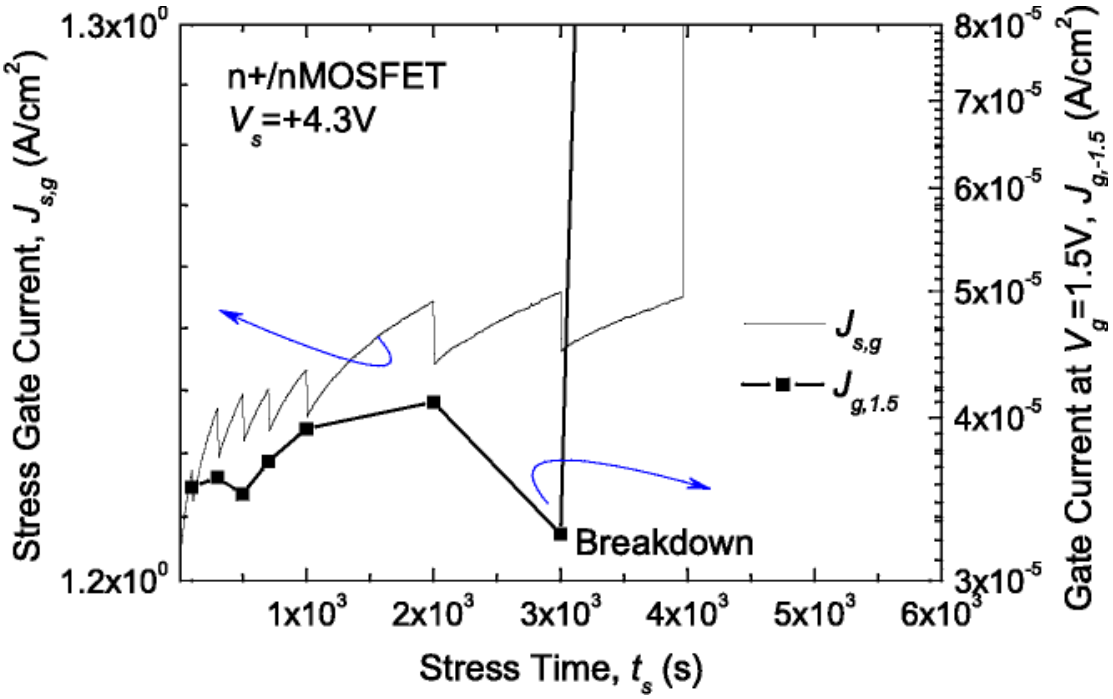

Figure 5.2: Recorded gate current during constant voltage stress and gate current after each cycle of stress, for an n+/nMOSFET. Gate area is 40 × 20 μm^2, and the gate oxide thickness is 2.2 nm.

5.3 SILC Generation and Oxide Degradation

By integrating the stress gate current shown in Figures 5.1 and 5.2, we obtain the amount of charges injected (Q_{inj}) across the gate oxide for a given stress time. Shown in Figures 5.3 and 5.4 are the normalized gate SILC as a function of charge injection, for p+/pMOS and n+/nMOS, respectively. For both devices, the relationship between the normalized gate SILC and charge injection can be described by a linear function in the log-log scale [2]. According to this correlation, for a given gate sense voltage

$$\log \frac{\Delta J_g}{J_{g0}} = k \cdot \log Q_{inj} + C \,, \tag{5.1}$$

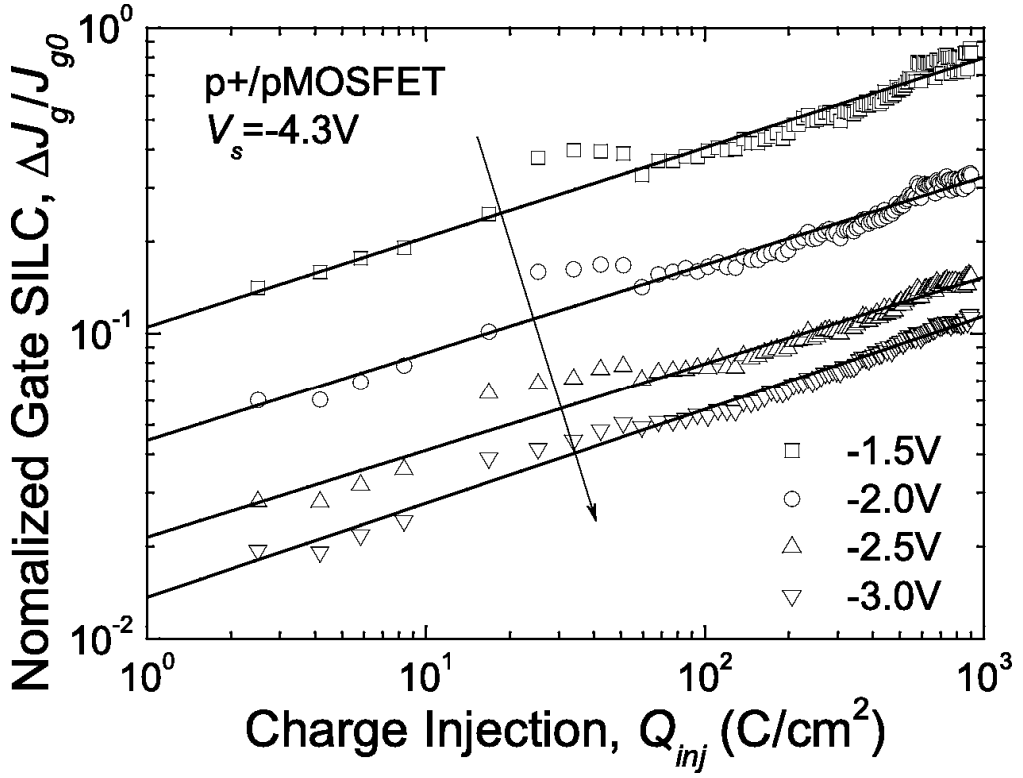

Figure 5.3: Normalized gate SILC as a function of charge injection, with the gate sense voltage as the parameter. The p+/pMOSFET was stressed −4.3 V.

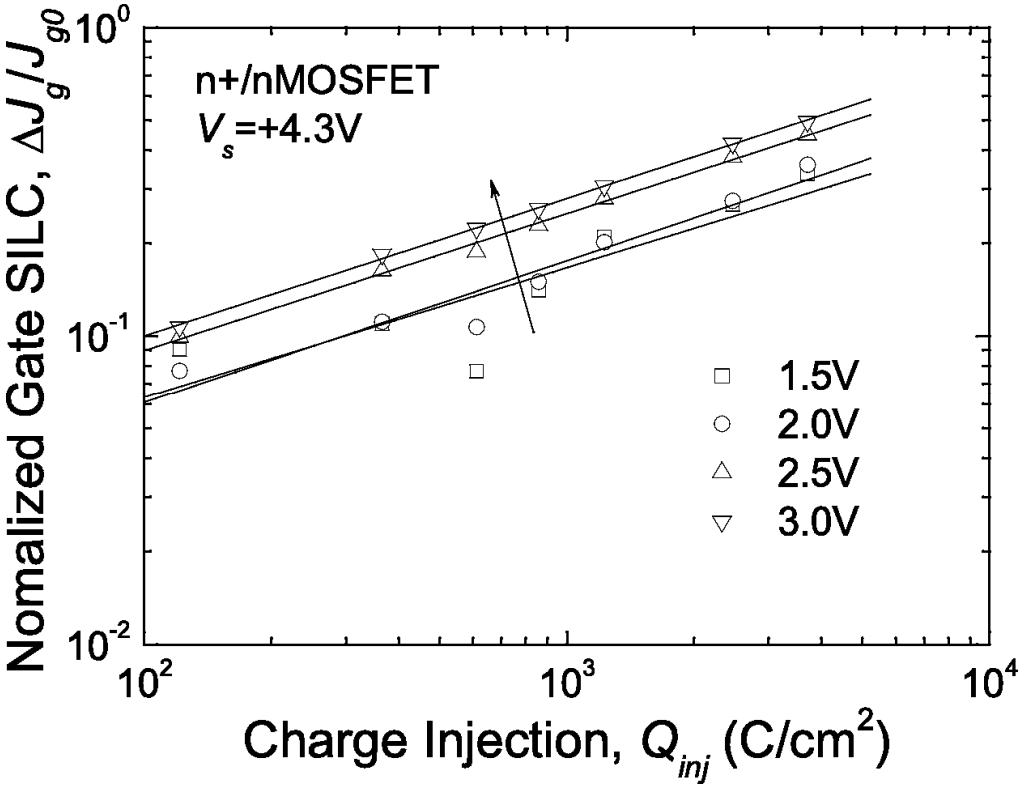

Figure 5.4: Normalized gate SILC as a function of charge injection, with the gate sense voltage as the parameter. The n+/nMOSFET was stressed +4.3 V.

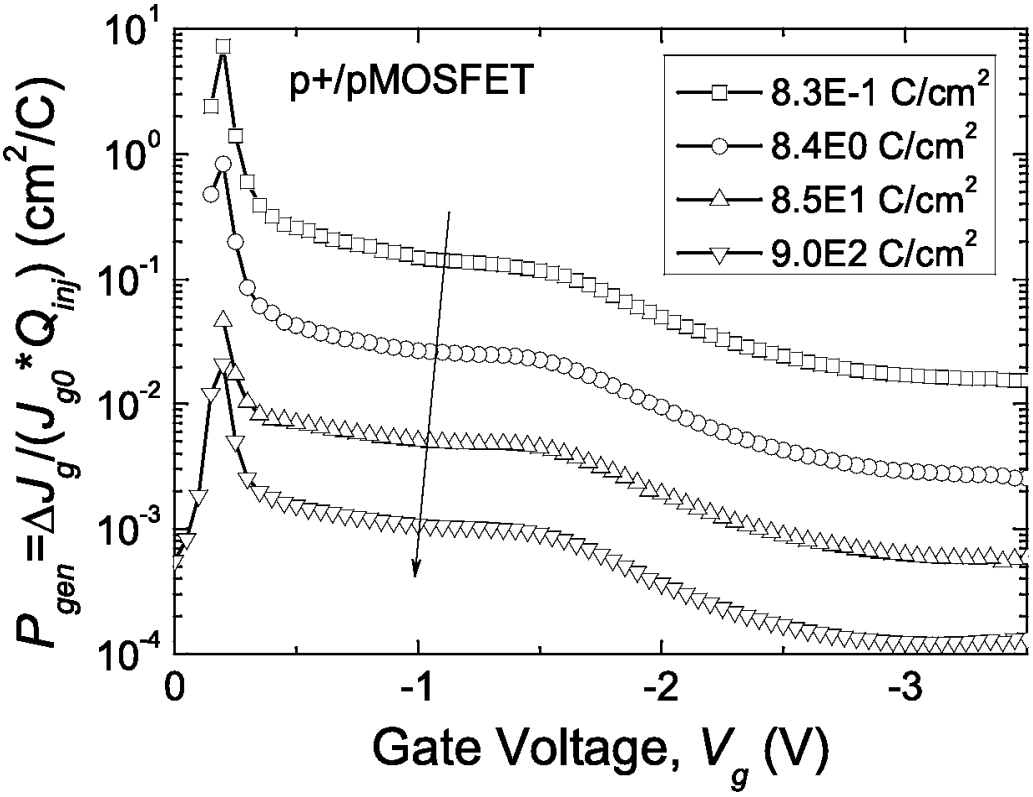

Figure 5.5: SILC generation probability as a function of gate sense voltage, for different charge injection levels. The p+/pMOSFET was stressed at −4.3 V.

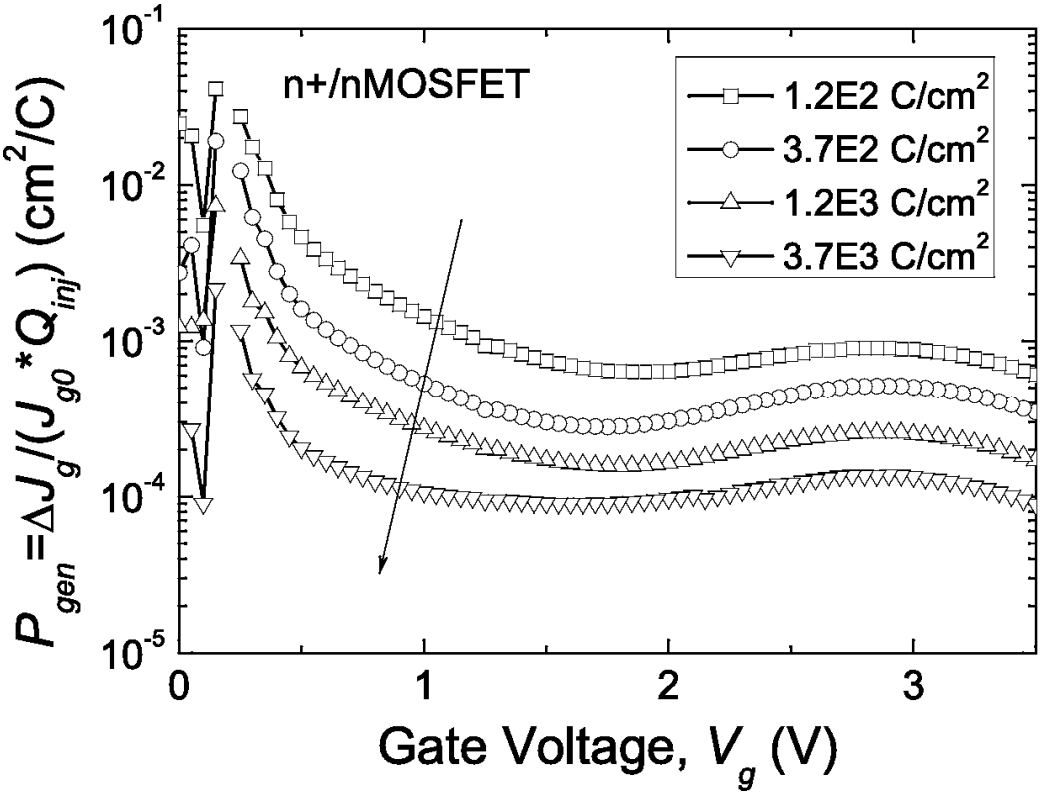

Figure 5.6: SILC generation probability as a function of the gate sense voltage for different charge injection levels. The n+/nMOSFET was stressed at as +4.3 V.

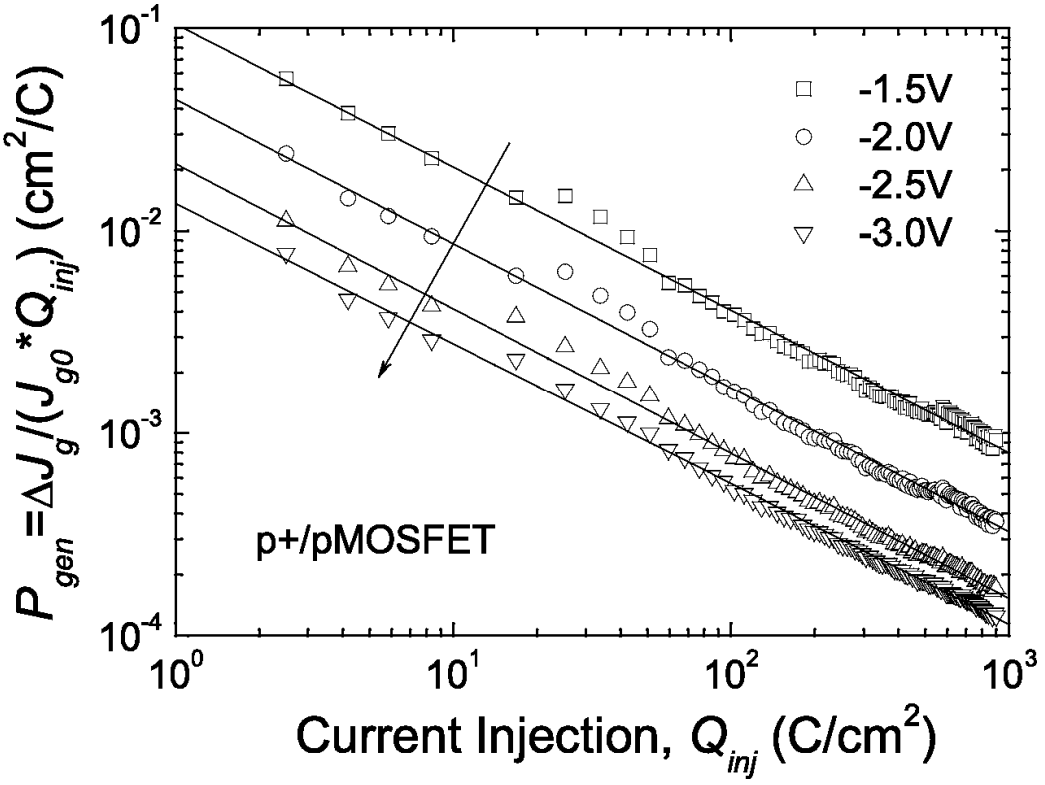

Figure 5.7: SILC generation probability as a function of charge injection, for different gate sense voltages. The p+/pMOSFET was stressed at −4.3 V.

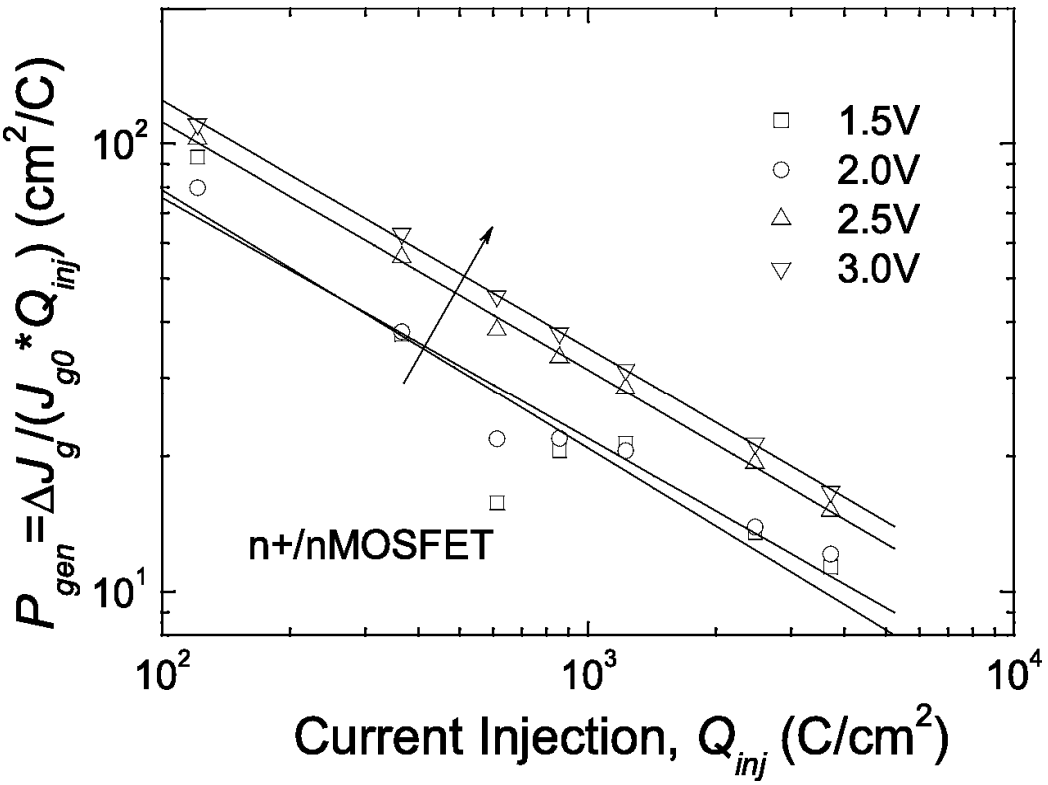

Figure 5.8: SILC generation probability as a function of charge injection, for different gate sense voltages. The n+/nMOSFET was stressed at +4.3 V.

where k and C denote the slope and the y intercept, respectively. From Figures 5.3 and 5.4, we note that k is not sensitive to sensing voltage. The value of k is about 0.30 for p+/pMOS and 0.44 for n+/nMOS. A larger k value for the n+/nMOS device indicates a faster degradation of gate oxide, consistent with the much shorter time-to-breakdown compared to the p+/pMOS device. The value of C is determined by the gate sense voltage. As indicated by the arrows in Figures 5.3 and 5.4, for the p+/pMOS device, C decreases as sensing voltage increases, while for the n+/nMOS device, the opposite applies. This is due to the fact that, for the p+/pMOS device, normalized gate SILC decreases as sensing voltage increases, while for the case of the n+/nMOS device, there exists a reversion region (refer to Chapters 3 and 4).

The SILC generation probability (P_{gen}) is defined as the normalized SILC generated per unit of injected charge. It can be easily obtained by multiplying the normalized gate SILC with the reciprocal of charge injection [3] - [5]

$$P_{\text{gen}} = \Delta J_{\text{g}} / (J_{\text{g0}} \cdot Q_{\text{inj}}) . \tag{5.2}$$

It is a good indicator of bulk defect generation probability at certain charge injection level [5]. As shown in Figure 5.5 to Figure 5.8, P_{gen} is dependent on the gate sense voltage as well as the charge injection level for both devices. For the p+/pMOS device, it decreases monotonically as the gate sense voltage increases. For the n+/nMOS device, P_{gen}-V_{g} basically exhibits a decreasing trend but there is a slight reversal from about V_g = 2.0 V to V_g = 3.0 V. Furthermore, P_{gen} becomes less sensitive at higher charge injection level. The SILC generation probability of p+/pMOS (n+/nMOS) device as a function of charge injection at different sensing voltages is shown in Figure 5.7 (Figure 5.8). For both devices, P_{gen} is a linearly decreasing function of Q_{inj} in the double-log scale. Thus, we can relate the SILC generation probability empirically to charge injection:

$$P_{\text{gen}} \propto Q_{\text{inj}}^{-x} , \tag{5.3}$$

where x indicates the slope of the plotting P_{gen} versus Q_{inj} in double-log scale, with a value of about 0.70 and 0.55, for p+/pMOS and n+/nMOS, respectively.

5.4 Driving Force of Oxide Degradation

Comparing Figure 5.1 and 5.2, we notice that for the same stress voltage in the inversion mode, n+/nMOS break down more easily compared to p+/pMOS, and exhibits several-orders higher SILC generation probability for a certain charge injection. There are two factors contributing to this difference: stress current density and carrier energy. The higher the stress current, the faster is the rate of oxide degradation. Similarly, more energetic carriers result in a shorter time-to-breakdown. As shown in Figures 5.1 and 5.2, the stress current density for n+/nMOS is at least two orders of magnitude larger than that for p+/pMOS. Furthermore, the energy barrier for valence band carrier tunneling (p+/pMOS case) is about 1 eV higher than conduction band electron tunneling (n+/nMOS case). There is still controversy on the main driving force of oxide degradation: Current or voltage. At this stage, it is difficult to decouple the impact of these two factors.

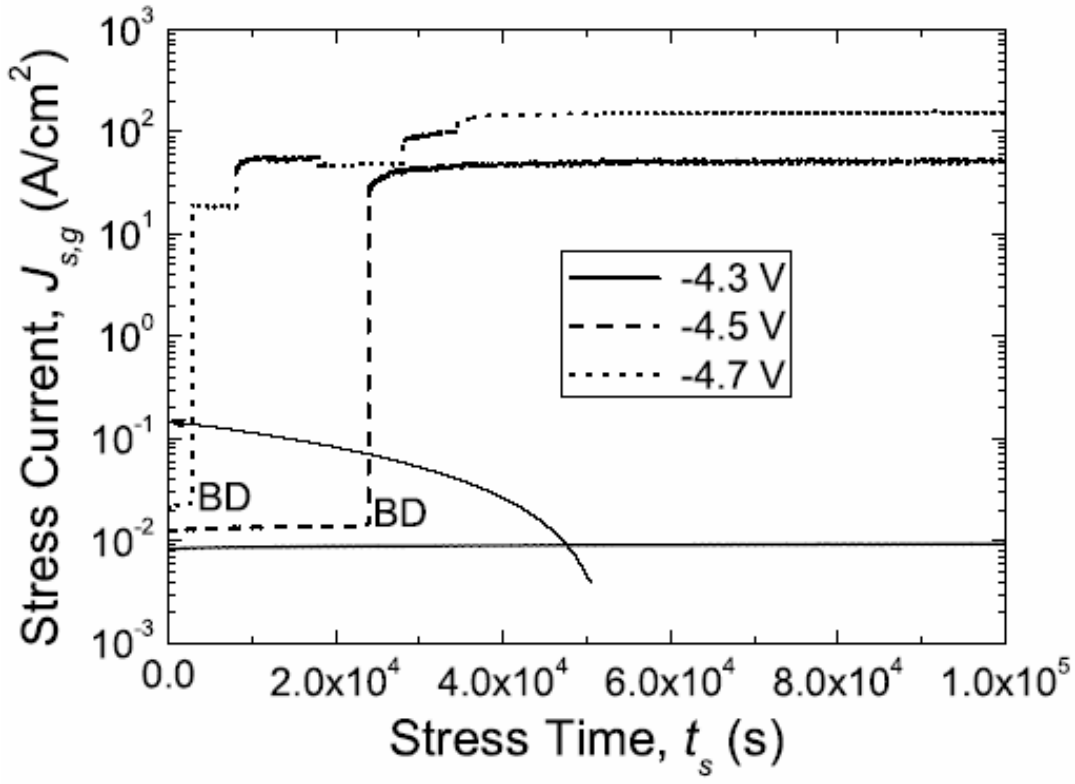

Figure 5.9: Evolution of stress gate current under different stress voltages: −4.3 V (solid line), −4.5 V (dashed line) and −4.7 V (dotted line). Stress is periodically stopped for SILC measurement.

In Figure 5.9, the increase in the gate current under three stress voltages is compared for a p+/pMOS device. When stress voltage slightly increases from −4.3 V to −4.5 V or form −4.5 V to −4.7 V, the time-to-breakdown of gate oxide is greatly shortened. For V_s = −4.3 V, no sign of breakdown was observed even after as long as 10^5 seconds, which is the maximum time allowed by our stress/measurement program. Since the energy of the tunneling carriers is a linear function of gate voltage, the energy change of 0.2 eV is unlikely to be responsible for the great reduction in the time-to-breakdown. On the other hand, a small change in the stress gate voltage translates into an exponential change in the stress current, implying that the current may play a more important role than voltage in the oxide degradation process.

5.5 Summary

In this chapter, the degradation process of ultrathin nitrided gate oxides under constant voltage stress is characterized through monitoring the evolution of SILC with stress time. Both the p+/pMOS and n+/nMOS devices demonstrated partial recovery of degradation after the withdrawal of stress voltage, prior to oxide breakdown. The degradation rate of gate oxide for a given charge injection level can be well predicted by Equation (5.1). The SILC generation probability shows very strong dependence on charge injection, in accordance with Equation (5.3). The sharp decrease in the SILC generation probability at high charge injection level indicates that neutral oxide trap generation tends to saturate at high stress level. Finally, from the stress voltage dependence of the time-to-breakdown of the p+/pMOS device, it is found that the degradation of ultrathin nitrided gate oxide is more current driven than voltage driven.

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Chapter 6

Conclusions and Future Work

6.1 Conclusion

SILC in p+/pMOSFET with 2.2 nm nitrided gate oxide generated by CVS and SHH injection has been characterized from a viewpoint of evolution of hole and electron component. It is found that hole current in SILC generated by CVS tends to dominate over electron current, and such a tendency of hole dominance is enhanced continuously during the stress. In SILC generated by SHH injection, hole current shows overwhelming dominance over electron current. A physical model featuring two separate energy distributions of oxide trap, which favors hole tunneling, is presented to explain the observed evolution of hole current and electron current in SILC. Oxide trap localization near substrate valence band is probably responsible for dominance of hole current. Such a localized trap distribution should be generated by hole injection into the gate oxide. The presented physical model is consistent with the established TAT framework for SILC.

SILC of n+/nMOSFET is found to be dominated by conduction-band electron tunneling. Furthermore, the TAT process of SILC in n+/nMOS is probably facilitated by a one-sided stress-induced trap distribution near the substrate conduction band edge, consistent with the model presented for SILC of p+/pMOSFET.

Degradation of the ultrathin gate oxide process can be well visualized by the generation and increase of SILC. Before oxide breakdown happens, both p+/pMOS and n+/nMOS demonstrated the partial recovery of degradation after the withdrawal

of stress voltage but before the oxide breakdown. The degradation rate of gate oxide for a certain charge injection level can be well predicted by Equation (5.1). SILC generation probability shows very strong charge injection dependence, which can well fit Equation (5.3). The sharp decrease of SILC generation probability at high charge injection indicates that neutral oxide trap generation tends to saturate at high stress level. Finally, from the stress voltage dependence of the time-to-breakdown of p+/pMOS, it is found that degradation of ultrathin nitrided gate oxide is more current driven than voltage driven.

6.2 Future Work

Further efforts are needed to achieve a complete understanding of SILC generation in ultrathin nitrided gate oxide, including polarity dependence, temperature dependence and dynamic stress induced leakage. It has also been demonstrated in this report that there is a possibility to unify the degradation of ultrathin gate oxides in p+/pMOS and n+/nMOS devices into one framework, which features oxide trap generation and build-up near valence band edge (p+/pMOS) or conduction band edge (n+/nMOS).

It will be very meaningful if this work can be extended to high-k materials, which is expected to replace nitrided oxide as gate dielectric in later generation of MOS technologies.