ADVANCED GATE STACK FOR SUB - 0.1 μm CMOS TECHNOLOGY

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SUMMARY

With the continuous scaling of the CMOS devices, the conventional poly-Si/SiO_2 gate stack shall be phased out, and advanced gate stack have to be developed to adapt to this change. The scope of this thesis emphasizes on studies of advanced gate stack for future nano-meter CMOS device application.

For ALD $(HfO_2)_x(Al_2O_3)_{1-x}$ high-K dielectrics, the materials properties including the energy band alignment to (100) Si substrate and the thermal stability have been studied. The energy gap E_g for $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset ΔE_v, and the conduction band offset ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100) Si substrate were studied based on high-resolution XPS measurement. It is also found that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al to form Hf aluminates, and the improvement is closely correlated with the Al percentage in the films. This observation is explained by (i) Al_2O_3 has much lower oxygen diffusion coefficient than HfO_2 at high temperature; (ii) doping HfO_2 by Al raises the film crystallization temperature of HfO_2 and thus drastically reduces the oxygen diffusion along the grain boundaries during annealing.

In this thesis, it is firstly reported a systematic study on novel HfN metal gate electrode for advanced CMOS devices applications. By using HfN metal gates, the devices with either SiO_2 or HfO_2 gate dielectrics demonstrate the robust resistance against high temperature RTA treatments (up to 1000°C), in terms of EOT, work function, and leakage current stability. It is also found that HfN metal possesses a mid-gap work function value. This superior electrical stability is attributed to the

excellent oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 and HfN/SiO_2 interface. Further, the high quality HfN/HfO_2 gate stack's EOT has been successfully scaled down to less than 10Å with excellent leakage, boron penetration immunity, and long-term reliability even after 1000^oC annealing, without using surface nitridation prior to HfO_2 deposition. The mobility is improved without surface nitridation for HfN/HfO_2 n-MOSFETs while achieving excellent EOT.

This thesis includes a study on metal gate work function thermal stability. A metal-dielectric interface model that takes the role of extrinsic states into account was proposed to qualitatively explain the dependence of metal work function on annealing process. The creation of extrinsic states and the resulting Fermi level pinning of the metal gate work function is observed for several combinations of metal gate and gate dielectric materials, particularly when the gate dielectric is SiO_2. The effect appears to be thermodynamically driven, becoming more pronounced when the annealing temperature is higher. In general, the generation of extrinsic states upon annealing is less significant for metal gates on HfO_2 compared to metal gates on SiO_2.

This thesis also presents a systematic study of hole tunneling current through ultrathin oxide and oxynitride gate dielectrics in *p*-MOSFET's devices. It is found that under typical inversion biases ($|V_g|< 2$ V), hole tunneling current is lower through oxynitride and oxynitride/oxide with about 33 at. % N than through pure oxide and pure nitride gate dielectrics. This is attributed to the competitive effects of the increase in the dielectric constant and decrease in the hole barrier height at the dielectric/Si interface with increasing with N concentration for a given EOT. For minimum gate leakage current and maintaining an acceptable dielectric/Si interfacial

quality, an N/O stack structure consisting of an oxynitride layer with 33 at. % N and a 3 Å oxide layer is proposed. For a *p*-MOSFET at an operating voltage of –0.9 V, which is applicable to the 0.7 μm technology node, this structure could be scaled to EOT = 12 Å if the maximum allowed gate leakage current is 1 A/cm^2 and EOT = 9 Å if the maximum allowed gate leakage current is 100 A/cm^2.

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Chapter 1

Introduction

1.1 Introduction of the MOSFETs Scaling

1.1.1 Overview

During the past several decades, silicon-based microelectronics devices have infiltrated practically every aspect of our daily life. This has been accomplished by continuously achieving the characteristics of higher speed, greater density, and lower power for the individual devices (the Metal Oxide Semiconductor Field Effect Transistors – MOSFET's). Therefore, "scaling", which is the reduction in individual device size, became the focus of engineers over the past 30+ years. The scaling behavior has followed the well known Moore's law, which predicts that the number of transistors per integrated circuit would double every ~ 18 months [1]. During the silicon industry's history and for most of the time, line features of the MOS devices (or Dynamic Random Access Memory – DRAM half pitch) have decreased at the rate of ~ 70% every two or three years. The design rules have been scaled from about 8 μm in the year of 1972 to the 90 nm (0.09 μm) DRAM half pitch of today's leading-edge technology. In the meantime, cost per function has decreased at an average rate

of ~ 25-30% per year per function [2]. Based on the predication of International Technology Roadmap for Semiconductors (ITRS), in the year of 2016, the MOSFET's with L_g (L_g is the final, etched length at the bottom of the gate electrode) of ~ 10 nm would be required for the mass production [2].

1.1.2 MOSFET Device Scaling – Approaches

There are various sets of scaling rules aimed at reducing the device size while keeping device function [3-5], such as constant-field scaling (*CES*), constant-voltage scaling (*CVS*), and the generalized scaling rules.

In *CES*, it was proposed to keep the electric field unchanged in a short-channel device in order to maintain comparable characteristics and reliability relative to a long channel device. The idea behind *CES* is to scale the device voltages ad the device dimensions (both horizontal ad vertical) by the same factor, so that the electric field remains unchanged. However, the requirement to reduce the supply voltage by the same factor as the physical dimension reduction in *CES* is difficult to meet since the threshold voltage and sub-threshold slope are not easily controlled for scaling [6]. If the threshold voltage scales slower than other factors, the drive current will be reduced. Thus, a constant voltage scaling rule (*CVS*) was proposed to address this issue, where the voltages remain unchanged while device dimensions are scaled. However, *CVS* will result in an extremely high electric field, which causes unacceptable leakage current, power consumption, and dielectric breakdown as well as hot-carrier effects [6]. To avoid the extreme cases of CFS and CVS, a generalized

scaling approach has been developed, where the electric field is scaled by a factor of κ while the device dimensions are scaled by a factor of α [4]. In Table 1.1, the scaling parameters for CES, CVS and generalized scaling schemes are compared. In reality, the CMOS technology evolution has followed mixed steps of CES, CVS, and generalized scaling.

Table 1.1. The scaling parameters for *CES, CVS* and generalized scaling guidelines

MOSFET Device and Circuit parameters	Multiplicative Factor for MOSFET's		
	Constant E	Constant V	Generalized
Device Dimensions (T_{ox}, L_g, W, X_j)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Voltage (V)	$1/\alpha$	1	κ/α
Electric Field (E)	1	α	κ
Capacitance ($C = \varepsilon A/t$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Inversion Layer Charge Density (Q_i)	1	α	κ
Circuit Delay Time ($\tau \sim CV/I$)	$1/\alpha$	$1/\alpha^2$	$1/\kappa\alpha$
Power per Circuit ($P \sim VI$)	$1/\alpha^2$	α	κ^3/α^2
Power-Delay Product per Circuit ($P\tau$)	$1/\alpha^3$	$1/\alpha$	κ^2/α^3
Circuit Density ($\propto 1/A$)	α^2	α^2	α^2
Power Density (P/A)	1	α^3	κ^3

(α: Dimensional Scaling Factor; κ: Voltage Scaling Factor)

1.1.3 Gate Dielectric Thickness Scaling

One of the purposes of MOSFET device scaling is to decrease the switching time τ of the MOSFET gate.

$$\tau = (CV / I_{dsat})^{-1} \qquad (1\text{-}1)$$

Eq. 1-1 gives the definition of the τ [7], in which C is the MOSFET gate's capacitance, V is the applied voltage, I is the current, taken as I_{dsat}. For the MOSFET with a high-K gate dielectric, I_{dsat} is given by the following equation [6]:

$$I_{dsat} = (w/2L_g)\,[(\varepsilon_{SiO2}\varepsilon_0 A) / CET_{high\text{-}K}]\;\mu\,(V_{DD} - V_{th})^2 \qquad (1\text{-}2)$$

V_{DD} is the power supply bias, V_{th} is the threshold voltage, $CET_{high\text{-}k}$ is the total electrically measured dielectric thickness in inversion, and L_g and w are the transistor's physical length and width, respectively. Note that *CET* extends the EOT to include the poly-depletion and quantum confinement effects. It can be seen that high drive current can be achieved by reducing L_g, decreasing the gate dielectric electrical thickness $CET_{high\text{-}k}$, or improving the channel carrier mobility μ. Reducing the *EOT* of the dielectric has been a most efficient method to obtain a higher I_{dsat}. In addition, *EOT* reduction enhances the gate control over the channel, ensuring good short-channel behavior. On the other hand, it is essential to maintain the off-state leakage current (including gate leakage currents) as low as possible. From this viewpoint, SiO_2 gate dielectric will be eventually phased out as the dielectric thickness is scaled down to sub-1 nm region, and this will be discussed in detail in the next session. By using high-K gate dielectric as the replacement of the conventional SiO_2 dielectric, the physical thickness, $T_{physical}$ of the gate dielectric could be increased with the decrease of the EOT (described by equations 1-3):

$$EOT_{high\text{-}K} = (\varepsilon_{SiO2} / \varepsilon_{high\text{-}K}) \times T_{physical} \quad (1\text{-}3)$$

where ε_{SiO2} and $\varepsilon_{high\text{-}K}$ are the dielectric constant of SiO_2 and the high-K dielectric respectively.

1.2 Limitation of SiO_2 as the Gate Dielectric for Nano-Scale CMOS Devices

The outstanding properties of SiO_2 have been the key element enabling the scaling of Si-based MOSFET's. The amorphous, high resistivity, stable (both thermodynamically and electrically) thin SiO_2 layer with a band gap of ~ 9 eV acts as an excellent insulator, separating two electrical signals. One traveling between the source and drain in the channel region underneath the SiO_2 and the other one flows in the semi-metallic layer (the gate) above the SiO_2. These two signals are coupled in a capacitive fashion by SiO_2 film. Presently, defect charge density of < $5x10^{10}/cm^2$, mid-gap interface state densities of < $5x10^{10}/cm^2$-eV, dielectric strength of ~ 15 MV/cm, minimal low-frequency CV hysterisis and frequency dispersion (< 10 mV), minimal dielectric charging and interface degradation, and the sufficiently high carrier mobility (both electrons and holes) can be usually obtained for the MOSFET's with Si/SiO_2 system [2].

The rapid shrinking of transistor feature size must be accompanied by the corresponding reduction in the gate dielectric thickness. The gate dielectrics thickness of SiO_2 has decreased from the range of ~ 50-100nm from the 4K

NMOSFET DRAM to ~ 1.2 nm EOT for the today's leading edge high performance logics, and Table 1.2 summarizes such a trend.

Table 1.2. Technology roadmap characteristics for the scaling of dielectrics thickness with time [2]

Year	*2004*	*2007*	*2010*	*2013*	*2016*
Technology node	90	65	45	32	22
Physical gate length for MPU (nm)	37	25	18	13	9
Physical gate length for low power logic (nm)	53	32	22	16	11
EOT for high-performance (nm)	0.9-1.4	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
EOT for low-operating-power (nm)	1.4-1.8	1-1.4	0.8-1.2	0.7-1.1	0.6-1
EOT for low-standby-power (nm)	1.8-2.2	1.2-1.6	0.9-1.3	0.8-1.2	0.7-1.1
Gate leakage at 100^{o}C for high performance (A/cm^{2})	270	4,000	17,000	54,000	110,000
Gate leakage at 100^{o}C for low-operating-power (A/cm^{2})	0.57	2.19	4.55	18.75	90.9
Gate leakage at 100^{o}C for low-standby-power (A/cm^{2})	0.0019	0.0031	0.014	0.044	0.091

With the rapid downscaling of SiO_2 gate insulators, several limits will become inevitable, such as interfacial structure, boron penetration, reliability, and gate leakage issues. The direct tunneling, reliability, and boron penetration concerns associated with ultrathin SiO_2 will be described below.

1.2.1 Gate Leakage

When the physical thickness of SiO_2 becomes thinner than ~ 3 nm, the gate leakage current will be dominated by the direct tunneling through the dielectric. As the SiO_2 thickness is decreased, the gate leakage current through the film increases exponentially according to the fundamental quantum mechanical rules [8]. The rapid increase in leakage current with the decrease of the gate dielectric thickness will pose serious concerns regarding to the operation of CMOS devices, especially with respect to standby power dissipation. The high gate leakage also causes the inversion charge loss, resulting in no further gains in transistor drive current when scaling the SiO_2 thickness thinner than about 10-12 Å [9].

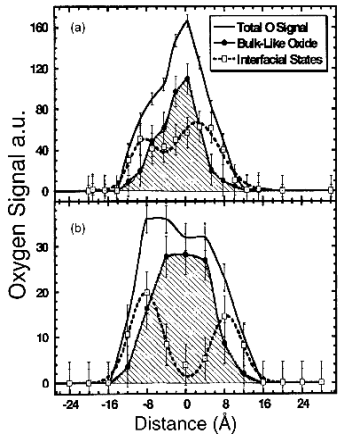

Fig. 1.1. Oxygen bonding profiles for poly-Si/SiO_2/Si structure measured by STEM-EELS. The Si substrate is at the left side and the gate polycrystalline Si is at the right side. (a) 1.0 nm (ellipsometric) oxide, annealed at 1050°C/10 s. The bulk-like O signal (y axis, arbitrary scale) yields a FWHM of 0.85 nm, whereas the total O signal yields a FWHM of 1.3 nm. The overlap of the two interfacial regions has been correlated with the observation of a very high gate leakage current, 10^2A/cm^2. (b) A thicker (~1.8 nm ellipsometric) oxide, also annealed. The interfacial regions no longer overlap and the gate leakage current is 10^{-5}A/cm^2. Courtesy from ref [10].

The study on SiO_2 electronic structure by electron energy loss spectroscopy (EELS) [10] indicates that the bulk SiO_2 energy band gap or the energy band offset to Si substrate cannot be maintained when the thickness of SiO_2 becomes less than two monolayers (~ 0.7 nm). As shown in Fig. 1.1, the EELS profiles consist of bulk-like regions and interfacial regions, and the interfacial regions are believed to be due to the interfacial states. Electrically, this 'interface' material would be unsuitable for low-leakage, high-mobility device operation, implying that a capacitor structure with two interfaces must be at least ~1.2 nm thick if considering the contribution from interfacial roughness (~0.5 nm). Therefore, SiO_2 ~ 10-12 Å is believed to be the practical limit, corresponding to the gate dielectric target in the 65 nm technology node [2].

1.2.2 Reliability

Reliability of ultrathin SiO_2 is another major concern for oxide scaling into the sub-2 nm range [11-13]. The carriers traveling through the SiO_2 layer may generate defects including carrier traps and interface states, and upon accumulation to the critical density, the dielectrics properties will be degraded. The accumulated charge to breakdown values (Q_{bd}) for the dielectrics decreases with the thickness [11]. Recently, it was predicted that oxide films thinner than ~ 1.4 nm would not achieve the reliability required by the industry roadmap [12]. Nevertheless, the real impact of oxide breakdown on circuit performance, which ultimately is the critical issue, should be further investigated.

1.2.3 Boron Penetration

As the SiO_2 film decreases in thickness, boron penetration from p+ poly-silicon gate to the channel region becomes significant especially upon thermal annealing [14,15]. This will result in a change in the doping concentration of the channel region, which in turn, leads to the poor threshold voltage control, the fluctuations in flat band voltage accompanied by increasing PMOSFETs sub-threshold slope, and decreased the low field carrier mobility [14].

1.3 Oxynitride and Oxynitride/Oxide Stack Dielectrics as Alternatives to SiO_2

Oxynitride and oxynitride/oxide stack structures as the near-term gate dielectric alternatives have been proposed to address the high leakage, boron penetration and reliability concerns of ultrathin SiO_2 [2]. It is noted that the hole and electron barrier height at the Oxynitride/Si interface, the oxynitride gap energy, as well as the dielectric constant vary linearly with the N concentration of the oxynitride film [16,17].

The addition of N to SiO_2 could greatly reduce the impurity (especially for boron) diffusion through the dielectric, and was suggested to be due to the particular Si–O–N bonding lattice formed in silicon nitride and oxynitride [15]. Small amounts of N (~ 0.1 at. %) at or near the Si channel interface provide the ability of controlling

channel hot-electron degradation effects [17]. However, larger amounts of N near this interface will degrade device performance. A work for depositing Si-nitride directly on the Si channel by remote plasma chemical vapor deposition (RPCVD), claimed the poor pMOS performance, with significant degradation of channel mobility and drive current [18]. This degradation mechanism is mainly attributed to excess charge of pentavalent N atoms, and hence a high defect density arising from bonding constraints imposed at the interface, which causes increased channel carrier scattering. In addition, the defect levels in the Si-nitride layer which reside near the valence band of Si also contribute the degradation. Oxynitride/oxide stack structure with the oxide as interfacial buffer layer is thus proposed in order to obtain the improved electrical properties [19,20].

Due to the ultimate limitation of the dielectric constant values of oxynitride (for Si_3N_4, the K value is ~ 7.8) and its smaller gap energy compared to SiO_2, the scaling limits for thickness of oxynitride (oxynitride/oxide stack) would be ~ 1.2 nm [20]. Further scaling of gate dielectrics requires other materials with higher K values.

1.4 Alternative Higher-K Materials

The metric of the high-K gate dielectrics rather than SiO_2 is to provide a physically thicker film for reduced leakage current and improved gate capacitance. In this section, the selection procedure for the alternative high-K gate dielectric is first discussed, followed by an overview of the research status on some potential high-K

gate dielectrics. Process issues for high-K gate stack fabrication and the pressing concerns associated with high-K transistors will also be briefed.

1.4.1 Selection Guidlines for High-K Gate Dielectrics

Several most important factors being considered for gate dielectric selection process are described as followings:

1.4.1.1 Electron/Hole Barrier Height and Dielectric Constant

First, the dielectrics should have barrier height for both electrons and holes (ΔE_c and ΔE_v) more than 1.0 eV to avoid unacceptable gate leakage either by thermal emission or tunneling [21]. A large gap energy value generally corresponds to a large ΔE_c, but the band structure for some materials has a large valence band offset ΔE_v which constitutes most of the band gap of the dielectric (such as Ta_2O_5).

The gap energy of the dielectric should be balanced against its dielectric constant. Permittivity generally increases with increasing atomic number for a given cation in a metal oxide. However, the band gap of the metal oxides tends to decrease with increasing atomic number [22]. Fig. 1.3 shows that for simple dielectrics, the gap energy will decrease with the increase of the dielectric constant [23].

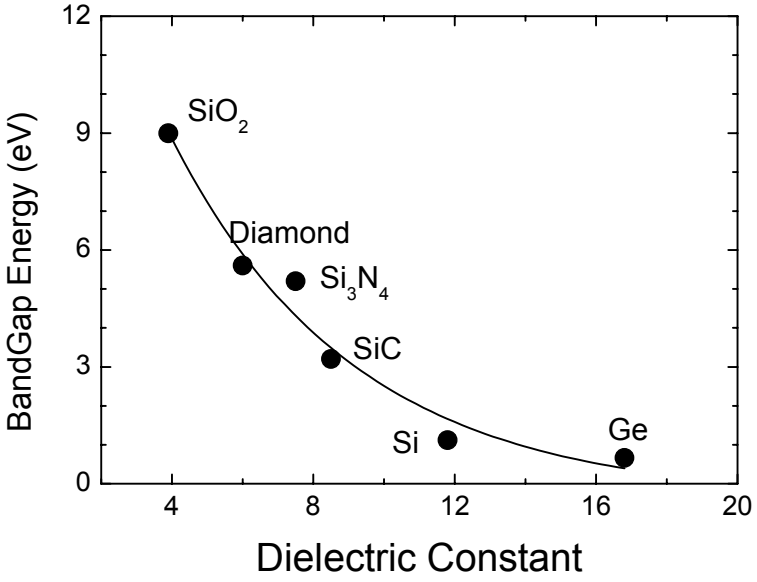

Fig. 1.2. For simple dielectrics, a relationship exists between the gap energy and the permittivity [23].

Attention is paid to such effect as the Fringing-Induced Barrier Lowering (*FIBL*) for high-K materials [24]. *FIBL* effect predicts that the device off-state leakage current increases as K value increases (become significant especially when K>25), which is due to that a significant fringing field at the edge of a high-K dielectric could lower the barrier for carriers transport into the drain, and hence seriously degrade the on/off characteristics of the device. It is therefore appropriate to find a dielectric which provides a moderate increase in K, but which also produces a large tunneling barrier and high quality interface to Si. A single dielectric layer with k ~ 12–25 could allow a physical dielectric thickness of 35–50 Å to obtain the *EOT* values required for 65 nm CMOS and beyond.

1.4.1.2 Film Microstructures

It is desirable that the gate dielectric remains amorphous throughout the necessary processing treatments [22]. The limitation of polycrystalline dielectrics could be the defects induced by grain boundaries, and the interfacial roughness arising from potentially faceted interfaces. Grain size and/or orientation changes inside a polycrystalline film can cause the variations in K value, leading to irreproducible properties for the dielectrics. In addition, the defects throughout the high-K films and interfacial roughness can cause the increase of gate leakage and the reduction of carrier mobility. The application of the single-crystalline dielectrics could be limited by its fabrication methods, although the grain boundaries and the interface issues could be addressed. These single-crystalline materials grown on Si substrate require sub-monolayer deposition control, which may only be obtainable by epitaxial approaches, which is not a cost-effective and manufacturable technique for mass production.

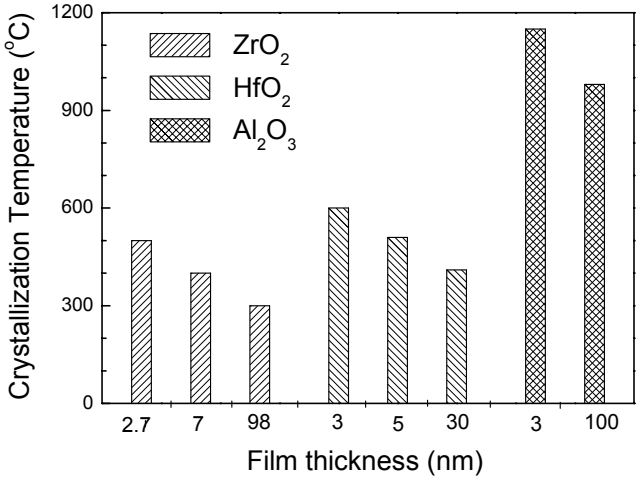

Fig. 1.3. Crystallization temperature increases with decreasing film thickness [25]

Fig. 1.3 shows the crystallization temperature for Al_2O_3, ZrO_2, and HfO_2 high-K dielectrics [25]. Al_2O_3 remains amorphous upon annealing till 1100 °C, while ZrO_2 and HfO_2 become crystallized below 600 °C. It is interesting to note that for all of three dielectrics, crystallization temperature increases with the decrease of the film thickness.

1.4.1.3 Thermal Stability and Channel Interface Quality

The interface with Si channel plays a key role for the realization of the high-K gate dielectrics in the IC. Most of the high-K materials reported up to date show the interface states density (D_{it}) of ~ 10^{11} – 10^{12} states/eV-cm^2, and a fixed charge density ~ 10^{11} – 10^{12} /cm^2 at the interface. It is proposed that the Si-dielectric interface quality depends on the bonding constraints [26]. The interface defect density will increase proportionally if the average number of bonds per atom is higher/lower compared to that of Si, leading to an over-/under- constrained interface with Si. These metal oxide (either over- or under- constrained with respect to SiO_2) result in the formation of a high density of electrical defects near the Si-dielectric interface.

In addition, for most of the high-K materials, during their deposition on Si substrate under equilibrium conditions, there would be an undesirable and uncontrollable interfacial layer [22]. Therefore an interfacial reaction barrier should be required for a better channel interface quality. The chemical stability of gate oxides on silicon in the subsequent process conditions also has a critical impact on the Si/dielectric interface quality. One step from a typical CMOS process flow is the source/drain (S/D) activation annealing, which the gate stack must undergo. The

typical S/D anneal is done by rapid thermal anneal technique (up to 1000°C). If the cations from the gate dielectric diffuse into the channel region, the device electrical properties (especially the channel mobility induced by the impurity scatter) will be degraded. To control and improve the channel interface quality, the knowledge of the following for the gate dielectric is required during subsequent process: reaction with silicon, oxygen diffusion kinetics, oxygen stoichiometry, film crystallization and component segregation.

For the high-K dielectrics with high oxygen diffusivities at high temperature, such as ZrO_2 and HfO_2 [17, 27], during the annealing treatments where an excess of oxygen present, rapid oxygen diffusion through the oxides could be expected. And hence, the SiO_2 or SiO_2-containing low-K interface layers would be formed, posing a serious concern regarding to *EOT* scalability of the high-K dielectric.

1.4.1.4 Mobility Issues

Mobility is a critical parameter to evaluate a high-K dielectric as the replacement to SiO_2. It is a key parameter determining a number of transistor metrics, such as saturation current, speed, threshold voltage, transconductance, and sub-threshold swing. It is desired to maintain the mobility of the high-K transistors close to that of the SiO_2 system.

Three scattering mechanisms determine the inversion carrier mobility: the Coulomb charge scattering, the phonon scattering, and the surface roughness scattering [42]. Surface roughness scattering dominates only when the effective field

is high enough so that channel carriers are close to the Si substrate surface. It has been shown that at a high effective field (≥ 1 MV/cm), the mobility of high-K transistors becomes close to the universal mobility curve.

Coulomb scattering may originate from different scattering centers. Coulomb scattering centers was traditionally known to be due to the substrate impurities. However, remote Coulomb scattering (*RCS*) has been identified to play an important role for the mobility degradation phenomena in high-K transistors. These remote scattering centers are away from the inversion layer, and might be due to fixed charge, oxide trap, interface trap and micro-crystallization related to the high-K dielectric. Ref. [43] concludes that a thicker interfacial layer between high-K dielectric and Si substrate would lead to a higher carrier mobility [Fig. 1.4], based on the results summarized from various research groups. This suggests that the remote Coulomb scattering centers centroid is nearby the interfacial layer. A research group at *International Sematech* observes that the mobility increases with decreasing high-K physical thickness, which is attributed to the reduced total Coulomb scattering due to charges in the high-K [44].

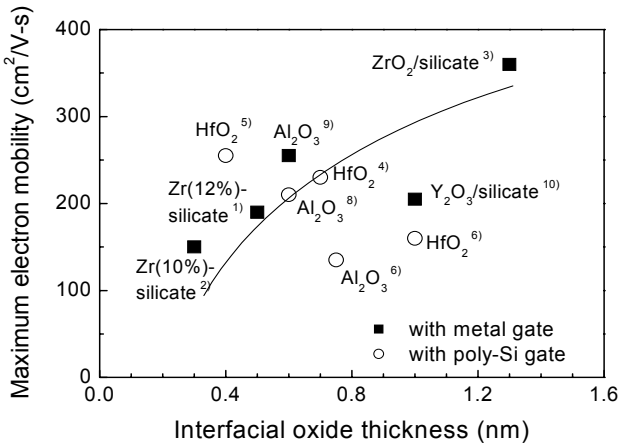

Fig. 1.4. Maximum mobility increases with the interfacial oxide thickness.

At low temperature, it is known that only Coulomb scattering and surface roughness scattering dominate for transistors with the SiO_2 dielectric [42], as the phonon scattering is suppressed. However, it is interesting to note that a recent study [45] suggests that soft phonons scattering in high-K dielectrics is a source of mobility degradation, by investigating the low temperature mobility of the HfO_2 transistor, and comparing it with the SiO_2 counterpart at the medium high effective electric field (when inversion charge > $5x10^{12}$ cm^{-2}). On the other hand, another study on the low temperature mobility measurement [46] shows that electron mobility of HfO_2 transistor is much lower than the SiO_2 control at the relatively low effective field, indicating the RCS is at least partly responsible for the mobility degradation in HfO_2 device.

1.4.1.5 Threshold Voltage Related Issues

Threshold voltage control is another key issue to be addressed in order to realize the high-K transistors in the IC. For the transistors with the poly-Si/HfO_2 gate stack and the poly-Si/Al_2O_3 gate stack, significant threshold voltage shift has been observed as compared to poly-Si/SiO_2 control devices [47]. It was found the respective positive and negative shifts in *n*- and *p*- MOSFETs with high-K gate dielectrics, and this has been interpreted as the Fermi pinning occurring at the interface of poly-Si/HfO_2 and poly-Si/Al_2O_3 [47]. Recently, the high threshold voltage is also reported in the transistors with high-K gate dielectrics using metal gate electrode [48], and again the Fermi pinning was suggested to play a determining role for such an observation [48, 49].

The dopant penetration through dielectrics leads to the uncontrolled threshold voltage shift of the transistors. This issue might be more significant for high-K transistors compared to the device with SiO_2, as most of the high-K become crystalline during the S/D annealing process. N-incorporation in high-K dielectrics is expected to suppress the dopant penetration [50], similar as the current SiO_xN_y technology.

It was observed that charge trapping phenomena occurs in the HfO_2 gate dielectric for MOSFETs under DC uniform ($V_{ds} = 0$) static stress [51,52], leading to severe bias temperature instability (BTI). BTI is important as it caused the device threshold voltage shift and saturation drive current decreases with electrical stressing. However, under AC ($V_{ds} \neq 0$) stressing, improvement of BTI degradation for MOSFETs with HfO_2 dielectric has been observed, and this improvement increases with increasing stress frequency [52]. It was thus concluded that the BTI should not be the "show-stopper" in realizing HfO_2 transistors for digital IC applications [52]. A model accounting for carrier trapping/de-trapping process and generation of new traps in HfO_2 dielectric under stress has been proposed to explain the frequency-dependant BTI degradation phenomena.

1.4.2 Research Status of Some Potential High-K Gate Dielectrics

Most of the high-K gate dielectric candidates studied up to date are the metal oxide, and Table 1.3 complies the materials properties for several potential high-k gate dielectric candidates.

Table 1.3. Band offsets and dielectric constants for different high-K gate dielectric candidates (including SiO_2 and Si_3N_4) [17, 22, 28]

Dielectric	Dielectric constant (K)	Gap energy (eV)	Electron barrier to Si (eV)
SiO_2	3.9	8.8	3.15
Si_3N_4	7.8	5.1	2.1
Al_2O_3	8 – 11.5	~6.5 - 8.7	~2.4 - 2.8
ZrO_2	22 – 28	~5.5 - 5.8	~1.4 - 2
$ZrSiO_4$	10 – 12	~6	1.5
HfO_2	25 – 30	~5.25 - 5.7	~1.5 - 1.9
$HfSiO_4$	~10	~6	1.5
TiO_2	~80	3.5	~1.2
Ta_2O_5	~25	~5	~0.3 - 0.5

High-K dielectric properties and quality is critically determined by the method it is deposited [29]. For sputter physical vapor deposition (PVD), surface damages and hence the interface states will be the inherent concerns. On the other hand, chemical vapor deposition (CVD) is proven to be a reliable technique for obtaining the uniform coverage over complicated device topologies. Several most promising CVD metal oxide high-K gate dielectrics will be discussed below.

Alumina (Al_2O_3) belongs to group IIIA metal oxide, and its characteristics are very similar to SiO_2. It has many favorable properties such as high gap energy value, thermodynamic stability on Si up to high temperature annealing, and remains amorphous under the conditions of interest. However, due to its relatively low k

values (only 8~11), alumina is only considered as the short-term solution for industry's needs. For Al_2O_3 deposited via atomic layer chemical vapor deposition (ALCVD) [30], severe dopant diffusion and the significant negative fixed charges have been demonstrated, therefore the carrier mobility at the dielectric/Si interface was significantly reduced.

TiO_2, ZrO_2 and HfO_2 belong to group IVB metal oxides. TiO_2 has a high dielectric constant (80~110) and has been studied for both the memory and gate dielectric application. CVD TiO_2 is not stable on Si during deposition, and it will crystallize at ~ 400 °C [31]. These properties rule out TiO_2 application as the gate dielectric. Zirconium oxide, hafnium oxide and their silicates and aluminates also received considerable attention [32-36]. Degradation of the chemical properties for ZrO_2 as compared to HfO_2 might be due to the interaction of the polysilicon gate electrode with the ZrO_2 [37], as well as the interaction of ZrO_2 with the lower silicon interface leading to silicide formation. For CVD ZrO_2 deposited on Si substrate, during annealing in UHV ambient, interfacial SiO_x triggers the $ZrSi_2$ and Zr formation at the channel interface, which are decomposed from ZrO_2 [38]. HfO_2 film has emerged as one of the most promising gate dielectric candidates due to its high dielectric constant, large energy gap, superior thermal stability with poly-Si and its compatibility with conventional CMOS process [32-34]. On the other hand, the zirconium or hafnium silicates and aluminates have been demonstrated to have better thermal stability (higher crystallization temperature, and lower oxygen diffusivity) compared to that of the pure oxide. Despite of their lower dielectric constants compared to the value of the pure oxide, (see table 1.3), they seem to be adequate to meet the transistor performance goals [22].

1.4.3 Process Issues for High-K Gate Stack Fabrication

Not only the specific deposition process, but the pre-deposition surface cleans and the post-deposition treatment, are critical in controlling the high-K films structure (crystallinity, micro-structure, and stoichiometry etc.) and, in turn, their electrical properties such as the EOT, gate leakage current and the reliability characteristics.

The study on pre- high-K deposition clean include standard RCA clean (SC1/SC2), HF last, ozone (O_3), etc. A high quality chemical oxide at Si surface would be grown with the aid of O_3 clean. It was found that the O_3 clean led to a smoother high-K film subsequently deposited by ALD compared to RCA or HF last pre-gate clean [7], though the interfacial chemical oxide would cause the EOT increase. It is observed that a post high-K deposition anneal (PDA) in N_2 at mild temperature (600°C-700°C) is helpful to improve the high-K quality and reduce the leakage current for a given film physical thickness [32-33]. However, the trace amount of oxygen in an inert ambient anneal during high-K PDA can be sufficient to cause the low-K interfacial layer growth at the high-K/Si interface [39-40]. An NH_3 anneal prior to high-K deposition was proposed to minimize the low-K interfacial layer growth during high-K PDA [41]. However, the interface defects caused by the N effect might degrade the device electrical properties [41].

1.5. Metal Gate Technology

1.5.1. Limitation of Poly-Si Electrodes for Nano-Meter CMOS Devices

1.5.1.1 Poly-Silicon Depletion Effect

The poly-Si depletion effect occurs when a MOS device with a poly-Si gate electrode is biased into depletion or inversion region. Fig. 1.5 illustrates poly-Si depletion effect for a n+ poly-Si n-MOS device. When a positive bias is applied at the gate, a depletion layer with a finite thickness is formed at the poly-Si gate side at the poly-Si/oxide interface, associating with the non-negligible band bending in the poly-Si gate.

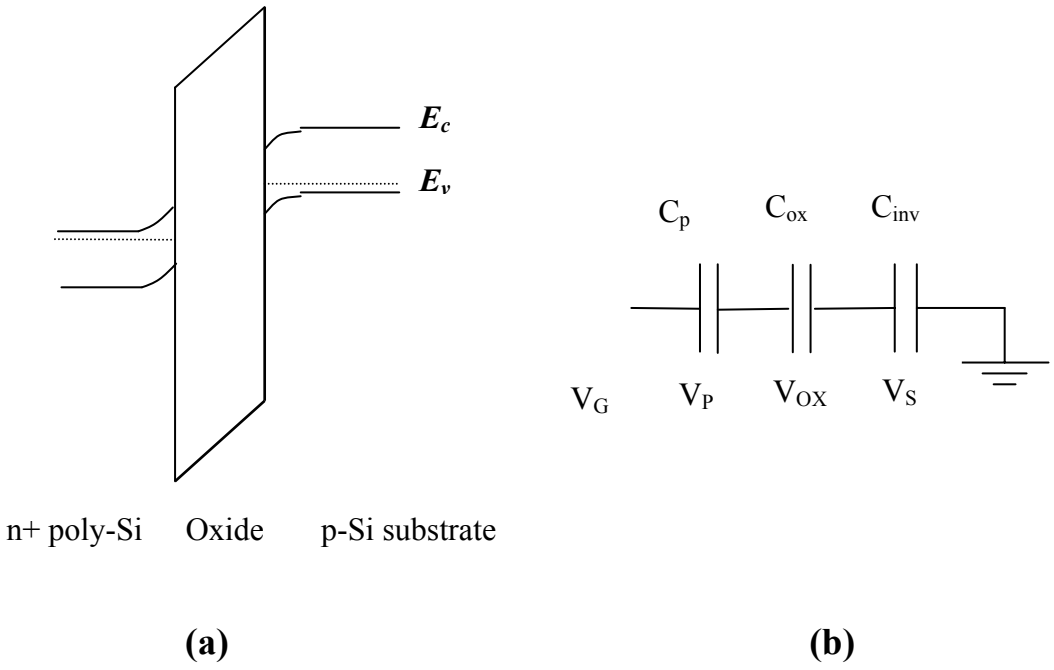

Fig. 1.5. (a) The energy band diagram of a N-MOS device showing the poly-Si gate depletion effect; (b) C_p, C_{ox}, and C_{inv} represent the capacitance from the poly depletion layer, gate oxide and substrate inversion layer, respectively.

From an equivalent circuit diagram shown in Fig. 1.5(b), the poly-Si depletion capacitance C_P is series with the gate oxide capacitance, leading to a reduction of the gate oxide capacitance in inversion. This is equivalent to an increase of the effective

oxide thickness. As a result, a smaller inversion charge density is expected, and hence a reduction of the drive current for the MOSFET device. With the aggressive scaling of the gate dielectric thickness, the poly-Si depletion effect becomes much more significant [2]. An increase of gate dielectric EOT of 5-6 Å due to poly-Si depletion effect is expected, as compared to EOT requirement (< 1 nm) in nanometer scale CMOS.

1.5.1.2 Gate Electrode Resistivity and Dopant Penetration Effect

Table 1.4. Scaling parameters on gate electrode from ITRS-2001 [2]

Year	*2004*	*2007*	*2010*	*2013*	*2016*
Technology node	**90**	**65**	**45**	**32**	**22**
Gate electrode thickness (nm)	37-74	25-50	18-36	13-26	9-18
Average gate electrode sheet resistance (Ω/□)	5	5	5	6	7

Tale 1.4 summarizes that scaling parameters on gate electrode, based on ITRS-2002. It is seen that the gate electrode resistivity is required to be scaled with the technology node. This is particularly important for MOS devices in RF application. One way to minimize the high gate resistance, as well as the poly depletion effect associated with poly-Si gate, the active dopant density in the poly-Si gate should be increased. However, it is difficult to get electrically active doping densities above 10^{20} cm^{-3} due to the limitation of the dopants solubility in the poly-Si films, especially for p+ poly-Si doped with boron [49]. Besides, for p-MOSFETs, the boron

penetration p+ poly-Si to the channel region induces threshold voltage shift and other reliability concerns for the transistors, as addressed in section 1.2.3 of this chapter.

1.5.1.3 Work Function Requirement for Novel MOS Devices

Work function of the conventional n+ poly-Si / p+ poly-Si is close to the conduction band / valence band edges of Si, and this is preferred for the optimal design of bulk n- / p-MOSFETs, respectively [53] because of the requirements on the threshold voltages and the need to use heavy dopants to control short-channel effects. However, the fixed work function value for n+ (p+) poly-Si might be adequate for some novel MOS devices. For examples, metal gate with a midgap work function is highly desired for ultra thin body FD-SOI devices to make low channel doping viable, so as to eliminate channel mobility degradation and minimize the V_{th} variation [54].

1.5.2. Metal Gate Technology

Metal gate electrodes not only eliminate the gate depletion and dopant penetration issues in CMOS devices, but also greatly reduce the gate sheet resistance. Moreover, the use of a metal gate material makes it possible to choose the work function of the gate and redesign the device for the optimum combination of work function and channel doping. Though metal gates promise superior performance, they pose significant technological challenges. The major challenge for metal gate technology is to identify the appropriate metals with suitable work functions and with sufficient chemical stability, and find a way to integrate the metal into CMOS process.

To maintain the acceptable performance advantage, metal gates with work functions near the conduction band and valence band edges of Si are desired for the optimal design of bulk n- and p-MOSFETs, respectively [55]. A simple and direct way is to use two metal gate electrodes (one replaces p+ poly-Si, and the other one replaces n+ poly-Si) with distinct work functions. However, the metal gate electrodes must be thermally and chemically compatible with the underlying gate dielectrics. They must have good adhesion, and they should be controllably patterned. Presently, active research is in progress to identity the suitable metals. The possible candidates include pure metal with high melting temperature (T_m), metal alloy, conductive metal oxides, metal silicide, and metal nitride. It is worth noting that by using one material system for the metal electrodes, it is possible to tune the metal work function for either n-MOS or p-MOS by varying the alloy composition or by doping. Such an approach is aimed to reduce the process complexity and cost. RuTa alloy is demonstrated to be able to meet both the requirement of p-MOSFETs (when Ta < 20%) and that of n-MOSFETs (when 40% < Ta < 54%) [56]. By doping nitrogen into the Mo, which is for the p-MOSFET metal electrode, Mo work function could be tuned toward the n-MOSFET required value [57].

Another promising solution is the fully silicidation of poly-Si gates (FUSI process) [58]. The metal silicide work function can be tuned by the doping the poly-Si before silicidation. In addition, FUSI process requires no new etch step, no high temperature post-gate step. The "gate-last" process for metal gate integration (by using replacement gate and damascene process) could avoid the high-temperature annealing of gate stack, however, it significantly increases the process complexity and cost.

1.6. Major Achievements in This Thesis

The focus of this thesis is the study of advanced gate stack for future nano-meter CMOS device application. In chapter 2, the materials properties of $(HfO_2)_x(Al_2O_3)_{1-x}$ high-K dielectrics grown by ALD are to be presented, including the energy band alignment to (100) Si substrate and the thermal stability. It is shown that Al 2*p*, Hf 4*f*, O 1*s* core levels high resolution XPS spectra, valence band spectra, and O 1*s* energy loss spectra all show continuous changes with HfO_2 mole fraction *x* in $(HfO_2)_x(Al_2O_3)_{1-x}$. These data are used to estimate the energy gap E_g for $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset ΔE_v, and the conduction band offset ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100) Si substrate. Further it will be reported that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al to form Hf aluminates, and the improvement is closely correlated with the Al percentage in the films. This observation is explained by (i) Al_2O_3 has much lower oxygen diffusion coefficient than HfO_2 at high temperature; (ii) doping HfO_2 by Al raises the film crystallization temperature of HfO_2 and thus drastically reduces the oxygen diffusion along the grain boundaries during annealing. The difference of IL growth between N_2 (10 torr) and high vacuum (~ 2×10^{-5} torr) 1000 °C annealing indicates that the active oxygen species from the annealing ambient is the main cause for the IL growth during RTA in N_2.

In chapter 3, a systematic study on novel HfN metal gate electrode for advanced CMOS devices applications is presented. For both SiO_2 and HfO_2 gate

dielectrics, HfN metal possesses a mid-gap work function, and shows robust resistance against high temperature RTA treatments (up to 1000°C), in terms of EOT, work function, and leakage current stability. This superior electrical stability is attributed to the excellent oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 and HfN/SiO_2 interface. Further, the high quality HfN/HfO_2 gate stack's EOT has been successfully scaled down to less than 10Å with excellent leakage, boron penetration immunity, and long-term reliability even after 1000^{o}C annealing, without using surface nitridation prior to HfO_2 deposition. The mobility is improved without surface nitridation for HfN/HfO_2 n-MOSFETs while achieving excellent EOT. HfN is proposed as an ideal gate electrode candidate for the FD-SOI and/or the symmetric double-gate (SDG) MOS devices applications where a mid-gap metal gate electrode is desired.

Chapter 4 studies the dependence of metal gate work function on annealing temperature. A metal-dielectric interface model that takes the role of extrinsic states into account was proposed to qualitatively explain the work function thermal instability. The creation of extrinsic states and the resulting Fermi level pinning of the metal gate work function is observed for several combinations of metal gate and gate dielectric materials, particularly when the gate dielectric is SiO_2. The effect appears to be thermodynamically driven, becoming more pronounced when the annealing temperature is higher. In general, the generation of extrinsic states upon annealing is less significant for metal gates on HfO_2 compared to metal gates on SiO_2. Interface dipole formation plays an important role in determining the amount of Fermi pinning and the threshold voltage of metal gate transistors.

Chapter 5 presents a systematic investigation of hole tunneling current through ultrathin oxide, oxynitride, and oxynitride/oxide (N/O) gate dielectrics in *p*-MOSFET's using a physical model. Under typical inversion biases ($|V_g|< 2$ V), hole tunneling current is lower through oxynitride and oxynitride/oxide with about 33 at. % N than through pure oxide and pure nitride gate dielectrics. This is attributed to the competitive effects of the increase in the dielectric constant and decrease in the hole barrier height at the dielectric/Si interface with increasing with N concentration for a given EOT. For a N/O stack film with the same N concentration in the oxynitride, the hole tunneling current decreases monotonically with oxynitride thickness under the typical inversion biases. For minimum gate leakage current and maintaining an acceptable dielectric/Si interfacial quality, an N/O stack structure consisting of an oxynitride layer with 33 at. % N and a 3 Å oxide layer is proposed. For a *p*-MOSFET at an operating voltage of –0.9 V, which is applicable to the 0.7 μm technology node, this structure could be scaled to EOT = 12 Å if the maximum allowed gate leakage current is 1 A/cm^2 and EOT = 9 Å if the maximum allowed gate leakage current is 100 A/cm^2.

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Chapter 2

ALD $(HfO_2)_x(Al_2O_3)_{1-x}$ High-K Gate Dielectric for CMOS Devices Application – the Band Alignment to (100)Si and the Thermal Stability Study

2.1 Introduction

HfO_2 high-K dielectric has been extensively studied for future generation of MOS transistors application due to its high dielectric constant, large energy gap, and its compatibility with conventional CMOS process [1-4]. However, it may suffer re-crystallization at high temperature during post deposition annealing (PDA), which in turn, may induce higher leakage current, non-uniformity of the film thickness, and severe dopant penetration issues. Furthermore, HfO_2 is ionic in nature, and is "transparent" to the oxygen diffusion [1]. Annealing in an oxygen-rich ambient will lead to fast diffusion of oxygen through the HfO_2, causing the growth of uncontrolled low-K interfacial layers (either SiO_x or SiO_x–containing layer). The uncontrolled low-K layer poses a serious limitation to further scaling of the equivalent oxide thickness (EOT) for HfO_2 gate dielectrics. On the other hand, Al_2O_3 films grown directly on Si was reported to remain amorphous up to 1000°C [5]. Recently Al has been proposed to alloy HfO_2 to raise the dielectric crystallization temperature, and

encouraging results were demonstrated [6]. It was reported that when Al concentration is increased to 31.7%, the corresponding crystallization temperature increases to between 850 – 900 °C, which is about 400 °C higher than that for HfO_2. And thus, hafnium aluminates are regarded as a promising candidate for high-K gate dielectrics application.

In the section 2.4 of this chapter, the energy gap E_g of $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset ΔE_v, and the conduction band offset ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100)Si substrate as functions of x (x: the mole fraction of HfO_2 in $(HfO_2)_x(Al_2O_3)_{1-x}$) are reported based on x-ray photoelectron spectroscopy (XPS) measurement. These information are of vital importance in assessing $(HfO_2)_x(Al_2O_3)_{1-x}$ as a promising high K gate dielectric in future CMOS device technology. Further in the section of 2.5, the thermal stability of the Hf aluminates and its impact on oxygen diffusivity through Hf aluminates are studied. We demonstrate that the resistance to the oxygen diffusion in HfO_2 films can be greatly enhanced by the incorporation of Al, and the improvement is closely correlated with the Al percentage in the films.

2.2 Theoretical Background on X-ray Photoelectron Spectroscopy

XPS is an important and key technique for the materials surface characterization. Its great strength is its ability to obtain both elemental and chemical information on sample surfaces. This technique provides a total elemental analysis,

except for hydrogen and helium, of the top 10 – 100 Å (depending on the sample and instrumental conditions) of any solid surface that is stable in vacuum [7].

2.2.1 Principles of XPS

The basic principle of XPS is the photoelectric effect. The fundamental processes in XPS are the absorption of a quantum of photon energy $h\nu$ and the ejection of a photoelectron, whose kinetic energy, referenced to an appropriate zero of energy (Fermi energy for solid samples), is related to the binding energy of an electron in the target atom. The binding energy of the photoelectron is defined as the energy required to remove it to infinity with a zero kinetic energy. In this photoelectron-production process, the incident photon transfers its entire energy to the bound electron, and elemental identification is provided by the measurement of the kinetic energy of the electrons that escape from the sample without any energy loss.

Thus there is:

$$E_B = h\nu - E_K - \phi_{ins} \qquad \textbf{(2-1)}$$

where E_B is the electron binding energy, E_K is the electron kinetic energy, and ϕ_{ins} is the instrument work function. All energies are expressed in eV. By calculating the binding energy, atoms can thus be identified.

Fig. 2.1 presents a schematic version of the experiment for a solid sample [8]. X-rays are produced at an anode by bombardment of electrons created by a filament. The anodes that have been used include Al (1486.6 eV), Mg (1253.6 eV), Ti (4511 eV), silicon (1739.5 eV) etc. Of all, Al provides a stable, reliable beam of Kα x-rays

dominated by the $K\alpha_{1,2}$, which is nearly monochromatic [7]. The solid sample is mounted on a suitable sample holder and placed in ultrahigh vacuum (UHV) environment. Photoelectrons produced by this process escape from the sample and their kinetic energies are detected and analyzed in the electron energy analyzer. The analyzer basically measures the number of electrons of different kinetic energies. The information is generally processed by a computer to produce a spectrum of photoelectron intensity as a function of binding energy. In a more sophisticated instrument, it may contain an x-ray monochromator to narrow the line width of the X-radiation, e.g., Mg Kα x-rays have a line width of ~ 0.75 eV, but an x-ray monochromator can produce a line width as low as 0.3 eV.

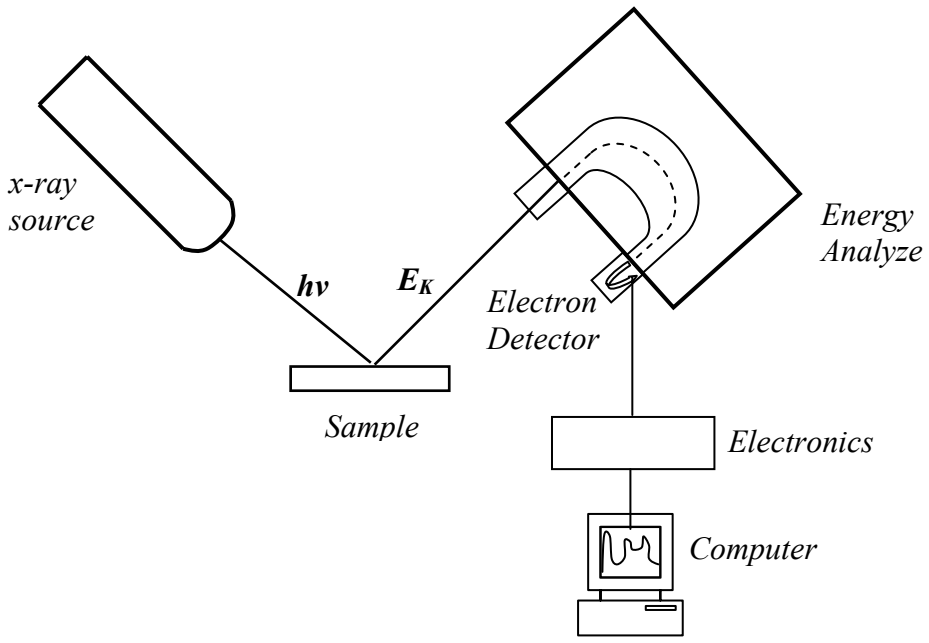


Fig. 2.1. Schematic diagram of an X-ray photoelectron spectroscopy experiment

When photoelectrons are constantly being emitted from the sample surface, the sample will charge positively. The surface charge is an electrical potential barrier

which the electrons must overcome to get into the vacuum. With such a barrier, the electrons emerge from the sample with lower kinetic energy and appear on the XPS spectrum with higher binding energy. Therefore, it is necessary to electrically ground the samples. Conducting and/or semiconducting samples are mounted in direct electrical contact the probe, which in turn is contact with the spectrometer ground circuit which provides a source of electrons. For those insulating samples, an electron flood gun is used to bathe the sample surfaces, eliminating the charging effect.

2.2.2 Applications of XPS

2.2.2.1 Elemental Analysis

XPS provides information about the binding energy of electrons in the material under study. Two types of electrons are generally distinguished, namely core electrons and valence electrons. Valence electrons influence chemical bonding and their binding energy is characteristic of molecular orbitals from which they arise. This energy depends on the amount of mixing between the constituent atomic orbitals in the molecular orbital. Electrons with a binding energy of 30 eV or less are generally classified as valence electrons. Core electrons are atomic in character, as they essentially take no part in chemical bonding. On the other hand, the subtle shift in the core level binding energy provides information on the chemical bonding, and this will be discussed in next section. Core electrons' binding energy can be readily used as atomic identification and core level XPS is extensively used for surface analysis.

The relative concentration of the various constituents can be obtained based on the intensity of photoelectron (measured as peak area) and XPS sensitivity factor (S/F) [7]. The photoelectron intensity ***I*** depends on many factors,

and there is,

$$I = nf\sigma\theta y\lambda AT \qquad \textbf{(2-2a)}$$

where ***n*** is the atomic concentration for the element (atoms/cm^3), ***f*** is the x-ray flux (photon/cm^2·sec), σ is the photoelectric cross section (cm^2), θ is the instrumental angular efficiency factor based on the angle between the photon path and detected electron, ***y*** is the photoelectron process efficiency for formation of photoelectrons of the normal photoelectron energy, λ is the photoelectron mean free path, ***A*** is effective sample area from which photoelectrons are detected, and ***T*** is detection efficiency for electrons emitted from the sample.

Rearranging equation above:

$$n = I / (f\sigma\theta y\lambda AT) \qquad \textbf{(2-2b)}$$

the denominator is the sensitivity factor ***S/F***. Thus atomic concentration of element A can be calculated as:

$$n_A\ (at.\ \%) = \frac{I_A / S_A}{\Sigma I_i / S_i} \qquad \textbf{(2-2c)}$$

2.2.2.2 Chemical Bonding Information

High-resolution XPS scans provide chemical bonding information from the shifts in the core levels due to environment of the atom in the substance under study.

A qualitative explanation for the chemical shift effect is the interaction of the core electrons with the surrounding atoms [8]. Consider that an atom bound to highly electronegative species, such as carbon bound to oxygen, results in the carbon electrons being attracted to the oxygen atom due to the electronegativity difference. Therefore, there is less negative charge to interact with the carbon nucleus, resulting in less electrostatic shielding of the carbon core electrons. It indicates that the core electrons are more strongly attracted by the nucleus, and thus a higher core level binding energy is observed. On the other hand, electropositive species will contribute to the electron density of the carbon, resulting in increased shielding for the nucleus charge and therefore a decreased core level binding energy. Empirically, the core level binding energy increases with oxidation state.

Because the chemical shifts are not very large, it is important to precisely reference the spectra for chemical shift analysis. Binding energy values are generally referenced to Fermi energy for solid samples. A Fermi energy in a solid is essentially the chemical potential of the electrons in that solid.

An XPS peak may consist of a number of components that could be resolved. Generally how to separate these peaks by suitable curve-fitting method are concerned. XPS peaks are normally Gaussian-Lorenz in shape [8]. With appropriate assumptions, the subcomponents of a given spectral peak could be deduced as adding two or more Gaussian-Lorenz functions to form a sum peak.

2.2.2.3 Energy Gap Measurement for Dielectrics

The determination of gap energy for dielectrics (the oxides) by XPS is schematically explained in Fig. 2.2. The outgoing photoelectrons could suffer inelastic energy losses to collective oscillations (plasmons) and single particle excitations (band to band transitions). Thus the onset of single particle excitations can be associated with the gap energy E_g. And the E_g values could be obtained by linearly extrapolating the segment of maximum negative slope of the energy loss spectrum to the base line. Fig. 2.3 gives an example showing energy gap measurement of SiO_2 by means of high resolution XPS O 1*s* energy loss spectrum [9]. The gap energy determined is about 9 eV, which is in agreement with that decided by optical measurement.

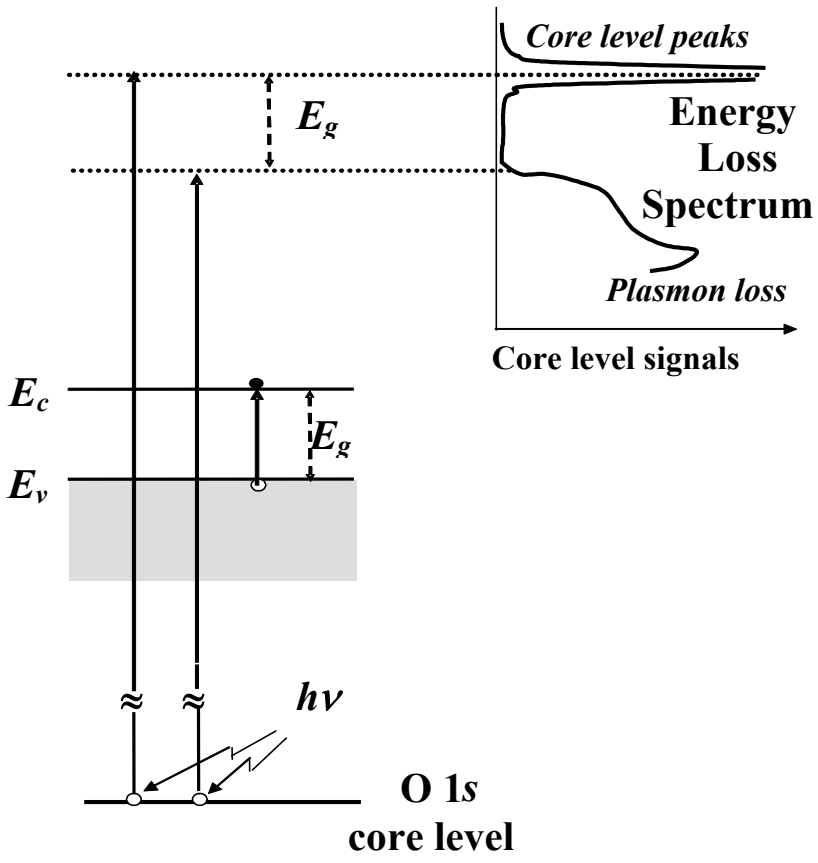


Fig. 2.2. Schematic diagram showing the formation of O 1s energy loss spectrum

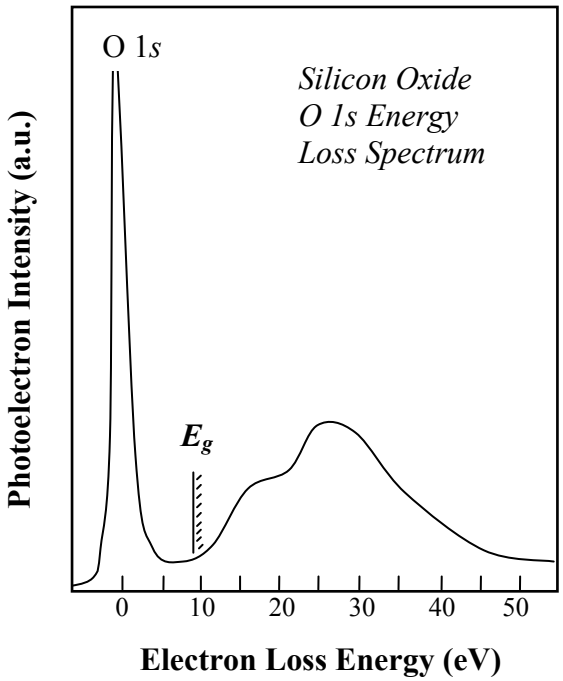


Fig. 2.3. An example showing energy gap measurement of SiO_2 by means of XPS O 1*s* energy loss spectrum

2.2.2.4 The Determination of Valence (Conduction) Band Offset between a Dielectric and the Si Substrate

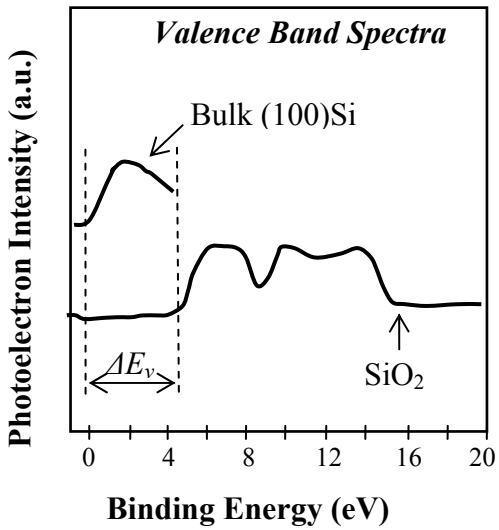


Fig. 2.4. Valence band offset for SiO_2 on (100)Si determined by XPS

By measuring the energy difference between the valence band maximum (VBM) of the dielectrics and the Si substrate, the valence band offset value (ΔE_v) could be determined. The valence band maximum value could be obtained by linearly extrapolating the leading edge of valence band spectrum to the baseline. Fig. 2.4. shows such a case to determine the ΔE_v value between SiO_2 and (100)Si substrate, which is ~ 4.5 eV [10].

The conduction band offset ΔE_c can therefore be derived using the Si energy gap value of 1.12 eV, using the following equation:

$$\Delta E_c = E_g - \Delta E_v - 1.12\ (eV) \qquad \textbf{(2-3)}$$

2.3 Experimental

Totally five $(HfO_2)_x(Al_2O_3)_{1-x}$ samples of various x values prepared by atomic layer deposition (ALD), with low-doped p-type (100)Si wafers as substrates ($n_a \sim 10^{15}$ cm^{-3}) were studied in this work. A thin layer of oxide around 10 Å was thermally grown on each Si wafer after the pre-gate clean using HF-last. The wafers were sent to *GENUS inc*. in the united states for ALD Hf aluminates deposition and a pre-HF vapor clean to remove the oxide was conducted prior to the deposition of the dielectric films. Trimethyl aluminum (TMA, $Al(CH)_3$), hafnium tetrachloride ($HfCl_4$), and water (H_2O) were used as precursors, and nitrogen was employed as carrier and purge gas. The $HfCl_4$ source is heated to ~ 160 – 165ºC to attain sufficient vapor pressure. Hf-Al-O composite films were formed by switching between the metal

precursors, TMA and $HfCl_4$, while H_2O pulse follows every metal pulse. For average growth rates of 0.6-0.9 Å/cycle, it takes 3 – 5 cycles to complete one oxide monolayer. Accordingly, by using different metal precursor pulsing sequence, composite oxides could be engineered. The deposition temperature for the ALD process is ~300^oC. Both thick films (with thickness of ~ 200 Å by ellipsometer) and thin films (with thickness of ~ 5 nm) with different composition were prepared using the same process recipes.

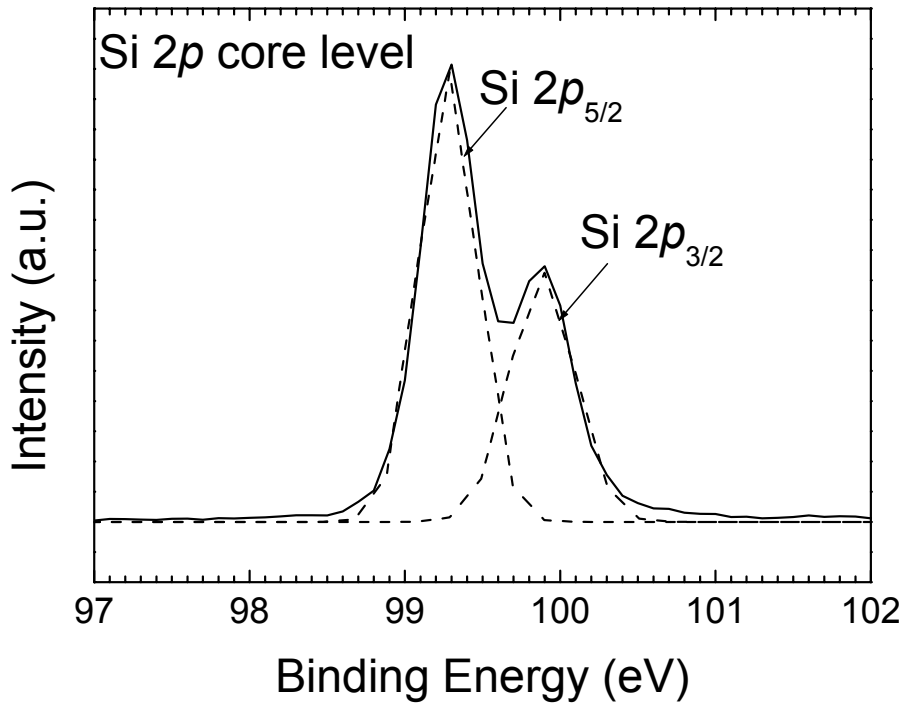


Fig. 2.5. Si 2p core level spectrum recorded from hydrogen terminated p-Si surface (Na ~ 10^{15} /cm^3) and the FWHM of Si $2p_{5/2}$ is measured as ~ 0.45 eV.

The ex-situ XPS measurements were carried out using a VG ESCALAB 220i-XLi system, equipped with a monochromatized Al $K\alpha$ source ($h\nu$ = 1486.6 eV) for the excitation of photoelectrons. All of the high-resolution scans were taken at a

photoelectron take-off angle of 90° and with a pass energy of 20 eV. Under such configurations, the full width at half maximum (FWHM) of Si $2p_{5/2}$ core level recorded from H-terminated Si surface was measured as ~ 0.45 eV (as shown in Fig. 2.5.), which gives an indication of the instrument energy resolution.

The chemical compositions of various thick $(HfO_2)_x(Al_2O_3)_{1-x}$ samples [change from HfO_2 (x = 1) to Al_2O_3 (x = 0)] can be determined XPS information. The five samples are denoted as HAO-1 to HAO-5 respectively, and their corresponding elemental compositions as well as the value of x are given in Table-2.3.1. The Hf atomic percentage (at.%) = $\frac{x}{5-2x}$ and the Al at.% = $\frac{2(1-x)}{5-2x}$ are determined by the intensities of XPS lines. All the samples show good stoichiometry and trace amount of carbon (~ 5 at. %) were detected from all of the samples surfaces.

Table 2.1. Elemental composition of various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples (labeled as from HAO-1 ~ HAO-5) estimated by XPS. The HfO_2 mole fraction value *x* as in $(HfO_2)_x(Al_2O_3)_{1-x}$ are also given in the table.

	HAO-1 (HfO_2)	HAO-2	HAO-3	HAO-4	HAO-5 (Al_2O_3)
Hafnium at.%	33.9%	25.8%	18.4%	9.6%	0
Aluminium at.%	0	9.2%	18.2%	27.7%	39.8%
Oxygen at.%	66.1%	65%	63.4%	62.7%	60.2%
HfO_2 mole fraction value x as in $(HfO_2)_x(Al_2O_3)_{1-x}$	1	~0.85	~0.67	~0.41	0

$(HfO_2)_x(Al_2O_3)_{1-x}$ films crystallinity is evaluated with x-ray diffraction (XRD). Crystallization temperature is estimated based on the XRD results for films annealed at 400 to 1000ºC for 20 s in N_2 ambient. The thick films are used for the XRD studies in order to achieve good signal to noise ratio.

The thick $HfAl_xO_y$ dielectric films were also used to study the band alignment of $(HfO_2)_x(Al_2O_3)_{1-x}$ to (100) Si substrate by the high resolution XPS measurement. Al 2*p*, Hf 4*f*, C 1*s*, O 1*s*, valence band maximum (VBM), and O 1*s* energy loss spectra were measured and analyzed. The intensities for all the XPS spectra reported here have been normalized for comparison and all of the spectra are calibrated against C 1*s* peak (285.0 eV) of adventitious carbon.

The thin $HfAl_xO_y$ dielectric films received rapid thermal annealing (RTA) conducted in either 10 torr of N_2 or in high vacuum (~ 2×10^{-5} torr) at several temperatures (800°C – 1000°C) for 20 seconds to the thin films. Thickness for the as-deposited high-K thin films determined by TEM are ~ 5.5 nm [HfO_2], ~ 4.4 nm [$(HfO_2)_{0.85}(Al_2O_3)_{0.15}$], ~ 4.2 nm [$(HfO_2)_{0.67}(Al_2O_3)_{0.33}$], and ~ 4.6 nm [$Al_2O_3$]. The thermal stability for the thin $(HfO_2)_x(Al_2O_3)_{1-x}$ and its impact on oxygen diffusivity through the $HfAl_xO_y$ dielectric films were evaluated using XPS and cross-sectional transmission electron microscopy (TEM).

2.4. Energy Gap and Band Alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si

2.4.1 Hf 4*f*, Al 2*p*, and O 1*s* Core Level Spectra

XPS spectra for Hf 4*f* and Al 2*p* core levels are shown as in Fig. 2.6 (a) and (b). It is observed that the core level peak positions of both Hf 4*f*, and Al 2*p* experience a shift to higher binding energy with the increase of Al composition in $(HfO_2)_x(Al_2O_3)_{1-x}$ system, and these changes are similar to the XPS chemical shifts in $ZrSiO_4$ versus SiO_2 and ZrO_2 as discussed in reference [11]. The above shift is due to the fact that Hf is a more ionic cation than Al in $(HfO_2)_x(Al_2O_3)_{1-x}$ [12], and thus the charge transfer contribution for Al and Hf atoms will increase with the increase of Al composition [11,12]. The core levels positions will shift in a similar way as partial charge contribution.

O 1*s* core level spectra are shown as Fig. 2.7. The O 1*s* core level peak positions are also observed to shift continuously towards greater binding energy with increasing of Al components, and the reason for this shift is the same as analyzed for Al 2*p* and Hf 4*f* core levels.

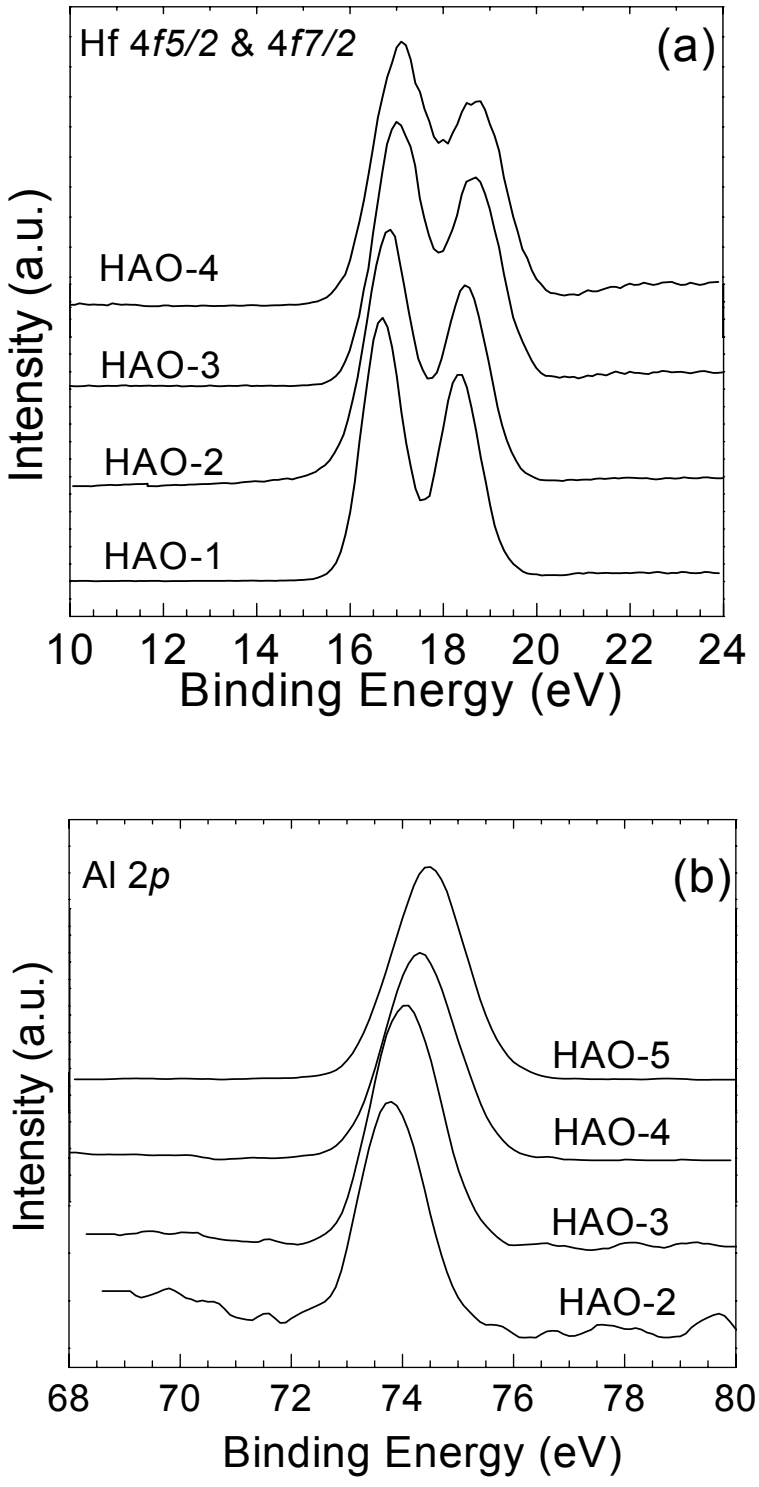


Fig. 2.6 XPS spectra for (a) Hf 4*f* and (b) Al 2*p* core levels taken from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples. The core level peak positions of both Hf 4*f* and Al 2*p* shift continuously towards greater binding energy with increasing of Al components. The intensities for all the XPS spectra reported have been normalized for comparison.

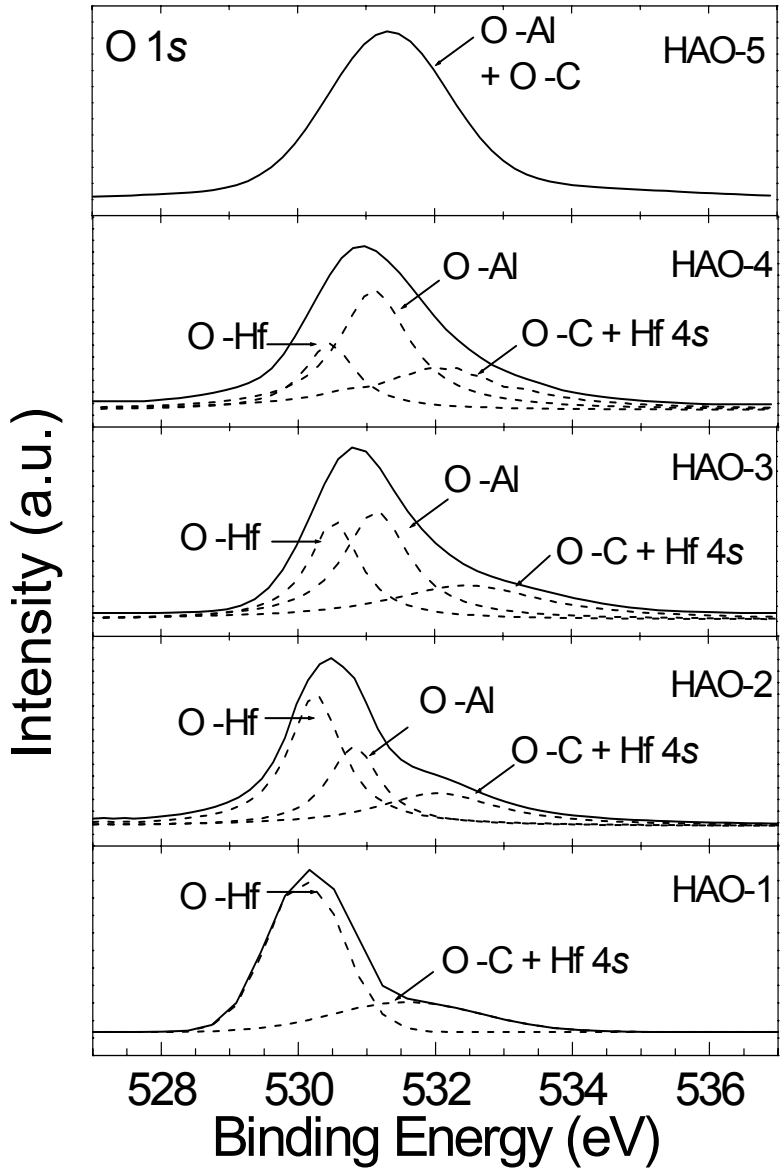


Fig. 2.7. XPS spectra for O 1*s* core level taken from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples. The core level peak positions shift continuously towards greater binding energy with increasing of Al components. Solid lines are experimental data and dashed lines are the curve fitting results.

For the experimental results (the solid lines) in figure 2.7, a curve-fitting method (the dashed lines) is applied to analyze the variation in O 1s spectra shape. For the samples HAO-2, HAO-3, and HAO-4, three peaks can be clearly resolved. The peak located at ~ 530.5 eV is attributed to Hf-O bonds, and another peak at ~ 531.2 eV to Al-O bonds. From the curve-fitting results as well as the O 1s spectra

collected from HfO_2 (HAO-1) and from Al_2O_3 (HAO-5), it is obvious that Al-O components increase with increasing Al in $(HfO_2)_x(Al_2O_3)_{1-x}$. The shoulder at ~ 532.3 eV is generally interpreted as due to residual surface contaminants (i.e. C-O bonds) [13] and it is observed that this shoulder decreases with the decrease of Hf component in $(HfO_2)_x(Al_2O_3)_{1-x}$. It should be noticed that Hf 4*s* photoelectron line is also located around this energy [7]. Therefore, it is suggested that both of the above-indicated sources contribute to the peak at ~ 532.3 eV.

2.4.2. Gap Energy, Valence Band Offset, and Conduction Band Offset to (100) Si Substrate

Let us turn to the topic of energy band alignment to (100)Si substrate for the $(HfO_2)_x(Al_2O_3)_{1-x}$. Fig. 2.8 shows the O 1*s* energy-loss spectra, which are caused by the outgoing photoelectrons suffering inelastic losses to collective oscillations (plasmon) and single particle excitations (band to band transitions). The energy gap values for the dielectric materials can be determined by the onsets of energy loss from the energy-loss spectra [14,15]. By this means, the energy gap value for HfO_2 (sample HAO-1) is measured as 5.25 ± 0.10 eV, and for Al_2O_3 (sample HAO-5) it is measured as 6.52 ± 0.10 eV. The energy gap value of Al_2O_3 is consistent with those reported by Itokawa *et al* [14] (6.55 ± 0.05 eV) and Bender *et al* [16] (6.7 ± 0.2 eV). From the results, a linear change of energy gap value with *x* in the $(HfO_2)_x(Al_2O_3)_{1-x}$ system could be also observed. In addition, we notice the continuous change in the energy loss spectra contour from sample HAO-1 to HAO-5.

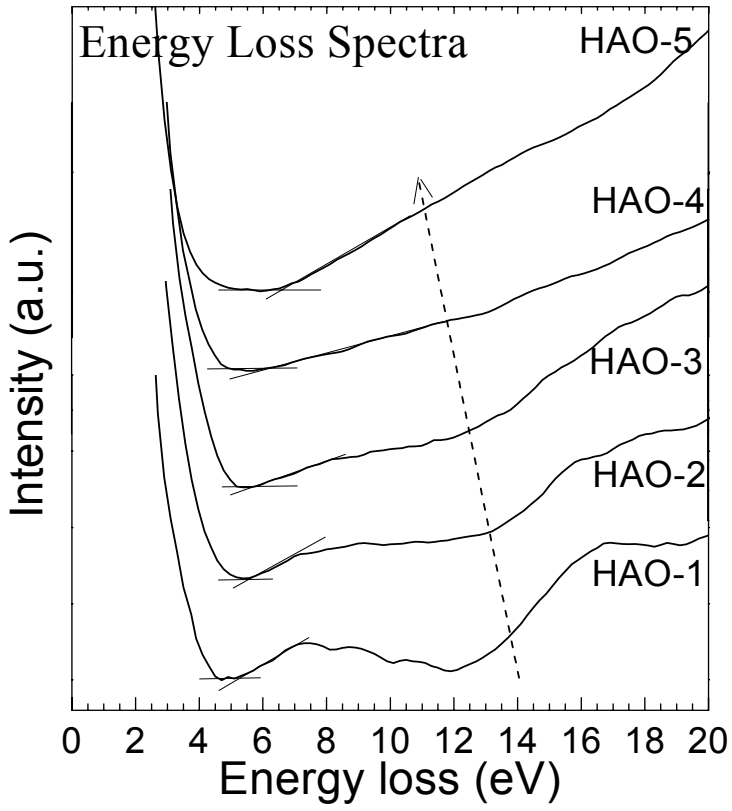


Fig. 2.8. O 1*s* energy-loss spectra for various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples. The cross points (obtained by linearly extrapolating the segment of maximum negative slope to the base line) denote the energy gap E_g values. Dashed arrow shows the continuous change in the energy loss spectra contour from sample HAO-1 to HAO-5.

The determination of valence band alignment of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si substrate was performed by measuring the difference of valence band maximum (VBM) between the $(HfO_2)_x(Al_2O_3)_{1-x}$ grown on p-Si(100) substrate samples and the H-terminated p-Si (100) substrate sample with the same substrate doping of $n_a \sim 10^{15}$ cm^{-3}, as demonstrated in Fig. 2.9. The valence band maximum for each sample is obtained by extrapolating the leading edge of valence band spectrum to the baseline (the cross points in Fig. 2.9) from its specific spectrum. Therefore, ΔE_V values of 3.03 ± 0.05 eV and 2.22 ± 0.05 eV are obtained for Al_2O_3 and HfO_2 respectively. The ΔE_V value of Al_2O_3 is consistent with the value 2.9 ± 0.2 eV reported by Bender *et al*

[16]. Another noteworthy point is that a gradual change in the valence band density of states (VBDOS) is also observed from sample HAO-1 to HAO-5.

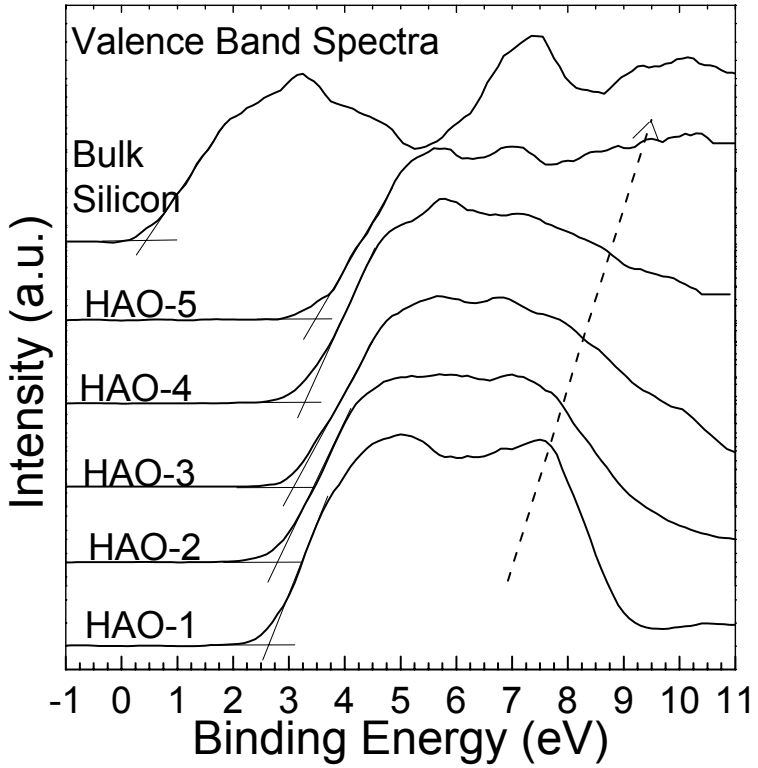
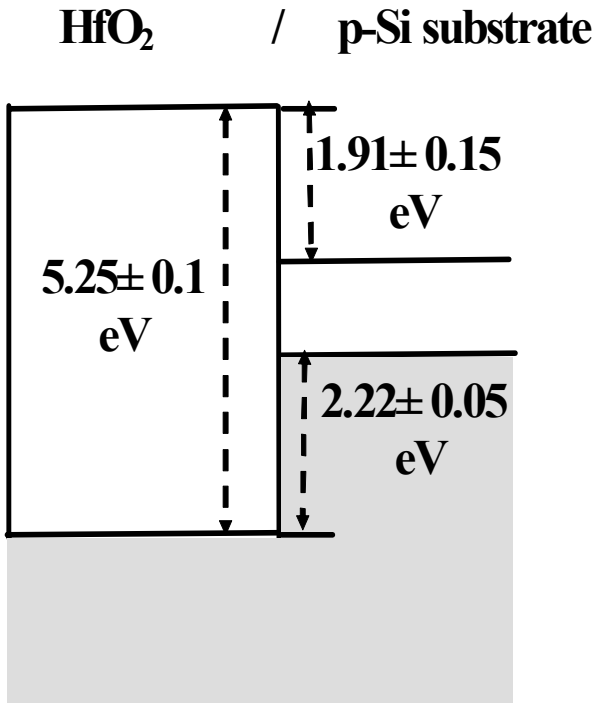


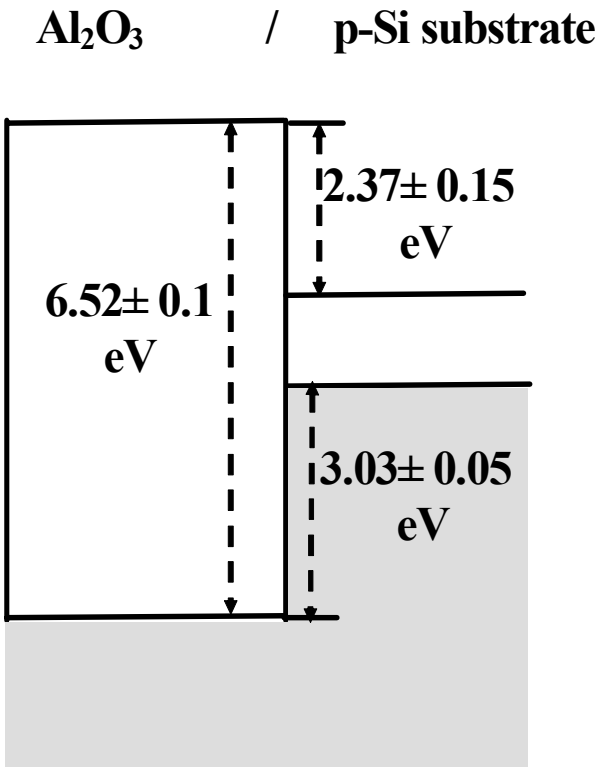
Fig. 2.9. XPS valence band spectra taken from various $(HfO_2)_x(Al_2O_3)_{1-x}$ grown on (100) Si substrate samples and H-terminated (100) Si substrate sample. The dashed arrow indicates the gradual change in the valence band density of states from sample HAO-1 to HAO-5.

With the knowledge of Si energy gap value of 1.12 eV, the ΔE_C values for $(HfO_2)_x(Al_2O_3)_{1-x}$ can be simply derived by the equation of 2-3

$$\Delta E_c = E_g - \Delta E_v - 1.12\ (eV) \qquad (2\text{-}3)$$



(a)



(b)

Fig. 2.10. Schematic energy band alignment of (a) HfO_2 and (b) Al_2O_3 on (100) Si substrate based on XPS measurements.

Hence ΔE_C for HfO_2 is calculated as 1.91 ± 0.15 eV and for Al_2O_3, it is calculated as 2.37 ± 0.15 eV. Afanas'ev et al reported 3.23 ± 0.08 eV for the (100) Si valence band to Al_2O_3 conduction band offset, measured by internal photoemission [17]. Considering 1.12 eV energy gap for Si, the Si to Al_2O_3 conduction band offset ΔE_C is calculated to be 2.11 ± 0.08 eV, which in turn, is in reasonable agreement with our XPS result.

Fig. 2.10 (a) and (b) depict the schematic energy band alignment of HfO_2 and Al_2O_3 on Si respectively based on XPS information. Note that both ΔE_c and ΔE_v for Al_2O_3 are greater than those for HfO_2.

The E_g, ΔE_v, and ΔE_c values obtained by XPS measurements and by eq. (2-3) for samples HAO-1 to HAO-5 are plotted in Fig. 2.11.

By linear least square fit, the following equations are obtained:

$$E_g = 6.52 - 1.27x \text{ (eV)}; \quad \textbf{(3-4a)}$$

$$\Delta E_v = 3.03 - 0.81x \text{ (eV)}; \quad \textbf{(3-4b)}$$

Where x stands for the mole fraction of HfO_2 in $(HfO_2)_x(Al_2O_3)_{1-x}$, as is clearly demonstrated in table 1. From the results, a linear change of energy gap value with x in the $(HfO_2)_x(Al_2O_3)_{1-x}$ system is observed. Accordingly, the electrical properties of $(HfO_2)_x(Al_2O_3)_{1-x}$ gate dielectrics should be able to be tuned by simply changing the HfO_2 mole fraction while keeping the stoichiometry of the materials.

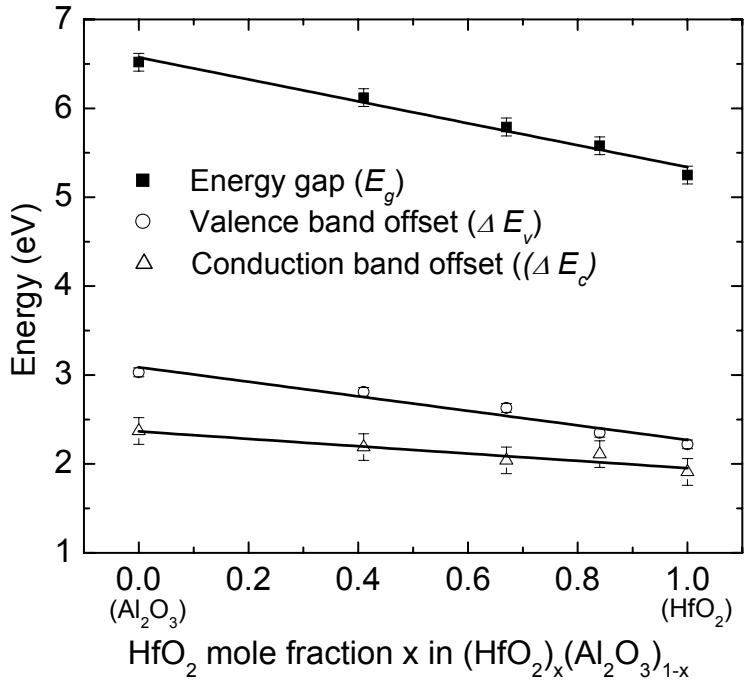


Fig. 2.11. Dependence of E_g, ΔE_v, and ΔE_c for $(HfO_2)_x(Al_2O_3)_{1-x}$ on HfO_2 mole fraction x. The E_g and ΔE_v data are obtained by XPS measurements. The ΔE_c data are calculated by eq (2-3). The solid lines are obtained by linear least square fits of the data points.

2.5. Thermal Stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si

2.5.1. XPS Study

High-resolution XPS was used to quantitatively describe the growth of the interfacial layer (IL) between $(HfO_2)_x(Al_2O_3)_{1-x}$ films and Si substrate during high temperature rapid thermal annealing (RTA) process. The Si 2*p* core level XPS spectra for the as-deposited sample and the samples after RTA annealing in 10 torr of N_2 for 20 sec at various temperature (800°C, 900°C, and 1000°C) are shown in Fig. 2.12.

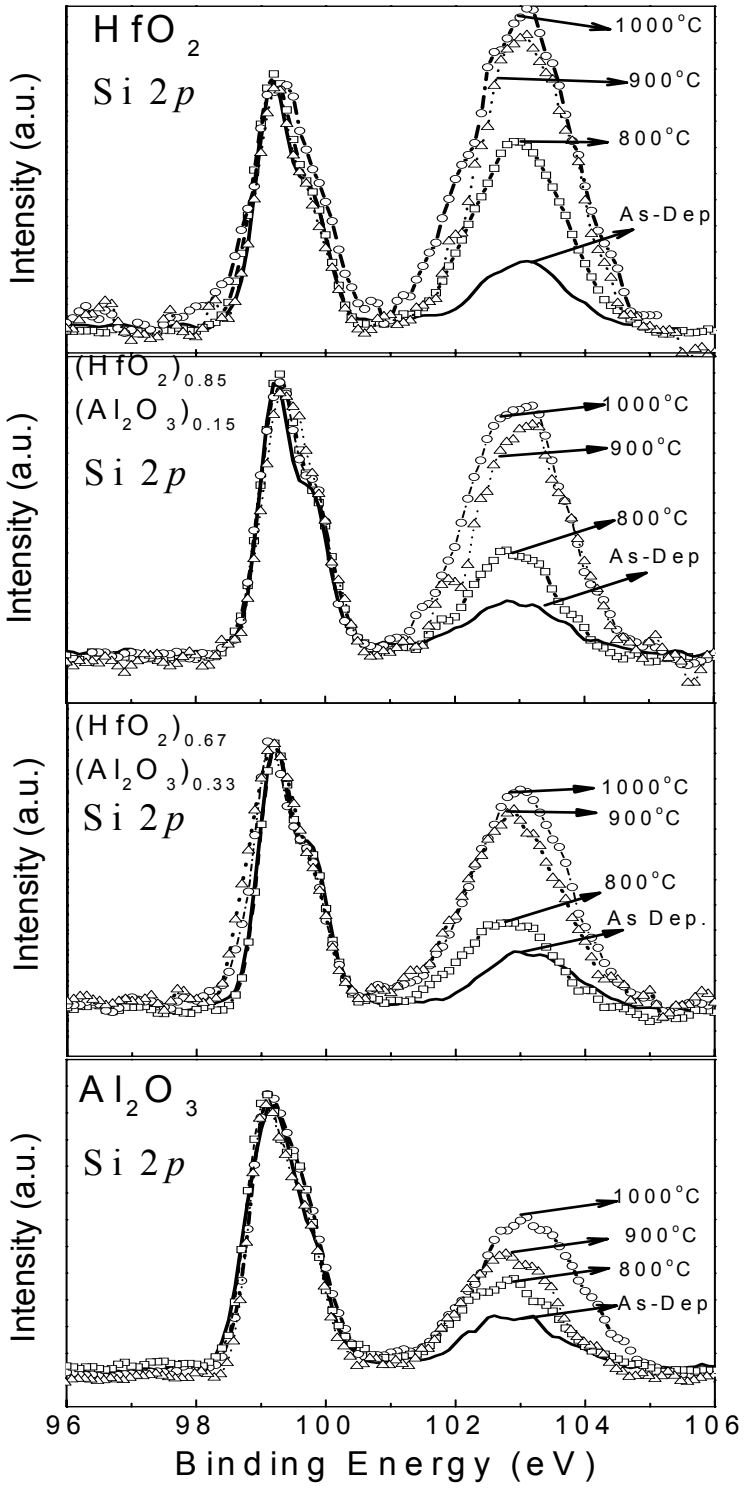


Fig. 2.12. XPS Si 2p core level spectra recorded from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples of as-deposited, after 10 torr of N_2 rapid thermal annealing at 800°C, 900°C, 1000°C respectively. The peak located at ~99.3 eV is assigned to Si-Si bonds from the substrates, and the one at ~103.0 eV to Si-O bonds from IL. The intensities for XPS peaks of Si-Si bonds have been normalized for comparison.

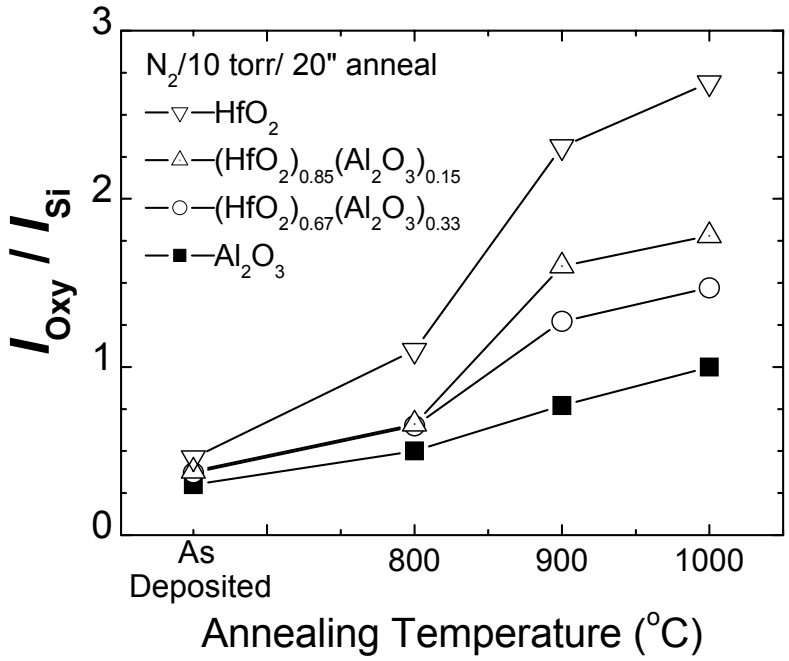


Fig. 2.13. The ratio of I_{Oxy}/I_{Si} for various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples versus the different annealing conditions based on XPS spectra in Fig. 2.12. The change in this ratio directly correlates with the variation of the IL growth.

The peak located at ~ 99.3 eV is attributed to Si-Si bonds from Si substrates, and the one at ~ 103.0 eV to Si-O bonds from the interfacial layer [7]. For the sake of comparison, the intensities of XPS peaks of Si-Si bonds have been normalized. From the Fig. 2.12, it is obvious that an IL exists for all of the as-deposited samples. For better understanding, the ratio of I_{Oxy}/I_{Si} for each sample with the different annealing conditions is plotted in Fig. 2.13. I_{Oxy} and I_{Si} are determined by integrating the Si-O and Si-Si peak area respectively after a Shirley background subtraction. The change in the ratio of I_{Oxy}/I_{Si} directly reflects the variation of the interfacial layer growth: the higher the ratio, the thicker the IL. In the case of annealing in N_2, IL thickness increases with increasing temperature for all of the four samples. For a given annealing temperature, the extent of IL growth is determined versus Al%, with HfO_2 film (0% Al) showing the largest growth, and Al_2O_3 film the smallest. Doping of HfO_2 film with Al slows down the IL growth during annealing. Based on these XPS

results, one can draw the conclusion that the ability to block oxygen diffusion through HfO_2 films is greatly enhanced by the incorporating of Al, and the ability becomes stronger when more Al is incorporated.

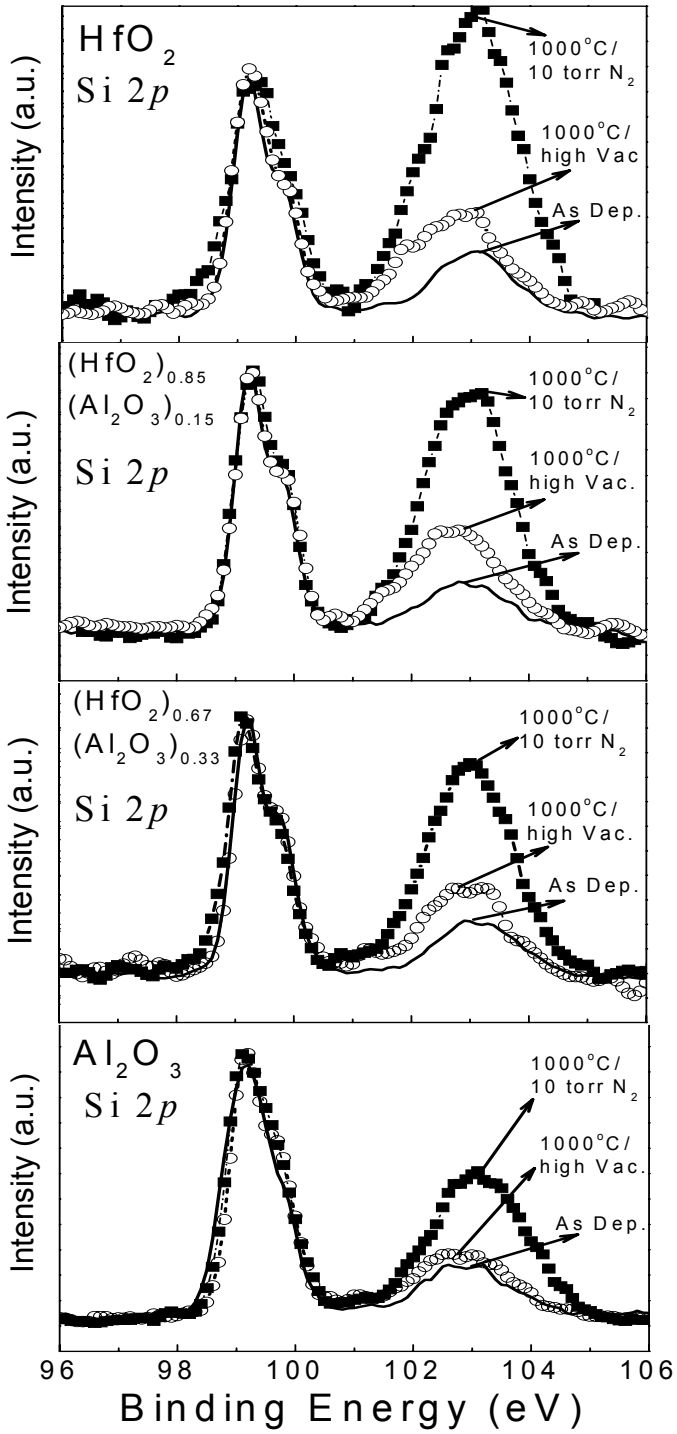


Fig. 2.14. XPS Si 2p core level spectra recorded from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples of as-deposited, after 1000°C RTA in 10 torr of N_2 and in ~ 2×10^{-5} torr of high vacuum respectively. The intensities for XPS peaks of Si-Si bonds have been normalized.

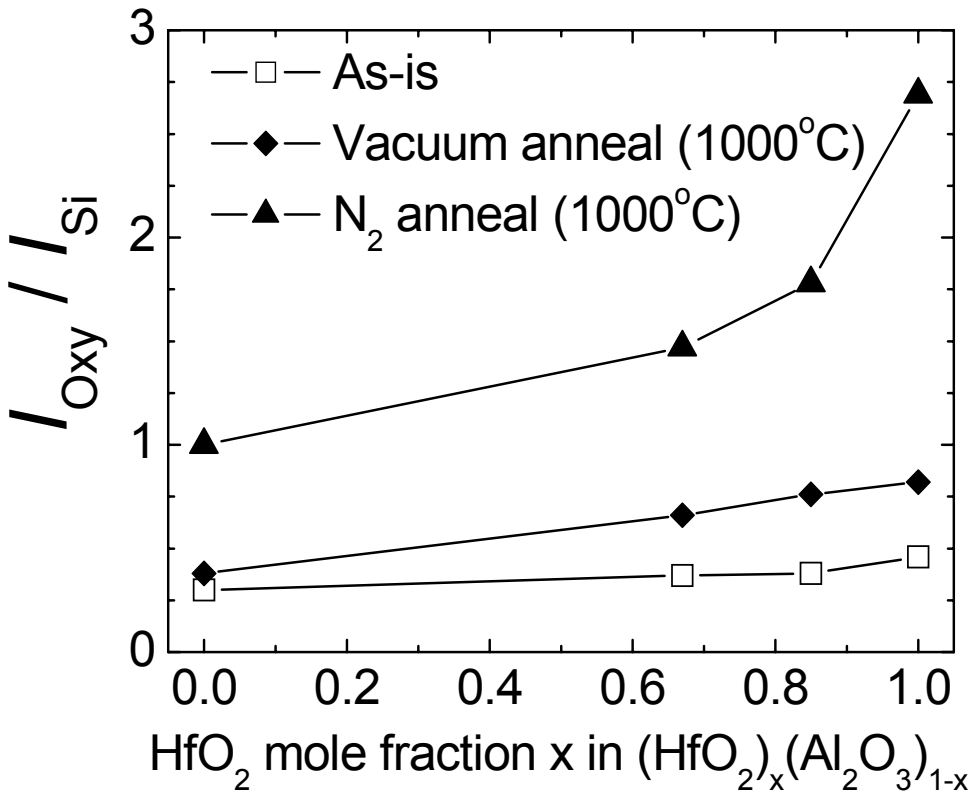


Fig. 2.15. The ratio of I_{Oxy}/I_{Si} for various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples versus the different annealing conditions based on XPS spectra in Fig. 2.14.

The Si 2*p* core level XPS spectra recorded from the as-deposited sample, and the samples after RTA annealing at 1000°C for 20 sec at different annealing gas atmosphere (10 torr of N_2, and ~ 2×10^{-5} torr of high vacuum) are shown in Fig. 2.14. Fig. 2.15 plots the ratio of ratio of I_{Oxy}/I_{Si} corresponding to the respective samples in Fig. 2.14. For the samples annealing in high vacuum, although the changes of I_{Oxy}/I_{Si} for these four samples show the same trend as that of annealing in N_2, these ratios are significantly smaller than those of annealing in N_2 at the same temperature. This result implies that the active source of oxygen in N_2 ambient, not the oxygen species present in the high-K films themselves, is mostly likely to be responsible for the IL growth during RTA.

It should also be noted that no Hf silicide (Hf-Si bonding) was detected from the Hf 4f core level scans (data not shown) for all samples after annealing in a high vacuum at 1000 °C. This is because the pressure for annealing in our study is not low enough to trigger the formation of SiO species at the high-k / IL region, which is the key step for silicide formation [18].

2.5.2. XTEM Study

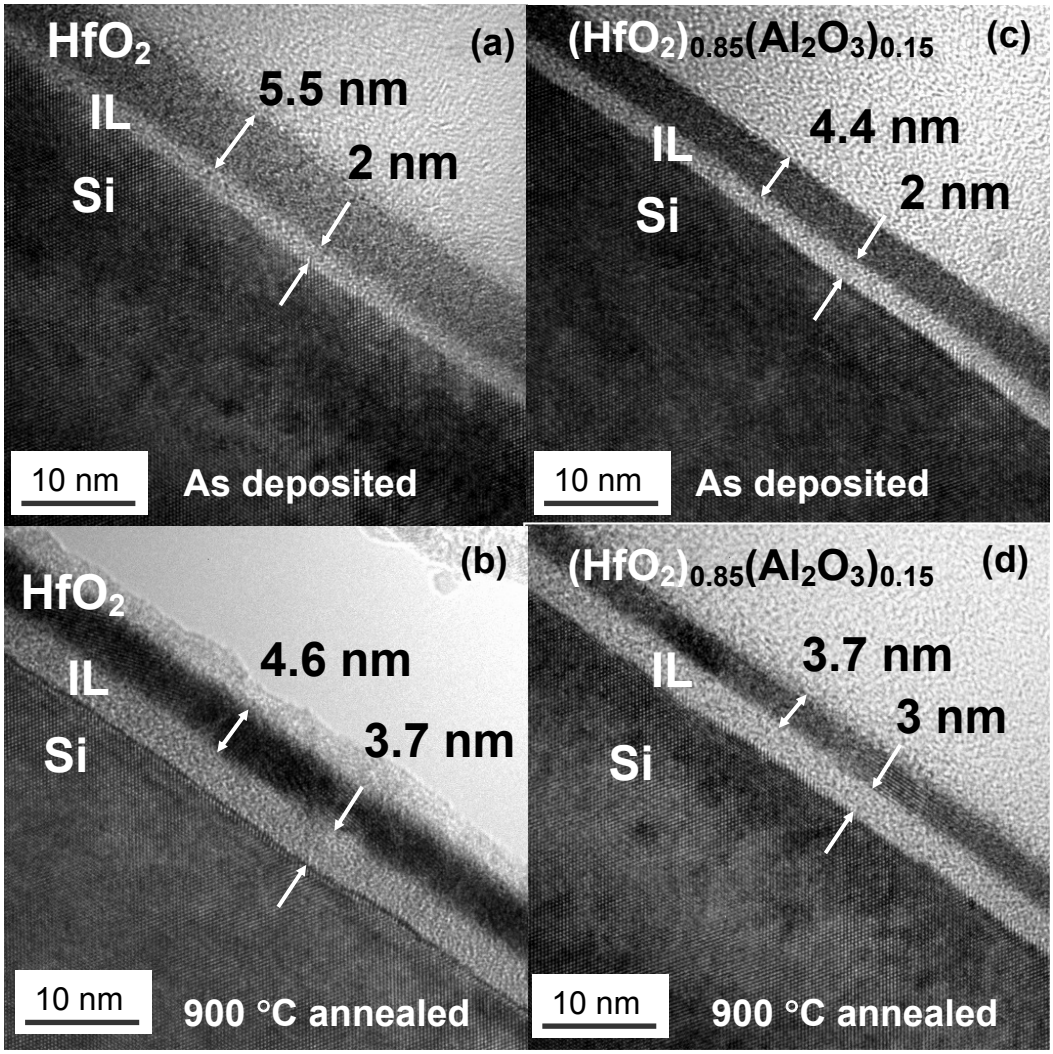


Fig. 2.16. High resolution XTEM images for of (a) the as-deposited HfO_2 sample, (b) the 900 °C/ N_2 annealed HfO_2 sample, (c) the as- deposited $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ sample, and (d) the 900 °C/ N_2 annealed $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ sample.

The high-resolution cross-sectional TEM micrographs of two samples [HfO_2 and $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ films] before and after 900 °C annealing in N_2 are presented in Fig. 2.16. After annealing, it is observed that the growth of IL is greater for the HfO_2 sample compared to the Al doped HfO_2, consistent with the XPS results shown in Figs. 2.12 & 2.13. The composition of the interfacial layer is likely to be Hf(Al) silicate (with SiO_2 rich) [19], which is supported by XPS measurements shown in Fig. 2.12. Another evidence for silicate formation is the high-K film thickness decrease after annealing, as shown by XTEM images, which may be due to the consumption of high-K films through the reaction with IL [19] and/or film densification [20].

2.5.3. XRD Study

As reported previously [6], HfO_2 film crystallization temperature is increased by alloying with Al. Our XRD study of 20-nm-thick $(HfO_2)_x(Al_2O_3)_{1-x}$ films after 900 °C annealing in N_2 also confirms this point, as depicted in Fig. 2.17. These spectra show that $(HfO_2)_{0.67}(Al_2O_3)_{0.33}$ remains amorphous after 900 °C annealing. Fig. 2.18 demonstrates that the crystallization temperatures increases with more Al incorporated [21]. These results are well correlated with the experimental observation regarding oxygen diffusion through $(HfO_2)_x(Al_2O_3)_{1-x}$ films (Figs. 2.12 and 2.13): the higher Al concentration, the higher the crystallization temperature, and hence the lower the oxygen diffusion along the grain boundaries of the high-K films which, in turn, reduces the IL growth. Another reason for the reduced rate of oxygen diffusion by the addition of Al_2O_3 is that the Al_2O_3 is known to have much lower oxygen diffusion coefficient compared to HfO_2 at high temperature [22].

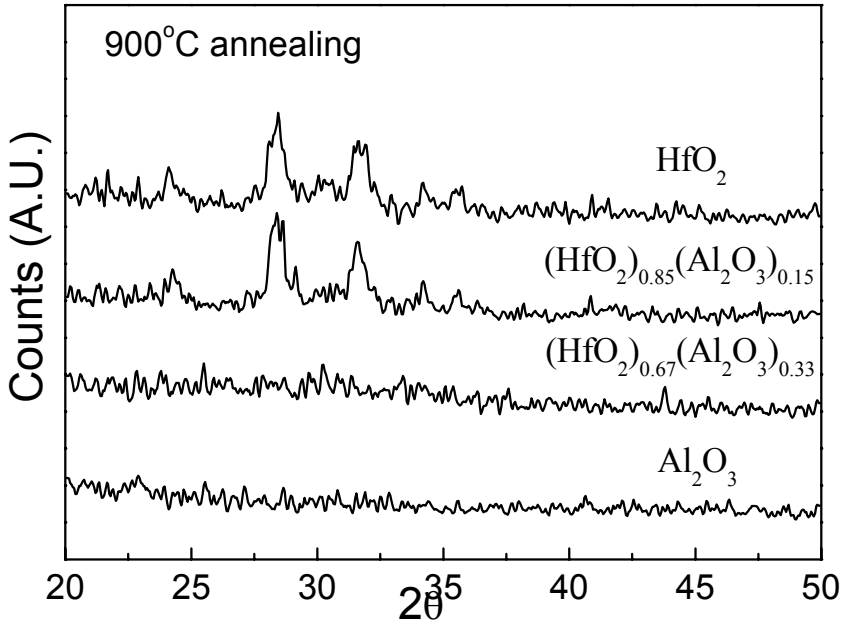


Fig. 2.17. XRD characteristics of various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples (~ 20nm) after 900 °C/ N_2 annealing.

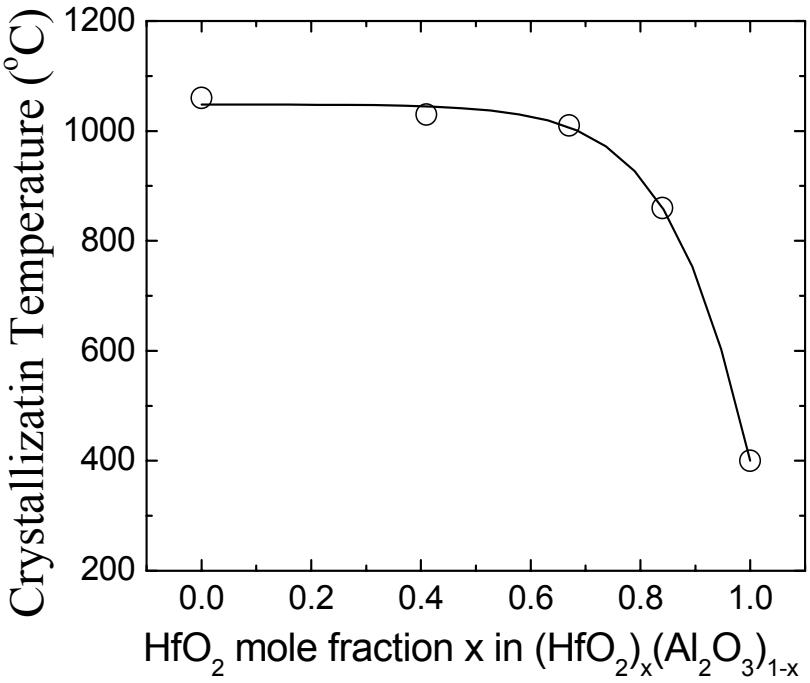


Fig. 2.18. Crystallization temperature of $(HfO_2)_x(Al_2O_3)_{1-x}$ variation with its composition [21].

2.6 Conclusion

In this chapter, the materials properties of $(HfO_2)_x(Al_2O_3)_{1-x}$ high-K dielectrics grown by ALD have been characterized, including their energy band alignment to (100) Si substrate and the thermal stability.

High resolution XPS was applied to characterize the electronic structures for $(HfO_2)_x(Al_2O_3)_{1-x}$ with different HfO_2 mole fraction x. Al 2p, Hf 4f, O 1s core levels XPS spectra, valence band spectra, and O 1s energy loss spectra all show continuous changes with x in $(HfO_2)_x(Al_2O_3)_{1-x}$. These data are used to estimate the energy gap E_g for $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset ΔE_v, and the conduction band offset ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100) Si substrate. Our XPS results demonstrate that the values of E_g, and ΔE_v for $(HfO_2)_x(Al_2O_3)_{1-x}$ change linearly with x, and the respective values can be calculated by $E_g = 6.52 - 1.27x$ (eV), and $\Delta E_v = 3.03 - 0.81x$ (eV).

We further report that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al to form Hf aluminates, and the improvement is closely correlated with the Al percentage in the films. This observation is explained by (i) Al_2O_3 has much lower oxygen diffusion coefficient than HfO_2 at high temperature; (ii) doping HfO_2 by Al raises the film crystallization temperature of HfO_2 and thus drastically reduces the oxygen diffusion along the grain boundaries during annealing. The difference of IL growth between N_2 (10 torr) and high vacuum (~ 2×10^{-5} torr) 1000 °C annealing indicates that the active oxygen

species from the annealing ambient is the main cause for the IL growth during RTA in N_2. A reduced oxygen atmosphere is therefore desired to suppress the IL growth for $(HfO_2)_x(Al_2O_3)_{1-x}$ films on Si during post deposition process.

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Chapter 3

Thermally Robust HfN Metal as a Promising Gate Electrode for Advanced MOS Device Applications

3.1 Introduction

As discussed in the first chapter of this thesis, with the aggressive scaling of the gate dielectrics electrical thickness in MOSFETs, the metal gate electrodes will be required to replace conventional poly-silicon gate due to the following pressing concerns associated with poly-Si gate: (1) poly-depletion effects, (2) high gate resistance, and (3) dopants penetration from heavily doped poly-Si into channel region. Although refractory metal nitrides such as TiN [1] and TaN [2] have been studied extensively as potential gate electrode candidates, these materials showed limited thermal stability [3,4] with considerable increase of EOT during high temperature annealing, and thus are not compatible with the conventional gate-first CMOS process. Due to the negatively larger heat of formation of HfN (also known as the most refractory metal nitride) compared to that of TiN and TaN (as shown Table 3.1), HfN is expected to possess better thermal stability with underlying gate dielectrics than TaN and TiN.

Table 3.1. Material properties of some refractory metal nitrides [5]

	HfN	TaN	TiN	ZrN
Melting Point (^{o}C)	~3330	~2950	~2950	~2950
Heat of Formation (kcal/mol)	– 88.2	– 60.3	– 80.4	– 88.0

In this chapter, a systematic study on HfN metal gate applications will be presented for both conventional SiO_2 dielectrics, and HfO_2 – one of the most promising high-K gate dielectrics. Our results show that the HfN metal possesses a mid-gap work function on both SiO_2 and HfO_2 and exhibits robust resistance against high temperature treatments (up to 1000°C) in terms of equivalent oxide thickness (EOT), work function, and leakage current stability. As a result, excellent EOT scalability of HfN/HfO_2 gate stack with EOT less than 1nm upon 1000^{o}C post metal annealing has been demonstrated without using a surface nitridation treatment before high-K deposition. This is significant since it is known that while surface nitridation is responsible for severe mobility degradation and CV hysteresis, it has been proved to be useful in suppressing interfacial oxide growth with other gate electrode during high temperature S/D annealing. It is proposed that the robust HfN metal gate is an ideal gate electrode candidate for fully-depleted silicon-on-insulator (FD-SOI) [6] and/or symmetric double-gate (SDG) [7] MOS devices application.

3.2 Experimental

The metal-oxide-semiconductor capacitors (MOSCAPs) studied in this work were fabricated using p-Si(100) substrates (B, $6x10^{15}/cm^{-3}$), if not otherwise stated. After the definition of the active area with 4000Å field oxide, a standard diluted hydrofluoric acid (DHF)-last RCA pre-gate clean process was applied to remove organic and metallic contamination and native oxide. For devices with SiO_2 gate dielectrics, thermal gate oxide with different thicknesses was grown using wet-oxidation technique. For devices with HfO_2 dielectrics, HfO_2 films of difference thicknesses were deposited at 400°C using $Hf[OC(CH_3)_3]_4$ and O_2 in a metal-organic chemical vapor deposition (MOCVD) cluster tool, followed by an in-situ post-deposition annealing (PDA) at 700°C in N_2 ambient for film quality improvement. Some devices received in-situ surface nitridation (SN) treatment in NH_3 at 700°C prior to CVD HfO_2 deposition. HfN films (~50nm) with 100 nm TaN as capping layer were then deposited in-situ by DC sputtering in $Ar+N_2$ mixed gas ambient. TaN is used as the capping layer to achieve a low gate sheet resistance (~10 Ω/sqr.) for the final gate scheme. Then HfN/TaN gate stack were patterned using a Cl_2– based etchant. Fig. 3.1 depicts the schematic structure of the MOS devices with the HfN/TaN metal gate stack studied in this work. For thermal stability comparison, we have also fabricated gate stack with TaN gate electrode. The MOSCAPs were then rapid thermal annealed (RTA) in N_2 at 600°C-1000°C for 20sec for thermal stability evaluation. For n- (p-) channel MOSFETs fabrication, source/drain implantation of phosphorus (BF_2) with a dose of $5x10^{15}cm^{-2}$ were performed, followed by RTA activation in N_2 at 950°C for 30s. All devices were finally subjected to back side Al metallization and sintering in a forming-gas ambient (H_2:N_2 = 1:10) at 420°C for 30min.

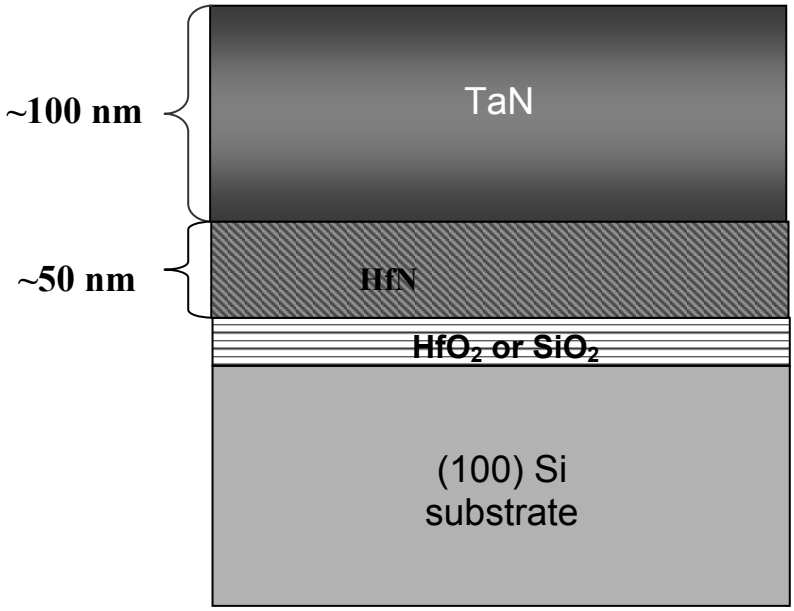


Fig. 3.1. Schematic structure of the MOS devices with the HfN/TaN metal gate stack

The capacitance-voltage (C-V) measurements were performed on large area (50x50 μm^2) MOS capacitors with an HP 4285A LCR meter at a high frequency (100 kHz). EOT and flat band voltage (V_{fb}) were simulated by taking into account the quantum mechanical correction using UC Berkeley tool. The current-voltage (I-V) characteristics were measured using an HP 4156A semiconductor parameter analyzer.

3.3 Results and Discussion

3.3.1 Material Characterization of HfN

HfN single-layered film (~200nm) was deposited on blank Si substrates (with native oxide) for material characterization. The stoichiometric HfN (Hf:N~1:1) film was deposited with Ar:N_2 flow rate ratio = 5:1 with a process pressure of 2 mTorr. The HfN films with different N concentration could be obtained by varying Ar:N_2 flow rate ratio during film deposition.

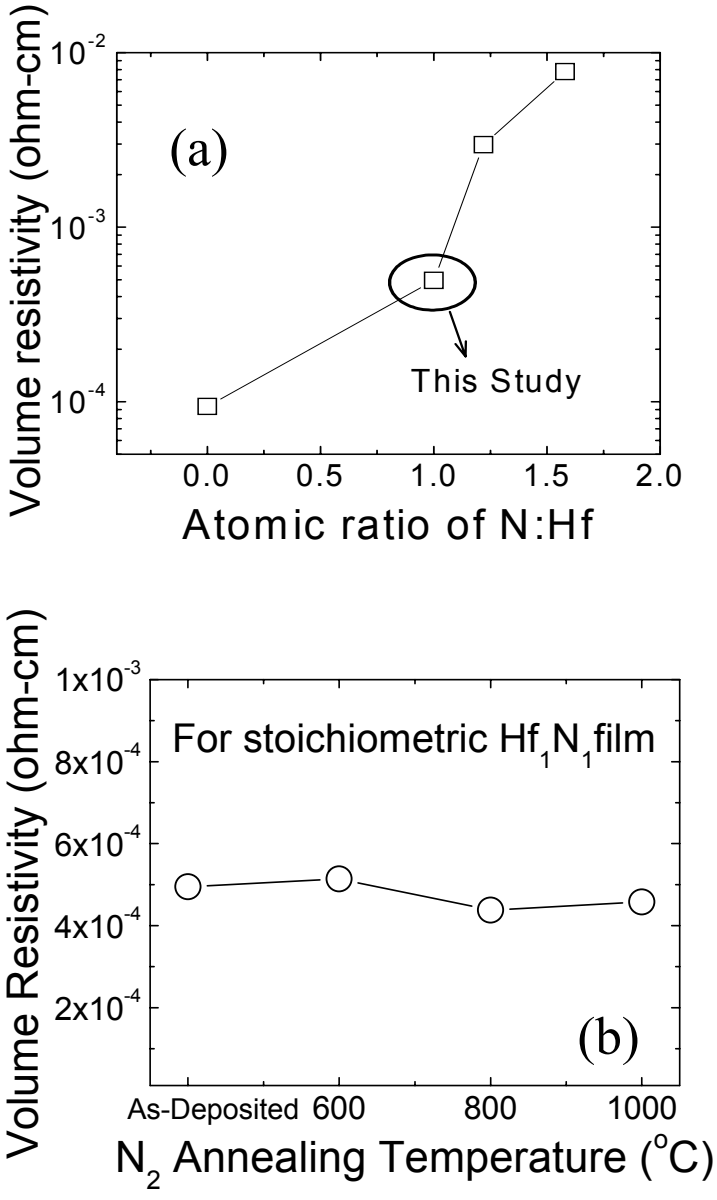
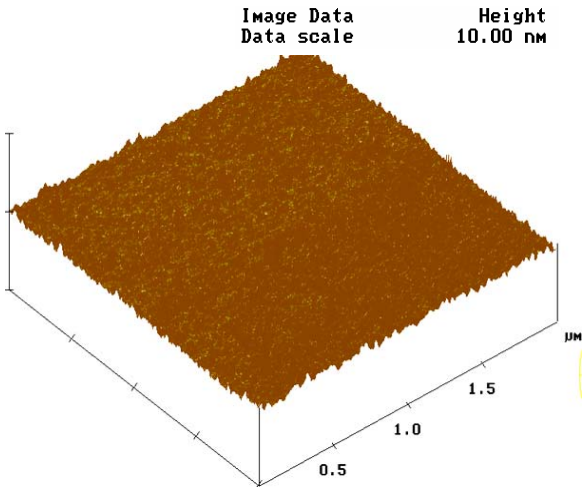
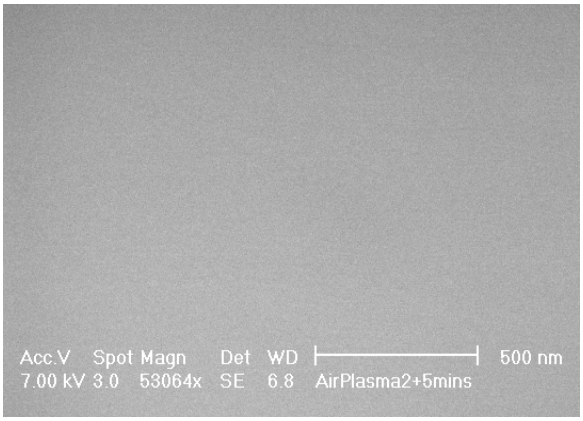


Fig. 3.2. (a) Dependence of volume resistivity (*Rv*) of HfN on HfN composition. *Rv* of pure Hf film is also shown (N:Hf = 0); (b) Dependence of volume resistivity of HfN on N_2 RTA temperature.

As shown in Fig. 3.2(a), the stoichiometric HfN (Hf:N~1:1) film exhibits the lowest volume resistivity (Rv) compared to the N-rich HfN films, and thus is used in this work. Note that the stoichiometric Hf_1N_1 volume resistivity does not change significantly under RTA treatments up to 1000^{o}C, as seen in Fig. 3.2(b).



(a)



(b)

Fig. 3.3. (a) AFM images of the PVD HfN film surface, with a RMS = 1.481nm; (b) SEM images of the PVD HfN film surface

Fig.3.3 (a) and (b) illustrate surface morphology of as-deposited HfN by atomic force microscopy (AFM), and scanning electron microscopy (SEM) respectively. The stoichiometric Hf_1N_1 film has smooth surface with a root mean square roughness (RMS) of 1.481 nm measured by AFM.

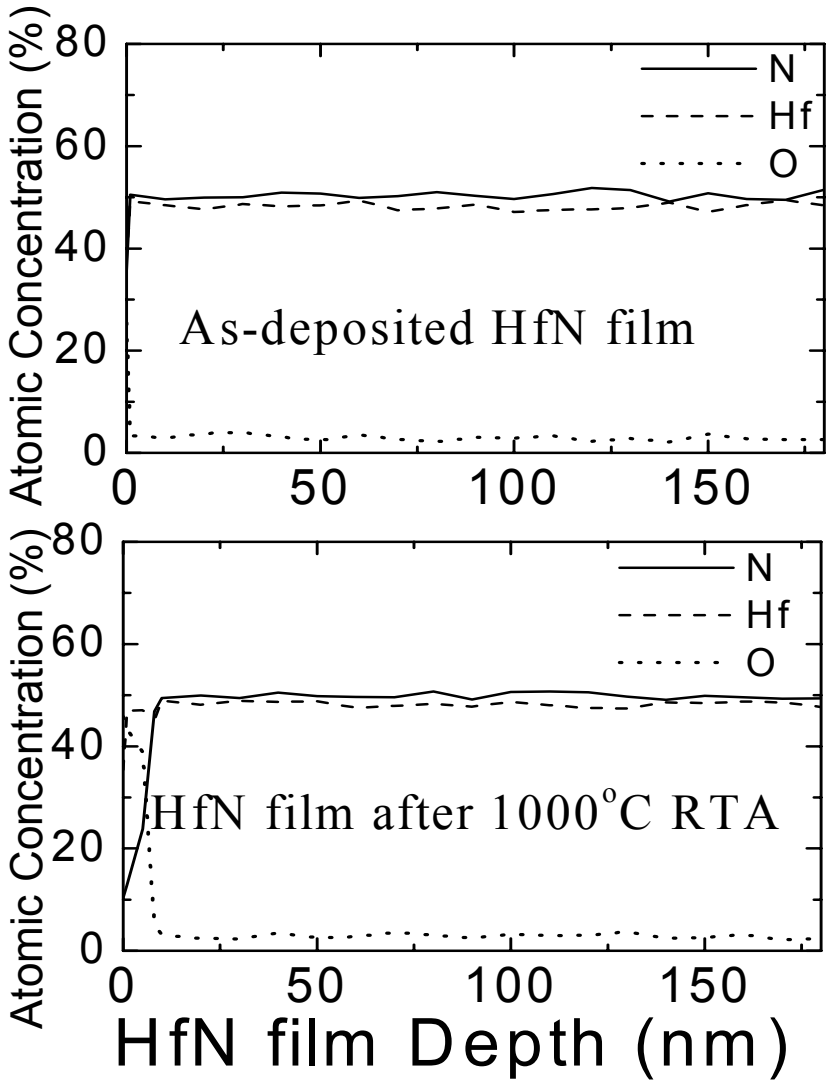


Fig. 3.4. AES depth profiles for as-deposited and 1000°C RTA treated HfN films

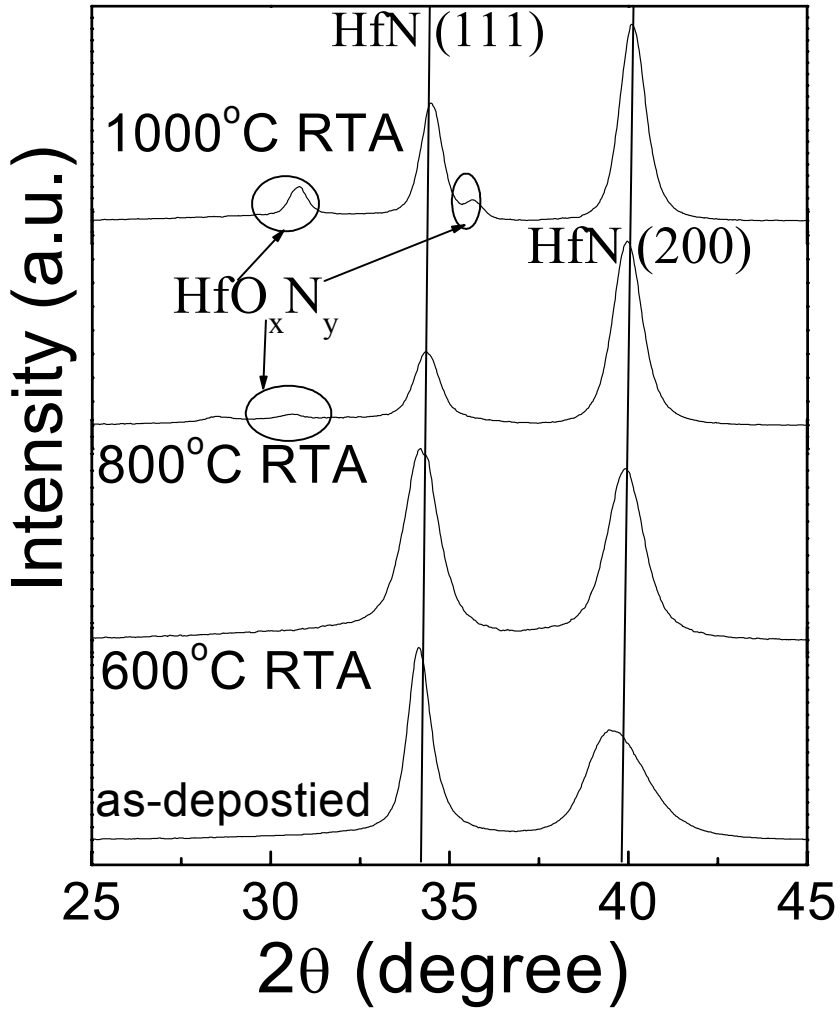


Fig. 3.5. XRD characteristics of HfN film before and after various RTA treatments. HfN crystalline planes (111) and (200) are indicated in the figure.

As demonstrated from the auger electron spectroscopy (AES) depth profile of Hf, N, and O in the single layer HfN film (Fig. 3.4), the as-deposited HfN films show stoichiometric composition (Hf:N ~ 1:1) and negligible oxygen contaminant. The HfN composition depth profile remains unchanged after 600°C rapid thermal annealing (RTA). After 800°C and 1000°C RTA, HfN film surface (~ 10 nm depth) is oxidized and converted into HfO_xN_y (Fig. 3.4). (AES depth profile of HfN after 600°C and 800°C RTA are not shown). This correlates well with the XRD results as

shown in Fig. 3.5. After 800°C and 1000°C RTA, newly generated crystalline planes are caused by the HfO_xN_y formation at the HfN surface. It is interesting to note that HfN(200) crystallization plane dominates over HfN(111) plane after 800°C and 1000°C RTA, compared to the as-deposited and 600°C RTA HfN films. The result suggests that HfN is a good oxygen diffusion barrier. Note that negligible oxygen contamination (<5 at.%) is incorporated into the HfN during film deposition process.

3.3.2 Electrical Characterization of HfN-SiO_2 Gate Stack

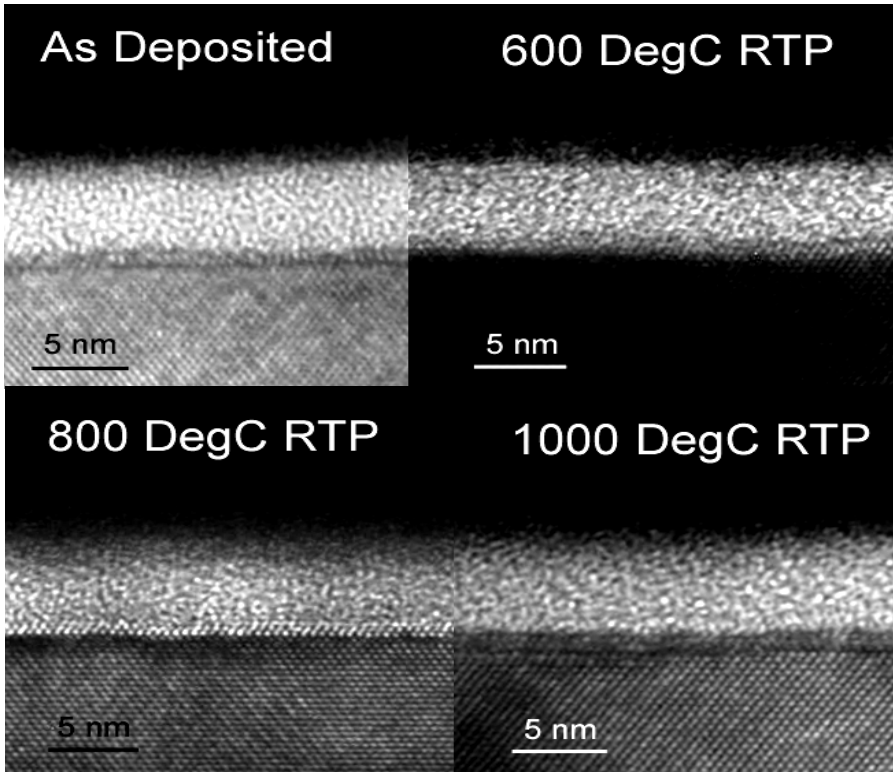


Fig. 3.6. The high-resolution cross-sectional TEM micrographs of the HfN/SiO_2/Si MOS structure before and after different RTA in N_2.

The cross sectional transmission electron microscopy (XTEM) micrographs of the HfN/SiO_2/Si MOS capacitors with SiO_2 ~ 4.5nm before and after different RTA in N_2 are presented in Fig. 3.6. As can be seen, there is no degradation of the gate oxide and the HfN/SiO_2 interface as a result of the RTA process.

The high-frequency CV measured data of all devices studied in this work well match the CV simulation results, suggesting good interface quality. One example is illustrated in Fig. 3.7, which shows the measured and the simulated CV curves for a MOS capacitor with TaN/HfN gate (SiO_2 ~ 3.12nm) after 1000°C RTA.

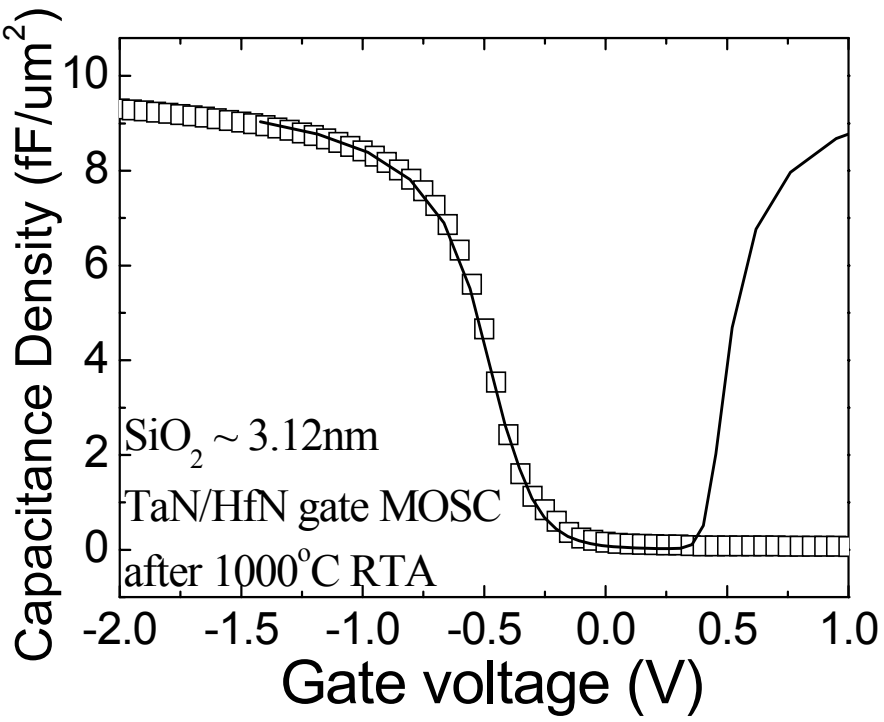


Fig. 3.7. HFCV measurement (open squares) and LFCV simulation (solid line) for a TaN/HfN gated MOS capacitor

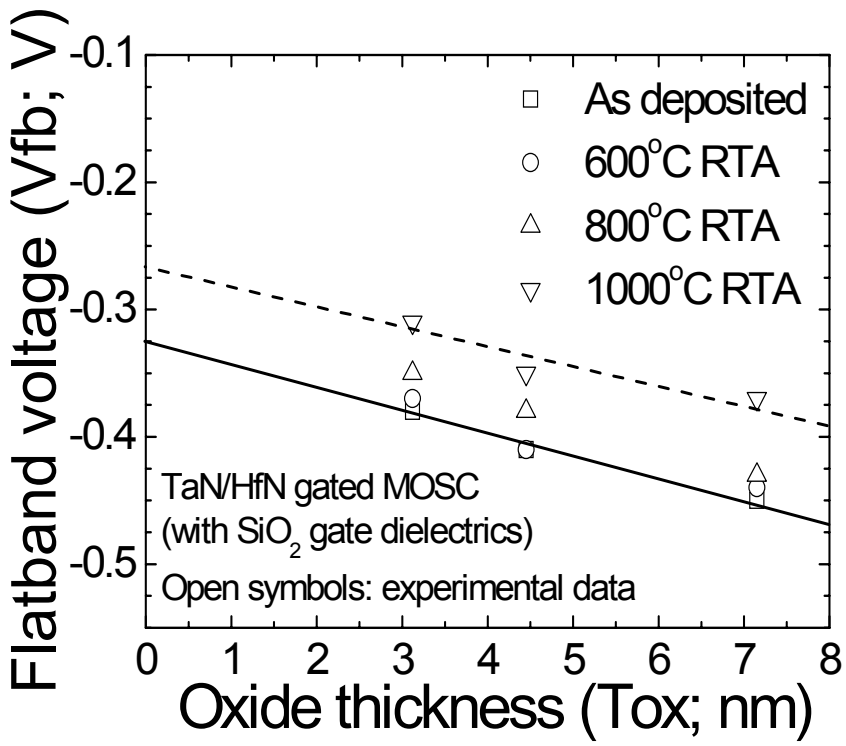


Fig. 3.8. The plot of V_{fb} versus T_{ox} (or EOT) for TaN/HfN gated MOSCAPs devices before and after various RTA treatments, with both V_{fb} and EOT extracting from CV measurements on these devices (three gate oxide thickness).

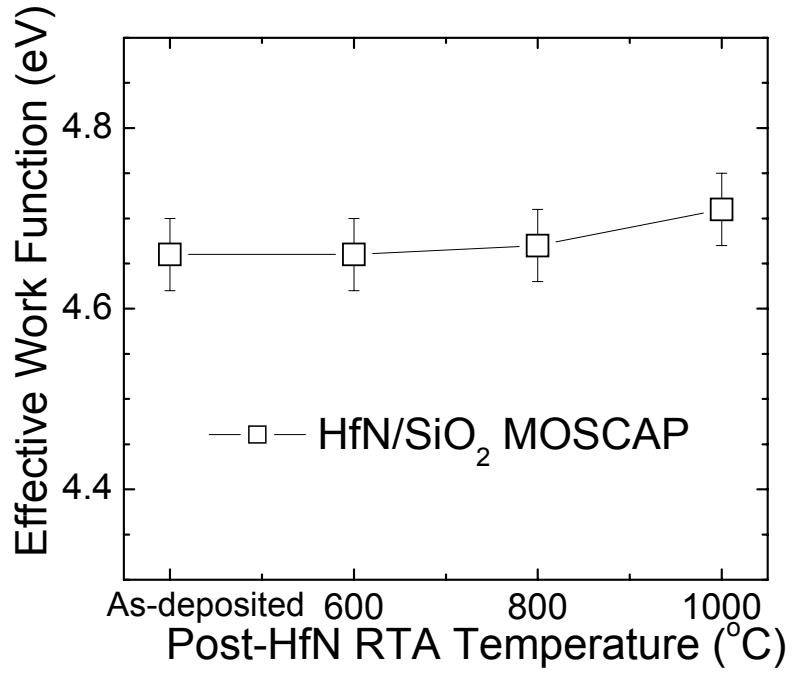


Fig. 3.9. The dependence HfN Φ_M on the N_2 RTA temperature for HfN/SiO_2 devices.

Fig. 3.8 summarizes the plot of V_{fb} versus EOT on TaN/HfN gated MOSCAP structures before and after various RTA treatments. The HfN metal gate work function (Φ_M) after various thermal treatments is extracted from this plot (as shown in Fig. 3.9), with the aid of the following equation [8],

$$\Phi_M = \Phi_{Si} + V_{fb} - Q_{ox}/C_{ox} \qquad (3\text{-}1)$$

where Q_{ox} is the equivalent oxide charge per unit area, C_{ox} is the oxide capacitance, and Φ_{Si} is the work function of Si substrate. The work function of as-deposited HfN is about 4.65 eV, and is kept as constant after 600°C RTA. The work function slightly increases after 800°C RTA (~ 4.67 eV), and after 1000°C RTA (~ 4.71 eV). The small amount of work function increase after RTA is suggested to be due to the change of HfN crystallization, as shown in Fig. 3.5, or be due to the different interface dipole formation originated from various thermal treatments to HfN/SiO_2 interface.

The superior electrical stability of the HfN-SiO_2 gate stack under RTA treatments is demonstrated in Fig. 3.10, where the device EOT are plotted as a function of N_2 RTA temperature. The results show that the EOT variations in all devices are negligible up to 1000°C RTA, indicating robust thermal stability of the HfN metal gate. Fig. 3.11 demonstrates stability of gate leakage current of the TaN/HfN gated devices (SiO_2~3.12nm) after the various RTA treatments. Therefore, the mid-gap HfN metal electrode with superior thermal stability is highly suitable for the fully-depleted SOI and/or SDG applications.

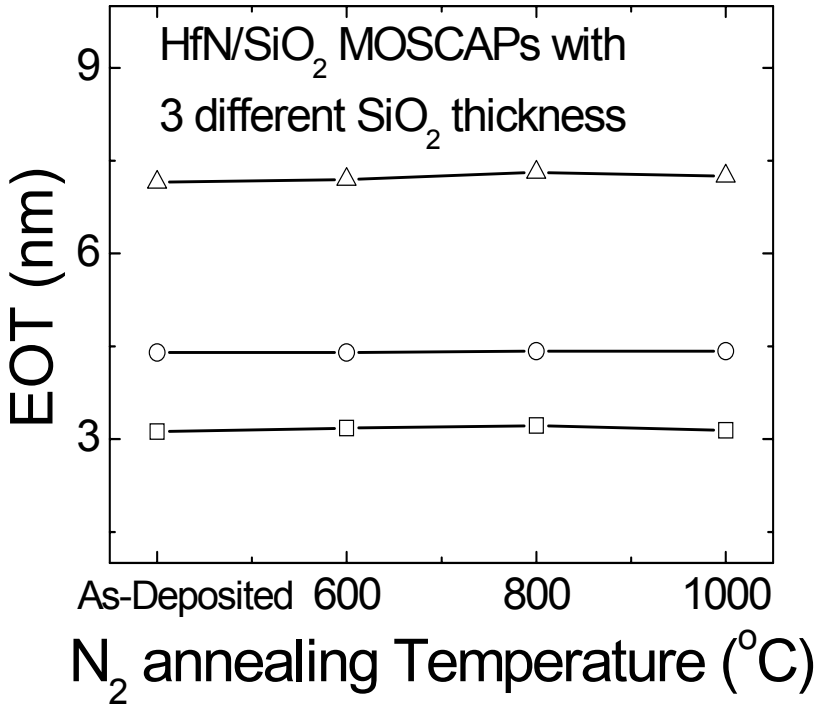


Fig. 3.10. Dependence of EOT for HfN/SiO_2 MOSCAPs on the N_2 RTA temperature.

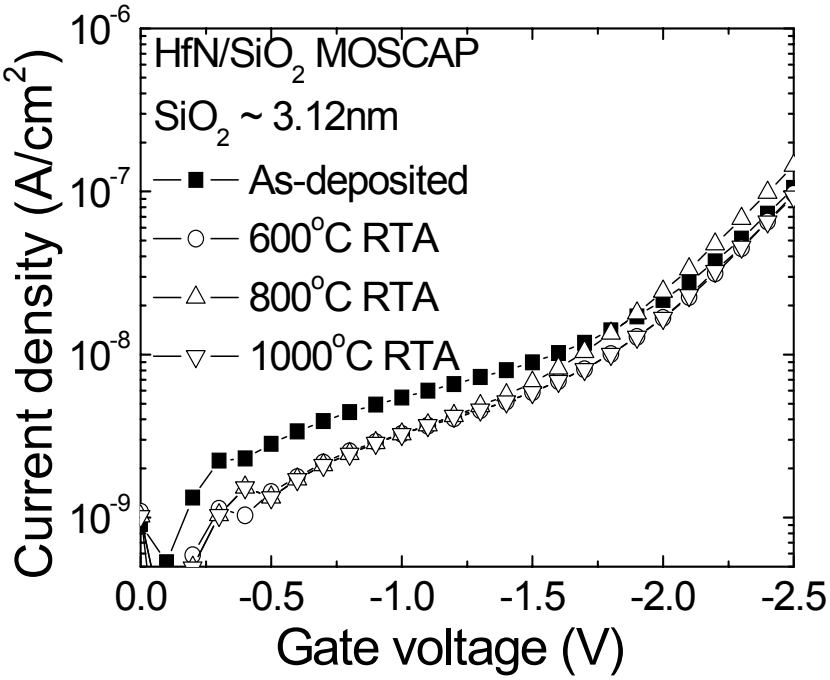


Fig. 3.11. Measured gate leakage comparison from the HfN/SiO_2 MOSCAPs (EOT=3.12nm) after various post metal annealing (PMA).

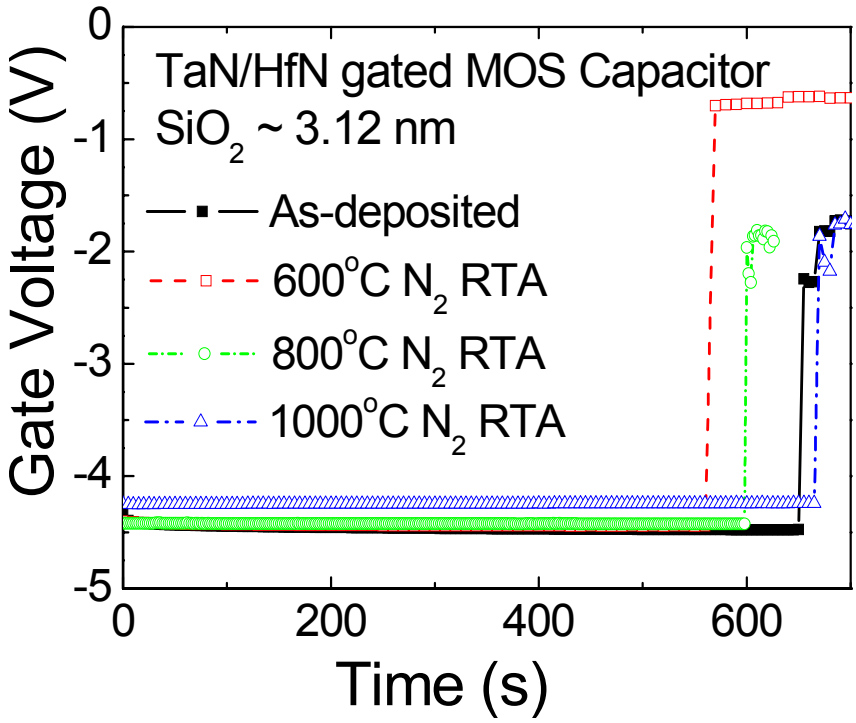


Fig. 3.12. Typical voltage-time characteristics of MOS capacitors with HfN/SiO_2 gate stack after various RTA under CCS.

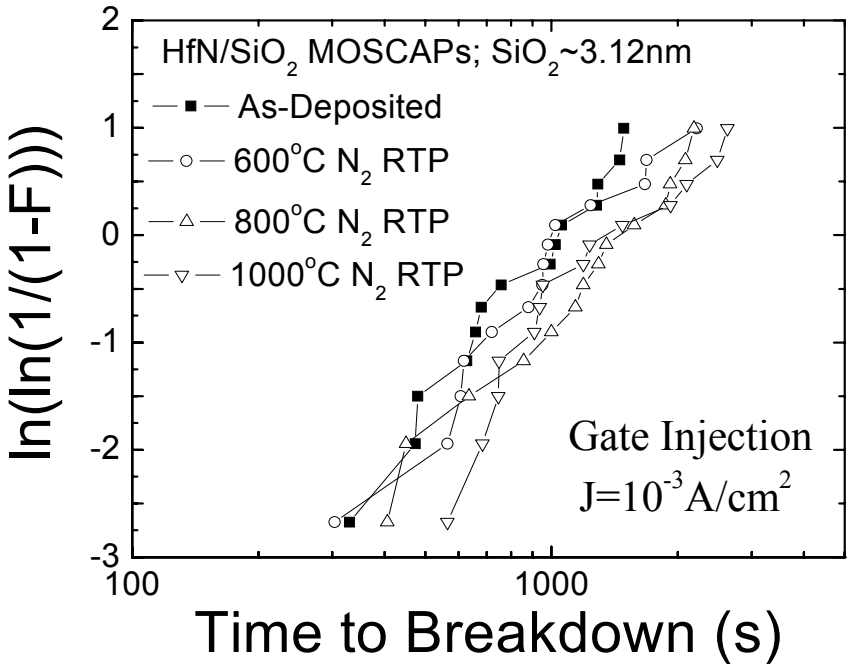


Fig. 3.13. Comparison on TDDB characteristics of HfN/SiO_2 MOSCAP (EOT=3.12nm) after various PMA.

Fig. 3.12 shows the typical voltage-time characteristics of MOS capacitors with HfN/SiO_2 gate stack after various RTA under constant current stressing (CCS). Time dependence dielectrics breakdown (TDDB) characteristics under CCS of TaN/HfN gated devices with SiO_2 ~ 3.15nm under various RTA treatments are demonstrated in Fig. 3.13. As can be seen in this figure, TDDB is improved after RTA, and time-to-breakdown slightly increases with increasing RTA temperature. This improvement is correlated to the annealing effect of plasma damages generated during sputtering deposition of the metal electrodes.

N-MOSFETs with HfN/SiO_2 gate stack (EOT ~ 4.52 nm) have also been fabricated with well-behaved I_{ds}-V_{ds} and I_{ds}-V_g characteristics and excellent subthreshold slope (SS ~ 68mV/dec), as shown in Figs. 3. 14(a) &(b).

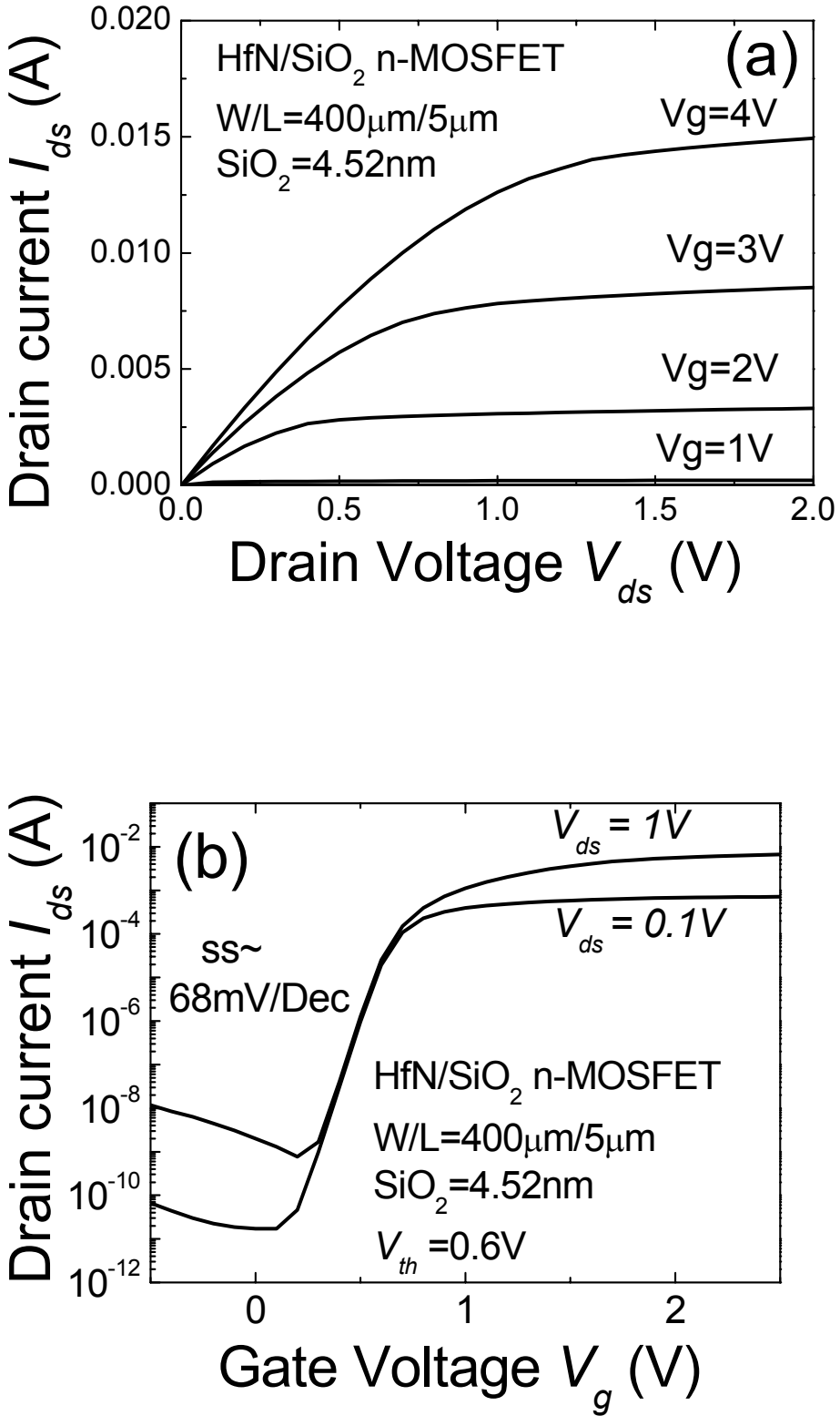


Fig. 3.14. (a) I_{ds}-V_{ds}; (b) I_{ds}-V_g characteristics of a HfN/SiO_2 n-MOSFET.

3.3.3 Electrical Characterization of HfN-HfO_2 Gate Stack

We now discuss the electrical characterization of HfN metal gate on HfO_2 gate dielectric. Recently, HfO_2 has been considered as one of the most promising high-K gate dielectrics [9]. However, HfO_2 is a poor barrier to oxygen diffusion, which caused the uncontrolled growth of low-k interfacial layer (IL) between HfO_2 and Si substrate during high-temperature post-processing [9,10]. This imposes serious concern to the EOT scalability. Although using surface nitridation or N-contained HfO_2 (i.e. HfOxNy) can minimize IL growth [11, 12], they also cause severe carrier mobility degradation. Due to the superior oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 interface, the HfN/HfO_2 gate stack demonstrates excellent EOT scalability against high temperature treatments, without using surface nitridation.

3.3.3.1 MOS Capacitors with HfN-HfO_2 Gate Stack

Fig. 3.15(a) compares measured and simulated CV curves of a HfN/HfO_2 device after various thermal annealing, showing good agreement. Without surface nitridation treatment, the EOT of the HfN/HfO_2 MOSCAP is as low as 8.2Å after forming gas annealing, and it slightly increases to 8.8Å / 9.1Å after 900^{o}C / 1000^{o}C post metal annealing (PMA). Insignificant variation of the gate leakage current is revealed in these devices after various thermal treatments, as shown in the insert of Fig. 3.15(b).

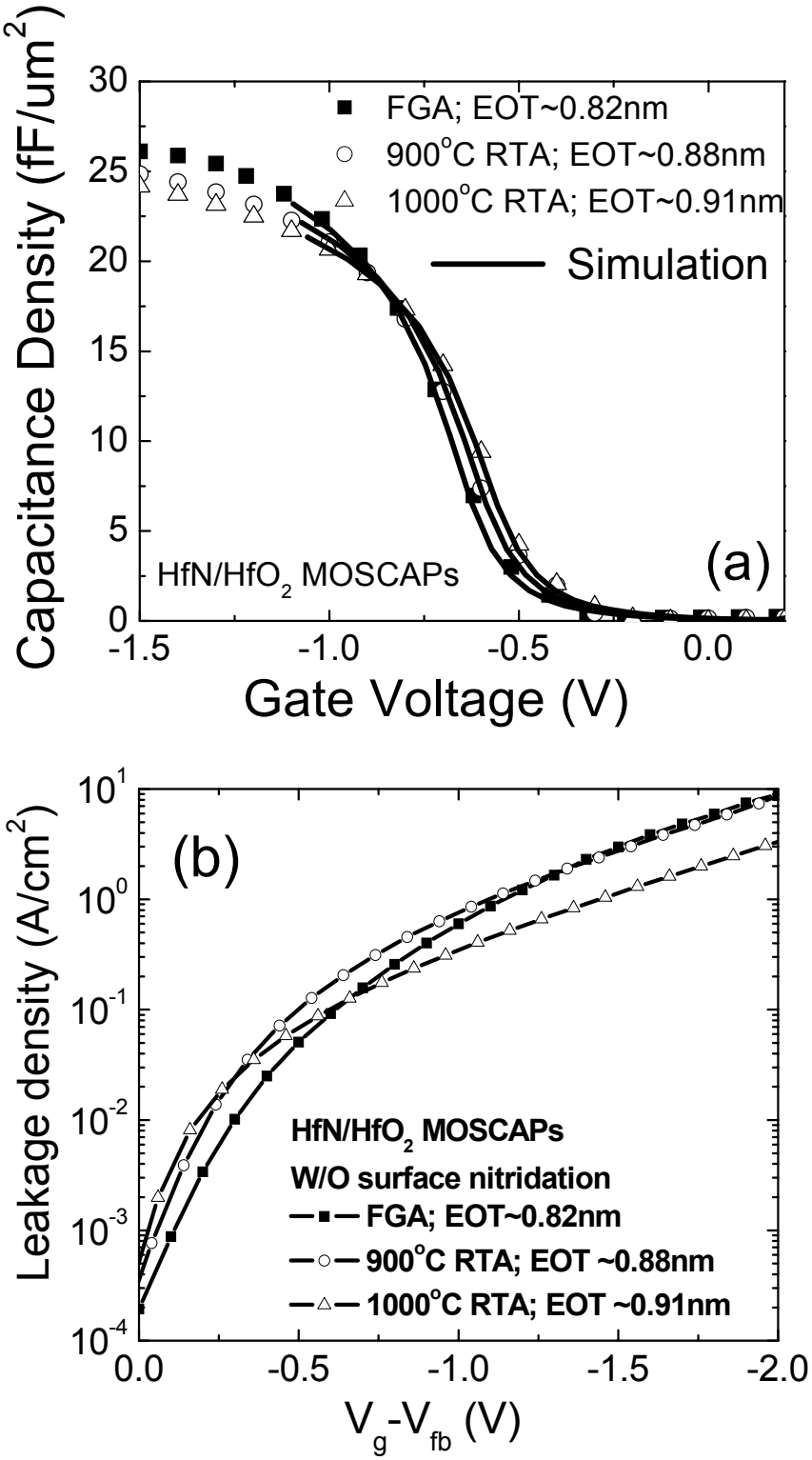


Fig. 3.15. (a) HFCV measurement (symbols) and LFCV simulation (solid lines) of HfN/HfO_2 n-MOSCAPs after different thermal treatment; (b) The corresponding leakage current measured from the HfN/HfO_2 NMOSCAPs after various thermal treatments. No surface nitridation was performed before HfO_2 deposition.

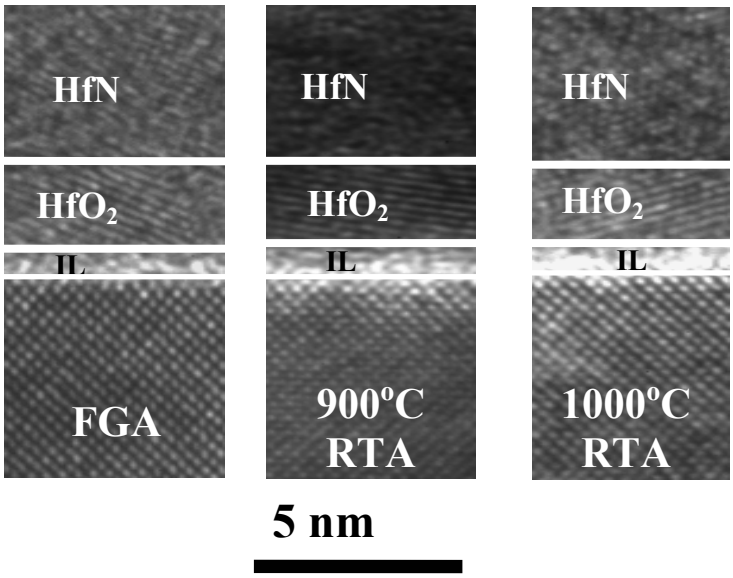


Fig. 3.16. XTEM of these HfN/HfO_2 devices with different thermal treatments (corresponding to devices shown in Fig. 3.15).

High-resolution XTEM is utilized to characterize these HfN/HfO_2 gate stacks after various PMA, as shown in Fig. 3.16. For the sample without PMA, IL is ~7Å and HfO_2 is ~22 Å. Negligible change in the physical thickness of both HfO_2 and IL is observed after 1000C annealing, consistent with results shown in Fig. 3.15(a). From the TEM and CV data and with the assumption that the K value of HfO_2 is 22~23, it appears that IL is has a K value of 7-8 and is not pure SiO_2 [10].

Fig. 3.17 shows the measured high-frequency C-V and I-V curves of HfN/HfO_2 gate stack with surface nitridation under different thermal treatments (FGA, 900°C, and 1000°C RTA). The well-behaved C-V characteristics with excellent agreement with simulated CV curves, as well as low gate leakage current densities are observed. The FGA sample shows EOT of 0.65nm with gate leakage of $0.3A/cm^2$ @ V_{FB}–1V. High temperature PMA (1000°C) increases EOT slightly by 0.1 nm along

with some reduction of gate leakage. The aggressively scaled EOT of HfO_2 dielectrics is attributed to both the NH_3-based surface nitridation prior to HfO_2 deposition (suppress interfacial oxidation at the HfO_2/Si interface) and the HfN gate electrode (an excellent oxygen diffusion barrier).

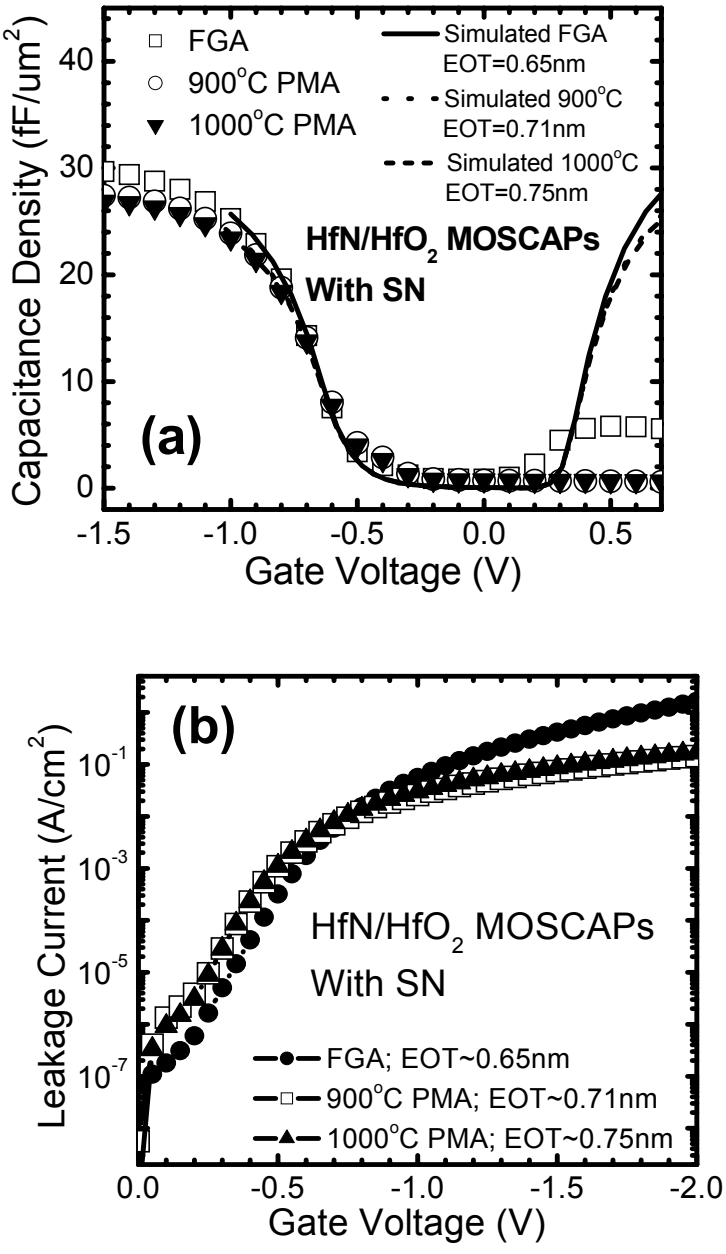


Fig. 3.17. (a) Measured CV (symbols) and simulated CV (lines) HfN/HfO_2 MOSCAP with surface nitridation after various thermal treatments; (b) The inset shows leakage comparison measured from these HfN/HfO_2 MOSCAP after various PMA.

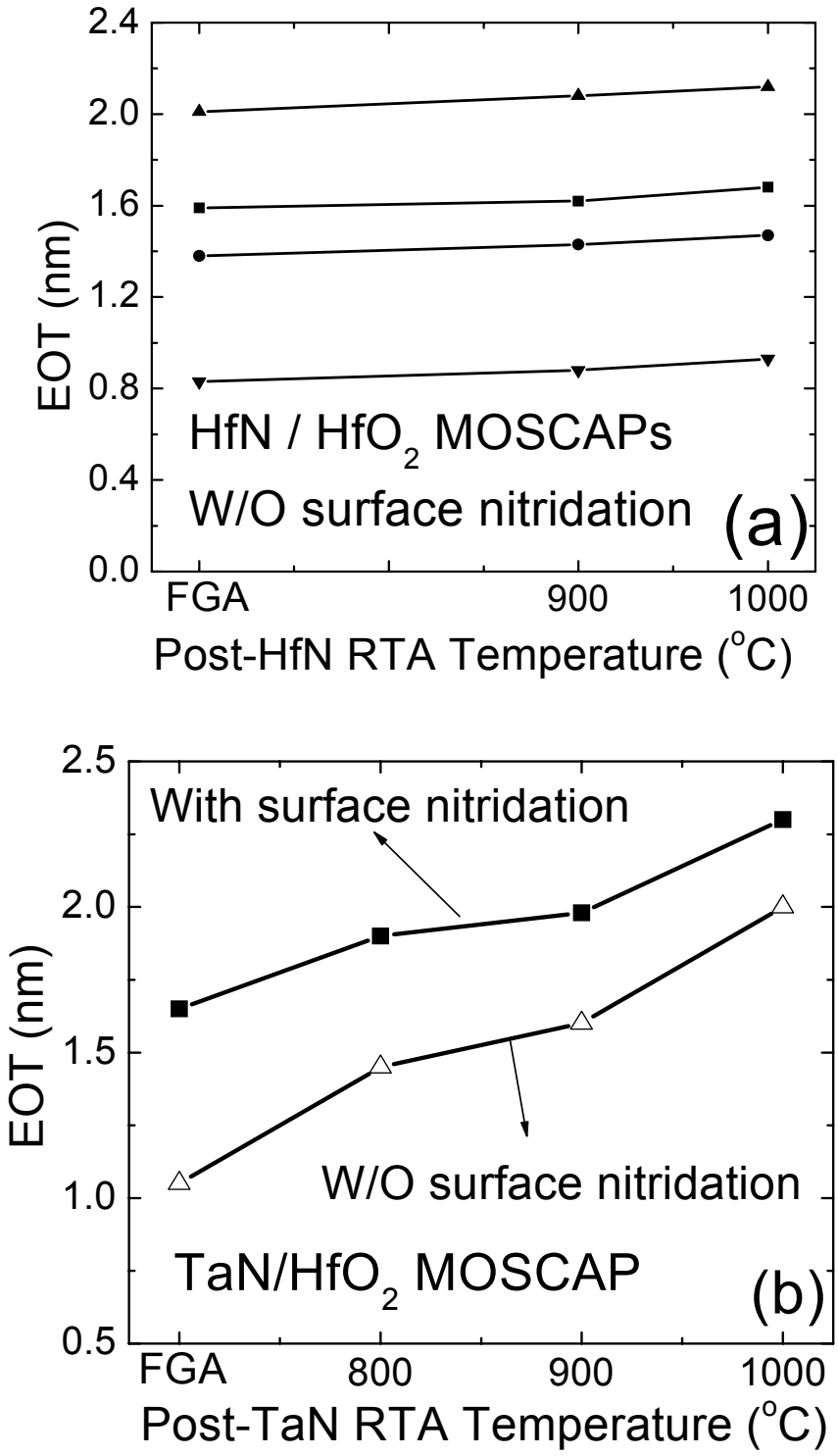


Fig. 3.18. Dependence of EOT for (a) HfN/HfO_2 MOSCAPs (b) TaN/HfO_2 MOSCAPs on the N_2 RTA temperature.

The superior thermal stability of HfN/HfO_2 gate stack is further demonstrated in Fig. 3.18(a), where four devices with different EOT are plotted as a function of PMA temperatures. The results show that the EOT variations in all HfN/HfO_2 devices are negligible up to 1000°C PMA. The electrical stability between TaN/HfO_2 and HfN/HfO_2 gate stacks is also compared. PVD TaN has been extensively studied as a promising metal gate candidate [e.g. ref. 12]. EOT of TaN/HfO_2 gate stack vs. PMA temperature is shown in Fig. 3.18(b). The EOT of TaN/HfO_2 shows significant increases upon 800-1000°C PMA. The poor thermal stability of PVD TaN compared to HfN might be attributed to its negatively smaller heat of formation [5] and its inferior ability to block oxygen diffusion. Fig. 3.19 depicts gate leakage at V_{fb}-1V as a function of EOT for HfN/HfO_2 without SN. Compared to poly/SiO_2 benchmark [13], HfN/HfO_2 shows more than a factor of 10^5 reduction in gate leakage with the same EOT.

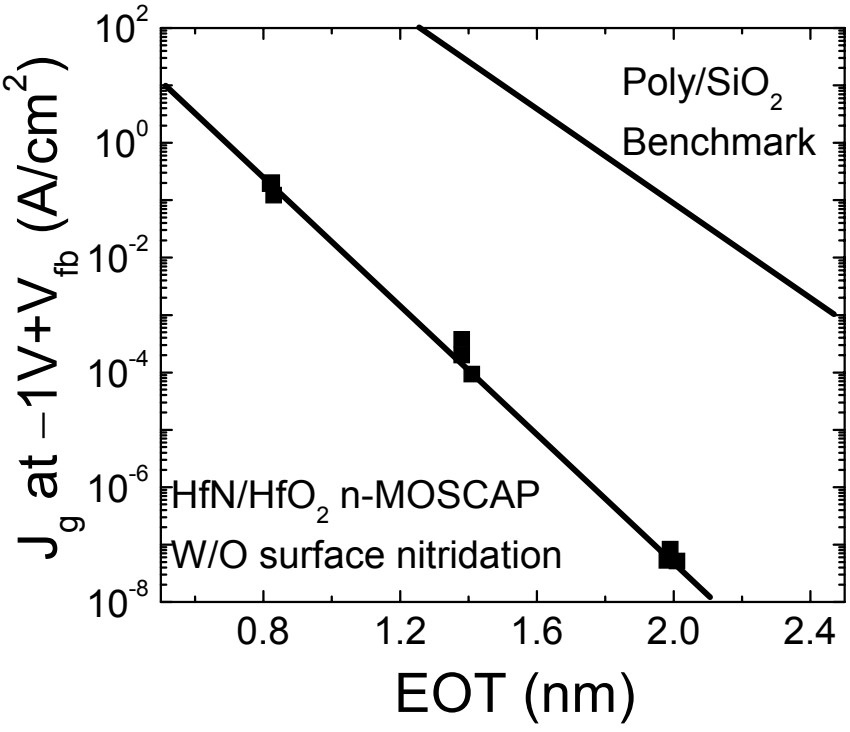


Fig. 3.19. Leakage vs. EOT relationship for MOSCAP devices with HfN/HfO_2 gate stack.

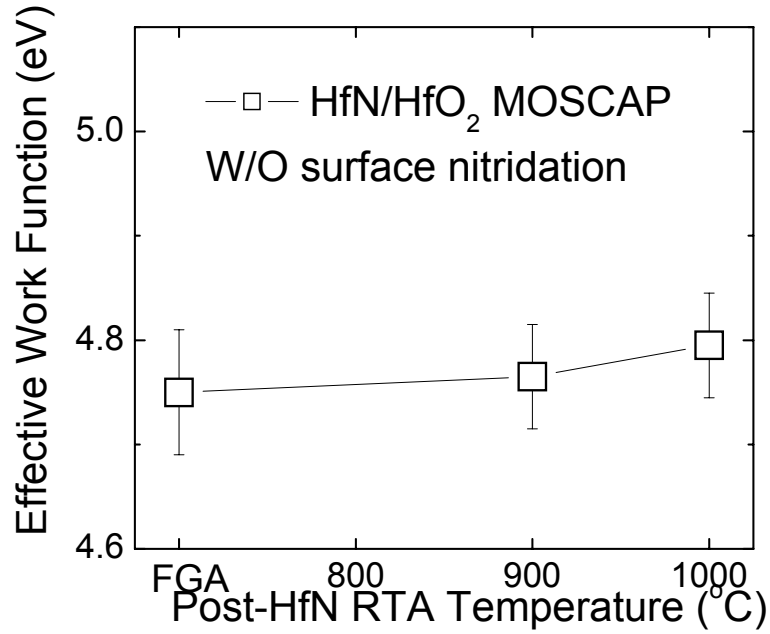


Fig. 3.20. Work function of HfN metal gate on HfO_2 dielectrics after various thermal treatments.

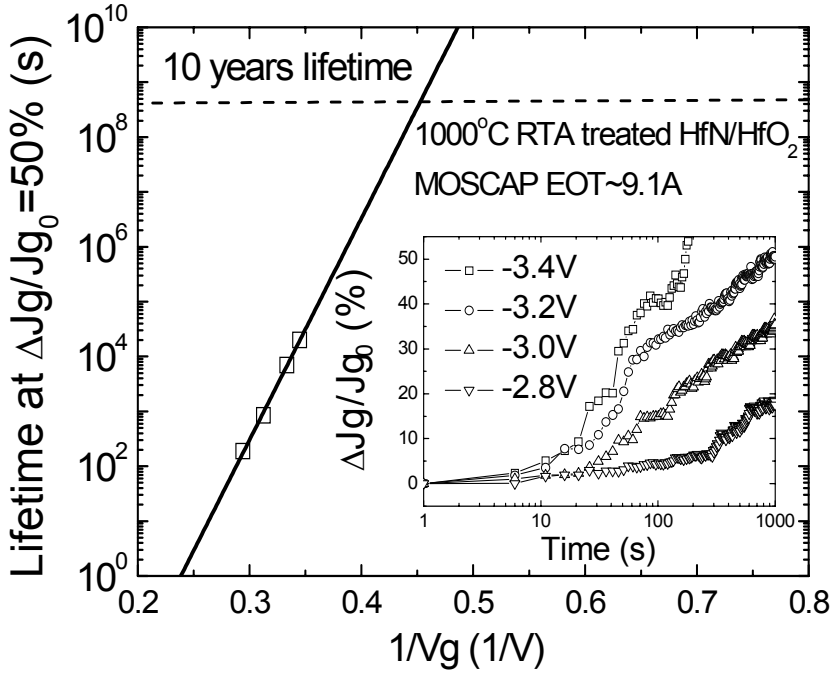


Fig. 3.21. Lifetime projection based on SILC for the HfN/HfO_2 MOSCAP (W/O SN) after 1000°C RTA with EOT=9.1Å. Inset shows typical SILC time evolutions at four gate voltages. Failure criterion is set at 50% increment of J_{g0}.

In Fig. 3.20, the work function of HfN on HfO_2, extracted from plots of V_{fb} versus EOT, is shown as a function of PMA temperature. Very little dependence of Φ_M of HfN on the underlying HfO_2 gate dielectrics after various thermal treatments is observed. As compared to figure 3.9, HfN Φ_M shows dependence on the underlying dielectrics, i.e. HfO_2 or SiO_2. The small difference is suggested to be due to the different interface dipole formation between HfN/SiO_2 or HfN/HfO_2 interface [14].

Stress-induced leakage current (SILC) characteristics of the 1000^{o}C RTA treated HfN/HfO_2 n-MOSCAP device (EOT = 9.1Å) are shown in Fig. 3.21. For the HfO_2 MOS capacitors with EOT = 9.1Å, it is hard to observe both hard breakdown and soft breakdown under typical stress conditions. While, it is observed that the continuous gate leakage increase with stress, and this leakage could eventually become unacceptable for normal device operation [15]. And hence the HfO_2 gate dielectrics lifetime is projected based on SILC. Inset of figure 3.21 shows typical the SILC time evolutions for the HfN/HfO_2 device at four gate voltages. Using *delta* J_g/J_{g0}=50% as failure criterion, the operating voltage for 10-year lifetime is projected as 2.2V.

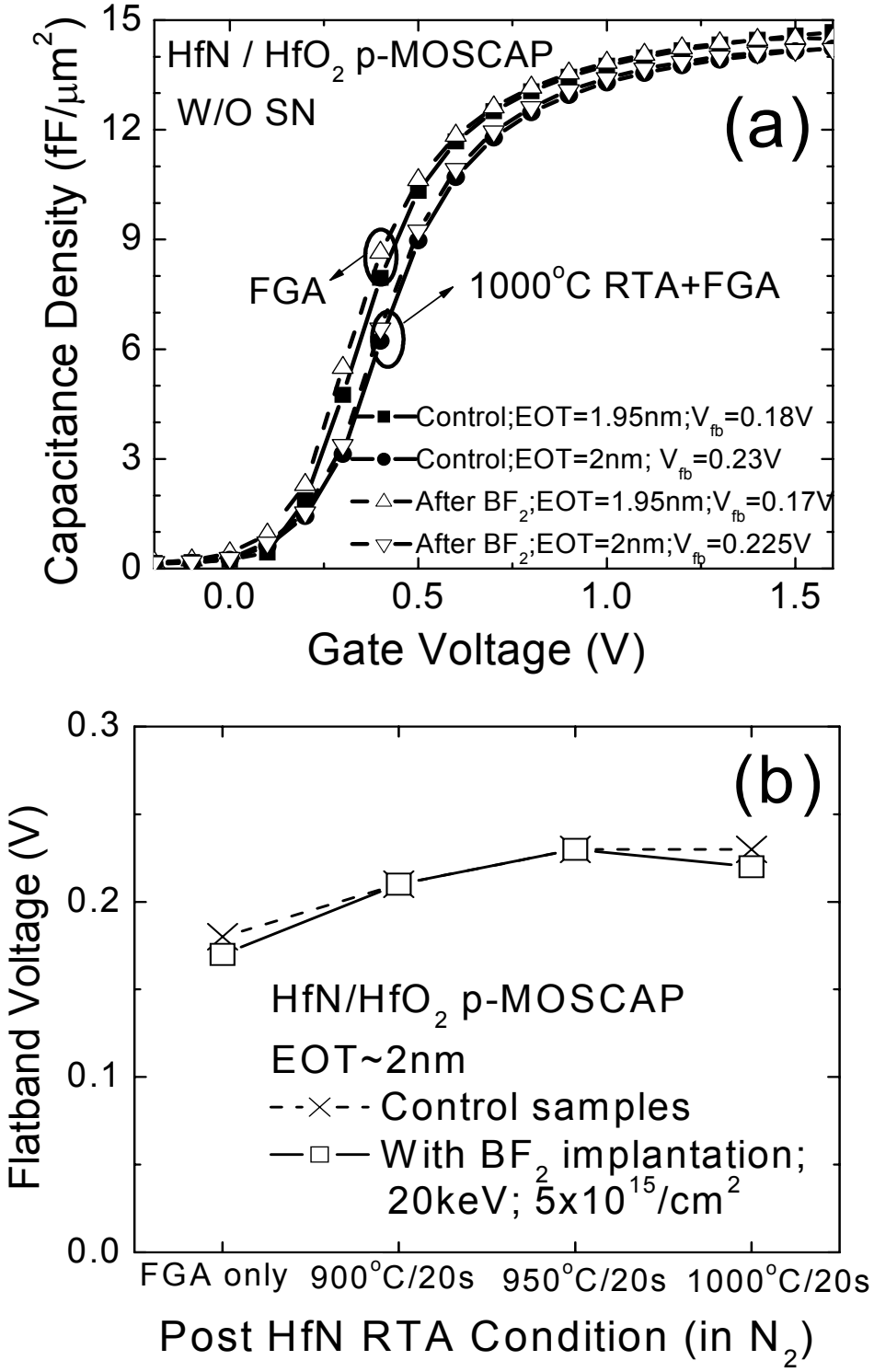


Fig. 3.22. (a) Boron implantation effect on CV characteristics of HfN/HfO_2 pMOSCAP. Solid symbols: control samples; empty symbols: BF_2 implanted samples. Measured CV after FGA and 1000°C RTA dopant activation are shown for both kinds of samples. (b) The comparison of the V_{fb} variation after different RTA between control samples and the BF_2 implanted samples.

The boron penetration effect in HfN/HfO_2 p-MOSCAPs (fabricated using n-Si substrates) with BF_2 implantation (dose of $5x10^{15}cm^{-2}$; implantation energy of 20 KeV) was also investigated and results are shown in Figs. 3.22(a)&(b). There is no difference in V_{fb} between the un-implanted (control devices) and BF_2-implanted devices after RTA at 900°C, 950°C, and 1000°C for 20s in N_2, indicating excellent boron penetration immunity of HfN/HO_2 gate stack.

The use of surface nitridation prior to HfO_2 deposition results in larger CV hysteresis, as shown in Fig. 3.23, which is explained by the higher trapped charge density induced by NH_3 annealing treatments [16]. Note that the high temperature PMA process can effectively reduce the hysteresis caused by the SN treatments.

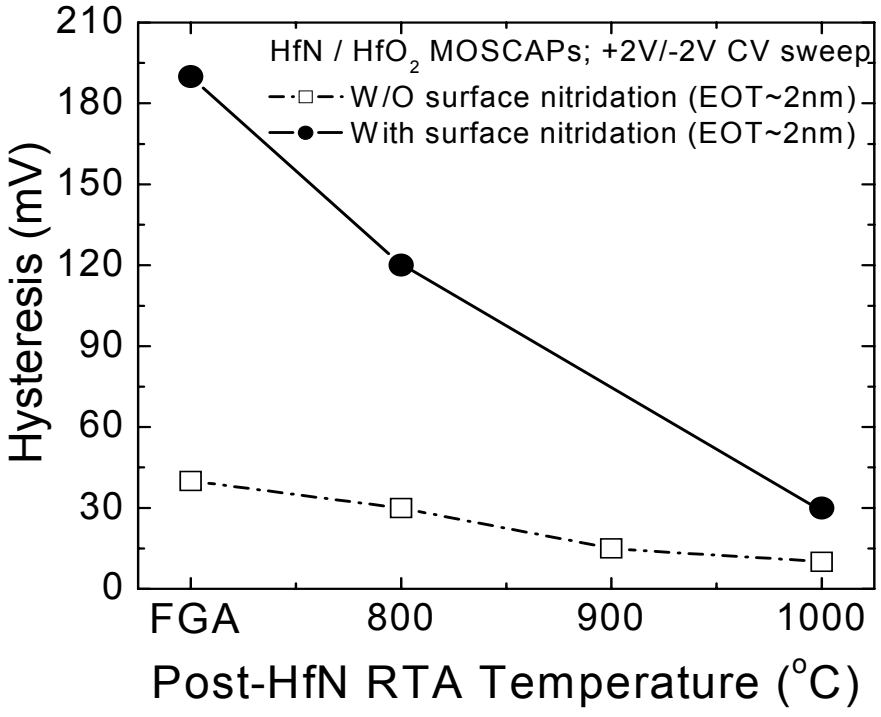


Fig. 3.23. Hysteresis vs. post-HfN RTA temperature for HfN/HfO_2 devices with and without surface nitridation prior to HfO_2 deposition.

3.3.3.2 MOSFETs with HfN-HfO_2 Gate Stack

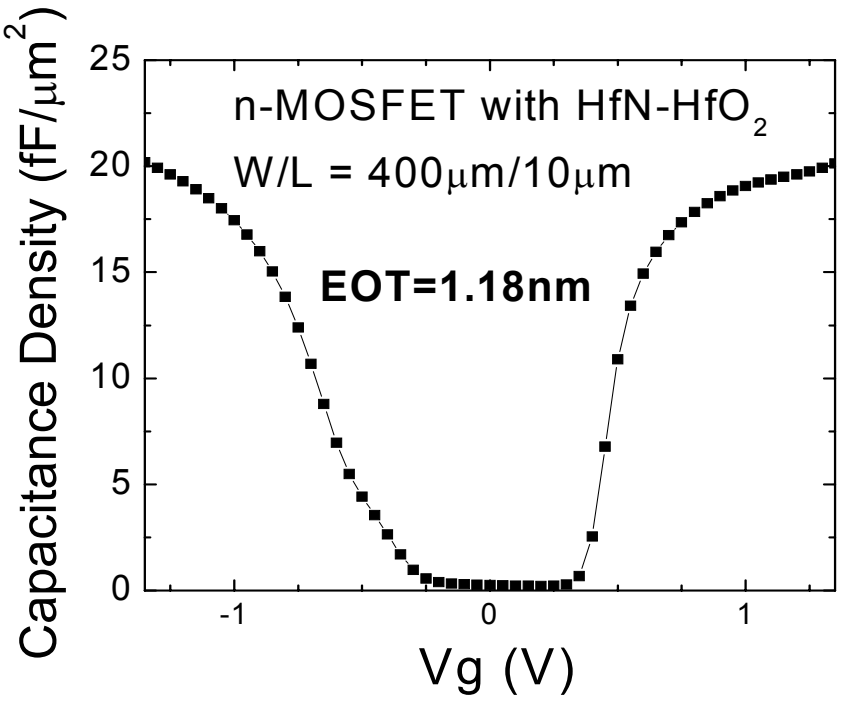


Fig. 3.24. HFCV characteristics of the n-MOSFET with HfN/HfO_2 gate stack; EOT of 1.18nm is obtained considering the quantum mechanical effect. No surface nitridation was performed before CVD HfO_2 deposition.

HFCV characteristic of the n-MOSFET with HfN/HfO_2 gate stack is shown in Fig. 3.24. No surface nitridation was performed before CVD HfO_2 deposition. EOT of 1.18nm is obtained considering the quantum mechanical effect. The poly-depletion effect is eliminated as expected. Figs. 3.25 (a) &(b) show the typical electrical characteristics (I_{ds}-V_{ds} & I_{ds}-V_g) of the HfN/HfO_2 n-MOSFET with a subthreshold slope (*SS*) of 78mV/dec.

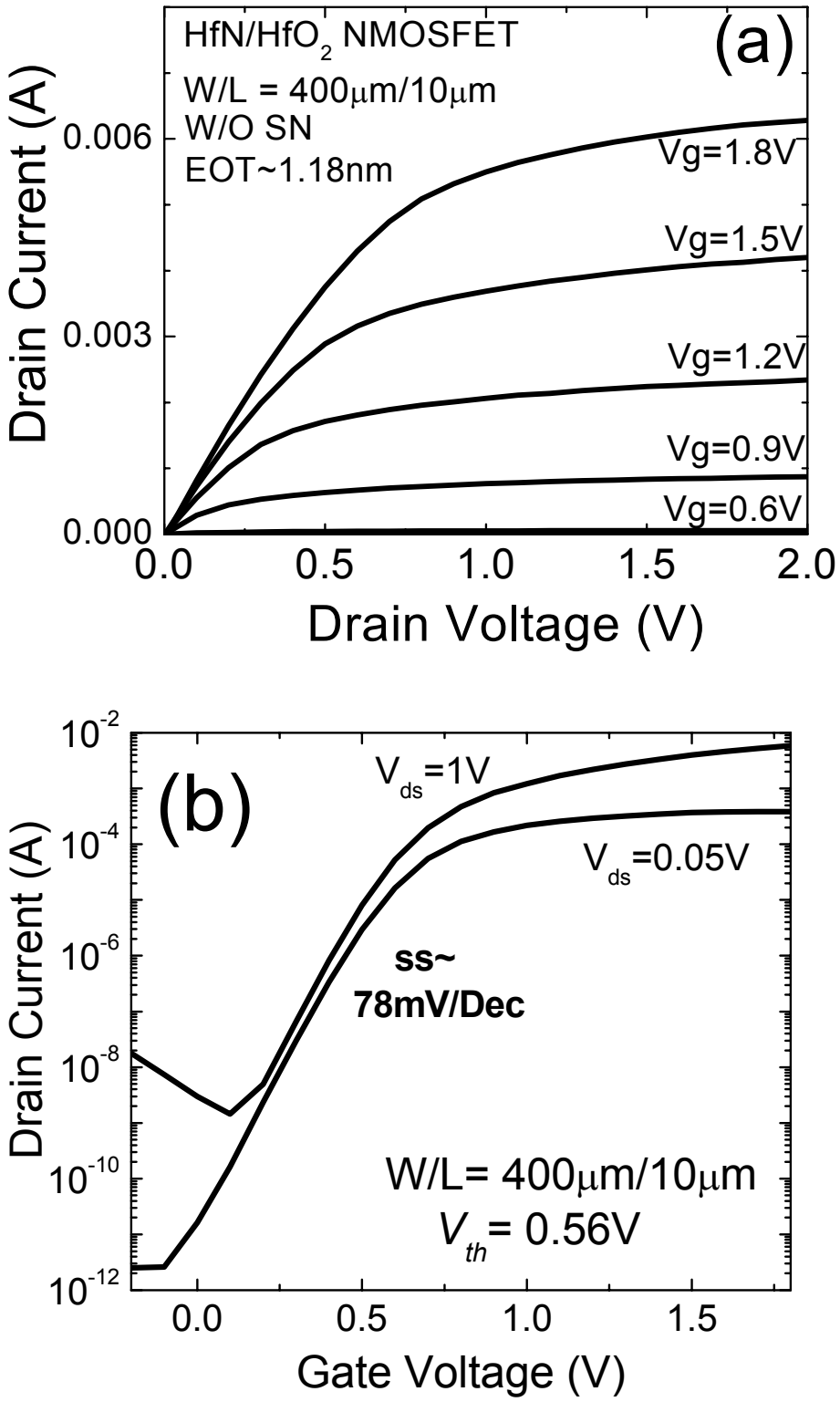


Fig. 3.25. (a) I_{ds}-V_{ds} (b) I_{ds}-V_g characteristics of HfN/HfO_2 n-MOSFETs without using SN and with EOT=1.18nm.

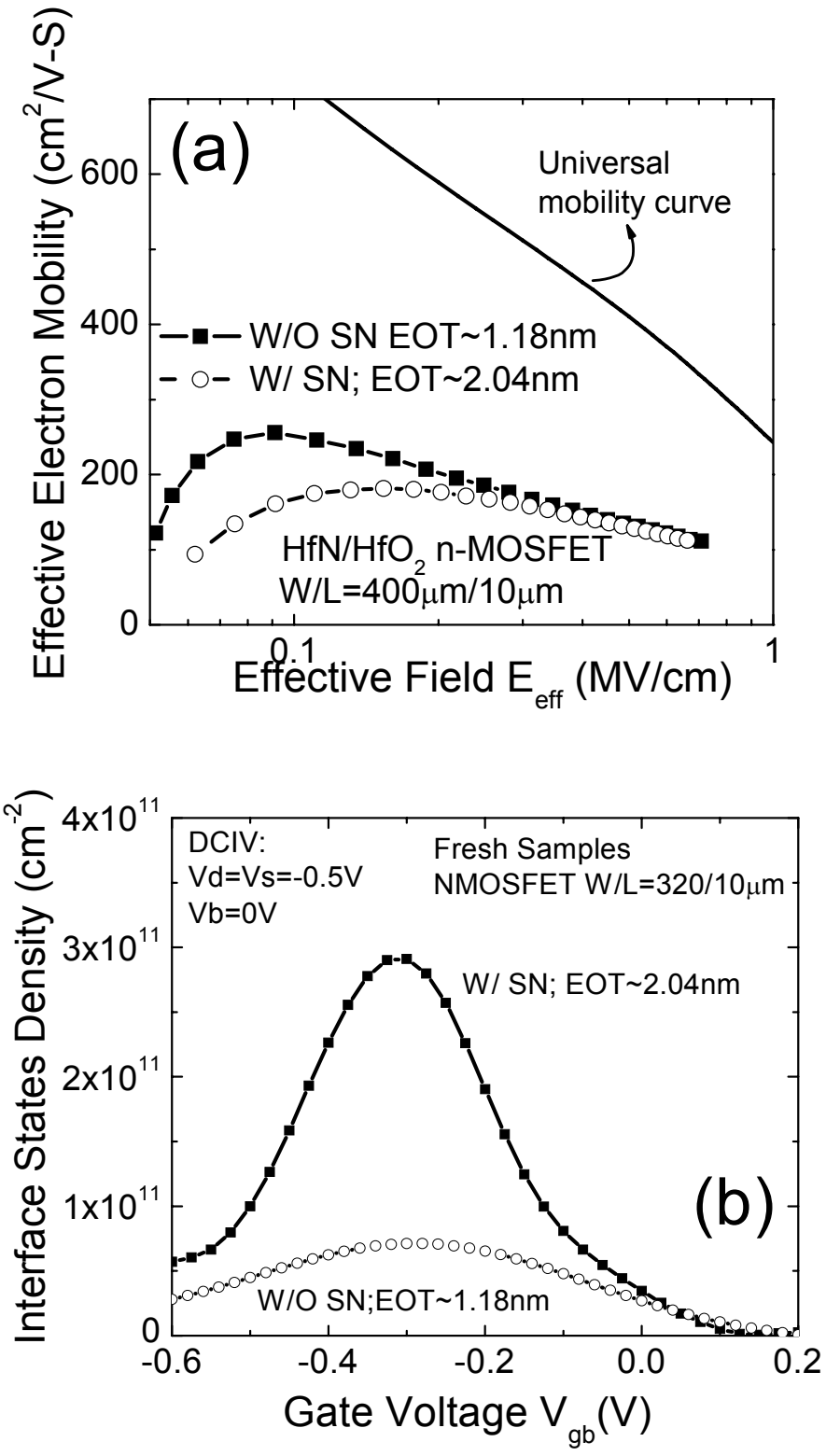


Fig. 3.26. (a) The effect of SN treatment on effective electron mobility for HfN/HfO_2 n-MOSFETs; (b) DCIV measurement show that interface trap density D_{it} is ~$3x10^{11}/cm^2$ for fresh nMOSFETs after SN treatment (EOT~2.04nm), and D_{it} ~$7x10^{10}/cm^2$ for fresh device W/O SN with EOT~1.18nm.

Effective electron mobility (μ_e) between devices with and without surface nitridation is compared in Fig. 3.26(a), where the μ_e is measured by the split CV method [17]. The universal mobility curve [17] is shown in this figure. It is seen that under low effective field, the electron mobility is degraded in the surface nitridation device despite its larger EOT, which is attributed to the larger interface trap density (D_{it}) due to nitrogen incorporation at the HfO_2/Si, as shown in Fig. 3.26(b) where D_{it} is measured by the direct-current current-voltage (DCIV) technique [18], using interface trap capture cross section of 4.4 $Å^2$ [19]. However, compared to the universal mobility curve, we observe the significant mobility degradation for both devices, which is attributed to the fixed charge induced remote coulomb scattering [20] or the remote phonon scattering [21] from the bulk HfO_2 gate dielectrics.

Figs. 3.27 (a) & (b) show well-behaved I_{ds}-V_{ds}, and I_{ds}-V_g characteristics of p-MOSFETs with HfN/HfO2 gate stack without SN (EOT=1.28nm) with an excellent subthreshold slope (*SS*) of 68mV/dec.

Effective hole mobility (μ_h) for the p-MOSFETs measured by the split CV method is shown in Fig. 3.28.

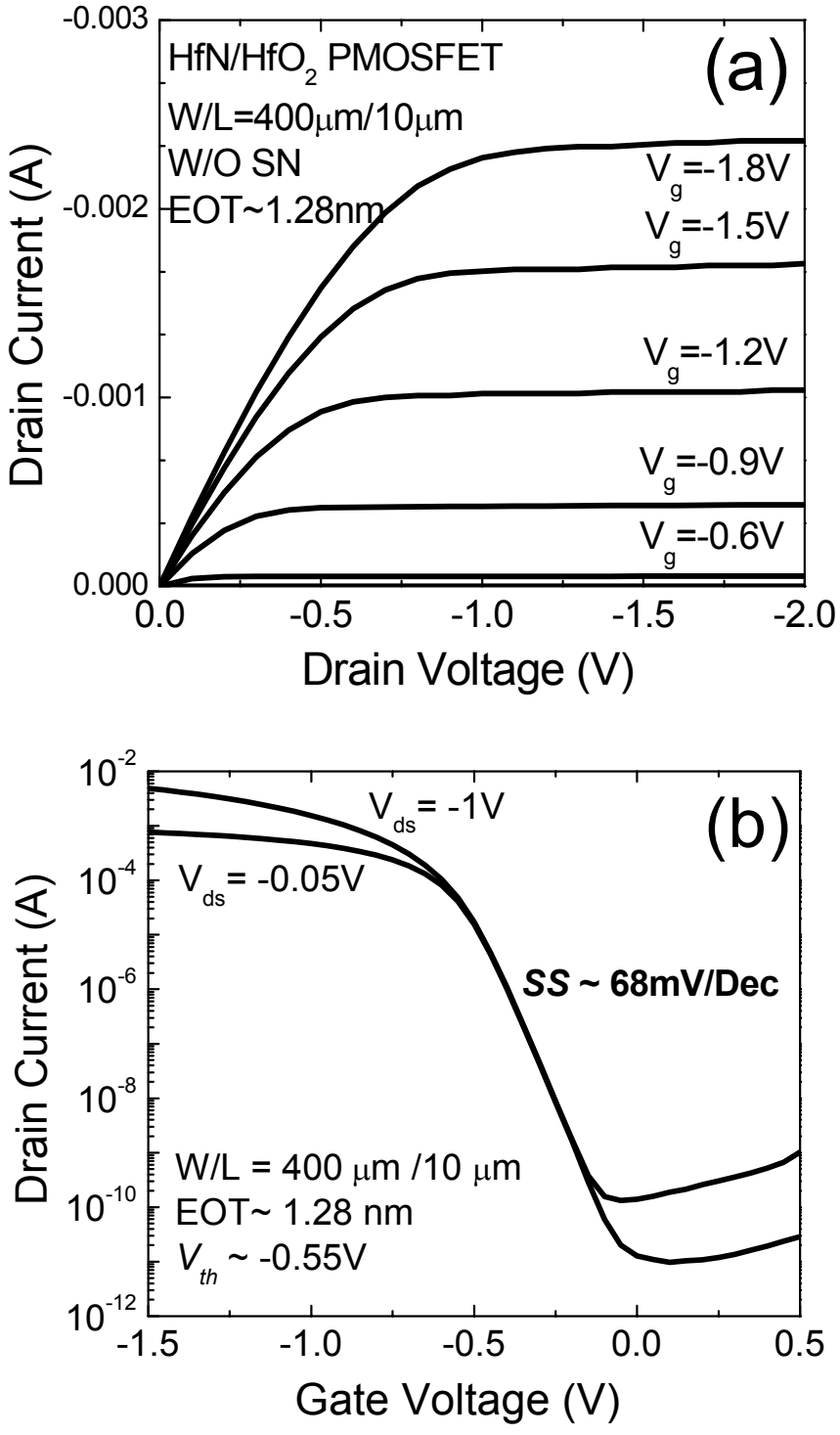


Fig. 3.27. (a) I_{ds}-V_{ds} and (b) I_{ds}-V_g characteristics of HfN/HfO_2 p-MOSFETs without using SN and with EOT=1.28nm.

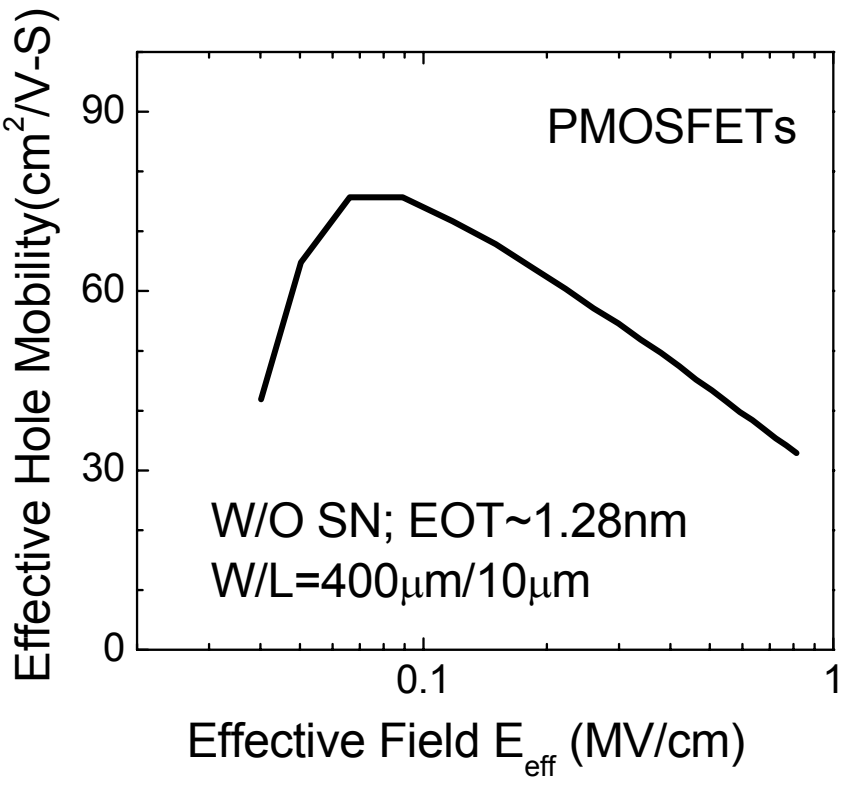


Fig. 3.28. Effective hole mobility measured by split CV for the p-MOSFETs shown in Fig. 3.27.

Negative bias temperature instability (NBTI) for the HfN/HfO_2 p-MOSFETs (without using SN and with EOT=1.28nm) was also studied at 100 °C. Fig. 3.29(a) demonstrates the V_{th} variation as a function of stress time during NBTI under three different negative gate biases. It is interesting to note that the V_{th} shift follows a power law dependence on the stress time. Lifetime projection based on NBTI is performed. Using 50 mV shift of V_{th} as the device failure criterion [22], the p-MOSFETs can satisfy the 10-year lifetime at an operating voltage of ~ 1 V, as shown in Fig. 3.29(b).

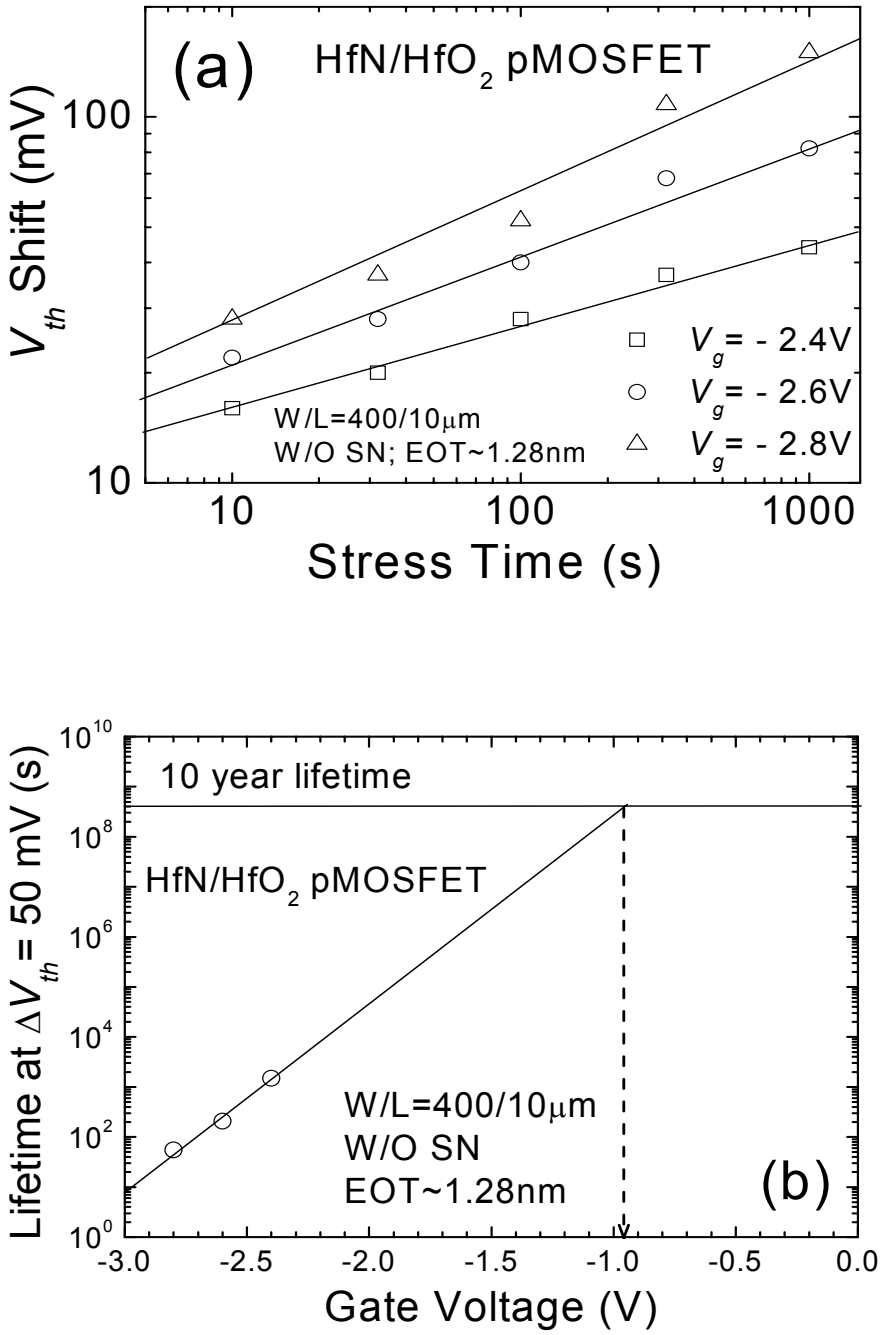


Fig. 3.29. (a) For HfN/HfO_2 p-MOSFETs without using SN & with EOT=1.28nm, the V_{th} variation as a function of stress time during NBTI under three different negative gate biases at 100°C. (b) Lifetime projection based on NBTI. Failure criterion is set as ΔVth=50mV. The devices can satisfy the 10-year lifetime at an operation voltage of ~1V.

3.4 Conclusion

In conclusion, for the first time, a systematic study on HfN metal gate electrode for advanced CMOS devices applications is presented. For both SiO_2 and HfO_2 gate dielectrics, HfN metal possesses a mid-gap work function, and shows robust resistance against high temperature RTA treatments (up to 1000°C), in terms of EOT, work function, and leakage current stability. This superior electrical stability is attributed to the excellent oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 and HfN/SiO_2 interface. Further, the high quality HfN/HfO_2 gate stack's EOT has been successfully scaled down to less than 10Å with excellent leakage, boron penetration immunity, and long-term reliability even after 1000^{o}C annealing, without using surface nitridation prior to HfO_2 deposition. The mobility is improved without surface nitridation for HfN/HfO_2 n-MOSFETs while achieving excellent EOT. HfN is proposed as an ideal gate electrode candidate for the FD-SOI and/or the symmetric double-gate (SDG) MOS devices applications where a mid-gap metal gate electrode is desired.

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Chapter 4

Fermi Pinning Induced Thermal Instability of Metal Gate Work Functions

4.1 Introduction

Metal gate electrodes not only eliminate the gate depletion and dopant penetration problems in CMOS transistors, but also reduce the gate sheet resistance. In selecting metal gate materials for device integration, the metal work function (Φ_m) is an important consideration since it directly affects the threshold voltage and the performance of a transistor. Integrating metal gate electrodes in a CMOS process is a challenging task because metal gate work functions are observed to be dependent on the underlying gate dielectric [1,2] and on the fabrication process conditions [3-8]. The dependence of Φ_m on the gate dielectric material was explained by Yeo *et al.* [1,2] to be due to dipole formation at the interface of the gate electrode and the gate dielectric. This model has been particularly successful for metal-dielectric interfaces where there is minimal interfacial reaction [1-2], or where *intrinsic states* or metal-induced gap states (MIGS) dominate. However, integrating metal gates in a gate-first or conventional approach is very attractive for introducing metal gates in a manufacturable process, and this typically requires the gate-stack to undergo high

temperature Source/Drain annealing process. Therefore, the metal/dielectric interface interaction and the dependence of Φ_m on the annealing temperature are critically important and must be clearly understood.

In this chapter, the experimental results on the dependence of the metal gate work function Φ_m on the underlying gate dielectric materials and the process temperature will be presented, and a model to explain the phenomenon of process-induced Φ_m thermal instability is to be proposed. It is shown that high temperature annealing could lead to the creation of *extrinsic states*, and hence the interface dipole, at the metal-dielectric, resulting in metal Fermi level pinning.

4.2 Theoretical Background of Metal-Semiconductor (or Metal-Dielectrics) Interface

4.2.1 The Work Function of a Solid

The work function Φ of a solid (either a metal or a semiconductor) is defined as the energy difference between the Fermi level in the solid and the vacuum level. For a semiconductor, the work function is a statistical concept and stands for the weighted average of the amount of energy required to raise an electron from the valence band and the conduction band to the vacuum level, respectively [9].

There are two parts for the work function calculation using quantum mechanics effect [9]: (1) A volume contribution which stems from the energy of an electron due to the periodic potential of the crystal and interaction of the electron with other electrons; (2) A surface contribution which is due to a possible surface dipole. As the electron charge distribution around the atoms at the solid surface is not symmetrically disposed around the nucleus, the center of the positive and the negative charge will not coincide, leading to a surface dipole. Therefore, any change in the surface electron charge distribution of a solid will result in the modification of the surface dipole layer, and hence the solid work function.

4.2.2 Schottky Model and Bardeen Model

Schottky Model describes an ideal metal-semiconductor (or dielectric) contact [10]. There is no charge transfer across the metal-semiconductor (or dielectric) interface, and the Schottky Barrier Height (SBH, ϕ_b) for electron is determined only by metal work function in vacuum $\Phi_{m,vac}$ and the electron affinity of the semiconductor χ_s. Therefore there is,

$$\phi_b = \Phi_{m,Vac} - \chi_s \qquad (4\text{-}1)$$

However, it was experimentally observed that *eq. (4-1)* is not generally obeyed. Bardeen proposed a Surface State model to explain this observation [10]. Bardeen's model assumes that there exist a high density of surface states at the semiconductor surface, and these states pin the metal Fermi level to a certain energy

level relative to the conduction edge of the semiconductor. However, later it was further pointed out by Heine [11] that the high density of surface states didn't exist in the fundamental gap for most metal-semiconductor interfaces, while the metal Fermi level pinning phenomena were still observed.

4.2.3 Interface Dipole Induced by Metal Induced Gap States (MIGS)

Heine was the first to point out that the tails of the conduction electron wave functions in the metal tunnel into the band gap of the semiconductor at the metal – semiconductor interface, and the resulting states in the forbidden gap are known as metal-induced gap states (MIGS), or intrinsic states [11]. As a result, any intrinsic electron states associated with a free semiconductor surface will be replaced by MIGS when a metal is deposited onto that surface. Recently, MIGS have been observed experimentally by Muller et al. using electro energy loss spectroscopy [12].

Any state in the band gap is necessarily a mixture of valence band (*Ev*) and conduction band (*Ec*) character [13]. If the state is close to *Ec*, the conduction-band character weight more than valence-band character. Filling this state gives a large excess negative charge, and it is said that the state lies nearby *Ec* has "acceptor-like" character. Vice versa, the state close to *Ev* is called as a "donor-like" state.

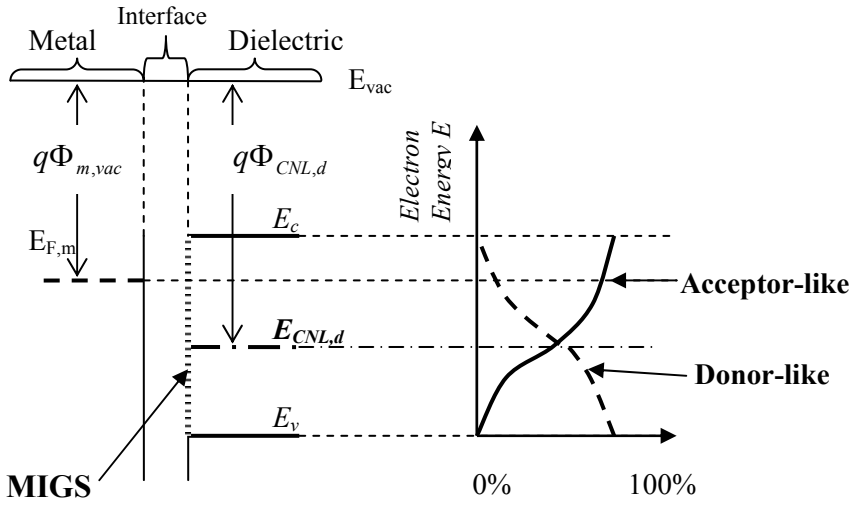

Fig. 4.1. Schematic energy band diagram (left) and the characteristics of the gap states (right) for metal gate on dielectrics. The character of MIGS becomes more acceptor- (donor-) like toward the Ec (Ev), as indicated by the solid (dashed) line [2].

The distribution of MIGS in the dielectrics band gap is shown in Fig. 4.1. The energy level at which the dominant character of the interface states changes from acceptor-like to donor-like is defined as the Charge Neutrality Level (E_{CNL}) [13]. In other words, above (below) the E_{CNL}, the state becomes more acceptor-like (donor-like). Note that E_{CNL} is the balanced point of the weights of the conduction-band and valence-band Density of States. A high density states near the valence (conduction) band edge tends to drive the E_{CNL} towards the conduction (valence) band edge.

The existing of MIGS would result in the charge transfer across the interface. Fig. 4.1 depicts the case where the Fermi level of metal ($E_{F,m}$) is above the dielectrics E_{CNL}. Electrons from the metal tend to transfer across the interface to fill the MIGS where the energy is below $E_{F,m}$. Consequently, negative charges are generated in the

intrinsic interface states on the dielectrics side, and a dipole is formed at the interface. $E_{F,m}$ would be driven towards the E_{CNL} by this interface dipole, and hence the effective metal work function $\Phi_{m,eff}$ would differ from its value in vacuum $\Phi_{m,vac}$. The relationship between $\Phi_{m,eff}$ and $\Phi_{m,vac}$ is given by the following equation [2]:

$$\Phi_{m,eff} = \Phi_{CNL,d} + S(\Phi_{m,vac} - \Phi_{CNL,d}) \quad (4\text{-}2)$$

where S is the Schottky pinning parameter [14], describing the dielectric screening. S empirically obeys the following equation [15]:

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2} \quad (4\text{-}3)$$

where ε_∞ stands for the electronic part of the dielectric constant. The smaller value of S parameter for a material, the more effectively for this material pins the metal Fermi level. When S equal to zero, $E_{F,m}$ would be fully pinned to the E_{CNL}, and this is the "Bardeen limit". When S becomes unity, there is no pinning of $E_{F,m}$, and this is called the "Schottky limit".

4.3 Experimental

The metal-oxide-semiconductor capacitors were fabricated using p-Si(100) substrates (B, $6x10^{15}/cm^{-3}$). After the definition of the active area with 4000Å field oxide, and a standard DHF-last RCA pre-gate clean process, either thermally grown SiO_2 or MOCVD HfO_2 with different thicknesses was grown [16]. Capacitors with

HfN, TaN, TaTi, and TaTiN metal gates were fabricated. The various metal gate electrodes were deposited by DC sputtering. HfN was used as the capping layer on TaN, TaTi, and TaTiN gate electrodes to minimize oxygen diffusion through the gate stack during high-temperature post process, and hence eliminate variation of the EOT of the gate dielectric induced by oxygen diffusion [8,16]. To study the thermal stability of Φ_m, the capacitors were annealed in forming gas (N_2/H_2) at 420ºC for 30 min., followed by rapid thermal anneal (RTA) at 800-1000ºC for a duration of ~20 s.

The C-V characteristics were measured on large area (50x50 μm^2) MOS capacitors with an HP 4285A LCR meter at a high frequency (100 kHz). EOT and the flat-band voltage V_{fb} were simulated by taking into account the quantum mechanical correction. The current-voltage measurements were performed using an HP 4156A semiconductor parameter analyzer. Values of metal gate work function Φ_m were extracted from plots of V_{fb} versus the gate dielectric EOT.

4.4 Results and Discussion

4.4.1 Metal Gate on SiO_2 Gate Dielectric

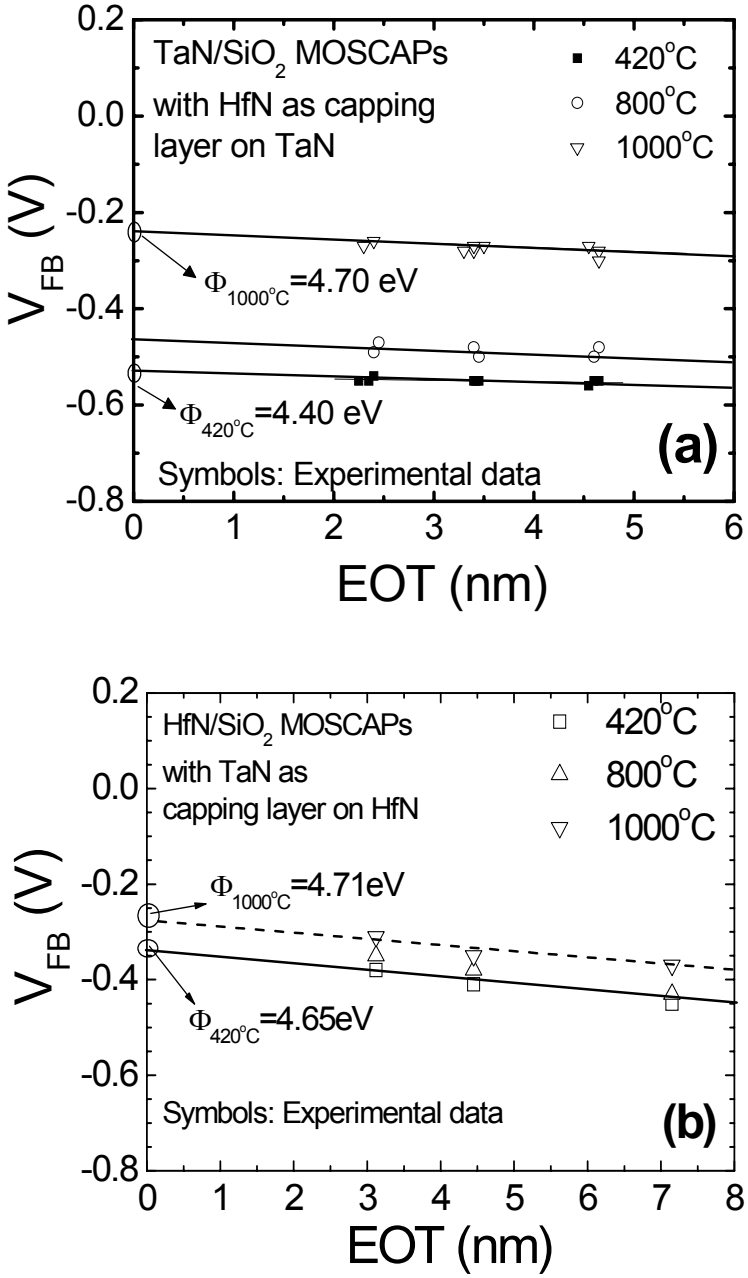

Fig. 4.2. Flat band voltage V_{FB} versus SiO_2 dielectric thickness after annealing at various temperatures for (a) HfN/TaN/SiO_2/Si, and (b) HfN/SiO_2/Si MOS capacitors.

Fig. 4.2 shows the extraction of Φ_m for HfN/TaN/SiO_2 and HfN/SiO_2 capacitors that were annealed at various temperatures. It is interesting to note that for TaN on SiO_2, TaN Φ_m significantly increases from 4.4eV after forming gas anneal

(FGA) to ~4.7eV after 1000°C post gate anneal (PGA); while for HfN on SiO_2, HfN Φ_m exhibits excellent thermal stability (change from 4.65eV after FGA to ~4.71eV after 1000°C PGA).

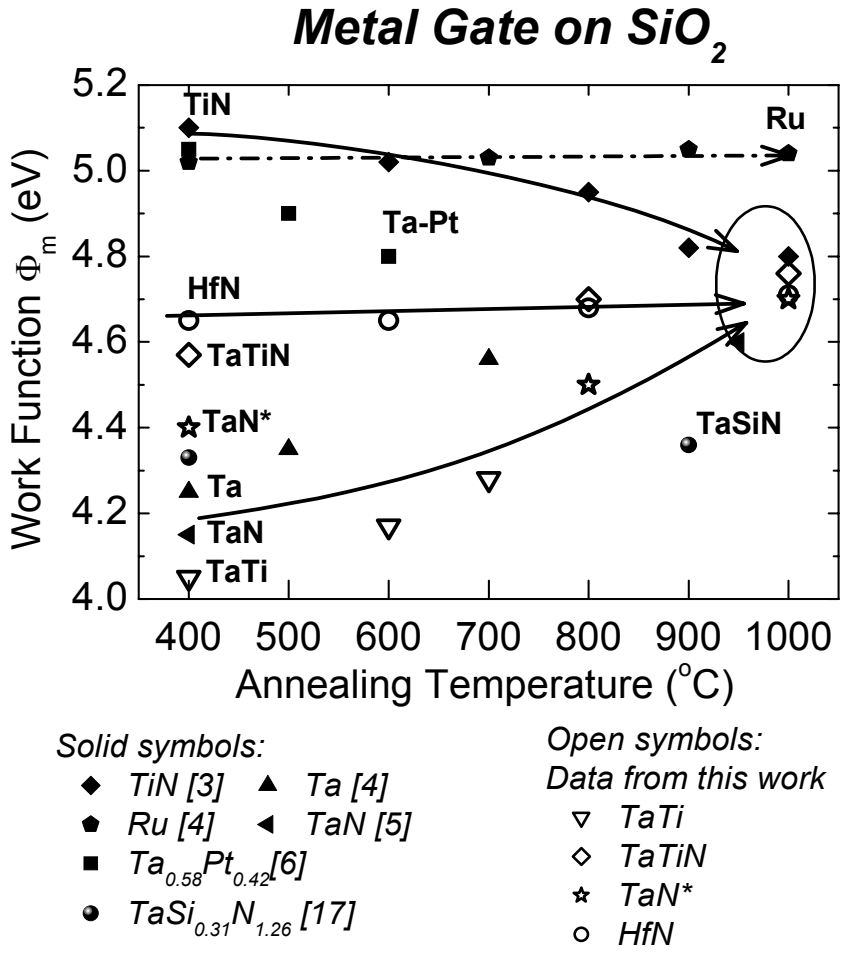

Fig. 4.3. The variation of metal gate work function Φ_m with the annealing temperature. The gate dielectric is SiO_2. Intrinsic states at the interface of metals and SiO_2 do not play a very significant role in modifying the vacuum metal work function. Therefore, the change of Φ_m with increasing temperature is predominantly due to extrinsic states.

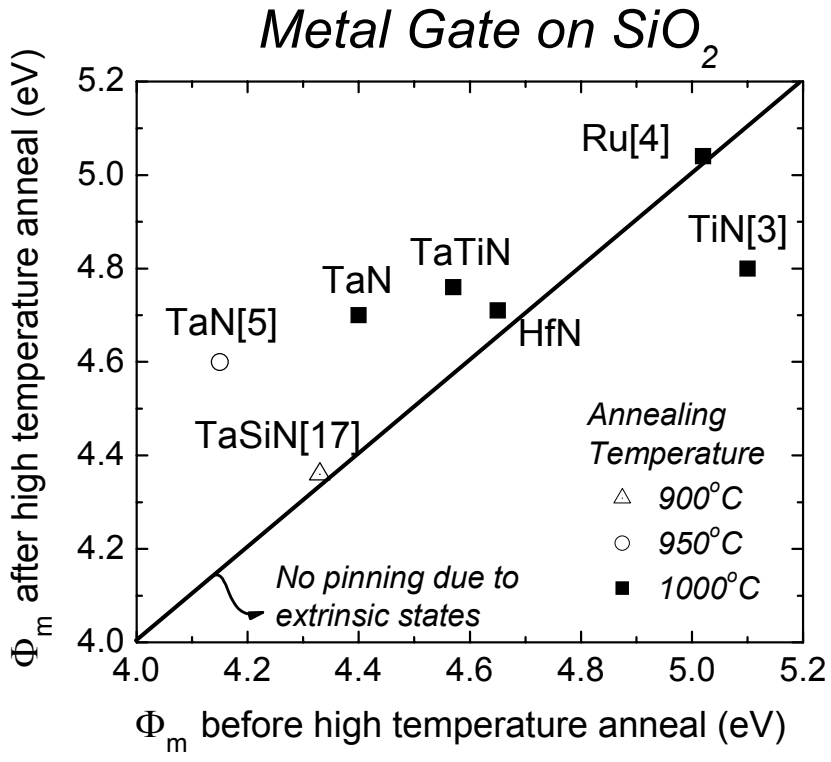

Fig. 4.4. Work function of metal gates on (a) SiO_2 and (b) HfO_2 before and after annealing at high temperatures. A 400°C anneal was performed prior to the high temperature anneal.

The variation of Φ_m with annealing temperature for various metal gate materials on SiO_2 is summarized in Fig. 4.3, showing that annealing temperature is a major factor affecting Φ_m. Experimental data from the literature [3-6,17] are also included in this figure. Another way to illustrate the impact of high temperature (high-*T*) anneal is to plot Φ_m before and after annealing on the horizontal and vertical axes, respectively, as shown in Fig. 4.4. When the work function of a metal gate does not change appreciably upon annealing at high temperature, it contributes a data point on the solid invariant line. Most data points deviate from the solid invariant line, emphasizing that Φ_m of most metal gates on SiO_2 change considerably upon high-*T* annealing. The change in Φ_m is not attributed to new compounds (new metal silicide

or new high-K material) formation at metal/SiO_2 interface [3,8]. It is noticed that negligible interfacial reaction occurs between TaN or HfN and the SiO_2 gate dielectric, as the EOT of the gate dielectric did not change upon annealing (Fig. 4.5).

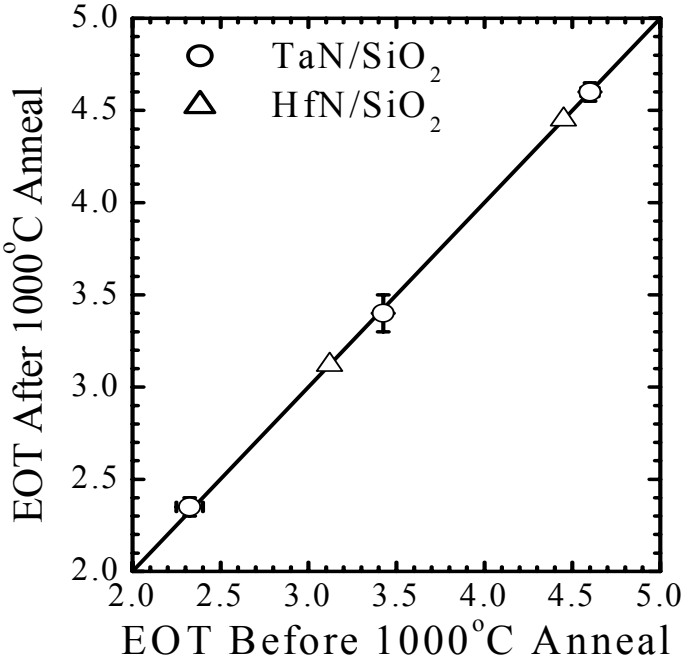

Fig. 4.5. Gate dielectric EOT of HfN/TaN/SiO_2 or HfN/SiO_2 devices does not change significantly after 1000ºC anneal.

In Fig. 4.3, a noteworthy trend is that the work function of metals like TiN, Ta, TaTi, TaN, TaPt, TaTiN, and HfN converge as the annealing temperature increases. This suggests metal gate Fermi levels are pinned at about 4.7-4.8 eV below the vacuum level, with the assumption that the volume workfunction of the bulk metal is unchanged after the post anneal. For SiO_2 dielectric, it is known that MIGS (or intrinsic states) at the metal-SiO_2 interface do not significant modify the vacuum work function of the metal [2]. Therefore the change in Φ_m with increasing temperature is likely to be due to the existence of a high density of localized extrinsic states. While

the annealing time for these data may vary, it appears that the major factor determining the above mentioned Fermi pinning is the annealing temperature. Extrinsic states, usually associated with bonding defects, drive the Fermi pinning and the convergence of Φ_m. The possible source of the extrinsic states could be oxygen-related vacancies, nitrogen-related vacancies, or metal-Si bonding defects at the metal-dielectrics interface. Given the chemical similarity of Ti, Hf, and Ta, it is plausible that extrinsic states with similar characteristics are formed between SiO_2 and these metals.

Note that the charge neutrality level for SiO_2, which is used to explain the Fermi pinning induced by MIGS (or intrinsic states) [2], would not be expected to play an important role to determine the extrinsic states pinning level.

It was recently reported that Fermi pinning occurs at the interface of poly-Si/HfO_2 and poly-Si/Al_2O_3, resulting in high transistor threshold voltages [18]. This work suggests that Fermi pinning due to extrinsic states also occurs at the interface of metal gate and SiO_2. Additionally, it is found that the extent of Fermi pinning increases with increasing annealing temperature. Elevation of the annealing temperature probably increases the density of extrinsic states and their effectiveness in pinning the Fermi level of the metal gate.

4.4.2 Fermi Level Pinning Induced by Localized Extrinsic States – the Model

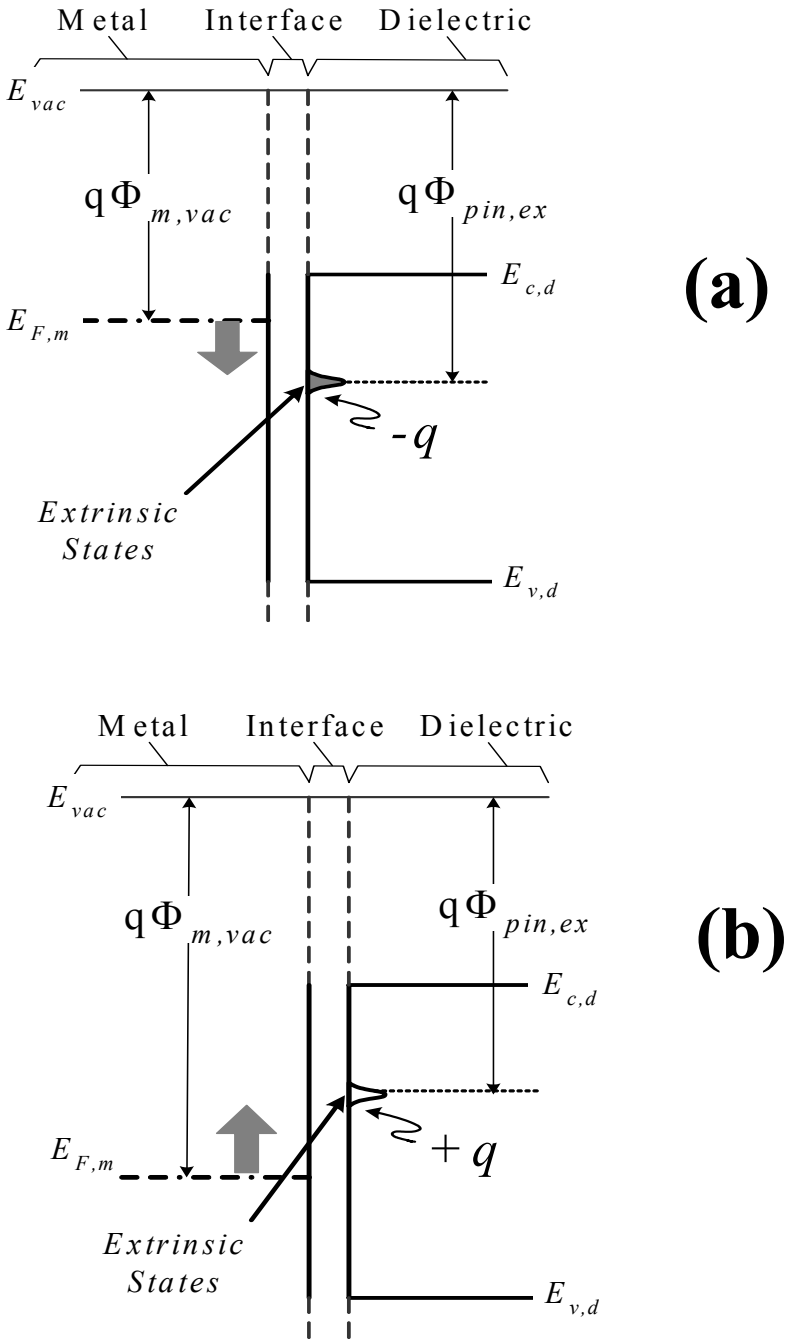

Fig. 4.6. Schematic energy band diagram for a metal gate on a dielectric, showing extrinsic states that pin the metal Fermi level. (a) When $E_{F,m}$ is above the pinning level, (b) When the $E_{F,m}$ is below the extrinsic pinning level. The conduction band edge and the valence band edge of the dielectric are denoted by $E_{c,d}$ and $E_{v,d}$, respectively.

Fig. 4.6 shows the model for a metal-dielectric interface where extrinsic states dominate. Fig. 4.6(a) illustrates the case where the metal Fermi level $E_{f,m}$ is above the energy level of the extrinsic states, and hence the empty states at the pinning location (at an energy $q\Phi_{pin,ex}$ below the vacuum level) are filled with electrons from the metal. This creates an interface dipole that is charged negatively on the dielectric side, driving $E_{f,m}$ towards the pinning position. Vice versa, for the case where the metal Fermi level $E_{f,m}$ is below the energy level of the extrinsic states, as shown in Fig. 4.6(b), the existing electrons at the pinning level tend to redistribute toward the metal side, resulting in an interface dipole that is charged positively at the dielectric side. The Fermi pinning effect will be less pronounced if $E_{f,m}$ is close to the pinning level of the extrinsic states. The extrinsic pinning level could be related to the interfacial bonding defects between the gate electrode and the gate dielectrics, and is thus determined by both the gate electrode and the gate dielectric materials. Pinning levels induced by Hf-Si and Al-O-Si bonds (defects) have been reported for poly-Si/HfO_2 and poly-Si/Al_2O_3 interfaces, respectively [18].

It should be noted that the creation of extrinsic states and the resulting Fermi pinning is not a universal phenomenon that occurs for all combinations of metal gates and gate dielectrics. Extrinsic states are absent at a defect-free interface where the metal work function is predominantly determined by intrinsic states. In Fig. 4.3, the work function of HfN, Ru and $TaSi_{0.31}N_{1.26}$ changes little with annealing temperature. This could be possibly due to the absence of extrinsic states at the associated interfaces or, for the case of HfN, the close alignment between the $E_{f,m}$ and the Fermi pinning level.

4.4.3 Metal Gate on HfO_2 Gate Dielectric

Next, let us turn to the metal-HfO_2 interface to examine the stability of Φ_m on a promising high-K gate dielectric. The value of Φ_m on HfO_2 is considerably determined by intrinsic states or MIGS even before high temperature annealing. Fig. 4.7 shows the extraction of Φ_m for HfN/HfO_2 capacitors after various thermal treatments. A similar Φ_m extraction is performed for HfN/TaN/HfO_2 capacitors. The values of Φ_m of various metals on HfO_2 dielectric before and after high-T anneal are plotted in Fig. 4.8. It is observed that the work function of a metal such as TaN or TaSiN appears to be more thermally stable on HfO_2 than on SiO_2. In addition, it is seen the tighter distribution of data points near the invariant line of Fig. 4.8, as compared to case shown in Fig. 4.4. This is possibly due to two reasons. Firstly, intrinsic states at the metal-HfO_2 interface already have a significant effect on the modification of Φ_m [1,2], and the role of extrinsic states is comparatively diminished. Secondly, it could be possible that the creation of extrinsic states or interfacial bonding defects upon thermal annealing is less significant for metal gates on HfO_2 compared to metal gates on SiO_2. The likelihood of extrinsic states generation could be determined by the chemical constituents in the gate dielectric and the gate electrode. For example, given the similarity in atomic radii and electronegativity of metal atoms in the metal gate investigated in this work and the metal atoms (the hafnium) in the HfO_2 high-K gate dielectric, it is plausible that chemical reactions are less likely to occur at the metal-HfO_2 interface than at the metal-SiO_2 interface [7].

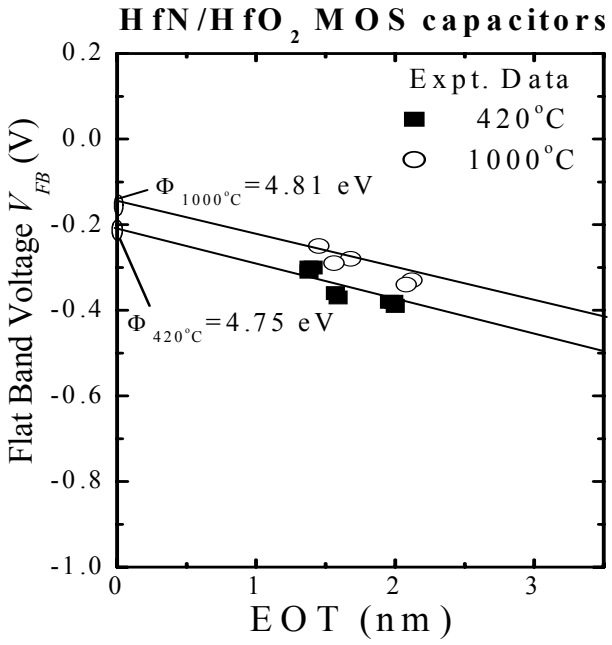

Fig. 4.7. Plot of V_{fb} versus EOT of $HfN/HfO_2/Si$ MOS capacitors before and after 1000°C anneal.

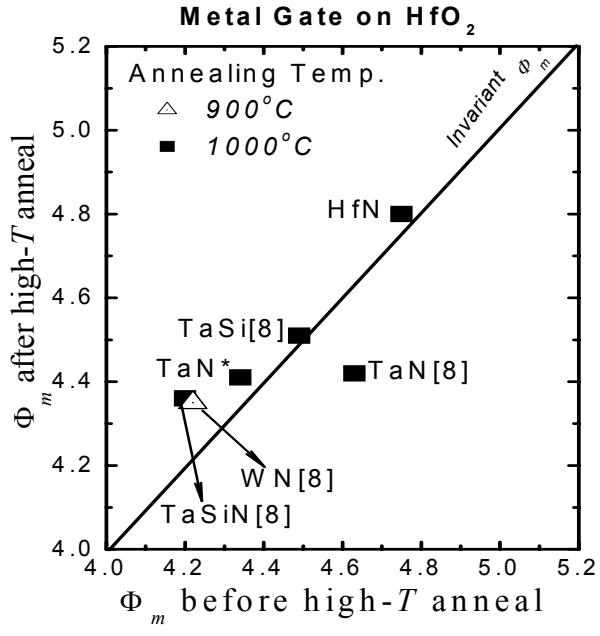

Fig. 4.8. Impact of high temperature anneal on metal work function on HfO_2. (data TaN* is from this work)

4.5 Conclusion

The dependence of metal gate work function on annealing temperature was investigated. A metal-dielectric interface model that takes the role of extrinsic states into account was proposed to qualitatively explain the work function instability phenomenon. The creation of extrinsic states and the resulting Fermi level pinning of the metal gate work function is observed for several combinations of metal gate and gate dielectric materials, particularly when the gate dielectric is SiO_2. The effect appears to be thermodynamically driven, becoming more pronounced when the annealing temperature is higher. In general, the generation of extrinsic states upon annealing is less significant for metal gates on HfO_2 compared to metal gates on SiO_2. Interface dipole formation plays an important role in determining the amount of Fermi pinning and the threshold voltage of metal gate transistors.

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Chapter 5

Investigation of Hole Tunneling Current through Ultrathin Oxynitride/Oxide Gate Dielectrics

5.1 Introduction

As discussed in the 1st chapter, silicon oxynitride, silicon nitride and other high-K materials have been extensively studied to replace the conventional silicon dioxide as the gate dielectrics to address the excessive gate leakage current concern with the continued scaling of the MOSFETs devices [1,2]. Due to the difficulties in integrating high-K material processing into the conventional CMOS process and reliability concerns associated with high-K materials, it is most likely that oxynitride/oxide and nitride/oxide stack films to be utilized as the alternative of pure oxide until the 65-nm technology node [1,3-5].

Electron tunneling through ultrathin oxynitride/oxide and nitride/oxide stack films has been extensively studied [6-9]. To our knowledge, work on hole tunneling through a dielectric was presented only in reference 8, in which hole tunneling in pure nitride is semi-empirically modeled. It has been demonstrated that hole tunneling would dominate the gate leakage current in a *p*-MOSFET if its gate dielectric is formed by an oxynitride/oxide or nitride/oxide stack under typical gate inversion

biases ($|V_g| < 1.7$ V) [8,10]. It is also noteworthy that under such gate biases and if the gate dielectric made of nitride, gate leakage in a *p*-MOSFET (in which hole tunneling current dominates) becomes higher than that in a n-MOSFET (in which electron tunneling current dominates) [8]. Hole tunneling is more serious in nitride than oxide. This is expected since the hole barrier height (ΔE_V) at the nitride/Si interface is almost 2.6 eV lower than that at the oxide/Si interface, while the electron barrier height (ΔE_C) at the nitride/Si interface is only about 1 eV lower than that at the oxide/Si interface [6,11-13]. As a result the scaling limit of nitride gate dielectric will probably be determined by the gate leakage in a *p*-MOSFET [10]. Hence there is a need for reliable prediction of the hole tunneling current through ultrathin oxide, oxynitride, nitride and the associated stack gate dielectrics in *p*-MOSFET's.

In this chapter, we explain hole tunneling current through a stack gate dielectric film using a physical model. The results obtained by simulation using this model and results obtained experimentally for hole tunneling current through oxide, nitride, oxynitride/oxide and oxide/oxynitride/oxide stack films are reported and compared. The N concentration in oxynitride and oxynitride/oxide stack films that results in the lowest gate leakage current is obtained theoretically. Finally the theoretical scaling limit of the oxynitride/oxide stack gate dielectric in MOSFET's is obtained.

5.2 Theoretical Background

5.2.1 Direct Tunneling

The basic mechanism of direct tunneling is schematically illustrated in Fig. 5.1. When the oxide voltage drop (V_{ox}) is less than the conduction band offset (ΔE_C) between gate dielectrics and Si, direct tunneling occurs, where the carrier tunnels through a trapezoidal barrier.

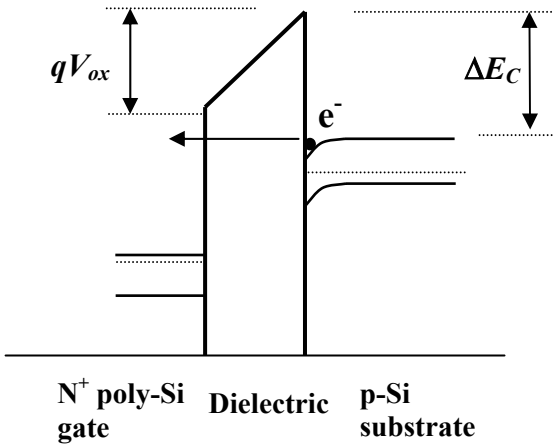

Fig. 5.1. Schematic sketch of electron direct tunneling in an n-MOS device under inversion.

Quantum theory predicts there is still a probability of carrier tunneling through forbidden region of the barrier. Different from the well-known Fowler-Nordheim (F-N) tunneling through a triangular barrier, the tunneling distance does not change with the oxide field in direct tunneling, and there is no simple dependence of the tunneling current density on voltage or electric field [14]. It is projected that the operating voltage will be reduced to 1.0 V or less within this decade, and modern MOS devices will be operated in the direct tunneling regime (gate dielectrics thickness < 4 nm).

5.2.2 Basic Quantum Mechanical Effect in MOS Devices

Fig.5.2 gives an illustration of the the carrier quantization phenomenon in the Si substrate. In the presence of an electric field, the energy band are bent strongly near the semiconductor-dielectrics interface, a potential well will be formed by the oxide barrier and the eletrostatic potential in the semiconductor, as shown in Fig. 5.2(a). The carriers will be confined in the potential well and form discrete sub-bands due to the confinement Instead of continuous classical three-dimensional (3-D) states. In the other two directions, the carriers are still free and consequently show 2-D characteristics. The lowest subband energy is shifted from the bottom of the bulk band to a higher value, as shown in this figure. Another highlight for 2-D carriers is the different density distribution in the z direction from that for 3-D carriers.

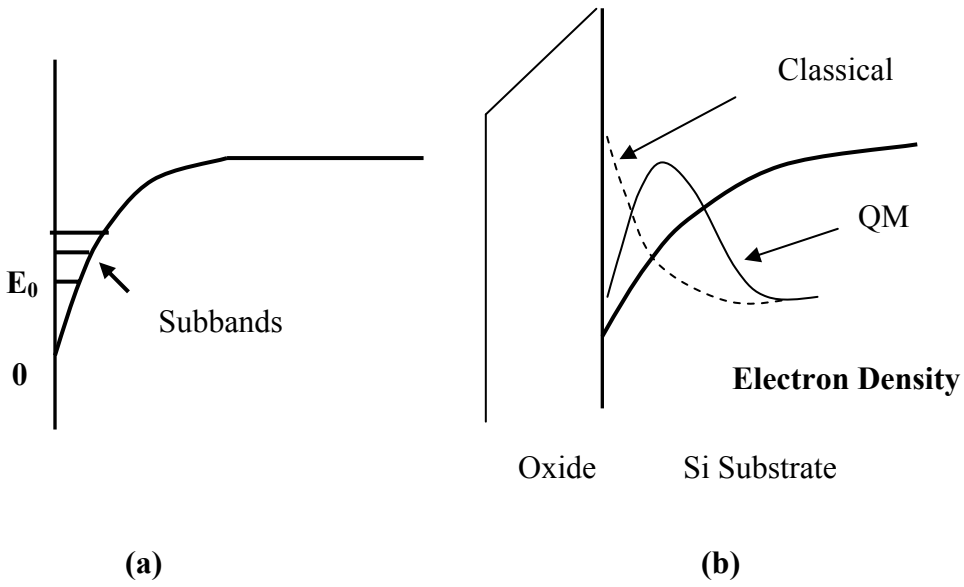

Fig. 5.2. Schematic illustration of the quantum mechanical effect (a) energy quantization, (b) carrier density distribution in the Si substrate.

Fig. 5.2 (b) shows the respective the electron and hole density distributions (schematic illustration) in the substrate calculated by the quantum mechanical (2-D) and classical (3-D) models [15]. The density distribution of the 2-D carriers is displaced from the Si/SiO_2 interface and the peak of carrier density is deeply positioned into the substrate, which peaks at the surface for the 3-D carriers case. The displacement of the carrier distribution, i.e. the finite thickness of the inversion/accumulation layers due to quantum mechanical effects, will increase the effective oxide thickness and correspondingly decrease the total capacitance of the device.

5.2.3 Conduction Mechanism

5.2.3.1 Carrier Separation Measurement

Carrier separation experiments [10] are applied to study the conduction mechanism in dual-gate CMOS transistors. The schematic experimental set-up is shown in Fig. 5.3.

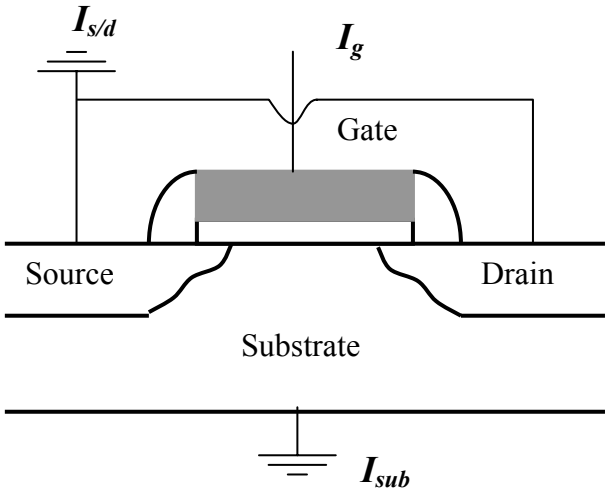

Fig.5.3. The cross-sectional schematics of the carrier separation measurement.

During the measurement, the source and drain of the transistor were tied together and grounded together with the substrate terminal. The static I-V characteristics were monitored using an HP4156A semiconductor parameter analyzer. The carrier separation experiments were conducted to measure the gate current I_g, the sum of the source and drain currents $I_{s/d}$, and the substrate current I_{sub} separately when a gate voltage Vg was applied to the gate terminal. All currents flowing into the device are taken as positive and $I_g + I_{s/d} + I_{sub} = 0$ if there are no other leakage channels.

When the device is biased in the inversion mode, $I_{s/d}$ measures the minority carriers current while I_{sub} measures the current of majority carriers. The carrier separation measurement in accumulation is a little more complicated to explain due to the possible electron-hole recombination process [16]. Under accumulation conditions, the device can be regarded as a quasi-bipolar transistor. The substrate acts as the base and I_{sub} measures the majority current in the base. The source/drain acts as the collector and $I_{s/d}$ measures the minority current in the base. If without electron-hole recombination, when applying negative (positive) gate voltage to the n-MOSFET (p-MOSFET), the $I_{s/d}$ and I_{sub} are the electron (hole) and hole (electron) currents, respectively. However, the recombination may become significant in some cases, where high density of recombination centers (interface traps, defects, etc) is present at the substrate surface. This case will be explained in detail during the following discussions.

5.2.3.2 Conduction Mechanism in P^+ Poly-Silicon Gate P-MOSFET's

Typical carrier separation experimental I-V curves for a p-MOSFET with SiO_2 as gate dielectrics are shown in Fig. 5.4. Under inversion (Fig. 5.4a), $I_{s/d}$ (hole current) dominates the gate leakage in the scale of 0 ~ 2 V, and the I_{sub} (electron current) become dominant at higher gate voltage. The corresponding band diagram is shown in Fig.5.5a. The positive hole current ($I_{s/d}$) is due to the tunneling of holes in the inversion layer to the gate. Electron tunneling from the gate could stem from both the conduction band electrons and the valence band electrons. Due to heavily doped p^+ gate, the inversion of the p^+ gate becomes impossible. As a result, the electron density in the conduction band of the p^+ gate is negligible and the electron current (I_{sub}) is mainly due to the valence band electron tunneling. It is also noteworthy the change of sign in the $I_{s/d}$ as shown in Fig. 5.4a, which results from the impact-ionization. The holes generated by impact-ionization, as the minority carriers in the n-type substrate of the p-MOSFET, are collected by the source/drain and lead to a negative $I_{s/d}$.

In the case of accumulation mode in Fig. 5.4b, the gate leakage is dominated by the tunneling of accumulated electrons in the substrate (I_{sub}). The hole current ($I_{s/d}$) is explained as following. Two tunneling mechanisms are accounted for: the accumulated holes in p^+ gate tunneling to substrate, and the holes generated by valence band electron in the substrate tunneling back to the gate. From the band diagram analysis in Fig. 5.5b, the valence band hole tunneling (from gate to substrate) occurs at Vg > ~ 1V (flat-band voltage, the V_{FB}) while the valence band electron tunneling from the substrate is possible only when $Vg > V_{FB} + (E_g)_{Si}$, where the $(Eg)_{Si}$ stands for the Si band gap (~ 1.1 V). Therefore, it is concluded that the $I_{s/d}$ below ~ 2.1 V is due to the hole tunneling, while valence band electron tunneling possibly contribute to the $I_{s/d}$ when Vg is higher than ~ 2.1 V.

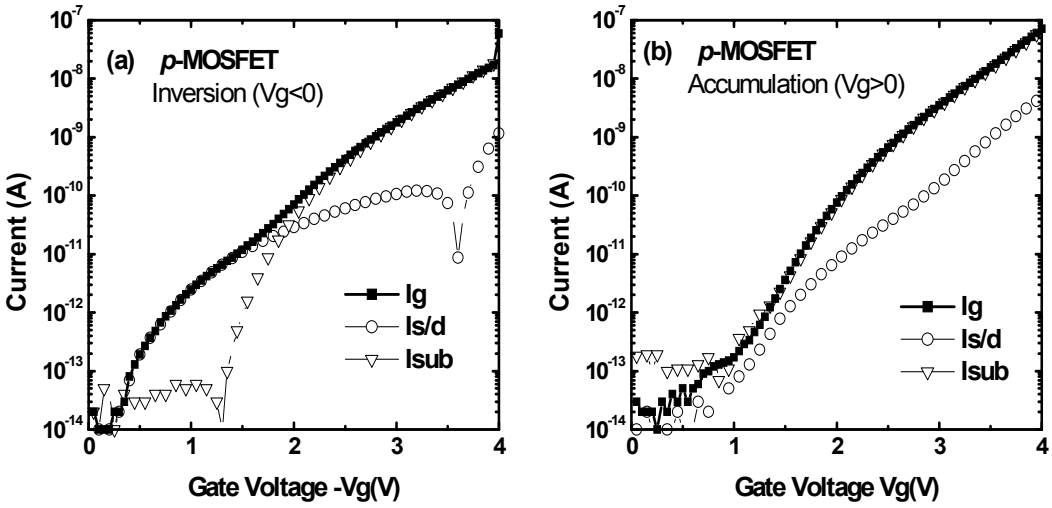

Fig. 5.4. I-V characteristics (carrier separation) of a typical p^+ poly-silicon gate p-MOSFET (SiO_2 as gate dielectrics) under (a) the inversion, and (b) the accumulation biases.

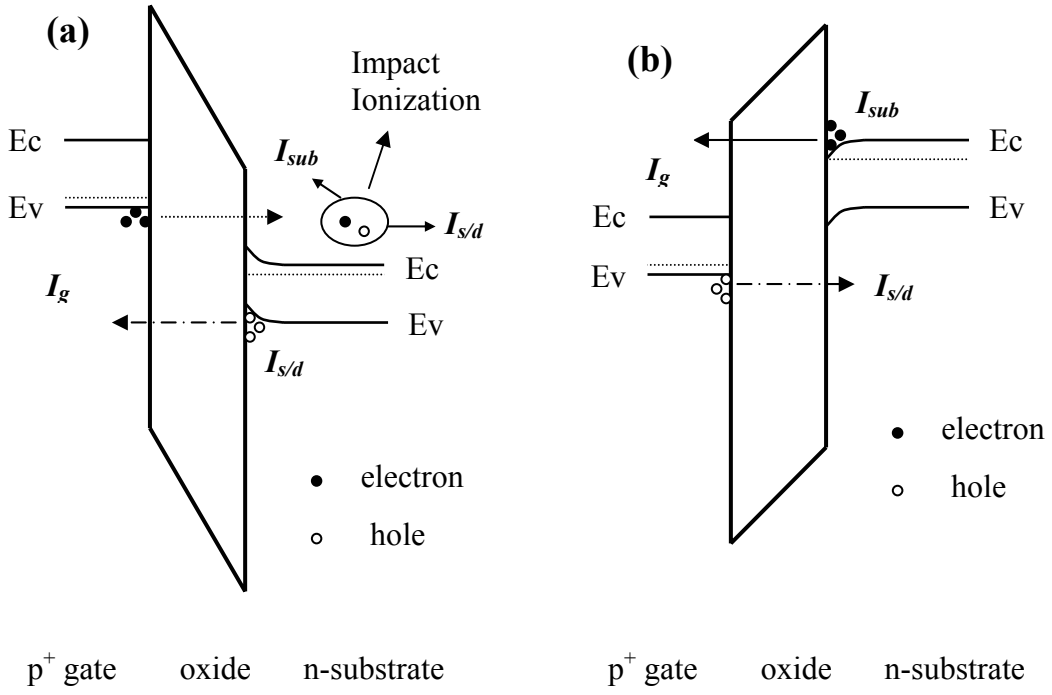

Fig. 5.5. Schematic band diagram of a p-MOSFET under (a) the inversion, and (b) the accumulation biases.

5.2.3.3 Conduction Mechanism in N^+ Poly-Silicon Gate N-MOSFET's

First, we will analyze I-V curves under the inversion bias as shown in Fig. 5.6a. The electron current ($I_{s/d}$) dominates the gate leakage, while the magnitude of hole current (I_{sub}) is 1 ~ 2 orders lower than $I_{s/d}$. The corresponding band diagram is given in Fig. 5.7a. The gate current is formed by the inversion electrons tunneling from the substrate to the gate. The electron density is high at substrate surface, and steady current could be established by supplying electrons to the inversion layer from the source/drain. The substrate current is interpreted as due to electron tunneling from the substrate valence band. When an electron is tunneled to gate, a hole will be left behind, which in turn diffuses into the substrate and forms the negative I_{sub}. The valence band electron tunneling occurs when Vg > ~1V (flat-band) and its much smaller magnitude is due to the higher tunneling barrier (~ 4.2 eV) for valence band electron than that for the conduction band electron (~ 3.1 eV).

Next, let us turn on for the case of accumulation. Fig. 5.6b shows that the gate current mainly stems from the $I_{s/d}$. From the band diagram shown in Fig. 5.7b, the dominant tunneling channel is the accumulated electrons tunneling from the n^+ polysilicon gate to the substrate. The electrons, as minority carriers in the p-type substrate of the n-MOSFET, are collected by the source/drain as the negative $I_{s/d}$. Fig. 5.6b shows the substrate current is of a much smaller magnitude and there is a change of the sign near ~ 4 V.

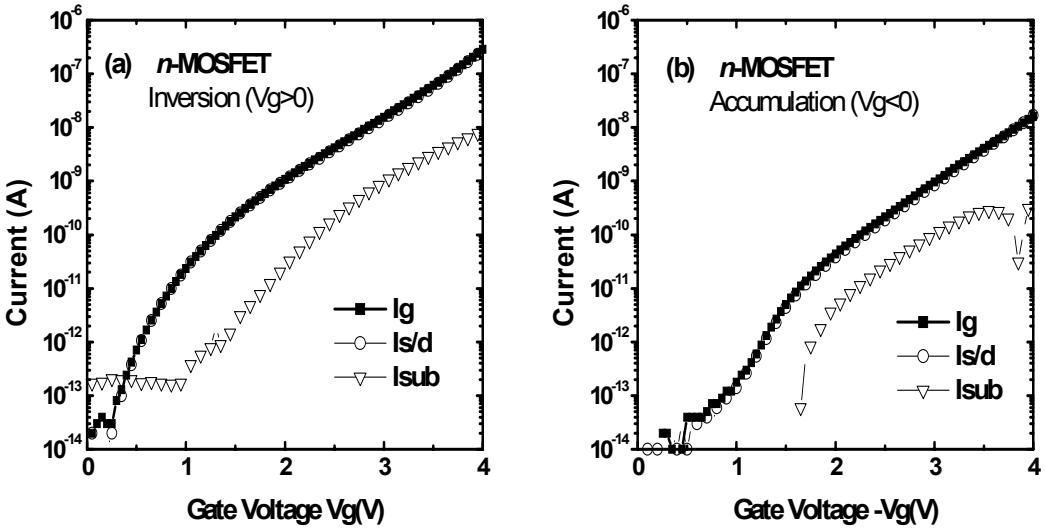

Fig. 5.6. I-V characteristics (carrier separation) of a typical n^+ polysilicon gate n-MOSFET (SiO_2 as gate dielectrics) under (a) the inversion, and (b) the accumulation biases.

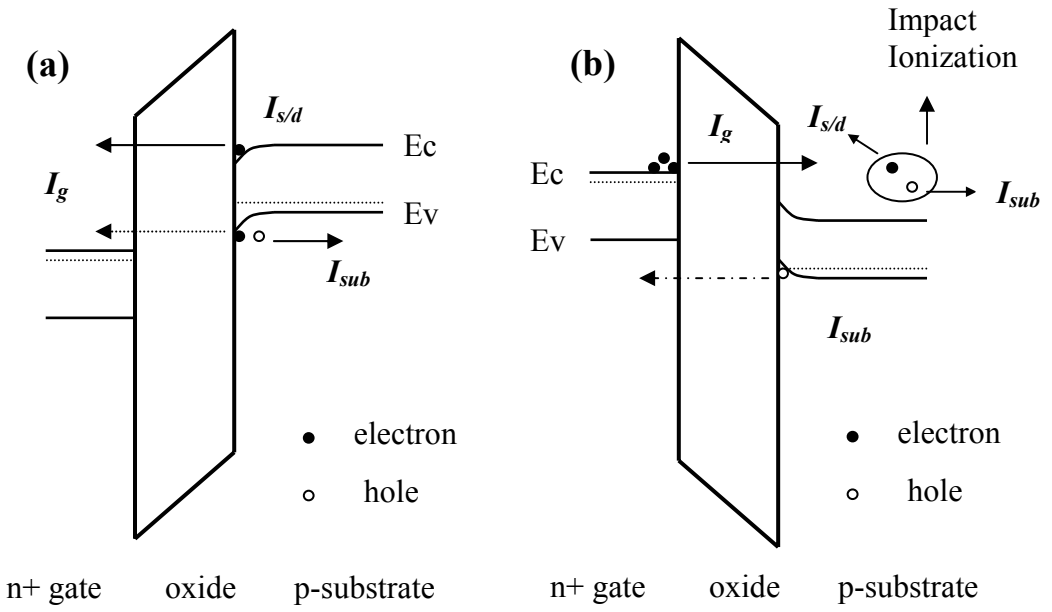

Fig.5.7. Schematic band diagram of a n-MOSFET under (a) the inversion, and (b) the accumulation biases.

Positive I_{sub} at low gate voltage is dominated by the accumulated holes tunneling from the substrate to the gate. At higher gate voltage, impact ionization

induced by the high energetic electrons injected from the gate generates the electron-hole pairs in the substrate. While the generated electrons are collected by the source/drain, the holes diffuse to the substrate terminal, forming the negative hole current. The change of sign in *Isub* will occur when the magnitude of the impact-ionization induced hole current (negative) becomes larger than the valence hole tunneling current (positive).

5.2.4 Modeling of Hole Current for p-MOSFET's Under Inversion

In the model, the gate stack dielectrics are assumed to be made up of several dielectric layers, each layer having a different dielectric constant, gap energy as well as electron and hole barrier height, as illustrated in Fig. 5.8

For a *p*-MOSFET under inversion, the holes are confined in the inversion layer and form discrete 2-D sub-bands [17]. For such 2-D sub-bands, the hole tunneling current can be expressed as [18, 19]

$$J = \sum_n N_n / \tau_n(E_n) \qquad (5\text{-}1)$$

where N_n and τ_n are the hole density and hole lifetime of the nth sub-band respectively. The lifetime of a quasi-bound state can be obtained semi-classically by

$$\frac{1}{\tau_n(E)} = \frac{T(E)}{\int_0^{z_n} \sqrt{2m^*_{\perp n} / [E_n - E_V(z)]}\, dz} \qquad (5\text{-}2)$$

where $T(E)$ is the hole transmission probability, E_n the sub-band energy for the nth quasi-bound state, $E_V(z)$ the edge of the Si valence band, and z_n the classical turning point for the nth bound state. It has been demonstrated that the lifetime evaluated by this formula is comparable to that obtained by rigorous quantum mechanical methods [20,21]

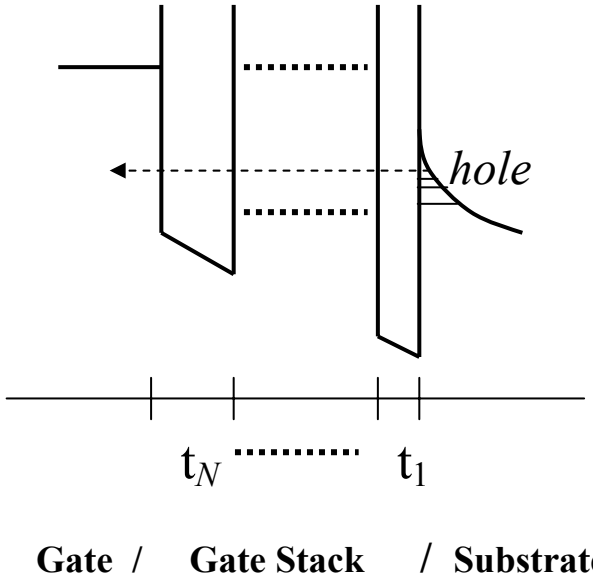

Fig. 5.8. Energy band diagram of a p-MOSFET in inversion, assuming the gate stack dielectrics contain N different layers (from t_1 to t_N). The inverted holes are confined in the inversion layer and form discrete 2-D subbands.
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The sub-band energies and hole densities in the inversion layer are determined by an improved one-band effective mass approximation (EMA) [18]. One feature of hole quantization that is distinct from electron quantization is the valence band mixing effect [17]. In the traditional one-band EMA [22,23], the hole effective masses derived from the bulk Si are used. Band mixing effect is neglected in the traditional one-band EMA, thereby resulting in the underestimation of the density of states and overestimation of the quantum mechanical effect [17]. In this improved one-band EMA, the hole effective masses are extracted from the results of the rigorous six-band

EMA with the valence band mixing effect included, thereby resulting in a more accurate modeling of the hole electrostatics in the inversion layer. The resulting sub-band energies, hole densities and surface potential for a p-MOSFET at inversion are consistent with those obtained from the more complex six-band EMA.

From Eq. 5-2, *T(E)* is obtained by a modified Wentzel-Kramers-Brillouin (WKB) approximation. For gate stack dielectrics with *N* layers, it is shown that

$$T(E) = T_R(E) \cdot T_1(E) \cdot T_2(E) \cdots T_N(E) \qquad (5\text{-}3)$$

where the correction factor T_R can be expressed as a function of the group velocities of the tunneling carrier:

$$T_R = \frac{4\nu_{Si}(E)\nu_{OX}(E_{OXi})}{\nu_{Si}^2(E)+\nu_{OX}^2(E_{OXi})} \times \frac{4\nu_{Si}(E+qV_{OX})\nu_{OX}(E_{OXo})}{\nu_{Si}^2(E+qV_{OX})+\nu_{OX}^2(E_{OXo})} \qquad (5\text{-}4)$$

where $\nu_{Si}(E)$ and $\nu_{Si}(E+qV_{OX})$ are the group velocities of the carriers incident and leaving the oxide layer, respectively. V_{OX} is the oxide voltage drop whereas $\nu_{ox}(E_{OXi})$ and $\nu_{ox}(E_{OXo})$ are the magnitudes of the imaginary group velocities of carriers tunneling in and out of the oxide layer, respectively [24,25], and $T_i(E)$ the tunneling probability through the *i*th layer, such that

$$T_i(E) = \exp\left(-2\int_{t_i} \kappa_i(E,z)dz\right) \qquad (5\text{-}5)$$

where κ_i is the imaginary wave number within the *i*th layer and t_i the layer thickness.

To calculate the tunneling current, an accurate determination of κ_i, which is obtained by the dispersion in the dielectric energy gap, is critical. The most commonly-used dispersion relationship in the band gap of SiO_2 is the parabolic dispersion [18], where an energy-independent effective mass, m_{ox}, is assumed,

$$\frac{1}{(\eta k)^2} = \frac{1}{2m_{ox}E} \tag{5-6}$$

where E is measured from the conduction (valence) band edge for electron (hole) tunneling.

5.3 Experiments

P^+-poly/p-MOSFET's with three different types of gate dielectrics were fabricated using a standard dual-gate CMOS process. The gate dielectric in the first device type (labeled as Device 1) was formed by rapid thermal oxidation (RTO). The oxynitride/oxide (N/O) stack gate dielectric in the second device type (labeled as Device 2) was obtained by forming a thin nitride layer in NH_3 at 900°C for 30 s, followed by oxidation in O_2 at 25 atm and 850 °C for 30 min in a vertical high pressure (VHP) furnace [26]. The oxide/oxynitride/oxide (ONO) stack gate dielectric in the third device type (labeled as Device 3) was obtained by forming a thin nitride layer in NH_3 at 900°C for 10 s, followed by oxidation in N_2O at 950 °C for 30 s [27].

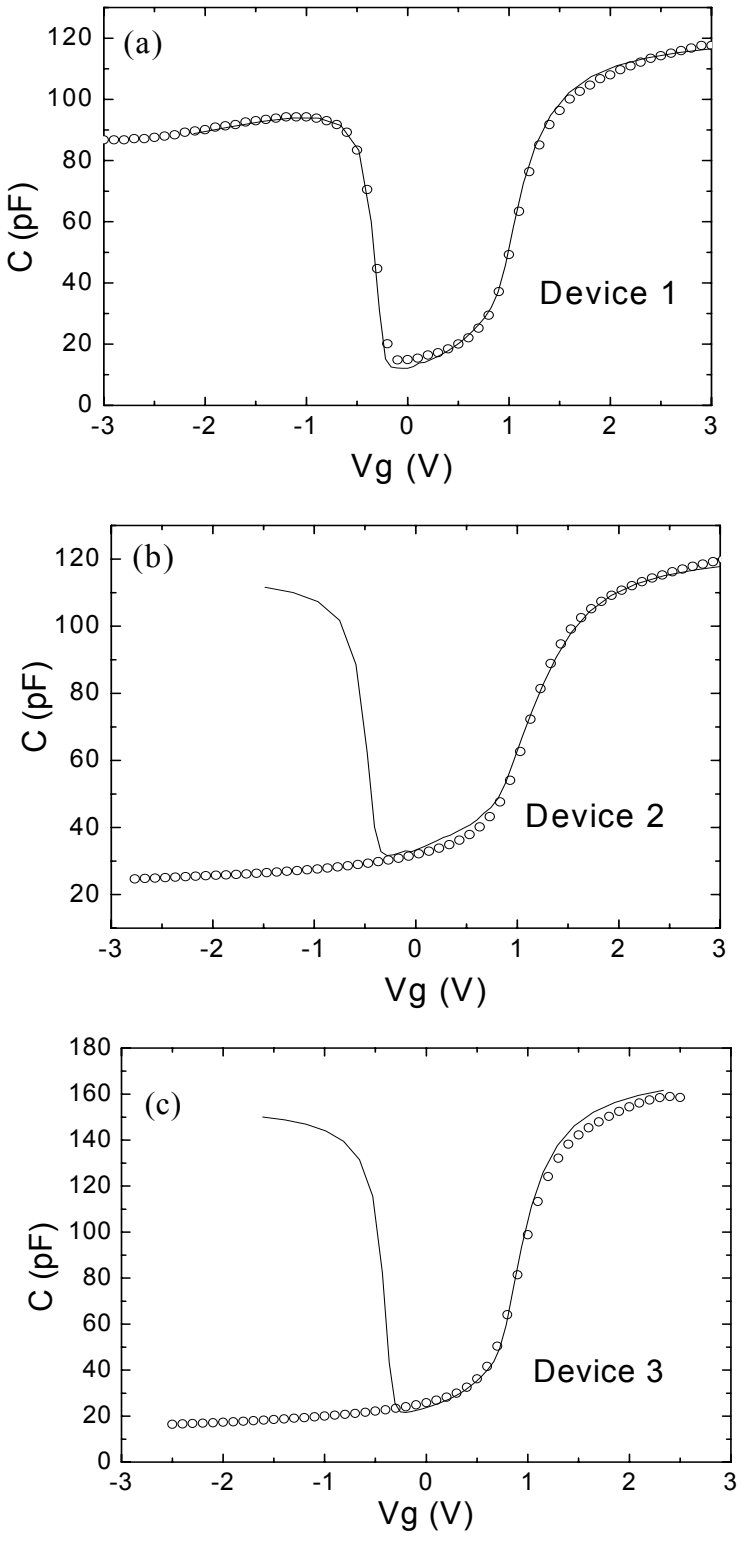

Fig. 5.9. High frequency C-V experimental data (open circles) and simulation results (solids lines) for (a) Device 1, (b) Device 2, and (c) Device 3. The device area is 10000 μm^2.

The capacitance-voltage (*C-V*) measurements were performed on large area (10000 μm^2) MOS capacitors with an HP 4285A LCR meter at a high frequency (100 kHz). Electrical oxide thickness (EOT) of all of the three types of gate dielectrics was determined in the strong accumulation region of the *C-V* curves in conjunction with quantum mechanical effects consideration. Identical EOT (~2.25 nm) of dielectrics for Device 1 and Device 2 was revealed. EOT of the dielectrics for Device 3 was determined as 1.6 nm. Negligible flat band voltage shifts (< 50 mV) from *C-V* simulations were revealed for all devices, indicating their low density of oxide charges. The current-voltage (*I-V*) characteristics were measured using an HP 4156A semiconductor parameter analyzer. Hole tunneling current is thus obtained from the source/drain current in the carrier separation measurements.

5.4 Results and Discussion

5.4.1 Simulation of Hole Tunneling Through Silicon Oxide and N/O Stack in p-MOSFET's

Fig. 5.10 shows that the hole and electron barrier height at the oxynitride/Si interface, the oxynitride gap energy, as well as the dielectric constant vary linearly with the N concentration of the oxynitride film [6,11-13]. It is seen all of the parameters show nice linear change with the composition of the silicon oxynitride.

Figs. 5.11 to 5.13 show the proposed energy band diagrams of the *p*-MOSFET's with three different gate dielectric structures used in this study. The hole

direct tunneling current formed by holes injected from the valence band of the Si substrate under inversion is also illustrated in each of these diagrams.

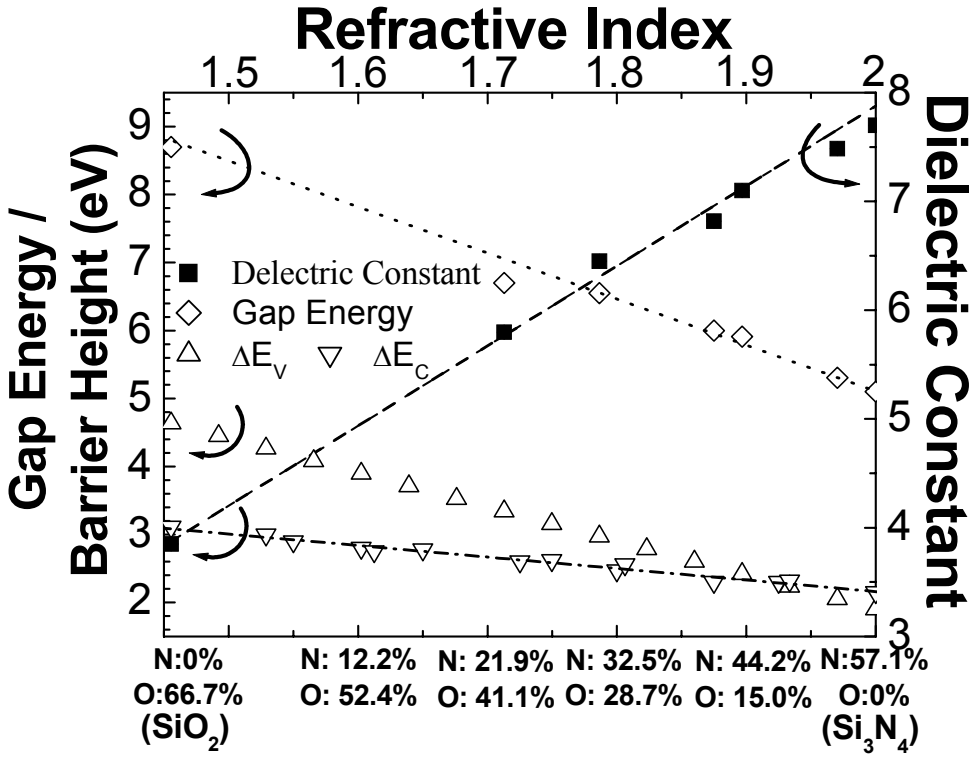

Fig. 5.10. Variation of the electron and hole barrier height at the oxynitride/Si interface (ΔE_C and ΔE_V), oxynitride gap energy (Eg), as well as dielectric constant with the oxynitride composition.

For Device 2, the oxynitride/oxide stack gate dielectric thickness obtained by High Resolution Transmission Electron Microscopy (HRTEM) is ~2.7 nm [26]. The thickness of the oxynitride and oxide layer is respectively, 2.06 nm and 0.7 nm as shown in Fig. 5.12. The inset of Fig. 5.12 shows the Secondary Ion Mass Spectrometry (SIMS) depth profile of N in the N/O stack gate dielectric of Device 2. The thickness and N concentration of the oxynitride layer can be determined from the shaded rectangular region and are respectively, 2.06 nm and 16 at. %.

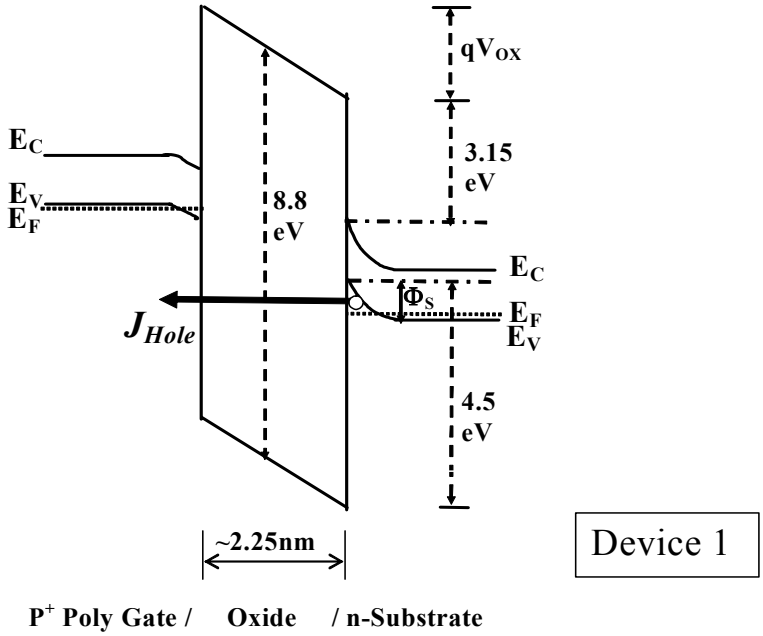

Fig. 5.11. Energy band diagram of a *p*-MOSFET with oxide gate dielectric (Device 1). Oxide thickness is determined as 2.25 nm from *C-V* measurements.

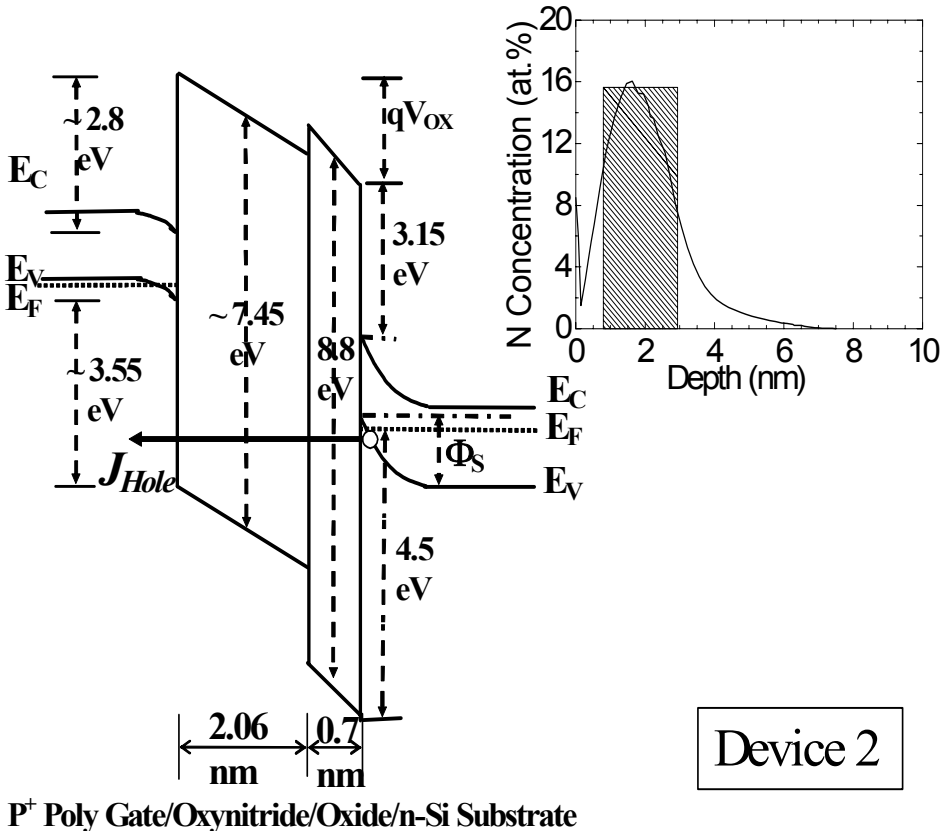

Fig. 5.12. Energy band diagram of a *p*-MOSFET with oxynitride/oxide stack gate dielectric (Device 2). Inset shows the SIMS depth profile of N in the oxynitride layer.

For device 2, in conjunction with the results shown in Fig. 5. 10, the EOT of the oxynitride layer is therefore 2.06 × 3.9 / 5.2 = 1.55 nm, where 3.9 and 5.2 are the dielectric constant of oxide and oxynitride containing 16 at. % N, respectively. This agrees with the EOT determined by *C-V* simulation.

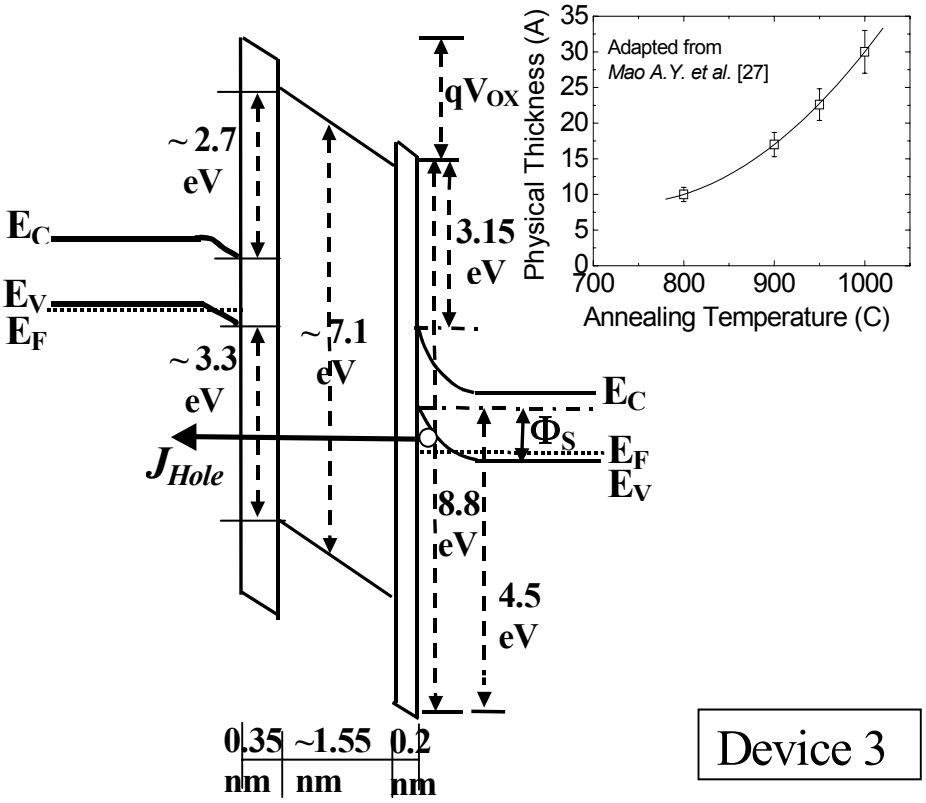

Fig. 5.13. Energy band diagram of a p-MOSFET with oxide/oxynitride/oxide stack gate dielectric (Device 3). Inset shows the variation of the physical thickness of the dielectric with annealing temperature. The 950 °C annealed gate stack in device 3 has a physical thickness of ~ 2.25 nm [27]. The N concentration in the Oxynitride in this device 3 is estimated to be around 21 at. % according to the XPS measurement. EOT of the oxynitride is 1.55 × 3.9 / 5.7 = 1.05 nm (3.9 and 5.7 are the dielectric constants obtained from Fig. 1 for the oxide and the oxynitride in device 3 respectively). EOT of the ONO stack is then 0.2+ 1.05+ 0.35= 1.6 nm, in corresponding to the EOT measurement based on *C-V* simulation.

The energy band diagram for Device 3 as shown in Fig. 5.13 is obtained from the results of an Angle Resolved X-Ray Photoelectron Spectroscopy (ARXPS) study of the ONO gate stack dielectric [27]. The inset of Fig. 5.13 shows that the 950 °C annealed ONO gate stack dielectric in Device 3 has a physical thickness of about 2.25 nm [27]. The N concentration in the oxynitride is estimated to be around 21 at. % based on the XPS measurement. Together with the results shown in Fig. 5.10. again, the EOT of the oxynitride layer is therefore 1.55 × 3.9 / 5.7 = 1.05 nm, where 3.9 and 5.7 are the dielectric constant of oxide and oxynitride containing 21 at. % N, respectively.

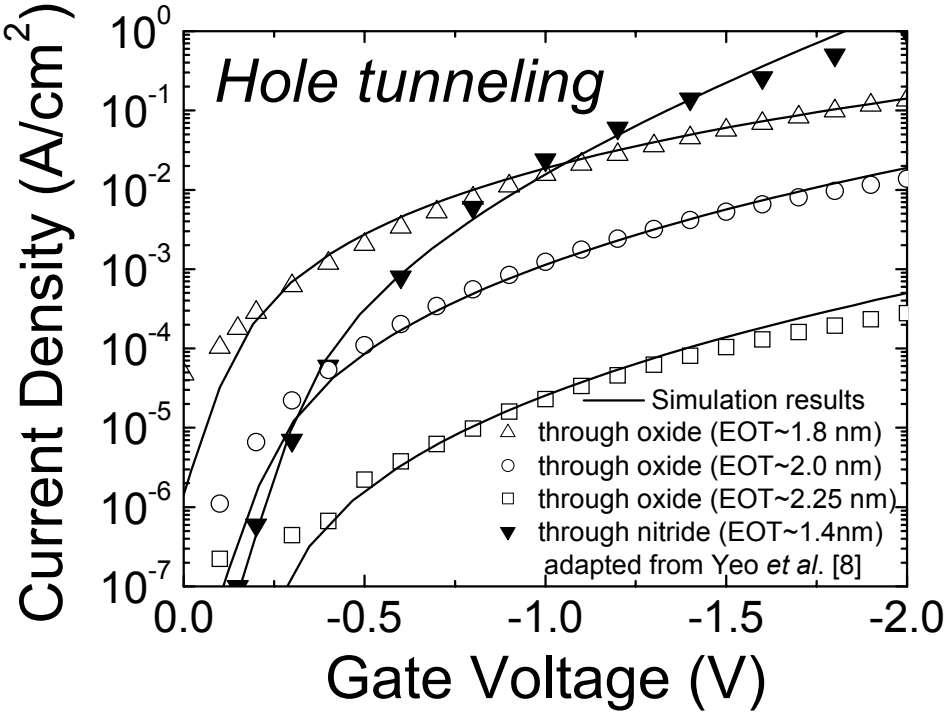

Fig. 5.14. Comparison of simulated (line) and measured (symbol) hole tunneling current through oxide and nitride gate dielectrics in *p*-MOSFETs at various dielectric thicknesses. In the simulation, $0.41m_0$ is used for the hole effective mass in both nitride and oxide [8].

Fig. 5.14 shows the simulated and measured hole tunneling current through the oxide gate dielectric in Device 1 for an oxide thickness between 1.8 and 2.25 nm, as well as through the nitride gate dielectric in another device type, hereby denoted as Device 4, for an EOT of 1.42 nm [8]. To calculate the tunneling current, an accurate determination of κ_i, which is obtained by the dispersion in the dielectric energy gap, is critical. When the oxide thickness is less than 2 nm or for tunneling current at a low gate voltage ($|V_g| < 2$ V), a parabolic approximation for hole dispersion in dielectric bandgap is applicable [18,28]. To obtain the best fit, an effective hole mass of $0.41m_0$ [8] is assumed in all the films. As shown in this figure, the discrepancy of the slope calculated at higher gate voltages from the experiments might be due to the inaccuracy of the parabolic approximation used to describe the hole dispersion in the films.

Fig. 5.15(a) compares the simulated and measured hole tunneling current through the N/O and oxide gate dielectrics in Devices 1 and 2, respectively, for the same EOT of 2.25 nm. When the gate bias is low ($|V_g| < 1.2$ V), the hole tunneling current through the N/O stack gate dielectric is almost one order of magnitude lower than the oxide gate dielectric. Fig. 5.15(b) shows the measured hole tunneling current through the ONO gate dielectric in Device 3 for an EOT of 1.6 nm. The simulated results are obtained by setting the N concentration to be 18 at. %, 21 at. %, and 24 at. % respectively. The characteristic that gives the best fit to the measured data is associated with 21 at. % N, and hence the estimated N content (~ 21 at. %) in the ONO film is justified. The good agreement between the tunneling simulation and the experiments indicates that the trap assisted tunneling mechanism such as Frenkel-Poole hopping [6] can be neglected in hole leakage current in our oxynitride samples,

which is also experimentally supported by the temperature insensitive of the gate current (see the inset of Fig. 5.15a.).

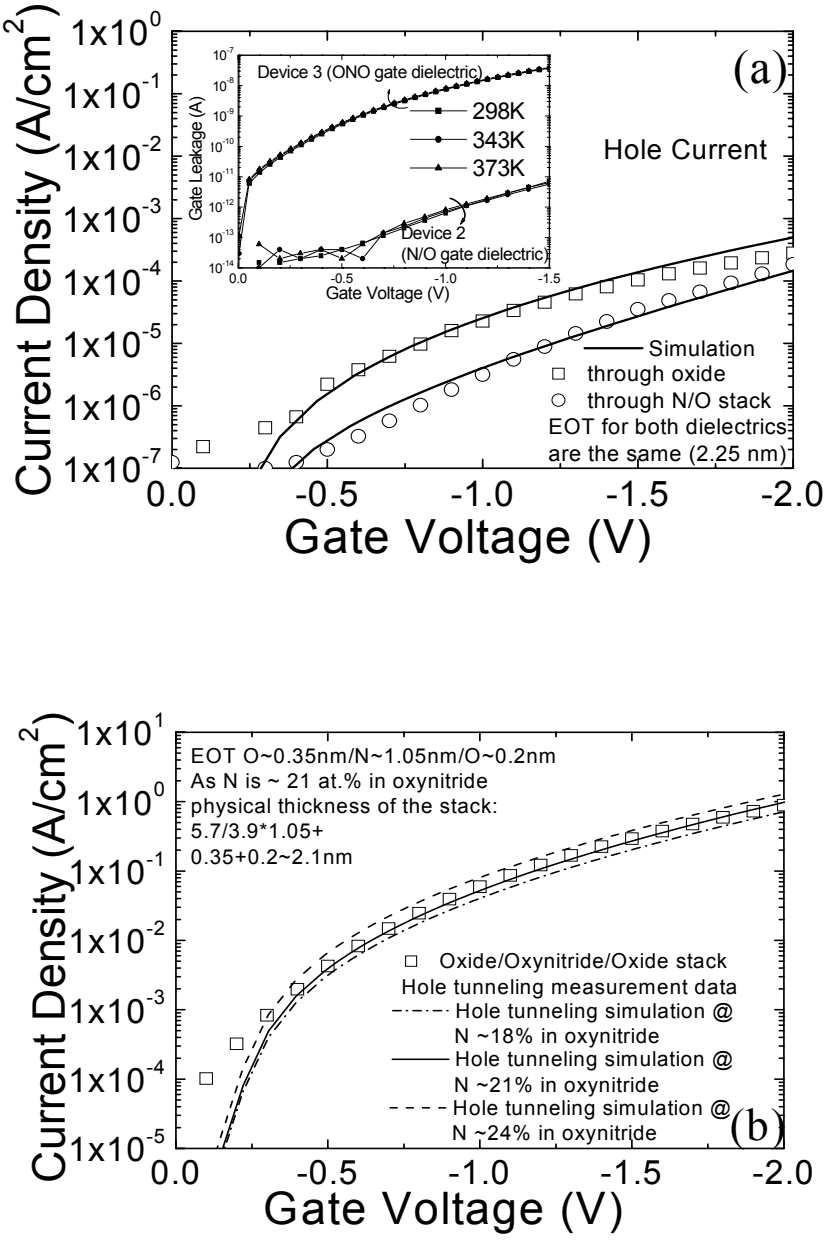

Fig. 5.15. Comparison of simulated (line) and measured (symbol) hole tunneling current through (a) oxide and oxynitride/oxide stack gate dielectrics in *p*-MOSFETs at EOT = 2.25 nm. Inset of Fig. 5.15a: negligible change of gate leakage through N/O (device 2) and ONO (device 3) with temperature up to 100 °C, indicating that the trap assisted tunneling mechanism such as Frenkel-Poole hopping can be neglected in hole leakage current in our oxynitride samples. (b) oxide/oxynitride/oxide stack gate dielectric in a p-MOSFET at EOT = 1.6 nm for various N concentrations in the oxynitride layer. In the simulation, $0.41m_0$ is used as the hole effective mass in both oxide and oxynitride [8].

The good agreement between the simulated and measured results for all the four device types as shown in Figs. 5.14 and 5.15 therefore corroborates the validity of the physical model.

5.4.2 Prediction of Optimum Nitrogen Concentration for Minimum Hole Tunneling Current for p-MOSFET's

Using this model, the variation of hole tunneling current with N concentration in an oxynitride gate dielectric is investigated. Fig. 5.16a shows the simulated *I-V* characteristics at various N concentration for an oxynitride gate dielectric with EOT = 2.25 nm. Fig. 5.16b shows the simulated hole tunneling current at $V_g = -1$ V as a function of film composition for an oxynitride gate dielectric with various EOT. It can be readily seen that when $|Vg| < 2$ V, the hole tunneling current through an oxynitride film with 33 at. % N is the smallest. This may be attributable to the competitive effects of the increase in actual thickness and decrease in hole barrier height with N concentration in an oxynitride film at a given EOT. In contrary, the electron tunneling current decreases monotonically with N concentration in an oxynitride film [6], which may be attributable to the smaller decrease in the electron barrier height with N concentration.

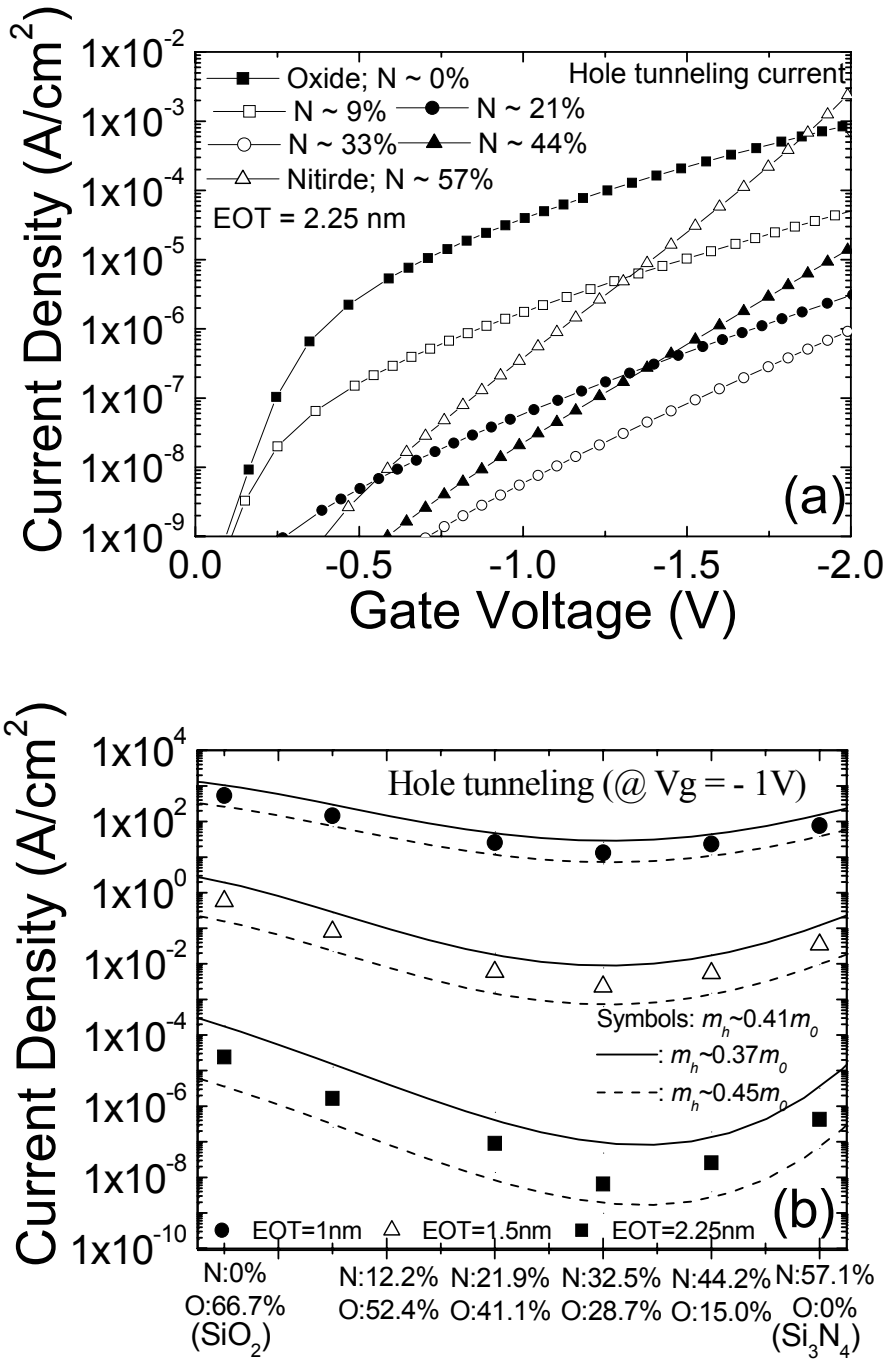

Fig. 5.16. (a) Simulated hole tunneling current through oxynitride gate dielectric in a p-MOSFET at EOT = 2.25 nm for various N concentrations in the dielectric. (b) Simulated hole tunneling current through oxynitride gate dielectric in a p-MOSFET at V_g = – 1 V for various EOT and N concentrations in the dielectric. The effect of +/- 10% variation of oxynitride hole effective mass value (0.41m_0) [8] on hole tunneling current is demonstrated in this figure (solid and dashed lines). Hole tunneling current is lowest through the oxynitride with ~33 at. % of N for all of the cases.

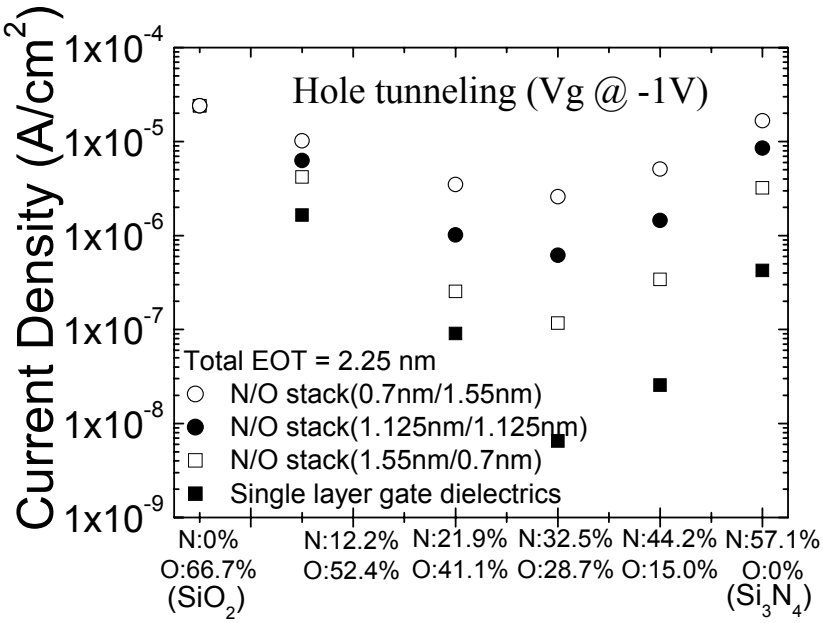

Fig. 5.17. Simulated hole tunneling current through oxynitride/oxide stack gate dielectric in a *p*-MOSFET at $V_G = -1.0$ V and EOT = 2.25 nm for various combinations of oxynitride and oxide thicknesses, and N concentrations in the oxynitride layer. (EOT of oxynitride /EOT of oxide data are given in the brackets.)

Fig. 5.17 shows the simulated hole tunneling current at $V_g = -1$ V as a function of film composition for an N/O stack film with EOT = 2.25 nm but formed by various oxynitride and oxide thicknesses. It can be readily seen that the hole tunneling current decreases monotonically with an increase in the oxynitride thickness when the N concentration in the oxynitride layer is kept constant. Furthermore the minimum hole tunneling current through an N/O stack film is again obtainable at 33 at. % N.

5.4.3 Projection of Scaling Limits of N/O Gate Dielectrics Used in MOSFET's

The interface state density at an oxynitride/Si interface is higher than that at an oxide/Si interface and the presence of N at a dielectric/Si interface degrades the peak channel mobility, which explains the rationale behind the N/O stack scheme for gate dielectrics [29,30]. Together with our results, we propose N/O stack gate dielectric being made up by an oxynitride layer with 33 at. %. N and an interfacial oxide layer. Fig. 5.18 shows the gate leakage current as a function of EOT at various operating voltages for proposed N/O stack with the oxide layer of different thickness. As expected, the gate leakage decreases with the oxide interfacial layer thickness at a gate voltage of –1.2 V. Therefore, an optimized N/O stack is suggested to consist of an oxide layer with a minimum thickness of 3 Å. Our calculation further indicates that under low gate biases ($|V_g|$<2V), for the same total EOT, the electron current through this optimized N/O stack in *n*-MOSFET is lower than the hole current in *p*-MOSFET, indicating that the EOT scaling for this stack is determined by the hole tunneling current in *p*-MOSFET. As a result, we can project the EOT scaling limit of the N/O gate stack dielectrics used in MOSFET's. It can be seen from Fig. 5.18 that at an operating voltage of –0.9 V applicable to the 0.65 μm technology node that is projected to be realizable by 2008 [35], the optimized stack structure could be scaled to EOT = 1.2 nm if the maximum tolerable gate leakage current is 1 A/cm^2 [31,32] and EOT = 0.9 nm if the maximum tolerable gate leakage current is 100 A/cm^2 [33,34].

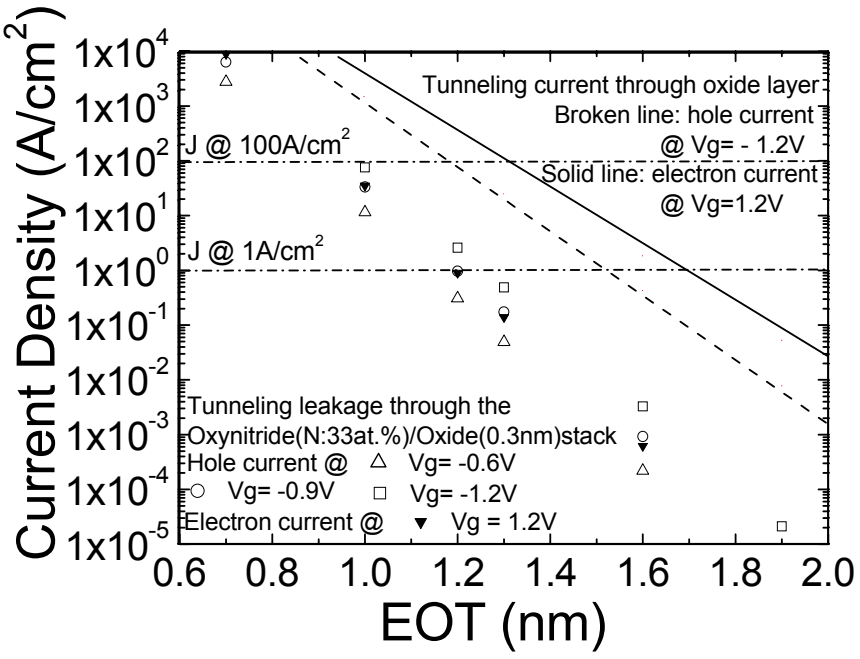

Fig. 5.18. Relationship between gate leakage currents (hole tunneling for *p*-MOSFET @ – 0.6V [open triangles], – 0.9V [open circles], – 1.2V [open squares] and electron tunneling for *n*-MOSFET @ 1.2V [solid triangles]) and total EOT of the optimized N/O stack. For same EOT and same absolute value of gate voltage (1.2 V), the electron current in *n*-MOSFET is lower than the hole current in *p*-MOSFET, which indicates that the EOT scaling for this optimized N/O stack is determined by the hole tunneling current in *p*-MOSFET, not by electron tunneling current in *n*-MOSFET. Also shown are the gate leakage currents through pure oxide layer (hole tunneling in *p*-MOSFET @ – 1.2V [dashed line], and electron tunneling in *n*-MOSFET @ 1.2V [solid line] for different EOT. The critical dashed line @ J = 1 A/cm^2 [14,15] suggests that the minimum EOT of this N/O stack structure used in MOSFET's is around 1.2 nm at a projected gate voltage of – 0.9V.

5.5 Conclusions

The systematic investigation of hole tunneling current through ultrathin oxide, oxynitride, oxynitride/oxide (N/O) and oxide/oxynitride/oxide (ONO) gate dielectrics in *p*-metal-oxide-semiconductor field effect transistors (*p*-MOSFET's) using a physical model is reported for the first time. The validity of the model is corroborated

by the good agreement between the simulated and experimental results. Under typical inversion biases ($|V_g|< 2$ V), hole tunneling current is lower through oxynitride and oxynitride/oxide with about 33 at. % N than through pure oxide and nitride gate dielectrics. This is attributed to the competitive effects of the increase in the dielectric constant, and hence dielectric thickness, and decrease in the hole barrier height at the dielectric/Si interface with increasing with N concentration for a given electrical oxide thickness. For a N/O stack film with the same N concentration in the oxynitride, the hole tunneling current decreases monotonically with oxynitride thickness under the typical inversion biases. For minimum gate leakage current and maintaining an acceptable dielectric/Si interfacial quality, an N/O stack structure consisting of an oxynitride layer with 33 at. % N and a 3 Å oxide layer is proposed. For a *p*-MOSFET at an operating voltage of –0.9 V, which is applicable to the 0.65 μm technology node, this structure could be scaled to EOT = 12 Å if the maximum allowed gate leakage current is 1 A/cm^2 and EOT = 9 Å if the maximum allowed gate leakage current is 100 A/cm^2.

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Chapter 6

Conclusion and Recommendations

6.1 Conclusion Remarks

6.1.1 Material Characterization of ALD $(HfO_2)_x(Al_2O_3)_{1-x}$ High-K Dielectric

HfO_2 has emerged as one of the most promising high-K candidates. However, it may suffer re-crystallization at high temperature during post deposition annealing (PDA), which in turn, may induce higher leakage current and severe boron penetration issues. More importantly, HfO_2 is transparent to the oxygen diffusion at high temperature. Uncontrolled low-K interfacial layers (either SiO_x or SiO_x– containing layer) will grow during HfO_2 annealing in an oxygen-rich ambient, posing a concern to EOT scalability for HfO_2 gate dielectrics. Al has been proposed to alloy HfO_2 to raise its dielectric crystallization temperature and improve its thermal stability.

In this thesis, we characterize the material properties of $(HfO_2)_x(Al_2O_3)_{1-x}$ deposited by ALD.

(a) The energy gap E_g of $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset ΔE_v, and the conduction band offset ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100)Si substrate were studied as functions of HfO_2 mole fraction x based on XPS measurement. It is shown that Al 2*p*, Hf 4*f*, O 1*s* core levels high resolution XPS spectra, valence band spectra, and O 1*s* energy loss spectra all show continuous changes with x in $(HfO_2)_x(Al_2O_3)_{1-x}$. These data are used to estimate E_g for $(HfO_2)_x(Al_2O_3)_{1-x}$, ΔE_v and ΔE_c between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the (100) Si substrate. These information are of vital importance in assessing $(HfO_2)_x(Al_2O_3)_{1-x}$ as a promising high K gate dielectric in future CMOS device technology.

(b) The thermal stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ and its impact on oxygen diffusivity through Hf aluminates were studied by XPS, XRD and TEM. It is demonstrated that the resistance to the oxygen diffusion in HfO_2 films can be greatly enhanced by the incorporation of Al. This observation is explained by (i) Al_2O_3 has much lower oxygen diffusion coefficient than HfO_2 at high temperature; (ii) doping HfO_2 by Al raises the film crystallization temperature of HfO_2 and thus drastically reduces the oxygen diffusion along the grain boundaries during annealing.

6.1.2 Thermally Robust HfN Metal Gate Electrode

Refractory metal nitrides such as TiN and TaN have been studied extensively as potential gate electrode candidates, however, these materials showed limited

thermal stability. Due to the negatively larger heat of formation of HfN (also known as the most refractory metal nitride) compared to that of TiN and TaN, HfN is expected to possess better thermal stability with underlying gate dielectrics than TaN and TiN.

In this thesis, a systematic study on the novel HfN metal gate applications is presented. For both conventional SiO_2 dielectrics and HfO_2 high-K gate dielectrics,

(a) HfN metal possesses a mid-gap work function.

(b) HfN exhibits robust resistance against high temperature treatments (up to 1000°C) in terms of EOT, work function, and leakage current stability. This superior electrical stability is attributed to the excellent oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 and HfN/SiO_2 interface.

(c) For MOS capacitors, the HfN/HfO_2 gate stack's EOT is scaled down to less than 1nm even upon 1000^{o}C post metal annealing, showing excellent leakage, boron penetration immunity, and long-term reliability. This encouraging result is demonstrated without using a surface nitridation before high-K deposition.

(d) For n-MOSFETs with HfN/HfO_2 gate stack, the mobility is improved without surface nitridation while achieving excellent EOT.

(e) It is proposed that HfN is a promising gate electrode candidate for the FD-SOI and/or the SDG MOS devices applications where a mid-gap metal gate electrode is desired.

6.1.3 Metal Gate Work Function Thermal Stability

Integrating metal gates in a conventional approach is very attractive to realize metal gates in a manufacturable process. This would require the gate-stack (the metal gate and the gate dielectric) to undergo high temperature S/D annealing process. Different research groups (from both academic and industry) have reported that the metal gate work function Φ_m is dependent on fabrication process conditions (or different annealing process). Therefore, the factors controlling Φ_m thermal instability are critically important and must be clearly understood.

In this thesis, the new experimental findings on the dependence of Φ_m on the underlying gate dielectric materials and process temperature is reported, and a model is proposed to explain the phenomenon of process-induced Φ_m thermal instability. This metal-dielectric interface model takes the role of *extrinsic states* into account. High temperature annealing could lead to the creation of *extrinsic states*, and hence the interface dipole, at the metal-dielectric interface, resulting in metal Fermi level pinning. Interface dipole formation plays an important role in determining the amount of Fermi pinning and hence the threshold voltage of metal gate transistors. Generally, the generation of *extrinsic* states upon annealing is less significant for metal gates on HfO_2 compared to metal gates on SiO_2.

6.1.4 Direct Hole Tunneling Current Study through Ultrathin Oxynitride/Oxide Stack Gate Dielectrics

ITRS predicts that the high-K gate dielectrics might be used for the mass production as early as in the year of 2005. Before that, silicon oxynitride dielectrics would dominate as the alternative to pure oxide until the 65-nm technology node.

It has been demonstrated that hole tunneling would dominate the gate leakage current in a *p*-MOSFET if its gate dielectric is formed by an oxynitride/oxide stack under typical gate inversion biases ($|V_g| < 1.7$ V). It is also noteworthy that under such gate biases and if the gate dielectric made of nitride, gate leakage in a *p*-MOSFET (hole tunneling current dominates) becomes higher than that in a n-MOSFET (electron tunneling current dominates). Therefore the scaling limit of nitride gate dielectric will probably be determined by the gate leakage in a *p*-MOSFET.

In this thesis, a systematic investigation of hole tunneling current through ultrathin oxide, oxynitride, and oxynitride/oxide (N/O) gate dielectrics in *p*-MOSFET's is performed using a physical model.

(a) For an N/O stack film with the same N concentration in the oxynitride, the hole tunneling current decreases monotonically with oxynitride thickness under the typical inversion biases.

(b) The N concentration in oxynitride and N/O stack films that results in the lowest gate leakage current is obtained theoretically. Under typical inversion

biases ($|V_g|$< 2 V), it is found that hole tunneling current is minimal through oxynitride and N/O with about 33 at. % N, while not through pure nitride gate dielectrics, as commonly believed. This is a result from the compromise between the increase in the dielectric constant and decrease in the hole barrier height at the dielectric/Si interface.

(c) The theoretical scaling limit of the N/O stack gate dielectric in p-MOSFET's is projected. For minimum gate leakage current and maintaining an acceptable dielectric/Si interfacial quality, an N/O stack structure consisting of an oxynitride layer with 33 at. % N and a 3 Å oxide layer is proposed. For a p-MOSFET at an operating voltage of –0.9 V, which is applicable to the 0.65 μm technology node, this structure could be scaled to EOT = 12 Å if the maximum allowed gate leakage current is 1 A/cm^2 and EOT = 9 Å if the maximum allowed gate leakage current is 100 A/cm^2.

6.2 Recommendations for Future Work

As a result of increasing research in this area, the gate-dielectrics candidates are narrowing down to hafnium-based system. It is suggested further studies on high-K field should center on the hafnium-based dielectrics.

Numerous detrimental effects observed in high-K transistors, such as mobility degradation, and BTI reliability might correlate with the charge trapping or fixed

charges within the high-K materials. It will be interesting to investigate the physical or chemical source of the traps, in order to improve the high-K quality.

Mobility is a key parameter determining a number of transistor metrics, such as drive current, speed, threshold voltage, transconductance, and sub-threshold swing. It is desired to maintain the mobility of the transistors with high-K dielectrics close to that of the SiO_2 system. To fulfill this goal, it is desirable to integrate novel channel materials such as Ge, strain-Si, or strain-Ge, with the high-K gate dielectric. Such devices using novel channel materials with the ultra-thin high-K dielectric (EOT < 1nm) need to be demonstrated, and the electrical performance, especially the carrier mobility, need to be evaluated.

Metal gate electrodes will be required for sub-65 nm CMOS technology. Efforts should be continued to identify the suitable metal gate materials with suitable work functions and with sufficient chemical stability for dual-gate CMOS devices. It is also a challengeable task to find a simple and cost effective way to integrate the metal gates into the conventional CMOS technology.

In the chapter 4 of this thesis, a metal-dielectric interface model taking the role of extrinsic states into account has been proposed to qualitatively explain the work function thermal instability. The possible source of the extrinsic states might be oxygen-related vacancies, nitrogen-related vacancies, or metal-Si bonding defects. The extrinsic states density level (or interfacial bonding defects) would be $<10^{16}$-10^{18} cm^{-3} if considering the distance of interface dipole induced by extrinsic states is less than several Å. This level is beyond the limitation of the analyzing limitation of the conventional physical analytical tool such as XPS, AES, or SIMS. However, it would

still be very interested to investigate the exact source of the extrinsic states at the metal/dielectric interface in order to control the process-induced metal gate work function variation. The atomistic simulation needs to be performed to identify the source of the extrinsic states.

The electrical reliability of a new material (either a gate dielectric or a gate electrode) needs be clearly understood for its application in CMOS technology. For the devices with metal gate electrodes, new reliability issues might arise due to the possible diffusion of metal atoms into the dielectric or the channel region. For the same dielectric (such as SiO_2), comparison reliability study (such as TDDB, SILC, and plasma introduced damage *PID*) needs to be conducted between the devices with poly-Si gate electrode and that with metal gate electrode.

In a wider scope beyond the gate stacks, the scalability of the planar CMOS devices will reach a fundamental limit somewhere down the technology roadmap. Therefore novel structures and technologies, such as multi-gate devices with high-K/metal gate stack need to be investigated.

List of Publications

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