

DESIGN OF HIGH SPEED 1:4 DEMULTIPLEXER FOR OPTICAL COMMUNICATION SYSTEMS

SUN PIN PING

(B.S., Fudan University)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2004

ACKNOWLEDGMENTS

I wish to express sincere appreciation to my supervisors, Associate Professor Lian Yong of National University of Singapore (NUS) and Dr. Aruna B.Ajjikutira of Institute of Microelectronics, Singapore (IME), for their valuable guidance and helpful suggestions in all aspects of my research works from the beginning to the end. Without their guidance and support, the project would not have been a success.

I would like to thank IME for allowing me to be a part of Optical Network Focused Interest Group (ONFIG), so that I could carry out some research work at the forefront of optical transmission system technology.

Finally, I would like to thank all the staff of IME's Department of VLSI Design and Test. In my design and measurement efforts, I received many valuable suggestions from them.

CONTENTS

ACKNOWLEDGMENTS	i
SUMMARY	v
LIST OF FIGURES	vi
LIST OF TABLES	x
LIST OF SYMBOLS AND ABBREVIATIONS	xi
CHAPTER 1 INTRODUCTION	1
1.1 Background	1
1.2 Literature Review	3
1.3 Contributions	8
1.4 Thesis Organization	9
CHAPTER 2 DEMUX DESIGN	10
2.1 Theory of Operation	10
2.2 Design Considerations	11
2.2.1 Logic Style used in CMOS 1:4 DEMUX	12
2.2.2 Logic Style used in BiCMOS 1:4 DEMUX	16
CHAPTER 3 CIRCUIT DESIGN AND SIMULATION IN 0.18- μm CMOS TECHNOLOGY	19
3.1 Introduction	19
3.2 MCML 1:2 DEMUX Cell	20
3.3 MCML to CMOS Converter	25
3.4 DCVSL 1:2 DEMUX Cell	27
3.5 Buffers	30
3.5.1 Internal Buffers	30
3.5.2 Input Buffer	32
3.5.3 Output Buffer	32
3.6 Simulation Results	33
3.6.1 Operation at 2.5 Gbps	33
3.6.2 Operation at 2.8 Gbps	36
3.6.3 Explanation of Graphs	37
3.6.4 Summary of Simulation Results	37
CHAPTER 4 CIRCUIT DESIGN AND SIMULATION IN 0.25- μm SiGe:C BICMOS TECHNOLOGY	41
4.1 Introduction	41
4.2 High-speed ECL DFF	42
4.3 Input and Output Buffers	46

4.4 Simulation Results	48
4.4.1 Operation at 10 Gbps	48
4.4.2 Operation at 12 Gbps	51
4.4.3 Summary of Simulation Results	52
CHAPTER 5 LAYOUT DESIGN	54
5.1 Introduction	54
5.2 Layout Techniques	54
5.2.1 Multifinger Transistors	55
5.2.2 Matching of Transistors and Resistors	55
5.2.3 Interconnects	57
5.2.4 Using of guard rings	59
5.2.5 Symmetry	60
5.2.6 Reducing the Power Line Noise	60
5.2.7 Impedance Matching	62
5.2.8 Pad, Bond Wire and Package	63
5.3 Layout	65
CHAPTER 6 MEASUREMENTS	68
6.1 Introduction	68
6.2 PCB Design	68
6.3 Measurement Set-up	69
6.4 Measurement Results	70
6.4.1 The Measurement Results of 2.5 Gbps DEMUX chip	71
6.4.2 The Measurement Results of 10 Gbps DEMUX chip	75
6.5 Comparison of Simulated values with Measurement Results	81
CHAPTER 7 IMPROVEMENT OF 10 Gbps 1:4 DEMUX 0.25- μm SiGe:C BICMOS TECHNOLOGY	83
7.1 Introduction	83
7.2 Modification	84
7.2.1 Removing the Test Pads	84
7.2.2 Removing the Ripples on the Eye-diagram	84
7.2.3 Internal Buffers	85
7.2.4 Improvement on Output Buffer	86
7.3 Simulation Results of Modified Design	87
7.3.1 Operation at 10 Gbps	88
7.3.2 Operation at 12 Gbps	91
7.3.3 Explanation of Graphs	92
7.3.4 Summary of Simulation Results	92
7.4 Layout of Improved 10 Gbps 1:4 DEMUX	93
CHAPTER 8 CONCLUSION	94
8.1 Conclusion	94

8.2 Future Work	95
REFERENCES	98
APPENDIX A Chip microphotograph of 2.5 Gbps DEMUX	100
APPENDIX B PCB photograph of 2.5 Gbps DEMUX	101
APPENDIX C Chip microphotograph of 10 Gbps DEMUX	102
APPENDIX D PCB photograph of 10 Gbps DEMUX	103

SYMMARY

A 2.5 Gbps 1:4 Demultiplexer (DEMUX) realized using standard 0.18- μm CMOS technology and a 10 Gbps 1:4 DEMUX realized in 0.25- μm SiGe:C BiCMOS technology have been presented in this report.

The 2.5 Gbps DEMUX is designed for SONET OC-48 systems. To meet the speed requirement with minimal power consumption, MOS current mode circuits are used in the first-stage 2.5 Gbps 1:2 DEMUX, while the two second-stage 1:2 DEMUXs working at the 1.25 Gbps is implemented in differential cascade voltage switch logic (DCVSL). Measurement results show that the designed DEMUX is able to operate in the frequency range from 1 – 2.5 GHz with a large phase margin, and consumes 137 mA from a 2.08V power supply. The layout area is $945\mu\text{m} * 1185\mu\text{m}$.

The 10 Gbps DEMUX's is developed for the SONET OC-192 system. A two-level series gating differential emitter-coupled logic (ECL) is used in the design of the high-speed D-flip-flops. The circuit operates from a single 2.5-V supply and consumes 110 mA (including 50Ω buffers). The active area is $838\mu\text{m} * 830\mu\text{m}$.

LIST OF FIGURES

Fig. 1.1 The block diagram of optical fiber communication system	3
Fig. 1.2 Shift- register type DEMUX	4
Fig. 1.3 Tree- type DEMUX	5
Fig. 1.4 Schematic of the feedback MCML latch	7
Fig. 2.1 Block diagram of 1:4 DEMUX	10
Fig. 2.2 Block diagram of 1:2 DEMUX Cell	11
Fig. 2.3 Timing chart	11
Fig. 2.4 MCML inverter	12
Fig. 2.5 DCVS structure	15
Fig. 2.6 Differential ECL buffer	17
Fig. 3.1 Schematic of the MSC latch	20
Fig. 3.2 Schematic of the MCML latch	21
Fig. 3.3 Schematic of MCML to CMOS converter	25
Fig. 3.4 Dynamic differential buffer	28
Fig. 3.5 Inverter	30
Fig. 3.6 A 4-stage inverter buffer	31
Fig. 3.7 Tandem output buffer	32
Fig. 3.8 Output waveform of 1:4 DEMUX at 2.5 Gbps (typical case)	33
Fig. 3.9 Output waveform of msm-DFF at 2.5 Gbps (typical case)	34
Fig. 3.10 Output waveform of ms-DFF at 2.5 Gbps (typical case)	34
Fig. 3.11 Output waveform of clock-divider at 2.5 Gbps (typical case)	35

Fig. 3.12 Output waveform of 1:4 DEMUX at 2.5 Gbps (worst case)	35
Fig. 3.13 Output waveform of 1:4 DEMUX at 2.5 Gbps (best case)	36
Fig. 3.14 Output waveform of clock-divider at 2.8 Gbps (typical case)	36
Fig. 3.15 Operation of the 1:4 DEMUX	37
Fig. 3.16 Simple two-transistor current mirror where the input current is set by the supply voltage and a resistor using MOS transistor	39
Fig. 4.1 High-speed ECL DFF	43
Fig. 4.2 Schematic of ECL latch	44
Fig. 4.3 Data input buffer	47
Fig. 4.4 Clock input buffer	47
Fig. 4.5 Output buffer	47
Fig. 4.6 Output waveform of 1:4 DEMUX at 10 Gbps (typical case)	49
Fig. 4.7 Output waveform of msm-DFF at 10 Gbps (worst case)	49
Fig. 4.8 Output waveform of ms-DFF at 10 Gbps (best case)	50
Fig. 4.9 Output waveform of clock-divider at 10 GHz (typical case)	50
Fig. 4.10 Output waveform of 1:4 DEMUX at 10 Gbps (worst case)	51
Fig. 4.11 Output waveform of 1:4 DEMUX at 10 Gbps (worst case)	51
Fig. 4.12 Output waveform of 1:4 DEMUX at 12 Gbps (typical case)	52
Fig. 5.1 Complex interconnect structure	58
Fig. 5.2 Phase margin reduction	60
Fig. 5.3 Ring connection	61
Fig. 5.4 Star connection	62

Fig. 5.5 Buffers and transmission lines for impedance matching	63
Fig. 5.6 Simulation setup considering DC block, bond wire and pad's resistance, capacitance and inductance	65
Fig. 5.7 Layout of 2.5Gbps 1:4 DEMUX in 0.18- μ m CMOS technology	66
Fig. 5.8 Layout of 10Gbps 1:4 DEMUX in 0.25- μ m SiGe:C BiCMOS technology	67
Fig. 6.1 Measurement set-up	70
Fig. 6.2 Pertaining to phase margin definition	71
Fig. 6.3 Output waveform of 1:4 DEMUX's Q1 and Q2 at 2.5 Gbps (Input pattern is 0011 0011 0011 0011)	72
Fig. 6.4 Output waveform of 1:4 DEMUX's Q3 and Q4 at 2.5 Gbps (Input pattern is 0011 0011 0011 0011)	72
Fig. 6.5 Output waveform of 1:4 DEMUX's Q1 and Q2 at 2.5 Gbps (Input pattern is 1010 1010 1010 1010)	73
Fig. 6.6 Output waveform of 1:4 DEMUX's Q3 and Q4 at 2.5 Gbps (Input pattern is 1010 1010 1010 1010)	73
Fig. 6.7 Output waveform of 1:4 DEMUX's Q1 eye-diagram at 2.5 Gbps	72
Fig. 6.8 Measurement set-up for the two-chip opto-electronic receiver solution	74
Fig. 6.9 Output waveform of 1:4 DEMUX's Q1 and Q2 at 10 Gbps (Input pattern is 1010 1010 1010 0000)	76
Fig. 6.10 Output waveform of 1:4 DEMUX's Q3 and Q4 at 10 Gbps (Input pattern is 1010 1010 1010 0000)	77
Fig. 6.11 Output waveform of 1:4 DEMUX's Q1 and Q2 at 10 Gbps (Input pattern	

is 1100 1100 1100 0000)	77
Fig. 6.12 Output waveform of 1:4 DEMUX's Q1 and Q2 at 10 Gbps (Input pattern	
is 1100 1100 1100 0000)	78
Fig. 6.13 Output waveform of 1:4 DEMUX's Q1 and Q2 at 10 Gbps (Input pattern	
is 0011 1100 0011 1100)	78
Fig. 6.14 Output waveform of 1:4 DEMUX's Q3 and Q4 at 10 Gbps (Input pattern	
is 0011 1100 0011 1100)	79
Fig. 6.15 Output waveform of 1:4 DEMUX's Q1 eye-diagram at 10 Gbps	79
Fig. 7.1 Internal buffers	85
Fig. 7.2 Output buffer	86
Fig. 7.3 Output waveform of improved 1:4 DEMUX at 10 Gbps (typical case)	88
Fig. 7.4 Output waveform of improved msm-DFF at 10 Gbps (typical case)	88
Fig. 7.5 Output waveform of improved ms-DFF at 10 Gbps (typical case)	89
Fig. 7.6 Output waveform of improved clock-divider at 10 GHz (typical case)	89
Fig. 7.7 Output waveform of improved 1:4 DEMUX at 10 Gbps (worst case)	90
Fig. 7.8 Output waveform of improved 1:4 DEMUX at 10 Gbps (best case)	90
Fig. 7.9 Eye-diagram of improved 1:4 DEMUX's Q1 at 10 Gbps	91
Fig. 7.10 Output waveform of improved 1:4 DEMUX at 12 Gbps (typical case)	91
Fig.7.11 Layout of improved 10Gbps1:4 DEMUX in 0.25- μ m SiGe:C BiCMOS	
technology	93

LIST OF TABLES

Table 1.1 Optical Line Rates	2
Table 3.1 Summary of 2.5 Gbps 1:4 DEMUX's simulation results at the highest input pattern (1010 1010 1010 1010)	38
Table 4.1 Summary of 10 Gbps 1:4 DEMUX's simulation results at the random input pattern	53
Table 6.1 Summary of 2.5 Gbps DEMUX's measurement results	74
Table 6.2 Summary of 10 Gbps DEMUX's measurement results	80
Table 7.1 Summary of improved 10 Gbps 1:4 DEMUX's simulation results at the random input pattern	92

LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

μ_n	Electron mobility constant
μ_p	Hole mobility constant
C_{ox}	Oxide capacitance
g_m	Transconductance
L	Length of transistor
V_{TH}	Threshold voltage
V_{GS}	Gate source voltage
V_{DS}	Drain source voltage
W	Width of transistor
k'_n	Process transconductance parameter of NMOS transistor
k'_p	Process transconductance parameter of PMOS transistor
k_n	Gain factor of NMOS transistor
k_p	Gain factor of PMOS transistor

Abbreviations

CDR	Clock and Data Recovery
CML	Current-Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DCVSL	Differential Cascode Voltage Switch Logic
DEMUX	Demultiplexer
DFF	D Flip-Flop
ECL	Emitter-coupled Logic
E ² CL	Emitter-emitter-coupled Logic
LA	Limiting Amplifier
MCML	MOS Current-Mode Logic
MOS	Metal Oxide Semiconductor
PLL	Phase-Locked Loop
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network
TIA	Transimpedance Amplifier
TTL	Transistor-Transistor Logic
TSPC	True Single-Phase Clock
VCO	Voltage-Controlled Oscillator