INTRA-LEVEL DIELECTRIC RELIABILITY IN DEEP SUB-MICRON COPPER INTERCONNECTS

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SUMMARY

As interconnects are scaled down to deep submicron regime, some of the back-end-of-line (BEOL) dielectric reliability issues such as intra-level leakage current, breakdown strength and time-dependent dielectric breakdown (TDDB) are becoming increasingly important. Assessing the BEOL dielectric reliability issues from a practical intra-level Cu capacitor structure can be quite complicated because of a convolution of many factors such as the fringing capacitances, the non-uniform distribution of electric and stress fields, the multistack dielectrics, the intrinsic BEOL dielectric material (USG and low-*k* SiOC in this thesis), the Cu drift into the dielectric as well as the interface trap density. In this research project, we conducted experiments on intra-level Cu capacitors using various surface treatments as well as different dielectric barriers to determine the origin of the leakage currents, their probable leakage pathways as well as the dielectric breakdown mechanisms.

With NH_3 and H_2 treatments, the intra-level leakage currents were improved significantly. From carrier transport modeling, it could be determined that the Poole-Frenkel (P-F) saturation effect occurs in structures treated with NH_3 and H_2 plasma. This verifies the reduction of interface trap density by the surface treatments. Moreover, from the dielectric constant values, it was deduced that the dominant leakage pathway is at the interface of BEOL dielectric (USG in this experiment) and dielectric barrier. Also, the improvement of time-dependent dielectric breakdown (TDDB) for structures with NH_3 and H_2 treatments indicates a suppression of Cu ion density which plays a dominant role in TDDB degradation mechanisms.

By varying the types of dielectric barriers used, it was shown that Cu movement into BEOL dielectric (SiOC in this experiment) can have a significant impact on dielectric breakdown mechanisms. In addition, the existence of broken bonds at the interface was found to be the major cause of high intra-level leakage current. Using the carrier transport modeling, we are able to distinguish the dominant leakage mechanisms: P-F emission in structures with SiN barrier and Schottky emission in structures with SiC barrier. The relatively high leakage current due to P-F emission implies that significant amount of incomplete covalent bonds were being formed during deposition of SiN. On the other hand, because SiC is chemically similar to SiOC, there were less broken bonds in the interface regions and as a result, the intra-level leakage current measured was comparatively low and displaying a Schottky emission characteristics. In addition, the dominant leakage pathways were found to be interface-induced for structures with SiN barrier and bulk-induced for structures with SiC barrier. From SIMS analysis of SiN and SiC dielectric materials, it was deduced that SiN has a superior barrier property against Cu diffusion. Despite giving a high leakage current, the TDDB performance of structures with SiN barrier was better. As expected, Cu drift into the low-*k* SiOC is the dominant factor in TDDB degradation mechanism.

Soft breakdown phenomenon was observed in structures with SiC barrier at relatively low electric field stress. It was observed from SEM images that permanent leakage paths were formed at the interface of SiC and low-*k* SiOC. The occurrence of soft breakdown was irregular and it poses a practical measurement problem.

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LIST OF SYMBOLS

AES	Auger Electron Spectroscopy
AHI	Anode Hole Injection
BEOL	Back-End-of-Line
BTS	Bias Temperature Stress
CMP	Chemical Mechanical Polishing
DUT	Device Under Test
ECP	Electrochemical Plating
ESL	Etch Stop Layer
F-N	Fowler-Nordheim
FTIR	Fourier Transform Infrared
IC	Integrated Circuit
IMD	Inter-Metal Dielectric
Low-*k*	Low Dielectric Constant
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Silicon
MOS	Metal Oxide Semiconductor
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
P-F	Poole-Frenkel
RC	Resistance-Capacitance
RIE	Reactive Ion Etching

SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectroscopy
TDDB	Time-Dependent Dielectric Breakdown
TEM	Transmission Electron Microscopy
ULSI	Ultra Large Scale Integration
USG	Undoped Silicate Glass

CHAPTER 1

INTRODUCTION

1.1 Background

In microelectronics industry, new materials and processes are being developed to fulfill the need for more powerful processors and memory chips. The speed of metal-oxide-semiconductor (MOS) devices is increased through the continual reduction of the minimum size of device features and development of new materials such as high dielectric constant gate dielectric, metal gate electrodes and so on. On the other hand, to obtain the full benefits from the faster device speed from the miniaturization of devices, it has become indispensable for us to connect the individual devices into circuits using advanced back-end-of-line (BEOL) technology with new interconnect materials and complex interconnect structures. However, the implementation of new interconnect materials and new fabrication processes has led to severe interconnects dielectric reliability issues.

1.2 Fundamental Interconnect Issues

In this section, we review some of the fundamental interconnect issues such as interconnect *RC* delay, the power dissipation and crosstalk.

1.2.1 Interconnect *RC* Delay

In the past, the circuit performance had been dominated by MOS device gate delay. As we progress into 0.18 μm technology node and beyond, the associated interconnect scaling has reached a point whereby the overall circuit performance will be largely constrained by interconnect *RC* delay – the product of interconnect line resistance, *R*, and the parasitic capacitance, *C*, coupling the interconnect to adjacent lines and underlying Si substrate [1]. Figure 1.1 shows the individual gate and interconnect delays (with different combinations of metal and dielectric materials) as well as the sum of gate and interconnect delays. It can be seen that although MOS transistor switches at a faster speed when the feature size is scaled down, signal propagation through interconnects (the *RC* delay) is unfortunately becoming the limiting factor in overall circuit performance which is indicated by the sum of both gate and interconnect delays.

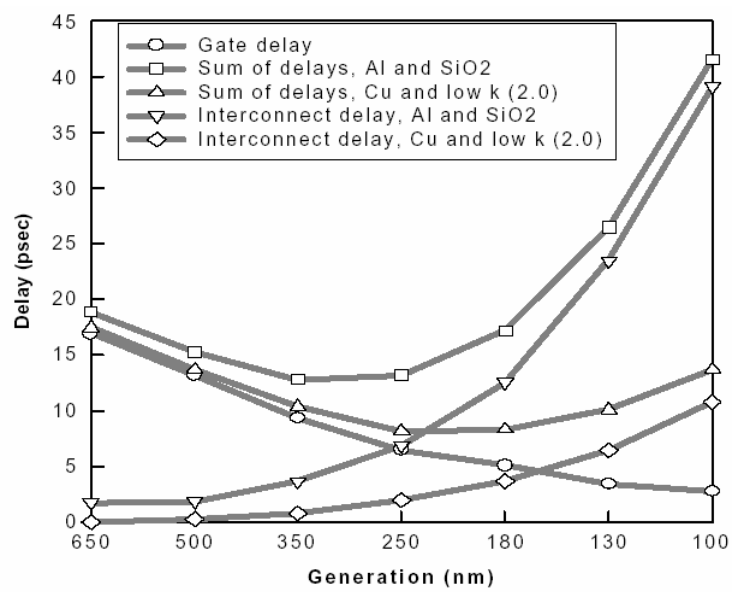

Figure 1.1: Gate and interconnect *RC* delays as a function of feature size [1].

A simple model can be used to estimate the effect of various geometries and materials on the *RC* delay [2], as shown in Figure 1.2.

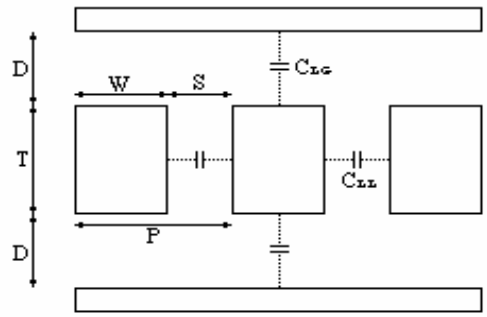

Figure 1.2: *RC* delay estimation model [2].

This model describes a set of metal lines that forms "vertical" metal-insulator-metal (MIM) capacitors as well as "lateral" intra-level comb capacitor. From Figure 1.2, W is the metal line width, T is the metal line thickness, S is the spacing between two lines, P is the metal line pitch ($P = W + S$) and D is the thickness of the BEOL dielectric between the top and bottom of the metal lines. Also, let L = length of a metal line and ρ = metal resistivity. Taking the pitch P and the metal thickness T as the basic parameters, we may set $W = aP$ and $D = bT$ where a and b are constant for a given geometry. The resistance R of a metal line is given by

$$R = \frac{\rho L}{WT} = \frac{\rho L}{aPT} \tag{1.1}$$

If the BEOL dielectric has a dielectric constant ε and the edge contributions from the metal lines and coupling of the metal line sidewalls to the ground planes are negligible, the capacitance due to "vertical" MIM capacitor is denoted as:

$$C_{LG} = \varepsilon\, \varepsilon_0 \frac{WL}{D} = \varepsilon\, \varepsilon_0 \frac{aPL}{bT} \tag{1.2}$$

and the capacitance due to "lateral" intra-level comb capacitor is denoted as:

$$C_{LL} = \varepsilon\, \varepsilon_0 \frac{TL}{S} = \varepsilon\, \varepsilon_0 \frac{TL}{P - W} = \varepsilon\, \varepsilon_0 \frac{TL}{(1 - a)P} \tag{1.3}$$

where ε_0 is the permittivity of free space. Hence the total capacitance C of a metal line formed with its surroundings can be written as

$$C = 2\,(C_{LG} + C_{LL}) = 2\,\varepsilon\varepsilon_0\, L \left[\frac{aP}{bT} + \frac{T}{(1-a)P}\right] \tag{1.4}$$

For the RC time delay,

$$RC = 2R\,(C_{LG} + C_{LL}) \tag{1.5}$$

Combining Equations (1.1), (1.4) and (1.5),

$$RC = 2\rho\, \varepsilon\varepsilon_0 L^2 \left[\frac{1}{bT^2} + \frac{1}{a(1 - a)P^2}\right] \tag{1.6}$$

Or equivalently,

$$RC = 2\rho\,\varepsilon\varepsilon_0\left(\frac{L^2}{P^2}\right)\left[\frac{P^2}{bT^2}+\frac{1}{a(1-a)}\right] \tag{1.7}$$

One may interpret Equation (1.6) in such a way that the factors $2\rho\varepsilon\varepsilon_0$ and $L^2(1/bT^2 + 1/a(1-a)P^2)$ represent the materials and architecture contributions to the interconnect time delay respectively.

If one defines the aspect ratio A of the metal lines as the ratio of line thickness to line width, $A = T / W$, or equivalently $A = T / aP$, Equation (1.7) can be expressed as

$$RC = 2\rho\,\varepsilon\varepsilon_0\left(\frac{L^2}{P^2}\right)\left[\frac{1}{a^2bA^2}+\frac{1}{a(1-a)}\right] \tag{1.8}$$

Note that in Equation (1.8) the term $1/a^2bA^2$ represents the "vertical" and the term $1/a(1-a)$ represents the "lateral" contribution to the total capacitance.

It can be concluded from Equation (1.8) that for fixed line length L and fixed aspect ratio A the RC delay increases quadratically with decreasing feature size (decreasing pitch P). In addition, Equation (1.8) implies that for $A < 1$ the inter-level ("vertical") capacitance contributes more to the RC delay than the intra-level ("lateral") capacitance, whereas the opposite is true for $A > 1$.

1.2.2 Power Dissipation

Power dissipation in integrated circuits (IC) generally consists of the two major components: static and dynamic power dissipation. The static component is basically due to the MOS transistor junction leakage while the dynamic component [3] is dominated by switching transients in digital circuits, and it can be expressed as

$$P = \frac{1}{2} f_d C V^2 f \tag{1.9}$$

where C is the total 'on-state' capacitance, V is the supply voltage, f is the operating frequency and f_d is the fraction of the gates that switch during a clock cycle. It can be easily deduced from Equation 1.9 that as the circuit switches at a higher frequency, the power dissipated will be higher. This high power dissipation in IC has resulted in more expensive packaging solution to remove the undesirable heat but another solution to high power dissipation, quite obvious, is to reduce both C and V. Hence, the implementation of low-k BEOL dielectric is one of the effective methods to reduce the power dissipation.

However, it should be noted that in the current technology node, the static power consumption which is governed by the 'off-state' leakage current is comparable with the dynamic power consumption. In the future, as 'off-state' leakage current becomes inevitably large [4], static power consumption will be dominant and as a result, implementation of low-k BEOL dielectric will probably not help in reducing total power consumption significantly.

1.2.3 Crosstalk

Crosstalk is one of the serious consequences of IC operating at very high frequencies (>100MHz). Crosstalk occurs at situation where an undesirable voltage is induced on neighboring lines by means of electromagnetic coupling at very high-frequency. This situation can be modeled as shown in Figure 1.3 [3].

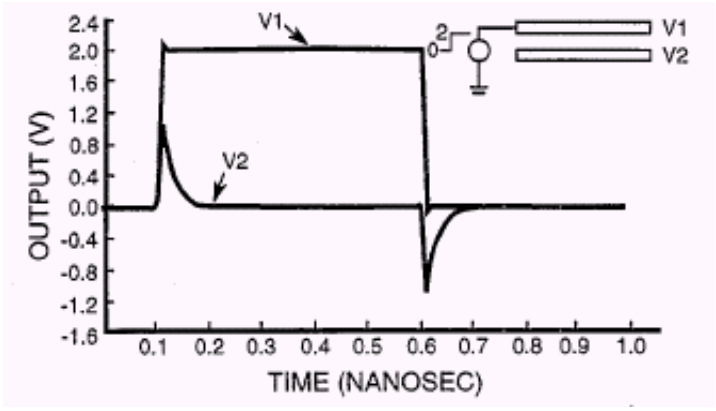

Figure 1.3: Crosstalk observed between two interconnects.
The driven line is V_1 and the crosstalk is V_2 [3].

From Figure 1.3, let us assume the driven line has a rise time pulse of 500MHz while the other line is attached to ground. During the rise and fall of the waveform on the driven line, a substantial undesirable voltage (~50% of V_1) is generated on the grounded line. The crosstalk effect will worsen as the intra-level spacing between the metal lines is reduced extensively to accommodate a larger wiring density. To minimize the crosstalk effect, the "lateral" capacitive coupling has to be reduced; and this can be again achieved by lowering the *k* value of the BEOL dielectric.

1.3 Interconnect Materials

To circumvent the limitation of *RC* delay, a more prominent interconnect scheme requiring the reduction of both metal line resistance and the capacitance of back-end-of-line (BEOL) dielectric has to be introduced and integrated into the IC fabrication process. A combination of low resistivity metal Cu and low dielectric constant (low-*k*) material has been proven to efficiently reduce the effects of some limiting factors, including *RC* time delay, power consumption and crosstalk.

1.3.1 Cu as BEOL Metal

Table 1.1: Comparison of properties of Cu and conventionally used Al.

Properties	Cu	Al
Resistivity ($\mu\ \Omega \cdot cm$)	1.67	2.66
Electromigration Resistance	Good	Poor
Melting point (^{o}C)	1085	660
Corrosion Resistance	Poor	Good
Adhesion to SiO_2	Poor	Good
Diffusion in SiO_2	High	Low
Reactive ion etching (RIE)	No	Yes

Al had been the material of choice for interconnects for many years until recently when the need to replace Al with a lower resistivity metal becomes indispensable. Only three metals Cu, Ag and Au have lower resistivity values than the conventionally used Al, however, the only practical option is Cu, in terms of costs, manufacturability and device reliability. Some of the properties of Cu and Al are summarized in Table 1.1. Besides

having a lower resistivity value, Cu also displays some excellent properties than Al in terms of electromigration resistance and melting point. Despite its virtues over Al, integrating Cu into the fabrication process is difficult because of its resistance to dry etch, ease of oxidation and corrosion, poor adhesion to dielectrics and most importantly high diffusivity in dielectrics such as SiO_2. To resolve these difficulties, damascene process has been developed of which dielectric is etched instead of Cu; The diffusion of Cu to surrounding material is prevented by encapsulating Cu completely by metal barriers such as Ta, Ti, TaN, TiN and so on, and dielectric barriers such SiN, SiC, BloK and so on. Before depositing dielectric barrier layers, Cu surface is also treated (either separately or built in with chemical mechanical polishing (CMP) process) to reduce Cu oxidation and corrosion.

1.3.2 Low-*k* material as BEOL Dielectric

Table 1.2: International Technology Roadmap for Semiconductors (ITRS) 2003 - Interconnect Dielectric Constant [4].

Year of Production	2003	2004	2005	2007	2010	2013	2016
Technology Node (nm)		90		65	45	32	22
Bulk dielectric constant	<3.0	<2.7	<2.7	<2.4	<2.1	<1.9	<1.7
Effective dielectric constant	3.3-3.6	3.1-3.6	3.1-3.6	2.7-3.0	2.3-2.6	2.0-2.4	<2.0

SiO_2 (k = 4.2) had been used as BEOL dielectric because of its low leakage, superior thermal stability and moisture resistance. However, from the International Technology

Roadmap for Semiconductors (ITRS) 2003 (Table 1.2), we could see that there is an increasing urge to use dielectric with lower and lower *k* value. In contrast to the BEOL metal, there are more choices for BEOL dielectric such as Black Diamond™ (from Applied Materials), SiLK™ (from Dow Chemical), CORAL™ (from Novellus) FLARE™ (from Allied-Signal), Aurora™ (from ASM), and many others. These low-*k* materials can generally be classified as silica-based materials and organic polymers. The deposition processes for these two materials are quite different. The silica-based dielectrics and organic polymers are deposited on the wafer by PECVD and spin-on deposition respectively. PECVD offers the advantages of being a dry process, capable of producing films with excellent uniformity and conformality while spin-on process is much like depositing photoresist in which the spin-on low-*k* precursors in its solvent form are first dispensed onto the wafer in liquid form and then cured to expel the solvent and induce polymerization and cross-linking of the structures [5]. From Table 1.2, we notice that there are two different classifications of *k* values. The bulk dielectric constant refers to the *k* value of low-*k* material which can be easily measured from metal-insulator-metal (MIM) or metal-insulator-silicon (MIS) structure while the effective dielectric constant refers to the *k* value of the integrated structure composed of low-*k* material and additional dielectric layers such as neighboring low-*k* material, the etch-stop layer (ESL) and the dielectric barriers (a simulator is needed for the complex structure).

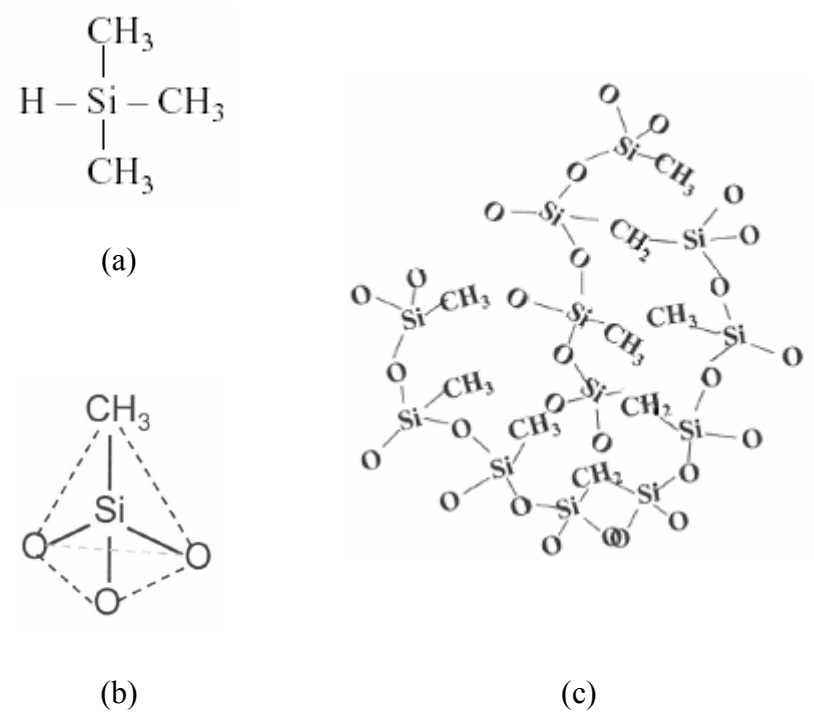

Figure 1.4: (a) The precursor: trimethysilane (3MS), (b) the basic structure and (c) the cross-linking structure of SiOC [6].

One particular silica-based material, the carbon-doped SiO_2 (SiOC) was investigated in this thesis. Figure 1.4(a) shows the precursor trimethylsilane or commonly known as 3MS which forms SiOC when reacted with a mixture of O_2 and He in PECVD chamber at 350 ºC. SiOC has a tetrahedral basic structure of SiO_2 of which one of the four O atoms is replaced by a terminating CH_3 group as shown in Figure 1.4(b) and CH_2 group to cross-link to other basic SiOC structure as shown in Figure 1.4(c). The *k* value usually measures an insulator's polarizability when exposed to an electric field. Replacing the Si-O bond with a less polarizable Si-C bond lowers the *k* value and increases the interatomic distances or porosity in the low-*k* films [6] .

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1.4 Interconnect Scaling

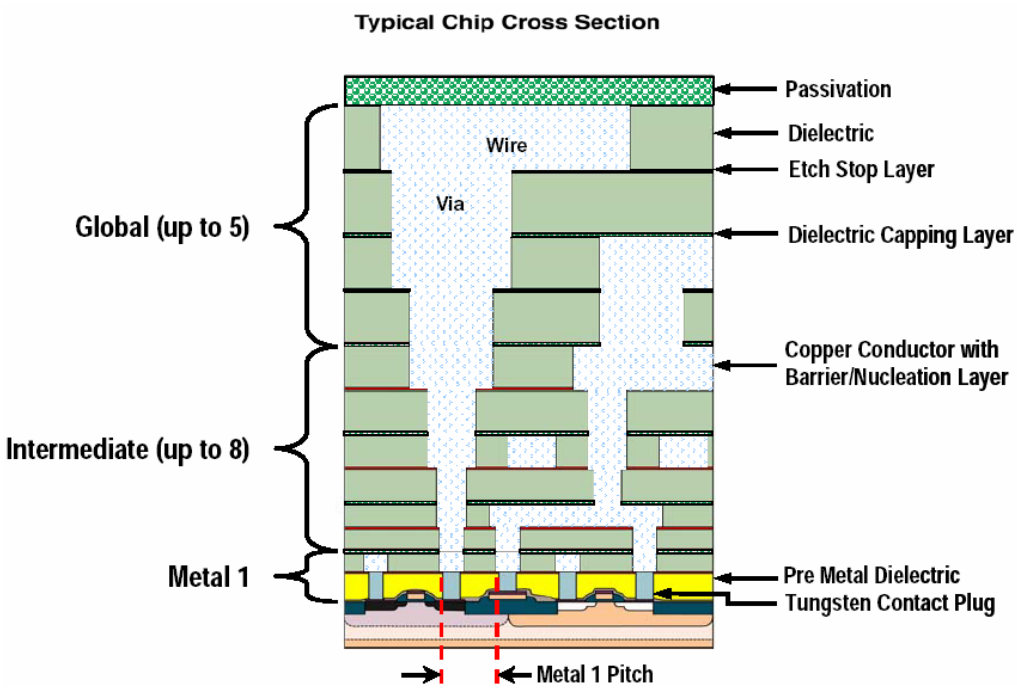


Figure 1.5: Cross-sectional diagram of a typical chip showing the classification of multi-metal layers [4].

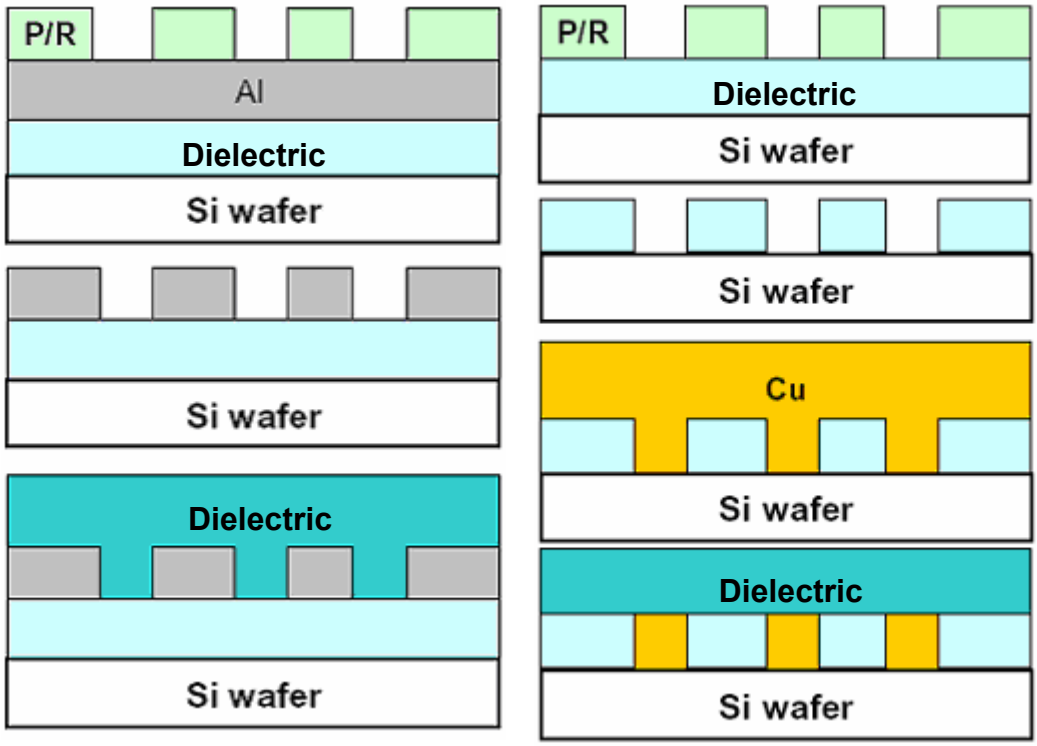
In order to accommodate the increasing transistor densities over larger chip areas, the wiring density has to be simultaneously increased by reducing interconnect wiring pitch and adding more interconnect wiring layers. Figure 1.5 shows the cross-sectional diagram of a typical chip showing the multi-stack interconnects which is generally categorized as the metal 1 interconnect, the intermediate interconnect and the global interconnect.

Table 1.3: International Technology Roadmap for Semiconductors (ITRS) 2003 - Interconnect Scaling [4].

Year of Production	2003	2004	2005	2007	2010	2013	2016
Technology Node (nm)		90		65	45	32	22
No. of metal levels	9	10	11	11	12	12	14
Metal 1 wiring pitch (nm)	240	214	190	152	108	76	54
Metal 1 aspect ratio (for Cu)	1.6	1.7	1.7	1.7	1.8	1.9	2.0
Intermediate wiring pitch (nm)	320	275	240	195	135	95	65
Intermediate aspect ratio (for Cu)	1.7	1.7	1.7	1.8	1.8	1.9	2.0
Global wiring pitch (nm)	475	410	360	290	205	140	100
Global aspect ratio (for Cu)	2.1	2.1	2.2	2.2	2.3	2.4	2.5

From the above ITRS 2003 table, as we advance into 90nm technology node and beyond, we need to achieve the requirements of reducing the wiring pitch and increasing the wiring aspect ratio. Refer to Section 1.2.1, we know that when the aspect ratio is greater than 1, the intra-level capacitance contributes more to *RC* delay than the inter-level capacitance. Hence, relative to inter-level capacitor, intra-level capacitor is prone to dielectric reliability issues such as high leakage, low breakdown strength and time-dependent dielectric breakdown (TDDB) performance. These reliability issues can be further exacerbated by the use of Cu and low-*k* materials and these will be elaborated in the following chapters.

1.5 Interconnect Damascene Process



(a) (b)

Figure 1.6: Interconnect fabrication using (a) conventional "metal" etch process (b) damascene "dielectric" etch process.

Dry reactive ion etching (RIE) had been used in metal-patterning for the interconnect fabrication. But this technique had its limitations, including non-planarity, poor coverage and most importantly difficulties in etching Cu. To overcome these limitations, a new interconnect technology - dual damascene process was developed. IBM was the first to develop and demonstrate the use of such technique for ULSI interconnect fabrication [7-8]. The name, damascene, was given because of the resemblance to ancient art of damascene for fabrication of jewelry, wherein, gold is interlaced in grooves made into

iron or wood to produce decorative designs. As shown in Figure 1.6, in contrast with the conventionally used process where interconnects are formed from patterning of metal wires by RIE, interconnects using damascene process are defined by patterning the dielectric first, followed by metal deposition and subsequent chemical mechanical planarization (CMP) for metal planarization and removal of the excess metals.

1.6 Motivation and Objectives of Project

Before the incorporation of Cu in interconnects, interconnects reliability had been dominated by electromigration and little attention was given to interconnects dielectric reliability because of their relatively large metal-to-metal spacing and low operating field (< 0.5 MV/cm). However, with interconnects wiring pitch scaling down rapidly to achieve high wiring density; and with the use of high diffusivity Cu metal and less stable low-*k* materials, some of the dielectric reliability concerns such as intra-level dielectric leakage, dielectric breakdown and TDDB lifetime failure are becoming increasingly important in interconnects reliability [9-13].

K. Maex in his recent publication [6] on the review of low-*k* dielectrics commented that the origin of the leakage currents in low-*k* materials has not been studied enough in detail and more works have to be done to analyze the conduction mechanisms and breakdown mechanisms in low-*k* dielectrics. However, besides the intrinsic low-*k* material issues, it has to be noted that the leakage current, breakdown strength and TDDB failures measured from a practical intra-level Cu capacitor structure are in fact, due to a

convolution of many factors such as Cu ion contamination, high dielectric trap density, the different dielectric layers used in multistack interconnects, fabrication process-related problems, non-uniform distribution of electric and stress fields, and so on. In order to uncover the origin of the leakage current and breakdown behaviors in intra-level Cu capacitors, it is indispensable for us to carry out a series of physical analysis to characterize and model the experimental data. With the help of these analysis, possible solutions could be designed to improve the interconnects dielectric reliability performance.

The main objectives of this research work are:

a) To fabricate intra-level Cu comb capacitor test structures using various plasma surface treatments and different dielectric barriers.
b) To assess the BEOL dielectric reliability performance by carrying out electrical tests to determine intra-level leakage current, breakdown strength and TDDB lifetime performance.
c) To analyze the experimental data and identify leakage mechanisms and leakage pathways and propose dielectric degradation models.

1.7 Organization of Thesis

This thesis is basically divided into five chapters, starting with the first chapter introducing the background of interconnect *RC* delay, interconnect materials,

interconnect scaling, a brief description of Cu damascene process as well as the motivation of the research project.

Chapter 2 will discuss the theory of some of the reliability issues such as conduction processes and time-dependent dielectric breakdown (TDDB) in insulators. In addition, some of the reported conduction mechanisms in intra-level Cu capacitors and TDDB degradation mechanisms will be reviewed.

Chapter 3 will present a detail fabrication process of the test structures: intra-level Cu comb capacitors using a damascene process. The reliability experiment approach, experiment setup and the test procedures will also be introduced.

Chapter 4 will present the experimental data collected followed by detailed discussions of the results. The effect of introducing additional surface treatments and the effect of using different dielectric barriers on interconnects dielectric reliability will be assessed. These experimental findings will be correlated to the existing degradation models and the origin of interconnects dielectric degradation will be uncovered.

Finally, in Chapter 5, the conclusion of the research project will be presented together with recommendations for further research.

CHAPTER 2

THEORY

2.1 Conduction Mechanisms in Insulators

Table 2.1: Conduction processes in insulators [9], [14].

Conduction Process	Expression	
Ohmic conduction	$J \sim E\exp(-\Delta E_{ae}/kT)$	(2.1)
Schottky emission	$J = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right]$	(2.2)
Frenkel-Poole emission	$J = C_1 E\exp\left[\frac{-q\left(\phi_t - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right]$	(2.3)
Fowler-Nordheim Tunneling	$J \sim E^{2}\exp\left[-\frac{4\sqrt{2m^{*}}(q\phi_B)^{3/2}}{3qhE}\right]$	(2.4)
Space-charge-limited conduction	$J = \frac{8\varepsilon_i \mu V^{2}}{9d^{3}}$	(2.5)
Capacitance charging current	$I = C\frac{dV}{dt}(1 - e^{-t/RC})$	(2.6)

A^{*} = effective Richardson constant, ϕ_B = Schottky barrier height, ϕ_t = Poole-Frenkel trap potential height, E = electric field, ε_i = insulator permittivity, C_1 = Poole-Frenkel pre-exponential factor, m^* = effective mass, d = insulator thickness, ΔE_{ae} = activation energy of electrons, h = Planck's constant, C = capacitance, dV/dt = voltage ramp rate, RC = characteristic capacitor charging time.

Ideally, there is no carrier conduction in an insulating film. However, practically, carrier conduction is observed when sufficiently high electric field and temperature are applied

to the insulators. The carrier characteristics in insulators vary according to many factors such as the strength of electric fields, the trap densities in the films, the barrier heights, ionic contamination and etc. Table 2.1 summarizes some of the basic conduction processes in insulators.

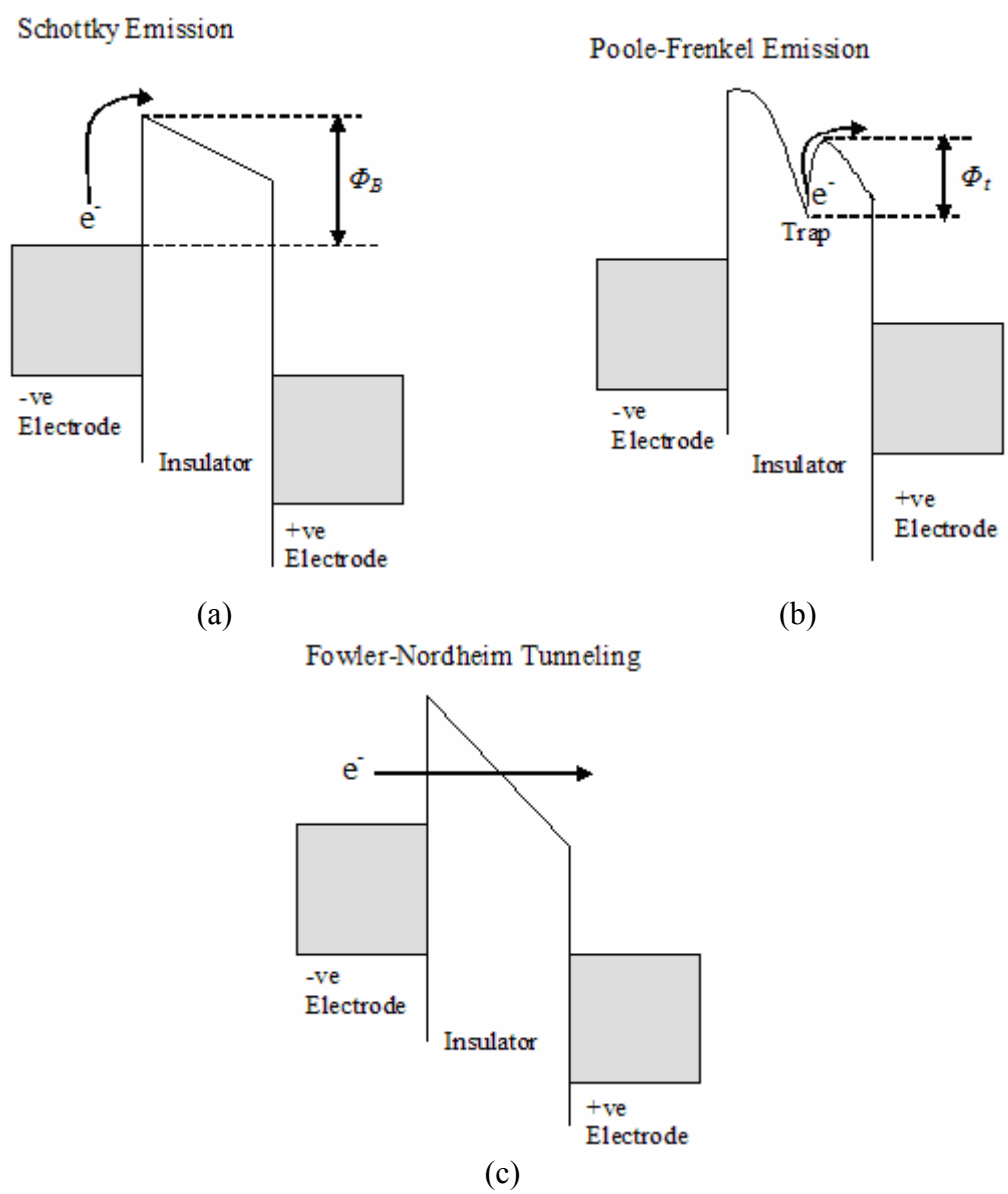


Figure 2.1: Schematic band diagram showing (a) Schottky emission, (b) Poole-Frenkel (P-F) emission and Fowler-Nordheim (F-N) tunneling.

At low applied electric fields, the leakage current is generally of Ohmic conduction characteristic and it is dependent on charged carriers such as electrons and ions in the intrinsic bulk insulators. Ohmic conduction can be easily determined by the linear fitting the graph of *log J* vs. *log E* at low initial electric field [15-16]. For large applied electric fields, determination of the leakage mechanisms through insulators are rather complex. The leakage characteristic can be due to one or more conduction processes as listed in Table 2.1. As shown in the band diagram in Figure 2.1(a), Schottky emission is basically thermionic emission across barrier height at the metal-insulator interface. Hence, Schottky emission is greatly dependent on the work function of the metal electode. To verify the existence of Schottky emission in insulators, plot of $ln(J)$ vs. $E^{1/2}$ should yield straight line with the slope corresponding to the dielectric constant of the insulator. The Poole-Frenkel (P-F) emission is due to the field-enhanced thermal excitation of trapped electrons in the insulators over the trap potential well height as depicted in Figure 2.1(b). The traps in bulk insulators can be thought as quantum-mechanical well in the forbidden energy gap having energies somewhere between the valence and conduction bands. They are generated by defects, dangling bonds, impurity atoms. The trapped electrons often reside in traps until sufficient energy is applied to excite them into the conduction band [17]. From Equations (2.2) and (2.3), the Schottky emission and P-F emission expressions are very similar. Hence, it has to be noted that conduction by P-F emission occurs only when the slope of plot of $ln(J/E)$ vs. $E^{1/2}$ matches the dielectric constant of the insulator. At very high electric field, electrons with energy less than the barrier height can tunnel through the triangular barrier as shown in Figure 2.1(c). This electron tunneling, also known as Fowler-Nordheim (F-N) tunneling depends very strongly on

electric field but independent of temperature change. F-N tunneling plays a very important role in dielectric breakdown failure. A straight line fit from graph of $ln(J/E^2)$ vs. $1/E$ shows the presence of F-N tunneling [18]. The space-charge-limited current arises when a carrier is injected into the insulator and there is no compensating charge present. The current is proportional to the square of the applied voltage [14]. The capacitance charging current is caused by the intrinsic ionic contaminants. Under an applied electric field, ions accumulate at the metal/insulator interface and effectively charging the capacitor. It is linearly dependent on the capacitance and the voltage ramp rate [9].

2.2 Conduction Mechanisms in Intra-level Cu Capacitors

The electrical characteristic in intrinsic BEOL dielectrics is one of the important factors for reliability assessment. It has to be noted that the leakage current is largely determined by the conduction mechanisms in the dielectrics. Hence, determining the conduction mechanisms could give us some insights to the origin of the leakage current (such as traps-assisted electrical transport or electron injection over the barrier height at metal/dielectric interface) and consequently provide us ideas to design solutions for suppression of leakage current. There are some papers which attempt to correlate the experimental data to some of the known conduction processes (as already introduced in Section 2.1). In this section, we will review some of their results and degradation models on conduction mechanisms in intra-level Cu capacitors.

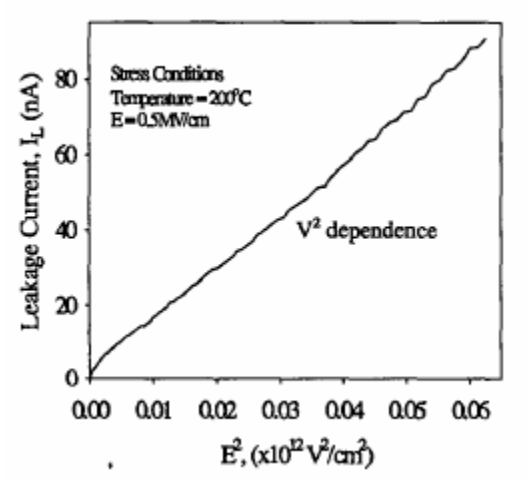


Figure 2.2: Leakage current characteristics showing V^2 dependence, indicating a space-charge-limited current mechanism [12].

Kim *et al.* [12] reported a space-charge-limited leakage current characteristic in low-*k* benzocyclobutene (BCB) dielectric after the intra-level Cu test structures were stressed at 200°C and a constant electric field of 0.5MV/cm for 10800 seconds. As shown in Figure 2.2, the leakage current measured showed a voltage square dependence which fits the space-charge-limited current expression (Equation 2.5) very well.

The origin of space-charge-limited current can be attributed to the missing or damaged barrier (Figure 2.3) during the etching of BCB film, deposition of thin Ta barrier layer or CMP process. Under an applied bias-temperature stress (BTS), Cu ions are injected from the anode through the localized surface defects to the cathode. These Cu ions accumulate at the interface near the cathode and establish two distinct electric field regions in R_1 and R_2. In R_1, the electric field is weaker due to the retarding field while in R_2 the electric field is enhanced due to the additional external applied electric field. As a result, the high electric field in R_2 lowers the cathode barrier height and electrons are easily injected into

R_1 region towards the anode and constitutes to space-charge-limited current characteristic.

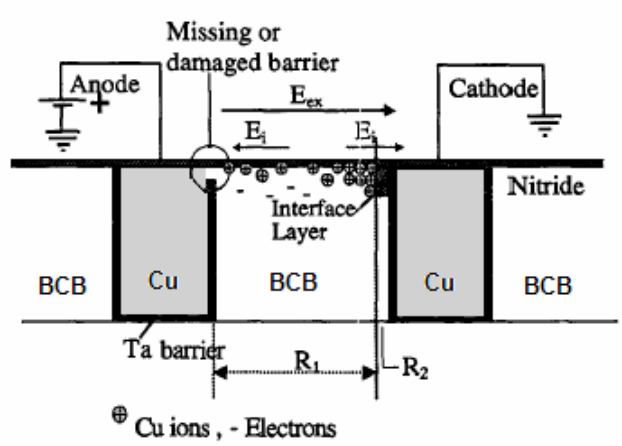


Figure 2.3: Schematic diagram showing the proposed model for bias-temperature induced leakage current degradation [9].

In another work by Bersuker *et al.* [9], similar to the previous literature, they attributed the intra-level leakage current to Cu ion contamination inherent to the low-*k* dielectric. Again, BCB was used as the BEOL dielectric. It could be observed from Figure 2.4 that at higher external voltages, the current saturated at a constant value for all temperatures at 100°C and below. The current saturation portion is typical of capacitor charging characteristic (Equation 2.6). Above 100°C, there is a significant increase in current especially when voltage was ramped above 6V.

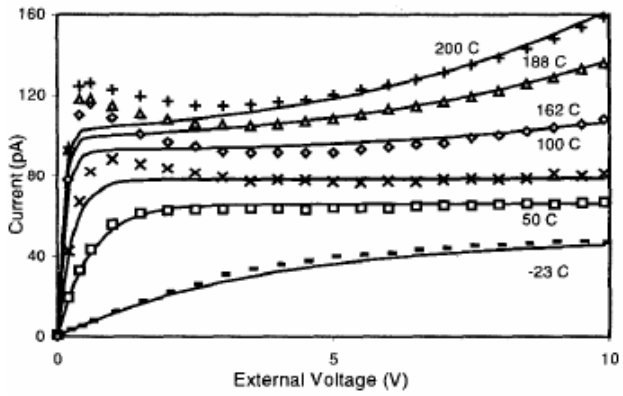


Figure 2.4: Experimental (symbols) and simulated (lines) currents. Simulated current is a sum current due to Schottky emission and capacitor charging effect [9].

The increased leakage current data showed close fit to the Schottky emission equation (Equation 2.2), indicating the presence of electron injections over the Cu/BCB barrier in addition to the Cu ions capacitance charging current (Figure 2.5). The hump shape of the measured leakage current above 100°C was attributed to a displacement current associated with the shift of chlorine ions attached to the dielectric material structure.

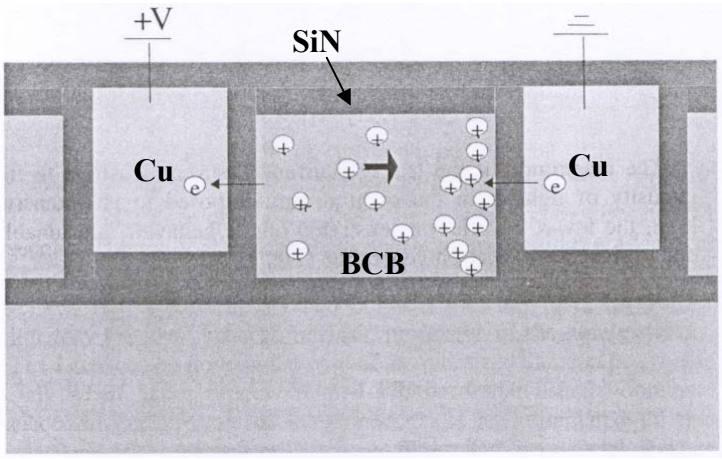
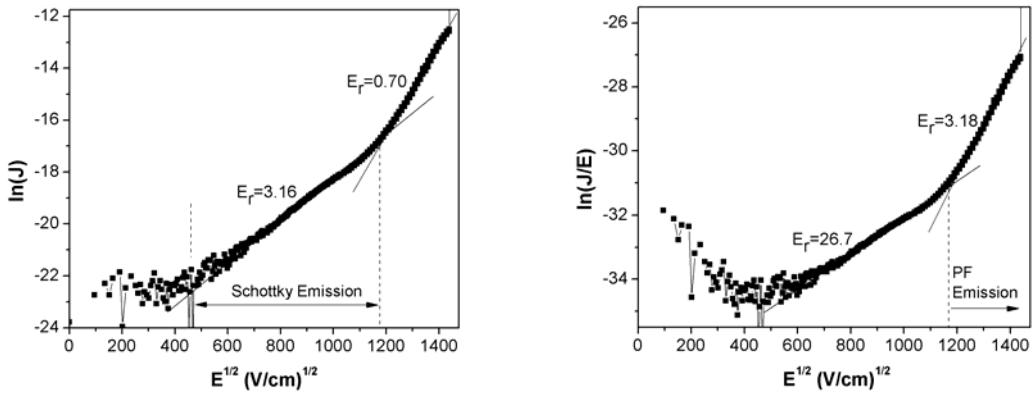


Figure 2.5: Schematic diagram showing ions and electron currents in BCB low-*k* dielectric [9].



(a) (b)

Figure 2.6: Schottky and P-F emission modelings of Cu/SiOC film [19].

For intra-level Cu capacitor using SiOC as low-*k* dielectric, different conduction mechanisms were observed at different electric field regimes [19]. In order to differentiate the different conduction mechanisms, Schottky plot of *ln(J)* vs. $E^{1/2}$ curve at low electric field (0.2MV/cm < E < 1.4MV/cm) was plotted as shown in Figure 2.6(a) and Poole-Frenkel (P-F) plot of *ln(J/E)* vs. $E^{1/2}$ at high electric (E > 1.4MV/cm) was plotted as shown in Figure 2.6(b). By comparing the dielectric constant obtained from the slopes of the curves, it could be concluded that the dominant conduction mechanism is due to Schottky emission at low electric field and P-F emission at high electric field. The presence of P-F emission suggests the existence of traps in SiOC low-*k* dielectric. This particular work differs from the others in which the reported conduction mechanism is solely due to electrons and the influence of Cu ions is negligible.

2.3 TDDB Models

Time-dependent dielectric breakdown (TDDB) is an important failure mode in deep-submicron CMOS technology. Various breakdown theories such as the linear electric field *E*-model [20-22], the reciprocal electric field (*1/E*) model [23-24], the anode hydrogen release model [25], the electron trapping model [26] were suggested to model the TDDB degradation mechanisms. The validity of these models have been controversial for many years, especially the *E* and *1/E* models of which the authors claimed are able to fit the TDDB data well over certain field ranges using the proposed modeling equations. Recent findings by McPherson *et al.* [27] and M. A. Alam *et al.* [59,60] attempted to combine both *E* and *1/E* models to explain the breakdown data over a wide range of electric field. These findings will be elaborated in Section 2.3.3.

2.3.1 Linear electric field *E*-Model

The linear electric field *E* model proposed by McPherson *et al.* [20-22], is based on electric field-induced degradation. In thermally grown SiO_2, from a molecular physics approach, the Si-O bond is a very polar bond, with a large dipole moment exists in the direction from negative oxygen ion to positive silicon ion. When an electric field is applied, it distorts the normal SiO_2 network because the dipoles orientate with a component in the opposite direction to the field have a significantly higher energy compared to those in the direction to the field. If the dipoles that oriented in the opposite

direction to the field are not constrained by forces of the lattice, they would easily flip to back to original direction. However, in the solid state, dipole flipping is expected to occur at a relatively low rate and can occur only via bond breakage. This is believed to give the dielectric breakdown its time-dependent characteristics. The final breakdown occurs when the broken bond sites or trap sites create a percolation path from the anode to cathode as shown in Figure 2.7, causing an abrupt increase in current resulting in severe Joule heating and ultimately thermal runaway shorting the anode to the cathode.

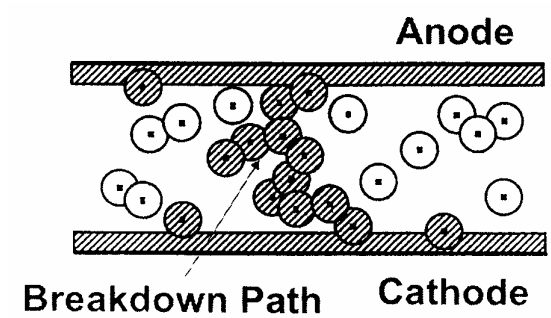


Figure 2.7: Percolation path shorting the anode to the cathode.

According to *E*-model, the time-to-failure can be expressed as:

$$\ln(TF) \propto \frac{E_a}{kT} - \gamma E \tag{2.7}$$

where TF is the time-to-failure, γ is the field acceleration factor, E is the electric field, E_a is the activation energy required for bond breakage, k is the Boltzmann constant and T is the temperature.

2.3.2 Reciprocal electric field *1/E*-Model

Hu *et al.* [23-24] proposed that TDDB is a current-induced oxide breakdown. The proposed TDDB degradation mechanism in SiO_2 is described in the schematic band diagram as shown in Figure 2.8.

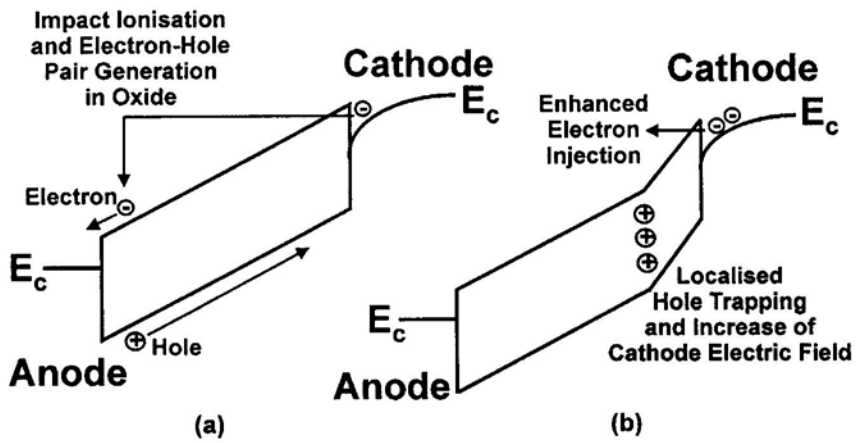


Figure 2.8: Schematic diagrams of TDDB degradation mechanism [23].

The degradation process begins when electrons are injected into the conduction band of the gate oxide from the cathode. When these electrons gain sufficient energy, they can cause impact ionization within the oxide thereby creating electron-hole pairs. The electrons are accelerated towards the anode while the holes are driven towards the cathode. Due to the low mobility of holes, these holes have high probabilities of being trapped in defect sites in the localized areas near the cathode. As more and more holes are trapped within the oxide, the internal electric field near the cathode is enhanced. As a result, more electrons can F-N tunnel from the cathode and causing more impact ionization. This process repeats itself creating a positive feedback and lead to ultimate

permanent oxide breakdown. As described by *1/E* model, the time-to-failure can be modeled as:

$$\ln(TF) \propto \frac{E_a}{kT} + G \cdot (1/E) \tag{2.8}$$

where G is the field acceleration factor, E_a is the activation energy required for current-induced hole injection and capture in SiO_2.

2.3.3 *E* and *1/E* Models

In 1998, McPherson *et al.* [27] presented a low-field (< 5MV/cm) three-year TDDB data which concluded that the *E*-model presents a much better fit to the data; and the poor fit of the *1/E*-model suggests very strongly that it is electric field and not current that causes the TDDB breakdown. Two years later, McPherson *et al.* again proposed a complementary model [28] which combines both *E* and *1/E* models to describe the TDDB degradation process using molecular bond strength. They claimed that for weak bonds below 3 eV, *E*-model better characterizes the bond breakage rate because it is comparatively easy to break the bonds by field-induced mechanism. On the other hand, for stronger bonds above 3 eV, *1/E* model better describes the bond breakage rate because the current-induced hole injection is required to catalyze the bond breakage by field-enhanced thermal means.

While McPherson *et al.* [27] has presented TDDB results that were best described by thermochemical model (especially at low electric field), a recent research done by Alam *et al.* [59, 60] shows that a new Anode Hole Injection model (AHI) can account for most of the breakdown data, including a change from the *E*-behavior to *1/E*-behavior. Besides the traditional majority carrier impact ionization described by Hu *et al.* [23], at low fields, minority carrier ionization can contribute significantly to hole tunneling current, especially when there is a significant hole accumulation at the anode interface. At low electric fields, the electron tunneling current has weaker field dependence and hence it is dominated by hole tunneling current that has an *E*-dependency. On the other hand, at higher electric fields where minority carrier ionization is less significant, the electron tunneling current has *1/E* dependency. In general, the new AHI model proposed by Alam *et al.* can account for both *E* and *1/E* models at low and high electric fields, respectively without changing the breakdown mechanism.

2.4 TDDB Degradation Mechanisms in Intra-level Cu Capacitors

TDDB degradation in intra-level Cu capacitor is becoming one of the important interconnects reliability issues. Because of the structure complexity, Cu ion contamination and non-uniform electric field distribution, analysis of TDDB data is sometimes quite puzzling. In this section, we review two different models which are backed by two different TDDB degradation mechanisms.

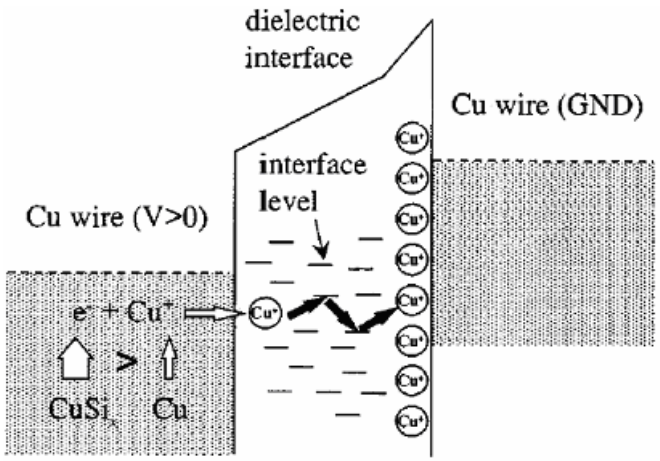


Figure 2.9: Schematic diagram of TDDB degradation proposed by Noguchi *et al.* [13].

According to one of the models proposed by Noguchi *et al.* [13] (Figure 2.9), TDDB degradation process is largely due to Cu ions drift through the dielectric surface trap states. Just after the Cu CMP process, the Cu surface contains large number of Cu ions while the dielectric surface contains large number of trap sites due to dangling bonds. As a result, under an applied bias-temperature stress, Cu ions can be easily injected into the dielectric and drifted through the interface trap levels in the dielectric leading to charge build-up and an eventual failure.

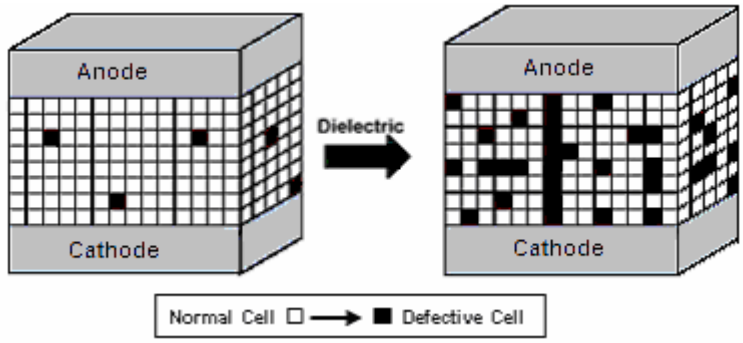


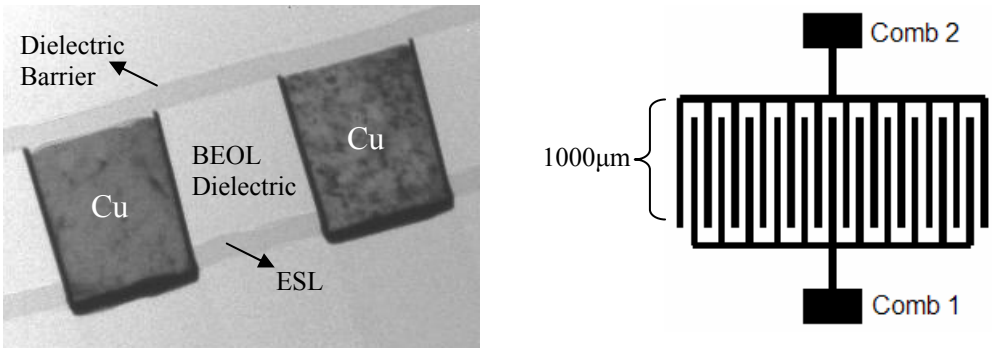
Figure 2.10: Percolation model for low-*k* breakdown [11].

On the other hand, Ogawa *et al.* [11] conducted TDDB experiments on different BEOL dielectrics with different *k* values. They found that dielectric films with higher degree of porosity (lower *k* values) tend to fail much more quickly. It was assumed that the pores in low-*k* materials have weaker bonds and some of these bonds break under high electric field and high temperature stress forming defective cells as shown in Figure 2.10. Eventually, TDDB occurs when these defective cells form a percolation path, shorting the anode to the cathode.

CHAPTER 3

EXPERIMENTAL DETAILS

3.1 Fabrication Process of Intra-level Cu Capacitors



(a) (b)

Figure 3.1: (a) Cross-sectional TEM image of comb capacitor test structure (b) top-view schematic diagram of comb capacitor test structure.

BEOL dielectric reliability tests such as leakage current and TDDB performance were carried out using comb capacitor test structure as shown in Figure 3.1. The comb capacitor is a series of intra-level Cu capacitors in parallel with one electrode normally grounded and the other electrode positively biased. This structure consists of 400 Cu lines each of length 1000 µm.

The experiments were carried out with the splits as shown in Table 3.1 below. Basically, two types of BEOL dielectric, USG and low-*k* SiOC were used. Cu/USG structure was used for the various surface treatments experiment while Cu/SiOC structure was used for the dielectric barrier experiment.

1) Surface treatment prior to dielectric barrier deposition				
	NH_3 treatment	H_2 treatment	SiH_4 treatment	No treatment
Cu/USG Structure	X	X	X	X
2) Dielectric barrier				
	SiN barrier		SiC barrier	
Cu/SiOC Structure	X		X	

Table 3.1: Surface treatment experiment using Cu/USG structure and dielectric barrier experiment using Cu/SiOC structure.

The focus of the surface treatment experiment is to examine the reliability performances of modifying the Cu surfaces with the various treatments. Since USG has a relatively stronger tetrahedral structure than the weakly bonded low-*k* SiOC material, by using USG bulk material, we minimize the many unknown degradation factors due to low-*k* bulk dielectric material (refer to Section 4.1 for results and discussions). On the other hand, the focus of the dielectric barrier experiment is to investigate the dependency of dielectric barrier on the reliability behavior of interconnects. The dielectric barrier materials used are SiN (k~7) and SiC (k~4.3), the development of lower k dielectric barrier material SiC is to couple with low-k bulk material (such as SiOC) so as to lower the overall effective k value of the structure. As a result, SiOC bulk dielectric material was used to study the effect of using conventionally used SiN and the lower k SiC.

Since the fabrication processes of Cu/USG structure and Cu/SiOC are very similar, their fabrication flows will be described and illustrated together as shown in the following diagrams. Please note the diagrams are not drawn in scale.

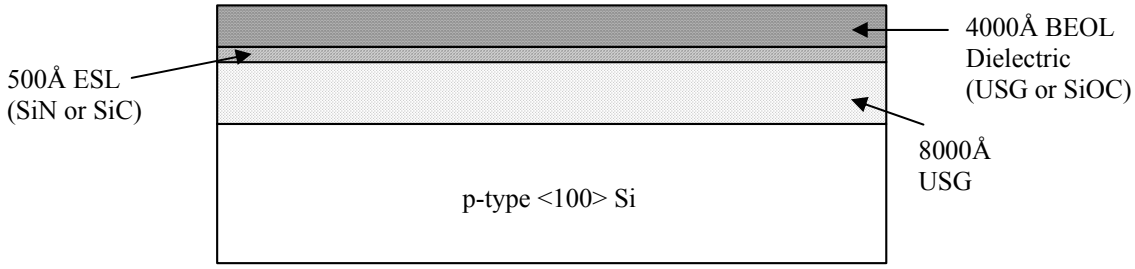


Figure 3.2: PECVD deposition of USG, ESL followed by BEOL dielectric.

To fabricate the comb capacitor test structure, to begin with, first inter-metal dielectric (IMD1) stack comprising 8 kÅ undoped silicate glass (USG), 500Å SiN or SiC etch-stop layer (ESL) and 4 kÅ dielectric (USG or SiOC) layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) system on top of device quality p-silicon substrate as shown in Figure 3.2. USG is used here as a buffer layer to prevent current from leaking through the substrate in the subsequent electrical tests and also, it has a better adhesion property with the Si substrate. The purpose of the etch-stop layer, as the name implies, is to provide an etch end point detection since the commonly used SiN and SiC has a high etch selectivity with respect to the BEOL dielectric.

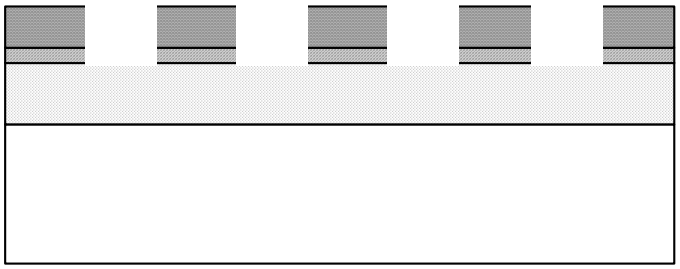


Figure 3.3: BEOL dielectric etch.

The wafers were patterned and then etched to open single damascene Cu trenches, followed by a wet clean process to remove post-etch polymer (Figure 3.3).

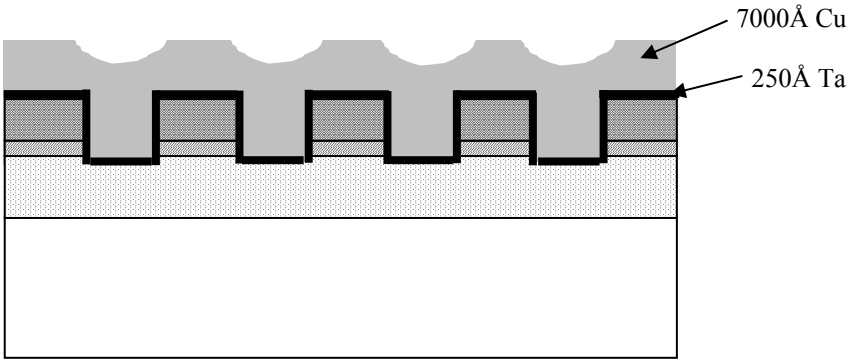


Figure 3.4: PVD Ta and Cu seed layer followed by ECP Cu deposition.

Subsequently, these trenches were filled with 250 Å Ta is the Cu diffusion barrier and 1.5 kÅ seed Cu by physical vapor deposition (PVD) followed by electrochemically plated (ECP) Cu. ECP is a deposition process which requires a conducting seed layer and it has proven to be ideally suited to damascene process as high ratio trenches are more readily filled than other deposition process such as PVD and CVD [29].

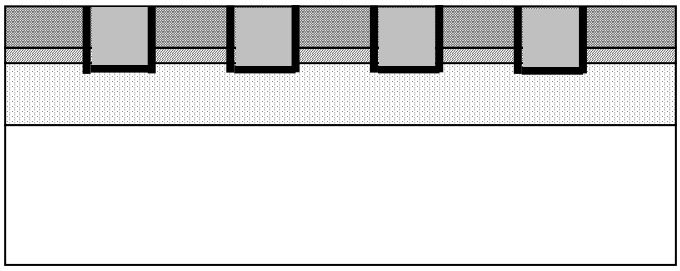


Figure 3.5: CMP of Cu and excess Ta.

Chemical mechanical planarization (CMP) (combination of the chemical removal from an acidic or basic fluid solution and the "mechanical" polishing from an abrasive material) was used to remove the Cu and Ta from the field areas.

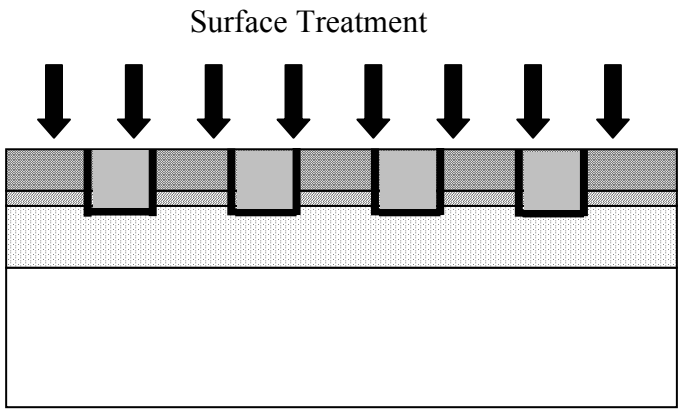


Figure 3.6: Introduction of additional surface treatment to improve reliability performance.

Because of the abrasive effect, the defects generated after Cu CMP (such as surface oxidation of Cu and generation of dangling bonds on the dielectric surfaces) have become a serious reliability concern in interconnect technology. Hence, the wafer surface was exposed to different surface treatments immediately after CMP (Figure 3.6) to enhance the reliability performance. The effect of various surface treatments such as NH_3, H_2 and SiH_4 treatments on the intra-level dielectric leakage and TDDB will be discussed in details in Section 4.1.

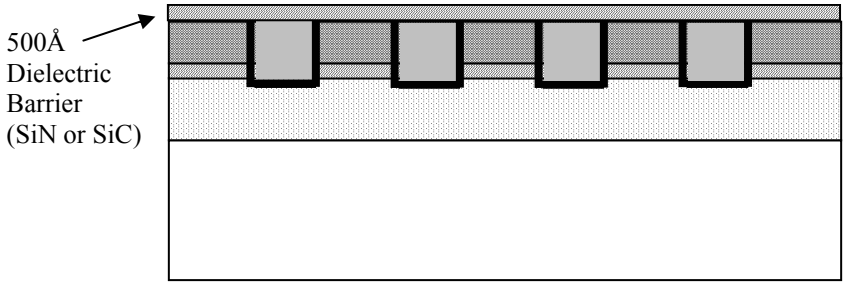


Figure 3.7: Dielectric barrier deposition.

In order to prevent Cu diffusion, the wafer surface was deposited with a layer of 500 Å of Cu different barrier layers – either SiC (k ~ 4.3) or SiN (k ~ 6.9). The effect of the two different diffusion barriers on reliability performance of Cu intra-level damascene structures will be studied comprehensively in Section 4.2.

3.2 BEOL Dielectric Reliability Assessment

To assess the dielectric reliability performance of the integrated intra-level comb capacitor structures with the different process splits, voltage-ramp tests at wafer-level and constant voltage (or electric field) stress TDDB tests at package-level were carried out.

3.2.1 Intra-level Leakage Current and Dielectric Breakdown Strength

Intra-level leakage current and dielectric breakdown strength tests were done using voltage-ramp tests by simply applying a sweeping voltage that linearly increases with time. At wafer-level, we are able to acquire the leakage current and breakdown strength

data fast and accurate. In our studies, voltage-ramp tests were carried out at different temperatures using a hot chuck control and a typical voltage ramp rate of 1V/s [9]. Figure 3.8 shows the integrated experimental setup for intra-level leakage current measurement at wafer-level. The probe station, the HP4156C Precision Semiconductor Parameter Analyzer and the E5250A Low Leakage Switching Matrix are connected to the host computer and these equipments are in turn controlled via a software control interface.

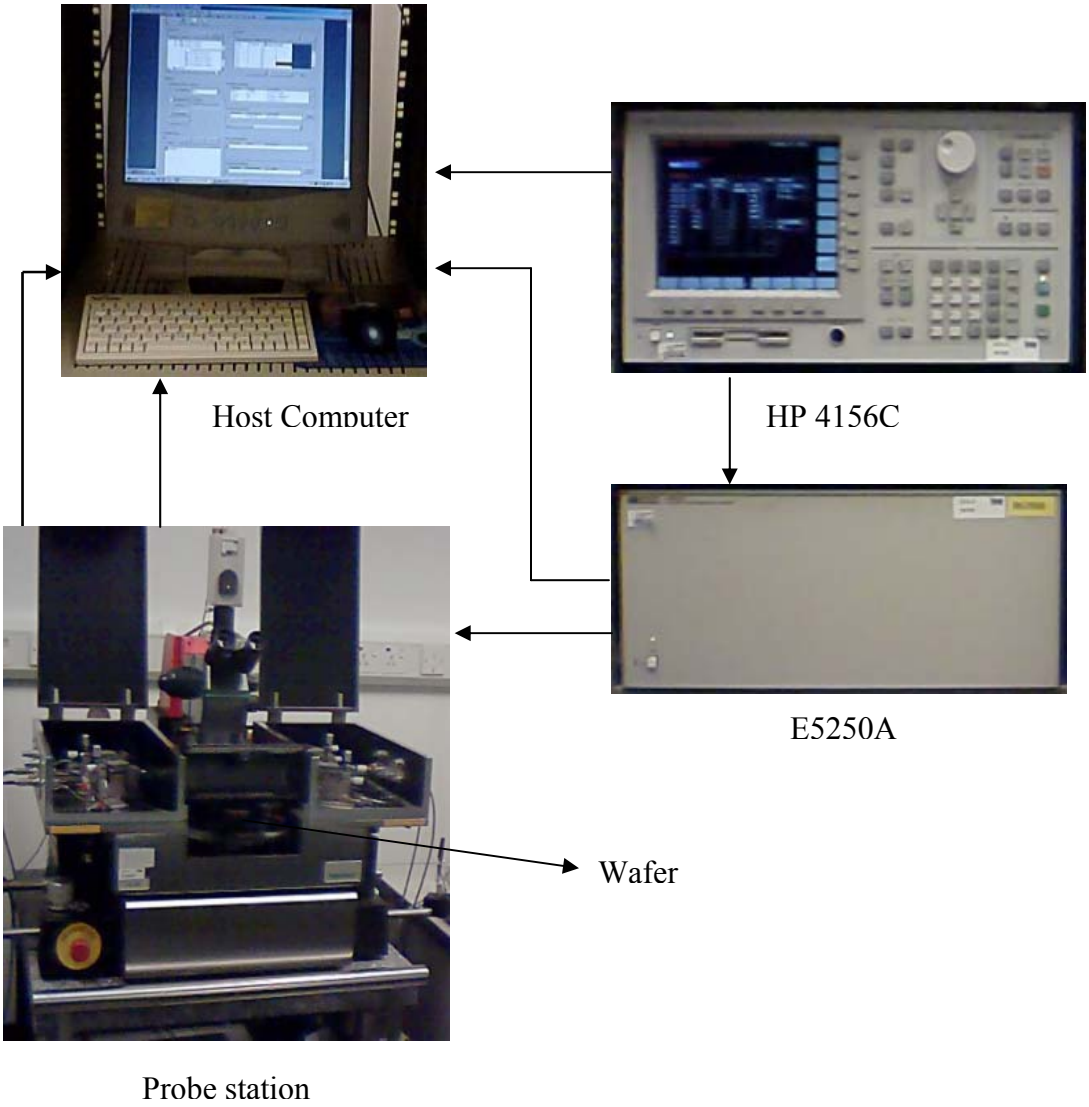


Figure 3.8: Experimental setup for intra-level leakage current test.

Due to the non-uniform distribution of electric fields in the intra-level comb capacitor [52], the area over which the current was injected (leakage pathway) was difficult to determine, therefore the measured current was expressed in terms of current, I_L rather than current density, J. Also, because of the sloped profile of Cu trenches, the applied electric field was obtained as the voltage drop across the dielectric divided by the minimum metal-to-metal spacing determined from the cross-sectional SEM images. The breakdown strength is typically defined as the electric field at which the leakage current rises abruptly by at least 1 order.

3.2.2 Constant Voltage Stress TDDB

Due to the relatively long testing time, TDDB tests were carried out at package-level. Prior to packaging the samples, leakage current test was first performed to weed out structures that have high initial leakage current. This will minimize the chances of having early failures in the subsequent TDDB tests. With the help of the dicing machine, the wafers were diced to small size with each piece containing the intended test strctures. Next, the die was attached to the ceramic packages using epoxy paste and the pads corresponding to the test structures were wire-bonded and finally the packaged device under tests (DUTs) were loaded into the Qualitau package-level reliability test system for TDDB reliability evaluation as shown in Figure 3.9.

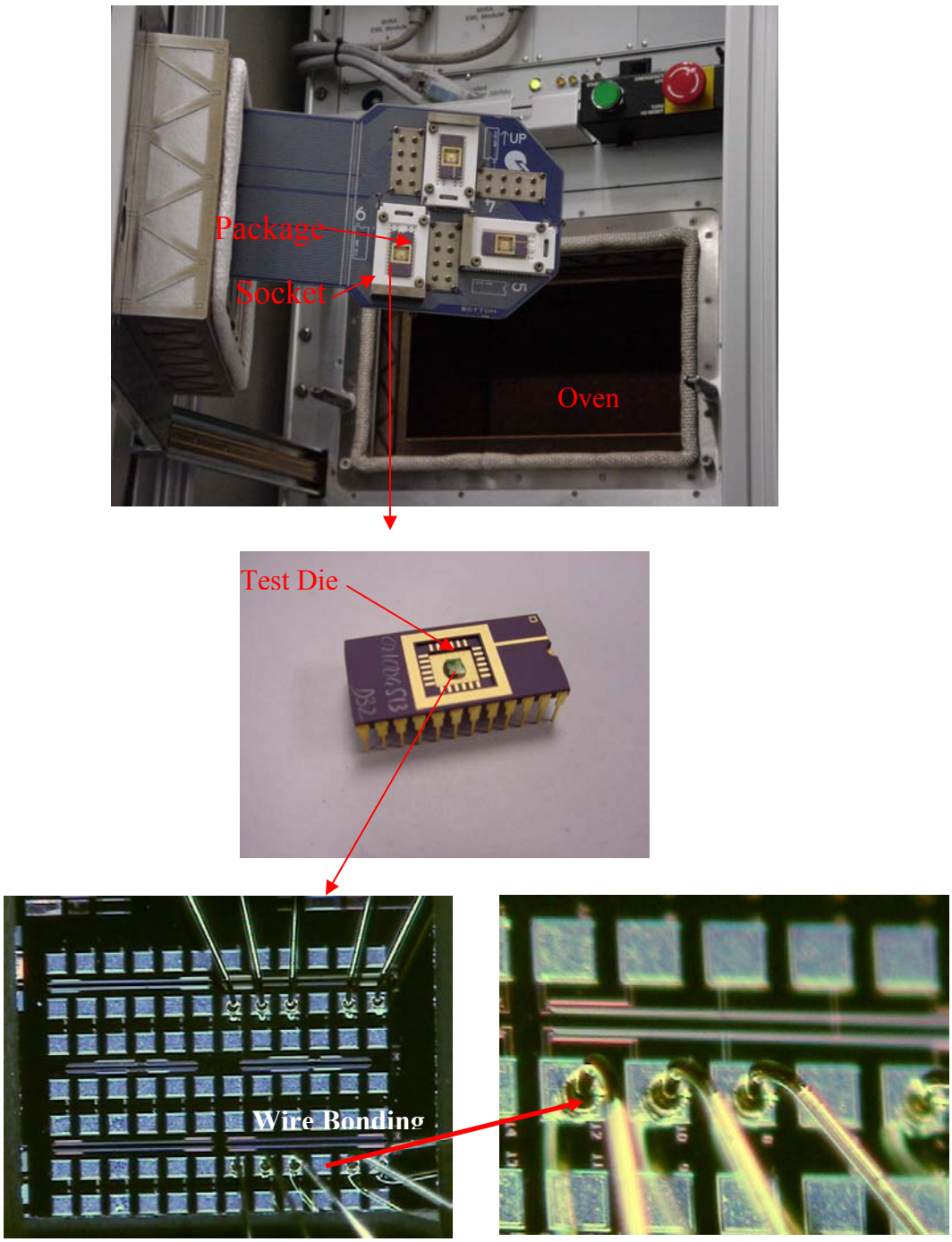


Figure 3.9: Experimental setup for TDDB test.

TDDB is an accelerated test of which the DUTs are tested at elevated temperatures and constant voltage stresses much greater than the normal operation condition. TDDB tests were conducted at various temperatures and voltages such that values of the field acceleration factor and the activation energy can be obtained. During testing, one electrode was typically grounded while the other was positively biased. The breakdown condition was typically defined as the abrupt rise in leakage current by at least 2 orders of magnitude [11]. However, due to the different BEOL dielectric (USG and low-*k* SiOC) and the different applied electric fields used, two distinct dielectric breakdowns: hard breakdown and soft breakdown were observed. This causes the TDDB analysis to be rather complicated. Details of soft breakdown phenomenon will be discussed in details in the following Section 4.2.7.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Effect of Surface Treatments on Interconnects Dielectric Reliability

The dielectric reliability of Cu interconnects such as intra-level leakage current, breakdown strength and time dependent dielectric breakdown (TDDB) are greatly dependent on the interface conditions of intra-level USG bulk dielectric/SiN barrier as well as Cu/SiN. Especially after Cu CMP process, the Cu surface is prone to oxidation and silicidation resulting in large number of high diffusivity Cu ions. Also, the dielectric surface is severely damaged resulting in dangling bonds being formed near the interface. Hence, the dielectric and Cu surfaces should be improved to reduce the dielectric surface trap states as well as the Cu surface ions that will degrade the dielectric reliability performance. In this particular section, the effect of modifying these interfaces by the surface treatments was studied using intra-level Cu damascene structures.

Table 4.1(a): Surface treatment split conditions

Surface Treatment	Gas Flow	Temp.	Power	Time	Condition
NH_3 treatment	NH_3 (100sccm)	130°C	250W	10s	In-situ
H_2 treatment	H_2 (450sccm), He (50sccm)	-	300W	60s	Remote
SiH_4 treatment	SiH_4 (105sccm), N_2 (2000sccm)	350°C	200W	4s	In-situ

The various surface treatments such NH_3, H_2 plasma, and SiH_4 (Table 4.1(a)) were performed immediately after CMP, but prior to dielectric barrier deposition (Figure 3.6). Some of these surface treatments were found to improve the USG/SiN and Cu/SiN interfaces thereby yielding a better leakage and TDDB reliability performances. Table 4.1(b) below lists the intentions and expectations of using the various surface treatments. Control wafers with no surface treatment were also fabricated.

Table 4.2(b): Expectation of the effect of various surface treatments on Cu and dielectric surfaces

Surface Treatment	Effect on Cu surfaces	Effect on dielectric surfaces
NH_3	The N component in NH_3 passivates the surface of Cu by forming CuN while the H component in NH_3 acts as a reducing agent of which it reduces Cu ions to Cu atoms. [13]	The N component in NH_3 passivates the dielectric surface by forming Si-N bond while the H component reacts to form Si-H bond. [13]
H_2	H_2 basically reduces Cu ions to Cu atoms. [13]	H_2 basically passivates the dielectric surfaces by forming Si-H bond. [13]
SiH_4	SiH_4 passivates the Cu surfaces by forming a layer of copper silicides. [31]	The H component in SiH_4 could form Si-H bond on dielectric surfaces.

4.1.1 Intra-level Dielectric Leakage Current of Cu/USG Interconnects

Intra-level leakage currents were measured from interdigitated comb capacitor test structures as shown in Figure 4.1. Due to the sloped profile of Cu trenches, the top Cu line-to-line spacing was 0.240 μm compared to the bottom Cu line-to-line spacing of 0.244 μm. The upper 0.240 μm spacing will be used in the following calculation of

applied electric field since our results (which will be discussed in the following sections) showed that the line-to-line leakage behavior is largely governed by the upper surface conditions. Similar results were reported by other researchers [12], [30], who concluded that the dominant leakage pathway in Cu damascene structures is at the interface of USG and SiN barrier.

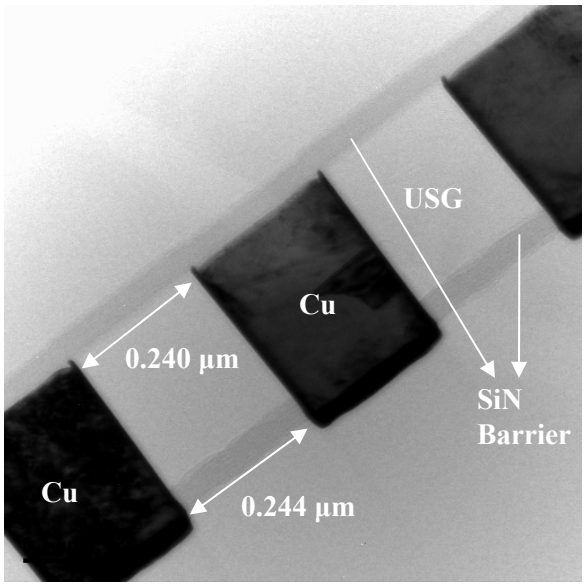


Figure 4.1: TEM cross-sectional image of the comb capacitor test structure.

Intra-level dielectric leakage current of structures treated by various treatments are shown in Figure 4.2. At electric field > 0.8 MV/cm, it could be observed that for structures with NH_3 and H_2 treatment, the leakage current was suppressed as compared to control samples without treatment.

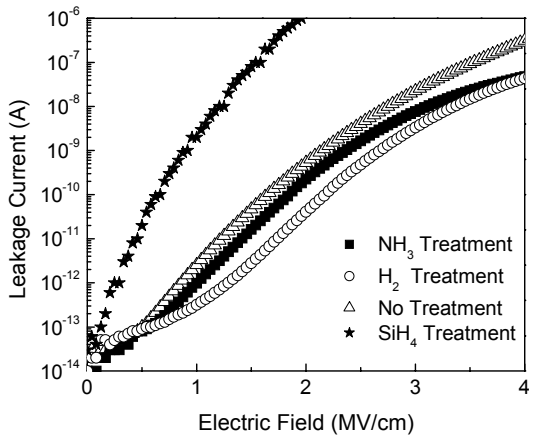


Figure 4.2: I_L-E_f plots showing effect of various surface treatments on intra-level leakage current at room temperature (measured from typical comb capacitor test structure with spacing of 0.240 μm as shown in Figure 4.3).

The improvement in leakage current is possibly due to the reduction of surface defect density by the H radicals generated by NH_3 and H_2 plasma treatments [13]. SiH_4 treatment was intended to form copper silicide that was reported to passivate and prevent oxidation of Cu lines [31]. However, with this treatment, the leakage current measured was very large, reaching approximately 10^{-11} A at 0.5 MV/cm. The large leakage current could be attributed to the ionization of Cu atoms due to formation of copper silicide that contributed to the large leakage current [13]. As such, SiH_4 treatment split was excluded in the subsequent reliability tests and discussions.

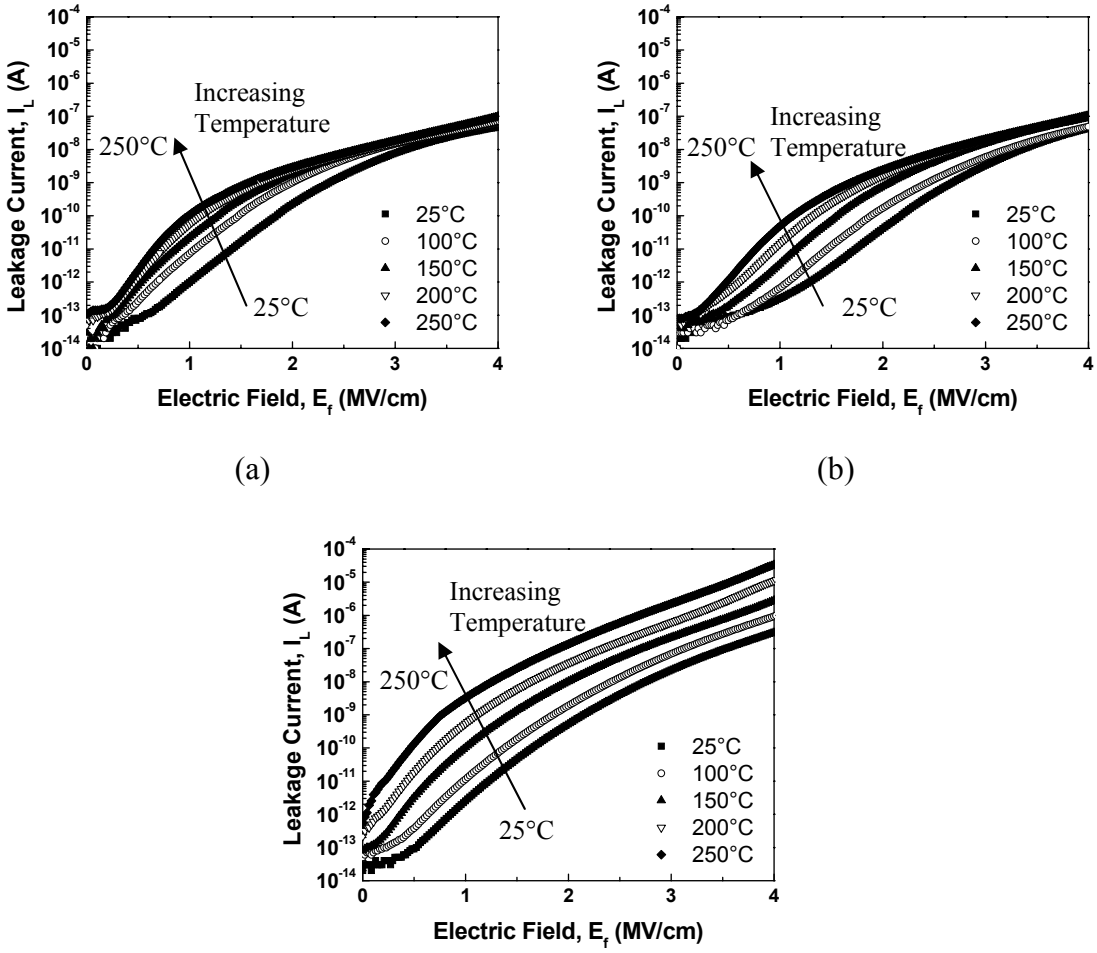


Figure 4.3: I_L-E_f characteristics of Cu/USG comb capacitor structures at different temperatures (a) with NH_3 treatment, (b) with H_2 plasma treatment and (c) without treatment.

Figure 4.3 shows the intra-level leakage current using a voltage ramp test from 25°C-250°C for the different split conditions. Interestingly, NH_3 treated structure shows rather weak temperature dependence and especially at electric field greater than 3MV/cm, the leakage current saturates regardless of temperature change. This phenomenon was equally observed in H_2 plasma treatment of which the leakage current begins to saturate above 3MV/cm. On the other hand, structures without any surface treatment have

stronger temperature dependence and no current saturation was observed over the range of electric fields.

To determine the physical mechanisms responsible for the leakage current, the dependence of current on electric field can be modeled to fit several dielectric conduction mechanisms including Schottky emission, Poole-Frenkel (P-F) emission, Fowler-Nordheim (F-N) tunneling, ohmic conduction and space charge limited current [14]. It was found that different conduction mechanisms dominate at different electric field regimes.

Note that in this particular work, I_L was not converted to current density J since the area over which the current was injected (leakage pathway) was difficult to determine. Moreover, for most of the analytical plots that will be discussed, the resulting linearity and slopes of the plots will not be affected whether we use I_L or J.

Intra-level leakage current in low electric field regime

From Figure 4.4, it was observed that in the low initial electric field region (< 0.4 MV/cm), the logarithm of the leakage current, $log\ I_L$ is directly proportional to the logarithm of the applied electric field, $log\ E_f$. The linear portions of the $log\ I_L$ vs. $log\ E_f$ curves with slopes of approximately 1 are typical of ohmic mechanism [15],[16],[32].

Ohmic conduction is very much dependent on the charged carriers such as electrons and ions in the intrinsic USG dielectric. In addition, the leakage current in this low electric field regime increases with increasing temperature, revealing a temperature dependence on the leakage behavior.

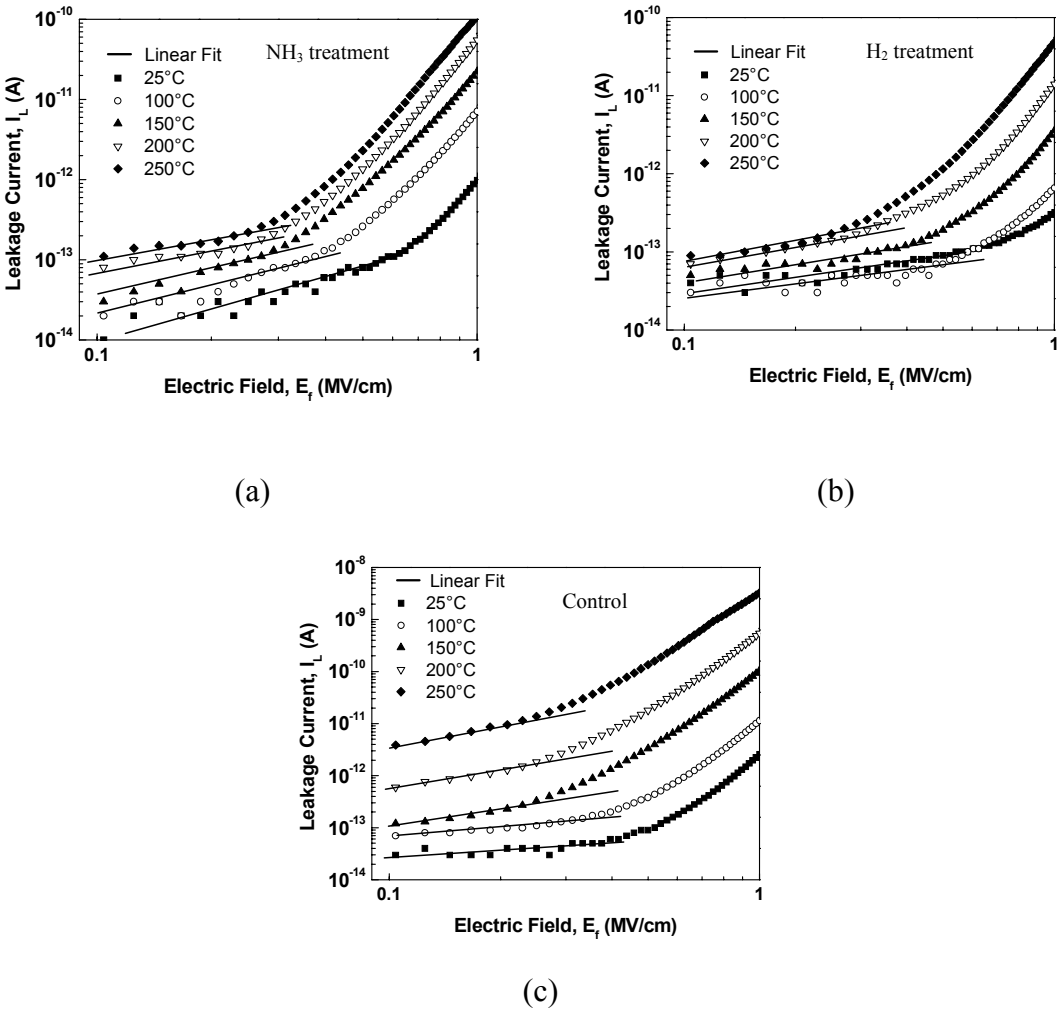


Figure 4.4: *Log* I_L vs. *log* E_f characteristics of Cu/USG comb capacitor structures (a) with NH_3 treatment, (b) with H_2 plasma treatment and (c) without treatment. The linear lines represent the nearly ohmic conduction at the initial low electric field.

Table 4.2: The slopes of the linear fitting of curves of log I_L vs. log E_f at low initial electric field (E_f < 0.4 MV/cm) and various temperatures.

Temperature	NH_3 treatment	H_2 treatment	No treatment
25°C	1.07	0.61	0.65
100°C	1.15	0.63	0.62
150°C	1.09	0.71	1.09
200°C	0.97	0.84	1.18
250°C	0.85	0.90	1.27

Table 4.2 lists the slopes of the linear fitting of curves of Figure 4.4 at low initial electric field (E_f < 0.4 MV/cm) with temperature range from room temperature to 250°C. The slope values of close to 1 at high temperatures yield ohmic conduction characteristics. On the other hand, at lower temperatures, especially in structures with H_2 plasma treatment and structures without treatment, the slopes obtained are very small. There could be two possible reasons behind this: firstly and clearly, the leakage mechanism is not dominated by ohmic conduction, it could be due to other mechanisms and secondly, the measured current is very small (in the order of 10^{-14}) and the sensitivity of the measurement instrument is not high enough to reflect the ohmic conduction characteristics. The latter seems to be a more logical explanation because of the inconsistencies of the data measured in this low field region.

Intra-level leakage current in high electric field regime

In order to determine the physical mechanisms responsible for the leakage current, I_L the dependence of current on applied electric field, E_f was compared for the two transport mechanisms known to be important for conduction in dielectric films: the Schottky and Poole-Frenkel (P-F) mechanisms.

From Equations (2.2) and (2.3), we change the current density, J to leakage current, I_L. The leakage current due to Schottky emission can be expressed as:

$$I_L = AA^*T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE_f / 4\pi\varepsilon_i}\right)}{kT}\right] \tag{4.1}$$

and the leakage current due to P-F emission can be expressed as:

$$I_L = C_1' E_f \exp\left[\frac{-q\left(\phi_t - \sqrt{qE_f / \pi\varepsilon_i}\right)}{kT}\right] \tag{4.2}$$

where A represents the area over which current is injected and C_1' is the product of A and the pre-exponential factor of Equation (2.3), C_1.

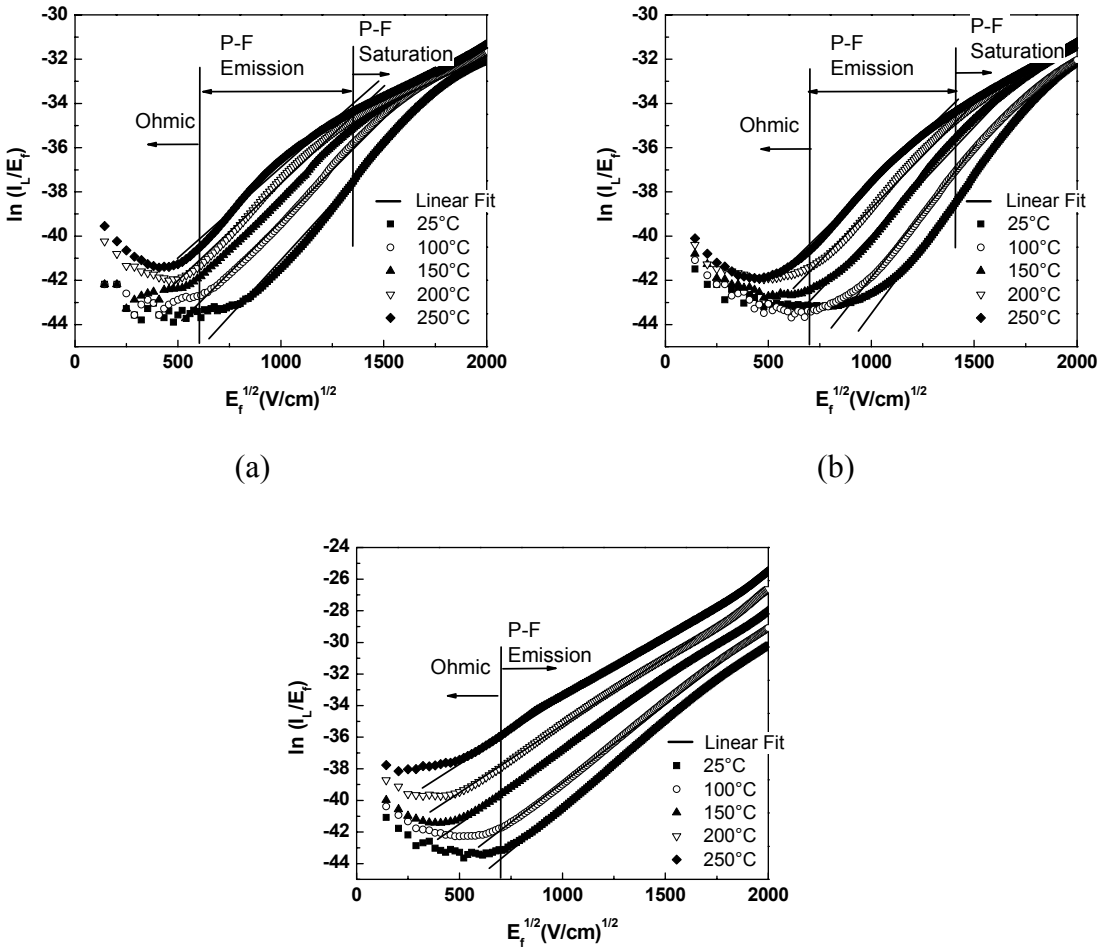


Figure 4.5: Plot of $ln(I_L/E_f)$ vs. $E_f^{1/2}$ showing P-F emission (a) with NH_3 treatment, (b) with H_2 plasma treatment and (c) without treatment.

Figure 4.5 shows P-F plots of $ln\ (I_L/E_f)$ versus square root of E_f for the NH_3 and H_2 plasma treated and the untreated structures. The linear fit regions imply the existence of P-F emission where the trapped electrons are excited into the dielectric conduction band and the increase in I_L with temperature is due to the enhancement in thermal excitation of the trapped electrons. On the other hand, plotting the Schottky plot of $ln\ (I_L)$ versus

square root of E_f (not shown here) also results in linear fit regions which indicates the possible presence of Schottky mechanism.

Table 4.3: List of dielectric constant, *k* obtained from intra-level comb capacitor structures due to Schottky and P-F emissions with various surface treatments.

Temperature (°C)	NH_3 treatment		H_2 treatment		No treatment	
	k_S	k_{PF}	k_S	k_{PF}	k_S	k_{PF}
25	<1	6.05	<1	5.43	<1	6.58
100	<1	5.46	<1	4.54	<1	5.58
150	<1	5.12	<1	4.51	<1	5.24
200	<1	5.03	<1	4.45	<1	5.02
250	<1	4.90	<1	4.38	<1	5.18

To differentiate P-F emission from Schottky emission, the values of dielectric constant, *k* due to Schottky, k_S and P-F, k_{PF} are calculated from the slopes of the linear fits of the respective P-F and Schottky plots. It has to be emphasized that the *k* values derived from either Schottky or PF-emissions are for references and they do not reflect the true *k* values of USG.

By comparing the *k* values as summarized in Table 4.3, we can see that the k_s derived ($k_s < 1$) are unreasonably low and this negates the occurrence of Schottky emission. On the other hand, the values of k_{PF} derived ($5 < k_{PF} < 7$) for NH_3 treated and the untreated

structures are quite inconsistent with any of the dielectric components (k_{USG}~4.2 and k_{SiN}~7) that made up the intra-metal capacitor while H_2 treated samples show k_{PF} ~ 4.5 which is rather consistent with k_{USG}. Hence, we postulate that with H_2 plasma surface treatment, the trap density at USG/barrier interface was significantly reduced as the dangling bonds were passivated by formation of Si-H bonds and hence the dominant leakage pathway is across bulk USG, I_{bulk} as shown in Figure 4.6. Due to the N component in NH_3 surface treatment, in addition to Si-H bonds, Si-N bonds were also formed on the surface of USG [13], and thus, a considerable amount of leakage current flows through this interface layer, $I_{interface}$ resulting in higher values of k_{PF}. NH_3 treated structure is showing a higher leakage current than H_2 treated structure, the main reason is due to the higher number of Si-N bonds at the interface. This corresponds well with the Poole-Frenkel emission modeling in which higher k_{PF} values were derived from NH_3 treated structure, suggesting presence of Si-N bonds. In the case of control samples without any surface treatment, because of the large number of unpassivated surface traps, the dominant leakage pathway occurs at the interface of USG/SiN, $I_{interface}$ giving larger values of k_{PF}.

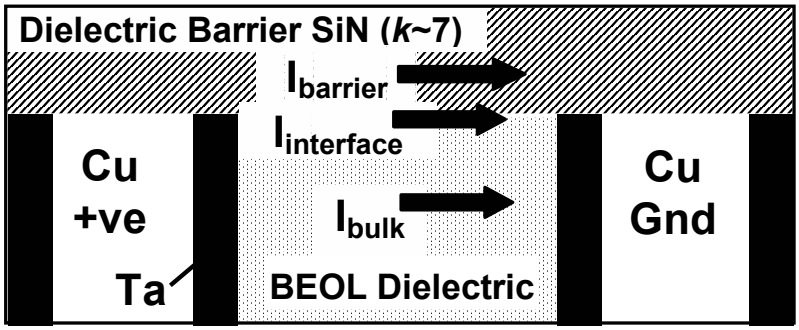


Figure 4.6: Schematic cross-sectional diagram of intra-metal capacitor test structure showing possible leakage pathways such as leakage through barrier layer, interfacial layer, bulk dielectric or their combinations.

The k_{PF} values obtained at 25°C seem to be relatively larger than those obtained at higher temperature. From Figure 4.3, we could see that the leakage current measured at lower temperature has a much lower magnitude, and as a results, the contribution of P-F emission may not be large enough due to the several other leakage mechanisms such as ohmic or Schottky processes which could be conducting at the same time.

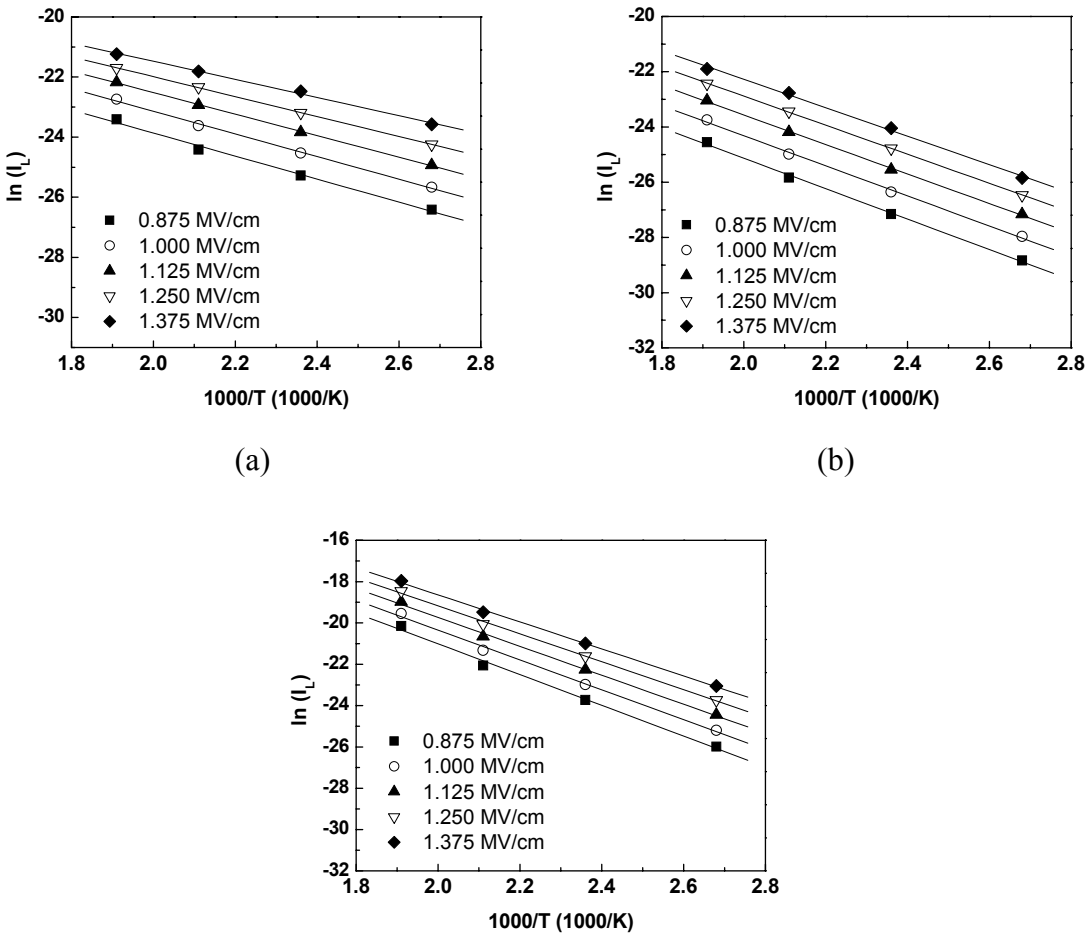


Figure 4.7: Dependence of $ln(I_L)$ on $1/T$ for comb capacitor structures (a) with NH_3 treatment, (b) with H_2 plasma treatment and (c) without treatment. The values of electric field were selected such as to correspond to conditions at which P-F emission is dominant, i.e., much lower than P-F saturation point.

Interestingly, P-F saturation effect [33] was observed in both NH_3 and H_2 plasma treated structures at E_f > 3MV/cm. To explain the physical meaning of P-F saturation, we recall P-F effect which is the thermal excitation of trapped electrons, enhanced by the electric field. So, at a given field, we expect more electrons to escape from the traps as the temperature increases. However, at P-F saturation, leakage current saturates with temperature change implying that all electrons are detrapped regardless of temperature, that is, there are no more trapped electrons responsible for P-F emission and as a result, P-F effect is no longer valid.

The Arrhenius plots in P-F dominant electric field range is shown in Figure 4.7. The thermally activated behavior further re-confirms the existence of P-F emission. From the y-intercept of curves, the pre-exponential factor of Equation (4.2), C_1' can be calculated.

The values of C_1' parameter obtained from the different surface treated structures are summarized in Table 4.4. With NH_3 and H_2 plasma surface treatments, C_1' was reduced by more than 4 orders of magnitude. This notable reduction is attributed to the suppression of surface trap density [34] by both NH_3 and H_2 plasma treatment.

Table 4.4: Values of pre-exponential factor, C_1' of P-F emission in comb capacitor structures with various surface treatments.

Surface Treatment	Poole-Frenkel Pre-exponential factor, C_1'
NH_3	1.5 (±0.5) × 10^{-13} $AV^{-1}cm$
H_2	3.1 (±0.9) × 10^{-14} $AV^{-1}cm$
No	2.8 (±0.2) × 10^{-9} $AV^{-1}cm$

The values of ϕ_t can then be easily obtained from the slopes of the fitted straight lines, m_{PF} which can be re-arranged from the P-F emission equation (Equation 4.2) and described as:

$$m_{PF} = \frac{-q(\phi_B - \sqrt{qE_f / \pi\varepsilon_i})}{k} \tag{4.3}$$

A careful look into Equation (4.3) reveals that the slopes of the curves are, in fact dependent on the square root of electric field, $E_f^{1/2}$.

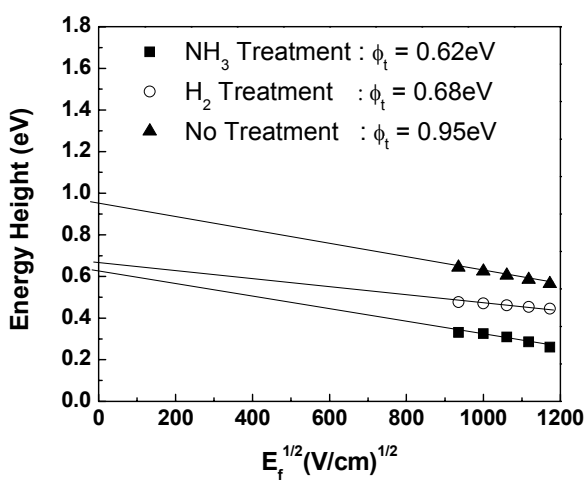


Figure 4.8: Graphical determination of P-F trap potential height, ϕ_t from the dependence of energy height on the square root of the electric field.

To extract ϕ_t, the energy height values of $-km_{PF}/q$ were plotted with $E_f^{1/2}$ as shown in Figure 4.8. Surprisingly, control samples without treatment (ϕ_t = 0.95eV) are showing a higher trap potential height than the NH_3 (ϕ_t = 0.62eV) and H_2 (ϕ_t = 0.68eV) treated structures. It is commonly thought that the lower the trap potential height, the higher the probability for thermally stimulated P-F emission to occur, and thus giving rise to higher current. However, our results are showing otherwise in which the surface treated structures are giving a lower value of ϕ_t and yet a much suppressed leakage current compared to structures without treatment that results in higher ϕ_t and larger leakage current. These, in fact can be well-explained from the P-F emission Equation (4.2).

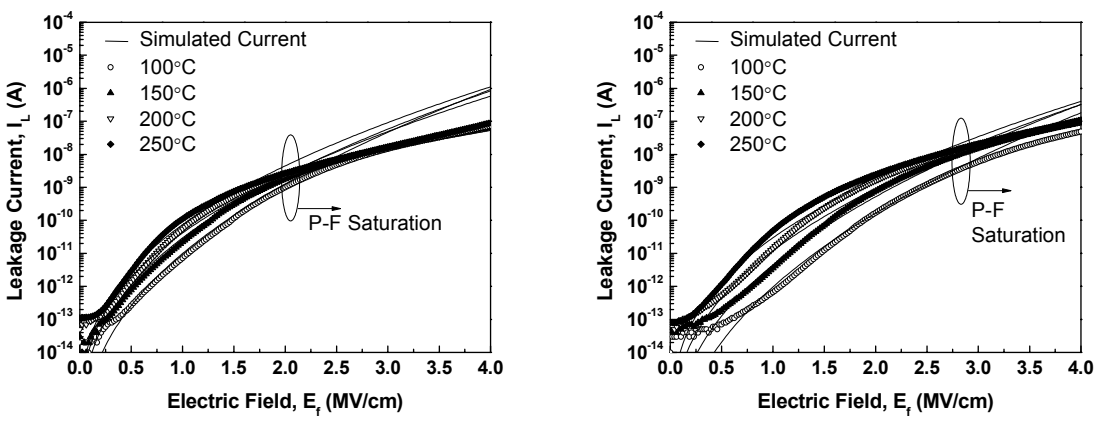
If we take the partial derivative of the Equation (4.2) with respect to temperature, we obtain:

$$\frac{\partial I_L}{\partial T} = I_L \left[\frac{q(\phi_t - \sqrt{qE_f / \pi\varepsilon_i})}{kT^2} \right] \tag{4.4}$$

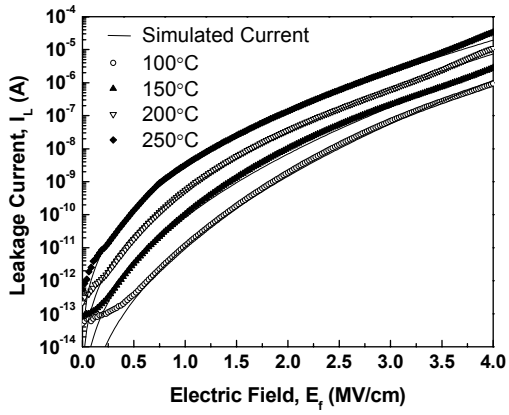
From Equation (4.4), the variation of current with temperature is in fact zero (P-F saturation) when $\phi_t = \sqrt{qE_f / \pi\varepsilon_i}$ [33]. It is therefore logical to obtain a lower ϕ_t for NH_3 and H_2 treated structures because P-F saturation occurs at a much lower E_f. Hence, we can conclude that it is in fact the trap density (indicated by the pre-exponential C_1 parameter) which ultimately decides the magnitude of the leakage current and not the commonly misinterpreted trap potential well height.

Together with the derived value of trap potential energy height, ϕ_t, the dielectric constant, k and the pre-exponential parameter, C_1', the I_L-E_f curves in the whole range of voltages and temperatures (except room temperature) were simulated using the P-F emission equation. Figure 4.9 shows the close fit of experimental and simulated current in the range of E_f of which P-F emission is dominant, i.e., until P-F saturation. It has to be noted that exceeding P-F saturation, the P-F simulation model becomes invalid.

Because USG has a breakdown strength higher than 5 MV/cm [10] and the machine limitation is at 100V, we are unable to conduct the breakdown strength experiment for intra-level Cu/USG structures.



(a) (b)

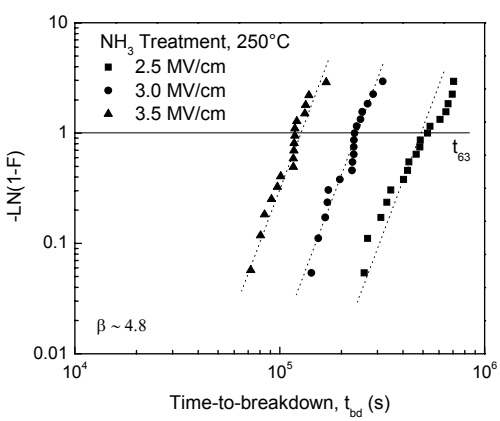


(c)

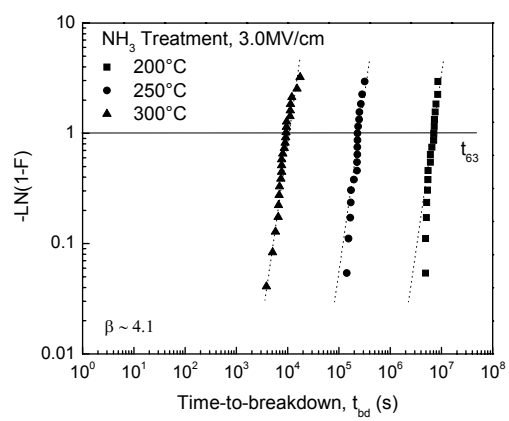
Figure 4.9: Comparison of experimental (symbols) and simulated (lines) currents of comb capacitor structures (a) with NH_3 treatment, (b) with H_2 plasma treatment and (c) without treatment.

4.1.2 TDDB

Time-dependent dielectric breakdown (TDDB) test is very useful in assessing the dielectric reliability of the integrated comb capacitor structure [10], [11], [13].



(a)



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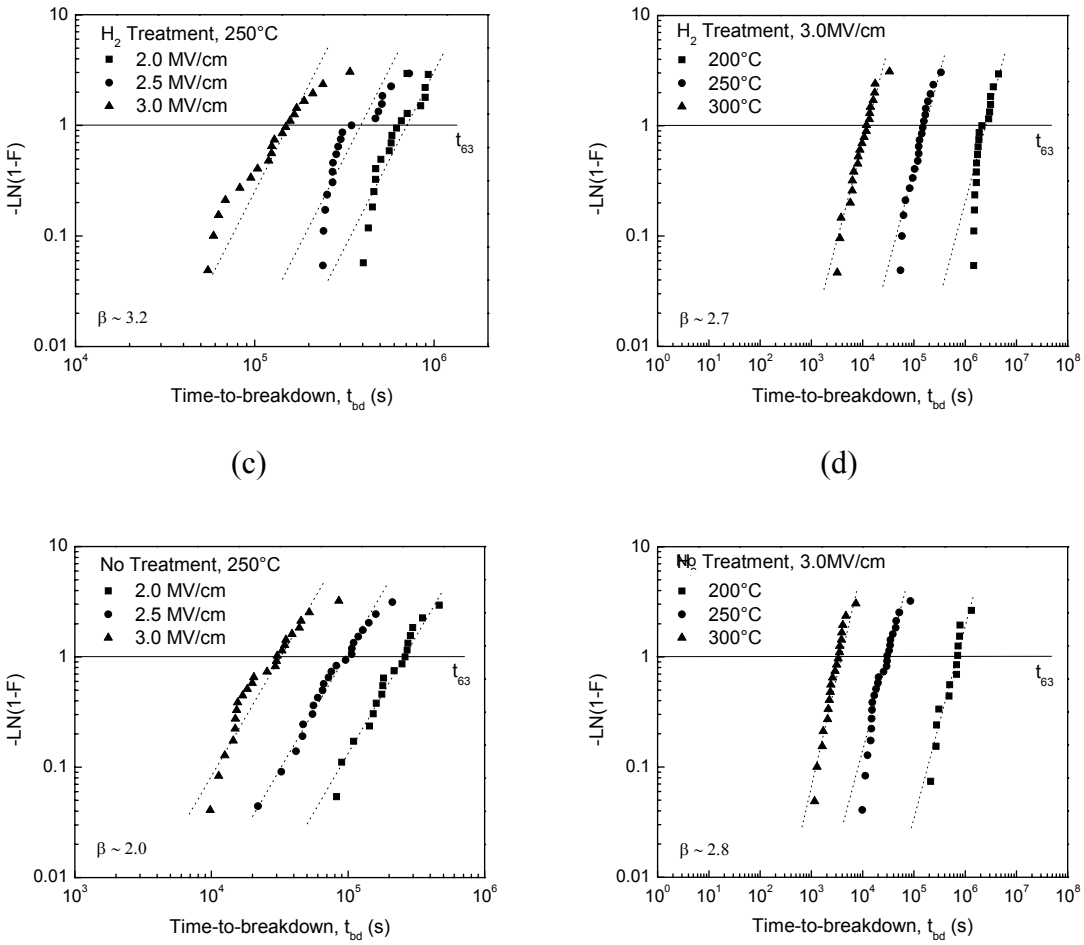


Figure 4.10: TDDB lifetime failure Weibull plots of intra-level comb capacitors (a) & (b) with NH_3 treatment (c) & (d) with H_2 treatment (e) & (f) without treatment at varying temperatures and electric fields

Figure 4.10 shows the TDDB Weibull plots for the various surface treatment splits. Generally, the TDDB lifetime results fit well with Weibull distribution. From the plots, both NH_3 and H_2 treated samples show relatively longer time-to-breakdown compared with control sample without treatment.

This is because the H component in NH_3 and H_2 is acting as a reducing agent in which it reduces copper ions to copper atoms and itself is oxidized to hydrogen ions (Equations

4.5 & 4.6). Hence, NH_3 and H_2 treatments improve TDDB performance relative to control samples without treatment.

$$Cu^{+} + e^{-} \rightarrow Cu \tag{4.5}$$

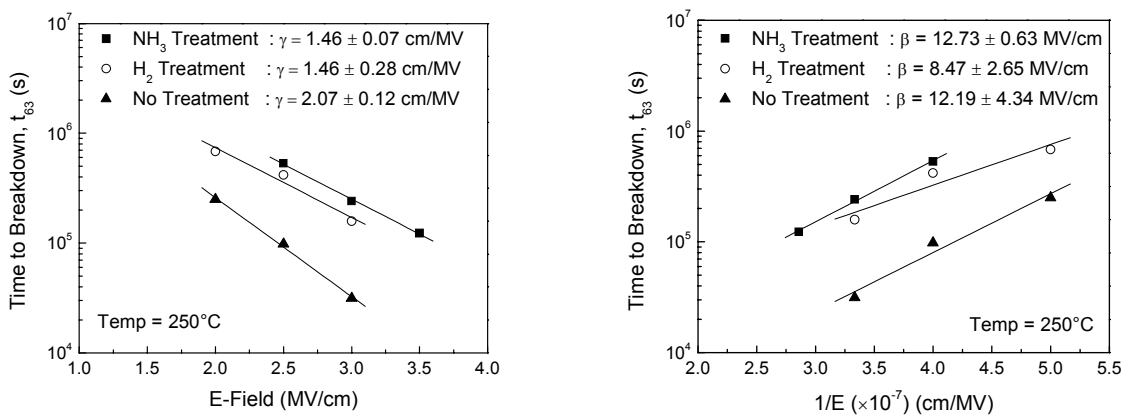
$$H \rightarrow H^{+} + e^{-} \tag{4.6}$$

At the same time, the N component in NH_3 forms a layer of CuN [13] which can inhibit further oxidation or silicidation of Cu and hence leads to better TDDB performance. Also, the Weibull shape parameter, β for the different splits were quite different. NH_3 treated samples were showing a larger β value ($\beta \sim 4.8$) than H_2 plasma treated samples ($\beta \sim 3.2$) and control samples without treatment ($\beta \sim 2.0$).

There has been much debate about the correct physical model for TDDB in front-end SiO_2 gate oxide. Recall the two TDDB models from Section 2.3, according to the proposed *E*-model, the time-to-breakdown is caused by dielectric bond breakage which ultimately create a percolation path from the anode to the cathode causing breakdown in the dielectric. On the other hand, *1/E* model suggests that the breakdown process is current-driven due to hole injection. The holes trapped in bulk SiO_2 increases the cathode electric field and eventually lead to dielectric breakdown by Fowler-Nordheim (F-N) tunneling.

Figure 4.11(a) shows the *E*-field dependence of TDDB lifetime failures of which the field acceleration factor, γ was derived (Equation 2.7) and Figure 4.11(b) shows the *1/E*-field

dependence of TDDB lifetime failures of which the field acceleration factor, *G* was determined (Equation 2.8). Interestingly, the values of γ obtained from structures with NH_3 and H_2 plasma treatments are identical (γ = 1.46 cm/MV) while γ = 2.07 cm/MV for control samples without treatment; and the values of *G* obtained from structures with NH_3 and without treatment are quite similar (~12 MV/cm) compared to H_2 treated structures which give *G* ~ 8 MV/cm.



(a) (b)

Figure 4.11: (a) Determination of field acceleration factor, *γ* from *E*-model of comb capacitor structures with SiN barrier. (b) Determination of field acceleration factor, *G* from *1/E*-model of comb capacitor structures with SiN barrier.

As mentioned earlier in Section 2.3.3, there has been much debate about the validity of *E* and *1/E* model in front-end gate oxide. But, which model best describes the TDDB degradation in back-end oxide with different surface treatments? According to the Noguchi's model (Section 2.4), TDDB degradation could be due to the injection of Cu ions through the interface trap levels in the dielectric leading to charge build-up and an eventual failure. On the other hand, as proposed by Ogawa *et al.* (Section 2.4), TDDB is due to percolation of defective sites of low-*k* materials.

In fact, both *E* and *1/E* models seem to explain both Noguchi's and Ogawa's degradation models well. By applying *E* model, it is assumed that under an applied electric field, TDDB failure occurs when the defective sites on the surface of the USG form a percolation path from the anode to the cathode. On the other hand, by applying *1/E* model, we assume that under an applied electric field, the mobile Cu ions will tend to drift through the dielectric and have high probability of being trapped in the defective sites (especially the interface traps) in the localized areas near the cathode. This can be modeled as a thinning in the effective dielectric thickness [38]. As a result, the internal electric field near the cathode is enhanced, and electrons can tunnel (F-N tunneling) easily from the cathode, causing impact ionization that creates electron-hole pairs in the dielectric. These holes will in turn get trapped in the dielectric as they were driven towards the cathode. As more and more holes are trapped, the electric field will be greatly enhanced. This process repeats itself creating a positive feedback and lead to TDDB failure (refer to Figure 2.8 for *1/E* schematic model and Figure 2.9 for TDDB due to Cu drift schematic model).

From Figure 4.10, the surface treated structures have longer lifetimes than the untreated ones. To fit *E*-model, it could be interpreted as: the reduction of surface trap density by the surface treatments has successfully reduced the probability of forming a percolation path that results in TDDB failure. On the other hand, to fit *1/E*-model, it could be interpreted as: the reduction of Cu ion density by the surface treatments decreases the probability of Cu ions being drifted into the dielectric, thereby enhancing the electric field near the cathode resulting in F-N tunneling and the final TDDB failure. At this

stage, it is difficult to come to a conclusion on which model best fits the back-end oxide TDDB degradation. Nevertheless, we shall show in Section 4.2.6 that *1/E* model is a valid model in explaining BEOL low-*k* TDDB degradation.

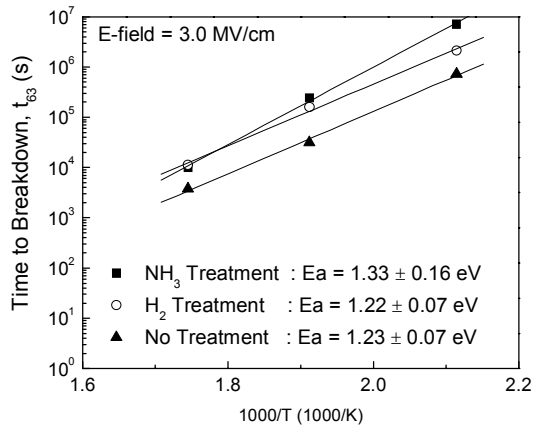


Figure 4.12: Temperature dependence plots of which the activation energies, *Ea* for the various process splits were extracted.

Figure 4.12 shows the temperature dependence of TDDB lifetime failures where the activation energy, E_a was calculated. It could be observed that the values of E_a for the different splits are very close. E_a = 1.33eV for NH_3 treated samples, E_a = 1.22eV for H_2 plasma treated samples and E_a = 1.23eV for control samples without treatment. The similarity in values of activation energy tends to suggest that the TDDB failure kinetics are quite consistent regardless of additional surface treatments.

4.2 Effect of Dielectric Barriers on Interconnects Dielectric Reliability

Due to the high diffusivity of Cu in backend oxide as well as low-*k* dielectrics [35-38], Cu diffusion into these dielectrics poses great reliability concerns such as high intra-level dielectric leakage, low breakdown strength and poor TDDB lifetime performance. To minimize Cu diffusion, Cu in damascene structures must be encapsulated by barrier materials such as barrier metal (Ta, Ti, TaN or TiN) at the bottom and sidewalls of Cu trenches and barrier dielectric (SiN or SiC) [39-44] at the top of Cu trenches. The high dielectric constant value of the conventionally used SiN barrier motivates the development and use of other lower dielectric constant barrier materials such as amorphous SiC. In this particular section, SiN barrier and the recently developed amorphous SiC barrier (using trimethylsilane as precursor) are characterized and evaluated for their electrical properties including dielectric constant; chemical properties such as relative elemental concentration, bonding structure and barrier properties against Cu diffusion; electrical reliability performance in integrated structure, including intra-level dielectric leakage, breakdown strength as well as TDDB lifetime.

4.2.1 Verification of Dielectric Constant

There is a large disparity in the dielectric constant values of amorphous SiC films reported in literature depending on the precursors used and deposition techniques [45-47]. Due to the process variations, it is important to determine the dielectric constant values of the diffusion barriers used. A targeted 150 nm thick SiN and SiC films were deposited

using a PECVD system. The measured film thickness and the derived dielectric constant, *k* values are listed in Table 4.5. The thickness of each sample was obtained from an average value of 49 different measurement points using Therma Wave Opti-Probe™ ellipsometry system. The *k* values of SiN and SiC films were obtained from C-V measurement at a frequency of 1MHz using Solid State Instruments 495 mercury probe system.

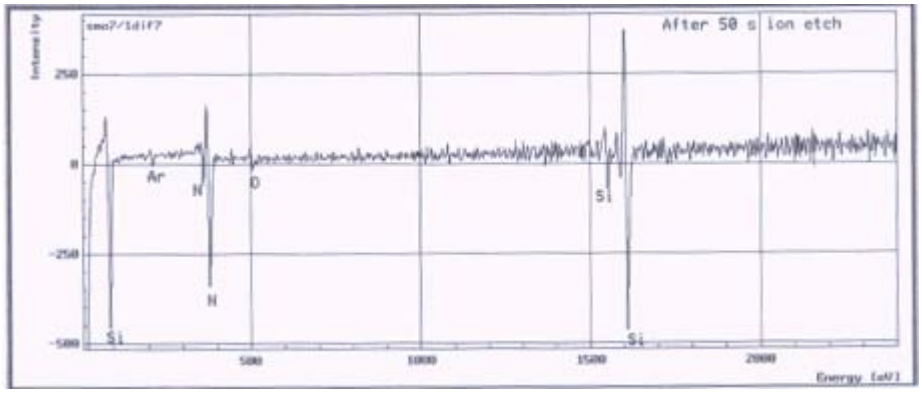
Table 4.5: Calculated dielectric constants of SiN and SiC films

Dielectric Barrier	Film Thickness (Å)	Dielectric Constant
SiN	1537	6.90
SiC	1425	4.37

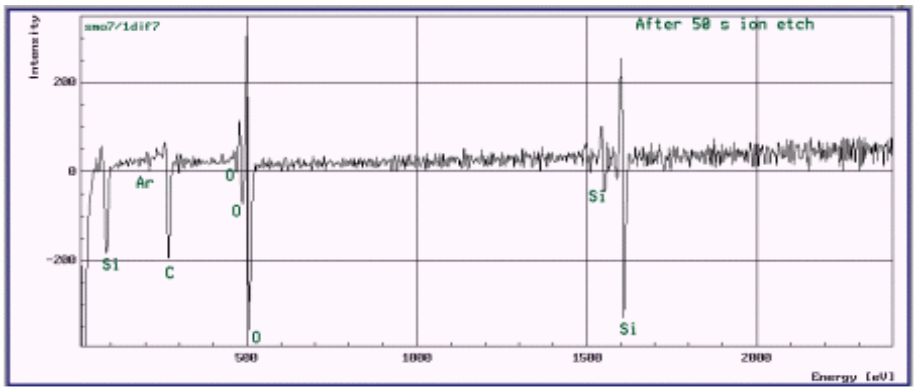
The use of SiC as Cu diffusion barrier has significantly reduced the dielectric constant by approximately 36% compared to conventionally used SiN. The physical and chemical reasons for this reduction will be discussed in the next section.

4.2.2 Chemical Analysis

In this section, we will discuss some of the chemical properties such as the degree of hydrogenation, the bond density, the ratio of silicon to carbon (in SiC) and silicon to nitrogen (in SiN), the porosity density and the content of defects. These properties have been reported as the fundamental parameters that will ultimately determine the properties of the films [47].



(a)



(b)

Figure 4.13: AES spectra 50 seconds Ar ion sputtering of 150nm thick (a) SiN film and (b) SiC film.

Auger electron spectroscopy (AES) with sputter-etching capability is one of the characterization methods for the study of compositional properties of dielectric materials. Figure 4.13(a) & (b) show the AES spectra after 50 seconds Ar ion sputtering of 150nm SiN and SiC films, respectively. A 50s Ar ion sputtering is to ensure that the results will not be affected by surface contamination of the films. The relative atomic concentrations of silicon, carbon, oxygen and nitrogen in SiN and SiC dielectric barrier films are shown in Table 4.6. The results indicate that both SiN and SiC films used are in fact Si-rich.

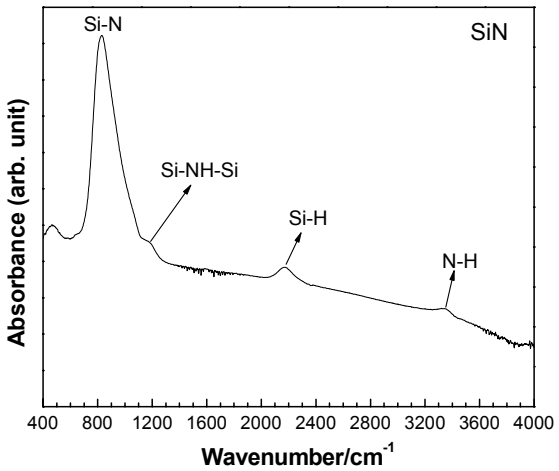
Oxygen concentration in SiC film is noticeably high, this is due to the usage of CO_2 gas during the deposition of SiC film. The more accurate chemical formula for SiN and SiC should be represented by $SiN_{0.53}$ and $SiO_{0.42}C_{0.47,}$ respectively and for simplicity these will be denoted as SiN and SiC hereinafter.

Table 4.6: Relative elemental concentration in percentage after 50s ion sputtering.

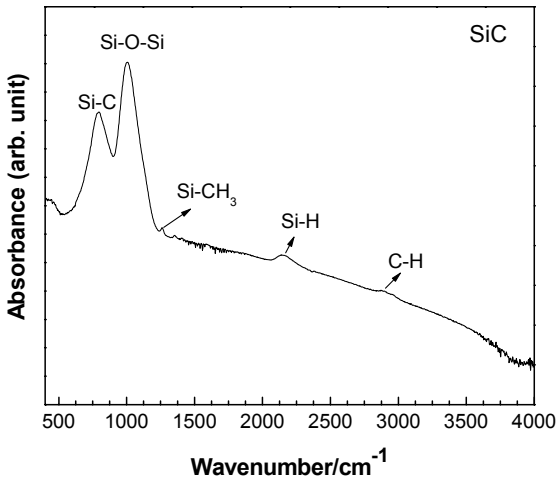
Dielectric Barrier	C	N	O	Si
SiN	-	34	2	64
SiC	25	-	22	53

Fourier transform infrared spectroscopy (FTIR) is one of the methods for characterization of dielectrics in terms of composition and bond structure. The FTIR spectra of SiN and SiC are shown in Figure 4.14(a) and (b), respectively. By analyzing the spectra of the films, it can be observed that the absorbance of hydrogen-related bond such as Si-H (at around 2130 cm^{-1}) in SiN film is relatively higher than that in SiC film. Moreover, the absorbance in other hydrogen-related bonds such as Si-NH-Si (around 1150 cm^{-1}) and N-H bond (around 3350 cm^{-1}) of SiN film is more prominent than Si-CH_3 bond (around 1270 cm^{-1}) and C-H bond (around 2920 cm^{-1}) of SiC film. The bonded hydrogen plays an important role in producing high interface trap density, rough interface and increase in carrier trapping sites [46], [48], [49]. Under electrical test, they will induce potential traps-assisted leakage pathways along the interface between dielectric barrier layer and

the underlying interconnects dielectric. The in-depth analysis of the traps-assisted leakage current will be discussed in the following Section 4.2.4.



(a)



(b)

Figure 4.14: FTIR spectra of 150 nm (a) SiN and (b) SiC barrier films.

The use of trimethylsilane precursor has significantly reduced the dielectric constant of SiC films. This is due to the presence of the terminating CH_3 group in SiC film that

greatly lowers the cross-linking and density of dielectric films as a result of larger volume occupied by the CH_3 group [50]. Carbon's low polarizability in Si-CH_3 bonding also contributes to the low dielectric constant of SiC films [6].

4.2.3 Cu Diffusion Barrier Property

The Cu diffusion barrier properties of the dielectric barriers, SiN and SiC were investigated by secondary ion mass spectrometry (SIMS). On top of p-silicon substrate, ~1-µm thick dielectric barrier films of SiN and SiC were deposited by PECVD. Following dielectric barrier deposition, an approximately 1.5 kÅ thick Cu was deposited by PVD. Finally, the films were annealed in a PEO601 Programmable Furnace (manufactured by Technologie Gmbh Muchen), in an Ar environment to prevent Cu oxidation. The temperature range used included those normally used for BEOL processes (200°C ~ 400°C) as well as higher temperatures (500°C ~ 800°C).

As observed in Figure 4.15, comparing the Cu diffusion profiles at all annealing conditions, the Cu intensity in SiC barrier is comparatively larger than in SiN barrier. This indicates that the barrier performance (against Cu diffusion) of SiN barrier is better than that of SiC barrier. When the annealing temperature was raised from 200°C to 400°C and 600°C, there is a significant increase in the Cu intensity in both barriers, especially in SiC film. Interestingly, at even higher temperature of 800°C, the Cu intensity drops at regions near Cu/barrier interface, and increases again at Cu/Si interface,

forming a hump shape. This phenomenon was previously reported by Gupta *et al.* [51], where the Cu diffusion coefficient in SiN film changed abnormally due to thermal instability above a certain temperature. The relatively poor performance in the diffusion barrier property of SiC might be due to microporous Si-O-Si cage structure (refer to Figure 4.14(b)) which is also responsible in lowering the *k* value of the film [40].

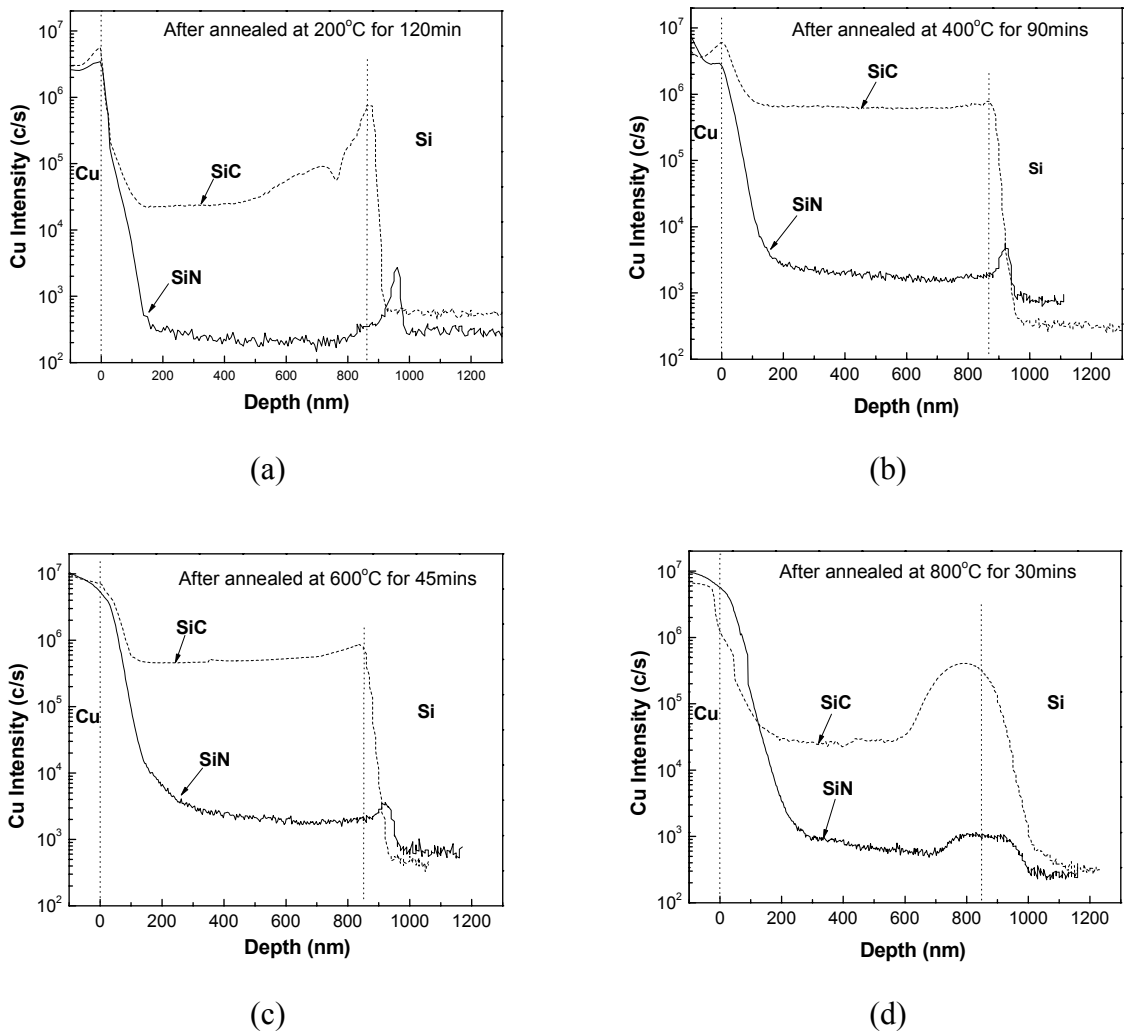


Figure 4.15: Depth profile of Cu obtained from Cu/dielectric barrier/Si structure after annealed at a) 200°C, b) 400°C, c) 600°C, d) 800°C in Ar atmosphere.

4.2.4 Intra-level Dielectric Leakage Current of Cu/SiOC (low-*k*) Interconnects

Low-*k* materials are generally quite leaky [10] and when they are integrated with Cu in interconnects, the maximum local electric field occurs at barrier/low-*k* dielectric interface. This happens when the etching process results in sloped sidewalls or when over-etching process etches through the etch stop layer (ESL) [52].

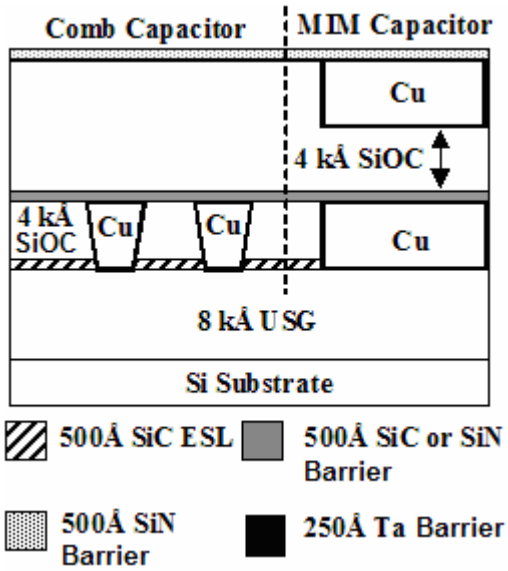


Figure 4.16: Schematic layout of intra-level comb capacitor and MIM capacitor structures.

Experiments were conducted on intra-level comb capacitor test structures consisting of 400 Cu lines each of length 1000 μm as shown in Figure 4.16. Details of the process of fabrication of comb capacitor test structures were already discussed in Section 3.1. Subsequently, MIM capacitor of metal area 0.008 cm^2 and 4 kÅ thick SiOC was also

fabricated by the standard dual damascene process. Finally, the completed structures were annealed in N_2/H_2 ambient at 350°C for 30 min.

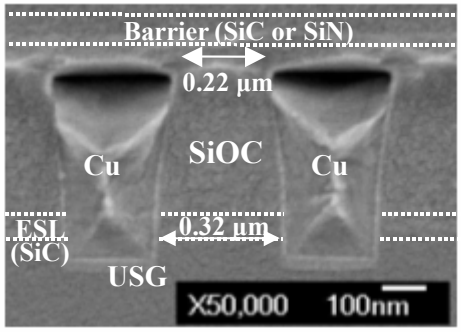


Figure 4.17: Cross sectional SEM image of a section of a Cu/low-*k* comb capacitor.

For reasons mentioned earlier, maximum electric field occurs at the interface of dielectric barrier and SiOC. Due to the sloped profile of Cu trenches, the measured minimum Cu line-to-line spacing was 0.22 µm as shown in Figure 4.17 and this value was used in the following calculation of applied electric field.

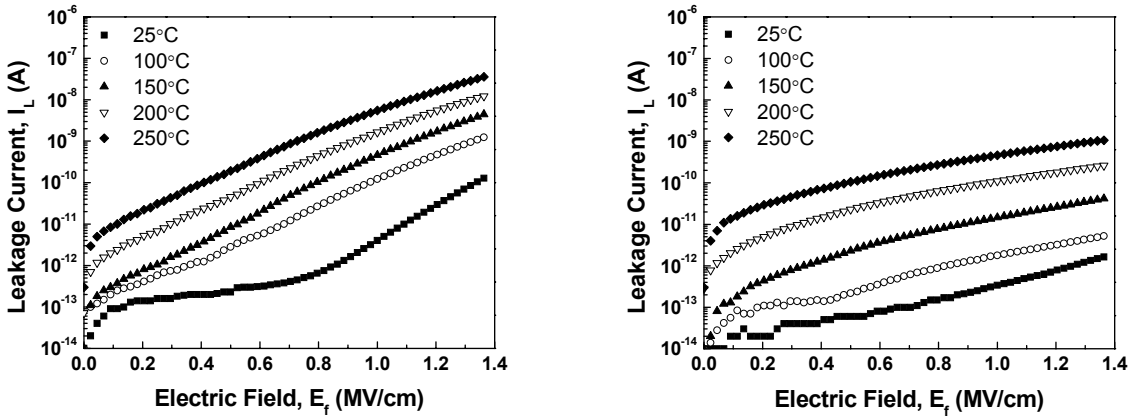
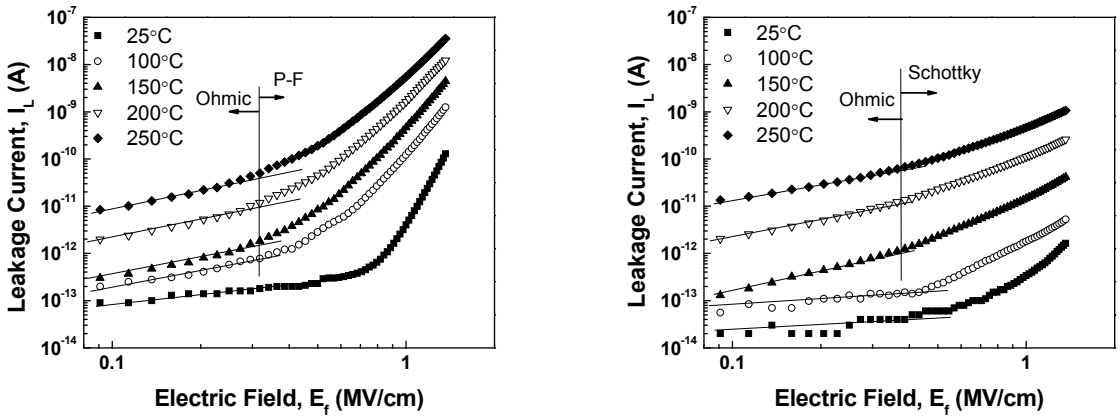


Figure 4.18: I_L-E_f characteristics of Cu/SiOC comb capacitor structures with (a) SiN and (b) SiC barrier layers.

Figure 4.18(a) and (b) show the leakage current-applied electric field (I_L-E_f) characteristics at different temperatures for comb capacitors using SiC and SiN barriers respectively. With SiC barrier, it could be observed that the leakage current measured is at least an order of magnitude smaller than that with SiN barrier. In term of leakage current, SiC barrier is better than SiN barrier.

Intra-level leakage current in low electric field regime

It can be seen from Figure 4.19 that in the low initial electric field region (< 0.4 MV/cm), the leakage current, I_L is linearly proportional to the applied electric field, E_f. Similar to the results discussed in Section 4.1.1, the linear portion of the *log* I_L vs. *log* E_f curve is typical of ohmic conduction mechanism.



(a) (b)

Figure 4.19: *Log* I_L vs. *log* E_f characteristics of Cu/SiOC comb capacitor structures with (a) SiN barrier and (b) SiC barrier. The linear lines represent the nearly ohmic conduction at the initial low electric field.

Table 4.7: The slopes of the linear fitting of curves of Figure 4.19 at low initial electric field (E_f < 0.4 MV/cm) and various temperatures.

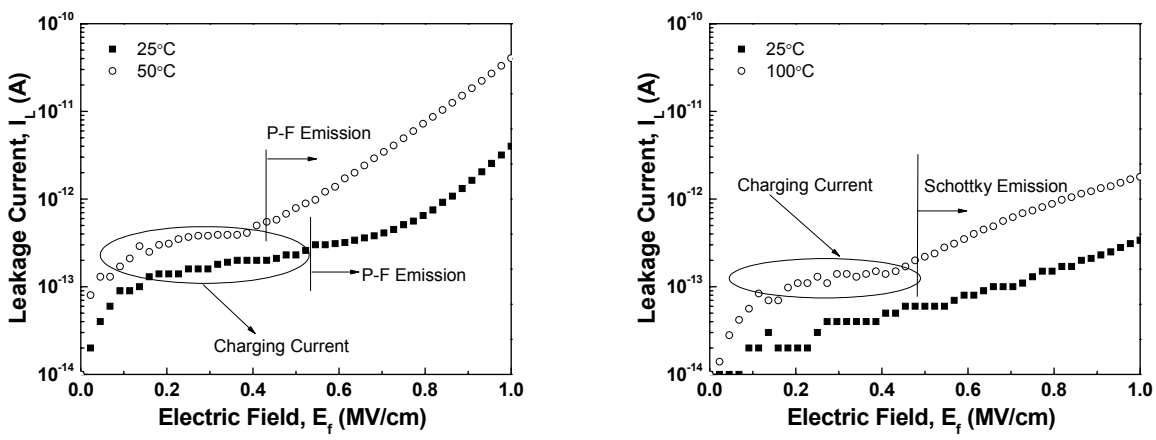
Temperature	SiN	SiC
25°C	0.70	0.39
100°C	1.14	0.43
150°C	1.16	1.31
200°C	1.18	1.21
250°C	1.25	1.24

Table 4.7 lists the slopes of the linear fitting curves of Figure 4.19 at low initial electric field (E_f < 0.4 MV/cm) and temperature (25°C - 250°C). The slope values of almost 1 at high temperatures confirm the existence of ohmic conduction mechanism. The discrepancies in the slope values at lower temperature especially in structure with SiC barrier indicate that the dominant leakage mechanism may not be of ohmic characteristic or the sensitivity of the measurement instrument is not high enough to reflect the ohmic conduction characteristics.

Intra-level leakage current in low electric field, low temperature regime

From Figure 4.18(a), the leakage current curve at 25°C seems to be different from the other curves at higher temperature. Also, Table 4.7 further shows the discrepancies in the values of the slopes of $log\ I_L$ vs. $log\ E_f$ curves at lower temperatures. In order to explain

the leakage current behaviors, curves at low electric field and low temperature were scrutinized and shown in Figure 4.20. At low temperatures of 25°C and 50°C for structure with SiN barrier and at temperature of 100°C for structure with SiC barrier, as the applied electric field increases, we could see a sudden rise in leakage current in the beginning of voltage ramp test, followed by a region of saturation of leakage current (< 0.6MV/cm). As mentioned earlier in Section 2.2, Bersuker *et al.* [9] attributed the observed leakage saturation characteristics to capacitance charging current in intra-level comb capacitor.

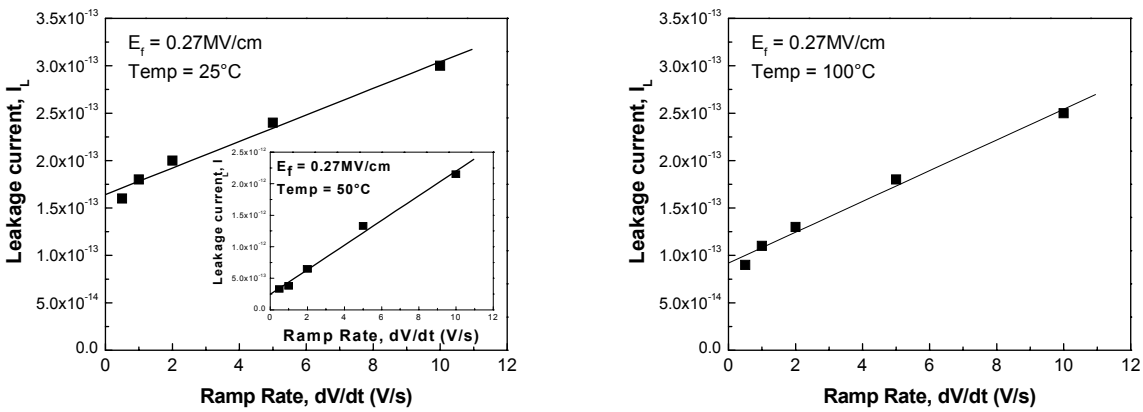


(a) (b)

Figure 4.20: I_L vs. E_f characteristics of Cu/SiOC comb capacitor structures with (a) SiN barrier and (b) SiC barrier showing capacitor charging current characteristic at low electric field and low temperature.

From Equation (2.6), we know that leakage current is proportional to voltage ramp rate. To verify the existence of capacitance charging current, the leakage current at constant applied E_f of 0.27MV/cm (corresponds to E_f in which charging current is active) is

plotted against voltage ramp rate as shown in Figure 4.21. The straight line fitting of the curves of comb structures with SiN barrier at 25°C, 50°C; and comb structures with SiC barrier at 100°C further re-confirms the capacitance charging current mechanism in the low temperature, low electric field regime.

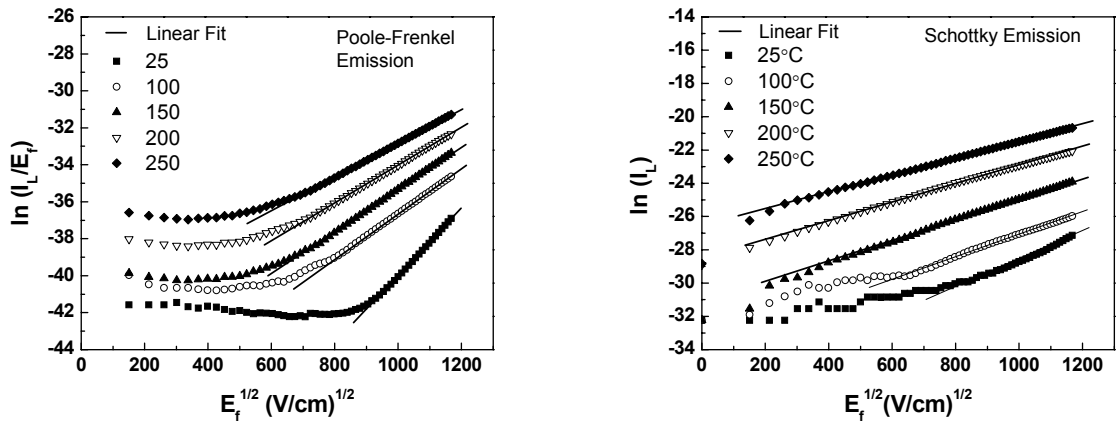


(a) (b)

Figure 4.21: I_L vs. dV/dt characteristics of Cu/SiOC comb capacitor structures with (a) SiN barrier at temperature of 25°C, the inset shows SiN barrier at 50°C and (b) SiC barrier at 100°C.

Intra-level leakage current in high electric field regime

The leakage current in dielectric film can be attributed to several widely-known conduction mechanisms including Schottky emission, Poole-Frenkel (P-F) emission, Fowler-Nordheim (F-N) tunneling and space charge limited current [14].



(a) (b)

Figure 4.22: (a) Plot of $ln(I_L/E_f)$ vs. $E_f^{1/2}$ showing P-F emission with SiN barrier and (b) plot of $ln(I_L)$ vs. $E_f^{1/2}$ showing Schottky emission with SiC barrier.

In order to determine the different types of conduction mechanisms in comb capacitors, I_L-E_f curves were re-plotted to fit Schottky emission and P-F emission equations. The values of k due to Schottky emission, k_S and P-F emission, k_{PF} can be calculated from the slopes of the respective straight lines of $ln(I_L/E_f)$ vs. $E_f^{1/2}$ with SiN barrier as shown in Figure 4.22(a) and $ln(I_L)$ vs. $E_f^{1/2}$ with SiC barrier as shown in Figure 4.22(b). Together with the k values of SiOC (k_{SiOC} = 2.69 to 2.89) derived from MIM capacitor, k_S and k_{PF} are summarized in Table 4.8. Note that the capacitance of the dielectric barrier layer which is in series with the capacitance of SiOC (Figure 4.16) has to be accounted for when obtaining the dielectric constant of SiOC from the MIM capacitor.

Table 4.8: List of dielectric constant, k obtained from MIM capacitor and comb capacitors due to Schottky and P-F emissions with both SiC and SiN barriers.

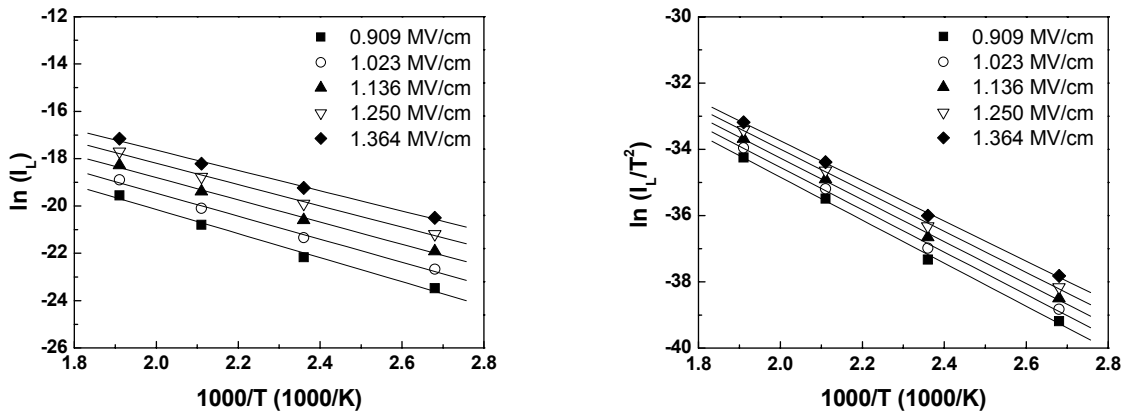
Temperature (°C)	MIM Capacitor	Comb Capacitor SiN Barrier		Comb Capacitor SiC Barrier	
	k_{SiOC}	k_S	k_{PF}	k_S	k_{PF}
25	2.92	<1	2.91	3.53	>30
100	2.85	<1	3.48	3.01	>30
150	2.77	<1	3.38	2.84	>30
200	2.72	<1	3.36	2.76	>30
250	2.69	<1	3.34	2.74	>30

For comb capacitors with SiN barrier, k_S calculated (k_{SC}<1) are unreasonably low. From P-F emission modeling, k_{PF} obtained at temperature above 100°C (k_{PF} = 3.34 to 3.48) are larger than that of SiOC but smaller than that of bulk SiN. This suggests that the probable path for P-F emission could be at the interface of SiN/SiOC, $I_{interface}$ as shown in Figure 4.6. Hence, we deduce that the interface of SiN/SiOC contains a substantial amount of traps such as dangling bonds or other process-induced defects (such as during PECVD of SiN).

With SiC barrier, k_S obtained at temperature above 100°C (k_S = 2.74 to 3.01) are consistent with k_{SiOC} obtained from MIM capacitor. On the other hand, k_{PF} extracted from P-F emission modeling are more than 30. These values are not in agreement with any of the k values of the components that made up the comb capacitor. Therefore, we deduce

that with SiC barrier, the dominant leakage is due to Schottky emission over Ta/SiOC barrier and the leakage pathway is indicated by I_{bulk} in Figure 4.6. Note that due to non-uniform distribution of electric field in the structure, maximum electric field concentrates at regions near the interface of SiC/SiOC. Hence, I_{bulk} in this case refers to the leakage pathway through bulk low-k in the regions very near to the interface. The absence of P-F emission in SiC-SiOC structures indicates that traps in bulk SiOC, SiC/SiOC interface and bulk SiC are negligible.

Interestingly, it can be seen from Table 4.8 that for both SiN-SiOC and SiC-SiOC structures, the values of k_{PF} and k_S derived (k_{PF} = 2.91 for SiN-SiOC structure, k_S = 3.53 for SiC-SiOC structure) at room temperature are inconsistent with the rest of the values of k_{PF} and k_S obtained at higher temperature. These inconsistencies could be due to the relatively small magnitude of leakage current measured at low temperature. The co-existence of ohmic and capacitor charging current mechanisms could have interfered with the overall leakage current and as a result no prominent dominance of one particular leakage mechanism can be observed.



(a) (b)

Figure 4.23: (a) Dependence of $ln(I_L)$ on $1/T$ for structures using SiN as barrier and (b) dependence of $ln(I_L/T^2)$ on $1/T$ for structures using SiC as barrier. The values of electric field were selected such as to correspond to conditions at which P-F or Schottky emission is dominant.

It is well known that P-F emission is caused by field-enhanced thermal excitation of trapped electrons into the dielectric conduction band. By plotting $ln(I_L)$ from SiN-SiOC structure as a function of $1/T$ for 5 different electric fields as shown in Figure 4.23(a), the height of the trap potential well, ϕ_t in SiN/SiOC interface can be obtained. The values of electric field were selected such as to correspond to conditions at which P-F or Schottky emission is dominant. The straight line fit supports P-F emission mechanism in Cu comb capacitor. On the other hand, Schotkky emission is due to thermionic emission of electron from metal electrode over the potential energy barrier into the conduction band of the dielectric. To obtain the Schottky barrier height, ϕ_B of Ta/SiOC interface, $ln(I_L/T^2)$ vs. $1/T$ was plotted for 5 different electric fields from SiC-SiOC structure as shown in Figure 4.23(b). Again, straight lines can be drawn from the data points which confirm the existence of Schottky emission in SiC-SiOC structure.

In deriving the trap potential well height, it has to be noted that ϕ_t is related to the square root of E_f as mentioned earlier in Section 4.1.1, as such, the values of ϕ_t can be obtained graphically. Also, the value of ϕ_B is dependent on the square root of E_f and it can be easily obtained from the slopes of the fitted straight lines, m_S from Figure 4.23(b) which is described as:

$$m_S = \frac{-q(\phi_B - \sqrt{qE_f / 4\pi\varepsilon_i})}{k} \tag{4.7}$$

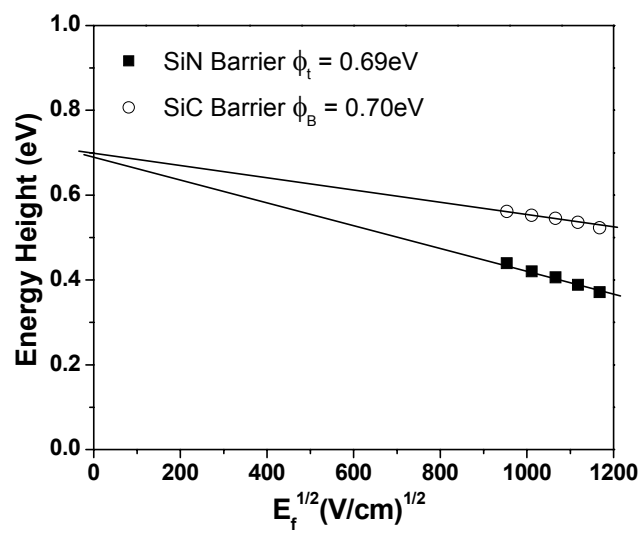


Figure 4.24: Graphical determination of P-F trap potential height, ϕ_t and Schottky barrier height, ϕ_B.

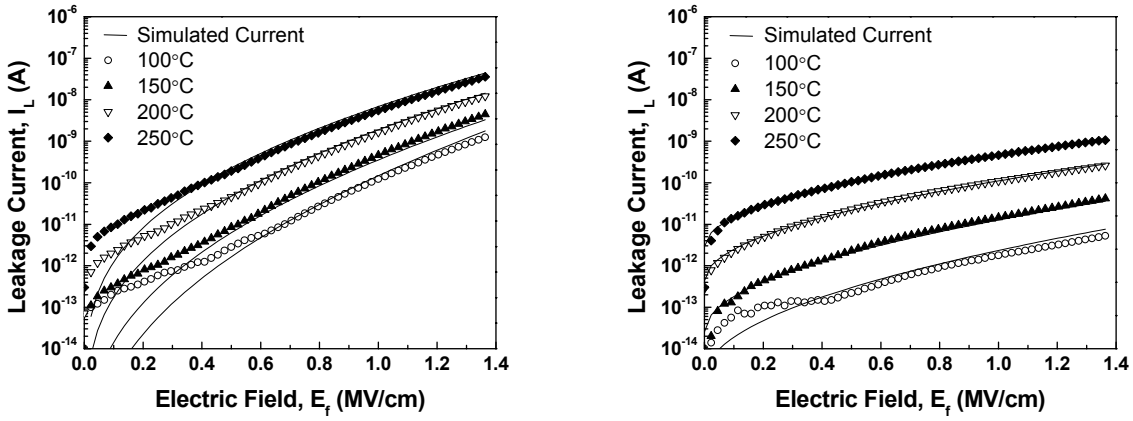
To verify this field dependence and to extract ϕ_t and ϕ_B, the energy height values of $-km_{PF}/q$ and $-km_S/q$ were plotted with $E_f^{1/2}$ as shown in Figure 4.24. From the y-intercepts of the curves, ϕ_t in SiN/SiOC interface with SiN barrier is approximately 0.69

eV while ϕ_B over Ta/SiOC interface with SiC barrier is around 0.70 eV. Surprisingly, the values of ϕ_t and ϕ_B are very close to each other. Since the fabrication process conditions and the structural dimensions of the comb capacitors are the same, we propose that in SiN-SiOC structures, in addition to P-F emission, Schottky emission may happen simultaneously. But because of larger leakage in SiN-SiOC by at least an order of magnitude, P-F emission can overwhelm Schottky emission.

Table 4.9: Values of pre-exponential factor, C_1' of P-F emission in SiN-SiOC structure and pre-exponential factor, AA^* of Schottky emission in SiC-SiOC structure.

Dielectric Barrier	**Poole-Frenkel Pre-exponential factor, C_1'**	**Schottky Pre-exponential factor, AA^***
SiN	7.1 (±1.2) × 10^{-11} $AV^{-1}cm$	-
SiC	-	3.9 (±0.5) × 10^{-10} AK^{-2}

From the y-intercepts of the curves in Figure 4.23(a) and (b), the pre-exponential factor, C_1' of P-F emission equation (Equation 4.2) and AA^* of Schottky emission equation (Equation 4.1) were obtained and listed in Table 4.9. Together with the derived values of energy heights, ϕ_t, ϕ_B and dielectric constant, k, I_L-E_f curves (Figure 4.18) in the whole range of voltages and temperatures (except room temperature) were simulated using Equations (4.1) and (4.2). Figure 4.25(a) and (b) show the close fit of experimental and simulated currents.



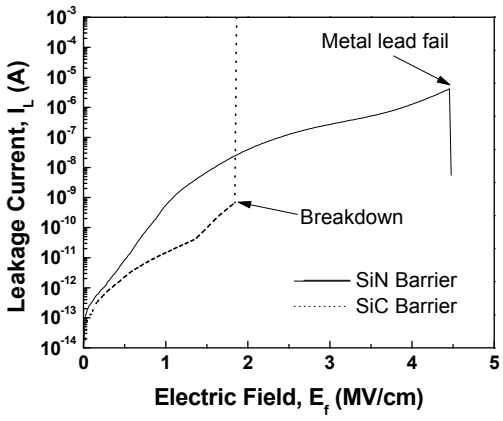
(a) (b)

Figure 4.25 Comparison of experimental (symbols) and simulated (lines) currents of structures using (a) SiN and (b) SiC as barriers.

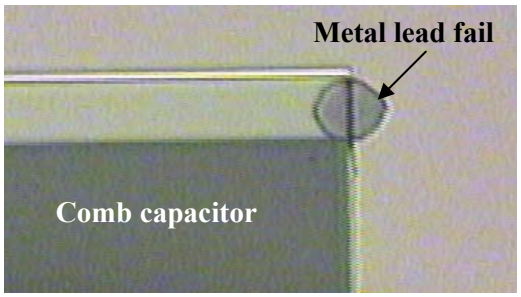
4.2.5 Breakdown Strength

A comparison between the breakdown strength of structures (with identical metal-to-metal spacing) using SiN and SiC barriers is shown in Figure 4.26. As mentioned earlier in the previous section, leakage current is greatly suppressed by the use of SiC barrier in replacement of conventionally used SiN barrier. However, when comparing the breakdown strength (the breakdown condition is defined as a sudden rise in leakage current of at least 1 order in magnitude), at temperature of 150°C, SiC-SiOC comb capacitor breaks down at ~2MV/cm while SiN-SiOC comb capacitor survives >4MV/cm before the metal leading to the capacitors fails resulting in open circuit and sudden drop of current. The metal lead failure is most likely due to the enhancement of local electric field at the metal-lead corners causing an unexpected failure in SiN-SiOC structure; this was also similarly observed by Noguchi *et al.* [13]. Although we cannot quantify the

breakdown strength of SiN-SiOC comb capacitor, still, we can qualitatively conclude that SiN-SiOC structure is showing higher breakdown strength than SiC-SiOC structure.



(a)



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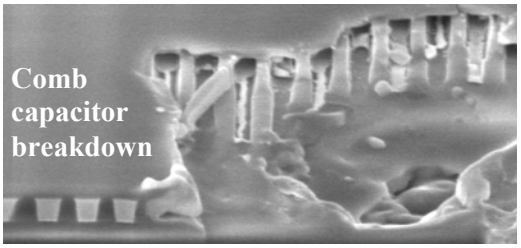


(c)

Figure 4.26: (a) I_L-E_f characteristics of Cu/SiOC comb capacitor structures with SiN and SiC barrier layers at 150°C until capacitor breakdown. (b) Top view picture (from optical microscope) showing failure spot at the corner of the metal line leading to comb capacitor structure. (c) SEM cross-sectional picture showing typical comb capacitor breakdown producing melting and fusion of Cu metals and SiOC dielectrics.

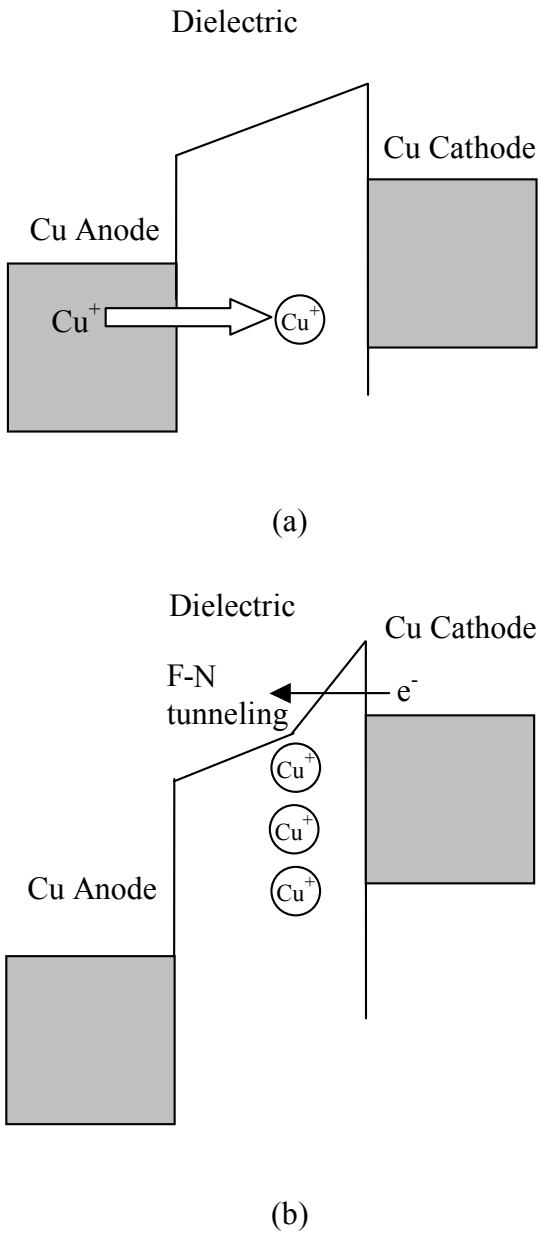


Figure 4.27: Schematic energy band diagrams of dielectric breakdown mechanism in Cu/SiOC damascene structure.

Yiang *et al*. [19] reported that Fowler-Nordheim (F-N) tunneling plays an important role in dielectric breakdown and the high electrical stress in this tunneling regime is the major cause of dielectric breakdown in Cu/SiOC damascene structures. Based on this theory, a

new dielectric breakdown model in Cu damascene structure is proposed and the schematic band diagrams are shown in Figure 4.27. At very high electric field prior to dielectric breakdown, Cu ions from the anode are drifted towards the cathode. As more Cu ions get injected into the dielectric, the electric field near the cathode is increased and results in enhanced electron injection by Fowler-Nordheim (F-N) tunneling. When a critical number of accumulated Cu ions are locally reached, the final runaway process happens and leads to dielectric breakdown and total destruction of the Cu comb capacitor structures. Since Cu ions are the major source of dielectric breakdown, the ability to block Cu penetration ultimately determines the breakdown strength of Cu/SiOC damascene structure. This model corresponds well with our experimental data of which SiN-SiOC structure has a better breakdown strength than SiC-SiOC structure because SiN has a better barrier performance than SiC (Section 4.2.3).

4.2.6 TDDB

TDDB tests were conducted at constant temperature and varying electric field stress ranged from 1.75 MV/cm to 2.25 MV/cm; and at constant electric field stress and varying temperature ranged from 85°C to 150°C such that values of field acceleration factor and activation energy can be obtained. The TDDB results were well-fit by Weibull statistical distribution and the results are shown in Figure 4.28.

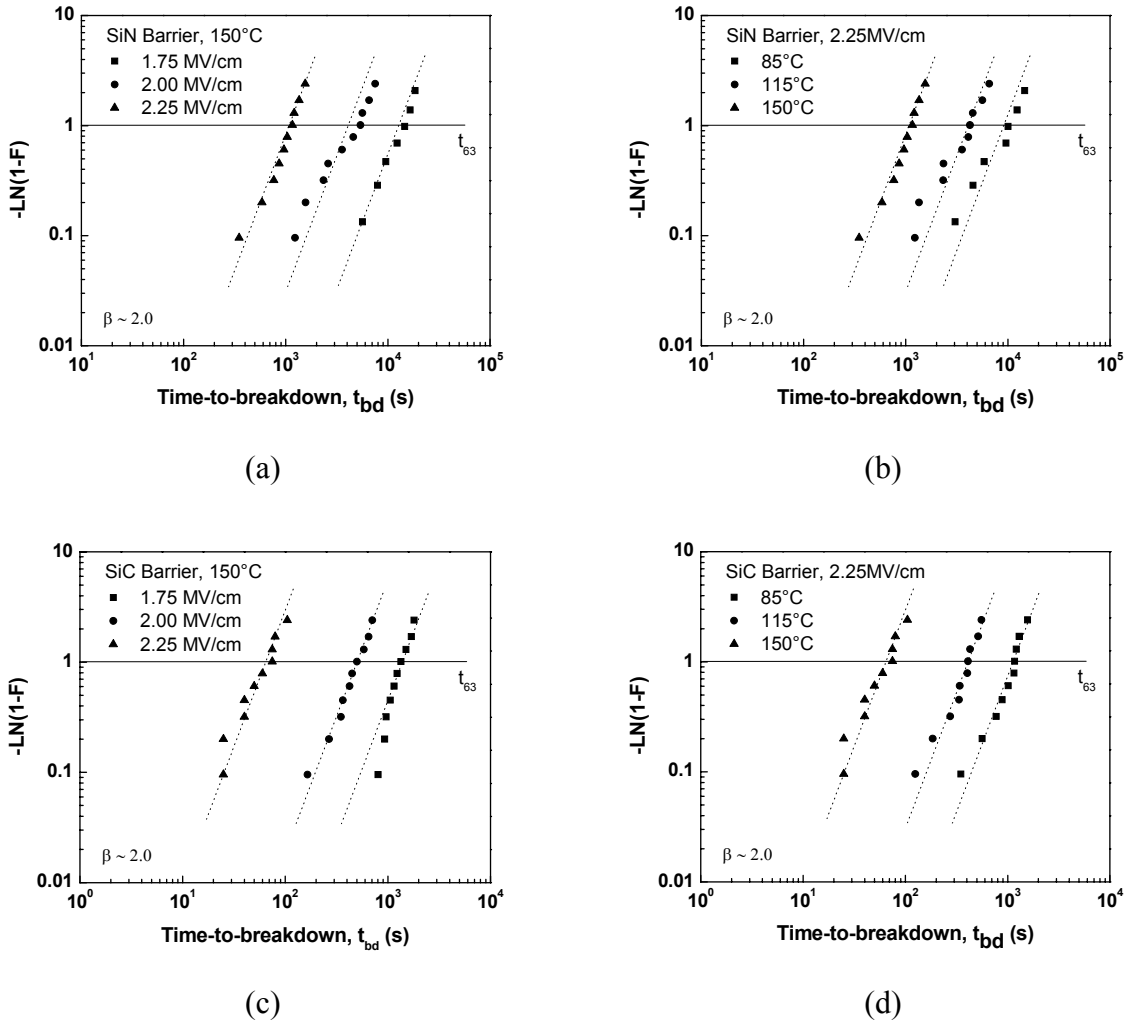
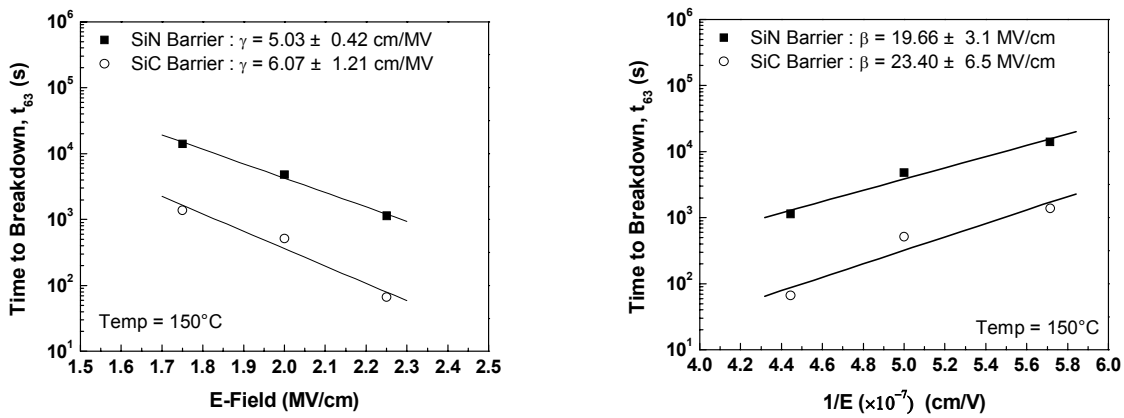


Figure 4.28: TDDB lifetime failure Weibull plots of intra-level comb capacitors with (a) SiN barrier at 150°C and varying electric field, (b) SiN barrier at 2.25MV/cm and varying temperature, (c) SiC barrier at 150°C and varying electric field and (d) SiC barrier at 2.25MV/cm and varying temperature.

These time-to-failure results indicate that structures with SiN barrier have a better TDDB lifetime performance than those with SiC barrier. Also, the Weibull shape parameters, β for the different barriers are very similar ($\beta \sim 2.0$). Based on percolation model for porous low-*k* breakdown, Ogawa *et al.* [11] concluded that the value of Weibull shape parameter is closely related to the porosity of the low-*k* dielectric. Hence, the almost identical

Weibull shape parameters obtained in our results suggest that the replacement of dielectric barrier from SiN to SiC has no effect on the porosity of the underlying low-*k* SiOC.



(a) (b)

Figure 4.29: (a) Determination of field acceleration factor, γ from *E*-model of comb capacitor structures with SiN and SiC barriers. (b) Determination of field acceleration factor, *G* from *1/E*-model of comb capacitor structures with SiN and SiC barriers.

The characteristic time-to-breakdown (t_{63}) data were plotted against electric field to describe *E*-model (as shown in Figure 4.29(a)) and the inverse of electric field to describe *1/E* model (as shown in Figure 4.29(b)). At 150°C, the field acceleration factor, γ obtained from *E*-model are 5.03 ± 0.42 cm/MV for SiN-SiOC structures and 6.07 ± 1.21 cm/MV for SiC-SiOC structures while the field acceleration factor, *G* obtained from *1/E*-model are 19.66 ± 3.12 MV/cm for SiN-SiOC structures and 23.40 ± 6.51 MV/cm for SiC-SiOC structures. For comparison, thick (>100Å) SiO_2 films was reported to have significantly higher γ (>6.0 cm/MV) [22] and higher *G* (~350 MV/cm) [53].

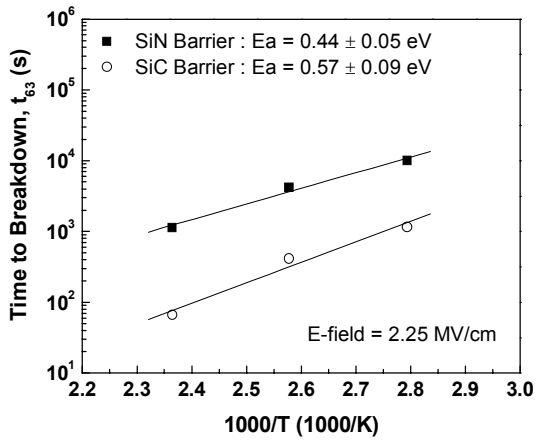


Figure 4.30: Determination of activation energy, E_a from Arrhenius plot of comb capacitor structures with SiN and SiC barriers.

From Figure 4.30, the activation energies, E_a derived from the Arrhenius plot are 0.44 ± 0.05eV and 0.57 ± 0.09eV for structures with SiN barrier and SiC barrier respectively. For comparison, E_a reported for SiO_2 was ~1.8eV at electric fields in the 1-3 MV/cm range [53].

Which model best describes BEOL low-*k* TDDB degradation? With SiN or SiC barrier used, our TDDB results show similar values of Weibull shape parameter, field acceleration factor (from both *E* and *1/E* models) and activation energy. All these tend to suggest that regardless of different barriers being used, the TDDB failure kinetics should be the same, but the change in barrier materials has major impact on the magnitude of time-to-breakdown as well as the breakdown strength (Section 4.2.5). We attributed these TDDB observations to Cu ion drift of which the ability of barrier against Cu ion penetration ultimately decides the TDDB performance. Similar to voltage breakdown

mechanism (Figure 4.27), the Cu ions that are injected into the low-*k* SiOC serve to increase the electric field near the Cu cathode. As more and more Cu ions get accumulated, it enhances the electron injection from the cathode by F-N tunneling into the conduction band of low-*k* SiOC. It is proposed that the final breakdown occurs when there is a rapid rise in current due to F-N current conduction causing severe Joule heating and formation of a melt filament shorting both electrodes. Since the theory of Cu ion drift and F-N current conduction best explains back-end low-*k* TDDB degradation mechanism, *1/E* model should be the more appropriate model to use.

In short, because SiN has a better barrier performance than SiC (refer to Section 4.2.3), structures using SiN barrier should have a better TDDB lifetime performance; and this corresponds well with our experimental data.

4.2.7 Soft Breakdown

During most of the TDDB tests carried out in SiC-SiOC structures, at low electric field stress (E_f < 1.75MV/cm), two different TDDB degradation mechanisms were observed: soft breakdown and hard breakdown. Figure 4.31 shows the occurrence of soft and hard breakdowns under the constant electric field stress condition of 1.25MV/cm at 150°C. Analogous to soft breakdown in gate oxide reliability [54], [55], soft breakdown in back-end dielectric is detected as the first abrupt increase of leakage current from the initial value to a μA level while hard breakdown is denoted as the breakdown which causes the

leakage current to reach the compliance mA level. Prior to the initial sudden increase of leakage current in soft breakdown, it can be observed that leakage current level is quite stable. However, immediately after the first soft breakdown, a region of high degree of current fluctuation from approximately 10^{-7} A to 10^{-5} A was detected. The region of fluctuation suggests the occurrence of multiple soft breakdowns as Cu is continuously migrating from the anodes to the cathodes, shorting the Cu capacitors thereby creating excess leakage pathways which will ultimately lead to catastrophic hard breakdown. These current fluctuations phenomenon corresponds to the observation reported by [56], [57] in front-end gate oxide.

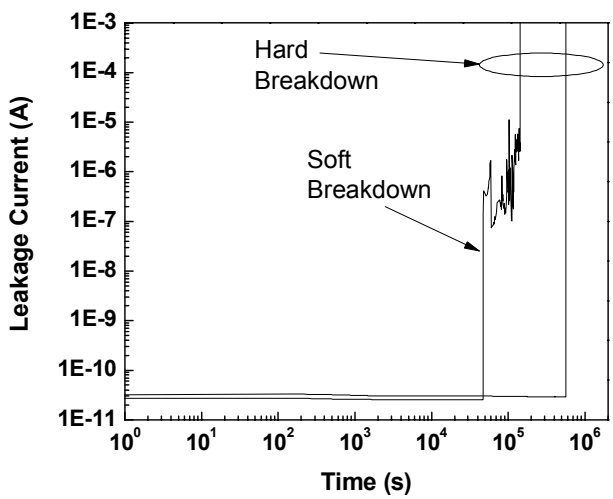


Figure 4.31: I_L-t plot of SiC-SiOC structures at 1.25MV/cm constant electric field stress and 150°C showing two different types of breakdown which are the sudden increase of leakage current to μA level soft breakdown and the final hard breakdown to mA compliance level.

Is soft breakdown in Cu/low-*k* intra-level capacitor recoverable? To verify this, post soft breakdown I_L-E_f characteristics were measured and presented in Figure 4.32. Soft

breakdown is clearly an irrecoverable failure and it can be seen from SEM images that permanent leakage paths have been formed (Figure 4.33) at the onset of soft breakdown which causes leakage current to rise greatly from pA to μA level.

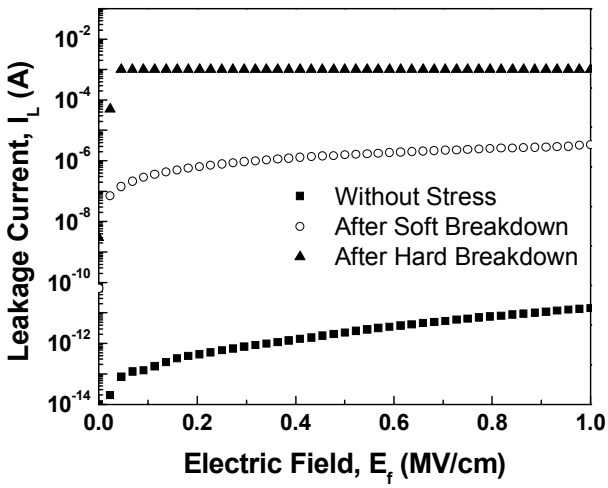
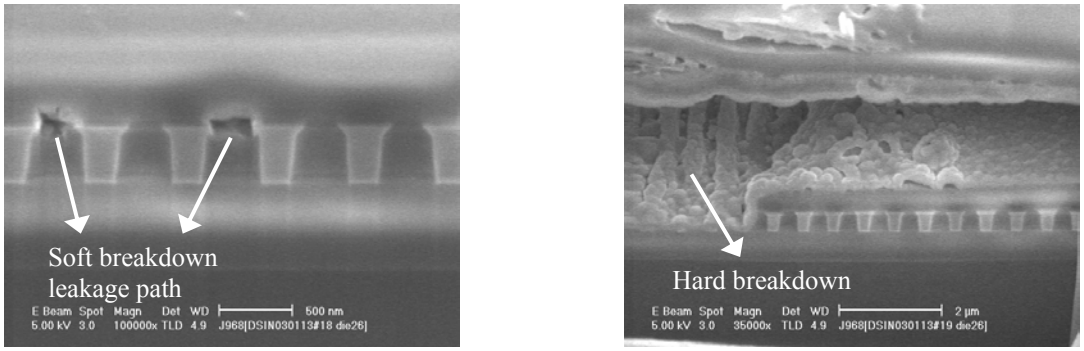


Figure 4.32: Comparison of I_L-E_f curves at temperature of 150°C after the occurrence of soft breakdown and hard breakdown.



(a) (b)

Figure 4.33: SEM cross-sectional image showing (a) the formation of permanent leakage path along the upper interface of SiC barrier and SiOC dielectric after soft breakdown, (b) the severe Joule heating causing melting of Cu lines, their adjacent dielectrics and shorting the electrodes after hard breakdown.

It should be noted that not all structures exhibited soft breakdown during TDDB test and statistics indicates that when the electric field stress is low, soft breakdown is easier to be detected. From Figure 4.34, it can be noticed that at low stress field of 1.25MV/cm, the percentage of occurrence of soft breakdown is 64.3% compared to only 20% at higher field of 1.50MV/cm and practically no soft breakdown was detected at *E*-field ≥ 1.75MV/cm. This can be explained by the reduced thermal effects for lower applied *E*-field [54]. Also, only SiC-SiOC structures showed soft breakdown characteristics and practically no soft breakdown was observed in SiN-SiOC structures and other structures using USG as dielectric. This again, indicates the poor barrier performance of SiC.

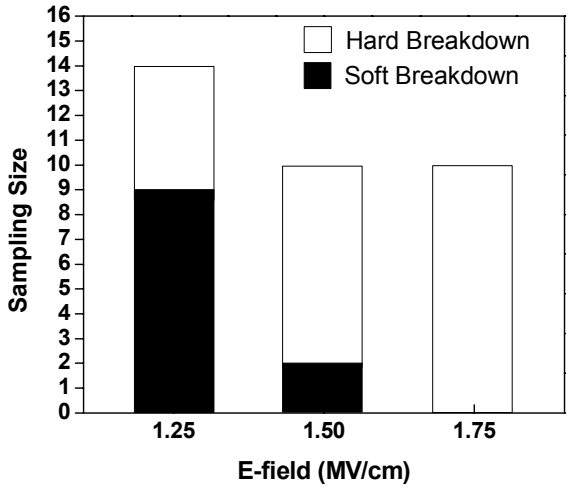
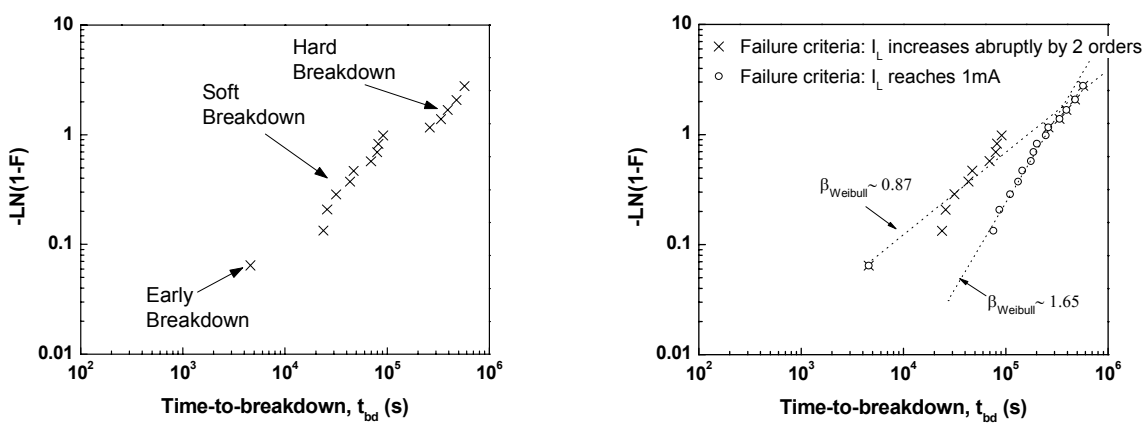


Figure 4.34: Comparison of the relative contribution of hard and soft breakdowns as a function of different constant *E*-field stress at 150°C.

The occurrence of soft breakdown poses a practical measurement problem. In conventional intra-level TDDB reliability assessment of Cu capacitors, the time to reach

a leakage current level of 1mA is typically used as the time to failure. Since soft breakdown is a permanent failure, we should take into account the impact of soft breakdown by changing the breakdown criteria to the time at which the leakage current rises abruptly by at least 2 orders of magnitude. Figure 4.35(a) explains the different breakdown modes at different time-to-breakdown regions in the Weibull distribution of TDDB data obtained from 1.25MV/cm electric field stress at 150°C. By comparing the different breakdown criteria as shown in Figure 4.35(b), we notice that a gentler Weibull slope ($\beta \sim 0.87$) will be obtained if we consider soft breakdown as failure while a steeper slope ($\beta \sim 1.65$) will be obtained if we only consider hard breakdown as failure. The irregular occurrence of soft breakdown causes the analysis of the Weibull plot to be rather complicated and hence, extra care has to be taken when setting the failure criteria and analyzing the statistical Weibull plot of TDDB data.



(a) (b)

Figure 4.35: Weibull distribution of TDDB data obtained from constant 1.25MV/cm stress at 150°C showing the (a) different breakdown modes and (b) the contribution of soft breakdown to the overall Weibull shape parameter, β.

CHAPTER 5

CONCLUSION

5.1 Conclusion

In summary, dielectric reliability assessment of intra-level Cu comb capacitor structures is challenging because of a combination of many factors such as the fringing capacitances, the non-uniform distribution of electric and stress fields, the multistack dielectrics, the intrinsic BEOL dielectric material, the Cu drift into the dielectric as well as the interface trap density. Varying some of the process steps such as surface treatments and use of different dielectric barriers besides enhancing dielectric reliability performance also led to the identification of the origin of the leakage currents, probable leakage pathways and the dielectric breakdown mechanisms in intra-level Cu interconnects.

Electrical characterization was performed on intra-level Cu comb capacitor test structures with different surface treatments. For structures with NH_3 and H_2 treatments, the dielectric reliability performance was greatly improved relative to structure with no treatment. By modeling the leakage current data with the different types of conduction mechanisms, we found that Poole-Frenkel (P-F) saturation effect occurs for structures with NH_3 and H_2 treatments. This shows that the improved leakage current performance is due to a reduction of interface trap density which is responsible for the electrical conduction in intra-level Cu capacitor. Also, the improvement of time-dependent

dielectric breakdown (TDDB) for structures with NH_3 and H_2 treatments indicates a suppression of Cu ion density which plays a dominant role in TDDB degradation mechanisms.

In another experimental split, the effect of using different dielectric barriers was studied. Based on the result of SIMS analysis, it was found that SiN has a better barrier performance against Cu diffusion than SiC. Dielectric reliability tests were carried out on intra-level comb capacitor structures integrated with SiN and SiC barriers. From the carrier transport modeling, Schottky emission was found to dominate the leakage behavior in structures with SiC barrier while P-F emission dominates in structures with SiN barrier. The relatively high leakage current due to P-F emission implies that significant amount of incomplete covalent bonds were being formed during deposition of SiN. On the other hand, because SiC is chemically similar to SiOC, there are less broken bonds in the interface regions and as a result, the intra-level leakage current measured is comparatively low and displays Schottky emission characteristics. Despite giving a high leakage current, the TDDB performance of structures using SiN barrier was in fact better than those using SiC barrier. From SIMS analysis, we know that SiN has a better Cu diffusion barrier property than SiC, and thus we could attribute the TDDB degradation mechanism to Cu drift into dielectric which enhances the electric field thereby causing electron injection by Fowler-Nordheim (F-N) tunneling and leads to eventual dielectric breakdown. Also, at low electric field stress, soft breakdown phenomenon was observed in structures with SiC barrier. From SEM images, leakage paths at the interface of SiC and SiOC, shorting both electrodes were observed. Soft breakdown is a permanent failure

and the irregular occurrence of soft breakdown causes the analysis of TDDB data to be rather complicated.

5.2 Recommendations

The following describes the future research work that can be carried out as extension of the work reported here:

1. Due to the fringing capacitances of the intra-level Cu comb capacitor, it is impossible for us to determine the dielectric constant of BEOL dielectric through direct capacitance measurement across the capacitor. To determine the *k* value of BEOL dielectric from the intra-level comb capacitors, we have to make use of the static simulation on a two-dimensional model with RAPHAEL software which is clearly discussed by Stucchi *et al.* [58]. It would be useful for us to study the effect of various surface treatments and dielectric barriers on the intrinsic *k* value of BEOL dielectric.

2. It was reported by Tsu *et al.* [10] that by monitoring the cathode and anode currents separately, during TDDB test, the breakdown mechanism due to Cu drift can be evidently identified. Prior to reaching a steady state of the Cu drift, we can observe a distinct difference between cathode and anode currents. However, due to limitation of the TDDB system, we are unable to measure both anode and

cathode currents separately. The TDDB system can be modified to fit this requirement.

5.3 Publications

1. V. C. Ngwan, C. Zhu and A. Krishnamoorthy, "Dependence of leakage mechanisms on dielectric barrier in Cu-SiOC damascene interconnects", Applied Physics Letters, vol. 84, no. 13, pp. 2316-2318, 2004.

2. V. C. Ngwan, C. Zhu and A. Krishnamoorthy, "Analysis of leakage mechanisms and leakage pathways in intra-level Cu interconeects", IEEE International Reliability Physics Symposium, 2004, Phoenix, Arizona.

3. V. C. Ngwan, C. Zhu and A. Krishnamoorthy, "Effect of surface treatments on dielectric leakage and breakdown of copper damascene interconnects", 2nd International Conference on Materials for Advanced Technologies, 2003, Singapore.

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