IF SAMPLING RECEIVER FRONT END DESIGN

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Summary

A high speed CMOS IF sampling receiver for digital wireless application is described in this thesis. The receiver consists of a continuous-time IF amplifier, a subsampling switched-capacitor gain stage and a fourth-order bandpass sigma-delta A/D converter. Due to its IF sampling nature, the receiver is highly immune to dc offset, flicker noise and errors due to mismatches between *I* and *Q* signal paths. The receiver is implemented in a 0.6um, double-poly, triple-mental CMOS process, and operated from a 3.3-V power supply. For a 210-MHz input signal, the measured result show that the receiver can achieve a 48-dB dynamic range over a 200kHz bandwith centered at 10MHz when sampled at 40MHz. The power dissipation of the receiver is 69.3mW.

Keywords:
IF sampling, analog-to-digital conversion, bandpass sigma-delta modulation, switched-capacitor, track&hold, intermediate frequency.

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Chapter 1: Introduction

As a key part in wireless communication system, the Radio Frequency (RF) receiver has attracted great research attention. Recent efforts in the design of RF receiver have focused on increasing integration and flexibility using a low cost technology (e.g. CMOS) to reduce analog circuitry. One way of reducing the analog circuitry is to replace the dual baseband A/D converters with a single IF sampling A/D converter. This allows not only the reduction of analog circuitry, but also a greater flexibility, which is important in the future to make the receiver compatible to multiple standards.

In this chapter, the conventional super-heterodyne and IF sampling receiver architectures are briefly described. Their advantages and disadvantages are discussed. An IF sampling receiver based on subsampling gain stage and bandpass sigma-delta A/D converter is then proposed for a high level integration and IF digitization with subsequent *I/Q* extraction and channel-select filtering in the digital domain. Finally, the scope and the organization of this thesis are presented.

1.1 Conventional Superheterodyne Receiver Architecture

The conventional superheterodyne has a good sensitivity and selection. In order to appreciate the advantage of the IF sampling receiver based on sigma-delta bandpass modulator, let us mainly review the difficulties and drawbacks in the conventional superheterodyne architecture

As shown in Figure 1, a double-conversion, or dual-IF, superheterodyne receiver based on the baseband A/D converter[Carlson86] comprises a tunable bandpass filter, a low-noise amplifier (LNA), which reduces the input-referred noise contributions of subsequent stages in the receiver, and two stages of mixing, intermediate frequency filtering and amplification. Following the second IF, the signal is multiplied by the two carries that are 90^o out of phase in order demodulate the signal into its *I* and *Q* components. The *I* and *Q* signals are then digitized at baseband by the two parallel lowpass A/D converters.

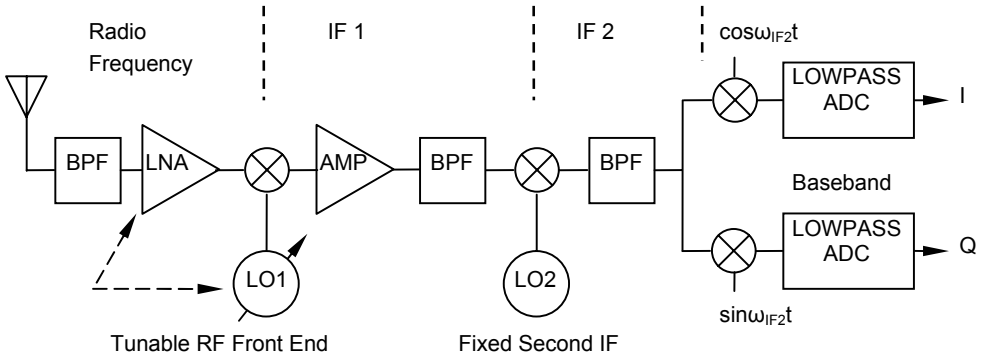


Figure 1: Superheterodyne receiver architecture with dual-IF and baseband A/D converter

The primary issue in the architecture of Figure 1 is that they suffer from the phase and gain mismatch between upper and the lower signal paths. It can be proved that the degree of the mirror-image rejection, IR, is calculated by [Ong98]:

$$IR = \frac{P_{im}}{P_{des}} = \frac{\left| j\vartheta \frac{A}{4} \right|^2}{\left| \frac{A}{2}\left(1 + j\frac{\vartheta}{2}\right) \right|^2} = \frac{\vartheta^2}{4\left(1+\vartheta^2/4\right)} \approx \frac{\vartheta^2}{4} \quad , \quad \vartheta \le 1. \tag{1.1}$$

which ϑ radian ($\vartheta \le \pi/2$) ia a deviation of phase between two mixer and A is the amplitude in local oscillators.

Without special trimming or analog tuning techniques, it is difficult to reduce the phase error between the LO signals to below 1^o [Stetzler95]. Therefore, assuming a phase error of 1^o, the unwanted mirror signal will be suppressed by approximately 40dB.

A similar analysis that accounts for amplitude imbalance in the local oscillators can be carried out to yield

$$IR = \frac{(\Delta A/A)^2}{4} \tag{1.2}$$

Where ΔA/A denotes that the relatively amplitude difference between the two local oscillator signals without nominally equal amplitude [Razavi98]. So these types of receivers require peripheral circuitry to perform dc offset cancellation and gain calibration between two mix paths.

1.2 Conventional IF Sampling Receiver Architecture

Most of the errors from analog circuitry in the back-end of a superheterodyne receiver can be avoided by digitizing the signal at an intermediate frequency rather than at baseband. In the Traditional IF sampling receiver architecture depicted in Figure 2, the RF signal enters at the antenna and is mixed through two stages and broadly filtered before being digitized at the second-IF location by a bandpass A/D converter.

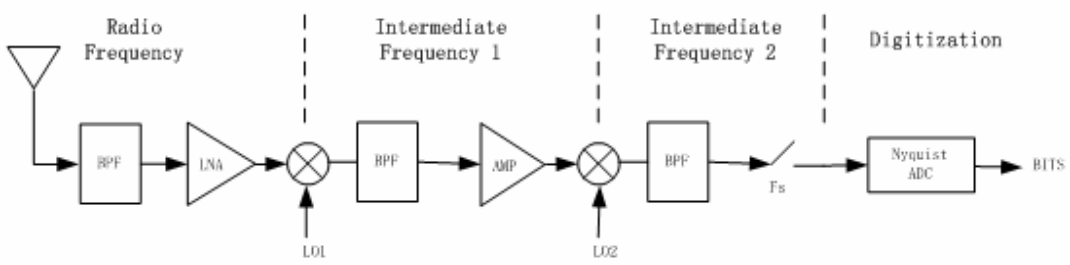


Figure 2: Traditional IF sampling receiver architecture

The IF sampling receiver confers several advantages.

First, the I and Q components of the signal are separated in the digital domain rather than in the analog domain. Consequently, the quality of the downconversion is not compromised by analog imperfections such as mismatch between the I and Q paths or the need to implement precise analog mixers. In fact, if the A/D converter's sampling frequency, f_s, is chosen to be 4 times the carries frequency of the desired signal, f_{IF2}, then I/Q demodulation in the digital domain becomes a trivial matter of the multiplication by 1, 0 and -1, as illustrated in Figure 3[Ong98].

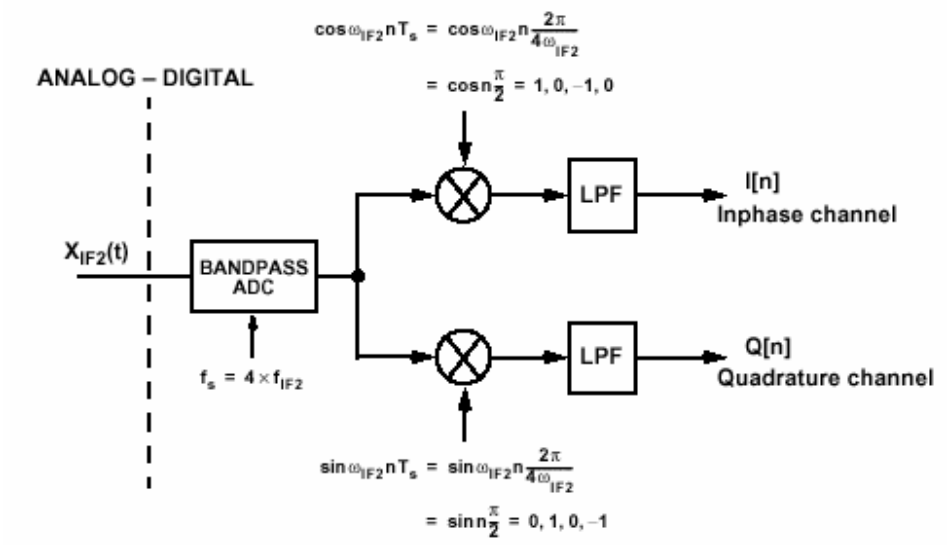


Figure 3: Digital I/Q demodulation of a signal centered at fs/4

Second, digitizing the desired signal, f_{IF2}, in the intermediate frequency can avoid the problems of the low frequency (*1/f*) noise and dc offset. This results in a higher level of integration and eliminates the need for dc offset cancellation and I/Q gain calibration. However, traditional IF sampling receivers make use of a high-speed Nyquist-rate A/D converter digitize the entire frequency band from dc to *fs/2*, where *fs* is the sampling frequency of the converter. According to the Nyquist sampling theorem, the sampling rate *fs* of the A/D converter must be at least twice of the highest input frequency in order to recover or represent the original waveform[Robert85]. Because the bandwidth of the IF signal is typically a small fraction of the carrier frequency, the use of the wideband Nyquist-rate converter doesn't result in the optimum solution for digitizing the IF signal and it also limit the frequency of the input signal. An optimum solution for digitizing a narrowband IF signal is an A/D converter which provides high resolution in the narrow band of interest and is capable of handling lager out-of-band signal.

1.3 Proposed IF Sampling Receiver Architecture

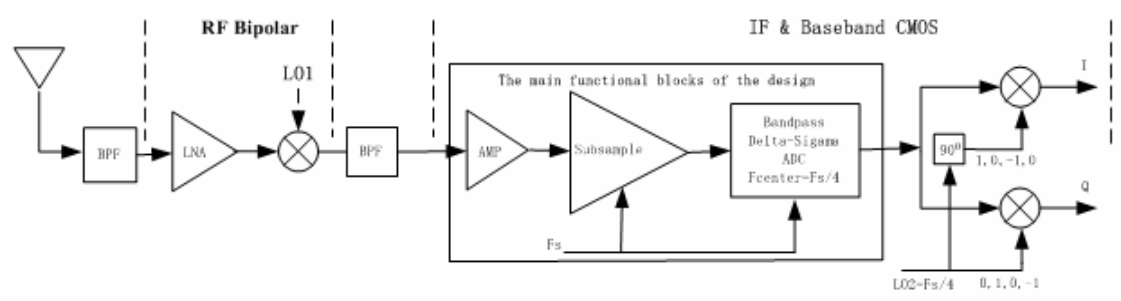


Figure 4: Proposed IF sampling receiver architecture

Bandpass sigma-delta modulators offer an attractive approach as they can perform a high resolution A/D conversion of a high frequency signal with a narrow bandwith [Bazarjani98]. Due to their oversampling and noise shaping nature, bandpass sigma-delta converters provide the most optimum solution for performing analog to digital conversion on narrow band IF signal. By digitizing only the band of the interest and not the entire Nyquist band, bandpass sigma-delta A/D converters provide high dynamic range with relatively low power consumption.

The proposed IF sampling receiver based on subsampling gain stage and sigma-delta bandpass modulator is showed in Figure 4. The IF and the baseband sections are combined and the analog to digital conversion is performed at an IF frequency using a bandpass sigma-delta A/D converter. This results in a higher level of integration and eliminates the need for dc offset cancellation and 1/Q gain calibration.

The second mixer in this architecture is a sampling stage which downconverts the signal from the first IF to the second IF. The second IF signal is then digitized by a bandpass sigma-delta A/D converter. The output of the bandpass A/D converter is passed

on to quadrature digital mixers which perform the final downconvesion and generate the baseband I and Q components.

The center frequency of the bandpass A/D converter is designed to be at the second IF or *fs*/4. This greatly simplifies the design of the digital mixer. The sampling frequency *Fs* which is normally a multiple of the output sampling rate, dictates the location of the first IF. With this frequency plan, the first IF should be an odd multiple of *fs*/4. These will be discussed in detail in the following chapter.

1.4 Objective and Specification

The main objective of this project is to design and implement the proposed IF sampling receiver. The emphasis in this research is on the performance of the IF sampling receiver at high sampling speeds and high input frequency (>200MHz). As showed in Figure 4:, the main functional blocks of the design consist of a continuous-time IF amplifier, a subsampling gain stage and a bandpass sigma-delta modulator.

The realization of the subsampling gain stage and sigma-delta bandpass modulator is based on the switched-capacitor technique. In order to simplify the design and analysis of the IF sampling receiver, the second intermediate frequency is designed at 10MHz. The sampling frequency *fs* is at 4 times of second IF or 40MHz. This results in an easy digital quadrature demodulation and allows a simple low-pass to band-pass transformation.

RF signal are usually demodulated from GHz band to a first intermediate frequency around 200MHz. As mentioned in the previous section, the first IF should be an odd multiple of the second IF. In this case the first IF is 21 times the second IF or 210MHz.

With a sampling frequency of 40MHz, it is possible to convert for example the GSM channels with channel spacing of 200KHz, with the required resolution of 9 bits, corresponding to a dynamic range of 56dB.

The specifications of the IF sampling receiver are listed as follows:

Supply voltage: 3.3 V

The input signal frequency: 210MHz

The second intermediate frequency: 10MHz

The sampling frequency: 40MHz

Signal bandwith: 200KHz

Dynamic range: 56dB

Technology: 0.6-um, double-poly, triple-mental CMOS process.

1.5 Thesis Organization

The thesis is organized into seven chapters.

Chapter 2 introduces the fundamentals of the subsampling stage design. A differential switched-capacitor sample and hold circuit and its behavior are presented.

The basic theory of bandpass sigma-delta modulator, such as the principle of oversampling and quantization noise shaping is introduced in Chapter 3. The system-level design of a fourth-order bandpass sigma-delta modulator is presented in Chapter 4. The comparisons among the behavioral and schematic simulation are also discussed in this chapter.

Chapter 5 focuses on the circuit-level design. The key circuit blocks, including IF amplifier, operational amplifier, comparator and the clock generator circuitry, are discussed. This is followed by the simulation results of the IF receiver.

The testing results of the fabricated IF receiver chip are presented in Chapter 6.

Conclusions on this work are given in Chapter 7.

Chapter 2: Design of the Switched-Capacitor Track&Hold Circuit for Subsampling Stage

2.1 Introduction

Subsampling systems take advantages of the fact that the radio signals have a narrow bandwith than their carrier frequency in order to sample the signal at a low frequency than the one required in usual sampling. These benefits are simplified receiver architecture and good integration, less power consumption and other benefits. Nevertheless, subsampling systems have two severe drawbacks that must be taken into account for their implementation: sampling noise and aperture jitter.

This chapter treats the design of SC track&hold circuit suitable for subsampling satge in the proposed IF sampling receiver. In section 2, the theory of bandpass sampling is briefly reviewed. Then in section 3, the design the circuit is described. The factors that introduce errors into circuit are discussed in section 4 and in section 5 the simulation results are presented.

2.2 Bandpass-Sampling

The Nyquist sampling theorem, as traditionally interpreted, requires the sampling rate be at least twice the highest frequency component in the signal being sampled in order to recover or accurately represent the original waveform. Because the radio signal have a narrower bandwith than their carrier frequency, the use of a wideband converter based on Nyquist sampling theorem does not result in optimum solution for digitizing the radio signal.

The theorem of bandpass sampling [Rodney92] shows that bandpass signal of bandwith B, with a carrier frequency F_c ($F_c >> B$), should be sampled at a lower frequency than required by the traditional Nyquist sampling theorem in usual base-band sampling. If F_s is the sampling frequency, then the signal should be ideally sampled at

$$F_s \geq 2B \qquad (2.1).$$

This causes the important consequence of relaxing the constraint on the sampling frequency.

As shown in Figure 5, it is can be seen that the result of bandpass sampling produces identical replicas of the signal around all the multiples of F_s. In particular, the image that fall in [0, $F_{s/2}$] is an exact represent of the signal.

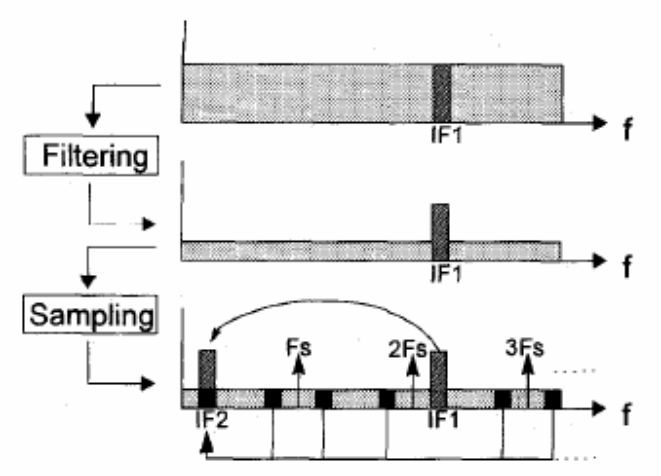


Figure 5: Susampling principle

In the IF sampling receiver, subsampling stage is utilized to down-convert the signal from *IF1* to *IF2*. Therefore, in this case:

$$IF_1 = nF_s \pm F_2, \quad \text{n=1, 2, 3....} \tag{2.2}$$

Assuming that the sampling frequency is higher than twice the channel bandwidth, no information is lost in this process. However, along with the desired channel, the wideband noise as well as all the unwanted components of the input signal will be aliased and appear between 0 and $Fs/2$. This increases the amount of noise that appears at *IF2* and degrades the signal-to-noise ratio. Therefore, in order to minimize the amount of unwanted noise that appears at *IF2*, the input signal should be filtered as much as possible before the sampling takes place.

2.3 SC Track&Hold Architecture

The constraints on track& hold circuit are severe because it must be able to follow, in the track mode, an input signal as high as 210MHz. One better way to realize such a

circuit is to perform the track&hold with a close loop architecture. The circuit in Figure 6 is a fully differential switched capacitor track&hold circuit which performs down-conversion and provides 0 and 6dB of programmable gain [Rothenberg95] [Vasseaux99]. The circuit comprises an OTA, several capacitors and MOS switches. It works with two distinct phases, *CK1* and *CK2* which correspond to the sample phase and the hold phase, respectively. This circuit can track a very high speed signal because in the sample phase, the signal only pass through the switch-on-resistances, R_{DSon} of M1 and M1' and the sampled capacitor C_s. So with an appropriate design of R_{Dson} and C_s, the circuit can track a signal as high as 210MHz.

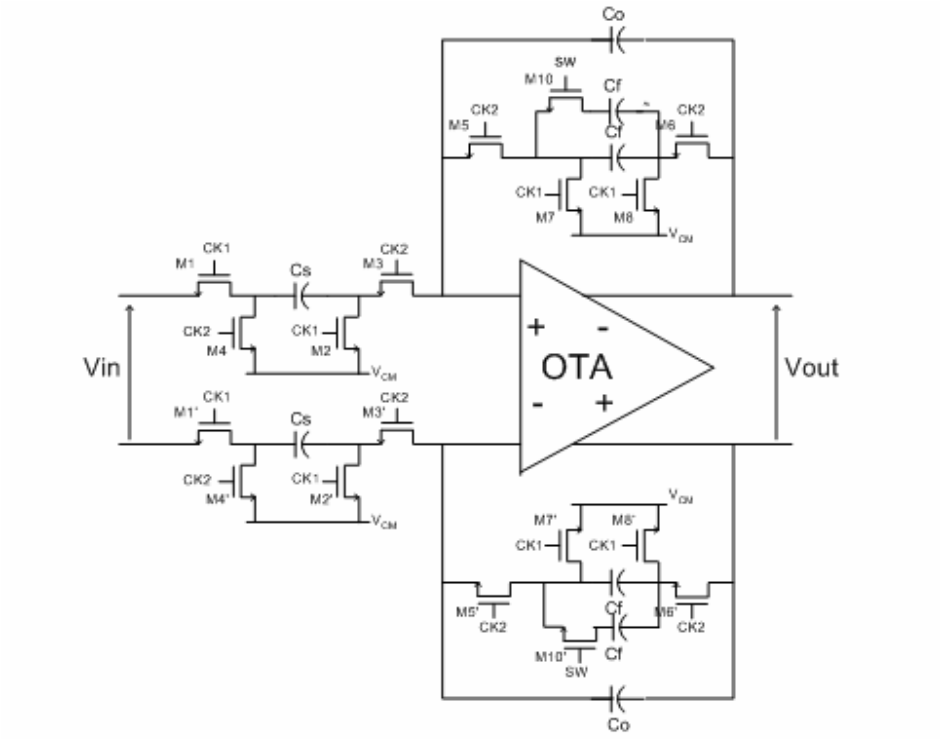


Figure 6: SC track&hold architecture

When the sw is set to 0, the operations of the SC track&hold circuit during the track and hold phase are depicted in Figure 7. During the sampling phase, *CK1*, the signal is

sampled on capacitance Cs. In the hold phase, *CK2*, sampled signal is retrieved at the output of the OTA, assisted by the virtual ground at the OTA input. In this way, the transfer function of the SC track&hold circuit is given by:

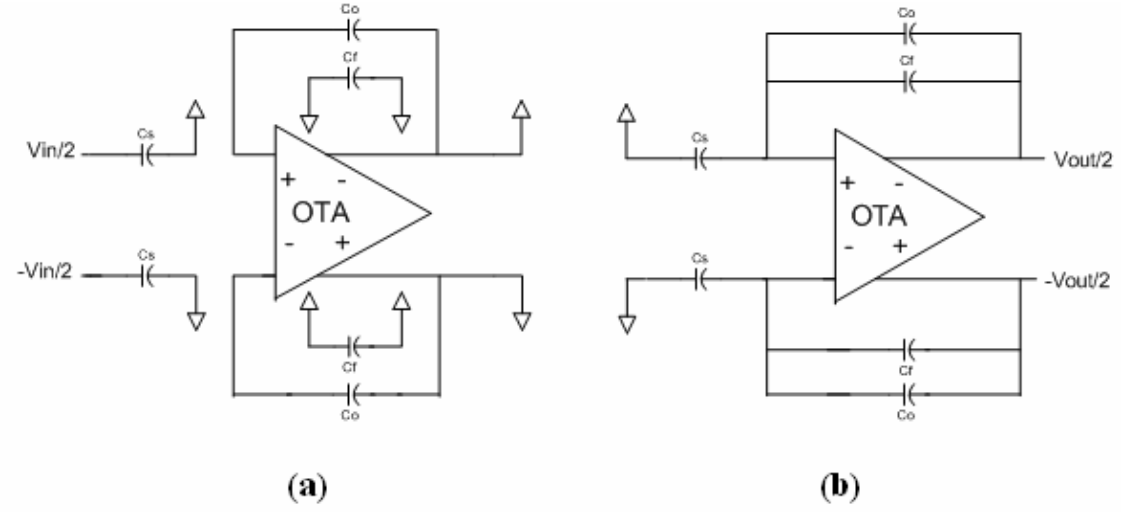


Figure 7: Operation of the track&hold circuit during (a) sampling phase, ck1; (b) holding phase, ck2

$$H(z) \approx \frac{C_s}{C_f} Z^{-1/2} \tag{2.3}$$

The capacitor C_o is used to assure that OTA is not in open loop in the interphase. By making C_o is much smaller than C_f and C_s, the E.Q(2.3) is gotten after approximation. If the value of C_s is twice of the value of C_f, the gain of circuit is approximately 6dB.

Similarly, when sw is set to 1, the transfer function of the SC track&hold circuit is given by:

$$H(z) \approx \frac{C_s}{2C_f} Z^{-1/2} \tag{2.4}$$

The gain of circuit is approximately 0dB if C_s is the twice of the value of C_f

2.4 Possible Errors into the Track&Hold Circuit

2.4.1 Settling Time

The speed of the subsampling stage during the sampling mode must be made high enough in order to avoid attenuating of the input signal. The settling time of the circuit is limited by the lowpass filter formed by the switch-on resistances, R_{DSon} and the sampling capacitors, C_s. Fast settling time requires small R_{DSon} and C_s. However, small C_s will increase the thermal noise (KT/C). With considering settling time and thermal noise, the switch-on resistances, R_{DSon} and the sample capacitor, C_s are chosen to be 144Ω and 0.8pF, respectively. Thus, the setting time is calculated to be $\tau \approx 1.444$ns, from Eq.(2.5):

$$\tau = 2R_{DSon}C_s \tag{2.5}$$

So the cut-off-frequency of the lowpass filter is 692MHz. It is enough to track a signal of 210MHz.

In the hold phase, the OTA must be sufficiently fast to settle in a half clock period. A sufficient bandwith is needed for the OTA for the desired settling accuracy. It has shown that the unity-gain bandwith, ω_0, should be (at least) five times as large as the clock frequency, ω_c [Gregorian86]. In the design, the clock frequency is 40MHz, which leads to a minimum unity-gain bandwith of 200MHz for the OTA.

2.4.2 Charge Injection

Another limitation on the precision of switched-capacitor circuit is the charge injection. This error is due to the unwanted charges injected into the circuit when transistors turn off. When MOS switches turn off, charge errors occur by two mechanisms [David97]. One is due to the channel charge, which must flow out from the channel region of the transistor to the drain and source. This charge often dominates. The other is due to the parasitic between the gate and the source or drain. The charge injection effects can be abated by adding two clock signals, ck1d and ck2d which are slightly behind ck1 and ck2, respectively. The clock scheme is shown in Figure 8. A fully differential SC Track&Hold circuit using this clock arrangement is shown in Figure 9. The reason for using this arrangement is as follows: when M1 and M1'or M4 and M4' is turn off, its charge injection will not affect the charge stored on C_s, since the right side of Cs is effectively open with the help of the delayed clock signals. when M2 and M2'or M3 and M3' is turn on, it is connected to ground or virtual ground, so the charge injections caused by M2 and M2'or M3 and M3' turned off are signal independent and can be considered as a dc offset. The system is fully differential, so this noise can be mostly rejected. Therefore, the charge injection effects are significantly reduced by using this four-phase clock scheme.

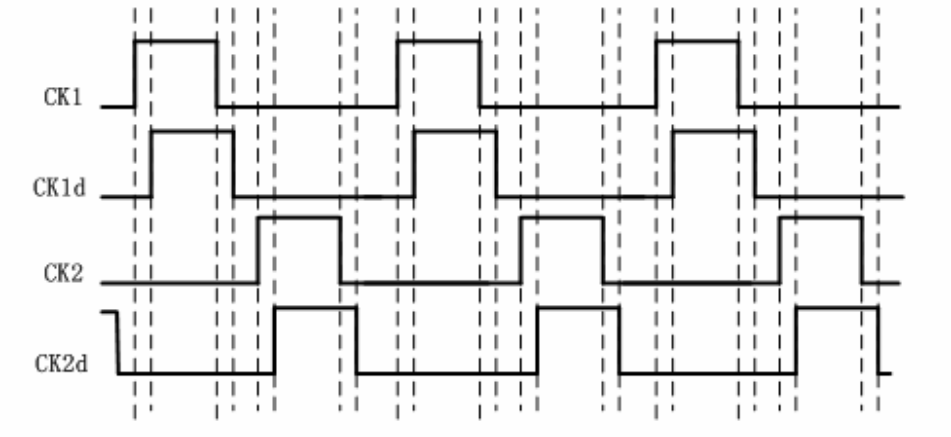


Figure 8: A four-phase clock scheme

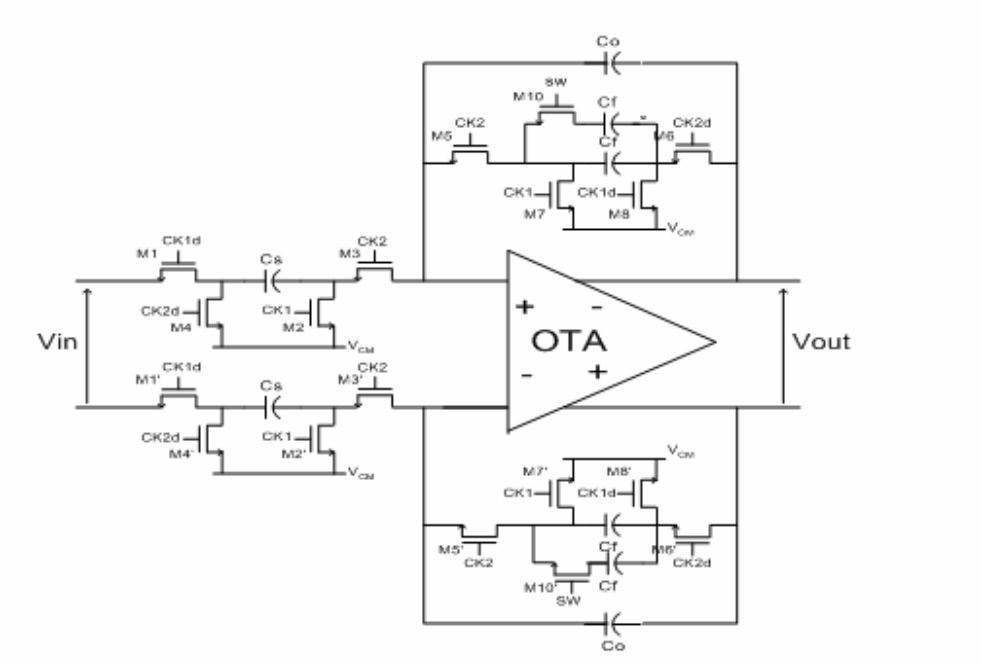


Figure 9: The SC Track&Hold circuit using four-phase clock scheme

2.4.3 Noise Sampling

First, it's reasonable to assume that the noise in the circuit mainly comes from the switches and the input MOS transistors of the OTA. As the bandwith of the OTA is

usually narrower than the bandwith of the lowpass filter formed by track&hold, noise contribution of MOS-switches can be neglected. So noise given by OTA-inputs-MOS transistors is preponderant. The OTA in our design is a single-pole amplifier with the pole-frequency in:

$$f_1 = \frac{g_m}{2\pi C} \tag{2.6}$$

where g_m is the transconductance of the input transistor and C is the total load capacitance. The noise is sampled and its power density spectrum $S^{S/H}$ at the output is given by [Gobet81], [Enz89]:

$$S^{S/H} = (\frac{T_h}{T_s})^2 \sin c^2 (fT_h) N S_0 \tag{2.7}$$

$$S_0 = 4KT(\frac{2}{3g_m}) \tag{2.8}$$

$$N \approx \frac{2.f_1}{f_s}\frac{\pi}{2} \tag{2.9}$$

where T_s is the clock period, T_h is the hold time duration, S_0 is the PDS of the OTA input-thermal noise. Because the bandwith of the OTA is greater than the sampling frequency, the thermal noise is undersampled and the noise level at the output is increased due to aliasing. So the N is the aliasing factor in E.Q. (2.7). The noise power is obtained by integration of E.Q (2.7) in the frequency band of interest:

$$P_{TOT} = \alpha KT\frac{1}{C}\frac{1}{OSR} \quad , \ \alpha \approx 1/3 \tag{2.10}$$

where $OSR = f_s/2f_b$ is the oversampling ratio of the next stage, bandpass sigma-delta ADC. It can be seen form the E.Q(2.10), it is necessary to have a great capacitance value.

However, as the time constant of the track mode $\tau = R_{on}C$ must be low enough to track a signal of 210MHz, the value of C can not be too high. The OSR in the bandpass sigma-delta ADC design is set to be 100, so the in-band noise power is about $1.7\text{x}10^{-11}\text{V}^2$ when the value of C is set to 0.8pF.

2.4.4 Aperture Jitter

Another important issue associated with the subsampling downconverters is the jitter of the sampling clock. Ideally, the signal is sampled at equal time intervals at f_s frequency. In practice, due to aperture jitter, the interval between two samples is not equal and varies randomly. This drawback increases the noise level.

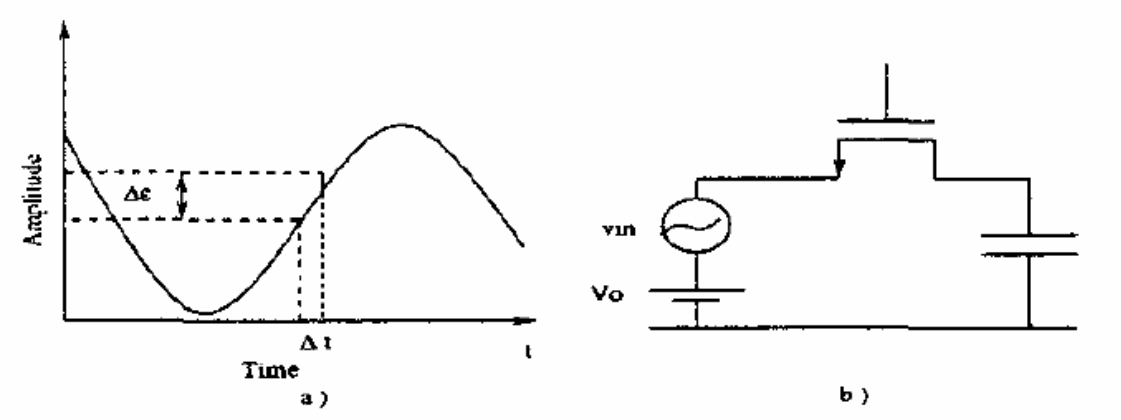


Figure 10: a) Aperture Jitter b) Basic sampler

It is possible to distinguish two causes of jitter. As shown in Figure 10, the first source is due to the instability of the oscillator that drives the switches. This jitter is treated generally as random white noise. For a sinusoidal signal V_{in} with a frequency f_{in} and an amplitude A, the signal to noise ratio SNR is given by [Shinagawa90]:

$$SNR = -10\log(2\pi^2 f_{in}^{\ 2} \overline{\Delta t_0^{\ 2}}) \tag{2.11}$$

Where f_{in} is the frequency of the signal V_{in} and Δt_0 is the time uncertainty. To reduce this jitter error, it is necessary to use a stable crystal oscillator. The second jitters source is the result of the variation of the threshold-voltage, V_{TH}, of the sampling switch with the input signal. As it has been demonstrated by [Jonsson97], in this case the aperture time Δt_v can be expressed by:

$$\Delta t_v = \frac{-V_{in} + V_{TH}(V_0) - V_{TH}(V_0, V_{in})}{a} \tag{2.12}$$

Where $V_{TH}(V0)$ and $V_{TH}(V_0, V_{in})$ are the threshold voltage without and with V_{in}. $a=Vdd/t_{fall}$ and t_{fall} is the falling time and V_{dd} is the supply voltage. Therefore Δt_v is diminished with increased V_{dd} and decreased fall time t_{fall}.

Finally to reduce the aperture jitter again, it is necessary to carefully design all the digital circuit that drive the switches.

2.5 Simulation Results

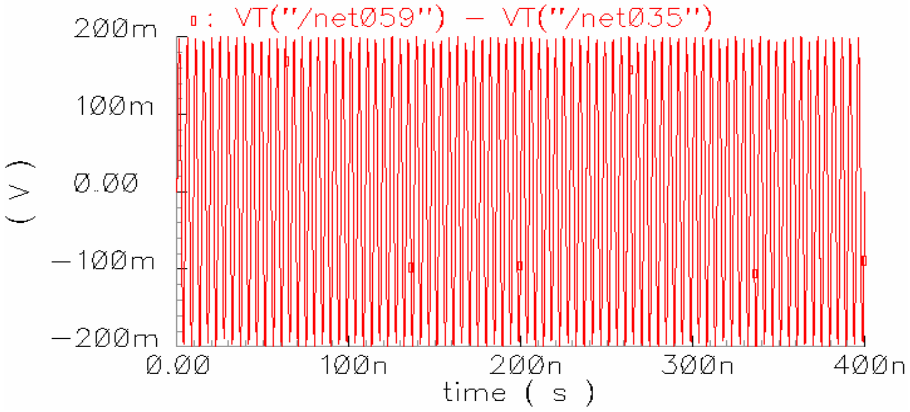
The different switch sizes and capacitor sizes in SC track&hold circuit are shown in Table 1. The switch transistors M1, M1', M2 and M2' are bigger than other switch transistors to offer a smaller switch resistance R_{DSon}. The Value of the sample capacitor, C_s, is defined based on trade-off between enough setting time and reducing the thermal noise. The capacitor C_0 is added only to assure that OTA is in close loop in the inter-phase, so its value is much lower than other capacitors.

The SC track&hold circuit for subsampling stage is operated from 3.3-V power supply and the analog ground is set to be 1.65-V. The external current of the bias circuit for OTA is set to be 200 μA .

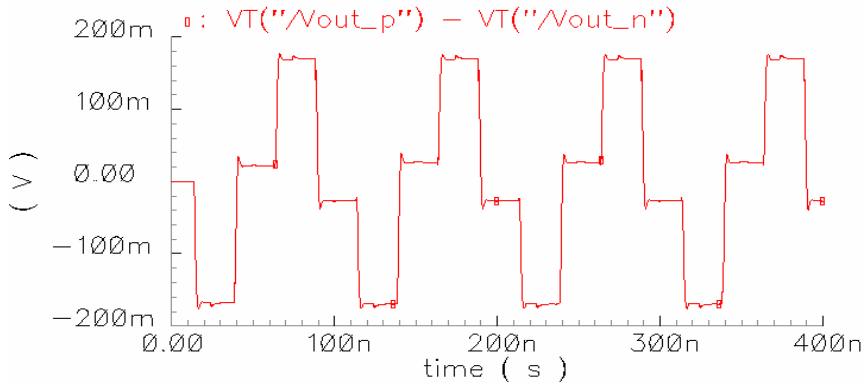
Transistor	W/L(um)	Capacitor	C(fF)
M1, M1',M2,M2'	45/0.6	C_s	800
M3, M3',M4,M4'	15/0.6	C_f	400
M5, M5',M6,M6'	15/0.6	C_o	50
M7, M7',M8,M8'	15/0.6		
M10, M10'	15/0.6		

Table 1: Switch sizes and capacitor sizes in SC track&hold circuit

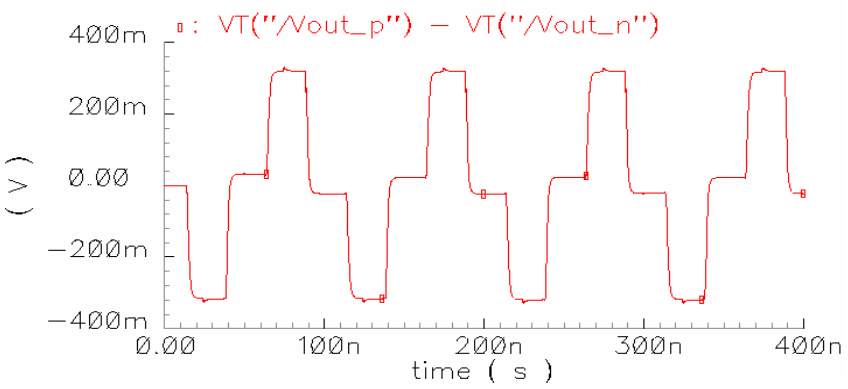
The schematic simulation is done using Spectres in Cadenece. The input to the tack&hold circuit is a 210MHz differential sine signals with an amplitude of 0.1-V. Since the signal is sampled at 40MHz, a signal of 10MHz is retrieved at the output as shown is Figure 11. Because of the effect of capacitor C_0, the signal power is slightly degraded. Figure 12 shows the output spectrum when the circuit gain is set to be 0dB. It can be clearly seen that the output signal is an odd multiple of $fs/4$, 10MHz, 30MHz, 50MHz ….The 10MHz output signal will be digitized through the bandpass sigma-delta ADC and the other frequency components in the output will be filtered out.



a) Input signal with frequency of 210MHz



(b) Output signal with frequency of 10MHz and 0dB Gain



(c) Output signal with frequency of 10MHz and 6dB Gain

Figure 11 Simulation Results of SC Track&Hold circuit

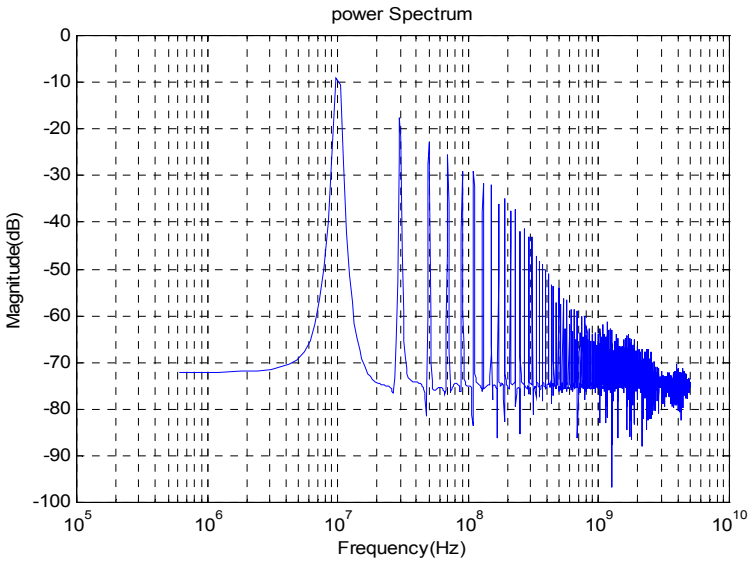


Figure 12 Output spectrum of SC Track&Hold circuit

Chapter 3: Sigma-Delta Fundamentals

3.1 Introduction

The subsampling gain satge is followed by a bandpass sigma-delta A/D converter. It is used to digitize the intermediate frequency (IF) signal in the proposed IF sampling receiver. In this Chapter, the fundamentals of the sigma-delta modulators are reviewed. Sigma-delta modulation has become popular for achieving high resolution. A significant advantage of the method is that analog signals can be digitized using simple and high-tolerance analog circuits to a high resolution.

This Chapter is organized into five main sections. In section3.2, the conventional Nyquist-rate A/D converters and their limitation are described. Section 3.3 introduces some basic properties of the quantization noise. In Section3.4, general oversampling ADC and sigma-delta modulator are discussed. Lowpass and bandpass sigma-delta modulation are discussed in section3.5 and section 3.6, respectively.

3.2 Nyquist-rate A/D Converter

Analog-to-digital conversion is the procession of encoding an analog signal that is continuous in time and amplitude into a signal that is discrete with respect to time and

quantized in amplitude. The process of the conversion can be divided into anti-aliasing filtering, sampling and holding, and quantization. The operation is shown in Figure 13.

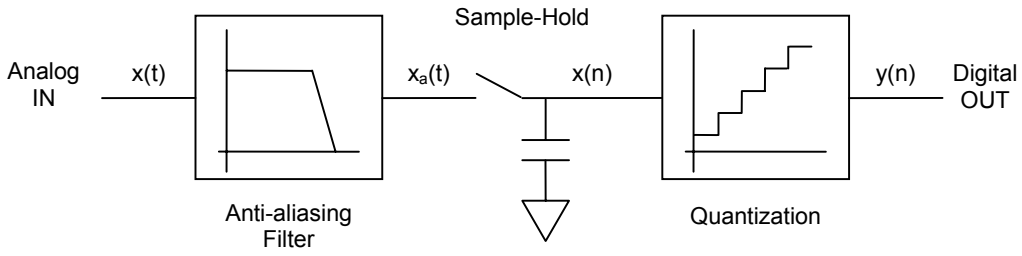


Figure 13 Fundamental operations of A/D converter

According to the relationship between sampling frequency and signal bandwith, A/D converter can be categorized into Nyquist-rate converter and oversampling converter. A Nyquist-rate A/D Converter quantizes the input samples every $1/f_s$ second, where f_s is the sampling rate, and generates a digital output. According the sampling theorem, if there is to be no loss of the information upon sampling, $x(t)$ must be sampled at a frequency higher than twice of the cutoff frequency for the anti-aliasing filter. It should be emphasized that the rate f_s must be chosen to be high enough so that after the pre-filter operation, the surviving signal spectrum within Nyquist interval $[-f_s, f_s]$ contains all the significant frequency components required by the application.

3.3 Quantization Noise

Quantization in amplitude and sampling in time are the two main functions of ADCs. The typical transfer characteristic of quantizers or ADCs with an input signal sample x and an output y is shown in Figure 14.

The quantizer, embedded in any ADC is a non-linear system, is difficult to analyzer. To make the analysis tractable, it is useful to represent the quantized signal y[n] by a linear function Gx[n] with an error e[n]: that is,

$$y[n]=Gx[n]+e[n] \tag{3.1}$$

The gain G is the slope of the straight line passing through the center of the quantization characteristic. In Figure 14, the level spacing Δ is 2. So the quantizer dose not get saturated when $-6 \le x[n] \le 6$ and the error is bounded by $\pm \Delta / 2$. This consideration remains applicable to a two-level (single-bit) quantizer but, in this case, the choice of gain G is arbitrary.

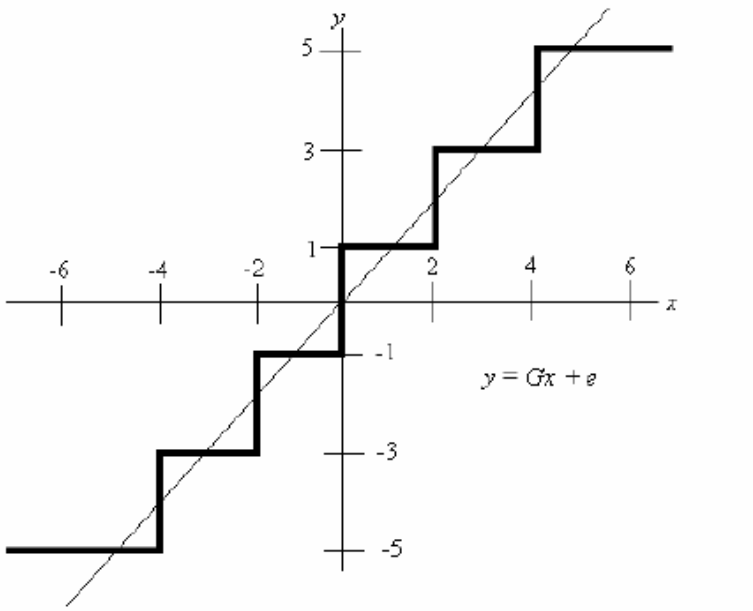


Figure 14 An example of the uniform multilevel quantization characteristic that is represented by linear gain G and an error e

To further simplify the analysis of the noise from the quantizer, the following assumptions are traditionally made [Oppenheim89]:

1. The error sequence e[n] is a sample sequence of a stationary random process,

2. The error sequence is uncorrected with the sequence x[n],

3. The random variables of the error process are uncorrected; i.e. the error is a white-noise process.

4. The probability distribution of the error process is uniform over the range of quantization error.

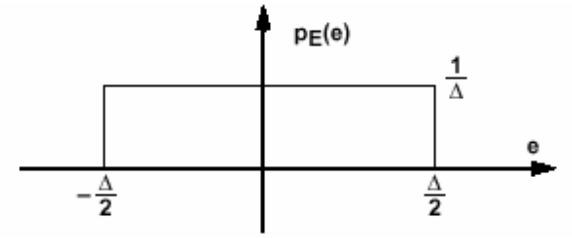


Figure 15 Probability density function of additive, white quantization noise

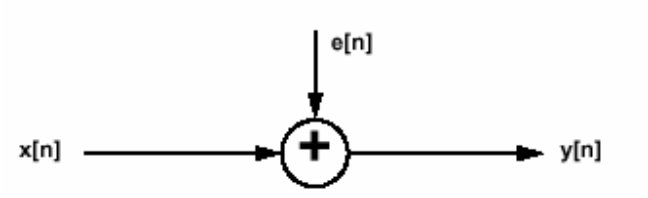


Figure 16 Linearized, stochastic model of quantizer

Under these conditions, it is permissible to assume that the quantization error has a rectangular probability density function shown in Figure 15. The quantizer can then be replaced with the linearized stochastic model of Figure 16. The variance of the quantizer error, e[n], is:

$$\sigma_e^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \qquad (3.2)$$

When a quantized signal is sampled at a sampled at frequency fs=1/T, all of its power folds into the frequency band $0 \leq f \leq fs$.Then, if the quantization noise is white, the spectral density of the sampled noise is given by:

$$E(f) = \sqrt{\frac{\sigma_e^{\,2}}{fs/2}} = \sigma\sqrt{\frac{1}{fs}} \tag{3.3}$$

This can be used to analyze the oversampling modulators. Consider a signal lying in the frequency band $0 \leq f \leq fs$. The oversampling ratio (OSR), defined as the ratio of the sampling frequency fs to the Nyquist frequency $2f_B$, is given by the integer:

$$OSR = \frac{fs}{2f_B} \tag{3.4}$$

Hence, the in-band quantizer noise is given by:

$$n_0^{\,2} = \int_0^{f_B} E^2(f)df = \sigma_e^{\,2}.\frac{2f_B}{fs} = \frac{\sigma_e^{\,2}}{OSR} \tag{3.5}$$

It can be seen that oversampling reduces the in-band quantizer noise power from ordinary quantization by of the oversampling ratio. Therefore, each doubling of the sampling frequency decreases the in-band noise by 3dB and thus increases the resolution by half a bit.

3.4 Oversampling and Sigma-Delta Modulator

A block diagram of a sigma-delta modulator is shown in Figure 17. The modulator consists of a loop-filter that has a transfer function *H(z)*, a quantizer and a digital-to-analog converter(DAC) in the feed back path. The quantizer can be linearized and modeled with an additive error is shown is Figure 18.

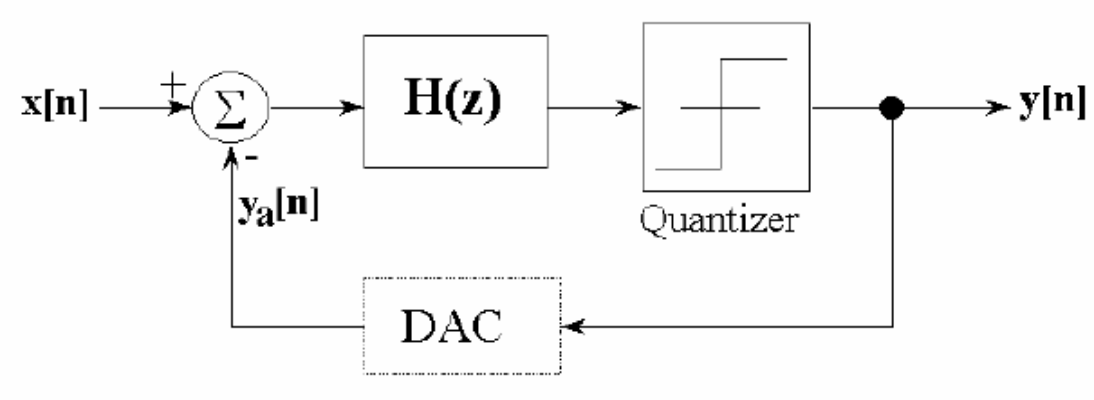


Figure 17 Block diagram of a sigma-delta modulator

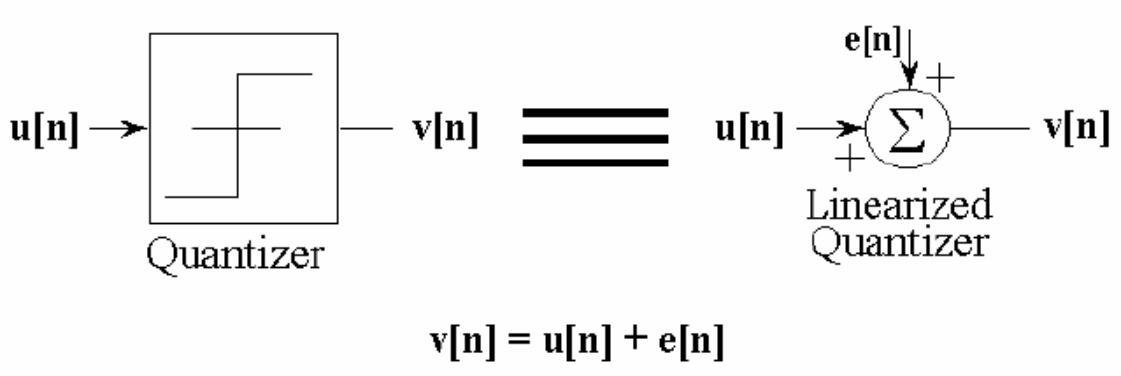


Figure 18 Linearized model of the quantizer

The output of the modulator can be expressed in z-domain by:

$$y(z) = \frac{H(z)}{1+H(z)}x(z) + \frac{1}{1+H(z)}e(z) \tag{3.6}$$

where the signal transfer function is

$$STF = \frac{H(z)}{1+H(z)} \tag{3.7}$$

and the noise transfer function is

$$NTF = \frac{1}{1+H(z)} \tag{3.8}$$

It can be seen from Eq. (3.6) that the poles of $H(z)$ become the zeros of *NTF*. At the frequencies which satisfy $H(z) >> 1$, $y(z) \approx x(z)$, that is, at these frequencies the signal is transferred while the noise is attenuated.

3.5 Low-pass Sigma-Delta Modulation

A block diagram of a first-order sigma-delta modulator is shown in Figure 19 and a lineared version of the block diagram is shown is Figure 20. The modulator is comprised of a subtraction node, a discrete-time integrator, and 1-bit quantizer.

The signal that is being quantized is a filtered version of the difference between the input signal x[n] and an analog representation, $y_a[n]$, of the quantized output, y[n]. The loop-filter is a discrete-time integrator whose transfer function is:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3.9}$$

The modulator output $Y(z)$ in the frequency domain is then given by:

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{3.10}$$

where $STF = z^{-1}$ and $NTF = 1 - z^{-1}$.

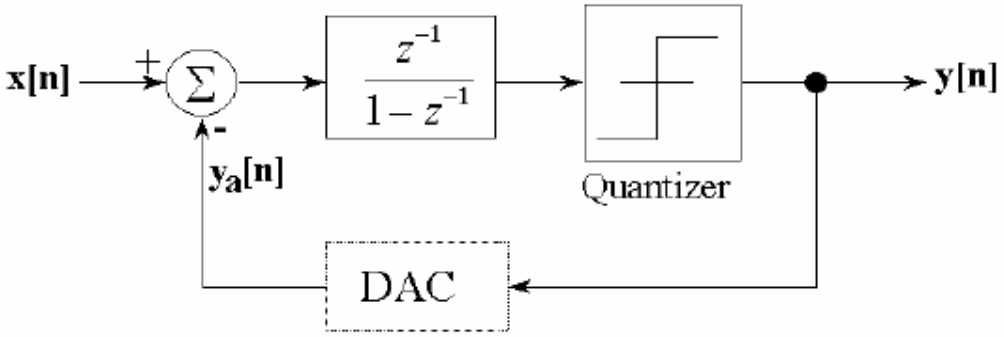


Figure 19 Block diagram of a first sigma-delta modulator

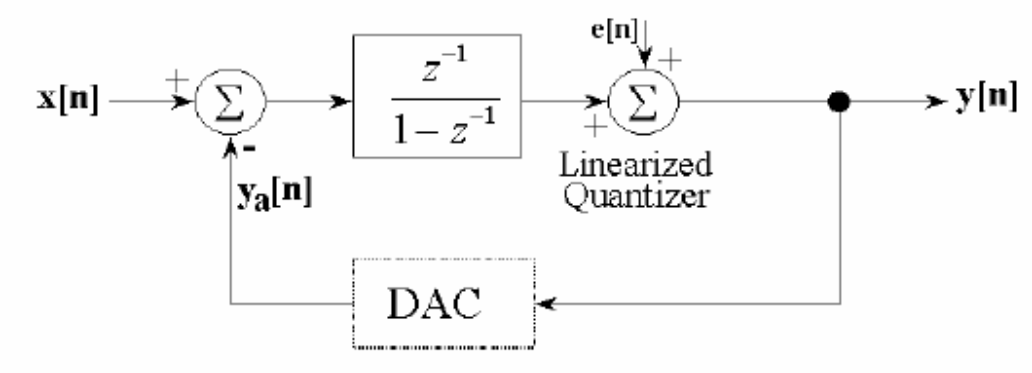


Figure 20 Lineared model block diagram of a first sigma-delta modulator

The output is just a delayed version of the signal plus a quantization noise shaped by a first-order differentiator (or high-pass filter). Note that a zero gain is provided by the NTF at DC frequency. The magnitude spectrum of a first-order sigma-delta noise transfer function (NTF) is plotted in Figure 21. The frequency axis has been normalized

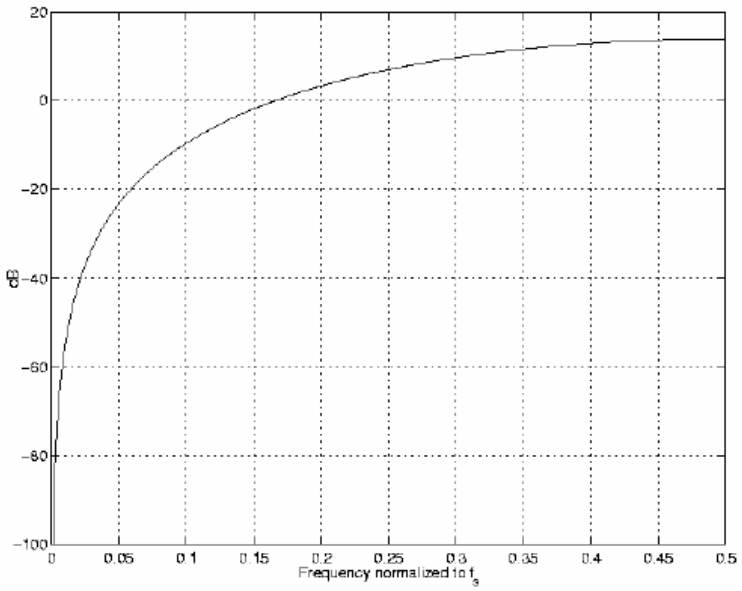


Figure 21 First-order noise transfer function (NTF) magnitude spectrum in dB

with respect to the sampling frequency, f_s.

The in-band quantization noise after the noise-shaping can be found by:

$$
\begin{aligned}
n^2 &= \int_0^{f_B} E^2(f)\left|1-z^{-1}\right|^2 df \\
&= \int_0^{f_B} \frac{\sigma_e^{\,2}}{fs/2}\left|1-z^{-1}\right|^2 df \\
&= \frac{2\sigma_e^{\,2}}{fs}\int_0^{f_B}(2-2\cos\frac{2\pi f}{fs})df \\
&= \frac{4\sigma_e^{\,2}}{fs}\int_0^{f_B} 2\sin\frac{\pi f}{fs}df \\
&\approx \frac{8\sigma_e^{\,2}}{fs}\int_0^{f_B}(\frac{\pi f}{fs})^2 df \qquad (f_B << f_s) \\
&= \frac{\sigma_e^{\,2}.\pi^2}{3}(\frac{2f_B}{fs})^3 \\
&= \frac{\sigma_e^{\,2}.\pi^2}{3}(\frac{1}{OSR})^3
\end{aligned}
\tag{3.11}
$$

Therefore, each doubling of the sampling frequency decreases the in-band noise by 9 dB and, or increases the resolution by one and a half bits. Figure 22 shows the quantization noise spectrum before and after noise shaping.

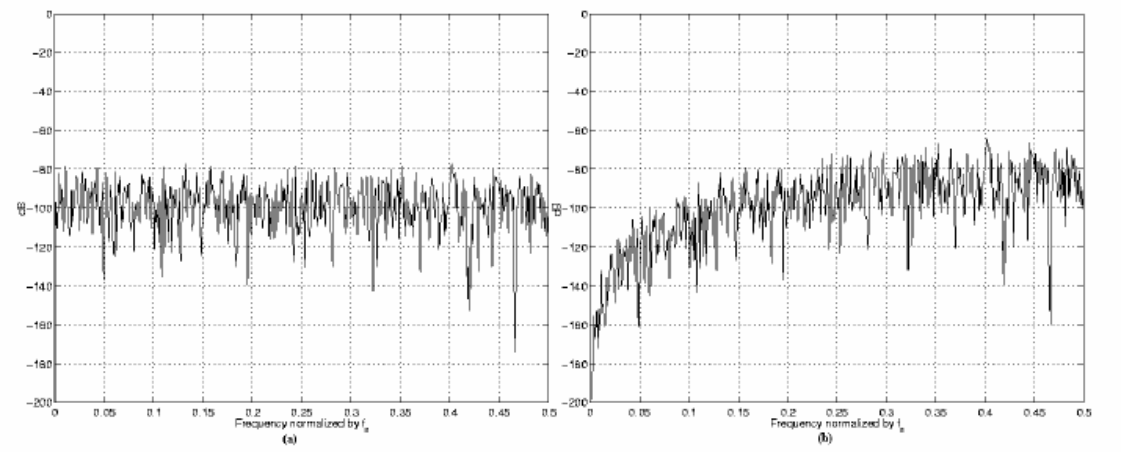


Figure 22 Quantization noise spectrum: (a) before first-order low-pass ΣΔ noise-shaping, (b) after first-order low-pass ΣΔ noise-shaping

In general, as the order of the noise shaping increases, the level of quantization noise present in the signal passband decreases and the out-of-band noise increases. Although the quantization noise is suppressed more effectively through the use of higher-order modulators, the order of a modulator cannot be increased arbitrarily because it is difficult to guarantee the stability of third- and higher-order single-bit modulators. Alternatively, higher-order modulators can be implemented by cascading first- and second-order modulators, which are known to be stable [Brandt91], [Williams94].

3.6 Bandpass Sigma-Delta Modulation

If a signal with a very narrow bandwidth B is located at a center frequency f_c, its highest frequency component is then $f_c+B/2$. If f_c is large, it would lead to an unreasonably large fs in the case of oversampling. Band-pass sigma-delta modulation

allows high-resolution conversion of band-pass signals if f_s is much greater than the signal bandwidth B, rather than the highest signal frequency.

Unlike low-pass sigma-delta modulators that realize NTF zeros at DC or low frequencies, the zeros of NTF for the band-pass modulators are located near the center frequency, f_c, that is, in the signal band of interest, $[f_c\text{-}B/2, f_c+f_B/2]$. Consequently, quantization noise that occurs over the signal band is attenuated, and noise power is pushed outside this band. No matter where the signal band is centered, high OSR makes its in less in-band noise power for a given NTF. Noise outside the signal band can then be attenuated with a digital decimation filter. Thus, high-resolution conversion is possible with large OSR.

Band-pass sigma-delta modulators operate in the same manner as low-pass sigma-delta modulators. A band-pass sigma-delta modulator can be constructed by connecting a filter and quantizer in a loop, as shown in Figure 23.

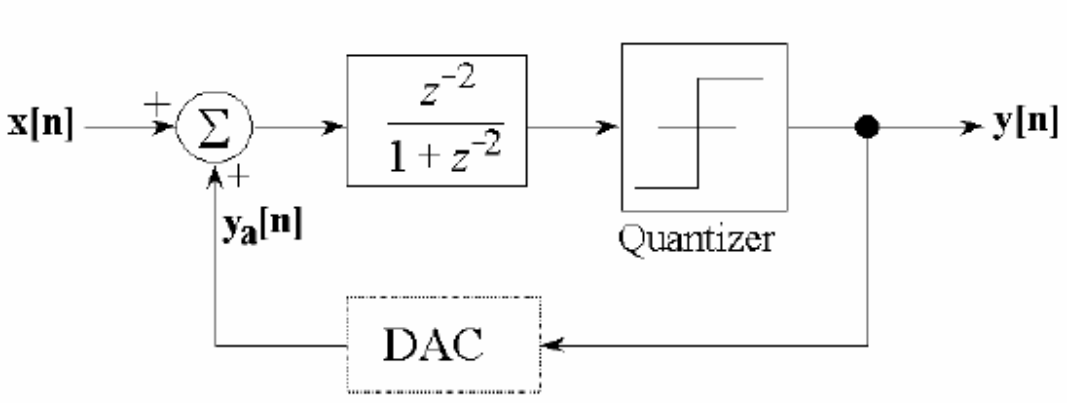


Figure 23 Block diagram of a second-order bandpass sigma-delta modulator

The filter is a discrete-time resonator whose transfer function is:

$$H(z) = \frac{z^{-2}}{1 + z^{-2}} \tag{3.12}$$

If the DAC is ideal, it is replaced by a unity gain transfer function. The modulator output *Y(z)* is given by:

$$Y(z) = X(z)z^{-2} + E(z)(1 + z^{-2}) \tag{3.13}$$

where the STF is z^{-2}, which again is simply a delayed versoin of input, and the NTF is $1+z^{-2}$, similar to a band-notched filter that shapes the quantization noise.

The designs for band-pass modulators can be derived from a low-pass modulators. For instance, by applying the transformation $z^{-1} \rightarrow -z^{-2}$ to a low-pass modulator, the zeros of $H_e(z)$ are mapped from DC to $\pm\pi/2$. This transformation places the center frequency at $\omega_0 = \pi/2$, and thus for a fixed center frequency, the sampling frequency is dictated by the relation $f_s=4f_c$. Also, since this transformation preserves the oversampling ratio, the oversampling ratio of the modulator is again determined by the signal parameters: OSR=$f_s/2B$.

The magnitude spectrum of a second-order band-pass sigma-delta NTF is plotted in Figure 24.The frequency axis has been normalized with respect to the sampling frequency, *f*s.

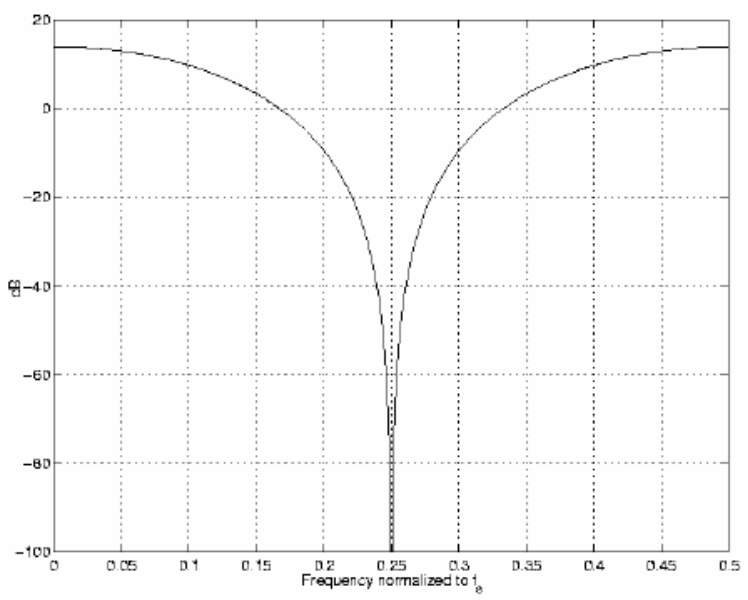


Figure 24 Second-order bandpass NTF magnitude spectrum in dB

The in-band quantization noise after the noise-shaping will be given by:

$$n^2 = \int_{f_C - f_B/2}^{f_C + f_B/2_B} E^2(f)\left|1 + z^{-2}\right|^2 df$$

$$= \int_{f_C - f_B/2}^{f_C + f_B/2} \frac{\sigma_e^{\,2}}{f_s/2}\left|1 + z^{-2}\right|^2 df$$

$$= \frac{2\sigma_e^{\,2}}{f_s}\int_{f_C - f_B/2}^{f_C + f_B/2}(2 + 2\cos\frac{4\pi f}{f_s})df$$

$$= \frac{4\sigma_e^{\,2}}{f_s}(f + \frac{f_s}{4\pi}\sin\frac{4\pi f}{f_s})\Big|_{f_C - f_B/2}^{f_C + f_B/2}$$

$$= \frac{4\sigma_e^{\,2}}{f_s}\left\{f_B + \frac{f_s}{4\pi}\left[2\cos\frac{4\pi f_c}{f_s}\sin\frac{4\pi f_B}{2f_s}\right]\right\}$$

$$= \frac{4\sigma_e^{\,2}}{f_s}\frac{f_s}{4\pi}\left[\frac{4\pi f_B}{f_s} - 2\sin\frac{2\pi f_B}{f_s}\right] \qquad (f_c = \frac{f_s}{4})$$

$$= \frac{8\sigma_e^{\,2}}{4\pi}\left[\frac{2\pi f_B}{f_s} - \frac{2\pi f_B}{f_s} + \frac{1}{3\times 2\times 1}\left(\frac{2\pi f_B}{f_s}\right)^3 - \ldots.\right]$$

$$\approx \frac{\sigma_e^{\,2}\pi^2}{3}\left(\frac{1}{OSR}\right)^3 \qquad (3.14)$$

Therefore, each doubling of the sampling frequency decreases the in-band noise by 9 dB and, or, increases the resolution by one and a half bits. Figure 25 shows the quantization noise spectrum before and after the second-order band-pass sigma-delta noise shaping.

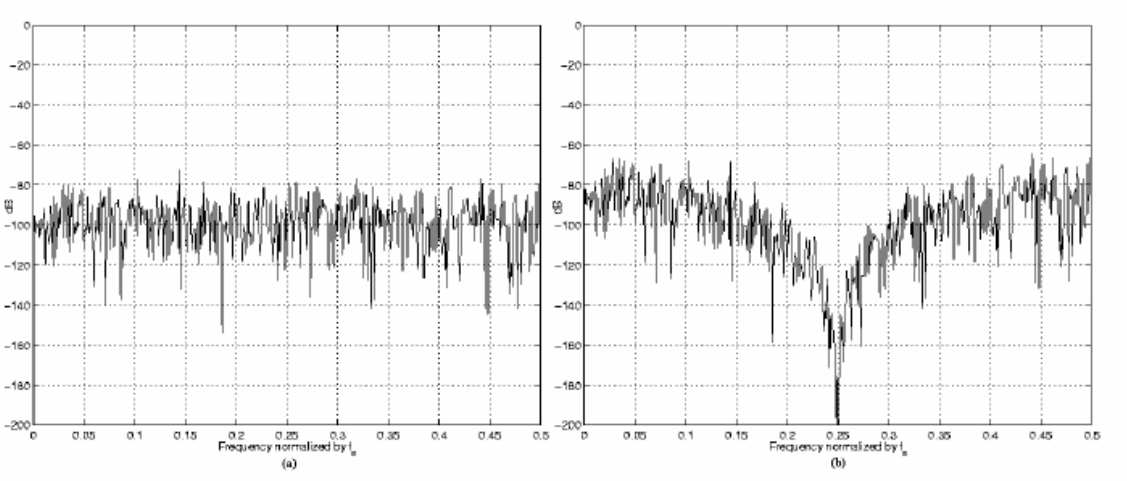


Figure 25 Quantization noise spectrum: (a) before second-order band-pass ΣΔ noise-shaping, (b) after second-order bandp-pass ΣΔ noise-shaping

Chapter 4: Design of the Fourth-order Bandpass Sigma-Delta ADC

4.1 Introduction

This chapter describes the design of the bandpass sigma-delta modulator for the proposed IF sampling receiver.

A single-bit 4^{th}-order bandpass sigma-delta modulator is chosen for the following reasons: a) At a sampling rate of 40MHz and OSR of 100, Matlab simulation shows that a dynamic range of 91dB can be obtained, which is sufficient to meet the dynamic range requirements with some design margins. b) The single-bit internal quantization leads to a very simple quantizer and to an inherently linear DAC implementation.

The design of the bandpass sigma-delta modulator is based on the switched-capacitor technique. As described in the previous chapter, its relatively high-precision characteristics make it suitable for the implementation of the analog loop filter.

In this chapter, the design and implementation of fourth-order bandpass sigma-delta modulator are described. The effects of the circuit non-idealities on the modulator performance are analyzed and simulation results are presented.

4.2 System Architecture

In a bandpass sigma-delta modulator, the quantization noise is shaped away from the signal band at the desired center frequency f_c by placing the quantization noise nulls at f_c. One attractive way of designing bandpass sigma-delta modulator is to perform a low pass to bandpass transformation which can be achieved by the following transformation:

$$z^{-1} \rightarrow z^{-2} \tag{4.1}$$

This transformation maps the zeros of the lowpass prototype from dc to $\pm f_s / 4$, suppressing the noise in the bandpass modulator around the $f_s / 4$ and the $3f_s / 4$ frequencies. The stability and signal-to-noise (SNR) characteristic of this bandpass modulator will be identical to that of the lowpass prototype [Jantzi96].

A classical realization of a 2th-order sigma-delta modulator and its modified topology [Boser98] are shown is Figure 26 and Figure 27, respectively. The modified architecture differs from the classical configuration in two respects: a forward path delay is included in both integrators, thus simplifying the implementation of the modulator with straightforward sampled-data analog circuits. An attenuation of 0.5 preceding the first integrator and a gain of 2 at the input of the second integrator result in the need for a large dynamic range at the output of this stage. The modified architecture in Figure 27 is chosen as the lowpass prototype of the fourth–order bandpass sigma-delta modulator.

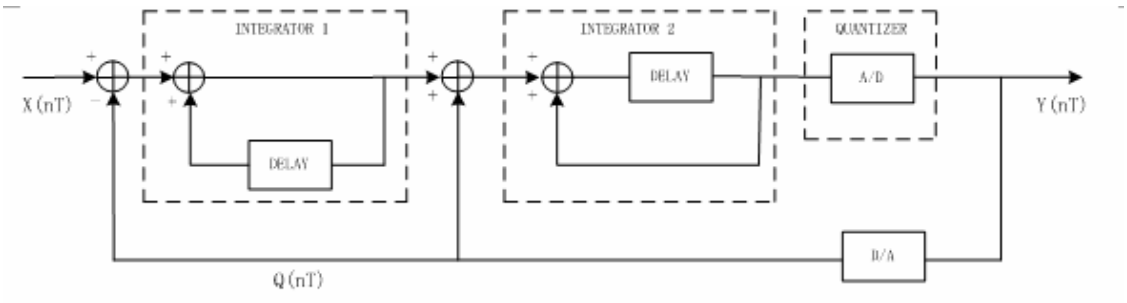


Figure 26 Classical topology for 2th-order lowpass sigma-delta modulator

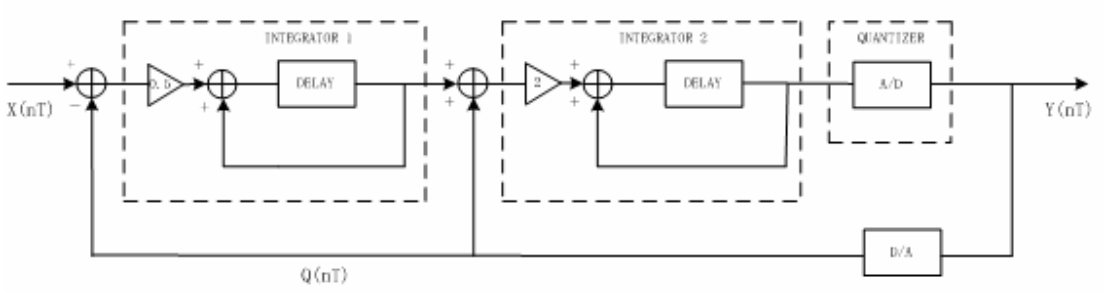


Figure 27 Modified topology for 2th-order lowpass sigma-delta modulator

The transfer function of integrator in the modified second-order lowpass sigma-delta modulator is:

$$H_{lp}(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{4.2}$$

After the transformation $z^{-1} \rightarrow z^{-2}$ is perform, the transfer function of the resonator in the fourth-order bandpass sigma-delta modulator is:

$$H_{hp}(z) = \frac{-z^{-1}}{1 + z^{-1}}\Big|_{z^{-1} \rightarrow -z^{-2}} = \frac{-z^{-2}}{1 + z^{-2}} \tag{4.3}$$

The system block diagram of a fourth-order bandpass sigma-delta modulator is shown is Figure 28:

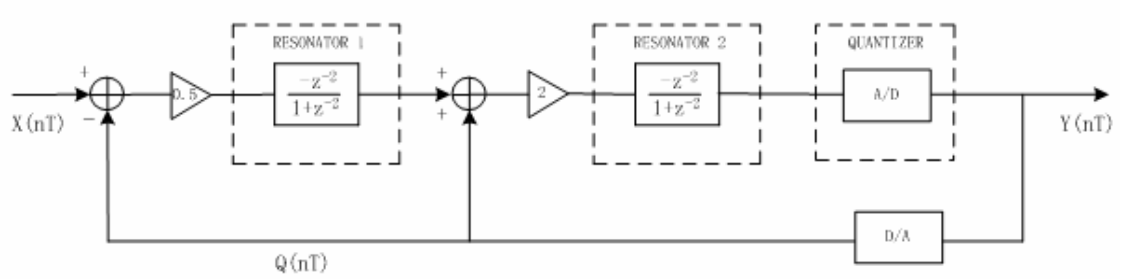


Figure 28 Block diagram of 4^{th}-order bandpass sigma-delta modulator

Assuming the quantization error to be white noise and the comparator gain to be unity, the output transfer characteristic of the bandpass modulator is:

$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2 E(z) \tag{4.4}$$

The noise transfer function of this modulator has a pair of complex-conjugates zeros located at $z = \pm j$. In the frequency domain, this corresponds to the notches around $(2n+1)f_s/4$, where n=0,1,2,…, and fs is the sampling frequency. As discussed before, this fourth-oder modulator is guaranteed to be stable because of the stability of the modified second-order lowpass prototype.

4.3 SNR Calculation

The maximum SNR for the ideal 4^{th} bandpass sigma-delta modulator can be calculated according to the similar procedure described in previous chapter. Assuming input signal is a sine wave, its maximum peak value without clipping is $2^N(\Delta/2)$, where Δ is the

quantization step and N is the number of bits of the quantizer [David97]. For this maximum sine wave, the signal power, *Ps*, has a power equal to:

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{4.5}$$

The inband quantization noise power is given by:

$$P_e = 2\int_{f_s/4-f_b/4}^{f_s/4+f_b/4} E^2(f)\left|N_{TF(f)}\right|^2 df \tag{4.6}$$

Set $f'=f-f_s/4$, and assume the width of the passband $f_b<<f_s$,

$$P_e = 2\int_{f_s/4-f_b/4}^{f_s/4+f_b/4} \frac{\Delta^2}{12 f_s} \times 16 \times \cos^4(2\pi f / f_s) df$$

$$= \frac{8\Delta^2}{3 f_s}\int_{-f_b/2}^{f_b/2} \sin^4(2\pi f' / f_s) df'$$

$$\approx \frac{8\Delta^2}{3 f_s}\int_{-f_b/2}^{f_b/2} (2\pi f' / f_s)^4 df'$$

$$= \frac{1}{60}\pi^4\Delta^2\left(\frac{2 f_b}{f_s}\right)^5$$

$$= \frac{1}{60}\pi^4\Delta^2\left(\frac{1}{OSR}\right)^5 \tag{4.7}$$

So the maximum SNR of this case is given by:

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right)$$

$$= 10\log\left(\frac{\Delta^2 2^{2N} 60}{8\Delta^2\pi^4} \times OSR^5\right)$$

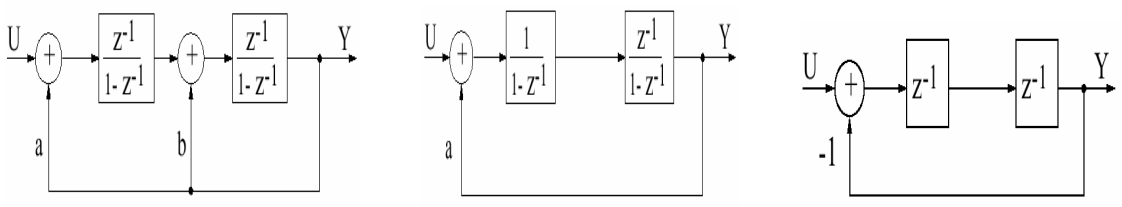
$$\approx 6.02N - 11.13 + 50\log(OSR) \tag{4.8}$$

Thus if N=1 and OSR=100, the maximum SNR can be as high as 95dB.

4.4 Resonator Consideration

4.4.1 Resonator Structure

One key factor in the design of a bandpass sigma-modulator is the implementation of the resonator. There are several structures that can be used to implement the given transfer function $H_{bp}(z)$ of the resonator. Under the ideal case, all of them produce identical performance. However, in the presence of errors in capacitor ratios, finite gain and bandwith in opamps, they behave differently. The most important effect is that the pole's positions of the transfer function are affected in different ways. If the pole are at wrong frequency (wrong angle, in the z-plane) then the notch frequency will not be properly centered, and if they move off the unit circle (wrong magnitude of the complex pole, in the z-plan) then the notch will be shallower and hence the SNR will be reduced [Singor95].



(a) FE loop (b) LDI loop (c) DD loop

Figure 29 Three structures of resonator

Several different structures of resonator, such as Forward Euler (FE), lossless discrete integrator (LDI), or double-delay (DD), have been reported. The block diagrams are shown in Figure 29. The transfer function are given in Eq.(4.9), Eq.(4.10), Eq.(4.11), respectively [Salo03].

$$H_{FE}(z) = \frac{z^{-2}U(z)}{1-(2+b)z^{-1}+(1-a+b)z^{-2}} \tag{4.9}$$

$$H_{LDI}(z) = \frac{z^{-1}U(z)}{1-(2+a)z^{-1}+z^{-2}} \tag{4.10}$$

$$H_{DD}(z) = \frac{z^{-2}U(z)}{1+z^{-2}} \tag{4.11}$$

The FE resonator (Figure 29.a) consists of two identical integrators with the feedback terms *a* and *b*. The notch place can be moved by the parameter *a* and *b*. If we select *a*=*b*=-2 the notch is fixed ideally at f_s=4. The disadvantage of the resonator based on FE structure is that both the notch frequency and the notch depth (Q-value) are dependent on the gain error. Therefore this structure is not favored.

The LDI resonator (Figure 29.b) also consists of two integrators, but one is delay-free. The loop has only one feedback coefficient *a*. Now the notch frequency can be changed by the parameter *a*. With *a*=-2 it is ideally fixed at f_s=4. It also depends on the integrator gain. The poles remain on the unit circle, and hence notch is maximally deep. In this sense it could be regarded as better than FE, but the gain error affects the notch frequency more than in FE and the inaccurate resonance frequency decreases the performance.

The DD resonator (Figure 29.c) consists of two delay elements in series, with a feedback term of one. Now the notch frequency is directly fixed at f_s=4 and therefore other choices cannot be made. The notch frequency is guaranteed and the notch is maximally deep (high Q), regardless of the capacitor mismatch. Consequently, the DD resonator is suitable for the realization of high-performance BP sigma-delta modulators and should be used if the center frequency of f_s=4 is desirable. However, the finite DC

gain and GBW of the amplifier affect the transfer function and have to be considered separately.

4.4.2 Errors due to Opamp Nonidealities

The non-idealities in the opamps could contribute significant errors to the transfer function of the resonator and consequently alter the noise shaping function of the sigma-delta modulator. In the presence of finite dc gain and limited amplifier bandwith, the resonator transfer function takes on the form:

$$H\ (z) = G.(1-\varepsilon_a).\frac{z^{-2}U(z)}{1+\varepsilon_b z^{-1}+(1+\varepsilon_c)z^{-2}} \tag{4.12}$$

where $\epsilon_{a,}\ \epsilon_b$ and ϵ_c model small deviation from the ideal transfer function [Ong97]. The factors $\epsilon_{a,}\ \epsilon_b$ and ϵ_c limit the height of the peak in the magnitude response and shift the peak away from f_s /4.

The dc gain of the opamps is commonly chosen to have a moderate value of more than 60dB.

Finite unity-gain bandwith of the opamp casues a non-zero settling time constant τ. If the resonator is assumed to settle linearly, incomplete settling only manifests itself as a gain error [Boser98]. Where the gain error term, $\epsilon_{a,}$ in Eq.(4.12) is:

$$\varepsilon_a = e^{-T/\tau} \tag{4.13}$$

T is the time allotted for settling. This error results in increased bandpass quantization noise. To reduce the settling errors, opamp with a unit-gain frequency more than 200MHz is required in our design.

4.5 Behavioral Level Simulation Results

The behavioral level simulation of the fourth–order bandpass sigma-delta modulator is done using Matlab program. It based on the discrete-time model in Figure 30. As described in previous section, the resonator in Figure 30 is designed using DD loop, so the Figure 30 can also be modified to Figure 30 which shows the variables declared in the Matlab program (The program is attached in Appendix A).

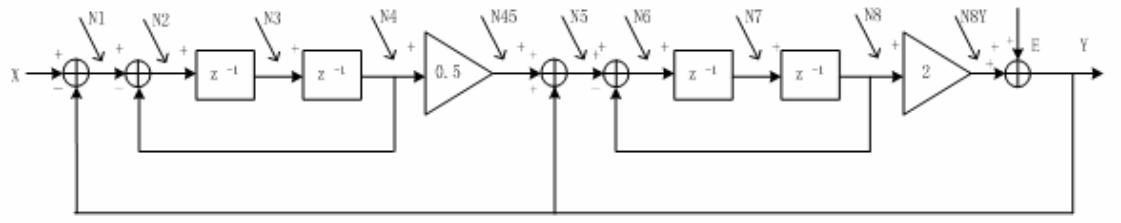
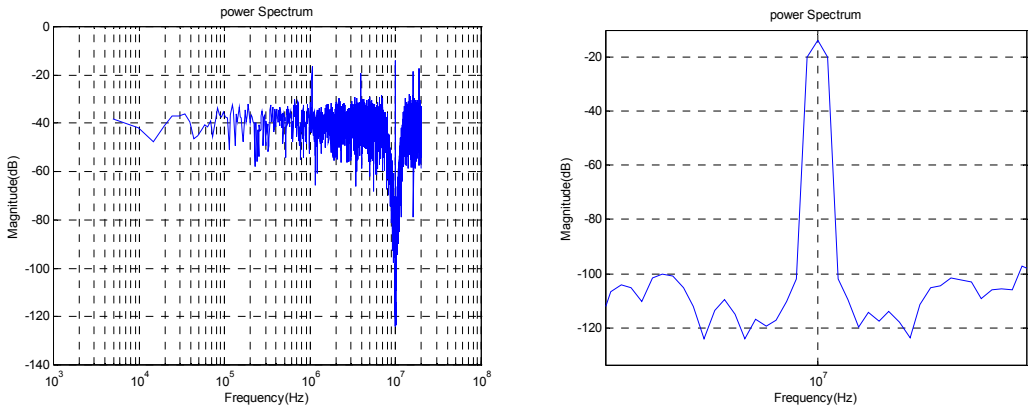


Figure 30 Matlab model of the 4th-order bandpass sigma-Modulator

The clock frequency is set to 40MHz, hence the signal is centered in 10MHz. Figure 31 shows the output power spectrum obtained using 4096-points FFT with a magnitude of 0.1. Figure 31 (a) shows the full range spectrum and Figure 31 (b) is the power spectrum zoomed into a 200KHz signal band centered at the signal frequency, which is the 10MHz in the case.

From Figure 31, it can be seen that the notch of the noise shaping is located at $f_s/4$. The signal-to-Noise Ratio (SNR) is also calculated. Figure 32 shows the in-band SNR against different input level. The modulator can achieve 70dB peak SNR and 91dB dynamic range.



(a) full scale **(b) zoom in 200k**

Figure 31 Output power spectrum of the Matlab simulation for the fourth-order bandpass sigma-delta modulator

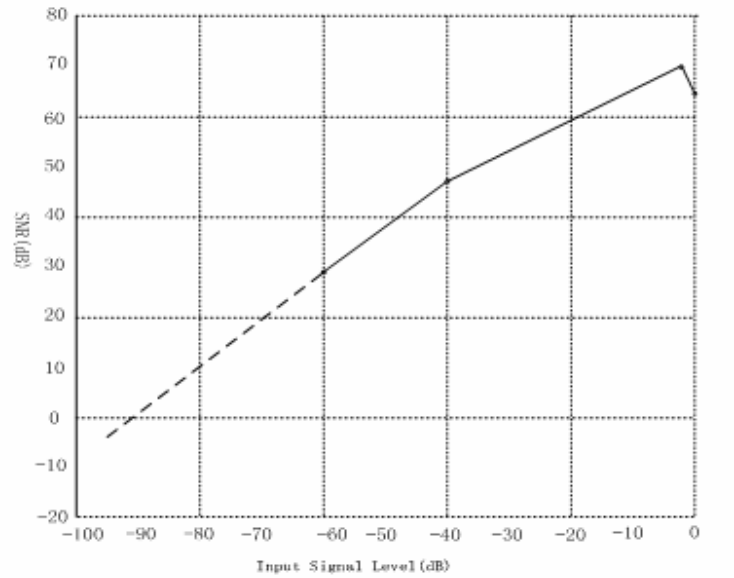


Figure 32 SNR performance of the the Matlab simulation for the fourth-order bandpass sigma-delta modulator

4.6 Circuit Design

The design of the bandpass sigma-delta modulator makes use of fully-differential signal paths. Compared to single-ended design, the fully-differential circuits have much better noise rejection. In fully-differential circuits, common-mode feedback circuits are required to set common-mode voltage at the desired value.

4.6.1 Full-cycle Delay Cell

A unity-gain, full-cycle delay cell is Figure 33. The delay cell comprises an operational amplifier, several capacitors and the switches.

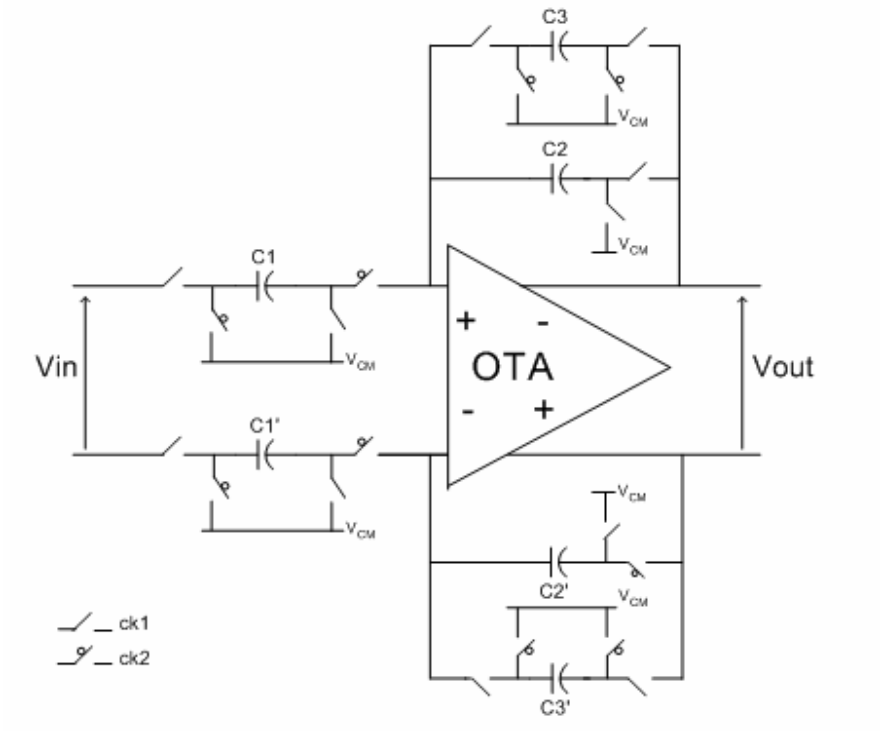


Figure 33 Schematic of the fully-differential delay cell

All the capacitors are assumed to have the same value. The switches are controlled by two non-overlapping clock, ck1 and ck2. The delay-cell operation during the sampling and charge-transfer phase is depicted in Figure 34. On the sampling phase, ck1, a charge

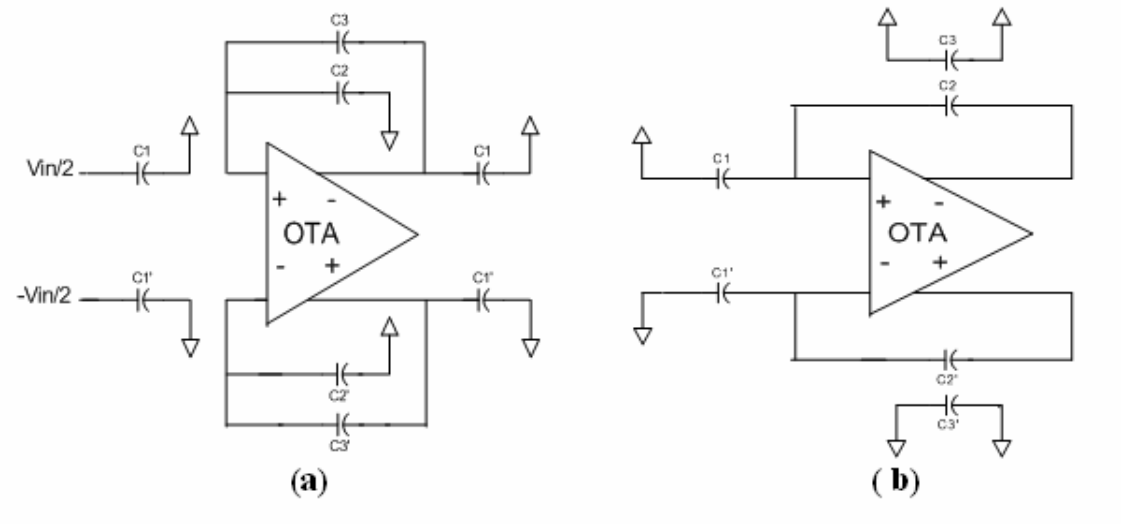


Figure 34 Operation of the delay cell during (a) sampling phase, ck1, and (b) charge-transfer phase, ck2.

proportional to V_{in} is stored on C_1 and C_1'. On the subsequent charge-transfer phase, ck2, the charge on C_1 and C_1' will be transferred to C_2 and C_2', respectively, assisted by the virtual ground at the opamp input. Thus at the end of charge transfer phase, the ouput voltage V_{out} is equal to the input voltage. At the next phase, ck1, the charge on C_2 and C_2' will be transferred to C_3 and C_3', respectively. Thus, the output voltage V_{out} is maintained at the end of phase, ck2. In this way, the full-cycle delay function z^{-1} is realized.

The differential topology used in the circuit of Fig .4.8 ensures that common-mode disturbances such as noise from the power and ground rails, as well as signal-independent switch charge injection, will be cancelled to the first order [Hsieh81]. Furthermore, the signal voltage swings are effectively doubled, which increases the maxi-mum signal

power by a factor of four, while the KT/*C* noise power is only increased by a factor of two. Thus, a net improvement of 3 dB in the peak SNR is obtained if the noise floor of the circuit is governed by KT/*C* noise. If opamp noise dominates the noise performance of the fully-differential circuit, the result is a 6 dB improvement in SNR [Hsieh81]. However, these advantages are obtained at the expense of the additional complexity imposed by the need for common-mode feedback circuitry in the amplifier and the greater area required to implement a fully-differential topology.

4.6.2 Resonator Circuit

The resonator is implemented using full-differential, switched-capacitor circuit by cascading two unity-gain full-cycle delay cells. The switched-capacitor implementation of the resonator based on the two delay cells is shown in Figure 35.

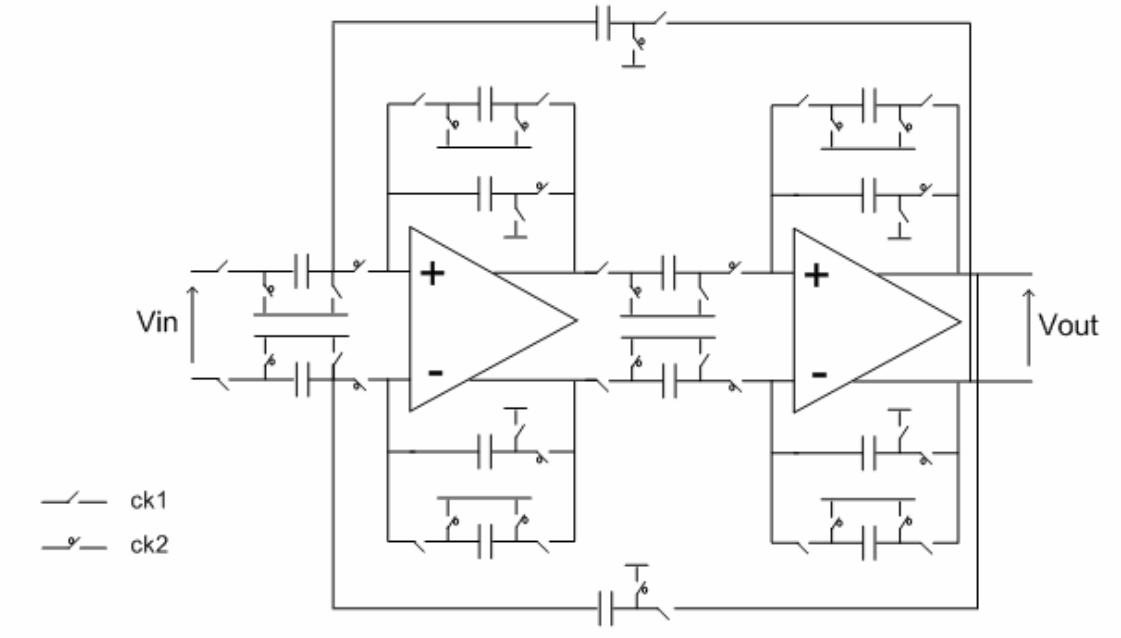


Figure 35 Schematic of the resonator based on two delay cells

4.6.3 Circuit of the Fourth-order Bandpass Sigma-Delta Modulator

The schematic of the fourth-order bandpass sigma-delta modulator is shown in Figure 36. The modulator comprises two cascaded resonator, a comparator and a 1-bit DAC. All the capacitors have the identical value of C_u, except the two capacitors marked by asterisk '*' which have a value of 2 C_u.

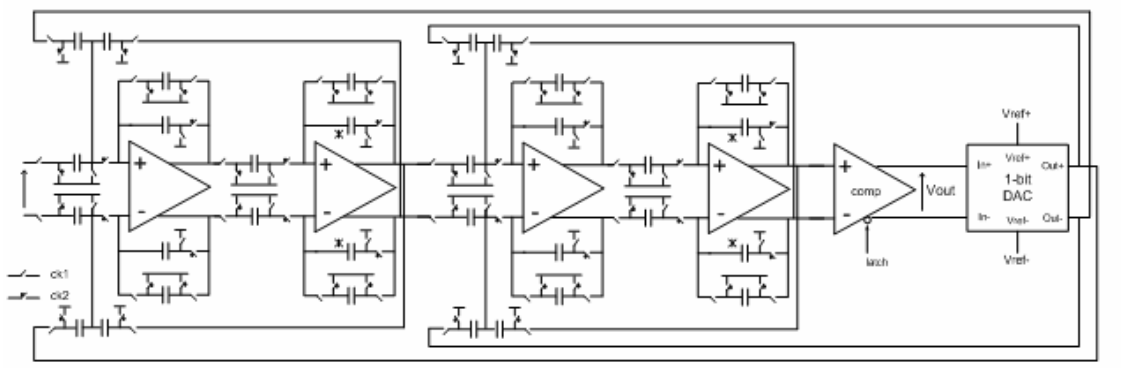
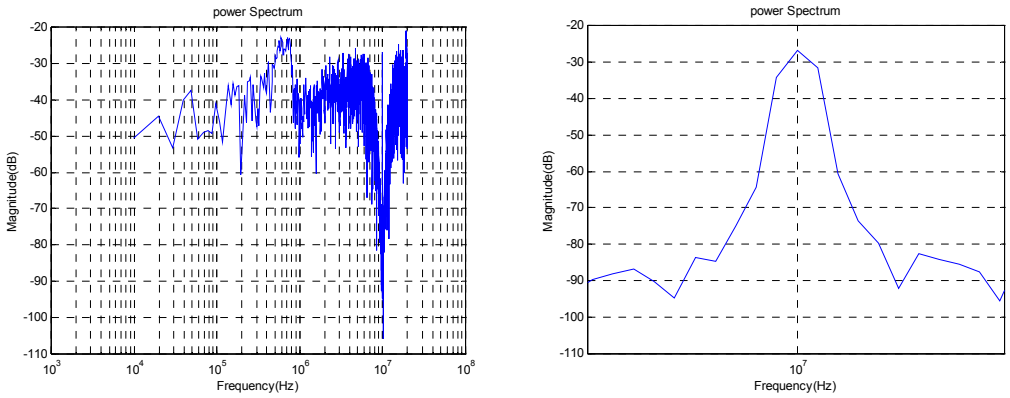


Figure 36 Schematic of the fourth-order bandpass sigma-delta modulator

4.7 Circuit Simulation Results

The fourth-order bandpass sigma-delta modulator is operated from 3.3V power supply and the analog ground is set to be 1.65V, half of the supply power. The feedback level is determined by the Vref+ and Vref- of the DAC. The value of the Vref+ and Vref- are chosen to 1.85V and 1.45V, respectively.

The schematic simulation is done using Spectres in Cadenece. Figure 37 shows the output power spectrum with 4096-point when the frequency of the clock is 40MHz and the frequency of the input signal is at 10MHz with a magnitude of 0.1. From Figure 37, it



(a) full scale **(b) zoom in 200k**

Figure 37 Output power spectrum of the schematic simulation for the fourth-order bandpass sigma-delta modulator

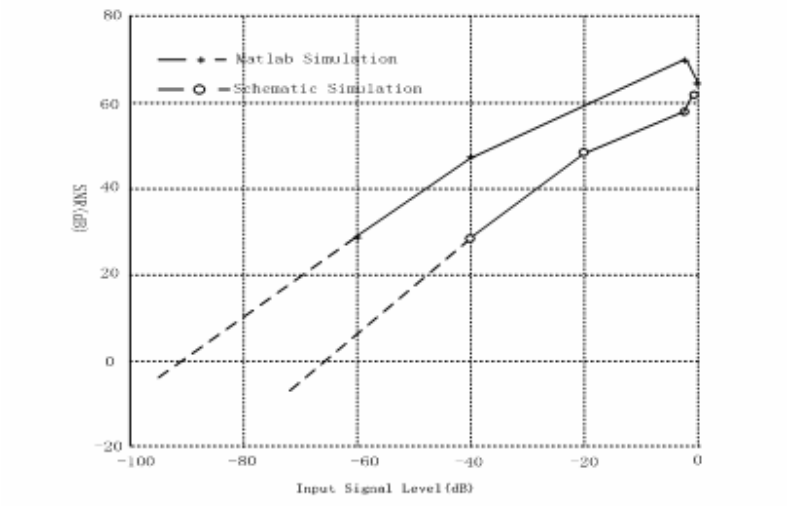


Figure 38 SNR performance of the the Schematic simulation for the fourth-order bandpass sigma-delta modulator

can be seen that the depth of the notch decreases to -90dB compared with -120dB in Fig.4.6, the results of the behavior simulation. As shown in Figure 38, the peak SNR and

calculated dynamic range is degraded to 61dB and 65dB, respectively. The degradation comes from the circuit imperfections, such as charge injection and opamp non-idealities.

Chapter 5: Circuit Level Design

5.1 Introduction

This chapter describes the circuit-level design and implementation of a 210MHz IF sampling receiver based on subsampling gain stage and 4^{th} bandpass sigma-delta modulator.

The design of the differential switch-capacitor subsampling and the 4^{th} bandpass sigma-delta modulator were introduced in the previous chapter. This chapter will present the function blocks of IF receiver in the section 5.2. The design for the key circuit blocks which are the heart of the proposed IF sampling receiver will described in section5.3-section 5.6, respectively. The simulation results for each individual block are also presented. The special consideration in the layout design is described in section 5.7. In the section 5.8 the results of schematic and post-layout simulation are presented.

The design is based on 0.6-um, double-poly, triple-metal CMOS process and operated under a 3.3-V supply.

5.2 Function Blocks

The block diagram of the IF sampling receiver is shown in Figure 39. The receiver consists of a continuous-time IF amplifier, a switched-capacitor subsampling gain satge and 4^{th}–order bandpass sigma-delta modulator. The input signal is at first IF of 210-MHz. The input signal is sampled at 40MHz and downconverted to the second IF through subsampling. The second IF is at $F_S/4$ or 10MHz. As mentioned in the previous chapter, the first input signal IF should be an odd multiple of the second IF. In this case, the first IF is 21times of the second IF.

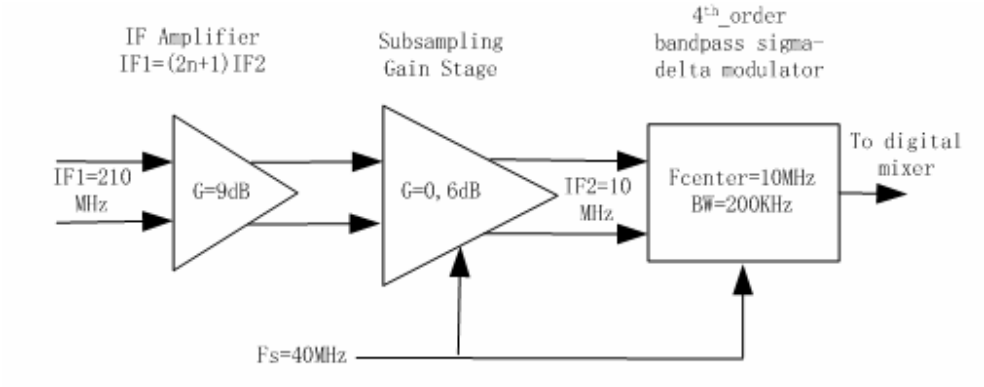


Figure 39 Block diagram of the 210MHz IF Receiver

A programmable gain of 15dB is distributed among the first two blocks. The IF amplifier provides 9dB and the subsampling gain stage 0 or 6dB. The receiver is designed for a channel bandwith of 200kHz.

The simplified schematic of the IF sampling receiver is shown in Figure 40.

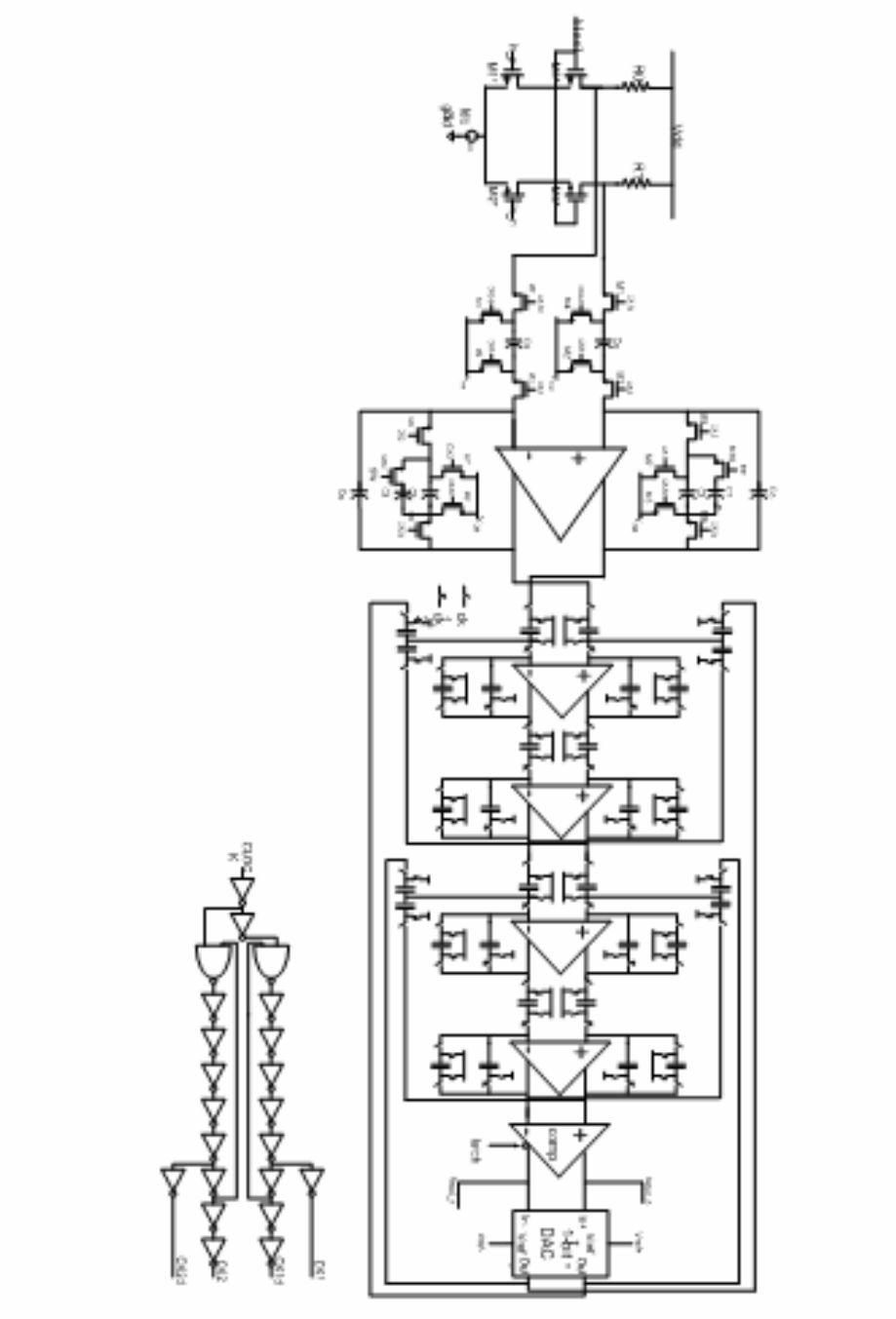


Figure 40 A simplified schematic of the IF sampling receiver

5.3 Operational Amplifier

5.3.1 Folded-cascode Opamp

In the fully-differential switched-capacitor design, the circuit is required to settle completely within half of the clock period. Thus, the opamp itself must be able to settle within half clock period. A sufficient bandwith is needed for the opamp to settle to the desired accuracy with the half periods. It has shown that the following condition must be satisfied,

$$\omega_0 T / 2 = \pi \omega_0 / \omega_c >> 1 \tag{5.1}$$

For a two-phase clock, the unity-gain bandwith, ω_0, should be (at least) five times as high as the clock frequency, ω_c [Gregorian86]. In this design, the clock frequency is 40MHz, which leads to a minimum unity-gain bandwith of 200MHz.

Furthermore, the opamp should have a fairly linear open-loop transfer function and possess a reasonable amount of low-frequency open-loop gain, so the distortion of the amplifier will be reduced even further when placed in a close loop configuration. To achieve a gain error less than 1%, the gain of the opamp should be at least greater than 1000, or 60dB.

With attention toward the requirement for high bandwith and a modest dc gain of 1000, the schematic of folded-cascode operational amplifier shown in Figure 41 is used to implement the switch-capacitor filters in the subsampling stage and 4^{th} bandpass delta-sigma modulator.

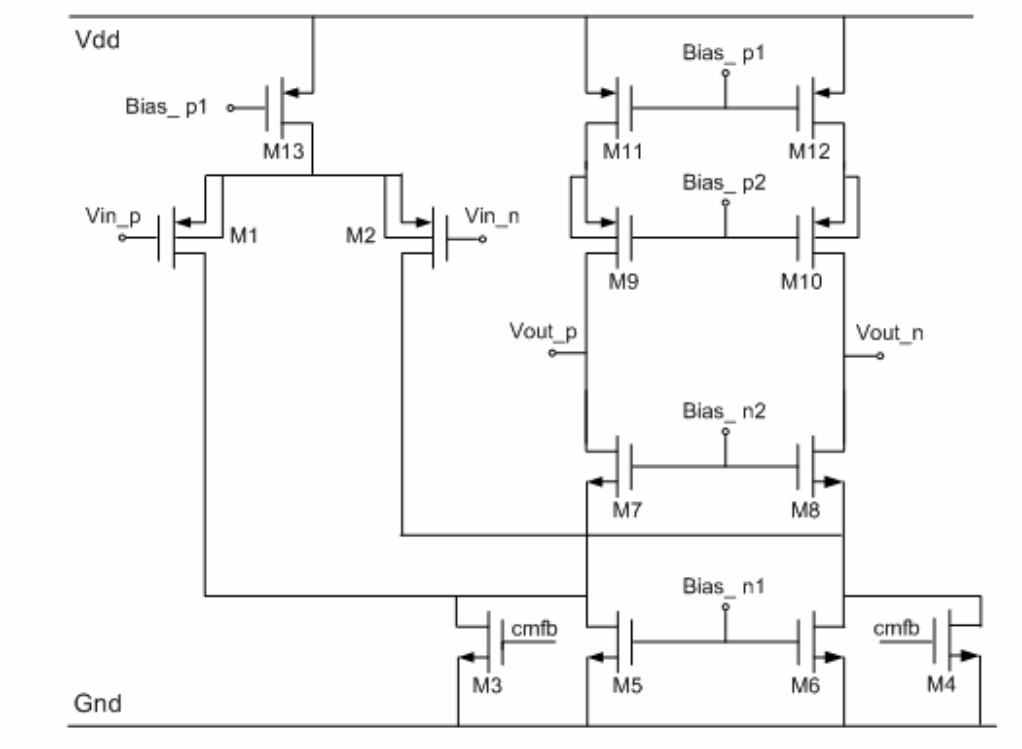


Figure 41 Schematic Folded-cascode operational amplifier

This topology is chosen over the telescopic-cascode topology because its input and output commom-mode levels are decoupled from one another and can be set easily and independently [Razavi01]. On the other hand, folded-cascode has higher input and output swing than the telescopic-cascode counterpart. In the design, both the input and output common-mode levels are set to 1.65V which is the middle of supply voltage.

As shown in Fig.5.3, M1, M2 are input differential pair who have large W/L ratios in order to obtain high $g_{m.}$ M3 to M6 are NMOS current sources and M11, M12 are PMOS current sources. M7 to M9 are cascoded transistors. The current flowing through M13 is twice as much as that through PMOS current source. As a result, the current through each of NMOS current source is twice the current through each transistor of the input

differential pair. The output common mode voltages are set by the switch-capacitor common-mode feedback applied to the bottom NMOS current sources.

The W/L rations of the transistors of folded-cascode operational amplifier are listed in Table 2. It can be seen from the table that M1 and M2 are designed in the minimum length and lage W/L ratios to achieve high $g_{m.}$ The long channel length is used in M11 to M13 to alleviate the channel length modulation effect. M3 to M9 also have longer channel lengths in order to increase the output resistance of the opamp. The W/L ratios of M7, M8 and M9, M10 are determined based on the trade-off between gain and frequency response through simulation.

Transistor	W/L(um)	Transistor	W/L(um)
M1, M2	900/0.6	M9, M10	440/1.8
M3, M4	354/2.4	M11, M12	157/1.5
M5, M6	354/2.4	M13	628/3.0
M7, M8	134/1.0		

Table 2 W/L ratios of the transistors of folded-cascode operational amplifier

As seen in Figure 42, the simulated unity-gain bandwith of the amplifier when driving a 2pF load at each output is approximately 303MHz. The dc gain is 61dB and the phase margin is 71.

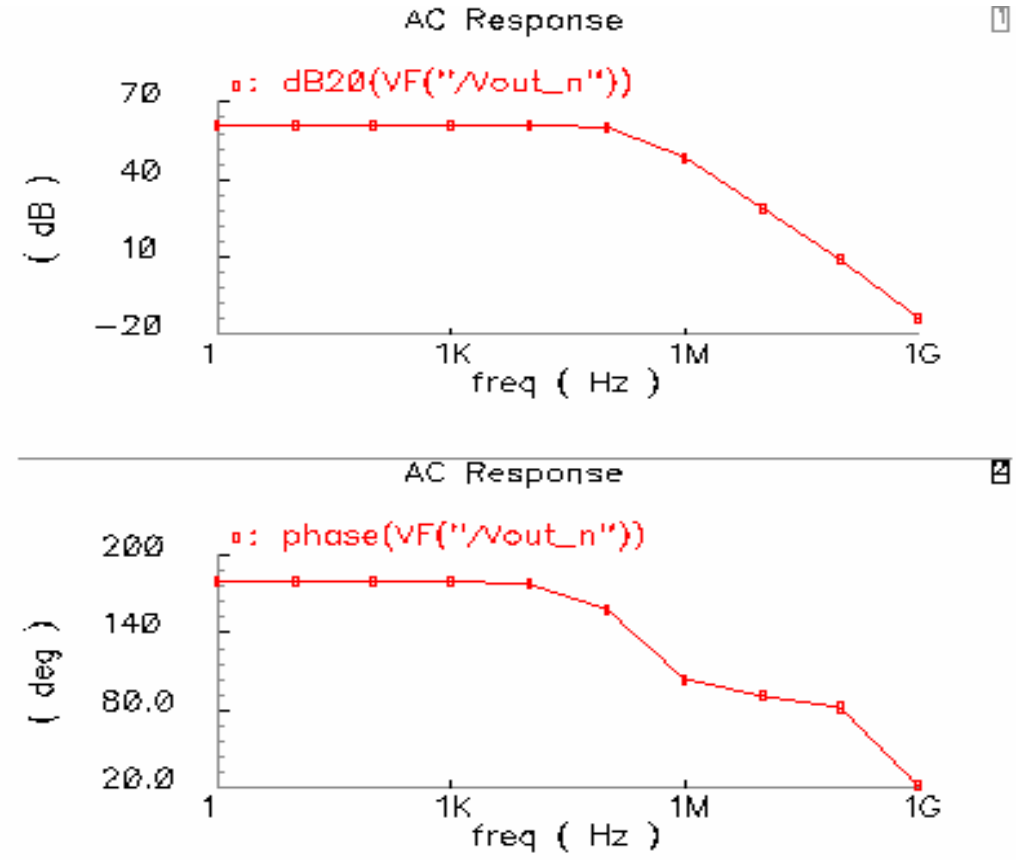


Figure 42 Frequency response of the Folded-cascode amplifier

5.3.2 Bias Circuit

Biasing of the OTA is achieved by the use of a single bias generator circuit. A single external reference current is used to generate the appropriate voltages through bias circuits shown in Fig 5.5. The transistors in the amplifier are biased such that their drain source voltage, V_{DS}, is greater than their gate-source overdrive voltage, V_{GS}-V_T, by several hundred mV to insure that the transistors remain well within the saturation region of the operation, thus maintaining a high output resistance. Low –voltage cascoded current mirror are used to bias the gates of the NMOS and PMOS current source transistors of the amplifier, M5-M6 and M11-M13, respectively [Ong97].

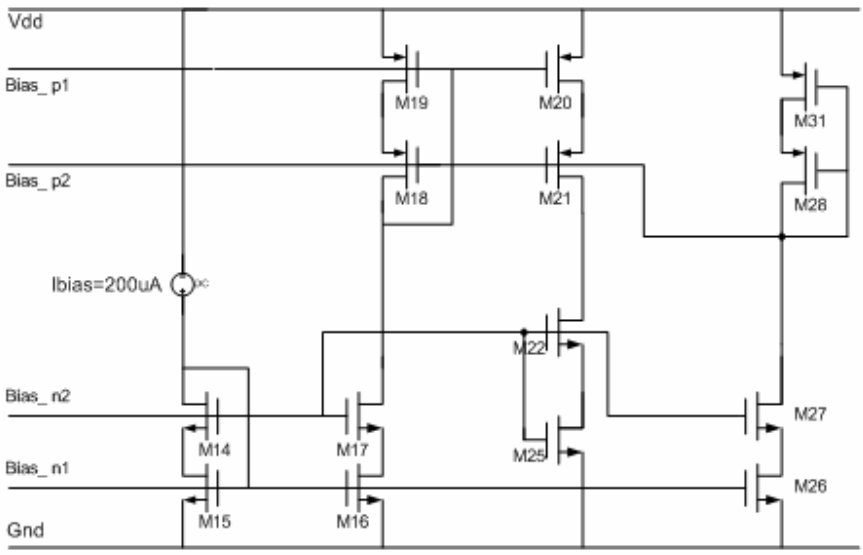


Figure 43 Bias circuit for folded-cascode operatonal amplifer

The gates of the NMOS cascode transistors,M7 and M8, are biased with two NMOS, M22-M25, that are operated in the linear regeion[Nishimura93]. The NMOS cascode bias voltage, bias_n2, is set at a nominal value of 1.8V. This is a compromise that ensures the NMOS current source transistors,M3-M6, are saturated while allowing for a relatively large swing at the amplifiers outputs. Similarly, the gates of the PMOS cascode transistors, M9 and M10, are biased by two transistors in their linear region, M28-M31, to a voltage of 1.1V.

All transistors in Figure43 have no minimum channel lengths in order to reduce the influence of the channel length modulation on the bias voltages. The W/L ratios of the transistors of the bias circuit are given in Table 3.

Transistor	W/L(micron)	Transistor	W/L(micron)
M14, M17	15/1.0	M28, M31	71/4.2
M15, M16	60/1.8	M22, M25	45.9/4.2
M18, M21	30/1.0	M26	60/1.8
M19, M20	123.2/1.0	M27	15/1.0

Table 3 W/L ratios of the transistors of bias circuit for folded-cascode operatonal amplifer

In order to reduce layout complexity , but at the expense of increased power dissipation, the experimental modulator contains four independent biasing circuits, one for each operational amplifier.

5.3.3 Switched-Capacitor Common-Mode-Feedback Circuit

In a fully-differential amplifier, it is necessary to add additional circuitry to maintain the output common-mode voltage at some specified voltage, usually about half way between the power-supply voltages.

In the switch-capacitor circuits, the switched-capacitor CMFB is generally preferred over its continuous counterpart since it allows for a large output signal swing. The common-mode feedback network employed in the opamp is shown in Figure44 [Recoules99].

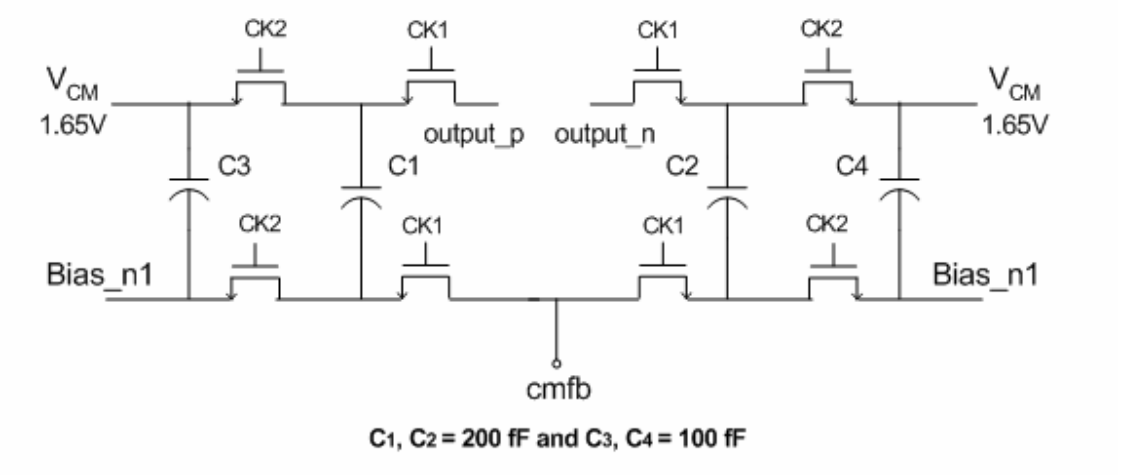


Figure 44 Switched-Capacitor Common-Mode-Feedback Circuit

The CMFB circuit is composed of two capacitors (C1, C2) sensing the output DC level, and two others (C3,C4) refreshing this network with non-overlapping clock phase CK1 and CK2. Sources Vcm and Bias_n1 represent respectively the desired output common mode voltage and a voltage close to the ideal value applied at the node V_{cmfb}. The circuit tries to keep V_{cmfb}-V_{out_p}(V_{out_n}) constant and equal to V_{bias_n1}-V_{cm} thanks to the refreshments through C3, C4 capacitors. The common-mode feedback circuit works as follows: If the output common-mode voltage increases, the control voltage Vcmfb will also increase. As a result, more current will be draw through transistors M3 and M4 (Figure 41). This will decrease the current of the output and pull down the output common-mode voltage. The capacitors of C1-C2 increase the opamp output capacitance, to avoid C1 and C2 deteriorate the amplifier frequency performance, both C1 and C2 are chosen to have a small value of 0.1pF.

5.4 Comparator

The comparator in the 4th–order bandpass sigma-delta modulator is used as a quantizer. The input offset of the comparator can be considered as quantization noise and will be suppressed by the feedback loop, so the pre-amplification is not required. The comparator is realized using a fast dynamic latch followed by the buffers and storage circuits that hold the data for a full clock cycle. The schematic of the comparator is shown in Figure45.

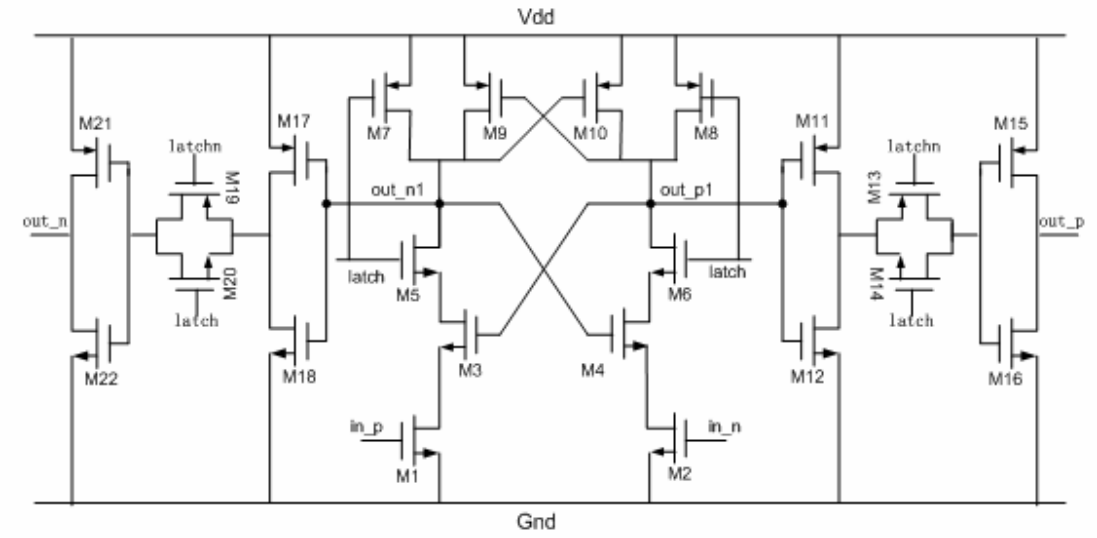


Figure 45 Schematic of the comparator

The comparator is operated in two phase, compare phase and reset phase.

In the compare phase, the latch signal is high, M7, M8 turns off and M5, M6 turns on, M3, M4, M9, M10 forms two back-to-back connected inverters. If input signal in_p is greater than in_n, the current flowing through M1 is slightly greater than the current flowing through M2. As a result, the voltage of node out_p1 is slightly greater than the voltage of the node of out_n1.The output voltage of the node out_p1 will be quickly pulled down to “low” and its counterpart out_n1 will be quickly pulled up to “high” until

the dynamic latch reaches the stable state. The decision of the comparison is transferred to the output through the transmission gate and the buffer.

In the reset phase, the latch is low, M5, M6 turns off, the transmission gates also turn off. The outputs of the comparing stage out_p1,out_p2 are pulled up to high. The previous results are stored in the output of the buffer stage out_p, out_n till next clock cycle.

In the determining the aspect ratios of the transistors in the comparator, high-speed operation has to be considered. The sizes of M1 and M2 should be large enough to provide a high gain (transconductance) and, at the same time, its gate capacitances should not overload the previous stage. Similarly, the sizes of M5 and M6 also should be large so that their resistance values are minimal. M15, M16 and M21, M22 should be optimized for the speed and driving capacity. Table 4 shows the W/L ratios of the transistors.

The comparator is simulated with 1pF load and 40MHz clock frequency. The simulated transient response is shown in the following Figure 46. The rising time is 1.39ns (10% accuracy), while the fall time is 1.17ns, which indicates a maximum sampling frequency of approximately 391MHz.

Transistor	W/L(micron)	Transistor	W/L(micron)
M1, M2	80/1.0	M12, M18	6.0/0.6
M3, M4	60/0.6	M13, M14	3.0/0.6
M5, M6	60/0.6	M19, M20	3.0/0.6
M7, M8	60/0.6	M15, M21	24/0.6
M9, M10	60/0.6	M16, M22	12/0.6
M11, M17	12/0.6		

Table 4 W/L ratios of the transistors of comparator

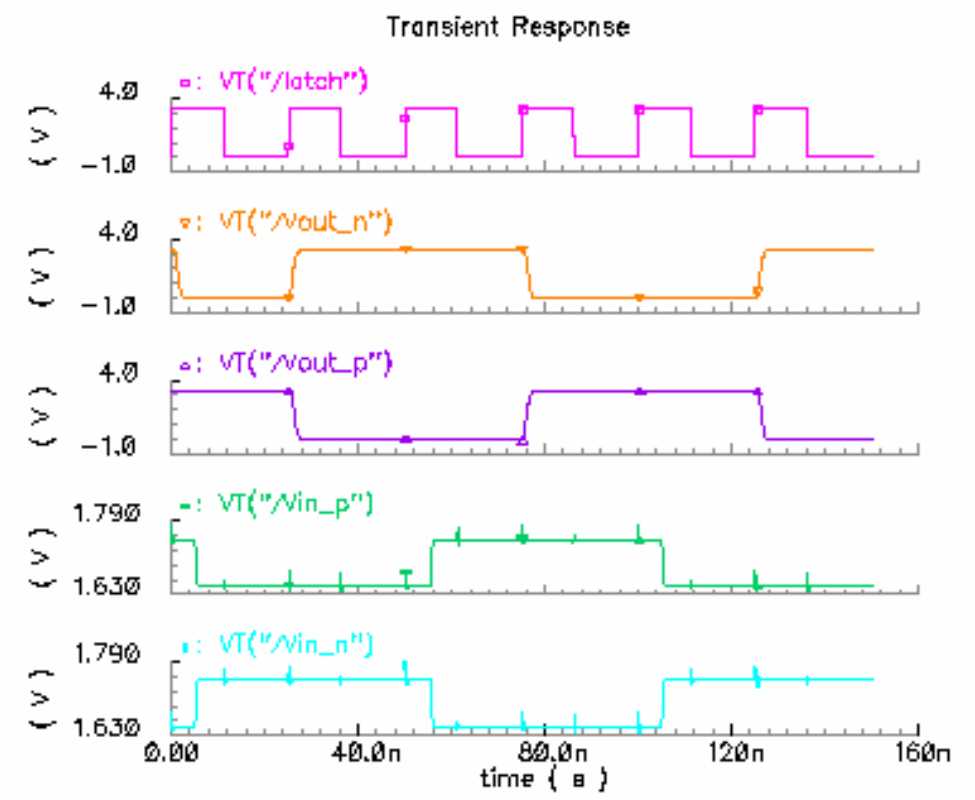


Figure 46 Transient response of the comparator

5.5 IF Amplifier

The main function of IF amplifier is to isolate the external LC filter from the switch-capacitor gain-stage. This isolation is necessary to prevent ringing on the external LC filter which can be triggered by coupling from the switched-capacitor clock signal. The IF amplifier in the design is required to have a gain of about 9dB for input signal frequency of 210MHz. A cascode amplifier as shown in Figure 47 is chosen. The bias current Idc3 are designed to be 1.0mA, the R0 and R1 are both 3.3kΩ, so the output common-mode voltage is 1.65v. Table 5 shows the W/L ratios of the transistors of the IF amplifier.

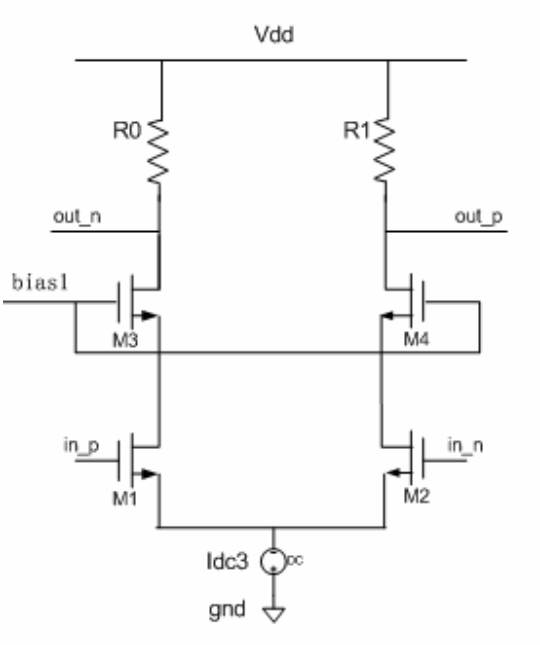


Figure 47 IF Amplifier

Transistor	W/L(micron)	Transistor	W/L(micron)
M1, M2	240/0.6	M3, M4	120/0.6

Table 5 W/L ratios of the transistors of IF amplifier

The AC response of IF amplifier is simulated with 200fF load on each output node. The result is shown in the Figure 48.

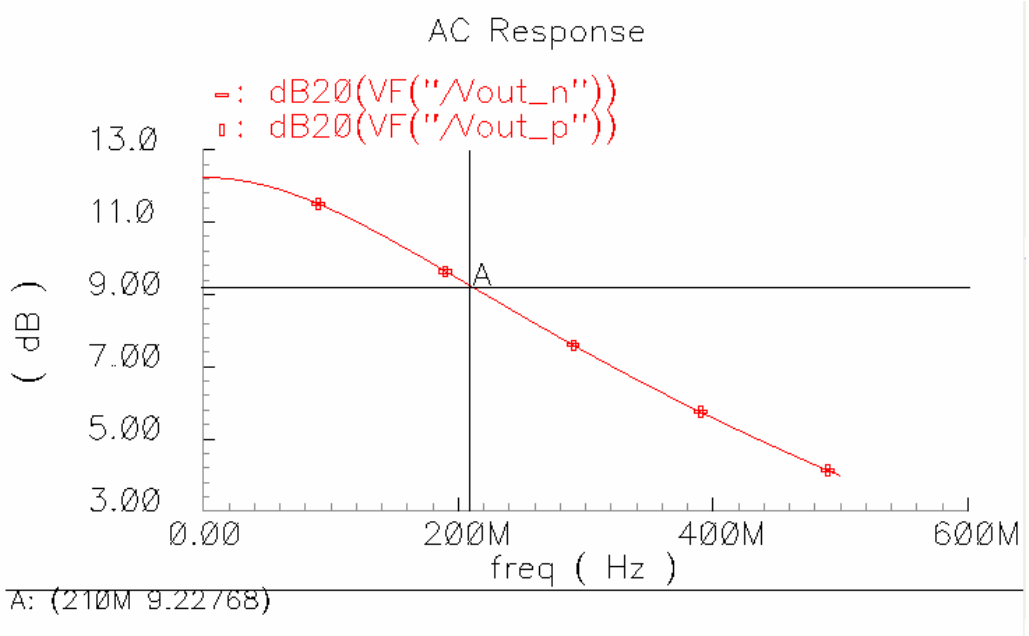


Figure 48 AC response of IF Amplifier

5.6 Clock Generator

Switched-capacitor circuits require the generation of two-phase non-overlapping clocks with delayed clocks to reduce signal-dependent charge injection [David97].

In the design, the four clock signals are driven by a master clock, supplied from an external source. A block diagram of the clock generator is shown in Figure49.

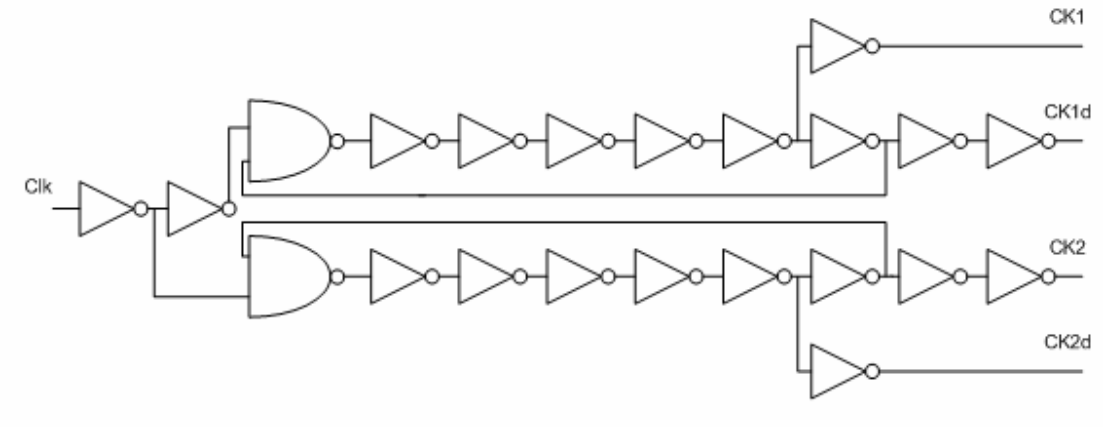


Figure 49　Schematic of the Clock Generator

Additional buffers are needed to be inserted to minimize the clock slew and minimize the clock jitter. Its transient response is shown in Figure50.

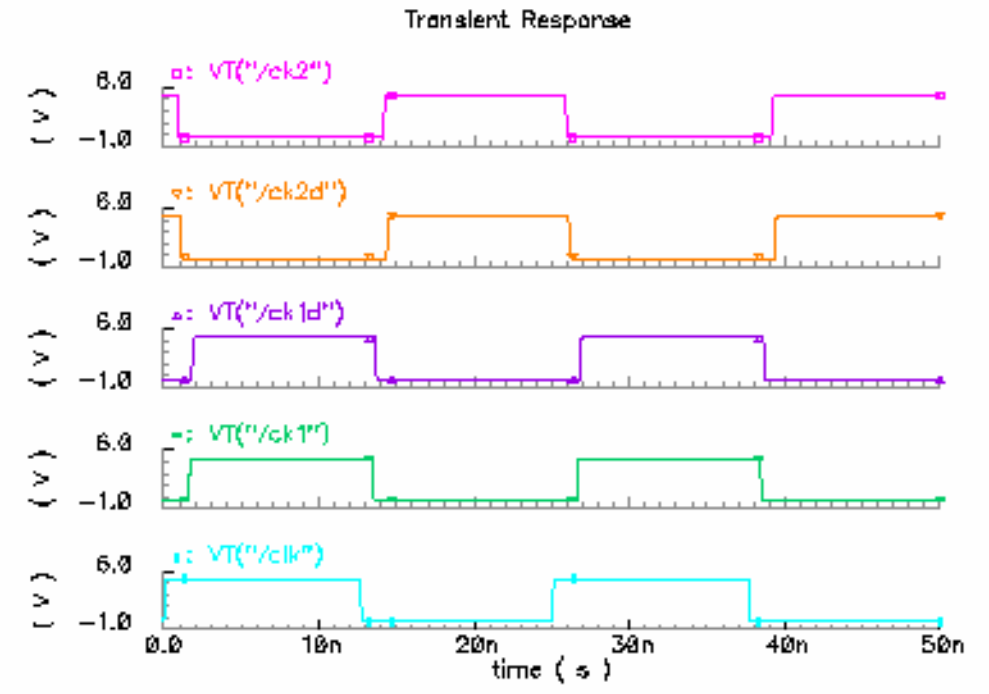


Figure 50　Transient Response of the Clock Generator

5.7 Layout Consideration

A number of layout strategies are adopted for the layout design: first, the analog cells are separated from the digital cells to reduce interference. Secondly, respect the symmetries that exist in the electrical network as well as in the layout (to limit offset).Thirdly, use low resistive paths (metal and not polysilicon) when large current needs to be carried (to avoid parasitic drop voltages). Finally, shield critical nodes (to avoid undesired noise injection).

The chip floor plan is shown as Figure 51.

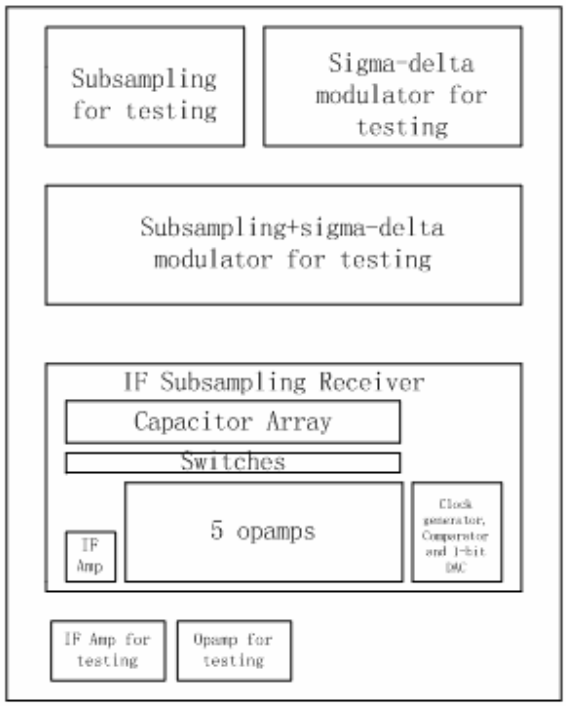


Figure 51 Layout Floor Plan

In the layout, there is a clear separation between analog and digital blocks. Digital blocks in our design include the comparator, clock generator. The analog circuits have a

different set of supplies from the digital circuits to decrease the noise. In addition, critical analog device and signal are placed far away the digital circuits.

Maintaining symmetry on the layout of the amplifiers and integrators preserves the many virtues of the fully-differential circuits. For example, Mirror symmetry of the layout can enhance the rejection of the common-mode disturbance in fully differential circuit.

Crossing routing is minimized wherever it is possible to reduce parasitic capacitances and reasonable wire width is used to reduce parasitic resistances. Moreover, to reduce noise coupling, the crossing between the signal paths and clock paths also need to be minimized.

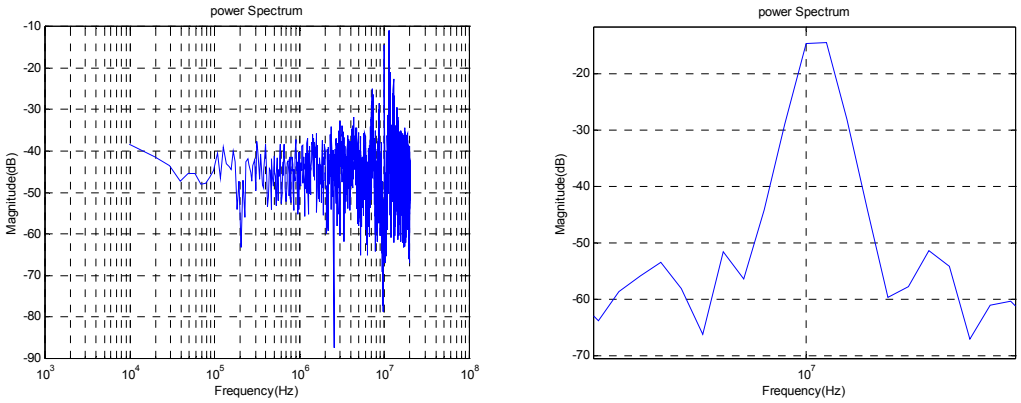
The capacitances are formed by connecting unit cells arranged in an array to decrease the capacitor mismatch. For example, the unit cell has a nominal capacitance of 200fF, the 400fF, 800fF, 1.6pF are formed by interconnecting 2, 4, 8 unit cell respectively. Dummy capacitors placed along outside edge of the capacitor array guarantee that the fringing fields at the periphery of the array are identical to those in the interior and insure that the unit cells are etched uniformly along all sides.

The final chip area is 3225x3225 micron with the pads. The chip is packaged in a DIL-48 package. The pin assignment and descriptions of chip pins as well as the chip microphotograph are given in Appendix B and C, respectively.

5.8 Schematic and Post-layout simulation

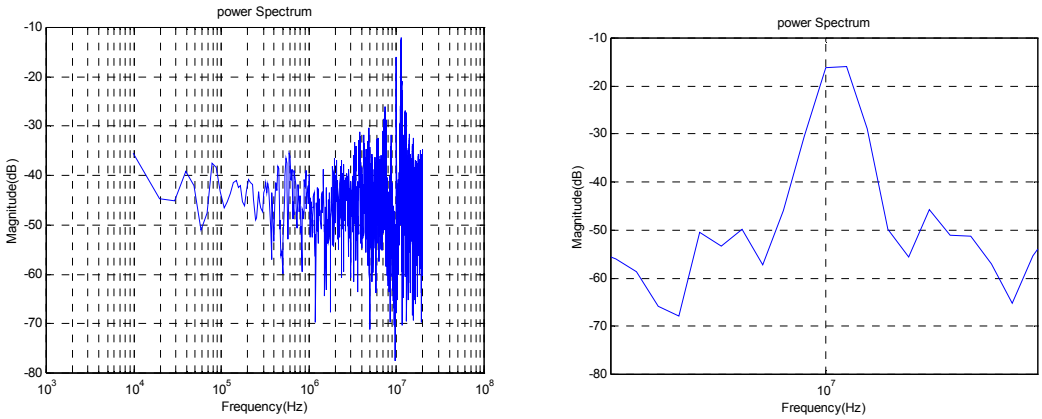
The IF receiver is simulated with an input signal of 210MHz and 40M clock. Since the receiver is designed for a channel bandwith of 200KHz, when the clock frequency is 40MHz, the oversampling rate (OSR) is 100. As described in the previous chapter, the IF amplifier should provide 9dB gain and the subsampling stage provides 0 or another 6dB gain. Due to the time limitation, simulation is only done with the overall gain set to 9dB.

All the stimulis of the schematic simulation and post-layout simulation are chosen to be same. The output power spectrums based on 4096-point fft are shown in Figure52 and Figure53, respectively.



(a) **(b)**

Figure 52 Schematic simulation results of IF receiver with 210-MHz input and 40-MHz clock (a) full scale, (b) zoom in 200k



(a) **(b)**

Figure 53 Post-layout simulation results of IF receiver with 210-MHz input and 40MHz (a) full scale , (b) zoom in 200k

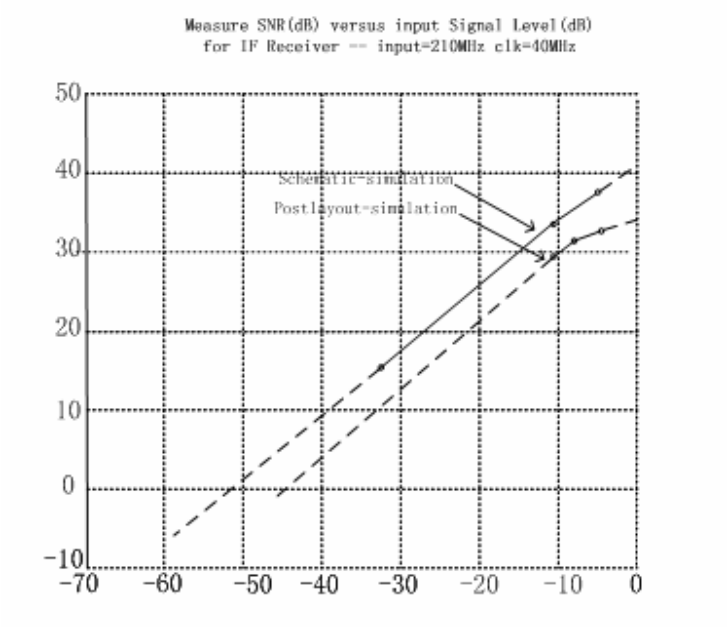
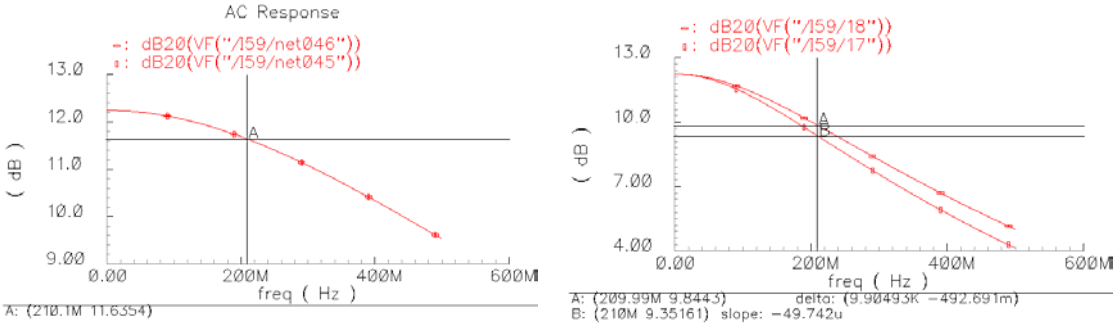


Figure 54 SNR performance comparison between schematic simulation and post-layout simulation

Source	Schematic simulation	Post-layout simulation
Input frequency	210MHz	
Clock frequency	40MHz	
Signal bandwidth	200KHz	
Supply Voltage	3.3V	
Overall gain	9dB	
Dynamic range	52dB	46dB
Peak SNR	41dB	34dB
Technology	0.6um single-poly, triple mental CMOS	

Table 6 Summary of schematic and post-layout simulation

The SNR performance comparison between schematic and post-layout simulation is shown in Fig 5.17 and summary is shown in Table 6. It can be seen that there are about 5dB discrepancies between these two simulations. This is partly attenuated to the loading of the IF amplifier. Simulation shows that the parasitic capacitance causes approximately 2dB gain degradation in the IF amplifier, as shown in Figure 55.



(a) **(b)**

Figure 55 AC Response of IF Amplifier with actual load (a) Schematic simulation, (b) Post-layout simulation

Chapter 6: Experimental Results

An experimental prototype of the IF sampling receiver is fabricated in AMS 0.6um, double-poly, triple-mental CMOS process.

This chapter describes the testing setup used to characterize the prototype chip and the measured results. Some discussions about the test results are also included.

6.1 Testing Setup

The complete testing setup is shown in Figure 56. The test board is a two-sided PCB board with separate analog and digital power supplies. The blocks inside the dotted line are built on PCB.

The input signal is generated by the RF signal generator and converts to the differential signals, in_p, in_n, by driving an external RF transformer. The common-mode voltage, Vcm, of the differential signals is set to 1.65V. A master clock, Clk, is generated by a pulse generator. Bias circuits provide the reference voltages and bias currents for the IF Receiver modulator. The output spectrum of the modulator, out_p, out_n, are observed using the spectrum analyzer. They also can be captured by the logic analyzer.

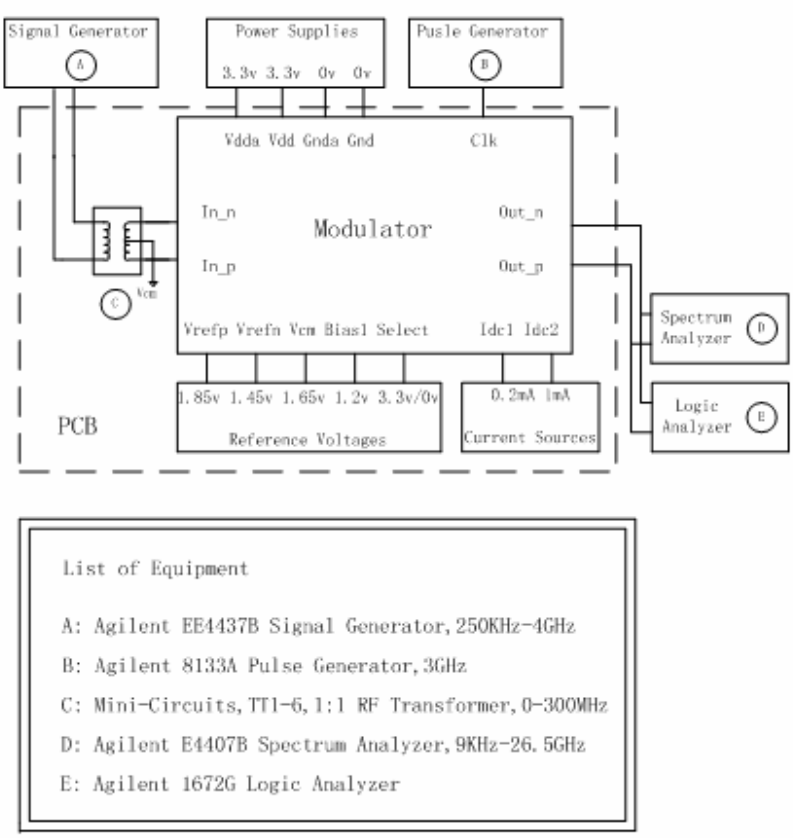
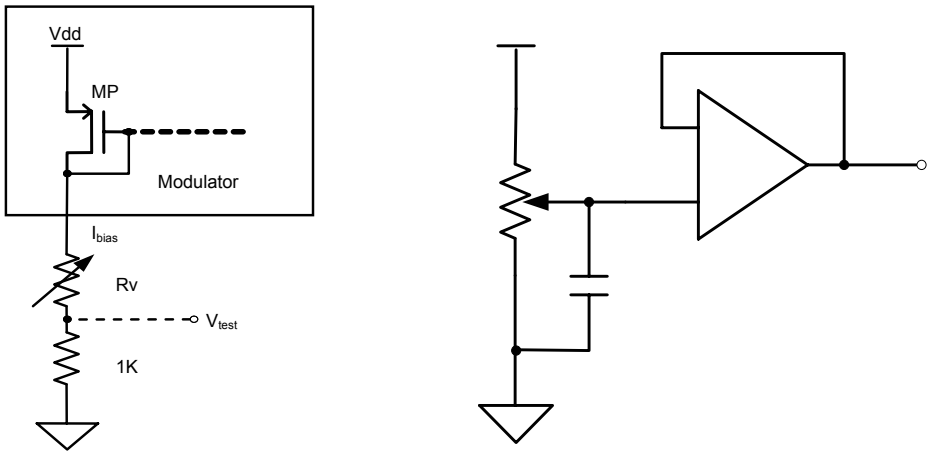


Figure 56 Experimental test setup of the modulators



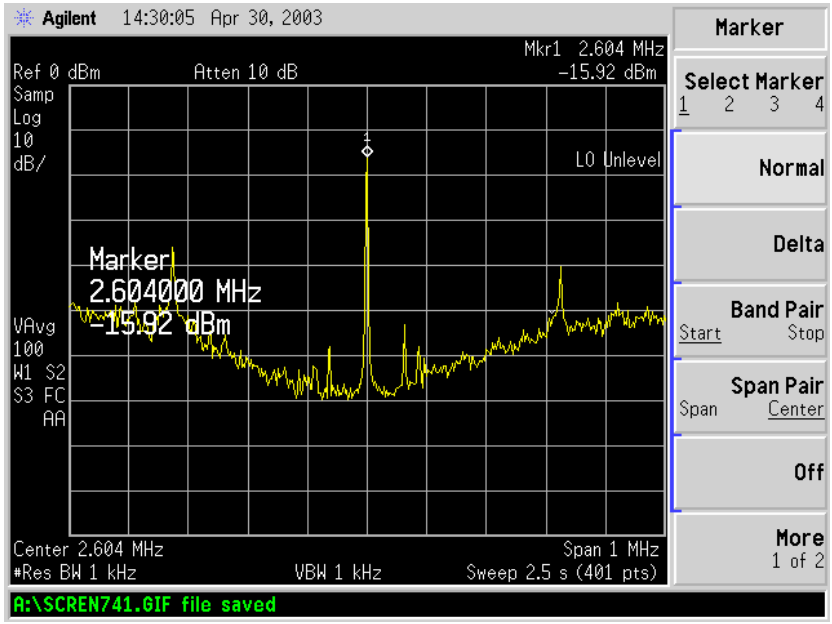
(a) **(b)**

Figure 57 Bias circuit (a) Bias current generation circuit (b) Reference voltage generation circuit

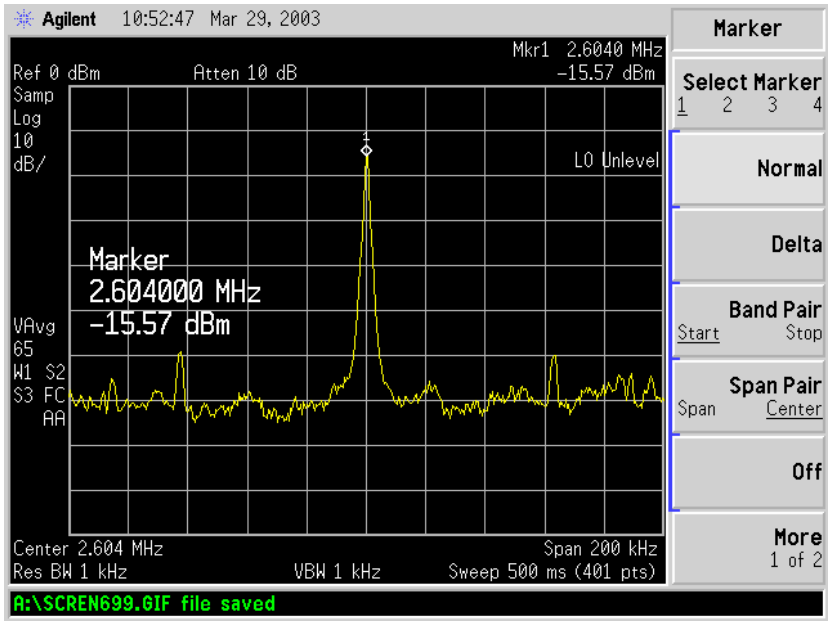
Bias circuits provide the bias currents and the reference voltages for the chip. The Figure 57 shows the bias circuits for the generation of the bias currents and reference voltages.

6.2 Testing Results

The modulator with subsample stage and 4th–order bandpass sigma-delta firstly is tested under different input frequencies and different clock frequencies. The power spectrums are shown on the Figure 58, Figure 59, Figure 60, respectively.



(a)



(b)

Figure 58 Subsample + 4th bandpass modulator output spectrum for Fin=13.02MHz; Fclk=10.416MHz (a) span=1MHz (b) span=200kHz

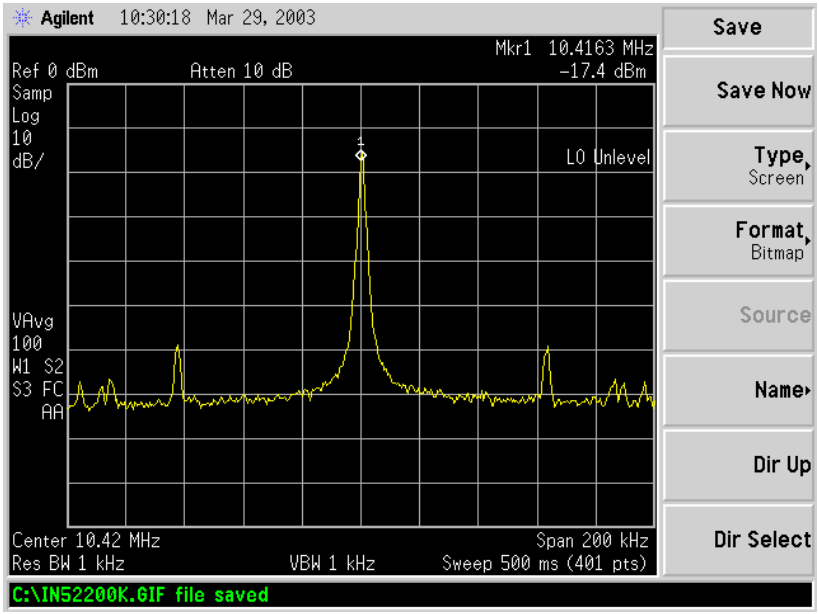


Figure 59 Subsample + 4th bandpass modulator output spectrum for Fin=52.08MHz; Fclk=41.67MHz

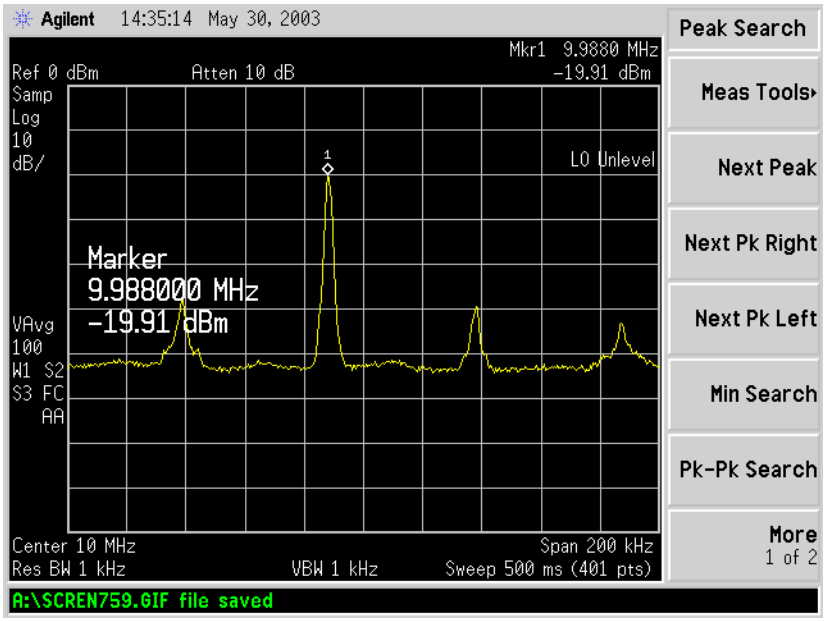


Figure 60 Subsample + 4th bandpass modulator output spectrum for Fin=210MHz; Fclk=40MHz

It can be seen that the modulator functions correctly. The noise shape can be clearly seen for the span of 1MHz. The inband noise floor is about 70dBm when the input frequency is 13MHz and clock frequency is 2.6MHz. When the input frequency increases to 210MHz and clock frequency increases to 40MHz, the inband noise level floor rises about 8dB.

The output spectrum of the IF sampling receiver with 210MHz input and 40MHz clock frequency is shown in Figure 60. The inband noise floor is slightly higher than the modulator without IF amplifier.

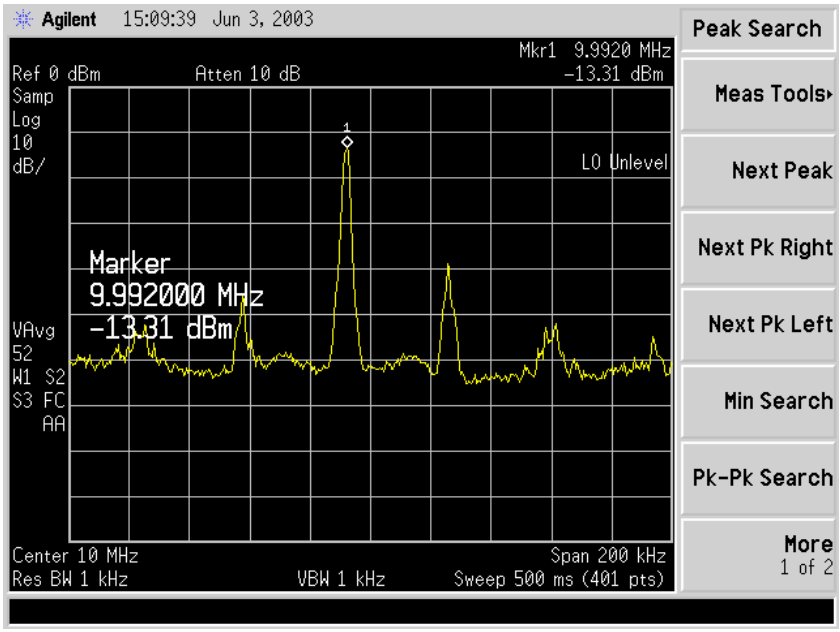


Figure 60 Output Spectrum of IF Receiver for Fin=210MHz; Fclk=40MHz

. The signal-to-Noise Ratio (SNR) is also evaluated. Since the receiver is designed for a channel bandwith of 200KHz, when the clock frequency is 40MHz, the oversampling rate

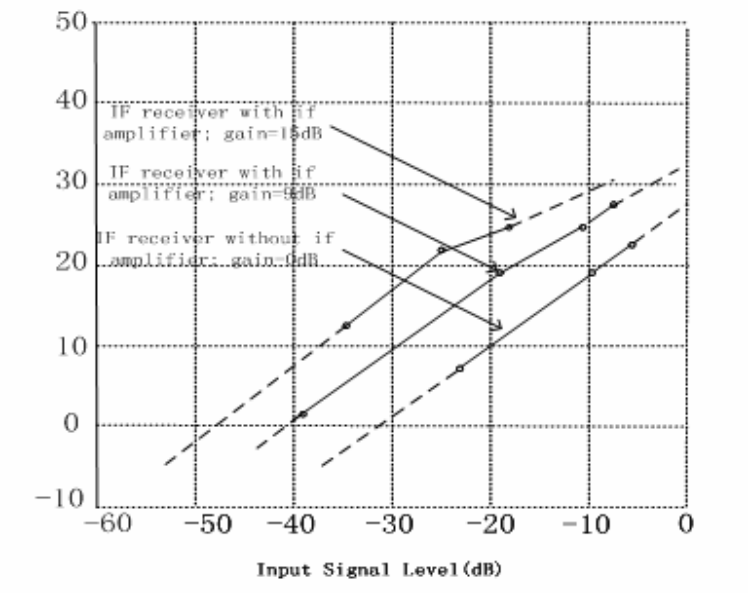


Figure 61 Measured SNR versus input amplitude for three gain settings; input=210MHz, clock frequency=40MHz

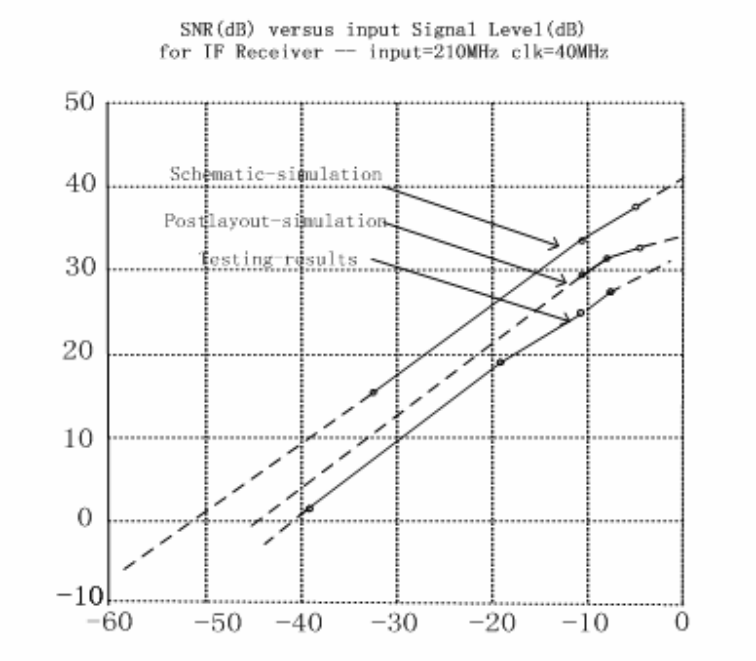


Figure 62 Compared SNR vs. input amplitude curves between schematic, post-layout simulation and measurement; for gain=9dB

(OSR) is 100. As described in the previous chapter, the IF amplifier provides 9dB gain and the subsampling gain stage provides 0, 6dB. So the IF receiver has two gain settings, 9dB and 15dB, respectively. In order to compare the effect of additional noise taken from IF amplifier, the receiver without IF amplifier (subsampling stage and 4^{th}-order bandpass sigma-delta modulator) for a 0dB gain setting is also tested.

The receiver performance evaluated by applying a 210MHz sinewave input and 40MHz clock frequency for three gain settings is shown in Figure 61. The curves indicate a dynamic range of 48dB and the peak SNR of 31dB.

The discrepancy between the receiver with IF amplifier and the receiver without IF amplifier is about 6dB-8dB. It is a slightly less than the gain of IF amplifier (about 9dB), the additional noise maybe due to the IF amplifier.

Source	Schematic	Post-layout	Testing
Input frequency	210MHz		
Clock frequency	40MHz		
Signal bandwidth	200KHz		
Supply Voltage	3.3V		
Overall gain	9dB		
Dynamic range	52dB	46dB	41dB
Peak SNR	41dB	34dB	31dB
Technology	0.6um single-poly, triple mental CMOS		

Table 7 Summary of schematic simulation, post-layout simulation and testing results

The comparion between schematic, post-layout simulation and measured results is also shown in Figure 62. The specifications of schematic simulation, post-layout simulation and experimental results are summaried in Table 7. Around -2 to -5 dB performance degradation between the post-layout simulation and measurement is observed. Some of this attributed to the loading of the parasitic to the IF amplifier, as mentioned in the previous chapter.

6.3 Summary of the Performance

The measured performance is summarized in Table 8.

Parameter	Value
Input frequency	210MHz
Clock frequency	40MHz
Signal bandwidth	200KHz
Dynamic range	48dB
Peak SNR	31dB
Supply Voltage	3.3V
Power Consumption	69.3mW
Core area	1.08mm^2
Technology	0.6um single-poly, triple mental CMOS

Table 8 Performance summary of IF receiver

Chapter 7: Conclusions

7.1 Conclusion

A high speed IF sampling receiver based on a subsampling gain stage and a fourth-order banpass sigma-delta A/D converter has been designed and evaluated. When compared with traditional superheterodyne receiver, the proposed IF sampling receiver has a higher level of integration and immune to dc offset, flicker noise and errors due to mismatches between *I* and *Q* signal path.

The subsampling track&hold circuit that performs down-conversion is realized using a fully differential switched-capacitor circuit with a programmable gain of 0dB or 6dB. By sampling the input signal at 40MHz, the 210-MHz IF_1 input is down-converted to 10MHz. The fourth-order bandpass sigma-delta modulator also implemented by the switched-capacitor technique, digitizes the down-converted IF_2 signal.

The IF receiver front end is fabricated with 0.6-um double-poly CMOS technology. The measured results show that the receiver is capable of digitizing the input IF_1 at 210-MHz when sampled at 40MHz. The dynamic range of the receiver is measured to be 48dB and the peak SNR is 31dB. The receiver is operated under a 3.3-V supply. The total power consumption of the receiver is 69.3mw.

Although the receiver is functional, it does not fully meet the specification. The performance degradation may partly due to the loading of the parasitic to the IF amplifier. Further improvement is needed.

7.2 Future Work

As the IF receiver does not fully meet its specification, further investigation needs to be carried out to find out the possible causes. The IF amplifier may be modified to avoid the parasitic loading effect and produces the desired gain. The subsampling stage should be further optimized to reduce the effect of noise sampling and clock jitter. Finally, other bandpass sigma-delta modulator structures, such as the N-path and the cascade high-order sigma-delta modulator, may be considered to further improve its dynamic range.

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Appendix A: Matlab Program for Behavior Simulation

```
%   Fourth-order Bandpass Sigma-delta modulator
%   System Achitecture Simulation
%   Program variable coressponds to Figure 30

%   clear working space and window
echo off
clear

%   Variable define
Fin=input('input signal frequency?');
size=input('numbers of datas?');
Fs=4*Fin;
SigPK=input('magnitude of input signal?');

%   File: SNR_f_4.txt and SNR_db_4.txt collect the datas for the SNR calculation
```

```
fid1=fopen('SNR_f_4.txt','w');
fid2=fopen('SNR_db_4.txt','w');

%   initial value
i=1;
N1(1)=SigPK*sin(2*pi*i*Fin/Fs+50);
N2(1)=SigPK*sin(2*pi*i*Fin/Fs+50);
N3(1)=0;N4(1)=0;
N5(1)=0;N6(1)=0;N7(1)=0;N8(1)=0;Y(1)=0;
i=2;
N1(2)=SigPK*sin(2*pi*i*Fin/Fs+50);
N2(2)=SigPK*sin(2*pi*i*Fin/Fs+50);
N3(2)=SigPK*sin(2*pi*(i-1)*Fin/Fs+50);
N4(2)=0;
N5(2)=0;N6(2)=0;N7(2)=0;N8(2)=0;Y(2)=0;

%   main program
while i<=size;
  i=i+1;
  X(i)=SigPK*sin(2*pi*i*Fin/Fs+50);
  N3(i)=N2(i-1);
  N4(i)=N3(i-1);
```

```
  N7(i)=N6(i-1);
  N8(i)=N7(i-1);
  N8Y(i)=2*N8(i);
   if  N8Y(i)>0;
      Y(i)=1;
   elseif  N8Y(i)==0;
      Y(i)=0;
    else
       Y(i)=-1;
     end
     N1(i)=X(i)-Y(i);
     N2(i)=N1(i)-N4(i);
     N45(i)=0.5*N4(i);
     N5(i)=N45(i)+Y(i);
     N6(i)=N5(i)-N8(i);
   end

%   plot PSD of the sigma-delta modulator
fclock=Fs;
fftpoints=1024*2;
window=hanning(fftpoints);
[pxx,f]=psd(Y,fftpoints,fclock,window);
normpxx=pxx*norm(window)^2/sum(window)^2;
```

```
db=10*log10(normpxx);
semilogx(f,db);
fprintf(fid1,'%d\n',f );
fprintf(fid2,'%d\n',db);
title('power Spectrum');
xlabel('Frequency(Hz)');
ylabel('Magnitude(dB)');
grid;
save result db;
fclose('all');
```

Appendix B: The Description of Chip Pins

No.	Name	Type	Analog/ Digital	Value	Description
1	Vdda	power	analog	3.3 V	Positive analog supply
2	Gnda	power	analog	0 V	Negative analog supply
3	Vdd	power	digital	3.3 V	Positive digital supply
4	Gnd	power	digital	0 V	Negative digital supply
5	Vin_p	input	analog		Positive input signal
6	Vin_n	input	analog		Negative input signal
7	Vin_p4	input	analog		Positive input signal for 4^{th}_bandpass_test
8	Vin_n4	input	analog		Negative input signal for 4^{th}_bandpass_test
9	Vin_p5	input	analog		Positive input signal for (opamp+if_amp)_test
10	Vin_n5	input	analog		Negative input signal for (opamp+if_amp)_test
11	Vrefp	input	analog	1.85 V	Positive reference voltage for 1-bit DAC
12	Vrefn	input	analog	1.45 V	Negative reference voltage for 1-bit DAC
13	clock	clock	digital	Low: 0 V High: 3.3 V	Main clock
14	Vcm	input	analog	1.65 V	Analog ground
15	Idc1	Bias current	analog	1mA	Bias current for all_circuit (LNA+subsample+4^{th}_bandpass)

16	Idc2	Bias current	analog	1mA	Bias current for circuits (subsample+4th_bandpass)
17	Idc3	Bias current	analog	1mA	Bias current for circuit subsample+4th_bandpass_test
18	Idc4	Bias current	analog	1mA	Bias current for if_amp (LNA+subsample+4th_bandpass)
19	Idc5	Bias current	analog	1mA	Bias current for if_amp _test_circuit
20	Idc6	Bias current	analog	0.2mA	Bias current for opamp _test_cicuit
21	latch	clock	digital	Low: 0 V High: 3.3 V	Latch of the comparator
22	Select	input	digital	Low: 0 V High: 3.3 V	Switch for the gain choice of subsample stage
23	Vout_p1	output	analog		Positive output signal for (LNA+subsample+4th_bandpass)
24	Vout_n1	output	analog		Negative output signal for (LNA+subsample+4th_bandpass)
25	Vout_p2	output	analog		Positive output signal for (subsample+4th_bandpass)
26	Vout_n2	output	analog		Negative output signal for (subsample+4th_bandpass)
27	Vout_p3	output	analog		Positive output signal for subsample
28	Vout_n3	output	analog		Negative output signal for subsample
29	Vout_p4	output	analog		Positive output signal for 4th_bandpass
30	Vout_n4	output	analog		Negative output signal for 4th_bandpass
31	Vout_p5	output	analog		Positive output signal for opamp
32	Vout_n5	output	analog		Negative output signal for opamp
33	Vout_p6	output	analog		Positive output signal for

					if_amp
34	Vout_n6	output	analog		Negative output signal for if_amp
35	Bias1	Bias voltage	analog	2.2v	Bias voltage for if_amp

Appendix C: Chip Microphotograph