MICROMECHANICAL RESONATOR BASED BANDPASS SIGMA- DELTA MODULATOR

WANG XIAOFENG

(B. of Eng., Northwestern Polytechnical University)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2003

Abstract

In modern RF receivers, high-speed and high-resolution ADCs are needed for IF or RF digitization. Bandpass ΣΔ modulator is seen as a potential candidate to fulfill this requirement. However, the speed of discrete-time bandpass ΣΔ modulator implemented with switched-capacitor circuit is limited by the settling time of the opamps, while the continuous-time bandpass modulator can operate at much high sampling frequency, but suffers from the degradation of dynamic range due to the low-Q LC or G_mC resonators.

This work is to investigate the possibility of employing micromechanical resonators in bandpass ΣΔ modulator design. The design of a newly proposed 2^{nd}-order bandpass ΣΔ modulator based on micromechanical resonator is presented. The micromechanical resonator is used to replace its electronic counterpart for its high Q value. The design is based on pulse-invariant transform and multi-feedback technique. A compensation circuit is proposed to cancel the anti-resonance in the micromechanical resonator in order to obtain the desired transfer function. The proposed modulator is implemented in a 0.6-μm CMOS process with an external clamped-clamped beam micromechanical resonator.

Due to the lack of qualified micromechanical resonator, the testing with the only micromechanical resonator did not give expected results. The test was subsequently carried out with crystal resonators and successfully demonstrated a 2^{nd}-order

bandpass ΣΔ modulator, which proves that the proposed idea is feasible. The test results have shown that when sampled at 4MHz the peak SNR in 200-kHz signal bandwidth is measured to be 22dB while the Matlab simulated value is 25dB. The modulator is also functional at the sampling frequency of 32MHz.

Acknowledgements

I would like to express my sincere appreciation to my supervisor Professor Xu Yong Ping for his guidance and support of my research in the past two years. I would also like to thank my co-supervisor Professor Tan Leng Seow for admitting me into NUS which makes my research possible. Many thanks go to my co-supervisor Dr. Wang Zhe of the Institute of Microelectronics (IME) for providing me the micromechanical resonators and the opportunity to access the equipment at IME.

I would like to thank Mr. Sun Wai Hoong. He generously shared his S-function programs with me. A numerous discussions with him are also very valuable.

I would also like to thank Mr. Saxon Liw of IME for his generous assistance and support in testing the resonator. He also helped me solve many practical problems.

I would like to express my gratitude to Miss Qian Xinbo, Mr. Su Zhenjiang, and Ms. Xu Lianchun for their help on circuit design and using Cadence. Xinbo also helped me a lot in using test equipment.

I would like to thank Miss Yu Yajun for providing me her past designs as reference. Thanks also go to Mr. Luo Zhenying, Mr. Liang Yunfeng, and Mr. Zhou Xiangdong for their advices on circuit design, and Mr. Francis Boey for his support on equipment and electronic components.

Very special thanks go to all my friends at the Laboratory of Signal Processing and VLSI Design for making my years in NUS a wonderful experience.

I would like to thank the National University of Singapore for providing me with the financial support.

Finally, I would like to thank my parents and my grandparents for their consistent support.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

One of the major technical successes in the 20th century is the development of wireless communication systems which origins in 1980s. It is estimated there are 440 million wireless subscribers worldwide by the end of year 2002. The wireless equipment industry worldwide is estimated at $45 billion annually. The number of subscribers is expected to double in several years. Driven by the great demand of personal communication systems, the wireless communication technology has developed rapidly to provide more and better services. As a key part in wireless communication system, the Radio Frequency (RF) receiver has attracted great research attention.

1.1 Motivation

In the RF receiver design, most of the efforts are made to improve the integration and flexibility. High-level integration will increase the system reliability and reduce its cost, size and power consumption. More flexibility, on the other hand, will make the receiver compatible to multiple standards.

Currently, most of the RF receivers are implemented in the super-heterodyne architecture with baseband ADC (Analog-to-Digital Converter). The block diagram of a dual-IF super-heterodyne receiver with baseband ADC is shown in Figure 1 [Carl86].

The RF signal is filtered and mixed through two IF stages, then demodulated and converted into digital domain with baseband ADC. The superheterodyne architecture

has good sensitivity and selectivity, but it is complex, requires precise analog components and has many off-chip filters, so it is difficult to realize high integration and good flexibility.

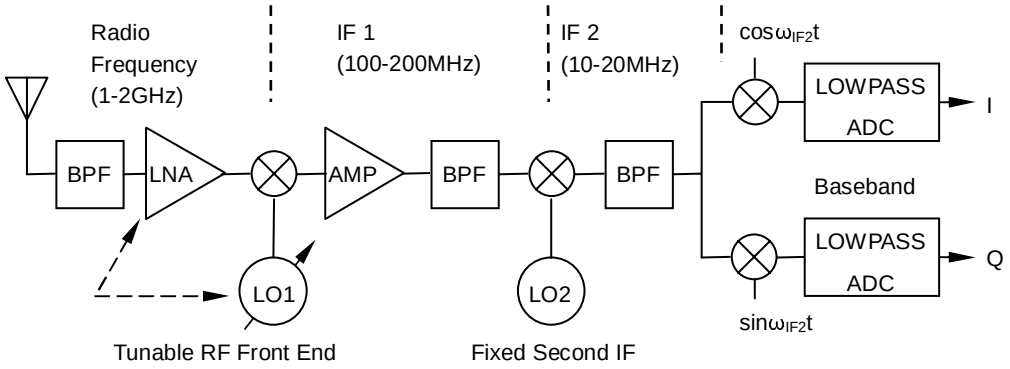


Figure 1. Superheterodyne receiver with dual IF and baseband ADC.

The research on new receiver architectures is carried out in two directions [Galt02]: one is to convert the RF signal directly to baseband or low-IF and use baseband ADC to convert the signal into digital domain. Such architectures are called zero-IF or low-IF direct conversion. Another direction is to use bandpass ADC to convert the signal into digital domain at IF, or even at RF frequency, such architectures are called superheterodyne receiver with bandpass ADC or direct-IF receiver [Galt02]. The block diagrams of direct-conversion receiver and bandpass ADC based direct-IF conversion receiver are shown in Figure 2 [Galt02] and Figure 3 [Galt02], respectively.

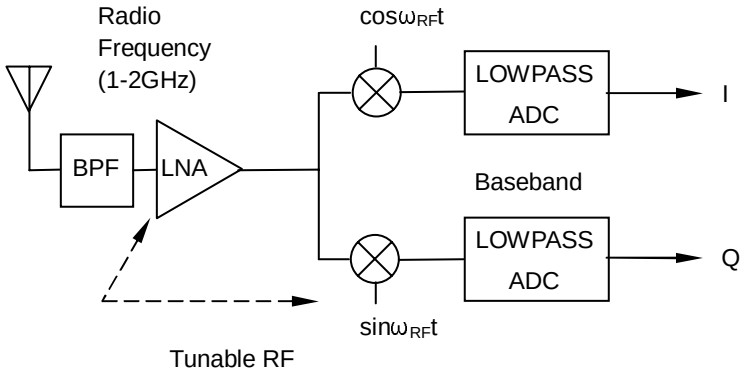


Figure 2. Direct-conversion receiver.

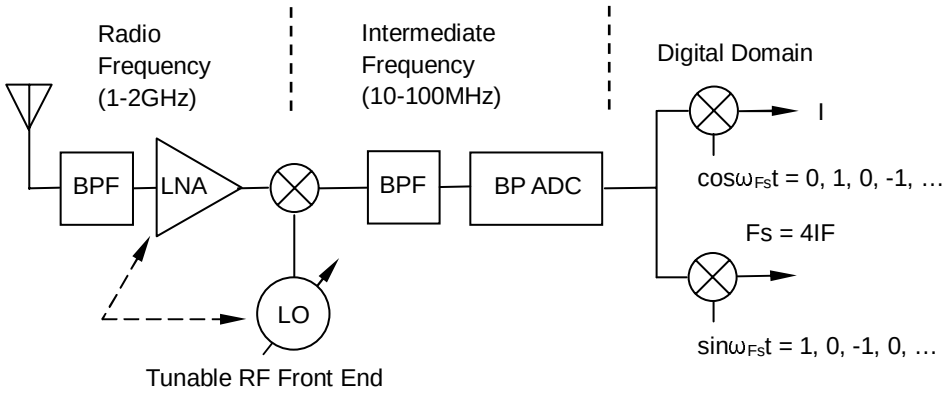


Figure 3. Direct-IF conversion receiver.

In the direct-conversion receiver, the RF signal is directly translated down to the baseband, where demodulation and A/D conversion are done. The direct-conversion relaxes the selectivity requirements on RF filters and eliminates all IF analog components, allows a highly integrated, low-cost and low-power realization of RF receivers [Abid95]. However, direct-conversion receivers have a severe DC offset problem that will affect the circuit biasing conditions. 1/f noise also degrades the dynamic range of the receiver.

In the bandpass ADC based superheterodyne receiver, the signal is converted to digital domain at IF. Compared with conventional superheterodyne receiver, the demodulation and channel selection in this architecture are done in digital domain, which alleviates the precision requirements on analog components. The channel selection is programmable so the flexibility is increased. The integration is also improved since the system structure is simplified. Moreover, compared with direct-conversion, the problems of 1/f noise and DC offset are avoided with the technique of direct IF digitization. The architecture is suitable for many RF receiver applications, such as, software-controlled digital radios. However, this architecture

requires high-frequency and high-resolution bandpass A/D converters. Bandpass Sigma-Delta (ΣΔ) ADC is seen as a good candidate in this application, since it can be realized in high resolution with coarse analog circuitry.

Currently, most of the bandpass ΣΔ ADCs reported are implemented using switched-capacitor circuits [Sing95] [Baza98]. Such converters have robust performance, but only at low frequencies. When their sampling frequency increases, the non-idealities of the circuit (such as the finite gain and settling error of the op-amp) degrade the performance. Continuous-time bandpass ΣΔ ADCs, on the other hand, can operate at high frequencies. But their performance is limited by the low Q factor and nonlinearity of the on-chip resonators [Shoa95] [Gao98].

In the past decades, the rapid development in silicon micromachining technology has led to the realization of micromechanical resonators (also called as μresonator) on silicon. Micromachining process can be made compatible with CMOS technology [Bust98] [Nguy01]. Therefore, it is possible to integrate micromechanical devices with CMOS circuit on a single chip. Different types of micromechanical resonators have been reported [Nguy01]. The major advantage of the micromechanical resonator is its high Q value (typically greater than 1000), which cannot be matched by its electronic counterpart, especially at high frequencies. In bandpass ΣΔ modulators, high-Q resonator provides better noise shaping and hence better performance. Therefore micromechanical resonator is a good candidate to replace conventional LC and G_mC resonators in high-speed bandpass ΣΔ ADC design.

The research carried out in this thesis is to investigate the possibility of realizing

bandpass ΣΔ modulator using micromechanical resonator. The intended application is IF digitization in modern RF receivers.

1.2 Thesis Outline

Chapter 2 of the thesis introduces the fundamentals of ΣΔ modulation and reviews the previous work on continuous-time bandpass ΣΔ modulator. Chapter 3 introduces micromechanical resonators. Chapter 4 describes system-level design of the proposed modulator. Chapter 5 deals with circuit-level implementation. Chapter 6 presents the testing results and Chapter 7 summarizes this research and suggests the future work.

Chapter 2 Sigma-Delta Modulation

According to the relationship between sampling frequency and signal bandwidth, A/D converters can be categorized into Nyquist-rate and Oversampling A/D converters. ΣΔ A/D converters belong to oversampling A/D converter.

This chapter reviews the fundamentals of Nyquist-rate A/D converter. The theory of oversampling A/D conversion and different modulator structures are then introduced. The previous work on continuous-time bandpass ΣΔ modulator is reviewed and their limitations are analyzed. Finally the idea of micromechanical resonator based continuous-time bandpass ΣΔ modulator is proposed.

2.1 Nyquist-rate A/D Converter

A/D conversion is a process of sampling in time and quantization in magnitude on an analog signal. The process of conversion can be divided into anti-aliasing filtering, sampling and holding, and quantization. The operation is shown in Figure 4.

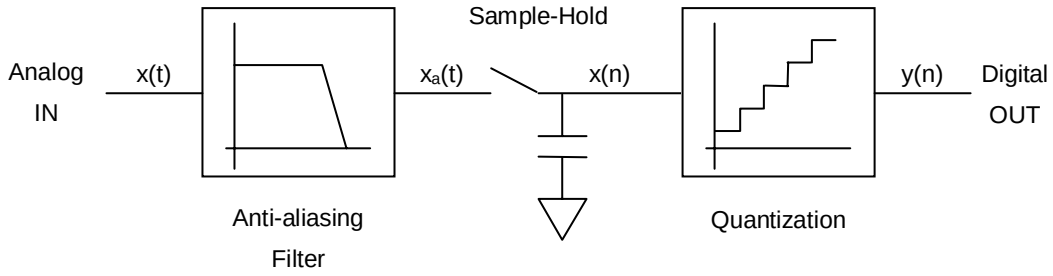


Figure 4. The operation of Nyquist-rate A/D converter.

2.1.1 Anti-aliasing

The analog signal must pass through a lowpass anti-aliasing filter to remove the signal components which are above 1/2 of the sampling frequency. Otherwise, high frequency components will alias into the baseband upon sampling and will corrupt the signal of interest.

2.1.2 Sampling

From the Nyquist sampling theorem [Oppe89], if the sampling frequency is higher than two times of the signal bandwidth, there is no loss of information or aliasing upon sampling. The sampling frequency which is two times of the signal bandwidth is called Nyquist sampling rate. Generally, in real applications, to alleviate the constraints on anti-aliasing filters, sampling frequency is chosen to be higher than the Nyquist sampling rate. If the sampling-rate is chosen at or slightly higher than the Nyquist rate (1.5 to 10 times [John97]) and the digital output rate equals the sampling rate, the A/D converter is called Nyquist-rate A/D converter. Otherwise, if the sampling rate is much higher than the Nyquist rate (typically 20 to 512 times [John97]) and digital filter is used to decimate the high-rate bit stream to Nyquist rate and remove the out-of-band quantization noise, the A/D converter is called oversampling A/D converter.

2.1.3 Quantization

When the data is sampled and held, it is converted to digital value by a quantizer. This process is called quantization. Consider the block diagram of an N-bit A/D

converter shown in Figure 5 [John97], where B_{out} is the digital output word, while V_{in} is the analog input signal and V_{ref} is the reference signal. b_1 and b_n represent the most significant bit (MSB) and least significant bit (LSB), respectively.

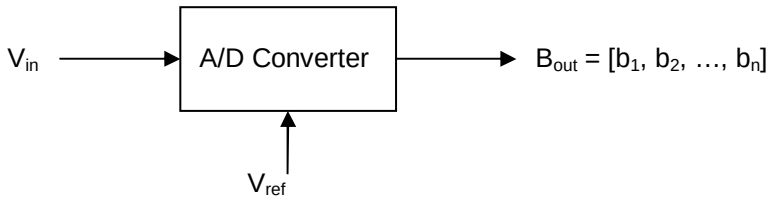


Figure 5. A/D conversion process.

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_n 2^{-n}) = V_{in} + e \quad (1)$$

where $-\frac{1}{2}V_{LSB} \le e \le \frac{1}{2}V_{LSB}$, e is quantization error. Because the quantization error is non-linear and signal dependent, it's difficult to analyze it. To simplify the analysis, the quantization error is often approximated to an additive white noise and is analyzed with statistical methods. Such an assumption is valid if the following conditions are satisfied [Benn48] [Widr56]:

1) The input signal never overloads the quantizer.
2) The quantizer has a large number of quantization levels.
3) The input signal is active over many quantization levels, and
4) The joint probability density of any two quantizer input samples is smooth.

With the white noise assumption, the non-linear quantizer can be modeled as a linear system shown in Figure 6.

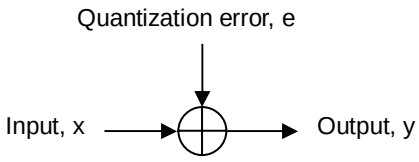


Figure 6. Linear model for quantization.

The output y is a combination of the input *x* and uncorrelated white quantization noise *e*:

$$y = x + e. \tag{2}$$

Since the quantization error is correlated with input signal, this white noise assumption is never exact, although the correlation is often too complex to be expressed analytically. Nevertheless, this model can be used to analyze the performance of a quantizer and it gives reasonable predictions in most cases.

With the above assumption, if the quantization step is defined as Δ, the power of quantization error can be expressed as [John97]:

$$e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}. \tag{3}$$

With a sampling frequency of f_s, the quantization noise will fold into the band of $[0, f_s/2]$. The spectral density of the quantization noise sampled is given by

$$E(f) = \sqrt{\frac{e^2}{f_s/2}} = e\sqrt{\frac{2}{f_s}}. \tag{4}$$

For a sinusoidal input signal with a full-scale magnitude of V_{ref}, the ac power of the input signal is $V_{ref}^2/8$. For $2^N >> 1$,

$$1LSB = \frac{V_{ref}}{2^N - 1} \approx \frac{V_{ref}}{2^N} = \Delta. \tag{5}$$

The SNR (Signal-to-Noise Ratio), which is defined as the ratio of signal power against the power of in-band noise can be obtained:

$$SNR = 10\log_{10}\left(\frac{V_{ref}{}^2/8}{\Delta^2/12}\right) = 6.02N + 1.76dB, \tag{6}$$

where, N is the bit number of the quantizer.

2.2 Oversampling A/D Converter

Oversampling A/D converters are sampled at a frequency much higher than the Nyquist rate. Compared with Nyquist-rate A/D converter, oversampling A/D converter can achieve high resolution with relatively coarse analog circuits. Since the sampling frequency is much higher than Nyquist rate, the constraints on anti-aliasing filter is alleviated. The sharp cut-off filter is not necessary which makes it possible to implement the filter on-chip. Another advantage of oversampling A/D converter is that the sample-hold stage is generally not required.

We define the Oversampling Ratio (OSR) as the sampling frequency over the Nyquist-rate. If the input signal bandwidth is [0, f_B],

$$OSR = f_s / 2 f_B . \tag{7}$$

For bandpass oversampling ADC, OSR is defined as the sampling frequency over two times of the bandwidth,

$$OSR = f_s / 2BW . \tag{8}$$

The spectral density of the quantization noise after sampling is shown in Eq. (4) and the in-band noise can be calculated:

$$n_{ib} = \int_0^{f_B} E^2(f) df = e^2 \frac{2 f_B}{f_s} . \tag{9}$$

For a Nyquist-rate ADC, $f_s=2f_B$, thus $n_{ib} = e^2$.

For an oversampling ADC,

$$n_{ib} = e^2 \frac{2 f_B}{f_s} = \frac{e^2}{OSR} = \frac{\Delta^2}{12 OSR}. \quad (10)$$

From the Eq. (10), it can be seen that the in-band noise can be reduced if OSR is increased. For every doubling of OSR, the in-band noise can be reduced by 3dB, which is equivalent to a half bit.

However, this SNR improvement is very limited. To further improve the in-band SNR, another technique called noise-shaping can be applied, which shapes the quantization noise out of the band of interest. The oversampling A/D converter that uses the noise-shaping technique is called ΣΔ A/D converter.

2.3 Sigma-Delta Modulation

The basic concept of ΣΔ modulation is the use of feedback to improve the effective resolution of a coarse quantizer. ΣΔ modulation was first proposed by Inose, and Yasuda in 1962 [Inos62]. The block diagram of a ΣΔ modulator is shown in Figure 7.

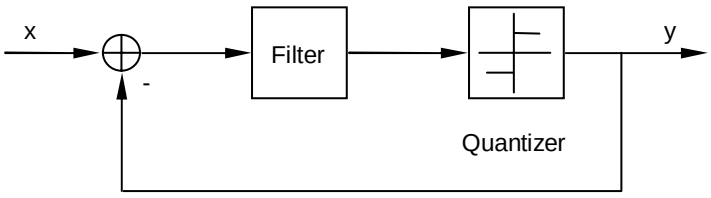


Figure 7. ΣΔ modulator.

A ΣΔ modulator is composed of a loop filter, a quantizer and a DAC in the feedback loop. The ΣΔ modulator is to modulate the analog input signal into a digital sequence which, in the frequency domain, approximates the input very well at certain frequencies. The feedback structure also shapes the quantization noise out of the signal band, thus high in-band resolution can be realized.

2.3.1 The Noise-shaping Technique

By applying the linear model of the quantizer discussed in Section 2.1, a linear model of the ΣΔ modulator can be obtained as shown in Figure 8. *H(z)* is the *Z*-domain transfer function of the loop filter.

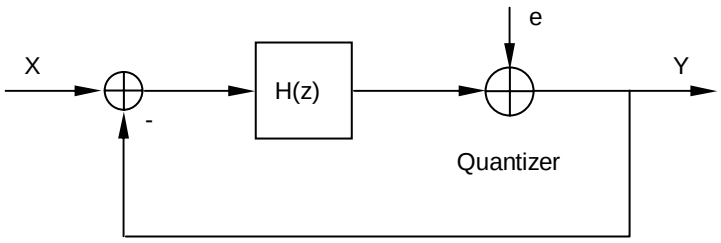


Figure 8. Linear model of ΣΔ modulator.

The linear model assumes that the quantization noise is white, additive and independent of input *X*. Under this assumption, the output of the modulator can be expressed as

$$y(z) = \frac{H(z)}{1+H(z)}x(z) + \frac{1}{1+H(z)}e(z). \tag{11}$$

where the signal transfer function is

$$STF = \frac{H(z)}{1+H(z)}; \tag{12}$$

and the noise transfer function is

$$NTF = \frac{1}{1+H(z)}. \tag{13}$$

It can be seen from Eq. (11) that the poles of *H(z)* become the zeros of *NTF*. At the frequencies which satisfy $H(z) >> 1$, $y(z) \approx x(z)$, that is, at these frequencies the signal is transferred while noise is attenuated. The concept can be demonstrated with the lowpass ΣΔ modulator shown in Figure 9.

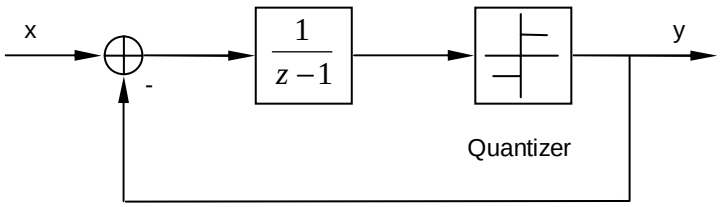


Figure 9. Lowpass ΣΔ modulator.

The forward loop filter for a 1st-order lowpass ΣΔ modulator is simply an integrator with a pole at DC. From Eq. (11), the signal transfer function can be calculated to be Z^{-1}, which is merely a unit delay; while the noise transfer function is *(Z-1)/Z*. The signal and noise transfer functions obtained in Matlab are shown in Figure 10. The output spectrum of the modulator is shown in Figure 11. At the frequencies close to DC, *H(z) >> 1*, the gain of the quantization noise is close to zero, so the quantization noise is shaped away from these frequencies. Such a technique that shapes the spectrum of the noise is called noise shaping.

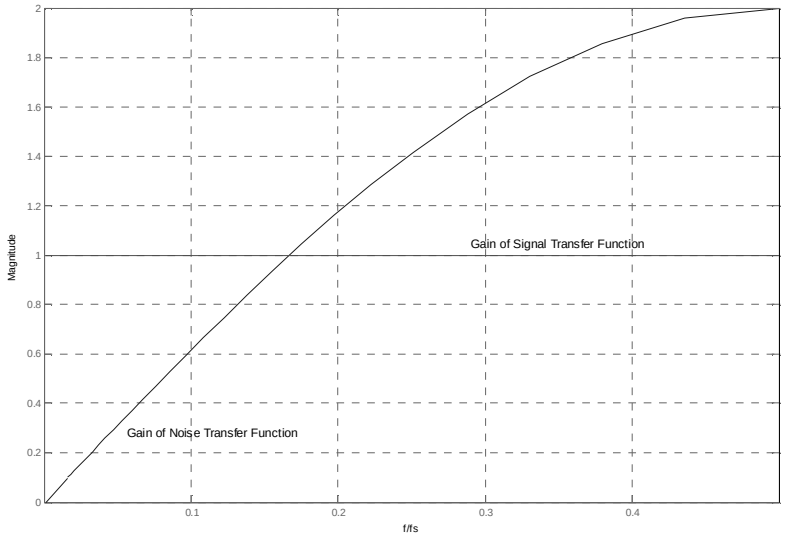


Figure 10. Gain of NTF and STF of the lowpass ΣΔ modulator.

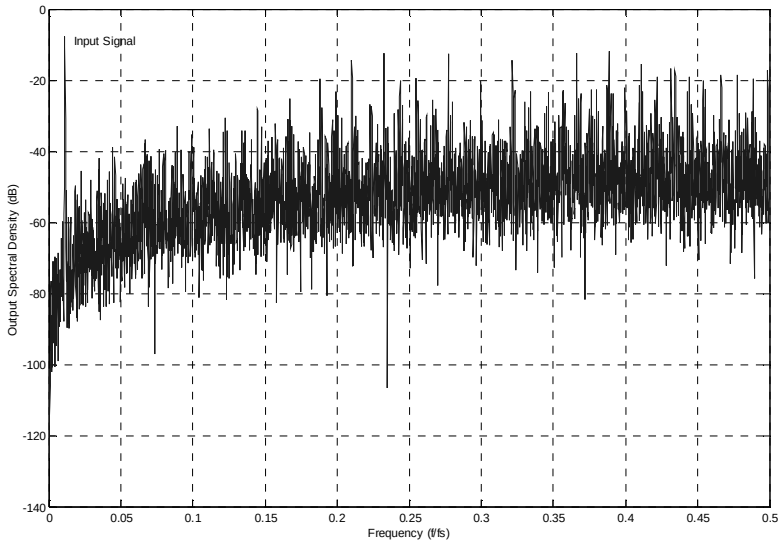


Figure 11. Simulated output spectrum.

For the 1st-order lowpass ΣΔ modulator, the in-band noise can be calculated as follows:

$$
\begin{aligned}
e_{ib}{}^2 &= \int_0^{f_b} e^2(f)\left|\frac{z-1}{z}\right|^2 df \\
&= \int_0^{f_b} \frac{e^2}{f_s/2}\left|1-z^{-1}\right|^2 df \\
&= \int_0^{f_b} \frac{\Delta^2/12}{f_s/2}\left|1-e^{-j\omega T_s}\right|^2 df \\
&= \int_0^{f_b} \frac{\Delta^2/6}{f_s}(2-2\cos\frac{2\pi f}{f_s})df \\
&= \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{1}{OSR^3}
\end{aligned}
\qquad (14)
$$

where f_B is the signal bandwidth.

It can be seen that doubling of OSR will lead to 9dB, equivalent to 1.5bit, increase in SNR. The increase is much higher than that of the oversampling converter without noise-shaping as indicated in Eq. (10). Eq. (14) also shows that high OSR is desired in ΣΔ modulation.

A complete block diagram of baseband ΣΔ A/D converter is shown in Figure 12.

The converter is composed of a ΣΔ modulator and a digital decimator. The decimator filters out the out-of-band noise and decimates the high-rate bit stream into Nyquist rate.

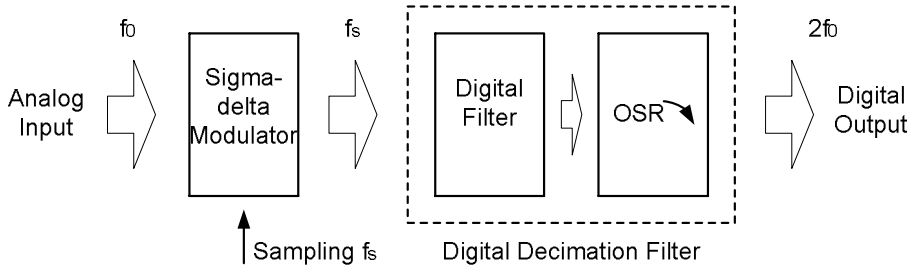


Figure 12. Structure of baseband ΣΔ A/D converter.

The ΣΔ modulation can also be extended to bandpass applications. If a resonator is used to replace the lowpass filter in the forward loop, the quantization noise will be shaped away from the resonant frequency instead of DC. Bandpass decimation circuit is used after the bandpass modulator to remove the out-of-band noise, so that high SNR can be obtained in the band of interest. In bandpass ΣΔ modulator, the sampling frequency is generally selected to be four times of the resonant frequency to simplify the design [Sing95]. A bandpass ΣΔ modulator is shown in Figure 13.

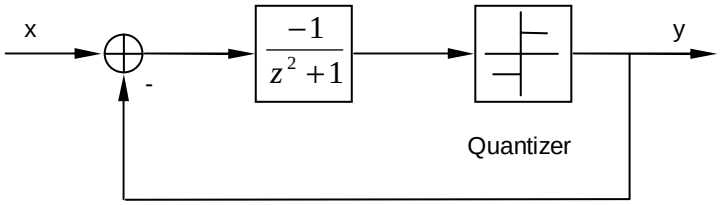


Figure 13. Bandpass ΣΔ modulator.

The output of the modulator can be written as:

$$y(z) = -x(z)z^{-2} + e(z)\frac{z^2+1}{z^2}. \quad (15)$$

The input signal is just delayed by two clocks cycles, but the quantization noise is shaped. The frequency responses of the signal transfer function and noise transfer function for a 2nd-order bandpass ΣΔ modulator are shown in Figure 14. It can be seen

at the resonant frequency, that is, one fourth of the sampling frequency, the quantization noise is close to zero. The output power spectrum obtained with Matlab simulation is shown in Figure 15. It is evident that the quantization noise is shaped away from the resonant frequency.

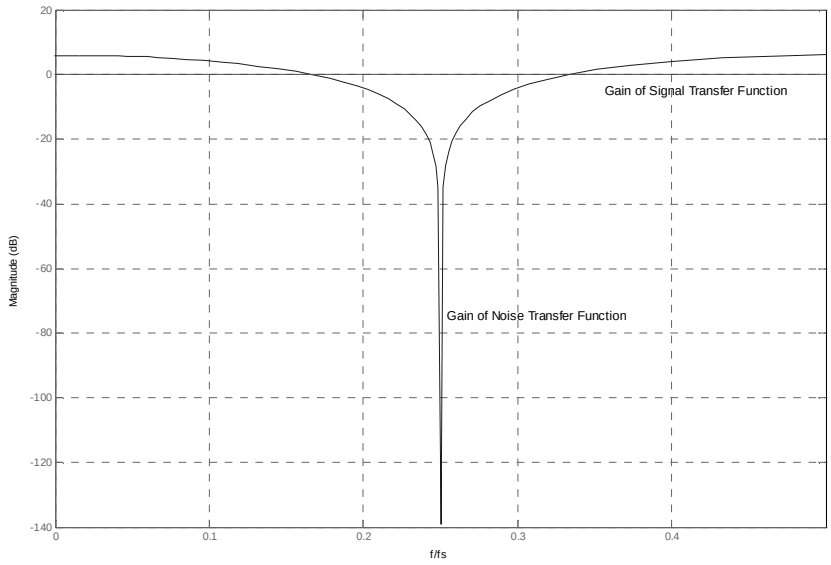


Figure 14. Magnitude responses of NTF and STF of a 2nd-order bandpass ΣΔ modulator.

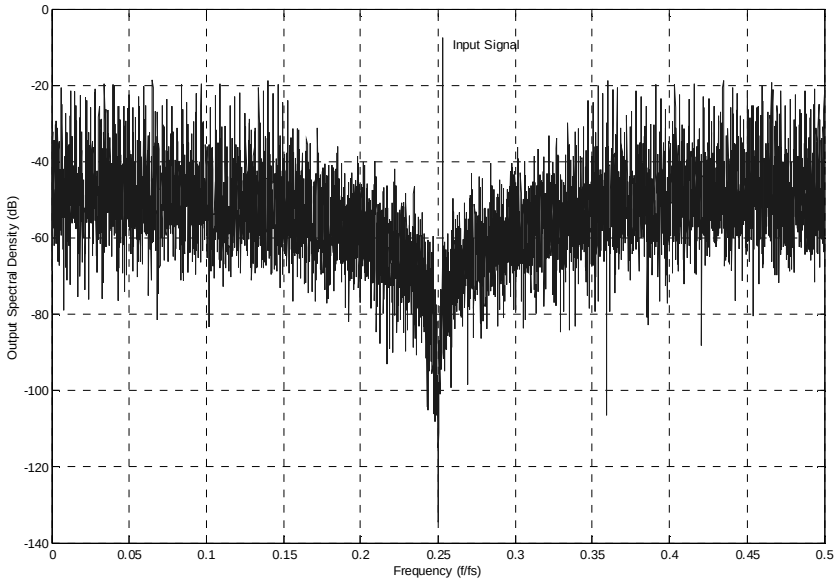


Figure 15. Output power spectrum of a 2nd-order bandpass ΣΔ modulator.

The in-band noise can be calculated as below:

$$
\begin{aligned}
e_{ib}{}^2 &= \int_{f_o-BW/2}^{f_o+BW/2} e^2(f)\left|\frac{z^2+1}{z^2}\right|^2 df \\
&= \int_{f_o-BW/2}^{f_o+BW/2} \frac{e^2}{f_s/2}\left|1+z^{-2}\right|^2 df \\
&= \int_{f_o-BW/2}^{f_o+BW/2} \frac{\Delta^2/12}{f_s/2}\left|1+e^{-j2\omega T_s}\right|^2 df \\
&= \int_{f_o-BW/2}^{f_o+BW/2} \frac{\Delta^2/6}{f_s}(2+2\cos\frac{4\pi f}{f_s})df \qquad , \quad (16) \\
&= \frac{\Delta^2}{3f_s}[BW-\frac{f_s}{2\pi}\sin\frac{2\pi BW}{f_s}] \qquad (f_s = 4f_0) \\
&\approx \frac{\Delta^2}{3f_s}\{BW-\frac{f_s}{2\pi}[\frac{2\pi BW}{f_s}-\frac{1}{3!}(\frac{2\pi BW}{f_s})^3]\} \qquad (f_s >> 2\pi BW) \\
&= \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{1}{OSR^3}
\end{aligned}
$$

where the band of interest is [f_0-BW, f_0+BW] and signal frequency is f_s.

Compared Eq. (14) and Eq. (16), it is noticed that the in-band noise power of the 2nd-order bandpass modulator is the same as the 1st-order low-pass modulator.

2.3.2 High-order Sigma-Delta Modulation

In the last section, the noise transfer function has been introduced. Generally, the order of the modulator is defined according to the order of its noise transfer function. High-order modulators will lead to better noise-shaping. It has been proven that, for an Lth-order lowpass modulator, (*6L+3*) dB SNR increase can be obtained when doubling the OSR [Cand92].

One method to realize high order ΣΔ modulator is to directly cascade filters in the forward path of the modulator loop while employing only one quantizer. This architecture is called single-stage or multi-loop ΣΔ modulator. A 2nd-order single-stage

lowpass ΣΔ modulator is shown in Figure 16 [Cher00]. Care should be taken in designing a single-stage ΣΔ modulator when its order is higher than two, as it may not be stable.

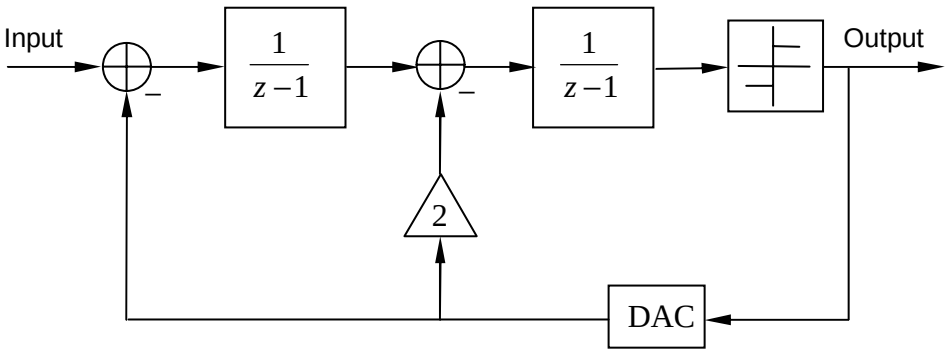


Figure 16. 2nd-order single-stage lowpass ΣΔ modulator.

Another method is to use multi-stage structure (typically called MASH, for multi-stage noise-shaping [Hay86]). A second-order lowpass MASH ΣΔ modulator is shown in Figure 17 [Cher00]. The output can be expressed as

$$Y = X + (1 - z^{-1})^2 e_2 . \qquad (17)$$

The 1st-order shaped quantization noise from the first stage is cancelled by the second stage and 2nd-order noise-shaping is achieved. Theoretically, the structure can be extended to high-order noise-shaping with unconditional stability since each 1st-order stage is unconditional stable. However mismatches between components in the stages result in imperfect noise cancellation [Mats87].

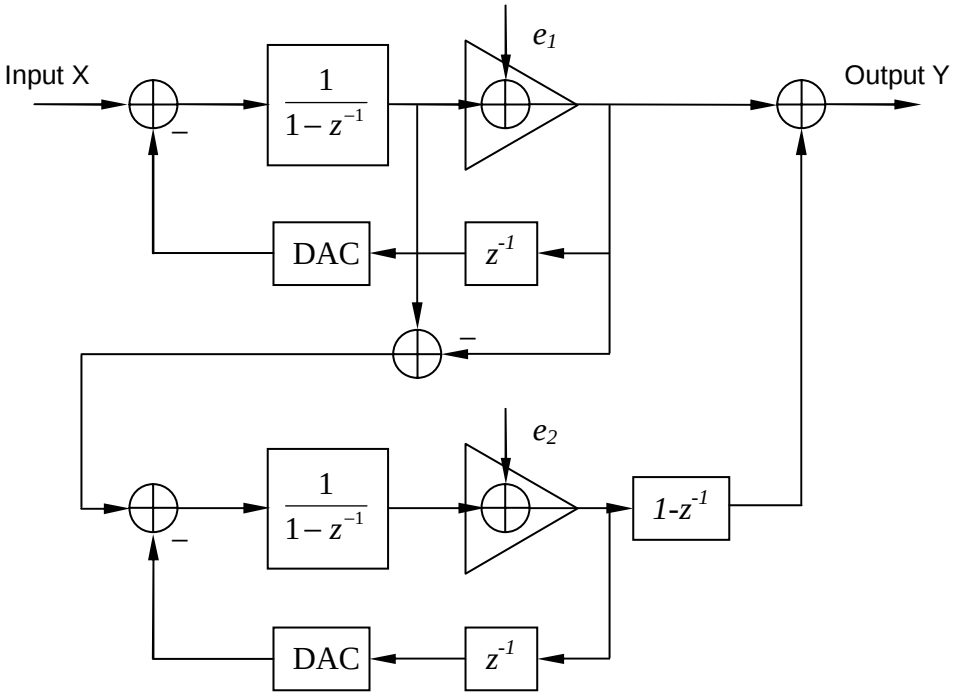


Figure 17. 2^{nd}-order lowpass MASH ΣΔ modulator.

2.3.3 Multi-bit Quantization

Most of the ΣΔ modulators use single-bit quantizer to take advantage of its good linearity. But the ΣΔ modulator with one-bit quantizer is prone to idle tones and stability problem. In some designs, multi-bit quantizer is used to increase the resolution and improve the stability, especially for the high-order modulators. The drawbacks of multi-bit quantizer are the complexity of circuit and SNR degradation due to the nonlinearity of the multi-bit DAC. To compensate the circuit imperfection, additional calibration circuits are often required in multi-bit quantizer modulators [Galt96].

2.4 Continuous-time Bandpass Sigma-Delta Modulator

2.4.1 Discrete-time and Continuous-time Sigma-Delta Modulators

Discrete-time ΣΔ modulators refer to the ΣΔ modulators which are implemented

with discrete-time switched-capacitor circuits [Sing95] [Baza98]. If the loop filter is realized with continuous-time circuit, such as LC or G_mC form, the modulator is called continuous-time ΣΔ modulator.

Discrete-time bandpass ΣΔ modulators have robust performance and can be easily analyzed in Z-domain [Schr89]. But their operating frequency is limited by the settling time of the circuit. This makes the discrete-time bandpass ΣΔ modulator unable to process high-frequency signals and also limits the maximum OSR that can be achieved. The sampling frequency of most reported discrete-time ΣΔ modulators are below 100MHz.

Continuous-time bandpass ΣΔ modulators are not constrained by the settling time problem and suitable for high-speed applications. The continuous-time modulators also have the advantage of inherent anti-aliasing [Shoa94], which alleviates the constraints on the anti-aliasing filter.

2.4.2 Design Methodology of Continuous-time Bandpass Sigma-Delta Modulator

Lowpass continuous-time ΣΔ modulators can be easily designed from the discrete lowpass modulators by simply replacing the discrete-time integrator with continuous-time one. But for bandpass continuous-time modulators, such a replacement of discrete-time resonator with continuous-time one does not yield a stable system [Nors97] [Cher00].

Due to the presence of a clocked sampler within the forward loop, one way to design the continuous-time bandpass ΣΔ modulator is to explore the equivalence

between discrete-time and continuous-time bandpass ΣΔ modulators [Shoa94]. A continuous-time and a discrete-time ΣΔ modulators are shown in Figure 18. If the two inputs to the quantizers are made the same at the sampling instants, then the same output bit streams *Y(n)* can be obtained from the modulators. This is illustrated in Figure 19.

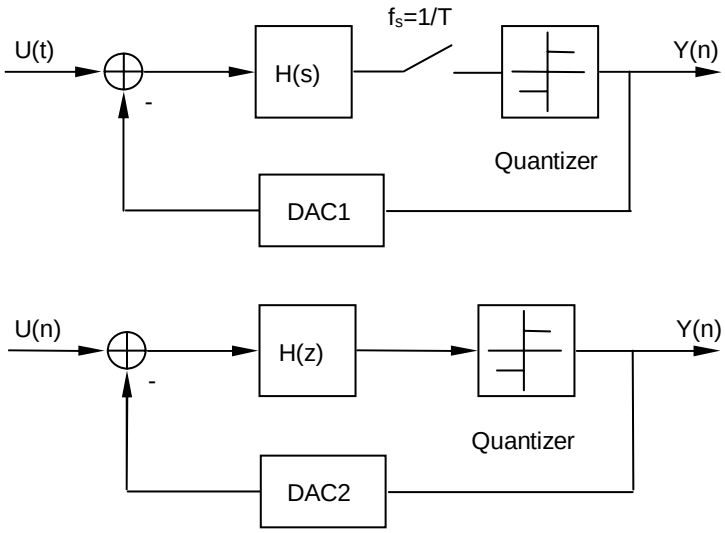


Figure 18. Equivalence between continuous and discrete-time modulators.

Since both modulators have the same input, the input can be ignored and the loop can be broken after the quantizers as shown in Figure 19.

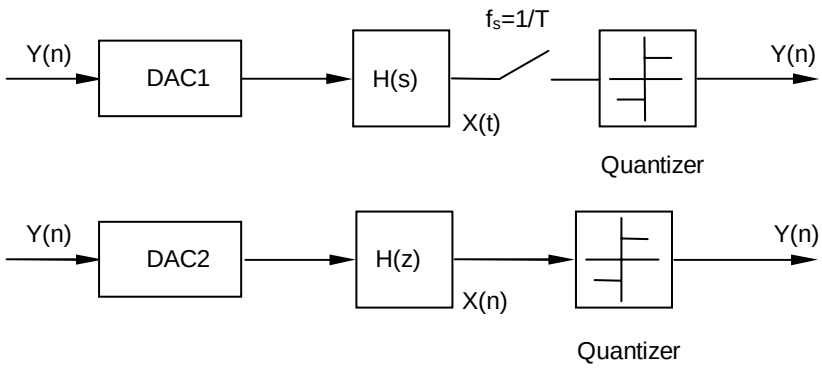


Figure 19. Forward loops of (a) continuous-time and (b) discrete-time ΣΔ modulators.

The equivalence can be expressed as:

$$X(t)|_{t=nT} = X(n) \tag{18}$$

or

$$H(z)D(z) = Z\{L^{-1}[H(s)D(s)]|_{t=nT}\}. \tag{19}$$

where, *D(s)* is the transfer function of DAC2, while *D(z)* is the transfer function of DAC1. Such a transformation between continuous-time and discrete-time is based on Pulse-Invariant Transform [Gard86] [Thur91].

The most commonly used continuous-time resonators are of LC and G_mC types. Since the transfer function of the resonators are generally fixed, other technologies, such as multiple feedback loops, have to be used to realize the equivalence. The detailed design methodology for continuous-time bandpass ΣΔ modulators will be discussed in Chapter 4.

2.4.3 Review of Continuous-time Bandpass Sigma-Delta Modulators

The idea of bandpass ΣΔ modulator was first proposed by R. Schreier and M. Snelgrove [Schr89]. The bandpass ΣΔ modulator was realized by putting the zeros of the noise transfer function at a certain frequency instead of DC. The modulator was implemented using switched-capacitor circuits.

Since then, many discrete-time bandpass ΣΔ modulators have been reported [Jant92] [Long93] [Sing95] [Hair96] [Ong97] [Cusi01]. With the increase of sampling frequency, the nonlinearities of the switched-capacitor circuits become obstacles in the high-speed bandpass ΣΔ modulator design. Continuous-time bandpass ΣΔ modulators,

which have the advantages of high operating frequency and inherent anti-aliasing, began to attract more attentions. But unlike discrete-time modulators, the continuous-time modulators lacked a systematic design methodology to predict the performance and stability. One effort to solve this problem was reported in [Thur91]. The pulse-invariant transform was introduced to explore the equivalence between the continuous and discrete-time modulators. But their method was still not an optimal solution since the equivalence was not fully realized due to limited controllability.

The problem was solved by Shoaei and Snelgrove [Shoa94]. In this paper, an idea that combines the multi-feedback technique together with the pulse-invariant transform was proposed. For the first time, a complete design methodology for continuous-time bandpass ΣΔ modulator design was presented. It was also pointed out in the paper that the low Q of resonators would affect the performance of the modulator. Low Q will lead to a SNR loss. A continuous-time bandpass ΣΔ modulator was designed and implemented with GmC resonator.

A LC resonator based continuous-time bandpass ΣΔ modulator was later reported in [Shoa95]. Due to the substrate loss, the on-chip LC resonator suffers from low Q factor. A Q-enhancement technique has to be used to improve the Q factor.

Many continuous-time bandpass ΣΔ modulators with different structures and technologies were reported later. The resonators used in the modulators were either LC or G_mC resonators. Table 1 lists the details of some reported continuous-time bandpass ΣΔ modulators.

Table 1. Continuous-time bandpass ΣΔ modulators published.

Reference	**[Shoa97]**	**[Gao98]**	**[Gao98a]**	**[Cher00a]**	**[Hsu00]**	**[Maur00]**
$F_{sampling}$	200	3,800	4,000	4,000	280	800
OSR	500	10,000	500	100	700	2,000
Order	2^{nd}	2^{nd}	4^{th}	4^{th}	2^{nd}	4^{th}
SNR_{max} (dB)	46	57	53	37	42	68
DR (dB)	50	N/A	62	40	N/A	60
Resonator	G_mC	LC	LC	LC	G_mC	G_mC
Process	0.8-μm BiCMOS	0.5-μm BJT	0.5-μm SiGe HBT	0.5-μm SiGe HBT	0.5-μm CMOS	SiGe BJT

It can be seen from the table that the resolution of the modulator is limited to 10 bits or lower. One of the major reasons that limit the resolution is the low Q of the LC and G_mC types of resonators. The low Q of LC resonator is mainly due to the losses from series resistance of the conductor and magnetically induced eddy current in the substrate. The Q degradation in the G_mC resonator, on the other hand, is because of its finite output impedance. Both are more severe at high frequencies.

2.4.4 Micromechanical Resonators

As it can be seen from the previous section, one of the limiting factors in high-speed continuous-time bandpass ΣΔ modulators is the low Q of the resonators. Both LC and G_mC resonators suffer from the poor Q factor. Although Q enhancement techniques are used in most of the designs [Shoa97] [Gao98] [Chee00a], they only have limited improvement. Besides, the Q-enhancement circuit degrades the linearity of the resonator.

Low Q will result in degradation of noise-shaping and SNR in ΣΔ modulators. Figure 20 illustrates the noise-shaping degradation due to low Q, while Figure 21

shows the SNR degradation. Similar analysis was done in [Shoa94] and [Gao98].

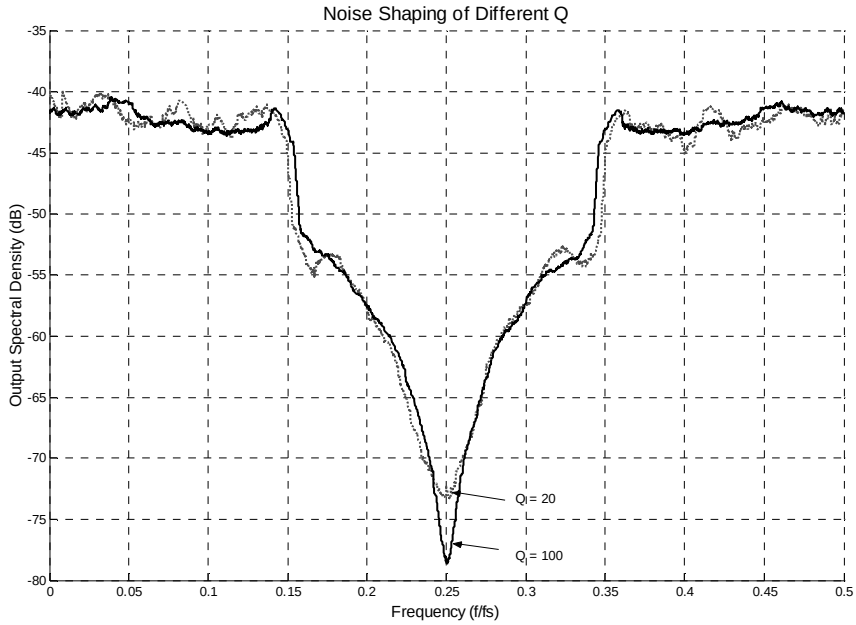


Figure 20. Noise shapes of the resonators of different Q.

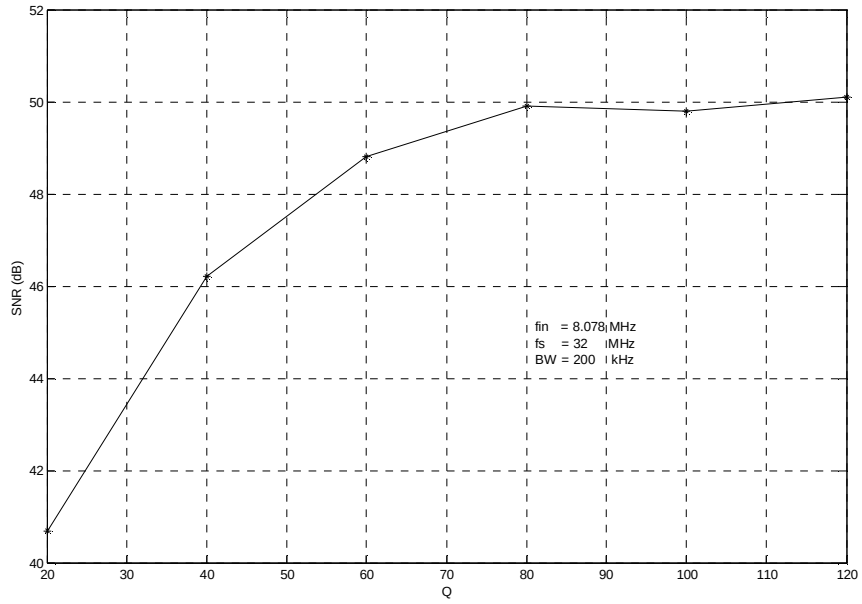


Figure 21. SNR degradation due to Q.

It can be seen that the SNR is highly dependant on the Q, especially when Q is less than 70. This can be easily understood as high-Q resonator gives a deeper notch at

the resonant frequency and have less quantization noise in the band of interest, as indicated in Figure 20.

Micromechanical resonators with resonant frequency as high as several hundreds of megahertz have been demonstrated [Bust98] [Nguy01]. Compared with LC and G_mC resonators, micromechanical resonators have the advantages of high Q (typically higher than 1000), good temperature stability, low power and high resonant frequency. The micromachining technology can be made compatible with CMOS process [Nguy01], which makes it possible to integrate with the circuits. The aim of the thesis is to investigate the feasibility of a micromechanical resonator based continuous-time bandpass $\Sigma\Delta$ modulator.

Chapter 3 Micromechanical Resonators

This Chapter introduces the various silicon micromechanical resonators. The MEMS (MicroElectroMechanical Systems) technology is briefly discussed. Comparison between the micromechanical resonator and other continuous-time resonators is presented. Finally, the clamped-clamped beam micromechanical resonator used in this project is introduced. The equivalent circuit is proposed to model the resonator and the resonator interface circuit is also presented.

3.1 MEMS Technology

MEMS is the acronym of MicroElectroMechanical Systems. They are micro-structures created on silicon or other materials.

The idea of MEMS was first proposed by the Nobel Prize-winning physicist R. R. Feynman in his famous talk “there is plenty of room at the bottom” given in Caltech in 1959. Since then, many researchers have developed various fabrication technologies and numerous MEMS devices and systems on silicon or other materials. Some commercial products, such as accelerometers, microphone, and pressure sensors, have been widely used in many applications [Gabr98].

The basic processes of MEMS, such as photolithography and chemical etching are borrowed from IC fabrication. But the IC fabrication is mostly based on surface processes, while the fabrication processes of MEMS are rather diverse.

The bulk micromachining technique [Gabr98] is a major technique in MEMS fabrication. It is based on etching (especially wet etching), and uses the anisotropic etchants to shape the structure.

Another important fabrication technique is surface micromachining [Bust98]. Like conventional IC fabrication, surface micromachining utilizes deposition, lithography and etching to realize microstructures. Surface micromachining can realize complex structures and is compatible with conventional IC processing. But it is inherently two-dimensional planar process and unable to realize structures with high aspect ratio.

LIGA [Bach95] is a new process proposed to realize the high-aspect-ratio structures. It is, in essence, a molding technique based on high-energy lithography source. But it has limited accessibility since it requires a synchrotron radiation source. Besides, it is not compatible with standard IC processing.

Many efforts have been made to integrate MEMS devices with integrated circuits so that the entire system can be realized on a single chip [Bust98] [Nguy01]. Although the integration is possible, it has not become the main stream technology due to the issues, such as cost and yield.

3.2 Structures of Micromechanical Resonators

Micromechanical resonator is a device, which generally utilizes the mechanical resonance driven by static electric force to work as a resonant component. The earliest version of the Micromechanical resonator as I know was the cantilever-beam resonator in [Nath67], shown in Figure 22. A bias voltage is applied to pull the beam close to the

substrate. The beam and the input force plate work as the two electrodes of a capacitor. The AC signal can be applied to the input force plate. When the frequency equals the inherent resonant frequency of the structure, the beam will have the largest movement. So, largest current output can be measured at the output port.

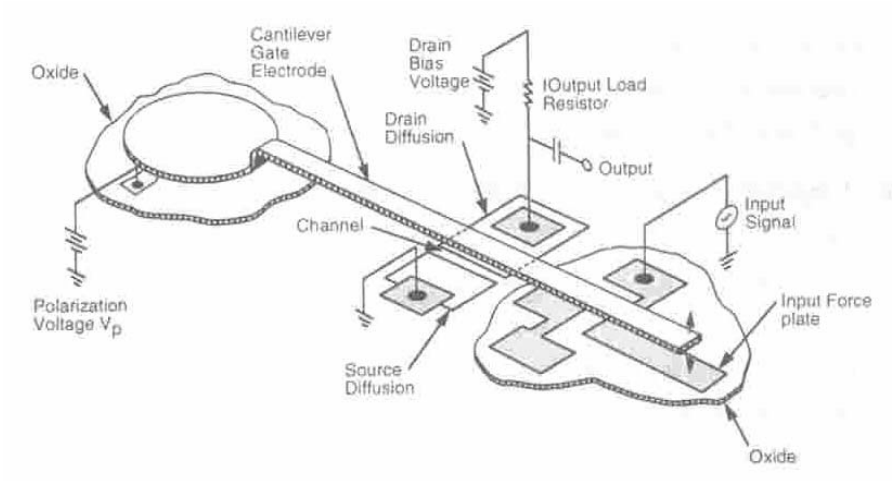


Figure 22. Cantilever-beam resonator.

Although the micromechanical resonator was reported decades ago, they didn't get much attention until recent years. Micromechanical resonators have the advantages of high Q and the potential to be integrated with circuits on single silicon, which makes them very attractive in the communication systems design. To date, many different structures of micromechanical resonators have been proposed, which are detailed as below.

Comb-transduced Resonator - Figure 23 [Nguy99] shows a comb-transduced resonator, together with its frequency response. Compared with cantilever-beam resonator, the vertical structure is replaced with two parallel inter-digit combs. The two combs act as the two electrodes of a capacitor. They move laterally when the electric force exists between them. The resonant frequency is determined by their mechanical

dimension, material, and bias voltage. Comb-transduced resonator has good linearity, but their working frequency is low (typically less than 1MHz) due to the bulky structure.

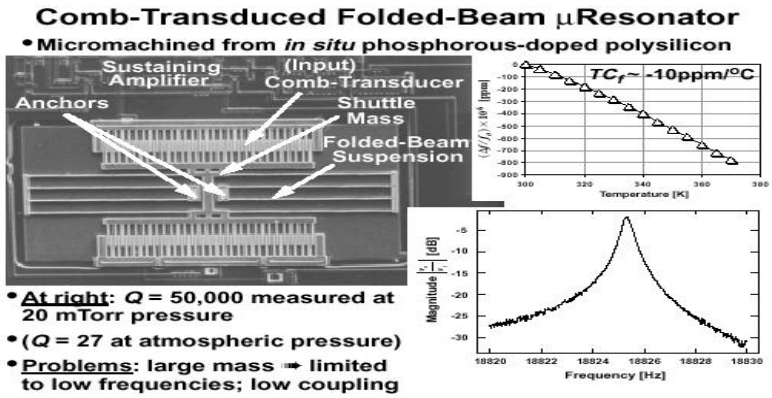


Figure 23. Comb-transduced resonator.

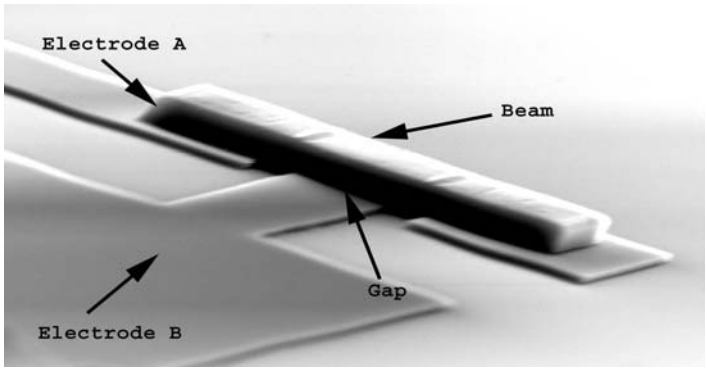


Figure 24. Clamped-clamped beam resonator.

Clamped-clamped Beam Resonator - The structure of the clamped-clamped beam micromechanical resonator is shown in Figure 24. Compared with cantilever-beam resonator, the beam has two stubs instead of one. The resonator consists of a polysilicon beam (connected to electrode A), and an electrode B, which lies under the beam. A bias voltage is applied to electrode A to pull the beam close to electrode B with electric force. The input signal is applied to electrode B to activate the resonator and the output signal is current. The output can be sensed with a resistive load or trans-impedance circuit. When the input signal frequency equals the resonant frequency, the signal will have the least loss in the transmission.

Free-free Beam Resonator - Free-free beam resonator is devised from the clamped-clamped beam resonator. It uses a membrane suspended with four beams as the resonant component. The beam length is designed at the one-fourth of the wavelength of the resonant frequency, so that the beam-introduced damping can be cancelled. With such a modification, free-free beam resonator can operate at higher resonant frequency than the clamped-clamped beam resonator. Figure 25 [Nguy99] shows a 92MHz free-free beam micromechanical resonator.

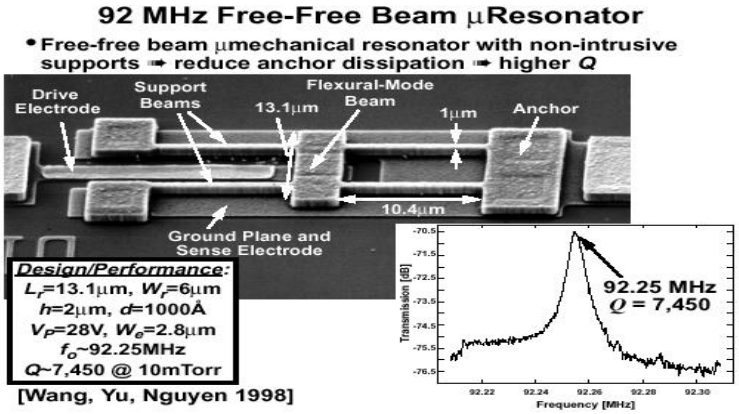


Figure 25. Free-free beam resonator.

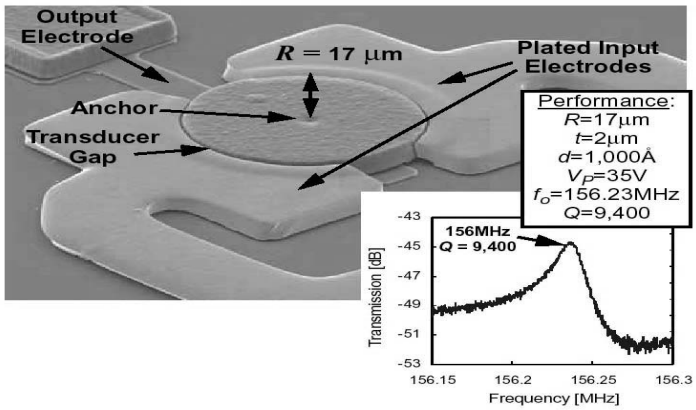


Figure 26. Disk resonator.

Disk Resonator – Disk resonator uses extensional, instead of flexural vibration mode to realize very high frequency resonance. Figure 26 [Nguy01] shows a radial contour-mode disk resonator. The resonator vibrates via uniform, well-balanced, radial expansion and contraction along its perimeter.

3.3 Resonator Model

A commonly used equivalent circuit for one-port micromechanical resonator is shown in Figure 27 [Sant99], where L_m, C_m and R_m are the motion elements and C_p is the static capacitor between the input and output of the micromechanical resonator.

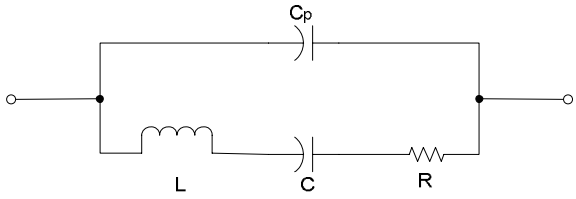


Figure 27. Equivalent circuit of the micromechanical resonator.

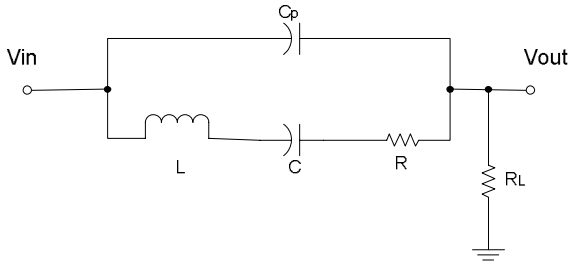


Figure 28. Equivalent circuit with resistive load.

The transfer function of the micromechanical resonator can be obtained based on the equivalent circuit in Figure 27. The transfer function with resistive load $R_{L,}$ as shown in Figure 28, is given by

$$M_R(s) = \frac{Vout}{Vin} = \frac{s(s^2 + as + b)}{s^3 + cs^2 + ds + e}, \tag{20}$$

where $a = R/L$, $b = (C+C_P)/(LCC_P)$,

$c = (R_LRC_P+L)/(R_LLC_P)$, $d = (R_LC_P+R_LC+RC)/(R_LLCC_P)$,

$e = 1/(R_LLCC_P)$.

The resonator used in our project is designed and fabricated by the Institute of Microelectronics (IME), Singapore. It is a one-port clamped-clamped beam resonator shown in Figure 24. The model parameters are given as below:

$R = 350K\Omega$, $C = 100aF$, $L = 3.6H$, $C_P = 200\,fF$.

Due to the bonding pads, there is a 5.5pF parasitic capacitor shunt at both the input and output.

Based on the parameters of this resonator and the equivalent circuit in Figure 27, the resultant frequency response with 50-Ω load and 50-Ω source impedance and 10 times amplification is shown in Figure 29, which closely matches the measured response shown in Figure 30 at a pressure of 20mTorrs. The loaded Q is measured to be around 200. When pressure is lower, the Q can be further improved. Considering the OSR of our design is expected to be 80, from Figure 21, it can been that a Q higher than 80 is adequate to ensure that the SNR loss due to non-ideal Q is negligible. So the Q of the micromechanical resonator is high enough.

The model is considered as accurate as far as the resonant frequency, anti-resonant frequency, insertion loss and Q are concerned.

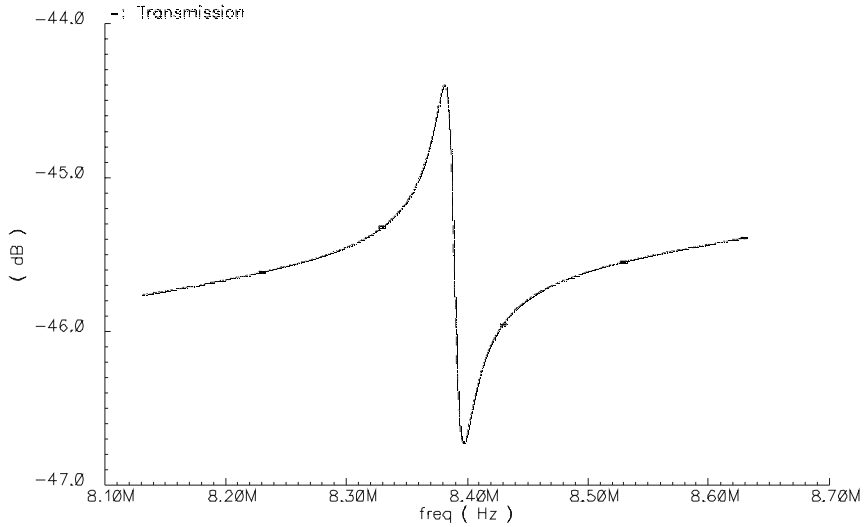


Figure 29. Simulated frequency response of the resonator (With 10 times amplification).

Figure 30. Measured frequency response of the micromechanical resonator (With 10 times of amplification).

Apart from the resonant peak, a notch also appears in the frequency response. The additional notch is referred as anti-resonance, which is caused by the existence of static capacitance C_P. Such a phenomenon is not a concern in the existing applications, as the resonators are mostly used as bandpass filters. However, it will be shown later that the anti-resonance is not desirable when the resonator is used to realize the ΣΔ modulator. The details will be discussed Chapter 4.

3.4 Sensing Circuits

When a voltage signal is applied at the input of the micromechanical resonator, a resistive load or trans-impedance circuit is generally used to sense the resonator output.

A sensing scheme based on resistive load is shown in Figure 31 [Wang00], where L_P is used to block the AC signal, while C_f blocks the DC. Generally, L_P=*1mH*, C=*0.1*μF are used.

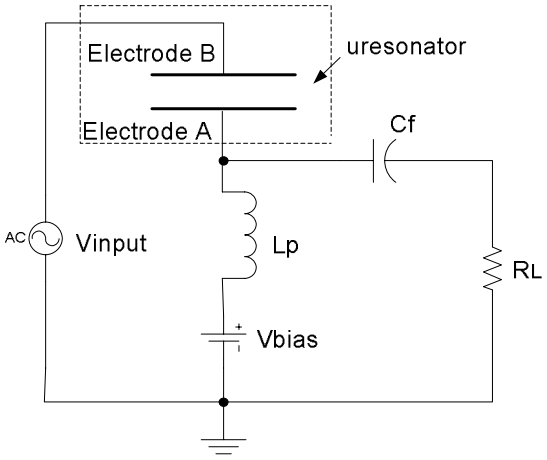


Figure 31. Resistive sensing circuit.

Another sensing scheme is based on trans-impedance circuit as shown in Figure 32 [Bili01].

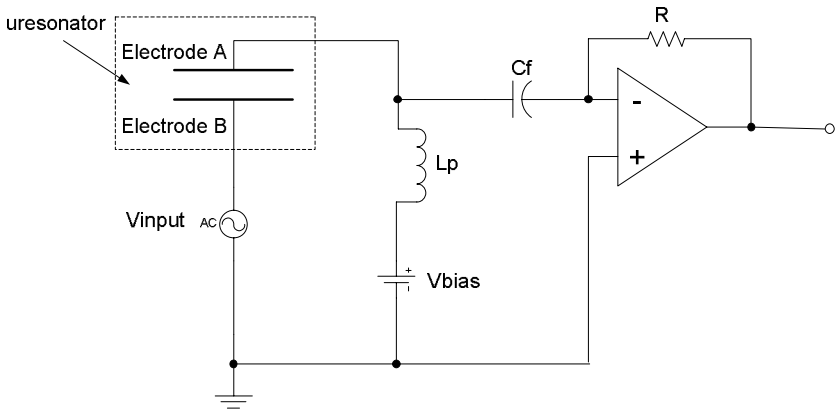


Figure 32. Trans-impedance sensing circuit.

Both circuits have the same function, that is, to convert the current output from the resonator to a voltage. Note that a coupling capacitor is needed to isolate the DC bias voltage.

3.5 Micromechanical Resonator versus LC and G_mC Resonators

Compared with LC and G_mC resonators, micromechanical resonators have the advantages of high Q, high resonant frequency, and good temperature stability. Their disadvantages lie in the insertion loss (inherent for passive elements), and the existence of anti-resonance.

All the continuous-time bandpass ΣΔ modulators published so far used LC or G_mC resonators. They suffered from low quality factor Q and poor linearity, which degraded the performance of the ΣΔ modulators. This is especially true at high frequencies. Q-enhancement circuits were generally needed [Shoa97] [Gao98] [Cher00a]. Micromechanical resonators have high Q and relatively high resonant frequency and the micromachining processing can be made compatible with IC processing [Bust98] [Nguy01]. Therefore, micromechanical resonator is a good candidate to replace LC and G_mC resonators in continuous-time bandpass ΣΔ modulators.

Chapter 4 Bandpass Sigma-Delta Modulator Based on Micromechanical Resonator

In Chapter 2, it was pointed out that the poor Q factor was one of the obstacles in realizing high-speed bandpass ΣΔ modulators. High Q micromechanical resonator is proposed to replace the LC and G_mC resonators in an attempt to overcome this problem. This chapter deals with the design of the micromechanical resonator based continuous-time bandpass ΣΔ modulator. The design methodology is first introduced. The effect of anti-resonance is then discussed and an anti-resonance cancellation circuit is proposed. Finally, the modulator architecture and its simulation results are presented. The circuit-level implementation is also recommended.

4.1 Design Methodology

The design methodology for continuous-time bandpass ΣΔ modulators was proposed by Shoaei and Snelgrove in 1994 [Shoa94]. It is based on the equivalence between the discrete-time and continuous-time ΣΔ modulators. Such equivalence can be achieved by pulse-invariant transform and multi-feedback technique.

For the continuous-time and discrete-time ΣΔ modulators shown in Figure 33, if the two quantizers produce the same output *Y(n)*, the quantizers inputs at the sampling instants must be the same. This is illustrated in Figure 34 and can be described mathematically by the following equation:

$$X(t)|_{t=nT} = X(n) \quad (21)$$

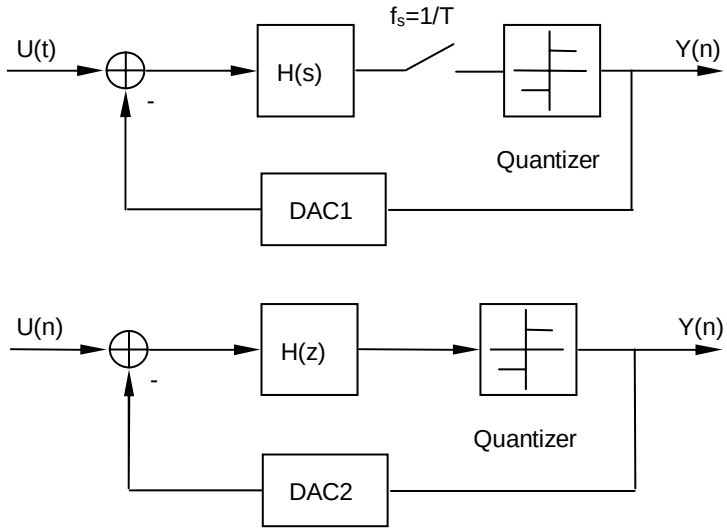


Figure 33. Equivalence between discrete-time and continuous-time modulators.

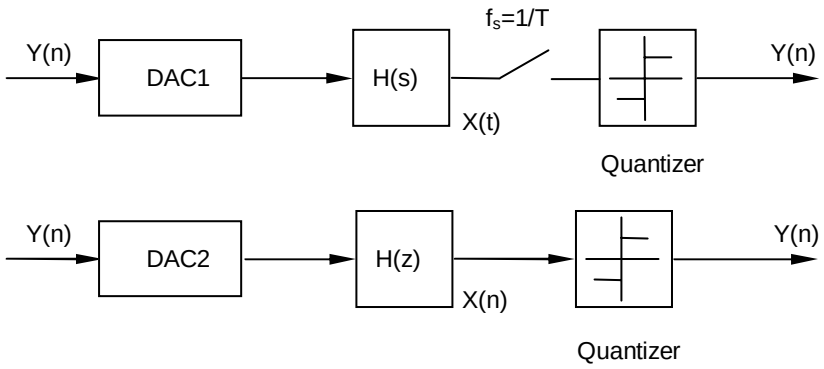


Figure 34. Broken loops of (a) continuous-time and (b) discrete-time ΣΔ modulators.

Thus, the loop transfer function of the continuous-time modulator should satisfy

$$H(z)D(z) = Z\{L^{-1}[H(s)D(s)]\big|_{t=nT}\}. \qquad (22)$$

where, *D(s)* is the transfer function of DAC2 and *D(z)* is transfer function of DAC1. Depending on the transfer function of the resonator, the above equation may not have a solution. In such a case, more degrees of freedom are needed. Thus, multi-feedback technique is used by adding an additional feedback loop, as shown in Figure 35.

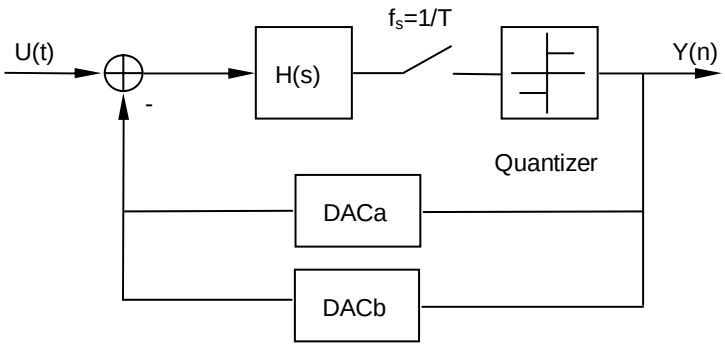


Figure 35. Continuous-time modulator with two feedbacks.

The DACs used in continuous-time modulator can be categorized into two types: non-return-to-zero DAC and return-to-zero DAC. Assume V_P, V_N are the positive and negative outputs of the DAC, respectively. Non-return-to-zero DAC outputs either V_P or V_N in each clock cycle. But for return-to-zero DACs, there is a period in a clock cycle, in which the DAC output will be zero. According to location of the return-to-zero period, return-to-zero DACs can be divided into return-to-zero, half-return-to-zero, and other types.

The waveforms of non-return-to-zero, return-to-zero, and half-return-to-zero DACs are shown in Figure 36.

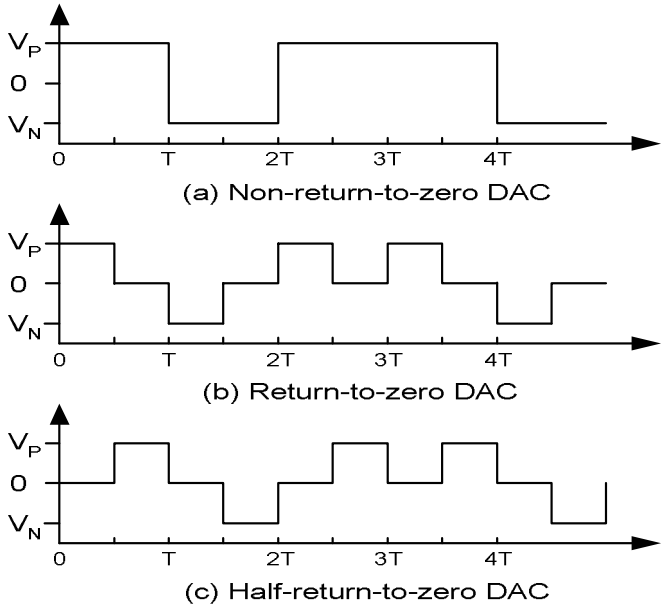


Figure 36. DAC waveforms.

The S domain transfer functions of the DACs are as below:

$$\text{Non-return-to-zero DAC:} \qquad DAC_N(s) = \frac{1-e^{-sT}}{s} \tag{23}$$

$$\text{Return-to-zero DAC:} \qquad DAC_R(s) = \frac{1-e^{-sT/2}}{s} \tag{24}$$

$$\text{Half-return-to-zero DAC:} \qquad DAC_H(s) = \frac{e^{-sT/2}-e^{-sT}}{s} \tag{25}$$

In multi-feedback technique, the linear combination of the DACs' transfer functions makes it possible to satisfy Eq. (22) and to realize the equivalence between the discrete-time and continuous-time ΣΔ modulators.

4.2 Anti-resonance and Its Cancellation

The idea to use micromechanical resonator in ΣΔ modulation is to take advantage of its high Q. However, the micromechanical resonator has the drawbacks of anti-resonance and insertion loss. While the insertion loss can be compensated with amplification, the effect of anti-resonance has to be analyzed.

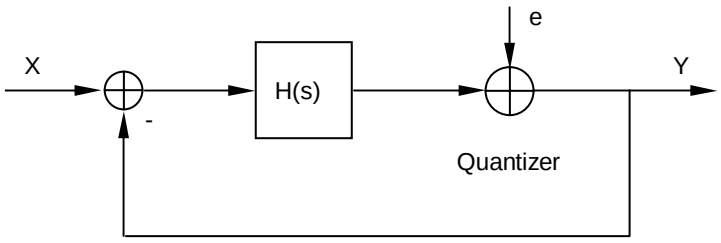


Figure 37. Linear model of ΣΔ modulator.

Consider the linear model of ΣΔ modulator shown in Figure 37, the signal and noise transfer functions are given below:

$$\textit{Signal}\ \text{Transfer Function:} \qquad STF = \frac{H(s)}{1+H(s)} \tag{26}$$

Noise Transfer Function: $$NTF = \frac{1}{1+H(s)}. \quad (27)$$

At the anti-resonant frequency, $|H(s)| << 1$, thus the signal is attenuated and the noise shaping cannot be attained. Matlab simulation also shows that the continuous-to-discrete equivalence cannot be achieved if the anti-resonance exists. Therefore, in order to realize the bandpass ΣΔ modulator, the anti-resonance must be removed. The proposed cancellation scheme is shown in Figure 38.

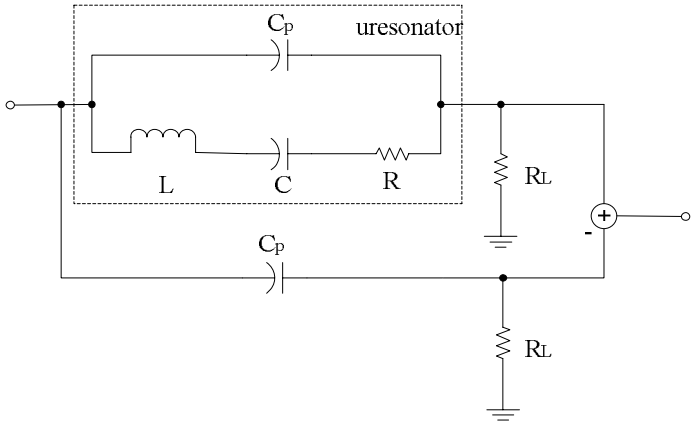


Figure 38. Anti-resonance cancellation scheme.

The existence of anti-resonance is due to the feed-through static capacitance C_P. In this scheme, the effect of C_P is generated in an additional branch and subsequently subtracted from the resonator output. The resultant transfer function normalized to the sampling frequency can be approximated to

$$H(s) = g\frac{s}{s^2 + (\pi/2)^2}. \quad (28)$$

The simulated frequency response of the micromechanical resonator with anti-resonance cancellation is shown in Figure 39, while the measured result is shown in Figure 40. When the two paths are not matched, the cancellation may be incomplete, as shown in Figure 41.

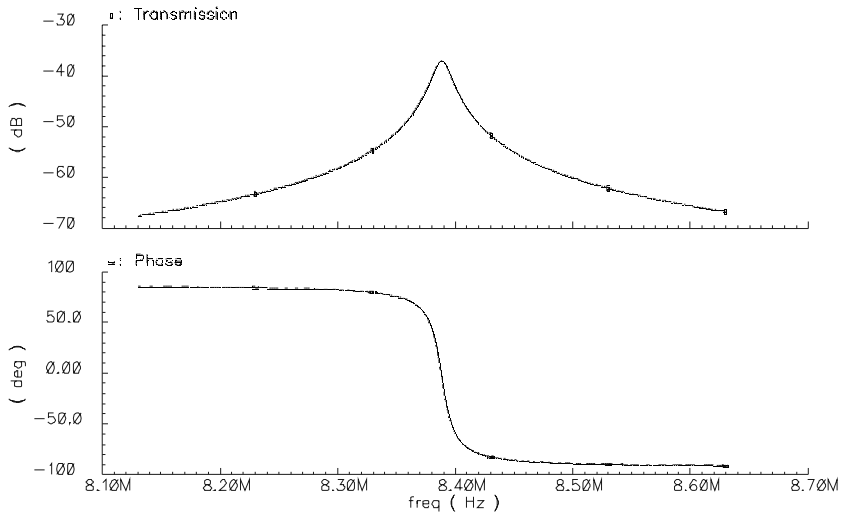


Figure 39 Frequency response of the resonator with anti-resonance cancellation.

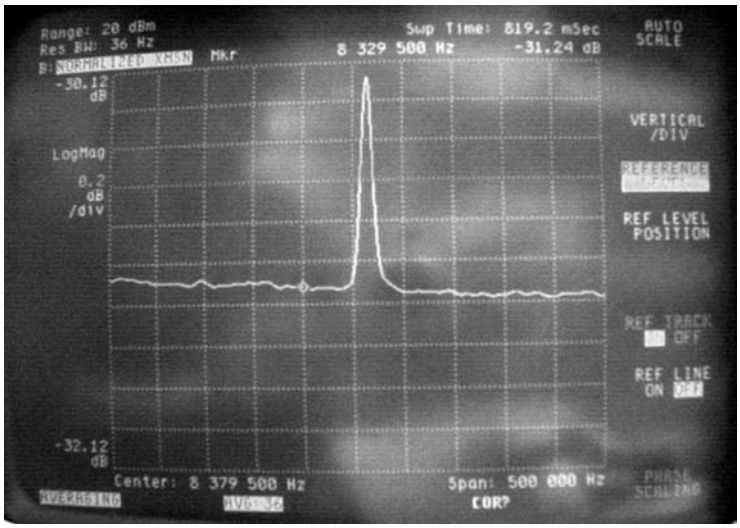


Figure 40. Frequency response of the micromechanical resonator with anti-resonance cancellation.

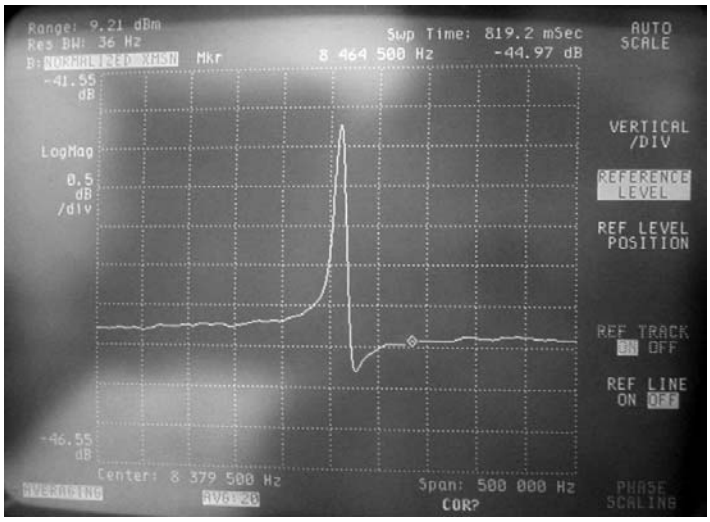


Figure 41. Frequency response of the micromechanical resonator with imperfect anti-resonance cancellation.

4.3 Modulator Architecture

The prototype discrete-time bandpass modulator is shown in Figure 13. With the design methodology discussed in Section 4.1, if only one non-return-to-zero DAC feedback is used, the loop transfer function after pulse-invariant transform will be

$$H(z) = Z\{L^{-1}[H(s)D(s)]|_{t=nT}\} \tag{29}$$

where H(s) is the resonator transfer function, and D(s) is the transfer function of the non-return-to-zero DAC.

With the anti-resonance cancellation, the transfer function of the micromechanical resonator can be written as

$$H(s) = \frac{s}{s^2 + (\pi/2)^2} \tag{30}$$

which is normalized to the sampling frequency f_s.

So Eq.(29) can be calculated to be

$$H(z) = Z\{L^{-1}[H(s)D(s)]|_{t=nT}\} = \frac{0.6366z - 0.6366}{z^2 + 1} \tag{31}$$

The calculation is done with the Matlab program in Appendix A1. The result doesn't equal to the loop transfer function of the second-order discrete-time bandpass ΣΔ modulator $\frac{-1}{z^2+1}$. The reason is that there is no enough controllability to make the continuous-time to discrete-time equivalence [Cher00]. Comparing the numerators of the two equations, it can be seen that two feedback loops are needed to realize the equivalence. They can be any combination of the three DACs proposed in Section 4.1. The two return-to-zero DACs are used in the design because they are immune to the asymmetric pulse waveform [Cherr00].

The proposed architecture for the micromechanical resonator based bandpass ΣΔ modulator is shown in Figure 42.

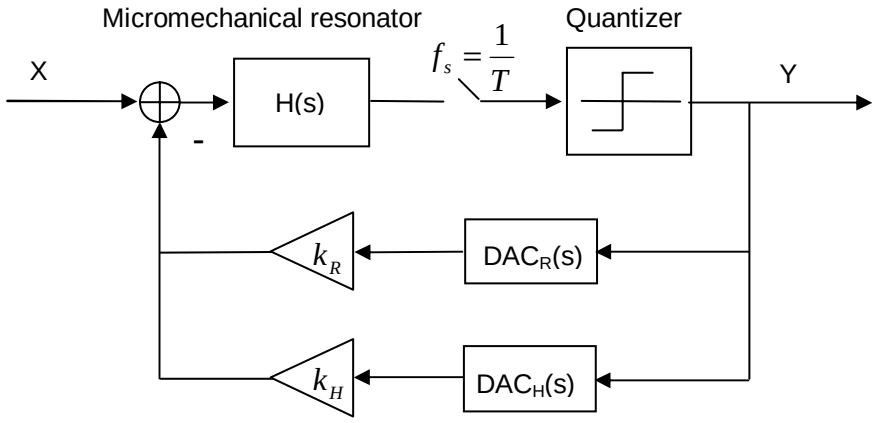


Figure 42. Proposed micromechanical resonator based bandpass ΣΔ modulator.

By applying pulse-invariant transform, an equivalent Z-domain transfer function can be obtained from that of the continuous-time bandpass ΣΔ modulator:

$$\begin{aligned} H(z) &= Z\{L^{-1}[k_R H(s) DAC_R(s) + k_H H(s) DAC_H(s)]\} \\ &= k_R \frac{0.1865z - 0.4502}{z^2 + 1} + k_H \frac{0.4502z - 0.1865}{z^2 + 1} \end{aligned} \tag{32}$$

The two coefficients k_R and k_H can be determined by equating Eq.(32) to the desired Z-domain transfer function of second-order sigma-delta modulator, that is,

$$H(z) = k_R \frac{0.1865z - 0.4502}{z^2 + 1} + k_H \frac{0.4502z - 0.1865}{z^2 + 1} = \frac{-1}{z^2 + 1}. \tag{33}$$

The coefficients obtained from Eq. (33) are

$$k_R = 2.6815, \qquad k_H = -1.1107.$$

4.4 Performance of the Proposed Sigma-Delta Modulator

The Simulink model shown in Figure 43 is used to evaluate the performance of the proposed ΣΔ modulator. Figure 44 shows the power spectrum of the output bit stream

when the input signal is at 8.07 MHz with a magnitude of -4.4dB, the sampling frequency is 32 MHz. Figure 45 is the in-band spectrum within the 200-KHz bandwidth. 8192 samples are used in the FFT calculation.

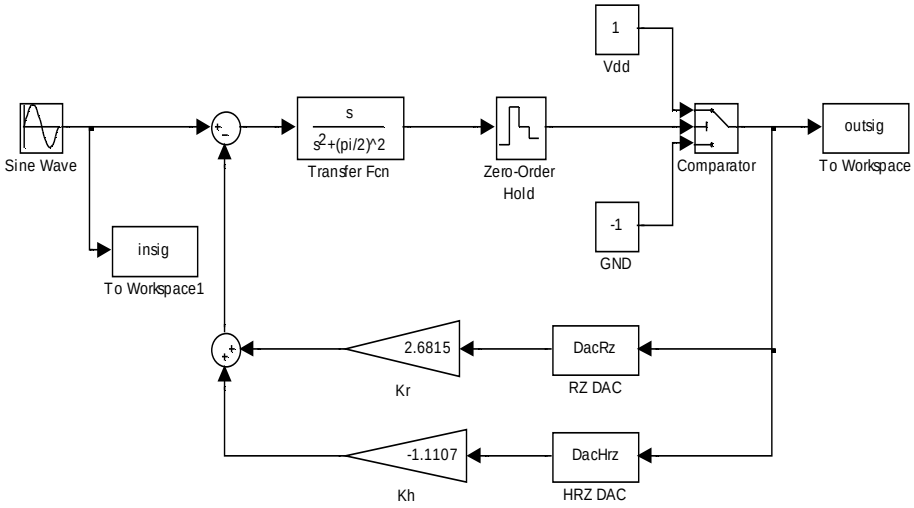


Figure 43. Simulink model of the continuous-time modulator.

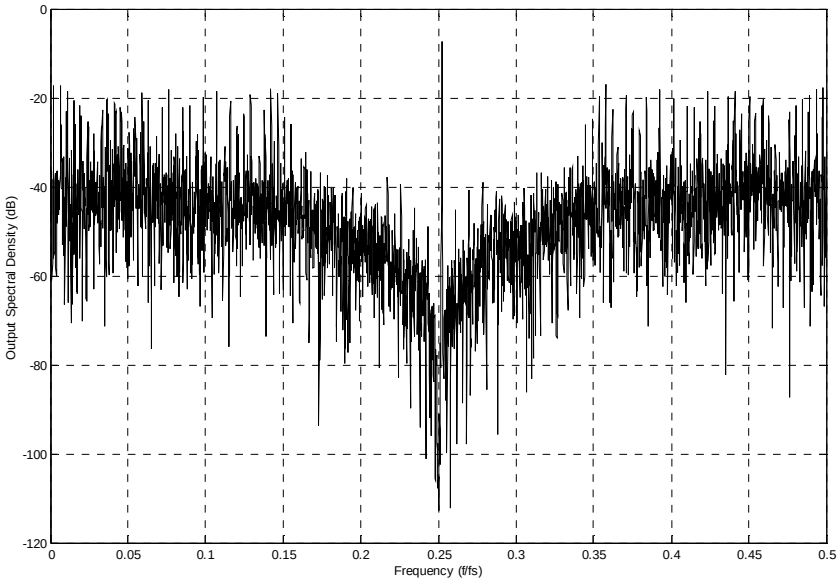


Figure 44. Output power spectrum (Matlab simulation).

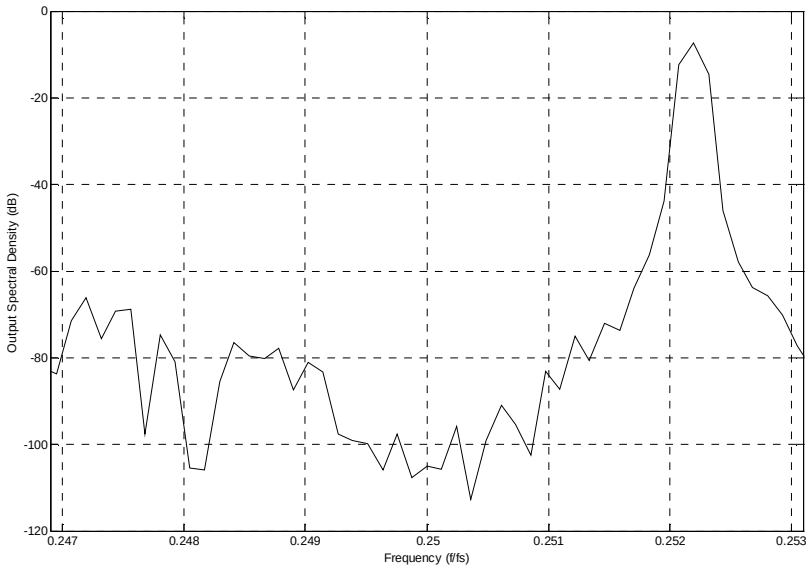


Figure 45. In-band power spectrum (OSR = 80, Matlab simulation).

Figure 46 shows the SNR again input magnitude for the bandwidth of 200 KHz and sampling frequency of 32 MHz. The calculated dynamic range is 48dB and peak SNR is 45dB.

The simulation result shows a similar noise shaping as obtained in the discrete-time 2^{nd}-order bandpass Sigma-delta modulator, which proves that the design methodology is correct. The SNR degradation when input approaches full scale is due to the increased spectral harmonic content. Here the full scale input is defined to be the one whose magnitude equals the maximum magnitude of the quantizer feedback [Cher00].

The dynamic range is determined by the noise floor, which is also the ideal peak SNR. Due to the SNR degradation at full scale, the peak SNR is slightly lower than the dynamic range.

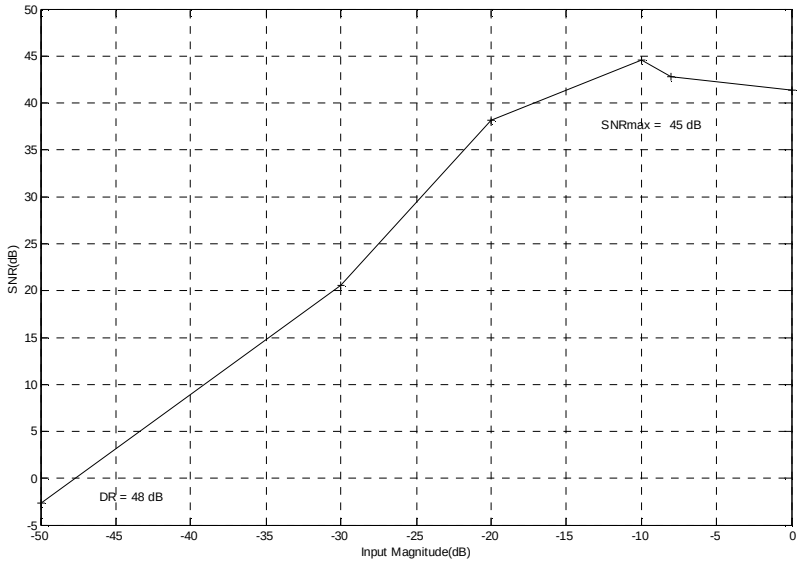


Figure 46. SNR against Input magnitude (Matlab simulation).

4.5 Circuit Implementation

The circuit implementation of the proposed modulator is depicted in Figure 47, where the micromechanical resonator and its anti-resonance cancellation circuit is off-chip.

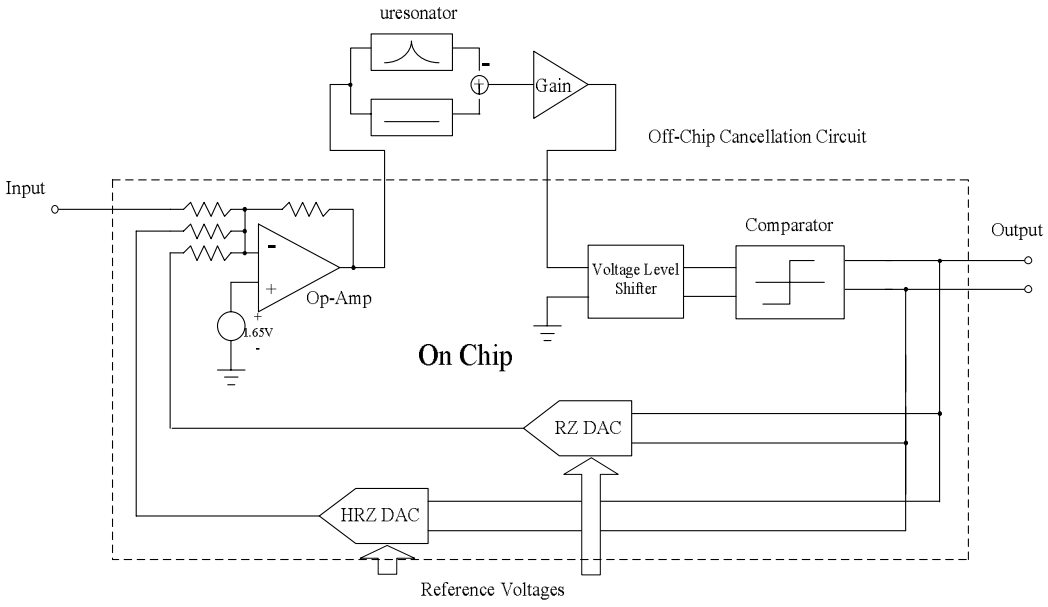


Figure 47. Circuit structure of the modulator.

The operational amplifier is used to realize the signal addition. The output from

the opamp is fed to the micromechanical resonator and the cancellation circuit. The gain stage is used to compensate the insertion loss of the micromechanical resonator.

Chapter 5 Circuit Level Design

This chapter describes the circuit-level design of the proposed modulator and presents the simulation results. The design is based on a triple-metal, double-poly 0.6-μm CMOS process from AMS (Austria MikroSystems). The design specifications are summarized in Table 2.

Table 2. Design specifications.

Process	0.6-μm CMOS
Supply Voltage	3.3V Single Supply
Sampling Frequency	32MHz
Signal Frequency	8MHz
Bandwidth	200kHz
OSR	80
Dynamic Range	48dB

5.1 Function Blocks

Figure 48 shows the circuit-level block diagram of the proposed modulator. The micromechanical resonator part is realized off-chip. The on-chip circuits include the operational amplifier, voltage shifter, comparator, and DACs. The operational amplifier is used to realize the sum amplifier. The voltage shifter shifts the signal with a proper DC level required by the comparator. The voltage shifter, comparator and DAC are designed in differential form to reduce noise and interference. The operational amplifier is single-ended, since the micromechanical resonator cannot handle the differential signal.

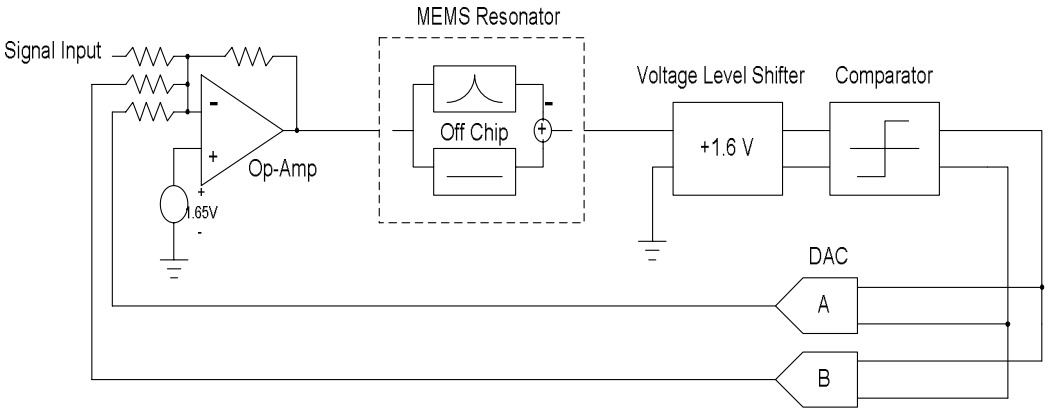


Figure 48. Modulator circuit structure.

5.2 Operational Amplifier

Since the opamp is used to realize a sum amplifier, considering the signal from DACs has a frequency of 32MHz, high bandwidth and a modest DC gain is needed. A folded cascode structure is chosen for the opamp. The circuit of the opamp is shown in Figure 49.

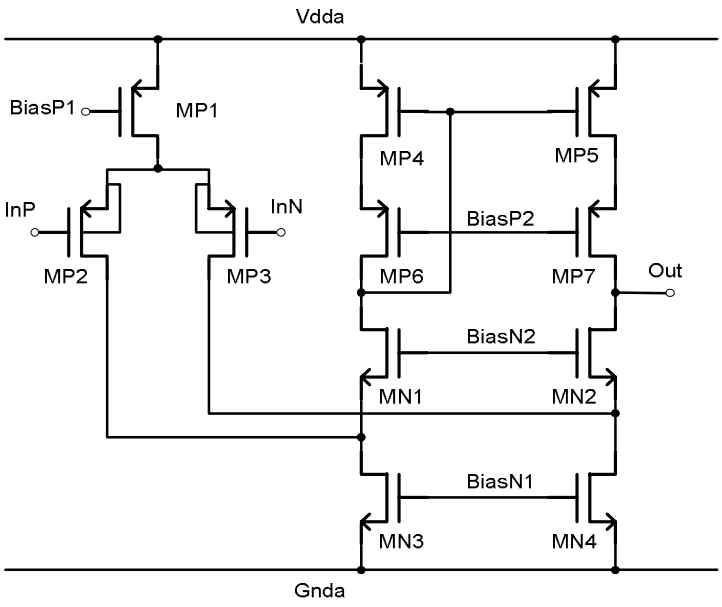


Figure 49. OTA schematic.

Both the input and output DC levels are set to 1.65V. MP4 to MP7 are the active load with differential-to-single ended conversion, so the long channel length is used to

alleviate the channel length modulation effect. MP2 and MP3 are designed in minimum length to achieve high g_m with a reasonable transistor width. The size of MN1, MN2 and MP6 and MP7 are determined based on the trade-off between gain and frequency response through simulation. The bias current of the input stage is 1.5mA and the currents of MP4 and MP5 are both designed as 0.75mA. The sizes of the transistors are listed in Table 3.

Table 3. OTA transistor sizes.

Transistor	W/L (micron)	Transistor	W/L (micron)
MP1	1107.6/4.8	MN1/2	134.6/0.9
MP2/3	684.95/0.6	MN3/4	335.25/2.1
MP4/5	383.4/4.8		
MP6/7	292/0.9		

Biasing circuit for the opamp is shown in Figure 50. The input reference current I_{Bias} is set to be 0.2mA and is generated off-chip. Large transistor length is used to reduce the channel length modulation effect. The transistor sizes are listed in Table 4 and the bias voltages in Table 5.

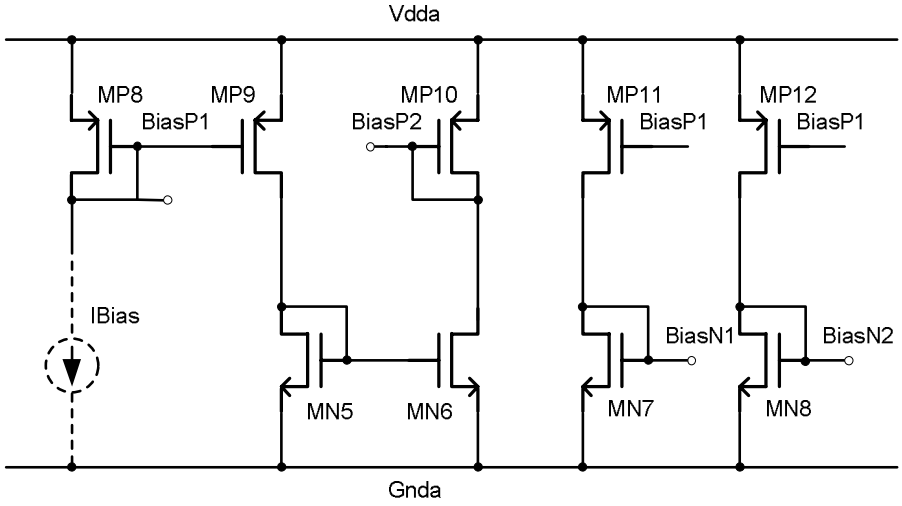


Figure 50. Basing circuit schematic.

Table 4. Transistor sizes of the biasing circuit.

Transistor	W/L (micron)	Transistor	W/L (micron)
MP8	147.75/4.8	MN5	160.5/4.8
MP9	73.65/4.8	MN6	161.4/4.8
MP10	19.55/4.8	MN7	54.3/4.8
MP11	73.3/4.8	MN8	16.4/4.8
MP12	75.5/4.8		

Table 5. Bias voltages.

Net Name	BiasP1	BiasP2	BiasN1	BiasN2
Voltage (V)	1.8	1.1	1.3	1.7

The simulation result is shown in Figure 51. The unity gain frequency is approximately 229MHz for a capacitive load of 2pF. The phase margin is 63˚. The power consumption of the OTA and basing circuit is measured to be 12mW.

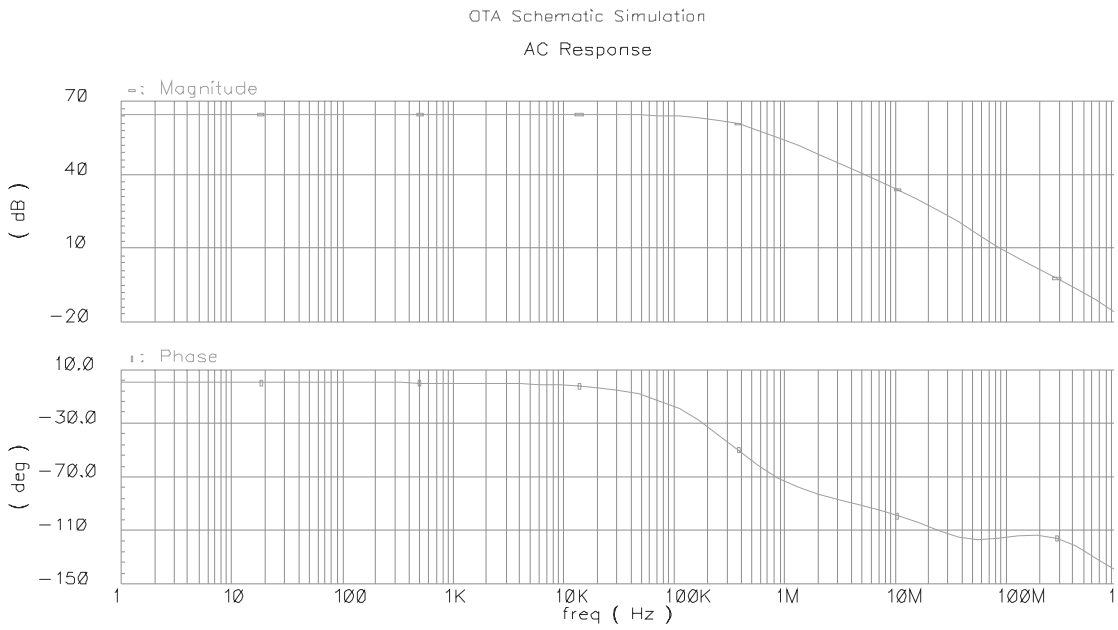


Figure 51. Frequency response of the OTA.

5.3 Comparator

The schematic of the high-speed latched comparator [John97] is shown in Figure 52. The comparator circuit can be divided into track-and-latch stage and the buffer. The latch-and-track stage is implemented with two back-to-back connected inverters and a buffer. The positive feedback regenerates the analog input into a full-scale digital output.

Latch and LatchN are two differential clocks. The comparator operates in two phases: the compare and reset phases. When Latch is high, MP5 and MP6 are off. The comparator does comparison, and the output appears at OutP and OutN. When Latch is low and LatchN is high, MP5 and MP6 are on, which resets the outputs of the track-and-latch stage. In the meantime, the two transmission gates are off, so that the previous result is stored at the buffer stage until next clock cycle. The reset phase is used to ensure that no memory is transferred from one decision cycle to the next. The transistor sizes are given in Table 6.

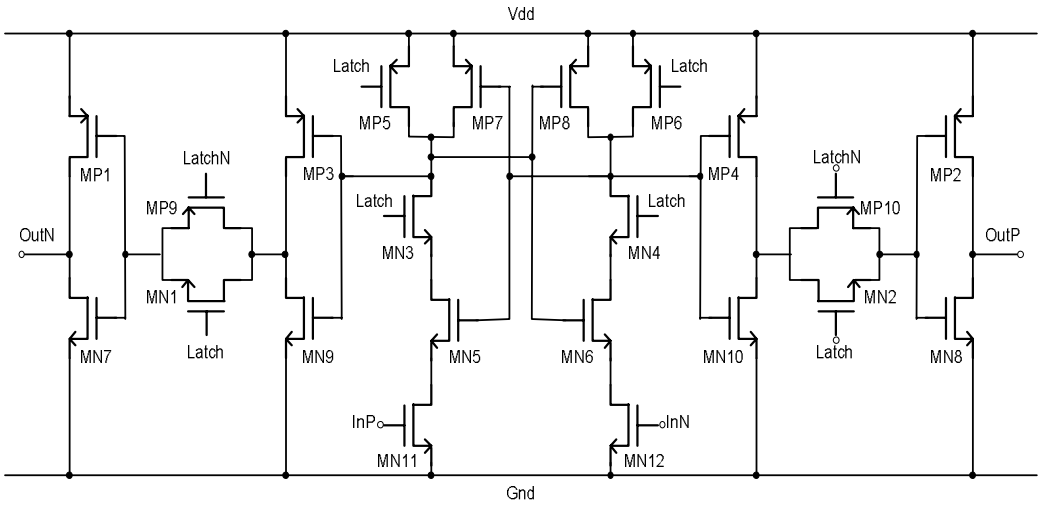


Figure 52. Schematic of the differential comparator.

Table 6. Transistor sizes of the differential comparator.

Transistor	W/L (micron)	Transistor	W/L (micron)
MP1/2	45/0.6	MN1/2	2/0.6
MP3/4	6/0.6	MN3/4	40/0.6
MP5/6	28/0.6	MN5/6	60/0.6
MP7/8	60/0.6	MN7/8	15/0.6
MP9/10	6/0.6	MN9/10	2/0.6
		MN11/12	120/1.2

The comparator is simulated with 1pF load. The input to InP is a sinusoidal signal with an amplitude of 300mV and a offset of 1.6V at the frequency of 12MHz. The input to InN is 1.6V DC voltage. The clock is set to be 40MHz. The transient response is shown in Figure 53. The rise time is 1.7ns (10% accuracy), while the fall settling time is 2.0ns, which indicates a maximum sampling frequency of approximately 270MHz.

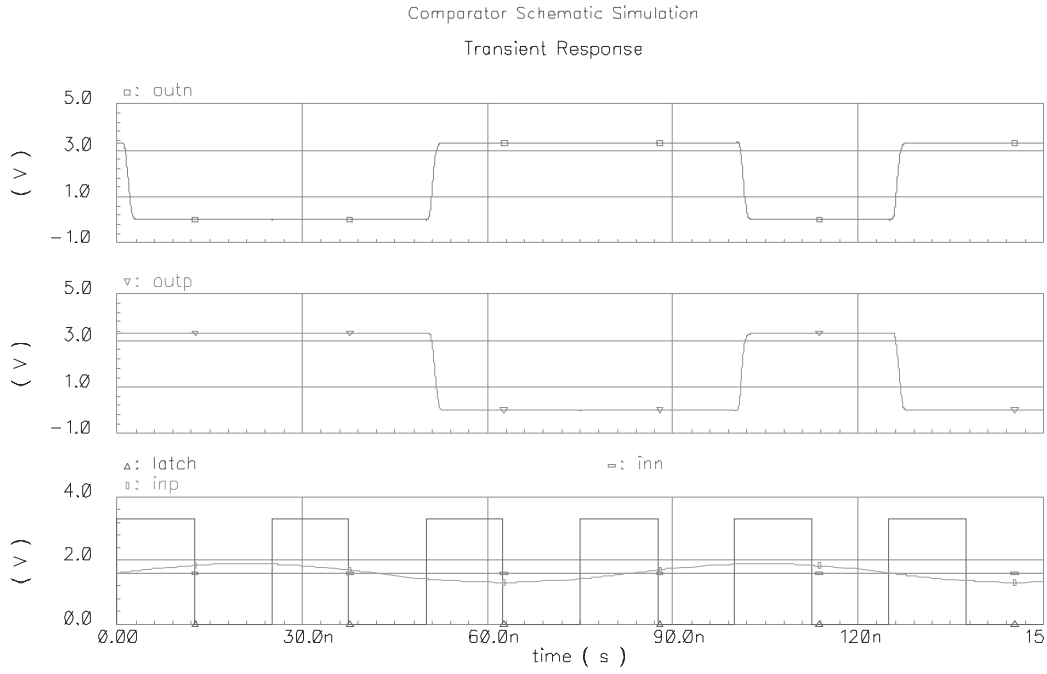


Figure 53. Transient response of the differential comparator.

5.4 One-bit DACs

The Schematic of the 1-bit DAC is shown in Figure 54. It is composed of eight CMOS transmission gates. The output voltages can be set through the reference voltages: V_{refp}, V_{refn} and V_{avr}. The output waveform is controlled by CLK signal together with the InP and InN signals. With different CLK signal, both return-to-zero and non-return-to-zero DACs can be implemented. The transistor sizes used are summarized in Table 7.

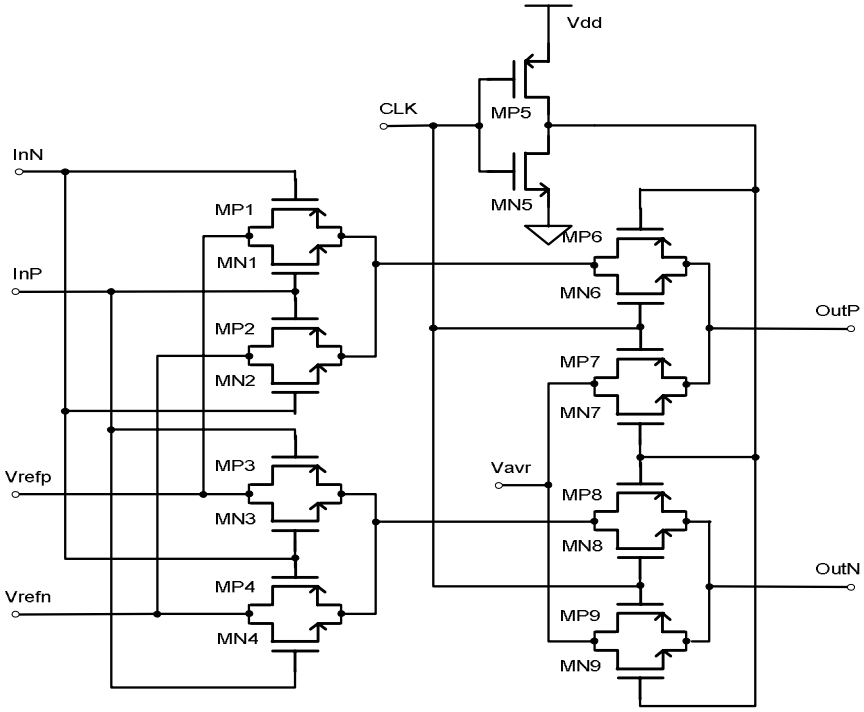


Figure 54. Schematic of the DAC.

Table 7. Transistor sizes of the DAC.

Transistor	W/L (micron)	Transistor	W/L (micron)
MP1/2/3/4	30/0.6	MN1/2/3/4	10.05/0.6
MP5	3/0.6	MN5	1/0.6
MP6/7/8/9	12/0.6	MN6/7/8/9	4/0.6

The waveforms of return-to-zero DAC, together with clock signal and DAC input

are depicted in Figure 55. The CLK signal is for return-to-zero DAC. Half-return-to-zero DAC can be implemented by simply inverting the clock signal. With 0.2pF load (OTA input capacitance), the rise time is 1.1ns, and the fall settling time is 0.6ns, which satisfies our requirements.

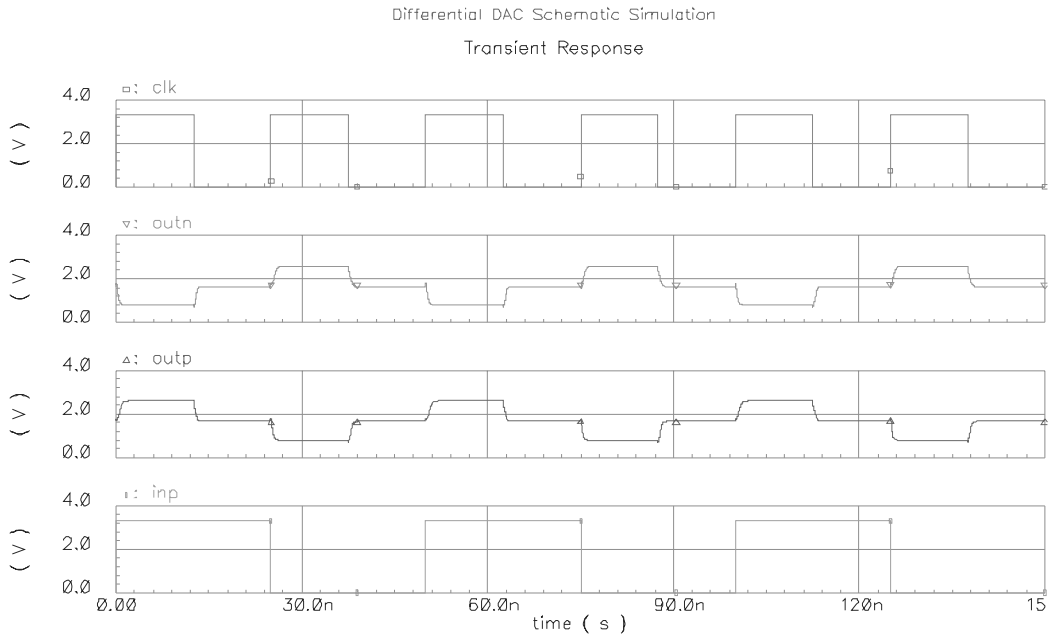


Figure 55. Transient simulation results of the return-to-zero DAC.

5.5 Voltage Level Shifter

The output of the resonator cancellation and amplification circuit is a single-ended AC signal. Since the comparator cannot handle negative signal, a voltage level shifter (VLS) is needed to introduce a positive 1.6V shift. The differential VLS is implemented with two PMOS source followers as shown in Figure 56. MP3 and MP4 work as source follower; MP1 and MP2 are the active loads. BiasN2 is provided by the OTA biasing circuit. The currents of both paths are designed to be 0.2mA. The sizes of the transistors are given in Table 8.

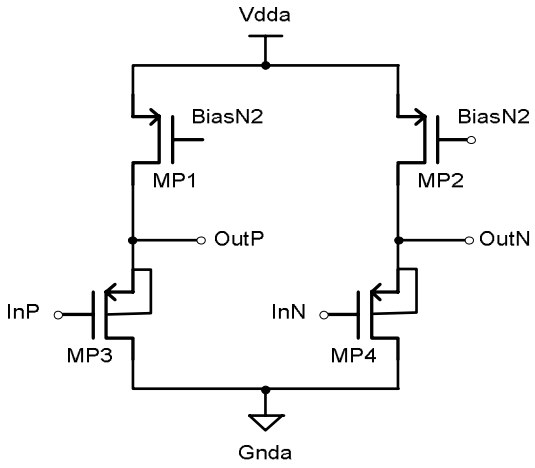


Figure 56. Schematic of the differential voltage level shifter.

Table 8. VLS transistor sizes.

Transistor	W/L (micron)
MP1/2/3/4	120/4.8

The transient response of the VLS is simulated with 32 MHz input. The result is shown in Figure 57. The transient response is measured with 2pF load on each output node. Although there is a little waveform distortion, it can be ignored since the output is applied to the comparator. The power consumption is measured to be 1.4mW.

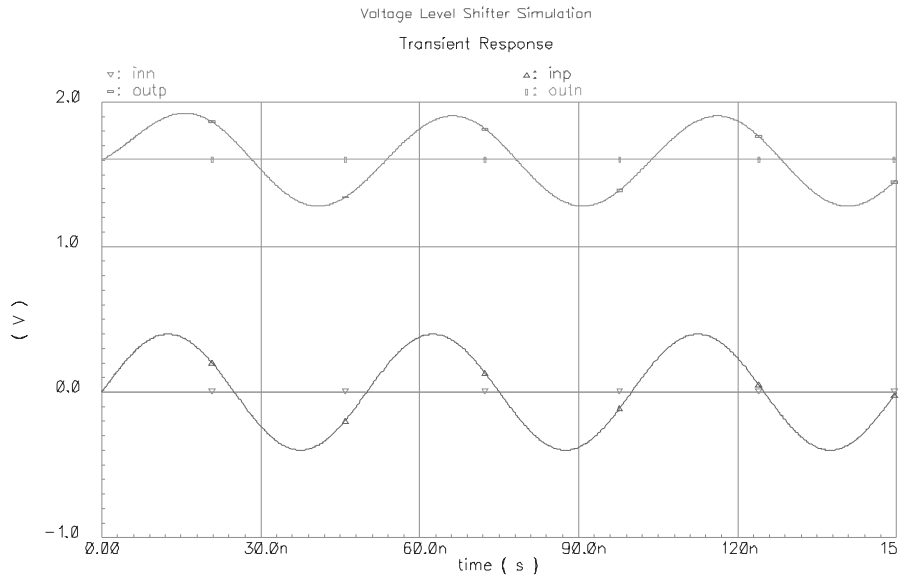


Figure 57. VLS transient response.

5.6 Resonator Interface Circuits

The resonator interface circuit includes two parts: amplification and cancellation circuits. The principle of the cancellation has been discussed in Section 4.2. Both the amplification circuit and cancellation circuit are implemented off-chip with OPA655 and BUF04. The circuits are shown in Figure 58 and Figure 59, respectively. The micromechanical resonator introduced in Section 3.3 is used in the design. The simulated frequency responses of the micromechanical resonator with and without cancellation circuit are shown in Figure 60 and Figure 61 respectively. The amplification is used to compensate the insertion loss of the micromechanical resonator, that is, the g in Eq.(28). Since the output of the amplification circuit is fed to the comparator and is converted to a digital output. The amplified signal has to be large enough to be resolvable for the comparator. For the comparator with 8-bit resolution, the Matlab simulation with g equal to 0.001 is shown in Fig. 62. Large idle tones and increased noise floor are observed. Further simulation shows, g has to be larger than 0.01 to make the SNR degradation negligible. The amplification circuit can realize the task.

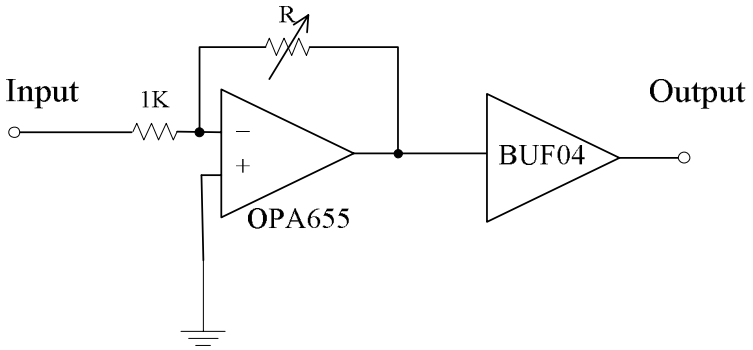


Figure 58. Amplification circuit.

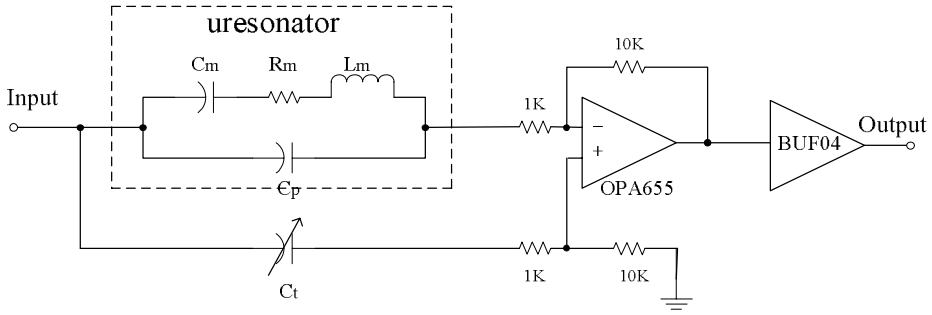


Figure 59. Cancellation circuit.

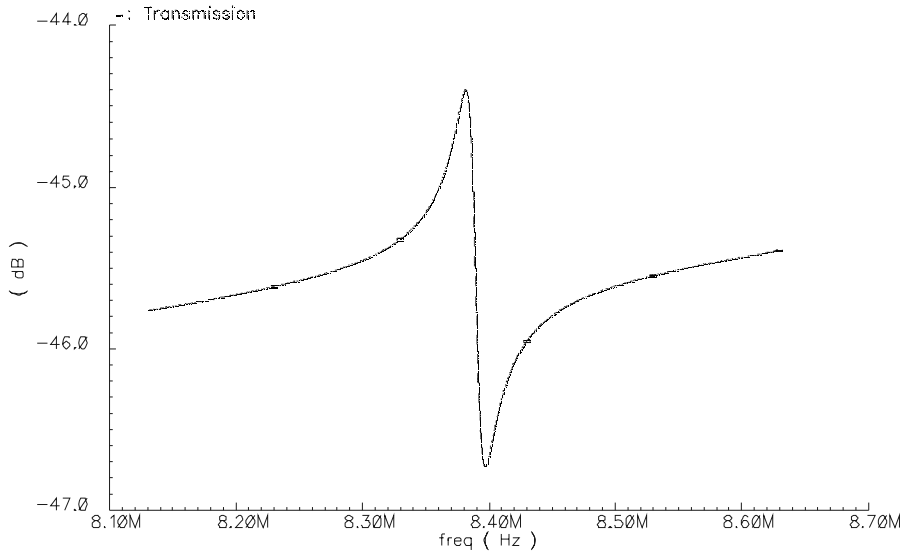


Figure 60. Frequency response of the micromechanical resonator.

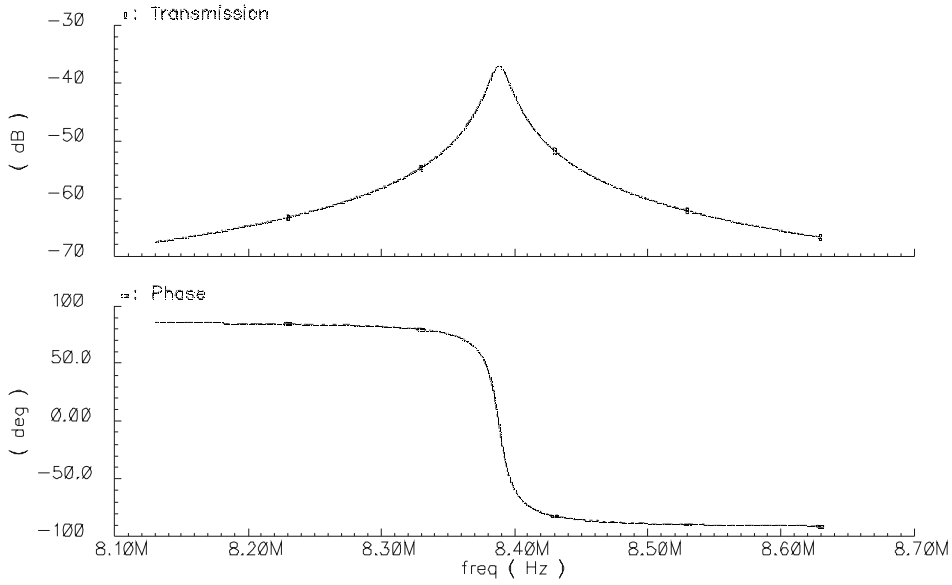


Figure 61. Frequency response of the resonator with anti-resonance cancellation.

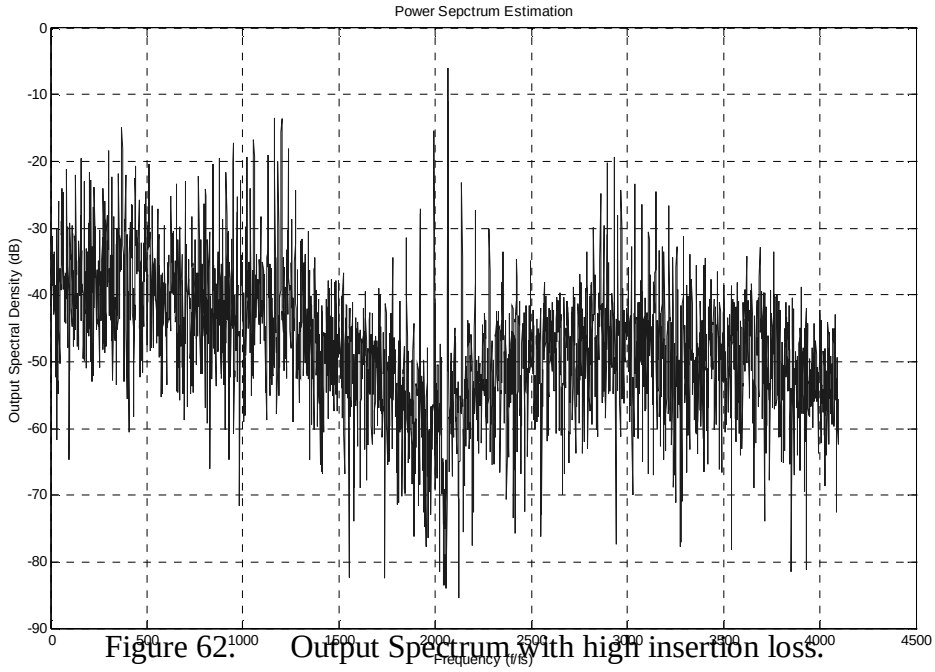


Figure 62. Output Spectrum with high insertion loss.

5.7 Performance of the Bandpass Sigma-Delta Modulator

The schematic-level simulation is done using Spectre in Cadence. The OPA655 and BUF04 are replaced with ideal op-amp and buffer. The micromechanical resonator model introduced in Section 3.3 is used in the simulation. The magnitude of the DAC output is chosen to be 200mV. Figure 63 shows the output power spectrum when the input signal is sinusoidal with amplitude of 120mV at 8.07MHz. The sampling frequency is 32MHz, and the spectrum is obtained with 8192-point FFT. Figure 64 shows the in-band spectrum in the 200-KHz bandwidth. The micromechanical resonator model described in Section 3.3 is used in the simulation. Figure 65 shows the SNR against input magnitude. The input magnitude is normalized with the DAC feedback voltage. For comparison, Matlab simulation result is also shown in Figure 65. Some SNR degradation is observed. The noise floor is also found to be lower than that of the Matlab simulation results as shown in Fig. 45. Since Matlab is based on ideal

logic blocks, the SNR degradation may due to the non-linearity of the circuit.

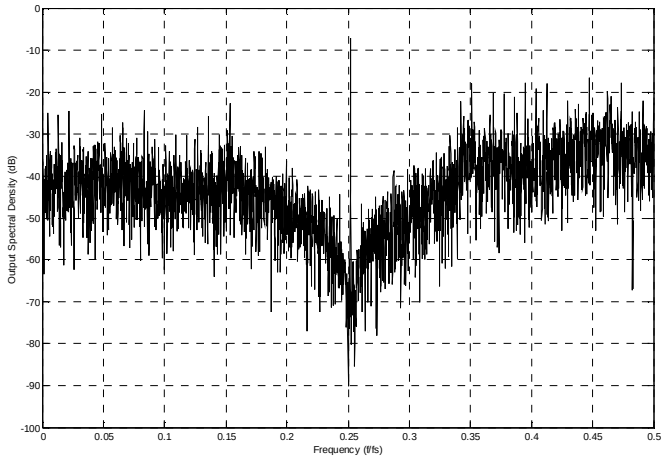


Figure 63. Output power spectrum at fs = 32 MHz.

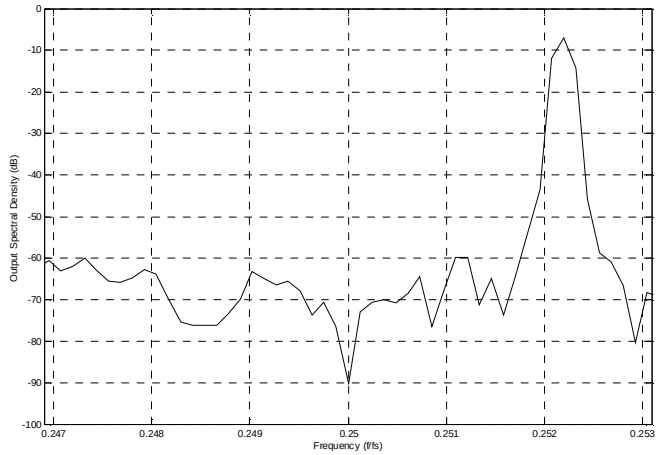


Figure 64. In-band output spectrum at fs = 32MHz.

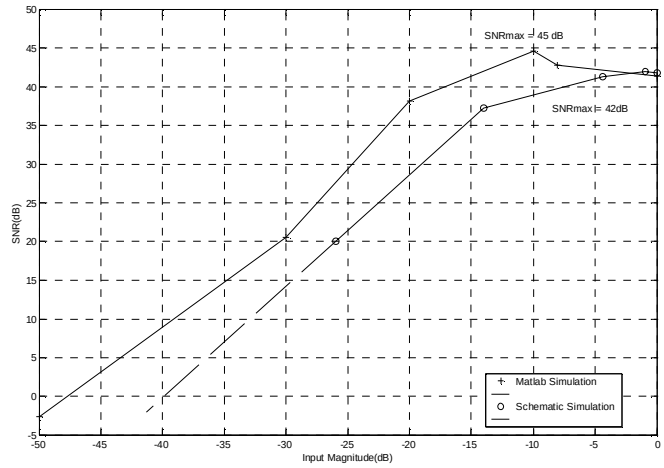


Figure 65. SNR against input magnitude at fs = 32MHz.

5.8 Layout Design and Post-layout Simulation

Some guidelines are adopted in the floor plan: first, the analog cells are separated from the digital cells to reduce interference. Secondly, the testing cells are arranged in similar environment to have the same performance. Thirdly, interconnects are considered in cell placement so that parasitic effects and crosstalk can be minimized.

The chip floor plan is shown in Figure 66.

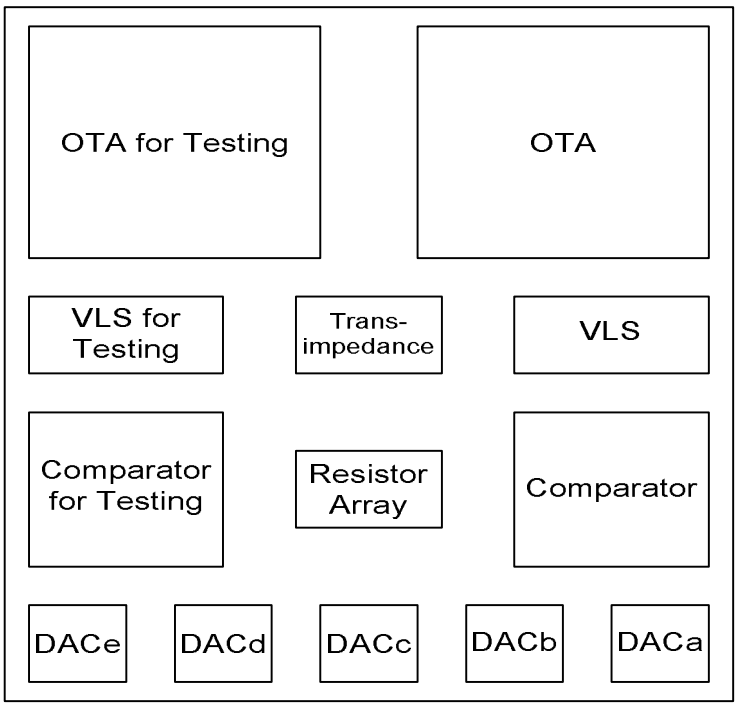


Figure 66. Layout floor plan.

In the layout, Separate analog and digital power supplies are used to reduce the interference. The analog ground is also separated from digital ground on-chip. Analog and digital cells are placed far from each other. To reduce substrate coupling, both N-well guard rings and P-well guard rings are used to separate the two sections.

Symmetric structures are adopted for most of the cells to improve the matching. Dummy cells are also used in the sensitive parts to eliminate the boundary effects. To further improve matching, the important transistors such as the OTA input transistors

are implemented in the common-centroid form [John97].

Parasitic effect is another important issue in the layout design. Crossing routing is avoided whenever it is possible to reduce parasitic capacitances, and reasonable wire width is used to reduce parasitic resistances.

The resistor array is implemented with high-resistive poly layer. To realize good matching among the resistors, each resistor is designed into two fingers. Each finger is interdigital with fingers from other resistors [John97]. Dummy fingers are included to match boundary condition.

The chip area is 580 × 650 microns without pads and 2160 × 2160 microns with pads. The chip is packaged in a Dual In Line 48 (DIL48) package. The full chip layout can be found in Appendix C.

The post-layout simulation is done with the same condition as that of the schematic level. The overall and in-band output power spectrum are shown in Figure 67 and Figure 68, respectively. The measured peak SNR is 42dB with -4.4dB input. The performance is close to the 45dB Matlab simulation result. The 3dB performance degradation is reasonable considering Matlab simulation is purely ideal. The simulation is close to the schematic simulation results.

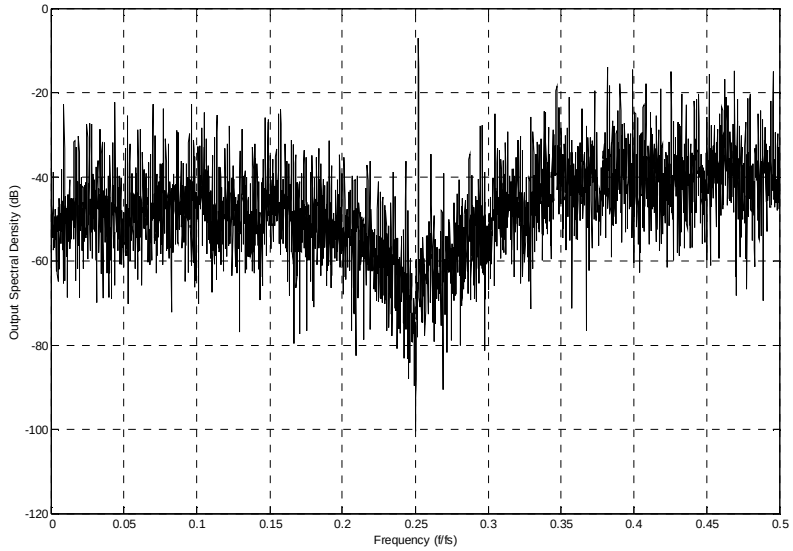


Figure 67. Output power spectrum at fs = 32 MHz from post-layout simulation.

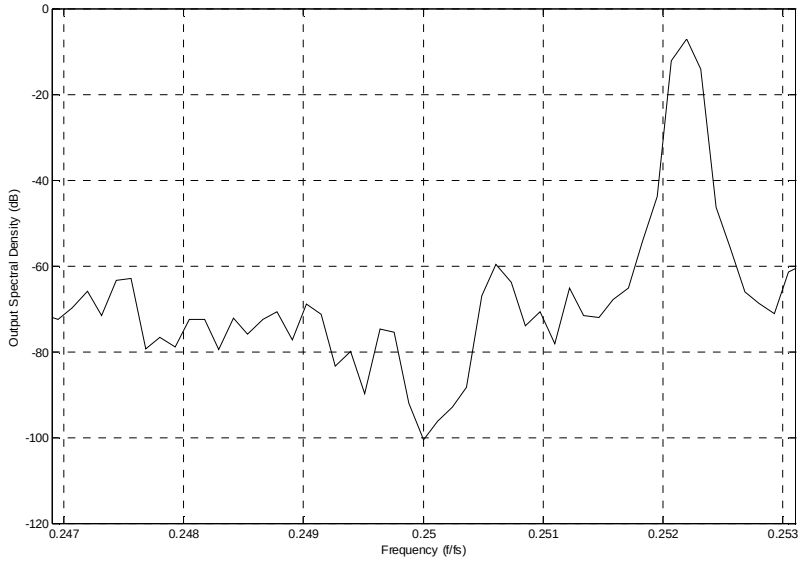


Figure 68. In-band output power spectrum at fs = 32 MHz from post-layout simulation.

Chapter 6 Testing

This chapter describes the chip evaluation and presents the test results. Some discussions about the test results are also included.

6.1 Testing Setup

The complete testing setup is shown in Figure 69.

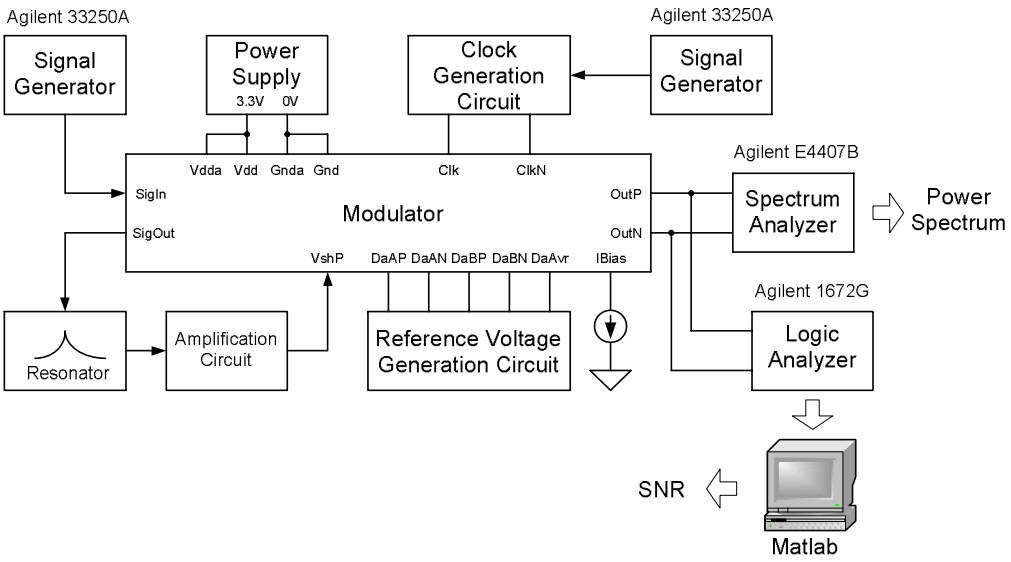


Figure 69. Test setup.

The analog spectrum analyzer is used to observe the output power spectrum. Its result is not accurate since it is sensitive to analog imperfections in the output bit stream waveform. Exact power spectrum is obtained through Matlab by using the data captured with the logic analyzer. Since the logic analyzer sampling period step size is 8ns, we select 248ns period for 4MHz, and 32ns for 32MHz sampling frequencies, respectively.

The analog ground is set to be 1.65V. Based on the coefficients calculated in

Section 4.3, the reference voltages of the return-to-zero DAC are 2.186V and 1.114V respectively. The reference voltages of the half-return-to-zero DAC are 1.872V and 1.428V respectively.

A complementary clock is needed in the testing. Signal generator Agilent 33250A is used as the master clock and the complementary clock is generated using a D flip-flop. The circuit is shown in Figure 70. The circuit can be used to generate clock up to 70 MHz.

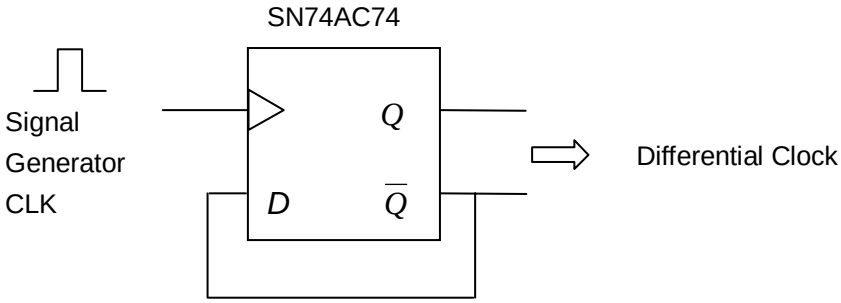


Figure 70. Differential clock generation circuit.

The biasing circuit for the OTA is shown in Figure 71. Rv is a variable resistor. The 1K resistor is used to monitor the bias current.

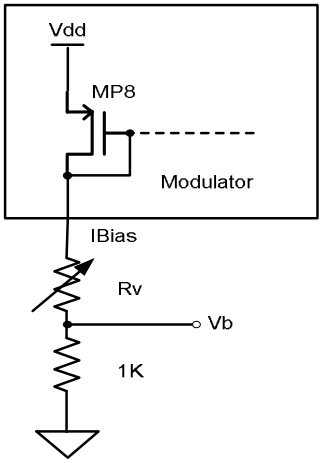


Figure 71. Off-chip bias circuit.

The reference voltages of the DACs are generated with the circuit shown in Figure 72.

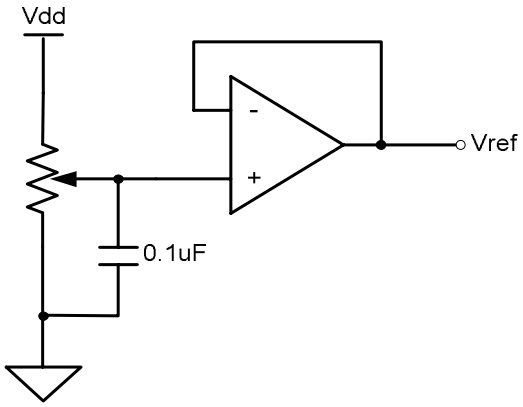


Figure 72. Reference voltage generation circuit.

6.2 Testing Result

6.2.1 Modulator with Micromechanical Resonator

The testing is first carried out with the micromechanical resonator discussed in Section 3.3. The amplification with a gain of 2000 is used for the resonator to boost its gain. Unfortunately, the test fails to demonstrate the function of the bandpass ΣΔ modulator. The noise shaping cannot be observed.

6.2.2 Modulator with Crystal Resonators

Since there is only one micromechanical resonator available for the testing and its performance is rather poor, a crystal resonator is used instead. Crystal resonator is very similar to the micromechanical resonator. Its equivalent circuit is the same as that of the micromechanical resonator. Compared with the micromechanical resonator, the crystal resonator has low insertion loss.

Two crystal resonators are used in the test. Their resonant frequencies are 1MHz and 8MHz, respectively. Figure 73 and Figure 74 show the measured frequency responses, respectively. Figure 75 shows their frequency response of the 1-MHz

resonator with the anti-resonance cancellation circuit.

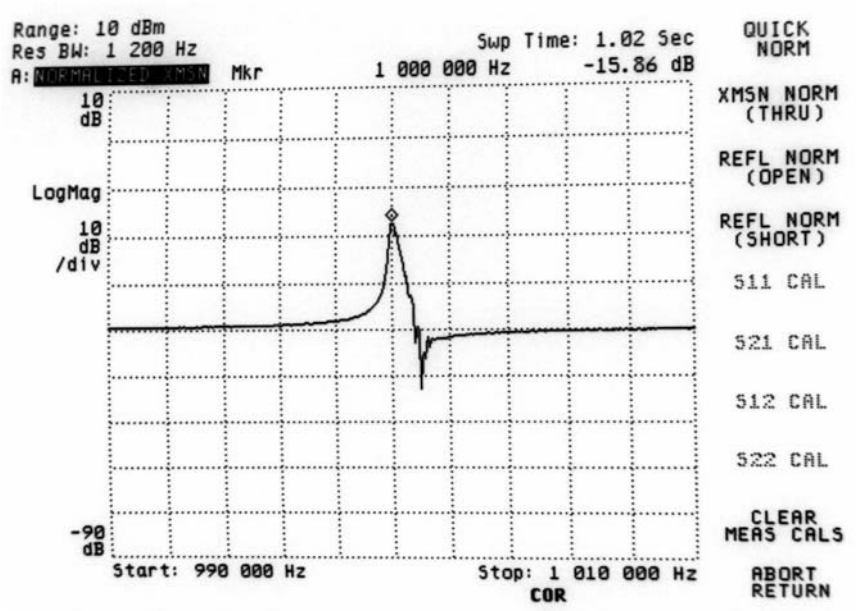


Figure 73. Frequency response of the crystal resonator with resonant frequency of 1MHz.

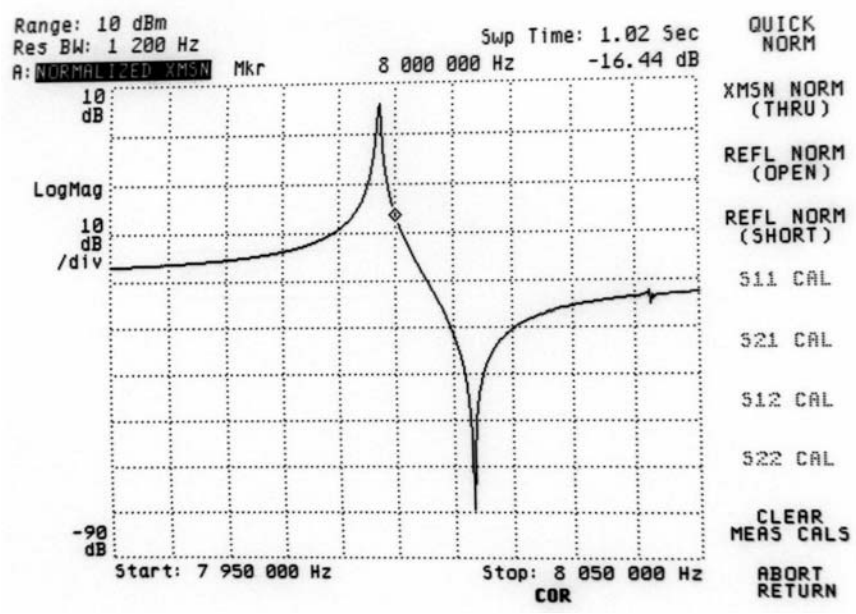


Figure 74. Frequency response of the crystal resonator with resonant frequency of 8MHz.

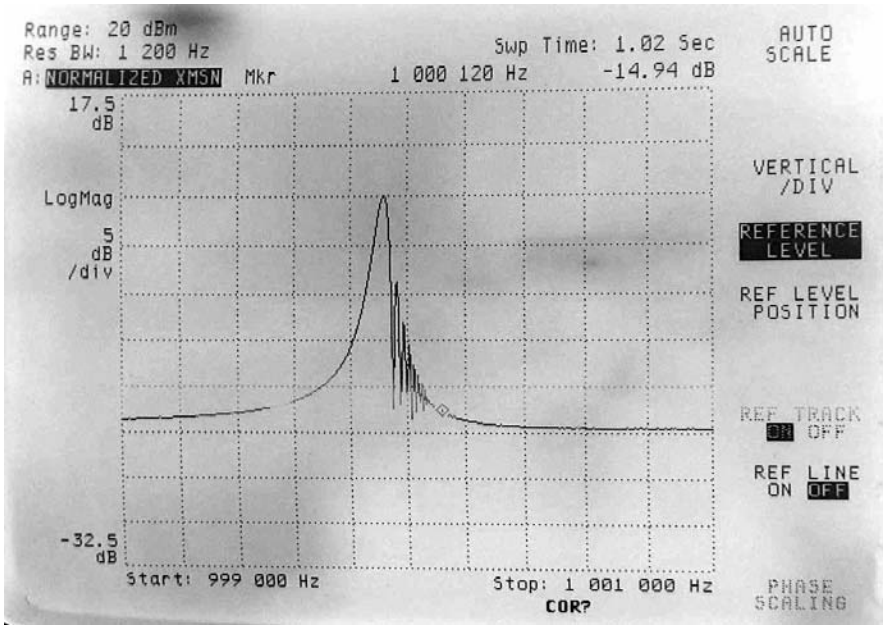


Figure 75. Frequency response of the 1-MHz crystal resonator with anti-resonance cancellation.

The bandpass ΣΔ modulator is first tested without the anti-resonance cancellation. The result is shown in Figure 76 where the 1-MHz crystal resonator is used. Figure 77 shows the in-band spectrum. The noise shaping (notch) in the output spectrum can be clearly seen, although there are many spurious tones which are typical for a second-order bandpass ΣΔ modulator.

Signal with amplitude of 120mV at frequency of 1.065MHz is used in the test. The full-scale input for the modulator is designed to be 200mV. An amplification with the gain of 73 is added for the resonator to boost its gain.

Another test is carried out with an increased frequency. The 8-MHz resonator is used in this test and a 10× gain stage is added. The measured output spectrum of this modulator is shown in Figure 78. The amplitude of the input signal used in the test is 120mV at 8.3MHz.

Although the theoretical analysis and Matlab simulation show that the bandpass

ΣΔ modulator using crystal resonator cannot be realized without anti-resonance cancellation, the experiments have demonstrated the bandpass ΣΔ modulators using crystal resonators with and without anti-resonance cancellation.

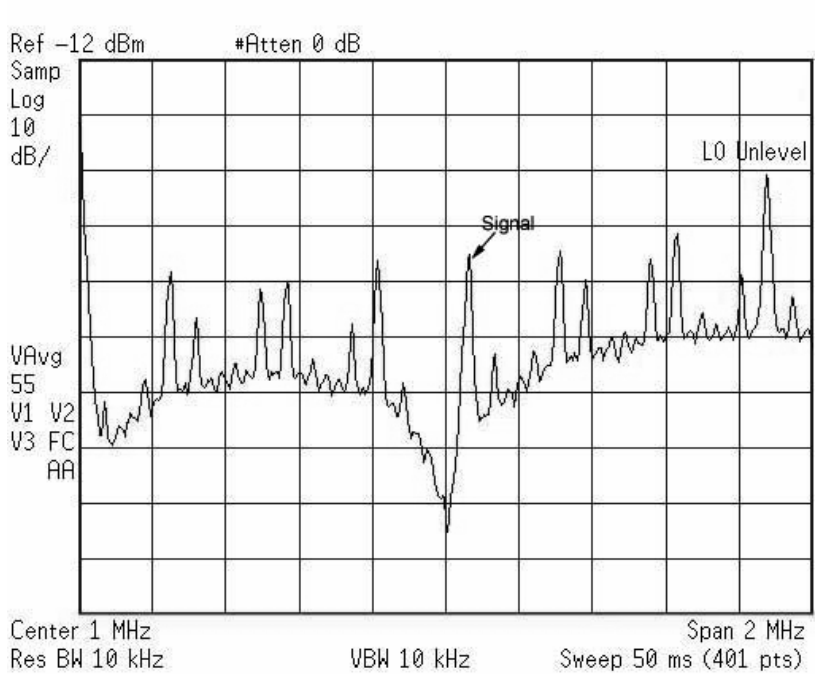


Figure 76. Output power spectrum of the bandpass ΣΔ modulator with 1-MHz crystal resonator.

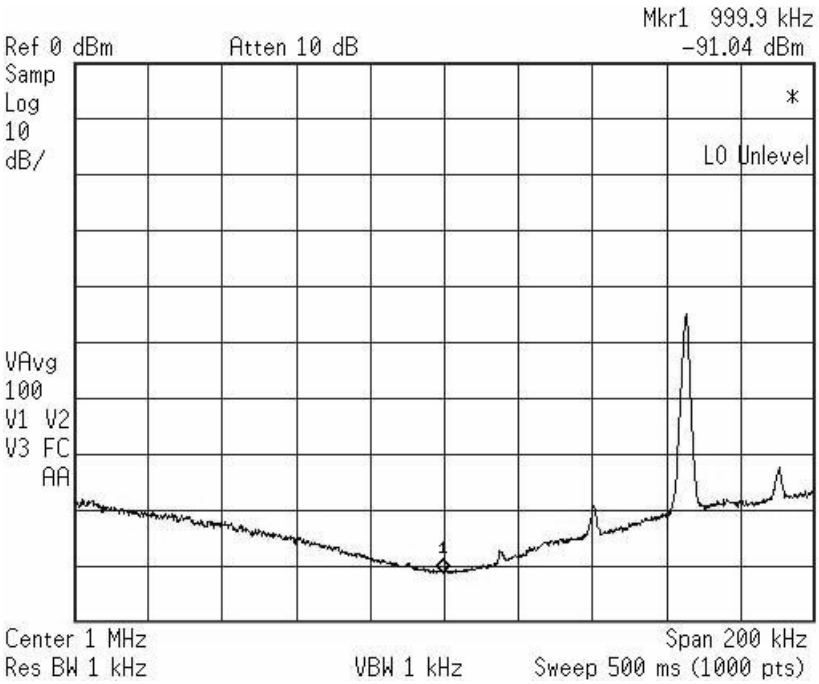


Figure 77. In-band spectrum of the modulator with 1-MHz crystal resonator.

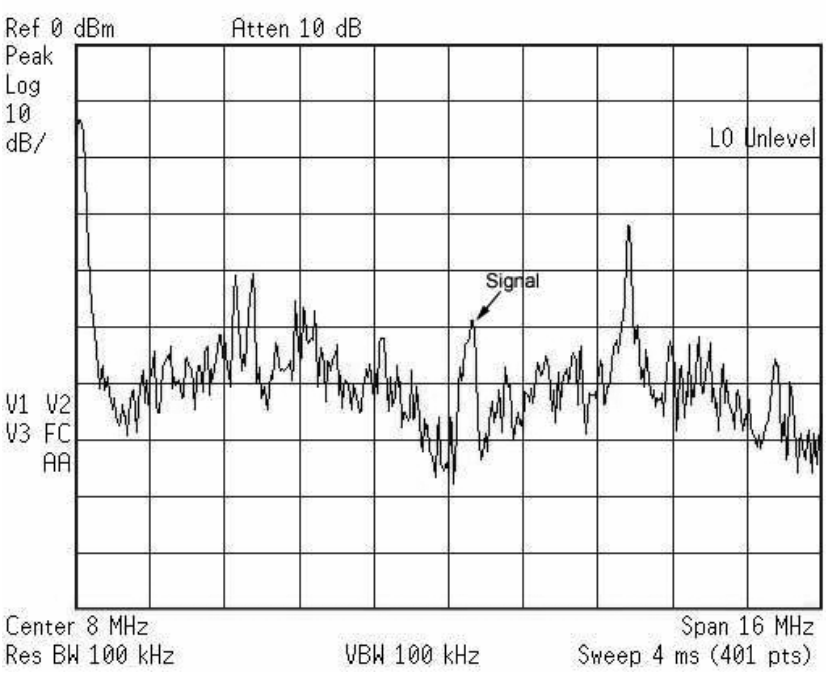


Figure 78. Output spectrum of the modulator with 8-MHz crystal resonator.

Figure 79 shows the output spectrum of the modulator with 1-MHz crystal resonator with anti-resonance cancellation circuit. The total gain, including the 10× gain in the cancellation circuit, is 73. The noise shaping and less spurious tones can be observed.

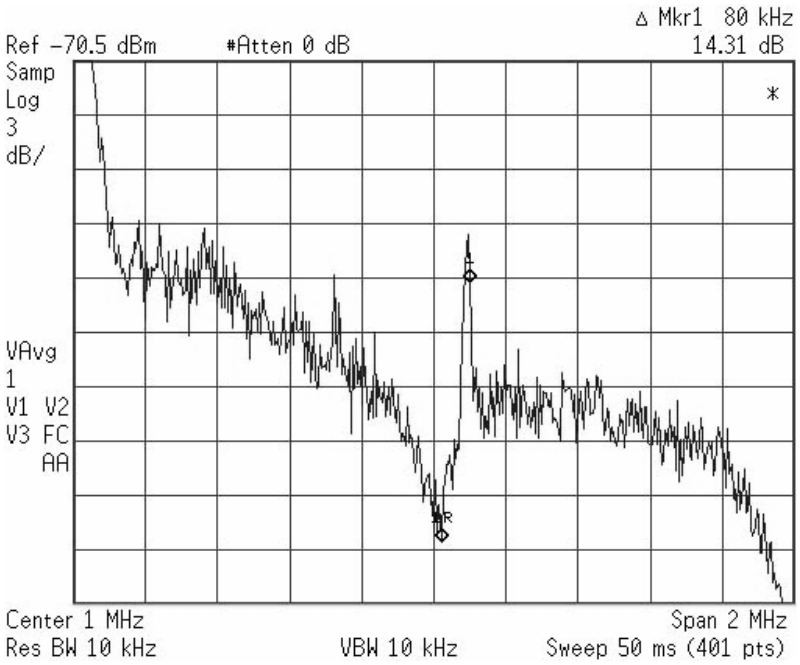


Figure 79. Output power spectrum (1-MHz crystal resonator with anti-resonance cancellation).

6.2.3 Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) of the modulator is also evaluated with a 1-MHz crystal resonator. The measured SNR versus input signal level, when the bandwidth is 200 kHz and OSR is 10, is shown in Figure 80 together with the simulation results from Matlab. Around -2 to -7dB performance degradation is observed. In testing, the minimum input applied is -4.4dB. When further decreasing the input, the SNR cannot be measured. That may be due to the poor sensitivity of the comparator. Similar phenomenon was also reported in [Gao98a]. When OSR is increased to 80, the peak SNR is measured to be 40dB. This value is close to the 45dB Matlab simulation and 42dB post-layout simulation results.

The SNR for 32MHz sampling frequency is not calculated, because the signal cannot be tuned into the bandwidth. Shifting the signal in the bandwidth will result in large idle tones.

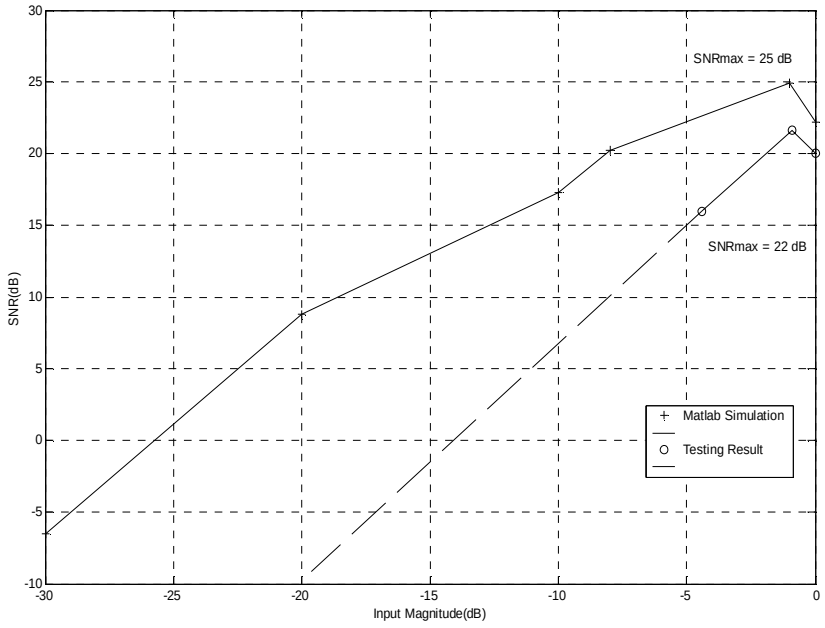


Figure 80. SNR vs. input signal level (1-MHz crystal resonator, OSR = 10).

6.3 Discussion

The chip testing fails to demonstrate the bandpass ΣΔ modulator with micromechanical resonator. The may be attributed to the poor performance of the micromechanical resonator used in the test. First the stop band rejection of the resonator with and without anti-resonance cancellation is very small, about 1-3dB. This makes the noise shaping notch is very small and hard to observe. Since the noise transfer function of the sigma-delta modulator is approximately the reciprocal of the resonator transfer function, small stop-band rejection reduces the depth of the notch in the noise shaping and hence degrades the SNR. Second, the high insertion loss, about -60dB, requires additional amplifier to boost the gain. The multi-stage off-chip amplifier introduces phase shift which may alter the overall transfer function.

Crystal resonators have similar transfer characteristics as micromechanical resonators. However, their insertion loss is low and the stop band rejection is higher than the micromechanical resonator, which can be seen from Figure 30 and Figure 74. Thus, the crystal resonators are used instead in the test. The test results with crystal resonators have shown reasonable good noise shaping, which proves that the proposed architecture and design methodology are correct.

Another phenomenon observed in the experiment is that the bandpass ΣΔ modulator can be realized with the crystal resonator when there is no anti-resonance cancellation. A possible reason is that the parasitic capacitance functions as a cancellation capacitor and compensates the effect of the anti-resonance. During the test, it is found that the cancellation circuit is very sensitive to parasitic effects. If the

parasitic capacitance is close to the desired cancellation capacitor, the relatively poor noise-shaping with additional cancellation circuit can be explained as over-compensation. The effect and cancellation method of anti-resonance need to be further studied.

Chapter 7 Conclusions and Future Work

7.1 Conclusion

A micromechanical resonator based second-order bandpass ΣΔ modulator has been proposed, designed and evaluated. In the proposed modulator, a micromechanical resonator is used to replace the conventional resonator implemented in electronic circuit. The modulator design is based on pulse-invariant transform and multi-feedback technique. A cancellation circuit is proposed to remove the anti-resonance from the micromechanical resonator and enables the realization of the desired transfer function for the bandpass ΣΔ modulator.

Based on the micromechanical resonator model, the simulation has shown that around 48dB dynamic range can be expected. However, the experiment fails to demonstrate the performance predicted in the simulation, due to the poor performance of the only available micromechanical resonator. The modulator chip is further tested with crystal resonators and reasonably good results were obtained. At a sampling frequency of 4MHz, when OSR is 10, the peak SNR is measured to be 22dB. When OSR is 80, the peak SNR is measured to be 40dB.

The test results with the crystal resonators have proven the feasibility of realizing bandpass ΣΔ modulator with crystal and other similar resonators.

7.2 Future Work

Although this work has demonstrated the possibility of realizing bandpass ΣΔ modulator with non-electronic resonators, such as crystal resonators, further study is needed to investigate the problem revealed during this work. First, it has been observed in the test that the bandpass ΣΔ modulator can be realized with the crystal resonator without anti-resonance cancellation. Further test and study should be carried out to understand the phenomenon. Second, the effect of the additional phase shift introduced by the gain boost circuit on the functionality and the performance of the modulator needs to be studied. Finally, upon resolving the above problems, high-order bandpass ΣΔ modulator may be attempted.

References

[Abid95] A.A. Abidi. "Direct-conversion radio transceivers for digital communications". *IEEE J. of Solid-State Circuits*, vol. 30, no. 12, Dec. 1995.

[Bach95] W. Bacher, W. Menz, and J. Mohr. "The LIGA technique and its potential for Microsystems-a survey". *IEEE Trans. on Ind. Electronics,* vol. 42, pp. 431-441, 1995.

[Baza98] S. Bazarjani and W.M. Snelgrove. "A 160-MHz fourth-order double-sampled SC bandpass Sigma-Delta modulator". *IEEE Trans. on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 45, no. 5, pp. 547-555, Mar. 1998.

[Benn48] W. Bennett. "Spectra of quantized signals". *Bell System Tech. J.*, vol. BSTJ-27, pp. 446-472, 1948.

[Bili01] D. Bilic. "Micromachined resonators". PhD thesis, UC Berkeley, 2001. (http://www-bsac.eecs.berkeley.edu/archive/)

[Bust98] J. M. Bustillo, R. T. Howe, and R. S. Muller. "Surface micromachining for microelectromechanical systems". *Proceedings of the IEEE*, vol. 86, no. 8, Aug. 1998.

[Cand92] J. C. Candy, and G. C. Temes. "Oversampling methods for A/D and D/A conversion". In J. C. Candy and G. C. Temes, editors. *Oversampling delta-sigma data converters: theory, design and simulation*, pp. 1-28. IEEE, New York, 1992.

[Carl86] A.B. Carlson, "Communication systems". San Francisco: McGraw-Hill, 1986.

[Cher00] J.A.Cherry, and W.M.Snelgrove. “Continuous-time delta-sigma modulators for high-speed A/D conversion – theory, practice and fundamental performance limits”. Kluwer Academic Publishers, 2000.

[Cher00a] J.A.Cherry, and W.M.Snelgrove. “On the design of a fourth-order continuous-time LC Delta-Sigma modulator for UHF A/D convresion”. *IEEE Trans. on Circuits and Systems–II: Analog and Digial Signal Processing*, vol. 47, no. 6, June, 2000.

[Cusi01] P. Cusinato, D. Tonietto, F. Stefani, and A. Baschirotto. “A 3.3-V CMOS 10.7-MHz sixth-order bandpass ΣΔ modulator with 74-dB dynamic range”. *IEEE J. of Solid-State Circuits*, vol. 36, no. 4, April, 2001.

[Gabr98] K. J. Gabriel. “Microelectromechanical Systems (MEMS) Tutorial”. *Proc. Int. Test Conf.*, pp. 432-441, 1998.

[Galt02] I. Galton. “Delta-Sigma data conversion in wireless transceivers”. *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, no. 1, January, 1996.

[Galt96] I. Galton. “Noise-shaping D/A conversion for ΔΣ modulation”. *Proc. Int. Symp. on Circuits and Systems*, vol. 1, pp. 441-444, 1996.

[Gao98] W. Gao, and W. M. Snelgrove. “A 950-MHz IF second-order integrated LC bandpass delta-sigma modulator”. *IEEE J. of Solid-State Circuits*, pp. 723-732, May 1998.

[Gao98a] W. Gao, J. A. Cherry, and W. M. Snelgrove. “A 4GHz fourth-order SiGe HBT bandpass ΔΣ modulator”. *Symp. On VLSI Circuits, Digest of Technical Papers*, pp. 174-175, June, 1998.

[Gard86] F. M. Gardner. “A transformation for digital simulation of analog filters”. *IEEE Trans. Communications*, pp. 676-680, July 1986.

[Hair96] A. Hairapetian. “An 81-MHz IF receiver in CMOS”. *IEEE J. of*

Solid-State Circuits, vol. 31, pp. 1981-1986, Dec. 1996.

[Hay86] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura. "A multi-stage delta-sigma modulator without double integration loop". *Int. Solid-State Circuits Conf. Technical Digest*, pp. 182-183, 1986.

[Hsu00] I. Hsu, and H. C. Luong. "A 70-MHz continuous-time CMOS band-pass ΣΔ modulator for GSM receivers". *Int. Symp. On Circuits and Systems 2000*, vol. 3, pp. 750-753, May, 2000.

[Inos62] H. Inose, Y. Yasuda, and J. Murakami. "A telemetering system by code modulation –Δ-Σ modulation". *IRE Trans. Space Electron. Telemetry*, vol. SET-8, pp. 204-209, Sep. 1962.

[Jant92] S. A. Jantzi, M. Snelgrove. "A 4^{th}-order bandpass Sigma-Delta modulator". *Proc. of IEEE 1992 Custom Integrated Circuits Conf.*, pp. 16.5.1-16.5.4, May, 1992.

[John97] D. A. Johns, and K. Martin. "Analog integrated circuit design". John Wiley & Sons, Inc. 1997.

[Long93] L. Long, and B.-R. Horng. "A 15b 30kHz bandpass Sigma-Delta modulator". *IEEE Proc. Int. Solid-State Circuits Conf.*, pp. 226-228, Feb. 1993.

[Mats87] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, and T. Yoshitome. "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping". *IEEE J. Solid-State Circuits*, pp. 921-929, Dec. 1987.

[Maur00] R. Maurino, and P. Mole. "A 200-MHz IF 11-bit fourth-order bandpass ΔΣ ADC in SiGe". *IEEE J. of Solid-state Circuits*, vol. 35, no. 7, July 2000.

[Nath67] H. C. Nathanson, W. E. Newell, R. A. Wickstrom, J. R. Davis, Jr.. "The resonant gate transistor". *IEEE Trans. on Electron Devices*, vol. ED-14, no. 3, pp. 117-133, March 1967.

[Nguy01] Clark T.-C. Nguyen. “Transceiver front-end architectures using vibrating micromechanical signal processors”. *Dig. of Papers, Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 23-32, Sep. 2001.

[Nguy99] C. T.-C. Nguyen. “Microelectromechanical components for miniaturized low-power communications”. *Proc. IEEE MTT-S International Microwave Symp. RF MEMS Workshop*, pp. 48-77, California, USA, June 1999.

[Nors97] S. R. Norsworthy, R. Schreier and G. C. Temes. “Delta-sigma data converters, theory, design and simulation”. IEEE Press, PC3954, 1997.

[Ong97] A.K.Ong, and B.A.Wooley. “A two-path bandpass Sigma-Delta modulator for digital IF extraction at 20 MHz”. *IEEE J. Solid-State Circuits*, vol. 32, pp. 1920-1934, Dec. 1997.

[Oppe89] A. V. Oppenheim and R. W. Schafer. “Discrete-Time Signal Processing”. New Jersey, Prentice Hall, 1989.

[Sant99] Hector J. de los Santos. “Introduction to microelectromechanical (MEM) microwave systems”. Boston: Artech House, 1999.

[Schr89] R. Schreier and M. Snelgrove, “Bandpass Sigma-Delta modulation”. *Electronics Letters*, vol. 25, no. 23, pp. 1560-1561, Nov. 1989.

[Shoa94] O. Shoaei and W.M. Snelgrove. “Optimal (bandpass) continuous-time ΣΔ modulator”. *Proce. of Int. Symp. on Circuits and Systems*, vol. 5, pp. 489-492, 1994.

[Shoa95] O. Shoaei and W.M. Snelgrove. “A multi-feedback design for LC bandpass Delta-Sigma modulators”. *Int. Symp. on Circuits and Systems*, vol. 1, pp. 171-174, May 1995.

[Shoa97] O. Shoaei and W.M. Snelgrove. “Design and implementation of a tunable 40 MHz-70 MHz Gm-C bandpass ΔΣ modulator”. *IEEE Trans. on Circuits and*

Systems–II: Analog and Digial Signal Processing, vol. 44, no. 7, July 1997.

[Sing95] F.W. Singor and W.M. Snelgrove. "Switched-capacitor bandpass Delta-sigma A/d modulation at 10.7MHz". *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 184-192, Mar. 1995.

[Thur91] A. M. Thurston, T. H. Pearce, and M. J. Hawksford. "Bandpass implementation of the Sigma-Delta A-D conversion technique". *Int. Conf. on A.-D. and D.-A. Conversion*, pp. 81-86, 1991.

[Wang00] K. Wang, A.-C. Wong, and C. T.-C. Nguyen. "VHF free-free beam high-Q micromechanical resonators". *IEEE J. of MEMS*, vol. 9, no. 3, September 2000.

[Widr56] B. Widrow. "A study of rough amplitude quantization by means of Nyquist sampling theory". *IRE Trans. Circuit Theory*, vol. CT-3, pp. 266-276, December 1956.

Appendix A Matlab Programs

A.1 Program for Pulse-invariant Transform

```
% ------------------------------------
% Program:          Ct2Dt.m
% Author:           Xiaofeng Wang
% Date:             02/25/2002
% Last Update:      12/29/2002
% Descritption:     To design the equivalent continuous-time modulator
%                   Only for 2nd order bandpass. Have to revise the
%                   calculation part for other modulators
% ------------------------------------


% --- Clear working space and window ---
clear all;
clc;
% --- Clear working space and window end ---


% --- Macro definition ---
% Normalized transfer function of the continuous modulator
num = [1 0];
den = [1 0 (pi/2)^2];
% --- Macro definition end ---


% --- System creation ---
SysC = tf(num,den);
% Continuous system in the form of transfer function
[ac,bc,cc,dc] = tf2ss(num,den);
% Continuous system in the form of state space
SysCSs = ss(ac,bc,cc,dc);
% Create a state space obeject based on the continuous system

SysDSs = c2d(SysCSs,1);
% Discrete state space form
% --- System creation end ---
```

```
% ---- Return-to-Zero ----
SysDRSs = SysDSs;
% Syshss is a temp variable
% DAC output pulse
TB = 0;
% DAC 1 beginning point
TE = 0.5;
% DAC 1 ending point
SysDRSs.b = inv(SysCSs.a)*(expm(SysCSs.a*(1-TB)) - expm(SysCSs.a*(1-TE)))*SysCSs.b;
fprintf('\n R-return-to-zero: ');
TfRz = tf(SysDRSs)
% --- Return-to-Zero end ----


% --- Half-Return-to-Zero ---
SysDHSs = SysDSs;
% syshss is a temp variable
% DAC output pulse
TB = 0.5;
% DAC 1 beginning point
TE = 1;
% DAC 1 ending point
SysDHSs.b = inv(SysCSs.a)*(expm(SysCSs.a*(1-TB)) - expm(SysCSs.a*(1-TE)))*SysCSs.b;
fprintf('\n Half-return-to-zero: ');
TfHrz = tf(SysDHSs)
% --- Half-Return-to-Zero end ---


% --- Coefficients calculation ---
% The following section is used to calculate the feedback coefficients
CoB = [TfRz.num{1}(2:3); TfHrz.num{1}(2:3)]
CoC = [0 -1];
% CoC is the desired numerator.
% The DAC coefficients in the sequence of the DACs
CoA = CoC*inv(CoB)
% --- Coefficients calculation end ---


% (The end)
% ---------------------------------------
```

A.2 Program for Power Spectrum Estimation

```
% --------------------------------
% Program:              OutAnalyse.m
% Author:               Xiaofeng Wang
% Date:                 12/26/2001
% Last Updated:         12/29/2002
% Description:          Analyze the spectrum of the bit stream
%                       The program must work together with Simulink simulation
% --------------------------------


% Notice: N = 2^m, m is an integer
% fsignal = Fs/N*p, p is an integer, to alleviate leakage


% --- Initialization ---
% Clear figure window
clf;
% Receive the data from the work space
% insig is the input signal sequence
inp=insig';
% outsig is the output signal sequence of the modulator
outp=outsig';
% N is the length of the sequence
N=length(outp);
% --- Initialization end ---


% --- Input and output display ---
% Comparison between the input analog signal and the output digital signal
figure(1); clf;

t = 0:100;
% Demonstrate 100 points
stairs(t, inp(t+1));
hold on;
stairs(t,outp(t+1));

% Plot label
xlabel('sample number');
ylabel('input, output');
title('Modulator Input & Output');
```

```
% --- Input and output display end ---


% --- Spectrum analysis ---
figure(2); clf;

Fs = 1;
w = hanning(N);
% Hanning windowing

[Pxx,f] = psd(outp,N,Fs,w,N/2);
% [magnitude,frequency] =
% (signal,sample number,sampling frequency,window,overlap number)

Pyy = Pxx*norm(w)^2/sum(w)^2;
% De-normalization
Pn = 10*log10(2*Pyy);
% Sum of positive and negative frequency

% Plot
plot(f/Fs,Pn);
xlabel('Frequency (f/fs)');
ylabel('Output Spectral Density (dB)');
title('Power Sepctrum Estimation');
grid;
% --- Spectrum analysis end ---


% (The end)
% --------------------------------
```

A.3 Program for SNR Calculation

```
% --------------------------------
% Program:          BpSnrCalculate.m
% Author:           Xiaofeng Wang
% Date:             12/30/2001
% Last Updated:     12/29/2002
% Description:      Calculate the SNR of a bandpass Sigma-Delta modulator
% --------------------------------


% --- Macro definition ---
% Receive the data from the work space
% outsig is the output signal sequence of the modulator
outp=outsig';
N = length(outp);
% N is the number of the samples; it should be power of 2.
OSR = 80;
% OSR is the oversampling ratio
BW = N/2/OSR;
% BW is the interest bandwidth
Fs = 1;
% Fs is the sampling frequency. It should be 1 after normalization.

BWbb = round(0.25*N-BW/2);
% BW beginning bin
BWeb = round(0.25*N+BW/2);
% BW ending bin
% --- Macro definition end ---


% --- Power spectrum calculation ---
w = hanning(N);
% Hanning windowing
[Pxx,f] = psd(outp,N,Fs,w,N/2);
% [magnitude,frequency] =
% (signal,sample number,sampling frequency,window,overlap number)
Pyy = Pxx*norm(w)^2/sum(w)^2*2;
% De-normalization of the hanning windowing
% --- Power spectrum calculation end ---


% --- SNR calculation ---
```

```
total_power = sum(Pyy(BWbb:BWeb));
% Total power of the interest bandwidth
[sigpw,fsigbintmp] = max(Pyy(BWbb:BWeb));
fsigbin = fsigbintmp + BWbb -1;
% Find the signal bin fsigbin

% Find the signal beginning bin
sbb = fsigbin;
while (Pyy(sbb-1) < Pyy(sbb)) & (sbb>BWbb);
      sbb = sbb-1;
end

% Find the signal ending bin
seb = fsigbin;
while (Pyy(seb+1) < Pyy(seb)) & (seb<BWeb);
      seb = seb+1;
end

% Calculate the total signal power
signal_power = sigpw;
% Calculate the total noise power
noise_power = total_power - sum(Pyy(sbb:seb)) + [Pyy(sbb-1)+Pyy(seb+1)]/2*(seb-sbb);
% Calculate the SNR
SNR = 10*log10(signal_power/noise_power)
% --- SNR calculation end ---


% (The end)
% -------------------------------
```

Appendix B Simulink Models

B.1 Simulink Model for Return-to-zero DAC

```
% -------------------------
% Program:          DacRz.m
% Author :          Sun Wai Hoong
%                   Revised by Xiaofeng Wang
% Date:             2001
% Last Updated:     12/29/2002
% Description:      S-function for Return-to-zero DAC
%                   It can be used for Half-return-to-zero DAC and other
%                   DACs with some modifications
% -------------------------


function [sys,x0,str,ts] = DacRz(t,x,u,flag)

dperiod = 1;
doffset = 0;

switch flag
case 0
      [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset);
case 3
      sys=mdlOutputs(t,x,u,doffset,dperiod);
   case {1, 2, 4, 9}
      sys = [];
      % do nothing
   otherwise
      error(['unhandled flag = ',num2str(flag)]);
end

function [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset)

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 0;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;
```

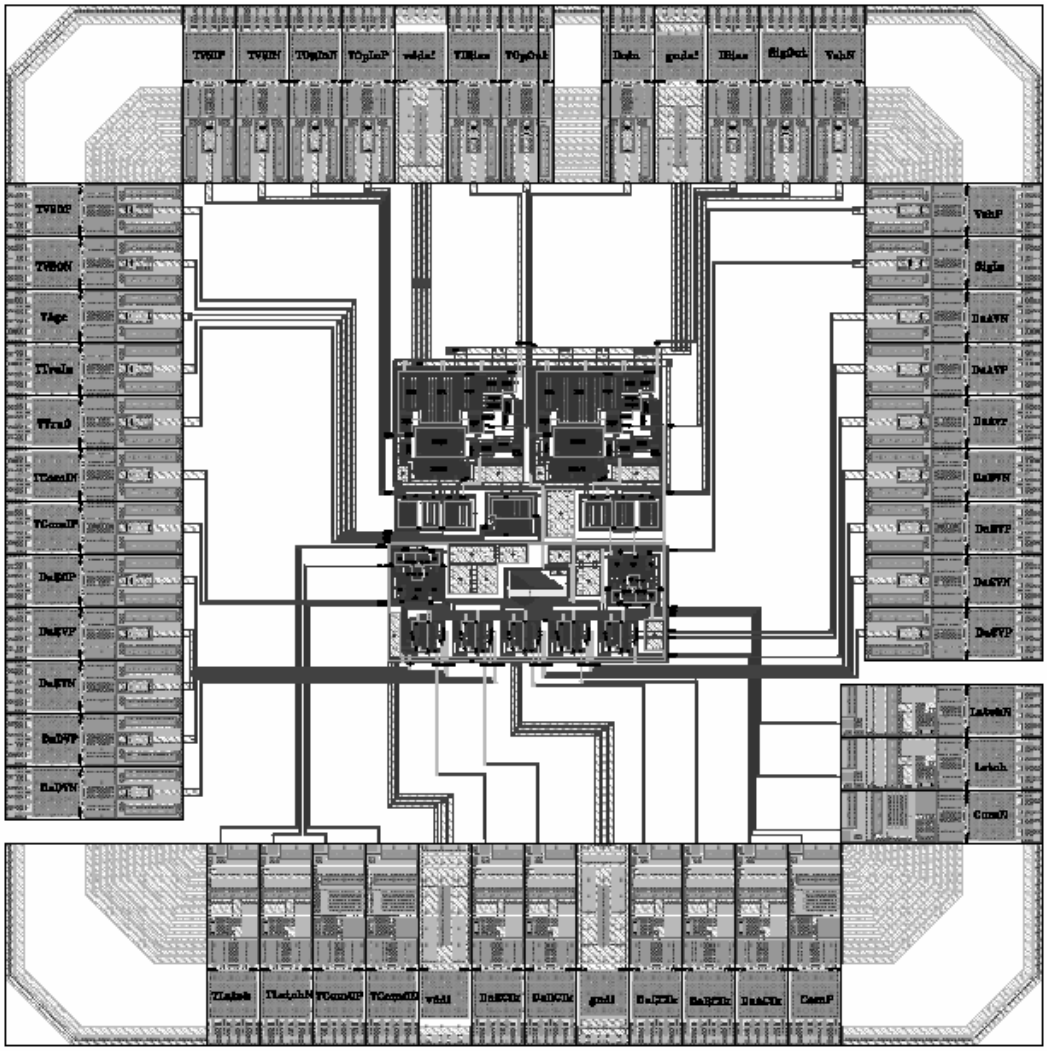
```
sys = simsizes(sizes);
x0    = [];
str = [];
ts    = [dperiod/2 0];
% Change this point according to the DAC you want to realize

function sys=mdlOutputs(t,x,u,doffset,dperiod)

if (t - doffset)/dperiod - floor((t - doffset)/dperiod) < dperiod/2
   sys = u;
% Change this point according to the DAC you want to realize
else
   sys = 0;
% Change this point according to the DAC you want to realize
end

% (The end)
% ----------------------------------------
```

B.2 Simulink Model for Half-return-to-zero DAC

```
% -------------------------
% Program:          DacHrz.m
% Author:           Sun Wai Hoong
%                   Revised by Xiaofeng Wang
% Date:             2001
% Last Updated:     01/05/2003
% Description:      S-function for Half-return-to-zero DAC
%                   It can be used for Return-to-zero DAC and other
%                   DACs with some modifications
% -------------------------

function [sys,x0,str,ts] = DacHrz(t,x,u,flag)

dperiod = 1;
doffset = 0;

switch flag
   case 0
      [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset);
   case 3
      sys=mdlOutputs(t,x,u,doffset,dperiod);
   case {1, 2, 4, 9}
      sys = [];          % do nothing
   otherwise
      error(['unhandled flag = ',num2str(flag)]);
end

function [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset)

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 0;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);
x0  = [];
str = [];
ts  = [dperiod/2 0];
```

```
function sys=mdlOutputs(t,x,u,doffset,dperiod)

if (t - doffset)/dperiod - floor((t - doffset)/dperiod) < dperiod/2
   sys = 0;
% Change this point according to the DAC you want to realize
else
   sys = u;
% Change this point according to the DAC you want to realize
end

% (The end)
% --------------------------------
```

Appendix C Chip Layout



Appendix D Chip Photograph