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ANALOG CMOS INTEGRATED CIRCUIT DESIGN

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NATIONAL UNIVERSITY OF SINGAPORE

2003

ANALOG CMOS INTEGRATED CIRCUIT DESIGN

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My appreciation also goes to my friends in Signal Processing and VLSI Design Lab, who have helped me through out my research work in many ways.

I also want to thank my families especially my wife Yang Jing. Because of their spiritual support, I have been able to complete this research work. They have given me the greatest courage to overcome all the difficulties.

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SUMMARY

This thesis is divided into two parts according to the two projects I was involved in during the past two years: VHF CMOS Transconductor design and CMOS LNA design.

In the first part, a novel IC structure realizing a low voltage CMOS VHF transconductor is proposed. This is a totally new design with some important features such as the high linearity I-V conversion and high common mode rejection ratio (CMRR). The advantage of the proposed transconductor is the simple circuit structure, which makes it suitable for very high frequency applications. The drawbacks of the proposed transconductor design are: there is no g_m tuning method except to changing the power supply voltage, which also implies that the transconductor has a poor power supply rejection ratio (PSRR); limited input signal range due to the cascade structure.

The second part of this thesis presents the detailed procedures of a CMOS fully integrated LNA design with the input and output matching network. Although the structure of a LNA contains only a small number of components in total, however, the choosing of each "proper" component contains lots of trade-offs. The performance of the LNA is sensitive to some of its components especially those in its output stage. Only a little incaution will cause oscillation or even result in the LNA failing to work. I have written down all my experiences of success and failure here to remind myself not to make the same mistake again.

In order to simplify the delivery of the main idea and let readers easily grasp the main

stem of the design procedure, only results are given in these two parts of the thesis. Readers can refer to the appendices for the detailed derivations procedures.

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1. PROJECT I: VHF CMOS Transconductor DESIGN 0[2]

1.1. Motivations

All modern communication systems, such as radio, TV, telephony and most instrumentation systems contain various types of electrical filters. Over the last decade active monolithic filters have become increasingly important for many signal processing applications. Monolithically integrated, filters have several advantages over active filters built with discrete components. These advantages are: good matching of components on chip, automatic tuning can correct the transfer function for process and temperature variations, reduced parasitic capacitances on chip, and last but not least: low-cost if these filters are fabricated in large numbers. In the design of monolithic analog filters at very high frequencies, high-speed, fully-balanced transconductance amplifier has received considerable attention as convenient active elements and the transconductance-capacitor (Gm-C) approach is used most often. This technique is well-known for implementing high-speed continuous time filters and is widely used in many industrial applications [4]

The core work of a Gm-C filter design is to design an OTA as ideally as possible with the following features:

An infinite input and output impedance;

An infinite frequency response bandwidth;

Large input and output linear range (Rail-to-rail);

Low voltage power supply and low power consumption;

Can be easily tuned;

Infinite CMRR (For differential input only).

Unfortunately these features are incompatible and have lots of trade-offs among them. Designers are trying their best to mediate the conflicts and focus their effort on the features which are more important in their application.

1.2. Some Transconductor design – A brief review

For a long time, in the field of continuous time analog filter design, people are seeking ways to make their design achieve better performance in HF application. In the realm of Gm-C filter design (low pass), the most critical problem is to design a transconductor that has a very high cut-off frequency. Further more, to get a better performance of the transconductor, a low voltage supply, linear input-output characteristic for wide range, large output resistance, high CMRR, and a tunable transconductance should be also be considered. In the following part of this report, these questions will be discussed and some design schemes will be presented.

1.2.1. Nauta's VHF transconductor design [5]

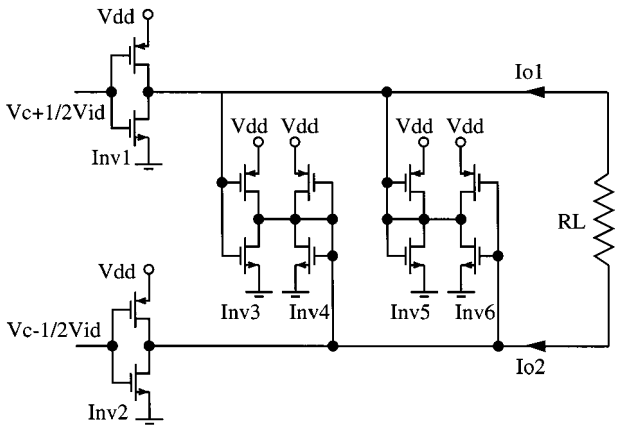


Fig 1 Nauta's VHF Transconductor.

A Gm-C filter technique for very high frequencies is proposed by Bram Nauta in 1994 that has a very attractive feature – VHF owing to its absence of internal node. The V-I conversion expression is shown below:

$$I_{od} = I_{o1} - I_{o2} = V_{id}\left(V_{dd} - V_{th} + V_{tp}\right)\sqrt{b_n \cdot b_p} = V_{id} \cdot gm_d \tag{1.1}$$

$$\text{Here} \quad b_n = \frac{m_n C_{ox} W_n}{L_n}, b_p = \frac{m_p C_{ox} W_p}{L_p} \tag{1.2}$$

The four inverters (Inv3--Inv6) constituting the so call Common-Mode Control and DC-Gain Enhancement part, which suppress the common mode signal and enhance the differential one. The result of this enhancement scheme is summarized in Table 1 Common and differential load resistances seen on nodes Vo1 and Vo2, Realized by the transconductors gm3-gm6 of Inv3-Inv6.

Output Node	Common Resistance	Differential Resistance
V_{o1}	$\frac{1}{g_{m5}+g_{m6}}$	$\frac{1}{g_{m5}-g_{m6}}$
V_{o2}	$\frac{1}{g_{m4}+g_{m3}}$	$\frac{1}{g_{m4}-g_{m3}}$

Table 1 Common and differential load resistances seen on nodes V_{o1} and V_{o2}, Realized by the transconductances gm3-gm6 of Inv3 -Inv6.

1.2.2. Szczepanski's OTA Design [6]

This is another transconductor design for VHF application proposed by Szczepanski.

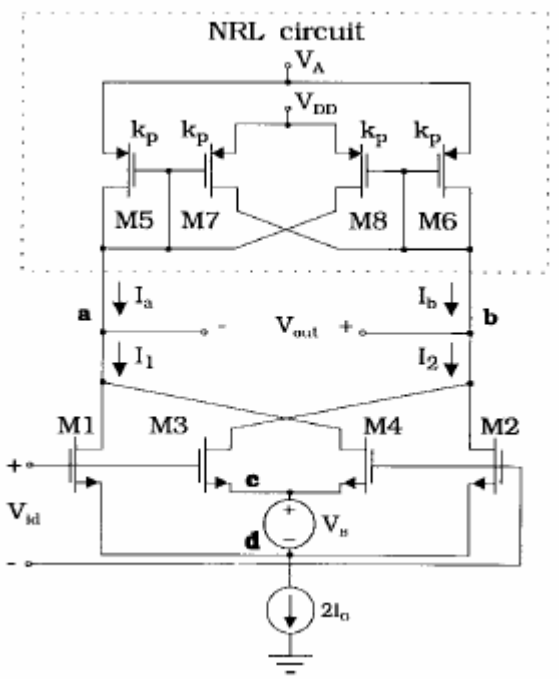


Fig 2 Simplified scheme of the proposed CMOS OTA with a voltage-variable NRL circuit

Without the upper potion of NRL (Negative Resistance Load) circuit, the V-I expression is:

$$I_{out} = I_1 - I_2 = 2k_n V_B V_{id} \tag{1.3}$$

The resistance of the NRL circuit:

$$R_N = \frac{-1}{k_p\left(V_{DD} - V_A\right)} \tag{1.4}$$

Here: $K_n = \frac{m_n C_{ox}}{2}\left(\frac{W}{L}\right)_n, K_p = \frac{m_p C_{ox}}{2}\left(\frac{W}{L}\right)_p$ (1.5)

The complete circuit diagram of the OTA with the NRL is shown below:

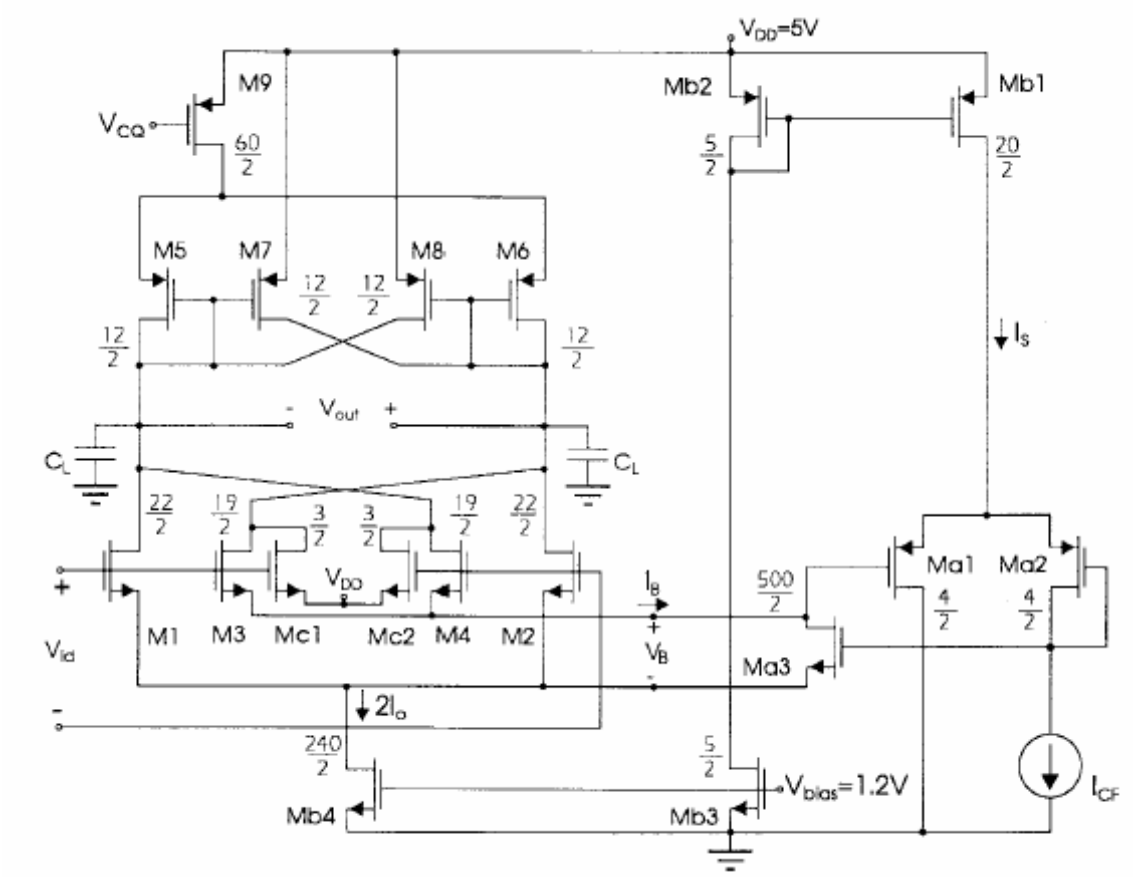


Fig 3 Complete circuit diagram of the CMOS OTA with the NRL.

1.3. Transconductor design

1.3.1. Introduction

CMOS transconductor is a useful building block for the design of Analog and mixed

signal integrated circuit systems, particularly for the design of continuous-time Gm-C filters. Over the pass few years, a few CMOS transconductor designs have been reported for high-frequency continuous-time signal processing applications. [5]-[8]

In this thesis, a new structure with some specific merits to realize the low voltage CMOS VHF transconductor is proposed. The 0.35μm CMOS BSIM3v3 model is used in Cadence simulation, DC analysis shows that the linear V-I conversion of the transconductor can be achieved with a high common mode rejection and a large linear differential mode input voltage range of $\pm$ 0.9*V*. Also, the small signal frequency analysis shows that a very high frequency bandwidth is achieved and with good agreement with the Cadence simulation. An auxiliary circuit is added to the design to control the output DC voltage level. Finally, the Cadence simulation results of the transconductor and a 3rd order elliptic low pass *Gm-C* filter is presented.

1.3.2. DC Analysis of the Transconductor

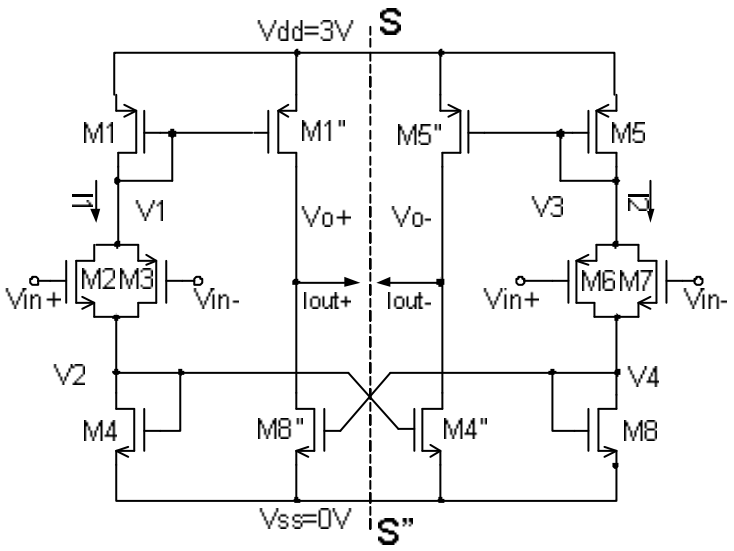


Fig 4 The proposed transconductor circuit.

The transconductor circuit is shown in Fig 4. The idea is to create a circuit structure with minimum number of internal nodes so that the circuit structure is suitable for high frequency operation. In addition, the circuit should have a high common mode input rejection. The circuit structure in Fig 4 is reflection symmetric about the SS' line. When the differential mode input V_{id} = 0 with only the common mode input V_{cm} is applied, the input does not change the circuit symmetry. If all current mirrors are ideal with unity current reflection, it is clear from Fig 4 that the output current $I_{out+} = I_{out-} = 0$. The circuit inherently has a good common mode rejection. Actually, checking the input at transistors M_2 and M_3, when V_{cm} is increased, the increased current through M_2 compensates the decreased current through M_3 and therefore their current summation, I_1 changes little. However, if the differential mode input V_{id} is increased, both currents through M_2 and M_3 increase and therefore their sum I_1 changes significantly. On the other hand, the differential mode input V_{id} destroys the symmetry of the circuit about the SS' line and leads to the current sum I_2 also changes significantly in the opposite sign of I_1. Therefore $I_{out+} = - I_{out-}$, and the output current $I_{out} = I_{out+} - I_{out-}$ is increased.

Detailed analysis shows that I_{out} changes almost linearly with V_{id} with a transconductance coefficient almost independent of V_{cm} within a certain range. This is analyzed as follows where the long channel CMOS device I-V equations for the saturation mode operation are used [9] as a first approximation:

For nMOS transistors:

$$I_{ds} = K_n (V_{gs} - V_{tn})^2 \qquad (1.6)$$

$$K_n = \frac{m_n C_{ox}}{2}\left(\frac{W}{L}\right)_n \tag{1.7}$$

and for pMOS transistors:

$$I_{sd} = K_p (V_{sg} - V_{tp})^2 \tag{1.8}$$

$$K_p = \frac{m_p C_{ox}}{2}\left(\frac{W}{L}\right)_p \tag{1.9}$$

where V_{tn} and V_{tp} are the *absolute value* of the nMOS and pMOS transistor threshold voltages respectively. Adjusting the *W/L* ratio of the nMOS and pMOS transistors to fit the following relationship:

$$K_n = K_p = \frac{m_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right)_{n,p} = K \tag{1.10}$$

or $W_p / W_n = m_n / m_p$ (1.11)

Re-writing (1.6) (1.8) using normalized drain current:

$$I_i = (I_{sd} / K)_i \tag{1.12}$$

For drain current of M_1, we have:

$$I_1 = (V_{dd} - V_1 - V_{tp})^2 \tag{1.13}$$

for the sum of the drain currents of M_2 and M_3, we have:

$$I_1 = \left(V_{cm} + \frac{V_{id}}{2} - V_2 - V_{tn}\right)^2 + \left(V_1 - V_{cm} + \frac{V_{id}}{2} - V_{tp}\right)^2 \tag{1.14}$$

for the drain current of M_4, we have:

$$I_1 = (V_2 - V_{ss} - V_{tn})^2 \tag{1.15}$$

Similarly for M_5, M_6, M_7 and M_8, we have:

$$I_2 = (V_{dd} - V_3 - V_{tp})^2 \tag{1.16}$$

$$I_2 = \left(V_{cm} - \frac{V_{id}}{2} - V_4 - V_{tn}\right)^2 + \left(V_3 - V_{cm} - \frac{V_{id}}{2} - V_{tp}\right)^2 \tag{1.17}$$

$$I_2 = (V_4 - V_{ss} - V_{tn})^2 \tag{1.18}$$

From (1.13) to (1.18), we obtain the following result:

$$I_{1,2} = \left(\frac{-2V_{tp} - 2V_{tn} - V_{ss} + V_{dd} \pm V_{id} - \sqrt{2 \cdot (2V_{cm} \pm V_{id} - 4V_{tn} - 2V_{ss})(-2V_{cm} \pm V_{id} - 4V_{tp} + 2V_{dd})}}{2} \right)^2 \tag{1.19}$$

Each current mirror in Fig 4 has a pair of identical transistors. We can easily obtain:

$$I_{out+} = -I_{out-} = I_1 - I_2 \tag{1.20}$$

and: $$I_{out} = I_{out+} - I_{out-} = 2(I_1 - I_2) \tag{1.21}$$

giving 0.35μm CMOS technology typical values to V_{tn} and V_{tp} and substituting $V_{dd} = 3V$, $V_{ss} = 0V$ into (1.19) (1.20), we obtain the following Taylor expansion of I_{out}:

$$I_{out} = A \cdot V_{id} + B \cdot V_{id}^{\ 3} + O(V_{id}^{\ 5}) \tag{1.22}$$

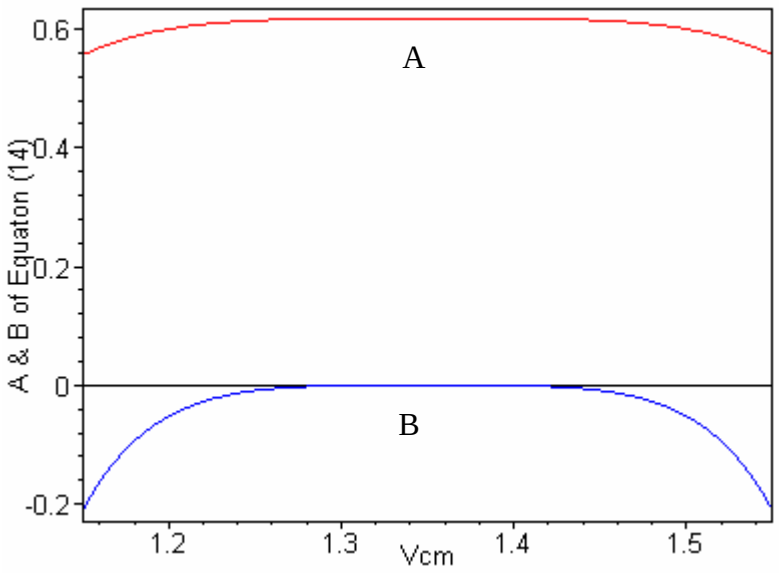


Fig 5 A in (1.22) is almost constant versus Vcm for Vcm from 1.2V to 1.5V. B in (1.22) is much smaller than A (less than 0.1) in this Vcm range. Vcm-ground= (1.2+1.5)/2=1.35V is designated as " common mode ground voltage" .

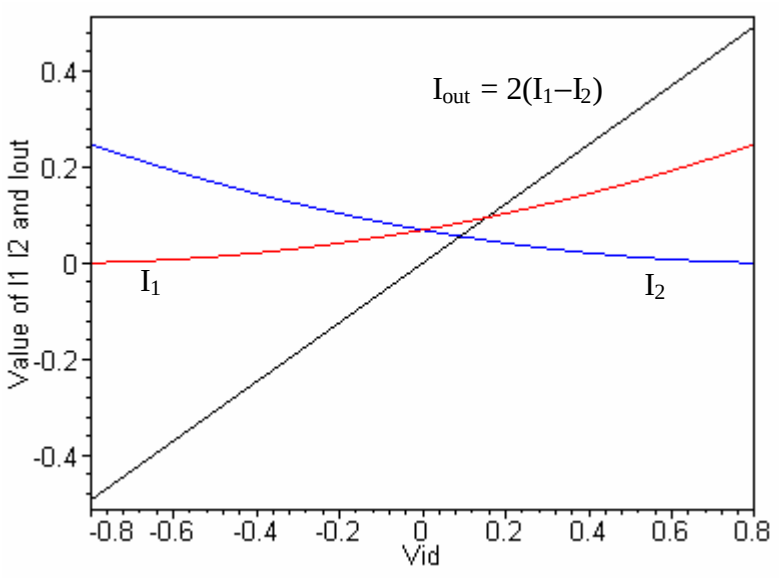


Fig 6 I1, I2 and Iout = 2(I1-I2) versus Vid (Vcm =Vcm-ground).

Both *A* and *B* in (1.22) are functions of V_{cm} as plotted in Fig 5 The analytical expressions of *A* and *B* in (1.22) can be found in the Appendix. As indicated in Fig 5, the transconductance value *A* is almost a constant within the V_{cm} range:

$$1.2V < V_{cm} < 1.5V \qquad (1.23)$$

and B is very close to 0 in this range. From (1.23), we designate (1.2+1.5)/2 =1.35V as the *"common mode ground voltage"* $V_{cm\text{-}ground}$. In the system design, a common mode feedback control is used to force the output common mode voltage approaching 1.35V.

In the above analysis, all MOS transistors in Fig 4 operate in the saturation region and strong inversion. The following conditions must be satisfied by the input MOS transistors M_2, M_3 and M_6, M_7:

for M_2:

$$(V_{ss} + V_{tn}) + V_{tn} \le V_{in+} \le (V_{dd} - V_{tp}) + V_{tn} \tag{1.24}$$

$$\therefore 0.94V \le V_{in+} \le 2.85V \tag{1.25}$$

for M_3:

$$(V_{ss} + V_{tn}) - V_{tp} \le V_{in-} \le (V_{dd} - V_{tp}) - V_{tp} \tag{1.26}$$

$$\therefore -0.15V \le V_{in-} \le 1.77V \tag{1.27}$$

similarly, for M_6 and M_7:

$$-0.15V \le V_{in+} \le 1.77V\ , 0.94V \le V_{in-} \le 2.85V \tag{1.28}$$

combining (1.25)-(1.28), we obtain :

$$0.94V \le V_{in\pm} \le 1.77V \tag{1.29}$$

(1.29) is another constraint condition for the input signal. Since $V_{cm\text{-}ground}$ = 1.35V is

almost at the middle of the range defined in (1.29), when the common mode voltage is at $V_{cm\text{-}ground}$, the differential mode input will have a maximum AC input range. Fig 6 is the plot for (1.19)-(1.21) which shows an almost linear output current I_{out} versus the input differential voltage V_{id} while the input common mode voltage is kept on $V_{cm-ground}$. In the system design, a common mode feedback control is used to force the common mode voltage V_{cm} approaching 1.35V.

Although the above analysis based on (1.6) (1.8) neglected the following effects: the finite output impedance [9], body effect of input nMOS's [9] and short channel effects [10], the overall specification is predicted fairly well compared with more accurate Cadence simulation result shown in Fig 7.

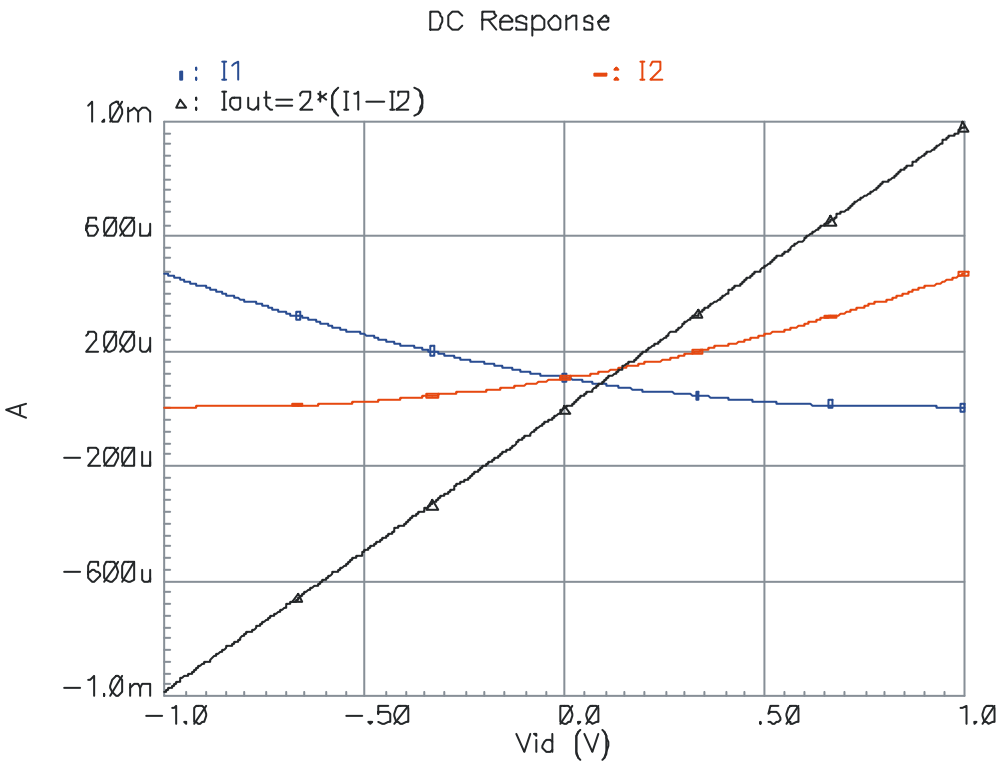


Fig 7 Simulation result of the proposed transconductor using 0.35*μm* BSIM3v3 model

1.3.3. Small Signal AC Analysis of the Transconductor

In the AC analysis of the transconductor circuit, the following approximations are used:

The small signal equivalent circuits as shown in Fig 8 are used for all MOS transistors.

Using the same scaling factor to characterize the parasitic capacitances of nMOS and pMOS transistors. Or $C_i = a_i W$. W is the channel width (while the channel lengths of all transistors are the same). The index i specifies C_{gs}, or C_{gd} or C_{ds}. Therefore, according to (1.11), C_{gs} (or C_{gd}, C_{ds}) of pMOS transistor is $m_n / m_p \approx 3$ times as that of nMOS transistor.

According to (1.6) (1.8), the transconductance of the transistor is $G_m = \sqrt{2K \cdot W \cdot I_{ds} / L}$. When the common mode input voltage is at $V_{cm\text{-}ground}$, the currents through M_2 and M_3 (M_6 and M_7) are nearly equal and are half of the current through M_1 (or M_4), so the G_m of M_2 and M_3 (M_6 and M_7) is $1/\sqrt{2}$ times the G_m of M_1 and M_4 (M_5 and M_8).

For nMOS transistors and pMOS transistors, the output resistance is $R = V_E L / I_{DSsat}$ [9] and it roughly neglects the difference of Early voltage per unit-channel length V_E between the nMOS and pMOS transistors. This approximation is very crude. However, the effect of R in the frequency response is almost negligible as is explained in the appendix, so the approximation is acceptable and will simplify the analytic equations.

The output voltage is clamped to a constant voltage level when simulating the V-I response. In other word, it is grounded during the small signal analysis. Otherwise the output node will introduce more poles or zeros depending on the load condition and cause

the mathematical analysis to be too complex.

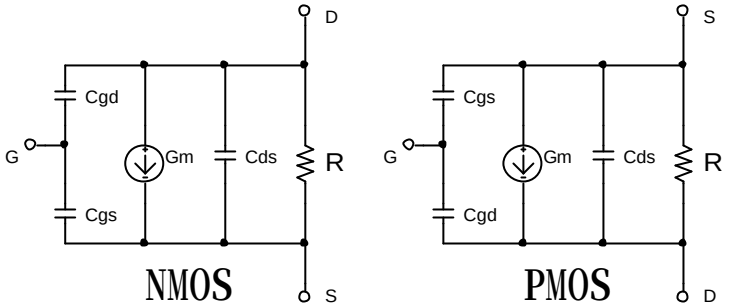


Fig 8 nMOS and pMOS transistors small signal equivalent circuits.

Under these approximations, the small signal equivalent circuit of the g_m-Cell is shown in Fig 9

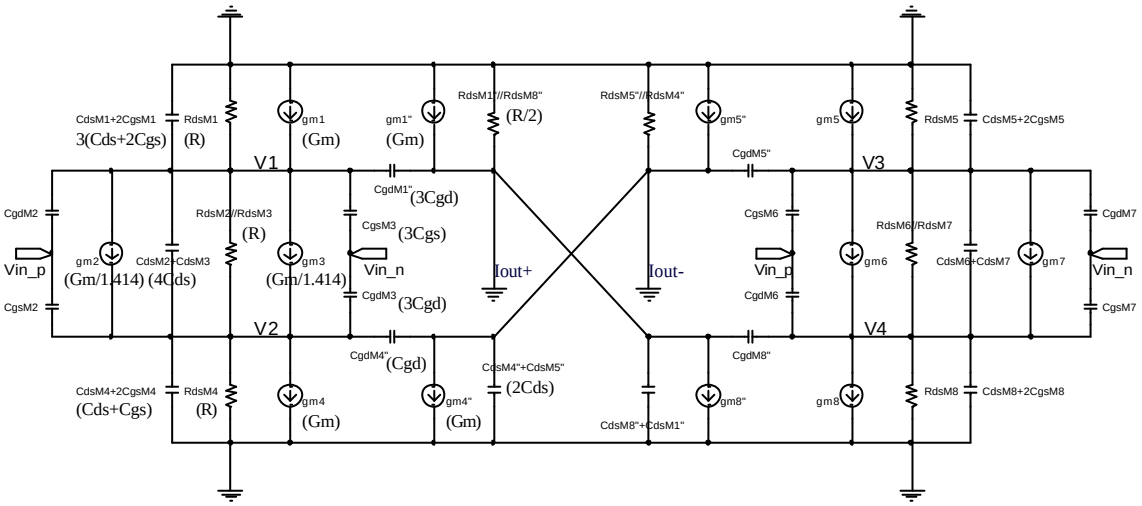


Fig 9 Small signal equivalent circuit of the proposed transconductor cell.

Using Kirchoff's Current Law (KCL):

At node V_1:

$$-V_1 \cdot s\left(C_{ds}+2C_{gs}\right)-\frac{V_1}{R}-V_1 G_m-3V_1 sC_{gd}+3\left(V_{in\_n}-V_1\right)sC_{gs}-\left(V_1-V_{in\_n}\right)\frac{G_m}{\sqrt{2}}$$
$$-\frac{\left(V_1-V_2\right)}{R}-\left(V_1-V_2\right)s\cdot 4C_{ds}-\left(V_{in\_p}-V_2\right)\frac{G_m}{\sqrt{2}}-\left(V_1-V_{in\_p}\right)sC_{gd}=0 \qquad (1.30)$$

At node V_2:

$$\begin{aligned}&\left(V_{in\_p}-V_2\right)sC_{gs}+\left(V_{in\_p}-V_2\right)\frac{G_m}{\sqrt{2}}+\left(V_1-V_2\right)s\cdot 4C_{ds}+\frac{V_1-V_2}{R}+\left(V_1-V_{in\_n}\right)\frac{G_m}{\sqrt{2}}\\&+\left(V_{in\_n}-V_2\right)s\cdot 3C_{gd}-V_2sC_{gd}-V_2s\left(C_{ds}+2C_{gs}\right)-\frac{V_2}{R}-V_2G_m=0\end{aligned}\quad(1.31)$$

substituting $V_{in\_p}=-V_{in\_n}=V_{id}$ into (1.30) (1.31) and solving these two equations, we obtain :

$$V_1=V_{id}\frac{a_{21}s^2+a_{11}s+a_{01}}{b_{21}s^2+b_{11}s+b_{01}},\ V_2=V_{id}\frac{a_{22}s^2+a_{12}s+a_{02}}{b_{22}s^2+b_{12}s+b_{02}}\quad(1.32)$$

the expression for parameters a_{ij} and b_{ij} can be found in the Appendix B. Since the g_m-Cell structure is reflection symmetric about line SS', therefore:

$$\therefore V_4=V_2\big|_{V_{id}\Rightarrow -V_{id}}=-V_{id}\frac{a_{22}s^2+a_{12}s+a_{02}}{b_{22}s^2+b_{12}s+b_{02}}\quad(1.33)$$

the output current:

$$I_{out}=I_{out+}-I_{out-}=2I_{out+}=2\cdot\left(V_1sC_{gd}-V_1G_m+V_4sC_{gd}-V_4G_m\right)(1.34)$$

$$I_{out}=K\frac{(s+z_1)(s+z_2)(s+z_3)}{(s+p_1)(s+p_2)}\cdot V_{id}\quad(1.35)$$

substituting the typical values of the following parameters into (1.35):

$$C_{gd}=2\times10^{-15}F\ ,C_{gs}=11\times10^{-15}F\ ,C_{ds}=18\times10^{-18}F\ ,$$

$$G_m=400\times10^{-6}\ A/V\ ,R=180\times10^{3}\Omega\quad(1.36)$$

after some approximation and simplification, we obtain the expression of the two poles

as:

$$p_{1,2} \approx -\frac{\left(10C_{gs}+6.8C_{gd} \pm \sqrt{40{C_{gs}}^2+24C_{gd}C_{gs}+8{C_{gd}}^2}\right)\cdot G_m}{\left(4C_{gd}+9C_{gs}\right)\left(4C_{gd}+3C_{gs}\right)} \quad (1.37)$$

On the other hand, the zeros can be derided by solving the following equations:

$$\begin{aligned} &2RC_{gd}\left(C_{gd}C_{gs}+9C_{gs}^2-6C_{gd}^2\right)s^3+ \\ &\left\{\left[26.14G_mR+7\right]C_{gd}C_{gs}+\left[17.73G_mR-1\right]C_{gd}^2-9G_mRC_{gs}^2\right\}s^2+ \\ &0.62\left[\left(-3.24-17G_mR\right)C_{gs}+\left(7.83-1.34G_mR\right)C_{gd}\right]G_ms- \\ &\sqrt{2}G_m^2\left(G_mR-1\right)=0 \end{aligned} \quad (1.38)$$

Thus, we obtain:

$$K \approx -4.0\times10^{-15} \quad (1.39)$$

$$p_1 \approx -0.49\times10^{10},\ p_2 \approx -1.8\times10^{10} \quad (1.40)$$

$$z_1 \approx -0.50\times10^{10},\ \ z_2 \approx -4.5\times10^{10},\ \ z_3 \approx 9.1\times10^{10} \quad (1.41)$$

and their relationship:

$$\left|p_1\right| \cong \left|z_1\right| < \left|p_2\right| < \left|z_2\right| < \left|z_3\right| \quad (1.42)$$

here pole p_1 and zero z_1 is very closed together and can roughly be cancelled each other. Substituting the typical parameters value above, we obtain the numerical expression of I_{out}:

$$I_{out} = -4.0\times10^{-15}\times\frac{\left(s+4.5\times10^{10}\right)\left(s-9.1\times10^{10}\right)}{s+1.8\times10^{10}}\cdot V_{id} \quad (1.43)$$

The Bode plot of transfer function in (1.43) is shown in Fig 10 It shows a large -3dB bandwidth of 2.9GHz ($1.8\times10^{10}/2p \approx 2.9GHz$). It is in good agreement with the SpectreS simulation result in Fig 13.

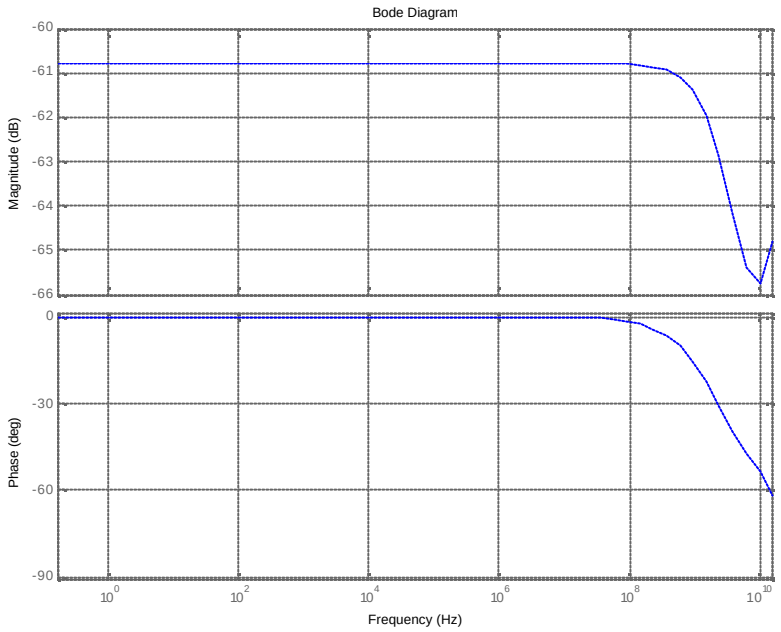


Fig 10 Bode plot of Iout versus frequency using (1.43). It exhibits only one pole and two zeros in the whole frequency range.

1.3.4. Output Common Mode DC Level Stability

The output common voltage in Fig 4 may not be at the desired level Vcm-ground and is sensitive to process variations. Therefore, an auxiliary circuit is used to control the output common mode dc level as shown in the right half circuit of Fig 11.

The circuit consists of N1-N4, N1", N8" is a copy of half of the transconductor circuit M1-M4, M1", M8". N5-N9 is an auxiliary differential amplifier with the input of N8 connected to the desired common mode voltage Vcm-ground and the input of N7 connected to the output Vsample (the drain of N1" and N8"). N10 is parallel to N8" and is

controlled by the output Vo of the auxiliary amplifier which creates a negative feedback ensuring Vsample equals to Vcm-ground. M11, M12 are the replica of N10 and are parallel to M8" and M4" respectively. This ensures that the output Vo+ and Vo- equal to Vcm-ground while the input of the transconductor is also set to Vcm-ground. One of the merits of this auxiliary circuit is that it does not introduce any additional internal node into the signal path, and thus will not affect the frequency response of the transconductor. On the other hand, this output dc voltage control scheme is not sensitive to the device parameter variation as has been verified by the SpectreS simulation.

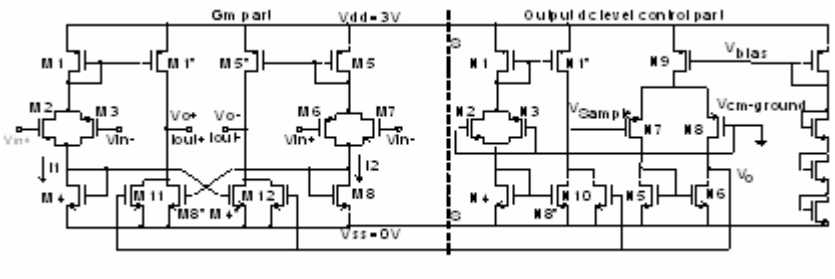


Fig 11 A complete schematic of the proposed transconductor. W/L (M1, M1" , M5, M5" , M3, M6, N1, N1" , N3) = 34.7µm/0.3µm; W/L (M2, M4, M7, M8, M11, M12, M4" , M8" , N2, N4, N10, N8") = 10µm/0.3µm.

1.3.5. SpectreS Simulation Results

The following are the simulation results using SpectreS BSIM3v3 model with the device parameters using 0.35*µm* CMOS technology. The extracted device parameters are around the same as in (1.36).

Fig 12 shows the simulation of Iout versus Vid. The linear V-I conversion characteristic highlights the validity of the theoretical analysis. The transconductance can be tuned by means of the power supply voltage *Vdd*. Though it's not easy for implementation, this

tuning method is applied by some designs [5][8].

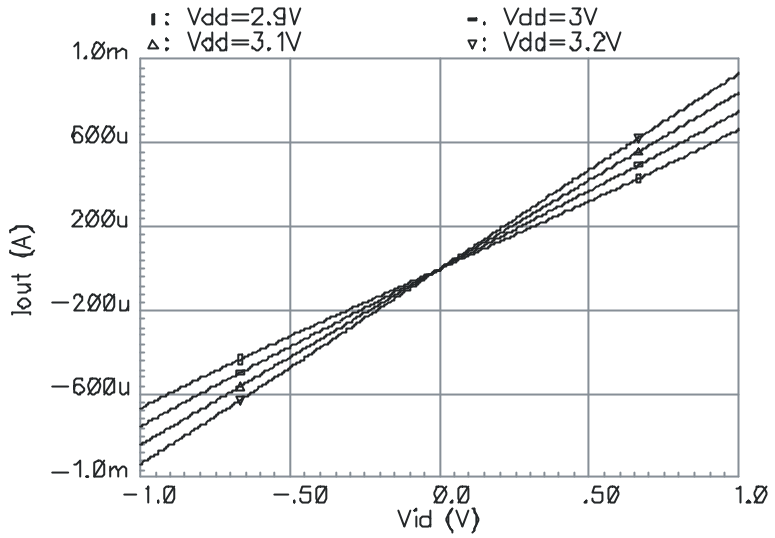


Fig 12 SpectreS simulation of Iout, versus Vid of the transconductor. The gm can be tuned by changing the power supply.

The frequency response of the gm-Cell is shown in Fig 13. A -3dB bandwidth of more than 1GHz is obtained because of the simplicity of the circuit structure, and it is in good agreement with the analytical result obtained in Fig 10.

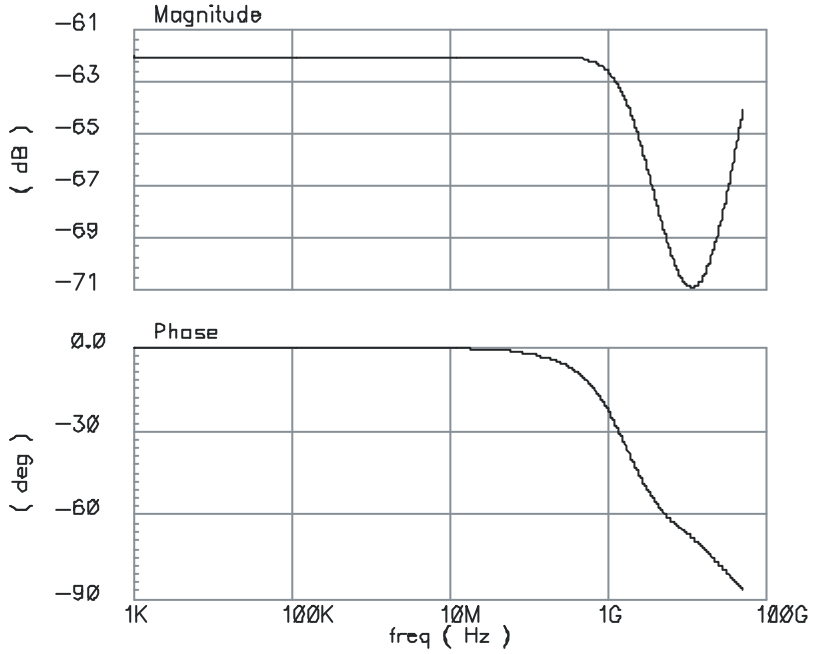


Fig 13 Frequency response of the gm-Cell.

Most of the previous analyses are based on the premise that the nMOS and pMOS are matched by (1.10). Since the ratio kn/kp of the transconductance parameters for nMOS(kn) and pMOS (kp) can vary within a range larger than 10% [12], an inspection of the performance of the proposed gm-Cell due to nMOS and pMOS mismatch is given. In Fig 14, the channel width of pMOSs (Wp) in the gm-Cell changes from 30μm to 40μm, which represents the variation of parameter values during process. If the pMOS is designed with a 34.7μm channel width, the THD of the gm-Cell will be at its best value – less than –70dB (0.032%). If a tolerance of ± 10% is introduced (20% variation, Wp varies from 31.3μm to 38.1μm), Fig 14 indicates that even in this worse case, the THD can be achieved less than –48dB (0.4%). Normally, if the variation range is narrow to ± 5%, the THD will be less than –54dB.

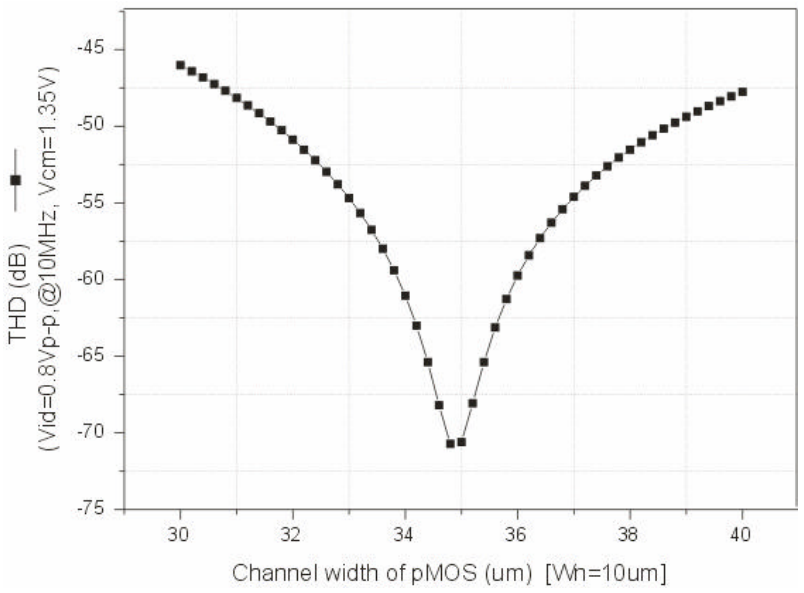


Fig 14 Change of THD of the transconductor circuit, when channel width of pMOSs (Wp) in the gm-Cell is changing while the channel width of nMOS (Wn) is a constant of 10μm, which represents the mismatch of parameters during process.

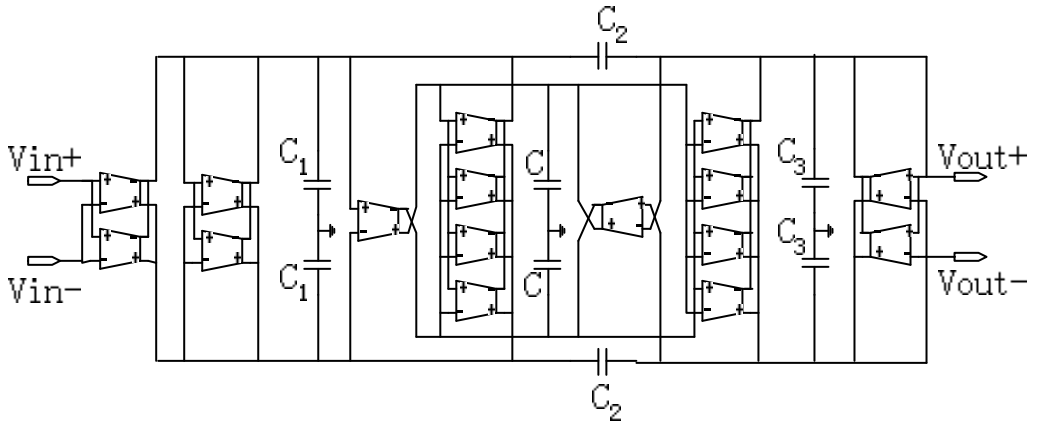
The achieved specification of the transconductor is listed in Table 2:

Supply voltage V_{dd} and V_{ss}	3V and 0V
Linear input voltage range	- 0.9V<V_{id}<0.9V
THD(V_{id}=0.8 V_{p-p},@10MHz, Vcm=1.35V)	- 54dB
- 3dB Bandwidth	>1GHz
CMOS Technology	0.35µm
Power consumption	<0.8mW

Table 2 Specification of the transconductor.

1.3.6. Gm-C Filter Application

Fig 15 is an active implementation of 3rd order elliptic low-pass filter using the proposed transconductor. This filter is derived from a passive ladder filter since ladder filters have good sensitivity and dynamic range properties. The normalized passive prototype filter [11] is given in Fig 16. Using the gyrator approach, both resistors and inductors are replaced by the proposed transconductor element. The simulation result together with the theoretical frequency response of this kind of filter is shown in Fig 17. A cutoff frequency of 150MHz is obtained, using the proposed gm-Cell.



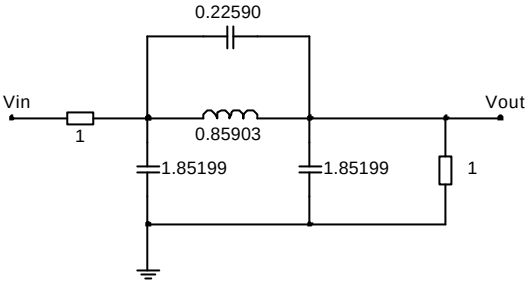


Fig 16 3rd order elliptic low-pass LC ladder filter.

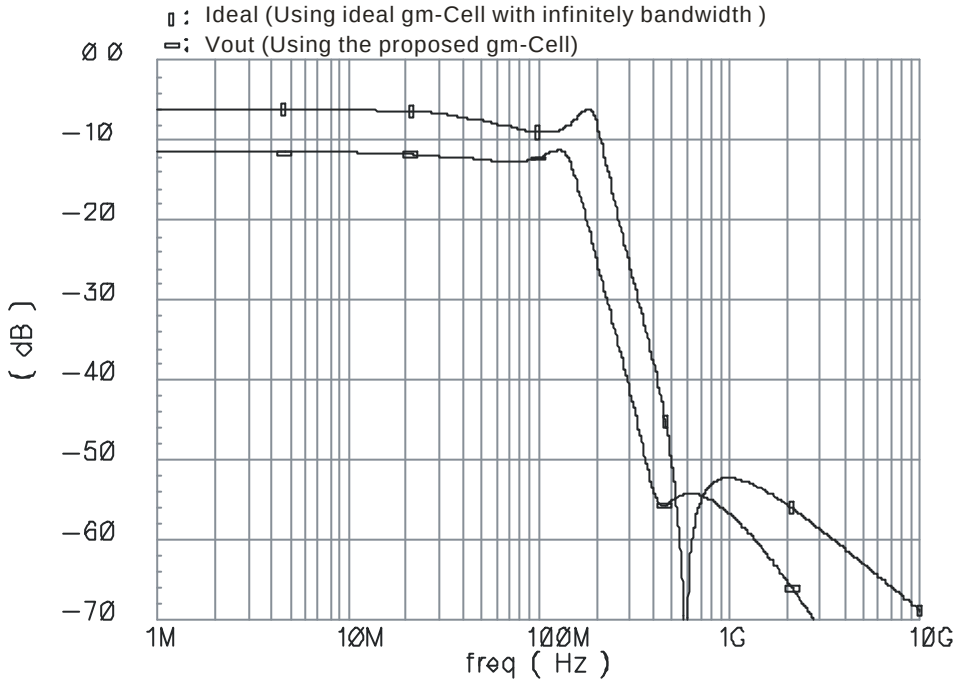


Fig 17 Simulation result of the filter. A cutoff frequency of 150MHz is obtained.

1.3.7. Conclusion

A new high frequency low voltage transconductor circuit which is suitable for VHF gm-C filter application is proposed. The transconductor inherently has a good common mode rejection ability and very high cutoff frequency. Using 0.35？m CMOS technology with 3V power supply, the transconductor has a ±0.9V linear differential input range with a —54dB total harmonic distortion (THD) and greater than 1GHz bandwidth. The

transconductor used in a 3rd order elliptic low-pass gm-C filter with a cutoff frequency of 150MHz is also demonstrated.

2. PROJECT II: CMOS FULLY INTEGRATED LNA DESIGN [3]

2.1. Introduction

The area of radio frequency (RF) circuit design is currently driven in particular by the recent, and largely unanticipated, explosive growth in wireless telecommunications. The RF and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones (as shown in Fig 18 [13]), cable modems, and RF identification tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. Semiconductor and system companies, small and large, analog and digital, have seen the statistics and are striving to capture their own market share by introducing various RF products.

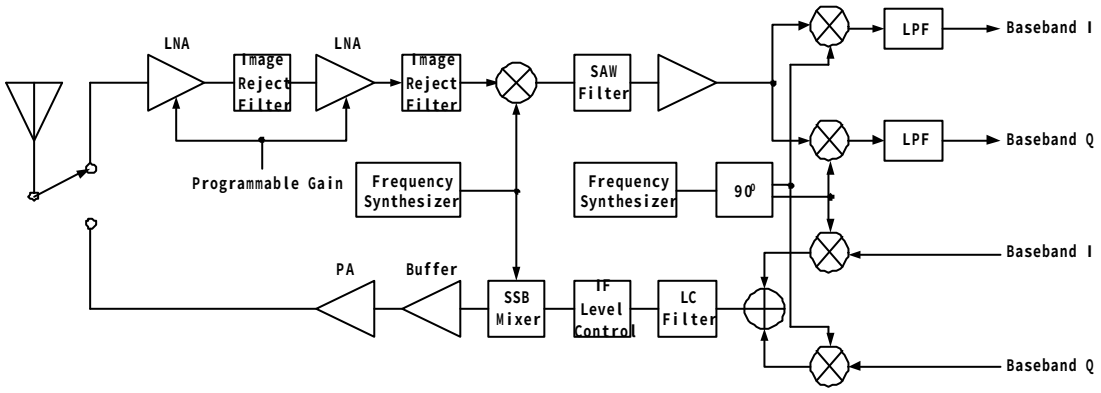


Fig 18 RF section of a cell phone.

The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as a mixer). Aside from providing this gain while adding as little noise as possible, an LNA

should accommodate large signals without distortion, and frequently must also present specific impedance, such as 50O, to the input source. This last consideration is particularly important if a passive filter precedes the LNA, since the transfer characteristics of many filters are quite sensitive to the quality of the termination.

The main purpose to design a LNA here is to:

Gain a deeper insight into the RFIC design;

Check the accuracy of the RF model of the components;

After a long time of stress, analyze the degradation of the performance of a single transistor and the LNA.

This LNA design, together with the reliability test structure in the following section, have been fabricated using CSM 0.18*μm* process.

2.2. LNA Design

2.2.1. Introduction:

The first stage of a RF front-end is typically an LNA, whose main function is to provide enough gain to overcome the noise of subsequent stages. There are many LNA designs being published so far; most of them used the off-chip network [15] or bond wire inductor [18] to accomplish the matching. In this project, in order to provide a deeper understanding to and facilitate the subsequent research in RFIC design, a fully integrated CMOS LNA without off-chip matching network is fabricated and analyzed. The target

specification is listed in Table 3.

Frequency	2.4 GHz
Power supply	1.0 V
Power Dissipation	< 20.0 mW
NF (dB)	< 5 dB
VSWR	< 1.5
Forward Gain	≈ 20.0 dB

Table 3 Target specification of the proposed LNA design.

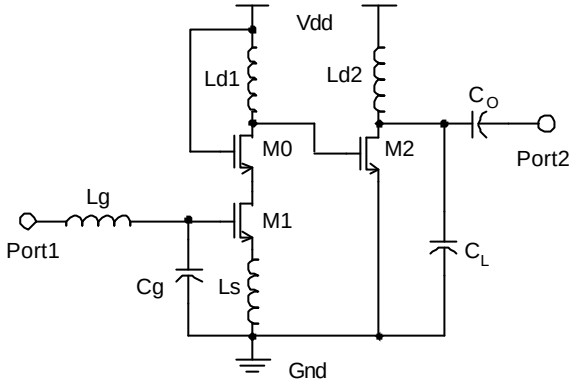


Fig 19 LNA Diagram.

The proposed LNA diagram is shown in Fig 19. We have used extracted RF models for all the components to achieve a "first silicon success". The main difficulty arises from the limited number of spiral inductors for which the extracted models are available. This puts a premium on the careful choice of the inductor to be used. The situation however eases out somewhat with the help of MIM capacitors as the lumped component values of the MIM capacitor RF models are observed to scale with the capacitance value.

2.2.2. Noise Figure Optimization:

For the two stage LNA structure, the input MOSFET of the first stage is the main noise contributor [14] (please refer to the appendices) and its size needs to be optimally chosen

based on noise considerations.

The input matching network is shown in Fig 20 (a) and is simplified into (b) under the assumption that C_g is chosen small enough to avoid the large amount input signal shunt to ground, thus the difference from R_S to R_{eq} or from L_g to L_{eq} is not significant. This leads to the conclusion that the optimum size of M1 in Fig 20 (b) will not vary much from that of M1 in (a).

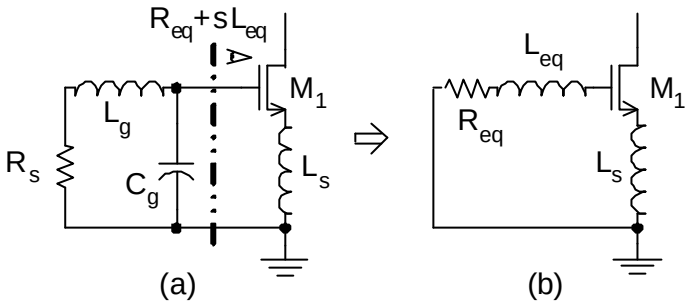


Fig 20 Simplified input structure.

The noise factor of the simplified input structure of Fig 20 (b) is shown in equation (2.1), its detail expression can be found in [15], where P_D is the power dissipation of the input stage; γ is the channel thermal noise coefficient, v_{sat} and e_{sat} are the carrier saturation velocity and electrical field respectively. We can find W, the channel width of M1, as a function of r and P_D as shown in (2.2). If we solve r as an expression of W and P_D (2.3) and substitute it into (2.1), the noise factor can be expressed in (2.4) as a function of W and P_D. The curves of NF versus W under some fixed P_D are shown in Fig 21. By using powerful mathematical software, the complicated derivation of the detail expression of (2.4) is avoided. Parameter values used in (2.4) can be found in the Appendix.

$$NF = 1 + \frac{gw_0 L}{3v_{sat}} P(r, P_D) \text{ here } \quad r \equiv \frac{V_{gs} - V_{TH}}{Le_{sat}} \tag{2.1}$$

$$W = \frac{3(1+r)P_D}{2C_{ox} L w_0 R_{eq} P_0 r^2} = f_W(r, P_D) \tag{2.2}$$

$$\therefore\ r = f_W^{-1}(W, P_D) \tag{2.3}$$

$$NF = 1 + \frac{gw_0 L}{3v_{sat}} P'(W, P_D) \tag{2.4}$$

It is clear from Fig 21 that for every given P_D, there is a corresponding optimum value of W which yields the minimum noise figure. In this LNA design, P_D is specified as $4.5mW$ (the solid line) and the optimum value of W is around $250mm$. The selection of W is a trade-off between the available RF models and the optimum noise figure, thus W of $150\mu m$ is chosen for which the extracted RF models were available. In this W range, the noise figure does not deteriorate significantly..

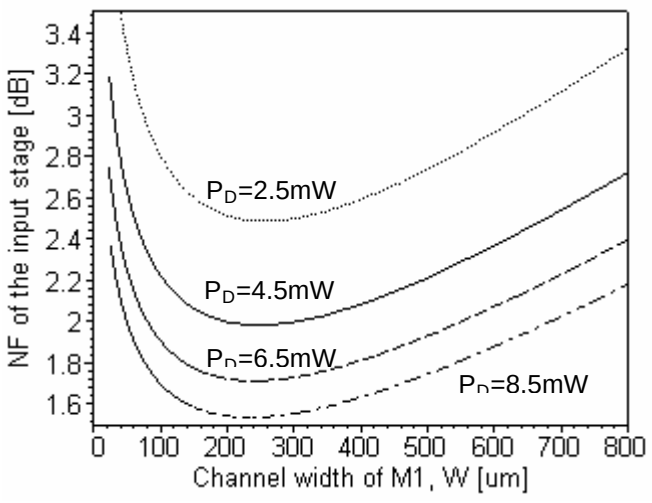


Fig 21 NF vs. *W*.

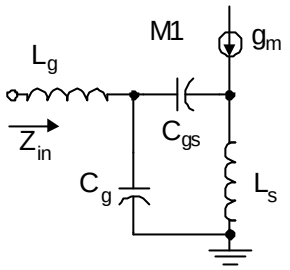


Fig 22 LNA input stage.

The cascode device M0 "shields" M1 from signal variations at its drain and greatly reduces $|S_{12}|$, thus the LNA can be treated approximately as a unilateral design ($|S_{12}|\approx 0$) [17]. In this way M0 reduces the interaction of the tuned output with the tuned input which facilitates the matching task. Channel width of M0 is simply chosen the same size as M1, 150μm, to provide the 4.5mW power dissipation for the input stage.

2.2.3. Input matching:

The input matching network is shown in Fig 22. L_g, L_S and M1 construct a source degeneration stage [16], without C_g, the input impedance is:

$$Z_{in} = \left[sL_g + sL_s + \frac{1}{sC_{gs}} \right] + \frac{g_m}{C_{gs}} L_s \qquad (2.5)$$

L_S is chosen to make the real part of Z_{in} to match the signal source resistance and L_g gets rid of the imaginary part of Z_{in}. But that's not always true while L_S and L_g can not be tuned continuously. In this case, capacitor C_g is connected between the gate of M1 and ground to give another order of freedom of tuning Z_{in} as shown in the approximated expression of (2.6). Note that if C_g is small enough to be neglected, Z_{in} in (2.6) will shrink back to the expression (2.5).

$$Z_{in} \approx \left[sL_g + sL_s \frac{C_{gs}}{\left(C_g + C_{gs}\right)} + \frac{1}{s\left(C_g + C_{gs}\right)} - s \frac{\left(L_s g_m\right)^2 C_g}{\left(C_g + C_{gs}\right)^2} \right] + \frac{g_m C_{gs}}{\left(C_g + C_{gs}\right)^2} L_s \qquad (2.6)$$

2.2.4. Linearity consideration:

One of the advantages of two stage amplifier is that it separates the optimization tasks of noise, linearity performance and input, output matching while, for single stage LNA, they need to be considered simultaneously. In a cascade structure, IP3 of the last stage is the prominent factor of the total IP3 [13][14] (see appendices), thus M2 contributes more to the LNA linearity than M1. IIP3 of M2 can be written as [19]:

$$IIP3_2^2 = \frac{4}{3} \left| \frac{V_{gs2} \left(2 + q V_{gs\,2}\right) \left(1 + q V_{gs\,2}\right)^2}{q} \right| \qquad (2.7)$$

where q is the normal field mobility degradation factor. (2.7) shows that IIP3 of the second stage can be enhanced by increasing V_{gs2}, for this reason the gate of M2 is connected to V_{dd} through L_{d1} to give V_{gs2} the maximum value. However, that increases the power dissipation as well; channel width of M2 needs to be reduced to compensate this problem. Fortunately, reducing the channel width of M2 will not affect the linearity significantly, thus a small device with relatively high V_{gs} is the way we use here to improve linearity of the LNA [14].

2.2.5. Output matching:

Making output matching is more complicated than the input one because the output impedance is very sensitive to the component values. L_{d1} is the load inductor of the first

stage, however it affects the output impedance significantly. As shown in the setup in Fig 23, *Ro* is the output resistance looking into the drain of M2. If the value of L_{d1} is chosen improperly, *Ro* will become negative at the desired resonant frequency and thus introduces the instable factor: $|S_{22}|>1$. We can get a more intuitive view from the simulation result in Fig 24. At the frequency of 2.4GHz, if L_{d1} is given a value of 4nH, *Ro* is negative. In another two cases, when L_{d1} is chosen 1nH or 8nH, Ro becomes positive.

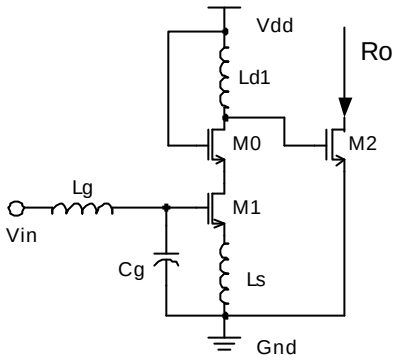


Fig 23 Analysis of the output resistance.

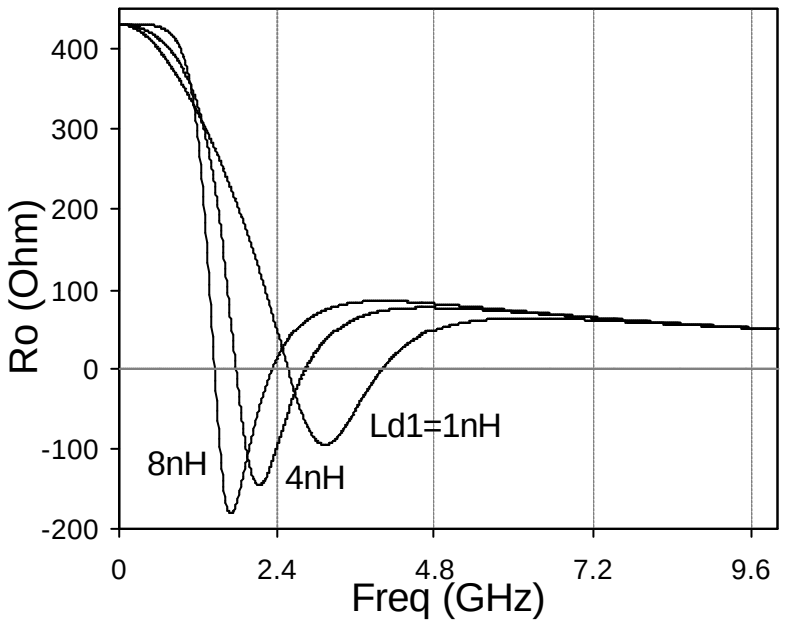


Fig 24 Simulation result of Ro vs. Freq.

To further investigate how L_{d1} affects *Ro*, the small signal analysis of Fig 23 is provided here. The circuit in Fig 23 is simplified to the equivalent circuit in Fig 25. Note that the effect of the input stage (including M0, M1, L_g, L_s and C_g) is neglected for simplicity thanks to the isolation provided by M0. The expression of *Ro* is shown in (2.8):

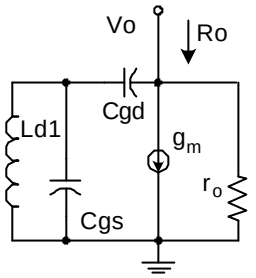


Fig 25 M2 & Ld1.

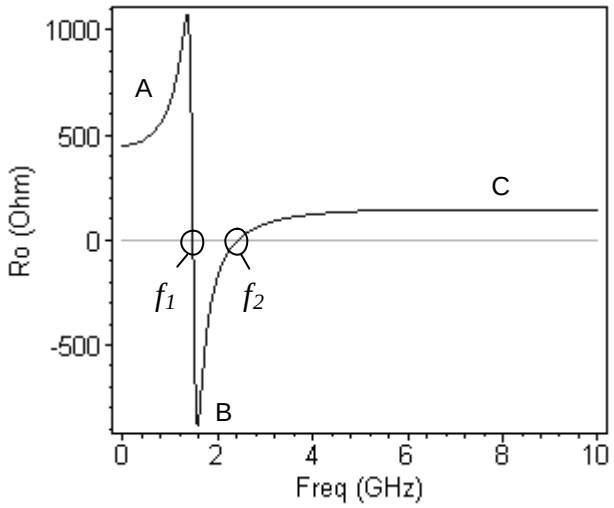


Fig 26 Ro vs. Freq.

$$R_o = \frac{\left[1-(f/f_1)^2\right]\left[1-(f/f_2)^2\right]r_o}{\left[1-(f/f_1)^2\right]^2+\left[1-(f/f_3)^2\right](f/f_4)^2} \approx \frac{1-(f/f_2)^2}{1-(f/f_1)^2}r_o \qquad (2.8)$$

where $f_1 \equiv 1/2p\sqrt{L_{d1}\left(C_{gd}+C_{gs}+C_{gd}g_m r_o\right)}$, $f_2 \equiv 1/2p\sqrt{L_{d1}\left(C_{gd}+C_{gs}\right)}$, $f_3 \equiv 1/2p\sqrt{L_{d1}C_{gs}}$ and $f_4 \equiv 1/2p\, r_o C_{gd}$. The plot of R_o versus frequency is illustrated in Fig 26. The effect of

f_3 is eliminated by f_4 in the frequency range we are considering since f_4 is much higher than 2.4GHz. The frequency axes can be divided by f_1 and f_2 into three regions: A, B and C. B is the undesired region as mentioned before: the negative R_o region. Thus L_{d1} needs to be properly chosen to shift region B to the left side or right side to drop the resonant frequency (2.4GHz) into region A or C. If region A is chosen, L_{d1} should be given a small value (around 1nH according to Fig 24 in this particular design) to ensure f_1>2.4GHz, that will largely reduce the forward power gain. Thus region C {$f > f_2$} is chosen, which requires a relatively large L_{d1} to ensure that R_o is positive at 2.4GHz (2.4GHz > f_2). Note that this is a case-by-case study, in a different process or a different setup of component values, maybe region A is a good option. Again, changing L_{d1} will not change the input matching much due to the isolation created by M0 and its effect can be minimized by finely tuning C_g in the later optimization step.

As illustrated in Fig 27, after L_{d1} is decided, the output impedance is located at point 1. If L_{d2} can be continuously tuned, ideally L_{d2} can be given a value that delivers the output impedance Z_{out} from point 1 to 3, which is the intersection of the line of L_{d2} and 50Ω circle. In this case, the shunt capacitor, C_L, is not necessary for output matching. However, the turns of the spiral inductor is discrete thus L_{d2} should be given a slightly SMALLER value to make room for C_L to tune the point 2 back to 3. But a TOO SMALL L_{d2} will greatly enlarge C_L. That causes a problem which makes L_{d2} becomes a sensitive component for output impedance: the oscillation frequency shown in (2.9) comes close to the resonant frequency (2.4GHz). This problem was overlooked in this LNA design and the effect will be shown in the experimental result later. C_O, the last component undecided, is used to

compensate the imaginary part of the output impedance and isolate the DC path between LNA and its load.

$$f_{osc} = \frac{1}{2p\sqrt{L_{d2}C_L}} \quad \{\approx 2.83GHz\} \tag{2.9}$$

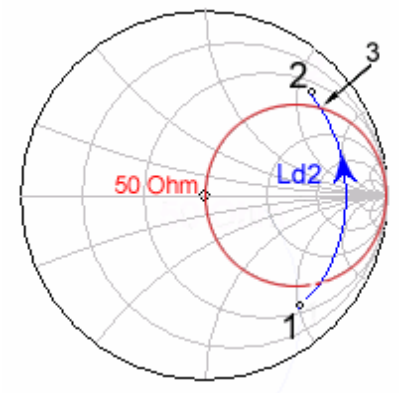


Fig 27 Ld2 selection.

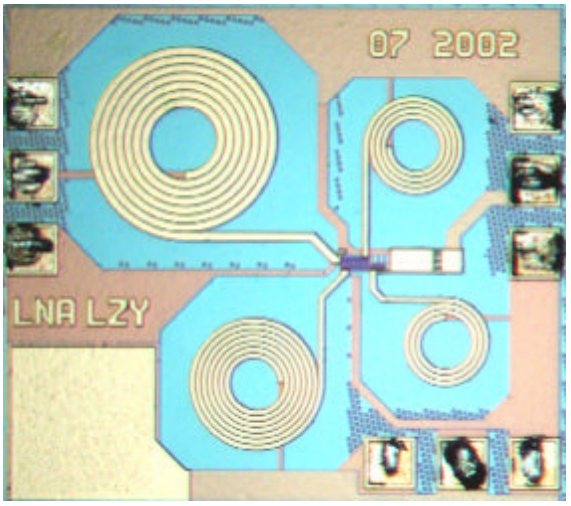


Fig 28 LNA micrograph .

2.3. Experimental Result:

The micrograph of the LNA is shown in Fig 28. This IC is implemented in a 0.18μm six metal process. The chip area is mainly occupied by the four spiral inductor L_g, L_S, L_{d1} and L_{d2}, whose inductance are 13.2nH, 2.6nH, 8.3nH and 1.6nH respectively at 2.4GHz.

Capacitances of the three MIM capacitors C_g, C_L and C_O are $50fF$, $1.9pF$ and $0.9pF$. Channel lengths of all transistors are $0.18\mu m$. S-parameters measurement results are shown in Fig 29. Marker 1 is positioned at 2.4GHz, the desired resonant frequency. Input and output matching are quite good: S_{11} is -16.8dB while S_{22} is -10.2dB. The forward gain (S_{21}) is 23dB and it has a value of more than 20dB from 2.2 to 3.4GHz. The reverse isolation (S_{12}) is less than -50dB at 2.4GHz. A problem occurs as we pay attention to the marker 3. There is an abnormal behavior around 2.8GHz. This is the oscillation caused by C_L and L_{d2} that is explained in section 2. Fig 30 shows that noise figure almost reaches its lowest value, 3.8dB, at 2.4GHz. This measurement result differs from the theoretical value of around 2.1dB in Fig 21, which implies that, if we want a more precise prediction, we need to take into account the noise contribution from the other two NMOS, M0 and M3 and the four spiral inductors whose quality factors are not high enough. Two tones IP3 test (2.4 and 2.41GHz) shows that the IIP3 of this LNA is about -9dBm. All the measurement results are listed in Table 4 and the summary component parameters of the LNA is listed in Table 5.

2.4. Measurement experience:

1. Using the Agilent 8753ES S-Parameter Network Analyzer:

a. Control Panel: “Avg” → IF Bandwidth: change from 3700Hz to 1000Hz;

b. Frequency range: default range 30kHz – 6GHz, I usually change it to 1GHz – 5GHz. It seems that the NWA is not so accurate at the lower and upper end of the frequency range.

c. Choose a proper POWER level: default 0dB. I think the default level is too high for

LNA measurement.

d. Number of point: default 201 points. The larger number you choose, the longer time it will take to measure. But the 8753ES is quite fast, a number of 801 will not take a very long time, however it is not true when you use the ICCAP to do a optimization.

2. Using the probe station:

a. The old probes are purchased from Cascade Com. Their probe tips are too soft and are not very good for testing pads made by Aluminum. Please use the probes made by GGB Industries INC. There are two kinds of GGB probes available in our Lab so far: P-10-5916-C (GSG DC probe for power supply) and 40A-GSG-100-C (GSG RF probe for the frequency range from 0.08GHz to 40GHz).

b. Be very careful when using the probes, they are very fragile. DO NOT move the probe station when the probes are installed.

3. Calibration:

a. A meticulous calibration will greatly improve the accuracy of the measurement result.

b. Before test, doing several times of calibration are recommended. Compare the stability measurement result in the Calibration Kit to find out which calibration set is more reliable.

2.5. Conclusion

The two stages 0.18μm fully integrated CMOS LNA with the input and output matching network is demonstrated here together with its detail analysis and design procedures. We can see that, the performance of the amplifier is sensitive to the component values

especially for the output stage design to which we need to pay more attention.

Frequency	2.4 GHz	S11	−16.8 dB (VSWR≈1.35)
Power supply	1.0 V	S12	−51.7 dB
Power Dissipation	13.0 mW	S21	23.0 dB
(First Stage)	4.5 mW	S22	−10.2 dB (VSWR≈1.9)
NF (dB)	3.8 dB	IIP3	−9.1 dBm

Table 4 LNA performance summary.

Channel length of all transistor	0.18μm
Channel width of M0 and M1	150μm (30 fingers)
Channel width of M2	80μm (16 fingers)
Lg	13.2nH
Ls	2.6nH
Ld1	8.3nH
Ld2	1.6nH
Cg	50fF
CL	1.9pF
CO	0.9pF

Table 5 Component parameters of the proposed LNA

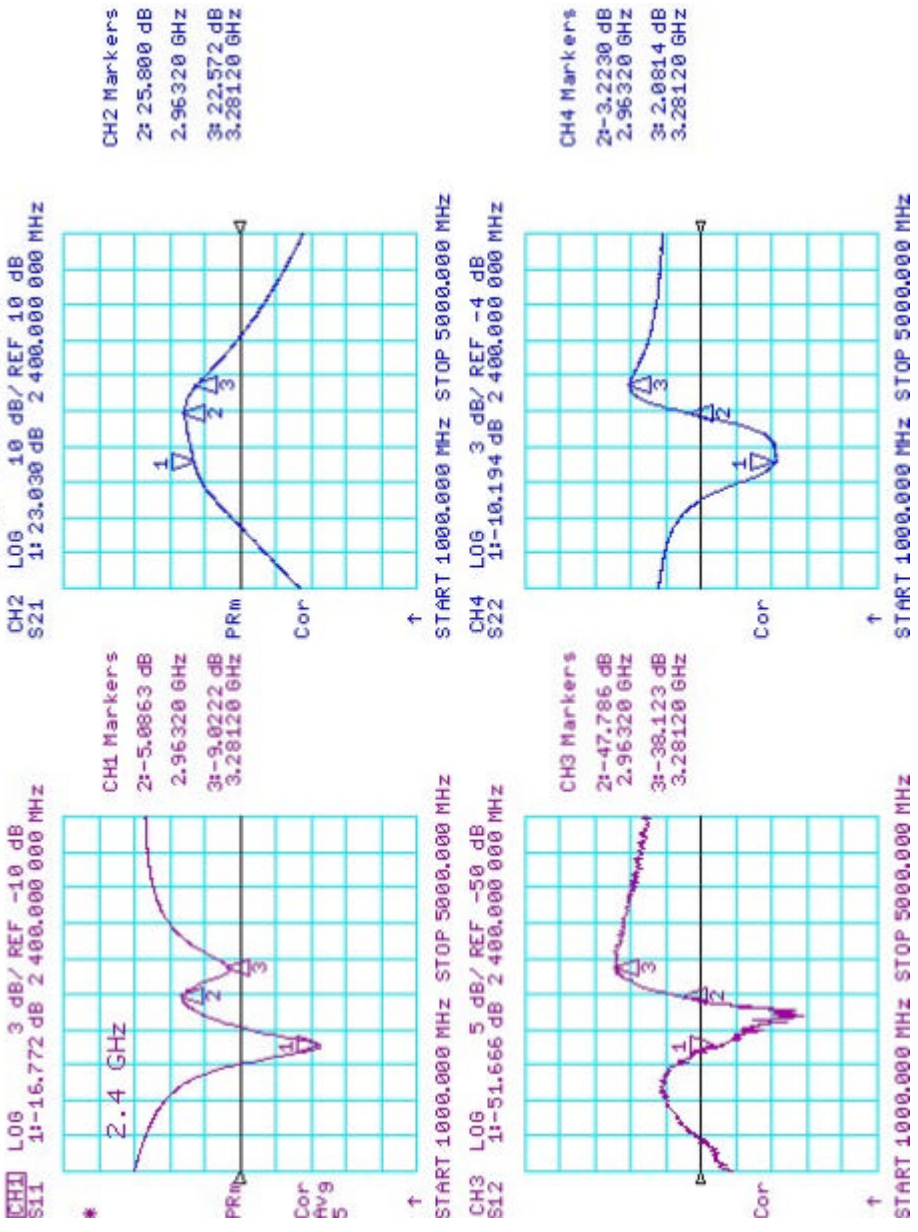


Fig 29 S-parameters of the LNA.

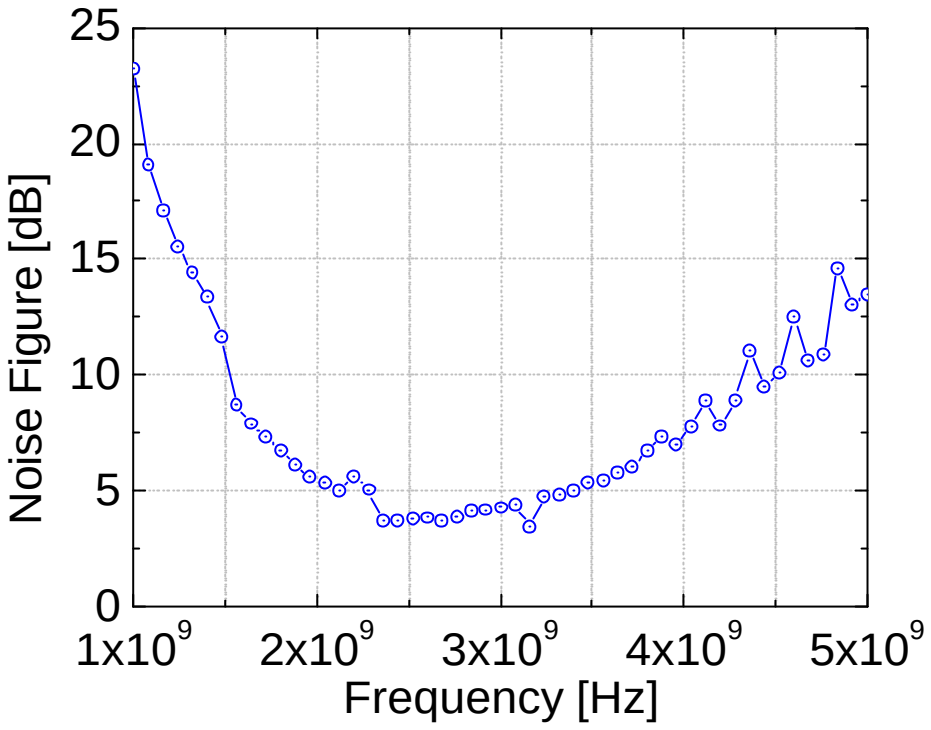


Fig 30 Noise Figure.

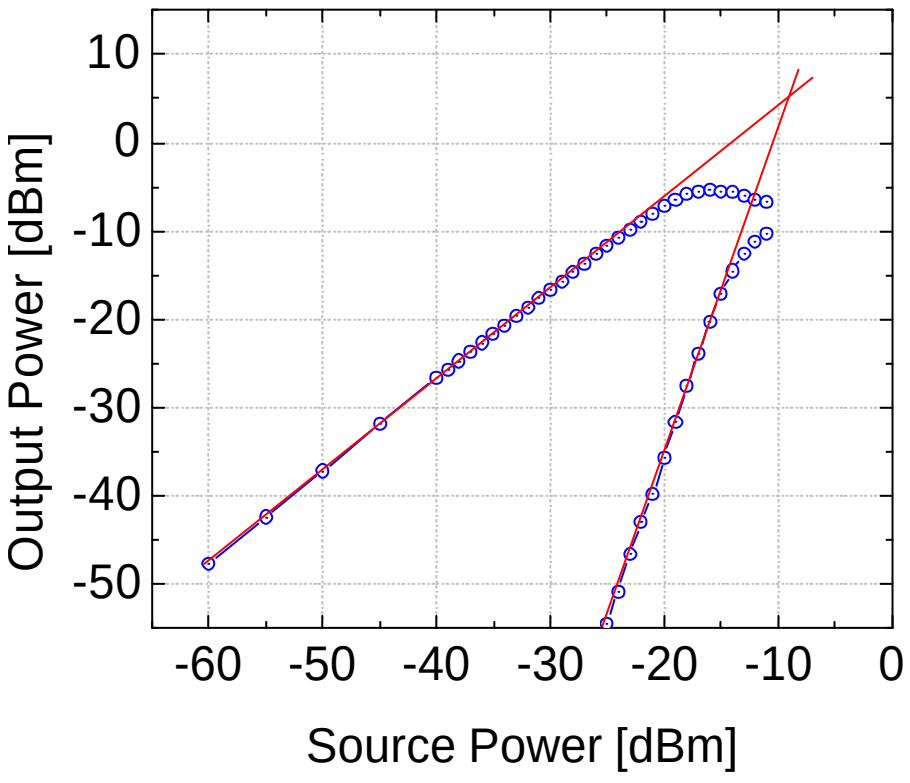


Fig 31 Two tone test.

PUBLICATIONS

Journal:

[1] Luo Zhenying, M.F. Li, Yong Lian and S.C.Rustagi, "New Low Voltage CMOS Transconductor for VHF Filtering Applications" Analog Integrated Circuits and Signal Processing. 37, 233–242, 2003.

Conference:

[2] Luo Zhenying, M.F. Li, Yong Lian and S.C.Rustagi, "MOS Transconductor Design for VHF Filtering Applications" Circuits and Systems, 2003. ISCAS '03, Volume: 1 Page(s): 517 -520

[3] Luo Zhenying, S.C.Rustagi, M.F. Li and Yong Lian, "A 1V, 2.4GHz Fully Integrated LNA using 0.18*μm* CMOS Technology" ASICON2003, Page 1062 - 1065.

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APPENDICES

A. Calculation of the coefficients A and B of I_{out} in (1.22)

From (1.19), we have:

$$I_{1,2}=\left(\frac{-2V_{tp}-2V_{tn}-V_{ss}+V_{dd}\pm V_{id}-\sqrt{2\cdot(2V_{cm}\pm V_{id}-4V_{tn}-2V_{ss})(-2V_{cm}\pm V_{id}-4V_{tp}+2V_{dd})}}{2}\right)^2 \quad (2.10)$$

$$I_{out}=2(I_1-I_2)=A\cdot V_{id}+B\cdot V_{id}{}^3+O(V_{id}{}^5) \quad (2.11)$$

substituting the following values to the parameters:

$V_{tn}=0.466V$, $V_{tp}=0.617V$, $V_{dd}=3V$, $V_{ss}=0V$.

and let:

$t=-(10V_{cm}-9)(5V_{cm}-9)$ and $s=V_{cm}-1.35$.

We can derive the following results:

$$A\approx 0.2\frac{\left(9\sqrt{t}-4t\right)\left(2\sqrt{t}-9\right)}{t} \quad (2.12)$$

$$B\approx -24960\frac{s^4}{t^{5/2}} \quad (2.13)$$

B. Detail expression of a_{ij} and b_{ij} in (1.32) and (1.33)

From the typical parameter value shown in (1.36), we make the following two

approximations:

$G_m R = 400\times10^{-6}\times180\times10^{3} = 72 >> 1;$

$C_{ds} << C_{gs}$ and C_{gd}, so that C_{ds} is neglected all the time during the approximation while comparing to C_{gs} or C_{gd}.

For V_1: $V_1 = R\cdot V_{id}\,\dfrac{a_{21}s^2 + a_{11}s + a_{01}}{b_{21}s^2 + b_{11}s + b_{01}}$ (2.14)

$a_{01} \approx 1.4G_m{}^2 R$ (2.15)

$a_{11} \approx \left(6.1C_{gd} + 8.7C_{gs}\right)G_m R$ (2.16)

$a_{21} \approx \left(-4C_{gd}{}^2 + 9C_{gs}C_{gd} + 9C_{gs}{}^2\right)R$ (2.17)

$b_{01} \approx 2.4G_m{}^2 R^2$ (2.18)

$b_{11} \approx \left(13.7C_{gd} + 20.5C_{gs}\right)G_m R^2$ (2.19)

$b_{21} \approx \left(16C_{gd}{}^2 + 48C_{gs}C_{gd} + 27C_{gs}{}^2\right)R^2$ (2.20)

For V_4: $V_4 = V_2\big|_{V_{id}\Rightarrow -V_{id}} = -R\cdot V_{id}\,\dfrac{a_{22}s^2 + a_{12}s + a_{02}}{b_{22}s^2 + b_{12}s + b_{02}}$ (2.21)

$a_{02} \approx 1.4G_m{}^2 R$ (2.22)

$a_{12} \approx \left(1.2C_{gd} + 12.3C_{gs}\right)G_m R$ (2.23)

$a_{22} \approx \left(-12C_{gd}{}^2 - 23C_{gs}C_{gd} + 9C_{gs}{}^2\right)R$ (2.24)

$b_{02} \approx 2.4G_m{}^2 R^2$ (2.25)

$b_{12} \approx \left(13.7C_{gd} + 20.5C_{gs}\right)G_m R^2$ (2.26)

$b_{22} \approx \left(16C_{gd}{}^2 + 48C_{gs}C_{gd} + 27C_{gs}{}^2\right)R^2$ (2.27)

C. LNA input stage NF & Fixed P_D NF optimization:

There are several noise sources in the LNA input stage:

The main noise contributors: drain and gate current noise i_{dn}, i_{gn} [20];

Signal source (*Rs*), distributed gate resistant (*Rg*) [21];

Losses of *Lg* and *Cg* which are neglected here.

In the following, the calculation of output noise density of the LNA input stage produced by these noise sources are given one by one, and the noise factor is derived finally.

Calculation of the noise from R_g:

Under assumption B. The LNA input stage is simplified From Fig 32 (a) into (b). v_{nRg} is the noise produced from gate resistor of M1.

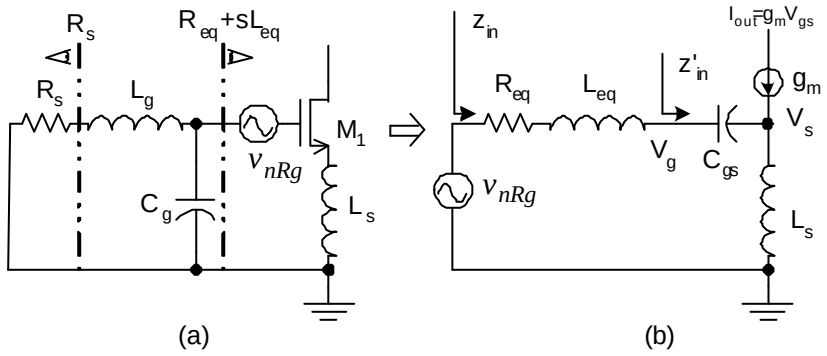


Fig 32 Simplification of the input matching structure.

Define: $w_T = \frac{g_m}{C_{gs}}$ (2.28)

$?_T$ is constant while channel width of M1 (*W*) changes.

$$Z_{in} = \left(\frac{1}{sC_{gs}} + sL_s + sL_{eq} \right) + R_{eq} + w_T L_s \tag{2.29}$$

$$z_{in}^{'} = \frac{1}{sC_{gs}} + sL_s + w_T L_s \tag{2.30}$$

At resonant frequency: $\frac{1}{sC_{gs}} + sL_s + sL_{eq} = 0$ (2.31)

Applying *KCL* at *Vg*: $\left(V_g - V_s\right)\left(g_m + sC_{gs}\right) = \frac{V_s}{sL_s}$ (2.32)

Thus: $V_g = V_s \frac{1/sL_s + g_m + sC_{gs}}{g_m + sC_{gs}}$ (2.33)

The *gm* (v_{nRg} to i_o):

$$G_{nRg} = \frac{i_o}{v_{nRg}} = \left(V_g - V_s\right) g_m \Big/ \left(\frac{Z_{in}}{z_{in}^{'}} V_g \right) \tag{2.34}$$

From (2.31)(2.32)(2.33)(2.34):

$$G_{nRg} = \frac{w_T}{sR_{eq}\left(1 + \frac{w_T L_s}{R_{eq}}\right)} = \frac{w_T}{sR_{eq}\Psi} \tag{2.35}$$

Defining: $\Psi \equiv 1 + w_T L_s / R_{eq}$ (2.36)

Note that: $G_{nR_{eq}} = G_{nR_g} = \frac{w_T}{sR_{eq}\Psi}$ (2.37)

Noise power density from *Rg*:

$$S_{a,R_g}(w_0) = S_{R_g}(w_0)\left|G_{nR_g}\right|^2 = \frac{4kTR_g \cdot w_T^2}{w_0^2 R_{eq}^2 \Psi^2} \tag{2.38}$$

The distributed gate resistance is:

$$R_g = \frac{R\square \cdot W}{12n^2 L}\text{[23]} \tag{2.39}$$

In (2.39): 1/12: Gate finger is contacted at both ends; n: number of fingers; $R\square$: Gate sheet resistance per square.

Calculation of the relationship between i_{odn} and i_{dn}:

In Fig 33, i_{dn} is the drain current noise, one of the main noise contributor. i_{odn} is the output noise current of the LNA input stage produced from i_{dn}.

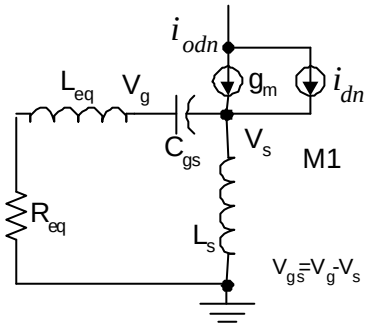


Fig 33 Illustration of drain current noise contribution of M1.

KCL at *Vg*: $\frac{-V_g}{R_{eq} + sL_{eq}} = V_{gs} sC_{gs}$ (2.40)

KCL at *Vs*: $-V_{gs} sC_{gs} + \frac{V_s}{sL_s} = i_{odn}$ (2.41)

$V_{gs} g_m = i_{odn} - i_{dn}$ (2.42)

From (2.28)(2.31)(2.40)--(2.42):

$$i_{odn} = \frac{i_{dn}}{1 + \frac{L_s g_m / C_{gs}}{\left(1/sC_{gs} + sL_s + sL_{eq}\right) + R_{eq}}} = \frac{i_{dn}}{1 + \frac{w_T L_s}{R_{eq}}} \tag{2.43}$$

or $i_{odn} = \frac{i_{dn}}{\Psi}$ (2.44)

The drain current noise power spectral density is: $\overline{i_{dn}^2} = 4kTg\, g_{d0}$ (2.45)

For simplicity, we ignore the difference between $\overline{i_{dn}^2}$ and $\overline{i_{dn}^2}/\Delta f$.

Calculation of the relationship between i_{ogn} and i_{gn}:

In Fig 34, i_{gn} is the gate current noise. It's another main noise contributor. i_{ogn} is the output noise current of the LNA input stage produced from i_{gn}.

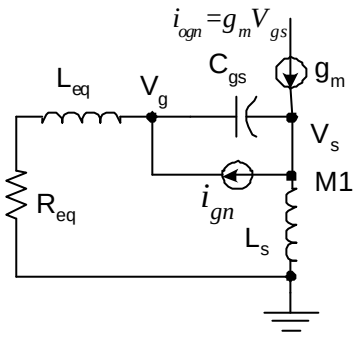


Fig 34 Illustration of gate current noise contribution of M1.

KCL at *Vg*: $-V_{gs}sC_{gs} + i_{gn} - \frac{V_g}{R_{eq} + sL_{eq}} = 0$ (2.46)

KCL at *Vs*: $-V_{gs}sC_{gs} + i_{gn} + \frac{V_s}{sL_s} = i_{ogn}$ (2.47)

and $i_{ogn} = g_m V_{gs}$ (2.48)

From (2.46)--(2.48)(2.28)(2.31)

$$\frac{i_{ogn}}{i_{gn}} = \frac{w_T}{s}\left(1+\frac{s\left(L_{eq}+L_s\right)}{R_{eq}}\right)\Bigg/\left(1+\frac{L_s w_T}{R_{eq}}\right) \tag{2.49}$$

Defining: $Q_L = \dfrac{w_0\left(L_{eq}+L_s\right)}{R_{eq}}$ (2.50)

From (2.36)(2.49)(2.50)

$$i_{ogn} = \frac{w_T}{w_0}\left(-j+Q_L\right)\frac{i_{gn}}{\Psi} \tag{2.51}$$

The gate current noise power spectral density is:

$$\overline{i_{gn}^2} = 4kTd\,g_g \quad [20] \tag{2.52}$$

and $g_g = \dfrac{w^2 C_{gs}^2}{5g_{d0}}$ (2.53)

Calculation of combined effect of drain noise and gate noise to the output noise current: (a) correlated and (b) uncorrelated portion.

The gate noise is partially correlated with the drain noise, with a correlation coefficient of *c*[20]:

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}} \approx 0.395\,j \tag{2.54}$$

Define: $i_{gn} = A\cdot i_{dn} + Z$ (2.55)

Where ($A\times i_{dn}$) is correlated to i_{gn} while *Z* is the uncorrelated portion [20].

Thus: $\overline{i_{gn}^2} = A^2 \cdot \overline{i_{dn}^2} + \overline{Z^2}$ (2.56)

$$\overline{i_{gn}^2} = \overline{i_{gn}^2}\left|c\right|^2 + \overline{i_{gn}^2}\left(1-\left|c\right|^2\right) \quad (2.57)$$

where $\overline{i_{gn}^2}\left|c\right|^2$ is correlated with $\overline{i_{dn}^2}$ and $\overline{i_{gn}^2}\left(1-\left|c\right|^2\right)$ is the uncorrelated portion.

From (2.56)(2.57):

$$A^2 \cdot \overline{i_{dn}^2} = \overline{i_{gn}^2}\left|c\right|^2 \text{ and } \overline{Z^2} = \overline{i_{gn}^2}\left(1-\left|c\right|^2\right) \quad (2.58)$$

Repeat (2.45)(2.52):

$$\overline{i_{gn}^2} = 4kTd\,g_g \text{ and } \overline{i_{dn}^2} = 4kTg\,g_{d0} \quad (2.59)$$

and (2.53) $g_g = \left(w^2 C_{gs}^2\right)\Big/\left(5g_{d0}\right)$ (2.60)

Define: $a \equiv g_m / g_{d0}$ (2.61)

From (2.58)(2.59)(2.60)(2.61):

$$A = \sqrt{\frac{\overline{i_{gn}^2}}{\overline{i_{dn}^2}}}\left|c\right| = \frac{w_0}{w_T}\sqrt{\frac{da^2}{5g}}\left|c\right| \quad (2.62)$$

From (2.44)(2.51), defining:

$$i_{on,i_{gn},i_{dn}} = i_{odn} + i_{ogn} = \frac{i_{dn}}{\Psi} + \frac{w_T}{w_0}\left(-j+Q_L\right)\frac{i_{gn}}{\Psi} \quad (2.63)$$

From (2.55)(2.63):

$$i_{on,i_{gn},i_{dn}} = \frac{1}{\Psi}\left[i_{dn} + \frac{w_T}{w_0}\left(-j+Q_L\right)\left(A\cdot i_{dn}+Z\right)\right] \quad (2.64)$$

Separate the correlated and uncorrelated parts of i_{on}:

$$i_{on,i_{gn},i_{dn}} = \frac{1}{\Psi}\left[A\frac{w_T}{w_0}(-j+Q_L)+1\right]\cdot i_{dn} + \frac{1}{\Psi}\frac{w_T}{w_0}(-j+Q_L)\,Z \tag{2.65}$$

Combined effect of drain noise and gate noise to output noise $i_{on,ign,idn}$:

$$S_{a,i_{gn},i_{dn}}(w_0) = \overline{i^2_{on,i_{gn},i_{dn}}} = \left|A\frac{w_T}{w_0}(-j+Q_L)+1\right|^2\cdot\frac{\overline{i^2_{dn}}}{\Psi^2} + \left(\frac{w_T}{w_0}\right)^2\left|-j+Q_L\right|^2\frac{\overline{Z^2}}{\Psi^2} \tag{2.66}$$

The correlated portion: $$C = \left|A\frac{w_T}{w_0}(-j+Q_L)+1\right|^2\cdot\frac{\overline{i^2_{dn}}}{\Psi^2} \tag{2.67}$$

And the uncorrelated portion:

$$U = \left(\frac{w_T}{w_0}\right)^2\left|-j+Q_L\right|^2\frac{\overline{Z^2}}{\Psi^2} \tag{2.68}$$

$$S_{a,i_{gn},i_{dn}}(w_0) = C+U \tag{2.69}$$

Correlated portion:

From (2.59)(2.67)

$$C = \left[\left(A\frac{w_T}{w_0}\right)^2 + \left(Q_L A\frac{w_T}{w_0}+1\right)^2\right]\cdot\frac{\overline{i^2_{dn}}}{\Psi^2} \equiv k\,\frac{4kTg\cdot g_{d0}}{\Psi^2} \tag{2.70}$$

Where $$k = \left(A\frac{w_T}{w_0}\right)^2 + \left(Q_L A\frac{w_T}{w_0}+1\right)^2 \tag{2.71}$$

From (2.62) $$k = \frac{da^2}{5g}|c|^2 + \left(1+|c|Q_L\sqrt{\frac{da^2}{5g}}\right)^2 \tag{2.72}$$

Uncorrelated portion:

From (2.58)(2.68)

$$U = \left(\frac{w_T}{w_0}\right)^2 \left(1+Q_L^2\right)\left(1-|c|^2\right)\frac{\overline{i_{gn}^2}}{\Psi^2} \tag{2.73}$$

From (2.62) $\frac{\overline{i_{gn}^2}}{\overline{i_{dn}^2}} = \left(\frac{w_0}{w_T}\right)^2 \frac{da^2}{5g}$ (2.74)

From (2.59)(2.73)(2.74)

$$U = \frac{da^2}{5g}\left(1-|c|^2\right)\left(1+Q_L^2\right)\frac{\overline{i_{dn}^2}}{\Psi^2} \equiv x\,\frac{4kTg\cdot g_{d0}}{\Psi^2} \tag{2.75}$$

Where $x = \frac{da^2}{5g}\left(1-|c|^2\right)\left(1+Q_L^2\right)$ (2.76)

Total contribution from i_{gn} and i_{dn} to $i_{on,ign,idn}$

Define: $c \equiv k + x$ (2.77)

From (2.72)(2.76):

$$c = 1+2|c|Q_L\sqrt{\frac{da^2}{5g}} + \frac{da^2}{5g}\left(1+Q_L^2\right) \tag{2.78}$$

From (2.69):

$$S_{a,i_{gn},i_{dn}}(w_0) = c\,\frac{4kTg\cdot g_{d0}}{\Psi^2} \tag{2.79}$$

Noise Factor of the input stage of the LNA:

Noise comes from R_{eq}:

From (2.37)

$$S_{a,R_{eq}}(w_0) = S_{R_{eq}}(w_0)\left|G_{nR_{eq}}\right|^2 = \frac{4kTR_{eq}w_T^2}{w_0^2 R_{eq}^2 \Psi^2} \tag{2.80}$$

Noise comes from R_g:

Repeat (2.38) here:

$$S_{a,R_g}(w_0) = S_{R_g}(w_0)\left|G_{nR_g}\right|^2 = \frac{4kTR_g w_T^2}{w_0^2 R_{eq}^2 \Psi^2} \tag{2.81}$$

Noise comes from i_{gn} and i_{dn}:

Repeat (2.79) here:

$$S_{a,i_{gn},i_{dn}}(w_0) = c\,\frac{4kTg\cdot g_{d0}}{\Psi^2} \tag{2.82}$$

Noise Factor of the LNA input stage:

$$NF = \frac{S_{a,R_{eq}}(w_0) + S_{a,R_g}(w_0) + S_{a,i_{gn},i_{dn}}(w_0)}{S_{a,R_{eq}}(w_0)} \tag{2.83}$$

From (2.80)(2.81)(2.82)

$$NF = 1 + \frac{R_g}{R_{eq}} + cg\cdot R_{eq} g_{d0}\left(\frac{w_0}{w_T}\right)^2 \tag{2.84}$$

From (2.31)(2.50):

$$Q_L = \frac{w_0\left(L_{eq}+L_s\right)}{R_{eq}} = \frac{1}{w_0 C_{gs} R_{eq}} \tag{2.85}$$

or $$R_{eq} = \frac{1}{w_0 C_{gs} Q_L} \tag{2.86}$$

From (2.61)(2.86)

$$R_{eq} g_{d0} = \frac{1}{w_0 C_{gs} Q_L} \frac{g_m}{a} = \frac{1}{Q_L a} \left(\frac{w_T}{w_0} \right) \tag{2.87}$$

Substituting (2.78) and (2.87) into (2.84), the noise factor is:

$$NF = 1 + \frac{R_g}{R_{eq}} + \frac{g}{a} \left(\frac{w_0}{w_T} \right) \left[\left(1 + \frac{da^2}{5g} \right) \frac{1}{Q_L} + Q_L \frac{da^2}{5g} + 2|c| \sqrt{\frac{da^2}{5g}} \right] \tag{2.88}$$

Note that all of the terms are well defined in (2.88) except for g and d, which are both depend on drain bias in an unspecified fashion. It's difficult to account properly for their contributions. To surmount this difficulty, we adopt the assumption that although each may be a function of bias, the ratio can be expected to show less variation because g and d will likely have similar dependence on bias, given their common progenitor [15].

For further simplification, the noise source of Rg can be neglected because:

a. Sheet resistance R is very small in silicided CMOS process;

b. The gate is given a structure to minimize Rg by means of increasing number of gates and connecting each finger at both ends.

Terms definition for fixed power consumption (P_D) optimization:

In the following, we try to find out the optimum value of channel width of M1 to

minimize the noise factor of the input stage when power consumption is fixed.

Defining: $r \equiv \frac{V_{od}}{L\varepsilon_{sat}}$ where $V_{od} = V_{gs} - V_{TH}$ (2.89)

$$\varepsilon_{sat} = \frac{2v_{sat}}{\mu_{eff}} \text{ [22]} \quad (2.90)$$

$$C_{gs} \approx \frac{2}{3} C_{ox} WL \quad (2.91)$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \text{ and } g_{d0} = g_m\Big|_{V_{ds}=0} \quad (2.92)$$

A 2nd order I-V model of MOSFET:

$$I_{ds} = WC_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} \text{ [22]} \quad (2.93)$$

From (2.89)(2.90)(2.92)(2.93):

$$g_m = \mu_{eff} C_{ox} \frac{W}{L} V_{od} \frac{1 + r/2}{(1+r)^2} \quad (2.94)$$

Another 2nd order I-V model:

$$I_{ds} = \frac{1}{2} \mu_{eff} C_{ox} \frac{W}{L} V_{od}^2 (1 + \lambda V_{ds}) \quad (2.95)$$

From (2.92)(2.95):

$$g_{d0} = \mu_{eff} C_{ox} \frac{W}{L} V_{od} \quad (2.96)$$

Use r to express all variables:

α expressed using r:

From (2.61)(2.94)(2.96)

$$a \equiv \frac{g_m}{g_{d0}} = \frac{1 + r/2}{(1+r)^2} \tag{2.97}$$

Power consumption expressed using r:

Power consumption: $P_D = V_{dd} I_{ds}$ (2.98)

From (2.89)(2.91)(2.93)(2.98):

$$P_D = \left(\frac{2}{3} C_{ox} WL\right)\left(\frac{3}{2} V_{dd} v_{sat} e_{sat}\right)\frac{r^2}{1+r} = C_{gs} w_0 R_{eq} P_0 \frac{r^2}{1+r} \tag{2.99}$$

Where: $P_0 = \frac{3}{2}\frac{V_{dd} v_{sat} e_{sat}}{w_0 R_{eq}}$ (2.100)

Q_L expressed using r and P_D:

From (2.85)(2.99)

$$Q_L = \frac{1}{w_0 C_{gs} R_{eq}} = \frac{P_0}{P_D}\frac{r^2}{1+r} \tag{2.101}$$

$?_T$ expressed using r:

From (2.28)(2.90)(2.91)(2.94)

$$w_T = \frac{g_m}{C_{gs}} = \frac{3v_{sat}}{L} r \frac{1 + r/2}{(1+r)^2} \tag{2.102}$$

Noise Factor expressed using r and P_D. Get rid of the a, Q_L and w_T and neglect the contributions of distributed gate resistance (R_g) to the noise factor:

From (2.88)(2.97)(2.101)(2.102):

$$NF = 1 + \frac{g w_0 L}{3 v_{sat}} P(r, P_D) \text{[15]} \tag{2.103}$$

Where: $$P(r, P_D) = \frac{\frac{P_D}{P_0} P_1(r) + P_2(r) + \frac{P_0}{P_D} P_3(r)}{r^3 \left(1 + \frac{r}{2}\right)^2 (1 + r)} \tag{2.104}$$

$$P_1(r) = (1 + r)^6 + \frac{d}{5g}(1 + r)^2 \left(1 + \frac{r}{2}\right)^2 \tag{2.105}$$

$$P_2(r) = 2|c| \sqrt{\frac{d}{5g}} (1 + r)^3 \left(1 + \frac{r}{2}\right) r^2 \tag{2.106}$$

$$P_3(r) = \frac{d}{5g} \left(1 + \frac{r}{2}\right)^2 r^4 \tag{2.107}$$

Fixed Power Noise Figure vs. W of M1:

From (2.91)(2.101) $$W \approx \frac{3}{2 w_0 L C_{ox} R_{eq}} \frac{P_D}{P_0} \frac{1 + r}{r^2} = f_W(r, P_D) \tag{2.108}$$

thus $$r = f_W^{-1}(W, P_D) \tag{2.109}$$

From (2.103)(2.109) $$NF = 1 + \frac{g w_0 L}{3 v_{sat}} P\left[f_W^{-1}(W, P_D), P_D \right] = 1 + \frac{g w_0 L}{3 v_{sat}} P'(W, P_D) \tag{2.110}$$

The actual expression of (2.110) is very complicated. However, what we care about is the trend that *W* affects *NF*. The plot of *NF* versus *W* can be plotted using mathematics softwares like Matlab and Maple to avoid the tough derivation of expression (2.110). Fig 35 shows the estimation plot of fixed power Noise Figure vs. channel width of M1, using the parameter values in Table 6:

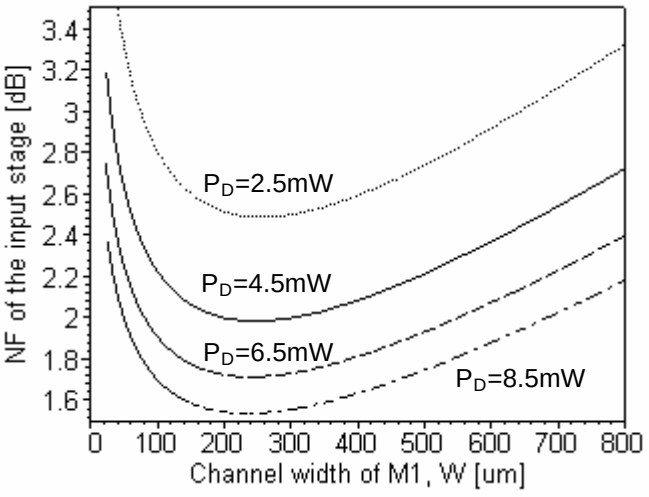


Fig 35 Fixed power Noise Figure *Vs* Channel width of M1.

D. Impedance of the LNA input stage:

Z_{in} of the LNA input stage:

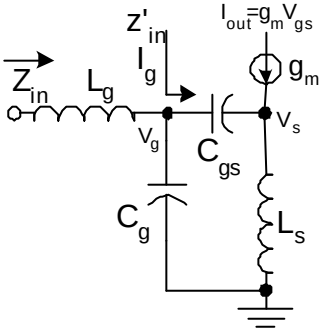


Fig 36 Small signal equivalent circuit of the LNA input stage.

Repeat (2.30) $$z_{in}^{'} = \frac{1}{sC_{gs}} + sL_s + w_T L_s \quad (2.111)$$

$$Z_{in} = sL_g + z_{in}^{'} // \frac{1}{sC_g} \quad (2.112)$$

$$s = jw \quad (2.113)$$

From (2.111)(2.112)

$$Z_{in} = jwL_g + \frac{\left(\frac{1}{C_{gs}} - w^2 L_s + \frac{L_s g_m}{C_{gs}} jw\right)\frac{1}{jwC_g}}{\frac{1}{C_{gs}} + \frac{1}{C_g} - w^2 L_s + \frac{L_s g_m}{C_{gs}} jw} \quad (2.114)$$

Parameter values used in estimation around 2.4GHz:

Give *Ls* an empirical value: $L_s \approx 2.6nH$ (2.115)

$$C_{gs} = C_{gs0} \times W + \frac{2}{3}\frac{e_{ox}}{t_{ox}} W L_{eff} \approx 221fF \quad (2.116)$$

Presumption: $C_{gs} >> C_g$ (2.117)

$$g_m \approx \frac{2I_{ds}}{V_{gs} - V_{th}} \approx \frac{2 \times 4.5}{0.7 - 0.35} \approx 25\frac{mA}{V} \quad (2.118)$$

Please refer to Table 6 to find out the other parameter values.

Magnitude estimation 1:

From (2.116) $\frac{1}{C_{gs}} \approx 4.52 \times 10^{12}$ (2.119)

At resonant f*req*uency: $w_0^2 L_s \approx 0.585 \times 10^{12}$ (2.120)

From (2.119)(2.117)(2.120)

$$\frac{1}{C_{gs}} + \frac{1}{C_g} >> w_0^2 L_s \quad (2.121)$$

From (2.114)(2.121)

$$Z_{in} \approx jwL_g + \frac{\left(\frac{1}{C_{gs}} + \frac{L_s g_m}{C_{gs}} jw - w^2 L_s\right)\frac{1}{jwC_g}}{\frac{1}{C_{gs}} + \frac{1}{C_g} + \frac{L_s g_m}{C_{gs}} jw} \tag{2.122}$$

$$\text{or} \quad Z_{in} \approx jwL_g - \frac{\left(1 + L_s g_m jw - w^2 L_s C_{gs}\right)\left[jw\left(C_g + C_{gs}\right) + w^2 L_s g_m C_g\right]}{w^2 C_g{}^2\left[\left(1 + \frac{C_{gs}}{C_g}\right)^2 + \left(wL_s g_m\right)^2\right]} \tag{2.123}$$

Magnitude estimation 2:

Under presumption (2.117):

$$\left(1 + \frac{C_{gs}}{C_g}\right)^2 > \left(1+3\right)^2 = 16 \tag{2.124}$$

From (2.115)(2.118) $\left(L_s g_m w_0\right)^2 \approx 0.95$ (2.125)

$$\text{Thus} \quad \left(1 + \frac{C_{gs}}{C_g}\right)^2 >> \left(L_s g_m w_0\right)^2 \tag{2.126}$$

From (2.123)(2.126)

$$Z_{in} \approx jwL_g - \frac{\left(1 + L_s g_m jw - w^2 L_s C_{gs}\right)\left[jw\left(C_g + C_{gs}\right) + w^2 L_s g_m C_g\right]}{w^2 C_g{}^2\left(1 + \frac{C_{gs}}{C_g}\right)^2} \tag{2.127}$$

or

$$Z_{in} \approx jwL_g + jwL_s\frac{C_{gs}}{C_g + C_{gs}} + \frac{1}{jw\left(C_g + C_{gs}\right)} - jw\frac{\left(L_s g_m\right)^2 C_g}{\left(C_g + C_{gs}\right)^2} + \frac{L_s g_m C_{gs}\left(C_g w^2 L_s + 1\right)}{\left(C_g + C_{gs}\right)^2} \tag{2.128}$$

Magnitude estimation 3:

From (2.115)--(2.117) $C_g w_0^2 L_s \ll C_{gs} w_0^2 L_s \approx 0.13 < 1$ (2.129)

Thus from (2.128)

$$Z_{in} \approx jwL_g + jwL_s \frac{C_{gs}}{C_g + C_{gs}} + \frac{1}{jw\left(C_g + C_{gs}\right)} - jw\frac{\left(L_s g_m\right)^2 C_g}{\left(C_g + C_{gs}\right)^2} + \frac{g_m C_{gs}}{\left(C_g + C_{gs}\right)^2} L_s \quad (2.130)$$

or $$Z_{in} \approx sL_g + sL_s \frac{C_{gs}}{\left(C_g + C_{gs}\right)} + \frac{1}{s\left(C_g + C_{gs}\right)} - s\frac{\left(L_s g_m\right)^2 C_g}{\left(C_g + C_{gs}\right)^2} + \frac{g_m C_{gs}}{\left(C_g + C_{gs}\right)^2} L_s \quad (2.131)$$

E. The effect of L_{d1} on the output resistance of M2 (before L_{d2}, C_L and C_o are added into the LNA):

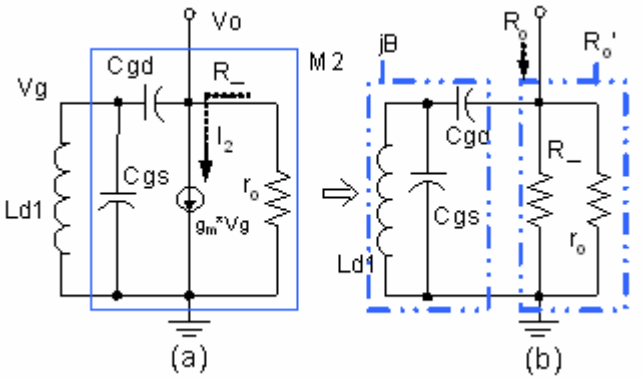


Fig 37 Simplified equivalent circuit of M2 in LNA output stage.

L_{d1} introduces resistor R_:

$$R\_ = \frac{V_o}{I_2} = \frac{V_o}{V_g} \cdot \frac{1}{g_m} \quad (2.132)$$

$$\frac{V_o}{V_g} = \frac{sL_{d1} // \frac{1}{sC_{gs}} + \frac{1}{sC_{gd}}}{sL_{d1} // \frac{1}{sC_{gs}}} = \frac{w^2 L_{d1}\left(C_{gd} + C_{gs}\right) - 1}{w^2 C_{gd} L_{d1}} \quad (2.133)$$

Output resistance of M2:

Define: $w_1 \equiv \frac{1}{\sqrt{L_{d1}\left(C_{gd}+C_{gs}+C_{gd}g_m r_o\right)}}$ (2.134)

$$w_2 \equiv \frac{1}{\sqrt{L_{d1}\left(C_{gd}+C_{gs}\right)}} \quad (2.135)$$

$$w_3 \equiv \frac{1}{\sqrt{L_{d1}C_{gs}}} \quad (2.136)$$

$$w_4 = \frac{1}{r_o C_{gd}} \quad (2.137)$$

$$R_o' = R\_ // r_o \quad (2.138)$$

From (2.132)(2.133)(2.138)

$$R_o' = \frac{1-w^2 L_{d1}\left(C_{gd}+C_{gs}\right)}{1-w^2 L_{d1}\left(C_{gd}+C_{gs}+C_{gd}g_m r_o\right)} r_o = \frac{1-\left(w/w_2\right)^2}{1-\left(w/w_1\right)^2} r_o \quad (2.139)$$

$$jB = \frac{1}{sC_{gd}} + sL_{d1} // \frac{1}{sC_{gs}} = -j\frac{1-w^2 L_{d1}\left(C_{gs}+C_{gd}\right)}{wC_{gd}\left(1-w^2 L_{d1}C_{gs}\right)} = \frac{-j}{wC_{gd}} \cdot \frac{1-\left(w/w_2\right)^2}{1-\left(w/w_3\right)^2} \quad (2.140)$$

$$Z_{out} = jB // R_o' = \frac{B^2 R_o'}{B^2 + R_o'^2} + j\frac{BR_o'^2}{B^2 + R_o'^2} \quad (2.141)$$

$$\mathrm{Re}\left(Z_{out}\right) = \frac{B^2 R_o'}{B^2 + R_o'^2} = \frac{\left[1-\left(w/w_2\right)^2\right]\left[1-\left(w/w_1\right)^2\right] r_o}{\left[1-\left(w/w_1\right)^2\right]^2 + \left(w/w_4\right)^2\left[1-\left(w/w_3\right)^2\right]^2} \quad (2.142)$$

F. List of parameter values:

L or L_{eff}	0.18E-6	?[15]	2.5
W	150E-6	|c|[15]	0.395
? 0	15E9	μ_{eff}	2.836E-2
L_s	2.6E-9	v_{sat}	8.165E4
R_{eq}	50	ε_{ox}	3.984E-11
V_{dd}	1	t_{ox}	4.1E-9
d[15]	5.0	C_{gs0}	3.061E-10

Table 6 Parameter values.

G. Cascaded Stage Linearity:

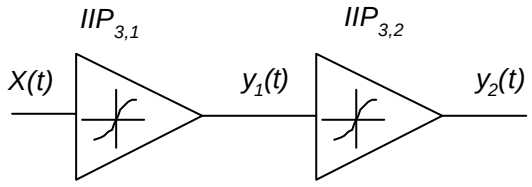
IIP3 Definition:

The nonlinear system model:

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.143}$$

$$A_{IIP3} \equiv \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}$$

General Cascaded Stages:



$$y_1(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.144}$$

$$y_2(t) \approx b_1 y_1(t) + b_2 y_1^2(t) + b_3 y_1^3(t) \tag{2.145}$$

$$\begin{aligned} y_2(t) \approx\ & b_1\left[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)\right] + \\ & b_2\left[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)\right]^2(t) + \\ & b_3\left[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)\right]^3(t) \end{aligned} \tag{2.146}$$

$$y_2(t) \approx a_1 b_1 x(t) + \left(a_3 b_1 + 2a_1 a_2 b_2 + a_1^3 b_3\right) x^3(t) + \cdots\cdots \tag{2.147}$$

$$A_{IIP3}=\sqrt{\frac{4}{3}\left|\frac{a_1 b_1}{a_3 b_1+2a_1 a_2 b_2+a_1^3 b_3}\right|} \tag{2.148}$$

$$\frac{1}{A_{IIP3}^2}=\frac{3}{4}\frac{|a_3 b_1|+2|a_1 a_2 b_2|+|a_1^3 b_3|}{|a_1 b_1|} \tag{2.149}$$

$$\frac{1}{A_{IIP3}^2}=\frac{1}{A_{IIP3,1}^2}+\frac{3a_2 b_2}{2b_1}+\frac{a_1^2}{A_{IIP3,2}^2} \tag{2.150}$$

Normal RF System Cascaded Stages:

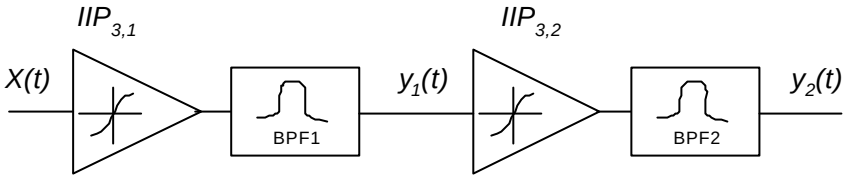


Fig 38 Cascaded nonlinear stages.

$$y_1(t)\approx a_1 x(t)+a_2 x^2(t)+a_3 x^3(t) \tag{2.151}$$

$$x(t)=\cos w_1 t+\cos w_2 t \tag{2.152}$$

$$y_1(t)\approx\frac{A}{4}\left\{\begin{array}{l}4a_2 A+\\ 4a_2 A\cos(w_1-w_2)t+\\ \left(4a_1+9a_3A^2\right)\left(\cos w_1 t+\cos w_2 t\right)\\ 3a_3A^2\left[\cos(2w_1-w_2)t+\cos(w_1-2w_2)t\right]+\\ 2a_2 A\left(\cos 2w_1 t+\cos 2w_2 t\right)+4a_2 A\cos(w_1+w_2)t+\\ 3a_3A^2\left[\cos(2w_1+w_2)t+\cos(w_1+2w_2)t\right]+\\ a_3A^2\left(\cos 3w_2 t+\cos 3w_1 t\right)\end{array}\right\} \tag{2.153}$$

Filtered by the BPF1:

$$y_1(t)\approx\frac{A}{4}\left\{\begin{array}{l}\left(4a_1+9a_3A^2\right)\left(\cos w_1 t+\cos w_2 t\right)\\ 3a_3A^2\left[\cos(2w_1-w_2)t+\cos(w_1-2w_2)t\right]\end{array}\right\} \tag{2.154}$$

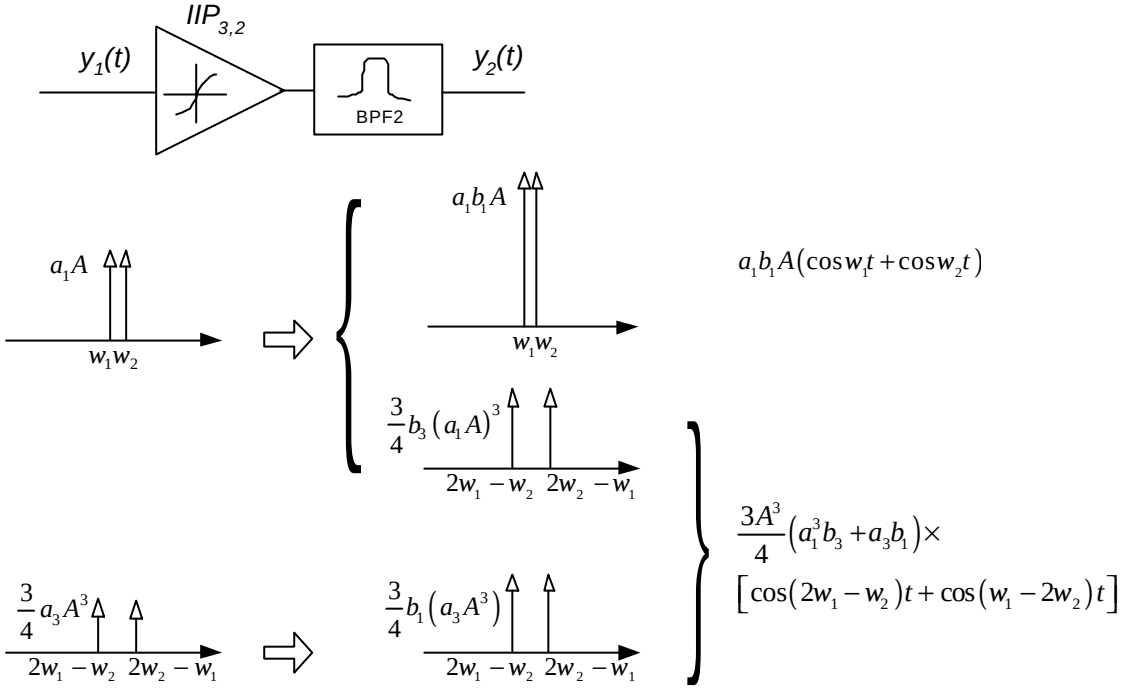
$\because a_1 >> a_3$

$$y_1(t)\approx\left\{\begin{array}{l}Aa_1\left(\cos w_1 t+\cos w_2 t\right)\\ \frac{3a_3A^3}{4}\left[\cos(2w_1-w_2)t+\cos(w_1-2w_2)t\right]\end{array}\right\} \tag{2.155}$$

$$A_{IIP3,1} \equiv \frac{4}{3A}\sqrt{\frac{a_1}{a_3}} \tag{2.156}$$

$$y_2(t) \approx b_1 y_1(t) + b_2 y_1^{\,2}(t) + b_3 y_1^{\,3}(t) \tag{2.157}$$

Filtered by BPF2:



$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1 b_1 A}{3A^3\left(a_1^3 b_3 + a_3 b_1\right)/4}\right|} = \frac{4}{3A}\sqrt{\left|\frac{a_1 b_1}{a_1^3 b_3 + a_3 b_1}\right|} \tag{2.158}$$

$$\frac{1}{A_{IIP3}^2} = \frac{1}{\left(\frac{4}{3A}\sqrt{\frac{a_1}{a_3}}\right)^2} + \frac{a_1^2}{\left(\frac{4}{3A}\sqrt{\frac{b_1}{b_3}}\right)^2} = \frac{1}{A_{IIP3,1}^2} + \frac{a_1^2}{A_{IIP3,2}^2} \tag{2.159}$$

For the more general expression, if m stages are cascaded in series. The k^{th} stage is express as:

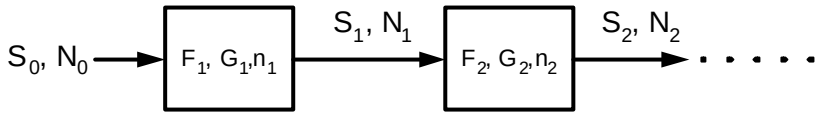
$$y_k(t) \approx a_{k,1} y_{k-1}(t) + a_{k,2} y_{k-1}^2(t) + a_{k,3} y_{k-1}^3(t) \tag{2.160}$$

The total A_{IIP3} can be expressed as:

$$\frac{1}{A_{IIP3}^2} = \sum_{n=1}^{m} \frac{a_{n-1,1}^2}{A_{IIP3,n}^2}, \quad a_{0,1} = 1 \tag{2.161}$$

We can see that, the nonlinearity of the latter stages becomes increasingly more critical because the IP3 of each stage is effectively scaled down by the total gain preceding that stage.

H. Cascaded Stage Noise:



F_i ≡ noise factor of the i^{th} stage

G_i ≡ power gain of the i^{th} stage

n_i ≡ internal noise power of the i^{th} stage

$$(NF)_i = \frac{\frac{S_{i-1}}{N_{i-1}}}{\frac{S_i}{N_i}} = \frac{\frac{S_{i-1}}{N_{i-1}}}{\frac{G_i S_{i-1}}{G_i N_{i-1} + n_i}} \tag{2.162}$$

$$(NF)_i = \frac{G_i N_{i-1} + n_i}{G_i N_{i-1}} = \frac{\text{Total output noise power}}{\text{Output noise due to input source}} \tag{2.163}$$

For two stages in Cascade, the output noise figure is:

$$NF = \frac{G_1 G_2 n_0 + G_2 n_1 + n_2}{G_1 G_2 n_0} = \frac{G_1 n_0 + n_1}{G_1 n_0} + \frac{n_2}{G_1 G_2 n_0} \tag{2.164}$$

$$NF = (NF)_1 + \frac{n_2}{G_1 G_2 n_0} \tag{2.165}$$

$$\because \left(NF\right)_2 = \frac{G_2 n_0 + n_2}{G_2 n_0} \tag{2.166}$$

$$\therefore \left(NF\right)_2 = 1 + \frac{n_2}{G_2 n_0} \tag{2.167}$$

$$\therefore \frac{n_2}{G_2 n_0} = 1 - \left(NF\right)_2 \tag{2.168}$$

$$NF = \left(NF\right)_1 + \frac{\left(NF\right)_2 - 1}{G_1} \tag{2.169}$$

This can generalized to:

$$NF = \left(NF\right)_1 + \frac{\left(NF\right)_2 - 1}{G_1} + \frac{\left(NF\right)_3 - 1}{G_1 G_2} + \cdots\cdots \tag{2.170}$$

$$NF = \left(NF\right)_1 + \sum_{i=2}^{N} \frac{\left(NF\right)_i - 1}{\prod_{j=1}^{i-1} G_j} \tag{2.171}$$