OXIDE BYPASSED POWER MOSFET DEVICES

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A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2003

ACKNOWLEDGEMENTS

I would like to commence by expressing my earnest gratitude to my supervisors, Professor Yung C. Liang and Professor Ganesh S. Samudra, for their precious suggestions, patience and great assistance in all the time of my research and writing this thesis.

Especially, I want to give my deep sense of appreciations to my parents, Yang Yiwei and Liu Lanqin, my husband, Shen Jiali, and my younger sister, Yang Fan, whose endless encouragement and love enable me to accomplish this work.

Appreciations are given to National University of Singapore, for providing me the research opportunity and financial support.

I am grateful to my colleagues, Gan Kian Paau, Zhu Yuanzheng and Lim Chow Yee, for their valuable guidance and help in the experimental work and theoretical analysis. Special thanks to the staff in Institute of Microelectronics Singapore, Liu Yong and Ren Changhong, for their kindly supports on process and fabrication.

Many thanks to all my friends in National University of Singapore, for making the research work become rich and colorful. I am also thankful to all the people who used to come into my life and provide certain assistance in various ways on my research.

DECLARATION OF ORIGINAL CONTRIBUTIONS

The author would like to declare the original contributions based on the research as follows:

1. Tunable Oxide Bypassed structure has an enhanced breakdown voltage and on-state resistance compared to conventional power MOSFETs as stated in Section 3.3 of Chapter 3.

2. Development of process steps and mask layout for 100V TOBUMOS fabrication with the standard clean room facilities as in Chapter 4.

3. The theoretical analysis of Gradient Oxide Bypassed structure as described in Section 6.1 of Chapter 6.

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SUMMARY

In the evolution of power industry, power devices with the property of high blocking capability but lower on resistance are required in many applications of modern power electronics. Recently, based on the extensive superjunction (SJ) theory with stacked p and n columns in drift region, SJ devices have been recognized as advanced power devices that can meet the requirements. The main methods of realizing SJ devices are multi-epitaxy and deep trench technology. Unfortunately, the applications of SJ devices are commercially restricted by the complicated fabrication steps, charge imbalance and inter-diffusion problems.

Poly-Flanked (PF) technology has been successfully applied to realizing advanced SJ-VDMOS. With a thin Oxide layer between p/n columns, SJ structure with minimized inter-diffusion problem can be easily fabricated. PF-VDMOS is experimentally proven to have lower specific on-resistance than the ideal silicon limit at the same voltage rating. However, charge imbalance is still a problem, which handicaps the development of SJ devices.

To overcome problems encountered in SJ devices, Oxide-Bypassed (OB) structure is introduced. By replacing the p column of SJ-MOSFETs with a thick thermal Oxide/Polysilicon stucture, OB-MOSFETs bring forth enhanced breakdown voltage by helping to deplete the n-drift region horizontally. Without the restriction of charge matching, OB devices are free from the difficult fabrication process. OB structure was also applied to the edge termination region of fabricated PF-VDMOS and it shows a good high voltage sustaining capability by depleting the sidewall n columns at

termination. Process and device simulations were performed on optimising the $R_{on,sp}$~V_{br} performance of OB devices.

For structural variation in the OB MOSFET devices, sidewall PolySi region can be electrically separated from the Source without any difficulty. This adds an additional tuning electrode connected to the sidewall PolySi region and a new device called Tunable Oxide Bypassed (TOB) MOSFET is created. Simulation result reveals that, by applying certain positive Control bias, the improvement on both off state blocking capability and on state conductivity is observed. This result exhibits a $R_{on,sp}$~V_{br} point further away from the ideal silicon limit compared to the optimum OBUMOS. At the same breakdown voltage, $R_{on,sp}$ of 100V TOBUMOS is about 46% lower than that of conventional UMOS.

Fabrications of 100V TOBUMOS and TOB-Diode were carried out on the same dual epi wafers. Formed on 0.55Ω-cm epi layer, measured V_{br} of TOB-Diode is 103V at 20V Control bias, and TOBUMOS exhibits the V_{br} of 79V under 5V bias with $R_{on,sp}$ of 0.674 mΩ-cm^2, while V_{br} is 68V for conventional Diode on the same wafer. The fabrication result of TOBUMOS successfully breaks the ideal SJ limit line. Thus, the concept of TOB structure is verified in the enhancement of the device performance in a practical method.

Gradient Oxide Bypassed (GOB) structure as another way to enhance the OB device performance is proposed later. Theoretically and through simulations, GOB structure has been proven to have a better performance than both conventional and SJ structures. However, due to the difficulties in forming a desired Oxide slope, future research on GOB device realization is required.

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LIST OF SYMBOLS

D	Diffusion coefficient	q	Elementary charge
ε_0	Vacuum permittivity	Q	Charge
ε_{ox}	Permittivity of Oxide	R_{ch}	Channel resistance
ε_s	Permittivity of Silicon	R_d	Drift region resistance
E	Electric field	R_{on}	On resistance
E_{crit}	Critical electric field	$R_{on,sp}$	Specific on-resistance
E_{max}	Maximum electric field	t_{ox}	Oxide thickness
E_{ox}	Electric field in Oxide	T	Temperature
F_T	Unity-gain frequency	T_{epi}	Epitaxy layer thickness
G_m	Transconductance	μ_n	Electron mobility
I_{DS}	Drain-Source current	V	Voltage
I_{GS}	Gate-Source current	V_{bi}	Built-in potential
J	Current density	V_{br}	Breakdown voltage
k	Boltzmann constant	V_{DS}	Drain-Source voltage
L	Length of drift region	V_{GS}	Gate-Source voltage
L_{dep}	Depletion length of pn junction	V_T	Threshold voltage
n_i	Intrinsic doping concentration	W	Width of drift region
N	Doping concentration	W_{bi}	Built-in depletion width
N_d	Drift region doping concentration	W_{dep}	Depletion width of pn junction
N_A	Acceptor doping concentration	W_n	Width of superjunction n column
N_D	Donor doping concentration	W_p	Width of superjunction p column
ρ_{epi}	Epi resistivity		

LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
Epi	Epitaxy
IGBT	Insulated Gate Bipolar Transistor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
DMOS	Double-diffusion MOS
LDMOS	Lateral DMOS
VDMOS	Vertical DMOS
UMOS	U-shaped trench Gate MOS
VMOS	V-shaped trench Gate MOS
SOI	Silicon on Insulator
OB	Oxide-Bypassed
GOB	Gradient Oxide Bypassed
TOB	Tunable Oxide Bypassed
PF	Poly-Flanked
SJ	Superjunction
PolySi	Polysilicon

Chapter 1

Introduction

1.1 History of Power MOSFETs

Since 1950's, when the first power semiconductor device was invented, power devices have been playing an important role in the power electronics industry [1]. They are widely used as power rectifiers and power switches, which are the key components in applications such as display drives, motor control, power supplies, automotive electronics, telecom circuits, etc. In the earlier applications of power switches, the Bipolar Junction Transistor (BJT) with the property of current control was popularly accepted. However, achievement of high current gain in BJT causes some problems in blocking voltage, on-state resistance, drive capability, temperature effects, etc. For this reason, it has been proposed to replace BJTs by power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

1.1.1 Power MOSFETs basic

The power MOSFET is a unipolar, majority carrier, voltage-controlled device. Being a majority-carrier device, power MOSFETs have been used in converters with high switching speeds. With Metal Oxide Semiconductor gate structure, the majority-carrier current in power MOSFET is controlled by gate potential. Thus, the power MOSFET has very high input impedance in steady state and no offset voltage at on state can be seen when it is used as an analog switch [2]. Power MOSFETs also exhibit a wide safe operating area and the feature of ease of parallel connection due to

the forward voltage drop with positive temperature coefficient. Because of the high mobility of electrons, n-channel MOSFETs are widely used in the industry.

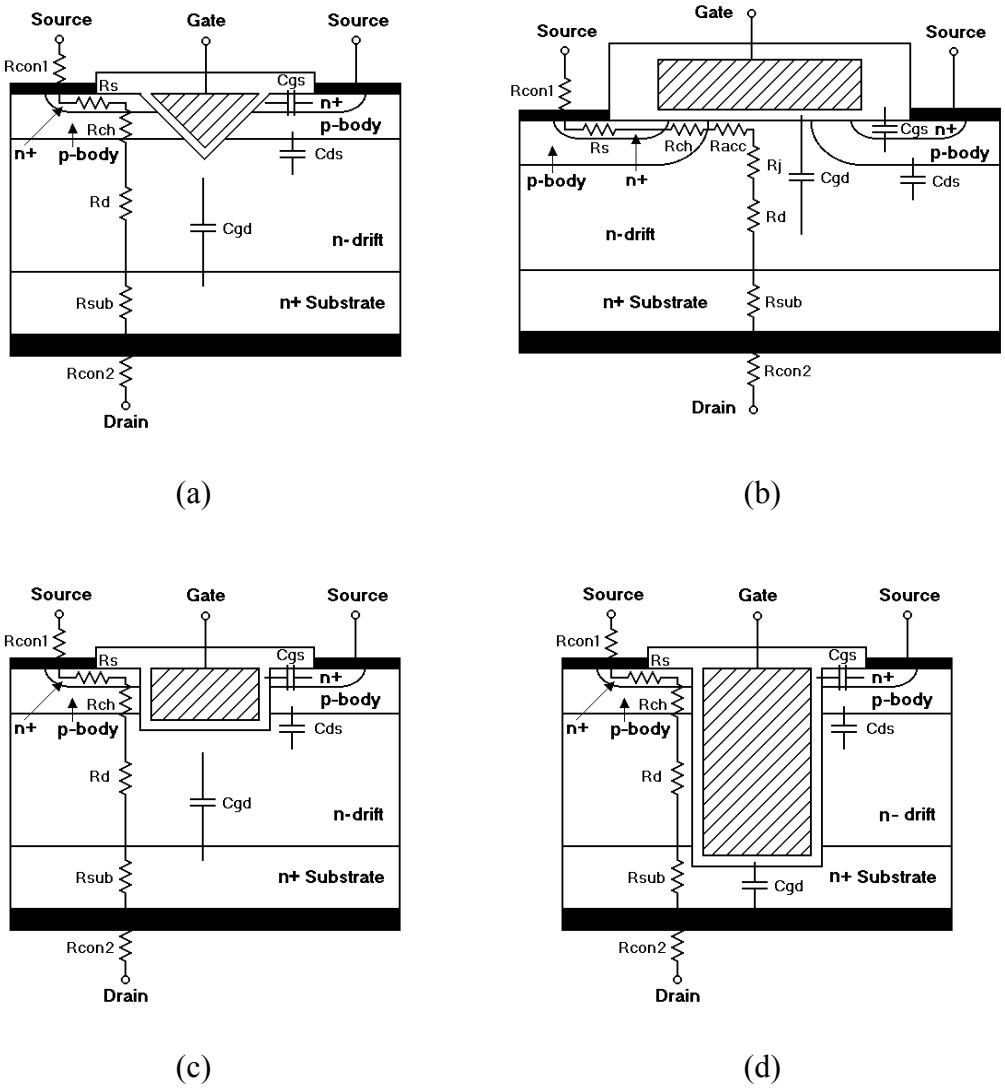


Figure 1-1: Conventional vertical Power MOSFET structures. (a) VMOS; (b) DMOS; (c) UMOS; (d) UMOS with extended trench Gate

The ordinary n-channel vertical MOSFETs are shown in Figure 1-1[3]. Basic MOSFETs have three electrodes of Gate, Source and Drain, as shown in Figure 1-1. The n-channel MOSFET is off when $V_{GS} < V_T$, where V_T is the threshold voltage. In this case, only a small reverse leakage current flows between the Source and Drain. When a sufficient V_{GS} is applied to be higher than V_T, a thin surface inversion layer or conducting n-channel forms. Once the inversion layer is formed, the electron current

flow from the Source to the Drain through the n-channel can be controlled by varying the Drain voltage (V_{DS}). If V_{DS} is small, electron flow yields a linearly increasing Drain current with V_{DS}. As V_{DS} increases, the inversion layer eventually reaches the pinch-off state. Beyond pinch-off, Drain current essentially saturates and does not increase with V_{DS}. The basic on resistance (R_{on}) parameters for the Power MOSFET are given as below:

$$R_{on} = R_{con1} + R_S + R_{ch} + R_{acc} + R_j + R_d + R_{sub} + R_{con2}, \tag{1.1}$$

The drift region resistance is:

$$R_d = T_d / (q\mu_n N_d), \tag{1.2}$$

where T_d is the depth of n-drift region.

Historically, V-MOSFET, as shown in Figure 1-1(a), was the first commercial vertical Power MOSFET structure. However, because of the etching solutions used for V-groove formation, there exists the stability problem of threshold voltage in manufacturing, and the high electric field at the tip of the V-groove results in a premature breakdown, V-MOSFET was replaced by Double-diffusion MOS (DMOS) shortly. Using double-diffusion and planar Gate process, DMOSFET shown in Figure 1-1(b) is easy to fabricate in comparison to V-MOSFET. However, in DMOSFET, there is a parasitic JFET between two p-body regions. The parasitic JFET can cause unwanted device turn-on and premature breakdown in DMOSFETs. To solve this problem, UMOS shown in Figure 1-1(c) was developed. Possessing of U grooved trench Gate structure, UMOS represents a higher channel density and therefore decreasing on-resistance compared to VMOS and DMOS. It was found that, if the trench depth becomes deeper, on-resistance is lower because of the formation of accumulation layer along the trench sidewall in drift region. Thus, if trench Gate structure can be extended down to the substrate as shown in Figure 1-1(d), on-

resistance reaches the lowest value. However, this structure is limited in application of below 30V because early breakdown occurs at the bottom of extended Gate Oxide in drift region. Increasing Oxide thickness in drift region can be a feasible way to alleviate this problem as in Reference [4].

1.1.2 Comparisons between Power MOSFETs and IGBTs

In the recent years, more and more semiconductor devices such as IGBT, SIT, SITH, GCT and MCT [5] were introduced to meet different requirements of power semiconductor industry. Especially, the IGBT combines the advantages of low power drive MOS gate structure with the low conduction losses and high blocking voltage characteristics of the BJT. It is possible to reduce on-state voltage drop by minority carrier injection in the IGBT. Therefore the device is highly suitable for high power, high voltage applications. However, because the tail current problem at turn-off cannot be solved in the IGBT as in the BJT, its switching speed is limited by the charge removal. Hence the IGBT is, at present, limited to lower frequency applications.

In consideration of the switching frequencies and overall size of switch-mode power supplies, power MOSFETs will remain as viable devices in low-voltage low-power high-frequency applications.

1.1.3 Problems encountered in Power MOSFETs applications

The power MOSFET still has limitations, especially in voltage rating and cost. The device has a much higher fabrication cost compared with BJTs. The intrinsic characteristics of the MOSFET produce a large on-resistance, which increases excessively when the devices' breakdown voltage is raised. Furthermore, the built-in

body diode in the power MOSFETs can carry full current but it also shows slow reverse recovery characteristics. Therefore, the power MOSFET is only useful up to voltage ratings of 500V and so is restricted to low voltage applications or in two-transistor forward converters and bridge circuits operating off-line. Improvements in fabrication techniques and device characteristics are still in progress so that the MOSFET is likely to replace BJTs in most applications especially as the cost per device is reduced.

1.2 Superjunction devices — improved Power MOSFETs

The term of "superjunction" [6], or so-called "COOLMOS" [7] or "3D Resurf" [8], was introduced to represent a novel MOSFET structure for the power switches. The generation of the Superjunction (SJ) structure is based on the concept of charge compensation [9-11]. Based upon the established theoretical analysis [6, 12], the development of SJ devices experienced a prosperous rapid period. During this period, research efforts on various SJ devices such as [13-23] were proposed for different applications.

1.2.1 Features of SJ devices

As is known that, in conventional power MOSFETs, lowering doping concentration is the only way to increase breakdown voltage (V_{br}). In addition, the specific on-resistance ($R_{on,sp}$) is limited by the voltage rating through $\sim V_{br}^{2.5}$. While in the SJ structure, this problem is solved by paralleling high doping alternative p/n layers in drift region. The p/n columns involved in SJ devices function to further deplete the drift region in horizontal direction. It is required that p/n columns have the equal charge to achieve the best performance. By properly controlling the charge of p/n

layers, high V_{br} can be realized in wide depletion region of p-n junction. At certain V_{br}, $R_{on,sp}$ can be further reduced by increasing the doping concentration. Therefore, compared to conventional MOSFETs, achievement of higher breakdown voltage in SJ devices is allowed, even at high impurity concentrations. Obviously, increasing the thickness of drift region will further increase V_{br}.

1.2.2 Difficulties in SJ devices realization

Presently, the main methods available to realize SJ devices are COOLMOS [13] multi-epitaxy technology and vertical deep trench technology [16-17]. As is known that, the horizontal auto-doping effect caused by high temperature and long time drive-in steps is the main problem in the multi-epitaxy process. It leads to the higher on-state resistance. Besides, high fabrication cost and complicated steps are also required to fulfill the multi-epitaxy process. Though vertical deep trench technology with precise controlled implantation is supposed to relieve the problems above-mentioned, charge imbalance (refer to Section 2.2.3) and inter-diffusion [24] between p and n columns of SJ devices are still the problem, which degrades the performance of the SJ devices. In addition, high off-state leakage current with Polysilicon involved and soft breakdown effect [17] restrict the popularization of vertical deep drench technology on SJ devices.

1.2.3 Current efforts on SJ device amelioration

(a) Polysilicon Flanked VDMOS (PFVDMOS) [24] was designed to overcome the inter-diffusion problem of SJ structure by simply adding a thin oxide layer at the interface between p/n columns. The detailed structure description and performance of PFVDMOS will be represented in the next chapter.

(b) Most distinguishingly, Oxide Bypassed (OB) VDMOS [25] set up the new milestone for the development of SJ devices. Theoretically, the OB structure functions as the p column in SJ structure. It makes the device extricate itself from the dependence of net charge balance and inter-diffusion problem. Owing to the application of OB structure, the benefits of SJ devices compared to conventional devices can be exerted to the greatest extent.

(c) Lateral SJ devices fabricated on SOI wafer [26-30] broadens the applications of the SJ structure in RF and power integrated circuits. Attempts on SJ-LDMOS with Partial SOI structure [31] are promising to realize Lateral SJ structure on economic bulk Silicon wafer.

1.3 Objectives

Based on the current state of the art, this work focuses on the study and development of improved SJ devices. The objectives are:

(a) To investigate the possibility of designing an ideal OB device structure with high V_{br} but low $R_{on,sp}$ to realize or enhance device performance predicted by the SJ theory by comparing current research efforts on applicable SJ structures,.

(b) To confirm the device parameters and verify the device function on proposed device, by using process and device simulations and theoretical analyses.

(c) To design mask layout and explore a feasible fabrication process flow on proposed OB device with the advantage of SJ principle to support the numerical simulations.

(d) To guarantee correct manufacturing process and carry out failure analyses in the meantime to fabricate a commercial functional device.

1.4 Thesis outline

This thesis aims to make thorough study on application and realization of SJ theory. It covers both the theoretical analyses and experimental operations. It is organized into 7 chapters:

Chapter 1 – Basic knowledge of conventional power MOSFETs and SJ structure are briefly reviewed to describe the background of present research. The project objectives are presented afterwards.

Chapter 2 – Detailed theoretical analyses of SJ devices are first carried out. The motivation of this work is then demonstrated by comparing features of different devices. Measurement results and analyses of PFVDMOS wafer are included to state the current efforts and achievements on SJ devices fabrication.

Chapter 3 – The characteristics of OBUMOS and research background are introduced. Efforts trying to improve the performance of OBUMOS are discussed. Tunable OB device is introduced after the discussion. Particular simulation methods on Tunable OBVDMOS and OBUMOS are presented to show the superior performance of Tunable MOSFETs compared to conventional MOSFETs and SJ devices at the same V_{br}.

Chapter 4 – Simulation, fabrication arrangement and process steps of 100V TOBUMOS are proposed in details.

Chapter 5 – Measurement results and discussions are presented, based on 100V TOBUMOS fabrication.

Chapter 6 – Future possibilities of research in the field of power switches, aimed on the improvement of OB SJ devices, are discussed.

Chapter 7 – In this section, the achievements of current researches are concluded and the future trends are briefly described.

Chapter 2

Superjunction Device Physics

The on-resistance of conventional power MOSFETs is limited by the doping concentration and thickness of epi layer to support known breakdown voltage. In other words, the applications of conventional Power MOSFETs are restricted by a certain V_{br} vs. $R_{on,sp}$ relationship, which is known as the ideal silicon limit [6][32]. The created Superjunction structure is able to break this limit at the high breakdown voltage range. This chapter begins with the theory of ideal silicon limit, followed by the theoretical deductions of $V_{br} \sim R_{on,sp}$ limit for SJ devices. The characteristics of existent SJ devices are introduced afterwards to address current research background and achievements.

2.1 Power MOSFETs basic concepts

2.1.1 Blocking voltage

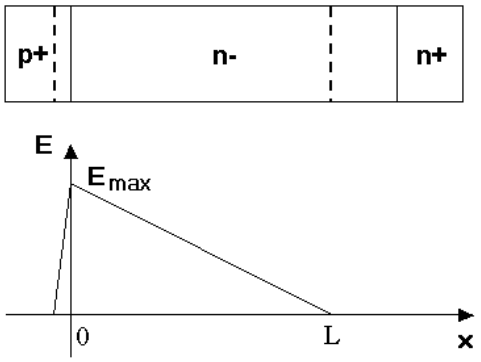


Figure 2-1: Electric field for normal p-i-n diode under reverse bias

In the power MOSFET, the ability to block current flow at high voltages is obtained by supporting the voltage across a reverse biased p-i-n junction. It can withstand the application of high current and voltage, for a short duration, without undergoing destructive failure due to second breakdown. The electric field plot for normal parallel-plane abrupt juction p-i-n diode under reverse bias is shown in Figure 2-1.

According to Poisson's Equation and boundary condition:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_s} = \frac{qN_d}{\varepsilon_s} \ (E = 0 \ at \ x = L), \tag{2.1}$$

the solutions of electric field (E) and applied voltage (V) can be obtained as:

$$E = \frac{qN_d}{\varepsilon_s}(L - x) \ ; \ V = \frac{qN_dL^2}{2\varepsilon_s} \tag{2.2}$$

When $x = 0$,

$$E_{\max} = \frac{qN_dL}{\varepsilon_s} \Rightarrow L = \frac{E_{\max}\varepsilon_s}{qN_d} \tag{2.3}$$

The breakdown voltage V_{br} is defined as the voltage when the maximum electric field E_{max} reaches critical electric field E_{crit}. Therefore, substituting Equation (2.3) to Equation (2.2), blocking voltage of normal p-i-n diode is given by

$$V_{br} = \frac{qN_d(\frac{E_{crit}\varepsilon_s}{qN_d})^2}{2\varepsilon_s} = \frac{\varepsilon_s E_{crit}^2}{2qN_d}, \tag{2.4}$$

where N_d is the donor concentration on the homogeneously doped n-drift region and $\varepsilon_s = 11.8\varepsilon_0 = 1.044 \times 10^{-12}$ (F/cm).

Critical electric field E_{crit} can be approximated by [32]

$$E_{crit} = 4010N_d^{1/8} \tag{2.5}$$

Thus, at certain doping concentration N_d, blocking voltage can be obtained by

$$V_{br} = 5.34 \times 10^{13} N_d^{-3/4} \tag{2.6}$$

2.1.2 Specific On-Resistance

(a) Specific On-Resistance of drift region ($R_{d,sp}$)

It is known that the impact ionization coefficient approximation is [32]:

$$\alpha = 1.8 \times 10^{-35} E^7 \tag{2.7}$$

The avalanche breakdown condition is:

$$\int_0^w \alpha \cdot dx = 1 \tag{2.8}$$

By combining Equation (2.2), Equation (2.7) and Equation (2.8), we may get the depletion region width (W_{dep}) at breakdown:

$$W_{dep} = 2.67 \times 10^{10} N_d^{-7/8} \tag{2.9}$$

Therefore,

$$R_{d,sp} = \frac{W_{dep}}{q\mu N_d} = 5.93 \times 10^{-9} V_{br}^{2.5} \tag{2.10}$$

(b) The Specific On-Resistance of Conventional VDMOS is given by [33]:

$$R_{on,sp} = \frac{27 V_{br}^2}{8\mu\varepsilon_s E_{crit}^3} \tag{2.11}$$

Substitute $E_{crit} = 8.2 \times 10^5 V_{br}^{-0.2}$ ($\mathrm{V \cdot cm^{-2}}$) and $\mu = 710 V_{br}^{0.1}$ ($\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$) [6] into Equation (2.11), thus

$$R_{on,sp} = 8.3 \times 10^{-9} V_{br}^{2.5} \ \ (\Omega \cdot \mathrm{cm^2}) \tag{2.12}$$

2.2 Superjunction devices

2.2.1 Basic Concept

The typical SJ structure is shown as in Figure 2-2. Different from the conventional structure shown in Figure 2-1, SJ devices show the superior performance on blocking

voltage and on-state resistance by replacing drift region with alternative heavily doped p/n semiconductor layers. Figure 2-2 also gives the approximate electric fields of the SJ device under the bias of $V_{DS} > 0$.

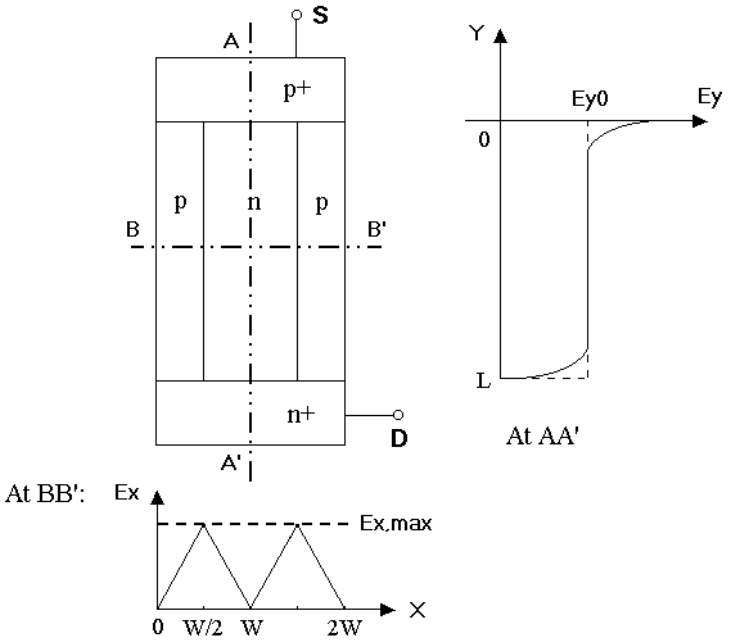


Figure 2-2: Superjunction structure and the approximate electric field at $V_{DS} > 0$.

(a) Optimum doping concentration $N_{d,op}$:

As is known that for SJ devices having a given breakdown voltage, there exists an optimum doping concentration $N_{d,op}$ that results in the minimum on resistance. Equation (2.13) gives the depletion width of p-n junction under certain reverse bias V.

$$W_{dep} = \sqrt{\frac{2\varepsilon_s V(N_A + N_D)}{qN_A N_D}} \tag{2.13}$$

where N_A and N_D are doping concentration of p and n column, respectively [32]. In ideal SJ devices abovementioned, it is required that

$$N_A = N_D = N_{d,op} \tag{2.14}$$

Assume such a condition that, when the device is at breakdown, the depletion region of SJ structure just pinch-off horizontally. That is, the p/n column width $W_p = W_n = W$ is

equal to the total depletion width of W_{dep}. By combining Equation (2.6), (2.13) and (2.14), the relationship between $N_{d,op}$ and W is approximated as:

$$N_{d,op} = 1.2 \times 10^{12} W^{-8/7} \tag{2.15}$$

(b) $R_{on,sp}$ Calculation:

From the simulation, we know the breakdown of SJ structure always happens at the interface between p and n columns. It is because that, in SJ structure, because of the influence from the sidewall p column, there is an additional horizontal electric field component (E_x) compared to conventional p-i-n diode, where the electric field is only in vertical direction. Along the central vertical line of n or p column, horizontal electric fields generated from neighboring p-n junction are in opposite direction and counteract each other. Thus only vertical electric field manifests. While at the interface of p/n column, because E_x reaches the maximum value $E_{x,max}$ and vertical electric field (E_y) doesnot change horizontally, total electric field (E) is highest as well. The profile of E_y is shown in Figure 2-2. To simplify the derivation of blocking voltage, we assume that when the p/n column length L is big enough, E_y has constant value of E_{y0} and breakdown happens in the condition that the total electric field reaches the critical electric field of silicon (E_{crit}), which is expressed by:

$$E_{crit} = \sqrt{E_{x,\max}^2 + E_{y0}^2} \tag{2.16}$$

If

$$E_{x,\max} = \alpha E_{crit} \tag{2.17}$$

Then

$$E_{y0} = \sqrt{1-\alpha^2}\, E_{crit} \tag{2.18}$$

where α is the coefficient which has the value between 0 and 1.

According to the expression of p-i-n junction structure, $E_{x,max}$ is given by:

$$E_{x,\max} = \frac{qN_aL}{2\varepsilon_s} = \frac{qN_dL}{2\varepsilon_s} < E_{crit} \tag{2.19}$$

Combining Equation (2.17) & Equation (2.19), we get

$$q\mu N_d = (2\mu\alpha\varepsilon_s E_{crit})/L \tag{2.20}$$

Thus, $R_{on,sp}$ in the region of ($0 < x < W$) is:

$$R_{on,sp} = \frac{2L}{q\mu N_d} = \frac{WL}{\mu\alpha\varepsilon_s E_{crit}} \tag{2.21}$$

Therefore when $L >> W$, V_{DS} is given by:

$$V_{DS} \approx E_{y0}L = \sqrt{1-\alpha^2}E_{crit}L \tag{2.22}$$

Substitute Equation (2.22) for (2.21):

$$R_{on,sp} = \frac{WV_{br}}{\alpha\sqrt{1-\alpha^2}\mu\varepsilon_s E_{crit}^2} \tag{2.23}$$

Numerical simulation by using MEDICI [34] was carried out in order to find out the relationship between electric field of SJ structure and critical electric field of conventional MOSFETs at the same epi doping concentration. In this simulation, SJ structures with different column width and length are included.

Table 2-1: Simulated relationship between $E_{x,max}$ and E_{crit} according to the ratio of W/L

N (cm^{-3})	9.8×10^{16}	4.47×10^{16}	1.27×10^{16}	7.1×10^{15}	3.2×10^{15}	1.5×10^{15}
W (μm)	0.5	1	3	5	10	19.5
E_{crit} (V/cm)	5.33×10^{15}	4.84×10^{15}	4.13×10^{15}	3.84×10^{15}	3.48×10^{15}	3.16×10^{15}
L = 15 μm						
$E_{x,max}$ (V/cm)	3.5692×10^{5}	3.2560×10^{5}	2.7732×10^{5}	2.5463×10^{5}	1.9560×10^{5}	1.1263×10^{5}
W/L	0.033	0.067	0.2	0.333	0.667	1.3
$\alpha = E_{x,max}/E_{crit}$	**0.670**	**0.673**	**0.671**	0.663	0.562	0.356
L = 20 μm						
$E_{x,max}$ (V/cm)	3.5692×10^{5}	3.2560×10^{5}	2.7751×10^{5}	2.5775×10^{5}	2.1585×10^{5}	1.4304×10^{5}
W/L	0.025	0.05	0.15	0.25	0.5	0.975
$\alpha = E_{x,max}/E_{crit}$	**0.670**	**0.673**	**0.672**	**0.671**	0.620	0.453
L = 50 μm						
$E_{x,max}$ (V/cm)	3.5692×10^{5}	3.2560×10^{5}	2.7752×10^{5}	2.5858×10^{5}	2.3293×10^{5}	2.0652×10^{5}
W/L	0.01	0.02	0.06	0.1	0.2	0.39
$\alpha = E_{x,max}/E_{crit}$	**0.670**	**0.673**	**0.672**	**0.673**	**0.669**	0.654

Table 2-1 gives the relationship between $E_{x,max}$ and E_{crit} according to the dimensions of SJ structures. To guarantee the accuracy of the simulation results, $E_{x,max}$ is extracted from the point at the center of the vertical line along the p/n interface. E_{crit} is extracted from Equation (2.5).

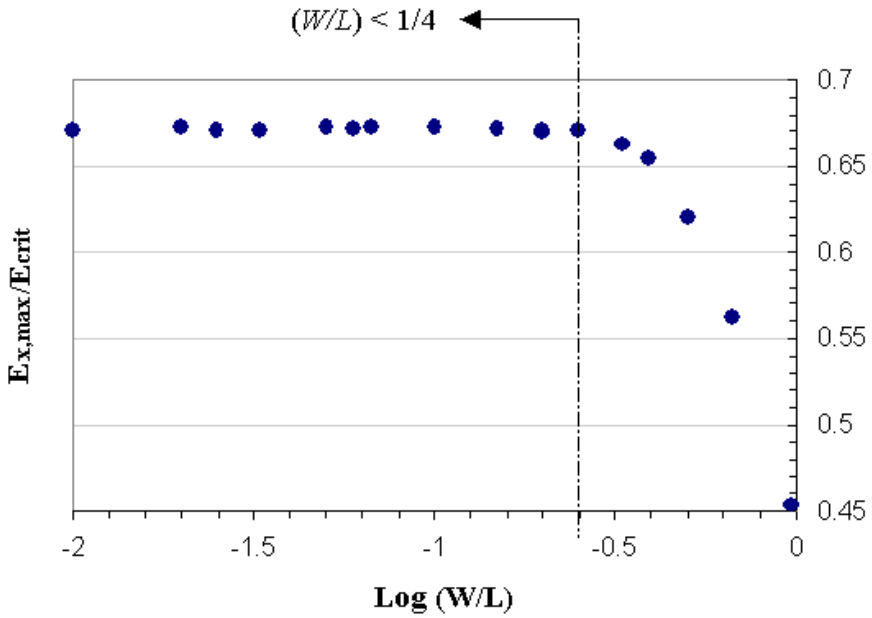


Figure 2-3: Relationship between $E_{x,max}/E_{crit}$ and W/L for SJ structure.

It was observed that, $\alpha = E_{x,max}/E_{crit}$ has a nearly constant value when $L >> W$ is satisfied. As shown in Figure 2-3, when W/L is smaller than 1/4, almost all the simulation results of $E_{x,max}/E_{crit}$ fall into the range of 0.669 to 0.673. Therefore, the average value of 0.672 is accepted for α.

The minimum $R_{on,sp}$ is then achieved by $R_{on,sp} \approx \dfrac{2WV_{br}}{\mu\varepsilon_s E_{crit}^2}$, when $\alpha = 0.672$. Thus, for vertical SJ devices,

$$R_{on,sp} = 2.18\times10^{-3} WV_{br}^{1.3} \tag{2.24}$$

According to Equation (2.24), the ideal SJ limits of $R_{on,sp}$ in terms of V_{br} for ideal SJ structure at different column widths are plotted compared to ideal Silicon limit, SJ limit for Vertical MOSFETs and simulated SJ MOSFETs [6] as shown in Figure 2-4.

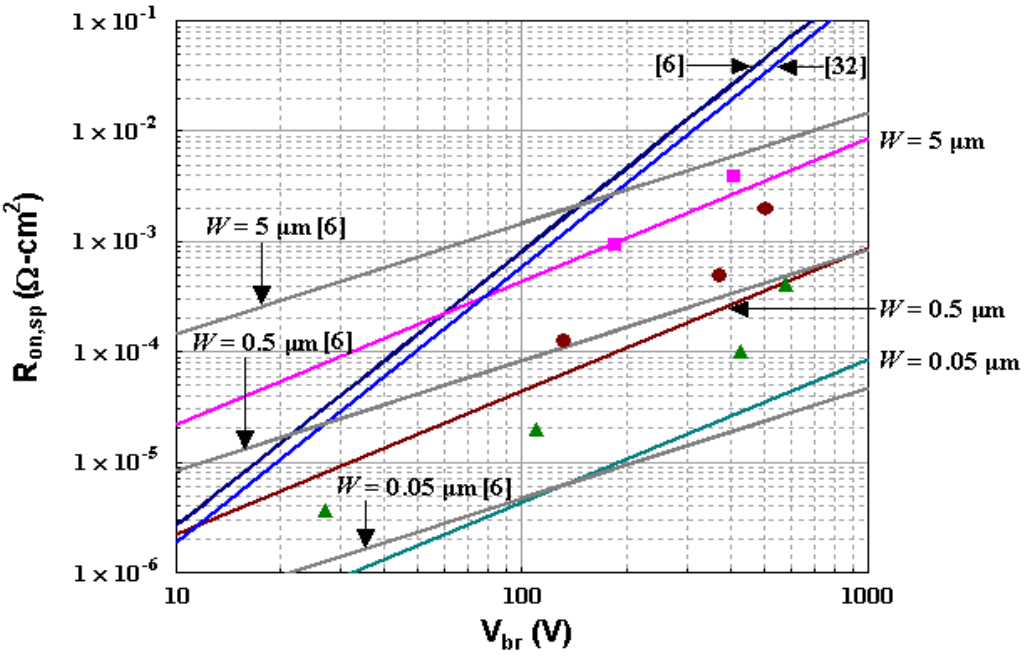


Figure 2-4: $R_{on,sp}$ vs. V_{br} relationship for ideal silicon limit [6][32] and SJ limit at W = 5µm, 0.5µm and 0.05µm according to Equation (2.24), together with SJ limit at W = 5µm, 0.5µm and 0.05µm and some simulation data extracted from [6]. The square points stand for simulated SJ MOSFETs at W = 5µm, round points stand for simulated SJ MOSFETs at W = 0.5µm and triangle points stand for simulated SJ MOSFETs at W = 0.05µm, respectively.

2.2.2 SJ characteristics at off state

Figure 2-5 shows the simulation results of SJ structure with W = 5µm and L = 15µm at different positive V_{DS} bias when V_{GS} = 0V, by using MEDICI [34]. V_{br} is simulated to be 261.1V for this structure. The doping concentration N_A and N_D for p and n column in the device simulation are exactly equal to get the ideal result. However, in the practical fabrication, perfect $N_A = N_D$ is difficult to achieve. The analysis of charge imbalance will be introduced later in Section 2.2.3 of this chapter.

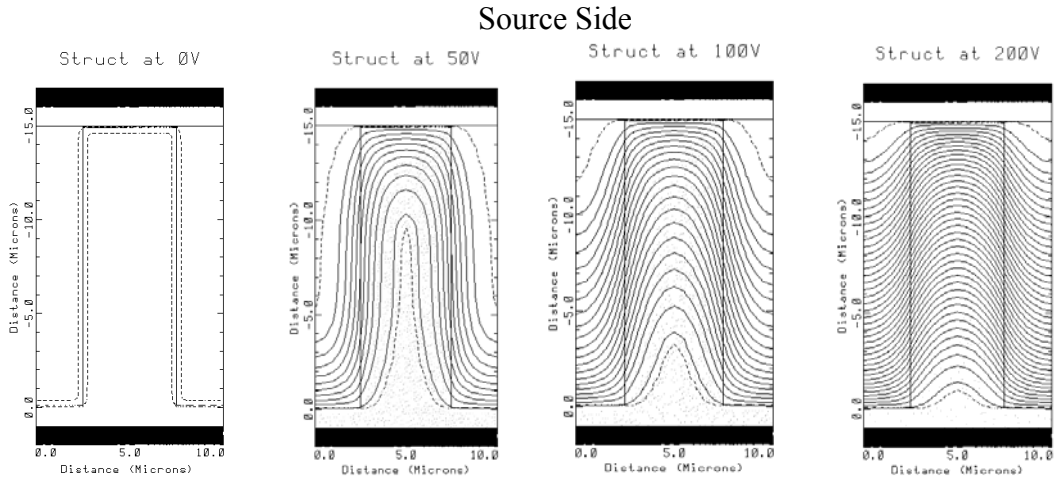


Figure 2-5: Simulation results of SJ structure at different V_{DS} bias before breakdown. (a) V_{DS} = 0V; (b) V_{DS} = 50V; (c) V_{DS} = 100V; (d) V_{DS} = 200V. The dashed lines stand for the boundary of depletion region and the solid lines stand for the potential lines at 5V interval.

When $V_{DS} = 0$ (See Figure 2-5(a)), the depletion region that results from built-in potential between p/n columns is very small. The built-in potential (V_{bi}) is approximated by

$$V_{bi} \approx \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.25}$$

From Equation (2.13) we know that for the case of $N_A = N_D = 7 \times 10^{15} cm^{-3}$, the built-in depletion width (W_{bi}) under such condition is about 0.5μm. When $V_{DS} > 0$, depletion regions start to extend. It is observed in Figure 2-5(b)~(d) that the depletion regions firstly merge on the top part of the drift region at a small bias, then move down with the increase of the bias. At the breakdown, the entire drift region is fully depleted as shown in Figure 2-6. The distributions of equal potential lines (the parallel curves shown in Figure 2-6(a)) are nearly uniform at this bias. The E-vector plots in Figure 2-6(b) represent that electric field varies obviously at the p/n column interface, especially at the top and bottom regions. Along the vertical line through the center of n-drift

region, only vertical electric field is found. The above simulation results verify the assumptions of electric field profile as in Figure 2-2.

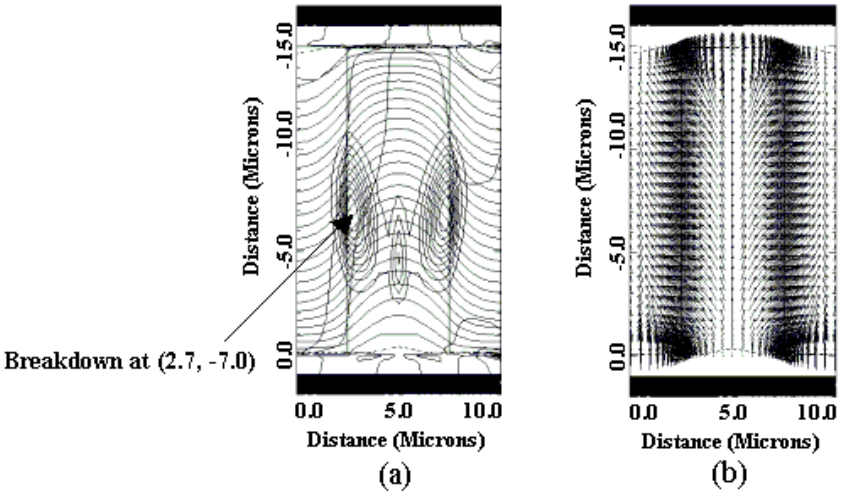
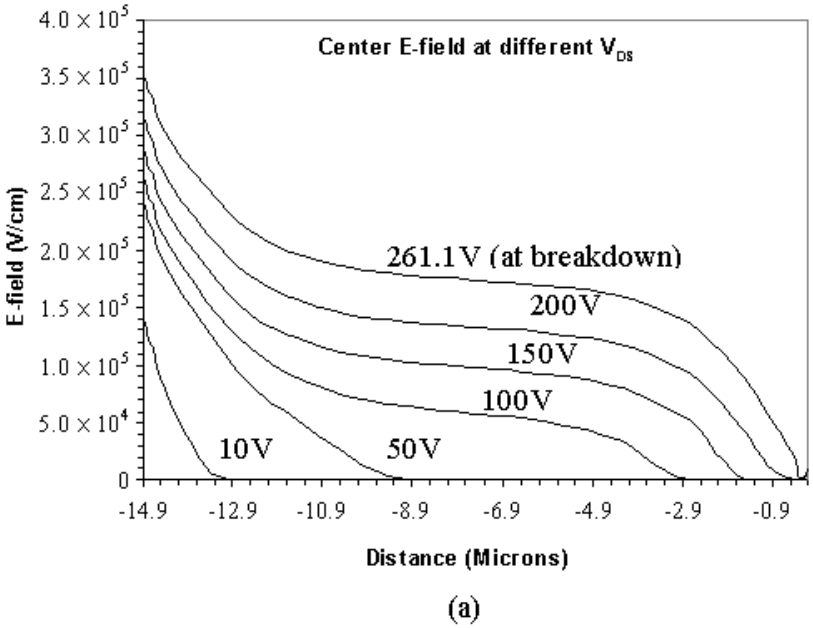
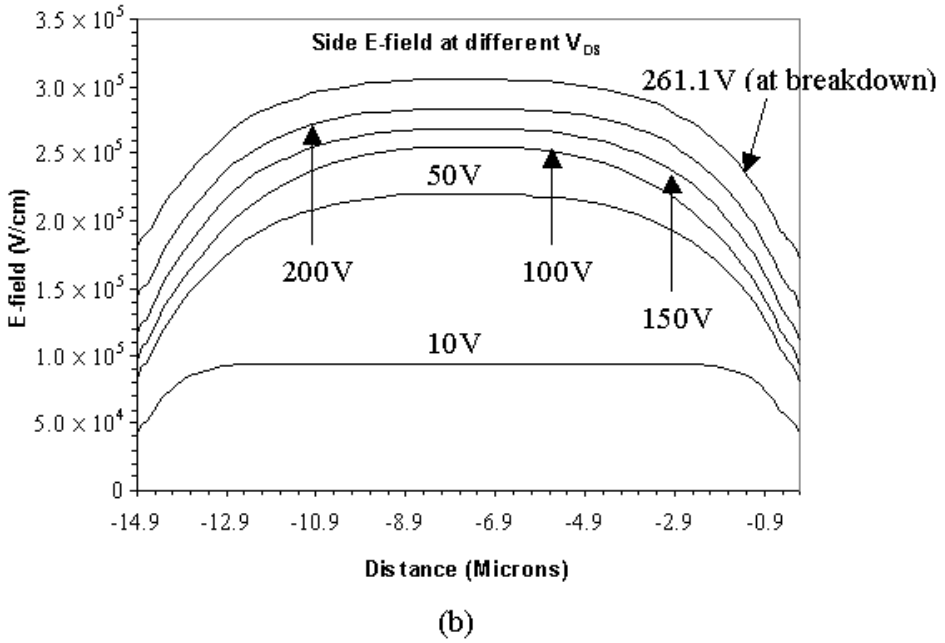


Figure 2-6: (a) Potential lines at 10V interval, impact ionization representations and (b) E-vector plots for SJ structure at breakdown

As given in Figure 2-7(a), when increasing V_{DS}, the vertical electric field profiles of SJ structure at center of n column at x = 5μm start to change from a triangle shape as in the conventional case, to more like a square disregarding the top and bottom regions. The electric field at p/n interface at x = 2.5μm, as shown in Figure 2-7(b), is almost constant at any bias but with varying magnitudes determined by the applied bias.





(b)

Figure 2-7: Electric field plots along (a) x = 5μm and (b) x = 2.5μm at different V_{DS}

2.2.3 The effect of charge imbalance for SJ devices

To utilize the benefits of SJ devices to the maximum extent, charge compensation must be satisfied, as

$$Q_n = Q_p \Rightarrow W_n \times N_D = W_p \times N_A \tag{2.26}$$

That is, the doping integral over a layer perpendicular to the current flow direction remains smaller than the specific breakthrough charge for silicon of about $2 \times 10^{12} cm^{-2}$ [7]. Thus the enhanced doping level of the current carrying n-regions results in a significant drop in resistivity.

Experiments mentioned in Reference [35] reveal that the change of V_{br} is dependant on the absolute value of the charge imbalance ($\Delta Q = |Q_p - Q_n|$), which becomes worse as ΔQ increases. The relationship between charge imbalance and the device performance is shown below:

$Q_p > Q_n \rightarrow$ Undepleted region in p column when n column is fully depleted becomes a path of current flow, which results in lower gate charge, delay time, turn-off E-field and higher peak reverse recovery current.

$Q_p < Q_n \rightarrow$ Undepleted region in n column forces the current flow through the channel, which leads to higher turn off losses.

Numerical simulations proved that the SJ device is highly sensitive to charge imbalance if designed for low on-resistance [35].

2.2.4 State of the art in SJ devices

(1) COOLMOS Technology

COOLMOS (600V) by SIEMENS is the first commercially available Si device exploiting the novel SJ concept (See Figure 2-8).

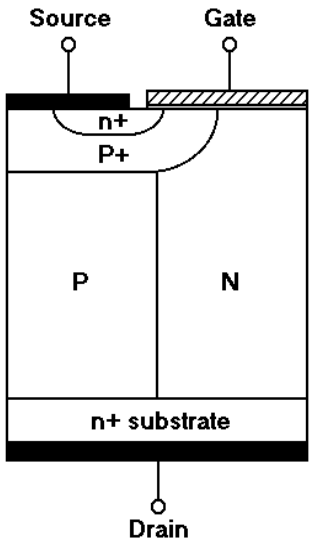


Figure 2-8: Typical COOLMOS structure

It is tested to be able to reduce the resistivity by the factor of at least 5, which leads to the reduction of the chip size in comparison of conventional MOSFETs. Because the

fall time of COOLMOS is very small due to the fast and complete removal of carriers in the charge storage time, it also competes with IGBTs in high voltage and high frequency applications, when transient losses of IGBTs become more predominant.

The most distinguished feature of COOLMOS is that multi-epitaxy technology is applied in the fabrication to achieve the precise charge balance. However, there are some drawbacks that still exist in the process [36]:

a. Large number of mask steps is required to realize fine cell pitch, which leads to high cost and complexity in the process.
b. It needs a very long time thermal treatment at a high temperature to connect vertically each buried impurity region. These long drive-in steps cause mutual diffusion of the same range in the horizontal direction for n-drift layers and p-layers resulting in compensation for the effective impurity concentration. As a result, the current flow lines of the multi-epitaxy cells are no longer straight. Consequently, $R_{on,sp}$ could not match the ideally lowest value as predicted.

(2) Super Trench Power MOSFET (STM) and Vertical Deep Trench RESURF DMOS (VTR-DMOS)

Instead of the conventional n- drift layer, STM [16] has vertical p and n layers formed within mesa regions between adjacent trenches filled with insulator, as in Figure 2-9(a). The p/n layers are made by Boron/Phosphorus tilted implant into the opposite sidewalls of the deep silicon trenches. It has $R_{on,sp}$ of 5mΩ-cm^2 @ V_{br} = 300V theoretically. The advantage of this device is that compared to multi-epitaxy technology used in COOLMOS, it simplifies the fabrication process by using only one

additional mask over the conventional DMOS process to achieve the superior performance.

The superjuction structure of VTR-DMOS shown in Figure 2-9(b) [17] is similar to that of STM, but its formation shows the difference as described in the following process sequence:

- p-well formation
- Silicon deep trench etching in n-epitaxy layer
- Thin in-situ boron-doped LPCVD PolySi deposition and Boron drive-in at 1000^0C
- 1000^0C dry oxidation to convert PolySi into SiO_2 (The conversion to SiO_2 is mandatory to prevent a leaky junction along the trench sidewall and eliminate PolySi over the surface)
- n+ implantation and TEOS filling into the trench

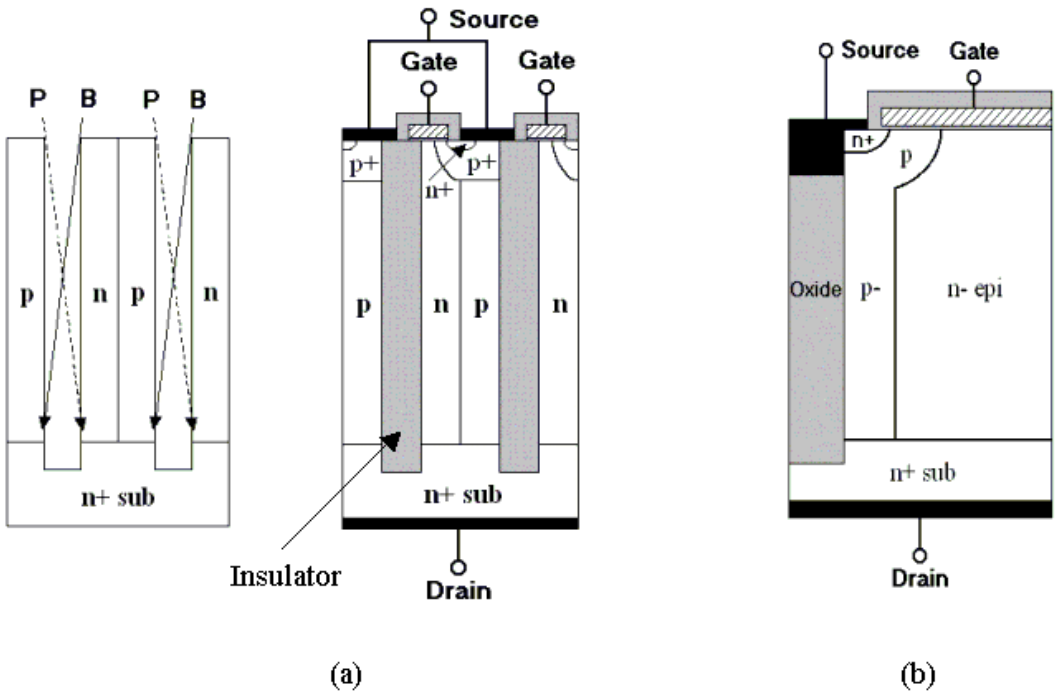


Figure 2-9: (a) STM structure and (b) VTR-DMOS structure

Device simulation results show the $R_{on,sp}$ vs. V_{br} relationship of VTR-DMOS is in the range between the best case of 25.7 mΩ-cm^2 @ V_{br} = 880V and the worse case of 26.1 mΩ-cm^2 @ V_{br} = 700V, while for conventional DMOS, it is 143 mΩ-cm^2 @ V_{br} = 710V. Therefore, by operating under the same basic principle of SJ structure, simulated $R_{on,sp}$ of VTR-DMOS has the improvement by factor of 5.5 over the conventional DMOS. There also exists a problem of VTR-DMOS that, a soft breakdown condition prevails at high drain currents, producing a non-linear drain current at high drain bias.

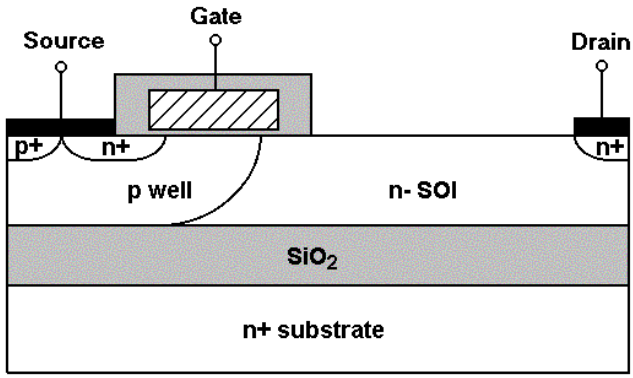
The drawbacks of both STM and VTR-DMOS are that:

a. The trench width, which takes up the conduction area of the drift region, must be at least 1.5μm to guarantee the depth of the trench and tilted implant. This problem is dominent when p/n columns become smaller. It limits the fabrication of the SJ device in low voltage application where device has small width.
b. Inter-diffusion problem cannot be solved.

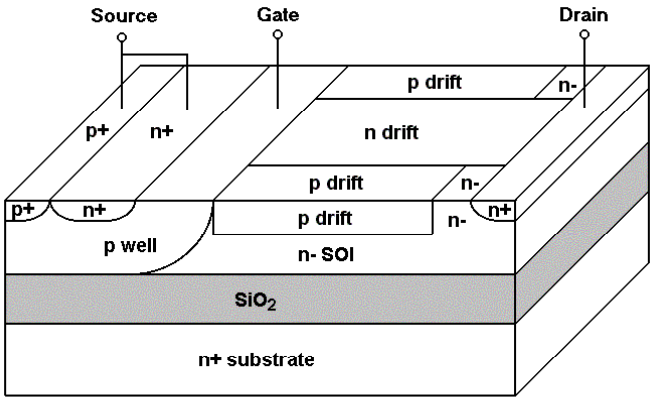
(3) Semi-Insulating Resurf Layers (SIPOS)

SJ Diode using SIPOS [37] is another implemented device by using thin oxide between superjunction p and n layers. SIPOS or so called as Polydox (PolySi Doped with Oxide) is used to fill the trench after thin sidewall oxide formation. SIPOS-SJ diode represents the enhanced breakdown voltage without the usual tight doping tolerances as in SJ devices.

(4) Superjunction LDMOS on SOI



(a)



(b)

Figure 2-10: Conventional LDMOS (a) and SJ LDMOS (b) on SOI wafer

For bulk silicon LDMOS devices shown in Figure 2-10(a), the performance is mainly limited by the inherent parasitic capacitance, especially the output capacitance. The Silicon-on-Insulator (SOI) technology is therefore attractive for RF applications.

Advantages of SOI devices:

With the SOI technique, the Gate, Source and Drain areas can be assured of minimal capacitance. The SOI circuit's capacitance will be negligible since the silicon oxide provides an efficient insulation barrier. The junction capacitance area is eliminated by

SOI, thus the transistor will be able to operate faster since the charging process is eliminated. In addition, reducing leakage current and high temperature performance compared to the traditional junction isolation are the advantages of SOI technology as well. The implementation of an LDMOS on thin-film SOI may enable the devices with improved gain, efficiency and bandwidth.

With the application of Super Junction concept on SOI LDMOS [29], the n drift region of LDMOS is replaced by a series alternating p/n stripes in lateral direction. With an insulator layer below, a nearly uniform electric field distribution can be achieved throughout the drift region despite doping levels being higher to some extent than the maximum allowable values limited for conventional LDMOS on bulk silicon.

Drawbacks of SOI devices:

There exist inherent thermal dissipation and floating body problems in the conventional SOI technology as Oxide blocks heat and carrier flow. Heat dissipation is still the problem on the application of SJ SOI MOSFETs.

Published SJ SOI LDMOS:

As shown in Figure 2-10(b), by exploiting the SJ concept into the LDMOS, n type drift region is replaced by a series of alternating stripes of opposite impurity content, such as [26-27, 29-30]. Such an arrangement allows the interesting possibility of extending the RESURF action to the third dimension whilst maintaining the original RESURF in the vertical direction. Hence a near uniform electric field distribution is achieved throughout the drift region despite doping levels being somewhat higher than the maximum permissible values limited by conventional LDMOS on bulk silicon.

Recently, SJ LDMOS in Silicon-On-Sapphire Technology [28] has been designed to alleviate the thermal problem existing in SOI SJ LDMOS.

2.2.5 PolySi Flanked VDMOS (PFVDMOS)

In order to overcome the high fabrication costs and complicated process of 600V COOLMOS^{TM} device as well as the inter-diffusion problem of SJ structure, a technology of PFVDMOS is introduced and demonstrated to have greatly reduced fabrication costs, simplified process and overcome the inter-diffusion problem of SJ columns. The simulation and fabrication of PFVDMOS [24, 38] were done successfully with the cooperation of Institute of Microelectronics, Singapore (IME). It has been proven to break the conventional MOSFET silicon limit. The full PF structure is given in Reference [24]. As it is symmetric, only part of the structure with the edge termination is shown in Figure 2-11. To minimize the inter-diffusion problem in SJ devices, thin oxide film is grown between alternating p and n columns. This thin oxide structure is obtained by etching a trench in n-epi layer and followed by dry oxidation. The oxide on the top and bottom surfaces is removed and the thin oxide is left only on the trench sidewall.

To achieve uniform doping for p poly column, Boron tilted implantation into the conformal poly layer, poly refill and poly drive-in are carried out subsequently in that order. Finally, the poly is etched back with slight over-etch to ensure that all Polysilicon is removed from the active n-epi region. The subsequent fabrication steps are the same as those of conventional VDMOS case applied to the n-epi columns. Thus, both high doping concentration and smaller column width are now achieved in alternating p and n layers to improve on-resistance while maintaining the blocking

voltage. Clearly, instead of complex multi-epitaxial growth, this process uses relatively simple steps of etching, deposition, implantation and poly-fill.

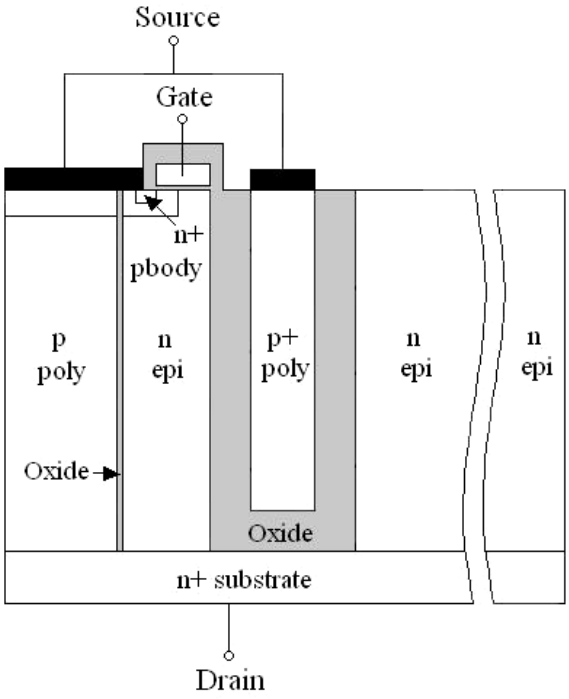


Figure 2-11: Part PFVDMOS structure with edge termination

Another feature of PFVDMOS is that by using the concept behind Oxide-Bypassed devices (will be described later in next chapter) for SJ termination, the thick oxide in termination region provides a region to sustain a high blocking voltage by depleting the n column sidewall. Therefore, pre-mature breakdown caused by the high electric field at n epi edge of the device can be prevented. This brings forth the new milestone that SJ MOS-devices can now be fabricated by the standard cleanroom facilities.

Device simulation by TSUPREM4 [39] and MEDICI [34] and measurement results of fabricated PFVDMOS devices represent the superior performance over conventional VDMOS. At the same blocking voltage of 240V, doping concentration of drift region of PFVDMOS ($N_d = 7 \times 10^{15} cm^{-3}$) is much higher than that in conventional VDMOS

($N_d = 1.21 \times 10^{15} cm^{-3}$). However, it was found that measured I_{DS} /V_{DS} curve of PFVDMOS at off state shows high leakage current compared to that of the conventional VDMOS, which was fabricated on the same wafer.

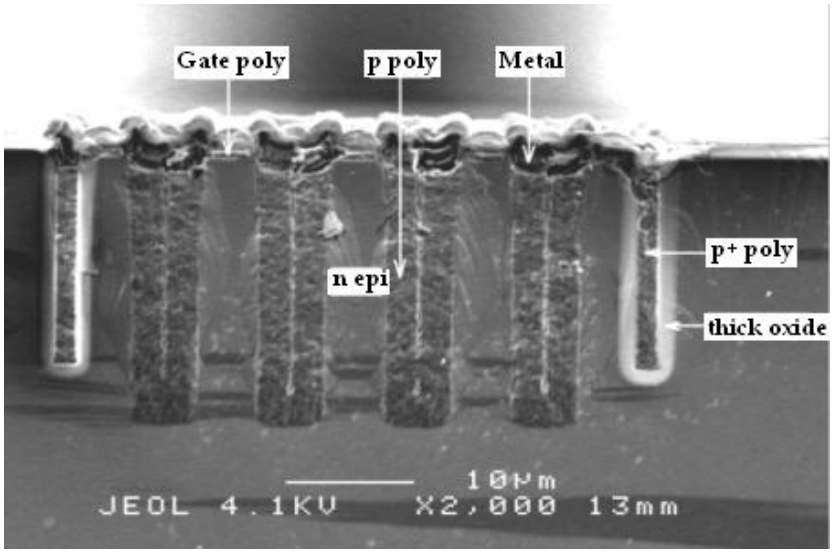


Figure 2-12**:** SEM picture showing PFVDMOS with thick Oxide-Bypassed termination

The SEM picture of PFVDMOS is shown in Figure 2-12. With minimized inter-diffusion because of the thin Oxide barrier between p/n columns, high doping concentration is allowed in alternating p and n layers to improve on-resistance while maintaining the blocking voltage. To avoid the premature breakdown happening at the edge of the device, an edge termination with thick oxide and doped poly in between is formed. The doped poly is directly connected to Source electrode of the device.

The Gate and Source pads are placed on a thick trench oxide beside the active region of the device. This thick oxide is used to support a high voltage applied on the pads. Figure 2-13 gives the SEM picture of 15µm-depth-2.5µm-width multiple trenches. The distance between two neighbor trenches is 1.2µm. Steps of wet oxidation and oxide deposition are followed to make a whole cubic oxide region.

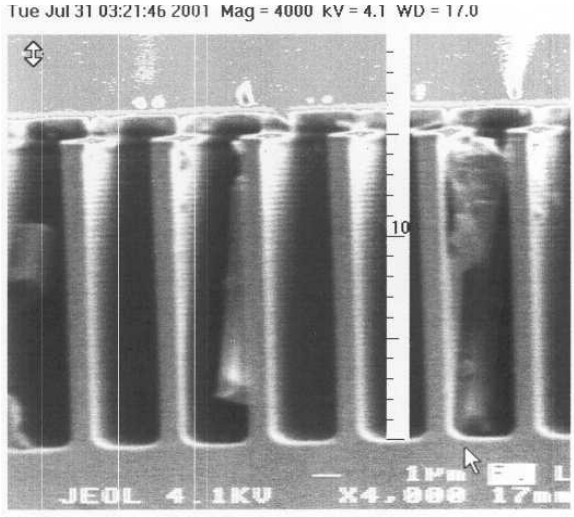


Figure 2-13: SEM picture for multiple trenches under the pad

Measured blocking voltage (V_{br}) of PFVDMOS is 187V, which is 3.4 times than that of conventional VDMOS (55V) at the same epi doping concentration of $N_d = 7 \times 10^{15} cm^{-3}$. At V_{GS} = 10V, measured $R_{on,sp}$ of PF-VDMOS is 3.68 mΩ-cm^2 with V_{br} = 187V, which is lower than the silicon limit of 3.97 mΩ-cm^2 at the current density of 100 A/cm^2.

However, there are some problems for the fabricated PFVDMOS:

1. Measured V_{br} of PFVDMOS is 22% lower than the simulated result.
2. High off state leakage current compared to the conventional MOSFET fabricated on the same wafer.

The problems above can be explained by several possible reasons:

1. The process sensitivity of charge imbalance. It is clear that, for designed PFVDMOS structure with V_{br} = 240V, V_{br} is reduced when the mismatch ratio goes up. Charge imbalance of ±10% results in 22% reduction of V_{br}. In device fabrication, this mismatch phenomenon most likely happens because the

doping profile in p poly is sensitive to the angle of tilt implantation and it is difficult to control the incident angle accurately.

2. Due to not so optimized process, the real trench oxide in edge termination of PFVDMOS does not go deeper than the poly trench. This non-optimum edge termination of PFVDMOS probably causes premature breakdown.
3. High leakage current of PFVDMOS is probably due to charge trapping effect in Polysilicon grain boundary. Therefore, large grain size of Polysilicon is required. This maybe achieved by longer annealing time and passivating the dangling bonds at the grain boundaries with dopants or hydrogen impurities. Oxygen-Doped Polysilicon, which is known as SIPOS, is a good candidate replacing Polysilicon for p column formation.
4. Top pad passivation maybe another reason for high leakage current of both PFVDMOS and conventional MOSFET.

Figure 2-14 gives the $R_{on,sp}$ vs. V_{br} performance of published VDMOS devices. Since most of the SJ devices are designed for high blocking voltages, PFVDMOS at 200V range becomes more attractive. The fabricated PFVDMOS still can break the ideal silicon limit. By carefully optimizing process parameters, performing proper checking during fabrication and using some feasible processing method, most of the problems above can be alleviated to achieve the superior performance of the device.

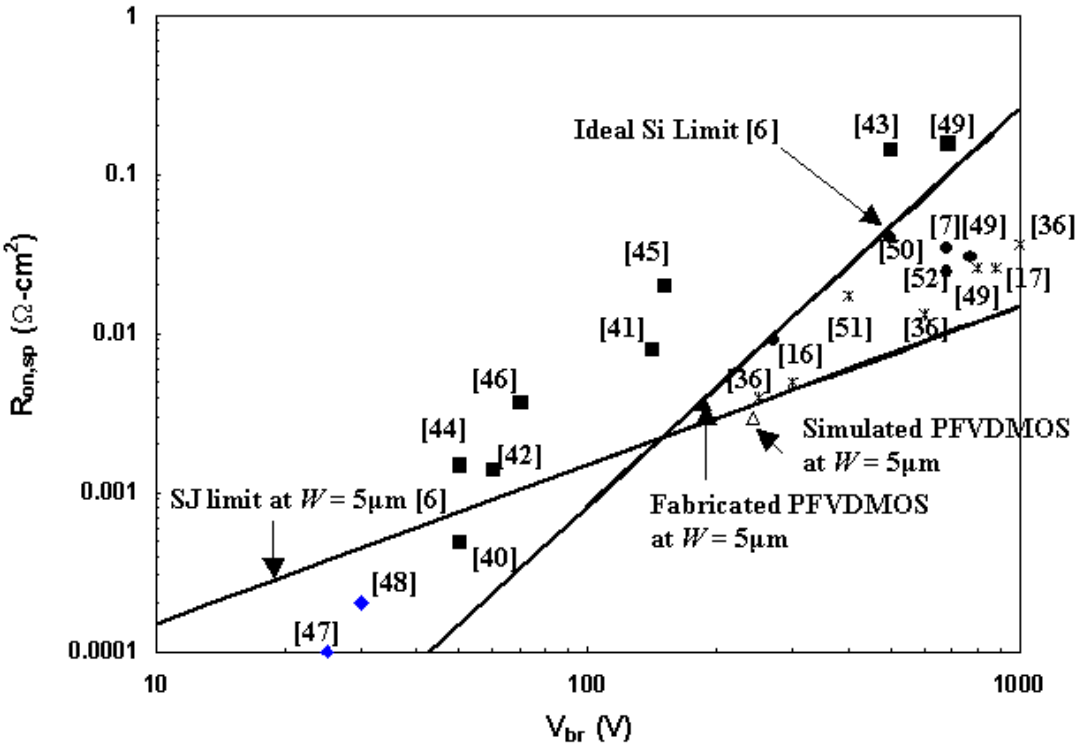


Figure 2-14: $R_{on,sp}$ vs. V_{br} performance of PF-VDMOS compared to ideal silicon MOSFET limit [6], superjunction structure at n/p column width W = 5 µm [6], and the previous work on VDMOS and SJ devices extracted from [7, 16, 17, 36, 40-52].

Chapter 3

Oxide Bypassed MOSFETs

It has been recognized that the SJ structure is attractive for power devices because of its high blocking ability. However, the performance of SJ devices is handicapped in reality by the realization of charge balance as mentioned in last chapter. So far the ideal charge balance in SJ p/n columns cannot be realized due to current fabrication technologies. The introduction of Oxide Bypassed (OB) MOSFETs [24] is to overcome the difficulties mentioned above. It has been found that if the p column of SJ structure is replaced by a thick oxide layer together with a Polysilicon layer beside, the new structure obtained still has high breakdown voltage compared to conventional MOSFETs. In this chapter, basic theory and research efforts on OB structure will be presented. Proposed OB MOSFETs will be studied in details.

3.1 Fundamental of Oxide Bypassed MOSFETs

The concept of Oxide Bypassed structure was proposed in Reference [24]. The simulation models of OBVDMOS and OBUMOS are shown in Figure 3-1. Compared to SJ MOSFETs, the OB structure is accomplished by using a deep trench beside the n-drift region. Along the trench wall, there is a thick oxide layer filled with highly doped Polysilicon, which is shorted to the Source Electrode of the MOSFET.

Therefore the OB region contains the thick oxide layer and the Polysilicon in between the oxide layers. This OB structure is to help depleting the n column and thus enhance the breakdown voltage.

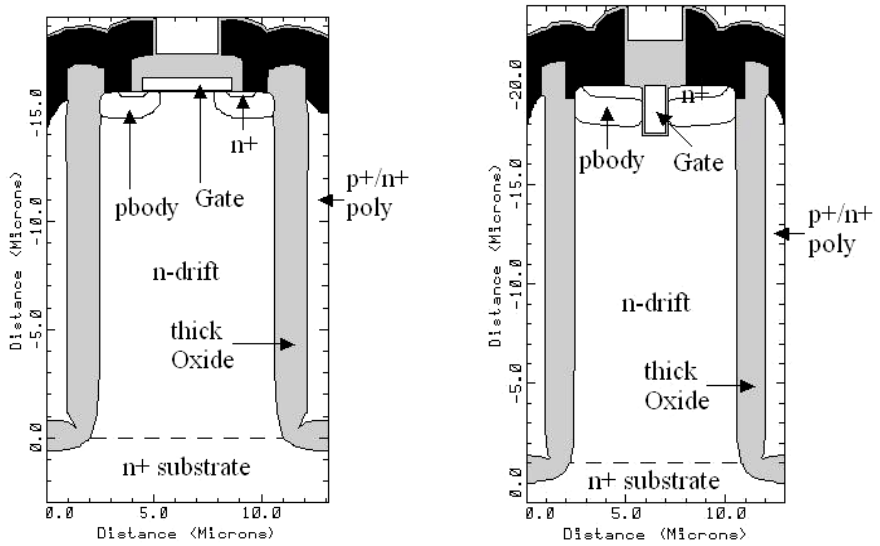


Figure 3-1: Simulation Models of OBVDMOS (left) and OBUMOS (right)

Under reverse bias, the depletion layer starts to expand from the oxide/silicon interface. With increasing reverse bias, the depletion layer expands into the n-drift region, and at a certain voltage, the drift region becomes fully depleted. The OB structure reduces the electric field at drift region, which results in the higher breakdown voltage. Obviously, OB structure functions like the p column of SJ devices. Experiments show that the breakdown voltage (V_{br}) depends on the oxide thickness (t_{ox}), the impurity concentration (N_d) and width (W) of the drift region between two neighboring thick Oxide layers.

The Si/Oxide/PolySi structure can be treated as a parallel-plate capacitor. That is, the voltage drop on both sides of thick Oxide can be obtained by:

$$V = \frac{Q}{C} = \frac{Q \cdot t_{ox}}{A \cdot \varepsilon_{ox}} = \frac{qN_d \cdot W \cdot t_{ox}}{2\varepsilon_{ox}} \tag{3.1}$$

where Q is the charge of the capacitor, C is the capacitance and ε_{ox} is the permittivity of Oxide.

When breakdown happens, the OB structure should have already depleted the charge in the whole n-drift region. Thus, solving Equation (2.6) and (3.1) by equating V to V_{br}, optimized OB structure should follow the approximal relationship as [24]:

$$N_d = 2.90 \times 10^{11} \cdot [t_{ox} \cdot \frac{W}{2}]^{-4/7} \tag{3.2}$$

The SEM picture of OBUMOS is shown in Figure 3-2. This 1.5μm thick MTO structure provides a region for sustaining high voltage while the field effect exerted by the metal electrode helps to deplete the n column laterally. Owing to this additional lateral depletion, the doping in the n region can be raised to a value comparable to those in SJ devices and thus overcoming the conventional limit. Precise matching of doping is not required in this device.

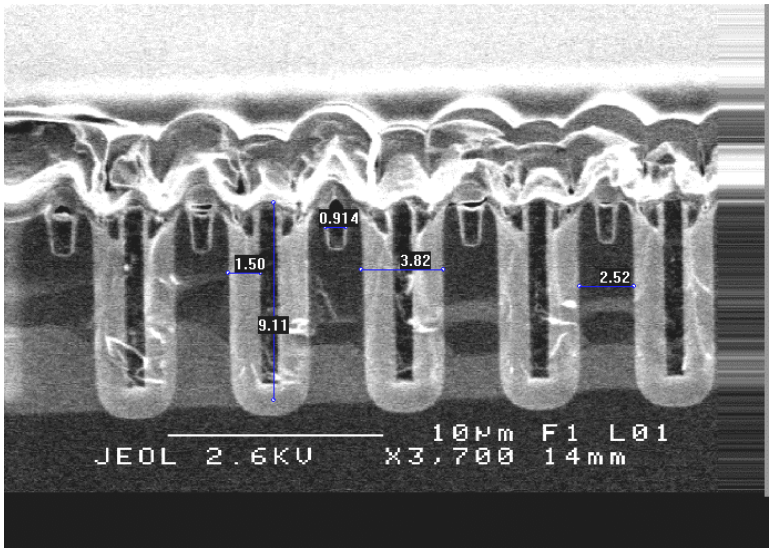


Figure 3-2: SEM picture of fabricated OBUMOS with t_{ox} = 1.5μm.

However, due to some fabrication process problems, OB-MOSFETs with superior performance of OB theory haven't been obtained yet. Only OB-PiN diode with 1μm thick oxide fabricated on a 7×10^{15} cm^{-3} n-epi starting wafer is able to verify the blocking capability of OB structure [25]. It is proven that, measured V_{br} for the OB

structure is 2.5 times that of conventional structure at 67V. A $R_{on,sp}$ reduction of about 2 times is thus predicted for OB device at similar voltage rating after taking into account the reduction in conduction area due to the sidewall Oxide.

3.2 Some efforts on OBUMOS improvement

3.2.1 Width variations of n-drift region

According Equation (3.2), we know that at a certain doping concentration N_d, oxide thickness t_{ox} is inversely proportional to W, to maintain the same breakdown voltage of the device. Therefore, one way to enhance the on-state performance of the OBUMOS is to increase the width (W) with correspondingly decreasing t_{ox}. Hereby, three different widths ($W/2$) of 2μm, 4μm and 6μm for half drift region are applied to OBUMOS and comparisons are made at the similar breakdown voltage of about 250 Volts.

Simulation results give the relationship of W, t_{ox} and V_{br}. For $W/2$ = 2.05 μm, t_{ox} = 0.8042 μm, V_{br} is 240.0V. For $W/2$ = 4.07 μm, t_{ox} = 0.9847 μm, V_{br} is 251.3V, while for $W/2$ = 6.07 μm, t_{ox} = 1.1296 μm, V_{br} reaches 258.6V. It is also established by simulation that, the transconductance (G_m) and Unity-gain frequency (F_T) of large OB devices are better than the smaller ones.

However, the application of this method is limited by the condition of low doping concentration (N_d) of the drift region. Simulation shows that at low N_d of 1×10^{15} cm^{-3}, the relationship between t_{ox} and W is fitted well (see Figure 3-3). We know that at N_d = 1×10^{15} cm^{-3}, conventional silicon limit of breakdown voltage is 300V. Though we can predict that when t_{ox} is higher than 2μm, the simulation result of V_{br} can be higher

than 300V, thus to overcome the silicon limit. In true fabrication, the maximum oxide thickness that can be grown in wet oxidation is around 1.5μm. Though using multiple Silicon trenches can realize a very thick oxide, the shape and thickness of the oxide is difficult to be controlled.

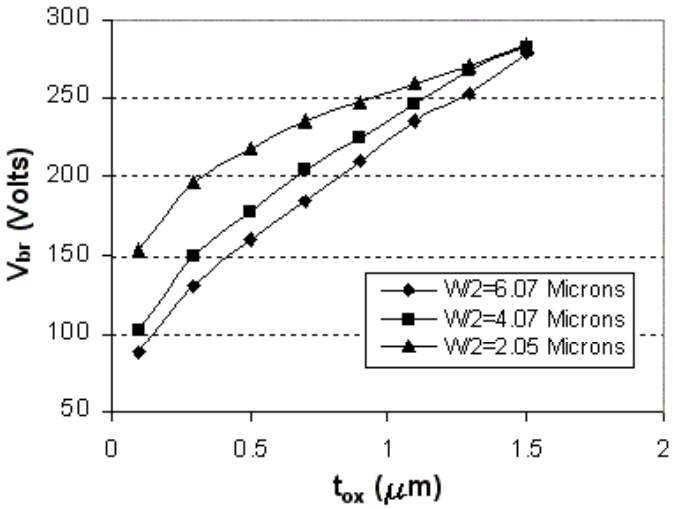


Figure 3-3: Comparisons of reverse breakdown voltage vs. Oxide thickness (t_{ox}) with different width of OBUMOS n-drift region (W), at $N_d = 1\times10^{15}$ cm^{-3}

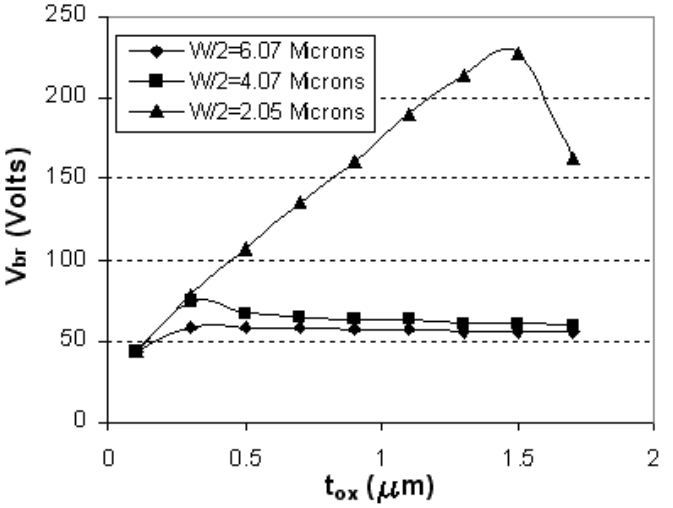


Figure 3-4: Comparisons of reverse breakdown voltage vs. Oxide thickness (t_{ox}) with different width of OBUMOS n-drift region (W), at $N_d = 7\times10^{15}$ cm^{-3}

At higher N_d of 7×10^{15} cm^{-3}, t_{ox} and W no longer follow the inverse relationship to maintain the high breakdown voltage, as shown in Figure 3-4, because large dimension

will prevent the pinch of depletion region and lead to the premature breakdown. In addition, device with large *W* is not suitable for circuit integration. Therefore, it is not a practical way to improve on-state performance.

3.2.2 Effects of graded doping concentration in the drift region

The previous analysis is based on the uniformly doped n-drift region. It is confirmed that with a non-uniform doping profile in the drift region of a vertical MOSFET, the on-resistance can be reduced. If $N_d(y)$ is the doping profile that will minimize the on-resistance of the drift layer, the optimum doping profile of conventional MOSFETs is known to be [32]:

$$N_d(y) = \frac{\varepsilon_s E_{crit}^2}{3qV_{br}\sqrt{1-(2E_{crit}y/3V_{br})}} \tag{3.3}$$

According to this Equation, the doping concentration must increase from the surface towards the interface between the drift layer and the n+ substrate.

Using this doping profile, the specific on-resistance is given by:

$$R_{on,\min} = \frac{3V_{br}^{\ 2}}{\varepsilon_s \mu_n E_{crit}^3} \tag{3.4}$$

where E_{crit} is the critical electric field for breakdown. This specific on-resistance is 8/9 that of conventional MOSFETs with the uniformly doped profile [33].

For OB structure, another advantage of this graded doping concentration is to adjust the E-field to enhance the breakdown voltage. As we know that, in SJ devices with uniform doping concentration, because of the symmetric alternative p/n columns, equal potential lines are nearly flat and uniformly distributed, which results in a constant

vertical E-field. While in OB devices, the vertical E-field has two peaks at the top region and near the OB trench bottom, respectively. Especially, the breakdown always happens at the bottom region where the E-field peaks. If the doping profile is gradually increased from the top surface to bottom as described in Equation (3.5), a uniform vertical E-field can be achieved [47]. Therefore, an improved breakdown voltage will be obtained compared to ordinary OB devices with uniform doped drift region. For OB structure, $N_d(y)$ can be shown to be

$$N_d(y) = \left[\frac{\varepsilon_{si}}{\frac{qm}{2}\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} + \frac{m}{4}\right)} \right] \cdot \left(\frac{V_{br}}{d - t_{ox}} \right) \cdot y \qquad (3.5)$$

One feasible way to implement the above concepts is to grow a number of epitaxial layers with different doping step by step. In such a way, the fabrication difficulty is proportional to the epi thickness required for the device. Nevertheless, this method is inapplicable for vertical Power MOSFET with deep drift region up to above 10μm.

Fortunately, by applying the graded doping profile on the lower part of OBUMOS drift region only, the on-resistance and blocking capability can also be improved none the less. Actually, after undergoing the thermal process, the dopant from highly doped substrate diffuses into drift region. As a result, a graded doping profile occurs due to the dopant redistribution. In this case, only one more epi layer needs to be added in between original drift region and substrate, serving to generate the required doping profile after process. Simple simulation was done on OBUMOS by raising the doping concentration gradually, from the center of drift region to the bottom.

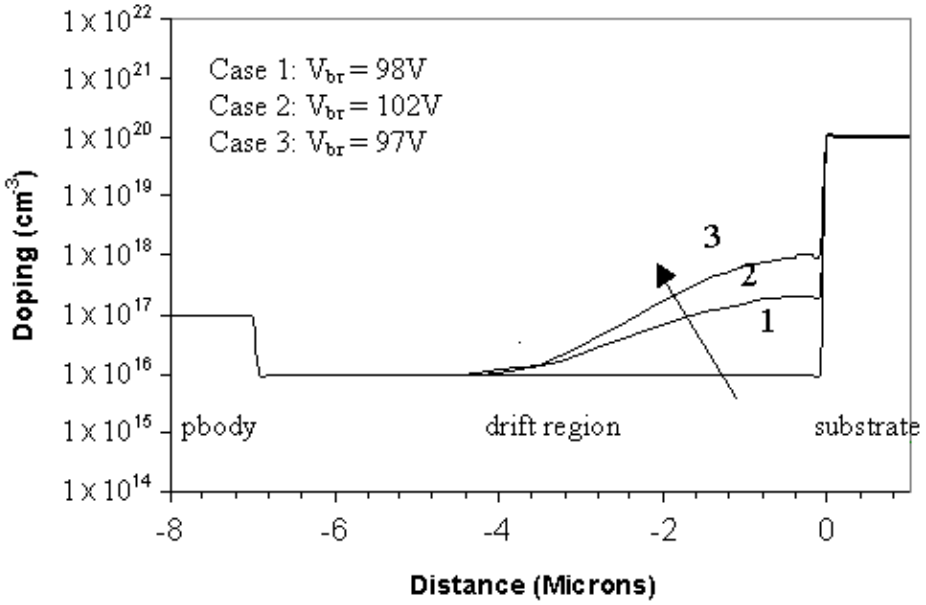


Figure 3-5: Plot of doping profile along n-drift region of OBUMOS

The doping at the top region maintains the same value as in optimum OBUMOS as shown in Figure 3-5. Obviously, the on-resistance is lower because of the higher doping at the nether drift region. According to the off-state simulation, it is proven that, by properly adjusting the doping profile, breakdown voltage is maintained.

3.3 Tunable Oxide Bypassed MOSFETS

Based on the established OB theory, further research is going on to improve the performance of OB devices. In the standard OBUMOS structure, poly contact of the Oxide-Bypass, p-body and n+ Source are all shorted using a metal line. However, if the poly contact is separated, it potentially provides an additional control voltage that can affect the device performance.

3.3.1 Introduction of Tunable Oxide Bypassed (TOB) Structure

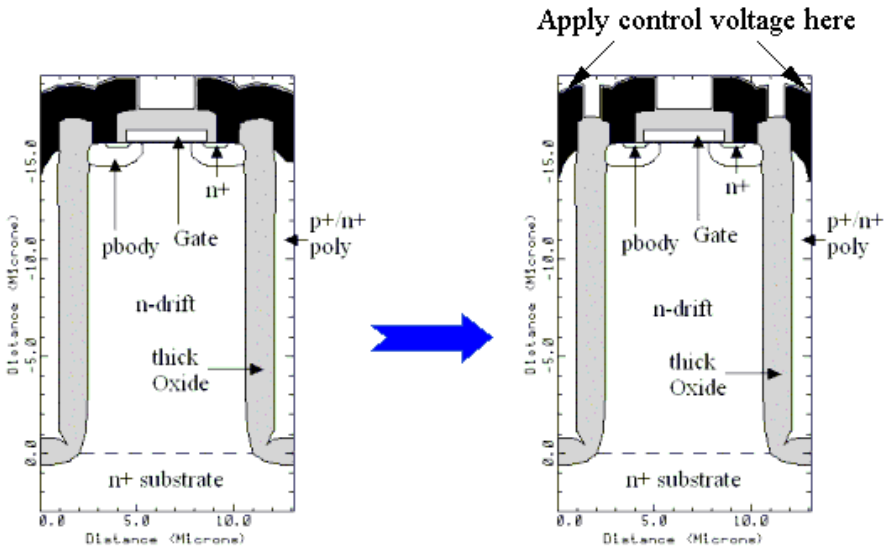


Figure 3-6: Comparisons of OB-VDMOS (left) and TOB-VDMOS structures (right)

In Figure 3-6, both of OB-VDMOS and TOB-VDMOS structures are shown. For the current work, we discover that the blocking voltage, on-state resistance and transconductance (G_m) of the OB structure can be tunable if an external voltage is applied at the poly contact, namely Control electrode, to vary the electric field at the thick oxide sidewall. This discovery enables the OB-device to have the V_{br}~$R_{on,sp}$ position moving further away from the ideal silicon limit line for a higher blocking voltage, and at the same time a higher and wider G_m for small signal amplifier applications.

3.3.2 Simulation on TOBVDMOS

(1) Off state

Table 3-1 gives V_{br} and the breakdown point coordinates in the device where it occurs at different control voltage from 0V to 100V, for TOBVDMOS with W = 8 μm, N_d =

2×10^{15} cm^{-3} and t_{ox} = 1.5 μm, where W is the width of n drift region, N_d is the impurity doping concentration of drift region and t_{ox} is the Oxide thickness of OB structure.

Table 3-1: V_{br} and the breakdown point at different control voltage from 0V to 100V

Control Voltage (Volts)	V_{br} (Volts)	Breakdown point (μm, μm)
0	**199.3**	**(10.8, -0.76)**
10	208.8	(10.8, -0.76)
20	218.2	(10.8, -0.76)
30	227.7	(10.8, -0.76)
50	246.6	(10.8, -0.76)
60	**256**	**(10.2, -14.3)**
80	131.5	(10.2, -14.3)
100	81.0	(10.4, -14.3)

It is clear that, with the increase of control voltage, V_{br} increases at first, and then drops. This is because, under the reverse bias, the electric potential at Drain electrode is higher than that at Source electrode. The positive control voltage provides an additional electric field in a direction opposite to the original one, to partially counteract the influence from the reverse bias. But the increasing control voltage also squeezes the depletion region into upper part of the n-drift region. This increases the electric field near p-body-n-drift junction. Therefore, the breakdown voltage of the device is enhanced when the electric field near p-n junction is not too high, and it drops afterwards while this electric field reaches the critical value.

Figure 3-7 shows the structures at breakdown for TOBVDMOS at different control voltage of 0V, 50V, 60V and 100V. In each simulated structure, regularly parallel curves represent the potential lines at 10V interval, while black curves gathering at certain place in drift region stand for the impact ionization at breakdown. It is obvious that for OB device without control voltage, breakdown happens at the Silicon/Oxide interface near the corner of OB structure. For TOB devices, when increasing control voltage, there are more potential lines gathering around pbody region, which leads to

the rise of electric field. Final breakdown results from the impact ionization at the location right below p body.

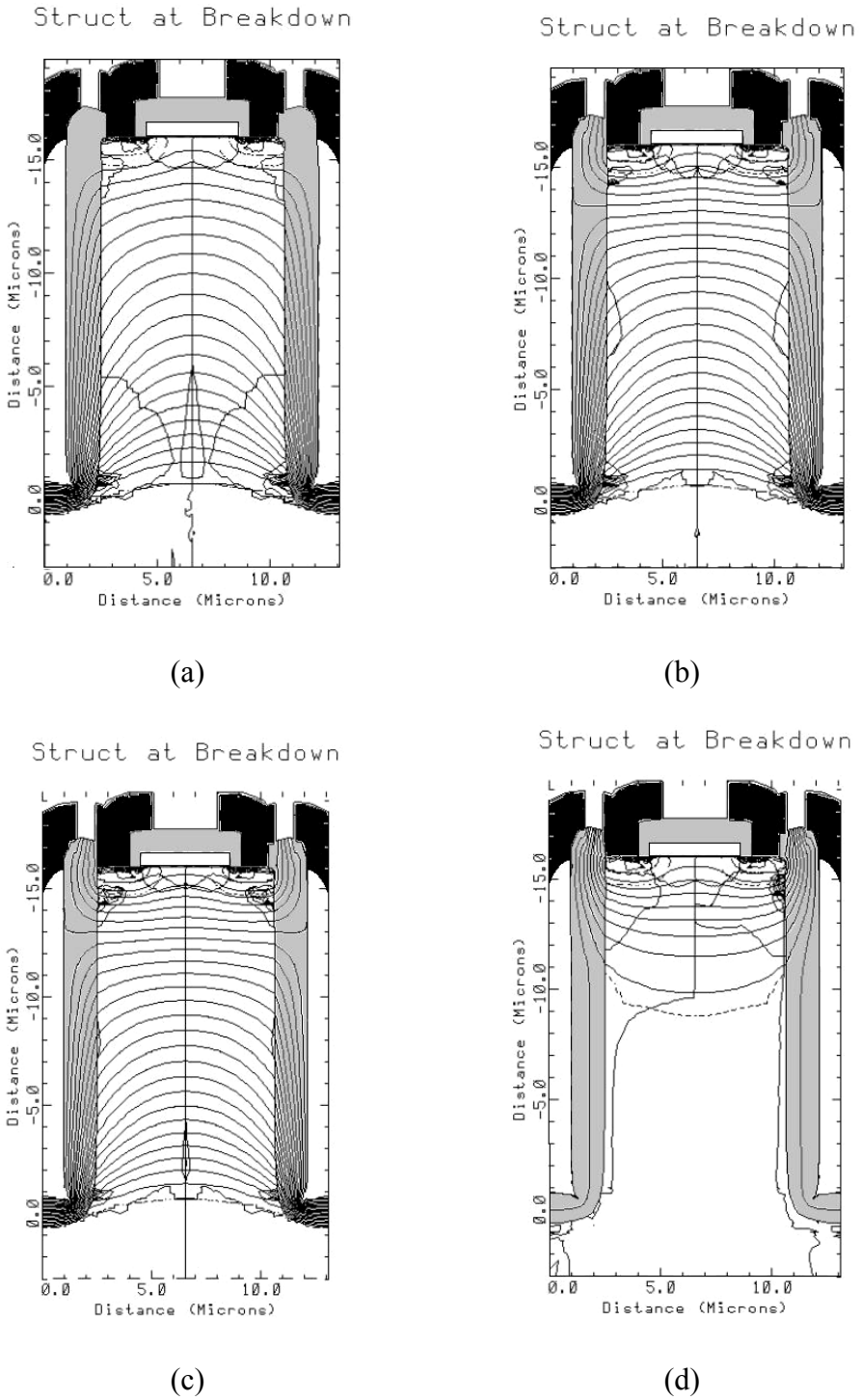


Figure 3-7: Structures at breakdown for TOBVDMOS at different control voltage of (a) 0V, (b) 50V, (c) 60V and (d) 100V.

(2) On state

When the device is at on state, a vertical accumulation layer is formed at the interface between MTO and n-drift region due to the lateral electric field produced by the additional positive control voltage. This accumulation layer provides additional path for the current flow in the drift region, and results in the reduction of on-resistance. Simulations have shown that, for TOBVDMOS with W = 8 μm, $N_d = 2\times10^{15}$ cm^{-3} and t_{ox} = 1.5 μm, specific on-resistance is 5.26 mΩ-cm^2 without control voltage and 4.58 mΩ-cm^2 at 60V control voltage.

3.3.3 Investigations on 200V TOBUMOS

(1) Structure description

In this project, UMOS was selected to be the basic device for the application of TOB structure. The advantages of UMOS structure compared to VDMOS structure are:

(a) UMOSFETs structure may reduce the resistance contributions from the channel region, the accumulation layer, and the JFET regions as in VDMOSFETs.
(b) UMOSFETs can be fabricated with a small cell size because of the absence of the JFET region. This allows obtaining a much higher channel density than in VDMOSFET structure.
(c) In consideration of the tunable characteristic on OB devices, UMOSFETs with vertical channel are better than VDMOSFETs.

Similar to TOBVDMOS design aforementioned in Figure 3-6, half TOBUMOS structure using trench gate is shown in Figure 3-8. Instead of connecting the

Polysilicon located beside MTO to Source in OBUMOS, we define an additional electrode named Control electrode, which is separated from Source electrode.

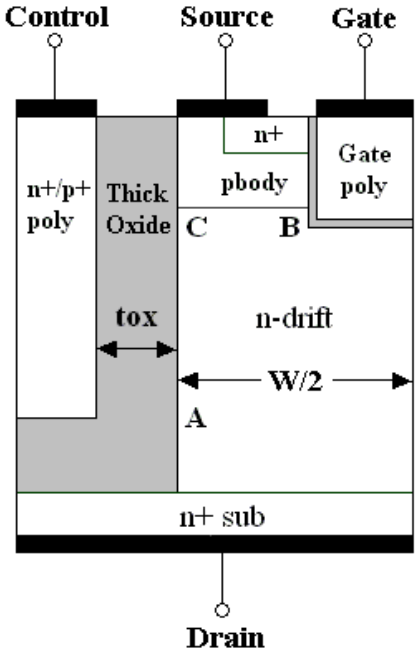


Figure 3-8: Schematic structure of half TOBUMOS

(2) Simulations and Analysis:

(a) Off state performance

Simulation was done on the device with $N_d = 3\times10^{15}$ cm^{-3}. The results in Figure 3-9 show that there is a linearly increasing relationship between Control bias and V_{br} when the positive bias is less than 60V, and V_{br} goes beyond the limit of optimized OBUMOS if Control bias is larger than 40V. Beyond Control bias of 60V, there is a sharp decrease in V_{br} until the bias reaches 80V and then a smooth and linear decrease in V_{br} continues when the bias is above 80V.

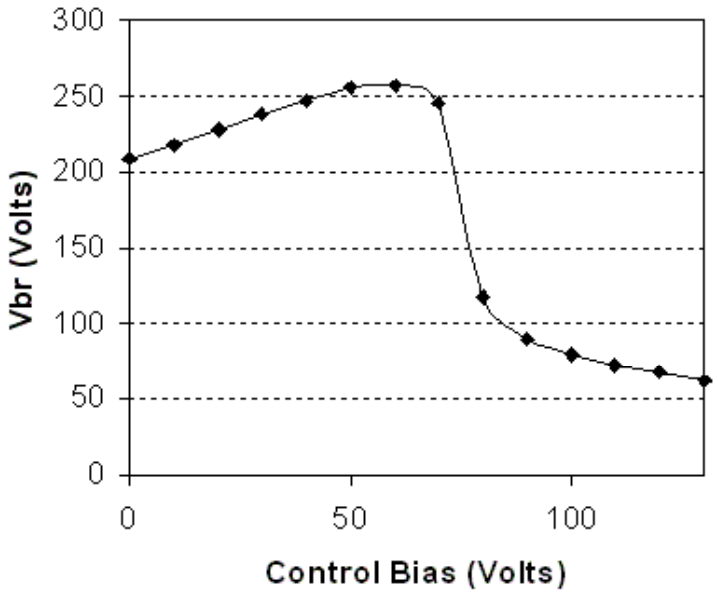


Figure 3-9: V_{br} vs. Control bias for the high-voltage tunable OBUMOS ($N_d = 3\times10^{15}$ cm^{-3}), at t_{ox} = 1.5μm and $W/2$ = 1.5μm.

The simulation results also indicate that, during off state, the breakdown for OB-structure at 0V Control bias occurs at position A (see Figure 3-8). At positive Control bias, the electric field on the top of the structure becomes higher. This induced electric field helps to decrease the field effect between Drain and Source, thus further increases the breakdown voltage. When the bias is less than 60V, the increase of V_{br} is approximately proportional to the increase of the Control bias. When the bias reaches the critical gate breakdown electric field, breakdown point moves from point A to point B. Further increasing the positive bias, breakdown point finally shifts to point C. This shift of breakdown point occurs because the increasing Control bias squeezes the depletion region into upper part of the n-drift region. This increases the electric field near P-body-n-drift junction leading to a lower V_{br}. Table 3-2 gives the relationship of V_{br}, $R_{on,sp}$ and breakdown location under different Control bias for TOBUMOS with N_d = 3×10^{15} cm^{-3}.

Table 3-2: Relationship of V_{br}, $R_{on,sp}$ and breakdown location listed under different Control bias for TOBUMOS with $N_d = 3\times10^{15}$ cm^{-3}.

Control Bias (V)	V_{br} (V)	$R_{on,sp}$ (mΩ-cm^2)	Breakdown Location
0	208.2	4.9	A
10	218.0	4.3	A
20	227.9	4.0	A
30	237.7	3.8	A
40	247.2	3.6	A
50	255.3	3.4	A
60	257.0	3.3	A
70	245.9	3.2	B
80	118.3	--	B
90	90.3	--	B
100	79.7	--	B
110	72.7	--	B
120	67.0	--	B
130	61.8	--	C

(b) On state performance

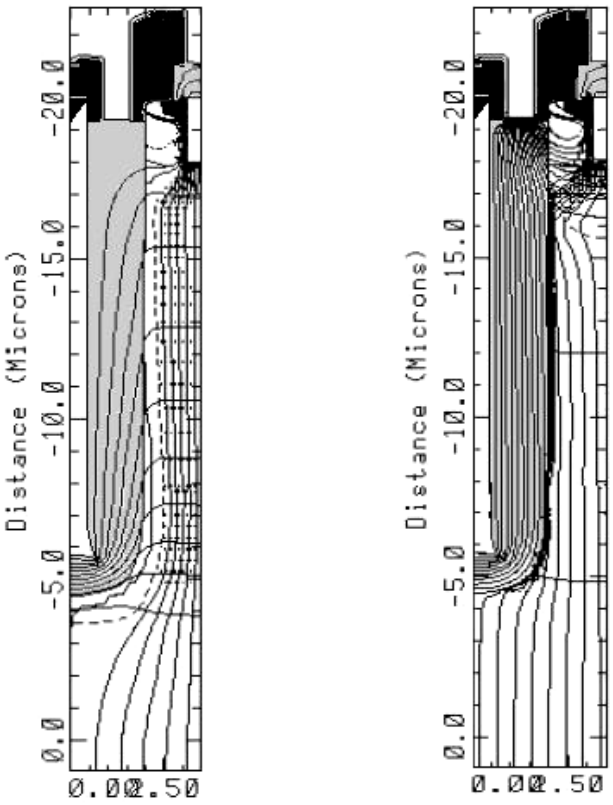


Figure 3-10: TOBUMOS with $N_d = 3\times10^{15}$ cm^{-3} at V_{GS} = 10V and V_{DS} = 30V, under 0V (left) and 60V (right) Control bias.

At on state, the lateral electric field produced by the positive bias from Control acts on the device and leads to the formation of vertical accumulation layer at the interface between MTO and n-drift region. Figure 3-10 shows the current flow lines, potential lines for TOBUMOS structure with $N_d = 3\times10^{15}$ cm^{-3} at V_{GS} = 10V and V_{DS} = 30V, under different Control bias 0V and 60V. It is obvious that, because of the existing of the accumulation layer, conduction area at on state is increased. This results in the reduction of on-resistance.

As in Table 3-2, if the bias is changed from 0V to 60V, V_{br} is increased by 48.8V and $R_{on,sp}$ is reduced by 1.6 mΩ-cm^2. Though the improvement of on-resistance does not match the $R_{on,sp}$ of original optimized OB-device, superior performance of TOBUMOS is clearly observed from the results shown in Figure 3-11, where $R_{on,sp}$ versus V_{br} curves are drawn in logarithm scale to show the relationship of ideal silicon limit [6][32], Superjunction devices [6], original OBUMOS and TOBUMOS structures.

All the results of the TOBUMOS devices in Figure 3-11 are obtained by reducing N_d to different value while maintaining the original OBUMOS structure. For each value of N_d, the Control bias is increased in steps of 10V beginning with a bias of 0V. All the points with increasing Control bias are shown in Figure 3-11. The number of points in each of the lines is different as the lines are terminated once V_{br} starts to drop. The minimum $R_{on,sp}$ obtained under 20V Control bias at $N_d = 6\times10^{15}$ cm^{-3} is much lower than ideal silicon limit and superjunction devices at a much higher V_{br}. It also goes further away from ideal silicon limit line compared to the original OBUMOS.

The reason for V_{br} degradation when Control voltage goes up to a certain value is due to the increase of electrical field on the top region of TOBUMOS.

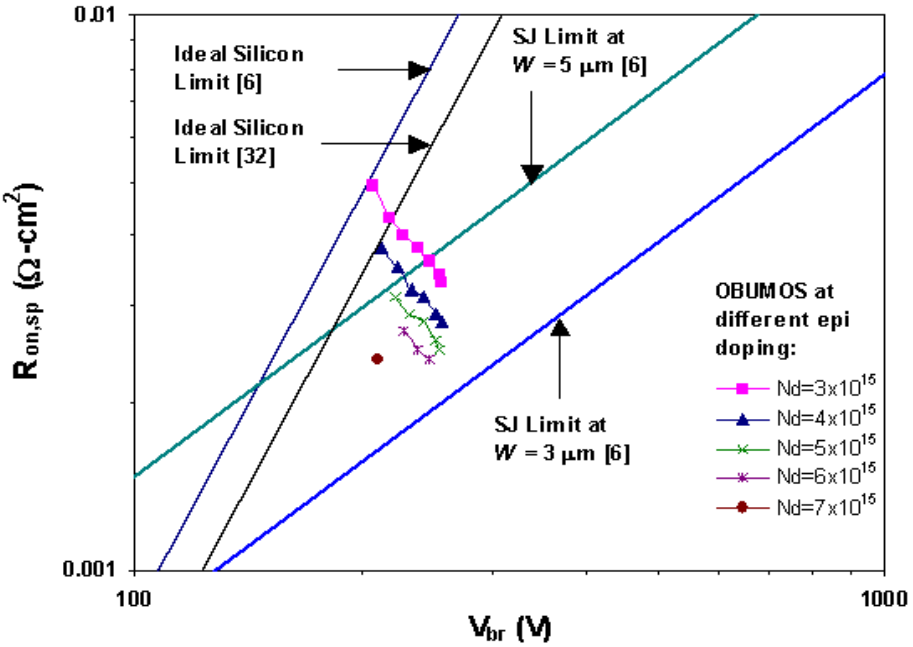


Figure 3-11: $R_{on,sp}$ vs. V_{br} curves of ideal silicon MOSFET limit [6][32] and superjunction structure at W = 3µm and 5µm [6]. The values for OBUMOS structure ($W/2$ = 1.5 µm, t_{ox} = 1.5 µm) with different epi doping are plotted at different Control bias varying from 0 to 60 V for $N_d = 3 \times 10^{15}$ cm^{-3}, 0 to 50V for $N_d = 4 \times 10^{15}$ cm^{-3}, 0 to 40V for $N_d = 5 \times 10^{15}$ cm^{-3}, 0 to 20V for $N_d = 6 \times 10^{15}$ cm^{-3} and 0V for $N_d = 7 \times 10^{15}$ cm^{-3}, respectively.

Simulation proved that, positive Control bias is able to raise the E-field on the upper part of TOBUMOS to a high value. The breakdown happens when E-field on the top region reaches the critical E-field value that can be sustained by Silicon. Simulation indicates that the maximum Control voltage ($V_{con,max}$), which makes the highest V_{br}, mainly depends on N_d if the device structure is fixed. Based on the optimized OBUMOS structure with $W/2$ = 1.5µm, t_{ox} = 1.5µm at $N_d = 6\times10^{15}$ cm^{-3}, $V_{con,max}$ equals to 20V. A higher $V_{con,max}$ of 60V is obtained if N_d is further decreased to 3×10^{15} cm^{-3}. It is also clear that under each N_d from 3×10^{15}cm^{-3} to 6×10^{15}cm^{-3}, both the V_{br} and $R_{on,sp}$ at $V_{con,max}$ are enhanced in comparison to the zero Control bias case. It is clear from Figure 3-11 that when V_{br} of OBUMOS is higher than 200V, the smallest achievable value of $R_{on,sp}$ is 0.0024 Ω-cm^2.

Table 3-3: Comparison of V_{br} with $R_{on,sp}$ = 0.0024 Ω-cm^2 for SJ device at p/n column width of 5μm and 3μm [6], ideal silicon limit [6], original OBUMOS with $N_d = 7 \times 10^{15}$ cm^{-3} and TOBUMOS with $N_d = 6 \times 10^{15}$ cm^{-3} at 20V Control bias.

	SJ at W = 5μm	SJ at W = 3μm	Ideal Silicon Limit	Original OBUMOS	Tunable OBUMOS
V_{br}	162.1V	307V	152.9V	210V	246.8V

Table 3-3 shows the comparison of V_{br} with the same $R_{on,sp}$ of 0.0024 Ω-cm^2. With this given $R_{on,sp}$, the SJ devices at W = 5μm and W = 3μm can support V_{br} of 162.1V and 307V, respectively, while the ideal silicon limit is 152.9V. In contrast, V_{br} of original OBUMOS device is increased by 37.3% beyond ideal silicon limit [6], and for TOBUMOS case, it is increased by 61.4%. Theoretically, the TOBUMOS mentioned is unable to break the SJ limit at the same W of 3μm. However, due to current technology constraint, SJ devices at voltage rating between 200V and 300V are only realizable when W is larger than 5μm. The advantage of this novel TOBUMOS device is that the breakdown voltage and on-resistance can be tuned to the desired value after fabrication, if the n-drift doping on the wafer is not the exact value as expected in the optimum design. However, because there is the relationship between Control bias and breakdown voltage as shown in Figure 3-11 and Table 3-3, the range on positive Control bias is limited.

(c) Characteristics on small signal amplifier application

The advantages of applying positive Control bias to enhance the $R_{on,sp}$ vs. V_{br} performance of OBUMOS structure have been stated in previous subsections. Another important performance enhancement occurs with the ability of improving transconductance (G_m) and unity-gain frequency (F_T). Transconductance is defined as the rate of change of drain current with change in gate voltage. A large

transconductance represents a good current handling capability with certain gate drive voltage and a high frequency response. When the MOSFET operates at the saturation region, the output characteristics are controlled by the gate voltage and channel characteristics. Therefore, G_m is determined by the design of channel and gate. In addition, according to the Equation: $F_T = G_m / (2\pi C_{iss})$, where C_{iss} is the sum of Gate-Source and Gate-Drain miller capacitance, F_T will increase correspondingly with the increase of G_m if there is no distinct change in C_{iss}.

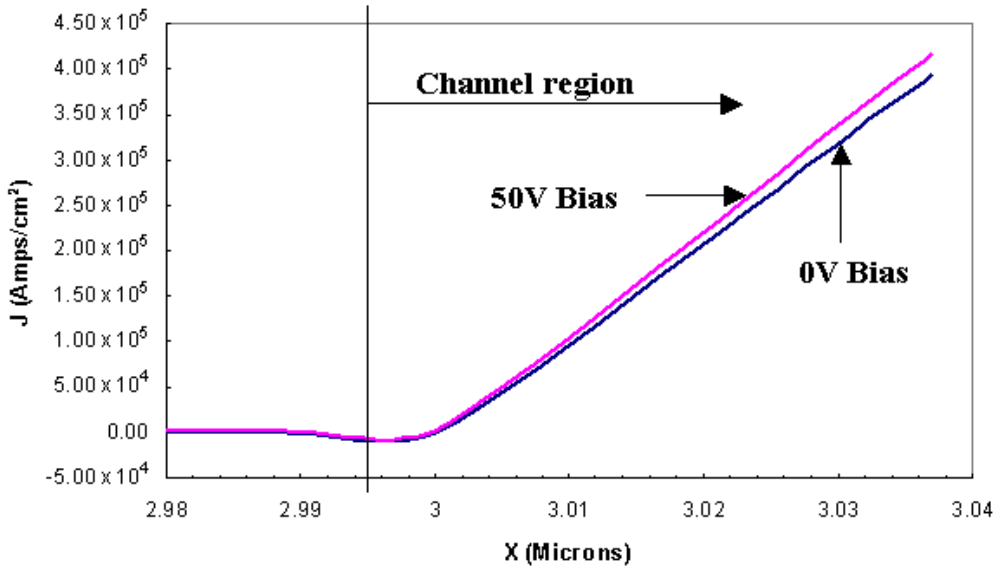


Figure 3-12: Current density comparison in channel region between OBUMOS and TOBUMOS with 50V bias at V_{GS} = 10V and V_{DS} = 30V

When OB-device is under a positive Control bias, the lateral electric field produced by the external bias acts on the channel and pulls the electrons towards the MTO. As a result, the inversion layer depth is increased reducing the channel resistance. Figure 3-12 indicates that, at 50V bias, current density of channel region is a bit higher than that at 0V bias. It is an evidence of reducing channel resistance at higher bias. It is also clear that, compared to the case without Control bias, E-field under 50V bias is much higher in MTO and p body region, while it becomes lower in the channel region, as shown in Figure 3-13 and Figure 3-14.

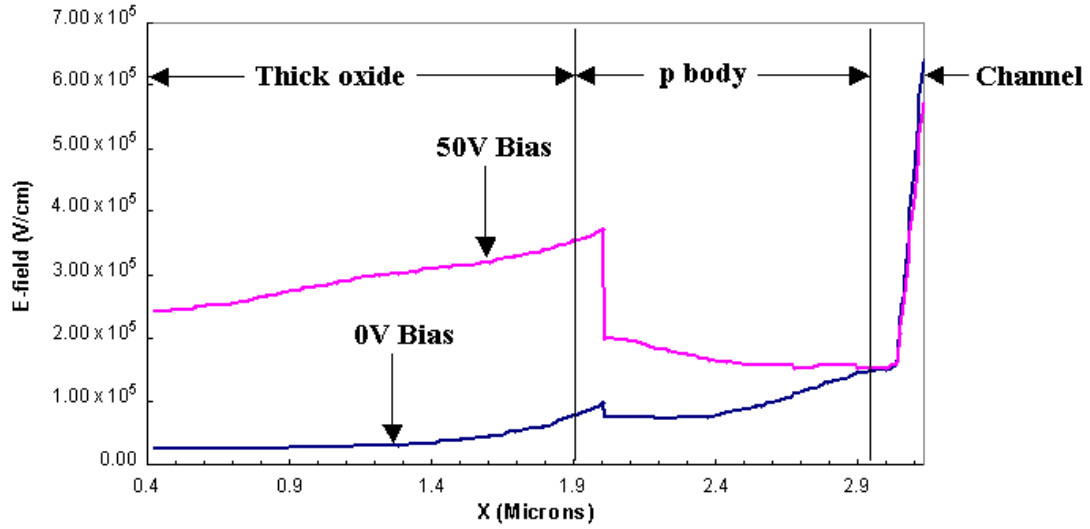


Figure 3-13: E-field distribution for OBUMOS and TOBUMOS with 50V bias, at V_{GS} = 10V and V_{DS} = 30V, cutting at y = -18.5μm (refer to Figure 3-10).

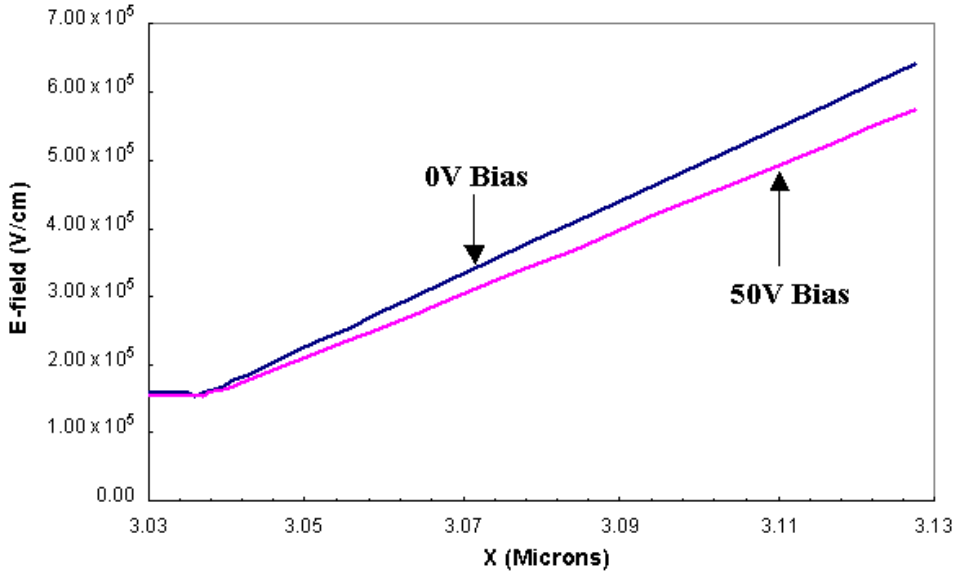


Figure 3-14: Comparison of E-field along horizontal line across channel region between OBUMOS and TOBUMOS with 50V bias.

As shown in Figure 3-15 and Figure 3-16, for device with $N_d = 5\times10^{15}$ cm^{-3}, at given V_{DS} = 30V and frequency of 1MHz, both G_m vs. V_{GS} curve and F_T vs. V_{GS} curve show the larger operational range of the Gate voltage at higher Control bias. Compared to the original OBUMOS, the width of G_m curve is increased by about 40% after applying 50 volts bias on Control electrode.

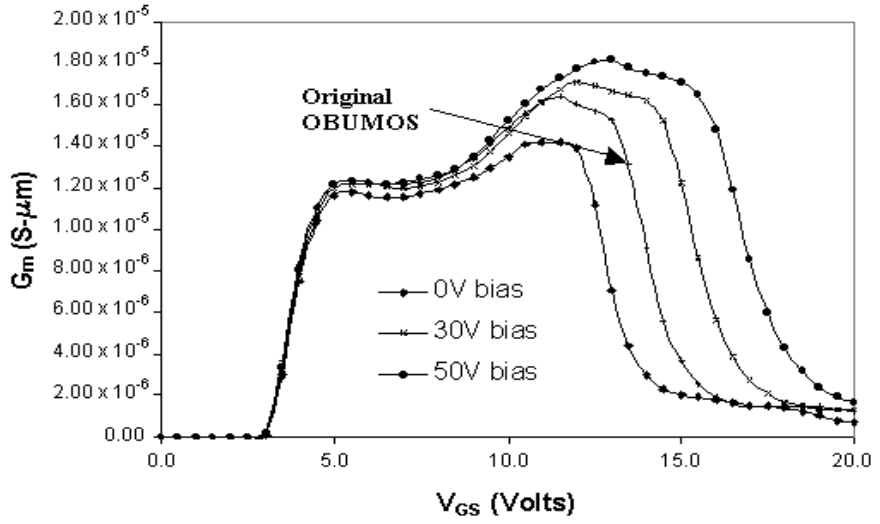


Figure 3-15: Variations of transconductance (G_m) vs. V_{GS} with different Control bias for TOBUMOS at $N_d = 5\times10^{15}cm^{-3}$ compared to original optimized OBUMOS at $N_d = 6\times10^{15}cm^{-3}$.

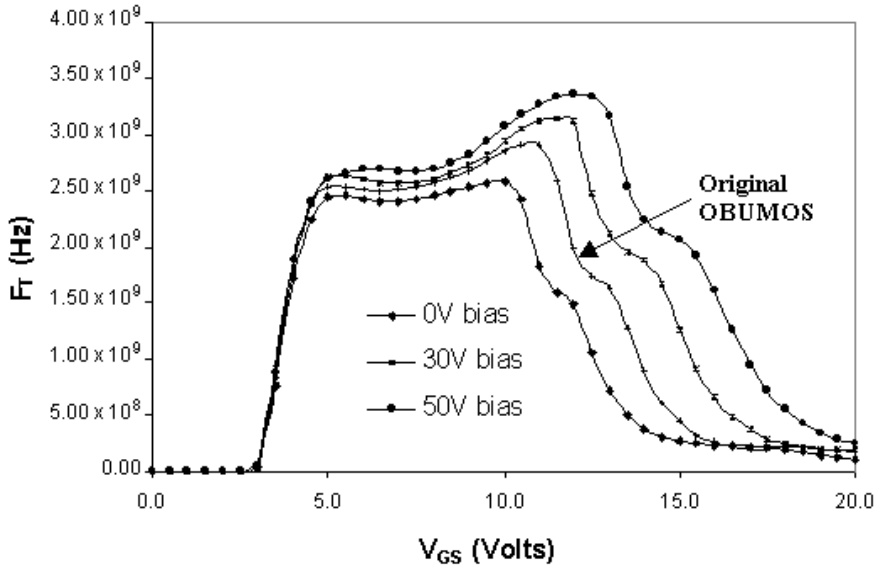


Figure 3-16: Variations of current gain cutoff frequency (F_T) vs. V_{GS} with different Control bias for TOBUMOS at $N_d = 5\times10^{15}\ cm^{-3}$ compared to original optimized OBUMOS at $N_d = 6\times10^{15}cm^{-3}$.

The reason is because the electric field produced by the external bias acts on the channel and increases the channel depth. This results in a reduced channel resistance and enhanced channel mobility. Therefore, higher and wider G_m and F_T curves are achieved. The melioration of small signal performance farther approve of the feasibility of applying TOB concept on the power MOSFETs.

Chapter 4

100V TOBUMOS Fabrication

Due to the requirements for current power MOSFETs applications, 100V Power MOSFETs are especially effective in both conventional and high-density isolated DC/DC power supplies for communications, automotive electrical system and industrial markets. Because in this voltage range, most of SJ devices cannot break the ideal silicon limit to show better performance, TOBUMOS becomes more attractive for medium power applications. This chapter covers the development of 100V TOBUMOS, which includes the numerical simulation, proposed fabrication process flow and mask layout design.

4.1 Simulation on 100V TOBUMOS

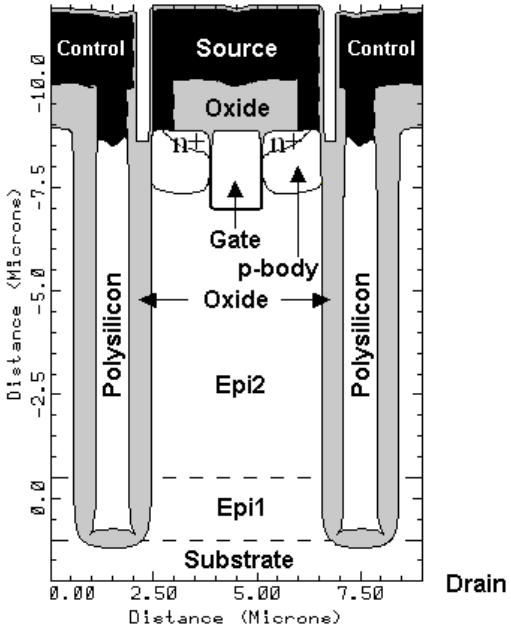


Figure 4-1: TOBUMOS Structure

A 100V TOBUMOS structure (given in Figure 4-1) was generated and simulated using process simulator [39] and device simulator [34]. The simulation was done on the device with dual epi layers. The width (W) of n-drift region is 4μm. The Oxide thickness in OB region is 0.525μm. The first Phosphorous epi layer above 0.003Ω-cm Antimony-doped substrate acts as the impurity diffusion source with resistivity of 0.02Ω-cm.

In consideration of the difference of parameters between simulation and fabrication, detailed simulation of TOBUMOS at certain ranges of epi thickness and resistivity was performed. The outcome of V_{br} and $R_{on,sp}$ of TOBUMOS at 0V Control bias and maximum allowed positive bias is given in Table 4-1.

Table 4-1: Relationship of epi resistivity (ρ_{epi}), epi thickness (T_{epi}), Control Bias, V_{br} and $R_{on,sp}$ @ V_{GS} = 15V and V_{DS} = 0.1V listed for 100V TOBUMOS at W = 4μm and t_{ox} = 0.525μm.

	T_{epi} = 8.0μm			T_{epi} = 8.5μm			T_{epi} = 9.0μm		
ρ_{epi} (Ω-cm)	Control (V)	V_{br} (V)	$R_{on,sp}$ (Ω-cm^2)	Control (V)	V_{br} (V)	$R_{on,sp}$ (Ω-cm^2)	Control (V)	V_{br} (V)	$R_{on,sp}$ (Ω-cm^2)
0.5	0	76.9	4.81×10^{-4}	0	80.3	4.28×10^{-4}	0	74.3	5.58×10^{-4}
	--	--	--	--	--	--	--	--	--
0.55	0	92.9	4.31×10^{-4}	0	100.6	5.57×10^{-4}	0	103.2	5.97×10^{-4}
	--	--	--	--	--	--	--	--	--
0.6	0	99.2	5.55×10^{-4}	0	100.5	5.99×10^{-4}	0	101.3	6.41×10^{-4}
	2	101.0	5.45×10^{-4}	7	106.3	5.69×10^{-4}	8	108.5	6.03×10^{-4}
0.65	0	97.3	5.86×10^{-4}	0	98.8	6.39×10^{-4}	0	99.6	6.86×10^{-4}
	7	103.8	5.57×10^{-4}	13	110.9	5.85×10^{-4}	12	111.0	6.27×10^{-4}
0.7	0	96.3	6.22×10^{-4}	0	97.3	6.77×10^{-4}	0	97.9	7.23×10^{-4}
	9	104.6	5.83×10^{-4}	17	113.2	6.04×10^{-4}	24	120.7	6.17×10^{-4}
0.75	0	94.3	6.60×10^{-4}	0	96.3	7.14×10^{-4}	0	96.7	7.65×10^{-4}
	17	110.8	5.93×10^{-4}	21	116.0	6.21×10^{-4}	23	118.6	6.51×10^{-4}

The bias on Control electrode of TOBUMOS is used to tune the $R_{on,sp}$ vs. V_{br} point to the farthest place from ideal silicon limit line. Because most of the cases listed in Table 4-1 can break the silicon limit line, it is safe to choose the 2nd epi thickness of 8.5μm with resistivity of 0.55Ω-cm and 0.7Ω-cm, respectively. The latter case with

resistivity of 0.7Ω-cm is to test the performance of TOBUMOS, while the former case is selected for optimal OBUMOS in comparison.

According to the Table 4-1, the relationship between V_{br} and resistivity for TOBUMOS on 8.5μm epi layer is shown in Figure 4-2. It is clear that, with the optimal epi resistivity of 0.55Ω-cm, there is no advantage of tunable voltage applied on Control Electrode. With nonoptimal epi resistivity of 0.7Ω-cm, positive Control bias is able to reach up to 17V.

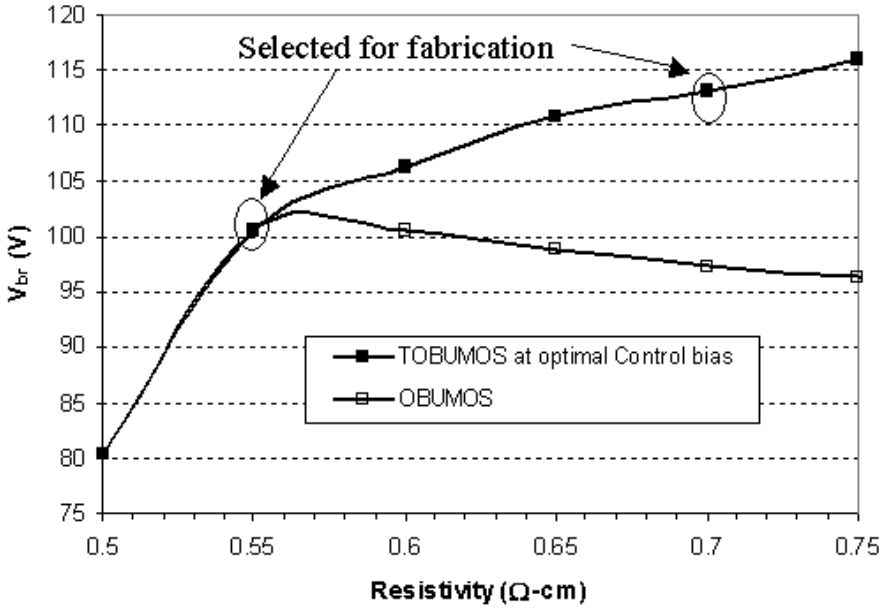


Figure 4-2: V_{br} vs. resistivity plots for OBUMOS and TOBUMOS at 2nd epi depth of 8.5μm

The minimum $R_{on,sp}$ obtained for the device with such epi resistivity is 6.04×10^{-4} Ω-cm^2. Most importantly, $R_{on,sp}$ vs. V_{br} relationship at this point is better than that on the optimal OBUMOS with epi resistivity of 0.55Ω-cm. Figure 4-3 and Figure 4-4 show the on-state performance of TOBUMOS structure. The threshold voltage of this device is about 1.2V.

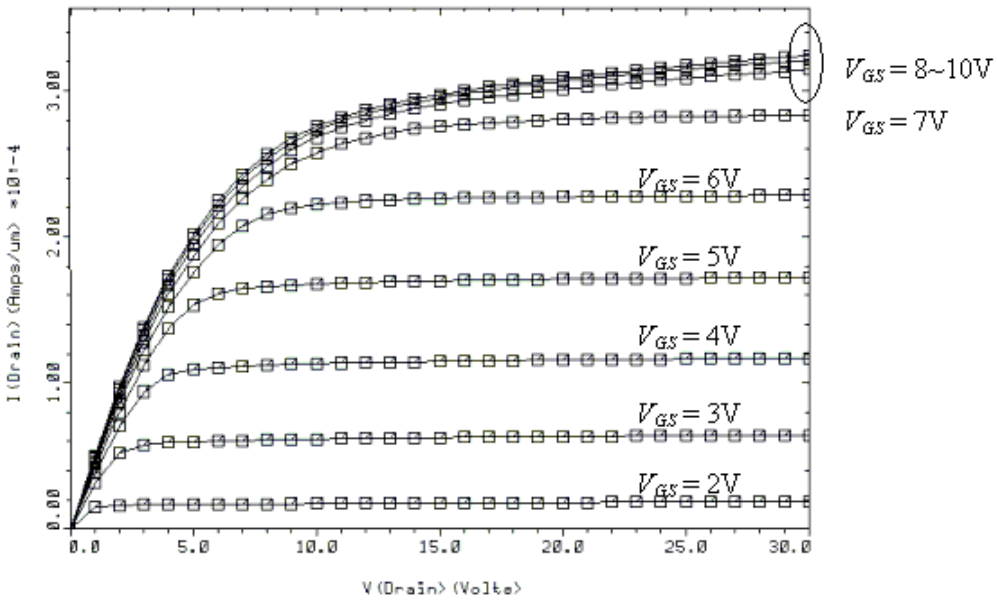


Figure 4-3: On state IV characteristics of half TOBUMOS structure

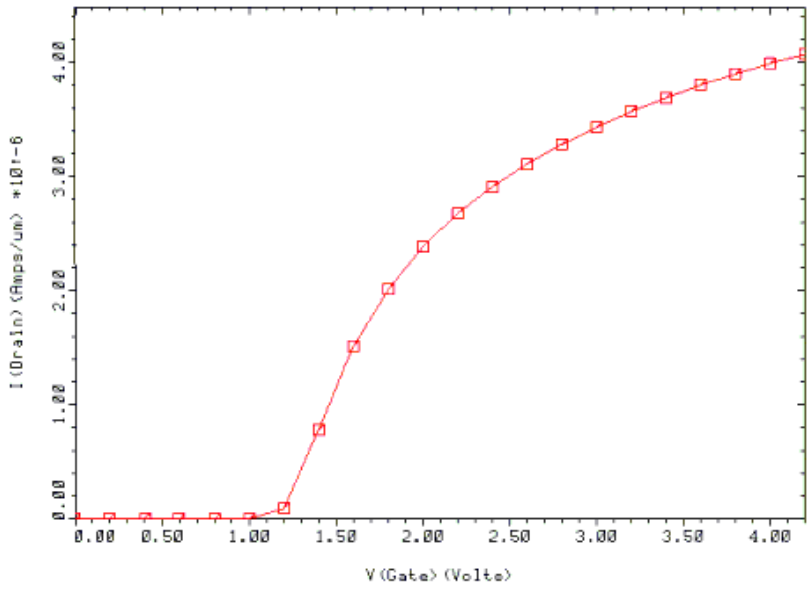


Figure 4-4: I_{DS} ~V_{GS} simulation of TOBUMOS at V_{DS} = 0.1V

Figure 4-5 shows the $R_{on,sp}$ vs. V_{br} relationship of 100V TOBUMOS according to Table 4-1, compared with ideal silicon MOSFET limit [6][32] and SJ structure at W = 3μm, 4μm and 5μm [6]. It is obvious that, 100V TOBUMOS breaks not only the ideal Silicon limit, but also its counterpart of SJ limit at W = 3μm. It is concluded that TOBUMOS has superior $R_{on,sp}$ compared to OBUMOS with the same V_{br}.

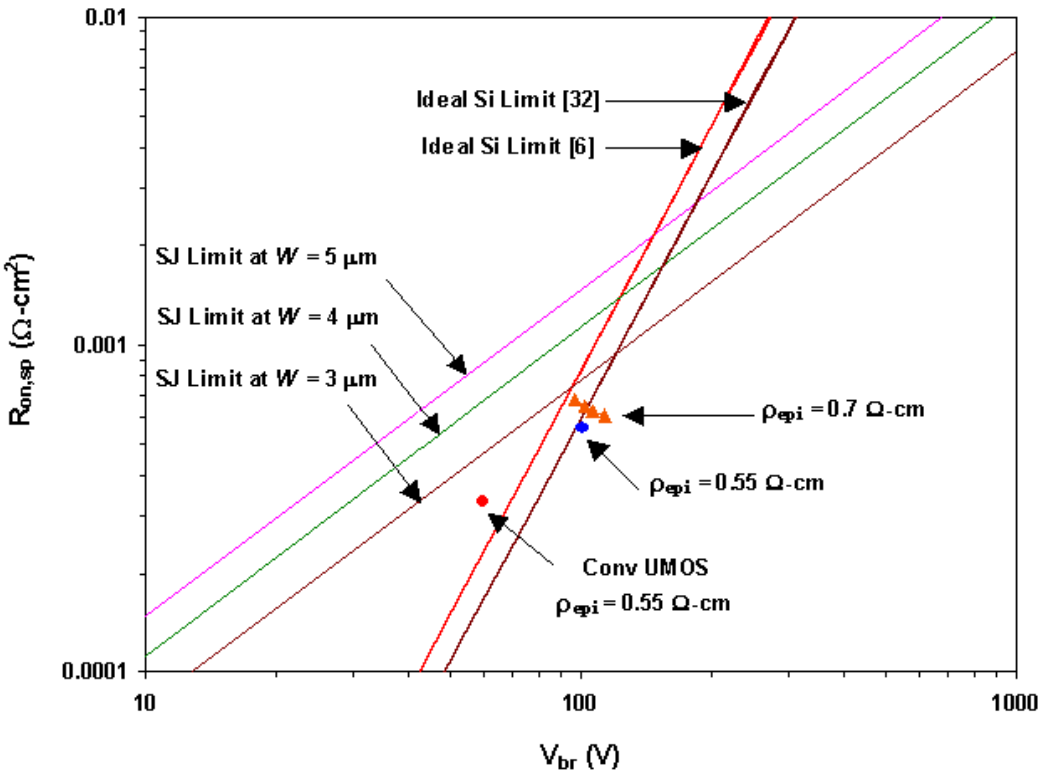


Figure 4-5: $R_{on,sp}$ vs. V_{br} curves of ideal silicon limit [6][32] and superjunction structures at W = 3µm, 4µm and 5µm [6]. The values for 100V TOBUMOS structures are plotted, at different Control bias of 0V for ρ_{epi} = 0.55 Ω-cm, varying at 0, 5, 10 and 17V for ρ_{epi} = 0.7 Ω-cm, respectively.

4.2 Results and analysis on the previous OBUMOS fabrication

4.2.1 Fabrication results of OBUMOS

OBUMOS has been fabricated on the wafers with 20µm, 0.7Ω-cm n type epi by the previous student. However, there are some problems in the measurement results of fabricated OBUMOS as below (refer to Chapter 7 of Reference [24]):

(1) High threshold voltage (V_T).

This might be attributed to the over-etch of Gate PolySi during Gate PolySi etch-back step resulting in no overlap between n+ source and Gate PolySi.

Even when there is a slight overlap between Source and trench Gate, high V_T may still be obtained as a result of PolySi re-oxidation step after PolySi etch back that creates a thicker Gate oxide beside the top of p-body region due to bird's beak effect (refer to Gate region of Figure 4-1).

(2) Gate-Source shorted at on state after the 1st split run

It may be due to two reasons: a. Over etch of oxide during active area etch and the subsequent poly deposition and contact etch as explained in Reference [24]; b. Short distance (refer to Figure 4-1) between Gate poly and Source contact according to the design, which results in the Gate-Source short when Gate poly is not etched below the surface. This problem has been removed when an additional gate mask is used and the poly re-oxidation step is removed for the 2nd split run.

(3) The drop of Drain current when Drain voltage goes up beyond a certain voltage

The measured IV curve shown this problem is presented in Chapter 7 of Reference [24]. It can be linked to the effect of a redistribution of electric field caused by rough surface of p-body edge, which results in the increase in potential of channel region. This rough surface might be created by the contact dry etch during actual device fabrication. It is possible that during contact etching, the sidewall oxide was slightly etched as the time-based etching was done. Thus, when the depletion edge spread to the rough surface at high drain bias, electric field in channel region was reduced and this leads to the drop in drain current due to an increase in channel resistance. This effect would

manifest itself only when the depletion edge spread to the rough surface and this explains why the drop in drain curve appeared only at high drain bias.

(4) Gate open

After Gate-Source short problem was removed during OBUMOS 2nd split run, it was found that for most of fabricated OBUMOS, on-state performance is unmeasured, though they have normal off-state performance. According to the Gate trench formation part of process flow (refer to section 4.3.4 or Chapter 7 of Reference [24]. Gate trench formation of 100V TOBUMOS proposed later is based on the same process principle as previous fabricated OBUMOS as in Reference [24].), it is supposed that the thick Oxide inside Gate trench region at OB termination couldn't be removed completely. The detailed description will be introduced later (shown in Figure 4-11) in this chapter. Thus, the connection between gate contact and Gate Poly within active region is cut off, which makes the device failure at on state due to Gate open.

4.2.2 Concerns for 100V TOBUMOS fabrication

To avoid the problems existed in the previous fabricated OBUMOS, some points must be taken into account for 100V TOBUMOS fabrication:

(1) Some variations should be made in consideration of mask alignment and process offset issues.

(2) The trench Gate and Gate oxide formation should be performed with extreme care, because the quality of the Gate oxide surface and the shape of Gate trench at termination area will affect the on state performance significantly.

(3) The distance between Gate trench mask and Source contact mask should be more than 0.8μm, to avoid the short of Gate and Source.

(4) There should be enough space between Source and Control contact.

With these concerns in mind, process for 100V TOBUMOS was designed.

4.3 100V TOBUMOS Fabrication

4.3.1 Device structure and mask layout design

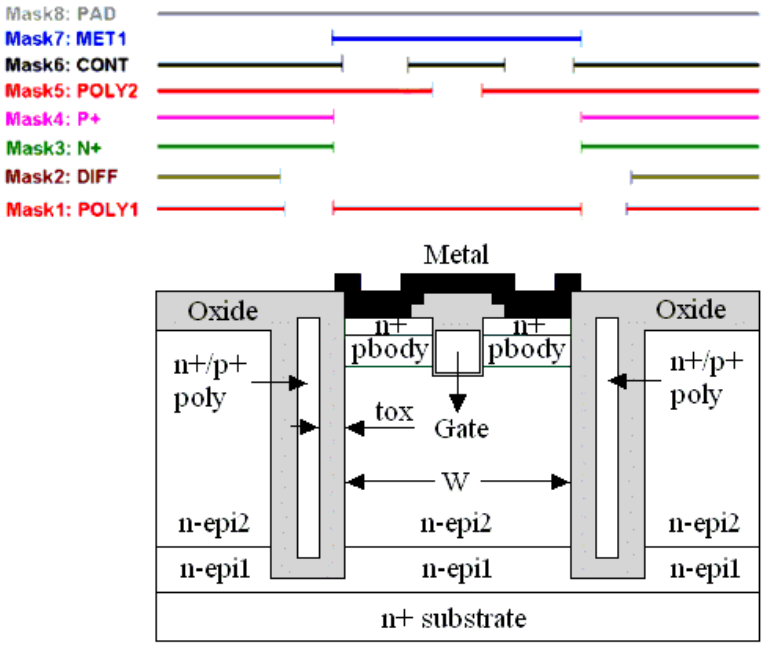


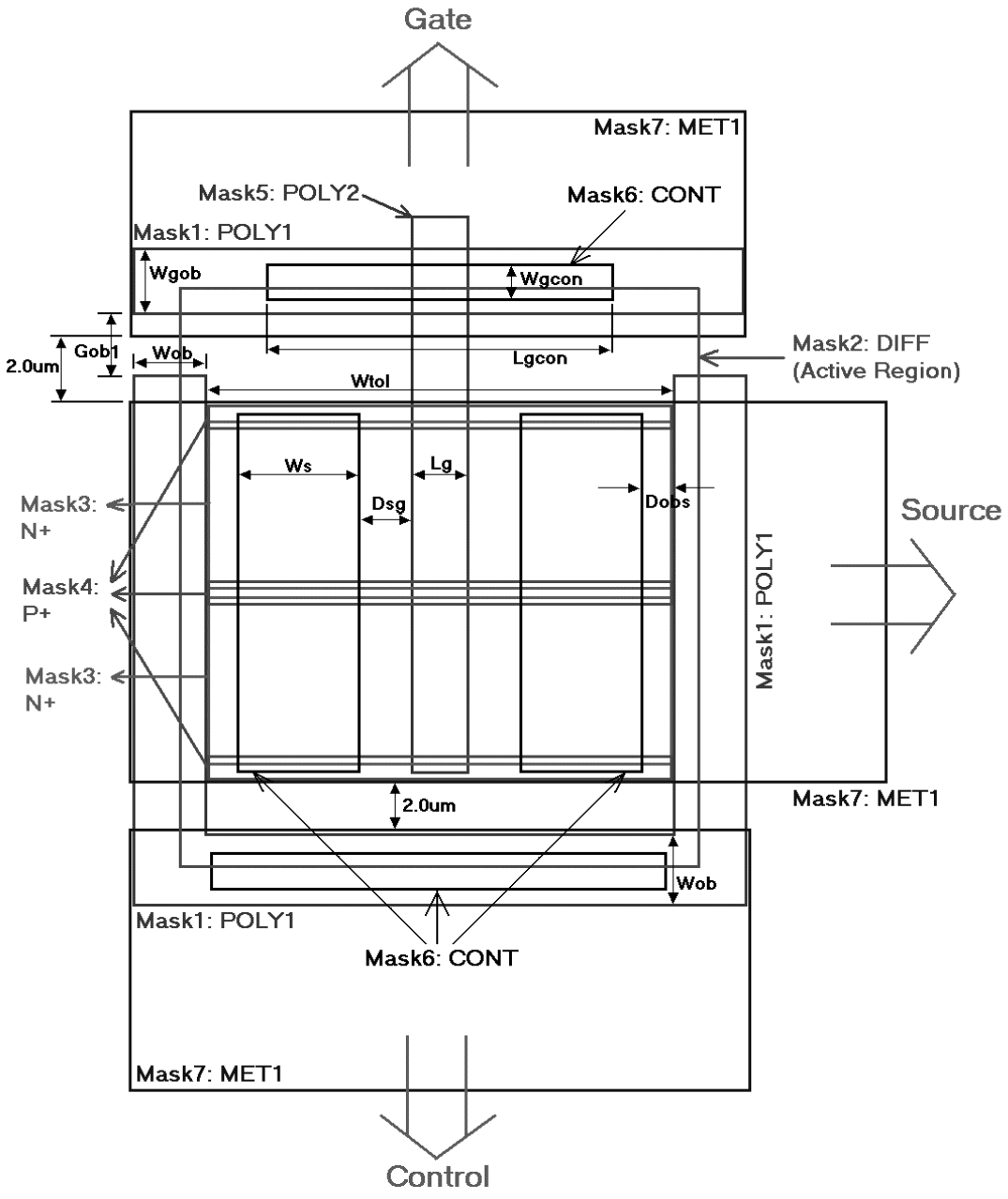
Figure 4-6: Cross-section view of 100V TOBUMOS together with masks

The proposed device cross section view and fabrication masks are shown in Figure 4-6 and Figure 4-7, respectively. Compared to conventional UMOS fabrication steps, only one additional mask (POLY1 Mask) is required. Figure 4-7 shows the top views of mask layout with different POLY1 masks. They were designed to check the effect of top termination on OB functionality.

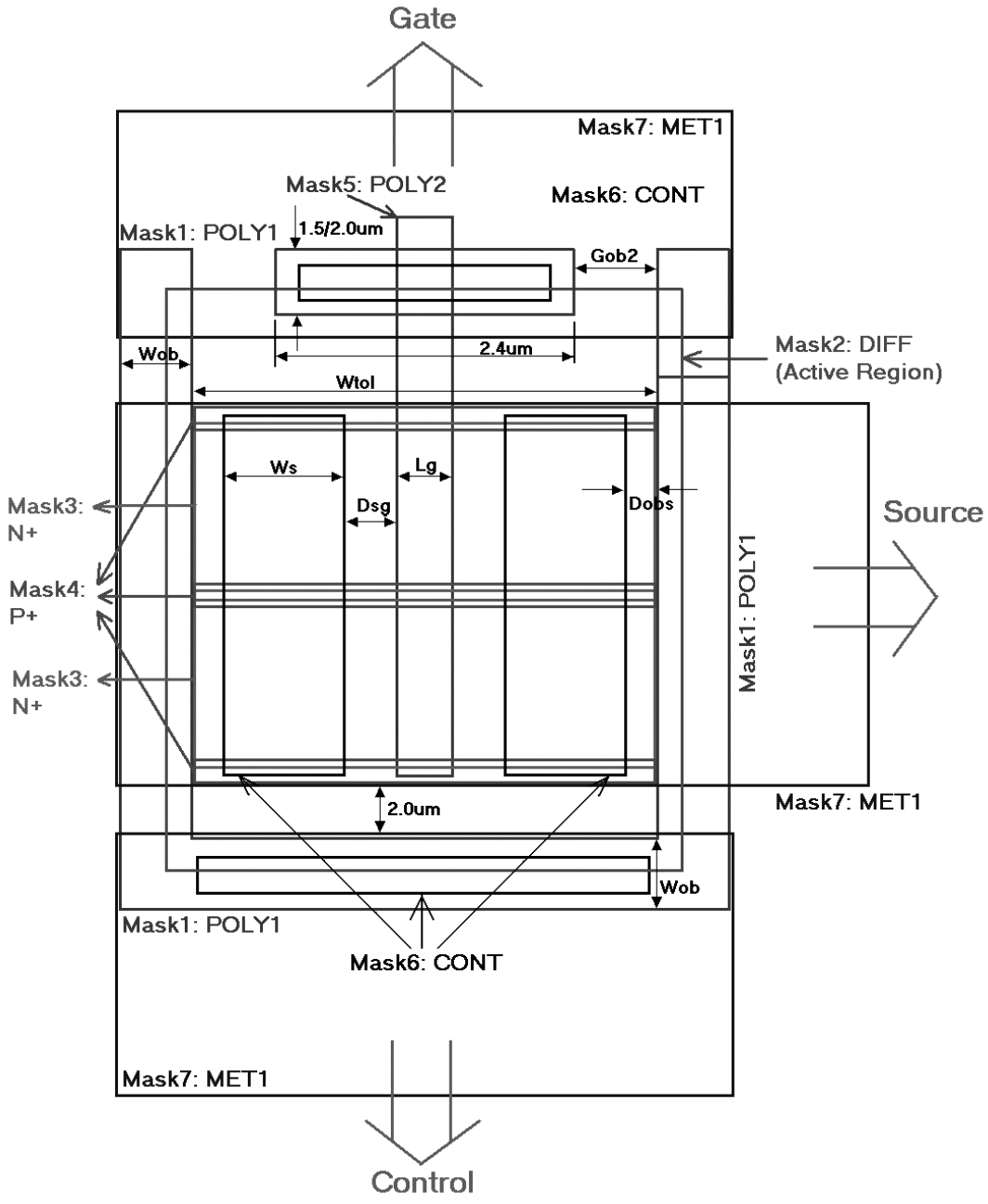
It is to be noted that Control contact is only located at the bottom of the OB trench due to the space limitation in lateral dimension. This won't affect the device performance

because only voltage bias is applied on Control contact. There is no current conduction in the highly doped Polysilicon region of OB structure. There are totally 9 masks in the process and no additional mask is needed compared to the fabrication of OBUMOS. Apart from the 8 masks shown in Figure 4-6 and Figure 4-7, Gate Pad Shield Mask is added at the step of sacrificial dry oxide etching, to protect the gate trench outside active region.

There are totally four electrodes for TOBUMOS. Except for Drain electrode, which is made at the bottom of the wafer, all the other three electrodes are all on the top of the wafer. The schematic of mask layout and parameter variation are shown as in Figure 4-7 and Table 4-2, respectively. Separated contact windows are made on Source contact and Control contact. Hence, TOBUMOS fabrication will not add any difficulties in comparison to the previous fabrication work, but leads to better device performance.



(a) Termination type 1



(b) Termination type 2

Figure 4-7: Top view of 100V TOBUMOS with two types of OB trenches at top termination

Table 4-2: Parameter variations of TOBUMOS mask layout

Parameter	Wgcon	Lgcon	Wob	Wgob	Gob1	Gob2
Range (μm)	0.8/0.9/1.0	2.8 ~ 7.0	1.0/1.5/2.0	1.5/2.0	1.25/1.75/2.0	0.8 ~ 1.8
Parameter	Wtol	Lg	Ws	Dsg	Dobs	
Range (μm)	3.0 ~ 6.0	0.8/1.0	0.6/0.8/1.0	0.3 ~ 1.05	0.1 ~ 0.7	

The explanations for the parameters shown in Figure 4-7 are as below:

Wgcon: Gate contact width

Lgcon: Gate contact length

Wob: OB trench width

Wgob: Width of OB trench on the Gate side

Gob1: Gap of OB trench for termination type 1

Gob2: Gap of OB trench for termination type 2

Wtol: Total width between neighboring OB trenches

Lg: Gate length

Ws: Width of Source contact

Dsg: Distance between Source contact and Gate trench

Dobs: Distance between OB trench and Source contact

4.3.2 Mask floorplan for 100V TOBUMOS fabrication

In real fabrication, mask misalignment (0.2~0.3μm in IME) and some parameter variations must be considered into mask layout design, as shown in Figure 4-8. The desired devices with exact same parameters as in simulation locate in column 4 and column b only. Variations such as n-drift region width (Wtol) from 3.0μm to 6.0μm are made within each region (column 1~7, column 8~e or column f~l), at 0.5μm interval. Conventional UMOS and Diode are also fabricated on the same wafer for comparisons.

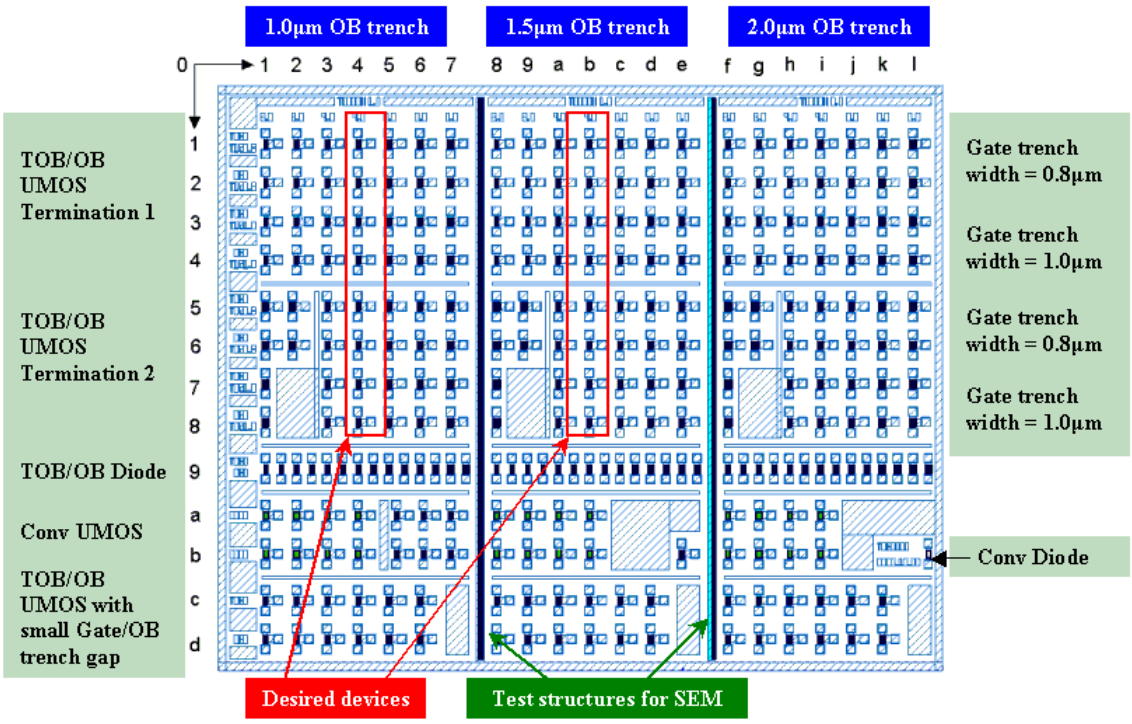


Figure 4-8: Mask floorplan design for 100V TOBUMOS fabrication

4.3.3 Wafer allocation index

There are 29 pieces of wafers in three groups involved in this fabrication.

Apart from 9 pieces of test wafers, the 20 pieces of functional wafers are divided into two groups with different epi resistivities. The group with heavily doped epi is to test the performance of 100V OBUMOS while the other group with lightly doped epi is to check the effect of tunable control voltage applied on OB region. The specifications are as below:

#01- #10: Dual epi wafers, Antimony-doped substrate
(Epi layer1: 0.02 Ω-cm Phos, 1.5 μm; Epi layer2: 0.55 Ω-cm Phos, 8.5 μm)
#11- #20: Dual epi wafers, Antimony-doped substrate
(Epi layer1: 0.02 Ω-cm Phos, 1.5 μm; Epi layer2: 0.70 Ω-cm Phos, 8.5 μm)
#21- #29: Test wafers

Considering the parameter offsets in fabrication, some wafers are split for Oxide thickness in OB region and pbody implantation dosage variations, as in Table 4-3.

Table 4-3: Oxide thickness and p-body implant splits for TOBUMOS fabrication

Wafer No.	Oxide Thickness -- OB	Boron Implant Dose -- pbody
01 & 11	0.4 μm	2×10^{13} cm^{-2}
02 & 12	0.4 μm	2×10^{13} cm^{-2}
03 & 13	0.4 μm	4×10^{13} cm^{-2}
04 & 14	0.5 μm	2×10^{13} cm^{-2}
05 & 15	0.5 μm	2×10^{13} cm^{-2}
06 & 16	0.5 μm	2×10^{13} cm^{-2}
07 & 17	0.5 μm	4×10^{13} cm^{-2}
08 & 18	0.6 μm	2×10^{13} cm^{-2}
09 & 19	0.6 μm	2×10^{13} cm^{-2}
10 & 20	0.6 μm	4×10^{13} cm^{-2}

4.3.4 Process flow

The simplified process flow of 100V TOBUMOS is shown below:

(1) Wafer Pre-treatment
(2) Oxide growth
(3) Silicon OB Trench etch and Resist strip
(4) OB Dry Oxide and Wet Oxide growth
(5) LPCVD PolySi deposition
(6) PolySi doping
(7) Global PolySi removal and Backside PolySi etch
(8) Active Region Oxide etch and Resist strip
(9) Dry oxidation
(10) p-body implant and Drive-in
(11) n+ implant and Resist strip
(12) p+ implant and Resist strip
(13) Oxide Deposition
(14) Oxide etch at Gate region
(15) Gate Silicon Trench etch and Resist strip
(16) Sacrificial dry oxidation
(17) Sacrificial Oxide etch and Resist strip
(18) Gate oxidation
(19) LPCVD PolySi deposition
(20) PolySi dope
(21) Global PolySi removal

(22) Poly re-oxidation

(23) TEOS/BPSG deposition

(24) Contact Oxide dry etch and Resist strip

(25) BPSG reflow

(26) PVD AL

(27) AL dry etch and Resist strip

(28) Passivation Oxide deposition

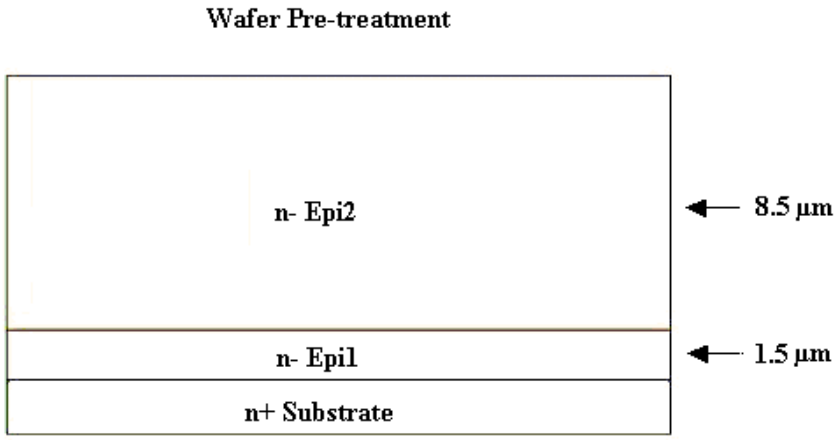
(29) Pad opening and Resist strip

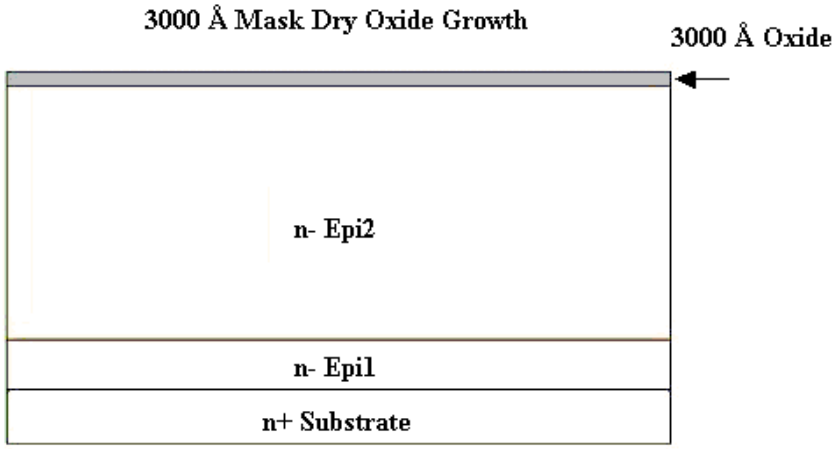
(30) Backside strip

(31) Alloy

4.3.5 Process description

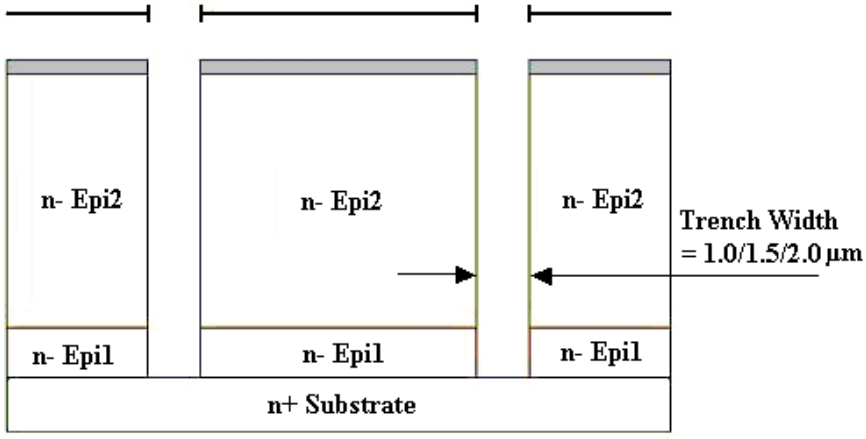
Following the process descriptions based on current technology [53-54]:



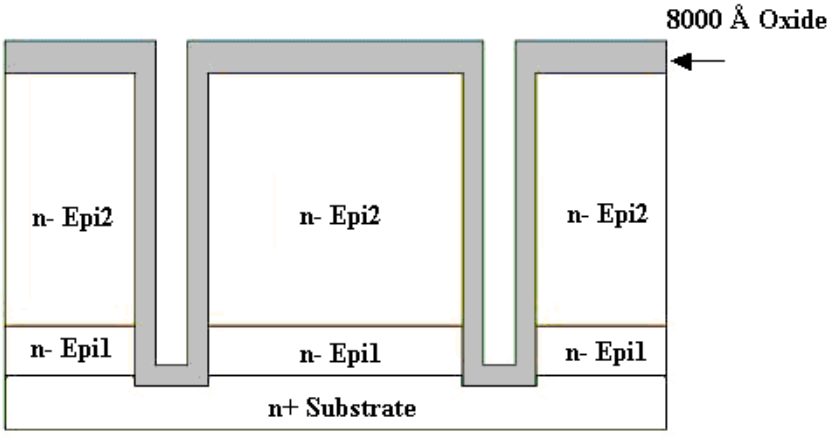


Mask 1: OB trench Mask

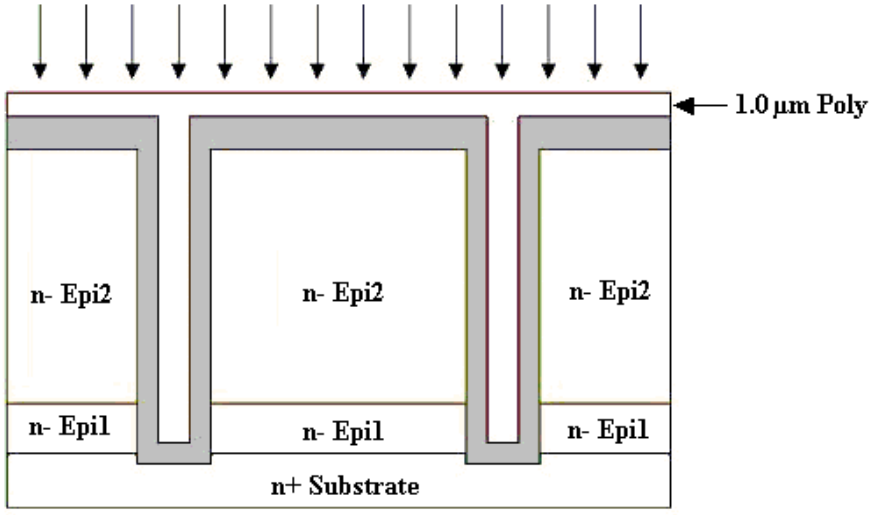
Mask Oxide Etching, Si Trench Etching (Trench depth = 10 µm), Resist Strip



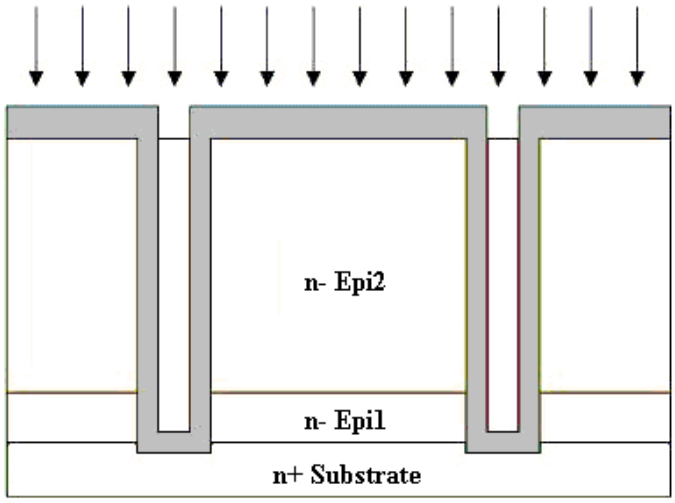
100 Å Dry Oxide growth & 0.5 µm Wet Oxide growth



LPCVD PolySi deposition_1.0 µm; POCL3 doping (900C, 60min)

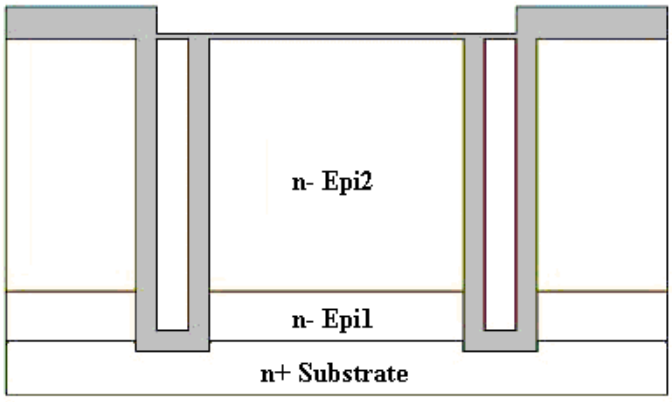


Global PolySi removal (Stop on Oxide and then over etch 0.6μm)
Backside PolySi etch; POCL3 doping (1050C, 60min)

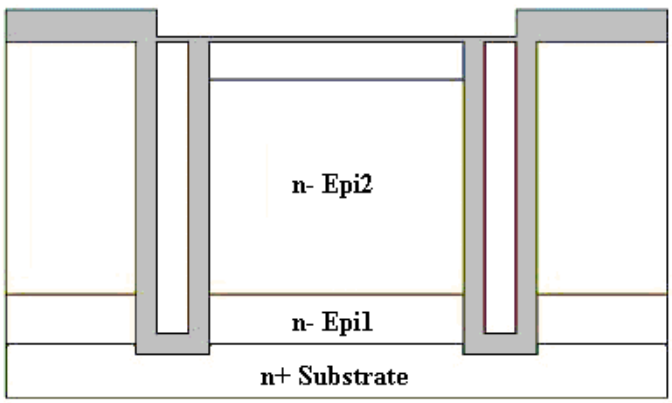


Mask 2: Active Region

0.8μm Oxide etch and Resist strip; Dry oxidation_200 Å



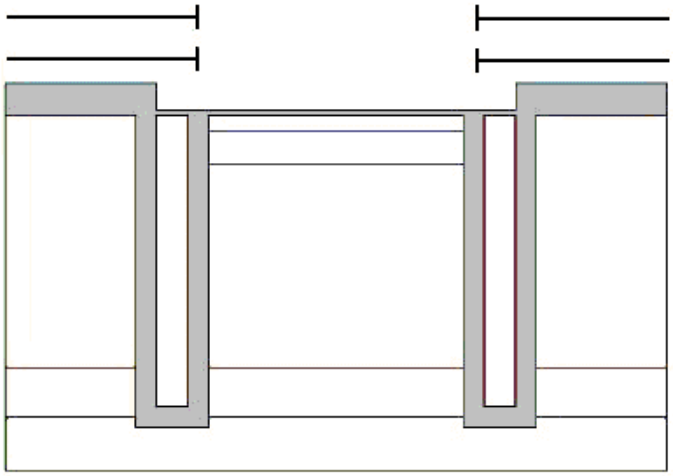
Boron implant (2×10^{13} cm^{-2}, 90KeV, tilt = 7), Resist Strip
Drive-in (Time = 100min, Temp = 1125), Dry Oxidation_200 Å



Mask3: n+ Mask: As implant (5×10^{15} cm^{-2}, 120KeV, Tilt = 7); Resist Strip

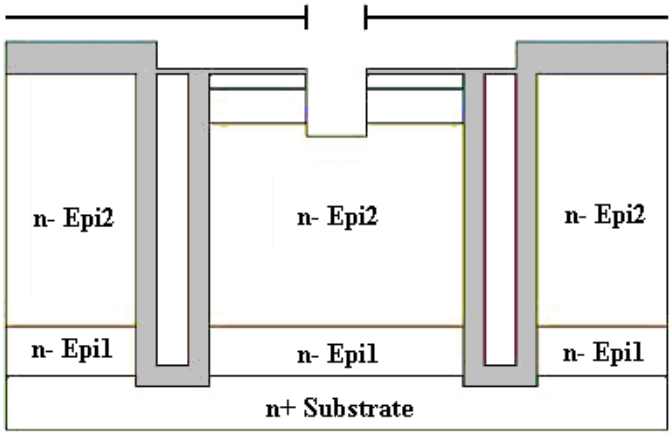
Mask4: p+ Mask: BF2 implant (3×10^{15} cm^{-2}, 80KeV, Tilt = 7); Resist Strip; SRO (200 A) + LPCVD TEOS (2500 A)

(In one 2D cross section, only one of n+ or p+ Mask can be seen)



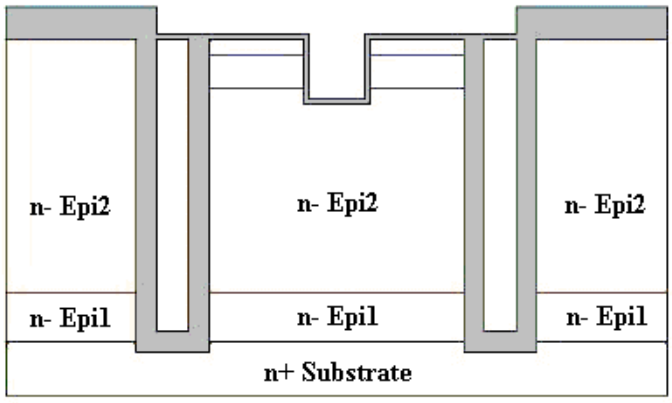
Mask 5: Gate Trench

Oxide etch; Si Trench etch_2μm; Resist Strip;
Sacrificial dry oxidation_200 Å



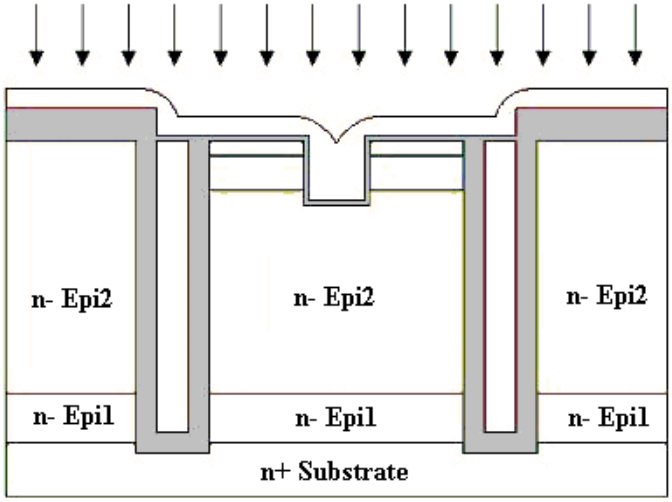
Mask 5-1: Gate Pad Shield

Sacrificial Oxide etch; Resist Strip;
Gate oxidation_430 A (Time = 40min, Temp = 1000)



Conformal PolySi deposition_0.2μm; PolySi deposition_0.9μm

POCL3 PolySi dope (Time = 30min, Temp = 930)

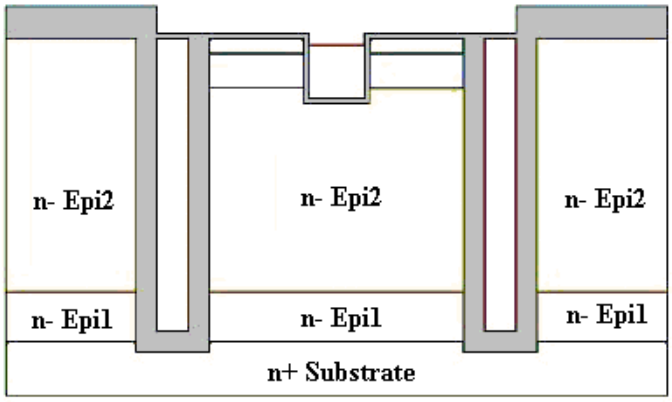


Global PolySi removal, stop on Oxide and then over etch 0.1μm

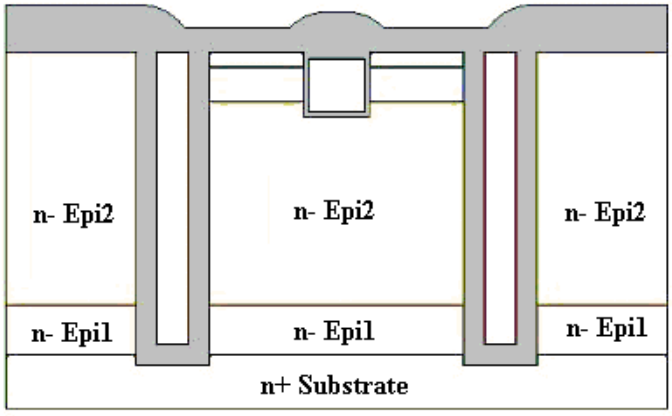
1000 Å Poly re-oxidation: Time = 10, Temp = 900 DRYO2

Time = 30, Temp = 900 WET

Time = 10, Temp = 900 DRYO2



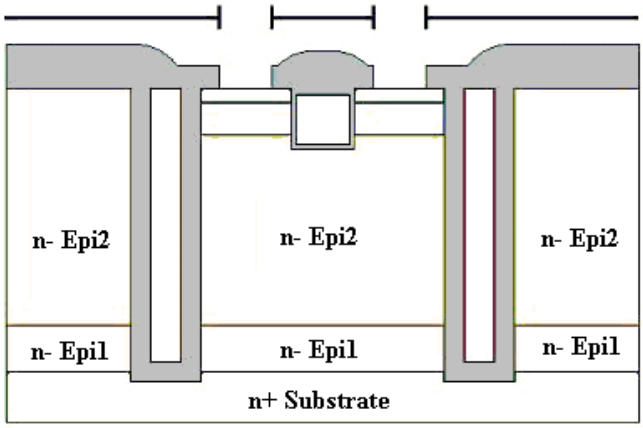
TEOS/BPSG deposition_9000 Å



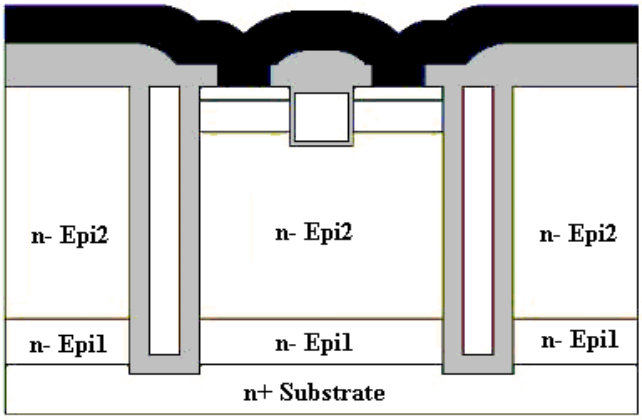
Mask6: Contact Mask

Oxide dry etch and Resist strip

BPSG Reflow (Time = 30, Temp = 900)



PVD Barrier Metal Deposition; RTP Silicidation; PVD AL_1.7μm



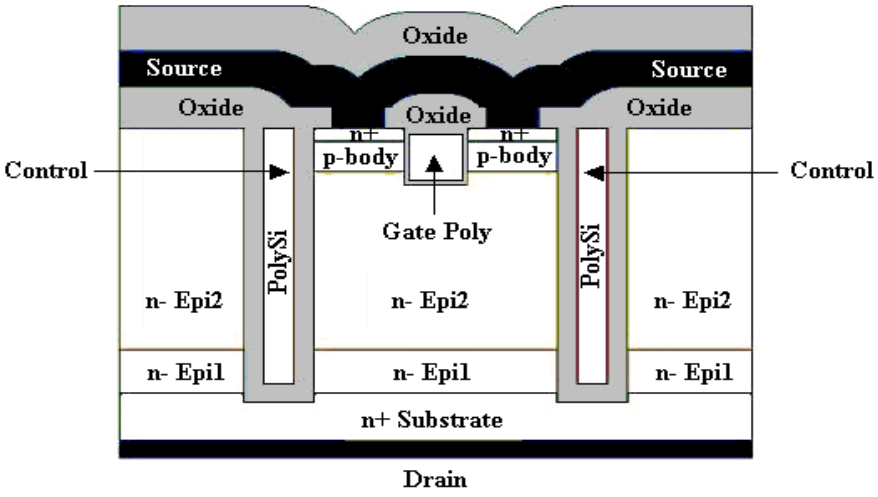
Mask7: AL Etch Mask

AL dry etch and Resist strip; Passivation Oxide deposition

(No etch regions are seen in this 2D cross section. However, they are clearly shown in Figure 4-7)

Mask8: Passivation Mask

Pad opening and Resist strip; Backside strip; Alloy



4.4 Key points on TOBUMOS fabrication

4.4.1 Oxide profile in OB region

The breakdown voltage is affected by the oxide thickness and profile at the trench bottoms. Because the breakdown always happens near the corner of the bottom trench oxide, a thicker oxide at the bottom than that of sidewall will increase the breakdown voltage. On the other hand, if the trench corner is rounded by isotropic etching before oxidation, the oxide grows uniformly around the trench during the oxidation. Thus device off state performance can be improved as well.

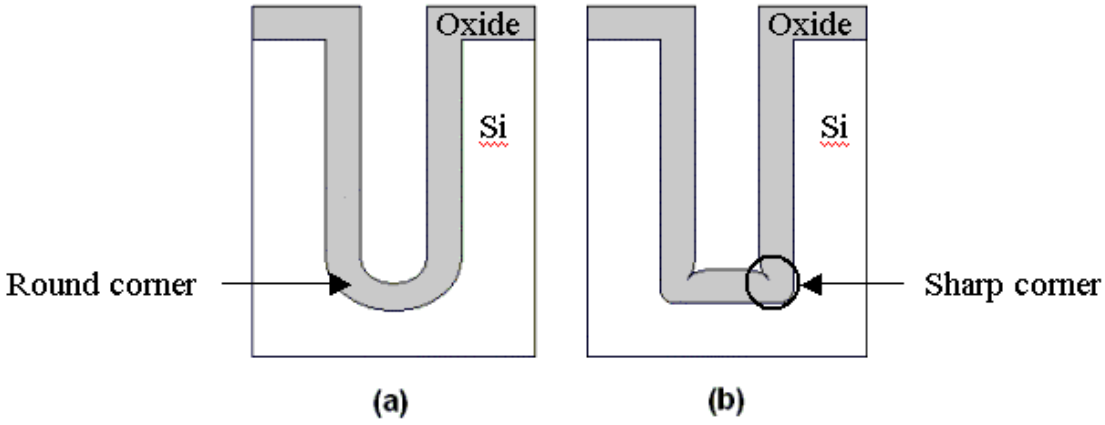


Figure 4-9: Comparison of two different trench profiles of after oxidation

As shown in Figure 4-9, Figure 4-9(a) is the desired oxide profile after fabrication because the trench corner is rounded by short-time isotropic etching. Compared to Figure 4-9(a), Figure 4-9(b) doesn't have such treatment before oxidation. The oxide in Figure 4-9(b) becomes thin at the trench corner after the oxidation. In this case, electric field generated by the reverse bias is likely crowded at the corner region, which leads to the premature breakdown. Earlier simulations such as the OB structure on Figure 3-1 (Page 34) has proved the phenomenon shown in Figure 4-9(b).

4.4.2 Optimum doping profile in drift region

As given in Figure 4-5, owing to OB structure and tunable control voltage, 100V TOBUMOS simulation has successfully shown the superior performance over conventional MOSFETs and SJ Devices. This simulation was done on 0.02 Ω-cm^2 Phosphorous-doped substrate. Phosphorous in substrate is likely to diffuse into epi layer under thermal cycles, which is known as out-diffusion. Therefore after the thermal fabrication process, doping profile in epi layer of the device becomes non-uniform. The doping concentration is gradually reduced from the bottom to the top.

It has been proposed that a lower on-resistance can be obtained by using a non-uniform epitaxial doping profile to obtain the same breakdown voltage [32]. As a result of out-diffusion from the substrate during epitaxial growth and processing with uniformly doped epitaxial layers, the doping profile of power MOSFETs approaches the ideal profile without the need to take a special effort to tailor the epitaxial layer doping. Some experiments trying different impurities and doping concentrations have been done to find the optimum epi doping profile for 100V TOBUMOS. It is established through simulations that, by using 0.02Ω-cm Phosphorous-doped substrate, the best performance of 100V TOBUMOS can be obtained. However, the wafer with phosphorous-doped substrate is commercially unavailable. In this case, wafers with multi-epi layer are selected. Same performance can be achieved by using this wafer instead of the previously designed one. As shown in Figure 4-6, the new wafer contains two epi layers. The 1st epi layer right above substrate is doped with phosphorous, which has the resistivity of ρ_{epi1} = 0.02Ω-cm. The resistivity for the 2nd epi layer above the 1st epi layer is in the range between 0.55Ω-cm and 0.75Ω-cm. The substrate material and doping are allowed to be in a big range. Here we choose

Antimony-doped substrate with ρ_{sub} = 0.003Ω-cm. Figure 4-10 shows the post-fabrication doping profile of 100V TOBUMOS with epi1 thickness = 1.5µm, epi2 thickness = 8.5µm, t_{ox} = 0.525µm, half drift region width = 2µm and half OB structure width = 1µm. The simulation result for this structure is V_{br} = 100.6 V @ (2.43, -2.4), $R_{on,sp}$ = 5.57×10^{-4} Ω-cm^2.

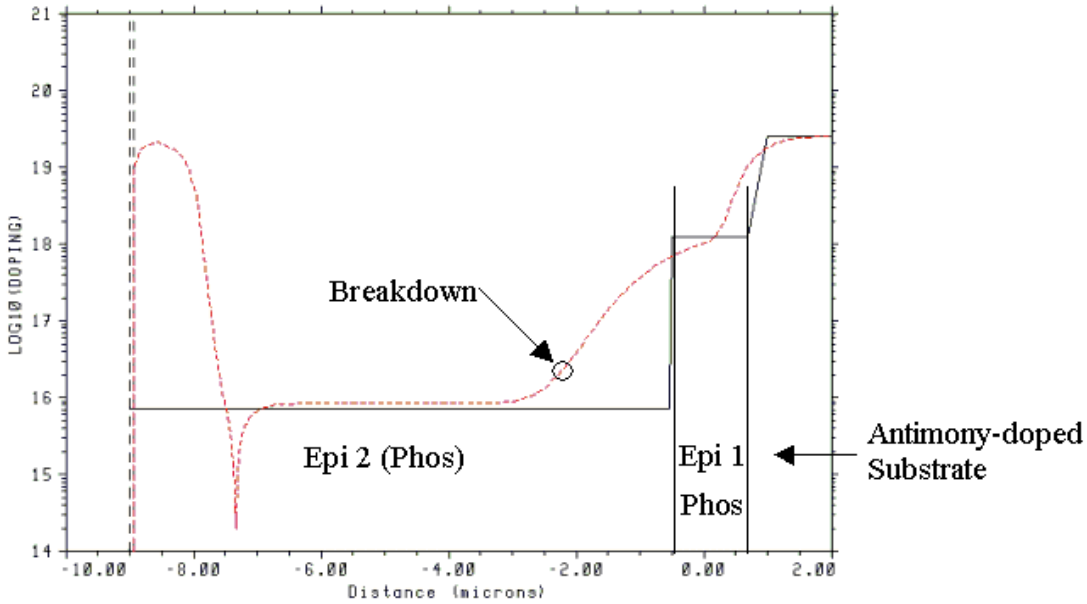


Figure 4-10: Vertical doping profile along drift region and substrate pre-fabrication (solid line) and post-fabrication (dashed line)

4.4.3 Oxide over etch at termination

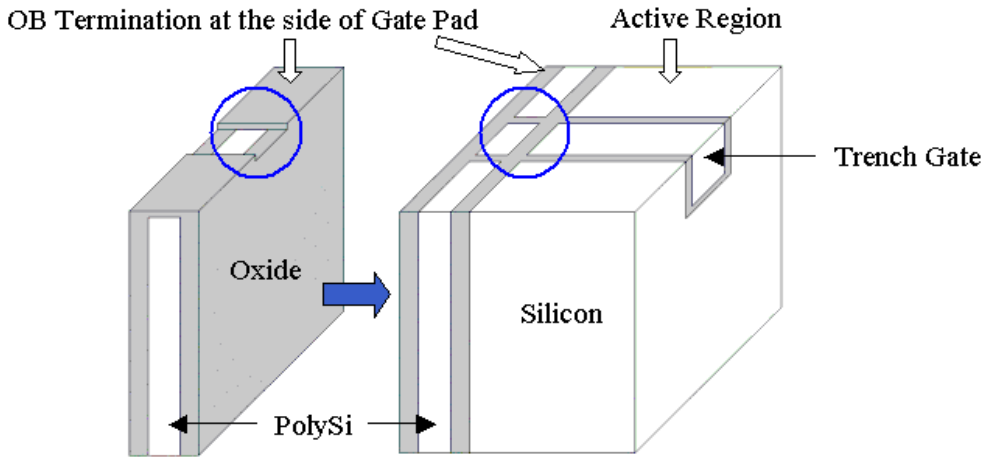


Figure 4-11: Failed structures with slight oxide etch at gate region before and after gate formation

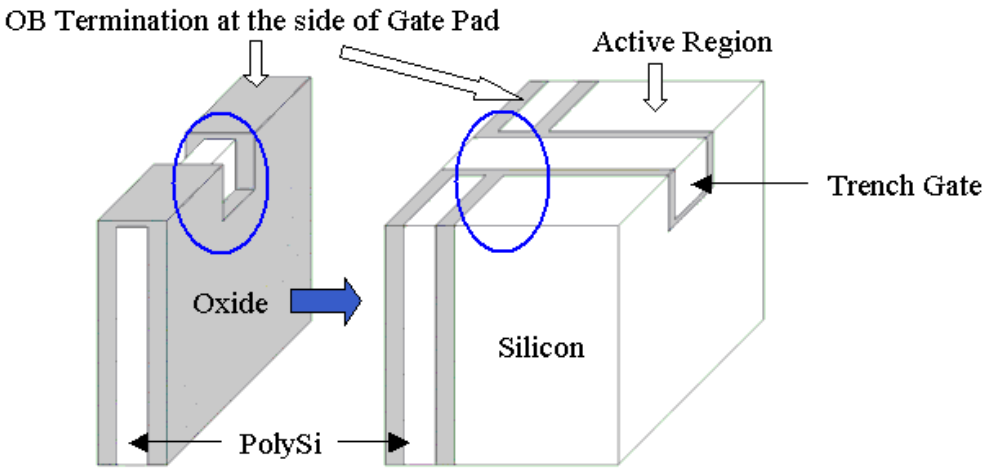


Figure 4-12: Functional structures with oxide over etch of 1~2μm at gate region before and after gate formation

As mentioned at the beginning of this chapter, in previous OBUMOS fabrication, most likely due to the discontinuity of Gate poly at OB termination, as shown in Figure 4-11, the Gate is electrically open since the Gate contact is only on the OB termination. Therefore, Oxide etch in OB region is required to be deep enough to make Gate poly going across. Normally, 1~2 μm Oxide over etch (See Figure 4-12) is desired for 2μm Gate trench.

To check the Oxide over etch depth at the termination mentioned above, a test structure as shown in Figure 4-8 and Figure 4-13, was designed for SEM test. Thus, by simply cutting the wafer along any horizontal line, the cross section view of Gate trench at OB termination can be seen clearly using SEM.

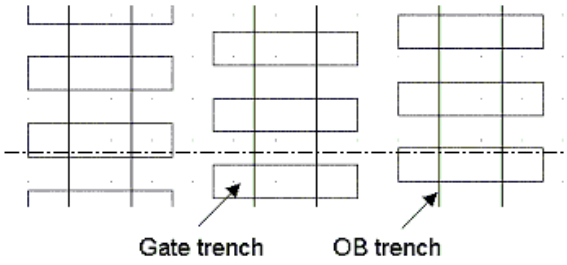


Figure 4-13: Gate trench Test structure

4.4.4 Resist-assisted etchback applied on PolySi removal

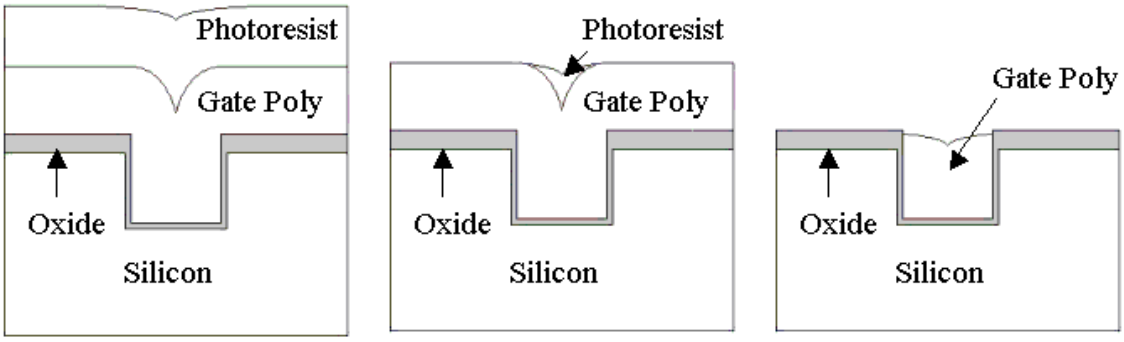


Figure 4-14: Gate Poly removal by using resist-assisted etchback technology

Although in principle, Polysilicon CMP is a straightforward technology applied on Gate Poly etching for UMOS devices, it is actually quite complex in practice. Proper controls must be guaranteed to yield a uniformly polished surface. Instead, resist-assistant etchback is simple to remove Gate poly and outcome a relatively planar surface. As given in Figure 4-14, photoresist is deposited onto Polysilicon. By using photoresist to fill up the notch of Polysilicon, a smooth surface profile can be patterned easily.

Chapter 5

100V TOBUMOS Measurement Results and Discussions

The fabrication of TOBUMOS was performed in IME on two types of dual-epi Silicon wafers. As described previously, simulated TOBUMOS devices show good performance on both on state and off state in comparison to conventional MOSFETs. It is verified on tunable OB-Diode that the tuning effect functions well on improving the breakdown voltage. In the same way, Drain current at on state can be improved as well under certain control bias. This effect allows the non-optimized OB devices to have a superior performance after being tuned. This chapter deals with the details of fabrication and analyses on measurement results.

5.1 Physical parameter measurements on fabricated TOBUMOS

Figure 5-1 shows the device active region after OB trench etching. To raise the operating current, there are actually 10 TOBUMOS device fingers paralleling to each other, sharing the same electrodes. As is shown that, device active region is surrounded by the OB structure. Apart from the top region, OB trenches are continuous elsewhere. The outside OB structure acts as the termination as well. Because of the good conductivity of the highly doped Polysilicon in between, the contact for Control electrode can be open at the lower side of OB termination only. The top OB trench, namely Gate OB trench, is the underlay isolation for Gate contact formation. Drain electrode is made at the bottom of the wafer.

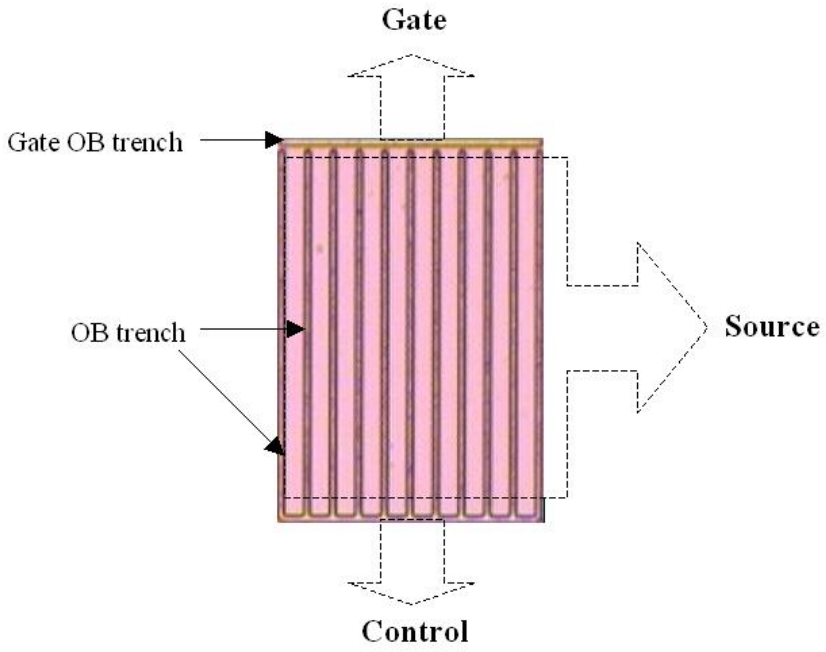


Figure 5-1: Top view of TOBUMOS device active region after OB trench etching under microscope

Figure 5-2 is the SEM picture showing the cross section view of TOBUMOS after OB trench etching. The 10μm deep trench sidewall is straight and it has a round trench corner at bottom as expected.

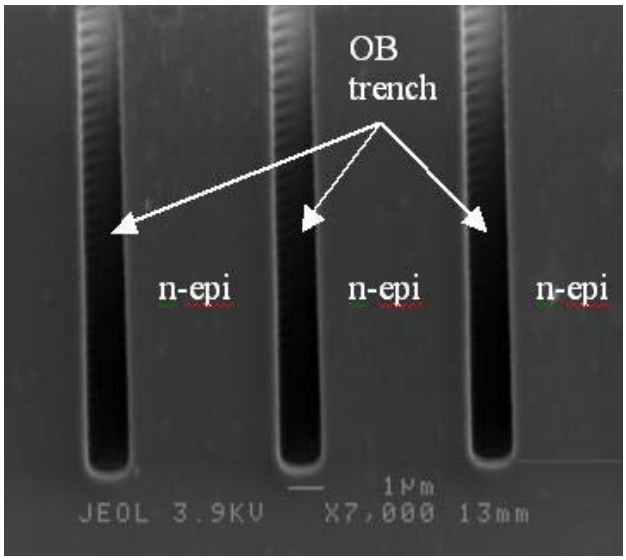


Figure 5-2: SEM picture for TOBUMOS cross section after OB trench etching

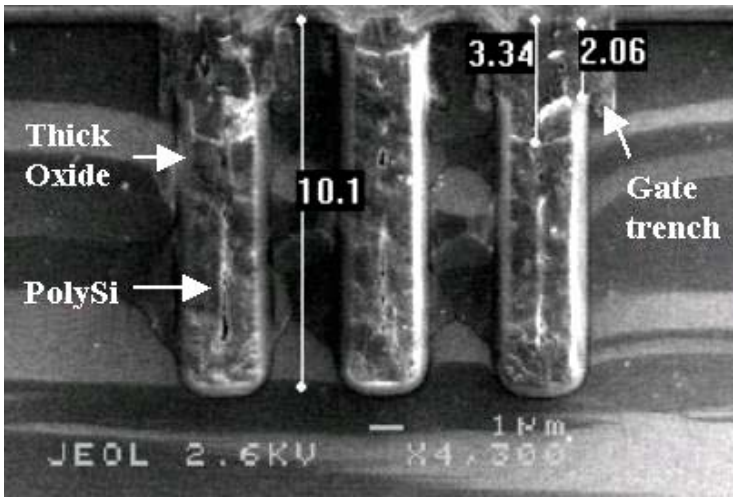
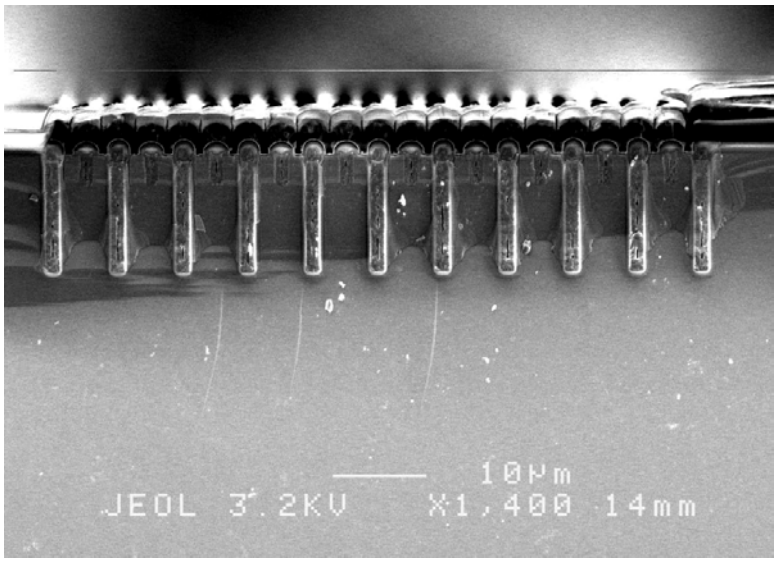


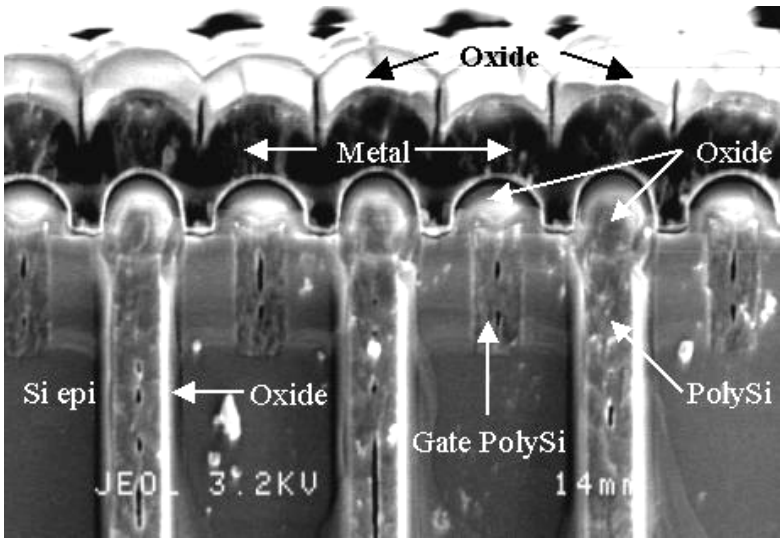
Figure 5-3: SEM picture for Gate trench test structure

The SEM picture of the test structure (according to Figure 4-13) for Oxide over etch at termination is shown in Figure 5-3. As described in Figure 4-12, at termination region, 1~2μm Oxide over etching is required to make the connection of PolySi in both Gate trench and OB trench regions. It is measured that, the Oxide over etching depth is about 2.06μm, while measured Si trench depth in Gate region is about 2.5μm. When doing the Si etching in Gate region, the etching rate for PolySi is higher than that of Si. This results in a deeper PolySi trench depth of 3.34μm as given in Figure 5-3.

SEM pictures under the acceleration voltage of 3.2 KV were taken for the final TOBUMOS structure as shown in Figure 5-4. This cross section view is obtained by cutting the device along the line perpendicular to Gate trench in active region. The entire structure and enlarged picture for Gate region are shown in Figure 5-4(a) and Figure 5-4(b), respectively. It is clear that the Source metal strides over the active region and the Source contact is open between Gate and OB trenches. Both Gate and OB trenches have the round Oxide profile at the trench corner. The Oxide thickness t_{ox} is designed to vary from 0.4μm to 0.6μm. The spacing between OB trenches is in the range of 3μm to 6μm.



(a)



(b)

Figure 5-4: SEM pictures for fabricated TOBUMOS

5.2 Tunable effects on breakdown voltage of TOB-Diode

Fabrication of TOB-Diode was done to verify the TOB concept. The top views of the device after OB trench etching and post-fabrication are given in Figure 5-5. Except for the absence of Gate structure and the close OB region, the device structure and dimensions are as same as in TOBUMOS.

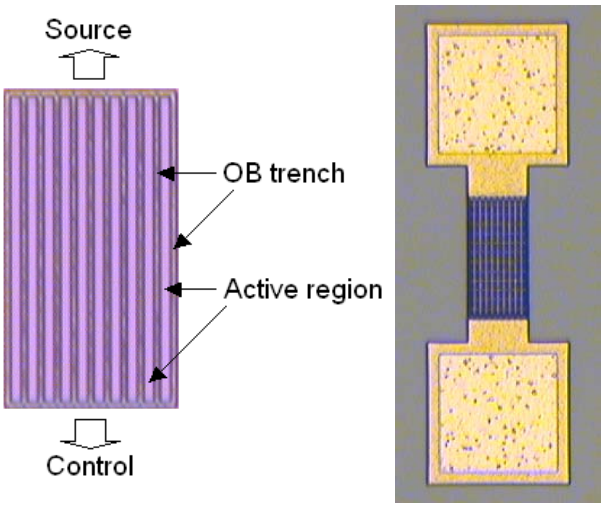


Figure 5-5: Top views of TOB-structure under microscope, after the step of OB trench etching (left) and post-passivation (right)

Without external bias, the breakdown voltage of TOB-Diode based on the epi resistivities of 0.55Ω-cm and 0.7Ω-cm is 83V and 82V, respectively. The comparisons of measured blocking characteristics of TOB-Diode under positive bias and conventional Diode fabricated on the same wafer of 0.55Ω-cm epi are shown in Figure 5-6 and Figure 5-7.

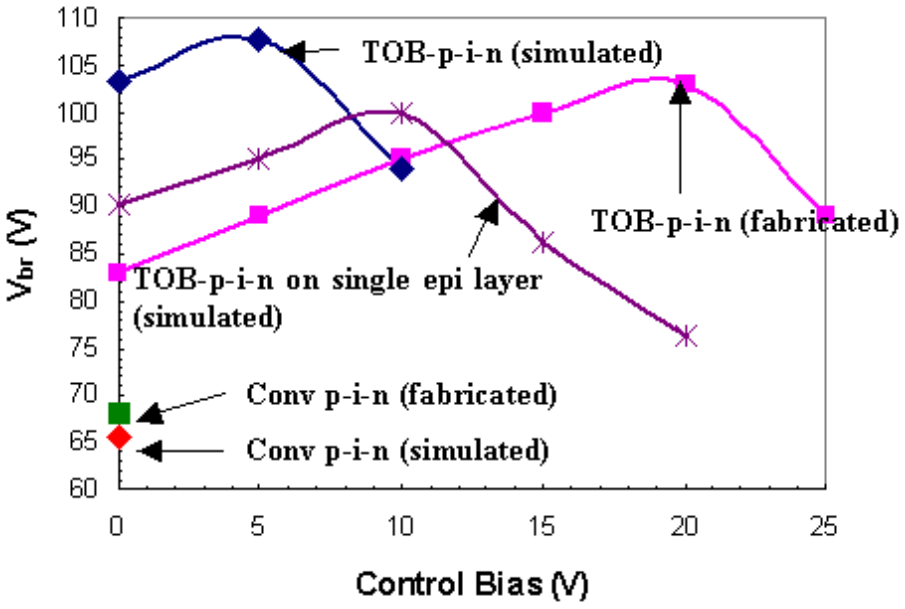


Figure 5-6: Breakdown voltage under positive control bias for TOB-structure and conventional structure on the same epi wafer

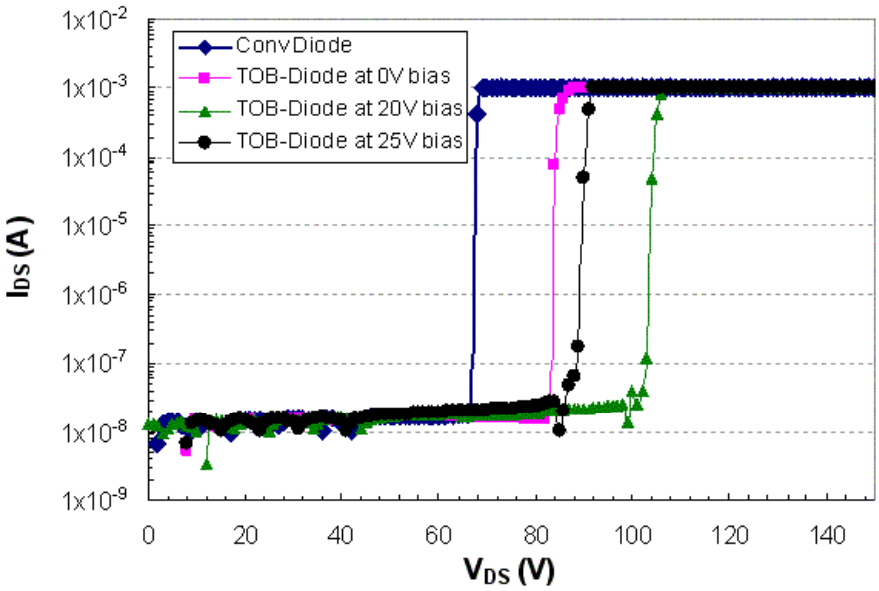


Figure 5-7: Measured blocking characteristics of TOB-p-i-n structure under 0V, 20V and 25V control biases on epi resistivity of 0.55Ω-cm in comparison with the conventional structure fabricated on the same wafer.

The V_{br} for both cases are not much higher than that of conventional Diode. The maximal V_{br} that TOB-Diodes can reach are 103V at 20V Control bias on the epi resistivity of 0.55Ω-cm and 112V at 30V Control bias on the epi resistivity of 0.7Ω-cm, respectively. As is known that, OB structure is sensitive to the dimensions of W, t_{ox} and n-drift doping concentration (N_d), but accompanied with the tuning effect as in TOB devices, some variations of parameters in fabrication will not bring too much influence on the device performance. Most probably due to variations of epi doping, the V_{br} of fabricated TOB-Diode without Control bias is about 15V lower than the result expected by simulation. However, adjusted by the Control voltage, a V_{br} higher than 100V can be obtained. It is clear that, the introduced of TOB structure represents good tunable characteristics without bringing on any leakage current to the device. Theoretically, TOB structure also has the ability of enhancing on-state resistance and transconductance if applied on the MOSFET. The successfully fabricated TOB-Diode will be the foundation of continued research on TOB-MOSFETs fabrication.

5.3 Experimental results on TOBUMOS

TOBUMOS devices are fabricated together with TOB-Diode on the same wafer. Unfortunately, the first separate run of TOBUMOS fabrication was not fully successful. Though the fabricated TOBUMOS expresses good IV characteristics and improved specific on-resistance under certain Control voltage, it was found that the breakdown voltage is always about 30V and the breakdown measurement manifests unrepeatable. By performing the electrical test and analysis on Gate region, the Gate Oxide breakdown near termination region was suspected. Therefore, follow-up efforts were performed in order to solve the problem of premature breakdown.

5.3.1 Fabrication results on 1st separate run

(a) On-state performance

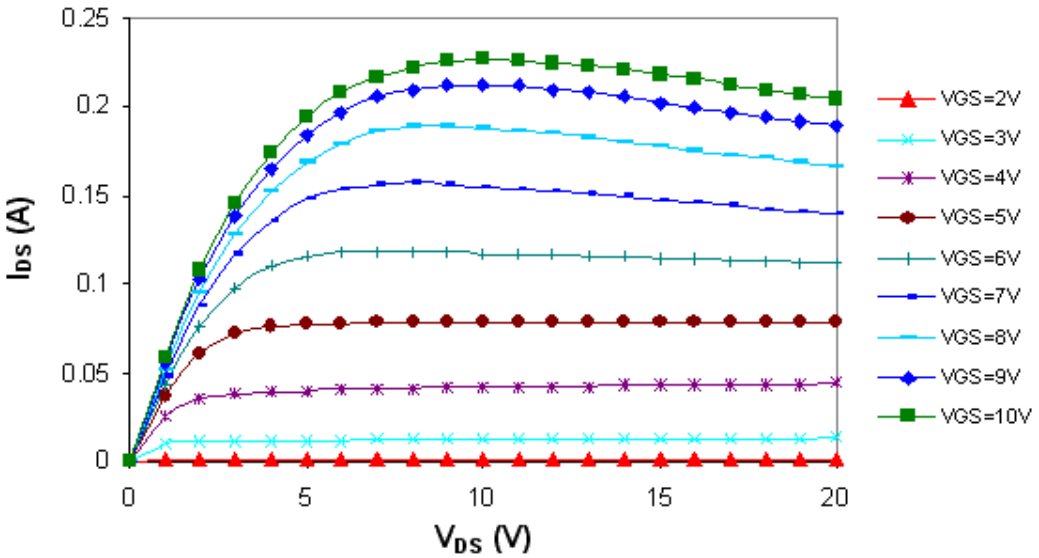


Figure 5-8: IV characteristics of TOBUMOS with W = 4.0μm, Wob = 1.5μm and Lg = 0.8μm (refer to Table 4-2) on wafer #06 at V_{GS} in the range of 0V to 10V

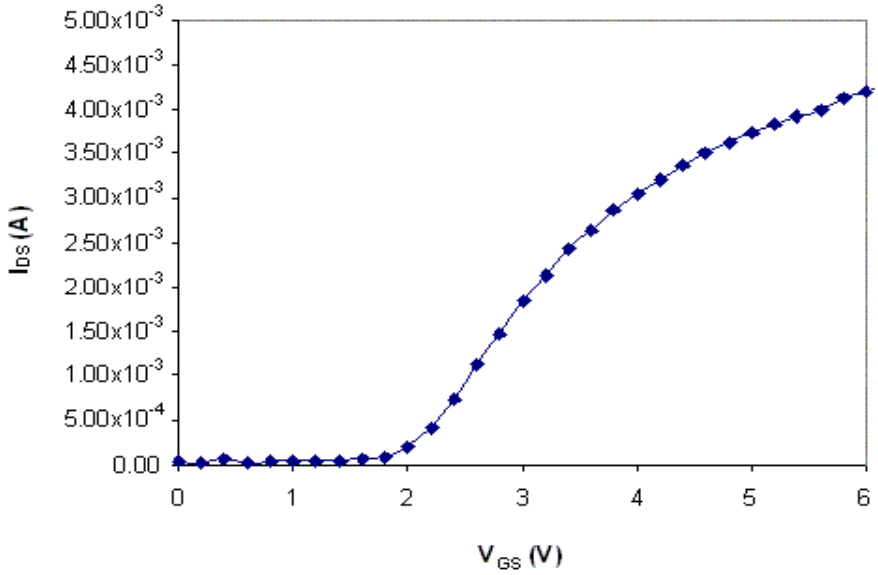


Figure 5-9: Drain current performance of TOBUMOS on wafer #06 at V_{GS} in the range of 0V to 6V and V_{DS} = 0.1V

Fabricated TOBUMOS was tested having normal IV characteristics. Figure 5-8 shows the Drain current vs. Drain voltage on wafer # 06 at different Gate voltages from 0V to 10V at 1V interval, without Control voltage. Measured threshold voltage as in Figure 5-9 is about 2V, which is higher than the simulated value of 1.2V.

(b) Tuning effects on TOBUMOS

It was found that by applying positive voltage on Control electrode, the on-state performance of TOBUMOS is enhanced. As given in Figure 5-10, the plots of IV characteristics of TOBUMOS under 20V Control bias are shown in comparison of the original IV performance without external bias. The enhanced Drain current under bias can be obtained in both linear region and saturation region of the MOSFET. The enlarged IV curve at V_{GS} = 10V at smaller V_{DS} below 0.1V is shown in Figure 5-11. Obviously, with the augment of I_{DS}, on-state resistance is improved when increasing the Control bias from 0V to 20V.

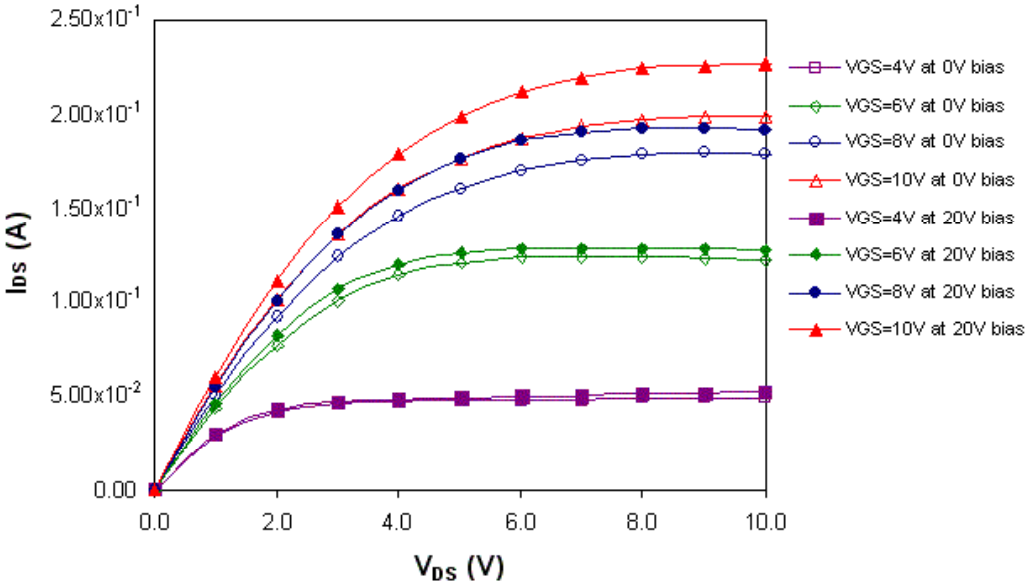


Figure 5-10: IV performance under positive Control bias of 0V and 20V for TOBUMOS with W = 3.5μm, Wob = 1.5μm and Lg = 0.8μm (refer to Table 4-2) on wafer #19, at V_{GS} = 4, 6, 8 and 10V, respectively

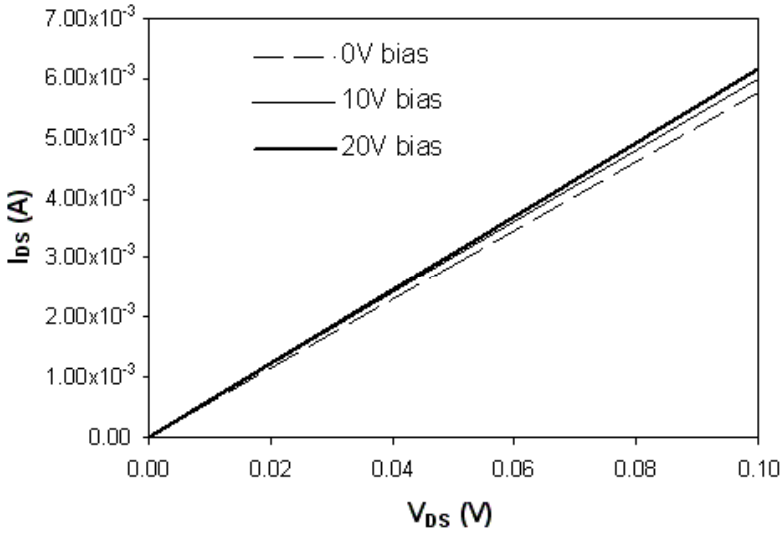


Figure 5-11: IV performance under positive Control bias of 0V, 10V and 20V for TOBUMOS with W = 3.5μm, Wob = 1.5μm and Lg = 0.8μm (refer to Table 4-2) on wafer #19, at V_{GS} = 10V

(c) Investigations for Off-state failure

Measured breakdown voltage for most fabricated TOBUMOS is below 30V, only on wafer #19, one or two devices were found to have the breakdown voltage of about 80V. There is no device showing an expected V_{br} of about 100V as desired. Moreover, in

any case, the breakdown test is unrepeatable. As shown in Figure 5-12, the breakdown test shows that the device has a V_{br} of 78V at first. Afterwards, V_{br} becomes below 5V for the following test. It was suspected that the dielectric breakdown happens at Gate Oxide region. Some measurements in sequence were then performed to confirm this suspicion.

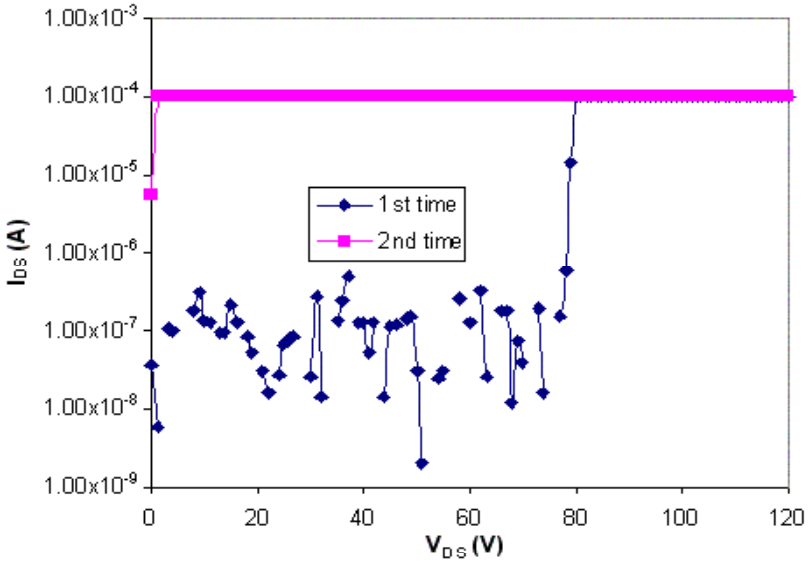
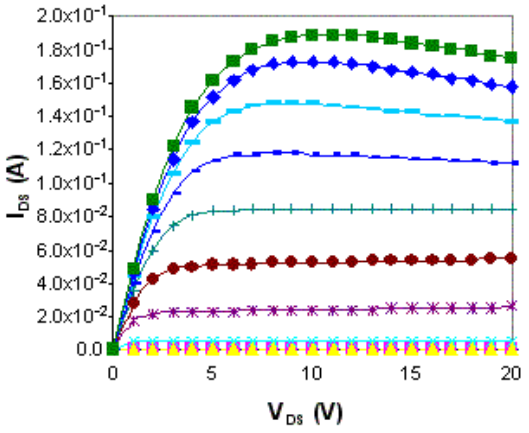
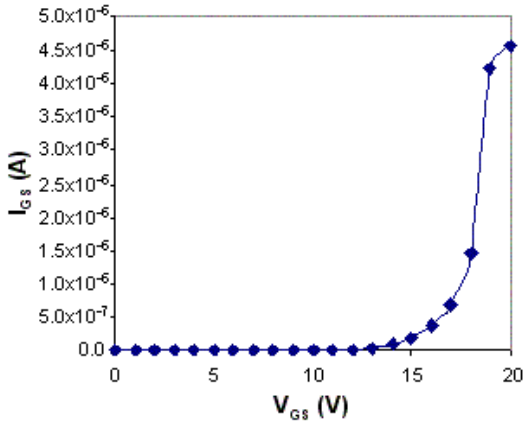


Figure 5-12: Measured off-state performance for TOBUMOS with W = 4.5μm, Wob = 1.5μm and Lg = 0.8μm (refer to Table 4-2) on wafer #19

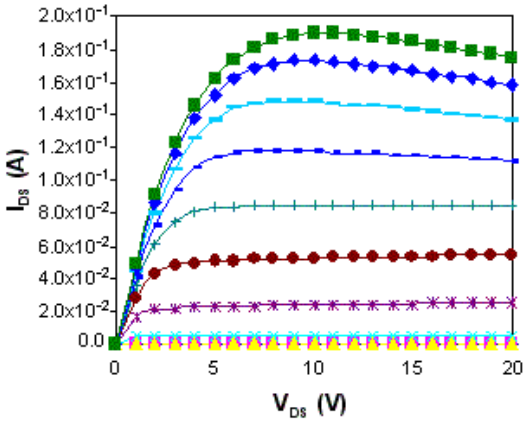
As given in Figure 5-13, a TOBUMOS on wafer #16 was tested having a normal IV performance at first. When testing the Gate current vs. Voltage performance, it shows Gate breakdown voltage of about 15V. In theory, with 430 Å Gate Oxide, the TOBUMOS should have at least 30V Gate breakdown voltage. When the Gate current limit is set to be very small, normal IV curves are still available afterwards as shown in Figure 5-13(c). However, after the Drain breakdown test, Gate leakage current becomes very large at small Gate bias and there is no good on-state performance that can be measured. Hence, Gate Oxide thinning at some locations is suspected to be a possible reason.



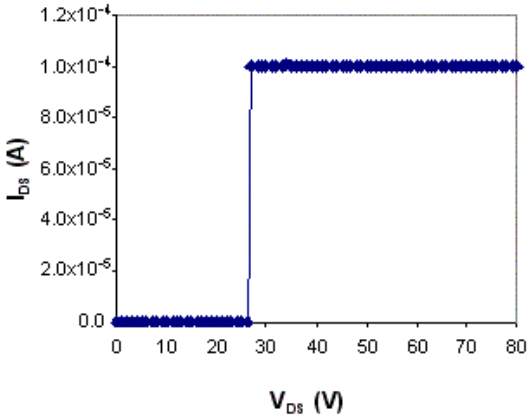
(a) Step 1: On-state characteristics



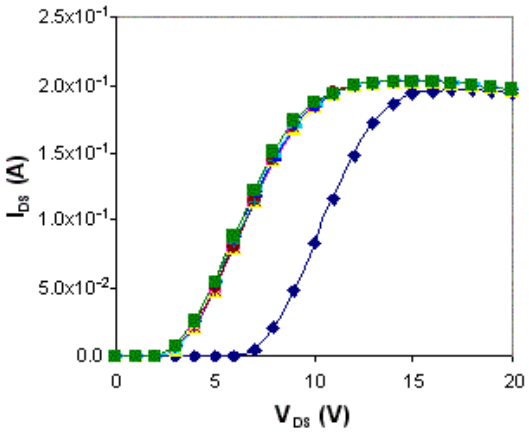
(b) Step 2: Gate breakdown



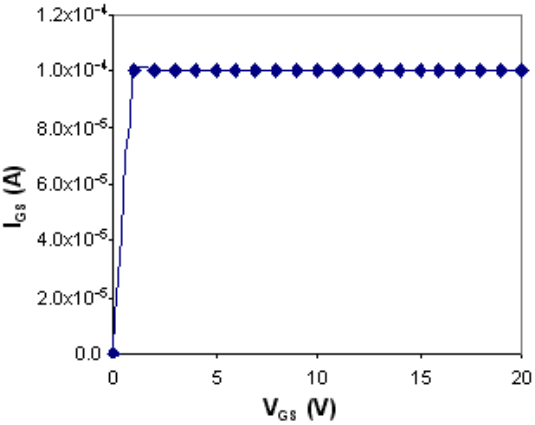
(c) Step 3: On-state characteristics



(d) Step 4: Drain breakdown



(e) Step 5: On-state characteristics



(f) Step 6: Gate breakdown

Figure 5-13: Measurement in sequence on TOBUMOS with W = 4.0μm, Wob = 1.5μm and Lg = 0.8μm (refer to Table 4-2) on wafer #16

(d) Hot spot analysis on TOBUMOS

To further investigate the mechanism resulting in the premature breakdown, the devices were imaged using an infrared photoemission microscope (IRPEM) operating in the wavelength range 800nm - 2400nm. The hot spot images by using this method are shown in Figure 5-14, where the TOBUMOS with termination type 1 (left) has the V_{br} of 25.4V, while for TOBUMOS with termination type 2 (right), the V_{br} is 28V.

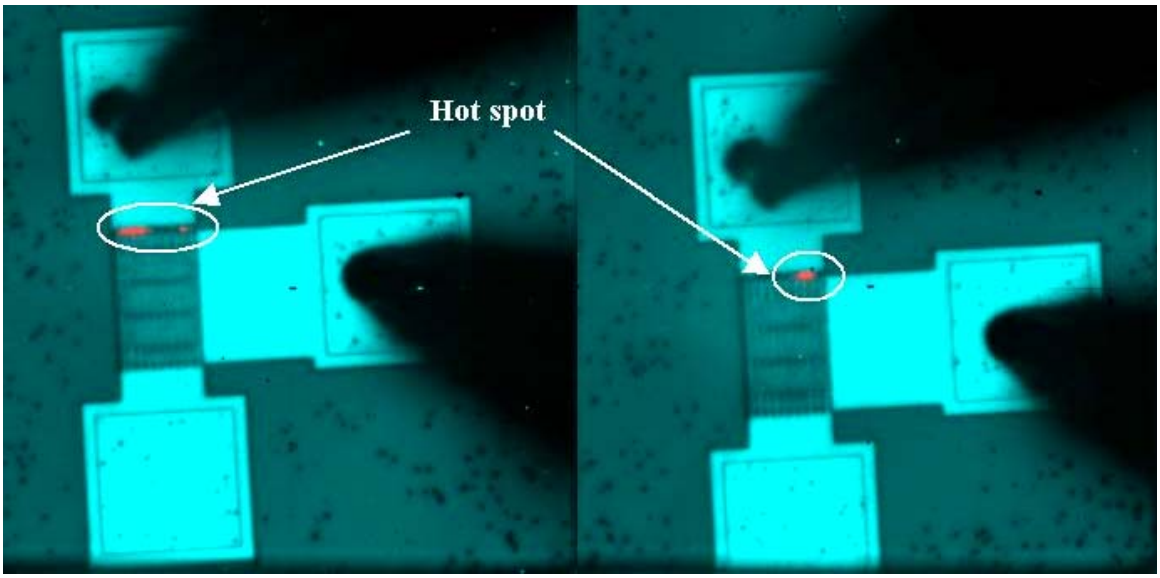


Figure 5-14: Hot spot images of TOBUMOS with two termination structures at breakdown, using an infrared photoemission microscope

It is clear that, for both of the cases shown above, the breakdown always happens at the top termination region. Thus, it is concluded that early breakdown happens most probably because of the weakness of Gate Oxide at top termination region.

5.3.2 Fabrication results on 2nd separate run

Device parameters for TOBUMOS at termination were checked to analyze the possible way to solve the problem of early breakdown. It was found that the minimum perpendicular OB trench gap at top termination region is 0.8μm, which is still larger than the required maximum Oxide thickness of 0.6μm in OB region. Therefore, after

the thermal Oxide growth, there is at least 0.2μm gap left in between the thick Oxide. This may result in the current leakage and a high electric field near the Gate Oxide region at the termination. In addition, due to the phosphorous segregation effect during Oxidation, the doping concentration nearby the termination is higher. Both of the reasons above are likely to cause the electric field crowding at Gate region, which leads to the premature Gate breakdown.

(a) Remedial process steps

To avoid the effect of high electric field acting on the termination region, 4μm Silicon trench dry etching followed by 2~3μm Silicon release etching and Oxide refill were added into the process at the top termination region.

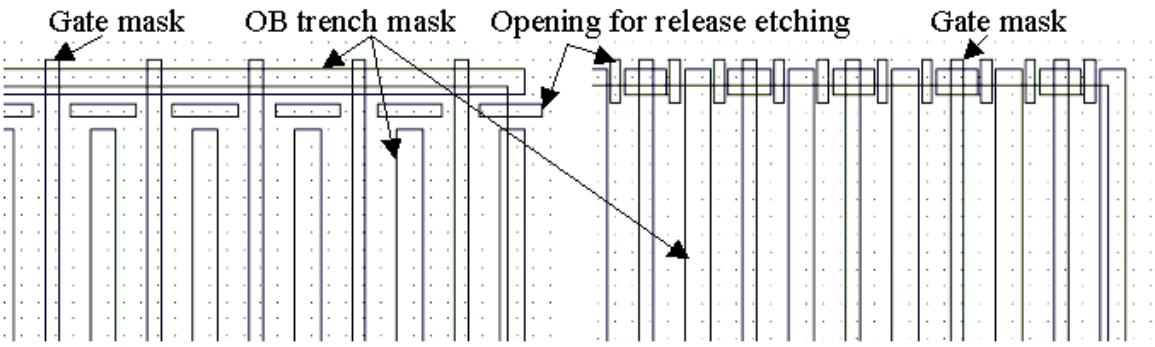


Figure 5-15: Release etching mask added for TOBUMOS on two types of terminations

The mask layout is shown in Figure 5-15. In the gap of perpendicular OB trenches, there is a group of square window openings for the abovementioned Silicon etching. Depending on the space, the width of opening varies from 0.5μm to 0.8μm. For termination type 1, lateral distance between opening and the edge of Gate trench is fixed at 0.7μm. Thus, to merge neighboring cavities done by Silicon wet etching, at least 1.2μm lateral encroachment is required.

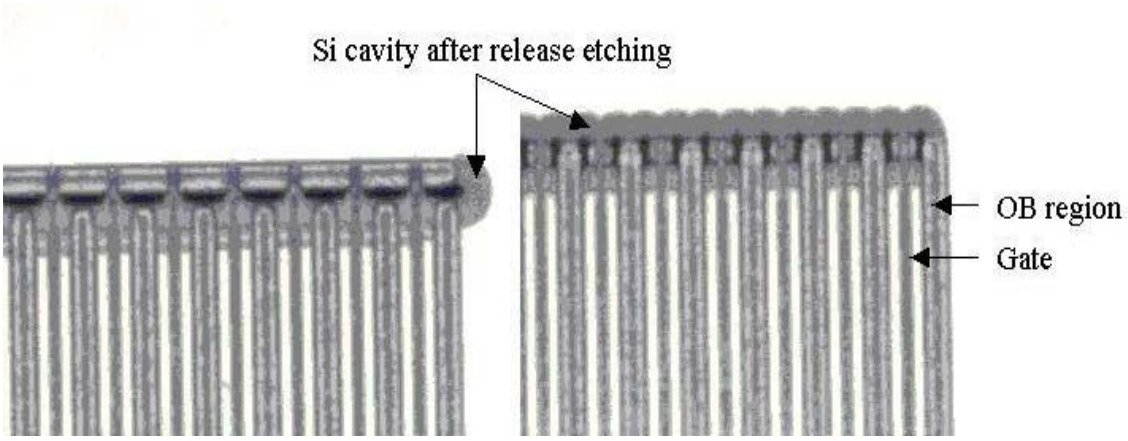


Figure 5-16: Images under microscope after release etching for both types of terminations

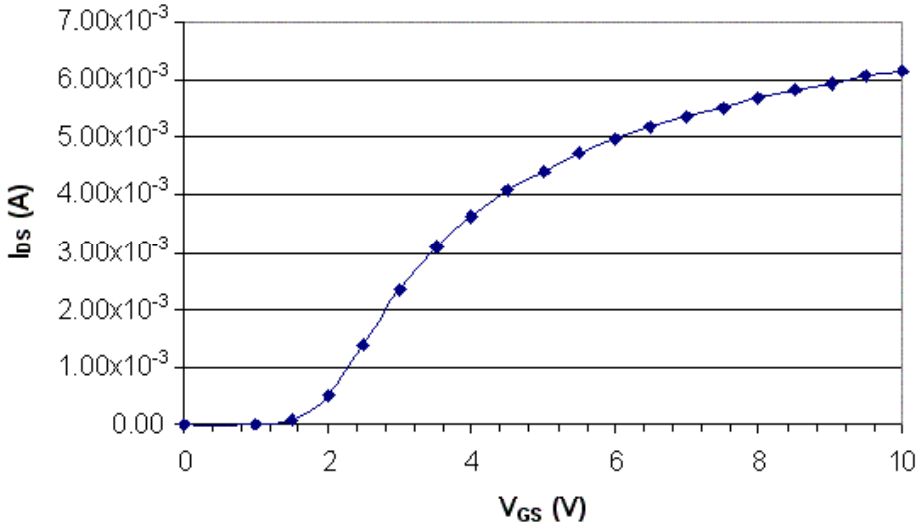
The images under microscope after release etching process are shown in Figure 5-16. The recipe for Silicon wet etching is selected using XeF2, which has high selectivity of Silicon to Oxide. Therefore, the etching process has no effect on Gate Oxide region. It is obvious that, after release etching, Gate trenches at top termination region are surrounded by a Silicon cavity underneath, which will be filled with Oxide afterwards. Thus, the Gate region is isolated at termination and thus it will not be affected easily by high electric field and Phosphorous segregation effect. OB-MOSFETs undergoing the process of Silicon release etching have the distinct improvement on breakdown voltage.

(b) Measurement results on TOBUMOS

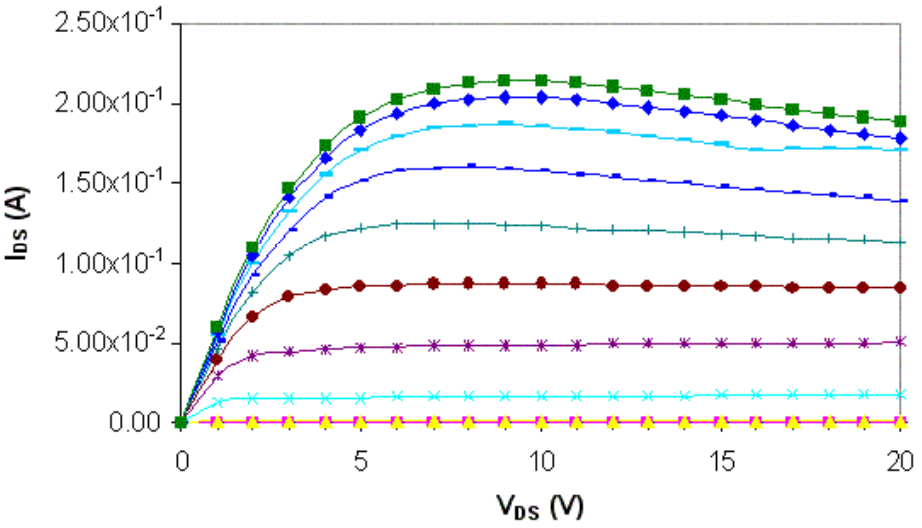
TOBUMOS devices with breakdown voltages ranging from 70V to 80V are found on Wafer #01 with the epi resistivity of 0.55Ω-cm in device drift region. The best result obtained on wafer #01 is the device, which has mesa width W of 3.5μm. The breakdown voltage measured on this device is 76V without Control bias and 79V under 5V Control voltage, while on the same wafer, breakdown voltage for

conventional Diode is 66V. The electrical on-state and off-state performance tested on this device is shown in Figure 5-17.

As shown in Figure 5-17(a), measured threshold voltage at V_{DS} = 0.1V is similar to the value obtained from the 1st separate run. It is 0.6V higher than the simulation result. This TOBUMOS has normal IV curves at on state as in Figure 5-17(b). The off-state performance of TOBUMOS is given in Figure 5-17(c).



(a)



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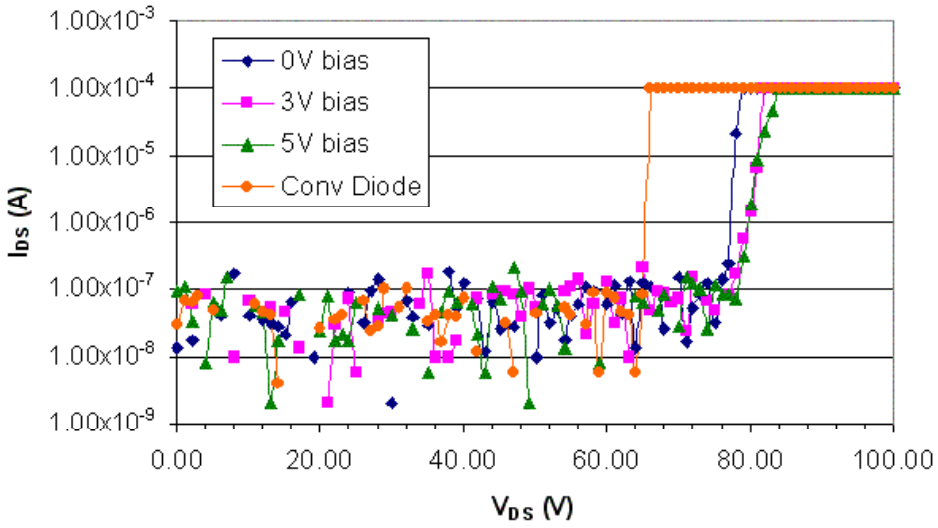

(c)

Figure 5-17: Measurement results on TOBUMOS with W = 3.5μm, Wob = 1.0μm and Lg = 1.0μm (refer to Table 4-2) on wafer #01 (a) Gate performance at V_{DS} = 0.1V (b) On-state IV performance (c) Off-state performance at Control Voltage varying from 0V to 5V compared to that of conventional Diode on the same wafer.

The reason why V_{br} of TOBUMOS is lower than that of TOB-Diode is probably due to the increasing depth of trench Gate. Though 2μm deep Gate trench is desired from simulation, real process results in a 0.5μm deeper Gate trench. According to the simulation, increase of Gate trench depth leads to the premature breakdown happening near the corner of Gate Oxide due to the high electric field nearby. As the positive Control voltage squeezes the depletion region into upper part of the n-drift region causing the electric field crowding near p-body-n-drift junction. TOBUMOS with the trench Gate structure in p-body region also handicaps the increase of Control voltage. Unlike TOB-Diode structure, the tunable Control voltage is only helpful in the range of 0V to 5V. When the external bias is higher than 5V, breakdown voltage of TOBUMOS tends to drop. Since at 5V bias, there is no improvement of breakdown voltage compared to that at 3V bias, further increase of Control voltage is not presented in Figure 5-17.

Experimental result shows that, maximum V_{br} measured on TOBUMOS with W = 3.5μm is 79V under 5V Control voltage. It is clear that, the introduction of TOB structure represents good tunable characteristics without bringing on any leakage current to the device. The corresponding $R_{on,sp}$ is tested to be 0.674 mΩ-cm^2 at the current density of 100A/cm^2.

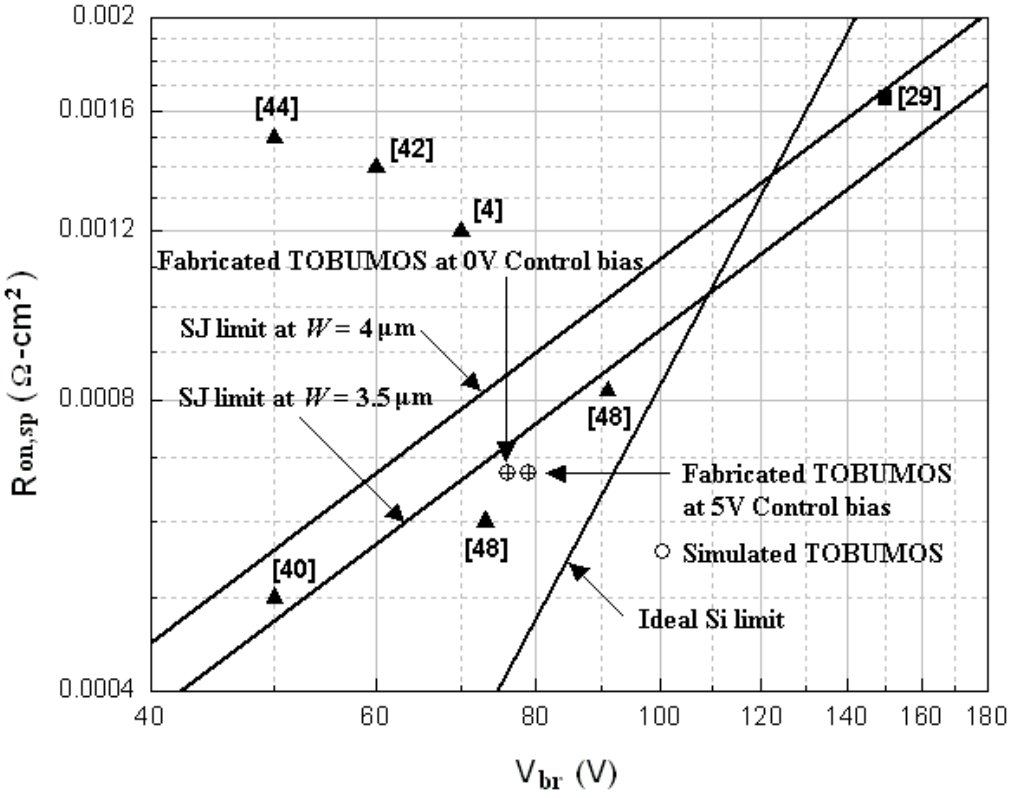

Figure 5-18: $R_{on,sp}$ vs. V_{br} for simulated and fabricated TOBUMOS together with the ideal silicon limit [6], SJ limit at W = 3.5μm and 4μm [6] and previous published devices [4, 29, 40, 42, 44, 48].

The V_{br}~$R_{on,sp}$ performance of simulated and fabricated TOBUMOS is shown in Figure 5-18, together with the ideal silicon limit [6], SJ limit at W = 3.5μm and 4μm [6]. At the same $R_{on,sp}$ of 0.674 mΩ-cm^2, ideal SJ devices can sustain the V_{br} of 71V, which is 10% lower than that of fabricated TOBUMOS. Thus, fabricated TOBUMOS can break the ideal SJ limit at this voltage range. Though fabrication result of TOBUMOS shows no better performance than ideal silicon limit, it is definitely superior to other

previously fabricated conventional VDMOS and UMOS devices [4, 40, 42, 44] and SJ MOSFET [29]. It is also comparable to newly fabricated trench LDMOS [48]. In the voltage range below 100V, no SJ device has ever been fabricated.

5.4 Conclusion

In this chapter, fabricated tunable Oxide-Bypassed device and the experimental electrical performance are presented for the first time. Adjusted by the Control voltage, enhancement of V_{br} is found and the $R_{on,sp}$~V_{br} point of TOBUMOS can be tuned further away from the ideal SJ limit. TOBUMOS exhibits the simple technology compared to the SJ technology as well as the superior performance of breaking the ideal SJ limit. It is proposed to be the replacement for SJ devices in certain applications.

Chapter 6

Concerns for Future Fabrication

Currently, vertical SJ devices have been fabricated commercially to replace ordinary power MOSFETs in certain applications. By combining the advantage of SOI technology, such as reducing parasitic capacitance and leakage currents, SJ structure can be further applied on LDMOSFETs. This makes the SJ structure more attractive on the application of smart power integrated circuits. However, because of the charge compensation theory involved, an SJ device with ideally charge balanced p/n columns is very difficult to realize. Being free of the restriction of charge balance problem, the Oxide Bypassed MOSFET has been developed. Though it can be fabricated with relatively simple process compared to COOLMOS technology and has been proven of having the superior blocking capability compared to conventional MOSFETs, it sacrifices the blocking voltage in comparison to SJ devices. For these reasons, some efforts are proposed to push the OB and SJ devices farther away from the ideal Silicon limit.

6.1 Gradient Oxide Bypassed (GOB) structure

It is known that in OB devices, electric field distribution in the vertical direction is not as uniform as in SJ devices. Along the vertical line passing through the center of n- drift region, it peaks at both p-body bottom and near OB trench bottom, but is lower in between. If the lower part of electric field can be raised up, higher breakdown voltage will be achievable. One way to ameliorate the electric field profile and blocking

capability is to apply a gradient Oxide sidewall at the inner-side of OB structure with thicker Oxide at bottom but thinner Oxide at top region, as shown in Figure 6-1.

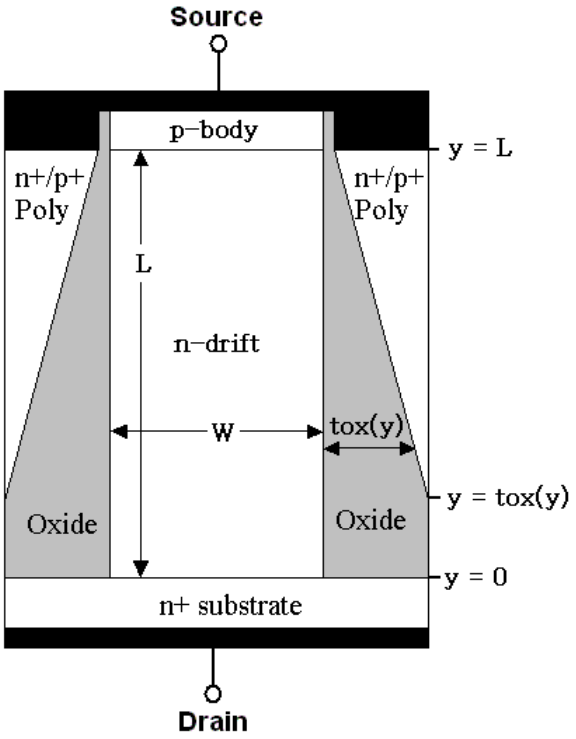

Figure 6-1: Proposed Gradient OB model

6.1.1 Theory of GOB structure

As is known that, in ideal SJ structure just before breakdown happens, if ignoring the electric field near p-body and substrate region, the y component of electric field (E_y) keeps constant in the entire drift region and x component of electric field (E_x) is constant in vertical direction but varies horizontally. Under certain positive V_{DS} bias, the voltage is highest at substrate and drops from bottom to the top. Therefore, the voltage drop on Oxide in horizontal direction must be highest at bottom and is linearly reduced down to zero near the bottom of p-body region. Thus, to ensure the constant electric field at Si/Oxide interface, Oxide thickness must be varied at different voltage level.

As shown in Figure 6-1, it is assumed that the Oxide region is in triangular shape and the oxide thickness $t_{ox}(y)$ is variable according to the depth y. Because the direction of electric field should be perpendicular to the hypotenuse, for a point at Si/Oxide interface with certain depth of y, there is such relationship as

$$\frac{t_{ox}(y)}{L-y} = \frac{E_{y,ox}}{E_{x,ox}} \tag{6.1}$$

where $E_{y,ox}$ and $E_{x,ox}$ are the y component and x component of the electric field in Oxide region, which is represented by E_{ox}.

It is assumed that there is no interface charge at the Silicon/Oxide interface. By applying the charge neutrality condition and Gauss' law on this Si/Oxide/PolySi structure, we have

$$E_{x,ox} \cdot e_{ox} = E_x \cdot e_{si} \tag{6.2}$$

and

$$E_{y,ox} = E_y \tag{6.3}$$

where $E_{x,ox}$ and E_x are the x components of constant electric field at Si/Oxide interface in Oxide region and Silicon region, while e_{ox} and e_{si} resprent the dielectric constants of Oxide and Silicon, respectively.

As is known in Chapter 2 that for SJ structures, E_x is proportional to the critical electric field (E_{crit}). For GOB structure, to compare with SJ devices, the N_d and W also have the relationship as described in Equation (2.15), where $W=d$ is the width of drift region. After careful analysis of E-field results from MEDICI simulations, According to the statistic results by MEDICI simulation, E_x can be expressed by

$$E_x \approx 0.710 E_{crit} \tag{6.4}$$

Substituting $E_{crit} = 4010 N_d^{1/8}$ [32] and $N_d = 1.2\times10^{12} \cdot W^{-8/7}$ into Equation (6.4), thus

$$E_x = 9.21\times10^{4} \cdot W^{-1/7} \tag{6.5}$$

By combining Equation (6.1), (6.2), (6.3) and (6.5), the approximal relationship of V_{br}, $t_{ox}(y)$, W and N_d is

$$t_{ox}(y) = 1.086\times10^{-5} \cdot \frac{e_{ox}}{e_{si}} \cdot (1-\frac{y}{L}) \cdot W^{1/7} \cdot V_{br} \tag{6.6}$$

Therefore, for a given breakdown voltage required, t_{ox} can be decided according to the value of W. Note that, this calculated $t_{ox}(y)$ is a bit higher that the value verified by simulation, it is because there is certain error from the equation of $N_d = 1.2\times10^{12} \cdot W^{-8/7}$. This relationship between N_d and W of SJ structure is based on the assumption that the charge contribution of p-body-n-drift junction is ignored under reverse bias. Thus, a bit higher N_d is required for optimal SJ structure in reality. The lower N_d used in deriving results in a slightly higher $t_{ox}(y)$.

6.1.2 Simulations on GOB structure

(1) T_{ox} variation

Device simulations were done to study the effects of t_{ox} on breakdown voltage of GOB structure. The simulation model is a GOB diode with epi doping concentration of 7×10^{15} cm^{-3}, epi depth of 15 μm and mesa width of 5 μm in drift region. As given in Figure 6-1, the Oxide thickness at the level of p-body bottom is chosen to be a small value of 0.1μm. By varying the bottom Oxide thickness t_{ox}, slope with different angles can be achieved for comparisons. The breakdown voltage vs. bottom Oxide thickness is plotted in Figure 6-2. It can be seen from Figure 6-2 that, when bottom Oxide

thickness is 2.5μm, the highest breakdown voltage of 289.3V is achieved. From Equation (6.6) we know that, calculated t_{ox} at bottom is 2.86μm, which is 14% higher than the simulation result. It is obvious that from Figure 6-2, when t_{ox} at bottom is in the range between 2μm and 2.8μm, the breakdown voltage is no lower than that of SJ devices. When t_{ox} further rises up from 2.8μm, premature breakdown happens due to the incompletely depleted drift region.

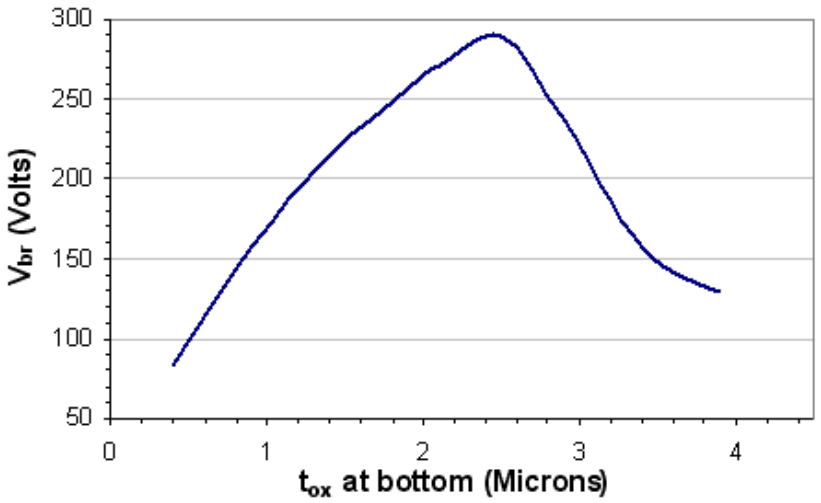

Figure 6-2: Effects of t_{ox} variations on breakdown voltage

(2) Performance of GOB devices

Comparisons were done on the performance of optimal SJ, OB and GOB Diodes at the same depth of 10μm and doping concentration of 9.2×10^{15} cm^{-3} in n-drift region. The optimal width of p/n column of SJ device can be calculated as 4μm. As shown in Figure 6-1, the vertical electric fields from p-body bottom to n+ substrate for different functional structures along the center of n-drift region are plotted. It was verified that compared to SJ structure, OB structure has the relative lower breakdown voltage. By plotting the electric field along the vertical line at the center of n-drift region, it can be seen that for OB structure, E-field is not centrosymmetric as in SJ structure.

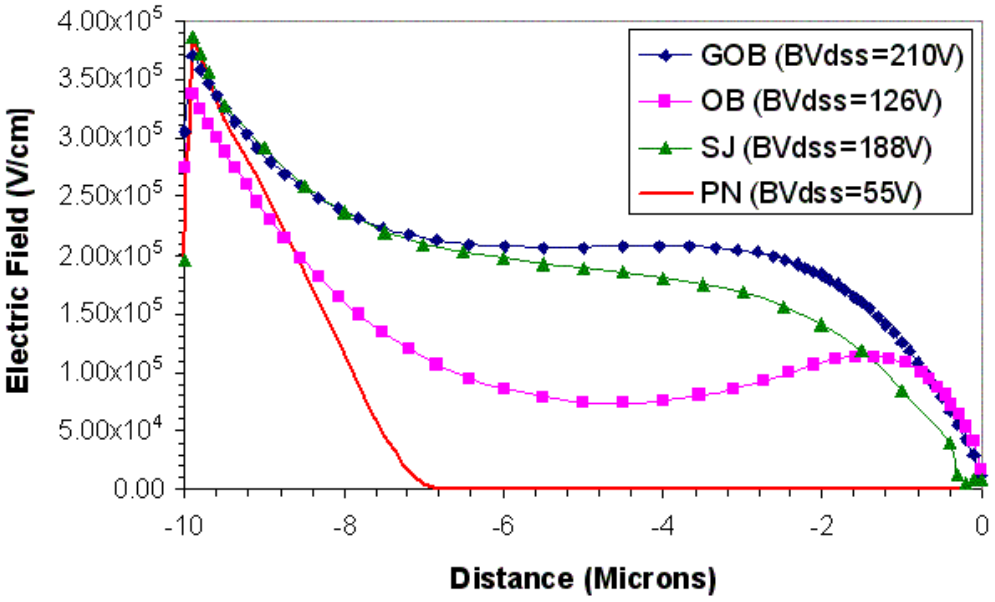

Figure 6-3: E-field plots for Conventional pn Junction, SJ, OB and GOB structures at the center of n-drift region, with L = 10 μm, N_d = 9.2×10^{15} cm^{-3} and W = 4 μm.

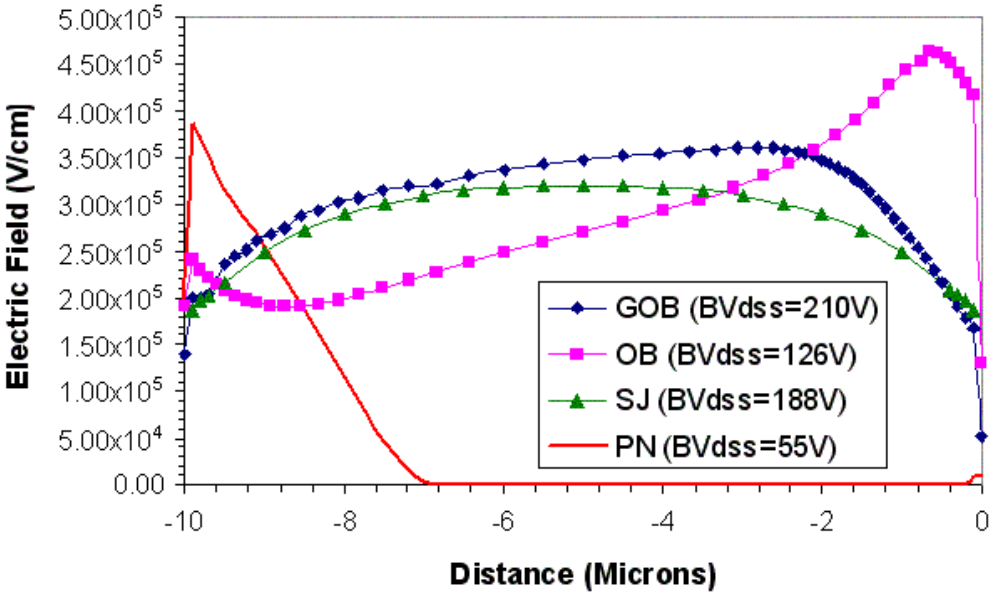

Figure 6-4: E-field plots for Conventional pn Junction, SJ, OB and GOB structures at the side n-drift region, with L = 10μm, N_d = 9.2×10^{15} cm^{-3} and W = 4μm.

Along the vertical line at the center of n-drift region, the voltage drops more at top region but less at bottom region, as shown in Figure 6-2. This makes OB structure

have an inferior blocking performance. In Figure 6-3, OB structure also shows much higher electric field at bottom of Si/Oxide interface, where the breakdown always happens.

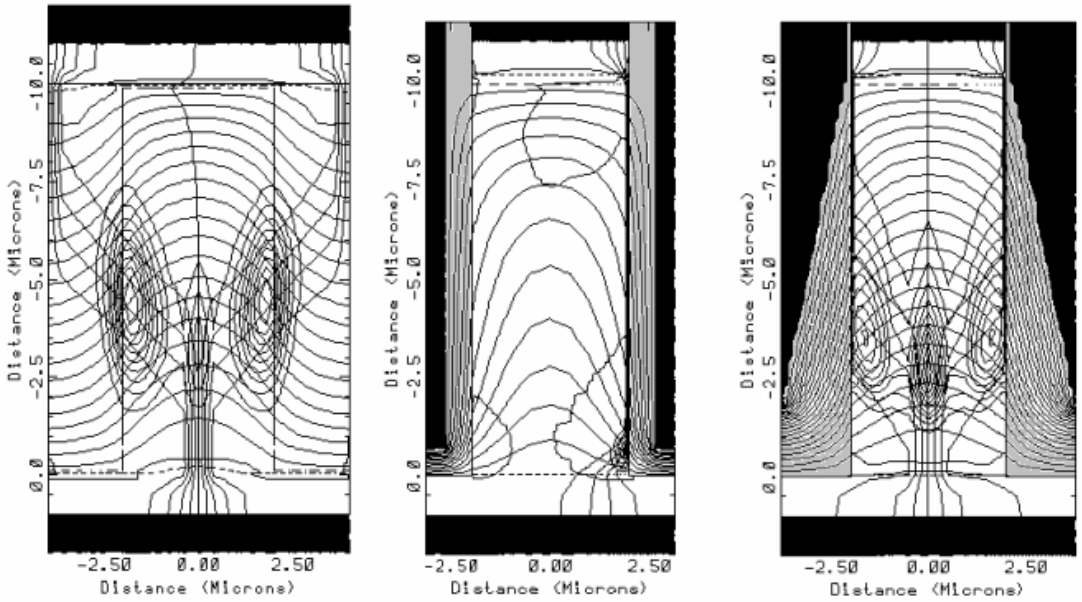

Figure 6-5: Comparison of vertical SJ (left), OB (middle) and GOB (right) Diodes at Breakdown. Parallel curves through p/n column junctions stand for potential contours at 10V interval, ringed curves stand for impact ionization and current lines flow vertically from Drain to Source via impact ionization datum.

Comparisons of SJ, OB and GOB structures at breakdown are given in Figure 6-5. All structures are simulated based on the same width, doping and depth of drift region. It is clear that compared to OB structure, the potential contours in GOB structure are well distributed at lower part of the drift region. Hence, the enhancement of breakdown voltage is apparent according to the integral of E-field of GOB structure as shown in Figure 6-2. Simulated V_{br} for different structures are listed in Table 6-1. In comparison to SJ structure, this novel GOB structure has higher breakdown voltage but smaller device area, which leads to lower specific on-resistance. It is without question that, GOB structure has a better performance in contrast to OB structure, even to SJ structure when epi depth is not too high.

Table 6-1: Comparisons of V_{br} of different structures

Model	L (μm)	W (μm)	N_d (cm^{-3})	V_{br} (V)
PN Diode	15	5	7×10^{15}	65.81
SJ Diode				260.3
OB Diode				155.1
GOB Diode				289.3
PN Diode	10	4	9.2×10^{15}	54.86
SJ Diode				187.7
OB Diode				125.8
GOB Diode				209.5
PN Diode	7	3	1.27×10^{16}	44.66
SJ Diode				144.3
OB Diode				100.2
GOB Diode				159.1

Note that there is a restriction on the application of GOB devices. For a given width and doping concentration of drift region, SJ devices can be made to satisfy the requirement of different breakdown voltage by changing the epi depth. While in GOB devices, while increasing epi depth, the oxide thickness at the bottom of OB region will be increased correspondingly. GOB devices will not show any advantage on device performance if the OB region takes up a larger area than the p column in SJ devices. Thus it is suggested that the epi depth of GOB devices is no deeper than 15μm. This is also the consideration for the quality of deep Silicon trench etching.

The realization of gradient oxide profile also brings some difficulties into the fabrication process. The fabrication of GOB device is still under investigation.

6.2 Device performance on SiGe-OBUMOS

As is known that higher electron mobility and higher diffusion coefficient lead to higher on state current of MOSFETs. Since Germanium has different material attributes compared to Silicon, such as on mobility and band gap, Silicon Germanium

technology combining the characteristics of Silicon and Germanium will be studied and applied on OB devices.

6.2.1 Simulation on Ge-OBUMOS

In order to understand the feature of Germanium material, Ge-OBUMOS formed on Germanium epi layer instead of Silicon in the entire region is studied at first. The diffusion coefficient and mobility comparisons between Germanium and Silicon are as shown in Table 6-2.

Table 6-2: Diffusion coefficient and mobility of electrons and holes for Silicon and Germanium at T = 300 K [55].

	D_n (cm^2/sec)	D_p (cm^2/sec)	μ_n (cm^2/V-sec)	μ_p (cm^2/V-sec)
Germanium	100	50	3900	1900
Silicon	35	12.5	1350	480

As is known that, an electric field can be present in addition to the carrier gradient as in Equation (6.7) and (6.8).

$$\vec{J}_n = qm_n\vec{e} + qD_n d\vec{n} \tag{6.7}$$

$$\vec{J}_p = qm_p n\vec{e} - qD_p d\vec{p} \tag{6.8}$$

In OBUMOS having n type drift region, on state drain current is decided by $\vec{J}_n$. From Table 6-2, we can see that both the mobility and diffusion coefficient of Germanium are about two times higher than that of Silicon. As a result, Ge-OBUMOS will have an improved on state characteristic compared to Si-OBUMOS theoretically.

While, wide bandgap results in high breakdown electric field, and hence leads to high breakdown voltage. Therefore, because bandgap of Silicon (1.12eV) is wider than that of Germanium (0.635eV), Silicon device has the higher breakdown voltage than Germanium device with the same structure. Simulation was done based upon 200V Si-OBUMOS structure with 3μm n-drift width, doping concentration of 7×10^{15} cm^{-3} and 1.5μm thick oxide of OB structure as in Figure 6-6.

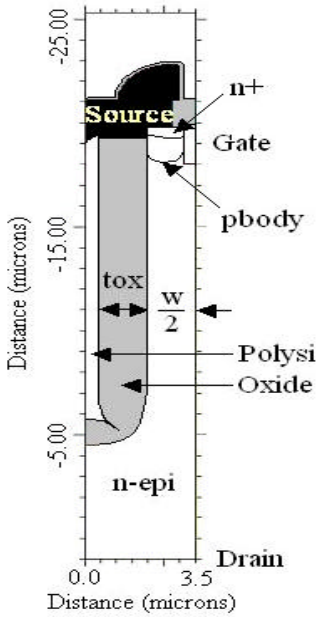

Figure 6-6: Half OBUMOS

(1) On-state Performance

The main difference between Si and Ge is the mobility, which results in different on-state performance.

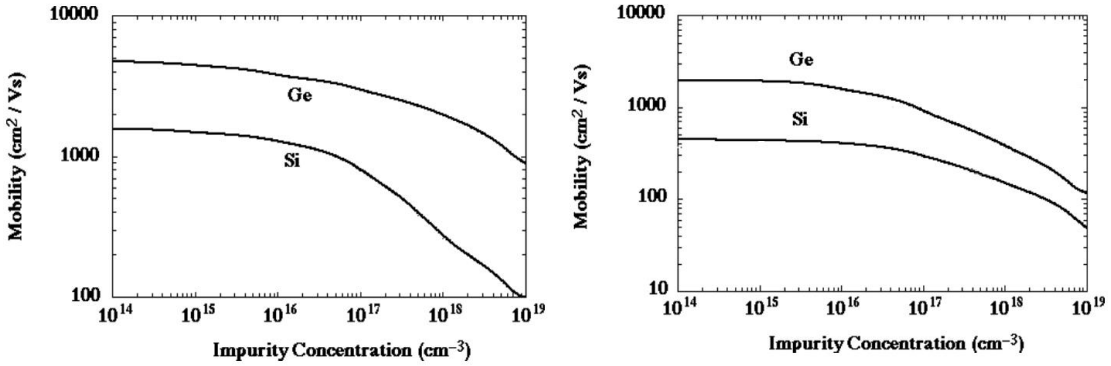

Figure 6-7: Electron mobility (left) and Hole mobility (right) at 300K

The curves on mobility vs. impurity concentration for Si and Ge are shown in Figure 6-7. Since the mobility depends on the doping concentration, the **Concentration Depended Mobility Model** was used in the device simulator MEDICI. By using this

model, the effect of impurity scattering can be included by using mobility values from Tables that depend on the local total impurity concentration, $N_{total}(x, y)$, as:

$$m_{0n} = m_{0n}(N_{total}(x, y)) \tag{6.9}$$

$$m_{0p} = m_{0p}(N_{total}(x, y)) \tag{6.10}$$

For Germanium, approximative mobility versus total impurity concentration for both electrons and holes at 300 K is shown in Table 6-3 (according to Figure 6-7). Using this Table, concentration dependent mobility can be selected with the **CONMOB** parameter on the MODELS statement.

Table 6-3: Mobility versus impurity concentration for both electrons and holes at 300 K

Concentration (cm^{-3})	Mobility in Silicon (cm^2/V-s)	
	Electrons	**Holes**
1×10^{15}	4500	2000
1×10^{16}	4000	1800
1×10^{17}	3500	900
1×10^{18}	3000	400
1×10^{19}	1000	120

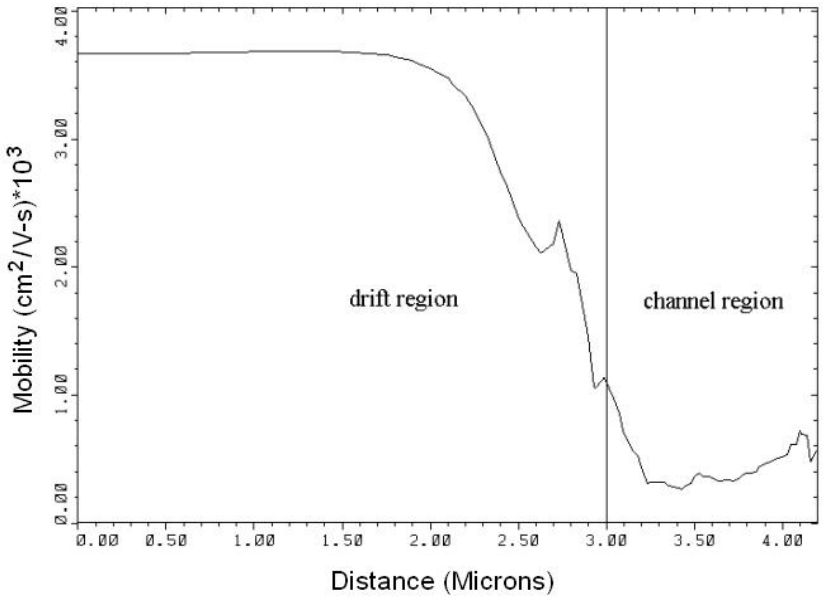

Figure 6-8: Simulated mobility in vertical direction of Ge-OBUMOS along channel region as shown in Figure 6-6.

Figure 6-8 shows the simulation result on mobility in vertical direction of Ge-OBUMOS, by replacing Silicon to Germanium on the entire device. Distance from 3.00µm to 4.20µm represents the channel region of OBUMOS, and the region with distance smaller than 3.00µm is a part of the drift region. It is clear that in the drift region, doping concentration is uniform. Therefore, the mobility in this region is constant. Along with the increase of the doping concentration near the interface of the two regions, mobility is decreased.

In the channel region where doping concentration is much higher than that in drift region, mobility also reaches to the lowest value. In order to get a more accurate result from simulation, the **Enhanced Surface Mobility Model** and a mobility model using the **parallel electric field component** is used in MEDICI simulator.

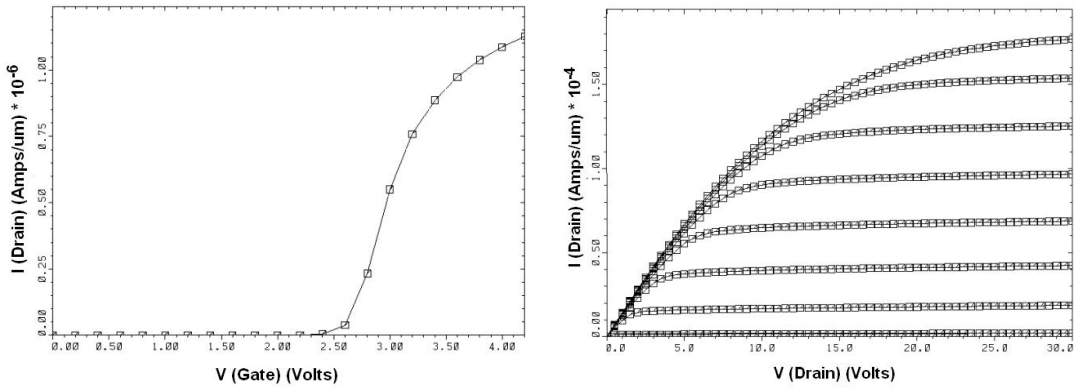

Figure 6-9: Simulated on state IV characters of Si-OBUMOS

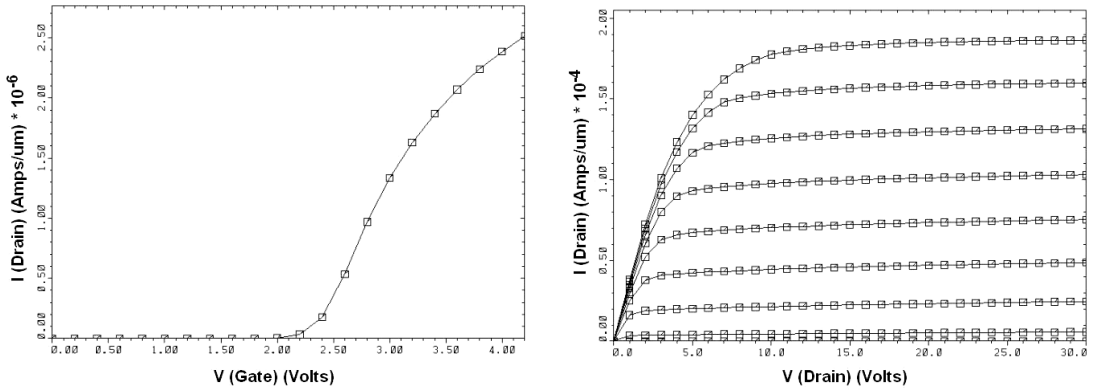

Figure 6-10: Simulated on state IV characters of Ge-OBUMOS

The results compared to Si-OBUMOS are shown as in Figure 6-10. Obviously, in the linear region, Ge-OBUMOS will get a much higher on-state Drain current than Si-OBUMOS.

(2) Off-state Performance

Breakdown voltage is an important parameter for measuring off-state performance of power device. It is mainly affected by energy bandgap, which is mainly decided by material, temperature and doping concentration. In our research on Ge-OBUMOS, n-drift doping concentration is selected to be 7×10^{15} cm^{-3}.

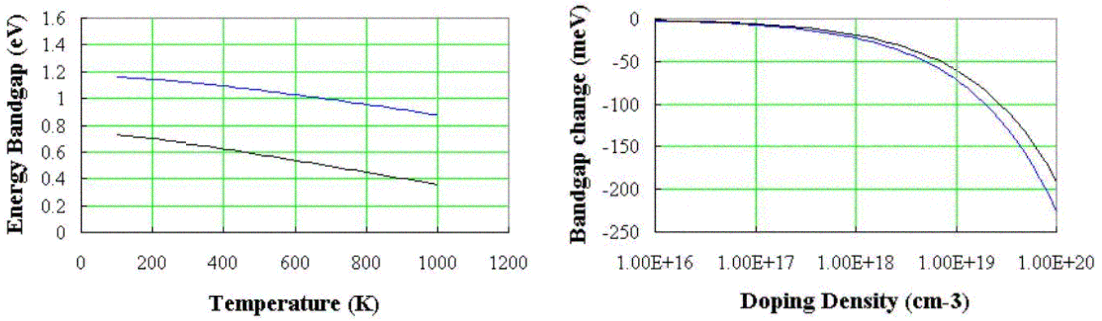

Figure 6-11: Temperature dependence of the energy bandgap of Germanium (top curve), Silicon (bottom curve) and doping dependence of the energy bandgap of Germanium (top curve) and Silicon (bottom curve)

According to Figure 6-11, we can assume that at room temperature, there is no bandgap change in this region. In case of vertical OBUMOS, the drift region contributes more proportion of current. Thus, constant bandgap was used in the whole device for simulation. In addition, at T = 300K, bandgap of Germanium is E_g = 0.66eV (For Silicon case, it is 1.12eV). Compared to Si device, the narrow bandgap of Ge induces impact-ionization at lower applied voltages. The off-state breakdown simulation by using Ge instead of Si in the whole OBUMOS device was performed using MEDICI. As parameters of the OB structure is suitable for Si-OBUMOS only,

readjustment of Oxide thickness is necessary to obtain an optimal Ge-OBUMOS structure.

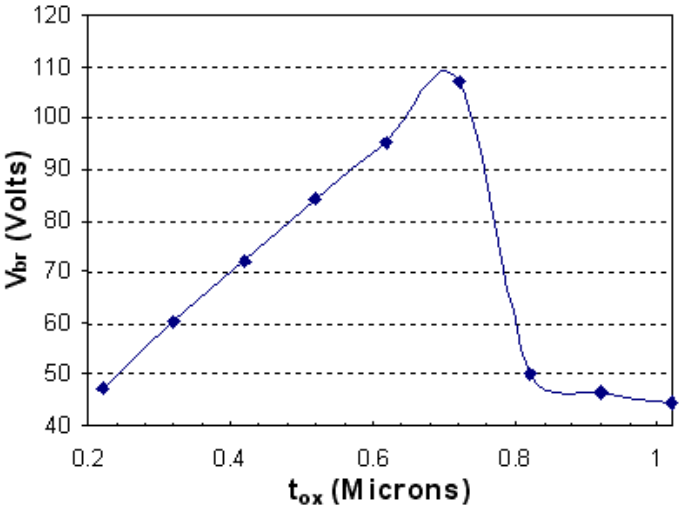

Figure 6-12: Breakdown voltage of Ge-OBUMOS at different t_{ox}

By varing the oxide thickness of OBUMOS, an optimum Ge-OBUMOS can be achieved with oxide thickness equals to 0.72μm as shown in Figure 6-12. When t_{ox} = 0.72μm, V_{br} can reach to about 107V, about half of the breakdown voltage in Silicon case. Therefore, optimum Ge-OBUMOS only has half breakdown voltage compared with Si-OBUMOS.

6.2.2 Efforts on SiGe-OBUMOS

Silicon Germanium (SiGe) heterojunction structure has recently been used instead of pure Silicon in order to have the enhanced mobility. As we know, mobility of Germanium is higher than that of Silicon with the same impurity concentration at the same temperature, but Germanium has a narrow bandgap compared to Silicon, which leads to the undesirable lower breakdown voltage. Bandgap and mobility of SiGe should have the value between that of Silicon and Germanium. Desired device performance is adjusted by setting the proportion of Ge in SiGe. The details are shown in the following.

(a) Energy bandgap of SiGe

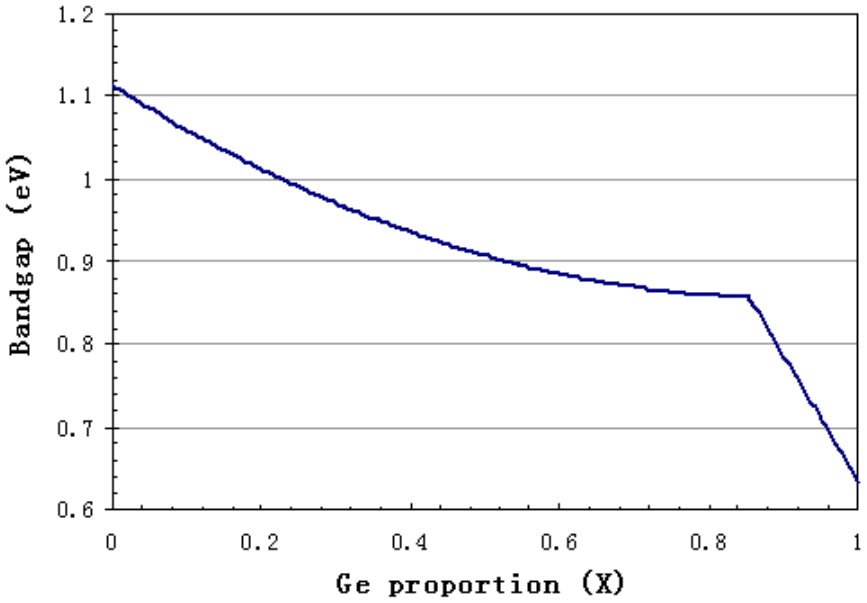

Figure 6-13: Bandgap changes according to the proportion of Ge in SiGe

From Figure 6-13 we can see that, any value of bandgap between that of Si and Ge could be obtained by adjusting the percentage of Germanium in SiGe.

(b) Mobility

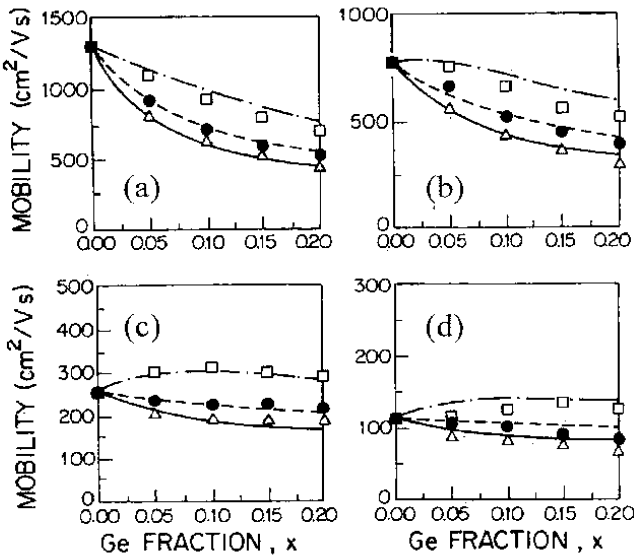

Figure 6-14: Calculated room temperature electron mobility components as a function of SiGe alloy composition for a donor concentration of (a) 10^{15} cm^{-3} (b) 10^{17} cm^{-3} (c) 10^{18} cm^{-3} and (d) 10^{19} cm^{-3}, where hollow triangle, solid circle and hollow square represent for Si, SiGe and Ge, respectively

Since Ge has the higher mobility, with the increase of Germanium proportion, the value of electron mobility is also increased. However, it is found that for compositions ranging from 0% to 30% Ge, **Monte Carlo** simulations and analytical calculations all indicate a gradual decreasing electron mobility with increasing Ge content in SiGe. For strained layers a similar decrease in the in-plane electron mobility in strained SiGe layers compared with Si was also found, while the perpendicular mobility was enhanced. One of these studies also considers the dependence of these trends on doping concentration, from which it was found that the perpendicular drift mobility component for the strained layers was slightly higher than the Si mobility only for doping concentrations in excess of 10^{17} cm^{-3}. At lower doping concentration, both components are reduced in comparison to Si and these findings are summarized in Figure 6-14 [55]. The reduced mobility observed for low doping was attributed to the dominance of alloy scattering, whereas for higher doping, impurity scattering limits mobility and is relatively independent of alloy composition.

(c) Simulation results

SiGe heterojunction layer cannot be too thick with present technology. It is known that for Germanium fraction of x = 0.3, the critical thickness of $Si_{1-x}Ge_x$ on bulk unstrained Si is no more than 0.1μm. Therefore, for vertical semiconductor device, it is difficult to put SiGe heterojunction structure into drift region since the thickness of drift region is more than 10μm. To get a best result in the simulation, 0.1μm was chosen to be the thickness of SiGe heterojunction layer and was introduced into the channel region of OBUMOS. That is to say, the Si p-body of OBUMOS was replaced by Si/SiGe alternant layers with equal thickness of 0.1μm as shown in Figure 6-15.

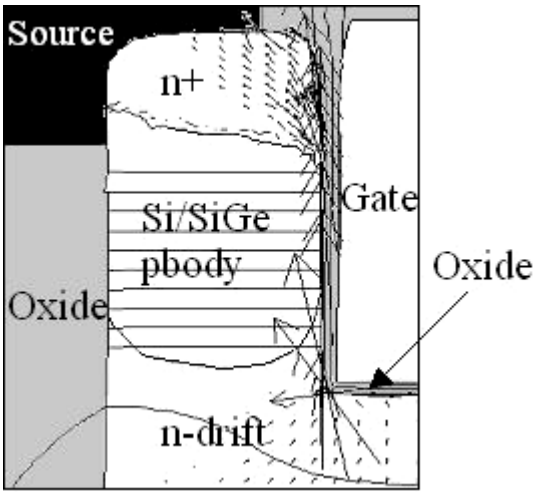

Figure 6-15: OBUMOS with SiGe heterojunction layers in channel region

In device simulation, **Universal Mobility Model** is used for this changed channel region. The Universal Mobility Model is appropriate for the modeling of MOSFET inversion layers. This model is similar in form to the surface mobility model described previously. However, it does not require the channel vertical grid spacing to be greater than the inversion layer width [34].

Simulation result shows that by changing the material in channel region, the on state characteristics of OBUMOS is slightly improved. When select V_{gs} = 7V and V_{ds} = 1V, drain current equals to 1.3502×10^{-5} Amps/μm, while for Silicon OBUMOS, it is 1.3448×10^{-5}Amps/ μm. At the same time, the threshold voltage of SiGe OBUMOS is decreased from 2.4V to 2.0V.

(d) Conclusion

Simulation results prove that SiGe heterojunction structure can be applied to MOSFET to improve the on-state performance, whereas it is unsuitable for OBUMOS because of the following reasons:

i. SiGe heterojunction layer is horizontal and the critical thickness of it is around 0.1μm. For vertical device such as OBUMOS, the on-resistance can only be improved significantly by manipulation of the drift region. For the epi depth of 18μm as in typical OBUMOS structure, it will bring too many difficulties in fabricating SiGe in the drift region.

ii. If applied on channel region of OBUMOS with deep drift region, SiGe heterojunction cannot significantly improve Drain current due to the smaller channel resistance compared to the drift resistance.

iii. It was found from the 2-D device simulation that when the interface between thick oxide and pbody is scraggy, on state performance tended to be worse as in Figure 6-16. This interface roughness is probably due to the different oxidation rate of Si and Ge layers.

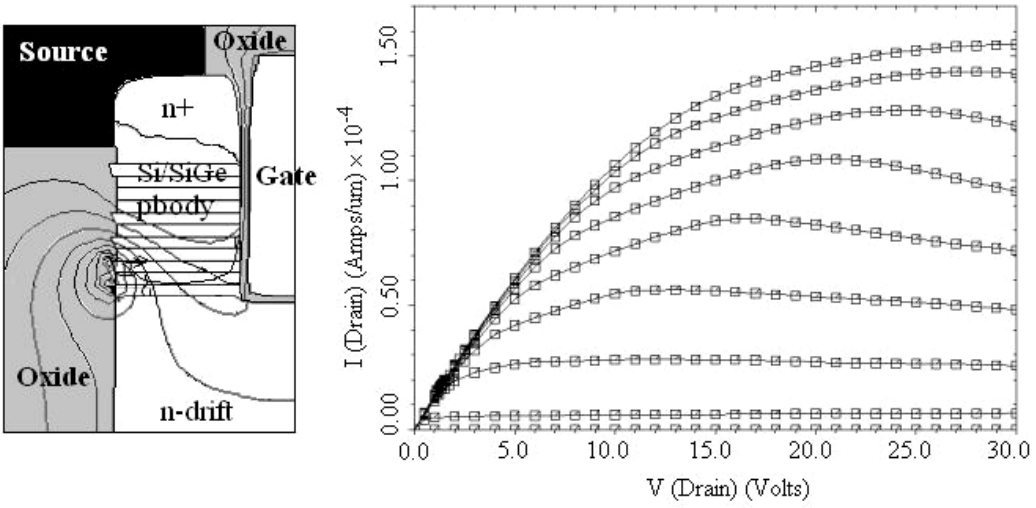

Figure 6-16: Rough interface caused by SiGe heterojunction layers results in the degradation of on-state performance

iv. The formation of thick Oxide requires high temperature and long time process. Because the diffusion coefficient of Germanium is much higher than that of Silicon, when growing the thick oxide, some Germanium will diffuse into the nearby Silicon and adversely affects the heterojunction structure.

Therefore, to obtain the superior performance with usage of SiGe, vertical OBUMOS with shallow drift region is desired. Careful process design is also required due to the sensitivity of the interface profile between Oxide and SiGe.

Furthermore, the lateral device will be a good choice in the future's study on SiGe technology. Actually, due to the features in lateral MOSFETs, SiGe heterojunction structure is easier to be formed. If combined with the advantages of SJ or OB techniques, SiGe technology can be successfully applied on Power devices.

6.3 120V SJ-LDMOS on Partial SOI

Thermal dissipation is the main issue for the operation of SJ MOSFETs on SOI wafers. Recently, IME (Singapore) has found a way, namely partial SOI (PSOI) technology [31], to overcome the inherent problems existing in SOI MOSFETs. Unlike conventional SOI LDMOS, the thick Oxide layer does not cover the entire active region. There is no Oxide right below the p well region. By using PSOI technology, the thermal dissipation problem for RF applications is overcome while maintaining the advantages of conventional SOI LDMOS structures.

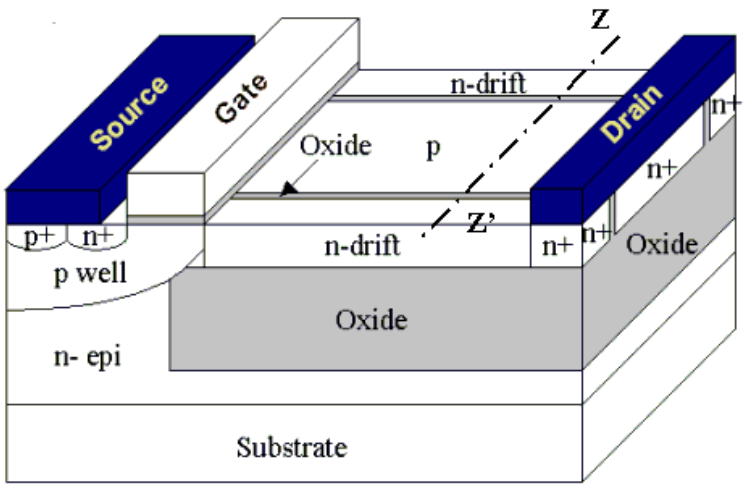

Figure 6-17: Proposed Partial SOI SJ-LDMOS device structure

Combining the advantages of PSOI technology in IME and SJ structure into conventional LDMOS, a novel power device called PSOI SJ-LDMOS can be designed in the future, as shown in Figure 6-17. Similar to the PFVDMOS as mentioned in Chapter 2, the LDD region of LDMOS in this device is replaced by SJ structure with thin Oxide layer in between, to avoid the inter-diffusion problem. Because both of the partial SOI and SJ structures are formed based on Si trench etching technology, there is no additional mask required for adding the SJ structure on PSOI LDMOS compared to PFLDMOS.

6.3.1 Partial SOI SJ structure formation

This PSOI SJ structure is made by two steps of Si trench etching, together with oxidation and some auxiliary processing steps, as shown in Table 6-4 and Figure 6-18.

Table 6-4: Process flow for PSOI SJ structure formation

Step	Process flow	Step	Process flow
1	Blank n+ implant	11	Piranah Clean
2	LPCVD TEOS 5000 Å	12	P-SOI Growth
3	Nitride Deposition 1500 Å	13	Nitride & Oxide Removal
4	LPCVD LISA 4000 Å	14	Sidewall Oxide Growth 300 Å
5	SOI Mask	15	Poly-Si Deposition
6	Oxide/Nitride/Oxide Etch	16	Boron Poly-Si Implant
7	Si Trench Etch 1.9µm & Resist strip	17	LPCVD Oxide
8	Dry Oxidation 85 Å	18	p-Poly Drive in
9	Nitride Deposition 480 Å	19	Oxide Etch
10	Deep Silicon Trench Etch 4.2µm	20	Poly-Si Etch

Thick Oxide in Partial SOI devices is formed on the multiple Silicon trenches on bulk Silicon and is based on principle of Silicon consumption during oxidation. After the thick Oxide growth for PSOI structure, SJ structure with thin Oxide layer can be formed. It includes thin Oxide growth, PolySi deposition, doping and drive-in and PolySi etchback, etc. This process is difficult to control to guarantee the Oxide occupies the entire Si trenches, because the pinch-off of neighboring oxide layers must

occur at the time when all the Silicon columns between trenches are consumed completely. It is required that the Silicon trench width and oxidation processing must be carefully designed. Also, oxide shape is not rectangular as seen in Figure 6-18. However, this shape has no adverse effect on device performance.

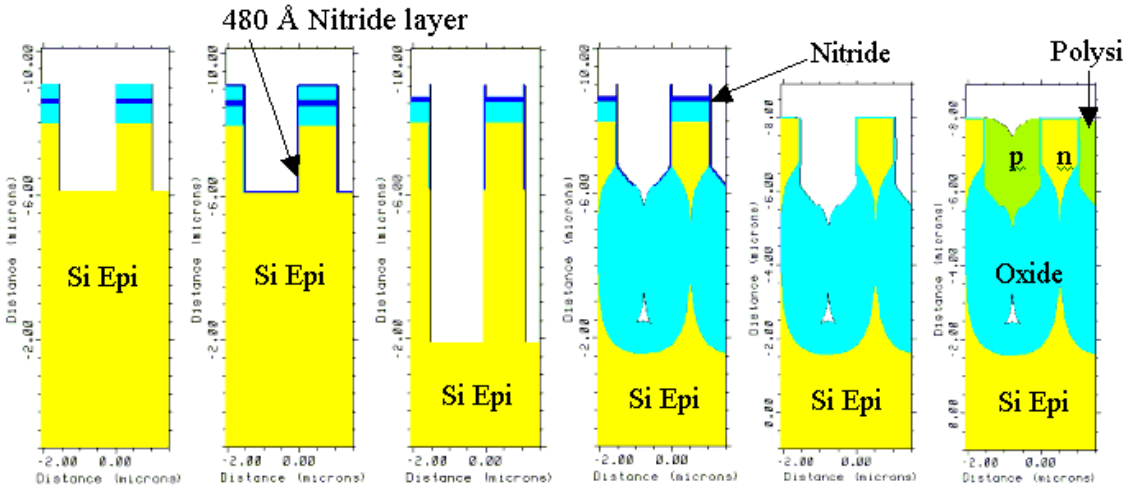

Figure 6-18: Cross section view of PSOI SJ structure formation

6.3.2 Parameter determinations for SJ structure on drift region

The column width of SJ structure should be decided by the trench width of PSOI region. It is known that for growth of 1μm Oxide, a layer of Silicon with a thickness of 0.44μm is consumed. In addition, the thickness of the Nitride mask used on the deep Si trench etching also affects the width of Si trench. Thus, in consideration of the factors above, SJ structures with dimension variations are proposed for future fabrications, as in Table 6-5.

Table 6-5: Parameters of SJ structure for three proposed dimensions

W_n (μm)	W_p (μm)	N_n (cm^{-3})	N_p (cm^{-3})	$L_n = L_p$ (μm)	V_{br} (V)
0.5	0.876	9.8×10^{16}	5.6×10^{16}	5	117.8
0.8	1.256	5.67×10^{16}	3.61×10^{16}	5	116.9
1.04	1.56	4.17×10^{16}	2.78×10^{16}	5	109.5

As indicated in SJ theory, for a certain dimension of SJ structure, there must be an optimized doping concentration calculated from Equation (2.15), which leads to the maximum V_{br}. In the mean while, charge compensation of $W_n \cdot N_n = W_p \cdot N_p$ must be satisfied. As shown in Table 6-4, the column length of 5μm is decided by simulation for SJ structures on 120V application.

Note that, when W_n is 1.04μm, desired doping concentrations in n and p columns are $4.17\times 10^{16}cm^{-3}$ and $2.78\times 10^{16}cm^{-3}$, respectively. Process simulation using TSUPREM-4 indicates that, simulated doping of SJ structure varies no more than ± 6%. It is within the range allowed taking into consideration the charge imbalance effect for SJ devices. However, due to Boron segragation at Oxide/PolySi interface, Boron doping concentration in Polysilicon region near the notch can be 25% higher. This should be given adequate attention in the future research on PSOI SJ-LDMOS fabrication to prevent early breakdown.

Chapter 7

Conclusions

The trade-off relationship between blocking voltage and on-state resistance is the main issue on the development of power MOSFETs. In the past power MOSFETs development, the UMOSFET, with gate structure completely buried in the trench and self-aligned process, became a promising structure with the reduction of process steps and the specific on-resistance compared to the DMOSFET structure. Currently, because of the low blocking capability, the UMOSFET structure shows its advantages only in the low voltage range below 50V. The applications of conventional MOSFETs are still restricted by the ideal silicon limit of $R_{on,sp} \propto V_{br}^{2.5}$. Consequently, to further enhance the breakdown voltage without compromising $R_{on,sp}$ is the primary objective in power switches industry.

The basic concept of superjunction structure is illustrated in Chapter 2. With p columns neighboring to the n-drift region, the drift region is depleted laterally as well as vertically at reverse bias. It has been theoretically and experimentally demonstrated that, superjunction devices have a much higher blocking voltage, especially when operating for high voltage rating. Though high conduction losses are presented in SJ structure drift region because the half conduction area is taken up by non-conducting p column, the overall performance of SJ structure is better than that of conventional MOSFETs due to the high blocking capability. With the application of superjunction theory to the drift region of power MOSFETs, the breaking of ideal silicon limit becomes possible. However, the realization of SJ structure is restricted by complicated process steps, the problem of inter-diffusion and consequential charge

imbalance. This project is to find out a simple and efficient alternative technology in the fabrication of SJ MOSFETs.

PFVDMOS technology as in Chapter 2 was firstly developed to solve the inter-diffusion problem. With a 500 Å Oxide layer in between as a diffusion barrier, the interaction between positive and negative charges in SJ p/n column interface is alleviated. It has been proven that, this thin Oxide layer has no influence on either on-state or off-state performance of SJ structures. The process to implement the SJ structure by using PFVDMOS technology was carried out as Silicon trench etching, dry Oxidation, conformal PolySi deposition, Boron tilted implantation, PolySi refill, PolySi drive-in, etc., in sequence. Proposed PFVDMOS structure is formed on the epitaxy layer with doping concentration of 7×10^{15} cm^{-3} and 20 μm in thickness. The SJ p/n column width is 5 μm. Simulated $R_{on,sp}$ of PFVDMOS with V_{br} = 240V is 2.9 mΩ-cm^2, while measured $R_{on,sp}$ of PFVDMOS is 3.68 mΩ-cm^2 with V_{br} = 187V. Due to charge imbalance and edge termination problems, the measurement result of PFVDMOS is 22% lower than the simulated result of 240V. In any case, both of the results show the superior performance in comparison with conventional MOSFETs. A better performance can be expected by carefully tuning the process parameters.

The contribution of PFVDMOS technology is to solve the inter-diffusion problem, but it provides no solution on high sensitivity to the net charge imbalance problem, which hinders the function of SJ devices. Hereby, the presence of OB MOSFETs with the absence of charge imbalance effect, as shown in Chapter 3, becomes more attractive compared to SJ devices. In OB MOSFETs, the p column of SJ structure is replaced by a thick oxide layer together with a highly doped PolySi layer beside. The OB structure helps to deplete the n-drift region and therefore enhances the breakdown

voltage. There is no charge balance requirement in realizing OB devices. To guarantee the best performance, the Oxide thickness, mesa width of drift region and doping concentration for optimal OB-MOSFETs should follow the relationship of $N_d = 2.90 \times 10^{11} \cdot [t_{ox} \cdot \frac{W}{2}]^{-4/7}$. For a given doping concentration of 7×10^{15} cm^{-3} and epi thickness of 20μm on optimized OBUMOS, simulated breakdown voltage is 210V, which is more than 3 times that of conventional UMOSFET, and measured OB Diode is 184V, which is 2.5 times that of conventional UMOSFET, respectively. Simulated specific on-resistance for OBUMOS with the parameters above-mentioned is 0.0024Ω-cm^2. With the same $R_{on,sp}$, calculated breakdown voltage of ideal silicon limit [32] is 175V. Therefore, the $R_{on,sp}$~V_{br} point of OBUMOS is lower than the ideal Silicon limit.

Continuous efforts were carried on to improve the performance of Oxide Bypassed structure. It was discovered that, in OB MOSFETs, if the sidewall PolySi region contact is separated from the Source Electrode and applied an external voltage, the improvement of blocking voltage, on-state resistance and even transconductance will be achieved. The OB device with this additional Electrode, hereby called Control Electrode, is named as Tunable OB (TOB) device. At off state, the Control voltage provides an additional electric field, which functions to counteract partial Drain-Source electric field. This results in an enhanced breakdown voltage. However, the Control voltage also increases the electric field near the p-body-n-drift junction. A premature breakdown potentially happens at the top region of TOB MOSFETs when the Control voltage is higher than a certain value. Therefore, there exists an optimum Control bias for TOB devices to achieve the maximum breakdown voltage. When the TOB device operates at on state, an accumulation layer along the thick Oxide and n-

drift interface is generated under positive Control voltage. The reduction of on-resistance is found due to the enlarged conduction area through the accumulation layer in this case. Hence, the $R_{on,sp}$~V_{br} point of TOBUMOS can be tuned further away from the ideal Silicon limit as shown in Chapter 3. In the same way, to achieve the specific on-resistance of 0.0024Ω-cm^2 as mentioned for 200V OBUMOS, TOBUMOS has the breakdown voltage of about 250V, which is 20% higher than that of OBUMOS at the same dimensions.

100V TOBUMOS was designed to meet the requirements of current power industry. Theoretically, formed on 8.5μm dual epi layer with resistivity of 0.7Ω-cm, simulated minimum $R_{on,sp}$ of TOBUMOS is 6.04×10^{-4} Ω-cm^2 at 17V Control voltage, while the breakdown voltage is 113V. The $R_{on,sp}$~V_{br} relationship of TOBUMOS is better than the ideal Silicon limit and the optimal 100V OBUMOS formed on 0.55Ω-cm epi layer as well. The MOSFETs and Diodes with conventional, OB and TOB structures were fabricated on the same wafer to verify the theoretical TOB concept. The detailed process description of TOBUMOS is given in Chapter 4.

TOB Diode was first successfully fabricated with tunable effect on breakdown voltage. Though measured breakdown voltage of TOB Diode on 0.55Ω-cm epi without Control bias is 83V, which is lower than simulated value of 100V. The maximal V_{br} can be tuned up to 103V at 20V Control bias. Thus, tunable effect at off state was fully verified. Fabricated TOBUMOS with W = 3.5μm represents the $R_{on,sp}$ of 0.674 mΩ-cm^2 at the maximum V_{br} of 79V under 5V Control voltage. According to the ideal SJ limit line, at the same $R_{on,sp}$, the V_{br} is 71V, which is 10% lower than that of fabricated TOBUMOS. Thus, TOBUMOS has successfully broken the ideal SJ limit line at the medium voltage range.

As is known that the OB device can be fabricated with relatively simple method but it sacrifices certain amount of breakdown voltage compared to SJ devices, especially in high voltage rating. By comparing the equal potential lines at breakdown, it is clear that the electric field in OB devices is not as uniform as in SJ devices. One way to rectify the electric field distribution is to apply a gradient Oxide Bypassed (GOB) sidewall as shown in Chapter 6. Theoretically, by adjusting the slope of GOB structure, GOB devices might have a superior performance to both OB and SJ devices. Because of the difficulties of realizing an ideal slope of Oxide profile as expected, the research of realizing the novel GOB structure is undergoing.

In addition, SJ structure and OB structure applied on LDMOS are promising for VLSI integration. Using SiGe heterojunction structure instead of pure Silicon, a good on-state performance is achievable. Having the advantage of SOI LDMOS, Partial SOI technology makes it available for LDMOS fabricated on economic bulk Silicon wafer.

In conclusion, by combining some new technologies in SJ and OB device fabrication, the advantages of both of these devices will be fully exhibited and exploited in many applications.

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APPENDIX A

LIST OF PUBLICATIONS

1. Yung C. Liang, Xin Yang, Ganesh S. Samudra, K.P. Gan and Yong Liu, "Tunable Oxide-Bypassed VDMOS (OBVDMOS): Breaking the Silicon Limit for the Second Generation", *Proceedings of International Symposium on Power Semiconductor Devices and ICs*, 2002, pp. 201-204.

2. Kian Paau Gan, Xin Yang, Yung C. Liang, Ganesh S. Samudra and Liu Yong, "A Simple Technology for Superjunction Device Fabrication: Polyflanked VDMOSFET", *IEEE Electron Device Letters*, Vol. 23, No. 10, October 2002, pp. 627-629.

3. Xin Yang, Yung C. Liang, Ganesh S. Samudra and Yong Liu, "Tunable Oxide-Bypassed Trench Gate MOSFET: Breaking the Ideal Superjunction MOSFET Performance Line at Equal Column Width", *IEEE Electron Device Letters*, Vol. 24, No. 11, Nov. 2003, pp. 704-706.

APPENDIX B

SIMULATION FILES

B.1 TOBUMOS TSUPREM-4 simulation program file

```
$  TSUPREM4 – TOBUMOS Process Simulation

$ Specify x & y mesh
LINE  X    LOCATION=1.5 SPACING=0.2
LINE  X    LOCATION=3.0 SPACING=0.2
LINE  X    LOCATION=3.9 SPACING=0.15
LINE  X    LOCATION=4.5 SPACING=0.2

LINE  Y    LOCATION=1   SPACING=1.0
LINE  Y    LOCATION=2   SPACING=1.0

$ Initialize the structure
INITIALIZE       AS=0.003          RESIST

$ Deposit 8.5+1.5 um n epitaxy
DEPOSIT          SI        THICK=1.5       SPAC=5          PHOS=0.02       RESIST
DEPOSIT          SI        THICK=1         SPAC=20         PHOS=0.7        RESIST
DEPOSIT          SI        THICK=1         SPAC=10         PHOS=0.7        RESIST
DEPOSIT          SI        THICK=3.5       SPAC=14         PHOS=0.7        RESIST
DEPOSIT          SI        THICK=3         SPAC=90         PHOS=0.7        RESIST

$ Plot intial mesh
PLOT.2D    GRID  SCALE   C.GRID=2

$ Deposit SRO & nitride as hard mask
DEPOSIT          OXIDE  THICK=0.06    SPAC=2
DEPOSIT          NITRIDE  THICK=0.25    SPAC=2

$ Poly trench mask and trench etching
ETCH       NITRIDE         P1.X=2.2          LEFT
ETCH       OXIDE           P1.X=2.2          LEFT
ETCH       SILICON         THICK=10

METHOD   VISCOELA  PD.TRANS  DY.OXI=0.1

$ Dry oxidation (100Å)
DIFFUSE    TIME=23 TEMP=900  DRYO2

$ 0.5 um wet oxide growth
DIFFUSE    TIME=50 TEMP=1050   STEAM

$ Poly refill & etch-back
DEPOSIT          POLY    THICK=1           SPAC=2
ETCH             POLY    THICK=1.5

$ Remove SRO and Nitride
ETCH       NITRIDE         ALL
```

```
ETCH    OXIDE              THICK=0.1

METHOD   COMPRESS  PD.TRANS

$ Grow 200A screen oxide
DIFFUSE    TIME=30 TEMP=950  DRYO2

$ p-body implant
IMPLANT    BORON  DOSE=2E13  ENERGY=90

$ p-body drive-in
DIFFUSE    TIME=100 TEMP=1125

$ N+ Source mask- Resist Deposit, and pattern
DEPOSIT    PHOTORESIST THICK=1.2  SPACES=2

ETCH      PHOTORESIST START X=3.0 Y=-50
ETCH      CONTINUE              X=3.0 Y=-3.0
ETCH      CONTINUE              X=4.5 Y=-3.0
ETCH      DONE                  X=4.5 Y=-50

$Source N+ implant
IMPLANT    AS  DOSE=5E15  ENERGY=120

ETCH PHOTORESIST ALL

$ Source P+ mask- Resist Deposit, and pattern
DEPOSIT    PHOTORESIST THICK=1.2  SPACES=2

ETCH      PHOTORESIST START X=0 Y=-50
ETCH      CONTINUE              X=0 Y=-3.0
ETCH      CONTINUE              X=3.0 Y=-3.0
ETCH      DONE                  X=3.0 Y=-50

$ SourceP+ implant
IMPLANT    BF2  DOSE=3E15  ENERGY=80

ETCH PHOTORESIST ALL

$ Trench gate mask and trench gate etch
ETCH      OXIDE          START  X=3.9 Y=-50
ETCH      CONTINUE              X=3.9 Y=-7.0
ETCH      CONTINUE              X=4.5 Y=-7.0
ETCH      DONE                  X=4.5 Y=-50

ETCH      SILICON         START X=3.9 Y=-50
ETCH      CONTINUE              X=3.9 Y=-7.0
ETCH      CONTINUE              X=4.5 Y=-7.0
ETCH      DONE                  X=4.5 Y=-50

METHOD   COMPRES  PD.TRANS

$ 567 A sacrificial oxide
DIFFUSE    TIME=60 TEMP=1000  DRYO2

$ Remove sacrificial oxide
ETCH      OXIDE          THICK=0.1
ETCH      OXIDE          START  X=3.5 Y=-50
ETCH      CONTINUE              X=3.5 Y=-6
ETCH      CONTINUE              X=4.5 Y=-6
```

```
ETCH      DONE                    X=4.5 Y=-50

$ 429A gate oxidation
DIFFUSE   TIME=40 TEMP=1000  DRYO2

$ Gate poly deposit and etch-back
DEPOSIT   POLY THICK=1.0  SPACES=1

ETCH      POLY          P1.X=3  LEFT
ETCH      POLY          START  X=0 Y=-50
ETCH      CONTINUE              X=0 Y=-8.9
ETCH      CONTINUE              X=4.5 Y=-8.9
ETCH      DONE                  X=4.5 Y=-50

$ 1000 Å poly reox
DIFFUSE   TIME=10 TEMP=900  DRYO2
DIFFUSE   TIME=30 TEMP=900  WET
DIFFUSE   TIME=10 TEMP=900  DRYO2

$ BPSG and contact holes
DEPOSIT         OXIDE           THICK=1
ETCH            OXIDE           LEFT    P1.X=1.85
ETCH            OXIDE           START  X=2.0   Y=-50
ETCH            CONTINUE                X=2.0    Y=-8.5
ETCH            CONTINUE                X=3.0    Y=-8.5
ETCH            DONE                    X=3.0    Y=-50

$ BPSG Reflow
DIFFUSE   TIME=30 TEMP=900

$ Metallization
DEPOSIT         ALUMINUM    THICK=1.7
ETCH            ALUMINUM    START  X=2.0 Y=-50
ETCH            CONTINUE                X=2.0 Y=-8.5
ETCH            CONTINUE                X=2.5 Y=-8.5
ETCH            DONE                    X=2.5 Y=-50

$ Passivation
DEPOSIT         OXIDE           THICK=0.1       SPAC=1

$ Define Electrodes
ELECTROD  NAME=ELE1         X=1.5
ELECTROD  NAME=Source       X=3
ELECTROD  NAME=Gate         X=4.5
ELECTROD  NAME=Drain        BOT

SAVEFILE   OUT.FILE=TOBUMOS.spu4  MEDICI ELEC.BOT POLY.ELE

STOP
```

B.2 TOBUMOS MEDICI simulation program files

(a) Off-state simulation

```
$  MEDICI device simulation for TOBUMOS off-state
$  Specified a rectangular mesh
MESH IN.FILE=TOBUMOS.spu4  TSUPREM4 PROFILE

PLOT.2D SCALE GRID BOUND  TITLE="Initial Grid"

$ Model statement
MODELS    IMPACT.I CONMOB    FLDMOB  CONSRH  AUGER  BGN SRFMOB2

$ Symbolic and method statement
SYMB              CARR=0
METHOD            ICCG  DAMPED

$ Initial solution, ELE1 represents for the additional Control Electrode
SOLVE             V(Source)=0.0              V(Drain)=0.0      V(ELE1)=0.0
SOLVE             ELECTROD=ELE1         V(ELE1)=0.0      VSTEP=4          NSTEP=4

$  Obtain solution by 2-carrier Newton with continuation
SYMB      CARR=2 NEWTON

$  Breakdown test with drain current of 1E-9 /um
SOLVE ELECTROD=Drain V(Drain)=0      VSTEP=0.1 NSTEP=2
SOLVE ELECTROD=Drain V(Drain)=0.5   VSTEP=0.5 NSTEP=2
SOLVE ELECTROD=Drain V(Drain)=1      VSTEP=5   NSTEP=2
SOLVE ELECTROD=Drain V(Drain)=10    VSTEP=10  NSTEP=4

$  Continue solving
SOLVE ELEC=Drain CONTINU C.VSTEP=0.001 C.VMAX=800 C.IMAX=1E-9 C.TOL=0.1

$  Breakdown curve plot
PLOT.1D           X.AX=V(Drain) Y.AX=I(Drain) POINTS ^ORDER  TOP=1E-9
+ LEFT=0 RIGHT=400

$  Full Flowlines, V and impact ionisation for last solution
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at Breakdown"
CONTOUR POTENTIA DEL.V=10 COLOR=2
CONTOUR FLOWLINE COLOR=1
CONTOUR II.GEN   COLOR=4

$  Plot E vector
PLOT.2D BOUND  JUNC  DEPL  FILL  SCALE   TITLE="E-vector"
VECTOR E.FIELD COLOR=1

$  Plot hole distribution in the region
PLOT.2D  BOUND  DEPL JUNC SCALE  TITLE="Holes Distribution Contour"
CONTOUR    HOLE LOG FILL

$  Plot electron distribution
PLOT.2D  DEPL BOUND  JUNC  SCALE  TITLE="Electrons Distribution Contour"
CONTOUR    ELECTRON LOG FILL MIN=1.0 DEL=1.0
```

(b) On-state simulation

```
$  MEDICI device simulation for TOBUMOS on-state
MESH   IN.FILE=TOBUMOS.spu4 TSUPREM4 PROFILE

$ Model Statement
MODELS         CONMOB FLDMOB CONSRH AUGER BGN SRFMOB2 SYMB CARR=0
METHOD         ICCG    DAMPED

$ Initial solution, ELE1 represents for the additional Control Electrode
SOLVE V(Gate)=0.0              V(Drain)=0.0     V(Source)=0.0
SOLVE ELECTROD=ELE1        V(ELE1)=0.0     VSTEP=4         NSTEP=4
SYMB   CARR=1                  NEWTON         ELECTRON

$ Gate characteristics simulation
LOG      OUT.FILE=OBUMOSVthdat
SOLVE  V(Drain)=0.1
SOLVE  V(Gate)=0.2       ELEC=Gate       VSTEP=0.2       NSTEP=20
PLOT.1D                  Y.AX=I(Drain)   X.AX=V(Gate)   POINTS          COLOR=2


$ Bias up the gate
SOLVE ELEC=Gate       V(Gate)=2.0       VSTEP=1         NSTEP=9
+          OUT.FILE=OBUMOSSOL02       SAVE.BIA

$ Drain characteristics simulation at Vg=10V
LOAD   IN.FILE=OBUMOSSOL10
LOG      OUT.FILE=OBUMOSD10
SOLVE ELECTROD=Drain         V(Drain)=0         VSTEP=1         NSTEP=30

$ Cutting at Z=1.0
PLOT.2D          BOUNDJUNC    DEPL    FILL     SCALE
+                TITLE="Struct at On-State (Vgs=10V, Vds=30V)"
VECTOR           J.TOTAL          COLOR=1
CONTOUR          POTENTIA         DEL.V=3          COLOR=2
CONTOUR          FLOWLINE COLOR=1
CONTOUR          II.GEN   COLOR=1

$ Drain characteristics simulation at other gate voltages
LOOP   STEPS=8
          ASSIGN           NAME=SFX       C.VAL=09         DEL=-1
          LOAD   IN.FILE="OBUMOSSOL"@SFX
          LOG      OUT.FILE="OBUMOSD"@SFX
          SOLVE ELECTROD=Drain         V(Drain)=0         VSTEP=1         NSTEP=30
L.END

$ Drain curve
PLOT.1D          IN.F=OBUMOSD10 X.AX=V(Drain) Y.AX=I(Drain) POIN   TITLE="Drain curve"
LOOP   STEPS=8
          ASSIGN           NAME=SFX       C.VAL=09         DEL=-1
          PLOT.1D IN.F="OBUMOSD"@SFX  X.AX=V(Drain) Y.AX=I(Drain) POIN   UNCH
L.END
```

B.3 MEDICI input file for superjunction concept analysis

```
$ MEDICI device simulation for ideal SJ Structure at Off-State
$ w: p/n column width; Ly: p/n column length; Nd: doping concentration at p/n column
ASSIGN          NAME=w          C.VAL=5
ASSIGN          NAME=Ly         C.VAL=15
ASSIGN          NAME=Nd         C.VAL=7E15

$ Specify initial mesh

MESH

X.MESH          LOCATION=-@w            SPACING=@w/10
X.MESH          LOCATION=-0.6*@w        SPACING=0.05*@w
X.MESH          LOCATION=-0.4*@w        SPACING=0.05*@w
X.MESH          LOCATION=0              SPACING=@w/10
X.MESH          LOCATION=0.4*@w         SPACING=0.05*@w
X.MESH          LOCATION=0.6*@w         SPACING=0.05*@w
X.MESH          LOCATION=@w             SPACING=@w/10

Y.MESH          LOCATION=-(@Ly+2)   SPACING=0.5
Y.MESH          LOCATION=-(@Ly+1)   SPACING=0.5
Y.MESH          LOCATION=-(@Ly+0.3) SPACING=0.1
Y.MESH          LOCATION=-(@Ly-0.3) SPACING=0.1
Y.MESH          LOCATION=-(@Ly-1)   SPACING=0.5
Y.MESH          LOCATION=-1         SPACING=0.5
Y.MESH          LOCATION=-0.3       SPACING=0.1
Y.MESH          LOCATION=0.3        SPACING=0.1
Y.MESH          LOCATION=1          SPACING=0.5
Y.MESH          LOCATION=2          SPACING=0.5


ELIMINATE COLUMNS X.MIN=-0.6*@w  X.MAX=-0.5*@w Y.MIN=-(@Ly+2) Y.MAX=-@Ly
ELIMINATE COLUMNS X.MIN=-0.5*@w  X.MAX=-0.4*@w Y.MIN=-(@Ly+2) Y.MAX=-@Ly
ELIMINATE COLUMNS X.MIN=0.4*@w   X.MAX=0.5*@w   Y.MIN=-(@Ly+2) Y.MAX=-@Ly
ELIMINATE COLUMNS X.MIN=0.5*@w   X.MAX=0.6*@w   Y.MIN=-(@Ly+2) Y.MAX=-@Ly

ELIMINATE COLUMNS X.MIN=-0.6*@w  X.MAX=-0.5*@w       Y.MIN=0        Y.MAX=2
ELIMINATE COLUMNS X.MIN=-0.5*@w  X.MAX=-0.4*@w       Y.MIN=0        Y.MAX=2
ELIMINATE COLUMNS X.MIN=0.4*@w   X.MAX=0.5*@w        Y.MIN=0        Y.MAX=2
ELIMINATE COLUMNS X.MIN=0.5*@w   X.MAX=0.6*@w        Y.MIN=0        Y.MAX=2

REGION          SILICON

ELECTROD  NAME=Source       X.MIN=-@w X.MAX=@w Y.MIN=-(@Ly+2) Y.MAX=-(@Ly+1)
ELECTROD  NAME=Drain        X.MIN=-@w X.MAX=@w Y.MIN=1          Y.MAX=2


PROFILE         N-TYPEN.PEAK=1E20   UNIF    X.MIN=-@w       X.MAX=@w
+       Y.MIN=0         Y.MAX=1
PROFILE         P-TYPE N.PEAK=1E17  UNIF    X.MIN=-@w       X.MAX=@w
+       Y.MIN=-(@Ly+1)          Y.MAX=-@Ly
PROFILE         P-TYPE N.PEAK=@Nd   UNIF    X.MIN=-@w       X.MAX=-0.5*@w
+       Y.MIN=-@Ly              Y.MAX=0
PROFILE         N-TYPEN.PEAK=@Nd    UNIF    X.MIN=-0.5*@w X.MAX=0.5*@w
+       Y.MIN=-@Ly              Y.MAX=0
PROFILE         P-TYPE N.PEAK=@Nd   UNIF    X.MIN=0.5*@w  X.MAX=@w
+       Y.MIN=-@Ly              Y.MAX=0
```

```
$ Plot structure
PLOT.2D   GRID  TITLE="Initial Grid"  FILL  SCALE
PLOT.2D  SCALE BOUND  FILL  TITLE="Impurity Contour"
CONTOUR DOPING LOG MIN=14 MAX=22 DEL=0.1 COLOR=2
CONTOUR DOPING LOG MIN=-22 MAX=-14 DEL=0.1 COLOR=1

$  Plot impurity profile
PLOT.1D          DOPING          X.START=5  X.END=5  Y.START=-17  Y.END=2
+          Y.LOG  POINT  BOT=1E14          TOP=1E22
+          COLOR=2          TITLE=" doping profile"

$ Model statement
MODELS    IMPACT.I CONMOB    FLDMOB  CONSRH  AUGER  BGN SRFMOB2

$ Symbolic and method statement
SYMB      CARR=0
METHOD    ICCG  DAMPED

$ Initial solution
SOLVE     V(Source)=0.0  V(Drain)=0.0

$  Plot structure at 0V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 0V"
CONTOUR POTENTIA DEL.V=5 COLOR=2

$  Obtain solution by 2-carrier Newton with continuation
SYMB      CARR=2  NEWTON

$  Breakdown test with drain current of 1E-9 /um
SOLVE ELECTROD=Drain V(Drain)=0 VSTEP=0.1 NSTEP=2
SOLVE ELECTROD=Drain V(Drain)=0.5 VSTEP=0.5 NSTEP=2
SOLVE ELECTROD=Drain V(Drain)=1 VSTEP=1   NSTEP=9

$  Plot structure at 10V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 10V"
CONTOUR POTENTIA DEL.V=5 COLOR=2

SOLVE ELECTROD=Drain V(Drain)=10    VSTEP=10  NSTEP=4

$  Plot structure at 50V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 50V"
CONTOUR POTENTIA DEL.V=5 COLOR=2

SOLVE ELECTROD=Drain V(Drain)=50    VSTEP=10  NSTEP=5

$  Plot structure at 100V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 100V"
CONTOUR POTENTIA DEL.V=5 COLOR=2

SOLVE ELECTROD=Drain V(Drain)=100  VSTEP=10  NSTEP=5

$  Plot structure at 150V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 150V"
CONTOUR POTENTIA DEL.V=5 COLOR=2

SOLVE ELECTROD=Drain V(Drain)=150  VSTEP=10  NSTEP=5

$  Plot structure at 200V
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at 200V"
```

```
CONTOUR POTENTIA DEL.V=5 COLOR=2

$  Continue solving
SOLVE ELEC=Drain CONTINU  C.VSTEP=0.001 C.VMAX=1500 C.IMAX=1E-9 C.TOL=0.1

$ Print electric field
PRINT   E.FIELD X.COM Y.COM X.MIN=-@w X.MAX=@w Y.MIN=-@Ly Y.MAX=0

$ Plot E field
PLOT.1D          E.FIELD X.START=-0.5*@w  X.END=-0.5*@w  Y.START=-(@Ly+2) Y.END=2
+          COLOR=2          TITLE="E-field at P/N interface"
PLOT.1D          E.FIELD X.START=0  X.END=0  Y.START=-(@Ly+2)        Y.END=2
+          COLOR=2          TITLE="E-field at center of N column"

$  Breakdown curve
PLOT.1D X.AX=V(Drain) Y.AX=I(Drain) POINTS ^ORDER  TOP=8E-10
+ LEFT=0  RIGHT=400 TITLE="Vbr, conventional"

$  Plot E vector
PLOT.2D BOUND  JUNC  DEPL  FILL  SCALE   TITLE="E-vector"
VECTOR E.FIELD COLOR=1

$  Plot hole distribution in the region
PLOT.2D  BOUND  DEPL JUNC SCALE  TITLE="Holes Distribution Contour"
CONTOUR    HOLE LOG FILL

$  Plot electron distribution
PLOT.2D  DEPL BOUND  JUNC  SCALE  TITLE="Electrons Distribution Contour"
CONTOUR    ELECTRON LOG FILL MIN=1.0 DEL=1.0

$  Full Flowlines, V and impact ionisation for last solution
PLOT.2D  BOUND JUNC  DEPL  FILL SCALE   TITLE="Struct at Breakdown"
CONTOUR POTENTIA DEL.V=10 COLOR=2
CONTOUR FLOWLINE COLOR=1
CONTOUR II.GEN   COLOR=4


STOP
```

B.4 MEDICI input file for Gradient OBUMOS structure

```
$ GOB Structure Off-State Simulation

$ Control bias = 5*X
$ 2w is the width of whole n-drift region
$ Ly is n-drift depth
$ dp is pbody depth
$ epi thickness = Ly + dp
$ pbody depth = 1.5 um
$ polysilicon width = 0.5 um

ASSIGN          NAME=X          C.VAL=0
ASSIGN          NAME=Nd         C.VAL=7E15
ASSIGN          NAME=Ly         C.VAL=15
ASSIGN          NAME=w          C.VAL=2.5
ASSIGN          NAME=tox        C.VAL=2.5
ASSIGN          NAME=X1         C.VAL=0.1
ASSIGN          NAME=X2         C.VAL=0.1


MESH

X.MESH          LOCATION=-@w-@tox  SPACING=0.1
X.MESH          LOCATION=-@w+0.3   SPACING=0.1
X.MESH          LOCATION=0         SPACING=0.5
X.MESH          LOCATION=@w-0.3    SPACING=0.1
X.MESH          LOCATION=@w+@tox   SPACING=0.1

Y.MESH          LOCATION=-(@Ly+1.5) SPACING=0.3
Y.MESH          LOCATION=-(@Ly+1)   SPACING=0.2
Y.MESH          LOCATION=-@Ly       SPACING=0.1
Y.MESH          LOCATION=-(@Ly-0.3) SPACING=0.1
Y.MESH          LOCATION=-@Ly/2     SPACING=0.5
Y.MESH          LOCATION=-@tox-0.3  SPACING=0.1
Y.MESH          LOCATION=-@tox      SPACING=0.1
Y.MESH          LOCATION=0          SPACING=0.1
Y.MESH          LOCATION=1          SPACING=0.5
Y.MESH          LOCATION=2          SPACING=0.5


REGION          SILICON
REGION          OXIDE  X.MIN=-@w-@tox X.MAX=-@w Y.MIN=-@Ly-1.5 Y.MAX=0
REGION          OXIDE  X.MIN=@w  X.MAX=@w+@tox  Y.MIN=-@Ly-1.5 Y.MAX=0

ELECTROD        NAME=Source   X.MIN=-@w      X.MAX=@w
+               Y.MIN=-(@Ly+1.5)             Y.MAX=-(@Ly+1)
ELECTROD        NAME=Drain    X.MIN=-@w-@tox       X.MAX=@w+@tox
+               Y.MIN=1       Y.MAX=2
ELECTROD        NAME=ELE1     POLYGON
+       X.POLY=(-@w-@tox, -@w-@tox, -@w-@tox+@X2, -@w-@X1, -@w-@X1)
+       Y.POLY=(-@Ly-1.5, -@tox, -@tox, -@Ly, -@Ly-1.5)
ELECTROD        NAME=ELE1     POLYGON
+       X.POLY=(@w+@tox, @w+@tox, @w+@tox-@X2, @w+@X1, @w+@X1)
+       Y.POLY=(-@Ly-1.5, -@tox, -@tox, -@Ly, -@Ly-1.5)

PROFILE         P-TYPE N.PEAK=1E17  UNIF    X.MIN=-@w      X.MAX=@w
+               Y.MIN=-@Ly-1            Y.MAX=-@Ly
```

```
PROFILE         N-TYPEN.PEAK=@Nd  UNIF    X.MIN=-@w      X.MAX=@w
+               Y.MIN=-@Ly        Y.MAX=0
PROFILE         N-TYPEN.PEAK=1E20  UNIF   X.MIN=-@w-@tox-0.5
+         X.MAX=@w+@tox+0.5       Y.MIN=0              Y.MAX=1

PLOT.2D         GRID    TITLE="Initial Grid"      FILL     SCALE
PLOT.2D         SCALE  BOUND                      FILL     TITLE="Impurity Contour"
CONTOUR         DOPING          LOG     MIN=14          MAX=22          DEL=0.1 COLOR=2
CONTOUR         DOPING          LOG     MIN=-22         MAX=-14         DEL=0.1 COLOR=1

$  Impurity Profile
PLOT.1D         DOPING          X.START=5       X.END=5         Y.START=-17     Y.END=2
+               Y.LOG           POINT           BOT=1E14        TOP=1E22
+               COLOR=2         TITLE=" doping profile"

$ Model statement
MODELS    IMPACT.I CONMOB    FLDMOB  CONSRH  AUGER  BGN SRFMOB2

$ Symbolic and method statement
SYMB            CARR=0
METHOD          ICCG  DAMPED

$ Initial solution
SOLVE           V(Source)=0.0           V(Drain)=0.0    V(ELE1)=0.0
SOLVE           ELECTROD=ELE1           V(ELE1)=0.0     VSTEP=5         NSTEP=@X

$  Obtain solution by 2-carrier Newton with continuation
SYMB      CARR=2          NEWTON

$  Breakdown test with drain current of  1E-9 /um
SOLVE  ELECTROD=Drain          V(Drain)=0      VSTEP=0.1       NSTEP=2
SOLVE  ELECTROD=Drain          V(Drain)=0.5    VSTEP=0.5       NSTEP=2
SOLVE  ELECTROD=Drain          V(Drain)=1      VSTEP=1         NSTEP=9
SOLVE  ELECTROD=Drain          V(Drain)=10     VSTEP=10        NSTEP=4

$  Continue solving
SOLVE ELEC=Drain CONTINU  C.VSTEP=0.001 C.VMAX=800 C.IMAX=1E-9 C.TOL=0.1

PRINT           E.FIELD         X.COM Y.COM X.MIN=-@w-@tox      X.MAX=0
+               Y.MIN=-@Ly      Y.MAX=0
PLOT.1D         E.FIELD         X.START=-@w+0.1         X.END=-@w+0.1
+               Y.START=-(@Ly+1.5)                      Y.END=@tox+1.5
+               COLOR=2         TITLE="E-field at Oxide/n-drift interface"
PLOT.1D         E.FIELD         X.START=0       X.END=0
+               Y.START=-(@Ly+1.5)              Y.END=@tox+1.5
+               COLOR=2         TITLE="E-field at center of n-drift"

$  Breakdown curve
PLOT.1D         X.AX=V(Drain)  Y.AX=I(Drain)   POINTS          ^ORDER          TOP=1E-9
+               LEFT=0          RIGHT=400       TITLE="Vbr, conventional"

STOP
```

END OF THESIS