THE DESIGN OF A 250MHZ CMOS BANDPASS SIGMA-DELTA A/D MODULATOR WITH CONTINUOUS-TIME CIRCUITRY

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SUMMARY

The bandpass delta sigma A/D converter is one of the best candidate to convert an RF or IF narrow band signal to a digital signal for processing and heterodyning in digital domain. The majorities of delta-sigma modulators in the literature are implemented as discrete-time circuits. However, the speed of these modulators is limited, both by OPAMP bandwidth and the required settling time. The idea of using continuous-time filters in delta sigma modulators was developed to relax the clock rate restrictions and in recent years clocking rates in the gigahertz range were reported. To achieve such a high speed data conversion, these modulators were realized using RF transistors based on GaAs or InP technologies, and were hard to be integrated on the same chip with digital signal processing modules which are realized in standard CMOS technology. On the other hand, attempts in CMOS bandpass delta sigma modulators are still limited to IFs of tens of megahertz. In this project, a fourth-order bandpass continuous-time delta sigma modulator was designed using 0.35μm CMOS technology which is sampled at 1-GHz for conversion of narrowband signals centered on 250 MHz.

The modulator presented here is based on two on-chip parallel LC tanks. The series connection of two second-order LC resonators yields a fourth order modulator. The integrated inductors have a quality factor as low as 1.5 at 250MHz, so Q-enhancement transconductors are connected to on-chip LC tank in parallel as negative resistors to cancel the positive resistance of the on-chip inductors. Due to the very low value of the inductor quality factor, the resonators realized by the LC tanks (together

with the negative resistors) have a low pass term included in the numerator, instead of being purely band pass. In order to maintain full controllability of the continuous-time modulator to keep it equivalent to its prototype discrete-time design, the single-bit quantizer and latches are arranged in a one-digital-delay multi-feedback architecture. Both Return-to-Zero (RZ) and Half-delayed Return-to-Zero (HRZ) feedback waveforms are used to provide four tunable parameters. The feedback is implemented by current-summing with simple tunable current-switching DACs. The clock feed-through problem is solved by placing a swing-reduction driver before the current-switching DACs. Excess loop delay is compensated by a specially introduced delay in the clock signal. Metastability effects are mitigated by the one-digital-delay scheme which introduces two additional half-sample delayed latches in the feedback loop. These two additional latches provide the circuits enough regeneration time to resolve the quantizer input. Transconductors used in the modulator are based on the structure first proposed by Nauta in 1989 which is applicable for operation in VHF up to gigahertz.

The bandpass delta sigma modulator is implemented in a 0.35μm triple-metal standard digital CMOS technology. The modulator occupies about 1.0 mm^2, with the two on-chip inductors consuming about 60% of the total area. Post-layout simulation in CADENCE design environment with the simulator SPECTRE demonstrates the modulator achieves a 7.5-bit performance in a 15.6MHz bandwidth corresponding to an over-sampling ratio of 64. The clocking limit of 1GHz is imposed by the quantizer circuit. If the same circuit is implemented in CMOS technologies with shorter channel lengths, the sampling rate limit can be pushed higher.

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LIST OF ABBREVIATIONS

ΣΔ (ΔΣ)	sigma delta
A/D	analog to digital
AC	alternating current
ADC	analog to digital converter
AGC	automatic gain control
CT	continuous-time
DAC	digital-to-analog converter
DC	direct current
DR	dynamic range
DSP	digital signal processing
DT	discrete-time
Gm-C	transconductor-capacitor
HNZ	half-delayed return to zero
IC	integrated circuit
IF	intermediate frequency
LNA	low noise amplifier
LO	local oscillator
NTF	noise transfer function
NTZ	non return to zero
NZ	return to zero

OPAMP	operational amplifier
OSR	oversampling ratio
Q	quality factor
RF	radio frequency
S/H	sample-and-hold
SNR	signal-to-noise ratio
SNDR	signal-to-noise-and-distortion ratio
STF	signal transfer function
VCO	voltage controlled oscillator

CHAPTER 1

INTRODUCTION

The relentless advances in integrated-circuit (IC) technology have provided compact, efficient implementation of digital signal processing algorithms in silicon, and indeed have moved many functions of signal processing to the digital domain. However, analog circuits have proved to be fundamentally necessary in many of today's complex, high-performance systems, since the naturally occurring signals are analog. The analog-to-digital (A/D) conversion determines the border between analog circuitry and digital signal processing (DSP). Therefore, the design of an analog-to-digital converter (ADC) becomes a crucial task in shifting the signal processing to the digital domain.

1.1 A/D Conversion in Radio Receivers

The architecture of a radio receiver front-end can mainly be partitioned into four parts: an antenna, an analog signal processing part, A/D interface and a digital signal processor [1].

Figure 1.1 shows the architecture model of a traditional super-heterodyne receiver. The radio frequency (RF) antenna signal is mixed with a sinusoid produced by the local oscillator (LO) down to an intermediate frequency (IF), after it is filtered by a wideband filter and amplified by a low noise amplifier (LNA). Then, the desired IF channel is selected and amplified with automatic gain control (AGC). A second LO further mixes the IF channel to baseband, with quadrature mixing of the signal to

in-phase (I) and quadrature-phase (Q) components for image rejection. The baseband signals are then digitized and further signal processing is done in the DSP.

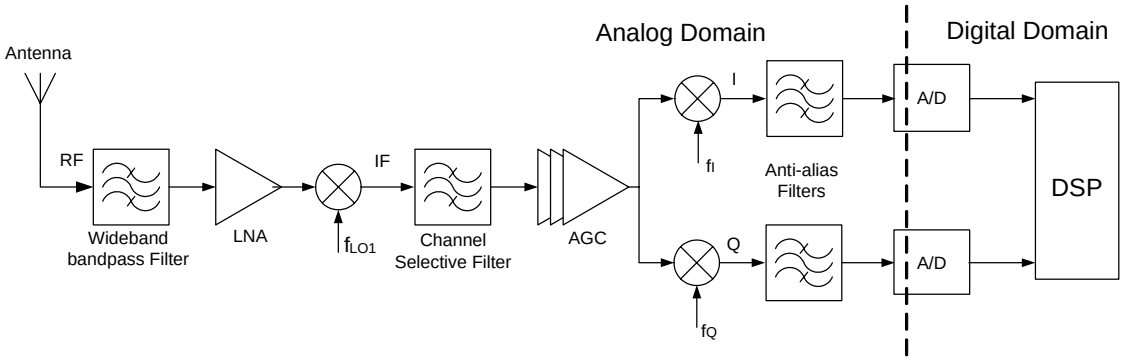

Figure 1.1 Traditional super-heterodyne receiver architecture

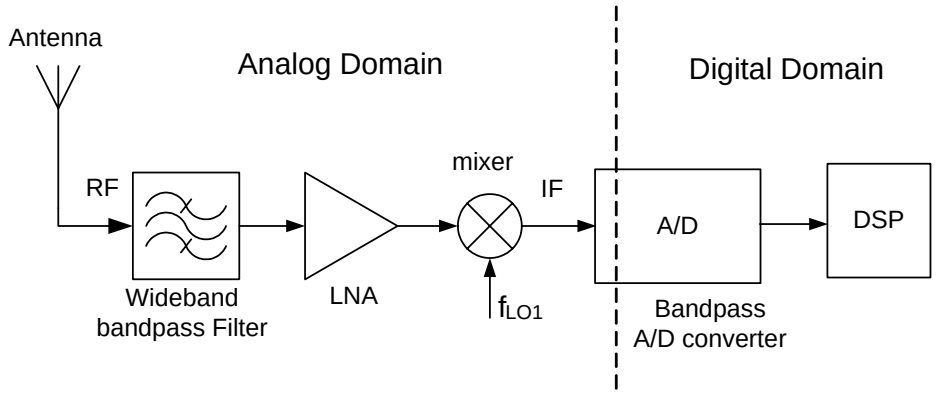

Figure 1.2 Digital radio receiver with wideband IF A/D conversion

The ADCs in such an architecture have relaxed requirements, as the desired channel is already selected and mixed to the baseband, but the analog part which includes LNA, channel filters and mixers, significantly adds to the total component count and power consumption, and it also has a substantial impact on size and cost. Shifting the analog functions into the digital domain is thus desirable to reduce the complexity of the receiver. Figure 1.2 demonstrates the structure of a radio receiver with IF digitizing, where the IF filters and the quadrature mixer are all realized in the digital domain. The wideband ADC digitizes all channels and leaves the channel selection to be

done in the DSP. The ultimate digital radio one can imagine is to nearly incorporate the whole system into the DSP, digitizing the RF signal right after the antenna.

By pushing signal processing functions into the digital domain, the overall system becomes more power efficient with less analog building blocks, and digital processing has the advantage of perfect linearity and matching for excellent image rejection performance. Another aspect of this architecture is the digital programmability, which allows for flexibility in adapting the radio to different standards or different systems by only changing software programs. Testing becomes systematic and changing filter coefficients becomes easy. However, with the A/D interface moved closer to the antenna, more stringent performance specifications are put on the ADC design and due to circuit non-idealities and parasitic effects, linearity and dynamic range requirements are more difficult to meet at higher frequencies.

1.2 Motivation and Objectives

The bandpass Sigma Delta ($\Sigma\Delta$) A/D converter has been a good candidate for audio and radio applications, due to its low power capability, high linearity and inherent anti-aliasing properties. It performs direct conversion of an RF or IF signal to digital for processing and heterodyning in digital domain.

The majorities of $\Sigma\Delta$ modulators in the literature are implemented as discrete-time (DT) circuits by switched-capacitor [2][3] or switched-current [4] techniques. However, the speed of these modulators is limited, both by operational amplifier (OPAMP) bandwidth and the required settling time. To reduce the settling time of the OPAMP, large current is required, resulting higher power dissipation and larger die size.

The idea of using continuous-time (CT) filters in $\Sigma\Delta$ modulators that eliminates the need of high speed OPAMPs was developed to relax the clock rate restrictions [5][6] and in recent years clocking rates in the gigahertz range were reported [7][8]. To achieve

such a high speed data conversion, these modulators were realized using RF transistors based on GaAs or InP technologies, and were hard to be integrated on the same chip with digital signal processing modules which are realized in standard CMOS technology. On the other hand, attempts in CMOS bandpass ΣΔ modulators are still limited to IF of tens of megahertz [9][10].

The objective of this project is to design a fourth-order bandpass CT ΣΔ modulator using 0.35μm standard CMOS technology. It is expected that the modulator is capable of being clocked at 1-GHz for direct conversion of signals centered on 250MHz. It is for the first time that such a high speed is ever tried in CMOS ΣΔ A/D designs.

1.3 Organization of the Thesis

Following the chapter of introduction, the fundamentals of traditional DT ΣΔ modulation are presented in Chapter 2 step-by-step. We provide a brief introduction to the key concepts, such as oversampling and noise shaping. The design of higher order and bandpass modulators is also explained.

In Chapter 3, we introduce the architecture of CT ΣΔ modulator and also briefly review some major advantages CT modulators have over their DT counterparts. Two methods of transformation between CT loop filters and the equivalent DT filters are explained, which enable us to make use of the available DT design techniques for the design of CT modulators. The multi-feedback architecture is also shown for a bandpass CT modulator design.

Chapter 4 explores the practical issues involved in the implementation of CT modulator designs. Important aspects of major non-idealities are covered: asymmetric DAC feedback pulses, delay in the modulator feedback path, timing uncertainty caused by clock jitter and metastability effects. Remedies for surmounting these performance limiting factors are also discussed.

Details about the design and simulation of the high speed CT bandpass ΣΔ modulator are presented in Chapter 5. Building blocks are characterized in detail. The continuous-time loop filter is based on two on-chip parallel LC tanks, and the modulator is implemented in a 0.35μm triple-metal standard CMOS technology. Results of post-layout simulation in CADENCE environment are also given.

Finally, the conclusions are drawn in Chapter 6. The performance of the modulator described in this work is compared with other state-of-the-art designs and some future work is recommended for further investigation.

Part of the research work presented in this thesis was reported in the publication [11]: Liang Yunfeng and Lian Yong. "A 250MHz CMOS Bandpass Delta-Sigma Modulator Using Continuous-Time Resonator Structure". *Proceedings of IEEE Circuits & Systems Workshop on Wireless Communications and Networking*, Pasadena, USA, Sep. 2002

CHAPTER 2

FUNDAMENTALS OF SIGMA DELTA CONVERTERS

Real world signals are continuous in time and amplitude. In order for digital systems to process these signals, they have to be sampled in time and quantized in amplitudes. While distortion resulting from sampling in time can be avoided by sampling faster than the Nyquist rate, the quantization in amplitudes will introduce errors. Sigma Delta converters utilize the concepts of both oversampling and noise shaping to increase the overall quantization performance. The basic idea behind oversampling is the exchange of resolution in time for resolution in amplitude. Noise shaping further attenuates the noise within the signal band and pushes it outside the band of interest, which can then be removed by decimation filters.

2.1 Nyquist Rate Conversion and Quantization Noise

Analog to digital conversion of a signal requires two separate operations: uniform sampling in time, and quantization in amplitude.

In the sampling phase, a continuous time signal is sampled at uniformly spaced time intervals (T). In the frequency domain, the sampling process is equivalent to creating periodically repeated versions of the signal spectrum, at multiples of the sampling frequency $f_s = 1/T$, [12], as represented in Eq.(2.1), where $X_s(f)$ is the

spectrum of the sampled signal, and $X(f)$ is the spectrum of the original continuous time signal.

$$X_s(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X(f - kf_s) \tag{2.1}$$

Figure 2.1 graphically shows the effect of the sampling process. Nyquist's sampling theorem states that a band limited signal should be sampled at a rate at least twice of its bandwidth f_B, i.e. $f_s \geq 2f_B$. The signal can be recovered only when the repeated versions of the original signal spectrum (the shaded area) do not overlap. The discretization or quantization in time as a result of the sampling is an invertible operation, since no signal information is lost.

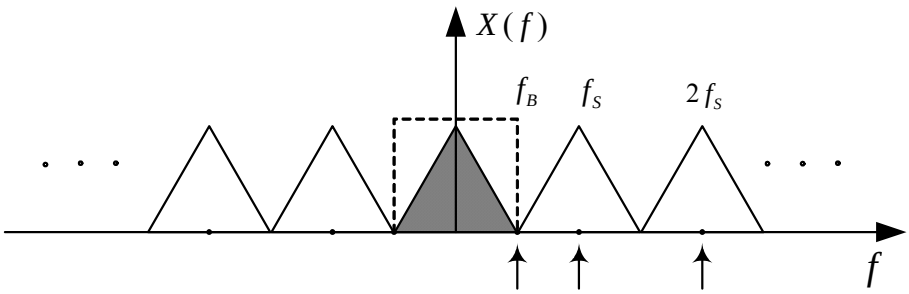

Figure 2.1 Nyquist rate sampling

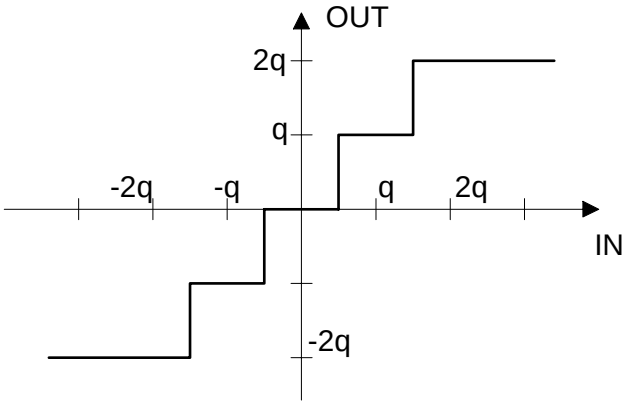

Figure 2.2 Five-level midtread quantization

Once sampled, the signal must also be discretized in amplitude to a finite set of values, which is a memoryless, time invariant and nonlinear operation. The amplitude continuous input signal is mapped onto a set of discrete output values by rounding or a type of truncation. Figure 2.2 is an example which shows the transfer characteristics of a 5-level rounding quantizer. The input threshold levels at which the output changes value are commonly spaced equidistantly with step size q, resulting in a uniform quantization.

Having looked at the sampling and quantization aspects, we now characterize the performance modeling of the quantization noise. An ideal $N-$bit ADC has 2^N quantization steps. Assuming an input signal range of $\pm V$, the quantization step height is $q = 2V / 2^N$. To simplify the analysis of the nonlinear operation, the quantization noise is commonly modeled by an independent additive white noise source, which is uniformly distributed over [-q/2, q/2], if certain requirements are met as suggested by Widrow [13]. The quantizer is therefore modeled as $y[n] = x[n] + e[n]$. Under these assumptions, the mean square value of $e[n]$, i.e, power of the noise signal, is

$$\sigma_e^2 = \frac{1}{q}\int_{-q/2}^{q/2} e^2 de = q^2/12 \tag{2.2}$$

The largest sine wave signal which does not overload the ADC has an amplitude of V. As a result, the maximum signal-to-noise ratio (SNR) is

$$SNR = \left(\frac{V^2}{2} / \sigma_e^2\right) = \left(\frac{V^2}{2} / \frac{\left(2V/2^N\right)^2}{12}\right) = 6.02N + 1.76(dB) \tag{2.3}$$

For most conventional Nyquist rate ADCs, higher resolution is achieved by using smaller step sizes, which demand the use of precisely-matched analog components. Therefore high resolution Nyquist rate converters are extremely difficult to be inexpensively realized.

2.2 Oversampling Technique and Noise Shaping Concept

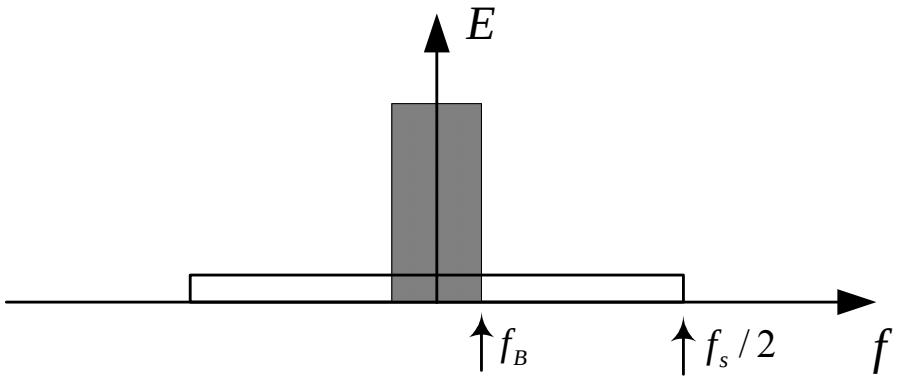

Figure 2.3 Power spectrum of quantization noise

Oversampling [14] is simply the process of sampling at a rate significantly faster than the Nyquist rate, and the oversampling ratio is defined as

$$OSR = \frac{f_s}{2 f_B} \tag{2.4}$$

Oversampling improves the resolution by reducing the amount of in-band quantization noise. Figure 2.3 shows the power spectral density of the quantization noise for both a Nyquist rate ADC (shaded) and an oversampled ADC (non-shaded). Although the total power (area) of the quantization noise is the same for both cases, as calculated in Eq.(2.2), the noise that falls within the signal band is much lower when the ADC is oversampled. The in-band noise power at the output of the oversampling ADC is:

$$n_0^2 = \int_{-f_B}^{f_B} E_q{}^2(f)df = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s} df = \sigma_e^2 \bullet \frac{2 f_B}{f_s} = \sigma_e^2 \bullet \frac{1}{OSR} \tag{2.5}$$

The maximum achievable SNR in db is then:

$$SNR = \log(\frac{V^2}{2} / n_0^2) = 6.02N + 1.76 + 10\log(OSR) \tag{2.6}$$

The maximum SNR has increased by $10\log(OSR)$, compared to Nyquist rate converters. The SNR improves by about 3dB, which is equivalent of an increase of 0.5 bit in

resolution, for every doubling of the OSR. In this scheme, the increased resolution in amplitude is achieved by the increased resolution in sampling time. Hence, the complexity of analog circuits is much lower than that of Nyquist converters, and the oversampling technique also enables a 1-bit ADC to achieve multi-bit resolution.

By oversampling, a fixed quantization noise power is spread to a much wider bandwidth which reduces the in-band noise. Techniques of noise shaping, or so called noise modulation, can further attenuate the noise within the signal band. It can be viewed as shaping the spectrum of the quantization noise as to push most of its energy outside the signal band. Out-of-band noise, including quantization noise, is then removed or suppressed by subsequent digital lowpass or bandpass filters which are sometimes referred as decimation filters. The simplest noise shaping modulator is a first-order sigma delta modulator with 1-bit quantization, which we are going to discuss in the next session.

2.3 Sigma Delta Modulators

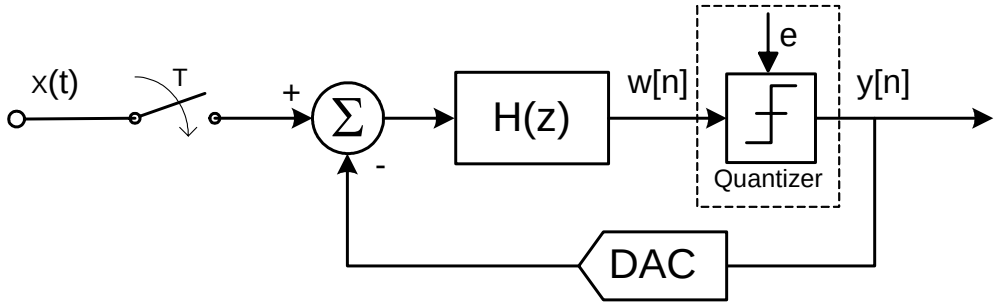

Figure 2.4 Basic components of a ΣΔ modulator

Actually, the term sigma-delta (ΣΔ) has almost become synonymous with noise shaping ADCs. It is so named because it utilizes integrators to accumulate the difference between the input and the quantization output [14][15][16]. A block diagram of a ΣΔ modulator is shown in Figure 2.4.

A $\Sigma\Delta$ modulator has three key components:

(a) A loop filter or loop transfer function $H(z)$

(b) A quantizer clocked at a period of T

(c) A Digital-to-Analog Converter (DAC) in the feedback path

In the figure, the quantizer is replaced by the linearized noise model, which was discussed in section 2.1, and the signal being quantized is not the discrete time samples of the input, $x[n]$, but $w[n]$, the filtered version of the difference between the input and an analog representation of the output. The discrete time filter $H(z)$ is often called as the feed-forward loop filter.

The output $y[n]$ may now be calculated in terms of the input x and the quantization noise e:

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) = STF \bullet X(z) + NTF \bullet E(z) \tag{2.7}$$

where $STF = \frac{H(z)}{1+H(z)}$ and $NTF = \frac{1}{1+H(z)}$. As we can see, the noise transfer function (NTF) is different from the signal transfer function (STF). We are exactly utilizing this difference to shape away the noise while being able to maintain the magnitude of the in-band signal.

2.3.1 First Order $\Sigma\Delta$ Modulator

Consider the system in Figure 2.4 with a one-bit quantizer which gives output value of only ± 1, while the feed-forward loop filter is a simple integrator, $H(z) = \frac{1}{z-1}$, we arrive at a first order $\Sigma\Delta$ Modulator.

From Eq.(2.7), the modulator output $Y(z)$ is then given by:

$$Y(z) = X(z)z^{-1} + E(z)(1-z^{-1}) \tag{2.8}$$

so that the $STF = z^{-1}$ and the $NTF = 1 - z^{-1}$, which means the input signal is reproduced faithfully in the output bit stream with only one delay, while the quantization noise has been shaped by a first order Z domain differentiator, or a high pass filter. The magnitude spectrum of the NTF is depicted graphically in Figure 2.5, with $z = \exp(j2\pi fT)$, where the frequency axis has been normalized to the sampling frequency $f_s = 1/T$. We can note the zero gain of NTF at DC (i.e. at $f = 0$) and it increases away from DC; hence, we say the quantization noise is shaped away from DC.

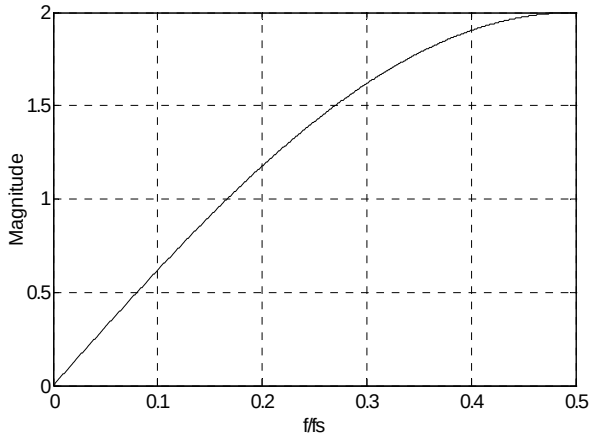

Figure 2.5 Noise transfer function of a 1st order modulator

At the output of a first order ΣΔ modulator, the in-band noise power in the frequency range of $[-f_B, f_B]$ is:

$$n_0^2 = \int_{-f_B}^{f_B} E_q^{\,2}(f)\left|1 - z^{-1}\right|^2 df = \int_{-f_B}^{f_B} \frac{\sigma_e^2}{f_s}\left|1 - e^{-j2\pi f/f_s}\right|^2 df = \sigma_e^2 \bullet \frac{\pi^2}{3} \bullet \left(\frac{2f_B}{f_s}\right)^3 = \frac{\pi^2 \bullet \sigma_e^2}{3 \bullet OSR^3} \quad (2.9)$$

The SNR in dB is then:

$$SNR = \log(\frac{V^2}{2} / n_0^2) = 6.02N + 1.76 + 30\log(OSR) - 10\log(\frac{\pi^2}{3}) \quad (2.10)$$

Thus, every doubling of the oversampling ratio results in an SNR improvement of 9dB, or equivalently, 1.5-bit increase in resolution.

As an example, we simulate the system mathematically in Simulink and obtain the power spectrum of the output bit stream, which is shown in Figure 2.6. In the simulation, the input tone has an amplitude of 0.5V, and it is located at 57.37Hz for a system with sampling rate of 10KHz. The power spectrum follows the shape of the NTF qualitatively. It is obviously from the picture that the noise is shaped away from the base band where the tone is located.

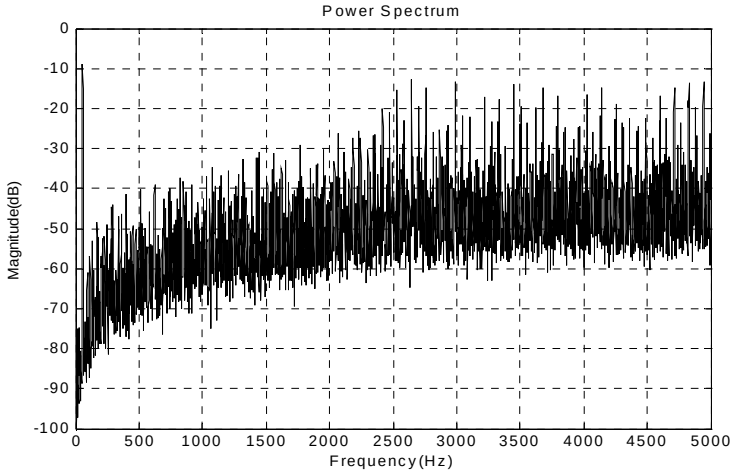

Figure 2.6 Simulated power spectrum after 1st-order noise shaping

The spectrum example in Figure 2.6 clearly contains periodic components spaced at an interval related to the input frequency. This is not surprising, because the ΣΔ modulator is a non-linear system, and the white noise assumption are not perfectly satisfied — the quantizer may be overloaded and successive quantizer input samples may be correlated (due to the non-random nature of the input signal).

2.3.2 Higher Order ΣΔ Modulator

In last subsection, we looked at the aspects of a modulator with a first order feed-forward loop filter and a single bit quantizer. The underlying ideas can be extended to higher order, multi-bit and multi-stage cascaded architectures. These ΣΔ converters

with higher order NTFs attain higher resolution by pushing more noise power outside the signal band. A modulator of order L based on a straightforward extension of the first order design realizes $STF = z^{-1}$ and $NTF = \left(1 - z^{-1}\right)^{L}$. Examples of higher order modulator topologies can be found in [17][18][19]. Most realizations of high order noise shaper have the single loop with a multi-order filter. Multi-loop structures with noise differencing are sometimes used. One typical topology is shown in Figure 2.7. Ideally, an L order modulator can achieve the in-band SNR of

$$SNR = 6.02N + 1.76 + (20L + 10)\log(OSR) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right)(dB) \qquad (2.11)$$

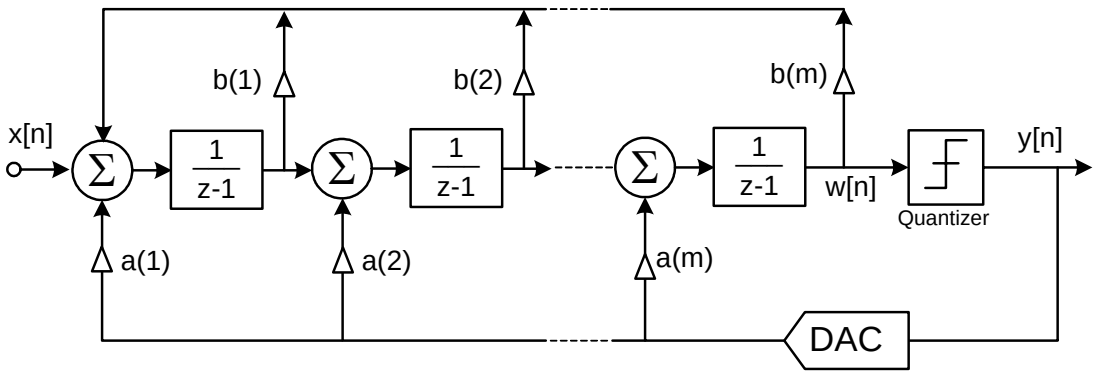

Figure 2.7 A typical m-order lowpass $\Sigma\Delta$ modulator structure

Each doubling of the oversampling ratio provides an extra $(6L+3)$ dB of SNR, or $(L+1/2)$ bits in resolution. As a result, a high-order modulator is usually desirable because of the great increase in converter dynamic range (DR). However, this level of performance is not achievable in practice. The stability of systems with $H(z)$ above order two becomes conditional when a one bit quantizer is used [20]. Input signals needs to be kept below a certain value to satisfy the stability criterion, otherwise, the modulator exhibits large, although not necessarily unbounded, states and a poor SNR compared with the predicted by Eq.(2.11), and thus the DR is greatly degraded.

Higher order modulators can also be built by cascading two or more low-order modulator stages, where later modulators' inputs are the quantization noise from previous stages [21]. Such ΣΔ modulators are called "MASH", an acronym deriving somehow from Multistage Noise Shaping. Figure 2.8 shows an example of a second order modulator obtained by cascading two first order modulators. The MASH structure provides a solution to the stability problems. Since each low order stage operates independently and each first order ΣΔ M is unconditionally stable, adding additional stages does not affect the stability of the overall system and thus the high order modulator is maintained unconditionally stable. However, in practice, this kind of structure is quite susceptible to circuit imperfections. Mismatches between components in stages will degrade the system performance and cause imperfect noise cancellation.

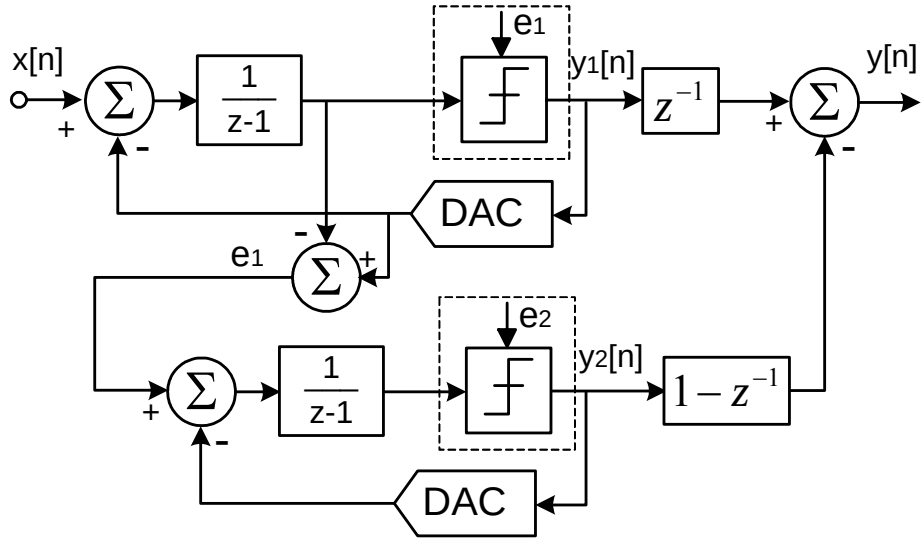

Figure 2.8 A second order multi-stage ΣΔ modulator

2.3.3 Multi-bit vs. Single-bit Quantizers

Until now, we have assumed that the quantizer and its corresponding DAC are one bit devices. One bit quantizer is frequently employed because of two reasons: the ease to build and its inherent linearity. Any mismatch in either of the two quantization

levels merely results in a DC offset or a gain mismatch. It is possible to replace the single bit quantizer with a multi-bit one to improve the overall $\Sigma\Delta$ M resolution. It is known that multi-bit quantizers enhance stability, especially for high-order designs. However, this is achieved at the expense of higher circuit complexity. Another main disadvantage is that the non-idealities in the multi-bit feedback DAC are directly input referred. A slight error in one DAC level substantially reduces system performance. Various techniques [22][23][24] have been proposed to compensate this effect, but circuit complexity will be further increased. The multi-bit output stream also requires a more complicated digital lowpass filter hardware following the modulator for multi-bit processing.

2.4 Bandpass $\Sigma\Delta$ Modulator

In the previous sections, we have discussed low-pass $\Sigma\Delta$ modulators, where the quantization noise has a high pass shape (Figure 2.5) with NTF zeros located at DC or low frequencies. They are built with low pass loop filters to shape the noise away from DC, as indicated by Eq.(2.7). If we replace the low pass filters with resonators, we can put the zeros of the NTF somewhere other than $z = 1$, and the noise will be shaped away from the resonant frequency. The resulting $\Sigma\Delta$ modulators then have a NTF of band stop shape and are called bandpass converters [25][26]. Regardless of where the signal is located with a center frequency of f_C, high resolution conversion can be achieved as long as the sampling rate f_S is much greater than the signal bandwidths $2f_B$ (equivalent two-sided bandwidth in baseband), rather than the highest signal frequency $(f_C + f_B)$. For bandpass $\Sigma\Delta$ modulators, the OSR is defined as the sampling frequency divided by the interested signal bandwidth $f_S / 2f_B$, which shares the same form as Eq.(2.4).

The design of bandpass modulators is not much more complicated than the lowpass cases. One of the many methods [27] is to perform $z \to -z^2$ transformation on the low pass prototype. The transformation maps zeroes of the NTF from DC ($z = 1$) to one quarter of the sampling frequency $f_S / 4$ ($z = \pm j$). This can produce a bandpass modulator with noise notch located at $f_S / 4$. Figure 2.9 shows an example of such modulators, which is derived from the first order prototype discussed in section 2.3.1. Its output magnitude spectrum is shown in Figure 2.10. The system has a sampling rate of 10KHz with the signal band around 2.5KHz. Quantization noise within the signal band is largely attenuated.

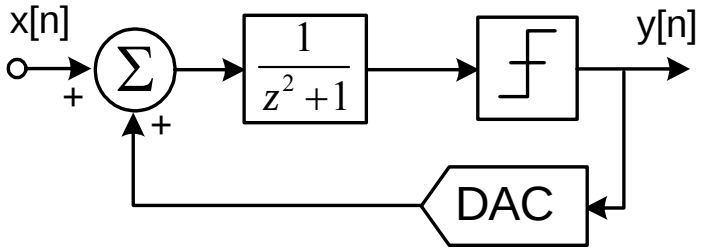

Figure 2.9 A 2nd order bandpass ΣΔM

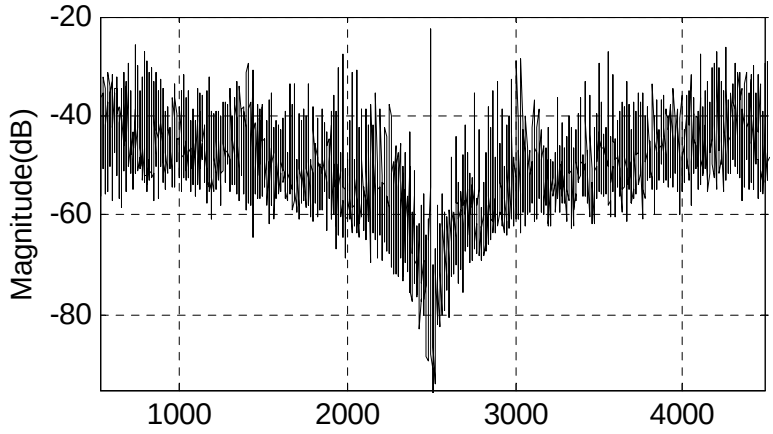

Figure 2.10 2nd-order bandpass output spectrum

Because this kind of bandpass modulators behaves as a pair of multiplexed low pass modulators with alternate samples, the stability and dynamics properties of the low pass prototype are maintained, even though the order is doubled. As a result, an N^{th} order bandpass modulator displays a SNR performance half the value as indicated by Eq.(2.11). The SNR improves at the rate of $(3N+3)dB$ per octave increment with the oversampling ratio.

The ability of such modulators to perform conversion of high-frequency narrowband signals to digital form makes them attractive for communication systems and special instrumentation for narrow-band sources. In communication applications, the capability of bandpass A/D conversion allows the A/D interface moved closer to the antenna, and results in a more robust system with increased flexibility, reduced component count and improved testability.

2.5 Summary

In this chapter, we begin with a brief description of the conventional Nyquist rate A/D conversion. The oversampling technique is then discussed, and the idea of noise shaping is introduced. The concept of sigma delta modulation is presented with a discussion of the first order modulator. The architecture and performance analysis of higher order designs are further explored. Finally, the design of bandpass $\Sigma\Delta$ modulation is reviewed.

CHAPTER 3

THE DESIGN OF CONTINUOUS-TIME ΣΔ MODULATORS

In order to simplify the understanding of the noise shaping concepts, thus far, we have assumed the signals and the loop filters of a noise shaper or ΣΔ Modulator to be discrete time. However, this is not a requirement. The loop filter can also be implemented as a continuous time (CT) circuit [6]. Although most reported ΣΔ modulators are designed with discrete time (DT) loops filters using circuit techniques such as Switched-Capacitor (SC) [2][3] or Switched-Current (SI) [4] circuits, they are limited by the maximum clock rate, due to settling time constraints in typical discrete time implementations. Because it is generally possible to clock CT ΣΔ modulators at much higher frequencies than DT modulators, there is increasing interest in building ΣΔ modulators using CT circuitry for the loop filter. It can be shown that the design of a CT ΣΔ modulator does not require much extra work. Since its overall behavior can be described and analyzed by it discrete time equivalent, with some kind of transformation, we can design a CT modulator in the DT domain as well.

3.1 Structure of Continuous time ΣΔ Modulators

In the discrete time model (Figure 3.1) which was discussed in the previous chapter, the continuous time input signal $x(t)$ is first pre-filtered and sampled, and then it

is fed to a fully discrete time modulator. For a continuous time modulator (Figure 3.2), on the other hand, the input signal $x(t)$ is not sampled before it enters the loop filter. A continuous time filter replaces the discrete time filter in the forward path of the modulator and the majority of the modulator is made with continuous time circuitry. The act of Sample-and-Hold (S/H) occurs inside the modulator loop, and in practice the SH circuitry can be combined with the quantizer. Although both the input and output signals of the loop filter $H(s)$ are continuous time signals, the output of the modulator $y[n]$ will remain a discrete time signal and a discrete to continuous time conversion $R(s)$ is therefore necessary to be performed in the feedback loop using a DAC. The boundary between continuous time and discrete time circuitry is shown in the models for both modulators.

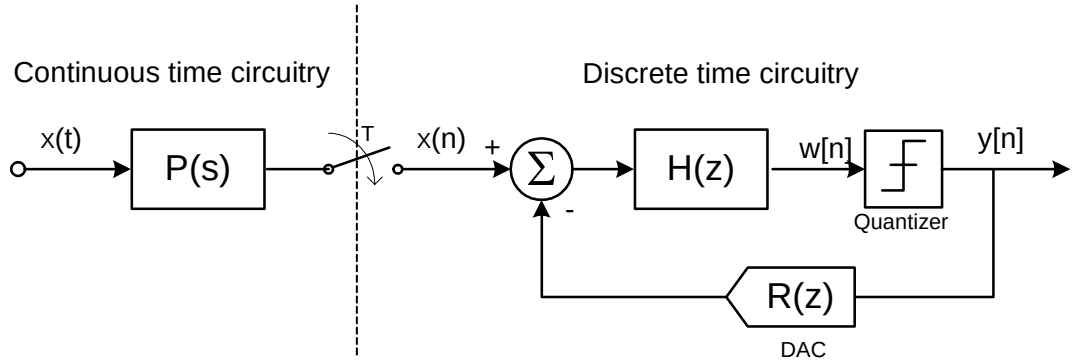

Figure 3.1 Model of a discrete time ΣΔ modulator

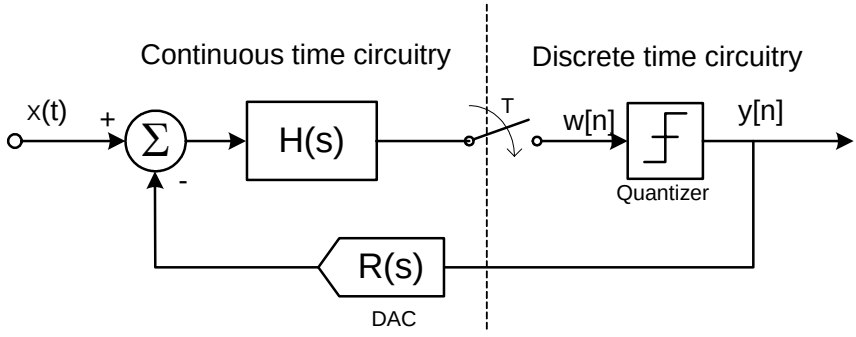

Figure 3.2 Model of a continuous time ΣΔ modulator

3.2 Motivation for Continuous time Design

A distinct advantage of CT modulators is the speed they can attain. A typical discrete time ΣΔ modulator has a maximum clock limited both by its OPAMP bandwidths and the settling time constraints. In continuous time modulators, waveforms vary continuously and the speed restrictions are relaxed. With no local feedback for the integrator, no settling requirement and no input sampling, a CT modulator could theoretically be clocked up to an order of magnitude faster than its DT counterpart in the same technology.

Another key advantage of using a continuous time loop filter instead of a discrete time loop filter is that the sampling operation takes place inside the loop. Pushing the sampling operation into the noise shaping loop causes S/H errors to be noise shaped along with quantizer errors. As a result, the criticality of the sample-and-hold block is also reduced.

The CT modulator is also less sensitive to clock glitches. As waveforms vary continuously in CT modulators, OPAMP (if any) virtual ground can be kept very quiet. But in a DT modulator, switching transients usually cause large clock glitches on OPAMP virtual ground nodes, which will surely impair the system performance.

Continuous time modulators can also provide a certain amount of anti-alias filtering at no cost [28]. Aliasing is a problem when working in the DT domain: due to the sampling process, any input frequency which is larger than half the sampling frequency f_S will reflect into the frequency range of $0 < f < f_S/2$, and thus signals separated by a multiple of the sampling frequency are indistinguishable. DT ΣΔ modulators usually require a separate filter, such as the $P(s)$ in Figure 3.1, at their inputs to suppress the aliasing components sufficiently. By contrast, anti-aliasing is an inherent property of the mathematics of CT ΣΔ modulators, as we shall see shortly.

3.3 Inherent Anti-Aliasing Property

From the Nyquist Theorem, we understand that the sampling process is equivalent to creating periodically repeated versions of the input signal spectrum, at multiples of the sampling frequency $f_S = 1/T$. As a result, extra filters are usually necessary to band limit the input signal and hence reduce the problem of aliasing. One nice feature of CT $\Sigma\Delta$ modulators is that they have inherent anti-aliasing capability.

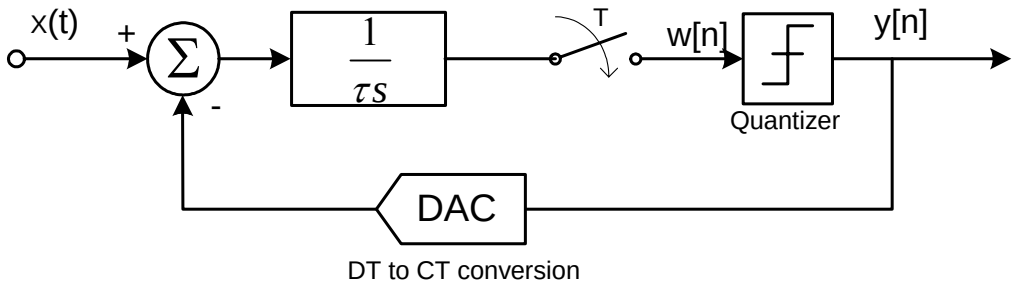

Figure 3.3 A first order CT $\Sigma\Delta$ modulator

Let's take a look of a simple example. Suppose we have in Figure 3.2 a single integrator, $H(s) = \frac{1}{\tau s}$, and an Non-Return-to-Zero (NRZ) DAC, $R(s) = 1$, which is a first order CT low pass modulator (redrawn in Figure 3.3). Immediately after the sampler, the quantizer input has the relation of

$$
\begin{aligned}
w[n+1] &= w[n] + \frac{1}{\tau}\int_{nT}^{(n+1)T} \big(x(t) - y[n]\big)dt \\
&= w[n] - \frac{T}{\tau}y[n] + \frac{1}{\tau}\int_{nT}^{(n+1)T} x(t)dt \\
&= w[n] - \frac{T}{\tau}y[n] + \frac{1}{\tau}\{x(t) * rect(0,T)\}\Big|_{t=(n+1)T} \\
&= w[n] - \frac{T}{\tau}y[n] + \frac{1}{\tau}\{X(s)\cdot sinc(f/f_S)\}\Big|_{t=(n+1)T}
\end{aligned}
\tag{3.1}
$$

where $rect(0,T)$ is a rectangular pulse of unit magnitude between 0 and T. It can be shown from Eq. (3.1) that the input spectrum is multiplied by the spectrum of a rectangular pulse which has spectral nulls right at the multiples of the sampling frequency. This is exactly where we want the nulls to be in the lowpass modulator for anti-alias purposes.

In the previous example, the input signal is integrated over one clock period prior to being sampled, and this is exactly where the anti-aliasing property arises. Because the sampling happens after the integration operation, the loop-filter is also operating as an anti-aliasing filter, therefore discarding the need for a special purpose anti-aliasing filter in front of the modulator. In a similar way, we can expect more anti-alias protection for higher order modulators, as they have more integrators before the sampler. It has been shown that the implicit anti-alias property is present for general CT modulators [29].

3.4 Design Methodology of CT $\Sigma\Delta$ Modulators

Discrete time $\Sigma\Delta$ modulators have had the most attention in the past and quite a great deal of software and literature are available for designing the DT modulator loop filters. Considerably less attention is devoted to the design of CT $\Sigma\Delta$Ms . Nonetheless, designing a CT modulator requires almost no extra work. We can find equivalence between DT and CT modulators, and thus CT design can be done in the discrete time domain. We can simply start the procedure by determining an appropriate DT loop filter $H(z)$, and then transform it to the continuous time equivalent $H(s)$ with the pulse shape of the DAC taken into consideration.

3.4.1 Transformation between CT and DT Systems

We have many methods for mappings between S domain and Z domain: forward Euler, backward Euler and bilinear transforms, but what we need is a mapping that can make the two modulators to be equivalent. We want the sampled responses of both the CT and DT ΣΔM loop-filters to be identical.

Impulse-Invariant Transformation

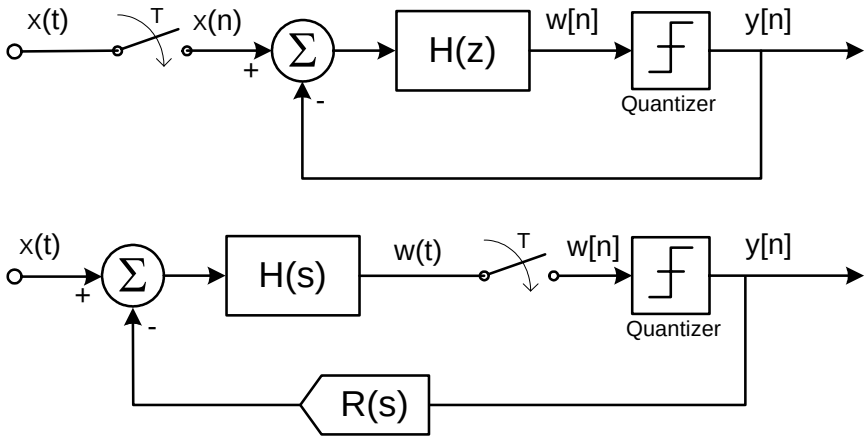

Figure 3.4 Mapping between DT and CT modulators

It turns out that the impulse invariant transformation is a straightforward choice. For the DT and CT modulators to be equivalent (Figure 3.4), their sampled impulse responses of the open-loops should be the same [28], and this leads to:

$$Z^{-1}\left[H(z)\right] = L^{-1}\left[R(s)H(s)\right]\Big|_{t=nT} \tag{3.2}$$

or, put in the time domain,

$$h(n) = \left[r(t) * h(t)\right]\Big|_{t=nT} \tag{3.3}$$

where $R(s)$ is the Laplace transform of the DAC feedback waveform $r(t)$ in the CT modulator. Suppose we have a DT modulator with a loop-filter $H(z)$ that has a particular noise shaping behavior. Given the DAC waveform $R(s)$, we can immediately find a CT modulator $H(s)$ with identical noise shaping performance by solving Eq. (3.2).

Eq. (3.2) and Eq. (3.3) also show us a most significant difference in the CT modulator design: as a continuous-time filter responds to signals continuously, a CT ΣΔ modulator has to be designed according to the DAC output waveform. CT ΣΔMs are sensitive to the exact behavior of the DAC over the entire feedback period, unlike DT designs which rely on the constancy of the DAC feedback value only at the end of sampling period.

There is no direct general solution for Eq. (3.2), and it must be solved by an analytic means for each case. However, in simple situations, we can still use symbolic mathematical program such as Maple or Matlab to solve the equation. As an example, we assume a perfectly rectangular DAC pulse of magnitude 1 that lasts within the sampling period (Figure 3.5):

$$r(t) = \begin{cases} 1, & \alpha T < t < \beta T, \ 0 \le \alpha < \beta \le 1 \\ 0, & otherwise \end{cases} \tag{3.4}$$

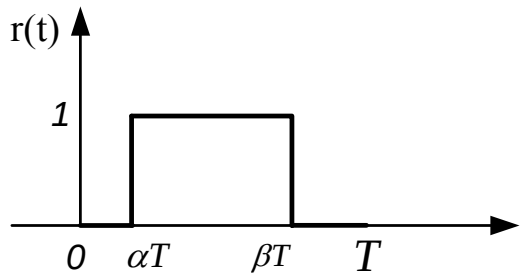

Figure 3.5 A rectangular DAC pulse

which covers most types of actual DAC waveforms. To simplify the following discussion, we normalize the sampling period T to 1 second. Applying the transformation to a second-order lowpass DT modulator

$$H(z) = \frac{-2z+1}{(z-1)^2} \tag{3.5}$$

with NRZ DAC $(\alpha, \beta) = (0,1)$, we can get the CT equivalent to be

$$H(s) = -\frac{1+1.5s}{s^2} \tag{3.6}$$

In the case of return-to-zero (RZ) DAC, $(\alpha, \beta) = (0, 0.5)$,

$$H(s) = -\frac{2+2.5s}{s^2} \tag{3.7}$$

can be derived as the CT equivalent of the second-order DT modulator in Eq. (3.5). If you prefer to remove the T=1 normalization, simply replace every s with sT in Eq. (3.6) and Eq. (3.7).

State-Space Method

In [30], Schreier presented another method that works in the state space domain. In stead of the pole-zero form like $H(z)$ or $H(s)$, he presented the linear parts of the DT and CT modulators in their state equations (Figure 3.6) as

$$m(n+1) = A \cdot m(n) + B \begin{bmatrix} x(n) \\ y(n) \end{bmatrix} \tag{3.8}$$

$$m_C(t)' = A_C \cdot m_C(t) + B_C \begin{bmatrix} x_C(t) \\ y_C(t) \end{bmatrix} \tag{3.9}$$

where m and m_C are respectively the state variables for DT and CT systems.

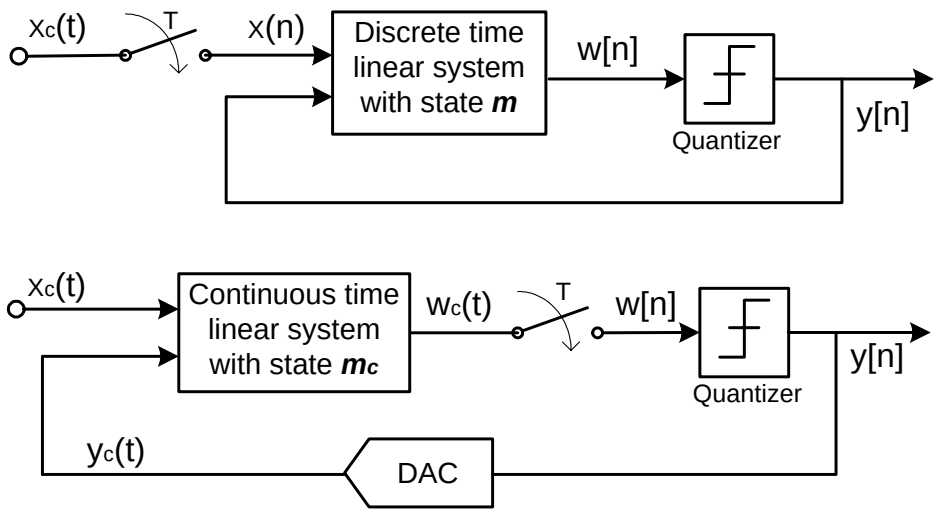

Figure 3.6 DT and CT modulators in the state space form

It was shown by Schreier that for the cases of rectangular DAC waveform as depicted in Eq. (3.4), the discrete and continuous systems would be equivalent, provided

$$A = e^{Ac} \tag{3.10}$$

and

$$B = A_C^{-1}(e^{Ac(1-\alpha)} - e^{Ac(1-\beta)})B_C \tag{3.11}$$

If the DAC waveform is a NRZ pulse with $(\alpha, \beta) = (0,1)$, Eq. (3.11) will be reduced to

$$B = A_C^{-1}(A - I)B_C \tag{3.12}$$

The advantage of using the State-Space Method is that there are readily available functions in Matlab [31] to do these transformations for us. To find the CT equivalent for the DT modulator in Eq. (3.5), we first convert the filter parameters of the transfer function into its state-space form using Matlab command "tf2ss" as shown below:

$$[A, B, C, D] = tf2ss([0\ -2\ 1],[1, -2, 1]) \tag{3.13}$$

which returns the matrices of a state space representation in A, B, C, and D. Then, the command ss is used to create the state-space model:

$$DTsys = ss(\mathrm{A,B,C,D},1) \tag{3.14}$$

The fifth parameter in the function is the sampling time in seconds. After that, the routine of $d2c$ transforms the discrete-time model to continuous time:

$$CTsys = d2c(DTsys) \tag{3.15}$$

If we convert the CT state-space model back into transfer function form with

$$tf(CTsys) \tag{3.16}$$

we will get the result of $H(s) = -\dfrac{1+1.5s}{s^2}$ just as in Eq. (3.6).

The $d2c$ command in Eq. (3.15) assumes a RTZ DAC with $(\alpha, \beta) = (0,1)$. For general rectangular DAC pulses (α, β), we have to take into consideration the difference

between Eq. (3.11) and Eq. (3.12), and make some modifications to the B matrix in the continuous time model after the step of Eq. (3.15):

$$CTsys.B = inv(expm(CTsys.A*(1-\alpha)) - expm(CTsys.A*(1-\beta))) \\ *(DTsys.A - eye(2))*CTsys.B \tag{3.17}$$

While this will work for most modulators, we have to consider the degenerate cases when the A matrix is singular and hence the expression involving $expm(CTsys.A)$ is also singular. This is exactly the situation for the exemplar modulator we are discussing, as

$$CTsys.A = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} \tag{3.18}$$

is singular. However, for practical purposes, we can avoid this singular matrix problem by manipulating the A matrix a little bit, such as changing Eq. (3.18) into $CTsys.A = \begin{bmatrix} 1 & -1.0000001 \\ 1 & -1 \end{bmatrix}$. We can still get an answer that is close enough to be correct. The complete Matlab code for the transformation is listed below.

```
[a,b,c,d]=tf2ss([0 -2 1], [1 -2 1]);
DTsys=ss(a,b,c,d,1);
CTsys=d2c(DTsys);
CTsys.A=CTsys.A+ [0 0; 0.0000001 0];
CTsys.B=inv(expm(CTsys.A*(1-m1))-expm(CTsys.A*(1-
            m2)))*(DTsys.A-eye(2))*CTsys.B;
tf(CTsys)
```

The `m1` and `m2` in the code denote the values of (α, β). With `m1` and `m2` set to be (0, 0.5), it will return $H(s) = -\frac{2+2.5s}{s^2}$, as we found out in Eq. (3.7).

3.4.2 Bandpass CT Modulators

The basic method for designing a bandpass CT $\Sigma\Delta$ modulator is the same as that for designing a CT low-pass modulator: Begin with a prototype DT design and convert it to an equivalent CT design.

As we have noted in section 2.4, performing the substitution of $z^{-1} \to -z^{-2}$ on a low pass DT $\Sigma\Delta$ modulator will give a bandpass system with the noise notch at $f_S/4$, while maintaining the stability properties and doubling the order. To study the design of bandpass CT $\Sigma\Delta$ modulator, we start with the double integration modulator $H(z) = \frac{-2z+1}{(z-1)^2}$ as in Eq. (3.5). After applying the $z \to -z^2$ substitution, we get our fourth order bandpass DT prototype

$$H_{BP}(z) = \frac{2z^2+1}{(z^2+1)^2} \tag{3.19}$$

Then the equivalent CT loop filter can be found using the transformation methods discussed previously. Doing this for RZ DAC pulses $(\alpha, \beta) = (0, 0.5)$, we get:

$$H_{BP}(s) = \frac{-2.146s^3 + 0.3906s^2 - 4.062s + 5.642}{(s^2 + (\pi/2)^2)^2} \tag{3.20}$$

In principle, the above mentioned process is straightforward. However, in practice, it can be complicated by numerous details, if we want to implement the derived equation in a circuit. First of all, we need address the controllability issue.

Fundamentally, lowpass $\Sigma\Delta$ modulators rely on having at least one integrator inside the loop, and DT $\Sigma\Delta$Ms have been built as a cascade of integrators $\frac{1}{z-1}$, which was shown in Figure 2.7. Building an $f_S/4$ bandpass DT modulator simply requires replacing the integrator blocks with resonator blocks $-\frac{1}{z^2+1}$ which is implied by the

$z \to -z^2$ substitution. To build lowpass CT modulators, it works quite much in the same way as their DT counterparts — cascading the CT integrators $\frac{1}{s}$, such as the ones in Figure 3.7 which is corresponding to Eq. (3.7). However, in order to build a bandpass CT modulator, simply replacing integrators with resonators (as we did for DT cases) is not sufficient. We have four numerator coefficients in Eq. (3.20) to control, but there are only two tunable parameters (a1 and a2) available in Figure 3.8. The design suffers from a lack of controllability.

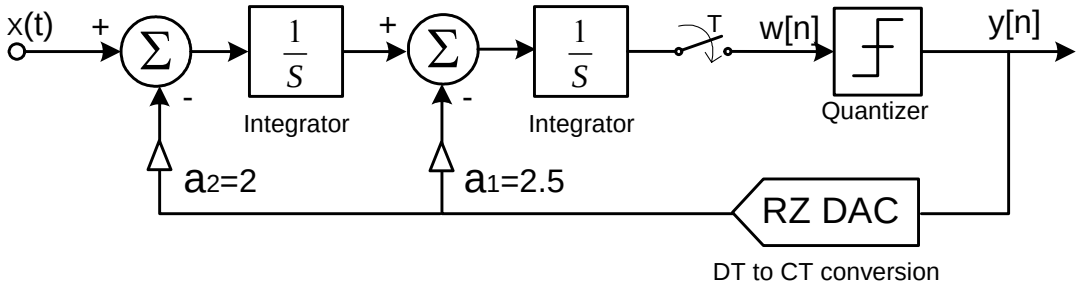

Figure 3.7 A lowpass 2nd-order CT ΣΔ modulator

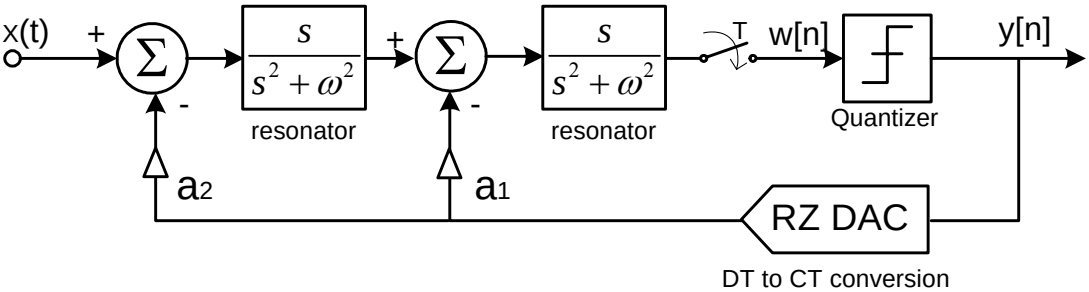

Figure 3.8 The controllability problem of replacing integrators with resonators

In order to maintain full controllability of the continuous-time modulator to keep it equivalent to the prototype discrete-time design, a multi-feedback architecture [5][32] can be adopted. We use one more type of feedback DAC in the loop (Figure 3.9), adding another set of two tunable parameters. Both Half-delayed Return-to-Zero (HRZ), which

has $(\alpha, \beta) = (0.5,\ 1)$, and Return-to-Zero (RZ) feedback waveforms are used to provide the necessary tunable parameters.

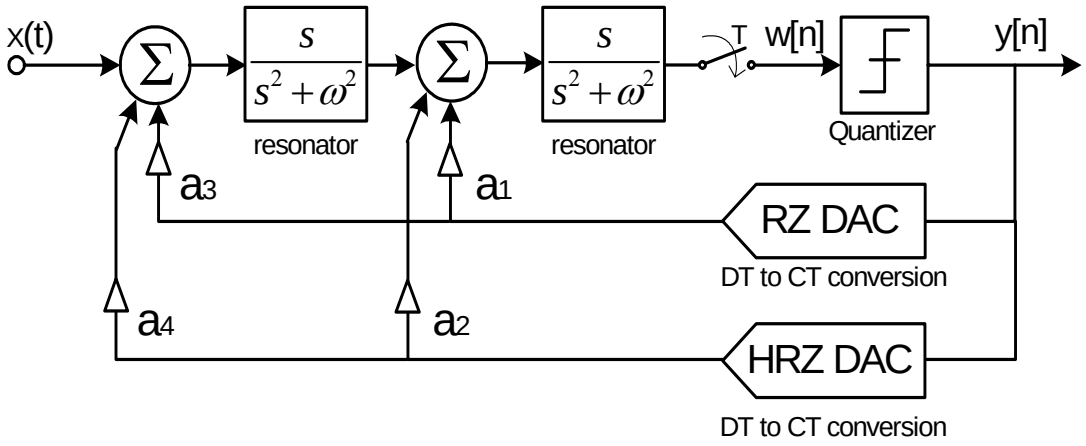

Figure 3.9 A multi-feedback structure for bandpass CT ΣΔ modulators

Thus far, we have mainly mentioned 3 types of DAC waveforms: NRZ, RZ and HRZ. Their exact shapes are depicted collectively in Figure 3.10.

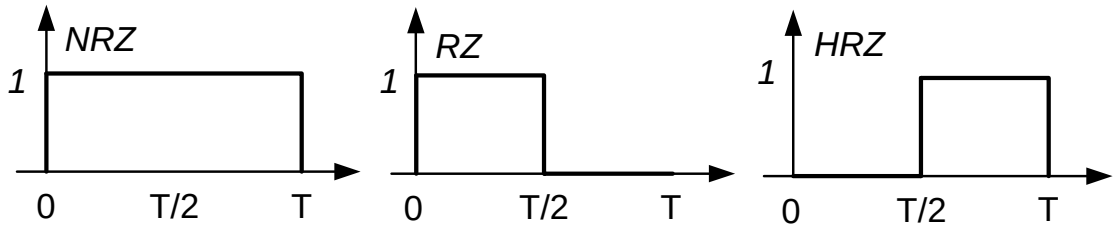

Figure 3.10 Common DAC pulse types

3.4.3 Calculation of the Feedback Coefficients

The controllability issue was addressed by the multi-feedback structure. However, in order for the system in Figure 3.9 to have an equivalent DT loop filter of Eq. (3.19), the feedback coefficients remain to be determined. Unfortunately, the methods covered in section 3.4.1 are not adequate to solve the puzzle, as we now have two DAC waveforms, instead of one, present in the system.

The previously discussed transformation methods are primarily aimed for mapping a working discrete time system into a CT system. On the other hand, their inverse transformation can be applied to a given CT modulator so that the resulting equivalent DT system can be found and analyzed. The loop filter and DAC can then be replaced by the equivalent DT filter to describe the overall behavior. In the light of this idea, we find our way to determine the feedback parameters.

There are four feedback paths in the system of Figure 3.9. For each path, we can find an equivalent DT transfer function of the continuous filter, by the inverse State-Space method with knowledge of the corresponding feedback DAC waveform. The linear superposition of these DT equivalents on the four feedback paths should yield the overall desired bandpass DT modulator in Eq. (3.19).

We begin with path *a1*, which has a continuous time filter of $H_{a1}(s) = \frac{s}{s^2 + w^2}$.

The w here equals to $\frac{\pi}{2}$ for a CT modulator with notch at $f_s / 4$. Applying the inverse State-Space transformation gives an equivalent DT transfer function of

$$H_{a1}(z) = \frac{\frac{(2-\sqrt{2})}{\pi} z - \frac{\sqrt{2}}{\pi}}{z^2 + 1} \tag{3.21}$$

Likewise,

$$H_{a2}(z) = \frac{\frac{\sqrt{2}}{\pi} z - \frac{(2-\sqrt{2})}{\pi}}{z^2 + 1} \tag{3.22}$$

$$H_{a3}(z) = \frac{0.2058z^3 - 0.3376z^2 + 0.0193z + 0.1125}{\left(z^2 + 1\right)^2} \tag{3.23}$$

$$H_{a4}(z) = \frac{0.1125z^3 + 0.0193z^2 - 0.3376z + 0.2058}{\left(z^2 + 1\right)^2} \tag{3.24}$$

are calculated respectively for the path of *a2*, *a3* and *a4*. Combining the four paths together to solve the equation of

$$a1 \cdot H_{a1}(z) + a2 \cdot H_{a2}(z) + a3 \cdot H_{a3}(z) + a4 \cdot H_{a4}(z) = \frac{2z^2 + 1}{(z^2 + 1)^2} \tag{3.25}$$

yields the feedback coefficients we are looking for:

$$(a1,\ a2,\ a3,\ a4) = (-3.3519,\ 2.3365,\ -2.6815,\ 1.1107) \tag{3.26}$$

The complete Matlab code for solving the feedback parameters is listed in Appendix A.

3.5 Summary

We explain in this chapter the structure of continuous time ΣΔ modulators and list some of the advantages CT ΣΔ modulators have over DT modulators. The inherent anti-aliasing property of CT modulators is covered in details. Next, we move on to explain how to design CT modulators in a step-by-step manner. The transformations that allow us to design CT modulators in the DT domain are presented and illustrated. For bandpass CT modulators, the design issue is complicated by the controllability problem. A multi-feedback structure is introduced and details of the feedback calculation are given.

CHAPTER 4

NON-IDEALITIY ISSUES FOR CT IMPLEMENTATION

While many kinds of non-idealities can limit system performances, CT designs of ΣΔ modulators are particularly sensitive to certain non-idealities involving the quantizer and feedback DACs. As a CT modulator responds to signals continuously, the modulator is sensitive to the exact shape of the DAC pulse. The DAC pulse is fed back directly to the modulator input, and therefore input referred. Any error in the DAC feedback waveform will appear in the spectrum of the quantizer output and is not noise-shaped by the loop mechanism. Ideally, the lower bound of the modulator input range is determined by the magnitude of the noise-shaped in-band quantization noise, but in practical designs, asymmetric DAC feedback pulses, extra loop delay, clock jitter and quantizer metastability can all fill the noise notch with white noise. These non-idealities result in a reduced DR by limiting the minimum convertible input signal. The effects are further exacerbated as clock rates and conversion bandwidths pushed ever higher. In this chapter, we will explore some of these problems in the context of high speed CT implementation.

4.1 Asymmetric DAC Feedback Pulses

A well-known type of non-idealities in a CT ΣΔ modulator is asymmetry between the positive and negative DAC feedback pulses. This problem arises where the

rising edge of the DAC pulse has a different transition time from its falling edge. The inequality in DAC pulse rise and fall time will cause inter-symbol interferences [33].

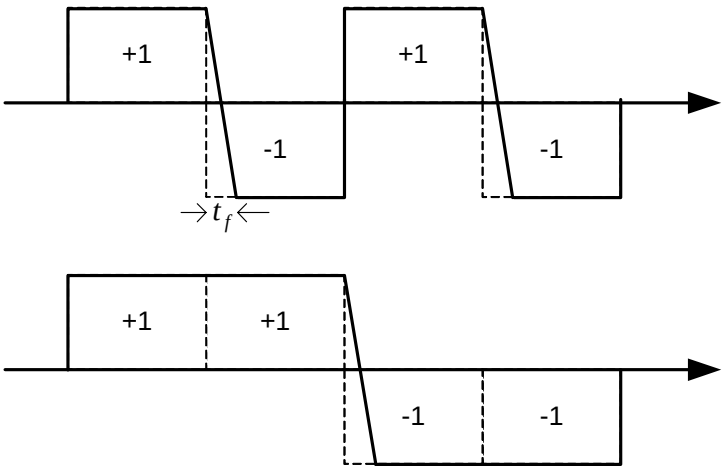

Figure 4.1 DAC feedback pulse with waveform asymmetry

Consider a case where the rising edge is steeper than the falling edge. For illustration purpose, we assume the DAC pulse has a rise time of zero, $t_r = 0$, while it takes t_f to transit on the falling edge. Because the charges transferred during the transition intervals do not balance out, a sequence of output pattern [1,-1, 1,-1] will have a different energy content from a pattern of [1, 1,-1,-1], as exemplified in Figure 4.1. Ideally, the ordering of the same set of bit sequence should not have any effects on the overall energy integrated. However, when there is a difference between rise and fall time, the energy does change. This kind of signal dependent imbalance will cause distortions and results in raised noise floor that is above the quantization noise.

Waveform asymmetry and the consequent inter-symbol interference can be reduced if we can shorten the transition intervals and match the transition edges, but this is never easy to realize, especially at higher sampling frequencies. One remedy is to use RZ DAC feedbacks rather than the NRZ waveforms (Figure 3.10). By resetting each feedback pulse for a fraction of the sampling period, all pulses have both a positive and a

negative edge. Thus the signal dependence of the mismatch is dismissed. However, RTZ DACs may still be desirable in some situation. In these cases, we can resort to the usage of differential circuitry rather than single-ended structure. Even if the individual waveforms are asymmetric, the properly balanced differential circuitry will still produce inherently symmetric waveforms.

These reasons explain in part why the differential structure is adopted in the design of this project.

4.2 Extra Loop Delay

Ideally, the DAC feedbacks should respond immediately to the quantizer clock edge. However, in practice, a real quantizer can not make a decision instantaneously. It needs some time to switch the transistors in the latches. Further more, the DACs also incur some delay. Because of the nonzero switching time of the transistors in the feedback path, the change in output bit as seen at the feedback point in the modulator happens only after the sampling clock edge. The total time interval between the sampling clock edge at the quantizer and the beginning of DAC output pulse is what we call the extra loop delay [34].

The extra loop delay is something unique to CT modulators. It does not exist in DT $\Sigma\Delta$ modulators and perhaps the closest analog in DT designs is incomplete settling. In a DT $\Sigma\Delta$ modulator, if the comparator can settle into a result and has the DAC finish transferring the charges all within one clock cycle, the integrator output is ready for ADC at the end of the clock cycle. However, for a CT implementation, the integrators in a low-pass modulator require a full clock cycle to integrate the DAC output. The error or delay in the DAC feedback waveform will cause an error or delay in output results of the integrators.

The extra loop delay has the effect of shifting the DAC pulse by some amount of time τ as illustrated by Figure 4.2. This is significant in the CT modulator design, since it alters the equivalence between the CT and DT representations of the loop filter, as we shall see in the following example.

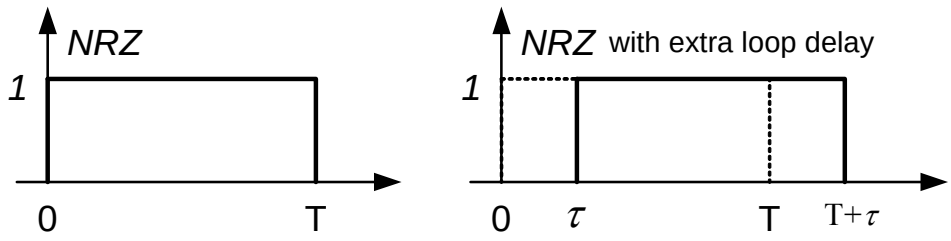

Figure 4.2 The effect of extra loop delay on DAC pulses

In Section 3.4.1, we have found the equivalent CT modulator

$$H(s) = -\frac{1+1.5s}{s^2} \tag{4.1}$$

for the DT low pass prototype

$$H(z) = \frac{-2z+1}{(z-1)^2} \tag{4.2}$$

assuming an NRZ DAC pulse with $(\alpha, \beta) = (0,1)$,

$$r(t) = \begin{cases} 1, & \alpha T < t < \beta T, \ 0 \le \alpha < \beta \le 1 \\ 0, & otherwise \end{cases} \tag{4.3}$$

But in reality, the DAC pulse lags behind by $\rho = \frac{\tau}{T}$ due to the extra loop delay, and the pulse lasts between $(\alpha, \beta) = (\rho, 1+\rho)$. If we continue to use the CT filter in such a system with extra loop delay, it will no longer have the noise shaping properties as we have expected. To find the DT equivalent to which the system actually corresponds, we regard the DAC pulse as a combination of a pulse between $(\alpha, \beta) = (\rho, 1)$ and a one-sample-delayed pulse between $(\alpha, \beta) = (0, \rho)$. This is because the transformations

discussed in Section 3.4.1 can only work with $0 \le \alpha < \beta \le 1$. Applying the CT-to-DT transformation to (4.1) for $(\alpha, \beta) = (\rho, 1)$ and $(\alpha, \beta) = (0, \rho)$ respectively, we get $H_1(z)$ and $H_2(z)$. After combining them together $H_\tau(z) = H_1(z) + z^{-1} \bullet H_2(z)$, we get the equivalent DT modulator the system has actually implemented:

$$H_\tau(z) = \frac{(-2 + 2.5\rho - 0.5\rho^2)z^2 + (1 - 4\rho + \rho^2)z + (1.5\rho - 0.5\rho^2)}{z(z-1)^2} \qquad (4.4)$$

where $\rho = \frac{\tau}{T}$. As we can see, only when $\rho = 0$, Eq. (4.4) turns into Eq. (4.2).

It is obvious from above, if the delay is not accounted for in the design process, the mapping between continuous and discrete domains will no longer be preserved, and the modulator suffers in both the in-band noise and maximum stable input amplitude, leading to a reduction in the dynamic range. Eq. (4.4) also shows us another problem caused by the extra loop delay. If in any CT modulator, the delay causes the DAC pulse to extend beyond the sampling period, i.e. $\beta > 1$, the order of the equivalent DT loop filter increases by one. This implies the stability of the modulator will worsen with increased delay. Detailed analysis of the effects on CT modulators can be found in [35]. It was shown that the detrimental effect on dynamic range was severe even for a fraction (40%) of the sampling period, and a loop delay of 65% was sufficient to make the modulator completely unstable, thus incapable to work properly. On the other hand, it is also found [35] that an optimal tuning of the feedback parameters can still greatly mitigate the performance loss due to loop delay. But the design of an on-chip tuning algorithm to maximize the DR is yet another problem to be addressed.

Consequently, it is imperative to recognize the presence of excess delay in a high speed design. If we know exactly what the loop delay τ is, by taking it into account in the actual DAC pulse (α, β), we can obtain the feedback coefficients to get exactly the

equivalent $H(z)$ we want. As we have noted, extending the DAC pulse to the next sampling period will cause the modulator order to increase by one. This implies the equivalent $H(z)$ will only retain its order for extra loop delay $\rho \le 1-\beta$ (if we use a pulse with $\beta < 1$). It also suggests that NRZ pulses $(\alpha, \beta) = (0,1)$ should be avoided in the design. Otherwise there will be one more coefficient in the numerator of the equivalent $H(z)$, necessitating an additional feedback to compensate for the added degree of freedom.

4.3 Clock Jitter

Clock jitter is another major non-ideality for CT ΣΔ modulators, which causes timing uncertainty (Figure 4.3). Even in a DT design, clock jitter is problematic, because it results in inaccurate sampling and is thus critical in dealing with fast changing input. The situation for CT ΣΔ modulators is worse. The sampling occurs at the quantizer instead of the modulator input, meaning the jitter affects both the input and quantization noise. Thus CT designs are more sensitive to clock jitter than DT modulators. For systems with higher order or higher center frequency, the likelihood of being clock jitter limited increases [36].

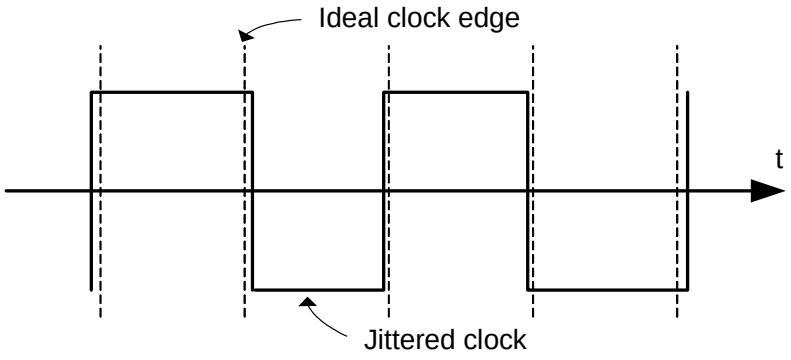

Figure 4.3 Waveform of a jittered clock

The errors in clock edges vary the DAC feedback with regard to the pulse delay and the pulse width. The effect of clock jitter is like adding a random phase modulation to the modulator feedback signal. This causes noise outside the signal band to fold into the band of interests to fill the noise notch, raising the noise floor, and hence degrades converter resolution. Figure 4.4 shows the effect of clock jitter on the output spectrum [37], for a fourth order bandpass modulator with noise notch at $f_S / 4$. It is obvious that with increased standard deviation σ_β of the clock jitter, more white noise is added to the output spectrum.

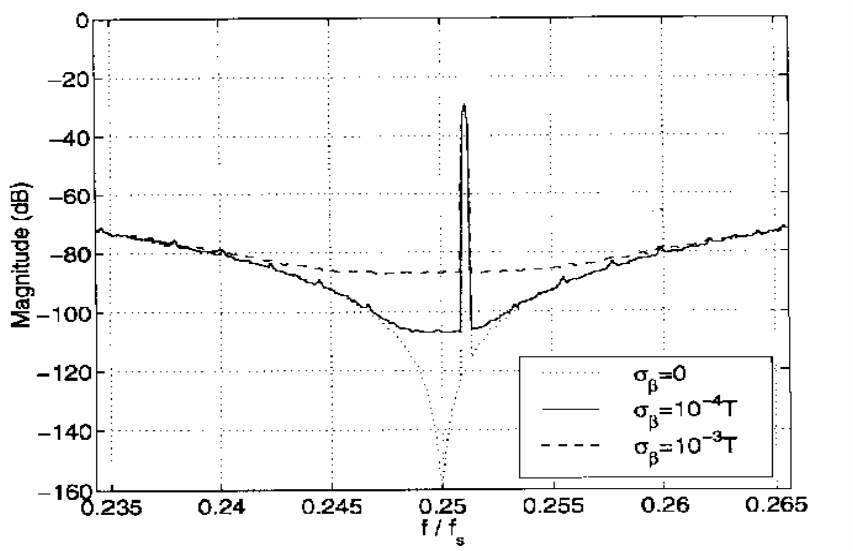

Figure 4.4 Effect of clock jitter on output spectrum

Clock jitter is difficult to combat, as there is little a designer can do to cope with it in CT $\Sigma\Delta$ modulators. Even the choice of DAC pulses does not help. RZ pulses are no better than NRZ DACs because the falling edge is subject to jitter in the same way the rising edge is. At the moment, the best way to minimize jitter effects seems to be using a low-jitter or low phase-noise crystal oscillator for clock generation. Careful layout technique is also preferred to avoid substrate coupling.

Luckily, it was shown [37] that the quality of a typical integrated VCO is good enough and is unlikely to be the limiting factor of modulator performance. For a VCO-clocked modulator with a typical phase noise specification, the maximum achievable DR was derived in [37] as

$$DR_{\max}(bit) \approx 19 - 0.5\log_2 f_N \tag{4.5}$$

where f_N is the Nyquist rate in megahertz. For a desired conversion bandwidth of 32MHz, $f_N = 64MHz$, and the DR is limited to around 16 bits, which is already far beyond the resolution any published high-speed modulator has achieved.

4.4 Signal-Dependent Timing Jitter

Even though the clock jitter is yet not problematic enough to be a performance limiting non-ideality, another kind of timing uncertainty turns out to be critical. There still exists a variation in the timing of DAC pulses, even with an ideal sampling clock.

Ideally, the quantizer will take a fixed amount of time to make a decision on its input. However, a practical quantizer has a circuit with finite regeneration gain. It takes longer time to resolve inputs close to zero volts than larger input signals. Loop delay in a real circuit is thus dependent on the magnitude of the quantizer input. This input dependent delay is actually a manifestation of the metastability problem in digital latches [38].

Figure 4.5 shows the loop delay against input magnitude $|V_{in}|$ for a practical quantizer. If inputs are large enough, there is only a fixed extra loop delay τ, which we have already discussed in Section 4.2. As the input gets smaller, the metastability problem sets in, and it takes longer to resolve the signal. When the input gets so small ($< V_{min}$) that the quantizer sometimes can not determine its input, no change will be made to the output bit, an effect sometimes referred to as hysteresis.

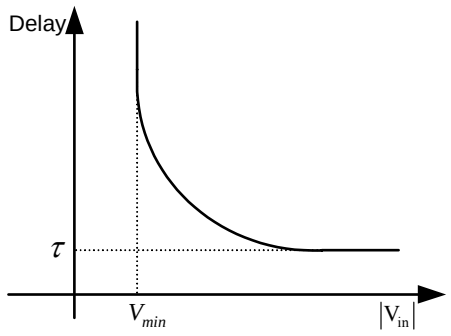

Figure 4.5 Quantizer characteristics

Metastability problem affects the system performance in two aspects. First, because the quantizer inputs close to zero occur at times that appear random, a random variation in the timing of DAC pulses will be introduced, adding wideband white noise to the output spectrum and degrading the modulator's dynamic range, in a quite similar way the clock jitter does (Figure 4.4). Second, quantizer metastability can result in worsened sensitivity to small input levels due to hysteresis. At low input amplitudes, there is a behavior of output limit cycles observed [37], preventing the modulator from encoding properly. All these effects combine to result in the modulator's poor SNR.

There are several approaches we can take to overcome the performance penalties imposed by quantizer metastability.

The first and the most fundamental way is to reduce the regeneration time of the quantizer latches, so that the quantizer has stronger capability to resolve small signals. However, circuit constraints will ultimately limit the achievable quantizer gain.

It seems more reasonable to enlarge the input standard deviation, reducing the probability of the quantizer input being too close to zero. In general, it is beneficial to have a larger quantizer input span under working condition. The range can be increased by choosing larger feedback currents. Alternatively, a preamplifier can be added immediately prior to the quantizer. However, a preamplifier that can work at such high

speed requires quite large gain-bandwidth, which is difficult to be designed, and inserting such a gain stage will also introduce more undesirable extra loop delay.

One more thing we can try is to add more latching stages to the end of the quantizer. By clocking the stages on an opposite clock phase from their previous, each latch gives the quantizer additional time of half a sample to settle. On the other hand, each stage also adds a loop delay of half a period to the system, which is detrimental to stability and DR (Section 4.2). However, this delay is a problem somehow we can overcome with a modified modulator structure.

Recall the bandpass CT modulator in Figure 3.9, which has an equivalent DT loop filter of Eq. (3.19), repeated here as

$$H_{BP}(z) = \frac{2z^2+1}{(z^2+1)^2} = \frac{2z^{-2}+z^{-4}}{(1+z^{-2})^2} = \frac{z^{-2}\cdot(2+z^{-2})}{(1+z^{-2})^2} \tag{4.6}$$

The loop filter has two-sample delay z^{-2} in the numerator. This implies we can place a full sample delay z^{-1} in the feedback path. Put Eq. (4.6) in another way:

$$H_{BP}(z) = z^{-1}\cdot\frac{(2z^{-1}+z^{-3})}{(1+z^{-2})^2} = z^{-1}\cdot\tilde{H}_{BP}(z) \tag{4.7}$$

where $\tilde{H}_{BP}(z) = \dfrac{2z^{-1}+z^{-3}}{(1+z^{-2})^2}$, we get the modified structure of Figure 4.6. The z^{-1} allows us to add two half-latch stages to combat the metastability effects.

With only a minor modification to the Matlab code in Appendix A — replacing the last line with

```
a = matrix\[2;0;1;0]
```

we can get the DAC feedback coefficients for $\tilde{H}_{BP}(z)$

$$(a1,\ a2,\ a3,\ a4) = (-0.9957,\ 4.6927,\ -1.1107,\ 2.6815) \tag{4.8}$$

The details of the calculation method can be found in Section 3.4.3.

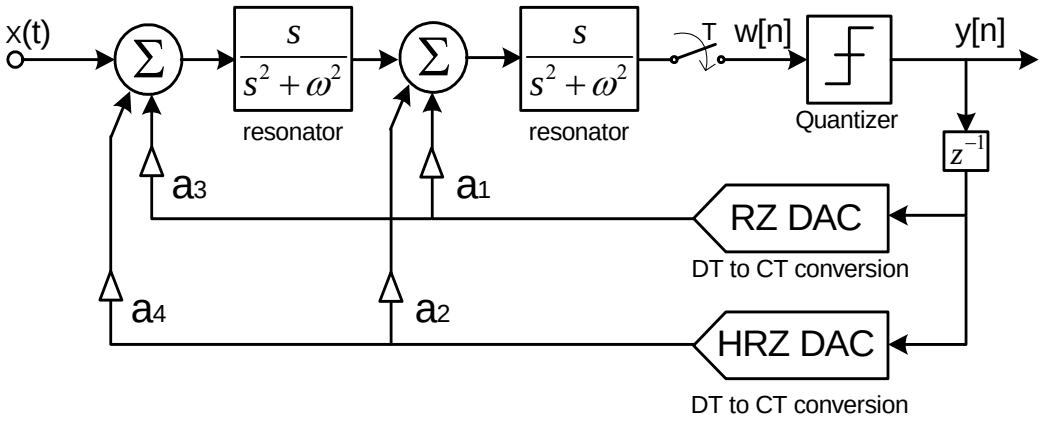

Figure 4.6 Modified multi-feedback structure for bandpass CT ΣΔ modulators

4.5 Summary

The effects of certain fundamental non-idealities are explored in this chapter. We examine how asymmetric DAC feedback, extra loop delay, clock jitter and quantizer metastability affect the performance of a CT ΣΔ modulator. As clock speed increases, all these effects tend to become more severe and have to be tackled with. Remedies to mitigate these effects are discussed. A modified multi-feedback structure for bandpass CT ΣΔ modulators is also explained to reduce adverse metastability effects.

CHAPTER 5

CIRCUIT TOPOLOGY AND MODULATOR IMPLEMENTATION

We have discussed the methodology of CT modulator designs in Chapter 3. Here, we will focus on the practical designs of the circuit topology and implementation details of the high-speed CT bandpass ΣΔ modulator. The modulator is implemented in a 0.35μm triple-metal standard CMOS technology and is based on two on-chip parallel LC tanks as resonators. It is expected that the modulator is capable of being clocked at 1-GHz for conversion of bandpass signals centered on 250 MHz.

5.1 Resonators

In order for the modulator to operate successfully on the expected 250MHz centered RF/IF signals, the availability of resonators capable of working at such a high speed is a prerequisite.

One plausible choice is to use active circuitry based on the transconductor-capacitor (Gm-C) technique [39], which is quite suitable to be integrated on-chip. However, such active resonators have a low dynamic range and they are also quite susceptible to the non-idealities in the transconductors. The enormously stringent requirements on the transconductors are further complicated by the targeted high speed.

As a result, passive LC resonators, which are based on the parallel connection of an inductor and capacitor pair (Figure 5.1), are utilized instead. However, on-chip spiral

inductors is typically small in Q (Q<10) [40]. The parasitic has to be taken into consideration for a proper design, and negative resistance circuits can be used to increase the effective Q [41].

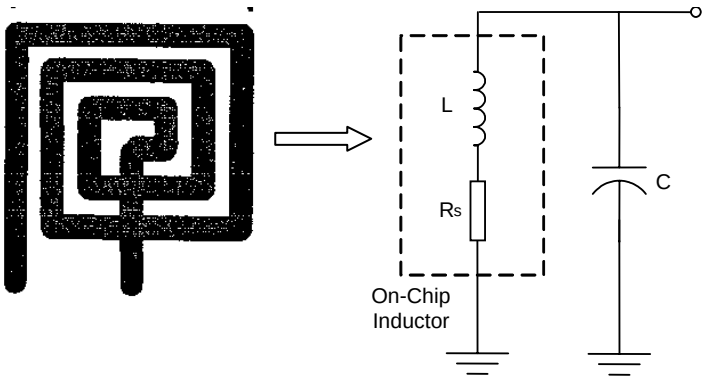

Figure 5.1 Passive LC resonator

A complete characterization of an on-chip inductor for circuit design consideration generally requires developing a lumped-element equivalent circuit from the physical layout, to model the finite inductor Q and self resonance effects. The inductance of spirals in silicon technology is quite similar to that of an inductor working in free space and the finite Q is primarily a result of the series resistance which can be estimated from the spiral dimension, trace width and number of turns, etc. [42].

Table 5.1 lists the major parameters of the on-chip inductor. With SPICE simulation models [43] similar to that of [44], AC analysis of the lumped equivalent circuits shows the inductor's characteristics in Figure 5.2 and Figure 5.3. It has a nominal value slightly above 40nH at the frequency of 250MHz with its self-resonant frequency at about 1.1GHz. Obviously from the curves, the inductor has a quite low quality factor which is even smaller than 3. The parasitic resistance R_S is significant and can not be neglected in the resonator design (Figure 5.1). This resistance is relatively frequency-independent in the interested range around 250MHz with a value of 41.74Ω.

Table 5.1 Parameters for the on-chip inductor design

Conductor layer	Metal 3
Shunting layer	Metal 1
Number of turns	8
Side length (μm)	500.0
Conductor width (μm)	12.4
Conductor spacing (μm)	1.2

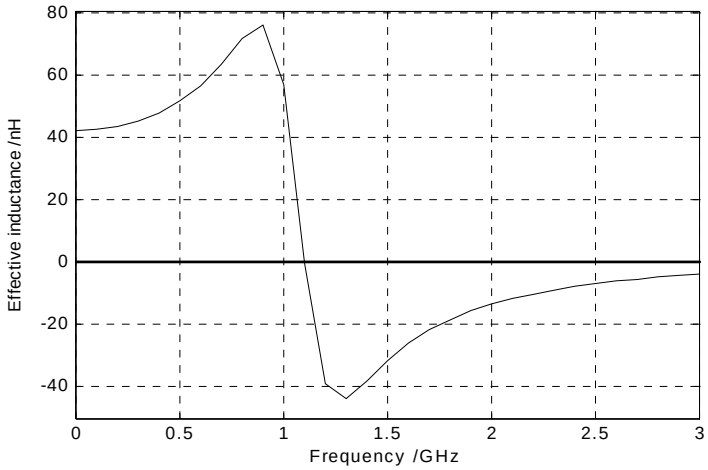

Figure 5.2 Effective inductance against frequency

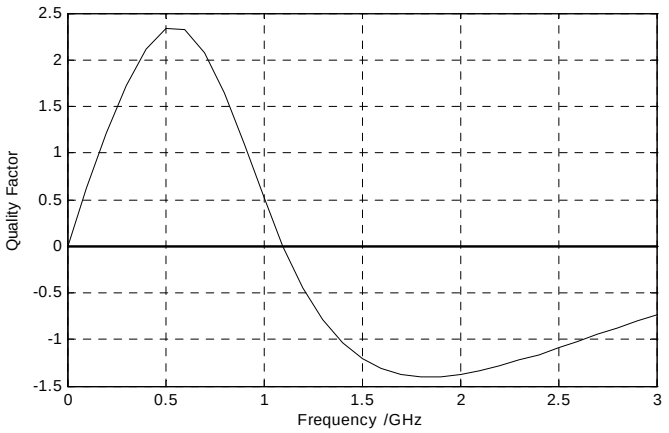

Figure 5.3 Inductor quality factor versus frequency

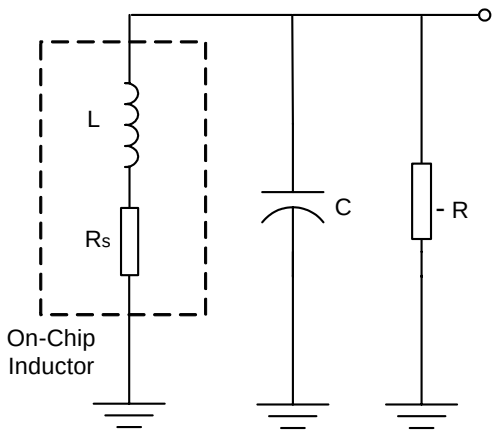

Figure 5.4 Compensation of the parasitic resistance

To offset the losses in the low-Q inductors' parasitic resistance, negative resistors –R are connected in parallel with the LC tanks (Figure 5.4). The equivalent resistance of the overall resonator structure is

$$Z_{eq} = \frac{1}{\frac{1}{sL+R_s} + sC + \frac{1}{-R}} = \frac{\frac{1}{C}s + \frac{R_s}{LC}}{s^2 + s(\frac{R_s}{L} - \frac{1}{CR}) + \frac{1}{LC}(1 - \frac{R_s}{R})} \tag{5.1}$$

The negative resister R can be implemented by a transconductor, which is capable of being tuned to make the s term coefficient in the denominator equal to zero.

$$R = \frac{L}{CR_s} \tag{5.2}$$

When $R_S \ll R$, Eq. (5.1) is simplified to the form of $\frac{As+B}{s^2+\omega^2}$. As we can see, the resonators we actually implemented have a low pass term in the numerator, instead of being purely bandpass we have assumed in Figure 3.9. The center frequency of the biquadratic transfer function is found to be

$$\omega_0 = \sqrt{\frac{1}{LC}(1 - \frac{R_s}{R})} = \sqrt{\frac{1}{LC} - \frac{R_s^2}{L^2}} \tag{5.3}$$

which means the capacitance C of the LC tank should be adjusted to

$$C = \frac{1}{L\omega_0^2 + R_S^2 / L} \tag{5.4}$$

for a predetermined center frequency of ϖ_0. In our case, the on-chip inductor is connected between the differential output nodes, so the single-ended equivalents is $L = \frac{40nH}{2} = 20nH$ and $R_s = \frac{41.74\Omega}{2} = 20.87\Omega$. This results in a capacitor of $C = 14.06\,pF$ for an expected $\omega_0 \approx 250MHz$. To compensate for the parasitic resistance, a transconductor of $G = \frac{1}{R} = 14.67mA/V$ results from Eq. (5.2). The component values are listed collectively in Table 5.2.

Table 5.2 Component values for Figure 5.4

Component	Value
Integrated inductance (nH)	40.00
Parasitic resistance of on-chip inductor(Ω)	41.74
Resonator capacitor C (pF)	14.06
Compensation transconductor $G = \frac{1}{R}$ (mA/V)	14.67

5.2 System Level Architecture

We expect the continuous-time modulator to have noise shaping properties of an equivalent 4th-order bandpass DT design. By starting with the DT prototype of

$$H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{(1 - z^{-2})^2} == z^{-1} \cdot \frac{2z^{-1} + z^{-3}}{(1 - z^{-2})^2} \tag{5.5}$$

and applying the design methods described in Chapter 3, we arrive at the system level structure shown in Figure 5.5.

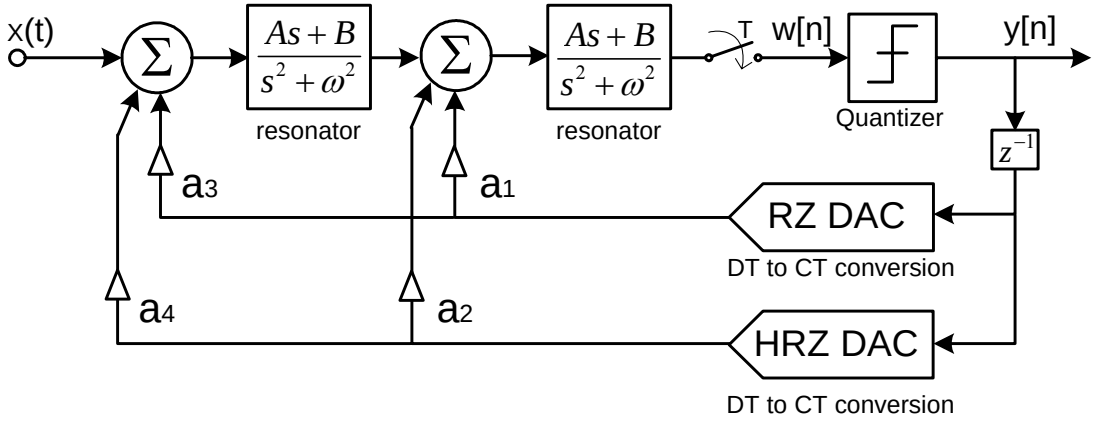

Figure 5.5 Overall system level structure

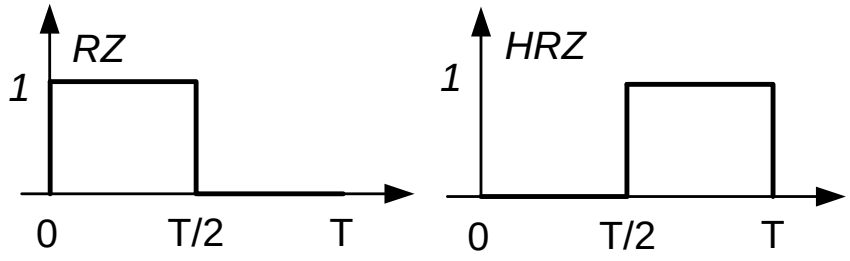

Figure 5.6 DAC pulses for feedbacks

Table 5.3 Calculated coefficients for Figure 5.5

Coefficient	Value	Coefficient	Value
A	7.11E-2	a2	1.59
B	7.42E-2	a3	1.99E+1
a1	8.71E-1	a4	1.50E-1

In Figure 5.5, the representation of the resonators is based on the practical design which was discussed in last section. To maintain full controllability of the CT modulator, a multi-feedback structure is adopted and is reminiscent of Figure 3.9 in style. To remedy the metastability effects which we have discussed in depth in last chapter, we

split the DT prototype $H_{BP}(z)$ into two parts: z^{-1} and $\frac{2z^{-1}+z^{-3}}{(1+z^{-2})^2}$, as shown in Eq. (5.5). The extracted z^{-1} will allow us to insert two additional latch stages in actual circuit implementation, which provide the quantizer circuit more regeneration time to resolve the quantizer input, mitigating the signal dependent timing jitter (the so-called metastability). Then, coefficients ($a1$, $a2$, $a3$, $a4$) of DAC feedbacks are calculated for the other part: $\frac{2z^{-1}+z^{-3}}{(1+z^{-2})^2}$ based on the chosen DAC pulses (Details about calculation of the feedback coefficients are referred to Section 3.4.3 and Appendix A). Both RZ and HRZ waveforms are selected for the feedback DAC pulses (Figure 5.6, repeated from Figure 3.10). The coefficients for the ideal model in Figure 5.5 are calculated and listed in Table 5.3 (in practical implementation, the coefficients of ($a1$, $a2$, $a3$, $a4$) need to be derived from the actual feedback waveforms and may be different from the ones listed).

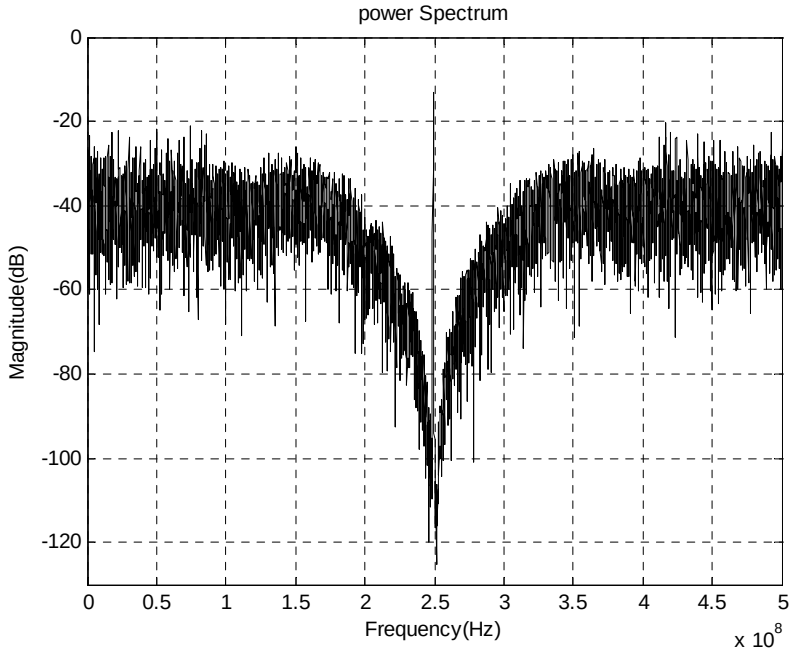

Figure 5.7 Output spectrum of the system level simulation

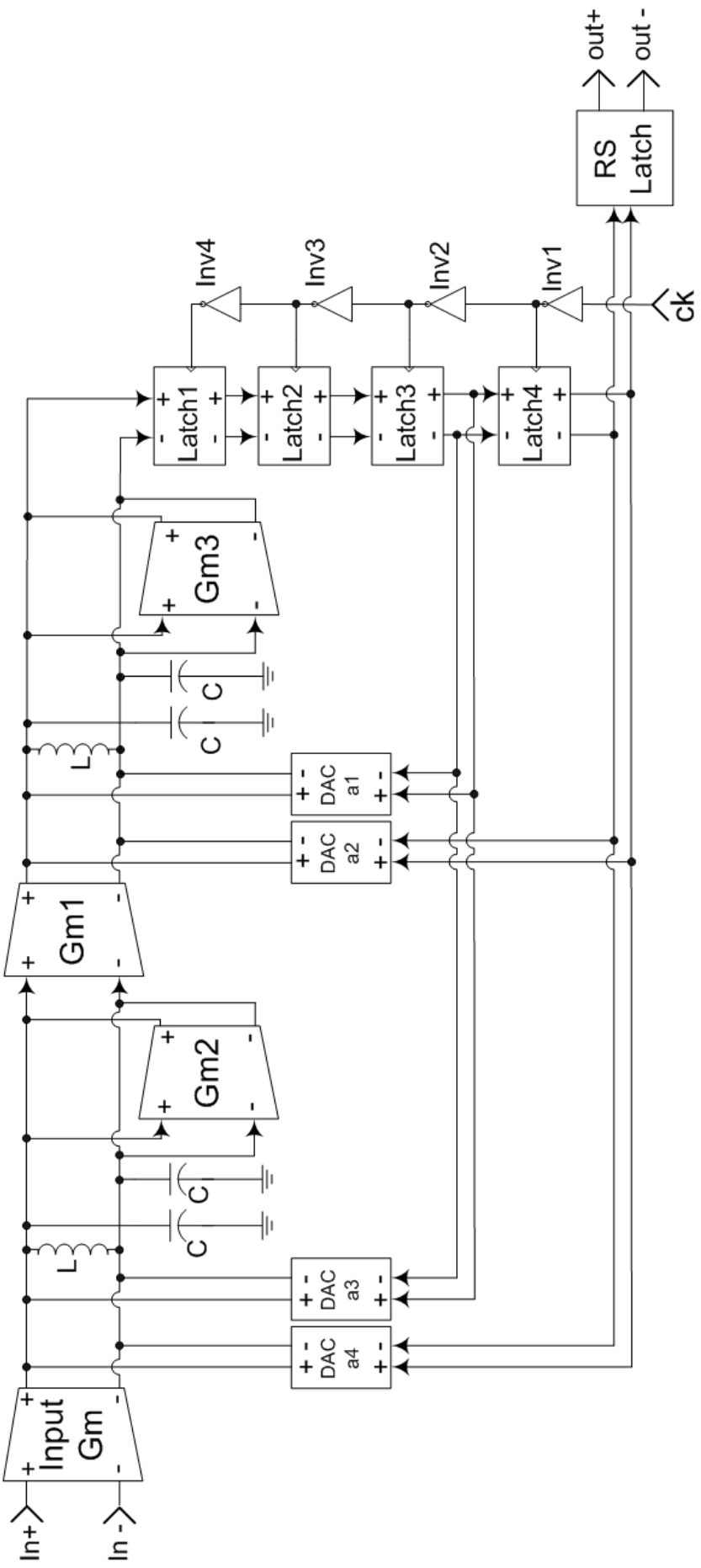

Figure 5.8 Overall circuit level structure

A behavioral simulation of the system model in Matlab's Simulink tool demonstrates that such architecture is viable. Figure 5.7 shows the power spectrum of the simulated output. The system has a sampling clock of 1GHz and the input signal is located at 249MHz with amplitude of 0.24. As we can see from the result, the quantization noise is shaped away from the interested signal band around $f_s / 4$.

5.3 Overall Circuit Level Structure

Based on the system level design in Figure 5.5, the circuit structure is determined (Figure 5.8). It is implemented in a fully differential style, for noise rejection and to avoid the negative effects of inter-symbol interferences (discussed in Section 4.1).

The input Gm and $Gm1$ are used to do the voltage-to-current conversion so that signal feedbacks can be done by simply summing in the current domain. The transconductors of $Gm2$ and $Gm3$ are acting as negative resistors. They are tuned to compensate for the parasitic resistance of the low-Q inductors L. The series connection of two second-order LC resonators yields a fourth order modulator. In the circuit level design, the sampler, quantizer and one-digital-delay z^{-1}, as well as the RZ and HRZ DACs in Figure 5.5 are combined together and implemented in a latching scheme by four identically structured latches (Latch1 to Latch 4).

The block diagram of the latching scheme is shown in Figure 5.9 with a single-ended model for simplicity. Each latch has a RZ output response. Latch1 serves as the sampler and one-bit quantizer by resolving its input polarity at uniform intervals of one nano second. The following latches are clocked on the inverted clock phase from their previous stage so that they each provide a half-sample delay. In this way, the voltage outputs of Latch3 and Latch4 become one-digital-delayed RZ and one-digital-delayed HRZ waveforms (graph c and d in Figure 5.9) respectively. The inverter series

proves to be essential in the design, and its function is more than just inverting the clock signal. A delay in the clock signals is introduced by the inverter series. For high speed operation, such a delay is significant and can not be neglected. This delay caused by the inverter circuits provides the latches enough setup time before the output of their previous stages is reset to zero. On the other hand, it also makes the clock signals for Latch3 and Latch4 ahead of those for Latch1 and Latch2. The lead in timing allows compensation for the extra loop delay (refer to Section 4.2) in the feedback pulses. Appropriate tuning of the lead by adjusting the transistor sizing in the inverter series enables complete balance of the loop delay.

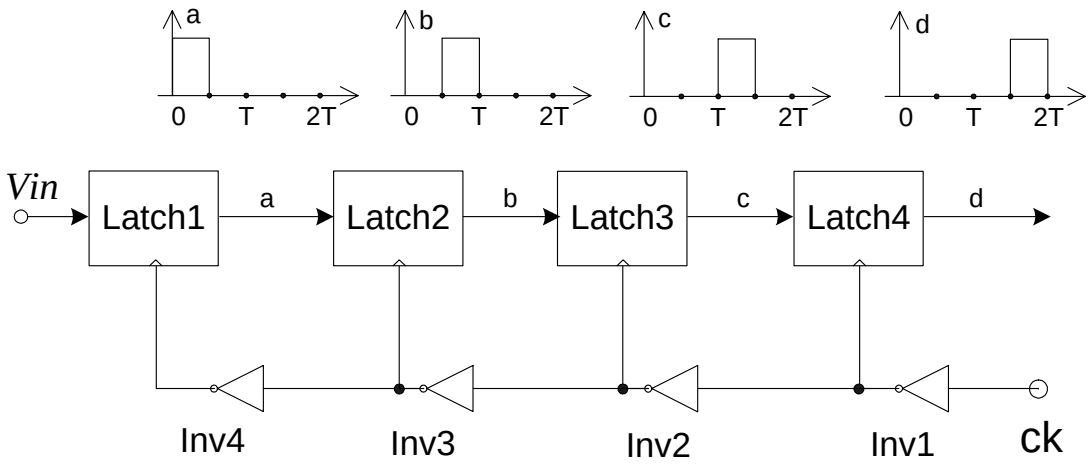

Figure 5.9 Latching scheme for generation of DAC pulses

The voltage outputs from Latch3 and Latch4, which have one-digital-delayed RZ and one-digital-delayed HRZ waveforms, are then fed back to the modulator by driving the DACs (a1 to a4). The DACs convert the voltage signals to currents for easy summing in current domain and they also provide a means to tune the feedback coefficients. The modulator's digital output is obtained from the RS latch driven by Latch3 or Latch4.

5.4 Circuit Blocks

With the overall circuit structure in mind, we now focus on the circuit design issues of the modulator's individual building blocks. The input transconductor and the output RS latch stage are actually outside the modulator loop, and they are individual stages that can be designed separately. For this reason, they are not included in the discussion of loop design.

5.4.1 Latches

As we have introduced in the overall circuit design, the four identically structured RZ latches combine in a latching scheme to realize the sampler, quantizer and one-digital-delay z^{-1}, as well as the RZ and HRZ pulse generators (Figure 5.9). Consequently, the design of the latches is critical and has significant impact on the overall circuit design. It must be sensitive enough to resolve small input signals. It also needs to operate fast enough to make a clock rate of 1GHz possible. The speed of the latches determines the fastest operational frequency of the modulator.

Figure 5.10 shows the circuit schematic of the latches. It is expected that the circuit output has a RZ waveform. During the first half clock cycle, the circuit amplifies the input voltage to a rail-to-rail status and during the other half period, both outputs are reset to a high voltage. In the following, we will explain how it works in detail.

In the reset phase when V_{CK} is low, the transistor M7 is cut off and the transistor pair of M5 and M6 is disabled. Both V_{out+} and V_{out-} will be pulled to the positive rail, Vdd!, by the shorting currents through M2 and M3. Both output signals are reset to a high voltage.

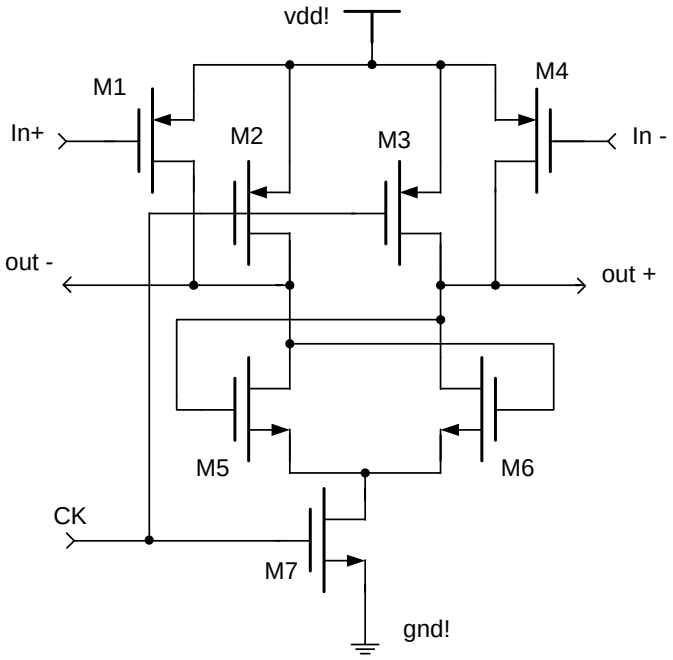

Figure 5.10 Schematic of the RZ latch

During the evaluation phase when V_{CK} is high, the transistor M7 is turned on and the cross coupled pair of M5 and M6 is enabled. On the other hand, M2 and M3 are cut off. Both V_{out+} and V_{out-} will begin to drop. If $V_{in+} > V_{in-}$, M4 allows more current to get through than M1. Hence the voltage of V_{out+} will drop at a lower rate than V_{out-}. This results in $V_{out+} > V_{out-}$. The voltage difference between V_{out+} and V_{out-} is then further amplified by the positive feedback among the cross coupled pair of M5 and M6. Eventually, V_{out+} is pulled back to the positive rail $Vdd!$ and V_{out-} is drawn to a voltage close to zero. For the case of $V_{in+} < V_{in-}$, a similar analysis can be done and is not repeated here.

The transient responses of the RZ latch in schematic simulation are shown in Figure 5.11 for an input pair of $V_{in+} = 1.7V$ and $V_{in-} = 1.4V$. It is obvious that the curves behave exactly in the way we have predicted. The circuit is tested under different input conditions, and it is shown that the latch can resolve an input difference as small as

$0.4mV$ when clocked at a rate of 1GHz. The latch may be clocked faster, but with the price of impairing its ability to resolve small signals.

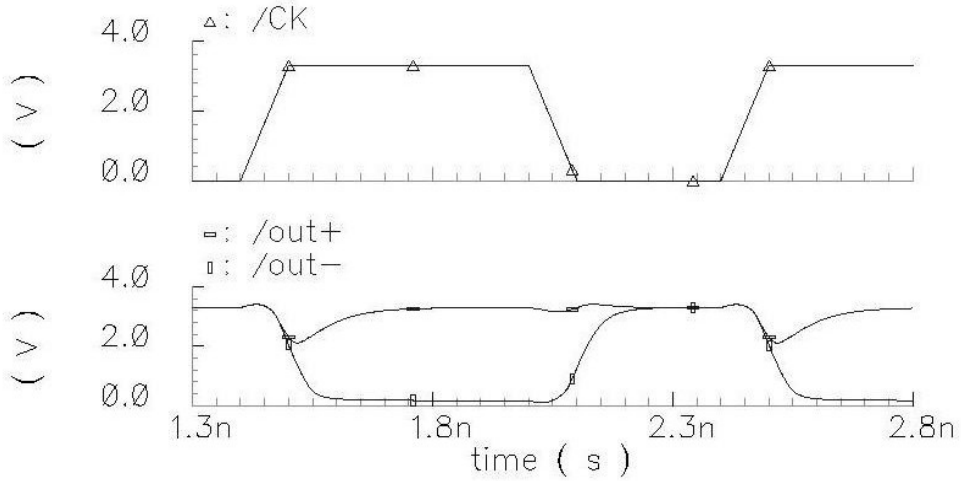

Figure 5.11 Transient response of the quantizer latch

The choice of the transistor sizes in the latch is somehow a balanced compromise. Large sizes of M2, M3 and M7 seem beneficial for the transistors to be quickly set on or off, but they also increase the capacitance loads on the clock signal. The sizes of M1, M4, M5 and M6 should be large enough to ensure quick response to the inputs, but their capacitance will reduce the speed of resetting operation.

Some special attention should be given to the design of Latch1 due to its delicate position in serving as the quantizer. Because it interacts directly with the voltage output of the LC resonator, its differential input is usually small, while the other latches are working with digital signals. Another fact is that the voltage swing at V_{out+} and V_{out-} is quite large, usually between $Vdd!$ and $gnd!$. Large signal glitches will be coupled back to the LC resonator's voltage output, through the parasitic capacitance within M1 and M4.

As a result, some special arrangements are made with Latch1. The size of its input transistor M1 and M4 is enlarged for higher sensitivity to small inputs. To further enhance Latch1's ability to resolve small signals, input and output buffers are also attached to reduce the parasitic influence from other stages (Figure 5.12). The buffers are implemented as simple source followers (Figure 5.13). The input source follower also serves to minimize crosstalk in the mixed signal system. It separates analog circuits from the switching functions in the digital domain.

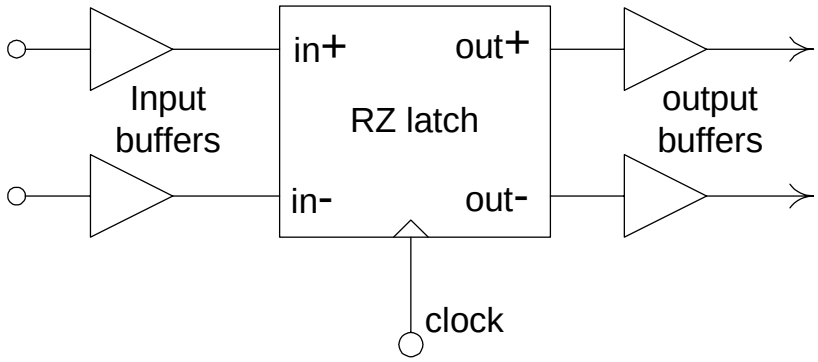

Figure 5.12 Special arrangement with Latch1

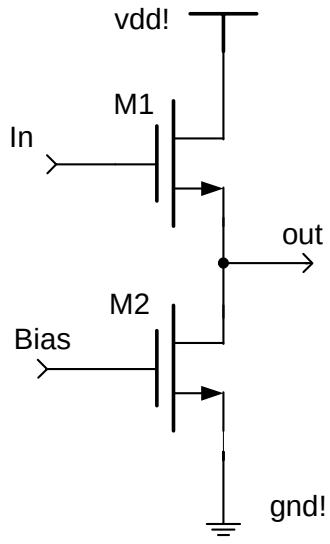

Figure 5.13 Source follower for Latch1 buffers

5.4.2 Feedback DACs

As we have introduced in the discussion of overall circuit structure (Figure 5.8), the output waveforms of Latch3 and Latch4 are fed back to the modulator by summing in the current domain. DACs of a1 to a4 serve to do the voltage-to-current conversion and they also provide a means to tune the feedback coefficients which is necessary for the CT modulator to maintain its equivalence with its DT prototype.

The DACs are implemented as simple tunable current switches. They are fully differential and the schematic of the current switch is shown in Figure 5.14. Driven by the digital voltage output of Latch3 or Latch4, the NMOS differential pair of M1 and M4 composes the core part of the switch. When $V_{in+} \neq V_{in-}$, one of the transistor is turned off and the current I_{in} goes completely through the other transistor. During the resetting period of the driving Latch3 or Latch4 when $V_{in+} = V_{in-} = vdd!$, the current I_{in} is shared equally among both paths. V_{bias} provides a means to control the current of I_{in}.

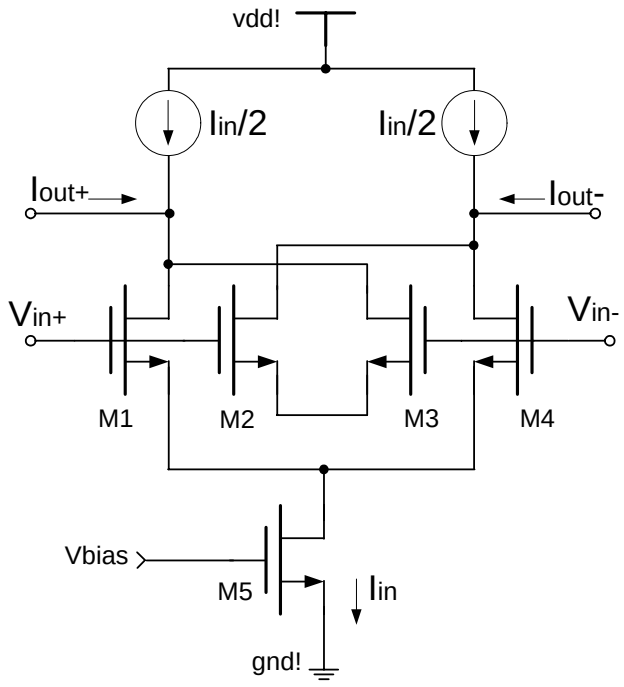

Figure 5.14 Schematic of the feedback current switch

Transistors M2 and M3 in Figure 5.14 are two dummy transistors for cancellation of the feed-through charges from the input gates. They have the same geometrical size as M1 and M4 to match their capacitance. The sources are connected together and floating, so that no channels are formed under their gates. M1 and M4 must be in either saturation region or cut-off region for complete cancellation.

However, due to the full swing signals at the voltage input V_{in+} or V_{in-}, large common-mode spikes are introduced in the output current I_{in+} and I_{in-} at each steep edge of the controlling signal, as shown in Figure 5.15. The main reason is the presence of stepping common-mode voltage at latch outputs right on the clock edges. Although differential current output ($I_{in+} - I_{in-}$) still maintains its square waveform, the large common-mode spikes in the feedback currents lead to excessive noise and error in the resonators of the system.

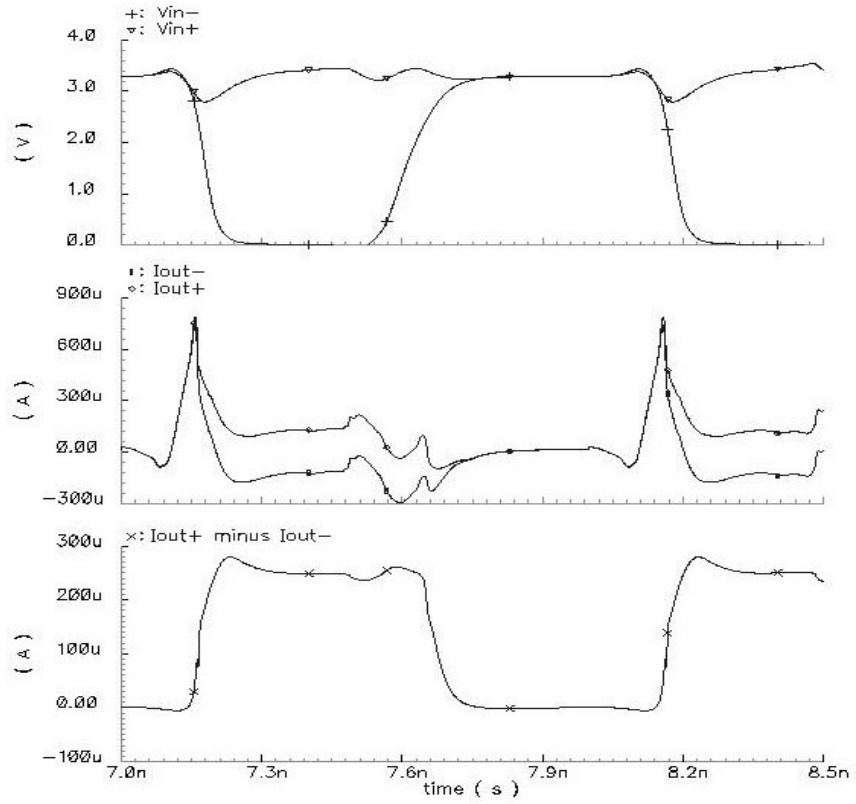

Figure 5.15 Transient response of the DAC current switch

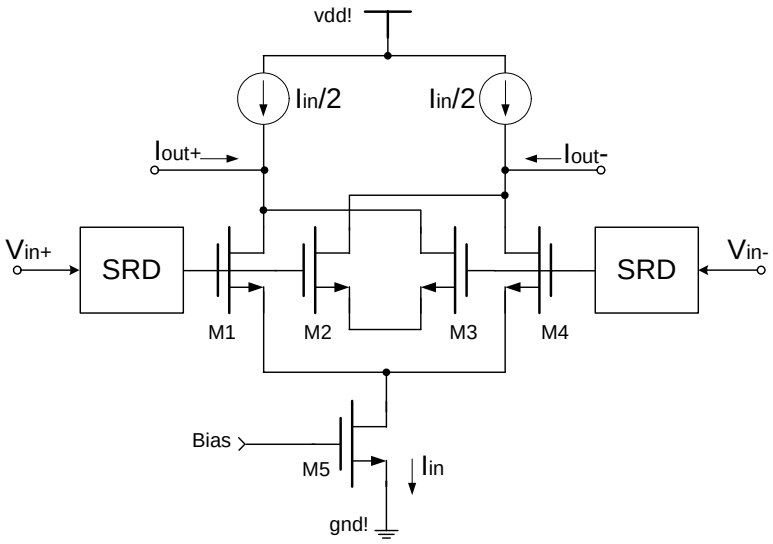

Figure 5.16 The use of SRDs for reducing current spikes

To reduce the common-mode current spikes, a scheme (Figure 5.16) was proposed in [45] to add a swing reduction driver (SRD) before each voltage input. With use of SRDs, the voltage swing on the gates of the switching transistors (M1 and M4) is adjusted to be just enough to fully turn on or turn off the transistors. By reducing the voltage swing, the charges being transferred to or from the transistor gates are minimized, and hence the common-mode current spikes are greatly attenuated. The use of SRD also improves the operation speed of the current switch by reducing the transistors' switching transition time.

The idea of using SRDs is effective, but the SRD circuit in [45] is not fast enough for a high speed operation of 1GHz. An innovated design of the SRD is shown in the diagram of Figure 5.17. The inverter composed of M1 and M2 determines whether M3 is turned on or off, and the inverter also removes the negative effects of voltage ripples in the input signal. M4 and M5 serve as resistors. When V_{in} is high, M3 is turned off and it is not functioning. The output voltage is determined only by the aspect ratio of M4 and M5. When V_{in} is low, M3 is turned on in triode region. It serves as another resistor in parallel with the "resistor" M5 to lower the output voltage.

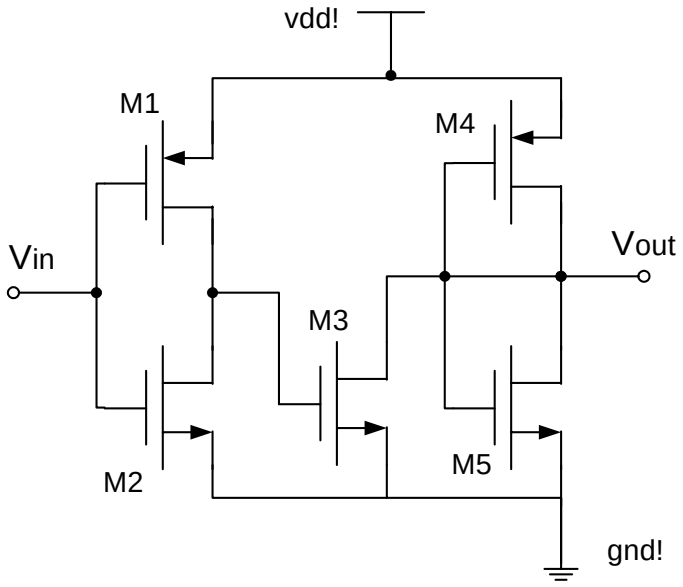

Figure 5.17 Schematic of the swing reduction driver

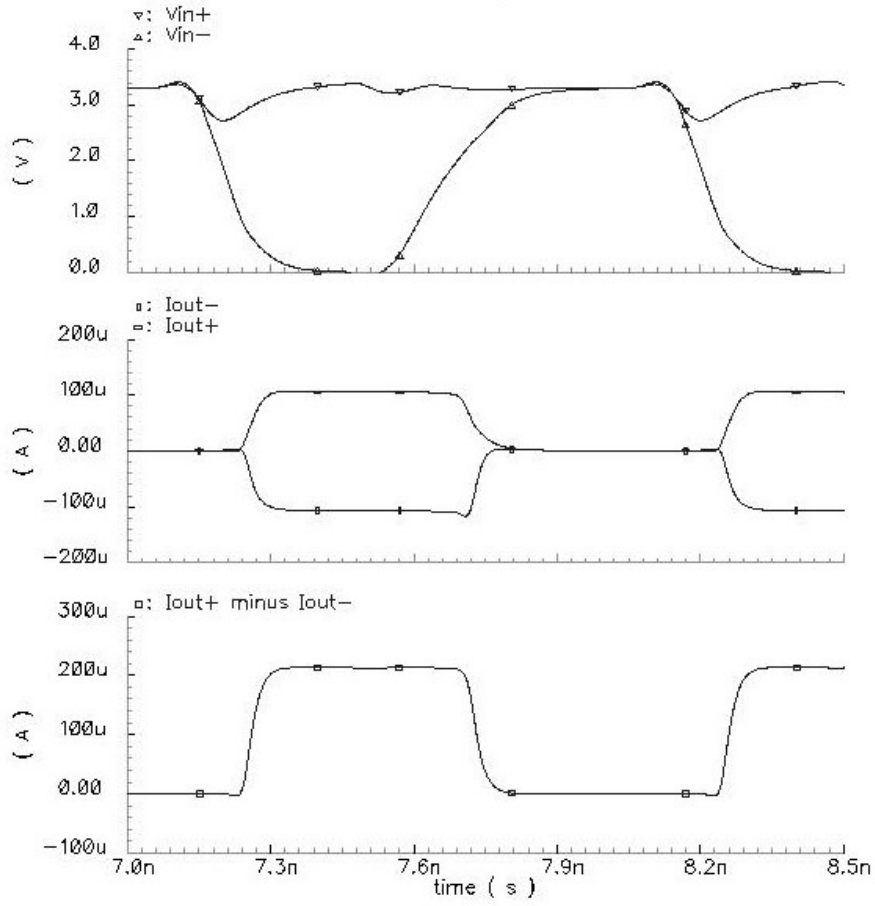

Figure 5.18 Transient response of the DAC current switch with SRDs inserted

In our design, the output voltage of the SRD is between 1.405V (when V_{in} is high) and 1.018V (when V_{in} is low). With SRD inserted to reduce the input swing, transient responses of the feedback current switch are shown in Figure 5.18. The improvement over the waveforms in Figure 5.15 is obvious. Not only are the common mode current spikes removed, a better square wave also results as the differential output.

Referring back to Figure 5.9, we expected the current feedback corresponding to Latch3 to be a one-sample-delayed RZ waveform that lasts from T to $3T/2$, and we also want the current feedback of Latch4 to hold between $3T/2$ and $2T$. But in practical implementation, there could be some minor deviation, which we should take into account.

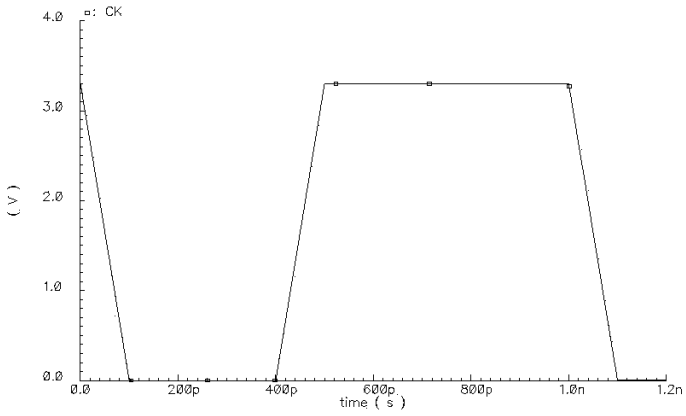

Figure 5.19 Clock waveform

With the system clocked by a 1GHz signal of the form in Figure 5.19, the current feedback from Latch3 lasts between $(\alpha, \beta) = (1,\ 1.688)$ after the sampling clock edge, and the Latch4 current feedback has $(\alpha, \beta) = (1.5,\ 1.973)$. Taking into consideration these actual feedback parameters, coefficients $(a1,\ a2,\ a3,\ a4)$ of DAC feedbacks are re-calculated for the equivalent DT system in Eq.(5.5), resulting:

$$(a1,\ a2,\ a3,\ a4) = (0.7702,\ 1.4521,\ 1.2605\frac{C}{Gm1},\ -0.3683\frac{C}{Gm1}) \qquad (5.6)$$

where C and Gm1 are the capacitor and transconductor in the system of Figure 5.8. The magnitude of feedback currents in the four paths ought to be in proportion with each other according Eq. (5.6), otherwise the system's equivalence with its DT prototype will be jeopardized. However, the absolute magnitude of these current feedbacks is not a major concern because it only affects the voltage swing of the LC tanks. As to the negative sign of $a4$ in Eq. (5.6), it simply means inverting the output connection of the current switch in that path.

5.4.3 Transconductors

In order for the system to work with narrow band signals centered on 250MHz, high-linearity transconductors suitable for very-high-frequencies is desirable. A transconductor based structure first proposed by Nauta [46] is adopted for the project. It has a very large bandwidth due to the absence of internal nodes, and is well suited for high speed operations up to gigahertz.

The transconductor [47] is based on two matched CMOS inverters. Consider a single inverter in Figure 5.20. When both MOS transistors are working in saturation region, the output current of the inverter can be written as:

$$I_{out} = I_2 - I_1 = \frac{\mu_n C_{ox} W_n}{2L_n}(V_{in} - V_{tn})^2 - \frac{\mu_p C_{ox} W_p}{2L_p}(V_{dd} - V_{in} - V_{tp})^2 \qquad (5.7)$$

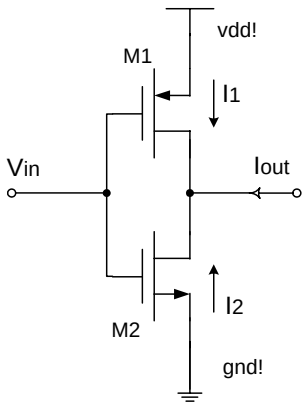

Figure 5.20 The inverter component for transconductors

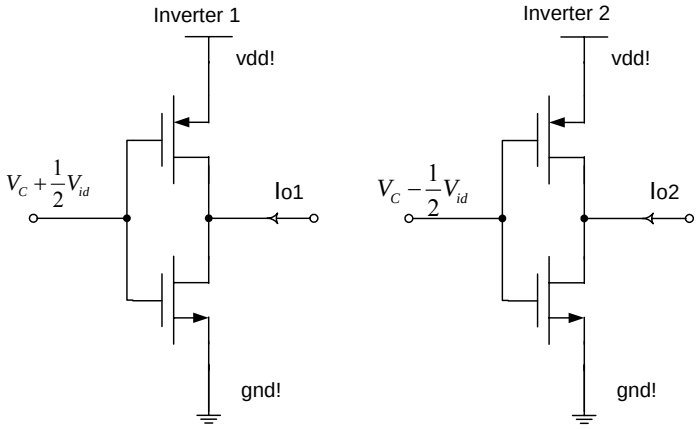

Figure 5.21 Two balanced inverters performing differential V/I conversion

With $\beta_n = \frac{\mu_n C_{ox} W_n}{L_n}$ and $\beta_p = \frac{\mu_p C_{ox} W_p}{L_p}$, Eq. (5.7) is simplified to the form of

$$I_{out} = a \cdot V_{in}^{\ 2} + b \cdot V_{in} + c \tag{5.8}$$

where $a = (\beta_n - \beta_p)/2$, $b = -\beta_n V_{tn} + \beta_p (V_{dd} - V_{tp})$ and $c = \frac{1}{2}\beta_n V_{tn}^{\ 2} - \frac{1}{2}\beta_p (V_{dd} - V_{tp})^2$.

For two matched inverters (Figure 5.21) driven by a differential input voltage V_{id} balanced around a common mode voltage of V_c, the differential output current can be calculated by subtraction:

$$I_O = I_{O1} - I_{O2} = 2a \cdot V_C V_{id} + b \cdot V_{id}$$

$$= V_{id} \cdot [\beta_n (V_C - V_{tn}) + \beta_p (V_{dd} - V_C - V_{tp})] = Gm \cdot V_{id} \tag{5.9}$$

where

$$Gm = \beta_n (V_C - V_{tn}) + \beta_p (V_{dd} - V_C - V_{tp}) \tag{5.10}$$

From Eq. (5.10), it can be concluded that the differential transconductance of *Gm* is linear even for nonlinear inverters ($\beta_n \neq \beta_p$), as long as the transistors are properly biased in the saturation region and the common-mode voltage V_C of the input is kept constant. As we can see from Eq. (5.10), *Gm* is dependent on the power supply to the

inverter. By controlling the source voltages of the PMOS transistors, we can fine tune the value of Gm.

In the project design (Figure 5.8), we combine the transconductors of $Gm1$ and $Gm3$, as well as the biasing circuits, into a single network as shown in Figure 5.22.

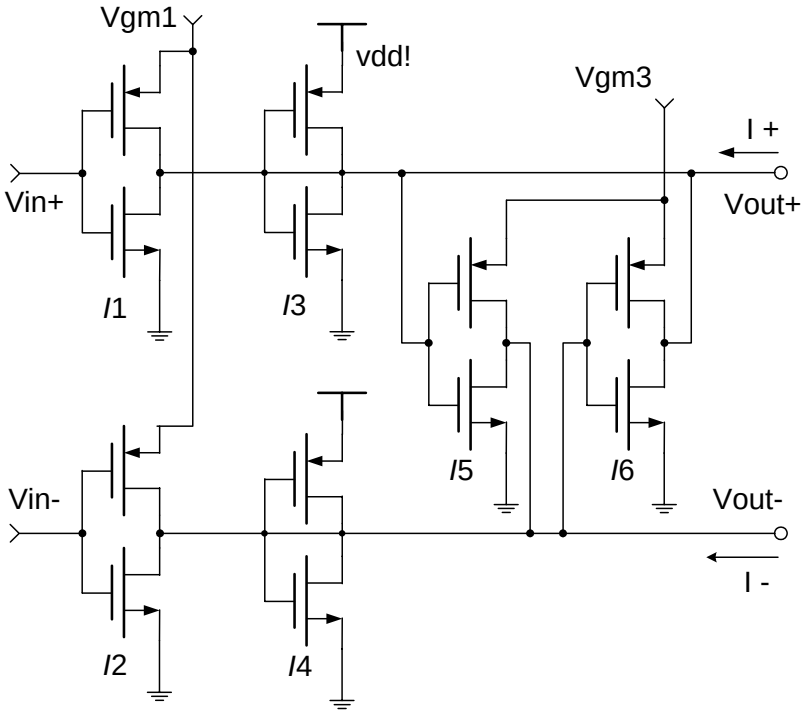

Figure 5.22 Transconductor network with biasing circuits

Inverters $I1$ and $I2$ work as the differential transconductor $Gm1$ and the inverter pair of $I5$ and $I6$ is equivalent to $Gm3$. We can adjust values of these transconductors by fine tuning the control voltages of V_{Gm1} and V_{Gm3}. It should be noted that the $Gm3$ is cross-connected between the two output nodes $Vout+$ and $Vout-$ to serve as a negative resister for differential changes in the output signal (recall in section 5.1 we need a negative resistor to compensate for the parasitic resistance of the low-Q inductor). $I3$ and $I4$ are shunted as resistors to bias the output voltages, which is necessary for transistors in $Gm1$ and $Gm3$ to operate in the saturation region. However, the positive load resistors introduced by $I3$ and $I4$ will compromise in part the

negative resistance realized by $Gm3$. The common-mode and differential load resistances at the nodes $Vout+$ and $Vout-$ are capitulated in Table 5.4.

Table 5.4 Common and differential load resistance on output nodes

Output node	Common-mode load resistance	Differential-mode load resistance
$Vout+$	$\frac{1}{Gm3+Gm6}$	$\frac{1}{Gm3-Gm6}$
$Vout-$	$\frac{1}{Gm4+Gm5}$	$\frac{1}{Gm4-Gm5}$

The same network can also be used for the design of input Gm , $Gm2$ and their biasing circuits. However, the input transconductor is actually outside the modulator loop as we can see from Figure 5.8 and it can be regarded as an individual stage to be designed separately.

5.5 Final Layout and Circuit Simulation

With the overall circuit structure set in section 5.3, and the schematics of individual building block designed in section 5.4, the continuous time bandpass ΣΔ modulator is implemented in 0.35μm triple-metal standard digital CMOS technology.

Figure 5.23 shows full layout of the circuit design. Because the circuit design is in a differential style, great emphases are placed on matching transistors between the two paths. The modulator covers an area of about 1.0 mm^2 in total. As we can see, the two bulky on-chip spiral inductors occupy quite some space, consuming about 60% of the total area. We can somehow reduce the size of inductors a little bit, but the size of capacitors has to be enlarged instead for a fixed modulator frequency $\omega_0 \approx \frac{1}{\sqrt{LC}}$. If the

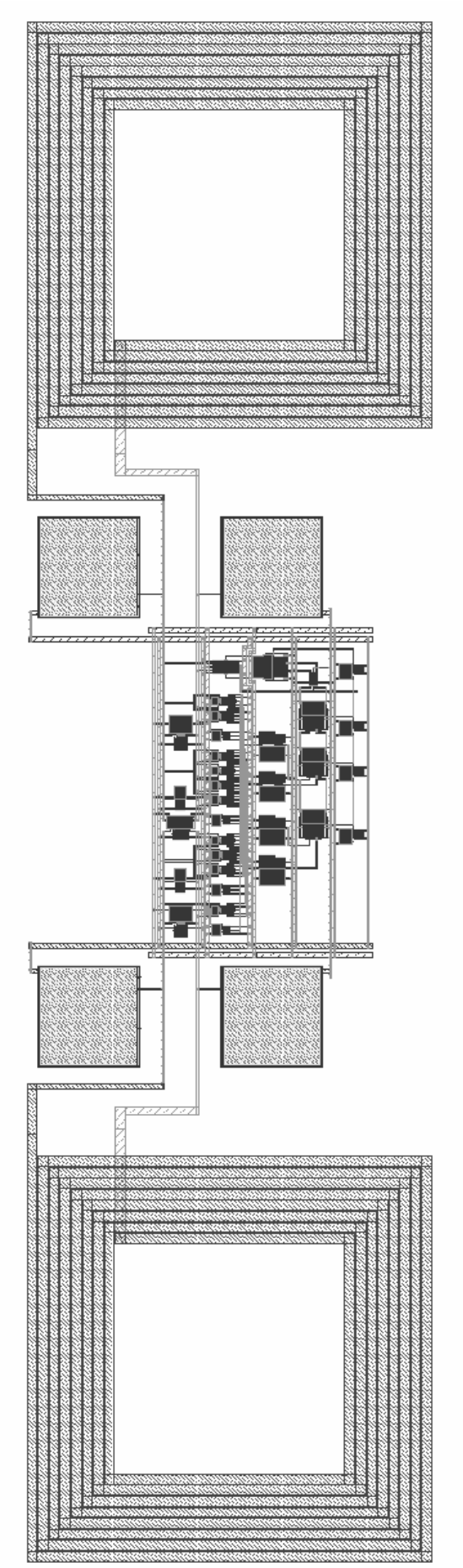

Figure 5.23 Overall circuit layout

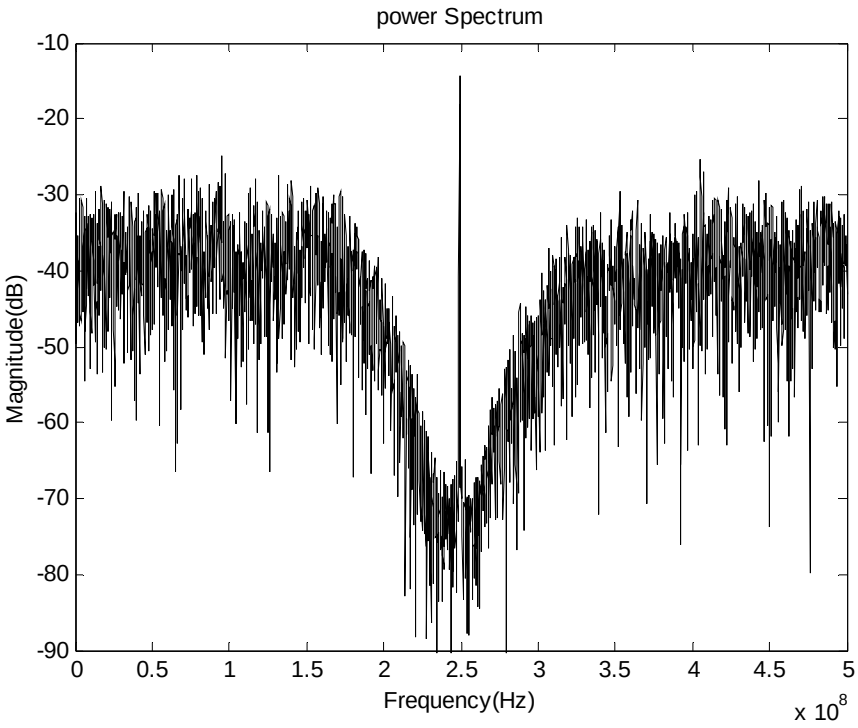

Figure 5.24 Output spectrum of the post-layout simulation

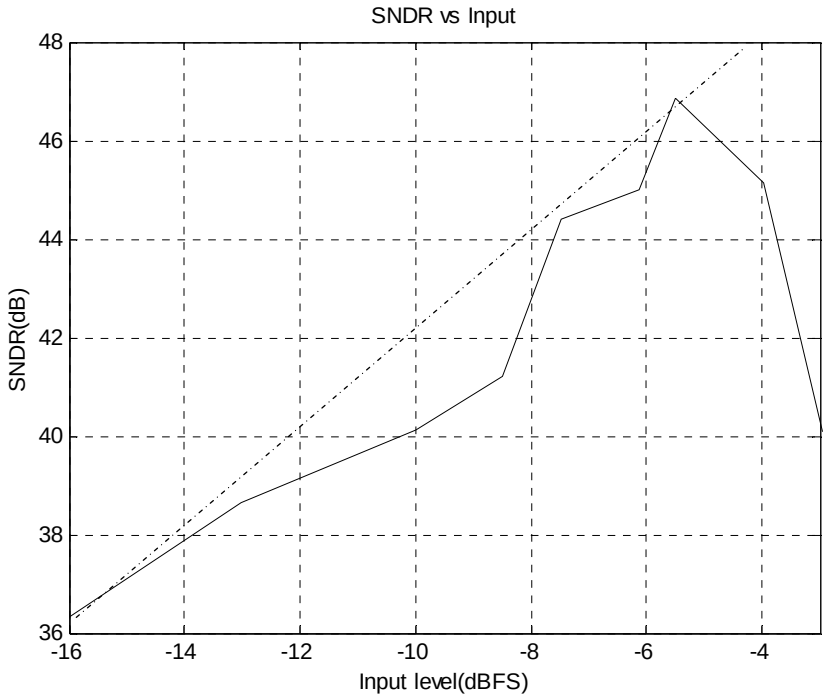

Figure 5.25 SNDR versus input magnitude

modulator was targeted for narrowband signals with higher frequency, both the size of L and C could be reduced. However, the increase in targeted ω_0 will also demand for a higher sampling rate, and results in more stringent speed requirements on the design of sampling latches discussed in Section 5.4.1.

With a power supply of 3.3V, the dissipation of the modulator is found from simulation to be 434 mW . The power consumption of the modulator is relatively high, compared to other low-frequency designs. However, by comparing power frequency ratio and some other measures, it should be established that this increase is consistent.

Post-layout simulation is carried out in CADENCE design environment, with RC parasitics and substrate noise modeling considered. Targeted for a conversion band centered on 250MHz, the modulator itself is clocked on a 1GHz signal. With a 249MHz sine wave as the input, the bit stream of the digital output is captured and then analyzed. Power spectrum of the modulator's output is shown in Figure 5.24. The simulation result shows that the quantization noise is shaped away from the interested signal band around 250MHz. However, if we compare the result to that of its ideal mathematical model in Figure 5.7, the modulator degrades a little bit in performance. The noise notch centered at 250MHz is filled with some white noise due to parasitic non-idealities in the circuit implementation, and the noise floor is raised to a magnitude of 70dB.

The modulator is tested with different amplitude of input signals and the resultant signal-to-noise-and-distortion ratio (SNDR) is calculated for a conversion bandwidth of 15.6MHz, which corresponds to an oversampling ratio of 64. Figure 5.25 shows the SNDR for different input levels. It is observed that the curve matches the expected slope of 1 dB/dB (the dashed line) well with only minor deviation. The modulator achieves a maximum SNDR of 47dB, which is equivalent to 7.5 bits of resolution.

5.6 Summary

In this chapter, details about the design of a 250MHz CT bandpass ΣΔ modulator are presented. With an introduction of the on-chip LC resonator, which sets the foundation for our high speed modulator, the system level structure is derived. Based on the mathematical model, the circuit level structure is further determined. Then, building blocks are characterized in detail: A high speed digital latch is designed, and the common-mode current spikes in DAC feedbacks are addressed by a swing reduction driver; the transconductor structure based on a pair of matched inverters is utilized for the high speed operation up to gigahertz range. Finally, the modulator design is laid out in 0.35μm triple-metal standard CMOS technology. Results of post-layout simulation in CADENCE environment are then given to show the effectiveness of the design.

CHAPTER 6

CONCLUSION AND FUTURE WORKS

6.1 Conclusion

In this work, we have presented the design of a fourth-order bandpass ΣΔ modulator with continuous time circuitry. Targeted for a conversion band centered on 250MHz, the modulator itself is clocked on a 1GHz signal. It is for the first time that such a high speed clocking is ever tried in CMOS ΣΔ A/D designs, and the center frequency of the conversion band is greatly pushed from tens of megahertz to 250 MHz for bandpass modulators in CMOS designs. The modulator is implemented in a 0.35μm triple-metal standard CMOS technology and occupies about 1.0 mm^2, with the two on-chip inductors consuming about 60% of the total area. Post-layout simulation is carried out in CADENCE design environment. For a conversion bandwidth of 15.6MHz, which corresponds to an over-sampling ratio of 64, the modulator achieves a maximum SNR of 47dB, an equivalent of 7.5 bits in resolution.

Among other designs available in the literature, the modulator designed in this project is summarized in Table 6.1. It can be seen that the modulator has a superior performance even comparable to those designed in special RF technologies. However, such a comparison may be unfair, as the performance result for the current work is not directly from chip measurements, but it somehow shows the great performance potential of the discussed modulator for high speed operation.

Table 6.1 Comparison of current work to other published sigma delta modulators

Type	Technology	IF	Sampling clock	OSR	SNR(dB)	Reference
2^{nd} order CT Lowpass(LP)	Inp-Transferred Substrate HBT	500MHz	18GHz	18	43	[7]
4^{th} order CT Bandpass(BP)	AlInAs/GaInAs heterojunction bipolar	180MHz	4GHz	32	39	[8]
2 CT LP	InGaP/InGaAs HEMT	50MHz	5GHz	50	43	[48]
2 CT LP	2μm CMOS	1MHz	50MHz	25	60	[10]
2 CT BP	0.5μm CMOS	200KHz	280MHz	700	42	[9]
BP with in-loop Freq.-translation	0.5μm CMOS	100MHz	400MHz	1000	45	[49]
4 CT BP	0.35μm CMOS	250MHz	1GHz	64	47	Proposed

6.2 Recommendation for Future works

The post-layout simulation shows the great performance potential of the designed CMOS modulator. It offers an economic way to realize high-speed A/D conversion and can be easily integrated on the same chip with DSP modules. Hence, it is recommended to test the design on a real chip.

However, in order for the modulator to work in good condition, quite some controlling signals need to be fine tuned. It is desired to find an algorithm to ease the control problem. Another issue is that the modulator's feedback waveforms are dependent on the timing of clock edges. A change in the clock duty cycle may result in a change in the feedback coefficients. It is preferable to integrate the clock generator with the modulator into the same chip.

In real silicon, the excess loop delay will vary depending on temperature and process corners, and performance may be consequently degraded. To make the inverters in the latch chain programmable or to tweak the transconductance values accordingly, are all plausible solutions to offset the variation in the loop delay. Methods to compensate for such performance degradation are worth further investigation.

In the current work, the modulator's sampling rate is limited by the speed of the digital latches. If the same modulator structure is implemented in a more advanced submicron process, a higher sampling rate and hence a higher conversion band may be reached.

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APPENDIX A

```
%Matlab Code for Feedback Coefficient Calculation in Section 3.4.3
w=pi/2;

%Create the State-Space model for the 2-order resonator
[CTsys1_A,CTsys1_B,CTsys1_C,CTsys1_D]=tf2ss([0 1 0],[1 0 w*w]);
CTsys1=ss(CTsys1_A,CTsys1_B,CTsys1_C,CTsys1_D);

%Find the discrete time model for path a1
%RZ DAC feedback
DTsys_Path_a1=c2d(CTsys1,1);
DTsys_Path_a1.B=inv(CTsys1.A)*(expm(CTsys1.A*(1-0))- ...
                expm(CTsys1.A*(1-0.5)))*CTsys1.B;

%Find the discrete time model for path a2
%HRZ DAC feedback
DTsys_Path_a2=c2d(CTsys1,1);
DTsys_Path_a2.B=inv(CTsys1.A)*(expm(CTsys1.A*(1-0.5))- ...
                expm(CTsys1.A*(1-1)))*CTsys1.B;

%Create the State-Space model for the 4-order resonator
[CTsys2_A,CTsys2_B,CTsys2_C,CTsys2_D]= ...
                tf2ss([0 0 1 0 0],[1 0 2*w*w 0 w^4]);
CTsys2=ss(CTsys2_A,CTsys2_B,CTsys2_C,CTsys2_D);
```

```
%Find the discrete time model for path a3
%RZ DAC feedback
DTsys_Path_a3=c2d(CTsys2,1);
DTsys_Path_a3.B=inv(CTsys2.A)*(expm(CTsys2.A*(1-0))- ...
                expm(CTsys2.A*(1-0.5)))*CTsys2.B;

%Find the discrete time model for path a4
%HRZ DAC feedback
DTsys_Path_a4=c2d(CTsys2,1);
DTsys_Path_a4.B=inv(CTsys2.A)*(expm(CTsys2.A*(1-0.5))- ...
                expm(CTsys2.A*(1-1)))*CTsys2.B;

%Convert the State-Space models to transfer funtion forms
%"tf_Adjustment" is for the purpose of making the denominators of the
% same order
tf_Adjustment=tf([1 0 1],[1 0 1],1);
H_DT_a1=tf(DTsys_Path_a1)*tf_Adjustment;
H_DT_a2=tf(DTsys_Path_a2)*tf_Adjustment;
H_DT_a3=tf(DTsys_Path_a3);
H_DT_a4=tf(DTsys_Path_a4);

%The coefficients of each numerator are loaded to "matrix" in columns
matrix=zeros(4);
num=H_DT_a1.num{:};matrix(:,1)=num(2:5)';
num=H_DT_a2.num{:};matrix(:,2)=num(2:5)';
num=H_DT_a3.num{:};matrix(:,3)=num(2:5)';
num=H_DT_a4.num{:};matrix(:,4)=num(2:5)';

%The feedback parameters are calculated and stored in column vector "a"
a=matrix\[0;2;0;1]
```