DESIGN AND DEVELOPMENT OF A CMOS POWER AMPLIFIER FOR DIGITAL APPLICATIONS

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NATIONAL UNIVERSITY OF SINGAPORE
2003

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A THESIS SUBMITTED
FOR THE DEGREE OF MASTER OF ENGINEERING
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING
NATIONAL UNIVERSITY OF SINGAPORE
2003

Acknowledgements

I would like to express my appreciation and sincere gratitude to my supervisors, Professor KOOI Pang Shyan, Professor LEONG Mook Seng and Dr. LIN Fujiang for their invaluable guidance, advice, and patience throughout my study and research work.

I would also like to express my deepest gratitude to Dr Rajinder SINGH for giving me the opportunity to pursue the degree during my employment with the Institute of Microelectronics (IME), Singapore.

I am also thankful to my colleagues in the IME for their support, advice and assistance.

Last but not least, my heartfelt thanks to my family, in particular, my husband for his understanding, thoughtfulness, and encouragement, without which this research project would have been unsuccessful.

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Summary

The IC technology for RFIC circuits continues to change as performance; cost and time to market are the three major factors that influence the choice of technology used. At present, GaAs, Silicon Bipolar and BiCMOS technologies constitute major portion of the RF market. However, CMOS technology, which supported by enormous momentum of the digital market have achieved higher transit frequencies in sub-micron region. Hence, it is viable now to integrate the RF portion in a single or even with digital circuits in future.

In this thesis, issues of implementing RF circuits in CMOS technology like substrate coupling, low Q passive components, low breakdown voltage, hot carrier effects, parameter variations with temperature and process, low current capabilities of metal layers will be discussed in details.

The main focus of this thesis will be the design and implementation of a 2.45GHz CMOS Power Amplifier. The models used in designing the power amplifier will be shown. The practical aspects of the implementation of the circuit will be highlighted. Methods are proposed to overcome some of the issues mentioned above. A cascade output stage structure is used to solve the hot carrier effects and low breakdown voltage issues. Temperature dependent biasing circuit is used in the design. The simulation results of the design and measurement results of the fabricated die will be presented.

CHAPTER 1

Introduction

This chapter will give the background of this project as well as the scope of the project work. The outline of this thesis will also be covered.

1.1 Background

Wireless communication systems have gained their popularities in the last few years. Everyone is competing to produce low power consumption and low cost products that are able to meet the system standards. Gallium Arsenide (GaAs) technology has been the prime choice of RF designers in implementing RF blocks for systems like GSM, CDMA and so on. The above mentioned technology has superior performance like higher output power, higher gain and lower noise figure. However, as other standards like WLAN and Bluetooth standards that have less stringent specifications for RF blocks are becoming more popular, RF designers are now trying to implement the circuits in standard CMOS technology.

However, CMOS technology, which supported by enormous momentum of the digital market has achieved higher transit frequencies in sub-micron region. As the CMOS technology critical physical dimensions scale down and f_T and f_{max} scale up, a

great deal of interest and research has been geared to realize RFIC (Radio Frequency Integrated Circuits) in CMOS technology. The reason being CMOS technology has so far still the cheapest wafer process technology available.

The power amplifier being the RF front end block of the transmitter, determine the success or the failure of the overall design of the transmitter. Hence, it serves as a very good test vehicle to realize RFIC in CMOS technology.

1.2 Project Scope

The main challenge is to integrate Power Amplifiers (PA) in standard CMOS process. The goal of this project is to realize a RF power amplifier in standard CMOS process and to integrate the power amplifier designed into a transceiver. The scope of the project includes studying of the basics of power amplifiers and designing a fully integrated power amplifier. The power amplifier designed would aim to satisfy the specifications of the Bluetooth Standard.

1.3 Report Outline

In this report, the practical implementation of a CMOS power amplifier will be discussed. This includes the realization of passive lumped components on silicon substrate and also parasitic effects introduced by package. Some reliability aspect of the realization of the power amplifier will be discussed as well.

In Chapter Two, an overview of the technologies used for high frequencies circuits will be given. The characteristics of CMOS technology and challenges faced

by the circuit designers will be discussed in details. The characteristics and shortcomings of the passive components in CMOS technology will be described at length.

In Chapter Three, the performance indicators of a power amplifier like power output, efficiency, linearity and so on will be discussed in details. Different classes of power amplifiers will be discussed at length. The literature review of CMOS power amplifiers will be reported in this particular chapter as well.

In Chapter Four, a detail description of the design implementation of the power amplifier will be given. The design setup discussed later will include simulation setup and models needed for the design.

In Chapter Five, the measurement setups for the testing of the power amplifiers designed will be described. The measurement of the power amplifier is performed as on-wafer measurement. The measurement results will be presented in comparison to the simulation results.

In Chapter Six, the conclusions will be summarizes and some suggestions for future work will be given.

1.4 Original Contributions

The power amplifier designed in this project has been integrated in a Bluetooth transceiver. The circuit's robustness is observed as it has maintained its performance under various conditions including temperature change, supply voltage change and

process variations. This is achieved by various circuit techniques. This is one of the aspects that have not been widely discussed in the literatures. The work done in this project is presented in the following conference papers:

[1] My The Doan, Qian Yin, Khoo Ee Sze, P. B. Khannur, S. C. Rustagi, J. Shi, P. D. Foo, A. Ajjikuttira, "Performance of a CMOS Bluetooth Transceiver IC with Copper RF Passives" RFIC Symposium, 2002

[2] A. Ajjikuttira, C. Leung, Khoo Ee Sze, M. Choke, R. Singh, T. H. Teo, B. C. Cheong, J. H. See, H, S. Yap, P. B. Leong, C. T. Law, Masaaki Itoh, "A Fully-Integrated CMOS RFIC for Bluetooth Applications" IEEE ISSCC Conference, 2001

CHAPTER 2

CMOS Technology: Characteristics and Challenges

This chapter will give an overview of the technologies used for Gigahertz frequencies circuits. The characteristics of CMOS technology and challenges faced by the circuit designers will be discussed in details. The characteristics and shortcomings of the passive components in CMOS technology will be described at length.

2.1 Technology Overview

There are a few semiconductor technologies that are used for realizing circuits at radio frequencies and microwave frequencies. They are GaAs MESFET, GaAs HBT, Si LDMOS, SiGe HBT, Si BJT, CMOS and etc. For power amplifiers with a high output power above 1Watt[1] or with an operating frequency above 10GHz[2], the technologies generally used would be GaAs MESFET or GaAs HBT. These technologies are able to provide high electron mobility transistor and substrate that is semi-insulating with negligible loss. Si LDMOS RF power transistors are able to produce 120 Watts RF power at 2GHz[3]. Of course, LDMOS process is more suitable for power amplifier modules instead of power amplifier integrated circuits. SiGe HBT power amplifiers are also capable of giving a high efficiency with sufficient linearity

for PCS CDMA applications[4]. A 2.8V, 3.2Watt Si BJT power amplifier with 54% PAE achieved at 900MHz has been reported[5].

The above-mentioned technologies have the capabilities of producing high performance power amplifiers compared to CMOS technology. However, we can see that a large number of efforts are made to realize power amplifiers in CMOS technology[6],[7],[8],[9]. This is because the technology's potential of giving lower cost solutions and higher integration level of the circuits which may lead to a single chip transceiver solution in future. As we all know, cost is the most important consideration for any design. Hence, if the designer is able to produce a power amplifier meeting the requirements with lowest cost, he or she will win the game in the market.

2.2 CMOS Technology Issues

In the following section, we will examine the limitations and the reliability issues in a standard CMOS technology.

2.2.1 Low Breakdown Voltage Limitations

CMOS transistors have a few device voltage limitations. They are drain-source punch-through, gate oxide rupture, drain or source diode zener breakdown and time-dependent dielectric breakdown (TDDB).

Drain-source punch-through happens when the drain voltage is high enough to cause the depletion region around the drain to extend all the way to the source,

effectively eliminating the channel. As a result, the gate voltage can no longer control the current flow from drain to source. As the gate length reduces, the drain-source punch-through voltage also reduces. For a 0.35µm gate length transistor, the punch-through voltage is in the order of $2V_{DD}$.

Gate oxide rupture will result in irreversible gate to channel short. The region of the gate oxide near the drain frequently ruptures first in a power amplifier when the drain voltage is at its maximum potential and the gate voltage is at its minimum potential. Oxide breakdown voltage for a 0.35µm MOSFET is about 7V.

The drain and source diffusion regions are heavily doped to reduce their resistivity. As a result, the junction diode formed by the drain and source diffusion regions with the substrate have low breakdown voltage. In a 0.35µm CMOS technology, the junction breakdown voltage for N+/P- diode and P+/N- diode is 7.0V.

Low breakdown voltage has limited the voltage swing at the drain of the transistor to $2V_{DD}$ if no immediate failure is to be seen. Hence, the output power of a CMOS power amplifier is also limited.

2.2.2 Low Substrate Resistivity

The substrate resistivity of the silicon substrate used is generally low, typically ranges from 0.01 Ω-cm to 10 Ω-cm. Hence, passive components have more substrate loss compared to other semi-insulated substrate like GaAs, InP and etc. Substrate loss is a result of capacitive coupling and inductive coupling to the substrate. As a

consequence, the Q-factor of the passive components like inductors and capacitors has been greatly reduced.

Also, noise is easily coupled from one portion of the circuit to another portion of the circuit. This is called substrate noise coupling. However, for power amplifiers, our main concern is actually to prevent the noise injected by the power amplifier into the substrate and then coupled to other circuits like Low Noise Amplifier (LNA), Voltage Controlled Oscillator (VCO) and so on. This is due to the large signal swing of the power amplifier and is more severe when the circuit is single-ended.

2.2.3 Temperature Effects

The transistors performance, for example power gain, varies with temperature. As there are two temperature-dependent effects in CMOS transistors. The threshold voltage will change with temperature; its temperature coefficient is roughly –2mV/^{o}C. Also, the carrier mobility reduces with increasing temperature in accordance with the following equation:

$$\mu(T) = \mu(T_O)\left[\frac{T}{T_O}\right]^{-\frac{3}{2}}, \tag{2.1}$$

where T_O is the reference temperature (e.g. 300K)

Of course, other than transistors, the characteristics of other components like capacitors, resistors, inductors and others are changing with temperature as the process materials' characteristics are varying with temperature. For example the temperature coefficient of the poly-resistor can be governed by:

$$TC = \frac{1}{R}\frac{\partial R}{\partial T} \quad , \tag{2.2}$$

where TC represents the temperature coefficient of the resistor and R represents the resistance.

2.2.4 Hot Carrier Effects

Deep sub-micron MOSFET will experience high lateral electric fields if the drain-source voltage is large. Although the average velocity of the carriers saturates at high electric fields, the instantaneous velocity of the carriers continue to increase, especially as they accelerate towards the drain. These carriers are called hot carriers.

Hot carrier effects generally cause threshold voltage shift and trans-conductance degradation. There are a few types of hot carrier injection mechanisms; namely channel hot-electron injection (CHE), drain avalanche hot-carrier injection (DAHEC), substrate hot electron injection (SHE), secondary generated hot carrier injection (SGHE) and direct tunnel injection.

The CHE injection is caused by the escape of “lucky electrons” from the channel, which had gain sufficient energy to surmount the Si-SiO_2 barrier, resulting in a sizable amount of gate current. If an n-channel MOSFET is operating at VG=VD, the condition is optimum for CHE injection. On the other hand, DAHC injection results in both hot holes and hot electrons due to impact ionization at the drain. Both holes and electrons are injected to the gate and across the drain junction below the substrate surface.

As for SHE injection, the carriers gain energy from the substrate voltage before impinging on the Si-SiO_2 interface. SHE injection does not occur in most of the circuits except for bootstrap circuits. However, it is often being used to evaluate the gate insulator qualities. Last but not least, SGHE injection is due to minority carriers from secondary impact ionization. Deep sub-micron MOSFET has very thin gate oxide, which enables direct tunneling of electrons or holes from the substrate to the gate. Hence, direct tunnel injection often dominates the gate leakage current for deep sub-micron MOSFETs.

Carrier injection into the gate oxide can lead to hot carrier degradation effects such as threshold voltage changes due to occupied traps in the oxide. Hot carriers can also generate traps at the silicon-oxide interface leading to transconductance degradation, sub-threshold swing deterioration and stress-induced drain leakage. In general, these degradation effects set a limit to the life-time of a transistor. The substrate current is directly related to the life-time of a device that is subjected to hot carrier injection, and is expressed as

$$\tau \alpha (I_{sub})^{-1} \quad , \tag{2.3}$$

where τ is defined as the aging time in which the threshold voltage is shifted by 10mV or the transconductance is reduced by 10%[10].

2.2.5 Current Carrying Capability

This issue is unique in high power output power amplifiers, as the current flowing through the interconnect metal can be up to hundreds of milli-amperes or even

up to a few amperes. The current carrying capability of aluminum interconnect in CMOS is not as good as the gold interconnect used in GaAs technology.

2.3 Passive Components of CMOS Technology

The quality of the passive components in CMOS technology plays a significant role in determining the circuit performance. The passive components should incur the lowest loss possible to the circuit and also their characteristics should change as little as possible with temperature variations. They should have low process variance.

2.3.1 Inductor

Due to the metal resistive loss and the substrate loss, integrated inductors in standard CMOS process generally suffer from low quality (Q) factor. As inductors are normally part of the input matching, inter-stage matching and output matching circuit, having low Q factor will result in power loss and lower efficiency of the whole circuit.

Significant amount of efforts have been reported to improve the Q-factor of the passive components especially the Q-values for the inductors. There are a few approaches to increase the quality factor of an inductor.

The first approach is to increase the substrate resistivity to reduce substrate loss. Increasing the substrate resistivity up to 2kΩ-cm has enabled the inductor to have a Q-factor of 10[11],[12]. Another method is to layout the inductor in SOI (Silicon-on-Insulator) or SOS (Silicon-on-Sapphire) substrate.

The second approach is to reduce the series resistive loss of the inductor coil that is made up of aluminum metallization. This can be achieved by increasing the thickness of the metal layer of the inductor [13],[14] or by stacking a few metal layers to increase the overall metal thickness [15],[16]. However, there is a limit to the increase of the metal thickness as the skin effect will eventually impose a diminishing return of the advantages in the increase of the metal thickness. The skin depth is given by

$$\delta = \sqrt{\frac{2}{\omega \mu_O \sigma}} \quad , \tag{2.4}$$

The third approach is to increase the oxide thickness between the inductor metallization and the substrate. This can be done by using a top metal layer to layout the inductor. Another method is to use thick polyimide as the dielectric between the inductor and the substrate [17].

To characterize an inductor, its surrounding has to be properly defined, especially the substrate. However, it is difficult to define the substrate as a good RF ground. However, we can put a patterned ground shield in between the inductor and the silicon substrate. Eddy current that flows in the silicon substrate that is semi-conducting will cause the effective inductance of the inductor to reduce and as a result reducing the Q-factor of the inductor. The patterned ground shield is able to reduce the Eddy current with the disadvantage of reducing the self-resonant frequency of the inductor. Halo substrate contact is able to provide proper RF ground without the degradation in maximum Q-factor and self-resonant frequency [18].

There are a few methods to layout the inductor. They can be layout as a straight transmission line, a meander structure or in a spiral form. The spiral form of layout is most popular one as it can provide the highest inductance value with the smallest area. The spiral inductor can be of rectangular shape, octagonal shape, circular or other shapes.

2.3.2 Capacitor

There are a few ways to realize a capacitor in a CMOS process. One method is to use the interconnect layers to make parallel plate capacitors. The unit capacitance of this type of capacitors is generally quite small as the dielectric thickness of the two adjacent metals is in terms of a few hundred Armstrong ($\mathring{A}$). Another method is to use the sidewalls of the two adjacent metal lines on the same metal layer. Of course, these two methods can be combined, in other words, both vertical flux and horizontal flux are used to contribute to the total capacitance. In order to reduce parasitic capacitance to ground, the top metal layers are preferred to form the capacitors.

If the CMOS process is an analog process that has double poly, inter-poly capacitor that has higher unit capacitance can also be used. However, the inter-poly capacitor will have higher percentage of parasitic capacitance to ground, since the poly layer is closer to the substrate compared to the metal layers. As a result, the inter-poly capacitor is best used as a shunt capacitor to ground where the parasitic capacitance can be lumped to the main capacitance.

Another alternative is to use a MOS capacitor, which is actually the gate capacitance of a MOS transistor. As the gate length of CMOS technology scales down

together with the scaling down of gate oxide thickness, the unit capacitance of MOS is increased. It is important to keep the transistor in strong inversion. Failing to do so will cause the capacitance to be small, lossy and non-linear. The MOS capacitor is usually used as a decoupling capacitor. There are also efforts in the use of resonator circuit for Voltage Controlled Oscillator (VCO) applications.

Junction capacitance such as capacitance formed by the P+ diffusion region in an N-well can be used in a VCO as well. This stems from the fact that the junction capacitance varies with the bias applied. And hence enabling the VCO to have certain tuning range.

2.3.3 Resistor

Another passive component that is available in CMOS process is resistor. There are a few types of resistors like unsalicide poly resistor, N+ diffusion resistor, P+ diffusion resistor, N-well resistors and so on. Among all these resistors, unsalicide polysilicon resistor will give the lowest parasitic capacitance to substrate. Salicide is a material used to reduce the resistance of the polysilicon and is used at the polysilicon at the gate of the transistor.

CHAPTER 3

Fundamentals of Power Amplifier

RF Power Amplifiers exist whenever there is a transmitter. They are used to transmit high power signals to any recipient through antenna. A short range radio link device is transmitting power in terms of a few milliwatts, a cellular phone is transmitting power in terms of hundred of milliwatts, and a base station is transmitting power in terms of a few hundred watts.

In this chapter, the performance indicators of a power amplifier like power output, efficiency, linearity and so on will be discussed in details. Another topic that will be discussed at length is different classes of power amplifiers. The literature review of CMOS power amplifiers will be reported in this particular chapter as well.

3.1 Power Amplifier Performance Indicators

3.1.1 RF Power

Power is defined as the instantaneous energy dissipated in the load. The power delivered to the load is given by the product of the voltage across the load and the current flowing into the load. RF power is characterized in terms of RMS power.

3.1.2 Power Gain

Gain refers to how well the amplifier converts the RF input power to the RF output power. When power gain is mentioned for a power amplifier, it is referred to as the transducer power gain, G_T, and is given as

$$G_T = \frac{\text{Power Delivered to the Load}}{\text{Available Input Power}} \quad . \tag{3.1}$$

3.1.3 Efficiency

Efficiency refers to how well the amplifier converts the DC input power to RF output power. This is called drain efficiency, DE, which describes the DC-to-RF power conversion efficiency:

$$DE = \frac{P_{out,RF}}{P_{in,DC}} \quad , \tag{3.2}$$

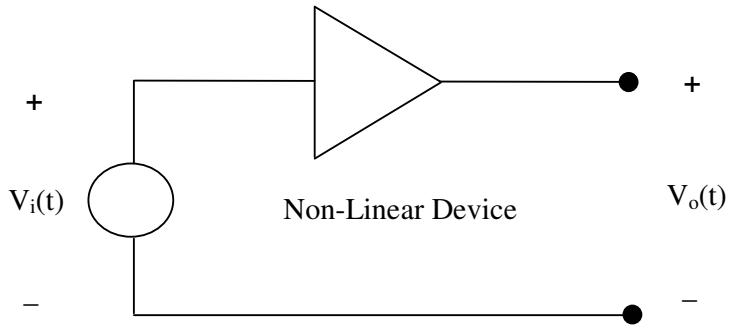
where $P_{in,DC}$ refers to the DC input power and $P_{out,RF}$ refers to the RF output power.

At RF frequencies, there is AC current flowing into the gate of the transistor. Hence, the RF input power used to drive the transistor must be taken into account when calculating the efficiency. A parameter needs to be derived to account for the drain efficiency and the power gain of the amplifier. The parameter is known as power added efficiency, PAE;

$$PAE = \frac{P_{out,RF} - P_{in,RF}}{P_{in,DC}} \quad . \tag{3.3}$$

3.1.4 Linearity

Figure 3.1 Non-Linear Device 1



The amplifier, which is also known as the non-linear device, output consists of an infinite series of nonlinear products, which are added to the linear gain represented by the first term:

$$v_o = a_1 v_i + a_2 v_i^{\,2} + a_3 v_i^{\,3} + a_4 v_i^{\,4} + a_5 v_i^{\,4} + \ldots\ldots\ldots\ldots \quad (3.4)$$

The series is called power series. The a_n coefficients are assumed to be real. The a_n coefficients are sensitive to the input and output matching circuit and the bias voltage of the gate and the drain of the transistor. For $v_i = A\cos\omega t$, the power series becomes

$$v_o = a_1(A\cos\omega t) + a_2(A\cos\omega t)^2 + a_3(A\cos\omega t)^3 + a_4(A\cos\omega t)^4 + \ldots\ldots \quad (3.5)$$

From Eqn 3.5, it can be observed that the distortion created by the higher order terms will be mixed down to the fundamental frequency. The odd order harmonic components (3f, 5f,..) are generated by odd order terms. Each odd order term will also generate a component in the fundamental frequency. These components are the cause of gain compression when the amplifier is driven strongly. Even order harmonics (2f,

4f,..) are generated by even order terms. The even order terms will also generate a component at DC. The components will result in a shift in bias point when the signal level is high. For example, the distortion created by the third order term is

$$a_3(A\cos\omega t)^3 = a_3A^3\left[\frac{3}{4}\cos\omega t + \frac{1}{4}\cos 3\omega t\right] \quad . \tag{3.6}$$

The term $a_3A^3\left(\frac{3}{4}\cos\omega t\right)$ will attenuate the fundamental output signal if a_3 is negative, causing the gain to be compressed.

The 1dB compression point (P_{1dB}) and the third order intercept point are good indicators for the linearity parameter of an amplifier. However, P_{1dB} will be a more realistic indicator for the linearity performance of a power amplifier as this parameter also includes the effects of the higher order terms other than the third order term. Also, it is more difficult to estimate the value of P_{1dB} with equations.

Power series has no phase representation in the output term. It can only derive the amplitude distortion of the amplifier, but not the phase distortion of the amplifier. In contrast, Volterra series includes both amplitude components and phase components.

For modern communication systems, digital modulated signals are being transmitted. Digital modulated signals can either be constant envelope signal or non-constant envelope signal with peak-to-average ratio. A digital modulated signals is also not a simple sinusoidal signal, but consist of a carrier signal (which is a sinusoidal signal) modulated by a modulating signal. The resultant signal occupies a certain

bandwidth. Hence, to measure the linearity of a power amplifier that is used to transmit a digital modulated signal, P_{1dB} is not sufficient, especially for signals with large peak-to-average ratio. Adjacent Channel Power Ratio (ACPR), defined as the power ratio of two neighboring frequency continuum is used to characterize the linearity of the power amplifier. When a non-linear device like a transistor is driven by a modulated signal, the output signal's bandwidth is broaden by the odd order terms. This is called spectral re-growth or spectral regeneration. Spectral re-growth is the cause of adjacent channel interference.

$$ACPR = \frac{\int_{f_3}^{f_4} S(f)\,df}{\int_{f_1}^{f_2} S(f)\,df} \quad , \tag{3.7}$$

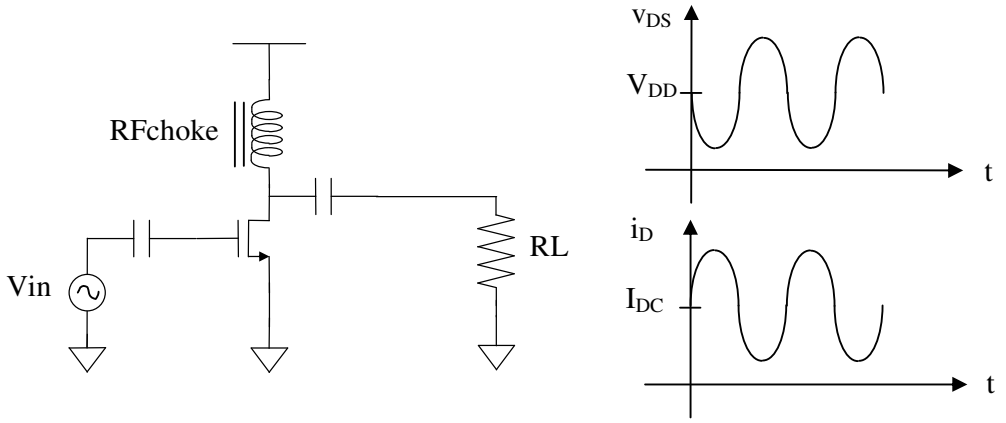
where S(f) represents the power spectral density (PSD), f_1 and f_2 represent the frequencies where the desired channel is occupying; f_3 and f_4 represent the frequencies where the adjacent channel is occupying.

3.2 Linear Power Amplifiers

A linear power amplifier employs a power transistor working as a current source. If the input signal swing is small, the transistor will operate in the saturation region only and the output signal swing will be directly proportional to the input signal swing. A few different types of the linear amplifiers will be discussed in the following section.

3.2.1 Class A Power Amplifier

Figure 3.2 Class A Power Amplifier 1



(a) Class A Implementation (b) Drain voltage and Current

A Class A power amplifier (PA) is the most basic type of power amplifier. In Class A operation, the transistor is always in the active region and conducting current. The AC drain voltage and AC drain current will swing symmetrically around the DC values. The drain current is approximated by:

$$i_D = I_{DC} + I_{RF} \sin \omega_o t \quad , \tag{3.8}$$

where I_{DC} is the DC bias current, I_{RF} is the amplitude of the AC signal component of the drain current and ω_o is the signal frequency or the operating frequency of the amplifier. The drain voltage is approximated by:

$$v_D = V_{DC} - I_{RF} R_L \sin \omega_o t \quad , \tag{3.9}$$

where V_{DC} is the DC bias voltage at the drain, R_L is the load resistance presented to the output terminal of the transistor. The drain voltage and drain current are sinusoidal that are 180^o out of phase with each other.

The maximum output power obtainable from a Class A power amplifier is determined by the power level at which the RF drain current and the RF drain voltage starts to clip; in other words, the output power is limited by the limited swing of the drain current and drain voltage. The maximum peak drain-to-source voltage will be $2V_{DD}$ while the maximum peak drain current will be $2V_{DD}/R_L$. The optimum load resistor that helps the amplifier to obtain maximum output power has a value of

$$R_{opt} = \frac{V_{\max}}{I_{\max}} \quad , \tag{3.10}$$

where $V_{\max} = 2(V_{DD} - V_{knee})$ and $I_{\max} = 2I_D$. As a result,

$$R_{opt} = \frac{V_{DD} - V_{knee}}{I_D} \quad . \tag{3.11}$$

The maximum output power of the amplifier is given by

$$P_{opt} = \frac{1}{2}(V_{DD} - V_{knee})I_D \quad . \tag{3.12}$$

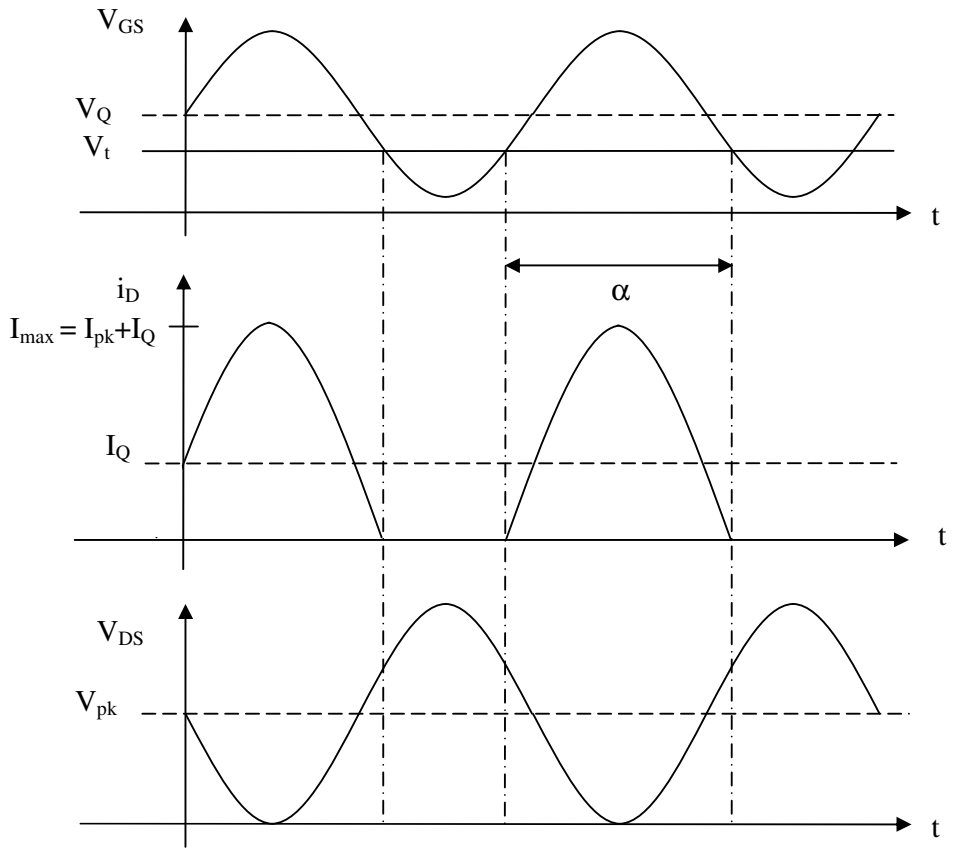
With DC power = $V_D I_D$, it is obvious the maximum drain efficiency of Class A power amplifier is less than 50%.

3.2.2 Amplifiers with Various Conduction Angle

Before proceeding to other classes of power amplifiers, let's look at how the conduction angle affects the current and voltage waveform; as other type of linear power amplifiers are characterized by differentiating the transistor's conduction angle.

By reducing the bias voltage of the transistor until at some point of the duty cycle, the drive signal goes below the threshold voltage, and thus there is no current conducting. It is illustrated in Figure 3.3.

Figure 3.3 Reduced Conduction Angle Waveform



Where V_t is the threshold voltage of the transistor, V_Q is the quiescent bias voltage of the transistor, I_Q is the quiescent drain current, I_{pk} is the amplitude of the drain current, I_{max} is the peak drain current and α is the conduction angle of the transistor, V_{pk} is the amplitude of the drain voltage.

$$\begin{aligned} i_D &= I_Q + I_{pk} \sin \omega_o t \quad , \; -\frac{\alpha}{2} < (\omega_o t) < \frac{\alpha}{2} \\ &= 0 \quad , \; -\pi < (\omega_o t) < -\frac{\alpha}{2} \; ; \; \frac{\alpha}{2} < (\omega_o t) < \pi \end{aligned} \tag{3.13}$$

where $$\cos\left(\frac{\alpha}{2}\right) = -\frac{I_Q}{I_{pk}} \quad , \quad \cos\left(\frac{\alpha}{2}\right) = -\frac{I_Q}{I_{\max} - I_Q} \tag{3.14}$$

& $$i_D = I_{pk}\left[\cos \omega t - \cos\left(\frac{\alpha}{2}\right)\right] . \tag{3.15}$$

By looking at the continuous drain current representation in the equation below:

$$i_D = I_{DC} + I_{FUND} \sin \omega_o t + I_{2nd} \sin 2\omega_o t + I_{rd} \sin 3\omega_o t + ... \tag{3.16}$$

where I_{DC} is the average drain current or the DC drain current and I_{FUND} is the amplitude of the fundamental drain current, I_{2nd} is the amplitude of 2nd harmonics drain current and I_{3rd} is the amplitude of the 3rd harmonics drain current.

$$I_{DC} = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} I_{pk}\left[\cos \omega t - \cos\left(\frac{\alpha}{2}\right)\right] d(\omega t) \tag{3.17}$$

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} I_{pk}\left[\cos\omega t - \cos\left(\frac{\alpha}{2}\right)\right]\cos(n\omega t)\,d(\omega t) \tag{3.18}$$

where I_n is the amplitude of the nth harmonics drain current.

As a result, for any conduction angle, α, the DC drain current and the fundamental drain current would be

$$I_{DC} = \frac{I_{pk}}{2\pi}\left[2\sin\frac{\alpha}{2} - \alpha\cos\frac{\alpha}{2}\right] \quad \text{or} \quad I_{DC} = \frac{I_{\max}}{2\pi}\frac{\left(\sin\frac{\alpha}{2} - \alpha\cos\frac{\alpha}{2}\right)}{1-\cos\frac{\alpha}{2}} \tag{3.19}$$

$$I_{FUND} = \frac{I_{pk}}{2\pi}(\alpha - \sin\alpha) \quad \text{or} \quad I_{FUND} = \frac{I_{\max}}{2\pi}\frac{\alpha - \sin\alpha}{1-\cos\alpha/2} \tag{3.20}$$

It is observed from equation (3.19) that the DC drain current reduces monotonically with the conduction angle.

The RF fundamental output power is given by:

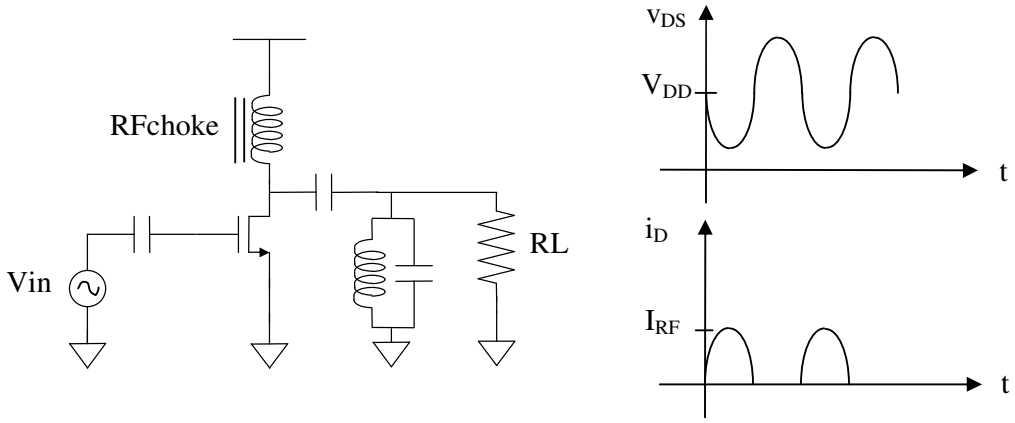
$$P_{FUND} = \frac{V_{FUND}}{\sqrt{2}}\frac{I_{FUND}}{\sqrt{2}} \tag{3.21}$$

$$P_{FUND} = \frac{1}{2}V_{pk}\left[\frac{I_{pk}}{2\pi}(\alpha - \sin\alpha)\right] \tag{3.22}$$

3.2.3 Class B Power Amplifier

A Class B power amplifier has gate current and gate voltage conducting for half a cycle. If the drive signal is symmetrical, the conduction angle remains to be 180° for varying drive signals.

Figure 3.4 Class B Power Amplifier



(a) Class B Implementation (b) Drain voltage and Current

The drain current is sinusoidal for half a cycle and zero value for the other half of the cycle:

$$i_D = I_{RF} \sin \omega_o t \quad \text{for } i_D > 0 \tag{3.23}$$

From eqn (3.19) & (3.20), it is obtained that for maximum output power

$$I_{DC} = \frac{I_{\max}}{\pi} \quad \& \quad I_{FUND} = \frac{I_{\max}}{2} \quad \& \quad V_{\max} = I_{\max} R_{opt} \tag{3.24}$$

As the maximum value for V_{max} is $2V_{DD}$, hence I_{max} would be $2V_{DD}/R_{opt}$. After some calculations, the maximum possible ideal drain efficiency of the transistor operating in Class B operation is $\pi/4$, which equals to 78.5%. However, to achieve the

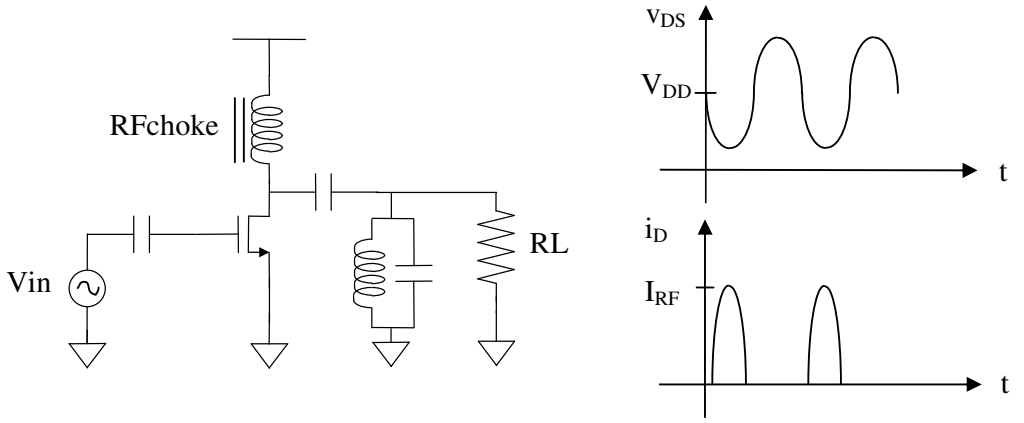
same output power as a Class A power amplifier, a Class B power amplifier requires 6dB more drive power or input power.

A high Q factor output tank circuit is essential to obtain a sinusoidal voltage waveform at the load. A parallel tank circuit is used.

3.2.4 Class C Power Amplifier

For a Class C power amplifier, the conduction angle of the transistor is less than 180°. The transistor is still assumed to be operating as a current source with high output impedance.

Figure 3.5 Class C Power Amplifier



(a) Class C Implementation (b) Drain voltage and Current

From eqn (3.20), $I_{FUND} = \frac{I_{pk}}{2\pi}(\alpha - \sin\alpha)$, the magnitude of the voltage across the load would be

$$V_{FUND} = \frac{I_{pk} R_{opt}}{2\pi}(\alpha - \sin\alpha) \tag{3.25}$$

By equating $I_{pk} = V_{DD}/R_{opt}$, the maximum efficiency is defined by

$$DE = \frac{\alpha - \sin\alpha}{4\left[\sin\frac{\alpha}{2} - \frac{\alpha}{2}\cos\left(\frac{\alpha}{2}\right)\right]} \quad . \tag{3.26}$$

The efficiency reaches 100% as the conduction angle shrinks towards zero. Of course, the output power also shrinks towards zero at the same time. Though the above observation is not useful, high efficiency can still be achieved by using class C power amplifier. However, the conduction angle changes with RF input drive signal causing the gain of the transistor also to vary with drive signal. Hence, class C power amplifier is not suitable for a modulated signal with amplitude-modulated envelope.

3.3 Switch Mode Power Amplifiers

A switch mode power amplifier has the power transistor operating as a switching device. If the switching device is an ideal device, the drain efficiency of the amplifier can be as high as 100%, that is, with zero switching time, zero on-resistance and infinite off resistance for the switching device. However, as the power transistor is not an ideal switch after all, the drain efficiency can never reach 100%. First of all, certain DC power will be dissipated in the transistor, as the on resistance is not zero. Secondly, the switching time is not zero as well, resulting in an overlap of voltage and current during the switching transition process, making the voltage and current (V-I)

product or the power dissipation non-zero. In a switch mode power amplifier, the output power is determined by the voltage supply and their relationship is as follow:

$$P_{OUT} \propto V_{DD}^2 \tag{3.27}$$

Of course, the effects of the non-idealities can be reduced by design. The different types of switch mode power amplifiers will be discussed in the following section.

3.3.1 Class D Power Amplifier

A Class D power amplifier uses a pair of transistors as a pair of switches that defines either a rectangular drain voltage or rectangular drain current waveform. It also has an output tuned circuit which is either a series tuned circuit or a parallel tuned circuit that is tuned to the operating frequency and presenting a sinusoidal output waveform at the load after removing the harmonics content in the waveform.

The complementary voltage switching Class D power amplifier is shown in Figure 3.6. The input transistors are driven by a pair of differential current (180° out of phase) after being coupled by the input transformer. The pair of transistors acts as a double pole switch. The switching of the transistor results in a square voltage waveform. An output series tuned circuit will present high impedance to the harmonics and nearly zero impedance to the operating frequency. Hence, only fundamental current waveform is present at the load, resulting in a sinusoidal current and voltage waveform. The output current is represented by:

$$i_o = \frac{2V_{CC}}{\pi R}\sin\omega_o t \quad , \tag{3.28}$$

The output power is represented by:

$$P_O = \frac{2}{\pi^2}\frac{V_{CC}^2}{R} \quad , \tag{3.29}$$

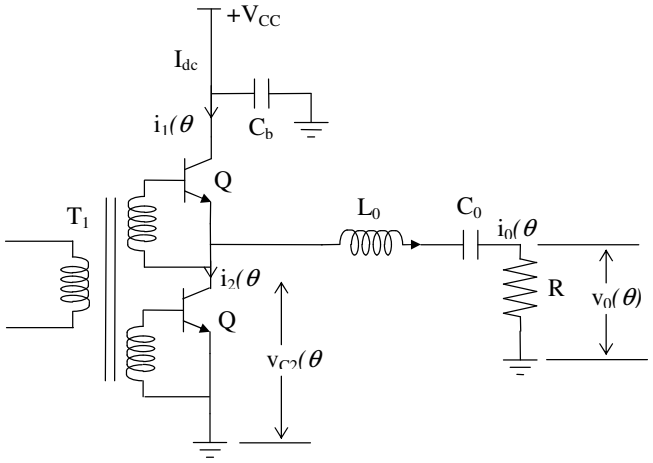
The DC current, I_{DC} is the average of i_o, which means $I_{DC} = \frac{2}{\pi^2}\frac{V_{CC}}{R}$.

It is also observed that $P_{DC} = \frac{2}{\pi^2}\frac{V_{CC}^2}{R}$, giving 100% efficiency for ideal case.

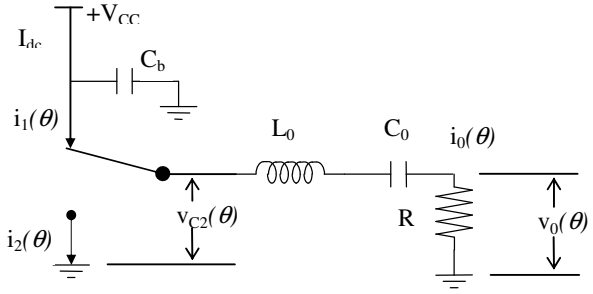
There are other types of configuration of Class D power amplifiers. They are transformer-coupled voltage switching configuration, using transformer between the output of the transistor and the tuned circuit and also transformer-coupled current switching configuration; which is the dual of the voltage switching configuration as the voltage and current waveforms are interchanged. The current switching configuration must be driven by a square wave input signal, whereas the voltage switching configuration can be driven by either a square wave input signal or a sine wave input signal.

It should be noted that as a result of the transistor's on-resistance and the slow switching time due to the parasitic capacitance of the transistor, the use of Class D power amplifier at GHz frequency range is extremely difficult.

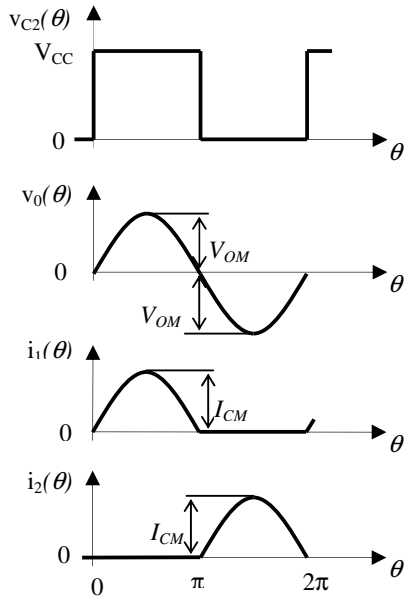
Figure 3.6 Complementary Voltage Switching Class D Power Amplifier



(a) Circuit Implementation



(b) Equivalent Circuit Diagram



(c) Voltage and Current Waveforms

3.3.2 Class E Power Amplifier

Class E power amplifier was first proposed by Sokal[19]. As the non idealities of the transistor as a switch has degraded the performance of Class D power amplifiers, Class E power amplifier has incorporated the non idealities into the design. For example, the parasitic output capacitance; Cds has been absorbed into the shunt capacitor. As a result, the parasitic capacitance is no longer the limiting factor for the operating frequency of the power amplifier.

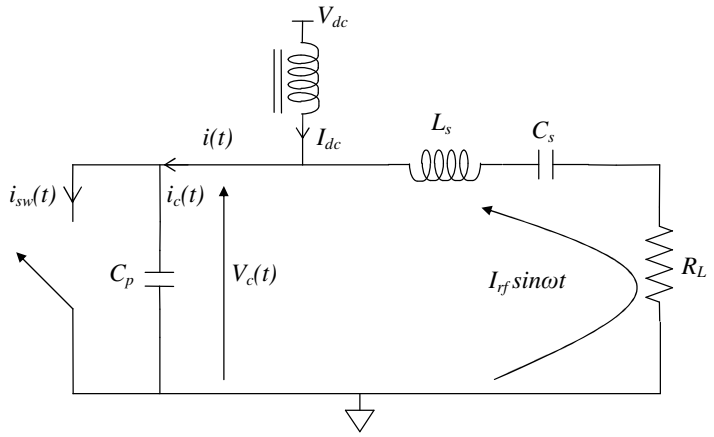
In order to ensure a high efficiency is achieved, the operation of the amplifier has to follow certain conditions, namely the rise of the voltage across the switching transistor at turn-off should be delayed until after the transistor is off and there is no current across the transistor, the voltage across the shunt capacitor should be brought back to zero at the time of transistor turn-on and last but not least, the slope of the voltage across the shunt capacitor should be zero at the time of transistor turn-on.

The circuit implementation and the voltage and current waveforms are shown in Figure 3.7. The zero crossings γ and β shown in Figure 2.7 are solutions for the following equation:

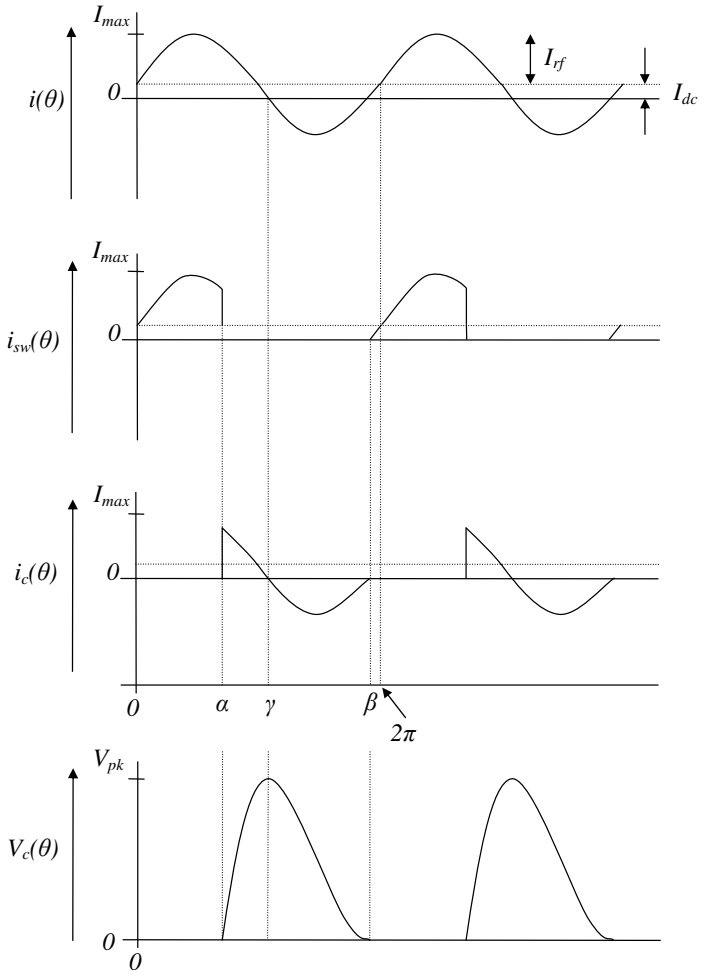
$$\sin(\beta,\gamma) = -\frac{I_{dc}}{I_{rf}} \quad , \tag{3.30}$$

where $\frac{3\pi}{2} < \beta < 2\pi$, $\pi < \gamma < \frac{3\pi}{2}$.

Figure 3.7 Class E Power Amplifier



(a) Equivalent Circuit of Class E Power Amplifier



(b) Voltage and Current Waveforms

The voltage across the shunt capacitor is given by the following equation:

$$v_C(\theta) = \frac{1}{\omega C_p} \int_{(2\pi-\theta)}^{\theta} i_C(\theta)\, d\theta \quad , \tag{3.31}$$

$$\begin{aligned} v_C(\theta) &= \frac{1}{\omega C_p} \left[I_{dc}(\theta - \alpha) + I_{rf}(\cos\alpha - \cos\theta) \right] \quad , \alpha < \theta < \beta \\ &= 0 \qquad\qquad\qquad\qquad\qquad\qquad , \beta - 2\pi < \theta < \alpha \ . \end{aligned} \tag{3.32}$$

The peak drain voltage, $v_{D,\max} = 2\pi V_{DD} \tan^{-1}\left(\frac{2}{\pi}\right) \approx 3.6 V_{DD}$, whereas the peak drain current is approximately $1.7V_{DD}/R$. The maximum output power delivered to the load is

$$P_o = \frac{2}{1+\frac{\pi^2}{4}} \frac{V_{DD}^2}{R} \approx 0.58 \frac{V_{DD}^2}{R} \quad . \tag{3.33}$$

As the peak drain voltage can be as high as $3.6V_{DD,}$ Class E power amplifier does not scale gracefully with the trend towards lower breakdown voltage technologies. Furthermore, the above analysis has based on the assumption that the parasitic output capacitance is independent of the switching voltage. If the non-linearity of the parasitic output capacitance, which makes up of a significant portion of the output shunt capacitance is taken into account, it can be observed that the peak drain voltage tends to go higher as the non-linearity increases [20].

3.3.2 Class F Power Amplifier

The essence of Class F power amplifier is in the output termination matching circuit. The circuit implementation diagram and waveforms are shown in Figure 3.8. The load network consists of a quarter-wavelength transmission line at the fundamental frequency and a shunt parallel tuned circuit. The output tank circuit is tuned to have a resonant frequency at the fundamental operating frequency and is assumed to have a high Q-factor such that it will present a short circuit at all harmonics. The transmission line acts as a quarter wave transformer for the fundamental frequency signal complying with the following equation:

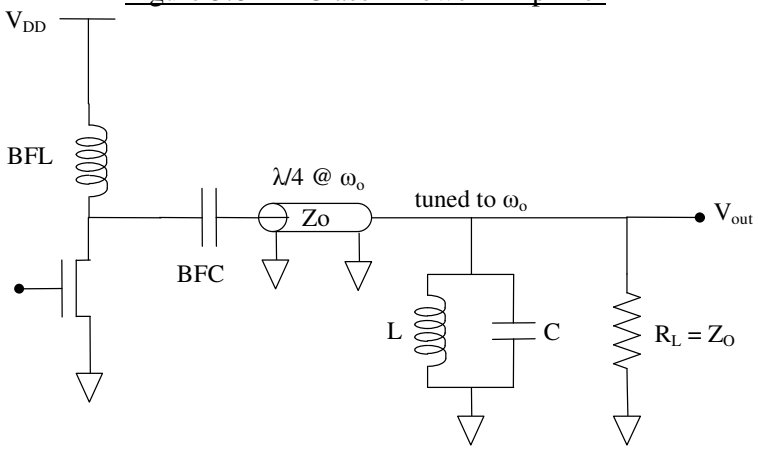
$$Z_{IN} = \frac{Z_O^2}{Z_L} \tag{3.34}$$

It is now our interest to investigate the impedance looking from the drain of the transistor towards the load network at all frequencies. At the fundamental frequency, the drain of the transistor sees a real resistance of Z_O, which is equal to the load resistance of R_L. At all the EVEN harmonics, the drain sees a short circuit. The reason being the transmission line appears as some integer multiple of a half wavelength at all even harmonics that make it acts as a short circuit and also the tank circuit appears to be a short circuit as well. Hence, there will be no even harmonic components for the drain voltage but only even harmonics components for the drain current.

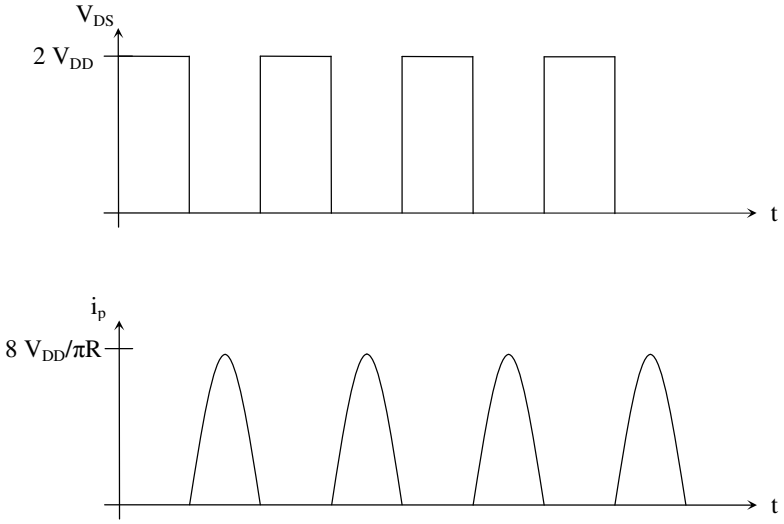
At all the ODD harmonics, the drain sees an open circuit. The reason being the transmission line appears as an odd multiple of quarter wavelength at all odd harmonics that make it acts as an open circuit and also the tank circuit appears to be a

short circuit as well. Hence, there will be no odd harmonic components for the drain current but only odd harmonics components for the drain voltage.

Figure 3.8 Class F Power Amplifier



(a) Circuit Implementation



(b) Voltage and Current Waveforms

It can be inferred that the switch in Class-F power amplifier has even harmonic currents and odd harmonic voltages, the switch will ideally dissipate zero power as the harmonics are orthogonal.

The output power delivered to the load is

$$P_O = \frac{\left[\left(\frac{4}{\pi}\right) V_{DD}\right]^2}{2R} \quad . \tag{3.35}$$

Inverse Class-F power amplifier that shorts the odd harmonics and opens the even harmonics has also been proposed and discussed [21]. However, inverse Class-F power amplifier is not so suitable for low breakdown voltage technologies as the peak drain voltage is higher compared to Class-F power amplifier.

3.4 Literature Review of CMOS Power Amplifiers

There are not many literatures reported on CMOS power amplifiers. One of the earlier CMOS power amplifiers reported is a balanced 20μW to 20mW 900MHz class-C power amplifiers in 1μm CMOS technology in the year of 1994[6]. The amplifier is operating with a 3V power supply and has a measured drain efficiency of 25%. No input matching is used as the power amplifier is going to be integrated with the up conversion mixer. The output matching circuit is off-chip. The output power is programmable by using a binary weighted array of driver MOSFETs that will be selected by switches.

Another power amplifier at the same frequency range (800MHz – 900MHz) but with a much higher efficiency is later reported [7]. The power amplifier is realized using a 0.8μm standard CMOS technology with 2.5V power supply. However, the integration level for this power amplifier is low as the input matching and output matching circuit are all off-chip. The inductors in the inter-stage matching circuit are realized by using bond-wires which has a higher Q-factor compared to on-chip spiral inductor. However, it should be noted that the repeatability of the bond-wire inductance is not very good. The measured PAE is 42%. The amplifier consists of four stages that belong to different classes of operation. First stage is operating at Class A, second stage is operating at Class AB and third stage is operating at Class C. Last but not least, the final stage is operating as Class D amplifier. The final stage transistor has a transistor total width divide by transistor gate length ratio of 8400/1 and on-resistance of 0.5Ω.

A few CMOS Class E power amplifiers have been reported. There is one that uses a novel technique of fulfilling the stringent requirement of input driving signal for Class-E power amplifier. The technique used is mode-locking technique [8]. Mode locking refers to the condition whereby an otherwise self-oscillating circuit is coupled to the amplifier to force it to oscillate at the same frequency as the input driving signal. The Class-E power amplifier has an output power of 1W at 1.9GHz using 0.35μm CMOS technology at 2V power supply. The PAE achieved with off-chip microstrip balun is 41%. The inductors are realized using bond-wires. The differential topology is used to reject the substrate noise coupling and also enable larger voltage swing differentially.

The effect of the quality factor governed by the equation $Q = \omega L/R$, where L is the inductor for the output tuned circuit of a Class-E power amplifier and R is load on the efficiency of the Class-E power amplifier has been studied. It is simulated that the power efficiency decreases with the above mentioned quality factor [22].

For Class E power amplifiers, the drain to bulk capacitance is lumped into the output shunt capacitor. However, the design equations given in [19] have assumed that the capacitance is linear. This is not true for the drain to bulk capacitance in CMOS technology [23], it is actually non linear and changing with the drain voltage. The non-linear effects of the drain to bulk capacitance have been studied and a set of modified design equations has been given [20].

CHAPTER 4

Power Amplifier: Design Implementation & Simulation

This chapter will give a detail description of the design implementation of the power amplifier. The design setup discussed later will include simulation setup and models needed for the design.

4.1 Design Setup

This section will give a more detail description of the technology used and the simulation setup for this project. The simulation setup description will include the models for the components used in the simulations for this project.

4.1.1 Technology

In this project, a standard 0.35um double poly four metal layer (2P4M) salicided CMOS technology is chosen to be the test vehicle for the power amplifier designed. The foundry for this process is Chartered Semiconductor Manufacturing (CSM). Metal one layer up to metal three layers have the thickness of 0.5μm, whereas the top metal has 0.8μm thickness. One of the analog options provided is the MiM (Metal Insulator Metal) capacitor. All the necessary setup files like Design Rule Check

(DRC) file, Extraction file, Layout vs Schematic (LVS) check file technology setup file and etc are provided by CSM and Institute of Microelectronics (IME), Singapore.

4.1.2 Simulation and Layout Tools

The simulation tool used for this project is Advanced Design System (ADS) Version 1.3, a CAD tool by Hewlett-Packacd. The software tool named Cadence Virtuoso Editor Version 4.4.6. is used for circuit layout.

4.1.3 MOSFET Model

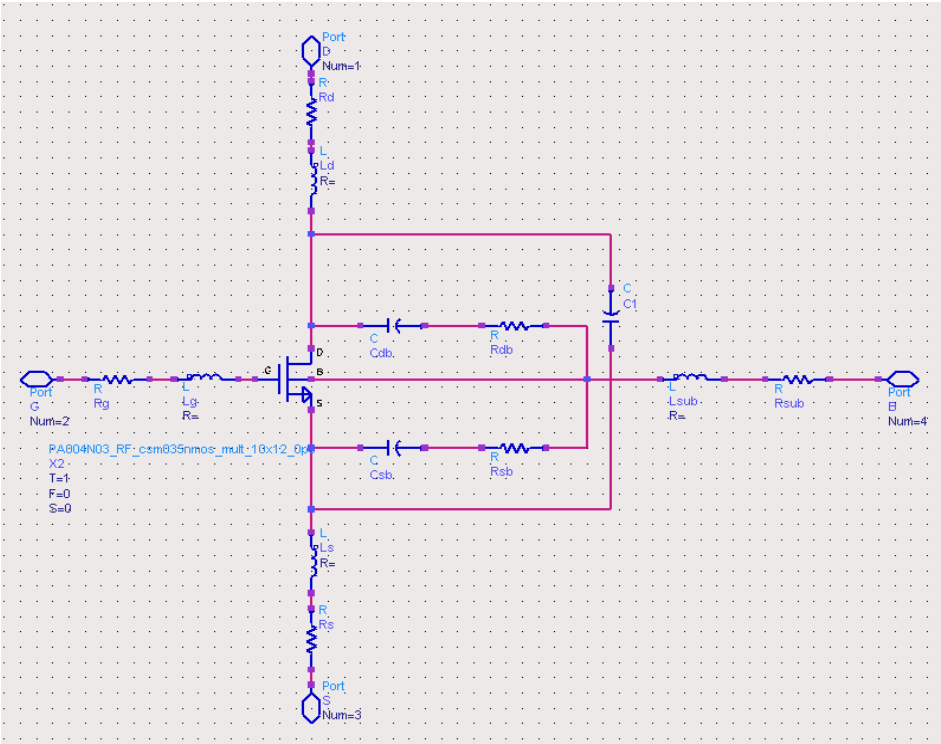
The transistor DC model used in this project is provided by the foundry. The model provided is BSIM3v3 compact MOSFET model. It is a physics-based model that is accurate, smooth, continuous, scalable, predictive and computationally robust over different regions of operation and a wide geometry range. BSIM3v3 considers all major physical effects in deep sub-micron MOSFETs. Its thorough, accurate and functional mathematical representation of MOS device physics, has made BSIM3v3 selected by an international consortium of semiconductor companies as the first industry standard MOSFET model.

The BSIM3v3 model provided by the foundry is only the intrinsic compact model that does not include the RF extrinsic parameters that are important when the operating frequency of the circuit goes up to Giga-hertz frequencies [23]-[27]. The RF extrinsic parameters include source resistance; drain resistance, gate resistance, substrate coupling resistance, source-to-bulk capacitance, and drain-to-bulk capacitance. These above mentioned parameters are going to affect the Scattering

parameters and also the admittance parameters of the transistor at high frequencies. These RF extrinsic parameters can actually be presented by an equivalent sub-circuit representation that is made up of lump circuit elements.

The RF extrinsic parameters represented by the sub-circuit are then added to the intrinsic compact BSIM3v3 model for simulation. The RF extrinsic parameters are extracted as bias independent parameters for our setup. The RF sub-circuit representation is shown in Figure 4.1.

Figure 4.1 Model with RF Sub-circuit

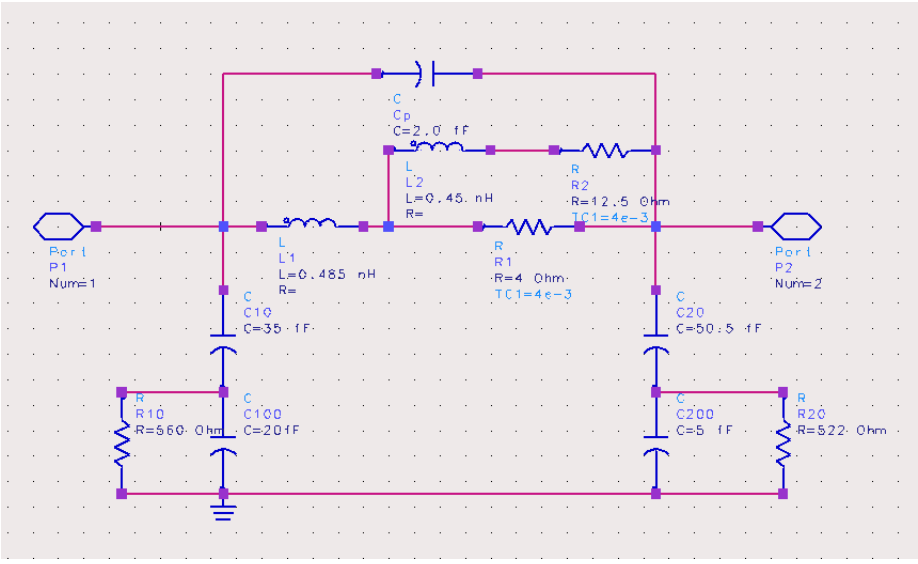


4.1.4 Inductor

The inductor used in this project is layout in spiral circular form using the top two aluminum metal layers (≈1.3µm) as the winding and the bottom two metal layers (≈1.0µm) as the underpass. The width of the winding and the underpass metals is 6µm. The measured quality factor of the inductor is around 4 to 5 at a frequency of 2.45GHz.

The inductor model used in the simulation is an extracted model. The extracted Scattering Parameters are used to construct the lumped circuit model for the inductor. The lumped circuit model is shown in Figure 4.2. The main inductance is represented by L1 in the inductor model. The frequency dependency of the series resistance, R1 is given by L2 and R2 that are parallel to R1. The frequency dependent effects such as Eddy Current and skin depth effect have thus been in co-operated. Capacitors C10 and C20 in the model represent the capacitive coupling to the substrate, whereas Cp includes the resulting effect of inter-winding capacitance and overlap capacitance.

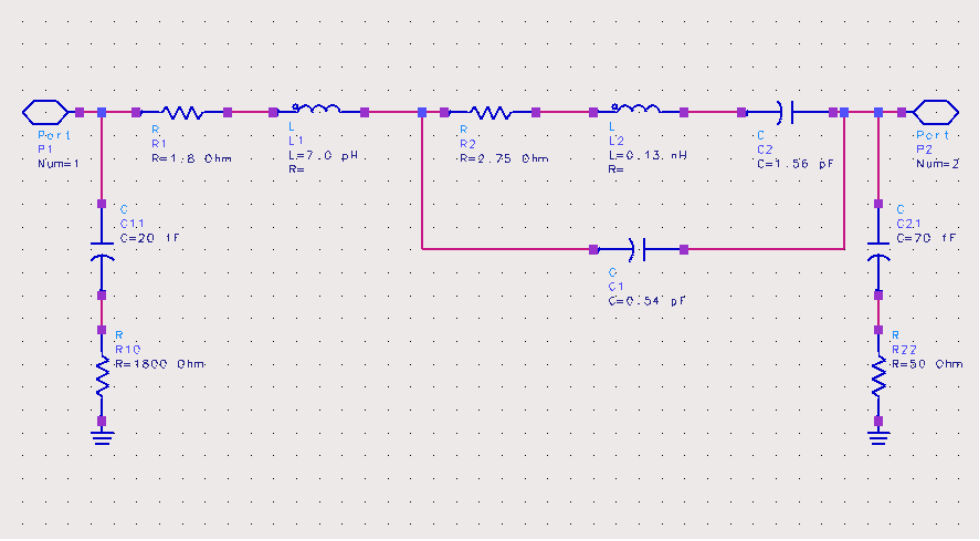
Figure 4.2 Inductor Lumped Circuit Model



4.1.5 Capacitor

The MiM (Metal Insulator Metal) capacitor is used in the matching circuit whereas the inter-poly capacitor is used as the on-chip decoupling capacitor. The inter-poly capacitor that has high unit capacitance is used as the decoupling capacitor because the on-chip decoupling capacitor needs to be as large as possible without occupying too much space. However, as the inter-poly capacitor has a high parasitic capacitance to substrate as well, it is not suitable to be used as a matching element. As for the MiM capacitor, although the unit capacitance is around three times smaller than inter-poly capacitor, its parasitic capacitance is more than ten times smaller. In Figure 4.3, the capacitor lumped circuit model is shown.

Figure 4.3 Capacitor Lumped Circuit Model



4.1.6 ESD Pad Model

Electro-Static Discharge (ESD) Diode protection for the bond pad is included in the design. The junction capacitance of the diode is roughly 0.25pF.

4.2 Specifications

The power amplifier will be design for Bluetooth applications. A Bluetooth system is operating in the 2.4GHz ISM (Industrial Scientific Medicine) band. Majority of the countries around the world use the frequency range of 2400MHz to 2483.5MHz. Channel spacing is 1MHz. The modulation scheme used in Bluetooth is Gaussian Frequency Shift Keying (GFSK), which is a constant envelope modulation scheme. There are three power classes for transmitted power (shown in Table 4.1). However, only two power classes will be focused in this project:

Table 4.1 Bluetooth Power Classes

Power class	Maximum Output Power (Pmax)	Nominal Output Power	Minimum Output Power
2	2.5mW (4dBm)	1mW (0dBm)	0.25mW (-6dBm)
3	1mW (0dBm)	N/A	N/A

Table 4.2 Specifications

Parameter	Condition	Min	Typ	Max	Unit
RF Frequency Range		2.40	-	2.50	GHz
Supply Voltage		2.7	3.0	3.3	
Temperature		-40	25	85	deg
Output Power	Before antenna switch	0	4	8	dBm
	After antenna switch	-2	2	6	dBm
2^{nd} Harmonics Power				-27	dBm
3^{rd} Harmonics Power				-27	dBm
Forward Isolation	Power off	20			dB
Input impedance	Single-ended		100		ohm
Output impedance	Single-ended		50		ohm
Total Current			TBD		mA

The specifications are given in Table 4.2. The output power range is defined under any conditions including temperature range from -40°C to 85°C, supply voltage range from 2.7V to 3.3V and of course any process variations.

The power amplifier designed will then be integrated with other sub-circuits to build a transceiver. As direct modulation scheme is employed, the output of the Voltage Controlled Oscillator (VCO) is fed to the input of the power amplifier. This is to monitor the practicality of the power amplifier designed and the effects of other circuits on the power amplifier. As the Bluetooth system is a TDD system, the antenna switch will be integrated on chip.

4.3 Power Amplifier Design

As Class 2 and Class 3 Bluetooth power amplifiers' maximum output power is 4dBm, there should be no current carrying capability issue for the interconnect metal layers and the winding metal layers of the inductor. As a result, the power amplifier designed will be fully integrated using on-chip spiral inductors and on-chip capacitors.

The modulated signal is an envelope constant signal. Hence, a switch mode power amplifier should be a good choice as the efficiency can be very high. However, it should be noted that the switch mode power amplifiers would need a high Q-factor for the output-tuned network in order to obtain a good quality sine wave at the antenna. This is difficult to achieve, as the Q-factor of the on-chip spiral inductor is low. As a result of careful considerations, switch mode amplifier topology will not be used.

4.3.1 Class AB Design

A two stage Class AB power amplifier topology is employed for its linear operation and moderate efficiency. A Class AB bias transistor has its biasing point in between a Class A bias transistor and a Class B bias transistor. A Class AB bias transistor has its conduction angle between 180° and 360°.

The gate length used for the transistors is 0.35µm, minimum gate length of this technology. The transistor size for 1st stage is 10x8µm and for 2nd stage is 10x12µm. The gate bias voltage (Vgs) for both stages is 1.13V. The DC biasing current is around 12% of I_{DSS} for both transistors. The first stage acts as a pre-amplifier that has enough driving capability to drive the next stage.

The requirements for the power amplifier emphasize on providing constant output power that is between 0dBm to 8dBm under any circumstances. The power amplifier is thus operated beyond its 1dB compression point so that output power remains fairly constant as input power changes

4.3.2 Feedback Circuit

There is a series RC feedback from drain to the gate of the FET for both stages. The values of the feedback resistor and capacitor are tuned until the stability circle is totally out of the impedance unity circle such that the FET itself is unconditionally stable. Stability factor also shows that the transistors are stable from DC to 3rd harmonic frequency. For the first stage feedback, *Cfb1* = 2pF and *Rfb1* = 2000 Ohm. As for the second stage feedback, *Cfb2* = 2pF and *Rfb2* = 4000 Ohm. This type of

feedback configuration will only reduce the AC gain but the DC gain will still maintained. Hence, the DC current will not be increased.

4.3.3 Matching Circuit

The optimum source and load impedance of the transistors (shown in Table 4.3) used is simulated using load-pull and source-pull simulation setup. The impedance obtained using Harmonic Balance (HB) simulation is the large signal impedance. The optimum impedance is obtained through the trade-off of mainly the output power and efficiency. As the linearity specification is not so stringent for Bluetooth, it is only verified after choosing the optimum impedance but not taken into consideration during the load-pull and source-pull simulation.

Table 4.3 Optimum Source and Load Impedance

FET size	Source impedance	Load impedance
10x8um	87.9-j*205.55	41.45-j*80.45
10x12um	67.75-j*183.05	47.65-j*86.85

The matching circuits are designed based on the simulated optimum source impedance and load impedance of the 1st stage transistor and 2nd stage transistor.

The input matching circuit comprises of one capacitor, *Cin* and one inductor, *Lin* in series. *Cin* mainly serves as the DC block capacitor. *Lin*, together with its parasitic resistance serves as the matching component. The inter-stage matching circuit only consists of a RF choke inductor, *Ld1* at the drain of the input transistor and an AC coupling capacitor, *Cint,* the value of which is chosen to transfer as much RF power as possible to the second stage.

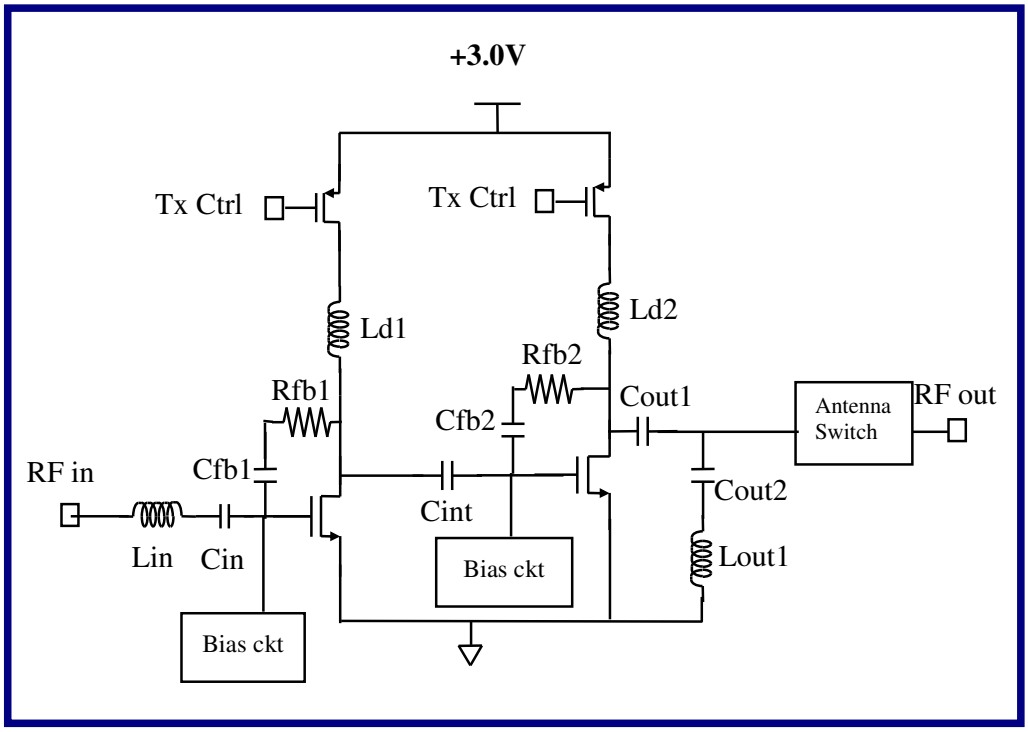
At the output stage, the matching circuit is made up of a ∏-network with a shunt inductor, *Ld1*, followed by a series AC coupling capacitor, *Cout1* and followed by a shunt network comprised of a LC series resonant tank, *Cout2 and Lout1* that resonates at 2nd harmonic. This is to suppress the 2nd harmonic at the output. In actual implementation, as the Q-factor of the LC series resonant tank is low, the resonant tank is designed to resonate at a frequency slightly higher than the 2nd harmonic such that the frequency response at the fundamental frequency is not affected. Of course, the tank circuit would help to suppress a certain amount of 3rd harmonics power.

The two inductors (*Ld1* and *Ld2*) used as the RF choke at the drain of the transistors are implemented on chip. Since their Q-factors are low (around 4-5), high inductance values would mean high series resistance values. As a result, the inductance of the on chip inductors could not be very high. Therefore, the inductors could not act as an ideal RF choke and has to be one of the components in the matching circuit.

The schematic of the fully integrated two-stage Class AB power amplifier (Version 1) with all the matching circuit is shown in Figure 4.4. The simulation results for the power amplifiers with all the corner conditions, temperature variations and supply voltage variations will be shown in Section 4.3.8. There are two corner conditions being simulated, namely fast corner and slow corner. There are altogether 24 scenarios or variations available. However, to simulate all 24 scenarios will be very time consuming. As a result, only scenarios with extreme results will be simulated. One extreme corner simulation corresponds to fast P channel and N channel transistor, maximum supply voltage (3.3V) and minimum temperature (-40 deg). Another

extreme corner simulation corresponds to slow P channel and N channel transistor, minimum supply voltage (2.7V) and maximum temperature (85 deg).

Figure 4.4 2-Stage Power Amplifier Schematic



It should be mentioned that the peak drain voltage in this design is kept to be $1.5V_{DD}$ instead of 2_{VDD} due to low breakdown voltage and hot carrier effects in CMOS technology. Some margin is given such that the power amplifier will still be functioning under any circumstances, including temperature changes and process variations. From equation (3.22), it can be observed that if the peak drain voltage is reduced, the peak drain current has to be increased in order to obtain the same output power. As a result, the DC drain current is also being increased according to equation (3.19).

4.3.4 Temperature Effects

From Section 2.2.3 in Chapter 2, it is known that the power gain of the transistor reduces as the temperature increases. Also, the resistance in interconnects is directly proportional to temperature. In order to counteract this phenomenon, the gate biasing has to increase as the temperature increases.

The gate biasing circuit of the power amplifier (shown in Figure 4.5) consists of a Proportional to Absolute Temperature (PTAT) Current Biasing circuit (shown in Figure 4.6) that provides a current source to a simple voltage reference circuit. This voltage reference will not try to keep a constant voltage across temperature. Instead, the idea here is to produce a voltage reference, which is the gate voltage that increases with the increment of temperature to keep the Pout as constant as possible across temperature. The voltage reference is achieved from a MOSFET (M1) and a single resistor (R3). A MOSFET is used because it has a smaller negative temperature coefficient compared to a BJT. The size of the MOSFET is also chosen to minimize the effects caused by process variations. The gate length is chosen to be 0.35μm while the unit gate width is chosen to be 10μm; which is the same as the power transistors. With the same gate width and gate length, the MOSFET can track the threshold voltage variation as well as other process variations of the power transistors.

The gate voltage equals

$$V_{gate} = V_{GS1} + \frac{R_3}{R_1} V_T \ln N \quad , \tag{5.1}$$

Figure 4.5 Gate Biasing Circuit

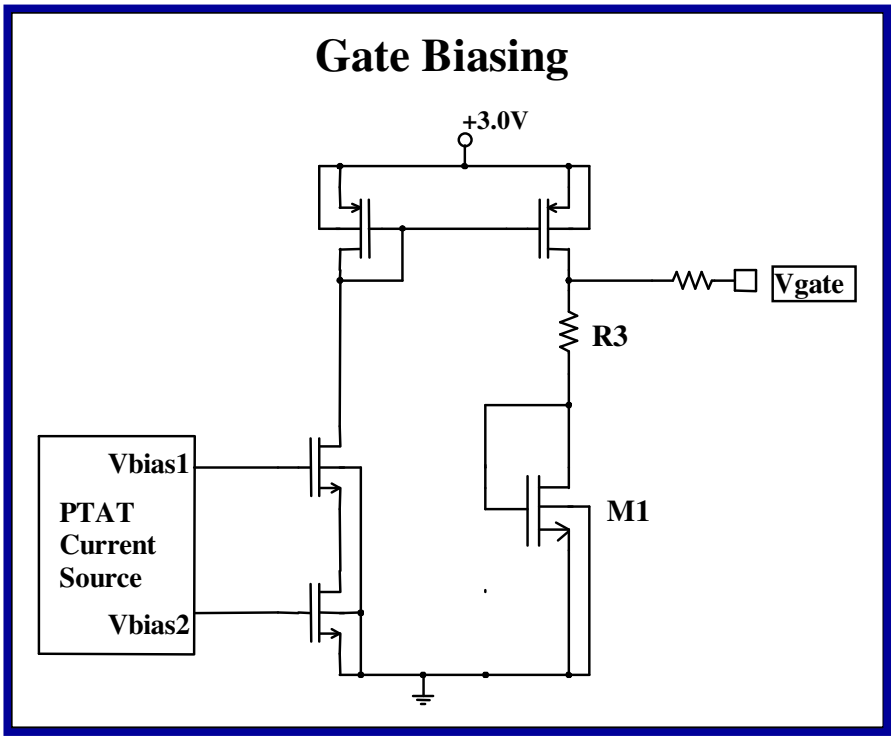
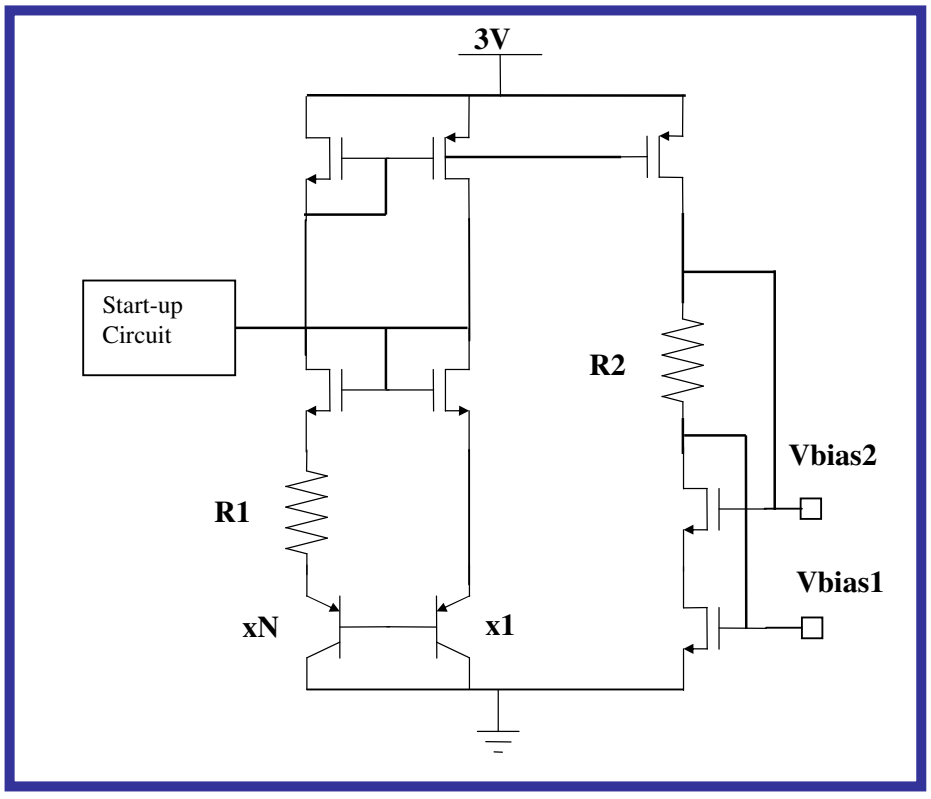


Figure 4.6 PTAT Biasing Circuit



4.3.5 Cascode Output Stage

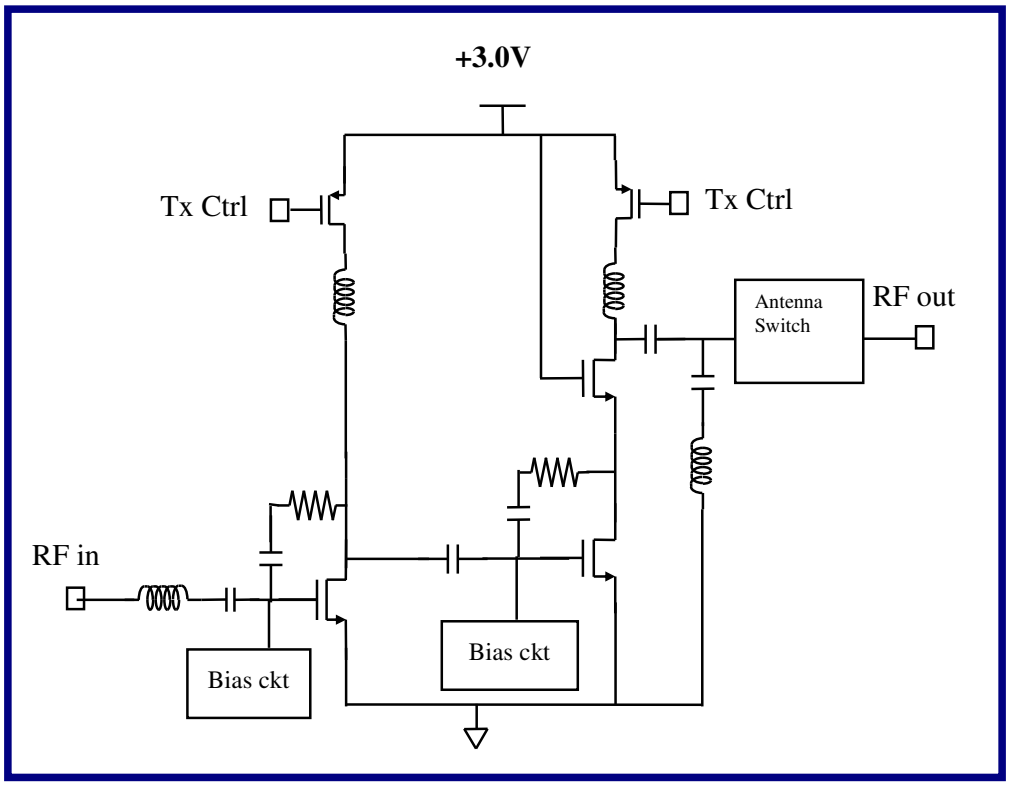
There are some reliability issues that need to be taken notice of. The low breakdown voltage limits the drain voltage to be $2V_{DD}$. For the design in the previous section (Version 1), although the peak drain voltage does not reach 2 V_{DD}, large gate-drain voltage can still degrade the tranconductance over the time as a result of hot carrier effect. To overcome the above-mentioned issue, a cascode structure is used at the output stage of the power amplifier for the second version.

The signal is fed into the gate of the bottom transistor of the cascode structure when the gate of the top transistor is biased at supply voltage, which is 3.0V. A decoupling capacitor has to be placed as close as possible to the gate of the top transistor to avoid un-stability. The transistor size of the top transistor and the bottom transistor is designed to be of the same. In this case, the transistor size is 10x12μm. By using the cascode structure, the voltage swing at the drain can go up to as high as $2V_{DD}$ if necessary.

As the peak drain voltage goes up to $2V_{DD,}$ the peak drain current can be reduced to maintain the same output power according to equation (3.22). As a result, the DC drain current is being reduced. Other advantages of designing a cascode output stage are stability of the power amplifier will be further improved and the reversed isolation and forward isolation will be improved as well.

The schematic of the fully integrated two-stage Class AB power amplifier with cascode structure for output stage (Version 2) including all the matching circuit is shown in Figure 4.7.

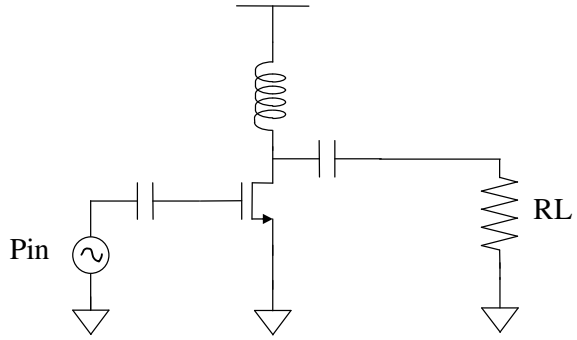
Figure 4.7 2-Stage Power Amplifier Schematic (Cascode Structure)



4.3.6 Power Amplifier with Copper Top Metal & Copper Inductor

Due to the low Q-factor of the inductors used in the matching circuit, the insertion loss of the input matching circuit, inter-stage matching circuit and output matching circuit is average 2dB to 3dB each. This loss has greatly reduced the efficiency of the power amplifier designed. To further illustrate this effect, one example will be given. For example, a transistor as shown in Figure 4.8 is simulated with ideal inductor with its input and output matched with optimum source and load impedance. The drain efficiency simulated would be 49%. However, when the ideal inductor is changed to the extracted inductor model, the simulated drain efficiency would drop to 25%, which is halved.

Figure 4.8 An Example of Single Stage Amplifier



In order to improve the PAE of the power amplifier, the Q-factor of the inductor has to be improved. In order to improve the Q-factor of the inductor, resistive loss and substrate loss has to be reduced. If resistive loss of the inductor were to be reduced, one can increase the winding aluminum metal thickness by using more metal layers for the inductor winding. However, as more metal layers are used, the lowest metal layer will be closer to substrate and thus increasing the capacitive coupling to the substrate. This will again reduce the Q-factor. As a result, whether the Q-factor of the inductor will be improved is questionable. Another method is to use another metal material that has lower resistivity compared to aluminum. One of the popular choices would be copper. Aluminum has a resistivity of about 1.6 times the resistivity of copper.

The third version (Version 3) has used the copper as the top metal layer for interconnect and for the inductor winding. The copper metal thickness is around 2μm whereas the two top aluminum metal layers have only 1.3μm thickness. The Q-factor of the copper inductor is around 100% higher compared to the aluminum inductor. Chartered Semiconductor Manufacturing (CSM) would process the wafer fabrication

up to metal three and via between metal three and metal four. The post processing of Copper metallization will then be done by the Semiconductor Process Technologies (SPT) Lab in IME. For the third version, the circuit is the same as the first version described in Section 4.3.1 to Section 4.3.3; but with the inductors and interconnects using copper metallization. There is no inductor model available at the time of design. As a result, no simulation is performed for this version. However, the measurement results of the power amplifier with copper inductors will be compared with the versions with aluminum inductor.

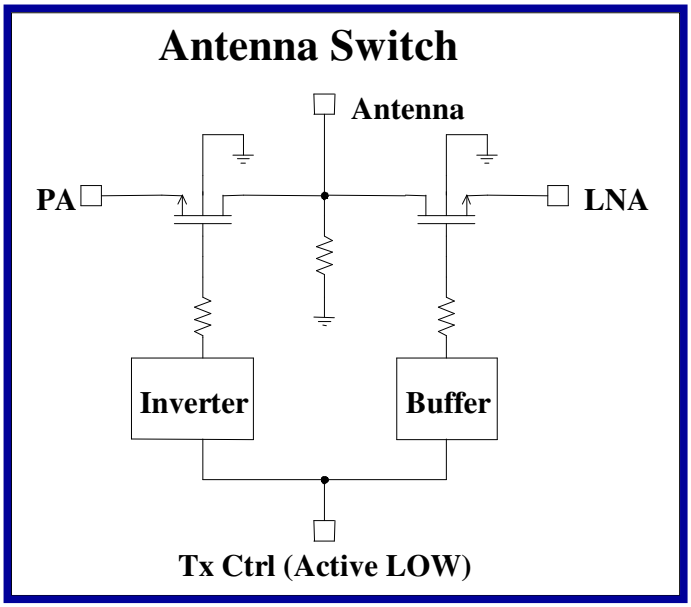
4.3.7 Antenna Switch Design

Although the design of antenna switch is not the main focus in this project, however it is important for the power amplifier if both of them were to be integrated in a transceiver. The insertion loss of the antenna switch will determine the power level to be transmitted through the antenna.

A single ended FET switch is designed (shown in Figure 4.9). This SPDT switch consists of only two MOSFETs with the same size. One FET is to switch PA to antenna and another FET is to switch antenna to LNA. There is a larger resistor (20Kohm) to ground at the junction where the two MOSFETs meet with each other to provide a good DC ground. There is also a resistor (5Kohm) at each of the gate of the MOSFET to prevent RF leakage to the control line. This design has ensures minimum insertion loss while satisfying the isolation specification which is not stringent as Bluetooth transceiver has half-duplex operation which does not require high isolation for antenna switch. The layout of the MOSFET used in switch circuit has single-line of contacts in the source and drain region. This is to reduce the parasitic capacitive loss to

ground. However, by having narrower drain and source, the parasitic drain resistance and source resistance will be more. Hence, an optimum MOSFET size has to be determined to get the most benefit out of having narrower drain and source.

Figure 4.9 Antenna Switch Schematic



4.3.8 Simulation Results

There are altogether three versions designed in this project. Their descriptions are stated in Table 4.4.

Table 4.4 Different Power Amplifier Versions

No.	Description	Issues Addressed
Version 1	Two stage Class AB	-
Version 2	Two stage Class AB with Cascode Output Stage	low breakdown voltage, hot carrier effect
Version 3	Two stage Class AB with Copper Top Metal	low Q inductor

For all the simulations with the results shown, the antenna switch is included in the simulation. The summary of the simulation results of Version 1 is shown in Table 4.5. The simulations are done across frequency (2.4 GHz – 2.5GHz), across temperature (-40 deg – 85 deg), across supply voltage (2.7 V – 3.3 V) and across process corner. Typical small signal power gain is 15.1dB. The gain is low for a two stage amplifier. This is due to the low Q-factor on-chip inductors, which have caused a significant amount of power loss by their parasitic resistance.

The plot of the output power (fundamental, 2nd harmonic, 3rd harmonic) versus input power is shown in Figure 4.10. The plot of the power gain versus input power is shown in Figure 4.11. The simulation of output power versus temperature for Version 1 is shown in Figure 4.12.

Table 4.5 Simulation Summary of 2 Stage Class AB Power Amplifier (Version1)

Parameter	Condition	Min	Typ	Max	Unit
RF Frequency Range		2.40	-	2.50	GHz
Supply Voltage		2.7	3.0	3.3	
Temperature		-40	25	85	deg
Output Power	Before antenna switch	-	-	-	dBm
	After antenna switch	0.8	3.8	6.2	dBm
2nd Harmonics Power		-42.4		-26.7	dBm
3rd Harmonics Power		-44.0		-31.6	dBm
Forward Isolation	Power off	42		48	dB
S21		10.3	15.1	19.1	dB
S11		-14.3	-12.6	-10.6	dB
S22		-12.8	-10.6	-9.8	dB
Input impedance	Single-ended		50		ohm
Output impedance	Single-ended		50		ohm
Total Current		12.1	13.3	16.9	mA

Figure 4.10 Output Power versus Input Power (Version 1)

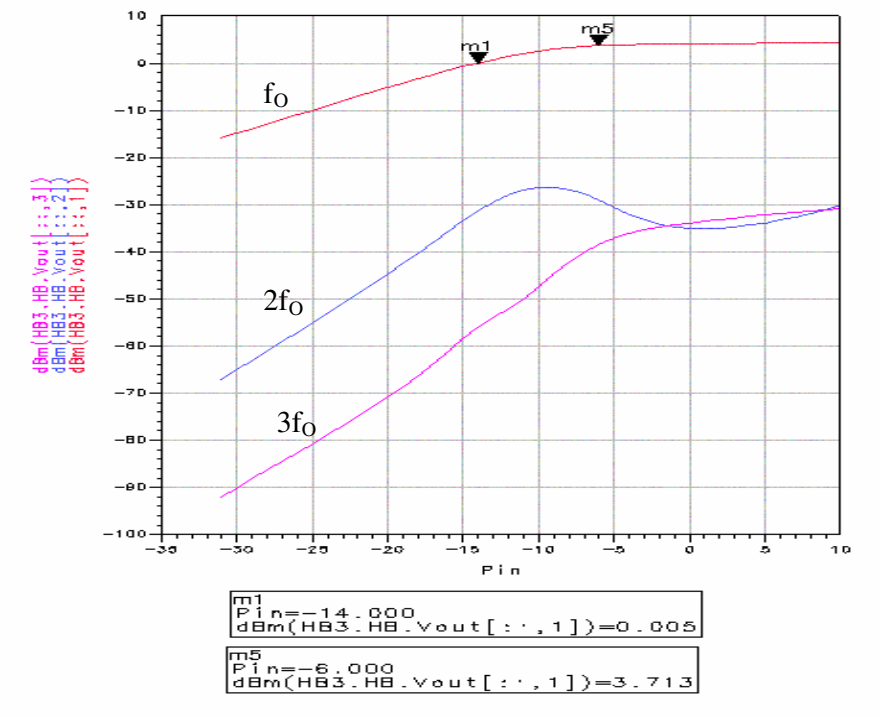


Figure 4.11 Gain Compression (Version 1)

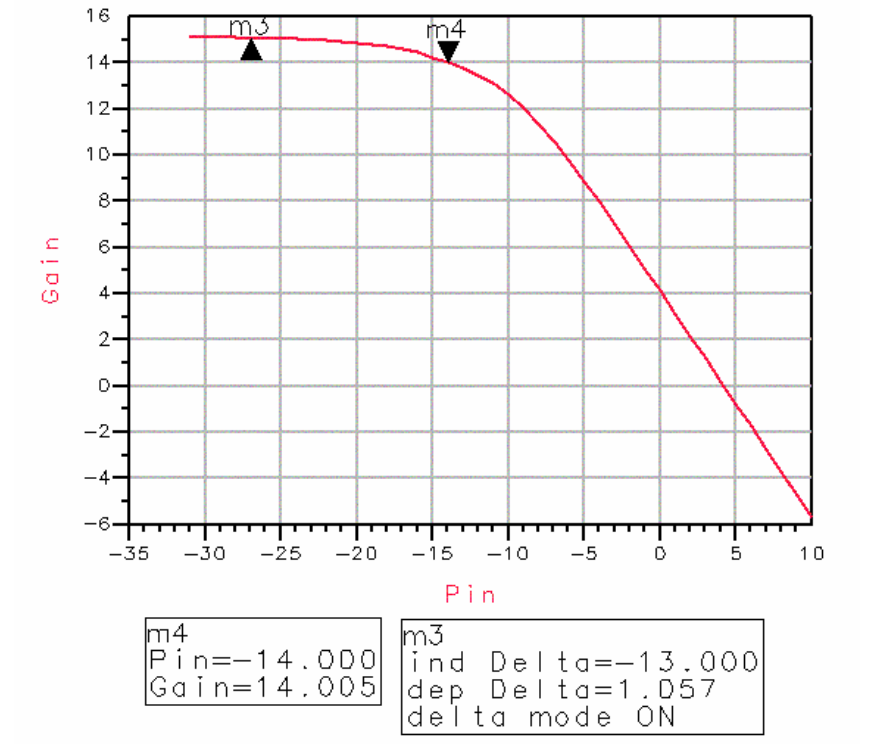
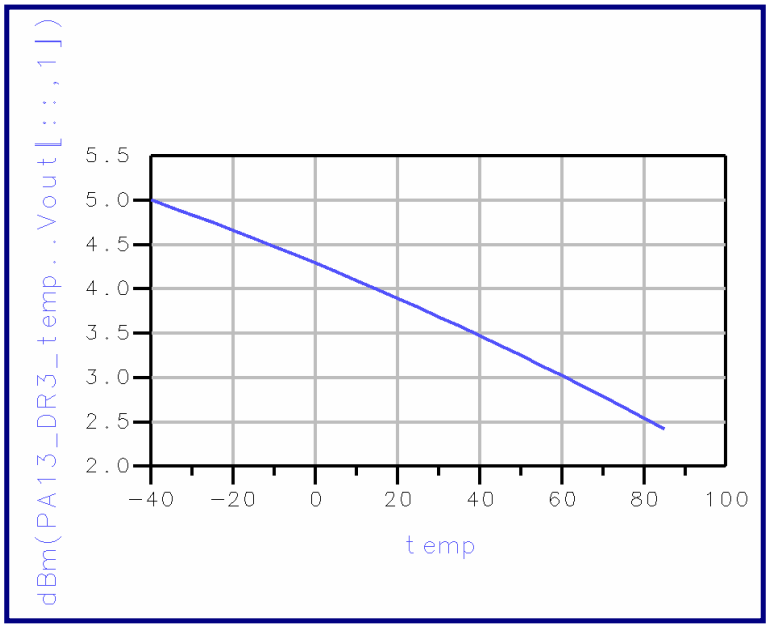


Figure 4.11 Output Power vs Temperature (Version 1)



The summary of the simulation results of Version 2 is shown in Table 4.6. The plot of the output power (fundamental, 2nd harmonic, 3rd harmonic) versus input power is shown in Figure 4.13. The plot of the power gain versus input power is shown in Figure 4.14. The simulation results of Version 2 are very similar to Version 1. The main difference is the current consumption of Version 2 is lower. The cascade structure has enable higher drain voltage swing with reliability ensured, as the voltage swing for common source structure has to be kept lower to avoid hot carrier effect.

Table 4.6 Simulation Summary of 2 Stage Class AB Power Amplifier with Cascode Output Stage (Version 2)

Parameter	Condition	Min	Typ	Max	Unit
RF Frequency Range		2.40	-	2.50	GHz
Supply Voltage		2.7	3.0	3.3	
Temperature		-40	25	85	deg
Output Power	Before antenna switch	-	-	-	dBm
	After antenna switch	1.2	3.7	6.2	dBm
2nd Harmonics Power		-31.9		-26.6	dBm
3rd Harmonics Power		-42.0		-28.4	dBm
Forward Isolation	Power off	42		49	dB
S21		9.7	13.9	19.9	dB
S11		-11.1	-10.4	-9.6	dB
S22		-11.7	-10.9	-10.3	dB
Input impedance	Single-ended		50		ohm
Output impedance	Single-ended		50		ohm
Total Current		10.4	12.0	16.9	mA

Figure 4.13 Output Power versus Input Power (Version 2)

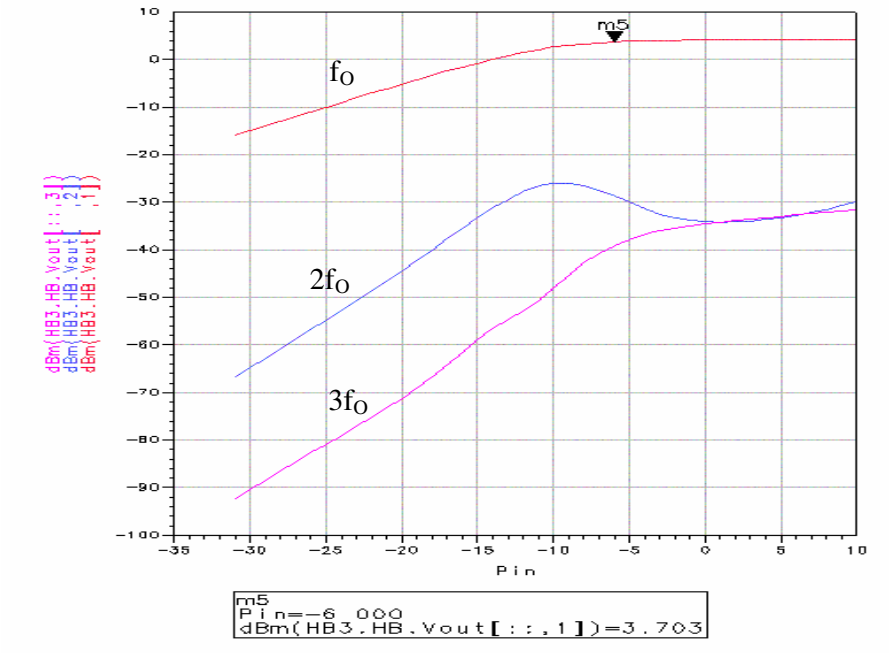
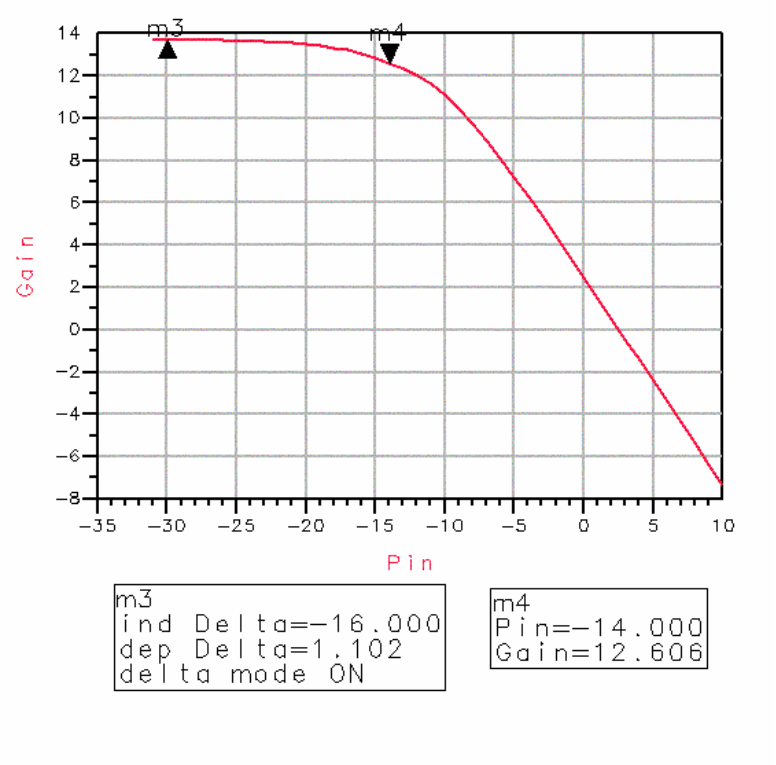


Figure 4.14 Gain Compression (Version 1)



The simulation results of the antenna switch alone are tabulated in Table 4.8. It is observed that the antenna switch with MOSFET size of 10x18µm gives the lowest insertion loss for the switch. Hence, this particular FET size is chosen to be the antenna switch that is integrated with the power amplifier for all the other simulations.

Table 4.8 Simulation Results of Antenna Switch

FET size	Insertion Loss (dB)		Isolation (dB)	
	Spec	Simulated	Spec	Simulated
10x8µm	1.5	2.31	15	49.7
10x12µm	1.5	1.91	15	45.8
10x18µm	1.5	1.55	15	39.6
10x24µm	1.5	2.02	15	33.9

The detailed schematic diagrams of both Version 1 and Version 2 are shown in Appendix. The transistor sizes and the passive components values are shown in the schematics.

The die photo for Version 1 is also shown in Appendix. The die size is 870µm x 1600µm for all the three versions.

CHAPTER 5

Measurements and Results

This chapter will describe the measurement setups for the testing of the power amplifiers designed. The measurement of the power amplifier is performed as on-wafer measurement. The measurement results will be presented in comparison to the simulation results.

5.1 Measurements

5.1.1 On-wafer Measurement

A complete customized Cascade Microtech RF/Microwave test system includes a Summit series probe station, patented Air Coplanar® RF Probes, NIST-verified Impedance Standard Substrates (ISS), powerful Nuceus Prober Control and WinCal Calibration Software, as well as a complete line of accessories are used for the on-wafer measurement. Cascade's WinCal Calibration Software provides the simplest, most accurate, repeatable, network analyzer calibrations for precision on-wafer measurements. Cascade's WinCal Calibration Software offers the Line-Reflect-Reflect-Match (LRRM) calibration with load-inductance compensation.

The pitch size of the RF probes is 150μm. The configuration of the probes used includes Ground-Power-Ground-Signal-Ground (GPGSG), Ground-Signal-Ground-Power-Ground (GSGPG) and Ground-Signal-Ground (GSG).

One of the problems with probing an aluminum pad is that a layer of aluminum oxide will grow on the pad surface when it is exposed to air. This leads to not only higher contact resistance but also variable contact resistance over the time. In order to overcome this problem, a tungsten probe tip has to be used for good measurement repeatability

.

5.1.2 Measurement Setup

Power Measurement

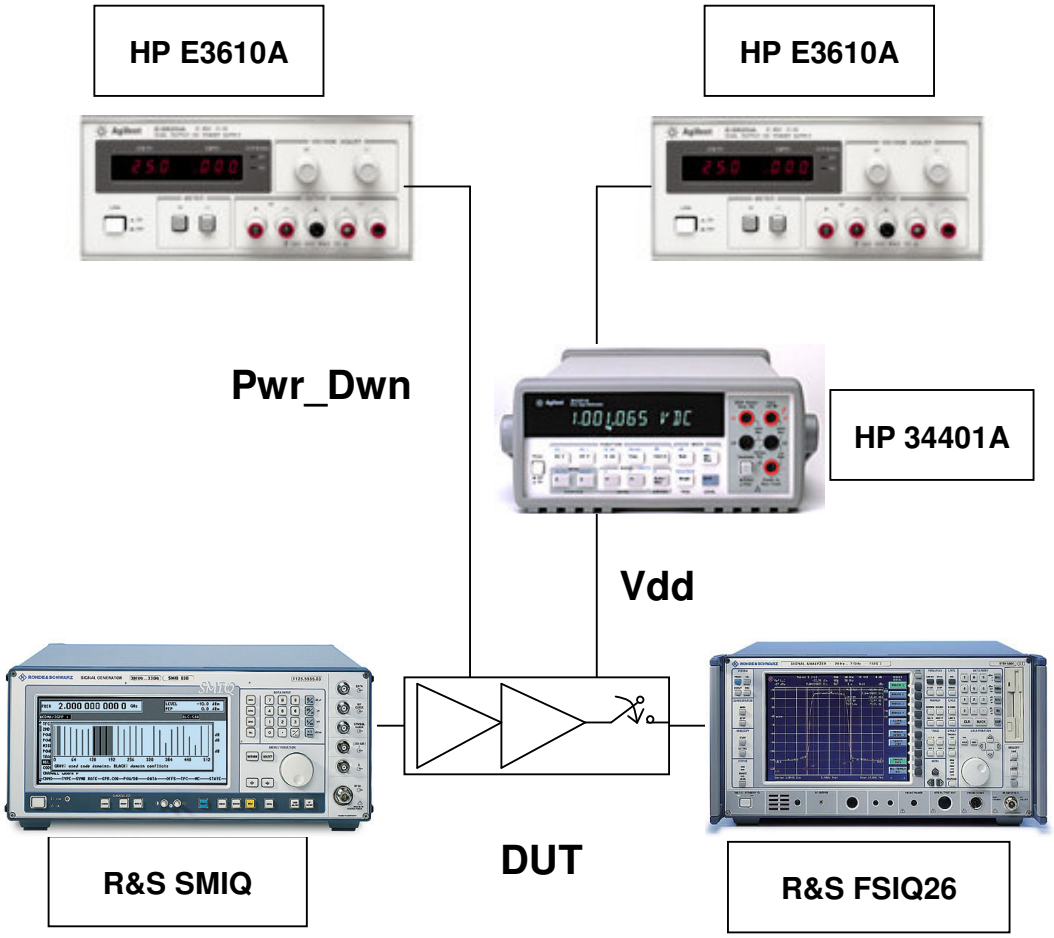
The measurement setup for power measurements including fundamental, 2nd harmonics and 3rd harmonics power measurements and 1dB compression point measurements is shown in Figure 5.1.

The equipments used for the power measurements include Rohde&Schwarz (R&S) FSIQ26 Signal Analyzer, R&S SMIQ 03B Signal Generator, Hewlett-Packacd (HP) E3610A Power Supply and HP 34401A Multimeter. The FSIQ26 Signal Analyzer has a total measurement uncertainty of 1.5dB up to 7GHz. The power measurement results using FSIQ26 have been compared with the measurement results using HP 436A Power Meter. The output power measured using these two equipments has a maximum difference of 0.3dB-0.4dB. Hence, FSIQ26 is used for the measurements since it enables the harmonics to be measured easily as well. The

settings of FSIQ26 are kept constant for all the measurements. The resolution bandwidth is kept 100 kHz and the video bandwidth is kept 10 kHz.

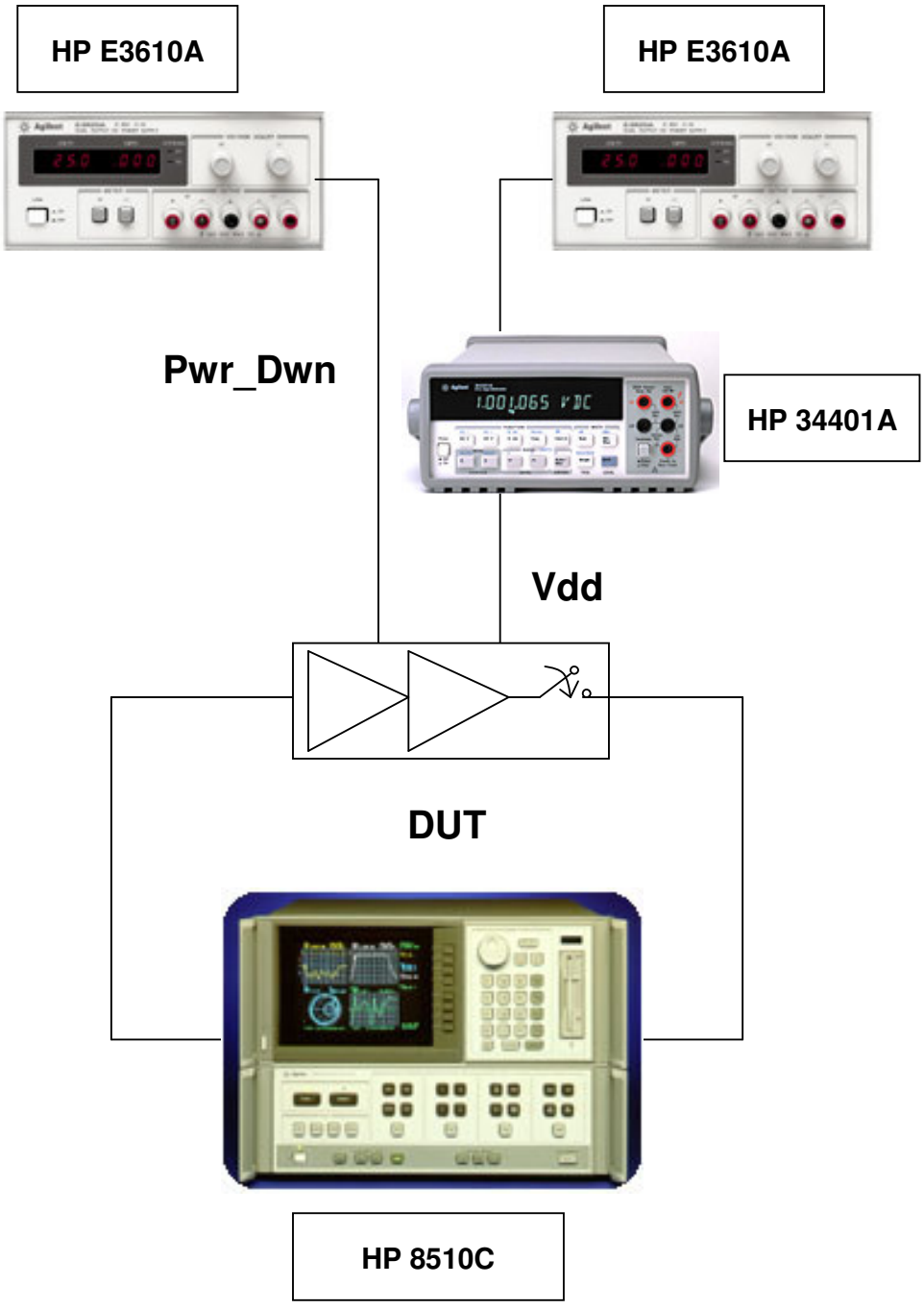
In order to obtain accurate measurement results, the insertion loss from the connector, cable down to the probe tip for both input side and output side is being de-embedded. The insertion loss is roughly 1.3dB at the input side and output side respectively.

Figure 5.1 Measurement Setup for Power Measurement



S-Parameter Measurement

Figure 5.2 Measurement Setup for S-Parameter Measurement



The measurement of Scattering (S) Parameters is performed using the following equipments, HP 8510C Vector Network Analyzer, E3610A Power Supply and HP 34401A Multimeter. (Shown in Figure 5.2)

Line-Reflect-Reflect-Match (LRRM) full two-port broadband calibration has to be performed first before the actual measurement.

5.2 Measurement Results

Detail measurement results will be shown in the following section and in the Appendix. The chip layout will also be shown in the Appendix.

5.2.1 Version 1 On-wafer Measurement Results

Table 5.1 Measurement Results Summary (Version 1)

Parameter	Condition	Simulation	Measurement	Unit
RF Frequency Range		2.45	2.45	GHz
Supply Voltage		3.0	3.0	V
Temperature		25	25	deg
Output Power	After antenna switch	3.8	3.8	dBm
2^{nd} Harmonics Power		-26.7	-22.8	dBm
3^{rd} Harmonics Power		-38.6	-35.7	dBm
Forward Isolation	Power off	42	41	dB
S21		15.1	14.6	dB
S11		-12.6	-10.7	dB
S22		-10.6	-12.0	dB
Input impedance	Single-ended	50	50	ohm
Output impedance	Single-ended	50	50	ohm
Total drain Current		13.3	14.8	mA

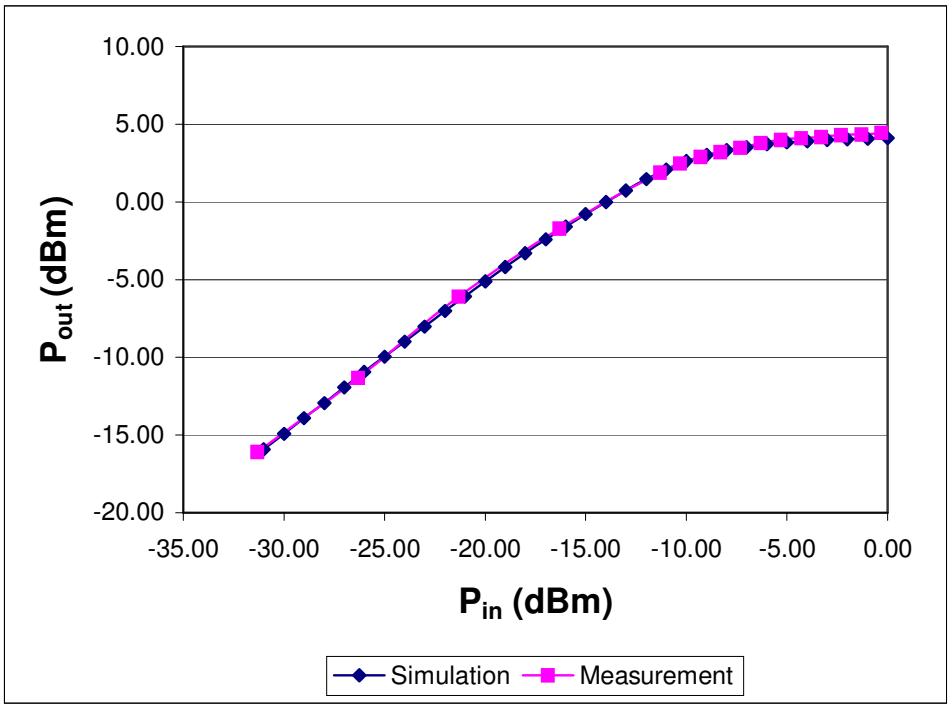
The measurement results summary for typical condition is shown in Table 5.1. Typical condition means temperature at room temperature and supply voltage at 3.0V. The measurement output power is 3.8dBm with input power, -6dBm, which is the same as simulation. However, after measuring a few samples, it is found that the output power ranges from 3.6dBm to 3.8dBm. The total measured DC drain current at this output power is around 11% higher than simulation. The discrepancy in the current may be due to the tolerance of the MOSFET transistors in the power amplifier and the tolerance of the resistor in the PTAT biasing circuit.

Figure 5.3 shows the plot of the comparison between measurement and simulation of the fundamental output power versus the input power. The discrepancy between the simulation and measurement is small. The 2^{nd} harmonic power measured is 3.9dBm higher than the simulated value whereas the 3^{rd} harmonic power measured is 2.9dBm higher than the simulated value as shown in Table 5.1. It can be stated that the discrepancies between simulation and measurement of the harmonics are greater. There may be two reasons causing the discrepancies:

- When extracting the RF extrinsic sub-circuit parameters in the transistor model. Some curve fitting has been done. More emphasis has been put on fitting the parameters at fundamental frequency rather than the harmonics.

- The RF extrinsic sub-circuit elements in the RF transistor model used in this design are bias independent. In actual fact, they are bias dependent and non linear.

Figure 5.3 Comparison of Pout versus Pin (Version 1)



The comparisons of the simulated and measured S-parameters are shown in Figure 5.4. The measured small signal forward transmission gain (S21) is 14.6dB, while the simulated S21 is 15.1dB at 2.45GHz frequency. The simulated S21 is 0.5dB higher than the measured S21. By looking at the input reflection coefficient (S11) and output reflection coefficient (S22), it can be concluded that there is no frequency shift in the frequency response. The measured reversed isolation (S12) has 10dB degradation compared to the simulation. The cause of this degradation might be due to the coupling of the output signal back to the input of the power amplifier through the substrate.

Figure 5.4 Comparison of S-Parameters (Version 1)

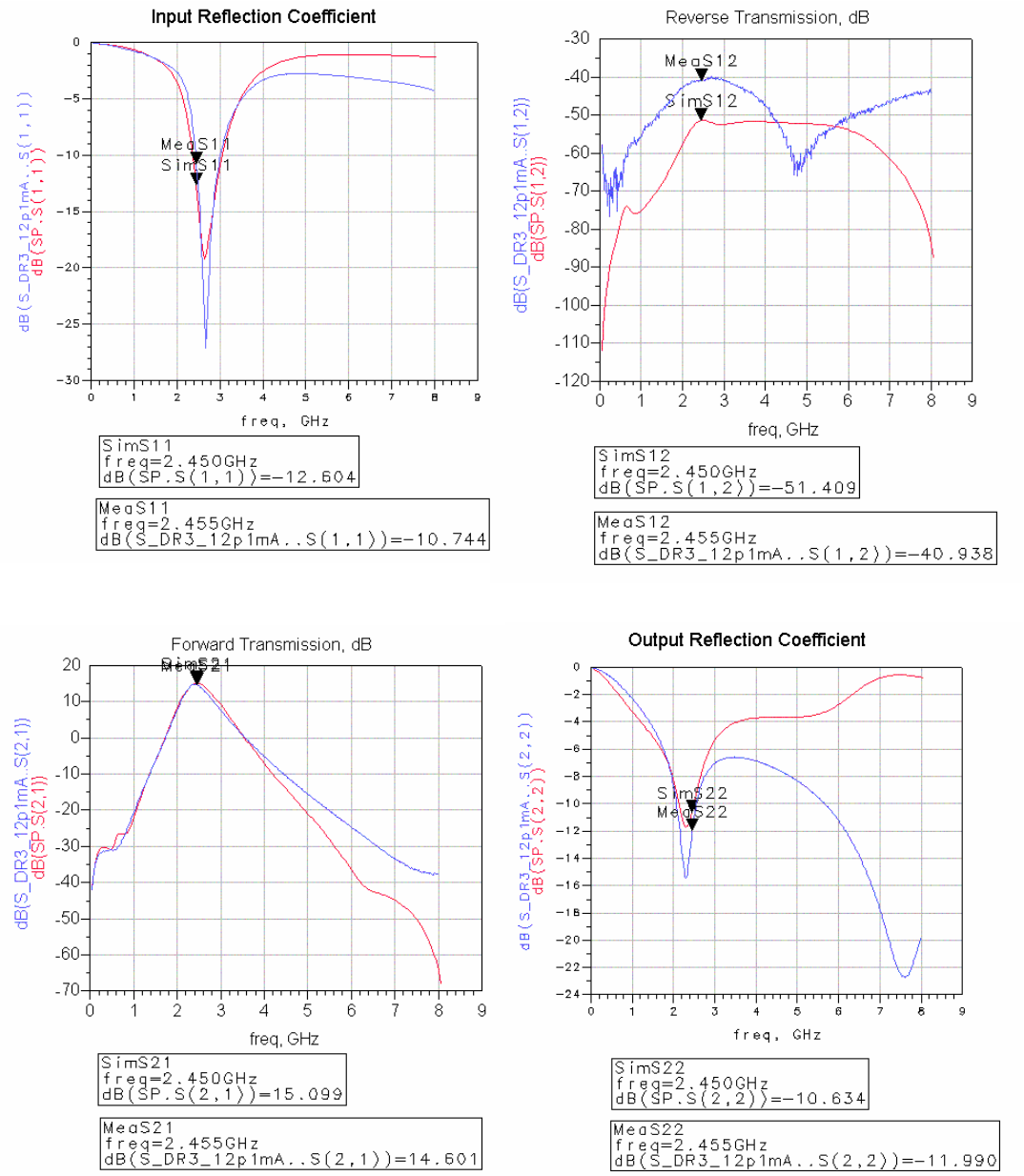
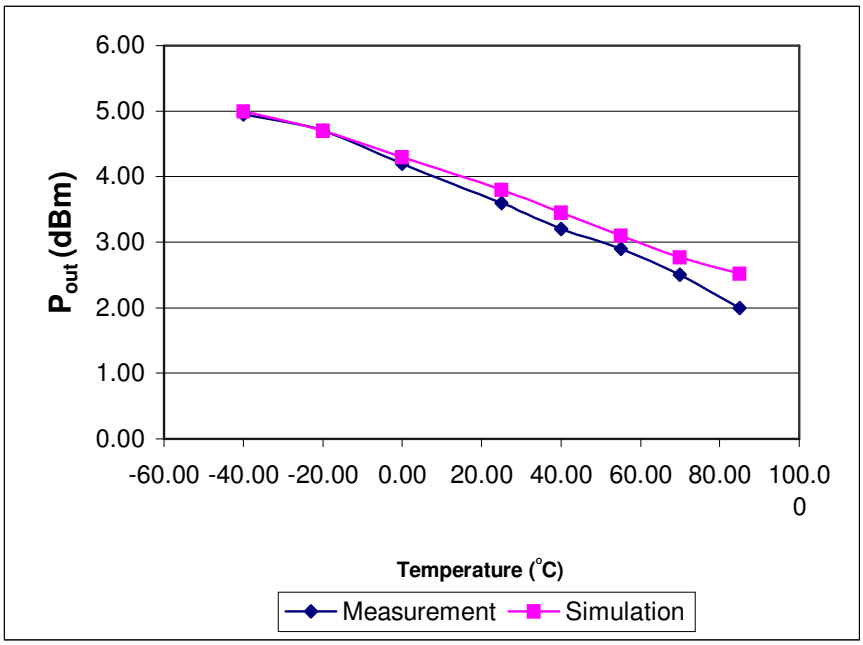


Figure 5.5 Comparison of Pout versus Temperature



In Figure 5.5, a comparison between the simulation and measurement of output power versus temperature is illustrated. It is shown that the output power only changes by 3dBm for the whole temperature range.

5.2.2 Version 2 On-wafer Measurement Results

The measurement results summary for a typical condition is shown in Table 5.2. The plot of the comparison between measurement and simulation of the fundamental output power versus the input power is shown in Figure 5.6. The comparisons of the simulated and measured S-parameters are shown in Figure 5.7.

It must be highlighted that there is a 15% reduction in the DC drain current for this version compared to Version 1. The reason for the reduction has been stated clearly in Chapter 4, Section 4.3.5.

Table 5.2 Measurement Results Summary (Version 2)

Parameter	Condition	Simulation	Measurement	Unit
RF Frequency Range		2.45	2.45	GHz
Supply Voltage		3.0	3.0	V
Temperature		25	25	deg
Output Power	After antenna switch	3.8	3.7	dBm
2nd Harmonics Power		-27.8	-24.2	dBm
3rd Harmonics Power		-39.3	-35.2	dBm
Forward Isolation	Power off	42	42	dB
S21		13.9	13.0	dB
S11		-10.7	-10.4	dB
S22		-10.6	-12.3	dB
Input impedance	Single-ended	50	50	ohm
Output impedance	Single-ended	50	50	ohm
Total drain Current		12.0	12.6	mA

Figure 5.6 Comparison of Pout versus Pin (Version 2)

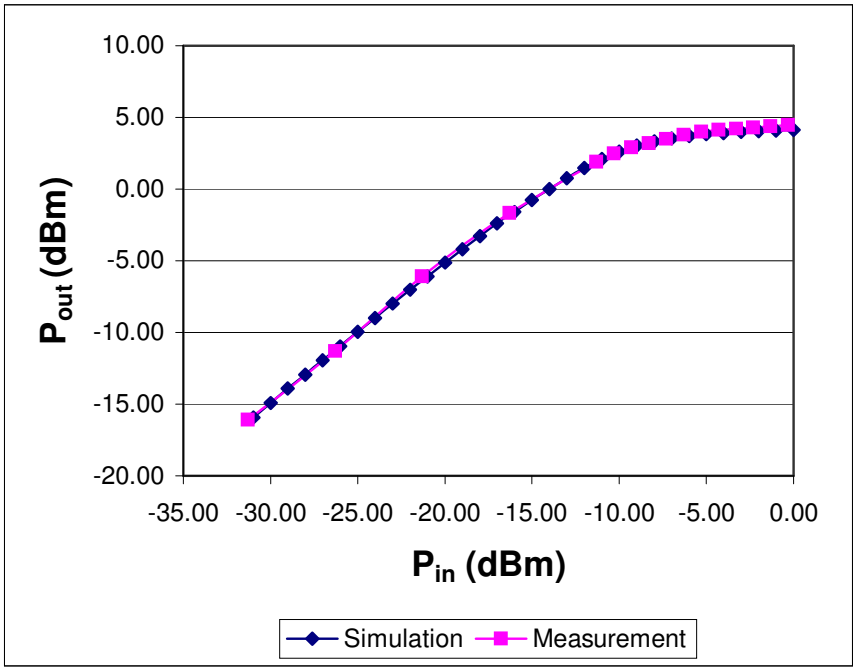
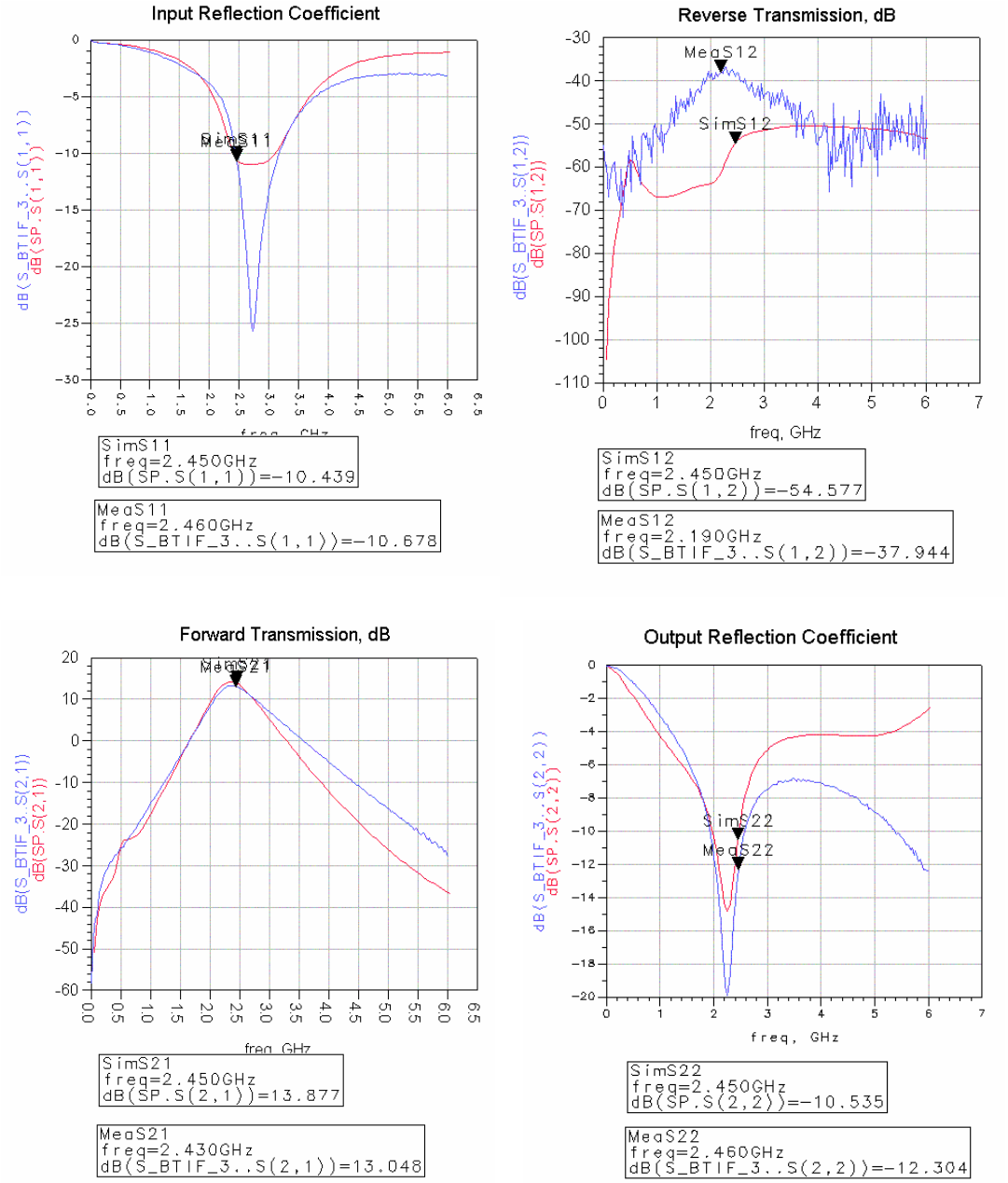


Figure 5.7 Comparison of S-Parameters (Version 2)



5.2.3 Version 3 On-wafer Measurement Results

Table 5.3 Measurement Results Summary (Version 3)

Parameter	Condition	Measurement	Unit
RF Frequency Range		2.45	GHz
Supply Voltage		3.0	V
Temperature		25	deg
Output Power	After antenna switch	5.0	dBm
S21		16.4	dB
S11		-9.9	dB
S22		-9.4	dB
Input impedance	Single-ended	50	ohm
Output impedance	Single-ended	50	ohm
Total drain Current		14.0	mA

The measured output power of Version 3 with copper inductor is 1.2dBm-1.4dBm higher compared to the measured output of Version 2 with aluminum inductor as shown in Table 5.3. The output power measured has a very good consistency with more than ten samples as shown in Figure 5.9.

However, the measured S11 and S22 for Version 3 are worse than the measured values for Version 1. This is because no re-matching was done as there was no copper inductor model available. As a result, some mismatch has incurred since the S-parameters of the copper inductors are different from the aluminum inductors. However, the advantage of low resistive loss has been able to surpass the disadvantage of mismatch, thus the output power measured still managed to show increment.

Figure 5.8 Measurement Results of S-Parameters (Version 3)

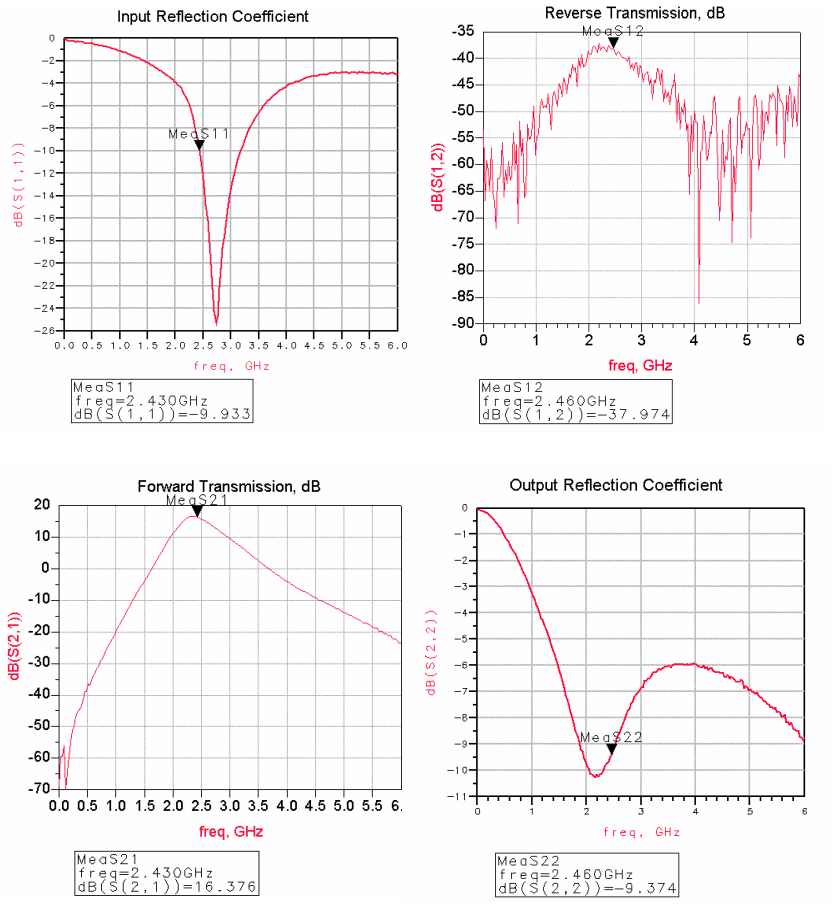
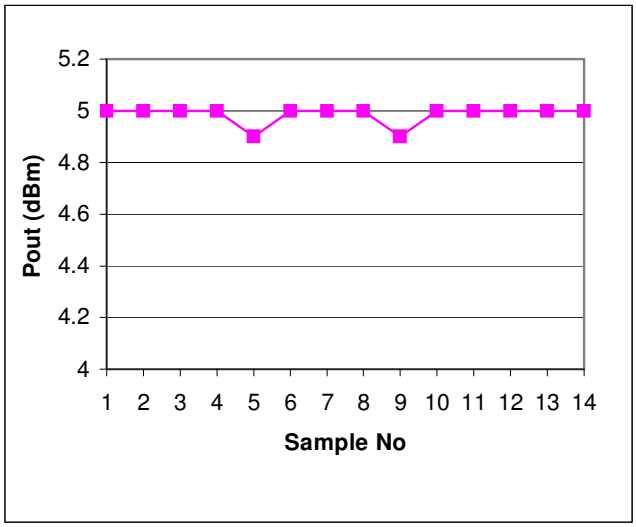


Figure 5.9 Output Power versus Sample No. (Version 3)



CHAPTER 6

Conclusions

A 2.45GHz fully integrated Class-AB CMOS Power Amplifier has been designed and tested. The following conclusions can be drawn:

There are a lot of issues to be resolved in order to design a CMOS power amplifier of practical use. The tolerance of the MOSFET is much higher compared to other types of transistors. The performance of the MOSFET is also very susceptible to temperature changes. There are reliability issues like low breakdown voltage and hot carrier effects. The low resistivity of the silicon substrate has caused the Q-factors of the matching components to be lower, especially the inductors has Q-factor as low as 5.

In the design of the CMOS power amplifier, a temperature-dependent biasing scheme is employed to counteract the performance change of the power transistors. This biasing circuit has managed to reduce the steepness of the reduction in the output power as the temperature increases.

A Cascode Common-Source Common Gate structure is used to overcome the reliability issues like low breakdown voltage and hot carrier effects. The ability to

accommodate higher peak drain voltage has helped to reduce the current consumption of the power amplifier.

By using the copper inductors with a Q-factor double the aluminum inductors, the output power of the power amplifier has increased by 32% to 38% without re-optimizing the matching circuit. This proves the significance of high-Q inductors in a fully integrated CMOS power amplifier.

Although the cascode structure enables a higher peak drain voltage, however, it is still limited to $2V_{DD}$. As a result, the output power of the power amplifier is still limited. In future work, two or three parallel power amplifiers can be combined at their outputs to obtain higher output power.

Differential power amplifier topology can be attempted if high efficiency on-chip transformer balun can be designed or two pins can be accommodated for the output of the power amplifier.

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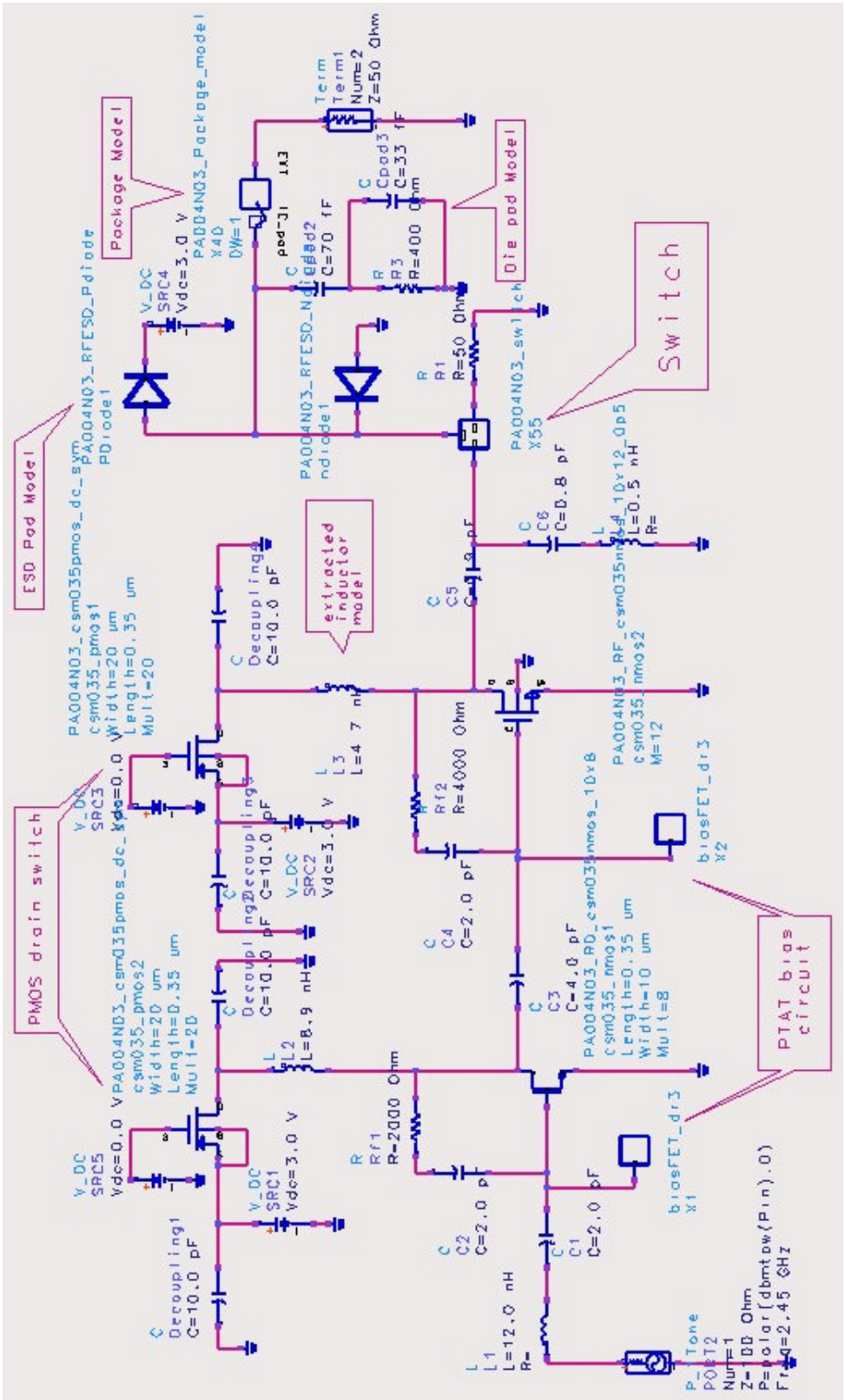
Appendix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ESD Pad Model
Die pad Model
Switch
PMOS drain switch
PTAT bias circuit
extracted inductor model
Term
Term1
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Z=50 Ohm
Cpad3
C=33 fF
Cpad2
C=70 fF
R3
R=400 Ohm
R1
R=50 Ohm
C6
C=0.8 pF
C5
C=1.3 pF
L3
L=4.7 nH
Rf2
R=4000 Ohm
C4
C=2.0 pF
C3
C=4.0 pF
L2
L=8.9 nH
Rf1
R=2000 Ohm
C2
C=2.0 pF
C1
C=2.0 pF
L1
L=12.0 nH
Decoupling1
C=10.0 pF
Decoupling2
C=10.0 pF
Decoupling3
C=10.0 pF
Decoupling4
C=10.0 pF
V_DC
SRC1
Vdc=3.0 V
SRC2
Vdc=3.0 V
SRC3
Vdc=0.0 V
SRC4
Vdc=3.0 V
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PORT2
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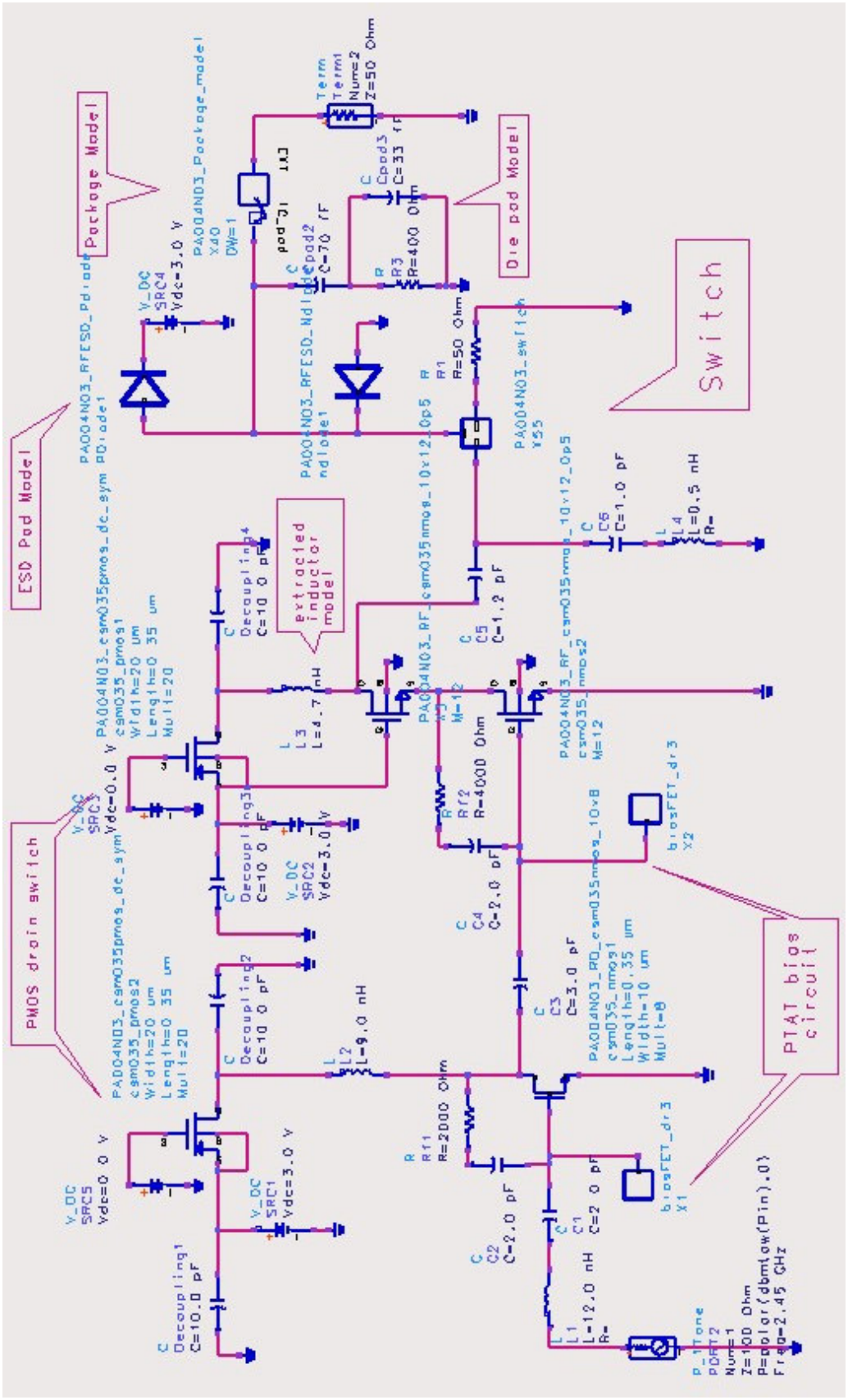
Freq=2.45 GHz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ESD Pad Model
PMOS drain switch
extracted inductor model
PTAT bias circuit
Term
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Z=50 Ohm
Cpad3
C=33 fF
Cpad2
C=70 fF
R3
R=400 Ohm
R1
R=50 Ohm
L4
L=0.5 nH
C6
C=1.0 pF
C5
C=1.2 pF
L3
L=4.7 nH
R2
R=4000 Ohm
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R=2000 Ohm
C2
C=2.0 pF
C1
C=2.0 pF
L1
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C=10.0 pF
Decoupling3
C=10.0 pF
Decoupling4
C=10.0 pF
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V_DC
SRC2
Vdc=3.0 V
V_DC
SRC3
Vdc=0.0 V
V_DC
SRC4
Vdc=3.0 V
V_DC
SRC5
Vdc=0.0 V
P_1Tone
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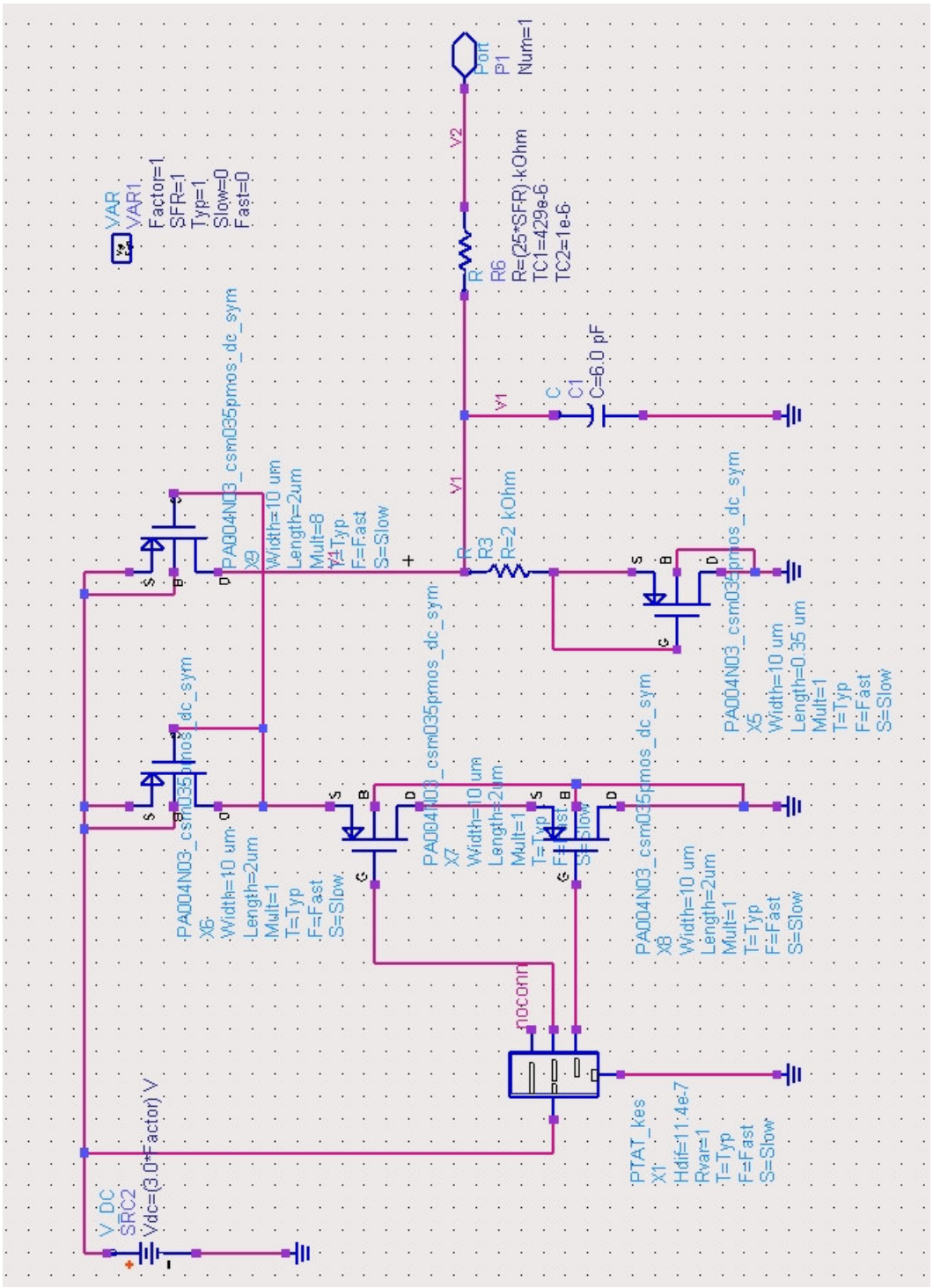
Freq=2.45 GHz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TC1=429e-6
TC2=1e-6
V2
V1
C
C1
C=6.0 pF
R
R3
R=2 kOhm
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Length=2um
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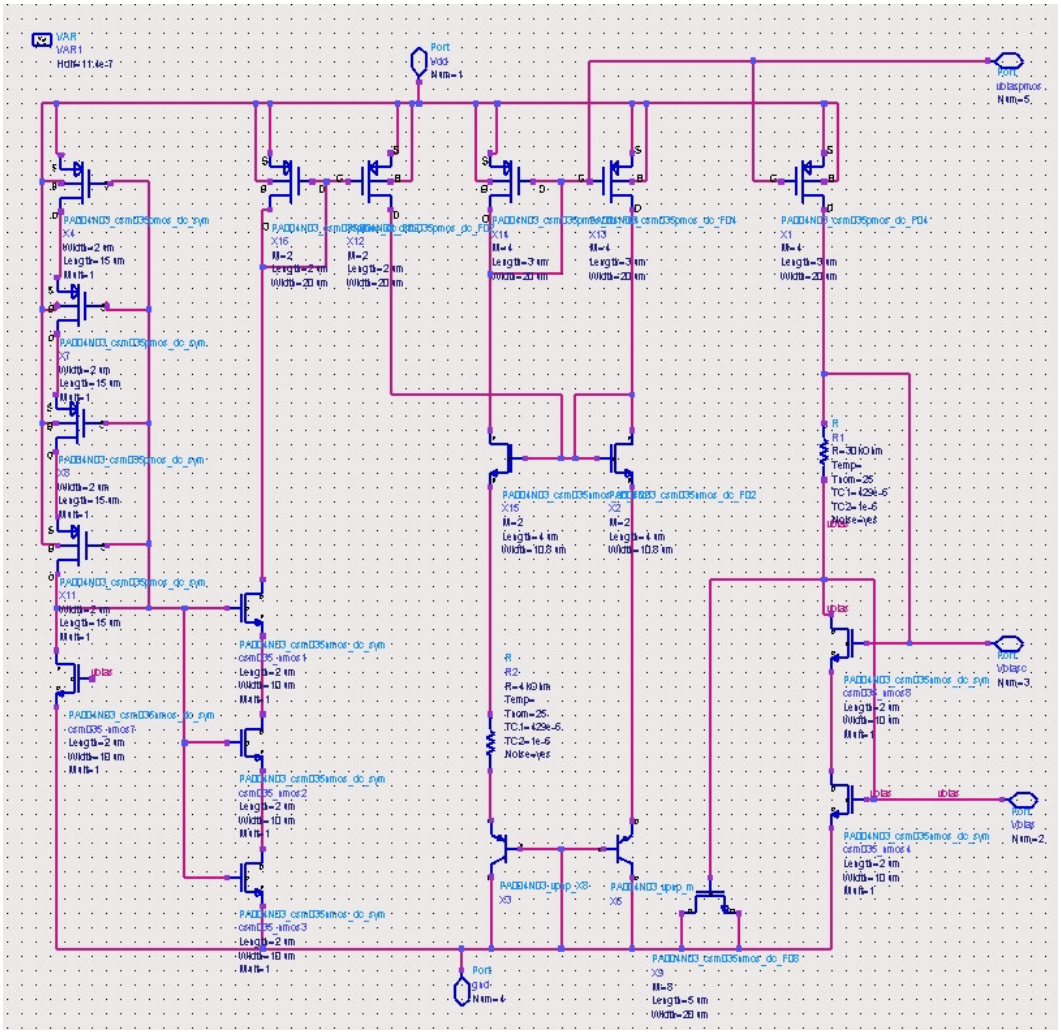

Version 1 Measurement Results

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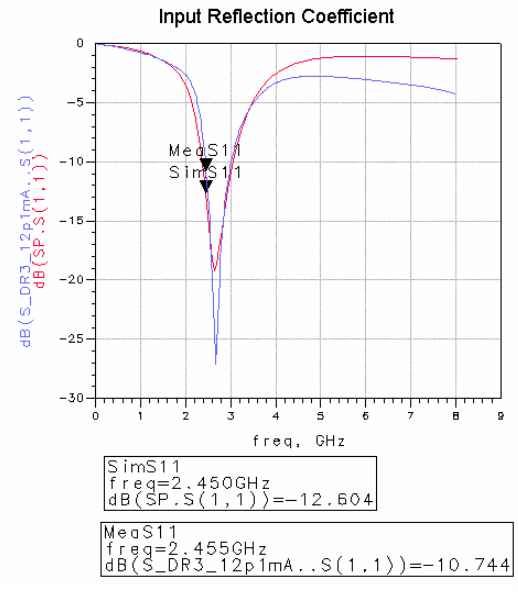
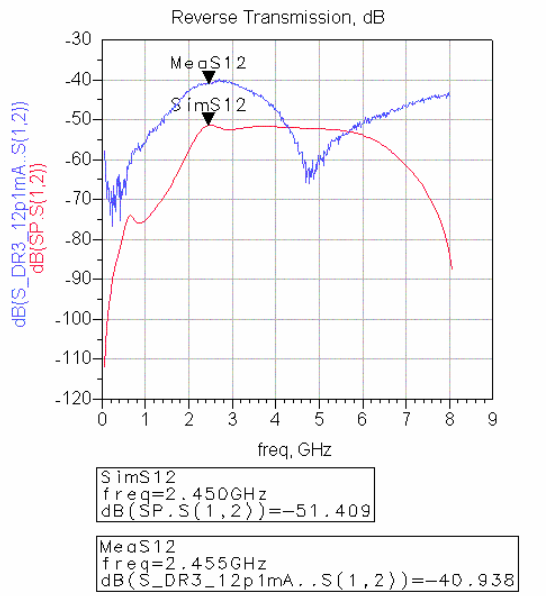
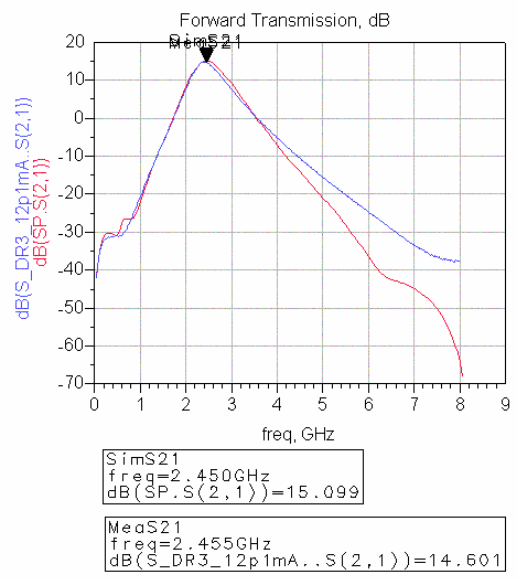
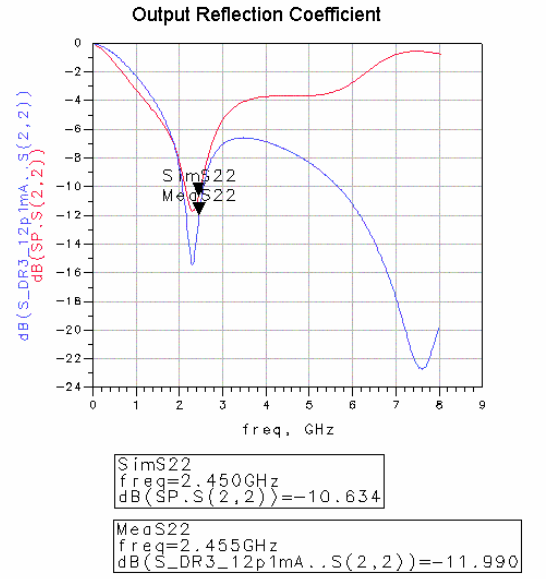
-31.3	-16.1	-65.7	-	11.8
-26.3	-11.3	-55.7	-	11.8
-21.3	-6.1	-45.4	-82.7	11.9
-16.3	-1.7	-34.8	-61.7	12.2
-11.3	1.9	-24.3	-47.3	13.3
-10.3	2.5	-23.0	-44.7	13.6
-9.3	2.9	-22.3	-42.7	13.9
-8.3	3.2	-22.1	-40.4	14.1
-7.3	3.5	-22.3	-37.9	14.5
-6.3	**3.8**	**-22.8**	**-35.7**	**14.8**
-5.3	4.0	-23.7	-33.7	15.1
-4.3	4.1	-24.8	-32.0	15.4
-3.3	4.2	-26.4	-30.5	15.7
-2.3	4.3	-27.9	-29.2	16.0
-1.3	4.36	-29.0	-28.2	16.3
-0.3	4.44	-29.3	-27.2	16.6

Version 1 Measurement Results









Version 2 Measurement Results

Pin (dBm)	Pout (dBm)	2nd Harmonics (dBm)	3rd Harmonics (dBm)	Current (mA)
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-26.3	-11.2	-57.7	-	8.7
-21.3	-6.1	-47.0	-	8.8
-16.3	-1.6	-36.5	-65.7	9.1
-11.3	2.0	-25.6	-47.3	10.1
-10.3	2.5	-24.4	-44.7	10.4
-9.3	2.9	-23.6	-41.8	10.9
-8.3	3.2	-23.4	-39.7	11.4
-7.3	3.5	-23.6	-37.2	12.0
-6.3	**3.7**	**-24.2**	**-35.2**	**12.6**
-5.3	3.9	-24.9	-33.1	13.3
-4.3	4.04	-25.8	-31.7	13.9
-3.3	4.15	-27.1	-30.2	14.5
-2.3	4.24	-28.0	-28.9	15.0
-1.3	4.27	-28.7	-28.0	15.5
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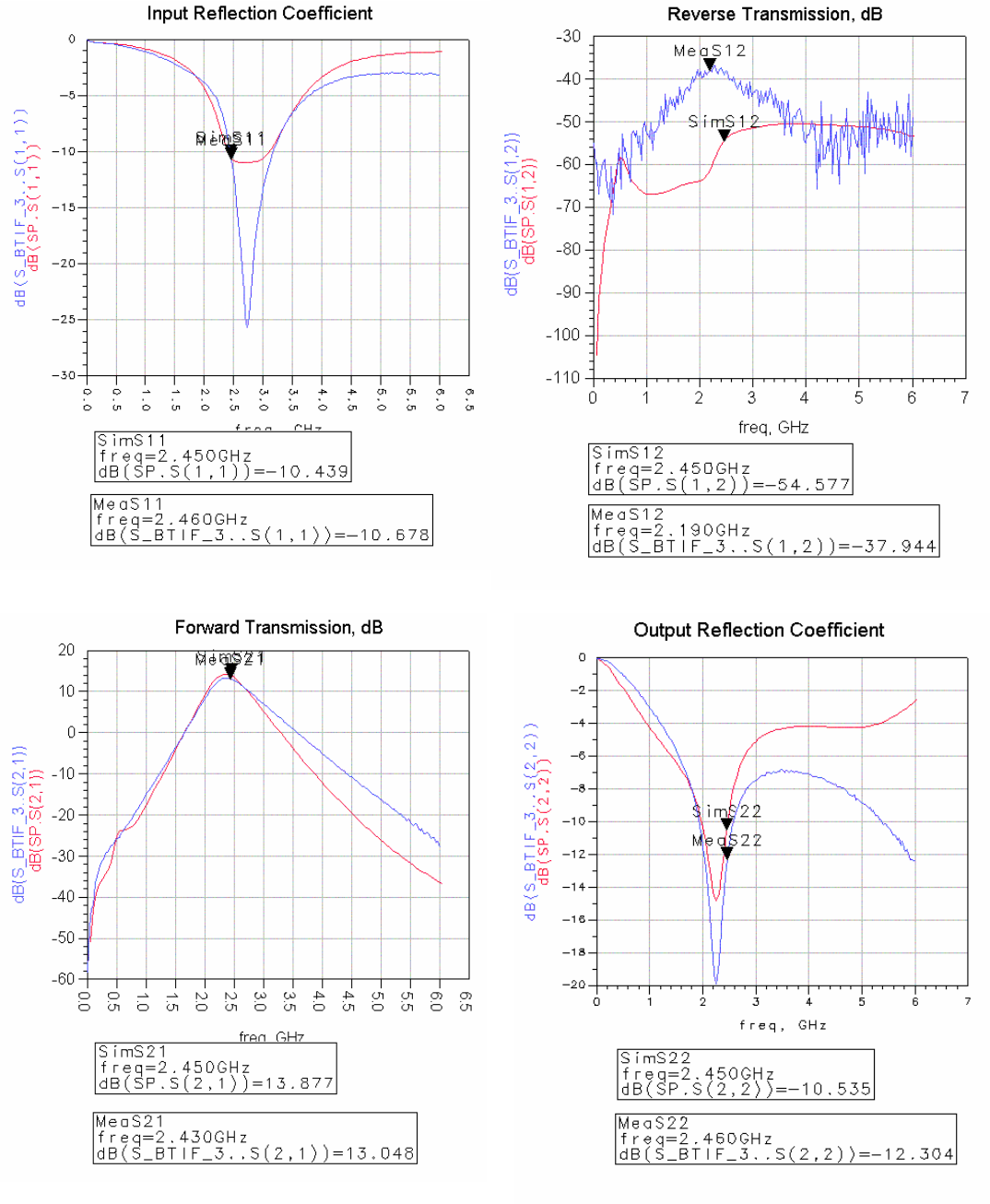
Version 2 Measurement Results



Die Photo