A NOVEL MMIC 3 PHASE-STATE LC SWITCHED-FILTER PHASE SHIFTER

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CONTENTS

Summary

Phase shifter is an important component of the communication industry. The major areas of research for phase shifters are the reduction in size, phase error, production cost, and increase in bandwidth. The design of a novel MMIC 3 phase-state LC switched-filter phase shifter is presented. Three phase-state phase shifter is a kind of novel phase shifter design achieved by adding one additional phase setting to a conventional single-stage 2 phase-state phase shifter. Thus each phase shifter has two differential phase shifts. The reason we choose LC topology to design our 3 state phase shifter is its smaller size, lower cost, wide bandwidth and easy implementation of lumped components. It is particularly attractive for monolithic integration because of lumped inductors and capacitors. The possibilities of using LC switched filter are analyzed and discussed. The novel 3 phase-state LC switched-filter phase shifters are designed for differential phase settings: 0°/11.25°/22.5° and 0°/33.75°/56.25°. The lower 3 bits of a conventional 5 bits phase shifter can be replaced by cascading two of the above 3 phase-state phase shifters. The same phase shift resolution of 11.25° is achieved. Finally the simulation results of each bit and cascading of the two bits are compared with the conventional 2 phase-state phase shifters. It yields very significant improvement of size and also shows satisfactory performance. The total RMS phase error of all the 8 phase states yielded by the cascading of the two bits is less than 1.05º and the phase error is well balanced over the bandwidth of 8 GHz to 10 GHz. The insertion losses are between –4.8±0.4 dB, with a maximum loss variation of 0.9 dB for all states over the 8 GHz to 10 GHz frequency range. By reducing the total bit number, a maximum return loss of –8.95 dB is obtained.

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Chapter 1

Introduction

1.1 Background

Phase shifter is a two-port device whose basic function is to provide a change in the insertion phase of a signal with minimal attenuation [1]. In many microwave communication, radar and measurement systems, phase shifters occupy a very important place. Particularly of interest is its function as a beam-forming network of an adaptive phased array antenna [2]. Phase shifters can be broadly classified as mechanical or electronic, depending on whether the phase control is achieved through mechanical or electronic tuning. Electronic phase shifters assume special significance because of their potential utility and volume requirement in phased array antenna systems for inertialess scanning [3].

Electronic phase shifters are those, which use control elements such as $p-i-n$ diodes and Gallium Asenide (GaAs) FET to change the phase of the RF signal. These control elements are used either as series or shunt switches. Basically the phase shift is obtained by switching the control elements ON and OFF, such that the RF signal is suitably routed or switched within the circuit to give the desired phase shift. Depending on the type of electronic control medium or mechanism adopted, electronic phase shifters can be classified as ferrite, semiconductor device, active FET, or bulk semiconductor phase shifters. Depending on the type of operation, they can be categorized as analog or digital. Other classification can be in terms of the type of transmission structure and the

technology adopted for fabrication [3]. As an example, Monolithic Microwave Integrated Circuit (MMIC) phase shifters experience rapid development in recent years.

Fig 1.1 provides the classification of electronic phase shifters.

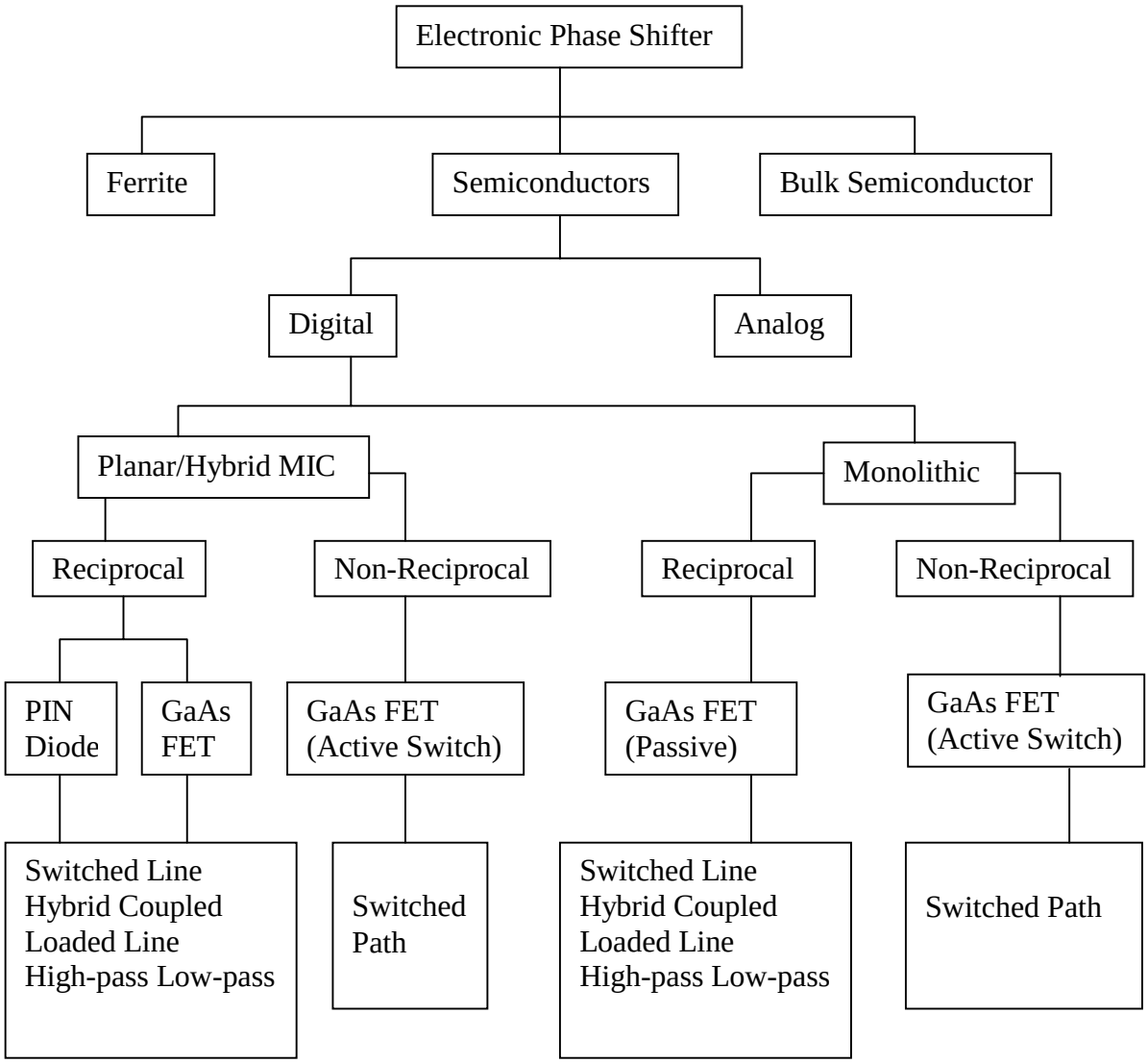


Fig 1.1 Classification of electronic phase shifters

Analog and Digital Phase Shifter:

Depending on the type of operation, phase shifters can be categorized as analog or digital, having reciprocal or nonreciprocal characteristics. Phase of analog phase shifters varies continuously while digital phase shifters have phase variation in discrete steps. A digital phase shifter generally consists of a cascade of several phase bits with phase shifts incremented in binary steps [1]. Since the bulk requirement of phase shifter is for phased-array radar, digital types are preferred over analog ones in view of the flexibility they offer for interacting with the digital computer for control signals [2]. There are generally four types of circuits used in the design of digital phase shifters: switched line, hybrid coupled, loaded line, high-pass low-pass.

MMIC and MIC Phase Shifter:

In a hybrid microwave integrated circuit (MIC), all passive integrated circuit are deposited on the surface of a low-loss dielectric substrate, and discrete semiconductor devices are either bonded or soldered onto the passive circuit. In the monolithic microwave integrated circuit (MMIC) technique, the entire circuit consisting of passive circuit elements, active devices, and interconnections are formed inside on or within a semi-insulating, semi-conducting substrate [3].

The present trend is shifting towards MMIC from MIC. The main advantages of MMIC over MIC are its small size and weight, improved reliability and reproducibility through elimination of wire bonds, and its ability to incorporate multifunctional performance on a single chip [4]. Elimination of wire bonds and embedding of active devices within the

semi-conducting substrate minimize the undesired parasitic and, therefore, improve the bandwidth performance. Furthermore, the multifunctional capability on a single chip offers scope for realization of integrated receiver front end or transmit-receive modules, including the phase shifter. While the MMIC approach offers all the advantages of integration, it loses the flexibility of circuit tuning and troubleshooting available in hybrid MICs. This problem can however, be circumvented by the use of CAD techniques so that the need for circuit adjustments is minimized.

Passive and Active Phase Shifter:

Phase shifters that amplify the RF signal in addition to the phase shift are known as "active" phase shifters. The GaAs MESFET, in particular, the dual-gate MESFET, is the key control element that enables this dual function. In the passive phase shifter, the GaAs MESFET is operated only as a switch by controlling the gate voltage. In an active phase shifter, the GaAs MESFET is used as a switching amplifier (active switch). In the case of phased arrays, the use of GaAs FET active phase shifters offers an attractive alternative to separate phase shifter and amplifier, which relax the insertion loss and power-handling requirement of phase shifters.

Application of Phase Shifters:

The most important application of phase shifter is its function as a beam-forming network, in the phased array. A typical phase array can have thousands of radiating elements, with each antenna element connected to a phase shifter. Normally phase shifters are placed before the amplifiers and each antenna is fed separately so that the phase and amplitude of

the signal can be controlled independently. There are basically two types of phase shifters: constant time-delay devices and constant phase-delay devices. Correspondingly, there are usually two types of electronic scanning schemes in array radars: phase scanning and time-delay scanning as shown in Fig 1.2. A typical practical planar array may consist of 1000 to 10,000 antenna elements and adopt one phase-delay device (phase scanning) or time-delay device (time-delay scanning) for each antenna element.

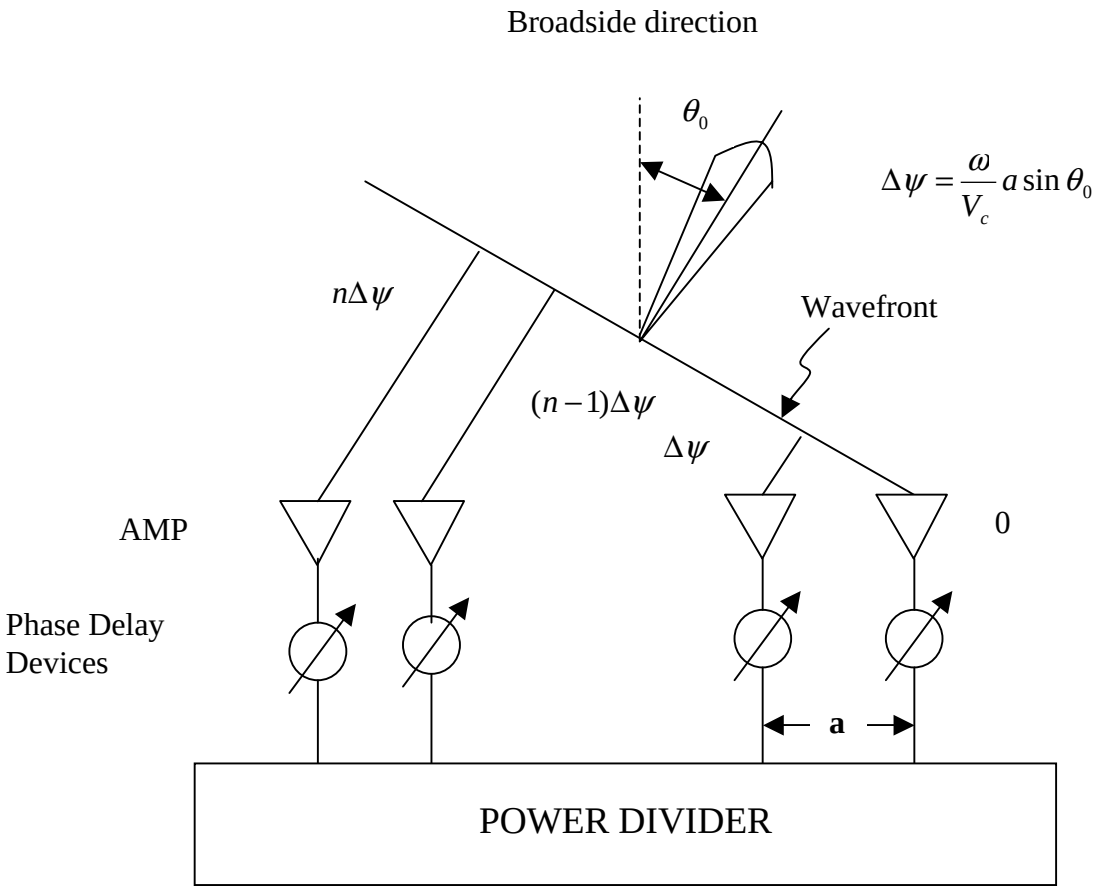


Fig 1.2 (a) Schematic diagram of a linear phase scanning array

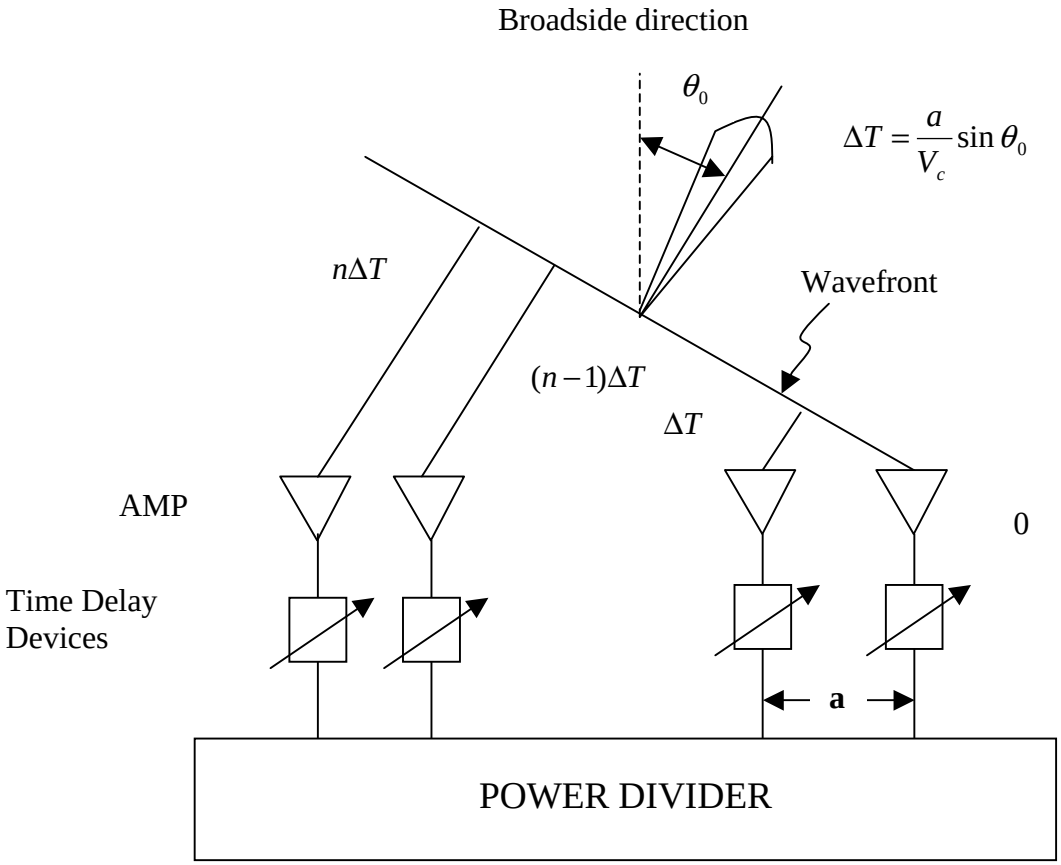


Fig 1.2 (b) Schematic diagram of a linear time-delay scanning array

In phase scanning, the phase-delay devices enable the beam to be scanned in both azimuth & elevation. If all the antenna elements are excited in phase, the radiated waves add coherently to form a wave front parallel to the line joining the antenna elements. Because the beam pointing direction is always perpendicular to the wave front, the radiated beam points in the broadside direction. In phased array, this wave front is adjusted by controlling the phase of the electromagnetic signal at the aperture of each of the radiating elements. The phase delay needed between adjacent antenna apertures can be calculated

as $\Delta\psi = \frac{\omega}{V_c} a \sin\theta$. Where "a" is the space between the adjacent elements, V_c is the free-space velocity and θ is the scan angle. To scan the beam, $\Delta\psi$ is varied continuously (by analog phase shifters) or in discrete steps (by digital phase shifters). If the phase shift is independent of frequency (constant phase delay device), a small change in the operating frequency changes the beam pointing direction θ. Thus the bandwidth of the operating frequency is limited by the phase scanning scheme.

This problem can be eliminated by using the constant time-delay device for which the phase delay $\Delta\psi$ is a linear function of frequency. As shown in Fig 1.2 (b) the phase-delay devices are replaced by time-delay devices, which offer a linear phase frequency response. The incremental time delay between successive elements is $\Delta T = \frac{a}{V_c} \sin\theta$. The scan angle θ depends on time delay and not frequency. However, for current technology, most time-delay devices are too lossy and expensive. On the other hand, phase-delay devices are produced relatively cheaper and have very low loss.

The Phase_Cum_Time Delay Scanning scheme is a compromise, which uses a combination of constant phase delay and constant time delay devices as shown in Fig1.3. The phased array is divided into several sub-arrays and each sub-array is connected to a variable time-delay device. It can be seen that the pattern of each sub-array is steered by the phase-delay devices and the total radiation pattern is steered by both the time-delay devices and the phase-delay devices. The bandwidth of the phased array increases by a factor of (N+1), where (N+1) is the number of sub-arrays. Since only one time-delay

device is connected to each sub-array, the number of time-delay devices is decreased tremendously.

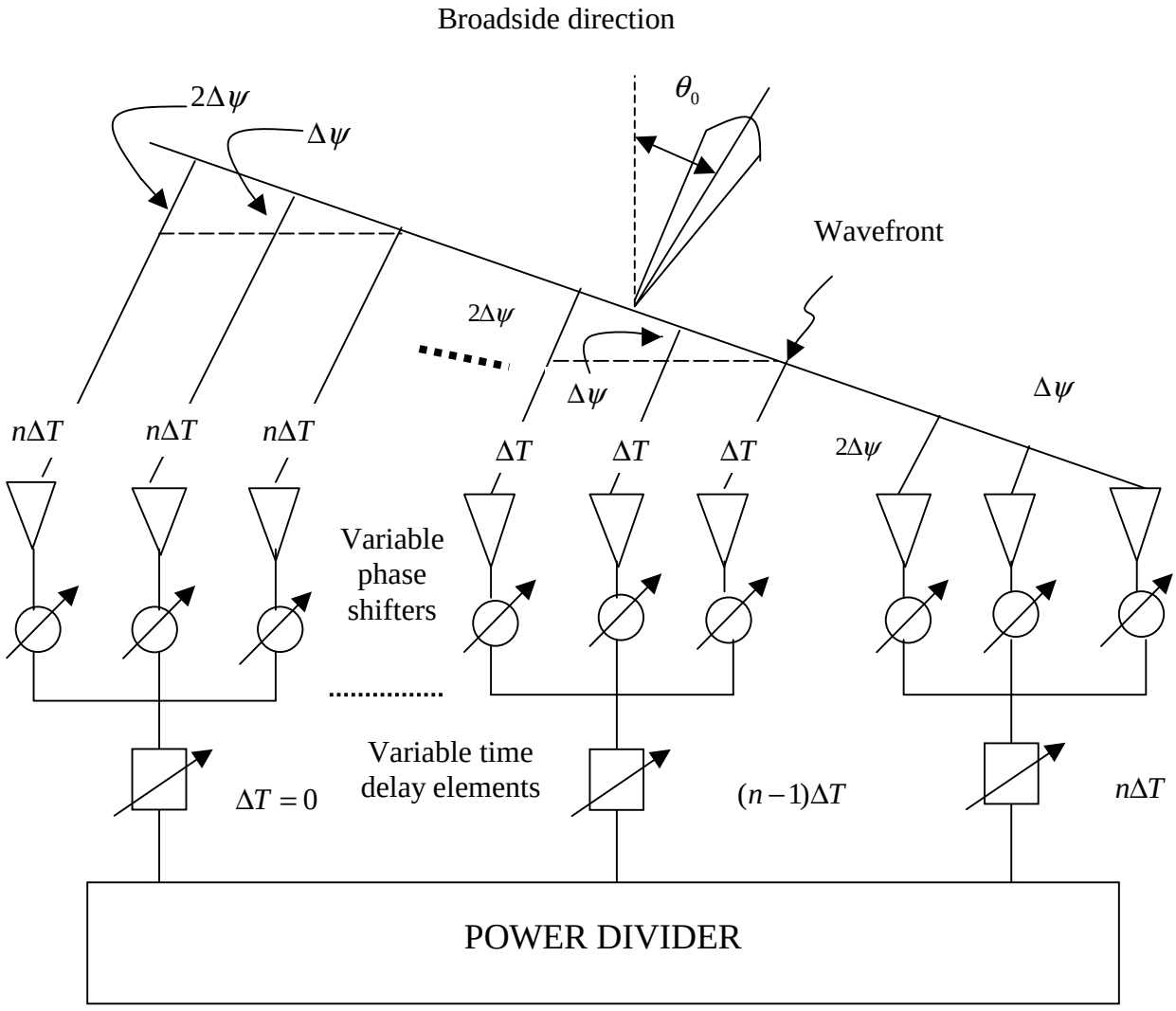


Fig 1.3 Schematic of a linear array using phase shifters and time-delay devices

Among the four types of phase shifters, the switched line and reflection types of phase shifters are most suitable for constant time delay, while all four types can be made into constant phase-shift devices [5].

The evolution of phased array techniques to its present sophisticated form is strongly based on the development of phase shifter technology. On the other hand, new vistas of application areas have opened up in radar, communication, and civilian sectors, demanding newer techniques and technologies for the phase shifters [3].

1.2 Motivation

The growing application of phase shifter in industrial applications addresses the need for reduced size, weight and cost without compromising on performance. The present trend is shifting towards MMIC from MIC because of its good reproducibility, reliable performance and small size. Since the main use of phase shifter is in phased array, the size and phase error is of great importance. The main motivation behind this project is to achieve a novel digital phase shifter design that can be implemented easily in MMIC form with reduced size, lower phase error and minimum cost of production.

1.3 Achievements

In this project, a novel type of 3 Phase-State Phase Shifter which utilizes a novel LC lumped components structure was designed. This is a new technique of building the phase shifter and fulfills the motivation behind the project.

This project has achieved the following objectives:

1. Proposed a novel type of 3 phase-state LC switched-filter phase shifter. Detailed theoretical analyses are presented which will contribute to the future work.
2. Designed a novel 3 phase-state LC switched-filter phase shifter using UMS foundry Ph25 process library and compared the simulation results with various types of conventional 2 phase-state phase shifters. (One Bit)
3. Designed two 3 phase-state phase shifters: 0°/11.25°/22.5° and 0°/33.75°/56.25°. It can be seen that three: 11.25°, 22.5°, 45° conventional 2 phase-state phase shifters can be replaced by cascading two 3 phase-state phase shifter: 0°/11.25°/22.5° and 0°/33.75°/56.25°. The simulation results were also compared with the conventional 2 phase-state phase shifter.
4. Achieved good performances of the above novel designs.

1.4 Scope

A completed MMIC phase shifter design consists of:

- Analysis of the available technology and literature and choosing the circuit topology
- Understanding the foundry capability and choice of process library
- Theoretical design and developing proper optimization criteria
- Simulation of the design using the foundry model
- Mask layer design using the layout macros form the foundry
- EM and statistical analysis
- Delivery of chip and wire bonding of MMIC into alumina test jig

- Testing of MMIC

The scope of this thesis is listed as follow:

Chapter 1 gives the background of phase shifter applications and its classification. It also provides the motivation and objectives of the project. The scope of the project is also discussed.

Chapter 2 reviews the literature survey on various designs of digital phase shifters and a summary of overall performance.

Chapter 3 provides discussions on considerations and constraints of phase shifter design including the performance specifications, topology selection criteria and switching device configurations.

Chapter 4 introduces the 3 phase-state phase shifter as well as the 3 phase-state phase shifter proposed by the author, using block diagrams.

Chapter 5 presents the circuit diagram of the 3 phase-state phase shifter block proposed in Chapter 4. It also discusses the analysis and design of the circuit.

Chapter 6 shows the simulation results of the proposed phase shifter and compares its performance with the performance of 2 phase-state designs.

Chapter 7 gives the summary of previous chapters as well as the performance of the novel 3 phase-state LC switched-filter phase shifter. It also looks into the future developments and improvement on this project.

The abstract published by “Progress in Electromagnetics Research Symposium”, July 5-14, 2000, Cambridge, MA, USA, is given in the Appendix. It should be noted that only abstracts are published in the proceedings.

Chapter 2

Literature Review

2.1 Introduction

Since 1960s, significant advances have taken place in semiconductor phase shifter, which is one of the most important and well-developed types of phase shifter, including P-I-N and GaAs FET types. In recent years, because of its compatibility with GaAs technology, the phase shifters using GaAs FET as switches have been experiencing a rapid development [6, 7, 8]. Digital phase shifters employing GaAs FET are of particular interests due to its ultra-fast switching speed [9]. This chapter is intended to provide a brief overview of various types of digital FET phase shifters. This is followed by a review of recent developments reported on the different types of FET phase shifters.

All the FET phase shifters can be mainly classified into two categories: reflective type and transmission type.

2.2 Reflective Phase Shifter

The reflection-type phase shifter is basically a one-port device in which there is reflection of a microwave signal at the termination of a transmission line. The magnitude of the reflection coefficient should ideally be unity, and phase shift is given by the change in the phase of the reflection coefficient between the two switching states [3]. A reflective-type circuit can be represented as a passive network terminated in an ideal on/off switch as shown in Fig 2.1. In most of the reflective-type circuits both the incident and reflective signals are separated using a circulator or a 3dB hybrid couplers.

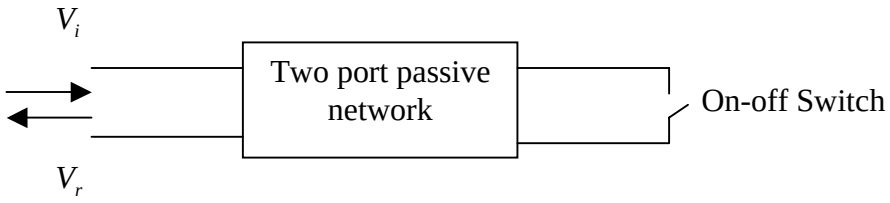


Fig 2.1 Schematic of a reflection-type network

2.2.1 Circulator Coupled Phase Shifter

The circulator is used to separate the incident and the reflective signals. The transmission coefficient T between the input and output ports is equal to the reflection coefficient Γ of the reflective network. Consider the Fig 2.2. The ports 1 and 2, 2 and 3, and 3 and 1 are coupled while no power goes into 3 directly from 1, from 3 to 2 and from 2 to 1. Therefore input is at port 1 and the signal goes to 2 where its gets reflected and then the signal goes from 2 to port 3 which is the output port. When the switch is on let the reflection coefficient be Γ. When the switch is off we introduce an extra electrical length β1 and the reflection coefficient is $\Gamma e^{-\beta L}$. Hence the differential phase shift is given by phase difference in two states, which is βl.

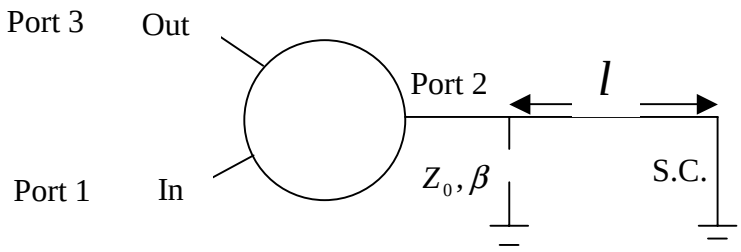


Fig 2.2 Circulator coupled phase shifter

2.2.2 Hybrid Coupled Phase Shifters

The hybrid coupled phase shifter [10] makes use of a 3dB, 90˚ hybrid coupler with two of its ports terminated in symmetric phase-controllable reflective networks. As shown in Fig 2.3, an input signal at port 1 gets divided equally but in quadrature phase at the two-coupled ports. On reflection from the two identical terminations, the two signals add up at port 2 but cancel at port 1. Phase shift corresponds to the additional path length traversed by signal between the two switching states.

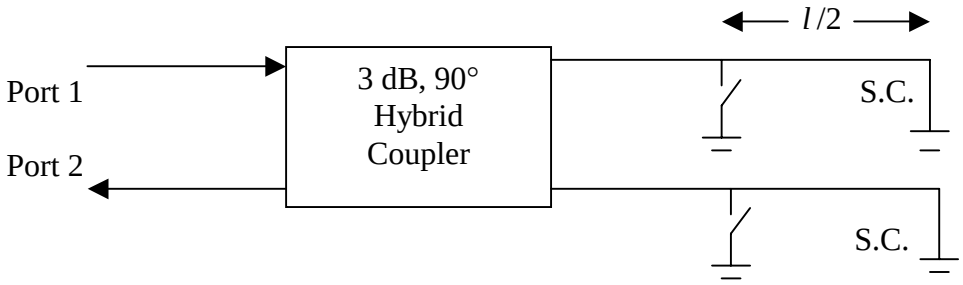


Fig 2.3 Schematic of hybrid coupled phase shifter

The commonly used 3dB hybrid couplers are branch line coupler, rat race hybrid coupler and parallel-coupled backward-wave (Lange) coupler. The bandwidth of the phase shifter bit is governed by the bandwidth of the coupler as well as the reflective network. The coupler bandwidth is assessed from its characteristics in terms of power split, phase relationship between the output ports, input VSWR, and isolation as function of frequency. Considering a combination of all these factors, the useful bandwidth of the branch-line coupler, the rat-race coupler, and the parallel-coupled backward-wave coupler as 3-dB hybrids is approximately 10%, 20% and 35%, respectively.

For the parallel-coupled backward-wave couplers on microstrip lines, there can be problems in implementing as the spacing gets smaller and it is harder to etch. However there is additional advantage that there is no need of any dc block as the input and output ports are coupled to the reflective network.

2.3 Transmission Type

An ideal transmission type phase shifter is a two-port network in which the phase of the transmission coefficient through the network is altered by means of a switch, while the magnitude remains unity in both the states. The phase shift is given by the change in the transmission phase through the network. Fig 2.4 shows the general schematic of the transmission type phase shifting network. The passive network can be lumped or distributed and the switch may be series or shunt mounted. Switching between the two states is equivalent to passing the RF signal through two different circuit paths. The change in the transfer phase of the network between the two switching states gives the phase shift.

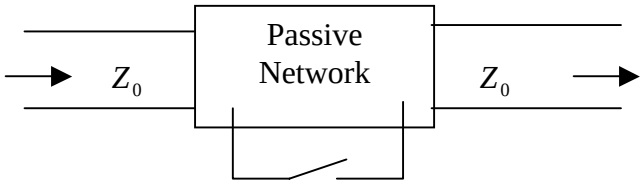


Fig 2.4 General schematic of a transmission-type phase shifter

2.3.1 Switched Line Type

Among all the various types of digital phase shifters, switched line is also most popular due to the ease of analysis. The switched line phase shifter is basically a time-delay circuit in which phase shift is obtained by switching between two transmission line sections of different lengths.

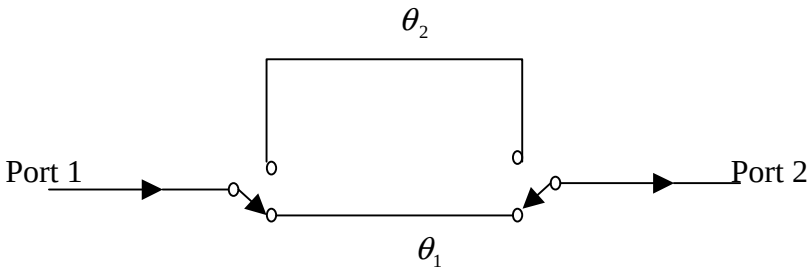


Fig 2.5 Schematic of switched line phase shifter

Consider the Fig 2.5. With appropriate switching states at the input and output, the RF signal is switched between a reference path (θ_1) and a phase shift path (θ_2). The difference in their electrical length determines the amount of differential phase shift

$$(\Delta\phi = \theta_2 - \theta_1) \qquad (2.1)$$

Where (θ_1) and (θ_2) is the transmission phase of the signal in the reference and phase shift path respectively and the electrical length of the line is characterized by equation 2.2.

$$\theta = \frac{2\pi}{\lambda_g} l \qquad (2.2)$$

Schiffman Phase Shifter

The most common switched-line configurations are given in Fig 2.5. Fig 2.6 shows the schematic circuit of a Schiffman [11] phase shifter: a broadbanding technique of switched line type phase shifter. A nearly constant phase shift can be achieved over a wide

bandwidth. The signal switches between two sections; an all pass U-Section and a straight line of suitably chosen length, both operating in the TEM mode. The U-section is a section of coupled transmission line with two if its ends connected together. The phase shift of the U-Section is a sinusoidal function of frequency.

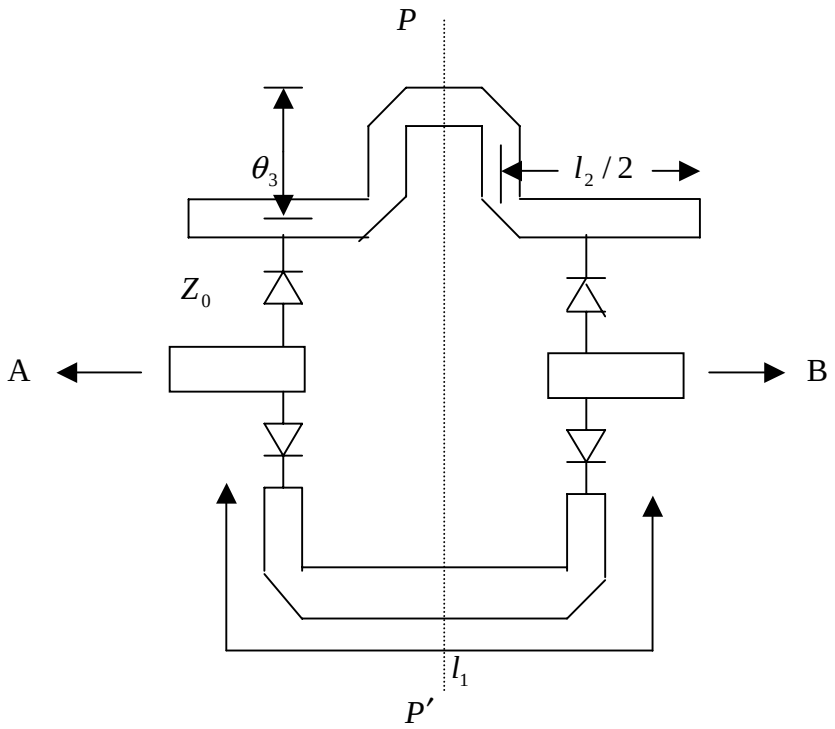


Fig 2.6 Schiffman phase shifter

The impedance looking into either port of Fig 2.6 is given by:

$$Z_{in} = \sqrt{Z_{0e} Z_{0o}} \qquad (2.3)$$

Where Z_{0e} and Z_{0o} are the even and the odd mode characteristic impedance of the coupled section. The phase-frequency response is governed by the equation:

$$\cos\phi = \frac{R - \tan^2\theta}{R + \tan^2\theta} \qquad (2.4)$$

where

$$R = \frac{Z_{0e}}{Z_{0o}} \qquad (2.5)$$

The analysis is based on even-odd mode analysis. If the diodes are assumed to be ideal, the differential phase shift is given by

$$\Delta\phi = \beta(l_1 - l_2) - \cos^{-1}\ \frac{R - \tan^2\theta_3}{R + \tan^2\theta_3} \qquad (2.6)$$

Hence, by controlling l_1, l_2 and θ_3 one can achieve the desired phase shift. Constant phase shift can be achieved over a wide bandwidth on the order of an octave. There are reports on this type of switched line type phase shifter at higher frequency and wider bandwidth [11, 12]. However, their performance deteriorates with increase in frequency and reduction in size.

The main difference between the switched line type and reflective type phase sifter is the size of the shifting element. The reflective phase shifter uses the switching of load at 1 or 2 of its terminations as phase shifting elements, the switched line type phase shifters uses the switching of signal path in different length. Generally the reflection type phase shifter uses less number of switches as compared to switched line type phase shifter. Nevertheless, both the designs are too big to be used at the monolithic level.

2.3.2 Loaded Line Phase Shifter

The loaded line phase shifter as shown in Fig 2.7 makes use of a transmission line loaded with a symmetric pair of switchable reactive elements. Although this design is more for

lower phase bits, there have been many attempts to build loaded line phase shifter for 90° and 180° bit. The spacing between the reactive elements as shown in Fig 2.7 is about a quarter wavelength such that the reflections from the reactive elements cancel at the input terminal at the design frequency.

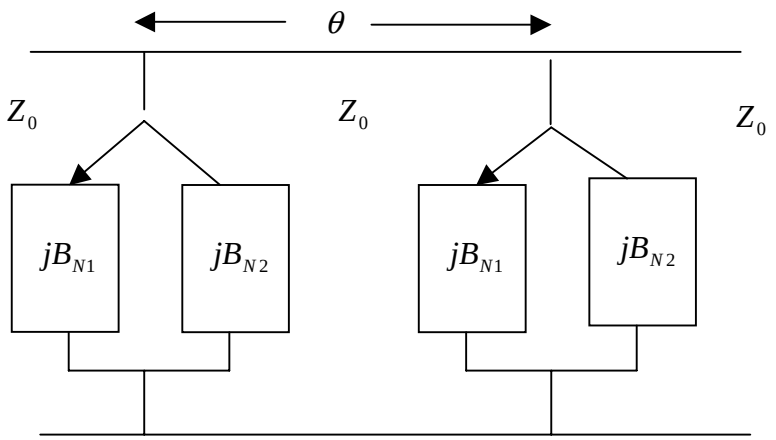


Fig 2.7 Loaded line phase shifter

The loaded line phase shifter in Fig 2.7 can be conveniently analyzed by using the ABCD matrix.

Considering the shunt-loaded circuit with switches connected to susceptances B_{N1} as shown in Fig 2.7:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ jB_{N1} & 1 \end{vmatrix} \begin{vmatrix} \cos\theta & jZ_0 \sin\theta \\ jY_0 \sin\theta & \cos\theta \end{vmatrix} \begin{vmatrix} 1 & 0 \\ jB_{N1} & 1 \end{vmatrix} \tag{2.7}$$

From ABCD Matrix, S Matrix is given by:

$$S_{21} = \frac{2}{(\cos\theta + B_{N1}\sin\theta) + j\{B_{N1}\cos\theta + (1 - \frac{B_{N1}^2}{2}\sin\theta)\}} \tag{2.8}$$

The input reflection coefficient and transmission phase are given by:

$$S_{11} = \left[1 - \frac{1}{1 + B_{N1}^2(\cos\theta - 0.5B_{N1}\sin\theta)^2}\right]^{1/2} \tag{2.9}$$

$$\phi_{11} = \tan^{-1}\left|\frac{B_{N1} + \left(1 - \frac{B_{N1}^2}{2}\right)\tan\theta}{(1 - B_{N1}\tan\theta)}\right| \tag{2.10}$$

If the switches are connected to susceptances B_{N2}, the transmission coefficient, phase and reflection coefficient are given by equations 2.8-2.10 respectively by replacing B_{N1} with B_{N2}. The phase shift $\Delta\phi$ is equal to $(\phi 2 - \phi 1)$.

It has been found that the widest bandwidth is achieved when $\theta = \pi/2$, and $B_{N1} = -B_{N2}$. With these conditions being true the phase shift is given by:

$$\Delta\phi = \tan^{-1}\left[-\frac{1 - 0.5B_{N1}^2}{B_{N1}}\right] - \tan^{-1}\left[\frac{1 - 0.5B_{N1}^2}{B_{N1}}\right] \tag{2.11}$$

$$= \pi - 2\tan^{-1}\left[\frac{1 - 0.5B_{N1}^2}{B_{N1}}\right] \tag{2.12}$$

$$= 2\tan^{-1}\left[\frac{1 - 0.5B_{N1}^2}{B_{N1}}\right] \tag{2.13}$$

Thus by controlling the value of B_{N1} we can achieve the desired phase shift, the loaded line phase shifter is particularly useful for a small phase shifts up to 45°. This is due to the

fact that the susceptance magnitude must be kept small for a good input match over the desired frequency band. Loaded line phase shifter are used to provide a relatively small phase shift, typically less than 90° as reported in some papers. Hence, we look into some other design techniques used to achieve higher phase bits.

2.3.3 Switched Filters Type

Switched filters phase shifter is a relatively new type of phase shifter. These structures are recommended for use at lower frequencies and are also the most promising ones for monolithic realization using either Schottky diodes or MESFETs as switching elements. When the switches are connected to the low-pass filter, the signal passing through the circuit undergoes a phase delay, and when the switches are connected to the high-pass filter, the circuit provides a phase advance. Phase shift is obtained by switching between the two filter circuits. This class of phase shifters is known as switched filter design and it can be divided into distinct groups: conventional and embedded MESFETs.

2.3.3.1 Conventional High-Pass Low-Pass Phase Shifter

The basic structure of high-pass low-pass phase shifter is shown in Fig 2.8. A low-pass filter comprised of series inductors and shunt capacitors provides phase delay to signals passing through it, and a high-pass filter comprised of series capacitors and shunt inductors provides phase advance. Since the passive components used are very small, therefore, the size of phase shifter is the smallest as compared to all the previously mentioned types of phase shifter designs.

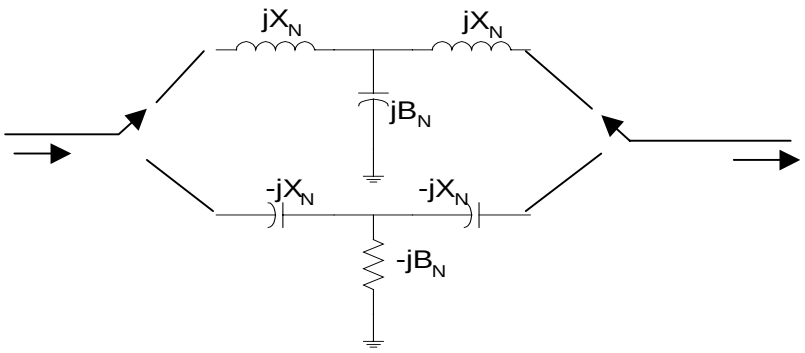


Fig 2.8 High-pass low-pass phase shifter

When the elements of Fig 2.8 are switched in the low-pass sate, the transmission coefficient is given by

$$S_{21} = \frac{2}{2(1-B_N X_N) + j(B_N + 2X_N - B_N X_N^2)} \qquad (2.14)$$

Where X_N and B_N represent the normalized reactance and susceptance, respectively. The transmission phase ϕ_1 is given by

$$\phi_1 = \tan^{-1} \; -\frac{B_N + 2X_N - B_N X_N^2}{2(1-B_N X_N)} \qquad (2.15)$$

When the circuit is switched to the high-pass state, the transmission coefficient S_{21} and the transmission phase ϕ_2 are obtained by replacing B_N by $-B_N$ and X_N by $-X_N$ in the previous equation. The differential phase shift is given by

$$\Delta\phi = \phi_1 - \phi_2 = 2\tan^{-1} \; -\frac{B_N + 2X_N - B_N X_N^2}{2(1-B_N X_N)} \qquad (2.16)$$

Assuming the phase shifter to be loss-less and imposing the condition of perfect match, i.e. $|S_{21}=1|$, we get phase shift as

$$\Delta\phi = 2\tan^{-1} \; \frac{2X_N}{X_N^2 - 1} \qquad (2.17)$$

The frequency response of the two filter circuits is such that as the frequency is increased, the increase in phase delay in the low-pass state is compensated by the decrease in phase advance in the high state. Thus a constant phase shift is obtained over a large bandwidth.

2.3.3.2 Embedded Switched Filters Phase Shifter

It can be seen that the High-pass Low-pass phase shifter can achieve constant phase shift with low VSWR over a fairly large bandwidth. But in such a design, the off state capacitance of the FETs tends to degrade the performance and limit the bandwidth of the phase shifter. The total capacitor shunting the high-impedance switch state is large. In order to realize the switching action, this capacitance must either be resonated or its effect must be included in the design of the impedance-matching sections. In both cases, bandwidth is limited.

By selection of appropriate circuit topologies, it is possible to incorporate switching FET off-state capacitances as filter elements. Since these capacitances are no longer undesired parasitic, high performance, broadband phase shifter response is more easily achieved. In this way, the maximum theoretical bandwidth that a high-pass low-pass section can provide is achieved despite non-ideal switching elements.

Their theoretical analysis is similar with the conventional one. The circuit takes into account of FET parameters as part of the filter networks so that the need to parallel resonate the off state capacitance can be eliminated. By doing this, the theoretical

bandwidth can be easily achieved [4, 13, 14]. Figs 2.9 and 2.10 show some typical circuit structures for switched components type phase shifter:

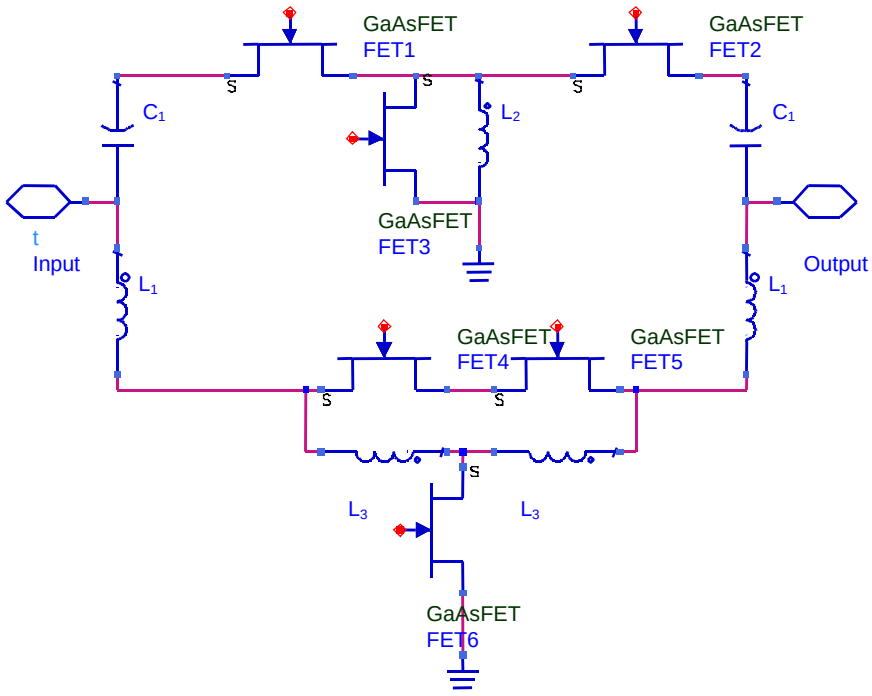


Fig 2.9 Embedded switched filter phase shifter-I

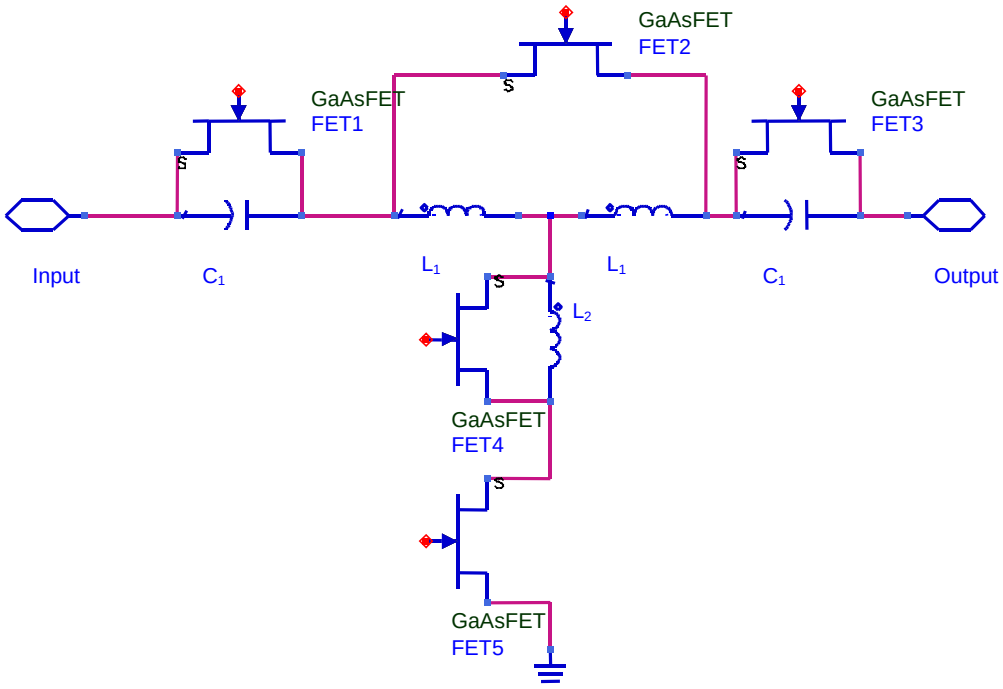


Fig 2.10 Embedded switched filter phase shifter-II

2.4 Recent Development of Digital Phase Shifter

In 1982, an X-Band GaAs monolithic passive phase shifter with 22.5°, 45°, 90° and 180° phase bits were developed using FET switches by Yalcin Ayasli [15]. By cascading all four bits, a four bit digital phase shifter with 5.1±0.6 dB insertion losses is realized on a single $6.4\times7.9\times0.1$ mm^2 chip. Although this chip is able to satisfy the insertion loss requirement of this project, it has a RMS phase error from 39.4° to 8.7° across X-Band frequencies. The large size is because of its extensive use of distributed components.

In 1988, state-of-art V-Band monolithic digital and analog phase shifters using FETs and varactor diodes have been developed [16]. At 60 GHz, the single-bit FET and varactor

branch-line phase shifter achieved 129° phase shift with insertion loss less than 11.4 dB and 54° with insertion loss less than 1.3 dB, respectively. Four cascaded FET branch-line phase shifters achieved 360° phase shift in 22.5° steps with insertion loss from 4.5 to 7.5 dB. Although the branch-line phase shifter has only an area of 1.5×2.3 mm^2, it must be noted that it is operating at 60 GHz. To use this design at lower frequency band would have much larger size of chip.

Also in 1988, a 2-18 GHz monolithic phase shifter for electronic phased array applications was developed [17]. The principle of operation is based on the quadrature vectorial theory. The originality of this device is to use one FET for the 180° phase shifter and high-pass low-pass filters for the 90° phase shifter. The recombination of modulation of the four vectors in quadrature is achieved by a conventional double-gate line, single-drain traveling wave combiner. The phase shifter requires 5 chips over 8.2×3 mm^2 and represents 10 dB insertion loss.

In 1988 again, a five bits MMIC phase shifter that covered over two octaves of bandwidth have been demonstrated [18]. The phase shifter composed of four separate phase shifter sections consisting of a 180° bit, a 90° bit, a 45° bit, and a combined 22.5°/11.25° bit section. The phase shifter has RMS phase error of 5.7° with average insertion loss of 10 dB. However, the phase shifter is rather large (8×5 mm^2).

A novel design for a MMIC 180° phase shifter was reported in 1992 [19]. The design is based on the high-pass low-pass filter phase shifter but with optimization to reduce the

number of components needed. The reduction of components can be achieved by changing the topology of the network with switching elements, thus reusing some components of the high-pass filter in the low-pass filter. Although this design reduces the size of the circuit, it also reduces the bandwidth of the phase shifter. Besides, the reduction of size is through reducing the number of capacitors and FETs, which is rather small on MMIC anyway. Therefore the saving in space that it has is not significant.

Finally, in 1995, a five bit MMIC phase shifter was described with the best reported performance levels over the 6 to 18 GHz band [20]. The phase shifter was specially designed to be tolerant of expected processing variations and to minimize production costs. The RMS phase error is reported as 4.7° and insertion loss of 14.1 dB. Again, the dimension of the completed chip is rather large (4.2×3.8 mm^2) because it uses 3 quarterwave couplers in the design.

Therefore, it can be seen that most of the previous designs had used distributed components, especially quarterwave couplers, thereby increasing the size of the phase shifters. Furthermore, some of the reported circuits have insertion loss > 8dB while others have RMS phase error > 5°. Thus, a different approach should be used to attempt to reduce the size of the phase shifter.

Chapter 3

Design Selections and Considerations

3.1 Introduction

Phase shifter design consists of choosing the circuit topology, then carefully setting up a model for optimization with CAD software, developing proper optimization criteria, fabrication and test [8]. In this chapter, we discuss aspects that the designer has to take into account in phase shifter design including broad selection criteria for phase shifters, the design consideration of switch devices as well as tolerable tradeoff expected to achieve a more complete design.

3.2 Phase Shifter Specifications

Multi-bit phase shifters are realized using one or more of the following circuit techniques: switched line, hybrid coupled, loaded line and high-pass low-pass. The choice between these topologies depends on the phase shifter specifications for a given application, such as the power handling capability, number of switch device, insertion loss, circuit complexity, and size.

The commonly specified electrical parameters of an electronic phase shifter are:

- Center frequency of operation: It is an important factor when choosing the design topology. We will discuss in detail in the following section.
- Bandwidth: The bandwidth of the phase shifters will affects the bandwidth of the whole system.

- Insertion Loss: The insertion loss should be as low as possible. In the transmitter mode, insertion loss in the phase shifter results in loss of transmitter power and heating of the phase shifter due to power dissipation. In the receiver mode, it results in lowering the signal-to-noise ratio. An insertion loss of about 0.8 dB is typical for phase shifters used in C and X-band radars.
- VSWR or Return Loss: The return loss should be as low as possible.
- Phase Shifter Error: This is a RMS (root-mean-square) phase error from the designed phase shift due to variations with frequency, phase state, power, and temperature. When considering a large number of phase shifters, the calculation of this error may include variations from unit to unit. Phase error reduces the antenna gain in a transmitting array and raises sidelobes in a receiving array. The RMS error permissible in a phase shifter typically is up to about 6°.
- Switching Time: The time needed to switch the phase shifter to a particular phase state should be as short as possible. Longer switching time will enlarge the minimum detectable radar range when nonreciprocal phase shifters are used or a burst of pulses is transmitted in different directions. Switching time requirements in practice normally lie in the range 1 μs to about 150 μs, which is easily met by the phase shifters.
- Driver and Driver Power: The driver circuit configuration is as important as the phase shifter, and the two are generally considered together as an integral package. The drive power to the phase shifter should be as small as possible. A large drive power generates more heat and may require a more complex driver.

- Power-Handling Capability: The transmitter power requirement depends on the radar range and data rate of the system design. In the transmitter mode, the phase shifter must be capable of handling much more power than in the receiver mode. The maximum power-handling capability in semiconductor phase shifters is decided by the topology of the phase shifters and the maximum voltage and current that the solid-state switches can withstand.
- Bit Phase Shifting: As compared with analog phase shifters, digital phase shifters offer greater speed of operation and ease in interface with control computers. The number of bits needed is determined by the radar design requirements, in particular, the number of radiating elements, element spacing, and scan angle increment. For larger arrays, the phase increment can be coarse; equivalently, number of bits can be smaller. Practical phased arrays generally use 4-bit phase shifters as a compromise among cost, size, insertion loss, and system performance. However, for applications that demand very low sidelobe levels with a fewer number of antenna elements, up to 8-bit phase shifters have been used.
- Physical Size and Weight: The inter-element spacing in an array is generally $\lambda/2$. Hence, the phase shifter module (with driver) should fit within cross-sectional area of $\lambda/2 \times \lambda/2$.

The phase shifter specifications for a given application are governed by the system requirements. For example, phased array radars employing thousands of elements particularly call for a careful selection of phase shifters, because the performance and cost of each phase shifter directly reflect on the overall performance and cost of the system.

For all application, it is desirable to have the insertion loss, drive power, and phase error as low as possible. It may be noted that in the case of active phase shifters, insertion gain is to be specified in place of insertion loss. The physical size and weight of the phase shifter should be minimized for use in mobile and airborne systems, whereas for ground based systems the requirements can be relaxed.

3.3 Comparison of Four Different Types of Phase Shifter Topology

After talking about the selection criteria of phase shifter, we will compare the performance of four different types of phase shifter in this section. We will also give the typical performance characteristics presented in the literature.

With appropriate choice of transmission media, all the four types of phase shifters can be fabricated in convenient sizes at microwave and millimeter-wave frequencies. But at lower frequency, because of the need to use long line lengths, the switched-line, hybrid coupled, and loaded-line phase shifters become physically large in size. The high-pass low-pass phase shifter is recommended because it is implemented using lump elements. Because of the more and more wide application of microwave and millimeter-wave circuits, this difference has distinguished.

The switched-line and reflection types of phase shifters are time delay devices. Phase shift will be proportional to frequency. For switched-line phase shifter, wide bandwidth may be achieved by using a Schiffman phase shifter in one of the transmission paths. The phase shift of the Schiffman coupled section is a linear function of frequency plus a sinusoidal

function of frequency. Wide bandwidth in the order of an octave can be achieved by careful design. For a hybrid coupled phase shifter, the bandwidth performance can be improved by suitably designing the reflective circuit to compensate for the frequency-dependent phase shift error due to the coupler. Another approach is to design the coupler and the reflective circuit independently so that each offers broadband performance.

When $\theta = 90°$, the loaded-line phase shifter has the best bandwidth performance. For example, for a 22.5° phase bit, the percentage bandwidth over which VSWR is <2 and phase shift error is <2% is reported to be about 43% when $\theta = 90°$, and 12% when $\theta = 75°$.

High-pass low-pass phase shifter has the potential of providing the greatest bandwidth. When the frequency is increased, the phase delay increase in the low-pass state is compensated for by phase advance lost in the high-pass state. The net effect is that the phase shift tends to stay matched as frequency changes. A phase shift of $90° \pm 2°$ is obtainable over almost an octave, while the smaller phase shifts are available over more than an octave. The bandwidth of the large phase-shift bits may be improved by using more elements in the high-pass and low-pass circuits.

Insertion Loss and Power Handling Capability:

For the switched-line phase shifter, both the peak power capability and the insertion loss are independent of the phase shift. On the other hand, in the hybrid coupled and loaded

line phase shifter bits, the smaller the phase shift is, the higher the peak power capability is and the smaller the insertion loss is.

If we consider a 180° phase bit, the switched line circuit offers the maximum peak power capability. The insertion loss is the same as that for the hybrid coupled bit. Another advantage of the switched line phase shifter is that switches contribution to insertion loss is practically the same in both the switching states, and any loss variation is due to the path difference between the two switched paths. The circuit is simple because no special matching circuit is required to equalize the insertion loss. The disadvantages are that it requires four switches per bit (for equal switch loss in the two bias states), whereas the hybrid coupled phase bit uses two switches. Secondly, the switched line phase bit requires complementary bias voltage for on and off paths of the circuit. Because the advantages outweigh the disadvantages, the switched-line is the most preferred configuration for the 180° bit. Where peak power is not a serious consideration, the hybrid coupled bit is also used.

For the 90° phase bit, the hybrid coupled configuration offers the best choice. This is because, while it has the same peak power capability as the switched line phase shifter phase bit, its insertion loss is less by a factor of $1/\sqrt{2}$.

In the case of a 45° phase bit also, the hybrid coupled configuration is commonly used, although the loaded line circuit offers a good alternative. The loaded line circuit is particularly suited for small phase bits 22.5° and 11.25° in size. The circuit is much

simpler. As it dispenses with the need to use any hybrid, the discontinuity effects are also reduced. Loaded line circuits with a small bit size are also best for maximum power handling. For 90° and 180° phase bits, although a three-element and a four-element model, respectively, are reported, from the point of view of performance, they do not score over the hybrid coupled and switched line circuits. The bandwidth of three-element and four-element models is small, and, furthermore, there is no saving in terms of number of switches used when compared with a hybrid coupled 90° phase bit and a switched line 180° phase bit. For high-pass low-pass phase shifter, the insertion loss is independent with phase shift.

Table 3.1 shows the choice of the cell structure versus frequency: [8-20]

Table 3.1
Choice of the cell structure versus frequency

Phase Shifter	4 bits			5 bits			6 bits		
Frequency Band	C	Ku	Ka	C	Ku	Ka	C	Ku	Ka
180°	I	II	II	I	II	II	I	II	II
90°	I	II	II	I	II	II	I	II	II
45°	IV	III	II	IV	III	II	IV	III	II
22.5°	IV	III	II	IV	III	II	IV	III	II
11.25°				IV	III	II	IV	III	II
5.625°							IV	III	II

I High-pass low-pass filters II Switched lines

III Loaded Lines IV Embedded switched filters

3.4 Switching Device

Switching device is the critical component of all kinds of electrical phase shifters. There are mainly two kinds of semiconductor switching devices: PIN diodes and GaAs FET based monolithic switches. In recent years the PIN diodes have been increasingly replaced by GaAs FET switches, especially for low power applications. Medium to high power GaAs FET switches are also being investigated. The main advantages of FETs over PIN diodes are simplified bias networks; ultra-fast switching speed (sub-nanosecond); simplified design of driver circuits; and compatibility for monolithic integration. Further more, for MMIC implementation, once they are fabricated on the same chip can enhance the design speed and high performance.

3.4.1 GaAs FET as a Passive Switch

The FET switch is a three terminal device in which the gate bias voltage V_{gs} controls the switch. The FET acts as voltage-controlled resistor in which the gate bias controls the drain-to-source resistance in the channel. In the passive mode of operation ($I_{ds} \cong 0$), the switch is in a low-impedance or on-state when $V_{gs} = 0$, and it is in a high–impedance or off-state when a negative bias voltage greater than the pinch-off voltage ($|V_{gs}| > |V_p|$) is applied. Fig 3.1 shows the two linear operating ranges of a GaAs MESFET switch. In order that the FET remains in its passive mode of operation, the drain-source voltage Vds of the FET should be less than the knee voltage, which is about 0.5 V. Since there is practically no drain current, the power consumption is negligible in both switching states.

The drive power required to charge or discharge the input gate capacitance during the transition between the two states is negligibly small. The switch is bi-directional.

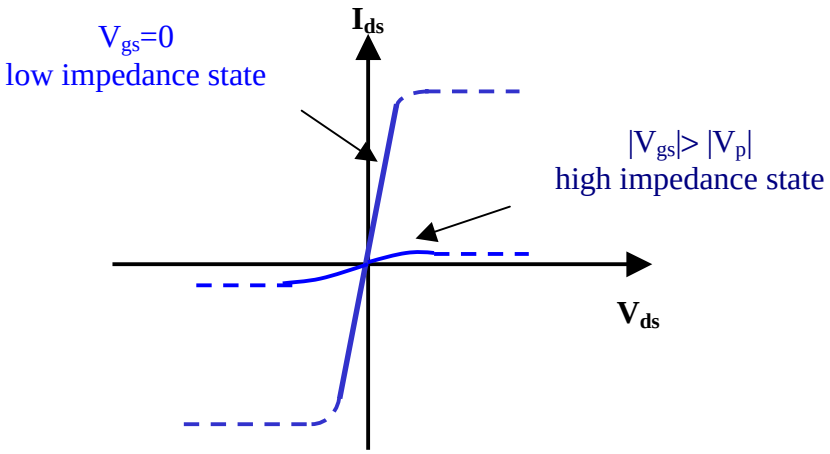


Fig 3.1 Linear regions of a MESFET switch at on/off states

The equivalent circuit parameters associated with the various regions for the two switching states on and off are shown in Fig 3.2 and Fig 3.3. The source is at ground potential and the drain is left floating (with no potential applied to it). The equivalent circuits shown do not include the lead inductances and the gate metallization resistance.

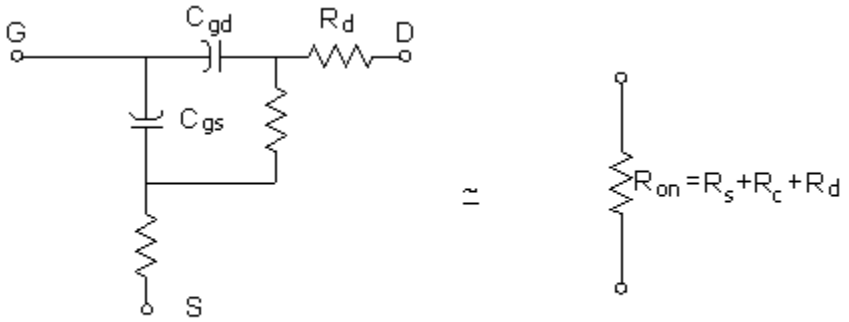


Fig 3.2 Equivalent circuit of MESFET switch in on-state

In the on-state ($V_{gs} = 0$), the depletion thickness under the gate is small. The channel region is virtually open except for the zero field depletion layer thickness. Because the drain is left floating, the gate-source and gate-drain capacitances (C_{gs} and C_{gd}) are unequal. The values of these capacitances, however, are very small and can therefore be neglected. The equivalent circuit, as a result, is reduced to a simple resistance between the source and drain. It is given by

$R_{on} = R_c + R_s + R_d$,

where R_c is the resistance of the portion of the channel below the gate , and R_s and R_d are due to the remaining portions of the channel on either side of the gate region. The value of R_{on} is typically in the range of 2Ω to 3Ω.

When the gate is negatively biased such that $|V_{gs}| > |V_p|$, the channel is almost completely depleted of charge carriers. The FET can then be modeled in terms of an equivalent circuit, as shown in Fig 3.3. The capacitance C_{ds} represents the fringing capacitance between the source and drain, and R_{ds}, which is in parallel with C_{ds} accounts for the channel resistance.

If the source and drain are both grounded, the depletion layer forms symmetrically about the gate. Therefore, in the on-state, we have $R_s = R_d$, so that

$R_{on} = R_c + 2R_s$

Similarly, in the off-state, $R_s = R_d$ and $C_{gs} = C_{gd}$. Since the source and drain are at the ground potential, the drain is not isolated from the gate terminal. The RF impedance of the gate bias circuit affects the equivalent drain-source impedance. In practice, the gate bias circuit is configured in order to present an effective RF open at the gate terminal. Under this condition, the equivalent source-drain capacitance can be approximated by $(C_{ds} + C_{gs}/2)$.

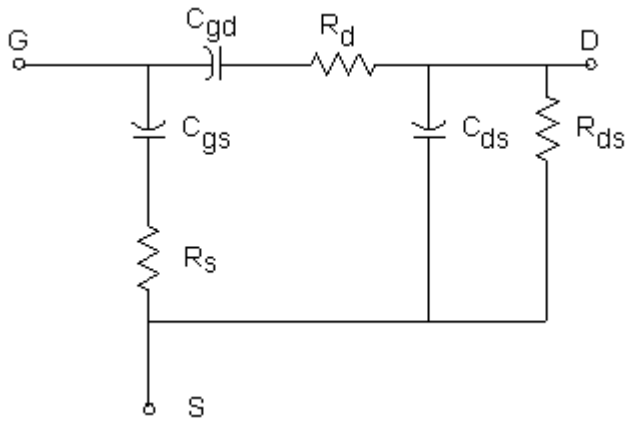
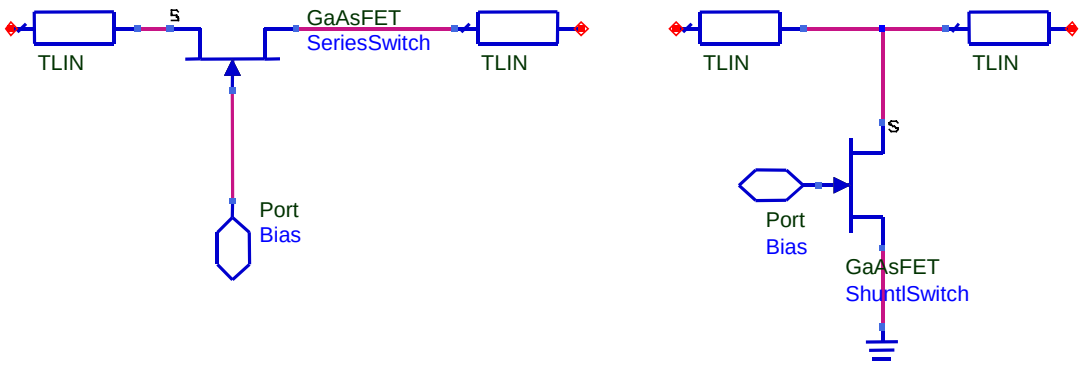


Fig 3.3 Equivalent circuit of MESFET switch in off-state

The different parameters are strongly affected by the physical parameters of the device like channel geometry, gate length, channel doping density and pinch-off voltage. The metallization scheme, gate structure influence the on state of the FET switch; the off-state impedance depends on the source-drain capacitance C_{ds}, its parallel resistance R_{ds} and the drain to gate and source to gate capacitance C_{gd} and C_{gs} and its associated series resistance R_d, R_g.

3.4.2 Design Considerations for a Switch FET

GaAs FET can be used either as series or shunt switches with respect to the transmission lines, as illustrated in Fig 3.4.



(a) **(b)**

Fig 3.4 Basic GaAs FET switch configurations (a) series (b) shunt

Switching circuits with FETs can be designed in essentially the same way as PIN diodes. There are, however, some salient features of FET switch circuit design that need to be mentioned.

The FET is a three-terminal device. The switching occurs only through the gate control voltages and no other bias is required for the operation of the phase shifter. The RF transmission lines do not carry any dc voltage and therefore there is no need for dc blocking capacitors between various switch elements: a significant design advantage.

Gate control voltage corresponding to the two switches are $V_{gs1} = 0$ V and $V_{gs2} = -V$ where $V > V_p$. In either state, the gate junction is reverse biased and the gate current is

either zero or negligible. Hence, the fact that switching control voltages need to be applied at negligible currents simplifies the requirements of the control circuit design.

In the off-state of the FET switch, note that gate-drain and gate-source capacitances are equal because both source and drain terminals are at ground potential. As a consequence of this, the drain terminal is not isolated from the gate terminal: the RF impedance of the gate bias circuit affects the equivalent drain-source impedance. In practice, the gate bias circuit is configured in order to present an effective RF open at the gate terminal. Under this condition, the equivalent off-state source-drain capacitance can be approximated by $(C_{ds} + C_{gs}/2)$ (referred as C_{off} in some literatures).

With the gate terminated in high impedance, the total drain capacitance (C_{off}) shunting R_{ds} represents a reactance of the order of 50 ohms at X-band frequencies. This capacitance is not large enough to approximate an ideal open circuit between the source and drain terminals at high frequencies. Thus, although the transistor is in its "OFF" state, there is still signal pass through the source and drain terminals of the MESFET. When the FET is used as a series switch, the off state capacitance degrades the isolation as higher frequencies. On the other hand, when the FET is used in a shunt configuration, this capacitance degrades the insertion loss. Therefore, to realize the switching action, this capacitance must be either resonated or its effect must be included in the design of the impedance matching sections. This is an important design consideration for FET switches, as it directly relates to the operation bandwidth.

Chapter 4

3 Phase-State Phase Shifter

4.1 Introduction

In chapters 1 to 3, we described various types of phase shifters. Various types of digital phase shifters have been developed in which each bit controls a circuit with 2 phase-states. The number of bits and their corresponding circuits increase with differential phase-shift resolution resulting in an increase of chip area. In integrated circuit design, an important consideration is the reduction of chip area without compromising device performance. To reduce the number of circuits and hence the chip area, the concept of 3 phase- state circuit was proposed by K. Nakahara in 1993 [14]. Nakahara added switches to convert a 2 phase-state phase shifter to a 3 phase-state phase shifter.

The idea of a 3 phase-state phase shifter is unconventional. Hence we first discuss Nakahara's concept in relation to the 2 phase-state circuit using block diagrams. Next, we discuss Nakahara's circuits used to implement these blocks and explain how the reduction in area is achieved. After this we introduce the 3 phase-state phase shifter proposed by the author again using block diagrams. The circuit implementation is discussed in the next chapter.

4.2 2 Phase-State Phase Shifter

In a 2 phase-state phase shifter, the circuit for each bit has two phase states. If the output phases of the two states are ϕ_1 and ϕ_2, the differential phase shift offered by the device is given by $\Delta\phi = \phi_2 - \phi_1$. In phased array radars differential phase shifts are required. A

digital phase shifter consists of a cascade of several circuits with differential phase shifts incremented in binary steps. In an n-bit phase shifter, the entire range of 0° and 360° is covered in 2^n steps. 2^n discrete differential phase shifts are provided. The smallest phase is $(360^0/2^n)$ and the largest phase is 180°.

A block diagram of a three bit phase shifter is given in Fig 4.1.

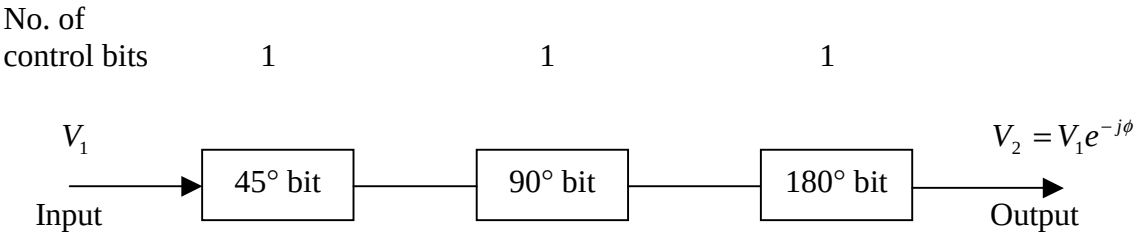


Fig 4.1 Block diagram of a three-bit phase shifter

As shown in Table 4.1, differential phase shifts can be incremented in steps of 45° to cover the full range of 0° to 360°.

Table 4.1 Switching states for the circuit blocks in Fig 4.1

Switching State			Output Phase Degrees	Differential Phase Shift Degrees
0	0	0	ϕ_0 (reference state)	0^0
1	0	0	(ϕ_0 + 45 °)	45 °
0	1	0	(ϕ_0 + 90 °)	90 °
1	1	0	(ϕ_0 + 135 °)	135 °
0	0	1	(ϕ_0 + 180 °)	180°
1	0	1	(ϕ_0 + 225 °)	225 °
0	1	1	(ϕ_0 + 270 °)	270 °
1	1	1	(ϕ_0 + 315 °)	315 °

4.3 3 Phase-State Phase Shifter

Fig 4.2 shows a 2 phase state 5 bit phase shifter with 5 control bits providing 2^5 or 32 discrete phase steps. Unlike in Fig 4.1, which follows the practice of giving block diagrams of 2 phase state phase shifters, the two differential phase states controlled by each bit are indicated in circuit blocks in order to facilitate the discussion of 3 phase state phase shifters.

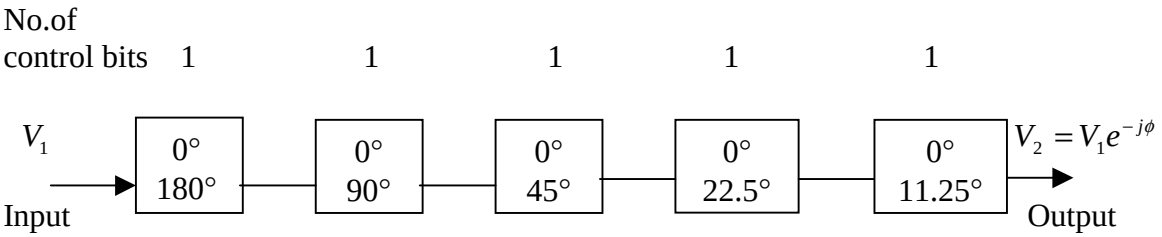


Fig 4.2 A 2 phase-state 5 bit phase shifter

If circuit blocks with three digitally controlled phase states can be used, and if these each circuit block requires about the same chip area as a 2 phase-state circuit block, the required chip area is reduced. This is the motivation for the design of a 3 phase-state phase shifter.

4.3.1 K Nakahara's Scheme of a 3 Phase-State Phase Shifter

The only 3 phase-state phase shifter reported in published literature is due to K. Nakahara [14]. Fig 4.3 shows a block diagram of a 2 phase-state phase shifter providing 32 discrete differential phase shifts together with a block diagram of Nakahara's design which also provides 32 discrete differential phase shifts. It is seen that the first three circuit blocks, each with two phase states, have been replaced by two circuit blocks with three phase states. The remaining 22.5^0 and 11.25^0 circuit blocks are 2 phase-state circuit blocks. Note that each 3 phase-state circuit block requires two bits for control. Only three of four

values of the two control bits are required to control 3 phase states. The remaining value is unused.

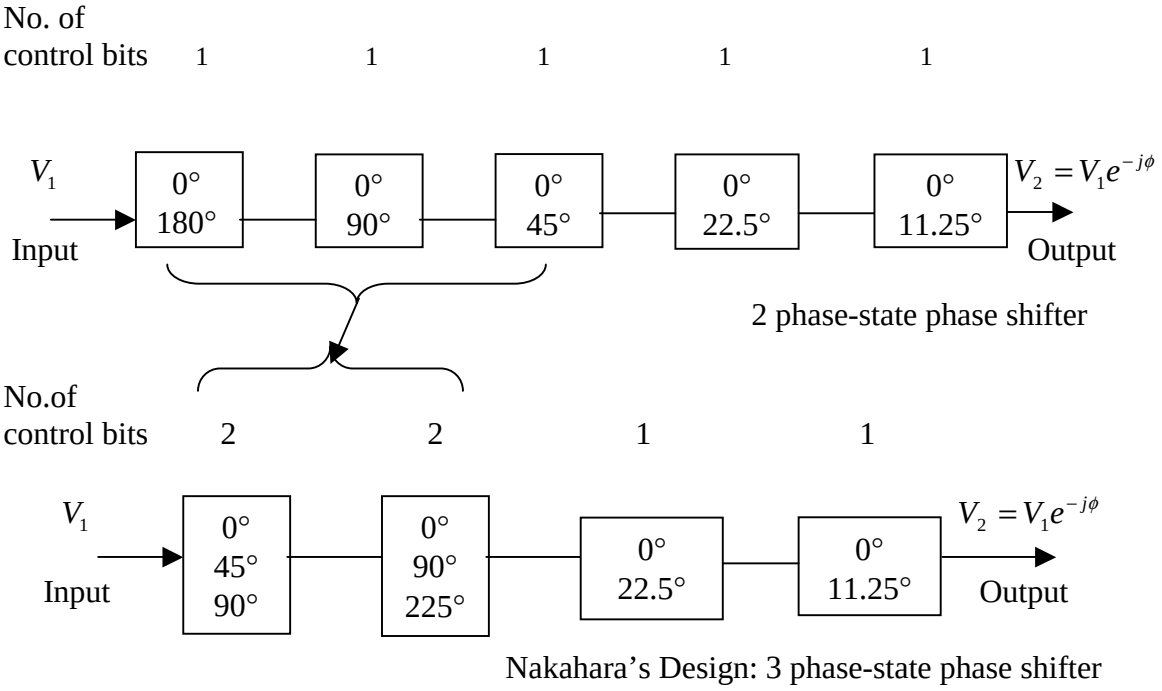


Fig 4.3 Block diagram of 2 phase-state phase shifter and Nakahara's design of 3 phase-state phase shifter

The 2 phase-state phase shifter requires 5 control bits and provides 2^5 or 32 discrete differential phase shifts. Nakahara's design requires 6 control bits but it does not produce 2^6 or 64 discrete phase steps, it provides 32 discrete phase steps. Thus it may be confusing to designate Nakahara's design a 5 bit phase shifter – it is equivalent to a 5 bit 2 phase-state phase shifter, but it requires 6 control bits.

Fig 4.4 shows the block diagram of Nakahara's two 3 phase-state phase shifter stages and the phasor diagram of its output. From the phasor diagram, it can be seen that the two 3 phase-state blocks produce the same phase shifts as the three $0^0/180^0$, $0^0/90^0$ and $0^0/45^0$ blocks of the 2 phase-state phase shifter.

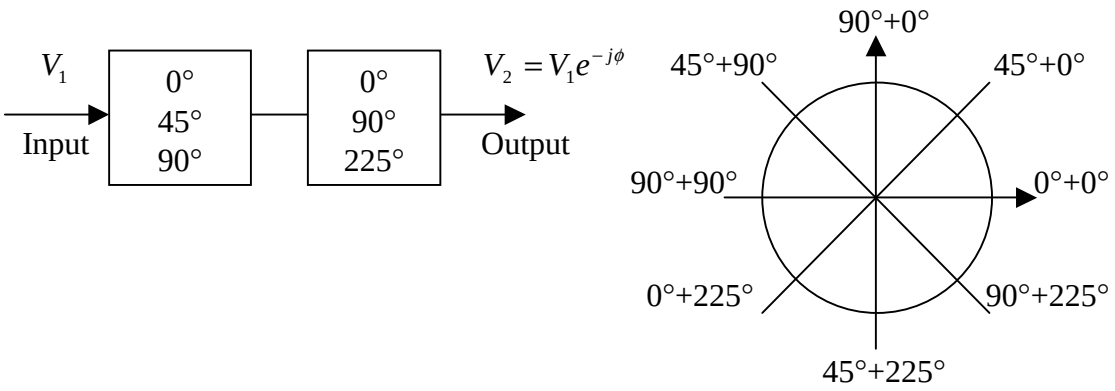


Fig 4.4 Block diagram of Nakahara's two 3 phase-state phase shifter stages and phasor diagram of the output

4.3.2 K Nakahara's Circuits for 3 Phase-State Phase Shifter Blocks

Fig 4.5 and Fig 4.6 show the schematic circuits of two types of 3 phase-state reflection phase shifters described by Nakahara [14]. In both circuits Nakahara added switches to convert a 2 phase-state phase shifter to a 3 phase-state phase shifter. Ignoring the area required by switches, Nakahara's scheme requires 2/3 of the area required by one additional phase state was added to the conventional reflection type phase shifter consisting of a 3 dB coupled line.

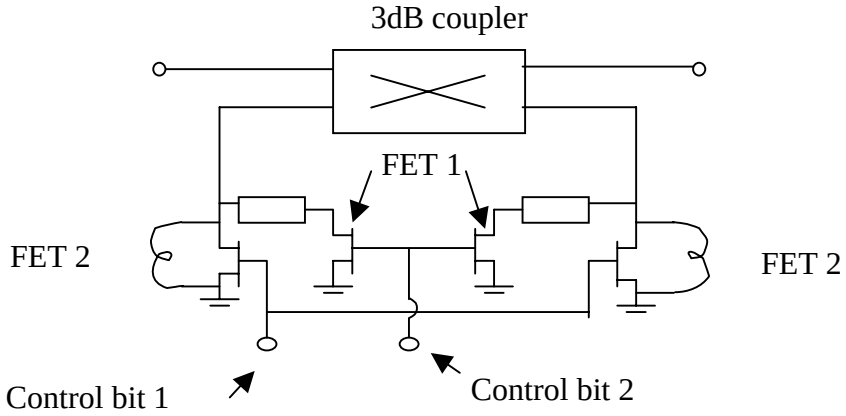


Fig 4.5 Schematic circuit diagram of a reflection-type phase shifter (Type 1)

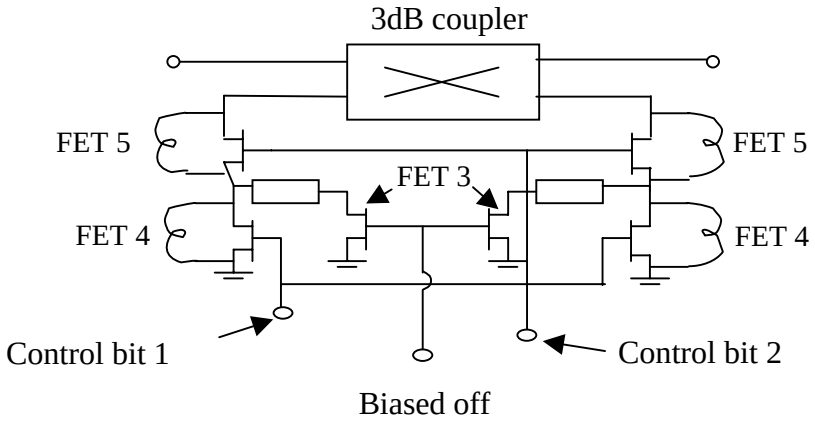


Fig 4.6 Schematic circuit diagram of a reflection-type phase shifter (Type 2)

For reflection-type phase shifter (type1 and type2), the transmission coefficient S_{21} and its phase factor $\angle S_{21}$ are expressed as:

$$S_{21} = -j\Gamma_T = -j\frac{jX_T - 1}{jX_T + 1} \qquad (4.1)$$

$$\angle S_{21} = Arc\tan(\frac{1 - X_T^2}{2X_T}) = \frac{\pi}{2} - \theta \qquad (4.2)$$

where Γ_T and $X_T (= \tan\theta)$ are the reflection coefficient and the normalized reactance of the terminating network respectively. Γ_T and X_T vary while the switch state of the switches changes. For example, in the circuit of Fig 4.5, the terminating network consists of a transmission line terminated by switches FET1 and FET2. There is an inductor which is connected in parallel with switch FET2 to resonant the drain-to-source capacitance C_{ds} of FET2 so that FET2 can be considered as short when it is on. Differential phase shifts of $0^0/45^0/\ 90^0$ and $0^0\ /90^0\ /225^0$ can be obtained respectively for type 1 and type 2 by different switching configurations of the FETs. Tables 4.1 and 4.2 show the switching states, equivalent circuits, and output phases as well as differential phase shifts of two types of the novel reflection type 3 phase-state phase shifters.

Table 4.2 Switching state and phase output for the reflection-type phase shifter (Type 1)

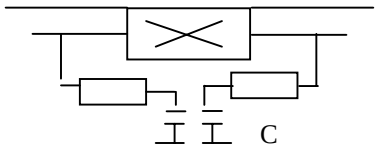
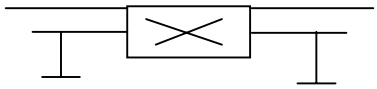
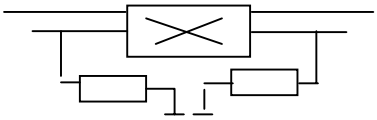
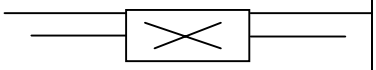
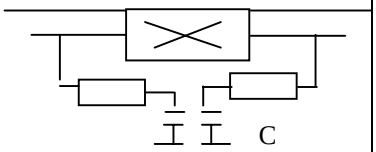
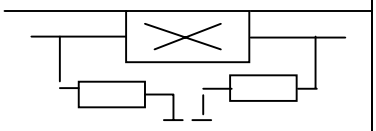
Switching State	FET 1	FET 2	$\angle S_{21}$	Differential Phase Shift	Schematic for phase shifter
1	off	off	135°	90°	
2	on	on	90°	45°	
3 (ref.)	on	off	45°	0°	

Table 4.3 Switching state and phase output for the reflection-type phase shifter (Type 2)

Switching State	FET 3	FET 4	FET5	$\angle S_{21}$	Differential Phase Shift	Schematic for phase shifter
1	on	off	off	270°	225°	
2	off	off	on	135°	90°	
3 (ref.)	on	off	on	45°	0°	

In Table 4.2, the phase difference between state 2 and state 3 is 45° and between state 1 and state 3 is 90°. Thus type 1 behaves like a 0°/45°/90° 3 phase-state phase shifter. In Table 4.3, the phase difference between state 2 and state 3 is 90° and between state 1 and state 3 is 225°. Thus type 2 behaves like a 0°/90°/225° 3 phase-state phase shifter.

There is another type of 3 phase-state phase shifter presented by K. Nakahara. Fig 4.7 shows schematic diagram of a conventional loaded-line-type phase shifter and a novel 3 phase-state loaded-line-type phase shifter.

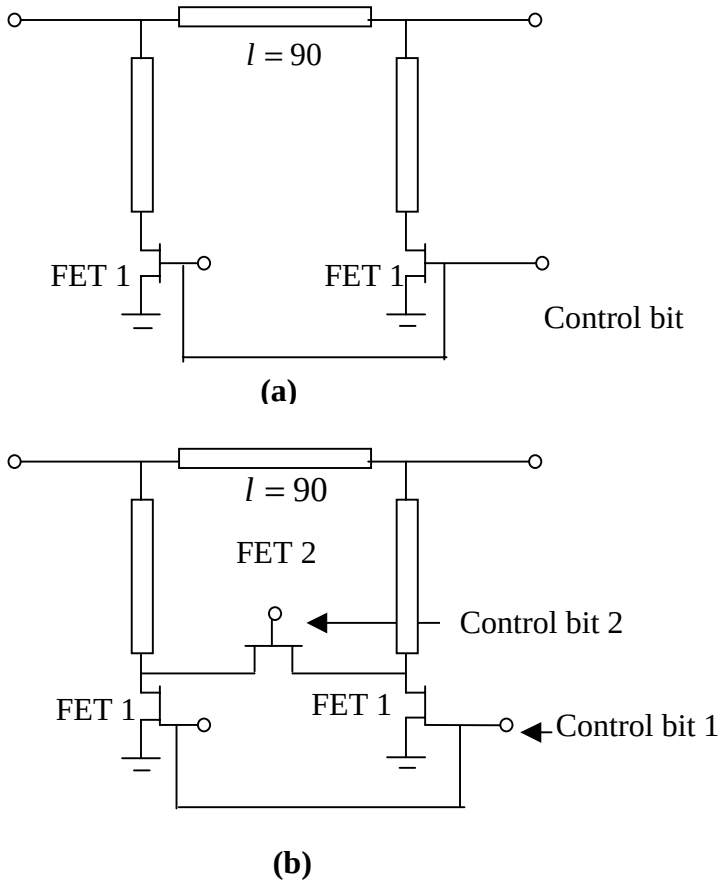
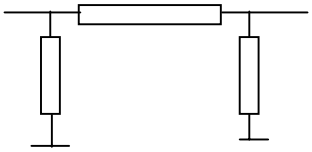
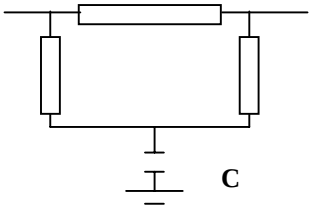
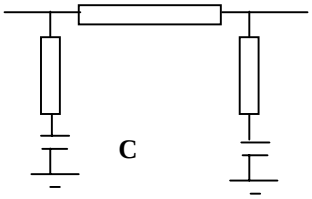


Fig 4.7 Schematic circuit of loaded-line phase shifters (a) conventional (b) 3 phase state

The loaded-line-type 3 phase-state phase shifter has one more phase state by adding a switching FET. Thus, ignoring the area required by the additional FETs, the 3 phase-circuit reduces area by 2/3. The switch states and equivalent circuits of 0°/11.25°/22.5° novel loaded-line-type 3 phase-state phase shifter are shown in Table 4.4.

Table 4.4 Switching state and phase output for the 0°/11.25°/22.5° loaded-line-type 3 phase-state phase shifter

Switching State	FET 1	FET 2	$\angle S_{21}$	Differential Phase Shift	Schematic for phase shifter
1	off	off	101.25°	22.5°	
2	off	on	90°	11.25°	
3 (ref.)	on	off	78.75°	0°	

K. Nakahara's paper presents the measured results of the phase shifter in Fig 4.3 and a 0°/11.25°/22.5° novel loaded-line-type 3 phase-state phase shifter as described in Fig 4.7. Chapter 6 will give a comparison between the performance of the reflection/loaded-line 3

phase-state phase shifters and the novel 3 phase-state phase shifter that we proposed in this project.

4.4 3 Phase-State Phase Shifter Proposed by the Author

Although Nakahara's design saves area by using two 3 Phase-State circuit blocks for the 180°, 90° and 45° bits, it employed transmission lines which can require long lengths. After the development of the embedded switched filter [13], there appears to be a general agreement that the switched filter circuit is the best topology for minimizing chip area definitely for the 180^0 bit and perhaps also for the 90^0 bit.. For very low phase shifts (say 5.625^0 for a 6-bit phase shifter), transmission line circuits are topologies of choice because of small lengths of transmission lines needed. For the medium range bits, there does not appear to be any agreement - both switched filter and transmission line circuit topologies have been investigated. For example a loaded transmission line topology is employed for 11.5^0, 22.5^0 and 45^0 bits in the 6-bit phase shifter by Andricos et al [21]. The same topology has been used for 22.5^0 and 45^0 bits in the X-band 4-bit phase shifter reported by Ayasli et al [15]. On the other hand, Reber and Felde [22] have used the switched filter topology for all six bits. It should be noted that all the phase shifters in the references cited above operate in the X-band.

The above discussion shows that it may not be worthwhile to pursue research for minimizing chip area by employment of 3 phase-state phase shifters for the 180^0,90^0 and 45^0 bits of a conventional 5-bit phase shifter. It may be more worthwhile to investigate 3 phase-state phase shifters for replacement of the 45^0, 22.5^0 and 11.25^0 bits for which the

jury is not yet out on the best topology for minimizing chip area. Consequently, the scheme investigated in this thesis is shown in the Figure below:

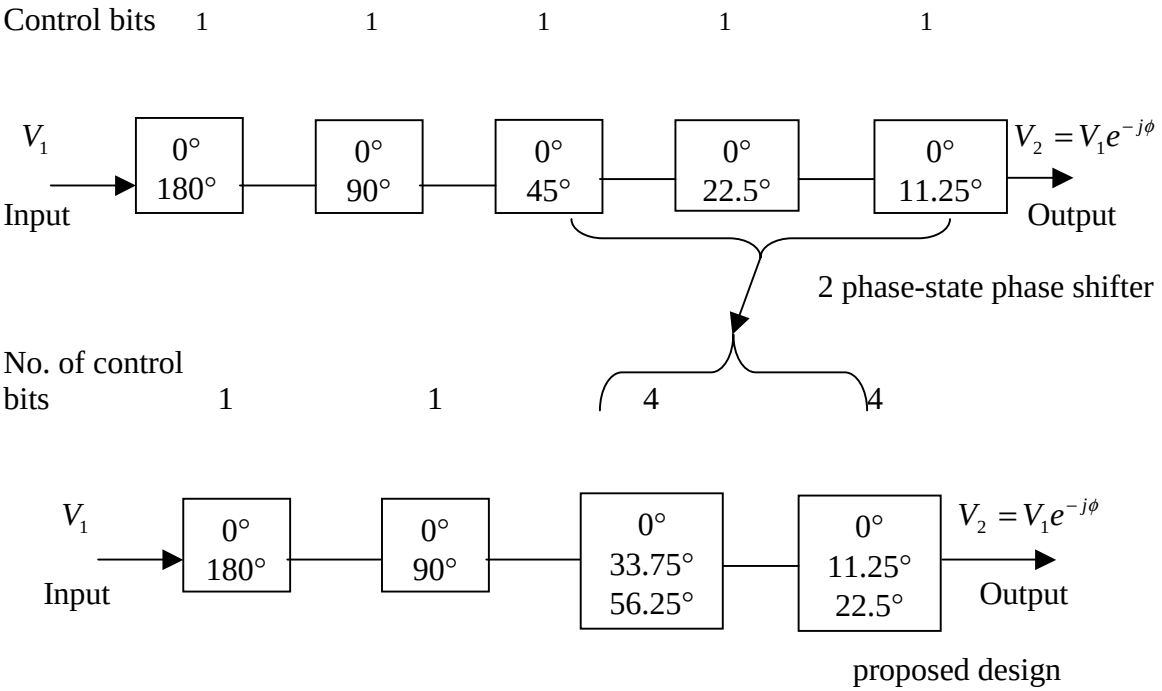


Fig 4.8 Block diagram of 5 stage 2 phase-state and 4 stage 3 phase-state phase shifter

As seen in the figure, two 3 phase-state blocks replace 11.25^0, 22.5^0 and 45^0 bits of the 2 phase-state phase shifter. The reason for the requirement of 4 control bits for each circuit block is given in the circuit implementation of the 3 phase-state blocks discussed in Chapter 5.

Fig 4.9 shows the block diagram of two 3 phase-state phase stages of Fig 4.11 and the phasor diagram of its output. From the phasor diagram, it can be seen that the two 3 phase state blocks produce the same phase shifts as the three 45^0, 22.5^0 and 11.25^0 blocks of the 2 phase-state phase shifter. Notice that all the phase shifts are in the first quadrant.

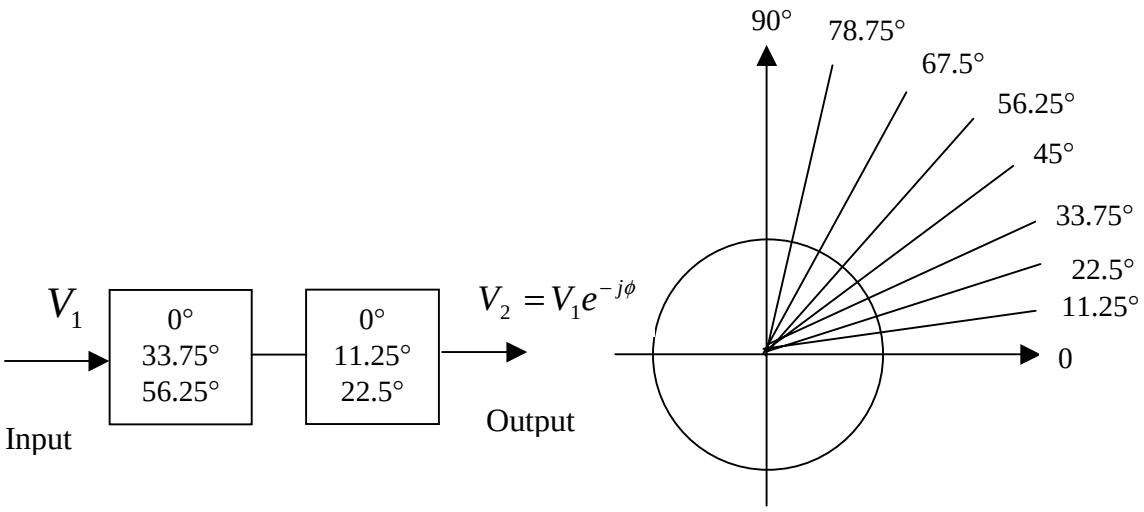


Fig 4.9 Block diagram of two 3 phase-state phase shifter stages and phasor diagram of the output

The circuit diagram, design and implementation of the 3 phase-state circuit blocks are discussed in Chapter 5.

Chapter 5

Circuit Design and Implementation

5.1 Introduction

Block diagrams of proposed 3 phase-state phase shifters are given in Chapter 4. In this Chapter, we discuss their circuit implementation. The circuit uses L-sections formed by inductors, capacitors and FET switches.

5.2 Circuit Implementation of the Proposed 3 Phase-State Phase Shifter Circuit Blocks

Fig 5.1 shows the circuit diagram for both $0^0 / 33.75^0 / 56.25^0$ and $0^0 / 11.25^0 / 22.5^0$ 3 phase-state circuit blocks discussed in Chapter 4.

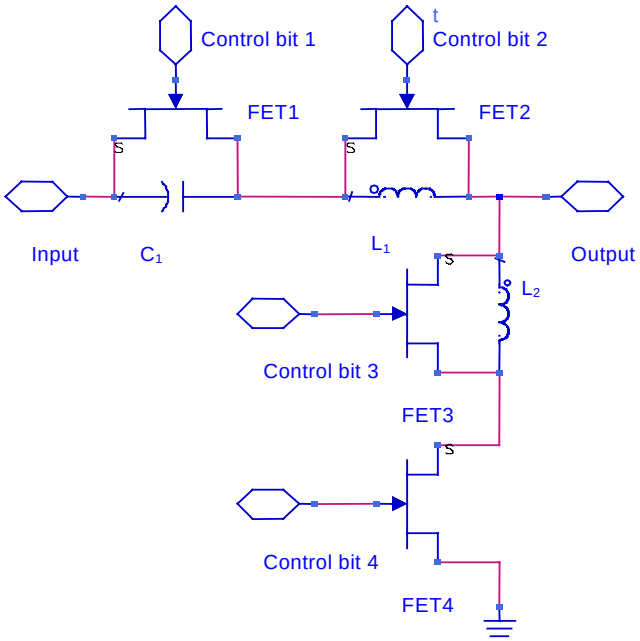


Fig 5.1 Circuit diagram of the 3 phase-state phase shifter circuit blocks

Unlike in a high-pass/low-pass filter phase shifter [13], in which high pass and low pass filters are switched, switching action in this circuit results in three different L-sections (explained later).

Table 5.1 shows the switching states, designed output phase as well as differential phase shifts which correspond to the $0^0 / 33.75^0 / 56.25^0$ and $0^0 / 11.25^0 / 22.5^0$ 3 phase-state circuit blocks discussed in Chapter 4. Note that there are four control signals and hence four control bits in Fig 5.1 to control the switching of the four FETs. Thus each 3 phase-state circuit proposed here requires four control bits and four FETs.

Table 5.1 Switching states, output phase and differential phase shifts for the circuit of Fig 5.1

Switching States	FET 1	FET 2	FET 3	FET 4	$0^0 / 33.75^0 / 56.25^0$		$0^0 / 11.25^0 / 22.5^0$	
					Output Phase	Differential Phase Shift	Output Phase	Differential Phase Shift
1	Off	On	Off	On	30^0	56.25^0	15^0	22.5^0
2	On	On	Off	On	7.5^0	33.75^0	3.75^0	11.25^0
3 (Ref.)	On	Off	On	Off	-26.25^0	0^0	-7.5^0	0^0

The circuit can have 2^4 or 16 switched states (corresponding to 4 control bits switching 4 FETs) out of which only three are used to obtain the three phase states. The 4 control bits can be obtained from 2 control bits using a 2 to 4 encoder. The reasons for the choice of the three switching states for the FET as well as the output phases, as given in Table 5.1, are as follow:

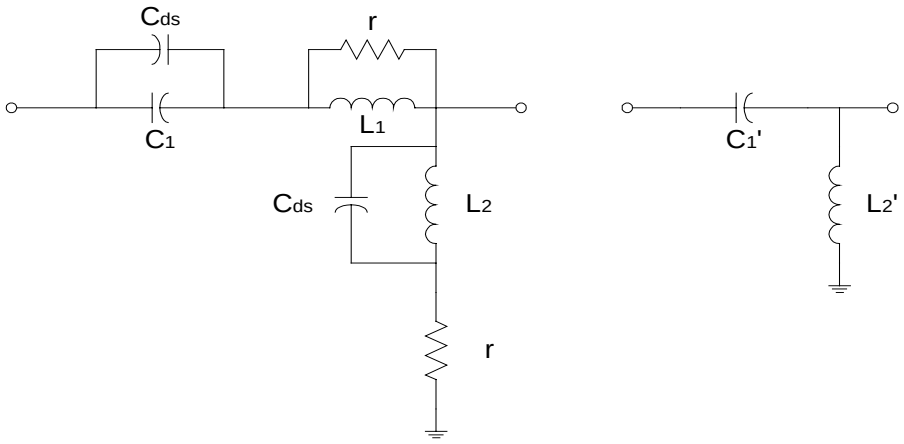
- Half of the switching states of the FETs do not result in LC networks; they result in C-C or L-L network.

- An LC L-section network has a good bandwidth when the output phase has a low value. As differential phase shift is important in phased array radars, we have chosen low values of output phases of the LC L-sections, which provide the required differential phase shifts.

The equivalent circuits resulting from switching action as shown in Table 5.1 together with their simplified equivalent LC L-sections are explained next.

5.2.1 State 1 (FET1 FET3 off, FET2 FET4 on)

The circuit can be reduced to the form shown in Fig 5.2 (a). The off-state impedance of an FET switch is represented by the capacitor, C_{ds}. The resistor, r, represents the on-state impedance of an FET switch. As the on-state resistance, r, is very small compared with the impedance in parallel, it can be approximated by a short circuit. Further, if we ignore component losses, the circuit can be further simplified to the form shown in Fig 5.2 (b). Note that FET off-state capacitances are absorbed in the components. The simplified circuit represents a high-pass LC L-section, which produces phase advance.



(a) **(b)**

Fig 5.2 Equivalent circuit when FET1 FET3 off, FET2 FET4 on

5.2.2 State 2 (FET3 off, FET1 FET2 and FET4 on)

The circuit reduces to the form shown in Fig 5.3 (a). For the same reason given for State 1, the circuit can be further simplified to the form shown in Fig 5.3 (b). This is a special case of the high-pass LC network shown in Fig 5.2 (b) with the capacitance of the series arm replaced by a short circuit. The analysis in next section will show that the circuit produces phase advance similar to a high-pass LC network of Fig 5.2 (b).

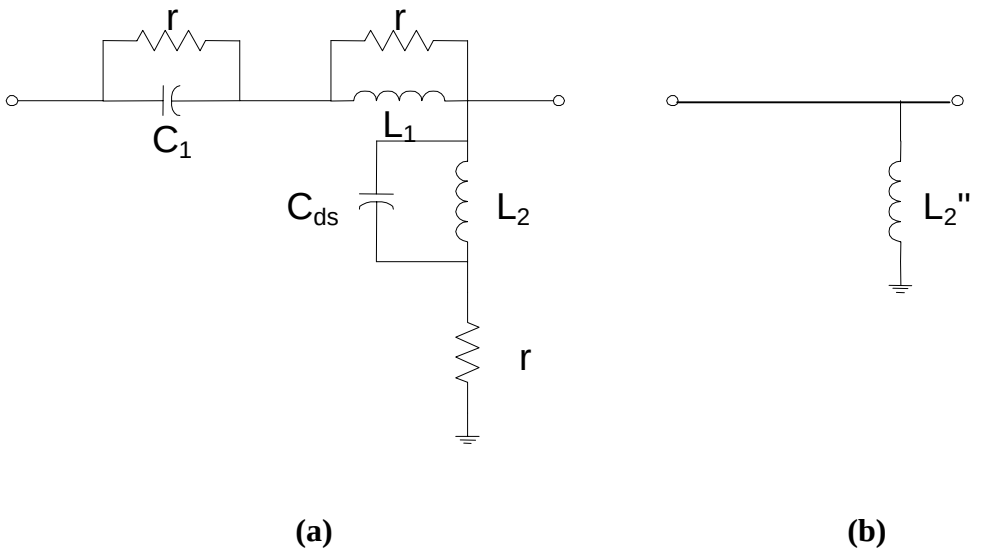
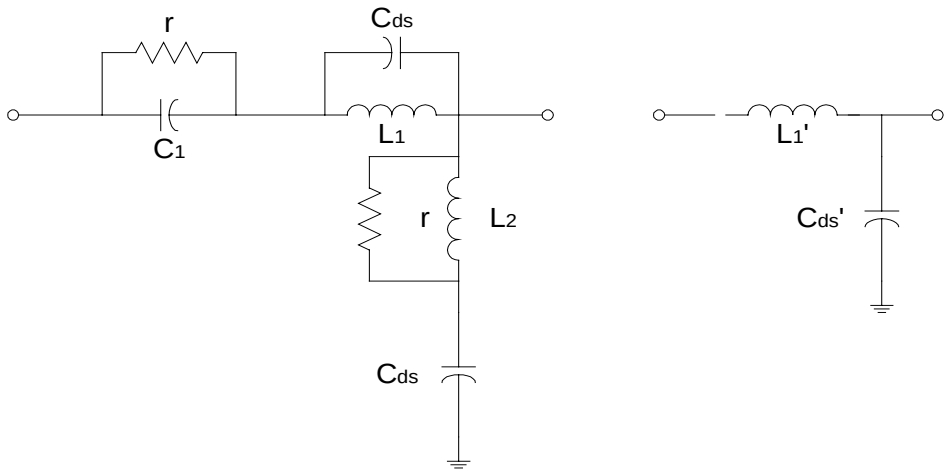


Fig 5.3 Equivalent circuit when FET3 off, FET1 FET2 FET4 on

5.2.3 State 3 (FET1 FET3 on, FET2 FET4 off)

The circuit reduces to the form shown in Fig 5.4 (a). For the same reason given for State 1, the circuit can be further simplified to the form shown in Fig 5.4 (b). The simplified circuit represents a low-pass LC L-section, which produces phase delay.

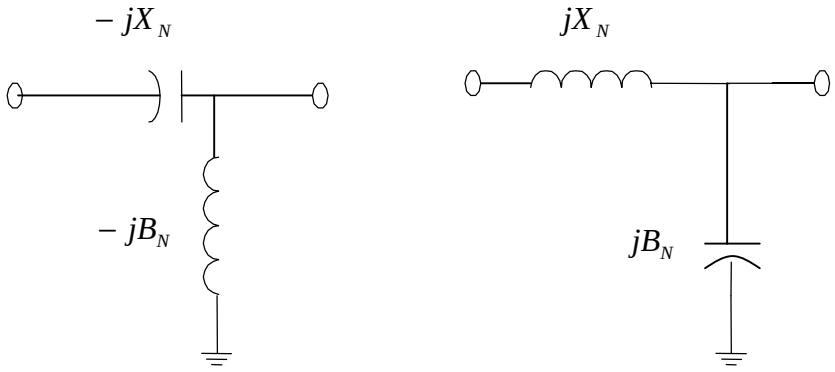


(a) **(b)**

Fig 5.4 Equivalent circuit when FET2 FET4 off, FET1 FET3 on

5.3 Phase Shift and Insertion Loss in L-sections

In Sec. 5.2 we showed that switching action in the proposed 3 phase-state phase shifter circuit block together with the lossless approximation reduces the circuit to lossless L-sections. Thus we need to obtain formulae for insertion loss and phase shift for the L-sections shown in Fig 5.5.



(a) **(b)**

Fig 5.5 LC filter circuit (a) high-pass (phase advance) (b) low-pass (phase delay)

5.3.1 Analysis of the Circuit of Fig 5.5 (a)

Note that Fig 5.5 (a) represents state 1 discussed in Sec.5.2.The analysis of this circuit can be easily carried out by cascading the normalized ABCD matrices of the series and shunt arms to obtain the overall normalized ABCD matrix. Note that the normalizing impedance is Z_0 (=50 Ω in actual designs) and normalized element values are distinguished from the unnormalized values by the subscript N .

The normalized ABCD matrix for the elements of Fig 5.5 (a) (high–pass state) is given by,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & -jX_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ -jB_N & 1 \end{vmatrix} = \begin{vmatrix} 1-X_N B_N & -jX_N \\ -jB_N & 1 \end{vmatrix} \qquad (5.1)$$

where

$$X_N = X / Z_0 = 1/C\omega Z_0 \qquad (5.2)$$

$$B_N = BZ_0 = Z_0 / L\omega \qquad (5.3)$$

The scattering matrix element, S_{21}, in terms of the normalized ABCD matrix is given by,

$$S_{21} = \frac{2}{A+B+C+D} = \frac{2}{2-X_N B_N - j(X_N + B_N)} \qquad (5.4)$$

The transmission phase is given by,

$$\angle S_{21} = \tan^{-1}\left[\frac{X_N + B_N}{2 - X_N B_N}\right] \qquad (5.5)$$

The insertion loss is given by,

$$|S_{21}| = \sqrt{\frac{4}{(2 - X_N B_N)^2 + (X_N + B_N)^2}} \qquad (5.6)$$

$$= \sqrt{\frac{4}{4 + X_N^2 B_N^2 - 4X_N B_N + X_N^2 + B_N^2 + 2X_N B_N}}$$

$$= \sqrt{\frac{4}{4 + X_N^2 B_N^2 - 2X_N B_N + X_N^2 + B_N^2}}$$

when $X_N = \frac{B_N}{1 + B_N^2}$, (5.7)

$$|S_{21}|_{\min} = \sqrt{\frac{4}{4 + \frac{B_N^4}{1 + B_N^2}}} \qquad (5.8)$$

In the limit, $B_N << 1$,

$$\frac{B_N^4}{1 + B_N^2} \approx 0 \qquad (5.9)$$

The minimum insertion loss, $|S_{21}|_{\min} \approx 1 \approx 0$ dB (5.10)

Fig 5.6 shows the graphs of X_N versus B_N for constant values of phase-advance (eqn.5.5) and insertion loss (eqn. 5.6), with eqn. 5.7 giving the graph for $|S_{21}|_{\min}$. Note that $|S_{21}|_{\min} = 0$ dB only in the limit $B_N << 1$. These constant contours of Fig 5.6 allow for the design consideration of minimum insertion loss for a desired output phase, as discussed later. Since B_N and X_N are frequency dependent, the insertion loss and phase shift are functions of frequency. Although the design is done at the centre frequency, bandwidth requirements may have to be considered for making design choices.

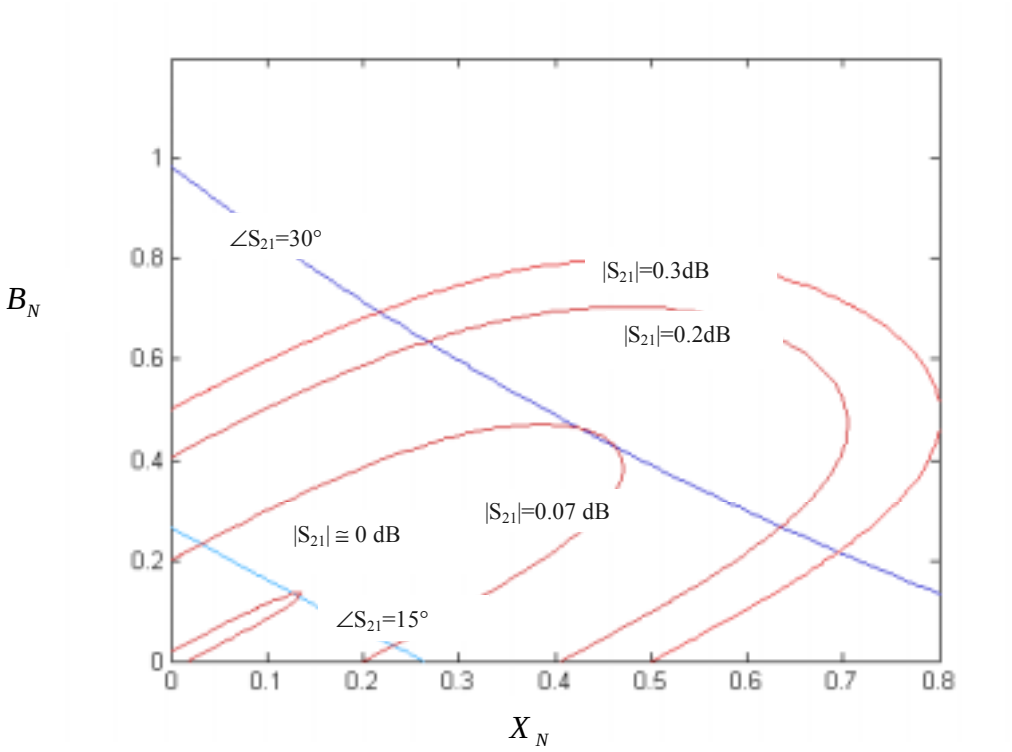


Fig 5.6 Graphs of X_N and B_N for constant values of phase advance and insertion loss for the circuit of Fig 5.5 (a)

5.3.2 Analysis of the Circuit of a Special Case of Fig 5.5 (a)

Fig 5.7 shows a special case of high pass L network of Fig 5.5 (a), which only consists of a short circuited series arm and a shunt inductive arm. It represents the simplified circuit for state 2 of Sec. 5.2.

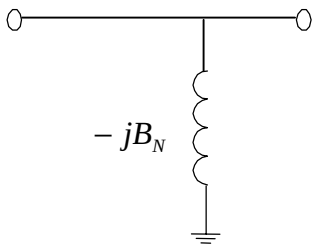


Fig 5.7 Special case of Fig 5.5 (a)

The normalized ABCD matrix is given by,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & 0 \\ -jB_N & 1 \end{vmatrix} \tag{5.11}$$

where

$$B_N = BZ_0 = Z_0 / L\omega \tag{5.12}$$

The scattering matrix element, S_{21}, in terms of the normalized ABCD matrix is given by,

$$S_{21} = \frac{2}{A+B+C+D} = \frac{2}{2-jB_N} \tag{5.13}$$

The transmission phase is given by,

$$\angle S_{21} = \tan^{-1}\left[\frac{B_N}{2}\right] \tag{5.14}$$

The insertion loss is given by,

$$\left|S_{21}\right| = \sqrt{\frac{4}{2^2 + B_N{}^2}} \tag{5.15}$$

In the limit, $B_N << 1$,

The minimum insertion loss, $\left|S_{21}\right|_{\min} \approx 1 \approx 0$ dB (5.16)

Since there is only one component in the network in Fig 5.7, the phase advance and insertion loss are all decided by the value of B_N as shown in equations 5.14 and 5.15. Figure 5.8 shows the curves of the $\angle S_{21}$ and $|S_{21}|$ versus B_N. Compared to the insertion loss and phase advance contours vs. X_N and B_N in Fig 5.6, the insertion loss in Fig 5.8 is fixed once the phase advance is decided. For small phase advance, the insertion loss is approximately 0. For example, for the phase advances of 3.75˚ and 7.5˚ as given in Table 5.1, $|S_{21}|$ is larger than 0.98 corresponding to the insertion loss smaller than 0.17 dB. This explains the choice of the circuit for state 2.

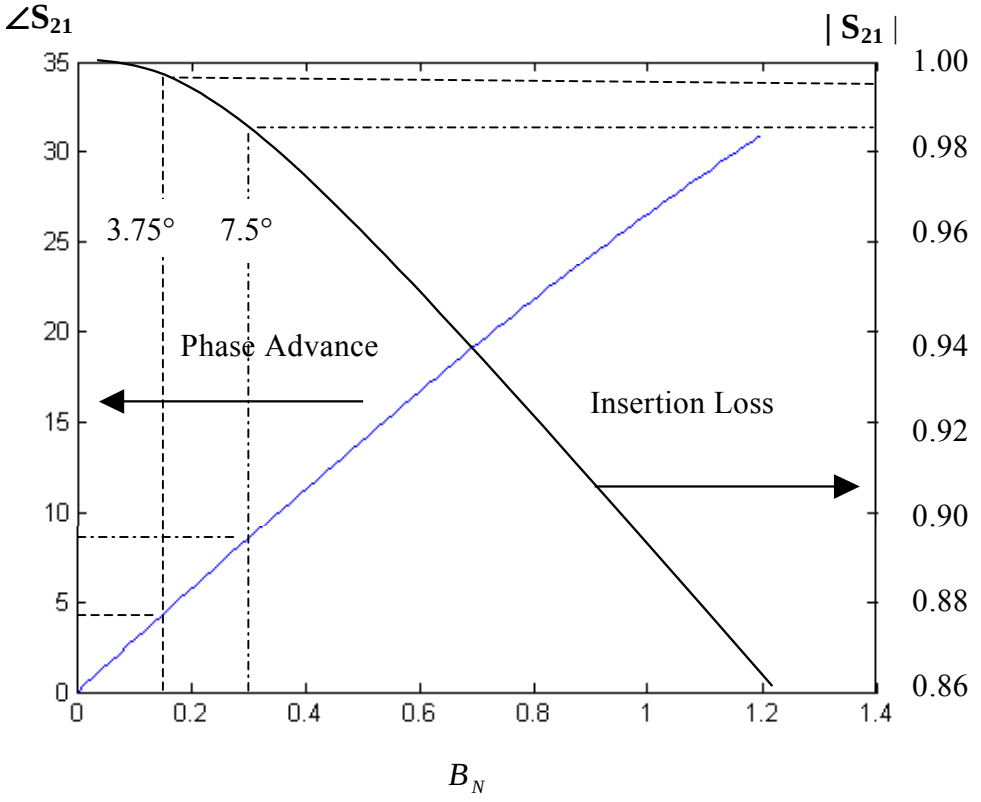


Fig 5.8 Graphs of phase advance and insertion loss vs. B_N for the circuit of Fig 5.7

5.3.3 Analysis of the Circuit of Fig 5.5 (b)

Note that Fig 5.5 (b) represents state 3 discussed in Sec. 5.2.

The normalized ABCD matrix is given by,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & jX_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ jB_N & 1 \end{vmatrix} = \begin{vmatrix} 1-X_N B_N & jX_N \\ jB_N & 1 \end{vmatrix} \tag{5.17}$$

where

$$X_N = X / Z_0 = L\omega / Z_0 \tag{5.18}$$

$$B_N = BZ_0 = C\omega Z_0 \tag{5.19}$$

The scattering matrix element, S_{21}, in terms of the normalized ABCD matrix is given by,

$$S_{21} = \frac{2}{A+B+C+D} = \frac{2}{2-X_N B_N + j(X_N + B_N)} \tag{5.20}$$

The transmission phase is given by,

$$\angle S_{21} = \tan^{-1}\left[-\frac{X_N + B_N}{2 - X_N B_N} \right] \tag{5.21}$$

The insertion loss is given by,

$$|S_{21}| = \sqrt{\frac{4}{(2-X_N B_N)^2 + (X_N + B_N)^2}} \tag{5.22}$$

$$= \sqrt{\frac{4}{4 + X_N^2 B_N^2 - 4X_N B_N + X_N^2 + B_N^2 + 2X_N B_N}}$$

$$= \sqrt{\frac{4}{4 + X_N^2 B_N^2 - 2X_N B_N + X_N^2 + B_N^2}}$$

when,

$$X_N = \frac{B_N}{1 + B_N^2} \tag{5.23}$$

$$|S_{21}|_{\min} = \sqrt{\frac{4}{4+\frac{B_N^4}{1+B_N^2}}} \tag{5.24}$$

It can be seen that in the limit when $B_N << 1$, $\frac{B_N^4}{1+B_N^2} \approx 0$ (5.25)

The minimum insertion loss, $|S_{21}|_{\min} \approx 1 \approx 0$ dB (5.26)

Fig 5.9 shows the graphs of X_N versus B_N for constant values of phase-delay and insertion loss.

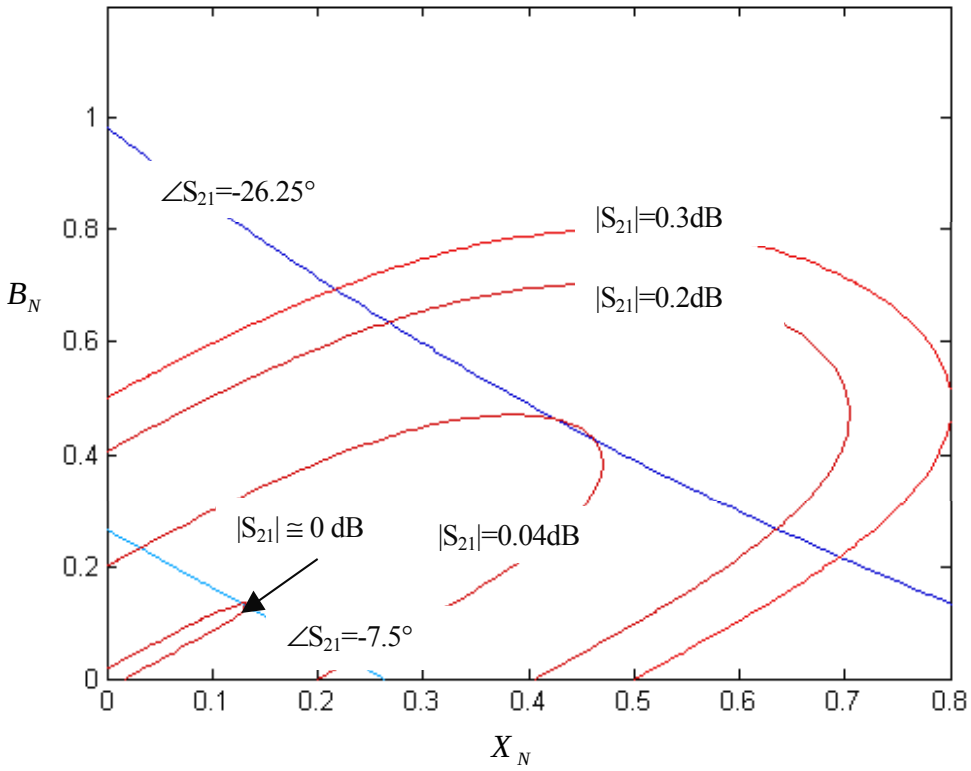


Fig 5.9 Graphs of X_N and B_N for constant values of phase delay and insertion loss for the circuit of Fig 5.5 (b)

5.4 Analysis of L-Sections for Lossy Components

It can be seen that the phase shift variations versus frequency is quite flat over a wide bandwidth. In real circumstances, the components usually have parasitic resistances and tend to be lossy as shown in Fig 5.10. The analysis of the lossy cases below shows that the phase shift and insertion loss behavior is quite similar to that of the lossless cases.

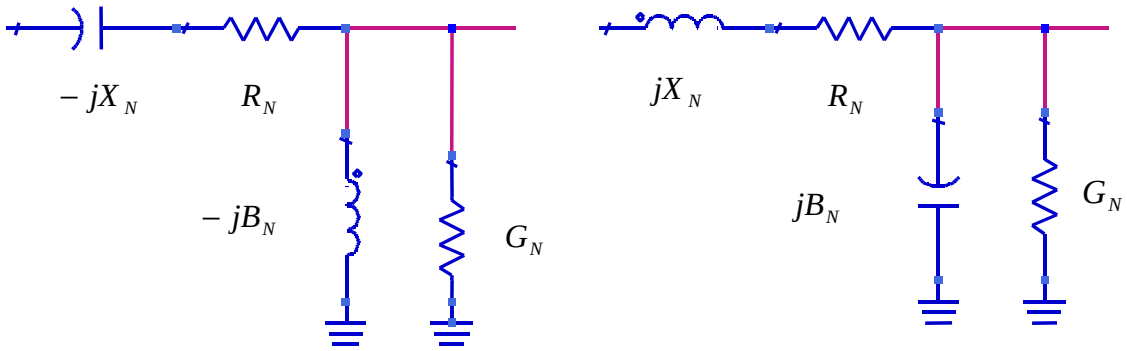


Fig 5.10 LC filter with lossy components

The normalized ABCD matrix for the elements of Fig 5.13 a (high–pass state) is given by:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & Z_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ Y_N & 1 \end{vmatrix} \qquad (5.27)$$

where

$$Z = R - j/\omega C \qquad (5.28)$$

$$Y = G - j/\omega L \qquad (5.29)$$

$$Z_N = Z/Z_0 = R/Z_0 - j/\omega C Z_0 = R_N - jX_N \qquad (5.30)$$

$$Y_N = YZ_0 = GZ_0 - Z_0 j/\omega L = G_N - jB_N \qquad (5.31)$$

Thus

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & R_N - jX_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ G_N - jB_N & 1 \end{vmatrix} \tag{5.32}$$

$$= \begin{vmatrix} 1+(R_N - jX_N)(G_N - jB_N) & R_N - jX_N \\ G_N - jB_N & 1 \end{vmatrix}$$

The transmission term of the scattering matrix S_{21} of the normalized ABCD matrix is given by

$$S_{21} = \frac{2}{A+B+C+D} \tag{5.33}$$

$$= \frac{2}{2+(R_N - jX_N)(G_N - jB_N)+R_N - jX_N + G_N - jB_N}$$

The transmission phase is given by

$$\angle S_{21} = \tan^{-1}\left[\frac{B_N(R_N+1)+X_N(G_N+1)}{2-X_N B_N + R_N G_N + R_N + G_N}\right] \tag{5.34}$$

when $R_N, G_N << 1$,

$$\angle S_{21} \approx \tan^{-1}\left[\frac{B_N + X_N}{2 - X_N B_N}\right] \tag{5.35}$$

Fig 5.11 shows the special case of the high pass state in Fig 5.10 (a).

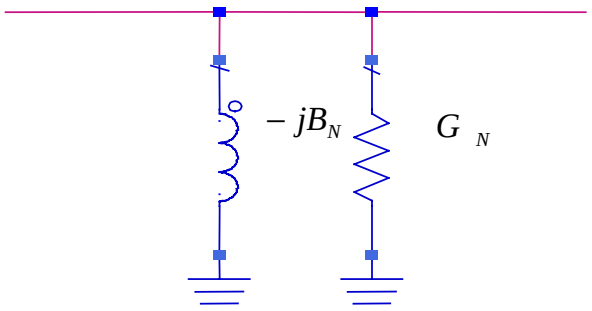


Fig 5.11 Special case of the high pass state in Fig 5.10 (a)

The normalized ABCD matrix for the elements of Fig 5.11 is given by:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & 0 \\ Y_N & 1 \end{vmatrix} \tag{5.36}$$

where,

$$Y = G - j/\omega L \tag{5.37}$$

$$Y_N = YZ_0 = GZ_0 - Z_0 j/\omega L = G_N - jB_N \tag{5.38}$$

Thus,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ G_N - jB_N & 1 \end{vmatrix} \tag{5.39}$$

The transmission term of the scattering matrix S_{21} of the normalized ABCD matrix is given by,

$$S_{21} = \frac{2}{A + B + C + D} \tag{5.40}$$

$$= \frac{2}{2 + G_N - jB_N}$$

The transmission phase is given by,

$$\angle S_{21} = \tan^{-1}\left[\frac{B_N}{2 + G_N}\right] \tag{5.41}$$

Similarly, when $G_N << 1$,

$$\angle S_{21} \approx \tan^{-1}\left[\frac{B_N}{2}\right] \tag{5.42}$$

The normalized ABCD matrix for the elements of Fig 5.10 (b) (low–pass state) is given by:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix}_N = \begin{vmatrix} 1 & Z_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ Y_N & 1 \end{vmatrix} \tag{5.43}$$

where,

$$Z = R + j\omega L \tag{5.44}$$

$$Y = G + j\omega C \tag{5.45}$$

$$Z_N = Z / Z_0 = R / Z_0 + j\omega L / Z_0 = R_N + jX_N \tag{5.46}$$

$$Y_N = YZ_0 = GZ_0 + Z_0 j\omega C = G_N + jB_N \tag{5.47}$$

Thus,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & R_N + jX_N \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ G_N + jB_N & 1 \end{vmatrix} \tag{5.48}$$

$$= \begin{vmatrix} 1+(R_N + jX_N)(G_N + jB_N) & R_N + jX_N \\ G_N + jB_N & 1 \end{vmatrix}$$

The transmission term of the scattering matrix S_{21} of the normalized ABCD matrix is given by,

$$S_{21} = \frac{2}{A + B + C + D} \tag{5.49}$$

$$= \frac{2}{2 + (R_N + jX_N)(G_N + jB_N) + R_N + jX_N + G_N + jB_N}$$

The transmission phase is given by

$$\angle S_{21} = \tan^{-1}\left[-\frac{B_N (R_N + 1) + X_N (G_N + 1)}{2 - X_N B_N + R_N G_N + R_N + G_N} \right] \tag{5.50}$$

when $R_N, G_N << 1$,

$$\angle S_{21} \approx \tan^{-1}\left[-\frac{B_N + X_N}{2 - X_N B_N}\right] \qquad (5.51)$$

It can be seen that when the normalized impedance and resistance $R_N, G_N << 1$, the phase shift has the same expression as the lossless case. Thus when the loss associated with the components is small, we neglect the loss and use the values obtained from the analysis for lossless cases as initial values for optimization of the values of lumped LC elements.

5.5 Characterization and Modeling of GaAs FET Switches

As shown in the earlier sections, the on resistance and off capacitance of the FET switches are required for designing the phase shifter. Hence we need to extract their values from the device models provided by the foundry.

UMS foundry HP25 process provides models of two kinds of switch devices: series switch and parallel switch. Fig 5.12 shows the different configuration for series and parallel switches. The switch models are linear models which are measured S-parameter data under different bias conditions.

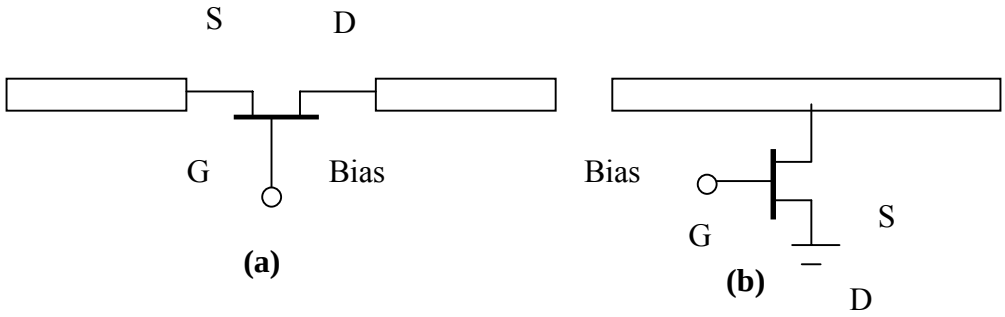


Fig 5.12 FET switches in (a) series and (b) shunt-mounted configurations

In the process of designing a phase shifter, a simple model of the FET switch should be extracted from the S-parameter of the FET model given by the MMIC foundry. This simplified model is only used to visualize the non-ideal behavior of FETs as switches. In the actual simulations, the accurate model will be used so as to obtain realistic results. Under approximation, a switching FET in the OFF state is equivalent to a capacitor from drain-to-source while a FET in the ON state is equivalent to a resistor from drain-to-source. To find the exact "C_{ds}" or "r" to represent the corresponding FET model, a simulation is set up to compare the S11 parameters of the exact and approximate model. Cds and r are adjusted such that their S11 match that of the FET when it is off and on. The schematic to achieve this is shown in Fig 5.13 and Fig 5.14.

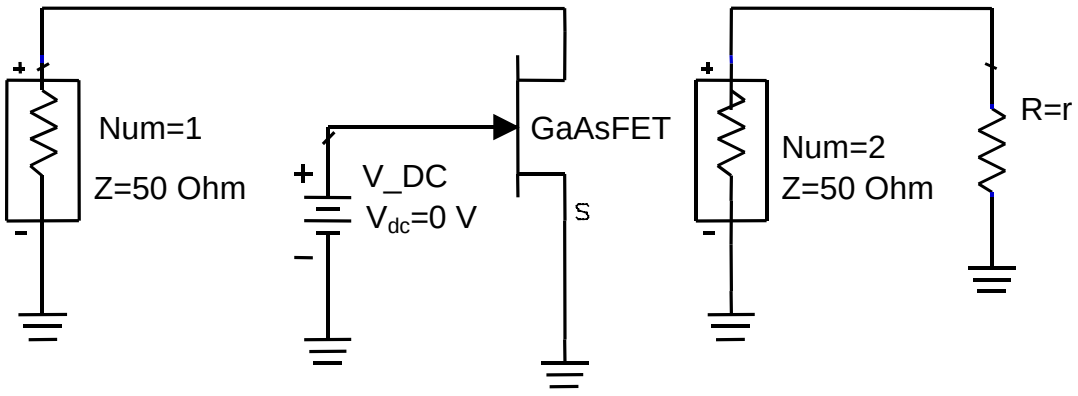


Fig 5.13 Circuit to extract on-state equivalent drain-source resistance

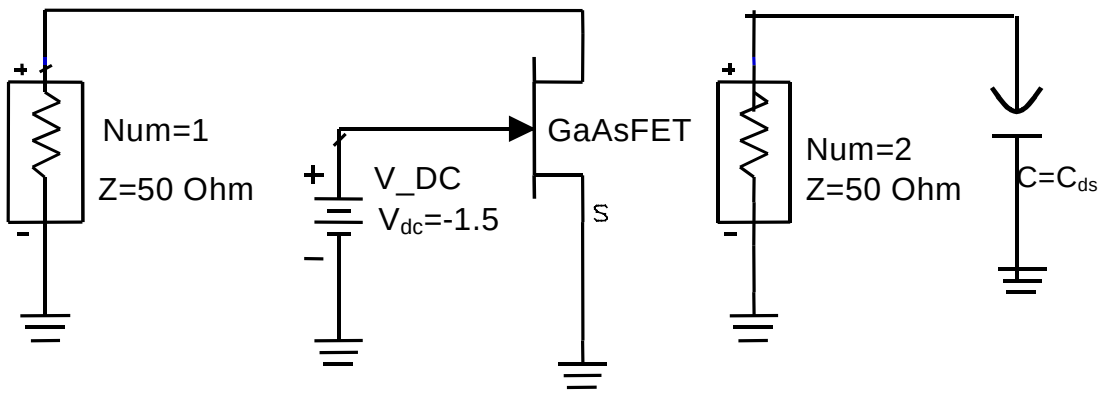


Fig 5.14 Circuit to extract off-state equivalent drain-source capacitance

Unlike hybrid-MIC implementation where the geometry of the FET is fixed, MMIC allows much more flexibility as the layout is scalable. The main factors affecting the model definition for GaAs MMIC FETs are:

- Channel geometry
- Gate length
- Metallization scheme
- Gate recess structure
- Channel doping density
- Pinch-off voltage

As shown in Fig 5.1, there are four switches in each bit. And the off-state capacitances C_{ds}, are utilized as the components of the network. Thus there are totally 7 design variables in the equivalent circuit: L_1, C_{ds1} (FET1), C_1, C_{ds2} (FET2), L_2, C_{ds3} (FET3) and C_{ds4} (FET4). To simplify the design, we fixed the perimeters of FET1, FET2 and FET3 but leave the perimeter of FET4 open for optimization, because C_{ds4} is the only component in the parallel stub for state 3: $B_N = C_{ds}\omega Z_0$.

We use three 4 fingers (N=4), 30 μm finger width (Wu=30 μm) MESFET switches for FET1, FET2 and FET3. The values of the on-state resistance (r) and off-state capacitance (C_{ds}) that reasonably approximate the FET's behavior in two states were found to be:

Parallel connection (FET3):

Approximated_r = 9.57 Ω

Approximated_C_{ds} = 0.1 pF

Series connection (FET1, FET2):

Approximated_r = 8.13 Ω

Approximated_C_{ds} = 0.1 pF

To decide the perimeter of FET4, we need to

1. Ignore the on-resistances and off-capacitances of FET1, FET2 and FET3 and calculate the values of L_1, L_2, C_1 and C_{ds4} from the formulas given in section 5.3.
2. Choose the perimeter of FET4 having the same off-capacitance value, C_{ds4}. Thus it is necessary to get the simple models for a set of MESFET switches with different geometry.
3. Calculate the real values of L_1, L_2 and C_1 taking account of the switch parasitics.
4. Use the perimeter of FET4 got from step 2 and the values of L_1,L_2 and C_1 got from step 3 as the initial value. Optimize the whole circuit and obtain the final design.

We will describe steps 1, 3 and 4 in detail in the next section. For Step 2, the model extraction method given in this section is very crucial.

5.6 Design of the Proposed 3 Phase-State Circuit

The design equations for the switch filter have been derived in sections 5.3 and 5.4. The formulas describe the performance of LC switched filter and are used to calculate the design values for the network components. The model of the switching MESFET extracted in Section 5.5 is used to simplify the circuit and choose the right perimeter for switches. In Section 5.6.1 we will first introduce how to get the theoretical design values ignoring the switch parasitics. Then Section 5.6.2 will specify the steps of design optimization.

5.6.1 Design Ignoring Switch Parasitics

It can be seen from the previous sections that the 3 phase–state phase shifter switches between 3 phase states as shown in Figs 5.2 – 5.4. The switch states and output phases are shown in Table 5.1. In this section, we ignore the switch parasitics, on-resistances r and off-capacitances C_{ds}. We will use the equivalent circuits shown in Figs 5.2 (b), 5.3 (b) and 5.4 (b) to calculate the value of susceptance and reactance of each state. The simulation results show a wide bandwidth phase performance.

As shown in Table 5.1, for the 56.25°/33.75° bit, the circuit was designed to give three output phase states: 30°, 7.5° and –26.25° that give two differential phase shifts of 56.25° and 33.75°. State 1 and state 2 are high pass paths which have phase advance. Since in State 2 the inductor value is fixed for fixed phase advance, we can get the value of L_2 by substituting 7.5° phase advance into Equation 5.14. We get $B_N = Z_0 / L_2\omega = 0.27$ and L_2=3.28 nH (at the center frequency of 9 GHz). And from Fig 5.8 we get the insertion loss

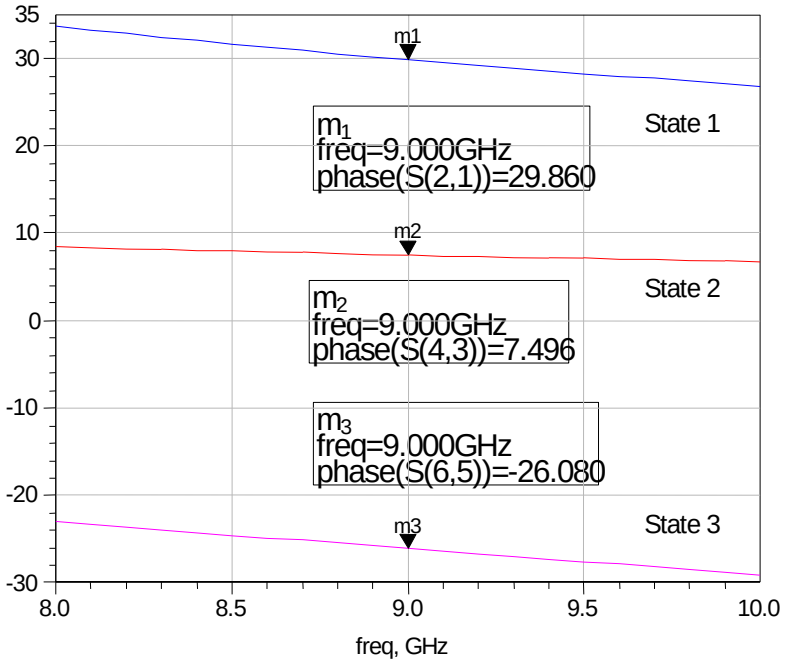
$|S_{21}| \cong 0.99$ (0.08 dB) which is quite acceptable. Given the value of L_2 and $\angle S_{21} = 30°$, C_1 can be decided as 0.46 pF ($X_N = 1/Z_0 C_{ds}\omega = 0.77$) using Equation 5.5 and the insertion loss corresponding to state 1 is about 0.97 (0.26dB). State 3 is low path state, which has phase delay. Substituting $\angle S_{21} = -26.25°$ into Equation 5.21 yields the design value of L_1, and C_{ds}. Since there are groups of L_1 and C_{ds} values that we can choose from, the values are decided by considering practical values of C_{ds} of the switches and minimizing the insertion loss. As seen from Fig 5.9, the minimum insertion loss is the insertion loss contour $|S_{21}|$= 0.04 dB which is tangential to the curve of $\angle S_{21}$= -26.25°. The X_N and B_N of this point are 0.44 and 0.45 corresponding to L_1 of 0.39 nH and C_{ds} of 1.6 pF which is a feasible value of the off capacitance of the switch. Table 5.2 shows the value of insertion loss, X_N and B_N and the values of corresponding L and C of each state.

Table 5.2 Insertion loss, values of X_N and B_N with corresponding L and C for the $0^0/33.75^0/56.25^0$ circuit block

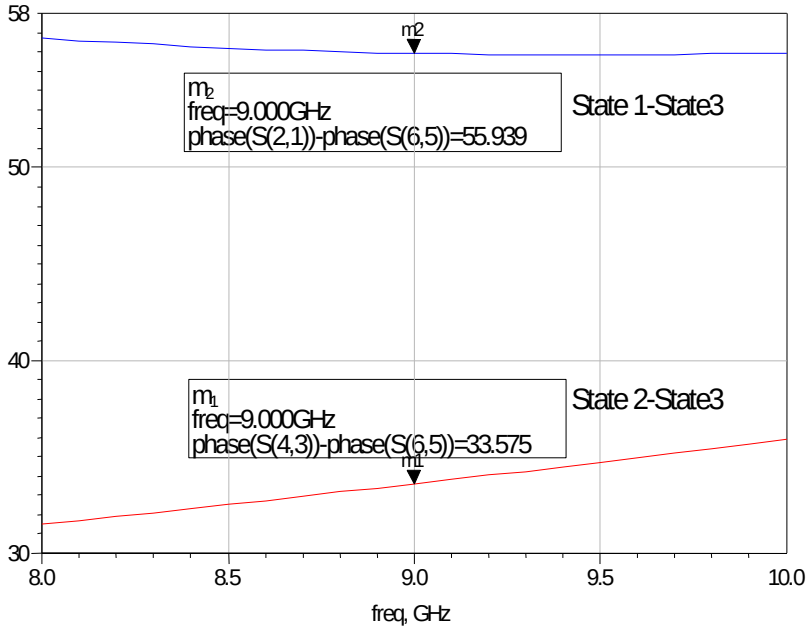
	Insertion loss	X_N	B_N
State 1	0.08 dB	$X_N = 1/Z_0 C_1 \omega = 0.77$	
		$C_1 = 0.46$ pF	
State 2	0.26 dB		$B_N = Z_0 / L_2 \omega = 0.27$
			$L_2 = 3.28$ nH
State 3	0.04 dB	$X_N = L_1 \omega / Z_0 = 0.44$	$B_N = C_{ds} \omega Z_0 = 0.45$
		$L_1 = 0.39$ nH	$C_{ds} = 1.6$ pF

By observing the variations of phase-shift versus X_N and B_N in Fig 5.6, Fig 5.8 and Fig 5.9, we can now find out that why this kind of phase shifter is able to work at wide bandwidth. Once the points of X_N and B_N are decided, in high-pass state (state 1), the series reactance ($X_N = 1/C\omega Z_0$) and the shunt susceptance ($B_N = Z_0 / L\omega$) both decrease with increasing frequency. The point of X_N and B_N moves towards the lower-left corner in Fig 5.6. On the other hand, in low pass state (state 3), the series reactance ($X_N = L\omega / Z_0$) and the shunt susceptance ($B_N = C\omega Z_0$) both increase proportional to frequency increases. The point of X_N and B_N moves towards the upper right in Fig 5.9.

For state 2, which has a phase advance of 7.5°, the phase advance varies with frequency in the similar way as that of the high-pass LC filter shown in Fig 5.5 (a). The net effect is that the phase shift tends to stay matched as frequency is increased, and the phase delay increase in the low-phase state is compensated for by phase advance lost in the high-pass state. Fig5.15 shows the simulation results of the $0^0 / 33.75^0 / 56.25^0$ bit LC phase shifter with three states as shown in Figures 5.5 and 5.7. The element values are given in Table 5.2. Fig 5.15 (a) shows the output phases of the three states and Fig 5.15 (b) shows the differential phases. It can be seen that although the output phase of each state decreases as frequency increases, the differential phase shifts are relatively flat.



(a)



(b)

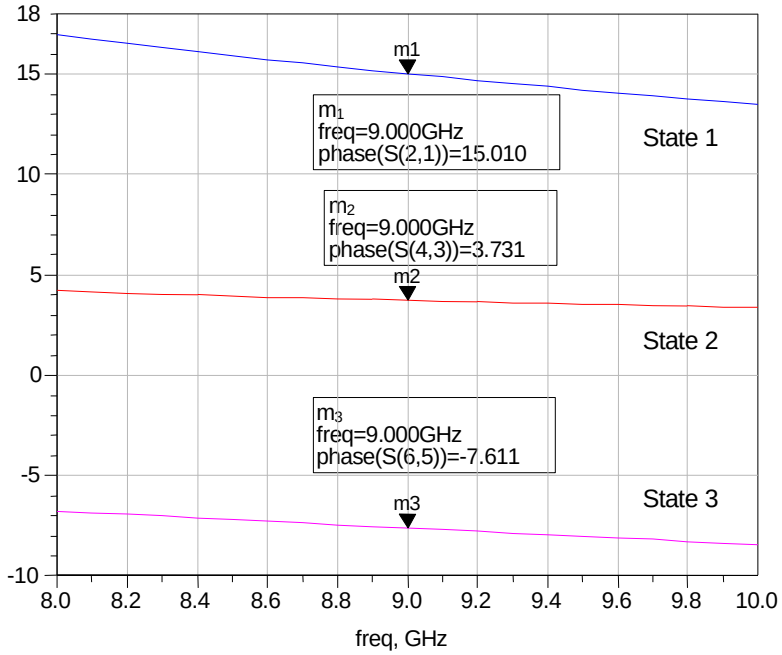
Fig 5.15 (a) Output phases (b) Differential phases of the 0^0 / 33.75^0 / 56.25^0 bit

Similarly we can get the design of the $0^0/11.25^0/22.5^0$ block with the help of Figs 5.6, 5.8 and 5.9. Table 5.3 shows the values of insertion loss, X_N and B_N and the values of corresponding L and C of each state for $0^0/11.25^0/22.5^0$ circuit block.

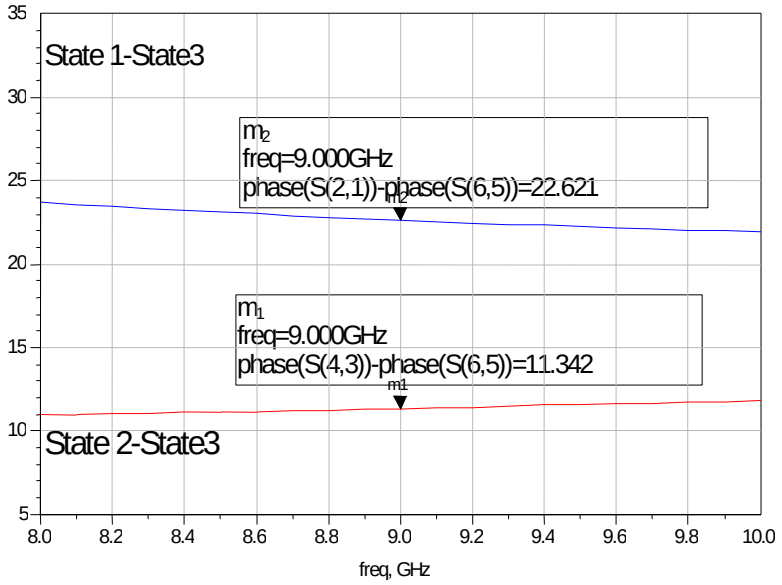
Table 5.3 Insertion loss, values of X_N and B_N with corresponding L and C for the $0^0/11.25^0/22.5^0$ circuit block

	Insertion loss	X_N	B_N
State 1	≅0.0 dB	$X_N = 1/Z_0C_1\omega = 0.37$	
		$C_1 = 0.87$ pF	
State 2	0.04 dB		$B_N = Z_0/L_2\omega = 0.13$
			$L_2 = 6.78$ nH
State 3	≅0.0 dB	$X_N = L_1\omega/Z_0 = 0.12$	$B_N = C_{ds}\omega Z_0 = 0.13$
		$L_1 = 0.106$ nH	$C_{ds} = 0.46$ pF

Fig5.16 shows the simulation results of the $0^0/11.25^0/22.5^0$ bit LC phase shifter with three states as shown in Figures 5.5 and 5.7. The element values are given in Table 5.3. Fig 5.16 (a) shows the output phases of the three states and Fig 5.16 (b) shows the differential phases.



(a)



(b)

Fig 5.16 (a) Output phases (b) Differential phases of the 0^0 / 11.25^0 / 22.5^0 bit

In total, the frequency dependence of all the differential phase shift settings given in Table 5.1 is shown in Fig 5.17.

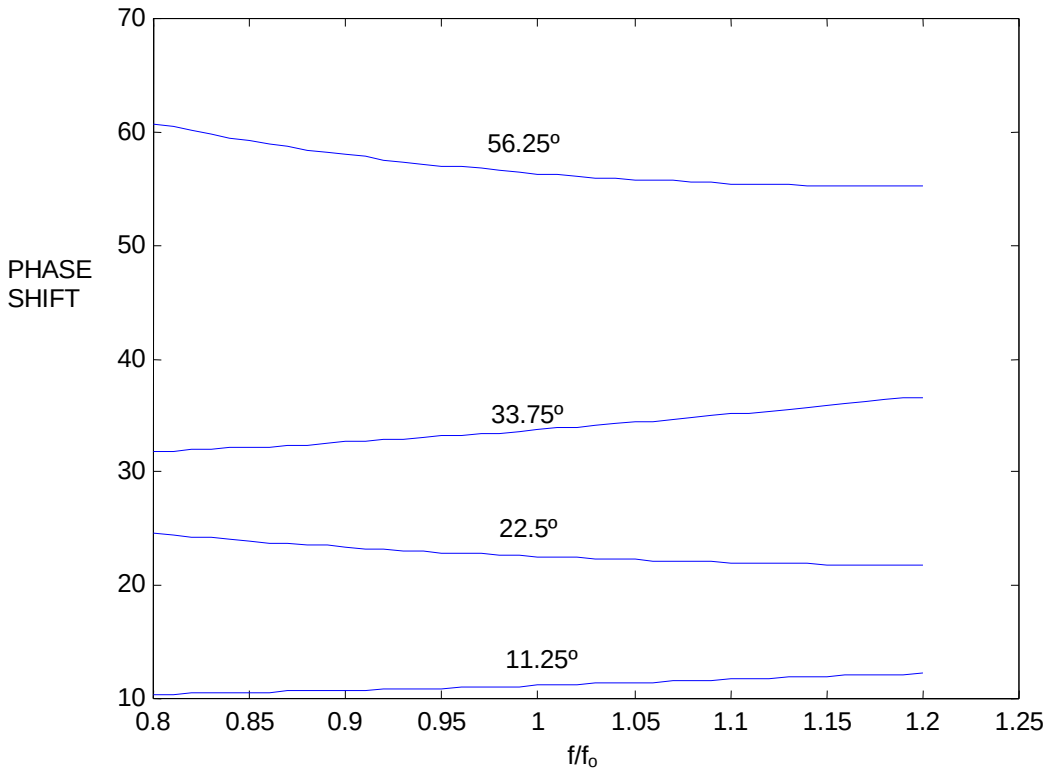


Fig 5.17 Phase shift vs. frequency f/f_o

5.6.2 Circuit Optimization

In Section 5.6.1, the design details of the switched network without the switch parasitics are given. If we apply the R-C model extracted in Section 5.5, the switches in the circuit should be replaced by a small resistor r in the on-state and a capacitor C_{ds} in the off-state. As seen from Section 5.4, when the loss is relatively small compared to 50 Ω, we can ignore the loss and use the formulas for lossless case. As a matter of fact, this statement has been verified by comparing the LC values obtained using the lossy formulas with the LC values listed in Tables 5.3 and 5.4. They are almost the same. But the difference here from the previous section is that since the off-capacitance will be absorbed into the

switched network, we need to distract the values of C_{ds} of FET1, FET2 and FET3 from the values of L_1, L_2 and C_1 listed in Tables 5.2 and 5.3.

Then the theoretical values of L_1, L_2, C_1 and the perimeters of FET4 are used as the initial value in the simulation, which is implemented in MDS. Optimization is carried out to optimize the performance. The optimization steps are given as following:

Step 1. Set the optimization variables in Fig 5.1: L_1, L_2, and C_1. Real transistor models are used for the four switches. The finger number N and finger width Wu of FET4 must also be optimized at the same time. The geometry of the other three switches are set fixed.

Step 2. Use the theoretical values for L_1, L_2 and C_1 as the initial value for optimization.

Step 3. Given the desired value of C_{ds}, choose the appropriate transistor perimeter of FET4 as the initial value for optimization.

Step 4. Set the optimization goals which are the minimum RMS (root-mean-square) phase error and insertion loss for each phase state across the band of 8GHz-10GHz. Equations 5.52 and 5.53 shows the objective function:

$$RMS\_PhaseError = \sqrt{\frac{\sum_{i=1}^{N}(PhaseError(freq(i)))^2}{N}} \le 2^0 \tag{5.52}$$

$$Insertion\_Loss = mag(dB(|S21(i)|)) \le 2dB \qquad i = 1,2,..N \tag{5.53}$$

where N (N=5) is the number of frequency points selected across the band of 8GHz-10GHz to do the optimization.

Table 5.4 shows theoretical design values as well as optimized values of circuit elements for 0^0 / 33.75^0 / 56.25^0 circuit block for a frequency range of 8 GHz to 10 GHz. It can be seen that, the theoretical values are close to optimized values.

Table 5.4 Theoretical and optimized values for the $0^0/33.75^0/56.25^0$ circuit block

Component Value	Phase States	State 1 30°	State 2 7.5°	State 3 -26.25°
L_1 nH	Theoretical Value			0.34
	Optimized Value			0.4
C_1 pF	Theoretical Value	0.36		
	Optimized Value	0.4		
L_2 nH	Theoretical Value	1.6	1.6	
	Optimized Value	1.5	1.5	
C_{ds} pF	Theoretical Value			1.6
	Optimized Value			1.4

Table 5.5 shows theoretical design values as well as optimized values of the circuit elements for the $0^0/11.25^0/22.5^0$ circuit block for a frequency range of 8 GHz to 10 GHz. It can be seen that, the theoretical values are close to optimized values.

Table 5.5 Theoretical and optimized values for the $0^0/11.25^0/22.5^0$ circuit block

Component Value	Phase States	State 1 15°	State 2 3.75°	State 3 -7.5°
L_1 nH	Theoretical Value			0.1
	Optimized Value			0.15
C_1 pF	Theoretical Value	0.77		
	Optimized Value	0.78		
L_2 nH	Theoretical Value	2.15	2.15	
	Optimized Value	2	2	
C_{ds} pF	Theoretical Value			0.46
	Optimized Value			0.32

5.7 MMIC Implementation of the Design

The validity of the design and the performance of the phase shifter are heavily dependent on the technology used for the fabricating the circuit and the CAD software used for circuit design and simulation. The software should perform a comprehensive analysis of the design that approximates the real performance very closely. At microwave frequencies it is very crucial. The performance of the phase shifter is also very closely linked to the MMIC fabrication process, as the foundry rules and capabilities are different for different vendors. UMS PH25 process is based on a 0.25 μm gate pseudomorphic high electron mobility transistor (0.25 μm PHEMT) technology. The major features of this process are PHEMT MBE active layer with embedded etch stop to improve Idss on-wafer spread and

0.25 μm T-shaped aluminium gate, featuring low resistance and excellent reliability, air-bridges and via-holes. Hewlett Packard's Microwave Design System (MDS) does not support multiplayer substrates. As a result the design that is done in schematics does not check for actual layout viability or correct inter layer transitions. The software thus, is unable to calculate the coupling effect that arises out of inter-layer transmission line crossings. It is therefore up to the designer to take into account the above factors by ensuring correct correspondence between the process layers and the components that they implement. There is therefore a need to understand the process layers to ensure a more optimum design. Layout feasibility was ensured by physically laying out the circuit to ensure proper inter-layer connectivity and prevent overlapping components.

The layout and geometry of the MESFET devices play an important role of the entire circuit because much of the chip surface is taken up by the MESFET switches. Table 5.6 gives the geometry of the MESFETs in 0^0 / 11.25^0 / 22.5^0 and 0^0 / 33.75^0 / 56.25^0 bits:

Table 5.6 MESFETs Geometry

		FET1	FET2	FET3	FET4
0^0 / 11.25^0 / 22.5^0 bit	Number of Fingers (N)	4	4	4	12
	Finger Width (Wu μm)	30	30	30	30
0^0 / 33.75^0 / 56.25^0 bit	Number of Fingers (N)	4	4	4	28
	Finger Width (Wu μm)	30	30	30	60

In the layout, the MESFETs were included together with the gate biasing circuitry. The FETs are all placed in the same direction according to the foundry's design rule that FET must be placed parallel to the x-axis. The biasing circuitries for sources are given in the layout. Since this circuit is to be cascaded with the other phase shifter bits only the RF part of the circuit is implemented. The biasing control lines can easily be implemented at later stage. In the layout, the transmission lines are spaced at least 20 μm apart to reduce coupling if they are parallel.

Chapter 6

Results and Discussions

6.1 Introduction

The main advantage of the novel 3 phase-state phase shifter compared to Nakahara's design is that it has smaller area as transmission lines and couplers are not used. It requires the same number (4) of FETs as Nakahara's Type 1 and Type 2 circuits. It is noted however that Nakahara's loaded line 3 phase-state phase shifter requires fewer (3) FETs. Compared to 2 phase-state designs (e.g. Ref. [23]), the design reported here requires fewer inductors. The performance is comparable to conventional designs. In this chapter, the simulation results of the optimized 3 phase-state phase shifters ($0^0/11.25^0/22.5^0$ and $0^0/33.75^0/56.25^0$) designed in Chapter 5 will be presented. The results are compared with the result for the $0^0/11.25^0/22.5^0$ 3 phase-state loaded-line type phase shifter reported by Nakahara. Next, a $0^0/11.25^0/22.5^0$ 3 phase-state type 1 Nakahara circuit is designed for comparison with the $0^0/11.25^0/22.5^0$ designed by that author as no results for the type 1 circuit is reported by Nakahara. Simulation results for the cascaded $0^0/11.25^0/22.5^0$ and $0^0/33.75^0/56.25^0$ 3 phase-state phase shifters is then presented. From Fig 4.8 in Chapter 4, it may be noted that such a cascaded section replaces three 2 phase-state phase shifters, $0^0/45^0$, $0^0/22.5^0$ and $0^0/11.25^0$. The latter is designed following the scheme of ref.23 and the performance is compared with that of cascaded $0^0/11.25^0/22.5^0$ and $0^0/33.75^0/56.25^0$ 3 phase-state phase shifters. Finally a comparison of various designs is presented.

6.2 Simulation Results for Optimized 3 Phase-State Phase Shifter Designed in Chapter 5

The predicted phase shifts of the two circuits, $0^0/11.25^0/22.5^0$ and $0^0/33.75^0/56.25^0$, are shown in Fig 6.1 and Fig 6.4 respectively. The accuracy of the phase shift over the 8-10 GHz band is very good, and phase error is well balanced over a 10% bandwidth. The insertion losses are plotted in Fig 6.2 and Fig 6.5 from 8 GHz to 10 GHz. The insertion losses for both circuits are between 1.5 dB and 3 dB, with a maximum loss variation of 3 dB. Return losses are plotted in Fig 6.3 and Fig 6.6 and are generally better than 10 dB.

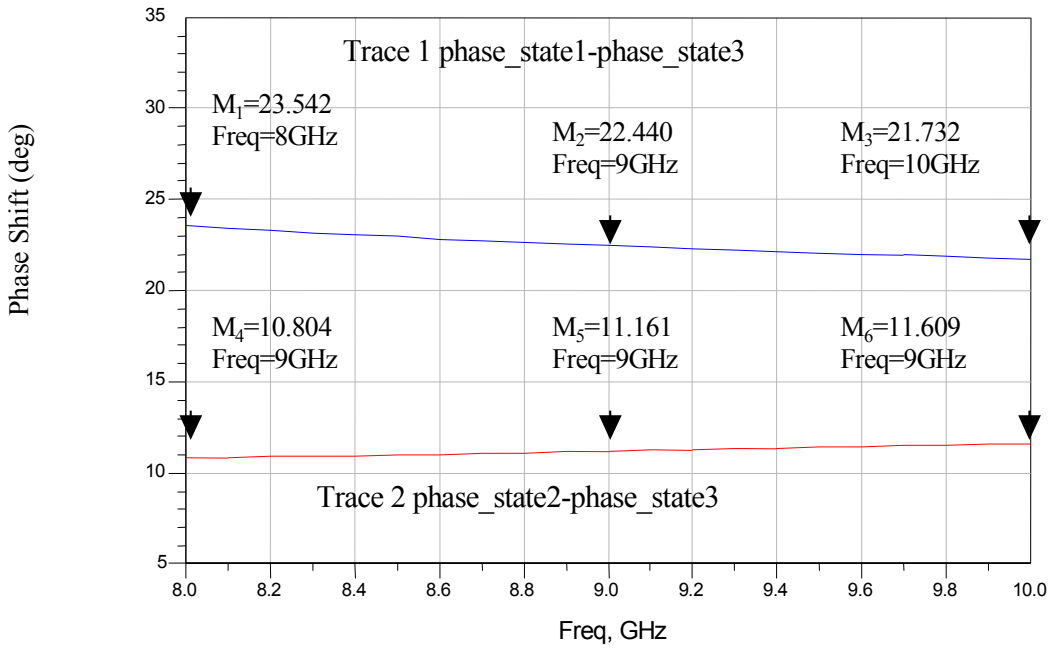


Fig 6.1 Phase response of 11.25°/22.5° bit

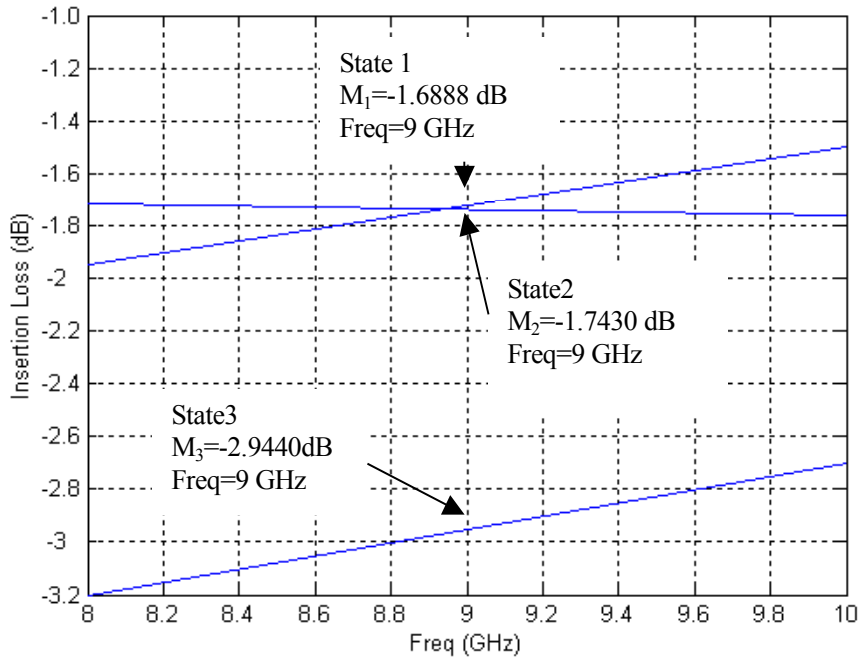


Fig 6.2 Insertion loss for three states of 11.25°/22.5° bit

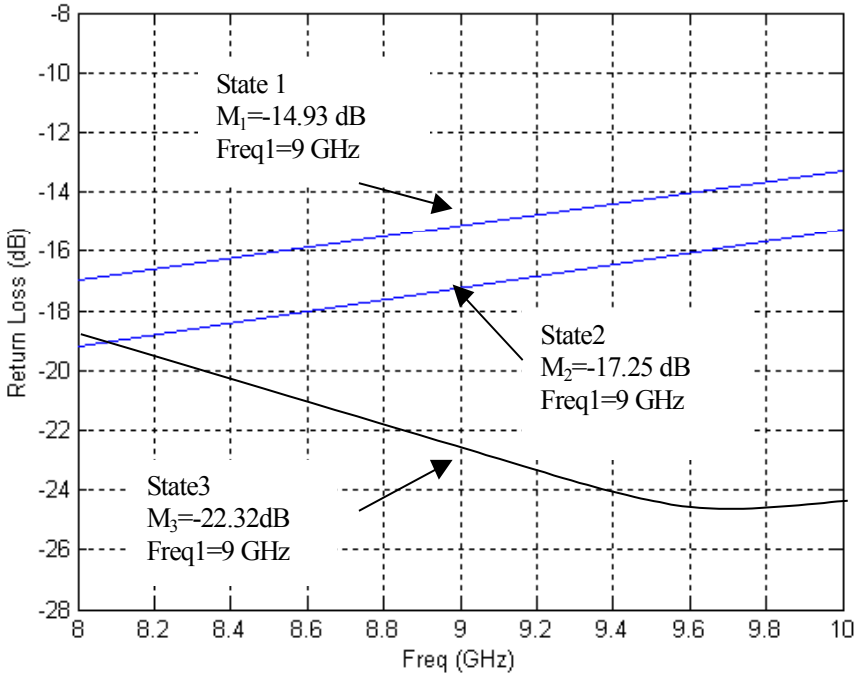


Fig 6.3 Return loss for three states of 11.25°/22.5° bit

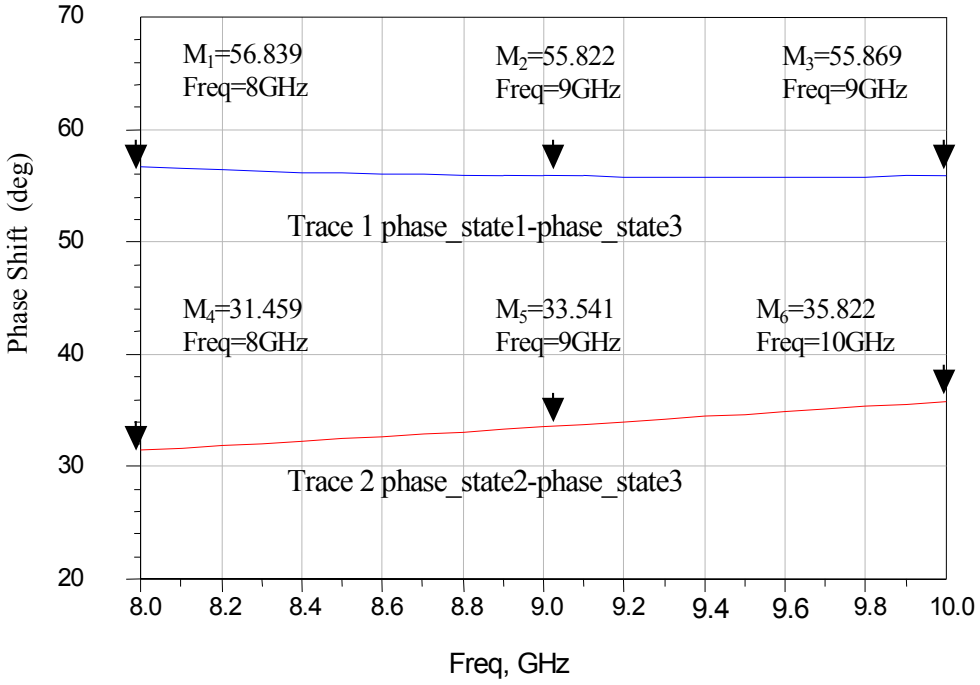


Fig 6.4 Phase response of 33.75°/56.25° bit

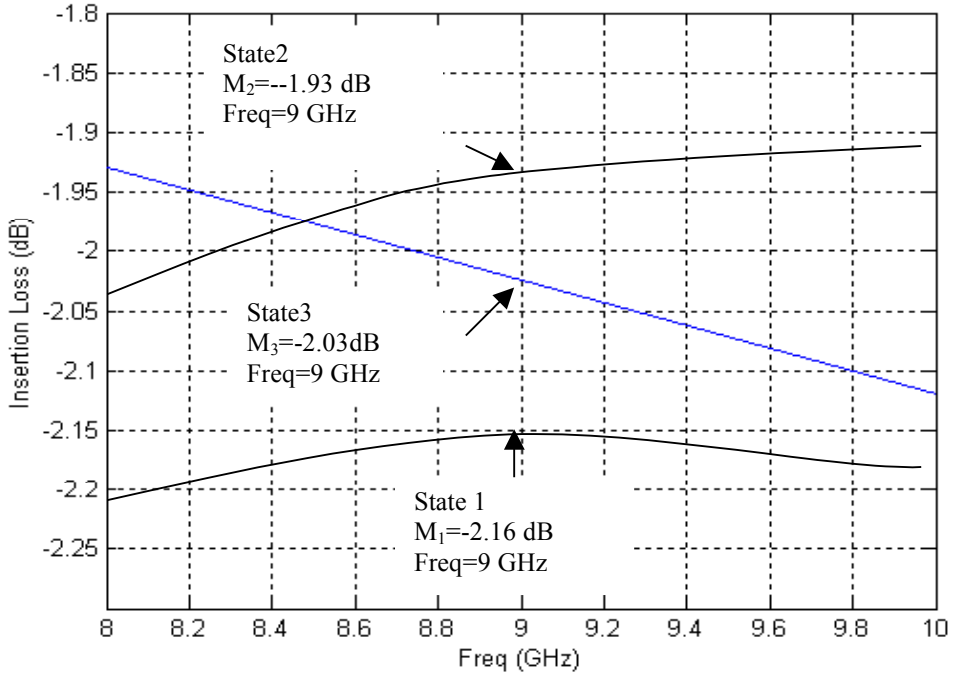


Fig 6.5 Insertion loss of 33.75°/56.25° bit

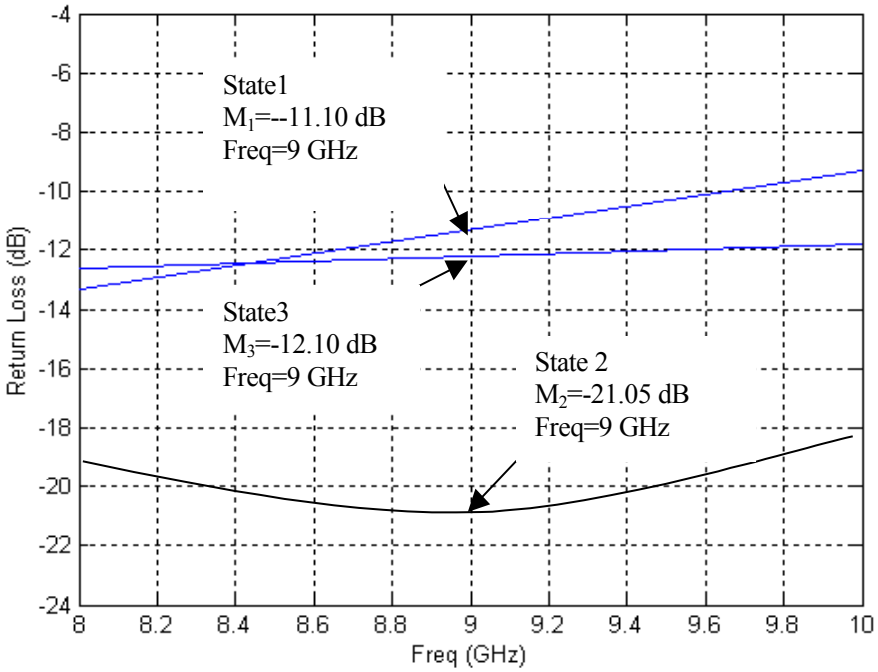


Fig 6.6 Return loss of 33.75°/56.25° bit

For comparison, the measured phase performance reported by K. Nakahara in 1993 [14] of the novel loaded-line type 3 phase-state phase shifter ($0^0/11.25^0/22.5^0$) is shown in Fig 6.7 (regenerated by MATLAB according to the data reported in the paper). The upper plot represents the response for the differential phase shift of 22.5^0 while the lower plot represents the response for the differential phase shift of 11.25^0.

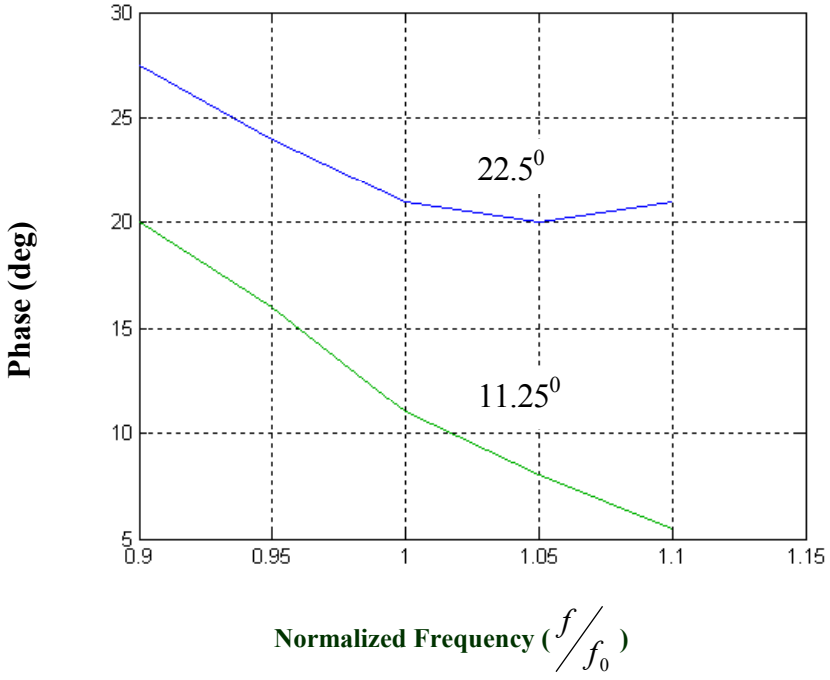


Fig 6.7 Measured phase performance of the novel Nakahara's loaded-line-type 3 phase-state phase shifter (upper plot for 22.5^0 and the lower plot for 11.25^0)

Comparing the performance of the loaded-line type 3 phase-state phase shifter in Fig 6.7 with what we presented in Fig 6.1, it can be seen that the phase performance of our LC switched filter 3 phase-state phase shifter is quite flat over the 8-10 GHz band (about 10 % bandwidth). The Max RMS phase error occurs at the 22.5°, which is 1.5°. The phase shift output of 11.25° is almost flat over a 10% bandwidth. In Fig 6.7, both 22.5° and 11.25° states have a RMS error about 5°. It is not a surprise that, as we explained in Section 5.2, wide band phase shift can be achieved using LC network phase shifter because the phase compensation between high pass and low pass states when frequency varies.

6.3 Comparison with Nakahara's 3 Phase-State Type 1 Phase Shifter

Nakahara does not give the phase performance of his novel type 1 reflection type 3 phase-state phase shifter. For comparison, we design a $0^0/11.25^0/22.5^0$ type1 reflection type phase shifter. For the convenience of the reader, Fig 4.5 is reproduced in Fig 6.8.

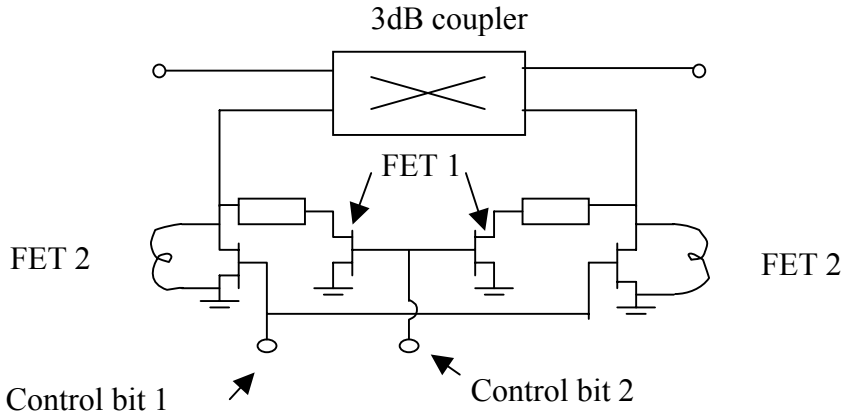


Fig 6.8 Schematic circuit diagram of a reflection-type phase shifter (Type 1)

The transmission coefficient S_{21} and its phase factor $\angle S_{21}$ are expressed as:

$$S_{21} = -j\Gamma_T = -j\frac{jX_T - 1}{jX_T + 1} \qquad (6.1)$$

$$\angle S_{21} = Arc\tan(\frac{1 - X_T^2}{2X_T}) = \frac{\pi}{2} - \theta \qquad (6.2)$$

where Γ_T and $X_T (= \tan\theta)$ are the reflection coefficient and the normalized reactance of the terminating network respectively. The detailed description of this circuit was given in Chapter 4 (Section 4.3). If θ = 11.25°, the output phase angles of the three phase states are 78.75°, 90° and 102.5° respectively which yield two differential phases of 11.25° and 22.5°. Figs 6.9-6.11 give the simulation performance of the 3 phase-state reflection type $0^0/11.25^0/22.5^0$ phase shifter.

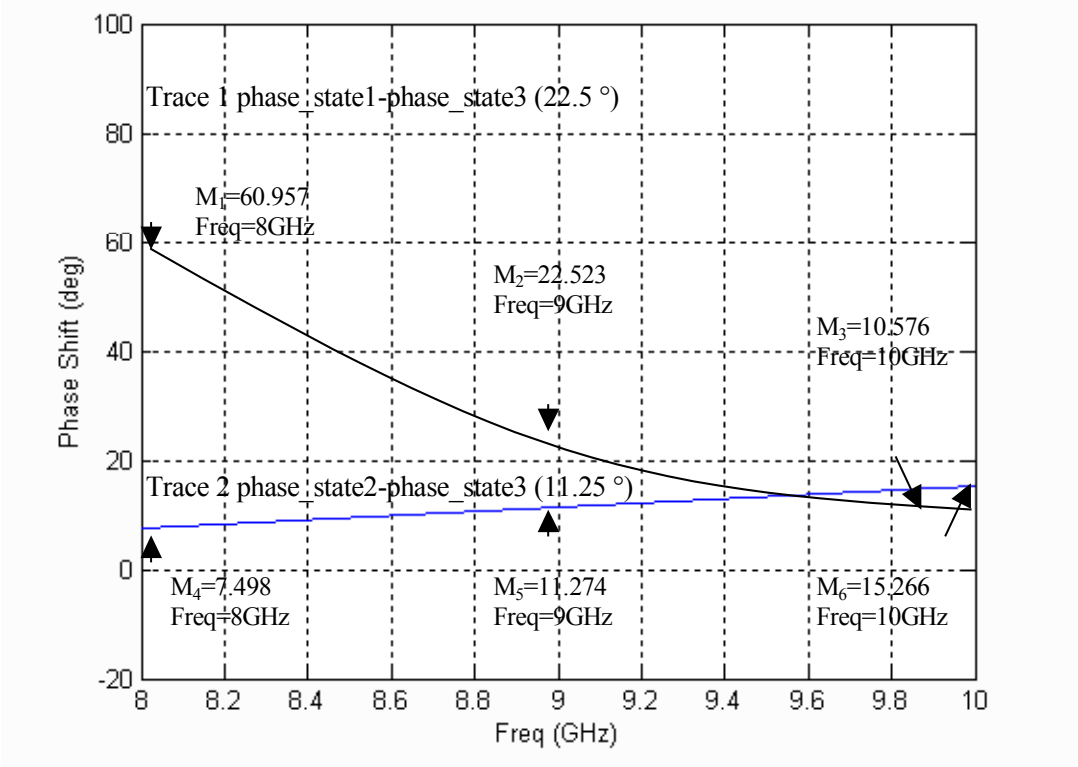


Fig 6.9 Phase response of reflection type

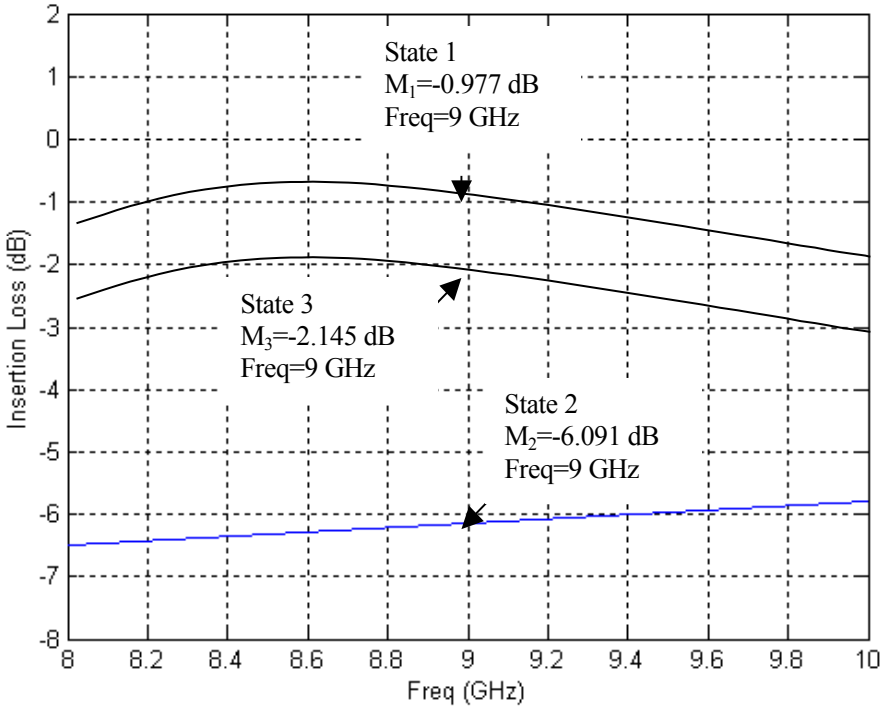


Fig 6.10 Insertion loss of reflection type

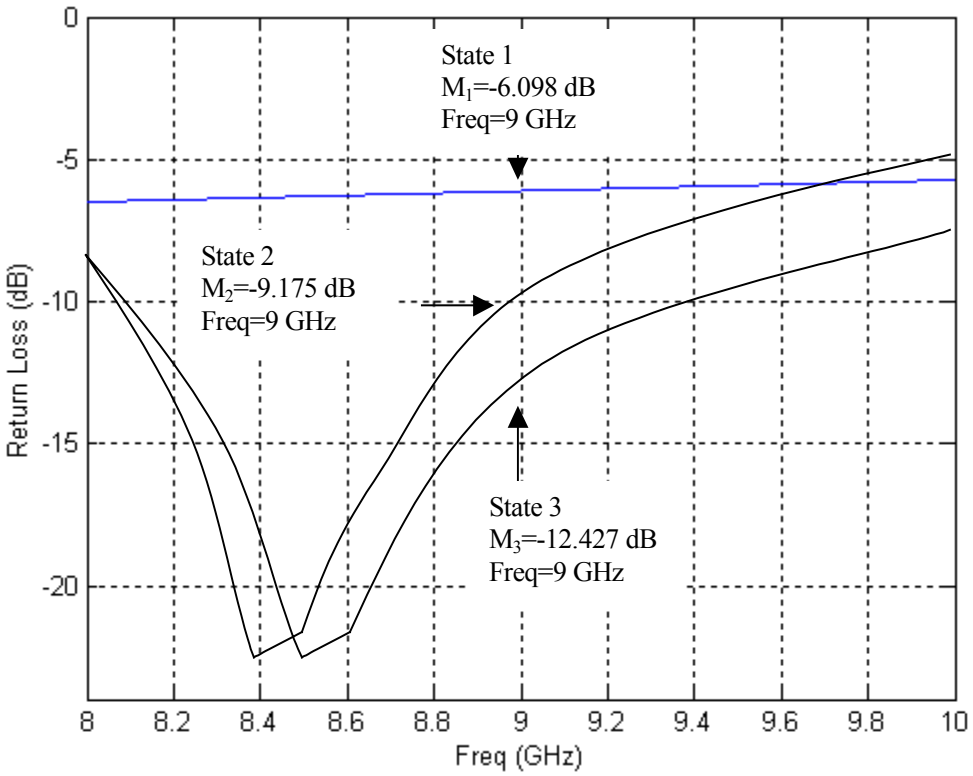


Fig 6.11 Return loss of reflection type

Comparing the phase performance in Fig 6.1 and Fig 6.9, it can be seen that the phase shift of the reflection type of 22.5^0 state at lower frequency increase rapidly to about 60^0.

6.4 Simulation Results for 2 Cascaded 3 Phase-State Phase Shifters

The above two bits of 3 phase-state LC switched-filter phase shifters are cascaded to give the continuous phase shift incremented in steps of 11.25˚ in the first quadrant. Thus the lower 3 bits of 11.25°, 22.5° and 45° in conventional 5 bits phase shifter can be replaced by two bits of the 3 phase-state shifter. Fig 6.12 shows the schematic circuit diagram of the 2 bit 3 phase-state phase shifter. The phase performance, insertion loss and return loss of the 2 bit phase shifter are plotted in Figs 6.13-6.15.

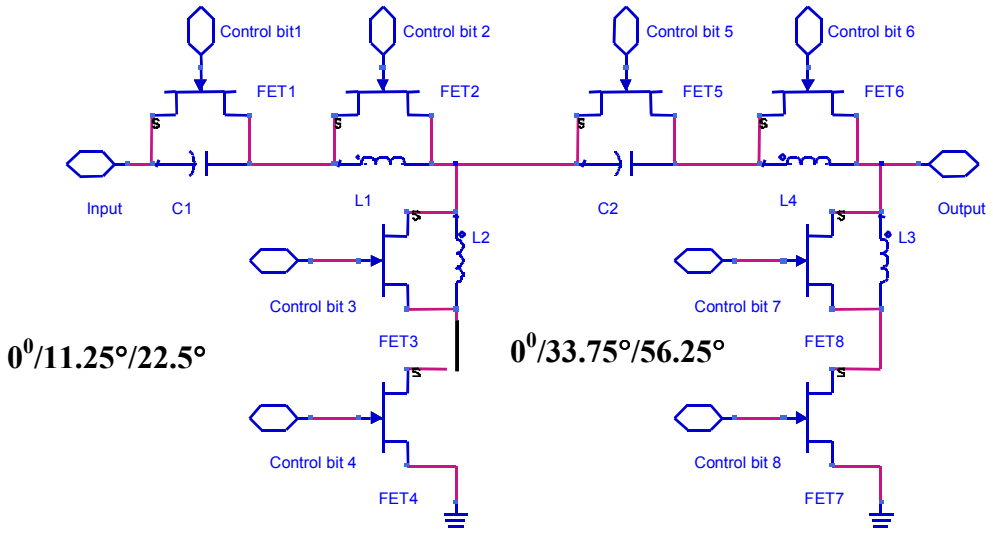


Fig 6.12 Schematic for 2 bit 3-phase-state LC switched-filter phase shifter

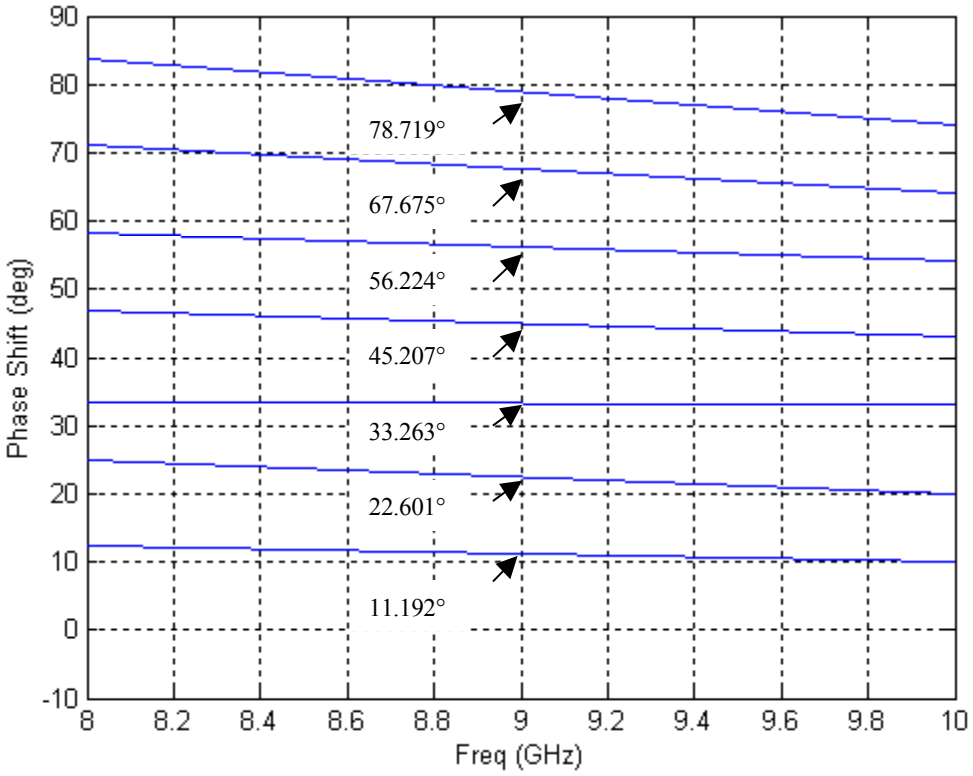


Fig 6.13 Phase response of two cascaded 3 phase-state phase shifters

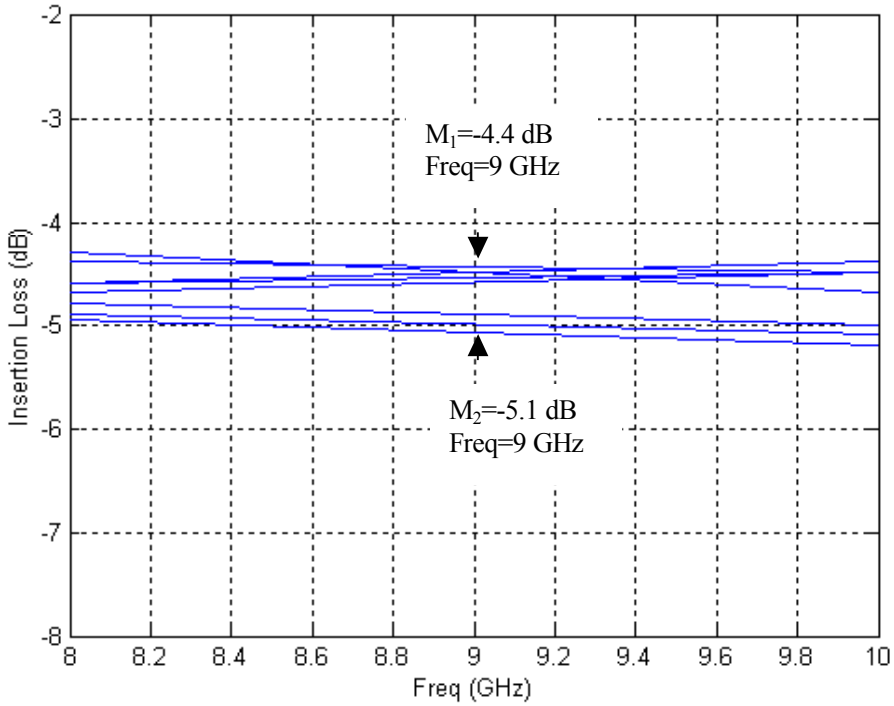


Fig 6.14 Insertion loss of two cascaded 3 phase-state phase shifters

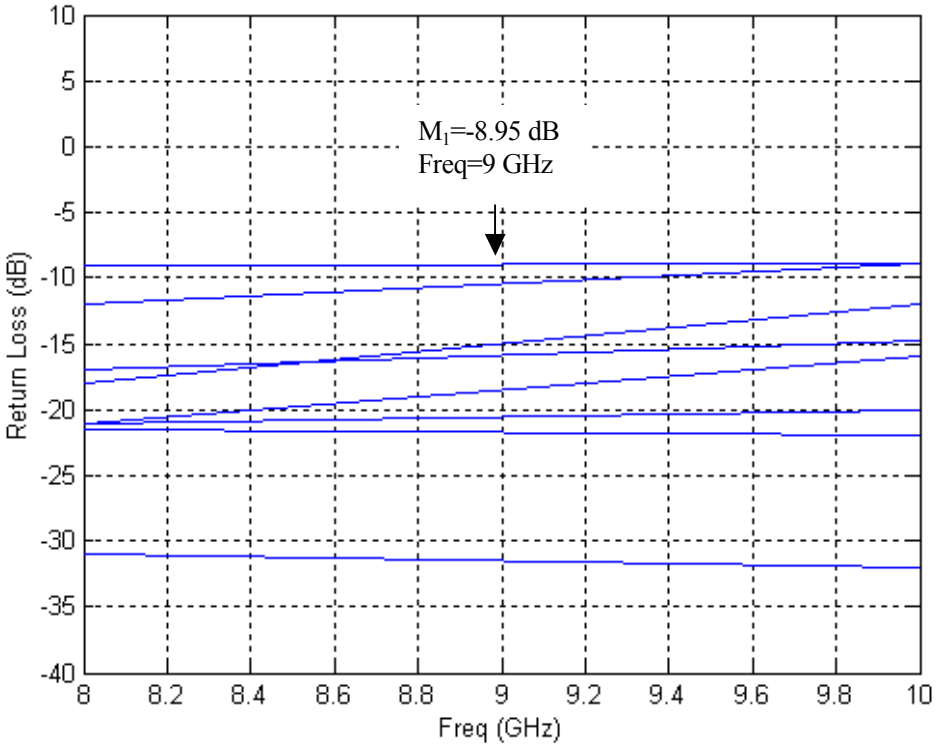


Fig 6.15 Return loss of two cascaded 3 phase-state phase shifters

The 2 bit 3 phase-state LC switched-filter phase shifter yields very significant improvement of size and also shows satisfactory performance. The total RMS phase error of all 8 phase-state in the first quadrant across the band of 8 GHz to 10 GHz is less than 1.05˚ and the phase error is well balanced over the bandwidth. The insertion losses are between –4.8±0.4 dB, with a maximum loss variation of 0.9 dB for all states over the 8 GHz to 10 GHz frequency range. It can also be seen that the insertion loss variation for each single state are less than 0.3 dB between 8 and 10 GHz. By reducing the total bit number, a maximum return loss of –8.95 dB is obtained. In K. Nakahara's paper, the 4 bit phase shifter (including 2 bits of 3 phase-state reflection type phase shifter) has a maximum RMS phase error as 10.2˚ and maximum insertion loss is 8.3 dB over a 10% bandwidth at X-Band.

6.5 Comparison with Cascaded 2 Phase-State Phase Shifters

From Fig 4.8 in Chapter 4, it may be noted that cascaded $0^0/11.25^0/22.5^0$ and $0^0/33.75^0/56.25^0$ 3 phase-state phase shifters replaces three cascaded 2 phase-state phase shifters, $0^0/45^0$, $0^0/22.5^0$ and $0^0/11.25^0$. For comparison, we design three cascaded 2 phase-state phase shifters, $0^0/45^0$, $0^0/22.5^0$ and $0^0/11.25^0$ using the conventional 2 phase-state high-pass low-pass switched filter design first proposed by Schindler and Miller for 45 ° and 90° in 1988 [23]. Fig 6.16 (a) shows the schematic circuit for a 2 phase-state high-pass low-pass phase shifter**.** Fig 6.16 (b) shows the block diagram of the cascaded 2-phase-state phase shifter.

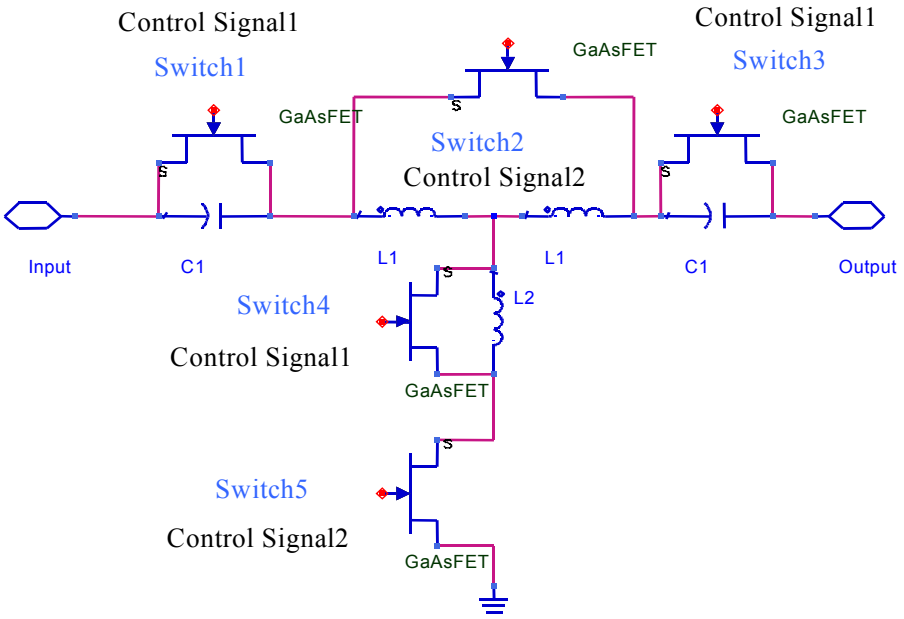


Fig 6.16 (a) Schematic circuit for 2 phase-state high-pass low-pass phase shifter

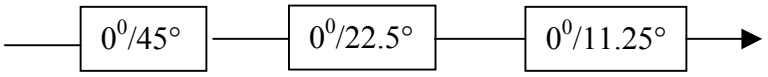


Fig 6.16 (b) Block diagram of cascaded 2 phase-state high-pass low-pass phase shifter

The 2 phase-state high-pass low-pass filter phase shifters above are implemented using the switched T network. The MESFET switches switch the network between a high-pass T network and a low-pass network that are shown in Fig 6.17. C_{ds}, the off-state capacitance of FET, is utilized as the network component. Table 6.1 shows the switching states, designed phase shifts as well as differential phase shifts for each of the three bits.

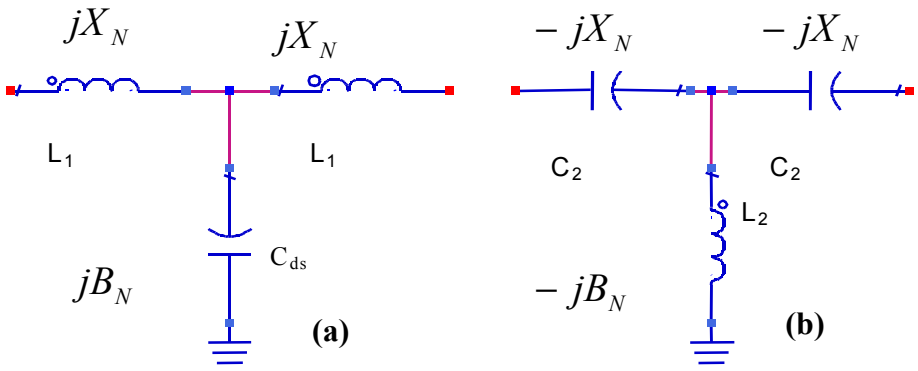


Fig 6.17 High-pass low-pass T network (a) low-pass (b) high-pass

Table 6.1 Switch states, and phase output for the circuit of Fig 6.17

Phase Shifter Block / Switches	11.25 °		22.5 °		45°	
	State a low pass	State b high pass	State a low pass	State b high pass	State a low pass	State b high pass
FET1	on	off	on	off	on	off
FET2	off	on	off	on	off	on
FET3	on	off	on	off	on	off
FET4	on	off	on	off	on	off
FET5	off	on	off	on	off	on
Output Phase	-5.625°	5.625°	-11.25°	11.25°	-22.5°	22.5°
Differential Phase Shift	11.25 °		22.5 °		45°	

For the low-pass sate, the transmission coefficient is given by:

$$S_{21} = \frac{2}{2(1 - B_N X_N) + j(B_N + 2X_N - B_N X_N^2)} \tag{6.3}$$

Where X_N and B_N represent the normalized reactance and susceptance, respectively.

The transmission phase ϕ_1 is given by

$$\phi_1 = \angle S_{21} \tan^{-1}\left[-\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)}\right] \tag{6.4}$$

For the high-pass state, the transmission coefficient S_{21} and the transmission phase ϕ_2 are obtained by replacing B_N by $-B_N$ and X_N by $-X_N$ in the previous equation. The differential phase shift is given by

$$\Delta\phi = \phi_1 - \phi_2 = 2\tan^{-1} -\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)} \tag{6.5}$$

Assuming the phase shifter to be loss-less and imposing the condition of perfect match, i.e. $|S_{21}=1|$, we get the relation

$$B_N = \frac{2X_N}{X_N^2 + 1} \tag{6.6}$$

and $$\Delta\phi = 2\tan^{-1} \frac{2X_N}{X_N^2 - 1} \tag{6.7}$$

Figs 6.18-6.20 show the simulation results of three cascaded conventional high-pass low-pass phase shifters: 11.25°, 22.5° and 45° shown in Fig 6.16.

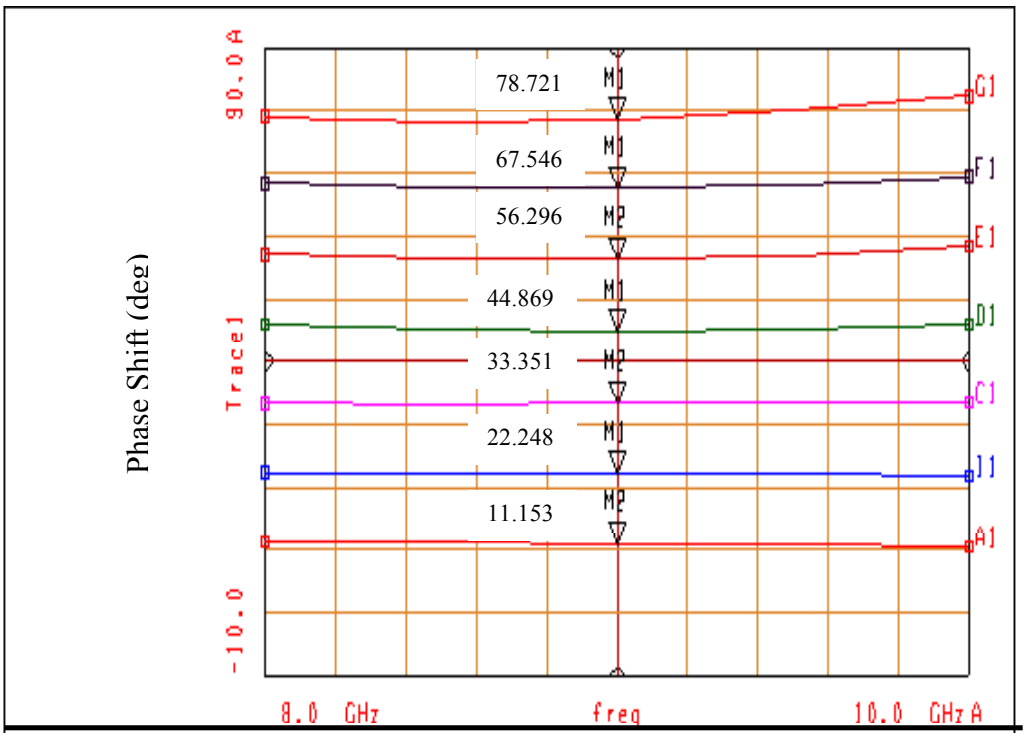


Fig 6.18 Phase response of three cascaded conventional 2 phase-state phase shifters

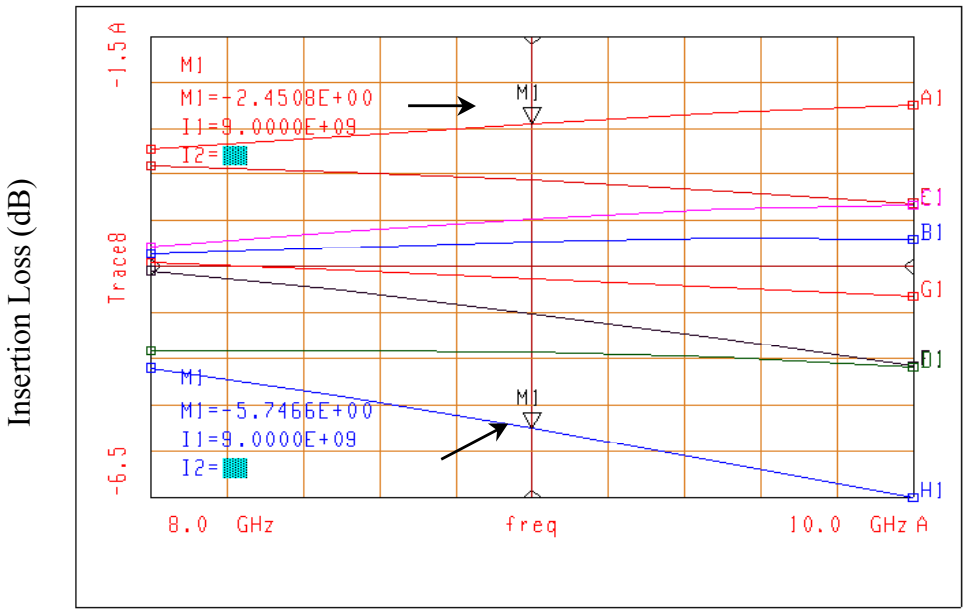


Fig 6.19 Insertion loss of three cascaded conventional 2 phase-state phase shifters

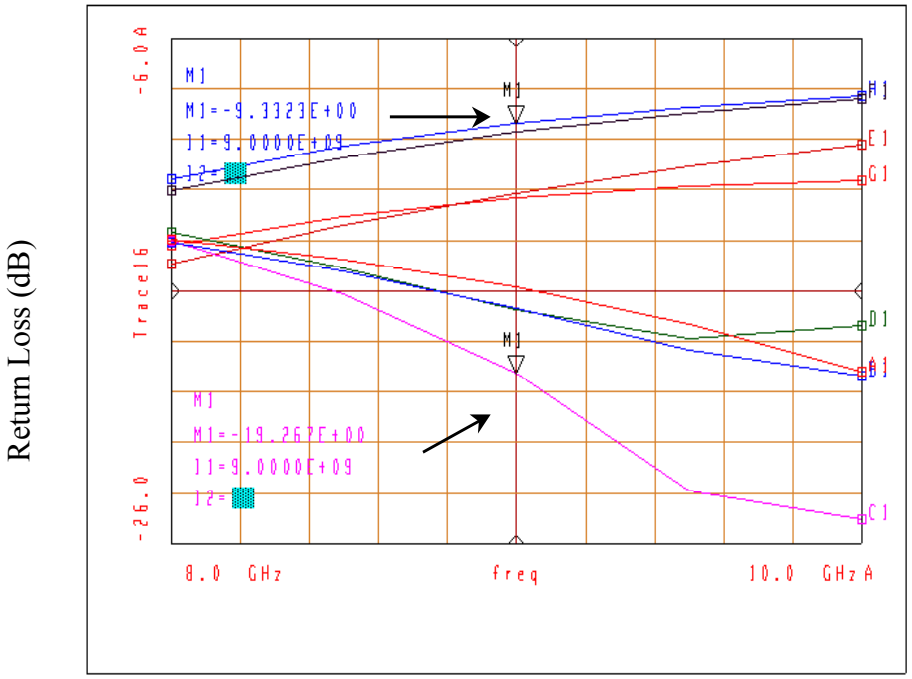


Fig 6.20 Return loss of three cascaded conventional 2 phase-state phase shifters

Compare the simulation results of 2 cascaded 3 phase-state LC switched filter phase shifter with that of 3 cascaded 2 phase-state high-pass low-pass phase shifter. The total size is reduced to 2/3 of the old one and the overall performance of the circuit is improved by reducing mismatch between each bit. The insertion losses of the 2 cascaded 3 phase-state phase shifter are between –4.8±0.5 dB, with a maximum loss variation of 0.9 dB for all states over the 8 GHz to 10 GHz frequency range. On the other hand, the insertion losses have a maximum variation of 4 dB for the 3 cascaded 2 phase-state phase shifter. Although the maximum return loss of single 3 phase-state phase shifter is 14 dB, the degradation of the total return loss is compensated by reducing the total bit number. It can be seen that a maximum return loss of 8.95 dB is obtained for the 2 cascaded 3 phase-state

phase whereas the maximum return loss of the 3 cascaded 2 phase-state phase shifters is 9.3 dB. Also, they both have a RMS phase error less than 1˚ across the entire bandwidth. It can be seen that the performances of the two phase shifters are comparable to each other whereas the former has better insertion loss variation, smaller size and less number of massy components like FET switches and inductors.

6.6 Summary

Table 6.2 provides the performance characteristics of 2 bit 3 phase-state LC switched-filter phase shifter, 3 bit conventional 2 phase-state high-pass low-pass phase shifter, 4 bit reflection type phase shifter in K. Nakahara's paper and some of the reported lumped element phase shifters [13, 14, 18, 23].

In conclusion, a novel MMIC 3 phase-state phase shifter is presented. It yields very significant improvement of size and also shows a good simulation result compared to the previous work.

Table 6.2 Comparison of performance

	3 phase-state LC switched filter	2 phase-state high-pass low-pass	A Novel 3 Phase-State Phase Shifter - K. Nakahara 1993 [14]	Wide band MMIC phase shifter - Yalcin A. 1984[13]	A 3 bit K/Ka Band MMIC Phase Shifter - M.J.Schindler 1988[23]	A GaAs Phase Shifter for Electronically Scanned Antenna - A.A.Lane [18]
Frequency range	8-10 GHz	8-10 GHz	X Band 10%	2-8 GHz	18-40 GHz	4 - 8 GHz
Number of phase bits	2 bits	3 bits 11.25°/22.5°/45°	4 bits 90°/225°,45°/90° 22.5°, 11.25°	2 bits 180°/90°	3 bits 180°, 90°, 45°	4 bits
Insertion loss	-4.8±0.4 dB	-4.5±2 dB	Max 8.3 dB	-7.5±1.5 dB	-9.5±2.5 dB	9.9±0.6dB
Insertion loss variation	0.9 dB	4 dB	4 dB	3 dB	5 dB	1.2 dB
Maximum return loss	8.95 dB	9.3 dB	NA	10 dB	10 dB	NA
RMS phase error at center frequency	Less than 0.1 deg	Less than 0.1 deg	NA	≈ 2 °	9.8 °	Less than 1.5 °
RMS phase error across entire band	Less than 1.05 deg	Less than 1 deg	10.2°	≈ 10 °	7.2°	2°
Number of FETs	8	11	14	12	16	NA
Number of Inductors	4	9	6	10	11	NA
Total FET gate periphery	Less than 1000 µm	Less than 1500 µm	4mm*5mm (chip Size)	7457 µm	7457 µm	6 µm (chip size)

Chapter 7

Conclusion and Future Developments

7.1 Conclusion

Phase shifter has important application in phased array system which addresses the need for reduced size, weight and cost. In recent years, because of the fast development of Monolithic Microwave Integrated Circuit (MMIC), there is a growing need for high-performance, small, inexpensive and easily implemented phase shifter design. In this report, a novel 3 phase-state phase shifter of switched-filter type (Fig 7.1) is presented, which adds one more phase state to the conventional 2 phase-state phase shifter without increasing the size of each bit. The total size is successfully reduced as compared to the conventional one and the overall performance of the circuit is improved by reducing mismatch between each bit.

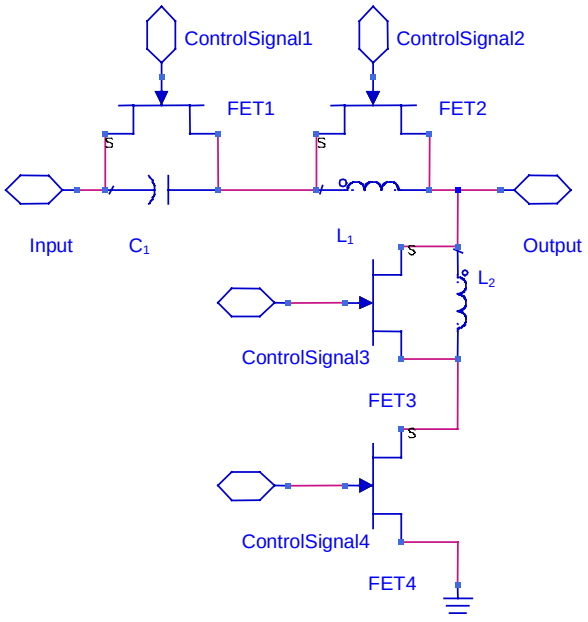


Fig 7.1 Simplified schematic of a 3 phase-state switched-filter type phase shifter

As described in the previous chapters, this novel MMIC 3 phase-state LC switched-filter phase shifter has the advantage of reducing the number of bits, switches and components, and thus decreases the size and the cost of the phase shifter which is an important factor for a planar array. The total RMS phase error of all 8 phase states in the first quadrant across the band of 8 GHz to 10 GHz is less than 1.05˚ and the insertion loss variation is less than 0.9 dB. The simulation results are also compared with conventional 2 phase-state phase shifter. It has very good performance on phase error and insertion loss variation in addition to the small size.

7.2 Future Works

The 3 phase-state LC switched-filter phase shifter has good performance except the return loss, which has the maximum value of 14 dB for single bit. This is because of the internal constraints of the LC switched-filter structure. Thus an area that one can explore into is to improve the LC structure to reduce the return loss. Another way is to design a 3 phase-state phase shifter using the high-pass low-pass switched filters. Although this will increase the size of the single bit, the total size is still smaller than the conventional 2 phase-state one and can achieve better performance.

This design is implemented by HP MDS software using UMS foundry Ph25 process library. All the results presented are simulation results. By implementing the circuit design on MMIC level, the experimental results can be obtained as verification of the design.

References

[1] Ian Robertson and Jim Turner, "*MMIC Design*", Institution of Electrical Engineers, Micheal Faraday House, London, 1995.

[2] Sunil Kansal, "*4-Bit MMIC Digital Phase Shifter*", B.Eng thesis, Department of Electrical Engineering, National University of Singapore, 1998/1999.

[3] Shiban K. Koul and Bharathi Bhat, "*Microwave and Millimeter Wave Phase Shifters*", Volume I: *Dielectric and Ferrite Phase Shifters*, Artech House Inc., MA 1991.

[4] Yalcin Ayasli, "*Microwave Switching with GaAs FETs*", *Microwave J.*, Vol. 25, November 1982, pp. 61-74.

[5] Robert V. Garver, "*Broadband Diode Phase Shifters*", *IEEE Trans. on Microwave Theory and Tech.*, Vol. MTT-20 June 1972, pp. 314-323.

[6] L. C. Upadhyayulu, "*Passive GaAs FET Switch Models and Their Applications in Phase Shifters*", *IEEE Int. Microwave Symp. Digest*, 1987, pp. 903-906.

[7] R.A. Gaspari and H.H. Yee, "*Microwave GaAs FET Switching*", *IEEE Int. Microwave Symp. Digest*, 1978, pp. 58-60.

[8] S.K. Koul, *"Computer Aided Design of GaAs FET Amplifiers", Technical Report,* School of Electronic Eng. Science, Univ. College of North Wales, U.K., 1984.

[9] Tan Chyun Yin, *"Investigation and Development of a Digital Phase Shifter",* Department of Electrical Engineering, National University of Singapore, 1998/1999.

[10] J. F. White, *"Diode Phase Shifters for Array Antennas", IEEE Trans. On Microwave Theory and Tech.,* Vol. MTT-22, June 1974, pp. 314-674

[11] B. M. Schiffman, *"A New Class of Broadband Microwave 90-Degree Phase Shifter", IEEE Trans. On Microwave Theory and Tech.,* Vol. MTT-6, April 1958, pp. 232-237.

[12] R. P. Coats, *"An Octave Band Switched Line Microstrip3B Diode Phase Shifter" IEEE Trans. On Microwave Theory and Tech.,* Vol. MTT-21, July 1973, pp. 444-449.

[13] Yalcin Ayasli, Steven W. Miller, Robert Mozz and Larry K. Hanes, *"Wide-Band Monolithic Phase Shifter", IEEE Trans. on Microwave Theory and Tech*., Vol. MTT-32, Dec. 1984, pp. 1710-1714.

[14] K. Nakahara, S. Chaki, N.Andoh and H. Matsuoka, *"A Novel Three Phase-States Phase Shifter", IEEE Microwave Theory and Tech. Symposium Digest,* 1993, pp. 369-372.

[15] Yalcin Ayasli, Aryeh Platzer, James Vorhaus and Leonard D Reynolds, *"A Monolithic Single-Chip X Band Four-Bit Phase Shifter", IEEE Trans. on Microwave Theory and Tech.,* Vol. MTT-30, Dec. 1982, pp. 2201-2205.

[16] C. K. Pao, *"V-Band Monolithic Phase Shifters", 10th Annual IEEE GaAs IC Symp. Digest,* 1988, pp. 269-272.

[17] Levy D., Noblet A. and Bender Y.W., *"A 2-18 GHz Monolithic Phase Shifter for Electronic Warfare Phase Array Applications", GaAs IC Symposium, Technical Digest, 10th Annual IEEE* 1988, pp. 265 – 268.

[18] Lane A.A., *"GaAs MMIC Phase Shifters for Phased Arrays", IEE Colloquium on Solid State Components for Radar, 1988,* pp. 3/1 - 3/5.

[19] Goldfarb M.E., *"A Novel Design for a MMIC 180 Degree Phase Shifter", Microwave and Millimeter-Wave Monolithic Circuits Symposium, Digest,* 1992, pp. 141-143.

[20] Boire D. C. and Marion R., *"A High Performance 6-18 GHz Five Bit MMIC Phase Shifter", GaAs IC Symposium, Technical Digest, 17th Annual IEEE*, 1995, pp. 267 – 270.

[21] Andricos, C., Bahl, I.J. and Griffin, E.L.; *"C-Band 6-bit GaAs Monolithic Phase Shifter", Microwave Theory and Techniques, IEEE Transactions on,* Vol. 33 Issue. 12, Dec 1985, pp. 1591 -159

[22] Reber, R.H., and Felde, H.P., *"A monolithic single-chip C-band 6-bit phase shifter , 21 European Microwave Conf. Proc., Stuttgart,* 1991, pp.479-482

[23] M. J. Schindler and M. E. Miller, *"A 3 bit K/Ka band MMIC phase shifter", Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1988. Digest of Papers., IEEE 1988* , 24-25 May 1988, pp. 95 -98

Appendix:

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A Novel MMIC 3 Phase-State Switched-Filter Phase Shifter

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Phase shifter is an important component of phased array system which may have thousands of phase shift elements. Thus size and cost are very important factors when designing phase shifter. In recent years, Monolithic Microwave Integrated Circuit (MMIC) addresses the need for reduced size, weight and cost without compromising on performance. In this paper, a novel 3 phase-state phase shifter of switched-filter type is presented which adds one more phase state to the conventional 2 phase states phase shifter without increasing the size of each bit. The total size is successfully reduced to 2/3 of the old one and the overall performance of the circuit is improved by reducing mismatch between each bit.

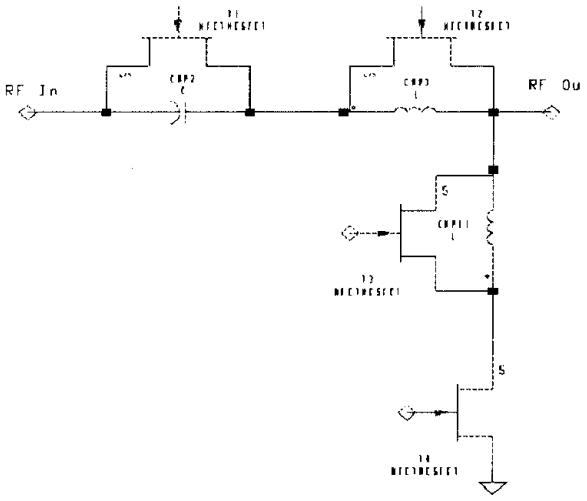

Figure 1. Simplified Schematic of a 3 phase-state switched-filter phase shifter shifter.

Figure 1 shows the simplified schematic diagram of a novel 3 phase-state switched-filter phase shifter proposed in our design. The circuit takes into account of FET parameters as part of the filter network so that the need to parallel resonate the off state capacitance can be eliminated. By switching the switches in a suitable combination, the circuit behaves like three low-pass and high-pass filters respectively. The value of the lumped elements and gate periphery of the switches are all treated as parameters for optimization to get three different phase states. By cascading two of such bits with different phase settings, 11.25°, 22.5° of one bit and 33.75°, 56.25° of another bit, we can have continuous phase shift incremented in steps of 11.25 degree in the first quadrant. Thus the lower 3 bits of 11.25°, 22.5°, 45° degree in conventional design can be replaced by two bits of the three-state phase shifter.

In conclusion, a novel MMIC 3 phase-state phase shifter is presented. It yields very significant improvement of size and also shows a good simulation result. The total RMS phase error of all 8 phase states in the first quandrant across the band of 8 GHz to 10 GHz is less than 1.05 degree and the insertion of loss variation is less than 0.9 dB. By reducing the total bit number, the return loss is also much better than cascading three 2 phase-state phase shifters.