ATOMIC LAYER DEPOSITED HAFNIUM–BASED GATE DIELECTRICS FOR DEEP SUB–MICRON CMOS TECHNOLOGY

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STATEMENT OF RESEARCH PROBLEMS

My research problem is to investigate the feasibility of atomic layer deposited Hf-based dielectrics to replace the conventional SiO_2 as gate dielectrics in CMOS technology. This study addresses the effect of Si surface treatments and post-deposition annealing on fixed charge concentration, phase transformation and thermal stability in HfO_2 and Hf-aluminate films.

SUMMARY

This study demonstrated that ultrathin chemical oxide underlayers ~ 5 Å provide improved growth of atomic layer-deposited (ALD) HfO_2 films compared to the thermal oxides/oxynitirde underlayers typically used for high-κ gate stacks. HfO_2 growth on chemical oxide occurs in a highly predictable manner from the onset of the first pulse, with no incubation period. By employing an ultrathin chemical oxide together with optimized post-deposition annealing conditions, both the fixed charge and the leakage current can be minimized at the cost of a slight increase in equivalent oxide thickness. A small flatband voltage shift, ΔV_{FB} of ~ 20-40 mV, was achieved by using high temperature (800ºC – 900ºC) annealing. This corresponds to a very low fixed charge concentration of ~ 2×10^{11} cm^{-2}. Lower annealing temperatures, 600ºC – 700ºC, were found to be less effective at minimizing ΔV_{FB} (ΔV_{FB} ~ 100-200 mV). With the proper chosen annealing conditions, gate leakages ~ 10000× lower than those of conventional SiO_2 were also demonstrated. The as-deposited ALD HfO_2 films on the chemical oxide underlayers are amorphous, while deposition on thermal oxide underlayers leads to polycrystalline films. The thermal stability of the amorphous Hf-aluminate films is significantly improved through the controlled addition of Al_2O_3. Films with 75% Al remain amorphous even after a 1050ºC spike anneal, which is a typical thermal cycle in CMOS processing. By varying the relative number of HfO_2 and Al_2O_3 cycles during ALD, the Hf-aluminates composition can be precisely tailored to the desired stoichiometry.

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LIST OF ACRONYMS AND SYMBOLS

AC	Alternating Current
ADF	Annular Dark Field
AFM	Atomic Force Microscopy
ALCVD	Atomic Layer Chemical Vapor Deposition
ALD	Atomic Layer Deposition
ALE	Atomic Layer Epitaxy
APCVD	Atmospheric Pressure Chemical Vapor Deposition
BF	Bright Field
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DC	Direct Current
DF	Dark Field
EOT	Equivalent Oxide Thickness
FWHM	Full Width at Half Maximum
GOF	Goodness of Fit
High-κ	High Dielectric Constant
IC	Integrated Circuit
ICDD	International Center for Diffraction Data
ITRS	International Technology Roadmap for Semiconductors
JVD	Jet Vapor Deposition
LCR	Inductance Capacitance Resistance

LSTP	Low Standby Power
MEIS	Medium Energy Ion Scattering
MOS-C	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCSU	North Carolina State University
NO	Nitric Oxide
PDA	Post-Deposition Annealing
RBS	Rutherford Backscattering Spectroscopy
RT	Room Temperature
RTA	Rapid Thermal Anneal
RTO	Rapid Thermal Oxidation
SC1	Standard Cleaning 1
SE	Spectroscopic Ellipsometer
SIA	Semiconductor Industry Association
SOM	Sulfuric Ozone Mixture
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
TMA	Trimethylaluminum
TOFSIMS	Time-Off-Flight Secondary Ion Mass Spectroscopy
ULSI	Ultra Large Silicon Integration
UV	Ultraviolet
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy

η	Order of reflection
λ	Wavelength
ω	Angular frequency of AC current
ω	Sample rotation angle around an axis perpendicular to the incident x-ray beam
A	Gate electrode area
C	Total capacitance
C_{min}	Minimum capacitance
C_{ox}	Oxide capacitance
C_s	Silicon capacitance
C–V	Capacitance-voltage
d	Lattice spacing
D	Density reduction factor
D_{it}	Interface trap density
E_1	Ion energy prior collision in MEIS experiment
E_2	Ion energy after collision in MEIS experiment
E_3	Ion energy leaving sample surface in MEIS experiment
E_c	Conduction band energy
E_{Fn}	Fermi level for *n*-type silicon
E_{Fp}	Fermi level for *p*-type silicon
E_o	Incident ion energy in MEIS experiment
E_v	Valence band energy
G	Conductance
I_D	Drain current

I_G	Gate leakage current
I–V	Current-voltage
J_G	Gate leakage density
k	Extinction coefficient
K	Kinematic factor
M_1	Mass of incident ion
M_2	Mass of target atom
n	Index of refraction
N	Bulk density
N_A	Acceptor doping density
N_f	Fixed charge density
Q_f	Fixed oxide charge
Q_{it}	Interface trap charge
Q_m	Mobile ionic charge
Q_{ox}	Bulk oxide charge
R	Growth rate
R'_p	Reflection coefficient parallel to the light incidence plane
R'_s	Reflection coefficient perpendicular to the light incidence plane
R_s	Sheet resistance
S	Source in a transistor
s	Time length for either pulse or purge in ALD
t	Film thickness
$t_{high\text{-}\kappa}$	Film thickness of high-κ materials

$t_{i/f}$	Interfacial layer (underlayer) thickness
V_D	Drain voltage
V_{FB}	Flatband voltage
V_G	Gate voltage
W_{eff}	Effective full width at half maximum
W_{meas}	Measured full width at half maximum
W_{system}	Measured full width at half maximum of (111) Si peak
x	Number of H_2O / TMA cycles pulsed in 1 bilayer
y	Number of H_2O / $HfCl_4$ cycles pulsed in 1 bilayer
z	Total number of bilayers
ΔE_C	Conduction band offset to Silicon
ΔV_{FB}	Flatband voltage shift
θ	Bragg angle
θ_M	MEIS scattering angle
ρ	Resistivity
Φ_{ms}	Work function difference between polysilicon gate and silicon substrate
Δ	Phase shift induced by light reflection
χ	Rotation angle about the direction of the incident x-ray beam
ε_o	Permittivity of free space
κ	Dielectric constant
$\kappa_{high\text{-}\kappa}$	Dielectric constant of high-κ materials
ψ	Ellipsometric angle

LIST OF PUBLICATIONS

1) M.-Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, W. H. Lin, A. See, S. K. Lahiri, M. E. Loomans, P. I. Räisänen, and T. Gustafsson, Suppressed Crystallization of Hf-based Gate Dielectrics by Controlled Addition of Al_2O_3 using Atomic Layer Deposition, Appl. Phys. Lett, **81** (2002) 4218.

2) M.-Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, P. M. Voyles, D.A. Muller, M. Bude, W. H. Lin, A. See, M. E. Loomans, S. K. Lahiri, and P. I. Räisänen, Morphology and Crystallization Kinetics in HfO_2 Thin Films Grown by Atomic Layer Deposition, J. Appl. Phys, **93** (2003) 1477.

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CHAPTER 1: INTRODUCTION

According to the 2001 edition of *The International Technology Roadmap for Semiconductors* (ITRS), it is expected that high dielectric constant materials may be needed as early as the year 2005 (80 nm technology node) to replace the conventional SiO_2 as gate oxide in some semiconductor devices (low power logic devices). While it may be technically feasible to manufacture 1.5 nm and thinner SiO_2 on 200 mm wafers, the direct gate-to-channel tunneling current associated with such thin SiO_2 – a fundamental, intrinsic physical phenomenon – compromises its ability to remain an insulator. An intensive global search is now, therefore, in progress to find an alternate gate dielectric to replace SiO_2.

To date, however, a gate dielectric material able to fulfill all the requirements for integration into future transistors has yet to be identified. In response to the need to identify a suitable replacement for SiO_2, the present work is aimed at exploring the feasibility of using atomic layer deposited (ALD) Hf-based materials as gate dielectrics in deep sub-0.1 μm CMOS technology. As will be discussed in section 1.1.2, besides having a high dielectric constant, HfO_2 has been reported to be thermodynamically stable when in contact with Si, and to be compatible with the conventional poly-Si process. The aluminates of this dielectric are also of interest due to the formation of a relatively stable amorphous phase in these materials. However, before high-κ materials can be inserted into the CMOS process, it must be possible to grow thin, dense, and smooth continuous films of the materials, and to control the fixed charge in the films. Other important issues such as thermal stability during thermal annealing and the effect of crystallinity of the

high-κ films on electrical properties, especially leakage current, also need to be addressed. This work will, therefore, specifically address the effect of surface treatments on the ALD Hf-based dielectrics growth behavior, and the effect of post-deposition anneal processing on the physical and electrical properties, including thermal stability, morphology, and crystallinity, and on the fixed charge in the films.

In order to give a comprehensive overview of the importance of high-κ dielectric materials to future CMOS technology, this chapter starts by addressing CMOS scaling and how it has led to an extensive search for alternative gate dielectric materials as we approach the deep sub-micron regime. In addition to this, a review of current work and literature in the area of alternative gate dielectrics is provided, as it will be useful as background material for readers from multi-disciplinary fields. In this work, HfO_2 and Hf-aluminate films were deposited using the ALD process. Section 1.2 outlines the basic principles of operation and the capabilities of this relatively new and potentially manufacturable deposition method. This comprehensive overview of ALD will facilitate the discussion throughout the thesis. Following this are chapters devoted to portraying and discussing the results of this research and the possibilities for successful integration of these Hf-based materials into future CMOS technology.

1.1 High-κ Dielectrics

1.1.1 The Need for High-κ Dielectrics

Integrated circuits (ICs) built with complimentary-metal-oxide-semiconductor (CMOS) transistors were introduced in the 1980s, and now the CMOS transistor has become the key component of most ultra large silicon integration (ULSI) devices. CMOS is so-named because it uses both *p*- and *n*-channel MOS field effect transistors (MOSFETs) to form the ICs (Fig. 1.1). The increased performance of silicon ICs

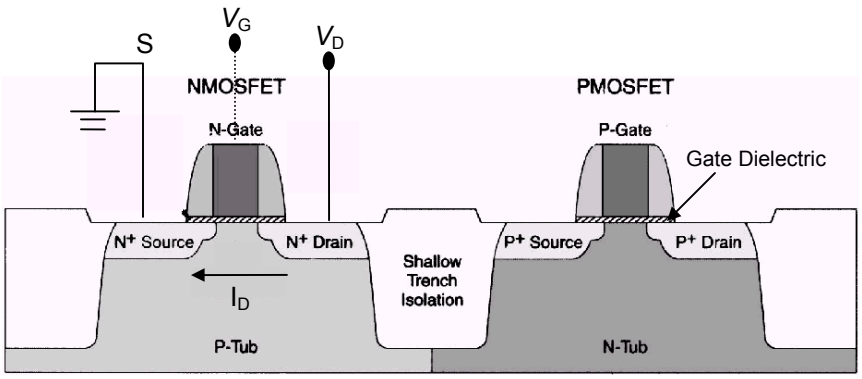

Fig. 1.1 Schematic illustration of a CMOS. V_G and V_D represent the gate and drain voltage respectively. S denotes the source and I_D is the drain current flowing when the NMOSFET is in ON-state. [adapted from Ref. 4; courtesy of C. P. Chang, Agere Systems]

has been achieved mainly by scaling down the size of individual MOSFETs. MOSFET scaling results in faster switching speed, lower power dissipation, and greater density (more devices per area), which enables cost/performance trends to be maintained [1-4].

SiO_2 has been the mainstay of the industry for the past 40 years. However, due to the continuous scaling down of the SiO_2 gate dielectric thickness, high-κ materials may be required for the gate dielectric by around the year 2005 [5], especially for low standby

power logic applications where the allowable gate leakage is very low [5, 6]. Table 1.1 lists the equivalent oxide thickness (EOT; to be discussed later) requirements associated with low standby power logic (LSTP) devices, outlined in the 2001 edition of the ITRS [5].

Table 1.1 Highlights of near-term technology requirements outlined by 2001 SIA International Technology Roadmap for Semiconductors [Ref. 5]

Year of Production	**2001**	**2002**	**2003**	**2004**	**2005**	**2006**	**2007**
Technology Node	130 nm	115 nm	100 nm	90 nm	80 nm	70 nm	65 nm
Physical Gate Length for *low standby power* (LSTP) (nm)	90	75	65	53	45	37	32
Equivalent physical Oxide Thickness for LSTP (nm)	**2.4 - 2.8**	**2.2 - 2.6**	**2.0 - 2.4**	**1.8 - 2.2**	**1.6 - 2.0**	**1.4 - 1.8**	**1.2 - 1.6**

Manufacturable solutions exists and are being optimized

Manufacturable solutions are found

Manufacturable solutions are NOT found

According to this roadmap, oxynitride dielectrics (with a leakage current about 100 times lower than that of SiO_2) will be the solution for 100 nm and 90 nm technology nodes to meet the gate leakage specifications. However, beyond 80 nm technology, high-κ dielectrics are expected to be needed. This comes from the fact that conventional SiO_2 gate oxide has approached its fundamental material limits due to the simultaneous needs for low leakage current and high capacitance. It has been shown that a direct tunneling current through SiO_2 grows exponentially with the decreasing physical thickness of the dielectric film [7]. The literature shows that when SiO_2 thinner than 15 Å is required (requirements in 80 nm technology node and beyond; see Table 1.1), the leakage current is larger than 1 A/cm^2, which cannot be tolerated because it significantly increases the OFF-current and standby power of a device [5, 7]. Even if devices were designed to tolerate higher leakage current and power dissipation, thus permitting the gate dielectric

thickness to be reduced further, it would not be a long-term solution because other processing problems such as boron penetration and dielectric reliability would certainly arise [6].

The term *equivalent oxide thickness* (EOT) refers to the relative dielectric thickness of a high-κ film, using the thickness of a SiO_2 film of equivalent capacitance as a metric. Equation 1.1 expresses this relationship mathematically.

$$\mathrm{EOT} = \frac{3.9\varepsilon_o A}{C_{ox}} = t_{i/f} + \frac{3.9 t_{\mathrm{high}-\kappa}}{\kappa_{\mathrm{high}-\kappa}} \tag{1.1}$$

C_{ox} is the gate oxide capacitance and can be written as

$$C_{ox} = \frac{\kappa\varepsilon_o A}{t}, \tag{1.2}$$

where κ is the dielectric constant of the gate dielectric (in the case of the SiO_2 gate dielectric, κ = 3.9), ε_o is the permittivity of free space (= 8.85 x 10^{-12} F/m), A is the area of the capacitor, and t is the physical thickness of the dielectric film. The EOT for a stacked dielectric comprising a layer of SiO_2 underlayer with thickness, $t_{i/f}$, and a gate dielectric with a higher dielectric constant, $\kappa_{\text{high-}\kappa}$, can therefore afford a larger physical thickness ($t_{\text{high-}\kappa}$) when it is employed to achieve a capacitance equivalent to that of SiO_2. For example, a ~ 50 Å thick high-κ dielectric film with κ ~ 20, with no SiO_2 underlayer, yields an EOT of 10 Å. It is worth noting, however, that this simple calculation ignores the possible quantum mechanical effect due to quantization in the Si substrate and depletion effect from the gate electrode [8]. Each of this effects may cause an over-estimation of the EOT values by 2-3 Å. Note that in this study, the term *physical*

thickness will be referred to later as *ellipsometry thickness*, since the thickness is measured by an ellipsometer.

1.1.2 High-κ Dielectrics – Candidates for SiO_2 Replacement

Currently, many experimental efforts are underway to search for alternative gate dielectric materials to replace SiO_2. The materials receiving the most attention are HfO_2, ZrO_2, La_2O_3, Y_2O_3, mixtures of these materials with Al_2O_3 (aluminates) and SiO_2 (silicates), and pure Al_2O_3. In general, besides having a dielectric constant significantly larger than that of SiO_2 (~3.9), the candidates for gate oxide should meet the following requirements [6, 9]:

(i) The gate oxide should be thermodynamically stable (i.e., no interface reaction) when in contact with Si or SiO_2.

(ii) Dopant (especially boron) penetration from the gate electrode through the gate oxide should be low to avoid a shift in the threshold voltage.

(iii) The interface between high-κ and Si or SiO_2 should have a low interface trap defect density, $D_{it} < 10^{10} - 10^{11}$ $eV^{-1}cm^{-2}$, to minimize the shift in threshold voltage.

(iv) The oxide layers should contain a low density of defects, such as fixed oxide charge, oxide trapped charge, and mobile ionic charge defects, so that the mobility can be maintained above 90% of that for SiO_2 of the same EOT [9]. An explanation of these different charges given in chapter 2, section 2.5.

(v) The gate oxide material should have a large band gap, together with a band alignment that results in a large silicon-to-insulator energy barrier height in order to prevent tunneling of both electron and hole carriers through the gate oxide.

(vi) The gate leakage density, J_G, should be as low as possible (preferably more than 3 orders of magnitude lower than SiO_2 of the same EOT).

(vii) The gate oxide should be compatible with conventional CMOS processing.

To date, however, there is no single material that is able to satisfy all the requirements listed above. Most of the high-κ candidates are not stable in direct contact with Si and require a thin silicon dioxide layer between the high-κ material and Si in order to prevent high-κ/Si interface reaction [6]. In fact, even if this interface reaction is not a problem, a very thin SiO_2 layer will likely still be required at the channel and/or gate electrode interface in order to preserve interface state characteristics and, thus, channel mobility [5, 10]. This has been identified in the 2001 ITRS [5] as one of the major problems for high-κ dielectrics, since introduction of SiO_2 underneath will undesirably increase the EOT. In addition, the gate oxide/Si substrate interface must have minimum oxide fixed charges and interface trap charges to minimize carriers' scattering at the channel (maximize mobility). Also, in gate dielectric materials, there is a general tendency of inverse correlation between the bandgap size and the dielectric constant [6], so that it becomes difficult to meet the leakage current requirement. In order to have a minimum gate leakage current, amorphous layers are generally preferred for gate oxides to minimize electrical and mass transport along the grain boundaries; a polycrystalline layer, however, may also be acceptable [11]. Consequently, the thermal stability of the amorphous phase

of the high-κ films becomes one of the key considerations in selecting suitable candidates. In this study, the phrase *thermal stability* refers to the ability of a phase to retain its amorphous state when subjected to thermal annealing.

Table 1.2 lists relevant data for several potential high-κ candidates recently investigated [6]. A substantial amount of work has been reported for each of these materials. Unfortunately, searching for the best candidate is not an easy task since each of these materials does impose some challenges, which will be briefly reviewed here.

Table 1.2 Comparison of relevant properties for high-κ candidates [adapted from Ref. 6].

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

[a] Calculated by Robertson [Ref.: J. Robertson, J. Vac. Sci. Technol. B **18** (2000) 1785.]
[b] Mono. = monoclinic
[c] Tetra. = tetragonal

Materials such as Y_2O_3 [12] and Al_2O_3 [13-15] with moderate κ values offer only relatively small increases in gate oxide thickness, and would therefore make it a relatively short-term solution for the industry's needs. If no longer-term solution is available by the time a replacement is required, Al_2O_3, which has been shown to be one of the insulators that does not have an interface reaction with Si substrate [13, 14], may indeed be suitable. Before it can be incorporated into CMOS technology, however, the considerable flatband voltage shift, ΔV_{FB}, resulting from fixed charge in this film must be reduced [15].

A substantial amount of effort has gone towards investigating group IVB oxides, specifically ZrO_2 and HfO_2, and their silicates [6, 16-19]. Pure oxide ZrO_2 has $\kappa \sim 25$, but one concern is that it reacts with poly-Si gate electrodes [20]. In particular, Lee *et al*. [20] found that chemical vapor deposited (CVD) ZrO_2 decomposed into Zr metal when a gate stack comprising poly-Si/ZrO_2 is annealed at 950°C in N_2 ambient. This ZrO_2 instability would be unacceptable in current CMOS processing. With HfO_2, on the other hand, no reaction at the poly-Si/HfO_2 interface was observed under identical processing conditions [21]. Nevertheless, recent work with ZrO_2 has yielded encouraging results. Copel *et al*. [22] demonstrated that a highly uniform layer of ZrO_2 can be deposited using the ALD method, and it was found that there is no reaction at ZrO_2/SiO_2 underlayer interface under vacuum annealing up to 900°C. Using yttria-stabilized ZrO_2, Wang *et al*. [23] reported that a leakage current density as low as $\sim 1.1 \times 10^{-3}$ A/cm^2 at 1V was achieved for an EOT ~ 14.6 Å. Although promising results have been reported, concerns remain regarding the reaction with the poly-Si gate, ΔV_{FB}, and diffusion of dopant impurities through ZrO_2 film. In fact, a relatively high ΔV_{FB} of a few hundred milivolts has been reported in the literature [24, 25]. Boron penetration through ZrO_2/SiO_2 structures after annealing at temperatures as low as 850°C has also been reported [26].

All the high-κ candidates mentioned above have advantages, but each has its own undesirable properties as well. The industry has not yet decided which gate dielectric to integrate into CMOS processing, but there is a strong leaning towards Hf-based materials [27]. Thus, HfO_2 and Hf-aluminates are the focus of study in this work. The current status of these two materials in gate application is addressed in the next section.

1.1.3 Current Status of HfO_2 and Hf-aluminates

HfO_2 has many desirable properties, such as a relatively large band gap (5.68 eV), a moderately high dielectric constant [28], and compatibility with poly-Si gate electrodes [21]. Gusev *et al*. [29] reported that ALD HfO_2 does not have an undesirable interface reaction when in contact with Si and exhibits ~ 4 orders of magnitude lower leakage current than SiO_2 for the same EOT. More recently, S. J. Lee *et al*. [30] reported that CVD HfO_2 with EOT ~ 7.8 Å and a leakage current of 5×10^{-4} A/cm^2 has been achieved. Boron penetration through HfO_2 films was detected after a 950°C anneal, but can be effectively suppressed by alloying the films with SiO_2 (forming Hf-silicates) [31].

At present, one of the hurdles facing researchers is bringing the electron mobility of HfO_2 in line with that of SiO_2. Gusev *et al*. [29] suggest that mobility can be improved by processing (interface engineering, thermal budget, etc.). Recent reports by Onishi *et al*. [32] show that NO anneals on HfO_2/Si gate stack yield a higher mobility compared to NH_3 anneal. Nevertheless, reports in the literature [24, 29, 32, 33] show that even with an optimized processing condition, the channel carrier mobility value for HfO_2 gate stack was found to be smaller, by a factor of ~ 2, than that expected by the universal mobility curve for SiO_2 (at an effective normal field in the inversion layer of 1 MV/cm, the electron mobility for SiO_2 is ~ 220 cm^2/Vs) [33]. This mobility degradation is currently attributed to Coulomb scattering due to interface trap charges and fixed charges in the films [29, 33]. It should be noted that these undesirable charges in the films also cause ΔV_{FB}, although a minor contribution of the ΔV_{FB} can also arise from oxide damage associated with gate electrode deposition or other forms or processing treatments [6, 29]. Large ΔV_{FB} (~ 100 - 300 mV) values have been observed by many independent groups

[6] for HfO_2 films; however, the origin of the fixed charge in the channel region and an effective way to reduce or perhaps eliminate these charges are still poorly understood.

The thermal stability of high-κ materials is another property that has become a key issue in selecting suitable high-κ candidates [6, 34]. This particular area has been studied for HfO_2 deposited by techniques such as ion beam assisted deposition [35], ALD [36, 37], and jet vapor deposition (JVD) [38], but very little attention has been given to the crystallization/transformation kinetics of ALD HfO_2 and Hf-aluminates. In the study by Zhu *et al*. [38], as-deposited JVD HfO_2 films did not show a clear crystalline peak. Whereas, Kukli *et al*. [37] found that as-deposited ALD HfO_2 films were polycrystalline and consisted mainly of the monoclinic HfO_2 phase. It must be pointed out here that amorphous layers for gate oxides may not be a mandatory requirement since integration of polycrystalline ALD HfO_2 films with poly-Si gate has been reported for MOSFETs with extremely low leakage current densities of $J_G \sim 10^{-7}$ A/cm^2 for an EOT as low as ~ 15 Å by Hergenrother *et al*. [11]. Utilizing polycrystalline materials that have a grain size comparable to or greater than the gate length may serve as a useful approach to selecting suitable high-κ candidates, since such a large grain size may be able to eliminate the variations in the effective electric field experienced by the charge carriers in the channel.

Alloying HfO_2 with Al_2O_3 is a practical approach for retaining an amorphous Hf-based film while maintaining a relatively high dielectric constant of $\kappa \sim 15$ [39]. It is worth noting here, however, that depending on the deposition condition, one can form *mixed* or *nanolaminate* Hf-aluminate films. "Nanolaminate" films refer to a structure consisting of thin-stacked layers of different materials with distinct regions of, for instance, HfO_2 and Al_2O_3. "Mixed" films, on the other hand, *do not* have a well-defined

interface between layers, and can have either uniform or a graded composition across the thickness of the films. In this work, only mixed aluminate films are focused on. Nanolaminate films may have their own advantages [40, 41], but are beyond the scope of this study. Previous studies on Zr-silicate [42, 43] and Hf-silicate [42] films show that for ~50% Zr or Hf cation fraction, crystallization begins at 800ºC to 900ºC. It has also been reported that sputtered $(ZrO_2)_x(Al_2O_3)_{1-x}$ films [44] and JVD $(HfO_2)_x(Al_2O_3)_{1-x}$ films [38] show increased stability of the amorphous phase. It was found that these 1000 Å jet vapor-deposited films with ~31% Al begin to crystallize at 900ºC [38].

A technique for depositing high-κ films that has been gaining attention recently for its excellent uniformity is ALD. As will be discussed later in section 1.2, the morphology of the ALD films depends greatly on the abundance of surface sites that are available for reaction. Reported results [22] show that growing a layer of oxide underneath (known as *underlayer* in this study) prior to depositing the high-κ film is inevitable even though this underlayer undesirably increases the overall EOT of the gate stacks. However, the requirement of this layer is not a drawback of the ALD method, since almost all of the film deposition methods, to date, end up forming interfacial SiO_2 either during high-κ film growth or during subsequent annealing. Therefore, it is desirable that this underlayer oxide be very thin, and yet able to yield overall good electrical performance. Although there are reports in the literature that ALD films grown on SiO_2 are much smoother than those grown on H-terminated Si [22], little attention has been paid to studying the effect of different underlayer oxides (for example, chemical versus thermal oxides) on the growth rate of ALD films and their effect on the electrical performance of the CMOS devices.

While there are still many roadblocks to using HfO_2, Hf-aluminates may be one of the perspective candidates for near-term solution. For long-term solutions, however, HfO_2 is viewed by many researchers as one of the most promising high-κ candidates. Thus, both systems (HfO_2 and Hf-aluminates) were evaluated in this work. This study began by investigating the effect of different surface treatments on the growth behavior of ALD HfO_2 film – this is discussed in chapter 4. In particular, the growth rate of ALD HfO_2 film on both chemical and thermal oxide underlayers was studied. As discussed earlier, inclusions of Al into HfO_2 films do offer higher crystallization temperature, and amorphous high-κ dielectrics such as aluminates are of interest for their potentially better device leakage and reliability. Therefore, a study on thermal stability of HfO_2 films *with* and *without* Al_2O_3 additions was also performed. The literature suggests that besides the amorphous layer, polycrystalline films may also be acceptable as a gate dielectric. Recently, Zhao *et al.* [45] found that the dielectric constant of the HfO_2 film varies dramatically with the crystal phase. Thus, the phase transformation and grain size evolution of crystallized HfO_2 films when they are subjected to thermal annealing used in conventional CMOS processing were also studied. Considering the importance of achieving the maximum mobility and minimum threshold voltage shift, the effect of post-deposition annealing on the amount of fixed charge in the ALD HfO_2 and Hf-aluminate gate stacks was thoroughly investigated in this study. Understanding the effect of annealing is of considerable important since a particularly demanding step in the CMOS process flow is the dopant activation anneal (900ºC – 1050ºC; 10 s). The goal is to minimize both the fixed charge and gate leakage with the minimum tradeoff of increasing EOT.

1.2 Atomic Layer Deposition

1.2.1 Introduction to ALD

It is necessary in the semiconductor manufacturing process to be able to deposit a film with good conformality and step coverage, no pinholes, excellent interface, and precisely controllable thickness. This was the motivation behind developing the deposition technique called atomic layer deposition (ALD). ALD was invented during the late 1970's in Finland by T. Suntola [46], but only since the mid 1990's have researchers become interested in using this technique in the manufacturing of silicon-based microelectronics. This review section provides an introduction to the basic principles of ALD together with its benefits and limitations.

ALD is sometimes referred to as "atomic layer epitaxy" (ALE), when this method is applied to the deposition of epitaxial films. ALD is also sometimes referred to as "Atomic Layer Chemical Vapor Deposition™" (ALCVD™), a trademark of a semiconductor process equipment supplier, ASM International Inc. ALD, however, is the most common name for the technique, and has therefore been adopted in this work.

1.2.2 Principle of Operation

ALD is a surface-controlled thin film deposition process based on alternate saturation surface reactions [47-51]. In ALD, a solid film is deposited on a substrate (for example, a Si wafer) in a *layerwise* manner by exposing the substrate surface alternately to different precursors. This method is very different from the various forms of chemical

vapor deposition (CVD) [52], such as, metalorganic CVD, plasma-enhanced CVD, low-pressure CVD, and atmospheric-pressure CVD.

The basic sequences of ALD [53] are schematically illustrated in Fig. 1.2 using the general example of forming a film of compound AB on a Si substrate. It must be emphasized that Fig. 1.2 is only schematic; the real process is often much more complicated. The reactants, or precursors, used to form this compound can be elements [i.e., A(g) and B(g)] or compounds [i.e., AX_n(g) and BY_m(g), where X_n and Y_m denote ligands]. In the case of compound reactants, ALD starts with the introduction, or "pulsing," of AX_n(g) onto the substrate surface (Fig. 1.2a). Both chemisorption and physisorption will take place. In chemisorption, AX_n reacts with the substrate termination, yielding a by-product and a molecule $AX_{n'}$ that is chemically bonded, through A to the substrate, where n' may be equal to or smaller than n. Precursor molecules that do not chemisorb can still bond to the substrate or chemisorbed-layer by means of physisorption, which involves only weak Van der Waals forces. The extent of the chemisorption process will depend on the abundance of surface sites that are available for reaction. This issue will be addressed in more detail in the next section. After pulsing, excess AX_n(g) (including physisorbed AX_n) is purged from the reaction chamber by an inert gas (for example, N_2; Fig. 1.2b), leaving an $AX_{n'}$(s) monolayer surface. Purging is followed by pulsing the second reactant, BY_m, onto the $AX_{n'}$(s) surface (Fig. 1.2c). Chemisorption and physisorption will again take place. Ideally, all A-X bonds in the $AX_{n'}$ surface layer will be replaced by A-B bonds during pulsing of BY_m. The first ALD cycle then ends with the N_2 purge. Purging will again follow pulsing, leaving this time a $BY_{m'}$ monolayer on the surface. AX_n can then be pulsed again and the process

repeated until the desired film thickness is achieved. It is clear that as long as the pulse times for both reactants are long enough to saturate the available surface sites, ALD is a self-limiting growth process.

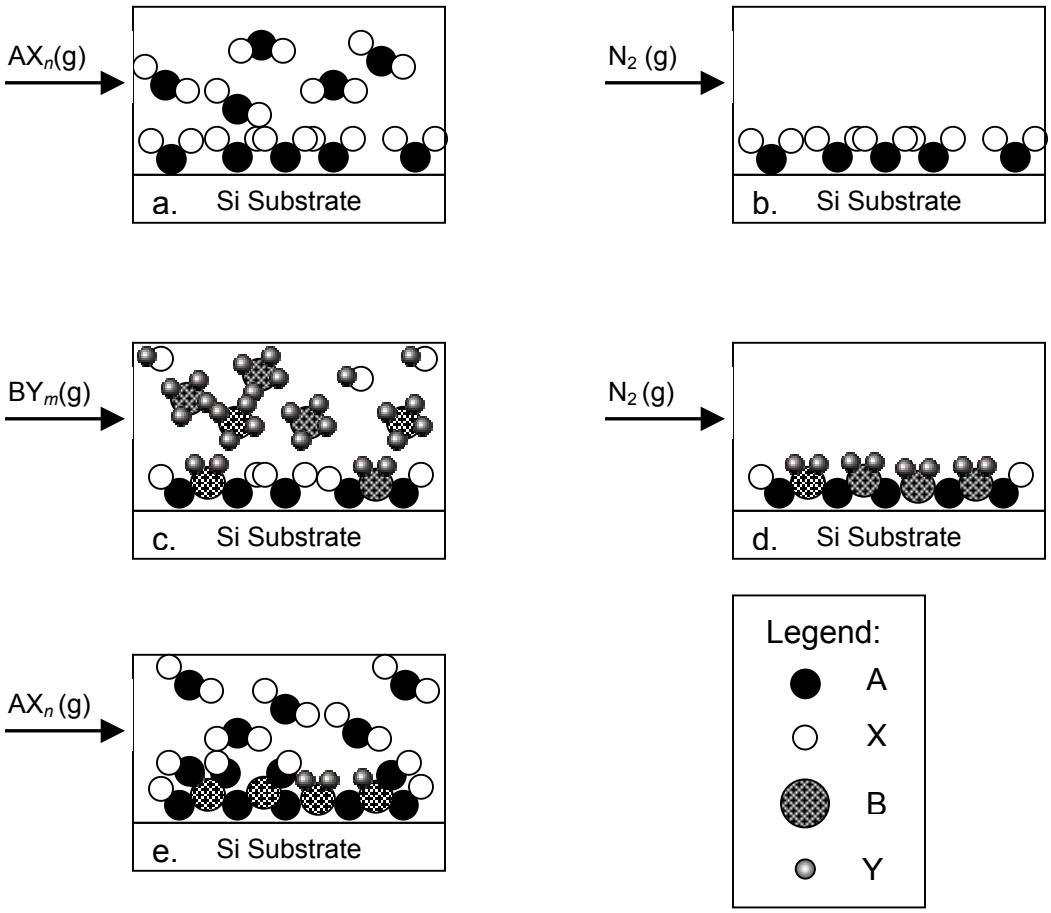

Fig. 1.2 Basic sequence of ALD for compound AB. (a) introduction of reactants $AX_n(g)$ onto the Si substrate surface, (b) purging extra reactants using N_2 gas, (c) introduction of reactants $BY_m(g)$ and react with $AX_n(g)$ to form AB and by-product, X_nY_m, (d) purging extra $BY_m(g)$ and X_nY_m, (e) repetition of the cycle from (a).

In an *ideal* situation, one pulse of reactant will result in one full monolayer [51]. This case is referred to as "a full monolayer per cycle." For some III-V materials, the saturation density has, in fact, been observed to correspond to the bulk density of the material [53]. However, in most of the cases, it is very likely that a given reaction

sequence will result in only a partial monolayer [53, 54], as will be described later in this section.

Mechanisms of HfO_2 films growth by ALD

To date, few theoretical studies of the growth mechanisms related to ALD have appeared in the literature. Esteve *et al.* [55] carried out a density functional theory study of the mechanism of ALD HfO_2 growth on hydroxylated SiO_2. A similar method was used to investigate the mechanisms and details of the initial pathways for ALD growth of Al_2O_3 [56, 57] and ZrO_2 [58]. In the present work, the focus is not on details of the mechanism of HfO_2 growth. The current understanding and presently accepted mechanism [59] of HfO_2 growth chemistry however, will be described here as a background for readers. Note that the discussion here is limited to oxidized Si surfaces where OH-groups are the surface sites since the HfO_2 data in this work involved only growth on hydroxylated Si surface. The results in chapter 4 shows that samples with chemical oxide underlayer results in much better two-dimensional HfO_2 coverage compared to the H-terminated samples. The growth mechanism on H-terminated surfaces is more complicated and not well understood and will not be discussed here. Chemisorption phenomena, as described above in general terms, are currently used for the development of models for ALD reaction mechanisms. In this study, HfO_2 was deposited using $HfCl_4$ and H_2O as precursors. Thus, $HfCl_4$ and H_2O are analogous to the compounds $BY_m(g)$ and $AX_n(g)$ used in the general description. The first cycle of ALD HfO_2 on a SiO_2 surface can be illustrated using two half reactions below:

(a) $\text{-Si-OH*} + HfCl_4 \rightarrow \text{-Si-O-HfCl*}_3 + HCl\ (g)$

(b) $\text{-Si-O-HfCl*}_3 + 3H_2O \rightarrow \text{-Si-O-Hf(OH*)}_3 + 3HCl(g)$

After the first cycle, the sequence of the chemical reactions are as follows:

(c) $-Hf-OH^* + HfCl_4 \rightarrow -Hf-O-HfCl^*_3 + HCl(g)$,

(d) $-Hf-O-HfCl^*_3 + 3H_2O \rightarrow -Hf-O-Hf(OH^*)_3 + 3HCl(g)$

In the first reaction (a), hydroxyl groups are the surface sites (surface sites are denoted by an asterisk). In this reaction, $HfCl_4$ molecules react with the hydroxyl groups, yielding the by-product HCl and leaving chlorinated hafnium atoms chemically bonded, through oxygen, to the substrate. The reaction terminates when no more hydroxyl groups are available for reaction. HCl is cleared away during the following purge step. (Note that the reactions given here are only representative: variations on these reactions are possible. In this first step, for example, other similar reactions, such as $2(Si-OH^*) + HfCl_4 \rightarrow (Si-O-)_2HfCl^*_2 + 2HCl$ (g) can also take place).

In reaction (b), chlorine atoms are the surface sites. Through reaction with H_2O, Cl atoms bonded to Hf are replaced by hydroxyl groups, so that the surface is once again terminated by hydroxyl groups. The reaction terminates when no more Cl atoms are available for reaction. The by-product of this reaction is HCl, which, again, is removed during the following purge step.

In subsequent cycles, as in the first, $HfCl_4$ is introduced to react with surface hydroxyl groups, yielding HCl and leaving chlorinated Hf bonded through oxygen atoms to the surface. H_2O is then introduced and the chlorine atoms terminating the surface are replaced by hydroxyl groups. One can see from the discussion above how repeated cycling of the $HfCl_4$ and H_2O precursors will lead to ALD growth of a HfO_2 film.

Surface sites:

Surface sites are sites on the surface with which the precursor reacts in such a way that the precursor ends up chemically bonded to the substrate. In the mechanism of ALD HfO_2 growth described above, the surface sites are alternately surface hydroxyl groups and surface chlorine atoms. They are the surface sites throughout the growth process. When the 2nd reaction path takes place [reaction (d)], the surface sites thus refer to Cl* group. The type of surface sites does not depend on the type of surfaces, but instead, depends on the type of precursor used. For example, both SiO_2 surface and HfO_2 surface will have the same surface sites (i.e., OH*) after H_2O pulse and Cl* after $HfCl_4$ pulse. The only difference is OH* is bonded to Si on SiO_2 surface, but bonded to Hf on HfO_2 surface.

Non-ideal ALD:

In practice full monolayer per cycle can never be achieve mainly due to two reasons [53, 54]:

(1) Steric hindrance from the chemisorbed precursor ligands. For any given metal precursor pulse, such as $HfCl_4$, steric hindrance from the ligands (e.g., Cl) of each precursor molecule prevent neighboring surface sites from reacting. Thus, the subsequent cycles do not necessarily lead to reaction and coverage at previously unreacted Si-OH sites.

(2) Limited density of surface sites (-OH groups in the case of SiO_2 surface). Thus, even if all available –OH sites are consumed, the density of Hf atoms bound is too low to form a monolayer of HfO_2.

Experimental result [60] has shown that only partial (~14%) monolayer growth per cycle is observed when HfO_2 is deposited on chemical oxide. Thus, ALD growth does not occur via a monolayer-by-monolayer mode in real situation as not every nucleation site will be utilized due to the two reasons above. Even though each half-reaction path shown in pages 17 – 18 is assumed to proceed to saturation, the saturation coverage of HfO_2 after a given cycle will be a submonolayer. More details on the growth behavior of ALD HfO_2 will be discussed in chapter 4.

1.2.3 ALD Processing Requirements

In designing a successful ALD process, the following factors must be considered: (1) the choice of proper precursors, (2) the reaction temperature, (3) pulse/purge times, and (4) the surface preparation prior to the ALD process.

The precursors can be gaseous, liquid, or solid [51, 53, 61]. Where a liquid or solid source is used, the requirements are that they must be volatile and the vapor pressure must be high enough for effective mass transportation. In contrast to the requirements for reactants in other CVD processes, reactants in ALD should react aggressively with each other. The precursors must react to form the desired stable and nonvolatile solid film, but the by-products formed should be unreactive, volatile, and easily purged from the reactor. Obviously, the precursors should also not decompose at the ALD processing temperature.

To achieve a self-limiting growth condition, the substrate must be heated to a sufficiently high temperature such that only the chemisorbed layer remains attached to

the substrate, while the atoms and molecules in excess of this layer (bonded weakly to the surface through physisorption) re-evaporate from the surface and are removed with the inert gas purge [51, 62]. The temperature range for surface sites saturation is specific to the precursor and surface involved [54, 63-65]. In the ALD process, the deposition temperature is relatively low (~ 300°C) compared to other CVD processes, which operate at about 500°C – 700°C [52].

From the productivity point of view, the pulse time should be kept to a minimum [51, 66]. However, it must be long enough to achieve full saturation of the surface sites. Insufficient precursor doses will generally result in a marked film thickness non-uniformity, where the regions of the substrate closest to the precursor inlet will be uniformly covered but the opposite part of the substrate will either be a much thinner film or not covered at all. The purging time does not have a marked effect on the growth rate, but should be sufficiently long to remove excess precursors and volatile by-products. Any residual left in the reactor after incomplete purging will cause gas phase reactions (i.e., CVD type of growth), which will contribute to additional film growth at the leading edge of the wafer (the regions of the wafer closest to the precursor inlet).

In the ALD process, the film growth rate is approximately proportional to the number of surface sites on the surface since only chemisorbed precursors contribute to film growth. For this reason, the availability of bonding sites for the reaction of the precursors in the *first* cycle is of particular importance [54, 61]. The type, character, and density of the bonding sites on the substrate often strongly depend on the type of substrate surface treatments prior to the ALD process.

1.2.4 Summary of Advantages and Limitations

The property and quality of a high-κ dielectric film depend on the method by which the film was deposited. High-κ dielectric films have been previously deposited by methods such as ion beam assisted deposition [35], metalorganic CVD [68], JVD [38], and ion beam sputtering [69]. None of these methods, however, is able to produce a uniform coating and satisfactory conformality for film deposition. Poor step coverage often results from the CVD process due to gas phase reactions, especially for high aspect ratio features such as the vertical gate transistor structure. In ALD, on the other hand, sequential pulsing of the precursors automatically eliminates the gas phase reactions that lead to this film non-uniformity. ALD, by its very nature, yields excellent step coverage with good thickness uniformity, even on very non-planar surfaces; and it is able to produce films with very low pinhole density.

Another advantage of the ALD process is the inherent control of growth rate and thickness. Since this method utilizes the principle of sequential growth, the thickness of the film can be predicted easily by multiplying the constant growth rate (Å/cycle) of the film by the number of cycles being pulsed. This is generally true assuming no incubation period occurs during growth.

Other benefits that have been gained by making use of the unique characteristics of the ALD can be briefly described as follows. Since the ALD growth proceeds one monolayer at a time, it has the ability to produce multilayer structures of different materials (also known as *nanolaminates*) [40, 41] and to produce complex compounds with good stoichiometry control. Because ALD utilizes self-limiting growth mechanisms, it is less susceptible to small variations in precursor fluxes. Therefore, solid

precursors are more easily adapted to ALD than to other deposition methods, such as CVD.

The major limitation of ALD is its slowness: only one monolayer of the film is deposited during one cycle, even in an ideal case. However, the dielectric film thicknesses have now shrunk down to a level where the low growth rate of ALD is losing its significance when weighed against the potential benefits.

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1.3 Thesis Outline

In this chapter, a review of the challenges and the general requirements associated with the possible candidates to replace conventional SiO_2 as the gate dielectric was provided. The basic operating principles of ALD were also presented. Many advanced analytical techniques, which were used for physical characterization, are covered in chapter 2. Chapter 3 outlines the experimental methodology used in preparing the samples for both physical and electrical analysis, together with the experimental setup for each characterization technique used in this work. Three separate chapters were devoted to present the results and discussions of this work. Chapter 4 presents the results on the growth behavior of the ALD HfO_2 films on various underlayers. The results of physical and electrical analysis on ALD HfO_2 and Hf-aluminate films are discussed separately in two subsequent chapters. In the final chapter, an overall summary and conclusions to this work are drawn. Appendices at the end of this thesis contain compilations of relevant data.

CHAPTER 2: CHARACTERIZATION TECHNIQUES

Many techniques were employed during this research to investigate the physical and electrical properties of both HfO_2 and Hf-aluminate films. The techniques involved in physical characterization include: XRD, MEIS, TEM, and ellipsometry. In order to aid readers in analyzing the data presented in this thesis, basic information regarding these techniques is presented in sections 2.1 to 2.4. Background information regarding the electrical characterization is presented in section 2.5.

2.1 X-ray Diffraction

In this study, x-ray diffraction (XRD) was used to monitor the degree of crystallization/transformation and the grain size evolution of the atomic layer deposited films. The principles of XRD are well documented in the literature, thus only a brief description is presented in this section. XRD is a non-destructive analytical technique that can be used to provide information such as crystal structure, degree of crystallinity/transformation, composition, and grain size [1-5]. Diffraction will occur when the *Bragg Equation* below is satisfied.

$$2d \sin \theta = \eta\lambda, \tag{2.1}$$

where λ is the wavelength of the incident x-ray beam, η is an integer called the *order of reflection*, and θ is the angle of incidence corresponding to the construction of the

diffraction peak (also known as Bragg angle). Since *d* is a function of the lattice parameter, and the diffracted intensity of peaks depends on the distribution of atoms within the crystal structure, an XRD pattern is specific to a given phase. An amorphous phase will not produce a diffraction pattern; thus, XRD is a useful method to detect a phase transition from an amorphous to a crystalline structure.

For a given sample, all x-ray beams diffracted from a family of planes with spacing *d* will lie on a single cone, which has its apex in the diffracting volume of the sample, which has its axis along the direction of the incoming x-ray beam, and which intersects its axis at an angle of 2θ. When the sample is polycrystalline with a large number of randomly oriented grains, x-rays diffracted from that family of planes will cover the cone completely. When the number of grains is smaller or when texture is present, the diffracted x-ray beams will lie on the cone distinct and separate from each other. In the latter case, the diffraction data out of the diffractometer plane are not detected by a conventional XRD system; thus, the material structure represented by the missing diffraction data will either be ignored, or extra sample rotation is needed to complete the measurements.

In this work, a high-sensitivity XRD system equipped with a two-dimensional (2D) detector [6] was used, which enables the user to detect diffracted beams that might have been missed in a conventional system. In addition, a 2D-detector provides a speed of data collection that can be 10^4 times faster than that of a conventional point detector.

2.1.1 Grain Size

XRD provides a simple method to measure the grain size in a polycrystalline film, based on the Scherrer's equation [5]. This equation shows an inverse relationship between grain size and diffracted peak profile width: the wider the peak, the smaller the crystallites. However, besides the contribution from grain size, peak broadening may also be due to instrumental broadening and microstrain. Only peak broadening due to grain size should be considered in the grain size calculation. The details of grain size calculation, including ways to correct for instrument broadening in order to estimate the ALD HfO_2 grain size, will be described later in section 3.3.1.

2.2 Medium Energy Ion Scattering

In this study, medium energy ion scattering (MEIS) was used to determine the composition of the ALD Hf-aluminate films. MEIS is, in principle, very similar to the common characterization technique, Rutherford backscattering spectrometry (RBS). MEIS [7, 8] is a powerful technique that provides structural and compositional information with a better depth resolution than that of RBS. In MEIS, a sample is bombarded with light ions (usually H^+ or He^+) and information is obtained by measuring the energy and direction of the *backscattered* ions. Compared to conventional RBS, where the incident beam usually has an amount of energy in the MeV range, MEIS uses a lower-energy beam usually in the range of 50-400 keV [7].

The interaction of a beam of incident ions with atoms in a target material can be divided into four categories, depending on the incident ion energy [9]:

- elastic atomic collisions
- inelastic atomic collisions with atomic excitation
- elastic nuclear collisions
- inelastic nuclear collisions with nuclear excitation

MEIS falls within the regime of inelastic atomic collisions and elastic nuclear collisions. When an ion of energy, E_o, enters a sample, it continuously loses energy due to inelastic atomic collisions until it experiences a scattering event with one of the atomic nuclei (elastic nuclear collisions). If the ion energy prior to nuclear collision is E_1, the energy after, E_2, is given by the equation 2.2, where E_3 is the energy of the ion leaving the sample surface.

$$E_1K = \left[\frac{\sqrt{M_2^2 - M_1^2 \sin^2 \theta_M} + M_1 \cos \theta_M}{M_1 + M_2} \right]^2 = E_2 \qquad (2.2)$$

In this equation, M_1 and M_2 are the mass of the incident ion beam and target atom, respectively. The angle, θ_M, is the angle through which the incident ion is scattered with respect to the incident beam angle. The ratio of incident ion energy after the elastic collision to that before the collision is called the *kinematic factor* K (tabulations of K exist for the H^+ projectile scattered at various angles θ_M). Those ions not scattered elastically are not detected. Multiple elastic scattering events are too improbable to influence the results.

In MEIS, the detector is placed at a fixed angle and records the number and energies of the ions that enter it. In a plot of backscattered ion counts versus

backscattered ion energy, the peak corresponding to elastic collisions from a given element of mass M_2 in a thin film begins at an energy E_1K and continues to a lower energy which depends on the film thickness. The positions and widths of the peaks in an MEIS spectrum thus provide information regarding the components and thickness of a film, respectively. The areas under the peaks correspond to the concentration of elements. Computer simulation program exits that use the tabulated stopping power, can be used to provide the structure and composition information. The stopping power of a material for a particular ion is defined as the energy loss per distance traveled in the material, expressed in eV/Å. The tabulated stopping value for H^+ projectile energy at 100 keV in Hf target, for example, is of the order 40 eV/Å [8].

2.2.1 Channeling and Blocking

Channeling is an effect obtained by steering the incident beam into channels between planes of atoms in a substrate (i.e., aligning the beam such that it is parallel to a symmetry direction of the crystal; see Fig. 2.1) [10]. In channeling, as in non-channeling, some ions impinging on the sample scatter elastically from the surface. In channeling, however, those ions entering the sample travel far into the bulk and do not generally make it to the detector. Thus, in the case of channeling, the backscattered ion signal from the bulk is much reduced. In this work, ions were channeled into the Si substrate in order to reduce the substrate contribution to the MEIS spectra. This resulted in improved sensitivity of light elements (such as Al and O) peaks from the film, which often superimposed with the Si peak.

If a backscattering atom is located beneath the surface layer, the backscattered projectile may be blocked by another atom on its way out. This phenomena is known as *blocking* [10, 11] and is illustrated in Fig. 2.1. The blocking effect causes the Si peak to show a pattern of so-called blocking dips in an angular or blocking spectrum (a plot of ions yield versus a scattering angle). It is worth noting that besides channeling, blocking can also further reduce the background Si signal. In this study, blocking was used for calibration purposes to correlate the angle in the detector with the real scattering angle (since the blocking dip marks angles where backscattered ions are prevented from re-emerging into the vacuum), and to further reduce the Si background signal.

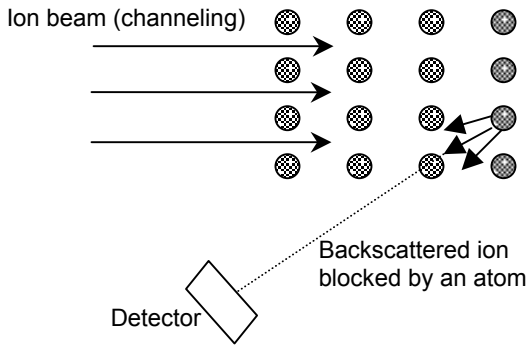

Fig. 2.1 Schematic illustration showing the channeling and blocking phenomena. Note that the incident beam is aligned with a crystal symmetry direction and the ion backscattered from one atom in the sample blocked by another atom results from the position of the detector.

With this simple concept of channeling and blocking in mind, one can imagine that channeling (thus, a blocking dip in the angular spectrum) will certainly occur for a crystalline sample (provided there is proper alignment between the incident beam and target), whereas for an amorphous sample, the normalized backscattered yield essentially equal ~ 1 (no angular dependence). Therefore, observing the angular spectrum gives a

direct indication of the degree of crystalline order in the film. This method is certainly not as sensitive as XRD (section 2.1), but MEIS depth profiling analysis relies on the film being amorphous or polycrystalline. It is important to note here that channeling in the film of interest must be avoided in order to obtain an accurate thickness of the film. The absence of any angular dependence in Hf for instance, verifies this assumption for depth profiling of HfO_2, as will be discussed later in section 5.2.

2.2.2 Advantages and Limitations

As mentioned at the beginning of this section, RBS, which uses ion beam energies in the MeV range, is the most commonly used ion scattering technique. This technique is convenient; however, it does not provide the mass resolution, sensitivity, or depth resolution required in some cases. MEIS, with a similar operating principle, utilizes a lower-energy (keV range) ion beam. Whereas high-energy ions can penetrate the order of microns into a solid, medium energy ions are more likely to scatter from the surface and therefore are of considerable use in surface analysis. Also, higher stopping power results from the lower ion energy, and this translates into improved depth resolution. The lower-energy ion beam used for MEIS results in a lower level of target heating as well as a higher scattering cross section, thus permitting use of a higher beam current and lower total analysis doses. However, if the ion energy is too low, then multiple scattering and resonant neutralization effects make quantification difficult.

As with many techniques, the sensitivity of MEIS is limited by background levels. Thus, MEIS is relatively insensitive to light target constituents such as oxygen in the presence of heavier target constituents. The angular range collected by the MEIS

detector is 22º. For a ~ 100 keV beam, the energy window is about 2 keV. The total system angular resolution is given as ~ 0.1º, while the total system instrumental energy resolution is approximately 110 eV (estimated from the full width at half maximum of a signal of an element with submonolayer coverage on a flat surface). With this energy resolution, depth resolution for an amorphous thin film is ~ 4 Å.

2.3 Transmission Electron Microscopy

In this study, transmission electron microscopy (TEM) and scanning-TEM (STEM) were used to provide information on crystallinity and the film thickness. TEM is a well-documented [7, 12-16] characterization technique familiar to scientists in a wide range of fields. It will therefore not be discussed here. STEM, however, is relatively less common and will be discussed briefly.

The basic principle of image formation in the STEM mode [12] is different from that for a static-beam TEM image. In STEM, a convergent beam (instead of the parallel beam used in TEM) is rastered across the sample. In TEM, an *aperture* is used to select direct or scattered electron beams to form a bright field (BF) or a dark field (DF) image, respectively. In STEM, a *detector* is used instead of an aperture. DF TEM images are formed by using the aperture to block all but a small fraction of scattered/diffracted electrons, whereas STEM images are formed by collecting most of the scattered electrons on the annular DF (ADF) detector. Therefore, STEM is particularly useful to form an image of samples with amorphous phases, which scatter electrons into a diffused ring in

the dark field mode, since the collection angle of the ADF can be adjusted so that the ring of scattered electrons falls on the ADF. For this reason, a TEM DF image shows a poorer contrast and is noisier than a STEM ADF image. In this work, ADF STEM was used to form an image of one of the amorphous film samples.

2.4 Ellipsometry

In this study, ellipsometry [17-22] was used to measure film thickness, termed *ellipsometry thickness*. A basic ellipsometer configuration consists of a light source, a polarizer (which can vary the angle in order to vary the polarization state of the incoming light), and an analyzer and detector to measure the changes in the polarization state after reflection. The light beam is first linearly polarized by the polarizer, and the polarized light can be resolved into two components: one oscillating perpendicular (s), and one oscillating parallel (p) to the plane of incidence. When a *plane* polarized light beam reflects from a sample, the two components experience different amplitudes and phase shifts, and thus the beam becomes *elliptically* polarized. If the sample has multiple reflecting surfaces, the various reflected photons will interact, yielding maxima and minima in the *reflectance* (the ratio of the reflected and incident light intensity) as a function of wavelength or incident angle. The two components of the reflection coefficient, R'_s and R'_p, are not separately measurable. However, the complex reflection

$$\frac{R'_p}{R'_s} = \tan\psi e^{i\Delta} \tag{2.3}$$

ratio (equation 2.3) can be determined from the ellipsometric angles, ψ and Δ, which are measurable. The parameter Δ is the phase shift, which is induced by the reflection. Both parameters ψ and Δ can be determined using null ellipsometry [2], which is not discussed here. Upon obtaining the values ψ and Δ, the optical parameters, extinction coefficient (*k*) and index of refraction (*n*) can be calculated using Fresnel's equations [2]. By using these *n* and *k* values, together with the wavelength at maxima reflectance, one can calculate the thickness, *t,* of the films using equations in the literature [2]. Even for a simple structure such as a thin film/substrate system, the equations that need to be solved become very complicated. The equations are best solved by using numerical techniques, as is commonly done in computer-controlled ellipsometers.

There is, in principle, no limit to the thickness of the layer that can be determined. However, for very thin films, the ability to determine both *n and k* is affected by the wavelength used [22]. The conventional single wavelength ellipsometer is limited to measuring the thickness and optical constant of simple, relatively thick structures as it uses a fixed wavelength of 632.8 nm. The spectroscopic ellipsometer (SE), on the other hand, provides more flexibility and degrees of freedom because it has the capability to vary not only the wavelength, but also the angle of incidence. It should be noted that sample preparation, contamination, oxidation, and surface roughness may induce some error in the measurements. Even for the simplest case of a substrate with cubic symmetry (optically isotropic), the surface can be reconstructed and rough. Therefore, cares must be taken during sample handling in order to obtain accurate and reproducible data.

2.5 *C–V* and *I–V* Measurements

2.5.1 The MOS Capacitor

The MOS capacitor (MOS-C) was used in this research as the test structure for studying electrical properties. The MOS-C can be manufactured in parallel with the MOSFET in production, thus the electrical properties obtained from a MOS-C are representative of those of a full MOS system. The MOS-C structure has the advantages over the MOSFET test structure of simple configuration (inset of Fig. 2.2a), simple fabrication, and simplicity of analysis. Even though the MOS-C cannot be used to measure properties such as threshold voltage, channel mobility, and channel leakage current [23], in which a MOSFET structure is necessary, it is adequate to study the oxide charges in the gate oxide, which is one of the main factors influencing the threshold voltage instabilities and channel mobility degradation.

In the study, the MOS capacitor was fabricated using the same processing (section 3.2.2) as found in actual CMOS processing. Capacitance-voltage (*C–V*) and leakage current-voltage (*I–V*) measurements obtained from the MOS-C were used to extract information such as flatband voltage (hence, flatband shift), fixed charge, and EOT.

2.5.2 Understanding *C–V* Curves, the Energy Band Diagram, and Flatband Shift

The theory of MOSFETs [23-27] has been adequately described in the literature. This section, therefore, focuses only on the background relevant to this work. In this study, flatband voltage, V_{FB} (and hence, fixed charge concentration), and EOT were extracted from the *C–V* measurements of MOS-C. A typical high frequency *C–V* curve

from a *p*-type MOS-C is displayed in Fig. 2.2a. Note that the *C–V* curve shape from an *n*-type MOS-C (in which the majority carriers are electrons) is a mirror image of the *p*-type MOS-C (in which the majority carriers are holes). The MOS-C can be represented by the simple equivalent circuit shown in the inset of Fig. 2.2a. The capacitance of the silicon, C_s, is shown as a variable capacitor in this figure because it is bias dependent. The total capacitance C across the contacts can be expressed as the series combination of the silicon capacitance C_s and oxide capacitance C_{ox}, as described by the following equation:

$$\frac{1}{C} = \frac{1}{C_s} + \frac{1}{C_{ox}}. \tag{2.4}$$

The operation of an ideal MOS-C can be divided into three regimes: *accumulation*, *depletion*, and *inversion*, which are illustrated in Fig. 2.2. Figures 2.2 (b) to (e) schematically illustrate the energy band diagrams corresponding to each gate voltage, V_G biasing conditions. It is important to note that these figures correspond to an *ideal p*-type MOS-C in which the following assumptions hold: (1) the work-function difference, Φ_{ms}, between the gate and the semiconductor is zero and (2) there are no charges within the oxide or at its interfaces (i.e., the oxide is defect-free). For this ideal case, the flatband condition (Fig. 2.2c) occurs at $V_G = 0$ (also called the *flatband voltage*, V_{FB}), where the E_{Fn} coincides with the E_{Fp}, and thus the band is flat. E_{Fn} and E_{Fp} are the Fermi levels of the *n*-type and the *p*-type Si, respectively. The form of the high frequency *C–V* curve can be explained as follows. For a *p*-type MOS-C, *accumulation* is observed when negative V_G is applied to the gate. This negative polarity attracts the majority carriers (holes in this case) towards the gate, where they accumulate at the oxide/substrate interface. At a sufficiently

negative V_G, the hole density, N_A, at the silicon surface will exceed the hole density in the bulk. This leads to a condition where $C_s \gg C_{ox}$, and therefore the total capacitance $C \approx C_{ox}$. As V_G becomes more positive, holes are less strongly attracted to the silicon surface, which results in the formation of a *depletion* layer. In the case of high frequency, minority carrier

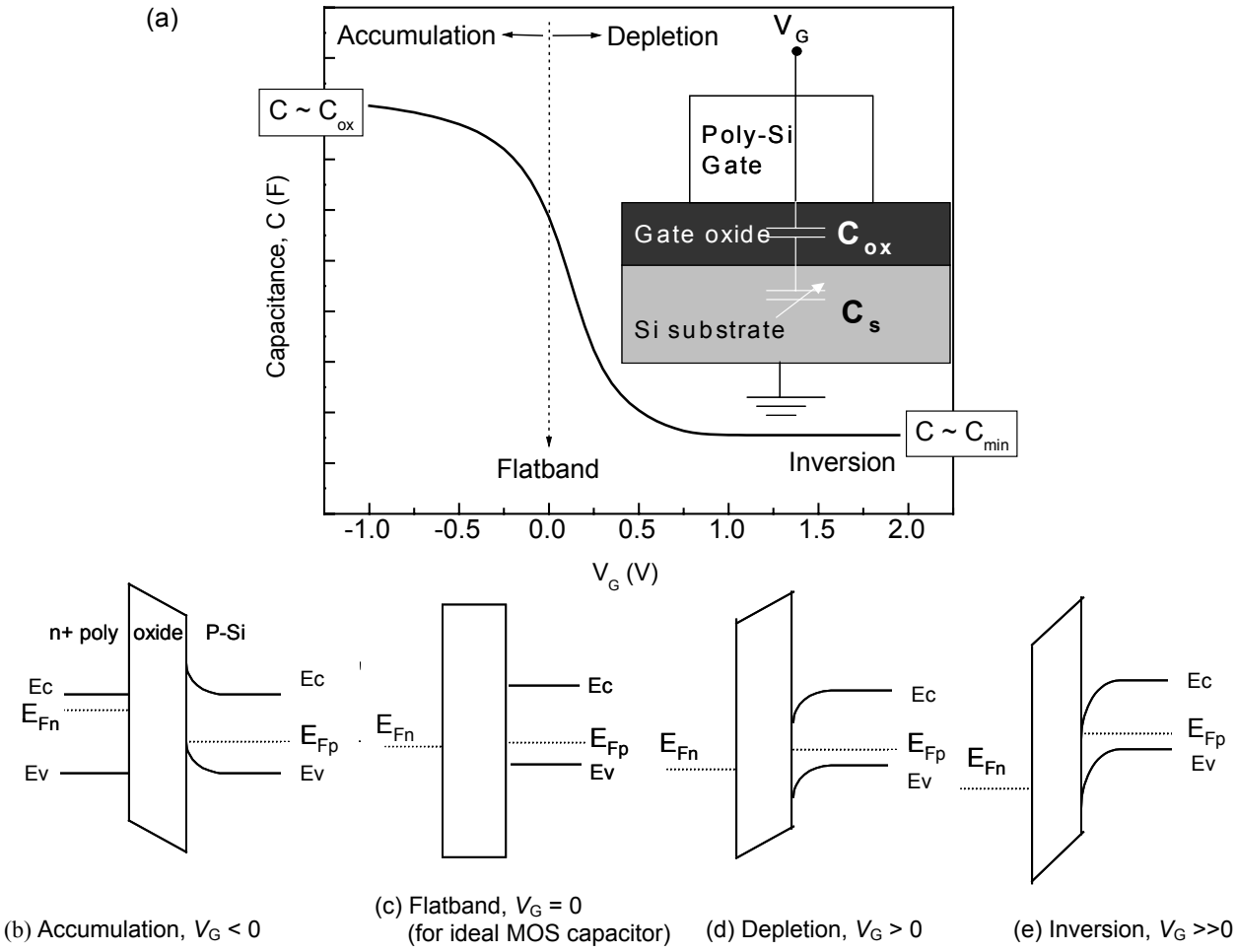

Fig. 2.2 (a) A typical high frequency *C–V* curve for a *p*-type MOS capacitor. The inset shows the basic MOS capacitor structure together with the equivalent circuit associated with it. Energy band diagram for ideal MOS capacitors for: (b) accumulation; (c) flatband; (d) depletion; and (e) inversion. E_v and E_c are energies at the valence and conduction band edges, respectively. E_{Fp} is the Fermi level of the *p*-type Si.

generation is not able to follow the rapidly varying AC voltage, and thus does not contribute to capacitance. Instead, to maintain charge neutrality, the majority carriers flow in and out across the boundary between the depletion layer and the bulk silicon. In this case, C_s is given by C_D, the capacitance of the depletion layer. The total capacitance, C, measured at high frequency is therefore C_D in series with C_{ox}. As V_G continues to increase, the depletion layer width increases, which results in a decrease in C_D and a corresponding decrease in C. Eventually the depletion layer reaches a maximum width; and this situation is referred to as *inversion*. C_D at this point is at its minimum and therefore so is C (i.e., $C \equiv C_{min}$).

Flatband shift: For a real MOS-C, Φ_{ms} depends on the substrate doping density and the gate electrode material, and is therefore rarely equal to zero. As a consequence, the voltage V_{FB} must be applied to attain the flatband condition. If no charges are present within or at the interfaces of the gate oxide, V_{FB} will equal Φ_{ms}. In a practical situation, however, charges are likely to exist and will alter the *C–V* curve position so that $V_{FB} \neq \Phi_{ms}$. The charges are classified with respect to their location and action as follows [24]: mobile ionic charge (Q_m), bulk oxide charge (Q_{ox}), interface state charge (Q_{it}), and fixed charge (Q_f),. Q_m (mobile ionic charge) arises mostly from the presence of sodium or potassium ions, which have very high diffusivities in the oxide. The presence of these ions causes instabilities in threshold voltage, but Q_m can be neglected because it can be (and was, in this work) minimized by scrupulous care and cleanliness in the present-day fabrication technology.

The oxide trap charge Q_{ot} arises from holes or electrons trapped in the *bulk* of oxide, and can be positive or negative. The trap sites, which are distributed inside the

bulk oxide captured (or emit) the charges introduced into the oxide film by ionizing radiation or high currents through the oxide. Low-temperature treatments (450 - 550ºC) has been implemented in modern MOS fabrication process (also in this work) as a standard step to minimize Q_{ot}, thus Q_{ot} has been considered relatively insignificant in modern MOS devices.

Interface states charge arises from allowed energy states (also referred to as interface states or interface traps) that exist within the bandgap of the Si in the region very close to the Si/oxide interface. These interfacial traps can either capture (or emit) hole or electron and the charge per unit area stored in the traps is symbolized by Q_{it}. Although models that detail the electrical behavior of the interfacial traps exist, the physical origin of the traps has not been totally clarified. The weight of experimental evidence, however, supports the view that the interfacial traps primarily arise due to imperfections (e.g. Si dangling bonds or oxygen dangling bonds) near the Si/oxide interface where the chemical composition is considered to be non-stoichiometric [24, 27, 28]. Other possible interfacial trap-formation effects include Si-Si bond stretching, Si-O bond stretching, and the presence of a metallic impurity at the Si surface. The presence of Q_{it} will caused frequency dispersion, especially in the depletion region of the *C–V* curves. In this study, negligible frequency dispersion was observed in the *C–V* curves, and this will be discussed further in Chapter 6.

For reasons given above, any shifts of the *C–V* curves were assumed, reasonably, to be mainly attributed to Q_f. Fixed charge Q_f refers to charges residing within the oxide or near to oxide interface, and will cause a translational shift in the *C–V* curve in either a positive or negative direction and the amount of this shift in the *C–V* curve is called the

flatband voltage shift, ΔV_{FB}. This ΔV_{FB} depends not only on the amount of charges in the film, but also on the distance, *w*, between the centroid of the charge distribution and the *gate electrode/oxide* interface. For a fixed amount of charge, ΔV_{FB} will increase with increasing *w*. Therefore, ΔV_{FB} is equal to zero if the centroid of the charge is located *at* the gate/oxide interface. By observing the direction of the *C–V* curve shift relative to the ideal or theoretical *C–V* curve, the polarity of the oxide charges can be determined. There are many hypotheses regarding the physical origin of Q_f. Although doping impurities from the semiconductor diffuse into the oxide during the high temperature oxidation process, Q_f has noted to be independent of the semiconductor doping concentration and doping type [28]. The existence of ionized doping impurities within the oxide can therefore be eliminated as a possible source of Q_f. One hypothesis is that Q_f is due to excess ionic silicon that broke away from the silicon proper and was waiting to react in the vicinity of the Si/oxide interface at the time that the oxidation process is abruptly terminated [28]. Note that unreacted Si bonds could also lead to interface state charge, Q_{it} if the energy level is *within* the Si gap. Regardless of the origin, it has been experimentally confirmed that the magnitude of Q_f is influenced by substrate orientation, oxidation temperature and anneal conditions after oxide growth [27]. Since Q_f is directly related to the oxidation process, it is reasonable to expect that Q_f may exist in the HfO_2 layer as well besides in the SiO_2 layer (known as underlayer in this work). Indeed, the existence of Q_f in the HfO_2 layer has been seen by many research groups [29 – 31].

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CHAPTER 3: EXPERIMENTAL PROCEDURE

This chapter outlines the experimental methodologies and setups used for the physical and electrical characterization performed in this work. Section 3.1 describes the parameters that were used during the ALD deposition. Optimizing these deposition parameters was necessary in order to ensure that the films grew in a layer-by-layer mode with good thickness uniformity and film coverage. The optimized parameters presented in the first section were not system specific and therefore could serve as starting values for deposition using a similar tool. In this study, *blanket wafers* were used in the physical characterization, while *device wafers*, each containing multiple MOS capacitors, were used in the characterization of electrical properties of the dielectric films. The fabrication procedure for both types of samples will be discussed in section 3.2. Section 3.3 outlines the details of the experimental setup used in each characterization technique of this research.

3.1 ALD Setup

3.1.1 ALD Reactor

ALD in this experiment was performed in a fully automatic, flow-type reactor with the trade name ASM Pulsar 2000™ module. In this subsection, the basic layout and operating principles of this reactor are briefly discussed.

The layout of this tool is shown in Fig. 3.1. The ALCVD™ module shown in this figure is equipped with a loadlock to maximize the throughput during wafer processing. The ALD process starts with a robot arm transferring a wafer from the loadlock to the reaction chamber. Simultaneously, the bottom plate, which has been pre-heated to 300°C in the reaction chamber, will move down, preparing to receive a wafer from the robot

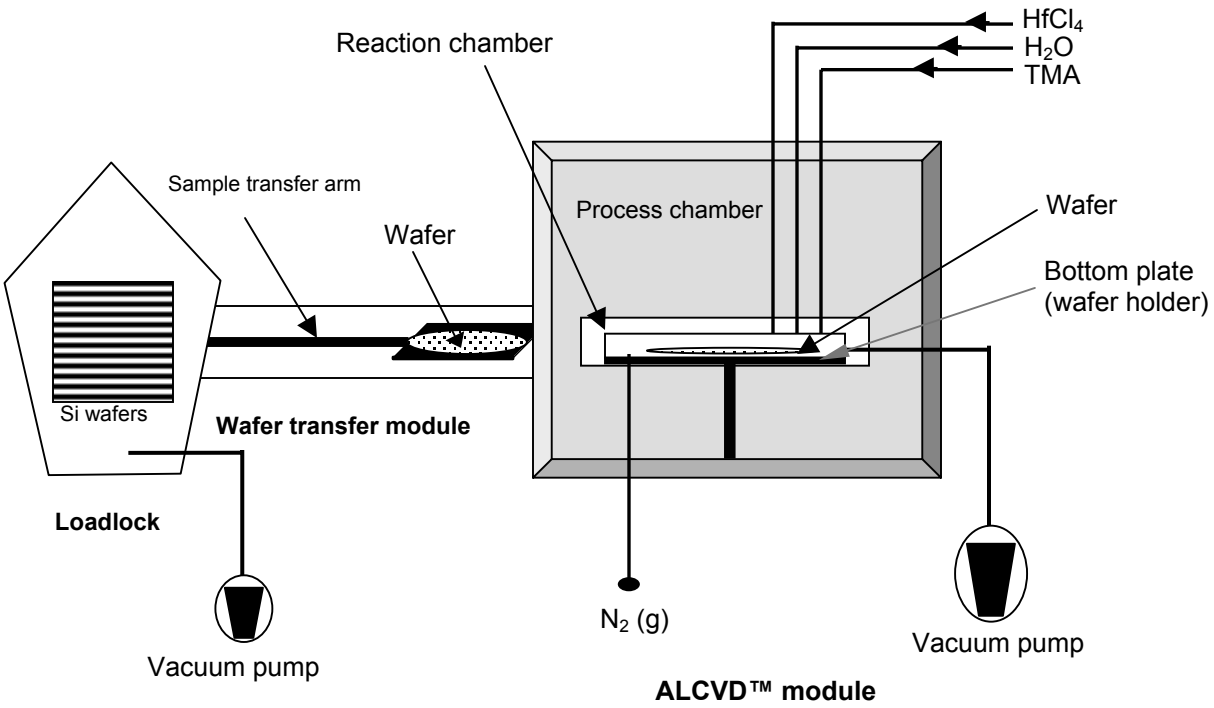

Fig. 3.1 Layout of the loadlock, wafer transfer module, and ALD chamber. Several other components are also shown.

arm. The pulsing of each precursor is controlled using pneumatic valves. It is very desirable in semiconductor manufacturing that the wafer has minimum exposure to the atmosphere in order to avoid further growing of native oxide and to prevent particle contamination. The loadlock, which can be pumped down to a pressure of 10^{-2} Torr, is, therefore, important for the temporary wafer storage place (storage capacity = 25 wafers) as well as for increasing productivity. The base pressure of the process chamber is about 10^{-3} Torr.

3.1.2 ALD Parameters

Table 3.1 lists all the important ALD process parameters as well as the optimized values used to deposit all films in this work. The optimized values were obtained by varying one parameter at a time until films with very smooth surface morphology

Table 3.1 Compilation of several important parameters used in this work for ALD deposition of HfO_2 and Al_2O_3 films. H_2O vapor served as the oxygen source for both cases and is the first precursor. The second precursor is the corresponding metal precursor.

Parameters	HfO_2 deposition	Al_2O_3 deposition
First precursor		
a) Precursor source temperature (ºC)	18ºC	18ºC
b) Precursor pulse time (msec)	300 msec	600 msec
c) Presursor purge time (msec)	2500 msec	2400 msec
Second precursor		
a) Precursor source temperature (ºC)	200ºC	18ºC
b) Precursor pulse time (msec)	100 msec	100 msec
c) Presursor purge time (msec)	3500 msec	400 msec
Purge/carrier gas (N_2) flow rate	800 sccm	
Pre-stabilization time	60 sec	
Post-stabilization time	60 sec	
Substrate Temperature (ºC)	300ºC	
Working Pressure (Torr)	1.5	

resulted. In this study, ellipsometry thickness across the 200 mm wafers varies less than 5 Å for a nominal film thickness of 50 Å. In all cases, ALD deposition was carried out such that the first pulse of the ALD cycle was the H_2O pulse.

In this work, substrates were held at 300ºC during deposition. N_2 gas (~ 800 sccm) was used as both carrier and purge gas. The working pressure during deposition was about 1.5 Torr. The HfO_2 films were grown by alternating pulses of hafnium tetrachloride ($HfCl_4$) and H_2O. Hf-aluminate films were grown by occasionally substituting $Al(CH_3)_3$ (also known as trimethylaluminium, TMA) pulses for $HfCl_4$ pulses. At moderate temperatures, $HfCl_4$ is a solid. To obtain an acceptable vapor pressure, the $HfCl_4$ source was heated to 200ºC during deposition. H_2O and TMA were held at 18ºC during growth, at which they are both liquid. As mentioned earlier, the bottom plate in the chamber had already been pre-heated to 300ºC prior to wafer loading. After the substrate was securely placed on top of this pre-heated plate, the N_2 gas was allowed to flow for 60 s before starting the sequential pulsing. This is known as pre-stabilization time, which allows pressures, flows, and temperatures to stabilize. The post-stabilization time is the delay time before unloading the wafer to purge all the excess reactants and by-products from the vacuum chamber.

In the ALD process, as noted in section 1.2.3, the quality and the uniformity of a film depend critically on the precursors' pulse and purge times. To have a better understanding of the terms "pulse" and "purge," consider the example of growing HfO_2. As shown in Fig. 3.2, deposition starts with a H_2O pulse for s_1 seconds, which is followed by s_2 seconds of N_2 purge to remove the excess water vapor. Ideally, after the first pulse and purge, the substrate is OH-terminated. After the first purge, $HfCl_4$ is pulsed for

100 msec. Hf will bond to oxygen in the OH-termination and yield HCl as a by-product of the bonding, leaving the surface Cl-terminated. The $HfCl_4$ pulse is followed by a 3500 msec purge to remove HCl and excess $HfCl_4$. Water is then pulsed again, reacting with the Cl-termination, yielding HCl, and leaving OH-termination. The process is repeated as desired. One sequence of "*H_2O pulse – N_2 purge – $HfCl_4$ pulse – N_2 purge*" is referred to as one ALD cycle.

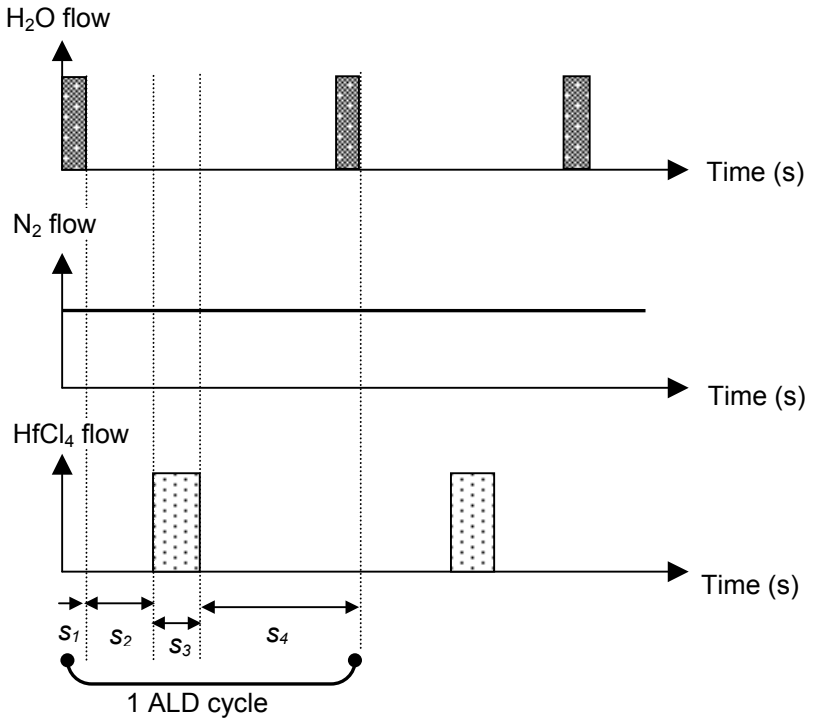

Fig. 3.2 Definition of pulse and purge sequences. s_1 to s_4 represent the time used for H_2O pulse, N_2 purge, $HfCl_4$ pulse and N_2 purge, respectively.

3.2 Sample Preparation

3.2.1 Blanket Wafers

In this study, the phrase "physical analysis" refers to non-electrical characterization, which includes ALD film growth behavior, film morphology, thermal stability and crystallization/transformation kinetics, and compositional analysis. *Blanket wafers* were prepared according to the following procedure. Bare, *p*-type silicon (100) wafers ($\rho = 5 - 10\ \Omega$-cm) were cleaned first in sulfuric acid – ozone mixture (SOM) and then in a solution of Standard Clean – 1 (SC1) (details of the solution chemistries are given in Appendix A). Next, the wafers were dipped for 45 s in a 50 H_2O : 1 HF solution in order to remove native oxide on the Si surface. After this, the wafers were rinsed with de-ionized water for 10 min and blown dry, resulting in a hydrophobic surface. Subsequent steps to prepare the blanket wafers varied slightly depending on the types of experiments to be performed. The variations are discussed in sections A and B below.

A. Samples for HfO_2 Growth Study

To investigate the effect of different silicon surface treatments on the ALD HfO_2 film growth rate, three types of underlayers were investigated: H-terminated Si, chemical oxide, and thermal oxide. The processing conditions (or treatments) used to form these underlayers are shown in Table 3.2. The process already described above yielded an H-terminated surface and therefore no further treatment for H-terminated samples was required after drying. To prepare the chemical oxide, wafers were rinsed for 60 s in de-ionized water containing approximately 5 ppm ozone. Thermal oxides (SiO_2 and SiO_xN_y)

were grown by rapid thermal oxidation (RTO) under the conditions shown in Table 3.2. The underlayer thicknesses shown are the mean thicknesses measured by ellipsometry (section 2.4 and later in section 3.3.4), taken from 49 different measuring sites per wafer.

Table 3.2 Underlayers fabrication

Underlayer name	Chemistry	Temperature (ºC)	Time (s)	Underlayer thickness (nm)
HF - last (no underlayer)	none	-	-	-
O_3 chemical oxide	De-ionized water rinse (with 5 ppm O_3)	RT	60	0.55
Thermal SiO_2	RTO in Oxygen	900	35	0.5
Thermal SiO_xN_y	RTO in 60% NO / 40% O_2	850	10	0.53

The stability of the underlayer oxide (or H-terminated surface) during air exposure is an important issue since these underlayers were formed *ex situ* prior to ALD. Care, therefore, was taken to minimize the air exposure time prior to ALD deposition. After underlayer preparation, wafers were loaded into the ALD tool loadlock within about 5 min, and remained there at a pressure of 10^{-2} Torr until each was transferred to the ALD deposition chamber. Similar care was taken in preparing all the other wafers (including the device wafers, described in the next section) used in this work.

Films were prepared with "thicknesses" ranging from 3 to 100 growth cycles. The HfO_2 film thicknesses were measured with an ellipsometer immediately after deposition. In addition, RBS (section 2.2) was used to obtain areal density (atoms/area) information from 200 Å thick films grown on various underlayers. The growth behavior

of HfO_2 films was monitored by plotting the film thicknesses (and Hf coverages) as a function of ALD cycles.

B. Samples for Crystallization/Transformation Kinetics and Compositional Studies

For these samples, following the already-mentioned HF dip to remove native oxide, a ~ 5 Å thermal SiO_2 underlayer was formed on the wafers by RTO in O_2 at 900°C, for 35 s (Table 3.2). HfO_2 and Hf-aluminate films were then grown on these wafers using ALD. Details of the ALD deposition have been described in section 3.1. Table 3.3 summarizes the relevant deposition information for the samples with aluminate films. The *x-y-z* notation is explained as follows: one *bilayer* consists of *x* H_2O / TMA cycles, followed by *y* H_2O / $HfCl_4$ cycles. The total number of *bilayers* is represented by *z*.

Table 3.3 Summary of the precursor pulses ratio and total number of cycle repetitions to obtain the desired thickness and composition for all the aluminate samples used in this experiment. The notation *x-y-z* refers to the value listed in the columns labeled *x*, *y* and *z*. Samples A to E and F to H were used for MEIS and XRD analysis, respectively.

Samples	Number of cycles being pulsed in one *bilayer*		Number of *bilayers*
	H_2O / TMA	H_2O / $HfCl_4$	
(x-y-z)	*(x)*	*(y)*	*(z)*
1-1-36 (A)	1	1	36
4-4-9 (B)	4	4	9
3-1-14 (C)	3	1	14
1-5-12 (D)	1	5	12
0-1-60 (E)	0	1	60
F	1	3	80
G	2	3	60
H	2	1	92

Transformation Kinetics and Thermal Stability Analysis – XRD was used to investigate the transformation kinetics and amorphous-to-crystalline thermal stability of both HfO_2 and Hf-aluminate films. XRD was also used to monitor grain growth in the films. Three different Hf-aluminate films compositions [samples F (25%Al), G (50%Al) and H (75%Al)] were examined. The Al fractions in these films were estimated using equation 3.1 given below. An additional sample consisting of a pure HfO_2 film deposited on a 0.55 nm *O_3-generated* chemical oxide underlayer was also examined. The preparation of this underlayer has been described in part A of this section. In order to obtain a satisfactory diffraction pattern, relatively thick films (~ 200 Å, as measured by ellipsometry) of the relevant samples were deposited. These samples were either rapid thermal annealed (RTAed, for annealing times ≤ 10 min) in a Heatpulse® 8108 RTA system or annealed in a tube furnace (for annealing times > 10 min), both in an N_2 ambient. In this RTA process, rapid temperature ramp-up and ramp-down rates (~ 30ºC/s) were achieved. The details on the XRD setup will be outlined in section 3.3.1. XRD results were further supported using TEM imaging.

Compositional Analysis – MEIS was used to investigate the correlation between Al to Hf ALD cycles ratio (i.e., *x* to *y* ratio in Table 3.3) and the composition of Hf-aluminate films. The film thickness obtained from the simulations of the MEIS data was used to verify the film thickness measured by ellipsometry. Samples A – E with Hf-aluminate films were analyzed by MEIS. These samples were thin (~ 40-50 Å) relative to those used in XRD analysis. Thin films were used in order to prevent the heavy element (Hf, in this case) peak from overlapping the oxygen and aluminum peaks. An assumption was made that annealing does not alter film compositions, and therefore, only

as-deposited films were examined for composition. A detailed description of the MEIS setup will be presented in subsection 3.3.2. The composition and thickness of the Hf-aluminate films were controlled by varying two parameters in the ALD process: (1) the ratio of cycles between the HfO_2 (y) and Al_2O_3 (x) reactants being pulsed and (2) the total number, z of cycle repetitions. The ability to predict the composition of this aluminate film was demonstrated by comparing Al fractions calculated using the formula below with Al fractions (or an equivalent Hf fraction) measured by MEIS.

$$\text{Al fraction (\%)} = \left[\frac{x_{Al} \bullet N_{Al} \bullet D_{Al} \bullet R_{Al}}{(x_{Al} \bullet N_{Al} \bullet D_{Al} \bullet R_{Al}) + (y_{Hf} \bullet N_{Hf} \bullet D_{Hf} \bullet R_{Hf})} \times 100 \right] \qquad (3.1)$$

The subscripts "Al" and "Hf" in the above formula represent the corresponding values for Al_2O_3 and HfO_2, respectively. The symbols x and y are described in Table 3.3. N is a given materials tabulated bulk density [1], and D is a density reduction factor estimated from the measured density. The measured ALD Al_2O_3 film density, grown on ~ 5 Å thermal SiO_2 using optimized ALD parameters listed in Table 3.1, was found to be approximately 74% of fully dense bulk Al_2O_3 (therefore, $D_{Al} = 0.74$), and the density of ALD HfO_2 was assumed to be equal to the bulk value (10.01 g/cm^3) [2]. The measured Al_2O_3 density was obtained by dividing the Al areal density as measured using MEIS by the TEM thickness obtained from a cross-sectional TEM image. R denotes the growth rate (will be determined in chapter 4) of Al_2O_3 (0.86 Å per cycle) and HfO_2 (0.59 Å per cycle).

3.2.2 Device Wafers (MOS Capacitor Fabrication Process)

200 mm diameter p/p^+ epitaxial Si(100) wafers were used as substrates for capacitor fabrication. These e*pi-wafers* (Fig. 3.3a), consisting of a lightly doped (N_A = 2E15/cm^3) epitaxial film on a heavily doped substrate, were used for device fabrication instead of regular Si wafers primarily to minimize the bulk series resistance. As can be seen from Fig. 3.3a, there are layers of undoped poly-Si (layer 1) and oxide at the backside of the wafers, which needed to be removed later. The wafer cleaning and

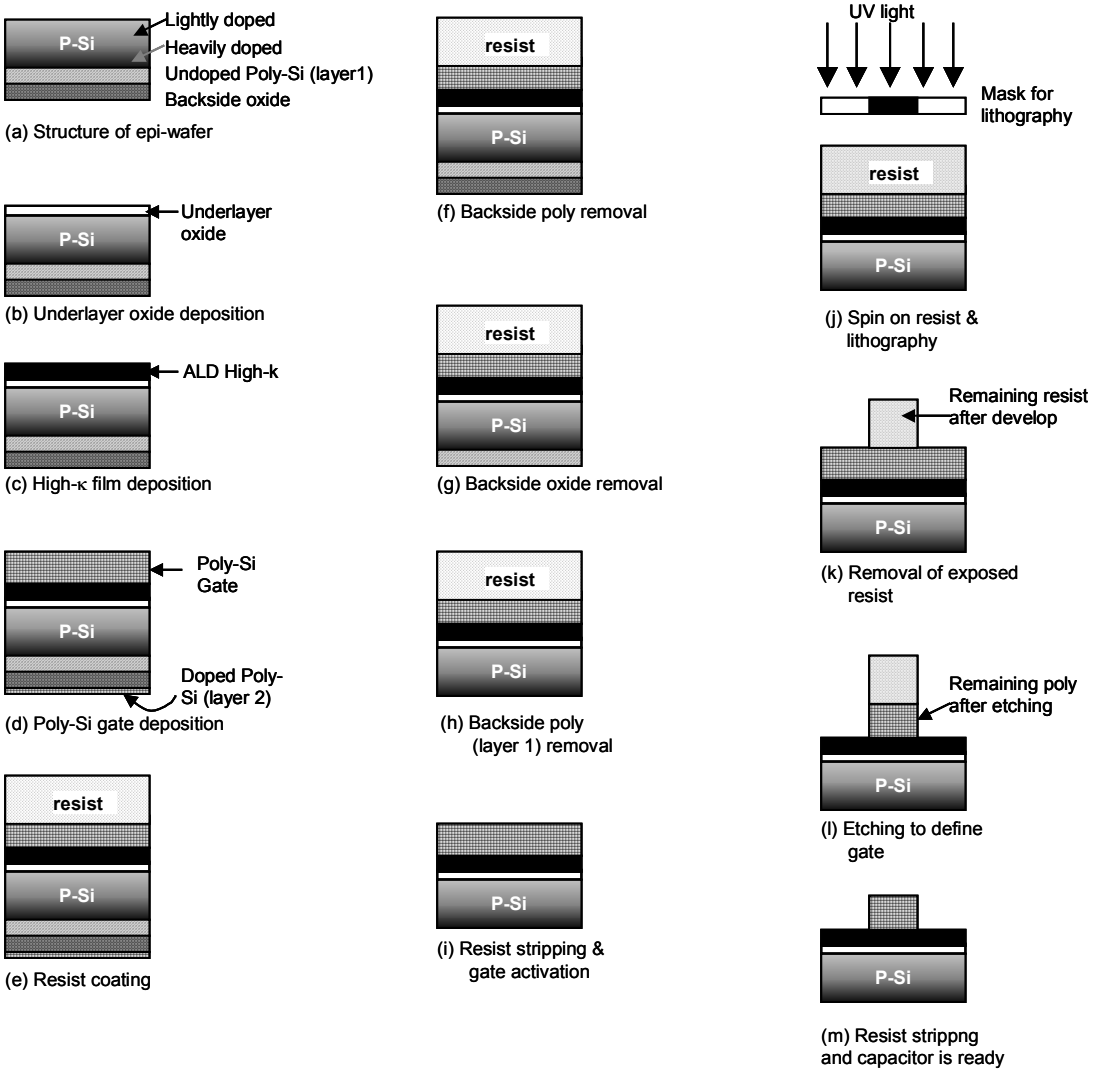

Fig. 3.3 Process flow for MOS capacitor fabrication

underlayer formation procedures were the same as those used to prepare the blanket wafers, described in section 3.2.1. Following wafer cleaning, MOS capacitors were fabricated according to the procedure described below and illustrated in Fig. 3.3.

Step 1. Underlayer oxides formation (Fig. 3.3b)

Thermal oxides (SiO_2) and oxynitrides (SiO_xN_y) were grown by RTO, while the chemical oxides were formed on H-terminated wafers using ozonated cleaning chemistries (see Table 3.2). The underlayers were grown to thicknesses of approximately 5 Å. Prior to ALD, selected wafers with chemical oxide were pre-annealed at 800ºC for 10 min in N_2 ambient. These pre-annealed samples were used to investigate the effect of pre-annealing on electrical properties of the gate stacks.

Step 2. ALD HfO_2 and Hf-aluminate films (Fig. 3.3c)

Films ranging from 30 Å to 120 Å in thickness were grown by ALD using the temperatures and growth cycle time parameters described in section 3.1.2.

Step 3. Post-deposition anneal (PDA)

To ensure that the ALD films had minimum exposure times to the atmosphere, *ex situ* PDA was performed immediately after ALD. Films were RTAed at atmospheric pressure in a Heatpulse 8108™ system for various temperatures and times. "Spike anneal" refers to RTA where the soak time was less than 1 s.

Step 4. Poly-Si deposition (Fig. 3.3d)

In order, again, to have minimum exposure times to the atmosphere, these films were loaded into the atmospheric-pressure chemical vapor deposition (APCVD) chamber immediately after PDA. Using APCVD, the annealed films were capped

with a 1500 Å thick *in situ* phosphorous-doped poly-Si film that acted as the n^+ gate electrode of the capacitor. This doped poly-Si gate electrode was deposited at 550ºC from a mixture of silane (SiH_4) and H_2 gas (flow rate ~ 300 sccm) with phosphine (PH_3) as the doping gas, according to the following reaction:

$$SiH_4\ (g) + 2H_2\ (g) \rightarrow Si\ (s) + 4H_2\ (g) \qquad (3.2)$$

Step 5. Photoresist spin-coating (Fig. 3.3e)

Approximately 1 μm thick layer of photoresist was spun on the top of the poly-Si, followed by curing at 110ºC for 90 s. The photoresist served to protect the poly-Si gate electrode during the backside removal process in the next step.

Step 6. Backside poly-Si (layer 2) removal (Fig. 3.3f)

In order to minimize the influence of contact resistance during electrical measurements, all insulators such as undoped poly-Si and oxide layers at the back of the wafers had to be removed. This backside removal procedure is described in this and the following two steps. Due to the design of the APCVD tool, a layer of poly-Si (layer 2) with approximately the same thickness as the gate electrode (~ 1500 Å) was formed simultaneously at the back of the wafer during poly-Si gate electrode deposition. This layer was "dry" etched in NF_3 gas at 55ºC (at this temperature, the etch rate is ~ 4000 Å/min) for 30 s.

Step 7. Backside oxide removal (Fig. 3.3g)

The 9000 Å oxide at the back of the wafers was removed by wet etching in a buffered oxide etch solution that contained a mixture of seven parts NH_4F to one part 49% HF acid (by volume) at room temperature. Wafers were immersed in this solution for approximately 360 s until a hydrophobic surface was obtained,

indicating the oxides were fully removed. Following oxide removal, samples were rinsed with de-ionized water and spin-dried.

Step 8. Backside poly-Si (layer 1) removal (Fig. 3.3h)

The 8000 Å layer of undoped poly-Si was removed using the same chemistry described in step 6. However, a longer etching time (~ 200 s) was needed since this layer was much thicker than the layer 2 poly-Si.

Step 9. Resist stripping (Fig. 3.3i)

After completing the backside removal, the protective photoresist layer on top of the wafers formed in step 5 was removed by holding the wafers at 250ºC in an oxygen plasma (stripping rate ~ 2.3 μm/min) for 60 s. This process is often called *resist ashing*.

Step 10. Gate activation

Dopants in the gate electrode were then activated at 800ºC RTA for 10 s in a N_2 ambient. The sheet resistance of this activated, doped poly-Si was measured using four-point-probe. Based on tabulated values [3], the corresponding phosphorus concentration is approximately 5×10^{19} cm^{-3}.

Step 11. Lithography (Figs. 3.3j and 3.3k)

In this step, a photoresist layer was again spin-coated on top of the poly-Si gate and cured as in step 5. The wafer was then aligned with the appropriate mask (which provides a pattern to be transferred to the wafer) using a 248 nm UV light stepper. Following alignment, the photoresist was exposed through the mask UV light. This exposed positive photoresist went through a chemical change, and became highly soluble in a specifically designed developer, leaving the

unexposed region as shown in Fig. 3.3k. It should be noted that on a single wafer, there were patterned more than 50 MOS capacitors with a gate area of 1×10^{-4} cm^2 (100×100 μm square) each. For simplicity, Fig. 3.3 only shows the formation of one individual MOS capacitor.

12. Poly-Si etching (Fig. 3.3l)

    Regions of exposed poly-Si were etched away in a gas mixture of 3 Cl_2 : 1 HBr at 60ºC for approximately 23 s, with a working pressure of about 50 mTorr.

13. Resist stripping (Fig. 3.3m)

    The remaining resist was then stripped in an oxygen plasma as described in step 9, leaving the poly-Si gate structure exposed.

14. Forming gas anneal

    All the patterned wafers were annealed for 30 min in a horizontal tube furnace at 400ºC under an atmosphere of forming gas (90%N_2 / 10%H_2).

For the purpose of process control, the thicknesses of selected films (including HfO_2, Hf-aluminates, oxide, and poly-Si films) were measured at various points of the fabrication process using ellipsometry (see Appendix B). The electrical measurements were then carried out on this n^+poly-Si/high-κ/underlayer oxides/p-Si capacitor structures, described later in section 3.3.5. Device parameters such as EOT values, flatband voltage, fixed charge density, and effective dielectric ($\kappa_{high\text{-}\kappa}$) constant were then extracted from these measurements. The value $\kappa_{high\text{-}\kappa}$ was calculated using equation 1.4 (chapter 1). Referring back to this equation, one can see that by plotting the EOT as a function of ellipsometry thickness ($t_{high\text{-}\kappa}$), the slope of this linear line will be equal to $3.9/\kappa_{high\text{-}\kappa}$. The y-intercept of this line represents the interfacial oxide thickness.

3.3 Sample Characterization

3.3.1 XRD Setup

XRD was performed in a General Area Detector Diffraction System (GADDS) [4] using Cu K_α radiation. The GADDS system was equipped with a 2D detector. All the samples were measured with the center of the 2D detector held fixed at $2\theta = 45^\circ$ and $\chi = 90^\circ$. During signal collection, the samples were continuously rotated through the range $10^\circ < 2\omega < 40^\circ$. The angle ω is the angle of sample rotation around an axis perpendicular to the incident x-ray beam; ω is zero when the film surface is parallel to the incident x-ray beam. To obtain a standard diffracted intensity versus 2θ plot, the collected 2D diffraction pattern was integrated over the range of $-65^\circ < \chi < -115^\circ$, where χ is an angle of rotation about the direction of the incident x-ray beam. The resulting plots covered the range of $15^\circ < 2\theta < 65^\circ$. All runs were performed for 500 s in order to yield a comparable signal-to-noise ratio from sample to sample. The average crystallite size in the samples was calculated using the *Scherrer* formula [5, 6]:

$$L = 0.94\lambda / W_{eff} \cos\theta, \tag{3.3}$$

where L is the structural coherence length (which is essentially equivalent to the average grain size), λ is the wavelength of the x-ray radiation (0.1542 nm), and W_{eff} is the effective full width at half maximum (FWHM) of the x-ray peak located at 2θ. It should be noted that besides grain size contribution, peak broadening could also be due to some other factors, such as instrumental broadening and microstrain. In order to determine the peak broadening due to instrumental parameters, which include beam size, sample-to-

detector distance, and air scatter, a bare Si substrate, the same type as used for film deposition, was scanned using the same XRD setup. It was found that the measured FWHM (W_{system}) of the (111) Si peak ($2\theta = 28.5^{o}$) was 0.527º. The W_{eff} is calculated from the measured peak width (W_{meas}), using equation 3.4 [6]:

$$W^2_{eff} = W^2_{meas} - W^2_{system}. \quad (3.4)$$

A well-developed HfO_2 peak near $2\theta = 28.4^{o}$ was the peak used in this study to estimate the grain size. A Gaussian line shape was fitted to the HfO_2 peak using standard software. The FWHM was then calculated by the software using this Gaussian line shape. From the uncertainty associated with a given fit, the software yielded an uncertainty for FWHM; this uncertainty was used to obtain the error associated with the measured grain size. The area under the Gaussian peak was used in gauging the degree of transformation in a film.

3.3.2 MEIS Setup

In this experiment, MEIS results were acquired using a 98 keV H^+ ion beam. The incident beam was channeled along a <112> axis of the Si substrate, which reduced the Si substrate contribution to the signal. The detector was held at a scattering angle of 90º, along the <111> direction of Si, in order to obtain blocking configuration by the Si atoms. The configuration is illustrated in Fig. 3.4. The analysis chamber was connected to a Ti sublimation pump and the working pressure was about 10^{-10} Torr. The yield of backscattered ions was proportional to the atomic number of the elements in the target. Since a heavy element, Hf (Z = 72), was involved in this experiment, a fairly low beam current was used (~ 3 – 5 nA) to prevent backscattered ions from *flooding* the detector.

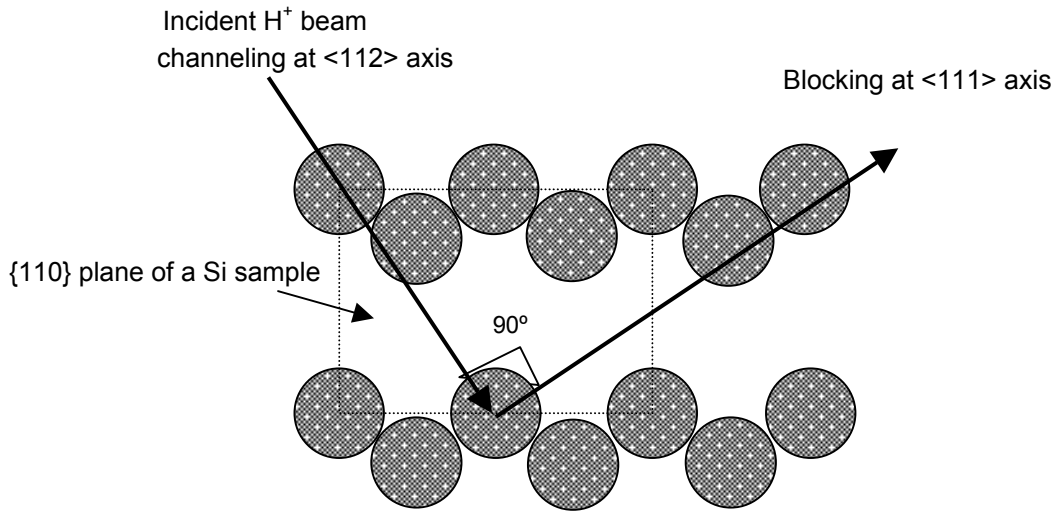

Fig. 3.4 Schematic configuration of an MEIS experiment, illustrating the use of channeling to reduce the Si substrate contribution to the signal from the light elements (O and Al) in the film. The detector is held at 90º relative to the incident beam to obtain a blocking configuration of Si atoms.

3.3.3 TEM Setup

TEM was performed in a Philips EM420 TEM system, operating at 120 kV. Cross section samples were imaged along the <110> direction of the Si substrate and were prepared as follows. The samples were cut and bonded with epoxy to produce the typical cross-sectional TEM sandwich structure. Then the sandwich was sectioned and mounted by glue on a polishing block. This was followed by mechanical grinding and polishing, using a Tripod Polisher [7] (a mechanical device with three pivot points, each driven by an individual micrometer, used to hold the sample against the polishing wheel). The samples were ground and polished on both sides to obtain a wedge shape of the sample with thickness at the wedge tip of 10-100 nm. In this work, one of the amorphous film samples was imaged along <110> direction using a STEM in order to obtain a

greater image contrast, as described in section 2.3. STEM was performed in a JEOL 2010F ARP-STEM system, operating at 200 kV.

3.3.4 Ellipsometry Setup

The spectroscopic ellipsometer (SE) employed in this work uses a broad spectrum of ultraviolet and visible light. It contains two separate bulbs, a tungsten-halogen bulb and a UV bulb. The tungsten-halogen bulb produces primarily visible wavelengths (4000 – 8000 Å), and the UV bulb provides wavelengths in the UV region (1900 – 4000 Å). The light from both of these sources is combined at a special beam combiner. The light path is then passed through a polarizer and focused onto the sample with an incident angle of 65º. The detector in this semi-automatic tool is equipped with a graphic display system showing the ongoing measurement data.

The need for accurate and precise measurements of film thickness is crucial in this work since most of the oxide films studied are < 10 nm thick. Simultaneous modeling of different layer characteristics (e.g., t, n, k) of a *very* thin film can cause inaccuracy in data acquisition due to strong correlation in the regression between these parameters. Therefore, a thick (> 20 nm) HfO_2 film (on top of a thin SiO_2 underlayer deposited on Si substrate) was used to determine the initial value of n using a two-layer model. The model uses the tabulated n and k values for SiO_2 and Si substrate (see Appendix B) as known parameters, while the n and t for HfO_2 are the variable parameters during measurements. Measurements were performed at 49 sites on the thick film. At the same time, the goodness-of-fit, GOF (confidence limits), was being monitored. The

value of n for HfO_2 film obtained from this measurement was then used as a known parameter during subsequent HfO_2 film thickness measurements. In this case, a single-layer model with fixed refractive index was used. The optical constants for various oxides are listed in Table B.1 (Appendix B).

3.3.5 *C - V* and *I - V* Measurement Setup

In this work, the *C–V* and *I–V* measurements were carried out in a light-proof probe station under an atmosphere of flowing dry N_2 [8, 9]. Exposure of the sample to light during testing would result in the undesirable generation of minority carriers, whereas exposure to ambient humidity could induce an undesirable current flow on the oxide surface. Ohmic contact was made to the MOS-C test structure on the device wafers by means of a tungsten contact probe mounted on a micromanipulator, which made it easy to position the probe on the relatively small poly-Si gates. The back contact was made by securing wafers on a chuck plate using a vacuum. It will be recalled from section 3.2.2 that the insulator layers on the backside of the wafer were removed to improve this back contact.

C – V measurements – The *C–V* profiles were obtained by employing an AC signal (with a *small-signal* amplitude range [9]) superimposed on a slowly varying DC gate voltage (V_G) sweep, while measuring the capacitance at a certain frequency using an impedance-capacitance-resistance (LCR) meter. The tungsten probe made contact with the poly-Si gate of a given capacitor (see inset of Fig. 2.2a in chapter 2); the backside of the Si substrate, which acted as one of the contacts to the capacitors, was grounded.

During a given test, V_G was stepped from inversion (1.0 V) to accumulation (–2.0 V) in steps of 0.05 V. The two contacts to the capacitor were connected to the LCR meter (HP 2484 A). A V_G sweep rate of 50 mV/s was used. It was found that this sweep rate ensured that the capacitor was in equilibrium during measurements. The *C–V* curves were obtained for each capacitor at three different frequencies: 10 kHz, 100 kHz and 1 MHz. In order to ensure that the *C–V* curve obtained was reproducible for a given test, the measurement was repeated using a new capacitor until a repeatable *C–V* curve was obtained.

I–V measurements – The gate leakage current, I_G, was measured by sweeping the DC voltage from 0 V to –3.0 V in steps of 0.05 V. The same setup used in the *C–V* measurements was used in the *I–V* measurements, except that the two contacts from the sample were connected to a parameter analyzer (instead of an LCR meter) that gave a direct measurement of the I_G. Leakage density, J_G, was then obtained by dividing I_G by the gate area.

3.3.5.1 Extracting MOS Device Parameters

In this work, two important parameters were directly extracted from the measured *C–V* curves using the NCSU *C–V* analysis program [10]: (1) EOT, and (2) ΔV_{FB}. Before the desired information could be extracted, however, it was necessary to correct the measured *C–V* data for the series resistance, R_s, which can cause errors in information extraction. R_s can arise from the contact made by the W-probe to the gate, from the back contact to the Si substrate, or from the Si substrate itself due to nonuniform doping distribution. R_s was measured separately for each capacitor. R_s will have its greatest

effect on both measured capacitance and equivalent parallel conductance under the condition of strong accumulation [9]. Therefore, in this work, the R_s was measured by the LCR meter when a given capacitor was in an accumulation state. The corrected capacitance, C_c and the corrected equivalent parallel conductance, G_c, at the frequency of interest were calculated using the equations:

$$C_c = \frac{\left(G^2_m + \omega^2 C^2_m\right) C_m}{a^2 + \omega^2 C^2_m}, \tag{3.5}$$

$$G_c = \frac{\left(G^2_m + \omega^2 C^2_m\right) a}{a^2 + \omega^2 C^2_m}, \tag{3.6}$$

where $a = G_m - (G^2_m + \omega^2 C^2_m)R_s$ and C_m and G_m are the measured uncorrected capacitance and the uncorrected equivalent parallel conductance. ω is the angular frequency of the AC voltage (radians sec^{-1}). The corrected *C–V* data were used as the input files for the *C–V* analysis program. The *C–V* analysis program also required the following two additional inputs to do the simulations calculations:

- Gate doping density: 5×10^{19} cm^{-3} (see section 3.2.2)
- Gate area: 1×10^{-4} cm^{-2}

The values of EOT, V_{FB} and Φ_{ms} were determined by matching the experimental *C–V* data to this physics-based theoretical model and given by the program as an output file. From these, ΔV_{FB} ($=V_{FB} - \Phi_{ms}$) can be obtained. The effects of polysilicon depletion and quantum mechanical phenomena (quantization of energy levels) [10, 11] are automatically accounted for during simulations; therefore, the EOT is not overestimated. Theoretical *C–V* curves presented in chapter 6 were also obtained from this program. To produce the theoretical *C–V* curves, the program uses the EOT (this is the EOT obtained

above from the measured data), type of substrate (in this case, *p*-Si), gate area, and gate doping density as the input information. The *theoretical C–V* curve represents the *ideal C–V* curve for a gate stack with defect-free gate dielectric.

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CHAPTER 4: GROWTH BEHAVIOR OF ALD HfO_2

As already mentioned in section 1.2.3, the presence of surface sites, such as –OH or –NH groups is essential for growth of ALD HfO_2. The best-known practical way of producing these surface groups is by forming an ultrathin oxide (SiO_2 or SiO_xN_y) layer on the surface of a Si wafer. This starting surface leads to well-behaved, two-dimensional ALD growth of HfO_2-based materials. The underlayer should be as thin as possible because the thickness of this layer will directly add to the overall equivalent oxide thickness (EOT) value of the gate stack. It is possible that future gate oxides for MOSFET will be processed by ALD due to the advantages of this technique discussed in chapter 1. HfO_2 deposited using this technique has been studied by many research groups, both physically and electrically [1-5]. A fundamental study on the growth behavior of HfO_2, however, is lacking. In order to successfully implement HfO_2 high-κ materials into CMOS technology, it is important to understand the effect of different silicon surface treatments on ALD film growth behavior. The goal of this study was to determine the efficiency of various underlayers for the nucleation and growth of atomic layer deposited HfO_2 films.

4.1 Effect of Different Surface Treatments on ALD Deposition Rate

In this part of the work, each sample was analyzed by ellipsometry *and* RBS. The details of the sample preparation have been described in section 3.2.1 (part A). The ALD deposition parameters (listed in section 3.1.2) were optimized to ensure that films grew in the most two-dimensionally continuous HfO_2 film with good thickness uniformity. The

effect of various underlayers on the growth rate is depicted in Figs. 4.1a and 4.1b. In Fig. 4.1a the ellipsometric thickness of HfO_2 layers grown on various underlayers are plotted as a function of ALD cycles. Figure 4.1b is a plot of Hf coverage obtained from RBS versus ALD cycles. The same set of samples provided the data for both figures. These figures also contain data from films grown on H-terminated Si. The ellipsometry thicknesses presented in Fig. 4.1a, were obtained using a pre-measured refractive index for HfO_2 of 2.08; the details of the measurement have been described in section 3.3.4. The measured refractive index for HfO_2 is in good agreement with those obtained by Balog *et al*. [6].

RBS was used to validate the ellipsometer thickness measurements because ellipsometry results are indirect and depend on an accurate knowledge of a number of parameters, and on the assumptions made for the layer structure (such as sharp planar film-substrate boundary and uniform material density). From an industry point of view (and also in this work), however, using ellipsometry is clearly a faster and more practical method of measuring thickness for processing control purposes during device fabrication. Measuring Hf coverage (areal density) with RBS provided an unambiguous method of studying the HfO_2 nucleation and growth behavior. Both methods show the same general trends in growth. The following discussions in this chapter will mostly be based on Fig. 4.1b.

Two extreme growth behaviors can be clearly observed: Firstly, the H-terminated (no underlayer) sample shows a very nonlinear growth, especially at a low Hf coverage region (Fig. 4.1b). Similar results have been reported by many research groups, where

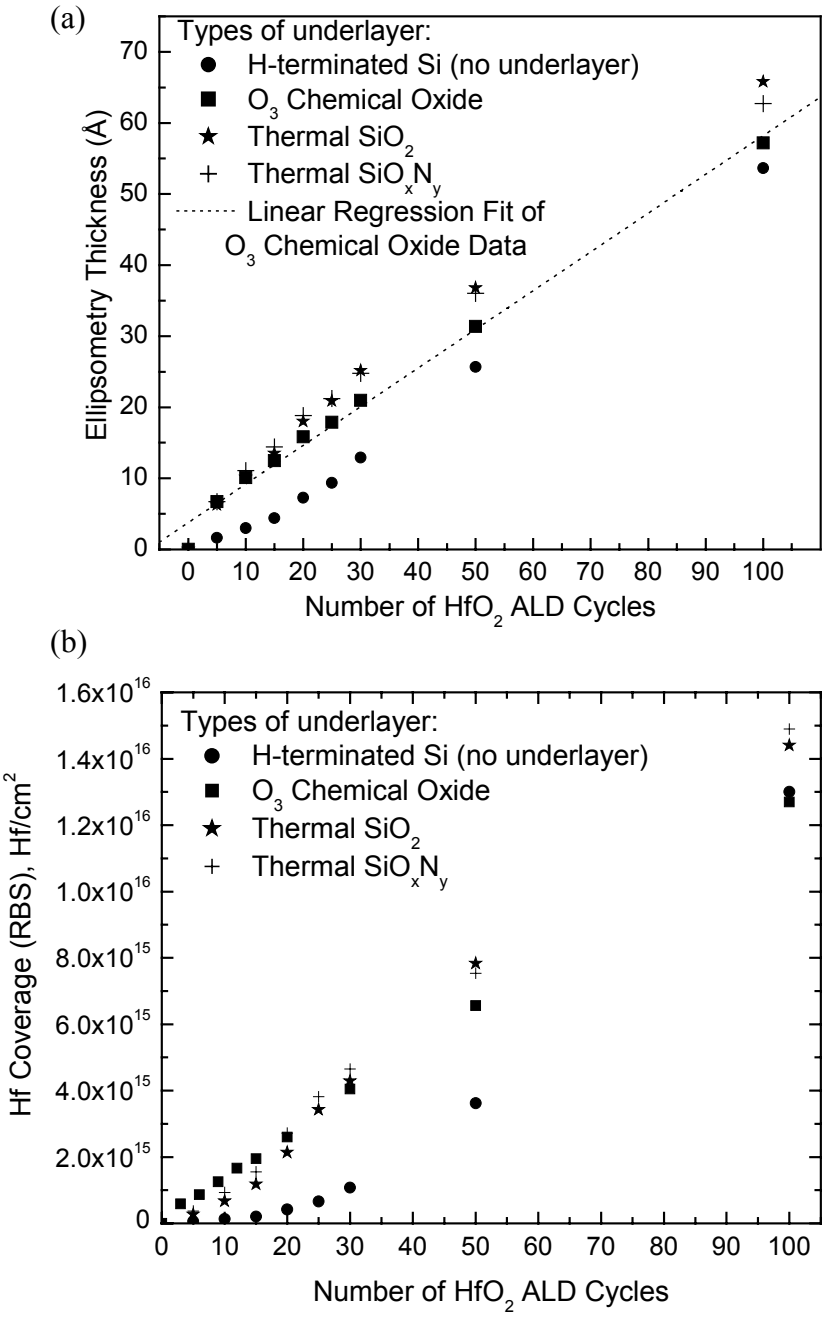

Fig. 4.1 (a) Ellipsometric thickness and (b) Hf coverage plotted as a function of ALD HfO_2 cycles for various underlayers. The slope of the linear regression fit in the top figure yields the ALD HfO_2 film growth rate of ~ 0.59 Å per cycle.

three-dimensional, island growth behavior is observed using TEM [7, 8]. This can be interpreted as a nucleation barrier characteristic of the weakly reactive H-terminated surface. The discrepancy between the ellipsometry and RBS results for the H-terminated sample (the growth seems to start out more slowly when measured by RBS) is probably due to the uncertainty of the ellipsometrically-determined-thickness measurements when there are islanded HfO_2 regions on bare Si rather than a continuous film. It is well known that microscopically surface roughness (due to incomplete coverage in this case) is a major factor in limiting accurate thickness measurement of the film thickness with an ellipsometer.

In order to determine whether HfO_2 growth occurs by a two-dimensional or three-dimensional mechanism, however, measurements by surface-sensitive techniques are required. Although time-of-flight SIMS (TOFSIMS) and atomic force microscopy (AFM) were not relied upon heavily in this work, and are therefore not included in the discussion of experimental techniques in chapter 3, they were employed sparingly to verify morphology of films deposited on thermal and chemical oxides and H-terminated Si (background information on these techniques can be found in Refs. 9, 10]. TOFSIMS was used to measure Si intensity from the substrate as a function of HfO_2 cycles. One expects that the film with the most two-dimensional HfO_2 coverage would have the steepest decrease in the underlying TOFSIMS Si signal as a function of Hf cycles. As discussed elsewhere [11], TOFSIMS data shows that HfO_2 grown on H-terminated Si exhibits a lesser decrease of Si intensity as compared to substrates with surface SiO_2. This indicates that HfO_2 growth on SiO_2 results in much more two-dimensional HfO_2 growth compared to growth on H-terminated samples. The increased roughness of HfO_2

films grown on H-terminated Si was also further evident by the increased root-mean-square (RMS) surface roughness values as measured using AFM (Table 4.1). The absolute RMS values in Table 4.1 clearly show that for HfO_2 growth of 25 cycles and above, the RMS value differs significantly between samples with and without initial SiO_2 layer. This observation is consistent with the reported findings of Copel *et al*. [8], where high-resolution TEM was used to distinguish the film morphology of ultrathin ALD ZrO_2 grown on an initial SiO_2 layer compared with growth on H-terminated Si. It was reported that growth on H-terminated Si resulted in the immediate formation of islands of three-dimensional growth, compared with nearly two-dimensional growth of very smooth ZrO_2 films on an underlying SiO_2 layer.

Table 4.1 AFM measurements of HfO_2 films grown on the various underlayers, as a functions of ALD $H_2O/HfCl_4$ cycles.

Number of H_2O / $HfCl_4$ cycles	RMS (Å)			
	H-terminated Si	Ozonated Chemical oxide	Thermal oxide	SiO_xN_y
0	1.22	1.30	1.32	1.10
10	1.36	no data	1.38	1.18
15	no data	1.02	no data	1.14
20	1.49	no data	1.35	1.19
25	2.09	1.33	no data	1.18
50	2.16	1.32	1.16	1.10
100	2.30	1.38	1.28	1.31

Secondly, Fig. 4.1b also shows that HfO_2 growth on chemical oxide occurs in a highly predictable, well-behaved manner from the onset of the first pulse. The data points lie essentially on a straight line that passes through the origin. This shows that there is a negligible *incubation* period (incubation time is defined as the delay, after starting the precursor pulse cycling, before measurable growth begins). The absence of

an incubation period indicates that growth initiates with the same density of surface sites (OH-terminated sites, in this case) that are maintained during steady-state growth. Note, however, that the linear fit to the chemical oxide data points obtained from the ellipsometry (Fig. 4.1a) intercepts slightly above the origin. This implies an inaccuracy in the ellipsometric subtraction model. The existence of OH* groups on SiO_2 and the consumption of OH* during the pulsing of $Al(CH_3)_3$ were evident using infrared spectroscopy in the study by Frank *et al*. [12, 13]. Note that the underlayer of the samples used in this work were prepared using the same method as in the experiment of Frank *et al*. [13].

It can be seen in Fig. 4.1b that the thermally grown underlayers represent intermediate cases, where the growth exhibits some nonlinearity at the initial stage of ALD, and only becomes linear after about 15-25 cycles. It can be observed further from the same figure that at a later stage (≥ 100 cycles), the growth rate per cycle is essentially the same for both thermal and chemical oxides. This indicates that thermal oxide has a lower density of initial surface sites compared to chemical oxide. In fact, studies have shown that chemical oxides do indeed have higher OH areal density than thermal oxide [13 - 15]. The amount of the surface sites on thermal oxide gradually increases with growth until it reaches a steady-state value, at which point, ALD growth for both underlayers is essentially the same. For the case of HfO_2 grown on a H-terminated surface, uniform film growth likely proceeds only after the coalescence of HfO_2 islands and the leveling of surface non-uniformities (i.e., the growth rate only becomes linear at a much later stage (after > 100 cycles) compared to surfaces with an oxide underlayer).

From the device performance point of view, this unavoidable oxide underlayer should be very thin to minimize the contribution to the equivalent oxide thickness of the gate stack, but be able to yield a uniform film with accurate thickness control. Results from this study show that chemical oxide is optimal. The ability to form a highly reproducible and uniform (ellipsometric thickness shows less than 1.5 Å variations across 200 mm wafers) chemical oxide as thin as ~ 5 Å was demonstrated in section 3.2.

The slope of the linear regression fit to the chemical oxide data of Fig. 4.1a yields a value of 0.59 Å per cycle. The linearity of the growth curve provides a good estimation of the HfO_2 film thickness by just calculating the number of cycles being pulsed. A similar investigation was performed for Al_2O_3 using the optimized deposition parameters listed in Table 3.1 and it was found that the growth rate for Al_2O_3 was ~ 0.86 Å per cycle. Both of these growth rate values were used to estimate the number of ALD cycles that are required to obtain the desired thickness of HfO_2 and Hf-aluminate films that were used in all the remaining experiments in this work. It should be noted also that these two values were used to estimate the Al or Hf fractions by using equation 3.1, described in section 3.2 and later in section 5.2.

4.2 Summary

HfO_2 has emerged as one the most promising gate dielectric material. Accurate thickness control and thickness uniformity of the deposited HfO_2 film are required for

these applications. While ALD is able to obtain atomic layer control of film growth, the type of underlayer plays an important role in determining the film growth behavior. Results from this study show that for ALD HfO_2 in particular, hydroxyl groups should be present on the top surface prior to the exposure of reactant vapors. Ultrathin oxides can be grown using RTO or ozonated water. The fact that *ozonated* chemical oxides (oxidation of silicon by means of ozonated solutions) yield the most predictable and well-behaved ALD growth has been proven by using both ellipsometry and RBS measurements. Chemical oxides have the added benefit of being able to be grown as thin as ~ 5 Å in good thickness uniformity and reproducibility, demonstrated in section 3.1. Because a minimum EOT is needed for optimum device performance in deep sub-micron CMOS technology, the benefit of being able to grow an ultrathin chemical oxide as the underlayer for high-κ gate stacks is clear. Besides, it also yields promising electrical data (lower oxide fixed charge compared to thermal oxide underlayer) as we will see later in chapter 6. Thermal oxide/oxynitride underlayers result in a short incubation period, as evidenced by the nonlinear growth for small HfO_2 coverages.

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CHAPTER 5:

PHYSICAL PROPERTIES OF Hf-BASED DIELECTRICS

5.1 Thermal Stability and Transformation Kinetics

The physical response of both HfO_2 and Hf-aluminate films during subsequent CMOS gate processing is presented in this section. Evaluation of transformation kinetics for HfO_2 films and thermal stability of Hf-aluminates amorphous phase has been established over a range of anneal temperatures and times, using blanket ALD high-κ films (~ 200 Å) deposited on either a chemical or thermal SiO_2 underlayer.

5.1.1 HfO_2

Figure 5.1 shows the XRD patterns obtained from HfO_2 films after annealing in an N_2 ambient at a series of different temperatures for various times. At the top of this figure are shown the peak positions and intensities for various structures of HfO_2 obtained from the powder diffraction ICDD card files [1]. For reference, these card files are reproduced in Appendix C. As described in the methodology chapter (section 3.2.1), ~ 200 Å films were used in this experiment to obtain an acceptable signal-to-noise ratio. A background XRD pattern was obtained from bare Si using the same setup as used for the other samples. This signal was then subtracted from all the spectra.

In Fig. 5.1, peaks shown by the solid arrows can be indexed as the monoclinic phase. The peak near $2\theta = 30.4^{\circ}$ (shown by the dashed arrow) was also observed in the

work of Ritala *et al*. [2], and may correspond to the orthorhombic phase, which was observed by Aarik *et al*. [3] for ALD HfO_2 films grown at 500ºC. The peak, however, can also be indexed as a tetragonal phase peak. Additional work is necessary to identify the phase(s) that produced this peak. There is no evidence that the as-deposited films on a thermal underlayer contain any amorphous phase. A study by Morisaki *et al*. [4] revealed that ALD HfO_2 films deposited on a thermal oxide underlayer were polycrystalline, while as-deposited HfO_2 films on a chemical oxide underlayer were amorphous. This is, in fact, consistent with the results obtained in this study for both a chemical and thermal oxide underlayer. The results associated with the chemical oxide underlayer will be addressed later in this section.

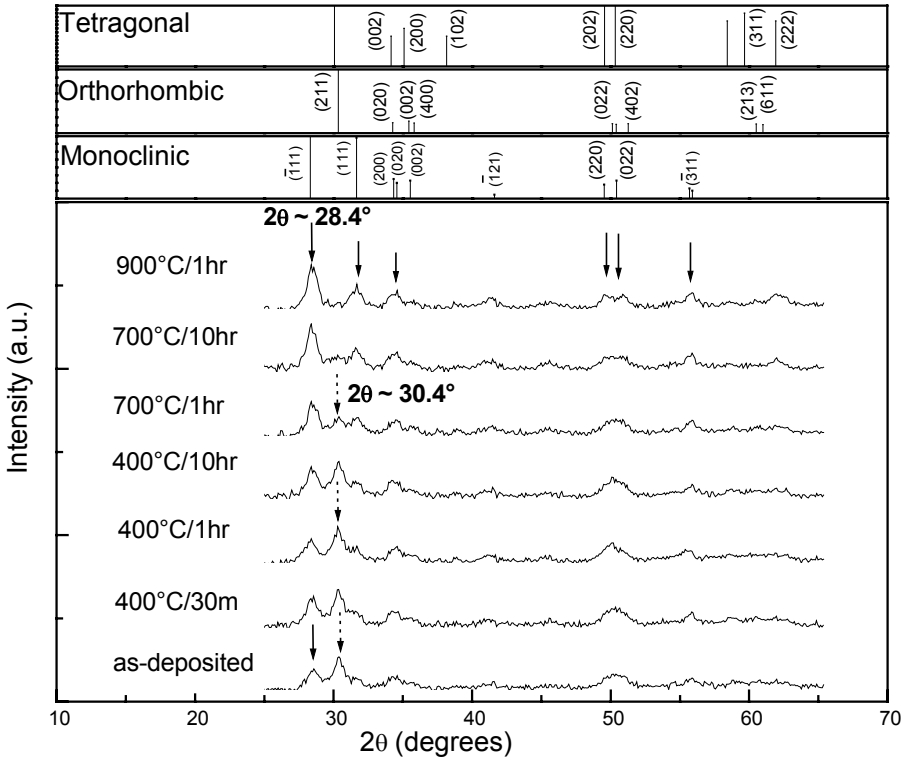

Fig. 5.1 XRD patterns of ALD HfO_2 films, showing the effect of annealing at a series of different temperatures and times. The upper part shows the peak positions and intensities for three main HfO_2 phases obtained from powder diffraction ICDD card files.

As the annealing temperature and time increased, all peaks intensified except the peak at 2θ = 30.4º, which suggests that the monoclinic phase is the stable phase in the films at the annealing temperatures used. Monoclinic HfO_2 is the stable polymorph of HfO_2 at room temperature and atmospheric pressure, whereas tetragonal and orthorhombic are the high-temperature (> 1900ºK) and high-pressure polymorphs (10 GPa), respectively [5, 6]. The transformation was complete after annealing at 900ºC for 1 hour, shown by the absence of the peak at 2θ = 30.4º in that spectrum. Additional experiments (not shown) were also performed using a series of intermediate annealing temperatures and times; the results fit the trend observed in Fig 5.1. The XRD area detector frame (Fig. 5.2) shows continuous HfO_2 rings with no obvious intensity variation, indicating that the films were polycrystalline with equiaxed grains. Therefore, it was practical to determine the grain size and the degree of transformation of the film by fitting to the crystalline $(\bar{1}11)$ peak. In this study, the phrase "degree of transformation"

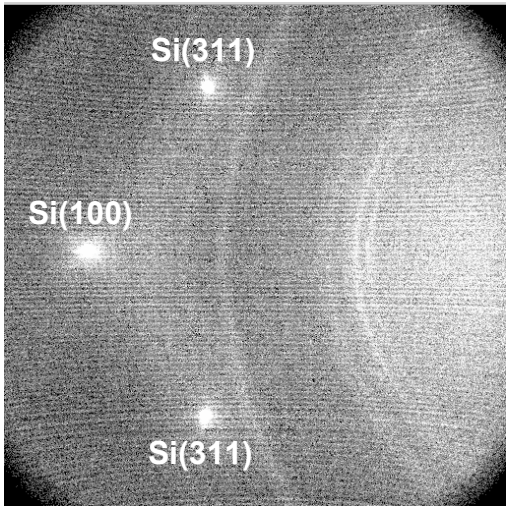

Fig. 5.2 An area detector frame, showing the continuous Debye rings, indicating the HfO_2 films are polycrystalline with equiaxed grains. The three bright spots belong to the Si substrate. The HfO_2 film has been annealed at 900ºC for 1 hour.

refers to the fraction of the monoclinic phase in a sample with respect to the fully transformed sample. The FWHM and area under the ($\bar{1}11$) peak (2θ = 28.4º) were determined by fitting the peak with a Gaussian curve.

Figure 5.3 shows the evolution of the HfO_2 grain size as a function of various annealing temperatures and times. The three different temperatures, 400ºC, 700ºC, and 900ºC chosen in this study fall in the temperature range where a typical high-κ film will be annealed. Even though a typical annealing time would not be longer than 30 minutes,

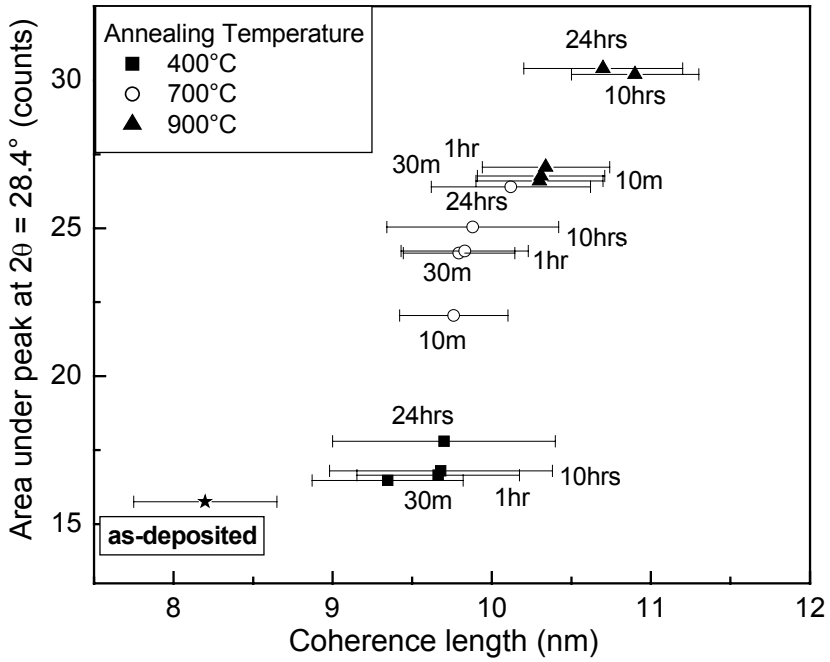

Fig. 5.3 Evolution of grain size in HfO_2 films as a function of various annealing conditions. The mean grain size is estimated using the Scherrer formula from the FWHM of the ($\bar{1}11$) peak, assuming equiaxed grains. The area under the same peak is deduced from Gaussian fits, representing the fraction of the sample that was crystallized upon heat treatment. The error associated with the Gaussian fits is presented with the error bar.

the annealing time in this study was purposely extended long enough to cause easily detectable changes if any, in the grain growth with time at a given temperature. The

areas under the peak (which are proportional to the fraction of monoclinic phase in the films) are plotted as a function of coherence length. Note that the error bars on the data points of this figure indicate the range of uncertainty associated with the coherence length calculations rather than a range of observed grain sizes. The coherent lengths (i.e., mean grain size) of the crystals were deduced from the Scherrer formula, as mentioned in section 3.3.1, assuming a single crystal size throughout the film. These calculated results shown in Fig. 5.3 are in very good agreement with the size shown by the cross sectional TEM image of an as-deposited sample (Fig. 5.4). TEM also showed that the grains were columnar through thickness. Figure 5.3 shows that at a given temperature, the changes in grain size with annealing time are small. The grain size increased from ~ 8 nm to

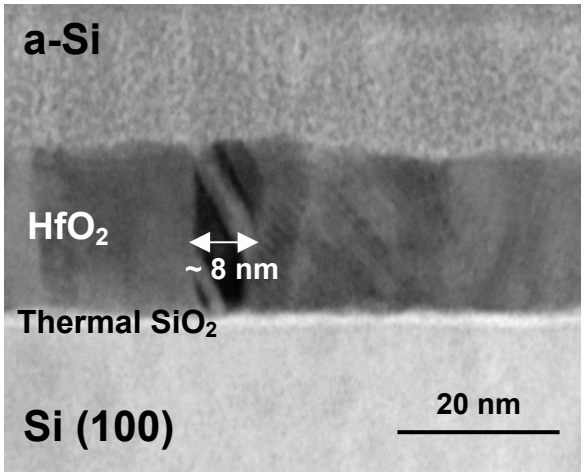

Fig. 5.4 Bright field cross-sectional TEM image shows the large, ~ 8 nm, columnar grains in the as-deposited ALD HfO_2 film on thermal SiO_2. The height of the grain spans the entire film thickness

approximately 9 to 10 nm after annealed at 400ºC, but there is no substantial changes in grain size occur upon further increased in annealing temperature. Only a very small increased in grain size (from ~10.5 nm to ~11 nm) was observed after a long anneal of 24 hours at 900ºC. This behavior with anneal time (at a given temperature) indicates that

grain growth is not kinetically-driven, but rather that the average grain size saturates relatively quickly with time at a given temperature. The crystallization fraction of the samples, however, shows a different behavior. A significant increase in the area under the peak was observed with increasing anneal temperature, but it is important to note that the average grain size did not substantially increase for higher temperatures and longer times. This behavior suggests that grain growth in this system is thermally-activated, and that increasing the thermal energy of the system serves to crystallize a larger fraction of the amorphous phase. It is interesting to see that even as more of the amorphous phase crystallized, the grains grow to the same average size, without any significant increase of existing grains. There was no significant change in the integrated areas upon annealing at 900ºC for > 24 hours, suggesting that the films had become fully crystallized.

Another interesting finding was that the types of underlayer have a significant effect on the degree of the crystallinity of the ALD HfO_2 films. Figure 5.5 shows the

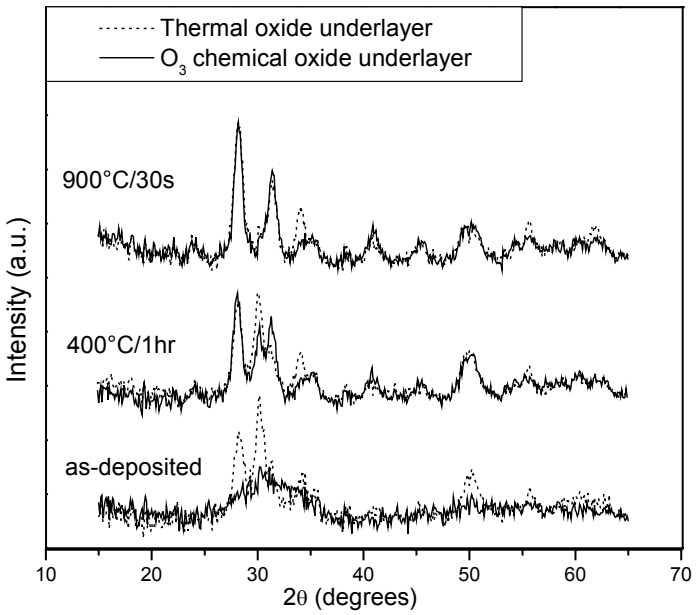

Fig. 5.5 XRD patterns from 20 nm ALD HfO_2 films grown on a thermal oxide underlayer (dotted line) and a chemical oxide underlayer (solid line).

effect of two different underlayers (thermal and chemical oxide) on the crystallinity of the as-deposited ALD HfO_2 films and the evolution of the films during annealing. The two films were deposited using the exact same procedure. It should be noted that the XRD results obtained from these two films were *not* scaled to match each other. The degree of crystallinity was significantly lower in the as-deposited ALD HfO_2 films on a chemical oxide underlayer than in the films grown on a thermal oxide underlayer. The amorphous nature of the film deposited on the chemical oxide is evident in the cross-sectional, dark field STEM image shown in Fig. 5.6. There are no visible grains in the film, which suggests that it is amorphous. However, in ADF-STEM, an amorphous material should

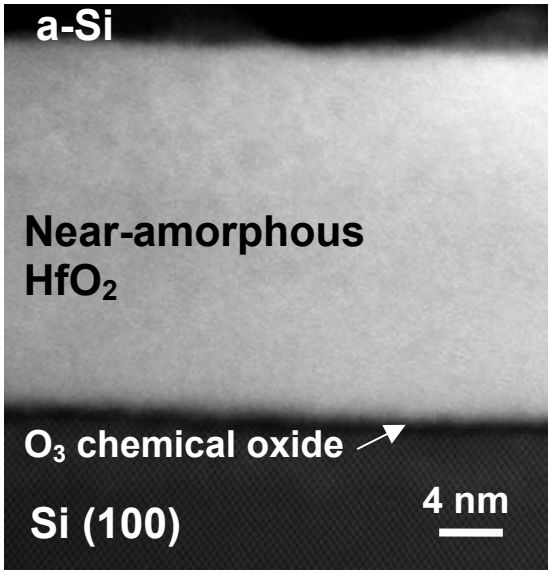

Fig. 5.6 Annular dark-field scanning transmission electron microscope image (Z-Contrast STEM) of a 20 nm thick as-deposited ALD HfO_2 film on a chemical oxide underlayer. The amorphous state of HfO_2 is clearly shown.

show no contrast since it is not using a coherent imaging mode as in high-resolution TEM (examples can be found in Refs. 7 and 8). The slight speckle pattern observed in the HfO_2 films in Fig. 5.6 suggests that the HfO_2 films are not fully amorphous. A convergent beam electron diffraction [9] pattern (not shown) from the same sample shows disc-like features, but they are not fully formed and they do not exhibit crystalline symmetry. This indicates that this sample has some degree of intermediate-range order with small (~ 1 nm or less) crystal-like clusters.

Although the reason behind the influence of the underlayer on crystallinity is not well understood, one can suppose that it could be due to the difference in nucleation density on the surface of the two underlayers. We have pointed out in the previous chapter that there are more –OH groups (surface sites) on the chemical oxide surface than on the thermal SiO_2 surface [10 – 12]. Ihanus *et al*. [13] have found a similar observation where substrate material had an effect on the ALE process. They suggested that fewer nucleation sites may enable nucleation and growth of separate grains for some time before coming into contact (i.e., before grain coalescence). On a substrate where the nucleation density is high (i.e., chemical oxide in this case), films growth leads to a more amorphous structure, because nearly every $HfCl_4$ that comes into contact with the oxide surface forms a chemical bond immediately, and therefore does not allow for much surface diffusion (required for crystal formation), because the entire monolayer is formed before crystal order can be achieved [13, 14]. Also note that this argument only holds if the growth does not proceed at thermal equilibrium. At the deposition temperature of 300ºC, the growth may indeed be kinetically controlled and thus, atomic motion is limited [15].

In these experiments, no study was performed on thermally grown SiO_xN_y underlayer. It might be expected that HfO_2 films grown on SiO_xN_y will behave similarly to those grown on thermal SiO_2 underlayer since both thermal SiO_2 and SiO_xN_y result in similar growth behavior, as shown in chapter 4.

XRD patterns from the as-deposited films on chemical oxides primarily show the broad maxima characteristic of an amorphous sample with a very weak peak near $2\theta = 30.4^{\circ}$ (solid line in Fig. 5.5). This indicates the presence of a very small crystalline fraction in the orthorhombic or tetragonal phase. STEM investigates only a small region of the film and might have missed a very low density of crystals. Despite the difference in the as-deposited structure, HfO_2 deposited on both chemical and thermal SiO_2 underlayers yield similar kinetics of transformation to the monoclinic phase, as the peak intensity of both films increased up to the same height and FWHM upon annealing at a given temperature for a given time.

5.1.2 Hf-aluminates

An investigation of the thermal stability of the amorphous phase was performed on the $(HfO_2)_x(Al_2O_3)_{1-x}$ films containing Al cation fractions of approximately 25%, 50%, and 75%. The specific approach by which these compositions were estimated will be discussed in the next section. This section presents the results obtained from blanket Hf-aluminate films (~ 200 Å) deposited on thermal SiO_2. The details of the sample preparation have been described in 3.2.1 (part B). It should be noted that Hf-aluminate films were also deposited on chemical SiO_2. However, compared to the case of thermal SiO_2, there was

no significant difference in the crystallization onset temperatures observed. Therefore, only results from films deposited on thermal SiO_2 are presented in this section.

Figure 5.7 shows the XRD patterns from Hf-aluminate films annealed over a range of different temperatures and times. Two observations that show the effectiveness in increasing the thermal stability of the amorphous phase by alloying HfO_2 with Al_2O_3 are as follows: (1) the as-deposited films for all three compositions are amorphous, and (2) the

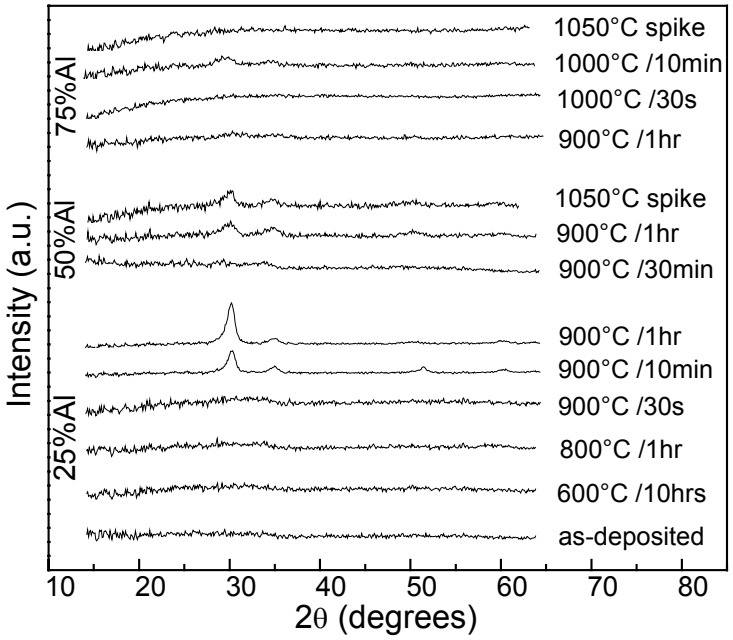

Fig. 5.7 XRD scans obtained from annealed films with various Al fractions show significant improvement in the stability of the amorphous phase as the percentage of Al increases. Note that the composition with 75% Al remains amorphous after a 1050ºC spike anneal.

onset of crystallization increases from 900ºC-10 min for the sample with 25% Al to 900ºC-1 hr for the sample with 50% Al. The sample with 75% Al remains amorphous up to a spike anneal at 1050ºC (soak time < 1 s). For 25% Al, annealing above 900ºC for 10 min yields clear crystalline peaks. It is evident from Fig. 5.7 that an amorphous phase could be retained over a range of $(HfO_2)_x(Al_2O_3)_{1-x}$ compositions (which correspond to

acceptable dielectric constants [16]) under processing conditions that would satisfy the present source/drain dopant activation requirements (~ 900-1000ºC; 10 s). For example, a film with 50% Al can retain its amorphous phase up to a 900ºC-30 min anneal and yet have a dielectric constant of ~13 [16], which is about three times higher than that of the conventional SiO_2 gate dielectric ($\kappa = 3.9$).

5.2 Tailoring the Compositions of Hf-aluminate Films

5.2.1 Introduction

The ability of the atomic layer deposition technique to produce films with precise thickness control, as well as excellent uniformity and conformality, has made this technique a leading manufacturable candidate for depositing high-κ oxides. As already mentioned in chapter 1, ALD is capable of preparing both *mixed* and *nanolaminate* films. As demonstrated by many research groups [17-19], controlling the composition and thickness of a multilayer structure (nanolaminate) is relatively easy since the number of ALD cycles will determine the thickness, while each sublayer would have their corresponding oxide composition. To date, however, utilizing the unique features in the ALD technique (self-limiting submonolayer-by-submonolayer growth) to tailor the compositions of *mixed* Hf-aluminate films has not been described in the literature. In this study, excellent control over a wide range of mixed Hf-aluminate compositions ranging from Hf cation fractions of 20% up to 100% (measured by MEIS) was achieved using a suitable choice of the ratio between the Al and Hf precursor pulses.

Referring back to chapter 3, blanket Hf-aluminate films with a series of different Al to Hf precursor pulse ratios (samples A to E) were deposited on *p*-Si substrate – the details of the deposition procedure have been listed in Table 3.3. The *x*-*y*-*z* notation that will be used later throughout this discussion is explained as follows: one *bilayer* consists of *x* H_2O / TMA cycles, followed by *y* H_2O / $HfCl_4$ cycles. The total number of *bilayers* is represented by *z*.

5.2.2 Results and Discussion

Figure 5.8 shows the MEIS spectra for samples A through E listed in Table 3.3 (chapter 3). As expected, the area under the Hf peak increases with the total number (equal to the product of *y* and *z*) of H_2O / $HfCl_4$ cycles, corresponding to an increasing amount of Hf in the film. However, samples D and E were both deposited using the same

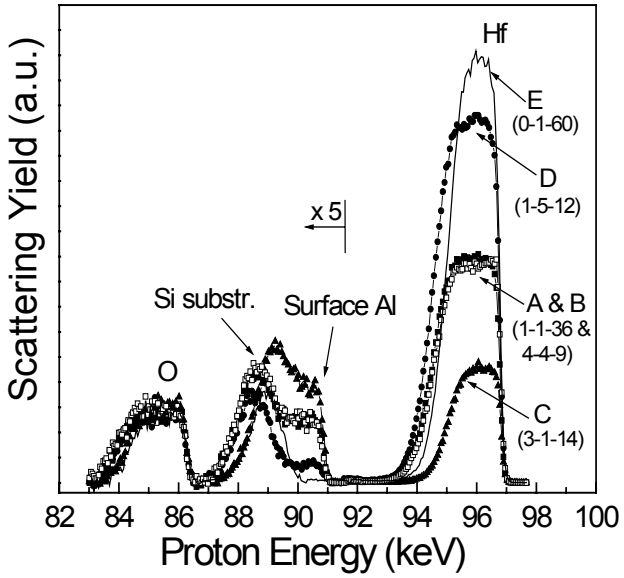

Fig. 5.8 MEIS proton backscattering spectra obtained from as-deposited Hf-aluminate films (samples A to E).

total number of H_2O / $HfCl_4$ cycles, i.e., 60 cycles, yet integration of the areas under the respective Hf peaks shows that sample D contains approximately 8% more Hf than sample E. Because the sample and detector alignments during MEIS were arranged to ensure that no significant channeling in the oxide films occurred, this indicates that there is an increased incorporation of Hf per cycle when Al_2O_3 is present in the film. This behavior could arise if the presence of Al_2O_3 enhances the sticking probability of $HfCl_4$ to the film surface, or reduces the steric hindrance effect of $HfCl_4$ on the surface of the film.

The suggestion that the presence of Al_2O_3 facilitates an increased Hf incorporation into the films is supported by the following observations. For a fixed number of Hf cycles (36 cycles), samples A (1-1-36), B (4-4-9), and a sample with 6-6-6 cycles consistently have 8-13% more Hf than the pure HfO_2 (0-1-36) sample. (The samples with 6-6-6 and 0-1-36 cycles are not shown in Fig. 5.8). This shows that the effect of Al in enhancing Hf

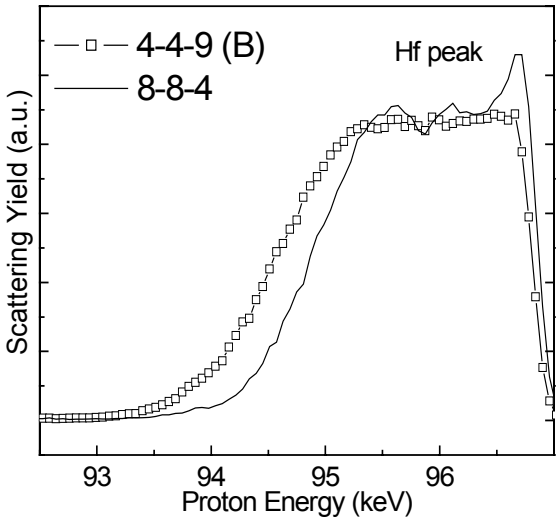

Fig. 5.9 MEIS proton backscattering spectra showing only the Hf peak for sample B, and a sample with 8-8-4 cycles. Oscillations in the Hf peak are only clearly observed in sample 8-8-4, indicating that full bilayer intermixing persists for samples with bilayers at least up to 4 cycles of each oxide.

incorporation is still being effective when there is more than 1 cycle being pulsed in each layer. The enhancement in samples that have ≥ 1 cycle pulsed in each bilayer (e.g., sample B) is only possible if bilayer *intermixing* (described later) occurs. Even though all three samples (A, B, and 6-6-6) that have Al presence consistently contain more Hf than the sample without Al (i.e., sample 0-1-36), there is, a continuous decrease in Hf coverage between samples A, B, 6-6-6, and 0-1-36. This is because the relative enhancement of Hf incorporation per cycle decreases as the number of cycles in each

HfO_2 layer is increased (i.e., as subsequent Hf cycles become further removed from the underlying Al_2O_3 layer).

The intermixing effect in the ALD is illustrated in Fig. 5.9. The smooth top surface of the MEIS peak of sample B shows clearly that full bilayer intermixing continues to occur for samples with bilayers up to 4 cycles of each oxide. The sample with 8-8-4 cycles clearly exhibits oscillations in the Hf peak, indicating distinct HfO_2 and Al_2O_3 regions. It should be noted that even the sample with 8-8-4 cycles does not contain fully segregated layers, as intermixing of Hf and Al still occurs on a scale of ~ 5 Å (based on simulations of the ion scattering data). It can therefore be concluded that complete intermixing did occur in both samples A and B, which made the significant Hf enhancement possible.

The intermixing effect can be explained by considering a phenomenon called "backfilling" of precursors. This backfilling can occurs for several cycles in the ALD process. For any given metal precursor pulse, such as $Al(CH_3)_3$, steric hindrance from the ligands, in this case CH_3, of each precursor molecule prevents neighboring surface sites from reacting. The subsequent H_2O pulse then reacts with these ligands, replacing them with smaller OH ligands, thus making the neighboring surface sites available for reaction. The next metal precursor pulse, therefore, "backfills" or intermixes with the previous metal pulse by reacting with sites on the same monolayer plane in the film. This phenomenon can occur for up to at least four cycles (Fig. 5.9). For the case of sample B, all four consecutive $HfCl_4$ pulses react (or "backfill") with the same underlying Al_2O_3 layer, but the fourth $HfCl_4$ intermixes less than the first pulse. Although the same backfilling mechanism can occur for a pure HfO_2 film (e.g., sample E), the fact that the

aluminate samples show increased Hf incorporation for the *same* total number of $HfCl_4$ pulses indicates that the presence of Al_2O_3 layers enhances the incorporation of Hf per cycle. Although it is not fully understood why the backfilling mechanism with Al_2O_3 is more effective at incorporating Hf, one possibility is that the methyl (CH_3) ligands on Al are much larger than the chlorine (Cl) ligands on Hf, such that the CH_3 ligands initially block out more neighboring bond sites in a given Al layer compared to a corresponding Hf layer. This would cause a more significant backfilling effect for Al, where many subsequent metal precursor pulses (either $Al(CH_3)_3$ or $HfCl_4$) could continue to react within the underlying Al_2O_3 layer once the CH_3 ligands are replaced by OH.

The calculated fraction of Al in the films shown in Table 5.1 was estimated using equation 3.2, described in chapter 3. No incubation period was considered between

Table 5.1 Percentage of Al in the films (calculated from separate HfO_2 and Al_2O_3 growth rates and densities) agrees well with the experimental data obtained from MEIS. Results also show that ellipsometer (the manufacturable tool) is able to obtain a reasonably accurate film thickness.

Samples *(x-y-z)**	Calculated Al fraction (%)	Measured Al fraction[a] (%)	Simulated thickness[a] (Å)	Ellipsometric thickness[b] (Å)
1-1-36 (A)	62.7	59.5	45	45.1
4-4-9 (B)	62.7	60.3	45	46.2
3-1-14 (C)	83.5	81.2	38	35.1
1-5-12 (D)	25.2	21.4	43	46.6
0-1-60 (E)	0	0	32	37.7

[a]Results from MEIS

[b]Measured using the index of refraction, n=2.08

* x: number of H_2O / TMA cycles, y: number of H_2O / $HfCl_4$ cycles

z: total number of repetitions of x-y pair

different pulses and this assumption is supported by the fact that samples A and B (both having a total of 36 H_2O / $HfCl_4$ cycles) have a very similar measured composition. One

can see that even with this simple approach to calculation, a very good agreement is obtained between the calculated and measured Al fraction. The same table also shows that by using an ellipsometer, a tool utilizable in a manufacturing environment, it is possible to obtain a reasonably accurate film thickness. The ability to accurately measure the films thickness with ellipsometer fulfills one of the practical requirements of integrating Hf-aluminate films into a CMOS process.

A very well-behaved, linear relationship between the Hf cation fraction in the film and the ratio of $HfCl_4$ / (TMA + $HfCl_4$) cycles is shown in Fig. 5.10. The Hf fraction calculated using equation 3.2 (chapter 3) was also shown in the same figure for

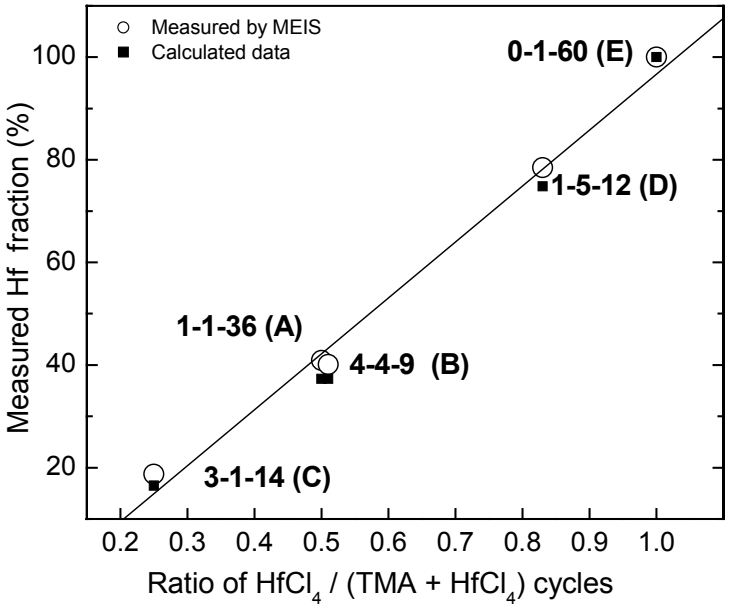

Fig. 5.10 A linear relationship exists between the Hf fraction in the film and the ratio of $HfCl_4$ / (TMA + $HfCl_4$) cycles, providing a useful guideline for attaining desired compositions of the Hf-aluminate films. The closed symbol is the calculated Hf fraction using equation 3.2.

comparison. Considering this extremely predictable growth behavior, the composition of $(HfO_2)_x(Al_2O_3)_{1-x}$ ALD films can clearly be tailored to the desired stoichiometry using a manufacturable deposition technique simply by fixing the Al/Hf cycle ratio.

5.3 Summary

Hf-based oxides as a possible candidate for alternative gate dielectric materials were physically investigated in this section. Specifically, the phase transformation kinetics of HfO_2, and the stability of the amorphous phase of Hf-aluminate films were studied. It was clearly shown that as-deposited ALD HfO_2 films grown on thermal SiO_2 are polycrystalline. Subsequent heat treatments were found to develop a relatively large grain size of about 10 nm, even after a short anneal at 900ºC, which is comparable to the gate length of future sub-100 nm MOSFETs. This result supports the idea of utilizing polycrystalline materials as alternative gate oxides. Unlike HfO_2, as-deposited ALD Hf-aluminate films are amorphous, and the ability of these films (with 25% Al) to remain amorphous up to 900ºC may be desirable for gate applications since the anticipated thermal budget in CMOS integration is in the range of 900ºC – 1000ºC, with annealing time ranging from < 1 s to 30 s. It is worthwhile to note here that "thermal budget" involves both time and temperature where can be defined as the amount of time the wafer is at particular temperature during the whole annealing process. One should keep in mind, however, that thermal stability is only one of the many requirements that need to be considered when selecting the proper candidates for replacing SiO_2. The price to pay

for adding Al into the HfO_2 films is the lower dielectric constant and higher oxide fixed charge, which will be described in the following section. Nevertheless, it is still too early to speculate which of these candidates is the better choice.

Attention has also been given to the effect of the underlayer on the crystallinity of the as-deposited ALD HfO_2 films. As-deposited ALD HfO_2 films on chemical oxide underlayers are amorphous (or < 1 to 2 nm grain size), while deposition on thermal oxide underlayers leads to polycrystalline films. Although this behavior is not yet well understood, this information is of considerable importance for obtaining a better understanding of thermal stability, which is a critical CMOS scaling issue.

This experiment has also demonstrated a new and practically achievable method to tailor the compositions of the mixed Hf-aluminate films using ALD. Hafnium aluminate films deposited by ALD have been obtained over a wide range of compositions with excellent control of both film stoichiometry and thickness. By using proper ratios between the Al and Hf precursor pulses, extremely predictable Hf-aluminate compositions were obtained, with Hf cation fractions ranging from 20% up to 100%, as measured by medium energy ion scattering. The Hf-aluminate results can serve as a guideline to other workers for obtaining ALD Hf-aluminate films with a desired composition and thickness.

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CHAPTER 6:

ELECTRICAL PROPERTIES OF Hf-BASED DIELECTRICS

In the previous section, the physical properties of the blanket HfO_2 and Hf-aluminate films were discussed. In this section are presented the electrical properties of the MOS capacitors containing these high-κ materials. The capacitors were fabricated using a conventional MOS process flow, as described in section 3.2.2. It is well known that post-deposition annealing (PDA) is essential to improve gate dielectric film quality (reducing the oxide charge that causes ΔV_{FB}, and thus a shift in threshold voltage) and to reduce leakage current of the high-κ gate stacks [1-3]. However, *non-optimized* PDA conditions can cause an undesirable increase in EOT due to diffusion of oxygen through the high-κ films to the Si substrate where it reacts to form additional SiO_2. Therefore, attention is given in this study to developing a detailed understanding of the effect of different PDA temperatures, times, and ambients on ΔV_{FB}, EOT, and J_G.

In this work, an ultrathin (~ 5 Å) intentional interfacial oxide was present between the high-κ material and Si. As already described in chapter 4, this underlayer is necessary to ensure well-behaved ALD film growth. The requirement of this layer is not a drawback of the ALD method because almost all of the film growth processes investigated to date end up forming interfacial SiO_2 anyway, either during high-κ film growth or during subsequent annealing [4, 5].

Following PDA, which was performed immediately after high-κ film deposition, all the samples were subjected to additional annealing for 30 min in *forming gas*

(10%H_2 / N_2) at 400°C as the last step in the process flow (see section 3.2.2). It has been shown by Onishi *et al*. [6] that this treatment on HfO_2 gate stack is efficient at reducing the interfacial state density. It is also worth pointing out here that the forming gas anneal is a typical processing step already in use in state-of-the-art CMOS technology [7].

Negligible frequency dispersion was observed, especially in the depletion region, upon comparison of the high frequency *C–V* curves measured at 10 kHz, 100 kHz, and 1 MHz. This indicates that there was negligible presence of interface traps, which would have reacted only at lower frequency (in this case, 10 kHz) and thus caused dispersion. This may be due to the effective removal of the interface traps by the forming gas anneal. Since results obtained from a large number of samples were essentially independent of frequency, only the 100 kHz *C–V* curves are shown in this section.

One of the other concerns of high-κ dielectrics is the *C–V* hysteresis, because of its effects on V_{FB} instability, which results from charge trapping. The *C–V* hysteresis was determined by measuring the change in V_{FB} after sweeping the gate voltage back and forth from +2/-2 V four times. A small hysteresis (< 20 mV at V_{FB}) was observed in all cases; therefore, it is neglected in the remaining discussion.

6.1 HfO_2 Gate Stack with the Conventional n^+ Poly-Si Gate Process

For the ALD process, the presence of hydroxyl groups (OH) on the sample surface is very important for yielding a uniform, high-quality film on Si. The results described in chapter 4 showed that chemical oxide underlayers are able to yield a highly predictable, well-behaved growth with no incubation period. On the other hand, thermal SiO_2 and SiO_xN_y underlayers, which are typically used for high-κ stacks, show some degree of nonlinear growth for the first ~ 10 Å. HfO_2 grown on both types of underlayers exhibits a better growth behavior compared to the H-terminated case. In this chapter, electrical properties of films grown on both thermal and chemical oxides will be reported. The most attention, however, will be given to films grown on the underlayer that yielded the most predictable growth behavior, i.e., the chemical oxides. N_2 and O_2 are commonly

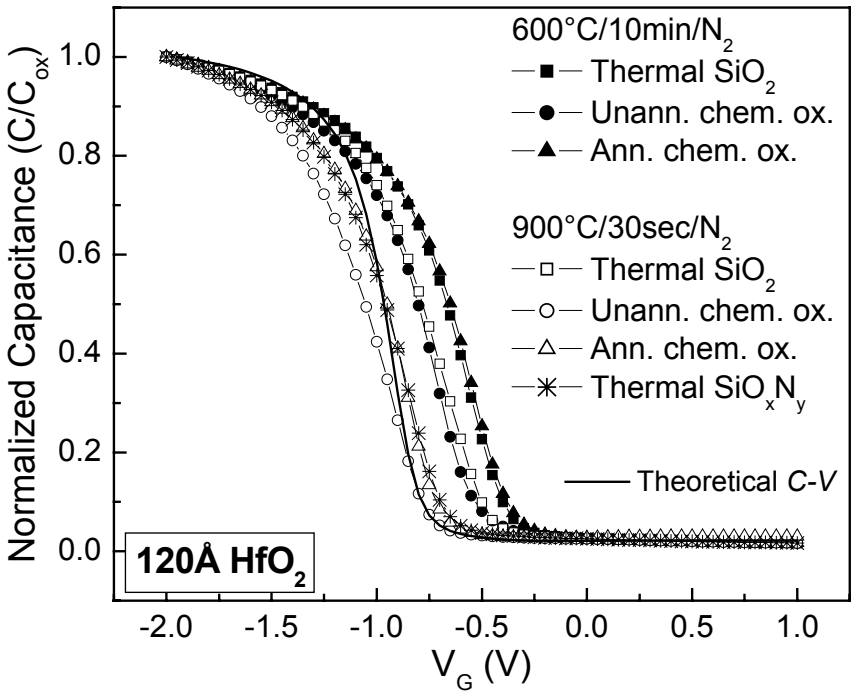


Fig. 6.1 900°C/30 s anneals greatly reduce ΔV_{FB} and N_f, especially for chemical oxide underlayers.

used as ambients during subsequent processing steps such as source/drain activation anneal, interlayer dielectric deposition, and poly reoxidation [7]. These gases would be the most practical PDA ambients because CMOS processing systems are already equipped to handle them. The literature also shows that annealing SiO_2 in nitric oxide (NO) results in lower leakage current and interface densities compared to annealing in N_2O [8]. Thus, in this study, PDA was performed under all three different ambients: N_2, O_2, and NO.

Figure 6.1 shows the *C–V* curves, normalized against the oxide capacitance (C_{ox}), for 120 Å HfO_2 films deposited on various ~ 5 Å thick chemical oxide, thermal SiO_2, and thermal oxynitride underlayers. One of the chemical oxide underlayers had been annealed at 800°C for 10 min in N_2 ambient prior to ALD deposition. The figure also compares the effect of different underlayers in two different PDA conditions. The theoretical *C–V* curve is the curve that would be obtained if there was no fixed charge in the film. The details on generating this curve have been described in section 3.3.5. Assuming that the ΔV_{FB} is entirely due to a fixed charge (since, as mentioned earlier, there was a negligible interface trap charge observed), equation 6.1 [3] below can be used to extract the fixed charge density N_f in the film, defined as $N_f = Q_f / q$, where Q_f is the number of charges in the films. In equation 6.1, Φ_{ms} is the work function difference between the poly-Si gate and the *p*-Si substrate, C_{ox} is the dielectric capacitance, and *q* is the charge constant (= 1.6×10^{-19} Coulomb). This equation is used with the assumption that the centroid of the fixed charge distribution is located ***at*** the oxide/Si interface [3].

$$V_{FB} = \Phi_{ms} \pm \frac{Q_f}{C_{ox}} \tag{6.1}$$

Results from Fig. 6.1 show that films grown on unannealed chemical oxide underlayers consistently yield a smaller ΔV_{FB} (= V_{FB} - Φ_{ms}) for both 600°C and 900°C PDAs, since the *C–V* curves are nearer to the theoretical *C–V* curve. It should be noted, however, that low temperature annealing at 600°C has much smaller impact on reducing the ΔV_{FB}, compared to the high temperature anneals (900°C/30 s). By using equation 6.1 above, one finds that 900°C/30 s anneal results in a lower N_f for chemical oxide than thermal oxide, with $N_f \sim 5 \times 10^{11}$ cm^{-2} versus $N_f \sim 1 \times 10^{12}$ cm^{-2}, respectively. The same effect of high temperature annealing on reducing fixed charge was also observed with physically thinner 40 Å HfO_2 films (Fig. 6.2) deposited on chemical and thermal oxides, where the 900°C/30 s again greatly reduces the $|\Delta V_{FB}|$ to less than 30 mV, with $N_f \sim 2 \times 10^{11}$ cm^{-2}.

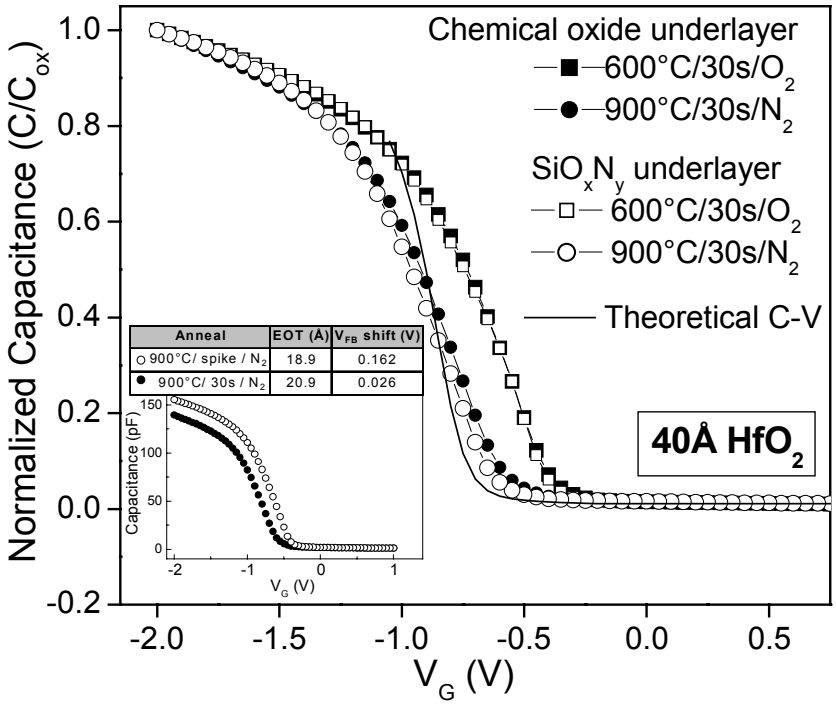


Fig. 6.2 The effect of 900°C/30 s anneals for reducing ΔV_{FB} and N_f is scalable to 40 Å HfO_2. The inset shows that a slight growth in interfacial layer seems to be necessary to reduce the ΔV_{FB}, in addition to high temperature anneals.

Figure 6.3 shows the leakage current densities, J_G for 900°C anneals on HfO_2 films of several thicknesses deposited on chemical and thermal oxides (EOT ~ 17-24 Å). The J_G obtained from a control sample with 30 Å SiO_2 as the gate oxide is also included in this figure for comparison. The results show that for a fixed EOT and bias condition, HfO_2 gate stacks yield significantly lower J_G than conventional SiO_2 gate stacks. For example, at V_G = -1.0 V, J_G obtained from 60 Å HfO_2 (EOT~ 20 Å) gate stack (~ 10^{-9} A/cm^2) is reduced by ~ 10× compared to that of SiO_2 (~10^{-8} A/cm^2) with an even *higher* EOT of ~ 30 Å. Figure 6.3 also shows that both chemical and thermal oxide underlayers yield comparable J_G. A more detailed discussion on leakage current will be presented later in this section using Fig. 6.10.

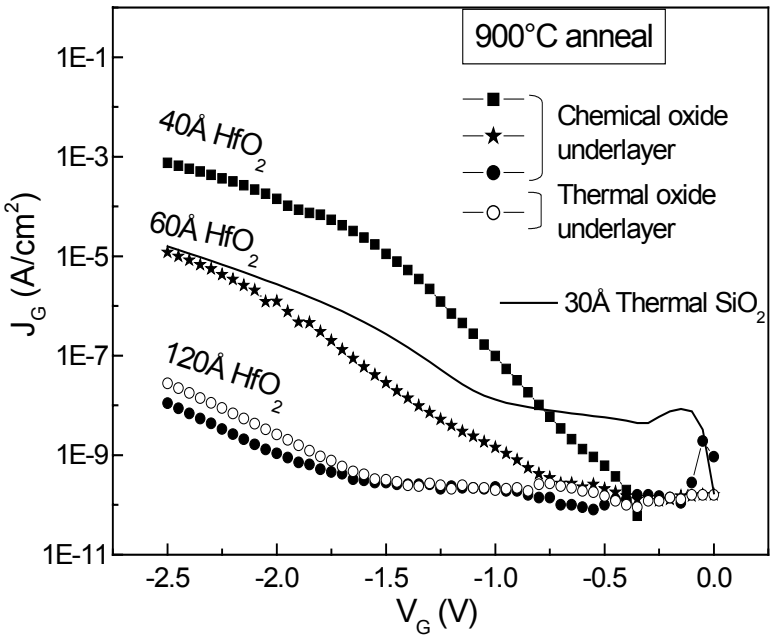


Fig. 6.3 Low leakage currents for chemical oxides with various HfO_2 thicknesses (EOT ~ 17-24 Å).

It can be seen from Fig. 6.1 that for 120 Å HfO_2 films, chemical oxides underlayers yield a better V_{FB} control than standard thermal oxides/oxynitrides, and yet yield comparable J_G. Note, however, that for thinner HfO_2 films (Fig. 6.2), samples with

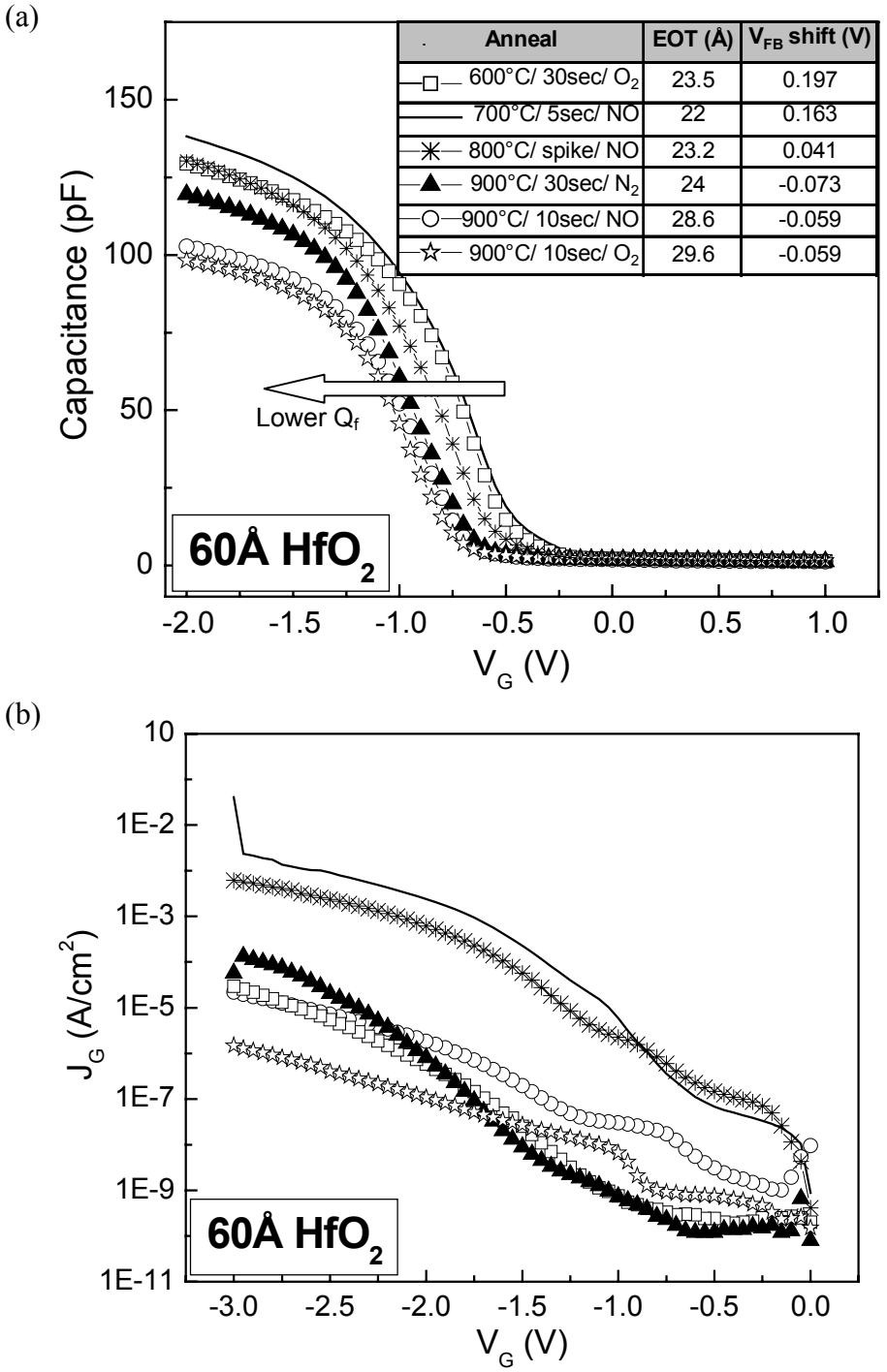


Fig. 6.4 Effect of different PDAs on *C–V* curves (a), and the corresponding leakage density characteristics (b) for 60 Å HfO_2 gate stacks.

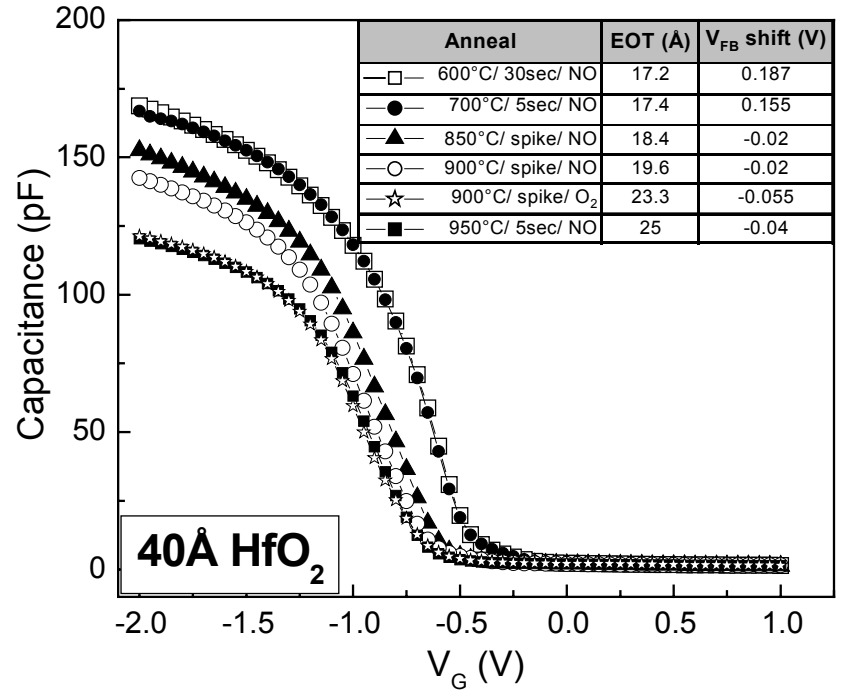
chemical oxide underlayers provide V_{FB} control equivalent to that of oxynitride underlayers. Because chemical oxide underlayers yielded V_{FB} and J_G as good as or better than those yielded by the thermal underlayers, and because chemical oxides also provides the best control of the growth process, the effect of various anneal temperatures, times, and ambients was further investigated using only the *chemical oxide* underlayer. The results are presented below.

In order to make sure that the trends associated with the shift in *C–V* curves presented here are material-dependent rather than thickness-dependent, three different physical thicknesses (30 Å, 40 Å, 60 Å) of HfO_2 were used for this further investigation. It should be noted that Figs. 6.4 to 6.6 only show representative *C–V* curves to illustrate the effect of different annealing conditions. The complete set of ΔV_{FB} data (including ΔV_{FB} data from the samples shown in Figs. 6.4 to 6.6) from these experiments will be shown later in Fig. 6.7 to support the observations and explanations given in this section.

Figure 6.4a shows the *C–V* characteristics of 60 Å HfO_2 films grown on ~ 5 Å chemical oxide. The inset in this figure displays the corresponding values of ΔV_{FB} and EOT (both extracted using the NCSU *C–V* fitting routine explained in section 3.3.5). The corresponding J_G–*V* characteristics are displayed in Fig. 6.4b. The *C–V* and J_G–*V* characteristics for thinner samples with 40 Å HfO_2 and 30 Å HfO_2 films are shown in Figs. 6.5 and 6.6, respectively.

Observing the *C–V* curves in Figs. 6.4a to 6.6a, it can be seen that regardless of annealing ambient, the interfacial oxide thickness increases (thus, EOT increases) with annealing temperature. Figure 6.4a shows that EOT increases from 22 Å to ~ 30 Å during

(a)



(b)

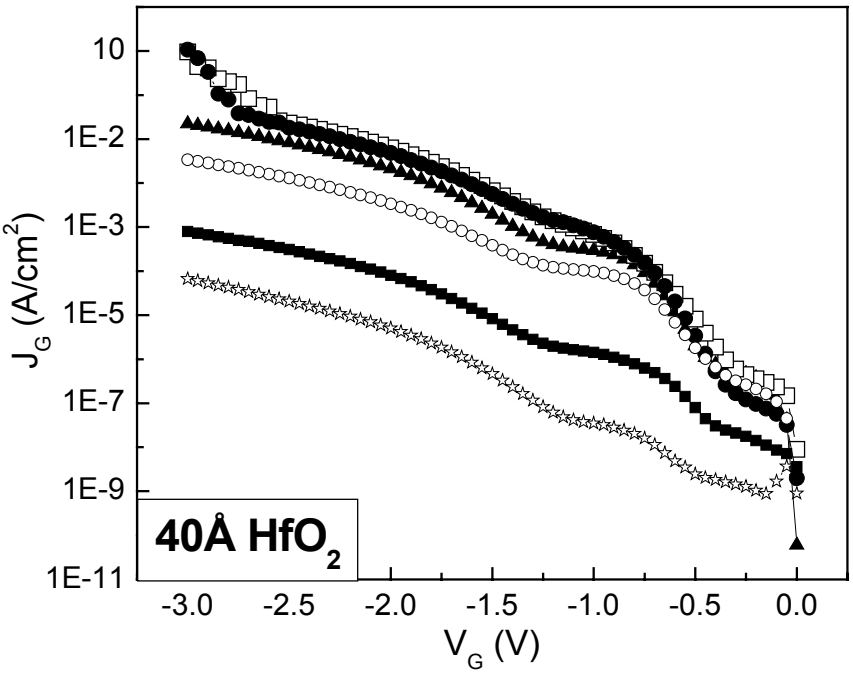


Fig. 6.5 Effect of various PDAs on *C–V* (a) and J_G–*V* (b) characteristics for 40 Å HfO_2 gate stacks.

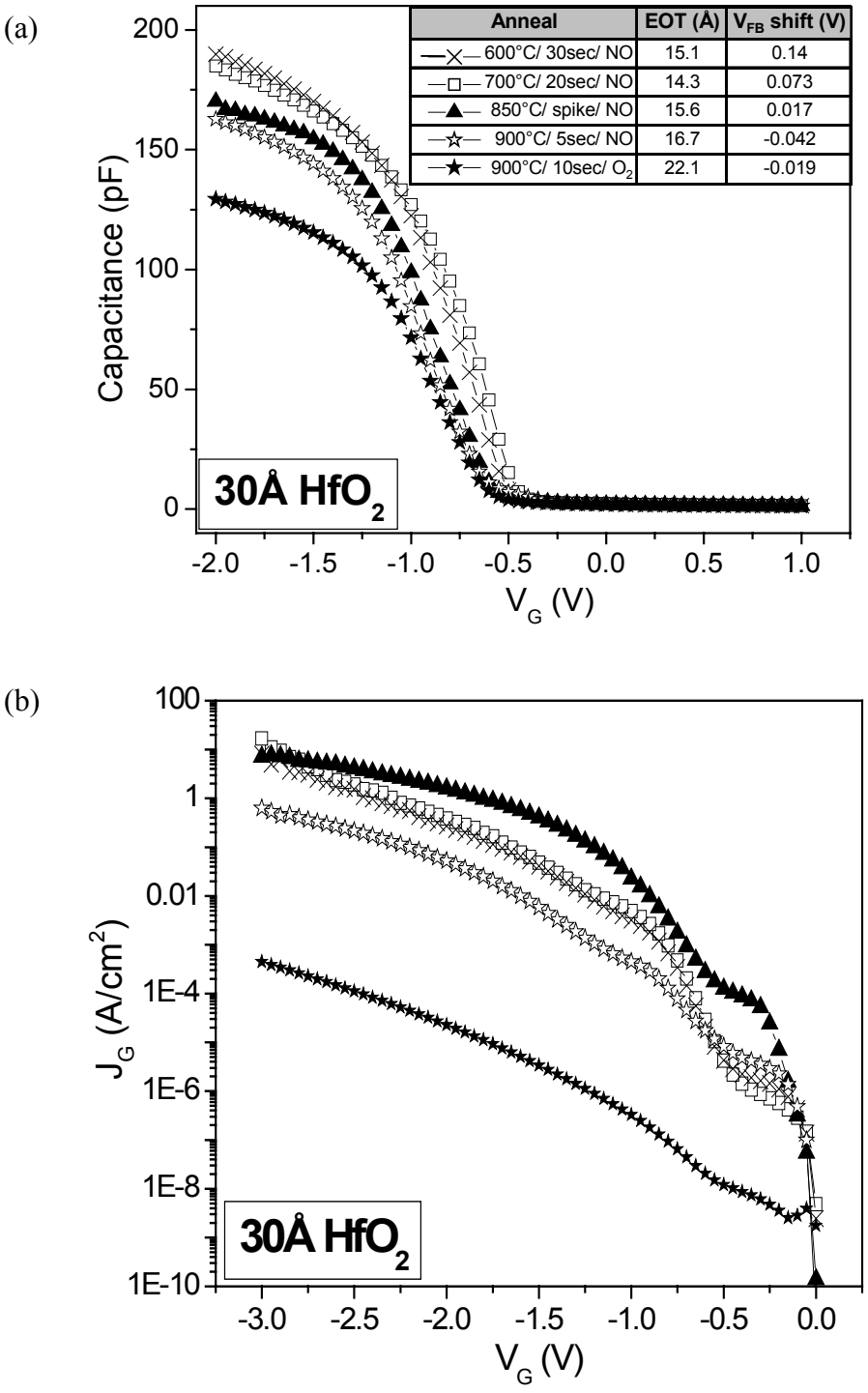


Fig. 6.6 Effect of various PDAs on *C–V* (a) and J_G–*V* (b) characteristics for 30 Å HfO_2 gate stacks.

annealing in O_2, when the annealing temperature increases from 600°C to 900°C, despite the fact that the sample at 600°C was annealed for a longer time than the sample at 900°C. Figures 6.5a and 6.6a shows similar observations for thinner HfO_2 films. Samples annealed in O_2 or NO ambient are more susceptible to increases in EOT, even at low temperature (600°C), compared to N_2 anneals. For example, the first three samples shown in Fig. 6.4a yield almost the same EOT as the fourth sample, which was annealed in N_2 ambient at a higher temperature. It is not surprising that O_2 and NO yield the larger increase in EOT because both contain oxygen. Among the three different ambients, O_2 anneals are most susceptible to interfacial oxide growth, which indicates that the O_2 ambient is able to introduce the most oxygen into a gate stack. An example of this behavior can be seen in Fig. 6.5a (compare the 900°C/spike/NO and 900°C/spike/O_2 anneals). It is believed that the increased in EOT observed in the case of N_2 anneal was due to oxygen introduced into films from O_2 impurities in the N_2 gas. In additional experiments (not shown) using de-oxygenated N_2 ambient, all capacitors were shorted, which indicates that the oxygen impurities in N_2 play a significant role in the system.

Another observation that can be obtained from all three figures (Figs. 6.4a to 6.6a) is that the *C–V* curves gradually shifted in a negative direction as annealing temperature increased from 600°C to 900°C. Even though this shift reflects the decrease in ΔV_{FB}, which is desirable, it comes at the expense of interfacial oxide growth. Figure 6.4a shows that ΔV_{FB} reduced from 197 mV down to 59 mV as the annealing temperature increased from 600°C to 900°C, while EOT increased from 22 Å to 30 Å. Similar trends were observed with 40 Å (Fig. 6.5a) and 30 Å (Fig. 6.6a) HfO_2 films where the ΔV_{FB} decreased from a few hundred mV to a few tens of mV in each case (while EOT

increased) as the annealing temperature increased from 600°C to 900°C. However, it should be noted that the *C–V* curves do not continuously shift in a negative direction with increasing EOT (or more accurately, increasing interfacial oxide growth since the physical thickness of HfO_2 films is the same in each figure). The last three samples in the inset of Fig. 6.4a show that EOT increased from 24 Å to 30 Å, but that the ΔV_{FB} remained at ~ 60 mV to 70 mV. The last three samples in the inset of Fig. 6.5a again show a similar trend, where ΔV_{FB} tends to remain approximately unchanged even though the EOT increased from ~ 20 Å to 25 Å.

The results from all these observations do, nevertheless, suggest that there is a correlation between ΔV_{FB} and interfacial oxide growth. In order to obtain a clearer picture of the correlation between these two parameters, the ΔV_{FB} obtained from all the samples used in this experiment were plotted against the interfacial oxide growth: the results are

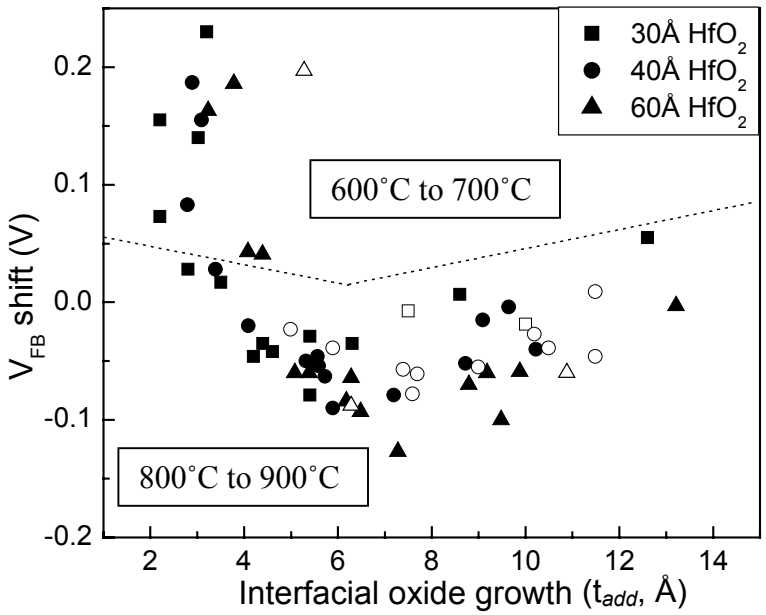


Fig. 6.7 High temperature anneals (≥ 800˚C) and ~ 4-5 Å additional interfacial oxide growth are necessary to reduce the ΔV_{FB}. Consistent results are obtained for (30 Å, 40 Å, 60 Å) HfO_2 films annealed in various temperatures and times, either in NO (filled symbols) or O_2 ambient (open symbols). The dotted line separates the samples annealed in two ranges of temperatures, 600°C – 700°C and 800°C – 900°C.

shown in Fig. 6.7. The results in Fig. 6.7 were obtained from samples having three different films thickness: 30 Å, 40 Å, and 60 Å, which are represented in the figure by squares, diamond, and triangle symbols, respectively. For each HfO_2 film thickness, samples were annealed either in NO or O_2 ambient. Samples annealed in NO are represented in the figure by closed symbols; samples annealed in O_2 are represented by open symbols. Samples were annealed in two ranges of temperatures, 600°C – 700°C and 800°C – 900°C; a dashed line in the figure separates the samples annealed at 600°C – 700°C from those annealed at 800°C – 900°C. The longer the annealing time at a given temperature, the higher the interfacial oxide growth. It is worth mentioning again that all these samples were deposited on the chemical oxide underlayer and are the *same* samples shown in Fig. 6.4 to 6.6.

From this figure, it can be seen that annealing temperature has a greater effect on the reduction of the ΔV_{FB} (thus, fixed charges), as compared to the annealing ambient or time. The low temperature 600ºC to 700ºC anneals yield the *highest* ΔV_{FB} values (100 – 200 mV) in both O_2 and NO ambients, which correspond to negative fixed charge on the order of $N_f \sim -10^{12}/cm^2$. Also shown in Fig. 6.7, annealing at lower temperature (600ºC to 700ºC) is able to reduce ΔV_{FB} only slightly, even though it results in an amount of interfacial growth similar to that sometimes obtained with high temperature annealing (800ºC – 900ºC). Similar behavior was observed regardless of annealing time and ambient.

A few other observations can be made from Fig. 6.7. Firstly, a very systematic shift in V_{FB} from positive to negative was observed when the additional interfacial oxide thickness increased to 4-5 Å. Devices with only SiO_2 gate dielectrics show negative

ΔV_{FB} [10]. If we ascribe this positive-to-negative shift shown in Fig. 6.7 to the introduction of opposite (positive) charges by SiO_2, which compensate (but do not eliminate) the negative charges in HfO_2 films, the ΔV_{FB} should continuously shift to a negative value as the interfacial SiO_2 growth increases. The results shown in Fig. 6.7, however, indicate that ΔV_{FB} remains rather constant after 5-6 Å additional growth. This suggests that the mechanism of reducing the fixed charge in the film is not as simple as the compensation of charges. This in turn is beneficial because if there is a large amount of fixed charge at the interface, and the ΔV_{FB} is reduced due to charge compensation, then the mobility of the FET will still be poor because the charges still remain to scatter electrons in the channel.

Secondly, it can also be seen that lowering ΔV_{FB} does not solely depend on the amount of interfacial oxide growth, but has a strong dependence on annealing temperature too. For a given amount of interface growth, upon comparing samples annealed at 600ºC – 700ºC and at 800ºC – 900ºC, it is clear that ΔV_{FB} significantly improved from a few hundred milivolts to a few tens of milivolts with high temperature (≥ 800ºC) anneals. These shifts represent negative fixed charge levels of $N_f < -10^{11}/cm^2$, which is ~ 10× lower than most values reported previously for various high-κ films [9, 11]. One can finds additional support for observations (1) and (2) in Fig. 6.5a, Fig. 6.6a and the inset of Fig. 6.2.

One possible explanation for the observations seen in Fig. 6.7 is as follows: hydroxyl groups (OH) may have been introduced during ALD deposition (during pulsing H_2O) or during exposing films to air prior to post-annealing. Assuming the positive net shift in V_{FB} (negative fixed charge) arises from the OH^-, annealing at high temperature

liberate the –OH groups, thereby removing the negative fixed charge, but at the same time increases EOT as the OH^- diffuses to SiO_2/Si interface and reacts with Si to form SiO_2. A continued increase in interfacial oxide without a further decrease in the ΔV_{FB} is to be expected since HfO_2 is extremely susceptible to oxygen diffusion [9].

It was found that, within the limit of accuracy of the ΔV_{FB} measurements (as mentioned in section 3.3.5, V_{FB} obtained from the *C–V* curve fitting may contain some

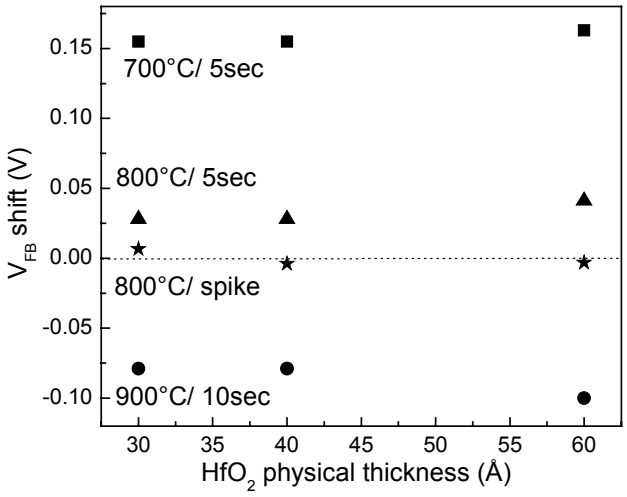


Fig. 6.8 The weak dependence of the ΔV_{FB} to the HfO_2 films thickness, suggesting that the centroid of the charges is not be *at* the HfO_2/SiO_2 interface

errors due to factors such as series resistance, gate depletion, and/or quantum mechanical effects), the ΔV_{FB} had negligible dependence on the physical thickness of the HfO_2 films. Figure 6.8 shows data obtained from a few selected samples deposited on a chemical oxide underlayer that have been annealed in NO or O_2 ambient at three different temperatures (700ºC – 900ºC) to illustrate this fact. Although not every single capacitor in this experiment showed the exact same behavior (some scattered data were observed) that may due to experimental error, considering a large number of samples did show the same trend, the results are convincing. It is also worth mentioning here that a similar

trend was observed for samples deposited on the thermal oxide underlayer. Referring back to the concept of where the ΔV_{FB} being charge position-dependent, explained in section 2.5.2, it can be suggested that the charges are *neither* located *at* the HfO_2/SiO_2 bottom interface nor *at* the poly-Si/HfO_2 top interface. Moreover, this thickness-independent behavior shown in Fig. 6.8, also indicates that the charges that contribute to the ΔV_{FB} are not uniformly distributed in the bulk, since if such were the case, the ΔV_{FB} would increase with physical thickness. Qualitatively similar behavior has actually been observed by Torii *et al.* [12], for ALD Al_2O_3 gate dielectrics, where the ΔV_{FB} remained somewhat unchanged when Al_2O_3 film thickness increased from ~ 10 Å to 35 Å. In order to explain the observed ΔV_{FB} as a function of anneal condition and HfO_2 thickness in Fig. 6.8, it is most likely that the –OH groups are concentrated in a fixed distance from the top HfO_2 interface. This observation is consistent with the X-ray photoelecton spectroscopy (XPS) spectra shown in Busch *et al*. [13], where the Al 2p peak (from Al_2O_3 film in that case) in XPS is shown to have a shoulder associated with Al-OH bonding, and angle-resolved XPS measurements showed that the –OH groups are located in the top ~1 nm of the film.

However, here may also be other effects giving rise to defects and charge in these structures. Recent work by Hobbs *et al*. [14] explained a Fermi level pinning effect at the top of HfO_2/poly-Si interface. It was proposed that a small fraction of the Hf atoms at that interface can form Hf-Si bonds, which produce a defect state in the bandgap of Si. There would be a high density states of this defect, such that the Fermi level of the poly-Si can get pinned at that defect level. In this case, different applied voltages would not be able to move the Fermi level, and would result in the observed ΔV_{FB} (observed in both

NMOS and PMOS devices). This newly suggested phenomenon illustrates the complexity and lack of fundamental understanding of the high-κ gate dielectric stacks.

In addition, work by Gusev *et al*. [15] showed that these high-κ films exhibit a much higher charge trapping density than SiO_2. Although the nature of these traps has not yet been identified, one possibility is oxygen vacancies. It has been known for a long time that these types of oxides contain a high equilibrium oxygen vacancy concentration ($>10^{18}$ cm^{-3}) [16]. Since oxygen vacancies in ceramics are known to act as shallow traps, it is possible that these inherent defects also contribute to the observed defect and charge observed in these films.

The dielectric constant of the HfO_2 films with n^+ poly-Si electrodes was determined from the slope of a linear fit to a plot of EOT (extracted from *C–V* characteristics) versus physical oxide thickness (Fig. 6.9). All three samples shown in Fig. 6.9 were deposited on the chemical oxide underlayer and annealed at 900ºC for 10 s in N_2 ambient. The physical thickness of the HfO_2 film was measured using an

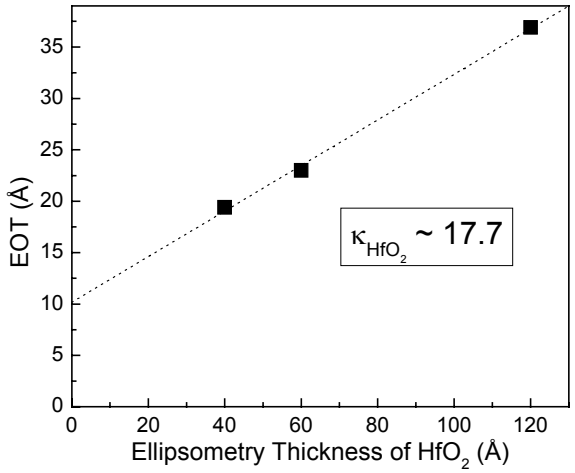


Fig. 6.9 EOT of ALD HfO_2 films grown on chemical oxide (annealed at 900°C/10 s) as a function of ellipsometric thickness yield an effective dielectric constant of ~ 17.7.

ellipsometer assuming a refractive index ~ 2.08 (see Appendix B), while the electrical EOT was corrected for quantum mechanical and gate depletion effects. The physical thicknesses of some of these samples were independently verified by TEM, and are within 2-3% of the nominally quoted values for the ellipsometric thickness. The effective dielectric constant, κ, was determined to be ~ 17.7, in agreement with the range of values (16-20) given in the literature [17-19]. Note that the κ values ranged from 16-19 were obtained in this experiment depending upon processing conditions, likely due to variation of interfacial layer thickness. The value 17.7 was used to calculate the additional interfacial oxide growth, t_{add} [= EOT – $t_{i/f}$ – ($\kappa_{SiO2}/\kappa_{HfO2}$) t_{phys}], shown in x-axis in Fig. 6.7. The term $t_{i/f}$ represents the as-deposited thickness of the oxide underlayer deposited prior to high-κ deposition (in this case, $t_{i/f}$ ~ 5 Å), and t_{phys} is the physical thickness of the HfO_2 films. The terms κ_{SiO2} and κ_{HfO2} are the dielectric constants of SiO_2 (3.9) and HfO_2 (17.7) films, respectively. The y-intercept of the linear fits represents the interfacial oxide thickness, and, of course, an assumption was made that the amount of increase in interfacial oxide for all three samples was the same. However, this may not be the case if interface growth is controlled by oxygen diffusion through the film.

Figure 6.10 displays the leakage densities, J_G measured at 1 V beyond V_{FB} for HfO_2 films with three different physical thicknesses (30 Å, 40 Å, and 60 Å). Each data point represents a unique PDA condition with various annealing temperatures (ranging from 600ºC up to 1000ºC) and times (ranging from 5 s to 30 s, including spike anneal). The chemical oxide underlayer data points (closed symbols) have been extracted from Figs. 6.4, 6.5, and 6.6, but presented in this format so that overall performance of HfO_2 films can be seen. In this figure, the HfO_2 data is compared with SiO_2 data from the

literature [17], which is linear fit by the solid line. Data from samples with thermal SiO_xN_y oxide underlayer (open symbols), which is not shown in Figs. 6.4, 6.5, and 6.6 are also included for comparison. The physical thickness of HfO_2 were translated into EOT using the formula mentioned in chapter 3, section 3.3.5, so that fair comparison can be made between samples with different physical thickness and also with conventional capacitor with SiO_2 as gate oxide. The gate leakage current is measured in the accumulation regime since a limited supply of minority carriers in a MOS capacitor structure may cause the measured J_G to be lower than the true value [20].

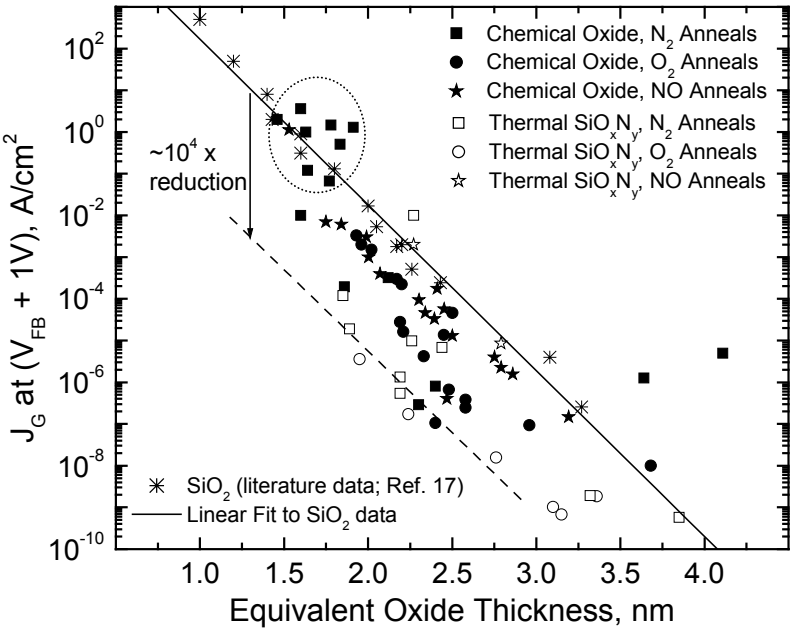


Fig. 6.10 The leakage densities for ALD HfO_2 gate stacks annealed to various temperatures (> 600ºC) and for various times. Plots are compared to the typical observed J_G for SiO_2 gate stacks (solid line), showing that reducing J_G by a factor of ~10^4 (marked by dotted line) is possible with properly chosen annealing conditions. The solid square data points in the dotted circle are the set of samples annealed in de-oxygenated N_2. The rest of the solid square data points denote samples annealed in house-N_2 that contains oxygen impurities.

Figure 6.10 indicates that properly chosen annealing conditions, HfO_2 gate stacks exhibit a reduction in J_G by a factor of ~10^4 compared to SiO_2 (see literature data for SiO_2 in Fig. 6.10) for the same EOT and bias conditions. This 10^4 decrease is represented by a dotted line in the figure. Many of the data points that fall on the dotted line are data from samples grown on thermal SiO_xN_y where the annealing temperatures varied from 600ºC to 900ºC, and annealing times varied from 30 sec for 600ºC to 5 sec for 900ºC. Samples with thermal SiO_xN_y underlayer can yield leakage densities comparable to or lower than samples with chemical oxide underlayer, but with the trade-off of higher ΔV_{FB} than that of chemical oxide underlayer (referring back to Fig. 6.1). A detailed list of the processing conditions used for the samples that fall on the dotted line (i.e., that result in lowest leakage current), can be found in Table D.1 of Appendix D. Samples with SiO_xN_y underlayer can yield leakage densities comparable to or lower than samples with chemical oxide underlayer, but with the trade-off of higher V_{FB} (i.e., higher fixed charge) than that of chemical oxide underlayer. Higher fixed charge in the gate dielectric is a critical show stopper since it reduces the mobility. It is worthwhile to mention that it is possible the leakage densities of the chemical oxide samples could be improved by further optimizing the annealing conditions. For this, however, further experimental work needs to be conducted.

A few very leaky samples (solid square symbols, circled with dotted line in Fig. 6.10), that have very low EOT (1.0 - 1.5 nm), are those samples that annealed in de-oxygenated N_2 conditions. Similar observation was obtained by Perkins *et al* [21] and Jeon *et al*. [22] from ZrO_2 samples annealed in vacuum. Oxygen loss by SiO evaporation is well established for thin SiO_2 films for temperatures between 700ºC to 1000ºC [23]. It

has been suggested in the literature [21] that annealing in an oxygen deficiency environment results in reduction of ZrO_2 since decomposed underlying SiO_2 removes oxygen from the ZrO_2. Thus, the presence of oxygen in the annealing environment may be essential even though there is a trade off of increasing EOT.

Amorphous gate maybe beneficial in terms of leakage path, however most metal oxides exhibit a strong tendency to crystallize. This is one of the motivation behind this work to study the both physical and electrical properties, and to find a correlation between them, if possible. In section 5.1 (Fig. 5.1), we saw that regardless of the underlayer used, ALD HfO_2 films achieved a similar degree of crystallinity upon annealing at temperatures as low as 400ºC. Several groups have suggested that crystallization can results in problem such as grain boundary leakage and non-uniformity in the k value and the film thickness [24, 25]. Since the lowest annealing temperature for samples that shown in Fig. 6.10 is 600ºC, all samples in this plot are considered have been crystallized. The fact that with properly chosen annealing treatment, very low leakage densities can be obtained, shows that amorphous gate *may not* be necessary to the meet gate leakage requirements for scaled CMOS. However, whether the crystallinity in the films is detrimental to device performance or reliability is still under scrutiny.

Unfortunately, there is no clear correlation can be made between various phases (monoclinic, orthorhombic, and tetragonal) observed in Fig. 5.1 and the electrical performance of the gate stack. The phase content shown in Fig. 5.1 was obviously mixed at low temperature. Even though the monoclinic phase become dominant at 900ºC, we do not believe that this is the reason behind having a lower ΔV_{FB}. More detailed

investigation to understand this correlation remains, however, beyond the scope of this study.

6.2 Hf-aluminates Gate Stack with the Conventional n^+ Poly-Si Gate Process

Amorphous high-κ gate dielectrics may be of interest for their potentially better device leakage and reliability [9]. We have seen in the previous section that alloying HfO_2 with Al_2O_3 significantly improved the stability of the amorphous phase. In this subsection, the electrical data on the ALD Hf-aluminate films will be presented.

Figure 6.11 shows the *C–V* characteristics and the corresponding leakage data for Hf-aluminate films with 75%, 60%, and 50% Al, using n^+ poly-Si gate electrodes. The films were all annealed at 900ºC for 10 s either in N_2 or NO ambient. The Al fractions in the films can be predicted quite accurately using the method developed earlier in section 5.2. Hf-aluminate films yield a lower J_G compared to pure HfO_2 films of similar EOT and under the same bias condition; however, the large ΔV_{FB} ~ 400 mV (Fig. 6.11a) observed even after high temperature (900ºC) anneals suggests that reducing the N_f in

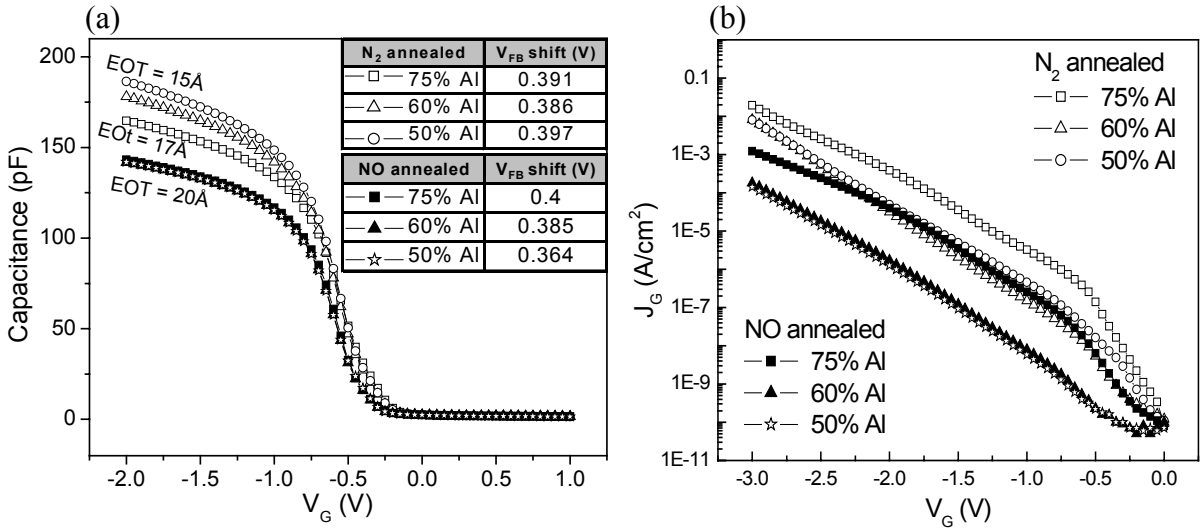


Fig. 6.11 (a) High temperature (900ºC/10 s) annealing leads to an increase in EOT, but has very little effect at lowering the ΔV_{FB}, and (b) films with 75%, 60%, and 50% Al exhibit a reduction in J_G by a factor of 10^2 to 10^4, compared to SiO_2 for the same EOT and bias conditions.

aluminates may be much more challenging than in the case of HfO_2. As expected, high temperature annealing increased the interfacial oxide thickness (thus, increasing EOT), but seemed to have very little effect on lowering the fixed charge. This behavior is consistent at three different Hf-aluminate compositions, as shown in Fig. 6.11a. Considering the results from the previous subsection on HfO_2 gate stacks, where high temperature anneals (900ºC) significantly reduced the N_f, this study shows that there is a technologically noticeable difference between HfO_2 and Hf-aluminate films. Although the reason for this behavior is not clear and cannot easily be resolved, this result provides valuable information for determining its applicability in MOS capacitors and MOSFETs.

The dielectric constant values for all three aluminate film compositions were estimated using samples annealed at 900ºC/10 s in NO ambients (Fig. 6.12).

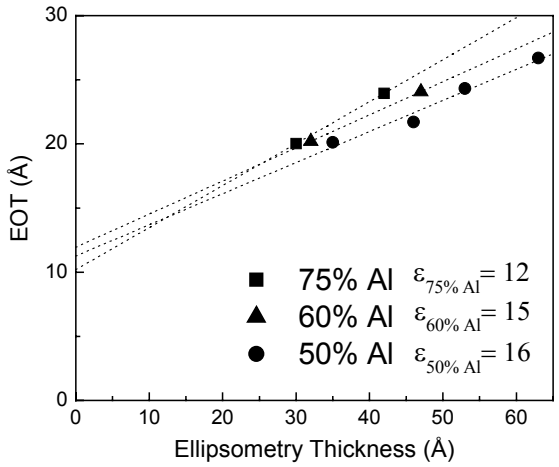


Fig. 6.12 The dielectric constant of Hf-aluminate films systematically decreases from 16 to 12 as the Al fraction in the films increases from 50% to 75%, as expected. The dotted lines are the linear fit of the measured data point.

Although the available experimental data for samples with 60% and 75% Al were not sufficient to determine the κ values very accurately, the result presented in this figure is only intended to show a systematic reduction in κ values with increasing Al content in

the films. This trend of decreasing in κ is expected since pure Al_2O_3 has a dielectric constant of only 9-10 [26]. Nevertheless, it is worth mentioning here that even with this rough estimation, the consistency of these estimated values is compelling, and very close to the values recently reported by Wilk *et al*. [11].

6.3 Summary

Atomic layer deposited HfO_2 and Hf-aluminate films as an alternative gate dielectric have been experimentally studied. Well-behaved *C–V* curves and leakage currents of ~10^4× lower than those of SiO_2 for the same EOT were achieved in this study, showing that HfO_2 and its aluminates are compatible with conventional poly-Si gate processing technology: new processing methods are not needed. High N_f is currently known to be the most critical problem in high-κ dielectric films, thus the results from this extensive study are of particular importance for advanced Si devices. First, we demonstrated that N_f in HfO_2 gate stacks can be reduced significantly down to a few tens of milivolts with optimized annealing conditions. The results of this study show that high temperature anneals (> 800ºC) are effective at reducing the ΔV_{FB} and achieving N_f as low as ~10^{11} cm^{-2} with a chemical oxide underlayer. This promising result indicates that ALD HfO_2 is compatible with the anticipated thermal budget (900ºC – 1000ºC) in current transistor process flow. The results also suggest that 4-5 Å interfacial oxide growth, together with high temperature anneals, may be necessary to minimize the ΔV_{FB}. It is suggested that the apparent decrease in N_f may be attributed to the elimination of the OH

groups, introduced during the ALD process. In contrast to HfO_2 films, Hf-aluminate gate stacks may have a higher thermal stability; however, the problem of ΔV_{FB} cannot be mitigated just by high temperature annealing.

It is always desirable that the films exhibit the lowest V_{FB} shift possible (to provide maximum mobility and thus device performance), yet yield a low enough J_G. HfO_2 films are able to yield a relatively low N_f without reducing much of the capacitance (i.e., not much increase in EOT). Aluminates (with κ >15) may be a viable alternate gate dielectric to Al_2O_3; however, the ΔV_{FB} has to be controlled before Hf-aluminate films can be seriously considered as replacements for SiO_2 as the gate dielectric. In short, the selection of a candidate gate material will not be complete until fixed charge, charge trapping, interface state density, and reliability similar to those of a Si/SiO_2 interface can be achieved.

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CHAPTER 7: SUMMARY AND CONCLUSIONS

The rapid, unrelenting gate oxide scaling has led to substantial work on alternative high-κ gate dielectrics. To date, however, there is no one single material that has emerged as an ideal replacement for thermally grown SiO_2. Among various high-κ materials that have been investigated, Hf-based dielectrics are currently the leading candidates to replace SiO_2 in deep sub-micron CMOS technology. An in depth analysis of both the physical and electrical properties of atomic layer-deposited HfO_2 and Hf-aluminate films was conducted in this work.

HfO_2 and Hf-aluminates were deposited using ALD. This technique has recently received much attention due to its ability to deposit films with excellent conformality and step coverage, which is particularly difficult for other deposition methods when high aspect ratio features are concerned. Some of the striking capabilities of ALD include large area uniformity, accurate and simple film thickness control, and good reproducibility. As the industry's focus shifts towards bringing this technique into production, ALD is destined to be the deposition method of choice for CMOS technology in the near future.

This work began with an investigation of the growth behavior of ALD HfO_2 films on various underlayers. At this point in time, the presence of an interfacial oxide layer between ALD high-κ films (especially HfO_2) and Si substrate seems to be needed in order to form a quality gate stack that will yield a functional and well-behaved device. Understanding the dependence of film growth on various underlayers and the controlling the formation of the underlayer are therefore very important for the successful

implementation of ALD high-κ dielectrics in the future devices. It was found that the use of a chemical oxide underlayer enables HfO_2 to grow at a constant density, with a linear growth rate of about 0.86 Å/cycle. Growth on H-terminated Si, on the other hand, exhibits a large barrier to nucleation and growth, resulting in rough, and non-linear growth. Growth on thermal oxide/oxynitride underlayers falls in between these two extremes, resulting in a small nucleation barrier and non-linear growth for small HfO_2 coverages. The use of chemical oxide underlayers clearly results in the best HfO_2 layers. Furthermore, the ability that was demonstrated in this work to grow chemical oxides as thin as ~ 5 Å will afford researchers the opportunity to study high-κ gate dielectric scaling below 1.0 nm EOT.

We have seen that as-deposited ALD HfO_2 films on thermal oxides are polycrystalline with a mixture of monoclinic and either tetragonal or orthorhombic phases. The monoclinic phase predominates as the annealing temperatures and times increase, with the grain size reaching ~ 10 nm, even after a short anneal at 900°C. The relatively large grain size is comparable to the gate length of future sub-100 nm MOSFETs: thus, the large grain sizes could be used to test the idea that using a polycrystalline film with a grain size greater than or equal to the gate length may eliminate the variations in the effective dielectric field experienced by the charge carriers in the channel. ALD HfO_2 deposited on *chemical* SiO_2 are amorphous or very-fine grain (~ 1 nm) nanocrystaline, as evidenced by both XRD spectra and TEM images. Further experiments are required to elucidate the structural details. Films deposited on both chemical and thermal oxide underlayers exhibit similar monoclinic-phase formation kinetics upon annealing.

Because the scientific community is still debating over the reliability of polycrystalline films as gate oxides, it is worthwhile investigating the Hf-aluminate films, since alloying HfO_2 with Al_2O_3 greatly improves the thermal stability of amorphous Hf-aluminates. It was shown that Hf-aluminate films with Hf:Al ~ 3:1 (25% Al) remain amorphous up to 900°C, while films with 75% Al remain amorphous even after a 1050°C spike anneal. Since the anticipated thermal budget in CMOS integration is in the range of 900°C – 1000°C, it is very likely that Hf-aluminate films such as those shown in this study will retain their amorphous phase throughout the CMOS process. The results of this study also demonstrate an excellent composition control over a wide range of Hf-aluminate compositions, ranging from Hf cation fractions of 20% up to 100%. Both the stoichiometry and thickness of the films can be controlled accurately by altering the ratio of Al and Hf precursor pulses. These practically achievable results can serve as a guideline to others for obtaining ALD Hf-aluminate films with a desired composition, thickness, and degree of crystallinity. A knowledge of how to control the composition and thickness of Hf-aluminate films is a major requirement for their integration.

Successful fabrication of functional capacitors using both HfO_2 and Hf-aluminate gate dielectric films with n^+ poly-Si electrodes using a conventional CMOS process flow was demonstrated. Focus was given to the fundamental understanding of the issues pertaining to the ΔV_{FB}, which is an indication of the presence of fixed charges in the film. This undesirable charge has deleterious effects on transistor performance, causing carrier scattering and therefore low carrier mobility. Until this charge can be reduced to acceptably low levels, high-κ materials will not be able to replace SiO_2. It was found that for HfO_2 film gate stacks on a chemical oxide underlayer, high temperature anneals

(800ºC – 900ºC) are effective at reducing the ΔV_{FB} down to 10-20 mV, corresponding to N_f as low as ~10^{11} cm^{-2} with chemical oxide underlayer. The results from this work also suggest that 4-5 Å interfacial oxide growth may be necessary to minimize the $\Delta V_{FB,}$ in addition to high temperature anneals. In short, chemical oxides demonstrated a better control than thermal oxides/oxynitrides for achieving predictable, high-quality growth of ALD HfO_2 films with a low fixed charge. The appropriate combination of chemical oxide and post-annealing minimizes both fixed charge and interfacial oxide growth in ALD HfO_2, and should be applicable to most high-κ materials. The dielectric constant of HfO_2 has been experimentally determined as 17.7, and this is about 4.5× higher than that of SiO_2 (κ = 3.9), which means that it can afford a gate oxide with a physical thickness 4.5× thicker than SiO_2 for the same EOT. Greater physical thickness while maintaining a low EOT is an essential requirement for achieving a low leakage current in CMOS devices.

While the amorphous Hf-aluminates have a better thermal stability, their benefits are presently offset by the presence of large fixed charge in the films unlike with HfO_2 films. A brief survey of these films found that films annealed at high temperature (900°C in either NO or N_2 ambient) show ΔV_{FB} ~ 400 mV, which is significantly higher than that for HfO_2 films annealed in the same conditions. In any case, Hf-aluminate films exhibit a lower gate leakage current compared to pure HfO_2, possibly due to the amorphous phase that eliminates the electrical and mass transport along the grain boundaries. The J_G–V characteristics of Hf-aluminate gate stacks with n^+ poly-Si gate show a significant reduction in leakage current density, J_G of 10^2 to 10^4×, compared to SiO_2 of the same EOT (16 Å) and bias conditions.

The information presented in this study is clearly of vital importance for judging the possibilities of Hf-based materials and for providing a vision of their use in CMOS technology in the future. It is not an easy task, however, to justify choosing one of the Hf-based materials over another as there are many aspects to consider. Both HfO_2 and its aluminates have certain advantages, but they also have some disadvantages. Indeed, there is no real "winner" for all applications. For low power logic (mainly for portable applications), the reduction of gate leakage current to reduce power dissipation is an important issue, but for other applications such as microprocessor unit products, improving the carrier's mobility and thus the device speed (not power dissipation) is the primary issue. Although several problematic material issues associated with HfO_2 have been identified, encouraging results were achieved in this work. These include the ability to reduce the ΔV_{FB} down to tens of milivolts (corresponding to a very low N_f in the order of 10^{11} cm^{-2}) and achieving a negligible level of hysteresis with properly chosen annealing conditions. Furthermore, the results suggest that regardless of the crystallinity of the film, achieving a leakage currents as low as 4 orders of magnitude lower than those of conventional SiO_2 films of the same EOT is possible. Since there are concerns about the increase in leakage current related to the presence of grain boundaries in the crystallized films, this result will likely influence the focus of future research activities. The effect of the inclusion of Al into HfO_2 is clear: with an increase in the crystallization temperature and a lower leakage current, however, the ability to reduce the fixed charge is still questionable. Why high-temperature annealing has little effect at reducing the flatband shift in Hf-aluminate films, as opposed to HfO_2 films, however, remains unclear.

Thus, a more detailed study of the possible ways to engineer the flatband shift of this film is required.

Although at this point in time, the integration of Hf-based materials into manufacturing remains to be proven, this study has provided experimental data that are essential to the development of a scalable solution for the successful implementation of these materials into the CMOS processes. Several other important issues that will dictate the schedule of their implementation, such as reliability and dopant diffusion from the gate electrode to the substrate, require further study.

APPENDICES

A. Wafers Cleaning Chemistry

The well-known RCA wet clean processes have been used extensively since the 1970s in semiconductor manufacturing. Two sequential cleaning solutions are used in conventional RCA cleaning: SC1 and SC2. Details can be found in C.Y. Chang and T. S. Chao, *Wafer-Cleaning Technology*, in: *ULSI Technology*, Ed. C. Y. Chang and S. M. Sze (McGraw-Hill, New York, 1996).

In this work, the cleaning sequence has been slightly modified to obtain a wafer surface that is free from particles and organic contaminant and at the same time, to minimize the surface microroughness. All the wafers used in this work begin with the SOM and SC1 cleaning sequence (Table A.1) before being treated with HF solutions to remove native oxides.

Table A.1 Cleaning step to produce ultraclean Si surface prior to being treated with HF solutions to remove native oxides.

Cleaning step	Chemistry	Temperature (ºC)	Dipping time (s)
SOM	1) H_2SO_4 (98%) / O_3 / H_2O 2) De-ionized water rinse	Room Temperature Room Temperature	600 120
SC1	200 H_2O : 4 H_2O_2 (30%) : 1 NH_3OH (29%)	45	600

B. Film Thickness Measurements Using Ellipsometer

Tabulated values of the optical constant can easily be found in the literature. However, the fabrication of the less well-known materials such as HfO_2, Hf-aluminates and Al_2O_3 is not reproducible enough to use the tabulated values directly. Therefore, in this work, the values of refractive index, *n* and the extinction coefficients, *k* for various oxides were measured experimentally (using a ThermalWave Opti-Probe™ spectroscopic ellipsometer) to obtain a precise and accurate film thickness.

Table B.1 below lists the values of *n* and *k* for various oxides. These values were obtained using a two layer film stack: thick oxide film (> 20 nm) deposited on top of 1 nm SiO_2 with single crystal Si(100) as the substrate. Since the optical constant for the two known materials, Si and SiO_2 are well established in the literature, the tabulated values found in *The American Institute of Physics Handbook* (McGraw-Hill, New York, 1963) were used.

Table B.1 Measured optical constant for various films. Values listed for SiO_2 and Si are tabulated values obtained from handbook.

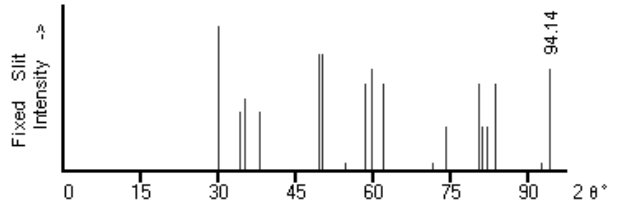
Target Film	**Refractive Index, *n***	**Extinction Coefficient, *k***
Al_2O_3	1.66	0
HfO_2	2.08	0
SiO_2	1.485	0
Poly Si (phosphorous doped, unactivated)	4.49	0.085
Poly Si (phosphorous doped, activated)	3.92	0.065
Aluminates	2.08	0
ZrO_2	2.10	0
Si	3.42	0.01

C. ICDD Card Files

The Powder Diffraction File™ (PDF) is a collection of single-phase X-ray powder diffraction patterns, maintained and distributed by the International Centre for Diffraction Data (ICDD). The data for each pattern are presented in the form of a table of diffracted angle 2θ (or characteristic interplanar spacings) and corresponding relative intensities. Miller indices and other supplemental data, such as crystal system, density, or cell information are also listed in this table. Identification of an unknown phase or material can be attained by a systematic comparison of measured XRD spectra and the standard patterns. For the purposes of this work, three cards corresponding to tetragonal, monoclinic, and orthorhombic HfO_2 are attached in this section.

Table C.1 Card number: 08-0342, standard patterns for tetragonal HfO_2

08-0342 Quality: O CAS Number: Molecular Weight: 210.49 Volume[CD]: 138.70 Dx: 10.080 Dm: Sys: Tetragonal Lattice: Primitive S.G.: $P4_2/nmc$ (137) Cell Parameters: a 5.14 b c 5.25 α β γ SS/FOM: F14=2(0.169, 41) I/Icor: Rad: CuKa Lambda: 1.542 Filter: Ni d-sp: Non-Ambient Temperature	Hf O2 Hafnium Oxide Ref: Curtis et al., J. Am. Ceram. Soc., 37, 458 (1954)

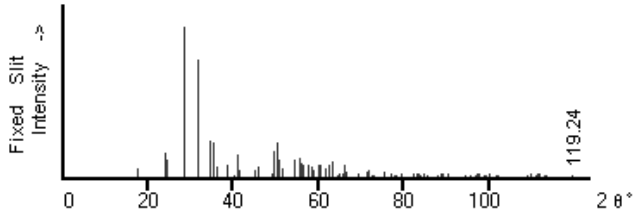


2θ	Int-f	h	k	l	2θ	Int-f	h	k	l	2θ	Int-f	h	k	l
30.092	100				54.813	5				80.441	60	3	1	3
34.201	40	0	0	2	58.496	60				81.345	30			
35.127	50	2	0	0	59.744	70	3	1	1	82.272	30	2	0	4
38.204	40	1	0	2	61.999	60	2	2	2	83.843	60	4	0	2
49.632	80	2	0	2	71.791	5	0	0	4	92.649	5	2	2	4
50.394	80	2	2	0	74.076	30	4	0	0	94.141	70	4	2	2

Table C.2 Card number: 34-0104, standard patterns for monoclinic HfO_2

34-0104 Quality: *
CAS Number: 12055-23-1
Molecular Weight: 210.49
Volume[CD]: 138.28
Dx: 10.111 Dm:
Sys: Monoclinic
Lattice: Primitive
S.G.: $P2_1/a$ (14)
Cell Parameters:
a 5.285 b 5.181 c 5.115
α β 99.259 γ
SS/FOM: F30=129(.0061, 38)
I/Icor:
Rad: CuKa1
Lambda: 1.5405981
Filter: Graph
d-sp: diffractometer

Hf O2
Hafnium Oxide
Ref: Natl. Bur. Stand. (U.S.) Monogr. 25, 20, 54 (1983)

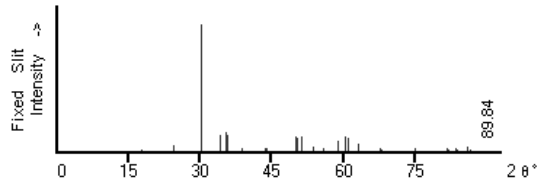


2θ	Int-f	h	k	l	2θ	Int-f	h	k	l	2θ	Int-f	h	k	l
17.544	6	0	0	1	63.265	11	1	1	3	83.653	3	$\bar{3}$	3	2
24.185	16	1	1	0	64.484	2	3	2	0	83.887	2	0	4	2
24.597	12	0	1	1	64.676	3	2	3	0	84.485	3	1	3	3
28.336	100	$\bar{1}$	1	1	64.676	3	$\bar{3}$	2	1	84.485	3	$\bar{2}$	3	3
31.665	78	1	1	1	65.433	1	0	3	2	84.724	3	$\bar{1}$	4	2
34.358	25	2	0	0	65.784	3	$\bar{2}$	3	1	85.498	2	0	2	4
34.595	20	0	2	0	66.133	9	2	2	2	86.736	1	$\bar{4}$	0	3
35.534	23	0	0	2	66.133	9	0	2	3	87.534	<1	2	4	1
36.086	7	$\bar{2}$	0	1	66.318	4	$\bar{1}$	3	2	88.036	2	1	4	2
38.776	9	1	2	0	69.367	3	2	3	1	88.804	3	4	2	1
39.046	1	0	2	1	70.094	1	$\bar{3}$	2	1	89.207	3	3	1	3
39.691	<1	0	1	2	70.634	1	$\bar{3}$	2	2	89.992	1	$\bar{4}$	0	2
40.185	2	$\bar{2}$	1	1	71.520	4	$\bar{1}$	2	3	90.423	3	$\bar{3}$	1	4
40.971	15	$\bar{1}$	1	2	71.520	4	$\bar{2}$	2	3	91.317	1	1	2	4
41.401	5	$\bar{2}$	0	1	71.721	5	$\bar{4}$	0	1	92.023	1	2	0	4
41.628	5	$\bar{1}$	2	1	72.410	1	4	0	0	94.472	2	2	3	3
45.096	5	$\bar{2}$	1	1	72.565	2	$\bar{2}$	3	2	95.490	1	4	3	0
45.783	7	$\bar{2}$	0	2	72.967	2	0	4	0	95.699	2	$\bar{3}$	4	0
49.230	3	$\bar{2}$	1	2	73.151	1	3	1	2	95.868	1	$\bar{3}$	4	1
49.559	18	2	2	0	74.033	1	$\bar{2}$	1	3	96.851	2	$\bar{4}$	2	3
50.436	23	0	2	2	74.033	1	$\bar{3}$	1	3	97.228	3	2	4	2
50.868	12	$\bar{2}$	2	1	75.203	2	0	0	4	97.228	3	0	4	3
51.513	6	$\bar{1}$	2	2	75.560	4	1	4	0	97.367	1	$\bar{1}$	3	4
54.461	12	2	0	2	76.967	3	$\bar{1}$	1	4	97.723	3	5	1	0
54.461	12	0	0	3	77.437	<1	$\bar{1}$	4	1	98.198	<1	0	3	4
55.032	1	2	2	1	77.899	2	3	3	0	98.701	2	0	5	1
55.722	13	3	1	0	78.079	2	$\bar{3}$	3	1	99.423	2	0	0	5
55.914	10	$\bar{3}$	1	1	78.599	1	4	0	1	99.527	1	$\bar{4}$	3	2
56.246	9	0	3	1	79.188	<1	$\bar{4}$	1	2	100.14	3	$\bar{5}$	1	2
57.535	9	0	1	3	79.428	3	2	3	2	101.13	<1	$\bar{2}$	0	5
57.535	9	$\bar{1}$	1	3	79.428	3	0	3	3	101.55	2	4	3	1
58.225	7	$\bar{1}$	3	1	80.953	<1	3	2	2	102.24	2	$\bar{2}$	2	4
58.635	5	$\bar{2}$	2	2	81.179	<1	4	1	1	103.96	<1	$\bar{5}$	2	1
60.155	9	1	3	1	81.794	1	$\bar{2}$	2	3	106.90	<1	4	0	3
60.433	9	$\bar{2}$	0	3	82.125	3	$\bar{4}$	2	1	106.90	<1	0	5	2
61.759	6	3	1	1	82.776	<1	4	2	0	107.27	1	$\bar{2}$	5	1
62.350	8	$\bar{3}$	1	2	83.108	3	$\bar{3}$	3	1	108.92	2	1	1	5
63.265	11	1	1	3	83.653	3	$\bar{3}$	3	2	109.90	3	$\bar{4}$	3	3
64.484	2	3	2	0	83.887	2	0	4	2	109.90	3	0	2	5
64.676	3	$\bar{2}$	3	0	84.485	3	1	3	3	110.79	2	$\bar{2}$	5	1
64.676	3	$\bar{3}$	2	1	84.485	3	$\bar{2}$	3	3	111.17	3	$\bar{3}$	3	4
65.433	1	0	3	2	84.724	3	$\bar{1}$	4	2	111.72	3	$\bar{2}$	2	5
65.784	3	$\bar{2}$	3	1	85.498	2	0	2	4	111.89	3	$\bar{3}$	4	2
66.133	9	2	2	2	86.736	1	$\bar{4}$	0	3	112.86	2	$\bar{3}$	4	3
66.133	9	0	2	3	87.534	<1	2	4	1	113.18	2	$\bar{4}$	4	1
66.318	4	$\bar{1}$	3	2	88.036	2	1	4	2	113.91	1	$\bar{4}$	4	0
69.367	3	2	3	1	88.804	3	4	2	1	114.06	<1	$\bar{2}$	5	2
70.094	1	$\bar{3}$	2	1	89.207	3	3	1	3	117.76	1	5	1	2
70.634	1	$\bar{3}$	2	2	89.992	1	$\bar{4}$	0	2	117.88	1	4	2	3
71.520	4	$\bar{1}$	2	3	90.423	3	$\bar{3}$	1	4	119.24	2	3	2	4
71.520	4	$\bar{2}$	2	3	91.317	1	1	2	4	119.24	2	5	3	0
71.721	5	$\bar{4}$	0	1	92.023	1	2	0	4					

Table C.3 Card number: 81-0028, standard patterns for orthorhombic HfO_2

81-0028 Quality: C
CAS Number:
Molecular Weight: 210.49
Volume[CD]: 264.96
Dx: 10.553 Dm:
Sys: Orthorhombic
Lattice: Primitive
S.G.: Pbca (61)
Cell Parameters:
a 10.01 b 5.227 c 5.059
α β γ
I/Icor: 15.22
Rad: CuKa1
Lambda: 1.54060
Filter:
d-sp: calculated
ICSD # : 071354

Hf O2
Hafnium Oxide
Ref: Calculated from ICSD using POWD-12++, (1997)
Ref: Ohtaka, O., Yamanaka, T., Kume, S., Nippon Seramikkusu Kyokai Gakujutsu Ronbunshi, 99, 826 (1991)



2θ	Int-f	h	k	l	2θ	Int-f	h	k	l	2θ	Int-f	h	k	l
17.694	21	2	0	0	57.694	1	3	2	2	75.930	10	8	0	0
24.596	52	2	1	0	57.939	3	6	1	0	76.436	1	7	0	2
26.052	2	1	1	1	58.159	2	1	1	3	76.436	1	4	3	2
30.355	999 *	2	1	1	58.968	86	2	3	1	77.297	7	4	2	3
34.280	131	0	2	0	60.522	114	2	1	3	77.577	5	6	2	2
35.454	150	0	0	2	61.023	107	6	1	1	77.817	3	2	4	1
35.828	127	4	0	0	61.023	107	5	2	1	77.817	3	2	0	4
36.507	2	3	1	1	61.608	2	5	1	2	78.282	1	1	1	4
36.606	3	1	0	2	63.150	66	4	2	2	78.482	1	7	2	1
38.745	32	0	2	1	64.345	1	3	1	3	78.482	1	8	1	0
38.832	19	2	2	0	65.169	1	4	3	0	78.950	1	7	1	2
39.815	3	1	2	1	65.850	9	0	2	3	79.431	4	6	3	0
39.883	2	4	1	0	66.388	5	6	2	0	79.620	2	1	3	3
39.883	2	2	0	2	66.591	3	1	2	3	80.351	1	2	1	4
40.595	1	1	1	2	67.118	6	6	0	2	81.181	6	8	1	1
42.892	5	2	2	1	67.886	26	2	3	2	81.181	6	3	4	1
43.626	23	2	1	2	68.062	15	4	3	1	81.681	23	2	3	3
43.863	28	4	1	1	68.789	1	2	2	3	82.122	20	6	3	1
44.916	2	3	0	2	69.256	2	6	2	1	83.121	6	0	4	2
47.662	1	3	2	1	69.502	3	4	1	3	83.475	29	6	1	3
48.339	1	3	1	2	69.793	2	6	1	2	83.475	29	5	2	3
50.142	118	0	2	2	69.793	2	5	2	2	83.773	15	3	1	4
50.426	109	4	2	0	70.688	1	7	1	1	85.145	11	3	3	3
51.291	117	4	0	2	71.499	1	3	3	2	85.145	11	0	2	4
52.080	1	5	1	1	72.230	6	0	4	0	86.008	39	4	4	1
53.589	8	2	2	2	72.382	3	3	2	3	86.008	39	4	0	4
53.792	35	4	2	1	74.505	1	5	3	1	86.693	12	8	0	2
54.413	2	4	1	2	74.999	26	0	4	1	87.861	1	2	2	4
54.953	3	6	0	0	74.999	26	0	0	4	88.680	5	8	2	1
55.815	34	2	3	0	75.930	10	5	1	3	89.841	1	4	3	3

D. Annealing Conditions for Fig. 6.10

A detailed list of annealing conditions used for samples labeled 1 - 7 that fall on the dotted line in Fig. 6.10 is listed in the Table D.1 below.

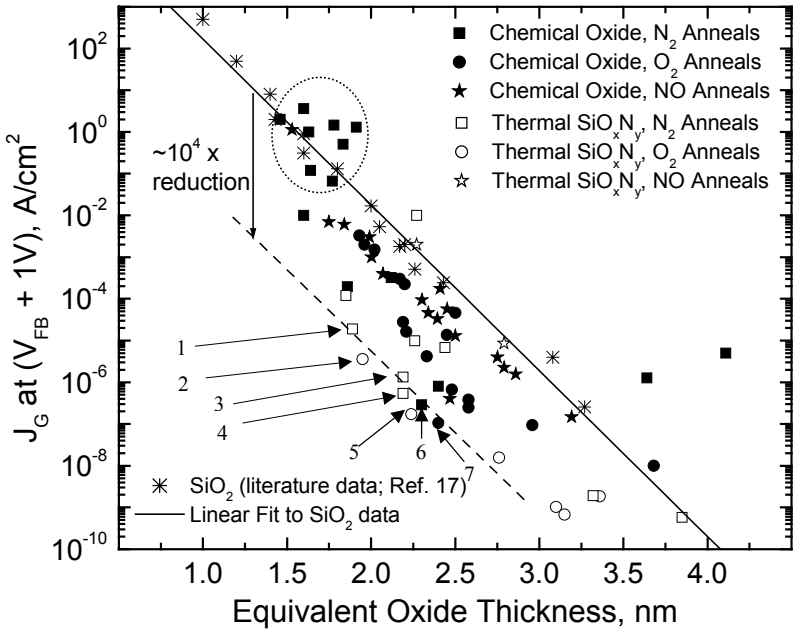


Fig. 6.10 The leakage densities for ALD HfO_2 gate stacks annealed to various temperatures (> 600ºC) and for various times. Plots are compared to the typical observed J_G for SiO_2 gate stacks (solid line), showing that reducing J_G by a factor of ~10^4 (marked by dotted line) is possible with properly chosen annealing conditions. The solid square data points in the dotted circle are the set of samples annealed in de-oxygenated N_2. The rest of the solid square data points denote samples annealed in house-N_2 that contains oxygen impurities. The detailed list of annealing conditions for samples labeled 1 to 7 that fall on the dotted line is given in Table D.1

Table D.1 List of annealing conditions used for samples 1 to 7 that fall on the dotted line in Fig. 6.10

Samples	Annealing conditions	HfO_2 films physical thickness (Å)	EOT (Å)	V_{FB} shift (V)	J_G at (V_{FB} + 1V) (A/cm^2)
1	600°C/30s/N_2	40	18.9	0.197	1.89 E-5
2	600°C/30s/O_2	40	19.5	0.189	3.59 E-6
3	900°C/spike/O_2	60	21.9	0.161	1.33 E-6
4	600°C/30s/N_2	60	21.9	0.211	5.44 E-7
5	600°C/30s/O_2	60	22.4	0.202	1.73 E-7
6	600°C/10m/N_2	60	23	0.215	2.91 E-7
7	600°C/30s/O_2	60	23.5	0.197	1.07 E-7