NOVEL DESIGN AND IMPLEMENTATION OF A BROADBAND AND HIGHLY EFFICIENT DOHERTY POWER AMPLIFIER

MEHDI SARKESHI

(M. ENG, National University of Singapore)

A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2007

Acknowledgements

I am truly indebted to my supervisors, Assoc. Prof. Ooi Ban Leong and Prof. Leong Mook Seng for their invaluable guidance and support during this work. I would specially wish to extend my thank to Ms. Atoosa Nasiri for her support and encouragement without which, this journey would not be so pleasant and memorable.

I would also like to gratefully acknowledge Mr. Tan Hong San for his kind support during my studies. Lastly, I would like to thank my parents for their endless love and priceless support.

Mehdi Sarkeshi

July 2007

Contents

Abstract

Modern communication systems require stringent capabilities in terms of linearity and efficiency. The need to amplify a variable envelope signal with high peak-to-average ratio in multi-carrier technologies such as WCDMA or OFDM, imposes tough challenges on the amplifiers that basically deliver their highest efficiency at their maximum output power. The Doherty power amplifier has recently gained a lot of attraction due to its simple concept, ease of implementation and promising efficiency enhancement in backed-off power region. However, the conventional Doherty power amplifier suffers from some disadvantages such as narrow bandwidth and large size due to its critical use of passive $\lambda/4$-transmission lines as impedance inverters. In this work, a novel configuration is proposed, which promises to eliminate the above mentioned problems by replacing the $\lambda/4$-transmission line with

an adaptive, compact and broadband alternative. A highly linear, varactor-based impedance transformer is placed at the output of the carrier amplifier, which performs wideband load-modulation by adaptively biasing the varactors according to the input signal envelope. Infineon's BB837 varactors have been used to realize the adaptive impedance inverter.

Three configurations, namely, a class AB, a conventional Doherty amplifier and the proposed novel Doherty amplifier, have been designed, simulated and fabricated using Transcom's TC2571 GaAs pHEMT discrete transistors. The proposed Doherty amplifier has displayed superior performance to the other two designs. Power added efficiency of more than 49.5% is achieved at maximum power level(33dBm) over a wide bandwidth (1.8GHz-2.2GHz). The high power added efficiency has been maintained within the 6-dB backoff power range. At 6-dB backoff point, power added efficiencyiy is more than 45.3% within the bandwidth of 1.8GHz to 2.2GHz. Third order harmonic distortion has been better than -42dBc within the entire power range over the above mentioned bandwidth. This verifes broadband performance of the proposed circuit. Moreover, 50% size reduction compared to conventional Doherty amplifier is achieved as a direct result of elimination of the $\lambda/4$-transmission lines .

List of Tables

List of Figures

List of Symbols

$A(t)$	Time-dependent amplitude
C	Capacitance
f	Frequency
G	Gain
I_{dc}	DC current
I_1	Fundamental current component
I_Q	Quiescent current
IM_3	Third order harmonic distortion
L	Inductance
$M_0, M_1, M_2 \ldots$	Nonlinear capacitance expansion coefficients
$N_0, N_1, \ldots$	Nonlinear capacitance expansion coefficients

n	Power law exponent
P_{RF}	RF power
P_{dc}	DC power
P_{in}	Input power
P_{opt}	Optimum power
PBO	Power backoff
PAE	Power Added Efficiency
P_{dcc}	DC power consumption of the carrier device
P_{dcp}	DC power consumption of the peak device
R_L	Load resistance
R_{opt}	Optimum resistance
t	Time
V_Q	Quiescent voltage
V_t	Threshold voltage
V_i	Input voltage
V_{dd}	Supply voltage
V_{SW}	Switch Voltage
V_{dc}	DC voltage
V_{c1}, V_{c2}	Control voltages of the impedance inverter
V_{c3}, V_{c4}	Control voltages of the phase compensator
v	AC voltage

V_{GG}	Gate bias voltage
Z_m	Impedance seen by the main(carrier) device
Z_p	Impedance seen by the peak device
Z_0	Characteristic impedance
Z_s	Source impedance
Z_l	Load impedance
Γ_{load}	Load reflection coefficient
Γ_{out}	Output reflection coefficient
η	Efficiency
ω	Angular frequency
λ	Wavelength
$\phi(t)$	Time-dependent phase
ζ	Input drive level coefficient
ϕ	Built-in potential

Chapter 1

Introduction

The wireless communication industry is pushing the next generation technology for higher data rates and broadband multimedia communications. Spectrum is costly so complex modulation schemes are required to transmit maximum amount of data with minimum spectrum occupation, which will result in complex signal waveforms.

Variable envelope signals with high peak-to-average ratios have to be linearly amplified and transmitted. This makes the power amplification block, the bottleneck of the entire transceiver system. Although acceptable linearity can be obtained from power amplifiers, it is almost always achieved at the expense of reduced efficiency. With the industry's demand for lower power consumption at base stations and smaller battery sizes and longer battery lifetime in hand held devices, tougher challenges are imposed on power amplifiers which are seemingly

being urged to satisfy contradictory requirements. Another problem with amplifying a variable envelope signal is that the power amplifier will be forced to operate at backed off power region for most of its "on" time. This is specially a problem for conventional power amplifiers which basically deliver their maximum efficiency only at a single power level near saturation. In the recent years, linearity issues have been somehow alleviated by linearization techniques such as digital predistortion, but achieving acceptable power added efficiency and maintaining it over the entire power level range remains to be a problem with no widely accepted solution.

Before moving to the motives of this research, we begin with a brief review of power amplifiers and their classifications followed by a review of power amplifier technologies. Subsequently, the focus of this work is detailed. Finally, this chapter will be concluded by outlining the organization of this dissertation.

1.1 Power Amplifiers

1.1.1 Conjugate Match and Load-line Match

For linear, small signal amplifiers, maximum power is delivered to the load when the load is conjugately matched to the output impedance of the amplifier, that is

$$\Gamma_{out} = \Gamma^*_{load}. \tag{1.1}$$

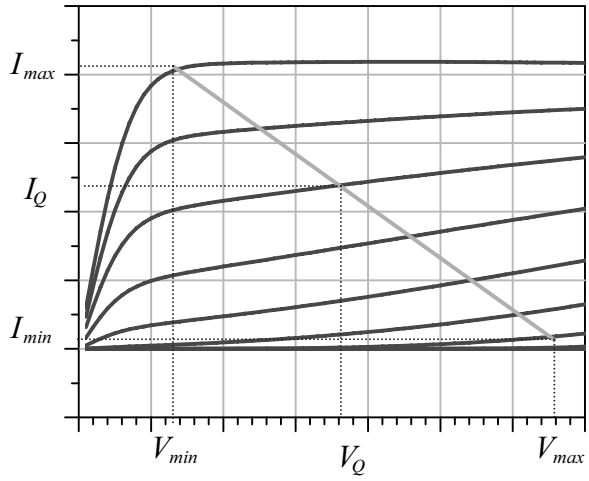


Figure 1.1: Optimum load resistance for maximum power delivery

However, this is not the case with power amplifiers where nonlinearities result in gain compression. For this reason, in large signal amplifiers, there is an optimum load R_{opt} for maximum power delivery, which is typically found by a method called load pull. An estimate of the optimum impedance R_{opt} can be made by adjusting the load so that the transistor current and voltage is maximized, as shown in Figure 1.1 , with the reactive part of the output impedance resonated out. R_{opt} can be determined as

$$R_{opt} = \frac{V_{max} - V_{min}}{I_{max} - I_{min}}, \tag{1.2}$$

where V_{min} is the knee voltage, V_{max} is the maximum device voltage limited by breakdown voltage, I_{min} is the minimum drain conduction current and I_{max} is the maximum conduction current that the device can tolerate.

1.1.2 Output Efficiency and Power Added Efficiency

Since power amplifiers are classified in different categories based on efficiency, it is necessary to review the precise definition of efficiency in the power amplifier design. There are two typical definitions to characterize the efficiency of an RF power amplifiers [2], "Output Efficiency" and " Power Added Efficiency ". Output efficiency is defined as the ratio of the RF output power P_{RF} to the dc power P_{dc},

$$\eta = \frac{P_{RF}}{P_{dc}}. \tag{1.3}$$

The above definition does not take into account the input power, P_{in} , and power gain G , whose effects are significant in RF power amplifiers specially when gain drops below 10 dB. This mandates the definition of the Power Added Efficiency (PAE),

$$PAE = \frac{P_{RF} - P_{in}}{P_{dc}} = \eta \left(1 - \frac{1}{G}\right). \tag{1.4}$$

1.1.3 Power Amplifier Classification

Based on their maximum possible efficiencies, RF power amplifiers are classified as class A, AB, B, C, D, E, F and S. In Class A, AB, B and C, the transistor is considered as a transconductive device. The classification as A, AB, B, or C describes the fraction of the full cycle, for which, current is flowing in the device.

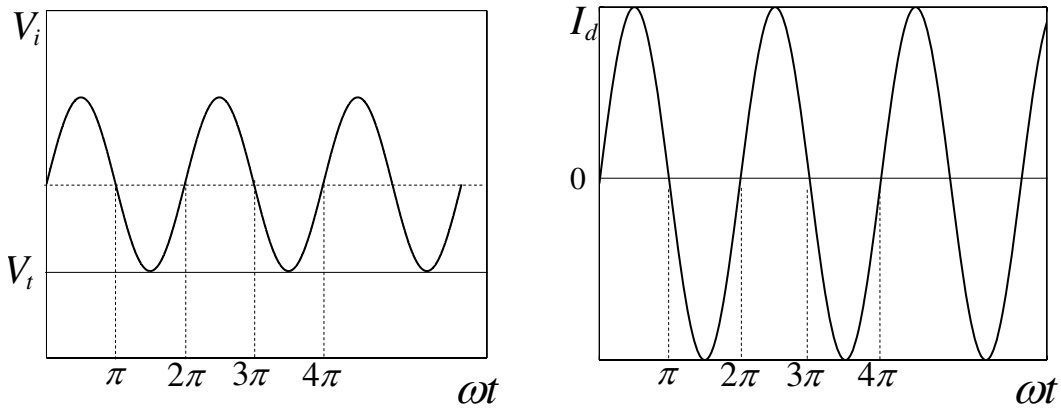
Such a fraction can be described as a conduction angle, which is the number of degrees (out of 360) for which current is flowing. If current is always flowing, the conduction angle is 360. As for Class D, E, F and S, the device acts like a switch. In order to provide a background for the motivations of this research, it is essential to briefly review the power amplifier classifications at this point.

1.1.3.1 Class A

Class A amplifiers are biased such that the variations in input signal occur within the limits of cutoff and saturation. The input instantaneous voltage, V_i, is always higher than the threshold voltage, V_t, so the drain(collector) current, I_d, flows during the complete cycle (360 degrees) of the input signal as shown in Figure 1.2. The center of the active region is set as the bias point. Class A operation provides the maximum linearity among all classes of operation since no clipping occurs under ideal circumstances. This, of course, comes at the price of reduced efficiency. Theoretical maximum efficiency of Class A amplifier is 50%.

1.1.3.2 Class B

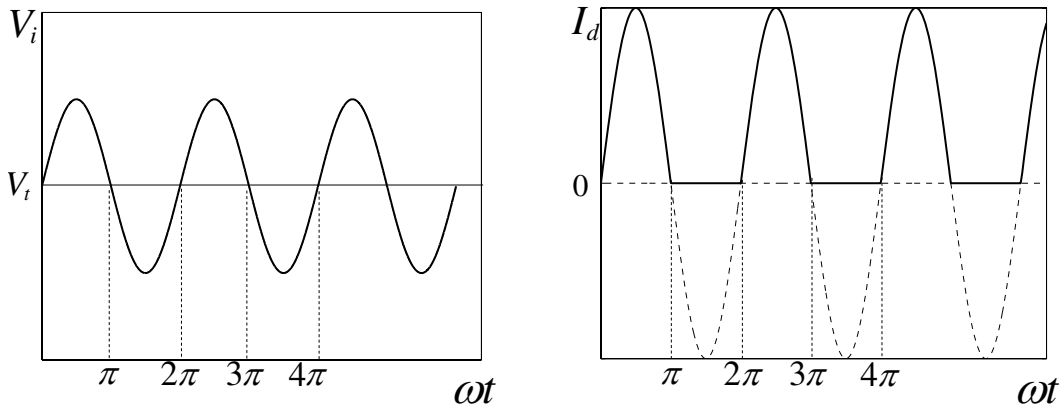
The conduction angle of the class B amplifier operation is 180 degrees, or one half the input cycle as seen in Figure 1.3. The DC bias point is selected so that no current flows in the device when there is no RF input. This is achieved by biasing the transistor at its threshold voltage, V_t. Maximum theoretical efficiency of class



(a) (b)

Figure 1.2: Class-A mode

B mode is 78.5%. Although this class of operation can achieve greater efficiencies than class A, linearity is compromised since the current waveform is significantly distorted. In low frequency applications, this problem is solved by realizing the class B mode of operation, in a push-pull topology as shown in Figure 1.4. In a push-pull configuration, each transistor conducts only for half of a period cycle. The two half-sine waveforms generated by the transistors, are combined to give the complete output waveform as shown in Figure 1.5. At RF frequencies, the push-pull arrangement is not viable due to difficulties in realizing the transformers. A harmonic short, realize by a parellel LC is usually employed at RF frequencies to filter out the harmonic components of the output signal and extract the fundamental component. The structure of the harmonic short will be more elaborated in the next sections where class F mode of operation is discussed. The schematic



(a) (b)

Figure 1.3: Class-B mode

diagram of a class B RF power amplifier is shown in Figure 1.6.

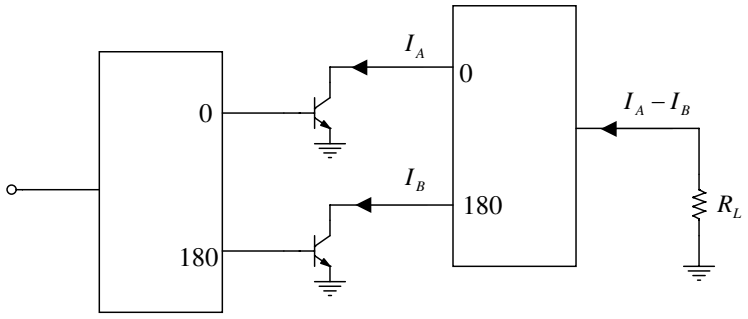
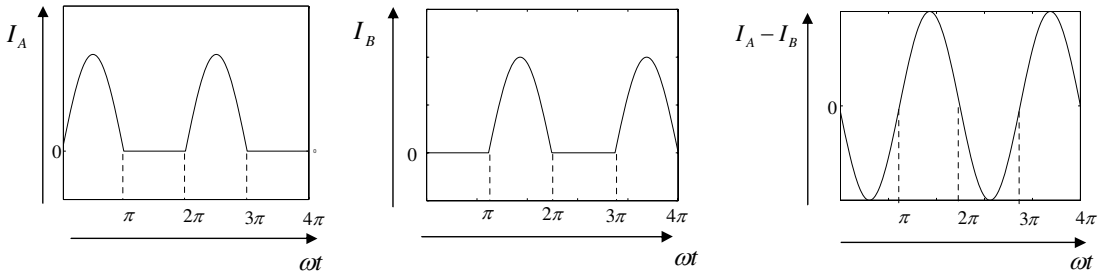


Figure 1.4: Push-pull class B amplifier with power combiner

1.1.3.3 Class AB

The operating point of the class AB operation is somewhere between class A and class B. The collector current flows for more than 180 degrees but less than 360 degrees of the RF input signal as seen in Figure 1.7 . The linearity of a class AB



(a) (b) (c)

Figure 1.5: (a) and (b): Currents of the individual transistors and (c): Combined current waveform

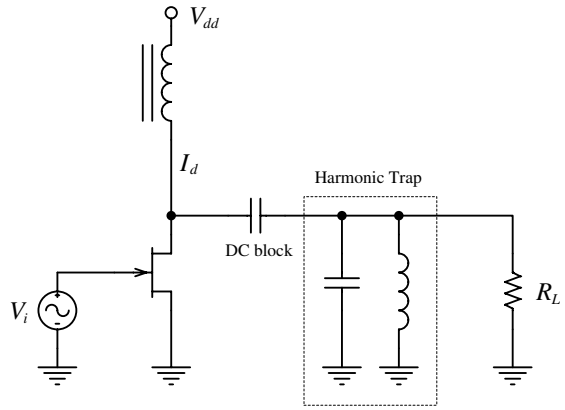
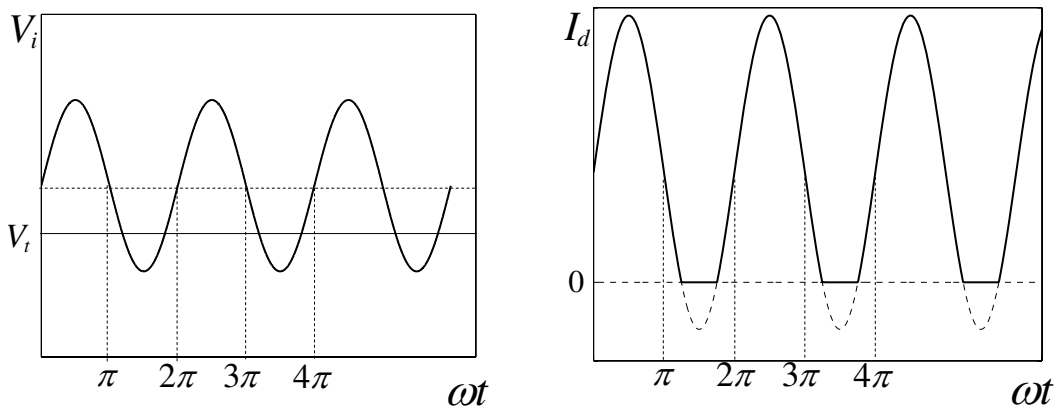


Figure 1.6: Schematic diagram of a class-B Power Amplifier



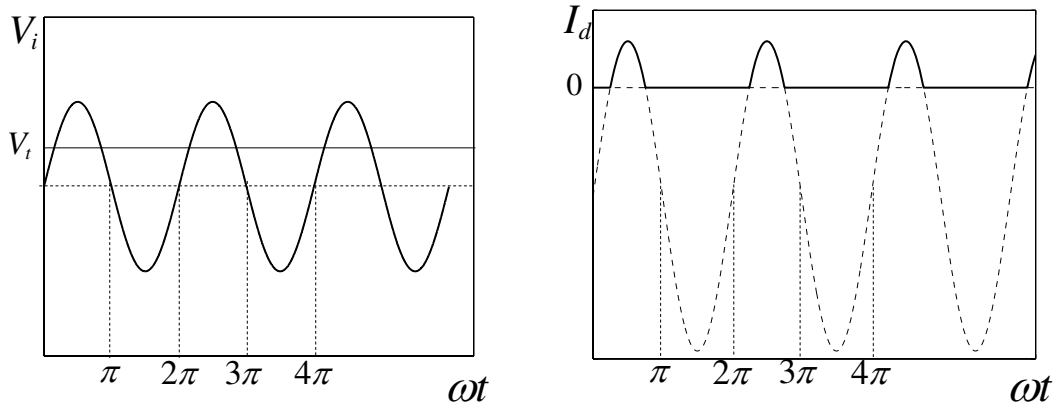
(a) (b)

Figure 1.7: Class-AB mode

power amplifier is closer to Class A operation and its efficiency closer to class B operation. This enables the selection of operating point of the class AB amplifier based on whether linearity or efficiency is the dominant requirement. Similar to class B mode of operation, a harmonic short is required to extract the fundamental component. Efficiency of Class AB amplifiers vary from 50% to 78.5%, depending on the bias point.

1.1.3.4 Class C

In class C mode of operation, drain current flows for less than one-half cycle of the input signal. The class C operation is achieved by setting the dc operating point below cutoff. Conduction is allowed only on the portion of the input signal that overcomes the reverse bias of the source gate junction as seen in Figure 1.8.



(a) (b)

Figure 1.8: Class-C mode

Although class C amplifiers are severely nonlinear, they provide highest efficiency among the four classes of amplifier operations discussed. Theoretical maximum efficiency of a class C amplifier is 100%.

Different classes of operation based on the device transfer characteristics are summarized in Figure 1.9.

Switch-mode Amplifiers

In switch mode amplifiers, the active device departs from its function as a transconductive element and behaves as a switch. This results in minimum overlap of drain (collector) voltage and current waveforms, which maximizes the efficiency. Class D, E, F and S amplifiers are defined in this course of device behavior. Switch-mode

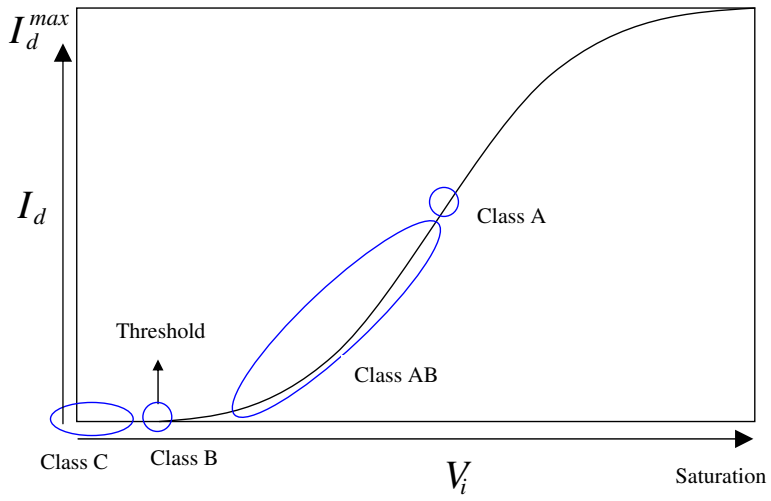


Figure 1.9: Power amplifier classes categorized based on the quiescent current

amplifiers are unquestionably nonlinear which means that information in the envelope of the input signal will be heavily distorted. This makes the switch-mode amplifiers suitable for constant-envelope signals.

1.1.3.5 Class D

Class D amplifiers have been overshadowed by class E amplifiers which are discussed in next section. This is because class E amplifiers outperform class D amplifiers and offer more attractions. Figure 1.10 shows a class D amplifier schematic diagram. It is made up of a two way switch, which is usually implemented using two transistors. A series resonator is employed at the output. The resonator is switched between a bypassed dc voltage and ground for alternate half cycles. Current and voltage waveforms of the class D power amplifiers are shown in Figure 1.11. Assuming that the transistors are ideal, the Q factor of the resonator is

high and the repetition cycle matches the resonant frequency of the LCR circuit, theoretical maximum efficiency is 100%. In practice, though, the switches pose problems at high frequencies in terms of parasitic reactances and driver requirements . This limits the application of Class-D amplifiers to low frequencies [2].

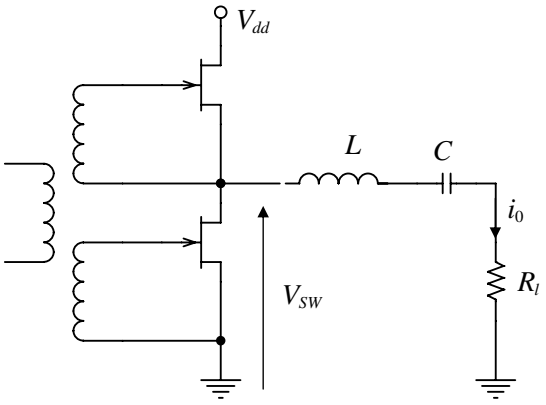
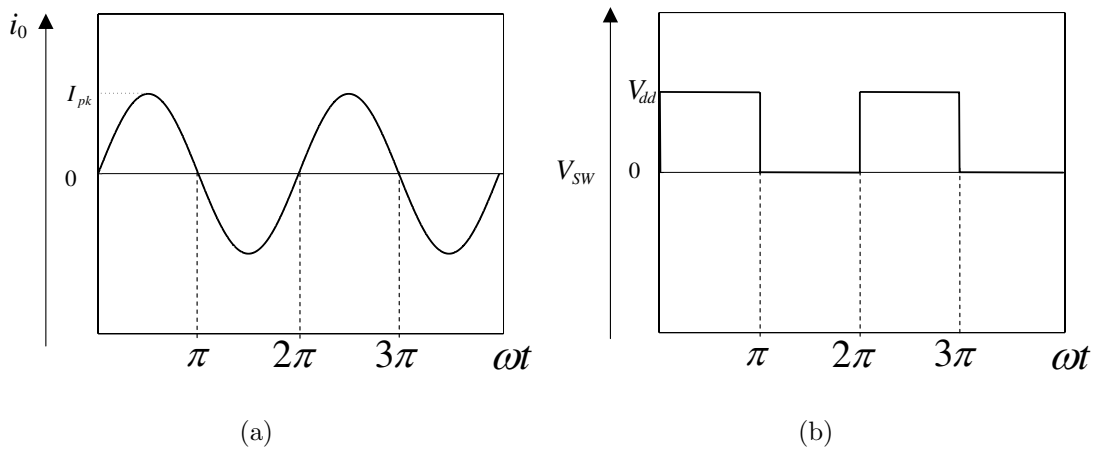


Figure 1.10: Schematic diagram of a class D power amplifier

1.1.3.6 Class E

Unlike other switch mode classes, the class E power amplifier promises potential possibilities of implementation at high frequencies. This is mostly due to the fact that, the class E amplifier can successfully achieve very high efficiencies in the presence of parasitics without requiring a nearly ideal switch. A schematic diagram of a class E amplifier is shown in Figure 1.12. The shunt capacitor at the output of the switch is a key component. A series resonator follows this arrangement [3]. The idea behind class E mode of operation is that when the switch is open, the



(a) (b)

Figure 1.11: Class D current and voltage waveforms

entire switch current will pass through the capacitor and the current will only pass through the switch when the collector (drain) voltage is zero and hence, there is no power loss in the switch. The voltage and current waveforms are depicted in Figure 1.13. It is important to note that, the component values and the switch frequency is chosen so that the switch will turn on at the exact moment that the capacitor current reaches zero. As seen in Figure 1.13, the high peak voltage of the shunt capacitor is a disadvantage of class E amplifiers [2].

1.1.3.7 Class F

The idea behind a class F amplifier is to simply add third order harmonics to the output voltage fundamental component to make it look more like a square-wave signal. This implies that the drain (collector) voltage is lower while current is flowing, but higher while current is not flowing, and hence the increase in efficiency.

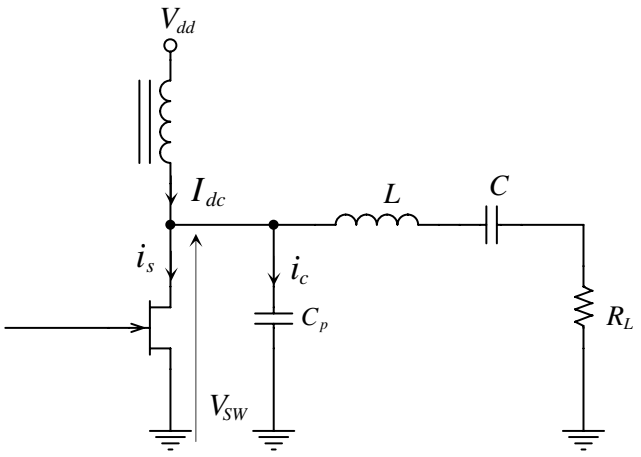


Figure 1.12: Schematic diagram of a class E power amplifier

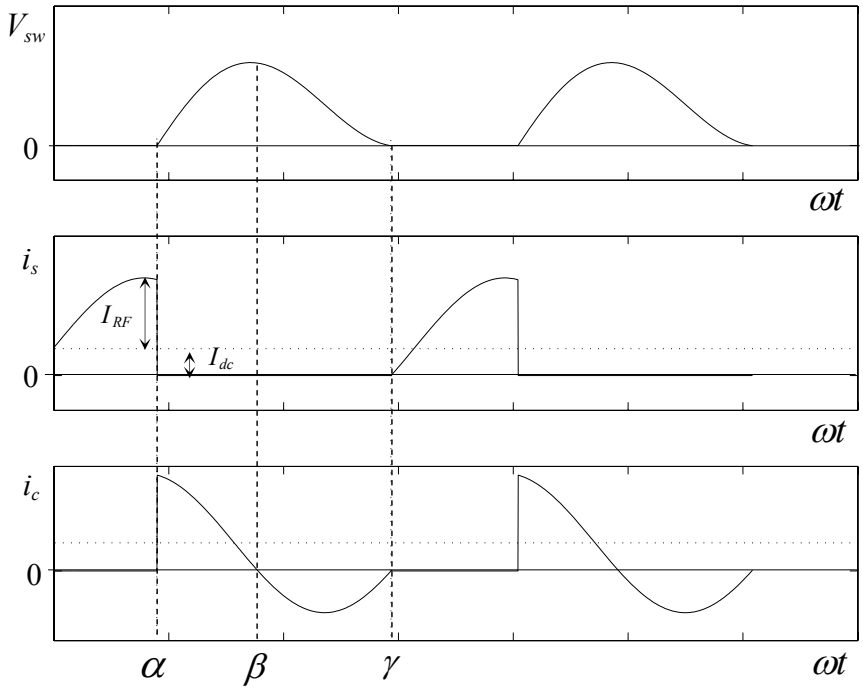


Figure 1.13: Voltage and current waveforms of a class E power amplifier

It has been derived in detail in [2] that this arrangement could maximize the efficiency. A class-F amplifier is shown in Figure 1.14. It is pretty much like a class B amplifier except that, instead of using a resonator at the output to extract the fundamental, a $\lambda/4$-transmission line has been employed to trap even order harmonics while letting in the odd order ones to square the sine wave.

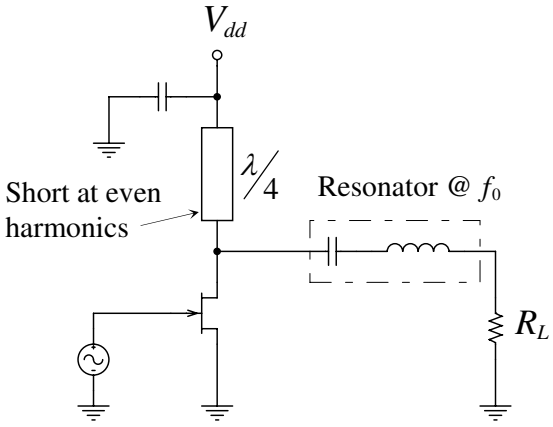


Figure 1.14: Schematic diagram of a class F amplifier

1.1.3.8 Class S

In class S amplifiers, the input signal is converted to a constant envelope signal using a pulse-width-modulator. The information in the envelope of the signal is transferred to the duty-cycle of an oscillating reference. This is subsequently applied to an inverter-like limiter which amplifies the pulse-width modulated signal. The amplified original signal is then retrieved using a bandpass filter. Theoretically, high linearity and efficiency are achieved but, in practice, problems arise since a

broad bandwidth is required for the device to amplify pulse shaped signals [3]. The need for a clock signal with frequencies much higher than the input signal is another challenge since high performance material/technology would be essential.

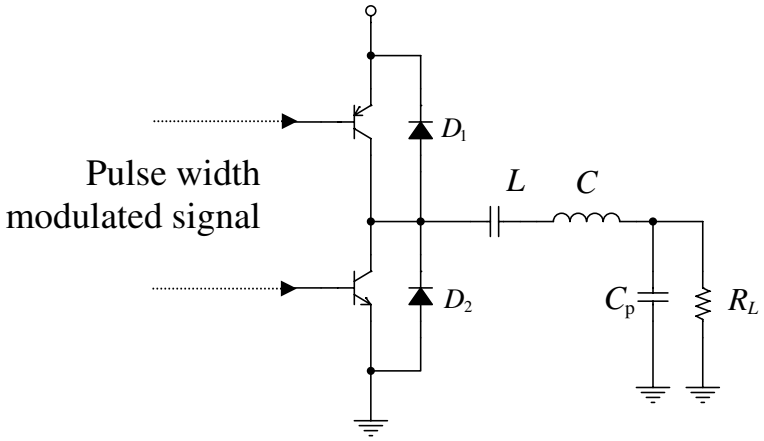


Figure 1.15: Schematic diagram of a class S amplifier

1.2 RF Power Amplifier Technologies

Several technologies are available for RF power amplifiers. Common benchmarks for a comparative study of the available technologies are efficiency, linearity, power gain, thermal conductivity, size, cost, integration level, breakdown voltage and cutoff frequency. The typical values of these parameters for some of the most common RF power amplifier technologies are summarized in Table 1.1 [4]. A brief description of each technology follows.

Technology	GaAs HBT	Si BJT	SiGe HBT	CMOS	LDMOS
f_T(GHz)	46	27(HF)[1] 22(HV)[2]	44 (HF) 25 (HV)	> 20	> 20
BV_{ceo}(V)	14.3	3.3 (HF) 6.2 (HV)	3.0 (HF) 6.0 (HV)	5	15
Thermal Conductivity (W/cm-C)	0.49	1.5	1.5	1.5	1.5
Normalized Cost 1mm2	1	0.3	0.3	< 0.2	0.3
Wafer Size	6" wafer	8" wafer	8" wafer	12" wafer	8" wafer
PAE	>40%	$> 30\%$	$> 30\%$	>30%	$> 35\%$
Linearity	great	good	good	good	good
Power Gain	great	good	great	poor	poor
Integration Level	poor	good	good	great	good

Table 1.1: Common technologies for RF power amplifiers

1.2.1 Si-BJT and CMOS Power amplifiers

Since the entire digital communication world is dominated by Si-based devices, it is natural that the attention of the designers have turned to realization of RF circuits in Si-based technologies. The possibility of integration of the entire system in a single chip has been very appealing although, obviously, this will cause numerous problems such as cross-coupling and noise. Si-based devices such as Si-BJT and CMOS enjoy high thermal conductivity and good $1/f$ noise as well as low cost. However, they suffer from poor linearity and high substrate loss. Presence of parasitics limits very high frequency applications as well. For power amplifier applications, high power levels can not be achieved with CMOS due to the low breakdown voltage. CMOS power amplifiers are also larger than their SiGe or GaAs counterparts for the same functionality. This is because CMOS devices, unlike GaAs or SiGe HBT technology which incorporate vertical transistors, become rapidly larger when scaled up to accommodate high output powers. The cross sections of an Si-BJT transistor and an NMOS transistor are shown in Figure 1.16

and Figure 1.17 respectively.

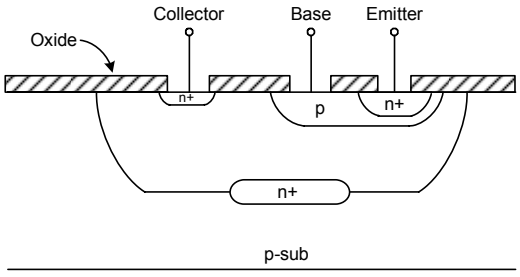


Figure 1.16: Si BJT cross-sectional structure

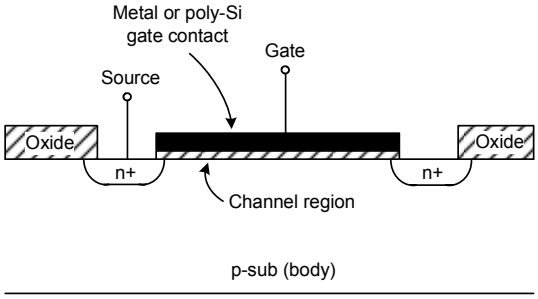


Figure 1.17: NMOS cross-sectional structure

1.2.2 LDMOS

The laterally diffused MOSFET (LDMOS) is a suitable choice for high power applications which can be realized in standard CMOS process. High breakdown voltage is achieved by using high resistivity Silicon. High bias voltage of LDMOS devices makes them suitable for base-station applications rather than hand-held ones. Unlike HEMTs that require a negative bias for the gate, LDMOS requires a single polarity supply since it is an enhancement mode FET. Major disadvantages

of LDMOS are poor linearity and lower efficiency compared to GaAs HEMT and GaAs HBT. Silicon LDMOS has dominated the market of devices in the GSM and WCDMA base-stations, primarily because of low cost and acceptable performance [5]. As shown in the cross-sectional structure in Figure 1.18, LDMOS consists of a p-doped layer of silicon underneath the n-type channel to isolate it from ground. The source is grounded using p+ sinkers that run vertically from the source contact at the surface through to the bottom of the substrate.

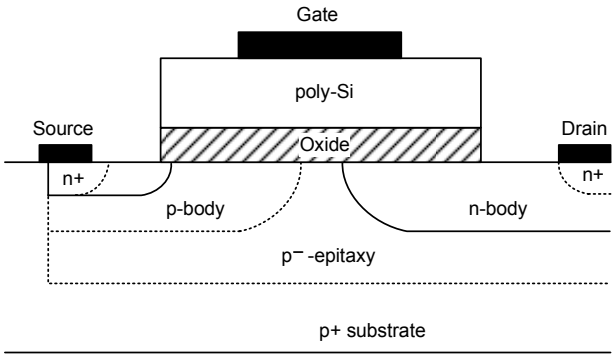


Figure 1.18: LDMOS cross-sectional structure

1.2.3 GaAs HBT

The HBT[3] can provide faster switching speeds than silicon bipolar transistors mainly because of reduced base resistance and collector-to-substrate capacitance. Since GaAs has a poorer thermal conductivity compared to silicon, its thermal effects are higher than BJTs. The HBT has also higher current gain and power

[3]Heterojunction Bipolar Transistor

density. The base region in the HBT can be made thinner and more heavily doped than in a normal BJT, decreasing the electron transit time and base capacitance, without increasing the base resistance [5] and hence, the high-frequency performance. However, HBTs suffer from high cost and low integration level. As shown in the cross-section shown in Figure 1.19, GaAs HBTs are fabricated using p-type GaAs in the base sandwiched between n-type GaAs in the collector and a layer of n-type AlGaAs in the emitter. The ohmic contacts to the emitter and collector are formed with heavily doped n-type GaAs.

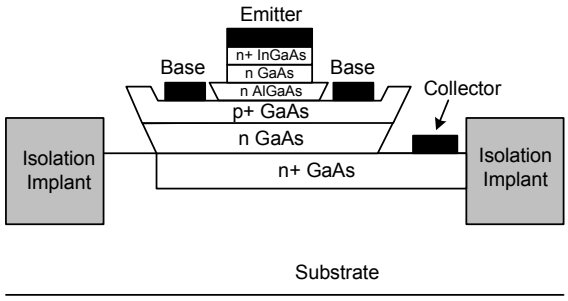


Figure 1.19: GaAs HBT cross-sectional structure

1.2.4 SiGe HBT

In order for better integration with Si-based devices, HBTs have also been fabricated using SiGe instead of AlGaAs in GaAs. Recent technologies have overcome the speed limitations of conventional silicon technologies. GaAs HBTs allow lower supply voltages due to a lower base-emitter turn-on voltage compared to GaAs

HBTs. The possibility of using larger wafers, better strength and thermal conductivity are other advantages over GaAs. In SiGe, between 10% to 20% of the silicon atoms are replaced by germanium. This will create a built-in electric field that results in acceleration of the carriers across the base due to reduction of the base transit time. Therefore, the f_T of the SiGe HBT is higher than a silicon BJT. The ultimate achievable power of SiGe devices is limited due to the low breakdown voltage of silicon technology. The cross-section of a SiGe HBT device is shown in Figure 1.20. The SiGe HBT uses a moderately doped p-type base of SiGe sandwiched between a lightly doped n-type collector and an n-type emitter, both of silicon. For power devices, a thick collector with light doping is frequently used to increase the base-collector breakdown voltage and also to improve linearity, even though the resulting current density (and output power) will still be smaller than for the GaAs HBTs [5].

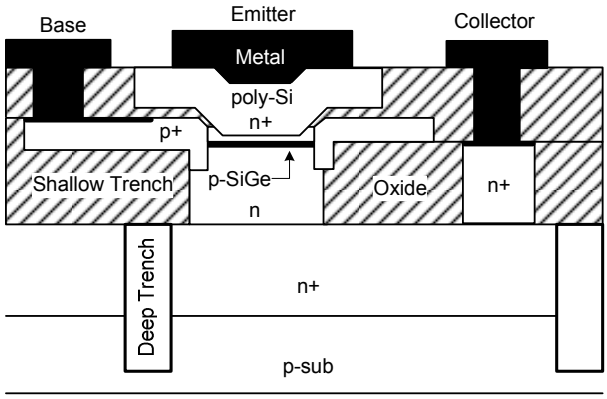


Figure 1.20: SiGe HBT cross-sectional structure

1.2.5 GaAs HEMT

The High Electron Mobility Transistor (HEMT) has a very similar structure to MESFET. The channel between the gate and the GaAs substrate is formed by an AlGaAs layer. HEMTs have also been fabricated using newer material structures, such as the pseudomorphic-HEMT (AlGaAs-InGaAs layers on GaAs), or the lattice-matched InP HEMT (AlInAs-GaInAs on an InP substrate) recently [5]. There is an important difference between HEMT and MESFET which results in higher gain and extended frequency performance in HEMTs. In MESFET devices, since the channel is doped, the ionized donors scatter the electrons. Therefore, the electron mobility is degraded due to high parasitic resistances. In HEMT devices, the channel and electron source are in different layers so there are no impurities in the channel. This results in a trapped layer of electrons (a two-dimensional "electron gas") having high saturated electron velocity under the compound semiconductor which explains HEMT's better performance compared to MESFETs. While HEMTs are inherently more efficient than HBTs, by properly tailoring the HEMT layers, increased linearity can also result. Although the current density is lower than HBTs, multiple heterojunctions can be created to increase the power. Figure 1.21 shows the cross-section of a GaAs pHEMT transistor. For realization of the present work, GaAs pHEMT devices have been used. TC2571 GaAs pHEMT transistors from Transcom company (Appendix A) have been employed to realize

the design. A photograph of the die of this transistor is shown in Figure 1.22.

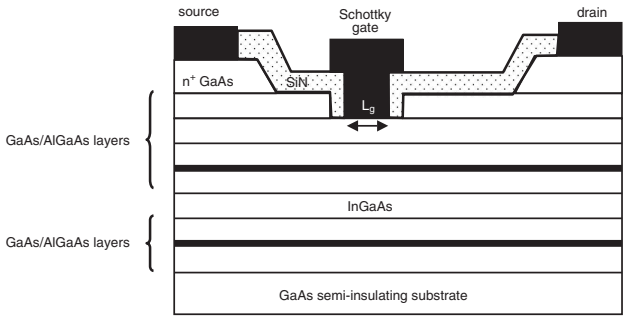


Figure 1.21: GaAs pHEMT cross-sectional structure

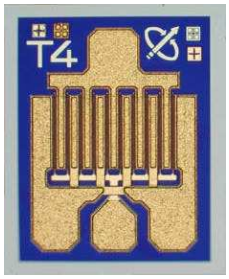


Figure 1.22: Transcom's TC2571 Pseudomorphic-HEMT

1.3 Research Focus

One of the promising methods for efficiency enhancement in the backed-off power region is the Doherty power amplifier, named after W.H. Doherty. It was introduced in 1936 [6] and was used to enhance the efficiency of traveling wave tubes in the lower power regime. Due to its simple concept, ease of implementation, and promising potential for efficiency enhancement, it has recently gained a lot of attraction for applications in modern wireless systems such as WCDMA, OFDM, and

WLAN, in which, variable envelope signals are involved. Although Doherty amplifiers can achieve significant efficiency enhancement in the backed-off region, they suffer major drawbacks. The Doherty amplifier has a narrow bandwidth, which is mainly because the Doherty amplifier employs a passive $\lambda/4$-transmission line as an impedance inverter for load modulation. The large size of the $\lambda/4$-impedance inverter in common wireless communication frequencies is another drawback which is the main obstacle for realizing a compact Doherty amplifier. As the main contribution of this research, a novel topology for the Doherty amplifier is proposed which tries to overcome the above mentioned problems by eliminating the $\lambda/4$-impedance inverter and replacing it with a compact and broadband alternative. The proposed circuit has been designed, simulated and fabricated. As a result of this research, a provisional patent has been filed in the United States with the reference number of "No. 60/936,151"[4] on 18 June 2007. Publications regarding this work are pending to be submitted after protection issues are resolved.

1.4 Dissertation Organization

Chapter 2 revisits the most common efficiency enhancement techniques. A literature review is carried out. Advantages and disadvantages of different approaches are briefly explained. The Doherty amplifier is discussed next and different aspects

[4]NUS ILO reference:OOI BL 01-US/PRV

and characteristics of the technique are detailed. The mechanism of efficiency enhancement in Doherty amplifiers through load modulation is comprehensively formulated. A review of major research works on Doherty amplifiers in recent years is also covered. Chapter 3 explains the drawbacks of the conventional approach in detail and a novel load modulation technique with the potential to overcome the mentioned problems is proposed. In chapter 4, the theoretical development of the proposed topology is presented. Detailed study of the models used for the devices, load pull theory and characteristics of the adaptive impedance transformation are covered. In chapter 5, the proposed circuit is challenged through simulations and measurements. Simulation results are compared with measured data from fabricated modules. Measured results from conventional approach and the proposed topology are compared. Chapter 6 concludes the dissertation with a discussion on the objectives achieved.

Chapter 2

The Doherty Power Amplifier

2.1 Efficiency Enhancement Techniques

There are two major problems with power amplifiers in modern communication systems. Firstly, power amplifiers generally deliver their maximum achievable efficiency at a single power level, which is somewhere near maximum output power. If the power is backed off from that single point, the efficiency will decrease. Since modern communication systems require amplification of a variable envelope signal with high peak-to-average ratios, power amplifiers are forced to work in the power back-off regime for most of their "on" time. The second problem is the difficulty in preserving the information carried in the envelope of the signals. Usually, the amplitude modulation information of signals will be heavily distorted especially near the maximum power level. "Efficiency enhancement techniques" have been

available for many years [2]. They mainly deal with the first problem but they certainly affect the second problem as well since linearity and efficiency are closely interrelated. Some techniques can be used to improve either efficiency or linearity, focusing on one as the primary design target. This chapter discusses the techniques that mainly deal with improving the efficiency under variable envelope conditions.

2.1.1 Envelope Elimination and Restoration (Kahn Technique)

First demonstrated by Kahn in 1956 [7], Envelope Elimination and Restoration (EER) is a technique to provide high efficiency and linearity using a switch-mode amplifier and a linear low frequency modulator. EER technique is a more efficient alternative for conventional class AB amplification. A block diagram of the EER system is shown in Figure 2.1. The basic idea is that the input signal is passed though a limiter so that the possibility of AM-PM distortion is eliminated and the phase information is preserved. The signal is then amplified using a switch mode nonlinear amplifier. The envelope of the signal, on the other hand, is retrieved by passing a sample of the input signal through an envelope detector and amplifying it using a voltage supply modulator. This, in return, is used to modulate the output signal to result in an undistorted amplified signal with the original waveform. Since the switch mode amplifier could be considered as a voltage source, the output signal

amplitude could be linearly modulated with bias supply. In practice, the process of supply modulation of the power amplifier requires a significant amount of power. If this process could be carried out with 100% efficiency, the overall efficiency could be maintained over the entire envelope range. One potential problem with this technique is poor bandwidth. Highly efficient amplification of broadband envelope signals introduces a big challenge in EER systems.

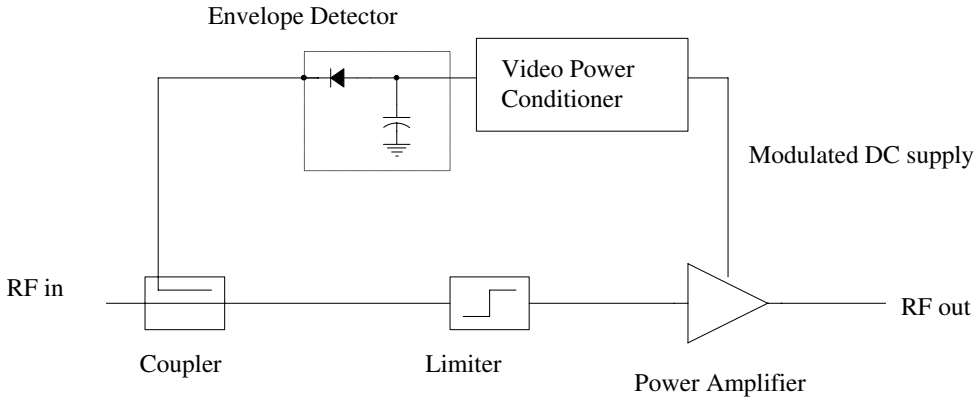


Figure 2.1: Envelope elimination and restoration

2.1.2 Bias Adaptation (Envelope Tracking)

Bias Adaptation or Envelope Tracking (ET) technique [8] is in many ways similar to Envelope Elimination and Restoration (EER) technique. The difference is that the main power amplifier can be any conventional device and input drive contains both envelope and phase information (no limiter is used). The envelope tracking path decreases the DC bias voltage for the low power input signals and increases it

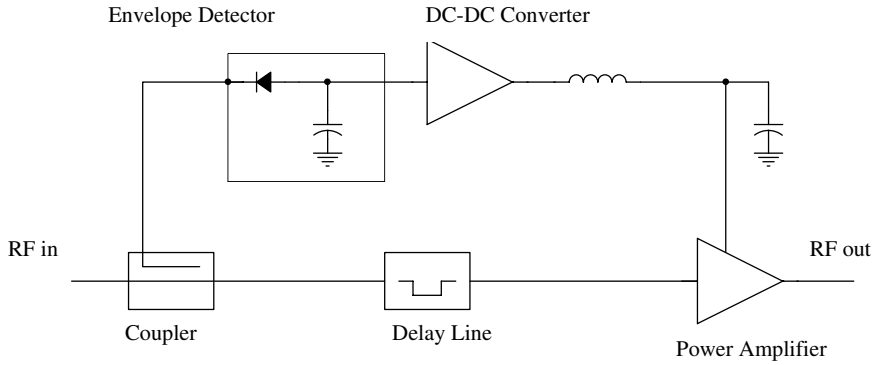


Figure 2.2: Block diagram of Envelope tracking technique

at the high power regime and hence the improvement in efficiency. Figure 2.2 shows the block diagram of the system. The envelope tracking technique appears to be more viable than the EER technique since there is no need to accurately replicate the signal envelope anymore. Practical implementations of ET technique [8],[9],[10] suffer from integration issues with the dc-to-dc converter and gain variation during the bias adaptation.

2.1.3 Switched Dynamic Biasing Technique

From the definition of power efficiency in section 1.4, it is obvious that an increase in efficiency can be achieved by reducing dc power consumption. This is typically carried out by reducing either the DC current (DCB) or DC bias voltage (DVB) or both. The problem with these approaches is that as the DC current is decreased dynamically as a means of maintaining high efficiency, the gain of the amplifier is reduced significantly. It is found that the gain variation in Envelope Tracking(ET)

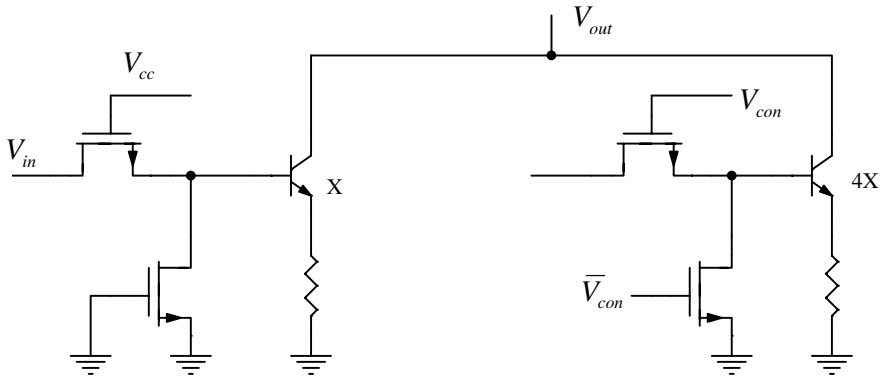


Figure 2.3: Switched dynamic biasing technique

and Envelope Elimination and Restoration(EER) technique, are mainly due to the decrease in drain (collector) current density. In order to overcome this issue, switched dynamic biasing techniques have been proposed [11] to keep the current density constant as the input power level changes. Low-loss switches have been utilized to switch on/off a number of parallel transistors according to the input power level as shown in Figure 2.3. As the input power increases more transistors are switched on while the current density of all transistors remain constant and hence the constant gain. The drawback of this approach is the difficulty to realize high isolation when the switch is turned off and low insertion loss as the switch is turned on.

2.1.4 Chireix Outphasing Technique (LINC Amplifier)

LINC[1] Amplifier was introduced by Chireix in 1935 [12]. As illustrated in the block diagram in Figure 2.4, the idea of the Chireix Amplifier is to decompose a variable envelope signal

$$S_{in}(t) = A(t).\cos(\omega t + \phi(t)), \tag{2.1}$$

into two outphased constant envelope signals

$$S_1(t) = \cos\left(\omega t + \phi\left(t\right) + \cos^{-1}\left(A\left(t\right)\right)\right), \tag{2.2}$$

$$S_2(t) = \cos\left(\omega t + \phi(t) - \cos^{-1}(A(t))\right). \tag{2.3}$$

These two signals can then be combined together after being amplified separately using two highly efficient (and possibly nonlinear) amplifiers. The resulting output $S_{out}(t)$, will be

$$S_{out}(t) = G[S_1(t) + S_2(t)] = 2GA(t).\cos(\omega t + \phi(t)). \tag{2.4}$$

This is also known as out-phasing technique.

[1] LInear amplification using Nonlinear Components

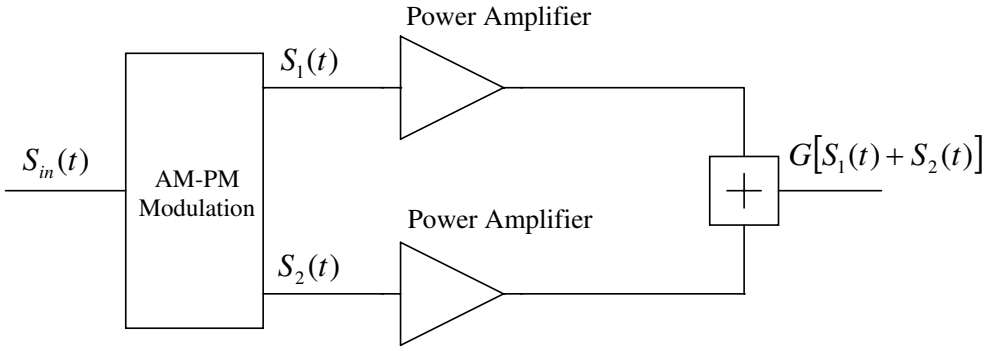


Figure 2.4: Block diagram of Chireix outphasing amplifier

2.2 The Doherty Technique

The Doherty Amplifier, first demonstrated in a classic paper by W. Doherty [6], primarily focuses on improving the efficiency in the backed-off region. As mentioned earlier, conventional power amplifiers are basically most efficient near the maximum output power. This degrades the average efficiency when a variable envelope signal with high peak-to-average ratio has to be amplified. Ideally, a constant maximum efficiency has to be maintained over the entire envelope range. The technique was originally applied to high power tube amplifiers but its simplicity and the novel idea behind it, has made it attractive, in recent years, for re-invention in solid-state applications.

2.2.1 Principles of Doherty Amplifier

In order to understand how the Doherty technique can improve the efficiency in backed-off power levels, we have to look into the nature of efficiency roll-off at lower

power levels. This will help to understand how load modulation can lift-up the efficiency curve in backed-off power regime. Let's consider a conventional Class-B amplifier as was previously shown in Figure 1.6. The theoretical efficiency of a class B power amplifier is shown in Figure 2.5. The optimum load for load line

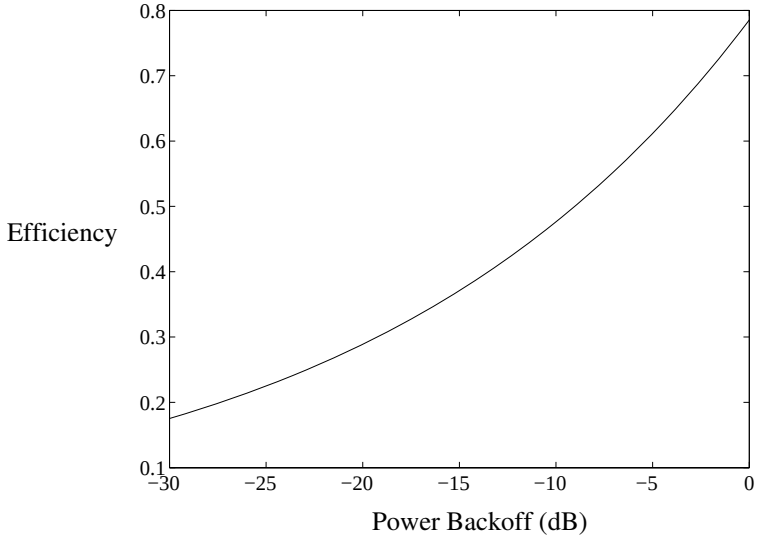


Figure 2.5: Efficiency of a class B power amplifier

match would be

$$R_{opt} = 2\frac{V_{dc}}{I_{max}}. \tag{2.5}$$

RF output power will be calculated as

$$P_{RF} = \frac{V_{dc}I_{max}}{4}. \tag{2.6}$$

DC power consumption is

$$P_{dc} = \frac{V_{dc}I_{max}}{\pi}. \tag{2.7}$$

Maximum efficiency is

$$\eta = \frac{\pi}{4} = 78.5\%. \tag{2.8}$$

Now if we decrease the input power by a factor of k^2 ($k = \frac{v_i}{V_{max}}$) , the fundamental RF current component I_1 would be

$$I_1 = \frac{I_{max}}{2k}, \tag{2.9}$$

so

$$P_{RF} = \frac{1}{2} I_1^2 R_{opt} = \frac{V_{dc} I_{max}}{4k^2}, \tag{2.10}$$

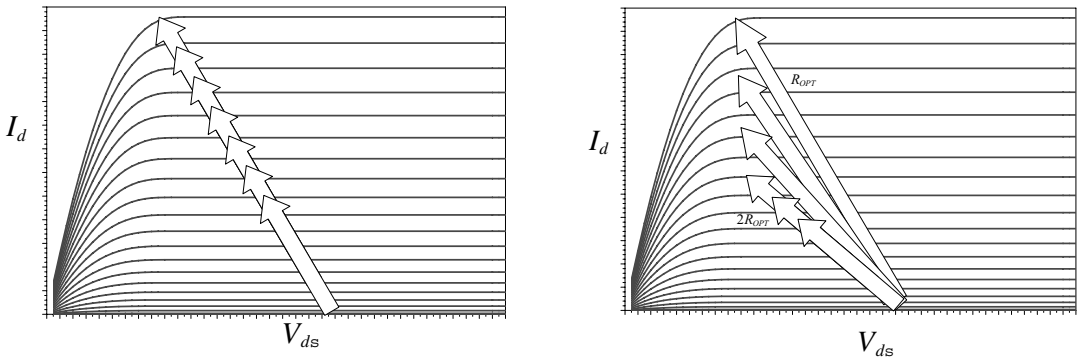
and

$$P_{dc} = I_{dc} V_{dc} = \frac{V_{dc} I_{max}}{k\pi}. \tag{2.11}$$

Efficiency will then become

$$\eta = \frac{P_{RF}}{P_{dc}} = \frac{\pi}{4k}. \tag{2.12}$$

This shows that the efficiency decreases by a factor of k if the input power is decreased by a factor of k^2. Looking carefully at equation 2.10, it can be seen that if the load could be adaptively increased (modulated) in proportion to k as the input power decreases in proportion to k^2, the efficiency would have remained constant regardless of input power level. This is the main idea behind the Doherty technique. In a nutshell, a Doherty amplifier employs load modulation to keep the



(a) (b)

Figure 2.6: Load line projection of (a) a class B power amplifier and (b) a Load modulated amplifier for constant efficiency

efficiency at constant maximum over a range of power back-off. Equation 2.10 also implies that increasing the load impedance with decreasing input power will result in constant output rail-to-rail voltage over a range of input power levels. This is illustrated in Figure 2.6, where the dynamic load line of a load modulated power amplifier is compared with the one of a conventional Class-B. In fact the reason for increasing the load impedance is to allow the output voltage, a full rail-to-rail swing within a range of input power.

Obviously, it is a physical challenge to dynamically modify the load impedance as the input power changes [2]. The other immediate problem with this approach is that even if this challenge could somehow be overcome, the amplifier would be inherently nonlinear even if an ideal device is used because the output power will decrease in proportion to k instead of k^2. So the enhancement in efficiency would

come at the price of a heavily distorted output waveform. In fact, both above mentioned problems, realizing the level-dependent impedance and the nonlinearity issue could be solved at the same time by Doherty's genius invention. Unlike the conventional power amplifier in which the RF load is considered a fixed, physically passive entity, Doherty amplifier employs a second, phase-coherent source to modify the load seen by the first.This configuration should not be mistaken with the Travelling wave amplifier despite the similarities in their structure. In a TWA multiple active devices are connected in series so that the parasitics of the gate port and the drain port build a transmission line network and thus they are cancelled out. Unlike the Doherty Power Amplifier all the transistors in a TWA are biased at the same point and the contribute equally to the output power while in a Doherty structure the Main and the Peak amplifier are biased differently and the contribute to the output power differently at different input power levels. Figure 2.7 shows two current generators driving a single load. If source 2 is set to give zero current, source 1 will see a load resistance of R_L. If both sources contribute in load current, the impedance seen by source 1 will be

$$Z_m = R_L \left(1 + \frac{I_p}{I_m}\right). \tag{2.13}$$

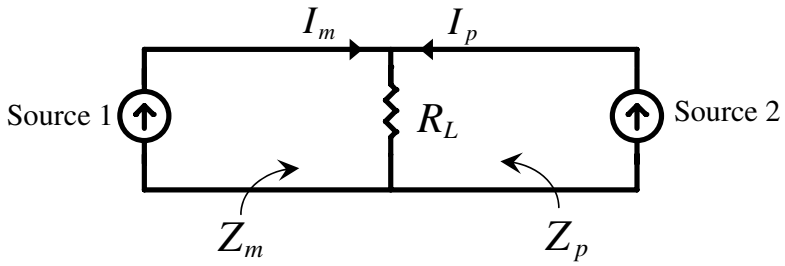


Figure 2.7: Load modulation using an additional source

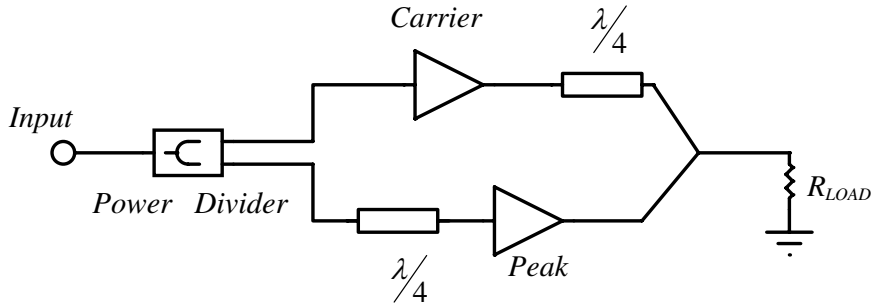


Figure 2.8: Block diagram of a Doherty amplifier

Similarly, source 2 would see an impedance of

$$Z_p = R_L \left(1 + \frac{I_m}{I_p}\right). \tag{2.14}$$

This shows that the impedance seen by either of generators can be pulled by changing the magnitude and phase of the other. In Doherty amplifiers, generators are considered to be the transconductances of possibly different transistors. For convenience, the transistors are termed "carrier" and "peak" devices [2]. Figure 2.8 shows a basic block diagram of a Doherty Amplifier. As the input drive is decreased, both transistors contribute to the load current until a certain threshold

point, which is conventionally 6-dB lower than the maximum combined power. Below this point, the peak amplifier shuts down, leaving only the carrier amplifier active. In practical implementations, the carrier amplifier is operated in class AB or class B while the peak amplifier is biased at deep class C to facilitate its shutdown at a certain drive level. In fact, the Doherty technique makes use of the dis-similarities between the two elements to open up opportunities to improve the efficiency through active load pull. A $\lambda/4$ impedance transformer is placed between the load and the carrier amplifier. This is a key element that acts like an impedance inverter. It makes the impedance seen by the carrier amplifier decrease while the peak amplifier current, I_p, increases. A second $\lambda/4$ transmission line is placed before the peak amplifier to compensate for the 90 degree delay imposed by the first $\lambda/4$ transmission line, placed after the carrier amplifier. This makes the output currents of the carrier and peak amplifier to combine in-phase. The $\lambda/4$ transformer is narrow-band and bulky in common frequencies used for wireless communications. This is the main obstacle for realization of broadband and highly integrated Doherty amplifiers.

The second problem associated with the load modulation technique was the inherent nonlinearity as mentioned before. Looking at the Doherty configuration, the output power increases in proportion to the input power level in a "square root" fashion. Meanwhile, the peak amplifier gives a "three-half" power transfer characteristic due to the upward load-pull effect[2]. The combination of the two power

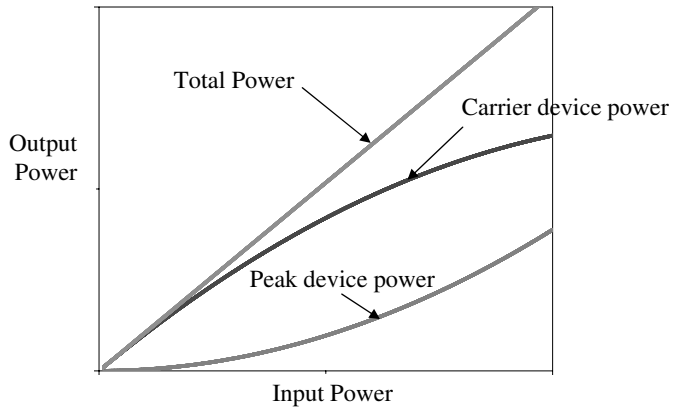


Figure 2.9: Power characteristics of the carrier and peak amplifier

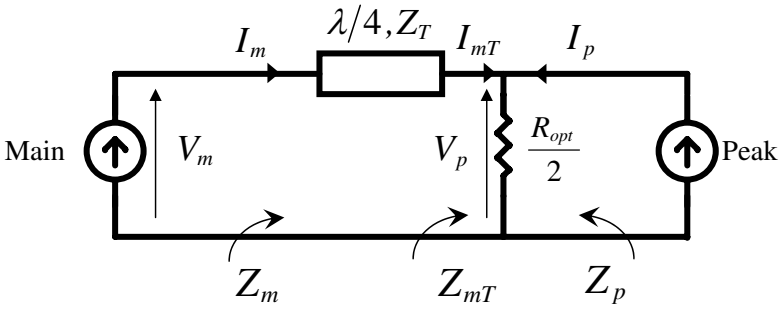


Figure 2.10: Schematic diagram of a Doherty amplifier

transfer characteristics results in an overall linear power response as shown in figure 2.9 while at the same time, efficiency has been kept at its maximum level above the 6-dB back-off point, up to the maximum power level. Figure 2.10 shows the schematic diagram of a Doherty amplifier and Figure 2.11 shows current/voltage relationships of the carrier and peak amplifiers. Above the 6-dB back-off point, both devices are contributing to the load current. Their fundamental currents would be

$$I_m = \frac{I_{max}}{4}(1+\zeta), \tag{2.15}$$

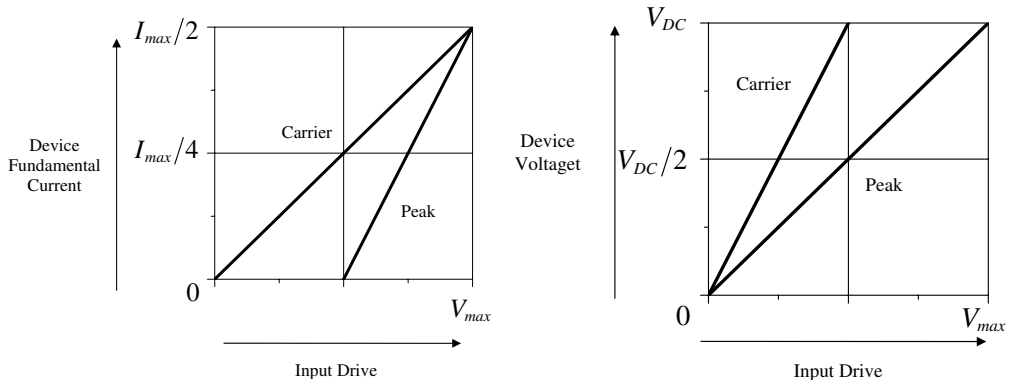


Figure 2.11: Device currents and voltages versus input drive

and

$$I_p = \frac{I_{max}}{2}\zeta, \tag{2.16}$$

where

$$0 \leq \zeta \leq 1.$$

$\zeta = 0$ corresponds to the 6-dB back-off point and $\zeta = 1$ corresponds to the maximum power level. It is assumed that both carrier and peak amplifier are identical and have the same I_{max}. Now, the load pulling relationships of equations 2.13 and 2.14 become

$$Z_{mT} = \frac{R_{opt}}{2}\left(1 + \frac{I_p}{I_{mT}}\right), \tag{2.17}$$

$$Z_p = \frac{R_{opt}}{2}\left(1 + \frac{I_{mT}}{I_p}\right). \tag{2.18}$$

It can be seen that at the maximum power level

$$I_{mT} = I_p = \frac{I_{max}}{2}, \tag{2.19}$$

$$Z_{mT} = Z_p = R_{opt}. \tag{2.20}$$

The relationship between the input and output voltages and currents of the $\lambda/4$-transmission line are

$$V_p I_{mT} = V_m I_m, \tag{2.21}$$

$$\left(\frac{V_p}{I_{mT}}\right)\left(\frac{V_m}{I_m}\right) = Z_T^2. \tag{2.22}$$

Combining equations 2.21 and 2.13 gives,

$$Z_{mT} = \frac{R_{opt}}{2}\left(1 + \frac{I_p Z_T}{V_m}\right). \tag{2.23}$$

The impedance seen by the carrier device is

$$Z_m = \frac{Z_T^2}{Z_{mT}} = \frac{2Z_T^2}{R_{opt}\left(1 + \frac{I_p Z_T}{V_m}\right)}. \tag{2.24}$$

The amplitude of the RF voltage swing at the output of the carrier device is

$$V_m = I_m Z_m = \frac{2I_m Z_T^2}{R_{opt}\left(1 + \frac{I_p Z_T}{V_m}\right)}.$$

Substituting for I_m and I_p from equations 2.15 and 2.16,

$$V_m = \frac{Z_T^2\left(\frac{I_{max}}{2}\right)(1+\zeta)}{R_{opt}\left(1 + \frac{\zeta\left(\frac{I_{max}}{2}\right)Z_T}{V_m}\right)}.$$

After re-arrangement,

$$V_m = \left(\frac{Z_T}{R_{opt}}\right)\left(\frac{I_{max}}{2}\right)\Big[Z_T + \zeta\left(Z_T - R_{opt}\right)\Big]. \tag{2.25}$$

If we choose $Z_T = R_{opt}$, the carrier device output voltage will become independent of input drive level (ζ) and it will become constant at

$$V_m = R_{opt}\left(\frac{I_{max}}{2}\right). \tag{2.26}$$

which is the maximum output voltage swing as desired. From equation 2.21 we can write,

$$\left(\frac{V_p}{I_m}\right) = \left(\frac{I_m}{V_p}\right) R_{opt}^2, \tag{2.27}$$

knowing that $Z_T = R_{opt}$

$$V_p = I_m R_{opt}. \tag{2.28}$$

Equation 2.28 and Figure 2.11 show that the power delivered to the load is linearly proportional to the input power. The final maximum power is twice as large as the power of each device. Assuming that the efficiency of both amplifiers is $\pi/4$ at maximum swing voltage, corresponding to class B operation, discussed in detail in section 2.2.1, the efficiency of each device will drop proportionally as the RF voltage swing decreases. For the low power regime, only the carrier device is active. The efficiency as shown in section 2.2.1, is

$$\eta = \frac{P_{RF}}{P_{dc}} = \frac{\pi}{4}\left(\frac{2v_i}{V_{max}}\right). \tag{2.29}$$

Above the break point, the RF output power is

$$P_{RF} = I_m^2 R_{opt}, \tag{2.30}$$

so from equations 2.9 and 2.5, we can write

$$P_{RF} = \left(\frac{I_{max}}{2}\right)\left(\frac{v_i}{V_{max}}\right)^2 V_{dc}. \tag{2.31}$$

The DC power consumption of the carrier device, for class B operation, is

$$P_{dcc} = \left(\frac{I_{max}}{\pi}\right)\left(\frac{v_i}{V_{max}}\right)V_{dc}, \tag{2.32}$$

and the DC power consumed by the peak amplifier will be

$$P_{dcp} = \left(\frac{I_{max}}{\pi}\right)\left(\frac{2v_i}{V_{max}-1}\right)V_{dc}, \tag{2.33}$$

so the total DC power consumption is

$$P_{dc} = \left(\frac{I_{max}}{\pi}\right)\left[3\left(\frac{2v_i}{V_{max}}\right) - 0.5\right]V_{dc}. \tag{2.34}$$

The overall efficiency from equations 2.31 and 2.34 is given by

$$\eta = \frac{\pi}{2}\frac{\left(\frac{v_i}{V_{max}}\right)^2}{3\left(\frac{v_i}{V_{max}}\right)-1}. \tag{2.35}$$

It can be easily seen that the efficiency will reach its maximum $\pi/4$ limit with both the maximum power condition $v_{in} = V_{max}$ and 6 dB backoff point $v_i = V_{max}/2$. For $v_i \leq V_{max}/2$, efficiency rolls off. Figure 2.12 shows the efficiency of the Doherty amplifier [2].

Let's now take a closer look at how the impedance transformation takes place. Below the break-point, the Doherty amplifier looks like the one shown in Figure

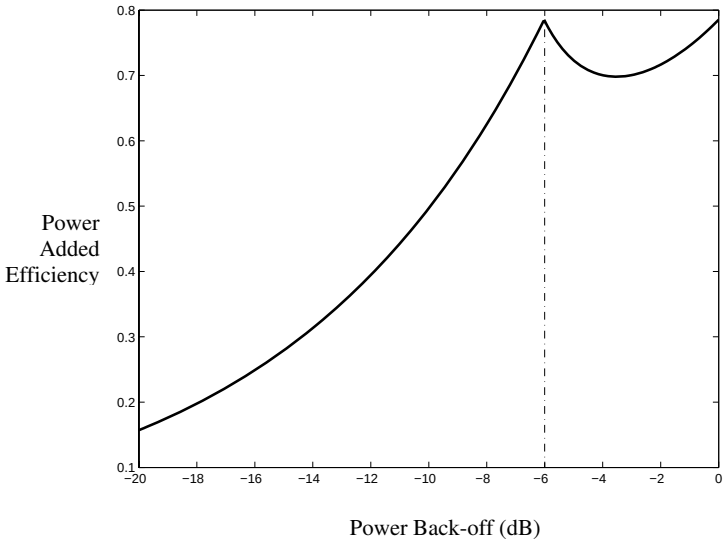


Figure 2.12: Power added efficiency of a Doherty amplifier versus power backoff

2.13. The $\lambda/4$-transmission line with $Z_T = R_{opt}$ transforms an impedance of $R_{opt}/2$ to $2R_{opt}$, which is twice as large as the optimum impedance for the carrier amplifier. At this point, the carrier device's output voltage swing reaches saturation with only half of the maximum input drive. This is exactly the point where the peak device is turned on to contribute to the load current and reduce the impedance seen by the carrier amplifier. This way, the carrier amplifier current can increase while its rail-to rail voltage swing remains constant. With its output voltage swing kept constant, the carrier amplifier can retain the constant maximum efficiency within the whole power range above the break-point. At maximum power level, as shown in Figure 2.14 , carrier and peak amplifiers supply equal maximum current to the load. The impedance seen at the input of the $\lambda/4$-transmission line will, therefore, become R_{opt}. Figure 2.15 shows the pulling effects on the impedances seen by the

carrier and peak amplifiers versus the input power drive.

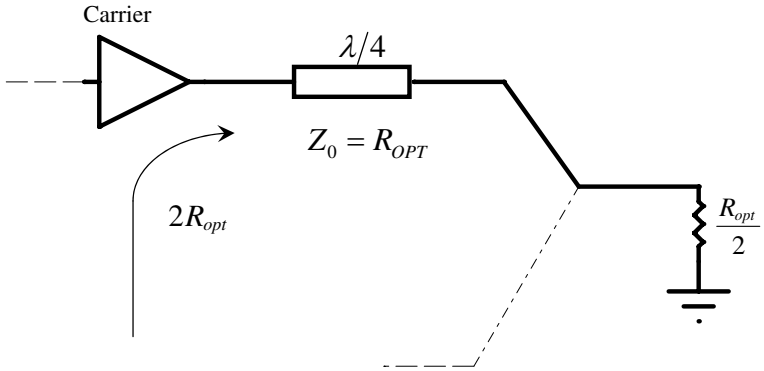


Figure 2.13: Doherty configuration below the break-point

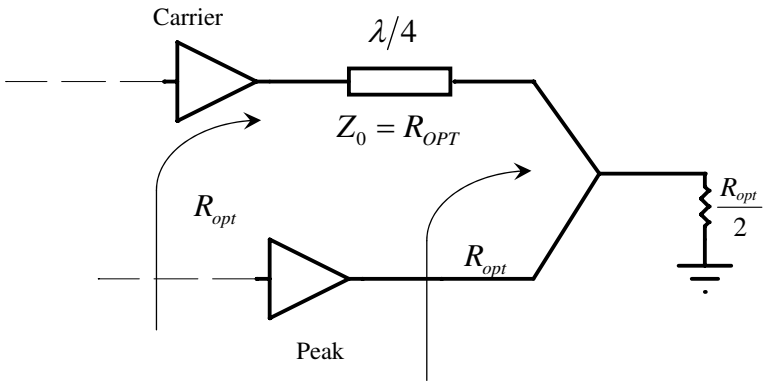


Figure 2.14: Doherty configuration above the break-point

Realization of defined characteristics of the peak amplifier brings a lot of problems. It is required for the peak amplifier to remain shut-off up to a certain break point (6-dB backoff from the maximum level in conventional Doherty power amplifier). The most straight forward way to obtain such a performance is to bias it in deep class C mode [2]. Another problem with the peak amplifier is that, once

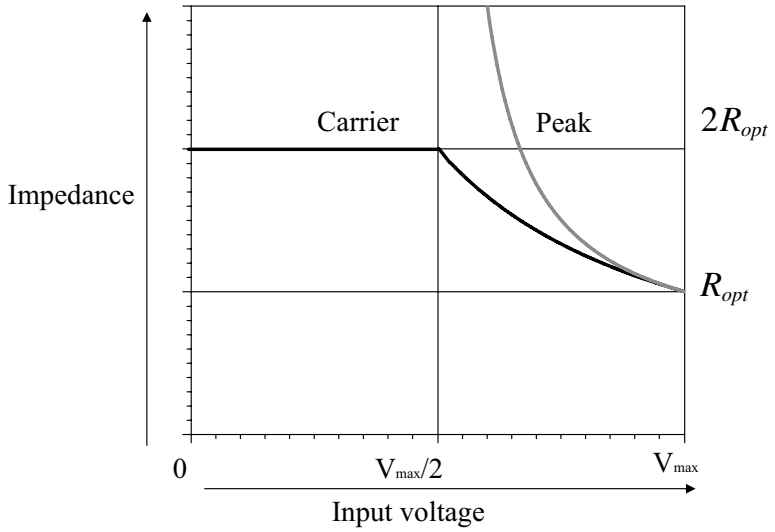


Figure 2.15: Load pulling effects on the carrier and peak amplifier

turned on, it has to race up to the maximum current with only half as much increase in the input drive. This implies that the peak amplifier should have double the periphery of the carrier amplifier. There are several practical problems involved with this configuration due to nonlinearities associated with a class-C amplifier. There are also gain, device periphery and breakdown issues. It turns out that it is possible to overcome these issues by applying certain techniques to the peak amplifier. Uneven power drive and bias tracking are some of the recently developed techniques which are discussed in the following sections.

2.2.2 Extended Doherty Amplifier

The threshold point for improved efficiency in the classic Doherty amplifier was the 6-dB back-off point. Raab [13] showed that the peak efficiency region can be

extended by using different transistors with different transfer characteristics resulting in so-called "asymmetrical Doherty power amplifier" which, in fact, is a generalized Doherty amplifier. The asymmetrical Doherty amplifier is most useful in applications where the envelope peak-to-average ratio is higher than 6-dB. The ratio between maximum currents of the carrier and peak amplifier is now a new design parameter which can stipulate the back-off break point [2]. Figure 2.16 shows the efficiency of an assymetrical Doherty amplifier for which the breakpoint has been set to -12 dB backoff level. It is important to note that as the breakpoint is extended, a dip in efficiency will appear in the medium range between the breakpoint and the maximum power efficiency peaks. The dip will be deeper as the range of efficiency enhancement increases. Peak power added efficiencies at ranges as wide as 15-dB back off from maximum power have been reported [14]. Figure 2.17 shows the voltage and current for a typical asymmetrical Doherty power amplifier.

2.2.3 Doherty Power Amplifier with uneven power-divide

In this configuration, higher input power is delivered to the peaking cell compared to the carrier cell for eliminating the need for a higher device periphery for the peaking cell. Optimizing linear power operation, especially for appropriate load modulation, is a second advantage. Both cells are matched differently to further

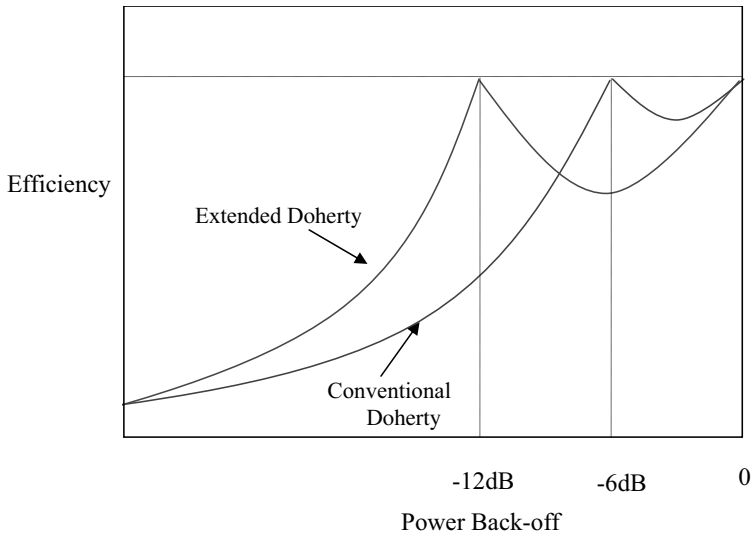


Figure 2.16: Efficiency of an assymetrical Doherty amplifier compared with a conventional Doherty amplifier

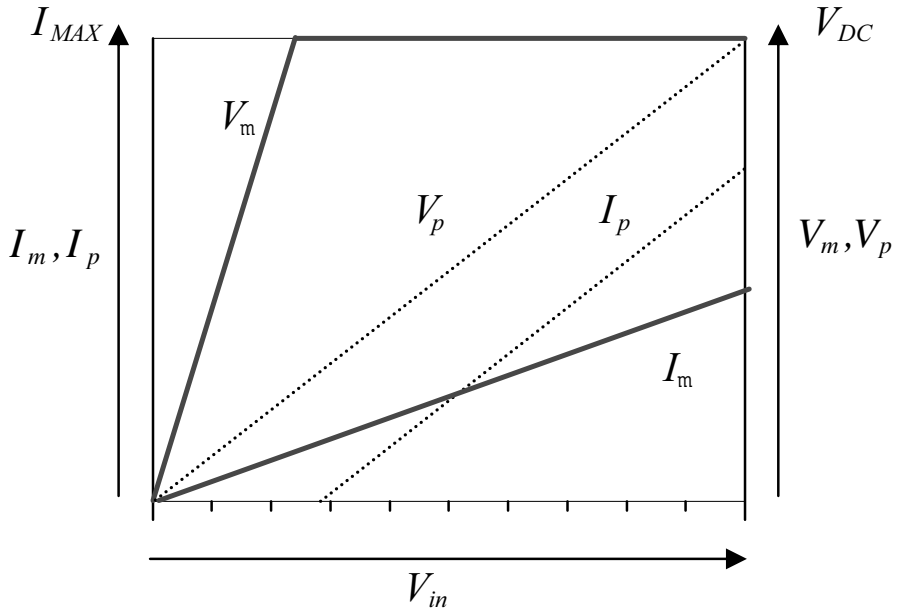


Figure 2.17: Current and voltage characteristics of assymetrical Doherty amplifier

optimize the performance [15]. This way, similar cells can be used as carrier and peak amplifiers. Reported results [16],[17] show that with an uneven power divide between carrier and peak amplifier optimal load modulation can be obtained. Figure 2.18 shows a schematic diagram of the proposed circuit.

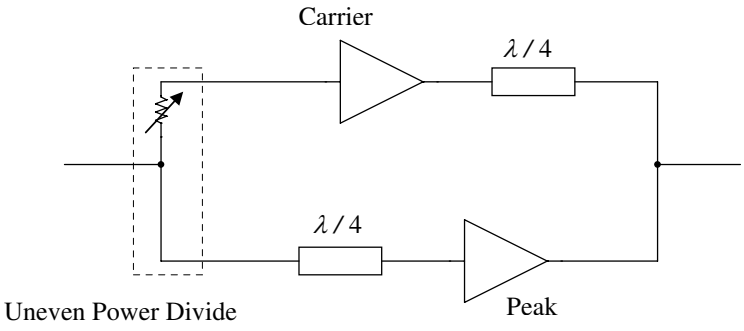


Figure 2.18: Doherty amplifier with uneven power divide

2.2.4 Doherty Amplifier with offset lines

It has been assumed by far that in the lower power regime when the peak amplifier is turned off, it has an ideally infinite output impedance. For a real device, however, this assumption is not true. In fact, the peak amplifier has a pretty low output impedance when it is shut down. This has inspired designers to employ offset lines at the output of carrier and peak amplifiers to adjust the circuit for the optimum output impedances at different power levels [18]. Figure 2.19 shows the block diagram of the proposed improvement. With proper selection of the offset line lengths and characteristic impedances, it is possible to fully match the carrier and

peak devices for optimum gain, linearity, and efficiency.

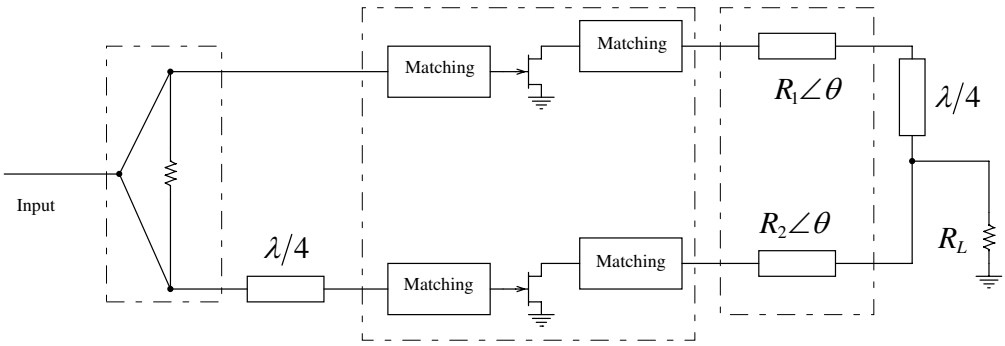


Figure 2.19: Doherty amplifier with offset lines

2.2.5 Doherty Amplifier with Envelope Tracking

It has been well demonstrated in previous sections that the peak amplifier is a demanding part of the Doherty amplifier. Envelope tracking method is one of the approaches taken by designers to alleviate the peak amplifier's stringent requirements. Figure 2.20 shows a block diagram of a Doherty amplifier employing envelope tracking. An envelope detector extracts the envelope of the input signal and modifies the bias of the peak amplifier adaptively. The peak device is biased to operate at deep class-C (or virtually shut down) for the low power levels. The bias will change adaptively making the peak amplifier contribute more current to the load as the input power level increases. At the maximum power level, the peak amplifier will have the same bias as the carrier amplifier and its current contribution to the load will be equal to the carrier amplifier. Thus, the bias adaptation

can help the peak amplifier to make up for the extra periphery it needs to catch up with the carrier amplifier. Therefore, identical devices can be used as carrier and peak amplifiers. Figure 2.21 shows the performance of the bias adaptation technique compared to the one with no bias adaptation. Practical implementations [19][20][21] have used detector diodes for envelope detection, video processing and wave-shaping in bias adaptation circuits.

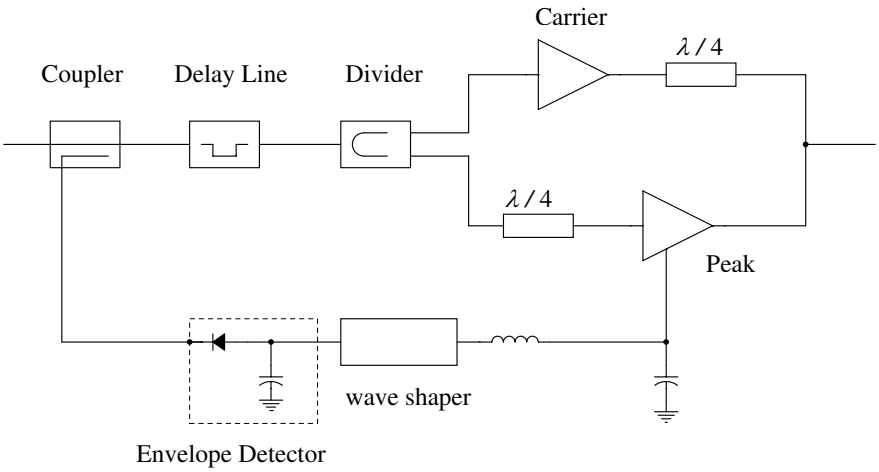


Figure 2.20: Block diagram of a Doherty amplifier with bias adaptation

2.2.6 Multi-stage Doherty Amplifier

In section 2.2.2, asymmetrical Doherty amplifiers were discussed. It was shown that by using dissimilar devices for the carrier and peak amplifier the breakpoint can be stipulated. The disadvantage of that approach is that extending the high efficiency region will result in a drop of efficiency between the peak points. A multistage Doherty amplifier maintains the maximum efficiency over a wide range

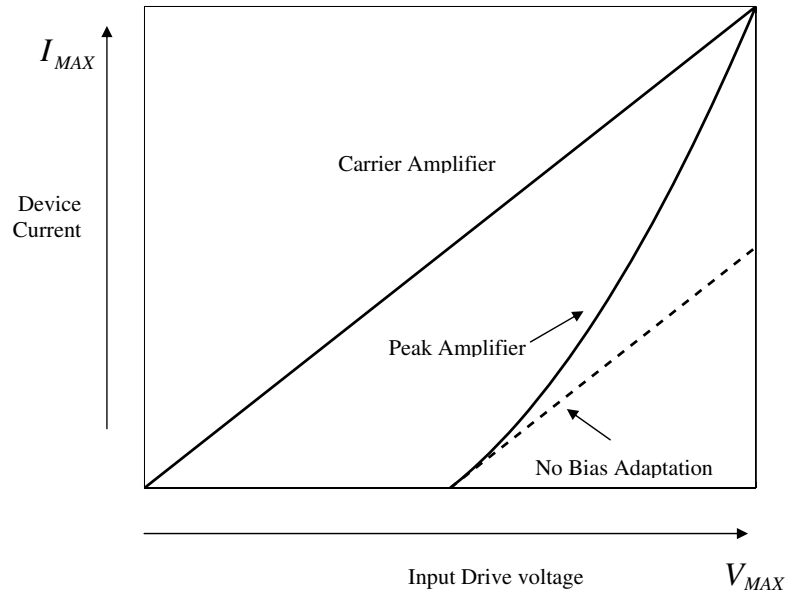


Figure 2.21: Bias adaptation for peak amplifier

without significant drop throughout the backoff region. The block diagram of an N-stage Doherty amplifier is shown in Figure 2.22. It consists of several Doherty amplifiers nested together so that the carrier amplifier of a Doherty amplifier is a Doherty amplifier by itself and so on. With proper matching and biasing, a flat high efficiency can be achieved in the backed off region. Figure 2.23 shows the efficiency of a multi-stage Doherty amplifier in comparison with that of an assymetrical Doherty power amplifier. Up to 3-stage Doherty amplifiers have been implemented and reported [22].

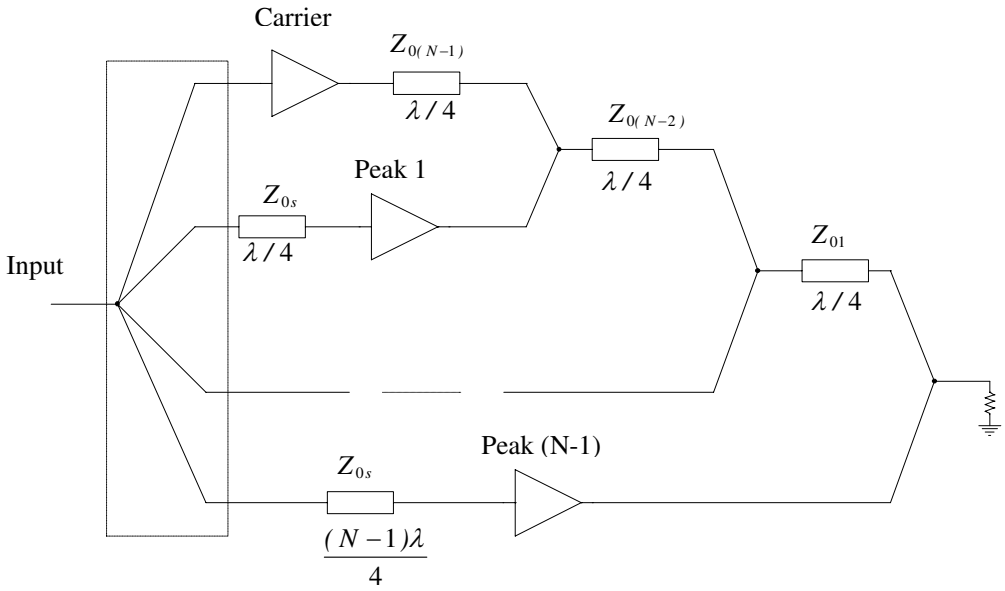


Figure 2.22: Block diagram of N-way Doherty amplifier

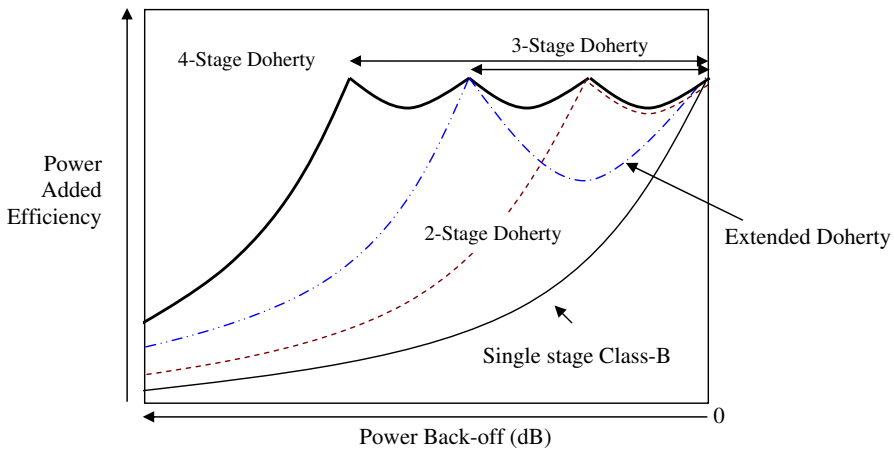


Figure 2.23: Efficiency of a multi-stage Doherty amplifier

2.2.7 Doherty Amplifier with active power splitter

One of the disadvantages of the conventional Doherty amplifier is that the required passive elements such as the input power splitter and the quarter wave impedance inverter have a large size. Therefore, realizing a highly integrated Doherty amplifier brings numerous physical challenges. Research has been going on to alleviate this issue by novel topologies and replacing these elements with compact alternatives. In order to address these issues, several novel techniques have been demonstrated which will be discussed in following sections. An active power splitter was proposed by J. Kim et al [1], which substitutes the input power splitter in order to reduce the size of the Doherty amplifier to make it suitable for handset applications. The schematic diagram of the proposed circuit is shown in Figure 2.24. According to the authors no compromise has been made in power amplifier performance except that the bandwidth of the circuit is poor.

2.2.8 The Series-type Doherty Amplifier

The series-type Doherty amplifier was reported by J.Jung et al [23]. The brilliant idea behind this approach is to place the carrier amplifier in series with the peak amplifier as shown in Figure 2.25. The input of the peak amplifier is driven by the output of the carrier amplifier through a carefully designed matching network. This way, the need for a bulky, hybrid power splitter is eliminated. Promising

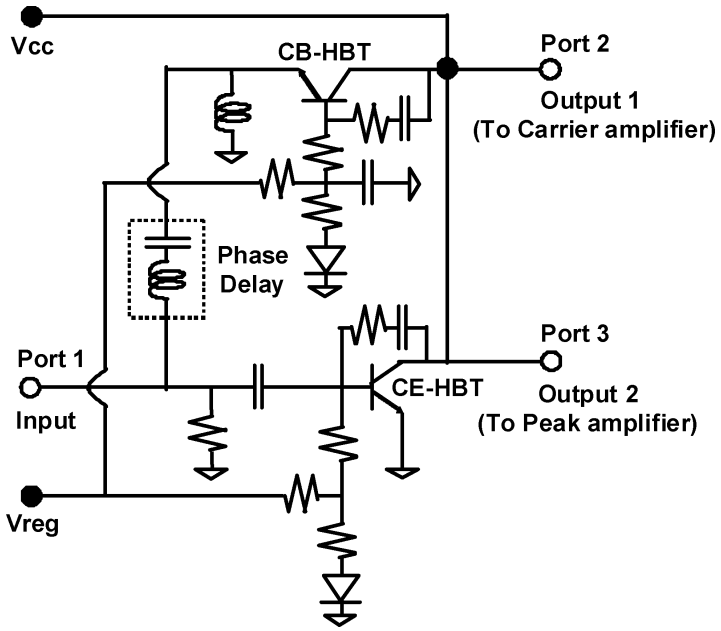


Figure 2.24: Schematic of the active phase splitter proposed in [1]

performance has been reported [24].

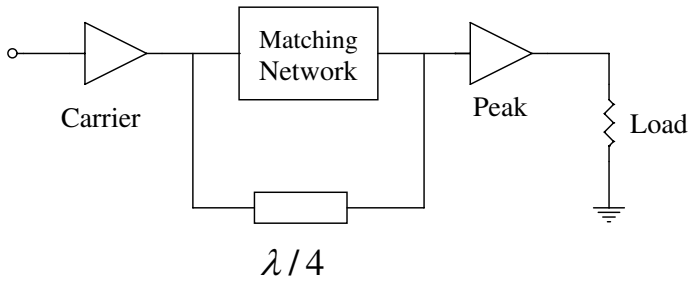


Figure 2.25: Series-type Doherty amplifier

2.2.9 Linearizing The Doherty Power Amplifier

It was shown in section 2.2.1 and Figure 2.9 that a Doherty amplifier is a linear amplifier in ideal conditions. The nonlinearities caused by the load modulation will

theoretically cancel out one another and the overall input-output power response will be linear. However, things are different in practice. Any mismatch or practical imperfection in the peak amplifier will cause the Doherty amplifier to suffer severe linearity issues. Several methods such as feedforward and predistortion techniques have been used to "linearize" the Doherty amplifier. There are several practical considerations in the implementation of feedforward systems. The error amplifier [25] must be highly linear, which results in a low efficiency topology (e.g. Class A) and limits the total efficiency of the feedforward system [26]. The most promising technique to linearize a power amplifier is "digital predistortion". It consists of an arrangement at the input of the power amplifier which modifies the input signal at the baseband level and suppresses harmonic components at the output of the amplifier. Thus, the overall configuration performs in a linear fashion [27] [28] [29]. Figure 2.26 shows the block diagram of a Doherty amplifier linearized with a digital predistorter.

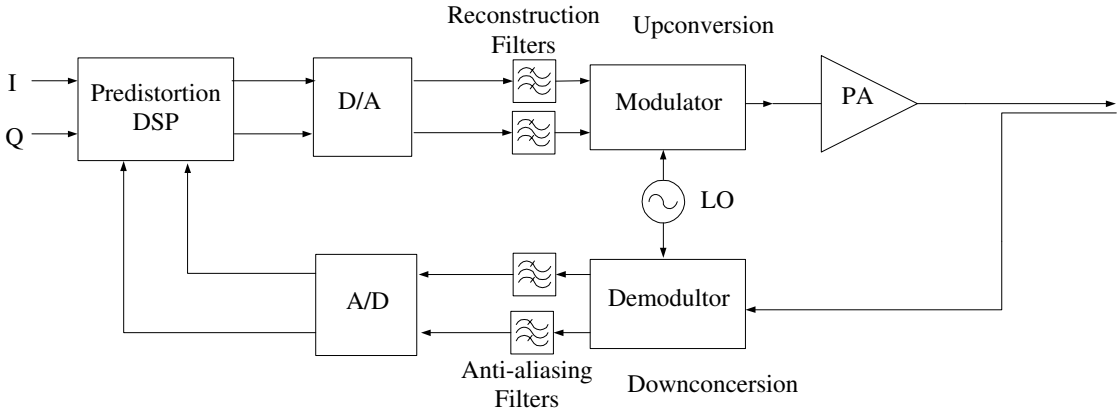


Figure 2.26: Block diagram of a digital predistorter

Chapter 3

A Novel Topology for the Doherty Amplifier

3.1 Problems With The Conventional Approach

It has been discussed earlier that the conventional Doherty amplifier employs a $\lambda/4$ transmission line to invert the load pulling effect of the peak amplifier. This is because the impedance seen by the main amplifier has to decrease as the input power drive increases. The conventional usage of the passive $\lambda/4$ transmission line is the origin of numerous problems. These problems are discussed in this chapter before introduction of a new approach which promises to eliminated these issues.

3.1.1 Large Size

At frequencies used for wireless telecommunications, the $\lambda/4$ impedance inverter appears to be large and bulky. With the current trend of RF transceivers toward miniaturization and the ongoing downscaling of the semiconductor components, this is specially a barrier against realization of highly integrated Doherty power amplifiers. The most commonly used solution for this problem is to realize the impedance inverter using lumped components [30], [31]. Figure 3.1 shows a π-network arrangement that can replace the $\lambda/4$ transmission line and act like an impedance inverter with the following conditions

$$L = \frac{Z_0}{\omega_0}, \tag{3.1}$$

$$C = \frac{1}{Z_0 \omega_0}. \tag{3.2}$$

Although this configuration can significantly reduce the design size [32] [33], it imposes bandwidth problems. This will be explained in the next section. A novel topology will be proposed shortly which promises to overcome the size issue.

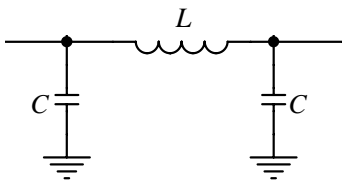


Figure 3.1: Lumped-element realization of the transmission line

3.1.2 Bandwidth

The $\lambda/4$ transmission line has a narrow bandwidth. Theoretically, it only works as a perfect inverter at a single frequency. This is a major disadvantage of the Doherty amplifiers with the conventional approach. The problem is even more severe with the lumped component alternative discussed in the previous section since it has a narrower bandwidth. The bandwidth of the $\lambda/4$ transmission line depends on its termination impedance. The closer the termination impedance is to the characteristic impedance, the wider is the bandwidth. The Doherty amplifier requires the $\lambda/4$ impedance inverter to transform a load impedance of $R_{opt}/2$ to $2R_{opt}$ in the lower power regime. The bandwidth of this transformation is shown in figure 3.2 for both a $\lambda/4$ transmission line and its lumped-component equivalent. The narrow bandwidth of the Doherty amplifier is an important problem and to the best of the author's knowledge, no research has been reported in the literature in this regard. The novel topology presented in this dissertation shows promising potentials to overcome the bandwidth issue.

3.1.3 Effect of Parasitics on Load Modulation

The analysis presented in section 2.2.1 assumed that the the carrier and peak devices were ideal in the sense that the impedance introduced to the output of each device is directly seen by the device current generators. This is obviously

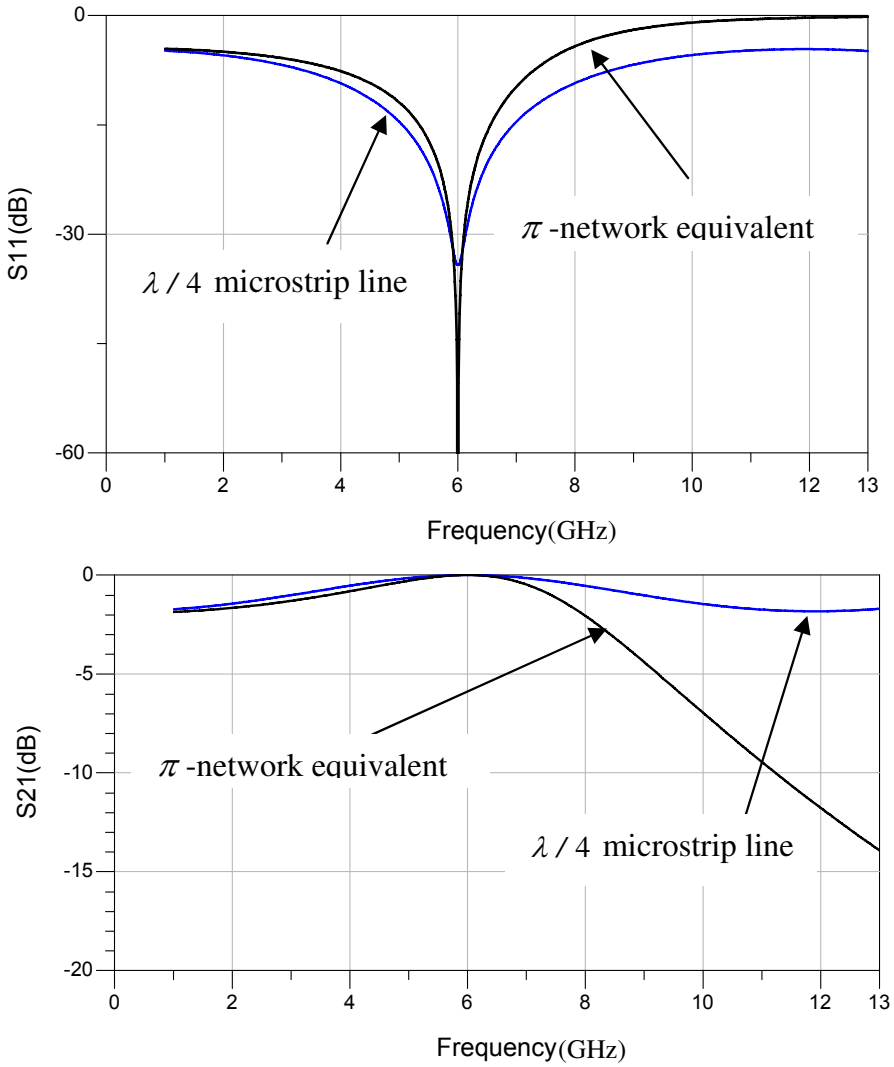


Figure 3.2: Bandwidth of a $\lambda/4$-transmission line compared to its lump element equivalent

not true when real devices are involved. The impedance seen at the output of the carrier and peak amplifier are modified by the parasitic capacitors (such as drain capacitance) and inductors (such as bond wires). In other words, the load impedance seen from the device lead reference plane is different from the one seen at the current generator reference plane. The very important point that should be carefully noted is that there is a subtle difference between compensating for parasitic effects in typical matching problems with fixed passive loads and the problems in which load pulling effects are involved. In the former, the parasitics could be compensated for, by absorbing them in matching components while in the latter, the solution is not trivial. Since the load is being modified at different power levels, it is impossible to compensate for the parasitics and produce the required load impedance at every power level with a static matching network. Figure 3.3 shows a current generator driving a load with the parasitics in between. For the correct Doherty operation, the impedance seen at the lead of the transistor is pulled from $2R_{opt}$ to R_{opt} as the power level increases from the backoff breakpoint to the maximum power level but the impedance seen at the current generator does not follow the same trajectory due to the existence of parasitics.

The above discussion implies that simply inverting the load impedance may not deliver the performance required for the Doherty operation. Higher degrees of freedom are required to present the suitable impedance to the lead of the transistor for the entire power level range. The synthesis of proper impedances for

the carrier amplifier at every power level requires a more sophisticated impedance transformation approach which is the subject of this research.

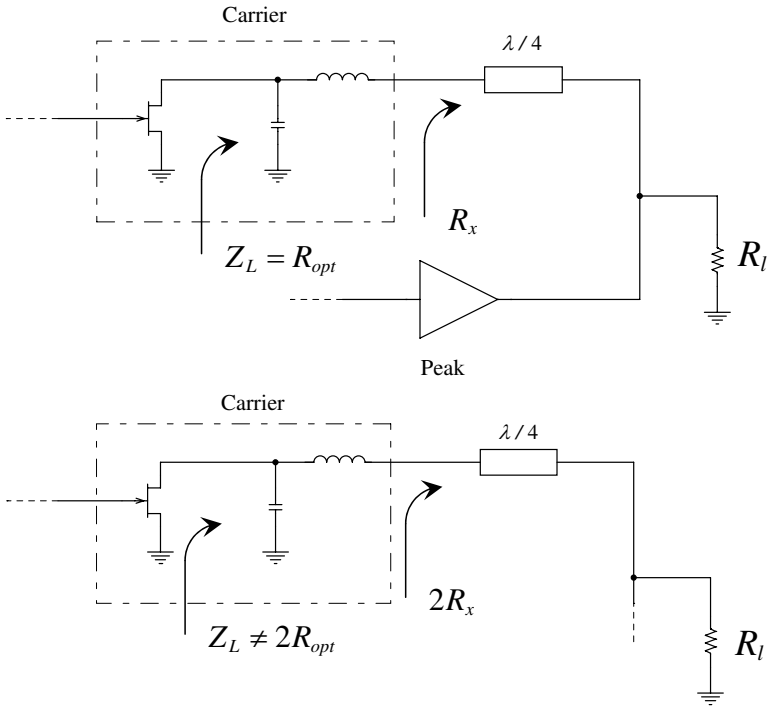


Figure 3.3: Effect of device parasitics on load modulation

3.2 The Novel Impedance Transformation

The problems associated with the $\lambda/4$ impedance inverter, used in the conventional Doherty amplifier, have been well elaborated in previous sections. In this section, an alternative topology is proposed which could emulate the function of the $\lambda/4$ impedance inverter while eliminating its disadvantages. The principle idea is presented in the following sections and the theoretical development of the concept is

carried out subsequently.

3.2.1 Envelope Tracking for Load Modulation

In section 2.1.2, the application of envelope tracking in efficiency enhancement was discussed. Also in section 2.2.5, it was shown that envelope tracking could be used to dynamically modify the peak amplifier bias in order to avoid high periphery devices. The principle behind this technique was to feed the envelope information separately to the peak amplifier so that it could somewhat adjust itself for optimum efficiency for the entire power range. The idea of this work is to employ the envelope tracking not only for bias adaptation of the peak amplifier, but also for impedance transformation required for the carrier amplifier. The block diagram of the proposed structure is shown in Figure 3.4. The envelope detector serves for two purposes now. Firstly, it controls the bias of the peak amplifier. Secondly, it controls a "special" piece of circuit which presents the required impedance for the carrier amplifier dynamically according to the input signal envelope. It should be noted that since this "special" piece of circuit introduces a phase delay in the carrier amplifier path, means should be provided to compensate for this delay in the peak amplifier path so that the output currents of the carrier and peak amplifier combine in-phase. Hence, a second circuit is placed before the peak amplifier to compensate for the delay caused by the first. The details of this piece of circuit,

which should be compact and capable of wideband load modulation, is described in following sections.

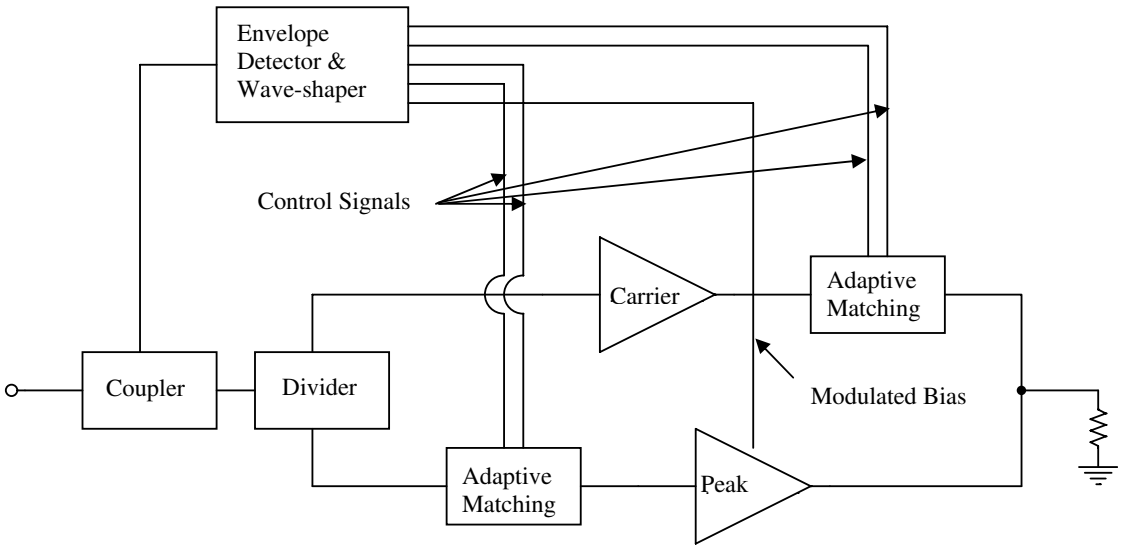


Figure 3.4: Block diagram of proposed topology

3.2.2 Adaptive Impedance Matching

In section 2.2.1, it was shown that in order for the Doherty amplifier to work, it is required for the load seen by the carrier amplifier to travel from $2R_{opt}$ to R_{opt} as the power level increases from backoff breakpoint to the maximum power level (Figure 2.15). In this section, an adaptive topology is proposed which can synthesize the required impedance at the output of the carrier amplifier for optimum Doherty operation. Figure 3.5 shows the general schematic diagram of the proposed topology. It consists of a π-network similar to the one discussed in section 3.1.1. Shunt capacitors have been replaced by variable capacitors which can be modified

using control signals based on the input signal envelope. The variable capacitors C_1 and C_2 can be realized using single varactor diodes or possibly multi-varactor topologies which will be discussed in next sections. In order to understand how the impedance transformation takes place, two extreme cases are distinguished without losing the generalization of the problem. Case I explains the impedance transformation required for the lower power regime (below the backoff breakpoint) and case II discusses the impedance transformation required at the maximum power level.

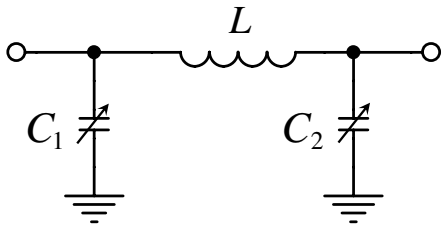


Figure 3.5: Adaptive impedance transformation

Case I:

The desired load impedance required for the carrier amplifier in the lower power regime is $2R_{opt}$. For the arrangement in Figure 3.5, let's assume that the variable capacitor C_1 is set to be equivalent to a capacitor C, while C_2 is set to zero. The equivalent circuit of this condition is shown in Figure 3.6. This is, in fact, a simple LC matching network which will transform the load impedance $R_{opt}$to $2R_{opt}$with

(a) C_2 is set to give zero capacitance (b) Equivalent circuit

Figure 3.6: Adaptive load modulation with variable capacitors, Case I

the following conditions

$$2R_{opt} = \frac{1}{\omega C}, \tag{3.3}$$

$$R_{opt} = \omega L. \tag{3.4}$$

The load impedance seen by the carrier amplifier is, indeed, in agreement with Doherty operation requirement seen in Figure 2.15.

Case II:

At maximum power level, it is important to note that the load impedance seen by the carrier device has changed due to the peak amplifier's load pulling effect. Since the peak amplifier contributes equal current to the load as the carrier amplifier, the load impedance seen by each will be $2R_{opt}$. Now let's assume that this time, C_1 is set to zero and C_2 is equivalent to capacitor C. The equivalent circuit is shown in Figure 3.7 which, satisfying the same conditions as equation 3.3 and 3.4, will transform an impedance of $2R_{opt}$ to R_{opt}. This is indeed the required impedance for the carrier amplifier at maximum power level for Doherty operation.

(a) C_1 is set to give zero capacitance (b) Equivalent circuit

Figure 3.7: Adaptive load modulation with variable capacitors, Case II

In real circumstances control signals which bias the varactors can be optimized to synthesize the precise impedance required by the main amplifier at every input power level. It is obvious that by using more than two variable capacitances, impedance transformation can be carried out in a wider bandwidth. Therefore, broadband load modulation can be achieved using this topology.

3.2.2.1 Varactor-based RF Adaptability

Varactors have been typically used for adaptive filtering and variable impedance matching. The voltage dependent capacitance of varactors has made them proper choices for RF adaptability. For the proposed topology shown in Figure 3.5, varactors are used as variable capacitances. Linearity of varactor based circuits is an immediate concern, which is discussed in detail in the next chapter. It will be shown that by a certain arrangement of multi-varactor topologies, it is possible to minimize distortion.

3.2.3 Solution Generalization, Broadband Performance

The proposed adaptive impedance transformation scheme was basically a single stage π-network. To obtain a broader bandwidth, a multi-stage ladder network of LC connection with varactors representing the capacitances can be realized. Figure 3.9 shows the increase in the bandwidth as the number of LC stages increases. A drawback of this approach is that the number of control signals (to bias the varactors) increase with the number of LC stages.

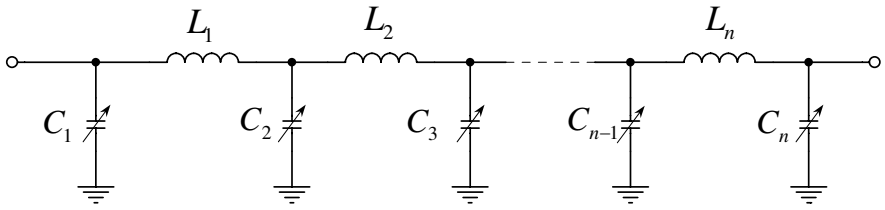
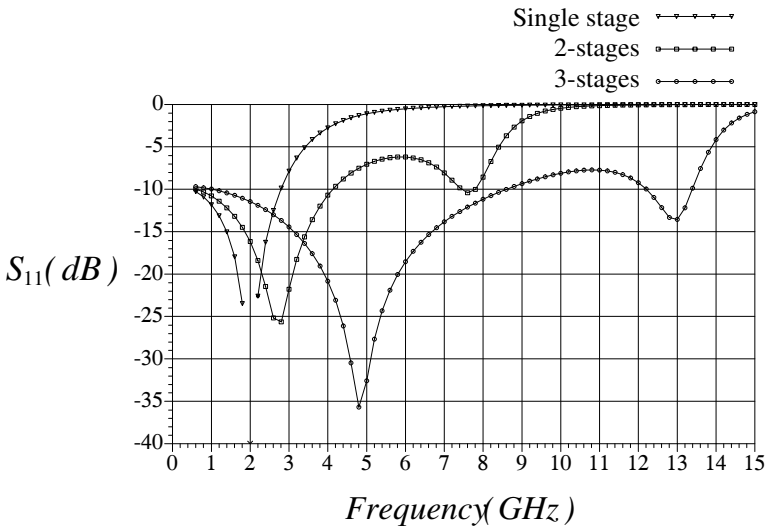
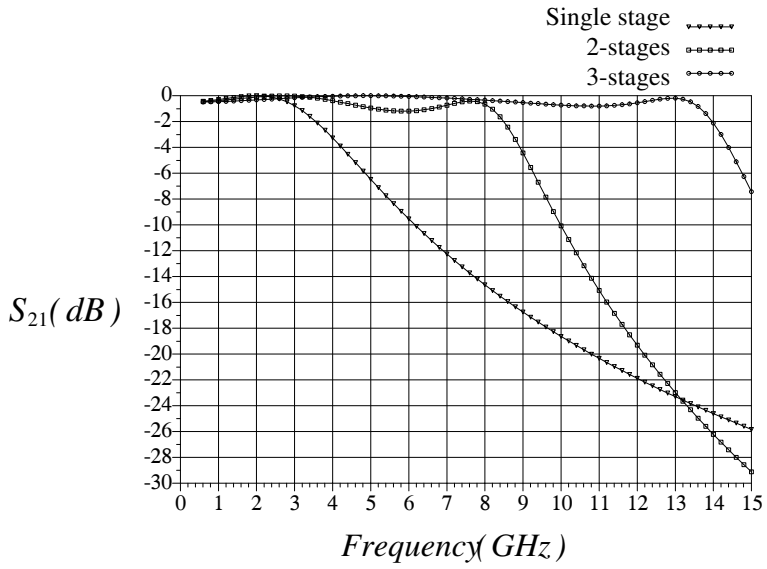


Figure 3.8: Generalization of the topology for broadband performance



(a) S_{11}



(b) S_{21}

Figure 3.9: Bandwidth of impedance transformers with different stages

Chapter 4

Theoretical Development

The theoretical background to support the proposed Doherty amplifier is detailed in this chapter. We begin by device modeling and elaborate on the theory behind the model used. Load pull technique is discussed next. A complete theoretical discussion on the load pull concept is provided for two reasons. Firstly, the whole idea behind the Doherty amplifier is efficiency enhancement by load modulation. In a Doherty amplifier, load modulation is carried out by the load pulling effect of a second generator. Therefore, a theoretical investigation of the load pull concept is required. Secondly, load pull is an essential procedure to characterize highly nonlinear power amplifiers. Varactor-based adaptive circuits are considered next. Characteristics such as linearity and tuning-range of several basic varactor-based topologies are compared before an analysis of the proposed varactor-based impedance inverterer is presented.

4.1 Device Modeling

The transistor selected for realization of the proposed Doherty amplifier is Transcom's TC2571 Pseudomorphic-HEMT. The model provided by the manufacturer for the chosen transistors is TOM-2. This model is explained in detail in following sections.

4.1.1 TOM-2 Model

TOM[1]-2 [34] is an improved model for GaAs FETs. It is based on the original Triquint model (TOM-1) with refinements to improve accuracy in the knee and sub-threshold region. Particular attention is paid to the temperature effects. TOM-2 retains the desirable features of TOM-1 while improving performance in the subthreshold (V_{gs}) near cut-off, and knee regions (V_{ds} of 1 volt or less). Additional temperature coefficients related to the drain current are included and major deficiencies in the behavior of the capacitance as a function of temperature are corrected.

4.1.2 Equivalent Circuit

Figure 4.1 shows the basic model used in TOM-2. The model specifies how the current sources and the variable capacitors depend on bias conditions and temperature [35]. The equations reference the voltages across the "intrinsic" portion of

[1]Triquint Own Model

the FET as outlined in the figure. The intrinsic voltages are denoted as V_{gs} and V_{ds} for the gate-to-source and drain-to-source respectively. The model does not provide a mechanism for modeling the low frequency drain conductance dispersion that is well known in GaAs FETs. This effect is modeled by an external subcircuit with feedback coupled through a low pass RC network which is beyond the scope of this dissertation.

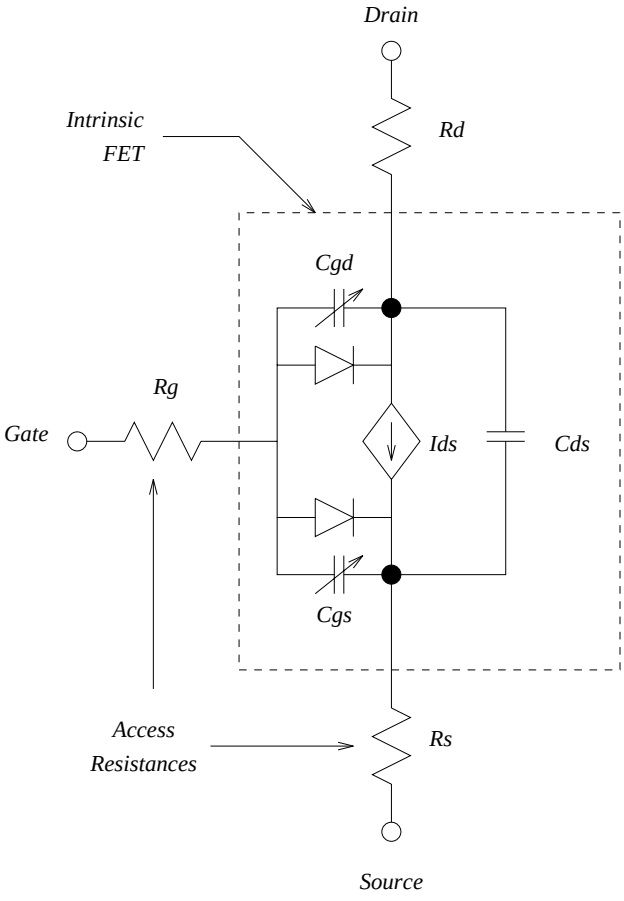


Figure 4.1: TOM-2 model

4.1.3 Basic Equations

4.1.3.1 Current Source Equations

The following expression is used to compute I_{ds} for the current source in Figure 4.1,

$$I_{ds} = \frac{I_{dso}}{1 + \delta V_{ds} I_{dso}}, \tag{4.1}$$

where

$$I_{dso} = w\beta V_g^Q . F_d\left(\alpha V_{ds}\right), \tag{4.2}$$

$$F_d(x) = \frac{x}{\sqrt{1+x^2}}, \tag{4.3}$$

and V_g is given by

$$V_g = QV_{st} \ln\left[\exp\left(\frac{V_{gs} - V_{to} + \gamma V_{ds}}{QV_{st}}\right) + 1\right], \tag{4.4}$$

where V_{to} and γ are constants and w is the device width. In general, we expect V_{st} to be near the thermal voltage kT/q, or about $26mV$ at 25 °C. q is the magnitude of the electrical charge on the electron (1.6×10^{-19} C) This leads us to present the V_{st} by an ideality factor, N_{st}. Thus

$$V_{st} = N_{st}\left(\frac{kT}{q}\right). \tag{4.5}$$

In addition, it is observed that the subthreshold slope varies slightly with V_{ds}, so a linear dependence is considered to account for this,

$$N_{st} = N_g + N_d V_{ds}. \tag{4.6}$$

Note that $N_{st} = 0$ corresponds to no subthreshold, that is, the current cuts off sharply at threshold. This behavior is similar to a diode where setting the ideality factor equal to zero results in a piecewise linear behavior [34]. The gate current, I_g, is the sum of the current due to the gate-drain diode, I_{ds}, and the gate-source diode, I_{gs}. These currents are given by the classic diode formula,

$$I_g = I_{gs} + I_{gd}, \tag{4.7}$$

$$I_{gs} = wI_s(e^{qV_{gs}/nkT} - 1), \tag{4.8}$$

$$I_{gd} = wI_s(e^{q(V_{gs}-V_{ds})/nkT} - 1). \tag{4.9}$$

The total drain current, I_d includes a component flowing from the gate which is

$$I_d = I_{ds} - I_{gd}. \tag{4.10}$$

4.1.3.2 Capacitance Equations

The Capacitance equations are based on those proposed by Statz, et. al.[36]

$$C_{gs} = \frac{C_{gso}}{2\sqrt{1-\frac{V_n}{V_{bi}}}}\left\{1+\frac{V_{eff}-V_{to}}{\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}}\right\} \times \frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\delta}\right)^2}}\right\} + \frac{1}{2}C_{gdo}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\delta}\right)^2}}\right\}. \tag{4.11}$$

$$C_{gd} = \frac{C_{gso}}{2\sqrt{1-\frac{V_n}{V_{bi}}}}\left\{1+\frac{V_{eff}-V_{to}}{\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}}\right\} \times \frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\delta}\right)^2}}\right\} + \frac{1}{2}C_{gdo}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\delta}\right)^2}}\right\}, \tag{4.12}$$

where,

$$V_{eff} = \frac{1}{2}\left(V_{gs}+V_{gd}+\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\delta}\right)^2}\right), \tag{4.13}$$

$$V_n = \frac{1}{2}\left(V_{eff}+V_{to}+\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}\right). \tag{4.14}$$

It is very important to note that these equations do not satisfy "charge conservation" with regard to the drain-source charge over a bias cycle. It has been argued that this will not pose a problem [37]. However, these equations may be difficult to implement in simulators whose capacitance is always the derivative of an internal state variable (charge).

4.1.3.3 Temperature Effects

An important aspect of modeling the GaAs FETs is a correct description of the behavior as a function of temperature.

$$I_s(T) = I_s \exp((T/T_{nom} - 1)qE_g/nkT)(T/T_{nom})^{Xti/n}, \tag{4.15}$$

$$V_{to}(T) = V_{to} + V'_{to}(T - T_{nom}), \tag{4.16}$$

$$V_{bi}(T) = V_{bi} + V'_{bi}(T - T_{nom}), \tag{4.17}$$

$$V_{max}(T) = V_{max} + V'_{bi}(T - T_{nom}), \tag{4.18}$$

$$\alpha(T) = \alpha \times 1.01^{\alpha'(T - Tnom)}, \tag{4.19}$$

$$\beta(T) = \beta \times 1.01^{\beta'(T - T_{nom})}, \tag{4.20}$$

$$\gamma(T) = \gamma'(T - T_{nom}), \tag{4.21}$$

$$R_g(T) = R_g(1 + R'_g(T - T_{nom})), \tag{4.22}$$

$$R_s(T) = R_s(1 + R'_s(T - T_{nom})), \tag{4.23}$$

$$R_d(T) = R_d(1 + R'_d(T - T_{nom})), \tag{4.24}$$

$$C_{gs}(T) = C_{gs}(1 + C'_{gs}(T - T_{nom})), \tag{4.25}$$

$$C_{gd}(T) = C_{gd}(1 + C'_{gd}(T - T_{nom})). \tag{4.26}$$

4.1.3.4 Model Parameters and scaling

A description of all model parameters along with scaling factors is briefed in Table 4.1.

4.1.3.5 Expressions for the Conductances

SPICE and many SPICE-like simulators, require analytical expressions for the conductances to be supplied. These expressions are used to compute small-signal parameters in Newton-Raphson integration routines. These expressions are derived directly from the expressions in section 4.1.3.1. In addition to expressions for the current sources, SPICE requires expressions for the conductances. To facilitate the computation, it is convenient to define a current reduction factor, p which is

Parameter	Symbol	Description	Units	Default	Scaling
LEVEL		model index (-1 for TOM-2)			
VTO	Vt	Threshold voltage	volt	-2.5	
ALPHA	α	Knee-voltage parameter	1/volt	2.0	
BETA	β	Tranconductance parameter	amp/volt-Q	0.1	
GAMMA	γ	Threshold shifting parameter	volt-1	0	
DELTA	δ	Output feedback parameter	volt	0.2	1/w
Q	Q	Power-law parameter		2	
NG	N_g	Subthreshold slope gate parameter		0	
ND	N_d	Subthreshold slope drain pull parameter	1/volt	0	
TAU	τ	Conduction current delay time	sec	0	
RG	R_g	Gate ohmic resistance	ohm	0	
RD	R_d	Drain ohmic resistance	ohm	0	$1/w$
RS	R_s	Source ohmic resistance	ohm	0	$1/w$
IS	I_s	Gate diode saturation current	amp	1×10^{-14}	
N	n	Gate diode ideality factor		1	
VBI	V_{bi}	Gate diode built-in potential	volt	1.0	
VDELTA	V_δ	Capacitance transition voltage	volt	0.2	
VMAX	V_{max}	Gate diode capacitance limiting voltage	volt	0.95	
CGD	C_{gd}	Gate-to-drain "zero-bias" capacitance	farad	0	w
CGS	C_{gs}	Gate-to-source "zero-bias" capacitance	farad	0	w
CDS	C_{ds}	Drain-to-source capacitance	farad	0	w
EG	Eg	Barrier height	volt	1.11	
XTI	Xti	I_s temperature exponent		0	
VTOTC	V'_{to}	V_{to}temperature coefficient(linear)	volt/ C	0	
VBITC	V'_{bi}	V_{bi}temperature coefficient(linear)	volt/ C	0	
ALPHATCE	α'	αtemperature coefficient(exponential)	%/ C	0	
BETATCE	β'	βtemperature coefficient(exponential)	%/ C	0	
GAMMATC	γ'	Linear temperature coefficient for γ	1/	0	
TRG1	R'_g	Linear temperature coefficient for R_g	1/	0	
TRD1	R'_d	Linear temperature coefficient for R_g	1/	0	
TRS1	R'_s	Linear temperature coefficient for R_g	11/	0	
CGDTCE	C'_{gdo}	Linear temperature coefficient for C_{gd}	11/	0	
CGSTCE	C'_{gso}	Linear temperature coefficient for C_{gso}	11/ 0		
KF	K_f	Flicker noise coefficient		0	
AF	A_f	Flicker noise exponent		1	

Table 4.1: TOM-2 model parameters

defined with reference to equation 4.1 as follows,

$$p = \frac{1}{1 + \delta V_{ds} I_{dso}} = 1 - \delta V_{ds} I_{dso}. \tag{4.27}$$

g_m and g_{ds} are expressd as,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = g_{mo} p^2, \tag{4.28}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = g_{dso} p^2 - \delta I_{ds}^2. \tag{4.29}$$

Differentiating equation 4.1 with respect to V_{gs} and V_{ds}, we obtain

$$g_{mo} = \frac{\partial I_{dso}}{\partial V_{gs}} = \frac{I_{dso}}{V_g} \frac{Q}{\left(\exp - \left(\frac{V_{gs} - V_{to} + \gamma V_{ds}}{Q V_{st}}\right) + 1\right)}, \tag{4.30}$$

and

$$g_{dso} = \frac{\partial I_{dso}}{\partial V_{ds}} = g_m \left(\gamma - N_d \frac{V_{gs} - V_{to} + \gamma V_{ds}}{N_g + N_d V_{ds}}\right) + \frac{Q N_d I_{dso}}{N_g + N_d V_{ds}} + \frac{\alpha \beta V_g^Q}{\left(1 + (\alpha V_{ds})^2\right)^{3/2}}. \tag{4.31}$$

Finally, for the gate diode

$$g_{gs} = \frac{\partial I_{gs}}{\partial V_{gs}} = \frac{q I_s}{nkT} e^{qV_{gs}/nkT}, \tag{4.32}$$

$$g_{gd} = \frac{\partial I_{gd}}{\partial V_{gs}} = \frac{q I_s}{nkT} e^{q(V_{gs} - V_{ds})/nkT}. \tag{4.33}$$

4.2 Load Pull

It is possible to measure contours of load impedances on the Smith chart that would result in a constant output power. Such a measurement is termed "load pull" measurement. In its simplest form, a load pull test setup consists of the Device Under Test (DUT) with some form of calibrated tuning device on its output.

Let's consider an idealized linear device like an ideal voltage-controlled current generator with zero output impedance and zero knee voltage. It is assumed that the parasitics and package effects are also negligible. According to the loadline theory discussed in section 1.1.1, the optimum load resistance to allow maximum voltage and current swing at the load terminals would be

$$R_{opt} = \frac{2V_{dc}}{I_{max}}. \tag{4.34}$$

In this optimal condition, the power delivered to the load will be

$$P_{opt} = V_{dc}I_{max}/4. \tag{4.35}$$

Now, the objective is to find the load impedance contours in order to achieve a certain output power of, say, P_{opt}/k. From Figure 4.2, it can be seen that two resistive terminations of R_{opt}/k and kR_{opt} can deliver the power of P_{opt}/k. It can also be shown that the P_{opt}/k point can be extended into a continuous curve if

some series reactance is added to the load resistance. The key point is that while the current swing remains at its maximum level it is possible to increase the voltage swing, without affecting the output power. The series reactance has a maximum value of $\pm X_M$, whose value is such that the series combination of X_M and R_{opt}/k gives a complex magnitude of R_{opt}.

$$R_L = R_{LO} = R_{opt}/k, \tag{4.36}$$

$$P_{RF} = I_{max}^2 R_L/8; \qquad -X_M \leq X_s \leq X_M;$$
$$P_{RF} = P_{opt}/k; \qquad -X_M \leq X_s \leq X_M;$$

where

$$\left(R_{LO}^2 + X_M^2\right)^{1/2} = R_{opt}. \tag{4.37}$$

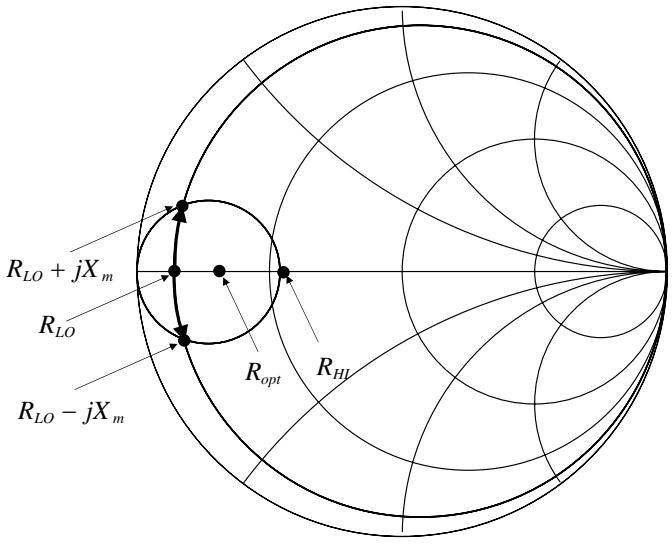


Figure 4.2: Constant power contour for the load impedances with resistive part lower than R_{opt}

Likewise, as shown in Figure 4.3, the kR_{opt} can be extended into a continuous curve if some shunt suceptance B_M is added to the load conductance. The maximum limit for B_M is that the complex admittance magnitude of the load is equal to $1/R_{opt}$.

$$R_{HI} = kR_{opt} = R_L, \tag{4.38}$$

$$P_{RF} = \frac{V_{DC}^2}{2R_L}; \qquad -B_M \leq B_p \leq B_M;$$

$$P_{RF} = P_{opt}/k; \qquad -B_M \leq B_p \leq B_M;$$

where

$$\left(1/R_{HI}^2 + B_M^2\right)^{1/2} = 1/R_{opt}. \tag{4.39}$$

It is trivial to show that the contour is closed and the limiting points of constant

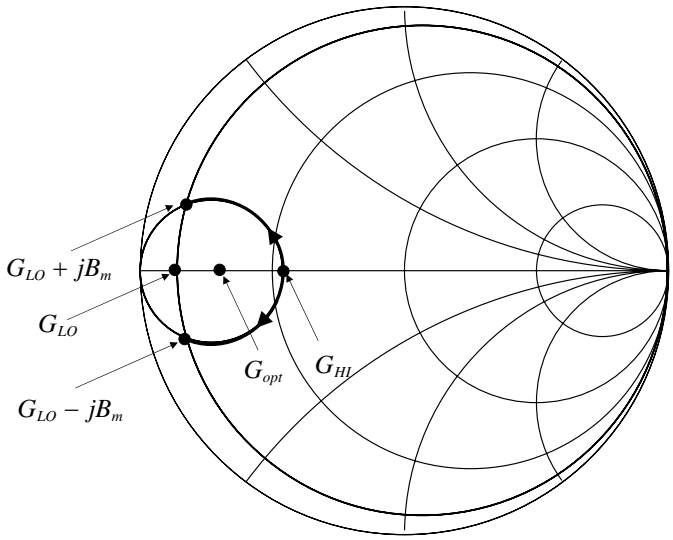


Figure 4.3: Constant power contour for the load impedances with resistive part higher than R_{opt}

power, coincide at the apex of the intersection of separate arcs. The final result

for $k = 2$ is shown in Figure 4.4. It can be seen that the constant power contours are non-circular. The contours apply at any frequency which is only true if the reference plane is at the current generator. In practice, since there are parasitics between the measurement reference plane and the current generator, contours will rotate.

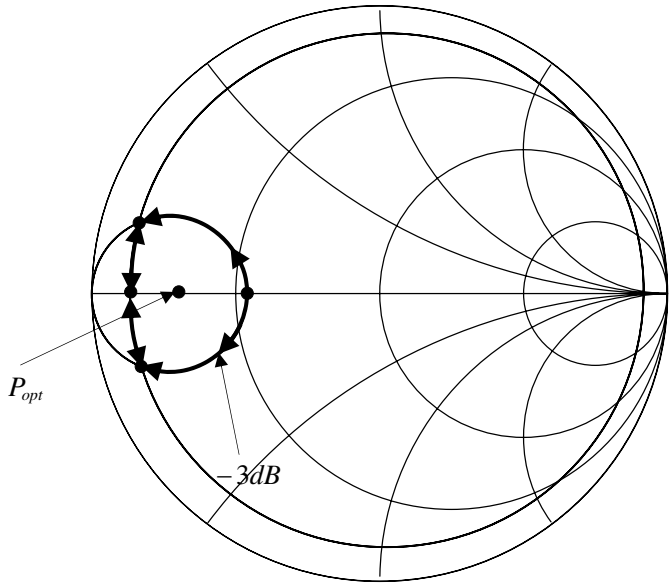


Figure 4.4: Theoretical load pull contour for $k = 2$

4.3 Analysis of Varactor-based Adaptive Impedance Transformers

In this section, several single-diode and multi-diode varactor-based circuits are investigated in terms of linearity, tuning range, and chances of forward-bias. An

adaptive varactor-based impedance transformer is then proposed and examined subsequently.

4.3.1 Linearity of Varactor-based Adaptive Circuits

In order to predict the effect of the varactor diode characteristics on linearity and impedance transformation, proper modeling of varactor diodes is required. The capacitance of a varactor diode is generally modeled as [38]

$$C(V) = \frac{K}{(\phi + V)^n}, \tag{4.40}$$

where $C = dQ/dV$ is the incremental diode capacitance, ϕ is the built-in potential, K is a constant, V is the total voltage and n is the power law exponent. If V_{dc} is the bias voltage and v is the ac voltage, then knowing that

$$V = V_{DC} + v, \tag{4.41}$$

equation 4.40 can be expanded as

$$C(v) = C_0 + C_1 v + C_2 v^2 + \ldots, \tag{4.42}$$

where

$$C_0 = \frac{K}{(\phi + V_{dc})^n}, \tag{4.43}$$

$$C_1 = -C_0 \frac{n}{(\phi + V_{dc})}, \tag{4.44}$$

$$C_2 = C_0 \frac{n\,(n+1)}{(\phi + V_{dc})^2}. \tag{4.45}$$

C_1 in equation 4.44 gives rise to second-order distortion while C_2 in 4.45 gives rise to third-order distortion [39].

4.3.1.1 Shunt Varactor Circuits

Figure 4.5 shows a varactor used in a shunt resonator. The resonant frequency of the resonator can be modified by changing the bias voltage of the varactor. Third-order harmonic distortion (IM3), as derived in [38], is

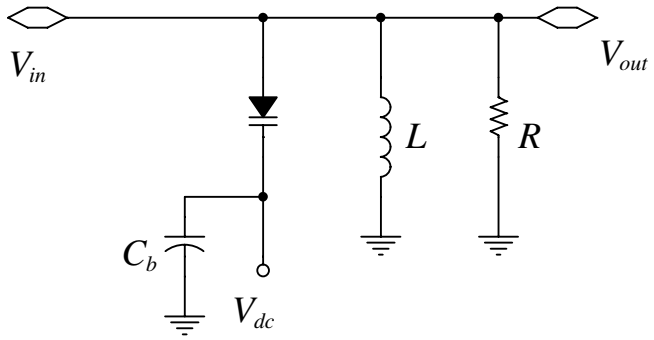


Figure 4.5: Varactor diode in shunt configuration

$$IM_3 = \frac{3}{4}\omega_0 R \frac{C_2}{3} V_{in}^2 \left(1 - \frac{2n}{1.5\,(n+1)}\right), \tag{4.46}$$

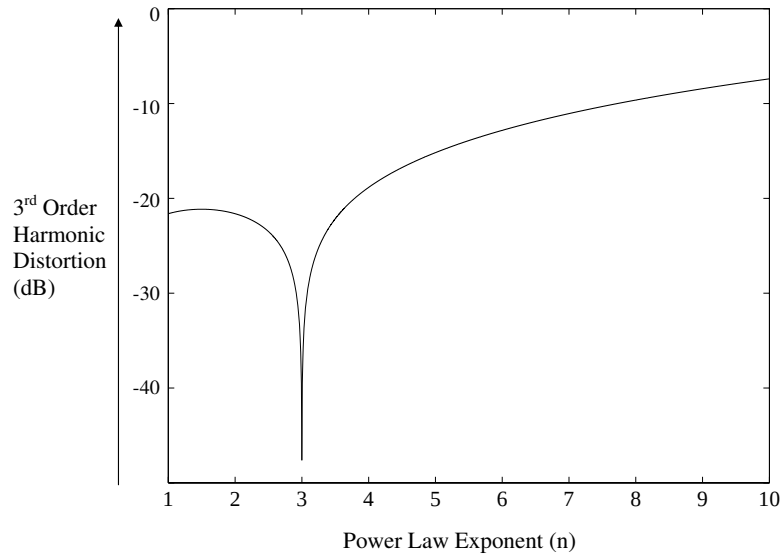


Figure 4.6: IM3 plot of a shunt varactor diode versus power law exponent(n)

where ω_0 is resonance frequency and C_2 is defined as per 4.45. Figure 4.6 shows the plot of IM3 distortion for the resonator with shunt varactor with typical parameter values versus the power law exponent n. Although for $n = 3$, IM3 seems to be eliminated, the practicality of realizing it is not certain. The reason is that the null at $n = 3$ is very sharp that means small fabrication errors in realizing the exponent factor will lead to large IM3 distortions. Besides, for RF signals with high peak-to-peak voltage, the diode will be forward biased leading to severe distortion.

4.3.1.2 Series Varactor Circuits

Figure 4.7 shows a series resonator with a varactor employed as the variable capacitance. A series varactor suffers from the same problems as the shunt varactor. It displays identical IM3 distortion as the shunt varactor (derived in [38]) and high

voltage RF signals can forward bias the varactor and cause severe distortion.

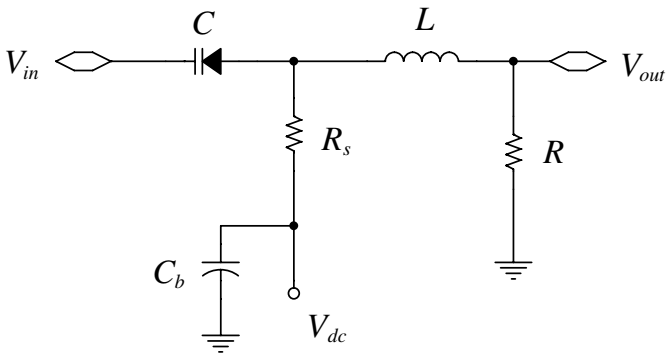


Figure 4.7: Series Varactor Resonator

4.3.2 Multi-diode configurations

Multi-diode schemes have been suggested to reduce distortion and chance of forward bias. Two common schemes are anti-parallel and anti-series configurations.

4.3.2.1 Anti-parallel configuration

Figure 4.8 shows the anti-parallel diode connection. With the same approach used in previous sections each diode can be represented as a power series of the incremental applied voltage as follows

$$C_1(v) = M_0 + M_1 v + M_2 v^2 + \ldots, \tag{4.47}$$

$$C_2(v) = N_0 - N_1 v + N_2 v^2 + \ldots. \tag{4.48}$$

The total capacitance is

$$C_T(v) = (M_0 + N_0) + (M_1 - N_1)v + (M_2 + N_2)v^2 + \dots. \tag{4.49}$$

For identical diodes

$$C_T(v) = 2M_0 + 2M_2v^2 + \dots \tag{4.50}$$

It is obvious from equation 4.50 that IM2 distortion in anti-parallel connection is theoretically zero [38] but the problem is that IM3 distortion is significant. It is even higher than a single diode configuration which makes it unsuitable for adaptive circuits. It also does not provide any improvement for the chance of forward bias compared to single diode shunt configuration.

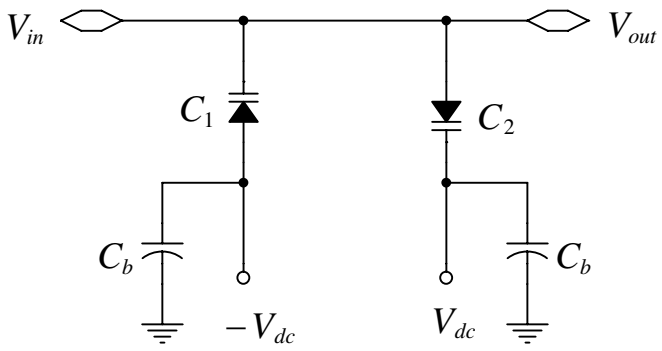


Figure 4.8: Anti-parallel Configuration

4.3.2.2 Anti-series configuration

Figure 4.9 shows the anti-series or common cathode connection. Distortion free

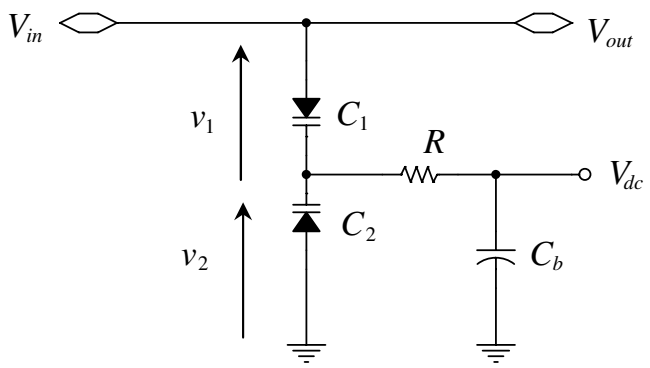


Figure 4.9: Anti-series Configuration

performance can be achieved using this configuration [38]. For the anti-series configuration, shown in Figure 4.9, the incremental voltage is shared between two diodes. If v is the total incremental voltage then in a similar fashion to equation 4.42, the capacitance of each diode can be represented by a power series as a functional of the incremental applied voltage.

$$C_1(v_1) = M_0 + M_1 v_1 + M_2 v_1^2 + \ldots \tag{4.51}$$

$$C_2(v_2) = N_0 - N_1 v_2 + N_2 v_2^2 + \ldots \tag{4.52}$$

where

$$v = v_1 + v_2. \tag{4.53}$$

It is shown in [38] that the total capacitance of the composite anti-series (common cathode) connection is

$$C(v) = \frac{1}{Y_0} - \frac{2Y_1}{Y_0^3}v + \frac{3}{Y_0^5}\left(2Y_1^2 - Y_0Y_2\right)v^2 + \ldots \tag{4.54}$$

where

$$Y_0 = \frac{1}{M_0} + \frac{1}{N_0} \tag{4.55}$$

$$Y_1 = -\frac{M_1}{2M_0^3} + \frac{N_1}{2N_0^3} \tag{4.56}$$

$$Y_2 = \frac{M_1^2/2 - M_0M_2/3}{M_0^5} + \frac{N_1^2/2 - N_0N_2/3}{N_0^5}. \tag{4.57}$$

For matched diodes,

$$C(v) = \frac{M_0}{2} + \frac{M_2}{8}\left[1 - \frac{1.5M_1^2}{M_0M_2}\right]v^2 + \ldots. \tag{4.58}$$

From equation 4.58, it can be seen that the constant term is halved and the linear term disappears. The v^2 term , which is responsible for third-order distortion, can be eliminated with the following condition

$$\frac{1.5M_1^2}{M_0M_2} = 1. \tag{4.59}$$

Using equations 4.43, 4.44 and 4.45 , the condition of equation 4.59 is equivalent to

$$n = \frac{1}{2}. \tag{4.60}$$

Figure 4.10 shows the performance of an anti-series configuration for typical parameters.

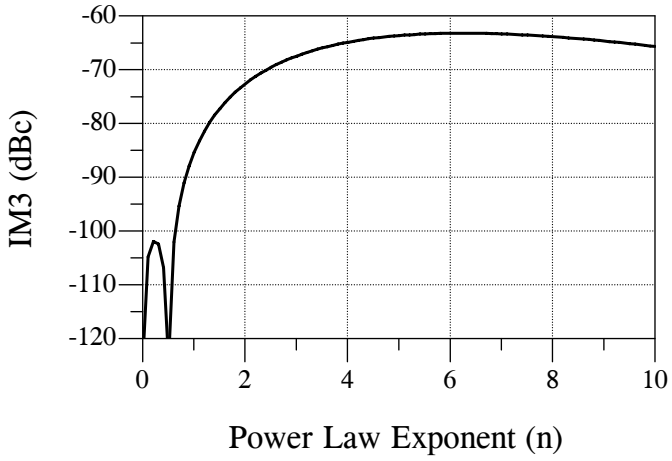


Figure 4.10: IM3 plot of two varactor diodes in anti-series connection for typical parameters versus power law exponent(n)

Fortunately, it is rather easy to realize variable capacitors with exponents close to 0.5 and achieve extremely low second- and third-order distortion. High impedance tapping for the control voltage makes the effect of forward biasing of the diodes minimum on the distortion [39]. This topology appears to be the best among the explained configurations.

4.3.3 The proposed topology for adaptive load modulation

Based on the investigated basic varactor diode connections and knowing that anti-series configuration is the most viable configuration because of its potential high linearity and its capabilities to prevent severe distortion, should forward-bias happen. The configuration shown in Figure 4.11 is proposed for adaptive impedance transformation. It can be implemented in a very small area since the varactors can easily be fabricated within standard semiconductor processes. It has also been shown in Chapter 3 that this arrangement can perform wideband load modulation. The $\lambda/4$-impedance inverter employed after the carrier amplifier in conventional

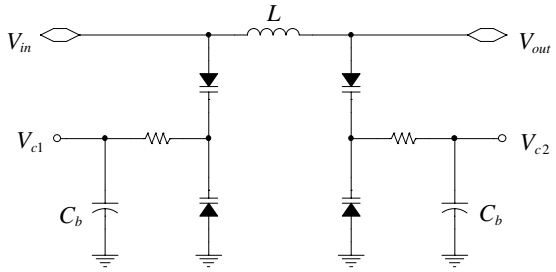


Figure 4.11: The single-stage proposed adaptive impedance transformer

Doherty amplifiers will be replaced with this circuit. A similar arrangement is placed before the peak amplifier for phase compensation in the peak amplifier path. This will result in a new configuration for Doherty amplifiers which is shown in Figure 4.12. The circuit is simulated in the next chapter. The design has also been fabricated with discrete elements. Measured results have also been presented.

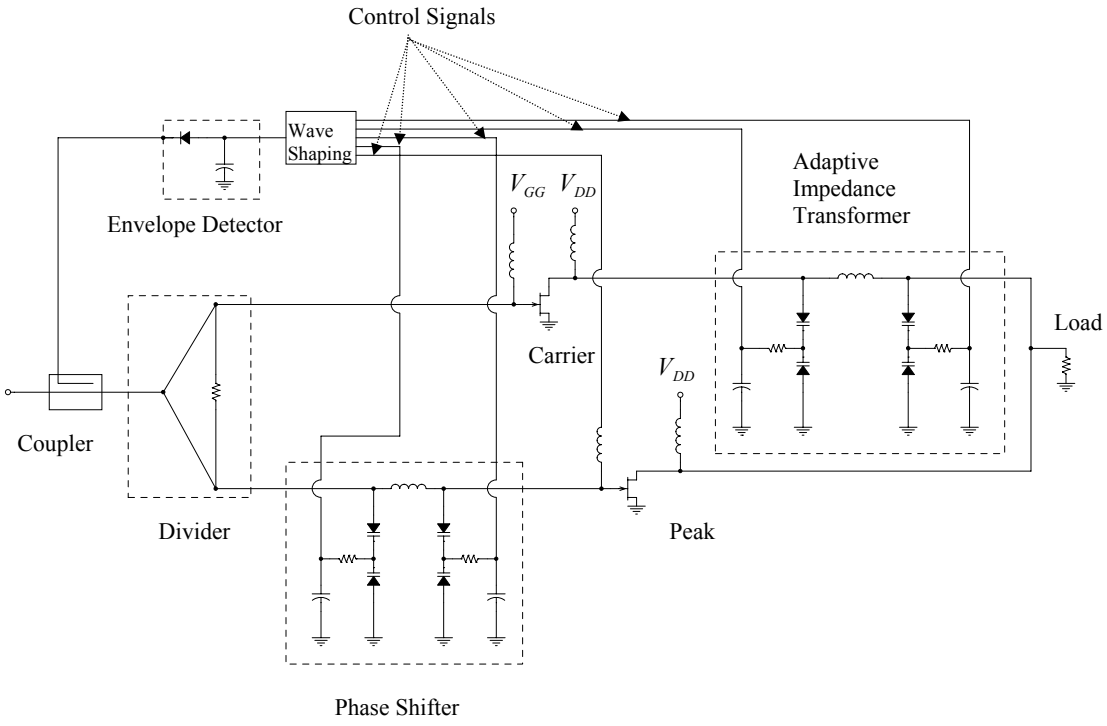


Figure 4.12: Deployment of the proposed impedance transformation scheme in a Doherty power amplifier

Chapter 5

Simulation and Measurements

In this chapter, we will try to verify the theoretical results derived in the previous chapter, through simulation and measurement. The design has been realized using Transcom's GaAs pHEMT transistor at 2 GHz. Details of the transistor specifications can be found in Appendix A. DC IV-curves have been simulated and measured in order to verify the model on one hand and find the optimum bias point for the design on the other hand. A load pull/source pull simulation and measurement have also been carried out to determine the optimum source/load impedances for maximum output power. In order for a comparative analysis, a class AB amplifier, a conventional Doherty amplifier and the proposed novel Doherty amplifier have been designed using the same transistor. Simulation results have been verified by measurements on fabricated modules. The final design objective for the proposed Doherty power amplifier is summarized in Table 5.1.

Specifications	Value
Operating Frequency	1.8GHz-2.2GHz
Maximum Output Power	33dBm
Power Gain	$\geq$ 14dB
PAE (within 6-dB backoff)	$\geq$ 40%
Third Order Harmonic Distortion (IM3)	$\leq$ -40dBc (100kHz tone-spacing)
Supply Voltage	8V

Table 5.1: Design Objectives for the proposed Doherty amplifier

5.1 Design and Simulation of a class AB Power Amplifier

Since the carrier amplifier of the final Doherty amplifier design is operated in class AB, a separate class AB power amplifier is designed and realized to determine the required design parameters for the final design. The class AB amplifier's simulated and measured results will also be compared with the final design.

5.1.1 DC IV-Curves Simulation and Measurement

In order to verify the transistor model and to determine the bias points of the transistor, a DC IV-curve analysis has been carried out. Measurements have been performed with MT4463 system from NMDG company. A photograph of this system is shown in Figure 5.1. Simulated and measured IV-curves are depicted in Figure 5.2. Good agreement between simulated and measured results can be observed.

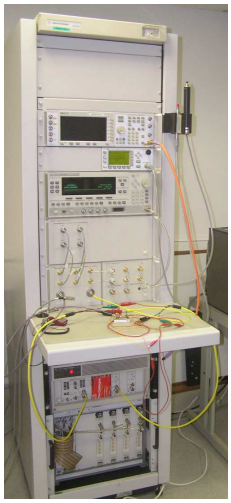


Figure 5.1: MT4463 system

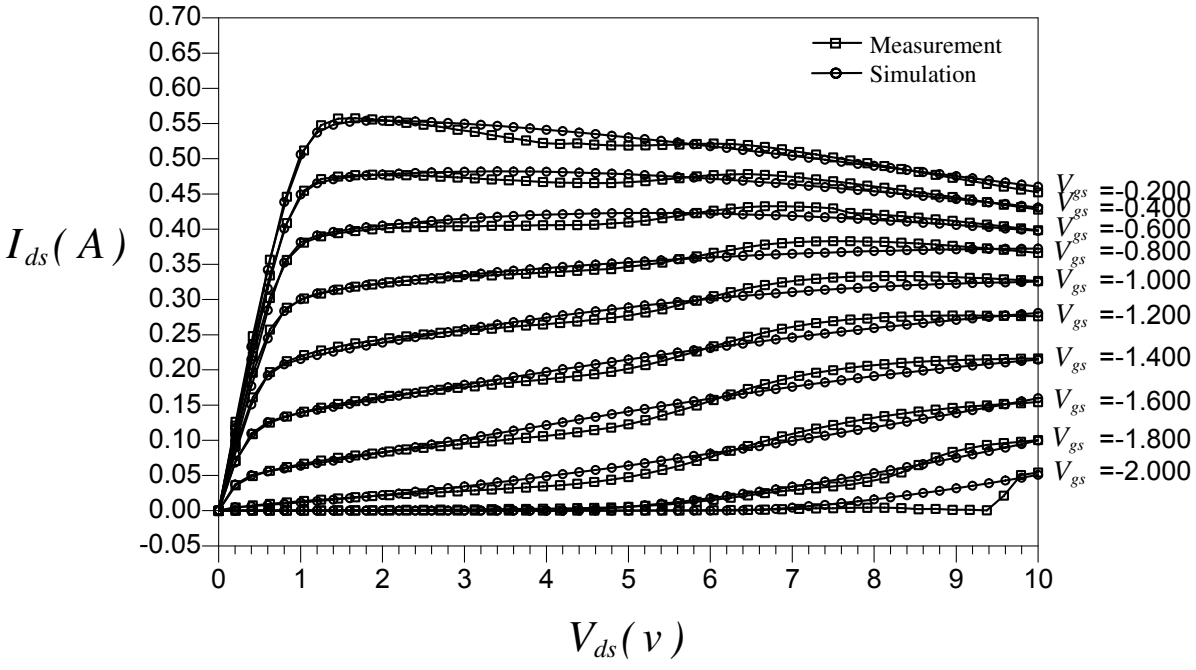


Figure 5.2: DC I-V curve simulation and measurement

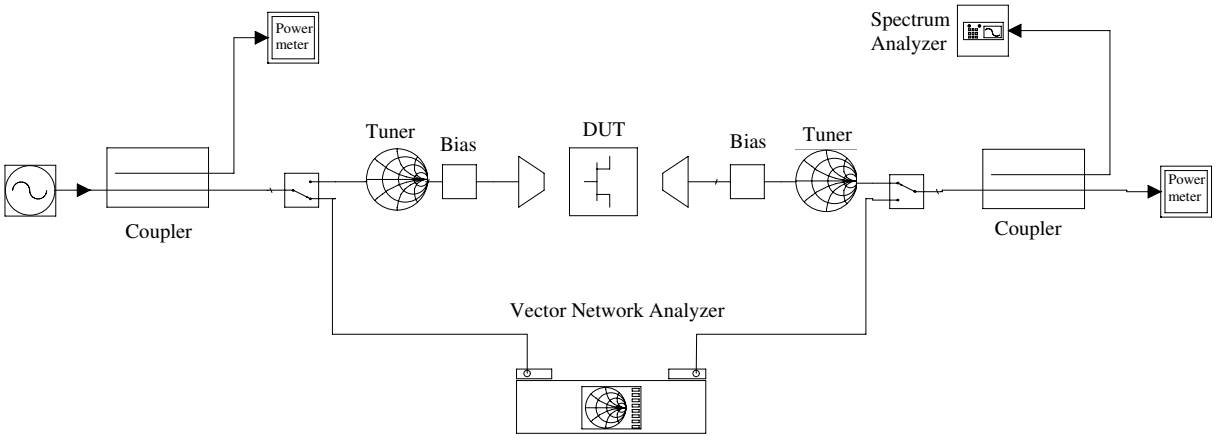


Figure 5.3: Block diagram of load pull setup

5.1.2 Load Pull Setup

A typical load pull setup is made up of two impedance tuners placed at the input and output of the DUT, a (Vector Network Analyzer) VNA for calibration purposes and power sensors. The load and source impedances seen by the DUT are swept through different impedances while power and efficiency are being measured. Constant power contours are then plotted using a computerized network. A block diagram of a load pull setup is shown in Figure 5.3.

5.1.3 Load Pull Simulation and Measurement

Figure 5.4 shows a picture of the load pull/source pull test bench from 'Focus Microwave', which has been utilized for our measurements. Figure 5.5 compares simulated and measured load pull results at 2GHz. Measured load pull results at 1.8GHz and 2.2GHz are also presented in Figure 5.6. It is important to note that

Figure 5.4: Load pull and source pull setup

the effect of connectors and Bias-Tees have been de-embedded.

Simulated and measured source pull results are shown in Figure 5.7. Based on the optimum source and load impedances found, input and output matching circuits can be designed.

5.1.4 Input and Output Matching Network Design

5.1.4.1 Input Matching Network

Since the active component is a nonlinear device, it is expected that the input impedance is a power-dependent parameter. This is due to nonlinearities associated to the gate-source capacitance. Therefore, it is very important to analyze the

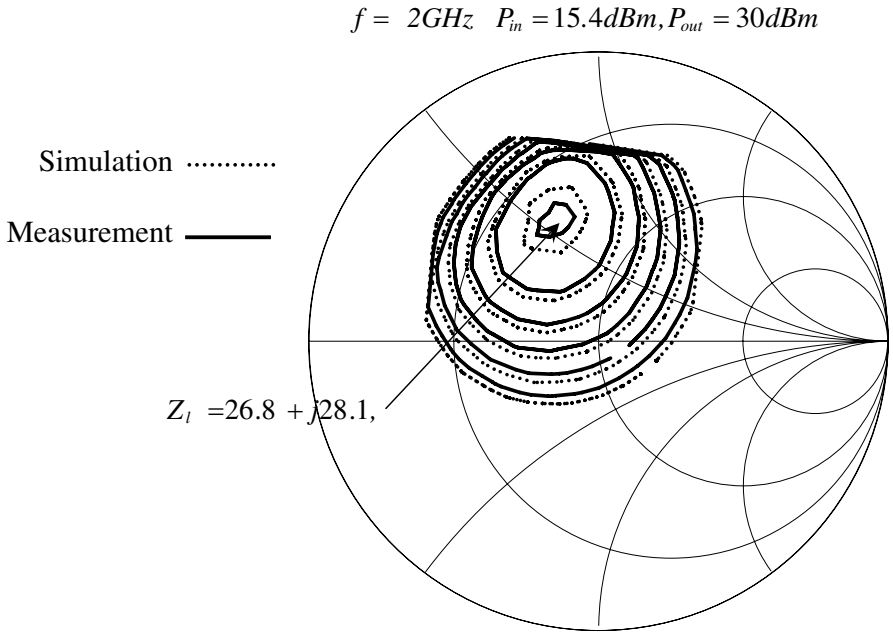
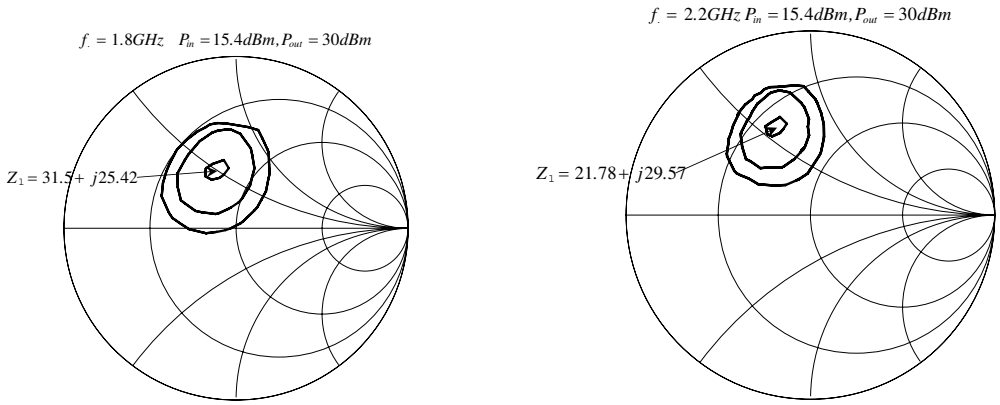


Figure 5.5: Simulated and measured load pull contours with 0.5 dB steps for maximum output power in class AB mode of operation



(a) (b)

Figure 5.6: Measured load pull data at 1.8GHz and 2.2GHz

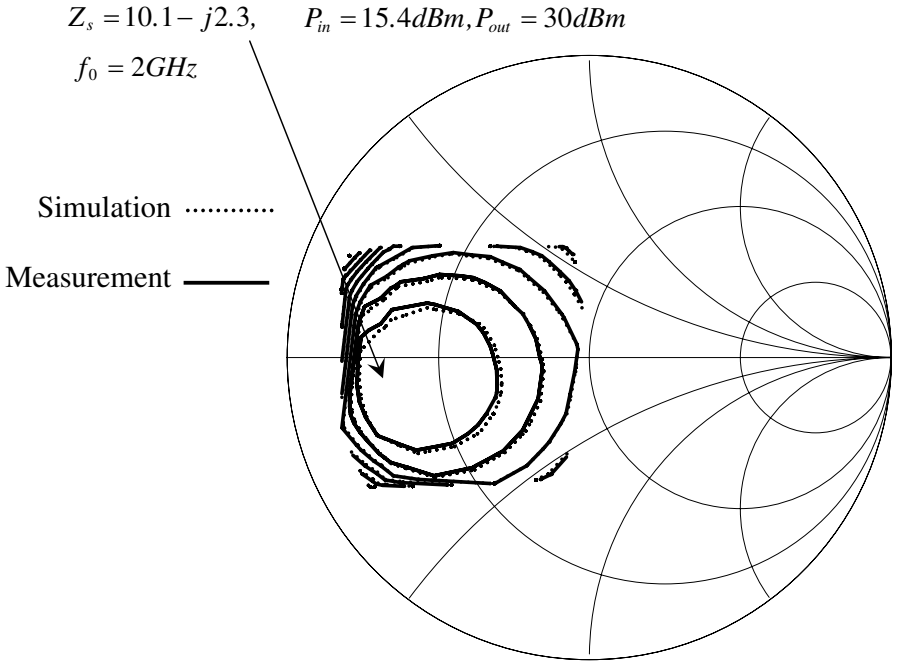


Figure 5.7: Simulated and measured source pull contours with 0.5 dB steps for maximum output power in class AB mode of operation

variations of the input return loss with the input power level, before designing the input matching network based on the optimum source impedance. Figure 5.8 shows the measured input impedance versus input power. Fortunately, the input impedance of the transistor does not change significantly in this case. Figure 5.9 shows the schematic diagram of the input matching network designed based on the source pull measured data and the variation of the input impedance with input power.

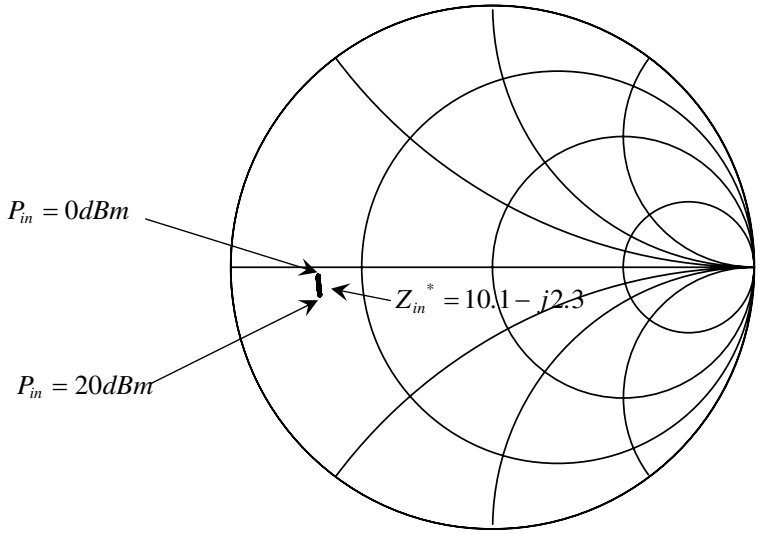


Figure 5.8: Variation of the transistors input impedance with input power level

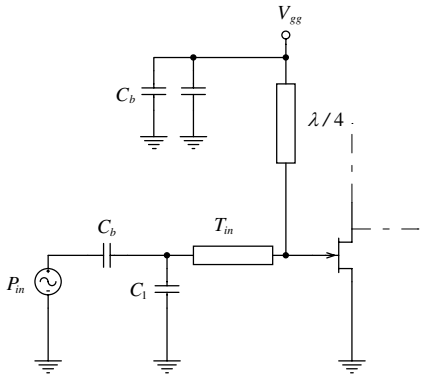


Figure 5.9: Input matching network for class AB design

5.1.4.2 Output Matching Network

An output matching network based on the measured load pull data has been designed as shown in Figure 5.10.

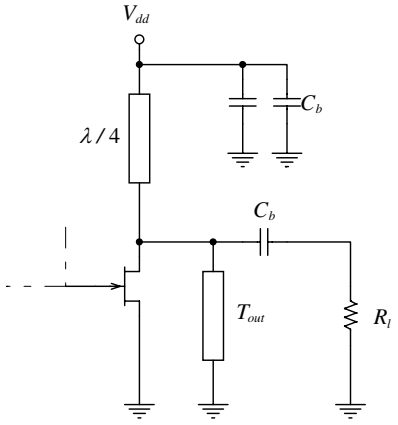


Figure 5.10: Output matching network for class AB design

5.2 Performance of the Class AB Power Amplifier

The schematic diagram of the designed class AB power amplifier is shown in Figure 5.11. It has been biased for $V_{GSQ} = -1.4(V)$, $I_{DSQ} = 200(mA)$ and $V_{DD} = 8(V)$. Table 5.2 lists the components used in the design.

Figure 5.12 compares the simulated and measured output power versus input power at 2GHz. Simulated and measured gain versus input power is shown in Figure 5.13. Maximum output power of 30dBm with a gain of 14.6dB has been

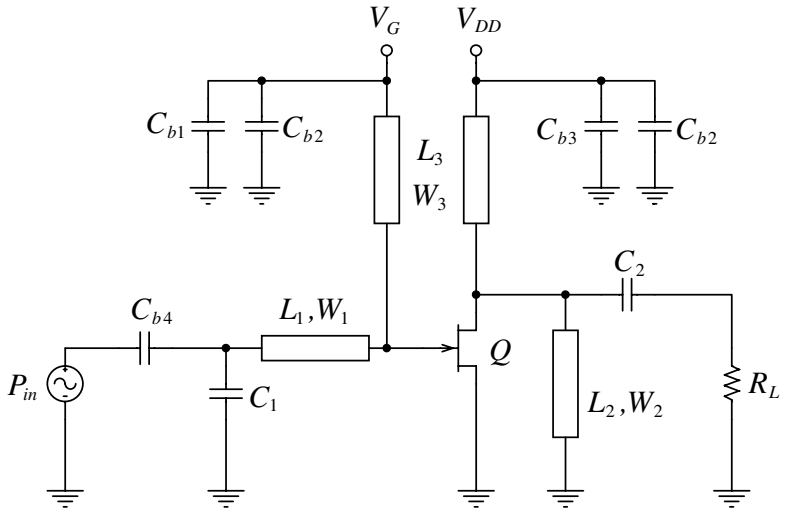


Figure 5.11: Schematic diagram of the class AB design

Component	Value	Component	Value
C_1	3.0pF	L_1	142mil
C_2	1.5pF	L_2	370mil
C_{b1}	15pF	L_3	726mil
C_{b2}	1nF	W_1	31mil
C_{b3}	100pF	W_2	72mil
C_{b4}	20pF	W_3	31mil
PCB	Rogers $\epsilon_r = 6.15$,H=50mil	Q	Transcom TC2571

Table 5.2: The class AB design components

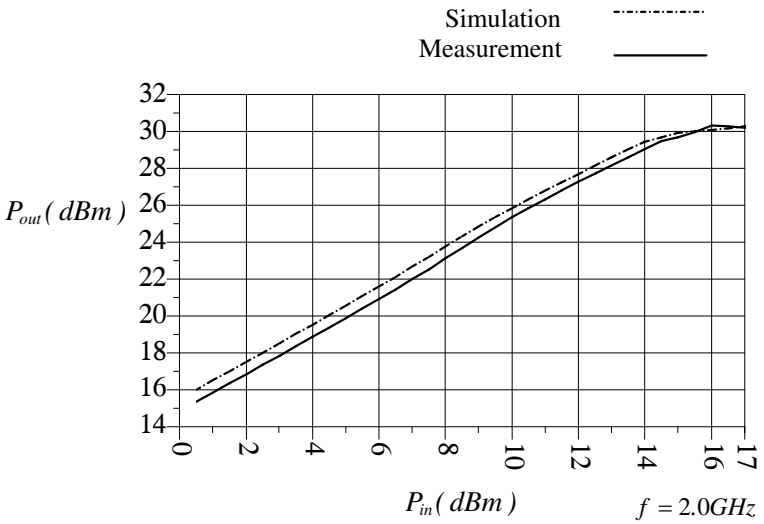


Figure 5.12: Simulated and measured output power of the class AB power amplifier design

achieved. The gain of the class AB power amplifier has been measured at 1.8GHz and 2.2GHz as well to evaluate its performance over a wide bandwidth. As seen in Figure 5.14, the gain drops at 1.8GHz and 2.2GHz. Figure 5.15 shows the measured input return loss of the power amplifier. Good matching is observed.

Power Added Efficiency of the class AB power amplifier versus input power at 2GHz is illustrated in Figure 5.16. Agreement between simulated and measured results is impressive. Power added efficiency of 49% has been achieved at 30dBm output power for 2GHz.

Power added efficiency of the design is compared at different frequencies in Figure 5.17. As expected, efficiency at 1.8GHz and 2.2GHz is poor. The linearity of the class AB power amplifier has also been analyzed. The 2-tone response of the

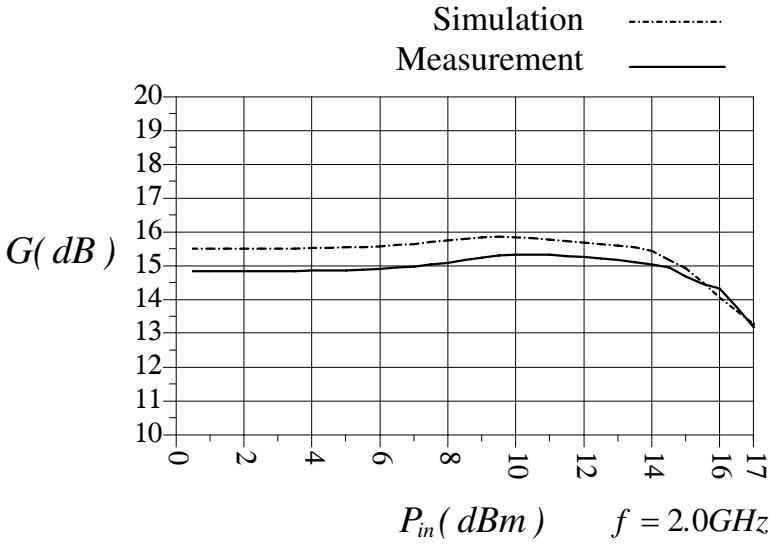


Figure 5.13: Simulated and measured gain of the class AB design

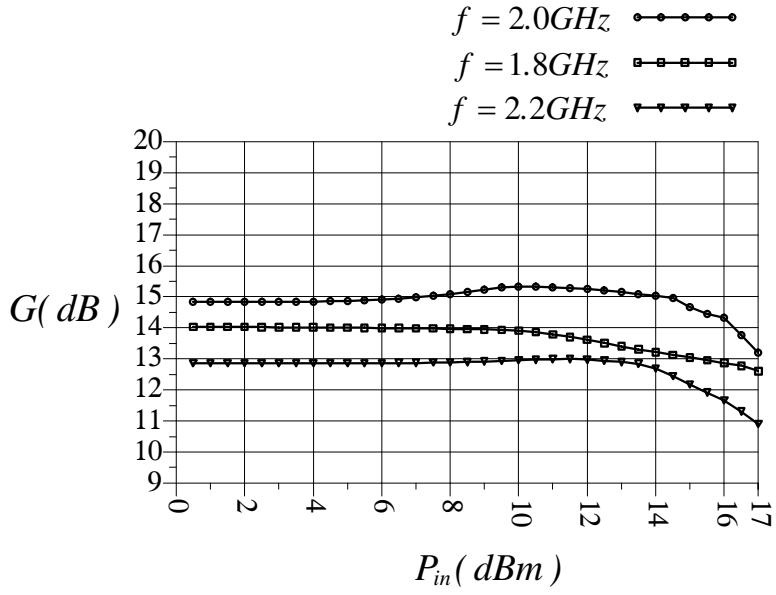


Figure 5.14: Gain performance of the class AB design at different frequencies

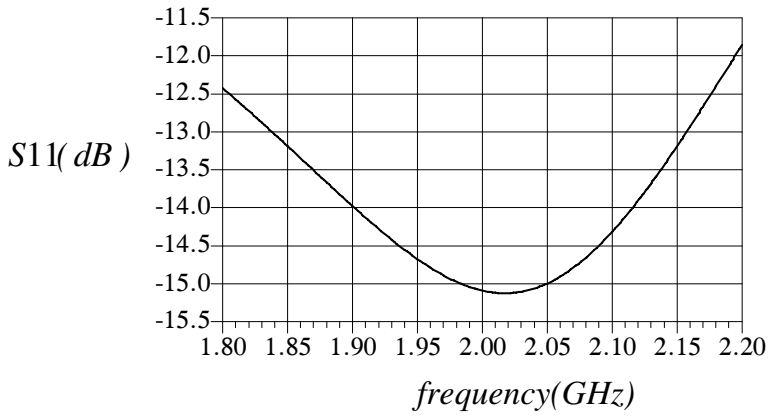


Figure 5.15: Input return loss of the class AB design at maximum power level

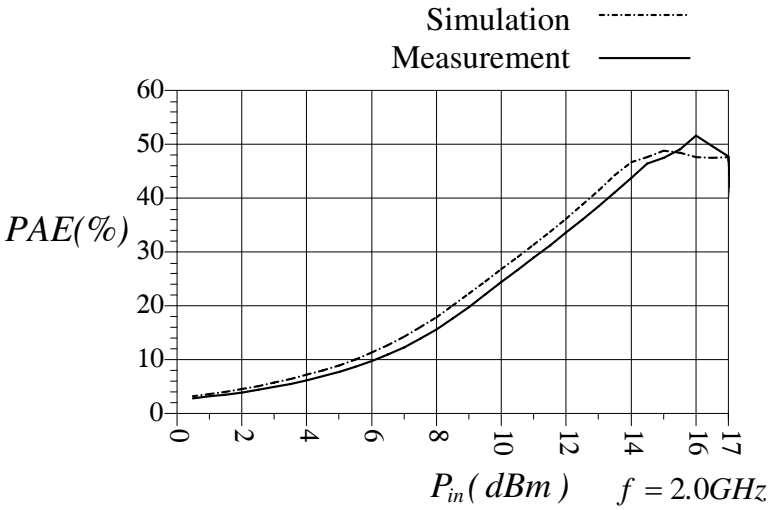


Figure 5.16: Simulated and measured PAE of the class AB amplifier

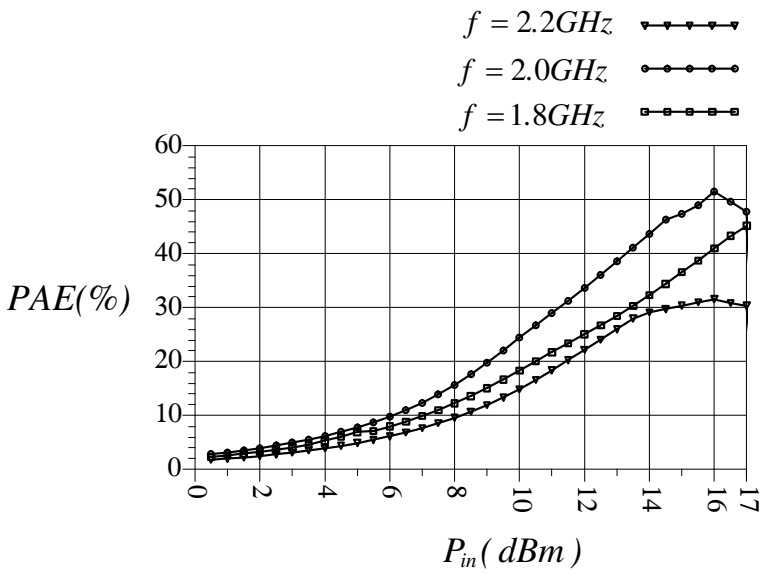


Figure 5.17: Measured PAE of the class AB design at different frequencies

power amplifier with a tone spacing of 100kHz has been simulated and measured. Third order harmonic distortion (IM3) versus input power is depicted in Figure 5.18.

5.3 Design and Simulation of a Conventional Doherty Amplifier

A conventional Doherty power amplifier is designed and realized to facilitate a fair comparison between the conventional arrangement and the novel proposed design. The schematic diagram of the designed conventional Doherty amplifier is shown in Figure 5.19. Identical transistors (Transcom GaAs pHEMT, TC2571) have been

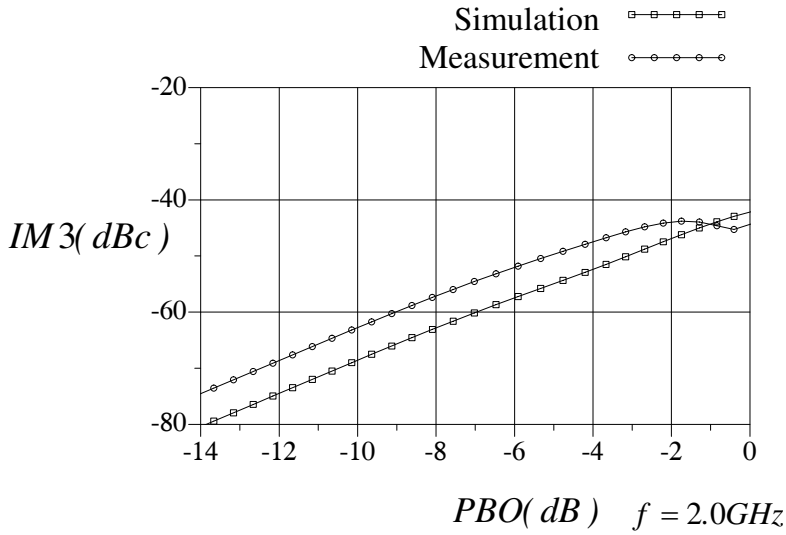


Figure 5.18: Simulated and measured third order distortion of the class AB design used for carrier and peak amplifier. A list of design components is shown in Table 5.3. Bias adaptation as discussed in section 2.2.5 is employed to control the peak

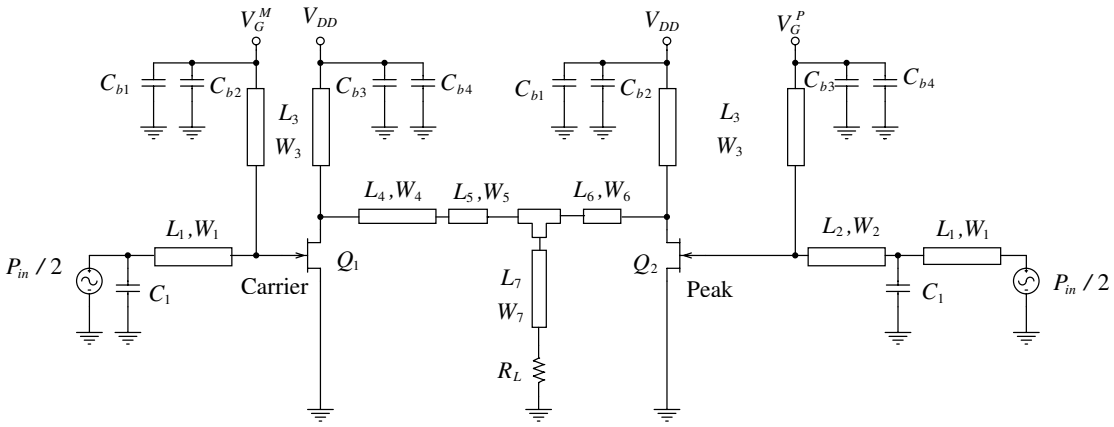


Figure 5.19: Schematic diagram of the designed conventional Doherty amplifier

amplifier's gate bias. The bias adaptation arrangement has been realized using an envelope detector to create the required gate bias according to the input power level. The peak amplifier's gate voltage versus the input power level for optimum

Component	Value	Component	Value
W_1	31mil	L_1	142mil
W_2	72mil	L_2	701mil
W_3	31mil	L_3	726mil
W_4	51mil	L_4	712mil
W_5	72mil	L_5	155 mil
W_6	87mil	L_6	150 mil
W_7	72mil	L_7	160mil
C_{b1}	15pF	C_1	3.0pF
C_{b2}	1nF	C_{b3}	100pF
C_{b4}	1nF	PCB	Rogers $\epsilon_r = 6.15$,H=50mil

Table 5.3: The conventional Doherty amplifier components

performance in terms of efficiency and linearity is shown in Figure 5.20. This profile for the gate voltage must be generated by the wave-shaping circuit to ensure the most effective Doherty operation. Simulation results accompanied by measured

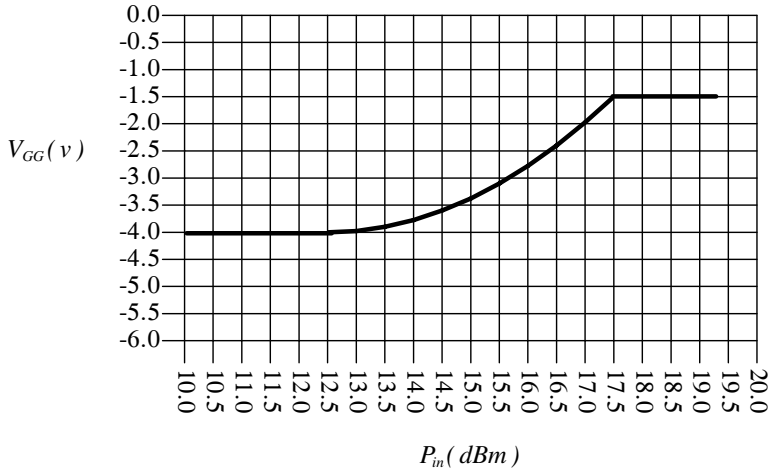


Figure 5.20: Peak amplifier's gate voltage profile versus input power level for optimum Doherty effect

data of the conventional Doherty power amplifier are presented here. The input matching networks of the the carrier and peak amplifier are the same as the ones for the class AB power amplifier explained in section 5.1.4.1 and 5.1.4.2. Figure

5.21 shows output power versus input power. Agreement between simulated and measured results is satisfactory.

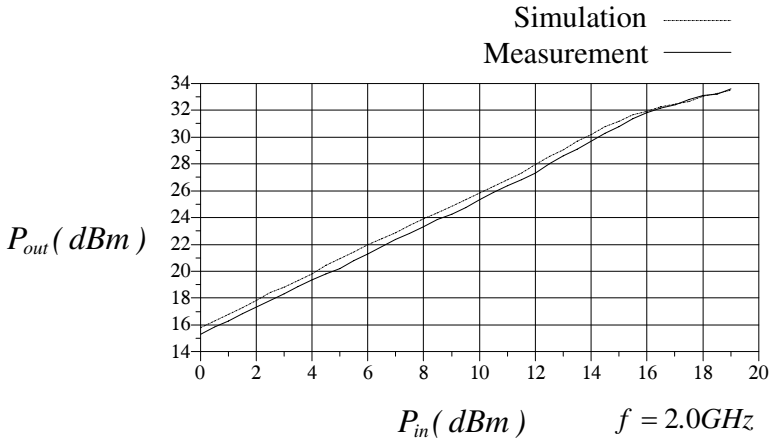


Figure 5.21: Simulated and measured output power of the conventional Doherty amplifier

Figure 5.22 shows gain versus input power of the conventional Doherty power amplifier. Simulated and measured results display good agreement. As discussed earlier, since the $\lambda/4$-impedance inverters work in a narrow bandwidth, it is expected that the performance of the conventional Doherty power amplifier degrades significantly at frequencies away from the design frequency. Figure 5.23 shows measured gain results at 1.8GHz, 2GHz and 2.2GHz.

Figure 5.24 compares measured and simulated PAE versus input power at 2GHz while Figure 5.25 compares measured PAE at 3 frequencies to observe the Doherty amplifier's performance over a wide bandwidth. Again, as suggested by gain results, PAE is heavily degraded at frequencies distant from 2GHz.

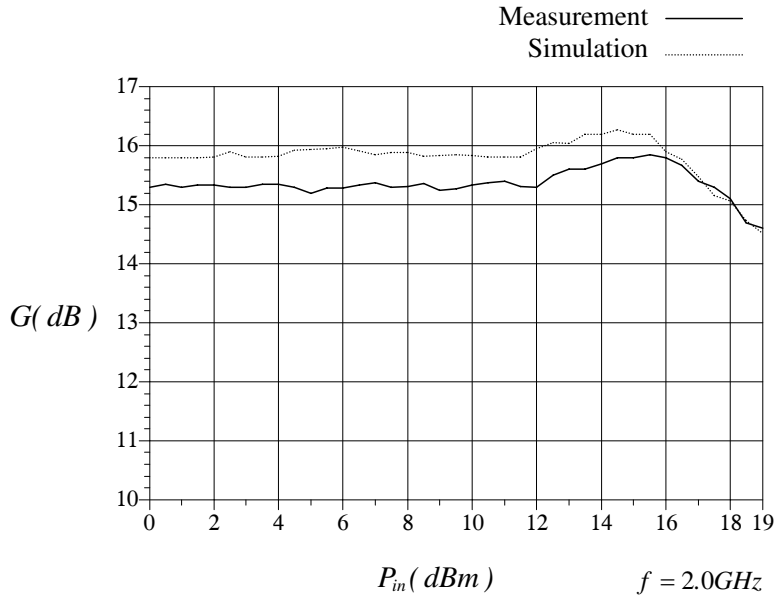


Figure 5.22: Simulated and measured gain of the designed conventional Doherty amplifier

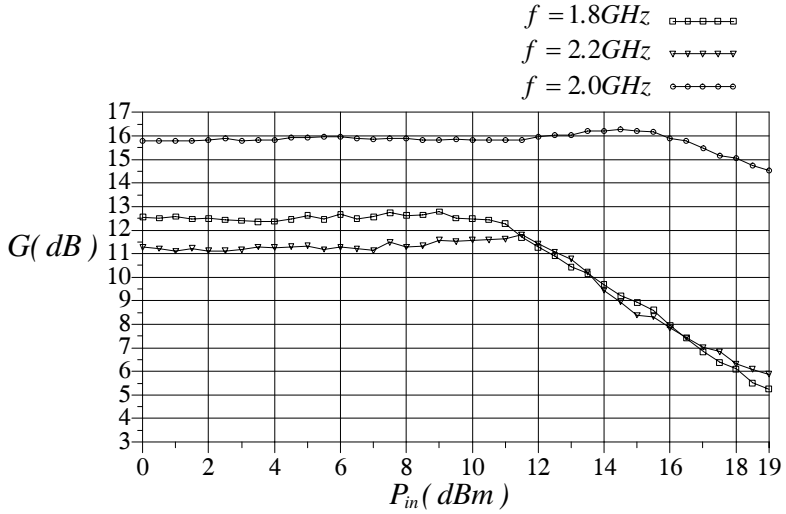


Figure 5.23: Comparison of gain performance of the conventional Doherty amplifier at different frequencies

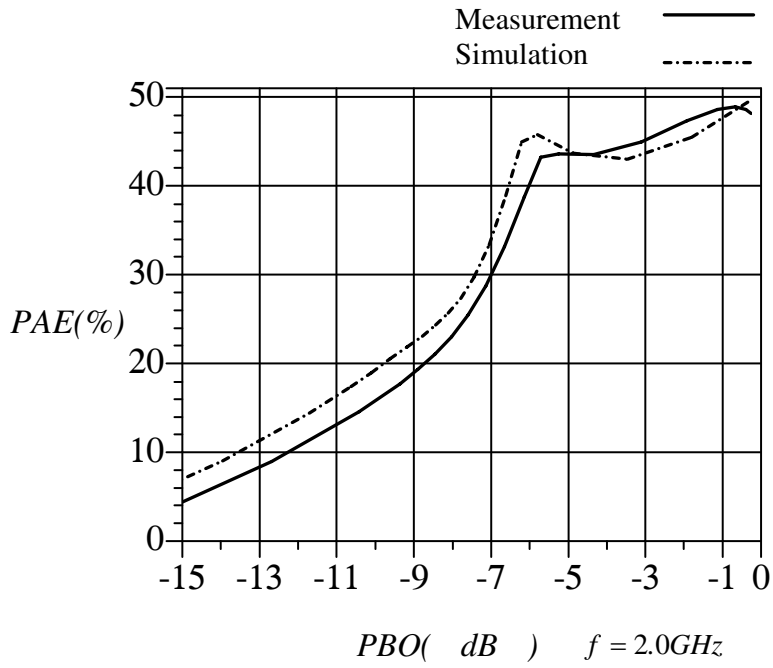


Figure 5.24: Simulated and Measured PAE of the conventional Doherty amplifier

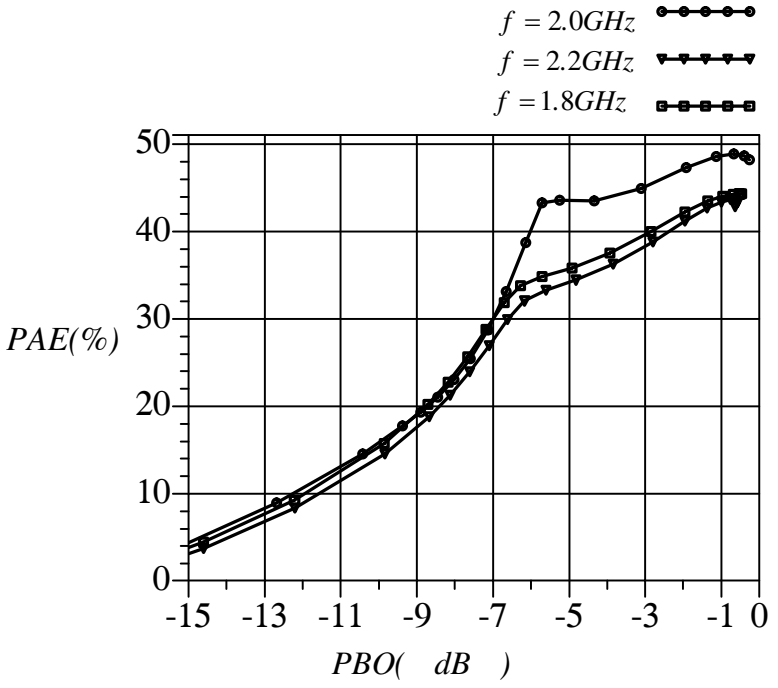


Figure 5.25: PAE of the conventional Doherty amplifier design at several frequencies

Linearity of the design is measured next. Figure 5.26 shows the third order harmonic distortion versus input power at various frequencies.

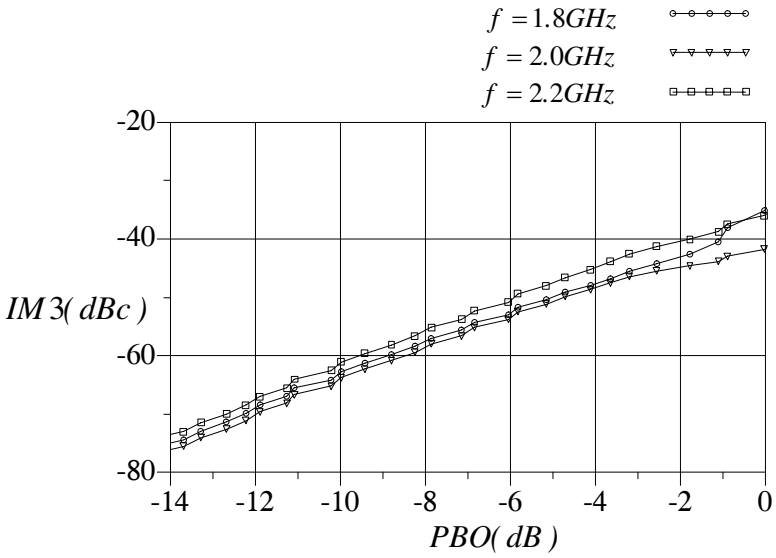
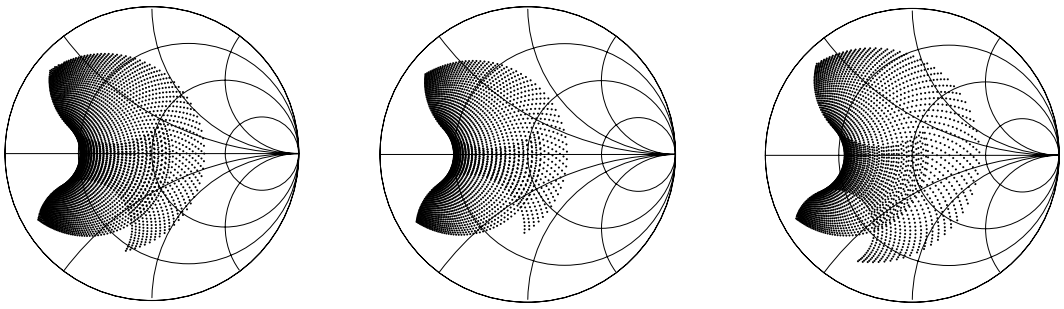


Figure 5.26: Comparison of third order harmonic distortion of the designed conventional Doherty amplifier measured at three frequencies

5.4 Design of the Adaptive Impedance Transformer

Before moving to the design of the proposed novel Doherty amplifier, the proposed adaptive impedance inverter has first been designed and analyzed separately to avoid complexity. This topology was discussed in detail in section 4.3 and its schematic diagram was shown in Figure 4.11. Infineon's BB837 varactors with



(a) 1.8GHz (b) 2.0GHz (c) 2.2GHz

Figure 5.27: Impedance transformation coverage of the varactor-based impedance inverter with swept control voltages

proper power law exponent as explained in section 4.3 have been selected for maximum linearity. Detailed specifications of the varactor diodes can be found in Appendix B. Impedance transformation coverage and linearity of the topology have been investigated and measured data accompanied by simulation results are given. As discussed in detail in section 2.2.1 for the correct Doherty operation, the load impedance seen by the carrier amplifier should be $2R_{opt}$ at low power levels (up to the 6-dB backoff point) and reduce to R_{opt} at maximum output power. Besides, any reactive impedance should be resonated out. In order to evaluate the impedance coverage performance of the proposed adaptive impedance transformer, control voltages are swept through all possible values and the optained impedances are noted. Measured results are shown on a Smith chart in Figure 5.27. Measurements have been carried out in 1.8GHz, 2GHz and 2.2 GHz.

The proposed adaptive impedance transformer will be placed at the output of

the carrier amplifier to modulate the load. A similar arrangement will be placed before the peak amplifier to compensate for the delay caused by the impedance transformer.

5.4.1 Linearity of the Adaptive Impedance Transformer

As discussed in the theoretical analysis (section 4.3), with certain arrangement and selection of the varactor diodes, very low distortions can be achieved. Measured third order harmonic distortion (IM3) versus the input power for a 2-tone signal with 100kHz tone spacing is shown in Figure 5.28.

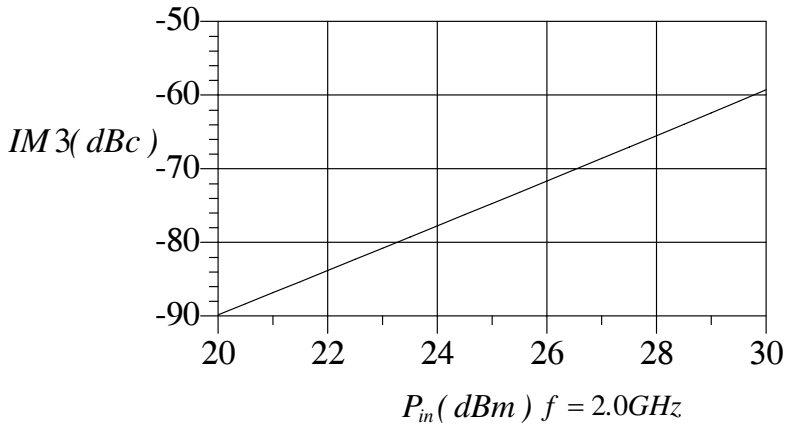
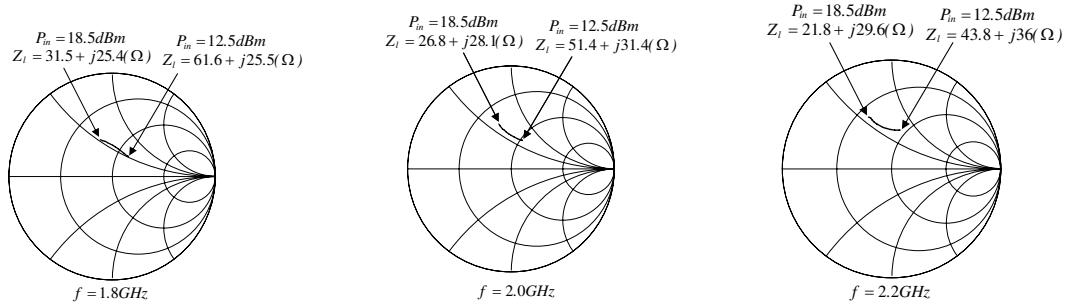


Figure 5.28: Measured third order intermodulation distortion of the varactor-based impedance inverter

5.4.2 Design of the Impedance Transformation Trajectory

According to the load pull measurements presented in section 5.1.3, and the mechanism of load modulation in Doherty amplifiers discussed in section 2.2.1, impedance



(a) (b) (c)

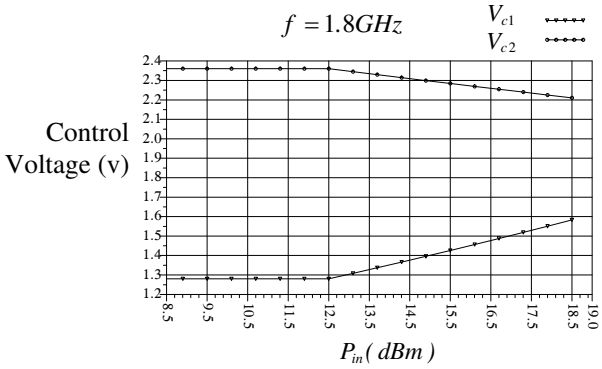
Figure 5.29: Simulated impedance transformation trajectory at the output of the carrier amplifier in three design frequencies

transformations required for Doherty operation are determined for three design frequencies 1.8GHz, 2GHz and 2.2GHz as shown in Figure 5.29.

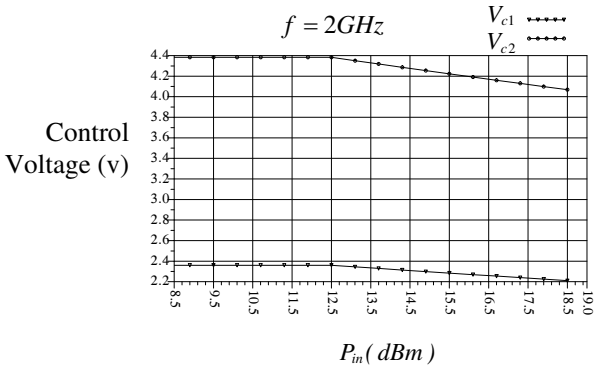
The adaptive bias voltages of the varactors for achieving the mentioned impedance transformation have been determined within the entire power range through simulation and are illustrated in Figure 5.30 at all three different frequencies.

5.4.3 Design of the Phase Compensator

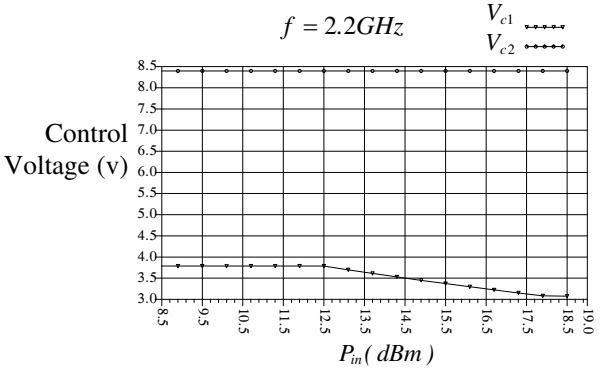
As mentioned earlier, a phase compensation arrangement similar to the adaptive impedance inverter has to be placed before the peak amplifier to compensate for the phase delay introduced in the carrier amplifier so that the output currents of the carrier and peak amplifier combine in-phase. The control voltages required for phase compensation are shown in Figure 5.31. The phase delay introduced by the adaptive impedance inverter and the phase compensator are supposed to be equal.



(a) 1.8GHz

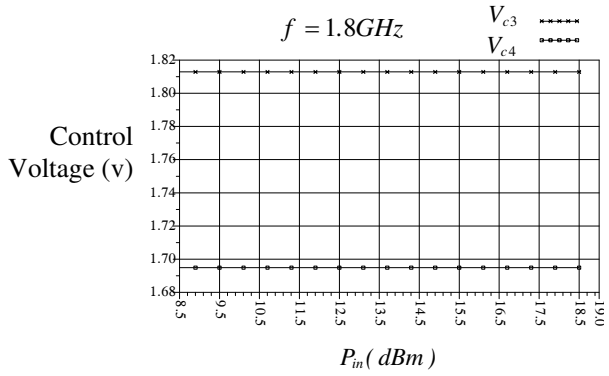


(b) 2.0GHz

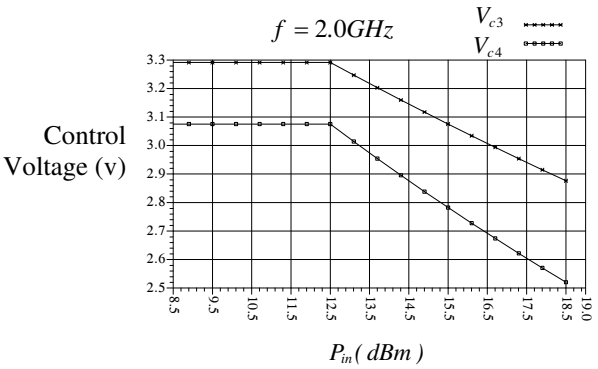


(c) 2.2GHz

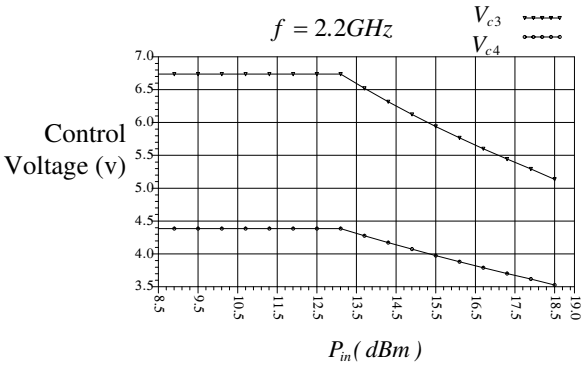
Figure 5.30: Control voltages of the adaptive inverter versus input power



(a) 1.8GHz



(b) 2.0GHz



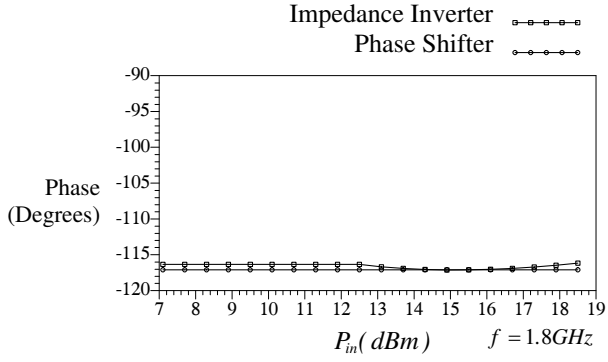
(c) 2.2GHz

Figure 5.31: Control voltages of the phase compensator versus input power

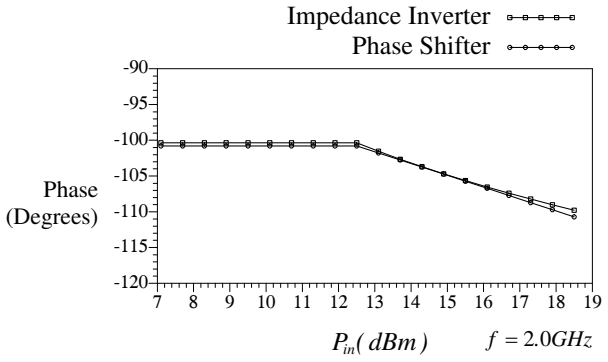
Measured results are compared in Figure 5.32 at three different design frequencies. Negligible differences are observed, suggesting that the phase compensator can successfully compensate for the delay introduced in the carrier path. Since this arrangement is only meant to be a phase compensator with no impedance transformation effect, it has to be matched to 50Ωat both input and output ports within the entire power range. Figure 5.33 shows the measured input return loss of the phase compensator versus input power at three design frequencies. Good matching is observed, which means the phase compensator can produce the correct phase delay while matched to 50Ω over the entire power range.

5.5 Design of the Doherty Amplifier with Adaptive Impedance Transformer

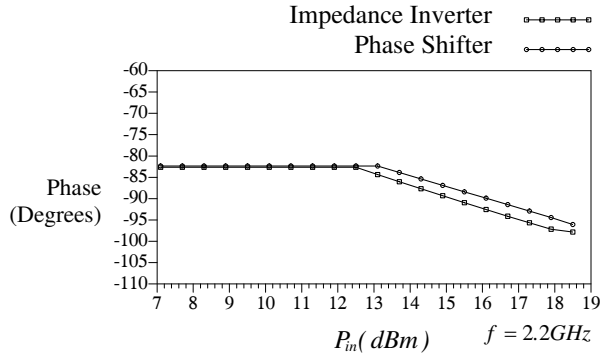
Finally, the complete circuit of the novel Doherty power amplifier with adaptive load modulation can be designed. The $\lambda/4$-impedance inverters of the conventional arrangement are replaced with the adaptive impedance transformer and the adaptive phase compensator. The required control signals and the gate voltage of the peak amplifier (bias adaptation) are generated based on the input power level through an envelope detector. The complete schematic diagram of the design is displayed in Figure 5.34 and the list of components is shown in Table 5.4.



(a) 1.8GHz

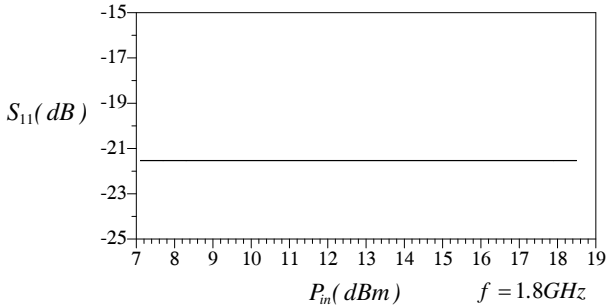


(b) 2.0GHz

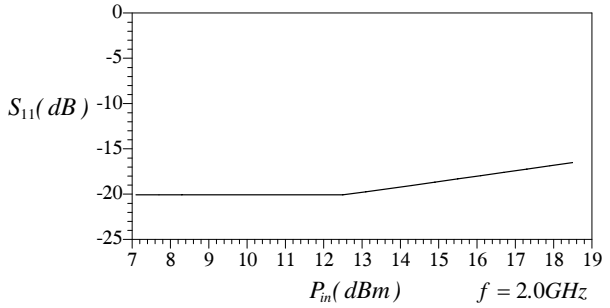


(c) 2.2GHz

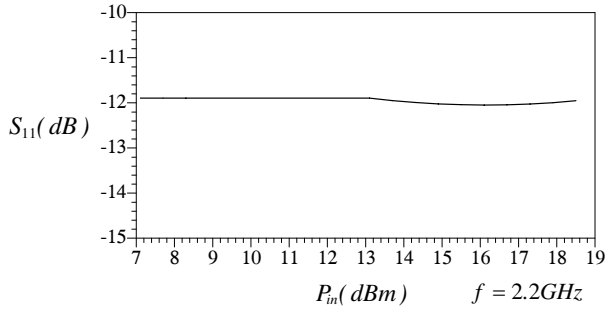
Figure 5.32: Measured phase delay of the adaptive inverter and the phase compensator



(a) 1.8GHz



(b) 2.0GHz



(c) 2.2GHz

Figure 5.33: Matching performance of the phase compensator within the entire input power range

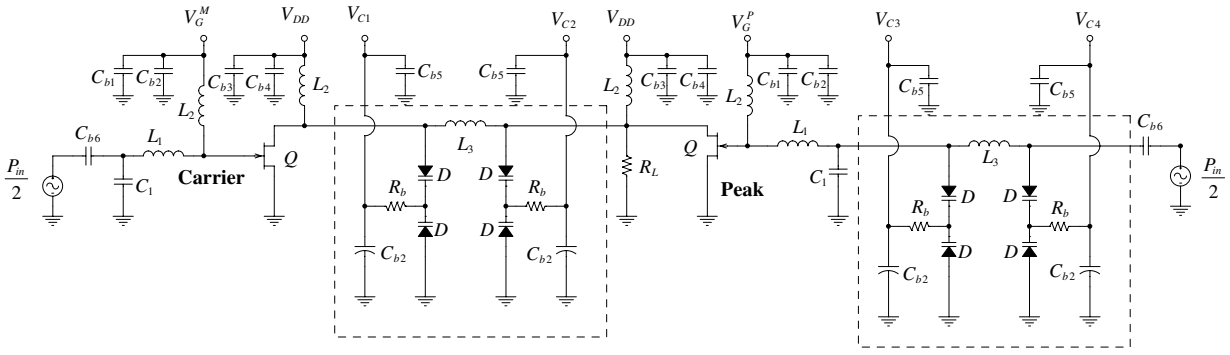


Figure 5.34: Complete design schematic of the proposed Doherty power amplifier

Component	Value	Component	Value
L_1	1.8nH	L_2	18nH
L_3	4nH	C_1	3.3pF
C_{b1}	15pF	C_{b2}	1nF
C_{b3}	100pF	C_{b4}	10nF
C_{b5}	100nF	C_{b6}	20pF
Q	TC2571,Transcom	R_b	10kOhm
PCB	Rogers $\epsilon_r = 6.15$,H=50mil	D	BB837,Infineon

Table 5.4: The proposed Doherty amplifier components

Figure 5.35 shows output power versus input power. Agreement between simulated and measured results is satisfactory. Figure 5.36 shows gain versus input power of the proposed Doherty power amplifier at 2GHz. Simulated and measured results display good agreement. As expected the performance at 2GHz is similar to conventional topology. Now let's look at the gain performance at 1.8GHz and 2.2GHz. This is where we expect improvements compared to conventional approach. Figure 5.37 compares gain at different frequencies. Significant improvement is observed at 1.8GHz and 2.2GHz compared to conventional design. This is due to elimination of narrow band $\lambda/4$-impedance inverters. Figure 5.38 shows PAE versus input power at 2GHz. Both measured and simulated data are given. Power

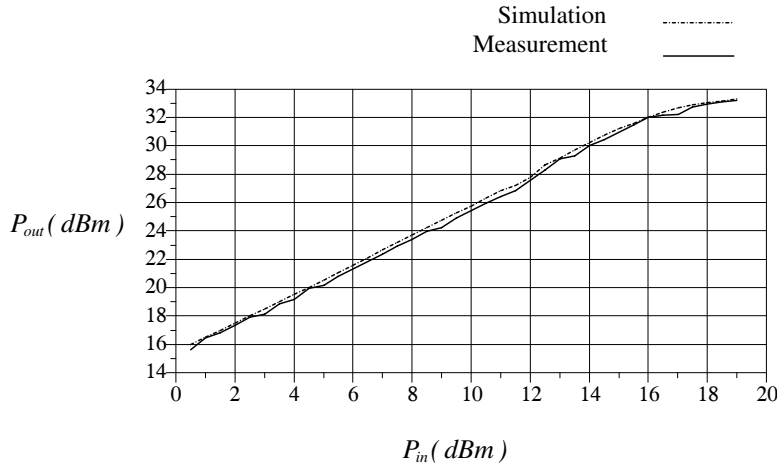


Figure 5.35: Output power of the proposed Doherty amplifier

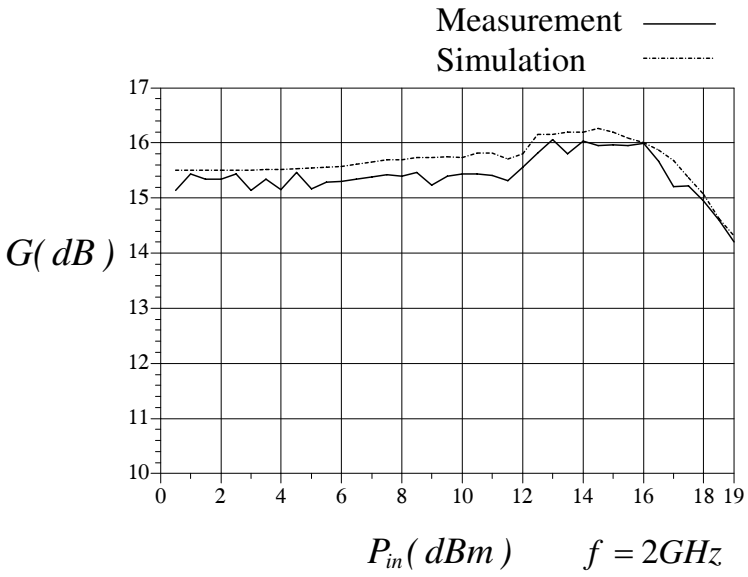


Figure 5.36: Gain of the proposed Doherty amplifier

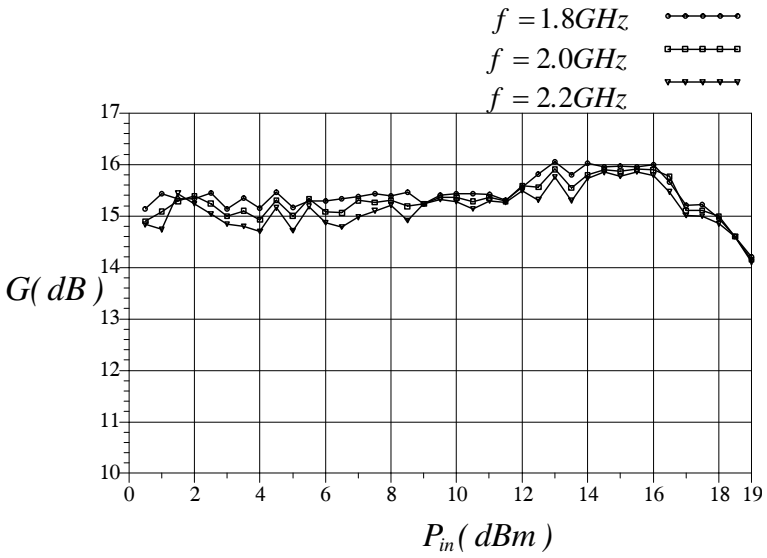


Figure 5.37: Measured gain of the novel Doherty amplifier compared at different frequencies

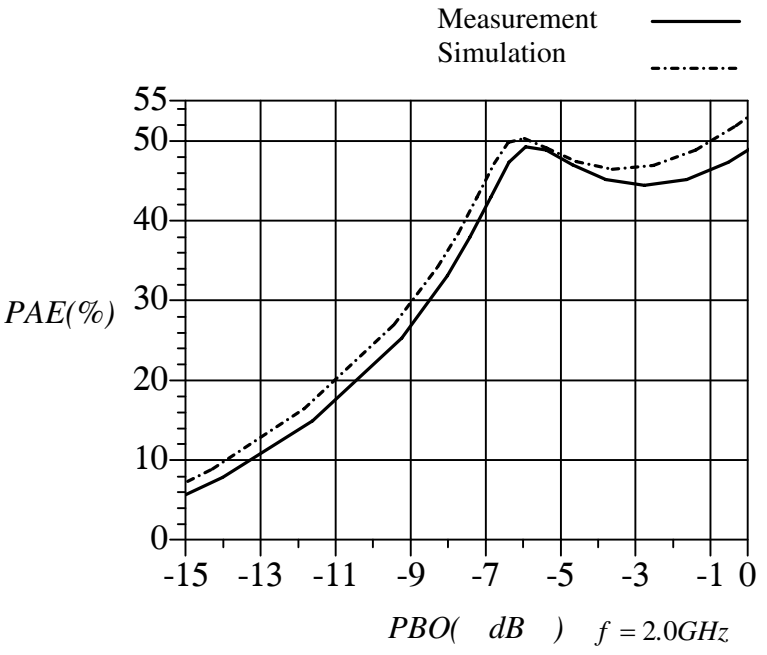


Figure 5.38: Power added Efficiency of the proposed configuration

added efficiency of this design, measured at different stimuli frequencies is shown in Figure 5.39. It is observed that the efficiency performance is not significantly degraded at 1.8GHz and 2.2GHz. Obviously, load modulation can successfully be carried out over an extended frequency range compared to a conventional design. Linearity of the design is analyzed next. Figure 5.40 shows the measured third or-

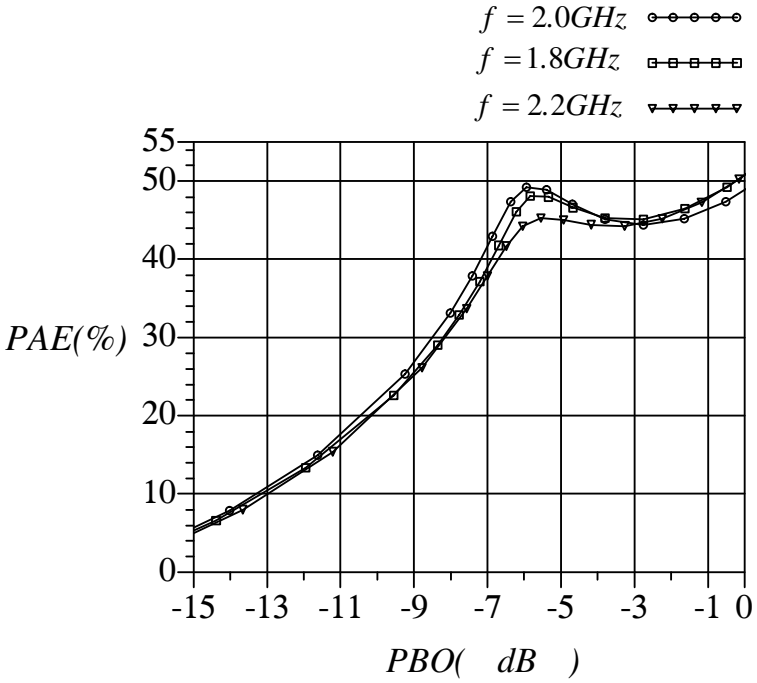


Figure 5.39: Comparison of measured PAE performance of the proposed design at different frequencies

der harmonic distortion versus input power, which verifies that acceptable linearity performance has been achieved.

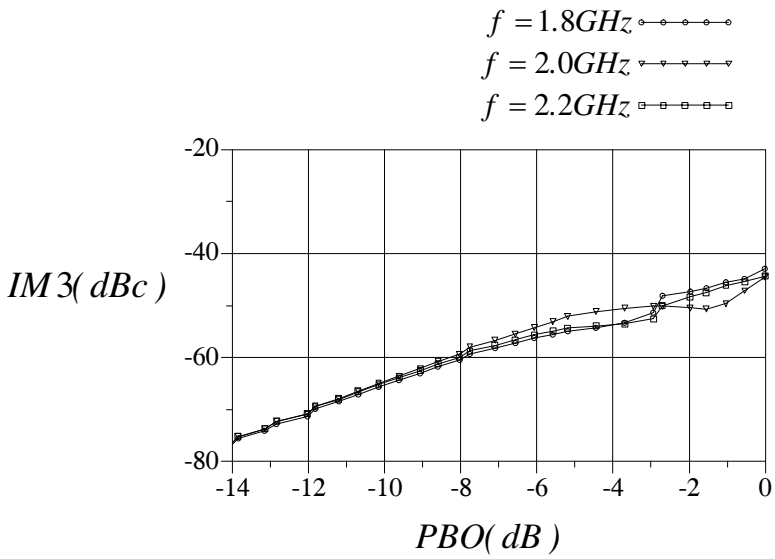


Figure 5.40: Third order harmonic distortion of the novel Doherty amplifier measured at 1.8GHz, 2GHz and 2.2GHz

5.6 Performance Comparison

A comparative investigation among the above three designs is presented in this section to clearly identify the advantages and disadvantages of the proposed approach.

5.6.1 Power Added Efficiency

The efficiency performance of the class AB design, conventional Doherty amplifier and the proposed Doherty amplifier are compared in Figure 5.41 over frequency. The class AB design and conventional Doherty amplifier display poor performance away from the design frequency due to frequency dependent elements employed in the designs. It can be observed that the proposed Doherty amplifier is capable of

maintaining the maximum efficiency as well as efficiency enhancement in backoff region over a larger bandwidth. This is attributed to wide band capabilities of the proposed adaptive impedance inverter which due to the controllability of the varactors can be adjusted to perform a valid load modulation at a wide frequency range.

5.6.2 Linearity

It is expected that the linearity of the class AB design be slightly better than the conventional Doherty amplifier since, as explained earlier, there is always a compromise between efficiency and linearity. It is also expected that since the adaptive impedance inverter has shown very good linearity performance, the proposed Doherty amplifier does not show any significant linearity degradation. Figure 5.42 compares the IM3 distortion of all three different designs.

5.6.3 Size

Figure 5.43 shows the photographs of the realized conventional Doherty amplifier and the proposed Doherty amplifier. The layout dimensions of the designs are clearly outlined. A size reduction of 50% has been achieved due to elimination of passive $\lambda/4$-transmission lines.

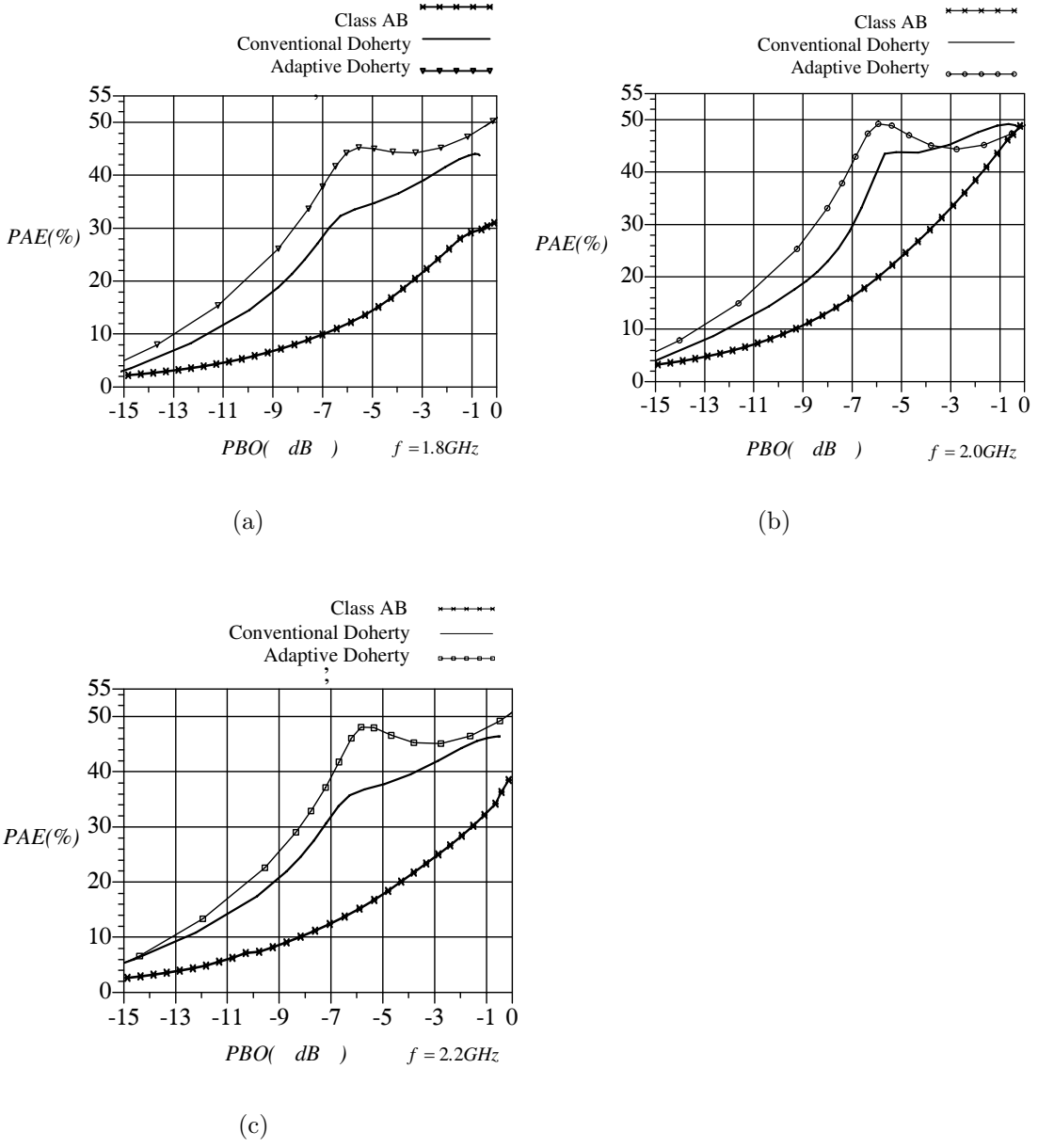


Figure 5.41: Comparison of PAE performance for class AB, conventional Doherty and proposed Doherty amplifiers over the bandwidth

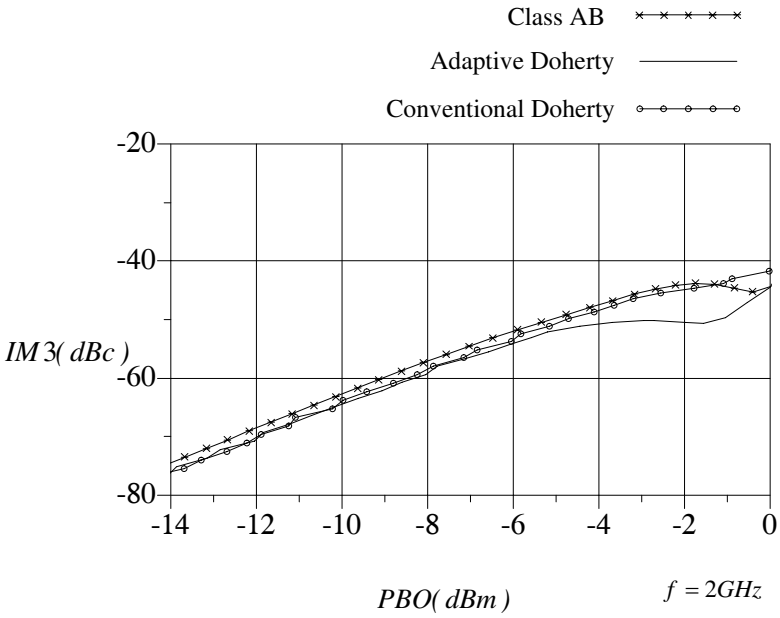
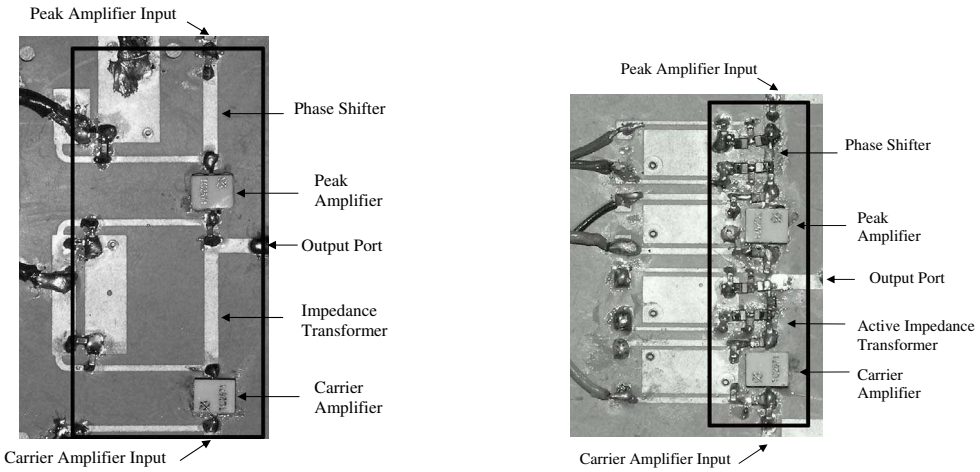


Figure 5.42: Comparison of linearity performance for the class AB, conventional Doherty and proposed Doherty amplifier



(a) 55mm× 24mm (b) 41mm× 15mm

Figure 5.43: Layout Sizes of (a) conventional Doherty amplifier and (b) proposed Doherty amplifier

Chapter 6

Conclusions

In this work, a novel topology for the Doherty amplifier has been proposed to overcome the size and bandwidth issues associated with the conventional Doherty amplifier. The conventional Doherty amplifier employs passive $\lambda/4$-transmission lines for load modulation. This results in a large area and a narrow bandwidth. In this work, load modulation has been carried out by using a highly linear, varactor-based adaptive impedance transformer, which is controlled by an envelope tracking circuit. The superiority of the proposed topology to the conventional approach in terms of size, bandwidth and efficiency, has been verified through simulations and measurements. Simulated and measured results have displayed reasonable agreement. The key research achievements are as follows:

- The proposed Doherty amplifier has achieved a 50% size reduction compared to its conventional counterpart. Since varactors can easily be implemented

in standard semiconductor processes, the proposed topology can facilitate a fully integrated chip solution for the Doherty amplifier.

- The proposed Doherty amplifier has achieved efficiency enhancement within 6-dB backoff range over a wide bandwidth. Power added efficiencies as high as 50.8% at 1.8GHz, 49.5% at 2GHz and 50.2% at 2.2GHz have been achieved at the maximum power(33dBm) and maintained up to the 6-dB backoff point. Power added efficiencies, achieved at 6-dB backoff point, are 48.1% at 1.8GHz, 49.4% at 2GHz and 45.3% at 2.2GHz.

- The proposed Doherty amplifier has displayed reasonable linearity performance. Measured third order harmonic distortion is better than -42.2dBc at 1.8GHz, -44.1dBc at 2GHz and -44dBc at 2.2GHz, for the entire power range from 6-dB backoff point up to 1-dB compression point. This is within the linearity specifications of most wireless communication technologies.

Measured results suggest that the proposed Doherty amplifier is a promising candidate for multi-band/broad-band performance for both hand-held and base-station applications.

Directions For Future Research

Size reduction has been a major objective of this work. Therefore, the entire circuit should be implemented on a single chip. It is a possible research area to investigate the ways to integrate high-Q varactors with the Doherty power amplifier on the same die.

It was discussed in chapter 4, that the varactor-based impedance inverter can be implemented in a multi-stage arrangement in order to further enhance the bandwidth. Therefore, a possible next step is to implement the proposed structure in a multi-stage anti-series varactor-based configuration to explore the ways for further bandwidth improvement.

Realizing a multi-stage Doherty amplifier with multi-stage adaptive impedance inverters, is the ultimate goal of this topic. This will further enhance the bandwidth and power backoff range simultaneously. Figure 6.1 shows a possible block diagram of such an arrangement. The theoretical background for such work is available in this dissertation while further complexities in the design, simulation and fabrication of this circuit, are expected.

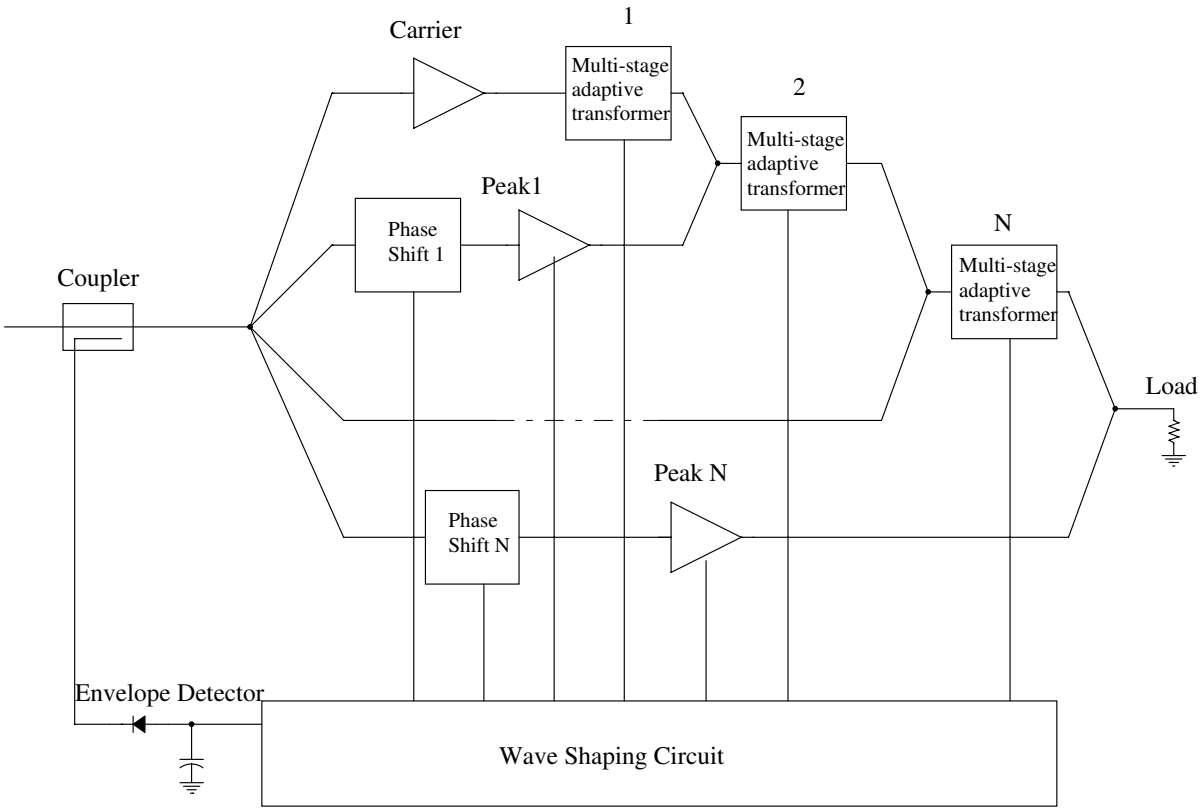


Figure 6.1: Block diagram of a multi-stage Doherty amplifier with multi-stage adaptive impedance transformer

References

[1] J. Kim, S. Bae, J. Jeong, J. Jeon, and Y. Kwon, "A highly-integrated Doherty amplifier for CDMA handset applications using an active phase splitter," *IEEE Microwave and Wireless Component Letters*, vol. 15, pp. 333–335, May 2005.

[2] S. C. Cripps, *'RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[3] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Norwood, MA: Artech House, 2003.

[4] K. Nellis and P. Zampardi, "A comparison of linear handset power amplifiers in different bipolar technologies," *IEEE Journal of Solid-State Circuits*, vol. 39,

pp. 1746–1754, Oct. 2004.

[5] R. Gilmore and L. Besser, *'Practical RF Circuit Design for Modern Wireless Systems.* Norwood, MA: Artech House, 2003.

[6] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," in *Proc. IRE*, vol. 24, pp. 1163–1182, Sep. 1936.

[7] L. R. Kahn, "Single sideband transmission by Envelope Elimination and Restoration," in *Proc. IRE*, vol. 40, pp. 803–806, July 1952.

[8] G. Hanington, P. Chen, P. Asbeck, and L. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for cdma applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, pp. 1471–1476, Aug. 1999.

[9] D. Anderson and W. Cantrell, "High-efficiency high-level modulator for use in dynamic envelope tracking CDMA RF power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1509–1512, June 2001.

[10] S. A. K. Deligoz, J. Desai, M. Figiel, and S. Kiaei, "Monolithic supply modulated RF power amplifier and DC-DC power converter IC," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 89–92, June 2003.

[11] J. Deng, P. Gudem, L. Larson, and P. Asbeck, "A high-average-efficiency SiGe HBT power amplifier for WCDMA handset applications," *IEEE Trans. Microw. Theory Tech.*, vol. 49, pp. 529–537, Feb. 2005.

[12] H. Chireix, "High power outphasing modulation," in *Proc. IRE*, pp. 1370–1392, Nov. 1935.

[13] F.H.Raab, "Efficiency of Doherty RF power-amplifier systems," *IEEE Trans. Broadcast.*, vol. BC-33, pp. 77–83, Sept. 1987.

[14] M. Iwamoto, A. Williams, P. Chen, A. Metzger, L. Larson, and P. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Tech.*, vol. 49, pp. 2472–2479, Dec. 2001.

[15] M. Iwamoto, A. Williams, P.-F. Chen, A. Metzger, L. Larson, and P. Asbeck, "Optimum operation of asymmetrical-cells-based linear Doherty power amplifiersuneven power drive and power matching," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 1802–1809, May. 2005.

[16] D. Yu, Y. woong Kim, K. Han, J. ho Shin, and B. Kim, "Fully integrated Doherty power amplifiers for 5 GHz wireless-LANs," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 177–180, June 2006.

[17] J. Kim, J. Cha, I. Kim, S. Y. Noh, C. S. Park, and B. Kim, "Advanced design methods of Doherty amplifier for wide bandwidth, high efficiency base station power amplifiers," in *Microwave Conference, 2005 European*, vol. 2, Oct. 2005.

[18] Y. Yang, J. Yi, Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of microwave doherty amplifier using a new load matching technique," *Microwave Journal*, vol. 44, pp. 20–36, Dec. 2001.

[19] Y. Yang, J. Cha, B. Shin, and B. Kim, "A microwave Doherty amplifier employing envelope tracking technique for high efficiency and linearity," *IEEE Microwave and Wireless Component Letters*, vol. 13, pp. 370–372, Sept. 2003.

[20] B. S. Jeonghyeon Cha, Youngoo Yang* and B. Kim, "An adaptive bias controlled power amplifier with a load-modulated combining scheme for high efficiency and linearity," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 1, pp. 81–84, June 2003.

[21] J. Lees, M. Goss, J. Benedikt, and P. Tasker, "Single-tone optimisation of an adaptive-bias Doherty structure," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, pp. 2213–2216, June 2003.

[22] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 852–860, March 2005.

[23] J. Jung, U. Kim, J. Jeon, J. Kim, K. Kang, and Y. Kwon, "A new series-type Doherty amplifier for miniaturization," in *IEEE Radio Frequency Integrated*

Circuits (RFIC) Symposium, pp. 259–262, June 2005.

[24] C. Koo, U. Kim, J. Jeon, J. Kim, and Y. Kwon, " A linearity-enhanced compact series-type Doherty amplifier suitable for CDMA handset applications," in *IEEE Radio and Wireless Symposium*, pp. 317–320, Jan. 2007.

[25] R. Wilkinson and P. Kenington, "Specification of error amplifiers for use in feedforward transmitters," in *IEE Proceedings on Circuits, Devices and Systems*, vol. 139, pp. 477–480, Aug. 1992.

[26] P. Kenington, " Efficiency of feedforward amplifiers," in *IEE Proceedings on Circuits, Devices and Systems*, vol. 139, pp. 591–593, Oct. 1992.

[27] O. Hammi, S. Bousnina, and F. Ghannouchi, " A linearized Doherty amplifier using complex baseband digital predistortion driven by CDMA signals," in *IEEE Radio and Wireless Conference*, pp. 435–438, Sept. 2004.

[28] S. Hong, Y. Y. Woo, J. Kim, J. Cha, I. Kim, J. Moon, and B. Yi, J.and Kim, "Weighted polynomial digital predistortion for low memory effect doherty power amplifier," *IEEE Microwave and Wireless Component Letters*, vol. 55, pp. 925 – 931, May. 2007.

[29] W.-J. Kim, K.-J. Cho, S. Stapleton, and J.-H. Kim, " piecewise pre-equalized linearization of the wireless transmitter with a Doherty amplifier," *IEEE Microwave and Wireless Component Letters*, vol. 54, pp. 3469–3478, Sept. 2006.

[30] J. Nam, J.-H. Shin, and B. Kim, "A handset power amplifier with high efficiency at a low level using load-modulation technique," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 2639–2644, August 2005.

[31] D. Yu, Y. woong Kim, K. Han, J. ho Shin, and B. Kim, "Fully integrated Doherty power pmplifiers for 5 GHz wireless-LANs," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[32] D. W. Ferwalt and A. Weisshaar, "A base control Doherty power amplifier for improved efficiency in GSM handsets," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 895–898, June 2004.

[33] J. Nam, J. Shin, and B. Kim, "Load modulation power amplifier with lumped-element combiner for IEEE 802.11b/g WLAN applications," in *Electronics Letters*, vol. 24, pp. 24–25, Jan. 2006.

[34] Agilent Technologies, *Advanced Design System User Manual*, 2006.

[35] AWR Microwave Office, *AWR Design Environment User Manual*, 2006.

[36] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. on Elect. Devices*, vol. 34, pp. 160–169, 1987.

[37] I. W. Smith, H. Statz, H. A. Haus, and R. A. Pucel, "On charge non-conservation in FET's," *IEEE Trans. on Elect. Devices*, vol. 34, pp. 2565–2568, 1987.

[38] R. Meyer and M. Stephens, "Distortion in variable-capacitance diodes," *IEEE Journal of Solid-State Circuits*, vol. Sc-10, pp. 47–54, Feb. 1975.

[39] K. Buisman, L. C. N. de Vreede, L. Larson, M. Spirito, A. Akhnoukh, T. Scholtes, and L. K. Nanver, "Distortion-free varactor diode topologies for RF adaptivity," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 157–160, Jun. 2005.

Appendix A

Manufacturer Specifications of the Selected Transistor

TRANSCOM

TC2571

REV3_20060519

1 W Low-Cost Packaged PHEMT GaAs Power FETs

FEATURES

- 1W Typical Output Power at 6 GHz
- 11dB Typical Power Gain at 6 GHz
- High Linearity: IP3 = 40 dBm Typical at 6 GHz
- High Power Added Efficiency:
  PAE ≥ 43 % for Class A Operation
- Suitable for High Reliability Application
- Breakdown Voltage: BV_{DGO} ≥ 15 V
- Lg = 0.35 µm, Wg = 2.4 mm
- 100 % DC Tested
- Low Cost Ceramic Package

PHOTO ENLARGEMENT

DESCRIPTION

The TC2571 is packaged with the TC1501 Pseudomorphic High Electron Mobility Transistor (PHEMT) GaAs Power chip. The Cu-based ceramic package provides excellent thermal conductivity for the GaAs FET. All devices are 100% DC tested to assure consistent quality. Typical applications include high dynamic range power amplifiers for commercial and military high performance power applications.

ELECTRICAL SPECIFICATIONS (T_A=25℃)

Symbol	CONDITIONS	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point , f = 6GHz V_{DS} = 8 V, I_{DS} = 240 mA	29.5	30		dBm
G_{1dB}	Power Gain at 1dB Gain Compression , f = 6GHz V_{DS} = 8 V, I_{DS} = 240 mA		11		dB
IP3	Intercept Point of the 3rd-order Intermodulation, f = 6GHz V_{DS} = 8 V, I_{DS} = 240 mA, *P_{SCL} = 17 dBm		40		dBm
PAE	Power Added Efficiency at 1dB Compression Power, f = 6GHz		43		dB
I_{DSS}	Saturated Drain-Source Current at V_{DS} = 2 V, V_{GS} = 0 V		600		mA
g_m	Transconductance at V_{DS} = 2 V, V_{GS} = 0 V		400		mS
V_P	Pinch-off Voltage at V_{DS} = 2 V, I_D = 4.8 mA		-1.7**		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at I_{DGO} =1.2 mA	15	18		Volts
R_{th}	Thermal Resistance		16		℃/W

*** P_{SCL} : Output Power of Single Carrier Level**

** For the tight control of the pinch-off voltage range, we divide TC2571 into 3 model numbers to fit customer design requirement (1)TC2571P1519 : Vp = -1.5V to -1.9V (2)TC2571P1620 : Vp = -1.6V to -2.0V (3)TC2571P1721 : Vp = -1.7V to -2.1V
If required, customer can specify the requirement in purchasing document. For special Vp requirement, please contact factory for details.

TRANSCOM, INC., 90 Dasoong 7th Road, Tainan Science-Based Industrial Park, Hsin-She Shiang, Tainan County Taiwan, R.O.C.
Web-Site: www.transcominc.com.tw Phone: 886-6-5050086 Fax: 886-6-5051602

TRANSCOM

TC2571

REV3_20060519

ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Symbol	Parameter	Rating
V_{DS}	Drain-Source Voltage	12 V
V_{GS}	Gate-Source Voltage	-5 V
I_{DS}	Drain Current	I_{DSS}
P_{in}	RF Input Power, CW	26 dBm
P_T	Continuous Dissipation	3.8 W
T_{CH}	Channel Temperature	175 °C
T_{STG}	Storage Temperature	- 65 °C to +175 °C

RECOMMANDED OPERATING CONDITION

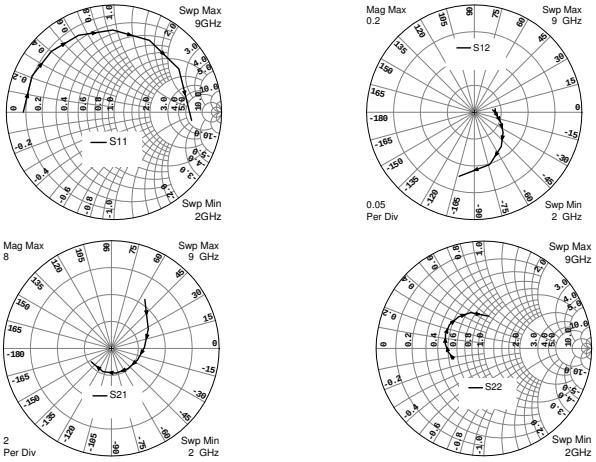
Symbol	Parameter	Rating
V_{DS}	Drain to Source Voltage	8 V
I_D	Drain Current	240 mA

HANDLING PRECAUTIONS :

The user must operate in a clean, dry environment. Electrostatic Discharge(ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must less than 300V.

TYPICAL SCATTERING PARAMETERS (T_A=25℃)

Power Bias : V_{DS} = 8 V, I_{DS} = 240 mA



FREQUENCY	S11		S21		S12		S22	
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2	0.8422	179.88	4.4104	55.63	0.0378	4.41	0.2968	-160.56
3	0.8330	156.09	3.0979	27.48	0.0410	-5.11	0.3334	-174.58
4	0.8128	135.66	2.4617	1.60	0.0463	-13.48	0.3617	172.88
5	0.7880	114.61	2.1283	-23.92	0.0531	-21.93	0.3796	159.66
6	0.7645	90.83	1.9470	-50.89	0.0655	-35.02	0.3879	145.45
7	0.7467	63.85	1.8797	-79.40	0.0813	-51.82	0.3770	128.62
8	0.7247	33.82	1.8428	-109.44	0.1016	-73.69	0.3550	110.31
9	0.7245	-5.98	1.7925	-146.06	0.1226	-103.34	0.3032	81.57

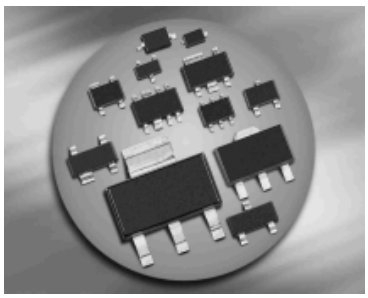
TRANSCOM, INC., 90 Dasoong 7th Road, Tainan Science- Based Industrial Park, Hsin-She Shiang, Tainan County Taiwan, R.O.C.
Web-Site: www.transcominc.com.tw Phone: 886-6-5050086 Fax: 886-6-5051602

Appendix B

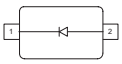
Manufacturer Specifications of the Selected Varactor Diode

Silicon Tuning Diode

- For SAT tuners
- High capacitance ratio
- Low series resistance
- Excellent uniformity and matching due to "in-line" matching assembly procedure



BB837
BB857



Type	Package	Configuration	L_S(nH)	Marking
BB837	SOD323	single	1.8	M
BB857	SCD80	single	0.6	OO

Maximum Ratings at T_A = 25°C, unless otherwise specified

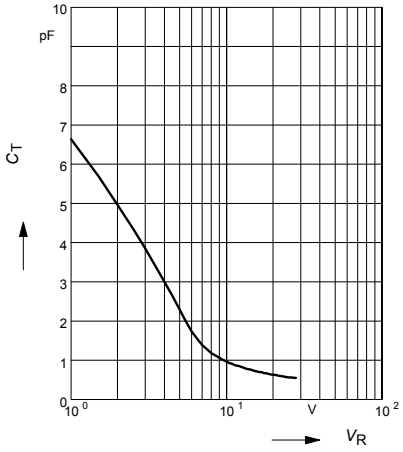
Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	30	V
Peak reverse voltage $R \geq 5k\Omega$	V_{RM}	35	
Forward current	I_F	20	mA
Operating temperature range	T_{op}	-55 ... 150	°C
Storage temperature	T_{stg}	-55 ... 150	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

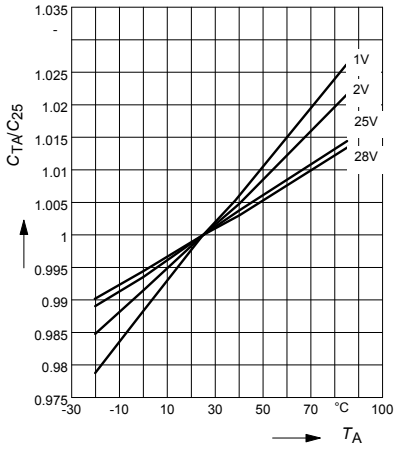
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Reverse current	I_R				nA
V_R = 30 V		-	-	10	
V_R = 30 V, T_A = 85 °C		-	-	200	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 1 V, f = 1 MHz		6	6.6	7.2	
V_R = 25 V, f = 1 MHz		0.5	0.55	0.65	
V_R = 28 V, f = 1 MHz		0.45	0.52	-	
Capacitance ratio	C_{T1}/C_{T25}	10.2	12	-	-
V_R = 1 V, V_R = 25 V, f = 1 MHz					
Capacitance ratio	C_{T1}/C_{T28}	9.7	12.7	-	
V_R = 1 V, V_R = 28 V, f = 1 MHz					
Capacitance matching[1)]	$\Delta C_T/C_T$	-	-	5	%
V_R = 1V ... 28V, f = 1 MHz, 7 diodes sequence					
Series resistance	r_S	-	1.5	-	Ω
V_R = 5 V, f = 470 MHz					

[1]For details please refer to Application Note 047

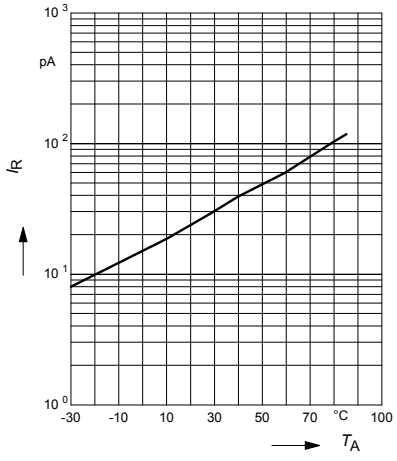
Diode capacitance $C_T = f(V_R)$
f = 1MHz



Normalized diode capacitance
$C_{(TA)}/C_{(25°C)} = f(T_A)$; f = 1MHz



Reverse current $I_R = f(T_A)$
V_R = 28V



Reverse current $I_R = f(V_R)$
T_A = Parameter