STUDY OF ADVANCED GATE STACK USING HIGH-K DIELECTRIC AND METAL ELECTRODE

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2008

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A THESIS SUBMITTED FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

NATIONAL UNIVERSITY OF SINGAPORE

2008

ACKNOWLEDGMENTS

First of all, I would like to express my heartfelt thanks to my two supervisors, Professor Yoo Won Jong and Professor Cho Byung Jin. I have been truly blessed to purchase Ph. D. under their supervision. Their guidance, support, and generosity have made me where I am today. I thank them for developing my potential and personality as well. I would like to take this opportunity to express my gratitude to my co-supervisor, Professor Chan Siu Hung. This thesis would not have been completed without his support and advice.

I would also like to sincerely thank other advisors and teaching staffs in Silicon Nano Device Lab (SNDL): Professor Li Ming Fu, Associate Professor Ganesh Samudar, Dr. Zhu Chunxiang, Dr. Lee Sungjoo, and Dr. Yeo Yee-Chia for their valuable comment and suggestions on my research work during internal meetings and seminars. The technical staffs in SNDL are also gratefully acknowledged: Mr. Yong Yu Fu, Patrick Tang, Mr. O Yan Wai Linn, and Lau Boon Teck.

Many thanks to my fellows and vital friends: Wang Xinpeng, Lim Eu-Jin, Pu Jing, Zhang Lu, He Wei, Shen Chen, Gao Fei, Li Rui, Song Yan, Chen Jingde, Tan Kian Ming, Yang Weifeng, Eric Teo Yeow Hwee, Dr. Zhu Ming, and Rinus Lee Tek Po for their useful discussion and everlasting friendships. Last but not least, my special gratitude to Mr. Whang Sung Jin, Ms. Oh Hoon Jung, and Mr. Choi Kyu Jin for their help in many ways; their care and mature experience in semiconductor technology.

My deepest thanks to my wife, Jin Hye Hyun, whose encouragement have made this work possible. Special recognition to my parents for their sacrifice and unconditional love.

SUMMARY

High-K dielectric and metal electrode are intensively studied to replace current SiO_2 dielectric and poly-Si electrode for continuous success of CMOS technology. The study on the formation of advanced gate stacks using high-K dielectric and metal electrode is included within the scope of this thesis. Several challenges regarding formation of metal electrode (chapter 2), high-K removal (chapter 3), hard mask effect on formation of metal electrode (chapter 4), and selection of metal electrode (chapter 5) are identified and addressed in this work.

For the integration of metal electrode in the gate stacks, plasma etching properties of metal electrode such as TaN, TiN, and HfN are discussed on anisotropic profile and high selective etching over underlying HfO_2 dielectric in chapter 2. High selective etching of metal electrode is achieved by the addition of O_2 in Cl_2. The etch rates of metal electrode slightly increase while etch rates of Hf-based high-K dielectric decrease by adding small amount of O_2 in Cl_2. Besides the high selective etching of metal electrode over Hf-based high-K dielectric, anisotropic profile is obtained by the appropriate passivation film on the sidewall of the gate stacks. The quality of this sidewall passivation film is analyzed by XPS analysis. Anisotropic profile and high selectivity over underlying HfO_2 could be achieved based on these results.

In addition to etching of metal electrode, removal of high-K dielectric is another big issue for a successful gate stack formation. In this work, alternative to wet etching or plasma etching for high-K dielectric removal, mixed process consisting of plasma treatments followed by wet removal will be proposed for removal of high-K dielectric on S/D regions in chapter 3. The feasibility of the low ion energy assisted wet removal process for short channel high-K MOS device fabrication is demonstrated by the smaller shift of threshold voltage and the higher driving current, compared to

the high ion energy assisted wet removal process as well as the wet-etching-only process.

Introducing new materials in the gate stacks as well as continuous scaling down faces challenges to meet the requirements of various device performance and low production cost. This also requires various attempts to develop small gate patterning technology. From these studies, SiO_2 or Si_3N_4, so-called hard mask, was proposed to replace conventional PR mask. In chapter 4, the effect of SiO_2 or Si_3N_4 on etching properties of metal gates is discussed. Reduced etching rates of advanced metal gate (TaN, TiN, and HfN) due to the SiO_2 / Si_3N_4 hard masks are observed in Cl_2 plasma. Si and O released from hard masks react with metal surfaces newly exposed to the plasma during etching, and the metal oxides formed on the etched surface retard the etch rates.

At last, selection of appropriate gate materials is still a big task to handle for advanced gate stack formation. The selection of materials in the gate stack is an ongoing research work, and has not been known for future gate stacks. So far, transition metal nitrides have been studied intensively for NMOS application whereas high work function materials have been proposed for PMOS. In this work, new gate metal electrode in the form of transition metal carbide is proposed and demonstrated for NMOS in chapter 5. Various metal carbides such as HfC, TaC, WC, and VC have been evaluated to implement metal carbides in the gate stacks. Based on the intensive study regarding basic material and electrical properties, HfC was proposed and demonstrated for NMOS application. HfC on HfO_2 showed a very low work function value, excellent thermal stability and diffusion barrier properties, and negligible Fermi level pinning. Therefore, the hafnium carbide is a promising candidate for NMOS gate electrode material for gate-first metal gate CMOS process.

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LIST OF SYMBOLS

C_{ox}	Gate dielectric capacitance
E_i	Ion energy
E_c	Silicon conduction band edge
$E_{F,m}$	Fermi level of metal electrode
E_g	Silicon bandgap
E_{th}	Threshold ion energy
E_{vac}	Vacuum energy level
E_v	Silicon valence band edge
ΔG_f^o	Gibb's free energy of formation
hp	Industry's most aggressive half-pitch target
J_g	Gate leakage current density
J_i	Ion current density
K	Dielectric permittivity constant
N_b	Doping concentration of Si substrate
P_b	Bottom power
Q_d	Total depletion charge in the channel region
Q_{ox}	Equivalent oxide charge density at the oxide/Si
S	Surface area of the wafer
t_{eq}	Equivalent oxide thickness
T_{high-k}	Thickness of high-k film
V_d	Drain voltage
V_{dc}	Self-bias voltage
V_{FB}	Flat-band voltage
V_g	Gate voltage
V_{th}	Threshold voltage
$W_{d\,poly}$	Thickness of poly-Si depletion layer
ε_M	Effective permittivity of M film
Φ_B	Difference between Fermi-level and intrinsic level
Φ_M	Metal work function
Φ_{MS}	Work function difference between metal electrode and silicon substrate
Φ_{Si}	Silicon work function

LIST OF ACRONYMS

AES	Auger electron spectroscopy
ALD	Atomic layer deposition
AFM	Atomic force microscopy
CD	Critical dimension
CES	Constant field scaling
CMOS	Complimentary metal oxide semiconductor
C-V, CV	Capacitance versus Voltage
CVD	Chemical vapor deposition
CVS	Constant voltage scaling
DHF	Diluted hydro fluoric acid
DPS™	Decoupled plasma source
EOT	Equivalent oxide thickness
FCC	Face-centered cubic
FDSOI	Fully-depleted silicon on insulator
FET	Field effect transistor
F-N	Fowler-Nordheim
FGA	Forming gas annealing
FinFET	Fin field effect transistor
FLP	Fermi-level pinning
FUSI	Fully silicided
HRTEM	High resolution transmission electron microscopy
HP	High performance
IC	Integrated circuit
ICP	Inductively coupled plasma
I-V, IV	Current versus voltage
ITRS	International technology roadmap of semiconductors
LOP	Low operation power
LPCVD	Low pressure chemical vapor deposition
LSTP	Low standby power
NMOS(FET)	n-channel MOSFET

MOCVD	Metal organic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field effect transistor
MPU	Microprocessor unit
OES	Optical emission spectroscope
PECVD	Plasma enhanced chemical vapor deposition
PDA	Post deposition anneal
PMOS(FET)	p-channel MOSFET
PR	Photo resist
PVD	Physical vapor deposition
RF	Radio frequency
RMS	Root mean square
RTA	Rapid thermal annealing
S/D	Source and drain
SEM	Scanning electron microscope
SIMS	Secondary ion mass spectroscopy
STI	Shallow trench isolation
TEM	Transmission electron microscopy
WF	Work function
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

CHAPTER 1

INTRODUCTION

1.1 Overview

From everyday experience, we cannot imagine life without the microelectronic devices. The silicon based microelectronic devices have successfully been evolved for the last 40 years since the invention of the first integrated circuit (IC) in 1958. The evolution with higher speed, greater performance, and lower production cost has been led by simply reducing the dimensions of the active area of transistor such as gate dielectric thickness and gate length. The scaling down of device dimensions is quite accurately governed by Moore's law [1.1] which predicts that the number of transistors on a chip doubles every two years, resulting in higher performance, lower production cost, and smaller chip with greater functionality. Figure 1.1 illustrates the number of devices integrated in the different generations of Intel's microprocessors as a function of the production year [1.2]. It indicates that over the past 35 years from 1971 to 2007, the minimum feature size in a typical semiconductor process technology has been reduced from 8 μm in 1972 to the current 65 nm technology.

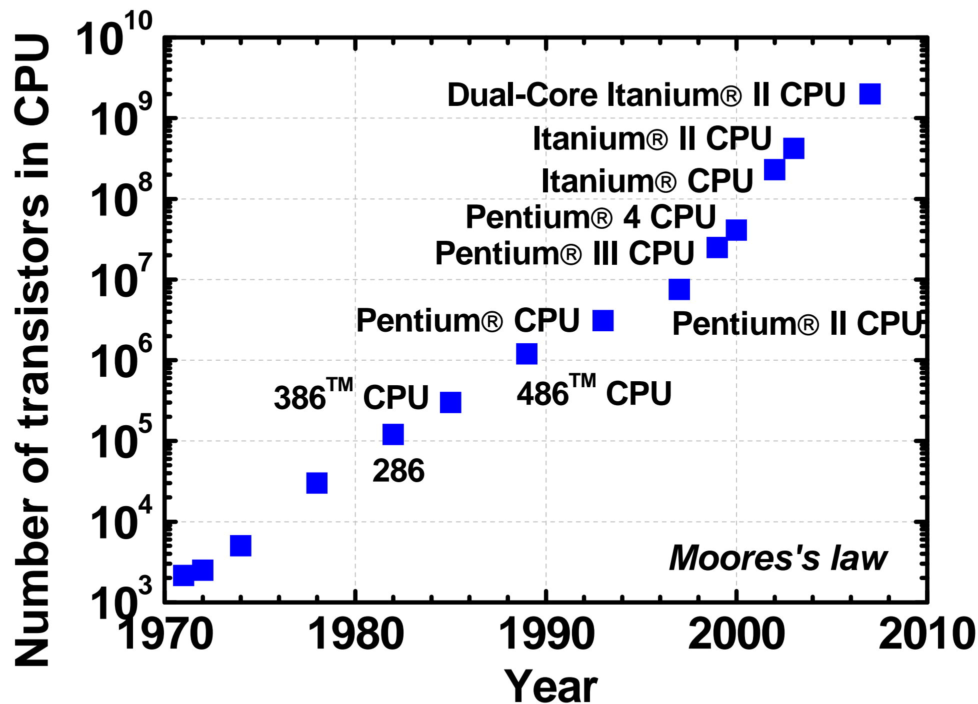

Fig. 1.1 Number of CPU transistor from 1970s to present, showing the device scaling according to Moore's Law; © Intel Corporation [1.2].

1.2 MOSFET Scaling: Opportunities and Challenges

MOSFET scaling has been aided by the rapid advancement of lithographic techniques. Several scaling rules such as constant-field scaling (CES), constant-voltage scaling (CVS), and generalized scaling were proposed to provide a basic guideline to the design of scaled MOSFETs [1.3]. In reality, scaling rules have followed mixed rule of CES and CVS. The principle of the generalized scaling is to scale both the electric field and the physical dimensions (both lateral and vertical) of MOSFET by different factors respectively. The requirement of reducing the supply voltage (V_d) by the same factor as the physical dimensions it too restrictive; therefore, the supply voltage (V_d) typically

scales slower than the channel length, which leads to the increase of electric field by a factor of α, as well as the increase of power density by a factor of α^2 to α^3. It leads to higher power dissipation of chips. This higher power dissipation becomes a considerable challenge for the continuous scaling of CMOS into deep-submicron regimes. In order to cope with the challenge of high power dissipation while maintaining higher performance, innovative device structures as well as new materials have to be explored.

1.2.1 Limitation of SiO_2 as the Gate Dielectrics

The excellent physical, chemical, and electrical properties of SiO_2 as a gate dielectric enable the Si-based MOSFET to successfully scale down for several decades [1.4]. However, as SiO_2 dielectric continues to shrink less than 2nm, only several atoms in thickness, several serious challenges are identified [1.5, 1.6]. The main issue is the direct tunneling current through the ultra thin SiO_2 which rise exponentially as the thickness of SiO_2 decrease [1.6]. The gate leakage will be dominated by direct tunneling rather than Fowler-Nordheim (F-N) tunneling through a triangular barrier, resulting in high standby power dissipation, high sub-threshold current, and poor controlling of field effect. Besides the direct tunneling, ununiformity, variability, will be another issue. It means only one atom variation over the large wafer size causes the more than 20% ununiformity over the entire devices; once thickness of SiO_2 is below 1.2nm. In addition, it was reported that there is a minimum thickness, 0.7nm, for SiO_2 to maintain its bulk properties, which means SiO_2 as a gate dielectric is invalid beyond 2010 according to table 1.1 [1.7]. Therefore, an alternative, instead of SiO_2, must be proposed.

Table 1.1 Gate dielectric technology requirements – selected data from latest ITRS- 2006 update.

Year of Production	***2007***	***2008***	***2009***	***2010***	***2011***
Technology node	*Hp65*	*Hp57*	*Hp50*	*Hp45*	*Hp40*
Physical gate length for HP (nm)	25	22	20	18	16
Physical gate length for LOP (nm)	32	28	25	22	20
Physical gate length for LSP (nm)	45	37	32	28	25
EOT for HP (nm)	1.1	1.0	0.9	0.65	0.5
EOT for LOP (nm)	1.2	1.1	1.0	0.9	0.9
EOT for LSP (nm)	1.9	1.6	1.5	1.4	1.4
Gate leakage at 25°C for HP (A/cm^2)	800	1180	1100	1560	2000
Gate leakage at 25°C for LOP (A/cm^2)	78	154	161	110	450
Gate leakage at 25°C for LSP (A/cm^2)	0.022	0.027	0.031	0.036	0.048

1.2.2 Post SiO_2 Dielectric: High-K Dielectric

Alternative gate dielectrics had been focused on SiON and SiO_2 / Si_3N_4 stacks in order to figure out whose permittivity is higher than that of SiO_2. Even if it leads to reduction of leakage and better reliability characteristics [1.8, 1.9], the SiON and SiO_2/Si_3N_4 stacks work well only down to 1.5nm. Below this, either high gate leakage or degradation of electron channel mobility limits the further improvements in these approaches. As an alternative to these gate stacks, lot of works have been done on high

permittivity (k) materials [1.10] such as Ta_2O_5 [1.11, 1.12], TiO_2 [1.13], Al_2O_3 [1.14], and HfO_2 [1.15] to replace SiO_2 or SiON. The high-k dielectrics provide a physically thicker film while maintaining same or low electrical thickness, resulting in reduction of direct tunneling current and improving the gate capacitance as shown in equation (1.1).

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-\kappa}} T_{high-\kappa,Phy} \qquad (1.1)$$

The candidate high-k dielectrics should have suitable permittivity (k $\approx$ 15-25), large barrier height for both electron and hole, high crystallization temperature, good thermal stability, and high carrier mobility for both electrons and holes. Among the various candidates of high-k dielectric, the HfO_2 has been extensively studied due to the appropriate k-values and relatively high barrier heights for both electrons and holes [1.10, 1.16, and 1.17]. Figure 1.2 shows the scalability of some higk-k dielectrics compared with the *ITRS* requirements [1.18]. It clearly shows that the gate leakage reduction can be achieved by 2 ~ 4 orders compared to SiO_2 by using high-k dielectrics.

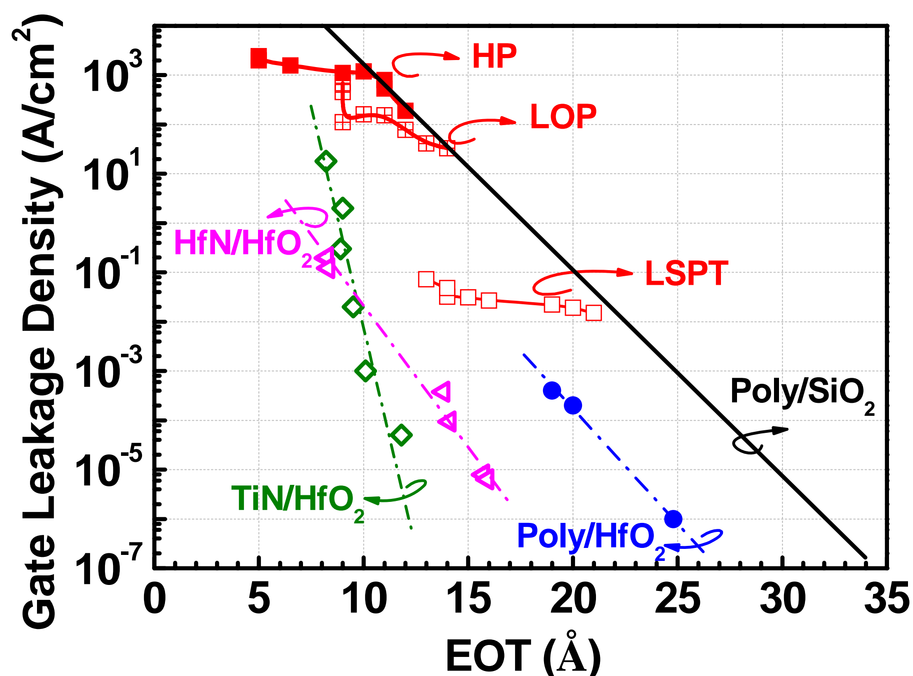

Fig. 1.2 Gate leakage current density of some high-κ dielectrics [1.18] as a function of EOT, compared with the gate leakage specifications for high-performance (HP), low-operating-power (LOP), and low-standby-power (LSTP) applications according to *ITRS* 2006 update.

1.2.3 Limitation of Poly-Si as Gate Electrode

Poly-Si has been used as a superior gate electrode for the gate-first CMOS process since 1970s, due to the excellent thermal stability with SiO_2 and easy adjustment of its work function by dopant implantation. However, as the device continues to shrink into the HP-45 nm technology node and beyond, conventional poly-Si is facing several fundamental limits such as poly-Si depletion [1.19], dopant penetrated effect [1.20], high gate resistivity [1.21], and compatibility with high-k dielectrics [1.22, 1.23].

Firstly, the poly-Si depletion is observed under the inversion mode of MOSFET as shown in Fig. 1.3. It shows that a depletion layer with a finite thickness is formed in the

poly-Si gate side near the poly-Si / oxide interface under the inversion mode, resulting in band bending, in other words, voltage drop in the depletion region. It causes a less inversion charges in the channel side and, thereby, leads to loss of gate control and reduction of drive current. The depletion regions due to poly-depletion can be reduced by increasing the doping concentration in poly-Si, but this may aggravate the dopant penetration problem, Moreover, even if doping concentration can be increased, the active dopant concentration will finally be restricted by the solid solubility of dopant in poly-Si. Figure 1.4 shows that three is no tolerance for poly-Si depletion beyond year 2010 [1.24]. Therefore the poly-Si electrode should be replaced by metal gate electrodes in which the electron density is high enough to make the gate depletion layer negligible.

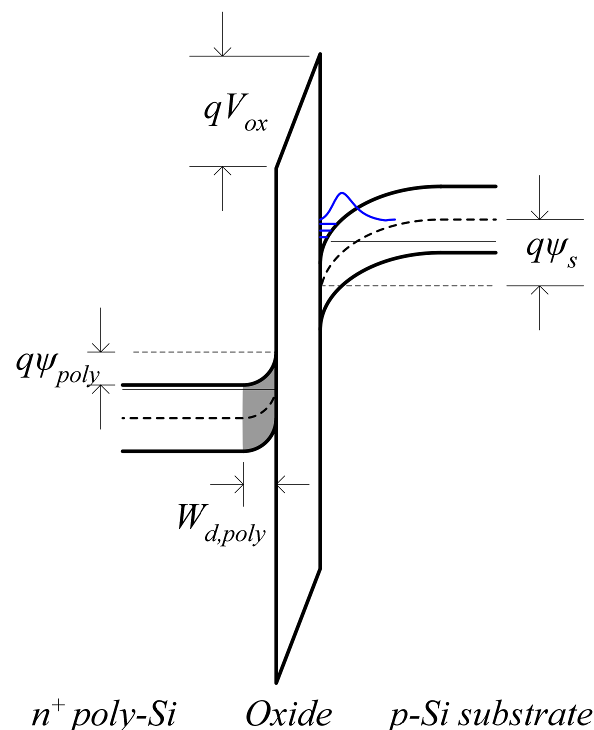

Fig. 1.3 The energy band diagram of an NMOS device showing the poly-Si gate depletion effect [1.25].

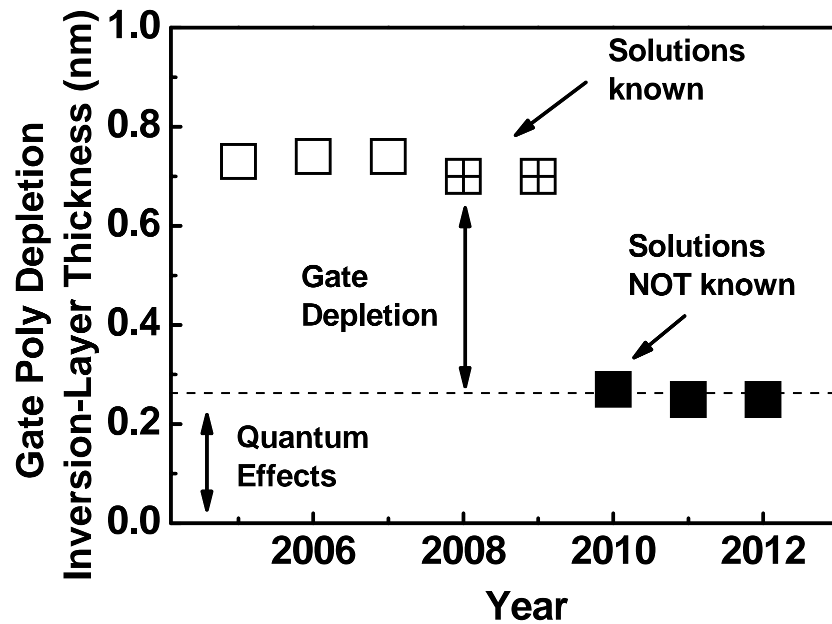

Fig. 1.4 Additional increase of electrical thickness caused by gate electrode depletion and quantum effects vs. projection years [1.24].

Secondly, dopant penetration into channel region from the heavily doped poly-Si electrode is another challenge for conventional poly-Si. The penetrated dopant degrades the quality of channel properties, causing instability of threshold voltage of transistors and raising some reliability concerns. A dopant-free metal gate electrode would be a potential solution to avoid the dopant penetration problem ultimately.

Thirdly, the other issue for conventional poly-Si is high gate resistivity. The resistivity of gate electrode determines the gate *RC* delay of digital circuits, particularly in radio-frequency (RF) applications [1.21]. Therefore, low resistivity material to replace conventional poly-Si is required to meet the sheet resistance specification for the gate electrodes.

Last but not least, as high-k dielectrics replace conventional SiO_2 dielectrics, compatibility of poly-Si electrode with high-k dielectrics become the critical issues due to

the interface quality between poly-Si and high-k. The identified challenge of poly-Si electrode with high-k dielectrics is Fermi-level pinning (FLP) which cause an undesirable shift of flat-band voltage V_{FB} [1.26, 1.27, and 1.28]. Many works have been done to find out the root cause of the FLP problem. It may be caused by dopant penetration and thereby formation of HfB_2 [1.26], formation of accepter or donor like interface [1.29], Hf-Si bond causing dipole [1.30], and oxygen vacancy on high-k side [1.30, 1.31]. Even if several mechanisms have been proposed, the origin of FLP still remains ambiguous. In summary, even if the conventional poly-Si has been used for gate electrode, several vital challenges such as poly-Si depletion, dopant penetration, high gate resistivity, and compatibility with High-k become more severe with scaling down of device feature.

1.2.4 Post Poly-Si Electrode: Metal Electrode

Metal electrode can eliminate the poly-Si depletion which is the main challenges for conventional poly-Si electrode. Additional advantages of metal electrode include elimination of boron penetration and the reduction of the gate resistivity. Furthermore, metal electrode could minimize the FLP due to the avoidance of Si-Hf bond in the interface between metal electrode and Hf-based high-k dielectrics.

To realize the metal electrode in the gate stacks, several methods have being tried such as gate last metal process [1.32], fully silicided (FUSI) [1.33] and gate first metal process [1.34]. Firstly, gate last metal gate was introduced in the gate stack [1.32], because the process is free from thermal instability of gate materials. However, process complex and difficulty of removing materials without damaging other active area are remaining challenges. For considering high cost and risk of technology migration, a little modification to the conventional process would be more benefit. In that sense, FUSI process was proposed and demonstrated using $CoSi_2$ [1.35] and NiSi [1.36]. So far, even

if intensive studies have been done, this process is still suffering from the phase instability of silicide and narrow process window causing deviations in work function particularly in the small gate length [1.37]. It is believed that even if gate last metal process and FUSI process show many advantage, the advantages of gate first metal process overweight the advantages of gate last metal process and FUSI process, because gate first metal process shows a best process compatibility with conventional CMOS process and minimal changes in process sequence.

1.3 Challenges in Formation of Metal/High-K Gate Stack

As both high-K dielectric and metal electrode are expected to be implemented at the same time for the next generation technology, wide-ranging studies of finding out appropriate materials and developing process integration have been carried out to realize the metal / high-K gate stacks. Selection of appropriate materials is mainly related to metal electrode and high-K dielectrics, whereas developing process integration is mainly related to both plasma etching and wet etching. The proper high-K dielectrics will be selected in terms of several issues such as thermal stability, interfacial layer growth, channel mobility, and threshold voltage. On the other hand, the proper metal electrode will be selected in terms of work function, thermal stability, and threshold voltage.

While the studies to find out right materials such as high-K dielectric and metal electrode in the gate stacks have been done intensively, the study of both plasma etching and wet etching for formation of advanced gate stack, so far, has not been carried out yet intensively. Even if electrical performance is achieved by implementation of proper materials in the advanced gate stacks, other properties such as etching must be investigated in order to implement these materials in the gate stacks successfully. In fact,

electrical performance of devices is affected by gate length, gate stack profile, residues and cleaning process; all of these are controlled by the etching process. So it is important to study etching properties in the advanced gate stacks as well as finding proper materials for the gate stacks.

1.3.1 Plasma Etching of Metal Electrode in Halogen Gases

Lots of etching works have been done on the formation of conventional poly-Si / SiO_2 gate stacks in mainly HBr plasma, leading to fulfillments of the requirement guided by *International Technology Roadmap for Semiconductors* (ITRS) [1.4]. With the help of understanding etching mechanism of poly-Si / SiO_2 gate stacks in mainly HBr plasma, conventional poly-Si / SiO_2 gate stack shows a 90° profile and almost infinite selectivity over underlying SiO_2 dielectric [1.38]. On the contrary, a lot of non-volatile residues are generated during the metal etching in HBr due to the high boiling temperature of its byproduct [1.39], resulting in difficulty of successful formation of gate stacks [1.40]. Most of the metal-bromide byproducts are nonvolatile and remains on the etched surface as well as sidewall in the gate stacks. The residues on the gate stacks will lead to CD gain, poor reliability, and contamination issues. The significance of CD gain due to the formation of residues on the sidewall of gate stacks is highlighted in terms of CD increase of gate length in the table 1.2. It shows that if 89° profile is formed, CD gain is 3.5nm representing 25% increase of gate CD in 2012.

Even if etching studies of metal electrode have been done in Cl_2, SF_6, CF_4, and CHF_3, most works of the metal etching have done on individual materials for metal and dielectric [1.41]. Etching study of individual materials is quite different from etching study of gate stacks, because most of the etching challenges such as selectivity, formation of residues and profile are revealed in the gate stack formation. However, referring to

etching properties in the advanced gate stacks; few studies have been done [1.42-1.44]. For the metal etching in the gate stack, anisotropic profile, high selectivity over underlying high-K dielectric, and detection of end point are remaining challenges.

Table 1.2 CD increase of Gate length @ 89º =3.5nm [1.24]

Projection year	2007	2010	2012
MPU physical gate length	25nm	18nm	14nm
% increase	14	19	25

1.3.2 Selective Removal of High-K Dielectric

Addition to the metal etching in the gate stacks, selective removal of the gate dielectrics from S/D region successfully is another key processing challenges. While conventional SiO_2 is well removed by DHF with high selectivity over underlying Si substrate, some high-K dielectrics such as HfO_2 after PDA show a very strong resistance on DHF [1.45], resulting in challenges on directional and anisotropic formation of high-K dielectrics. Usually, the high-K dielectrics are thicker in thickness than conventional SiO_2, thereby the isotropic wet etching would cause significant undercut and lead to device reliability. Furthermore, some of the candidate high-K dielectrics are quite inert to strong acids, making to difficult to remove the materials completely and leaving some residue on S/D region [1.46, 1.47]. In order to overcome the difficult on wet etching of high-K dielectrics, damascene gate integration was proposed [1.48], however, it is expected that it requires complex and additional process steps, leading to high processing cost. Alternative to wet etching, plasma etching of high-K dielectrics was demonstrated using F-, Cl-, and Br-based halogen gases [1.49-1.51]. Nevertheless many efforts to removal of high-K dielectrics by plasma, it was reported that plasma etching-only-process maybe

inapplicable to remove high-K dielectrics, because it tends to generate large amounts of nonvolatile byproducts of Hf-based high-K dielectrics in F, Cl, and Br based halogen plasmas [1.52]. In addition, plasma etching of high-K dielectric shows a very low selectivity which can cause a consumption of S/D region. As thickness of Si is thinner in SOI technology, this consumption of Si disables this approach to be implemented. Therefore, other alternatives in stead of wet etching and plasma etching should be developed.

1.3.3 Photoresist Mask in Advanced Gate Stack

As device continues to shrink with introduction of new materials in the gate stack, not only metal electrode / high-K dielectric, but also conventional photoresist mask is facing several challenges. The challenges include CD gain caused by erosion and swelling of PR, as well as re-deposition of PR byproducts [1.53]. In addition to CD gain, conventional PR mask possesses several challenges such as low etching selectivity to metal electrode [1.54]. Therefore, it becomes evident that hard mask is urgently required to overcome these challenges. Even if the use of hard mask can provide significant advantages, it should be noted that extra deposition and etch step are added to the overall process to form hard mask. In addition, in most CMOS process, hard mask needs to be completely removed prior to the subsequent silicidation step on top of poly-Si gate electrodes. During the removal of hard mask, unwanted erosion and notching of gate dielectrics, shallow trench isolation (STI), and sidewall spacers should be avoided. Therefore, for the selection of hard mask, highly selective removal of hard mask technique against gate dielectrics, STI, and sidewall spacers is required. Meanwhile, metal electrode is being extensively studied to replace poly-Si as a gate electrode in CMOS process. The introduction of both hard mask and metal electrode in the gate stacks

brings out new challenges in the etching process, because more nonvolatile byproducts are generated with the presence of hard mask during etching of metal electrode. Etching of poly-Si under hard mask is well understood [1.54] whereas etching of metal electrode under hard mask has hardly been discussed [1.55].

Therefore, the hard mask effect on gate stacks of metal electrode / high-K dielectric should be investigated and understood for successful implementation of hard mask in the gate stack.

1.3.4 Challenges of Metal Electrode Selection

Material selection is still ongoing and one of the most challenging issues for formation of advanced gate stacks. When it comes to selection of metal electrode, work function of metal is one of the most important parameters for metal electrode candidates. The metal work function directly leads to the threshold voltage (V_{th}) of MOSFET. The V_{th} of a MOSFET is typically given by the following equation (1-2) [1.56]:

$$V_{th} = V_{FB} + 2\phi_B + \frac{Q_d}{C_{ox}} = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_{Si} q N_b \phi_B}}{C_{ox}} \qquad (1\text{-}2)$$

where V_{FB} is the flat band voltage across the MOS stack, Φ_B is the difference between the Fermi-level and the intrinsic level of Si substrate, Q_d is the total depletion charge in the channel region, C_{ox} is the gate dielectric capacitance, ε_{Si} is the permittivity of Si, and N_b is the doping concentration of Si substrate (for uniform channel doping). Here, V_{FB} can be expressed by the following equation (1-3):

$$V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} = (\Phi_M - \Phi_S) - \frac{Q_{ox}}{C_{ox}} \qquad (1\text{-}3)$$

where Φ_{MS} is the work function difference between the metal electrode (Φ_M) and silicon substrate (Φ_S), Q_{ox} is the equivalent oxide charge density at the oxide / Si interface. It shows that metal work function controls V_{FB} for a given C_{ox} and Q_{ox} as shown in equation (1-3). In turn, V_{FB} directly affects V_{th} as shown in equation (1-2). It was reported that the work function of metal electrode should be located about 4.05~4.25 eV and 4.97~5.17 eV for NMOS and PMOS respectively for sub-50-nm bulk-Si devices [1.57]. In other words, the work function of metal electrode should be within 0.2 eV from the band-edges of Si as shown in fig. 1.5. In that sense, for the fully-depleted and multi-gate devices, e.g. FDSOI or FinFET, work function of metal electrode should be located above or below 0.15 eV from the mid-gap level of Si, because work function of Si substrate is mid-gap level, almost intrinsic level for the FDSOI or FinFET [1.58]. Recently, it was reported that band-edge work function of Si is required for metal electrode as the body thickness of ultra-body SOI is below 5nm, even if the channel property is intrinsic Si [59].

Figure 1.5 shows that metals such as Ta, Hf, Zr, and Al are suitable for NMOS application whereas Ni, Ir, Ru, and Pt are suitable for PMOS application in terms of work function consideration. Even if these materials satisfy the work function requirement, these pure materials reveal several challenges in terms of process integration. The materials for NMOS application are very reactive in nature and thereby they can not sustain the S/D activation process, whereas the materials for PMOS application are very inert in nature and thereby they possess etching challenges and film stress/poor adhesion issues. When it comes to the materials for NMOS application, alloy material in the form of metal nitrides was proposed to overcome this poor thermal stability [1.60]. However, the work function of these metal nitrides moves from low work function to mid-gap level

after S/D activation process. Recently, the very low work function materials such as Tb, Er, and Yb were incorporated in the metal nitride to obtain low work function property even after S/D activation process [1.61]. However, this approach brings out new etching challenges due to the high boiling temperature of etching by-products in halogen gases [1.62]. When it comes to PMOS application, the challenge is more serious, because it is difficult to form binary structure such as nitrides using those Ni, Ir, Ru, and Pt. Therefore, a new approach is required for selection of gate electrode materials for NMOS and PMOS application respectively.

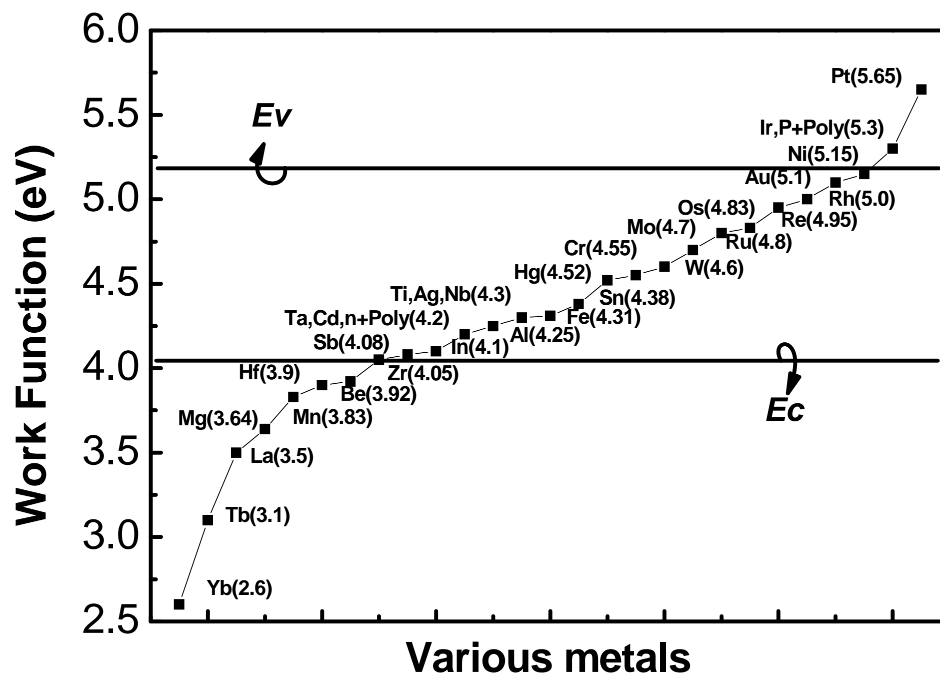

Fig. 1.5 Work function of various metals for CMOS application [1.63].

1.4 Research Scope and Major Achievement in this Thesis

The overall objective of this work is to: develop a proper integration schemes (Chapter 2 and 3), identify some issues (chapter 4), and propose new gate materials (chapter 5) for formation of advanced metal / high-K gate stacks. These attempts could be of practical values for the formation of advance metal/high-K gate stacks.

For the integration of metal electrode in the gate stacks, plasma etching properties of metal electrode such as TaN, TiN, and HfN will be discussed on anisotropic profile and high selectivity over underlying HfO_2 dielectric in the chapter 2. The linear dependence of etch rates of metal nitrides on the square root of bias voltage indicates the dominance of ion-induced etch mechanism of the metal nitrides. This phenomenon is well-explained by internal binding energy of substrate, evaporation temperature and Gibb's free energy (ΔG_f^o) of formation of by-products. The addition of O_2 in Cl_2 and HBr decreased etch rates of the metal nitrides and HfO_2; however, for O_2 concentration lower than 1.5% in Cl_2, a slight increase of etch rates of the metal nitrides was observed while decrease of etch rates of high-K dielectrics. Anisotropic profile and high selectivity over underlying HfO_2 could be achieved based on these results.

In addition to etching of metal electrode, removal of high-K dielectric is another big issue for successfully gate stack formation. In this work, alternative to wet etching or plasma etching for high-K dielectric removal, mixed process consisting of plasma treatments followed by wet removal will be proposed for removal of high-K dielectric on S/D regions in chapter 3. The feasibility of the low ion energy assisted wet removal process for short channel high-K MOS device fabrication would be demonstrated by the

smaller shift of threshold voltage and the higher driving current, compared to the high ion energy assisted wet removal process as well as the wet-etching-only process.

Introducing new materials in the gate stacks as well as continuous scaling down faces challenges to meet the requirements of various device performance and low production cost [1.64]. This also requires various attempts to develop small gate patterning technology [1.65, 1.66]. From these studies, SiO_2 or Si_3N_4, so-called hard mask, was proposed to replace conventional PR mask. In chapter 4, the effect of SiO_2 or Si_3N_4 on etching properties of metal gates will be discussed. Reduced etching rates of advanced metal gate (TaN, TiN, and HfN) due to the SiO_2/Si_3N_4 hard masks are observed in Cl_2 plasma. Si and O released from hard masks react with metal surfaces newly exposed to the plasma during etching, and the metal oxides formed on the etched surface retard the etch rates. The suppression of etch rates from using hard mask is more obvious for TiN than for TaN and HfN, because Ti oxides are formed readily on the etched TiN surface due to their low Gibb's free energies of formation. The surface of TiN degrades with etching time when SiO_2 mask was used, due to the difference in the etching rates between Si oxides and Ti oxides in $(TiO_2)_{1-X}(SiO_2)_X$ residues remaining on the etched surface and thereby the micro-mask effect. In contrast, conventional poly-Si electrode does not show the mask effects on etch rates and surface roughness. This work is helpful to understand the phenomena on etching properties during metal etching under hard mask.

At last, selection of appropriate gate materials is still a main challenge for advanced gate stack formation. The selection of materials in the gate stack is an ongoing research work, and is not determined for future gate stacks. So far, transition metal nitrides have been studied intensively for NMOS application whereas high work function materials have been proposed for PMOS. In this work, new gate metal electrode in the form of transition metal carbide will be proposed and demonstrated for NMOS in chapter

5. These proposed transition metal carbides for NMOS allow easy of fabrication, good thermal stability, and stable V_{th} performance. Therefore, it offers a new option for metal selection. Finally, the thesis is completed with summary and conclusions in Chapter 6.

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CHAPTER 2

Investigation of Etching Properties of Metal-nitride / High-K Gate Stacks Using Inductively Coupled Plasma

2. 1 INTRODUCTION

Poly-Si electrode / SiO_2 dielectric gate stacks have predominantly been used for complementary metal-oxide-semiconductor (CMOS) integrated circuit technology. However, the aggressive scaling of channel length and SiO_2 thickness in recent years has exacerbated the problems of increased leakage current, poly-Si gate depletion, and boron penetration into the channel region. To overcome these problems, extensive studies to replace SiO_2 / poly-Si with high-K dielectric / metal electrode have been carried out [2.1]. On the etching of TaN / Ta and Al / TiN metal stacks [2.2-2.4] using high density plasmas, one of the main problems reported is the low etching selectivity of the materials to the photoresist mask and underlying dielectric materials. In addition, the etching process creates anomalous edge roughening, notching, and generation of non-volatile

residues which are problematic issues for the fabrication of sub-100 nm feature devices. In addition to etching of metal electrode, etching resides as well as subsequent cleaning process is remaining challenge.

In this work, etching properties of metal electrode (TaN, TiN and HfN as promising metal gates [2.5 – 2.11]) / high-K dielectric gate stacks are discussed. In addition, angle resolved x-ray photoelectron spectroscopy (XPS) was used to analyze etching residues on both the etch front and sidewall of gate stacks. On the other hand, high selectivity of metal etching over underlying high-K dielectrics is one of the challenging issues. Various approaches using the oxygen addition and bias control are made to obtain high selectivity of metal etching over underlying high-K dielectrics. Furthermore, the etching properties using the conventional photoresist (PR) and SiO_2 hard masks are investigated.

2. 2 EXPERIMENTAL DETAILS

The experiments were performed in an inductively coupled plasma (ICP) source; details of the ICP equipment are described elsewhere [2.11]. In contrast to electron cyclotron resonance (ECR) and helicon plasma sources, ICP source does not need a magnetic filed for efficient power coupling. An inductive plasma power source produces a high ion density in the chamber. Etching was performed using Cl_2 / HBr / O_2 with a source power of 400 W, a bias voltage of -200 V_{dc}, and a pressure of 10 mTorr. The metal nitride electrode of TaN, TiN, and HfN and the gate dielectric of SiO_2 and HfO_2 were prepared. All the metal nitride electrodes were deposited by reactive sputtering. SiO_2 film was grown on the Si wafer and HfO_2 film was deposited on the Si wafer by atomic layer deposition (ALD). The films were patterned by photoresist and the etch rates were

determined using a surface profiler after etching. The photoresist was subsequently removed by acetone in an ultrasonic cleaner and the etch rates of dielectric films were measured using an ellipsometry. Optical emission spectroscope (OES) technique was used to estimate ion densities in the plasma, detect endpoint signals, and confirm the presence of by-products in the plasma. The ion current density J_i was estimated using the equation (2-1) [2.4],

$$J_i = \frac{P_b}{V_{dc} \times S} \tag{2-1}$$

where P_b is the bottom power, V_{dc} is the self-bias voltage and S is the surface area of the wafer. The self-bias voltage (V_{dc}) developed on the conductive areas of the substrate holder was measured through the matching network between the electrode and radio frequency (RF) power supply. In this work, the self-bias voltage is assumed to be equivalent to the energy of ions impinging onto the wafer.

Metal gate stacks consisting of 70nm hard mask (SiO_2) / 100nm metal nitride (TaN, TiN, and HfN) / 6nm HfO_2 / Si wafer or PR mask / bottom anti-reflective coating (BARC) / 150nm metal nitride (TaN, TiN, and HfN) / 6nm HfO_2 / Si wafer were fabricated to study the effect of different masks on etching properties. After etching, the profile was analyzed using a cross-sectional scanning electron microscope (SEM). For the X-ray photoelectron spectroscopy (XPS) analysis of residues remaining on the etch front and gate stack sidewalls after etching, the substrate was tilted to align at 45 ^{o} or 30 ^{o} toward the electron energy analyzer as shown in Fig. 2.1. For the surface roughness measurement, atomic force microscopy (AFM) was used with the tapping mode and data

were acquired on 1μm / 1μm frames. Dilute hydrofluoric acid (DHF) was used for wet cleaning process.

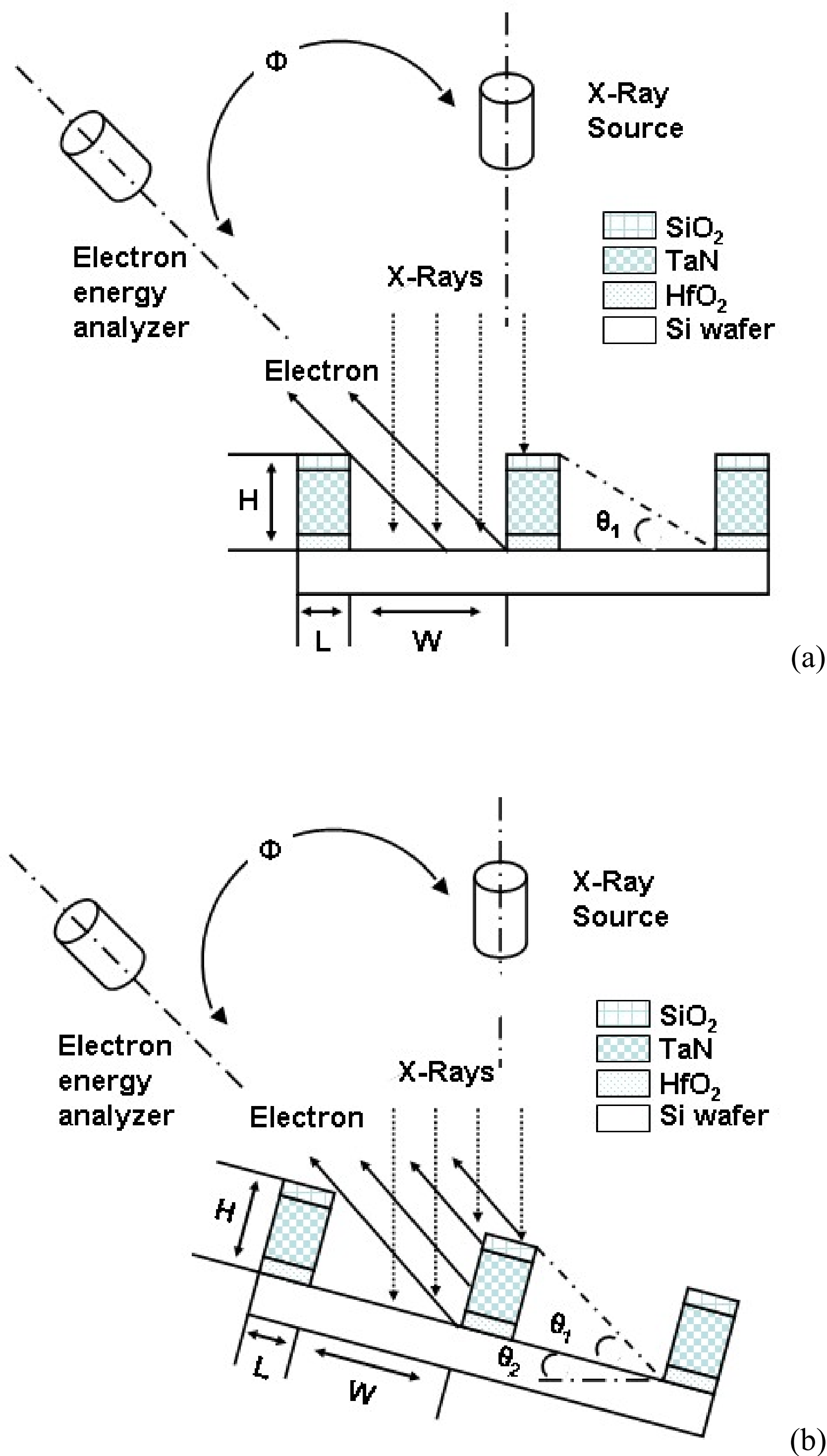
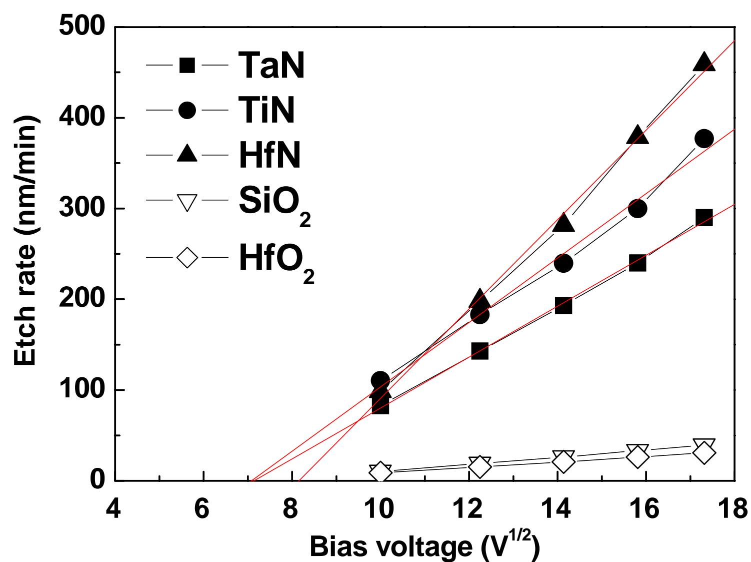


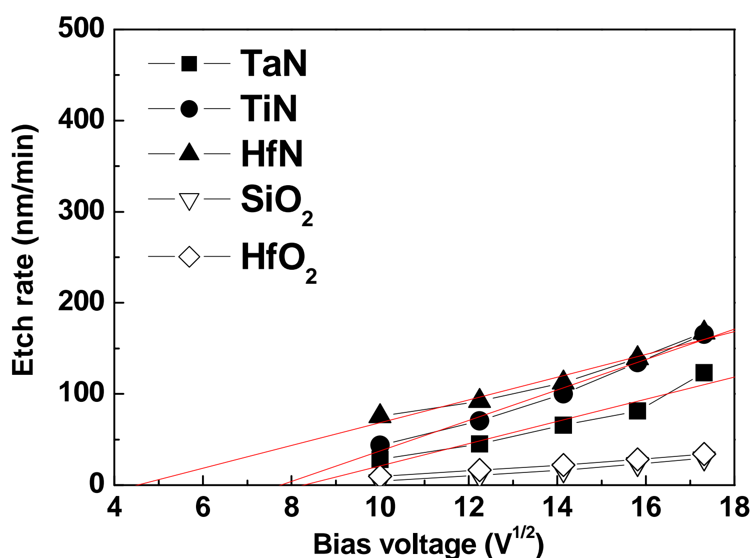
Fig. 2.1 Schematic illustration of the XPS experiment: The substrate is tilted to adjust the electron energy analyzer: (a) 45 º and (b) 30 º. H: 150±20nm, L: 100±10nm, W: 250±50nm.

2.3 RESULTS AND DISCUSSION

2.3.1 Etch Rates versus Bias Voltage



(a)



(b)

Fig. 2.2 Etch rates of metal nitrides and dielectrics as a function of square root bias voltage in (a) Cl_2 and (b) HBr. The experiments are performed at a pressure of 10mTorr and a source power of 400W.

Figures 2.2 (a) and (b) show that the etch rates of metal nitrides are dependent on ion bombardment. The etch rates of all the metal nitrides (TaN, TiN, and HfN) vary linearly with the square root of the bias voltage, which are characteristic of the ion-induced etch mechanism [2.12], $Y = A(E^{1/2} - E_{th}^{1/2})$, where Y is the etching yield, A is the proportionality constant, E is the ion energy, and E_{th} is the threshold ion energy. On the other hand, the magnitude of the etch rates tends to be determined by various factors such as the internal binding energy of substrate, evaporation temperature, and Gibb's free energy of formation (ΔG_f^o) of by-products. The etch rate of TiN is higher than that of TaN. This is attributed to the lower binding energy of TiN (476 kJ/mol, compared to 611 kJ/mol for TaN) as well as the lower evaporation temperature of the $TiCl_4$ by-products (136.4°C, compared to 242°C for TaN). However, the etch rate of HfN is the highest among the films at all bias voltages in HBr and high bias voltage in Cl_2, although the binding energy of HfN (536 kJ/mol) and the evaporation temperature of $HfCl_4$ by-products (317°C) are high. This can be explained by the lower Gibb's free energy of formation of volatile $HfCl_4$ by-products, compared to that of volatile $TaCl_5$ or $TiCl_4$ by-products, as listed in Table 2.1 and it is known that the probability of ion-enhanced chemical reaction is determined by the heat of chemical reaction under ion bombardment [2.15]. It represents that the probability of chemical reaction (etching) for HfN is high compared to that for TaN or TiN, it can lead to the highest etch rate of HfN even though binding energy of HfN and evaporation of HfN byproduct is high compared to that of TaN or TiN. For the metal nitrides investigated in this work, the etch rates in Cl_2 are higher than those in HBr. This can be explained by the higher volatility, which is related to the lower evaporation temperatures of metal-chlorides (242°C for $TaCl_5$, 136.4°C for $TiCl_4$, and 317°C for $HfCl_4$) compared to those of metal-bromides (349°C for $TaBr_5$, 230°C for $TiBr_4$, and 322°C for $HfBr_4$). In addition, the lower ΔG_f^o of volatile chlorides

($TaCl_5$, $TiCl_4$, and $HfCl_4$) than volatile bromides ($TaBr_5$, $TiBr_4$, and $HfBr_4$) supports the high etch rates of the metal nitrides in Cl_2 compared to those in HBr. The etch rates of the metal nitrides in HBr show a similar trend with those in Cl_2.

Table 2.1 Thermodynamic data of reaction of various etch products and residues that can be generated by etching the metal nitride films in Cl_2 / HBr / O_2 plasma [2.13].

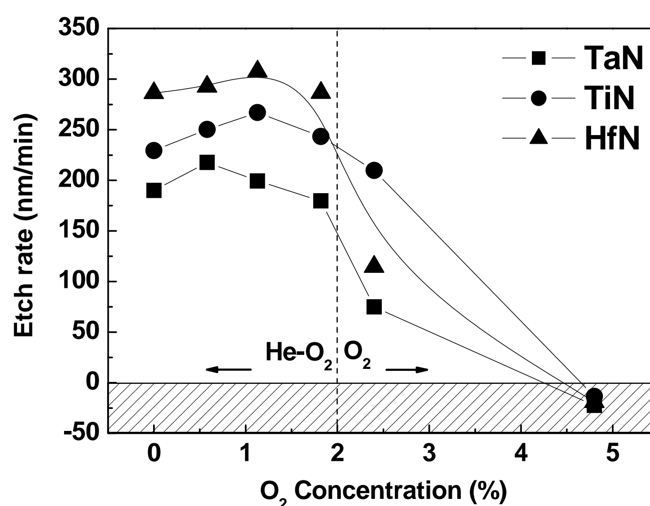
	Cl_2 / O_2				HBr / O_2			
	Volatile etch products		Non-volatile residues		Volatile etch products		Non-volatile residues	
	Reaction	ΔG_f^o (kJ/mol)	Reaction	ΔG_f^o (kJ/mol)	Reaction	ΔG_f^o (kJ/mol)	Reaction	ΔG_f^o (kJ/mol)
TaN	TaCl [g] $TaCl_2$ [g] $TaCl_3$ [g] $TaCl_4$ [g] $TaOCl_3$ [g] $TaCl_5$ [g]	328.160 -77.011 -313.170 -540.657 -748.318 -709.287	$TaCl_{2.5}$ [s] TaO_2Cl [s] $TaCl_3$ [s] $TaOCl_3$ [s] $TaCl_4$ [s] $TaCl_5$ [s] Ta_2O_5 [s]	-425.488 -968.390 -480.010 -802.599 -613.663 -746.410 -1911*	$TaBr_5$ [g]	-493.885	$TaBr_5$ [s] Ta_2O_5 [s]	-547.070 -1911*
TiN	$TiCl_4$ [g] $TiCl_2$ [g] $TiCl_3$ [g] TiOCl [g] $TiOCl_2$ [g] TiO_2 [g]	-726.764 -244.529 -524.829 -249.944 -535.028 -312.660*	TiO A [s] TiO B [s] TiO_2^R [s] TiO_2^A [s] Ti_2O_3 A [s] Ti_2O_3 B [s] Ti_3O_5 A [s] Ti_3O_5 B [s] Ti_4O_7 [s] $TiCl_2$ [s] $TiCl_3$ [s]	-513.278 -421.919 -889.406 -883.266 -1433.824 -1384.095 -2317.294 -2245.626 -3213.016 -465.823 -654.451	$TiBr_2$ [g] $TiBr_3$ [g] $TiBr_4$ [g] TiO_2 [g]	-216.618 -404.708 -569.116 -312.660*	TiO A [s] TiO B [s] TiO_2^R [s] TiO_2^A [s] Ti_2O_3 A [s] Ti_2O_3 B [s] Ti_3O_5 A [s] Ti_3O_5 B [s] Ti_4O_7 [s] $TiBr_2$ [s] $TiBr_3$ [s] $TiBr_4$ [s]	-513.278 -421.919 -889.406 -883.266 -1433.824 -1384.095 -2317.294 -2245.626 -3213.016 -383.187 -525.596 -590.646
HfN	$HfCl_2$ [g] $HfCl_3$ [g] $HfCl_4$ [g]	-326.546 -636.760 -850.774	HfO_2 A [s] HfO_2 B [s] $HfCl_4$ [s]	-1088.280 -796.350 -901.169	$HfBr_4$ [g]	-678.043	HfO_2 A [s] HfO_2 B [s] $HfBr_4$ [s]	-1088.280 -796.350 -734.703

- A: alpha, B: beta, ^{A}: Anatase, ^{R}: Rutile
- * [2.14]

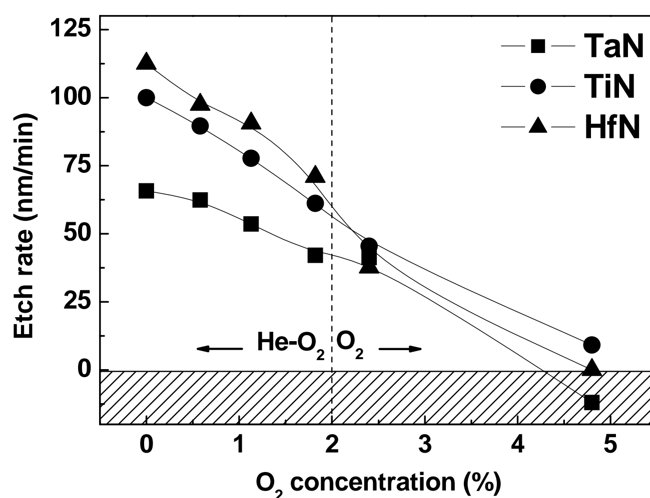
2.3.2 O_2 Effects on Etch Rates for High Selectivity

The HBr and Cl_2 plasmas are widely employed for etching process, due to the superior anisotropic profiles and etch selectivity compared to fluorine-based plasmas. It is known that O_2 incorporation into Cl_2 plasma can promote the formation of passivation films of the sidewall [2.16]. In addition, small amounts of oxygen can improve the selectivity of poly-Si over SiO_2 and high-K HfO_2 [2.11, 2.17, and 2.18]. Figures 2.3 (a) and (b) show the etch rates of the metal nitrides as a function of O_2 concentration in Cl_2

and HBr at a total gas pressure of 10 mTorr. The etch rates of dielectrics decrease significantly as O_2 concentration increases even with very low O_2 concentration (less than 1%), while the etch rates of the metal nitrides do not decrease but increase slightly at the same amounts of O_2 concentration in Cl_2.

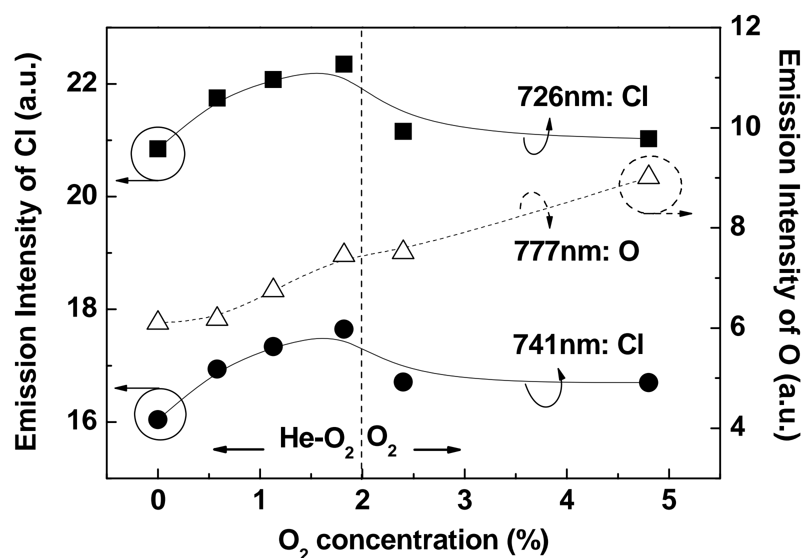


(a)

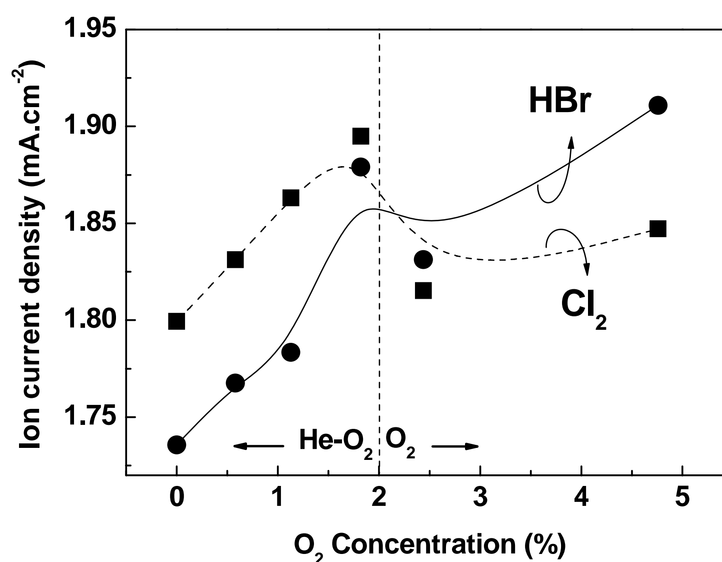


(b)

Fig. 2.3 Etch rates of metal nitrides as a function of O_2 concentration in (a) Cl_2 and (b) HBr. In the range of O_2 concentration less than 2 %, dilute gas of He (80 %) / O_2 (20 %) is used. That is, additional He is incorporated in this range. The experiments are performed at a pressure of 10mTorr, a source power of 400W, and a bias voltage of -200V_{dc}.



(a)



(b)

Fig. 2.4 (a) Optical emission intensity of chlorine as a function of O_2 concentration in Cl_2 plasma. 777nm is for O, and 726nm and 741nm are for Cl (b) Ion current density as a function of O_2 concentration in Cl_2 and HBr respectively. The ion current density is determined by $J_i = P_b / (V_{dc} \times S)$. In the range of O_2 concentration less than 2 %, dilute gas of He (80 %) / O_2 (20 %) is used.

The increase of etch rates can be explained by the increase of atomic Cl concentration, as shown in Fig. 2.4 (a). There have been reports on this increase for etching of poly-Si and Al using high density plasmas with O_2 < 10% in Cl_2 and HBr [2.19 – 2.21]. However, as O_2 concentration increases further, the etch rates of the metal nitrides decrease noticeably. This can be explained by: (1) the enhanced oxidation of metal nitrides, as shown in the Gibb's free energies of oxidation listed in Table 2.1; (2) the re-deposition of metal-oxygen-halogen by-products which can be more stable than metal-halogen by-products, as listed in Table 2.1; and (3) the reduced Cl ion density due to the dilution of Cl_2 when O_2 concentration increases further above 2 %, as shown in Fig. 2.4 (a). In the case of HBr, etch rates of the metal nitrides decrease monotonically as O_2 concentration increases. This may be due to the dominance of re-deposition of metal-oxygen-halogen by-products on the surface after etching in HBr / O_2. It is noted that the addition of O_2 to Cl_2 and HBr resulted in the increase of surface roughness of the metal nitrides, as shown in Fig 2.5.

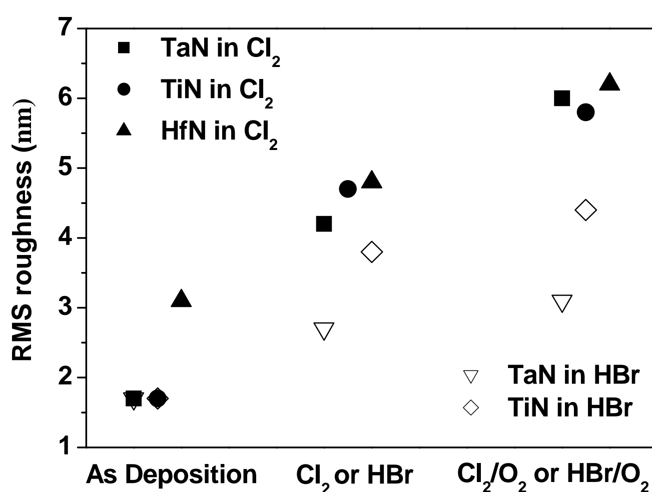


Fig. 2.5 RMS roughness of films before etching and after etching in Cl_2 and HBr. The experiments are performed for 20s, at a pressure of 10mTorr, a source power of 400W, and a bias voltage of -200V_{dc}.

2.3.3 Optical Emission Spectroscopy

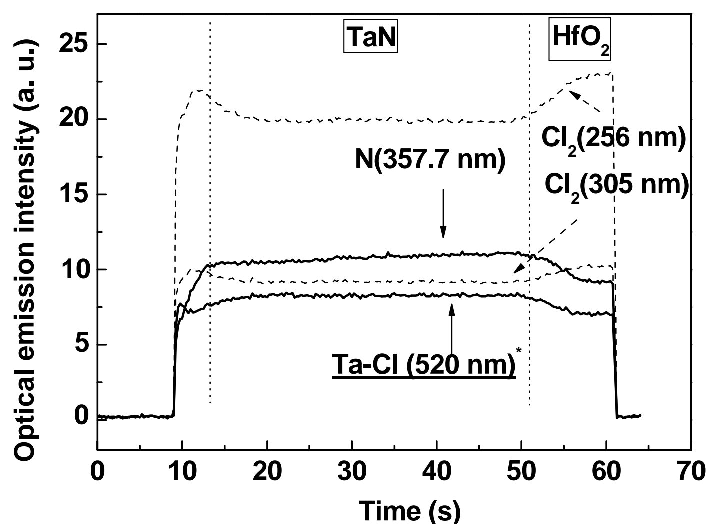


Fig. 2.6 Temporal change of optical emission intensity during TaN / HfO_2 gate etching in Cl_2. 256 nm and 305 nm are for Cl_2, 357 nm is for N, and 520 nm is for Ta-Cl containing byproducts. The experiments are performed at a pressure of 10mTorr, a source power of 400W, and a bias voltage of -200V_{dc}.

When a constant source power is applied to ICP using Cl_2, the emission spectra without substrate and with TaN substrate (no bias power) are almost identical, indicating that no etching by-products are generated with the source power alone. The emission signals in the range of 450 to 800 nm increase with increasing bias voltage, indicating the generation of various TaN etch by-products with the bias voltage applied. Figure 2.6 shows the temporal change in optical emission intensities of N, Cl_2, and Ta-Cl during the etching of the 150 nm TaN / 6 nm HfO_2 / Si substrate gate stack. Here, a wavelength of 520nm is chosen for the endpoint detection of TaN etching, considering industry application, because the 520nm optical emission from CO species is being used widely.

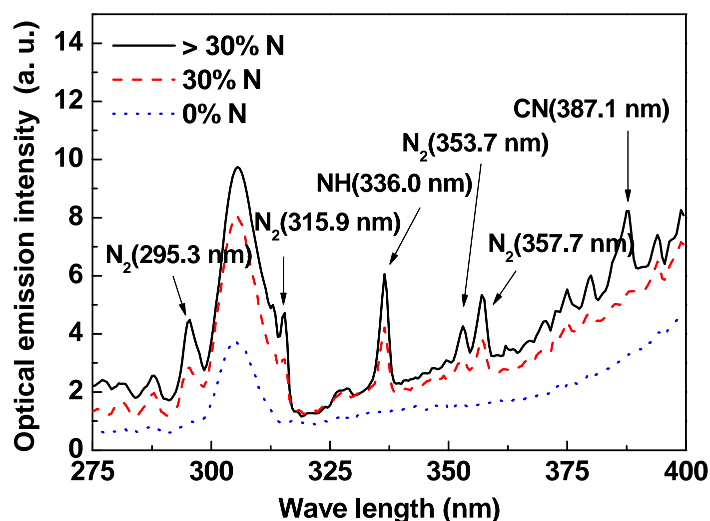
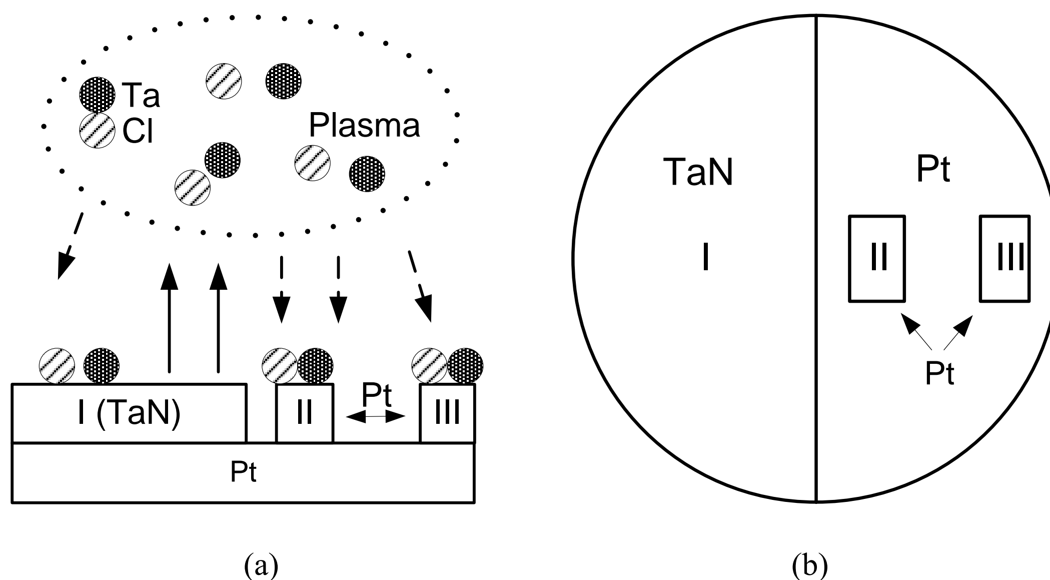


Fig. 2.7 Emission intensities detected during etching of Ta and TaN in Cl_2 at various N concentrations. 295.3 nm, 315.9 nm, 353.7 nm, and 357.7 nm are for N_2, and 336.0 nm is for NH. The experiments are performed at a pressure of 10mTorr, at a source power of 400W, and a bias voltage of -200V_{dc}.

Figure 2.7 shows the difference in by-products generated during the etching of TaN in Cl_2 with different concentrations of N. As the N concentration of the TaN films increases, the intensity of optical emission spectra from N-containing by-products [2.22, 2.23] such as N_2 (295.3 nm, 315.0 nm, 353.7 nm and 357.7 nm) and NH (336.0 nm) increases. It is expected that there are both nitrogen by-products and Ta-Cl by-products in Cl_2 plasma. Optical emission of N-containing by-products is detected at the specific wavelengths, while no optical emission of Ta-Cl by-products has been reported at the specific wavelengths. It is attributed to inherent property of these transition metals having unfilled d-orbits. These unfilled d-orbits involve in complex energy transition, giving off numerous and various photon emissions.



(a) (b)

Fig. 2.8 Schematic diagrams showing the residue formation during TaN etching in Cl_2 with various collection sites. Site I: TaN substrate, Site II: Pt substrate (2 cm away from TaN), Site III: Pt substrate (6 cm away from TaN): (a) side view, (b) top view. Experiments for the residue formation during TiN and HfN etching in Cl_2 were performed by the same method.

Therefore, alternative to OES analysis, other method as shown in Fig. 2.8 was conducted to confirm the presence of Ta-Cl by-products in Cl_2 plasma. In this test, pieces of Pt wafers were placed apart from the metal nitrides to determine etch products that have ended up via plasma, by eliminating the probability of surface reaction from the inert properties of Pt. It is found that Ta and Cl are detected by XPS at all the sites of I, II, and III. These Ta- and Cl- containing residues which remain at the sites of II and III must have been formed through the Cl_2 plasma. This confirms the presence of Ta-Cl by-products in the Cl_2 plasma. The result from HfN shows a similar trend to TaN while the result of TiN shows a different trend from TaN and HfN. Ti is not detected at the sites of II and III by XPS after etching of TiN substrate. This is understood from high volatility [2.24] of $TiCl_4$ compared with $TaCl_5$ or $HfCl_4$.

2.3.4 Residue Analysis by XPS

The XPS analysis is performed *ex-situ*. The samples for XPS analysis are kept in vacuum to minimize the possibilities of the change in chemical compositions of the residues induced by the exposure to air, The Gaussian-Lorentzian curve fitting method is used for XPS data analysis.

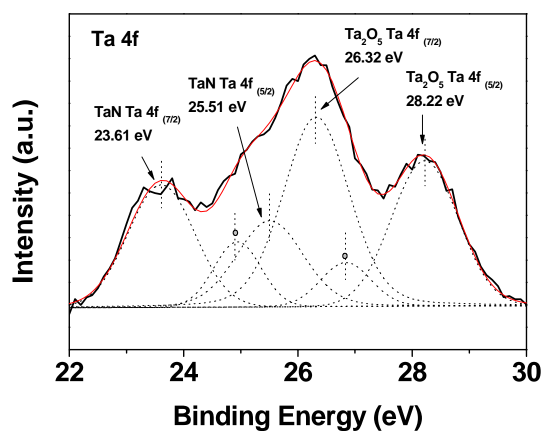
Table 2.2 Composition (atomic %) of residues detected by XPS from SiO_2 / TaN / HfO_2 / Si gate stack after Cl_2 or HBr etching (refer to Fig. 2.1).

	Detection Angle	Ta (4f)	Hf (4f)	Si (2p)	Cl (2p)	Br (3d)	O (1s)	N (1s)
Cl_2	30 º	12.7	0.5	18.3	1.2		43.8	5.4
	45 º	5.6	0.9	30.3	0.7		39.2	2.9
HBr	30 º	21.2	0.7	10.6		1.4	25.3	20.9
	45 º	9.1	0.6	33.5		1.2	26.5	7.7

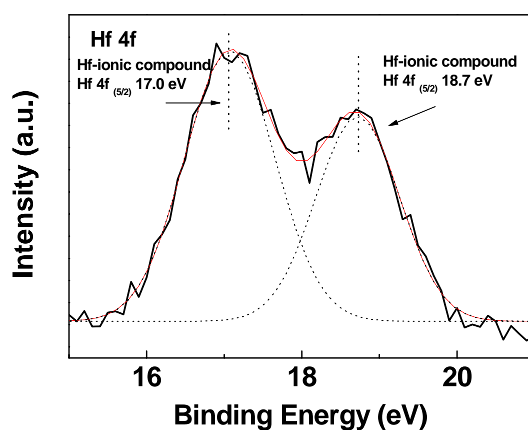
Table 2.2 lists the atomic percentages of residues detected by XPS after Cl_2 or HBr etching of the gate stack, from the two different angles of the electron energy analyzer, as shown in Fig. 2.1. The result shows the remaining chemical components are primarily O and Ta. Cl and Br atoms are detected more on the sidewall than the etch-front surface, indicating that Ta-halogen or Ta-halogen-oxygen compounds remain more on the sidewall. However, peaks of $TaCl_5$ at 27.3 eV [2.25] and $TaBr_4$ at 26.9 eV [2.25] are not detected, perhaps because Ta-oxygen-halogen compounds are more stable than Ta-halogen compounds in Cl_2 as shown in Table 2.1.

Figures 2.9 (a), (b), and (c) show the respective results for the typical *Ta 4f*, *Hf 4f* and *O 1s* peaks, detected from the electron analyzer aligned at 45 º from the surface, as

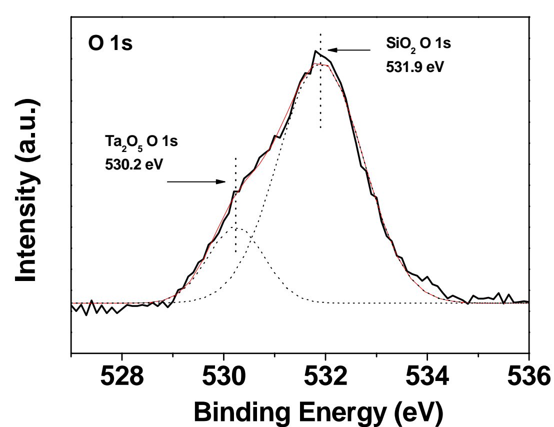
shown in Fig. 2.1 (a). The Ta 4f peak clearly shows two components: one spin-orbit pair corresponds to Ta_2O_5 and the other corresponds to TaN. The observed binding energies for Ta_2O_5 are 26.32 eV (*Ta 4f (7/2)*) and 28.22 eV (*Ta 4f (5/2)*), and the observed binding energies for TaN are 23.61 eV (Ta 4f (7/2)) and 25.51 eV (Ta 4f (5/2)) [2.26]. In addition, the peaks at 24.94 eV and 26.84 eV believed to originate from Ta-Cl-O compounds are observed very weakly. Hf 4f peaks show a sharp doublet due to spin-orbit splitting into the *Hf 4f (5/2)* and *Hf 4f (7/2)*. *Hf 4f (5/2)* has a higher binding energy by 1.7 eV than Hf 4f (7/2) as shown in Fig. 2.9 (b). The peak at 17.0 eV originates from Hf 4f (7/2) of Hf-ionic compounds and this agrees with the results by Gassman *et al* [2.27]. The other peak at 18.7 eV is believed to originate from *Hf 4f (5/2)* of Hf-ionic compounds in $HfCl_x$ or HfO_xCl_y. In the case of the Hf-O bond, the binding energies corresponding to Hf 4f (5/2) and Hf 4f (7/2) are located at 19.5 eV and 17.8 eV, respectively, with a separation of 1.7 eV between the peaks [2.28]. Therefore the peak at 18.7 eV is believed to originate from Hf 4f (5/2) of Hf-Cl compounds, which is separated from the peak of *Hf 4f (7/2)* by 1.7 eV. O 1s shows two peaks in Fig. 2.9 (c). The peak at 530 eV originates from Ta-O [2.29] or Hf-O [2.30]. The peak at 530 eV is understood to originate more likely from Ta-O, because Ta-O bond is confirmed by Ta 4f peak in Fig. 2.9 (a), whereas Hf-O bond is not confirmed by *Hf 4f* peak in Fig. 2.9 (b). The peak at 531.9 eV originates from Si-O which is close to the other reported value from SiO_2 at 532.4 eV [2.31]. From the XPS and etching profile results, it is proposed that the by-products on the sidewall help to attain high anisotropic profiles by forming passivation films.



(a)



(b)



(c)

Fig. 2.9 XPS spectra from the residues on the gate stack after Cl_2 etching (refer to Fig. 2.1 (a)): (a) *Ta 4f*, (b) *Hf 4f*, and (c) *O 1s*.

2.3.5 Etching Metal Nitride / HfO_2 Gate Stack

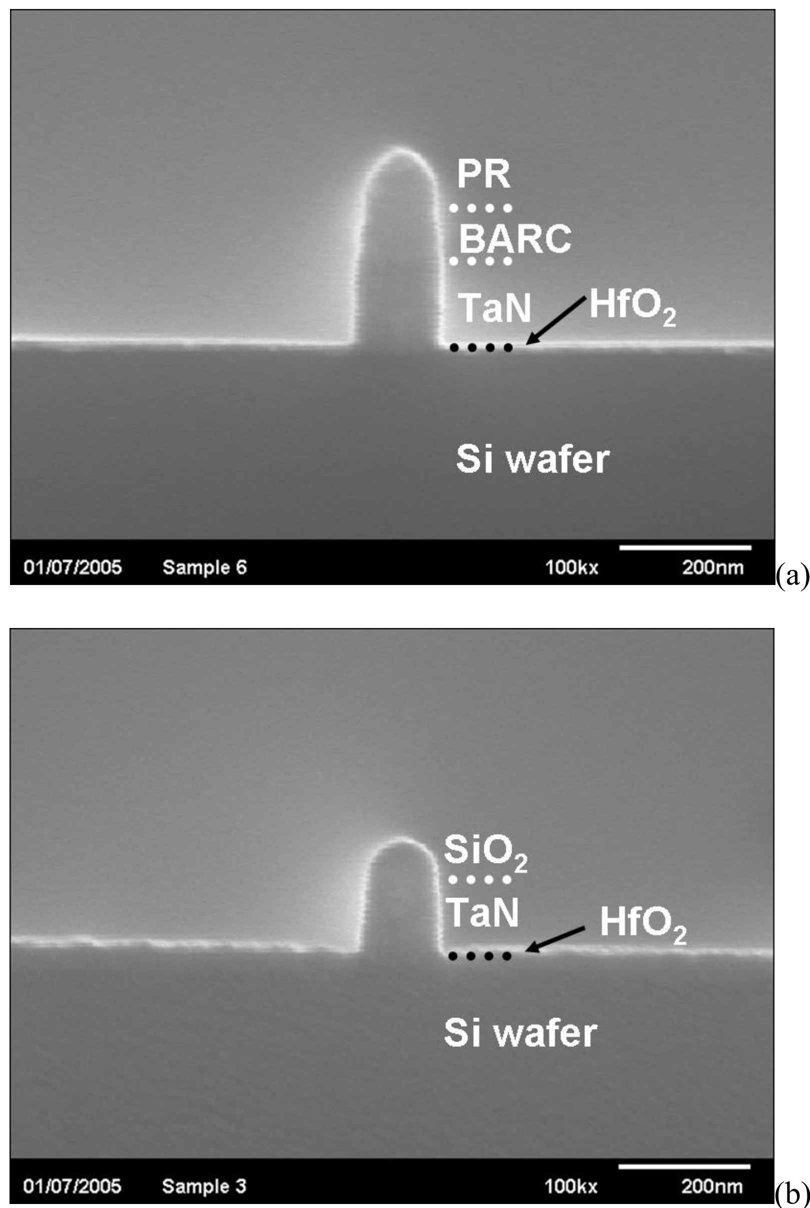


Fig. 2.10 SEM of (a) PR / BARC / TaN / HfO_2 / Si gate stack and (b) SiO_2 mask / TaN / HfO_2 / Si gate stack etched in Cl_2. The experiments are performed at a pressure of 10mTorr, a source power of 400W, and a bias voltage of -200V_{dc}.

Photoresist mask is used in TaN / HfO_2 gate stack as shown in Fig. 2.10 (a). The small amounts of by-products on the surface are detected by SEM after etching in Cl_2. It is believed that these are carbon-based by-products which are evidenced by the *in-situ*

evaporation of the byproducts during exposing them under the focused electron beam of SEM at 10 keV. The amounts of carbon based by-products increased as the area covered by PR increases. Also, the denser the pattern density is, the more carbon-based by-products remain. Furthermore, the addition of a small amount of O_2 results in the formation of a large amount of residues. Figure 2.10 (a) shows that PR mask for metal / HfO_2 gate stack can do away with the need of the hard mask such as SiO_2. However, as patterns become denser and oxygen is added to achieve high selectivity to the underlying dielectric, the advantage of using PR mask is offset by the challenge due to the generation of residues. It will be discussed in the following section.

Figure 2.10 (b) shows the profile of the TaN / HfO_2 gate stack with SiO_2 hard mask. It is found that as the ratio of space to line becomes smaller, micromasking tends to occur more. It is supposed that as pattern density becomes higher, removal rate of by-products decreases, leading to the generation of more residues containing hard mask materials that can result in micromasking. Micromasking is observed even from isolated pattern structures on the HfN / HfO_2 gate stack with SiO_2 hard mask.

2.3.6 Residue Analysis in the Gate Stacks after Metal Etching

Etched surface was investigated as a function of etching time in Fig. 2.11. Agglomerated residues were observed and the amount of residue increase with HfN etching time. The cross sectional images of AFM in the inset show that surface properties were also degraded with etching time. It is believed that the nonvolatile residues generated during etching play a role as a local mask, resulting in increase of surface roughness. It was reported that high selectivity can be achieved with addition of small amount of O_2, which increases the etch rate of metal electrode [2.32] while suppresses the etch rate of dielectrics [2.11]. Figure 2.12 shows the comparison of residues formation

after etching between in (a) Cl_2 and (b) Cl_2/O_2. Agglomerated residues were observed after etching in Cl_2/O_2, indicating that addition of O_2 (1%) enhances residues formation on the etched surface.

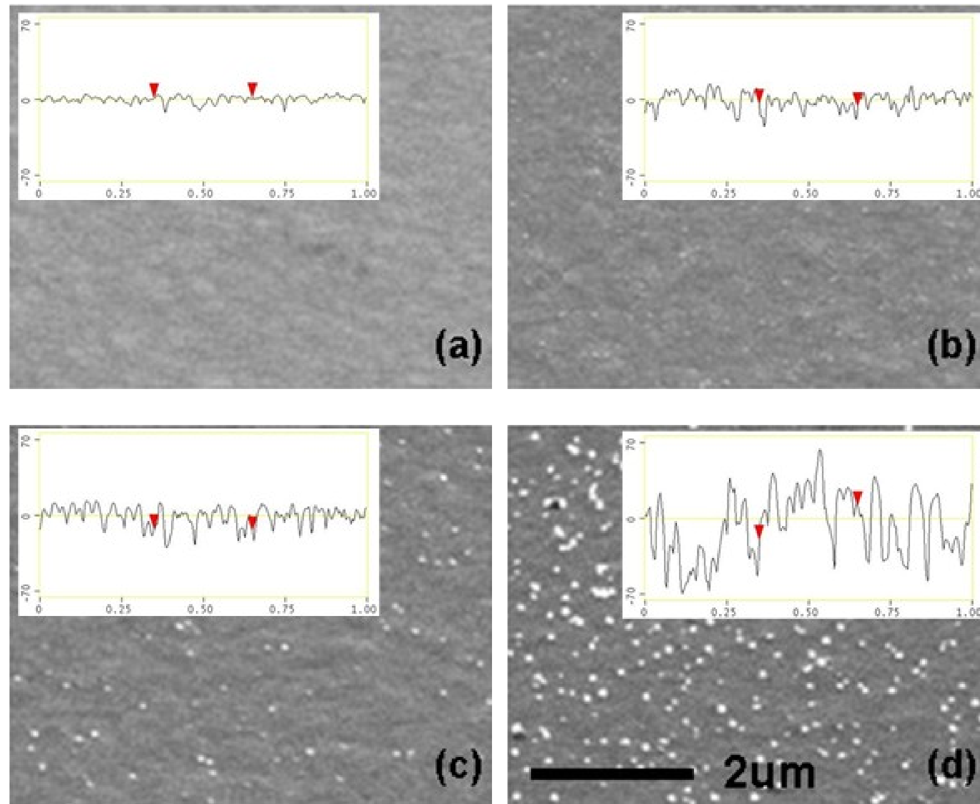


Fig. 2.11 SEM images of etched HfN surface in Cl_2 with etching time; (a) 10s, (b) 15s, (c) 20s, and (d) 25s. The inset shows an evolution of surface topography (height) using AFM with various etching time; X: 0.25 um/div, Y: 70nm/div. The experiments were performed at a pressure of 10mTorr, source power of 400W, and bias voltage of $-200V_{dc}$.

More Cl and O were observed by adding 1% O_2 in Cl_2 and the residues were removed by wet cleaning process. It is expected that the residues generated during etching on the gate stack can be removed by wet cleaning process such as dilute HF. The residues formation as shown in Fig. 2.13 can be correlated to the boiling temperature of the byproducts (239 ^oC for $TaCl_5$, 136 ^oC for $TiCl_4$, and 317 ^oC for $HfCl_4$) which are most favorable phases, according to Gibb's free energy. As expected, the significant amount of

residues were formed on the surface during HfN etching due to high boiling temperature of $HfCl_4$ while no degradation of surface properties was observed during TiN etching due to low boiling temperature of $TiCl_4$.

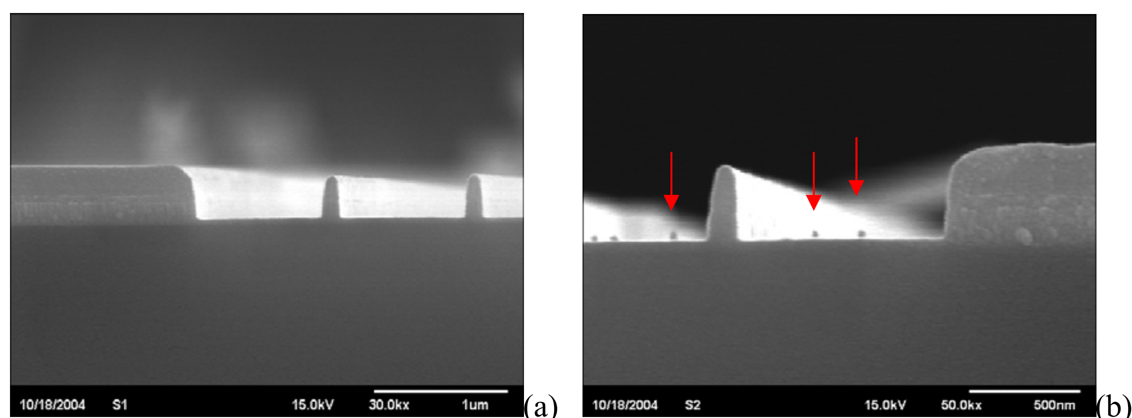
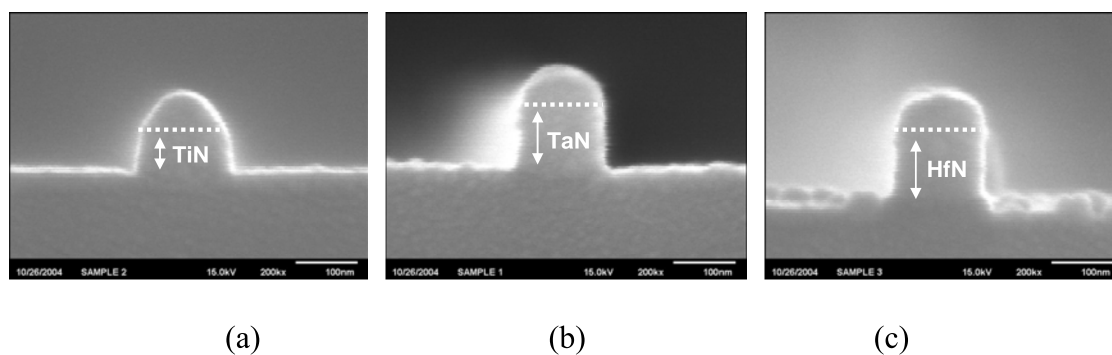


Fig. 2.12 SEM images of TaN gate stack with photoresist masks after etching (a) in pure Cl_2 and (b) Cl_2 / O_2. The experiments were performed at a pressure of 10mTorr, source power of 400W, and bias voltage of -200V_{dc}.



(a) (b) (c)

Fig. 2.13 SEM images of (a) TaN, (b) TiN and (c) HfN gate stack with SiO_2 mask after etching in Cl_2. The experiments were performed in the same condition as shown in Fig. 2.12.

The cross sectional TEM image of TaN metal electrode gate stack after etching is shown in Fig. 2.14 (a). Thick residues were observed on the sidewall of the gate stack after etching. To analyze the residues on the sidewall, angle resolved XPS was done with substrate tilting [2.32] and analysis was performed *ex-situ*. The samples for XPS analysis

were kept in vacuum to minimize the possibility of the change in chemical compositions of the residues induced by the exposure to air. Gaussian-Lorentzian curve fitting method is used for XPS data analysis. Figure 2.15 shows the results of XPS analysis with top view (electron analyzer faces substrate horizontally so only electrons coming from etched surface and top of mask were detected) and side view (substrate was tilt for the electron analyzer to face sidewall of gate so only electrons coming from sidewall of gate stack were detected).

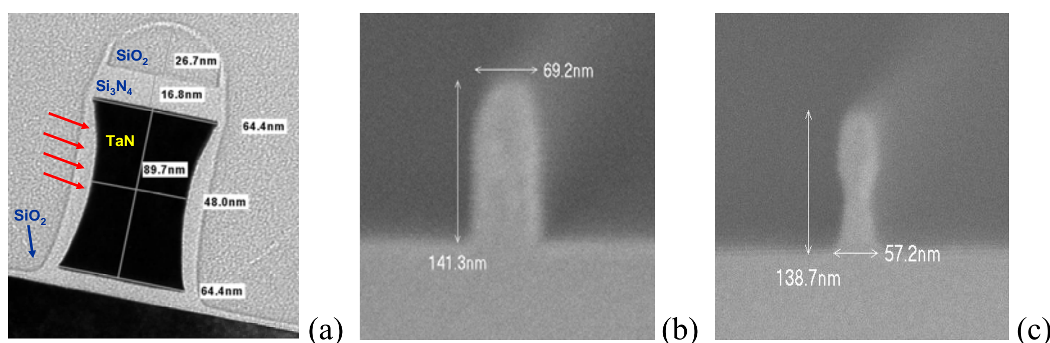


Fig. 2.14 (a) TEM image of TaN metal electrode gate stack after Cl_2 etching, revealing thick residues formation on the sidewall (etching was done in DPS^{TM}); SEM image of TaN metal electrode (b) before and (c) after DHF cleaning.

One strong peak detected at the binding energy lower than the designated Si peak in Figs. 2.15 (a) and (b) is believed to be originated from Si-Ta bond. Peak position of Si will be shifted to lower binding energy when Si reacts with materials showing lower electronegavity (such as Ta at 1.5) than Si (at 1.9). On the other hand, peak position of Si will be shifted to higher binding energy when Si reacts with materials showing higher electronegavity value (such as O at 3.44, N at 3.04, and Cl at 3.16) than Si (at 1.9) [2.33]. Figures 2.15 (c) and (d) show that more oxychlorides residues were observed on the sidewall of the gate than etched surface between gate stack. Since XPS results show that most of the sidewall and etched surface consist of Si-Ta based residues, it is expected that

these residues can be removed by DHF. In fact, Si-Ta based residues are incorporated into passivation films during plasma etching, and this helps to achieve anisotropic profile.

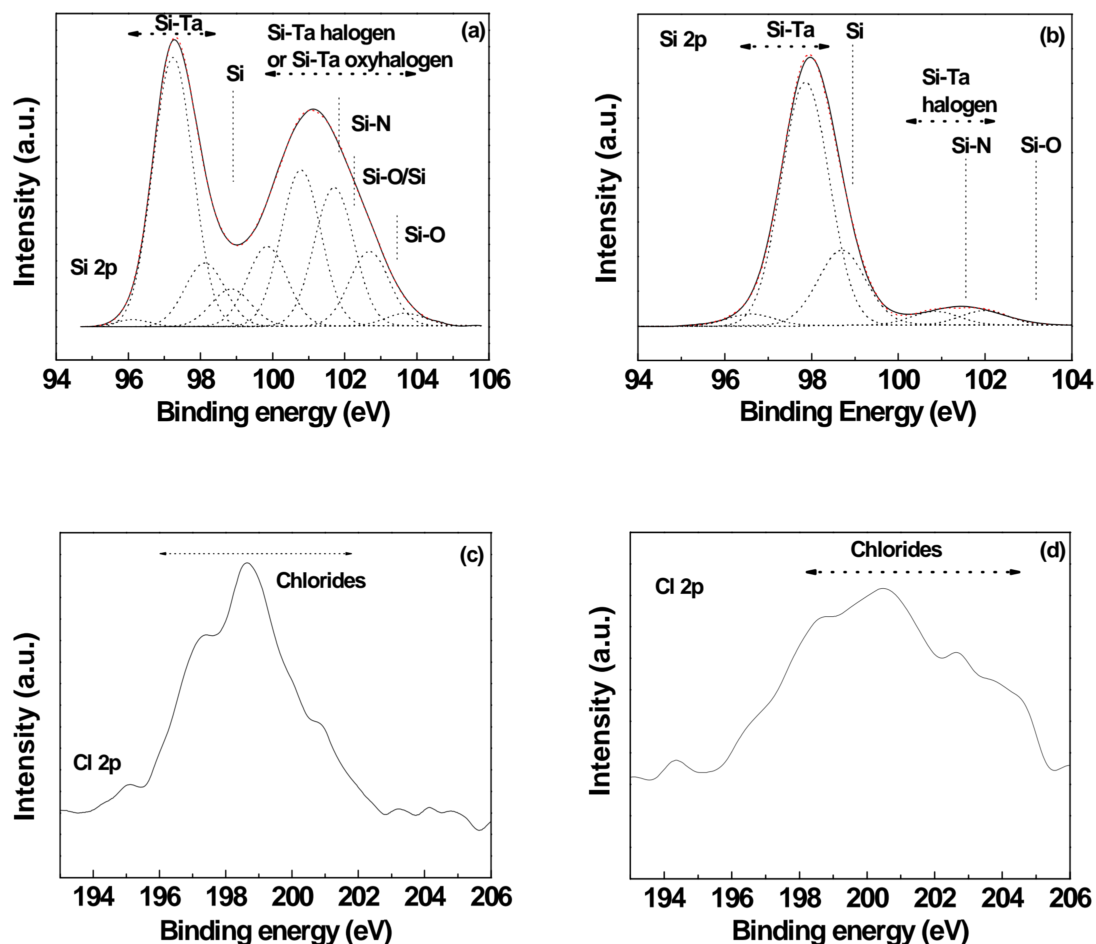


Fig. 2.15 XPS spectra from the residues on the gate stack after Cl_2 etching: (a) and (b) *Si 2p*, (c) and (d) *Cl 2p*: (a) and (c) top view: (b) and (d) side view.

Currently wet cleaning process is an essential step to remove particles and residues generated after plasma etching and megasonic energy helps to remove particles effectively. In this work, DHF is used for cleaning process because DHF is widely employed in the current CMOS fabrication to clean and/or remove remaining residues on the gate stack after plasma etching.

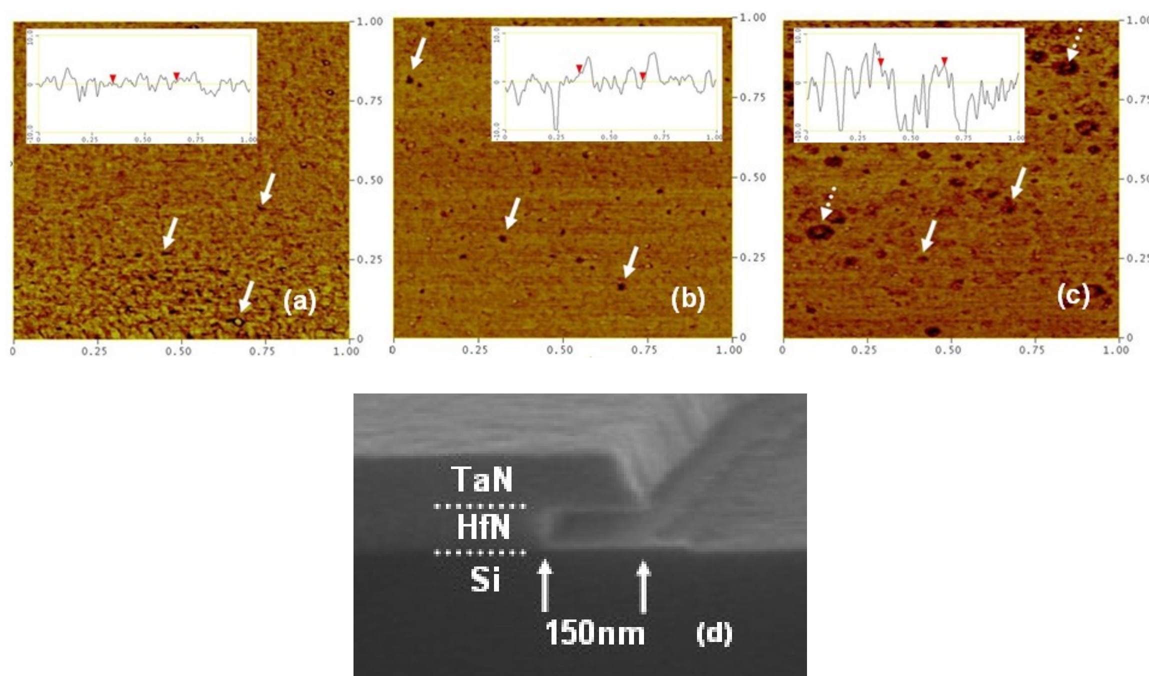


Fig. 2.16 AFM images of etched surface of HfN films after 1% DHF dipping with the time; (a) 5 s, (b) 15 s, (c) 40 s; (d) SEM image of metal gate stack after etching 5min in 1% DHF, showing HfN film is laterally etched.

Figure 2.14 (c) shows that thick residues consisting of Si-Ta have been successfully removed by DHF cleaning; indicating that DHF works effectively also for new metal gate stacks. However, Fig. 2.16 shows that pitting was observed only on the etched surface of HfN. In addition, the pit size increases with cleaning time. It was also found that HfN film can be even laterally etched as shown in Fig. 2.16 (d), indicating that HfN film is highly soluble in DHF.

2.4 SUMMARY

It was found that etching of TaN, TiN, and HfN obeyed the relation of $Y = A\ (E^{1/2} – E_{th}^{1/2})$ for ion-assisted chemical etching. The etch rates of the metal nitrides were higher in Cl_2 than in HBr, and this was due to the difference in volatility between the etching

byproducts of the metal nitrides. Ti-Cl by-products were not detected by XPS on the surface after etching, whereas Ta-Cl by-products and Hf-Cl by-products were detected. It was found that the etch rate results of the metal nitrides agrees well with the thermodynamic data. The addition of O_2 in Cl_2 and HBr resulted in the decrease of etch rates of metal nitrides and HfO_2. However, the slight increase of the etch rates of the metal nitrides were observed when O_2 concentration is less than 1.5 % in Cl_2. The use of O from the addition of O_2 or the use of SiO_2 mask resulted in micromasking of the etched surfaces of metal nitride / HfO_2 gate stacks and thereby increased surface roughness. Most of the sidewall and etched surface consist of Si-Ta based residues after TaN metal gate etching with SiO_2 mask. These residues are incorporated into passivation films during plasma etching so as to help to achieve anisotropic profile. Results of wet cleaning process for new metal gate materials show that DHF is effective for TaN gate, whereas it brings about pit formation on HfN gate.

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CHAPTER 3

Low Energy N_2 Ion Bombardment for Removal of $(HfO_2)_x(SiON)_{1-x}$ in Dilute HF

3.1 INTRODUCTION

The viability of current SiO_2 gate dielectric faces several challenges such as high leakage current caused by direct tunneling current, boron penetration, and low reliability in the thickness regime of 1 to 2nm as devices continue to shrink [3.1, 3.2]. Therefore high-K dielectrics have been extensively studied to replace SiO_2. It is known that HfO_2 meets the several major requirements of material properties such as barrier height, effective tunneling mass, and permittivity to replace SiO_2 [3.3]. Nevertheless, the low crystallization temperature of HfO_2 gives rise to problems such as higher leakage current, lateral nonuniformity associated with grain boundaries, and strong etching resistance in dilute hydrofluoric acid (DHF) [3.4-3.10]. Currently, $(HfO_2)_x(SiON)_{1-x}$ is receiving considerable attention to replace the conventional SiO_2, especially for low standby power device application requiring to maintain low leakage current, since $(HfO_2)_x(SiON)_{1-x}$ shows balanced advantages in terms of crystallization temperature, dielectric constant,

band offset, carrier mobility, thermal compatibility with gate electrode and Si substrate, dopant penetration, gate stack integration and contamination [3.11].

It is obvious that the development of removal processes of high-K dielectrics is crucial for successful integration of $(HfO_2)_x(SiON)_{1-x}$ into the gate stacks. Amorphous Hf-based high-K materials are removed readily in DHF with minimal loss of the underlying Si [3.12, 3.13]. On the contrary, crystallized Hf-based high-K dielectrics show strong resistance in DHF after post-deposition annealing (PDA) [3.14], posing a challenge in their removal at source and drain (S/D) regions of transistors. The PDA process is performed immediately after the deposition for the densification of the high-K dielectrics and the removal of impurities in the film originated from the precursors, because high-K materials are currently formed by either atomic layer deposition (ALD) or metal organic chemical vapor deposition (MOCVD) which uses organic / halogen precursors.

Plasma etching-only-process may be inapplicable to this case, because it tends to generate large amounts of nonvolatile byproducts of Hf-based high-K materials in F, Cl, and Br based halogen plasmas [3.15], introducing unwanted defects such as pin-holes and residual islands. Recently, an ion implantation technique to intentionally damage the high-K dielectrics followed by a wet removal has been introduced, but its mechanism needs to be understood to apply this technique for gate stacks so that inefficiency of the removal of films can be remedied [3.16]. Alternative process schemes, thus, are required to remove the high-K materials at S/D region so as to form shallow junctions or S/D salicides in a controlled manner.

Very recently, ion assisted wet removal has been proposed by several authors [3.17, 3.18]. For the ion assisted wet removal, inert plasma gases with energetic ions, e.g. nitrogen or argon, are used to damage without etching high-K dielectrics. This approach brings about the following advantages: (1) *in situ* plasma treatment is applicable after

spacer formation in the same etch tool; (2) very low kinetic energy (compared to usual ion implantation) is applied from high density plasma species, resulting in controlled degree of structural damage as a function of ion energy and process time; (3) this process brings about high etch rates to the exposed region by causing structural damage, compared to unexposed region, resulting in anisotropic profile without undercutting; (4) advanced metal electrodes and / or conventional poly-Si electrode play a role as a mask for plasma treatment; and (5) the DHF can be used for the removal of high-K dielectrics.

While several works [3.17, 3.18] have been performed on blanket wafers for the purpose of showing the feasibility of the process, device performance that can be obtained from patterned gate stacks remain elusive. Therefore, it is necessary to correlate the properties of ion assisted wet removal with the device performance obtained from patterned gate stacks. In this work, ion assisted wet removal of crystallized $(HfO_2)_x(SiON)_{1-x}$ is discussed. In particular, low ion energy N_2 bombardment is applied to damage the crystallized high-K dielectrics and its mechanism is discussed in detail.

3.2 EXPERIMENTAL DETAILS

$(HfO_2)_x(SiON)_{1-x}$ high-K dielectrics were deposited on p-type Si (100) wafers using co-sputtering of Hf and Si targets in N_2 and O_2, although $(HfO_2)_x(SiON)_{1-x}$ will have likely been deposited by ALD or MOCVD in the future device fabrication, thus, requiring PDA. N_2 plasma, prior to wet etching of $(HfO_2)_x(SiON)_{1-x}$, were performed in an inductively coupled plasma (ICP) system at a source power of 400W, a pressure of 4mTorr, and at room temperature, unless otherwise mentioned. The bias power was varied from 45W to 400W in order to see the ion energy effects. Chemical structures of the dielectrics were analyzed using x-ray photoelectron spectroscopy (XPS) with a

monochromatized Mg *Kα* source on a constant pass energy of 10 eV, while physical structures are analyzed using the grazing incidence x-ray diffraction (XRD) technique. In addition, atomic force microscopy (AFM) was used for surface roughness analysis and secondary ion mass spectrometry (SIMS) equipped with a Cs^+ ion source as a primary beam was used for depth profiling. The $(HfO_2)_{0.6}(SiON)_{0.4}$ was used for the study of ion assisted wet removal and the gate stack of TaN / $(HfO_2)_{0.6}(SiON)_{0.4}$ / Si was used to demonstrate device performance.

3.3 RESULTS AND DISCUSSION

3.3.1 Properties of $(HfO_2)_x(SiON)_{1-x}$

Table 3.1 Wet etching properties of Hf-based high-K dielectrics with dielectric constants and crystallization temperatures. Nitridation also helps to increase crystallization temperature all the cases. * source/drain (S/D) activation annealing at 900°C for 30s.

	Additional elements	High-K materials	Dielectric constants	Crystallization Temperatures (°C)	Etchability in DHF*	References
Hf-based high-K materials	None	HfO_2	20	400	No	[3.4]
	Si	HfSiO	15-25	800, 30min≤	Yes	[3.5]
	Al	HfAlO	13-19	900	Yes	[3.6]
	La	HfLaO	15-25	900	Yes	[3.7]
	Ta	HfTaO	26	1000	Yes	[3.8]
	Ti	HfTiO	50	700	N/A	[3.9]
	Zr	HfZrO	N/A	≤1000	N/A	[3.10]

Although it has been reported that crystallization temperature of HfO_2 can be increased significantly by incorporating additional elements (Table 3.1), the correlation

between the percentage of elements and crystallization for the advanced dielectric materials such as $(HfO_2)_x(SiON)_{1-x}$ remains elusive.

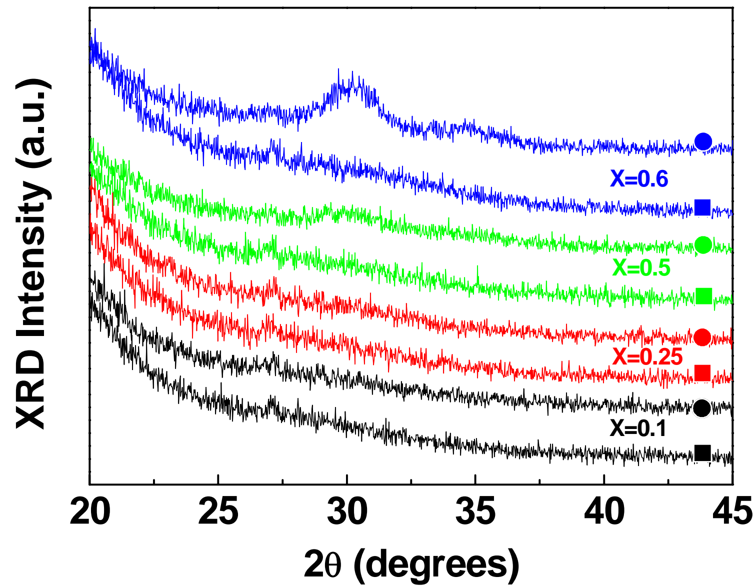


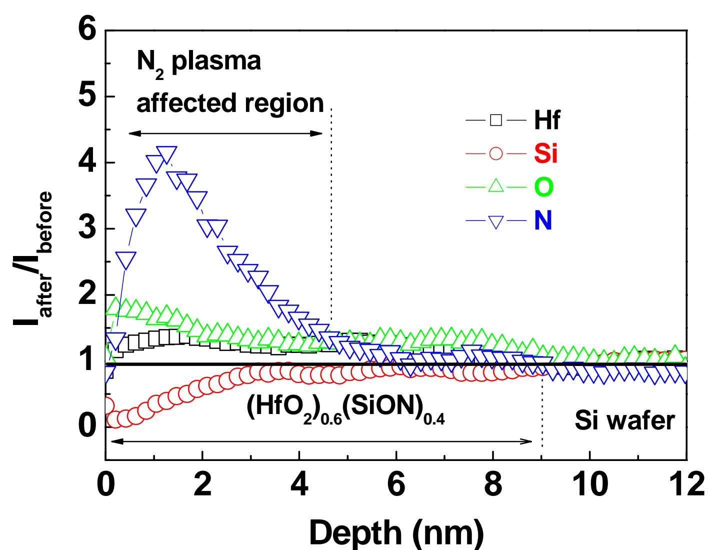
Fig. 3.1 XRD intensity as a function of x in the $(HfO_2)_x(SiON)_{1-x}$; square: as-deposited, circle: annealed at 1000 ^oC for 30 s in N_2 environment, the thickness of the each film is around 9 nm. (The reported crystallization temperature of HfO_2 is around 400^oC and the crystallized HfO_2 at 400^oC is very difficult to be etched away in HF. The degree of crystallite of HfO_2 increases and the more difficult to be etched away, as PDA temperature increases. The reason why the film was crystallized at very high temperature (1000^oC) is to demonstrate the feasibility of ion assisted wet removal clearly at the fully crystallization films.)

Figure 3.1 shows that no XRD peaks associated with crystallization are observed after annealing of $(HfO_2)_{0.1}(SiON)_{0.9}$ and $(HfO_2)_{0.25}(SiON)_{0.75}$ at 1000^oC for 30 s in N_2. It indicates that amorphous property is retained for $(HfO_2)_{0.1}(SiON)_{0.9}$ and $(HfO_2)_{0.25}(SiON)_{0.75}$ after high temperature annealing. This is because of the low percentage of HfO_2 in $(HfO_2)_x(SiON)_{1-x}$. On the contrary, $(HfO_2)_{0.5}(SiON)_{0.5}$ shows peaks corresponding to the monoclinic and tetragonal phases of HfO_2 after annealing at 1000^oC

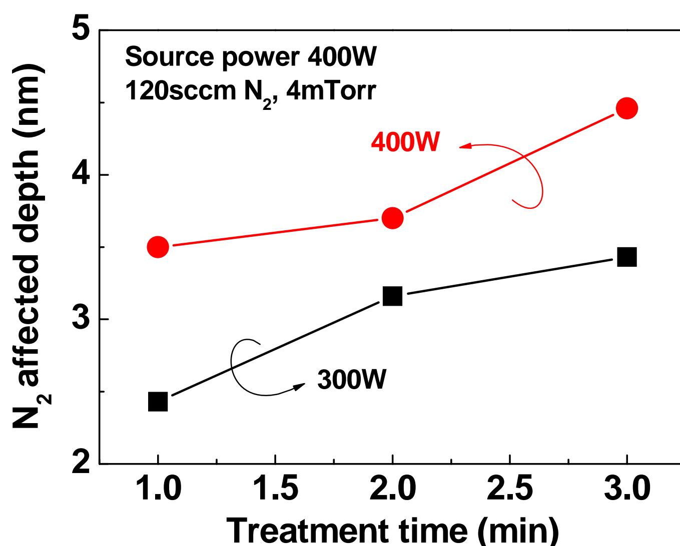
for 30 s [3.19, 3.20]. These peaks are weak and mainly originated from short-range order of crystallization, which is indicative of the formation of very small crystallites. These peaks become more intense for $(HfO_2)_{0.6}(SiON)_{0.4}$, suggesting a higher degree of crystallization. Root mean square surface roughness of $(HfO_2)_{0.6}(SiON)_{0.4}$ increases significantly from 0.076 nm to 0.203 nm after annealing at 1000°C for 30 s in N_2, while surface roughness of $(HfO_2)_{0.1}(SiON)_{0.9}$ changes little from 0.078nm to 0.075nm. It indicates that crystallization of the film can result in degradation of surface roughness. It is understood that amorphous HfO_2 in $(HfO_2)_{0.6}(SiON)_{0.4}$ converts to crystallized HfO_2 during PDA. It is consistent with the previous findings [3.4-3.10], in which crystallization temperature of Hf-based high-K dielectrics increases sensitively by incorporating additional elements such as Si, Al, La, Ta, Ti, Zr, and N into HfO_2 as shown in Table 3.1.

3.3.2 Ion Assisted Wet Removal of $(HfO_2)_x(SiON)_{1-x}$ using N_2 Plasma

Figure 3.2(a) shows the SIMS results on the intensity change (I_{after} / I_{before}) of each component of $(HfO_2)_{0.6}(SiON)_{0.4}$ as a function of depth from the surface before and after N_2 plasma. It reveals that the thickness of the film remains constant and N species are incorporated into the film up to the certain depth by N_2 plasma. Figure 3.2(b) shows the depth affected by N_2 plasma as a function of bias power and treatment time. Note that ion energy is generally proportional to bias power in ICP etching. The results of Fig. 3.2(a) are consistent with those of Fig. 3.2(b). For example, the N incorporated depth by the N_2 plasma is ~ 4.5 nm as revealed by SIMS analysis in Fig. 3.2(a) and the N_2 plasma affected region is ~ 4.7 nm as estimated by film removal rate in Fig. 3.2(b). It suggests that N is incorporated into the film by the N_2 plasma and it causes the damage of the films up to the depth that N is incorporated. The damaged region, consequently, is subjected to the fast removal in DHF.



(a)



(b)

Fig. 3.2 (a) SIMS data showing intensity changes (I_{after} / I_{before}) of atomic percentage of Hf, O, Si, and N on 9 nm $(HfO_2)_{0.6}(SiON)_{0.4}$ on Si substrate before and after the N_2 plasma. It was performed at the source power of 400 W, bias power of 400W for 3 min. (b) N_2 plasma affected depth at various bias power and treatment time. The damaged depth was estimated by the etch rates in 1% DHF, assuming that the initial fast etching of the film within 5 s upon the N_2 plasma is attributed to the amorphous structure. The damaged region of amorphous $(HfO_2)_x(SiON)_{1-x}$ was removed completely in the same condition

Further experiment was conducted; samples were treated by N_2 plasma, followed by annealing in the temperature range of 700°C to 900°C. All the films show strong wet etching resistance in DHF again, despite the incorporation of N species. Therefore it is understood that fast removal of HfSiON is attributed to rupture the crystalline structure by the incorporation of energetic N whereby wet etch will likely proceed preferentially at damaged sties. Figure 3.3 shows etching rates of $(HfO_2)_{0.6}(SiON)_{0.4}$ in DHF before and after the various N_2 plasma. In this work, the thickness is designed to be 3.5 nm as a realistic thickness for CMOS application because the thickness range of 3 - 5 nm is equivalent to EOT of ~ 1 nm as a value required for high performance logic devices as suggested by International Technology Roadmap for Semiconductors [3.2]. It appears that the dielectric before the N_2 plasma shows very strong resistance, while the dielectric is readily removed in DHF after the N_2 plasma. The XRD peaks associated with crystallization become weakened after the N_2 plasma, suggesting that physical structure is changed from crystalline to amorphous. For example, after N_2 plasma the peak intensity of tetragonal HfO_2 at 2θ of 30.1 degrees reduced to 95% and that of monoclinic HfO_2 at 2θ of 28.3 degrees reduced to 45%; there is a limitation on the detection of XRD peak intensities from 3.5nm thick films, which are not as strong as the peaks from 9nm thick films. Therefore, XRD results from 9 nm thick HfO_2 as shown in Fig 3.1 can be used to demonstrate the general trend on crystallization property as a function of composition changes for 3.5nm thick HfO_2 as well. The fast removal of amorphous film is attributed to the intrinsic property of Hf that can be dissolved in HF. Furthermore, results show that Hf, HfN, HfOC as well as amorphous HfO_2 can be etched readily in DHF, being different from crystallized HfO_2. The above results imply that this method can be extended from HfO_2 films [3.18] to other Hf-based high-K dielectric showing low crystallization temperature and thus strong resistance in DHF after PDA.

It is worth noting that the 9 nm thick $(HfO_2)_{0.6}(SiON)_{0.4}$ shows very high wet etching resistance in DHF after high temperature annealing, whereas the 3.5 nm thin $(HfO_2)_{0.6}(SiON)_{0.4}$ show low etch resistance, as shown in Fig. 3.3. The 3.5 nm $(HfO_2)_{0.6}(SiON)_{0.4}$ show 3 different regions (surface, bulk, and interface-layer) before the N_2 plasma. The surface region within the thickness of 0.3 nm and the interface-layer show high wet etching resistance, whereas the ~ 2.0 nm bulk region, the region with the depth range of 0.3 – 2.3 nm, shows the fast wet removal of the film, as shown in Fig. 3.3. This implies that if the top surface is removed and / or damaged by the N_2 plasma, bulk of the film can be readily removed. In other words, the whole wet etching properties of thin $(HfO_2)_{0.6}(SiON)_{0.4}$ could be controlled primarily by the top surface. This can explain why the low bias power N_2 plasma still effective to remove thin film, whereas the same low bias power N_2 plasma is ineffective to remove thick films in DHF.

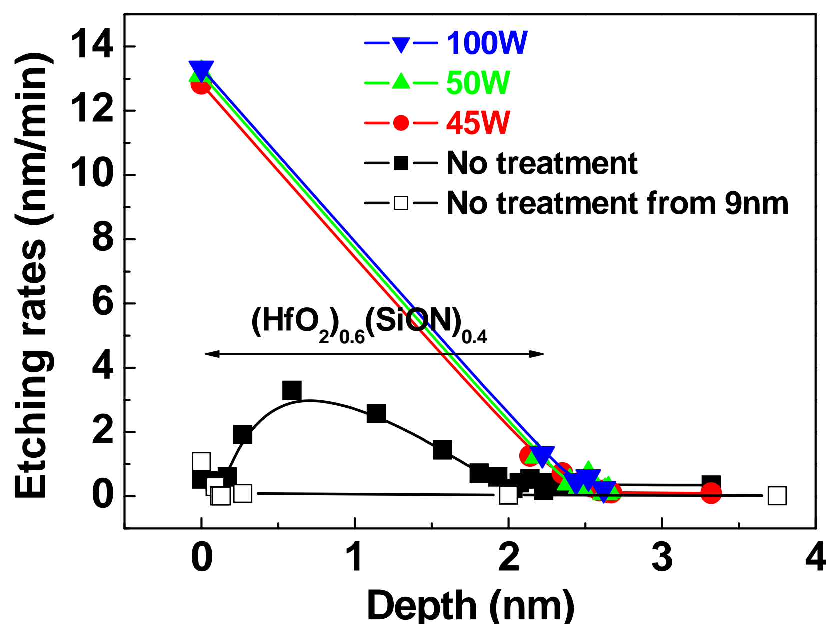
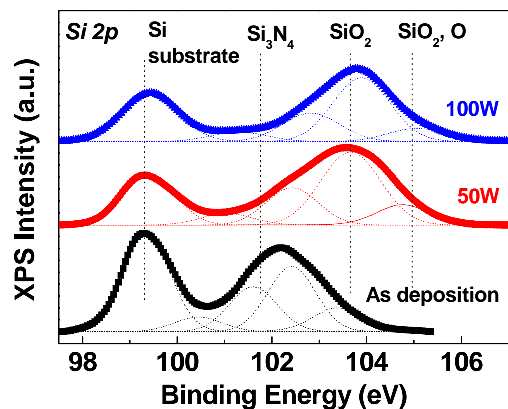
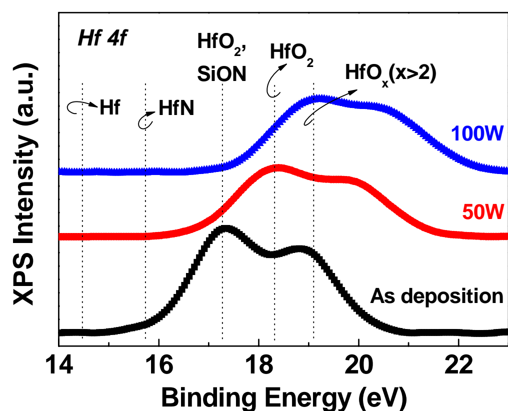


Fig. 3.3 Wet etching rates of the 3.5 nm $(HfO_2)_{0.6}(SiON)_{0.4}$ which was annealed and N_2 plasma was conducted at various bias power for 15 s (wet etching: 1% DHF).

3.3.3 XPS on $(HfO_2)_{0.6}(SiON)_{0.4}$ after N_2 Plasma Treatments



(a)



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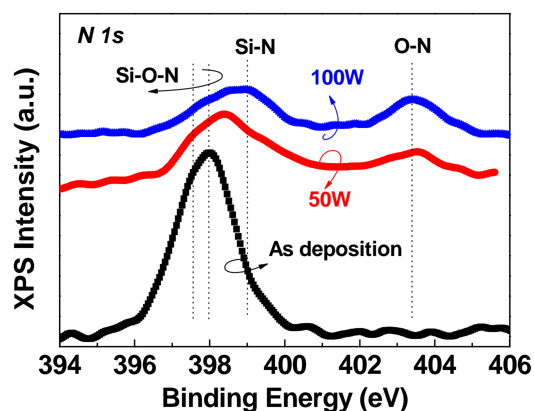


(c)

Fig. 3.4 XPS spectra of (a) *Si 2p*, (b) *Hf 4f*, and (c) *N 1s* from $(HfO_2)_{0.6}(SiON)_{0.4}$. Each of XPS signals is taken before and after the N_2 plasma for comparison.

Figure 3.4 illustrates the changes in chemical bonding of $(HfO_2)_{0.6}(SiON)_{0.4}$ upon the N_2 plasma on (a) *Si 2p*, (b) *Hf 4f*, and (c) *N 1s* by XPS analysis. The *Si 2p* signal before N_2 plasma in Fig. 3.4(a) shows two main peaks; one near 99.3 eV represents Si substrate under the thin $(HfO_2)_{0.6}(SiON)_{0.4}$ and the other near 102.2 eV represents $(HfO_2)_{0.6}(SiON)_{0.4}$ which is close to the binding energy of Si_3N_4. It indicates that there is a significant degree of Si-N bonding in the $(HfO_2)_{0.6}(SiON)_{0.4}$ [3.21]. After N_2 plasma on $(HfO_2)_{0.6}(SiON)_{0.4}$, the main peak associated with $(HfO_2)_x(SiON)_{1-x}$ shifts to higher binding energy near or beyond the energy representing SiO_2. It seems that $(HfO_2)_{0.6}(SiON)_{0.4}$ disintegrates into SiON/SiO_2, and furthermore generates excess oxygen near SiON/SiO_2. It can be explained by the difference of electro-negativity between two elements. If SiON is bonded with HfO_2 like $(HfO_2)_x(SiON)_{1-x}$, binding energy of SiON shifts toward lower binding energy as seen in several sub-peaks from the as-deposition sample; electro-negativity of Hf (1.3) is lower than that of Si (1.8). On the contrary, if SiON is separated from HfO_2 and/or bonded with O/N after N_2 plasma, the binding energy of SiON shifts toward higher binding energy as seen from the samples of the 50W and 100W bias powers; electro-negativities of O (3.5) and N(3.0) are higher than that of Si (1.8) [3.22].

The Hf 4f signal before the N_2 plasma in Fig. 3.4(b) indicates the $(HfO_2)_x(SiON)_{1-x}$ bonding, i.e., Hf-O bonding in the vicinity of SiON [3.23]. In contrast, the peaks shift toward higher binding energy upon the N_2 plasma with a bias power of 50W. It shows that Hf-O bondings are separated from $(HfO_2)_x(SiON)_{1-x}$ bondings. Furthermore, it is found that the peaks shift to even higher binding energy upon the N_2 plasma with a bias power of 100W, indicating that there are excessive oxygen around Hf-O bonding. It is again interpreted that $(HfO_2)_x(SiON)_{1-x}$ bondings are disintegrated into HfO_2 and SiON/ON after the N_2 plasma.

The *N 1s* signal before the N_2 plasma in Fig. 3.4(c) indicates the Si-O-N bonding whose peak can be de-convoluted into several sub-peaks depending on the ratio between Si, O, and N [3.24]. In contrast, after the N_2 plasma, the number of Si-O-N bonds decreases and new O-N bonds are observed. O-N bonds are easily formed, because their chemical bonding strength (1.7 eV) is much smaller than that of Si-N (3.5 eV) [25]. The above XPS results of Figs. 3.4(a), (b), and(c) consistently suggest that the $(HfO_2)_{0.6}(SiON)_{0.4}$ bonding disintegrates into HfO_2 + SiO(N) + ON upon the N_2 plasma treatment.

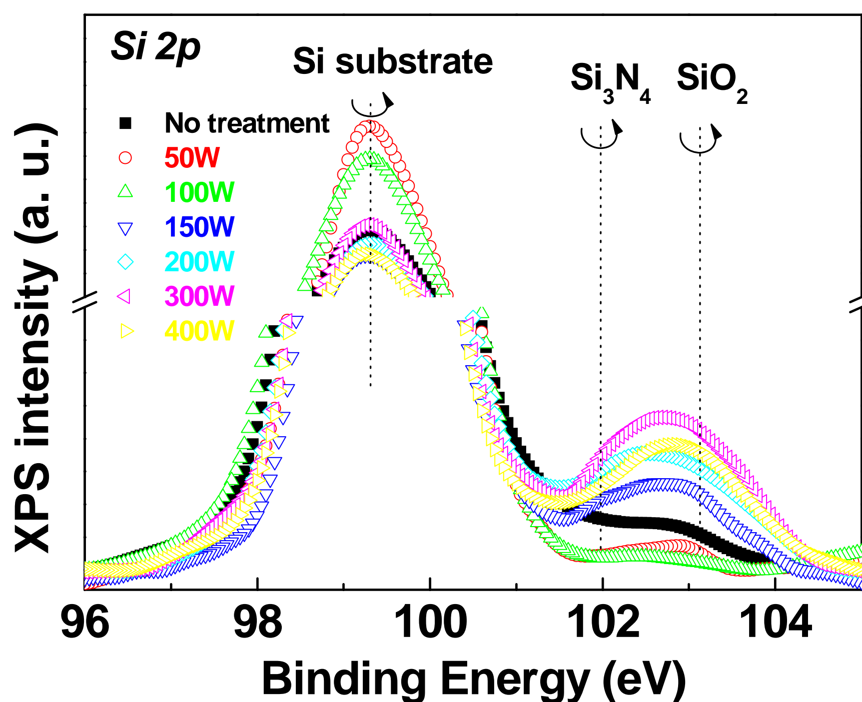
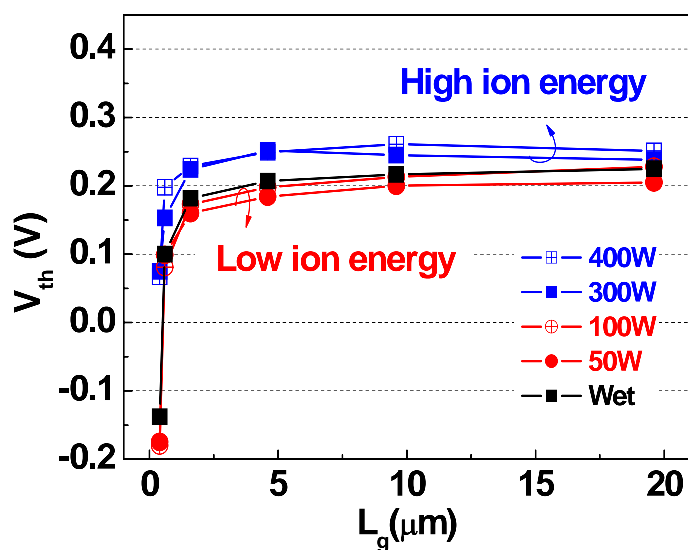


Fig. 3.5 XPS spectra from TaN / $(HfO_2)_{0.6}(SiON)_{0.4}$ / Si gate stack after ion assisted wet removal of $(HfO_2)_{0.6}(SiON)_{0.4}$ using N_2 plasma; initial physical thickness of $(HfO_2)_{0.6}(SiON)_{0.4}$ was 3.5nm. N_2 plasma was generated at various bias powers for 15s, followed by 1% DHF etching for 1 min except the case of no N_2 plasma process which went through in DHF for 20 min.

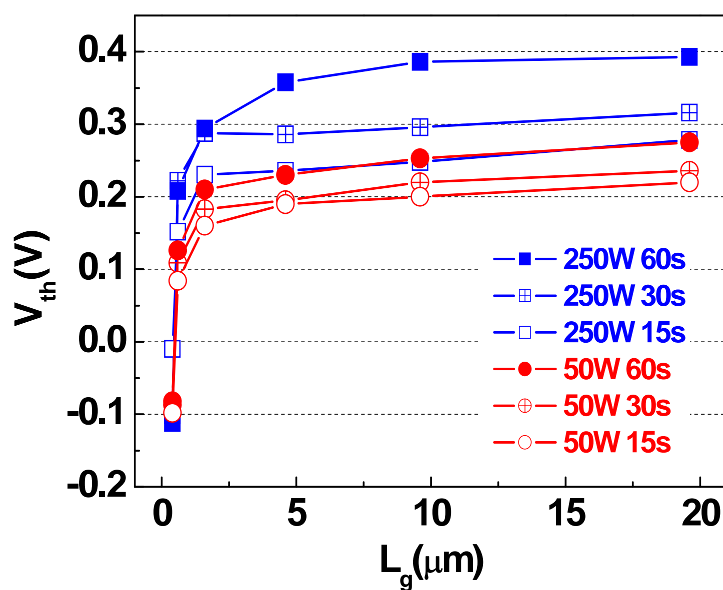
Figure 3.5 shows the XPS intensity upon the various N_2 plasma treatments measured from S/D regions after the removal of the film in DHF. Higher XPS intensity representing the formation of SiON is observed after high bias power N_2 plasma, while no surface nitridation is observed after the N_2 plasma with bias power below 100W. It shows that low bias power is required to avoid surface nitridation on S/D regions. Nitride-like properties also are observed from the surface of S/D region after wet-etch-only process without N_2 plasma, as shown in Fig. 3.5. It may account for the residual dielectric, which has not been completely removed in DHF. The remaining residue on S/D region leads to high series resistances, giving rise to higher threshold voltage (V_{th}) as shown in Fig. 3.6.

3.3.4 Electrical Properties of TaN / $(HfO_2)_{0.6}(SiON)_{0.4}$ / Si Gate Stack

In Figs. 3.6(a) and (b), V_{th} is measured to assess the various removal processes of high-K dielectric. V_{th} is expressed as a function of gate length rather than one point V_{th} at certain gate length. The result indicates that this finding is universal for all the MOS devices using HfSiON gate dielectric and ion assisted wet removal process. V_{th} increases with increasing bias power in Fig. 3.6(a) and process time in Fig. 3.6(b). The increase of V_{th} may result from the surface nitridation on S/D region after the high bias power N_2 plasma, as shown in Fig. 3.5. It is also observed that the wet-etch-only process for 20 min gives rise to higher V_{th}, compared to the process of the low bias power process. It is attributed to higher sheet resistance on S/D region caused by residual dielectrics which has not been removed completely for wet-etch-only process as shown in Fig. 3.5.



(a)



(b)

Fig. 3.6 Threshold voltage (V_{th}) of TaN / $(HfO_2)_{0.6}(SiON)_{0.4}$ / p-Si gate stack as a function of gate length from the various N_2 plasma conditions for high-K wet removal. (a) The N_2 plasma was performed at various bias power for 15s, followed by 1% DHF wet etch. For comparison, the result of the wet-etch-only process is included; it was obtained after dipping in DHF for 20 min, however, the film is not clearly removed as shown in Fig. 6. (b) The N_2 plasma was conducted for various times.

3.4 SUMMARY

This work investigated ion assisted wet removal of $(HfO_2)_x(SiON)_{1-x}$ in dilute HF for the advanced CMOS process. HfO_2-rich $(HfO_2)_x(SiON)_{1-x}$ where x is > ~ 0.5 was crystallized after high temperature annealing. The crystallized $(HfO_2)_{0.6}(SiON)_{0.4}$ was damaged via the incorporation of N species into the film by the N_2 plasma, resulting in the fast removal of the film in DHF. This is attributed to the structural changes of the film from crystalline to amorphous. In addition, the structure of $(HfO_2)_{0.6}(SiON)_{0.4}$ was disintegrated into HfO_2, SiO(N), and ON after N_2 plasma. It was observed that S/D regions were nitrided more by higher bias power and this adversely affected the electrical property of the devices by increasing threshold voltage. The wet-etch-only process in DHF for 20 min also gave rise to high threshold voltage, compared to the low bias power N_2 plasma process, due to high sheet resistance caused by residual dielectric. In conclusion, the efficient ion assisted wet removal process explored in this work can be extended from HfO_2 to other high-K materials showing low crystallization temperature.

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CHAPTER 4

Effects of SiO_2 / Si_3N_4 Hard Masks on Etching Properties of Metal Gates

4.1 INTRODUCTION

The rapid progress in high drive current and high speed in CMOS (complementary metal oxide semiconductor) processing has been driven by scaling down of gate length and thickness [4.1, 4.2]. However, CMOS scaling is about to meet its limitation of direct tunneling as dielectric thickness is reduced to below 1nm [4.3]. It has resulted in the needs for alternative metal electrode / high-K dielectric to replace conventional poly-Si electrode / SiON dielectric in the gate stacks with same design concept [4.3]. Meanwhile, new structures of multi gate transistors, e.g. Fin Field Effect Transistor (FinFET), are considered to replace current planar CMOS device structures due to the advantages in electrical properties such as superior channel control and high on-off current ratio [4.4]. Whether new device structures such as FinFET or conventional planar CMOS structures, introduction of new materials in the gate stacks as well as continuous scaling down brings a lot challenges to meet the requirements of various device performance and low

production cost [4.5]. This also requires various attempts to develop small gate patterning technology [4.6, 4.7]. From these studies, it becomes clear that conventional photoresist (PR) mask is not suitable to form those device structures, primarily due to the low etching selectivity to poly-Si gate [4.8]. Critical dimension (CD) gain was reported during plasma etching due to the sloped profile of PR by erosion, PR swelling, and the re-deposition with PR mask [4.9]. Furthermore, it is known that the presence of PR during poly-Si gate etching tends to decrease etching selectivity of poly-Si electrode with respect to oxide dielectrics [4.8]. Therefore, it becomes evident that hard mask is urgently required to overcome these challenges. Until now, hard masks have been used mainly in the research level, except for some limited application to gate processing of integrated circuit device fabrication, because hard mask shows several advantages over PR mask [4.9, 4.10]; more resistant to the attack or erosion by plasma, better control of gate length, and higher selectivity than PR. It is also worthwhile to note that the surface of plasma reactor can remain clean with hard masks, because there is no polymer build-up originated from PR mask. Even if the use of hard mask can provide significant advantages, it should be noted that extra deposition and etch step are added to the overall process module flow. In addition, in most CMOS process, hard mask needs to be completely removed prior to the subsequent silicidation step on top of poly-Si gate electrodes. During the removal of hard mask, unwanted erosion of shallow trench isolation (STI) and sidewall spacers should be avoided as well as notching of gate dielectrics. Therefore, for the selection of hard mask, highly selective removal of hard mask technique against gate dielectrics, STI, and sidewall spacers is required.

Meanwhile metal electrode is being extensively studied to replace poly-Si electrode in the gate stacks. The introduction of both hard mask and metal electrode in the gate stacks poses new challenges in etching process, because nonvolatile byproducts are

generated more during the etching of most metals than poly-Si, and the etch rates of metal are lower than that of poly-Si. Etching properties of poly-Si with hard mask are well understood [4.8] whereas etching properties of metal with hard mask have been hardly discussed [4.10]. *Aoki et al.* reported that selectivity of Al electrode with respect to underlying SiO_2 is higher with SiO_2 hard mask than with PR mask due to the lack of a carbon source in the plasma [4.11]. In addition, the suppression of the microloading and the CD shift was reported with SiO_2 hard mask processing [4.11]. In this work, hard mask effects on advanced metal gate stack etching are addressed.

4.2 EXPERIMENTAL DETAILS

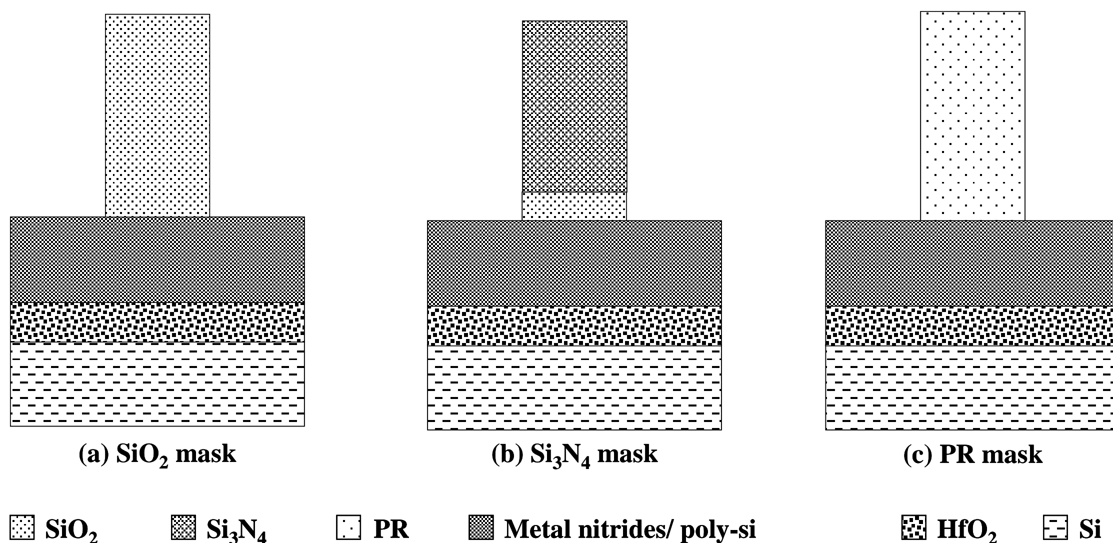


Fig. 4.1 Gate stacks of metal nitrides (TaN, HfN and TiN) or poly-Si / HfO_2 / Si wafer with (a) SiO_2, (b) Si_3N_4, and (c) PR masks; thin SiO_2 layer is inserted between Si_3N_4 mask and TiN to enhance adhesion under Si_3N_4 mask in (b). The thickness of SiO_2 (a) is 100nm, 100nm for Si_3N_4 (b), and 1000nm for PR (c) for each structure.

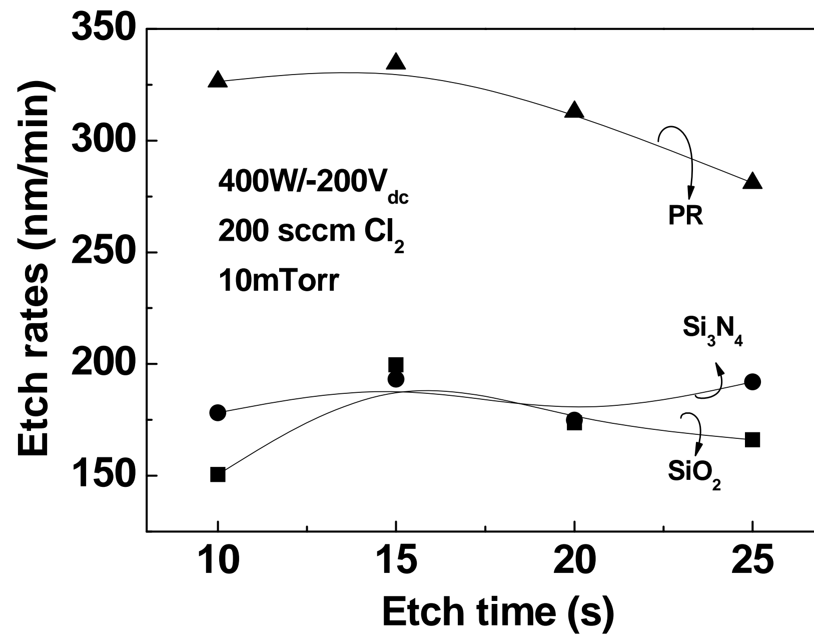
Metal nitrides (TaN, HfN and TiN) and HfO_2 were deposited by reactive sputtering and poly-Si was deposited by LPCVD. SiO_2 and Si_3N_4 as hard masks were

prepared by plasma enhanced chemical vapor deposition (PECVD). Gate stacks consisting of various masks (SiO_2, Si_3N_4, and PR) / metal nitrides (TaN, HfN and TiN) or poly-Si / HfO_2 / Si wafer were fabricated to investigate etch rates and surface roughness as shown in Fig. 4.1. Additionally, Si oxide and Ti oxide were prepared by reactive sputtering to investigate the effect of metal oxide formed on the etched surface of poly-Si and TiN respectively by the reaction during the plasma etching. X-ray photoelectron spectroscopy (XPS) was performed for the residue analysis on the etched surface. Atomic force microscope (AFM) was used on the etched surface near the mask for roughness measurement with tip radius less than 10nm.

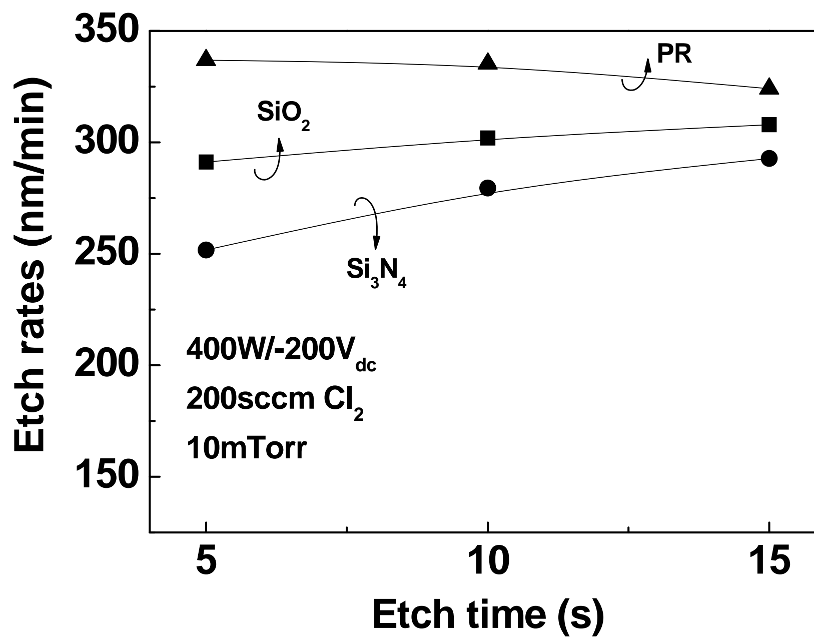
4.3 DETAILSRESULTS AND DISCUSSION

4.3.1 Etch Rates with Hard Masks

TaN, TiN, and HfN [4.12-4.14] have been studied recently as promising electrode candidates to replace poly-Si. It was found that etch rates of those materials were suppressed with hard masks, compared to PR mask. The suppression of etch rate of TiN is more obvious than that of TaN and HfN. It is explained by lower Gibb's free energy of formation of Ti oxide (-3213kJ/mol for Ti_4O_7) than those of Ta oxide (-1911kJ/mol for Ta_2O_5) and Hf oxide (-1088kJ/mol for HfO_2) [4.15]. Furthermore, Gibb's free energies of formation of those oxides are lower than that of SiO_2 (-856kJ/mol) [4.15]. This indicates that etched surface of metal electrodes (especially, for NMOS where chemically active materials are used for low work function) can be more affected than that of poly-Si electrode, in the point of the oxidation of etched surface by the reaction during plasma etching. In this work, etching properties of TiN electrode were examined in detail to understand the mask effect.



(a)



(b)

Fig. 4.2 Etch rates of (a) TiN and (b) poly-Si as a function of etch time for different masks (SiO_2, Si_3N_4, and PR).

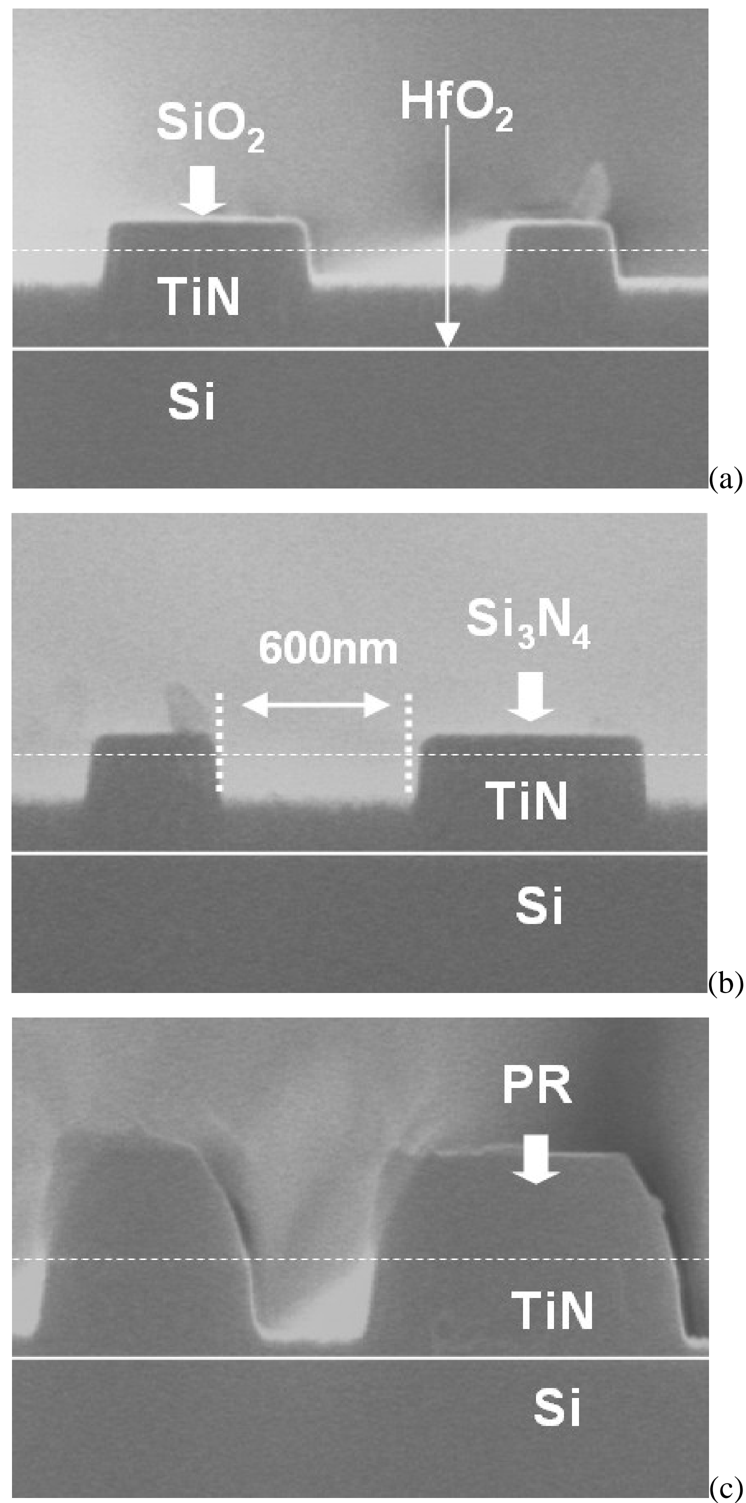


Fig. 4.3 Cross-sectional SEM images of etched TiN gate stacks with different masks; (a) SiO_2 mask, (b) Si_3N_4 mask, and (c) PR mask.

Figures 4.2 and 4.3 show that etch rates of TiN decrease with hard masks (both SiO_2 and Si_3N_4), compared to PR mask. For comparison, etch rates of poly-Si electrode

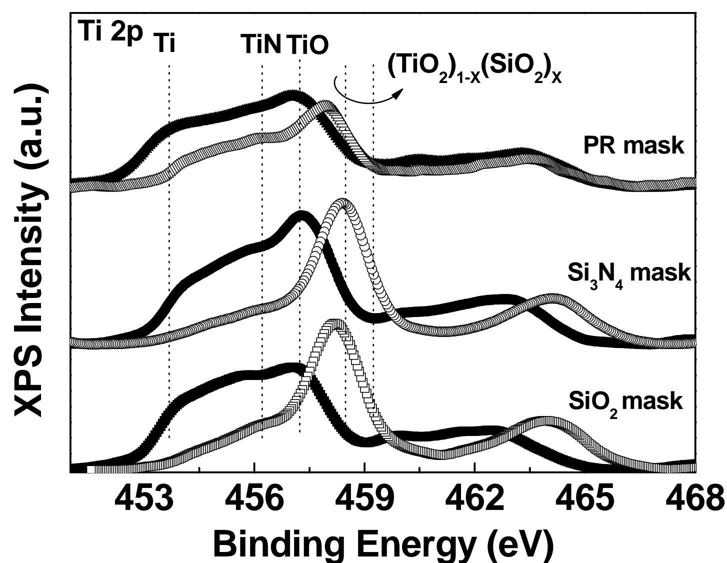
with different masks are shown in Fig. 4.2(b). It is considered that materials, released from SiO_2 and Si_3N_4 hard masks, react with etched TiN surface during the plasma etching, resulting in formation of Ti oxides and / or metal compounds on the etched surface which can be supported by negative Gibb's free energy of formation ($\Delta_f G^o$), e.g. -513kJ/mol for TiO, -945kJ/mol for TiO_2, -1434kJ/mol for Ti_2O_3, -2317kJ/mol for Ti_3O_5, and -3213kJ/mol for Ti_4O_7, -130kJ/mol for SiTi, -132kJ/mol for Si_2Ti, and -581kJ/mol for Si_3Ti_5 [4.15]. The presence of these oxides indicated by ($\Delta_f G^o$) can explain the reduced etch rates with hard masks. The etch rates of Ti oxides have also been measured to investigate the effect of Ti oxide residues on etched surface of TiN. Etch rates of Ti oxides are ~ 46nm/min which is significantly lower than the etch rates of TiN of ~ 340 nm/min. This supports that Ti oxide residues formed on the etched TiN surface suppress the etching of TiN, being different from Si oxides residues formed on the poly-Si.

4.3.2 XPS Analysis for Various Mask Processes

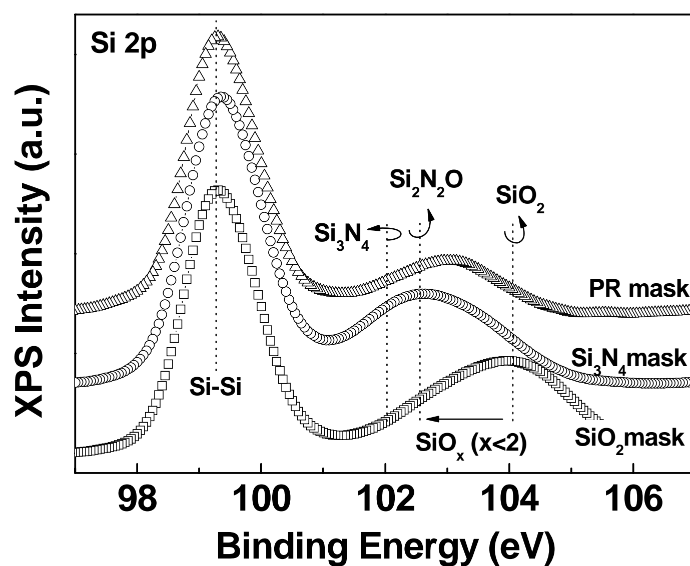
XPS analysis is performed to understand the origin of the suppression of etch rates of TiN with hard masks [4.16]. XPS analysis of TiN gate stacks before etching shows that TiN surface consists of TiN, Ti and Ti oxides as shown in Fig. 4.4(a); the TiO are considered to be formed during the sample delivery. The samples for XPS analysis are stored in vacuum to minimize the change in chemical composition of the residues induced by the exposure to the air during the delivery of the samples. Since all the samples that had undergone etching are stored in vacuum environment with only N_2 and then analyzed together, it is considered that the differences in peak intensity and binding energy reflect the as-etched surface conditions. XPS analysis after etching of TiN gate stacks reveals the following two phenomena. Firstly and qualitatively, the main peak is shifted towards higher binding energy after etching with SiO_2 and Si_3N_4 hard masks, showing that TiN

surface is heavily oxidized in the form of Ti oxides and / or TiSiO compounds after the plasma etching: see Fig. 4.4(a). In contrast, the TiN surface with PR mask is not heavily oxidized as much as TiN surface with hard mask, i.e., mainly TiCCl residues remain on the etched TiN surface. Secondly and quantitatively, Fig 4.4(a) shows that the relatively thick residues of Ti oxides and / or TiSiO compounds are detected with hard mask whereas thin residual films are detected with PR mask on the etched TiN surface. This is induced from the consideration of the escape depth of photoelectrons of *Ti 2p* from TiN. That is, few photoelectrons from TiN are detected due to the thick residual films with hard mask, whereas more photoelectrons are detected from TiN due to the thin residual films with PR mask (it is assumed that mean free path of *Ti 2p* photoelectron is similar in both residue layers). It is interpreted that these residues formed with hard masks suppress the further etching as shown in Fig. 4.2(a) and Fig. 4.3. For comparison, XPS analysis is performed after etching of poly-Si gate stacks with different masks as shown in Fig. 4.4(b). It is considered that a very thin residual film of SiO_X ($x < 2$) remains on the etched poly-Si surface with both the hard masks and PR mask; a large amount of photoelectrons of *Si 2p* from poly-Si are detected with both the hard masks and PR mask due to the thin residual film on the etched poly-Si. It is reasonable that O released from SiO_2 mask reacts with etched TiN surface, forming Ti oxides during plasma etching; whereas it seems unreasonable that thick Ti oxide residues are detected on the etched TiN surface even with Si_3N_4 mask, as shown in Fig. 4.4(a). Here, it is considered that a small amount of oxygen can be supplied from the surface of inner chamber and / or from the SiO_2 adhesion layer under the Si_3N_4 mask as well. Furthermore it is noted that Si released from both the SiO_2 and Si_3N_4 masks promotes the re-deposition of residues on the etched surface in the form of $(TiO_2)_{1-X}(SiO_2)_X$. Although Fig 4.4(a) shows that the main peaks

after etching belong to $(TiO_2)_{1-X}(SiO_2)_X$ with hard masks, it is difficult to tell the difference between TiO_2 and $(TiO_2)_{1-X}(SiO_2)_X$.



(a)



(b)

Fig. 4.4 XPS spectra of (a) *Ti 2p* from TiN gate stacks and (b) *Si 2p* from poly-Si gate stacks with various masks; solid data points: before etching, open data points: after etching for 15s. All samples were dipped into 1% diluted hydrofluoric acid (DHF) for 20s before etching in order to remove any native grown metal oxides. The *Ti 2p* peak is composed of spin orbit doublets, each separated by 6 eV [4.16]. Only *Ti* $2p_{3/2}$ is indicated

in (a). All XPS analyses were performed using a monochromatized Mg *K* α source on a constant pass energy of 10eV.

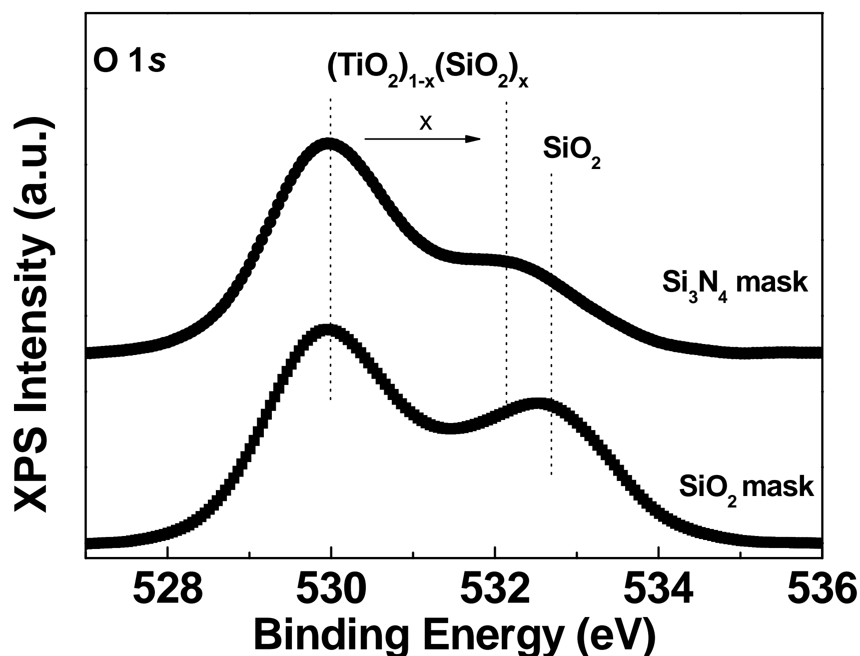


Fig. 4.5 XPS spectra of *O 1s* peak after etching for 15s with various masks. $(TiO_2)_{1-X}(SiO_2)_X$ shows a wide range of binding energy according to the ratio of TiO_2 to SiO_2.

In contrast, Fig 4.5 clearly shows that $(TiO_2)_{1-X}(SiO_2)_X$ as well as TiO_2 are detected on the etched TiN surface under Si_3N_4 mask, indicating that Si in the plasma enhances the re-deposition of $(TiO_2)_{1-X}(SiO_2)_X$ on the etched surface. Mainly, TiO_2 rich $(TiO_2)_{1-X}(SiO_2)_X$ residues ($0 < x < 0.5$) are observed with Si_3N_4 mask (It is believed that oxygen is not sufficient to form both SiO_2 and TiO_2 with Si_3N_4 mask, therefore TiO_2 is formed preferably due to low Gibb's free energy), whereas the $(TiO_2)_{1-X}(SiO_2)_X$ residues in the wide range composition ($0 < x < 1$) are observed with SiO_2 mask. This may be the main reason of the increase of surface roughness with the increase of etch time with SiO_2 mask (it will be discussed in the following section). It is reported that both the Ti-O and Si-O bonds are formed more favorably than Ti-Si bonds; Ti (1.54) has greater electron

affinity for oxygen (3.44) than Si (1.9), in the same way, Si (1.9) has greater electron affinity for oxygen (3.44) than Ti (1.54) [4.15]. This helps to explain the re-deposition of $(TiO_2)_{1-X}(SiO_2)_X$ on the etched surface. Oxygen supplied by degassing from the chamber surface assists the generation of $(TiO_2)_{1-X}(SiO_2)_X$ residues even with Si_3N_4 mask, whereas the same oxygen reacts with carbon to form volatile CO_2 (g) with PR mask as described in the model shown in Fig. 4.6. Schematic models on the behavior of various byproducts generated from the etching of TiN gate stacks are proposed for different masks as shown in Fig. 4.6.

The XPS analysis of Fig. 4.7 shows again that the amount of oxygen contained in residues on the etched TiN surface increases more with increasing etch time with the hard masks, compared to the PR mask. The results show that oxygen concentration increases significantly by 19% with hard mask, whereas oxygen concentration increases slightly by 7% with PR mask as a function of etch time. On the contrary, nitrogen concentration drops significantly by 13% (SiO_2) and 18% (Si_3N_4) with hard mask, whereas nitrogen concentration drops slightly by 5% with PR mask. This implies that thick residual films containing oxygen remain on the etched TiN surface with hard mask, whereas thin residual films containing less oxygen remain with PR mask. The decrease of Ti concentration due to the metal oxide residues is not as significant as the decrease of N concentration, because Ti containing residues are re-deposited on the etched TiN surface under hard mask.

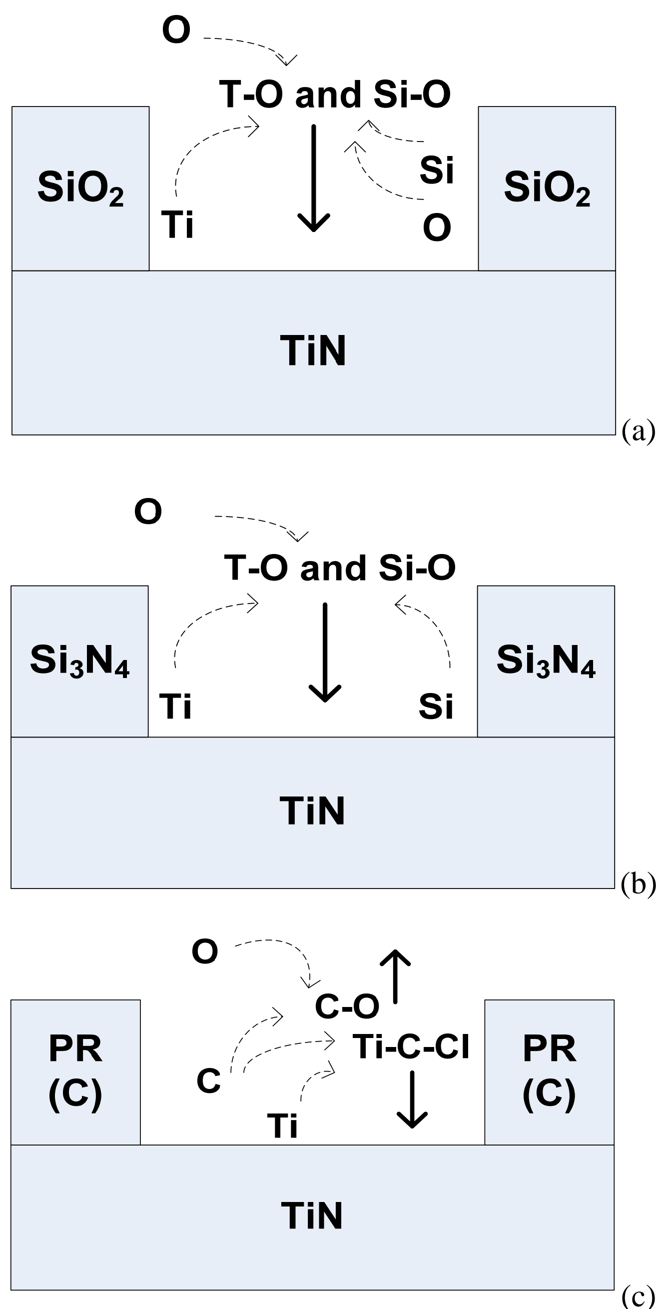
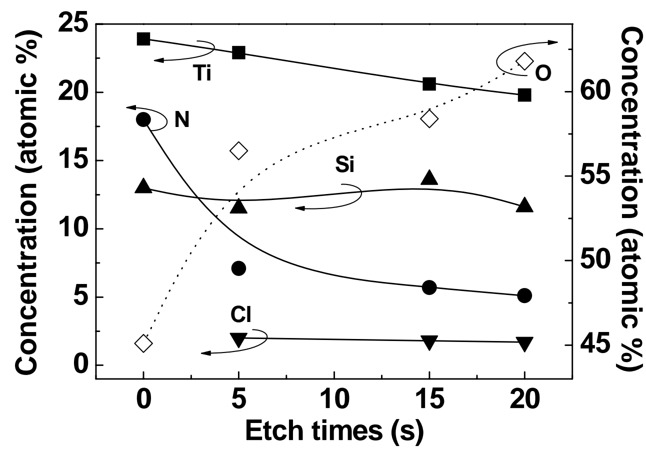
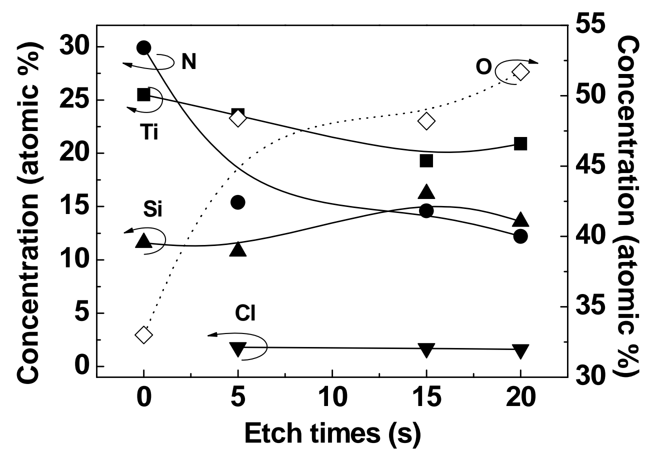


Fig. 4.6 Schematic illustration on the behavior of various byproducts generated from the etching of TiN gate stacks for different masks; (a) SiO_2 mask, (b) Si_3N_4 mask, and (c) PR mask. Oxygen generated from inside the chamber can be a source for the reaction since working pressure is 10 mTorr and base pressure is 1 mTorr in these experiments. There is thin SiO_2 layer inserted between Si_3N_4 mask and TiN to enhance adhesion under Si_3N_4 mask.



(a)



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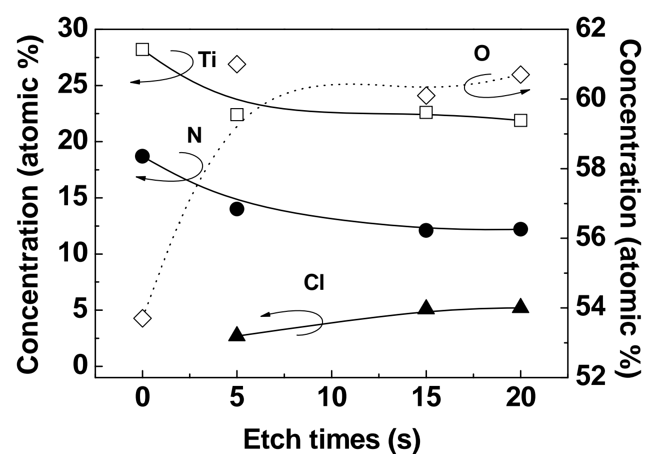

(c)

Fig. 4.7 Concentration of elements from the etched TiN gate stacks as a function of etch time for different masks; (a) SiO_2 mask, (b) Si_3N_4 mask, and (c) PR mask.

4.3.3 Degradation of Surface Properties with SiO_2 Mask

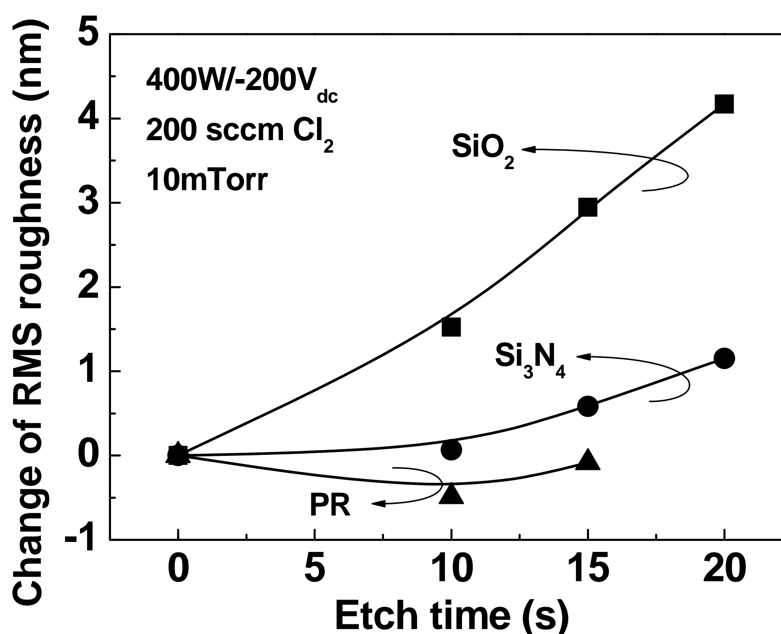

Fig. 4.8 Change of RMS roughness of the etched TiN surface for various masks; negative and positive values in y axis represent the decrease and increase of surface roughness after etching compared to before etching, respectively.

It is found from Figs. 4.8 and 4.9 that surface roughness increases significantly as a function of etch time with SiO_2 mask, whereas surface roughness shows weak time dependence with Si_3N_4 and PR masks. Surface analysis as shown in Fig. 4.4 indicates that chemical components of etched surface are similar each other with both the SiO_2 and Si_3N_4 masks, leading to a similar level of the suppression of etch rates. However, the surface roughness of TiN shows a different trend between SiO_2 and Si_3N_4 masks, respectively. It is attributed to the formation of $(TiO_2)_{1-X}(SiO_2)_X$ residues on the etched surface with SiO_2 mask. That is, $(TiO_2)_{1-X}(SiO_2)_X$ residues of wide composition range ($0 < x < 1$) are observed on the etched surface with SiO_2 mask, which lead to the development of uneven topography during the etching due to the difference in etching rates of TiO_2 and SiO_2, thereby resulting in surface degradation. It is found that etch rates

of Si oxides are higher than those of Ti oxides by 60% under the same condition. That is, the surface degradation of TiN under SiO_2 mask with etch time can be understood as the result of the uneven etching rates of Ti oxides and Si oxides in $(TiO_2)_{1-X}(SiO_2)_X$ residues on the etched TiN surface.

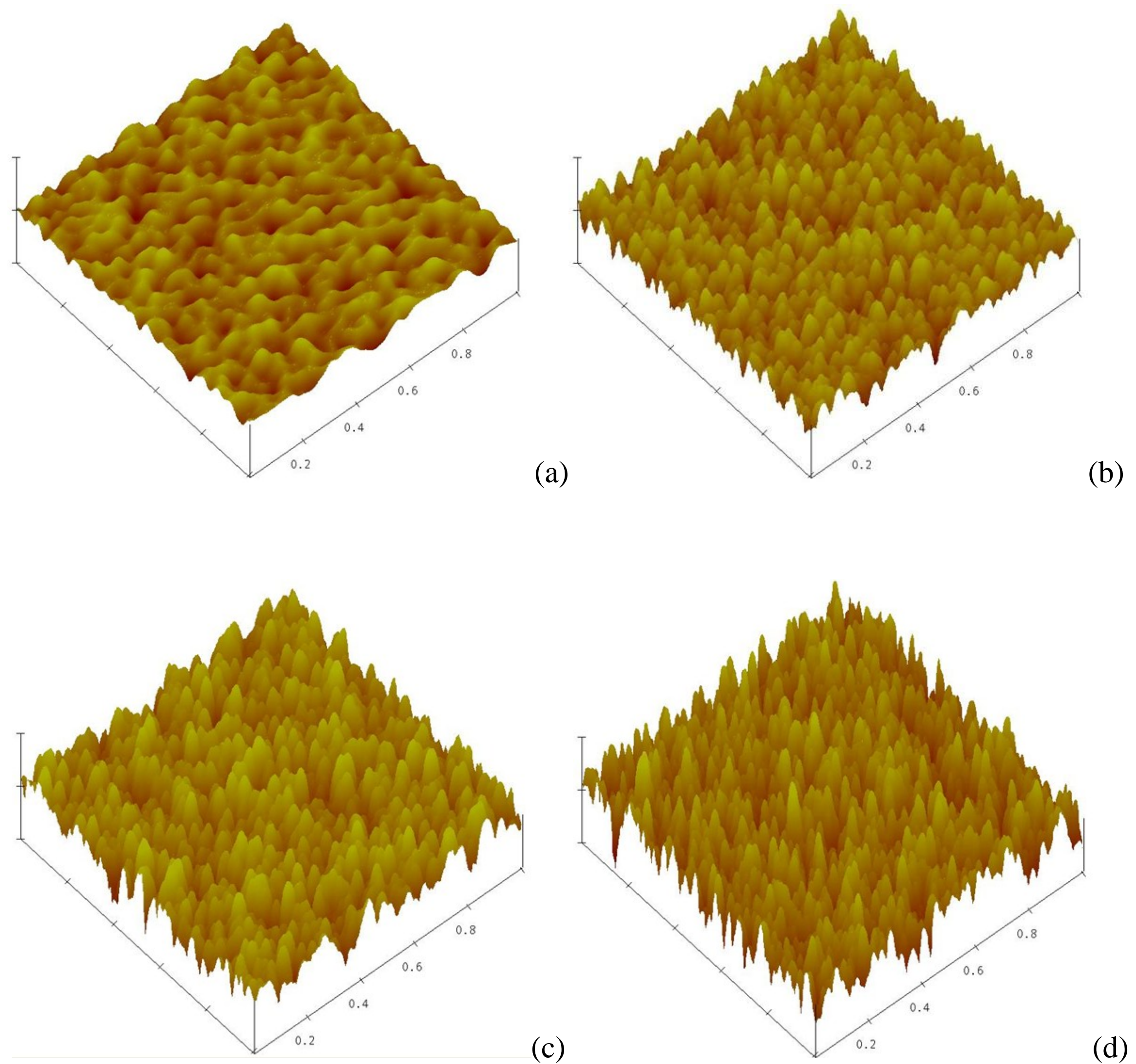

Fig. 4.9 AFM morphology of TiN surface as a function of etch time. The etching experiments are performed at a pressure of 10 mTorr, a source power of 400W, and a bias voltage of -200V_{dc}; (a) 0 s, (b) 10 s, (c) 15 s, and (d) 20 s; 0.2 um/x, 10 nm/y.

4.4. SUMMARY

The suppression of etch rates of TaN, TiN, and HfN was observed with hard masks, compared to PR mask. The decrease of etch rates of TiN was more obvious than that of TaN and HfN under hard mask, because Ti oxides are readily formed on the etched TiN surface due to low Gibb's free energy of the formation of metal oxides. The metal oxide formed on the etched metal surface suppresses further metal etching. $(TiO_2)_{1-X}(SiO_2)_X$ residues are formed on the etched TiN surface due to the reaction of the released Si/O and the etched TiN surface from the TiN gate stacks with hard masks. The surface of TiN degraded significantly with increasing etching time with SiO_2 mask, due to the difference in the etching rates of Si oxides and Ti oxides in the $(TiO_2)_{1-X}(SiO_2)_X$ residues on the etched surface. The mask effects on the etching property of gate materials were well correlated to Gibb's free energy of metal oxide formation.

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CHAPTER 5

A Novel Hafnium Carbide (HfC_x) Metal Gate Electrode for NMOS Device Application

5.1 INTRODUCTION

Transition metal nitrides such as TaN, TiN, and HfN have been intensively studied for NMOS application due to the good thermal stability and the low work function (WF) properties [5.1-5.3]. The low WF properties of these transition metal nitrides are attributed to intrinsic properties of these transition metals. However, the low WF properties of these metal nitrides move to the mid-gap work function properties after S/D activation process [5.3]. It causes to high V_{th} for bulk-Si devices. In order to retain the low WF value even after S/D activation process, very low WF materials, whose WF is less than 4.0 eV, such as La, Gd, Tb, Dy, Er, and Yb, have been incorporated into metal nitrides [5.4]. The WF of the metal nitrides with incorporation of the low WF materials showed around 4.2 ~ 4.3 eV even after 1000°C RTA, which is attractive for the NMOS

application of gate first process. However, this approach shows an integration issues because the evaporation temperature of La, Gd, Tb, Dy, and Er-based byproducts in halogen gases is above 1000^oC. It indicates that those elements make gate stack dry etching difficult. Therefore, alternative to metal nitrides, new metal electrode should be proposed. It is noted that not only metal nitrides but also metal carbide can be formed using low WF transition metals. While intensive studies have been done on metal nitrides, metal carbides for CMOS process have rarely studied. In this work, various metal carbides are thoroughly evaluated for CMOS metal electrode application in terms of thermal stability, feasibility of WF tunability, and easy of fabrication.

5.2. EXPERIMENTAL DETAILS

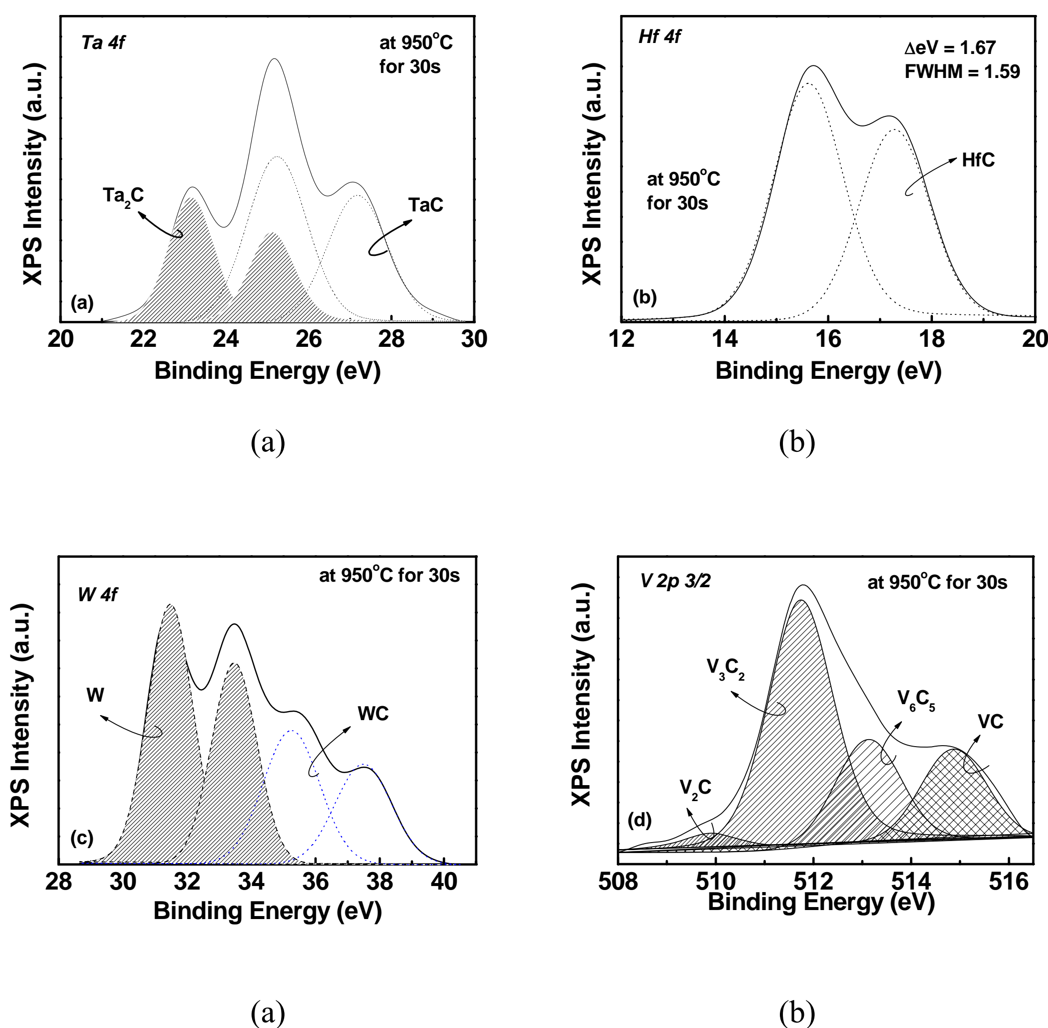
MOS devices were fabricated on p-type Si(100) substrates. Various transition metal carbides (HfC, TaC, WC, and VC) were deposited by direct current (DC) sputtering using alloy targets of HfC, TaC, WC, and VC respectively in an Ar ambient. TaN was deposited on top of the metal carbide for low sheet resistance and the ease of fabrication. The devices experienced an rapid thermal annealing (RTA) at 950^oC for 30 sec for thermal stability evaluation and followed by a forming gas annealing (FGA) at 420^oC for 30min.

Capacitance-voltage (*C-V*) and current-voltage (*I-V*) curves were measured using a HP4284A LCR meter and HP4156A Semiconductor parameter analyzer, respectively, on MOS capacitors with area of 200/200 um^2. EOT and flat-band voltage (V_{FB}) were obtained by fitting the *C-V* curves with the simulated *C-V* curve. X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), X-ray diffraction (XRD), and

high-resolution transmission electron microscopy (HRTEM) were used for material characterization.

5.3 RESULTS AND DISCUSSION

5.3.1 Material and Electrical Properties of Several Metal Carbides



(a) (b)

(a) (b)

Fig. 5.1 XPS spectra of the sputtered (a) TaC , (b) HfC, (c) WC, and (d) VC after RTA at 950°C for 30s. Existence of phase is consistent with phase diagram information; one phase for HfC, two phases for TaC, and four phases for VC, in addition, there is no stable single phase for WC below 1000°C, in other word, W and WC coexist.

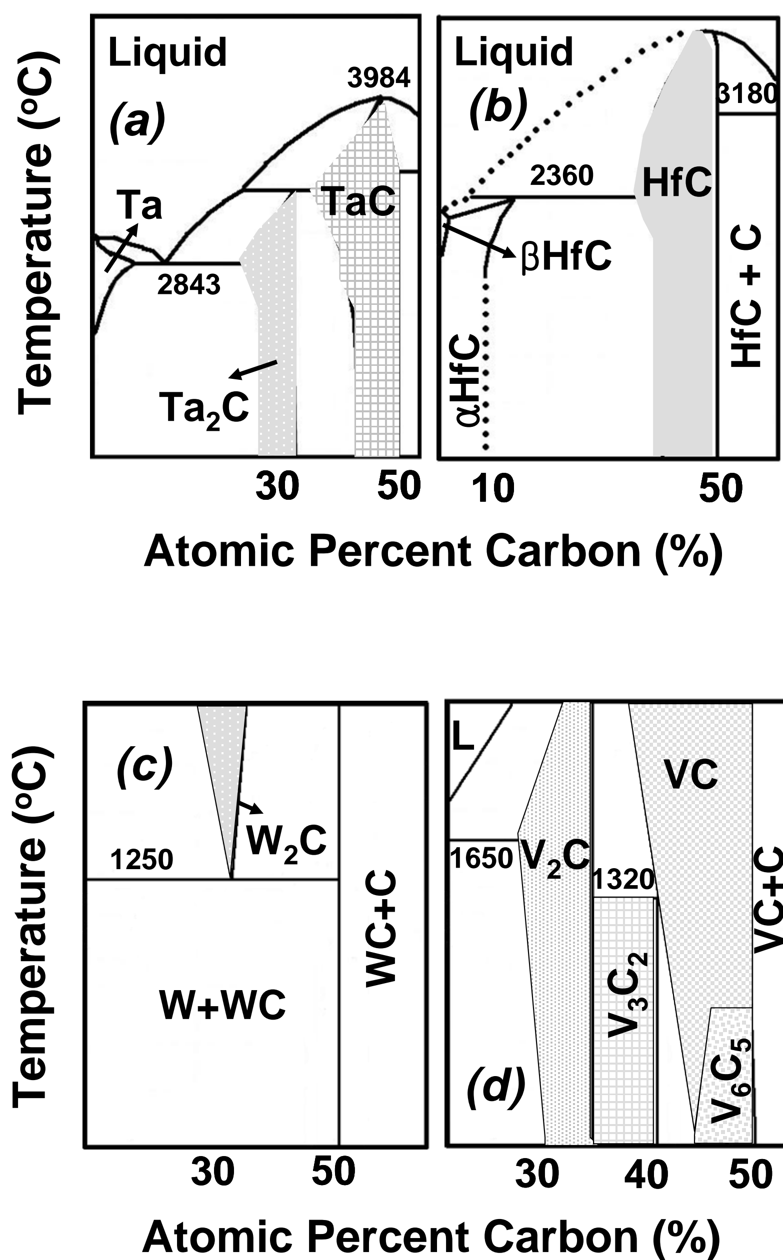


Fig. 5.2 Carbon- (a)Ta, (b)Hf, (c)W, and (d)V phase diagram. Homogeneity range is shown in shadow section. The trend of homogeneity phase of each metal carbide is consistent with XPS results as shown in fig.5.1.

Chemical states of various metal carbides were analyzed using XPS as shown in Fig. 5.1. Figure 5.1 shows the core level spectra of *Ta 4f* (a), *Hf 4f* (b), *W 4f* (c), and *V 2p* $_{3/2}$ (d) for the TaC (a), HfC (a), WC (c), and VC (d) respectively. It shows that there is one phase on the sputtered HfC film, two phases on TaC film, and four phases for VC. For the

WC, not only WC but also W is observed. It indicates that HfC has one single phase and provides wide process window, on the contrary, VC has multi-phases resulting in narrow process window. Simplified phase diagrams of Ta-C, Hf-C, W-C, and V-C are shown in Fig. 5. 2. It also shows that there is one phase for HfC, two phase for TaC, and four phases for VC, respectively. On the other hand, there is no single stable phase for WC under 1250°C. The presence of phases of metal carbides as shown in Fig. 5.2 is consistent with the existent chemical states as shown in Fig. 5.1. For VC, many phases such as V_2C, V_3C_2, V_6C_5, and VC, coexist, which implies the narrow process window and poor reproducibility. The VC film shows carbon-rich nature and the C-C bond is observed by XPS. For the VC film, the excessive carbons are easy to be segregated in the grain boundary and will diffuse into dielectrics during high temperature process, leading to degradation of gate dielectric, which is evidenced by the stretch out of *C-V* curve in Fig. 5.3.

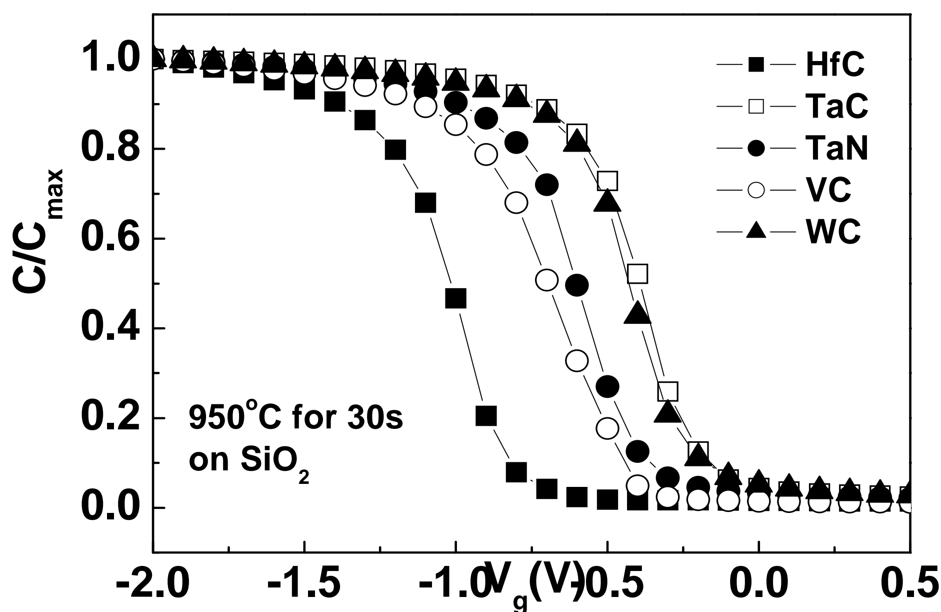


Fig. 5.3 The normalized *C-V* curves of various metal carbides on SiO_2.

The work function behavior of various metal carbides can be estimated by high-frequency *C-V* measurement. Figure 5.3 show the *C-V* curve of various metal carbides on SiO_2 after 950°C RTA. The *C-V* curves in Fig. 5.3 show that metal carbides are thermally stable on SiO_2 gate dielectric at high temperature (950°C). HfC has very low flat-band voltage, indicating a low work function and will be suitable for NMOS, whereas TaC and WC have a high flat-band voltage and can be candidates for PMOS. For WC, W is coexisting with WC. This W will react with underlying dielectrics at high temperature process and increase the interfacial layer thickness, resulting in a significant increase of EOT. Figure 5.1-5.3 show that HfC is a good candidate for NMOS application because it shows a low WF and wide process window.

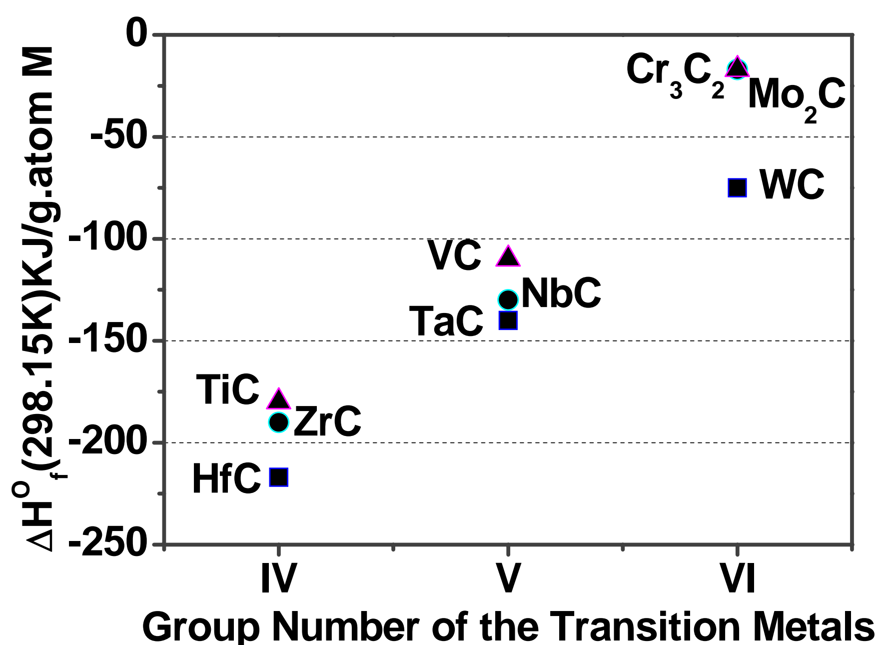


Fig. 5.4 Heats of formation of interstitial carbides. Heat of formation indicates thermal stability [5.5]. Lower (more negative) heat formation value indicates better thermal stability.

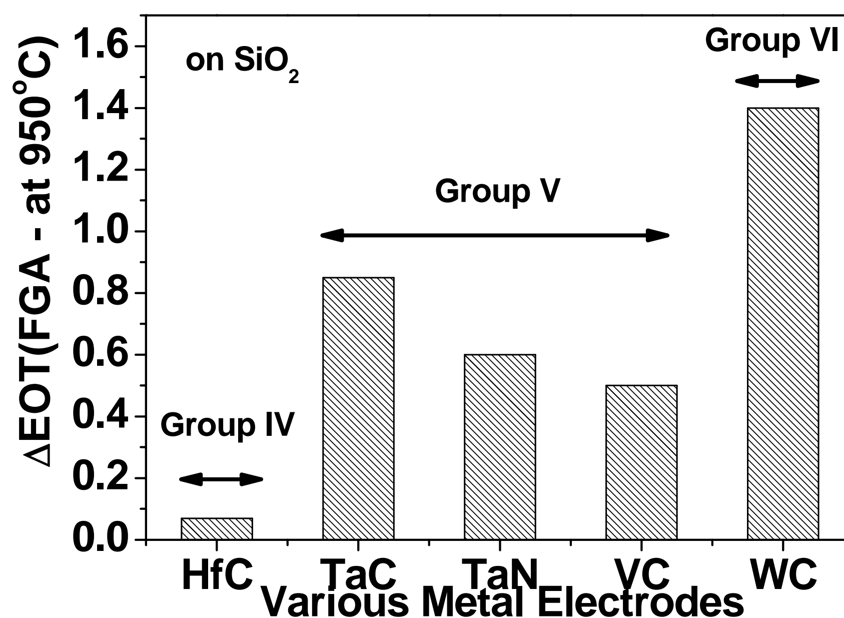


Fig. 5.5 ΔEOT (EOT after RTA minus EOT before RTA) for various metal electrodes. ΔEOT results are well matched to the heat of formation trend.

In addition to electrical performance of metal carbides, thermal stability of metal carbides is another key integration issue. Heat of formation of metal carbides is shown in Fig. 5.4 to investigate the thermal stability of metal carbides. It shows that group IV carbides show better thermal stability than any other metal carbide. Furthermore, thermal stability of HfC is better than that of any other group IV metal carbides as shown in Fig. 5.4. Figure 5.5 shows ΔEOT (EOT after RTA at 950°C followed by forming gas annealing at 450°C minus EOT after forming gas annealing at 450°C) for various metal carbides. It indicates that HfC shows a superior thermal stability due to the lower heat of formation as shown in Fig. 5.4. Furthermore, the ΔEOT trend in Fig. 5.5 is consistent with the trend of heat of formation as shown in Fig. 5.4. Considering various factors of metal carbides as shown in Fig. 5.1 ~ 5.5, HfC metal carbide can be chosen for NMOS

device application because it shows low work function and good thermal stability among other metal carbides.

5.3.2 HfC Metal Carbides for NMOS Applications

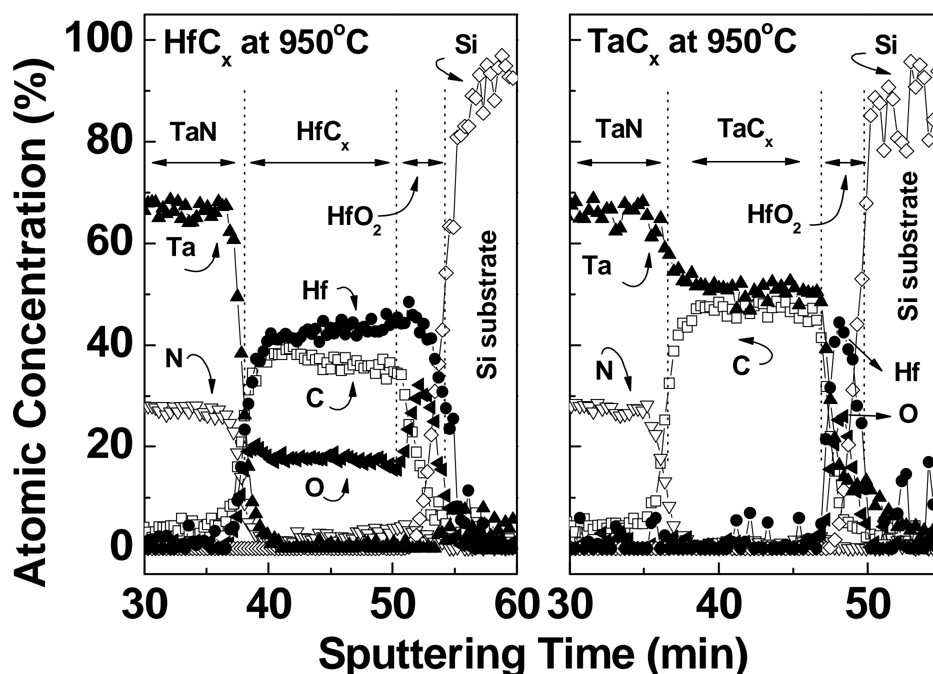


Fig. 5.6 AES depth profiles of TaN / HfC / HfO_2 and TaN / TaC / HfO_2 gate stacks.

The HfC in Fig. 5.1(b) shows a shift of *Hf 4f* peak spectra to a higher binding energy compared to reported HfC peak value, which indicates the presence of residual oxygen at the interstitial sites in the HfC [5.6]. The residual oxygen in HfC is beneficial for the application to gate electrode, because it is known that the oxygen residues at interstitial sites of HfC enhances the diffusion barrier properties [5.7] which helps to reduce interfacial layer growth due to reduced oxygen diffusion. The AES depth profiles of HfC also show the oxygen residues in HfC, whereas there is no oxygen in TaC as shown in Fig. 5.6 even if the deposition method is identical. Furthermore, the AES data

shows that there is no indication of inter-diffusion between TaN and HfC, for comparison, depth profile of TaN /TaC is also shown.

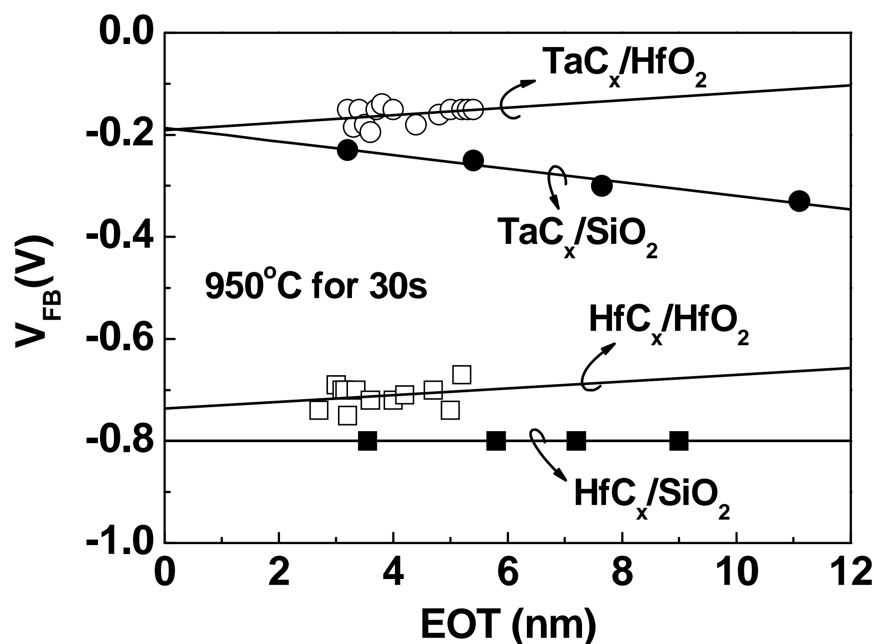


Fig. 5.7 V_{FB} versus EOT for metal carbides on HfO_2 or SiO_2 gate dielectrics.

The WF values of HfC and TaC on SiO_2 and HfO_2 in the work were extracted from the V_{FB} versus EOT plots as shown in Fig. 5.7. The extracted work function values of HfC on SiO_2 and HfO_2 are 4.10 eV and 4.16 eV respectively which is perfectly suitable for NMOS application. Dependence of work function on different gate dielectric, which is the indication of Fermi-level pinning, is also negligible, even though the WF of HfC is near the conduction band-edge of silicon as shown in Fig. 5.8. For the comparison, the WF of TaC was obtained and showed a mid-gap work function value of 4.7 eV on both SiO_2 and HfO_2. Figure 5.8 summarizes the WF values of HfC, TaC, and TaN on different gate dielectrics. It shows clearly that WF of HfC on gate dielectrics is close to conduction band of Si, indicating that HfC is suitable for the NMOS application.

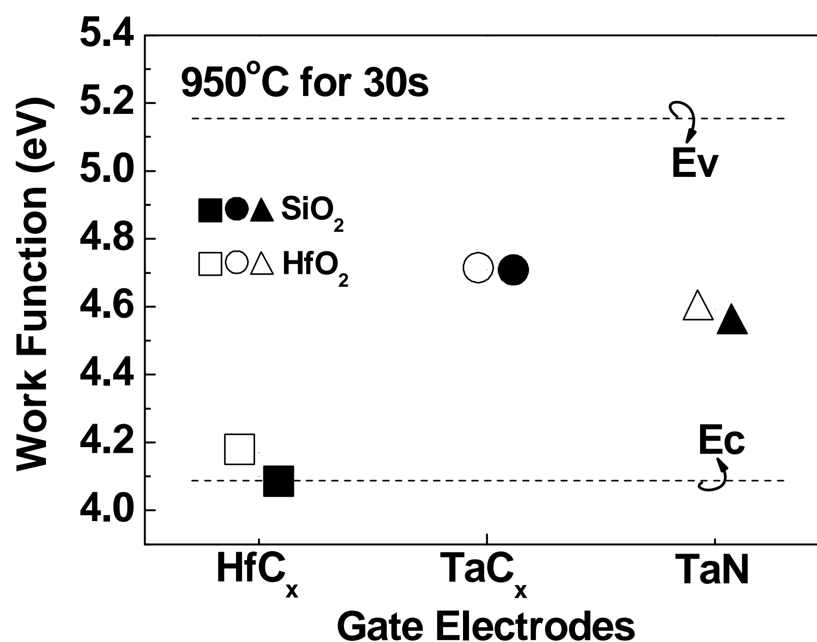


Fig. 5.8 Effective work functions for various gate electrodes and dielectrics

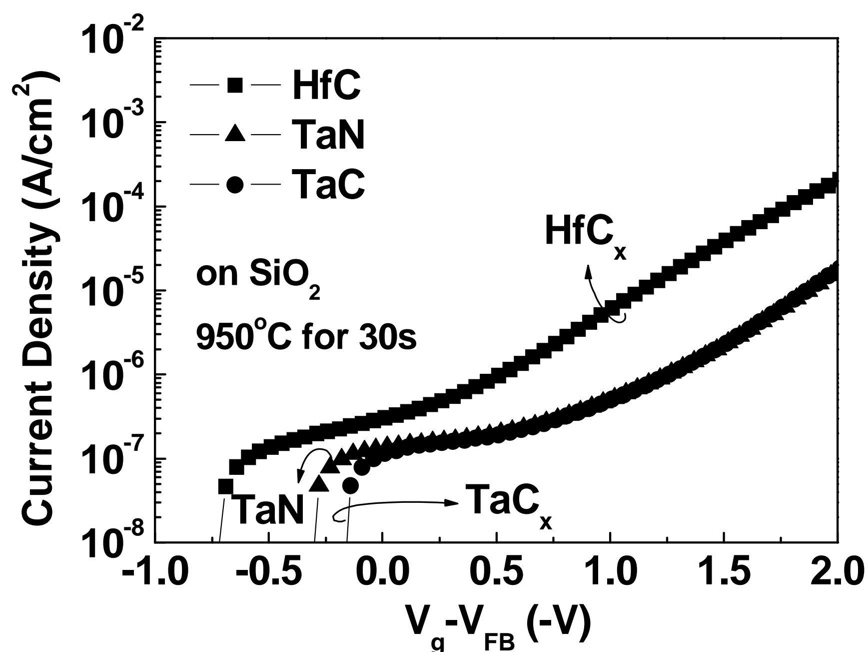


Fig. 5.9 Gate leakage currents of TaC, TaN, and HfC on SiO_2 under negative gate bias.

Figure 5.9 shows electron tunneling currents under gate-side injection (negative bias to gate). Early start of tunneling for HfC confirms the lowest work function of HfC among the three. Figure 5.10 shows the TEM pictures of various metal electrodes. It is shown that the interfacial layer of HfC is thinnest among other layers of metal electrode as shown in Fig. 5.10. It indicates that HfC plays a role as a good oxygen barrier material, resulting in lower EOT.

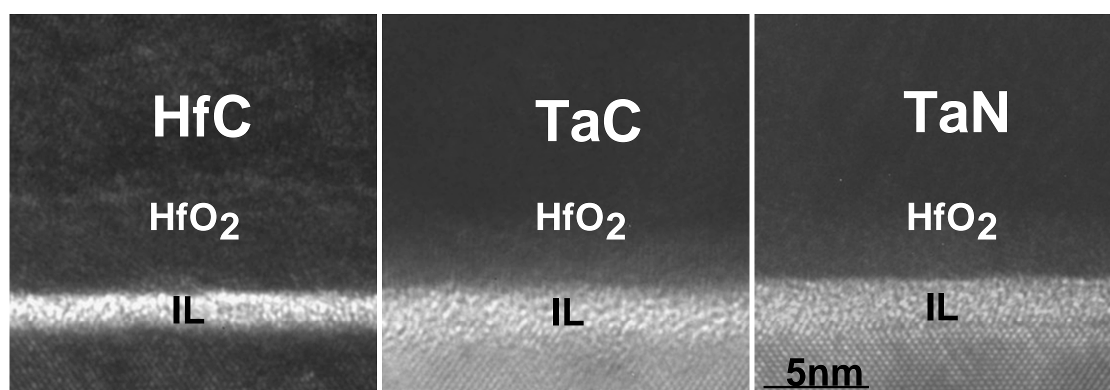


Fig. 5.10 TEM images of HfC, TaC, and TaN on HfO_2 after annealing at 950^oC for 30s. Interfacial layer (IL) between HfO_2 and Si is minimal for HfC, demonstrating good oxygen diffusion barrier property of HfC.

Figure 5.11 shows that work function dependence on thickness of metal electrode. It shows that WF of HfC increase, as thickness of HfC decrease, whereas WF of TaC or TaN does not shows thickness dependence. It indicates that material properties of HfC vary depending on thickness of HfC. XRD analysis was carried out to investigate the materials properties as a function to thickness of metal electrode. XRD data as shown in Fig. 5.12 shows that HfC film consist of Face-Centered Cubic (FCC) for 35nm thickness, whereas monoclinic and FCC peaks appear as thickness of HfC decrease. It indicates that there is a critical thickness to retain the bulk properties of FCC HfC. As the thickness of HfC become thin (~ 15 nm or less), both monoclinic HfO_2 and FCC HfC coexist,

resulting in relatively higher work function as shown in Fig. 5.11. Furthermore, TEM images are shown to understand the micro-structure changes depending on thickness of HfC in Fig. 5.13. The TEM images of HfC also show that as thickness of HfC decrease from 30nm to 15nm, the well arranged structure turn into be disarranged and interfacial layer properties become poor as shown in Fig. 5.13. Based on the results of Figs. 5. 12 and 5. 13, it is found that there is a minimal thickness for HfC film to obtain low WF properties and good thermal stability.

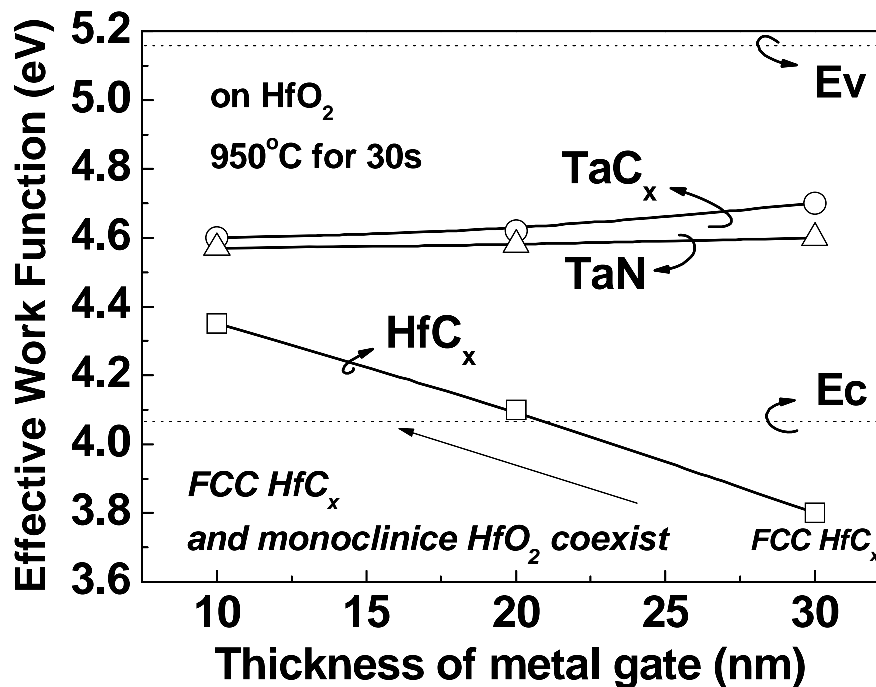


Fig. 5.11 Thickness dependence of work function for TaC, TaN, and HfC on HfO_2. Thicker (at least 20 nm or more) HfC is required to ensure band-edge work function.

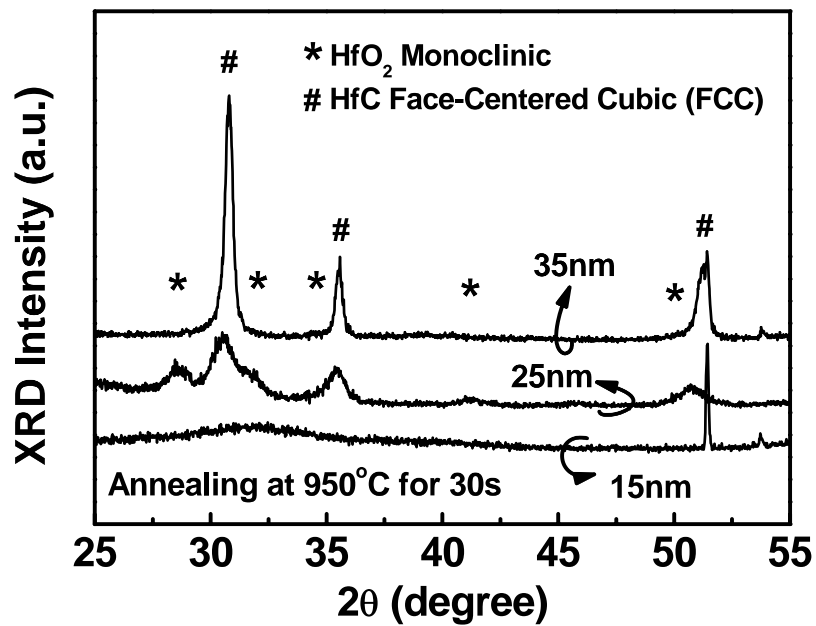


Fig. 5.12 XRD patterns of HfC film. The HfC lattice increase due to oxygen residual.

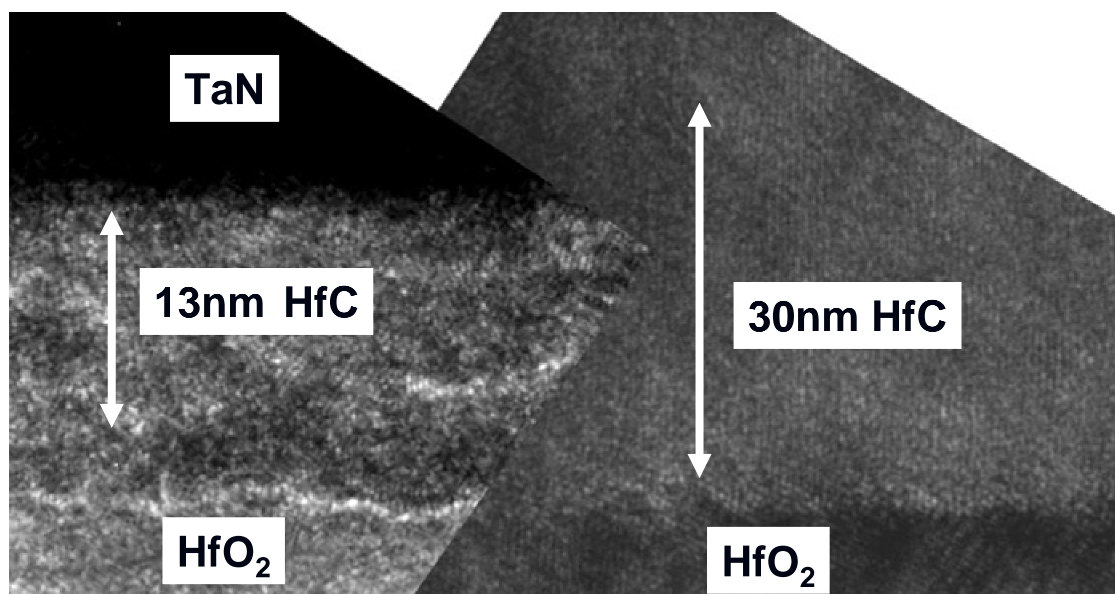


Fig. 5.13 TEM images of HfC on HfO_2. FCC HfC and HfO_2 coexist in HfC when deposited HfC is thin, whereas only FCC HfC exists in HfC for thicker deposited HfC.

2.4. SUMMARY

Various metal carbides such as HfC, TaC, WC, and VC have been evaluated to implement metal carbides in the gate stacks. Based on the intensive study regarding basic material and electrical properties, HfC was proposed and demonstrated for NMOS application. HfC on HfO_2 showed a very low work function value of 3.8 eV, excellent thermal stability and good diffusion barrier properties, and negligible Fermi level pinning. Therefore, the hafnium carbide is a promising candidate for NMOS gate electrode material for gate-first metal gate CMOS process.

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CHAPTER 6

CONCLUSION

6.1 SUMMARY

This work addressed some of the challenging issues for the formation of advanced metal electrode / high-K dielectric gate stacks. The advanced gate stacks consist of hard mask / metal electrode / high-K dielectric. For the successful formation of the gate stacks; formation of metal electrode (chapter 2), high-K removal (chapter 3), and hard mask effect on metal etching (chapter 4) were covered in this work. Furthermore, a new metal electrode candidate was proposed (chapter 5). Not only process issues (chapter 2 – 4) but also device characterization (chapter 5) was discussed to implement metal electrode / high-K dielectric successfully in the gate stack.

6.1.1 Study of Etching Properties of Metal Electrode Gate Stacks

Metal nitrides such as TaN, TiN, and HfN have been intensively studied for metal electrode. Implementation of these metal nitrides in the gate stack was studied using plasma etching of metal electrode. It was found that etching of TaN, TiN, and HfN

obeyed the relation of $Y = A (E^{1/2} - E_{th}^{1/2})$ for ion-assisted chemical etching. The etch rates of the metal nitrides were higher in Cl_2 than in HBr, and this was due to the difference in volatility between the etching byproducts of the metal nitrides in Cl_2 and HBr. Anisotropic profile of TaN metal gate was achieved in Cl_2-based gases. It is attributed to the passivation layer on the sidewall of the gate stacks. The passivation layer is consisted of Ta-Cl-O residues and can be removed in DHF. High selectivity of TaN metal etching over HfO_2 dielectric was obtained using additional O_2 in Cl_2, whereas the use of O from the addition of O_2 or the use of SiO_2 mask resulted in micromasking of the etched surfaces of metal nitride / HfO_2 gate stacks and thereby increased surface roughness. DHF is effective for removal of etching residues after TaN metal etching, whereas HfN is laterally etched.

6.1.2 Study of Wet Removal of High-K Dielectrics

In addition to metal etching, high-K removal is another critical challenge for successful formation of advanced gate stacks. This work investigated ion assisted wet removal of $(HfO_2)_x(SiON)_{1-x}$ in DHF for the advanced CMOS process. HfO_2-rich $(HfO_2)_x(SiON)_{1-x}$ where x is > ~ 0.5 was crystallized after high temperature annealing at 950°C. The crystallized $(HfO_2)_{0.6}(SiON)_{0.4}$ was damaged via the incorporation of N species into the film by the N_2 plasma, resulting in the fast removal of the film in DHF. This is attributed to the structural changes of the film from crystalline to amorphous. It was observed that S/D regions were nitrided more by higher bias power and this adversely affected the electrical property of the devices by increasing threshold voltage. The wet-etch-only process in DHF for 20 min also gave rise to high threshold voltage, compared to the low bias power N_2 plasma process, due to high sheet resistance caused

by residual dielectric. The ion assisted wet removal process explored in this work can be extended from HfO_2 to other high-K materials showing low crystallization temperature.

6.1.3 Study of Effects of SiO_2 / Si_3N_4 Hard Mask on Metal Etching

Not only metal electrode / high-K dielectric gate stacks but also hard mask will be implemented for the further advanced gate stacks. The effect of hard mask on metal etching was studied. The suppression of etch rates of TaN, TiN, and HfN was observed with hard masks, compared to PR mask. The decrease of etch rates of TiN was more obvious than that of TaN and HfN under hard mask, because Ti oxides are readily formed on the etched TiN surface due to low Gibb's free energy of the formation of metal oxides. The metal oxide formed on the etched metal surface suppresses further metal etching. $(TiO_2)_{1-X}(SiO_2)_X$ residues are formed on the etched TiN surface due to the reaction of the released Si/O and the etched TiN surface from the TiN gate stacks with hard masks. The surface of TiN degraded significantly with increasing etching time with SiO_2 mask, due to the difference in the etching rates of Si oxides and Ti oxides in the $(TiO_2)_{1-X}(SiO_2)_X$ residues on the etched surface.

6.1.4 Study of Metal Carbide Electrodes for Gate Stacks

Selection of new metal electrode in the gate stack is ongoing work. In the chapter, a novel HfC_x was proposed and demonstrated for NMOS application. HfC_x on HfO_2 showed a very low work function value of 3.8 eV, excellent thermal stability and diffusion barrier properties, and negligible Fermi level pinning. Therefore, the hafnium carbide is a promising candidate for NMOS gate electrode material for gate-first metal gate CMOS process.

6.2 Suggestion for Future Work

Even if this work contains a lot of practical and helpful information for advanced metal electrode / high-K dielectric gate stacks, more detailed investigation and study should be followed to satisfy the coming ITRS road map. Therefore, it is worthy to note the suggestions for the future work.

In chapter 2, plasma etching of metal nitrides such as TaN, TiN, and HfN was studied. However, selection of metal electrode is not finalized yet, therefore, once metal electrode is finalized, plasma etching of new metal electrode should be studied; transition metal nitrides were intensively studied for potential metal electrode at this moment. Recently, Al-contained metal electrode was reported for PMOS application [6.1] in stead of high WF materials such as Pt, Ni, and Ir, while La-contained metal electrode was reported for NMOS application [6.2]. When it comes to La-contained metal electrode, the La elements make gate stack dry etching difficult. Therefore, once selection of metal electrode is finalized depending on the application, new process should be developed based on the new metal electrode. Besides developing new process, as device continues to shrink, the effect of sidewall roughness of metal electrode on device performance such as variability and reliability is significant. The effect of sidewall roughness in the gate stacks should be investigated.

For the development of high-K removal, recently, Al contained Hf-based high-K was reported for PMOS application [6.3], whereas La contained Hf-based high-K was reported for NMOS application [6.4]. In that case, contamination caused by addition of Al and La will be a new challenge. Successful removal of Al/La-contained Hf-based high-K should be investigated. Besides the contamination issues, undercut of gate dielectric is another challenge. Most of dielectric etching in the gate stacks; wet etching is preferred to

avoid excess over-etching of S/D region and residues after plasma etching. However, wet etching of the high-K material can lead to unacceptable undercut profiles due to the thickness of high-K dielectric, compared to SiO or SiN materials. The undercut of gate dielectrics degrades both device performances (low capacitance, low drive current, high threshold voltages and early breakdown) and process performance (poor uniformity). This challenge comes from the synthesized factors; increase of dielectric thickness, scaling of devices, and Isotropic wet etching. Undercut issues have not been issued so far due to very thin SiO_2 dielectric. Therefore, new process should be developed to avoid isotropic properties of wet etching.

In addition, as device continues to shrink, the aspect ratio of hard mask keeps increasing and carbon mask will be introduced in stead of SiO_2 or Si_3N_4 hard mask [6.5]. Based on the modification, the effect of high aspect ratio of hard mask or carbon mask should be investigated.

Moreover, for the proposed metal electrode using metal carbides, further WF tunning in the form of ternary system may be necessary for dual metal gate application. The mobility, charge-trapping, and reliability due to the carbon originated from metal carbides also should be investigated.

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APPENDIX – List of Publications

- ***Journal Papers***

1. **<u>Wan Sik Hwang</u>**, Daniel S. H. Chan, and Byung Jin Cho, “Metal Carbides for Band-Edge Work Function Metal Gate CMOS Devices”, submitted to IEEE *Trans. Electron Devices* in January, 2008.

2. **<u>Wan Sik Hwang</u>**, Byung-Jin Cho, Daniel S. H. Chan, Sangwon Lee, and Won Jong Yoo, “Effects of volatility of etch byproducts on surface roughness during etching of metal gates in Cl_2”, *J. Electrochemical Society,* vol. 155, pp. H6, 2008.

3. **<u>Wan Sik Hwang</u>**, Byung-Jin Cho, Daniel S. H. Chan, and Won Jong Yoo, “Low energy N_2 ion bombardment for the removal of $(HfO_2)_x(SiON)_{1-x}$ in dilute HF”, *J. Vac. Sci. Technol A,* vol. 25, pp. 1056, 2007.

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5. **<u>W. S. Hwang</u>**, H. H. Ngu, W. J. Yoo and V. Bliznetsov, “Chemical analysis of etching residues in metal gate stack for CMOS process”, *Studies in Surface Science and Catalysis*, vol. 159 (new developments and application in chemical reaction engineering) pp. 365, Elsevier, Netherlands, 2006.

6. **<u>W. S. Hwang</u>**, J. H. Chen, W. J. Yoo, and V. Bliznetsov, “Investigation of etching properties of metal-nitride / high-k gate stacks using inductively coupled plasma”, *J. Vac. Sci. Technol A,* vol. 23, pp. 964, 2005.

7. Y. Q. Wang, **W. S. Hwang**, G. Zhang, G. Samudra, Y. -C. Yeo, and W. J. Yoo, "Electrical characteristics of memory devices with high-k HfO_2 trapping layer and dual tunneling layer SiO_2 / Si_3N_4", IEEE *Trans. Electron Devices,* vol. 54, pp. 2699, 2007.

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9. Andy E. -J. Lim, **W. S. Hwang**, X. P. Wang, Doreen M. Y. Lai, G. S. Samudra, D. -L. Kwong, and Y. -C. Yeo, "Metal gate work function modulation using hafnium alloys obtained by the Interdiffusion of thin metallic layers", *J. of the Electrochemical Society,* vol. 154, pp. H309, 2007.

- ***Conference Papers***

1. **W. S. Hwang**, C. Shen, X. P. Wang, Daniel S. H. Chan, and B. J. Cho, "A novel hafnium carbides (HfCx) metal gate electrode for NMOS device application", ***2007 Symposium on VLSI Technology,*** June 2007 in Kyoto, Japan.

2. **W. S. Hwang**, B. –J. Cho, D. S. H. Chan and W. J. Yoo, "Study on nonvolatile byproducts generated during etching of advanced gate stacks", *28th International Symposium on Dry process,* November 2006 in Nagoya, Japan.

3. **W. S. Hwang**, V. N. Bliznetsov, B. –J. Cho, D. S. H. Chan and W. J. Yoo, "Damage free etching of RuO_2 in O_2 / He plasma", *28th International Symposium on Dry process*, November 2006 in Nagoya, Japan.

4. **W. S. Hwang**, W. J. Yoo, B. J. Cho, and D. S. H. Chan, "Effects of low energy nitrogen plasma on the removal of HfSiON", *AVS 53rd International Symposium, November 2006* in San Francisco, CA, USA.

5. **W. S. Hwang**, H. H. Ngu, G. Zhang, V. N. Bliznetsov, and W. J. Yoo, "Effect of SiO_2 mask on surface properties of advanced gate stacks using ICP of Cl_2 / HBr", *27th International Symposium on Dry Process,* November 2005 in Jeju, Korea. **(Won DPS 2006 Young Research Award)**

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13. B. J. Cho, **W. S. Hwang**, and D. S. H. Chan (**Invited**), "Metal carbide electrodes for gate-first metal gate CMOS process", *4th International Symposium on Advanced Gate Stack Technology,* September 2007 in Austin, Texas, USA.

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