RADIO FREQUENCY FRONT-END CIRCUITS

FOR W-CDMA DIRECT CONVERSION RECEIVER

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NATIONAL UNIVERSITY OF SINGAPORE

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Summary

The work presented in this thesis focuses on the system analysis and the development of RF front-end circuits for the direct conversion receiver. The system analysis includes the brief review on the W-CDMA system, the studies of different wireless receiver topologies and in-depth analysis of the problem associated with the direct conversion receiver. Furthermore, the technical requirements of the direct conversion receiver for the W-CDMA application are also analyzed and the design goals for the RF front-end circuits are derived.

In the second part of the thesis, the designs, simulations and the measurements from two LNA topologies, two down-converted mixers and one integrated front-end circuit are covered. In the LNA designs, single-ended and differential versions are presented. The core circuits for both versions are based on the cascode topology with inductive source degeneration. The active balun circuit is also included for the conversion of single-ended LNA output to differential signals. For the mixer circuits, two different approaches are adopted for improving the issues related to LO-leakage and the second-order intermodulation products. In the first mixer design, the transconductance driver stage and the switching stage are separated to avoid the direct path for the leakage from LO – port to RF – port. The second mixer circuit, the common-gate configuration is utilized as driver stage and current injection technique and frequency trap are used to improve the flicker noise and the second-order intermodulation products. For the verification of the IM2

performance of the direct conversion receiver, the integrated front-end design which consists of the differential LNA and the second mixer circuit are fabricated and measured.

All the circuits are implemented through the Chartered Semiconductor Manufacturing 0.35 μm CMOS technology with the RF option. The models of active and passive devices used in the designs are based on IME in-house extracted RF model. All the circuits are mounted on QFP-24 pin package and measured on the FR-4 PCBs.

The measurement of LNAs showed that the version consisting of single-ended LNA and active balun has better noise figure and power gain than differential design. However, the measured noise figure and power gain are lower than the simulated results. This discrepancy becomes larger for the low gain mode when the bypass switches are turned on. The unexpected higher loss from the transmission gate is the suspected root cause for such deviations. For the down-converter, the Gilbert cell mixer with the common-gate input has inferior conversion gain and worse port-to-port isolation than the other approach. The mismatches of the common-gate input may result in considerable signal loss. However, the integrated front-end design shows more encouraging results, the total gain and noise figure in high gain mode are 22 dB and 9.5 dB respectively. The *IIP2* is 23 dBm in high gain mode, this result will be further improved when the bypass switch of the LNA is turned on. The total current consumption is 17 mA in high gain mode and it is reduced to 12 mA when the LNA is switched off.

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List of Abbreviations

GSM	Global System of Mobile Communication
CDMA	Code-Division Multiple Access
WLAN	Wireless Local Area Network
W-CDMA	Wideband Code-Division Multiple Access
GPS	Global Positioning System
PCB	Printed Circuit Board
IC	Integrated Circuit
BiCMOS	Bipolar – Complementary Metal Oxide Silicon
CMOS	Complementary Metal Oxide Silicon
BJT	Bipolar Junction Transistor
RF	Radio Frequency
DCR	Direct Conversion Receiver
LO	Local Oscillator
DSP	Digital Signal Processor
LNA	Low Noise Amplifier
MIX	Down-Conversion Mixer
3G	Third Generation
2G	Second Generation
DS-SS	Direct-Sequence Spread Spectrum
FDD	Frequency-Division Duplexing

UMTS	Universal Mobile Telecommunication System
3GPP	3rd- Generation Partnership Project
BPSK	Binary Phase Shift Keying
QPSK	Quadrature Phase Shift Keying
IF	Intermediate Frequency
SAW	Surface Acoustic Wave
BOM	Bill of Materials
DC	Direct Current
FSK	Frequency Shift Keying
BER	Bit-Error Rate
TDMA	Time-Division Multiple Access
ETSI	European Telecommunication System Institute
GPRS	General Packet Radio Service
EDGE	Enhanced Data Rates for GSM Evolution
SiGe	Silicon Germanium
BPF	Bandpass Filter
SINAD	Signal Power / (Noise Power + Distortion)
ESD	Electrostatic Discharge
SOC	Silicon-on-Chip
MESFET	Metal-Semiconductor Field Effect Transistor

List of Symbols

SNR	Signal-to-noise ratio
NF	Noise figure
F	Noise factor
F_{min}	Minimum noise factor
f_{LO}	Frequency at mixer's LO port
f_{RF}	Frequency at mixer's RF input port
f_{IF}	Frequency at mixer's IF output port
L_{eff}	Effect channel length of MOS transistor
HD2	Second-order harmonic distortion
HD3	Third-order harmonic distortion
IM2	Second-order intermodulation product
IM3	Third-order intermodulation product
IP2	The second-order intercept point
IIP2	Input-referred second-order intercept point
OIP2	Output-referred second-order intercept point
IP3	The third-order intercept point
IIP3	Input referred third-order intercept point
OIP3	Output referred third-order intercept point
P_{IIP3}	Input referred third-order intercept point in dBm
P_{1dB}	1-dB power compression point in dBm
$P_{in,min}$	Minimum input signal power to the receiver in dBm

S_{11}	Input reflection coefficient of S-parameter
S_{22}	Output reflection coefficient of S-parameter
S_{21}	Forward gain of S-parameter
S_{12}	Reverse isolation of S-parameter
$SFDR$	Spurious-free dynamic range
DR_{min}	Minimum dynamic range required for the receiver
g_m	Transconductance
$g_{m,sat}$	Transconductance of transistor in saturation
$I_{d,sat}$	Drain current of transistor in saturation
W	Width of MOS transistor
f_T	Unity-gain cutoff frequency
ω_T	Unity-gain cutoff angular frequency
V_{od}	Gate overdrive voltage
v_{sat}	Saturation velocity
E_{sat}	Velocity saturation field strength
μ_{eff}	Effective mobility
μ_o	Low field mobility
θ	fitting parameter

Chapter 1 Introduction

1.1 Motivation

A successful launch of cellular communication system, such as Global System of Mobile Communication in late 1980s, has ignited an explosive growth of the number of wireless services subscribers in recent years. From 1990s onward, many wireless services (e.g. CDMA, WLAN, HiperLAN, Bluetooth, etc.) were offered by telecommunication companies world wide to meet the strong consumer demand on portable terminals. The current trend of convergence among various technologies such as data communications and mobile communications into a single platform will greatly improve the capabilities of a wireless handset, however, this development will also increase the technical complexity of the wireless system. It can be foreseen that the strong consumers' demands on such multi-mode and multi-band wireless terminals, which are inclusive of short range applications (e.g. Bluetooth, WLAN, etc.) and long range mobile services (e.g. GSM, W-CDMA, GPS, etc.), will drive the developments of RF transceiver into smaller form factor, lower power consumption, and higher performance in all aspects.

In the past decade, wireless systems were realized by assembling different modules on to single printed circuit board. These modules usually consist of discrete passive components together with various integrated circuits. Because of different functionalities and technical challenges, the ICs for wireless communication systems are fabricated from different

semiconductor technologies as shown in Figure 1.1. To build a cost effective transceiver for consumer markets, it is preferable to have all the circuits manufactured in the same semiconductor technology. Among the current semiconductor processes, BiCMOS technology is considered the most suitable process for meeting the technical challenges, however, higher manufacturing cost may not be a viable solution for the wireless devices targeted for consumer market. On the other hand, continuous improvement of the CMOS processes has provided an alternative way of achieving low cost single-chip solution for wireless transceiver. Although a standard CMOS process can increase the integration level with lower cost and avoid the interfacing and compatibility issue with the digital baseband circuit, the performance of CMOS circuits is still not very competitive to operate in radio frequency range due to inferior transconductance (g_m) and lower unity-gain cut-off frequency (f_T) than bipolar transistor. Hence, it is a challenge to implement the RF front-end circuit in CMOS technology.

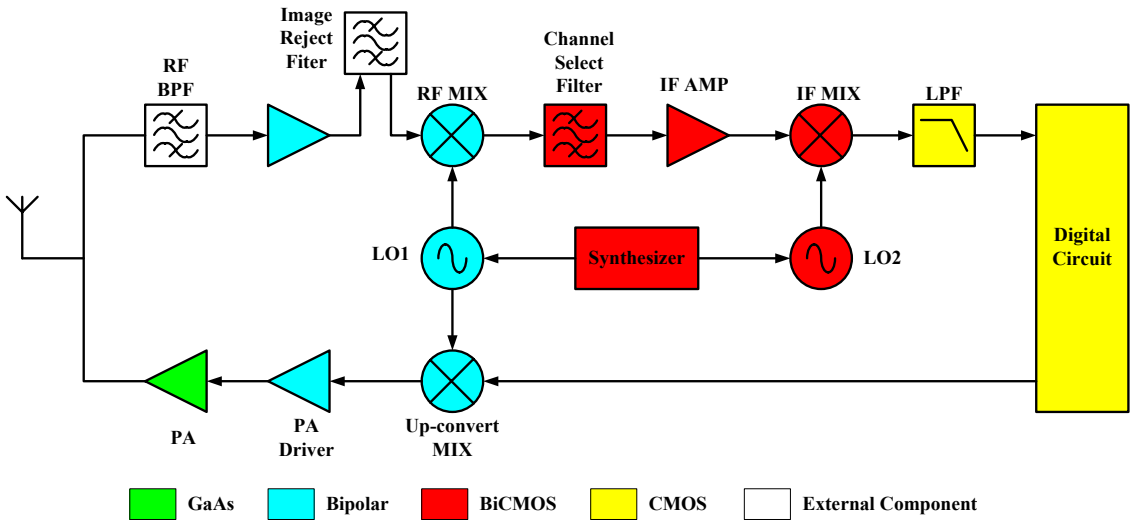


Figure 1.1 The semiconductor technologies used in wireless transceiver modules

To meet the technical challenges mentioned above, the receiver architecture plays a crucial role in wireless system. Among receiver topologies, direct conversion receiver has the simplest structure and attains the highest integration level of receiver circuitry, it is also considered as one of the most promising solutions for the next generation wireless communication platform. However, the unique problems associated with the direct conversion receiver, such as dc offsets, leakages from local oscillator, etc., have limited the use of direct conversion receiver in highly demanding services (e.g. GSM and W-CDMA). The intense research efforts from academic communities and industrial players have shown encouraging results and great progress in the receiver design from system and circuit level respectively. It is believed that by combining the direct conversion receiver with the growing power of digital signal processing, the ultimate goal of having a single-chip solution for all wireless systems becomes realistic and achievable in the near future.

1.2 Objectives of The Work

The main objectives of this project primarily focus on the development of low-power RF front-end circuits for an integrated CMOS direct conversion receiver, which will be targeted for the application of W-CDMA wireless communication system.

The design and realization of the RF front-end consist of two main circuits, namely, a low noise amplifier for providing signal amplification and a down-conversion mixer for frequency translation. The design goals of having low noise figure and achieving good

linearity are essential to meet the technical requirements for the W-CDMA applications. Apart from these design goals, the integrated front-end circuits also need to have low dc-offset at the output of the mixer stage and provide sufficient gain to the received signal before signal processing in the subsequent stages.

All the circuit blocks are developed and implemented with CMOS technology, so that the front-end circuits can be further integrated with other RF, mixed-signal and digital baseband circuits to alleviate the issues of interface and compatibility among different process technologies.

1.3 Thesis Outline

The presentation of this thesis is organized from the system level down to the circuit level, and then followed by the experimental results, discussion and conclusion. The thesis is divided into five chapters.

After the introductory chapter on the project scope and objectives, an overview of a W-CDMA communication system is presented in Chapter 2. The unique properties and technical requirements of W-CDMA system are highlighted. This chapter also covers the basics of receiver architecture, followed by the introduction of the direct conversion receiver for the W-CDMA system and its advantages and disadvantages as a radio frequency wireless receiver. The second part of the chapter focuses on the analysis and

system planning of the proposed DCR architecture. Finally, the design goals of RF front-end circuits for the W-CDMA receiver are derived.

In Chapter 3, the technical challenges of the RF circuits and the design considerations of the respective circuits are presented. In the second section, the design equations for the circuit topologies are derived and a detailed discussion on the implementation issues of LNA and mixer is presented. In the last section of Chapter 3, the design of the integrated RF front-end circuit is introduced.

Chapter 4 contains the details of IC implementation of the LNA and mixer, and then the experimental results of the chipset and integrated version of RF front-end design are shown and discussed. All the designs are implemented using a CMOS 0.35μm technology.

In the final chapter, the conclusion of this work is presented and the recommendations for future work are given.

Chapter 2 RF System for W-CDMA Applications

2.1 Overview of W-CDMA System

The communication protocol of wideband code-division multiple access technology for the third generation cellular network was officially adopted in 1999 [49]. Comparing with the current second generation GSM system, the W-CDMA system provides higher subscriber capacity and enhanced capability in handling mobile data communication, where the data rate can be as high as 2 Mbps [1]. During the high speed data communication, wider channel bandwidth is required for signal transmission and maintaining good signal quality. For W-CDMA technology, the efficient utilization of valuable communication bandwidth is achieved by using a direct-sequence spread spectrum technique, coupled with the code division multiple access method for baseband signal processing. This kind of system not only increases the capacity of wireless subscribers, it also offers strong resistance to interferences and jamming signals under the same signal condition as GSM. By randomly spreading the data stream, the transmitted signal can be recovered by de-spreading the received signal back from the level as low as noise floor [1], [2].

The operating frequencies of W-CDMA handset range from 1920 ~ 1980 MHz for the uplink communication (from handset to base station) and 2110 ~ 2170 MHz for the downlink communication (from base station to handset). The communication bandwidth is

60 MHz for transmit and receive respectively. Since W-CDMA performs full duplex communication, the minimum frequency gap of 30 MHz between the transmit signal and receive signal become very essential to the performance. With such a frequency gap, the technical requirements of the transceiver design can be relaxed by having a bandpass filter to isolate the receiver and transmitter from signal leakage. In the W-CDMA system, there are twelve channels and each channel occupies about 5 MHz. Since the channel bandwidth is much wider than GSM (i.e. 200 kHz), it is relatively easier to implement the direct conversion receiver architecture because a fractional loss of information caused by the dc-offset at baseband frequencies does not degrade the performance significantly.

Some key performance characteristics of band I of W-CDMA Universal Mobile Telecommunication System – Frequency Division Duplex mode are summarized in Table 2.1. The details of the technical specifications on wireless transmission and reception can be found in the document written by the 3rd-Generation Partnership Project group [3]:

Table 2.1 System characteristics of WCDMA UMTS – FDD mode

Parameter	**Specification**	**Unit**
Uplink frequency	1920 ~ 1980	*MHz*
Downlink frequency	2110 ~ 2170	*MHz*
Nominal channel spacing	5 ± 0.2	*MHz*
Chip rate	3.84 (or 4.096)	*Mcps*
Data rate	32/64/128/256/1024/2048	*Kbps*
Channel bandwidth	5/10/20	*MHz / channel*
Modulation: Uplink Downlink	BPSK QPSK	
Multiple access technique	DS-CDMA	
Duplex procedure	FDD	
Maximum output power	24 (average)	*dBm*

2.2 Receiver Architectures for Wireless Applications

In general, there are three categories of RF receivers used in wireless communication industry based on the bandwidth of intermediate frequency before the demodulation process takes place [4], [5]. All the receiver architectures have their advantages and disadvantages in terms of integration level, power consumption and technical performance. Among RF wireless receivers, the most common form is "superheterodyne" which is invented by E. Armstrong in 1918. As shown in Figure 2.1, this receiver utilizes multiple frequency translations and signal amplifications to improve the received signal-to-noise ratio before the baseband signal processing. By using multiple amplifiers and filters for boosting the signal level and rejecting the interferences, the superheterodyne receiver can achieve superior performance in terms of sensitivity and selectivity. However, these advantages are mainly achieved by implementing many bulky and expensive off-chip filters, for example, the surface acoustic wave filter is used for image rejection and the crystal filter is used for channel selection. These filters limit the integration level of this architecture and increase the cost and the bill of material of the receiver.

To realize a cost effective solution for wireless handsets, the research direction of RF receiver in recent years is to improve the integration level of the receiver. The simplest approach is to make only one signal down-conversion in the receiver (Figure 2.2), which is also called "homodyne" or "direct conversion" receiver [4] - [7]. The single conversion

architecture is suitable for implementation in the form of integrated circuit because no off-chip filters are required, however, the technical challenges like dc-offset, self-mixing, LO leakage, etc. have deterred the use of this architecture in many stringent applications.

Another method (Figure 2.3) of increasing the integration level and avoiding the problems associated with direct conversion receiver is to down-convert the received signal to a very low intermediate frequency ("low-IF"), which is usually in the range of 1 kHz to 10 MHz, and then the low-IF signal is processed digitally [8]. Although dc-offset is not a critical issue in this design, the image frequency may become a serious problem. To overcome this problem, a highly symmetrical image-reject RF mixer is necessary. It is required to ensure that the cancellation of the image signal is substantial without degrading the sensitivity of the receiver (>50 dB rejection in some applications). Since the multi-path mismatches in the circuit layout cannot be completely removed, the image rejection is always limited to 30 ~ 40 dB for a CMOS low-IF receiver. This image frequency problem can be alleviated to a certain degree by moving the image-reject operation to lower frequency range rather than at RF frequency, as proposed in [9]. By using the "wideband-IF" receiver approach as shown in Figure 2.4, the received signal is down-converted twice, image-reject mixer is located after the IF1. As long as IF1 is chosen wide enough, the image rejection can be more effective by trading off higher power consumption with the high frequency active filters.

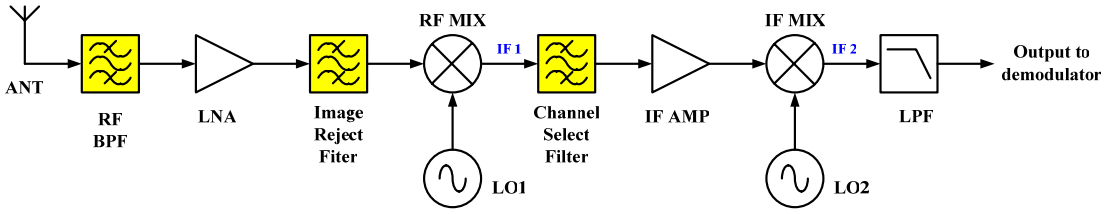


Figure 2.1 Building blocks of superheterodyne receiver

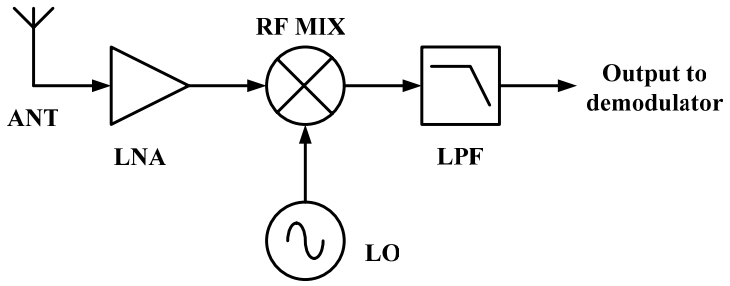


Figure 2.2 Building blocks of direct conversion receiver

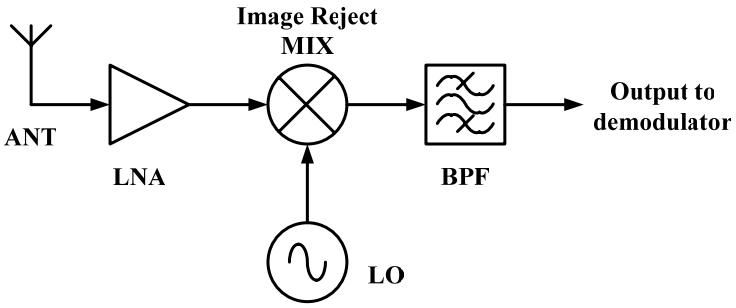


Figure 2.3 Building blocks of low-IF single conversion receiver

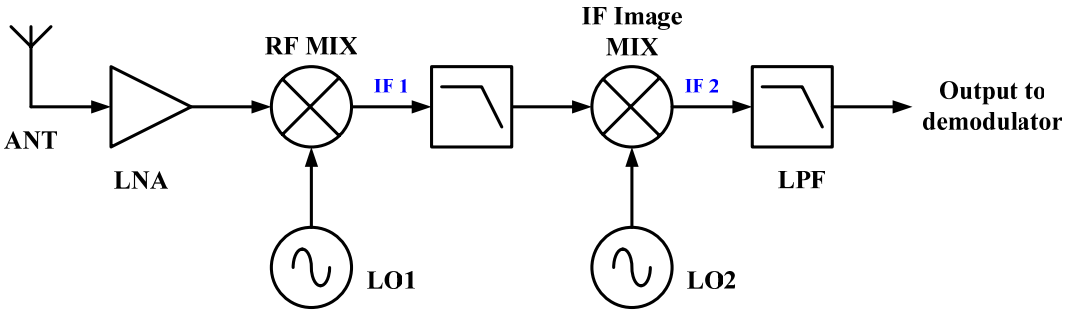


Figure 2.4 Building blocks of wideband IF double conversion receiver

2.3 Direct Conversion Receivers

The direct conversion receiver has a very simple architecture as shown in Figure 2.2, a modulated signal only requires signal down-conversion before demodulation and baseband signal processing. Since the f_{LO} is exactly the same as the received carrier f_{RF}, no f_{IF} will be produced, i.e. $f_{IF} = 0$, and the down-converted signal will be centered at $0\ Hz$. In the low frequency regime, the construction of an active filter is simpler and the rejection of unwanted out-of-band signals accompanied with the RF carrier during the down-conversion process is higher. Theoretically, no image frequency will be observed at the mixer output if the I/Q-path shows a good symmetrical property. In fact, the requirement of the image rejection ratio for the DCR is less stringent ($> 25\ dB$) than the requirement for low-IF receiver ($> 50\ dB$) [10].

2.3.1 Issues Associated with Direct Conversion Receivers

Although the direct conversion receiver offers many advantages such as smaller die area, lower count of off-chip components and lesser power consumption, some problems associated with DCR implementation are still quite challenging to tackle [6], [7]. These inherent problems of DCR are listed below:

- DC-offset after the signal down-conversion
- LO leakage and radiation

- Self-mixing of leaked LO or RF signal
- The impact of flicker noise to output *SNR*
- Intermodulation products from second-order nonlinearity

The origins of these issues are discussed in detail in the following sections.

2.3.1.1 DC Offsets

In a direct conversion receiver, the RF modulated signal is directly down-converted to baseband after the mixer. Since the down-converted signal is centered at *0 Hz*, the baseband signal is subjected to the disturbance of dc operating point or "dc-offset" at the mixer output. There are many factors contributing to the dc-offsets, the major root causes are from circuit imperfections, for example an asymmetric differential circuit, mismatches of active or passive components, self-mixing of LO or RF leakage signals, even-order distortion of nonlinear active components, etc.

From the origins of dc-offsets, it can be categorized into two types, which are based on the time-varying nature of the offset.

Type I: Static DC-Offsets

These types of discrepancies usually result from the components' mismatches or multi-path errors, the offsets are usually time-invariant. The circuit solutions to these problems have been discussed in many references [4] – [7]. Basically, these can be categorized into the following approaches:

(a) ac coupling

(b) high-pass filtering;

(c) dc-calibration method;

(d) dc-cancellation method.

The feasibilities and effectiveness of these solutions strongly depend on the modulation scheme applying to the received signal. When the modulation scheme has no information content at dc, e.g. frequency shift keying, the solutions have less impact to the degradation of bit-error rate after the baseband signal processing. If the baseband signal happens to fall exactly on *0 Hz*, some information loss is unavoidable when method (a) and (b) are implemented. The ac-coupling and high-pass filtering will result finite response time and will cause significant loss in data frame of time-division multiple access system [4], [5]. The method (c) and (d) rely on the servo feedback mechanism to perform one-time or real-time dc-offset removal. Special attention needs to be taken when implementing the feedback circuits, so that the stability and the settling time can meet the timing requirements of the application [5].

Type II: Dynamic DC-Offsets

Aside from the static dc-offsets mentioned above, there is another scenario, which will generate time-variant dc-offset. This scenario arises from the finite isolation between the LO-port and RF-port in the receiver IC. When the leakage happens either from LO-to-RF port or from RF-to-LO port coupled with the nonlinearity of active devices as shown in Figure 2.5, the dynamic dc-offset will be produced at the mixer outputs due to self-mixing

of the signal and its own replica. This kind of time-varying dc-offset is difficult to be removed completely by any offset cancellation schemes.

The mechanism of the leakage signal can be illustrated in the following sections:

(a) LO – RF leakage

The LO – RF leakage mechanisms are illustrated in Figure 2.5. When the reverse isolation between the RF-port and LO-port is not high enough, the strong LO signal may leak to the RF front-end circuits. The LO leakage will be reflected whenever there is a mismatch of impedances between the interface of LNA and mixer (Figure 2.5 (a)) or between the interface of antenna and LNA (Figure 2.5 (b)). After the reflection, the LO leakage signal will travel to the RF-port of down-converter and mix with the actual LO signal, dc-offset is then produced at the output. There is another circumstance when the LO leakage radiate through the antenna and then reflects back by the nearby obstacle as shown in Figure 2.5 (c). This reflected wave is then received by the antenna and amplified by the LNA before mixing. Since the reflected wave by the obstacle may result in a change of the phase in the LO signal, the dc-offset caused by the self-mixing of radiated LO signal will also distort the phase information at the baseband.

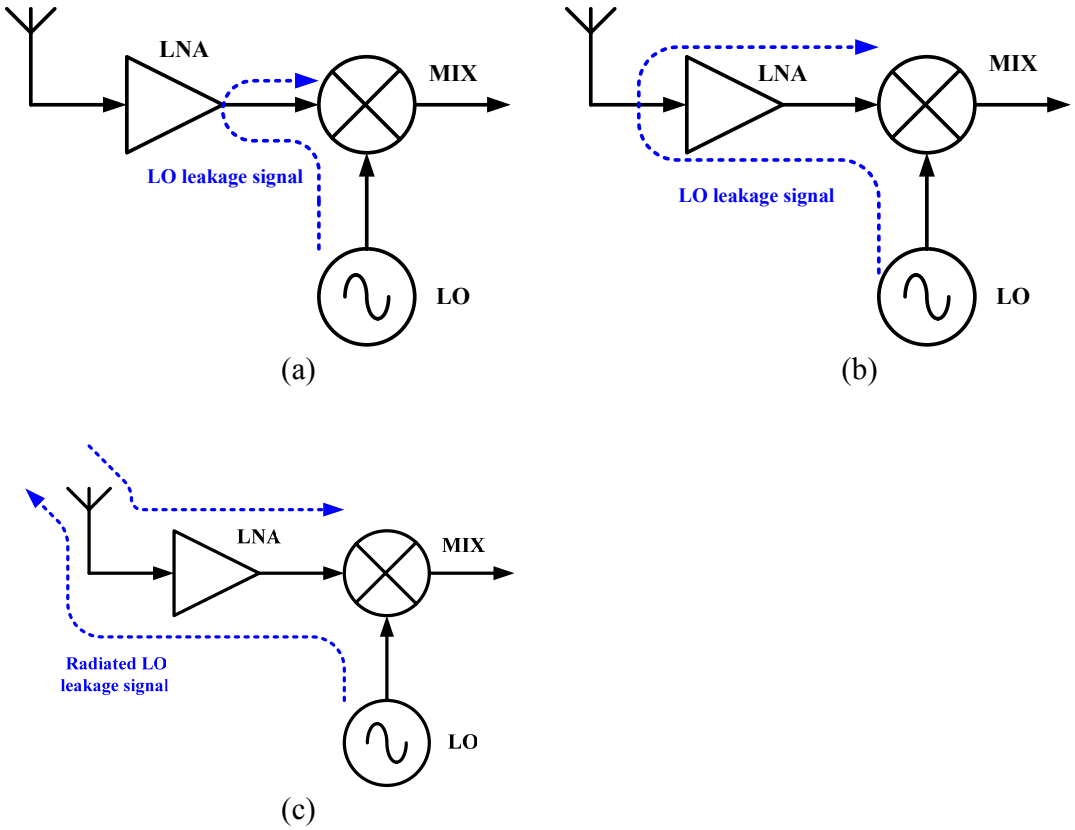


Figure 2.5 The mechanism of self-mixing due to LO – RF leakage. (a) Self-mixing due to reflected wave of LO – RF leakage from LNA output (b) Self-mixing due to reflected wave of LO – RF leakage from antenna port (c) Self-mixing due to receiving of radiated LO signal.

The mathematical formulation of these mechanisms is presented below. Assume that the modulated RF carrier signal (both amplitude and phase) and the LO signal are represented by $V_{RF}(t) = A_{RF}(t)\cos(\omega_c t + \theta(t))$ and $V_{LO}(t) = A_{LO}\cos(\omega_o t)$ respectively. The reflected wave of LO – RF leakage which suffers from phase delay, α, can be represented by $V_{LO\_leak}(t) = A_{LO\_leak}\cos(\omega_o t + \alpha)$.

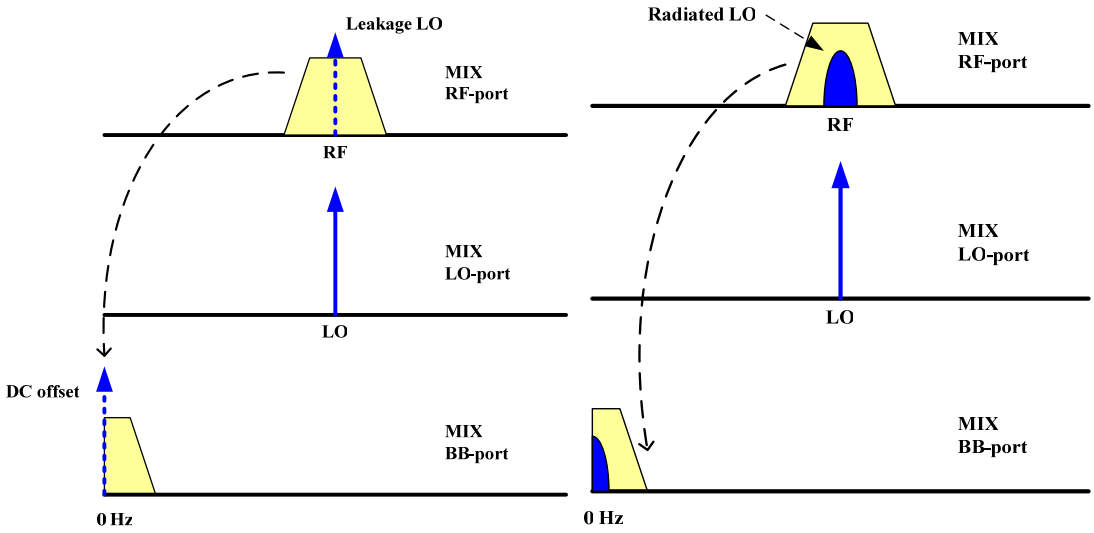
During the mixing process, the following frequency components are produced:

$$
\begin{aligned}
&\left[V_{RF}(t)+V_{LO\_leak}(t)\right]\times V_{LO}(t)\\
&=\left\{A_{RF}(t)\cos\left(\omega_c t+\theta(t)\right)+A_{LO\_leak}\cos(\omega_o t+\alpha)\right\}\times A_{LO}\cos(\omega_o t)\\
&=\frac{A_{RF}(t)A_{LO}}{2}\cos\left[\left(\omega_c-\omega_o\right)t+\theta(t)\right]+\frac{A_{RF}A_{LO}}{2}\cos\left[\left(\omega_c+\omega_o\right)t+\theta(t)\right]\\
&+\frac{A_{LO\_leak}A_{LO}}{2}\cos(\alpha)+\frac{A_{LO\_leak}A_{LO}}{2}\left[\cos(2\omega_o t)+\alpha\right]
\end{aligned}
\qquad (2.1)
$$

After the mixing, the low pass filter will reject the high frequency components of the baseband signal.

$$
\begin{aligned}
&\left[V_{RF}(t)+V_{LO\_leak}(t)\right]\times V_{LO}(t)\\
&\approx \underbrace{\frac{A_{RF}(t)A_{LO}}{2}\cos\left[\left(\omega_c-\omega_o\right)t+\theta(t)\right]}_{\textit{wanted signal}}+\underbrace{\frac{A_{LO\_leak}A_{LO}}{2}\cos(\alpha)}_{\textit{unwanted}\ \text{dc component}}
\end{aligned}
\qquad (2.2)
$$

The self-mixing of the reflected LO – RF leakage and the LO produces a dc-offset voltage at the mixer output as shown in Figure 2.6. The level of the dc offset is proportional to the product of the LO signal strength and its leakage. This offset may degrade the receiver performance because the offset voltage level is sometimes stronger than the received signal.



(a) (b)

Figure 2.6 The simplified spectrum diagram of RF – LO leakage. (a) LO signal leaks to RF-port of mixer and then down-convert to baseband. (b) The reflected LO signal is received by its own antenna and then down-convert to baseband.

(b) RF – LO leakage

Another leakage mechanism occurs from the RF–port to LO–port. This is seldom mentioned in the publications but it has a more damaging impact on the demodulation. The self-mixing of the RF signals due to RF – LO leakage happens when the amplified carrier signal after the LNA leaks to the LO-port and then reflects back and mixes with the carrier signal itself. The mechanism is illustrated in Figure 2.7. Because of the time-varying nature of the modulated carrier wave, the offset produced by this mixing effect is always changing with time, furthermore, the offset signal is not a pure dc but has a frequency bandwidth of two times of the original signal. The overlapping of this down-converted interferer on the desired baseband signal can seriously affect the demodulation and degrade the *SNR* significantly.

Assume that the leakage of RF signal to the LO port suffers from amplitude variation and phase change: $V_{RF\_leak}(t) = A_{RF\_leak}(t)\cos[\omega_c t + \alpha(t)]$

During the mixing process, the following frequency components are produced:

$$\begin{aligned} & V_{RF}(t) \times [V_{LO}(t) + V_{RF\_leak}(t)] \\ & = A_{RF}(t)\cos[\omega_c t + \theta(t)] \times \{A_{LO}\cos(\omega_o t) + A_{RF\_leak}(t)\cos[\omega_c t + \alpha(t)]\} \\ & = \frac{A_{RF}(t)A_{LO}}{2}\{\cos[(\omega_c + \omega_o)t + \theta(t)] + \cos[(\omega_c - \omega_o)t + \theta(t)]\} \\ & + \frac{A_{RF}(t)A_{RF\_leak}(t)}{2}\{\cos[2\omega_c t + \theta(t) + \alpha(t)] + \cos[\theta(t) + \alpha(t)]\} \end{aligned} \quad (2.3)$$

After the mixing and following the low pass filter, high frequency components of the baseband signal are rejected.

$$\begin{aligned} & V_{RF}(t) \times [V_{LO}(t) + V_{RF\_leak}(t)] \\ & \approx \underbrace{\frac{A_{RF}(t)A_{LO}}{2}\cos[(\omega_c - \omega_o)t + \theta(t)]}_{\text{wanted signal}} + \underbrace{\frac{A_{RF}(t)A_{RF\_leak}(t)}{2}\cos[\theta(t) + \alpha(t)]}_{\text{unwanted baseband signal}} \end{aligned} \quad (2.4)$$

The self-mixing of RF – LO leakage with the RF signal produces a time-varying modulated signal which falls into the baseband as shown in Figure 2.8. The bandwidth of this unwanted signal can be as large as twice the desired signal due to the multiplication of $A_{RF}(t)\, A_{RF\_leak}(t)$.

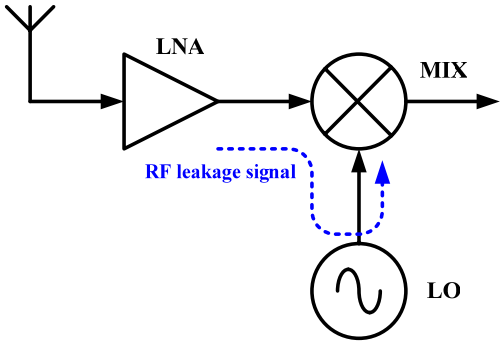


Figure 2.7 The mechanism of self-mixing due to RF leakage to LO port

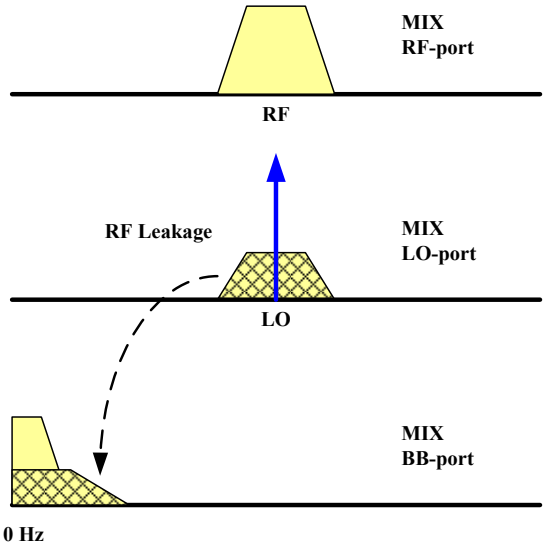


Figure 2.8 The spectrum diagram of the self-mixing of RF – LO leakage

2.3.1.2 Flicker Noise

The direct conversion receiver has only one frequency translation to baseband, the *SNR* after the down-conversion may not be as good as the superheterodyne receiver or low-IF receiver, which has multiple gain stages for signal amplification and filtering. As a result, there is always an issue for the direct conversion receiver. Besides dealing with the dc-offset, it also needs to combat with the low frequency flicker noise overlapping on the desired baseband signal centered at *0 Hz*.

The flicker noise effect is more obvious in CMOS process than in bipolar process. This low-frequency noise spectrum at the mixer output originates from the switching stage of the mixer and direct feedthrough of flicker noise from the driver stage during the imperfect switching among transistors. For short channel MOSFETs ($L_{\text{eff}} < 1\ \mu m$), the flicker noise can be significantly higher and the corner frequency can be as large as 1 MHz. This detrimental effect will degrade the *SNR* before the demodulation takes place. If the communication system has a narrow information bandwidth, the flicker noise can degrade the receiver performance considerably.

2.3.1.3 LO Leakage and Spurious Radiation

This is the problem unique to direct conversion receiver. Because of the same LO frequency and RF carrier frequency, the undesirable LO signal may leak through the front-end circuits and then radiate through the antenna as shown in Figure 2.5 (c). This radiated spurious signal will interfere with the nearby wireless handsets and disrupt the reception of the signal.

In order to pass the stringent type approval test specified in the ETSI document during the certification of the devices [3], this kind of electromagnetic interference needs to be sufficiently suppressed or shielded, so that the radiation level is controlled below a certain level. Another way of reducing the radiation is to improve the reverse isolation from the

LO to RF path, a low noise amplifier with good reserve isolation, S_{12}, can substantially reduce the LO leakage signal.

2.3.1.4 Intermodulation Products from Second-order Nonlinearity

In general, a receiver can only maintain as a linear system with limited range of input signal. The unwanted nonlinear products start to appear at the output of the system whenever the input signal becomes too large. Nonlinear products can also be generated because of the inherent nonlinear properties of active devices used in the receiver. The most important nonlinear frequency products include the harmonic components of the signal, *HD2* and *HD3*, which are generated from the distortion of one-tone input. There are other non-linear products as well, for example the second-order and third-order intermodulation products, *IM2* and *IM3*, which are generated by the two-tone inputs.

The harmonic distortion caused by gain compression of the system can be easily filtered off if the fundamental frequency is in the *GHz* range. However, the third-order intermodulation products from two-tone inputs (f_1 and f_2), such as ($2f_1 - f_2$) and ($f_1 - 2f_2$) can occur at the frequencies too close to the desired operating frequency band, hence, the interferers cannot be filtered easily after the mixing because the required Q-factor of the filter is too high and it is difficult to be realized by integrated circuit. This problem has been well presented in the literature, the solutions include the pre-select filter for rejecting the interferers before mixing or improving the linearity of the system by selecting a proper

biasing. In general, these effects can be characterized by *IIP3* and *OIP3* when designing the communication system.

For the second-order intermodulation products ($|f_1 - f_2|$), there is usually not a serious issue whenever the system is fully differential. The symmetrical nature of the differential circuit can cancel the common-mode terms generated by the active devices, however, the rejection of the *IM2* products are far from infinite because of the imbalances of the devices introduced during the fabrication process. The *IM2* products are usually in the low frequency range and these can be easily filtered out by a bandpass filter after the mixer in superheterodyne receiver or low-IF receiver. However, this situation becomes problematic for the direct conversion receiver because the *IM2* product may coincide with the baseband and affect the receiver performance.

There are two scenarios that can generate the *IM2* products. In the case (I), the *IM2* products are produced by two strong and close-by blockers passing through the nonlinear mixer. Because of the nonlinear property of the mixer, the two blockers experience the second-order distortion and produce the unwanted dc component and low frequency beat at $|f_1 - f_2|$. All these unwanted components fall into the baseband and there will corrupt the desired signal as shown in Figure 2.9.

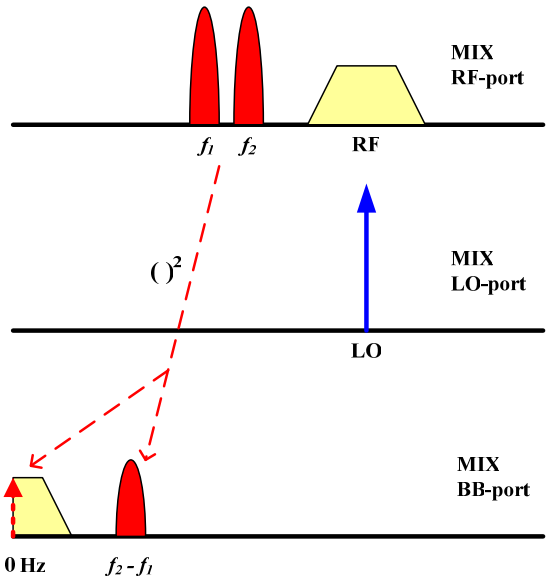


Figure 2.9 IM2 product from two-tone inputs

These effects can be modeled using Taylor series approximation:

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^2(t) + \cdots \tag{2.5}$$

where $y(t)$ and $x(t)$ represent the output signal and input signal of the system.

Neglecting the dc and higher order terms, the second-order distortion comes from the $a_2 x^2(t)$ term:

$$\begin{aligned} y(t) &= a_2 x^2(t) \\ &= a_2 \times A_{blk}^2 \left[\cos(\omega_1 t) + \cos(\omega_2 t)\right]^2 \\ &= a_2 A_{blk}^2 \left\{1 + \frac{1}{2}\left[\cos(2\omega_1 t) + \cos(2\omega_2 t)\right] + \cos\left[(\omega_1 + \omega_2)t\right] + \cos\left[(\omega_1 - \omega_2)t\right]\right\} \end{aligned} \tag{2.6}$$

After the mixing and followed by the low pass filter, the high frequency components of the baseband signal are rejected:

$$y_{baseband}(t) \approx \underbrace{a_2 A_{blk}^2}_{unwanted\ dc} + \underbrace{a_2 A_{blk}^2 \cos[(\omega_1 - \omega_2)t]}_{unwanted\ baseband} \tag{2.7}$$

The unwanted *IM2* components fall into the baseband and there are not possible to be filtered by the channel select filter. To reduce the *IM2* effect, the mixer needs to be as linear as possible and maintain good symmetry. RF bandpass filter inserted in between the LNA and mixer also could help suppressing the blocker signals before mixing, hence the *IM2* products are much lower than the desired signal at the baseband.

In the case (II), the unwanted baseband components are produced when a single-tone amplitude modulated blocker experiences the second-order distortion as shown in Figure 2.10 [11]. The mathematical analysis of this mechanism is shown below.

Assume that the single-tone blocker is represented by $[1+m(t)]A_{blk}\cos[\omega_{blk}t+\theta(t)]$. From the simplified Taylor series shown in Equation 2.6,

$$\begin{aligned} y(t) &= a_2 x^2(t) \\ &= a_2 \times \{[1+m(t)]A_{blk} \cdot \cos[\omega_{blk}t+\theta(t)]\}^2 \\ &= a_2 \cdot [1+m(t)]^2 \cdot A_{blk}^2 \cdot \left\{ \frac{1}{2} + \underbrace{\frac{1}{2}[\cos(2\omega_{blk}t+2\theta(t)]}_{high\ frequency\ component} \right\} \end{aligned} \tag{2.8}$$

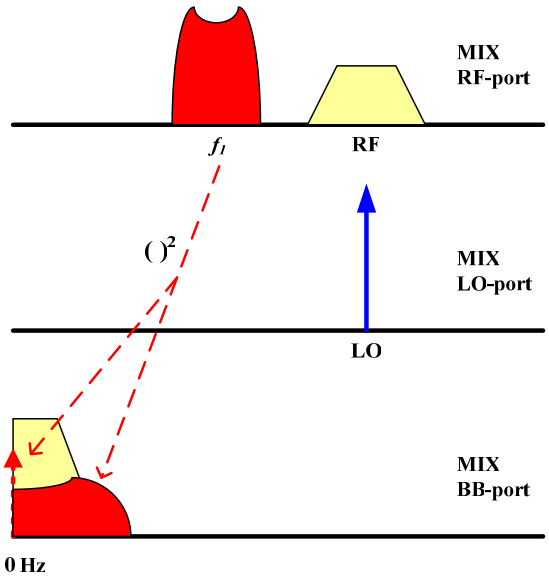


Figure 2.10 Single blocker envelope distortion

After the mixing and followed by the low pass filter, the high frequency components of the baseband signal are rejected:

$$y_{baseband}(t) \approx \underbrace{\frac{1}{2}a_2 A_{blk}^2}_{unwanted\ dc} + \underbrace{\frac{1}{2}a_2 A_{blk}^2\left[2m(t)+m^2(t)\right]}_{unwanted\ baseband} \tag{2.9}$$

The overlapping of the distortion products on the desired baseband can desensitize the receiver significantly.

2.4 Direct Conversion Receiver for W-CDMA System

2.4.1 Introduction

The recent demand of multi-mode (e.g. WLAN, GSM, GPRS, EDGE and W-CDMA) and multi-band (e.g. 900 MHz, 1.8 GHz and 2.14 GHz) handsets have changed the technology path projected by the wireless communication industry. The direct conversion receiver becomes the most promising solution to provide a common platform for different wireless applications. The advantages of the direct conversion receiver, such as simpler architecture and fewer number of off-chip components not only reduce the cost of a receiver but also allow different applications to coexist in the same receiver.

For narrowband applications, e.g. GSM, the implementation of the direct conversion receiver poses a very tough technical challenge for the circuit designers. The problems of dc-offset and flicker noise can dominate the receiver performance completely because fractional loss of signal content at baseband with dc-removal circuits may considerably affect the demodulation and decoding of the received signal. For W-CDMA application, the channel bandwidth is significantly wider than GSM, hence it is possible to implement the direct conversion receiver with a simpler dc-cancellation circuit. It is reported in [12], the dc notch filter with 2000 *Hz* cutoff frequency was realized to achieve the BER of 10^{-6} for W-CDMA direct conversion receiver.

The direct conversion receiver is an active research area for recent years. Many researchers have focused on SiGe bipolar technology, which shown superior performance in RF front-end design, lower flicker noise and better device matching of bipolar transistors also improve the production yield, hence many reported direct conversion receivers for W-CDMA are related to SiGe processes [12] ~ [17]. CMOS technology started to receive the attention from the research community in the last three years, [18] ~ [19]. The improvement of processing power of digital baseband circuits can compensate some of the performance degradation originated from RF CMOS circuits.

The typical block diagram of the direct conversion receiver is shown in Figure 2.11. Due to the project scope, only the RF front-end circuits, LNA and mixer, are discussed here.

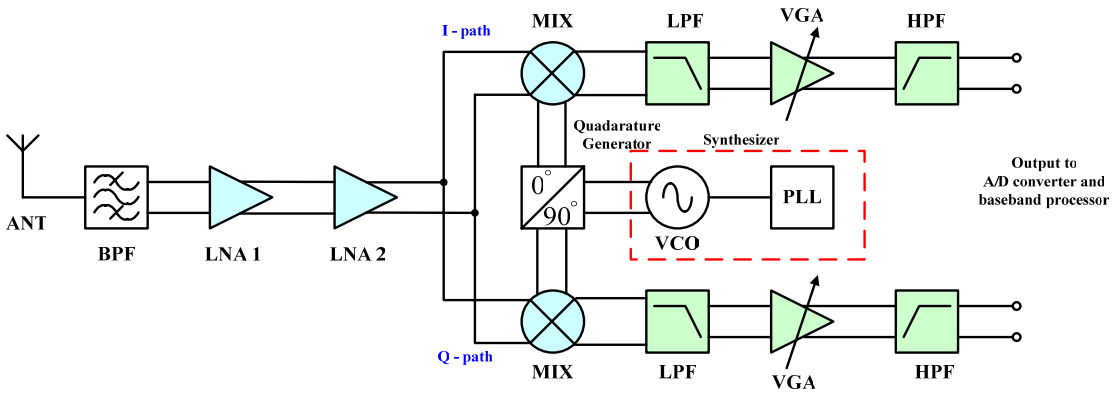


Figure 2.11 Typical direct conversion receiver for WCDMA application

2.4.2 System Considerations of Front-end Design

For the direct conversion receiver, the front-end design is straightforward because only one down-conversion of signal is involved as shown in Figure 2.12. Such a simpler design does not offer good immunity to interference and always requires superior performance from LNA and mixer, hence it is not suitable for CMOS IC implementation.

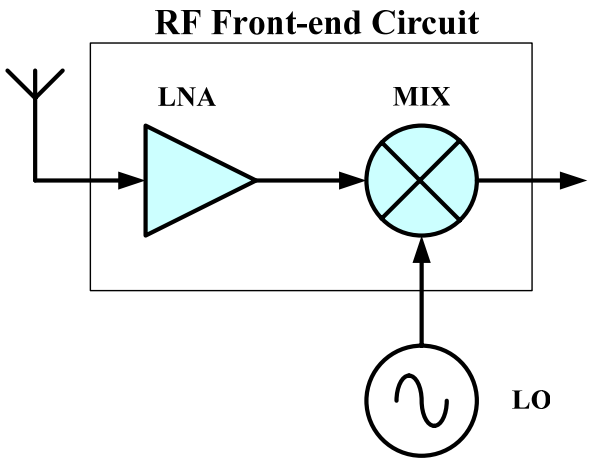


Figure 2.12 Typical front-end design of direct conversion receiver

The front-end design of any communication systems always involves the trade-offs among different electrical parameters such as gain, noise figure and linearity under the constraint of power consumption. These design trade-offs are not easily achieved for cellular applications as the power consumption of the receiver keeps reducing. For a highly integrated receiver to meet the stringent design specifications, some off-chip components are used in commercial products to compensate the drawbacks of integrated circuits. The most common off-chip components include duplexer, T/R switch, passive balun, RF

bandpass filter, etc. These bulky off-chip components not only occupy large PCB area, they also increase the bill-of-material and the cost of the receiver. As a result, it is necessary to minimize the number of off-chip components used in the front-end design. In the following sections, some issues associated with the front-end design are discussed.

2.4.2.1 Single-ended Input vs. Differential Input

Differential circuits are always implemented in the receiver IC, so that better common-mode rejection can be achieved. However, the majority of the antennas implemented in the handset are monopole and single-ended, which is in contrast to the differential input of the receiver. The interface between antenna and differential low noise amplifier requires off-chip balun or RF bandpass filter as a device to perform single-to-differential conversion (Figure 2.13). Because of the passive nature of the balun (or filter), the loss incurred by this device will be directly converted to an increment of system noise figure.

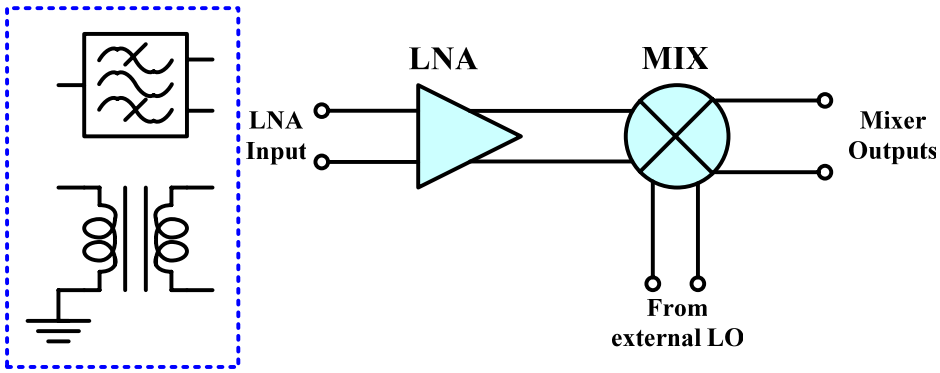


Figure 2.13 Fully differential RF front-end design

To remove the off-chip balun, the function of single-to-differential conversion is incorporated into the LNA as shown in Figure 2.14. By choosing the single-ended LNA

design, the interface between antenna and LNA can be straightforward. However, the multi-path (I/Q-path) approach for signal processing in DCR will require the differential signal before the down-conversion mixer, hence a single-to-differential conversion circuit is added after the LNA to split the amplified signal into two 180° out-of-phase signals. It is a challenge to design such a circuit operating in RF because the amplitude imbalance and phase error in the circuit needs to be compensated carefully without further degrading the noise figure of the front-end circuits.

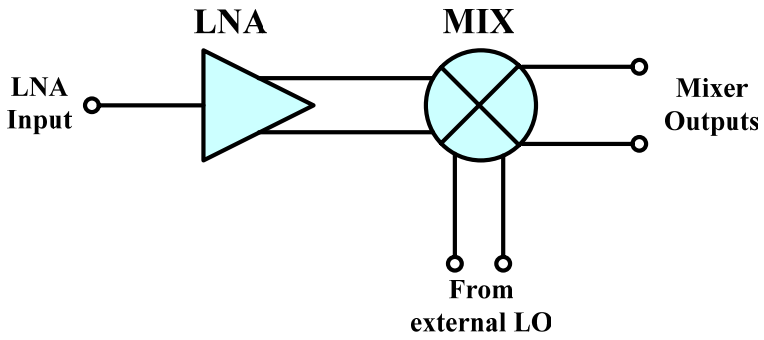


Figure 2.14 RF front-end with single-ended input

2.4.2.2 Reciprocal Mixing

In W-CDMA system, the receiver and transmitter are operating simultaneously to realize the full duplex communication. In order to avoid interference from each other, the received frequencies and transmitted frequencies occupy a different spectrum according to the frequency-division duplexing scheme. The minimum separation of these two frequency bands is 30 MHz. It can be seen from Figure 2.15 that an off-chip duplexer is necessary to isolate the receiver and transmitter, more than 40 dB of out-of-band rejection

is needed for the received and transmitted signal in their respective operating frequency bands.

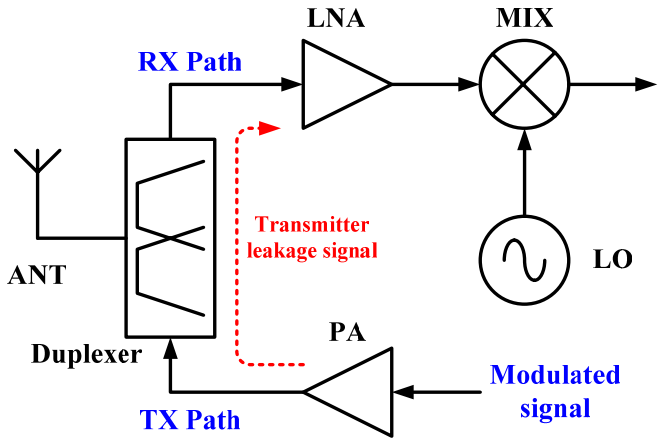


Figure 2.15 The typical front-end design of WCDMA transceiver

Although the duplexer can be used as the first level of isolation, the rejection of the transmit leakage may not be sufficient for the receiver because the strong leakage from transmitted signal may still appear at the receiver input through substrate coupling. This scenario is similar to the blocker test when a receiver faces desensitization the problem due to a strong nearby signal. If the far-out phase noise of the transmitted spectrum is too high, it may fall into the received band and seriously impact the demodulation after the mixing (Figure 2.16). This scenario is called “reciprocal mixing” [21] and it appears to be the most thorny issue in W-CDMA system.

The reciprocal mixing is very similar to the issue caused by the second-order nonlinearity discussed in the previous section. To alleviate the desensitization of the receiver due to the strong transmitted blocker signal, the mixer in a DCR needs to operate in a very linear

manner, hence the requirement of the input second-order intercept point could be very stringent, i.e. IIP2 > 60 dB [11]. It is a very challenging task to realize this design goal in CMOS due to the poor matching of sub-micron devices and low substrate isolation.

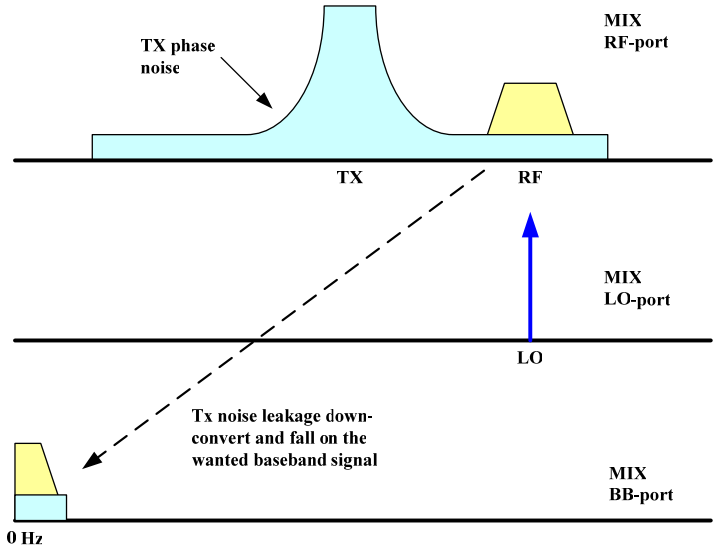


Figure 2.16 Strong blocker arisen from the leakage of transmitter signal

The alternative way of relaxing the IIP2 requirement is to add a RF bandpass filter in between the LNA and mixer as shown in Figure 2.17 (a) for suppressing the blocker signal originated from the transmit leakage. Since the required Q-factor for this RF filter is more than 37 and need to achieve 40 dB of rejection at the transmit frequency range, it is very difficult to be realized on-chip, hence an off-chip SAW filter is usually selected. The disadvantage associated with this filter is an insertion loss, which would degrade the system noise figure and attenuate the passband signal level. To circumvent this issue, another RF amplifier is added after the BPF in Figure 2.17 (b) to amplify the received signal and improve the *SNR* before the mixer. The alternative solution is to increase the

LNA gain before the lossy filter but this would significantly degrade the linearity performance when the input signal is large.

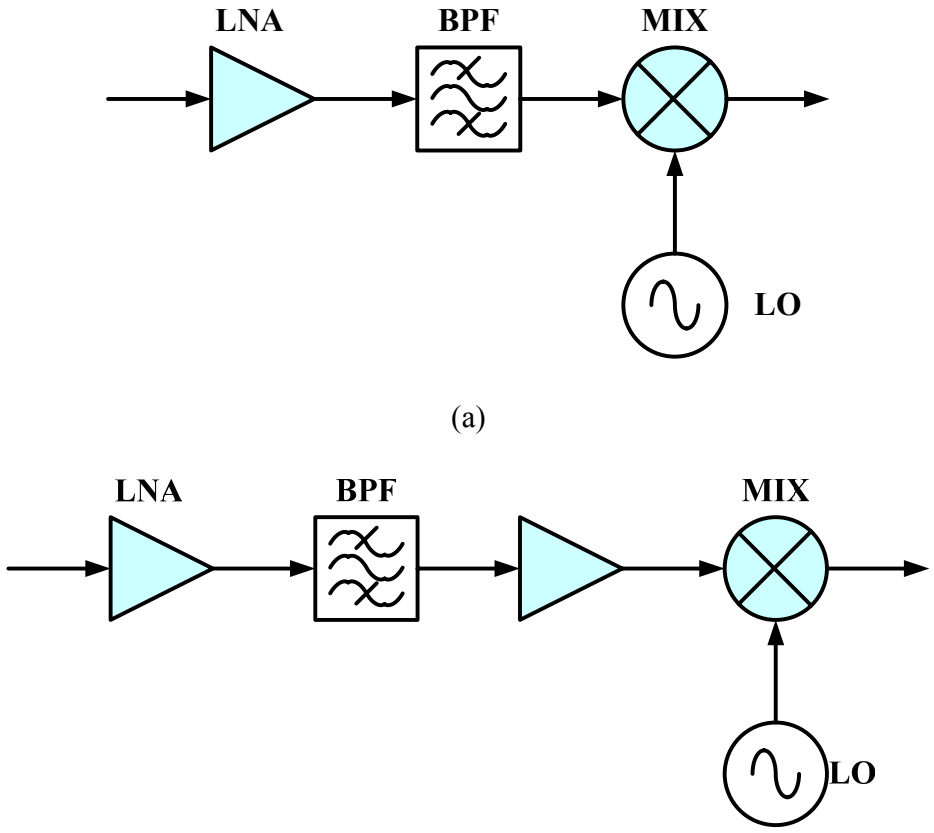


Figure 2.17 An alternative way to reduce the effect of a strong out-of-band blocker

2.5 System Plan for Direct Conversion Receiver

System budgeting of the receiver is a very essential step to ensure the receiver complying with the technical requirement stated in ETSI documents [3]. In this section, the system requirements of direct conversion receiver for the W-CDMA are analyzed and the design targets are derived.

2.5.1 System Requirements of W-CDMA Receiver

The interpretation of the W-CDMA communication protocol and the conversion of the RF link budget into the system requirements of the receiver are not covered in this project. The reader can refer to publications [22] – [26] for the detailed derivations of system requirements on noise figure, adjacent channel selectivity, second-order intercept point, third-order intercept point, and image-rejection ratio. Table 2.2 summarizes the requirements for the W-CDMA receiver based on the research work reported in [22].

Table 2.2 Summary of the system requirements of W-CDMA receiver

Parameter	**Description**	**Freq. Deviation ($f_c \pm \Delta f$)**	**Entire Receiver**	**Unit**
Sens.	Reference sensitivity	-	-114	*dBm*
$(SNR)_{out,min}$	Output SNR of receiver	-	7	*dB*
$P_{in(max)}$	Max. input level	-	-25	*dBm*
NF	Noise figure	-	≤ 9	*dB*
	In-band Selectivity			

$ACS_{(5MHZ)}$	1st Adjacent Channel	5 MHz	≥ 33	*dB*
$ACS_{(CW)}$	CW Interferer	5 MHz	≥ 58	*dB*
$ACS_{(15MHz)}$	3rd Adjacent Channel	15 MHz	≥ 58	*dB*
$ACS_{(20MHZ)}$	Modulation Blocker	>15 MHz	≥ 58	*dB*
	Intercept Point			
$IIP2_{(10MHz)}$	2nd-order Intercept Point	10 MHz	≥ -16	*dBm*
$IIP2_{(15MHz)}$	2nd-order Intercept Point	15 MHz	≥ +8	*dBm*
$IIP2_{(TX)}$	2nd-order Intercept Point	Tx	≥ +47	*dBm*
$IIP3_{(10/20MHz)}$	3rd-order Intercept Point	10/20 MHz	≥ -17	*dBm*
$IIP3_{(67/134MHz)}$	3rd-order Intercept Point	67.4/134.8 MHz	≥ -8	*dBm*
IRR	Image Rejection Ratio	>85 MHz	≥ 84	*dB*

The different IIP2 and IIP3 requirements come from the in-band and out-of-band interferers specified in the type approval tests outlined in [3].

2.5.2 Gain Budget of Direct Conversion Receiver

To determine the front-end system requirements, the performance of baseband circuits are required. However, baseband designs are beyond the project scope, hence, the experimental results of baseband circuit listed in [2] is used as a reference for gain budgeting of the front-end design. The critical parameters used in the system calculation are listed in Table 2.3. It is assumed that a variable gain amplifier and a channel select filter are used in the receiver chain as shown in Figure 2.11. The variable gain amplifier provides the feature of automatic gain control when the input signal varies. Gain control is realized by the demodulator, which uses the analog-digital converter to monitor the output signal level. With the channel select filter, it is assumed that the out-of-band interferers will be fully suppressed without affecting the receiver performance.

Table 2.3 Baseband (VGA and filter) performance reported in [2]

Parameter	Description		Unit
G_{BB}	Voltage gain range	-9 ··· +69	dB
NF_{BB}	Noise figure	27	dB
$IIP3_{BB}$	Input 3rd-order intercept point	+14	dBm
$IIP2_{BB}$	Input 2nd-order intercept point	+60	dBm

To obtain the design targets for the RF front-end circuit, a simpler hand calculation is performed here. From Table 2.2, the minimum dynamic range, DR_{min}, and minimum front-end gain, $G_{RFE(min)}$, are calculated as follows.

$$\begin{aligned} DR_{\min} &= Max.\ Input\ Level - \text{Reference Sensitivity} \\ &= -25 - (-114) \\ &= 89\,(\text{dB}) \end{aligned} \tag{2.10}$$

$$\begin{aligned} G_{RFE(\min)} &= DR_{\min} - G_{BB(\max)} \\ &= 89 - 69 \\ &= 20\,(\text{dB}) \end{aligned} \tag{2.11}$$

To achieve the dynamic range of 89 dB, the minimum front-end gain must be greater than 20 dB. As discussed earlier, the number of high frequency gain stages for DCR is less than other receiver topologies, hence the *SNR* at the mixer output may not be sufficient for the baseband circuits. Although the VGA can provide higher gain for the downconverted signal to meet the input requirement of the ADC, this scenario is always accompanied by a large dc-offset seen by the ADC because the dc-offset produced by the mixing process will also be amplified. To circumvent this issue, the front-end gain for DCR needs to be as

high as possible. However, for front-end gain of more than 30 dB, the circuits may become unstable due to poor reverse isolation.

From Table 2.2, the total noise figure of the receiver cannot exceed 9 dB. Assuming 3 dB loss from the duplexer, the noise figure of the receiver IC must be below 6 dB. Although the minimum front-end gain is only 20 dB, another 3 dB is added to compensate for the signal loss at the duplexer. For the purpose of reliable operation, 3 dB of design margin is provided, hence 26 dB of gain is assigned to front-end circuits.

To obtain the required noise figure of the front-end circuit, Friss' formula expressed in Equation (2.12) is applied [21], [50].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \times G_2} + \cdots + \frac{F_n - 1}{G_1 \times G_2 \times \ldots \times G_{n-1}} \tag{2.12}$$

It is noted that all the variables in Friss' formula are dimensionless. The conversion of noise figure and gain in decibel to magnitude are shown in the following equations.

$$NF_{(dB)} = 10 \times \log(F) \Rightarrow F = 10^{NF_{(dB)}/10} \tag{2.13}$$

$$G_{(dB)} = 10 \times \log(G) \Rightarrow G = 10^{G_{(dB)}/10} \tag{2.14}$$

Since only three gain stages are involved, Equation (2.12) is simplified into Equation (2.15), where NF_{FE}, F_{sys}, $F_{Duplexer}$, F_{FE}, F_{BB}, $G_{Duplexer}$ and G_{FE} represent the front-end noise

figure, system noise factor, noise factor of duplexer, noise factor of front-end circuits, noise factor of baseband circuit, duplexer gain and front-end gain respectively.

$$
\begin{aligned}
&F_{sys} = F_{Duplexer} + \frac{F_{FE} - 1}{G_{Duplexer}} + \frac{F_{BB} - 1}{G_{Duplexer} \times G_{FE}} \\
&\Rightarrow F_{FE} = G_{Duplexer} \times \left(F_{sys} - F_{Duplexer} - \frac{F_{BB} - 1}{G_{Duplexer} \times G_{FE}} \right) + 1 \\
&\Rightarrow F_{FE} = 10^{-3/10} \times \left(10^{6/10} - 10^{3/10} - \frac{10^{27/10} - 1}{10^{-3/10} \times 10^{26/10}} \right) + 1 \\
&\Rightarrow F_{FE} = 2.725
\end{aligned}
\tag{2.15}
$$

$$
NF_{FE} = 10 \times \log\left(F_{FE}\right) = 4.353 \quad \text{(dB)} \tag{2.16}
$$

For the third-order intercept point, the following equation is used [50]. All the IIP3 terms described in the equation (2.17) are expressed in power (W):

$$
\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 \times G_2}{IIP3_3} + \cdots + \frac{G_1 \times G_2 \times \cdots \times G_{n-1}}{IIP3_n} \tag{2.17}
$$

$$
IIP3_{(dBm)} = 10 \times \log\left(IIP3 / 0.001\right) \Rightarrow IIP3 = 0.001 \times 10^{IIP3_{(dBm)}/10} \tag{2.18}
$$

The general form of the *IIP3* equation can be modified into Equation (2.19). Here $IIP3_{sys}$, $IIP3_{Duplexer}$, $IIP3_{FE}$, $G_{Duplexer}$, and G_{FE} represent the system *IIP3*, duplexer *IIP3*, *IIP3* of front-end circuit, gain of duplexer and front-end gain respectively. The calculated IIP3 for the front-end circuit is -19 dBm, however, 3 dB of design margin is added to cater for some process variations and inaccuracy of the calculation.

$$\frac{1}{IIP3_{sys}} = \frac{1}{IIP3_{Duplexer}} + \frac{G_{Duplexer}}{IIP3_{FE}} + \frac{G_{Duplexer}G_{FE}}{IIP3_{BB}}$$

$$\Rightarrow \frac{1}{IIP3_{FE}} = \frac{\left(IIP3_{sys}\right)^{-1} - \left(IIP3_{Duplexer}\right)^{-1} - G_{Duplexer}G_{FE} \cdot \left(IIP3_{BB}\right)^{-1}}{G_{Duplexer}}$$

$$\Rightarrow \frac{1}{IIP3_{FE}} = \frac{10^{-IIP3_{sys}/10} - 10^{-IIP3_{Duplexer}/10} - \left(10^{G_{Duplexer}/10} \times 10^{G_{FE}/10} \times 10^{-IIP3_{BB}/10}\right)}{10^{G_{Duplexer}/10}} \quad (2.19)$$

$$\Rightarrow \frac{1}{IIP3_{FE}} = \frac{10^{-17/10} - 10^{-\infty} - \left(10^{-3/10} \times 10^{26/10} \times 10^{-14/10}\right)}{10^{-3/10}}$$

$$\Rightarrow \frac{1}{IIP3_{FE}} = 84151$$

$$\Rightarrow IIP3_{FE} = 1.188 \times 10^{-5}$$

$$IIP3_{FE} = 10 \times \log\left(IIP3_{FE} / 0.001\right) = -19.251 \quad \text{(dBm)} \quad (2.20)$$

The calculations of the system parameters are summarized in Table 2.4.

Table 2.4 The hand calculated receiver plan

Parameter	**Duplexer**	**LNA + MIX**	**Filter + VGA**	**Total**	**Unit**
Gain	-3	26	69	89	dB
NF	3	4.4	27	6	dB
IIP3	∞	-19.3	14	-17	dBm

Table 2.4 shows the minimum requirements for the front-end circuit to meet the W-CDMA system requirement. To achieve better performance, more stringent design targets for the RF front-end are tabulated in Table 2.5.

Table 2.5 Design goals of the RF front-end circuit for the W-CDMA application

Parameter	**Description**	**Design Goal**	**Unit**
f_c	Operating frequency	2110 – 2170	*MHz*
G	Gain	26	*dB*
NF	Integrated noise figure	4.3	*dB*
IIP2	Input 2nd-order intercept point	>30	*dBm*
IIP3	Input 3rd-order intercept point	-16	*dBm*
P_{1dB}	1-dB gain compression point	-26	*dBm*
$G_{LO\text{-}RF}$	LO-RF isolation	>60	*dB*
S_{11}	Input reflection coefficient	<-10	*dB*
I_d	Current consumption	20	*mA*

Chapter 3 RF Front-end Circuits

3.1 Introduction

The successful implementation of RF circuit depends on many factors, such as system planning, process technology, etc [21]. When the circuits operate in radio frequencies, undesirable side effects from active and passive devices start to arise and dominate the performance eventually. Noise, bandwidth, nonlinearity and parasitic capacitance associated with the RF circuit elements will deteriorate as operating frequencies enters the GHz range. The use of a deep-submicron CMOS process for RF designs can provide some performance compensation due to a higher unity-gain cutoff frequency, a better transconductance and a smaller parasitic capacitance associated with the active devices. However, these benefits do not come without penalty in other aspects. The following effects, which will be discussed in details, are especially essential to the circuits' performance:

3.1.1 Trade-offs Between the Noise Figure and Linearity

When a battery-powered wireless receiver operates in a hostile outdoor environment, maintaining good reliability and quality during the communication is always the

challenging task for the RF circuits' designer. For cellular communication, the receiver must be able to cope with two kinds of situations. In the first scenario, the user's wireless terminal is far away from the base station and the received signal can be as low as -114 dBm. In another scenario, the received signal is too strong (i.e. -25 dBm) for the receiver because the user terminal is near to the base station. In both situations, the qualities of the communication can be considerably degraded if the receiver does not have good sensitivity and linearity. The extreme working conditions of the receiver can be represented pictorially by the noise floor and the input third-order intercept point as shown in Figure 3.1.

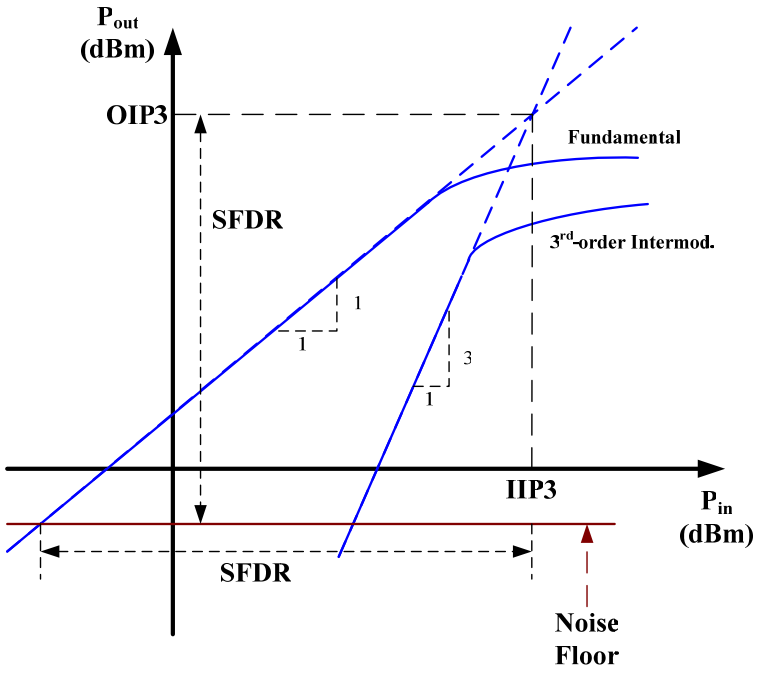


Figure 3.1 Graphical representation of spurious-free dynamic range

When the wireless terminal is operating in weak signal condition, the receiver performance is determined by the sensitivity, which also defines the minimum input signal

level, $P_{in,min}$, the receiver can operate. Its relationship with the circuit parameter (*NF*) and system parameters (*BW* and *SNR*) are shown in Equation (3.1).

$$P_{in,\min} = -174 + NF + 10\log(BW) + (SNR)_{\min} \tag{3.1}$$

The magnitude of -174 in Equation (3.1) is expressed in dBm/Hz, which is model from the input thermal noise generated from the antenna when it is operated at 290K [54]. The noise figure can be further linked to the *SNR* of the system by Equation (3.2).

$$F = 10^{NF/10} = \frac{(SNR)_{in}}{(SNR)_{out}} \tag{3.2}$$

where

F	is noise factor of the receiver with dimensionless unit
$(SNR)_{in}$	is defined as signal-to-noise ratio at the input of receiver
$(SNR)_{out}$	is defined as signal-to-noise ratio at the output of receiver
$(SNR)_{min}$	is defined as minimum required signal-to-noise ratio at the output of the receiver for demodulation

Since the *BW* and $(SNR)_{min}$ requirement for the demodulator input are pre-determined by the communication protocol, *NF* becomes the only design parameter linked to the receiver circuitry. It is obvious that good sensitivity can only be achieved when the noise figure of the receiver is kept below 4.3 dB.

When the receiver is operating in large signal condition, the linearity is usually characterized by the third-order intercept point, P_{IIP3}, and 1-dB power compression point, P_{1dB}. Both define the maximum input power level that the receiver can operate under the influences of two-tone and one-tone interferer.

The difference between noise floor and the intercept point is defined as spurious-free dynamic range, *SFDR*. The relationship among *SFDR*, the third-order intercept point, noise floor, operating bandwidth and *SNR* required for the demodulation can be linked by Equation (3.3). Here, the noise floor is represented by the noise figure, *NF*.

$$SFDR = \frac{2}{3} \times \left[P_{IIP3} + 174 - NF - 10\log(BW) \right] - SNR_{\min} \qquad (3.3)$$

SFDR is the most important design merit for characterizing the receiver, it shows how well the receiver responds to the variations of signal level during the operation. To make the receiver versatile in hostile environment, a large *SFDR* is highly desirable. As shown in Figure 3.1, this objective can be achieved by reducing the *NF* and increasing the P_{IIP3}. However, these improvements cannot be realized simultaneously in most of the situations. These dilemmas in RF system design will be further illustrated by the example, which is based on a single short-channel NMOS transistor operated in common-source topology.

When an NMOS transistor is operated in the saturation region under the common-source connection, *I-V* characteristic and transconductance of the short channel device can be represented by Equation (3.4) and Equation (3.5) respectively [29]. The ratio of

transconductance-to-drain current is defined as current efficiency, the expression is shown in Equation (3.6). One of the key challenges in CMOS circuit design is to design high-quality RF circuits with a low transconductance-to-current ratio [27].

$$I_{d,sat} = W v_{sat} C_{ox} \frac{V_{od}^2}{V_{od} + E_{sat} L} \tag{3.4}$$

$$g_{m,sat} = W v_{sat} C_{ox} \mu_0 V_{od} \frac{\mu_1 V_{od} + 4 v_{sat} L}{\left(\mu_1 V_{od} + 2 v_{sat} L\right)^2} \tag{3.5}$$

$$\frac{g_{m,sat}}{I_{d,sat}} = \frac{1}{V_{od}} \cdot \left[1 + \frac{1}{1 + \left(\frac{\mu_1 V_{od}}{2 v_{sat} L} \right)} \right] \tag{3.6}$$

$$\Rightarrow \frac{g_{m,sat}}{I_{d,sat}} = \frac{C}{V_{od}} \Rightarrow g_{m,sat} \times V_{od} = C \cdot I_{d,sat}$$

where V_{od} represents the gate overdrive voltage and C is a constant between 1 and 2 when v_{sat} is changed from 0 to ∞. Here, the device parameters related to short channel effects, such as v_{sat}, E_{sat}, μ_{eff}, μ_o and θ represents the saturation velocity, velocity saturation field strength, effective mobility, low field mobility and fitting parameter respectively.

$$V_{od} = V_{gs} - V_t \tag{3.7}$$

$$E_{sat} = 2 v_{sat} / \mu_{eff} \tag{3.8}$$

$$\mu_{eff} = \frac{\mu_0}{1 + \theta V_{od}} \tag{3.9}$$

$$\mu_1 = \mu_0 + 2\theta v_{sat} L \tag{3.10}$$

The receiver parameters such as input *IIP3* and minimum noise factor, F_{min}, of a single transistor operating in common-source mode are derived in [28] and [29]. For the *IIP3*, the following equation is given. It is noticed that the input third-order intercept point is directly proportional to gate overdrive (i.e. $P_{IIP3} \propto V_{od}$) from Equation (3.11).

$$P_{IIP3} = \frac{8}{3} \cdot \frac{v_{sat} L}{\mu_1 R_s} \cdot V_{od} \cdot \left(1 + \frac{\mu_1 V_{od}}{4 v_{sat} L}\right) \cdot \left(1 + \frac{\mu_1 V_{od}}{2 v_{sat} L}\right)^2 \tag{3.11}$$

For the minimum achievable noise factor, expression (3.11) shows that the $F_{\min}$ is inversely proportional to the unity-gain cutoff angular frequency, ω_T, which is also closely related to the transconductance of the transistor. Thereby a lower $F_{\min}$ can be achieved by shrinking the device length but this approach also results in higher biasing current and higher transconductance (i.e. $F_{\min} \propto 1/g_{m,sat}$).

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \left(\frac{\omega}{\omega_T}\right) \sqrt{\delta \gamma \left(1 - |c|^2\right)} \tag{3.12}$$

$$\omega_T \approx \frac{g_{m,sat}}{C_{gs}} = \frac{3}{2} \cdot \left(\frac{v_{sat} \mu_0}{L}\right) \cdot V_{od} \cdot \frac{\mu_1 V_{od} + 4 v_{sat} L}{\left(\mu_1 V_{od} + 2 v_{sat} L\right)^2} \tag{3.13}$$

To extend the *SFDR*, the common-source transistor needs to be operated at high V_{od}, so that P_{IIP3} can be made as large as possible. On the other hand, F_{min} needs to be as small as possible by increasing the $g_{m,sat}$. As long as the current, $I_{d,sat}$, is kept constant as shown in

equation (3.6), the trade-off of 3rd-order intercept point and minimum noise factor becomes inevitable. The simultaneous improvement of both P_{IIP3} and F_{min} can only be realized by increasing the biasing current, $I_{d,sat}$. For the portable devices, this may not be a feasible solution as higher current consumption has significant impact on the battery life and reduces the operating time of the devices.

3.1.2 RF Modeling Issues

The successful implementation of integrated circuits is closely related to the models used in the simulation. This is extremely important for RF circuits because the measured performances can deviate considerably from the simulation if the model lacks the accuracy and the sophistication to represent the characteristics of circuit elements and RF phenomena. Currently, the industrial standard of CMOS model for simulation is based on *Berkeley Short-Channel IGFET Model for MOS Transistors version 3.3* (BSIM3v3), which originates from University of Berkeley, California. However, this physics-based model does not account for some high-frequency effects such as gate resistance, transconductance delay, high frequency noise, etc [30]. Parasitic components arising from the metal connections and the contributions of the lossy substrate are also not included in the original model. Usually, these effects can be represented by adding lumped elements on top of the BSIM3v3 model of the intrinsic transistor core. The empirical model is used for curve fitting of the measured data, hence the parameters of the element are layout dependent. Furthermore, the induced gate noise effect is not accounted for in BSIM3v3

[28], the simulated noise figure of the transistor will be under-estimated and this would have significant impact on the design of a low noise amplifier.

In this project, IME in-house RF models, which are based on Chartered Semiconductor Manufacturing 0.35μm CMOS process, are used in the design. One of the drawbacks of these models is the lack of scalability in dimension. Only limited choices of transistor width (5 μm and 10 μm) and finger numbers are available, hence the design freedom is strictly limited.

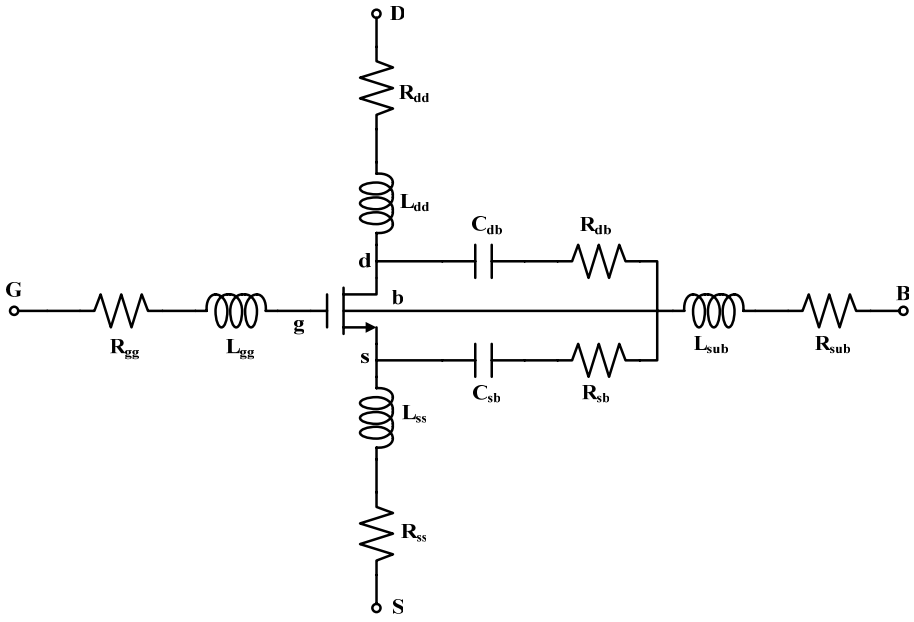


Figure 3.2 The RF model and substrate network of NMOS transistor [51]

3.2 Design of Low Noise Amplifier

3.2.1 Introduction

The low noise amplifier (LNA) is usually the first functional block in the receiver chain and, as a result, its performance is always crucial to the receiver sensitivity. Since the modulated RF signal received by the antenna is usually weak and noisy, signal boosting is always required for improving the signal-to-noise ratio before it can be further down-converted to the baseband and processed by the analog-to-digital converter.

For the direct conversion receiver shown in Figure 2.11, there are very stringent requirements placed on the LNA block. The typical signal gain of a LNA is usually 25 ~ 30 dB for a DCR, which is 5 ~ 10 dB more than other receiver topologies. The main reason to require a high gain for a DCR front-end is due to fewer high frequency gain stages than heterodyne receiver or low-IF receiver. After the LNA, the RF modulated signal is directly mixed by the LO and down-converted to baseband (or zero-IF) in a DCR, dc-offset will be generated at the outputs of the mixer if component mismatches or signal leakages happen during the frequency translation process. Any signal amplification after the mixer not only will boost up the desired signal level but also the dc-offset at the same time, as a result, it is not an effective way to improve the *SINAD* (*Signal /(Noise+Distortion)*) of the received signal. Although such impairments can be minimized by various dc-offset removal schemes, the effect of offset cannot be nullified completely,

and the residue will still partially impair the performance of a DCR. To circumvent the dc-offset problem, the gain of the LNA needs to be kept at a high level for improving the received signal quality before down-conversion as well as suppressing the electrical noise arisen from the subsequent stages.

3.2.2 Design Considerations

The most important design parameters for an LNA are power gain and noise figure. Linearity is usually not a major design issue. To achieve the design goals, the LNA circuit topologies need to be studied thoroughly.

Single-ended vs. Differential Design

An LNA can be realized by single-ended or differential topology. A single-ended LNA offers lower noise figure because of simpler design. For a differential LNA, at least twice of the power consumption of single-ended design is needed to achieve the same noise figure. However, from the system point of view, single-ended design does not offer any immunity to common-mode interferences, it is easily affected by the disturbance on the supply line and ground return path.

Active balun vs. passive balun

If the multi-path I/Q signal processing technique is utilized, the output signal of a single-ended LNA must be converted to a differential signal before the double-balanced mixer. The signal conversion can be realized by a passive balun or an active balun. For a passive

balun, the differential signal is produced by a discrete and wideband power divider or center-tapped transformer. This method is seldom used in integrated circuit because the required area for passive elements can be quite large, so it is mostly applied in microwave engineering. Furthermore, a passive balun is always lossy and presents higher noise figure. On the contrary, an active balun not only can produce the differential signal, it also can provide additional gain and a lower noise figure during the differential conversion [34] – [36]. However, it is a challenging task to maintain the 180° balanced signals at RF frequency, any parasitic capacitance associated with the active balun circuit has to be taken care of. This method is only effective if the circuit is operated in narrowband.

3.2.3 Circuit Topologies

As stated in the previous section, an LNA with a low noise figure and high power gain is essential to the receiver performance. However, many design approaches applied to low frequency amplifiers cannot be utilized for the LNA design. Impedance matching, circuit stability and noise issue are easily degraded when the circuit complexity is increased. As a result, simpler circuit topologies with superior transistor characteristics are always critical to realize the low noise amplifier. For cellular applications such as W-CDMA, the LNA is mostly implemented in GaAs MESFET transistor or BJT fabricated from SiGe or silicon process. These types of transistors possess better g_m, higher f_T and lower F_{min} than a conventional CMOS process. Although the deep submicron CMOS process has significantly improved the transistor performance, it is still a challenging task to design the LNA with a 0.35 μm NMOS transistor.

Two different LNA design approaches are selected in this project. In the first design, a single-ended LNA is adopted and followed by the active balun for producing a differential signal. By choosing the single-ended design, not only the interface issue with the antenna can be avoided, it also increases the integration level. For the second design, a two-stage cascaded differential LNA is implemented so that symmetrical signal paths can be maintained before down-conversion. Although the balanced structure can improve the IP2 performance of the front-end circuit, the differential LNA needs an off-chip balun to interface with the antenna.

3.2.3.1 Low Noise Amplifier

To design the LNA operated in RF, the common circuit topologies include common-source, common-source with resistive feedback, common-gate [32] and cascode topologies (Figure 3.3). The common-source approach (Figure 3.3 (a)) can achieve the lowest noise figure but it faces stability issues at high frequencies because of poor reverse isolation arising from Miller effect. By adding the shunt feedback resistor as shown in Figure 3.3 (b), the stability of common-source amplifier can be improved but a higher noise figure is expected. If the requirement of noise figure is not stringent, the common-gate approach (Figure 3.3 (c)) can be utilized because the input matching can be simplified by designing the input transistor to match the source impedance (i.e. $Z_{in} = Z_s = 1/g_{m,in}$) directly.

To overcome the stability problem and achieve a low *NF*, the cascode topology shown in Figure 3.3 (d) is considered as an alternative solution. Although it has slightly higher noise figure, it also offers a wider operating bandwidth and better reverse isolation than the common-source topology. In this project, a modified cascode amplifier is used as LNA for single-ended and differential design.

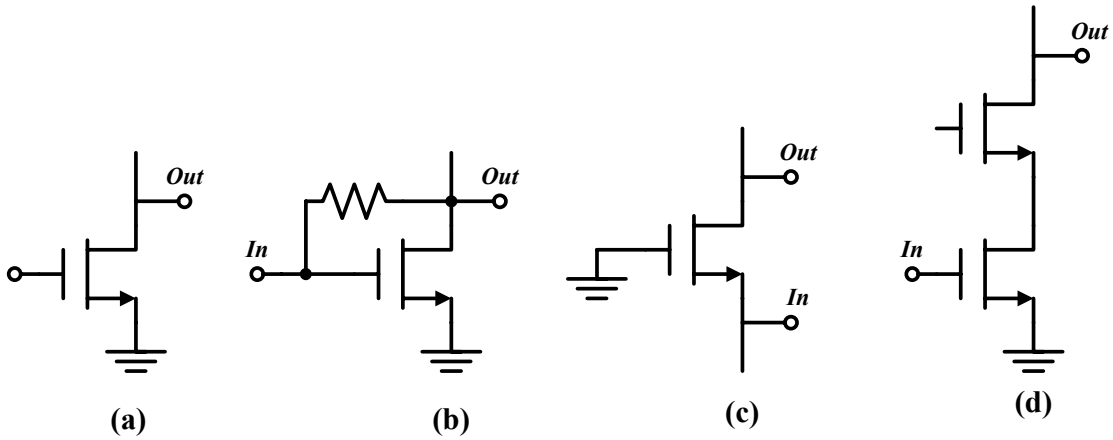


Figure 3.3 The circuit topologies of CMOS LNA design: (a) common-source; (b) common-source with resistive feedback; (c) common-gate and (d) cascode

Another issue encountered during the design of a LNA is to balance between the power match and noise match [37]. It is beneficial to have power matching between the antenna (that is 50 Ω typically) and LNA, so that the weak received signal from the antenna can be transferred to the LNA effectively for power amplification. On the other hand, the operation of the LNA requires a low noise figure that is achieved through the matching of the source impedance, Z_s, to the Γ_{opt} point which defines the input impedance for achieving the minimum noise figure.

Condition for matching to achieve maximum power transfer:

$$Z_S = Z_{in}^* \qquad (3.14)$$

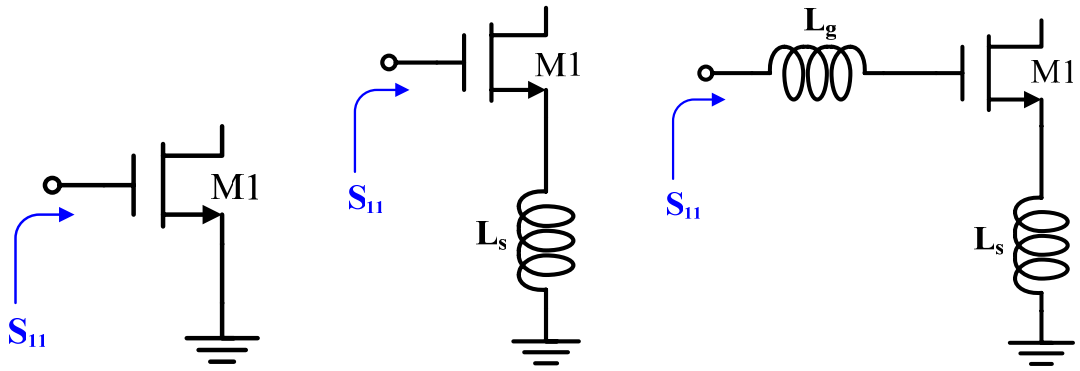
Equation (3.14) states the condition for the matching between the source impedance and the conjugated input impedance (Z_{in}^*) of LNA.With this condition, there will be the maximum power transfer between the antenna and the LNA. On the contrary, the minimum noise of the device, which corresponds to lowest noise factor, $F_{\min}$, can only be achieved by matching the input to the noise impedance, Z_{opt}.

Noise matching: $Z_S = Z_{opt}$ (3.15)

These contradicting requirements on the input impedance for having maximum power transfer and achieving minimum noise figure are impossible to be realized simultaneously in a CMOS LNA because of the correlation of drain current noise and induced gate noise from the common-source transistor [28]. Hence, the trade-off of minimum noise figure and maximum power gain is inevitable from classical noise theory.

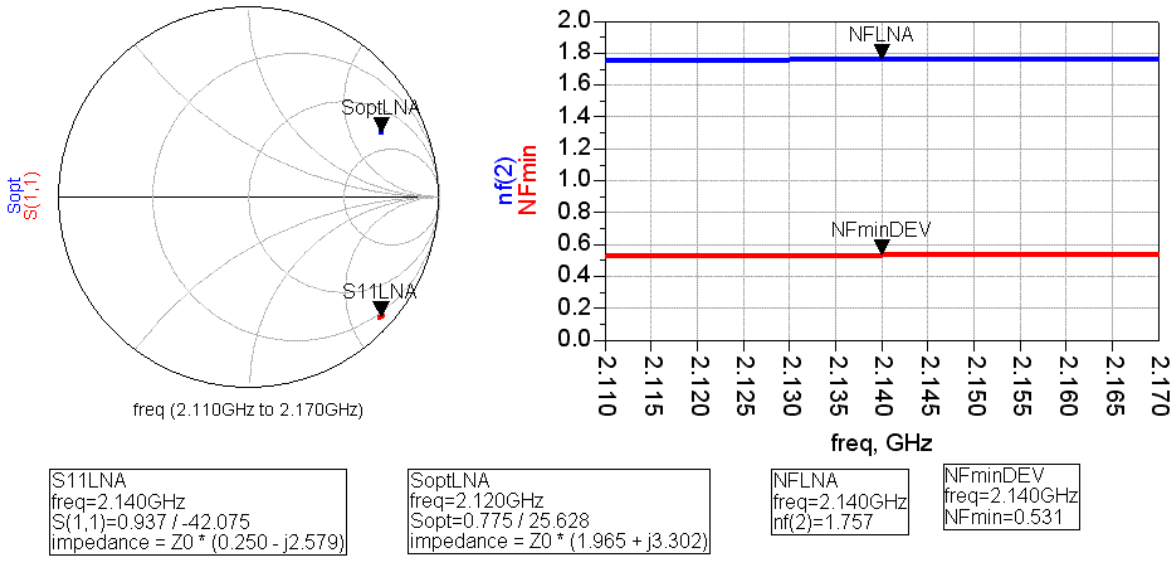
With the feedback element, L_s, added to the amplifier, it is possible to realize the power matching and noise matching in close proximity [33], [38]. Since the resistive feedback element will produce additional noise to the circuit, inductive source degeneration is used with the cascode amplifier. Although there is a mild change of $F_{\min}$ compared to the simple cascode topology, it is possible to achieve the power match with minimum penalty from the degradation of noise figure if the lossy inductor is used. The procedures of the LNA

matching with ideal inductor L_s and L_g are illustrated by Figure 3.4. The effect of source degeneration to the F_{min} can be found in Figure 3.5.

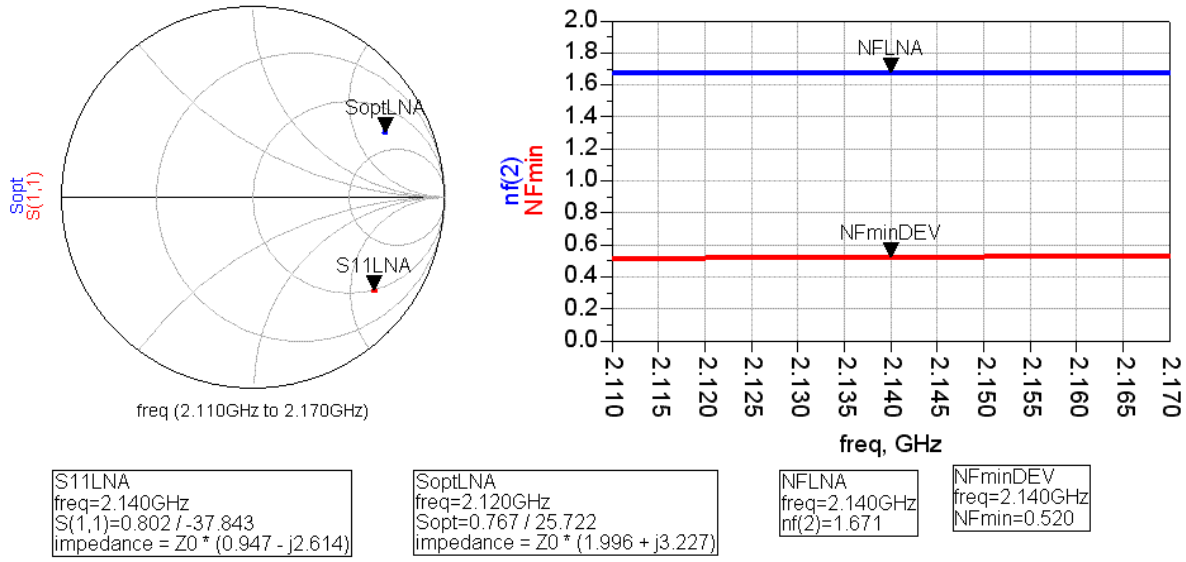


(a) (b) (c)

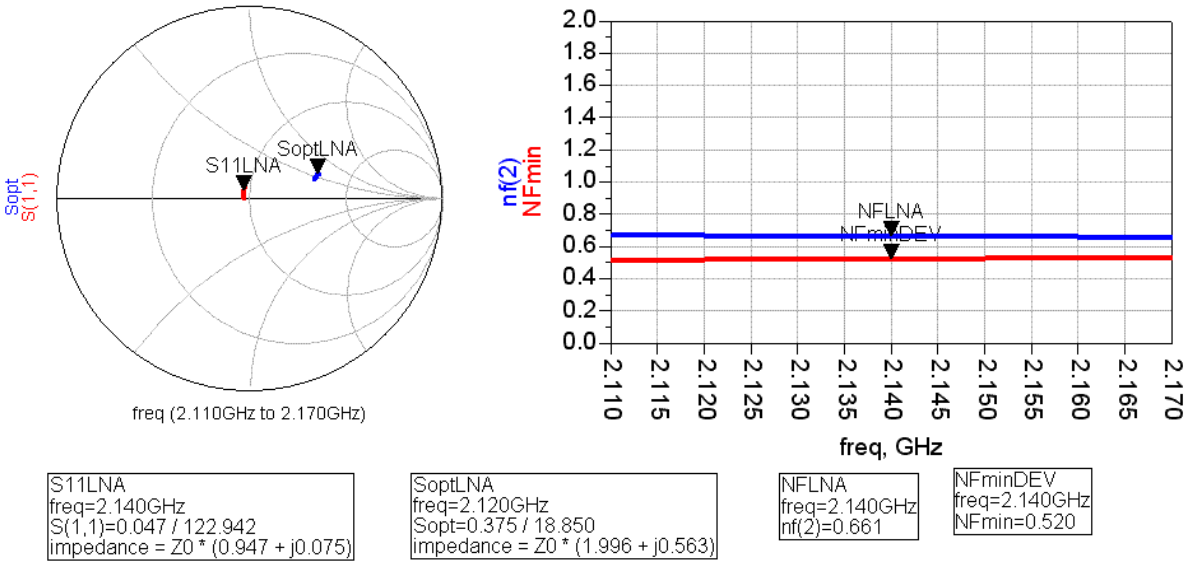
Figure 3.4 The matching of transistor M1 (a) The S_{11} of device (b) Add source inductor to shift the S_{11} curve (c) Add gate inductor to shift the S_{11} to 50 Ω point at the Smith chart.



(a)



(b)



(c)

Figure 3.5 The change of S_{11}, S_{opt} and F_{min} after adding the source inductor (b) and gate inductor (c) to the transistor (a).

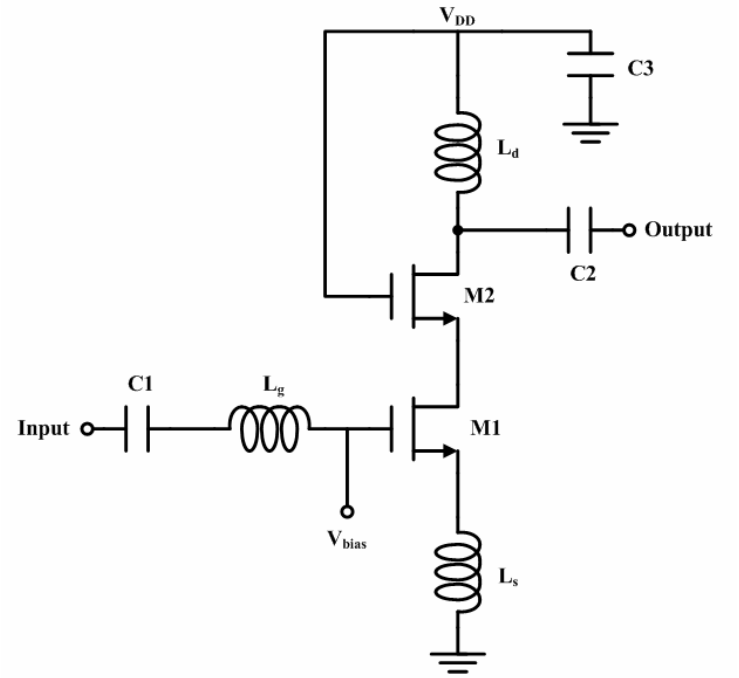


Figure 3.6 Schematic of single-ended LNA with inductive source degeneration

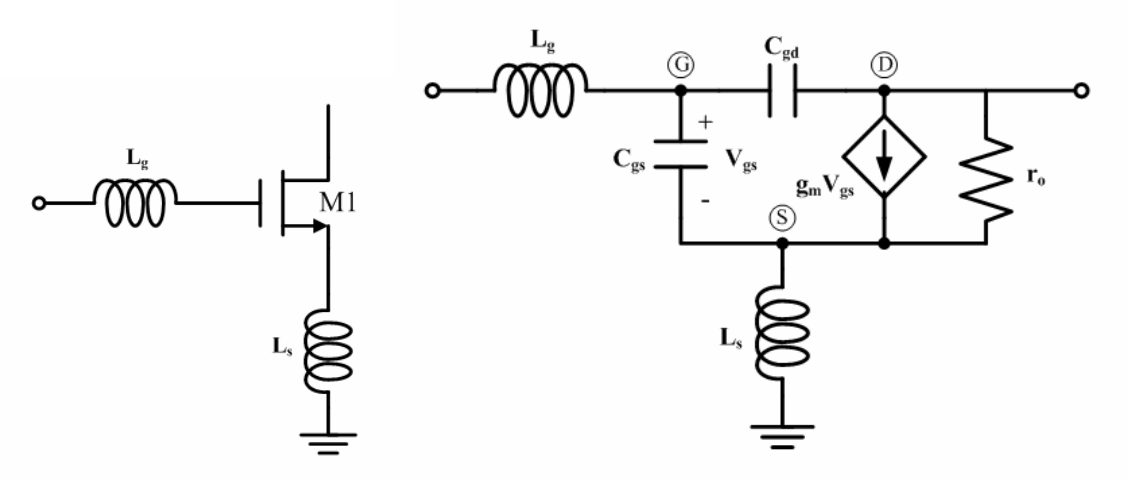


Figure 3.7 The small signal model of M1

The LNA design adopted in this project can be represented by the single-ended circuit as shown in Figure 3.6. The cascode structure formed by M1 – M2 is the core of the LNA.

The impact of the cascode transistor, M2, to the noise figure and input matching is considerably smaller than M1, hence it was neglected in the small signal model shown in Figure 3.7. The input matching is achieved by L_g, L_s. and the intrinsic capacitance, C_{gs1},of M1. The values of L_g and L_s can be determined by Equation (3.17) and Equation (3.18) if C_{gd1} is ignored for simplicity. The input impedance of 50Ω can be designed by proper biasing the transistor (i.e. g_{m1}) and L_s according to Equation (3.17).

$$
\begin{aligned}
&Z_{in} \approx j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs1}} + \left(\frac{g_{m1}}{C_{gs1}}\right)L_s \\
&\Rightarrow Z_{in} \approx j\left[\omega\left(L_s + L_g\right) - \left(\frac{1}{\omega C_{gs1}}\right)\right] + \left(\frac{g_{m1}}{C_{gs1}}\right)L_s \\
&\Rightarrow Z_{in} = \left(\frac{g_{m1}}{C_{gs1}}\right)L_s = 50\Omega \quad \text{when } \omega = \omega_0 = 2\pi f_0
\end{aligned}
\tag{3.16}
$$

$$
f_0 = \frac{1}{2\pi\sqrt{(L_s + L_g)\cdot C_{gs1}}} \tag{3.17}
$$

The power gain and output matching are dependent on L_d, which is designed to be as large as possible for providing a larger output voltage swing and acting as a RF choke. The input and output of the circuit are ac-coupled through *C1* and *C2*. The decoupling capacitor, *C3*, has a very important role in the design, it not only provides an ac ground at high frequencies, it also improves the stability of the circuit.

The noise factor of Figure 3.7 can be approximated by the following equation [28] and [48]:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right)$$
$$= 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{1}{Q_L}\cdot\frac{\gamma}{\alpha}\cdot\left(\frac{\omega_0}{\omega_T}\right)\cdot\left[1 - 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_L^2\right)\right] \quad (3.18)$$

where

R_s	Source resistance (typically 50Ω)
R_l	Series resistance in inductor L1
R_g	Gate resistance associated with M1
γ, χ	Bias-dependent parameter
δ	Coefficient of gate noise
α	Ratio between g_m and drain conductance when $V_{DS} = 0$
c	Correlation coefficient between the gate induced noise and drain current noise. It is about $-j0.395$ typically.
Q_L	The quality factor of the input matching network, which is equivalent to $\omega_0\left(L_s + L_g\right)/R_s$ or $1/\omega_0 R_s C_{gs}$

Equation (3.18) shows that the noise factor improves with ω_T of the transistor. In other words, the scaling of the transistor can reduce the transistor's noise, hence the minimum feature length 0.35 μm is chosen for M1 and M2. The design criterion for the width of M1 is based on Equation (3.19), which gives the optimum width, $W_{1,opt}$, for the minimum noise factor under the fixed power consumption. Hence, the calculated width of M1 is 306 μm. In the physical layout, the width of 340 μm is selected due to the availability of the

extracted RF model. It is observed that the inductor Q is very crucial to the performance of the noise factor. From Equation (3.19), the parasitic resistance associated with the inductors can significantly degrade the noise factor because the noise factor is proportional to the resistance and inversely proportional to the loaded-Q of the circuit, which is dominated by the inductors.

$$W_{1,opt} = \frac{3}{2} \times \frac{1}{\omega_0 L C_{ox} R_s Q_{L,opt}} \tag{3.19}$$

For M2 of Figure 3.6, it is connected in common-gate configuration. Although its impact to the noise figure is not significant, the sizing of this transistor will affect the OIP3 of the LNA. To improve the voltage headroom, the width is chosen to be 140 μm so that the V_{DS} of M2 is minimized.

Similarly, the same design procedures can apply for the differential LNA. However, the noise figure will increase because of more transistors and passive components are involved in the design. To achieve the same noise figure as single-ended design, twice the power consumption is needed.

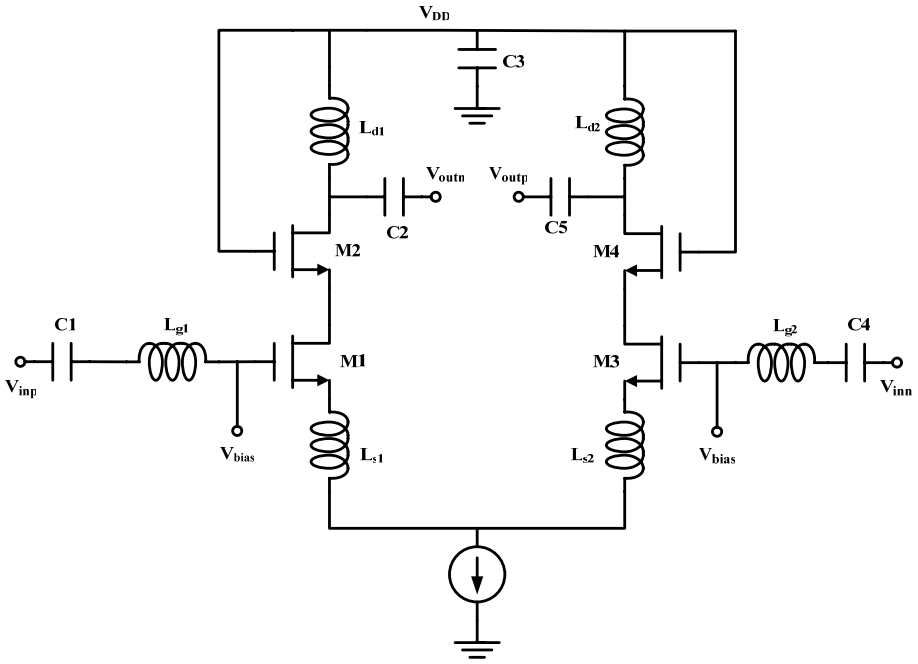


Figure 3.8 Schematic of differential LNA with inductive source degeneration

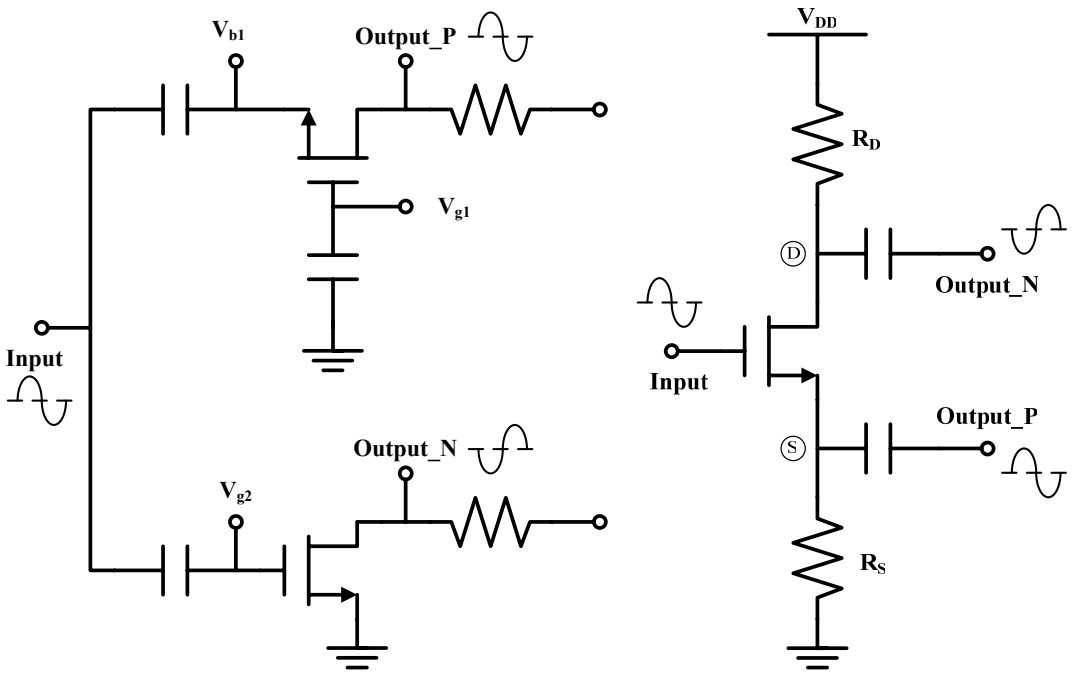
3.2.3.2 Active Balun

The single-ended LNA offers lower noise figure and simpler interfacing with the antenna than the differential LNA. However, the single-ended output is not suitable for the double balanced mixer that is a preferred mixer topology due to good port-to-port isolation. As a result, it is necessary to convert the single-ended signal to differential signal by either an off-chip passive balun (or bandpass filter) or an on-chip active balun.

To increase the integration level, an active balun design is utilized here. The merits of an active balun such as higher gain and lower noise figure can improve the front-end performance and result in better sensitivity. The most challenging design task for this

circuit is to maintain good balance on gain and phase difference between the differential output signals. Since the specification on image-rejection ratio is less than 30 dB for DCR [10], the gain imbalance and phase difference of DCR are not as stringent as for the low-IF receiver.

The single-to-differential converter can be realized with simple circuit topologies. In Figure 3.9 (a), [34] utilized the output nature of common-source and common-gate configurations to produce two out-of-phase signals. The drawback of this circuit is the imbalance of the differential output amplitudes. The biasing of the transistors and output loading needs to be designed carefully to produce the same outputs' swing. Another simpler approach shown in Figure 3.9 (b) is using a single transistor with the connections to source and drain resistors. By properly selecting R_S and R_D, the balanced gain and phase difference can be achieved. However, this circuit is problematic when it is operated in radio frequencies, the different parasitic capacitances associated with the drain and source would cause the imbalances in output signals' level and phase. Furthermore, the two circuits shown in Figure 3.9 are based on single-ended approach. There are easily affected by the common-mode disturbances, thereby the topologies shown in Figure 3.9 are not suitable for the DCR.



(a) (b)

Figure 3.9 Examples of active balun circuits

In general, a differential circuit with single-ended input can also produce differential outputs with equal i_p and i_n but opposite polarity This situation is valid when the virtual ground is formed by the infinite impedance looking into the current source from node X (Figure 3.10). The differential output signals start to deteriorate when the operating frequency goes higher and parasitic capacitance, C_{p1}, provide the leaking path for the ac current, i'. The leakage through the parasitic capacitor would disrupt the symmetrical properties of the differential circuit, and as a result, the output phase of the output is not maintained at 180°.

The necessary conditions for Figure 3.8 to act as single-to-differential converter are

$$|i_p| = |i_n| \Rightarrow i' = 0 \tag{3.20}$$

$$phase(i_p) - phase(i_n) = 180° \tag{3.21}$$

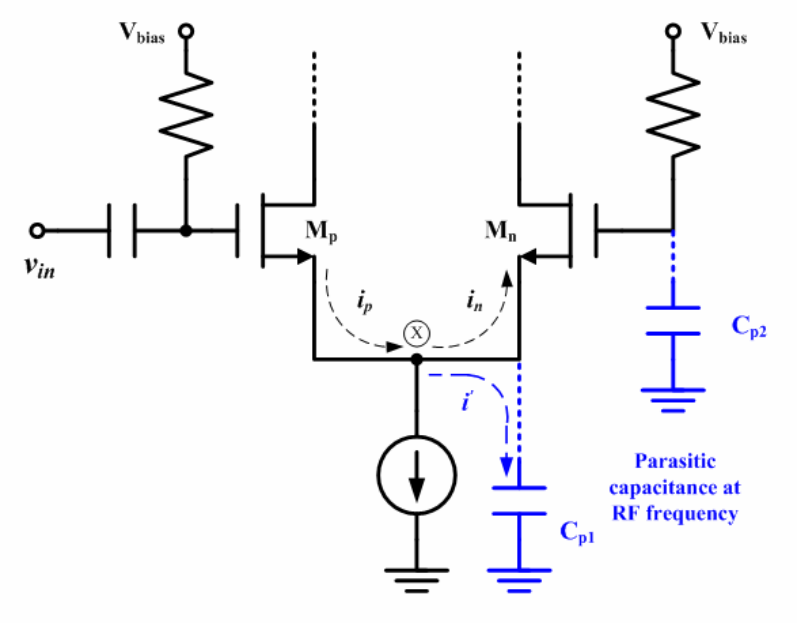


Figure 3.10 Problems of differential circuit use as an active balun

When the parasitic capacitance , C_{p1}, starts to appear at node X at RF,

$$i_p = i_n + i' \tag{3.22}$$

To circumvent this problem, the modified active balun circuit is designed based on the topology presented in [36]. To counter the imbalance of the amplitude and phase difference caused by the parasitic capacitances, two tank circuits are added to the conventional differential circuit as shown in Figure 3.11. The parallel resonant tank formed by L_p and C_p, will improve the impedance looking into the current source at the

operating frequency, which is set to be 2.14 GHz. This approach would reduce the leakage current caused by parasitic capacitance, C_{p1}. To further improve the output phase and amplitude of the ac current, the series resonant circuit has been inserted to the path between node *Y* and node *Z*. The series resonant circuit formed by L_s and C_s is designed such that a small amount of output current signal at the drain of M_p is channeled to the gate of M_n, so that the output signal at the drain of M_n is enhanced. Since the tank circuits are used in the design, the differential phase and gain balance can only maintain in a narrow frequency range.

$$f_0 = \frac{1}{2\pi\sqrt{L_p C_p}} = \frac{1}{2\pi\sqrt{L_s C_s}} = 2.14\,\text{GHz} \tag{3.23}$$

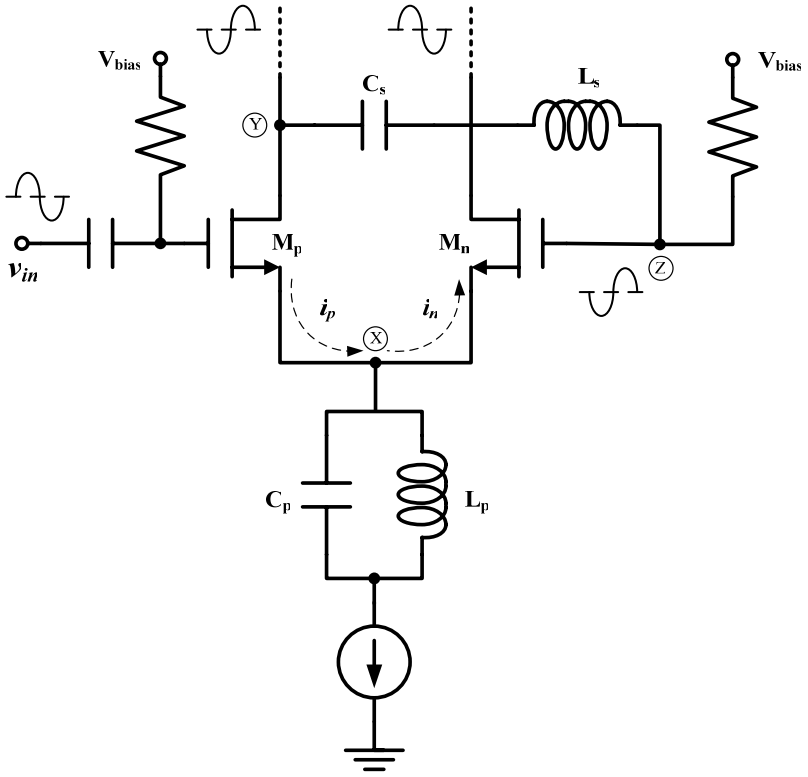


Figure 3.11 The modified active balun

3.2.3.3 LNA with Gain Switching

From Table 2.5, the minimum requirement for *IIP3* of the front-end circuit is at least -16 dBm. This design goal on *IIP3* is difficult to realize if the LNA gain is more than 25 dB. Under a strong signal condition, the maximum RF input power can reach -25 dBm. At the mixer input, the signal strength can be as high as 0 dBm after a 25 dB signal amplification from the LNA. There are two solutions to this problem, firstly, the *IIP3* of the mixer needs to be as high as possible. Since the *IIP3* is related to the power consumption by Equation (3.4) and Equation (3.11), the improvement of *IIP3* requires a larger biasing current to the transistor. The trade-off between linearity and power consumption is usually inevitable.

To circumvent this problem, a variable gain feature is added to the LNA. When the signal is too strong, the bypass route is provided to the input signal without any amplification from the LNA (Figure 3.12). Since the LNA is not utilized in this scenario, it can be shut down to reduce the current consumption. This advantage does not come without penalty, the *NF* of the front-end will be degraded.

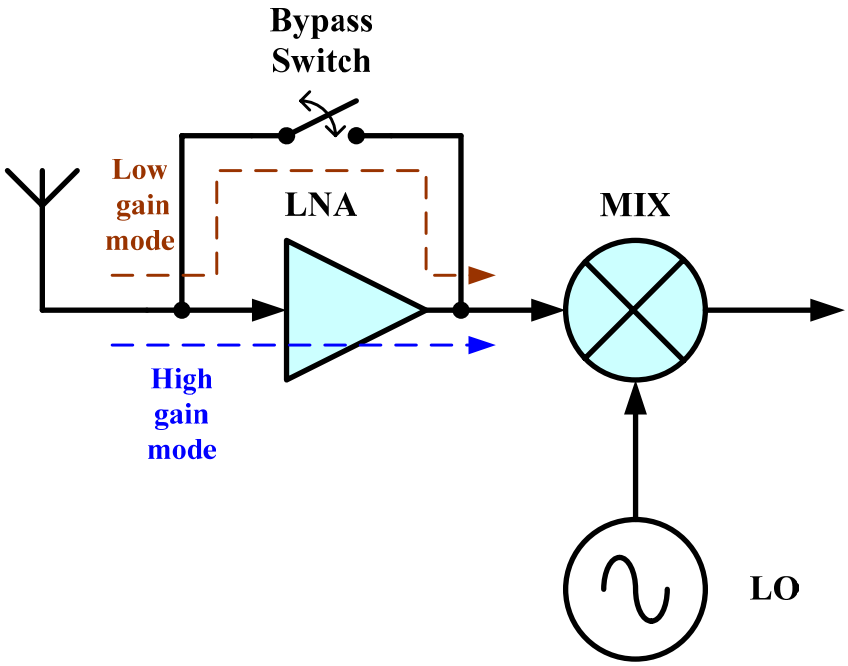


Figure 3.12 The LNA with gain switching

The bypass route is controlled by a switch, which is realized by a transmission gate. When the bypass route is activated during the strong signal condition, the received RF signal is bypassing the LNA without any amplification and the mixer will not be saturated by the input signal. Since the bypass route is controlled by the transmission gate, the "ON" resistance of this switch needs to be careful designed, otherwise, the attenuation of the signal may be too large and result in poor *SNR* at the mixer input.

The ON resistance of long channel NMOS and PMOS can be represented by Equation (3.24) and Equation (3.25) respectively [52]:

$$R_{ON,n} = \left(\frac{\partial i_{DS}}{\partial v_{DS}} \right)^{-1} = \frac{L}{\mu_n C_{ox} W \left(v_{GS} - V_T - v_{DS} \right)} \tag{3.24}$$

$$R_{ON,p} = \left(\frac{\partial i_{DS}}{\partial v_{DS}} \right)^{-1} = \frac{L}{\mu_p C_{ox} W \left(\left| v_{GS} - V_T \right| - \left| v_{DS} \right| \right)} \tag{3.25}$$

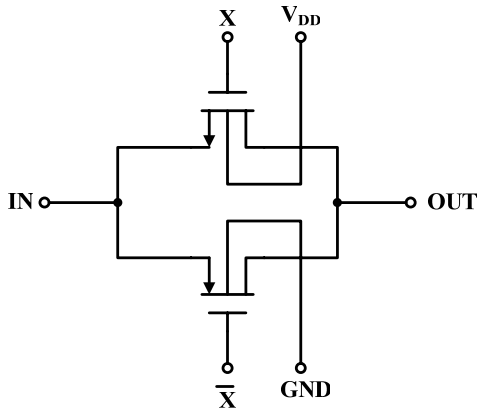


Figure 3.13 Structure of transmission gate

The equivalent ON resistance of the gate is expressed in Equation (3.26).

$$R_{ON} = R_{ON,n} // R_{ON,p} \tag{3.26}$$

3.2.4 Circuit Implementations

As mentioned in Chapter 2.4.2.1 and 3.2.2, two LNA designs are implemented in this project, namely the differential LNA (LNA_v1) and the single-ended LNA (LNA_v2). The detailed schematics of these designs are shown in Figure 3.14 and Figure 3.15 respectively. The feature size of the elements used in the circuits are also tabulated in Table 3.1 and Table 3.2 respectively.

In the fully differential design, better second-order intermodulation performance is targeted because of the stringent requirement for the W-CDMA application. By adopting a differential and symmetrical architecture, the degradation of IP2, which usually arises from path imbalances and components' mismatches, can be reduced significantly. To meet the gain requirement, two differential stages were cascaded to provide higher gain by ac-coupling. With the capacitive coupling (C3 and C4) between two stages, the biasing of the gain stages can be designed independently. In the scenario of a strong RF input signal, the bypass routes are provided from the differential outputs of the first-stage LNA to the output of the second-stage LNA (SW3 and SW4). Although the total LNA gain is reduced when the second gain stage is bypassed, the noise figure is not degraded considerably because of the high gain in the first-stage LNA. Another advantage of this design is the reduction of current consumption, the second-stage amplifier will be shut down by SW1 in strong signal condition, which can be controlled by the baseband circuitry.

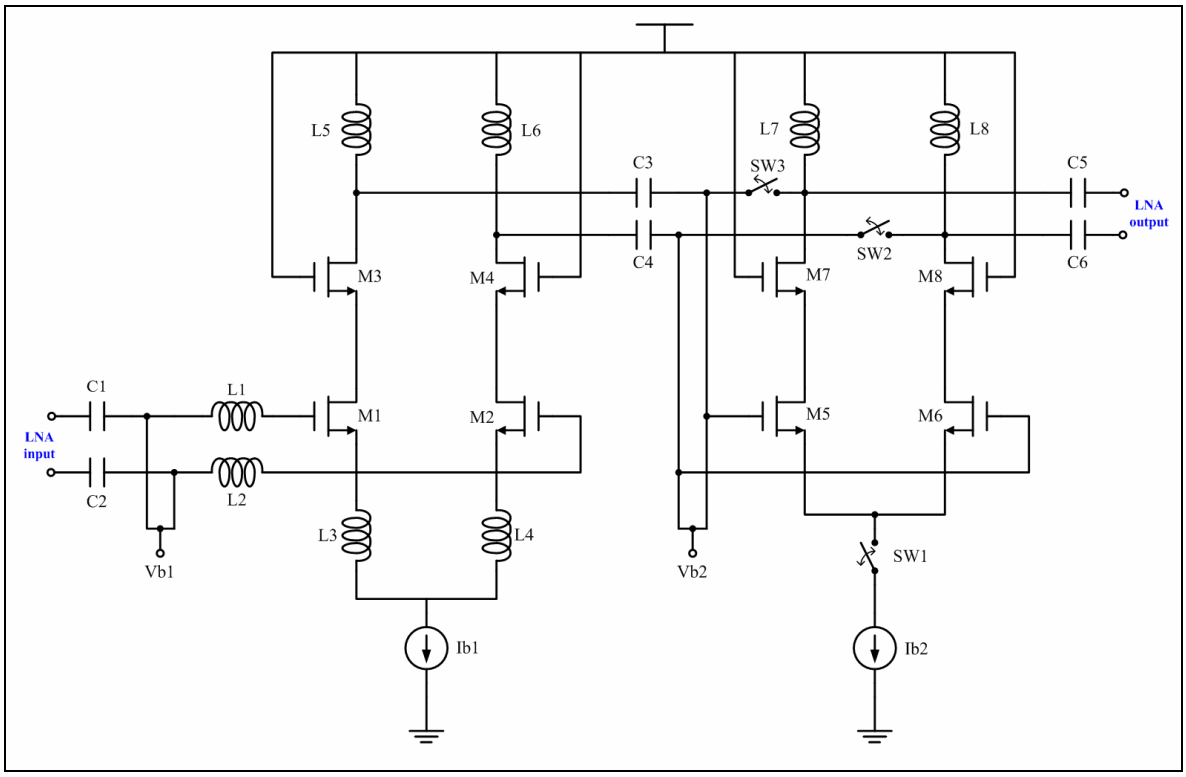


Figure 3.14 Schematic of LNA v1

Table 3.1 The feature sizes of the elements used in LNA_v1

Transistor	**W/L**
M1	340μm / 0.35μm
M2	340μm / 0.35μm
M3	140μm / 0.35μm
M4	140μm / 0.35μm
M5	200μm / 0.35μm
M6	200μm / 0.35μm
M7	140μm / 0.35μm
M8	140μm / 0.35μm
Inductor	
L1	6.8 nH @ Q = 5.3
L2	6.8 nH @ Q = 5.3
L3	0.5 nH @ Q = 2.1
L4	0.5 nH @ Q = 2.1
L5	12.8 nH @ Q = 4.1
L6	12.8 nH @ Q = 4.1
L7	9.0 nH @ Q = 4.9

L8	9.0 *nH* @ *Q* = 4.9
Capacitor	
C1	6 *pF*
C2	6 *pF*
C3	0.35 *pF*
C4	0.35 *pF*
C5	0.35 *pF*
C6	0.35 *pF*

For the LNA_v2 as shown in Figure 3.15, the design is based on a single-ended inductively source degeneration topology. The choice of single-ended design is made largely because of the straightforward interface between the monopole antenna and the LNA, no off-chip balun is required as in the case of LNA_v1, hence the system noise figure can be improved. The main challenge faced in the LNA_v2 comes from the design of the single-to-differential converter. Since the double balanced mixer topology is chosen for better port-to-port isolation, the amplified signal after the LNA is converted into a differential signal before the frequency down-conversion. Applying the same gain control feature as in LNA_v1 (SW2), the first stage is bypassed to meet the stringent linearity requirement. To implement the signal bypass mode on the first stage of LNA rather than second state is due to higher gain is provided in the first stage, which is not required when facing a strong input signal.

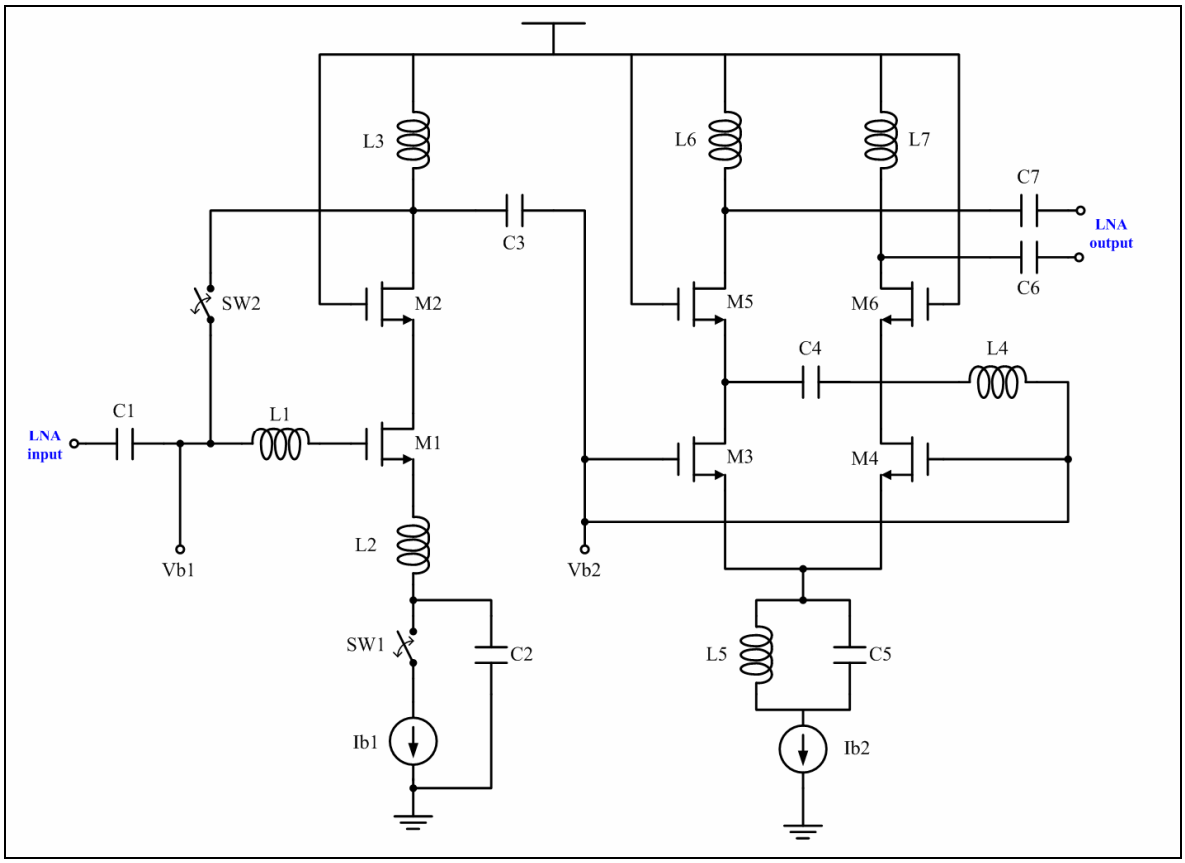


Figure 3.15 Schematic of LNA v2

Table 3.2 The feature sizes of the elements used in LNA_v2

Transistor	**W/L**
M1	340μm / 0.35μm
M2	140μm / 0.35μm
M3	140μm / 0.35μm
M4	140μm / 0.35μm
M5	100μm / 0.35μm
M6	100μm / 0.35μm
Inductor	
L1	6.8 nH @ Q = 5.3
L2	0.5 nH @ Q = 2.4
L3	12.8 nH @ Q = 4.1
L4	4.2 nH @ Q = 5.1
L5	1.7 nH @ Q = 4.2
L6	9.5 nH @ Q = 4.2
L7	9.5 nH @ Q = 4.2

Capacitor	
C1	6 *pF*
C2	8 *pF*
C3	4 *pF*
C4	0.60 *pF*
C5	2 *pF*
C6	0.35 *pF*
C7	0.35 *pF*

3.2.5 Simulation Results of LNA

Both LNA circuits are simulated using Agilent Advanced Design System (ADS2002). The models for transmission line, active and passive elements are based on IME in-house extracted models, which are from Chartered Semiconductor Manufacturing 0.35μm CMOS process with RF options. The parasitic networks are included in these models as stated in section 3.1.2.

Figure 3.16 and Figure 3.17 show the simulation results of the S-parameters for LNA_v1 and LNA_v2 respectively. The forward gain of LNA , S_{21}, is about 26.9 dB for LNA_v1 and LNA_v2 when high gain mode is turned on. Such a high gain level is critical for suppressing the noise came from the mixer and baseband circuits. The spot noise figures of LNA_v1 and LNA_v2 at 2.14 GHz are 3.07 dB and 3.17 dB respectively. Although the difference between two noise figures are minor, the reader should be reminded that an additional off-chip balun is required for the interface between the antenna and the differential LNA, hence the total noise figure will be further degraded.

The simulated P-1dB compression point for the high gain and the low gain mode can be found in Figure 3.18 to Figure 3.21. In the weak signal condition, the LNA bypass switches are turned off, so the P-1dB compression points are -30 dBm and -34 dBm for LNA_v1 and LNA_v2 respectively. As the bypass switches are turned, the gain of LNAs are reduced and the P-1dB are improved to -13 dBm and -10 dBm for LNA_v1 and LNA_v2 respectively.

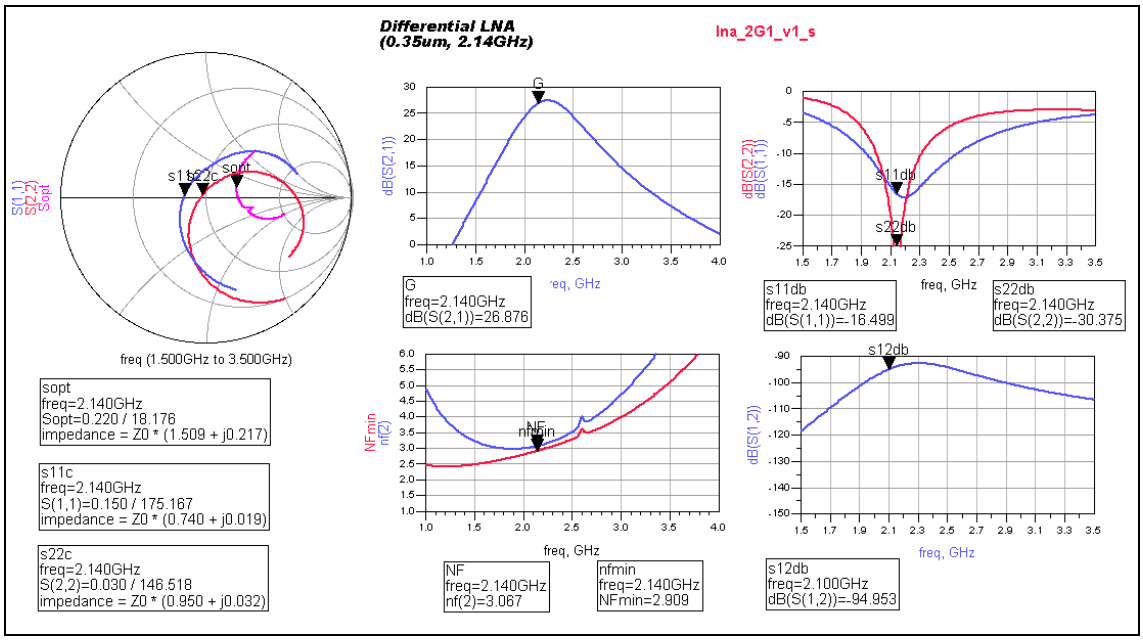


Figure 3.16 S-parameters and noise figure of LNA_v1 (high gain mode)

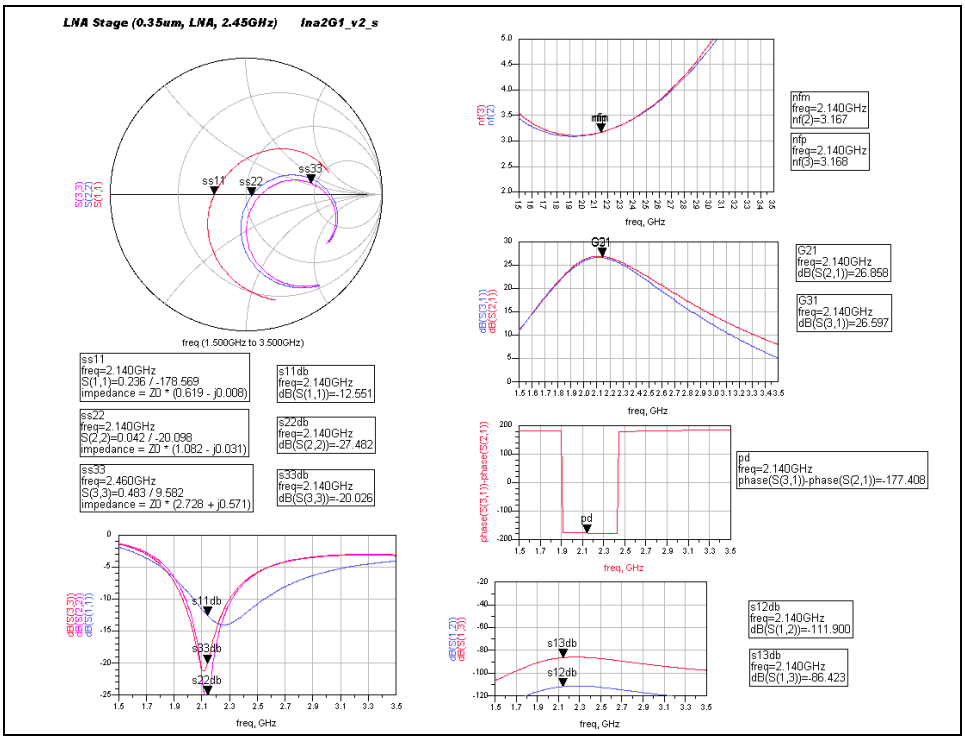


Figure 3.17 S-parameters and noise figure of LNA_v2 (high gain mode)

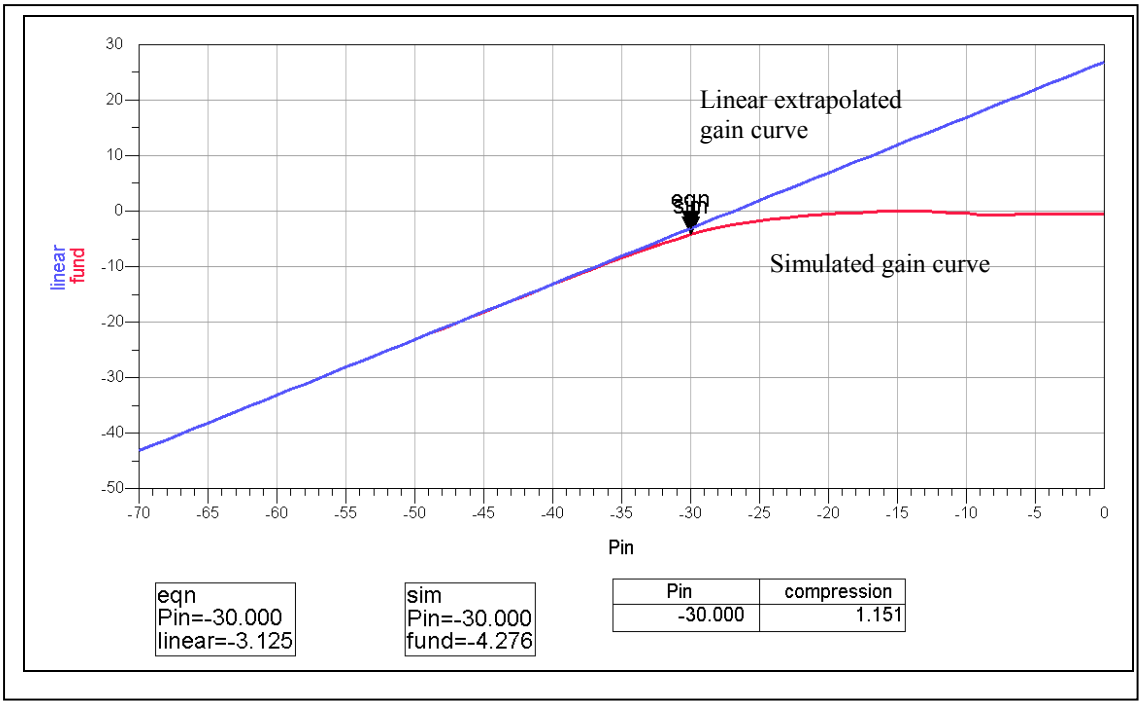


Figure 3.18 1-dB compression point of LNA_v1 (high gain mode)

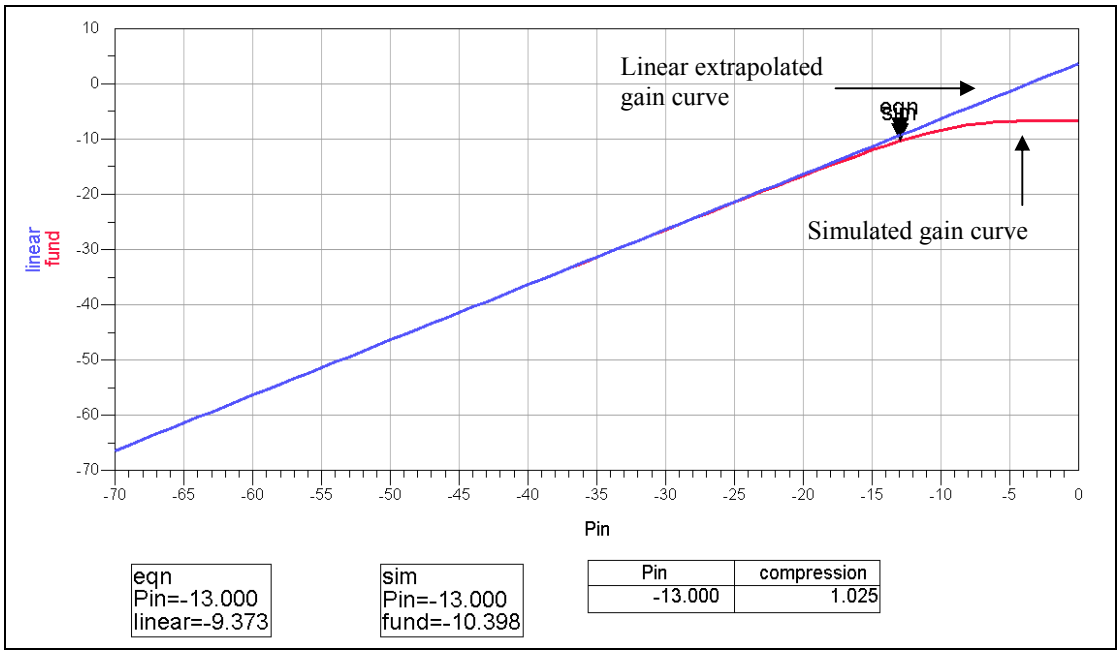


Figure 3.19 1-dB compression point of LNA_v1 (low gain mode)

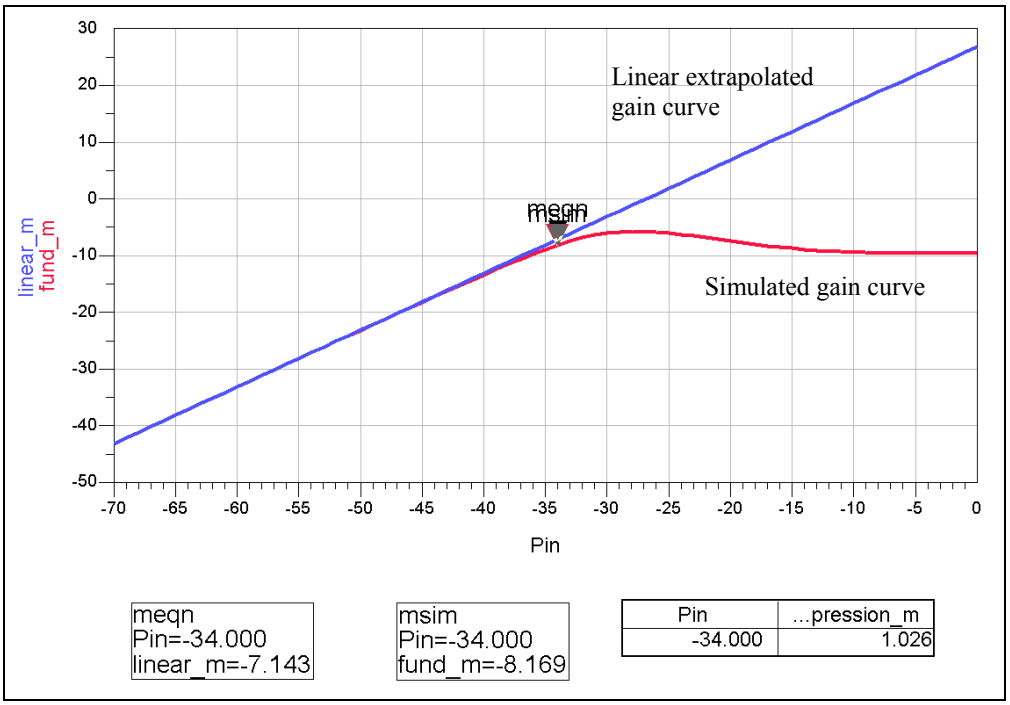


Figure 3.20 1-dB compression point of LNA_v2 (high gain mode)

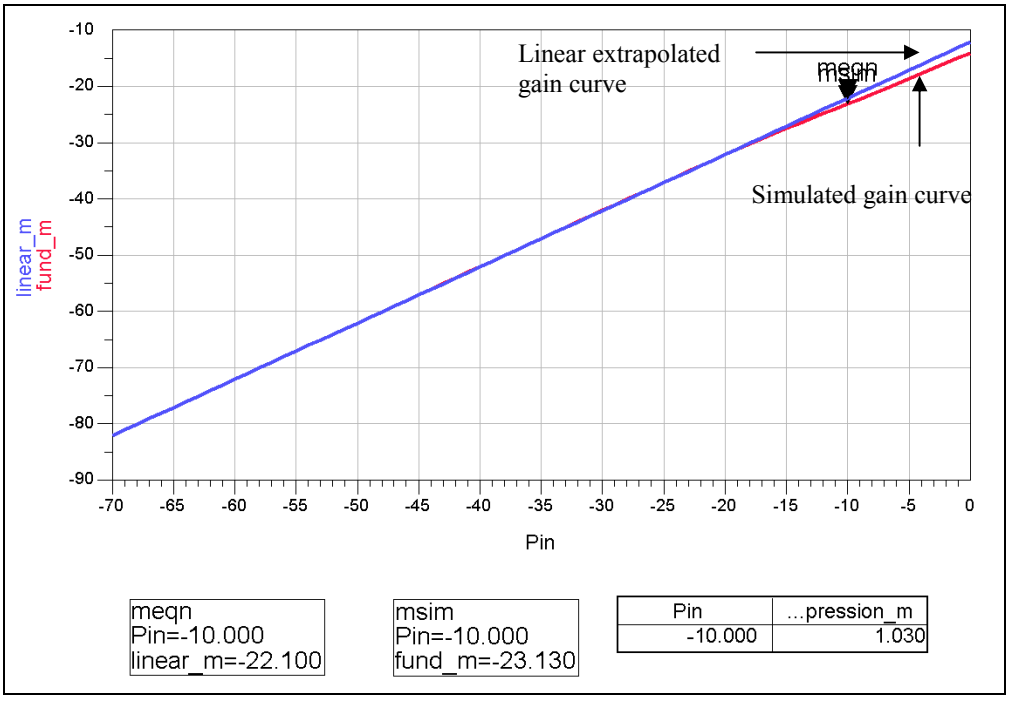


Figure 3.21 1-dB compression point of LNA_v2 (low gain mode)

To ensure stability of the LNA during when it is operated in high gain mode, the simulations are performed. According to [37], the necessary and sufficient conditions for the system to become unconditional stability are

$$K > 1 \tag{3.27}$$

$$|\Delta| < 1 \tag{3.28}$$

where K and Δ can be defined by the following equations.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.29}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.30}$$

Here, S_{11}, S_{22}, S_{21} and S_{12} represent the input reflection coefficient, output reflection coefficient, forward transmission coefficient and reverse transmission coefficient respectively. Based on these two conditions, the stability of LNA_v1 and LNA_v2 are simulated.

The simulated results from Figure 3.22 and Figure 3.23 show that LNA_v1 and LNA_v2 achieve unconditional stability. The *K*-factor and Δ for LNA_v1 at 2140 MHz are 1.123 and 0.007 respectively. For the LNA_v2, *K*-factor and Δ are 1.332 and 0.019 respectively.

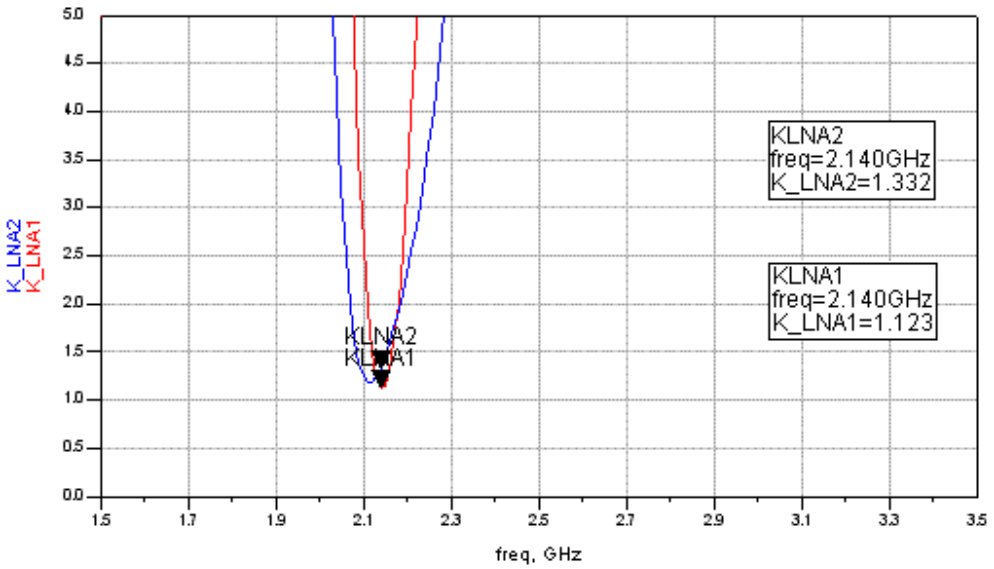


Figure 3.22 Simulated *K*-factor of LNA_v1 and LNA_v2

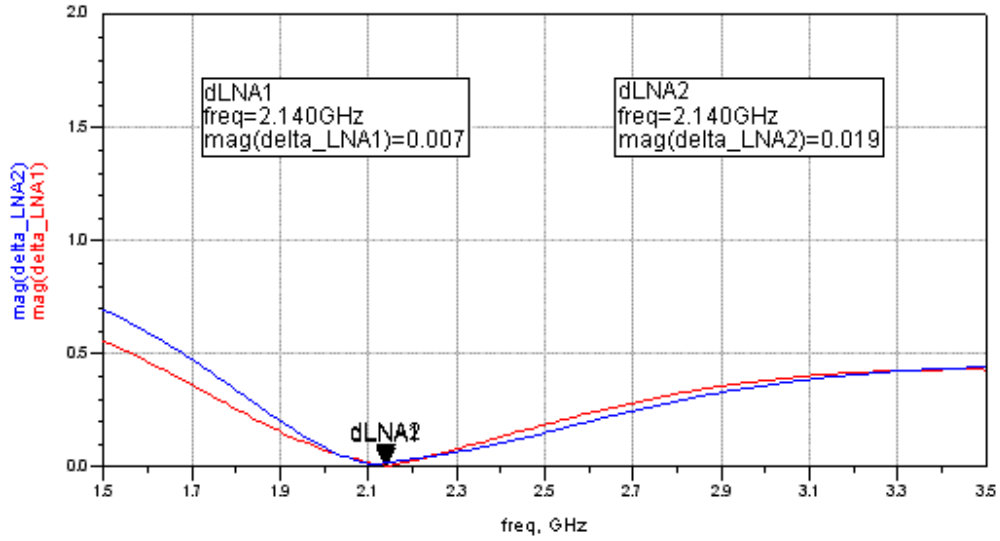


Figure 3.23 Simulated Δ of LNA_v1 and LNA_v2

The other simulation results such as *IIP3*, *IIP2* and other design parameters can be found in Appendix A.1. All the results from the LNA simulations are summarized in Table 3.3.

Table 3.3 Summary of LNA Simulation Results

Parameter	**Description**	**LNA v.1**	**LNA v.2**	**Unit**
		HG / LG	**HG / LG**	
f_c	Operating frequency	2140	2140	*MHz*
NF	Spot noise figure	3.1 / 4.0	3.2 / 26	*dB*
G	Power gain	26.9 / 3.6	26.6 / -12.0	*dB*
P_{1dB}	1-dB gain compression point	-30 / -13	-34 / -10	*dBm*
IIP3	3^{rd}-order intercept point	-21.0 / -2.5	-24 / 0	*dBm*
IIP2	2^{nd}-order intercept point	+122.0 / –	+69.9 / –	*dBm*
S_{11}	Input reflection coefficient	-17 / -17	-13 / -5	*dB*
S_{22}	Output reflection coefficient	-30 / -17	-20 / -20	*dB*
S_{12}	Reverse isolation	-95 / -56	-86 / -65	*dB*
I_d	Current consumption	12.1 / 8.1	9.6 / 4.5	*mA*

3.3 Design of Mixer Circuit

3.3.1 Introduction

In most of the applications, the LNA is followed by a mixer in the receiver chain as depicted in Figure 2.11. The main function of the mixer is to translate the modulated radio-frequency signal into a low frequency signal for further processing. The function of such frequency translation can be realized by either linear multiplication or non-linear operation. To achieve better efficiency for frequency conversion, the non-linear operation is adopted in most of the RF designs. During the process of frequency translation, not only the wanted signal is produced, many undesired signals are also generated due to the non-linearity of the circuits. These unwanted frequency components may interfere with the circuit operations and degrade the receiver performance considerably if they are not sufficiently rejected. It is also essential in making the mixer as linear as possible, so that the impact of mixing with the external interferers can be minimized. For the mixer circuit, *IP3*, *IP2* and *P-1dB* are the important design parameters to measure the linearity besides the conversion gain and noise figure.

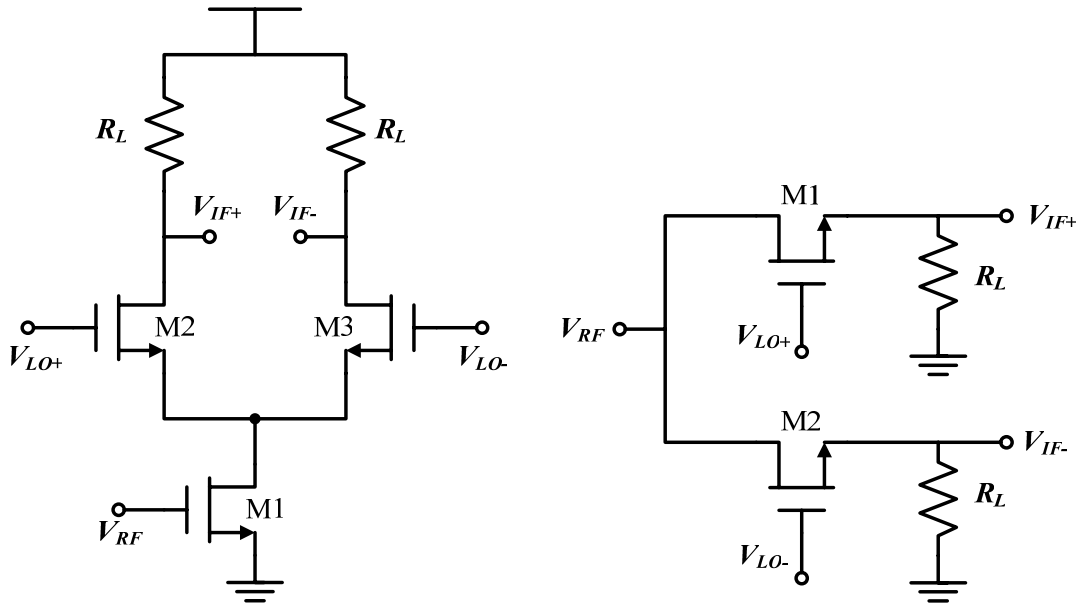
In the direct conversion receiver, the mixer plays an important role in the overall performance. Since the DCR requires only one frequency down-conversion instead of multiple conversions like in the superheterodyne receiver and in the low-IF receiver, the front-end gain of the receiver is solely determined by the LNA and mixer. The system

budgeting of the receiver shown in Table 2.5 requires the LNA to be more than 20 dB of gain reduce the impact of the noise contributed by the subsequent stages. As a result, the mixer must have good linearity to handle the amplified signal from the LNA without distorting the signal. In section 3.2.3.3, bypass modes are incorporated into the LNA_v1 and LNA_v2 to handle the large input signal condition and alleviate the linearity issue of the mixer. With this feature in place, the mixer still has to provide enough gain and a low noise figure for achieving the *SNR* requirement for the receiver. Furthermore, the DC-offset appearing at the mixer outputs after the frequency conversion is also a critical issue that may impair the receiver performance significantly. All these design challenges and trade-offs make the CMOS mixer design the most challenging circuit to be implemented.

3.3.2 Design Considerations

The mixer is the key building block in a direct conversion receiver. Without exception, noise figure and linearity performances are the major considerations in the mixer design as similar to the LNA. However, a mixer suffers more from the issue related to linearity rather than circuit noise problem. Since it is located after the LNA, the mixer can face strong signal situation, henceforth the linearity of the mixer is likely to be a bottleneck of the receiver performance when the wireless terminal is too close to the base station. In a W-CDMA system, the receiver needs to have a wide dynamic range to cater for the fluctuations of the received signal strength.

In general, there are two categories of mixer circuits based on the ability of signal amplification, namely an active mixer and a passive mixer [21] (Figure 3.20). Moderate signal gain is readily achievable in active mixer design but the linearity is limited because of voltage headroom issue between the supply rail and the circuit ground. In contrast, a passive mixer can offer superior linearity performance because they are lossy and always perform as a non-linear switch during the down-conversion of the RF signal to baseband frequencies.



(a) (b)

Figure 3.24 Mixer circuits for RF applications: (a) active mixer (b) passive mixer

The implementation of the active mixer is more advantageous than the passive counterpart in the direct conversion receiver. To improve the overall DCR performance, the combined front-end gain of LNA and mixer needs to be sufficiently high (> 25 dB) to improve the *SNR* of the receiver signal. Because of the conversion loss, the use of a passive mixer in a

DCR will degrade the noise figure of the receiver chain. Furthermore, higher gain is required for the LNA to compensate the signal loss from the passive mixer. When the gain of the amplifier is too high (> 30 dB), the stability of the system becomes the critical issue and oscillation will happen if the isolation from the output of the LNA to the input is not enough.

Another design issue of a mixer stems from the port-to-port isolation. After the direct down-conversion, the output signal of the mixer is subjected to the DC disturbance due to mismatch of components and self-mixing of the feedthrough signal. The isolations among RF, LO and IF-port are essential in minimizing this effect. The use of the double-balanced mixer architecture in the DCR design can reduce the problem of signal leakage. The highly symmetrical layout of the differential circuit can reduce the mismatch of the components caused by process variations, hence the circuit topologies and layout of the circuit needs to be carefully selected and planned before implementing the design.

3.3.3 Circuit Topologies

The active mixer topology is adopted here for the direct conversion receiver because of its superior gain and noise figure compared to the passive mixer. Among the active mixer circuits, the double-balanced Gilbert cell mixer as shown in Figure 3.21 is commonly used in RF applications. Not only it can provide a moderate conversion gain and low noise figure, it also offers good isolation between the RF, LO and IF-ports. The port-to-port isolations are very important to the performance of direct conversion receiver. Many

publications ([5] – [6]) have indicated that the poor performance of direct conversion receiver is mainly due to signal leakage from the mixer LO-port to RF-port. This problem will be exacerbated in the receiver built in a CMOS process because the LO signal may leak to the LNA through the silicon substrate. In this section, the phenomena of non-ideal switching of the double-balanced Gilbert cell will be examined. The impact on the conversion gain, noise figure, linearity and dc-offset will be analyzed below.

Conversion Gain and Noise Figure

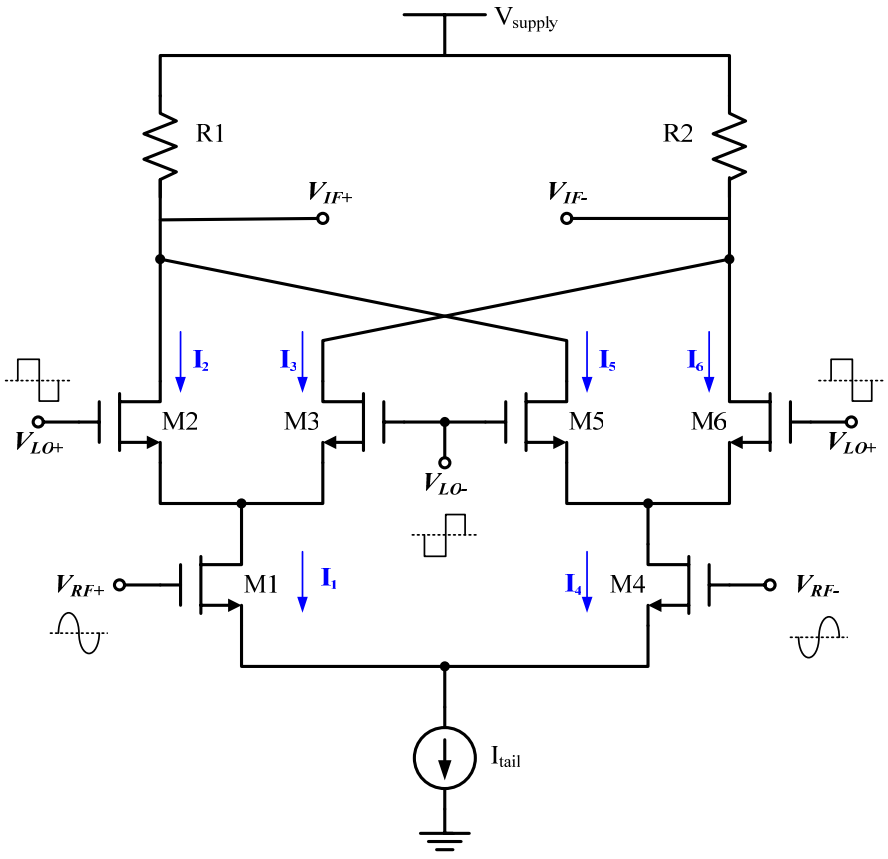


Figure 3.25 The double-balanced Gilbert cell mixer

In Figure 3.23, the mixing is done in two stages. M1 and M4 form a driver stage where the high-frequency V_{RF} signal is converted to i_{RF}. The major part of the mixer gain is also contributed by the driver stage, which can be controlled by the tail current source, $I_{tail,}$ and proper sizing of the transistors M1 and M4. The composite current of DC and small-signal components, ($I_1 + i_{RF}$) and ($I_4 - i_{RF}$), will then be commutated and steered to outputs (i.e. I_2, I_3, I_5 and I_6) through the quad-switches formed by M2, M3, M5 and M6. The mixing process is performed here through the ON/OFF actions of the quad transistors shown in Figure 3.22. By applying the square-wave local oscillator signal, V_{LO}, the instantaneous switching from transistors M2 and M6 to M3 and M5 will produce the signal multiplication effects. This mechanism can be represented mathematically by the following expression.

Assume that

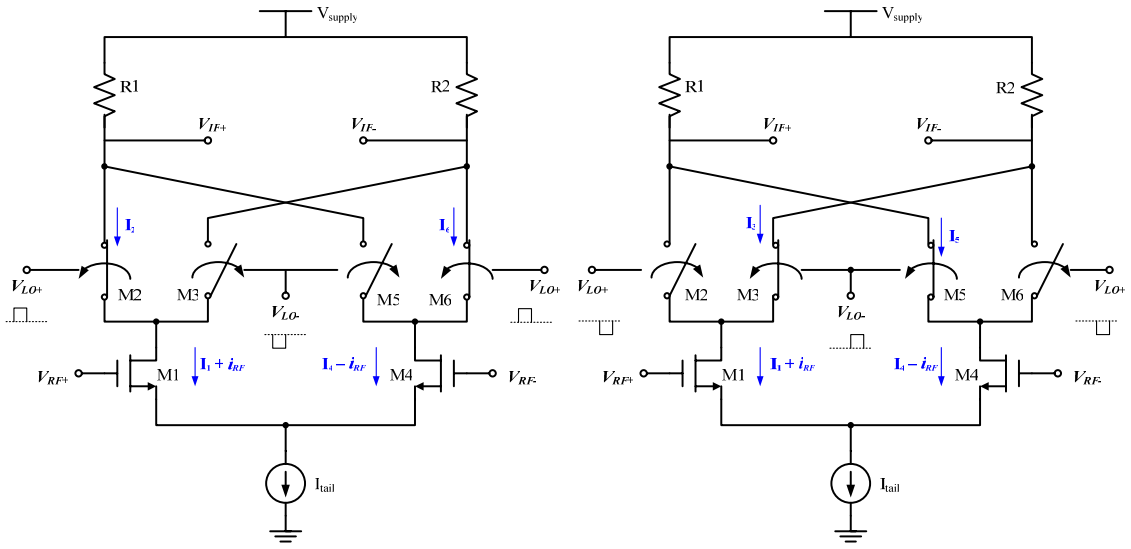
$i_{RF}(t) = g_{m1} \times v_{RF}(t) = g_{m1} A_{RF} \sin(\omega_{RF} t)$ and $Sqr(t)$ represents a square wave, which is expressed in a form of Fourier series.

$$\begin{aligned} I_2(t) &= i_{RF}(t) \times Sqr(t) \\ &= g_{m1} A_{RF} \sin(2\pi \cdot f_{RF} t) \times \frac{4}{\pi}\left[\sin(2\pi \cdot f_{LO} t) + \frac{1}{3}\sin(2\pi \cdot 3 f_{LO} t) + \cdots\right] \\ &= \left(\frac{4}{\pi}\right) g_{m1} A_{RF} \sin(2\pi \cdot f_{RF} t)\sin(2\pi \cdot f_{LO} t) + \cdots \\ &\approx \left(\frac{2}{\pi}\right) g_{m1} A_{RF} \cos[2\pi(f_{RF} - f_{LO})t] \end{aligned} \tag{3.31}$$

$$
\begin{aligned}
V_{IF} &= V_{IF}^{+} - V_{IF}^{-} \\
&= I_2 R_1 - I_6 R_2 \\
&= 2 \times \left(\frac{2}{\pi} \right) g_{m1} R_L A_{RF} \cos\left[2\pi \left(f_{RF} - f_{LO} \right) t \right]
\end{aligned}
\tag{3.32}
$$

The down-converted current signal, which has the frequency component of $(f_{RF} - f_{LO})$, is riding on the DC current of I_2 and I_6 simultaneously (or I_3 and I_5). The differential output voltage of the double-balanced mixer, V_{IF}, can be determined by Equation. (3.28).

At any moment, only two transistors are turned on and the other two are in "OFF" mode as illustrated in Figure 3.24. This operating condition is very essential to the signal leakage, conversion gain and noise figure of the mixer ([9], [39] – [41]).



(a) (b)

Figure 3.26 The switching action of the conventional double-balanced Gilbert cell mixer

When ideal switching (i.e. square-wave V_{LO}) is applied to the Gilbert cell mixer, the conversion gain and noise figure can be represented by the following equations.:

$$G_{mix} = 2 \times \left(\frac{2}{\pi} \right) \cdot g_{m,RF} \cdot R_L \tag{3.33}$$

The maximum conversion gain of the mixer shown in Equation (3.29) is based on the assumption that the quad-transistors act as perfect switches. Their impacts on the mixer's conversion gain are neglected in the equation above. In the expression, $g_{m,RF}$ is the transconductance of M1 or M4, R_L represents the load resistance (R1 or R2).

The derivation of the mixer's noise figure is more complex and tedious due to the periodically time-varying nature of mixer operation. The contributions from the noise sources during the ON/OFF period are not the same. The derivation of the expression for single-side band (SSB) noise factor for the double-balanced Gilbert cell mixer is given by [39]:

$$F_{SSB} = \frac{\alpha}{c^2} + \frac{2(\gamma_1 + r_{g1} g_{m1}) g_{m1} \alpha + 4\gamma_2 \overline{G} + 4 r_{g2} \overline{G^2} + 1/R_L}{c^2 g_{m1}^2 R_S} \tag{3.34}$$

where α represents the power of the current waveform resulting from the switching action. c is the ratio of conversion gain over the transconductance of the driver stage and $\overline{G}$ is the mean square of time varying transconductance of the switching stage. Equation (3.30) can be further simplified if the noise contributions from the quad-switches are ignored.

$$F_{SSB} = \left(\frac{\pi}{2}\right)^2 + \frac{2\gamma_1 g_{m1} + 1/R_L}{g_{m1}^2 R_S} = 2.467 + \frac{2\gamma_1}{g_{m1} R_S} + \frac{1}{g_{m1}^2 R_s R_L} \quad (3.35)$$

where γ_1 and g_{m1} are the process parameter and the transconductance of M1, R_S and R_L are source resistance and load resistance respectively. It should be noted that Equation (3.31) only applies to the single-side band (SSB) noise factor. There are 3 dB improvement of noise factor because double-sided band (DSB) of the information bandwidth is demodulated in the direct conversion receiver during the recovery of the received signal.

In practice, perfect switching of the quad transistors by the square wave will not happen because of the parasitic capacitance and limited slew rate of V_{LO}. The common waveforms applied to the LO-port of the mixer are shown in Figure 3.25. When a sinusoidal wave is applied to M2, M3, M5 and M6, the quad switches will be turned "ON" simultaneously when v_{LO}(t) is within the region from -V_x to V_x , where V_x represents the voltage level when the transistor behaves as a switch. In this scenario, the conversion gain and noise figure will be degraded because the quad transistors are still in saturation mode. Furthermore the leakage from LO – RF and RF – LO would happen and result in self-mixing products. Hence, a large V_{LO} is always injected to the LO - port of the mixer and a minimum channel length is applied to the quad switches to emulate the effect of the square waveform. When the slope of v_{LO}(t) becomes steeper, ΔT_{LO} will be shortened as shown in Figure 3.25 (c). For very short duration, it can be expressed in the following equation.

$$\Delta T_{LO} = \frac{\sqrt{2}\left(V_{gs2} - V_{t2}\right)}{V_{LO}\omega_{LO}} \quad (3.36)$$

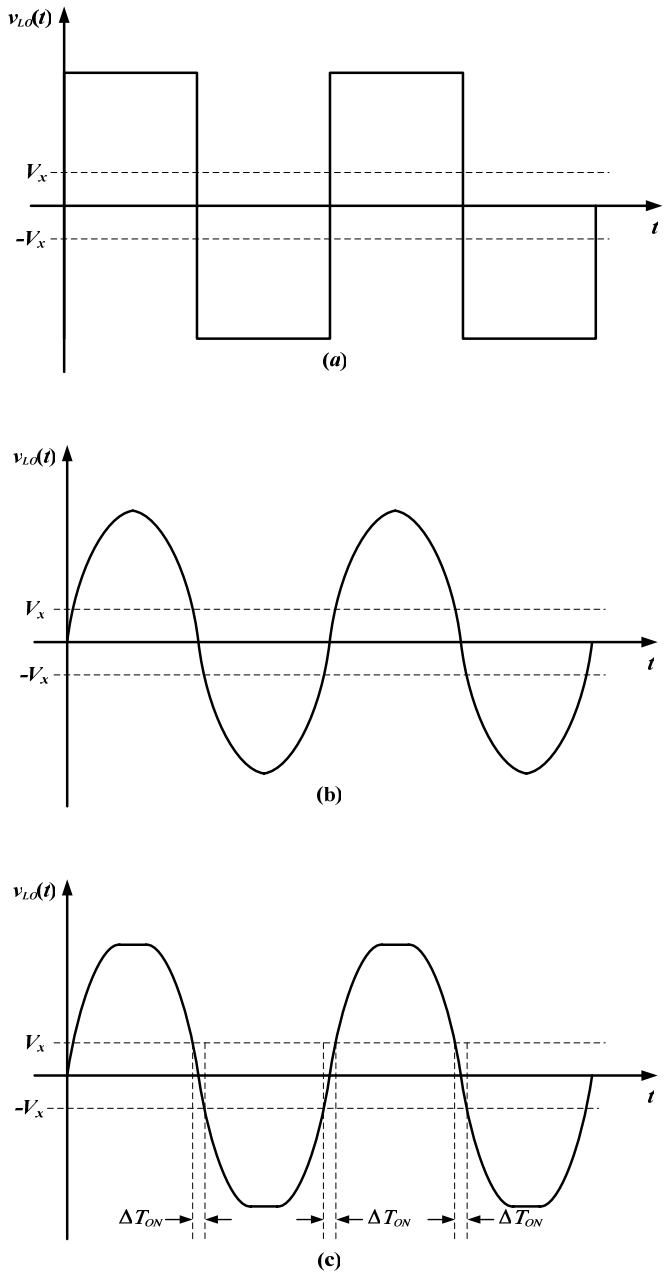


Figure 3.27 The various input waveforms at the LO-port of mixer. (a) Square wave; (b) sinusoidal wave; (c) non-ideal square wave.

The impact of ΔT_{LO} on the mixer conversion gain can be represented by the following equation [9]:

$$G_{mix} = 2 \times \left(\frac{2}{\pi}\right) \cdot g_{m1} R_L \cdot \left[1 - \frac{\sqrt{2}\left(V_{gs2} - V_{t2}\right)}{\pi V_{LO}}\right] \tag{3.37}$$

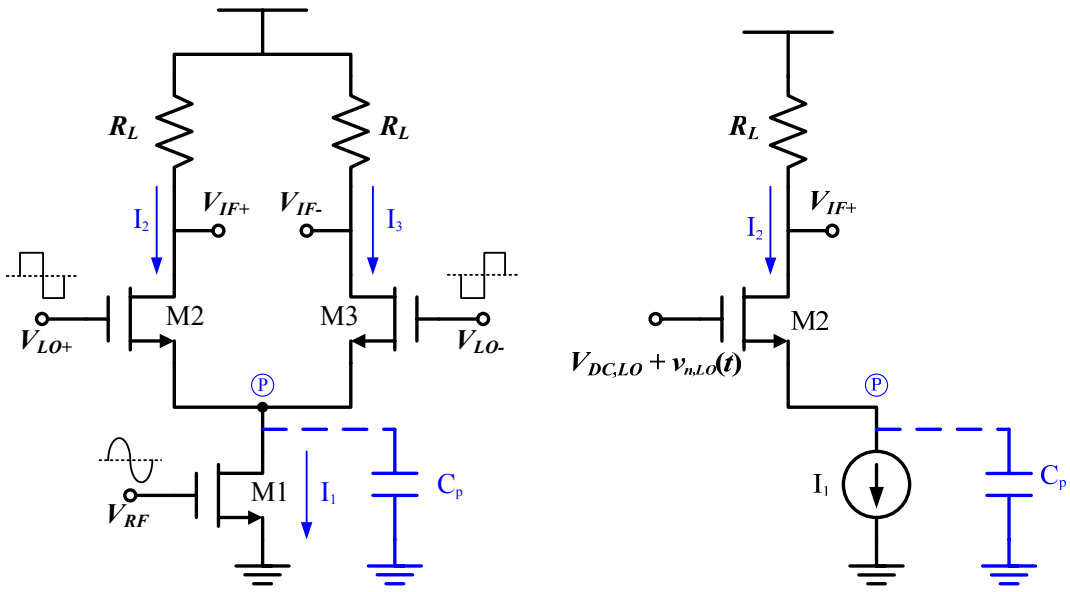
Equation (3.33) shows that the conversion gain is degraded when the non-ideal square waveform of V_{LO} is applied.

Flicker Noise

The noise figure presented by Equation (3.31) mainly considers the effect of thermal noise of the transistors. In fact, the direct conversion receiver suffers more from flicker noise due to the direct down-conversion of the RF signal to 0 Hz. The flicker noise profile will coincide with the baseband spectrum and significantly affect the SNR at the mixer output.

With the double-balanced mixer topology, the flicker noise from the driver stage will be up-converted to RF but the flicker noise of the quad switches will leak to the output as a common-mode noise. This common-mode flicker noise will be eliminated when an ideal square wave is applied to the quad switches. However, the noise cancellation is limited by the finite slope of V_{LO} and the parasitic capacitance shown in Figure 3.25 (c) and Figure 3.26 (b). The detailed analysis of this situation is presented in [41]. The direct switch noise and indirect switch noise model is proposed to explain the flicker noise phenomenon at the mixer output.

When M2 and M3 are not switched instantaneously, M2 will enter the saturation mode and act as a source follower as shown in Figure 3.26 (b). The LO noise will charge and discharge through the parasitic capacitor associated with node P. The charging and discharging noise current, i_{Cp}, will be commutated to the mixer output with twice the LO frequency. Because of the finite slew rate, LO signal with square waveform is hard to maintain at RF and even harmonics will start to appear. When this noise current is mixed with the second harmonic of the LO signal, the low frequency components will be generated and it will then form the flicker noise appearing at the mixer output. The total mixer noise can be expressed in Equation (3.34).



(a) (b)

Figure 3.28 The model of switching noise

$$\overline{V_{o,n}^2} = 8kTR_L\left(1+\gamma\frac{2R_L I_1}{\pi A_{LO}}+\gamma g_{m1}R_L\right) \tag{3.38}$$

where the first term results from the two load resistor, R_L. The second term is the output noise due to the two switches (i.e. M2 and M6), and the third term shows the noise of the driver stage (i.e. M1) transferred to the mixer output. A_{LO} is the amplitude of the sinusoidal LO signal.

Linearity and DC-offset

When the distortion performance of the mixer is assumed to be dominated by the input driver stage, the third-order intercept point of the Gilbert cell mixer can be approximated by the following expression [9].

$$V_{IIP3} \approx 4 \times \sqrt{\frac{2}{3}} \times \left(V_{gs1} - V_{t1}\right) \tag{3.39}$$

Equation (3.35) shows that the *IIP3* is directly related to the input overdrive voltage, which can be increased by biasing with higher current.

For the *IIP2*, the analysis is not straightforward. The mathematical analysis of the distortion is too complicated to gain insight into the mechanism of producing the second-order nonlinearity. Based on the mismatch analysis published in [44], the *IIP2* and dc-offset of the double-balanced mixer can be expressed in the following equations.

$$IIP2 \approx \frac{\sqrt{2}}{\eta_{nom} \cdot \pi \cdot \alpha_2^{'}} \cdot \frac{4}{\left[2\Delta\eta \cdot \left(\Delta g_m + \Delta A_{RF}\right) + \Delta R \cdot \left(1 + \Delta g_m\right) \cdot \left(1 + \Delta A_{RF}\right)\right]} \tag{3.40}$$

$$V_{offset} = \eta_{nom} R_L \cdot \frac{\Delta R}{2} \cdot \left(2I_T + \frac{1}{2} g_m \alpha_2^{'} A_{RF}^2 \right) \tag{3.41}$$

The *IIP2* of a double-balanced mixer is very sensitive to the mismatch in the load resistance. It is not as sensitive to the errors in the duty cycle because of the double-balanced configuration. It is obvious that the maximum *IIP2* is not necessarily achieved when the DC offset is zero because of the different mismatch terms in the two equations.

3.3.4 Circuit Implementations

The downconversion mixer is the most challenging circuit block to be designed and implemented for direct conversion receiver. Studies of DCR have shown that the dc-offset is the major root cause for the degradation of the receiver performance. The offset is partly from the self-mixing of the signal and its leakage, hence the port-to-port isolation of the mixer is very crucial in achieving good performance. The DC-offset can also be generated by the nonlinearity of the devices and asymmetry of the circuit during the mixing, the *IM2* products will fall into the baseband and disrupt the demodulation [6], [7], [11].

To tackle the problems arising from the finite isolation between LO-port and RF-port and also the 2nd-order intermodulation products, two designs are proposed. The first approach (MIX_v1) is shown in Figure 3.27, the mixer was realized by two separately controlled blocks, i.e. transconductance stage and switches stage. The transconductance stage was

realized by a cascode amplifier (M1 – M4), which offers better reverse isolation from the LO to the LNA. Since the current of the transconductance and switches were separately biased by Ib1, Ib2 and Ib3, the performance of the respective blocks can be optimized independently for low noise and good linearity performance. In order to achieve the requirements on linearity and conversion gain, a higher current was injected to the transconductance stage. On the other hand, a low bias current would improve the switching action and reduce the flicker noise. This kind of design flexibility cannot be provided by the conventional Gilbert cell mixer design.

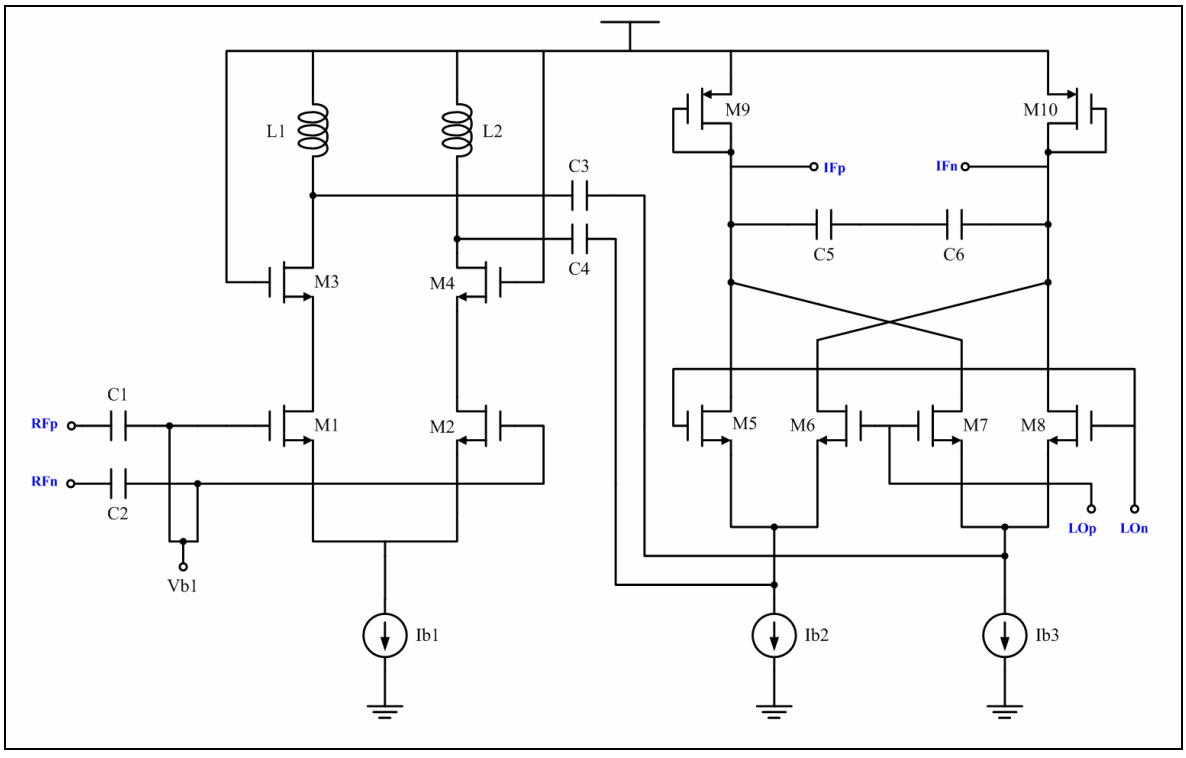


Figure 3.29 Schematic of MIX_v1

Table 3.4 The feature sizes of the elements used in MIX_v1

Transistor	W/L
M1	$200\mu m$ / $0.35\mu m$

M2	$200\mu m$ / $0.35\mu m$
M3	$200\mu m$ / $0.35\mu m$
M4	$200\mu m$ / $0.35\mu m$
M5	$100\mu m$ / $0.35\mu m$
M6	$100\mu m$ / $0.35\mu m$
M7	$100\mu m$ / $0.35\mu m$
M8	$100\mu m$ / $0.35\mu m$
M9	$100\mu m$ / $1\mu m$
M10	$100\mu m$ / $1\mu m$
Inductor	
L1	6.1 nH @ Q = 5.1
L2	6.1 nH @ Q = 5.1
Capacitor	
C1	6 pF
C2	6 pF
C3	1 pF
C4	1 pF
C5	1 pF
C6	1 pF

In the second design (MIX_v2, Figure 3.28), the mixer is based on the conventional Gilbert cell structure, however the design is modified to adopt the common-gate topology for the V-I converter instead of the common-source configuration [53]. By choosing proper sizes of the transistors, M1 and M2, the input impedance of the mixer can be designed to match the output of the LNA without using the inductor to perform the impedance transformation.

$$Z_{in} = \frac{1}{g_{m,CG}} = \frac{L}{\mu_n C_{ox} W\left(V_{gs} - V_t\right)} \tag{3.42}$$

To improve the 2nd-order linearity, a frequency trapping technique is used in the design. L1, L2, C5 and C6 shown in Figure 3.28 act as a high pass filter [42]. The higher order

harmonics of the LO signal and RF signal will leak to the ground through the HPF, but the fundamental LO signal will be blocked. If the second-order term is substantially filtered, the IM2 products will be lowered.

$$\frac{1}{2\pi\sqrt{L_1 C_5}} \geq 2f_o \tag{3.43}$$

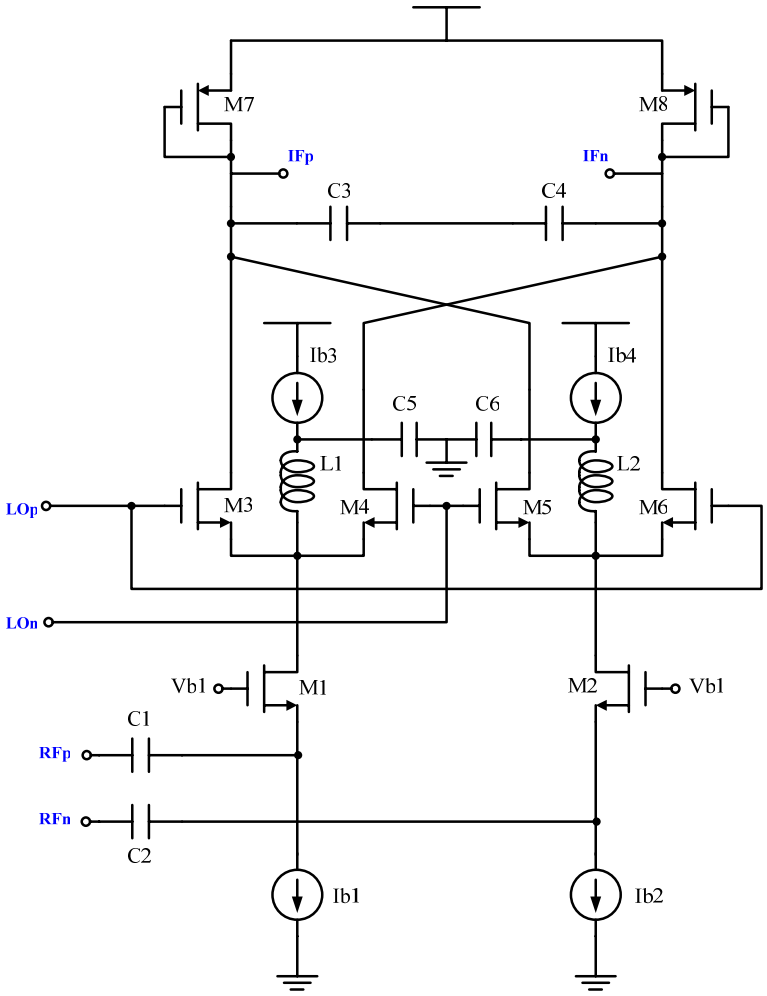


Figure 3.30 Schematic of MIX_v2

Another modification is to connect the current sources to the common node of transconductance and switches. Since the flicker noise of the MOS transistor is directly proportional to the drain current as shown in Equation (3.40). With lower current passing through the quad switches, the mixing can be more ideal when the large LO is applied to the gates of the quad transistors.

$$\frac{\bar{i}_n^2}{\Delta f} = \frac{K_1 I_D}{C_{ox} L} \times \frac{1}{f} \tag{3.44}$$

With the current injection technique, the flicker noise can be reduced without disrupting the biasing current of the common-gate stage. When the current is steered away from the switches, the rise and fall time could be improved during the charging and discharging action, hence the square-wave like switching can be obtained.

Table 3.5 The feature sizes of the elements used in MIX_v2

Transistor	**W/L**
M1	340μm / 0.35μm
M2	340μm / 0.35μm
M3	100μm / 0.35μm
M4	100μm / 0.35μm
M5	100μm / 0.35μm
M6	100μm / 0.35μm
M7	100μm / 1μm
M8	100μm / 1μm
Inductor	
L1	9.0 nH @ Q = 4.9
L2	9.0 nH @ Q = 4.9
Capacitor	
C1	6 pF
C2	6 pF

C3	1 *pF*
C4	1 *pF*
C5	0.3 *pF*
C6	0.3 *pF*

3.3.5 Simulation Results of Mixer

Two mixer circuits are designed and simulated in this project. In MIX_v1, the two-stage cascode topology is selected, so that the mixing can be done in two steps. The conversion gain of MIX_v1 is provided by the cascoded transconductance stage and the down-conversion is done by the quad switches. The simulated results of MIX_v1 are presented in Figure 3.29 to Figure 3.32. The voltage conversion gain, noise figure, *P-1dB* and *IIP3* are 6.3 dB, 8.4 dB, -17 dBm and -7 dBm respectively. All the data is based on an LO input of -5 dBm. There are problems encountered during the *IIP2* simulation. For the ideal and symmetrical differential design, *IIP2* is close to inifinte as shown in Figure 3.32 (a) and it only degrades when mismatches are introduced to the circuit. In the simulation, it is hard to make an assumption on the mismatches because no foundry data is provided. If 1% of load mismatch is assumed for the MIX_v1, the simulated IIP2 is +49.7 dBm.

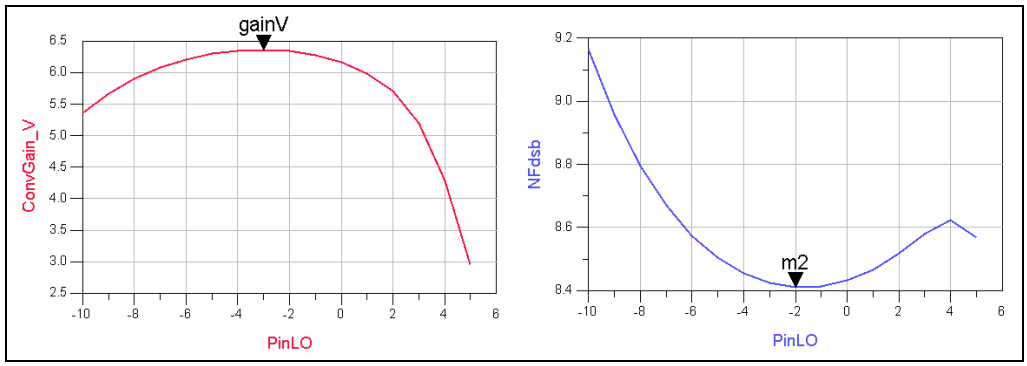


Figure 3.31 Voltage conversion gain and double side band noise figure of MIX_v1

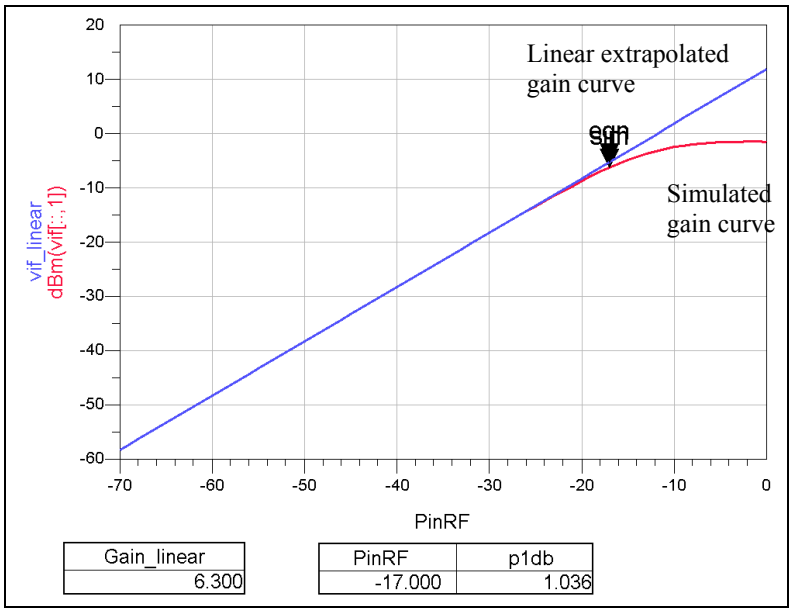


Figure 3.32 1-dB compression point of MIX_v1

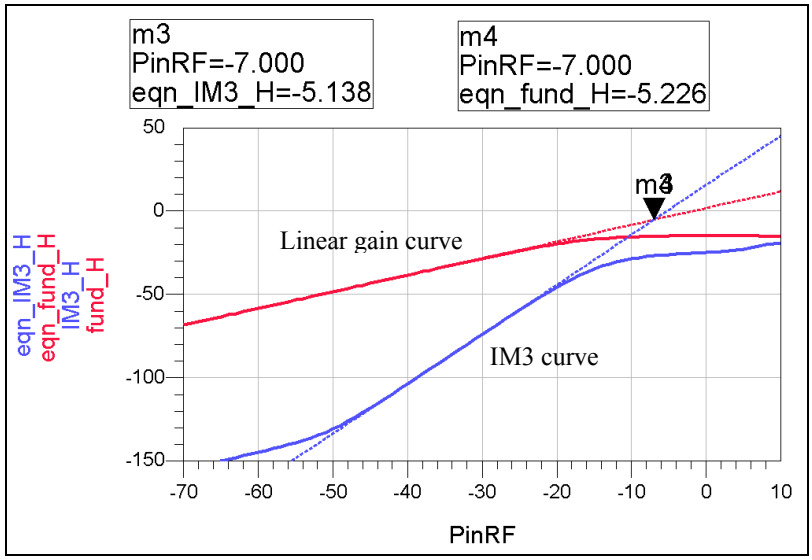
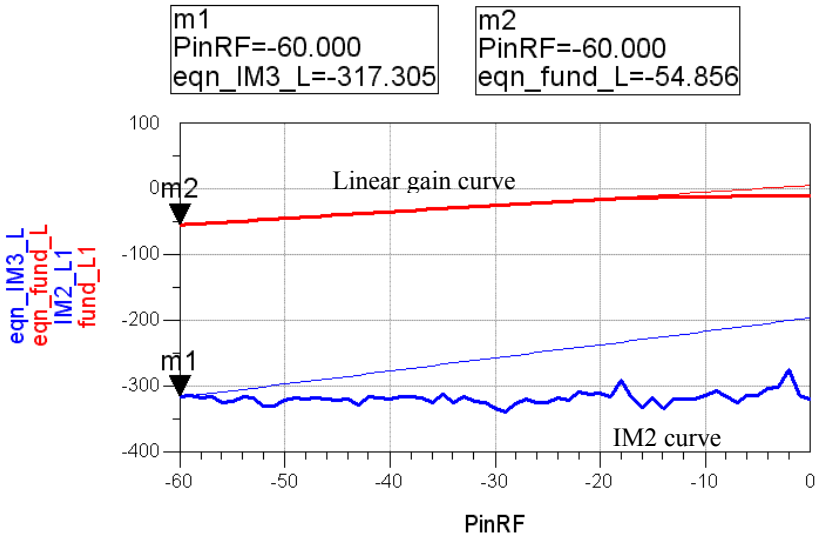
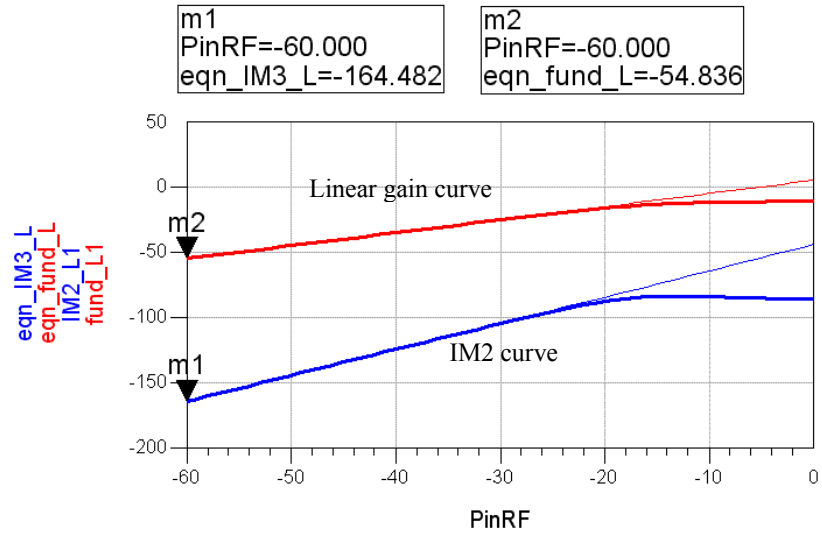


Figure 3.33 3rd-order intercept point of MIX_v1



(a)



(b)

Figure 3.34 2nd-order intercept point of MIX_v1(a) no load mismatch (b) 1% load mismatch

For the MIX_v2, the current injection topology with high pass filter is adopted. The simulated conversion gain and noise figure of MIX_v2 are 9.2 dB (Figure 3.33) and 10 dB (Figure 3.34) respectively. Although MIX_v2 shows poorer noise figure than MIX_v1, but the IIP3 is 2 dB better than MIX_v1. This improvement is critical in the mixer design because the input signal can be as large as 0 dBm if the bypass switch of the LNA is not

turned on. Although the conversion gain of both versions are below 10 dB, this is more than the requirement because the simulated gain of the LNA is about 26 dB (Table 3.3), which is enough to meet the front-end requirement. With 1% of load mismatch, the simulated IIP2 for MIX_v2 is about +50 dBm

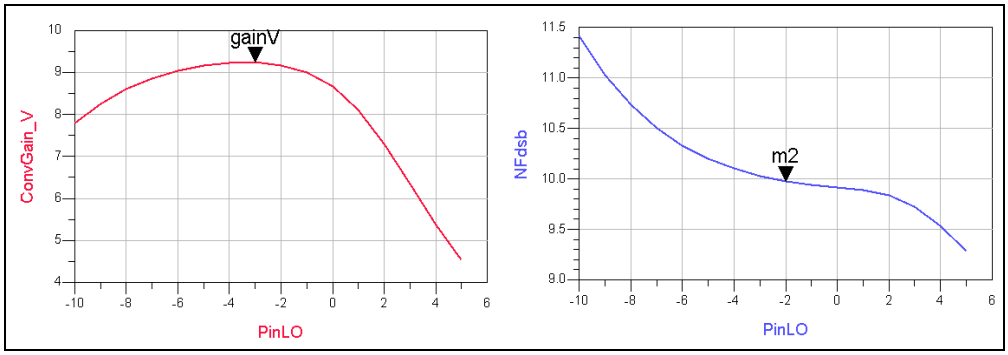


Figure 3.35 Voltage conversion gain and double side band noise figure of MIX_v2

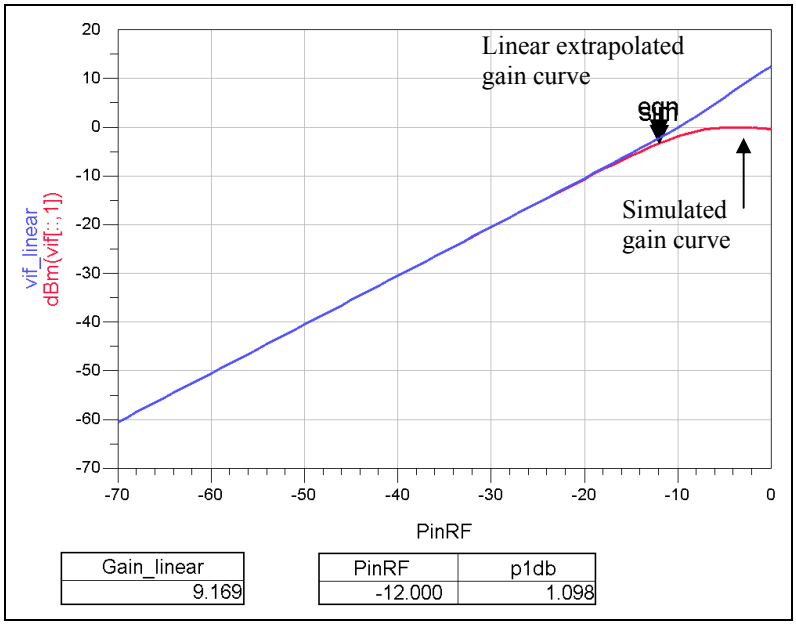


Figure 3.36 1-dB compression point of MIX_v2

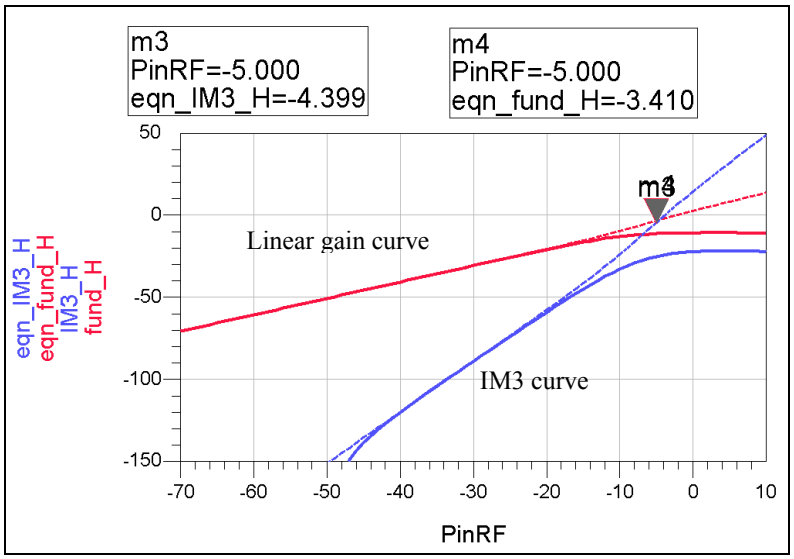
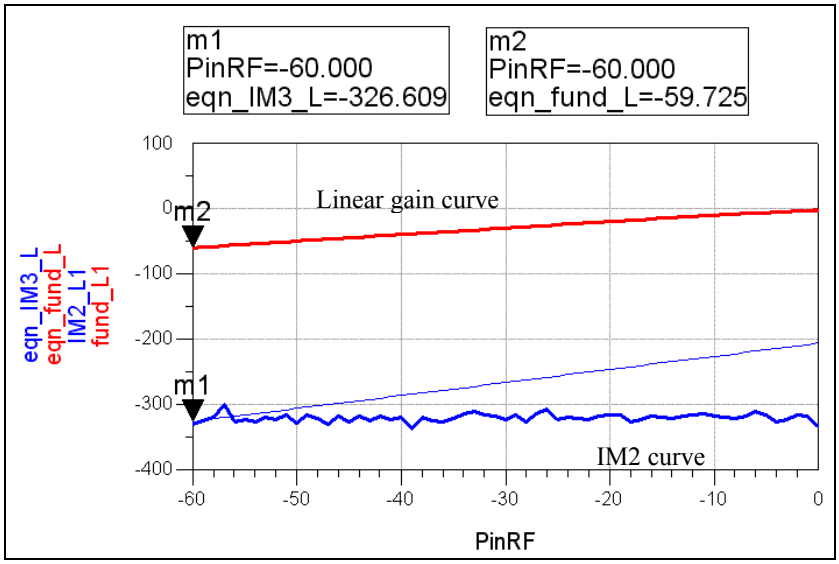
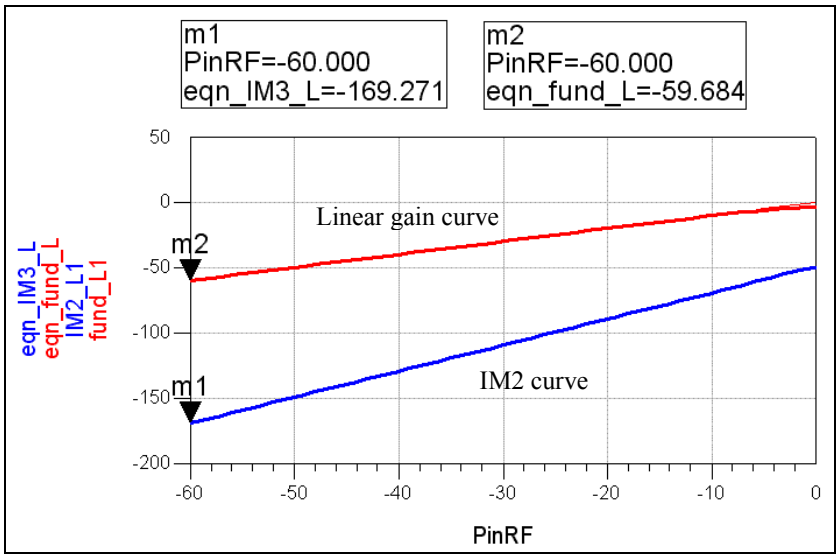


Figure 3.37 3rd-order intercept point of MIX_v2



(a)



(b)

Figure 3.38 2nd-order intercept point of MIX_v1(a) no load mismatch (b) 1% load mismatch

The supplementary results for the simulation of the reverse isolation and other design parameters of the mixer can be found in Appendix A.2. All the results from the mixer simulations are summarized in Table 3.6.

Table 3.6 Summary of mixer simulation results

Parameter	**Description**	**MIX v.1**	**MIX v.2**	**Unit**
f_c	RF frequency	2145	2145	*MHz*
f_{LO}	Oscillator frequency	2140	2140	*MHz*
P_{LO}	Oscillator power	-5	-5	*dBm*
G_c	Voltage conversion gain	6.3	9.2	*dB*
P_{1dB}	1-dB gain compression point	-17.0	-12.0	*dBm*
IIP3	3rd-order intercept point	-7.0	-5.0	*dBm*
IIP2	2nd-order intercept point	+49.7	+50.0	*dBm*
NF	DSB noise figure @ 5 MHz	8.4	10	*dB*
$G_{LO\text{-}RF}$	LO-RF isolation	>100	>100	*dB*
I_d	Current consumption	3.04	3.02	*mA*

3.4 Design of an Integrated RF Front-end

3.4.1 Circuit Implementations

The RF circuits like LNA and mixer have been separately analyzed and discussed in the previous sections. Two LNA designs and two mixer topologies have been proposed and simulated. However, it is necessary to integrate them as a front-end design for the direct conversion receiver, so that the RF system performance can be verified.

Due to the limited silicon area for the tapeout, it was not possible to test all the combinations of the LNAs and the mixers. Based on the system analysis of the DCR for W-CDMA application, the performance of port-to-port isolation and IM2 become the criteria for selecting the LNA and mixer circuit. As a result, the differential LNA_v1 and the current injection mixer, MIX_v2, are cascaded to form the RF front-end for the DCR. The schematic of the circuits are shown in Figure 3.14 and Figure 3.28. To interface the LNA and mixer, ac coupling capacitors are used. The low frequency second-order nonlinear products and dc-offset from the LNA will be blocked by the coupling capacitors.

3.4.2 Simulation Results of the RF Front-end Circuits

The simulated results of the proposed RF front-end design are presented in Figure 3.37 to Figure 3.44. Two operating modes are simulated. In the high gain mode, the spot noise figure and voltage conversion gain of the RF front-end at 2.14 GHz are 3.3 dB and 34 dB respectively. When the LNA is switched to low gain mode, the noise figure and gain are reduced to 4.7 dB and 18 dB. This result shows that the noise figure of the front-end is still kept below 5 dB even when there is a drastic change in front-end gain. The input matching of the LNA, shown in Figure 3.37 and Figure 3.38, is only slightly affected by the gain switching.

The performance of *P-1dB*, *IIP3* and *IIP2* are shown in Figure 3.39 to Figure 3.44. Since the loss of the duplexer is not considered in the simulation, it is not surprising to find that the *IIP3* is below the requirement during the low gain mode. With the 3 dB loss of duplexer added to the system, the front-end circuit can meet the linearity requirements in most of the situations.

The supplementary results for the simulation of reverse isolation and other design parameters of the RF front-end circuits can be found in Appendix A.3.

Table 3.7 Summary of RF front-end simulation results (LNA v.1 + Mix v.2*)*

Parameter	**Description**	**Spec.**	**HG / LG**	**Unit**
f_c	Operating frequency	2110 – 2170	2140	*MHz*
G	Voltage gain	26	34 / 18	*dB*
NF	Spot noise figure	4.3	3.3 / 4.7	*dB*
IIP2	2^{nd}-order intercept point	>30	+54/+75	*dBm*
IIP3	3^{rd}-order intercept point	-11	-29 / -12	*dBm*
P_{1dB}	1-dB gain compression point	-22	-37 / -21	*dBm*
$G_{LO\text{-}RF}$	LO-RF isolation	>60	>90	*dB*
S_{11}	Input reflection coefficient	<-10	-12	*dB*
I_d	Current consumption	20	15 / 11	*mA*

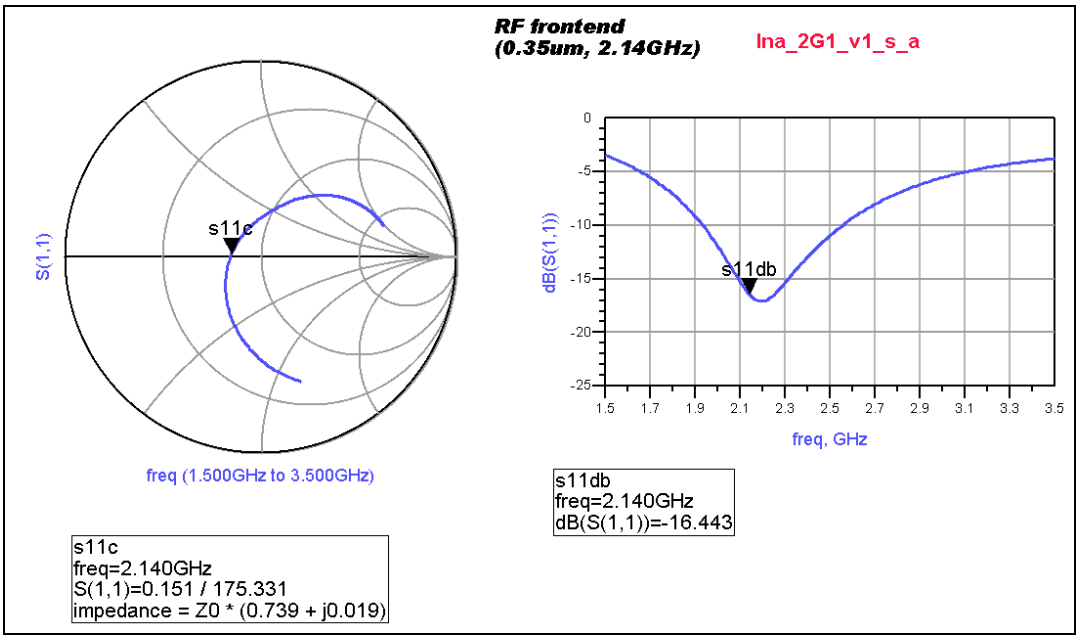


Figure 3.39 S_{11} of RF front-end (high gain mode)

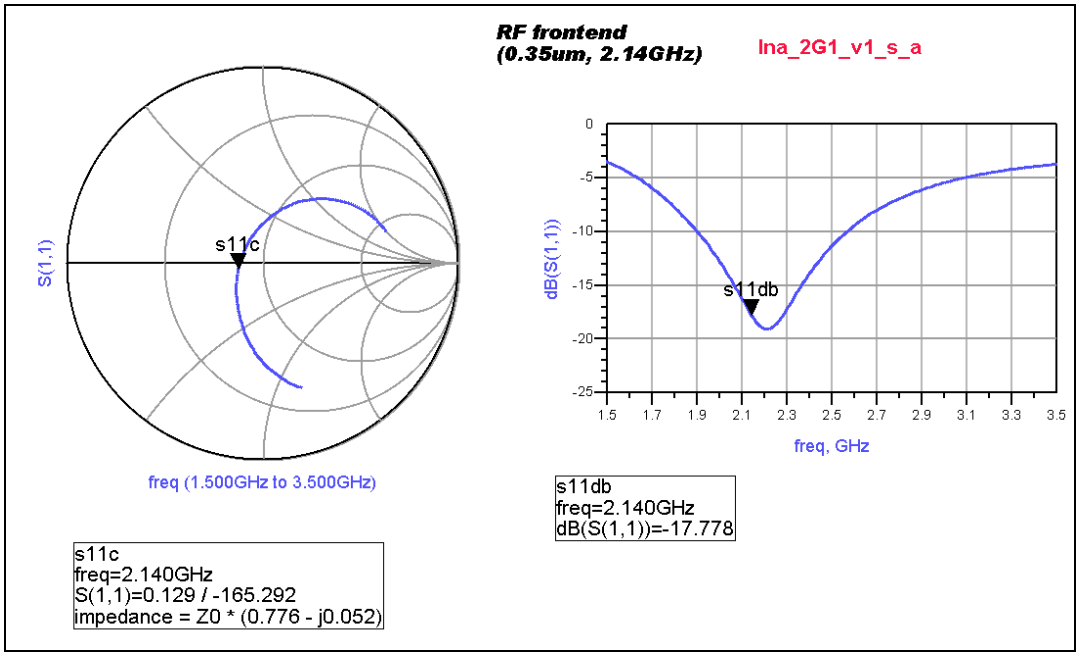


Figure 3.40 S_{11} of RF front-end (low gain mode)

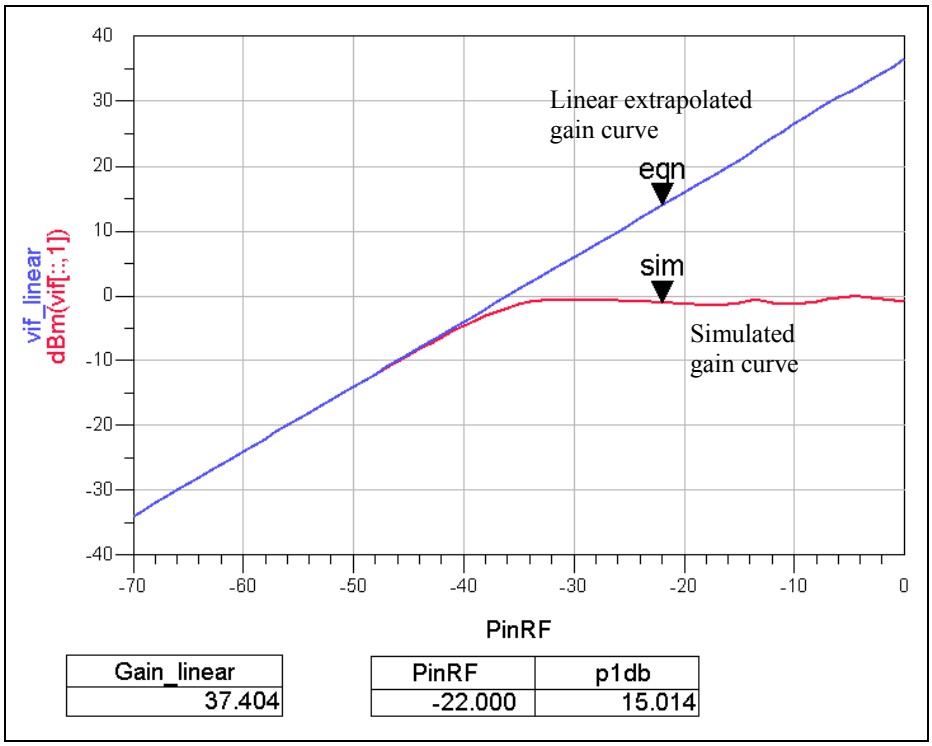


Figure 3.41 1-dB compression point of RF front-end (high gain mode)

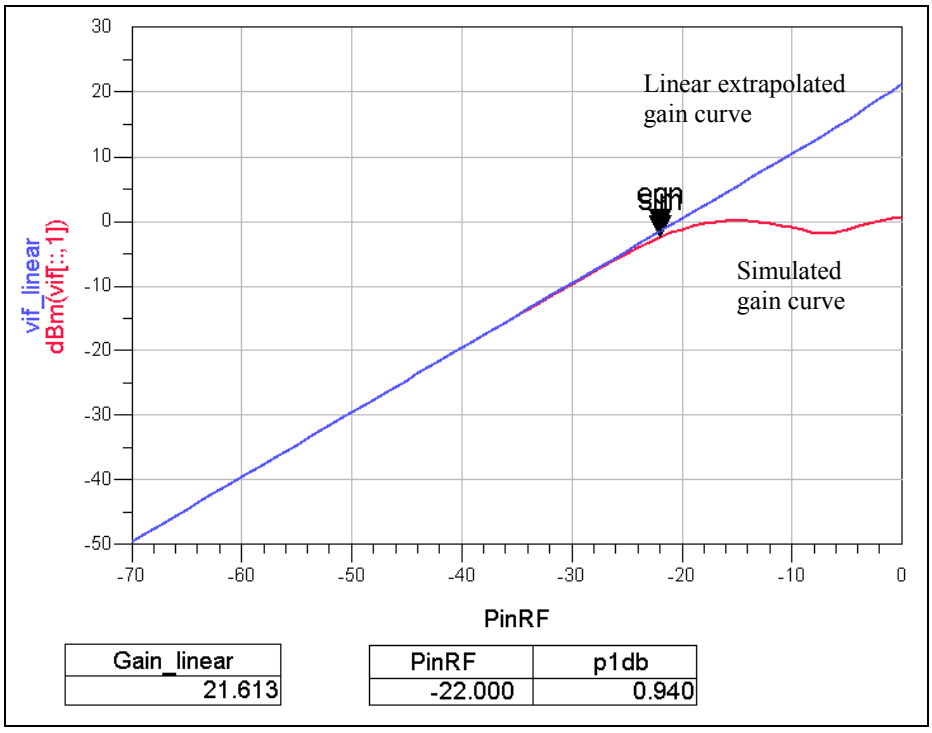


Figure 3.42 1-dB compression point of RF front-end (low gain mode)

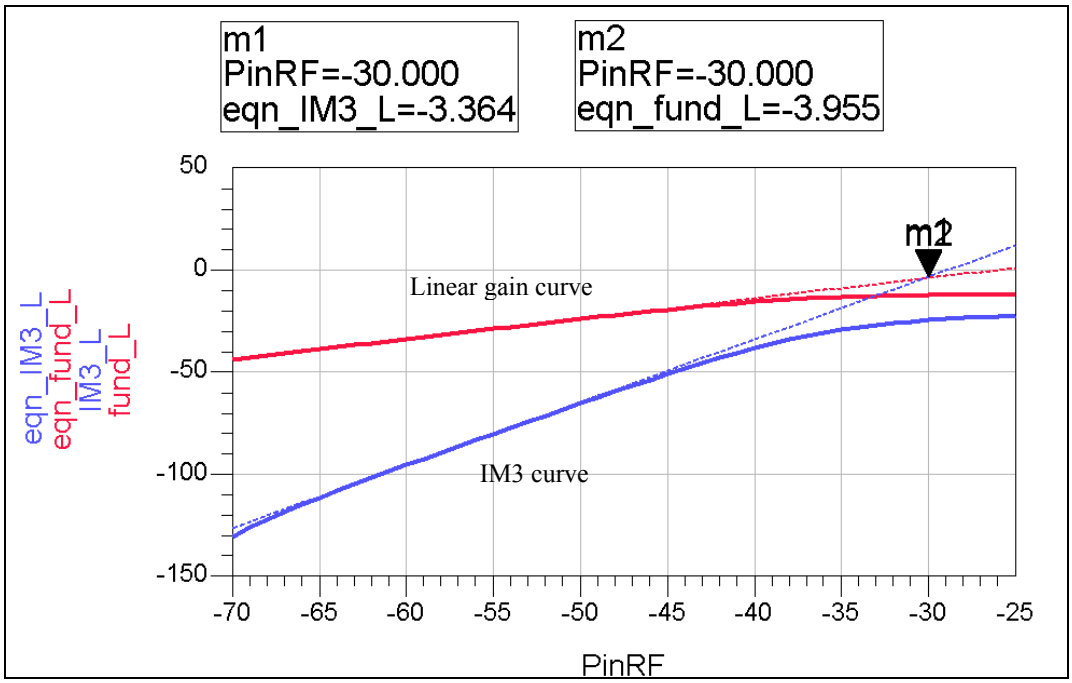


Figure 3.43 IIP3 of RF front-end (high gain mode)

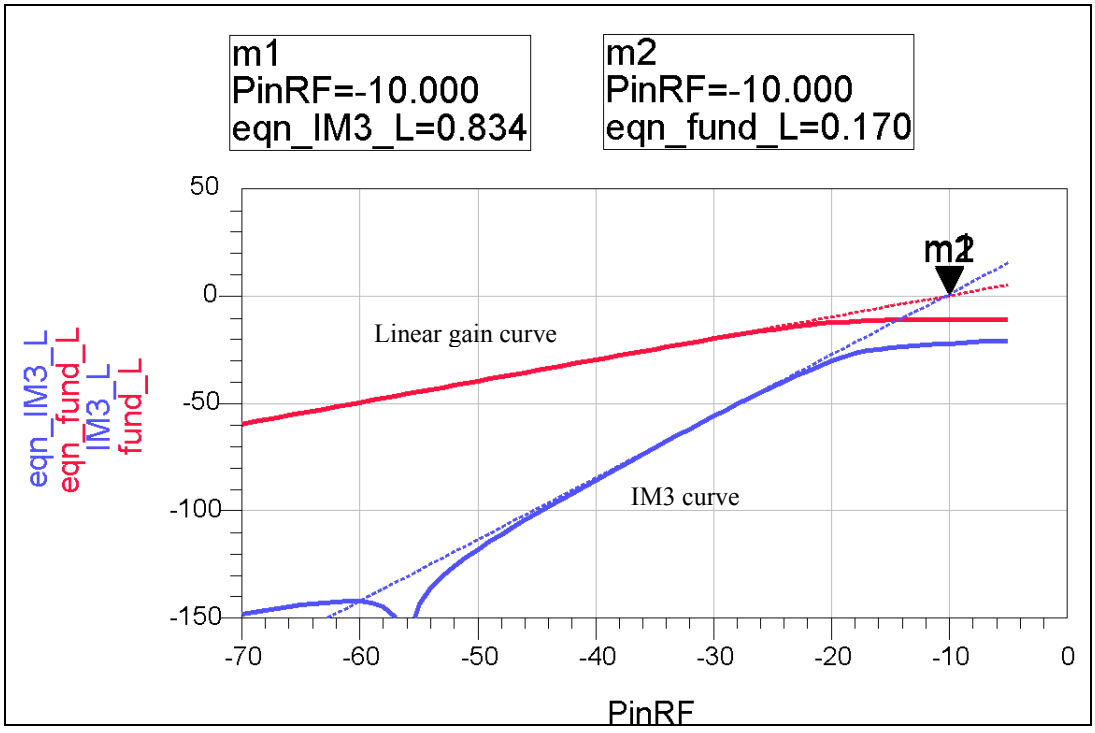


Figure 3.44 IIP3 of RF front-end (low gain mode)

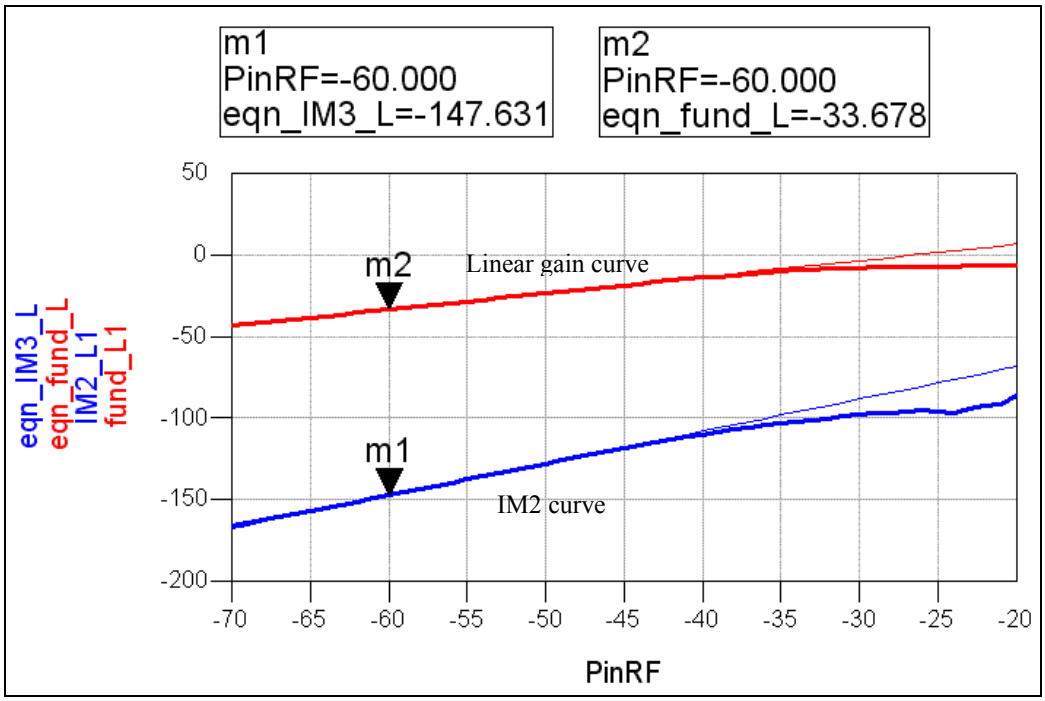


Figure 3.45 IIP2 of RF front-end (high gain mode)

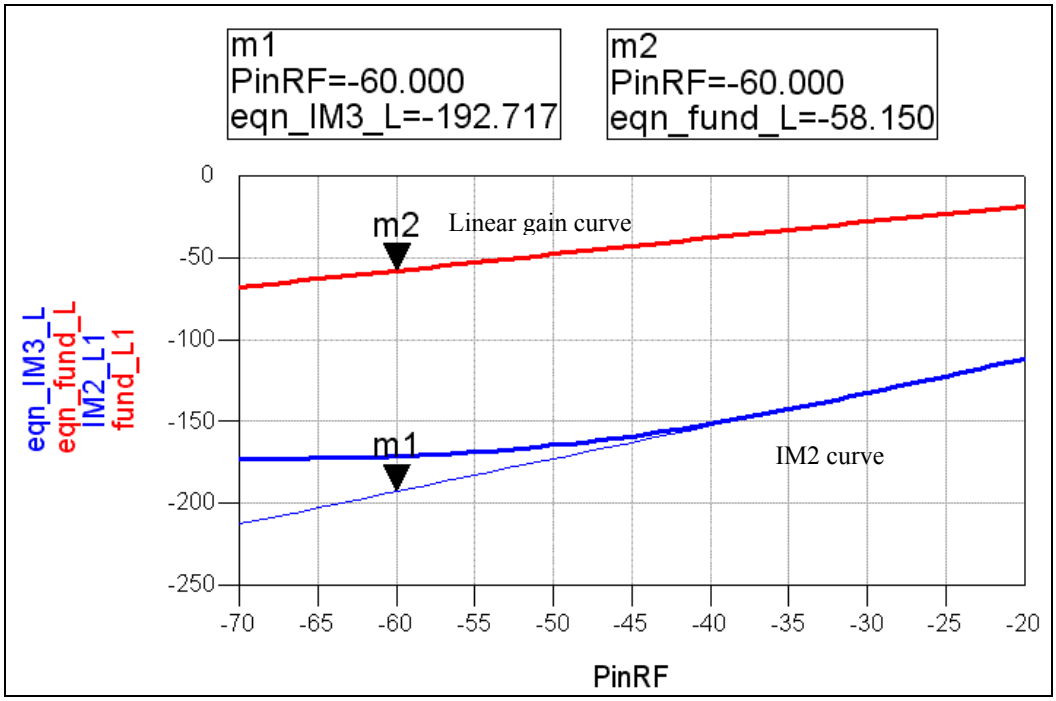


Figure 3.46 IIP2 of RF front-end (low gain mode)

Chapter 4 Experimental Results

4.1 Introduction

Two LNAs, two mixers, and one integrated RF front-end have been implemented and laid out separately. The test chips have been fabricated in Chartered Semiconductor Manufacturing 0.35 μm CMOS process with four metal layers and RF options. All the dies are mounted and wire-bonded in QFP-24 pin package. The packages are then soldered on the FR-4 printed circuit boards (PCB) for testing.

The layout drawings of the circuits and the designs of the PCB can be found in Appendix B and Appendix C respectively. The sizes of each die, which are inclusive of the pads, are tabulated in Table 4.1.

Table 4.1 Summary of test chip versions

Circuit Name	Description	Area
LNA_v1	Differential LNA with gain control	1.8×1.2 mm^2
LNA_v2	Single-to-differential LNA with gain control	1.5×1.2 mm^2
MIX_v1	Two-stage cascode Gilbert cell mixer	1.5×1.2 mm^2
MIX_v2	Current injected Gilbert cell mixer	1.5×1.2 mm^2
RFE_v2	LNA_v1 + MIX_v2	2.6×1.2 mm^2

4.2 Test Methodology

The measurements of the RF front-end circuits require many high-performance equipments, such as a vector network analyzer, spectrum analyzer, noise figure analyzer, etc. Most of the RF equipment is designed to work with single-ended signals rather than differential signals, hence an external power splitter and power combiner are required for the signal conversion. The calibration of these devices before the measurement is essential because the signal loss and phase distortion introduced by the power splitter and power combiner can affect the measurement accuracy.

To characterize the RF circuits, the parameters like signal gain, noise figure, S-parameters, second-order and third-order intermodulation products are measured. It is straightforward to measure the LNA performances because the test frequency at input and output of the LNA is the same. However, it is challenging to perform measurements on the mixer and the integrated front-end design. The down-converted baseband signal falls exactly at dc because $f_{IF} = 0\ Hz$. The accuracy of the measured signal level and noise level are compromised by the dc disturbance from the devices and equipment. To mitigate the issue of dc disturbance during the measurement, $f_{IF} = f_{RF} - f_{LO} = 1$ MHz is chosen, so that the signal level and the noise floor can measured accurately.

The noise figure measurement of the mixer and the front-end circuits for the direct conversion receiver become another issue because the minimum frequency that the noise figure analyzer can support is 10 MHz. To circumvent this problem, another test

methodology, which is called “Gain Method” is adopted [46]. For the details of this method and the test setup for other measurements, the reader can refer to Appendix D.

4.3 Measurement of Test Chips

The performances of low noise amplifier, mixer and integrated RF front-end have been summarized in Table 4.2, 4.3 and 4.4 respectively. Most of the measurements are performed at room temperature, i.e. 27°C, with 3V power supply using an external LO source of -5 dBm. The RF and LO frequencies during the characterization of the mixer and the RF front-end were set to 2.141 GHz and 2.140 GHz respectively in most of the scenarios.

In terms of dc characteristic, the measured current consumption of the test chips and dc voltage level at respective nodes are slightly higher than the simulations but the data is still within the acceptable ranges of tolerance.

4.3.1 Low Noise Amplifier

The measured results of the low noise amplifier are shown in Figure 4.2 to Figure 4.14 and the performance is summarized in Table 4.2 and Table 4.3.

Table 4.2 Summary of low noise amplifier measurements (LNA_v1)

Parameter	**Description**	**Simulation**		**Measurement**		**Unit**
		HG	**LG**	**HG**	**LG**	
f_c	Operating frequency	2140		2140		*MHz*
NF	Spot noise figure	3.1	-	5.7	-	*dB*
G	Power gain	26.9	3.6	22	-16	*dB*
P_{1dB}	1-dB gain compression point	-30	-13	-27	10	*dBm*
IIP3	3rd-order intercept point	-21	-2.5	-11	14	*dBm*
S_{11}	Input reflection coefficient	-17	-	-8	-	*dB*
I_d	Current consumption	12.1	8.1	11	8	*mA*

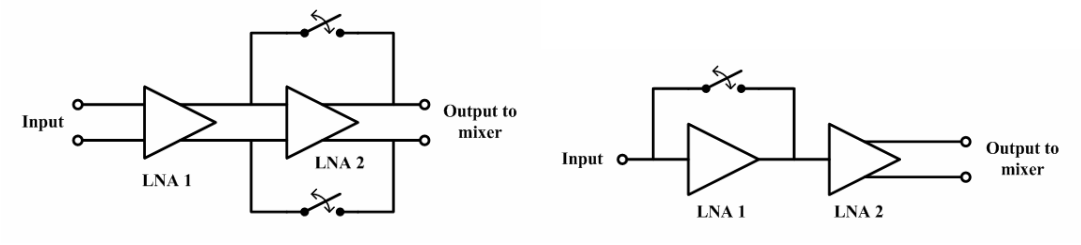
Table 4.3 Summary of low noise amplifier measurements (LNA_v2)

Parameter	**Description**	**Simulation**		**Measurement**		**Unit**
		HG	**LG**	**HG**	**LG**	
f_c	Operating frequency	2140		2140		*MHz*
NF	Spot noise figure	3.2	-	4.1	-	*dB*
G	Power gain	26.6	-12	24	-14	*dB*
P_{1dB}	1-dB gain compression point	-34	-10	-22	10	*dBm*
IIP3	3rd-order intercept point	-24	0	-13	18	*dBm*
S_{11}	Input reflection coefficient	-13	-	-12	-	*dB*
I_d	Current consumption	9.6	4.5	10	6	*mA*

The important parameters such as noise figure, power gain, and input reflection coefficient have been measured from 2000 MHz to 2300 MHz. The power gain of LNA_v1 and LNA_v2 are 22 dB and 24 dB respectively at 2140 MHz, which are about 3 dB lower than simulations with reference to 50 Ω. Similarly, the noise figure curve shown in Figure 4.4 and Figure 4.5, the degradations of the noise figure are worse than expected, the measured figures exceed the simulations by 2 dB for LNA_v1 and 0.7 dB for LNA_v2. It is also found that the S_{11} curve of Figure 4.14 is drifted away from the optimum 2140 GHz. The drift of S_{11} response has more significant impact on the performance of the fully differential LNA_v1 than LNA_v2.

The gain curves shown in Figure 4.2 and Figure 4.3 for the low gain mode indicate that the gain control features are not working as expected. The reductions of gain are about 30 dB for both designs, the attenuation is too large and these may impact to the *SNR* of the receiver output considerably even when the receiver is operating in the strong input signal condition. To meet the linearity requirement in some circumstances, the power gain of the LNA is reduced through bypassing the gain stages, which are activated by the MOS switches. The gain measurement showed that the switches might not function properly. The signal loss when passing through the switches is too large. one of the possible reasons may be due to the breakdown of such switches. The bonding pad used for the input of the low noise amplifier is not electrostatic-discharge (ESD) protected. Furthermore, the aspect ratio used by the switch is W/L = 5 μm/0.35 μm, which may be too weak subjected to the ESD when the IC is handled and manually soldered on the PCB. The signal loss due to the

switches may be under-estimated due to the model used in the design. The RF model of the switch is not available when the bypass route is designed, hence the typical dc model, which is only valid up to 1 GHz, is used in the simulation.



(a) (b)

Figure 4.1 Illustration of bypass topologies for LNA operating in low gain mode: (a) LNA_v1; (b) LNA_v2.

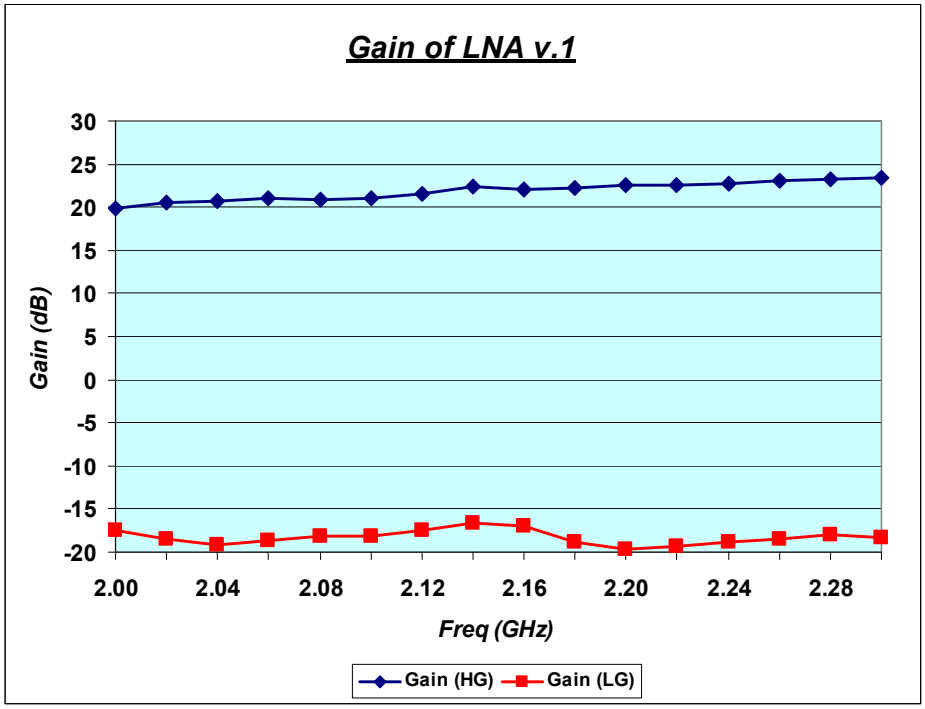


Figure 4.2 Gain of LNA_v1 (high/low gain mode)

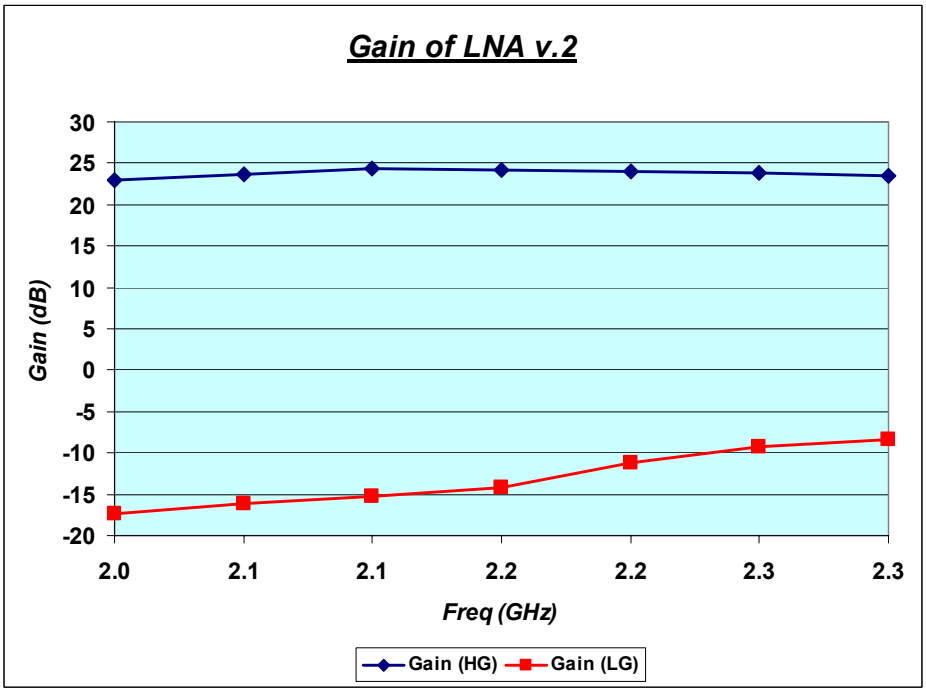


Figure 4.3 Gain of LNA_v2 (high/low gain mode)

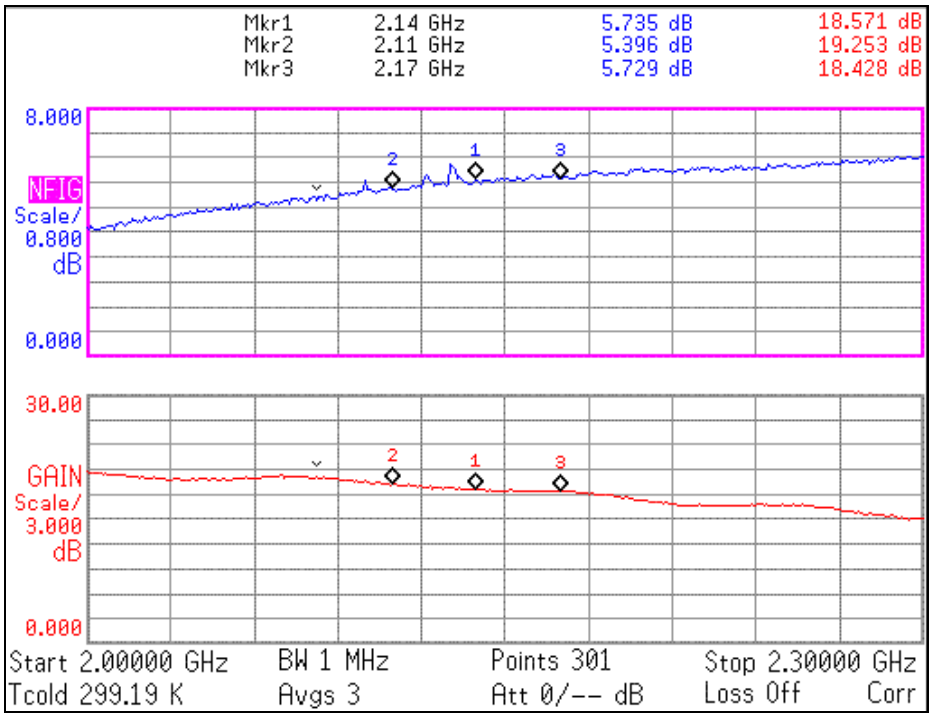


Figure 4.4 Noise figure of LNA_v1 (high gain mode)

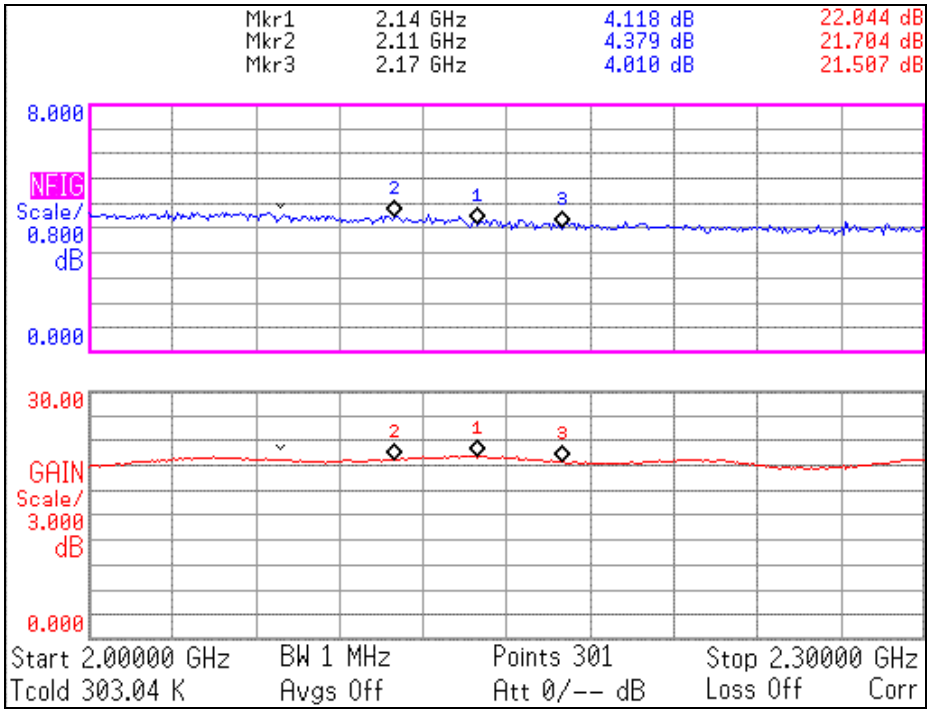


Figure 4.5 Noise figure of LNA_v2 (high gain mode)

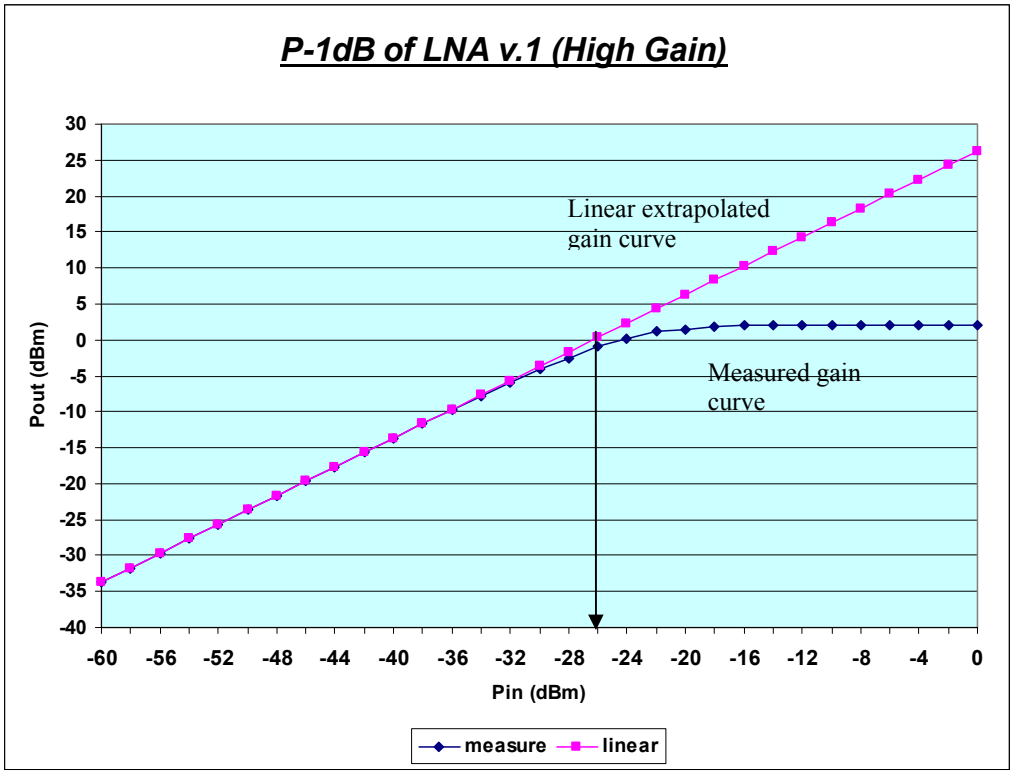


Figure 4.6 1-dB compression point of LNA_v1 (high gain mode)

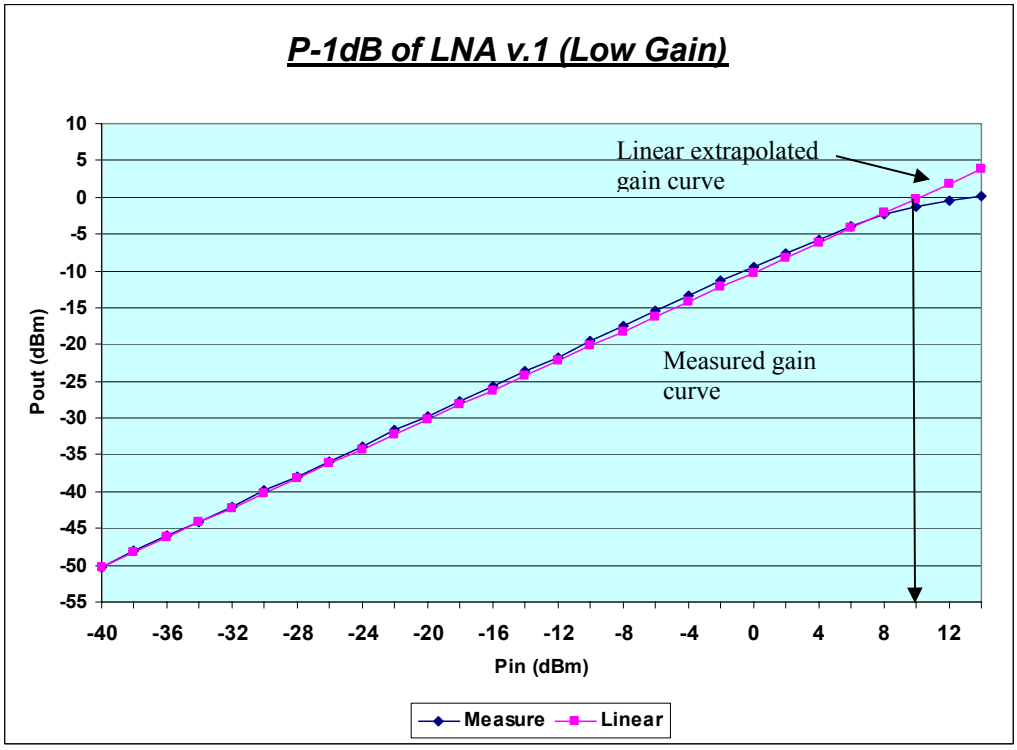


Figure 4.7 1-dB compression point of LNA_v1 (low gain mode)

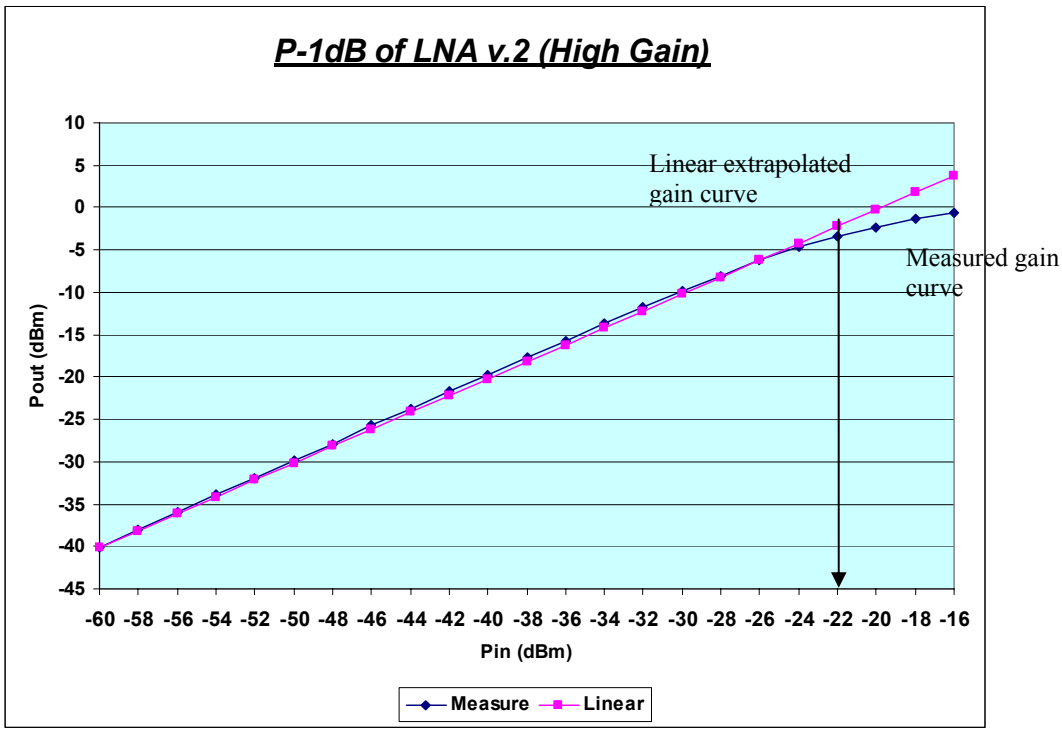


Figure 4.8 1-dB compression point of LNA_v2 (high gain mode)

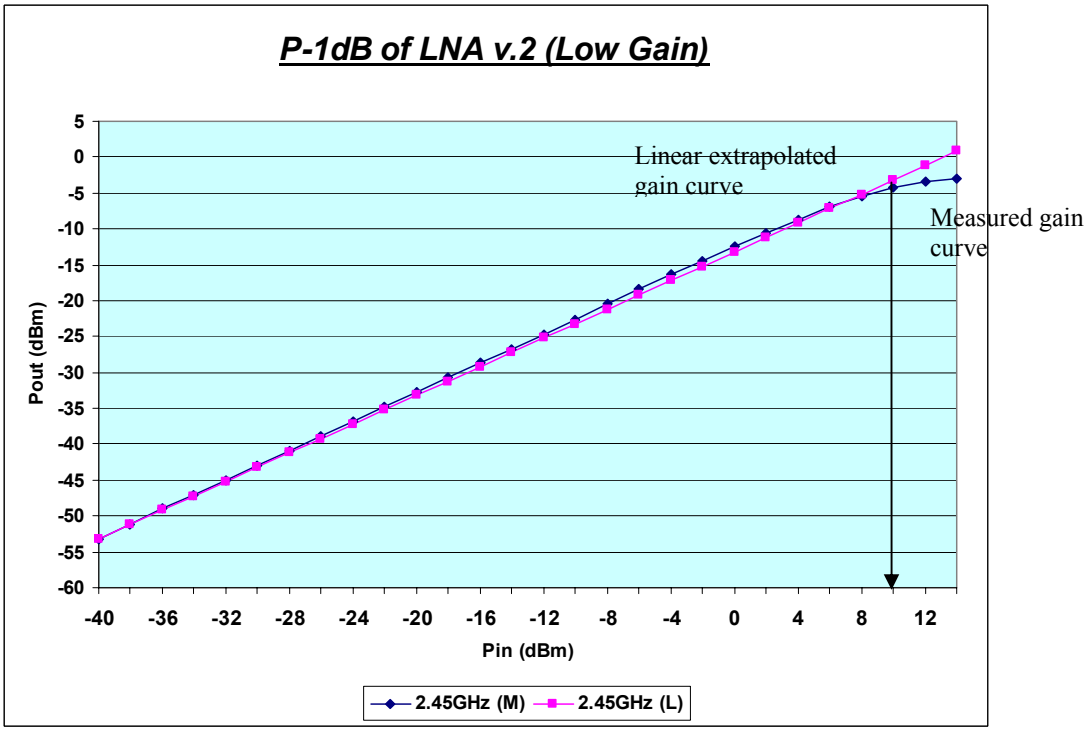


Figure 4.9 1-dB compression point of LNA_v2 (low gain mode)

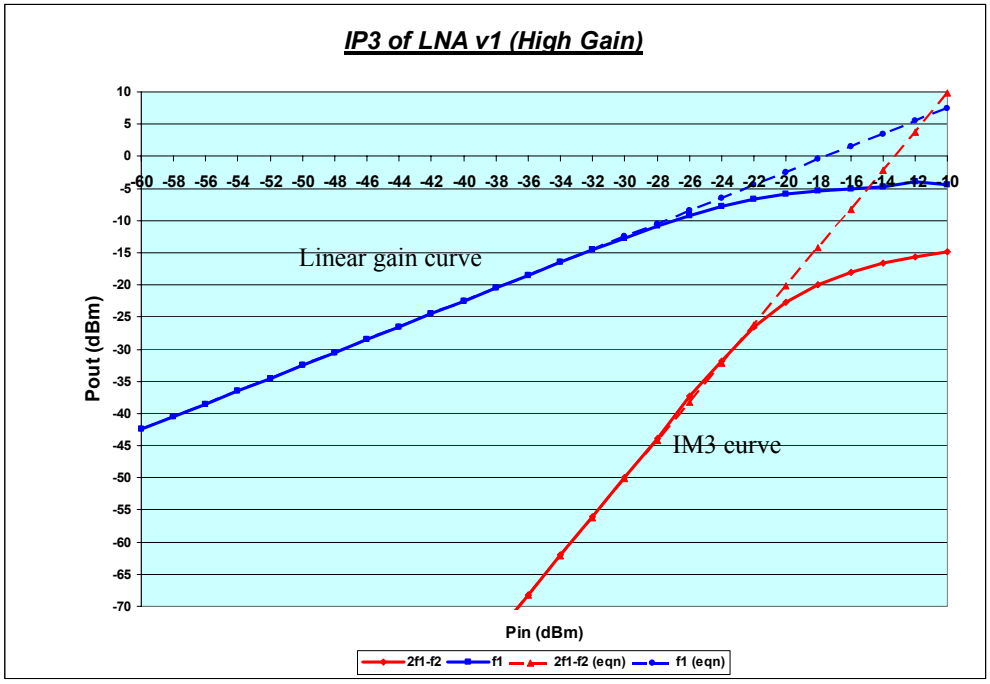


Figure 4.10 3rd-order intercept point of LNA_v1 (high gain mode)

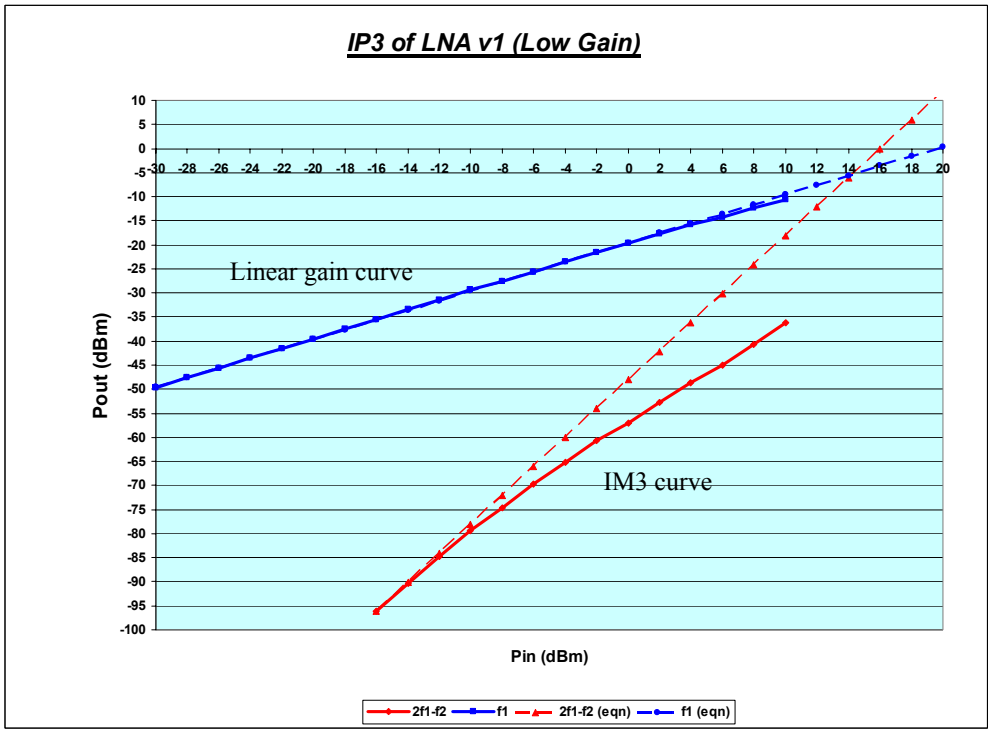


Figure 4.11 3rd-order intercept point of LNA_v1 (low gain mode)

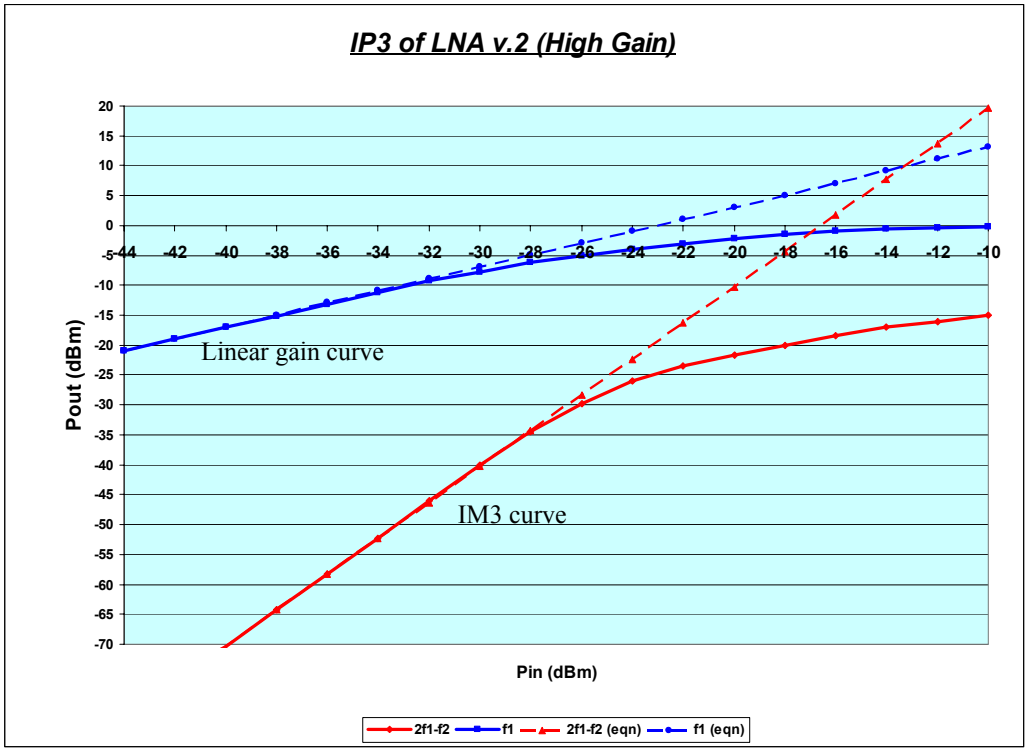


Figure 4.12 3rd-order intercept point of LNA_v2 (high gain mode)

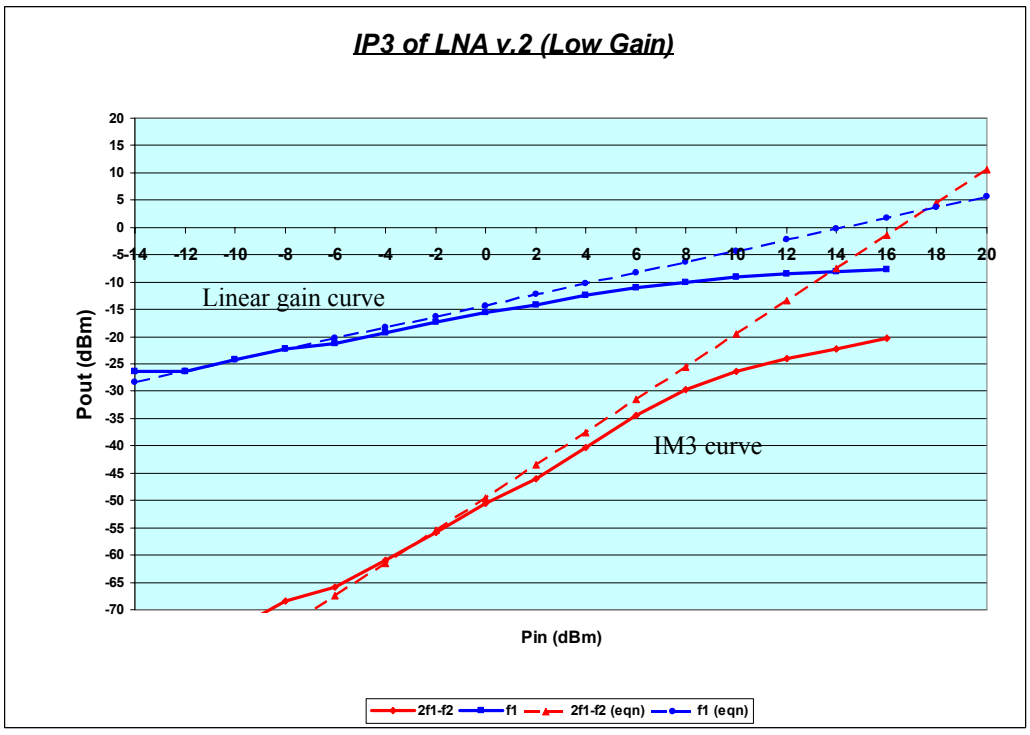


Figure 4.13 3rd-order intercept point of LNA_v2 (low gain mode)

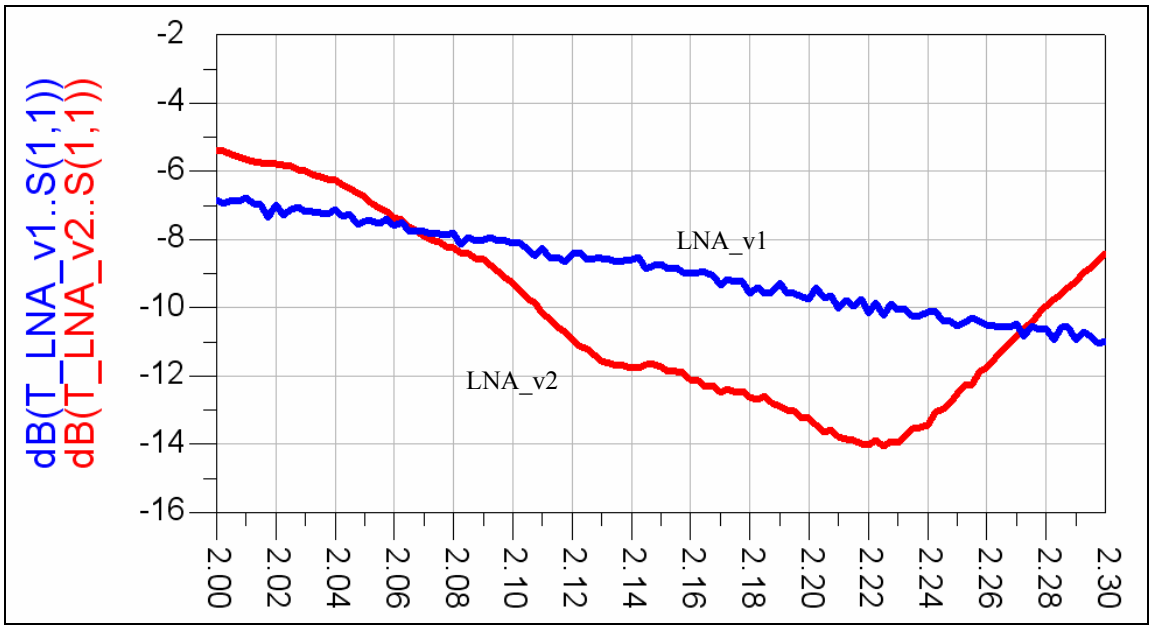


Figure 4.14 S_{11} of LNA_v1 and LNA_v2 (high gain mode)

After the measurements, the degradation of gain and noise figure are studied. It is found that the parasitic effects of some components are not well simulated during the design phase. This problem is exacerbated when the critical post-simulations are not performed after the layout. The foundry do not provide CMOS 0.35μm product design kit (PDK) for the ADS environment. Hence, the parasitic resistance and capacitance based on the actual layout are not extracted. Although IME in-house extracted RF models are used in the simulation, these RF models are not scalable and limited sizes of NMOS transistor, MIM capacitors, inductors and transmission lines are provided. For the biasing blocks and the switches, the dc model provided by the foundry is used. However, the parasitic elements associated with this scalable dc model become unrealistic when the operating frequency is above 1 GHz. The loss due to the additional parasitic networks based on the actual layout is not accounted for in the simulation. Another effect may be overlooked came from the coupling capacitance among the neighbouring circuit elements.

It is also suspected that the estimated model of bondpad (Figue 4.15) and package (Figure 4.16) applied in the simulation may contribute to such degradation. The C2 in Figure 4.15 may be under-estimated. It should be 150 fF after checking with the measured data. Additional series resistance of 1.5 Ω and inductor of 0.8 nH are needed to account for the bonding wire and PCB traces. In the previous simulations, the direct connection of the power supply and ground to the LNA as shown in Figure 4.17 (a) is applied. In the actual chip connections, the power supply and circuit ground are connected to the PCB through the package, bonding wire and pads as shown in Figure 4.17 (b). When all these undesirable effects are included in the simulation of LNA_v1, the simulated gain is reduced from 26.6 dB to 22.9 dB, which is closer to the 22 dB of measured gain. The same degradation can be found on the NF, the simulation after the measurement shows that the NF is degraded to 4.8 dB from 3.1 dB as shown in Figure 4.19.

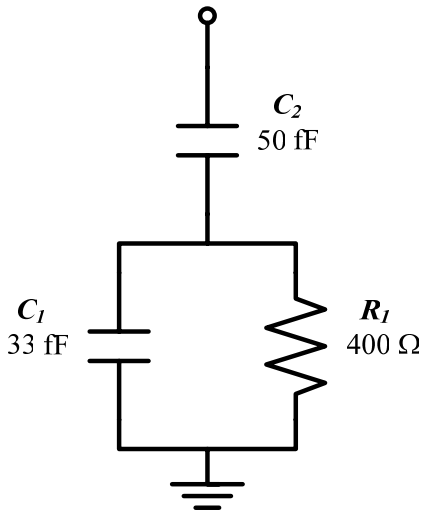


Figure 4.15 The estimated model of bond pad

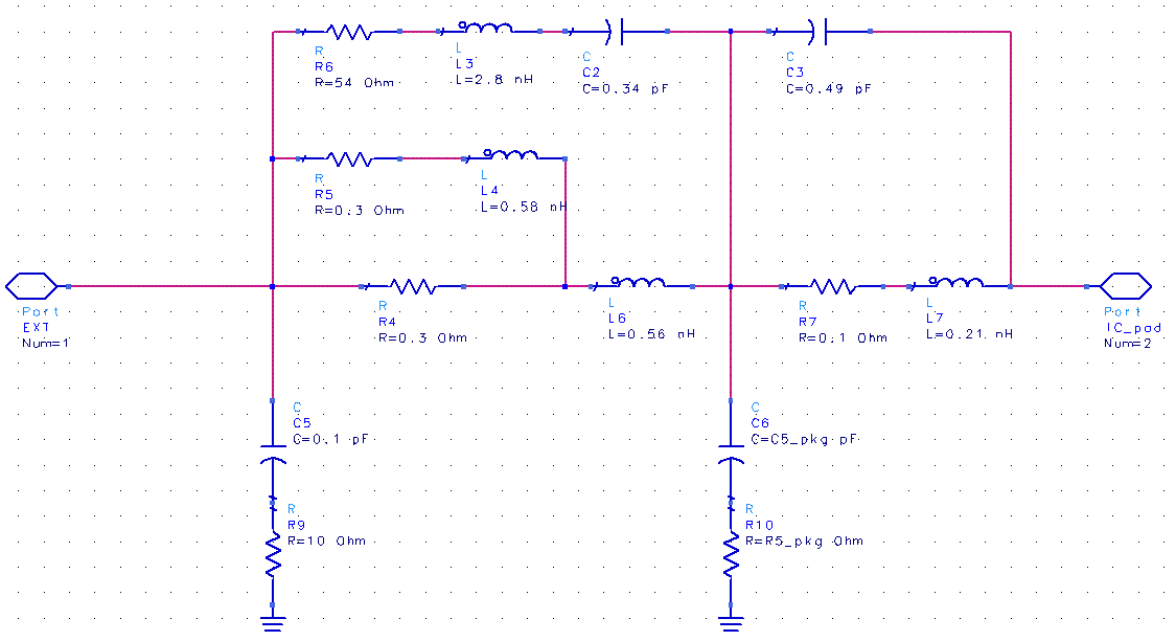
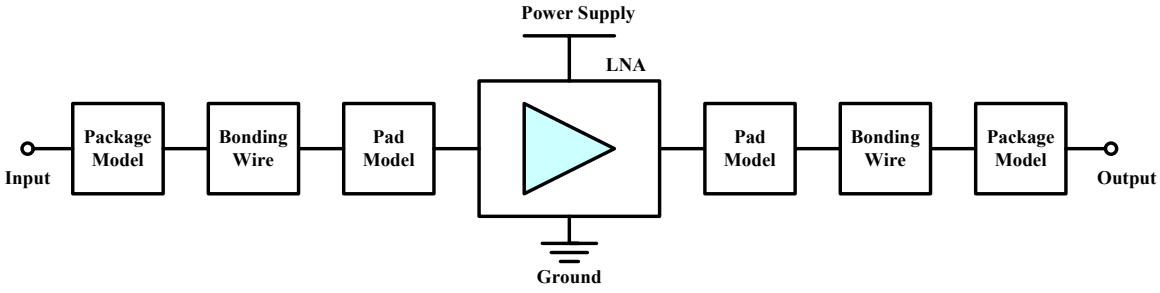
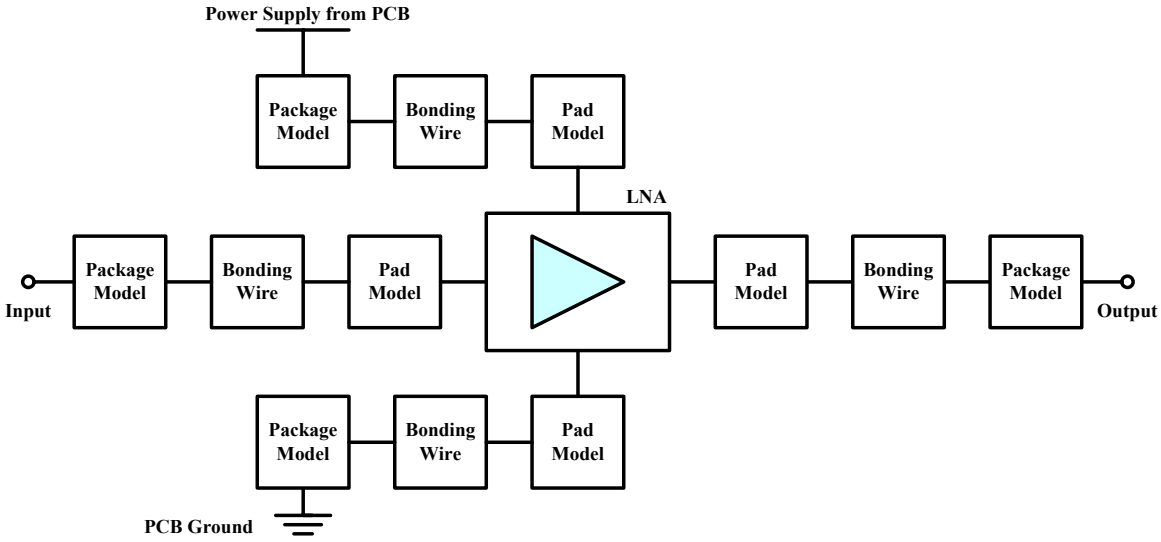


Figure 4.16 The estimated model of the package



(a)



(b)

Figure 4.17 The simulation of the LNA (a) without the the package/bonding network; (b) with the package/bonding network

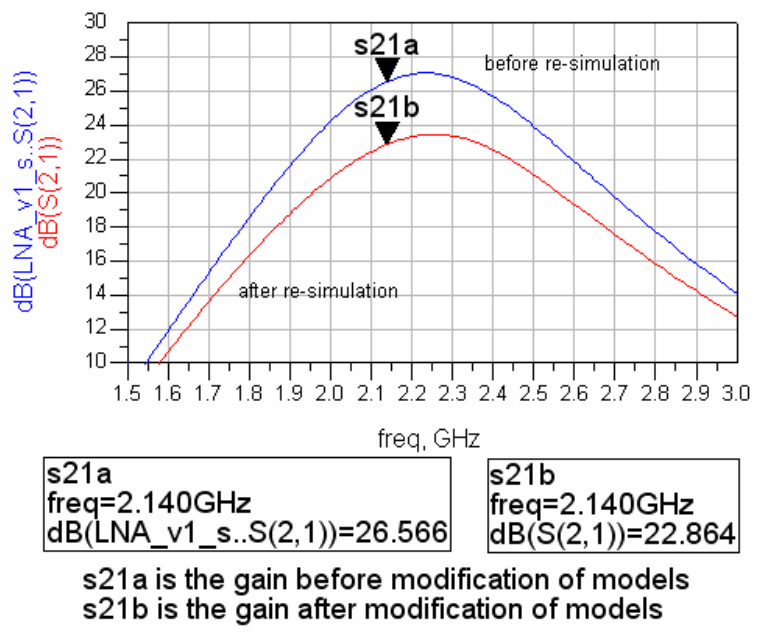


Figure 4.18 Reduction of the gain (LNA_v1) after adding the package/pad network to the power supply and ground

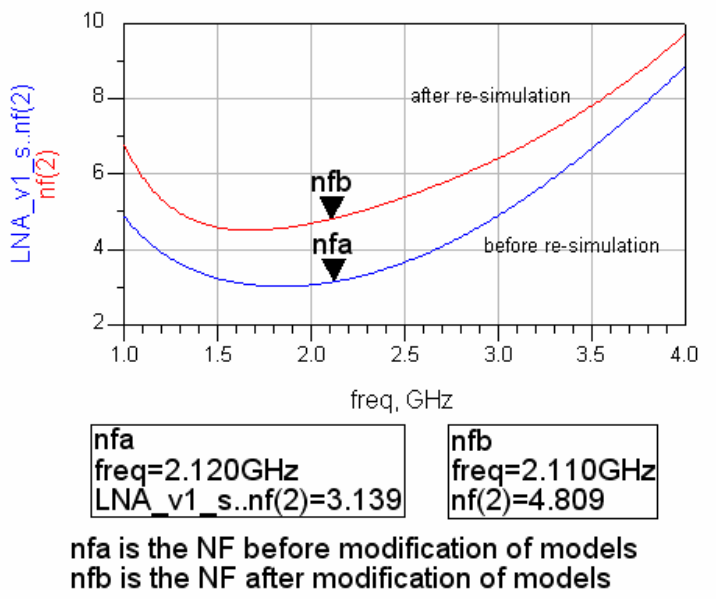


Figure 4.19 Degradation of the noise figure (LNA_v1) after adding the package/pad network to the power supply and ground

The degradation of NF is also partly due to an inaccuracy of the transistor model used in the design. The Equations (3.18) and Equation (3.19) are based on the effect of induced gate noise. However, this effect is not accounted for in the BSIM3.3 model and the in-house RF model, so the actual transistor noise may be higher in the measurement than in the simulation, furthermore the inaccurate transistor model may result in under-estimation of the required Q for the input of LNA. With limited Q-factors ($Q < 8$) for the on-chip matching inductors, the LNA is difficult to achieve NF below 2.5 dB. If the off-chip inductor (typical $Q > 15$) is used, the noise figure can be further improved and provide more design margin for the WCDMA receiver.

In terms of overall performance, LNA_v2 works better than the fully differential LNA_v1. The lower noise figure and higher power gain of LNA_v2 can be attributed to the single-ended amplifier used in the first stage before the differential conversion. However, the differential outputs suffered from small gain and phase imbalances, which may degrade the second-order intercept point for the receiver, therefore it was not chosen for the integrated RF front-end.

4.3.2 Down-conversion Mixer

The measurement results are shown in Figure 4.21 to Figure 4.27 and are summarized in Table 4.4 and Table 4.5. All the measurements have been performed with the RF input frequency of 2.141 GHz and LO frequency of 2.140 GHz, a non-zero intermediate frequency (f_{IF}) is observed at the mixer output. The 1 MHz f_{IF} is selected so that the strong DC interference from the equipment (e.g. spectrum analyzer) can be avoided. The optimum LO level of -5 dBm is found by sweeping the external signal source (Figure 4.21). Since the frequency divider is not included in this project, the LO power level and close proximity of f_{RF} and f_{LO}, have significant impact on the performance of DC offsets and the *IP2* of the mixer.

The most important design parameters for the mixer are conversion gain and linearity. The measured voltage conversion gains of MIX_v1 and MIX_v2 are 5.5 dB and -3 dB respectively. The 12 dB gain difference between the simulation and the measurement of MIX_v2 is quite unexpected, the data collected so far has pointed that the transconductance stage is the most likely root cause, the gain is much lower than the simulated 9.2 dB. Further investigation on the test chip found that the input of the common-gate stage has very poor S_{11} that is only -3 dB, hence much of the RF input signal has been reflected. The illustration of this problem is shown in Figure 4.20. The parasitic capacitances associated with the common-gate amplifier, the bonding pad, and the package are severely under-estimated as mentioned in the previous section. The

cancellation of this additional parasitic capacitance is possible if an off-chip shunt inductor is connected to the input of MIX_v2.

Table 4.4 Summary of direct conversion mixer measurements (MIX_v1)

Parameter	**Description**	**Simulation**	**Measurement**	**Unit**
f_{LO}	Oscillator frequency	2140	2140	*MHz*
P_{LO}	Oscillator power	-5	-5	*dBm*
G_c	Voltage conversion gain	6.3	5.5	*dB*
P_{1dB}	1-dB gain compression point	-17	-13	*dBm*
IIP3	3^{rd}-order intercept point	-7	3	*dBm*
IIP2	2^{nd}-order intercept point	+49.7	-	*dBm*
NF	DSB noise figure	8.4	-	*dB*
G_{LO-RF}	LO-RF isolation	>100	-46	*dB*
G_{RF-LO}	RF-RF isolation	-	-32	*dB*
I_d	Current consumption	3.04	4.8	*mA*

Table 4.5 Summary of direct conversion mixer measurements (MIX_v2)

Parameter	**Description**	**Simulation**	**Measurement**	**Unit**
f_{LO}	Oscillator frequency	2140	2140	*MHz*
P_{LO}	Oscillator power	-5	-5	*dBm*
G_c	Voltage conversion gain	9.2	-3	*dB*
P_{1dB}	1-dB gain compression point	-12	-8	*dBm*
IIP3	3^{rd}-order intercept point	-5	6	*dBm*
IIP2	2^{nd}-order intercept point	+50	-	*dBm*
NF	DSB noise figure	10	-	*dB*
G_{LO-RF}	LO-RF isolation	>100	-17	*dB*
G_{RF-LO}	RF-RF isolation		-25	*dB*
I_d	Current consumption	3.02	5.2	*mA*

For the noise figure of mixer, it have not been measured as a stand-alone circuit because the voltage conversion gain is low (< 6 dB) and it is difficult to measure the noise figure correctly by using the "Gain Method" [46].

For the reverse isolation of mixers, MIX_v1 shows better performance than MIX_v2 and this can be attributed to the two-stage design of MIX_v1. Since MIX_v2 is modified from the conventional Gilbert cell topology, the leakage from the LO-port to RF-port is difficult to be reduced due to the DC path sharing by the transconductance and switches. This problem is also exacerbated by the MOS transistors used for the mixer, a strong LO signal can leak to the RF-port through the silicon substrate. Such a leakage is difficult to simulate because the substrate coupling effect is not included in the current RF transistor model.

To summarize the mixers' performance, MIX_v1 has shown superior performance compared to MIX_v2. Not only on the conversion gain, it also achieves better linearity. However, the comparison may not be absolutely objective since the degradation of MIX_v2 performance is partly caused by the poor design of the input matching network.

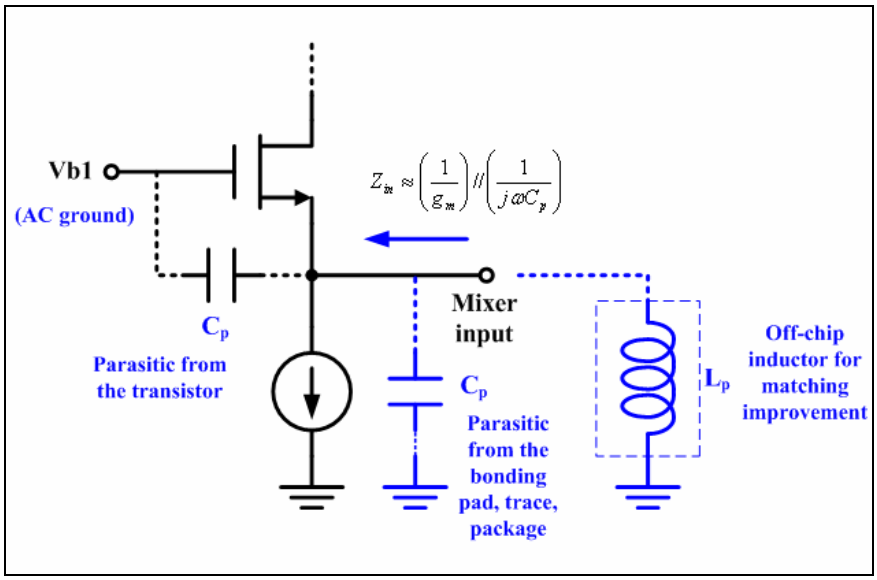


Figure 4.20 The parasitic capacitance associated with common-gate topology

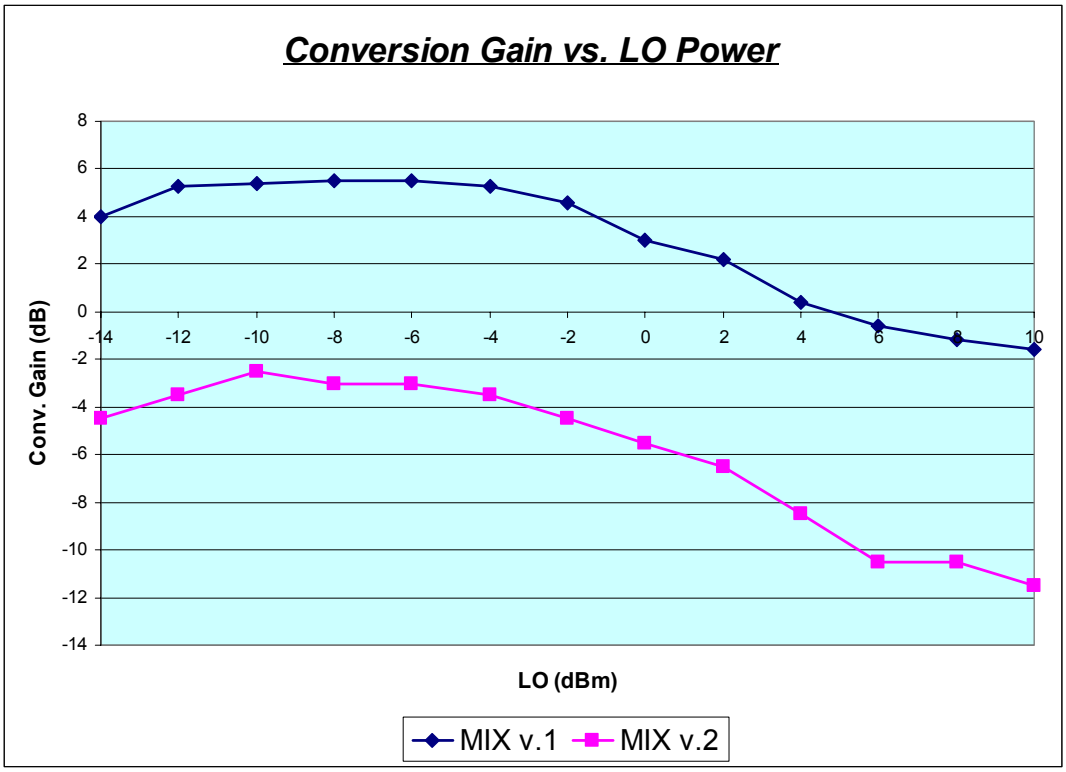


Figure 4.21 Mixer conversion gain vs. LO level

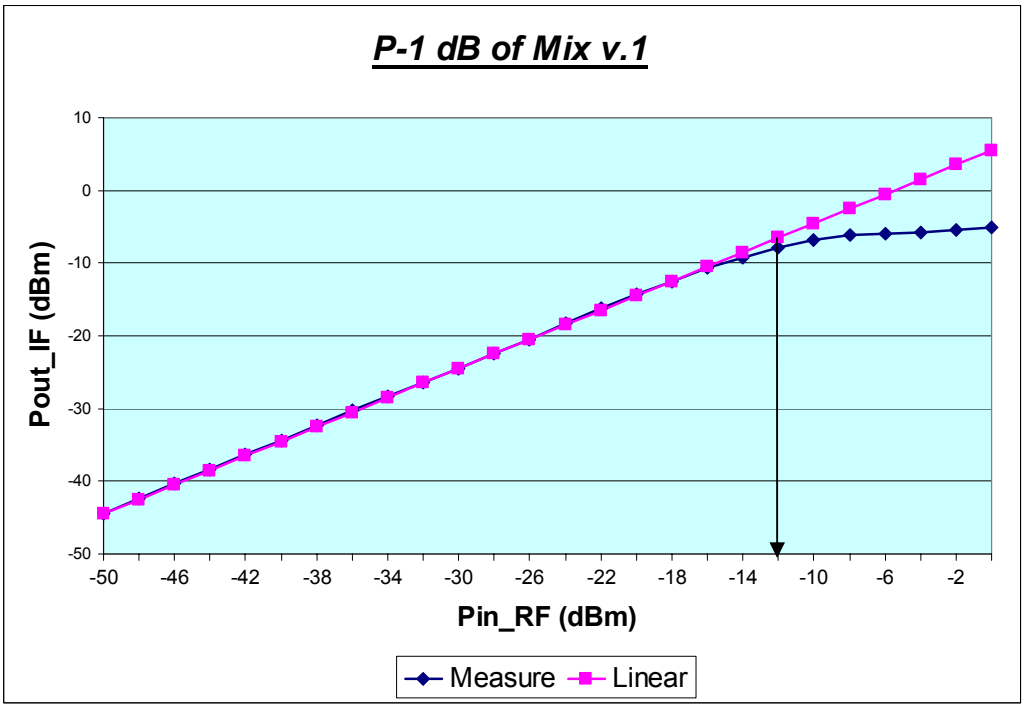


Figure 4.22 1-dB compression point of MIX v.1

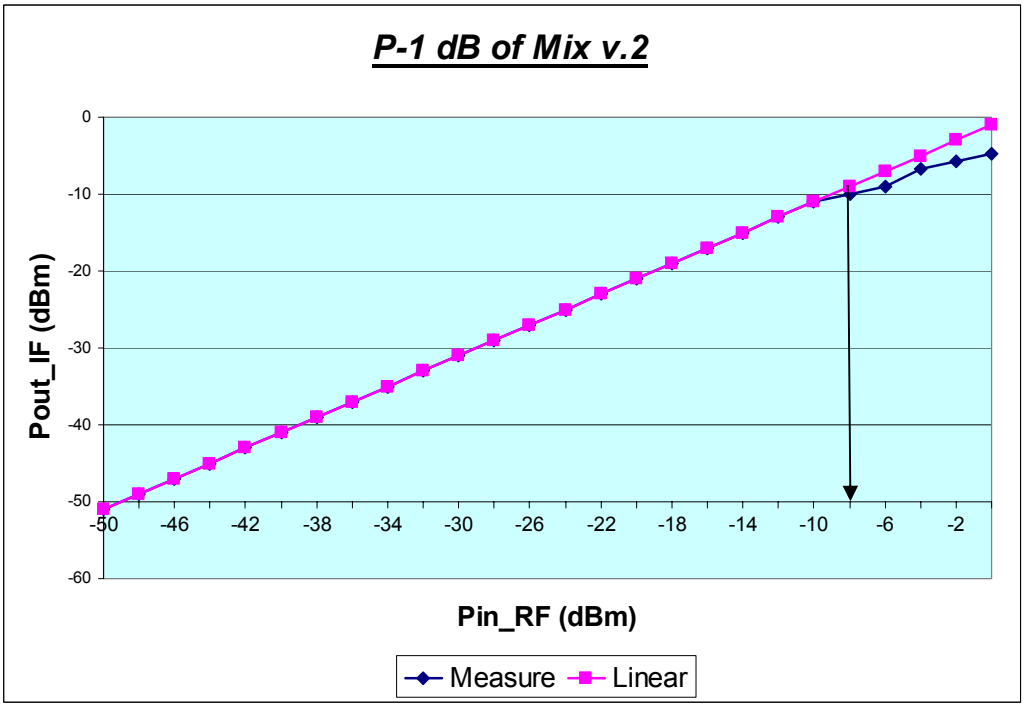


Figure 4.23 1-dB compression point of MIX v.2

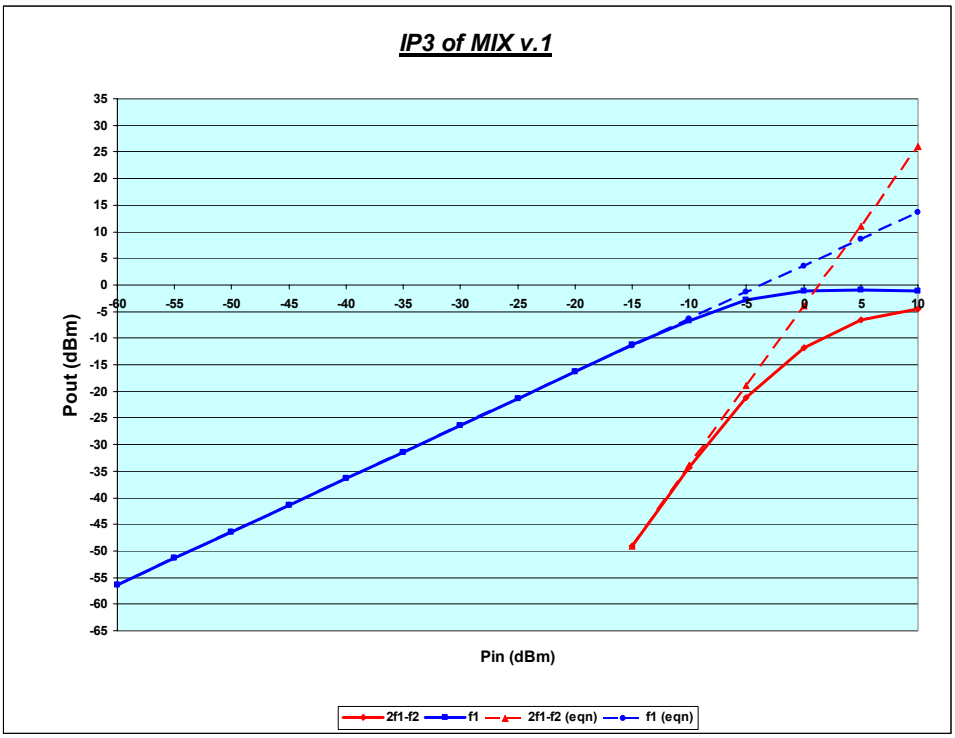


Figure 4.24 3rd-intercept point of MIX v.1

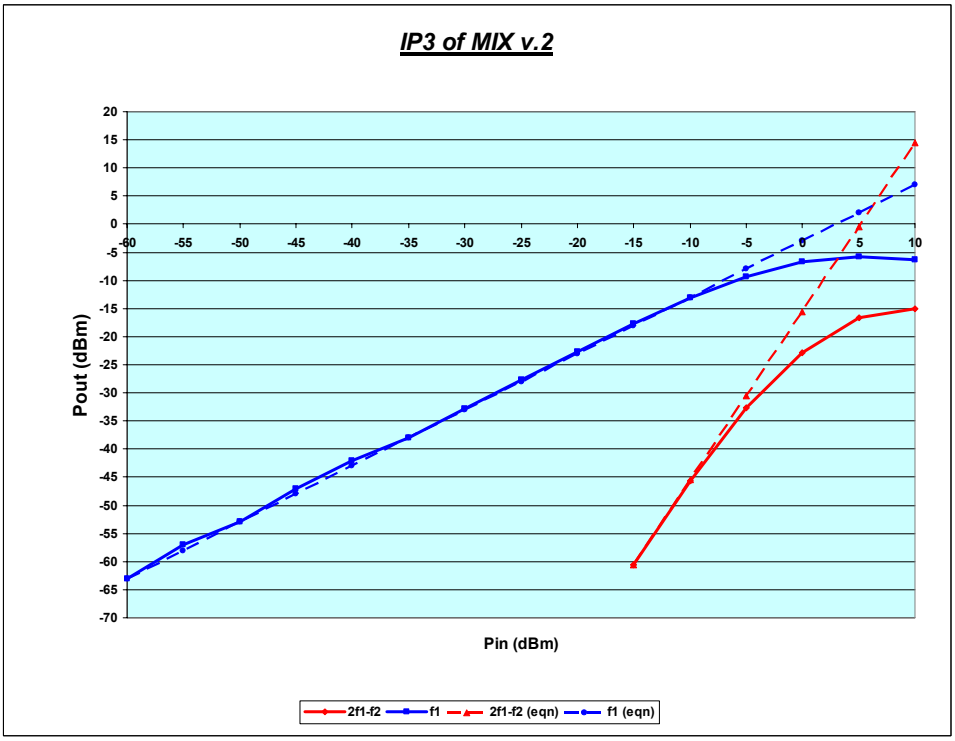


Figure 4.25 3rd-intercept point of MIX v.2

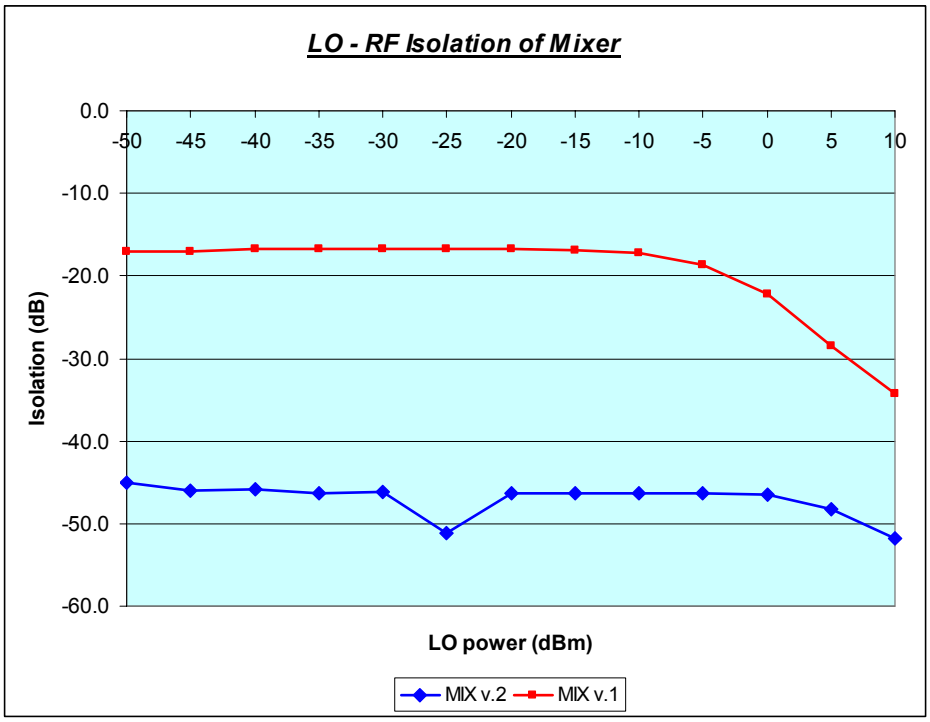


Figure 4.26 LO – RF isolation of mixer

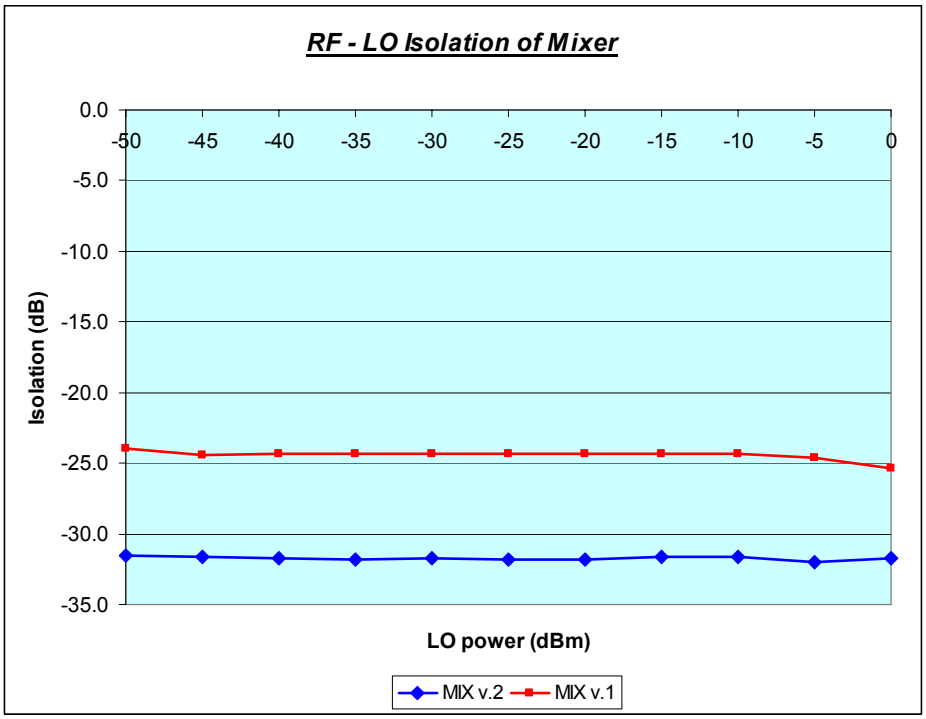


Figure 4.27 RF – LO isolation of mixer

4.4 Integrated RF Front-end Chip

For W-CDMA applications, *IIP2* is the most demanding technical challenge during the implementation of a direct conversion receiver, hence it is preferable to adopt a differential topology for the receiver chain. Based on the co-simulation of LNA and mixer for different designs, it has been found that the front-end design formed by the integration of LNA_v1 & MIX_v2 is the most suitable combination to realize the direct conversion receiver. The measured data of RFE_v2 are shown from Figure 4.28 to Figure 4.35 and the numerical results are summarized in Table 4.6. After comparing the measured data with the simulation, it has been found that the overall performance of RFE_v2 is greatly affected by the unexpected degradation of the gain control circuit and the parasitic capacitances which are not captured by the model and simulations.

Table 4.6 Summary of RF front-end measurements

Parameter	**Description**	**Simulation**		**Measurement**		**Unit**
		HG	LG	HG	LG	
f_c	Operating frequency	2140		2140		*MHz*
G	Voltage gain	34	18	22	-7.6	*dB*
NF	Noise figure (average)	3.3	4.7	9.5	-	*dB*
IIP2	2nd-order intercept point	54	75	23	-	*dBm*
IIP3	3rd-order intercept point	-29	-12	-24	9	*dBm*
P_{1dB}	1-dB gain compression point	-37	-21	-39	-3	*dBm*
$G_{LO\text{-}RF}$	LO-RF isolation	>90	>90	>80	>80	*dB*
I_d	Current consumption	15	11	17	12	*mA*

The voltage conversion gain and the integrated noise figure are 22 dB and 8 dB over 2 MHz of bandwidth respectively (Figure 4.28 and Figure 4.29). Since the gain is 12 dB below the simulation in high gain mode, the noise figure degrades quite significantly and 6.2 dB more than the simulation is observed. With such a high noise level from the transistors, the differential LNA (LNA_v1) is difficult to achieve the NF requirement of W-CDMA receiver with on-chip inductors. Although the performance can be improved by implementing high-*Q* off-chip inductors, it may not be an effective solution as the inherent noise from the LNA is too high. The most effective way of improving the noise figure and meeting the stringent requirements of W-CDMA application are to use the single-ended LNA design with an off-chip inductor connected to the input as shown in LNA_v2. It is because the total output noise of LNA is directly related to the number of transistors used in the design, a differential pair presents more noise sources than the single-ended design. Hence the differential LNA always shows inferior noise figure than the single-ended LNA under the same power consumption. Furthermore, the use of single-ended design can interface with the antenna easily and avoid the off-chip balun, which would further degrade the noise figure.

When operating in the strong input signal condition, the 1-dB compression point and *IIP3* of the RFE_v2 exceed the specification considerably. However, it should be reminded that the failure of the transmission gate for the gain control in the LNA could result in a high attenuation of the RF signal when it is diverted to the bypass route. To investigate the effectiveness of the differential topology and the proposed mixer design against the dc offset and second-order intermodulation, the second intercept point of the circuit is measured and shown in Figure 4.29. The *IIP2* happens when the input is +23 dBm.

Although this extrapolated data cannot meet the target of +30 dBm, one should keep in mind that these results are based on the close proximity of RF and LO frequencies (1 MHz deviation) and it is achieved without any calibration plan for *IP2* and DC-offset. On the other hand, most of the reported *IIP2* for the direct conversion receiver are achieved using divider (÷2) in between the LO and mixer. Since the LO frequency is twice the required frequency for mixing, the effects of leakage and self-mixing are substantially reduced. The direct measurement of the leakage for RFE_v2 is shown in Figure 4.35, the isolation between the LO – RF port is more than 80 dB. The isolation can be further improved if the advanced CMOS technology options, such as triple well NMOS (or deep N-well) are implemented [47]. The reduction of substrate coupling is very crucial to achieve a high performance direct conversion receiver and the forthcoming wireless silicon-on-chip (SOC). Further refinement in performance is possible if the MIX_v2 is replaced with the two-stage design (MIX_v1). The effect of LO direct feedthrough is more dominant in the MIX_v2 compared to MIX_v1.

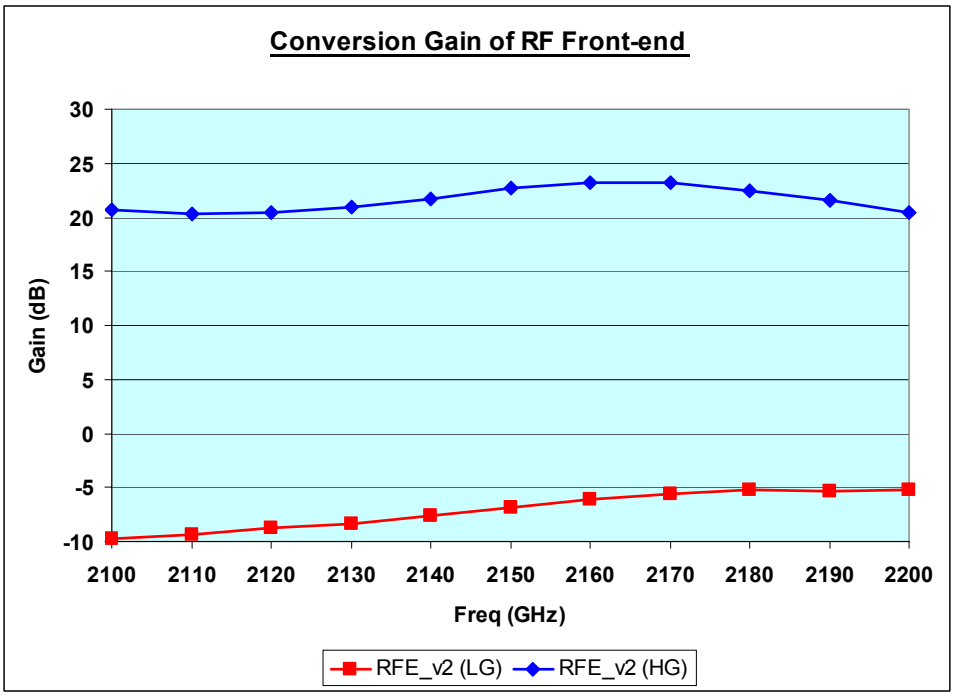


Figure 4.28 Voltage conversion gain of RF front-end at high/low gain mode

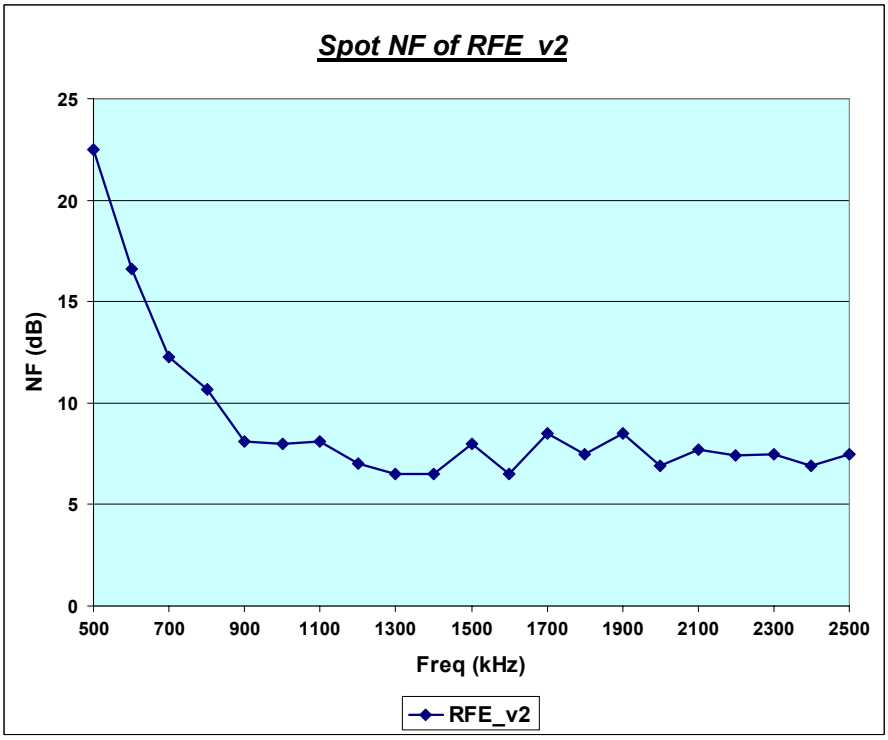


Figure 4.29 Spot noise figure of RF front-end at high gain mode

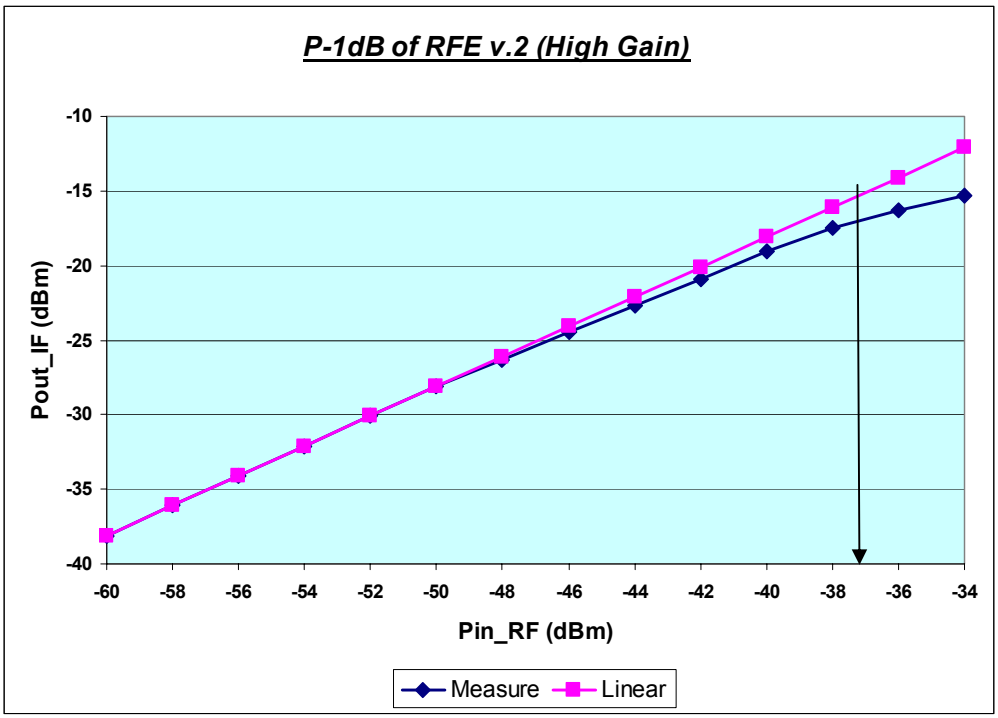


Figure 4.30 P-1dB of RF front-end at high gain

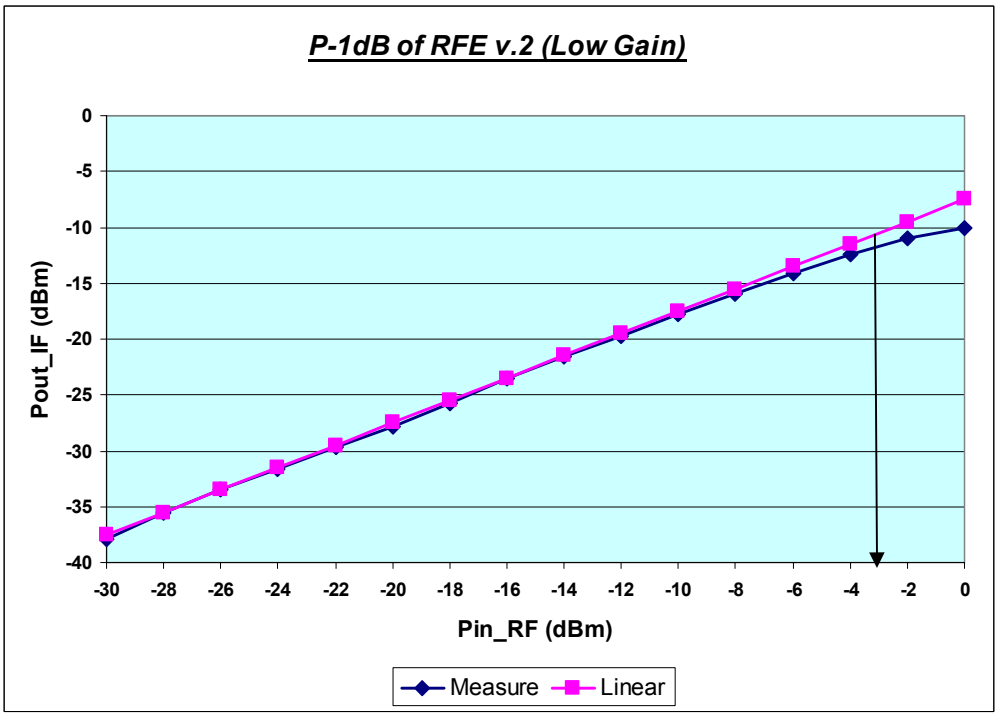


Figure 4.31 P-1dB of RF front-end at low gain

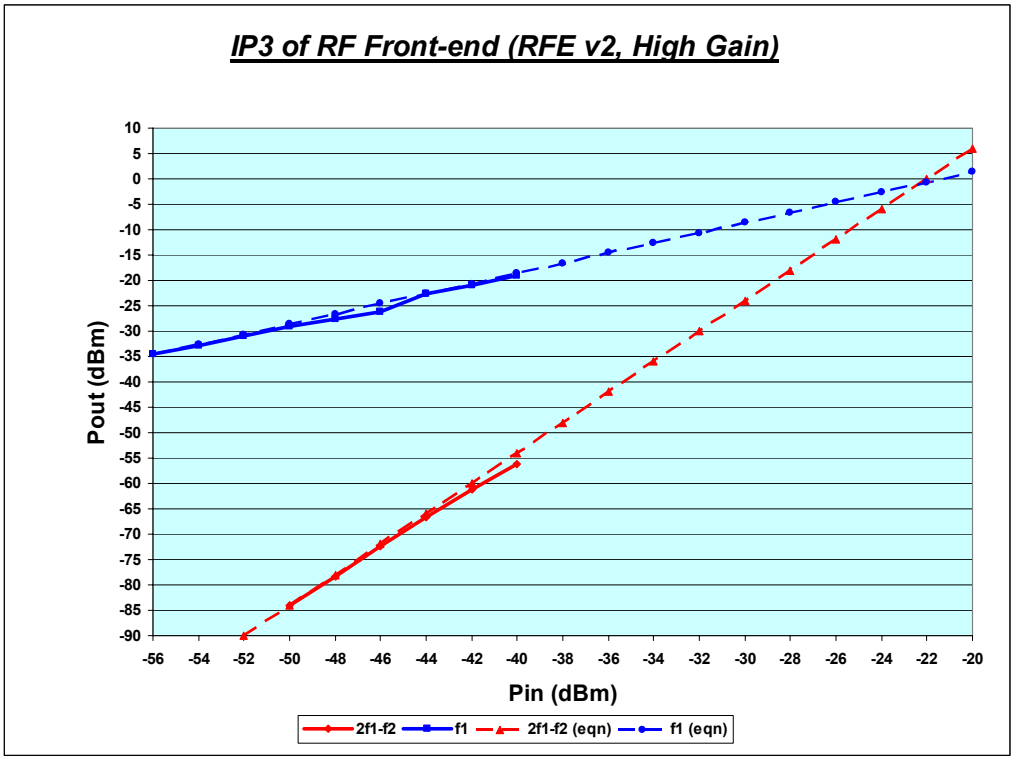


Figure 4.32 IIP3 of RF front-end at high gain

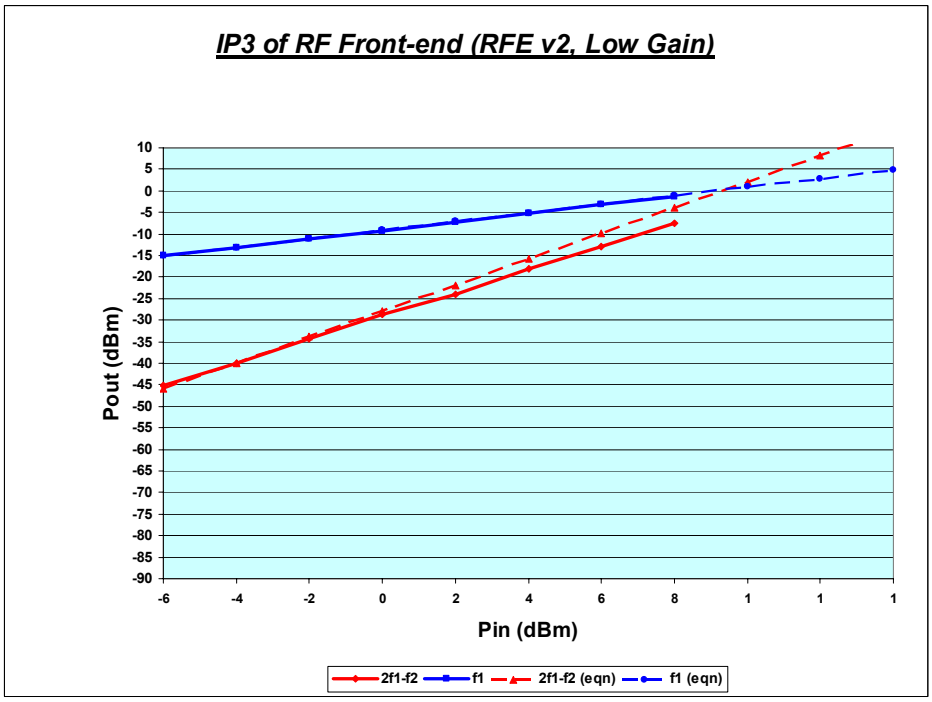


Figure 4.33 IIP3 of RF front-end at low gain

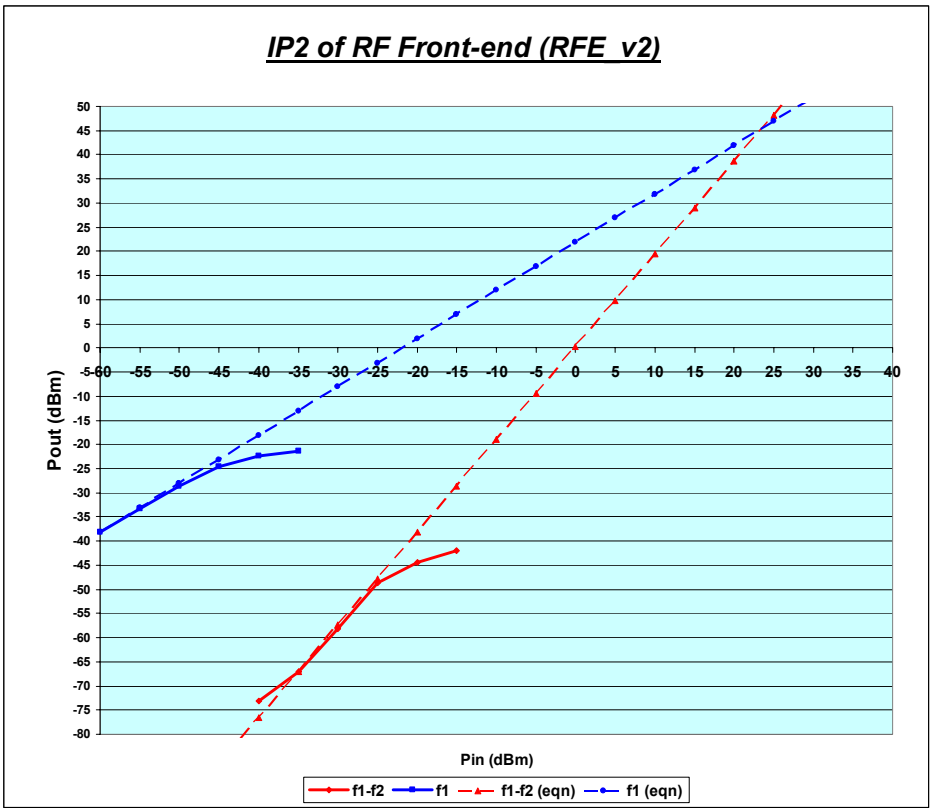


Figure 4.34 IIP2 of RF front-end at high gain

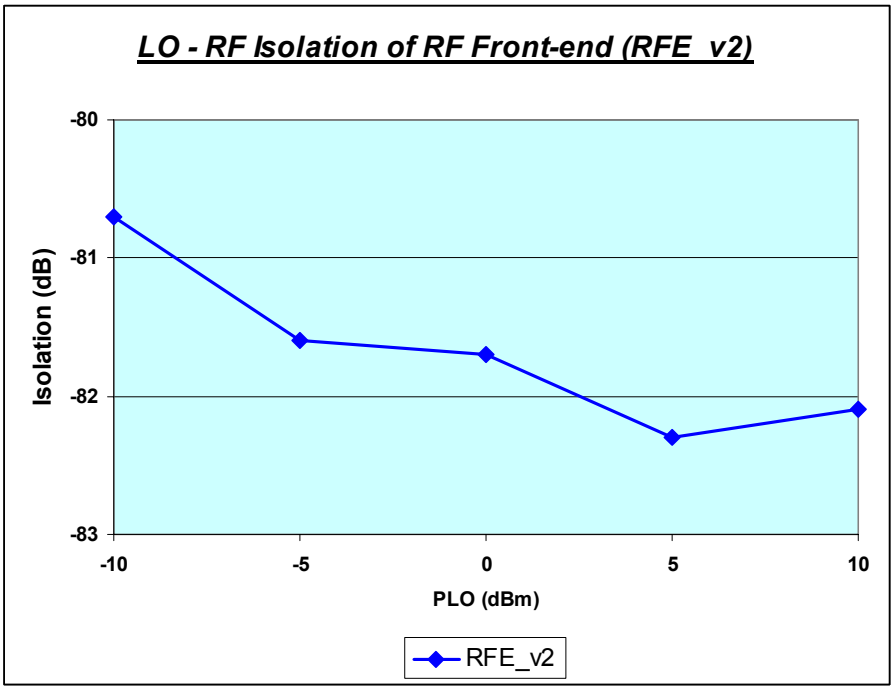


Figure 4.35 LO-RF isolation of RF front-end at high gain

4.5 Comparisons with published results

W-CDMA has very stringent requirements on the receiver, therefore most of the published results are built in SiGe BiCMOS technology [12] – [17], only two references are implemented in CMOS process [18], [19]. It is difficult to compare this work with those published result as most of the work are highly integrated receiver, which consists of RF front-end and baseband circuit. Table ?.? listed the front-end performance of the reported results from [12] and [18].

The measured results from the integrated front-end circuit in this thesis are inferior to those reported results, especially for the noise figure and *IIP3*. The performance of LNA and mixer need further optimization and they still have much room for improvement if the effect of parasitic are taken care in the design.

Table 4.7 Performance comparison with the published results.

Parameter	Description	This work	[12]	[18]	Unit
G	Voltage gain	22	25	-	*dB*
NF	Noise figure (average)	9.5	4.0	3.0	*dB*
IIP2	2nd-order intercept point	23	43	27	*dBm*
IIP3	3rd-order intercept point	-24	-9	-14	*dBm*
P_{1dB}	1-dB gain compression point	-39	-25	-27	*dBm*
I_d	Current consumption	17	-	17.5	*mA*
	Process technology	CMOS 0.35μm	BiCMOS 0.35 μm	CMOS 0.13μm	

Chapter 5 Conclusions

In this thesis, the issues related to direct conversion receiver architecture are addressed and analysed, particularly to the challenges of implementing the DCR for W-CDMA. Apart from the system analysis and receiver planning, the research also focuses on the front-end circuits such as the low noise amplifier and the mixer. Different circuit topologies are compared and investigated. Five test chips, which include two LNAs, two mixers and one version of the integrated front-end circuits, are implemented and measured.

It is found that the cascode structure with the inductive source degeneration is the most optimum circuit topology for the LNA. Although the single-ended amplifier approach can ease the interface issue with antenna and give better noise figure than the differential LNA, an active balun is required for the differential signal conversion. For the mixer design, improving the port-to-port isolation is the most essential requirement for achieving good DCR performance. The symmetrical circuit structure will also improve the IM2 performance and reduce the DC-offset. For increasing the isolation between LO – port and RF – port, the conventional Gilbert cell mixer is divided into the transconductance driver stage and the mixing stage, the direct feedthrough path is minimized. With this approach, better isolation is achieved. For the IM2 and flicker noise improvement, the frequency trap and current injection technique are adopted. The measured results for this approach deviate from the simulation considerably due to lower conversion gain from the mismatch at the input of the common-gate configuration as a *V-I* converter.

The measurement results of five test chips are reported. All the designs were functional though the measured results were not agreeing well with the simulation, especially the noise figure and the power gain, which were 9.5 dB and 22 dB respectively for the integrated version. The difference between simulation and measurement of the gain and the noise figure was due to the under-estimation of parasitic elements associated with transistors, bonding pads and package. The lack of higher Q on-chip inductors for the design also partly limited the LNA performance. For the linearity, the test chips exceeded system performance targets for *IIP3* and P-1dB at low gain mode. For the *IIP2*, the integrated chip misses the design goal by 7 dB. It only achieves +23 dBm when the same RF and LO frequency are injected to the test chip. The *IIP2* could be further improved if the divider circuit was used.

Although the measured results could not meet the design targets completely, it was still possible to employ standard CMOS process for the implementation of a W-CDMA receiver front-end [18], [19]. As the technologies progress, the noise figure can be further improved if the advanced CMOS technology such as 0.13μm and below are used in the designs. The only bottleneck may come from the monolithic passive components, which are degraded by the lossy silicon substrate. However, it is believed that with the improved CMOS technologies along with the calibration circuits and digital signal processing techniques, all these limitations can be overcame in the course of realization of single-chip transceiver.

Chapter 6 Recommendations

After the measurements, it was found that some of the discrepancies and performance degradations could be further improved if the following schemes were implemented:

(I) Proper Design Flow

Under the available CAD environment, it is highly possible that the simulation just based on the RF models alone may under-estimate the effect of parasitic networks considerably and result in large deviation between the simulation and measurement. Since the post-simulation is very essential step in predicting the circuit performance in *GHz* range, it is recommended that the design, simulation and extraction were done on the same CAD platform, e.g. Spectre-RF simulator and ASSURA extraction tool.

(II) Divider Circuit

Since there was no divider circuit between the local oscillator and mixer, the RF frequency and LO frequency was the same, hence the effect of self-mixing was more evident because of the strong leakage signal from LO-port to RF-port. In most of the reported results, good dc-offset, IIP2 and LO – RF isolations were achieved through the implementation of divider circuit along the LO path. With the ÷2 or ÷4 circuit, LO frequency can be twice or four times of RF frequency, this can reduce the undesirable effect of self-mixing.

(III) Differential Inductor

In this project, two inductors were used for the input matching of the differential amplifier and another two were used as output loading. Using two separated inductors for the differential path may not be area efficient. It also offered a lower Q than a differential type inductor. It was found that no differential inductor was available in the passive components library provided by IME in-house model. It is recommended to incorporate these inductors into the future design for differential circuit so that the circuit's performance can be further improved and a more symmetrical layout can be achieved.

(IV) Advanced CMOS Process

One of the limiting factors for RF front-end circuits came from the 0.35μm CMOS transistors. The inherent noise associated with the transistor is higher and this may not meet the stringent requirement for the W-CDMA application. For the more advanced CMOS technology, the NF_{min} can be much lower with the same biasing current, hence it is recommended to use a CMOS transistor, which have the feature length of 0.18μm and below for the applications demanding stringent noise figure.

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Appendix A Simulation Results

This appendix presents the supplementary results from the simulation of low noise amplifier, down-converted mixer and the integrated front-end design.

A.1 Low Noise Amplifiers

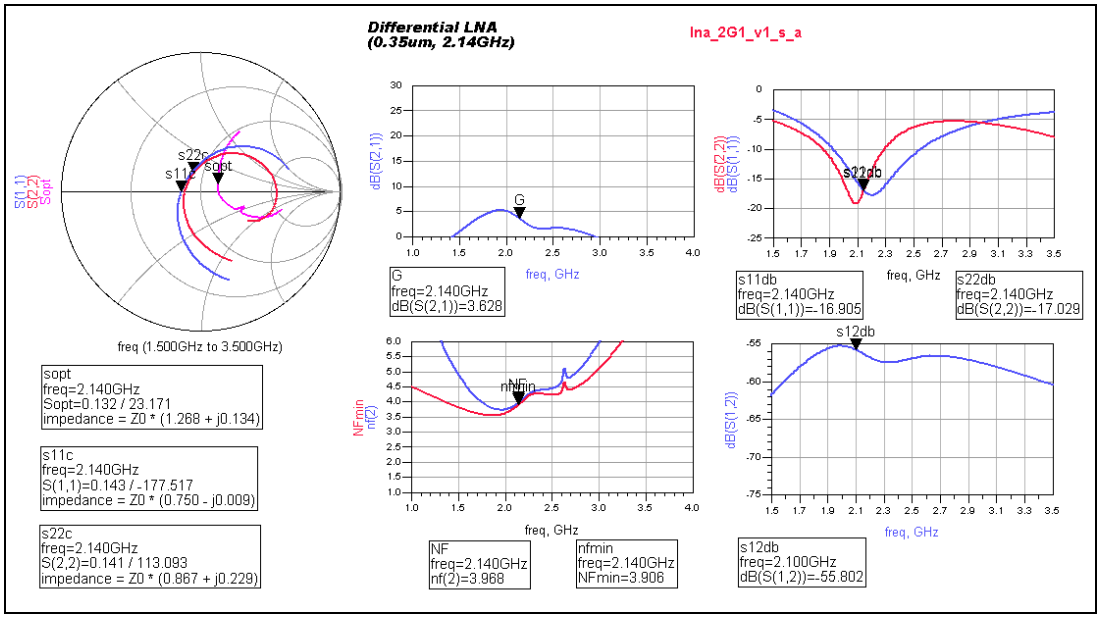

Figure A.1 S-parameters and noise figure of LNA_v1 (low gain mode)

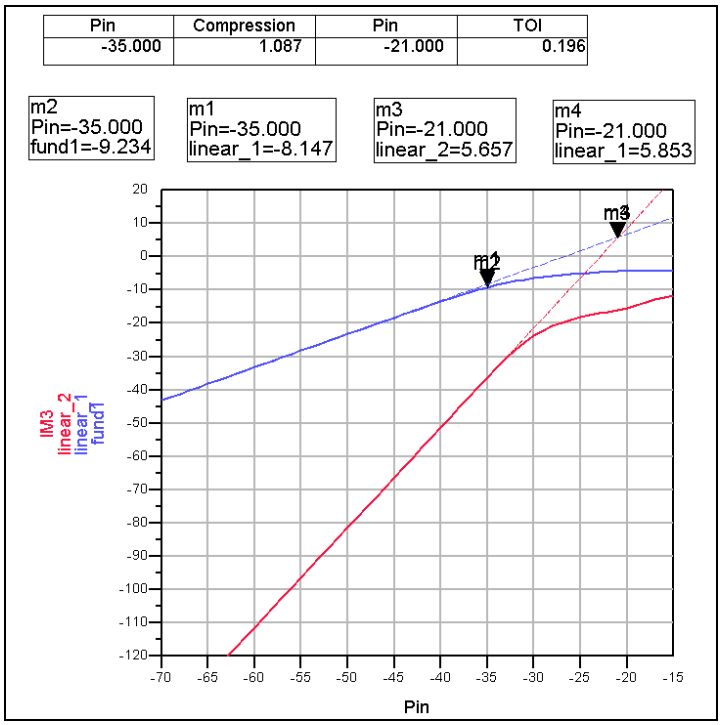

Figure A.2 IIP3 of LNA_v1 (high gain mode)

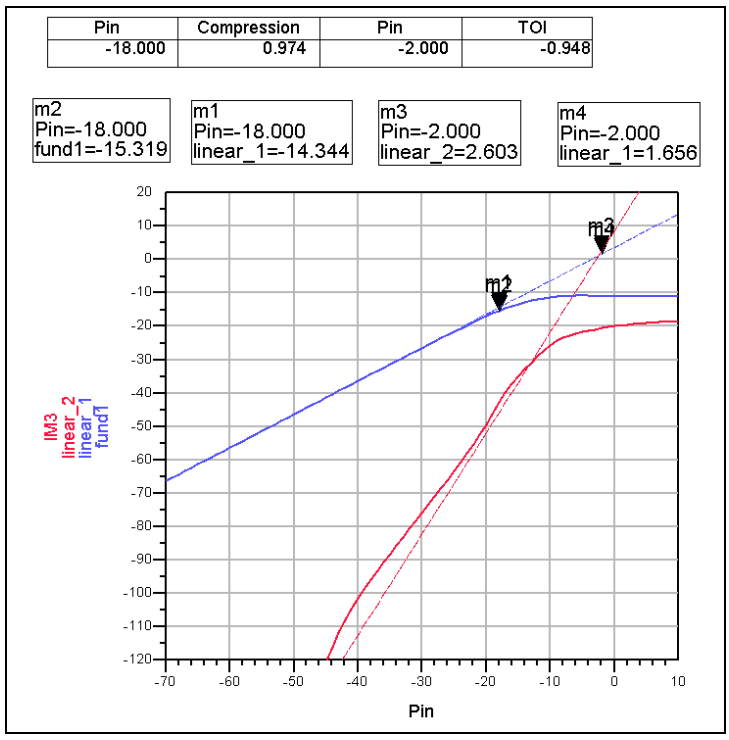

Figure A.3 IIP3 of LNA_v1 (low gain mode)

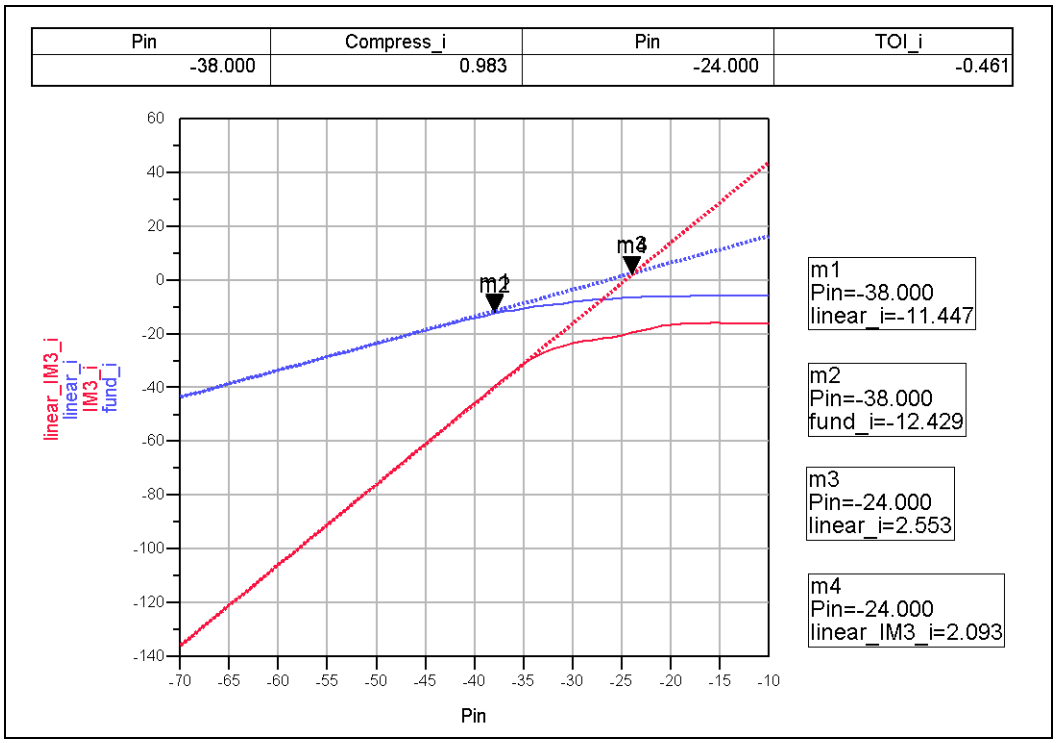

Figure A.4 IIP3 of LNA_v2 (high gain mode)

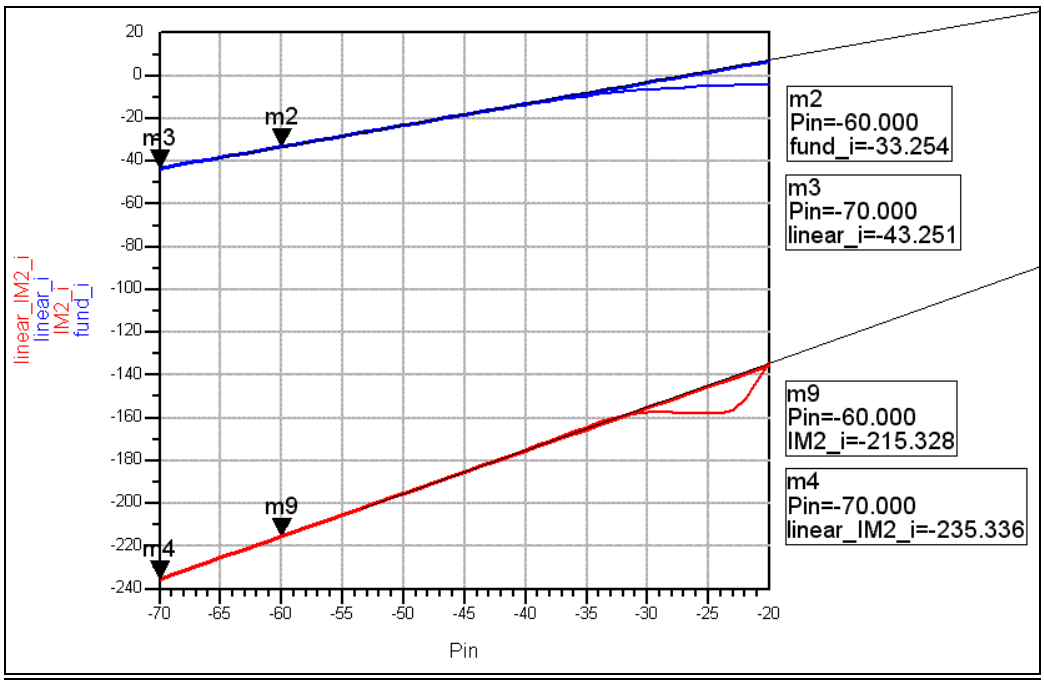

Figure A.5 IIP2 of LNA_v1 (high gain mode)

For LNA_v1, the extrapolated lines to represent the linear output and IM2 product can be represented by the following equations:

Linear output : $y = x + 26.7$ (A.1)

IM2 product: $y = 2x - 95.3$ (A.2)

By solving Equation (A.1) and Equation (A.2), x = 122 and y = 148.7. The figures mean that the IIP2 and OIP2 are 122 dBm and 148.7 dBm respectively

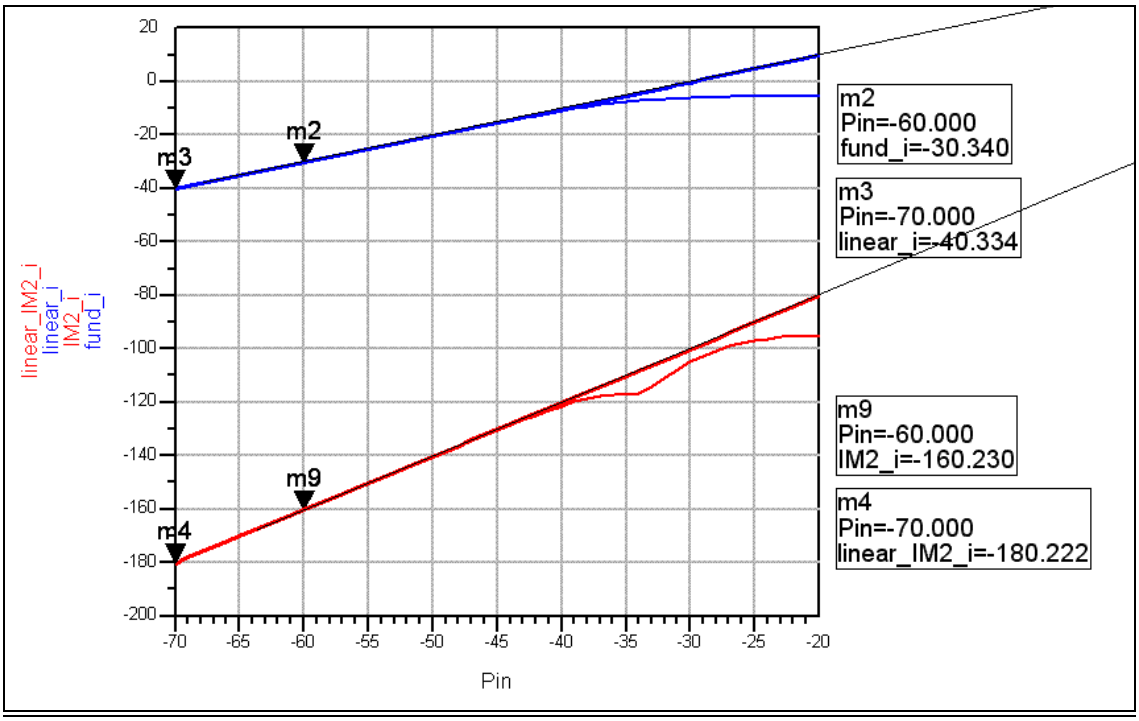

Figure A.6 IIP2 of LNA_v1 (high gain mode)

For LNA_v2, the extrapolated lines to represent the linear output and IM2 product can be represented by the following equations:

Linear output : $y = x + 29.7$ (A.3)

IM2 product: $y = 2x - 40.2$ (A.4)

By solving Equation (A.3) and Equation (A.4), x = 69.9 and y = 99.6. The figures mean that the IIP2 and OIP2 are 69.9 dBm and 99.6 dBm respectively

A.2 Down-convert Mixers

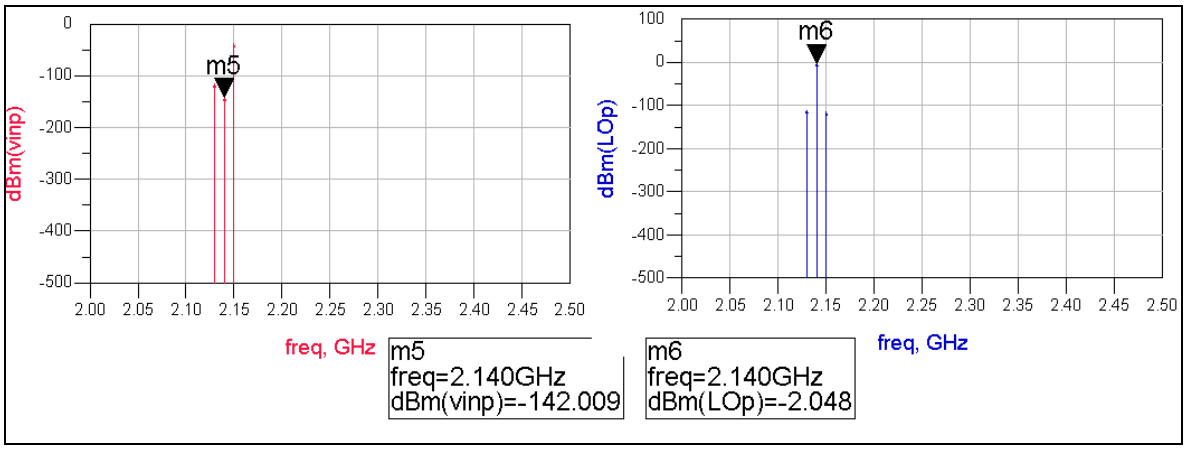

Figure A.7 LO – RF isolation of MIX_v1

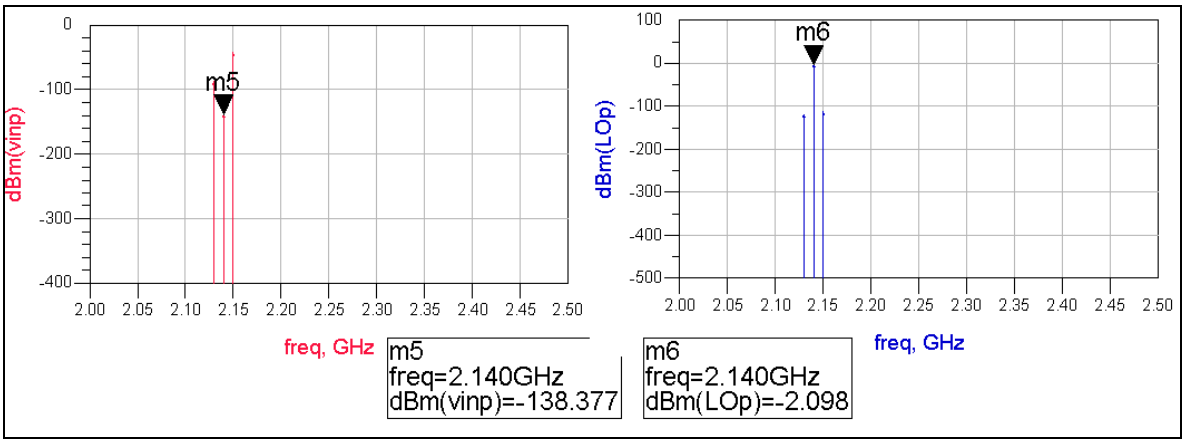

Figure A.8 LO – RF isolation of MIX_v2

A.3 RF Front-end Circuit

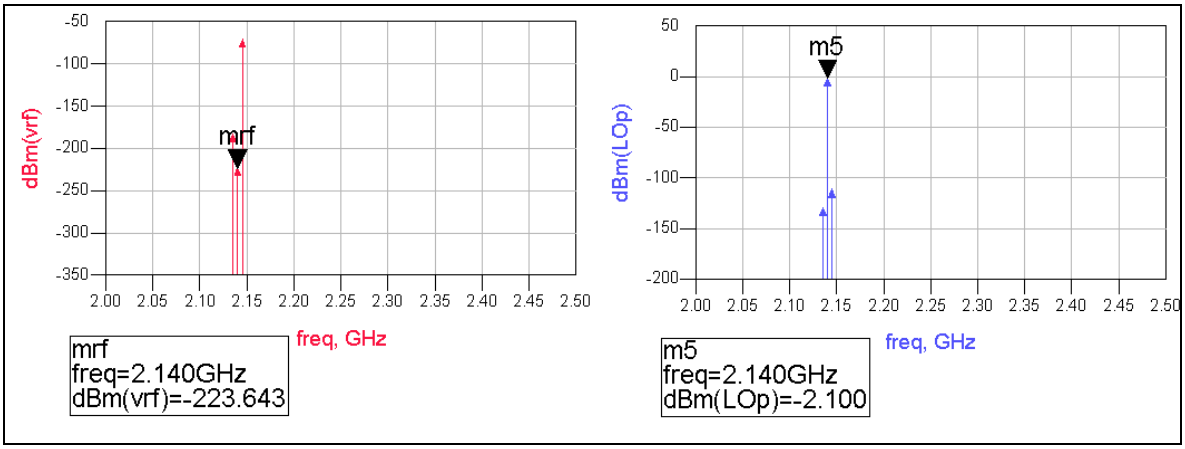

Figure A.9 LO – RF isolation of RFE_v2 (high gain mode)

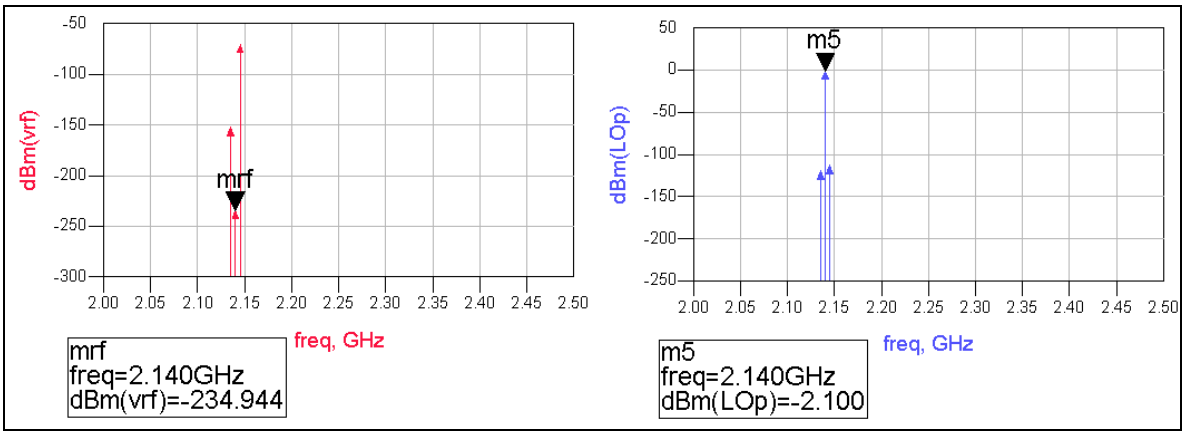

Figure A.10 LO – RF isolation of RFE_v2 (low gain mode)

Appendix B Chip Layout Diagrams

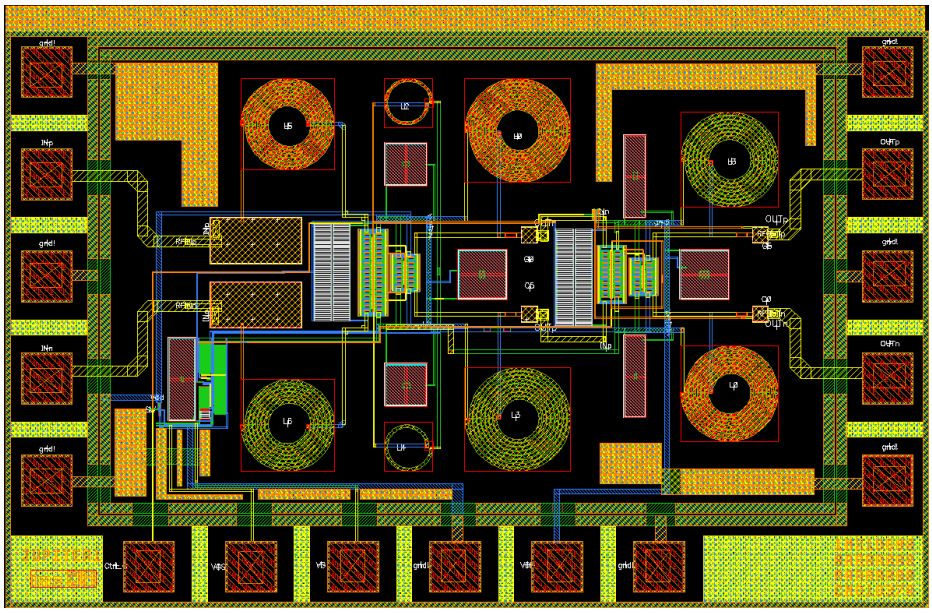

Figure B.1 The layout of LNA_v1

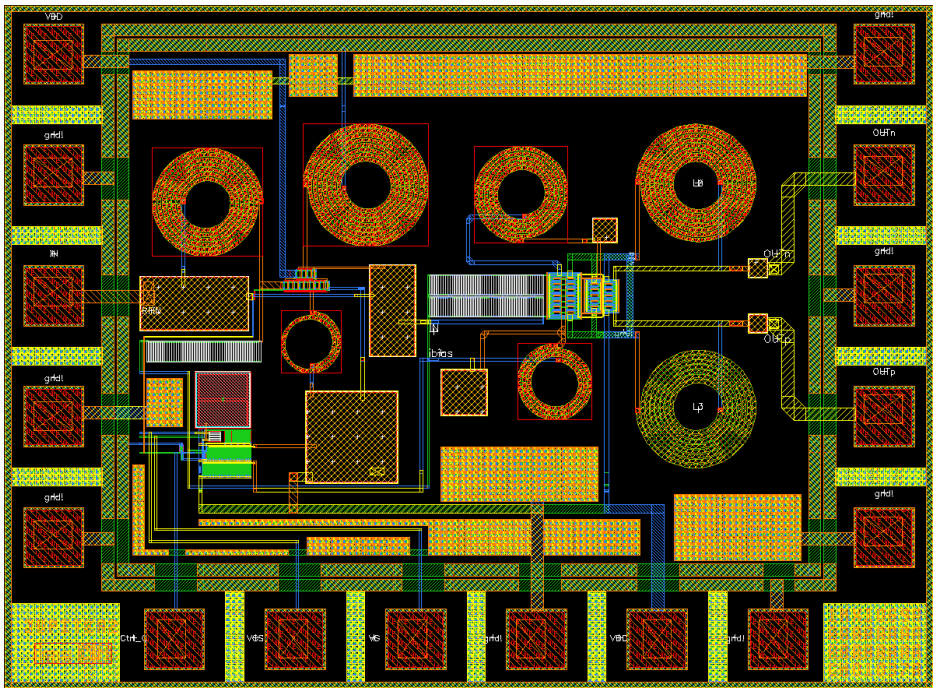

Figure B.2 The layout of LNA_v2

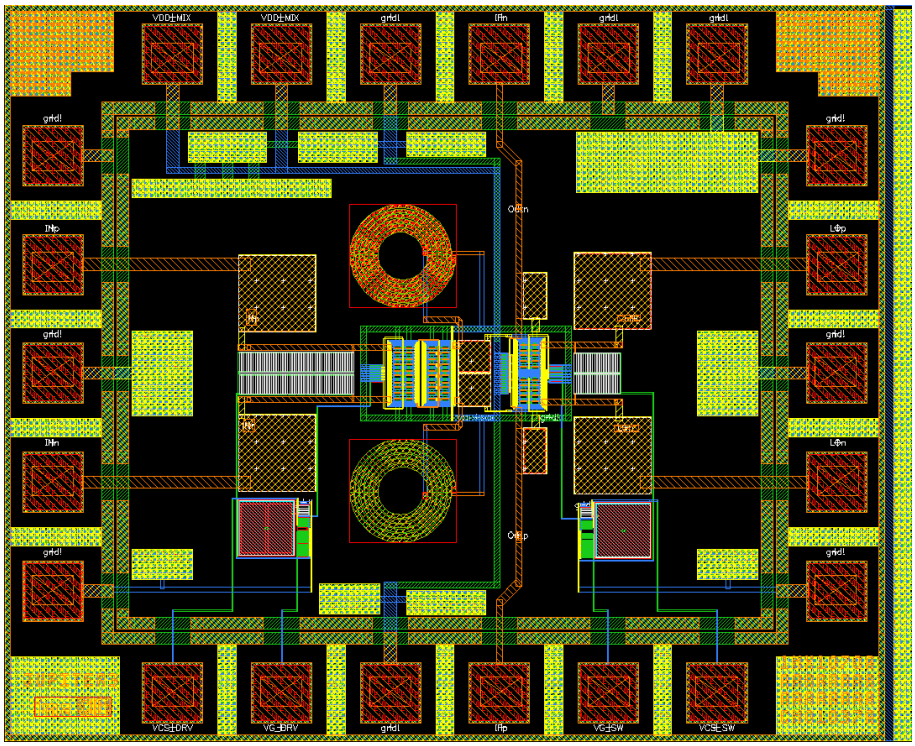

Figure B.3 The layout of MIX_v2

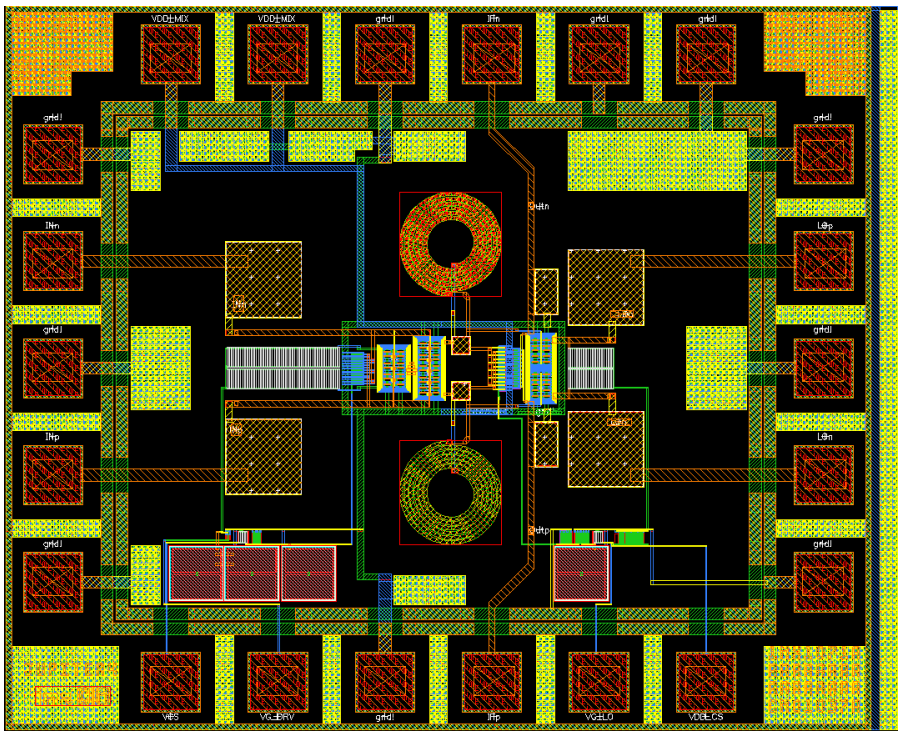

Figure B.4 The layout of MIX_v2

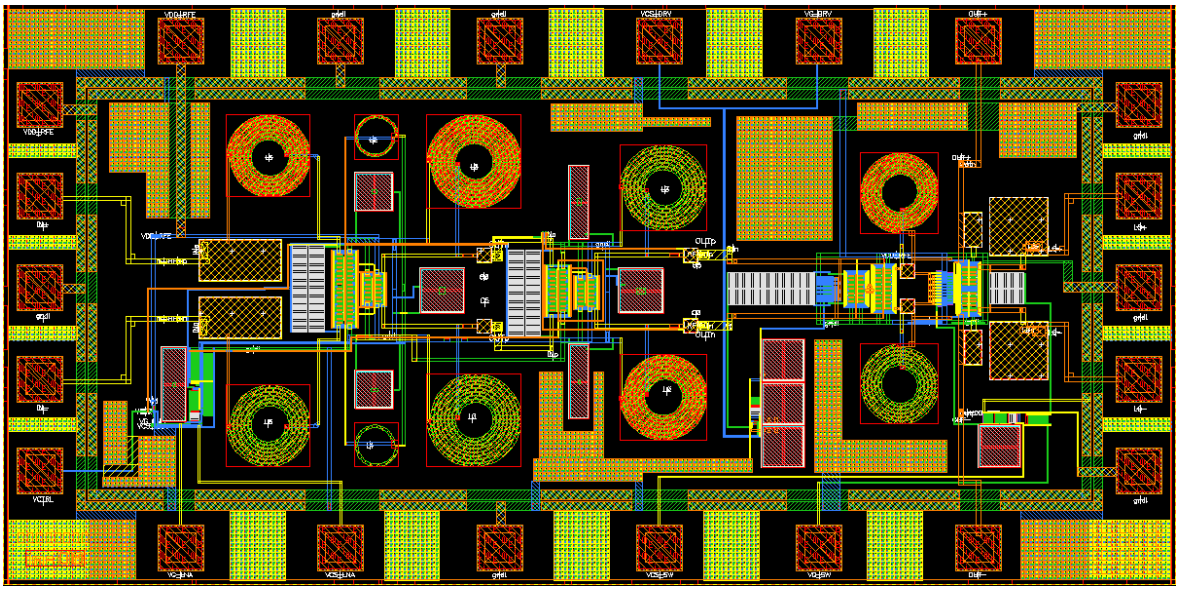

Figure B.5 The layout of RFE_v2

Appendix C PCBs for Test Chip Measurements

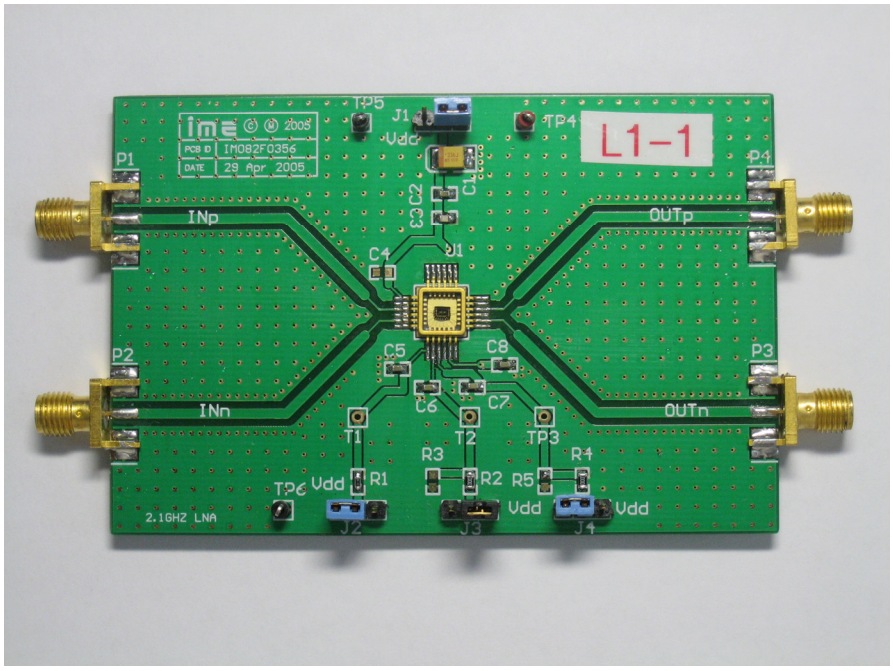

Figure C.1 The PCB used in the LNA_v1 measurement

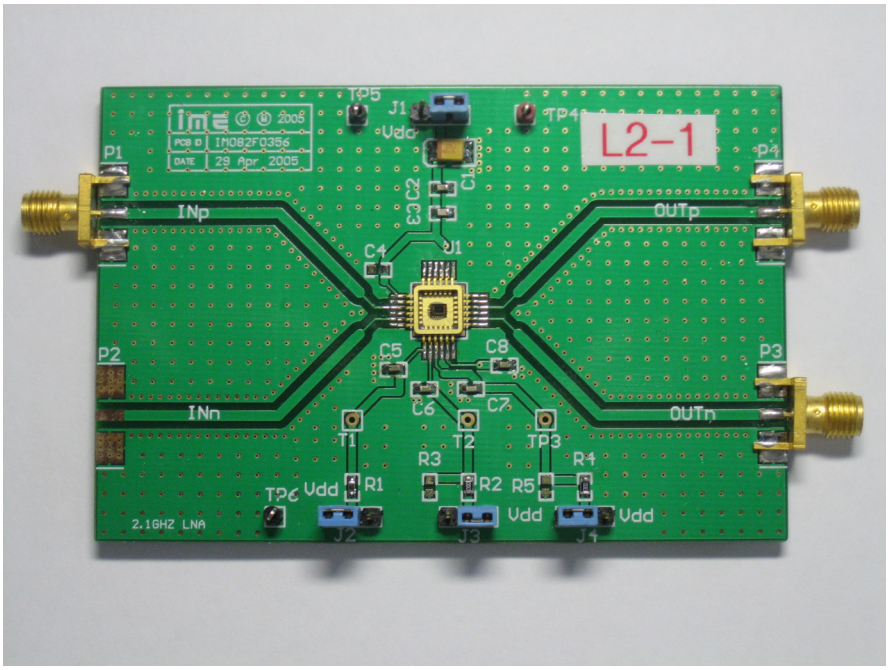

Figure C.2 The PCB used in the LNA_v2 measurement

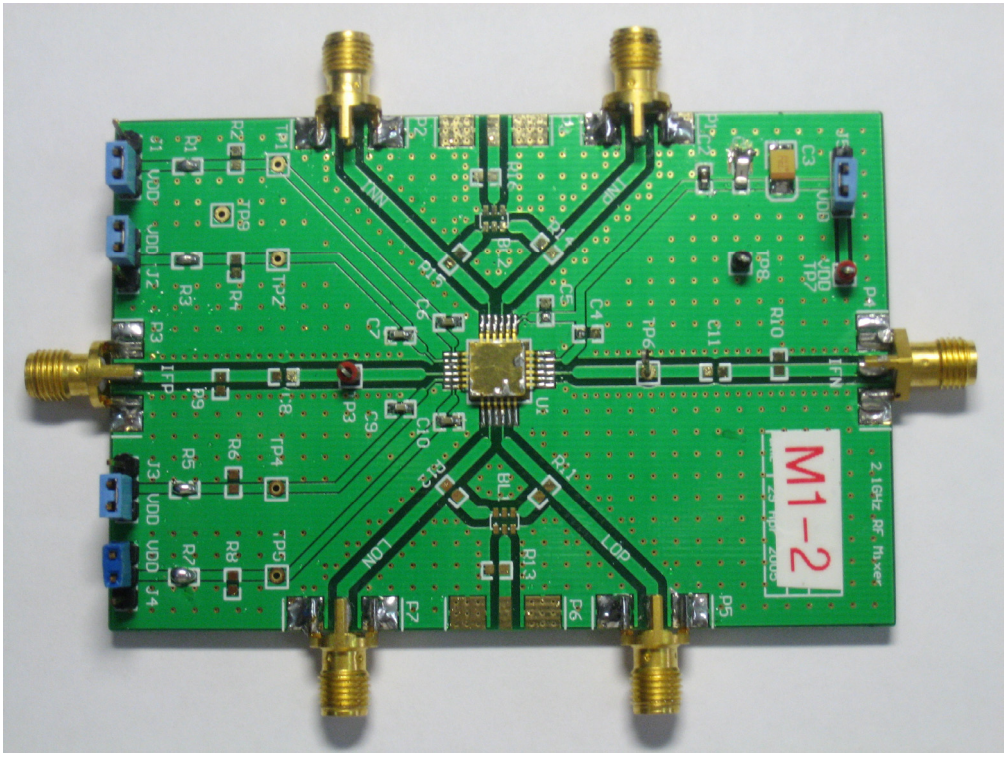

Figure C.3 The PCB used in the MIX_v1, MIX_v2, and RFE_v2 measurement

Appendix D Test Setup for Measurements

D.1 Low Noise Amplifier

The LNA measurements were quite straightforward. Since no frequency translation was involved, the gain and noise figure could be measured directly from noise figure analyzer and network analyzer as shown in Figure D.1 (a) and (b).

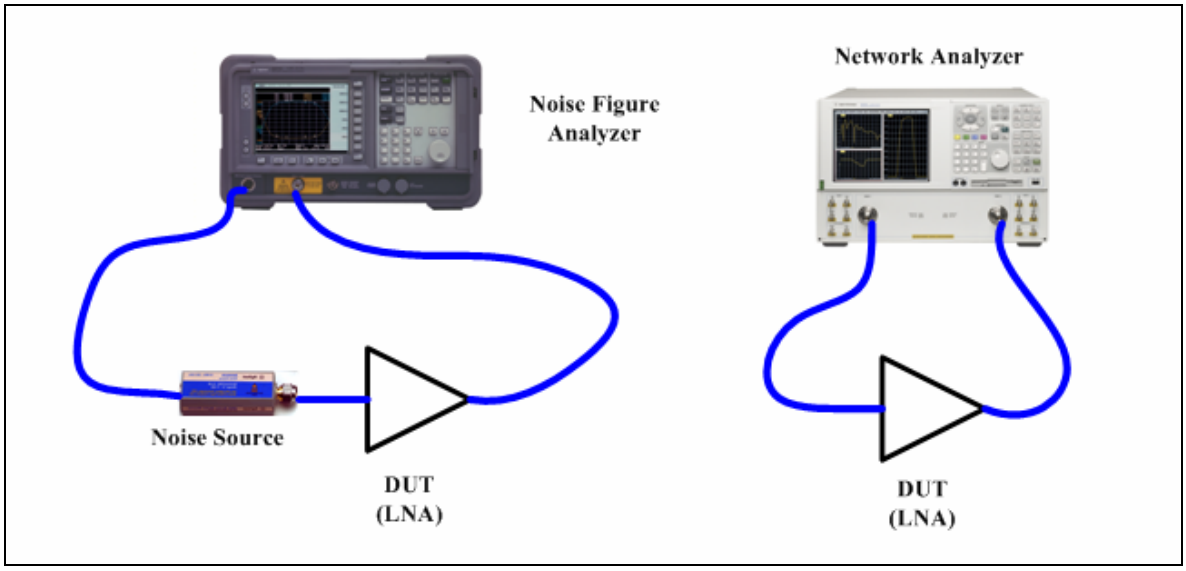

Figure D.1 Test setup for the measurement of (a) noise figure and (b) S-parameter of LNA

D.2 Mixer and RF Front-end Circuit

The measurement process of mixer and the integrated RF front-end were quite complicated. Since the frequency translation was involved, some precautions were taken during the characterizations of device under test (DUT). Furthermore, the output of direct down-converted mixer would center at 0 Hz, which would interfered with dc voltage of the equipment. The better option is to incorporate the off-chip buffer IC between the DUT and equipments for isolation and 50Ω driving purposes. However, this problem was not well taken care and considered during the PCB design phase. Hence, Differential probes and high frequency probe were used to avoid the direct coupling of the DUT to the equipment.

Another challenge faced during the measurements came from the noise figure characterization. The IF after down-conversion was located near 0 Hz, so the direct measurement from noise figure analyzer became inapplicable. The lowest frequency could be generated by noise source was 10 MHz, which was well above the bandwidth of WCDMA signal. To measure the noise figure of mixer or RF front-end circuits indirectly, gain method was used [3]. The problem associated with the gain method was the total gain of DUT needed to be high. As a result, the measurement of low gain mixer was quite inconsistent. To obtain the reliable measurement data, only front-end circuits were measured.

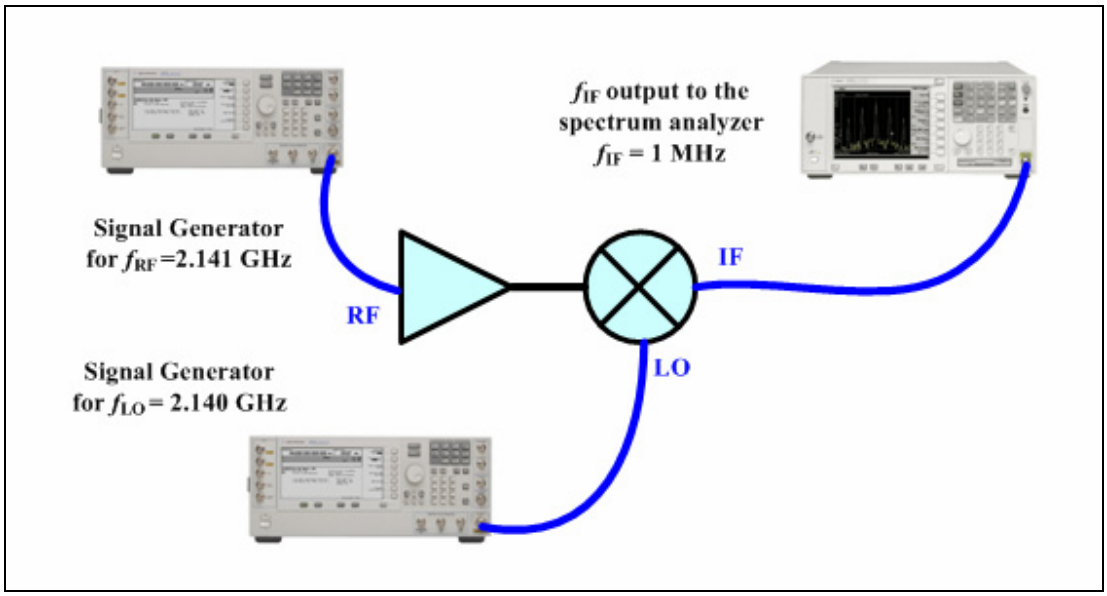

Figure D.2 Test setup for the measurement of front-end conversion gain, noise figure and 1-dB compression point.

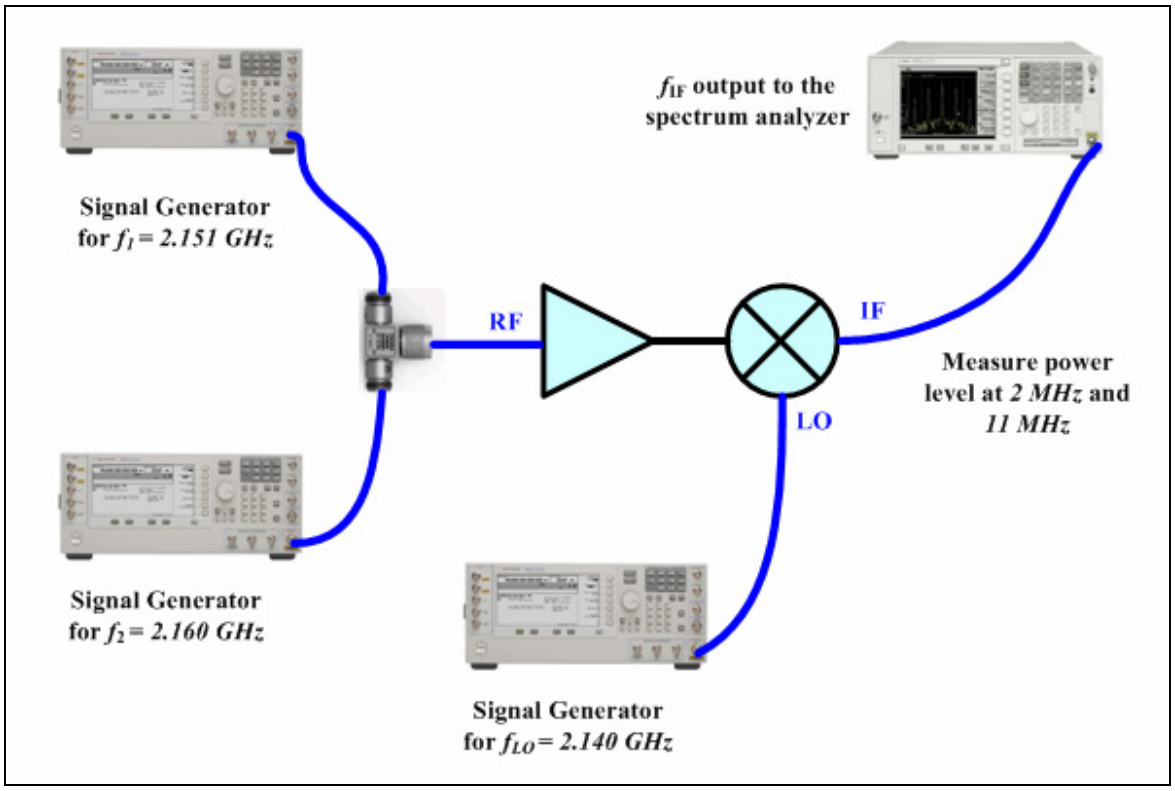

Figure D.3 Test setup for the IP3 measurement of front-end

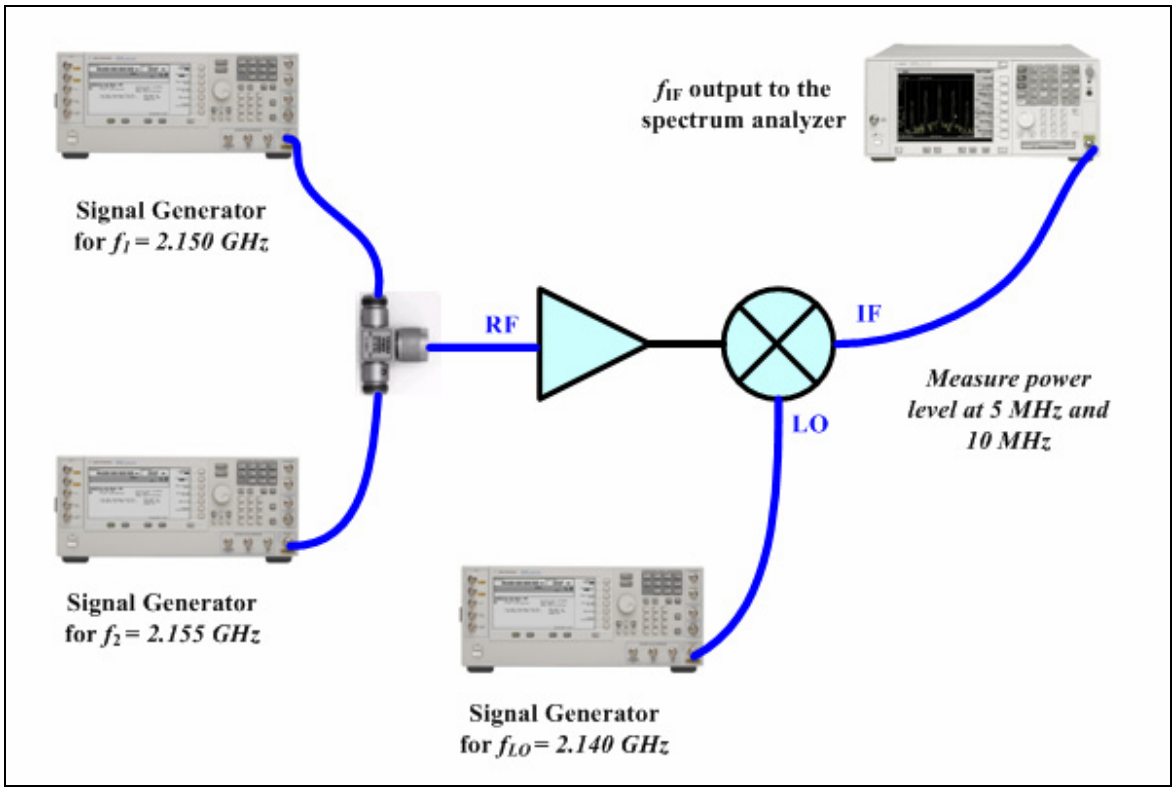

Figure D.4 Test setup for the IP2 measurement of front-end

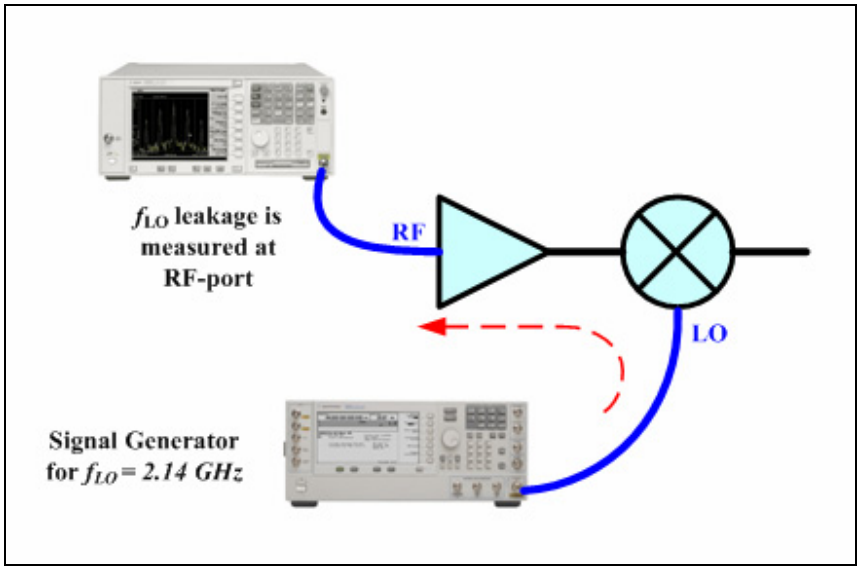

Figure D.5 Test setup for measurement of LO-RF leakage

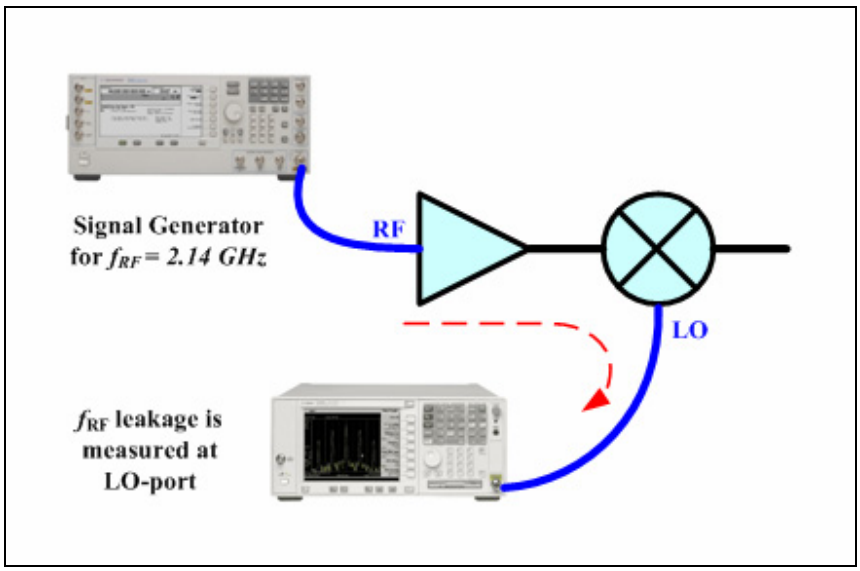

Figure D.6 Test setup for measurement of RF-LO leakage