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ADVANCED PROCESS AND EQUIPMENT CONTROL FOR THERMAL PROCESSING IN LITHOGRAPHY

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Contents

Summary

Lithography is the key technology driver and "bottleneck" controlling the device scaling, circuit performance and magnitude of integration for silicon semiconductors. Critical dimension (CD) or linewidth is one the most critical variable in the lithography process with the most direct impact on the device speed and performance. During the lithography sequence, one important source of CD variation comes from variations in photoresist properties including extinction coefficient and thickness. It is important to achieve a uniform extinction coefficient and thickness profile across wafer. This can be achieved by integrating control system into the existing process like softbake process. Previous works in the literature can only control the average uniformity of the extinction coefficient. Using a spectrometer, a multi-zone bakeplate and simple PI control algorithms, the temperature distribution of a bakeplate is manipulated in real-time to reduce the variation of extinction coefficient within wafer and from wafer to wafer.

It is also important to ensure the uniformity of the photoresist thickness across the substrate. An in-situ photoresist thickness contour monitoring system is proposed and developed by integrating a spectrometer to acquire the photoresist thickness contour on the wafer during the spin-coating step or edge-bead removal step. The influence of wafer warpage on the resist properties estimation is also investigated.

The temperature non-uniformity in post-exposure bake (PEB) process also contributes to the final variation in CD. A design of an integrated bake/chill module

for photoresist processing is then presented in the thesis, with an emphasis on the spatial and temporal temperature uniformity of the substrate. The system consists of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide real-time regulation of the substrate temperature. The feasibility of the proposed approach is demonstrated via detailed modelling and simulations based on first principle heat transfer analysis. Less than 0.1^oC temperature non-uniformity is achieved across the wafer substrate during the whole cycle of heating and cooling process.

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

The evolution of integrated circuit (IC) technology has been governed mainly by device scaling due to rapid technology development (Plummer *et al.*, 2000). However, the semiconductor industry is facing increasingly difficult challenges as the feature sizes go beyond 100 nm, which almost reach the physical limit of existing technology. One of the "grand challenges" is to make affordable lithography available at and below 100nm (ITRS, 2005).

For many years, as the key technology driver for semiconductor industry, optical lithography has been the engine driving Moore's Law. Lithography is also a significant economic factor, currently representing 30-35% of the chip manufacturing cost (Plummer *et al.*, 2000). Figure 1.1 depicts the typical steps in a lithography process (Quirk and Serda, 2001). This sequence of operations begins with a priming step to promote adhesion of the polymer photoresist material to the substrate. A thin layer of resist is spin-coated on the wafer surface. The solvent is evaporated from the resist by a baking process (softbake). After patterning with (deep UV) radiation, a post-exposure bake process is used to promote a reaction that alters the solubility of the resist in the exposed areas. A subsequent chemical

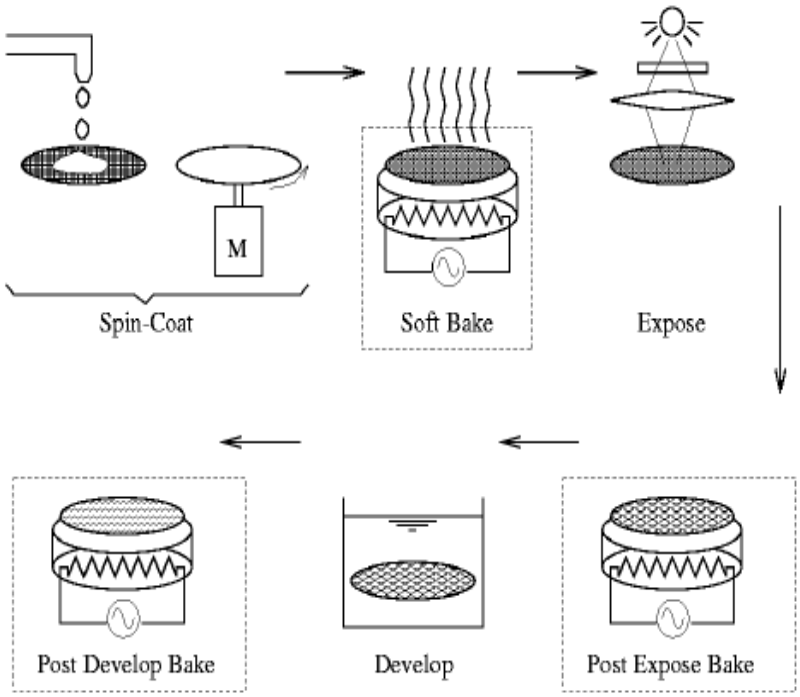

Figure 1.1. The typical lithography sequence including spin-coating, soft bake, exposure, post exposure bake, develop and post develop bake process.

develop step then removes the exposed/reacted resist material while keeping the non-exposed areas in place. The developed resist is then baked to promote etching stability. In addition to the exposure step, lithography requires precise thermal processing of the photoresist including softbake, post exposure bake (PEB) and post develop bake.

The most important variable in the lithography process is the linewidth or critical dimension (CD), which is the single variable with the most direct impact on the device speed and performance (Edgar *et al.*, 2000). CD control is required for obtaining adequate transistor, interconnect and consequently overall circuit performance. The application of advanced computational and control methodologies have seen increasing utilization in recent years to improve yields, throughput, and, in some cases, to enable the actual process to print smaller devices (Edgar *et al.*, 2000; Schaper *et al.*, 1999). The value of applying such mathematical systems

science tools to microelectronics manufacturing has already been demonstrated in the area of photoresist processing (Schaper *et al.*, 1999; Tay *et al.*, 2001; Ho *et al.*, 2002; Palmer *et al.*, 1996).

One exciting new challenge for process control is the development of control and optimization strategies that compensate for the non-uniform processing in one step (process) with that in another (Edgar *et al.*, 2000). An effective controller could work to resolve several integration problems, possibly speeding development time.

There are many factors that contribute to the final variation of the printed critical dimension (Zhang, 2002). Any drifts and variations in the lithographic process variables will affect the final linewidth. Two important sources of CD variation are: 1) photoresist properties non-uniformity, including extinction coefficient (Sheats and Smith, 1998; Sung *et al.*, 2000; Palmer *et al.*, 1996) and thickness variation (Levison, 1999; Lee *et al.*, 2002); 2) post-exposure bake temperature non-uniformity (Friedberg *et al.*, 2004; El-Awady, 2000; Leang *et al.*, 1996).

1.1.1 Effects of resist property variation in lithography process

The thickness and extinction coefficient are two of the photoresist properties that can have an impact on the CD uniformity (Lee *et al.*, 2002; Palmer *et al.*, 1996). The extinction coefficient is a measure of the absorption of the photoresist and determines the required exposure dose for printing the features (Sheats and Smith, 1998). Non-uniformity in extinction coefficient across the wafer will lead to non-uniformity in the linewidth (Sung *et al.*, 2000). Due to thin-film interference effects, CD varies with the resist thickness (Levison, 1999). The resist thickness has to be well controlled to remain at the the extrema of the swing curve where the sensitivity of CD to resist thickness variations is minimized (Brunner, 1991). In addition, the

industry is also moving toward 300mm wafers for economic reasons. This places a stringent demand on the lithographic processes as the control requirement is now stretched over a larger area.

1.1.2 Thermal effects in lithography process

Thermal processing of semiconductor substrates through conductive heat transfer is common and critical to the lithography process as shown in Figure 1.1. Each thermal processing step involves baking the substrate to an elevated temperature for a given period of time, this is then usually followed by a chill step which is used to cool the wafer to an appropriate temperature for subsequent processing (Plummer *et al.*, 2000). The effect of temperature on CD has been studied extensively. For every degree variation in wafer temperature uniformity, CD can vary as much as 20 nm (Levison, 1999). A 9% variation in CD per 1^oC variation in temperature has been reported for a Deep ultraviolet (DUV) resist (Leang *et al.*, 1996). As the width of the feature size continues to shrink, temperature uniformity specifications become more stringent. Table 1.1.2 shows the temperature requirements for different thermal processing steps in lithography (Parker and Renken, 1997). For some critical bake processes such as post-exposure bake (PEB), temperature uniformity as stringent as $\pm 0.1^oC$ is required.

In the conventional thermal processing of semiconductor substrate, the heated plate is usually thermally massive relative to the substrate and is held at a constant temperature by a feedback controller. Because of its large thermal mass and resultant sluggish dynamics, conventional hotplates are robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Other disadvantages include uncontrolled and nonuniform temperature fluctuation during the mechani-

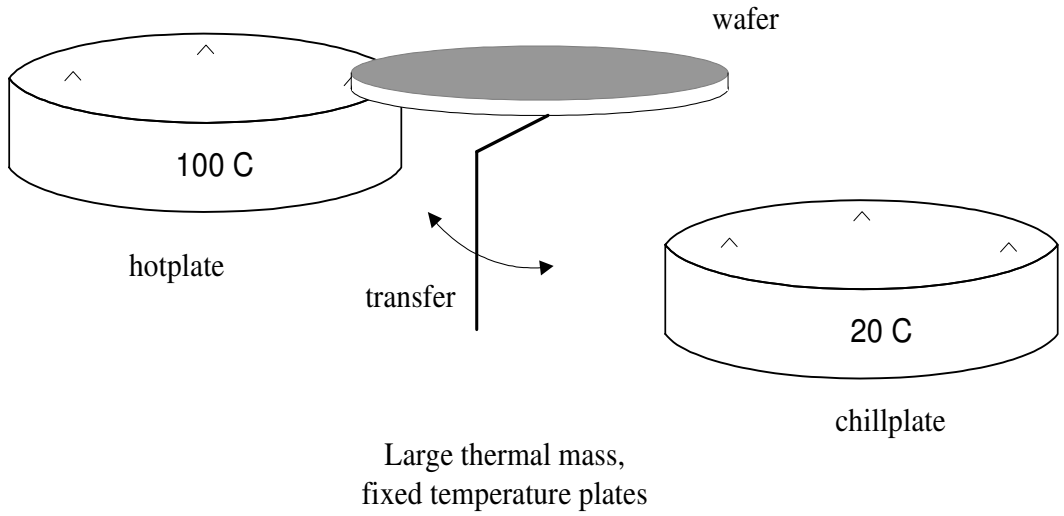

Figure 1.2. The conventional approach for lithography baking and chilling involves substrate transfer between large thermal mass, fixed temperature plates.

cal transfer of the substrate from bake to chill plates (see Figure 1.2), spatial temperature non-uniformities during the entire thermal cycle, etc (El-Awady, 2000). This lack of a method to conduct real-time distributed, closed-loop temperature control with conventional hotplates is a source of process error in the lithography chain.

Although some improvements are possible (Ho *et al.*, 2000; Tay *et al.*, 2001; Tay *et al.*, 2004*b*), we conclude that the conventional hotplate design has poor controllability that ultimately limits the achievable performance. Hence, new thermal processing system have to be developed for optimal processing of temperature-sensitive photoresist so as to address the abovementioned issues.

1.2 Contribution

In this thesis, the application of advanced process control and equipment control to reduce the process variation in lithography is investigated. This thesis addresses these areas: 1) Real-time monitoring and control of photoresist extinction coefficient uniformity; 2) In-situ monitoring of photoresist thickness contour in lithog-

Table 1.1. Temperature sensitivity of the thermal processing steps

Thermal Step	**Purpose**	**Temperature Range**	**Precision Required**
HMDS bake	Promote Adhesion	$70 - 150^oC$	$\pm 5^oC$
ARC bake	Cure ARC	$90 - 180^oC$	$\pm 1 - 2^oC$
Softbake	Drive off solvent stabilize thickness	$90 - 140^oC$	$\pm 1^oC$
Post-exposure bake (PEB)	i-line resist: smooth standing waves	$90 - 180^oC$	$\pm 0.5 - 1^oC$
PEB	DUV resist: deblock exposed resist	$90 - 150^oC$	$\pm 0.12 - 0.5^oC$
Post-develop bake	Improve etch stability	$120 - 180^oC$	$\pm 1^oC$

raphy; 3) Development of a lamp thermoelectricity based integrated bake/chill system for photoresist processing.

1.2.1 Real-time monitoring and control of photoresist extinction coefficient uniformity

Critical dimension (CD) is one of the most critical variables in the lithography process. The extinction coefficient can have an impact on the CD uniformity (Sung *et al.*, 2000). Non-uniformity in extinction coefficient across the wafer leads to non-uniformity in the linewidth. In this thesis, an innovative approach to control the within-wafer photoresist extinction coefficient uniformity is proposed and demonstrated. Previous research in the literature can only control the average uniformity of the extinction coefficient (Palmer *et al.*, 1996). Our approach uses an array of spectrometers positioned above a multizone bakeplate to monitor the extinction coefficient in real-time. The extinction coefficient can be extracted from the spectrometer data using standard optimization algorithms. With these in-situ measurements, the temperature profile of the bakeplate is controlled in real-time by manipulating the heater power distribution using conventional proportional-integral (PI) control algorithm. We have experimentally obtained a repeatable

improvement in the extinction coefficient uniformity within wafer and from wafer to wafer. A 70% improvement in extinction coefficient uniformity is achieved (Tay *et al.*, 2006).

The effect of warpage on the extinction coefficient estimation has also been investigated and an in-situ calibration method has been proposed. Based on it, accurate estimation of resist extinction coefficient in the presence of wafer warpage is obtained.

1.2.2 In-situ monitoring of photoresist thickness contour in lithography

The coating of photoresist on semiconductor substrate is a common process in the lithography sequence. It is important to ensure the uniformity of the photoresist thickness across the substrate as nonuniformity in photoresist thickness leads to nonuniformity in critical dimension (Levison, 1999). An in-situ photoresist thickness contour monitoring system has been proposed (Ho *et al.*, 2006). In the setup, a spectrometer is used to measure the photoresist thickness contour on the wafer after the spin-coat process or edge-bead removal process. The experimental results are compared with offline ellipsometer measurement. The worst-case error is experimentally found to be less than 2%.

1.2.3 A lamp thermoelectricity based integrated bake/chill system for photoresist processing

Thermal processing of semiconductor substrates through conductive heat transfer is critical to the lithography process. Of these baking steps, the post-exposure bake step is the most sensitive to temperature variation for the current generation of chemically-amplified resists (CARs) (Plummer *et al.*, 2000; Parker and Renken, 1997). In this thesis, a new design of an integrated bake/chill module

for photoresist processing in lithography is presented, with an emphasis on the spatial and temporal temperature uniformity of the substrate (Tay *et al.*, 2007). The system consists of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide real-time dynamic and spatial control of the substrate temperature. The TEDs also provide active cooling for chilling the substrate to a temperature suitable for subsequent processing steps. The use of lamps for radiative heating offers fast ramp-up and ramp-down rates during thermal cycling operations. In the proposed system, the bake and chill steps are integrated thereby eliminating the loss of temperature control typically encountered during the mechanical transfer from the bake to chill step as in the conventional lithography track system. The feasibility of the proposed approach is demonstrated via detailed modelling and simulations based on first principle heat transfer analysis, in particular the complete spectral optical properties of the wafer has been accounted for. The distributed nature of the design also engenders a simple decentralized control scheme which satisfies tight spatial and temporal temperature uniformity specifications. Original contributions have been made to account for spectral optical properties of wafer in the simulation. It is a new modelling with higher accuracy without assuming that the wafer is a opaque object. Based on it, new modelling of radiation absorption by translucent silicon wafer is proposed and implemented. A simple modelling of spiral wafer chiller is also presented.

1.3 Organization

This thesis is organized as follows. The first chapter covers the the motivation, contribution and organization of the thesis. Chapters 2, 3 and 4 discuss the real-time monitoring and control of photoresist properties in lithography. Chapter 2 presents an application of control system methodology for extinction coefficient uniformity

improvement by manipulating the power distribution for a multi-zone bakeplate. Chapter 3 investigates the effect of wafer warpage on the resist extinction coefficient and thickness estimation and proposes a calibration method for extinction coefficient estimation. In Chapter 4, an in-situ monitoring of photoresist thickness contour on wafer is implemented. Chapter 5 discusses a new design of integrated bake/chill equipment for photoresist processing in lithography. Chapter 6 gives the conclusions and recommendations for future work.

Chapter 2

Real-time Control of Photoresist Extinction Coefficient Uniformity

2.1 Introduction

To form the resist patterns, the wafer substrate is spin-coated with a thin film of resist, followed by a softbake process to remove excess solvent in the resist film. The desired patterns are then patterned onto the resist film by exposing the substrate with deep UV radiation. During the exposure step, some of the incident light is absorbed by resist and it becomes more soluble in develop solution for positive resist or less soluble for negative one. The extinction coefficient is a measure of the absorption of the photoresist and determines the required exposure dose for printing the features (Sheats and Smith, 1998). Non-uniformity in the extinction coefficient across wafer can result in the consequence that the resist is effectively underexposed where the extinction coefficient is lower and overexposed where it is higher (Plummer *et al.*, 2000). This leads to non-uniformity in the final CD printed on wafer. Hence, the uniformity of extinction coefficient has to be well controlled within wafer and from wafer to wafer. Furthermore, the industry is moving towards the use of 300 mm substrate for economic reasons. This places a

stringent demand on the lithographic processes as the control requirement is now stretched over a larger area.

Softbake process is performed after the spin-coating process (see Figure 1.1) to remove excess solvent from the resist film, reduce standing waves and relax the resist polymer chain into an ordered matrix (Plummer *et al.*, 2000). The temperature control during softbake process is important (Sheats and Smith, 1998; Ho *et al.*, 2000). Conventionally, the resist is baked at a fixed temperature with temperature of $\pm 1^oC$ for consistent lithographic performance (Sheats and Smith, 1998). In general, the resist extinction coefficient formed after the spin-coating process will not be uniform. If a non-uniform resist film is formed during spin-coating, experiments have shown that maintaining a uniform temperature profile across the bakeplate will not reduce the resist extinction coefficient non-uniformity.

Our approach to controlling the photoresist extinction coefficient uniformity make use of an array of in-situ photoresist film properties extraction sensors positioned above a multizone bakeplate (Schaper *et al.*, 1999; Tay *et al.*, 2001; Schaper *et al.*, 2003) to monitor and control the resist extinction coefficient. With these in-situ measurements, the temperature profile of the bakeplate is controlled in real-time by manipulating the heater power distribution using a standard PI controller for each of the zones. Various sites on the wafer are made to follow a predefined resist extinction coefficient trajectory to reduce the extinction coefficient non-uniformity at the end of the softbake process.

The literature consists of a number of different techniques for in-situ monitoring of photoresist properties during the different baking process in lithography (Paniez *et al.*, 1998; Fadda *et al.*, 1996; Morton *et al.*, 1999; Metz *et al.*, 1991; Leang and Spanos, 1996). In related work, Metz *et al.* (Metz *et al.*, 1991) used in-situ multi-wavelength reflection interferometers to measure the resist thickness versus bake time to determine the optimum bake time. Leang and Spanos (Leang and Spanos, 1996) developed a novel metrology using photospectrometers to monitor both resist

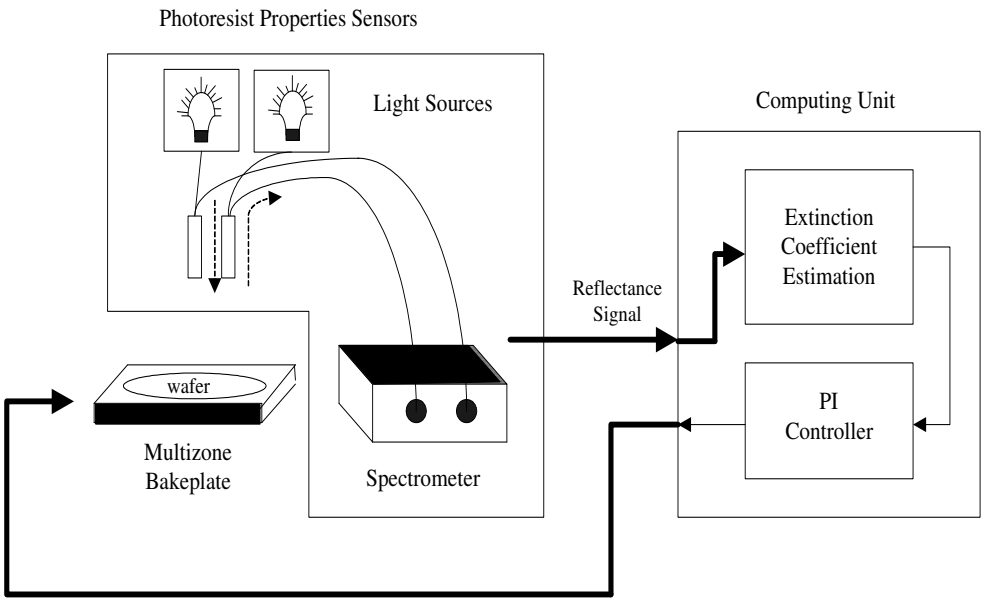

Figure 2.1. Schematics of the experimental setup used to control resist extinction coefficient. The system consists of three main parts: a multizone bakeplate, extinction coefficient sensors, and a computing unit.

thickness and photoactive compound concentration. Existing approaches in the literature (Palmer *et al.*, 1996) can only control the average non-uniformity of the extinction coefficient across the wafer from wafer-to-wafer, and it is not a real-time approach. Our approach make use of an array of multi-wavelength spectrometers to monitor and control the resist properties across the wafer in real-time during the softbake process. Our objective is to develop a metrology and control scheme capable of controlling the spatial uniformity of the photoresist extinction coefficient on the wafer.

2.2 Experimental setup

Figure 2.1 shows the experimental setup for monitoring and control of the photoresist properties during the softbake process. An array of 2 in-situ film properties extraction sensors is positioned above the wafer to monitor the resist extinction coefficient at 2 sites on the wafer as shown in Figure 2.1. The in-situ measure-

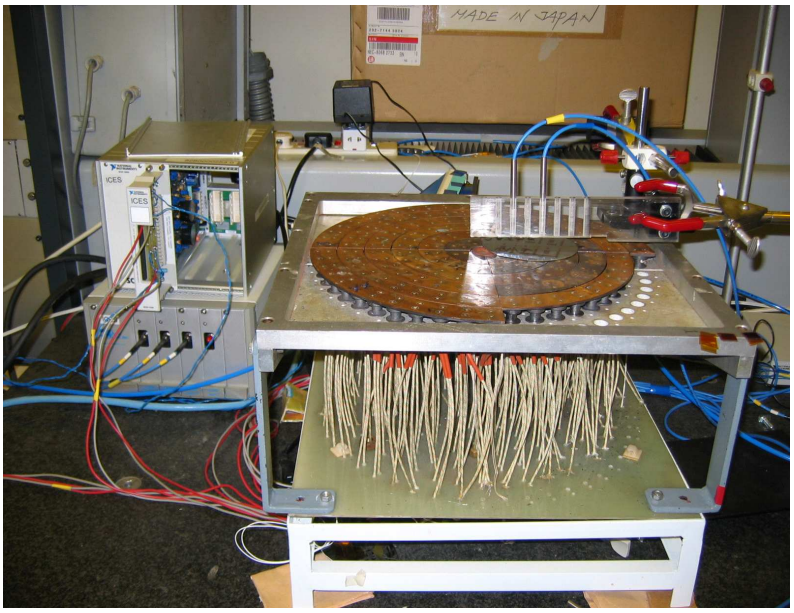

Figure 2.2. Photograph of the experimental setup.

ments are also used to detect the endpoint of the softbake process. The setup comprises a broadband light source (LS-1), a spectrometer with the capability of monitoring the reflected light intensity at two sites simultaneously (SQ2000) and a bifurcated fiber optics reflection probe (R200) from OceanOptics (*Product catalog*, 2002). The reflection probe consisting of a bundle of 7 optical fibers (6 illumination fibers around 1 read fiber) is positioned above the wafer to monitor the resist properties in real-time. During softbake, light from the broadband light source is focused on the resist through one end of the probe and the reflected light is guided back to the spectrometer through the other end. Figure 2.2 shows a photograph of the experimental setup.

The programmable thermal processing module developed comprises an array of heating zones that allow for spatial control of temperature in non-symmetric configurations. The schematics is shown in Figure 2.3. Resistive heating elements are embedded within each of the heating zones. The heating zone is configured with its own temperature sensor (RTDs) and electronics for feedback control. The heating zones are separated with a small air-gap of approximately 1 mm. The fact

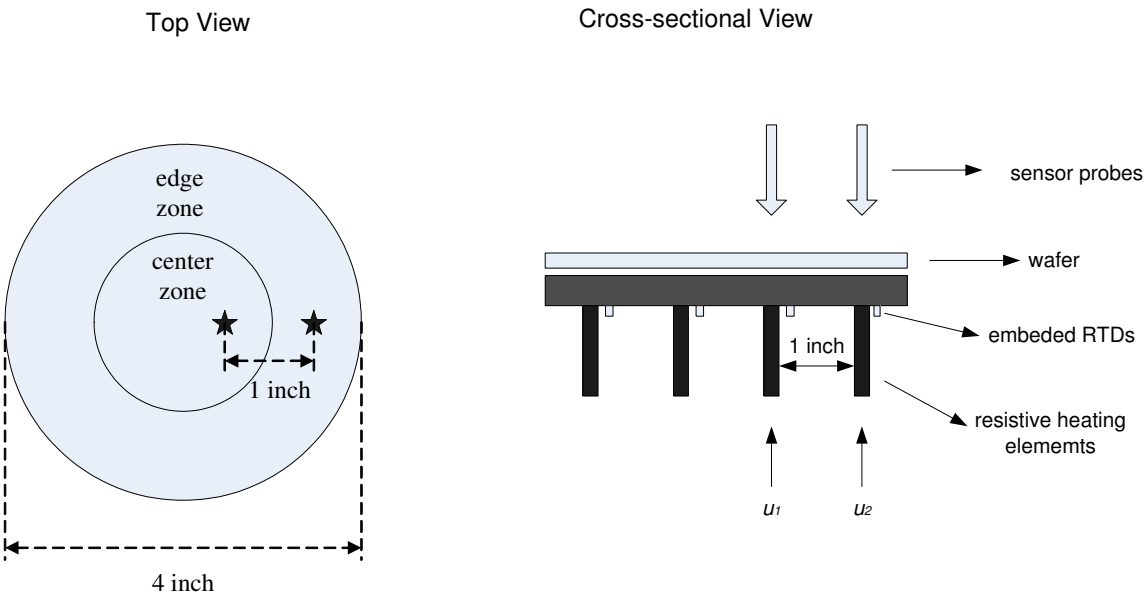

Figure 2.3. Schematics of multizone bakeplate

that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability. Its small thermal mass allows for fast dynamic manipulation of the temperature profile. Depending on the application, the number of zones of the bakeplate can easily be configured. We will make use of this system to control the photoresist extinction coefficient through temperature manipulation at different locations on the bakeplate in real-time.

For all our experiments, the photoresist used is Shipley 1813, a positive resist. The sampling rate is 1 second. In all our experiments, the resist is spin-coated at 2000 rpm for 30 seconds on a 4-inch wafer. The wafer is then baked for 3 minutes during the softbake process. On average, we have obtained about 70% improvement in extinction coefficient uniformity at steady-state. Currently, the experimental setup is for a 4-inch wafer. This can be easily scaled to a 12-inch wafer with the addition of more sensor probes. The number of sensors and hence the amount of computation required for a 12-inch wafer is roughly tripled and this should not be an issue. Besides silicon wafers, our method may also be applied to photomask manufacturing.

2.3 Photoresist extinction coefficient estimation

The photoresist extinction coefficient may be estimated from the reflectance signals of the multi-wavelength spectrometer using a thin film optical model. When light is focused onto the resist film, phase difference between the incident and reflected light creates interference effects within the resist. Consider an absorbing photoresist film with a complex index of refraction, n_r+ik. Its relation with the reflectance intensity is given by (Born and Wolf, 1980)

$$h(\lambda,k,y)=\frac{\rho_{12}^2e^{2k\eta}+\rho_{23}^2e^{-2k\eta}+2\rho_{12}\rho_{23}cos(\phi_{23}-\phi_{12}+2n_r\eta)}{e^{2k\eta}+\rho_{12}^2\rho_{23}^2e^{-2k\eta}+2\rho_{12}\rho_{23}cos(\phi_{23}+\phi_{12}+2n_r\eta)} \tag{2.1}$$

where

$$\begin{aligned}
\rho_{12}^2 &= \frac{(n_a-n_r)^2+k^2}{(n_a+n_r)^2+k^2},\\
\rho_{23}^2 &= \frac{(n_s-n_r)^2+k^2}{(n_s+n_r)^2+k^2},\\
\phi_{12} &= \arctan\frac{2k}{n_r^2+k^2-1},\\
\phi_{23} &= \arctan\frac{2kn_s}{n_r^2+k^2-n_s^2},\\
\eta &= \frac{2\pi}{\lambda}y;
\end{aligned}$$

and n_a, n_r and n_s are the refractive index of air, resist, and substrate, respectively. y is the resist thickness, k is the resist extinction coefficient and λ is the wavelength of light.

The resist refractive index, n_r, is a function of wavelength, λ, and is given by the Cauchy equation (Born and Wolf, 1980)

$$n_r(\lambda)=A+\frac{B}{\lambda^2}+\frac{C}{\lambda^4} \tag{2.2}$$

where A, B, C are the Cauchy parameters of the resist. The Cauchy parameters

for Shipley 1813 resist are $A = 1.5935$, $B = 1.8854\times10^4$, and $C = 4.1211\times10^6$.

Equation (2.1) is a function of wavelength, resist extinction coefficient and resist thickness. Leang and Spanos (Leang and Spanos, 1996) proposed an approach for estimating both the resist thickness and extinction coefficient at each time instant. First, at higher wavelength of the reflectance signal shown in Figure 2.4, the photoresist extinction coefficient of light is essentially zero (Leang and Spanos, 1996; Born and Wolf, 1980). Hence solving the best curve fit at these wavelength is equivalent to solving the resist thickness. Once the resist thickness is obtained, the resist extinction coefficient can be computed making use of the spectrum at shorter wavelengths, where resist is absorptive. The approach is thus to decouple the computation of the resist thickness and the extinction coefficient. Essentially, at higher wavelength, Equation (2.1) reduces to a function of wavelength and resist thickness, which is given as Equation (2.5); at shorter wavelength, with the computed thickness, Equation (2.1) reduces to a function of wavelength and resist extinction coefficient.

The solution to the above problem is non-convex and does not contain a global minimum over the search space. However, we have a reasonably good initial estimate of the resist thickness from the coating process. Therefore, a local minimum solution for the resist thickness is obtained using least square estimation. First, for thickness computation at the higher wavelengths, the extinction coefficient, k is zero and Equation (2.1) is approximated by taking the Taylor series expansion such that

$$h(\lambda, y) = h(\lambda, y_0) + \left.\frac{\partial h}{\partial y}\right|_{\lambda, y_0} \Delta y \tag{2.3}$$

where y_0 is the initial thickness estimate and $\partial h/\partial y$ the derivative. The estimated

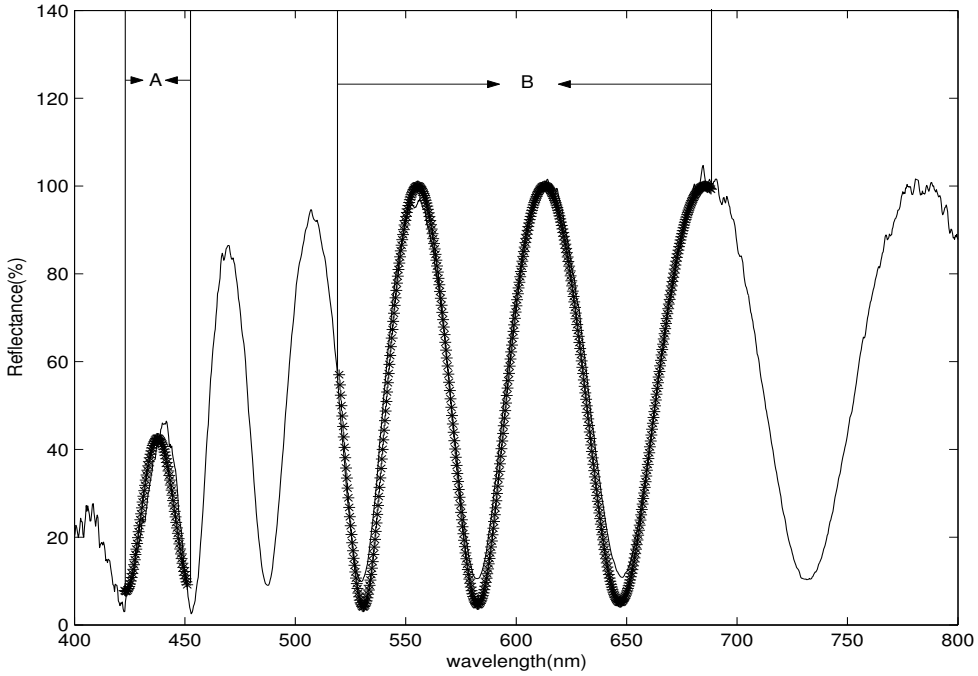

Figure 2.4. Extraction of resist thickness and extinction coefficient using least square estimation: range A is used to estimate extinction coefficient, while range B is used to estimate resist thickness. Solid line shows the experimental data while the '$*$'-line shows the theoretical fitted result.

resist thickness, $\hat{y}$, is given as

$$\hat{y} = y_0 + \Delta y \tag{2.4}$$

and the change in thickness, Δy, is estimated using the least square estimation

$$\Delta y = \left(\frac{\partial h}{\partial y}^T \frac{\partial h}{\partial y} \right)^{-1} \frac{\partial h}{\partial y}^T (h - h_0) \tag{2.5}$$

where

$$\frac{\partial h}{\partial y} = \begin{bmatrix} \left.\frac{\partial h}{\partial y}\right|_{\lambda_1, y_0} \\ \left.\frac{\partial h}{\partial y}\right|_{\lambda_2, y_0} \\ \vdots \\ \left.\frac{\partial h}{\partial y}\right|_{\lambda_M, y_0} \end{bmatrix} \qquad h = \begin{bmatrix} h(\lambda_1, y) \\ h(\lambda_2, y) \\ \vdots \\ h(\lambda_M, y) \end{bmatrix} \qquad h_0 = \begin{bmatrix} h(\lambda_1, y_0) \\ h(\lambda_2, y_0) \\ \vdots \\ h(\lambda_M, y_0) \end{bmatrix}$$

Once the resist thickness is obtained, for the computation of the resist extinction coefficient at shorter wavelengths, Equation (2.1) is approximated by taking the Taylor series expansion such that

$$h(\lambda, k) = h(\lambda, k_0) + \left.\frac{\partial h}{\partial k}\right|_{\lambda, k_0} \Delta k \tag{2.6}$$

where k_0 is the initial coefficient estimate and $\partial h/\partial k$ the derivative. The derivative is calculated using numerical method as the explicit expression of derivative is quite tedious. The estimated extinction coefficient is then given as

$$\hat{k} = k_0 + \Delta k \tag{2.7}$$

and the change in extinction coefficient, Δk, is estimated using least squares estimation

$$\Delta k = \left(\frac{\partial h}{\partial k}^T \frac{\partial h}{\partial k}\right)^{-1} \frac{\partial h}{\partial k}^T (h - h_0) \tag{2.8}$$

where

$$\frac{\partial h}{\partial k} = \begin{bmatrix} \frac{\partial h}{\partial k}|_{\lambda_1, k_0} \\ \frac{\partial h}{\partial k}|_{\lambda_2, k_0} \\ \cdots \\ \frac{\partial h}{\partial k}|_{\lambda_N, k_0} \end{bmatrix} \quad h = \begin{bmatrix} h(\lambda_1, k) \\ h(\lambda_2, k) \\ \cdots \\ h(\lambda_N, k) \end{bmatrix} \quad h_0 = \begin{bmatrix} h(\lambda_1, k_0) \\ h(\lambda_2, k_0) \\ \cdots \\ h(\lambda_N, k_0) \end{bmatrix}$$

To estimate the resist thickness and extinction coefficient, reflectance measurements are obtained at wavelength between 520-690 nm (501 points in total each 0.34 nm apart) and 420-450 nm (81 points in total each 0.35 nm apart) respectively. The initial estimated k_0 is updated with the current value of $\hat{k}$ at every sample. The curve fitting result is shown in Figure 2.4. The least squares estimation approach is compared with a nonlinear estimation approach. The nonlinear estimation method uses Equation (2.1) to search for a solution. Since no approximation is made to

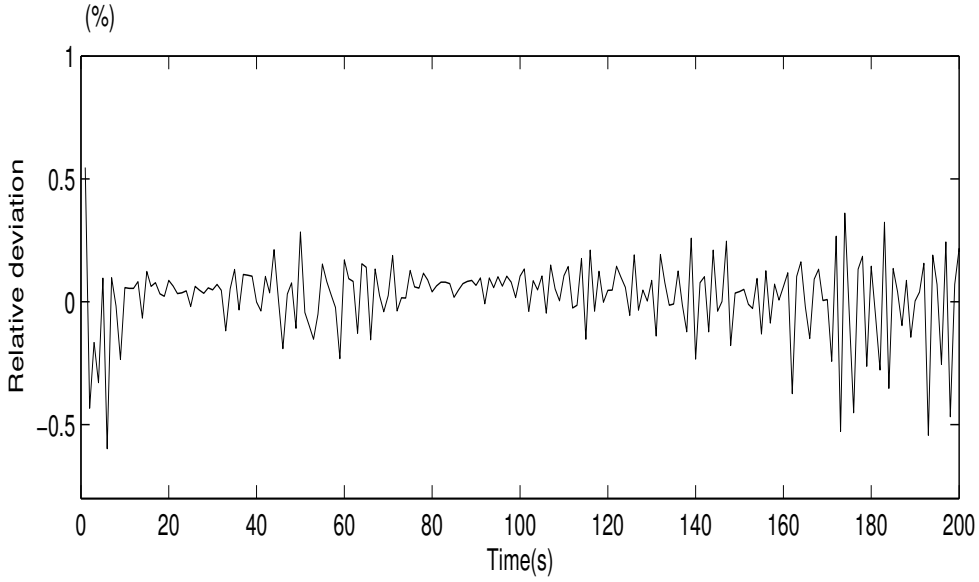

Figure 2.5. Comparison of least square estimation and nonlinear curve fitting methods of estimating photoresist extinction coefficient.

Equation (2.1) in this approach, it gives the most accurate measurements. The resist extinction coefficient obtained using least squares estimation is compared with the one using the nonlinear estimation method. Figure 2.5 shows the percentage deviation during the 200 seconds softbake. Despite making an approximation to Equation (2.1), there is only a negligible difference in the results between the least squares estimation and nonlinear estimation method.

2.4 Control of photoresist extinction coefficient uniformity

For conventional softbake, the wafer was baked at a uniform temperature of 90^0C across the whole bakeplate. During the softbake process, the extinction coefficients at two different sites (center zone and edge zone of wafer which is 1 inch apart along the radial direction, as shown in Figure 2.3) were monitored. A feedback controller is used to maintained the bakeplate temperature at 90^0C during

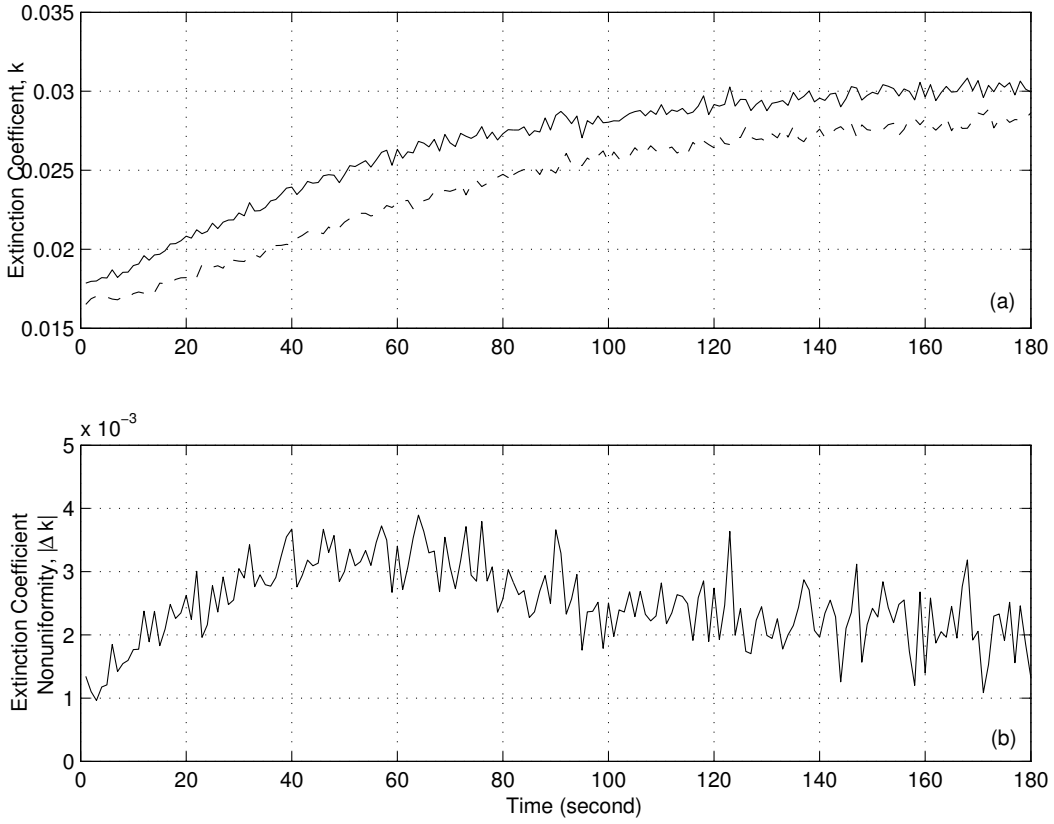

Figure 2.6. Conventional softbake with bakeplate maintained uniformly at 90^0C: (a) resist extinction coefficient, (b) resist extinction coefficient non-uniformity profile of the two sites monitored. Solid line represents center zone of the wafer, while dashed line represents edge zone.

the entire softbake process. Figure 2.6 shows the experimental result under conventional softbake. The experiment shows that at the end of the softbake process, the extinction coefficients is non-uniform. An average non-uniformity of 0.0023 in absolute extinction coefficient is obtained at steady-state as shown in Figure 2.6(b).

To control the extinction coefficient uniformity, the spectrometers is used to provide in-situ measurement of the resist extinction coefficient. Based on the measured information, two decentralized proportional-integral (PI) controllers of the following form are implemented:

$$u(t) = k_{Pi}e(t) + k_{Ii}\int e(t)dt$$

where $u(t)$ and $e(t) = k_{ref}(t) - k(t)$, are the control signal to the bakeplate and the error signal (difference between the reference extinction coefficient, $k_{ref}(t)$, and actual extinction coefficient, $k(t)$) respectively. The PI parameters for the center zone and edge zone are $k_{P1} = 320, k_{I1} = 5, k_{P2} = 335$ and $k_{I2} = 5$ respectively.

The above PI controllers are used to control the resist extinction coefficients at the two different sites to track a predefined reference trajectory. The reference trajectory shown in Figure 2.7(a) is designed by shifting the extinction coefficient trajectory of a typical conventional softbake extinction coefficient profile (e.g. Figure 2.6(a)) such that the trajectory settle at a certain peak value, e.g. 0.032 in our experiment. Other predefined trajectories can also be implemented. The experimental results were shown in Figure 2.7. After about 35 seconds, the resist extinction coefficients of two different sites begin to converge to the specified target extinction coefficient. At about 90 seconds, the extinction coefficients approaches and is maintained at the peak value of 0.032. An average extinction coefficient non-uniformity of 0.0007 was maintained at steady-state, as shown in Figure 2.7(d). As shown in Figure 2.7(b), a non-uniform bakeplate temperature profile is required to maintain a uniform resist extinction coefficient. The corresponding heater power is shown in Figure 2.7(c).

Next, the repeatability of the proposed approach is demonstrated in Figure 2.8. Experimental runs 1 to 3 is for the case of conventional softbake while experimental runs 4 to 9 is for the case of multizone PI controlled softbake. On average a 70% improvement is achieved in the resist extinction coefficient average non-uniformity.

2.5 Conclusion

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control and signal processing methods are effec-

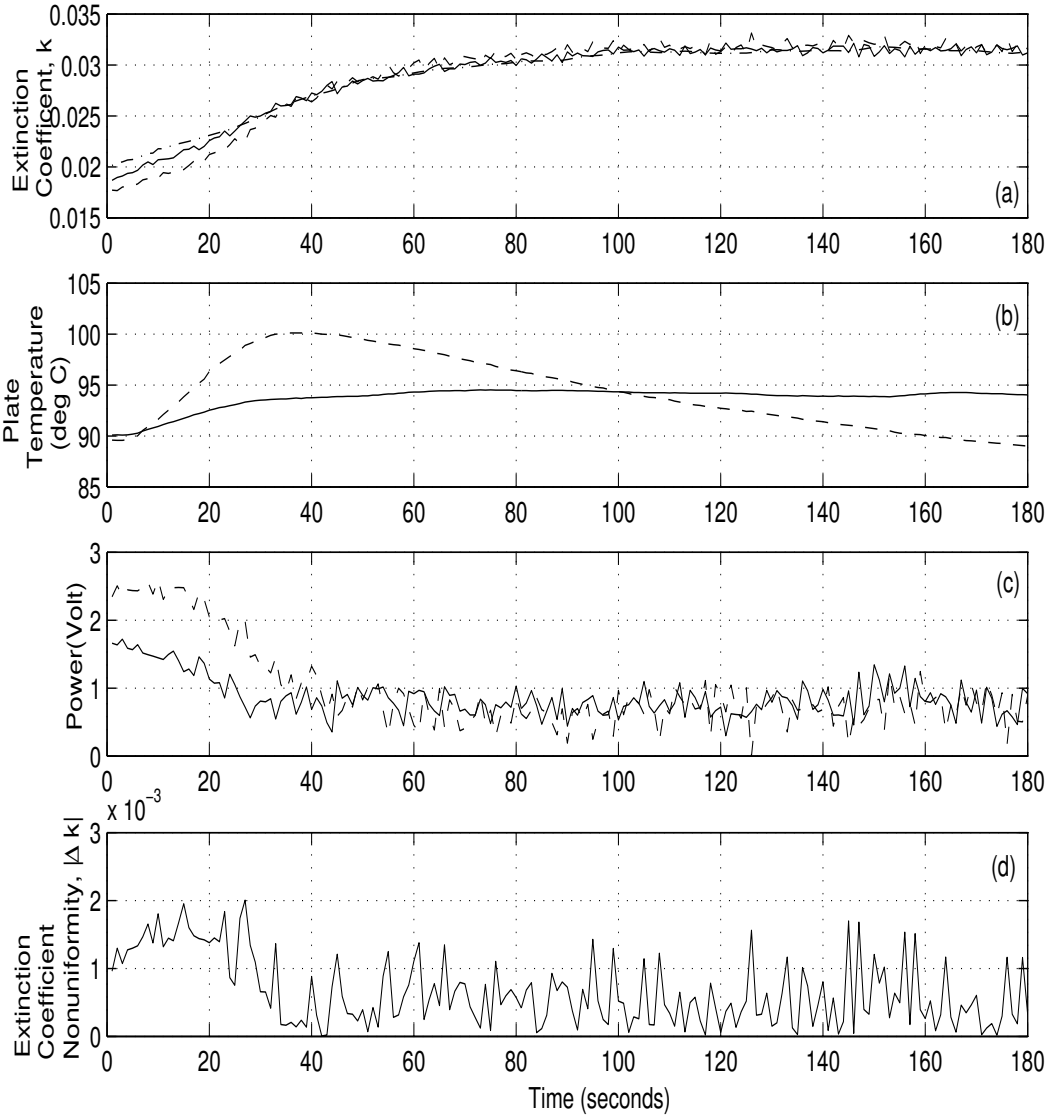

Figure 2.7. Multizone softbake with PI controllers: (a) resist extinction coefficient, (b) bake plate temperature, (c) heater power, (d) resist extinction coefficient non-uniformity profile of the two sites monitored. Solid line represents center zone of the wafer, while dashed line represents edge zone. The reference extinction coefficient trajectory is given by the dash-dot line in plot (a).

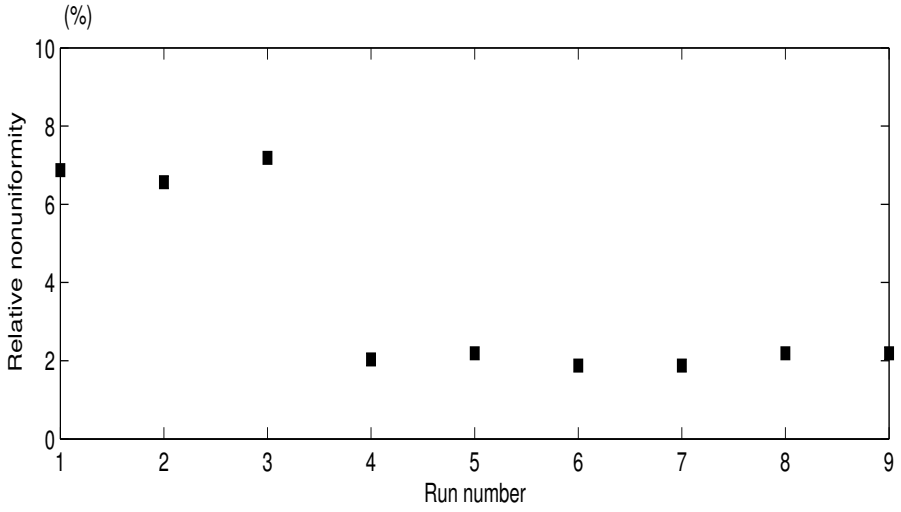

Figure 2.8. Extinction coefficient non-uniformity comparison for different experimental runs. The first three runs are under the conventional bake, while the next 6 runs are using the multizone bake with real-time control.

tive in reducing the enormous costs and complexity associated with the lithography sequence. In this chapter, real-time control of extinction coefficient has been implemented using an array of in-situ spectrometers, a multizone bakeplate and a conventional PI control strategy. It has been demonstrated that by maintaining a nonuniform temperature profile through the manipulation of power distribution, an average of 70% improvement in resist extinction coefficient nonuniformity has been obtained across the wafer and from wafer to wafer.

Chapter 3

Photoresist Extinction Coefficient and Thickness Estimation in the Presence of Wafer Warpage

3.1 Introduction

Resist extinction coefficient and thickness are two important parameters in the lithography process (Palmer *et al.*, 1996; Lee *et al.*, 2002). Both of them can have an impact on the final CD printed on wafer (Levison, 1999; Sung *et al.*, 2000). Hence, accurate estimation of these two parameters is critical for CD control as feature size continually shrinks. Estimation of these photoresist film properties can be obtained using reflectrometry (Leang and Spanos, 1996). In related work, Metz *et al.* (Metz *et al.*, 1991) used in-situ multi-wavelength reflectometer to measure the resist thickness versus bake time to determine the optimum bake time. In Lee *et al.* (Lee *et al.*, 2002), in-situ thickness measurements using reflectometer was used to realize a thickness control strategy, thereby reducing the resist thickness non-uniformity at the end of the process.

The above mentioned monitoring methods using reflectometer work under the

assumption that the inspected wafer is flat. Wafer warpage is common in microelectronics processing. Warpage can affect device performance, reliability and linewidth or critical dimension (CD) control in various microlithographic patterning steps. Warped wafers also affect the various baking steps in the lithography sequence (Ho *et al.*, 2004).

Wafer warpage will result in a non-uniform distance between the wafer and the sensors (e.g. reflectometers) mounted above the wafer. As such, the measured data from the sensors have to be compensated to account for the variation in distance. In this chapter, the effect of wafer warpage on the accuracy of resist properties estimation is investigated and an in-situ calibration method is proposed. We will also demonstrate how the measured data can be used to detect wafer warpage in real-time during wafer processing. This is an improvement compare to existing methods which are mainly off-line where the wafer have to be removed from the processing chamber to the measurement system.

Current techniques for measuring wafer warpage include thermal processing method (Ho *et al.*, 2004; Tay *et al.*, 2005), capacitive measurement probe (Poduje and Balies, 1988), shadow Moire technique (Wei *et al.*, 1998), and pneumatic-electromechanical technique (Fauque and Linder, 1998). The thermal method (Ho *et al.*, 2004) is an in-situ detection method which requires no extra sensor and can be realized in a common thermal processing step. The rest methods are offline methods where the wafer has to be removed from the processing equipment and placed in the metrology tool resulting in increase of processing steps, time and cost.

3.2 Experimental setup

Figure 3.1 shows the schematics of the warped wafer and flat wafer (Tay *et al.*, 2005). Warpage is realized by mechanically pressing the center of the wafer against

a thermal insulating tape of known thickness. No tape is used under the center of wafer so that the warpage is decided by the proximity pin height l_p. The proximity pin height can be increased at interval of 55 μm. For all our experiments, the degree of warpage corresponds to 55, 110, 165, and 220 μm.

The experimental setup is shown in Figure 3.2. The sensor probe from a reflectometer is positioned above the warped wafer or flat wafer with a distance of 4 mm and it is perpendicularly pointing to the center ares to acquire the reflected light intensity. The reflectometer sensor has the same setup as the sensor used in Chapter 2. It comprises a broadband light source (LS-1), fiber optics reflection probe (R200), and a spectrometer from Ocean Optics (*Product catalog, 2002).* The reflection probe consisting of a bundle of 7 optical fibers(6 illumination fibers around 1 read fiber) is positioned above the wafer to monitor the resist properties in real-time. The reflectance signal collected by the spectrometer is transmitted to the computer, from which the resist properties including the resist thickness, extinction coefficient can be estimated. The algorithms of properties estimation will be discussed in the next section. By analyzing the acquired reflectance signal, we also notice that the spectral reflectance curve itself is related the degree of warpage, which make the in-situ detection of warpage possible using the acquired reflectance curve.

Two types of photoresist are used the photoresist used in the experiments, namely Shipley 1813 (g-line resist) and SL4000 (DUV resist). The Cauchy parameters of refractive index for Shipley 1813 resist are $A = 1.5935$, $B = 1.8854\times10^4$, and $C = 4.1211\times10^6$. And for SL4000, $A = 1.546$, $B = 0.59\times10^4$, and $C = 6\times10^8$. The Shipley 1813 resist is spin-coated at 1000 rpm on wafer A, and 2000 rpm on wafer B. SL4000 resist is coated at 1000 rpm on wafer C.

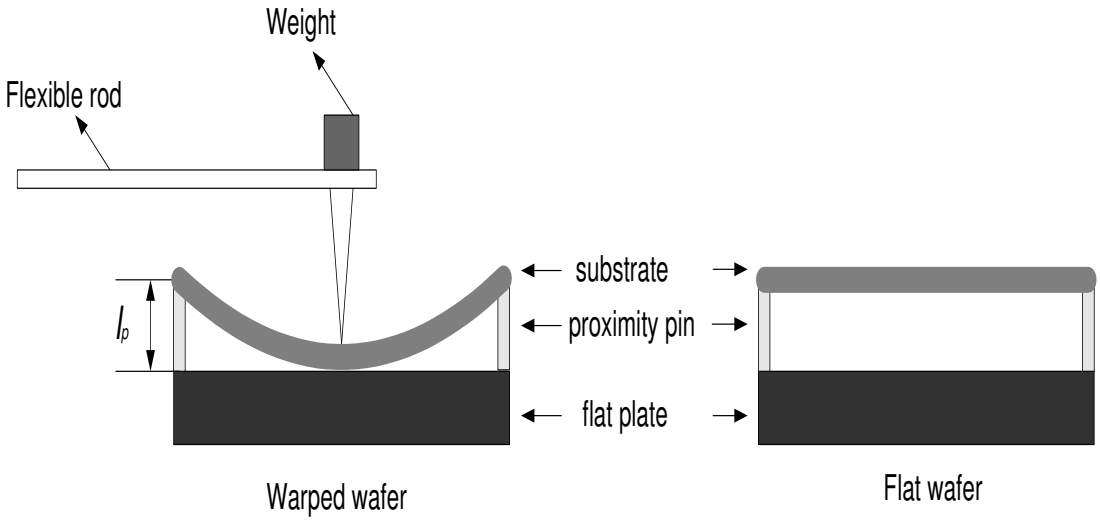

Figure 3.1. Schematics of warped substrate and flat substrate

3.3 Photoresist properties estimation

The photoresist thickness and extinction coefficient can be estimated from the reflectance signals using a thin film optical model, as done in Chapter 2. When light is focused onto the resist film, phase difference between the incident and reflected light creates interference effects within the resist. Consider an absorbing photoresist film with a refractive index of n_r, a extinction coefficient of k and a thickness of y, they relate to the reflectance light intensity as given in Equation (2.2).

Equation (2.2) is a function of wavelength, resist extinction coefficient and resist thickness. The detailed estimation algorithms for resist thickness and extinction coefficient have also been elaborated in Chapter 2. They are summarized as follows. First, at higher wavelength of the reflectance signal shown in Figure 3.3, the photoresist extinction coefficient of light is essentially zero (Leang and Spanos, 1996; Born and Wolf, 1980). Hence solving the best curve fitting at these wavelength is equivalent to solving the resist thickness. Once the resist thickness is obtained, the resist extinction coefficient can be computed making use of the spectrum at shorter wavelengths, where resist is absorptive. The approach is thus

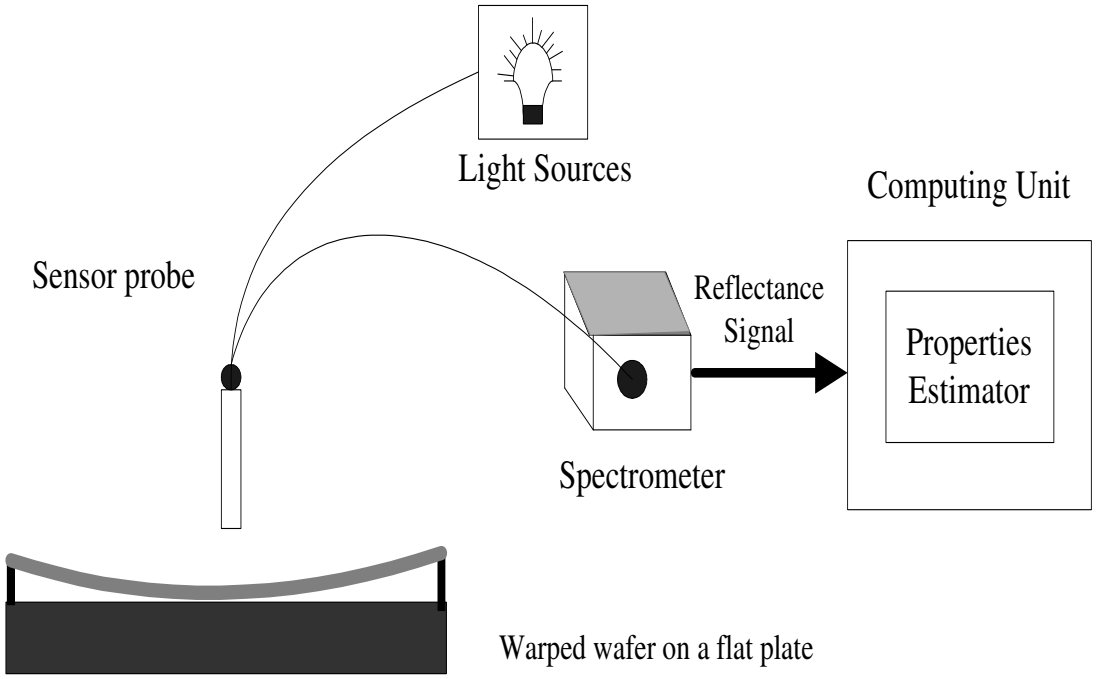

Figure 3.2. Experimental setup, including warped wafer, reflectometer sensor, and computing unit

to decouple the computation of the resist thickness and the extinction coefficient. Essentially, at higher wavelength, Equation (2.2) reduces to a function of wavelength and resist thickness; at shorter wavelength, with the computed thickness, Equation (2.2) reduces to a function of wavelength and resist extinction coefficient.

To estimate the resist thickness and extinction coefficient, reflectance measurements are obtained at wavelength between 625-800 nm and 420-450 nm, respectively. To extract resist thickness and extinction coefficient, the problem is formulated as

$$\min \sum_{\lambda=625nm}^{800nm} (h_{meas}(\lambda, y) - h_{theo}(\lambda, y))^2 \tag{3.1}$$

and

$$\min \sum_{\lambda=420nm}^{450nm} (h_{meas}(\lambda, k) - h_{theo}(\lambda, k))^2 \tag{3.2}$$

where h is the relative reflectance data and λ is the wavelength. h_{meas} refers to

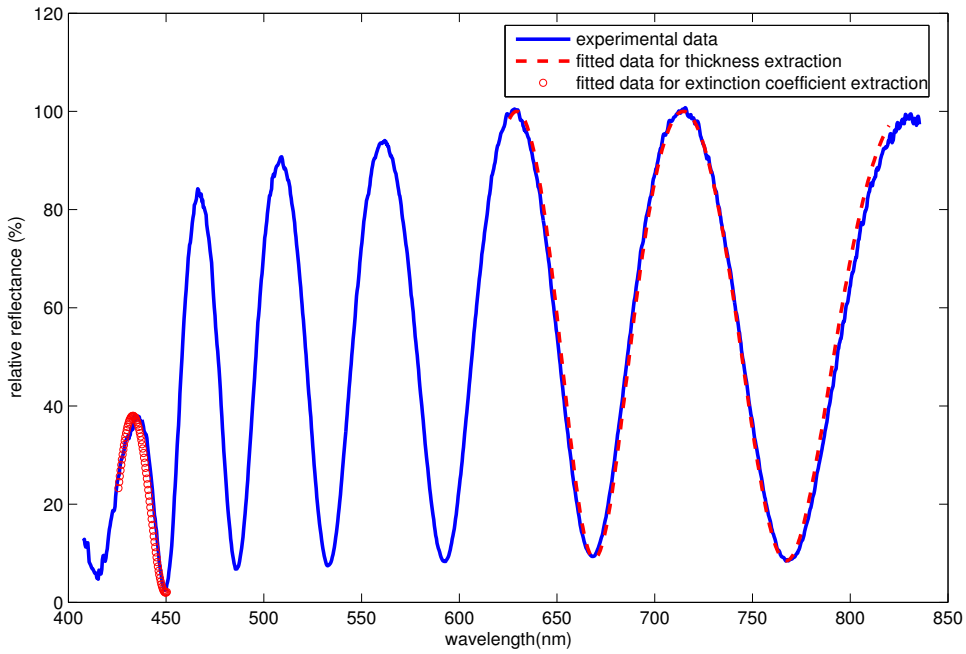

Figure 3.3. Extraction of resist thickness and extinction coefficient for flat wafer: low wavelength range is used to estimate extinction coefficient, while high wavelength range is used to estimate resist thickness.

the measured reflectance data while h_{theo} refers to the theoretical reflectance data based on the thin-film model given in Equation (2.2).

Due to the limitation of the tungsten halogen light source, only the film thickness can be estimated for wafer C which is coated with a DUV resist SL4000. The tungsten halogen light source used in the resist extinction coefficient extract only emits light with wavelength above 300nm. But for SL4000 resist it is a DUV resist which is sensitive to light with a wavelength of 248. Excimer light source has to be used to extract its extinction coefficient.

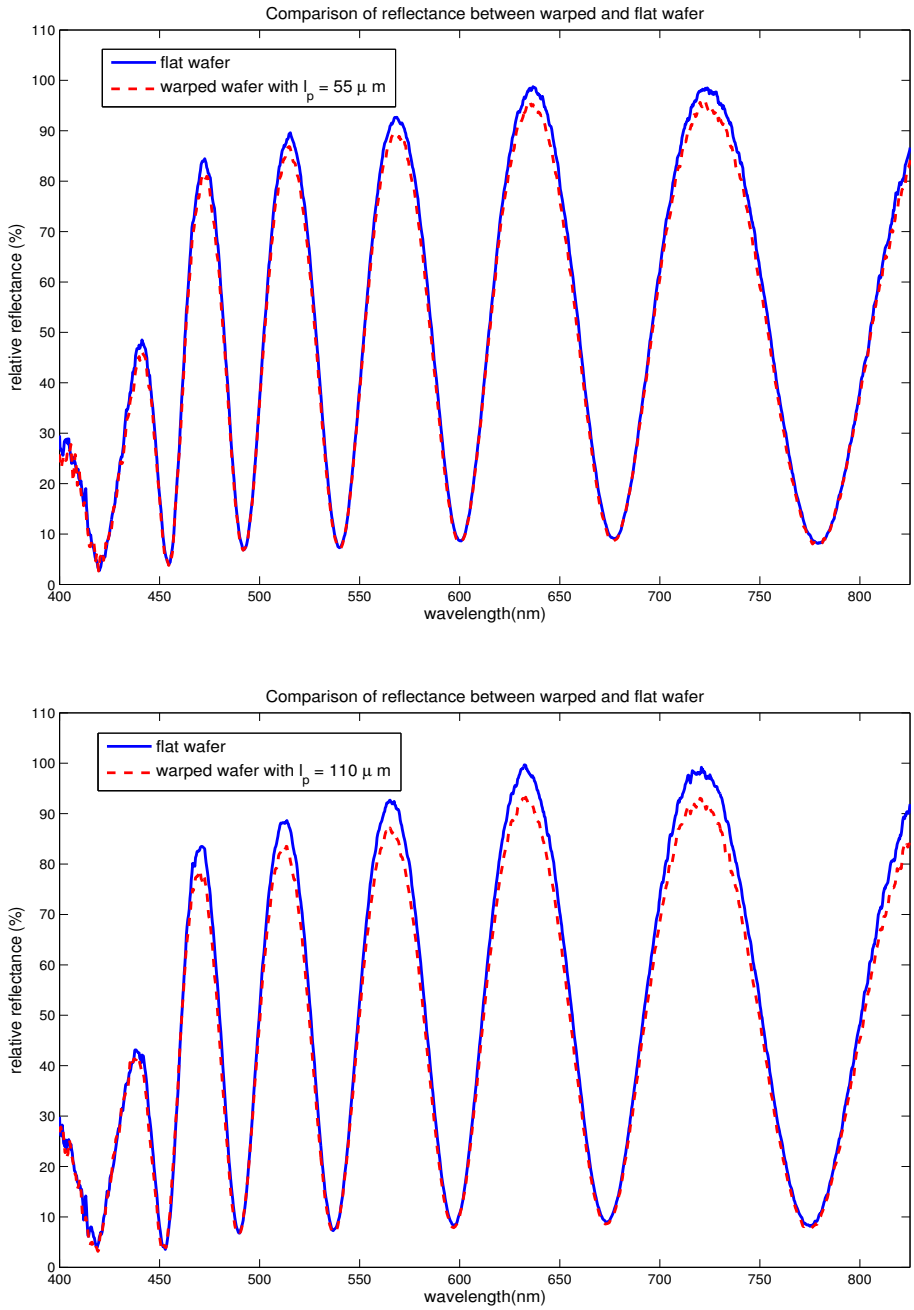

Figure 3.4. Comparison of reflectance curve between flat wafer and warped wafer. Wafer warpage $l_p = 55\mu m$ and $l_p = 110\mu m$. The solid line is the reflectance curve for flat wafer, while the dash line is the one for warped wafer.

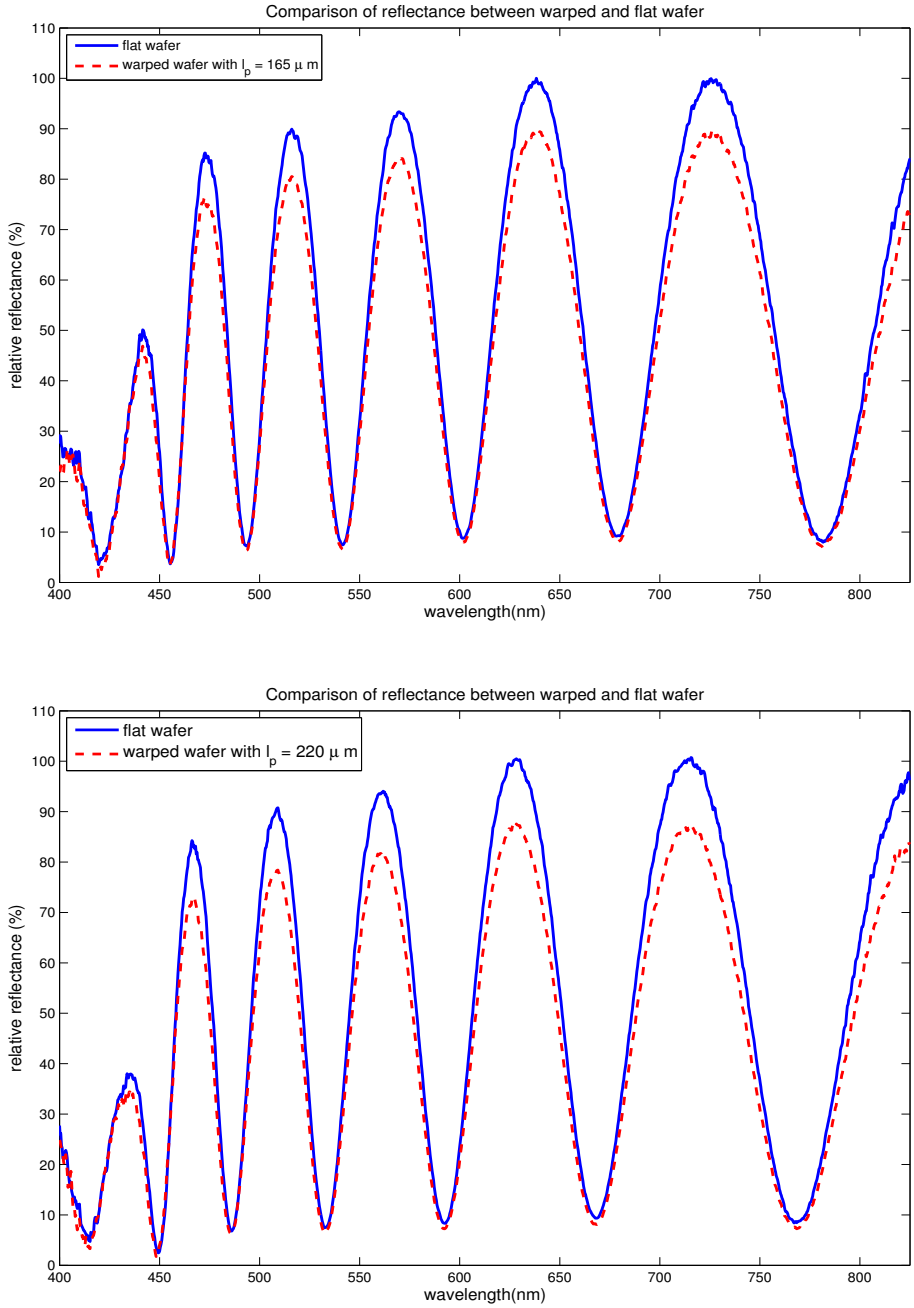

Figure 3.5. Comparison of reflectance curve between flat wafer and warped wafer. Wafer warpage $l_p = 165\mu m$ and $l_p = 220\mu m$. The solid line is the reflectance curve for flat wafer, while the dash line is the one for warped wafer.

Table 3.1. Estimation of resist thickness (y (nm))

proximity pin height	wafer A		wafer B		wafer C	
	flat	warped	flat	warped	flat	warped
55 μ m	1556.6	1556.1	1110.2	1110.2	246.6	246.7
110 μ m	1547.9	1547.8	1120.1	1119.6	234.7	234.7
165 μ m	1560.9	1560.8	1133.6	1132.5	238.7	238.8
220 μ m	1534.8	1535.2	1128.8	1127.3	237.4	237.7

3.4 Effect of warpage on photoresist properties estimation

Spectral reflectance signal of bare wafer is used as a reference. For wafer coated with a layer of resist, the thin film effect will cause constructive and destructive interference at different wavelength, as shown in Figure 3.3. This figure shows the reflectance curve for flat wafer. The wafer warpage effectively changes the distance between the probe tip and wafer surface, which can affect the acquired reflected light intensity. The effect of different warpages on the spectral reflectance curve is illustrated in Figure 3.4 and Figure 3.5.

From Figure 3.4 and Figure 3.5 show that the peaks of the reflectance curve is lower when the wafer is warped. The higher the proximity pin the larger the drop. Based on the acquired reflectance data for warped wafer, the resist properties including the film thickness and extinction coefficient can be estimated using the same method described in the previous section.

The estimated resist thickness and extinction coefficient for both flat and warped wafer are summarized in Table 3.1 and Table 3.2. For the three different wafers, wafer A is coated with Shipley 1813 photoresist with a spin speed of 1000 rpm; wafer B is coated with Shipley 1813 photoresist with a spin speed of 2000 rpm and wafer C is coated with SL4000 photoresist with a spin speed of 1000 rpm. y is

Table 3.2. Estimation of resist extinction coefficient (k)

proximity pin height	wafer A			wafer B		
	flat	warped	calibrated	flat	warped	calibrated
55 μ m	0.018	0.019	0.018	0.035	0.036	0.034
110 μ m	0.020	0.022	0.020	0.029	0.032	0.029
165 μ m	0.016	0.019	0.016	0.027	0.032	0.027
220 μ m	0.024	0.028	0.024	0.027	0.033	0.027

the thickness in nm and k is the extinction coefficient. From Table 3.1, it is observed that the deviation of thickness estimation between flat and warped wafer is negligible. But it is a different situation for the estimation of k and the estimated extinction coefficient is inflated due to the existence of warpage.

The fitting of experimental data with theoretical data for warped wafer is shown in Figure 3.6. We can see the fitting is not good for thickness estimation but the peak and valley positions of both the theoretical and measured reflectance curve remain at the same wavelength. It is resulted from the spectral optimization regulated as Equation (3.1). It is observed that reflectance curve down-shift has very small effect on the estimation of resist thickness, as there is negligible left-or-right curve shift. But it is different with the estimation of extinction coefficient k. As extinction coefficient is related to the amount of light that is being absorbed by the resist, a shift (in this case, a lower value) of reflectance curve will induce an error in the coefficient estimation, that is the estimated extinction coefficient will become larger than its real value.

The percentage of deviation for extinction coefficient $\delta k\%$ are computed as

$$\delta k\% = \frac{k_{warped} - k_{flat}}{k_{flat}} \tag{3.3}$$

The deviation for thickness $\delta y\%$ can be calculated in the same way. The deviation percentage of calculated parameters are shown in Figure 3.7.

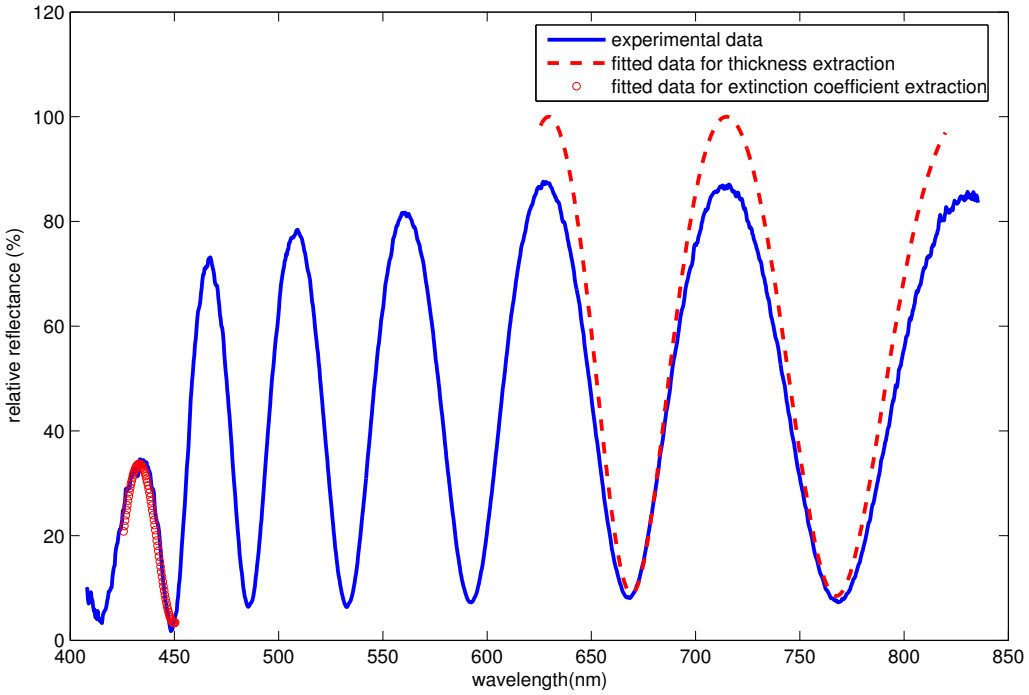

Figure 3.6. Extraction of resist thickness and extinction coefficient for warped wafer.

From Figure 3.7, we observe that the relationship between the deviation percentage of extinction coefficient and warpage can be approximated by a linear model. Based on the average deviation for wafer A and wafer B, a linear deviation model $\delta k\%$ is obtained using least square estimation as

$$\delta k = 0.11 \times l_p - 1.47 \tag{3.4}$$

where l_p is the proximity pin height in the unit of micron (μm). The linear model is plotted as dash line, also shown in Figure 3.7.

Based on the linear deviation model, real-time calibration of extinction coefficient estimation can be realized provided that the wafer warpage l_p is known. The

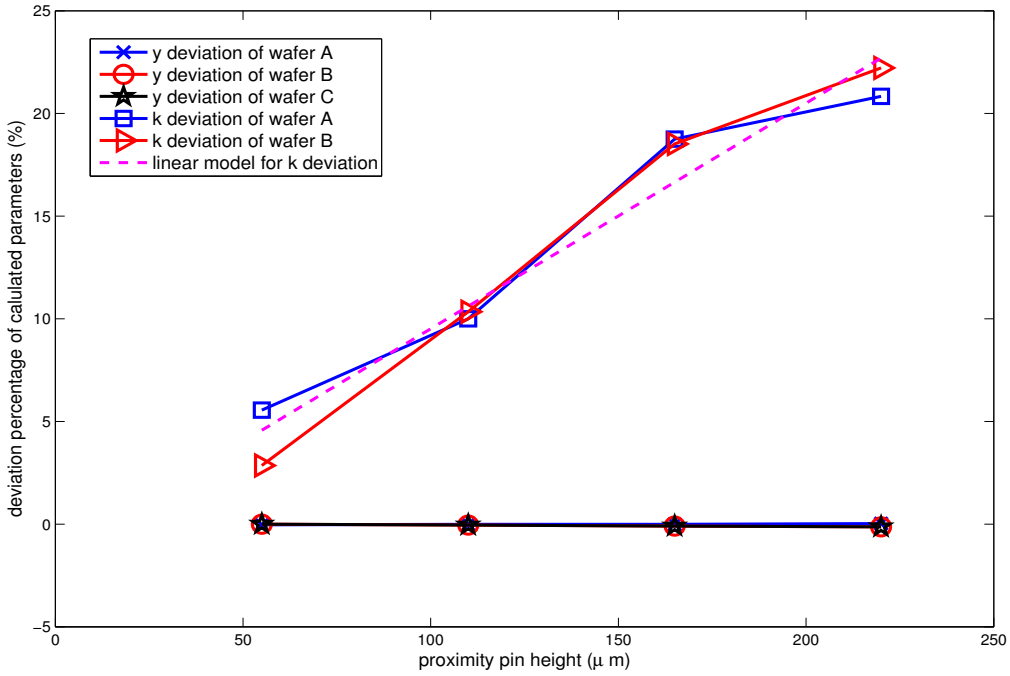

Figure 3.7. Effect of wafer warpage on the thickness and extinction coefficient estimation.

real value k_{real} can be calibrated as

$$k_{real} = k_{flat} = \frac{k_{warped}}{1 + \delta k\%} = \frac{k_{warped}}{1 + (0.11 \times l_p - 1.47)/100} \tag{3.5}$$

Using the calibration model, the extinction coefficient estimation is calibrated and summarized in the Table 3.2. We found that the calibrated extinction coefficient is almost the same as it real value. Accurate estimation of extinction coefficient (k) is achieved.

3.5 In-situ detection of wafer warpage

The spectroscopic reflectometer is conventionally used as a sensor for resist properties estimation. A reflectance curve down-shift is observed in the presence of wafer warpage. The percentage of down-shift is strongly related to the warpage. A figure

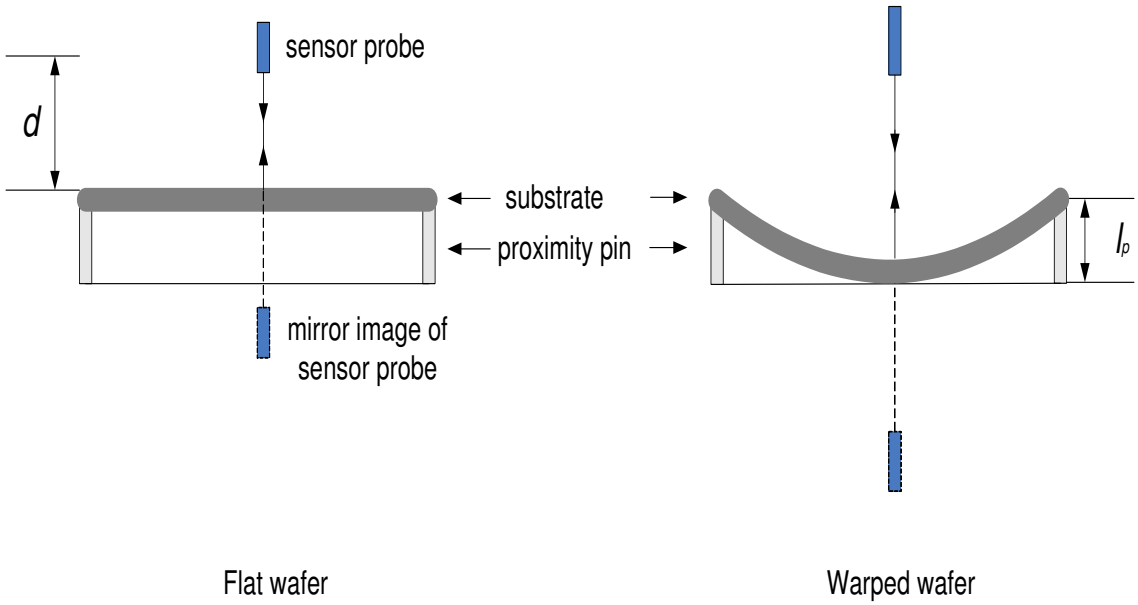

Figure 3.8. Calculation of reflected light intensity deviation using inverse square law

of peak percentage downshift from original 100% for different warpages is shown in Figure 3.9. The experimental results show that the reflectance downshift percentage is strongly depended on the proximity pin height (which means warpage) but weakly related to different coating conditions.

The inverse square law of light (Born and Wolf, 1980) states that the rectilinear light intensity is inversely proportional to the square of the distance from the source of light ray.

Based on the inverse square law, the theoretical light intensity deviation due to the wafer warpage can be solved. As for the sensor probe used in the experiment, the illumination and read fibers are bundled together. we have to assume that the position of the light source is at the mirror image of the sensor probe with respect to wafer surface. And it is demonstrated in Figure 3.8. Using the inverse square law, the reflected light intensity deviation $\delta R\%$ between warped wafer and flat wafer can be calculated as

$$\delta R\% = 1 - \frac{I_{warped}}{I_{flat}} = 1 - \frac{(2 * d)^2}{(2 * (d + l_p))^2} = 1 - \frac{d^2}{(d + l_p)^2} \tag{3.6}$$

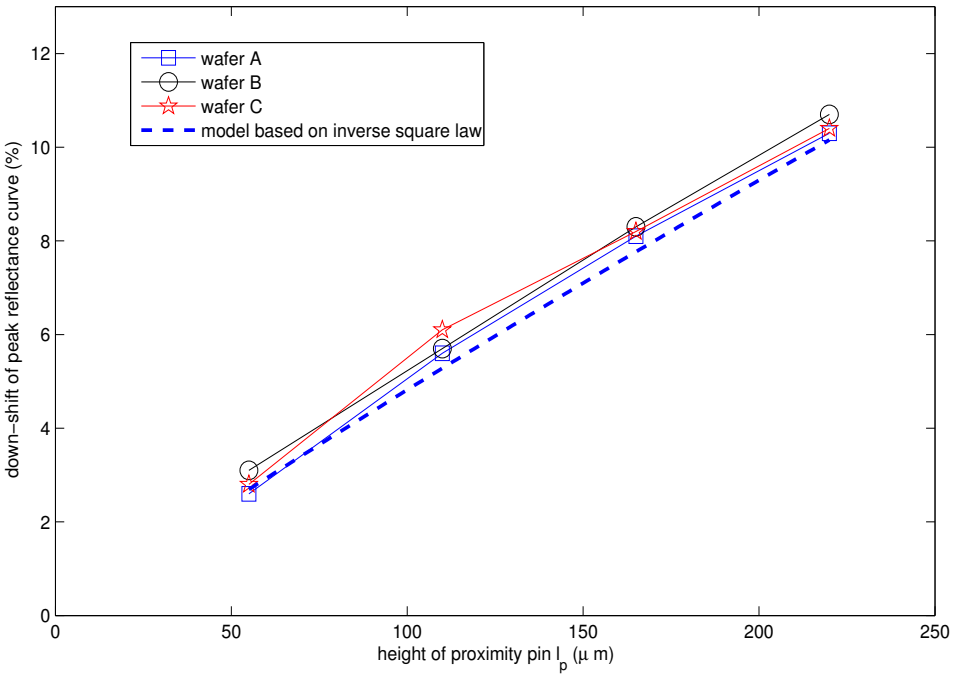

Figure 3.9. Validation of light intensity deviation model with experimental data

whereby I_{warped} and I_{flat} are the reflected light intensity for warped wafer and flat wafer, respectively. d is the distance from sensor probe to flat wafer surface while l_p is the warpage. Equation (3.6) can be easily used for in-situ warpage detection using reflectometer.

The theoretical prediction is compared with the experimental results, as shown in Figure 3.9. In the experiment $d = 4$mm. The experimental results show good agreement with the model given in Equation (3.6).

The procedures for warpage detection and estimation calibration is as follows. In the process of measuring resist properties using reflectometer, Equation (3.6) is used for warpage detection. With the availability of warpage information, Equation (3.5) can then be applied for calibration of extinction coefficient estimation so that accurate estimation of resist extinction coefficient is realized. The wafer warpage information can also be used in the subsequent process steps for feedforward control.

3.6 Conclusion

In this chapter, the effect of wafer warpage on the accuracy of resist properties estimation is investigated and an in-situ calibration method for extinction coefficient estimation is proposed. Accurate estimation of resist extinction coefficient is achieved. This calibrated estimation can be used as further information for real-time control to improve the resist properties control and ultimately CD control. Based on the proposed approach, it is also demonstrated how wafer warpage can be detected in real-time using conventional reflectometers during the thermal processing steps in lithography.

Chapter 4

In-Situ Monitoring of Photoresist Thickness Contour in Lithography

4.1 Introduction

As the feature size of semiconductor devices decrease dramatically, the challenge to accomplish efficient monitoring of process status in the semiconductor manufacturing process becomes more difficult (ITRS, 2005). One of the key parameters is the resist thickness contour on the wafer because of its impact on the critical dimension (CD) uniformity across wafer (Sheats and Smith, 1998).

During the exposure step, some of the incident light propagates through the resist film and reflects at the substrate-resist interface. The phase difference between the incident and reflected light creates an interference effect within the resist film and the total amount of light absorbed by the resist film "swings" up and down as a function of resist thickness, typically knows as a swing curve (Sheats and Smith, 1998). As a result, the final CD also varies with resist thickness (Levison, 1999), as given in Figure 4.1. The CD can vary as much as 4 nm for every 1 nm change in resist thickness (Brunner, 1991). Furthermore, the industry is also moving towards the larger 300 mm wafers for economic reasons and uniformity tends to deteriorate

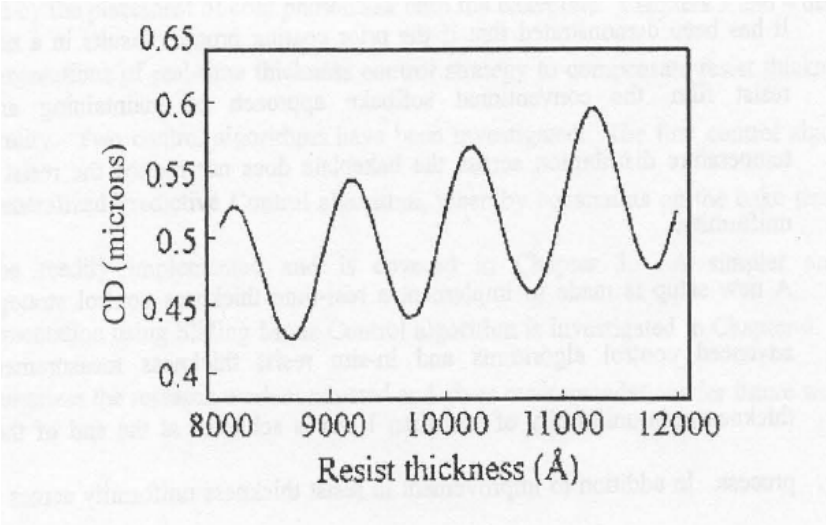

Figure 4.1. Variation of CD with resist thickness

for a larger surface area.

In a streamlined process flow of microelectronics production, there is tremendous benefit to perform in-situ monitoring of process status so that defective wafer can be detected early. Rectifications can be made before the defective wafer proceeds to downstream processes incurring unnecessary costs. Our objective is to develop an in-situ thickness contour monitoring system such that a wafer once coated with photoresist can immediately be inspected to determine its suitability for subsequent processes.

There have been some research on in-situ monitoring of the resist thickness and properties. To study the bake mechanism, Paniez *et al.* (Paniez *et al.*, 1998) used in-situ ellipsometry while Fadda *et al.* (Fadda *et al.*, 1996) used contact angle measurements to monitor the resist thickness. Morton *et al.* (Morton *et al.*, 1999) used in-situ ultrasonic sensors to monitor the change in resist properties to determine whether the resist has been sufficiently cured, thereby determining the endpoint of the softbake process. In related work, Lee *et al.* (Lee *et al.*, 2002) used in-situ multiwavelength reflection spectrometer to measure the resist thickness versus bake time and then real time feedback control applied to improve thickness uniformity.

In reference (Lin, 1999), a plastic-fiber-bundle probe array was applied to monitor the photoresist thickness change at multiple sites for developing rates and also develop endpoint could be determined.

In contrast with the multiple-probe instrument (Lin, 1999), we propose a new instrumentation that uses only one probe attached to a linear slider to monitor resist contour on the wafer.

Typically the coating process involves the spraying of photoresist on a spinning wafer before transferring to another station to remove the edge beads that have built up during the spin coat process. Edge bead removal (Romig *et al.*, 1996) is performed immediately after spin coat by directing a stream of remover near the edge of the wafer while it is spinning. A spectrometer attached to a linear slider mounted above the spinning wafer can be used to take measurements to give the contour of the photoresist thickness. For convenience, readings are taken at low speed. Specifically, measurement can be taken at the end of the spin-coat process when the spinning slows down to stop. Alternatively, measurements can be taken at low spinning speed before and/or after the dispensing of the edge bead removal when spinning begins and ends.

In the following sections, the experimental setup and theoretical analysis are described. It is followed by the description of thickness estimation algorithm and experimental results. Finally, some conclusions would be given.

4.2 Experimental setup

The experimental setup used to demonstrate the concept consists of three main parts as shown in Figure 4.2: a motor to spin the wafer, a spectrometer attached to a linear slider and a computing unit. The photo is shown in Figure 4.3. In all experiments, commercial DUV resist Shipley SL4000 was spin-coated on an 8-inch wafer. The thickness profile across the wafer was monitored.

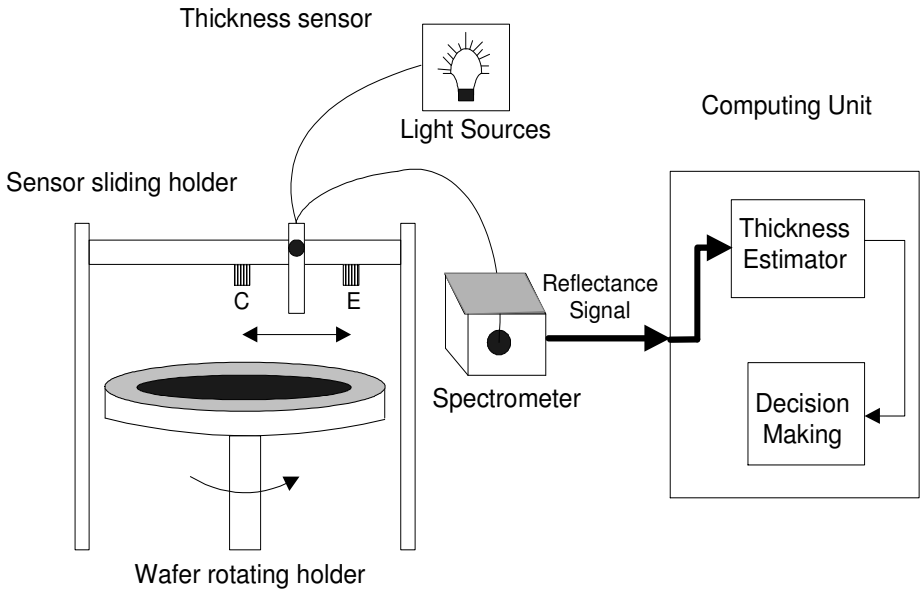

Figure 4.2. Experimental setup, including the X-Y table, spectrometer sensor, and computing unit

The spectrometer probe was attached to a linear slider mounted above the spinning wafer and moved back and forth continuously between the center and edge of the wafer. The sliding speed can be adjusted to monitor different points on the wafer.

The thickness sensor has a similar setup as the multiwavelength DRM (Henderson *et al.*, 1998). It comprises a broadband light source (LS-1), a spectrometer with the capability of monitoring the reflected light intensity(S2000), and a bifurcated fiber optics reflection probe consisting of a bundle of 7 optical fibers (6 illumination fibers and around 1 read fiber) is positioned above the wafer to monitor the resist thickness in real time.

The reflectance signals were acquired through the A/D converter and the computing unit converts them to thickness measurements using a thickness estimation algorithm in a LabView environment. The thickness estimation algorithm is dis-

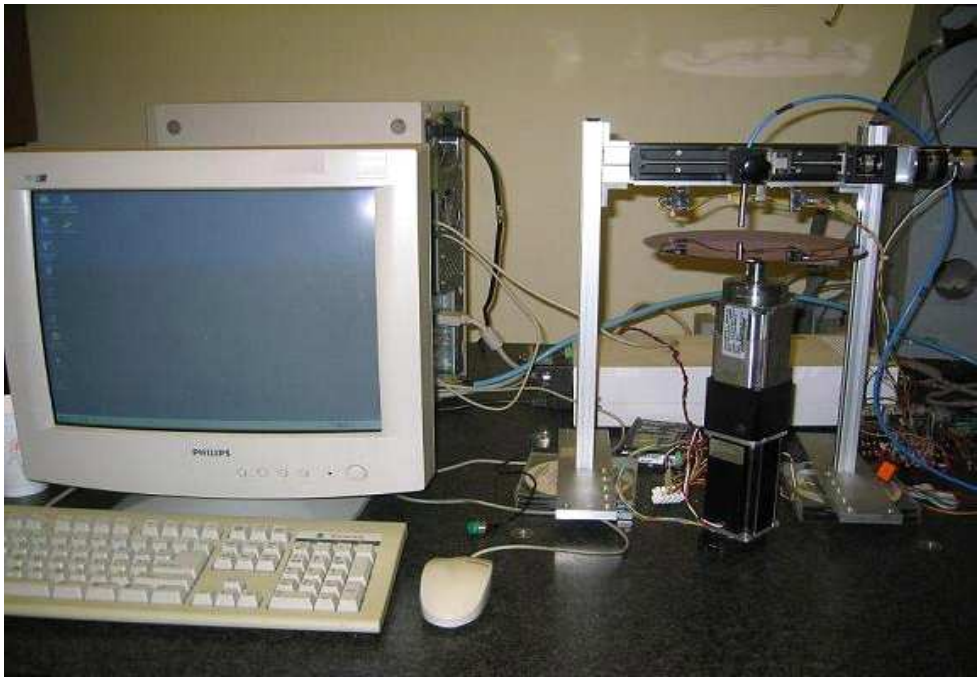

Figure 4.3. The experimental setup for photoresist thickness contour monitoring

cussed later. With the availability of the entire thickness contour across wafer, proper assessment and rectification actions can be taken.

4.3 Reflection of light by moving medium

Reflection of electromagnetic wave by a moving medium has been investigated by numerous researchers. For a detailed review readers can refer to the paper (Huang, 1996). Two factors affects a moving medium reflectivity measurement: reflection angle and reflection coefficient. For the reflection angle, the ordinary law of reflection may not be valid when the plane is moving. Consider the construction of Figure 4.4 and the equation below (Gjurchinovski, 2004) which gives the relationship between the incident angle α and reflected angle β as a function of the relative moving velocity v

$$\frac{sin\alpha - sin\beta}{sin(\alpha + \beta)} = \frac{v}{c} sin\varphi \tag{4.1}$$

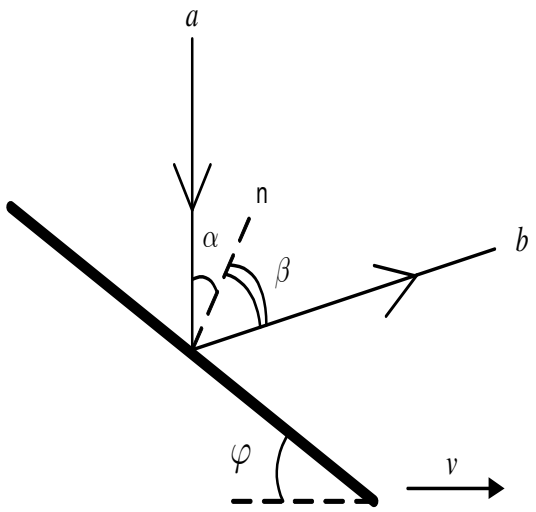

Figure 4.4. The geometry of the problem. The plate is moving at a constant speed of v. a is the incident light, with a angle of α. b is the reflected light, with a angle of β.

where c is the speed of light in air. In the experimental setup, $\varphi = 0$ for the normal incidence of light. Hence the ordinary law of reflection $\alpha = \beta$ still holds, which means that the reflected light of normal incident light is still normal.

Next, we consider the reflection coefficient. If the incident light is not normal to the moving plate, the reflection coefficient expression is complex. But for the experimental setup, the incident light is normal to the moving wafer. The reflection coefficient is given as (Shiozawa *et al.*, 1967)

$$r = -\frac{n^2 - \sqrt{\frac{n^2-\gamma^2}{1-\gamma^2}}}{n^2 + \sqrt{\frac{n^2-\gamma^2}{1-\gamma^2}}} \tag{4.2}$$

where n is the refractive index of the moving medium, and $\gamma = \frac{v}{c}$. For the stationary medium or low speed moving medium ($v \approx 0$), Equation (4.2) can be simplified to the familiar equation

$$r = \frac{1-n}{1+n} \tag{4.3}$$

Combined with the thin film reflectivity given in Equation (4.5), the influence

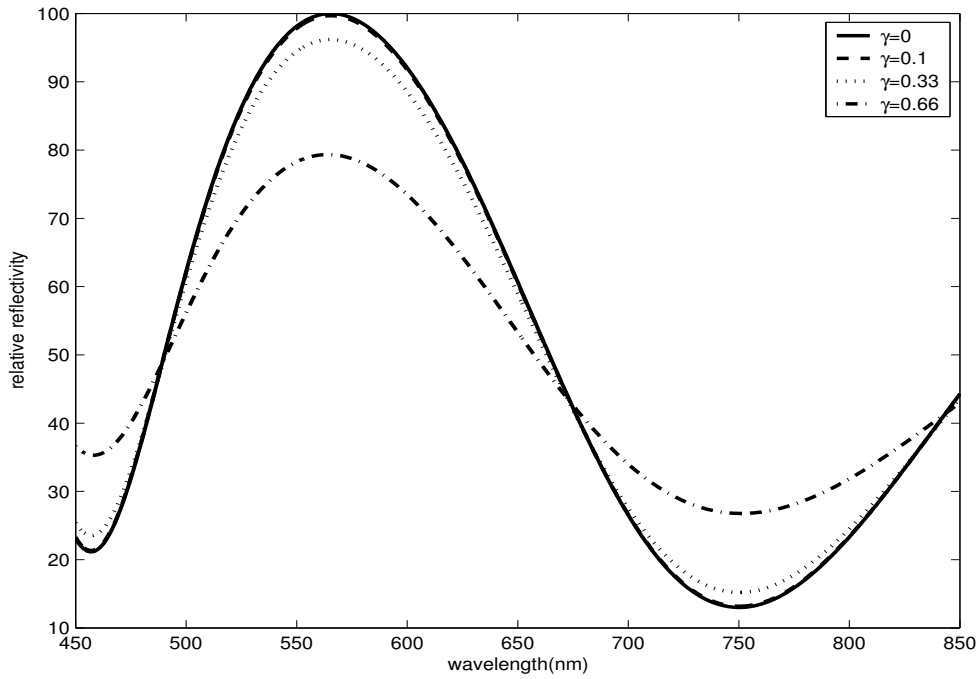

Figure 4.5. The influence of moving speed to the spectral reflectivity curve. $\gamma = \frac{v}{c}$ where v is the speed of moving plate and c the speed of light in the air.

of speed on the spectral reflectivity curve can be computed as shown in Figure 4.5. From this figure, we can see that at low speed ($\gamma < 0.1$) the spectral reflectivity is almost the same as the stationary case. Only at high speed, the spectral reflectivity curve will deviate noticeably from its stationary counterpart.

Figure 4.6 is a quantitative investigation of reflectivity deviation under different wafer rotating speed. The sensor probe is fixed at the edge of 200mm wafer and the incident light is normal to the wafer surface. The calculated maximum reflectivity deviation in the spectrum of 450-850nm corresponding different wafer rotating speed is given in the figure. It demonstrates that at low wafer rotating speed, the spectral reflectivity is essentially the same as that of stationary wafer.

In our experiment, the relative wafer moving speed corresponding to the incident light can be calculated, based on the schematics of Figure 4.7. The relative wafer moving speed can be calculated as

$$v = \sqrt{v_S^2 + v_R^2} \tag{4.4}$$

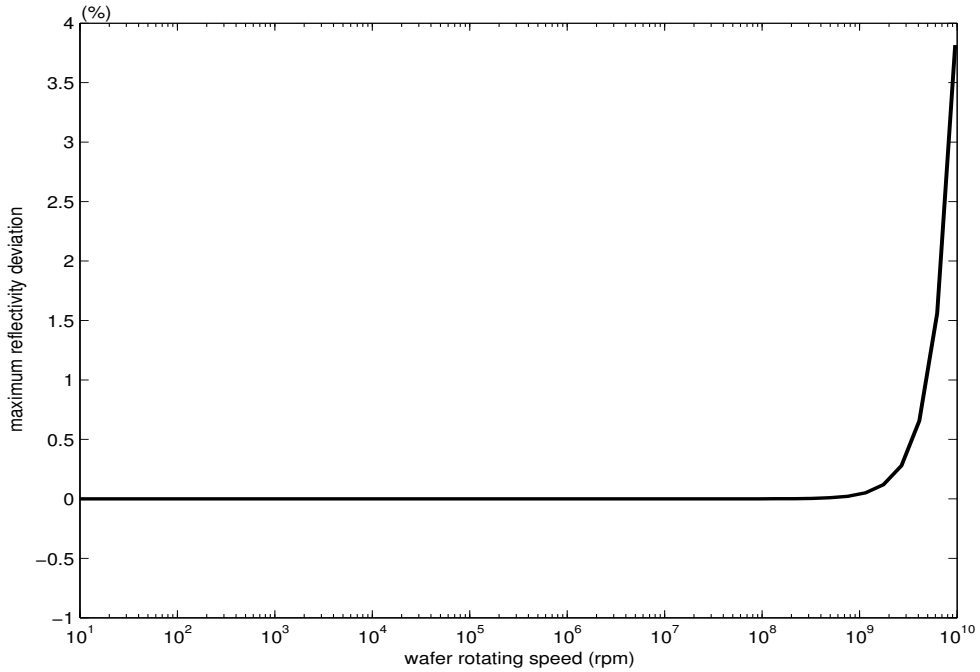

Figure 4.6. The calculated maximum reflectivity deviation in the spectrum of 450-850nm corresponding to different wafer rotating speed.(The incident light is normal to the wafer edge surface.)

Take an example of wafer rotating period $T_R = 6s$ and slider sliding period from wafer center to edge $T_{CE} = 1.3s$. It is the speed setting in our experiment. The maximum wafer moving speed is 0.13m/s for a 200mm wafer. From it, we can see the relative speed of wafer is incomparable to the light speed. Therefor, in our thickness estimation we can simplify Equation (4.2) to Equation (4.3).

4.4 Thickness estimation

The spectrometer is positioned above the wafer coated with a layer of photoresist to measure the resist thickness (Leang and Spanos, 1996). We can get the reflectance signals in the wavelength range from 450 nm to 850 nm. Photons at low wavelength will incur unwanted exposure at resist, so proper optical filter can be attached to eliminate low wavelength range.

After getting the reflectance signal, the resist thickness y can be derived from a

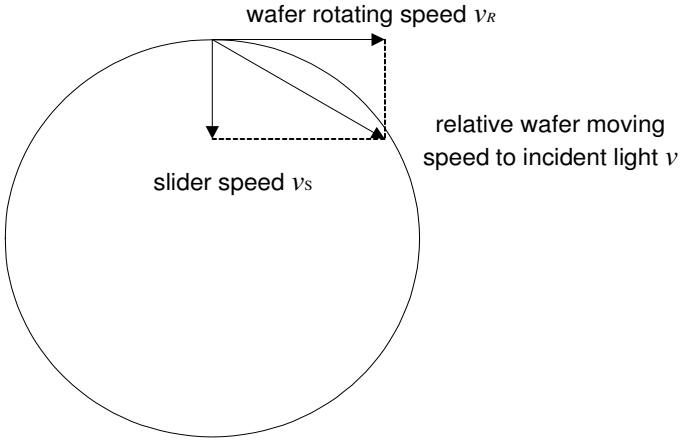

Figure 4.7. Calculation of relative wafer moving speed corresponding to incident light based on wafer rotating and sensor probe sliding

thin-film optical model. Based on discussion in previous section, at low speed, the spectral reflectivity curve can be approximated as the stationary curve. Consider a photoresist film with a refractive index of n_r. Its relation with the reflectance intensity is given in Equation (2.1). It is a function of both thickness y and extinction coefficient k. As discussed in Chapter 2, for the thickness estimation, high wavelength range is used so that the extinction coefficient is essentially zero. Then Equation (2.1) can be simplified as

$$h(\lambda, y) = \frac{r_{12}^2 + r_{23}^2 + 2r_{12}r_{23}cos(2\beta)}{1 + r_{12}^2 r_{23}^2 + 2r_{12}r_{23}cos(2\beta)} \tag{4.5}$$

where

$$r_{12} = \frac{n_a - n_r}{n_a + n_r} \qquad r_{23} = \frac{n_s - n_r}{n_s + n_r} \qquad \beta = \frac{2\pi n_r y}{\lambda}$$

and n_a, n_r and n_s are the refractive index of air, resist, and silicon substrate, respectively. Here the equation $r_{12} = \frac{n_a - n_r}{n_a + n_r}$ is equivalent with Equation (4.3), as the refractive index of air is 1. y is the resist thickness. The variation of the resist refractive index with wavelength λ is given by the Cauchy equation (Born and Wolf, 1980).

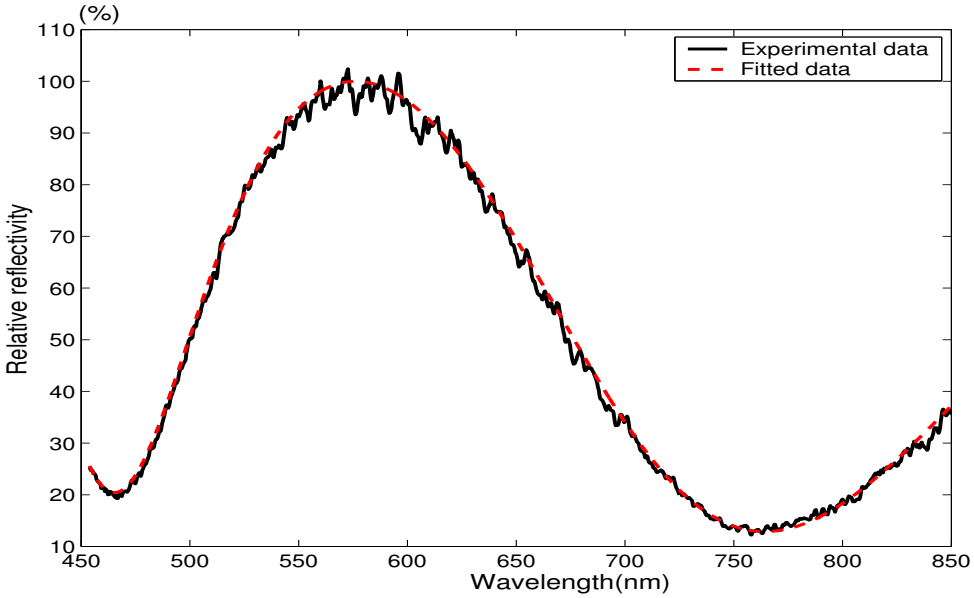

Figure 4.8. Fitting of experimental data with optical model. Solid line is the experimental data, while dash line is the theoretical data based on model.

Given the reflectance measurements, the resist thickness can be estimated using Equation (4.5). For a fairly repeatable process, we can give a good initial estimate of the thickness. To meet the demand of real-time monitoring, we use the least square estimation method to estimate the resist thickness (Lee *et al.*, 2002).

Equation (2.3) to Equation (2.5) is used for thickness estimation. To estimate the resist thickness, reflectance measurements were obtained at wavelength between 450 nm and 850 nm, about 0.35 nm apart. For this setup, a sample rate of 0.16s was used. Results from the optical model is compared with experimental data in Figure 4.8.

4.5 In-situ monitoring of thickness contour

Trajectory

The trajectory to monitor is decided by the combination of wafer spinning speed and spectrometer sliding speed. Denote T_R as the time for one revolution of the

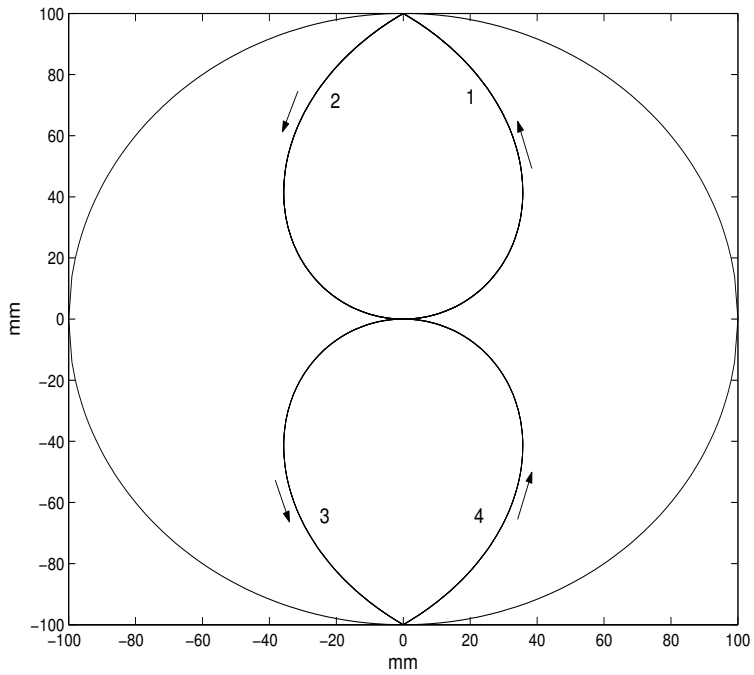

Figure 4.9. In the course of wafer rotating, the slider will also travel from origin to edge and reverse. This figure shows the actual sensor travelling trajectory on a 200mm wafer with a speed ratio of $\eta = 4$.

wafer and T_{CE} the time for the sensor probe to move from center to edge of the wafer or vice versa. Define the ratio of period as

$$\eta = \frac{T_R}{T_{CE}} \tag{4.6}$$

The ratio η decides the trajectory monitored on the wafer surface. For $\eta = 4$, the effective monitoring trajectory is shown in Figure 4.9. From this figure, we can see that using such a ratio, the monitoring coverage on the wafer is quite poor. In the experiments we set $T_R = 6$s, $T_{CE} = 1.3$s which gives $\eta = 4.5$. And the sampling time is set to be 0.16s . The monitoring trajectory is shown in Figure 4.10. The sensor probe will travel along the curved line from line 1 to line 18 and then repeat it. The points on the wafer with thickness readings are marked with asterisks, which are decided by the sampling time.

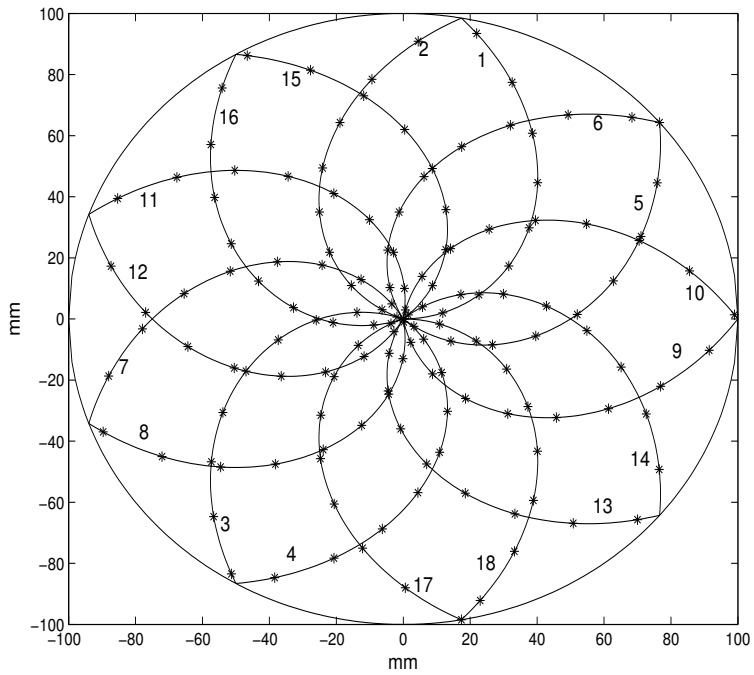

Figure 4.10. In the course of wafer rotating, the slider will also travel from origin to edge and reverse. This figures shows the actual sensor travelling trajectory on a 200mm wafer with a speed ratio of $\eta = 4.5$. Thicknesses are measured at the positions marked by "*".

Experimental result

An 8-inch wafer was coated with a layer of Shipley SL4000 photoresist. The sensor probe would start from the wafer origin and travel along the trajectory shown in Figure 4.10. The thickness data are recorded in the period of 4 rounds of wafer rotating. Based on the measurement and their positions shown in Figure 4.10, the resist thickness contour and the 3-D profile are obtained and they are shown in Figures 4.11 and 4.12. From the thickness profile, we would be able to evaluate the coating quality across the whole wafer. Statistical quality such as thickness mean and standard deviation can be calculated as well. For this test wafer, photoresist at the center was thicker than the edge. The statistical mean $\overline{y} = 371.45nm$ and standard deviation $\sigma = 9.25nm$. Based on these information, simple accept/reject action or advanced run-to-run control scheme can then be applied to improve the control of process. This in turn possibly leads to cost saving and manufacturing

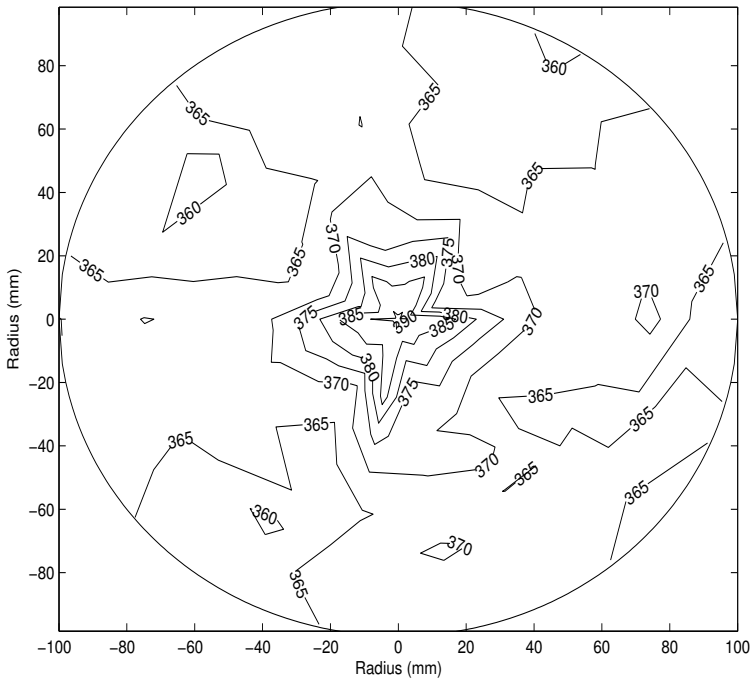

Figure 4.11. Resist thickness contour based on thickness measurements

performance improvement.

Comparison with off-line ellipsometer

The thickness measurements obtained from the experiments were compared with those from an off-line spectroscopic ellipsometer measurement. Ellipsometry is an optical technique devoted to the analysis of surfaces based on the measurement of the variation of the polarization state of the light after reflection on a plane surface. The thickness measurements from the ellipsometer are compared with those from the experiments.

Both single point measurement and statistical results are compared and good agreement between them is obtained. The comparison results are shown in Table 4.1. The positioning of P1, P2, P3, P4, P5 are shown in Figure 4.13. The worst-case percentage error is less than 1%. Further experiments on two more wafers gave a worst-case percentage error of less than 2%.

Table 4.1. Comparison of in-situ measurements with off-line ellipsometer measurements

	P1	P2	P3	P4	P5
Off-line Ellipsometer(nm)	390.29	363.51	366.74	364.12	366.48
In-situ measurement (nm)	389.12	365.07	365.38	364.95	363.53
Percentage error (%)	0.3	-0.4	0.4	-0.2	0.8

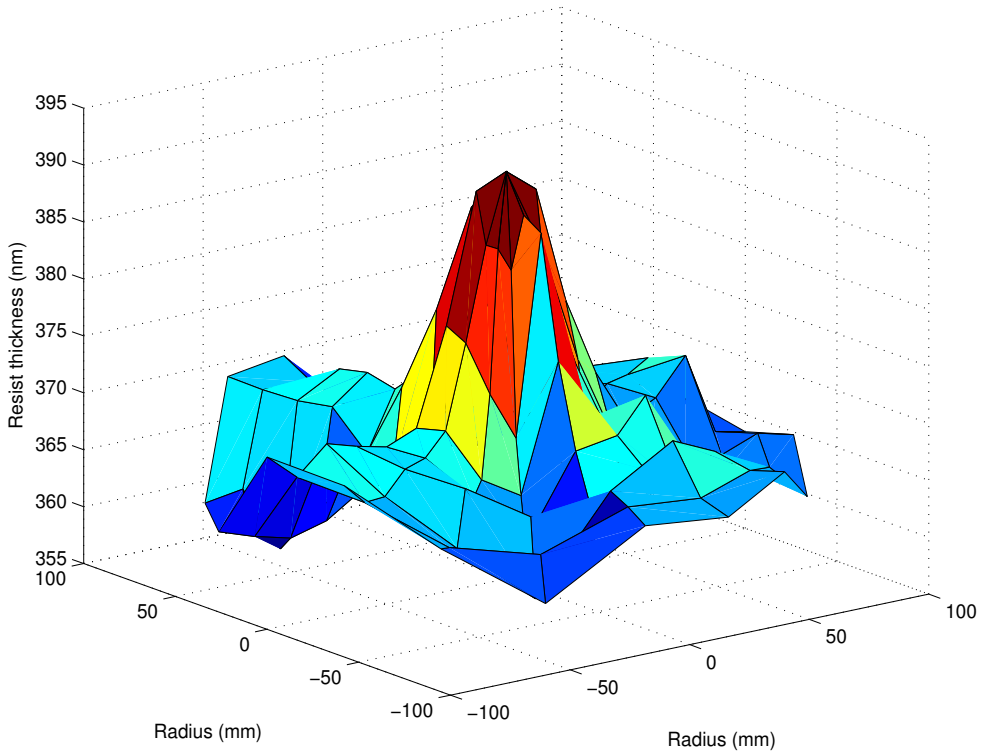

Figure 4.12. Resist thickness profile: 3-D representation.

4.6 Conclusion

In semiconductor manufacturing process, coating of photoresist is a common process. It is important to ensure the uniformity of the photoresist across the wafer. In this chapter, an in-situ monitoring system is developed for the modern lithography process. In the setup, a spectrometer was used to measure the photoresist thickness contour on the wafer in the spin-coat step or edge-bead removal step. The experimental results are compared with off-line ellipsometer measurements. The worst-case error was experimentally found to be less than 2%. Using the

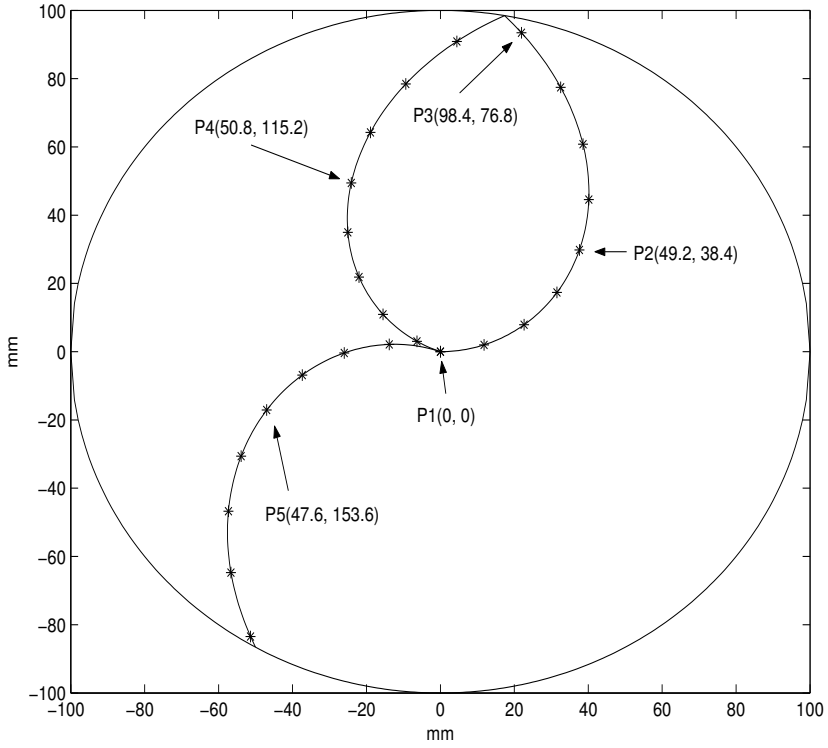

Figure 4.13. Five positions at the monitoring trajectory shown in Figure 4.10 are selected to be monitored by off-line ellipsometer to validate the accuracy of the dynamic measurement, which are P1-P5. The positions are given in polar coordinate (r, θ) in mm and degree, respectively.

resist contour information, advanced feedforward process control could be implemented to adjust the subsequent processes to compensate for the resist thickness non-uniformity

Chapter 5

A Lamp Thermoelectricity Based Integrated Bake/chill System for Photoresist Processing

5.1 Introduction

Thermal processing of semiconductor substrates through conductive heat transfer is common and critical to the lithography process as shown in Figure 1.1. Each thermal processing step involves baking the substrate to an elevated temperature for a given period of time, this is then usually followed by a chill step which is used to cool the wafer to an appropriate temperature for subsequent processing (Plummer *et al.*, 2000). Of these baking steps, the post-exposure bake step is the most sensitive to temperature variation for the current generation of chemically-amplified resists (CARs) (Parker and Renken, 1997). For such CARs, the temperature of the wafer during this thermal cycle has to be controlled to a high degree of precision both spatially and temporally (Sturtevant *et al.*, 1993; Seeger, 1997; Braun, 1998). For example, Sturtevant *et al.* (Sturtevant *et al.*, 1993) reported a 9% variation in the linewidth or critical dimension (CD) per 1% variation in temperature for

a deep ultraviolet (DUV) resist. A number of recent investigations also show the importance of proper bakeplate operation on CD control (Smith *et al.*, 2001; Steele *et al.*, 2002; Friedberg *et al.*, 2004).

According to the International Technology Roadmap for Semiconductors (ITRS, 2005), the post exposure bake (PEB) resist sensitivity to temperature will be ever more stringent for each new lithography generation (Parker and Renken, 1997). With a precise temperature control, existing resists can be used for future technology nodes. Although less temperature sensitive photoresist materials are desired, the requirements become more stringent as the feature size shrinks. Consequently, the temperature control system for this process requires careful consideration, including the equipment design and temperature sensing techniques. The application of mathematical systems science tools have seen increasing utilization in recent years to improve yields, throughput, and in some cases, to enable the actual process to print smaller devices (Edgar *et al.*, 2000; Kailath and Tay, 2001).

In the thermal processing of semiconductor substrate during lithography, the heated plate is usually thermally massive relative to the substrate (e.g. silicon wafer) and is held at a constant temperature by a feedback controller that adjusts the resistive heater power in response to a temperature sensor embedded in the plate near the surface. Because of its large thermal mass and resultant sluggish dynamics, conventional hotplates are robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Other disadvantages include uncontrolled and nonuniform temperature fluctuation during the mechanical transfer of the substrate from bake to chill plates (see Figure 1.2), spatial temperature nonuniformities during the entire thermal cycle, etc (El-Awady, 2000). This lack of a method to conduct real-time distributed, closed-loop temperature control with conventional hotplates is a source of process error in the lithography chain.

In this chapter, a new thermal processing system will be proposed for optimal processing of temperature-sensitive photoresist so as to address the above-mentioned issues. This development is motivated by the general inclination to improve the capabilities of conventional hotplates through advanced control algorithms alone. Although some improvements are possible (Ho *et al.*, 2000; Tay *et al.*, 2001; Tay *et al.*, 2004*b*), we conclude that the conventional hotplate design has poor controllability (Skogestad and Postlethwaite, 1996) that ultimately limits the achievable performance. Our proposed system comprises of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide spatial and temporal temperature uniformity control and active cooling. The proposed system offers excellent temperature control during the entire thermal cycle, eliminates substrate movement during the baking and chilling processes, and accommodates *in situ* temperature measurement for real-time control. The feasibility of the proposed approach is demonstrated via detailed simulations based on first principle heat transfer modelling. Other unique applications are rendered possible because of the rapid response, and real-time sensing capabilities exhibited by this thermal processing technology. For example, our method offers an elegant solution to the bake-chill transition in an oxygen free environment commonly encountered in copper annealing. Other demanding applications include thermal control of spin-on dielectrics or low-k materials.

My main contributions in this work is summarized as follows. The existing wafer thermal modelling assumes that the wafer is an opaque object with a constant emissivity across whole spectral range. Original contributions have been made to account for spectral optical properties of wafer in the simulation. It is a more accurate modelling method. Based on it, new modelling of radiation absorption by translucent silicon wafer is proposed and implemented. A simple modelling of spiral wafer chiller is also presented. It applies counterflow Archimedes' spiral design and high water flow rate is maintained to simplify thermal modelling. Decentralized

control structures are proposed without going into more advanced multivariable controllers.

5.2 Proposed thermal processing module

Efforts in addressing some of these issues discussed in section (3.1) have been ongoing by some research groups around the world (El-Awady *et al.*, 1999; Schaper *et al.*, 1999; El-Awady *et al.*, 2003; Tay *et al.*, 2004*a*). A fluid-heat-exchanger based thermal cycling module was earlier developed (El-Awady *et al.*, 1999; El-Awady *et al.*, 2003). The heat-exchanger module provides thermal cycling by alternating between hot and cold fluids. Spatial and temporal control were provided by auxiliary heaters in the form of thermoelectric devices (El-Awady *et al.*, 1999) and a multizone etched foil heater (El-Awady *et al.*, 2003). Both methods, while having a much lower "thermal mass" than conventional units, still require large amounts of power for thermal cycling. The use of fluids for bulk heating is costly, and the presence of hot fluids in the system represents a safety hazard. The etched foil heater units also deflect during cyclings and thus raising the question of long term reliability. A considerable improvement was achieved in a spatially programmable module using an array of cartridge heaters developed by Kailath's group in Stanford (Schaper *et al.*, 1999) and subsequently commercialized. This system is excellent for processing substrates but without modification, it may not be able to achieve fast enough ramp-down rates during a thermal cycling operation. In addition, all of the above approaches lack the capability to conduct real-time temperature control on the substrate. A notable exception is the recent work (Tay *et al.*, 2004*a*) featuring a thermal cycling module integrated with *in situ* measurement of substrate temperature.

Because resist processing steps are thermally activated, a performance specification is required to take into account nonuniformities during the transient and steady

state (El-Awady, 2000). This indicates that the ability to create any arbitrary temperature profile is highly desirable and one approach is to have a system that can provide extremely fast ramp-up and ramp-down rates. One attractive solution is the use of a lamp-based heating method which is common in rapid thermal processing (RTP). In RTP, intense radiation is used to heat the wafer to temperatures over 700^{o}C for annealing and oxidizing the wafer. As in photoresist processing, it is important in RTP to maintain temperature uniformity, although the temperature requirement is not as stringent as in photoresist processing. In RTP, active cooling is usually not available, chilling is typically achieved by turning off the lamps. In this chapter, we propose to make use of this radiant heating technology coupled with TEDs to provide for both active heating and cooling. The proposed method for photoresist processing will also be suitable for low-temperature RTP processes. Constructing such a prototype would be cost-prohibitive as energetic efficiency mandates a gold coated chamber; instead we present a detailed simulation of the system based on first principle thermal modelling.

A schematic of the proposed thermal processing module is shown in Figure 5.1. The system consists of a heating chamber with three annuli of tungsten halogen lamp arrays. Energy is radiated through a quartz window of the lamps onto a semiconductor substrate either directly or via reflections from the chamber walls. This lamp structure design is an offshoot of the Stanford RTP system design (Norman, 1992). The power ratings of lamps are kept sufficiently high to prevent saturation during the thermal cycle. The exact capacities of the lamps will depend on the configuration of the lamp structure/placement. To achieve optimal temperature uniformity, the output heat flux profile of each zone can be optimized based on the lamp positions and size (Cho *et al.*, 1994). Suitable filters are used to prevent the photoresist from being exposed to UV irradiation during the post-exposure bake step in lithography.

The substrate sits on an array of proximity pins approximately 5 mils above the

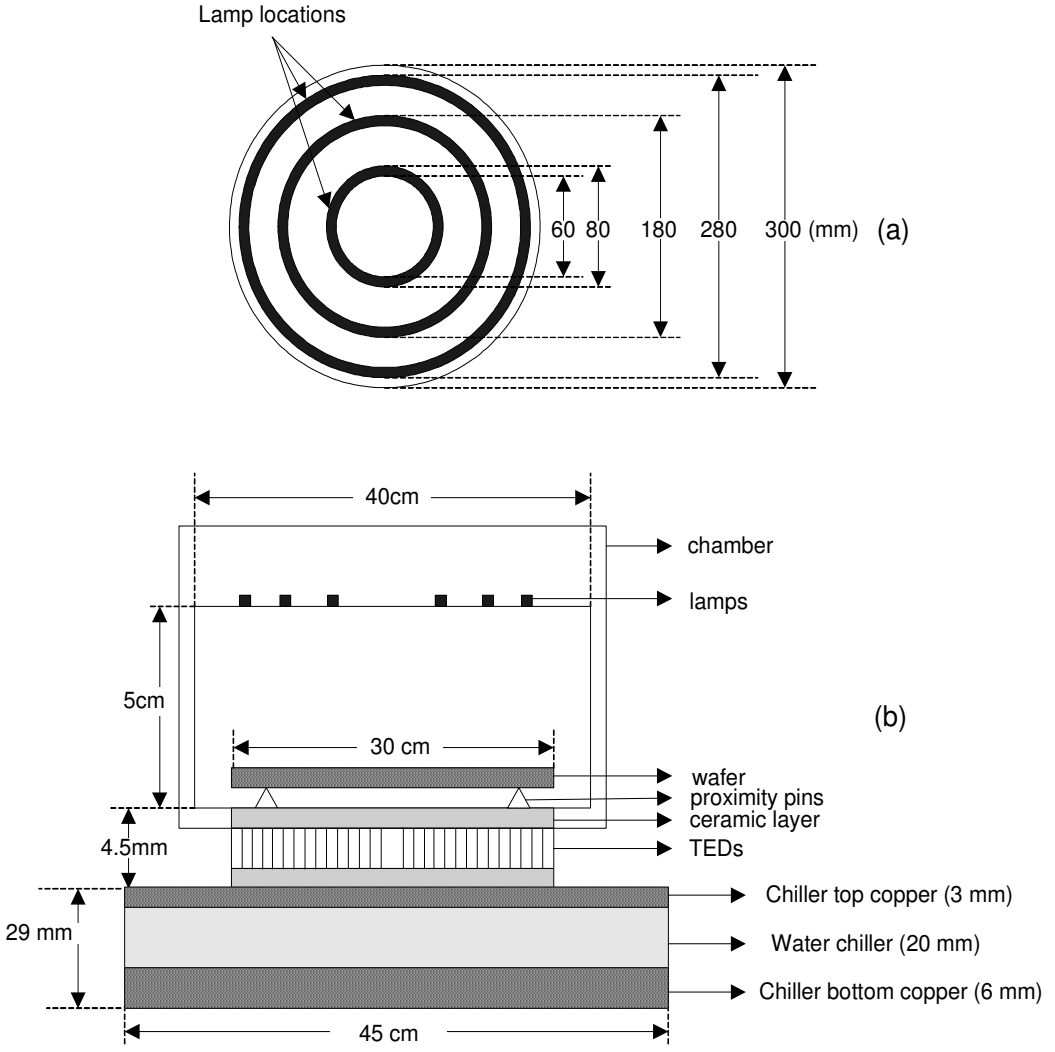

Figure 5.1. Schematic diagram of the integrated bake/chill design. (a) is the top view of lamp locations; (b) is the cross section of whole designed system.(Note: Figure not drawn to scale.)

ceramic. These proximity pins can be embedded with temperature sensors (*Surface temperature measurement*, 2004) (with an accuracy of $\pm 0.5^{o}$C and 25 ms response time) to provide in situ temperature measurement. Proximity baking is the preferred method in the industry compared to contact baking due to contamination issues. The bismuth telluride thermoelectric devices (TEDs) provide real time dynamic and spatial control of the substrate temperature. The TEDs sit on top of a chiller (see Figure 5.1) and together form the cooling mechanism. The TEDs are assembled such that they can be controlled independently as separate annular zones. Annular TEDs, although not common, can be custom made.

A typical heat-and-chill cycle would proceed as follows. The whole system, with the substrate sitting inside, starts at around room temperature. During the baking process, the lamps will be switched on and progressively heat up the wafer. The gold coated chamber, characterized with a very low emissivity facilitates the heating up of the wafer. During the baking process, the various zones of TEDs will be separately and judiciously energized to maintain temperature uniformity throughout the wafer. Depending on the polarities applied to the TEDs, they can operate in either heating or cooling mode. This makes them excellent regulating devices. Chilling is achieved by switching off the lamps and dictating the TEDs to provide active cooling and maintaining temperature uniformity. The chiller unit consisting of cold circulating water (or fluid) serves as the dominant means for heat dissipation. As shown in Figure 5.1, the chiller is designed to provide uniform temperature across the chiller surface.

5.3 Thermal modelling

In order to ascertain the performance of the proposed design, a mathematical model is developed for the integrated bake/chill operation. We assume that the substrate is a silicon wafer and adopt an axisymmetrical cylindrical coordinate system. Fig-

ure 5.1 presents the main sections of the system including the annular lamp arrays, wafer, TEDs and heat sink. We will subsequently consider the complete optical properties of a silicon wafer and the governing equations for the major system components.

Lamp design considerations

The lamp system consists of three annular lamps arrays as shown in Figure 5.1. The encapsulation of the tungsten filaments by a quartz envelope dictates that no radiation beyond 4 μm (Timans, 1996) wavelength from the filament will be transmitted through the envelope. In addition, a typical glass filter (Lot Oriel, 2005) is employed to prevent resist exposure to wavelengths below 500 nm. A host of glass filters with different cutoff wavelengths (Lot Oriel, 2005) is available to cater to most types of photoresist.

Since it takes a finite time to heat up the tungsten filaments, the thermal mass of these lamps have to be considered. Our quartz tungsten halogen lamps are from Oriel Model No. 6337 (*Quartz Tungsten Halogen Lamps*, 2004). Based on the data sheet provided therefrom, the thermal mass of each of the annular lamp arrays is computed and tabulated in Table 5.1.

Thermal radiative properties of silicon wafer

It is considered that the chamber walls are diffuse, opaque and gray and the lamp zones gray and Lambertian. For our temperature regime, the silicon wafer is translucent (INSPEC, 1988), so that its various spectral optical properties have to be taken into account. The range of wavelengths between 500 nm to 4μm sufficiently encompasses the domain of radiative interaction of our application. The spectral emissivity, ϵ_λ, of silicon wafer can be computed as follows (Sato, 1967;

Timans, 1996).

$$\epsilon_\lambda = \frac{(1-R_\lambda)(1-T_\lambda)}{1-R_\lambda T_\lambda} \tag{5.1}$$

$$R_\lambda = \frac{(n_{si,\lambda}-n_{air})^2+k_{si,\lambda}^2}{(n_{si,\lambda}+n_{air})^2+k_{si,\lambda}^2} \tag{5.2}$$

$$T_\lambda = \exp(-\kappa_\lambda z) \tag{5.3}$$

$$\kappa_\lambda = \frac{4\pi k_{si,\lambda}}{\lambda} \tag{5.4}$$

where R_λ, T_λ are the reflectivity and transmissivity respectively and n: refractive index, k: extinction coefficient, κ: absorption coefficient, λ: wavelength, z: thickness of wafer, si: silicon, and, air: air.

The silicon spectral absorption coefficient, κ_λ, and refractive index, n, can in turn be computed as a function of wavelength and temperature (Timans, 1996). For photoresist processing, the wafer is usually at a processing temperature of about 100 ^{o}C (Parker and Renken, 1997) most of the time. As such, all computation of the various optical properties are done at 100 ^{o}C. From the room temperature to 100 C, their variations with respect to temperature are very minor. Figure 5.2 shows the spectral emissivity for a standard 300 mm wafer of thickness 675 μm; the emissivity is essentially zero after 1.3 μm.

In addition to the spectral emissivity, the apparent reflectivity, ρ_λ, and transmissivity, τ_λ, are also important for the computation of the various surface radiosities in the system. The apparent reflectivity and transmissivity consider reflections from both the top and bottom surfaces of the wafer and treat them as effective surface phenomena. Invoking the Kirchhoff's law (Sato, 1967), the following relationship holds:

$$\epsilon_\lambda + \rho_\lambda + \tau_\lambda = 1$$

where

$$\rho_\lambda = R_\lambda\left[1+\frac{T_\lambda^2(1-R_\lambda)^2}{1-R_\lambda^2T_\lambda^2}\right], \qquad \tau_\lambda = T_\lambda\frac{(1-R_\lambda)^2}{1-R_\lambda^2T_\lambda^2}.$$

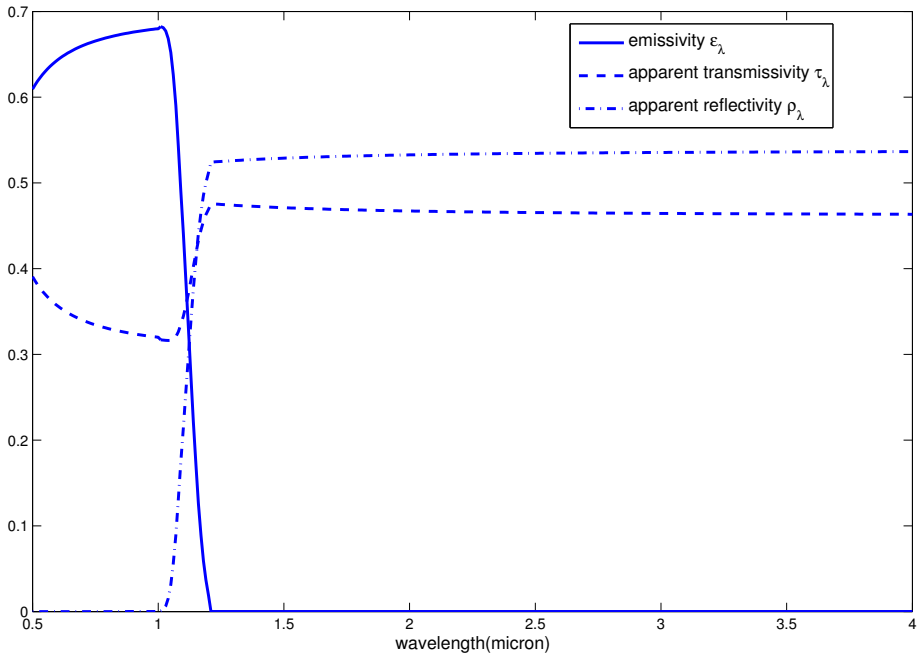

Figure 5.2. Spectral emissivity, apparent transmissivity and apparent reflectivity of a silicon wafer at a temperature of 373 K. The wafer is 300 mm in diameter and 675 μm thick.

The apparent reflectivity and transmissivity are also shown in Figure 5.2.

Heat transfer in wafer

The wafer is assumed to be cylindrical with a diameter D, thickness Z and negligible thermal expansivity. The wafer temperature is also assumed to be uniform in the axial z direction as the wafer is thin. The wafer is discretized and for each discrete wafer element, the following diffusion equation holds.

$$\dot{T}_{wafer,i} = \frac{1}{\rho v_i c_p} \left(\frac{k v_i}{r} \frac{\partial}{\partial r} \left(r \frac{\partial T_{wafer,i}}{\partial r} \right) + q_i \right) \tag{5.5}$$

where r is the radial direction, v_i is the volume of the element i, and q_i the net heat input per unit volume into each wafer element embodying radiative and convective losses from the wafer element, radiative absorption by the wafer element and conductive heat transfer from the TEDs.

A finite difference scheme is employed for our numerical computation. The wafer is discretized into 15 zones (1 circular and 14 annular elements). The edge of the wafer is taken into account when we compute for the radiative interaction. The TEDs will also be arranged into 15 zones similar to the wafer. Such circular and annular TEDs can be custom made. For the same purpose, the chamber ceiling is divided into 20 zones comprising 1 circular zone and 19 annular zones. Some of these zones are used to represent the annular lamp arrays. The outer radius of each zone increases uniformly from the center zone to the edge zone. The portion of the chamber sidewall between the wafer bottom surface and the chamber ceiling is divided into 5 equal zones. The annular region between the wafer bottom surface and the chamber bottom surface is treated as one zone. The remaining floor of the chamber (including the the ceramic surface of the TEDs) is divided into 20 zones corresponding to the ceiling. The radii of the annuli increase uniformly from the center zone to the edge zone. The system dimensions are shown in Figure 5.1.

During the wafer heat transferring modelling the effect of photoresist on wafer surface is neglected since the resist thickness is very small comparing to the wafer thickness. Typical resist thickness is 1 um while wafer thickness is 675um.

The net heat transfer q_i into each wafer element i is taken as the sum of the following terms

$$q_i = q_i^{em} + q_i^{abs} + q_i^{cond} + q_i^{conv} \tag{5.6}$$

with each term explained below.

1. Radiation emitted by wafer element i, q_i^{em}:

   The radiation emitted by hot objects has a spectral distribution related to the Planck's distribution (Levy, 1989). For the wavelength range of interest, the radiation emitted by wafer element, i, denoted by q_i^{em} is given by

   $$q_i^{em} = -\int_i \int_0^{\infty} \varepsilon_\lambda \frac{C_1 \lambda^{-5}}{exp(\frac{C_2}{\lambda T}) - 1} d\lambda dA_i \tag{5.7}$$

   where $C_1 = 3.7403 \times 10^8$ W$\cdot\mu m^4/m^2$ and $C_2 = 1.4387 \times 10^4 \mu$m$\cdot$K.

2. Radiation absorbed by wafer element i, q_i^{abs}:

   The main sources of radiative energy in the proposed system with which the wafer elements interact are the lamps and gold-coated chamber. For this purpose, the whole system is divided into $N = 77$ zones. The radiation absorbed by element i of the wafer can be expressed as follows

   $$q_i^{abs} = \int_{0.5}^{4} (1 - \rho_\lambda - \tau_\lambda) \sum_{j=1, j\neq i}^{N} F_{ji} A_j J_{j,\lambda} d\lambda \tag{5.8}$$

   where $J_{j,\lambda}$, A_j and F_{ji} are respectively the spectral radiosity between zone j and wafer element i, the surface area of zone j and the view factor (Norman, 1992) between each zone. The view-factor model used here is adapted from those of Norman (Norman, 1992) and Lord. (Lord, 1988) which exhibit good

agreement between simulation results and experimental data. (Lord, 1988; Campbell *et al.*, 1991; Apte and Saraswat, 1992)

The spectral radiosity of each surface element i is denoted as $J_{i,\lambda}$ and given by

$$\begin{aligned}
J_{lamp,i,\lambda}(t) &= \epsilon_{lamp,\lambda} E_{b,\lambda}\left(T_{lamp}(t)\right) + \rho_{lamp,\lambda} \frac{1}{A_{lamp}} \sum_{j=1}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{gold,i,\lambda}(t) &= \epsilon_{gold,\lambda} E_{b,\lambda}(T_{gold}(t)) + \rho_{gold,\lambda} \frac{1}{A_{gold}} \sum_{j=1}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{wafer,i,\lambda}(t) &= \epsilon_{wafer,\lambda} E_{b,\lambda}(T_{wafer}(t)) + \rho_{wafer,\lambda} \frac{1}{A_{wafer}} \sum_{j \neq wafer,TED}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{TED,i,\lambda}(t) &= \tau_{w,\lambda} \epsilon_{TED,\lambda} E_{b,\lambda}(T_{TED}(t)) \\
&\quad + \tau_{w,\lambda} \rho_{TED,\lambda} \tau_{wafer,\lambda} \frac{1}{A_{TED}} \sum_{j \neq wafer,TED}^{N} F_{ji} A_j J_{j,\lambda}
\end{aligned}$$

where $lamp, gold, wafer$ and TED denote the lamp, gold-coated chamber, wafer and ceramic respectively. $E_{b,\lambda}(T(t))$ is the spectral blackbody emission which is a function of temperature.

There are a total of N discrete surfaces with N linear equations. At every time instant, these surface radiosities can be computed algebraically and then Equation (5.8) can be computed accordingly.

3. Conductive heat transfer from the TEDs into wafer element i, q_i^{cond}:

   The air gap between the wafer and TEDs is 5 mils. Since this gap is much less than 5.8 mm, and their temperature difference considerably smaller than 200^{o}C. (Hollands *et al.*, 1975), the heat transfer mechanism is essentially conductive and given by

$$q_z^{cond} = \frac{T_i - T_{air,i}}{L_{wafer}/2k_{wafer} + L_{air}/2k_{air}} \tag{5.9}$$

where A_z is the cross sectional area between wafer element i and the corresponding air gap.

The governing thermal equation for the air gap is given by

$$\begin{aligned}\rho c_p V_i \frac{dT_{air,i}}{dt} &= \frac{k}{r} V_i \frac{\partial}{\partial r}\left(r \frac{\partial T_{air,i}}{\partial r}\right) + \frac{T_{ce,i} - T_{air,i}}{L_{ce}/(2k_{ce}A_i) + L_{air}/(2k_{air}A_i)} \\ &\quad + \frac{T_{wafer,i} - T_{air,i}}{L_{wafer}/(2k_{wafer}A_i) + L_{air}/(2k_{air}A_i)} \end{aligned} \tag{5.10}$$

with the following boundary conditions

$$\begin{aligned}\left.\frac{\partial T_{i,air}}{\partial r}\right|_{r=0} &= 0 \\ -k\left.\frac{\partial T_{i,air}}{\partial r}\right|_{r=D/2} &= h(T_{air,i} - T_\infty)\end{aligned}$$

where V_i is the volume of air between wafer and TED elements i, and L_{cera}, L_{air} and L_{wafer} are the thicknesses of the TED ceramic, air gap and wafer respectively.

4. Convective heat transfer into wafer element i, q_i^{conv}:

   The convective heat transfer between each element i of the wafer and the surrounding air is given by

$$q_i^{conv} = -h_i A_i \left(T_{wafer,i} - T_\infty\right) \tag{5.11}$$

   where h_i is the area-weighted average convective heat transfer coefficient over the exposed surface area A_i of element i and T_{air} is the air temperature. T_∞ is the temperature of air in the chamber.

Heat is also transferred from the chamber to the air by convection. The equation

for the convection term q_{cham}^{conv} is given by

$$q_{cham}^{conv} = hA_{cham}\left(T_{cham} - T_{\infty}\right) \tag{5.12}$$

where A_{cham} is the internal surface of the chamber in contact with the air.

We note that in most practical radiative systems, some surfaces reflect specularly and others reflect diffusely. A rigorous calculation of the radiative heat transfer in the system demands the use of ray-tracing techniques (Modest, 2003), and entails a large programming effort as well as computing effort. Nevertheless, the present formalism has been found to yield good agreements with experimental data (Lord, 1988; Campbell *et al.*, 1991; Apte and Saraswat, 1992).

Thermoelectric devices (TEDs) modelling

The Peltier, Thomson and Joulean effects are the governing principles of thermoelectricity. For bismuth telluride, the Thomson effect is negligible (Chua *et al.*, 2002). Consequently the governing thermal transport equation in the semiconductor arms is given by (Rowe, 1994)

$$\rho_t c_{p,t}\frac{\partial T_t}{\partial t} = k_t\frac{\partial^2 T_t}{\partial z_t^2} + \frac{J^2}{\sigma_t} \tag{5.13}$$

where T is the temperature, k the thermal conductivity, ρ the density, c_p the specific heat capacity, σ the electrical conductivity, $J(= I/A)$ the current flux where I and A are respectively the direct current flowing through the TEDs and the cross-sectional area. The subscript, t, denotes the thermoelectric modules.

The Peltier effect is manifested at the boundary between the TED's metal contacts and the thermoelectric elements. It is given by

$$k_t A_t\frac{\partial T_t}{\partial z_t} + k_m A_m\frac{\partial T_m}{\partial z_m} \pm \alpha I T_b = 0 \tag{5.14}$$

where α is the Seebeck coefficient. The subscripts m and b denote the metal film in the TEDs and the interface between the metal contact and semiconductor respectively. The first two terms denote the thermal conduction into the interfacial layer while the last term represents the Peltier effect at the boundary. The sign in the last term in Equation (5.14) is positive during heating mode and negative during chilling mode. The thermal transport phenomenon in the metal film element is similarly expressed as

$$\rho_m c_{p,m} \frac{\partial T_m}{\partial t} = k_m \frac{\partial^2 T_m}{\partial z_m^2} + \frac{J^2}{\sigma_m} \tag{5.15}$$

The metal film is sandwiched between the thermoelectric elements and the ceramic substrates. Perfect contacts are assumed for all the interfaces. The equation describing the interface between the metal film and ceramic substrate is expressed as

$$-k_m A_m \frac{\partial T_m}{\partial z_m}\bigg|_{boundary} = -k_{ce} A_{ce} \frac{\partial T_{ce}}{\partial z_{ce}}\bigg|_{boundary} \tag{5.16}$$

The governing thermal transport equation of the ceramic substrate is

$$\rho_{ce} c_{p,ce} \frac{\partial T_{ce}}{\partial t} = k_{ce} \frac{\partial^2 T_{ce}}{\partial z_{ce}^2} \tag{5.17}$$

where the subscript ce denotes the ceramic substrate.

Additional boundary conditions are required for (i) the interface between the ceramic substrate and the chiller and (ii) the top ceramic plate facing the air-gap:

$$\begin{aligned} -k_{ce} A_{ce} \frac{\partial T_{ce}}{\partial z_{ce}}\bigg|_{boundary} &= -k_{cop1} A_{cop1} \frac{\partial T_{cop1}}{\partial x_{cop1}}\bigg|_{boundary} \\ -k_{ce} A_{ce} \frac{\partial T_{ce}}{\partial z_{ce}}\bigg|_{boundary} &= \frac{T_{ce,b} - T_{i,air}}{R_a} + J_{TED,\lambda}(t) - \tau_{wafer,\lambda} G_{i \neq wafer,TED} \end{aligned}$$

The subscript $cop1$ denotes the top layer of the chiller (copper) and $G_{i \neq wafer,TED}$ denotes the irradiation of element i. R_a is the thermal resistance between the air

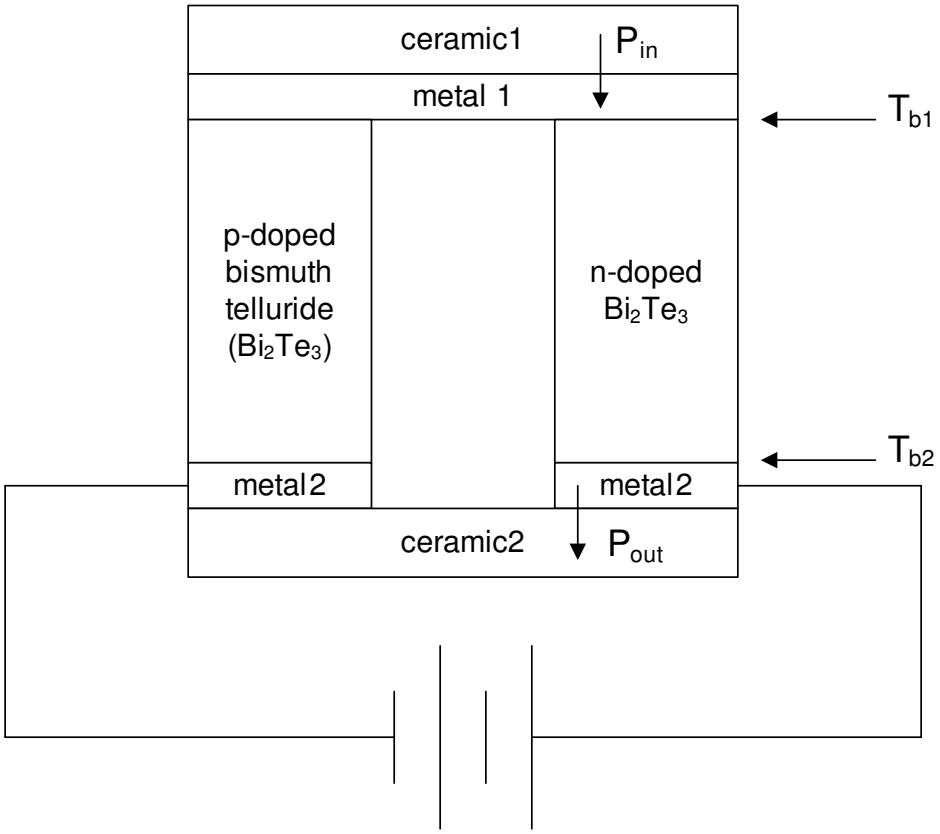

Figure 5.3. Schematic diagram of a TED element. (Note: Figure not drawn to scale.)

gap and ceramic substrate element.

Finally, to compute the power consumption by each TED zone, consider the simplified schematic of a TED in Figure 5.3. The electricity power consumed by each TED zone can be computed via an energy balance as

$$P_{electricity} = [P_{out} - P_{in} + \Delta P + 2\alpha \times I \times (T_{b1} - T_{b2})]\, N \tag{5.18}$$

where $P_{out} = -k_m A_m \frac{\partial T_{m2}}{\partial z_{m2}}$ is the energy transferred from metal2 to ceramic2; $P_{in} = -k_{ce} A_{ce} \frac{\partial T_{ce1}}{\partial z_{ce1}}$ the energy transferred from ceramic1 to metal1; $\Delta P = \sum \rho_i v_i c_{p,i} \frac{\partial T_i}{\partial t}$ the internal power change, i stands for metal1, metal2 or TED; N is the number of pairs of TED arms in a particular zone; α the Seebeck coefficient; I the TED current and T_{b1}, T_{b2} are the respective metal-ceramic boundary temperatures.

Design of water chiller

During the cooling process, heat absorbed at the cold junction of TEDs is pumped to the hot junction. At the hot junction, the energy absorbed is dissipated via the chiller. Figure 5.4 shows the schematic of the water chiller. The chiller is made of copper. The top layer is 3 mm thick while the bottom layer is 6 mm thick, as a tunnel is dug inside to facilitate circulation of water. The dimension of the cross section of water vessel is $20mm \times 20mm$. The counterflow Archimedes' spiral design for the copper based chiller effectively ensures spatial temperature homogeneity throughout the region which is in contact with the TED array. Note that the incoming chilled water converges at the center of the spiral heat exchanger which then spirally radiates out again via the adjoining outgoing channel; also referring to Figure 5.4 the chiller has been deliberately oversized to weed out any end effects on the TED array.

To provide efficient heat dissipation, turbulent water flow inside chiller has to be maintained which requires the Reynolds number to be always higher than 3000 in the simulation. An initial water flow rate 0.15kg/s is accordingly applied which corresponds to a Reynolds number of 7500. To avoid mathematical complexity, it is assumed that the temperature within the chiller is uniform, which is given as T_{chi}. The energy balance equation of the chiller is given as

$$c_{p,chi} m_{chi} \frac{dT_{chi}}{dt} = hA(T_{cop1} - T_{chi}) + hA(T_{cop2} - T_{chi}) - \dot{m} c_{p,water}(T_{chi} - T_{in,water}) \tag{5.19}$$

where the subscript *chi* denotes the chiller; T_{cop1} and T_{cop2} are respectively temperatures of chiller top and bottom copper layer; A the water contact area with top and bottom copper layer; $\dot{m}$ the mass flow rate of the cooling water; $T_{in,water} = 20^oC$ is the temperature of water at the inlet of the chiller and the convective heat

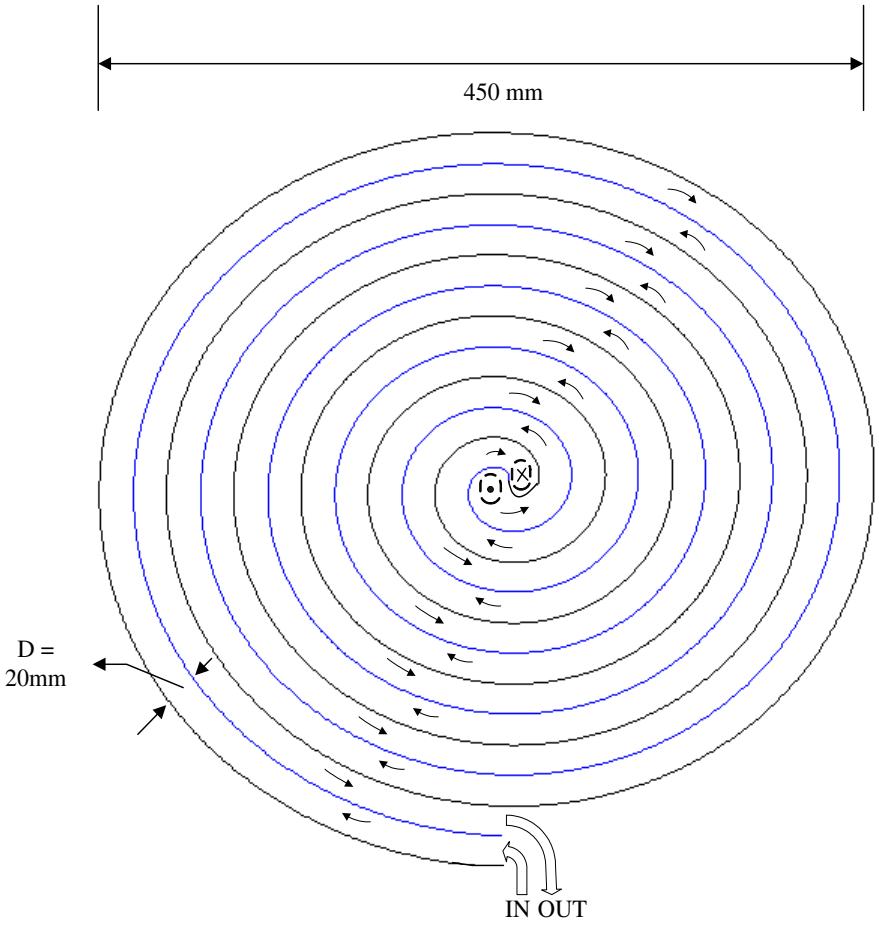

Figure 5.4. Top view of wafer chiller

coefficient, h, can be calculated from (Incropera and DeWitt, 2002)

$$\begin{aligned} f &= (0.79ln(Re) - 1.64)^{-2} \\ Nu &= \frac{(f/8)(Re - 1000)Pr}{1 + 1.27(f/8)^{1/2}(Pr^{2/3} - 1)} \end{aligned}$$

A standard Proportional-Integral-Derivative (PID) controller is used to control the chiller flow rate so as to maintain the chiller temperature at a desired level. For our simulation, the chiller setpoint is set equal to the water temperature at the inlet of the chiller. The PID controller is of the following form

$$u(t) = K_{ci}\left(e(t) + \frac{1}{T_{Ii}}\int e(t)dt + T_{di}\frac{de(t)}{dt}\right) \tag{5.20}$$

where K_{ci}, T_{Ti} and T_{di} are the controller parameters; $u(t)$ and $e(t)$ are respectively the control signal to the valve controlling the water flow rate and the error between the desired and actual water temperatures.

5.4 Control and simulation results

Simulations were carried out to assess the performance of the proposed lamp-TEDs thermal processing system. The objective is to demonstrate that the proposed design is able to maintain temperature uniformity during the entire thermal cycling process. It will be demonstrated that because of the decoupled nature of the system design, simple decentralized controllers can be used for this system without going into more advanced multivariable controllers. The lamps will be used to provide the bulk heating while the TEDs are used to address the nonuniformity problem between the different zones. During chilling, the lamps are turned off and the TEDs are used to minimize the temperature nonuniformity. For simplicity, the lamp portion of the system is treated as a single input system, i.e., one control

signal is sent to the three zones of lamps. Table 5.1 shows the thermophysical properties of the parameters (Rowe, 1994; Raznjevic, 1976) used in the simulation.

In the simulation, two sets of temperature are of interest, namely the real and measured temperatures of the wafer. The model of the temperature sensor is given as

$$\frac{dT_{\text{measured}}}{dt} = \frac{1}{\tau}\left(T_{\text{real}} - T_{\text{measured}}\right) \tag{5.21}$$

where τ is the time constant of the temperature sensor; for the temperature sensors modelled, $\tau = 25$ ms. For the simulation, a sampling time of 0.1 s is used.

We first analyze the capability of the lamp system without the TEDs. Figure 5.5 shows the wafer temperature responses at 15 equally spaced measurement sites along the radius of a 300 mm wafer during a thermal cycle. The feedback system is set up with a simple PID controller where the feedback temperature stems from the center of the wafer. The same control signal generated by the PID controller is sent to the three different lamp zones. It is thus a single-input-single-output system design (Skogestad and Postlethwaite, 1996). Notice that the peak temperature non-uniformity is about 2.7 ^{o}C during the transient period; a slight improvement could be obtained by feeding back other spatial wafer temperature points. An alternative and improved control approach is to make use of the multizone nature of the lamp system. Since the lamp system consists of three zones, three wafer temperature measurements directly below each of the lamp locations provide feedback to the respective lamp controllers. Figure 5.6 demonstrates the temperature response of the 3-zone setup. Notice that the peak temperature non-uniformity has dropped to about 0.7 ^{o}C. Again other wafer temperature locations can be chosen for feedback, however the improvement is limited.

We now investigate the use of the TEDs to regulate and improve the spatial temperature uniformity. Closed-loop control using the 15-zone system was configured as shown in Figure 5.7. The innermost zone causes the wafer center tempera-

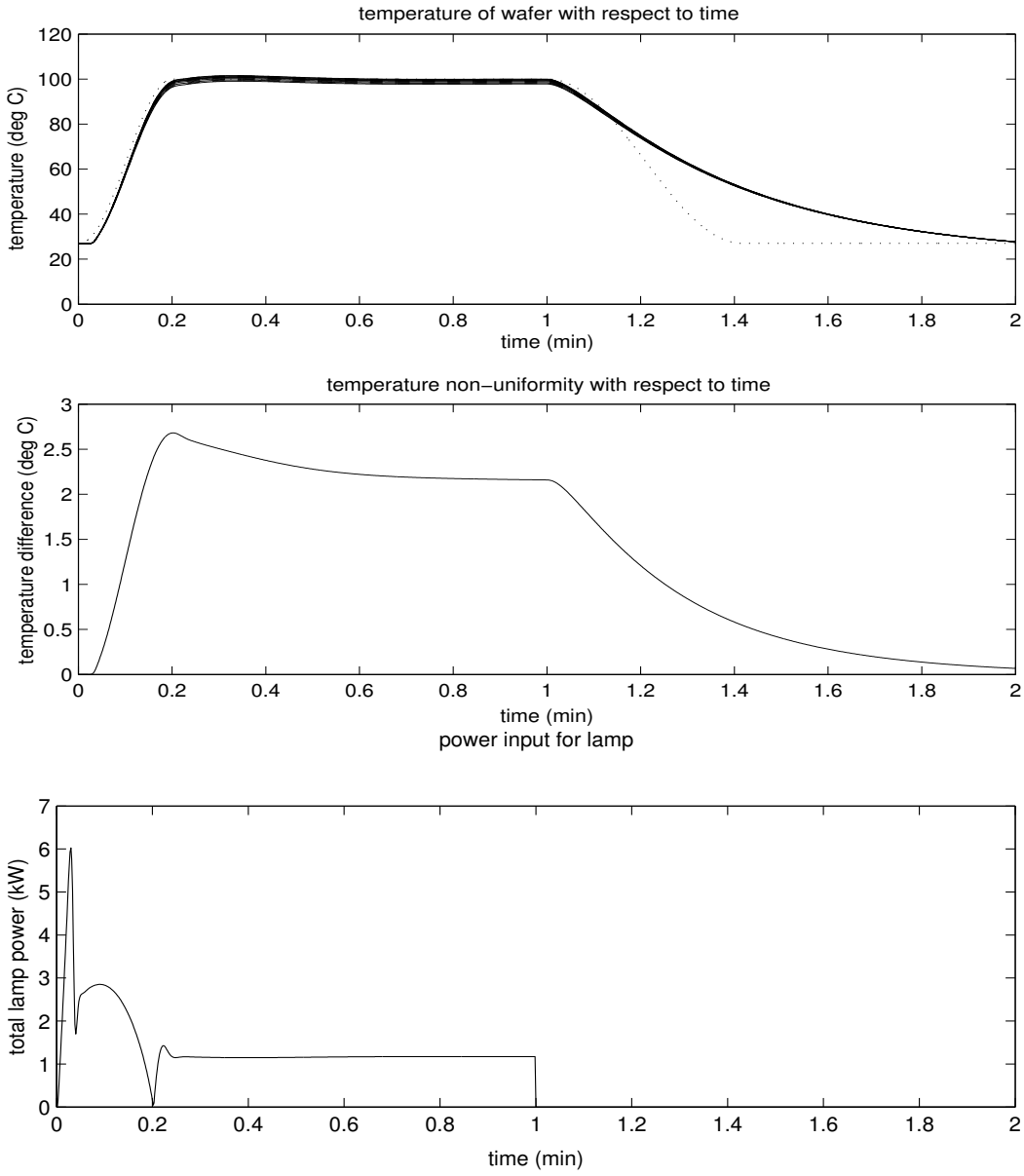

Figure 5.5. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle. The system is set up as a single zone system with the center of the wafer temperature being fed back to the controller. The second plot shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. The third plot shows the total lamp power.

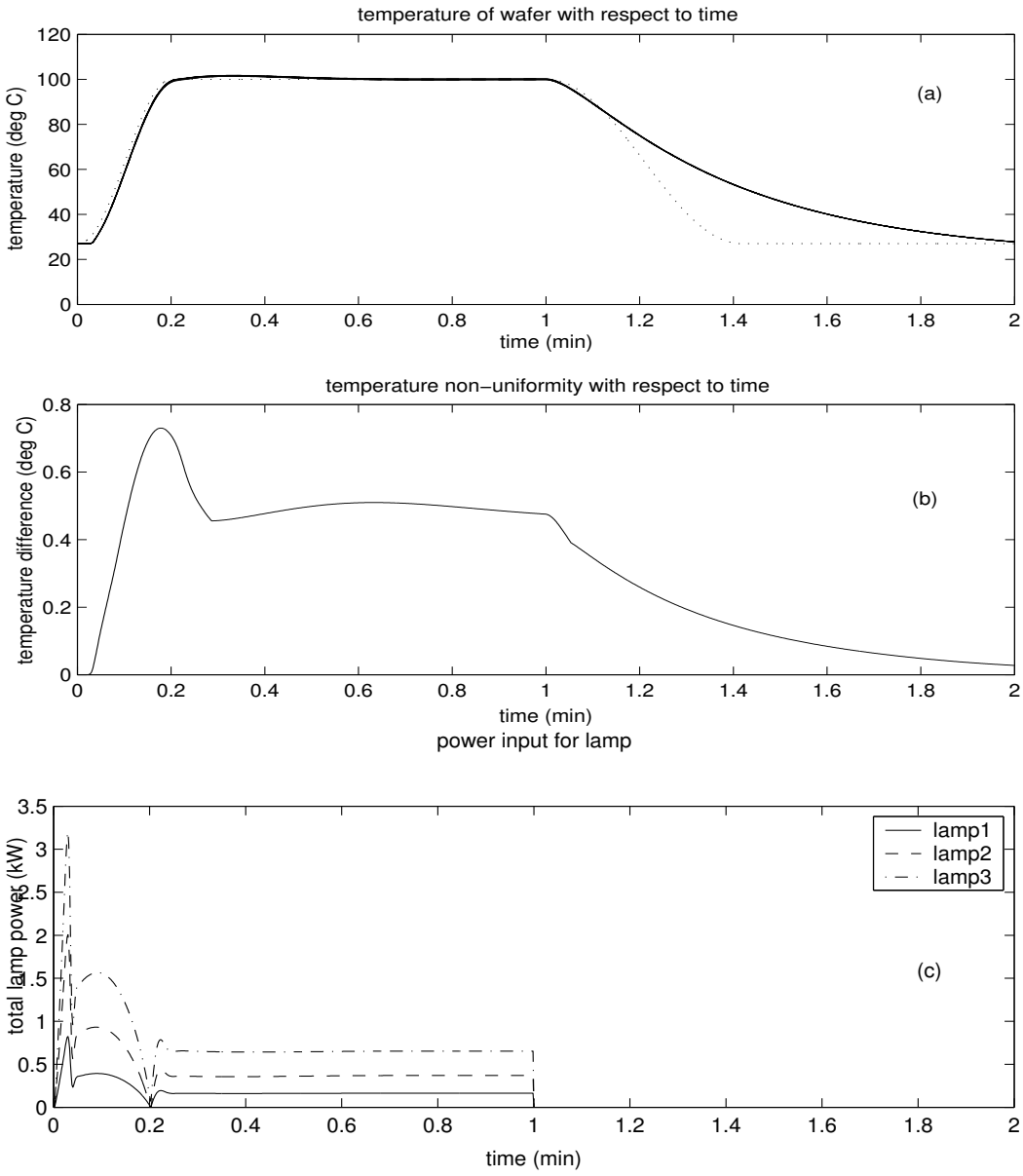

Figure 5.6. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle shown at plot (a). The system is set up as 3 single decentralized systems with each of the wafer temperatures directly below each of the lamp locations being fed back to the respective lamp controllers. Plot (b) shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. Plot (c) shows the lamp power in each of the lamp zones. Solid line indicates the innermost zone, dashed line indicates the middle zone and dotted line indicates the outermost zone.

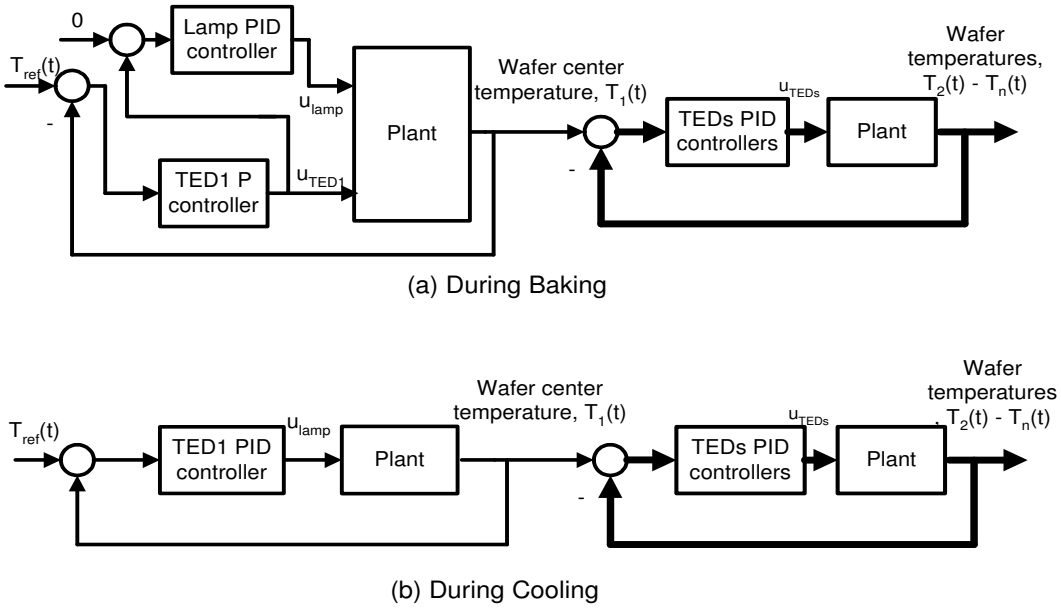

Figure 5.7. Block diagram of the integrated bake/chill control configuration. Plot(a) is the control scheme at the phase of heating; plot(b) is the control scheme at the phase of cooling.

ture to follow a desired wafer temperature trajectory. The rest of the zones maintains temperature uniformity by forcing their temperatures to follow the wafer center temperature. The individual controllers used are of the proportional-integral-derivative (PID) type; in short, a decentralized control scheme is used (Skogestad and Postlethwaite, 1996). During baking, a cascade control structure is used as shown in Figure 5.7(a). The cascade implementation (Skogestad and Postlethwaite, 1996) has the advantages of decoupling the design of the lamp and TED controllers where u_{TED1} takes care of the fast control and u_{lamp} the long-term control. Note that a single-zone lamp configuration is used here, simulation below shows that this is sufficient to obtain the desired specifications. More advanced control algorithms can be used to improve performance, but the objective of our approach is to develop a system that can achieve the desired specification using simple control algorithms.

Figure 5.8 shows the wafer temperature responses. The temperature nonuniformity is less than 0.1^oC during the entire thermal cycle. The rise time of 10 seconds

is much faster than conventional proximity bake systems which typically have a rise time of about 20-30 seconds (El-Awady, 2000). This is made possible due to the lamp-based heating approach. The total lamp power is also shown in Figure 5.8(c); as expected, the power consumption is high during the initial transient period. The electrical powers to the 15 zones of TEDs during a thermal cycle are shown in Figure 5.8(d). Since the lamp configuration is designed to achieve tight temperature uniformity, any temperature regulation during the baking process from the TEDs is minimum as shown in Figure 5.8(d). Notice that the zone powers are neither equal nor proportional in magnitude. In fact the different zones have very different power distribution to achieve temperature uniformity thereby demonstrating the power of the proposed multizone approach. We note also that better temperature uniformity could be achieved by re-tuning the respective controllers, a more powerful approach is to design a multivariable controller that takes into account the interaction between each zone (Skogestad and Postlethwaite, 1996). Figure 5.9 shows the flow rate of the chiller and its corresponding temperature. The temperature of the chiller is regulated back to its original temperature after each wafer run so that the process is repeatable for each wafer processing cycle.

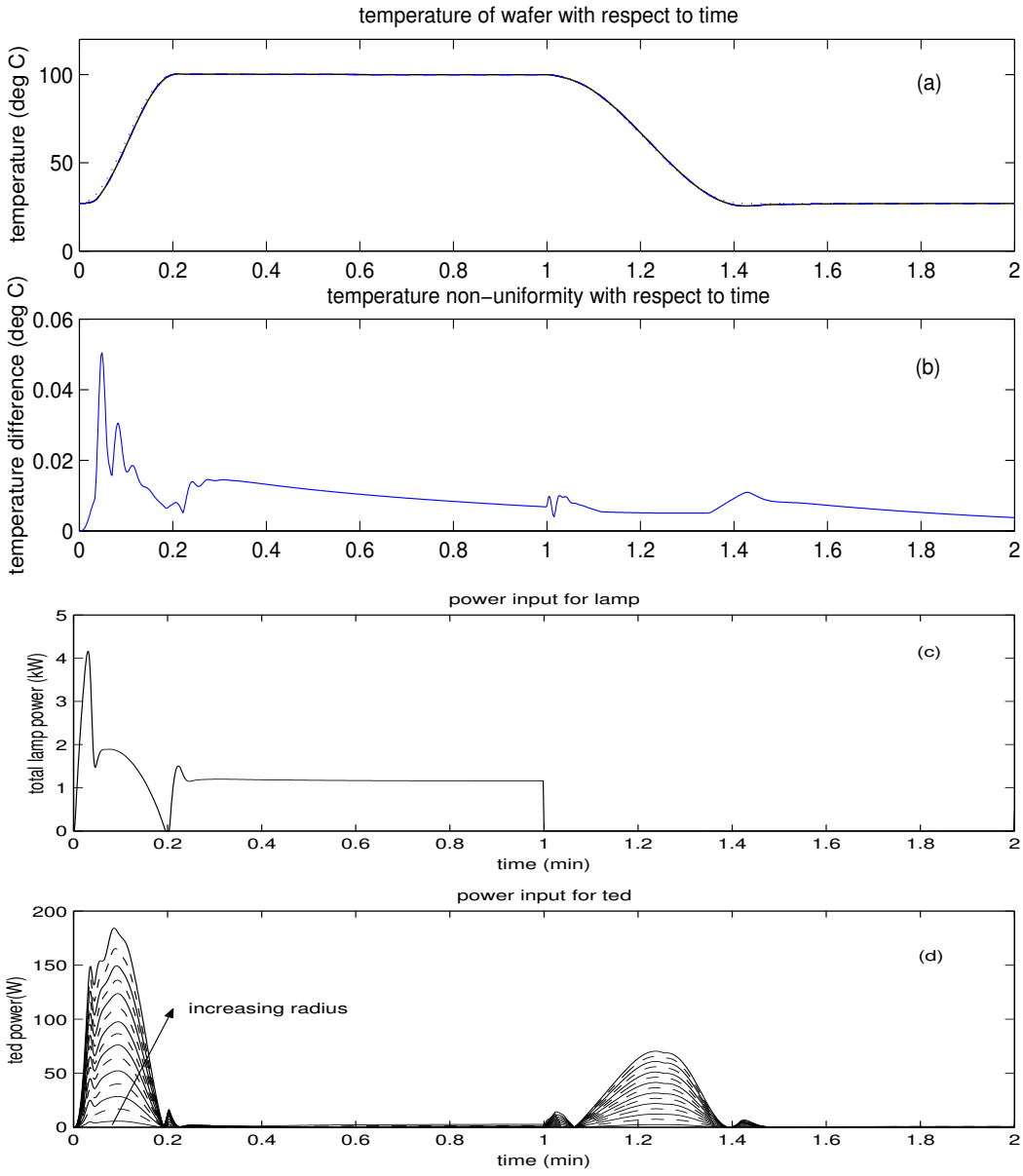

Figure 5.8. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle is shown at plot (a). Plot (b) shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. Plot (c) shows the total lamp power. The TED power in each of the zones is shown in the plot (d).

In all instrumentation and measurement designs, the dynamics of the temperature sensor used have to be taken into consideration. All the previous plots shows the real wafer temperatures, while the measured temperature is used as a feedback to the controller. Figure 5.10 shows the difference between the measured and real wafer temperatures during a thermal cycle. As expected, the measured temperature has a slightly delayed response to temperature variations due to the sensor dynamics.

Figure 5.11 shows the respective surface temperature during the thermal cycle. The wafer and TEDs (ceramic) surfaces are obtained from the center of the wafer. The lamp and chamber is assumed to be isothermal and hence represented by a single temperature respectively. As expected, the ceramic surface is at a higher temperature compared to the wafer during initial transient baking and lower temperature during the initial transient chilling. During the chilling process, the lowest temperature of the ceramic surface is about 17 ^{o}C. In a typical cleanroom environment, the air temperature is about 24 ^{o}C and with a the relative humidity of about 50%, the dew-point temperature is about 13 ^{o}C. Since the temperature of the top ceramic is considerably higher than the dew-point temperature, we can rule out the chances of condensation during thermal cyclings. The temperature of the different TED layers are shown in Figure 5.12. Figure 5.13 shows the corresponding radiosities of the various surfaces.

In determining the recipes for post-exposure baking, it is normally necessary to obtain data at multiple temperatures. These studies can be time-consuming and costly. In addition, errors can occur if drifts in the other equipment affect results and thus making it difficult to determine the impact the temperature has on the process. Using the proposed system, it becomes possible however to achieve several different processing temperatures using a single experiment. This situation is achieved by programming the temperature to different set points across the surface of the substrate by utilizing the multizone temperature control capability.

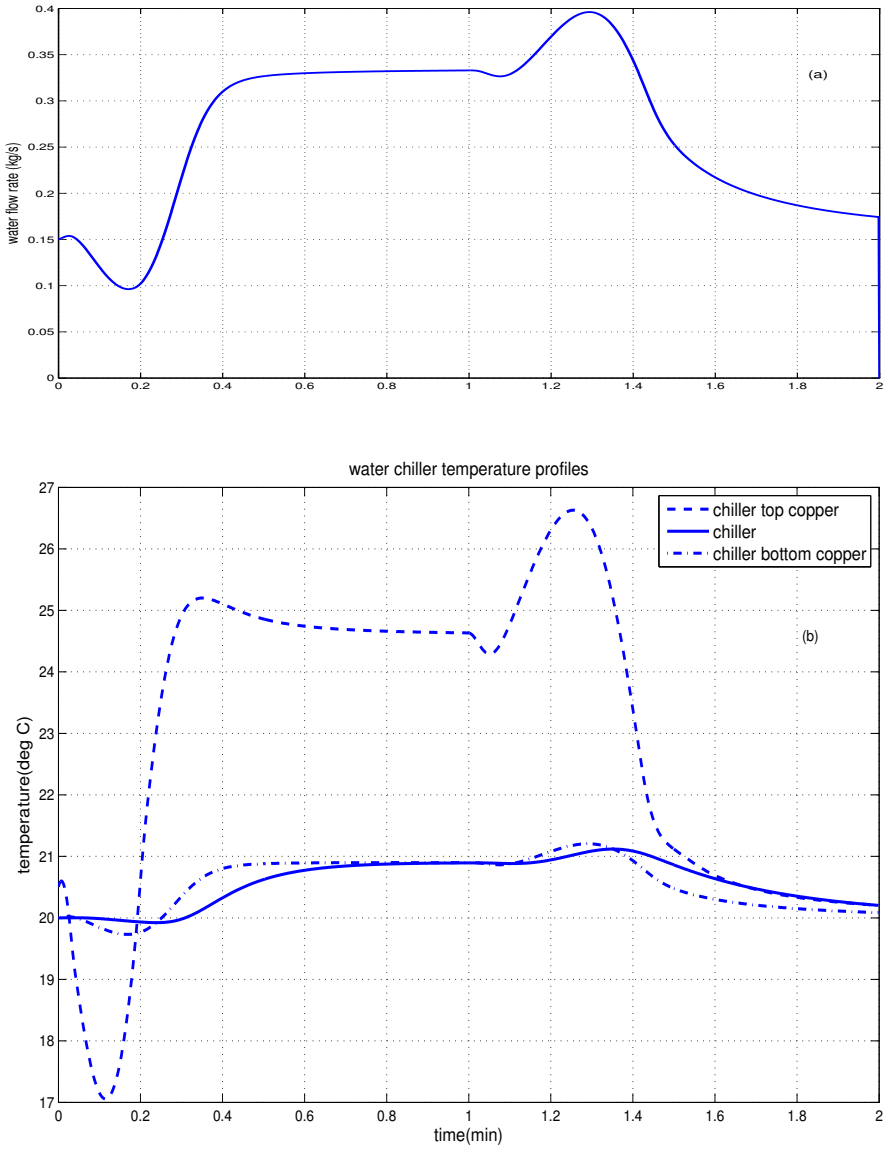

Figure 5.9. Flow rate and chiller temperature responses during the entire thermal cycle. Plot (a) is the cooling water flow rate in the whole cycle; plot (b) shows the temperature profiles for chiller and top and bottom copper plate.

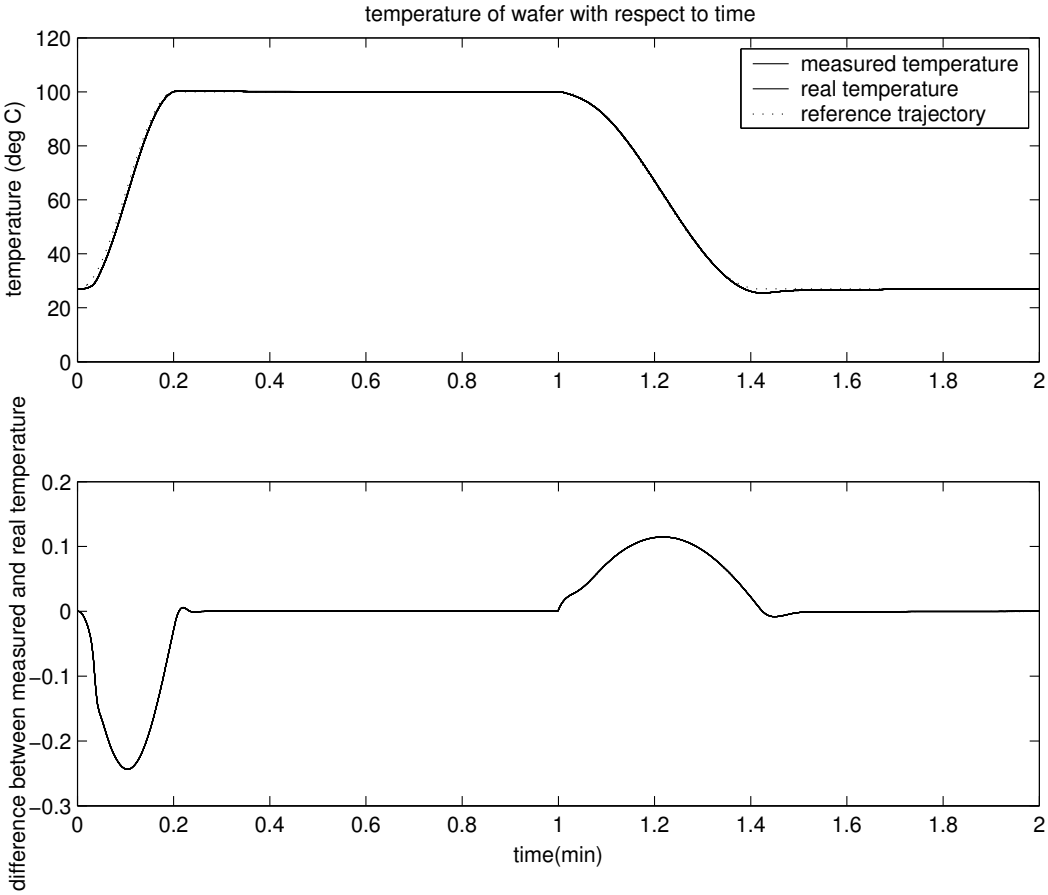

Figure 5.10. Comparison between real and measured wafer temperatures. The first plot shows the comparison between real and measured temperatures, and the second plot is the difference plot.

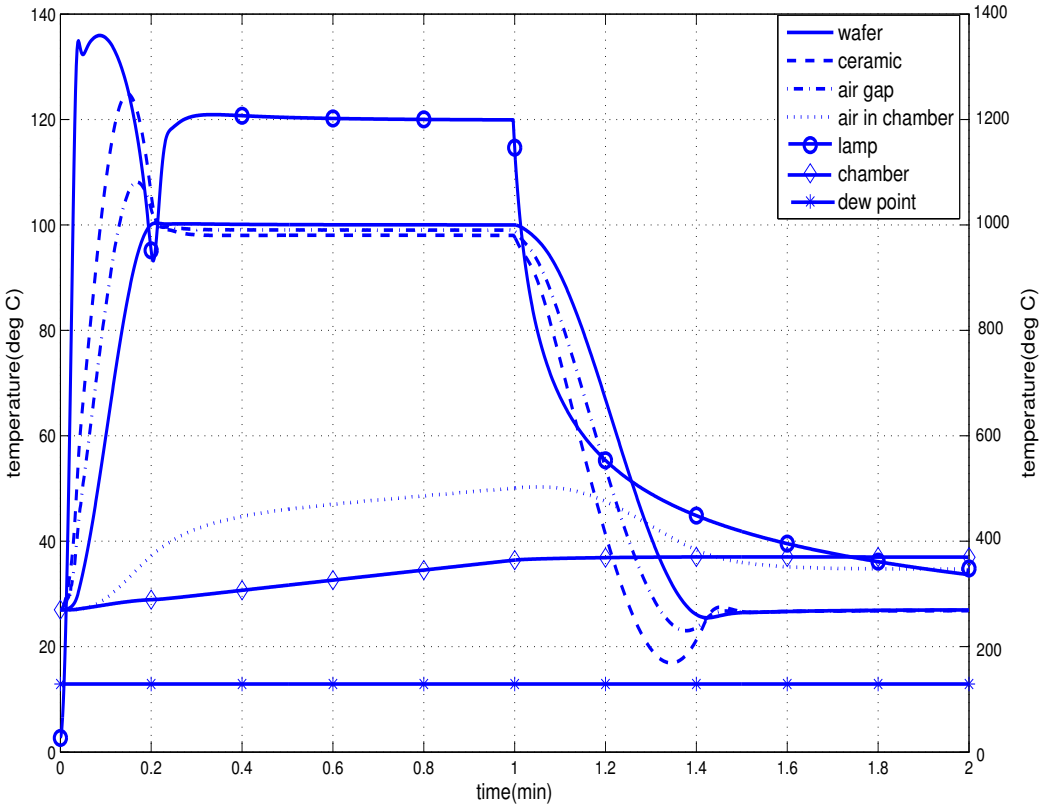

Figure 5.11. Different surface temperature during the entire thermal cycle is shown. The lamp temperature is indicated on the right ordinate. The rest are indicated on the left ordinate.

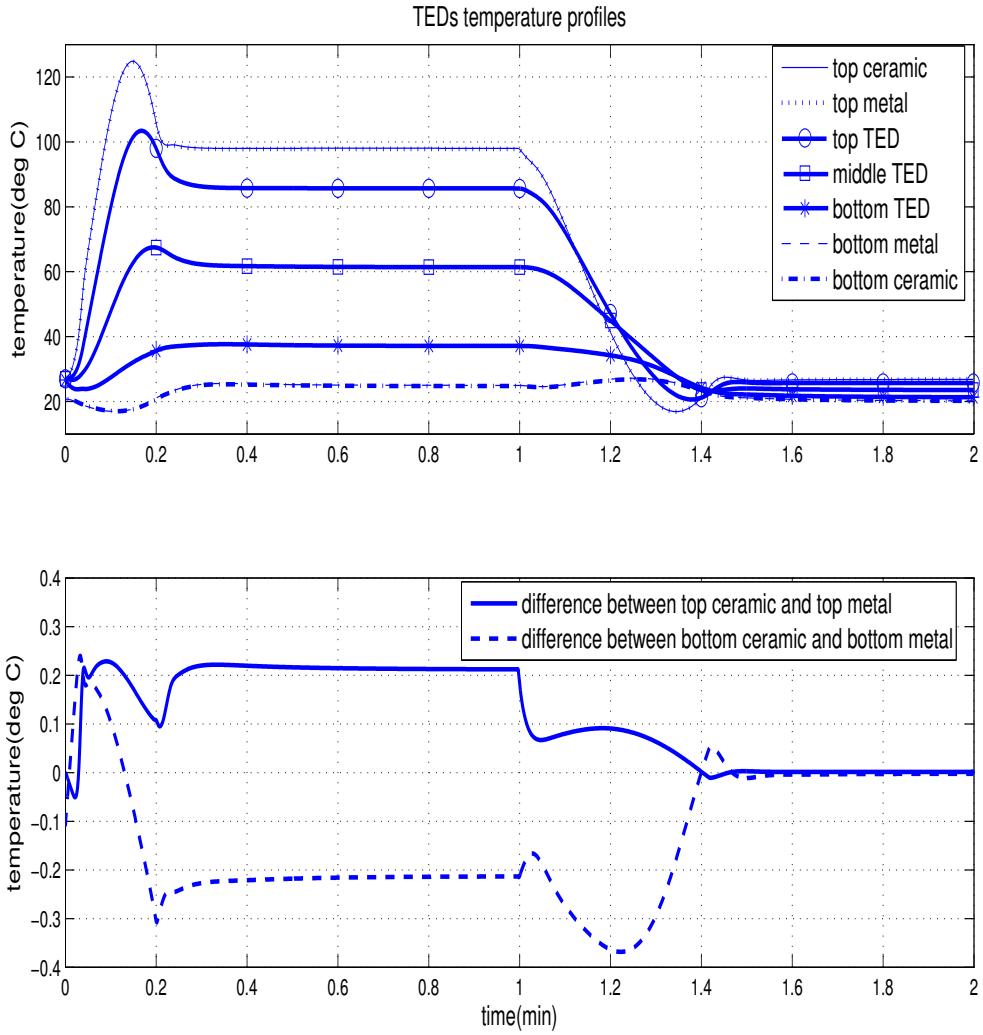

Figure 5.12. Different surface temperature during the entire thermal cycle shown in Figure 5.8. The lamp temperature is indicated on the right ordinate. Temperatures of different layers of TEDs during an entire thermal cycle shown in (b) and (c).

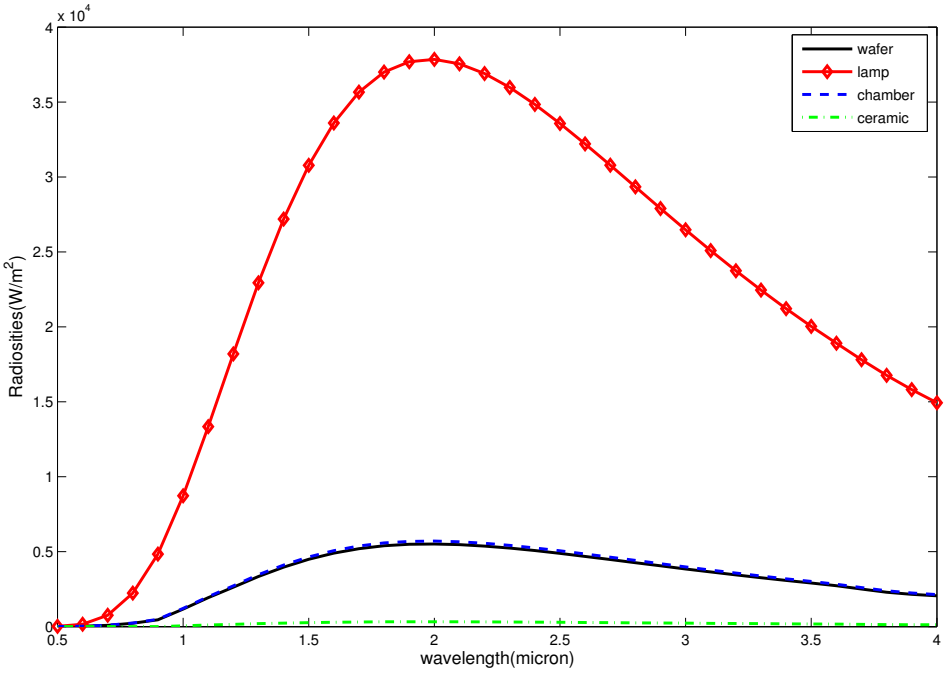

Figure 5.13. Spectral radiosities for the different surfaces at 10 seconds of the thermal cycle shown in Figure 5.8.

The flexibility of the thermal processing module to achieve multiple set points across a substrate is simulated in Figure 5.14. Here the 15 zones on the substrate are controlled such that the temperature set point for each zone is separated by 1.4^{o}C. Other distributions of temperature are certainly possible, of course where each temperature site across the entire substrate is biased. This capability also demonstrates the decoupled nature of the system.

5.5 Conclusion

The design of an integrated bake/chill module for photoresist processing in lithography is presented in this chapter, with an emphasis on the spatial and temporal temperature uniformity of the substrate. The system consists of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide real-time dynamic and spatial control of the sub-

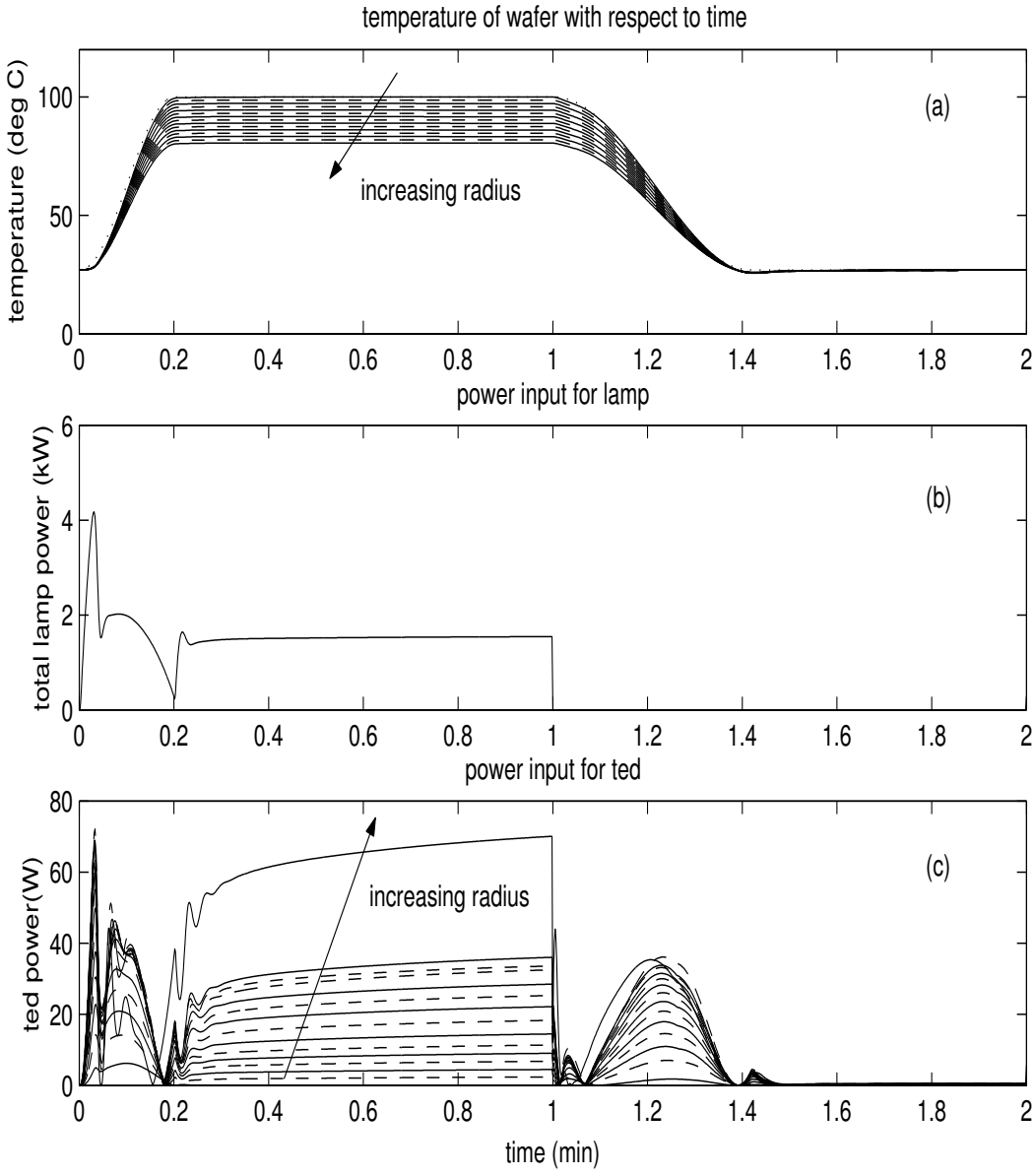

Figure 5.14. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle with temperature biasing. Each zone is set to a different temperature trajectory with a temperature difference of 1.4^oC between each zone at steady state. The lamp and TEDs power are also shown.

strate temperature. The TEDs also provide active cooling for chilling the substrate to a temperature suitable for subsequent processing steps. The use of lamps for radiative heating offers fast ramp-up and ramp-down rates during thermal cycling operations. In the proposed system, the bake and chill steps are integrated thereby eliminating the loss of temperature control typically encountered during the mechanical transfer from the bake to chill step. The feasibility of the proposed approach is demonstrated via detailed modelling and simulations based on first principle heat transfer analysis, in particular the complete spectral optical properties of the wafer has been accounted for. The distributed nature of the design also engenders a simple decentralized control scheme which satisfies tight spatial and temporal temperature uniformity specifications.

	Property	**Value**
Lamp	Emissivity, ϵ	0.425
	Thermal mass of zones 1, 2, 3	0.0041 kg, 0.0099 kg, 0.0157 kg
Chamber (unpolished gold coated)	Emissivity, ϵ	0.02
	Density, ρ	8933 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	385 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	401 $\mathrm{Wm^{-1}K^{-1}}$
	Thickness, t_{ch}	1 mm
Wafer (silicon)	Density, ρ	2330 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	712 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal Conductivity, k	148 $\mathrm{Wm^{-1}K^{-1}}$
	Thickness, Z	0.675 mm
	Diameter, D	300 mm
Ceramic	Emissivity, ϵ	0.9
	Density, ρ	3110 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	375 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	36 $\mathrm{Wm^{-1}K^{-1}}$
	Thickness, t_c	0.5 mm
Metal contact (copper)	Density, ρ	8933 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	385 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	401 $\mathrm{Wm^{-1}K^{-1}}$
	Thickness, t_m	0.25 mm
Thermoelectric elements[1]	Density, ρ	7534 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	554 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	1.5 $\mathrm{Wm^{-1}K^{-1}}$
	Seebeck coefficient, α	$(22224 + 930T - 0.9905T^2) \times 10^{-9}$ $\mathrm{VK^{-1}}$
	Electrical resistivity, R	$(5112 + 163.4T + 0.6279T^2) \times 10^{-10}$ Ωm
	Thickness, t_{ted}	3 mm
air in chamber	Density, ρ	1.239 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	1000 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	0.025 $\mathrm{Wm^{-1}K^{-1}}$
chiller (copper)	Density, ρ	8933 $\mathrm{kgm^{-3}}$
	Specific heat capacity, c_p	385 $\mathrm{JK^{-1}kg^{-1}}$
	Thermal conductivity, k	401 $\mathrm{Wm^{-1}K^{-1}}$

Table 5.1. Physical parameters of the thermal processing system.

Chapter 6

Conclusions

6.1 Conclusions

Semiconductor manufacturing has entered the era of extremely fine feature size and exceedingly complex integrated systems. Lithography is recognized as the cornerstone of modern IC manufacturing. As transistor dimension continues to scale down and wafer size continues to scale up, it has caused a dramatic increase of process variation and in particular critical dimension variation in lithography. Advanced process/equipment control would be the enabling technology needed to enhance process control and yield in IC manufacturing.

Consistent with this trend, the thesis examines the application of advanced process/equipment control methodology to meet the challenges of thermal processing in the lithography process. The control system methodology is applied to the real-time monitoring and control of photoresist property. Resist property uniformity is improved within wafer and from wafer to wafer. Another contribution of this thesis is the design of a new integrated bake/chill equipment for photoresist processing. Advanced equipment control is realized to meet tighter temperature specifications required by future technology generation.

A new application of control system method in the real-time adjustment of

photoresist extinction coefficient during the softbake process has been presented in Chapter 2. The capability of the real-time process control has been demonstrated by the uniformity improvement of the resist extinction coefficient. This could lead to CD uniformity improvement. The application has been realized by controlling the temperatures of a multizone bakeplate through the regulation of the power distribution for different zones. An average of 70% improvement in resist extinction coefficient nonuniformity has been obtained across the wafer and from wafer to wafer

In Chapter 3, the influence of wafer warpage on the photoresist properties estimation using reflectometer has been investigated. It has been found that wafer warpage has almost no effect on the thickness estimation while it can result in a considerable error on the estimation of extinction coefficient. The estimation error is resulted from the reflectance curve shift in the presence of wafer warpage. Proper calibration method for extinction coefficient estimation has been proposed so that accurate parameter estimation is obtained in the presence of wafer warpage. It has also been demonstrated that the acquired reflectance data can be used for real-time wafer warpage detection.

As an extended application of the reflectometer, a new integrated metrology system is proposed and demonstrated in Chapter 4. It has been found that by integrating such a metrology system into the spin-coating or edge-bead removal process, in-situ information of photoresist thickness profile can be obtained.

A new design of integrated bake/chill equipment for photoresist processing has been presented in Chapter 5. The new equipment emphasizes on the spatial and temporal temperature uniformity of the substrate for photoresist processing. It consists of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) to realize real-time dynamic and spatial control of the substrate temperature. The feasibility of the proposed system has been demonstrated by detailed modelling and simulations. This new bake/chill

system could meet the requirement of temperature uniformity of 0.1^oC in the PEB process.

6.2 Future work

In the real-time photoresist extinction coefficient control application, the control algorithm manipulates the multizone bakeplate temperature so that a non-uniform temperature distribution can result in a uniform resist extinction coefficient distribution. This idea can be extended to control the CD as CD is a function of resist properties (extinction coefficient or thickness). Similarly, the resist properties can be manipulated in real-time so that a non-uniform resist extinction coefficient can give rise to a more uniform CD distribution. This can help to compensate for any CD variation caused by variations of other process variables. This concept can be realized in a run-to-run control scheme. Open-loop experiments can be done to identify the correlation model between CD and resist extinction coefficient. Using it, resist extinction coefficient of next wafer can be controlled to its optimal value based on the CD measurement of current wafer. An uniform CD can be achieved from wafer to wafer. The influence of wafer warpage on CD can also be considered and CD variation due to wafer warpages can be compensated.

Resist coating contour has been obtained by the integrated metrology system proposed in Chapter 4. The contour information can be compared with given specification and simple accept/reject action be taken. Rejection of "defective wafers" would result in increase of manufacturing cost. So if some of the "defective wafers" can be re-adjusted to "normal" status, it would be beneficial for cost saving. Advanced feedforward process control could meet the requirement. The resist thickness contour can be used as feedforward information for subsequent process including bake or develop process. Feedforward controller can be designed to adjust the subsequent processes to compensate for the resist thickness non-

uniformity. For example, bake temperature may be raised or develop time may be longer when the resist is thicker.

Author's Publications

List of publications

Journal Papers

[1] A. Tay, W. K. Ho and X. D. Wu, "Real-time control of photoresist extinction coefficient uniformity in microlithography". *IEEE Transactions on Control System Technology*, 15(1), 2007, pp. 99-105.

[2] A. Tay, H. T. Chua and X. D. Wu, "A lamp thermoelectricity based integrated bake/chill system for photoresist process". *International Journal of Heat and Mass Transfer*, 50, 2007, pp. 580-594.

[3] W. K. Ho, A. Tay, X. D. Wu and X. Q. Chen, "In-situ monitoring of photoresist thickness contour on wafer in microlithography". Submitted to *Optical Engineering*, 2007.

[4] A. Tay, W. K. Ho and X. D. Wu, "Influence of wafer warpage on photoresist film thickness and extinction coefficient measurements". Submitted to *Review of Scientific Instruments*, 2007.

Conference Papers

[1] A. Tay, W. K. Ho, X. D. Wu and C. M. Kiew, "In-situ measurement and control for photoresist processing in microlithography". *AIChE Annual Meeting, Conference Proceedings*, 2004, pp. 7473-7487.

[2] A. Tay, W. K. Ho, X. D. Wu, K. Y. Tsai and J. H. Lee, "Real-time control of photoresist absorption coefficient uniformity". *Proceeding of SPIE*, vol. 5755, 2005, pp. 187-195.

[3] A. Tay, H. T. Chua, X. D. Wu and Y. H. Wang, "A lamp thermoelectricity based integrated bake/chill system for advanced photoresist process". *Proceeding of SPIE*, vol. 6153, 2006, p. 61534M.

[4] W. K. Ho, X. Q. Chen, X. D. Wu and A. Tay, "Real-time monitoring of photoresist thickness contour in microlithography". *15th International Symposium on Semiconductor Manufacturing*. 25-27 September 2006. Tokyo, Japan.

[5] X. D. Wu and A. Tay, "Influence of wafer warpage on photoresist film thickness and extinction coefficient measurement". *Proceeding of SPIE*, vol. 6518, 2007, p. 65184F.

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