CONTROL OF HIGH PERFORMANCE SINGLE PHASE DC-AC INVERTER

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A THESIS SUBMITTED

FOR THE DEGREE OF MASTER OF ENGINEERING

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2006

Acknowledgments

I would like to express my gratitude to all those who bring me the possibility to complete this thesis.

First of all, I would like to express my sincere appreciation and thanks to my supervisor Prof. Sanjib Kumar Panda whose help, stimulating suggestions and encouragement helped me in all the time of research for and writing of this thesis. Without his patient, inspiriting and thoughtful guidance, this thesis can not be completed. I am also deeply grateful to my co-supervisor Prof. Xu Jian-Xin, for his detailed and constructive comments, and for his important support throughout this work. His overly enthusiasm on research, sharp insight in area of control theory and application have been a source of inspiration for me.

I wish to express my warm and sincere thanks to all the lab officers, lab-mates and friends from Electrical Machines and Drives Lab, Power Electronics Lab and Power Systems Lab. Lab officers Mr. Woo is always diligent, helpful and friendly to all the students. Mr. Chandra, Mr. Teo and Mr. Seow help me on my research work, thesis and my graduate assistant work. My warmest thanks to research scholars in EMD lab, Dr. Dong Jing, Dr. Anshuman Tripathi, Mr. S.K. Sahoo, Dr. Liu Qinghua, Ms. Qian Weizhe, Dr. Phyu, Mr. Krishna Mainali. Dong Jing, Weizhe and Phyu

took good care of me during my two years in NUS like my elder sisters. Anshuman, Sahoo and Qinghua helped me and supported me in many respects, research, paper work and even my job seeking. Krishna, a great guy with a warm heart, helps me a lot in my research without any hesitate. I am also very fortunate to meet my lab-mates Mr. Amit Gupta, Mr. Jolly Laurent, Ms. Wu Xinhui, Ms. Zhou Haihua, friends from PE lab Ms. Yin Bo, Ms. Kong Xin, Ms. Chen yu, Mr. Deng Heng, Mr. Cao Xiao, Mr. Yang Yuming, Mr. Hadja Marecar, and Mr. K. Viswanathan. My good friend Amit shared lots of his invaluable experience and resources with me selflessly. The huge energy, curiosity, and passion from Laurent influences me in the way he may not even know. Thanks Haihua for helping for my administrative matters many many times when I am working outside the campus.

In my two years life in NUS, I am honored to make many warm-hearted, smart and wonderful friends. Yanyu and Yiqun, you two are amazing friends who shared the most joyful time with me. Shimiao, yuting, you are the one who cheer me up when I am upset and lost. Thanks my old friends from Zhejiang University, you helped me to repel loneliness when I first came to Singapore. Chen Tong, your love, understanding, and encouragement stimulated me to reach this far.

Deep in my heart is special thanks to my family, especially to my mother. Thank you for being most supportive and giving incredible love to me. You gave me faith to be strong through all the bad and good moments. I only hope that what I have accomplished can pay somewhat for the efforts for raising and making me the person that I am today.

Contents

Summary

DC-AC Pulse Width Modulation (PWM) inverters have been extensively used in applications such as AC power conditioning systems, uninterruptible power supplies (UPS) and AC drives. In recent years, with the increase in non-linear power electronics loads which draw non-sinusoidal currents from the utility supply, the power quality distortions become a serious problems in electrical power distribution systems. UPS systems provide reliable, and high-quality power for critical loads. They protect sensitive loads against power outage as well as over-voltage and under-voltage conditions. They also suppress line side transients and harmonic distortions. UPS systems are widely used for computer systems, medical emergency facilities and life-support systems etc. In these applications, the output voltage of the inverter is required to be sinusoidal under all operating conditions. Output voltage Total Harmonic Distortion (THD) is one of the important performance index to evaluate the performance of the inverter system. Extensive research works have been carried out on control of the DC-AC inverters for UPS applications. PWM modulation techniques have been adopted for minimizing the voltage distortions. But due to their open-loop control characteristics, they are not able to maintain good performance with load or supply side disturbances. Conventional control methods such as PID control, single-loop voltage feedback control, and cascaded control have been applied for inverters in the past. However, none of these

are able to achieve good steady state and dynamic performance while supplying power to nonlinear loads. Deadbeat control has been adopted to provide fast dynamic performance, but the performance is highly dependent on accuracy of the plant model parameters those are used to derive the control algorithm. Model based control methods such as sliding-mode control gives good dynamic response and low THD for various operating conditions. However, sliding-mode control has drawbacks such as requiring information of all state variables or their estimates, high switching frequency and difficulty in choosing a good sliding surface. Neural networks control method needs large training database, which is time consuming to build. Compared with these methods, repetitive control is a good solution for minimizing periodic errors for inverter system due to the periodic characteristic of the error voltage. Moveover, repetitive control being a modular unit can be used as a plug-in module to any existing control system. Due to the relatively simple control law, it is easy to implement the repetitive controller.

This thesis presents two digital plug-in repetitive controllers namely: Time Domain Repetitive Controller (TDRC) and Frequency Domain Repetitive Controller (FDRC). The two controllers are used together with conventional deadbeat controller for minimizing the tracking error of the output voltage in single-phase DC-AC inverters. Repetitive control is a control scheme applied to plants that must track a periodic trajectory or reject periodic disturbances with the explicit use of the periodic nature of the trajectory or disturbances. Owing to the fact that low frequency harmonics significantly contribute to the periodic error in the output voltage, repetitive control is suitable for the DC-AC inverter system. It does not need an accurate model of the plant system, but needs only minimum information such as approximate gain of plant transfer function.

The two proposed control schemes consist of a conventional deadbeat controller as the feedback controller and a plug-in repetitive controller. The deadbeat controller contains a cascaded structure with two loops: *outer voltage control loop* and *inner current control loop*. It is designed to achieve fast dynamic response, good steady state performance and suppression of the load disturbances. The plug-in repetitive controller can be designed in two different ways: one based on *time domain* and the other based on *frequency domain* respectively. Time domain based repetitive controllers memorize the previous cycle output tracking error signal and filters out the unwanted high frequency signals in order to compensate for the present cycle error. Digital filters incorporated within the time domain based repetitive controller and analog pre-filters for feedback signals lead to different phase shifts for different harmonic components of the error signal. However, the phase delay compensation can only be provided for only one frequency component and in most of the case it is the fundamental component in the time domain design approach. Hence, phase delays of other harmonic components which are not compensated deteriorate the system performance.

However, using frequency domain based repetitive controller it is possible to solve this different phase delay problem for different frequency components. The learning algorithm is designed based on Fourier series approximation method instead of commonly used time domain approach. It uses Fourier series analysis to obtain the magnitude and phase angle of each frequency component in the error signal, and uses these parameters to reconstruct a signal which only contains chosen frequency components for learning. Moreover, the time delay generated due to filters can be easily compensated for each frequency component just by adding a phase delay compensation in the reconstructed signal. Besides, frequency domain

based repetitive control gives the freedom of choosing a different learning gains for each frequency component individually, and therefore achieves better tracking performance. This approach offers significant improvement in the voltage tracking objective as compared to the conventional time domain based repetitive approach.

Simulation and experimental results for a DC-AC single phase inverter (1 kVA) obtained with time domain and frequency domain based repetitive controllers are presented and compared to that obtained with conventional cascaded deadbeat feedback controller. Both the repetitive control approaches provide significant performance improvements as compared to the conventional cascaded deadbeat controller. However, amongst the two repetitive approaches, the frequency domain based approach provides improved tracking performance due to the additional flexibility of implementing different control gains and phase delay compensations for each frequency component. The analysis of stability and evaluation of choosing learning control gains of the time domain based repetitive controller has been provided and supported with simulation results.

Compared with other control methods, the proposed time domain based and frequency domain based repetitive control schemes have demonstrated low THD 3 % and 1 % respectively for nonlinear loads, reduced from 4.9 % by using only deadbeat controller. An important merit of the proposed repetitive scheme is that they can be designed and implemented without the detailed knowledge of the plant model. For future developments, the proposed control schemes could be extend to three phase DC-AC inverter system as well.

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Chapter 1

Introduction

Power electronics is the technology associated with the efficient conversion, control and conditioning of electric energy by using static power semiconductor devices. Thus the power electronics converter process the raw electrical energy and converts it into the desired electrical output form from an available input in raw electrical form into the desired electrical output form as required by the load. In recent years, power electronic technology has grown dramatically due to the introduction of power semiconductor devices and digital signal processors. The market for power electronics has significantly expanded at the same time.

The key element of power electronic system is the switching power converter. A common switching power electronics system comprises four basic parts: power source, converter, load, and controller. Compared with linear power supply, switched mode power converter provides the required electrical power to the load system with high efficiency. On the other hand, power electronic devices make efficient conversion and utilization of electrical energy. By using the high frequency

switching technology, large and heavy line frequency transformers used in linear power supply is replaced by small size high frequency transformers in switched mode power supply. Moreover, since the power loss and hence the heat dissipation is highly reduced, the converter can be packaged with high density, which leads to a further smaller size and weight, low temperature rise, reliable converter.

Power converters may be classified based on its input and output supply: AC-DC rectifier, AC-AC converter, DC-AC inverter and DC-DC converter. An DC-AC power converter transforms a DC input voltage to a desired magnitude and frequency AC output voltage. The AC power it provides is reliable and efficient, widely used in Uninterruptible Power Supplies (UPS), motor drives system, and high frequency illumination etc. The power range is varied from tens of watts to several thousands watts.

1.1 DC-AC Inverter in Uninterruptible Power Supplies

Uninterruptible Power Supplies (UPS) provide reliable, and high-quality power for critical loads. Appliances such as computer systems, medical facilities, life-support systems, telecommunications, and emergency equipments are protected by UPS in case of power outage as well as power line over-voltage and under-voltage conditions. These critical loads require high quality sinusoidal voltage under all operating conditions.

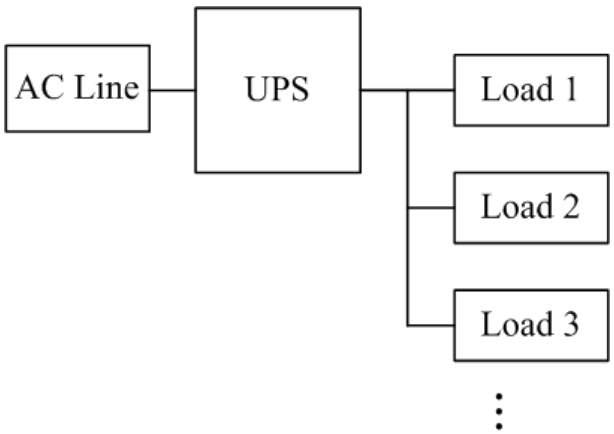


Figure 1.1: Block diagram of a centralized UPS system

There are two approaches in UPS system development: *distributed* and *centralized*. In centralized approach, only one UPS unit provides power for all the loads, as shown in Fig. 1.1. In the distributed approach, many different UPS units connected in parallel supply the individual loads, as shown in Fig. 1.2. If there is a power failure in centralized UPS system, the load will be not able to operate. However, in distributed UPS system, failure of one UPS would not affect the operation of loads. Hence, the distributed approach is more practical than centralized approach for high power applications because of its high reliability, flexibility of expansion, and low price. Many research works are focused on control in UPS for parallel operation [1][2][3].

Generally, UPS systems are classified into three types: *static*, *rotary* and *hybrid static/rotary* [4]. Static UPS systems consists of battery bank and power electronics systems including rectifier, inverter, and filter. A block diagram of a static UPS system is shown in Fig.1.3. In the event of a mains line outage, the battery provides power to the inverter instead of the rectifier under normal

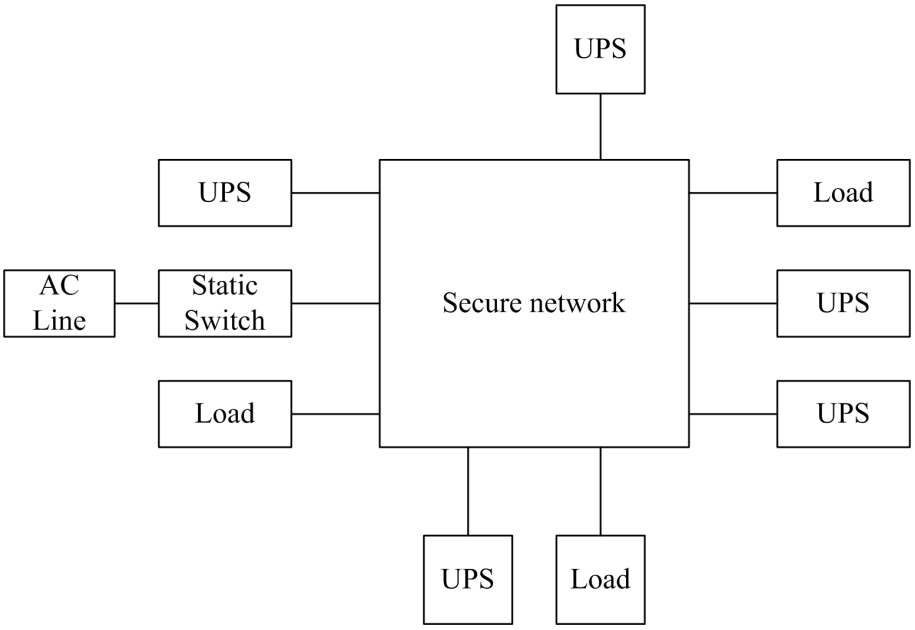


Figure 1.2: Block diagram of a distributed UPS system

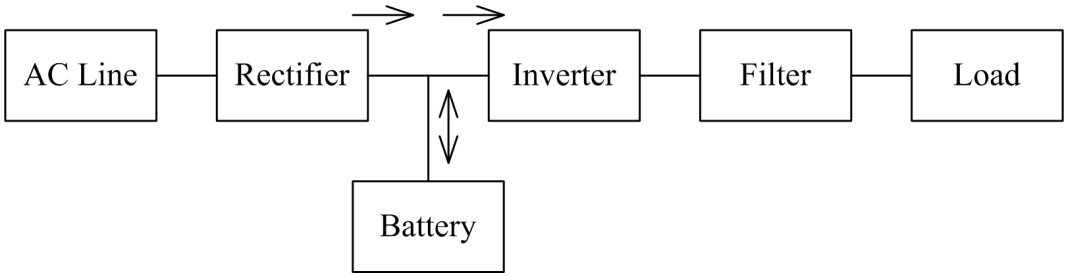


Figure 1.3: Block diagram of a UPS

operating mode. The filter minimizes the high frequency harmonics in AC output voltage. The inverter could provide a single-phase or a three-phase electrical power according to the load requirements.

Rotary UPS systems use motors and generators to convert electrical energy from one form to another and provide the desired power. Hybrid static/rotary UPS combine static power electronic converter and motor generator together. In high power applications, the rotary UPS and hybrid UPS have better transient

overload capability as compared to the static UPS systems. But static UPS needs less maintenance and have a relatively smaller size and weight. They have various application from low-power to high-power utility system. Some of the disadvantages of the static UPS system are relatively poor performance with nonlinear and unbalanced loads and high cost for achieving improved reliability. In this thesis, the research work focuses on improving system performance of a static UPS system.

1.1.1 Control of DC-AC Inverters

In control of DC-AC inverters, Total Harmonic Distortion (THD) of the output voltage and dynamic response of the converter are the two most important features of the static UPS system. The parameter THD, which indicates the output voltage harmonic contents, is defined as equation (1.1).

$$\text{THD}_{\text{voltage}} = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \times 100\% \tag{1.1}$$

The filtered output of the inverter is required to maintain little distortions in the output voltage when connected to a highly nonlinear load.

There are several types of disturbances, such as DC-link voltage variation, Pulse Width Modulation (PWM) pulse harmonics, effect of switch dead-time, load disturbances, and sensor measurement noise which may cause distortions in the output voltage. Dead-time effect and measurement errors are considered to be minor disturbances. A large part of disturbance of PWM pulse harmonics can be

attenuated by the designed LC low pass filter. By increasing the frequency modulation ratio m_f, PWM modulation harmonics contain higher frequency harmonic components which can be easily removed by a small LC filter. In contrast, load disturbance is unknown when designing the controller.

Many control methods have been implemented for the control of switched mode inverter in order to eliminate the harmonics in the output voltage. Control of switching signal helps to reduce the size of inductor and capacitor as well as dynamic response of the system with variation of load condition. Extensive research has focused on the harmonic minimization of the output voltage, that includes reduction of tracking error and THD in both dynamic and steady states. They are discussed in the next section.

1.2 Literature Review on Control of Inverters

Given the importance of THD and dynamic response in a UPS system, the issues of minimizing THD and improving dynamic response have been receiving much attentions recently. Various PWM switching techniques, conventional and modern control methods have been proposed to solve these two problems.

In order to minimize the THD and tracking error, a simple method is to increase the switching frequency and design appropriate LC filter to remove unwanted high frequency components. However, increasing frequency leads to higher switching power losses in the high-power semiconductor devices and EMC prob-

lem. Large inductor and capacitor also increase the size and weight of the inverter system. Hence, the other alternative i.e. active control of the inverter is a good candidate to improve the performance of the inverter system. In square-wave switching scheme, each switch changes its state only twice in one cycle of the output voltage. Low switching frequency on the other hand causes less switching power losses. However, in this switching scheme, the output of inverter has significant low frequency harmonic components, and the inverter is not able to control the magnitude of output voltage. Alternatively, PWM technique provides a good solution of reducing the voltage distortions, and is capable of controlling the output voltage magnitude by changing the modulation index m_a while keeping the dc-link voltage fixed [5]. Many control schemes based on this modulation strategy have been proposed [6]-[7]. Although various PWM modulation methods have good steady-state performance, they are not capable of maintaining good quality waveform when load condition changes due to their open-loop control structure.

Closed-loop regulation of PWM inverters employing feedback control schemes has been proposed to improve the performance when load disturbance occurs [8]-[9]. A simple feedback loop can provide a well-regulated output with relatively low THD. This scheme could be implemented either in digital or analog controller. Sinusoidal PWM (SPWM) modulation algorithm usually use a sinusoidal feed-forward signal plus a feedback control signal as a modulation waveform. For continuous control based on analog control technique, the feedback signal could be the peak value, or average value or instantaneous value of the output voltage.

However, the dynamic response of instantaneous voltage feedback control [9] is considered to be slow comparing to the digital deadbeat controllers for step change in reference and nonlinear loads.

With the introduction of micro-processors, a digital real-time feedback control is feasible. With this kind of real-time feedback controllers, it is possible to obtain very fast response for load disturbances and nonlinear loads. Digital deadbeat controller can be considered a good candidate to track the reference in one or several sampling periods by placing all the closed-loop poles at the origin in the z-domain [10][11][12]. The response of deadbeat control is faster than other analog based controllers. However, deadbeat controller requires accurate information of the inverter-filter system which is sometimes difficult to obtain. Another digital method, optimum PWM technique modifies the switching algorithm to minimize specific harmonics in output signal [13]-[14]. With this scheme, output switching pattern is predefined. Particular output voltage patterns can be selected by minimizing a suitable objective function. It has a good steady-state response with linear loads; but performance deteriorates with nonlinear loads.

Analog PID control has prevailed in industry the last 50 years. Digital PID controller overcomes drawbacks of analog PID controller. It is more convenient to adjust PID control gains in digital controller so that the digital one has more flexibility. Some works have been carried out in digital PID control for DC-AC inverter [15]- [16]. PID control has advantages of easy implementation, good performance, and requires less model information. But it also has two limitations:

one is measurement noise deteriorates the tracking accuracy, the other is sample and hold module changes the control system to a delay system, and therefore the stability range shrinks so that the design of PID parameters becomes more difficult.

Problem of time delay is worth mentioning. In digital controllers, a time delay, due to both the analog-to-digital conversion and the processor's computation time, is introduced to digital feedback control systems. The maximum or minimum duty cycle is limited by this time delay and therefore affects the system performance. By increasing the dc-link voltage and reducing modulation index, the maximum duty cycle could be decreased to avoid this problem, but sometimes in reality it may not be feasible. There are several methods to compensate this delay as highlighted in [17][18][19]. In [20], two PWM methods, two-polarity PWM method and asymmetric PWM method, are proposed to handle this problem. They have the advantage of being model independent as compared to the former methods. The two-polarity PWM method combines advantages of the traditional active-high and active-low polarity PWM pattern to increase the feasible duty cycle range. Asymmetric PWM method increases the range further, but both of them create new distortions owing to change of modulation patterns or asymmetry of modulation pattern.

Cascaded control scheme provides faster response of the system than the single loop control strategy [21] [22] [23]. In [21]-[22], current-loop regulated PWM inverters with output voltage compensation have been proposed. These schemes have an inner current loop with an outer voltage loop to split the pair of undamped

poles caused by the second order LC filter. With these methods, system performance is good and has fast dynamic response. However, the gain of the inner current loop controller is required to be high enough to suppress the disturbances; and high gain controller may amplify the noise and limit cycle ringing. In [23], a decoupling method is proposed which can use modest loop gain to get a satisfactory response. It employs two cascaded deadbeat control loops, an inductor current inner loop and a load voltage outer loop to achieve fast response, and uses knowledge of load voltage and load current to decouple the system. Load current also can be seen as a compensation for load disturbance. But similar to the single loop deadbeat controller, they are highly dependent on plant model and their performance depends on the accuracy of model parameters. In addition, their tracking performance deteriorates under nonlinear loads.

To further improve the system performance and dynamic response, modern advanced control techniques, such as sliding-mode control (SMC) [24], neural networks (NN) [25] and learning control [26][27][28][29][30][31][32], have been adopted. The purpose of the sliding-mode control is to force the system status to move on a suitable surface in the state space called the sliding surface. This is accomplished by keeping the sliding function near zero. The advantage of SMC is its insensitiveness to parameter variations and disturbances. The drawback of SMC is that information about all state variables or their estimations are required, high switching frequency required and difficulty in determining a good sliding surface.

In [25][33], neural network controllers are presented. Neural network con-

troller requires a large database of patterns which is obtained through simulations. A selected feed-forward neural network controller is trained to model this controller using back propagation algorithm. Neural network controller is used to control the inverter on-line. This scheme is easy to implement and has good response with nonlinear loads, but the large pattern database is difficult to build.

In most ac power conditioning systems, periodic load disturbances are major sources of waveform distortions. Repetitive controller based on the Internal Model Principle [34] was proposed to eliminate periodic error [35]-[26]. The internal stability and asymptotic convergence of error for continuous-time internal-model-based repetitive of certain systems has been presented. In [26], the discrete time repetitive control for linear systems is proposed. Repetitive control is a control scheme applied to plants that must track a periodic trajectory or reject a periodic disturbance with the explicit use of the periodic nature of the trajectory or disturbance. Thus, it is a good solution for minimizing periodic errors for inverter system. Repetitive control has been applied to minimize the steady-state error and periodic distortions in single-phase voltage-source PWM inverters. Toshimasa Haneyoshi etc. [27] proposed a digital feedback control scheme, a one-sampling-ahead preview controller with a repetitive controller. Ying-Yu Tzou etc. [29] developed a plug-in repetitive controller to minimize low-order harmonic distortions. In this paper, there are four filters used in repetitive controller to remove the unwanted frequency components from repetitive control and compensate for phase-delays of the corresponding plant. To further improve the performance, an odd harmonic plug-in repetitive controller

is adopted in [32]. Due to the half-wave symmetric nature of the output voltage, odd harmonics have significant large magnitudes than even ones. Hence, an odd harmonic repetitive controller is an effective candidate, and it has the advantage of saving half of the memory. The above repetitive control algorithms are all implemented in discrete time domain by digital controllers. Repetitive control can be considered a good candidate to enhance the steady state performance of the system, however, the cancellation of harmonics are based on error information of the last period. This characteristic may cause a slow dynamic response using repetitive controller only. Although the previous research works above add a voltage feedback loop to speed up the response, the dynamic response can be further improved by cascaded deadbeat controller. In this thesis, a simple structure repetitive controller with a cascaded loop deadbeat controller in discrete time domain is proposed to minimize the distortions in PWM inverter. It has the advantage of both the cascaded deadbeat control providing fast response and repetitive control providing good steady state performance. Moreover, load compensation and voltage feed-forward signal are added in order to reduce the effect of load disturbance.

There are two drawbacks of time domain repetitive controller. First, it requires complicated filter design. Second, phase delay due to digital filters in time domain repetitive controller and analog pre-filters for feedback signals are not same for different frequency components. In time domain controller, only one single compensation for a fixed frequency delay is used to improve the performance in time domain design approach. This has limited performance improvement because the

uncompensated phase delay of other frequency components may cause ineffective cancellation of the harmonics.

In recent years, frequency domain repetitive control scheme has been used for motor control applications [36]. Frequency domain learning uses Fourier analysis to obtain the magnitude and phase of each frequency component, and uses these parameters to reconstruct a signal which only contains chosen frequency components for learning. As a result, learning frequency components could be easily chosen to meet this goal rather than designing filters. We choose odd and low frequency components to be eliminated to improve the performance of the inverter system. Furthermore, different phase delays for different frequencies due to analog filters can be compensated in a direct way. A frequency domain repetitive controller is developed in this thesis. It could be easily implemented with several accumulating parameter rather than a whole range of one cycle memories which usually contain hundreds of sampling data. Simulation and experimental results validate the effectiveness of the proposed control schemes.

1.3 Motivation of the Thesis

A DC-AC inverter system is widely used to provide a high quality and reliable AC power supply to the critical utilities such as computers, medical appliance. THD, steady state error of the output voltage and fast dynamic response are important performance indices of the inverter system. As discussed in the literature

review, many control methods have been proposed such as innovative PWM modulation techniques, voltage feedback control, deadbeat control, sliding-mode control and neural networks control. Control methods with innovative PWM modulation techniques and voltage feedback control methods encountered poor regulation problem with a nonlinear load and slow dynamic response when large load change takes place. Deadbeat control could achieve a fast response, but its tracking performance is highly dependent on the accuracy of the model parameters. Modern control methods like sliding-mode control and neural networks control could obtain an output voltage with a low THD and a small steady state error. However, they face the problem of acquiring precise information of the system model, state variables or a large pattern database. Repetitive control which is perfect for periodic error minimization of the inverter system has a slow dynamic response. Therefore, two hybrid control schemes which take the advantage of fast dynamic response of deadbeat control during transient conditions and good steady-state response of repetitive control are proposed in this thesis.

1.4 Main Contribution of the Thesis

We summarize the key contributions of this thesis as follows.

- We have proposed a time domain based repetitive control scheme for DC-AC inverter system. Significant reduction of tracking error of load voltage is achieved using this control scheme. The plug-in repetitive controller is

combined with a cascaded deadbeat controller. Load disturbance compensation and load voltage feed-forward signal enhance the ability of maintaining voltage regulation with any load conditions. The proposed scheme has the advantages of both deadbeat control–fast response and repetitive control–good steady state response. In addition, repetitive control makes up for the deficiencies of deadbeat controller which is caused by variation of model parameters.

- The effect of learning gain of the performance of the time domain based repetitive control has been investigated through analysis. A simplified model of the time domain base repetitive control inverter system is developed to analyze the stability of the system. The learning gain is chosen to guarantee a stable control system and as large as possible to get a fast dynamic response and a small steady state tracking error of the output voltage.

- We also proposed a novel frequency domain based repetitive control scheme which is applied for inverter system for the first time. It solves the problem of compensating for each frequency components properly due to different phase delays caused by filters. It also gives the freedom of choosing different learning gains for each frequency component. Because of these factors, the steady state performance is further improved as compared to that using the time domain based repetitive controller.

1.5 Outline of the Thesis

The thesis is organized as follows.

The background and literature review of the research are presented in Chapter 1.

In Chapter 2, the model of a DC-AC inverter is developed. The design of a cascaded deadbeat controller is then presented. The advantages and disadvantages of the proposed controller are discussed. Simulation results using MATLAB and SIMULINK and experiment results are shown to evaluate the effectiveness of the cascaded deadbeat controller. The specifications of experimental implementation including hardware and software environments are described as well.

In Chapter 3, the basic principle of operation of the repetitive control is presented. A time domain based repetitive controller for a DC-AC inverter system is proposed. The convergence condition of the proposed controller is analyzed and discussed. Simulation results are given to show the effectiveness of the repetitive controller.

In Chapter 4, the frequency domain based repetitive control algorithm is shown first. Design and implementation of frequency domain based controller in inverter are discussed. A comparison of time domain and frequency domain controllers is provided in aspect of both design and system performance in simulation.

Chapter 5 presents the concluding remarks and future research directions.

Chapter 2

Mathematical Model of the Inverter System

2.1 Introduction

Since many of the inverter control schemes require a mathematical model of the inverter, a mathematical model of the inverter is first developed and then subsequently a simplified version of it is presented for controller design propose in this chapter. The load is considered to be resistive when the transfer function of the inverter system is developed. The cascaded deadbeat control of PWM inverter system for a single-phase UPS system is presented. Sinusoidal two-level PWM modulation method is used in generating the gate drive pulse pattern. With the development of power semiconductor device technology, the use of IGBT switch makes high switching frequency PWM inverters with improved control performance at high power level possible. Design of low pass LC filter is also presented in this chapter.

In the inverter control system, high switching frequency of $10\,kHz$ is cho-

sen which could improve the output waveform as much as possible. Generally a switching frequency less than 100kHz is chosen for IGBT power electronics device. A higher switching frequency is not chosen due to the higher loss of the switching devices. Choosing a lower switching frequency may reduce switching loss, but it will bring the drawbacks such as higher ripple current. Bigger LC filters are needed to filter out the lower frequency harmonics. The switching frequency should always more than 20 times output voltage frequency. A lower frequency will also give a slower response to the system. The sampling time period is chosen to be longer than the computation time of digital controller in one cycle. The cascaded control structure with an inner current control loop and an outer voltage control loop is used. This controller is designed based on the model described in [23]. Basically, the outer voltage loop tracks the voltage reference, and the inner current loop controls the inductor current though the inverter. Feed-forward signals such as load voltage (v_o) and load current (i_o) are used to compensate the load disturbance since the load is unknown. Two advantages of this cascaded control structure are: improved dynamic response and capability of suppressing the effect of load variation. However, since the controller is model based, the controller gains are dependent on the accuracy of model parameters. Moreover, when the load changes, the system model will change accordingly since the load impedance varies. Therefore, a model based control method could not reject the load disturbance very well. Simulation program using the MATLAB programming language and SIMULINK toolbox have been developed. Simulation results with an open-loop feed-forward control scheme and the proposed feedback controller for linear and nonlinear loads are presented

and compared.

2.2 Model of DC-AC Inverter

A block diagram of digital control for PWM inverter is shown in Fig. 2.1. The digital controller generates switching signals to control the PWM inverter switches so that the output voltage tracks the sinusoidal reference at each sampling instant.

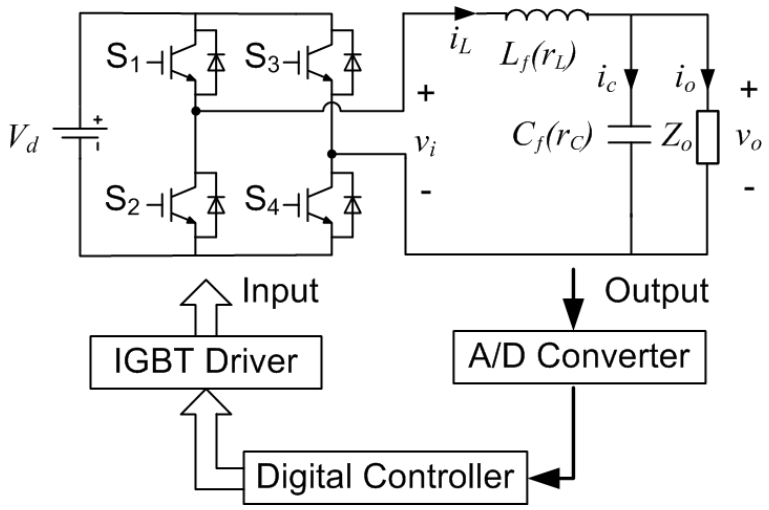


Figure 2.1: Block diagram of digital control for PWM inverter

Either a half-bridge inverter, containing two switches in one leg, or a full-bridge inverter, with four switches in two legs, could be used to convert DC voltage to AC form. However, the half-bridge inverter has two disadvantages: (1) two large capacitors on the DC side is required to provide a midpoint in DC power side to be connected as the negative point of output AC power; (2) to generate the same amplitude of output voltage, half-bridge inverter needs twice of DC voltage level as compared to that a full-bridge inverter needs. Therefore, we have adopted a full-bridge inverter in this research work.

The full-bridge inverter consists of two legs. Two switches in each leg are switched in such a way that they are never turned on simultaneously. In practice, to prevent short circuiting of the dc input, there is a short time period, known as dead-time, is provided for the two switches in one leg. This allows enough time for one switch to turn-off before the other switch being turned on. This is a source of distortions in the output voltage. However, the amplitude of voltage dropping or increasing caused by dead-time effect are not so significant [5], since the dead-time interval is chosen to be only a few microseconds for IGBTs.

2.2.1 Bipolar Voltage PWM Modulation

PWM with bipolar voltage switching is used in this work. The switching signals are generated by comparing the triangular carrier signal waveform v_{tri} with the sinusoidal control signal $v_{control}$. When $v_{control} > v_{tri}$, S1 and S4 are turned on simultaneously, while S2 and S3 are turned off. When $v_{control} < v_{tri}$, S2 and S3 are turned on, and S1 and S4 are turned off. Inverter output voltage v_i in Fig. 2.1 has two polarities, which are positive when S1 and S4 are on, negative when S2 and S3 are on. v_i is derived as [5]

$$v_i = \frac{V_d}{\hat{V}_{tri}} v_{control} \tag{2.1}$$

where V_d is dc link voltage, and $\hat{V}_{tri}$ is the amplitude of the triangular carrier waveform.

In sine PWM modulation technique, modulation signal has the desired fundamental frequency f_1 of the inverter output voltage and the peak amplitude $\hat{V}_{control}$.

Carrier signal is a triangular waveform at switching frequency f_s and peak amplitude $\hat{V}_{tri}$. The corresponding modulating signal, carrier signal and the corresponding gating signals are shown in Fig. 2.2. The amplitude modulation ratio m_a and

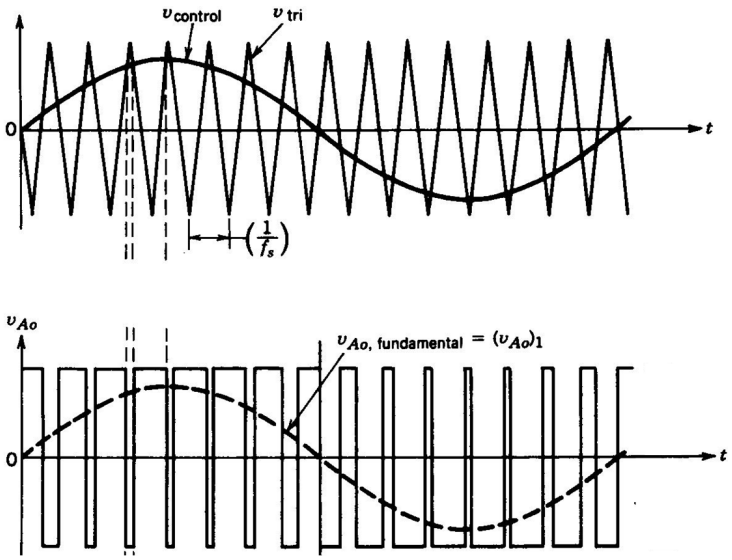


Figure 2.2: Pulse width modulation

the frequency modulation ratio m_f are defined as

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{2.2}$$

$$m_f = \frac{f_s}{f_1} \tag{2.3}$$

Modulation signal varies sinusoidally at $f_1 = \omega_1/2\pi$, thus

$$v_{control} = \hat{V}_{control} \sin \omega_1 t \tag{2.4}$$

where $\hat{V}_{control} \leq \hat{V}_{tri}$. Substituting m_a into eqn. 2.1, the fundamental frequency component of PWM output of the inverter $(V_i)_1$ is

$$(V_i)_1 = m_a V_d \sin \omega_1 t \qquad \text{for } m_a \leqslant 1.0 \tag{2.5}$$

Eqn. (2.5) shows that in the range of m_a from 0 to 1, the amplitude of fundamental-frequency component of the output voltage varies linearly with m_a. In the linear range, harmonics of v_i centers around the switching frequency f_s and its multiples as sidebands. Over-modulation range $m_a > 1.0$ causes the output voltage to contain many more harmonics in the sidebands as compared with the linear range. Therefore, in this research, m_f is set to 200 which is large enough to "push" the harmonics to high frequency range, and $m_a = 0.7$ to keep it in the linear range. At the same time, a low m_a reduces the maximum duty cycle in PWM modulation.

2.2.2 Mathematical Model of the System

A linear resistive load R is considered when modelling the inverter-filter system. In practice, inductor L and capacitor C have their equivalent series resistance (ESR) r_L and r_C respectively. The inverter, LC filter, and load are considered as the plant of the closed-loop control system. A block diagram of the plant is shown in Fig. 2.3. From the block diagram,

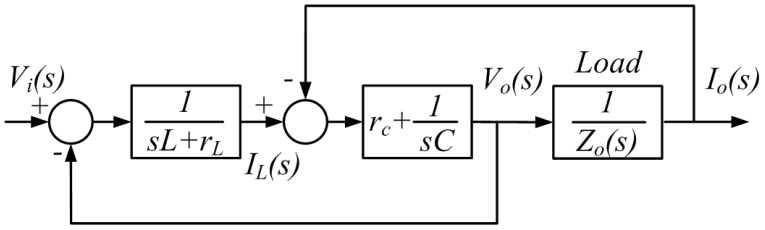


Figure 2.3: Block diagram of the system plant

$$I_L(s) = \frac{V_i(s) - V_o(s)}{sL + r_L} \tag{2.6}$$

$$V_o(s) = (I_L(s) - I_o(s))(r_C + \frac{1}{sC}) \tag{2.7}$$

$$I_o(s) = \frac{V_o(s)}{Z_o(s)} \tag{2.8}$$

Transfer function of LC filter is derived from (2.6)-(2.8)

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{(sL + r_L)/(r_C + 1/(sC)) + (sL + r_L)/R + 1} \tag{2.9}$$

Cutoff frequency of the LC filter can be presented simply as

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.10}$$

Incorporating (eqn. 2.1), transfer function from control signal to output voltage is

$$\begin{aligned} \frac{V_o(s)}{V_{control}(s)} &= \frac{V_o(s)}{V_i(s)} \frac{V_i(s)}{V_{control}(s)} \\ &\cong \frac{r_C C s + 1}{(LC + r_C LC/R)s^2 + ((r_L + r_C)C + (r_L r_C C + L)/R)s + r_L/R + 1} \cdot \frac{V_d}{\hat{V}_{tri}} \end{aligned}$$

2.3 Real-Time Implementation

The proposed control schemes were implemented on an 1 kVA IGBT PWM voltage-source inverter using a dSPACE 1104 controller board. Fig. 2.4 shows the configuration of the experimental setup. The DSP control board executes commands from the PC and generates PWM gating signal to control the inverter system. Feedback signals such as v_o and i_L are captured by sensor board and filtered where required, and fed into DSP DAC I/O ports. The program codes, in which the control algorithm are contained, are written in C language.

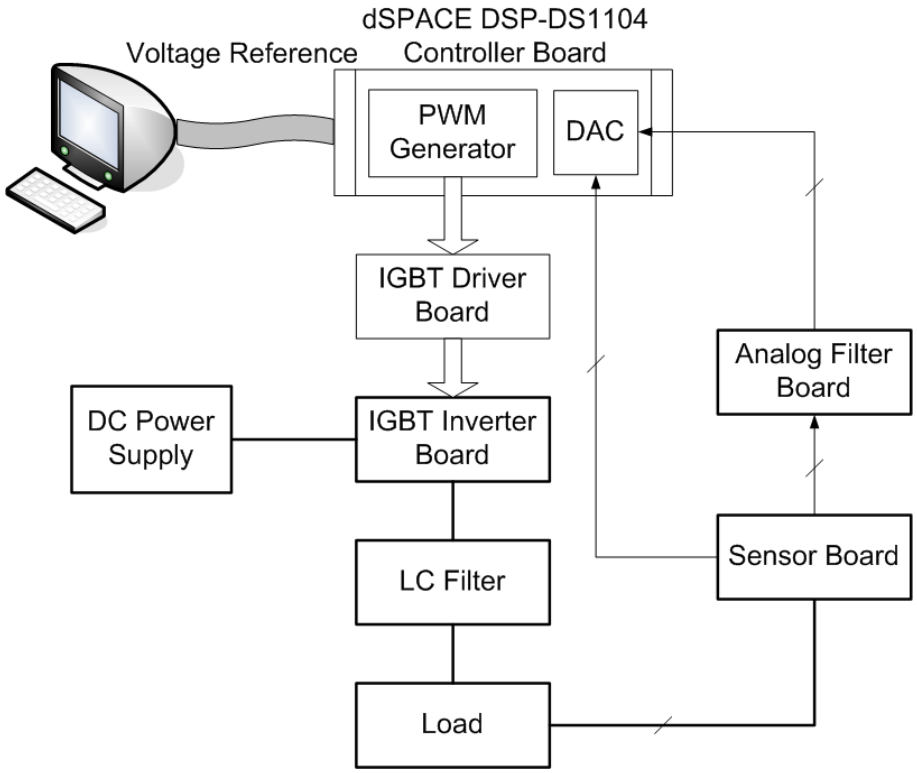


Figure 2.4: Hardware implementation platform

2.3.1 System Hardware

The photograph of the experimental setup is shown in Fig 2.5. The whole platform comprises of the followings:

- Pentium III PC for rapid-prototyping and real-time control
- dSPACE DSP-ds1104 controller board for running control programs, generating control signals, sampling feedback signals and communicating with the computer
- Voltage source inverter including a IXYS MUBW 10-12 converter-brake-inverter module and two SEMIDRIVER SKHI 24 hybrid dual IGBT drivers

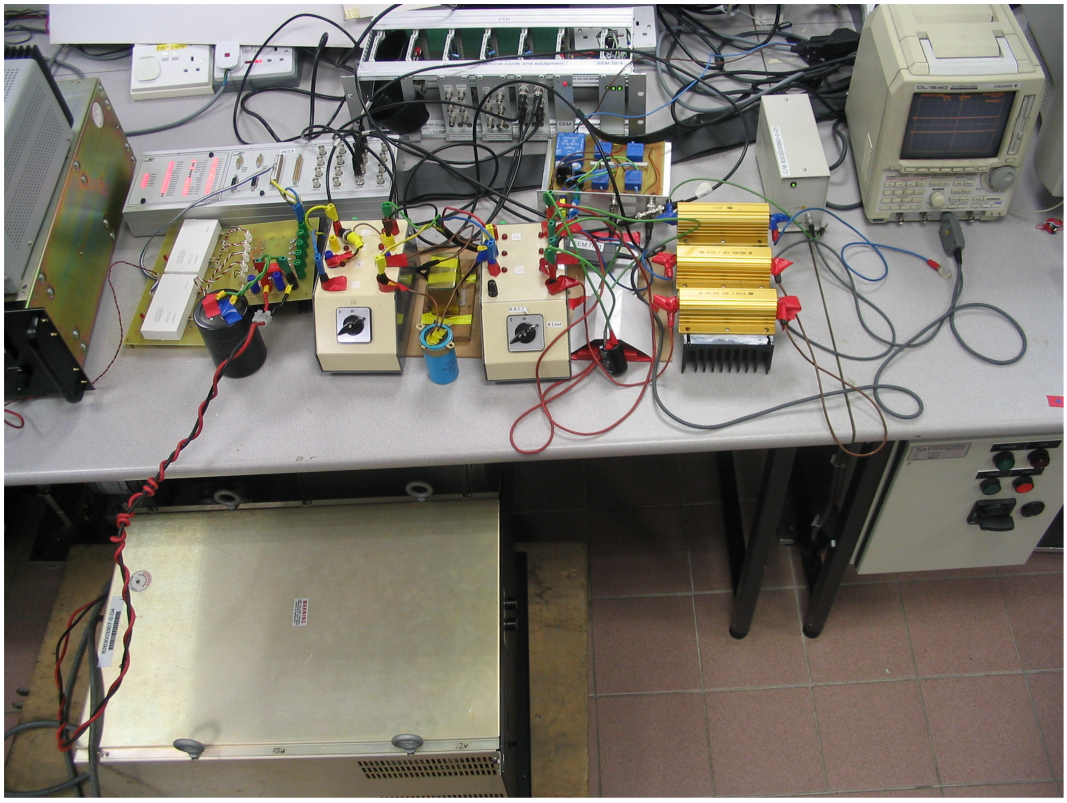


Figure 2.5: Photograph of the inverter control system used in experiment

- Sorensen DCR 600-16T DC power supply
- Sensing devices including a voltage transducer LEM LV25-P and 2 Current transducers LEM LA25-NP
- LC filter
- Resistor load and a rectifier load
- Analog filter card
- Fluke 41B Power Harmonics Analyzer

2.3.1.1 Controller Board

The dSPACE DS1104 controller board is specially designed for research and development works having features for simulation and real time implementation of digital controllers in various fields. The DS1104 board consists of PowerPC 603e microprocessor as main processor and TMS320F240 as slave DSP. The main processor runs at 250 MHz and controls ADC unit, DAC unit and 20-bit I/O, incremental encoder and serial interface. The slave DSP runs at 20 MHz and controls 14-bit digital I/O unit, PWM and serial peripheral interface. The A/D converters convert the analog feedback signals of $\pm 10\,V$ into digital format. Voltage and current feedback signals are read by the DSP. PWM gating signal generator converts the digital signal commands in DSP into analog signals of $\pm 10\,V$ in order to control the inverter switches. The DS1104 controller board is inserted into the PCI slot of PC. Using software ControlDesk for communications between PC and the microprocessor, user can debug the user-program that is loaded in the DSP (via C programming and the Texas Instruments C Compiler), tune the experimental parameters on-line and display the variables in the experimental set up in real-time (via ControlDesk). The detailed architecture of DS1104 board is given in Appendix A.

2.3.1.2 Inverter

A single-phase, 1 kVA PWM inverter is used as the power circuit for the system. Table 2.1 shows the parameters of the inverter system. The inverter consists of a IGBT module (MUBW 10-12A7), DC-link capacitors and driver board. The driver

Table 2.1: Experimental Parameters

Filter inductance	L=614 μH, r_L=1.7 Ω
Filter capacitance	C_f=125 μF, r_C=0.925 Ω
DC input voltage	V_c=100 V
Modulation Factor	m_a=0.7
Reference voltage	V_{peak}=70 V, f=50 Hz
Linear load resistance	R=10 Ω
Rectifier load resistance	R=45 Ω
Rectifier load capacitance	C=1200 μF

board consists of two SEMIDRIVER SKHI 24 hybrid dual IGBT driver modules. Each driver module controls two switches in one leg. All devices necessary for driving, voltage supply, error monitoring and potential separation are integrated in the driver. In case of shoot-through in upper and lower IGBT in the same leg or a high value of V_{CE} detected, the driver will turn off the switching device. It also provides a digitally adjustable dead-time. Details of the inverter and driver are given in Appendix B.

2.3.1.3 Filters and Sensors

Two low-pass analog filters are used for voltage and current feedback signals. One analog card integrates the two simple resistive-capacitive op-amp filters. The cut-off frequency of the voltage feedback signal filter and current feedback signal filter are 1 kHz and 500 Hz respectively. Details of the analog filter board is included in Appendix C.

Accurate measurements of feedback signals are important in a closed-loop

control system. DSP limits its input I/O in the range $\pm 10\,V$. Therefore, current and voltage transducers are used to scale down voltage or current signal to voltage signal in the range of $\pm 10\,V$ by using appropriate resistances. LEM LV25-P and LA25-NP are used in the sensor board. Specifications of the sensor board are given in Table 2.2.

Table 2.2: Specifications of sensor board

	Module Name	Resistance in Original Side	Resistance in Secondary Side	Ratio
Voltage Sensor	LV25-P	$12\,\text{k}\Omega$	$400\,\Omega$	120:10
Current Sensor	LA25-NP	–	$400\,\Omega$	25:1

The LC filter components are chosen based on the cut-off frequency of the filter, efficiency, components size and cost. Generally the inductive voltage drop should not be more than 5 - 10% of the output voltage at rated current and accordingly the inductor value is chosen. Therefore for this application, the second order filter inductance should be around $600\,\mu H$. In simulation and experiment, switching frequency f_{sw} and output voltage frequency f_O are chosen to be $10\,kHz$ and $50\,Hz$ respectively. Increasing the cut-off frequency may allow more low frequency components pass to the output voltage and cause more distortion of the output voltage. Decreasing f_{sw} requires larger size of the filter components. Therefore cut-off frequency f_c is chosen as $f_{sw} \gg f_c \geq 10 f_O$, in this thesis experiment around $500\,Hz$. Eqn. 2.10 shows the calculation of cut-off frequency of the filter. Based on the chosen inductor value and Eqn. 2.10, we could decide the capacitance value to $120\,\mu F$ according to cutoff frequency.

2.3.1.4 Load Systems

Linear resistive and nonlinear rectifier loads are used to test the system performance in this research work. We use a power resistor for linear load. For nonlinear load, a diode bridge rectifier with resistor and capacitor connected parallel in DC side, are shown in Fig. 2.6. 25ETF fast soft recovery QUIET**IR** rectifier is used in the experimental setup.

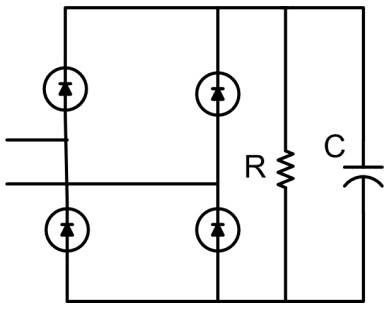


Figure 2.6: Rectifier nonlinear load

2.3.1.5 THD measurement

THD was measured using power meter device Fluke 41B Power Harmonics Analyzer. Its accuracy is +/-3 %Reading. Output voltage data were captured and calculated according to Eqn. 2.11.

$$\text{THD}_{\text{voltage}} = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1} \times 100\% \tag{2.11}$$

since $V_{rms}^2 = V_1^2 + \sum_{h=2}^{\infty} V_h^2$. They are consistent with the measuring result by using power meter. Since In a word, THD is calculated by knowledge of rms value of the output voltage and fundamental value of the voltage, taking account of all the harmonics.

2.3.2 Software Environment

The entire control program for the implementation of this research work is written in C language. Using C programming, the user has the freedom to optimize the source codes so that it results in the lowest execution time; hence, achieving a fastest sampling time. Moreover, in *dSPACE* rapid-prototyping software, RTW automatically generates C codes from the SIMULINK block diagrams. C codes generated from RTW results in significantly higher program execution times than those in user-optimized C programs, and therefore the control algorithms are written in C-codes.

Fig. 2.7 presents the flowchart of the main control program that is implemented in C. All the control programs are implemented within the interrupt service routine (ISRT). At every interrupt the program code executes once and returned to the top when the next interrupt generates. The flowchart for the Interrupt Service Routine is shown in Fig. 2.8, and the flowchart of the learning control part is shown in Fig. 2.9.

The master PowerPC (PPC) converts the C source code into assembly language source codes by compiling, assembling and liking C source code modules, when the C coded control program is downloaded to the processor. Then the assembler translates the assembly language source codes into machine language object files. The object files are then loaded into the DSP, and the DSP begins program execution. When the program execution begins, using the software ControlDesk,

the user is able to modify the process variables, control parameters on-line, or to monitor process variables. At the same time, real-time process variables can be acquired by ControlDesk for storage or display purposes. While rapid prototyping is implemented easily using ControlDesk, it consumes a significant amount of processing time, and hence, it substantially limits the fastest sampling time of the system.

DSP TMS320F240 has a high speed CPU and adequate memory for software implementation. Fig. 2.10 shows the interactions among the software during the DSP program execution.

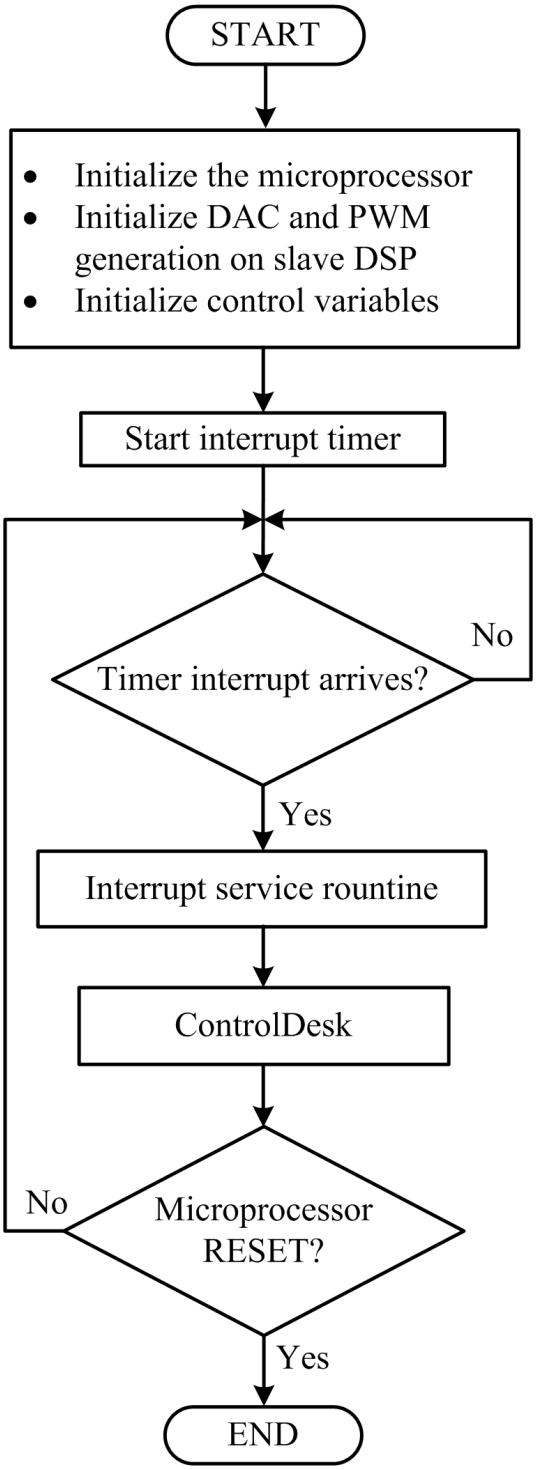
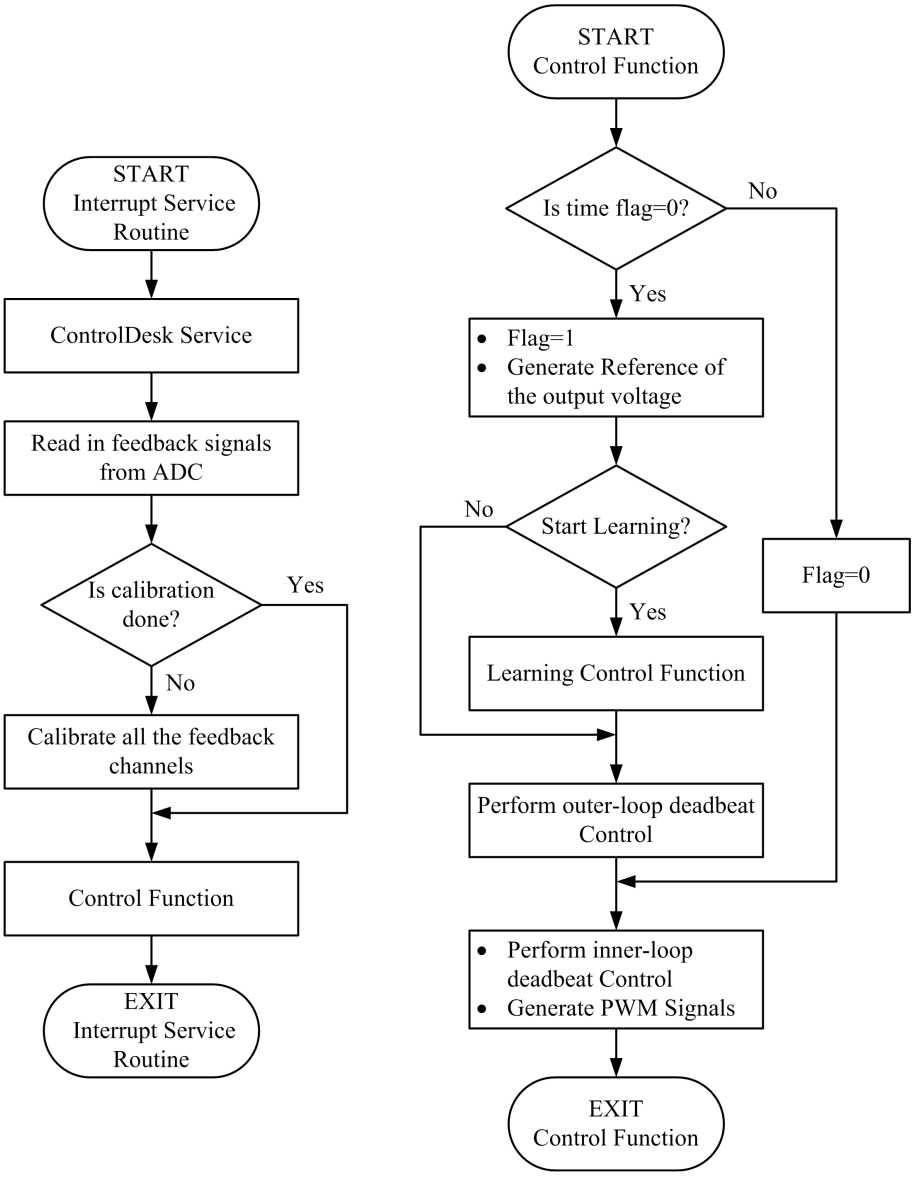
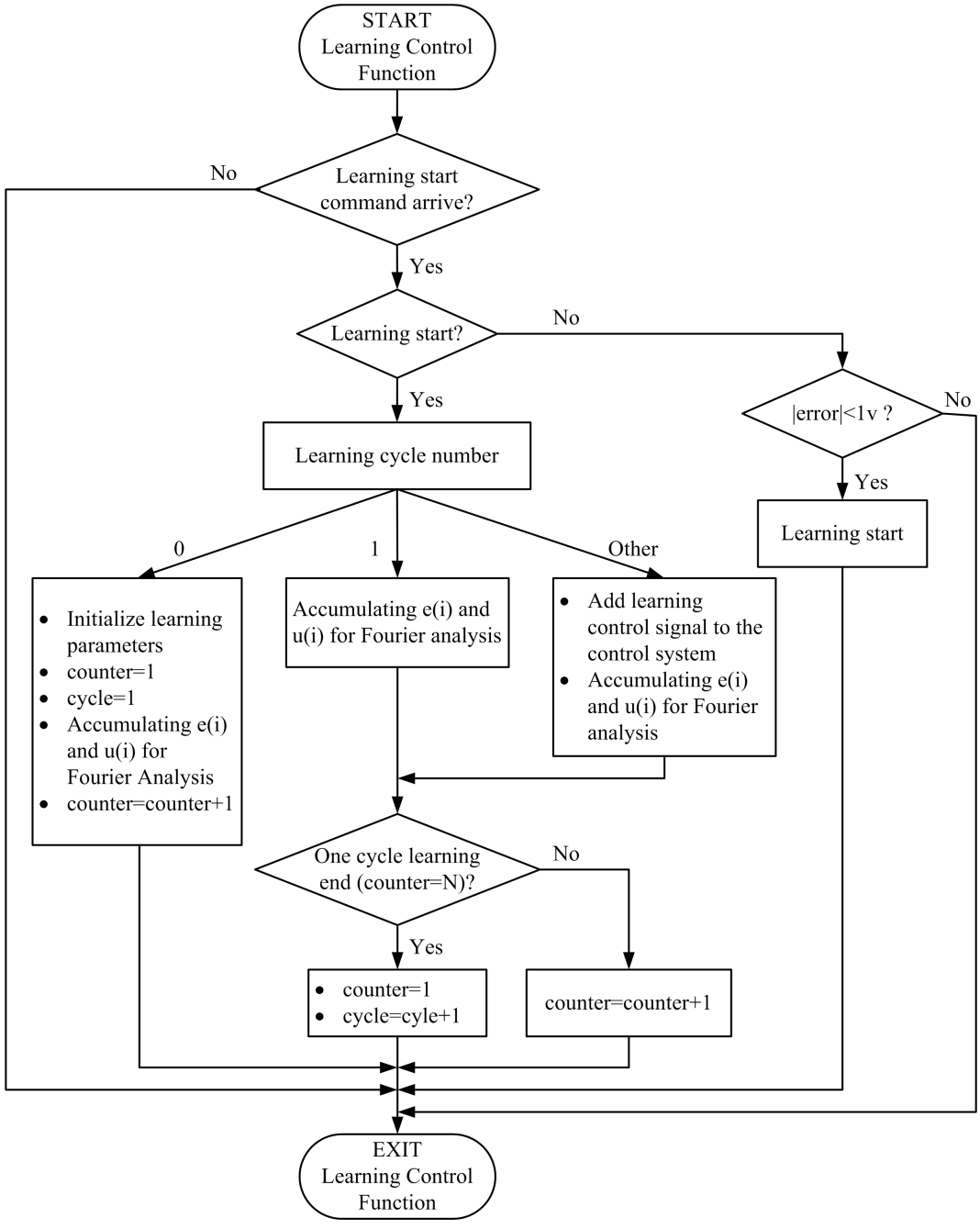


Figure 2.7: Flowchart of the main control program



(a) Flowchart of ISRT (b) Flowchart of Control Function

Figure 2.8: Flowchart of the interrupt service routine



(b) Flowchart of Learning Control Function

Figure 2.9: Flowchart of the learning control function

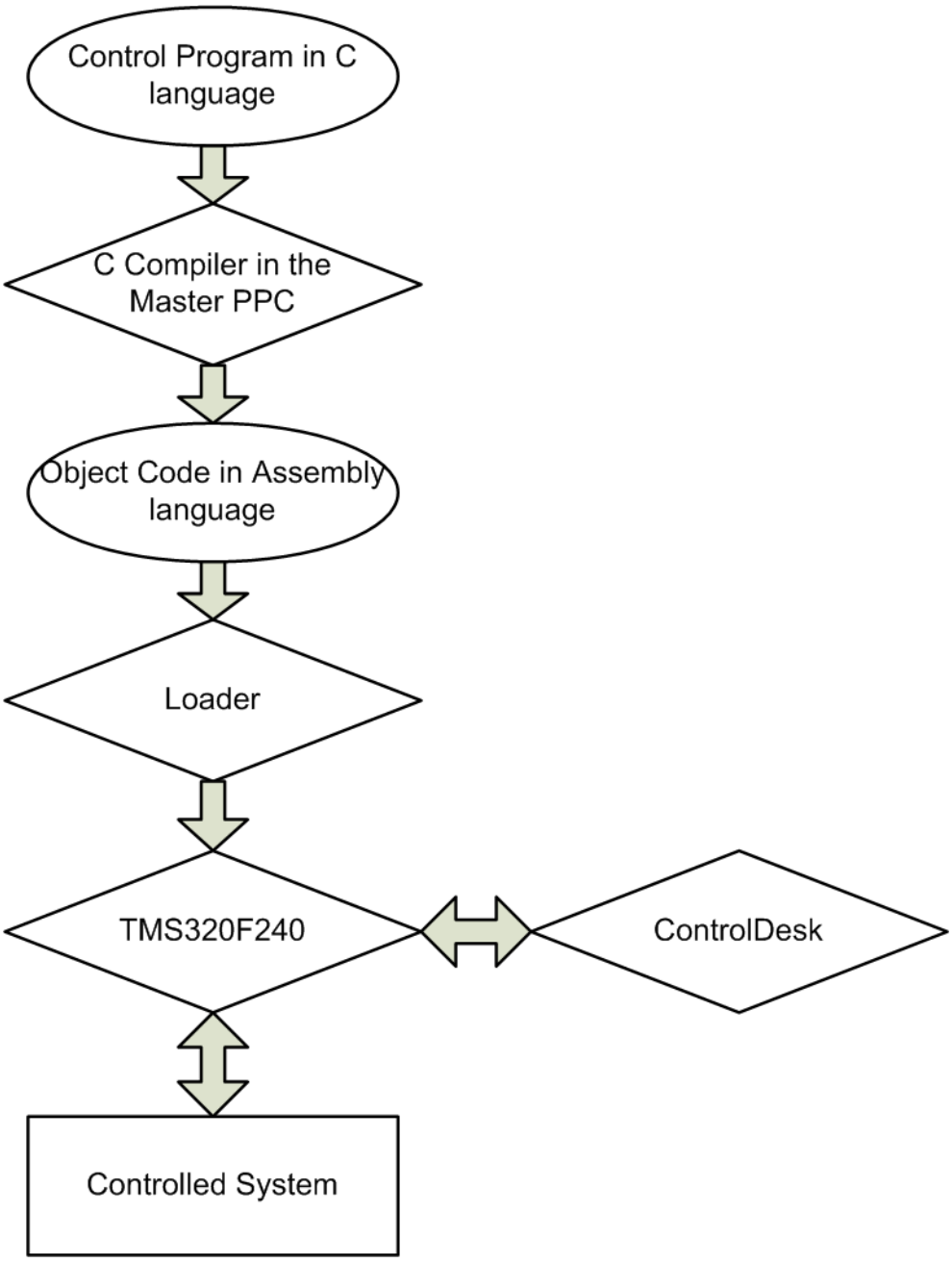


Figure 2.10: Real-time executable code generation

2.4 Cascaded Deadbeat Control for Inverter

In this section, we present a cascaded deadbeat control scheme which provides good and fast dynamic performance for load disturbance. Deadbeat control is a control technique devised by Gokhale [37][38][10] based on deadbeat control theory [39]. The digital controller places closed-loop poles in discrete time domain to the origin so that the output is corrected within several sampling intervals, which are determined by the order of system. This could not be implemented possibly in continuous time domain because one cannot place poles to negative infinity in S-plane. Thus, the PWM duty cycle is determined at every sampling instant by the digital signal processor (DSP) based on the feedback and the reference. This control method provides very good voltage regulation, and fast dynamic response for disturbances, however it requires full knowledge of the plant, and the good performance is highly based on the accuracy of model parameters.

The block diagram of the proposed scheme is shown in Fig. 2.11. It consists

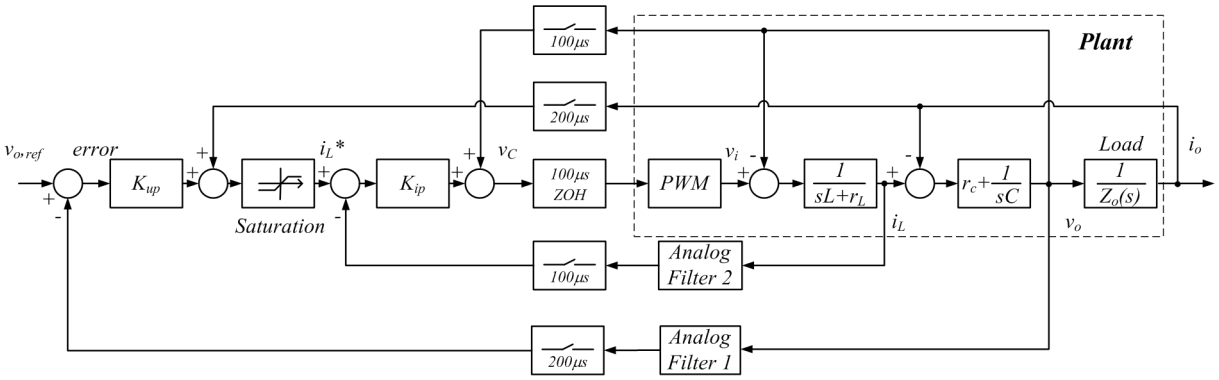


Figure 2.11: Block diagram of cascaded deadbeat control

of two loops: the outer voltage loop tracking the voltage reference, and the inner

current loop controlling the inductor current in the inverter [23]. Feed-forward signals such as load voltage (v_o) and load current (i_o) are used to compensate load disturbance since the load condition is unknown.

2.4.1 Inner Loop Current Controller Design

Inner current-loop block diagram is shown in Fig. 2.12. From Fig. 2.12 (a), we can

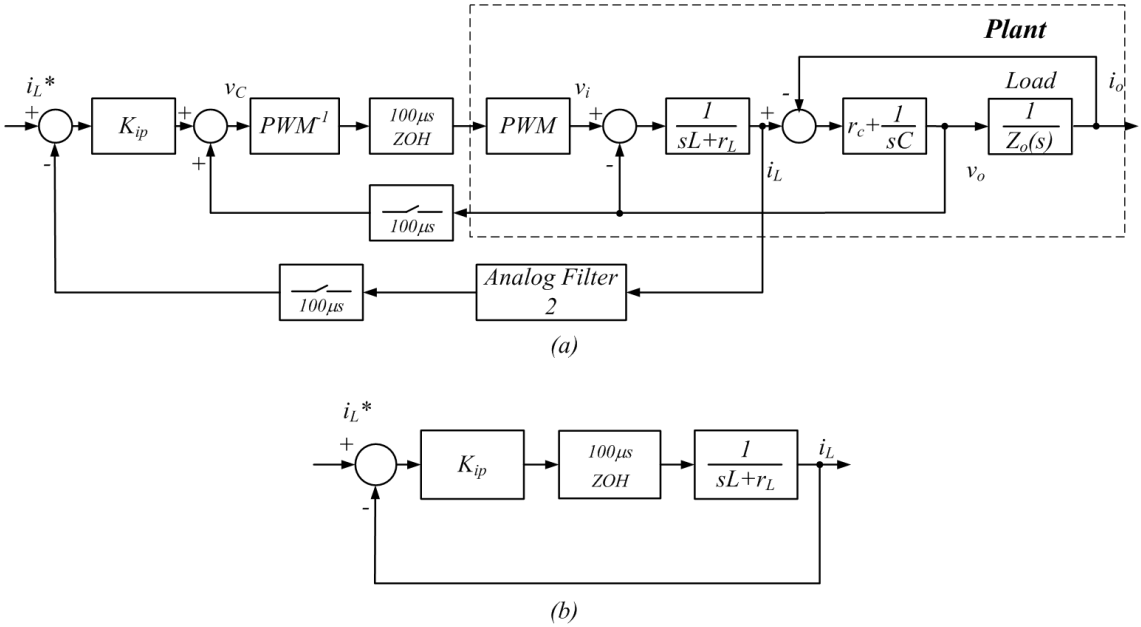


Figure 2.12: (a) Block diagram of current inner-loop (b) simplified block diagram

see in current inner loop, the negative "disturbance" v_o which is injected to the plant is compensated by a positive feed-forward signal v_o added in the digital controller. The effect of v_o is suppressed to improve the performance of inner control loop. Hence, by ignoring the effect of v_o the model of the inner-loop can be simplified as in Fig. 2.12 (b).

The open-loop transfer function is

$$\begin{aligned} G_i(z) &= Z\left(K_{ip}\left[\frac{1-e^{-T_i s}}{s}\right]\left[\frac{1/L}{s+a}\right]\right) \\ &= \frac{K_{ip}}{r_L}\frac{1-e^{-aT_i}}{z-e^{-aT_i}} \end{aligned} \tag{2.12}$$

where $T_i = 100\,\mu s$ is the sampling time of the current inner loop, and $a = r_L/L$.

The analog filter 2 of inductor current feedback shown in Appendix C is neglected in this study. The characteristic equation of the closed current loop is

$$z - \left[e^{-aT_i} - K_{ip}\left(\frac{e^{-aT_i}-1}{r_L}\right)\right] = 0 \tag{2.13}$$

The gain K_{ip} is designed to as follows to place the pole to the origin,

$$K_{ip} = \frac{r_L e^{-aT_i}}{1-e^{-aT_i}} \tag{2.14}$$

With the well tracking of inductor current, the outer voltage loop can be easily designed by assuming the inner current-loop controller as a constant gain. The assumption is based on the condition that the sampling speed of outer loop is slower than the speed of inner loop and that the plot of magnitude and phase in control bandwidth are flat in bode diagram of the closed inner loop model. However, due to the effect of analog filter, the closed-loop characteristic polynomial is not a simple first order one. In our experiment, we made use of a second order analog filter. The two closed-loop bode diagrams with and without analog filter are shown in Fig. 2.13. It could be clearly seen that in both magnitude and phase, precise model reveals that large variation in frequency range which is higher than

$300\,Hz\,(1885\,rad/sec)$. It means that in practice, deadbeat controller may not make the system output track the reference accurately.

2.4.2 Outer loop Voltage Controller Design

In outer voltage-loop design, the inner current-loop is assumed to be a constant gain when designing the voltage loop controller as mentioned before. Block diagram of the current inner-loop is shown in Fig 2.14. In Fig 2.14 (a), unknown load current i_o is seen as a disturbance to the outer loop. Compensation i_o is added to suppress the load disturbance. Neglecting the analog filter dynamics, the outer loop is simplified as shown in Fig 2.14 (b), and the open-loop transfer function is given as follows

$$\begin{aligned} G_i(z) &= Z\left(K_c \cdot K_{up}\left[\frac{1-e^{-T_u s}}{s}\right]\left[r_C + \frac{1}{sC}\right]\right) \\ &= K_c \cdot K_{up}\left[r_C + \frac{T_u}{C(z-1)}\right] \end{aligned} \tag{2.15}$$

where K_c is the equivalent gain of current inner loop, $T_u = 200\,\mu s$ is the sampling time of the outer voltage loop. We place the closed-loop pole at origin to achieve deadbeat effect. The gain K_{up} is designed as

$$K_{up} = \frac{C}{K_c \cdot (T_u - C \cdot r_C)} \tag{2.16}$$

Similarly, the cancellation of load disturbance is not perfect because of presence of the analog filter and also due to measurement inaccuracies.

Table 2.1 and Table 2.3 give the parameters of the single-phase DC-AC inverter control system and the cascaded deadbeat controller used in all the simulation and experiment in this thesis.

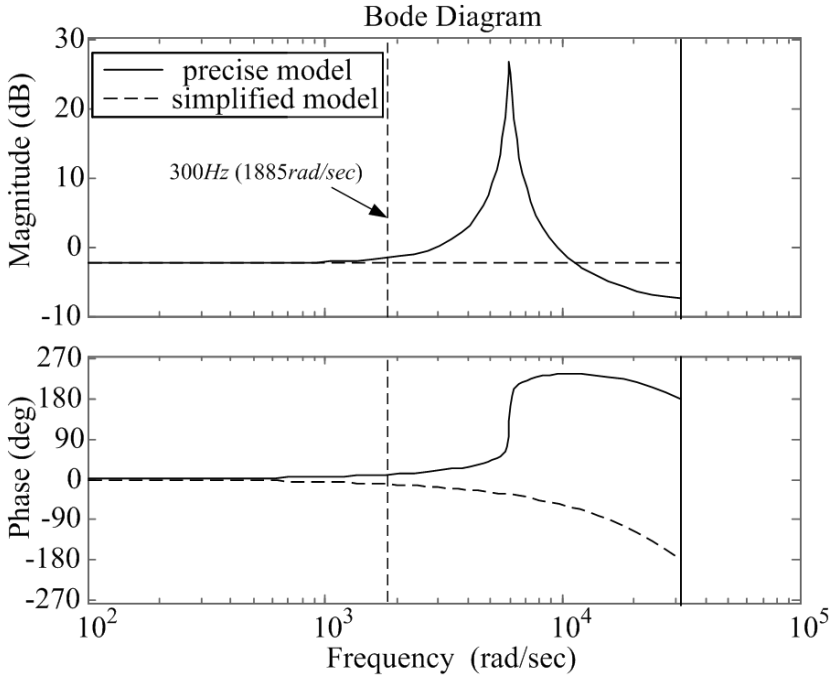


Figure 2.13: Bode diagram of a precise and a simplified closed current loop model

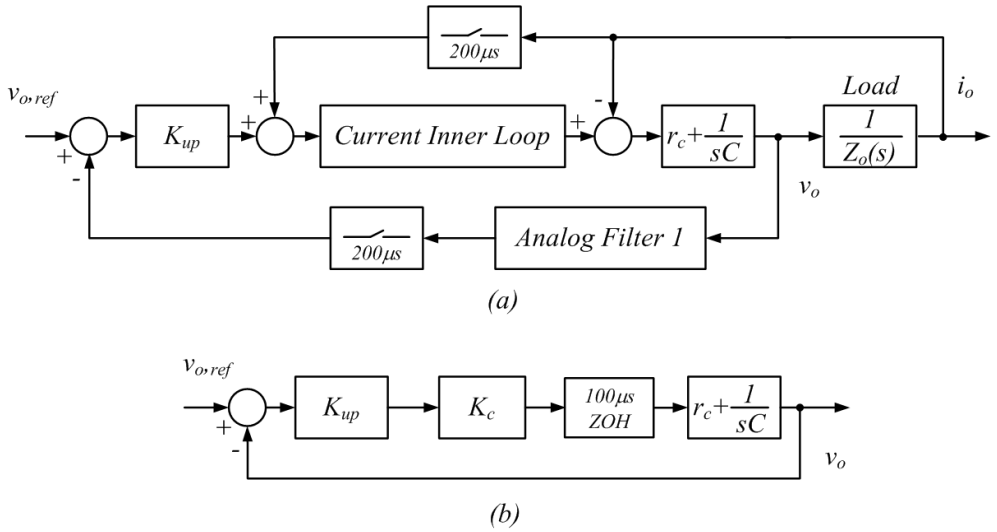


Figure 2.14: (a) Block diagram of voltage outer-loop (b) simplified block diagram

Table 2.3: Controller Parameters

Voltage loop gain K_{up}	0.48
Current loop gain K_{ip}	5.3
Sampling frequency	f_s=10 kHz
Switching frequency	f_{sw}=10 kHz

2.4.3 Simulation Results Using Conventional Cascade Deadbeat Control for Inverter

To investigate the performance of the cascaded deadbeat control scheme, in order to compare with the two proposed repetitive control schemes further, simulations were carried out using MATLAB and SIMULINK software package. The IGBT switches of the inverter is substituted by ideal switches that have no power loss. The performance of the control system is evaluated only when the system reaches its steady state condition. Therefore, the tracking error of the output voltage and THD are determined only in the steady state. These two essential parameters in evaluating the performance are compared among the two repetitive control schemes and the conventional cascaded deadbeat control to show the effectiveness of the proposed schemes in harmonic distortions minimization. The performance of inverter system is evaluated with a $10\,\Omega$ resistive full load for linear load and rectifier load with a crest factor of 3. The maximum load current drawn is $10\,A$.

2.4.3.1 Linear Load

When the voltage reference peak value is $70\,V$, simulation results of the steady state output voltage using open-loop control and the conventional deadbeat controller under a linear load are shown in Fig. 2.15 and Fig. 2.16 respectively. Deadbeat control helps the output voltage track the reference more accurately. The tracking error of output voltage using open-loop control and the conventional deadbeat controller under a linear load are shown in Fig. 2.17. The maximum value of the volt-

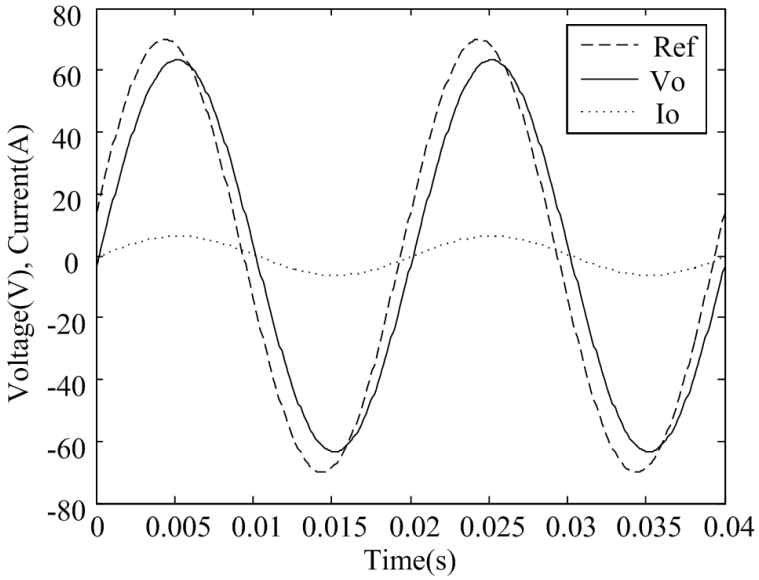


Figure 2.15: Simulation result: steady state output voltage of the inverter system under a linear load using openloop control

age tracking error is reduced from $17\,V$ to $8.9\,V$ as shown in Fig. 2.17. Frequency spectrum of voltage error signal in Fig. 2.18 shows that deadbeat controller minimizes the dominant fundamental frequency component, while the other frequency component magnitudes increase slightly. By reducing the fundamental frequency component of error, deadbeat control scheme introduces the 3^{rd}, 5^{th}, 7^{th}, and 9^{th} harmonic components, therefore THD of deadbeat control increases from $0.2\,\%$ to $0.4\,\%$. Frequency components which are more than $500\,Hz$ are not shown because of their insignificant contribution.

2.4.3.2 Nonlinear Load

The system performance with a nonlinear load is carried out to evaluate its ability to reject load disturbance. With the same parameters in the inverter system, simulation results of the steady state output voltage using open-loop control and

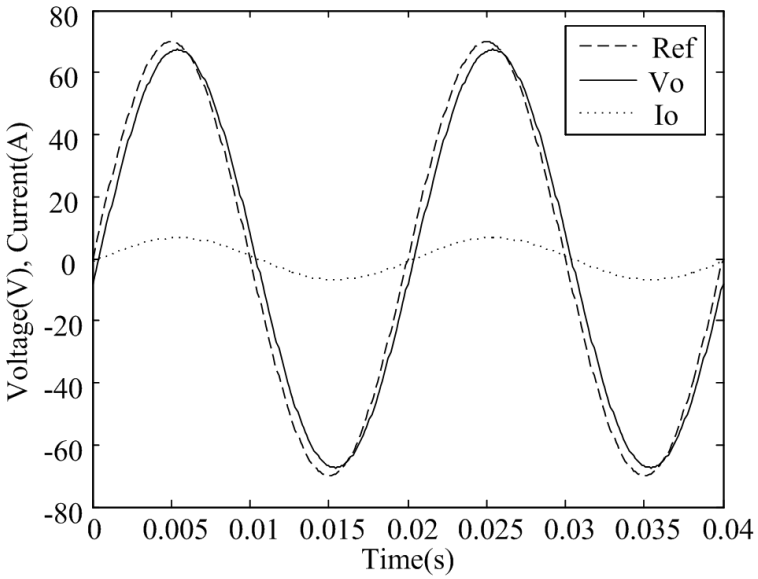


Figure 2.16: Simulation result: steady state output voltage of the inverter system under a linear load using cascaded deadbeat control

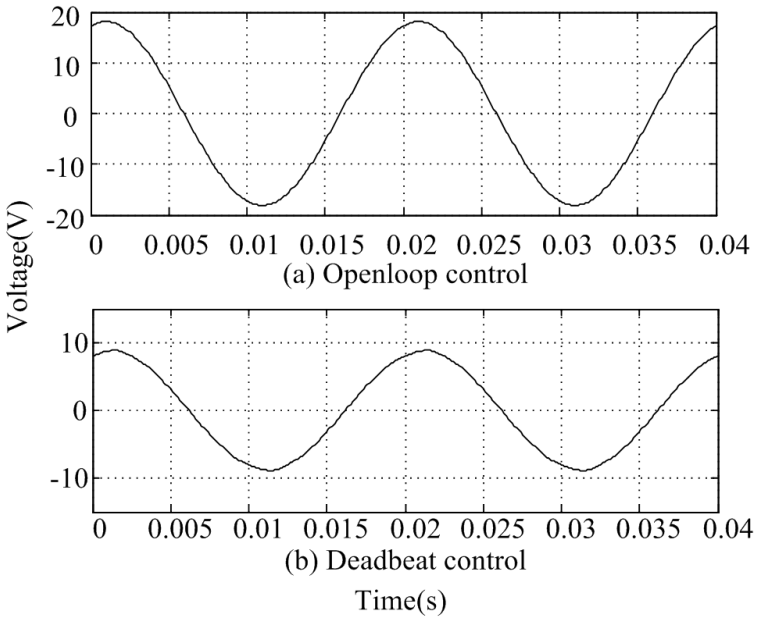


Figure 2.17: Simulation result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using openloop control and (b) cascaded deadbeat control

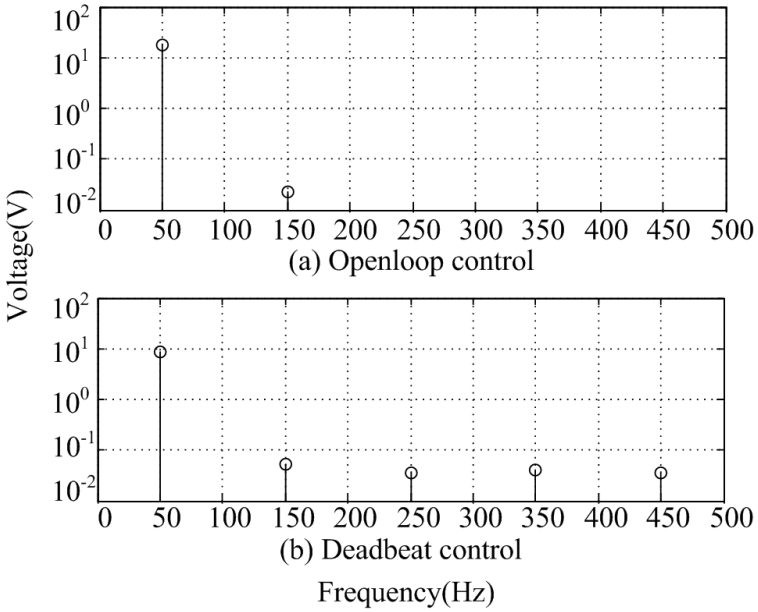


Figure 2.18: Simulation result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using openloop control and (b) cascaded deadbeat control

the conventional deadbeat controller under a nonlinear load are shown in Fig. 2.19 and Fig. 2.20 respectively. Deadbeat control minimizes the magnitude difference between the reference voltage and the output voltage. However, because deadbeat control method is highly dependent on the model which is changed by the load variation, at around the peak values in simulation the deadbeat controller is unable to track the voltage reference. The non-linear load is modelled by a rectifier RC load as shown in Fig. 2.6. In this non-linear model, when the diode bridge in the non-linear load is not conducting, the state space equation is given by Eqn. 2.17 and Eqn. 2.18

$$\begin{pmatrix} \dot{v}_o \\ \dot{i}_L \end{pmatrix} = \begin{pmatrix} 0 & 1/C_f \\ -1/L_f & -R_L/L_f \end{pmatrix} \begin{pmatrix} v_o \\ i_L \end{pmatrix} + \begin{pmatrix} 0 \\ 1/L_f \end{pmatrix} u \tag{2.17}$$

$$v_o = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{pmatrix} v_o \\ i_L \end{pmatrix} \tag{2.18}$$

And when the non-linear load is conducting, which happened around the output voltage peak, the control system model change to Eqn. 2.19 and Eqn. 2.20

$$\begin{pmatrix} \dot{v}_o \\ \dot{i}_L \end{pmatrix} = \begin{pmatrix} -1/((1+C/C_f)C_fR) & 1/((1+C/C_f)C_f) \\ -1/L_f & -R_L/L_f \end{pmatrix} \begin{pmatrix} v_o \\ i_L \end{pmatrix} + \begin{pmatrix} 0 \\ 1/L_f \end{pmatrix} u \tag{2.19}$$

$$v_o = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{pmatrix} v_o \\ i_L \end{pmatrix} \tag{2.20}$$

The deadbeat controller is designed using a linear load model. Thus when the system model suddenly changes during output voltage peak period, the deadbeat controller could not track the output voltage track properly. As compare to Fig. 2.19(open-loop control), the drop in output voltage during load conduction period is less. In conclusion, deadbeat control could not fully reject the load disturbance due to its model based nature.

The tracking error of output voltage using open-loop control and the conventional deadbeat controller under a nonlinear load are shown in Fig. 2.21. The maximum value of error is reduced from $18\,V$ to $7.8\,V$. Frequency spectrum of the output voltage error in Fig. 2.22 shows that deadbeat controller minimizes the dominant fundamental frequency, 3^{rd}, and 5^{th} order harmonic components, and other frequency component magnitudes remain the same or increase slightly. THD of deadbeat control reduce from 6.5% to 3.8%, which shows that the deadbeat control scheme improves the performance significantly under a nonlinear load operation.

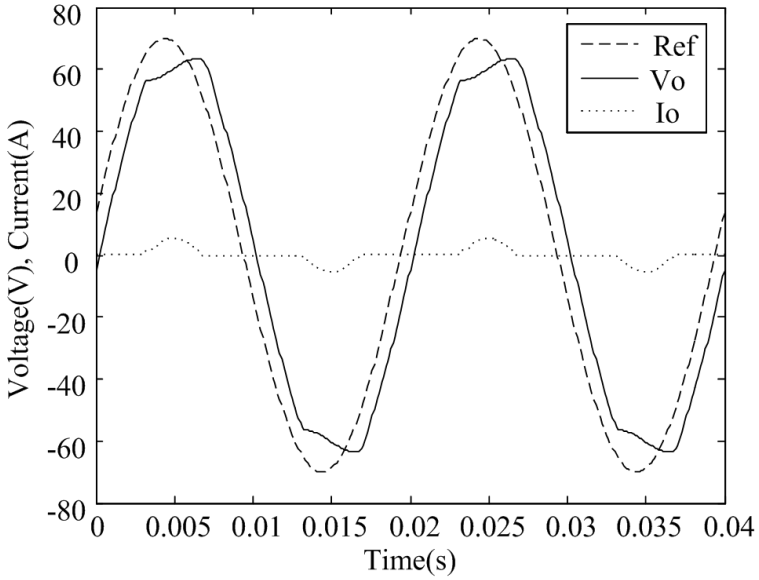


Figure 2.19: Simulation result: steady state output voltage of the inverter system under a nonlinear load using openloop control

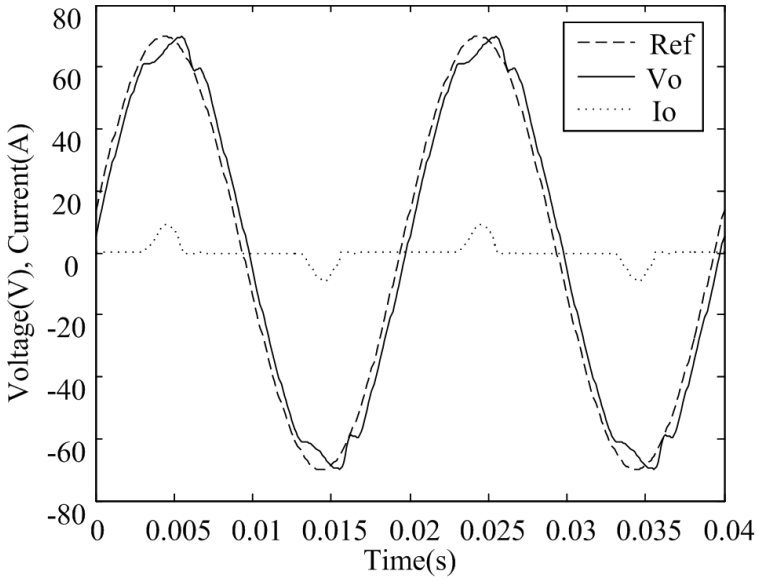


Figure 2.20: Simulation result: steady state output voltage of the inverter system under a nonlinear load using cascaded deadbeat control

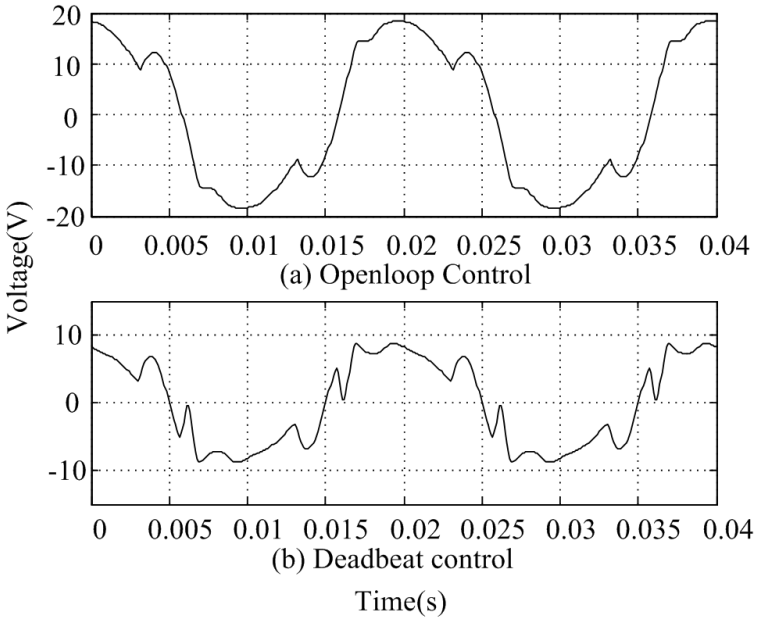


Figure 2.21: Simulation result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using openloop control and (b) cascaded deadbeat control

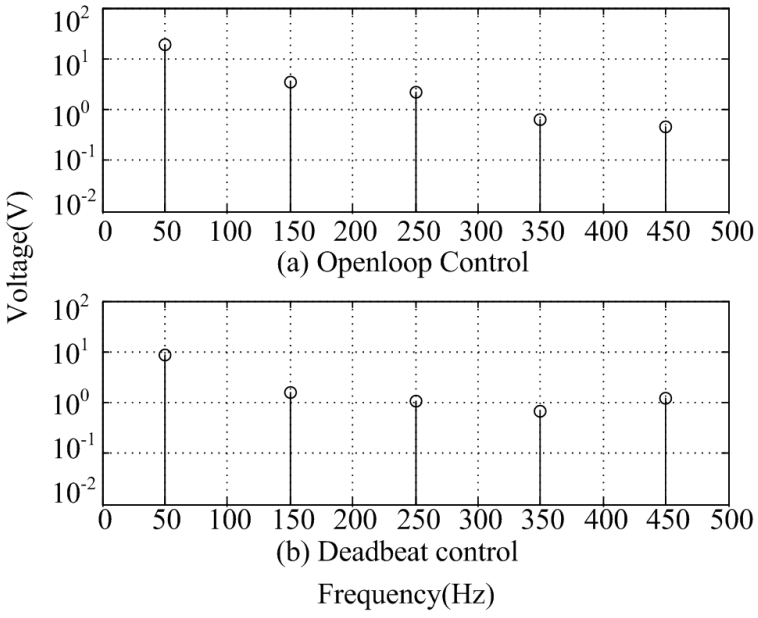


Figure 2.22: Simulation result: error spectrum of output voltage of the inverter system in steady state under a nonlinear load (a) using openloop control and (b) cascaded deadbeat control

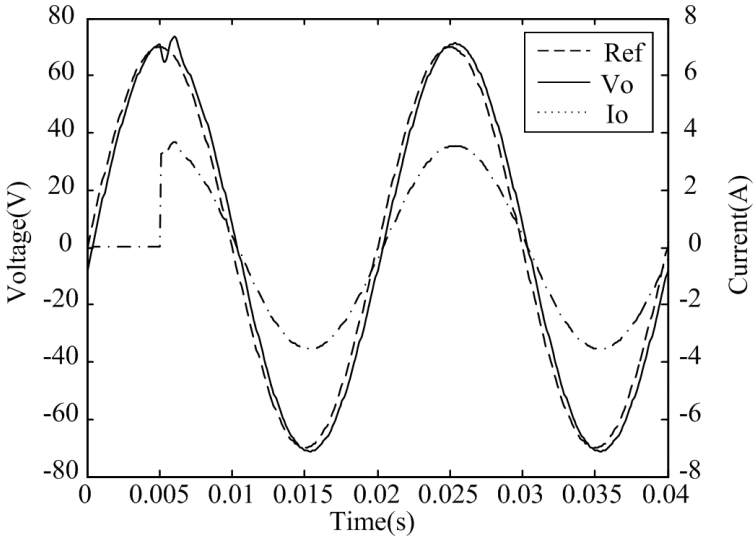


Figure 2.23: Simulation result: Transient response of the inverter system in steady state with a step load using cascaded deadbeat control

2.4.3.3 Load Change

To evaluate dynamic response of the deadbeat controller, simulation was carried out with a 1/2 rated step load (20 Ω) change. Fig. 2.23 depicts the output voltage and current with a step change in load. Note that the output voltage remains virtually unchanged 1.5 ms after the step load.

From simulation results with a nonlinear load, the cascaded deadbeat control method gives fast dynamic response, and feed-forward compensations provide the capability of suppressing the effect of load variations. But error in model parameter estimation leads to tracking errors in the system. Moreover, analog filters are added in order to remove unwanted high frequency harmonic components. The existence of analog filters cause imperfect compensations for decoupling of voltage and current control loops.

2.4.4 Experimental Results Using Conventional Deadbeat Control for Inverter

To evaluate the performance for a real-time control platform for voltage distortions minimization and to verify the simulation results, experimental tests were performed on a DSP-based PWM inverter system. The experimental setup and implementation details have been described in the pervious section. Same control and plant parameters are used in experiment as in the simulation.

2.4.4.1 Linear Load

When the voltage reference peak value is $70\,V$, experimental results of the steady state output voltage using open-loop control and the conventional deadbeat controller under a linear load are shown in Fig. 2.24 and Fig. 2.25 respectively. Similar to the simulation result, deadbeat control minimizes error of the output voltage. The tracking error of output voltage using open-loop control and the conventional deadbeat controller under a linear load is reduced from $18\,V$ (Max) to $13\,V$ (Max), as shown in Fig. 2.26. Frequency spectrum of error as shown in Fig. 2.27 indicates that deadbeat controller minimizes the dominant fundamental frequency component, while the other frequency component magnitudes increase slightly. By reducing the fundamental frequency component of error, deadbeat control scheme introduces the 3^{rd}, 5^{th}, 7^{th}, and 9^{th} harmonic components, therefore THD of deadbeat control increase from 1.2% to 1.5%. Harmonics components with their frequency less than $500\,Hz$ significantly contribute to the voltage error.

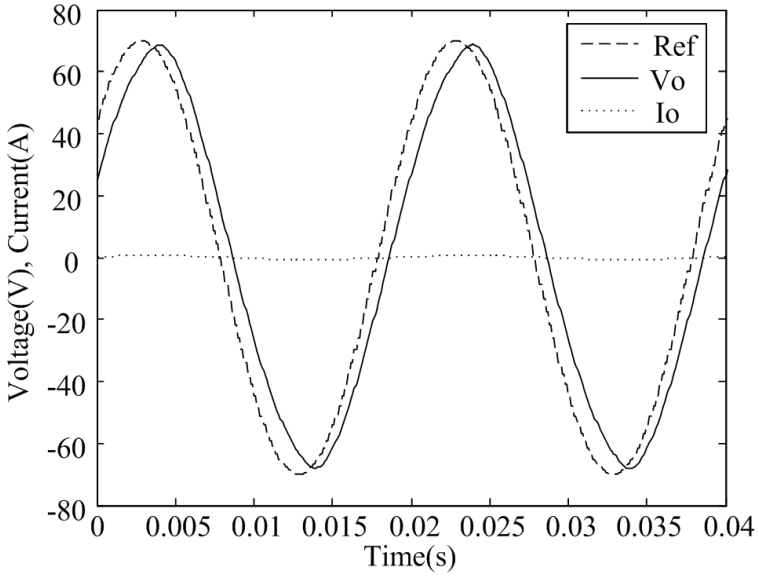


Figure 2.24: Experimental result: steady state output voltage of the inverter system under a linear load using openloop control

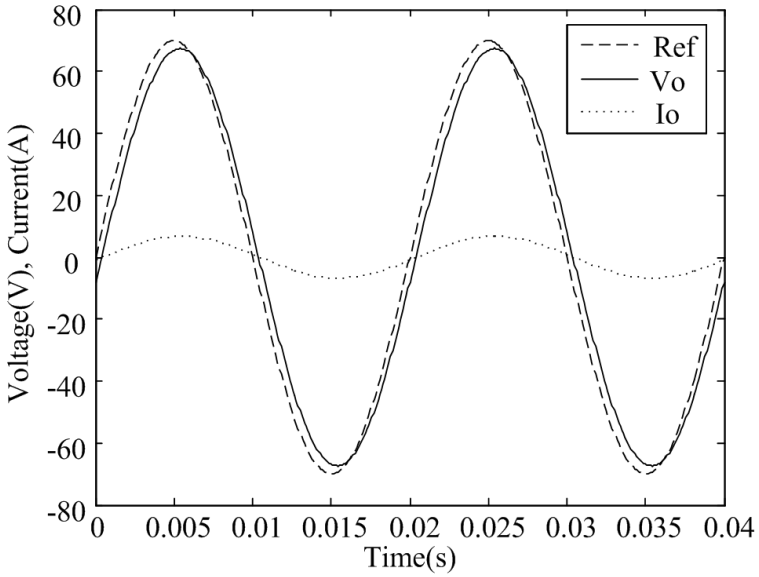


Figure 2.25: Experimental result: steady state output voltage of the inverter system under a linear load using cascaded deadbeat control

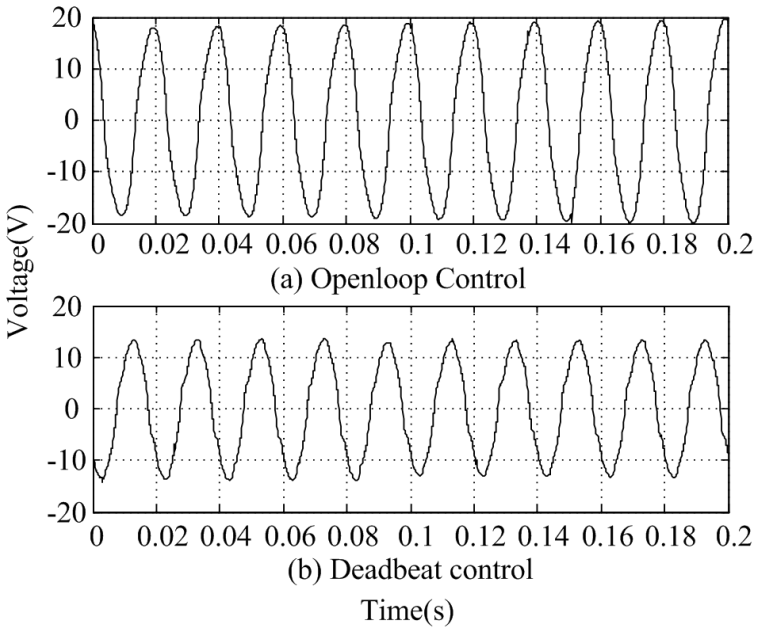


Figure 2.26: Experimental result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using openloop control and (b) cascaded deadbeat Control

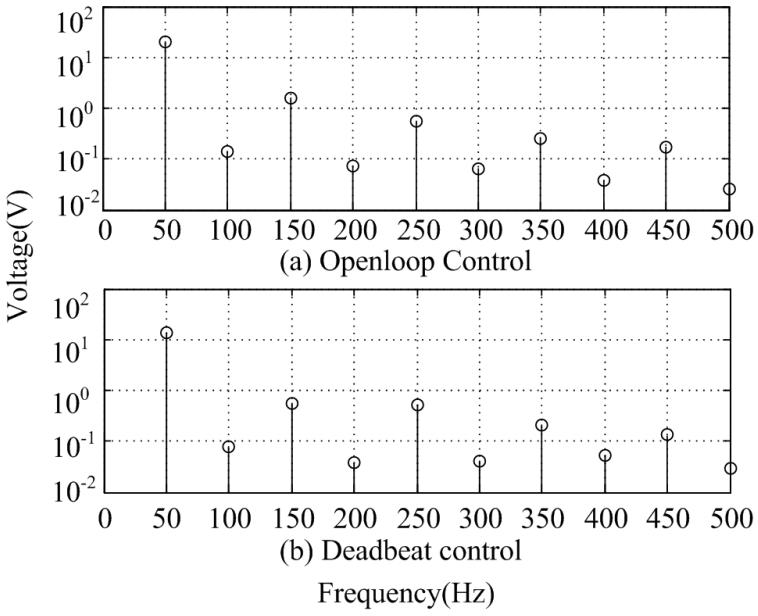


Figure 2.27: Experimental result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using openloop control and (b) cascaded deadbeat control

2.4.4.2 Nonlinear Load

The system performance with a nonlinear load is carried out in the same operating condition as in simulation to evaluate its ability of load disturbance rejection. Experimental results of the steady state output voltage using open-loop control and the conventional deadbeat controller under a nonlinear load are shown in Fig. 2.28 and Fig. 2.29 respectively. Deadbeat control minimizes tracking error of output voltage compared to using open-loop control and the conventional deadbeat controller under a linear load, as shown in Fig. 2.30. The maximum value of error is reduced from $23\,V$ to $14\,V$. The error in the experimental results with a deadbeat controller is higher than that in simulation. This reveals that the inaccuracy of the model deteriorates the performance of the deadbeat control. Frequency spectrum of error as shown in Fig. 2.31 indicates that deadbeat controller minimizes the dominant fundamental frequency component, 1^{st}, 3^{rd}, and 9^{th} order harmonics, and other frequency component magnitudes remain the same or decrease slightly. THD is reduce from $8.3\,\%$ to $4.9\,\%$, which shows that the deadbeat control scheme improves the performance significantly under a load disturbance.

The experimental results show the consistency with the simulation results. The cascaded deadbeat control method offers feed-forward compensations which provides the capability of suppressing the effect of load variations. But it also has the disadvantage such as sensitive to model parameter estimation and imperfect compensations for decoupling voltage and current loops. Repetitive controllers are introduced in next chapter to make up for this deficiency and to reduce harmonics

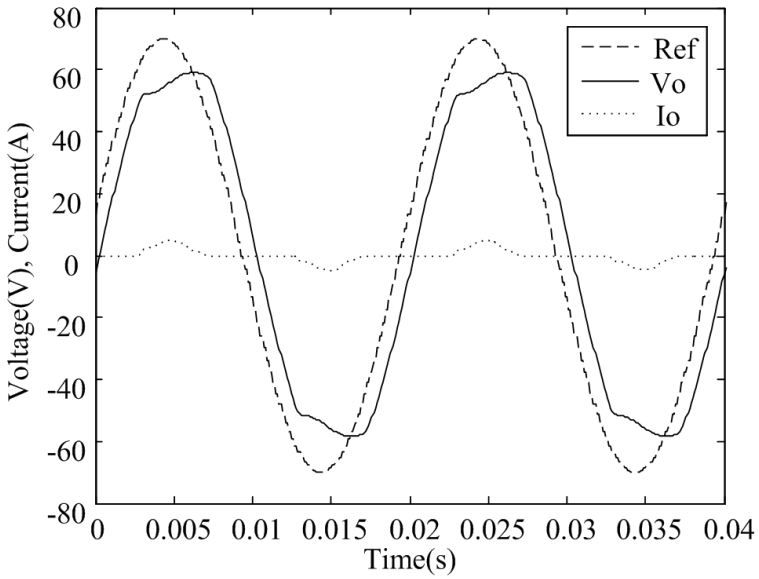


Figure 2.28: Experimental result: steady state output voltage of the inverter system under a nonlinear load using openloop control

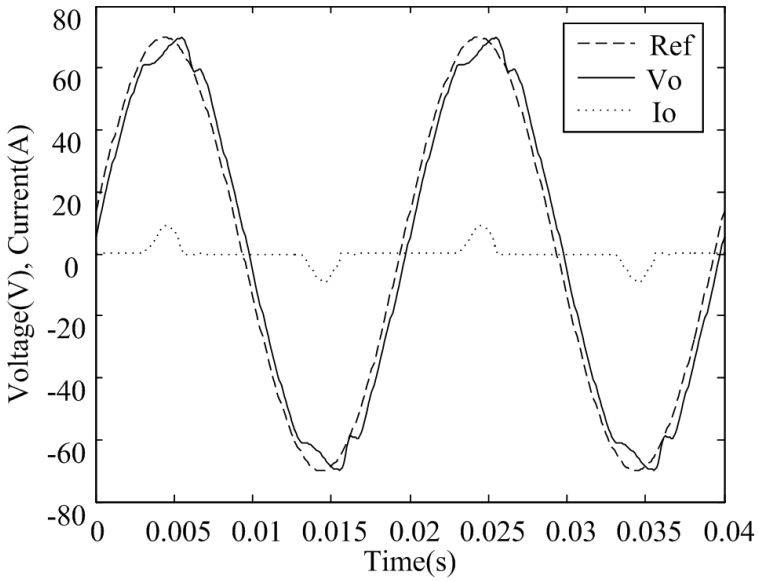


Figure 2.29: Experimental result: steady state output voltage of the inverter system under a nonlinear load using cascaded deadbeat control

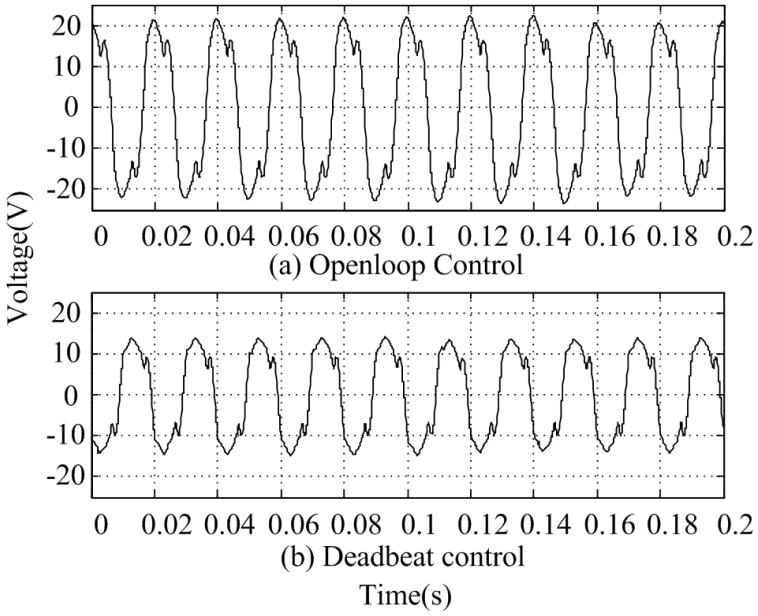


Figure 2.30: Experimental result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using openloop control and (b) cascaded deadbeat control

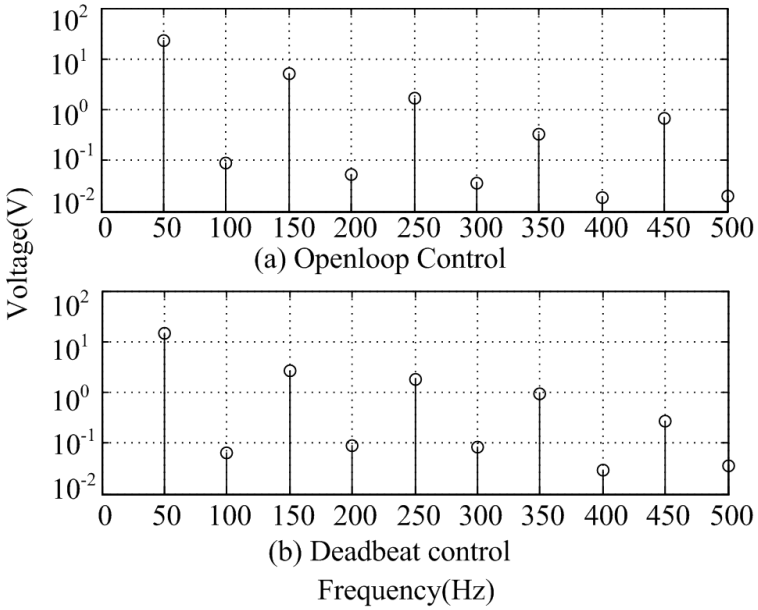


Figure 2.31: Experimental result: error spectrum of output voltage of the inverter system in steady state under a nonlinear load (a) using openloop control and (b) cascaded deadbeat Control

in the output voltage further.

2.5 Conclusion

This chapter presented a cascaded loop deadbeat control scheme for the single-phase UPS inverter. To achieve deadbeat response and decouple the second order system, two compensation signals v_o and i_o are adopted. Two loop gains are designed in the following ways:

1) Compensate the disturbances in the designed loop by adding feedback or feed-forward signal in digital controller.

2) Place the single pole of one closed-loop to origin of z-domain by given an appropriate scalar gain.

Experimental results show that the cascaded deadbeat control scheme reduce THD output voltage by a factor of 1.7 compared with open-loop control under a nonlinear load. Moreover, the maximum tracking errors are reduced by a factor of 1.4 and 1.6, with a linear and a nonlinear load in experimental study respectively.

Chapter 3

Time Domain Based Repetitive Control

3.1 Introduction

In this chapter, the time domain based repetitive control (TDRC) for single-phase inverter is presented. To minimize voltage output distortions further, a time domain based repetitive controller is plugged into the cascaded deadbeat control system described in the previous chapter. Repetitive control is a good solution for minimizing periodic errors, and it is effective for reducing low frequency harmonics. This is due to the limited bandwidth of the controller to eliminate high frequency components. Owing to the fact that low frequency harmonics significantly contribute to the error, repetitive control is a suitable candidate for the DC-AC inverter system. Compared to the deadbeat control method, repetitive control does not require the precise parametric model of the system. Therefore, this control method has significant practical advantages over the other model based schemes,

since the system modelling and identification are difficult to obtain precisely.

In the next section, the basic concept of repetitive control is presented. Its applications to DC-AC inverter is presented in the third section, including both the algorithm and simulation results. Discussions of the results and conclusions are made in the last section.

3.2 Concept of Repetitive Control

Repetitive control (RC) is a control scheme applied to plants that must track a periodic trajectory or reject a periodic disturbance with the explicit use of the periodic nature of the trajectory or disturbance. Repetitive control has been applied to many problems, including [40]:

- robotic manipulators ([41][42][43])
- disk drive servo control ([44][45][46])
- machining ([47][48][49])
- multiple axis systems, e.g. X-Y tables ([48][50])
- vibration control ([51][52][53])
- active noise control ([54][55][56])
- video disk servo control ([57])

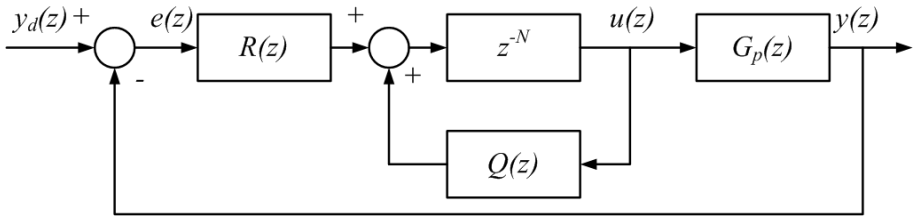


Figure 3.1: Block diagram of repetitive controller in a discrete time system

- power conversion ([58][59][60])
- motor control ([61][62])
- cold rolling process control ([63])
- peristaltic pump control ([64])

Repetitive control method has been developed based on the Internal Model Principle (IMP) [34]. IMP states that in order to track a given signal with asymptotically zero error for a feedback controller, a model that generates the tracking reference should be included in the stable closed-loop system. A repetitive control uses the tracking error and control input in the previous cycle to derive the control input for the present cycle.

A conventional repetitive controller in the discrete time domain is shown in Fig. 3.1. In this figure, N is the number of sampling time intervals. The mission of the controller is to make the output $y(z)$ track the desired periodic trajectory $y_d(z)$. The filter blocks $R(z)$ and $Q(z)$ are designed to improve robustness to high frequency unstructured uncertainty and ensure the convergence of the tracking error to zero asymptotically.

When designing the repetitive controller, there are some issues to be considered.

1) To get a good tracking performance using a repetitive controller, some easily obtainable information about the existing feedback control system should be used. First a frequency response test is performed to get the Bode plot of the system. The Bode plot is based on the output voltage data without the plug-in repetitive controller to examine the dominant harmonics of the system output voltage in simulation or experimental results. The desired controller is designed to work based on this description of the system. This avoids system modelling and identification as well as the inaccuracies caused by them. By analyzing the frequency response, filters $R(z)$ and $Q(z)$ are designed to remove the unwanted high frequency components in the learning process.

2) To guarantee good learning dynamic performance, the gain of $R(z)$ is adjusted to change the error decay rate. One should notice that for different frequency components, the error decay rate is different. Unfortunately, TDRC can assign only one gain for all frequency components. A larger learning gain could accelerate the convergence speed, but it may make the control system unstable. Therefore the choice of the gain is a balance between speed of convergence and stability. A universal gain is given in TDRC to meet the convergency condition for high frequency components, which is relatively small for the low frequency components. It actually slows down the convergency process. However, frequency domain repetitive control which is introduced in the next chapter provides the freedom of

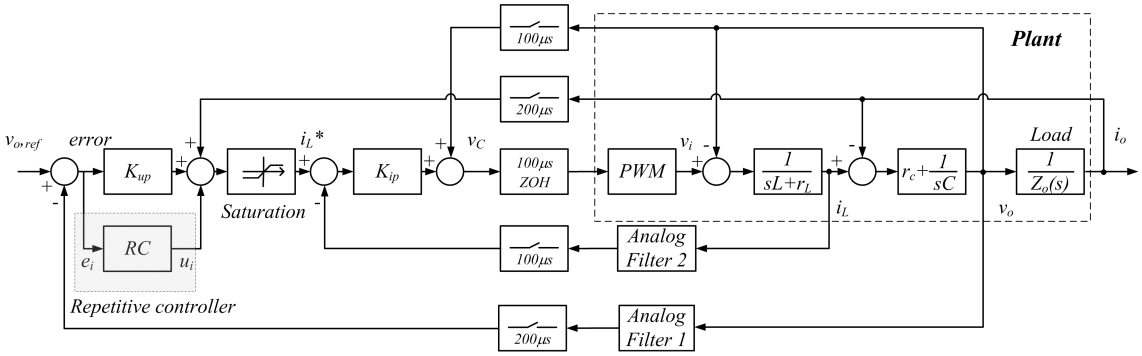


Figure 3.2: Block diagram of the plug-in repetitive control system

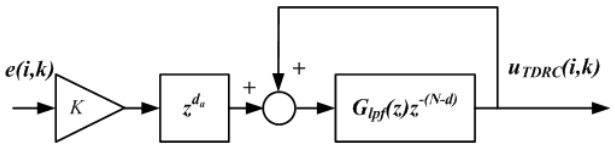


Figure 3.3: Time domain repetitive control scheme

assigning different gains for different frequency components and thereby overcomes the problem of TDRC.

3.3 Plug-in Time Domain based Repetitive Control for Inverter

To further reduce the tracking error of the output voltage, a plug-in repetitive controller is incorporated into the outer voltage loop of the cascaded deadbeat control system, as shown in Fig. 3.2. Block RC (Repetitive Control) represents either time domain based or frequency domain based repetitive controllers. TDRC control block diagram is shown in Fig. 3.3. The learning gain K is chosen based on the convergence speed and stability of the system. Low pass filter is added to cut

off the learning process for high frequency signals, and to make learning controllers easily converge. TDRC control scheme output signal is given as

$$\frac{u_{TDRC}(i,k)}{e(i,k)} = \frac{K \cdot G_{lpf}(z) z^{-(N-d)+d_a}}{1 - G_{lpf}(z) z^{-(N-d)}} \tag{3.1}$$

where i - cycle number; k - position interval number; K is TDRC learning gain; $u_{TDRC}(i,k)$ is the control input of TDRC at k^{th} position in the present i^{th} cycles; $e(i,k)$ is the tracking error at k^{th} position of the present i^{th} cycle; $G_{lpf}(z)$ is a low pass filter to limit the frequency bandwidth in TDRC; d is the number of samples corresponding to the phase delay at fundamental frequency caused by the low pass filter; d_a is the number of samples corresponding to the phase delay at fundamental frequency of the analog filter 1 in Fig. 3.2, and it is used to compensate the phase delay caused by analog filter 1.

3.3.1 Investigation of Learning Gain Effect on Time Domain Repetitive Controller

3.3.1.1 Stability Analysis Based on Simplified Model of the Control System

To simplify the model and find out an optimal learning gain for TDRC, we consider the inner current loop as a constant gain as mentioned in Section 2.4.1. Based on this simplification, the block diagram of the inverter control system can be drawn as shown in Fig. 3.4. In the inverter system block diagram, $G_p(z)$ represents transfer function of inner current loop and inverter system; $G_{af1}(z)$ represents discrete time

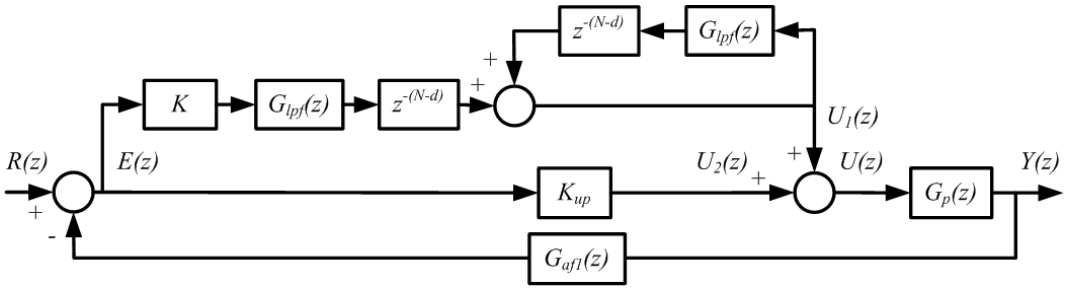


Figure 3.4: Simplified control block diagram of the TDRC control system

domain transfer function of the analog filter 1 in Fig 3.2, which is converted from the continuous time domain transfer function. The plug-in time domain repetitive controller is same as in Fig. 3.3 except omitting the phase delay correction block z^{d_a} to avoid the complexity of the analysis. According to the block diagram in Fig. 3.4, we can derive the open-loop transfer function as below:

$$E(z) = R(z) - G_{af1}(z)Y(z) \tag{3.2}$$

$$U_1(z) = KE(z)G_{lpf}(z)z^{-(N-d)} + G_{lpf}(z)U_1(z)z^{-(N-d)} \tag{3.3}$$

$$U(z) = \left(\frac{KG_{lpf}(z)z^{-(N-d)}}{1 - G_{lpf}(z)z^{-(N-d)}} + K_{up}\right) E(z) \tag{3.4}$$

$$Y(z) = G_p(z)U(z) \tag{3.5}$$

Therefore, open-loop transfer function is given as

$$\frac{G_{af1}(z)\,Y(z)}{E(z)} = G_{af1}(z)\,G_p(z)\left(\frac{KG_{lpf}(z)z^{-(N-d)}}{1 - G_{lpf}(z)z^{-(N-d)}} + K_{up}\right) \tag{3.6}$$

where in simulation and experiment

$$G_{lpf}(z) = \frac{0.13}{z - 0.87} \tag{3.7}$$

$$G_p(z) = \frac{0.703z + 0.513}{z - 1} \tag{3.8}$$

$$G_{af1}(z) = \frac{1}{12} \cdot \frac{0.1132z + 0.0633}{z^2 - 0.9956z + 0.172} \tag{3.9}$$

Notice that G_{lpf} is the low pass filter to remove the unwanted high frequency components in time domain repetitive controller, thereby the cut-off frequency of the low pass filter is set more than the highest frequency component of the selected learning frequency components. Without losing generality, we take G_{lpf} cut-off frequency to be 200 Hz in the following analysis, which means frequency components chosen in the learning process are less than 200 Hz. In simulation and experiment, cut-off frequencies 100Hz, 200Hz, and 300Hz are chosen and implemented in the control system. Same analysis could be used on system with any cut-off frequency filters. $G_p(z)$ is derived from Eqn. 2.15; transfer function Eqn. 3.9 of analog filter 1 G_{af1} is derived in Appendix C, and its continuous time domain form is

$$G_{af1}(s) = \frac{1}{12} \cdot \frac{1}{1.034 \times 10^{-7} s^2 + 9.1 \times 10^{-4} s + 1} \tag{3.10}$$

. This analog filter has a gain less than 1 is because the output voltage is amplified from the desired reference voltage.

Gain margins and phase margins of the openloop transfer function Eqn. 3.6 are evaluated for the stability of the inverter system as shown in Table 3.1.

Table 3.1: Phase Margins and Gain Margins of the Simplified Model

K	0.01	0.05	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1	2	5
$G_m\,(dB)$	21	22	18	16	12	9	6	3	1	0.8	0.8	1.3
$P_m\,(degree)$	77	50	41	30	22	15	9	4	-1	-7	-11	-32

From Table 3.1 we can conclude that with a learning gain K higher than 0.3, the gain margins and phase margins are not sufficient; on the other hand, too low

control gains will cause slow response. Therefore we choose the gain K to be 0.2 as our optimal gain and validate it through simulation studies.

3.3.1.2 Evaluation of Learning Gain Effect

To further investigate the learning gain effect on the system, simulation studies are carried out. The corresponding simulation results are shown in Fig. 3.5. The same inverter system operating conditions and cascaded deadbeat controller parameters are used in this Chapter and Chapter 2. Giving a small learning gain $K = 0.05$ in simulation, the tracking error of output voltage converges to its steady state in a long time period of $0.5\,s$ (TDRC starts working from $t = 0.04\,s$, and the following tests are carried out by using the same time setting). The steady state error can not be reduced lower than $1.2\,V$. Increasing the learning gain to 0.2 in simulation, the tracking error takes $0.2\,s$–less than half time in the first test to reach its steady-state $0.4\,V$. Further increasing the gain to 0.4, error converges to its minimum steady-state value $(0.2\,V)$ within a short time $0.08\,s$ (4 cycles). Giving a large gain $K = 0.7$, the output voltage oscillates for 3 cycles and then reaches its minimum value. When $K = 1.0$, the error oscillates and finally causes the control system unstable. $K = 2.0$, the tracking error oscillates to a higher voltage level comparing to $K = 1.5$. Therefore, using a gain $K > 0.7$ will cause the oscillation and unstable of the system. The optimum gain $K = 0.4$ is chosen to achieve fast convergence speed, low steady state error and stability.

In conclusion, simulation results show consistency with the theoretical stabil-

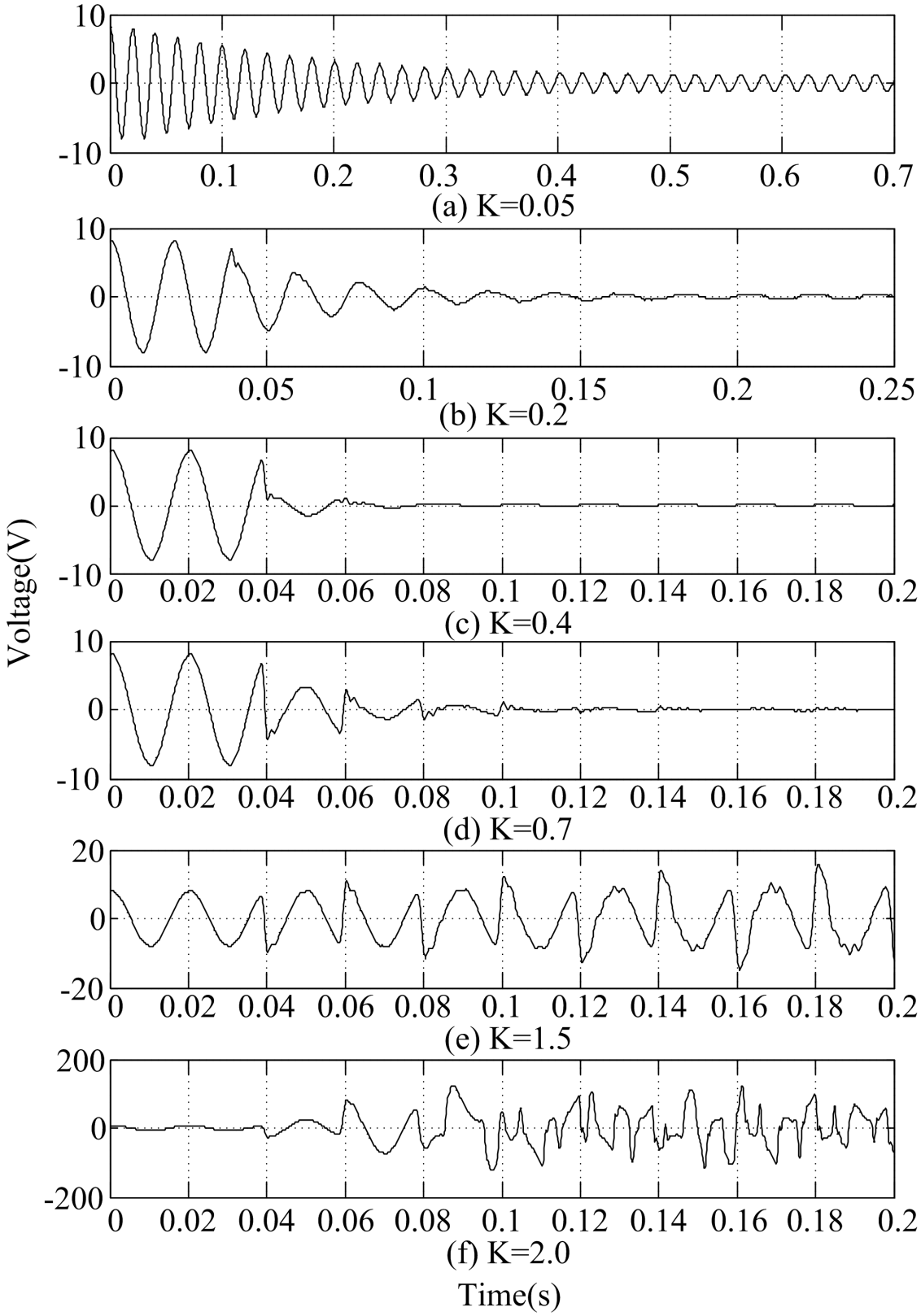


Figure 3.5: Tracking error of output voltage of the inverter system under a linear load with different learning gains in TDRC a) K=0.05 b) K=0.2 c) K=0.4 d) K=0.7 e) K=1.5 f) K=2.0

ity analysis in the choice of the learning gain. The little difference of the learning gain values between analysis and simulation may be due to the assumption and simplification in the analyzing model or inaccuracy of the system parameters such as the nominal value of the LC filter.

3.3.2 Simulation Results Using Time Domain Repetitive Control for Inverter

3.3.2.1 Linear Load

To investigate the performance of the proposed repetitive control scheme, simulations were carried out in the same software environment and plant parameters as described in Chapter 2. Error spectrum in Fig. 2.18 (b)(pp.41) shows that the 1^{st}, 3^{rd}, 5^{th} harmonic components are the most dominant components in output voltage tracking error with a linear load. Consequently, a low pass filter is added to prevent the learning process for high frequency signals above $300\,Hz$, and to make sure the learning controller convergence. Performance using different cutoff frequency of the low pass filters are compared in the following discussions.

The output voltages in steady state are shown in Fig. 3.6. Cutoff frequency of low pass filters in TDRC are set to $300\,Hz$. Comparing to the output voltage using deadbeat controller, we can see that the plug-in time domain repetitive controller removes the phase delay of output voltage. The output voltage tracks the reference almost perfectly under a linear load in simulation. Tracking errors of output volt-

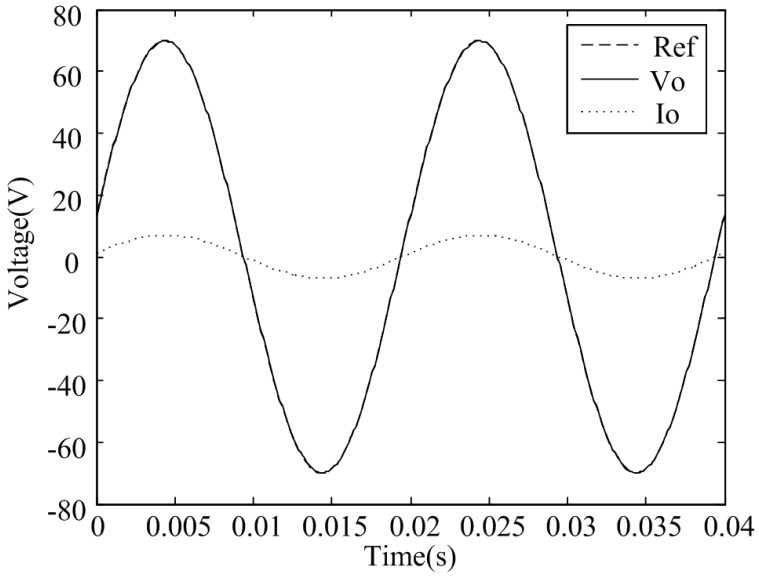


Figure 3.6: Simulation result: steady state output voltage of the inverter system under a linear Load using TDRC control scheme, with low pass filters cutoff frequency 300 Hz

age in steady state using the cascaded deadbeat controller and the proposed TDRC control scheme with different filters are shown in Fig. 3.7. Tracking error is significantly reduced from 8.9 V to 0.52 V, 0.31 V and 0.29 V, using TDRC controller with cutoff frequency of low pass filters 100 Hz, 200 Hz, and 300 Hz respectively. From the frequency spectrum as shown in Fig. 3.8, the frequency components whose frequency are lower than the cutoff frequency of low pass filters are reduced respectively. THD are reduced from 0.4% (deadbeat control) to 0.3% (TDRC 100 Hz), 0.2% (TDRC 200 Hz), 0.1% (TDRC 300 Hz). These data show that the proposed time domain based repetitive control scheme is able to track the output voltage accurately and thereby reduce the output voltage distortions. Especially with a cutoff frequency 300Hz for the low pass filters, TDRC reduces the distortions by a factor of 4. Error converging dynamics using TDRC control scheme is shown

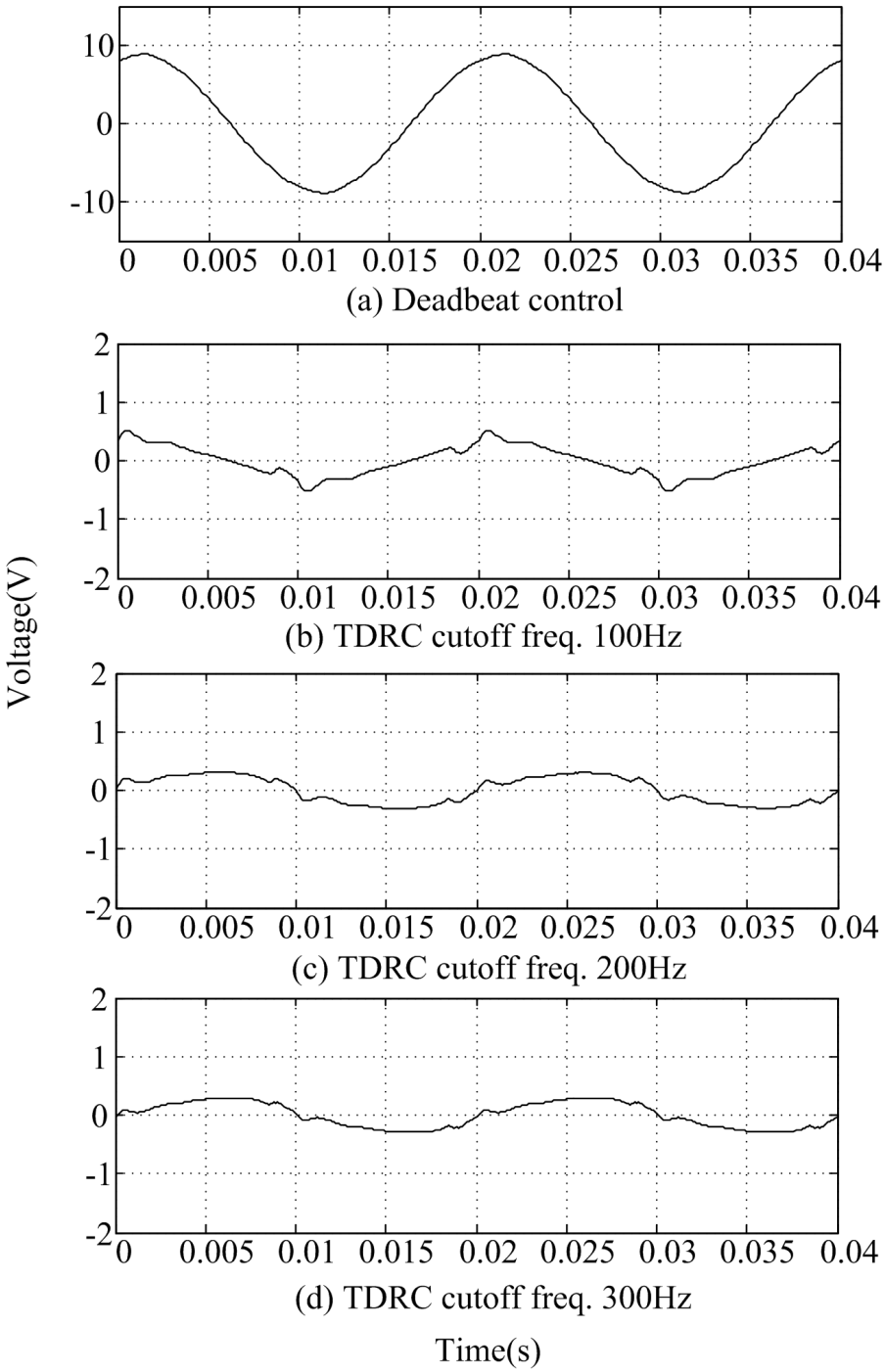


Figure 3.7: Simulation result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

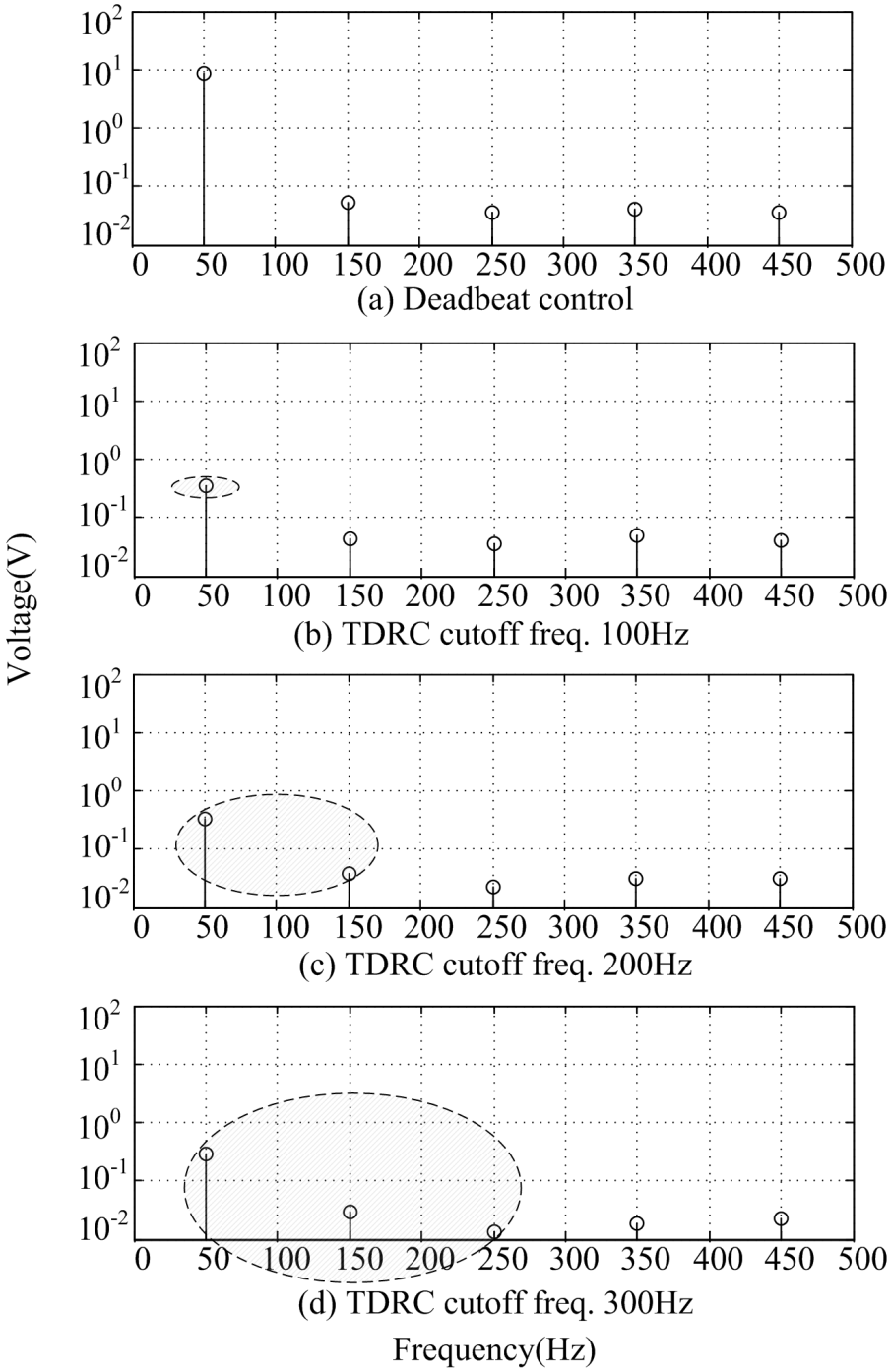


Figure 3.8: Simulation result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

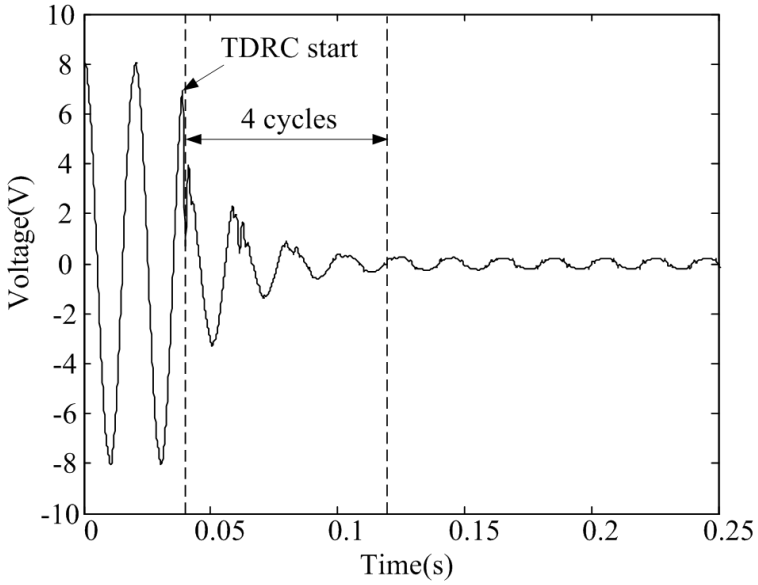


Figure 3.9: Simulation result: error of the output voltage of the inverter system in transient under a linear load using TDRC control scheme, with low pass filters cutoff frequency $300\,Hz$

in Fig. 3.9. During time period $0\,s$ to $0.04\,s$, only deadbeat controller is used to control the inverter system. As soon as the TDRC is activated the output voltage error further reduces to the steady state value in 4 cycles.

3.3.2.2 Nonlinear Load

Using deadbeat control, error spectrum under a nonlinear load in Fig. 2.22 (b)(pp.43) shows that the 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components are the most dominant components in output voltage tracking error with a nonlinear load. The output voltages in steady state are shown in Fig. 3.10- 3.12. Cutoff frequency of low pass filters in TDRC are set from $100\,Hz$ to $300\,Hz$ respectively. Comparing with the output voltage using deadbeat controller, we can see that the plug-in time domain

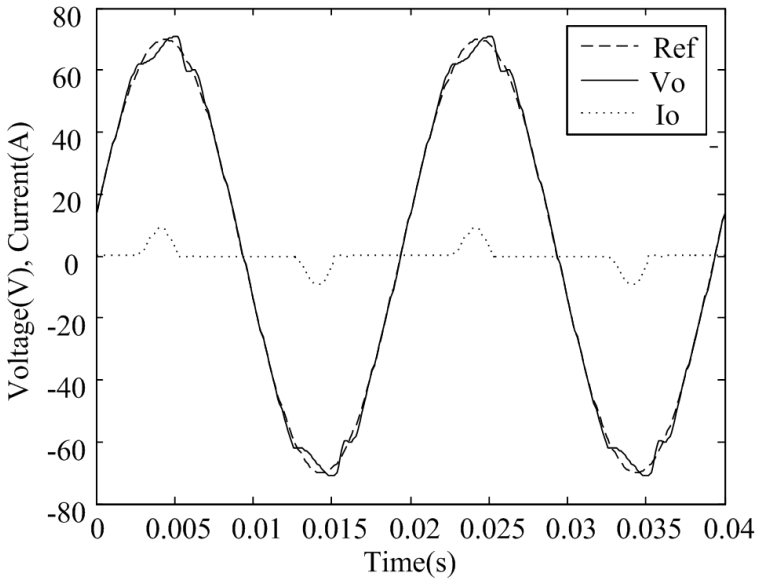


Figure 3.10: Simulation result: steady state output voltage of the inverter system under a noninear load using TDRC control scheme, with low pass filters cutoff frequency $100\,Hz$

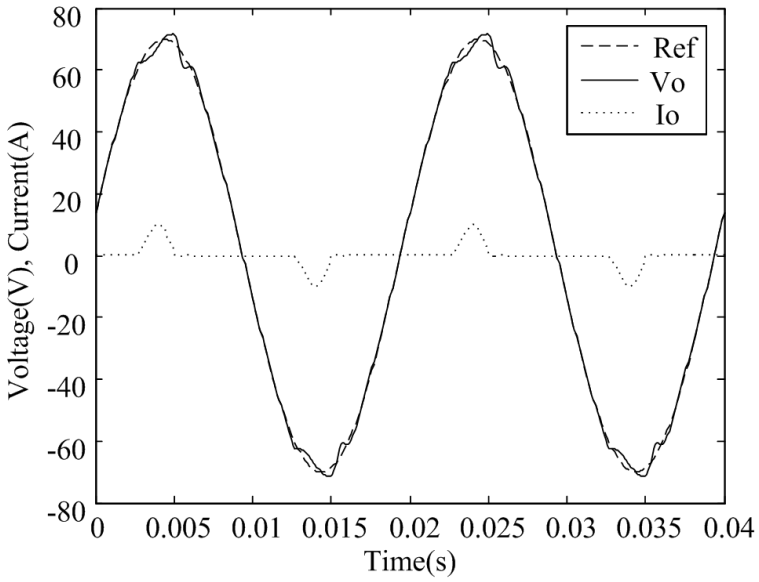


Figure 3.11: Simulation result: steady state output voltage of the inverter system under a nonlinear load using TDRC control scheme, with low pass filters cutoff frequency $200\,Hz$

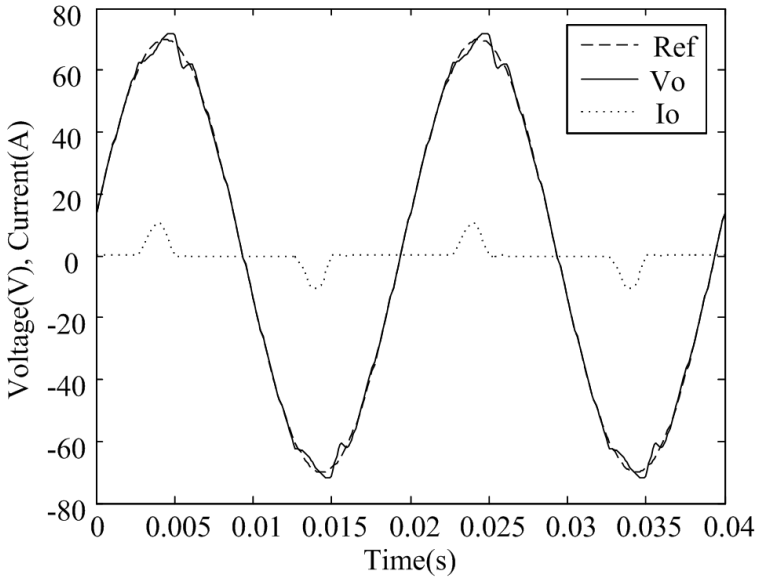


Figure 3.12: Simulation result: steady state output voltage of the inverter system under a nonlinear load using TDRC control scheme, with low pass filters cutoff frequency 300 Hz

repetitive controller removes the phase delay of the output voltage. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed TDRC control scheme with different cut-off frequencies of filters are shown in Fig. 3.13. Compared with the deadbeat control method,tracking error is significantly reduced from 7.8 V to 4.0 V, 3.7 V and 3.7 V, using TDRC controller with cutoff frequency of low pass filters 100 Hz, 200 Hz, and 300 Hz respectively. From the frequency spectrum as shown in Fig. 3.14, the frequency components whose frequency are lower than the cutoff frequency of low pass filters are reduced respectively. Compared to the deadbeat control scheme, THD are reduced from 3.8 % to 2.7 %. With cutoff frequency 300 Hz of low pass filters, TDRC gives the best performance and reduces the distortions by a factor of 1.4. However, it can be clearly seen that for the 5th harmonic frequency component, the reduction by

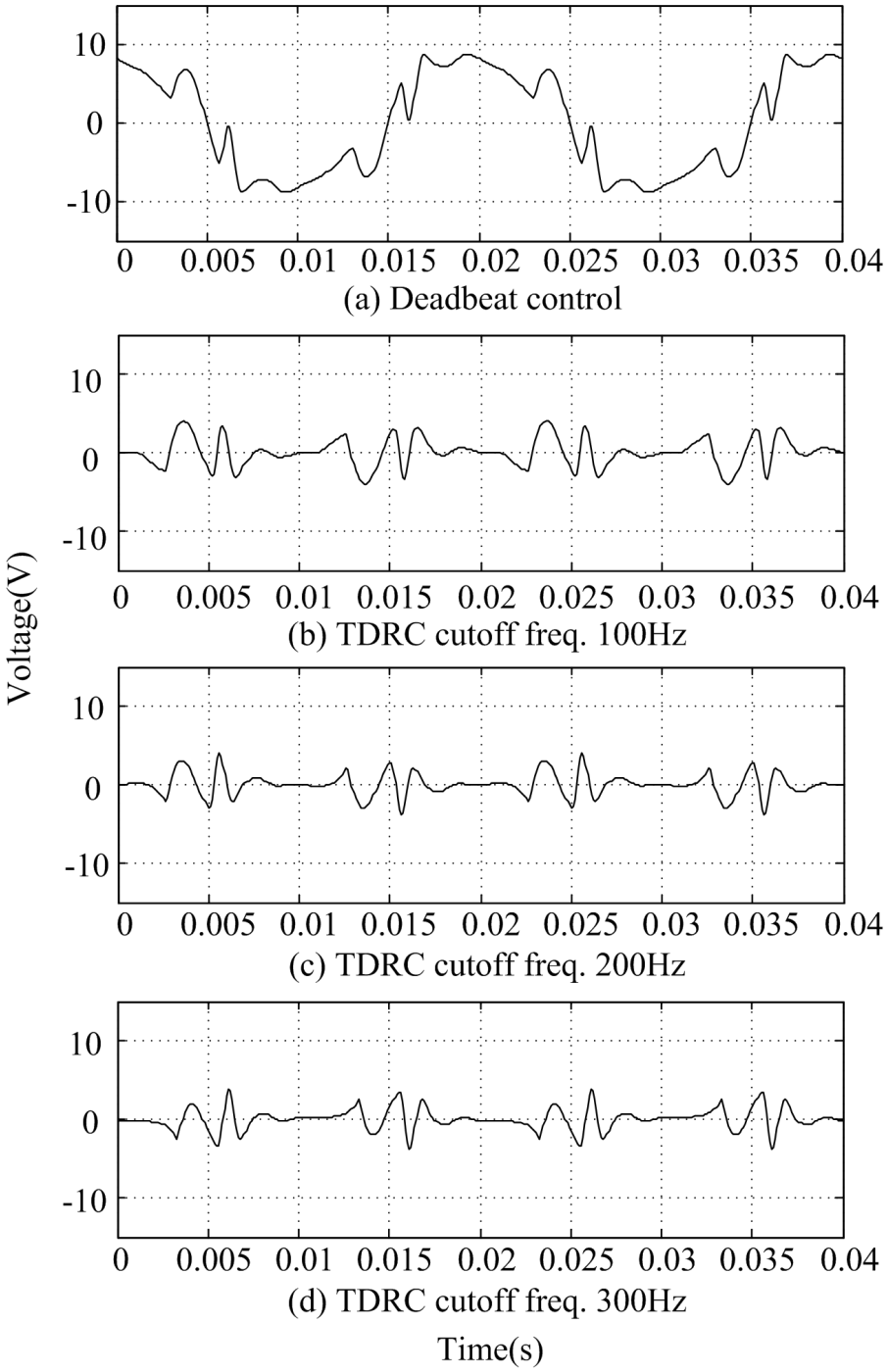


Figure 3.13: Simulation result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d) $300\,Hz$

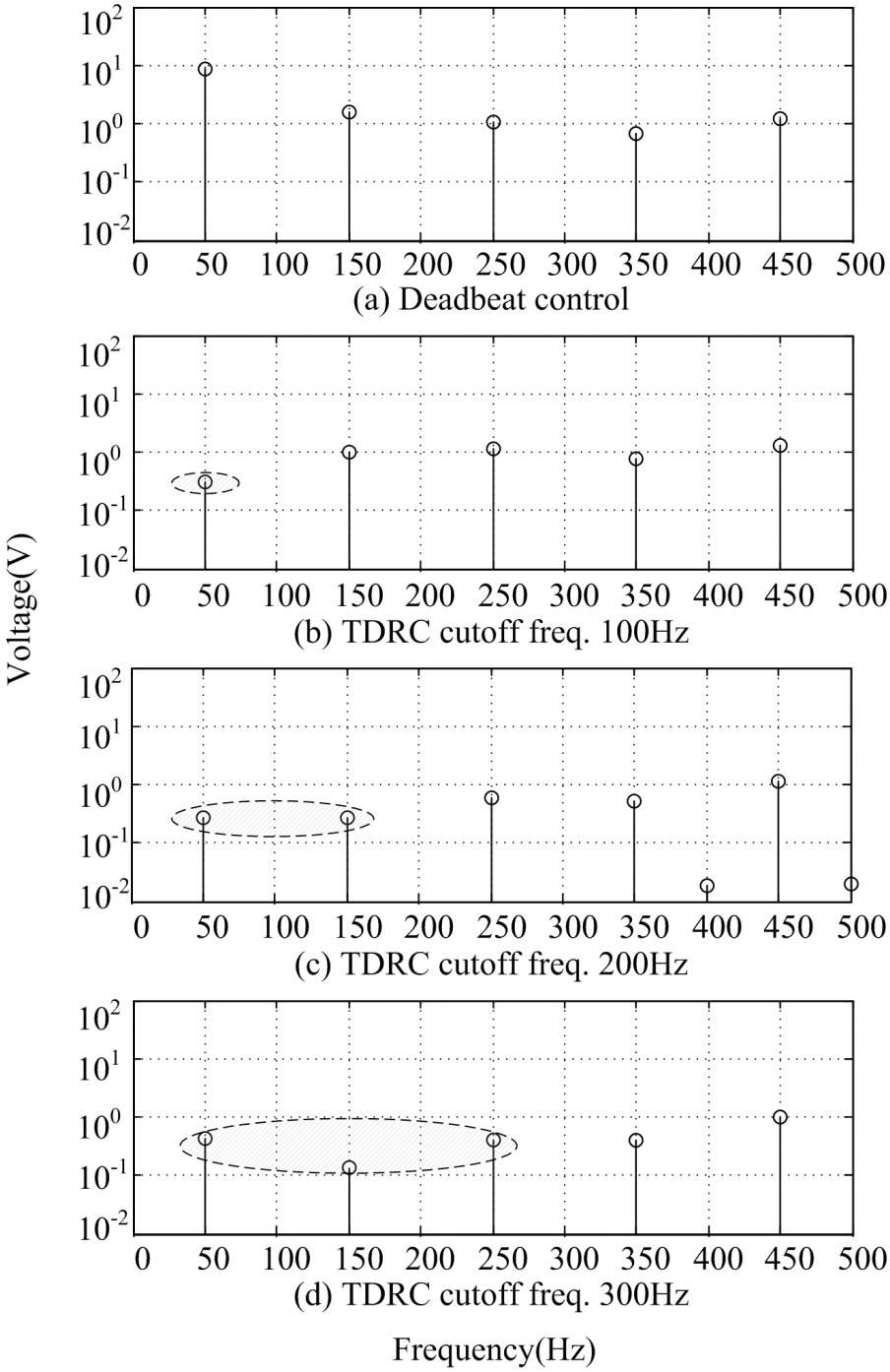


Figure 3.14: Simulation result: error spectrum of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

TDRC is relatively small. Moreover, if the cutoff frequency of the low pass filters are increased further, the higher order harmonic components are not able to converge and cause oscillations of the output voltage. This shows the limitation of time domain repetitive controller. As we know, the phase delay of low pass filters including both digital and analog filters increases as the frequency increases. Phase delay of digital filters could be removed by proper filter design, but phase delay of analog filter is difficult to be cancelled in a conventional way. In time domain repetitive control, we could reduce the repetitive time period to compensate for the phase delay. But the repetitive time period is universal for all the frequency components. On the other hand, high frequency components cannot be compensated as the phase compensation time is determined by the phase delay of fundamental frequency. Hence, inability to cancel the phase delay for high frequency harmonic components causes deterioration of the system performance. Fortunately, this problem can be solved using the proposed frequency domain repetitive controller which is introduced in the next chapter.

3.3.2.3 Load Change

Fig. 3.15 shows the simulation result of transient response when the load change from no load to half load ($20\,\Omega$) takes place. The figure shows that the system exhibits fast dynamic response with little change in the output voltage, which indicates that the proposed controller is capable of maintaining a "stiff" output voltage.

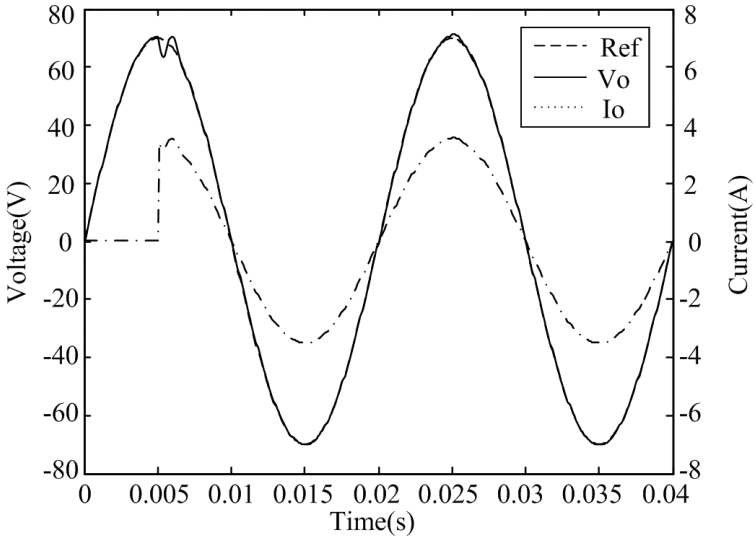


Figure 3.15: Simulation result: Transient response of the inverter system in steady state with a step load using TDRC control scheme

3.3.3 Experimental Results Using Time Domain Repetitive Control for Inverter

3.3.3.1 Linear Load

Experimental results show the coherence with the simulation results. Error spectrum in Fig. 2.27 (b)(pp.48) shows that the 1^{st}, 3^{rd}, 5^{th} harmonic components are the most dominant components in output voltage tracking error with a linear load. Hence, the cutoff frequency of low pass filter is set lower than $300\,Hz$ to choose the learning frequency components below the cutoff frequency.

The output voltages in steady state are shown in Fig. 3.16-Fig. 3.18. Cutoff frequency of low pass filters in TDRC are set from $100\,Hz$ to $300\,Hz$ in steps of $100\,Hz$. TDRC removes the phase delay of output voltage which is similar

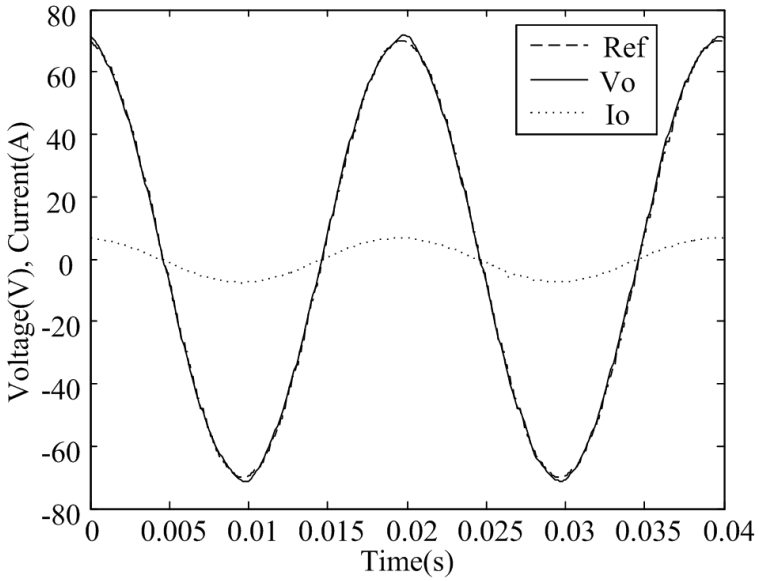


Figure 3.16: Experimental result: steady state output voltage of the inverter system under a linear load using TDRC control scheme, with low pass filters cutoff frequency 100 Hz

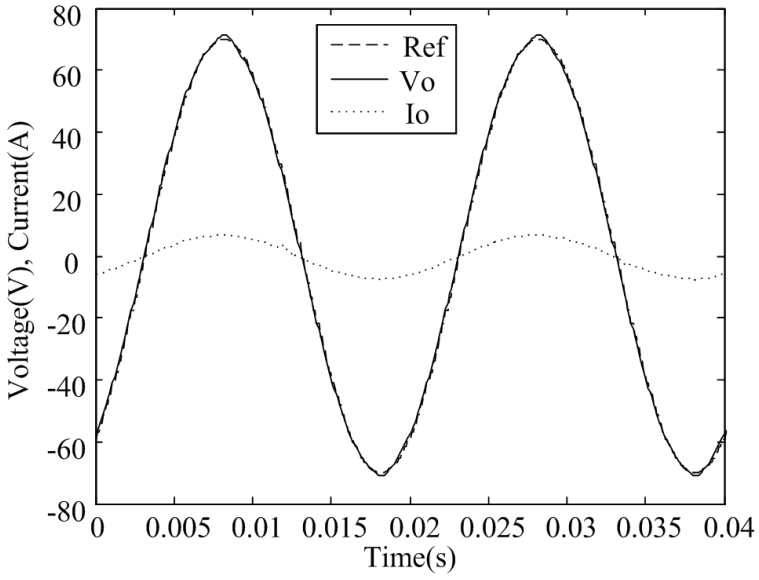


Figure 3.17: Experimental result: steady state output voltage of the inverter system under a nonlinear load using TDRC control scheme, with low pass filters cutoff frequency 200 Hz

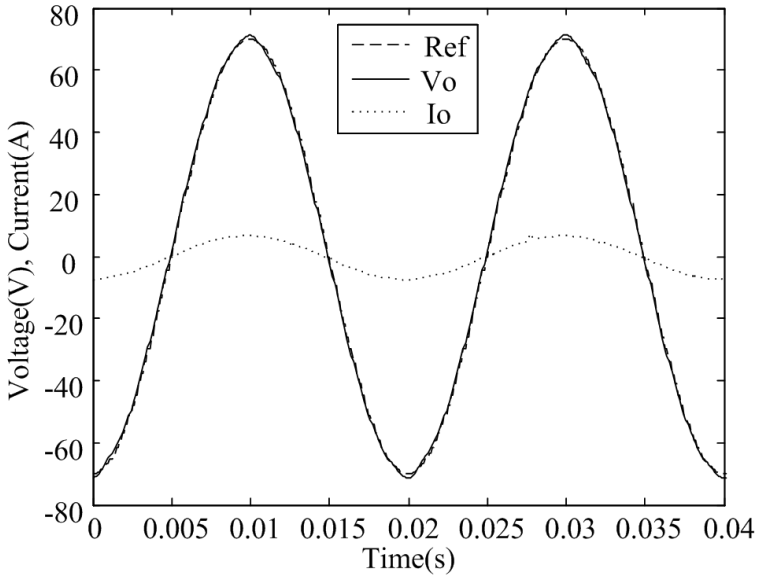


Figure 3.18: Experimental result: steady state output voltage of the inverter system under a linear load using TDRC control scheme, with low pass filters cutoff frequency $300\,Hz$

to results in simulation. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed TDRC control scheme with different filters are shown in Fig. 3.19. Tracking error is reduced from $13\,V$ to $1.8\,V$, $1.6V$ and $1.5V$, using TDRC controller with cutoff frequency of low pass filters $100\,Hz$, $200\,Hz$, and $300\,Hz$ respectively. From the frequency spectrum, the frequency components whose frequency are lower than the cutoff frequency of low pass filters are reduced respectively. THD are reduced from $1.5\,\%$ (deadbeat control) to $1.2\,\%$ (TDRC $100\,Hz$), $1.0\,\%$ (TDRC $200\,Hz$), 0.6% (TDRC $300\,Hz$). Experimental THDs are higher than that obtained through simulation ones due to the measurement noise, effect of deadtime in IGBT switching, and some other unexpected disturbances. But from the results, TDRC is still able to contribute to the distortions reduction by a factor of 2. Convergence of error is shown in

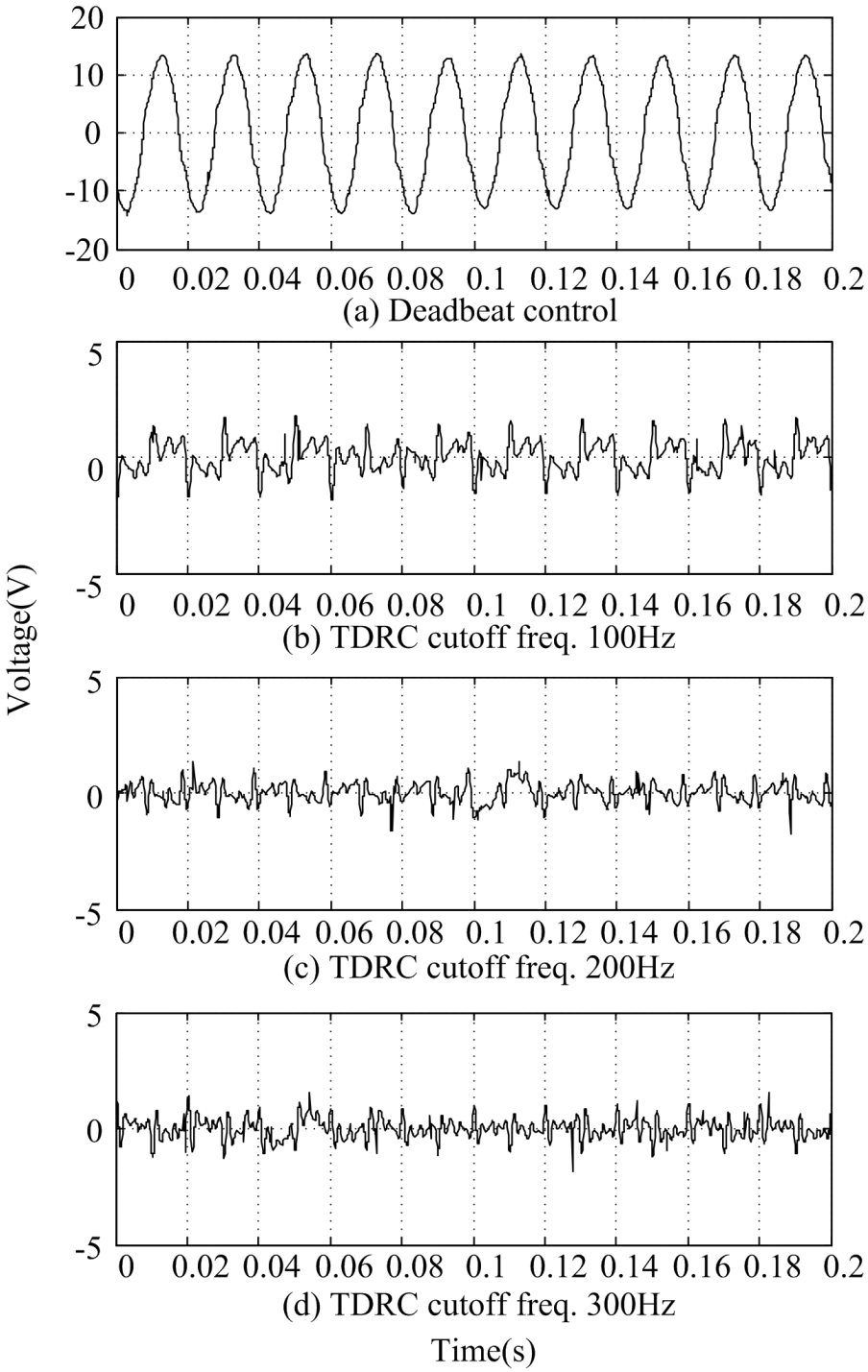


Figure 3.19: Experimental result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

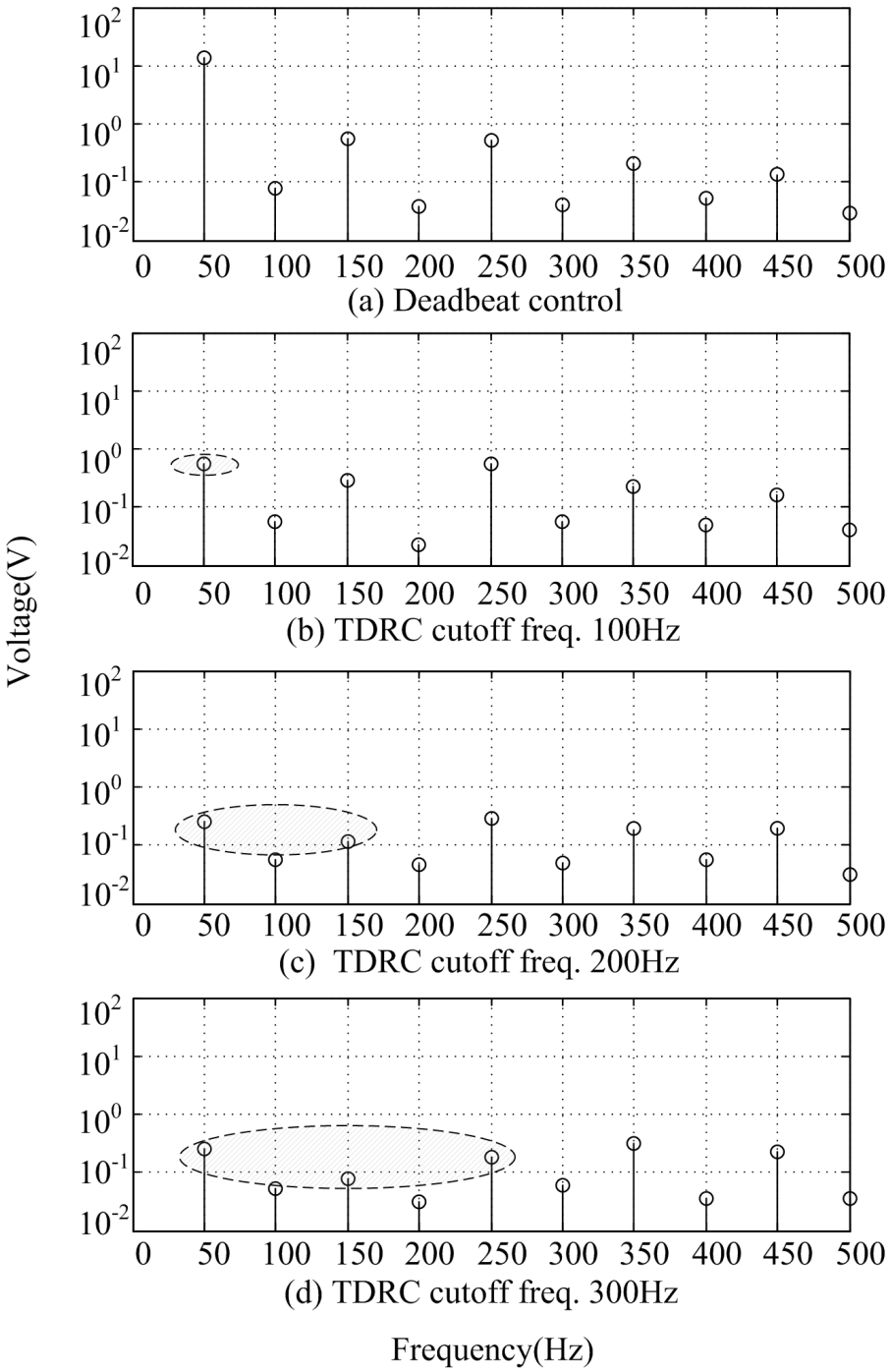


Figure 3.20: Experimental result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

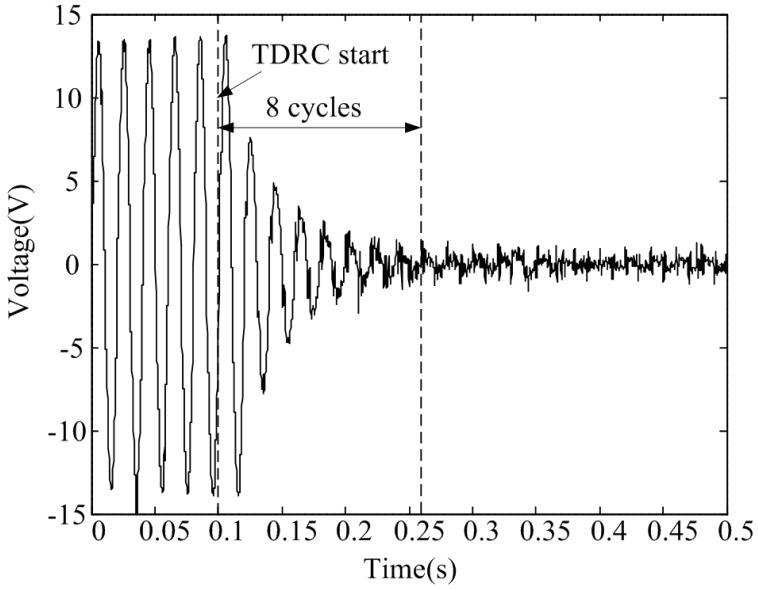


Figure 3.21: Experimental result: error of the output voltage of the inverter system in transient under a linear load using TDRC control scheme, with low pass filters cutoff frequency 300 Hz

Fig. 3.21. Due to the limitation of TDRC, a universal gain has to be given for each frequency component. Therefore, when the cutoff frequency of low pass filters is high, a small gain is required to prevent the unstable response of the system. Moreover, in real-time implementation, noise and disturbance limit the learning as well. The best performance can be achieved in 8 cycles, which is twice longer than the response that is obtained in simulation.

3.3.3.2 Nonlinear Load

Similar to simulation studies, using deadbeat control, error spectrum under a non-linear load in Fig. 2.31 (b)(pp.50) shows that the 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components are the most dominant components in output voltage tracking error

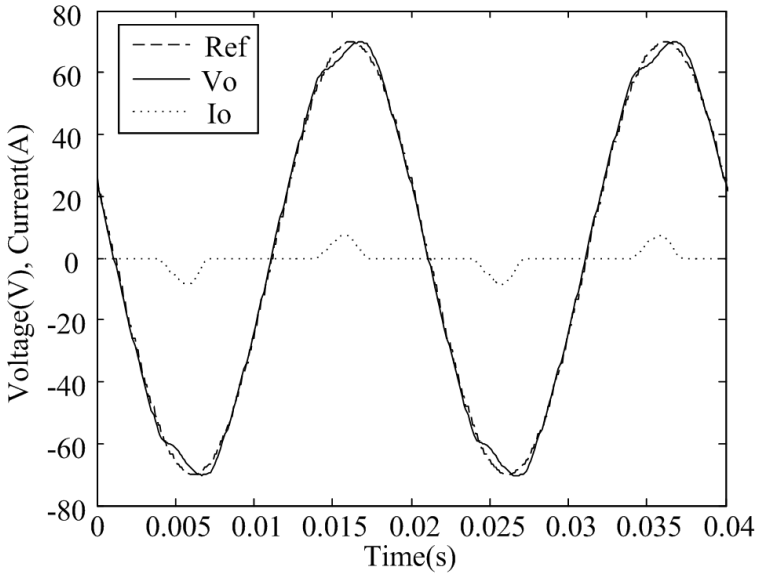


Figure 3.22: Experimental result: steady state output voltage of the inverter system under a noninear load using TDRC control scheme, with low pass filters cutoff frequency 100 Hz

with a nonlinear load. The output voltages in steady state are shown in Fig. 3.22 - Fig. 3.24. Cutoff frequency of low pass filters in TDRC are set from 100 Hz to 300 Hz. Similarly, the plug-in TDRC removes the phase delay of output voltage. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed TDRC control scheme with different filters are shown in Fig. 3.25. Tracking error is significantly reduced from 14 V to 5.0 V, 3.5 V and 5.0 V, using TDRC controller with cutoff frequency of low pass filters 100 Hz, 200 Hz, and 300 Hz. From the frequency spectrum as shown in Fig 3.26, the frequency components whose frequency are lower than the cutoff frequency of low pass filters are reduced respectively. THD are reduced from 4.9 % (deadbeat control) to 3.8 % (TDRC 100 Hz), 3.0 % (TDRC 200 Hz), 4.0 % (TDRC 300 Hz). With cutoff frequency 200 Hz of low pass filters, TDRC gives the best performance and reduce

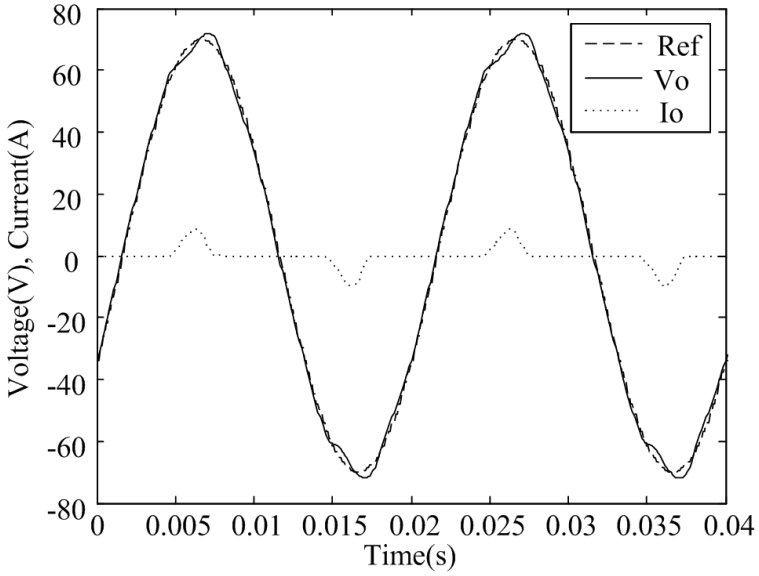


Figure 3.23: Experimental result: steady state output voltage of the inverter system under a nonlinear load using TDRC control scheme, with low pass filters cutoff frequency 200 Hz

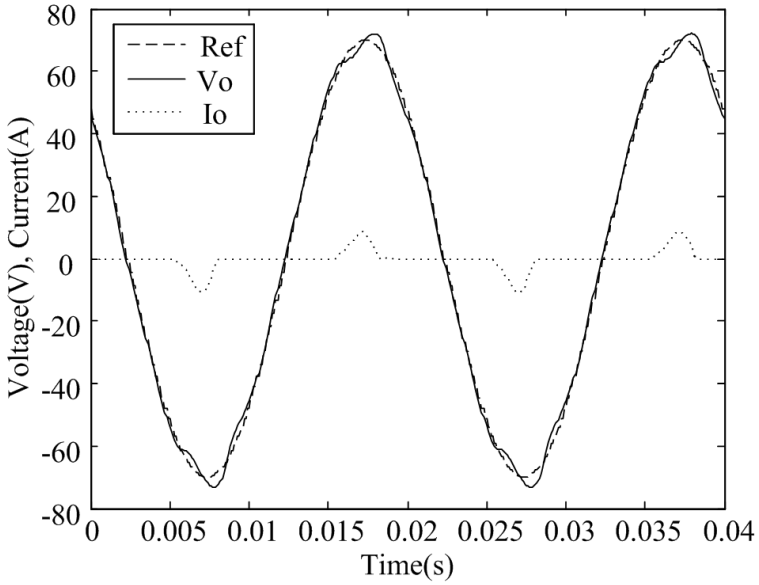


Figure 3.24: Experimental result: steady state output voltage of the inverter system under a nonlinear load using TDRC control scheme, with low pass filters cutoff frequency 300 Hz

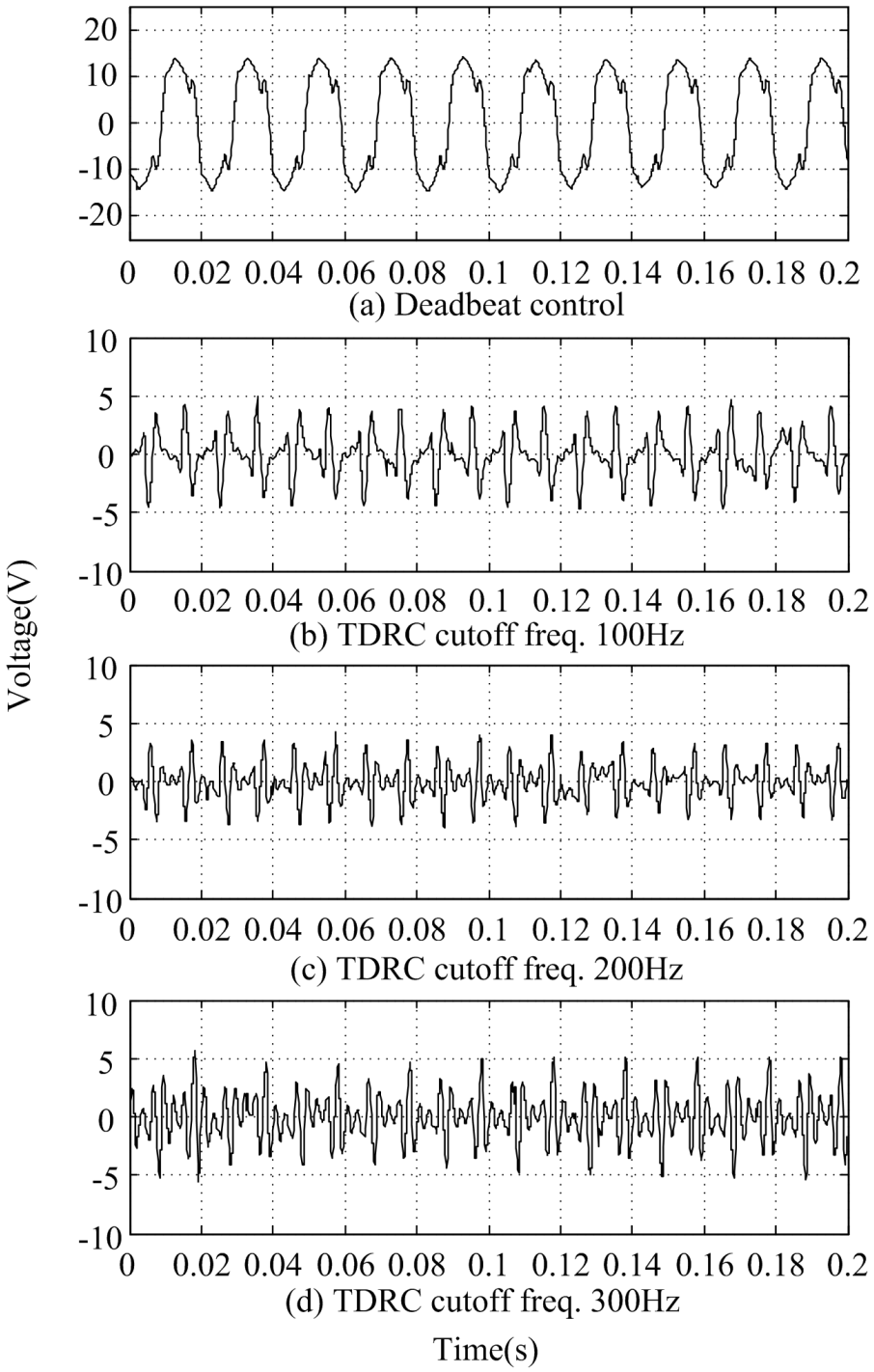


Figure 3.25: Experimental result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

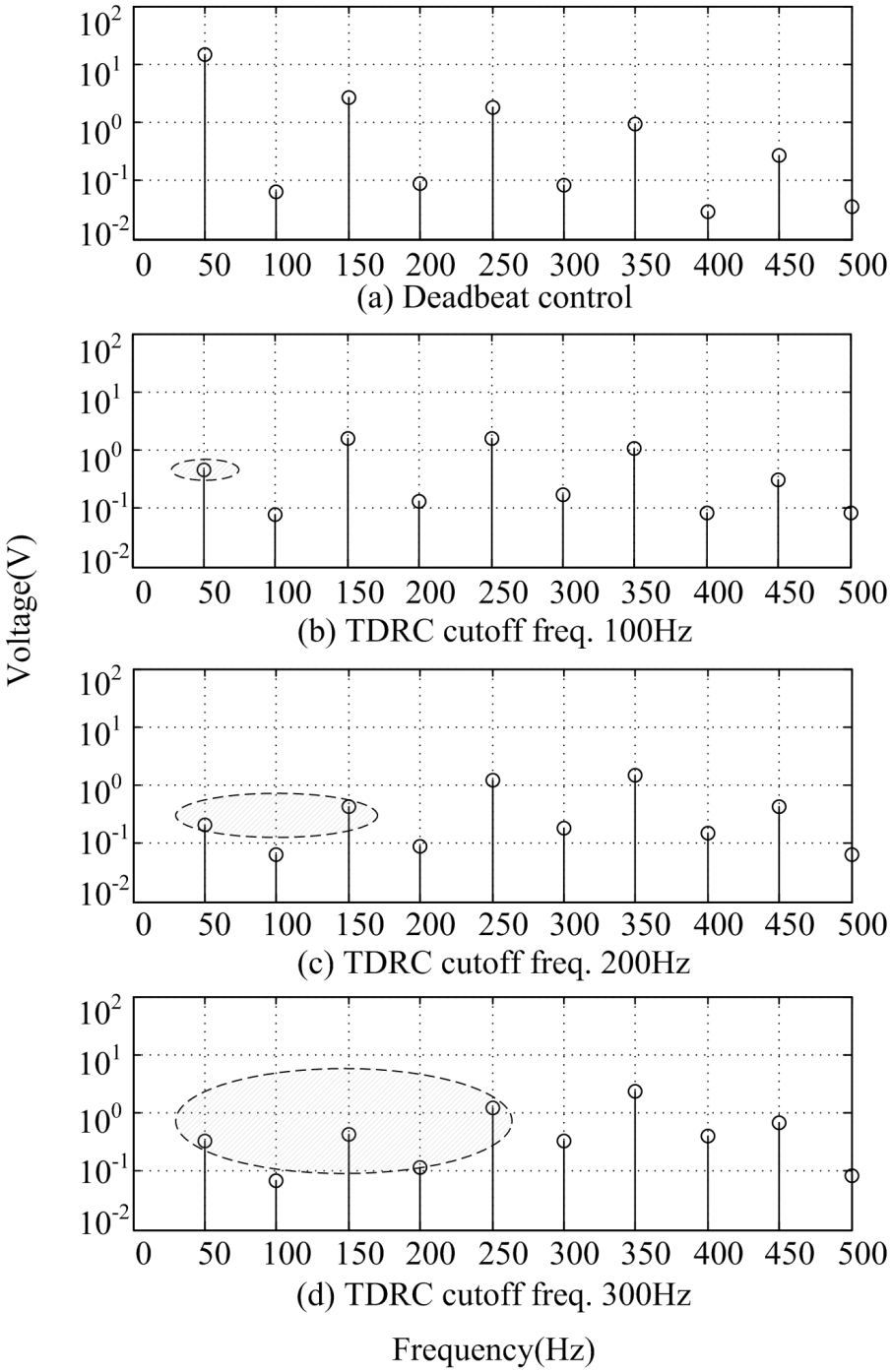


Figure 3.26: Experimental result: error spectrum of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme, with low pass filters cutoff frequency (b) $100\,Hz$ (c) $200\,Hz$ (d)$300\,Hz$

the distortions by a factor of 1.6. However, due to the large contribution of $7th$ and $9th$ harmonic components, the performance of TDRC with cutoff frequency $300\,Hz$ filters is worse than the one with cutoff frequency $200\,Hz$ filters. This is because when the filter cutoff frequency is nearby $7th$ and $9th$ harmonics, there are some small magnitude of $7th$ and $9th$ harmonics learning in TDRC; but for $7th$ and $9th$ harmonics, the phase delay of both the analog filter and digital filters are much higher than the lower frequency harmonics. Hence, the inability to cancel the phase delay will cause $7th$ and $9th$ harmonics increasing significantly. In the next chapter, FDRC is introduced to overcome this problem.

3.4 Conclusion

This chapter presents a time domain based repetitive control scheme for control of a PWM inverter system. This time domain scheme is plugged into a cascaded deadbeat control system to promise both dynamic and steady-state performance of the system. TDRC helps the conventional deadbeat control to overcome the sensitivity of accuracy of model parameters. In addition, it reduces the steady state error by a factor of and 8.7 and 4, and minimizes THD by a factor of 2 and 1.6, respectively for the linear load and nonlinear load conditions in experiment. However, the limitation of fixed operating gain and fixed phase compensation for all the harmonic components deteriorate the performance when the learning frequency increases. This problem is solved effectively by frequency domain based repetitive control scheme as proposed in the next chapter.

Chapter 4

Frequency Domain Based Repetitive Control

4.1 Introduction

In this chapter, a novel repetitive controller based on frequency domain for a single phase inverter is presented. Similar to TDRC, this controller is a plug-in controller working along with the cascaded deadbeat control system. The basic idea of frequency domain repetitive control (FDRC) is to obtain the magnitude and phase of each frequency component using Fourier Series analysis. Subsequently, use these parameters to reconstruct a signal which only contains chosen frequency components for learning. As a result, the chosen frequency components could be easily learned to meet this goal rather than designing filters to eliminate the unwanted harmonic components. Furthermore, comparing with time domain repetitive control scheme, different learning gains and phase delay compensations could be assigned to different frequency components to reduce the tracking error. Besides, it

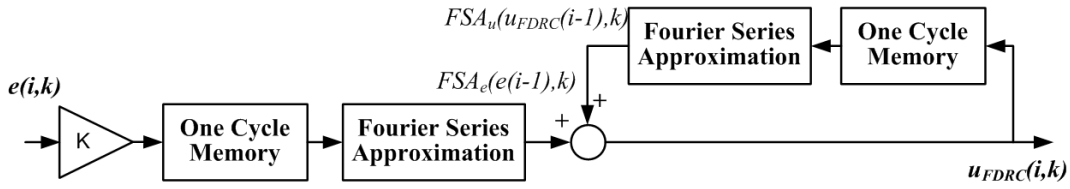


Figure 4.1: Frequency domain repetitive control scheme

does not require the precise parametric model of the system.

4.2 Repetitive Control Based on Fourier series Approximation

The plug-in FDRC block diagram is shown in Fig. 4.1. FDRC control output signal is given as

$$u_{FDRC}(i,k) = FSA_u(u_{FDRC}(i-1),k) + K \cdot FSA_e(e(i-1),k) \tag{4.1}$$

where i - cycle number; k - position interval number; K is the learning gain; $u_{FDRC}(i,k)$ is the control inputs of the present cycle (i^{th} cycle) at k^{th} interval; $u_{FDRC}(i-1)$ and $e(i-1)$ are the control input and tracking error signals respectively in the previous $(i-1)^{th} cycle$; $FSA_e(e(i-1),k)$ and $FSA_u(u_{FDRC}(i-1),k)$ are Fourier series approximations of previous $(i-1)^{th}$ cycle error and control signal at k^{th} interval respectively.

Fourier series approximation is used for error signal $e(i,k)$ and control signal $u_{FDRC}(i,k)$. We represent them as a continuous periodic signal $f(t)$, which is defined over time interval $0 \leq t < T$ for one cycle, can be sampled with sampling

time ΔT, and DFT as

$$f(k\Delta T) = R_0 + \sum_{n=1}^{V-1}(R_n \cos(n\omega k\Delta T) + I_n \sin(n\omega k\Delta T)). \tag{4.2}$$

where

$$R_0 = \frac{\Delta T}{T}\sum_{k=0}^{N-1} f(k\Delta T). \tag{4.3}$$

$$R_n = \frac{2\Delta T}{T}\sum_{k=0}^{N-1} f(k\Delta T)\cos(n\omega k\Delta T). \tag{4.4}$$

$$I_n = \frac{2\Delta T}{T}\sum_{k=0}^{N-1} f(k\Delta T)\sin(n\omega k\Delta T). \tag{4.5}$$

$$n = 1, 2, 3, ..., V-1,\ \ k = 0, 1, 2, ..., N-1$$

where N denotes sampling number in the interval $0 \leq \mathrm{t} < \mathrm{T}$; V is the number of harmonics; $\omega = 2\pi/T$.

Consider the linear load condition, we select $50\,Hz$, $150\,Hz$ and $250\,Hz$ frequency components to learn, and assign learning gain weights according to the magnitude of each component.

In the FDRC updating law, we use the product of frequency components vector and the coefficient vector,where frequency component vector is given as

$$\begin{aligned}\Theta(k\Delta T) = [1 \quad & \cos(k\Delta T) \quad \cos(3k\Delta T) \quad \cos(5k\Delta T) \\ & \sin(k\Delta T) \quad \sin(3k\Delta T) \quad \sin(5k\Delta T)]\end{aligned} \tag{4.6}$$

and coefficient vector of control input $u(i-1)$ is given as

$$\Psi_u(k\Delta T) = [\ R_0 \quad R_1 \quad R_3 \quad R_5 \quad I_1 \quad I_3 \quad I_5\ ]^T \tag{4.7}$$

To assign different gain to FDRC, a gain weight vector is given to $e(i-1)$ as

$$\Psi_e(k\Delta T) = [R_0 \quad W_1R_1 \quad W_3R_3 \quad W_5R_5 \quad W_1I_1 \quad W_3I_3 \quad W_5I_5]^T \tag{4.8}$$

where $[\ W_1 \quad W_3 \quad W_5\ ]$ is gain weight vector. Based on the experience of gain choosing in TDRC controller, gain and gain weights are chosen and tried on the simulation first, then implemented in experiment. The evaluation of the gain choice and stability is rather time consuming and beyond this thesis scope. In every cycle, FDRC updates its coefficient vector based on previous cycle information. Therefore for error signal and control input signal, the updating law is given as

$$FSA_u(f(k\Delta T)) = \Theta(k\Delta T) \times \Psi_u(k\Delta T) \tag{4.9}$$

$$FSA_e(f(k\Delta T)) = \Theta(k\Delta T) \times \Psi_e(k\Delta T) \tag{4.10}$$

4.2.1 Phase Delay Compensations

As shown in Fig. 3.2, analog pre-filters are usually used to eliminate high frequency noise from the feedback sensing signals. However, these filters introduce phase delays in the feedback signals. Additionally, the phase delay for each frequency component is not the same and differ from one to another. For higher frequency components, the phase delays are larger. For example, for $50\,Hz$, $150\,Hz$, $250\,Hz$, $350Hz$, and $450\,Hz$, the phase lag are respectively 14.1°, 38.6°, 57.3°, 71.2°, and 81.1°. To compute and extract the phase lag of each harmonic frequency, only the system output voltage data are needed to be computed to extract the information

of each harmonics. Due to the presence of phase delay, the error that we are trying to eliminate in controller is not same as the actual tracking error. This phase delay problem which commonly exists in all control systems gives rise to ineffective error minimization. The TDRC could compensate the phase delay of fundamental frequency by adding the delay compensation z^{d_a} as shown in Fig. 3.3, but certainly it will not match the phase delay of other harmonic components. In FDRC, phase compensation could be easily added into eqn. (4.6), so that Θ can be modified to

$$\Theta_{pc}(k\Delta T) = [1 \quad \begin{matrix} \cos(k\Delta T + \alpha_1) & \cos(3k\Delta T + \alpha_2) & \cos(5k\Delta T + \alpha_3) \\ \sin(k\Delta T + \alpha_1) & \sin(3k\Delta T + \alpha_2) & \sin(5k\Delta T + \alpha_3)] \end{matrix} \tag{4.11}$$

Therefore, the Fourier series approximation updating law for error signal is modified as

$$FSA_e(f(k\Delta T)) = \Theta_{pc}(k\Delta T) \times \Psi_e(k\Delta T) \tag{4.12}$$

4.2.2 Simulation Results Using Frequency Domain Based Repetitive Control for Inverter

4.2.2.1 Linear Load

To investigate the performance of the proposed FDRC control scheme, simulation tests were carried out in the same software environment and plant parameters as described in Chapter 2. Error spectrum in Fig. 2.18 (b)(pp.41) shows that the 1^{st}, 3^{rd}, 5^{th} harmonic components are the most dominant components in output voltage tracking error with a linear load. Consequently, the three dominant harmonics are incorporated in learning of FDRC.

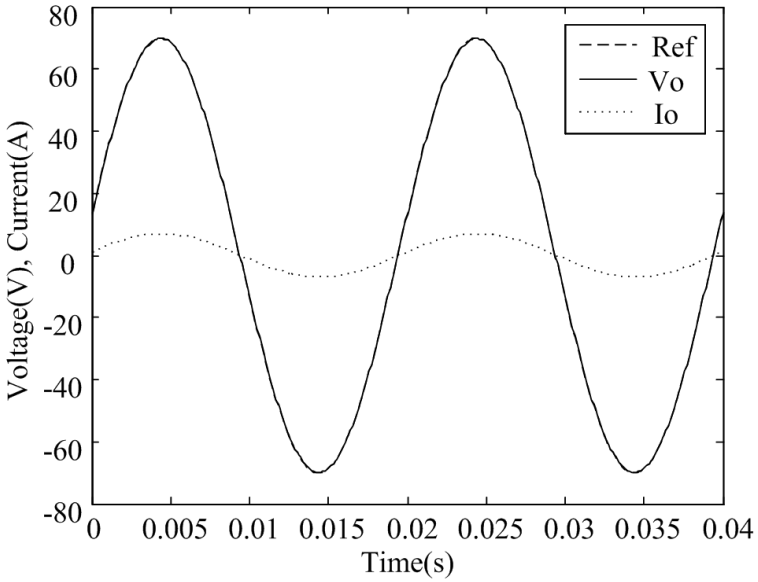


Figure 4.2: Simulation result: steady state output voltage of the inverter system under a linear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

The output voltages in steady state are shown in Fig.4.2. Cutoff frequency of low pass filters in TDRC are set to $300\,Hz$. Comparing to the output voltage using deadbeat controller, we can see that the plug-in frequency domain repetitive controller removes the phase delay of output voltage. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed FDRC control scheme with different learning frequency components are shown in Fig. 4.3. Tracking error is significantly reduced from $8.9\,V$ to $0.09\,V$, $0.07\,V$ and $0.06\,V$ respectively, which is at least four times less than the error that is obtained using TDRC. From the frequency spectra as shown in Fig. 4.4, the frequency components which are chosen are reduced significantly. THD is reduced from $0.4\,\%$ (deadbeat control) to $0.2\,\%$, $0.1\,\%$, $0.05\,\%$ respectively. These data show that the proposed frequency domain repetitive control scheme reduce the output

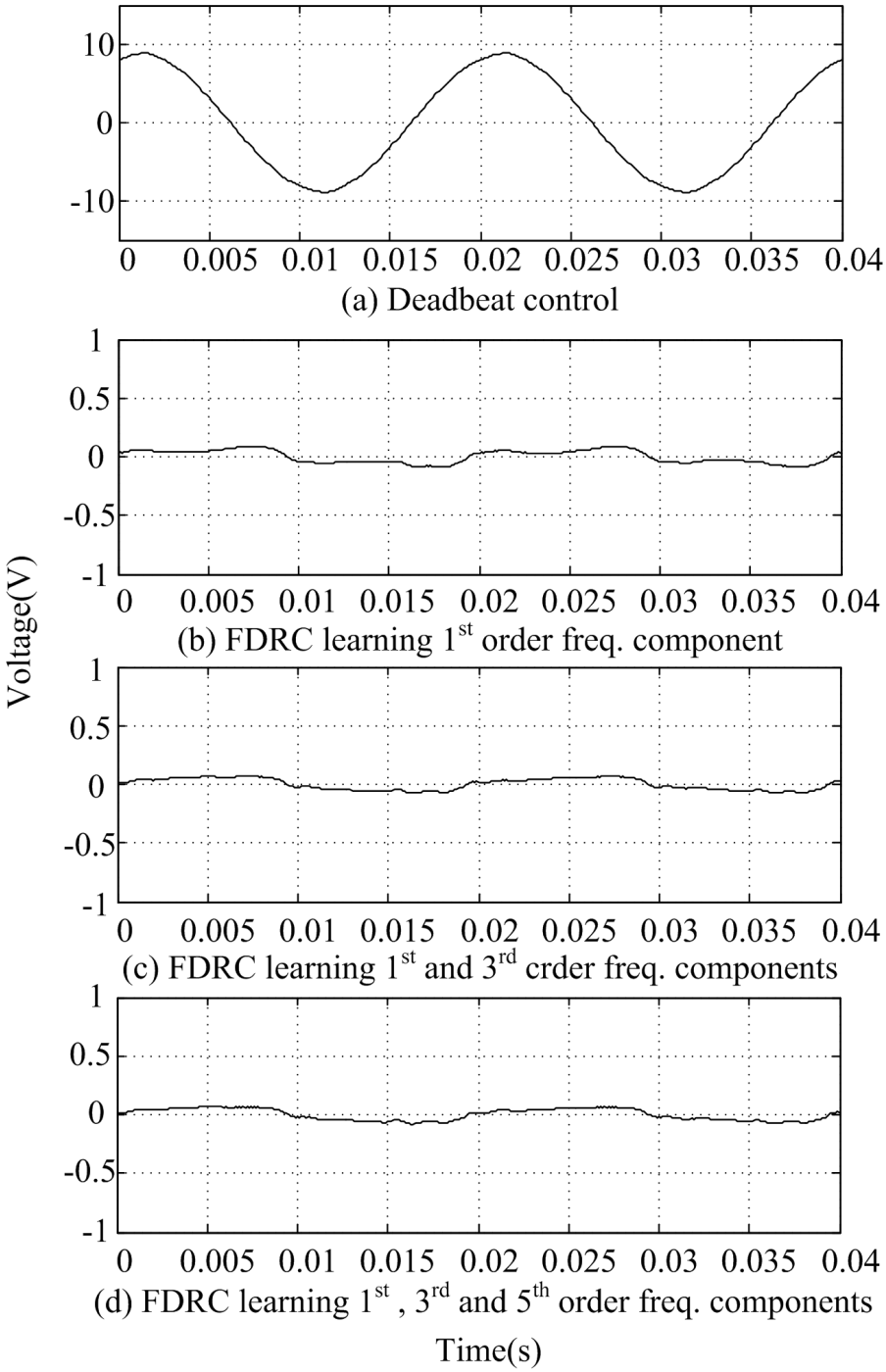


Figure 4.3: Simulation result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using FDRC control scheme, learning (b) 1^{st} (c) 1^{st} and 3^{rd} (d)1^{st}, 3^{rd}, and5^{th} frequency components

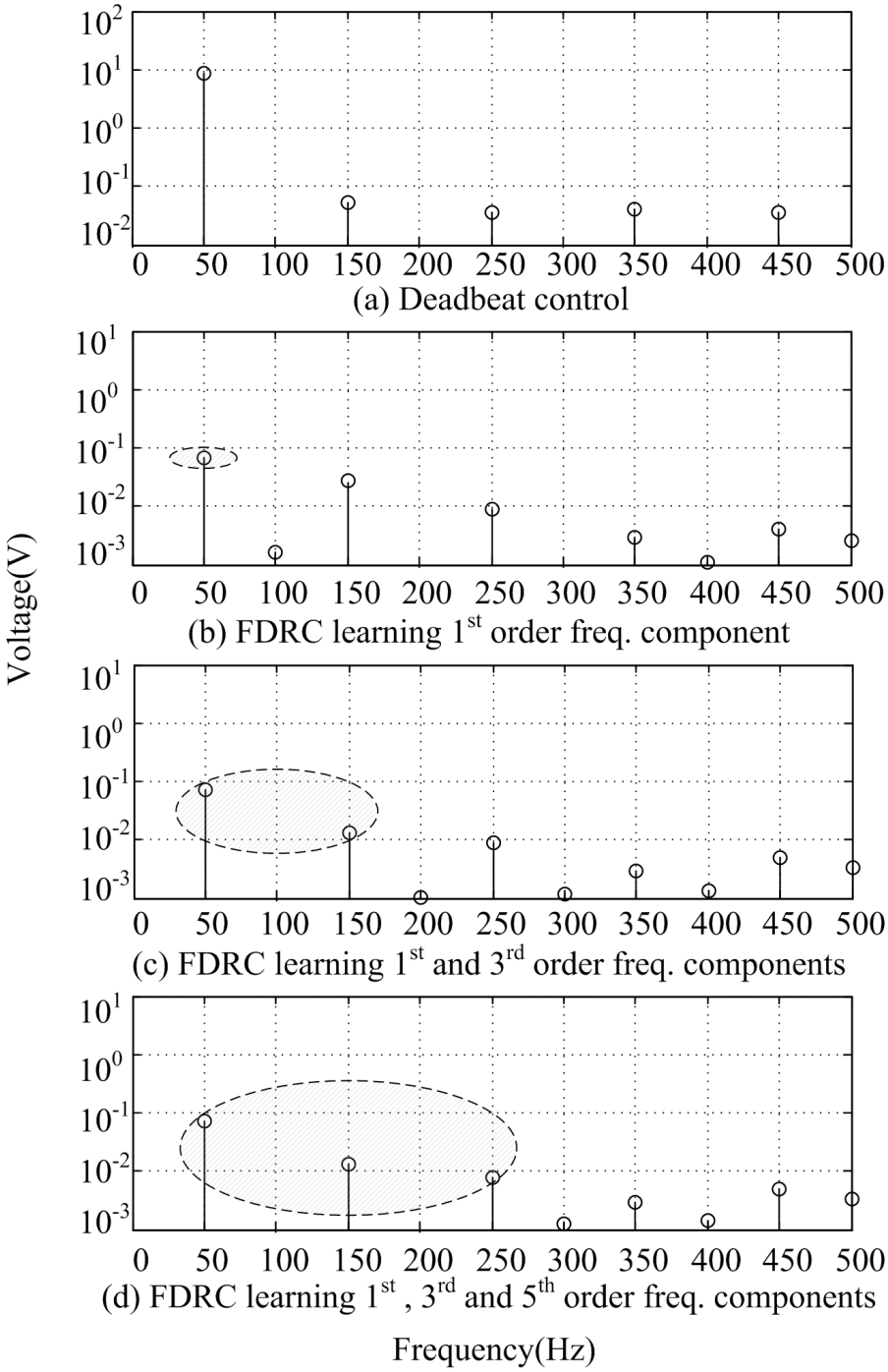


Figure 4.4: Simulation result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using FDRC control scheme, learning (b) 1^{st} (c) 1^{st} and 3^{rd} (d)1^{st}, 3^{rd}, and5^{th} frequency components

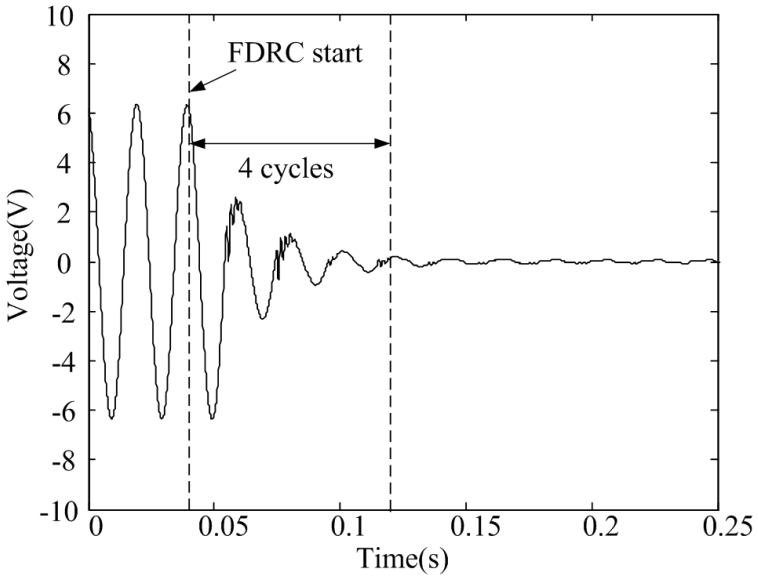


Figure 4.5: Simulation result: error of the output voltage of the inverter system in transient under a linear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

distortions effectively. Comparing to TDRC, FDRC gives more improved results due to its advantages we mentioned before. Dynamic response using the FDRC control scheme is shown in Fig. 4.5. The voltage error converges to the minimum value in four cycles.

4.2.2.2 Nonlinear Load

Using deadbeat control, the error spectrum under a nonlinear load in Fig. 2.22 (b) (pp.43) shows that the 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components are the most dominant components in output voltage tracking error with a nonlinear load. The output voltages in steady state are shown in Fig.4.6 - 4.10. Choosing 1^{st} order harmonic component as shown in Fig. 4.6 and 1^{st} and 3^{rd} order harmonic com-

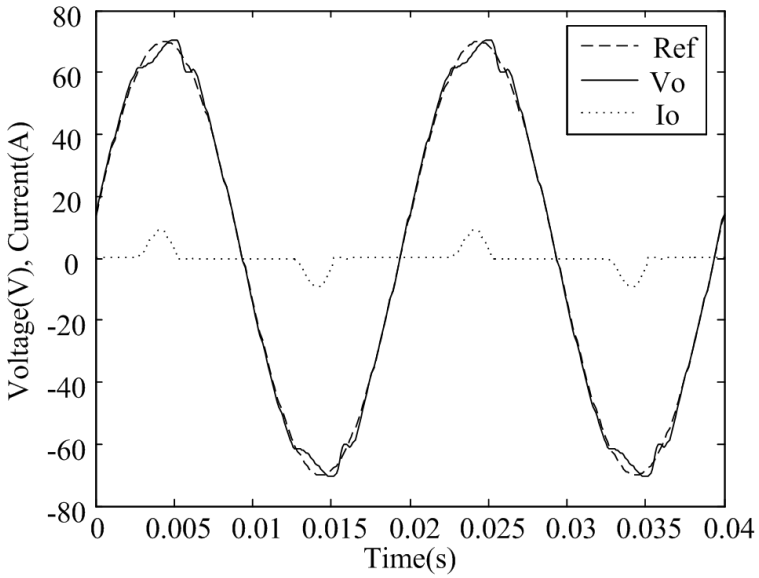


Figure 4.6: Simulation result: steady state output voltage of the inverter system under a noninear load using FDRC control scheme, learning the 1^{st} harmonic components

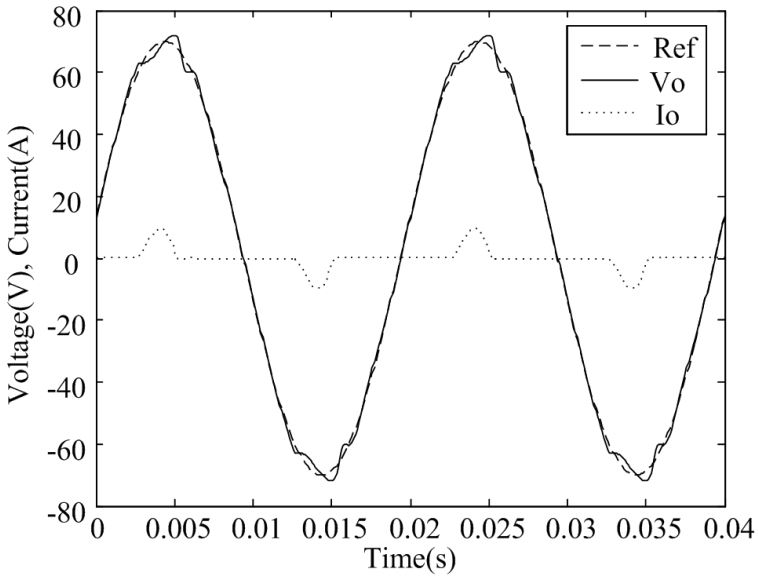


Figure 4.7: Simulation result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st} and 3^{rd} harmonic components

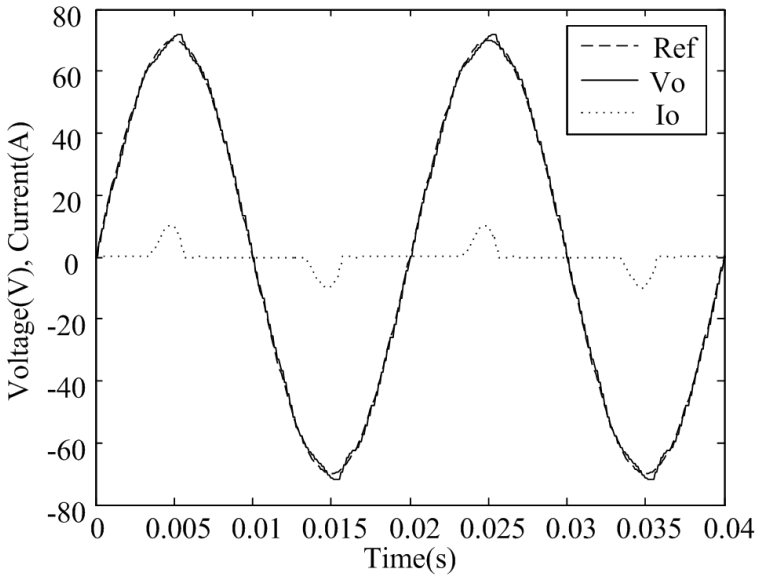


Figure 4.8: Simulation result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

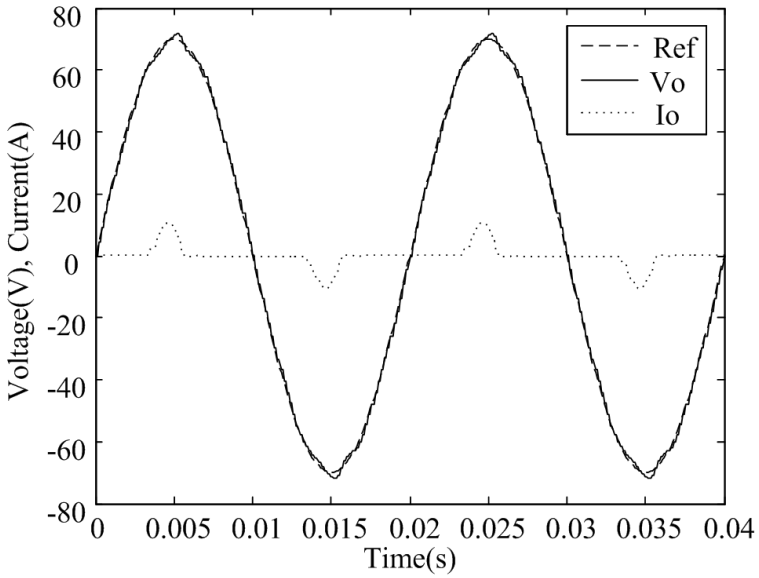


Figure 4.9: Simulation result: steady state outputvoltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, 5^{th} and 7^{th} harmonic components

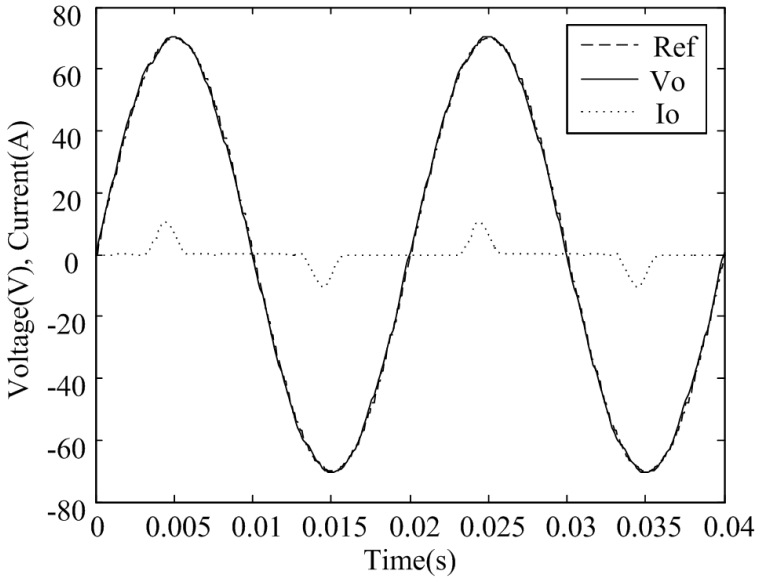


Figure 4.10: Simulation result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

ponents as shown in Fig. 4.7, the output voltage track the reference with a much reduced tracking error comparing with the results by using TDRC control scheme. In Fig. 4.10, FDRC helps the output voltage almost tracking the reference exactly under a nonlinear load. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed FDRC control scheme with different frequency components are shown in Fig. 4.11. Tracking error is significantly reduced from $7.8\,V$ to $1.8\,V$, using FDRC controller compared with cascade deadbeat control. The maximum tracking error is half of the maximum tracking error achieved using TDRC ($3.7\,V$). From the frequency spectrum, the harmonics are reduced significantly when they are included in FDRC. THDs are reduced from 3.8% to 0.8% under a nonlinear load, where as the lowest THD of TDRC is 2.7% under the same operation conditions. All the figures and data show the effectiveness of

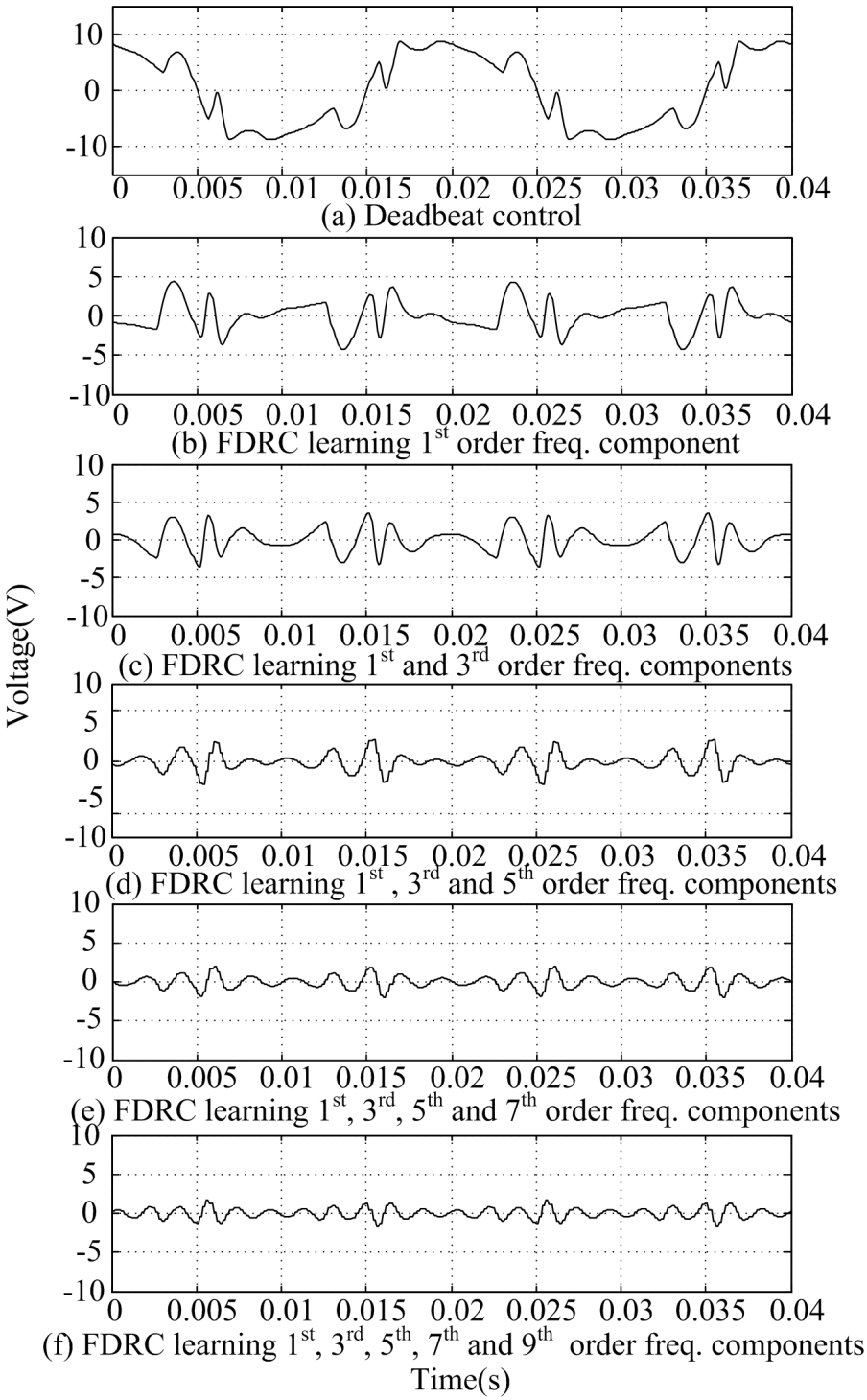


Figure 4.11: Simulation result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme learning the (b) 1^{st} (c) 1^{st} and 3^{rd} (d) 1^{st}, 3^{rd} and 5^{th} (e) 1^{st}, 3^{rd}, 5^{th} and 7^{th} (f) 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

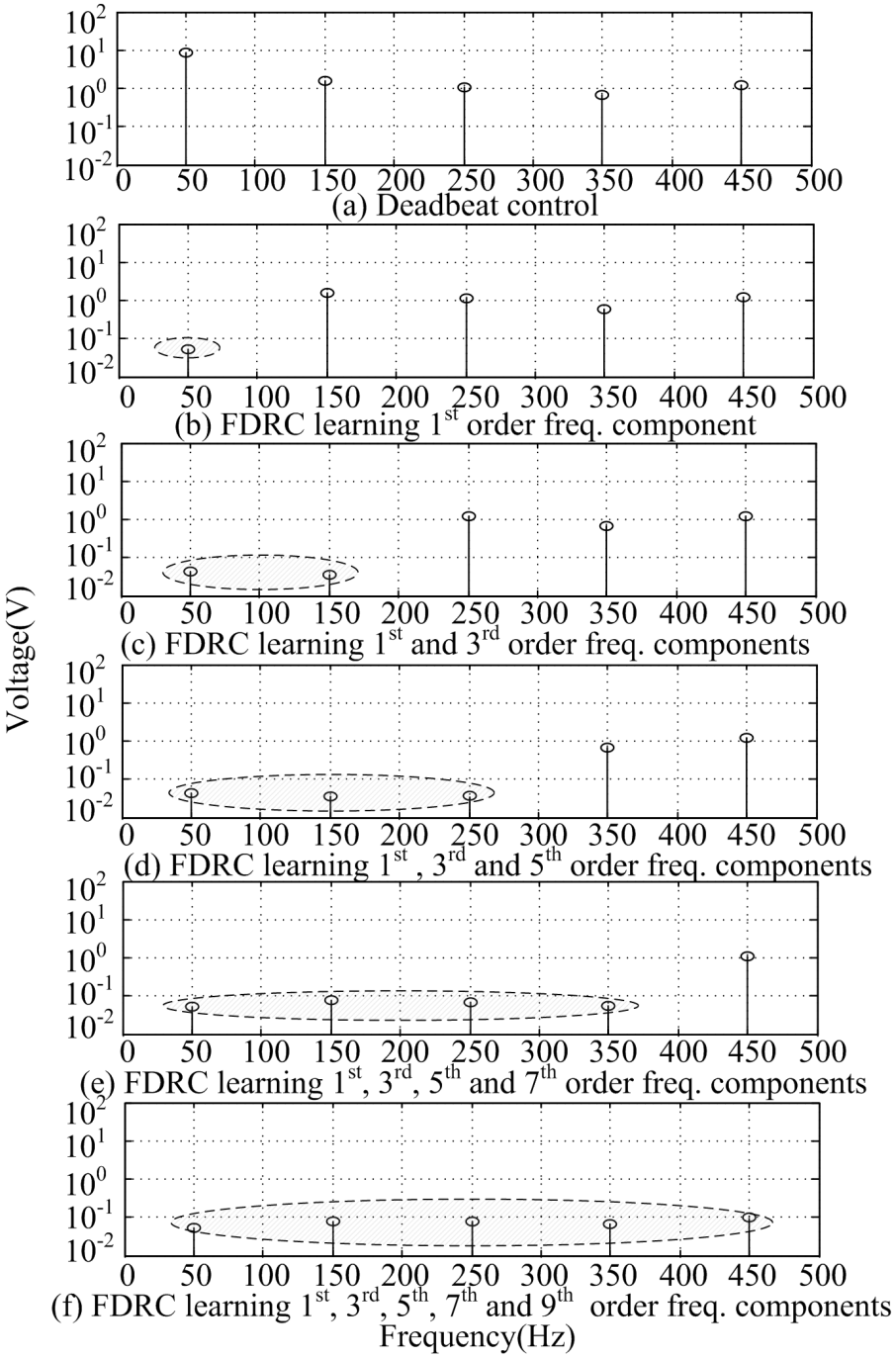


Figure 4.12: Simulation result: error spectrum of output vVoltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control sScheme learning the (b) 1^{st} (c) 1^{st} and 3^{rd} (d) 1^{st}, 3^{rd} and 5^{th} (e) 1^{st}, 3^{rd}, 5^{th} and 7^{th} (f) 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

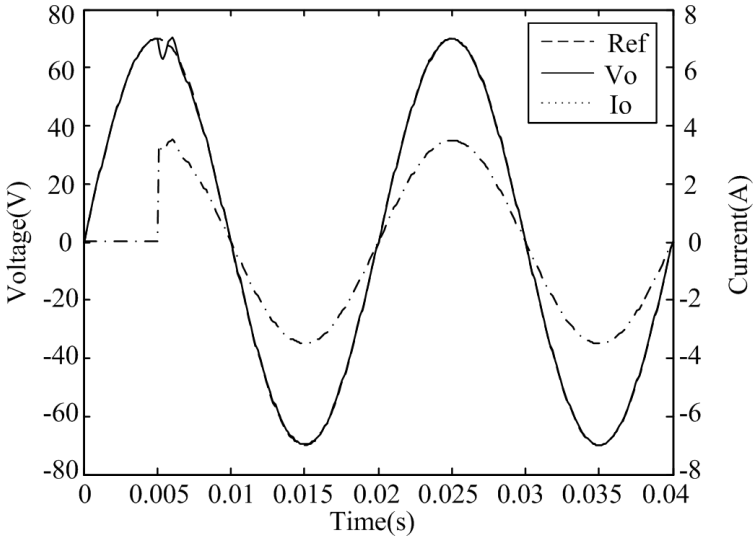


Figure 4.13: Simulation result: Transient response of the inverter system in steady state with a step load using FDRC control scheme

the proposed FDRC control scheme. With the ability of choosing different gains and different phase compensations for each frequency component, FDRC gives a better performance than the conventional repetitive controller, especially under a nonlinear rectifier load.

4.2.2.3 Load Change

To test the dynamic performance of inverter system, simulation of large load change was carried out. Fig. 4.13 shows the simulation result of fast dynamic response consistent with TDRC control scheme. The maximum inverter output voltage drop is less than 10% of its amplitude with a $4\,A$ step change of current. Voltage tracking is recovered within $0.002\,s$. THD is less than 2.2% during the transient period.

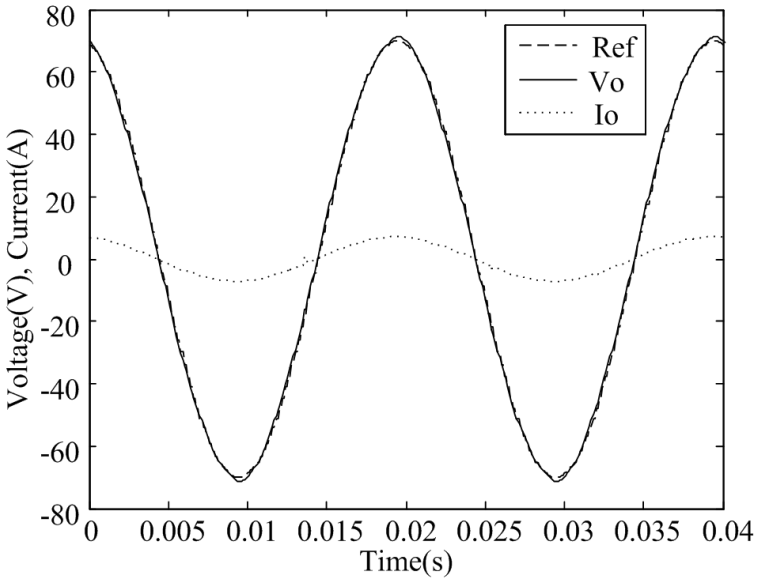


Figure 4.14: Experiment result: steady state output voltage of the inverter system under a linear load using FDRC control scheme, learning the 1^{st} harmonic components

4.2.3 Experimental Results Using Frequency Domain Repetitive Control for Inverter

4.2.3.1 Linear Load

To prove the coherence of the simulation results, and to further evaluate the performance using FDRC control scheme, experiment results are shown in the following part. Same as in the simulation, the first three dominant harmonics are incorporated in learning of FDRC under a linear load.

The output voltages in steady state are shown in Fig.4.14 - 4.16. Comparing with the output voltage using deadbeat controller, we can see that with the plug-in frequency domain based repetitive controller there is no phase delay between output

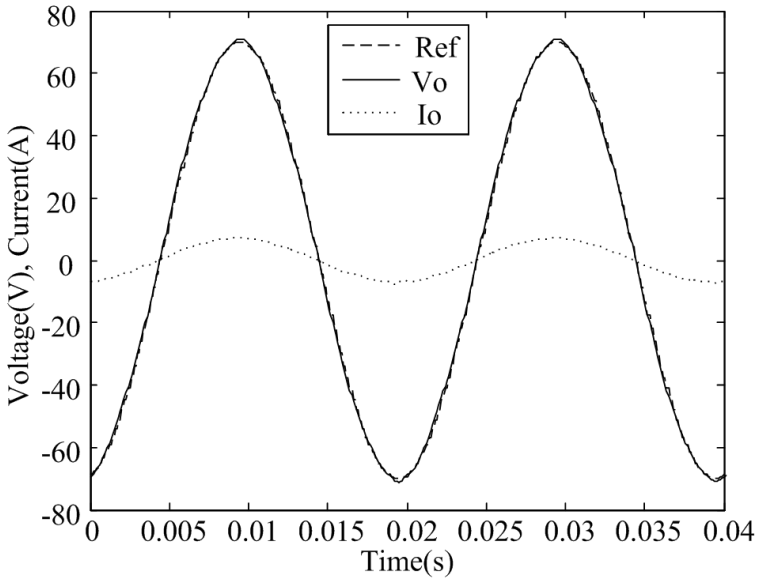


Figure 4.15: Experiment result: steady state output voltage of the inverter system under a linear load using FDRC control scheme, learning the 1^{st} and 3^{rd} harmonic components

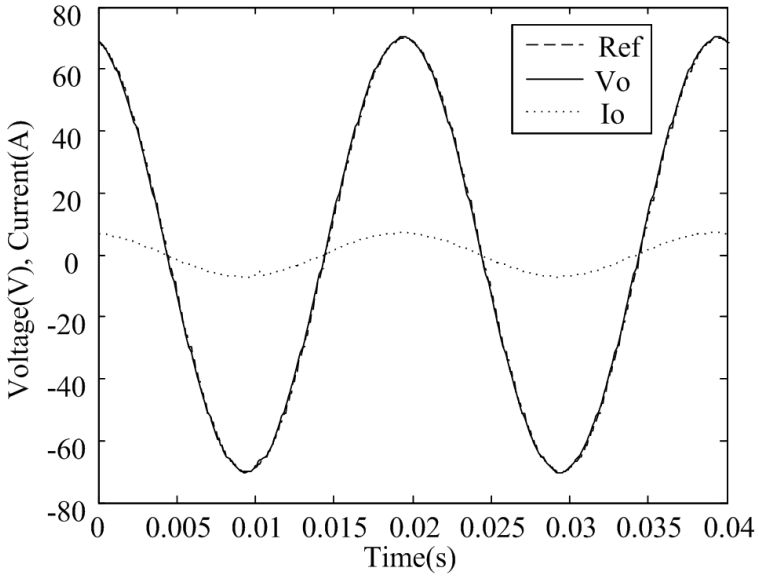


Figure 4.16: Experiment result: steady state output voltage of the inverter system under a linear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

voltage and reference voltage. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed FDRC control scheme with different learning frequency components are shown in Fig. 4.17. Tracking error is significantly reduced from $13\,V$ to $1.8\,V$, $1.8\,V$ and $1.1\,V$ respectively, which is slightly less than the error using TDRC. Notice that FDRC reduces the maximum error to 1/4 of the maximum error achieved by using TDRC under the same load condition in simulation, we should point out that in a real-time application, error less than 1 % of the peak voltage is too small to minimize further. From the frequency spectrum as shown in Fig. 4.18, the frequency components which are chosen are reduced significantly. THD is reduced from 1.5 % (deadbeat control) to 1.2 %, 1.0 %, 0.6 % respectively. These data show that the proposed frequency domain repetitive control scheme reduces the output distortions effectively. Comparing to TDRC, FDRC gives a lower THD of 0.6 % as compared to 0.9 % in TDRC. As shown in Fig. 4.19, error of voltage converges in four cycles, two times faster than TDRC dynamic response with experimental test results. The faster response is due to the freedom of choosing different gains for different frequency components in the FDRC. Although higher frequency need smaller gain to ensure the convergence, a higher gain could be given to the low frequency learning which improves the dynamic response.

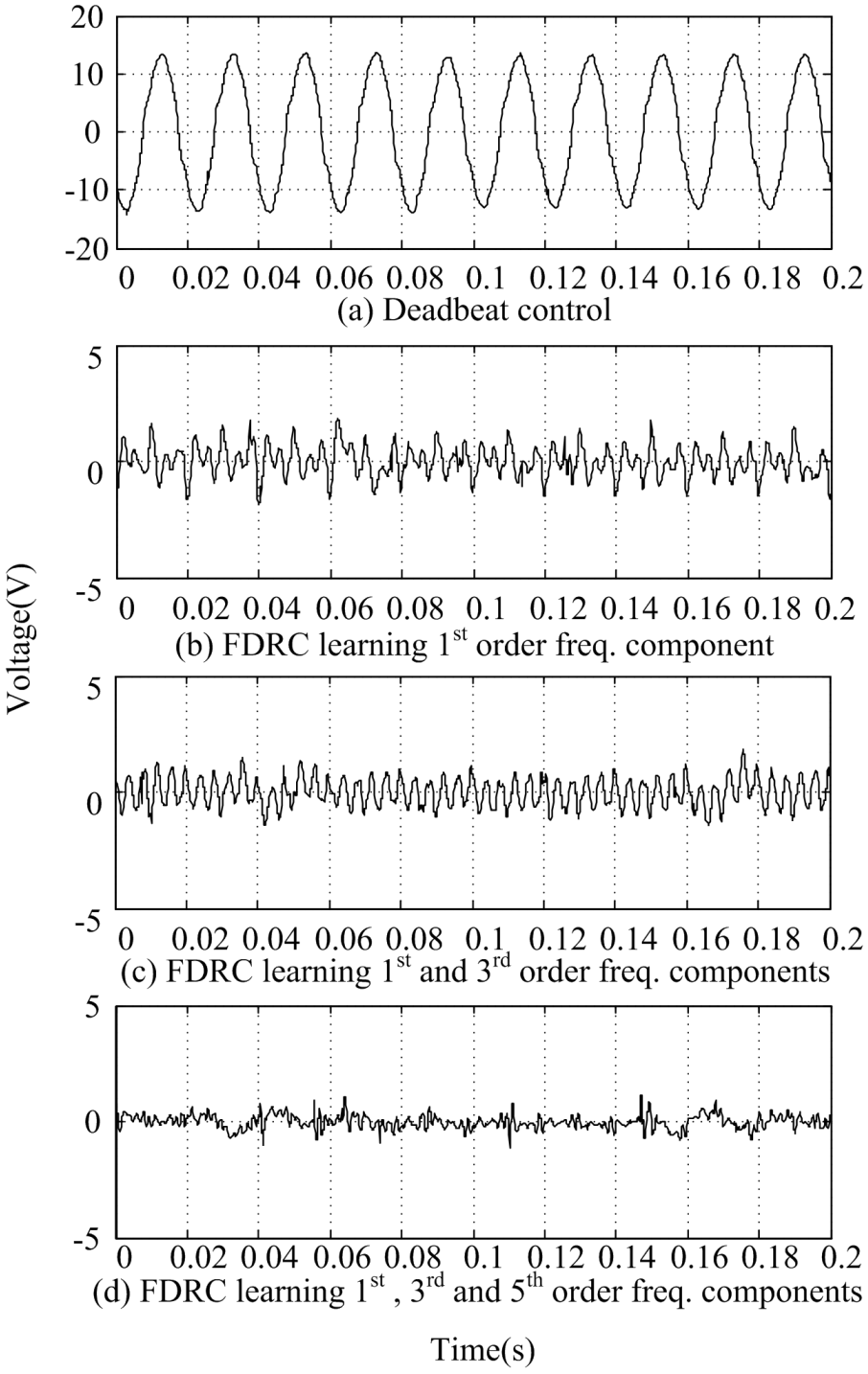


Figure 4.17: Experiment result: tracking error of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using FDRC control scheme, learning (b) 1^{st} (c) 1^{st} and 3^{rd} (d)1^{st}, 3^{rd}, and5^{th} frequency components

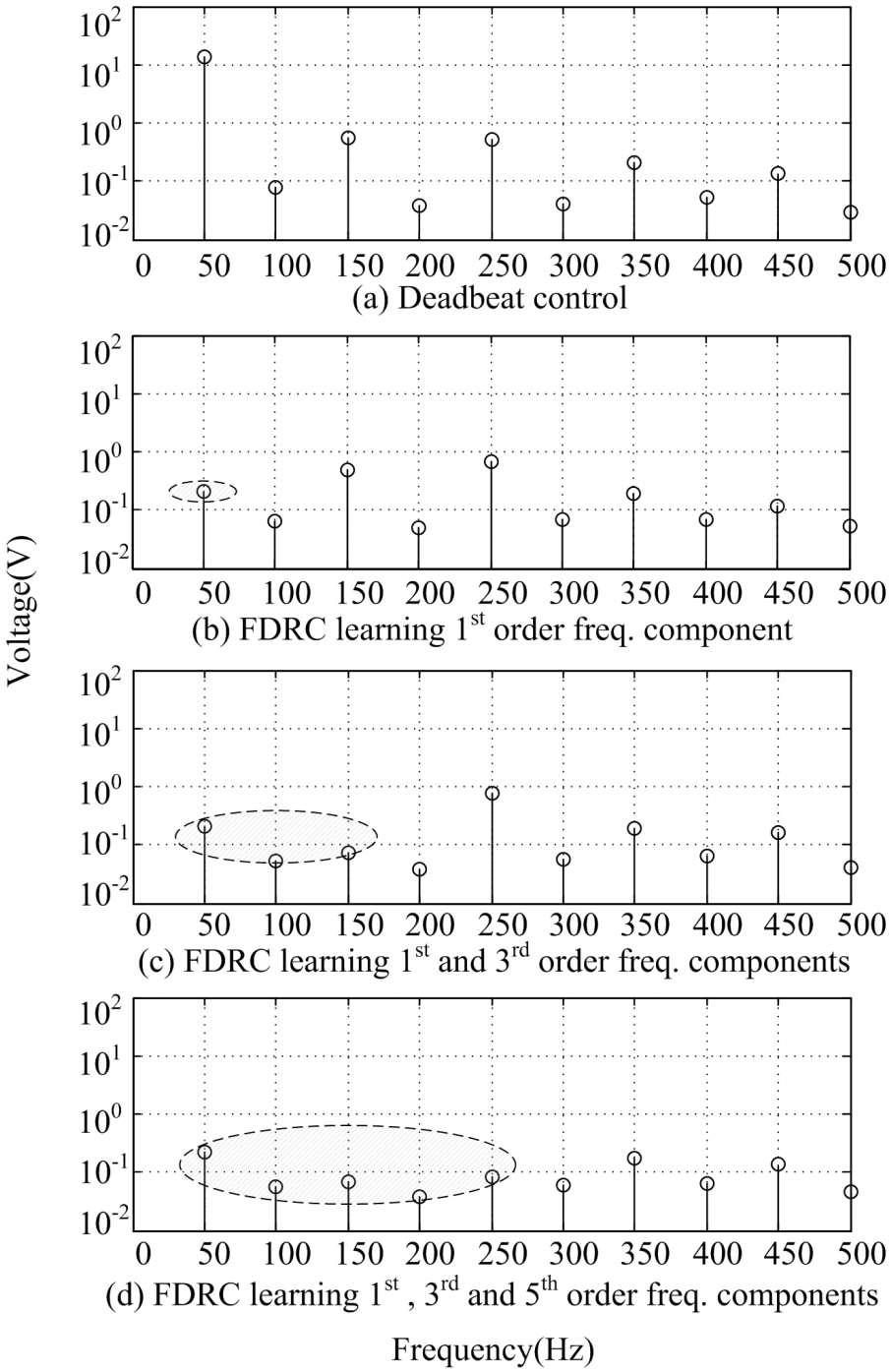


Figure 4.18: Experiment result: error spectrum of output voltage of the inverter system in steady state under a linear load (a) using cascaded deadbeat control, and using FDRC control scheme, learning (b) 1^{st} (c) 1^{st} and 3^{rd} (d) 1^{st}, 3^{rd}, and5^{th} frequency components

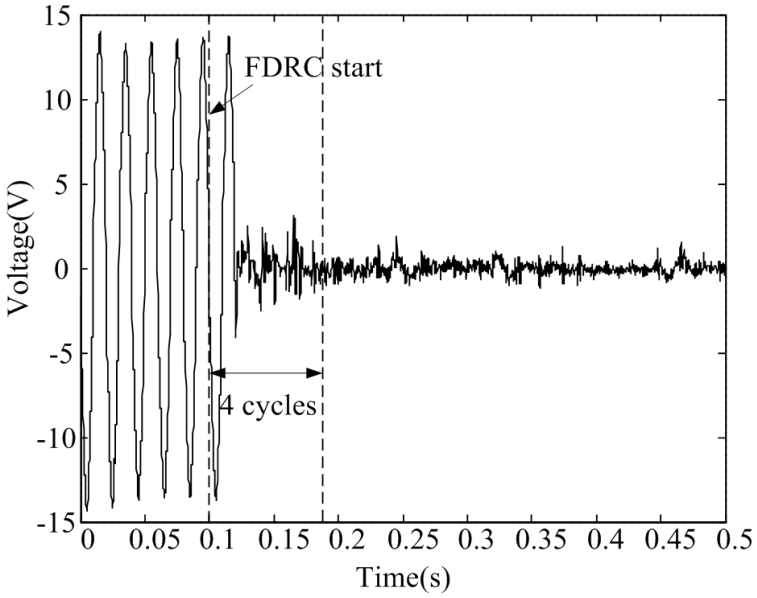


Figure 4.19: Experiment result: error of the output voltage of the inverter system in transient under a linear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

4.2.3.2 Nonlinear Load

Under a nonlinear load, the output voltages in steady state are shown in Fig. 4.20-Fig. 4.24. Similarly as in simulation, FDRC including the first 5 odd harmonics helps the output voltage track the reference without obvious distortions under a nonlinear load. Tracking errors of output voltage in steady state using the cascaded deadbeat controller and the proposed FDRC control scheme with learing frequency components are shown in Fig. 4.25. Tracking error is significantly reduced from $14\,V$ to $2\,V$, using FDRC controller compared with cascaded deadbeat control. The maximum tracking error is 75 % less than the maximum tracking error obtained using TDRC scheme $(3.5\,V)$. From the frequency spectrum as shown in Fig. 4.26, the harmonics are reduced significantly when they are included in learn-

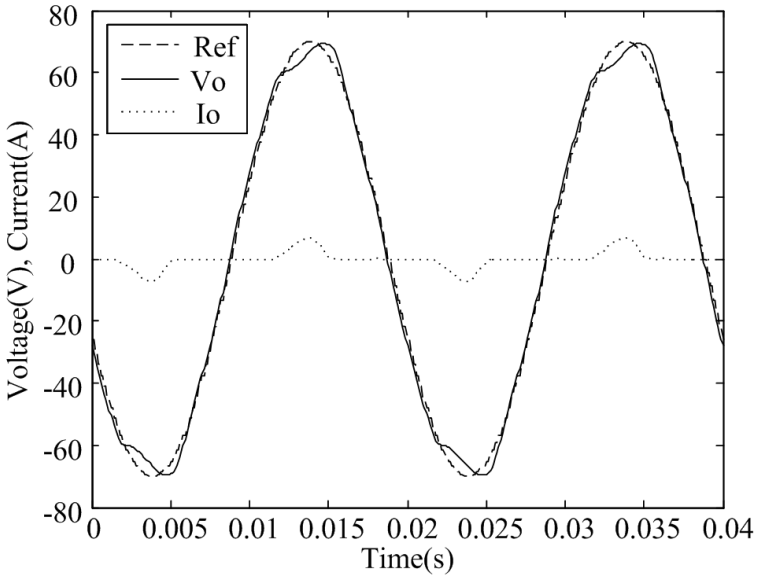


Figure 4.20: Experiment result: steady state output voltage of the inverter system under a noninear load using FDRC control scheme, learning the 1^{st} harmonic components

ing of FDRC. THD are reduced from 4.9 % to 1.0 % under a nonlinear load, where as the lowest THD of TDRC is 3.0 % under the same operation conditions. Experimental results show the consistency with simulation results and the effectiveness of the proposed FDRC control scheme. A comparison between time domain repetitive control and frequency domain repetitive control is given in the following:

1) FDRC uses Fourier Series approximation method to reconstruct signals in which frequency components can be chosen easily. TDRC uses previous cycle signal and filters to remove the frequency components which are not to be learned, and it requires complex digital filter design.

2) Learning gain could be different from one frequency component to other in FDRC. One has the freedom to choose frequency component and give learning

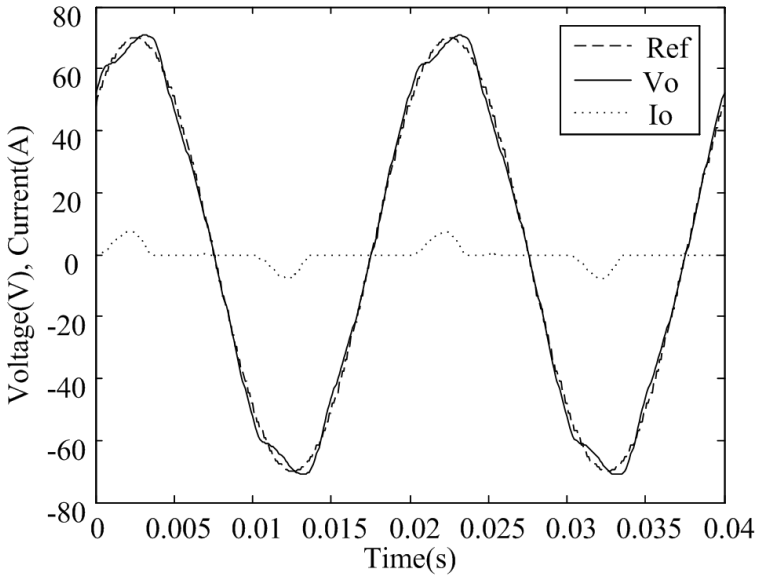


Figure 4.21: Experiment result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st} and 3^{rd} harmonic components

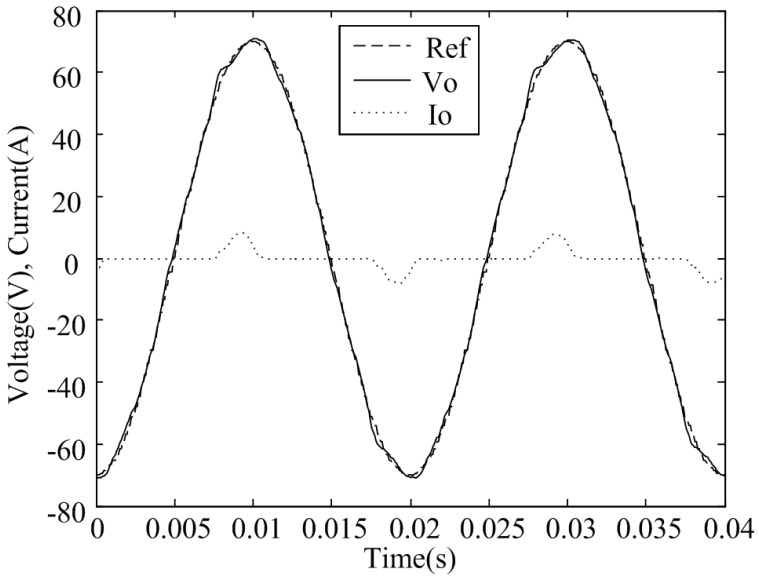


Figure 4.22: Experiment result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, and 5^{th} harmonic components

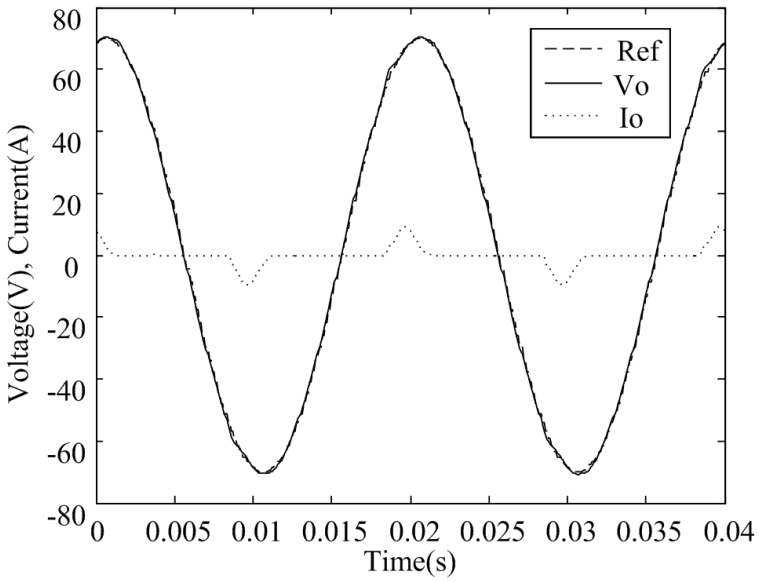


Figure 4.23: Experiment result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, 5^{th} and 7^{th} harmonic components

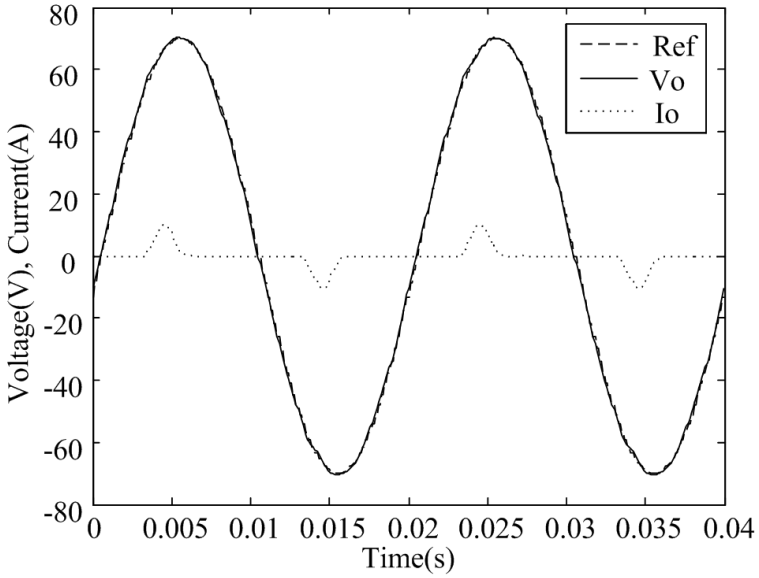


Figure 4.24: Experiment result: steady state output voltage of the inverter system under a nonlinear load using FDRC control scheme, learning the 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

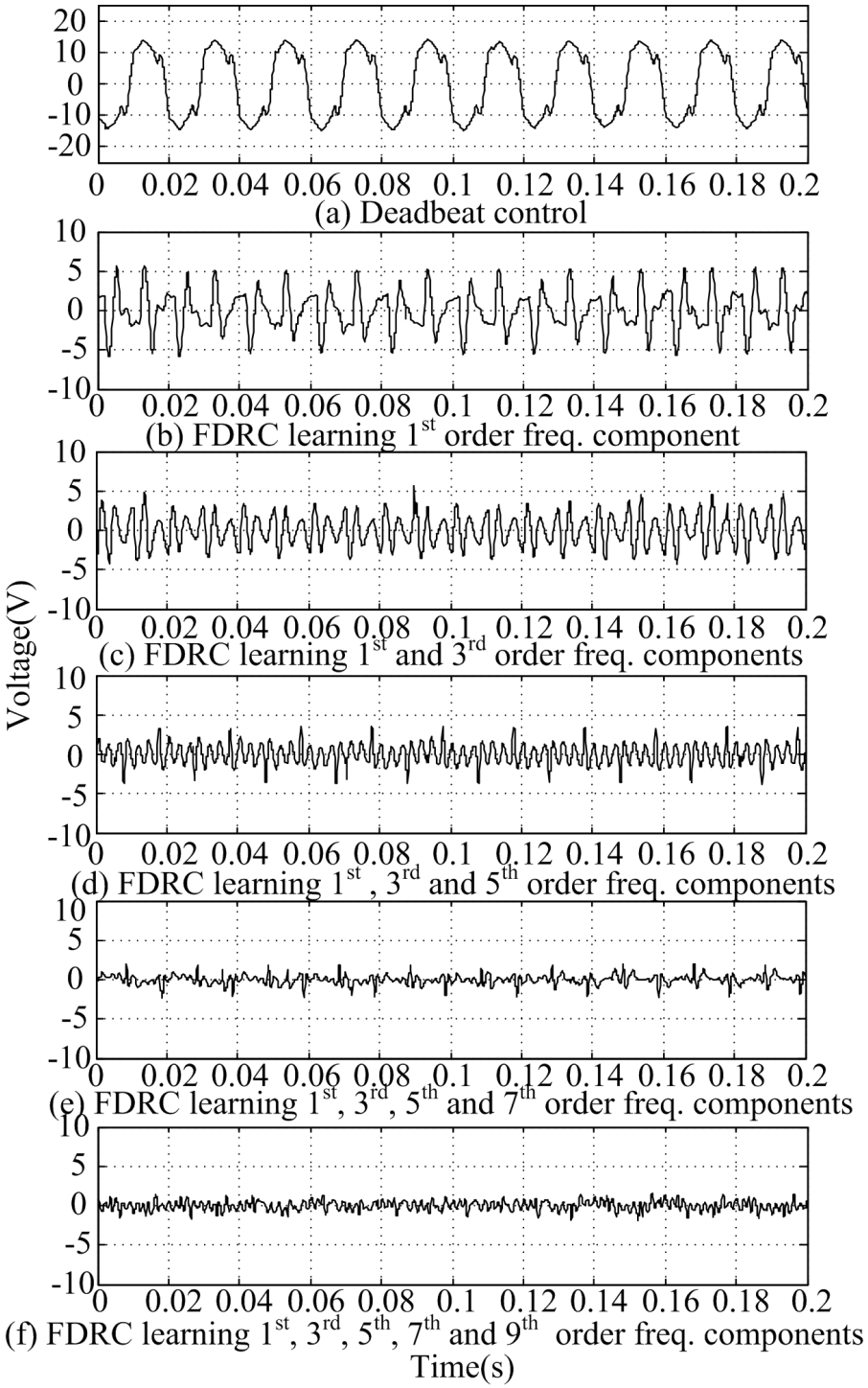


Figure 4.25: Experiment result: tracking error of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme learning the (b) 1^{st} (c) 1^{st} and 3^{rd} (d) 1^{st}, 3^{rd} and 5^{th} (e) 1^{st}, 3^{rd}, 5^{th} and 7^{th} (f) 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

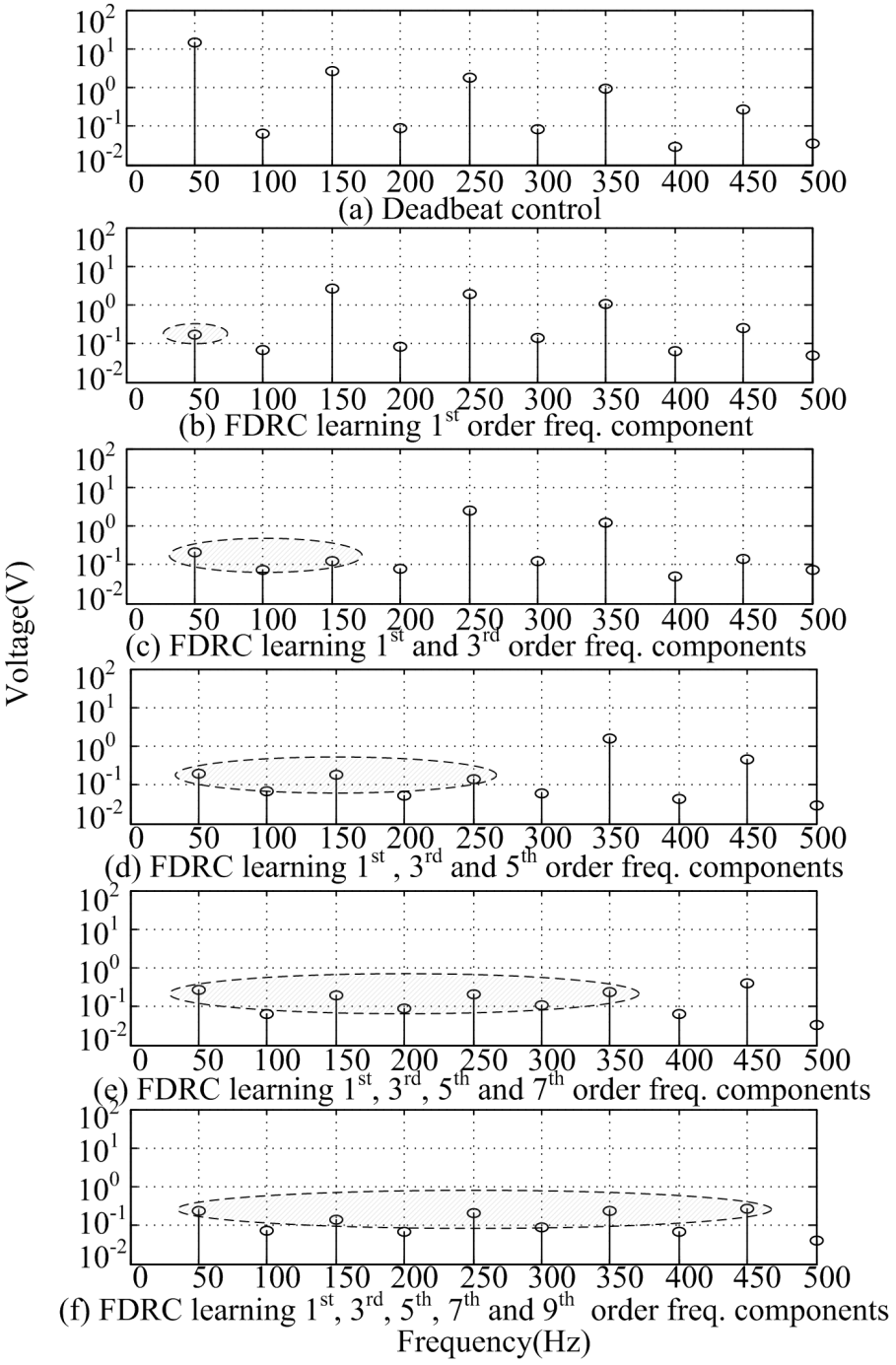


Figure 4.26: Experiment result: error spectrum of output voltage of the inverter system in steady state under a nonlinear load (a) using cascaded deadbeat control, and using TDRC control scheme learning the (b) 1^{st} (c) 1^{st} and 3^{rd} (d) 1^{st}, 3^{rd} and 5^{th} (e) 1^{st}, 3^{rd}, 5^{th} and 7^{th} (f) 1^{st}, 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonic components

gain's weight based on error spectrum. In contrast in TDRC, only one learning gain is used for the whole range of frequency components. Therefore, compared to TDRC, FDRC gives a faster convergence.

3) In FDRC phase compensation for each frequency component can be added directly. In TDRC, only one fixed phase compensation for every frequency component can be added. Hence, FDRC improves the steady state tracking error of output voltage further.

4) TDRC is better than FDRC in terms of implementation. It does not require either memory space for the analysis of the output voltage or computation of the amplitude and phase angle of the harmonics. However, FDRC requires to store only 100 sample voltages in each cycle ($0.02\,s$), and the computation of Fourier analysis is carried out once in every cycle. This should not be a problem for a low end microcontroller or DSP. Moreover, FDRC has many good merits stated above which TDRC does not have. Therefore, FDRC is still a good choice of inverter power supply control.

4.3 Conclusion

This chapter presents a frequency domain repetitive control scheme for control of a PWM inverter system. The frequency domain repetitive control scheme gives an outstanding performance of the control system. It reduces the steady state error by a factor of and 12 and 7, and minimize THD by a factor of 2.5 and 5, respectively

for the linear load and nonlinear load conditions in experiment. It solved the phase delay problem which is raised in the conventional time domain based repetitive control. Furthermore, it gives a faster response due to the flexibility of using different gains for different frequency components in learning.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The thesis deals with high performance control on DC-AC inverter system using two repetitive control methods. AC power supply systems such as UPS require a low harmonic distortions, small steady-state error, and fast dynamic response for the output voltage. However, the inverter output voltage gets distorted due to effect of load disturbance, DC-link voltage variation, PWM modulation pulse harmonics, effect of switching dead-time, and measurement errors. In this thesis, two harmonic distortion minimization schemes for the inverter system using the time-domain based repetitive control method and the frequency-domain based repetitive control method are proposed, implemented and evaluated.

Many control methods have been proposed in literature to improve the performance of DC-AC inverter. Deadbeat control, sliding-mode control, and neural network control are able to provide an output voltage waveform with low harmonic

distortions. However, all of them have some difficulties in information acquisition such as precise parameters of the system model, state variables, or a large pattern database. Therefore, a more simple yet effective approach is required. Recognizing the effectiveness of the repetitive control in suppressing periodic disturbances, in the face of modelling uncertainties, two repetitive control schemes based on time domain and frequency domain are employed to achieve voltage distortions minimization.

A mathematical model of the inverter system is presented in this thesis. Using an inaccurate information of the model, the problem of deadbeat control is revealed by analysis, simulation and experiment results. The two repetitive controllers are plugged into the same deadbeat controller to show their effectiveness.

Time domain based repetitive control scheme makes use of error signal of the previous cycle. Due to the limitation of repetitive control on learning high frequency components, the bandwidth of learning controller has to be selected accordingly. With appropriate filters to remove the unwanted frequency components which are not to be learnt, this scheme reduces the error of voltage greatly and decrease the harmonic distortions further. In addition, a precise model of the system is not necessary. The learning gain can be changed easily during the process of learning to control the convergence speed.

However, a problem of phase delay caused by digital and analog filters gives rise to ineffective error minimization in repetitive control. Hence, this approach

requires complex digital filter design to minimize the phase delay caused by the digital filters. Moreover, it is not capable to deal with the phase delay caused by the analog filters. Notice the fact that phase delays are different from one to other frequency components, only a fixed phase compensation can be added in the digital time domain based repetitive controller. Fortunately, frequency domain based repetitive control scheme is a good solution to this problem. It uses Fourier series approximation method to reconstruct signals in which frequency components can be chosen easily. Furthermore, phase compensation for each frequency component can be added directly. Hence, frequency domain based repetitive controller improves the steady state tracking error of output voltage further. Learning gain could be different from one frequency component to other in FDRC. One has the freedom to choose frequency component and give learning gain's weight based on error spectrum. In contrast in TDRC, only one learning gain is used for the whole range of frequency components.

To further validate the effectiveness of the two proposed schemes, experimental tests were performed on a DSP-based digital control DC-AC inverter setup. This experimental setup is described in the thesis. The performance of TDRC and FDRC schemes are compared to the performance of deadbeat controller. The experimental tests show that both proposed TDRC and FDRC schemes are effective in suppressing the voltage distortions, which is in agreement with the results obtained in the simulation studies. Further reduction in harmonic distortions is possible by using the FDRC compensation compared with the results obtained

from TDRC scheme. From the experimental studies, it is evident that the proposed TDRC and FDRC schemes effectively reduce THD by 40 % and 80 % under a nonlinear load respectively. Furthermore, it is demonstrated that both schemes achieve low THD to an acceptable level in a reasonably short time. However, the FDRC scheme performs better than TDRC scheme.

5.2 Future Work

1. In design of repetitive controller, learning gain and gain weights have a direct impact on system performance. Therefore, choice of gains are carefully selected in our studies. In TDRC control scheme, an evaluation of the learning gain effect is given by theoretical analysis as well as the consistent simulation results. However, choice of gains in FDRC controller scheme could be studied further.

2. We assume that every two integer multiple of fundamental frequency components are orthogonal in design of frequency domain based repetitive controller. However, simulation and experiment results in Fig. 4.4, Fig. 4.12, Fig. 4.18 and Fig. 4.26 illustrate that learning the chosen frequency components has some influence on other frequency components. The reason might be existing of sub-harmonics. A controller which is able to eliminate the inter-harmonics can be studied to further reduce the output voltage distortions.

3. During the learning process of FDRC, for all frequency components, the magnitude and phase information are "collected" by Fourier analysis once every

fundamental frequency period. Therefore, for high frequency components in learning process, take 5th harmonic component example, parameters of Fourier approximation for 5th harmonic component updates every 5 cycles. Obviously it delays the convergence speed. Additionally, it may deteriorate the learning process. A solution is proposed in [65] for repetitive control of robots. Certain modification of the learning updating algorithm can be done to improve the learning dynamics.

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List of Publications

Conference Papers

1. Wang Wei, Sanjib Kumar Panda, Jian-Xin Xu, "Control of High performance DC-AC Inverters Using Iterative Learning Control", *IEEE International Region 10 Conference (TENCON)*, Chiang Mai, Thailand, 2004.

2. Wang Wei, Sanjib Kumar Panda, Jian-Xin Xu, "Control of High Performance DC-AC Inverters Using Frequency Domain Based Repetitive Control", *the Sixth IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Kuala Lumpur, Malaysia, 2005.

Submitted Journal Papers

1. Wang Wei, Sanjib Kumar Panda, Jian-Xin Xu, "Control of High Performance DC-AC Inverters Using Time Domain Based Repetitive Control", *submitted for review to IEEE Trans. on Power Electronics.*

2. Wang Wei, Jian-Xin Xu, Sanjib Kumar Panda, "Control of High Performance DC-AC Inverters Using Frequency Domain Based Repetitive Control", *sub-*

mitted for review to IEEE Trans. on Power Electronics.

Appendix A

Architecture of DS1104

Fig. A.1 shows the architecture of the DS1104 controller board. The DS1104's consists of a PowerPC 603e microprocessor (master PPC) and a slave Texas Instruments TMS320F240 DSP subsystem.

The master PPC running at 250MHz (CPU clock) containing data and instruction cache of 16KB each. It has an interrupt controller, a synchronous DRAM controller, several timers, a PCI interface. The master PPC controls the fully programmable ADC unit, DAC unit, 20-bit I/O unit, incremental encoder interface, serial interface. The PCI interface provides an access from/to the host PC via 33 MHz-PCI interface. The interface serves the board setup, program downloads and runtime data transfers from/to the host PC. The host interface also provides a bidirectional interrupt line. Via this line, the host PC can send interrupt requests to the master PPC and vice versa.

The DS1104's slave DSP subsystem consists of Texas Instruments TMS320F240

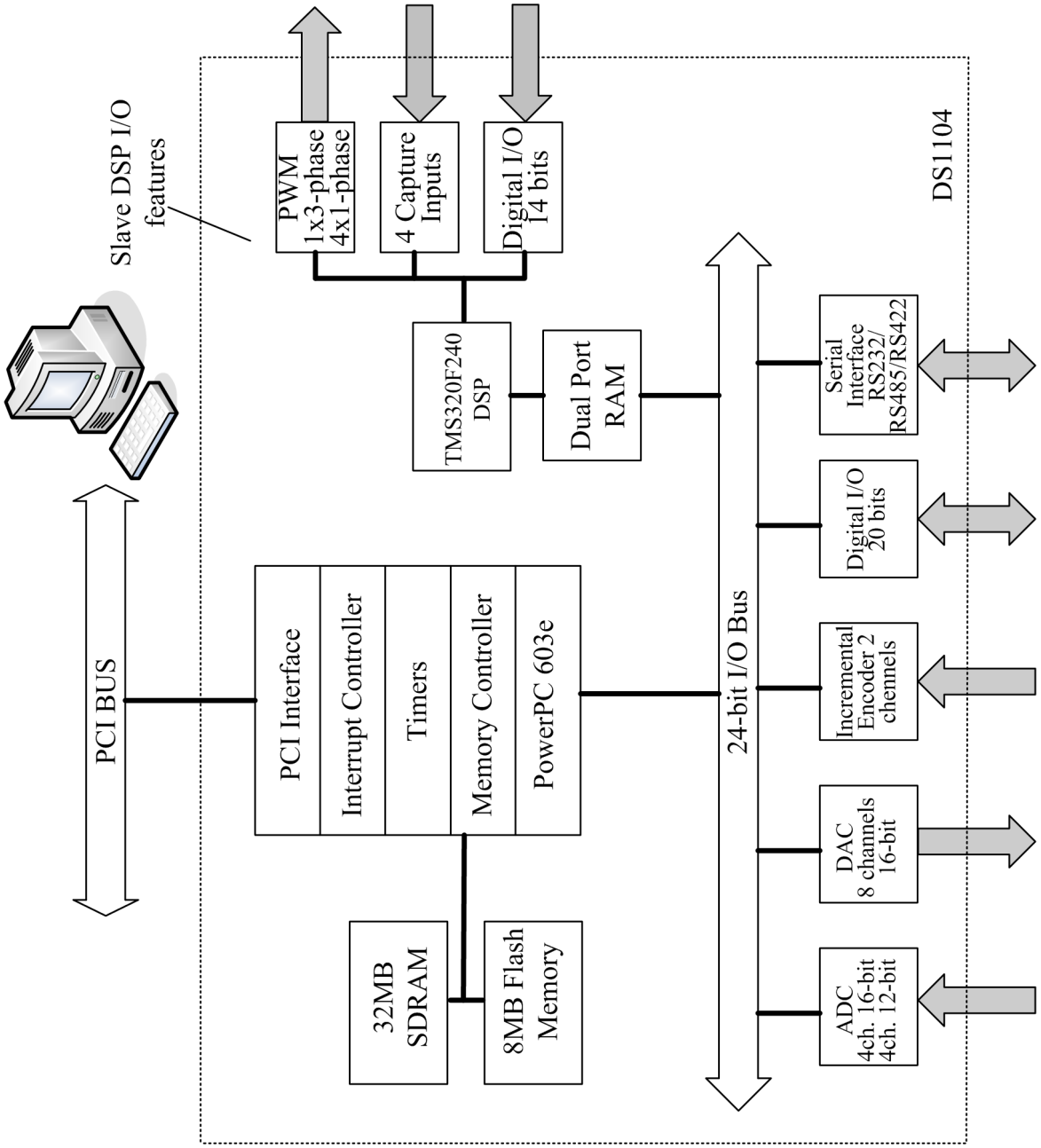

Figure A.1: Architecture of DSP DS1104 controller board

DSP Running at 20 MHz. The slave DSP on the DS1104 provides 14-bit direction selectable digital I/O unit. The slave DSP on the DS1104 provides a timing I/O unit that can be used to generate and measure pulse width modulated (PWM) and square-wave signals. It also controls a serial peripheral interface (SPI), which can

be used to perform high-speed synchronous communication with devices connected to the DS1104, such as an A/D converter.

The DS1104 R&D Controller Board upgrades PC to a development system for rapid control prototyping. It enables online control parameters tuning and reduces the prototyping time significantly. The real-time hardware based on the PowerPC 603e microprocessor and its I/O interfaces make the board ideally suited for developing controllers in various fields. Detailed description of the DS1104 board are given in dSPACE User's Guide.

Appendix B

Inverter and Driver

1. **Specifications**

   - **Input**: 0-120V DC
   - **Output**: single-phase, 0-100V (peak value)
   - **Power**: up to 1 kW

2. **Description**

   - **IGBT module–MUBW 10-12A7 (IXYS)**

     The IGBT module comprises a 3-phase uncontrolled rectifier, six IGBT switches, one IGBT for braking and a built-in NTC thermistor for temperature sensing.

   - **DC-link capacitors & transformer board**

     Fig. B.1 shows the schematic diagram of IXYS module. The DC-link capacitor is connected across pins 22-23. An NTC thermistor is connected in between pins 21-22 to limit the in-rush current.

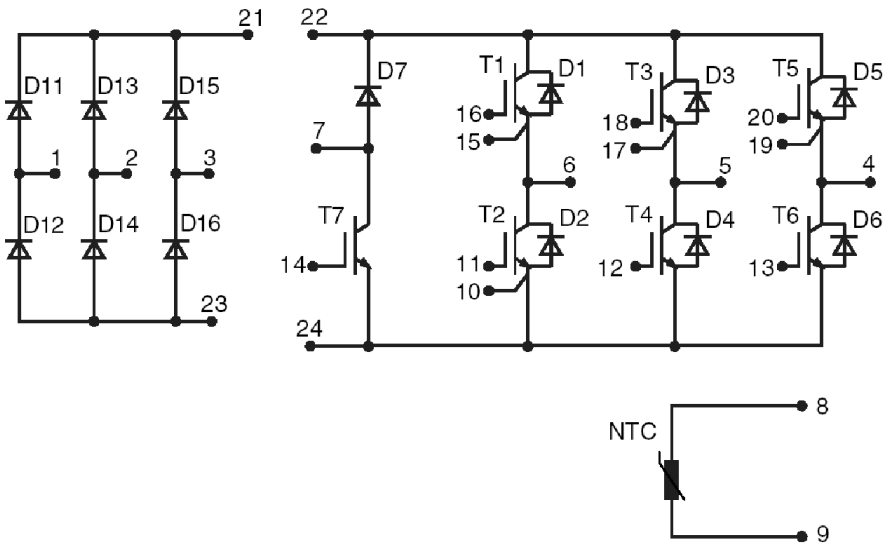

Figure B.1: Schematic diagram of MUBW 10-12A7.

- **SEMIDRIVER SKHI 24 hybrid dual IGBT driver**

SEMIDRIVER SKHI 24 hybrid dual IGBT driver module block diagram is shown in Fig. B.2. The driver module is hybrid component which may directly mounted to the PCB. Devices for driving, voltage supply, error monitoring and potential separation are integrated in the driver. The forward voltage of the IGBT is detected by an integrated short-circuit protection, which will turn off the module when a certain threshold is exceeded. In case of short-circuit or too low supply voltage the integrated error memory is set and an error signal is generated. The driver is connected to a controlled +15V supply voltage. The input signal level is 0/5V. Additionally a digitally adjustable interlocking time is generated by the driver, which has to be longer than the turn-ff delay

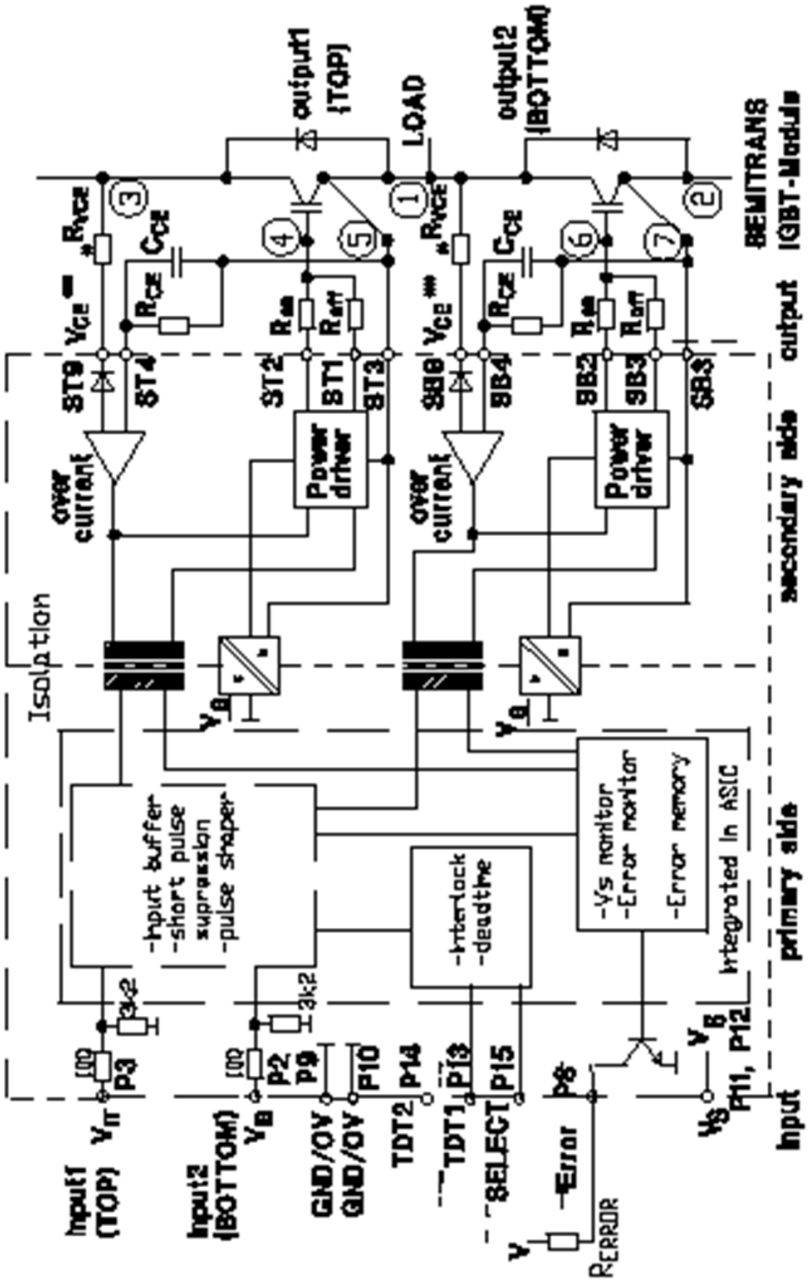

Figure B.2: Block Diagram of SKHI 24 Driver Module

time of the IGBT. The connections in between the driver board and the IGBT module are made by wires of twisted pairs. The driver board is connected with the Control-PWM Card via a shield flat-ribbon cable.

Appendix C

Analog Signal Card

A schematic diagram of the main part of a analog filter on the Analog Signal Card is shown in Fig. C.1.

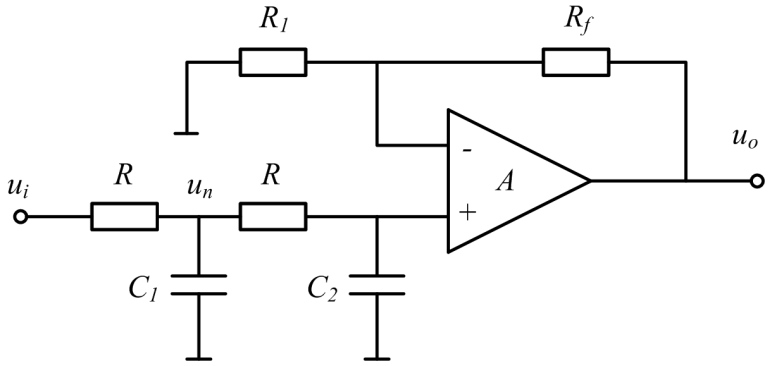

Figure C.1: Schematic diagram of a analog filter

Transfer function is given as

$$A_u(s) = \frac{U_o(s)}{U_i(s)} = \frac{A_{up}}{1 + (RC_1 + RC_2 + RC_2)s + (R^2C_1C_2)s^2} \tag{C.1}$$

where $A_{up} = 1 + \frac{R_f}{R_1}$. Cutoff frequency of the filter is decided by the following

$$f_c = \frac{1}{2\pi\sqrt{C_1C_2R^2}} \tag{C.2}$$

In the research work of this thesis, $R_f << R_1$, $C_1 = 0.047\mu F$, $C_2 = 0.022\mu F$; for the inner current loop filter $R = 4.7k\Omega$, and for the outer voltage loop filter $R = 9.5k\Omega$. The cut-off frequency of these two filters are $1kHz$ and $500Hz$ respectively.