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Si/SiC bonded wafer: A route to carbon free SiO_2 on SiC

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This paper describes the thermal oxidation of Si/SiC heterojunction structures, produced using a layer-transfer process, as an alternative solution to fabricating SiC metal-oxide-semiconductor (MOS) devices with lower interface state densities (D_{it}). Physical characterization demonstrate that the transferred Si layer is relatively smooth, uniform, and essentially monocrystalline. The Si on SiC has been totally or partially thermally oxidized at 900–1150 °C. D_{it} for both partially and completely oxidized silicon layers on SiC were significantly lower than D_{it} values for MOS capacitors fabricated via conventional thermal oxidation of SiC. The quality of the SiO_2, formed by oxidation of a wafer-bonded silicon layer reported here has the potential to realize a number of innovative heterojunction concepts and devices, including the fabrication of high quality and reliable SiO_2 gate oxides. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3099018]

Silicon carbide (SiC) has been extensively studied for application in power electronic devices. Its physical and thermal properties including superior blocking characteristics, high intrinsic temperature, and good thermal conductivity have intimated that SiC will eventually replace silicon in the next generation of high-voltage applications. In addition, its relatively mature growth and processing technology and its native thermal oxide (SiO_2),[1] give SiC a significant advantage over alternative wide band-gap semiconductors such as GaN and diamond. Despite this period of intensive research, SiC Schottky-barrier unipolar devices remain the only device commercially available today.[2] The absence of a commercially available electronic switch, in particular, a successful metal-oxide-semiconductor field-effect transistor (MOSFET), is one of the main factors preventing widespread uptake of SiC technology. The key issue relating to the performance of MOS devices is the quality and reliability of the gate dielectric, especially a low Si/SiO_2 interface state density.[3] Unfortunately, SiC MOSFETs fabricated using thermally grown gate oxides exhibit low inversion layer mobilities—attributed to high SiO_2/SiC interface state densities which act as scattering or trapping sites, reducing channel mobilities.[4–6] Though SiO_2 is the native oxide of SiC and can be thermally grown on the SiC surface, the presence of carbon and its efficient removal during the oxidative consumption of SiC, is believed to have a detrimental influence the SiO_2/SiC interface and its bulk insulator properties.[6] In this letter, we present a novel solution—the use of Si/SiC heterojunction structures—toward the realization of overcoming the poor reliability (and high interface trap density) of SiC thermal oxides. This alternative approach to direct thermal oxidation of SiC, relies on the thermal oxidation of a silicon layer, wafer bonded to a SiC substrate. Oxidation of this layer has the potential to produce SiO_2 of Si complementary MOS (CMOS) quality which is considered as the *model* insulator in semiconductor technology.[7] Another application of the direct wafer bonding technique is the monolithic integration of silicon and SiC devices onto the same chip. The key issue surrounding Si/SiC heterostructures is the implementation of a thick monocrystalline Si layer on top of SiC. We have previously reported investigations using several techniques to grow Si on SiC including the following: chemical vapor deposition (CVD), molecular beam epitaxy (MBE), and electron beam evaporation under UHV conditions (EBE-UHV).[6,8,9] However, the large lattice mismatch between Si and SiC prevented each of the aforementioned techniques from achieving a Si layer with sufficient quality for a MOS gated device. In 2008,[10] we reported the successful layer transfer (LT) of a thin silicon layer, suitable for MOS device fabrication, onto a 3 in. SiC wafer. LT was achieved using a novel wafer bonding (WB) process, based on the SMARTCUT® technique, to form Si/SiC heterojunction structures.

Layer transfer was performed by room temperature hydrophilic wafer bonding[11,12] of a 0.008° orientation, *n*-type (doping concentration of 3.0×10^{16} cm^3), 4*H*-SiC (Si-face) 75 mm diameter Cree, Inc. substrate wafer to a 150 mm diameter hydrogen-implanted *p*-type (doped 2×10^{17} cm^{-3}) silicon wafer. The root mean square (rms) surface roughness of the SiC wafer before bonding, measured using an atomic force microscope was 0.6 nm. Extensive wafer bonding trials revealed that the low 0.6 nm rms value of on-axis wafers was crucial to achieving a successful bond.[12] In contrast, only limited bonding could be achieved using 4° off-axis wafers with a rms roughness of 1.5 nm—attributed to the inherently higher surface roughness values of the off-axis wafers.[10] The bonding surfaces of wafers were activated using oxygen and nitrogen plasma treatments. Layer transfer was subsequently achieved by annealing the bonded wafers at 300 °C to cleave the silicon wafer along the hydrogen-implant plane, leaving a 400 nm layer of *p*-type silicon bonded to SiC. To form a high strength, covalent bond between the thin silicon layer and the SiC substrate, and the LT wafer was annealed at 1000 °C. After the complete heterojunction formation by

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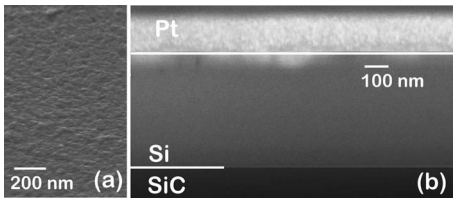

FIG. 1. SEM characterization (a) surface and (b) cross section of the (400 nm) Si/SiC heterojunction structure.

direct wafer bonding on on-axis SiC, the Si surface was relatively smooth [Fig. 1(a)] with a rms roughness of 5.8 nm. A focused ion beam has been used to investigate the silicon layer structural composition and the Si/SiC interface. Cross-sectional scanning electron microscopy (SEM) images of the bonded wafer show an abrupt interface between Si and SiC, with no evidence of any large extended defects in the Si layer [Fig. 1(b)]. An assessment of the monocrystalline nature of the Si on SiC has been carried out by x-ray diffraction (XRD). Figure 2 shows a comparison of the layer-transferred Si/SiC layer to a MBE grown of Si on SiC. As mentioned above, CVD, MBE, or EBE-UHV of Si on to SiC results in polycrystalline or amorphous Si layers. The large lattice mismatch induces Stranski–Krastanow growth or polycrystalline island formation during the growth process,[8] which is a major impediment when considering the oxidation of the Si layer due to a poor aspect ratio. In contrast XRD scans of the wafer-bonded Si layer reveal only a single cubic silicon phase, *c*-Si ⟨400⟩, which corresponds to the same crystalline phase as that in the donor Si wafer. Prior to the successful formation of a Si/SiC heterojunction was created by the wafer bonding process, the Si wafer suffered a series of stressing steps.[10] Moreover, taking into account the surface bow and roughening of the SiC wafer, the different lattice constants and the different coefficients of thermal expansion of Si versus SiC, it is not so obvious that the crystalline structure of the transferred Si layer would remain intact. XRD experiments shown in Fig. 2, have revealed no sign of texturation of the Si layer. Also evident in Fig. 2 are the peaks from the *n*-type monocrystalline 4*H*-SiC substrates. The survival of a high quality crystalline layer after the WB process is of paramount importance not only for a good, stoichometric SiO_2 formation, but also for a number of applications one can envisage. In particular, the monolithical integration of Si CMOS logic and/or Si-based optoelectronics, cantilevers, or

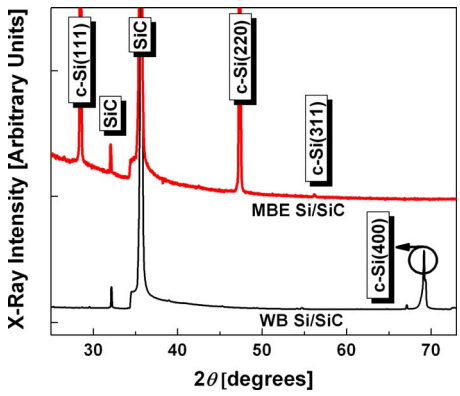

FIG. 2. (Color online) XRD θ-2θ scan revealing the monocrystalline nature of wafer-bonded Si/SiC structure, compared to polycrystalline Si on SiC grown by MBE.

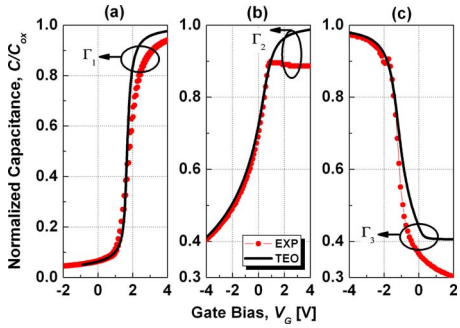

FIG. 3. (Color online) High frequency (100 kHz) *C-V* characteristics for (a) SiO_2/SiC thermally grown (TH-SiO_2/SiC), (b) SiO_2/SiC from oxidation of the transferred layer by wafer bonding (WB-SiO_2/SiC), and (c) SiO_2/Si/SiC from the partially oxidized Si layer (WB-SiO_2/Si/SiC).

sensors together with SiC power devices on the same Si/SiC wafer. The technology associated with the Si part of the circuit would remain unchanged.

The Si/SiC heterostructures were partially and totally oxidized to obtain SiO_2/Si/SiC (WB-SiO_2/Si/SiC) and SiO_2/SiC (WB-SiO_2/SiC) interfaces, respectively. Partial thermal dry oxidation of Si/SiC samples were performed at 1050 °C in a tube furnace with an oxygen flow of 1 L/min for 1 h and 45 min to obtain an oxide around 70 nm thick. Complete dry oxidation of the silicon layer was performed at an initial temperature of 1150 °C for 11 h followed by further oxidation for 32 h at 1050 °C. The intention of the oxidation was to only consume the silicon layer and to avoid oxidation of the SiC substrate. The oxidation time and lower oxidation temperature of 1050 °C were thus used to avoid significant penetration of the oxide into the SiC substrate, since SiC is oxidized only very slowly at this temperature. A SiO_2 layer around 800 nm thick was obtained. To enable capacitance-voltage (*C-V*) measurements to be taken, this oxide was etched to 100 nm using a $3HF:2HNO_3$:60 deionized water solution.

Figure 3 shows a comparison between the typical experimental and theoretical[13] *C-V* characteristics, after a high frequency (100 kHz) measurement. A thermally grown SiO_2/SiC reference sample (TH-SiO_2/SiC) has been included for comparison [Fig. 3(a)]. This sample was oxidized under dry conditions at 1150 °C for 3 h to obtain an oxide layer of 40 nm in thickness. A significant density of interface traps (D_{it}) results in a stretch-out and subsequent deviation from the ideal MOS *C-V* characteristics. On *n*-type MOS capacitors, the near-conduction band edge traps produce a distortion of the *C-V* characteristics near the flatband voltage for the capacitor biased in both, accumulation or depletion [Γ_1, Fig. 3(a)]. This deviation is much less noticeable for SiO_2 thermally grown on Si/SiC [Fig. 3(b)]. There, it is difficult to obtain a good accumulation signal from this interface [Γ_2, Fig. 3(b)], which is attributed to a lattice mismatch between the insulator and the semiconductor surface.[14] Figure 3(c) presents the *C-V* characteristics for a partially oxidized Si/SiC. This SiO_2/Si/SiC structure exhibits a modified *C-V* characteristic in the strong inversion region [Γ_3, Fig. 3(c)] which is explained in terms of an additional capacitance from the SiC surface. From the *C-V* characteristics the D_{it} has been extracted using the high frequency Terman method,[13] as shown in Fig. 4. A reduced D_{it} of 4.8×10^{11} cm^{-2} eV^{-1} has been extracted at $E_c - E_T = 0.25$ eV for

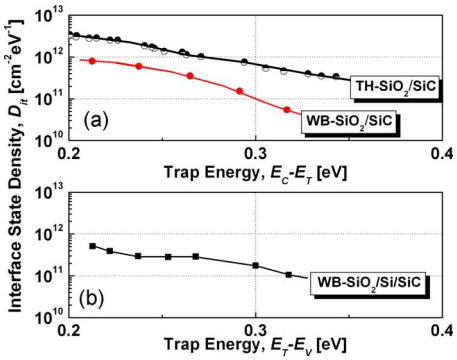

FIG. 4. (Color online) Density of interface traps D_{it} (a) close to the SiC conduction band (TH-SiO_2/SiC and WB-SiO_2/SiC) and (b) close to the Si valence band (WB-SiO_2/Si/SiC) for the partially oxidized Si/SiC sample.

the SiC/WB-SiO_2 sample, compared to 1×10^{12} cm^{-2} eV^{-1} extracted at $E_c-E_T=0.25$ eV for the TH-SiO_2/SiC sample.

It was suggested[4] that the strong increase of D_{it} close to the 4*H*-SiC conduction band is attributed to defects extended into the oxide near the SiO_2/SiC interface, otherwise known as near interface traps (NITs). Using spectroscopy techniques, NIT peaks can be distinguished in the distribution of acceptor states near the conduction band edge. It has been observed that the extracted trap distribution seems to be independent of SiC polytype, orientation, substrate, and—to some extent—even of the oxidation conditions. Quantum mechanical atomistic computer simulations[15] suggested that neither σ- nor π-type bonds between sp^2-hybridized carbon atoms at the interface, nor dangling bonds may cause NIT or the continuous increase toward the conduction band edge. In addition, small disordered graphite clusters at the interface simply cannot explain the D_{it} profile. Si interstitial intrinsic oxide defects can introduce further defects into the upper half of the band gap. However, NIT can only be explained by $C_i=C_i$ carbon dimers substituting two nearby oxygen atoms and then being incorporated into the SiO_2 during the thermal oxidation process of SiC. A reduced D_{it} has been found on WB-SiO_2/SiC when compared to thermal oxidation. This result appears to be consistent with the concept of a reduced number of carbon dimers present at the SiO_2 on SiC. However, an interfacial suboxide (SiO_x) is inevitable at the Si/SiC interface due to the nature of the LT method utilized in this work. Therefore, it can be inferred that this thin SiO_2 layer will almost certainly contribute to some increase in the density of interface states. It should also be mentioned that a number NITs, having a similar energy position have been detected on the SiO_2/Si MOS interface,[4] shielded by states over the conduction band edge of Si in this case. These Si/SiO_2 NIT states that are obviously not related to carbon could also play a role in the density of interface traps observed in the SiO_2/SiC system. To further reduce the density of interface states, it is possible to incorporate much of the knowledge previously acquired after a decade of research regarding the SiO_2/SiC interface. In particular, post WB-SiO_2/SiC formation NO and NO_2 anneals and/or oxidation,[16] SiC implantation prior to Si bonding[17] or ozone annealings.[18] In addition, the wafer bonding of SiO_2 and SiC seems to be another perfectly plausible approach for achieving a high quality insulator on SiC.

The D_{it} profile close the valence band for the partially oxidized samples is also presented in Fig. 4(b). An interface state density of 2.7×10^{11} cm^{-2} eV^{-1} has been extracted at $E_c-E_T=0.25$ eV. This value is rather high when compared to state-of-the-art for Si/SiO_2 interfaces ($\sim10^{10}$ cm^{-2} eV^{-1}).[13] This may be attributed to the fact that no additional action was taken to passivate dangling bonds or interfacial imperfections. Such treatments could yield significant reductions in D_{it} values.

In conclusion, we have demonstrated that Si/SiC direct wafer bonding is a simple route for achieving a relatively smooth, high quality, stoichiometric, and completely carbon free SiO_2 layer on SiC. The interfacial properties of the SiO_2/SiC structures, fabricated using oxidation of Si/SiC heretostructures, are already significantly better than those from conventional thermal oxides grown on SiC. It is reasonable to suggest that improving the bonding methodology would result in a SiC/SiO_2 MOS interface even closer to the ideal Si/SiO_2 interface.

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