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Low temperature mobility in hafnium-oxide gated germanium *p*-channel metal-oxide-semiconductor field-effect transistors

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Effective mobility measurements have been made at 4.2 K on high performance high-*k* gated germanium *p*-type metal-oxide-semiconductor field effect transistors with a range of Ge/gate dielectric interface state densities. The mobility is successfully modelled by assuming surface roughness and interface charge scattering at the SiO₂ interlayer/Ge interface. The deduced interface charge density is approximately equal to the values obtained from the threshold voltage and subthreshold slope measurements on each device. A hydrogen anneal reduces both the interface state density and the surface root mean square roughness by 20%. © 2007 American Institute of Physics. [DOI: 10.1063/1.2828134]

Germanium is a promising channel material for future complimentary metal oxide semiconductor (MOS) primarily due to its lower effective carrier masses compared to those of silicon, which gives it higher electron and hole mobilities. Also, Ge-*p*MOS devices have been reported which have mobilities well in excess of those given by the silicon universal mobility curve.^{1,2} Germanium lacks a stable natural oxide and therefore prior to the deposition of the gate dielectric, the Ge surface must first be passivated. Many combinations of dielectric and surface passivation have been attempted and the result is often a multilayered gate insulator consisting of the passivating gate oxide at the channel interface and high-*k* dielectric on top of this.¹⁻⁴

The performance of a metal-oxide-semiconductor field-effect transistor MOSFET is highly dependent on fixed charges at the interface and interface roughness which, in addition to phonons, scatter carriers. Often, the mobility in the inversion layer and therefore the device performance is limited by the quality of the interface as much as the properties of the channel material.

Ge-*p*MOS devices were fabricated in a Si-compatible process flow on 200 mm in diameter (100) silicon wafers with thick Ge layers on the surface grown by chemical vapor deposition. The high-*k* dielectric is hafnium oxide with a subnanometer Si layer as a surface passivation which is partially oxidized before high-*k* deposition and results in an overall equivalent oxide thickness of 18 Å. A process listing and detailed room temperature characteristics have been reported elsewhere¹ and of particular note are the high peak mobility of 358 cm² V⁻¹ s⁻¹ and the variability of devices across a given wafer due to interface state density. Devices in this study were selected to have a high density of interface states, ($D_{it} > 2 \times 10^{12}$ eV⁻¹ cm⁻²) and hence do not perform

as well as those devices previously reported.¹ The interface states have been reported¹ to have the effect of reducing the peak transconductance and inducing a large negative threshold voltage shift ΔV_t from the value obtained for a more ideal device ($D_{it} \sim 10^{11}$ eV⁻¹ cm⁻²). A hydrogen anneal performed on some devices has been reported to improve uniformity and increase mobility.¹

Drain current-gate voltage measurements have been performed at room temperature on many devices with a drain bias of $V_d = -50$ mV and the threshold voltage (V_t), subthreshold slope, and peak field effect mobility μ_{FE} (determined from the peak transconductance⁵) extracted. It is assumed here that $Q_{inv}(V_g) = C_{ox}(V_g - V_t)$ is a valid approximation for the inversion charge as a function of gate voltage $Q_{inv}(V_g)$.

It is suggested that donorlike interface states are responsible for threshold voltage shifts by acting as a source of oxide charge as the device turns on and these charges increase Coulomb scattering of carriers in the channel, thus reducing the mobility μ . These two separate effects arising from the same charges near the channel should be related by $\Delta V_t \propto \Delta D_{it}$ and $\mu^{-1} = \mu_C^{-1} + \mu_{ph}^{-1} + \mu_{SR}^{-1} \propto \mu_C^{-1} \propto D_{it}$. The second expression simply relates the total mobility μ to those limited by Coulomb scattering μ_C , phonon scattering μ_{ph} , and surface roughness scattering μ_{SR} using Mathiessen's rule. μ_C is inversely proportional to the number of charged scattering sites. Hence, where Coulomb scattering is present, the value of μ^{-1} should contain a term proportional to threshold voltage shift. This predicted relationship between the threshold voltage and mobility is clearly demonstrated in Fig. 1 for many devices. Note the improvement in both mobility and uniformity due to the post metallization annealing (hydrogen ambient at 400 °C). The annealed devices have higher mobilities than the unannealed devices for the same D_{it} , which suggests that another contributing scattering mechanism is reduced. As the phonon scattering is a property that is not altered by a hydrogen annealing, it is most likely that a re-

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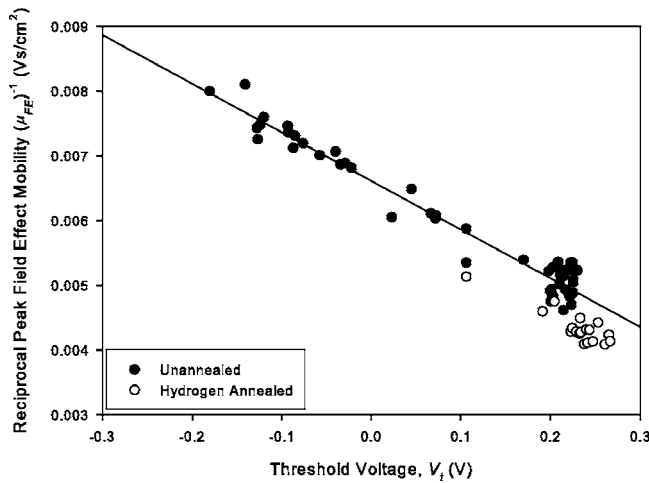


FIG. 1. Decreasing peak field effect mobility with negative threshold voltage shift due to interface states.

duction in the surface roughness is the cause of the improved mobility.

The average value of D_{it} present in the band gap between the midgap and near the valence band edge was extracted for the devices, by comparing threshold voltages⁵ with that of a device with low D_{it} . A value of D_{it} present at a specific energy in the band gap has also been extracted for each device from the subthreshold slope.⁵ As shown in Fig. 2, the two deduced values of D_{it} agree over the distribution of devices with the average value consistently slightly higher. Charge pumping measurements were performed on a limited number of devices and gave a range in D_{it} values of 10^{12} – 5×10^{13} $\text{eV}^{-1} \text{cm}^{-2}$, which is consistent with the values extracted above.

Three devices from the non-hydrogen annealed group (labeled as D) and two devices from the hydrogen annealed group (labeled as H) were selected for further investigation and assigned a D_{it} value accordingly (Table I). They are cooled in an environmental probe station to 4.2 K where phonon scattering is eliminated.⁶ Inversion charge carrier sheet density n_s and depletion charge sheet density N_D are calculated from split C-V measurements performed at 10 KHz using a HP 4284A precision LCR meter. Device

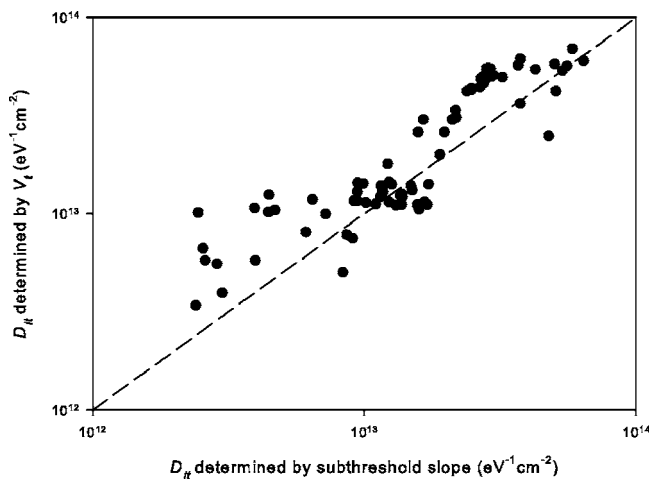


FIG. 2. Comparison of D_{it} extracted from two different techniques, one using the subthreshold slope and the other using the threshold voltage of a given MOSFET.

TABLE I. Extracted interface state density D_{it} , fitting parameters of interface charge density n_i , and rms surface roughness Δ for each MOSFET.

MOSFET	$D_{it} \times 10^{13}$ ($\text{eV}^{-1} \text{cm}^{-2}$) (± 0.5)	$n_i \times 10^{13}$ (cm^{-2}) (± 0.5)	Δ (nm) (± 0.03)
D1	3.1	2.6	0.62
D2	3.8	3.5	0.58
D3	5.8	5.5	0.65
H1	2.6	1.5	0.48
H2	0.6	0.7	0.48

transfer characteristics are measured at $V_d = -50$ mV, and corrections are then made for series resistance and a diffusion current⁷ contribution in order to obtain the effective mobility as a function of E_{eff} [Figs. 3(a) and 3(b)].⁸

The effective mobility at high vertical fields varies as E_{eff}^{-1} , which is closely similar to the behavior seen in Si-*p* (MOSFETs), and which is associated with scattering from the roughness at the SiO_2/Si interface. We will therefore use the following model to analyze the present data.

The interface charge limited mobility μ_C and the interface roughness limited mobility μ_{SR} may be expressed as functions of n_s in the forms^{9–11}

$$\mu_C = \frac{e\hbar n_s}{\pi m^* E_F n_i} \left\{ \frac{F(2K_F)[1 - G(2K_F)] + (2K_F/q_s)}{F_i(2K_F)} \right\}^2, \quad (1)$$

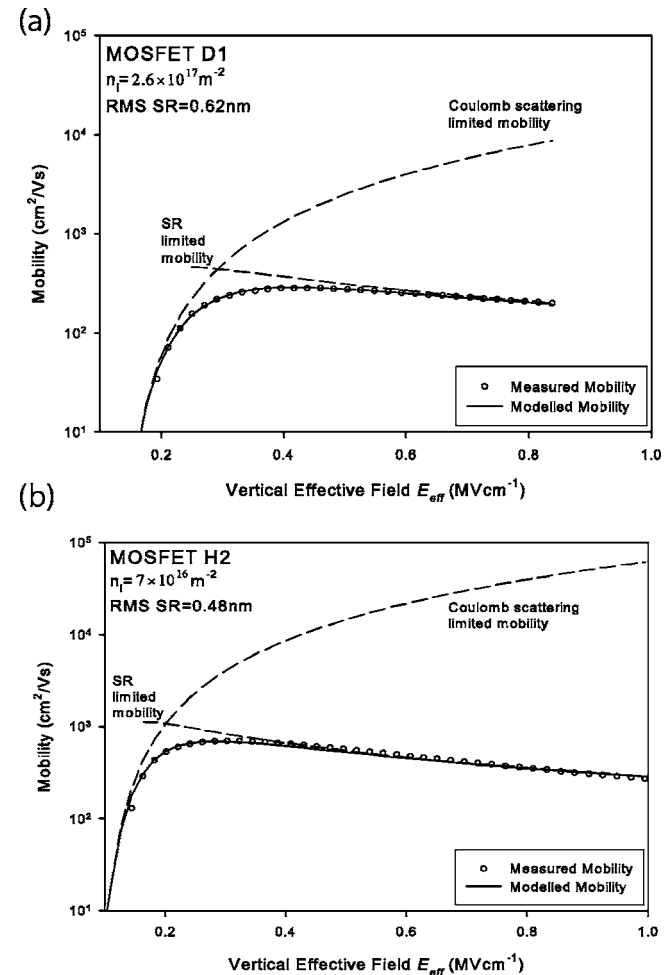


FIG. 3. Measured mobility and fit obtained by summing the surface roughness limited mobility and Coulomb scattering limited mobility using Mathiessen's rule for MOSFETs D1 (a) and H2 (b).

$$\mu_{\text{SR}} = 0.48 \frac{e\hbar}{m^* \Lambda^2 \Delta^2 K_F^4 E_F} \left(1 + \frac{2N_D}{n_s}\right)^{-2} \times \left\{ F(2K_F)[1 - G(2K_F)] + \frac{2K_F}{q_s} \right\}^2, \quad (2)$$

where E_F is the Fermi energy with corresponding Fermi-wave vector K_F , $F(2K_F)$ and $F_i(2K_F)$ are form factors;⁹ the local field Hubbard correction $G(2K_F)$ is evaluated as 0.447. The surface roughness correlation length Λ is put equal to the reciprocal of K_F , since this corresponds to the condition of maximum scattering. The best fit for each mobility curve is obtained by combining the two contributions using Mathiessen's rule and adjusting the number of impurities per unit area n_i at the interface and rms surface roughness Δ accordingly. Band nonparabolicity and anisotropy are neglected and a heavy-hole effective mass $m^* = 0.3m_0$ is used. It is assumed that the confinement splits the heavy-hole and light-hole bands, with the heavy hole lying lowest.

Our calculations show that the gas is degenerate and that there is a single subband occupancy, since $E_F - E_0 \gg kT$ and $E_1 - E_0 > E_F - E_0$. $E_F(n_s)$ ranges from 10 to 180 meV and $E_1(n_s)$ from 40 to 200 meV. Note that E_F is the Fermi energy and E_n is the potential energy of the n th subband with $n=0$ as the lowest subband.

Depletion charge sheet density N_D is calculated as a function of gate voltage from the gate-body branch of the split C - V curve for each device. This does not vary significantly between devices and has a maximum value of $1.1 \times 10^{16} \text{ m}^{-2}$ in strong inversion.

The fits of $\mu(E_{\text{eff}})$ obtained for each device agree well with the measured effective mobility over the entire applied effective field. Parameters for each device are given in Table I and of note is that the value of n_i used to obtain the mobility fit is comparable to the extracted value of D_{it} of each device, suggesting that the theoretical calculations of mobility in the channel are valid.

Before postmetallization annealing, the average rms surface roughness deduced is $0.62 \pm 0.03 \text{ nm}$ and after $0.48 \pm 0.03 \text{ nm}$ which is a reduction of $\sim 20\%$, and which has a large effect on the mobility at high values of E_{eff} where the

carriers are confined closely to the interface. Also, interface charge density is reduced by approximately $3 \times 10^{13} \text{ cm}^{-2}$. This supports the hypothesis that both reduced interface charge density and surface roughness are responsible for the improved peak mobilities of hydrogen annealed devices at room temperature in Fig. 1. In the mobility curves at 4.2 K shown in Fig. 3, the peak effective mobility in the hydrogen annealed device H2 is roughly double that in the unannealed device D1 at $694 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

In summary, mobility has been extracted at 4.2 K on Ge- p MOS devices and successfully modeled by making suitable approximations. The mobility increases after a postmetallization hydrogen annealing. We show for the first time that this can be explained as being due to a diminution of both surface roughness of the gate dielectric-germanium interface and the interface state density. Reducing surface roughness scattering has been identified as a critical objective for enabling germanium MOSFETs in the deep sub-100 nm regime.¹²

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