Chopper-Stabilized High-Pass Delta-Sigma Modulators

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Abstract

The Delta-Sigma Modulator (DSM) is widely applied in high-precision analog-to-digital (A/D) conversion, especially for low-frequency applications including sensor interface and biomedical signal acquisitions. In these applications, the DSMs are required to deal with biomedical signals, such as electroretinography, electroencephalogram, electrocardiogram and electromyogram signals; so it is required to have low offset and low flicker noise as the frequency range of these noises overlaps with the signals of interest.

Although offsets can be removed by digital circuits, it is always desirable that the analog front-end circuits can remove the offsets in the first hand. The chopper stabilization technique is popular for reducing offset and flicker noises in amplifiers by shifting the signal to outside the noise frequency range before the processing and converting it back to the baseband after the processing.

In this thesis, a first chopper-stabilized high-pass DSM with experimental results is reported for suppressing offset and low-frequency noises, and an improved version of the chopper-stabilized high-pass DSM is reported with simulation results. For the first DSM, a new circuit technique to suppress the residual offset caused by the chopper switch charge injection is proposed. Enabled by an amplifier sharing architecture, the technique diverts the error charge generated by the critical chopper to the second stage of the modulator such that the error becomes first-order high-pass shaped. Fabricated in a 0.18μm CMOS technology, the 2nd-order DSM realizes 82dB dynamic range over a 1kHz bandwidth while consuming 144μW from a 1.8V supply. The offset is 403μV and the flicker noise is invisible in the measured output spectrum down to 4Hz. The core area of the chip is 0.16mm^2. For the second DSM, it aimed at less chopper pairs to achieve more stable and area saving circuit and at low power consumption for the usage of portable devices. It was also designed in a 0.18μm CMOS technology; this 2nd-order feed-forward DSM realizes 55dB dynamic range over a 256Hz bandwidth, while consuming a very low power of 840nW from a 1.2V supply.

摘要

差和转换器已经广泛应用于高精度模数转换，尤其在低频类应用，包括传感器接口和生物信号的获取．在这些应用中，差和转换器需要处理各种生物类信号输入，比如视网膜电波(直流--交流 50 赫兹)，脑电波(直流--交流 150 赫兹)，心电波(交流 0.01 赫兹--交流 250 赫兹)和肌电波(交流 5 赫兹--交流 500 赫兹)．这类应用需要低直流失调，低闪烁噪声，因为这些噪声的频域与信号频域重叠．

尽管直流失调可以在数字电路中消除，但我们还是希望模拟前端电路可以直接消除直流失调．斩波稳定技术是一种常用的减少直流失调和闪烁噪声的方法，具体实现为在信号处理之前，将信号频域移动到高频频域，从而与噪声频域分离；处理之后，再将信号频域移回到原先的基频频域．

在本篇论文中，讲解了一个斩波稳定高通差和转换器的流片测试结果和一个改进的斩波稳定高通差和转换器的仿真结果．对于第一个差和转换器，本文提供了一个新的减小斩波开关引起的电荷沟道注入的技术．运用共用放大器的结构，这个技术将误差电荷引入第二阶差和转换器电路．芯片采用 0.18 微米晶体管技术，此两阶差和转换器实现 82dB 的动态范围，带宽 1kHz，在 1.8V 电源下功耗为 144 微瓦．直流失调为 403 微瓦并且闪烁噪声完全消除．芯片尺寸为 0.16㎜^{2}．对于第二个差和转换器，目标是减少斩波开关对从而实现更稳定，更小尺寸的芯片，另一个目标是减小功耗从而实现在便携式设备上面的应用．转换器同样采用 0.18 微米晶体管技术，此两阶差和转换器实现 55dB 的动态范围，带宽 256Hz，在 1.2V 电源下功耗为 840n 瓦．

Contents

List of Figures

List of Tables

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Chapter 1 Introduction

1.1 Motivation

There is an increasing trend of sensing biomedical signals using low-power portable devices. The history of biosensors started in 1962 when Leland C.Clack invented enzyme electrodes for glucose concentration measurement. Since then, research communities from various fields have worked together to develop more sophisticated, reliable bio-sensing devices. The use of thermal transducers of biosensors was proposed in 1974 and the new devices were named thermal enzyme probes and enzyme thermistors. Then in 1975, the optical sensor was proposed. [1]

The biosensor is a combination of two parts: a bio-element and a sensor element. Depending on the transducing mechanism used, the biosensors can be categorized to different types, such as resonant biosensors, optical biosensors, thermal biosensors, ion-sensitive Field Effect Transistor (FET) biosensors, electrochemical biosensors and so on. [1]

The bio-interface is a key part in biosensor system; Figure 1.1 shows the basic block diagram of the front-end bio-interface of a portable biomedical sensor system. INA here means instrumentation amplifier. A key block of the system is the analog-to-digital converter (ADC). Typically Delta-Sigma (DS) ADC is employed in biomedical sensor systems for its high resolution and robust performance against circuit non-idealities.

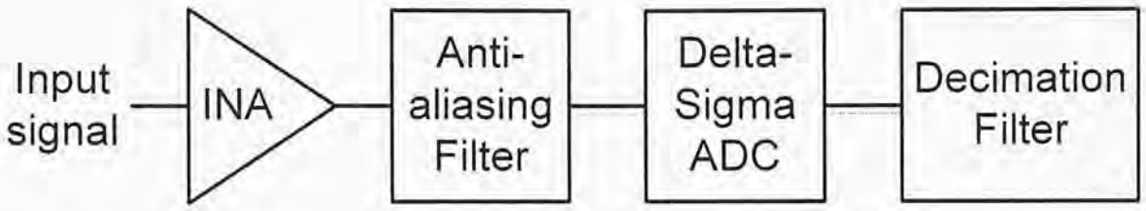


Figure 1.1: Block diagram of bio-interface

The typical medical signal parameter and their frequency ranges are shown in Table 1.1; from this table, we can find that all the medical signals has very low frequency range, and also we know that these signals has very small magnitudes in the scale of micro-volt. Therefore, the input signal should be amplified by instrumentation amplifier before goes through Delta-Sigma Modulator. And through all processes, the low frequency noise including flicker noise and offset should be small enough to make sure that it will not exceed the thermal noise floor.

Parameter	Abbreviation	Frequency Range
Electroretinography	ERG	DC-50Hz
Electroencephalogram	EEG	DC-150Hz
Electrocardiogram	ECG	0.01-250Hz
Electromyogram	EMG	5-500Hz

Table 1.1: The frequency range and magnitude of bio-signals

Figure 1.2 illustrates the state of the art in ADCs in CMOS technologies with the resolution and bandwidth relationships placed [2]. The ranges of the specifications for

the main applications of our project area (the biomedical system) are depicted on this plane in an approximated way. From this figure, the Delta Sigma Modulation based ADCs provide high resolution for low to medium signal bandwidths, perfectly suitable for biomedical signal acquisition.

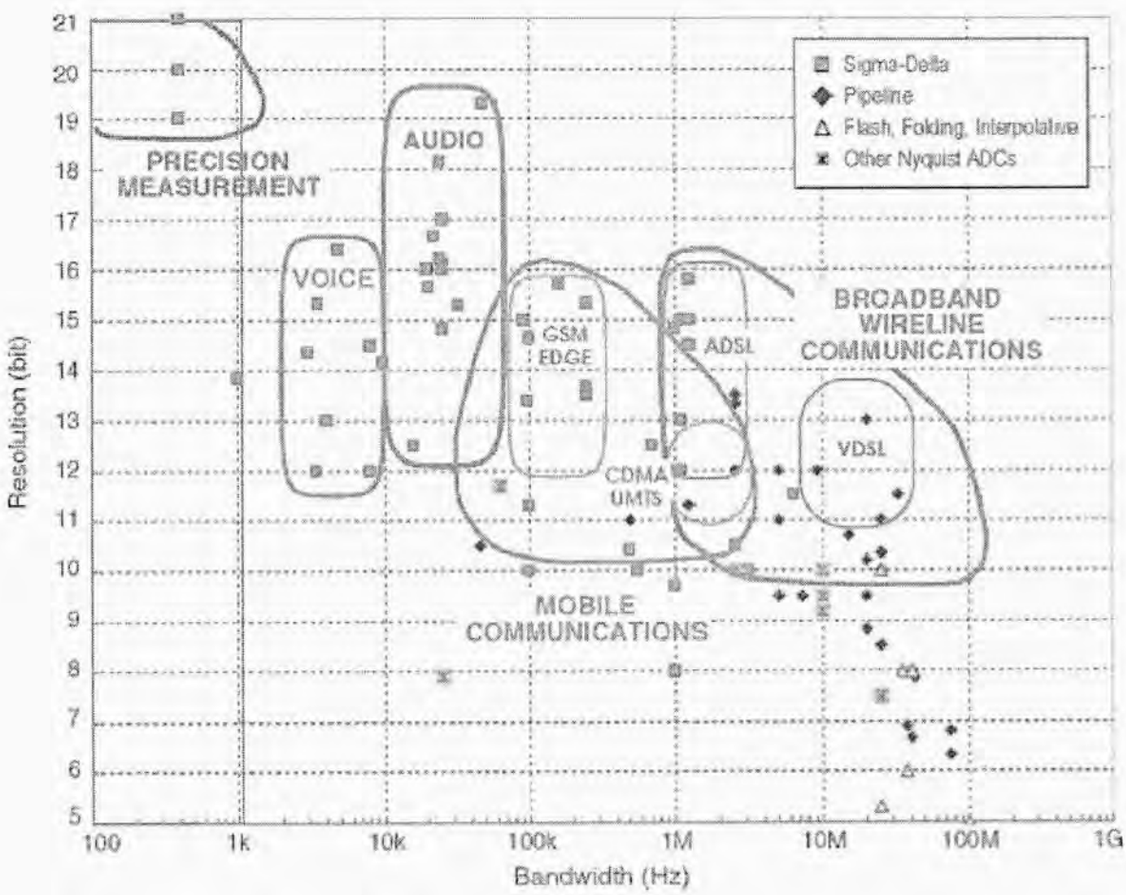


Figure 1.2: The art of ADCs in CMOS technologies for different applications (Reproduced from "CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom" [2])

In these applications, the overall performance of the DSM is influenced by the noise induced from the whole circuit, because high resolution needs large signal to noise ratio, which means the output noise should be reduced as low as possible. Three kinds

of noises may degrade the output performance, which are thermal noise, flicker noise and offset; for the low frequency applications, the flicker noise and offset are the dominant noises. To reduce the effect of these noises, three ways can be used. The first way is to reduce the noise directly by carefully selecting physical parameters, for the thermal noise, which is constant over all frequency bands; it can be reduced directly by enlarging the sampling capacitor. For the flicker noise, it can be degraded by increasing the gate area W*L of the input MOS transistor. For the offset, the switch offset can be reduced by decreasing the gate area W*L of the switch; the operational amplifier offset can be reduced by choosing small $V_{DS,sat}$; the second way is called correlated double sampling technique [3], it samples the noise in one phase and cancel it in next phase. For the sample and hold process, this technique may have some accuracy problem if the changing rate of the noise is large. The third way is using chopper-stabilization technique to separate the large-noise outside the signal band [3]. It modulates the signal to high frequency band before it goes to the circuit with large flicker noise and offset, and then modulates the signal back to baseband, at the same time convert the flicker noise and offset to high frequency band.

For the area saving and simplicity of chopper-stabilization technique, it is widely used in low frequency applications. So in this thesis, we are aimed at further reducing the low frequency noise by using chopper-stabilization technique, the circuit will be more efficiency and have less remaining noises.

1.2 Organization of the Thesis

This thesis is organized as follows. Chapter 2 reviews the fundamental theory of the DSM, including the chopper-stabilization technique for reduction of low-frequency noise. In Chapter 3, the non-idealities in system modeling is introduced, which includes the jitter noise, the finite open-loop gain, finite bandwidth, finite slew-rate, capacitor ratio error, thermal noise and switch charge injection error. Chapter 4 introduces a chopper-stabilized high-pass delta-sigma modulator in 1.8V 0.18μm CMOS, it contains the structure selection, system modeling and parameter selection, circuit implementation, layout implementation and measurement results. Chapter 5 introduces a low-power chopper-stabilized delta-sigma modulator in 1.2V 0.18μm CMOS, it contains the structure selection, system modeling and parameter selection, circuit implementation and simulation results. Chapter 6 gives the basic method to build the decimation filter in Matlab. Finally, Chapter 7 concludes the thesis and gives some suggestions for further research.

Chapter 2 Basic Theorems of Delta Sigma ADC

2.1 Introduction to sampling technique

There are two categories of ADC depending on the rate of sampling, one kind of ADC samples the input at Nyquist rate, which is twice of the bandwidth, the other kind of ADC samples the input at a rate that is much higher that the bandwidth and we call it oversampling.

There are three main reasons for using oversampling:

1. It is easier to avoid the aliasing problem, because it is very difficult to construct an anti-aliasing filter with the sharp cutoff slope without increasing the sampling rate. But if we use oversampling technique, only simple first-order filters are required. Figure 2.1 and Figure 2.2 illustrate the sampled signal with different frequencies.
2. It can achieve higher resolution easily.
3. It can reduce random noise. Let's say, if multiple samples are taken with random noise added to each sample, N samples will reduce the average noise power to 1/N, so using the oversampling technique can reduce the average noise power by 1/OSR, where OSR means oversampling ratio.

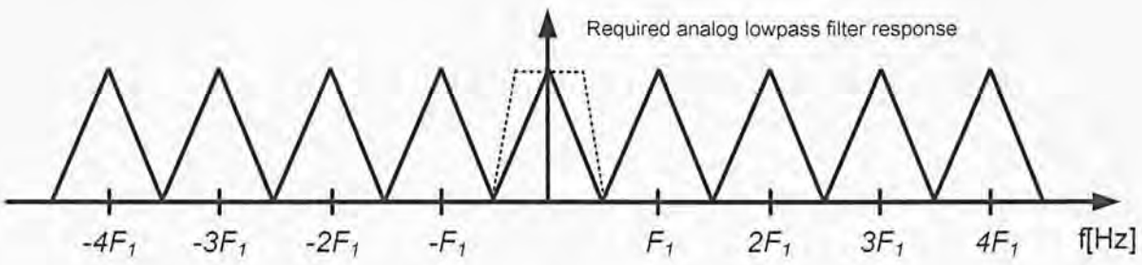


Figure 2.1: Sampled signal with sampling frequency a little bit larger than Nyquist rate

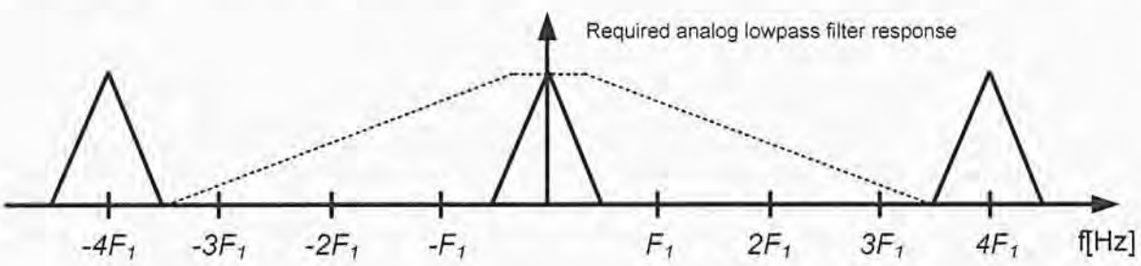


Figure 2.2: Sampled signal with sampling frequency much larger than Nyquist rate

The OSR is defined as the ratio between the sampling frequency (fs) and the Nyquist frequency (2*bandwidth).

$$OSR = \frac{fs}{2*BW} \qquad \text{Eq(2.1)}$$

Aliasing

Aliasing [4] is a serious problem in sampling process; it is an effect that causes different continuous signals to become indistinguishable when sampled, or the distortion that when the signal is sampled and reconstructed as an alias of the original signal. In order to avoid aliasing problem, we should make sure that the sampling frequency is at least twice input frequency.

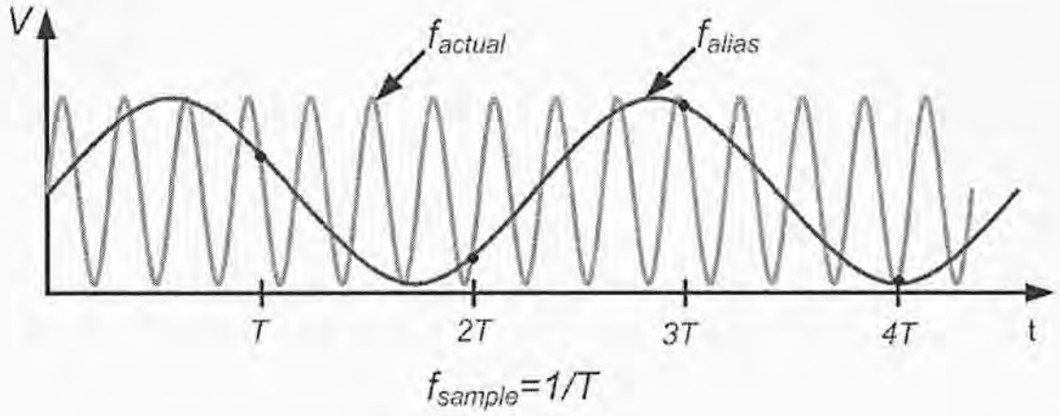


Figure 2.3: Two different sinusoids that fit the same set of samples

2.2 Delta-sigma order & noise-shaping order

2.2.1 First order delta-sigma modulator

The DSM provides the quantization form of a pulse-density signal, the density of the pulses means the average value of the signal. The basic 1st order DSM is shown in Figure 2.4.

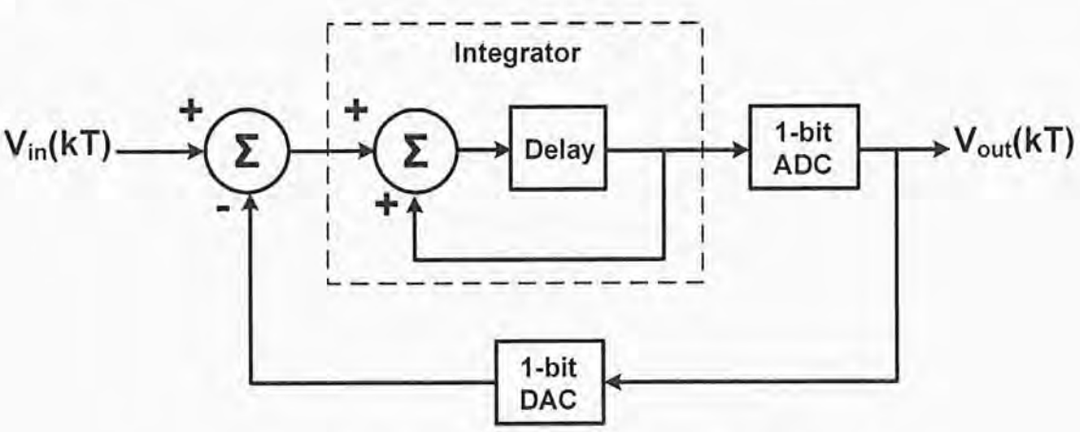


Figure 2.4: Block diagram of a 1st order DSM

The negative feedback system to perform subtraction is the concept of "delta". The difference between the input voltage and the negative feedback output voltage is added

together by an integrator. This process is the concept of sigma. If we represent the transfer function of an ideal integrator as 1/s, the 1-bit quantizer modeled as a simple white error, $Q_e(s)$. We can get the transfer function [5]

$$V_{out}(s) = V_{in}(s)\frac{1}{s+1} + Q_e(s)\frac{s}{s+1} \qquad \text{Eq(2.2)}$$

The frequency domain model is shown in Figure 2.5.

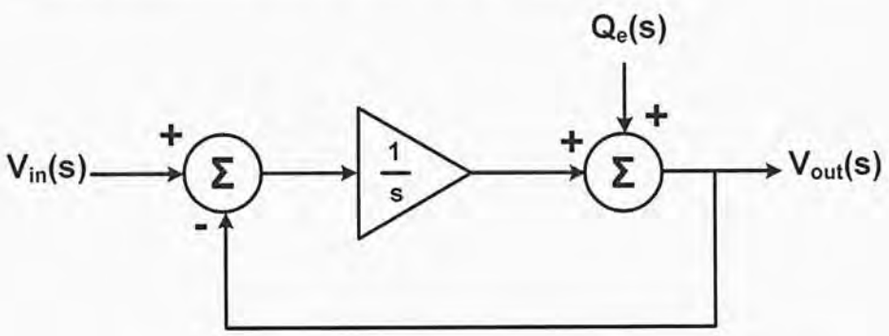


Figure 2.5: Frequency domain model of a 1st order DSM

The digital output comparing to the analog input is shown in Figure 2.6.

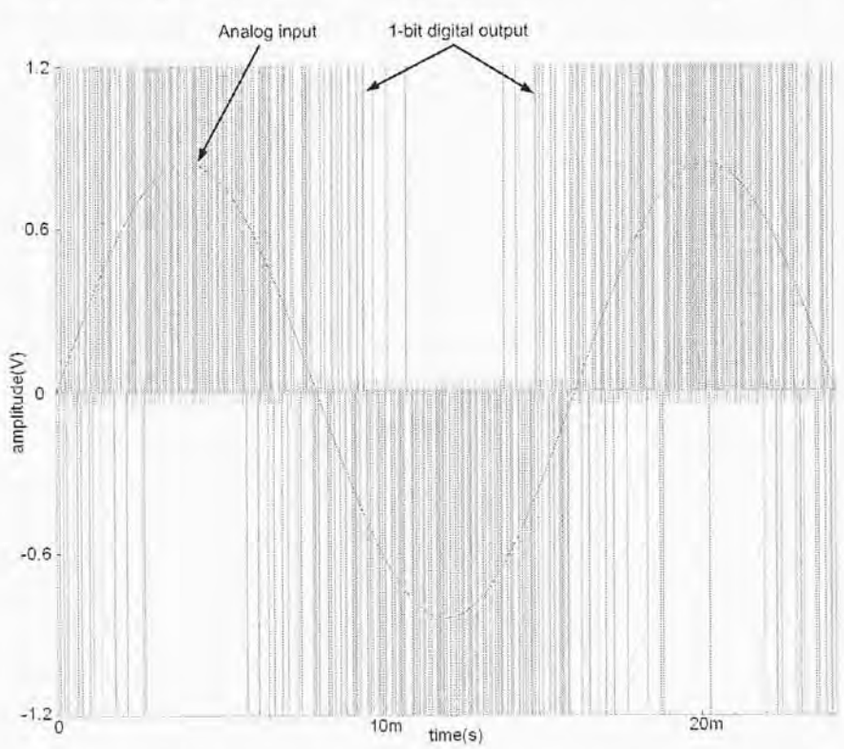


Figure 2.6: The digital output comparing to the analog input

From the characteristic equation, we can see that the transfer function for the input signal is a low-pass filter but the transfer function for the quantization noise is a high-pass filter. So the signal has a higher gain and the noise has very small gain within the bandwidth, and the noise is larger out of the bandwidth. The action that pushes the noise out of the bandwidth is called noise shaping [5].

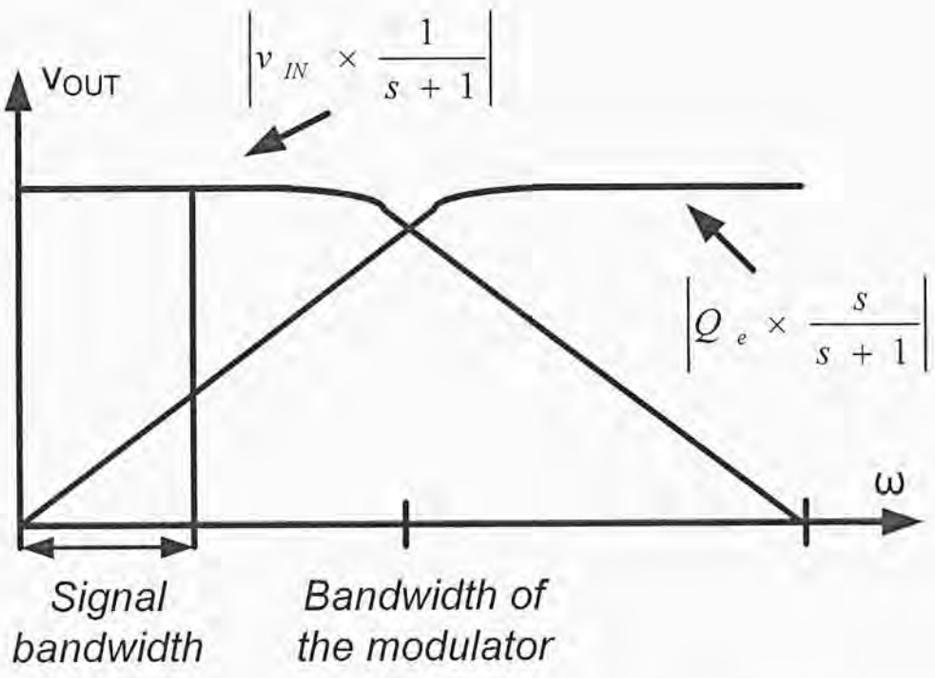


Figure 2.7: Frequency response of the 1st order DSM

The in-band quantization noise power [2] with 1st order noise-shaping is calculated by

$$\sigma_{e,DSM}^2 = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} * \frac{1}{f_s}\left(\frac{2\pi f}{f_s}\right)^2 df = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \qquad \text{Eq(2.3)}$$

where Δ is the least significant bit of the quantizer.

And the peak dynamic range of 1st order lowpass DSM is

$$DR = 10log\left(\frac{P_S}{\sigma_{e,DSM}^2}\right) = 10log\left(\frac{V_p^2}{2} * \frac{36*OSR^3}{\Delta^2\pi^2}\right) = 10log\left(\frac{V_p^2}{2} * \frac{36*OSR^3}{(V_p/2^N)\pi^2}\right)$$

$$= 6.02N + 1.76 - 5.17 + 30log(OSR) \qquad \text{Eq(2.4)}$$

2.2.2 High order delta-sigma modulator

For the high order DSM, the transfer function is

$$V_{out}(s) = V_{in}(s)\left(\frac{1}{s+1}\right)^L + Q_e(s)\left(\frac{s}{s+1}\right)^L \qquad \text{Eq(2.5)}$$

where L is the delta-sigma loop order.

So the in-band quantization noise power with higher order noise-shaping is calculated by

$$\sigma_{e,DSM}^2 = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} * \frac{1}{f_s}\left(\frac{2\pi f}{f_s}\right)^{2L} df = \frac{\Delta^2}{12\pi(2L+1)}\left(\frac{\pi}{OSR}\right)^{2L+1} \qquad \text{Eq(2.6)}$$

And the peak dynamic range of higher order lowpass DSM is

$$DR = 10log\left(\frac{P_S}{\sigma_{e,DSM}^2}\right) = 10log\left(\frac{V_p^2}{2} * \frac{12\pi*(2L+1)*OSR^{2L+1}}{\Delta^2\pi^{2L+1}}\right)$$

$$= 6.02N + 1.76 + 10log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10log(OSR) \qquad \text{Eq(2.7)}$$

The noise shaping graph of first order, second order and third order modulator is shown in Figure 2.8.

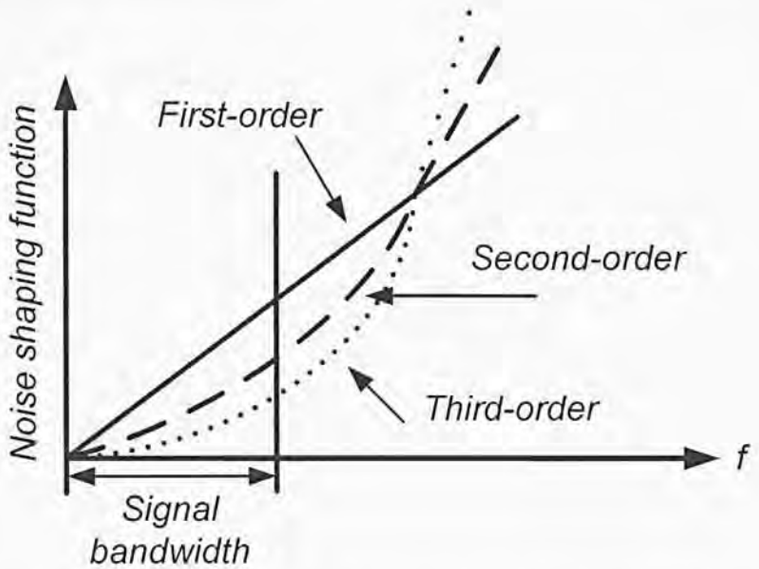


Figure 2.8: Noise shaping comparison of different orders

From Figure 2.8, we can see that as the loop order increases, the noise shaping effect is more obvious. So the dynamic range is higher as the loop order increases with the same OSR. The relationship between dynamic range (DR) and loop order is shown in Figure 2.9, which is based on decibel value of DR in Eq(2.7). [2]

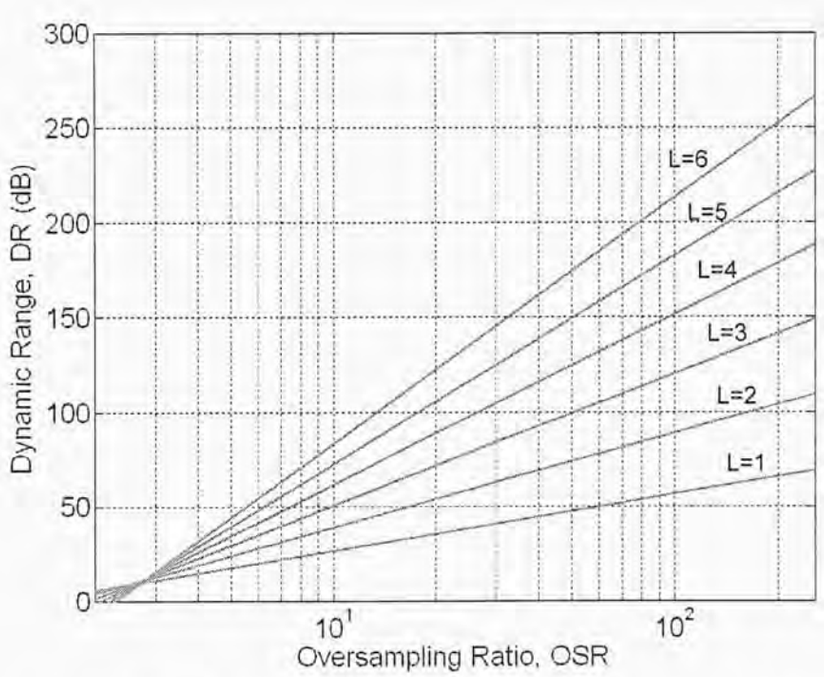


Figure 2.9: The relationship between SNR, OSR and Loop order

The problem is that higher order filtering using single-loop DSM suffers from instability problems and higher power consumption, so there is tradeoff between dynamic range, stability and power consumption.

2.3 Chopper-stabilization technique

There are two kinds of intrinsic noise in MOS transistors, namely thermal noise and flicker noise. The thermal noise is a kind of white noise, which means that it is constant through all frequency range. For the MOS operating in the triode and saturation regions, the thermal noise can be estimated as:

$$S_{v,triode} = 4kTR_{on}\ (V^2/Hz) \qquad \text{Eq(2.8)}$$

$$S_{v,saturation} = \frac{8}{3}\frac{kT}{g_m}(V^2/Hz) \qquad \text{Eq(2.9)}$$

where k is the Boltzmann constant, T is the absolute temperature, and Ron is the turned-on resistance of the MOS transistor [6].

The flicker noise is related to the life time of the carrier and is inversely proportional to frequency.

$$S_{v,1/f} = \frac{K}{WLC_{oxf}}\ (V^2/Hz) \qquad \text{Eq(2.10)}$$

where K is the fabrication parameter, W is the width of the MOS transistor, L is the length of the MOS transistor, C_{ox} is the gate capacitance per unit area, and f is the operational frequency [6].

Normally, the flicker noise dominates in the frequency band when the frequency is smaller than the corner frequency f_c, and the thermal noise dominates in the frequency band when the frequency is larger than the corner frequency f_c. Figure 2.10 illustrates the previous relationships between two kinds of noises.

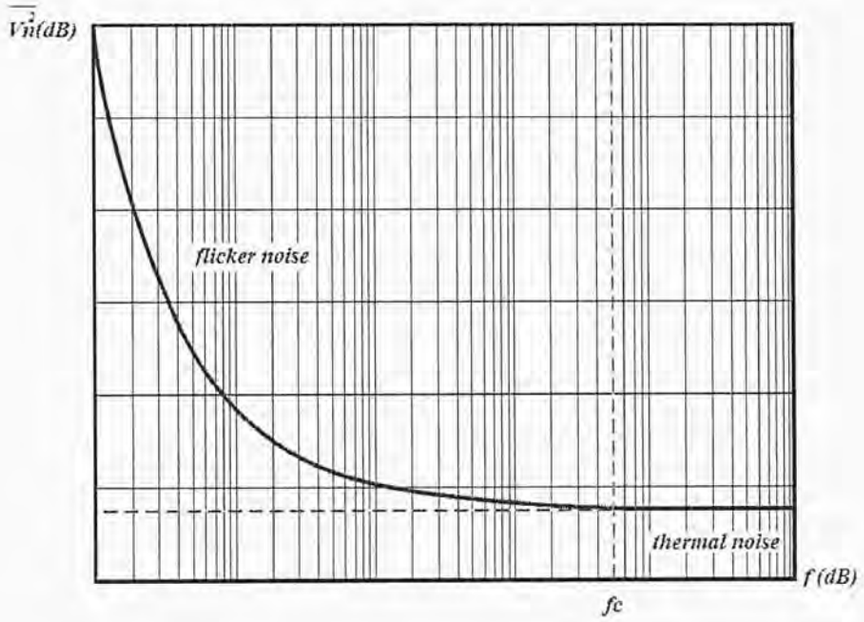


Figure 2.10: The noise model with different frequency

So when the frequency is small, we need to eliminate the flicker noise in the frequency band. The basic idea of chopper technique [3] is to separate the signal frequency band and noise frequency band. Firstly, the input signal is modulated to a higher frequency through one chopper, and then the modulated signal goes through the circuit with offset and 1/f noise; for the offset and 1/f noise is at low frequency band and the modulated signal is at high frequency band, they will not influence each other; finally, one chopper is used to modulate the input signal back to the baseband, the chopper processes are illustrated in Figure 2.11 and Figure 2.12.

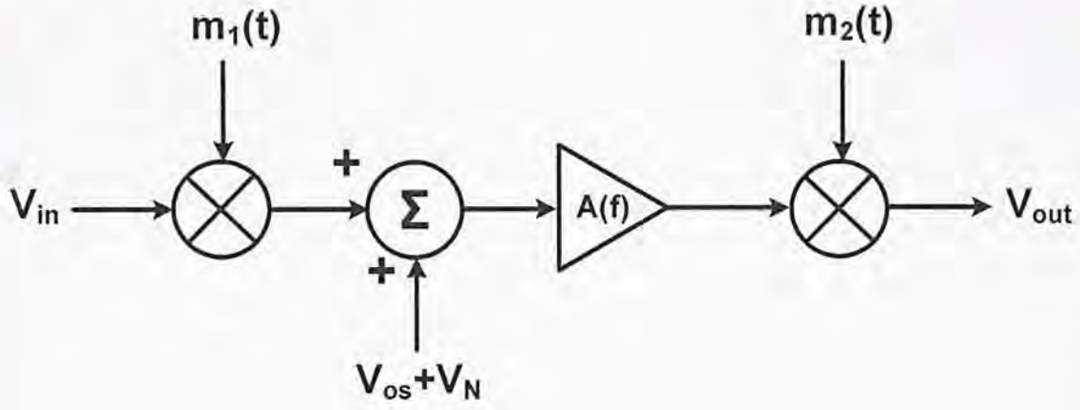


Figure 2.11: The chopper amplification block diagram

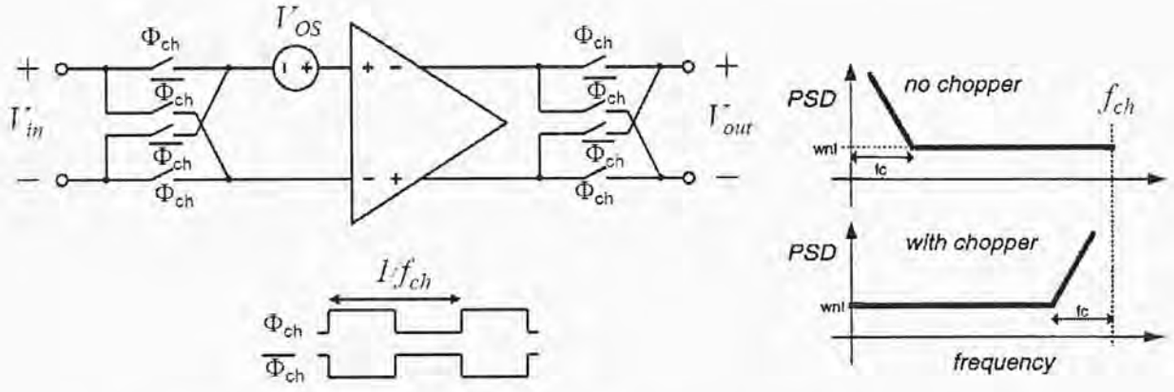


Figure 2.12: The power spectra density illustration of chopper effect

But this technique has charge injection problem. As illustrated in Figure 2.13, when the input chopper switch changes its state, it will induce charge injection errors; these spikes originate from the charge injection mismatch of the switches. And the residual offset voltage can be calculated as: [3][6][7]

$$Vos \cong \frac{2\tau}{T} V_{spike} \qquad \text{Eq(2.11)}$$

where τ is time constant of switch, T is the period of chopper clock, V_{spike} is the average voltage magnitude of the spikes. So normally we can reduce the charge

injection errors by lowering the chopping frequency, lowering the input impedance and reducing the spike energy.

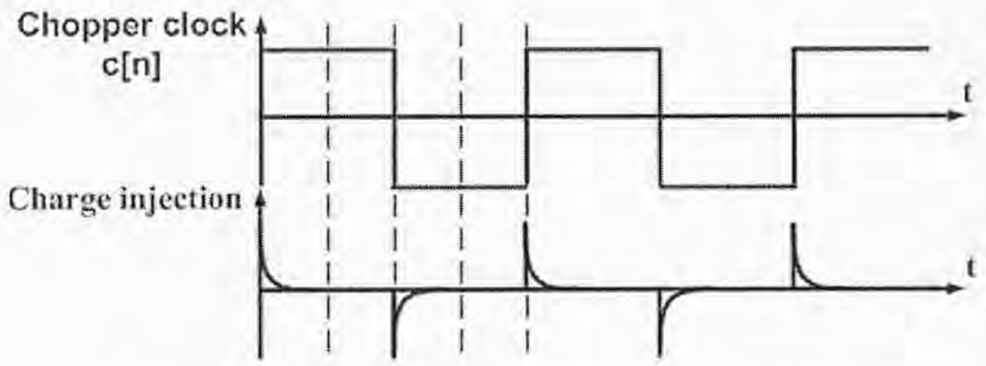


Figure 2.13: The chopper switch charge injection error

2.4 Mirrored integrator

Figure 2.14 shows a chopper-stabilized integrator. The two choppers enclose only the amplifier to suppress its flicker noise and offset. These choppers are transparent to the rest of the circuit and this integrator can readily be used as a part of the loop filter in a low-pass DSM. When the positions of the choppers change to the places shown in Figure 2.15, where the signals stored in the feedback capacitors C_{h1}'s are also modulated by the choppers, the signal transfer function (STF) of the circuit becomes:

$$\frac{V_{out}}{V_{in}}(z) = \frac{C_1}{C_{h1}} \frac{z^{-1}}{1+z^{-1}} \qquad \text{Eq(2.12)}$$

The positive sign in the denominator of Eq(2.12) is a result of the modulation of the feedback capacitor. This circuit is called mirrored integrator [8][9] and its STF has infinite gain at $f_s/2$ and a gain of $C_1/2C_{h1}$ at DC. It can be used as the loop filter for a

high-pass DSM to generate infinite loop gain (ideally) at $f_s/2$. In other words, when the integrator is chopper-stabilized, it becomes a resonator.

In Figure 2.15, the amplifier's flicker noise and offset flow to the output through the same path as the input does. However, as the input of the high-pass DSM lies around $f_s/2$ and the flicker noise and offset are around DC, the latter does not corrupt the former. The choppers here merely change the transfer function. To accept baseband inputs, another chopper can be added in front of the input sampling network to modulator the baseband signal to $f_s/2$ before being processed by the DSM.

The mirrored-integrator-based high-pass DSM are more immune to capacitor mismatches than the resonator-based one. The design presented in this paper is based on the former structure.

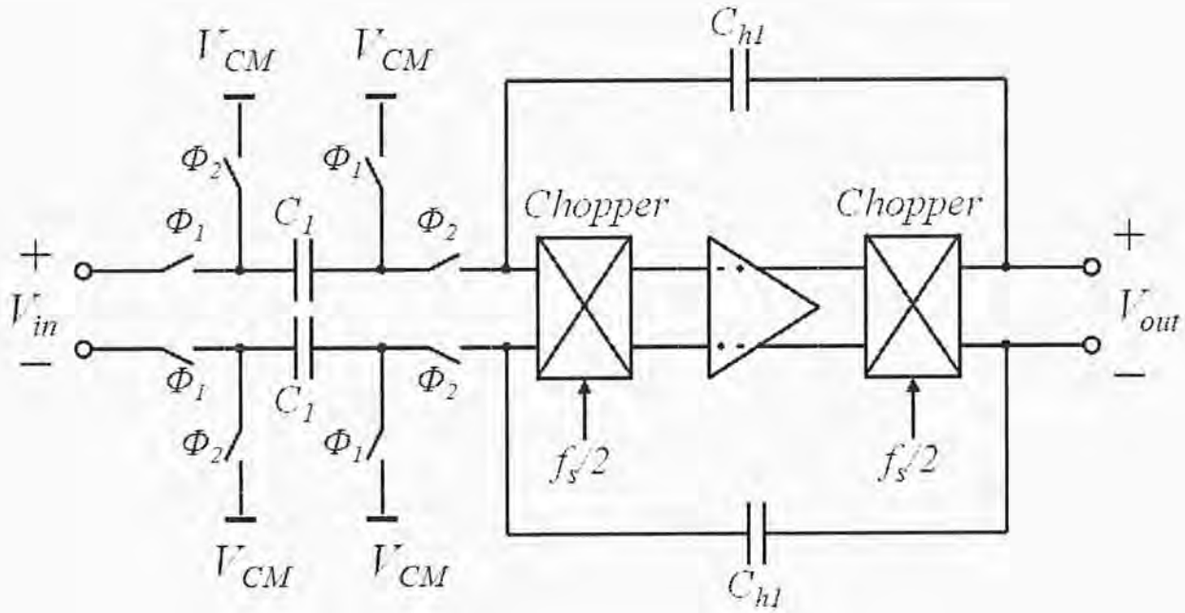


Figure 2.14: The chopper-stabilized integrator.

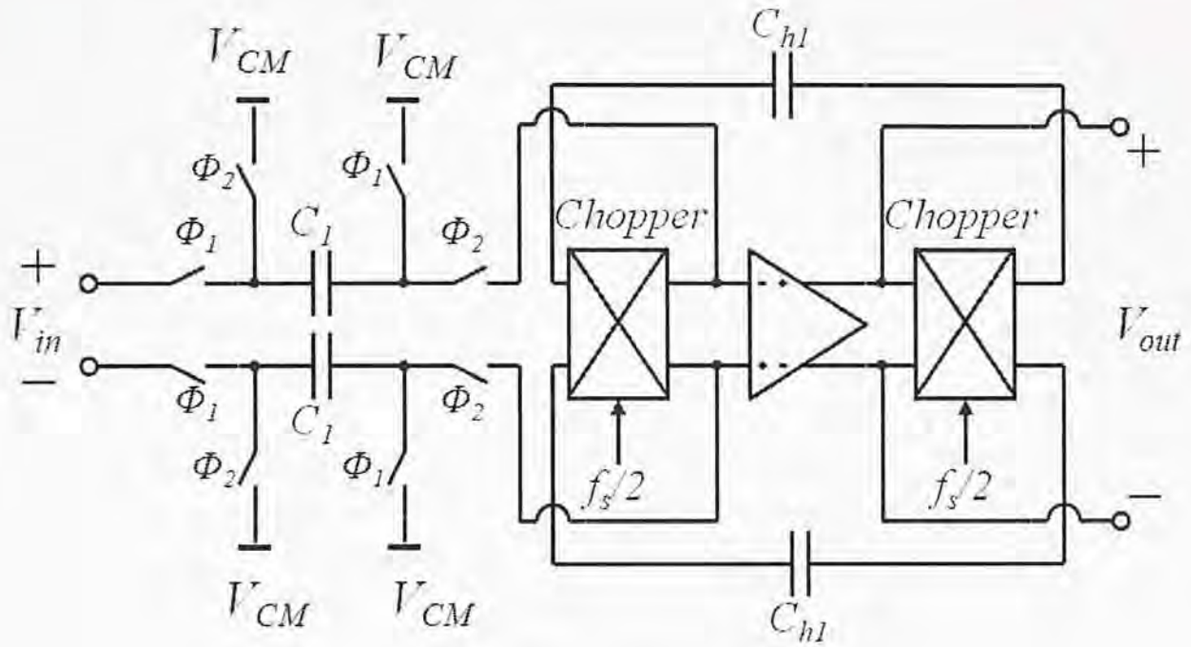


Figure 2.15: The mirrored integrator

2.5 Performance metrics

It is convenient to introduce the most important specifications commonly used to characterize the performance of oversampling delta sigma converters. [2]

2.5.1 Signal to noise ratio (SNR)

Signal to noise ratios of ADCs represents the value of the largest root-mean-square (RMS) output signal into the converter over the RMS value of the noise. It commonly accounts for the linear performance of the converter, and is usually given in decibels.

$$SNR|_{dB} = 10log\left(\frac{A_y^2}{2P_Q}\right) \qquad \text{Eq(2.13)}$$

where A_y is the amplitude of the output, P_Q is in-band power of quantization error.

2.5.2 Signal to noise and distortion ratio (SNDR)

It is the ratio of the output power at the input frequency to the total in-band error power, it also takes the possible harmonics at the converter output into consideration [2].

2.5.3 Dynamic range

It is the ratio of the largest output signal over the smallest output signal. Also it defined as the ratio of the output power at the input frequency with full-scale amplitude to the output power with SNR=0 [2]. If we only consider the quantization error, then the dynamic range will be

$$DR|_{dB} = 20log(2^B - 1) + 1.76 + 10log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10log(OSR) \quad \text{Eq(2.14)}$$

where B is the number of bits, L is the loop order, OSR is the oversampling ratio.

2.5.4 Effective Number of Bits

The effective number of bits (ENOB) is a measure based on the SNDR of an ADC with a full scale sinusoidal input signal. The ENOB can be calculated by:

$$\text{ENOB} = (\text{SNDR}_{\text{dB}} - 1.76) / 6.02 \quad \text{Eq(2.15)}$$

2.5.5 Overload lever, X_{OL}

As in Figure 2.16, for large amplitudes close to full scale value $X_{FS}/2$, overloading occurs, causing an increase of the in-band noise and a sharp drop in the SNR. The

maximum value of the SNR before that drop is SNR peak and the corresponding input signal level is the overload level X_{OL} of this DSM.

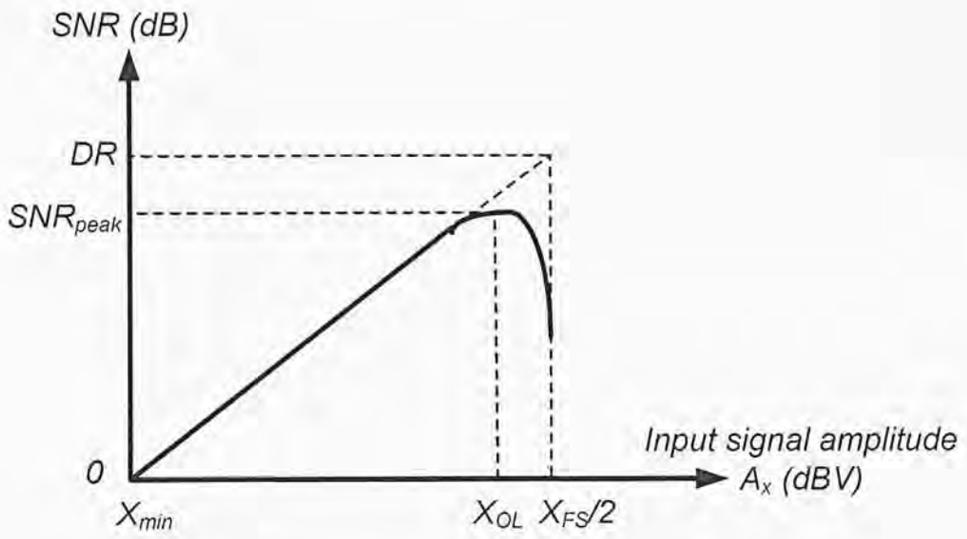


Figure 2.16: SNR versus input voltage

2.6 Conclusion

In this section, we have introduced some basic principles which are related to the final projects in this thesis. The sections 2.1, 2.2 and 2.5 are the principles to decide the details of DSM, such as oversampling ratio, loop order, quantization bits and so on; the sections 2.3 and 2.4 are the principles to decide the structure of the DSM and the techniques to reduce some non-ideal effects.

Chapter 3 Non-Idealities in System Modeling

This chapter presents a study on the main non-ideal mechanisms that affect the performance of DSMs, and the system modeling of these non-ideal effects.

3.1 Clock jitter

The effect of clock jitter in DSM is independent of the structure or order of the modulator. The operation of a switched capacitor circuit depends on complete charge transfers during each of the clock phases, so the effect of clock jitter on it can be calculated in a fairly simple manner. Figure 3.1 shows the effect of clock jitter in the sinusoidal signal.

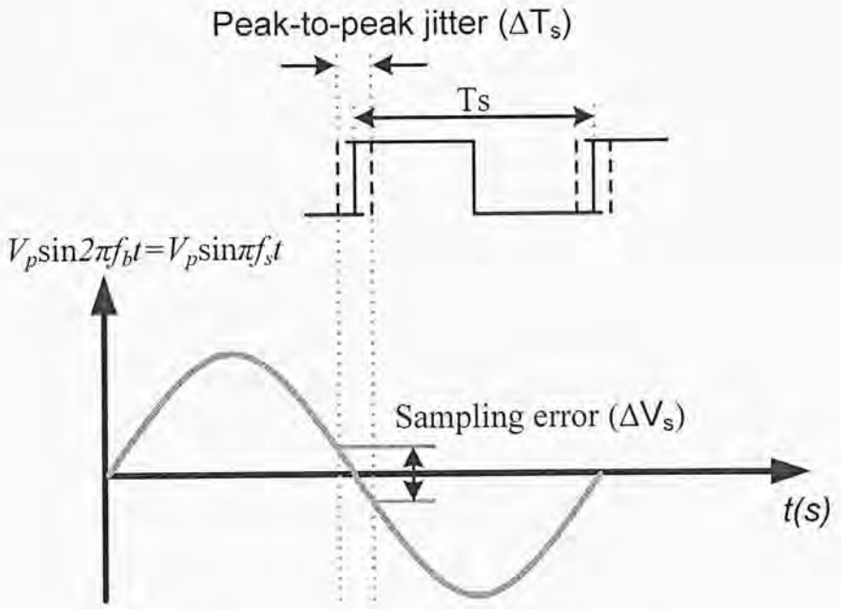


Figure 3.1: The effect of clock jitter in the sinusoidal signal

The sampling clock jitter increases the total error power in the quantizer output

during the non-uniform sampling. The error introduced when a sinusoidal signal with amplitude V_p and frequency f_{in} is sampled at an instant and the amount of ΔT_s is given by:

$$x(t + \Delta T_s) - x(t) \approx 2\pi f_{in} \Delta T_s V_p cos(2\pi f_{in} t) = \Delta T_s \frac{d}{dt} x(t) = \Delta V_s \qquad \text{Eq(3.1)}$$

If ΔV_s is required to be at most 0.5 LSB = $(V_{REF+} - V_{REF-})/2^{N+1}$ and we know V_p = $(V_{REF+} - V_{REF-})/2$, then the maximum allowable peak-to-peak clock jitter should be

$$\Delta T_s \leq \frac{1}{2^N} \times \frac{1}{\pi f_s} \qquad \text{Eq(3.2)}$$

In Figure 3.2, the model which is used to implement Eq(3.1) is presented and this effect can be simulated with Simulink. The sampling uncertainty ΔT_s is assumed a Gaussian random process with standard deviation $\Delta\tau$.

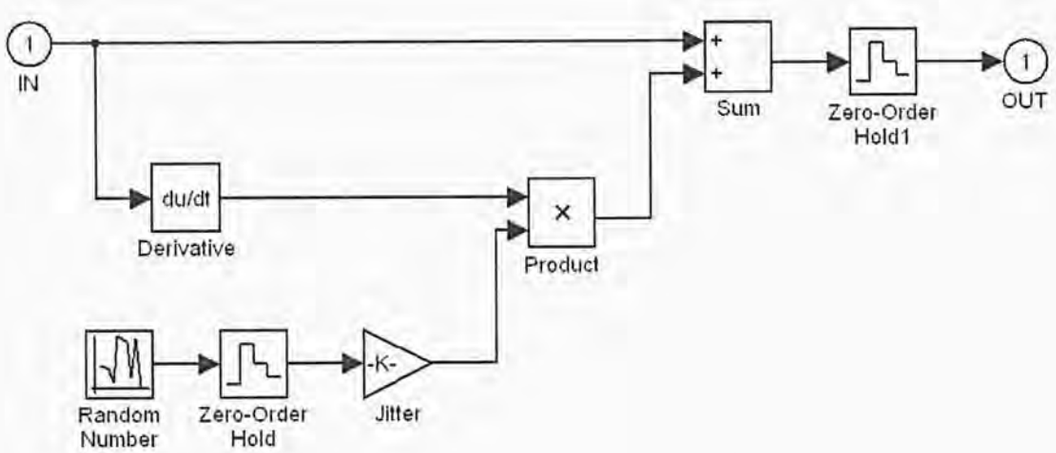


Figure 3.2: Simulink model of clock jitter

3.2 Non-ideal effect of operational amplifier

3.2.1 Finite open-loop gain

The integrator non-idealities for op-amp based design are generally finite DC gain, bandwidth and slew rate. In this section, we will focus on the first issue. The schematic of a single-ended switched-capacitor integrator is shown in Figure 3.3.

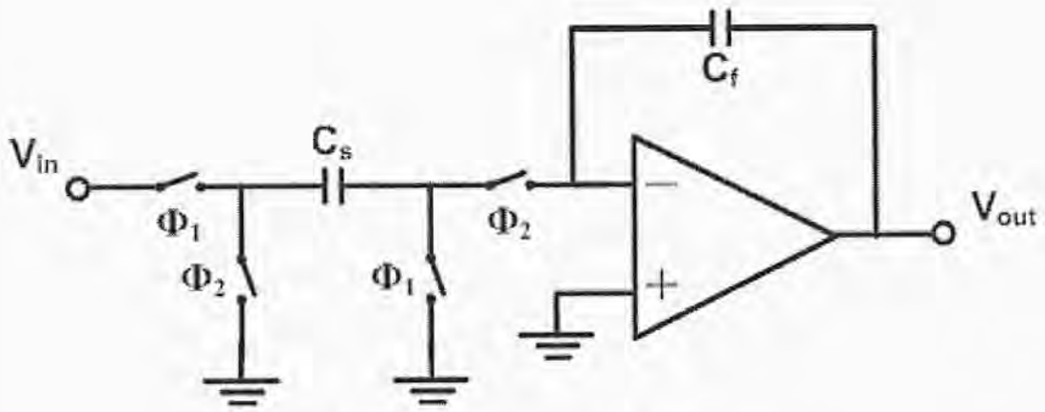


Figure 3.3: The single-ended SC integrator

The ideal single-ended SC integrator transfer function is determined as:

$$H(z) = \frac{C_s}{C_f} * \frac{z^{-1}}{1-z^{-1}} \qquad \text{Eq(3.3)}$$

The DC gain of the integrator is infinite in ideal case. However, the real amplifier has finite dc gain. This consequence of integrator "leakage" that a fraction α is added to the previous output of the integrator to each new input sample. And now, the new transfer function of the integrator with leakage becomes:

$$H(z) = \frac{C_s}{C_f} * \frac{z^{-1}}{1-\alpha z^{-1}} \qquad \text{Eq(3.4)}$$

where the leakage factor α is equal to

$$\alpha = 1 - \frac{1}{A_{OL}} \qquad \text{Eq(3.5)}$$

and A_{OL} is the open loop gain of the amplifier.

3.2.2 Finite bandwidth and slew-rate

There are two regions included in the settling time of Figure 3.4: linear and non-linear region. The linear region is due to the finite gain bandwidth (GBW) of the op-amp; the non-linear settling time is due to slew rate (SR) limitation of the amplifier; furthermore, it is heavily dependent on the step-size of the output.

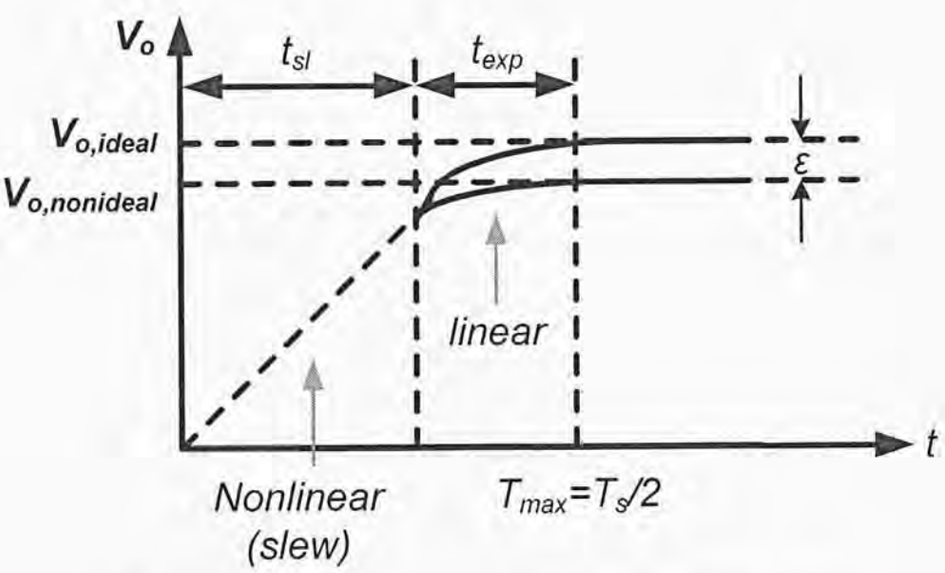


Figure 3.4: Step responses indication the settling time

For the slew rate limitation, slew rate is defined as the maximum rate of change at the output of the amplifier, and can be expressed as:

$$SR = max\left(\frac{dV_o}{dt}\right) = \frac{max(I)}{C_{L,tot}} \qquad \text{Eq(3.6)}$$

For the bandwidth limitation, the settling time is defined to be the time it takes for an amplifier to reach a specified percentage of its final value and can be expressed as [10] :

$$t_{exp} = -\tau \ln \varepsilon_{d,spec} \qquad \text{Eq(3.7)}$$

where time constant τ is limited by the amplifier finite bandwidth and feedback factor, the relationship between the specific error $\varepsilon_{d,spec}$ and the settling time/ time constant ratio can be summarized in Table 3.1.

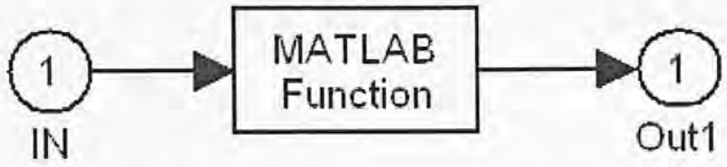
$\varepsilon_{d,spec}$	t_s/τ
1%	4.6
0.1%	6.9
0.01%	9.2
10^{-6}	13.8

Table 3.1: Percentage error and corresponding t_s/τ ratio

So the total settling time $t_{settling}$ is the sum of the abovementioned two times:

$$t_{settling} = t_{sl} + t_{exp} \qquad \text{Eq(3.8)}$$

The Simulink model to realize the finite dc gain, finite bandwidth and finite slew rate is shown in Figure 3.5; it is actually used in a Matlab function block.




```
function out = slew(u, alfa, sr, GBW, Ts)
% Models the op-amp slew rate for a discrete time integrator
% in:   input signal amplitude
% alfa: effect of finite gain (ideal op-amp alfa=1)
% sr:   slew rate in V/s
% GBW:  gain-bandwidth product of the integrator in Hz
% Ts:   sample time
% out:  output signal amplitude

tau=1/(2*pi*GBW);  % Time constant of the integrator
Tmax = Ts/2;
slope=alfa*abs(u)/tau;

if slope > sr              % Op-amp in slewing
    tsl = abs(u)*alfa/sr - tau;  % Slewing time
    if tsl >= Tmax
        error = abs(u) - sr*Tmax;
    else
        texp = Tmax - tsl;
        error = abs(u)*(1-alfa) + (alfa*abs(u) - sr*tsl) * exp(-texp/tau);
    end
else                       % Op-amp u luear region
    texp = Tmax;
    error = abs(u)*(1-alfa) + alfa*abs(u) * exp(-texp/tau);
end
out = u - sign(u)*error;
```

Figure 3.5: The Simulink model of finite dc gain, BW and SR effects

3.3 Capacitor ratio error

The capacitor ratio is the ratio of the feedback or feedforward capacitor and the sampling capacitor in the integrator circuit. And the capacitor has errors when it is produced and also it is influenced by the parasitic capacitors, so it induces the

capacitor ratio error; in the Simulink, we use the mean value and standard deviation to estimate the real ratio as:

$$\text{ratio} = \text{mean} + \text{mean} * \text{std} * \text{randn}(1) \qquad \text{Eq(3.9)}$$

where randn is the normally distributed random number

3.4 Thermal noise

The normal integrator is shown in Figure 3.6(a) [11], where Φ_1 is the sampling phase and Φ_2 is the charging phase. During Φ_1, the circuit can be represented by Figure 3.6(b), the switches S_1 and S_3 can be replaced by on resistance and noise voltages. Then two series switches are combined so that the on resistance is doubled, as in Figure 3.6(c). Then the thermal noise across C_1 in Φ_1 can be expressed as [11]:

$$\overline{v_{n,c1,p1}^2} = \frac{4kT(2R_{on})}{4*(2R_{on})C_1} = \frac{kT}{C_1} \qquad \text{Eq(3.10)}$$

As we can see that the thermal noise induced by C_1 is independent of R_{on}.

During Φ_2, switches S_2 and S_4 are conducting, as shown in Figure 3.6(d); and if we model the operational amplifier as in Figure 3.6(e), and replace the amplifier symbol in Figure 3.6(d), then we can get the whole noise analysis model in Figure 3.6(f). The noise across C_1 in Φ_2 induced by switches and amplifier can be expressed as:

$$\overline{v_{n,c1,p2}^2} = \overline{v_{n,c1,sw}^2} + \overline{v_{n,c1,op}^2}$$

$$= \frac{4kT*(2R_{on})}{4*(2R_{on}+1/g_{m1})C_1} + \frac{16kT/3g_{m1}}{4*(2R_{on}+1/g_{m1})C_1} = \frac{2kTR_{on}+4kT/3g_{m1}}{(2R_{on}+1/g_{m1})C_1} \quad \text{Eq(3.11)}$$

Since these noises are uncorrelated, then the noise across C_1 is the sum of the previous noises, and can be expressed as:

$$\overline{v_{n,c1}^2} = \overline{v_{n,c1,p1}^2} + \overline{v_{n,c1,p2}^2} \quad \text{Eq(3.12)}$$

For the noise across C_2, the noise charge across C_2 is equal to the noise charge across C_1 by charge conservation. So the mean square value of noise across C_2 is:

$$\overline{v_{n,c2}^2} = \frac{C_1^2}{C_2^2}\overline{v_{n,c1}^2} \quad \text{Eq(3.13)}$$

So in the Simulink, we can model the thermal noise source using the blocks as in Figure 3.7, in this model, the gain is multiplied both to noise and input.

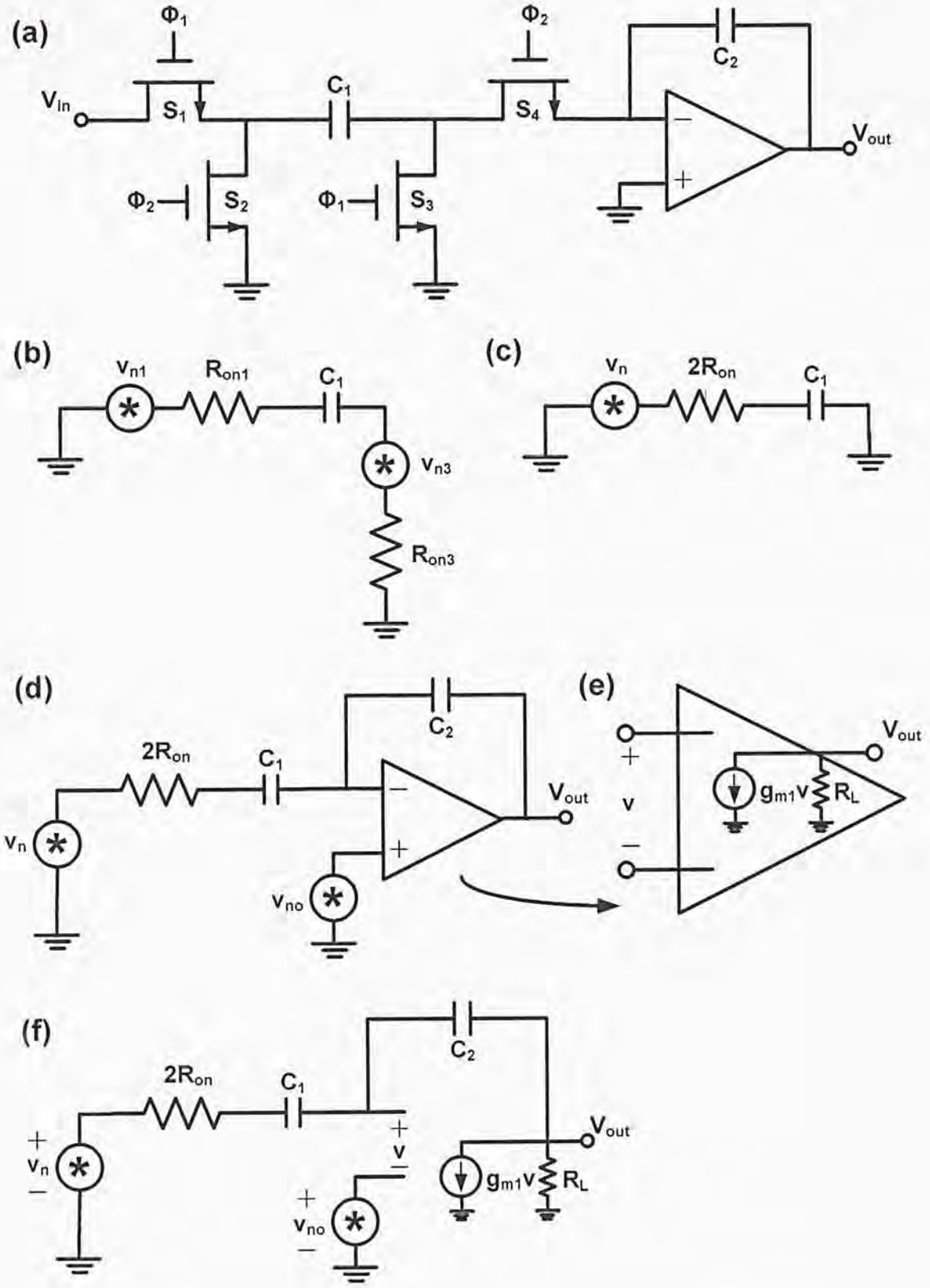


Figure 3.6: The switched capacitor thermal noise analysis in integrator.

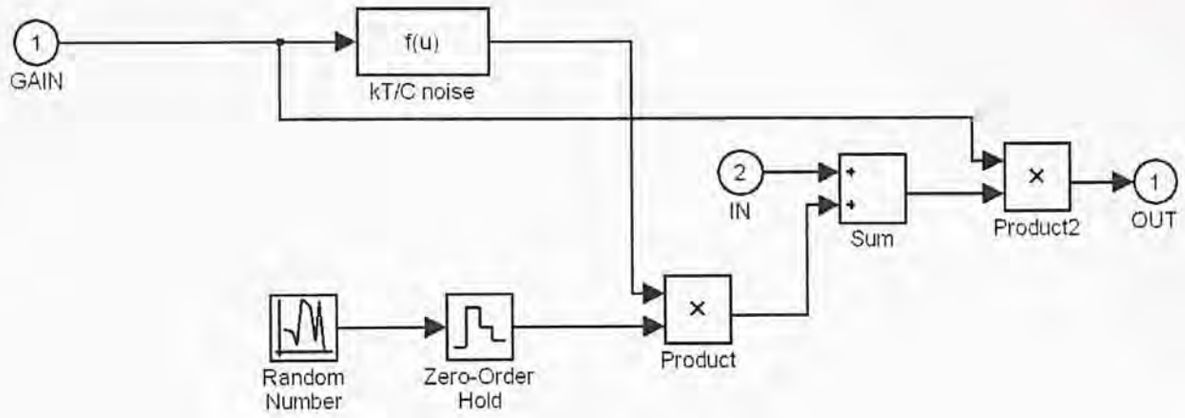


Figure 3.7: The Simulink model for thermal noises

3.5 Switch charge injection error

There exist some errors when the switch suddenly turns off or turns on, in which the main errors are induced by change injection. When the switch turns off, the total charge in the inversion layer Q exits through the source and the drain terminals, this is called charge injection.

As in Figure 3.8, the charge injected to the left side of transistor is absorbed by the input source and creates no error, but the charge injected to the right side of the transistor is deposited on C_H, introducing an error in the voltage stored on the capacitor.

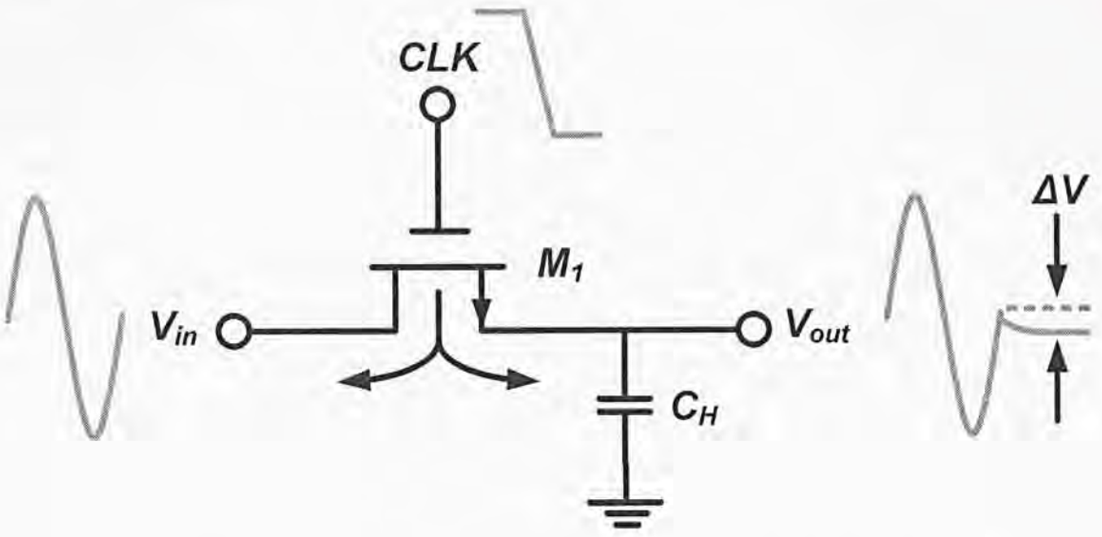


Figure 3.8: Effect of charge injection when the switch turns off

Then we can analyze the charge injection offset error by Figure 3.9(a), assume the standard equation is:

$$\Delta V = \varepsilon V_{in} + V_{OS} \qquad \text{Eq(3.14)}$$

When the clock at V_G is slow clock as in Figure 3.9(b), the voltage difference induced by charge injection can be expressed by:

$$\Delta V = \frac{C_{ov}}{C_H + C_{ov}}[V_L - (V_{in} + V_{th})] \qquad \text{Eq(3.15)}$$

Comparing to Eq(3.14), we can get:

$$\varepsilon = -\frac{C_{ov}}{C_H + C_{ov}} \cong -\frac{C_{ov}}{C_H} \qquad \text{Eq(3.16)}$$

$$V_{OS} = -\frac{C_{ov}}{C_H + C_{ov}}(V_{th} - V_L) \cong -\frac{C_{ov}}{C_H}(V_{th} - V_L) \qquad \text{Eq(3.17)}$$

When the clock at V_G is fast clock as in Figure 3.9(c), the voltage difference induced by charge injection can be expressed by:

$$\Delta V = \frac{C_{ov}}{C_H + C_{ov}}(V_L - V_H) - \frac{WLC_{ox}(V_H - V_{in} - V_{th})}{2C_H} \quad \text{Eq(3.18)}$$

Comparing to Eq(3.14), we can get:

$$\varepsilon = \frac{WLC_{ox}}{2C_H} \quad \text{Eq(3.19)}$$

$$V_{OS} = \frac{C_{ov}}{C_H + C_{ov}}(V_L - V_H) - \frac{WLC_{ox}(V_H - V_{th})}{2C_H} \quad \text{Eq(3.20)}$$

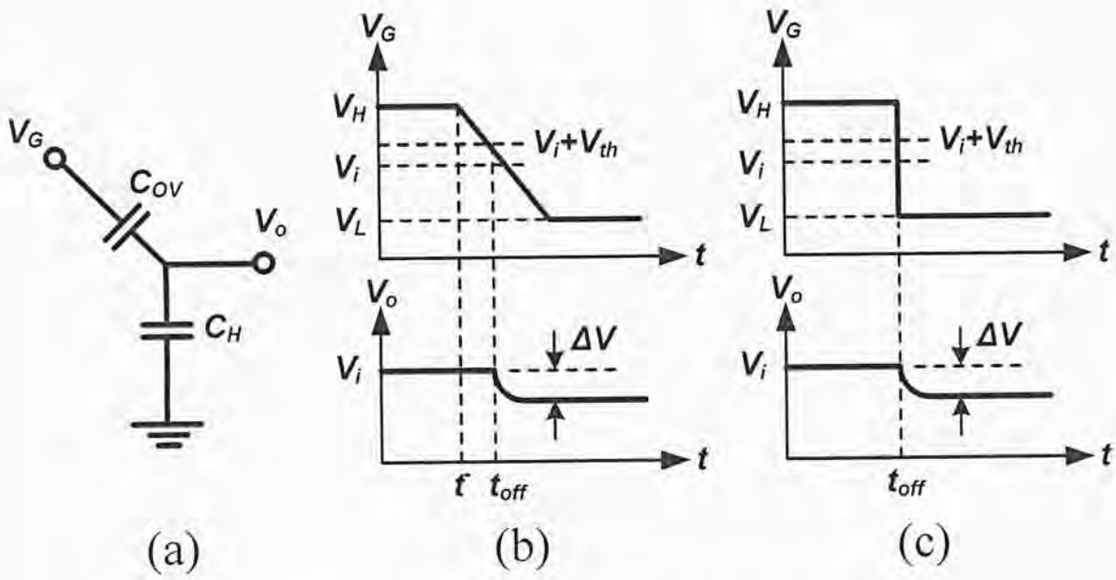


Figure 3.9: The analysis model of switched capacitor circuit

In order to reduce the injection current and the nonlinearity, we incorporate both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other. As Figure 3.10, for Δq_1 to cancel Δq_2, we must have

$$-\Delta q_1 = \Delta q_2 \quad \text{Eq(3.21)}$$

$$-W_n L_n C_{ox}(V_H - V_{in} - |V_{thn}|) = W_p L_p C_{ox}(V_{in} - |V_{thp}|) \quad \text{Eq(3.22)}$$

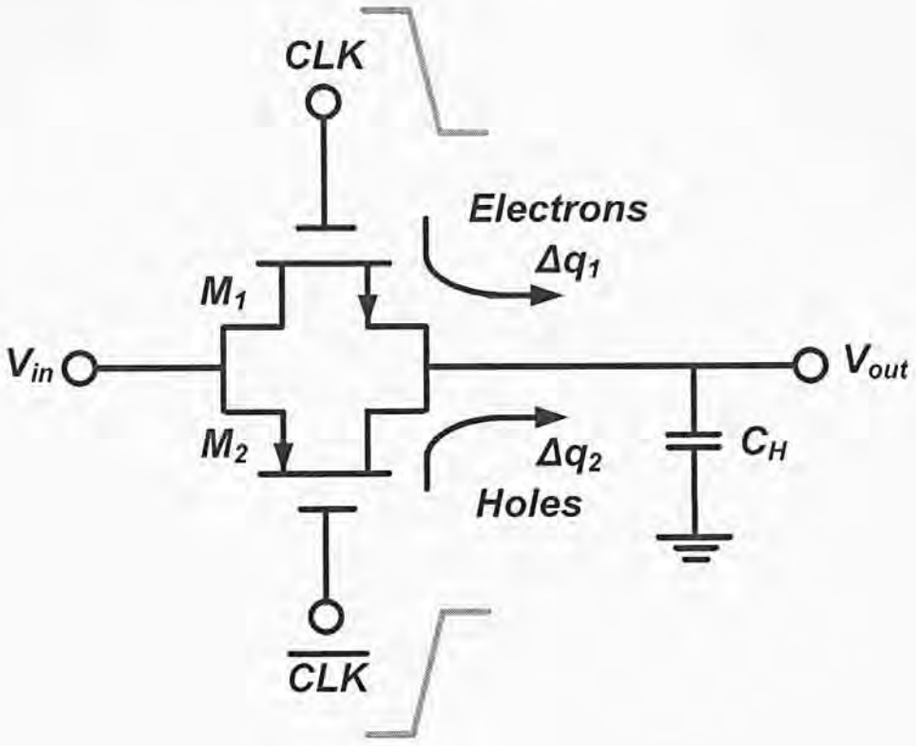


Figure 3.10: CMOS switch to reduce signal dependent offset

If we want the resistance of CMOS to be independent of input voltage, we should set:

$$W_n L_n = W_p L_p \qquad \text{Eq(3.23)}$$

Figure 3.11 plots the behavior of $R_{on,eq}$ in the general case, revealing much less signal dependent variation than that corresponding to each switch alone. So CMOS is also more suitable to be used in the circuit with large signal swing.

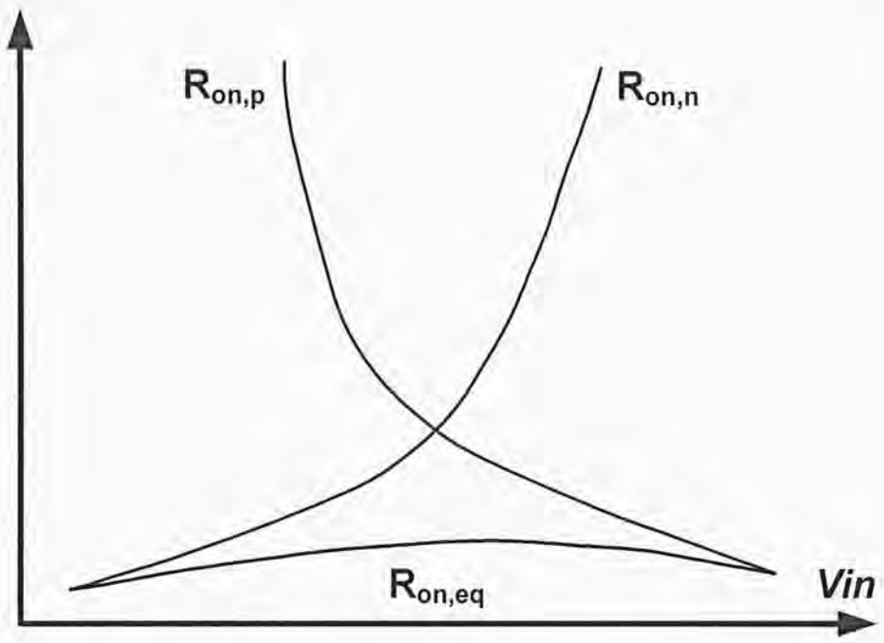


Figure 3.11: On-resistance of the complementary switch

In the Simulink model, we can just add some offsets at specific points to represent the charge injection effect.

3.6 Conclusion

In this section, we have introduced some non-ideal effects and their Simulink modeling method, such as clock jitter, finite amplifier dc gain, and finite amplifier bandwidth and slew rate, thermal noise, coefficient mismatch and switch charge injection error. Through the previous analysis, we can make sure that our Simulink models can successfully model many types of DSM.

Chapter 4 A Chopper-Stabilized High-Pass Delta-Sigma Modulator in 1.8V 0.18μm CMOS

In this section, a chopper-stabilized high-pass DSM will be introduced step by step, which includes the structure selection, system modeling and parameter selection, circuit implementation, layout implementation, and measurement results.

4.1 Structure selection

Firstly, the initial target of this DSM is to achieve 12 bits resolution with the signal bandwidth 1kHz, through the final result of Eq(2.7):

$$DR = 6.02N + 1.76 + 10log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10log(OSR) \quad \text{Eq(4.1)}$$

And for 12 bit resolution DSM, its corresponding dynamic range is 12*6.02+1.76=74dB. We select the loop order L=2, the quantizer bit N=1 and the oversampling ratio OSR=128, thus it can achieve dynamic range of 94dB. The additional 20dB is the margin to make sure the goal can be achieved.

So firstly we construct a second order single bit DSM block diagram as in Figure 4.1, and the transfer function is:

$$Y = z^{-3/2}X + (1 - z^{-1})^2 E \quad \text{Eq(4.2)}$$

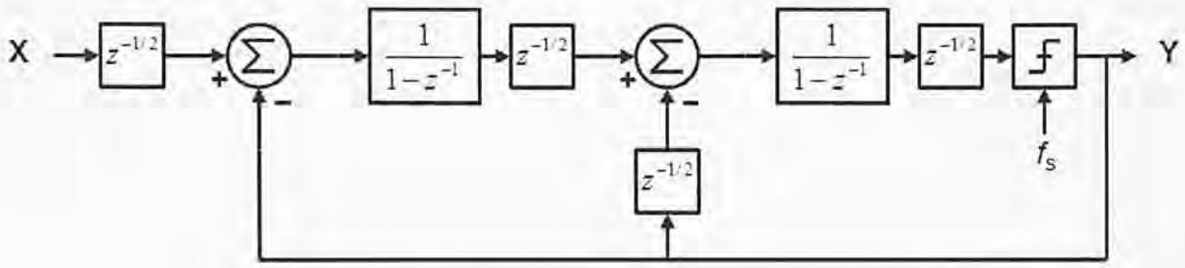


Figure 4.1: The block diagram of selected DSM

For the input signal bandwidth is in the frequency band of flicker noise, we should use chopper-stabilized technique to separate them to a different frequency band; at the same time, in a chopper-stabilized DSM, the chopping frequency, f_{ch}, is often set at $f_s/4$ or $f_s/2$, where f_s is the sampling frequency of the DSM. When $f_{ch} = f_s/4$, the modulator must be of a band-pass one with noise notches at $f_s/4$. When $f_{ch} = f_s/2$, it must be of a high-pass one with noise notches at $f_s/2$. Furthermore, a second order band-pass modulator only gives a first order noise shaping. In contrast, a second order high-pass modulator in the latter case gives a second order noise shaping. Thus the high-pass option is more efficient in terms of chip area and power consumption [12].

There is a former case called resonator-based high-pass structure [12]. The notch frequency, and thus the signal to noise ratio (SNR), of the resonator-based modulators are very sensitive to capacitor mismatches, only small mismatch of the capacitors may induce the SNR to an unacceptable value.

Comparing to the resonator-based high-pass structure, the mirrored integrator high-pass structure that is introduced in section 2.4, is more immune to the mismatch. So in this project, the mirrored integrator high-pass structure is used.

The design here starts from the second-order low-pass DSM prototype shown in

Figure 4.1. It has a half-sample delay in each integrator. Four pairs of choppers are then inserted in the front and rear ends of each non-delayed integrator, as shown in Figure 4.2(a). This insertion does not affect the STF or NTF of the modulator as two adjacent choppers null the effect of each other. Figure 4.2(b) shows the equivalent model by moving choppers A and B backward and C forward in the signal flow direction. Further equivalence is obtained in Figure 4.2(c) with the choppers D and E in Figure 4.2(b) moved backward and F forward [8][9]. The relationships between chopper clocks and the main clock Φ_1 and Φ_2 are shown in Figure 4.3. It is noticed that c[n] = –c[n-1] and c[n-1/2] = –c[n-3/2].

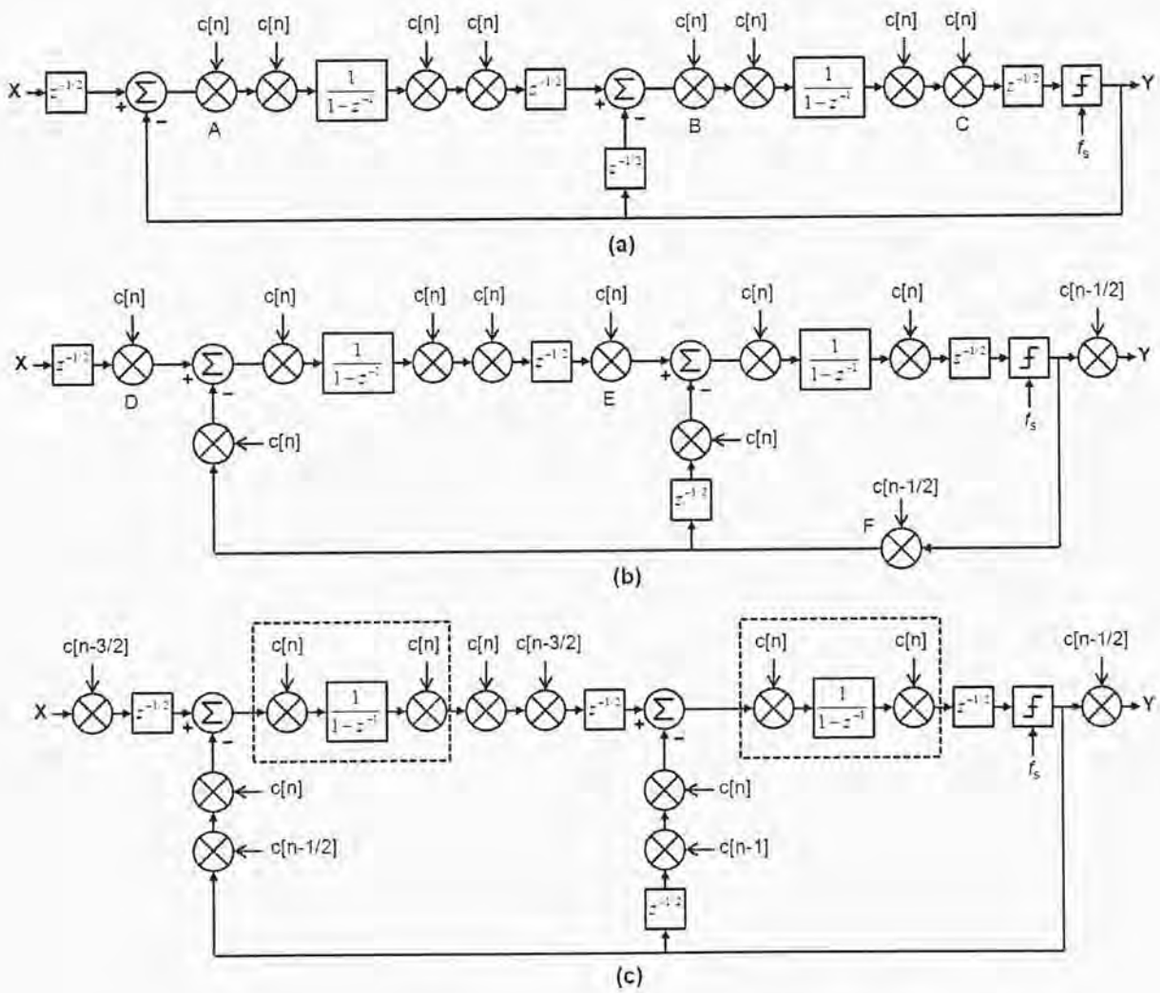


Figure 4.2: The transformation from normal structure to high-pass structure

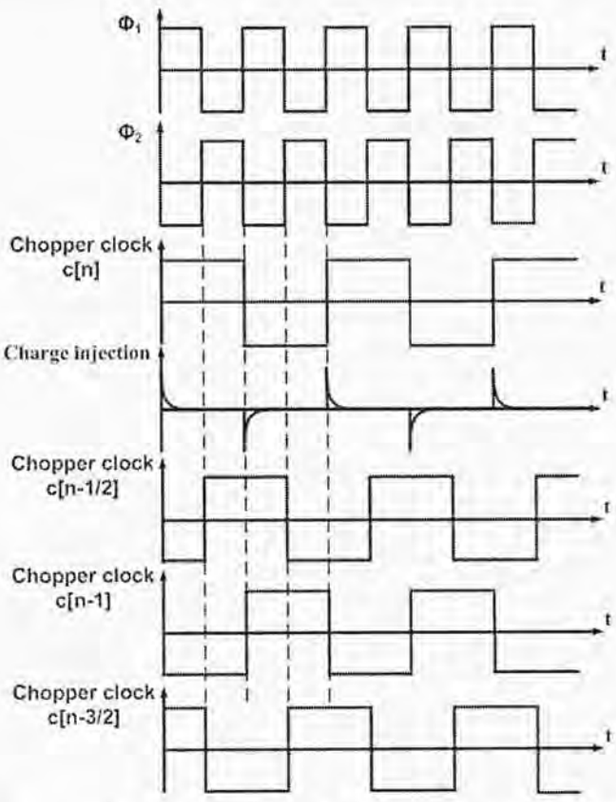


Figure 4.3: The clock relationship of the DSM

The overall system of Figure 4.2(c) is a low-pass modulator from input X to output Y. However, the modulator itself, i.e., the circuit after the first chopper following input X, is of a high-pass type and the modulator is therefore referred to as a high-pass modulator. The mirrored integrator of Figure 2.15 can be used to implement the two boxed blocks in Figure 4.2(c).

Furthermore, the two boxed parts have identical structure and there is a half clock delay between them, meaning that their change transfer phases are interleaved. Therefore, these two blocks can share a single amplifier in the circuit implementation.

4.2 System modeling and parameter selection

Firstly, in the Simulink, we should construct the block diagram as in Figure 4.2(c).

In order to reduce the signal swings at integrators' outputs for improved linearity performance of the modulator, we should scale the coefficient of DSM. Figure 4.4 shows the output swing of each integrator with -3dB input signal, the total time of x-axis is nfft*Ts, where Ts is the sampling period and nfft is the number of points selected. Because for folded-cascode amplifier, the output swing is $V_{DD}-2V_{DS,SATN}-2V_{DS,SATP}\approx 1.8-0.4-0.4=1$ V. So the scaling factors are chosen such that the integrators' outputs have a swing less than 0.8V (give 0.2V margin). Based on system-level simulations, the capacitor ratio is set to be 1/8, 1/2.

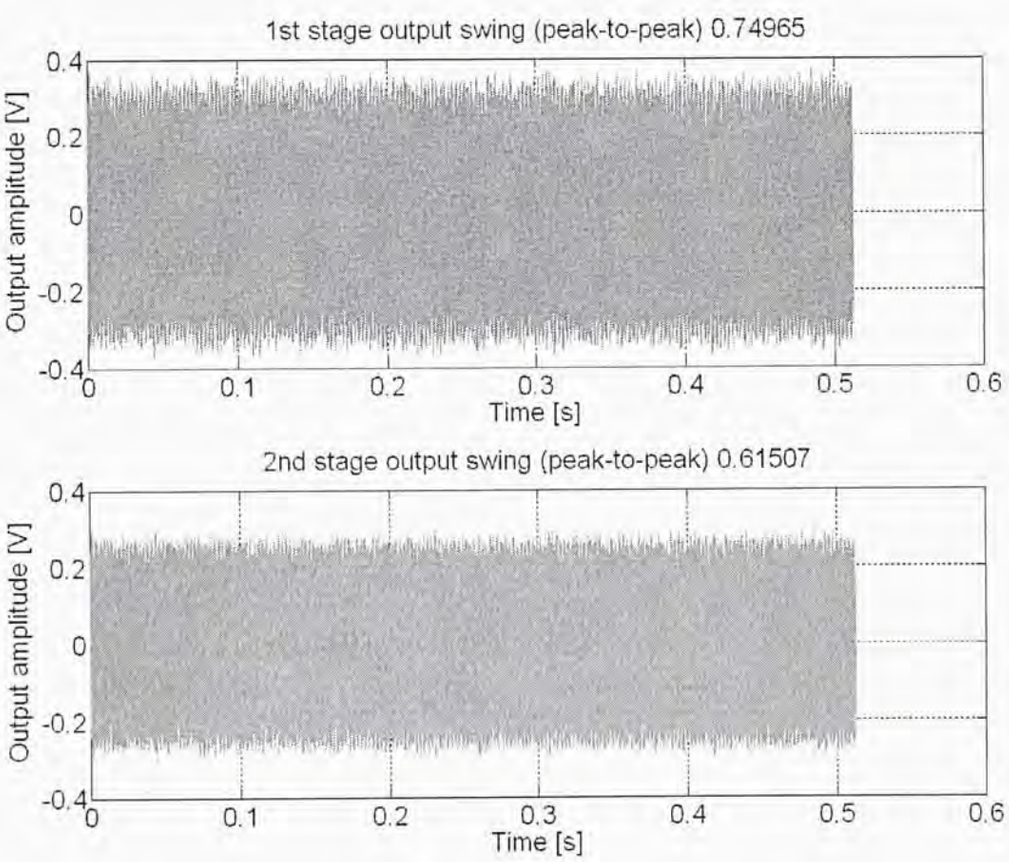


Figure 4.4: The output waveform of each stage of DSM

So finally after output scaling of each stage, the block diagram of the whole circuit is shown in Figure 4.5.

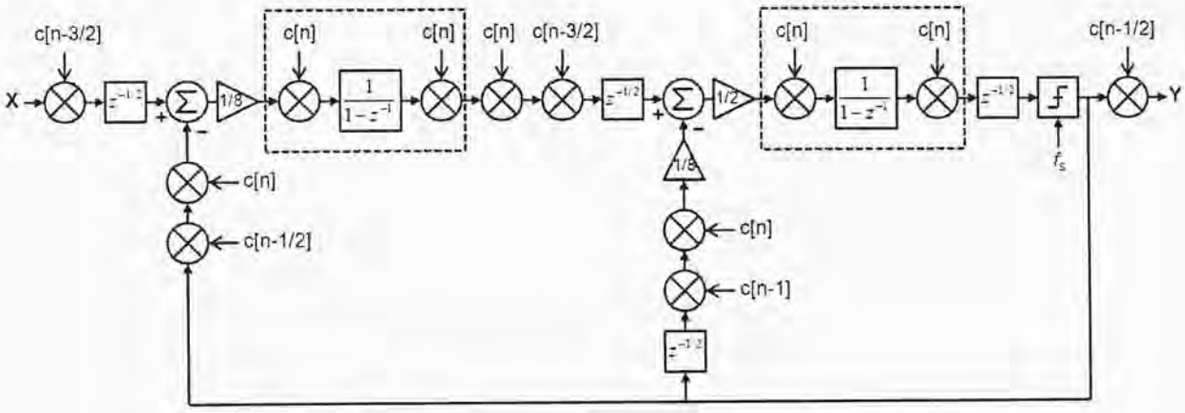


Figure 4.5: The block diagram of the modulator with output scaling.

Then the system-level model can be built from the block diagram shown in Figure 4.5, and with the consideration of several non-ideal effects in Chapter 3, the whole model is shown in Figure 4.6. In this block diagram system, we not only added the jitter noise, thermal noise, amplifier finite dc gain, amplifier finite bandwidth, amplifier finite slew rate, coefficient mismatch, but also added the offset on specific place and the feedback noise. The zero-order hold blocks are used to specify half sampling period, because we constructed some half delay blocks in Figure 4.6. The choppers here are realized by multiplying the original signal to the positive and negative references.

Finally the output spectra spectrum is shown in Figure 4.7. The SNR is now 86.1dB, which is 8dB less than the calculated value, and this is acceptable because we induced some small non-ideal effects when we do the simulation.

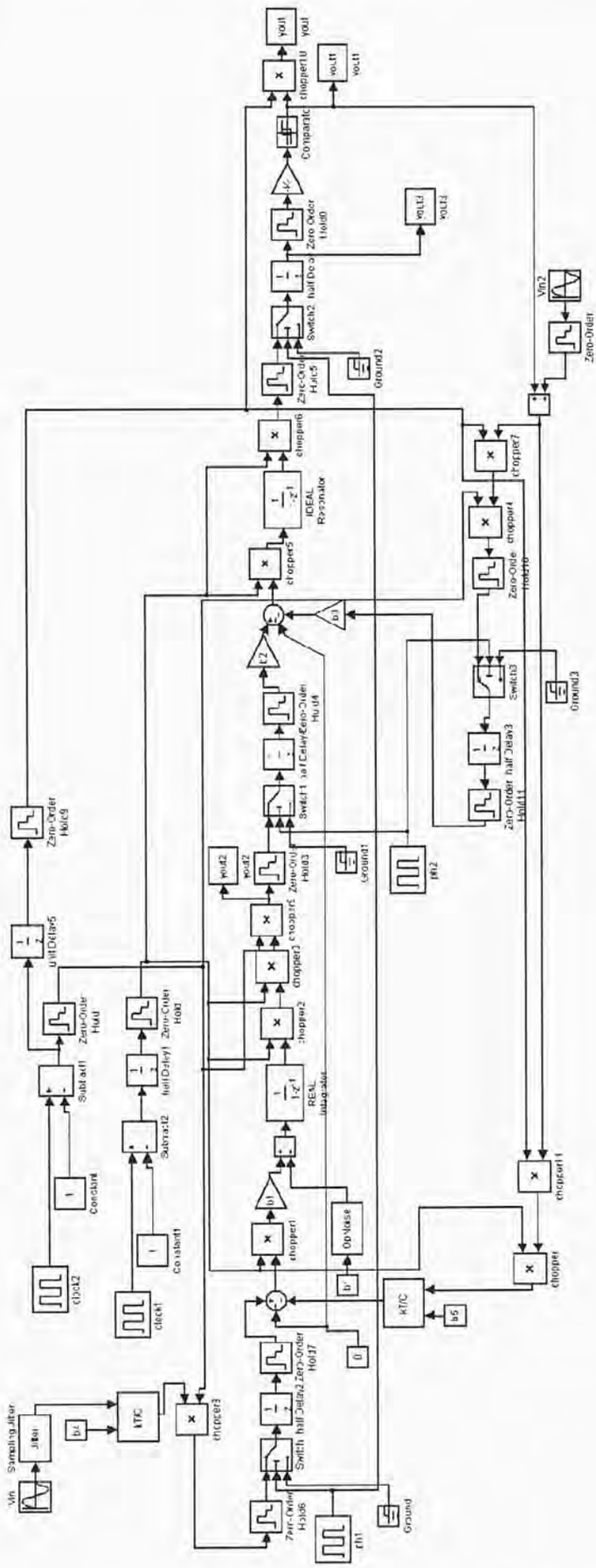


Figure 4.6: The Simulink model of the whole system.

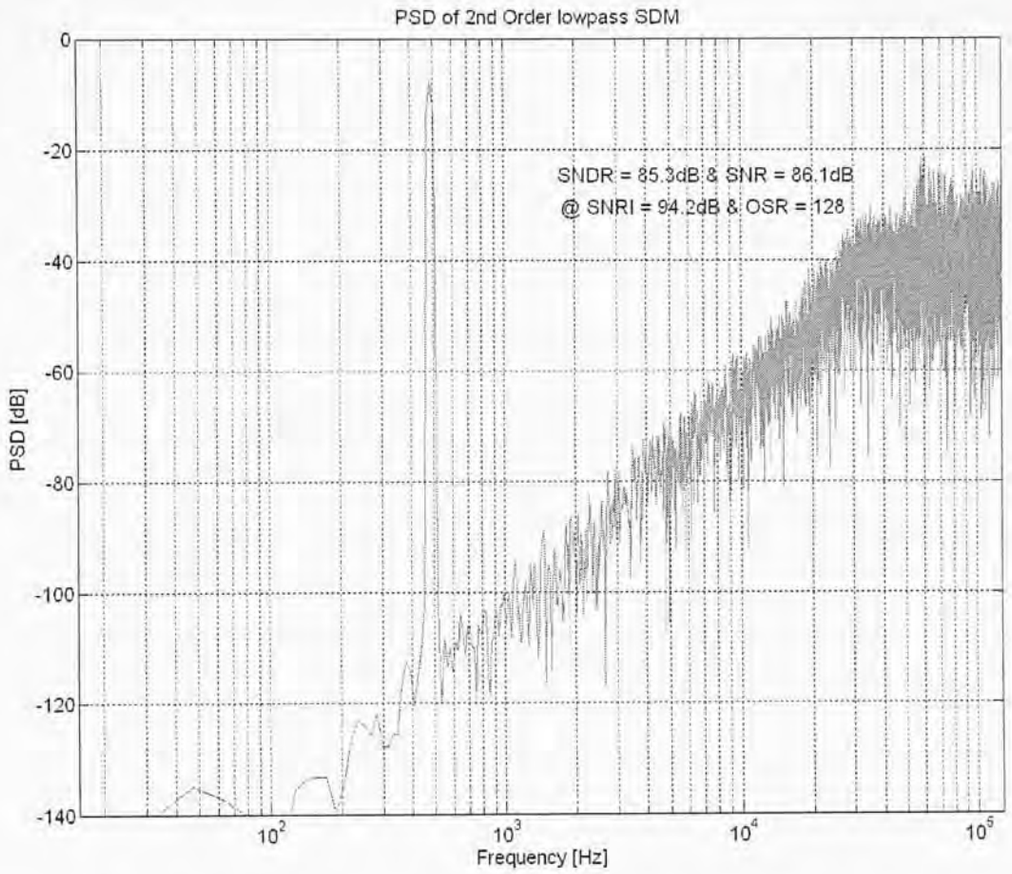


Figure 4.7: The simulation output spectra of Simulink model.

4.3 Circuit implementation

4.3.1 Operational amplifier

In this project a simple single-stage folded-cascoded operational amplifier has been used to achieve high open-loop gain, and as shown in Figure 4.8. The open-loop gain of the amplifier can be calculated as:

$$A_{DC} = g_{m1}[g_{m5}r_{o5}(r_{o3}//r_{o1})//g_{m7}r_{o7}r_{o9}] \qquad \text{Eq(4.3)}$$

And the unity bandwidth frequency is

$$f_b = g_{m1}/2\pi C_L \qquad \text{Eq(4.4)}$$

The input referred noise of this amplifier is:

$$\overline{v_{n,op}^2} = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right) \approx \frac{16kT}{3g_{m1}} \qquad \text{Eq(4.5)}$$

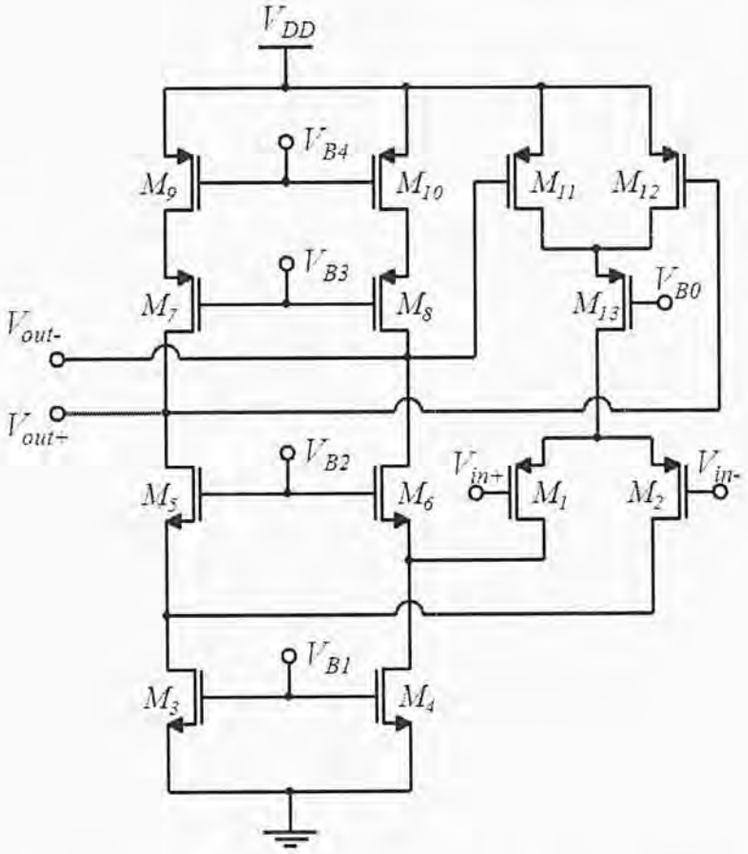


Figure 4.8: The folded-cascode operational amplifier.

The ac response of this amplifier with a 3-pF loading is shown in Figure 4.9, the amplifier has a DC gain of 63dB, a unity-gain frequency of 7.1MHz and a phase margin of 67°.

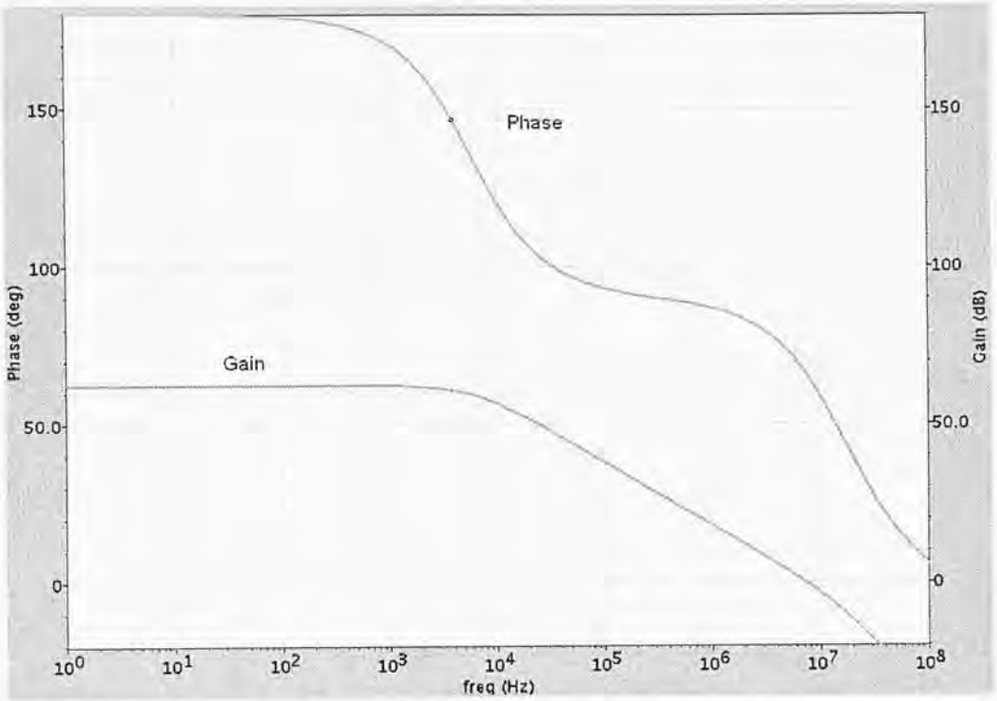


Figure 4.9: The AC response of the amplifier.

4.3.2 Quantizer

Quantizer is one of the most important parts in the analog-to-digital conversion, it can convert the continuous input into several non-overlapping ranges, a discrete and specific value assigns to each sub-ranges. The number of the sub-ranges depends on the resolution of the quantizer. For example, an N-bit quantizer has 2^N levels and 2^{N-1} intervals. The discrete output then is converted into digital code.

There are two main kinds of quantizers: mid-rise and mid-tread, which are shown on Figure 4.10. The x-axis and the y-axis are the input and the output respectively. The unit of them is one least significant bit. In order to cancel the offset voltage, the transfer function should be symmetric. If the quantizer is mid-rise quantizer, the number of levels should be even. And if the quantizer is mid-tread quantizer, then the

number of level should be odd.

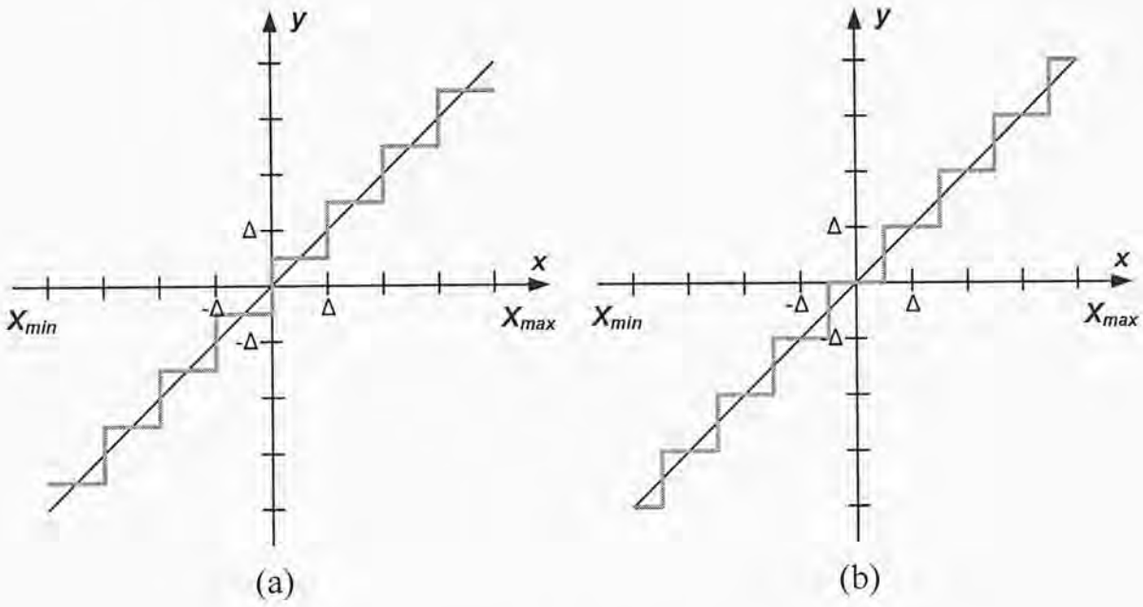


Figure 4.10: (a) Mid-rise and (b) mid-tread quantizer.

In this project, 1 bit quantizer is used, which means that the output has only two levels, V_{REF+} and V_{REF-}; 1 bit quantizer has the advantage of good linearity, and its circuit representation is only a comparator.

For the normal comparator, it often has two main problems which influence the performance of the circuit, one is called offset error, and the other is called propagation delay. As shown in Figure 4.11, the offset error of the comparator will influence the threshold voltage which in turn changes the duty cycle of the output waveform. The propagation delay is the time difference between the mean value of input excitation and the mean value of the output response, as shown in Figure 4.12.

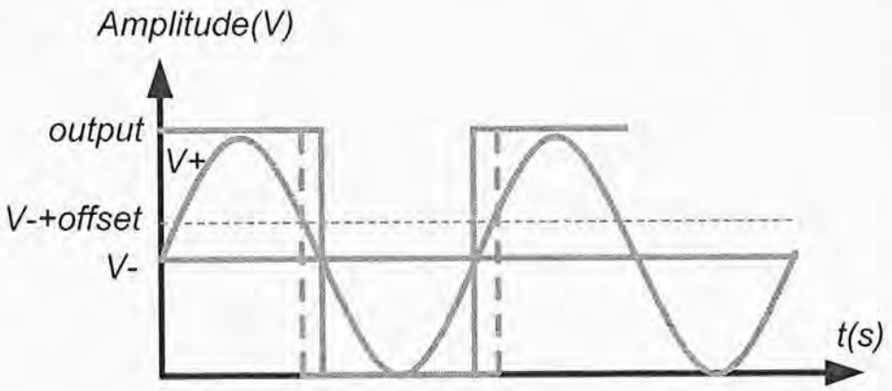


Figure 4.11: The comparator offsets.

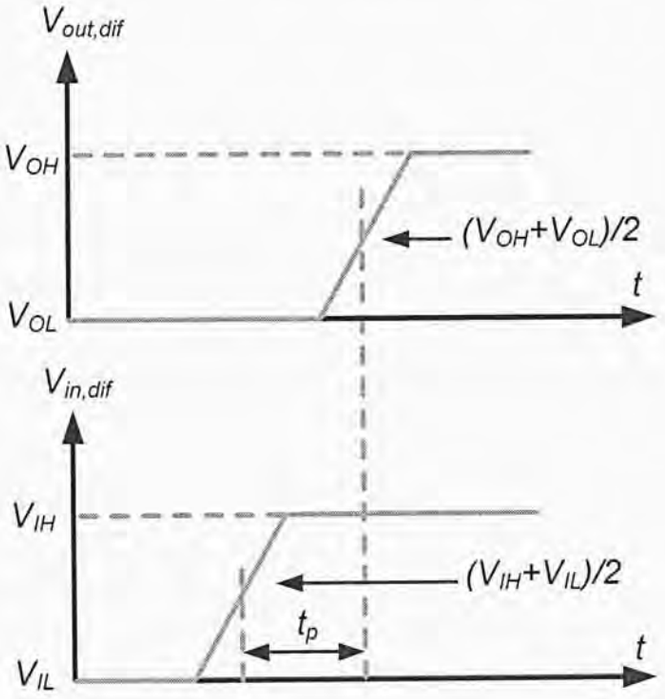


Figure 4.12: The comparator propagation delay.

In this project, a conventional dynamic latched comparator is used in the modulator for low power consumption. The schematic is shown in Figure 4.13. The internal nodes are reset to ground in non-active periods to eliminate any memory effect.

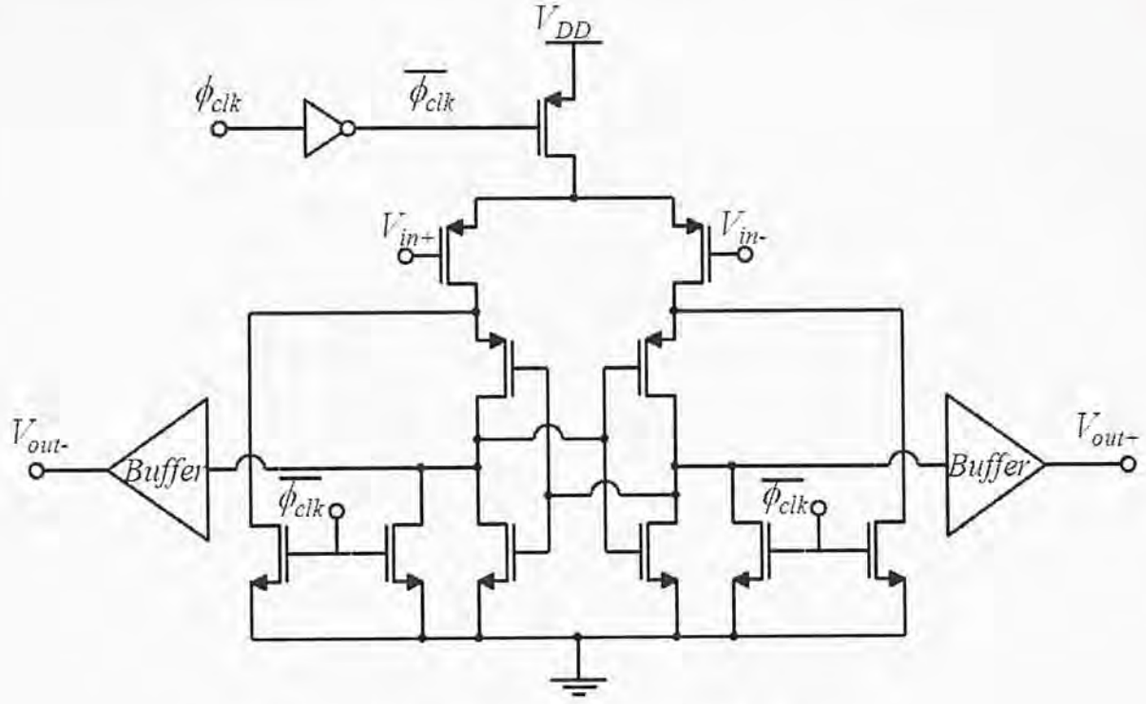


Figure 4.13: The comparator circuit diagram.

4.3.3 Frequency divider

A master-slave frequency divider circuits (divided by two) are used to generate the chopper clocks from the main clocks Φ_1 and Φ_2, as shown in Figure 4.14.

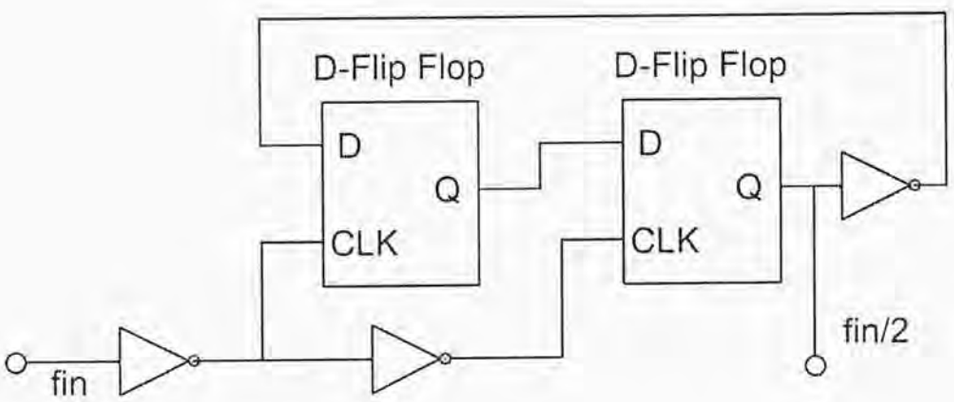


Figure 4.14: The frequency divider circuit diagram.

4.3.4 Overall circuit

Figure 4.15 shows the switched-capacitor implementation of the proposed modulator (Figure 4.5). The values of the capacitors are: C_1 = 0.5pF, C_2 = 2pF, C_3 = 0.5pF, C_{h1} = 4pF, and C_{h2} = 4pF. These capacitance values are chosen such that a thermal noise limited SNR (including the amplifier's thermal noise) of 94dB is resulted (using the thermal noise estimation method presented in [11]). This 94dB value is the SNR of an ideal 2nd order 1-bit modulator with an oversampling ratio of 128. It is noticed that these capacitance values are chosen conservatively because our targeted performance is only 12bit (74dB SNR) and the main purpose of this work is to verify the proposed offset reduction technique. Smaller capacitance values can be used for more aggressive power optimization.

The boxed blocks in Figure 4.5 share the same amplifier and choppers. In Figure 4.15, the chopper in front of the amplifier is the most critical one in terms of generating the charge injection error. The charge injection error from the chopper that follows V_{in} is also important, but it can be carefully minimized by using the bottom-plate sampling technique. Other choppers are either enclosed inside the modulator loop or in the digital domain and their charge injection errors are of much less importance.

The master chopper clock c[n] can be aligned either to Φ_1 or Φ_2. The choice here has a significant impact on the residual offset. Since the charge injection occurs only when the switch changes its status, we let the chopper switches switch when Φ_1 goes HIGH and Φ_2 goes LOW, as shown in Figure 4.3. So error charge flows through the

switch controlled by Φ_{1E} (Φ_{1E} being the same as Φ_1 except having a slightly earlier fall time compared to the latter) to C_{h2}, which belongs to the second stage. In addition, Φ_{2E} (Φ_{2E} being the same as Φ_2 except having a slightly earlier fall time compared to the latter) is made to go LOW slightly earlier than the chopper's switching moment in order to ensure no error charge flows to the first stage capacitor C_{h1} [13], we have given enough margin to achieve good charge reducing effects. Now, the error charge due to mismatches of the chopper switches flows to the second stage instead of the first stage. Since any error in the second stage of the DSM is suppressed by the gain preceding it, the charge injection error is significantly reduced, actually by a factor equal to the open-loop gain of the first stage amplifier (the shared amplifier).

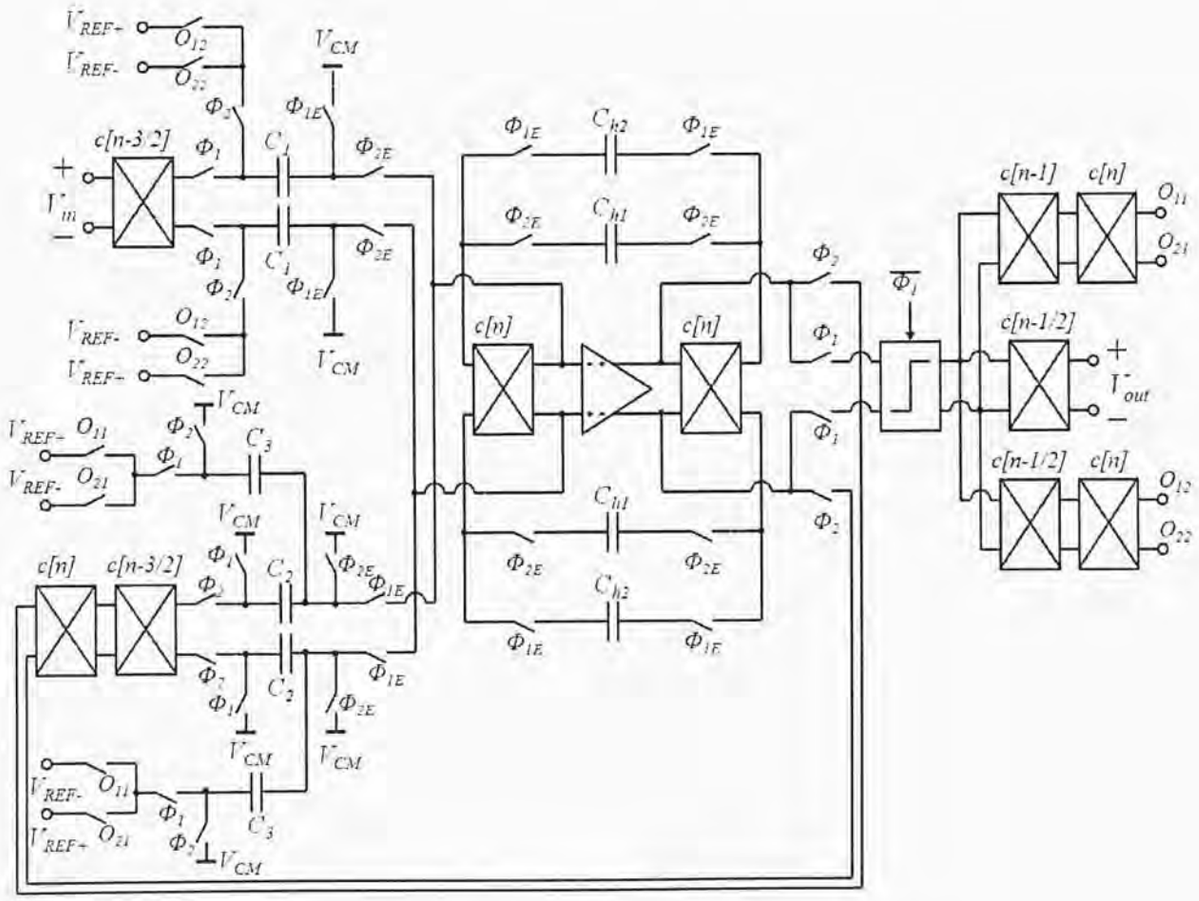


Figure 4.15: The whole modulator circuit diagram.

4.4 Layout implementation

4.4.1 Layout symmetric technique

a. Inter-Digit

For large transistors, symmetry becomes more difficult to establish. The two transistors of the input pair have a large width so as to achieve a small input offset voltage, but gradients along the x-axis give rise to appreciable mismatches. Such gradient-induced mismatches can be minimized by reducing the distance between the centroid of the matched devices. The common-centroid layouts can totally cancel the effects of long-range variations by dividing the transistors into fingers or segments to allow the construction of a compact array. The simplest types of arrays involve the placement of multiple device fingers in parallel. If these fingers are properly inter-digit, then the centroid of the matched devices will align at a point midway along the axis of symmetry bisecting the array. Figure 4.16 shows an example of a pair of matched MOS transistors laid out as an inter-digit array.

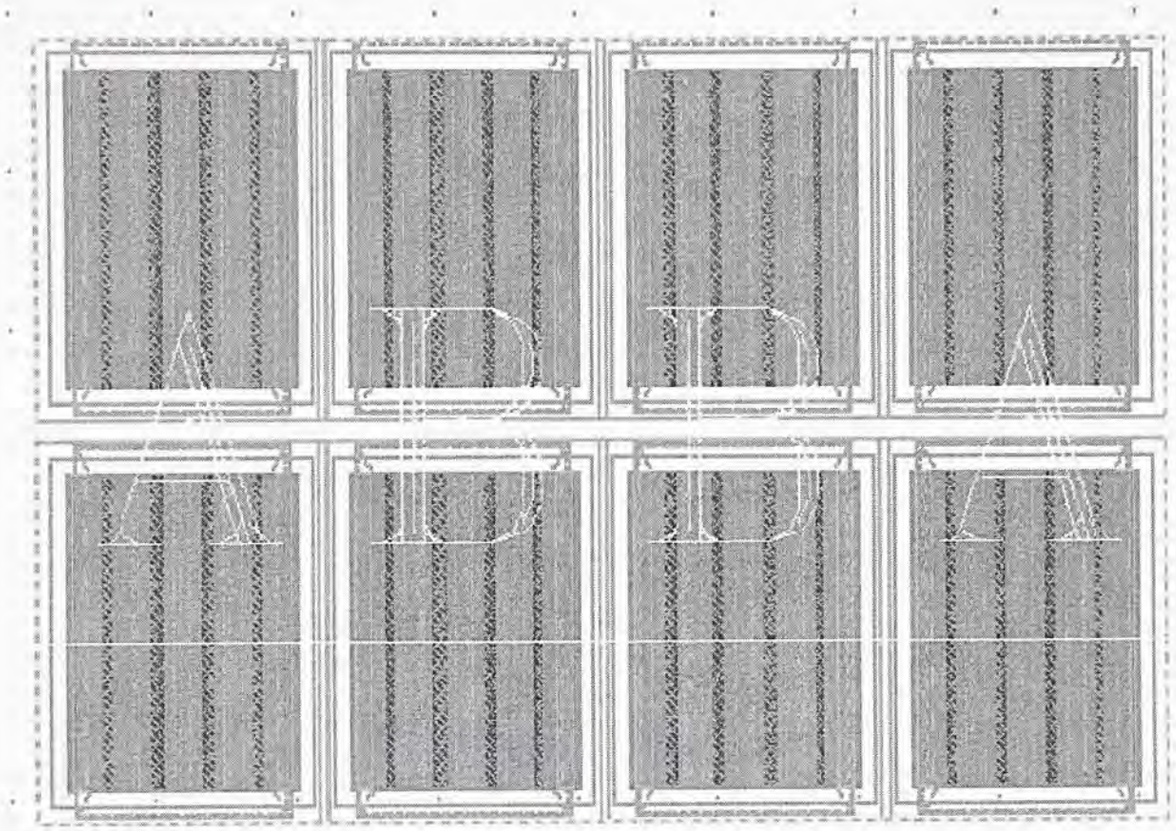


Figure 4.16: Inter-digit MOS transistors.

b. Two-dimensional common-centroid

The best possible cancellation of gradients is not provided by inter-digit MOS transistors because they depend on the symmetry of individual device segments to provide one of their two axes of symmetry. A two-dimensional common-centroid array provides a high degree of symmetry because both axes of symmetry arise from the layout of the array rather than if is comprised from the segments. This sort of layout is called the cross-coupled pairs and it is shown in Figure 4.17.

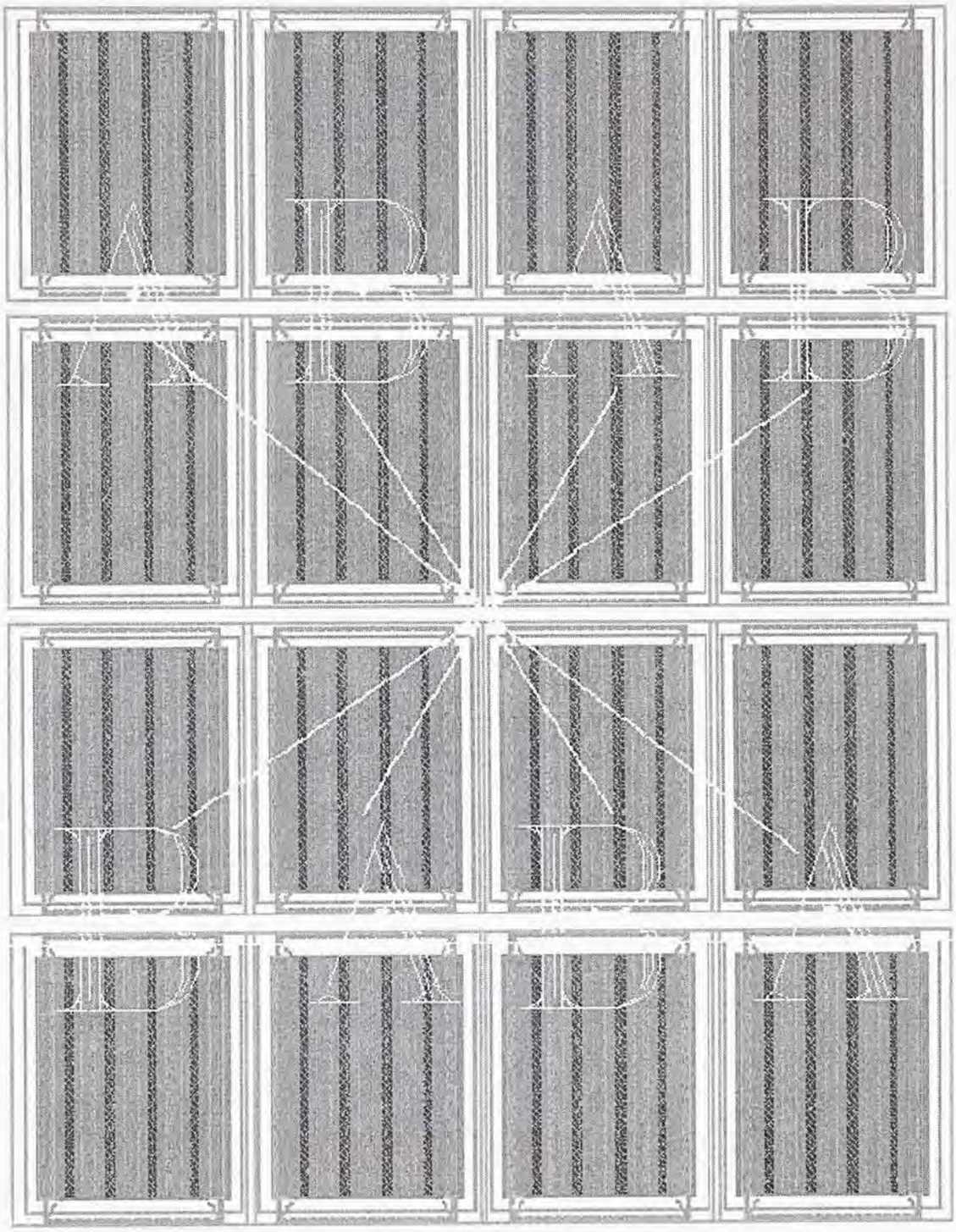


Figure 4.17: Cross-coupled MOS transistors.

c. Dummy

Dummy segments at the end of two sides should be included in arrayed transistors. Figure 4.18 shows that the segments of M_1 and M_2 are approximately in the same

environment. Furthermore, the two devices sustain no asymmetry result from shadowing. The spacing must be equal in between the dummy segments and the actual segments and the spacing between actual segments. In addition, the dummy transistor must be connected preferably to the high to low reference in potential that channel formation beneath them is prevented.

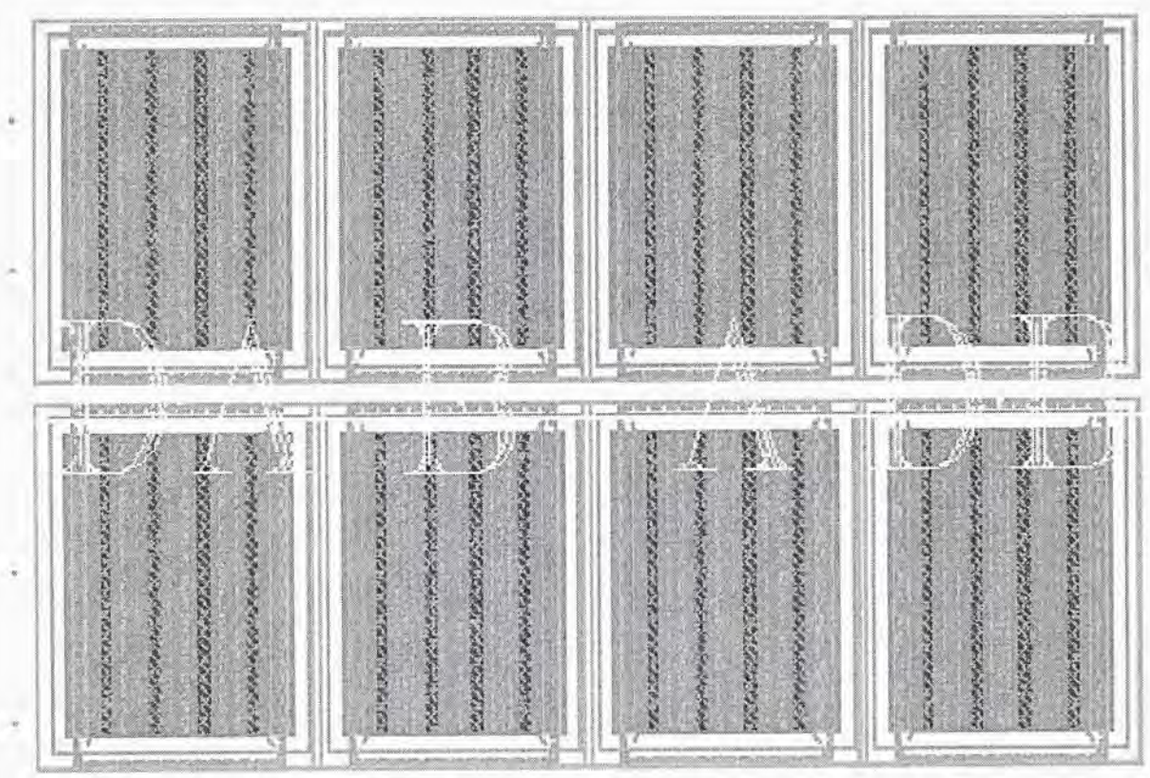


Figure 4.18: Addition of dummy device to improve symmetry.

4.4.2 Circuit layout

The folded-cascode amplifier has been drawn using inter-digit technique, and the layout is shown in Figure 4.19, the PMOSs were put on the upper half and the NMOSs

were put on the lower half, the input differential pair has best matching in layout because it uses two-dimensional common centroid technique.

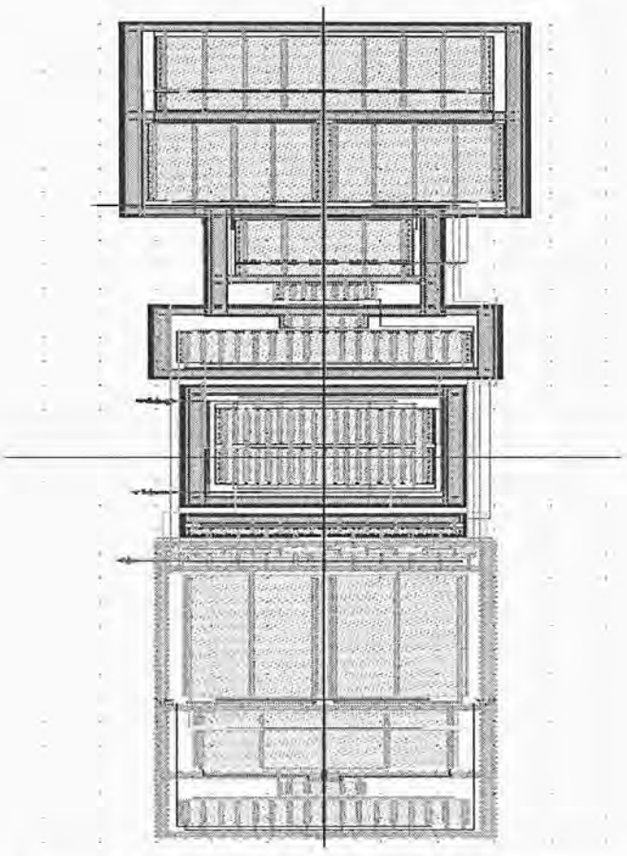


Figure 4.19: Layout of operational amplifier.

The layout of comparator is shown in Figure 4.20, the matching of the comparator is not very important because our DSM is only one bit. So the input pair uses simple inter-digit technique but not two-dimensional common centroid technique.

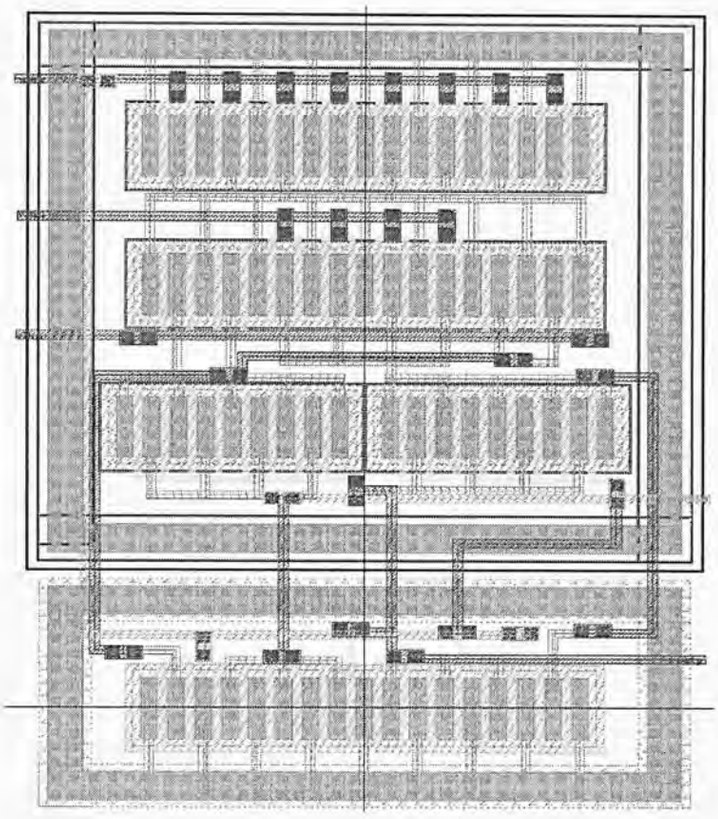


Figure 4.20: Layout of comparator.

For there are lots of clocks in this project, and some clocks require relative large clock delay, so the clock system occupies large area and has lots of output clocks, as shown in Figure 4.21.

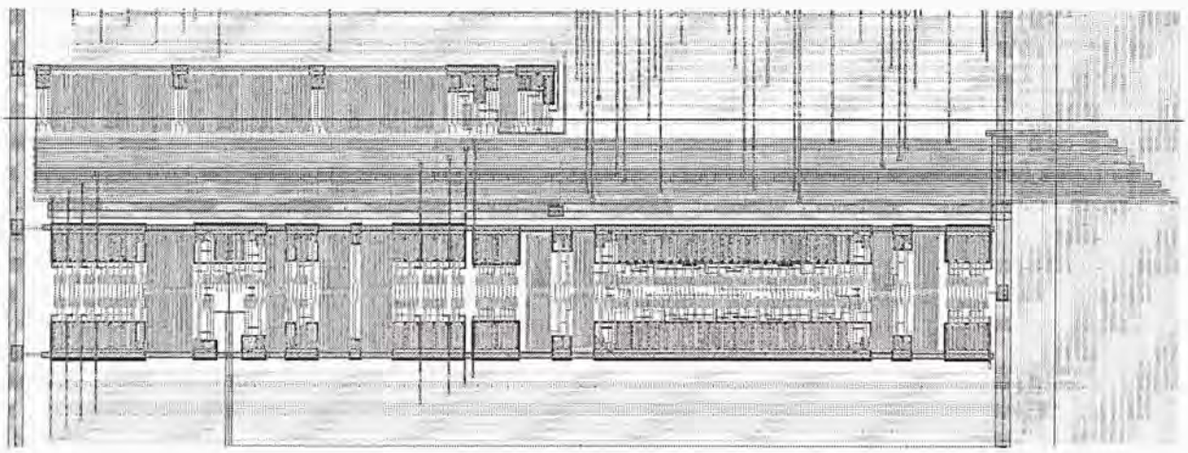


Figure 4.21: Layout of clock system.

4.4.3 Floor planning and top level inter-connection

Once the dimensions of the die and the areas of all the cells have been determined, a floor plan should be constructed. A good floor plan includes an outline of the dies, and the sizes and locations of all major cells. The initial floor plan often requires revision as the layout processes. The floor planning of this DSM is shown in Figure 4.22. As we can see that the clock system is the noisiest part, and the digital logics and switches also induce noises; so the amplifier is located away from these noise sources, and the capacitor is located to separate the noisy part and amplifier. For the comparator, the accuracy requirement is not high in this project, so we can put it around switches.

The final layout process is the top-level inter-connection. It should be verified that the each analog signal has been properly routed. In this layout design, the channel routing technique uses multi-metal layers to produce a compact wiring arrangements, as shown in Figure 4.23. This chopper-stabilized high-pass DSM was fabricated in a 0.18μm 1-poly 6-metal CMOS process. The core size is only 380μm*420μm. The whole chip is 720μm*750μm with the 13 pads included. The clock generation circuit occupies a substantial portion of the chip due to the use of NMOS capacitors to generate some required delays.

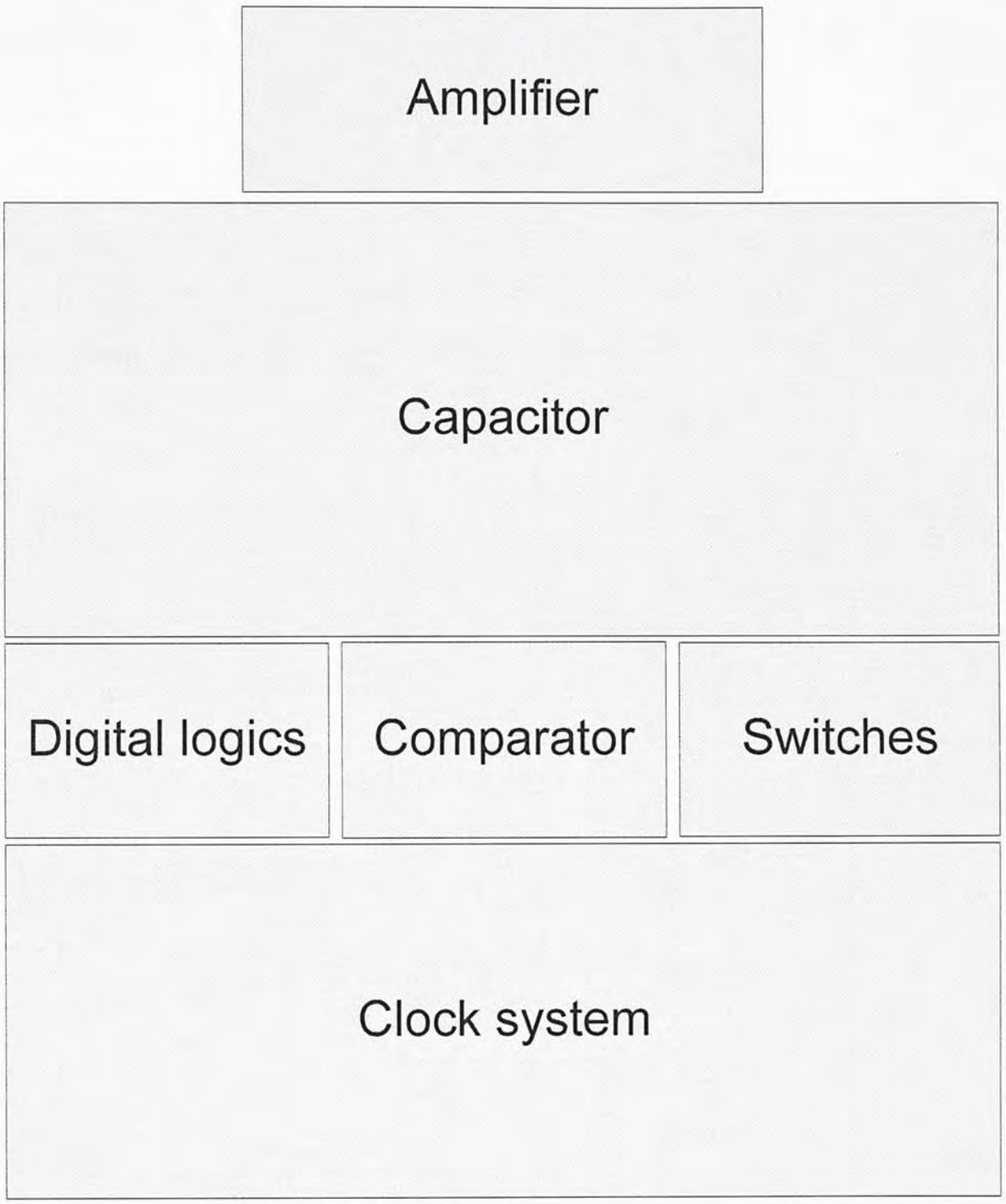


Figure 4.22: Floor planning of the layout.

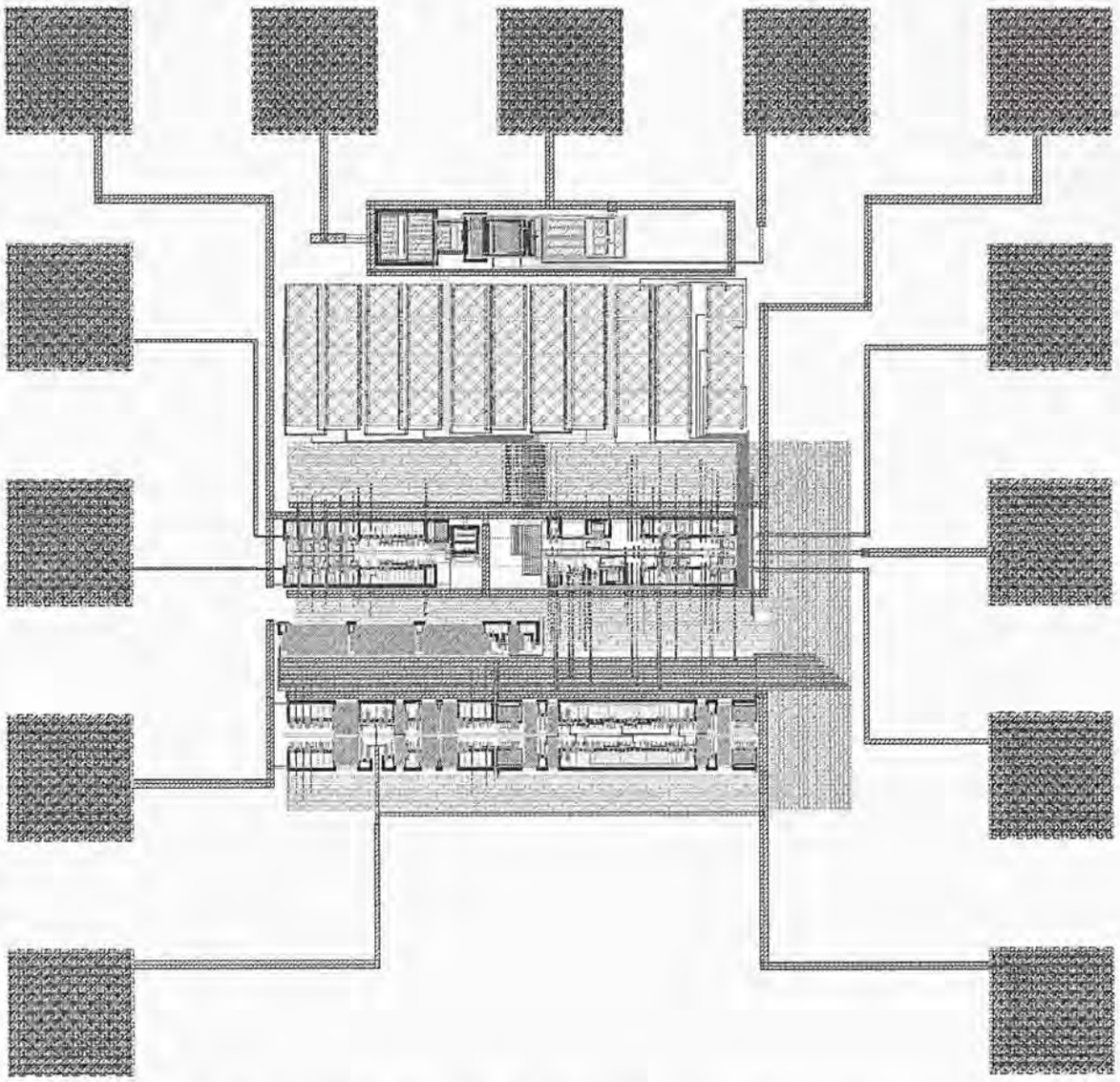


Figure 4.23: The whole delta-sigma modulator layout.

4.5 Measurement results

Figure 4.24 shows the measured signal to noise ratio and signal to noise plus distortion ratio for a 189-Hz sinusoidal input with an amplitude varying from -45dBV_{FS} to 0dBV_{FS}, where V_{FS} = 3.6$V_{pp,diff}$. The lower boundary of the input amplitude is limited by the signal generator used in the measurement. The maximum SNR achieved is 79.2dB over 1kHz signal bandwidth, recorded when the input

amplitude is -3dBV$_{FS}$. The maximum SNDR achieved is 76.3dB over the signal bandwidth, recorded when the input amplitude is -4.5dBV$_{FS}$. Based on the peak SNDR, the effective-number of resolution of this modulator is 12.4 bits, meeting our target. The projected dynamic range (DR) is 82dB. The harmonics starts to influence the SNDR when the input is large than -15dBV$_{FS}$.

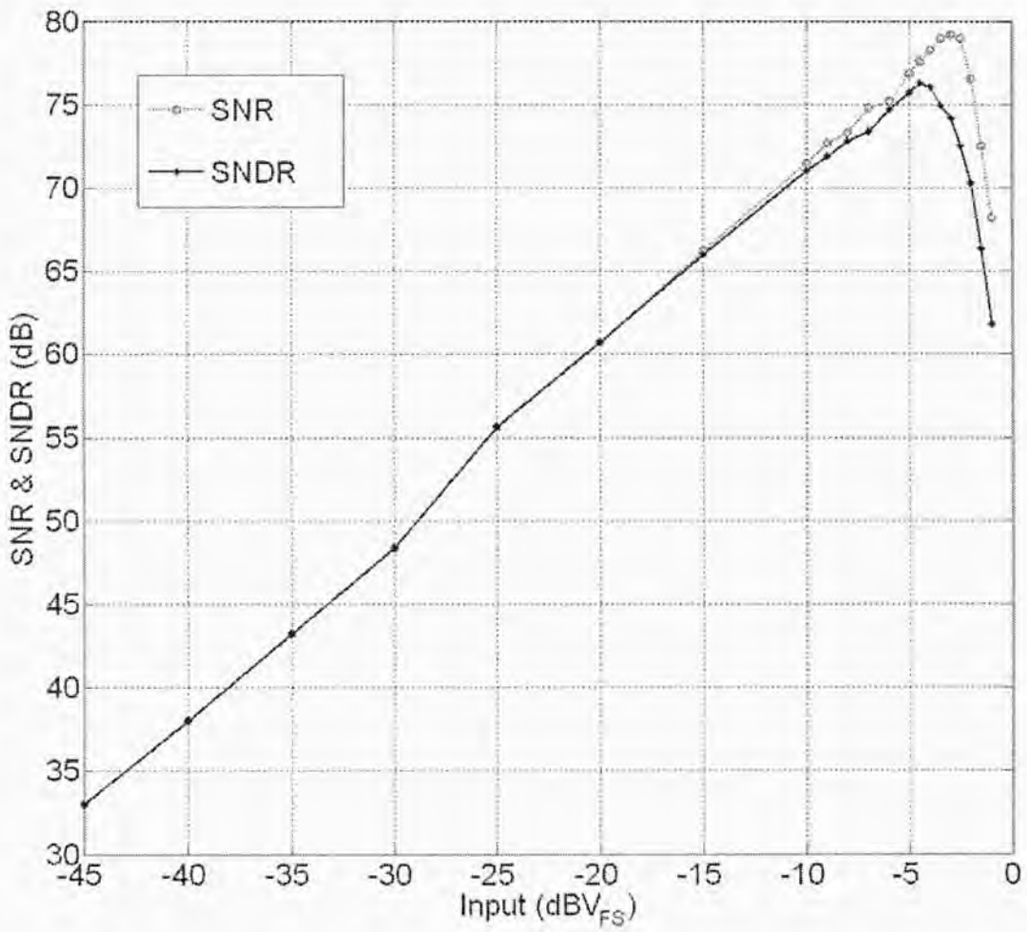


Figure 4.24: SNR and SNDR versus input amplitude for a 189-Hz sinusoidal.

Figure 4.25 and Figure 4.26 show two measured output spectra of the DSM for a 2.27V$_{pp,diff}$ (or -4dBV$_{FS}$ with V$_{FS}$ =3.6V$_{pp,diff}$) input at 189Hz and 822Hz. We used 2^{17} data points in the FFT calculation with a Hanning window, resulting in a frequency resolution of 1.95Hz. Notice that the amplitude loss due to Hanning windowing has

been compensated in the FFT calculation. Some harmonics are observed in the spectrum for the 189Hz input; the 3rd harmonic is the largest, which is -83dB to the signal. For the 822Hz-input case, the harmonics are out of the signal band, resulting in a better SNDR but almost the same SNR compared to those of the 189-Hz case (the difference between the SNRs is less than 0.3dB). From Figure 4.25, the offset value (the first frequency point in the FFT) is -73dB to the full scale of 1.8V (peak amplitude, not the peak-to-peak amplitude), which corresponds to an absolute value of 403μV. There is no visible $1/f$ noise in the output spectrum for frequency down to 4Hz. A total of 8 packaged chips available to us were measured and they have very close SNR and SNDR performance. Their offset voltages average 570μV with a standard deviation of 130μV. The chip draws 80μA from a 1.8V supply.

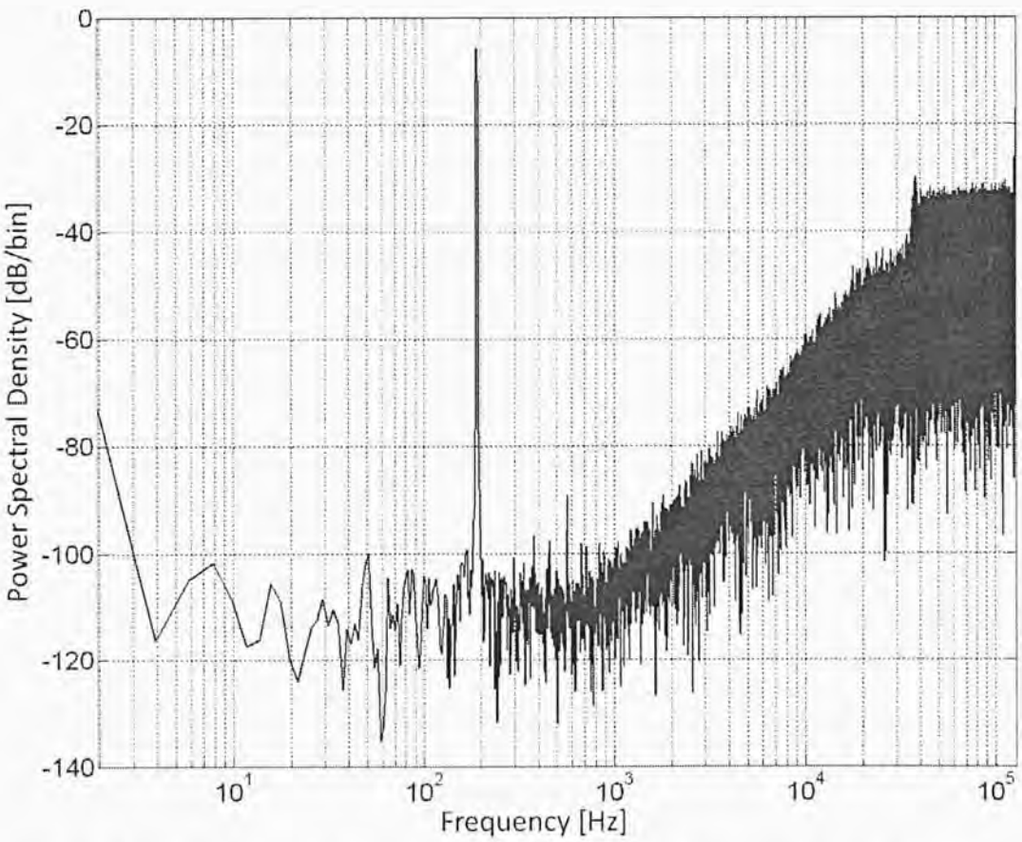


Figure 4.25: Measured output spectrum for a 2.27$V_{pp,diff}$ input at 189Hz.

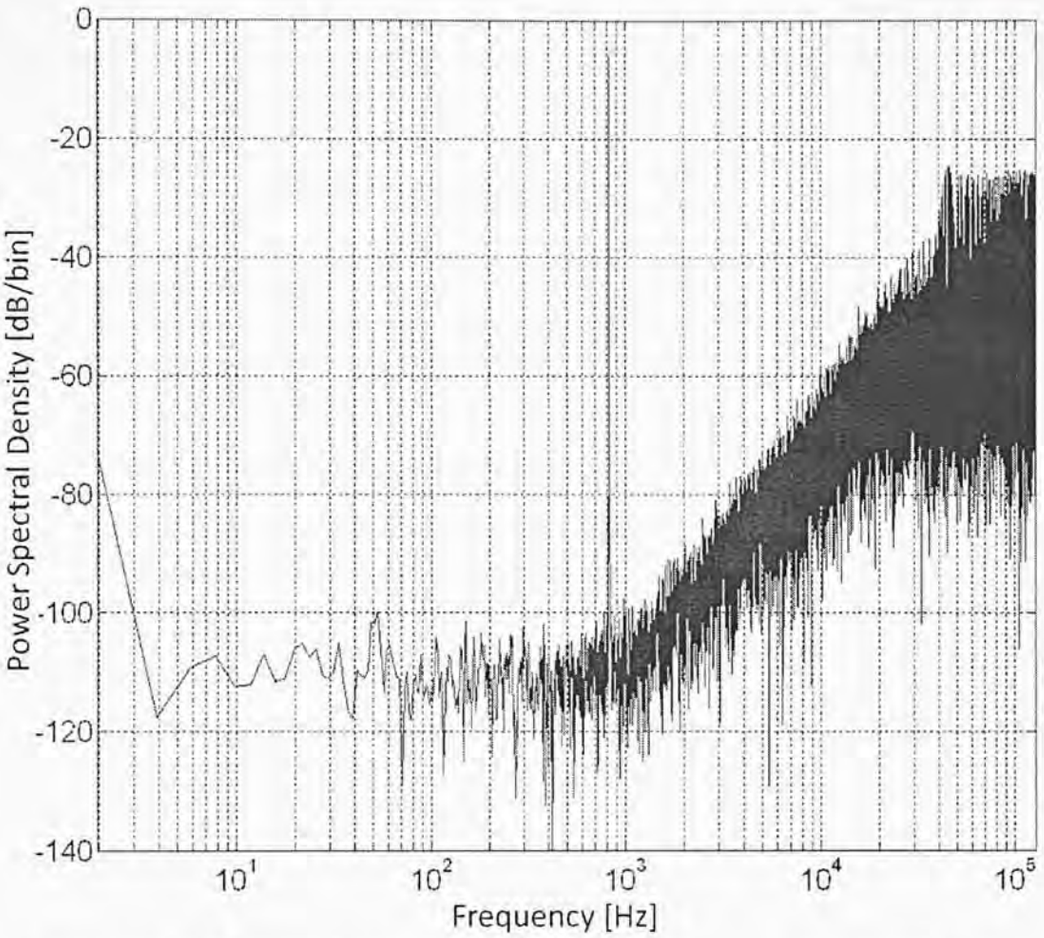


Figure 4.26: Measured output spectrum for a $2.27V_{pp,diff}$ input at 822Hz.

The measured results are summarized in Table 4.1, in the last column. The Figure-of-Merit (FoM) in the table is defined as [14]:

$$FoM = \frac{P}{2^{ENOB} * f_n} \qquad \text{Eq(4.6)}$$

where ENOB is effective number of bits and is defined in Eq(2.15), P is the power consumption in Watts and f_n is the Nyquist frequency in Hz. The FoM of this high-pass DSM is 14pJ/conversion-step. Table 4.1 also compares this work with earlier works. Since there is only one high-pass DSM (resonator based architecture) reported with measurement results (instead of only simulation results) [15], some low-pass DSMs with relatively small low-frequency noise or small offset are included

for reference. The FoM of this design is one order of magnitude smaller (the better) than that of the other high-pass DSM [15]. Furthermore, the offset achieved in this design is the best compared to reported high-pass or chopper-stabilized low-pass DSMs.

Specification \ Paper	[5]	[16]	[14]	[15]	[17]	**This work**
DSM type	LP	LP	LP	HP	LP	**HP**
Process (μm CMOS)	0.35	0.18	0.5	0.35	0.35	**0.18**
Supply Voltage (V)	3	0.7	1.2	3.3	3.3	**1.8**
Bandwidth (*k*Hz)	4	8	0.025	156	10/20	**1**
Sampling freq. (*k*Hz)	1024	1024	3.2	10000	5120	**256**
Peak SNDR (dB)	87	67	62.6	53	---/85.7	**76**
Peak SNR (dB)	92	70	66.5	59	90.7/87.3	**79**
DR(dB)	92	75	67.4	59	113.8/110	**82**
Power (μW)	950	80	0.14	42000	14700	**144**
FoM (pJ/conv.)	6.8	2.8	2.5	371	--/24	**14**
Input normalized offset* (mV)	3	22	12	1.3	1.8	**0.403**
Core area(mm^2)	-	0.082	0.6	0.9	5.7	**0.159**

* Offsets are estimated from the measured output spectrum.

Table 4.1: The comparison between this work and previous works

Chapter 5 A Low-Power Chopper-Stabilized Delta-Sigma Modulator in 1.2V 0.18μm CMOS

In this section, a low-power chopper-stabilized DSM will be introduced step by step, which includes the structure selection, system modeling and parameter selection, circuit implementation, and simulation results.

5.1 Structure selection

In this project, the DSM is constructed to deal with the instrumentation amplifier's (INA) outputs, where the input signal of the instrumentation amplifier is Electrocardiogram (ECG) signal. The main objectives are low power consumption, low flicker noise, low offset; the target resolution is 8-9 bits with the signal bandwidth 256Hz [18].

And for 8 bit resolution DSM, its corresponding dynamic range is 12*6.02+1.76=50dB. We select the loop order L=2, the quantizer bit N=1 and the oversampling ratio OSR=32, thus it can achieve dynamic range of 64dB. The additional 14dB is the margin to make sure the goal can be achieved.

The power supply in this project is 1.2V, so for a simple amplifier without cascade structure, the single-end output swing is $1.2\text{-}2V_{DS,sat} \approx 1.2\text{-}2*0.2=0.8V$, and the swing is set around 0.7V if we give some safety margins. So it needs large capacitor ratios (around 1:10) to achieve such low output swing, but large capacitor ratio may induce

large capacitor mismatch, large die area, and long settling time problems. Thus we use feed-forward technique to suppress the amplifier output with small capacitor ratio.

So we construct a second order single bit feed-forward DSM block diagram as shown in Figure 5.1, the transfer function can be expressed as:

$$Y = X + (1 - z^{-1})^2 E \qquad \text{Eq(5.1)}$$

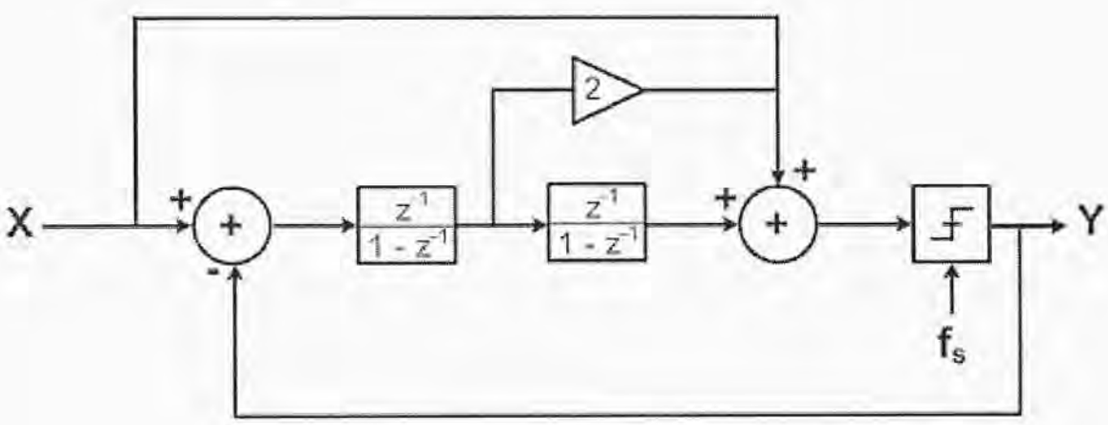


Figure 5.1: The block diagram of DSM

For this modulator is part of the ECG interception and conversion system, and the amplitude of ECG signal is in the order of micro-volt, so it needs to be amplified by several thousand times, before it is converted by the modulator. The instrumentation amplifier can amplify the signal, but if the gain of the amplifier is too high to achieve, it will consume large quantity of power. So in this project, we use the gain of DSM to relax some of the amplification specification of INA, as shown in Figure 5.2. Total system gain = gain_INA x gain_DSM.

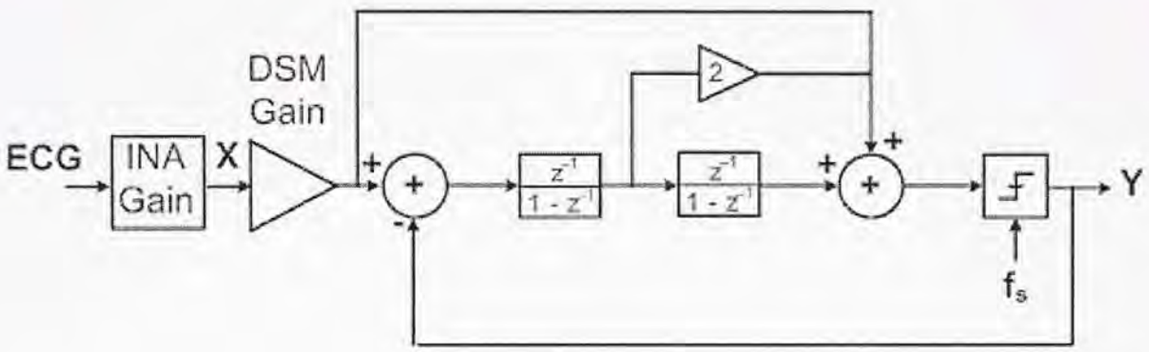


Figure 5.2: The block diagram of DSM with input gain.

As the design processes in 1st project, we start from the basic feed-forward structure in Figure 5.2, and two pairs of choppers are inserted in the front and rear ends of the first stage non-delayed integrator and the other pair of choppers are inserted in the feed-forward path, as shown in Figure 5.3(a). In this circuit we only add the chopper to the first stage of modulator, because the low frequency noises in the second stage modulator is relatively small, and also the fewer chopper pairs used, better stability and smaller area the modulator can be realized.

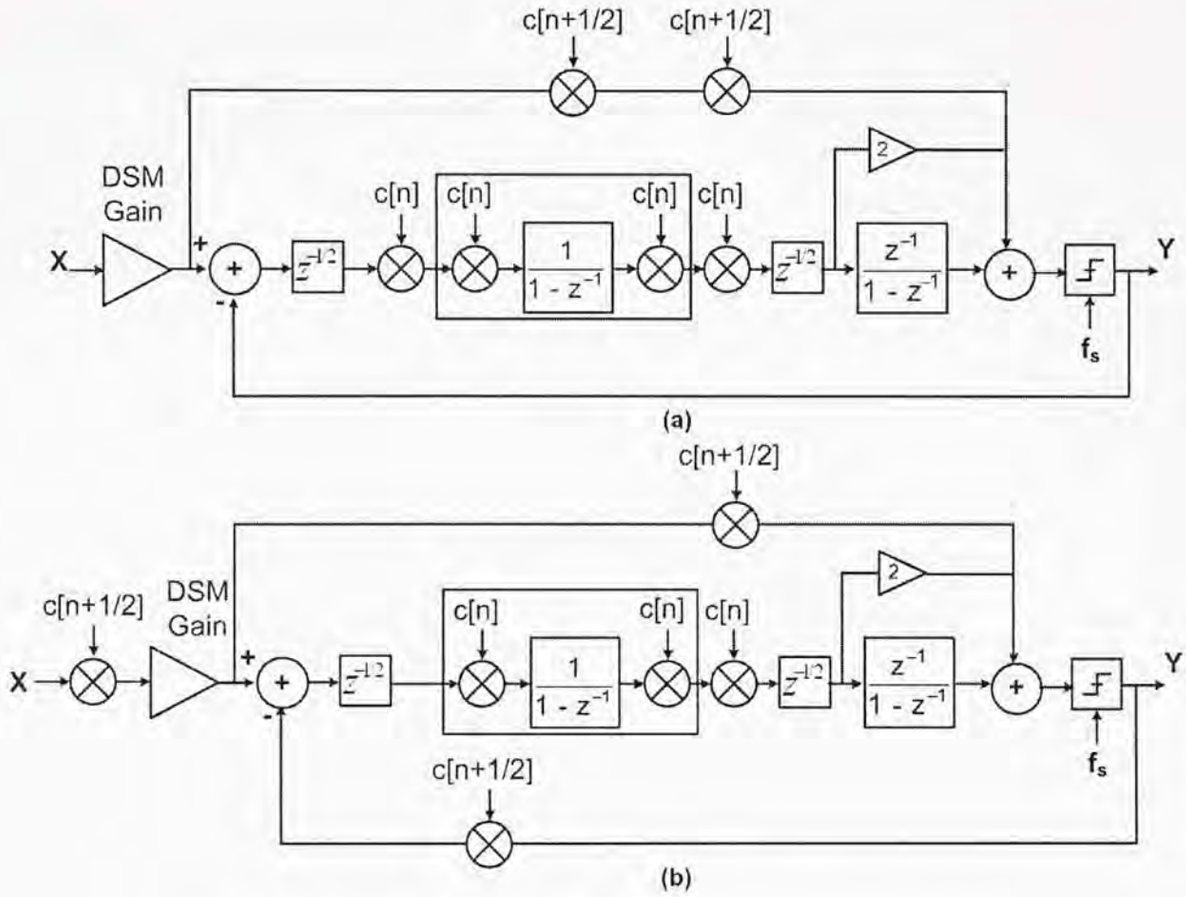


Figure 5.3: The block diagram of DSM with choppers inserted.

The insertion of choppers does not affect the STF or NTF of the modulator as two adjacent choppers null the effect of each other. Figure 5.3(b) shows the equivalent model by moving choppers backward through the signal flow direction. The relationships between chopper clocks and the main clocks Φ_1 and Φ_2 are shown in Figure 5.4. It is noticed that c[n] = –c[n-1] and c[n-1/2] = –c[n-3/2].

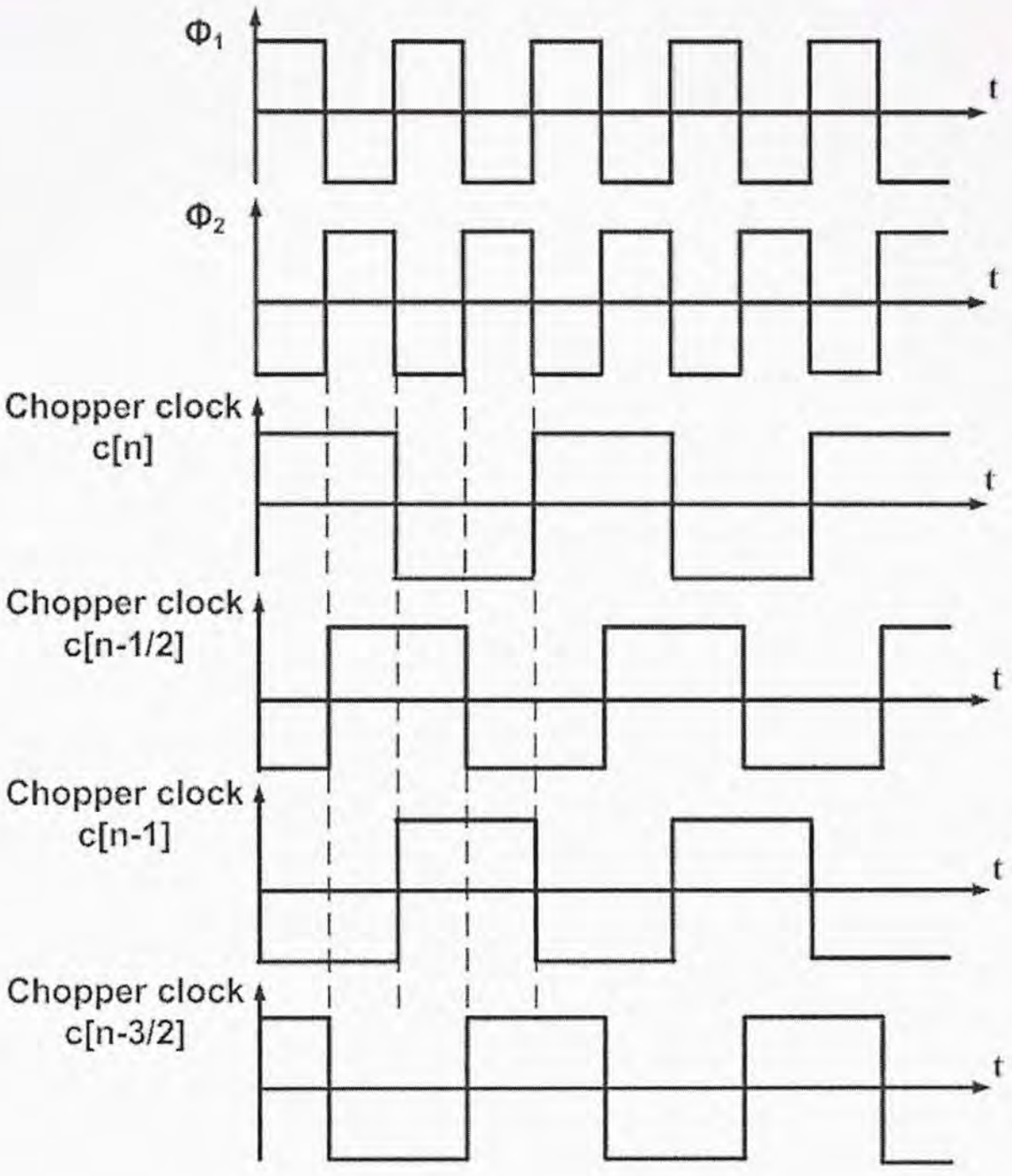


Figure 5.4: The clock relationship of the feedforward DSM

5.2 System modeling and parameter selection

In this section, we should define the value of capacitor ratio and the gain of the DSM. Firstly we should construct the block diagram as in Figure 5.3(b). In order to reduce the signal swings at integrators' outputs for improved linearity performance of

the modulator, we should scale the coefficient of DSM. Figure 5.5 shows the output swing of each integrator with -3dB input signal, the total time of x-axis is nfft*Ts, where Ts is the sampling period and nfft is the number of points selected. Because for simple current mirror amplifier, the output swing is V_{DD}-$V_{DS,SATN}$-$V_{DS,SATP}$≈1.2-0.2-0.2 =0.8 V. So the scaling factors are chosen such that the integrators' outputs have a swing less than 0.7V (give 0.1V margin). Based on system-level simulations, the capacitor ratio is set as in Figure 5.6(a).

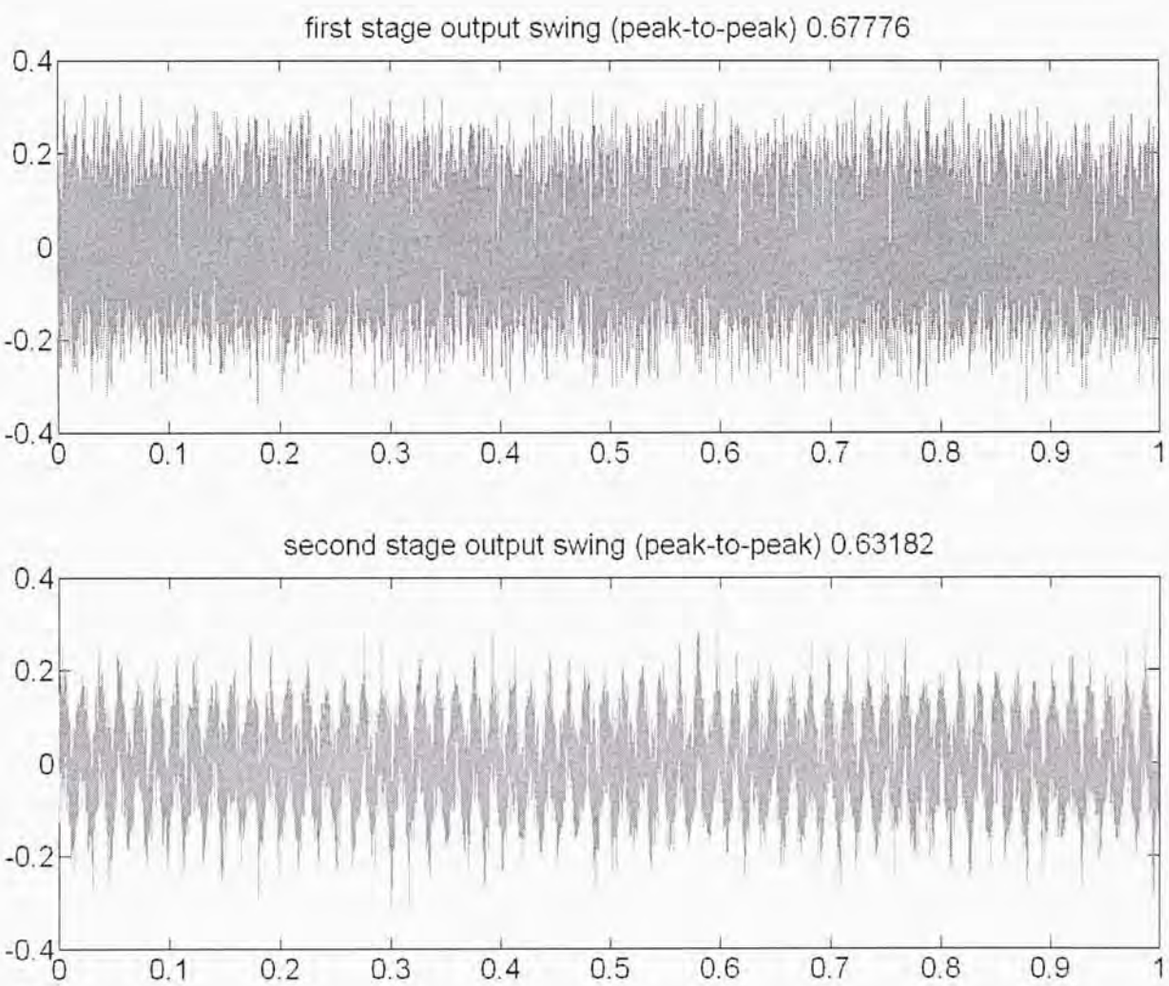


Figure 5.5: The output swing of the feedforward DSM

For the total system gain=gain_INA * gain_DSM, and in the normal condition, the ECG signal should be amplified around 4000 times before it goes into the modulator, so the product of gain_INA and gain_DSM should at least be 4000. For a DSM, if we want the input gain doesn't influence the whole circuit, we should not reduce the smallest capacitor value of the original modulator (thermal noise consideration), and should not enlarge the largest capacitor value of the original modulator (mismatch and area consideration). So in this project, we set the DSM gain to be 6, so that the INA only needs to realize the gain of around 700. Finally the scaled block diagram of the modulator is shown in Figure 5.6(b).

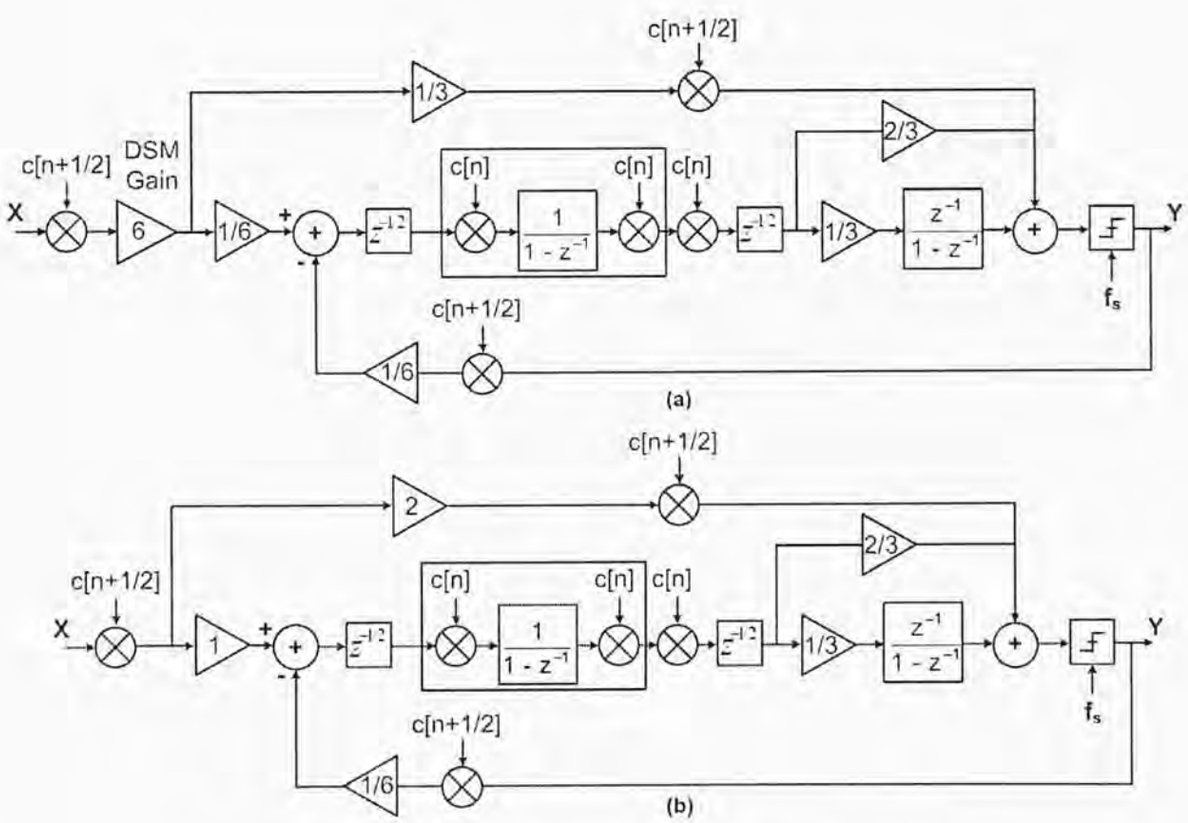


Figure 5.6: The scaled block diagram of the feedforward DSM

With the consideration of several non-ideal effects in Chapter 3, finally the output spectra spectrum is simulated as in Figure 5.7. The SNR is now 56.8dB, which is 7.3dB less than the calculated value, and this is acceptable because we introduced some small non-ideal effects when we do the simulation. And this SNR has enough margins to realize the 8 bits resolution, which is only 50dB.

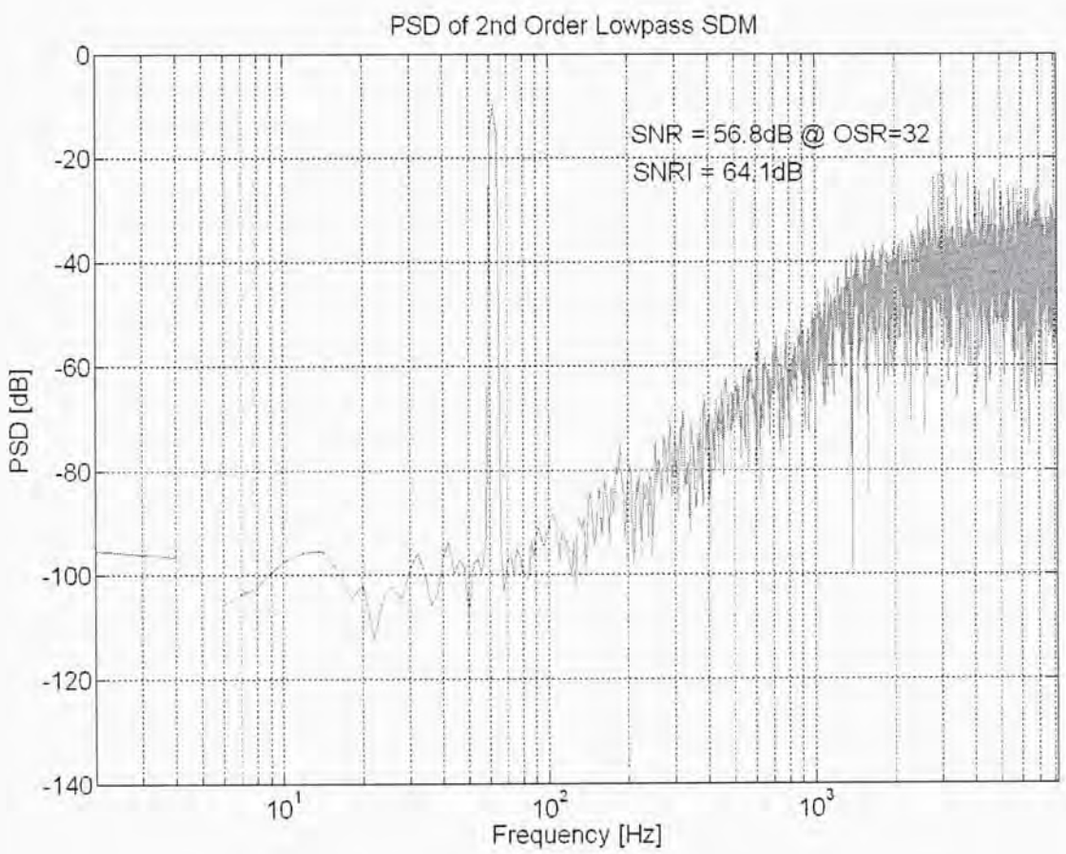


Figure 5.7: The simulation output spectra of Simulink model

5.3 Circuit implementation

5.3.1 Operational amplifier

In this project, a simple current mirror operational amplifier has been constructed

as in Figure 5.8. This amplifier has the advantages of large output swing and large unity-gain bandwidth, and it is suitable to be used if the requirements of open loop gain are not very high. The open-loop gain can be calculated as:

$$A_{DC} = K * g_{m1}(r_{o5}//r_{o7}) \qquad \text{Eq(5.2)}$$

Although the A_{DC} seems to increased by K times, we notice that the output resistances of r_{o5} and r_{o7} are decreased by K times because the current is K times larger; so the current ratio K will not change the open loop gain A_{DC}.

And the unity bandwidth frequency is

$$f_b = K * g_{m1}/2\pi C_L \qquad \text{Eq(5.3)}$$

where K is the ratio of the current mirror.

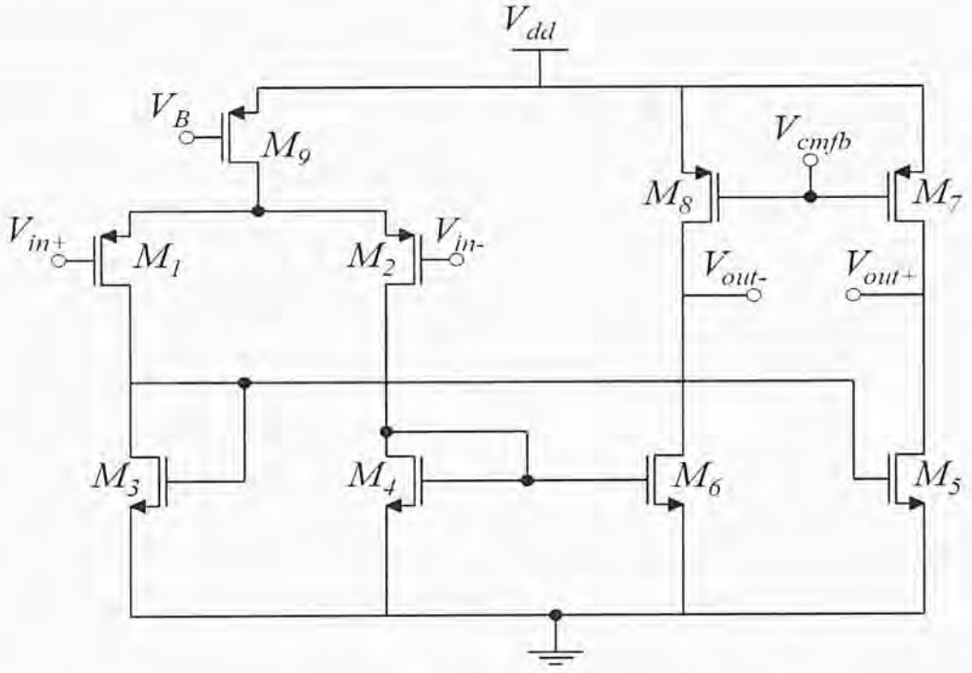


Figure 5.8: The current mirror amplifier.

And a switched capacitor common mode feedback circuit is used as in Figure 5.9. The capacitor C_s is 100fF and the capacitor C_f is 400fF. C_1 and C_2 are two

non-overlapping clocks and have the same frequency as the sampling clock.

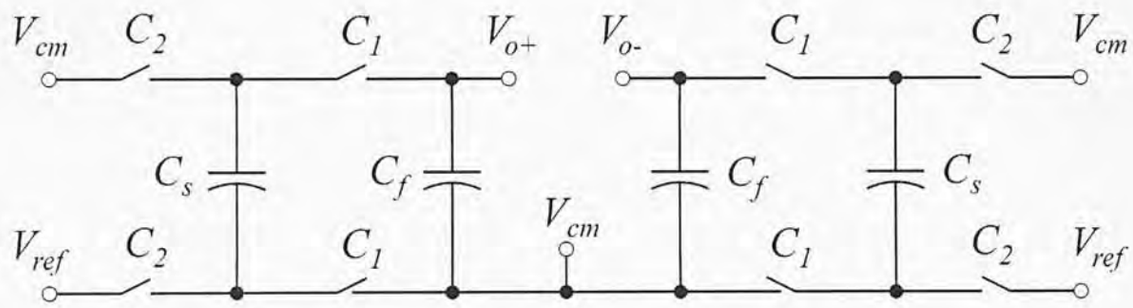


Figure 5.9: The switched capacitor common mode feedback.

The ac responses of two amplifiers in two stages, with a 500-fF loading are shown in Figure 5.10 and the summary of two amplifiers' specifications are shown in Table 5.1.

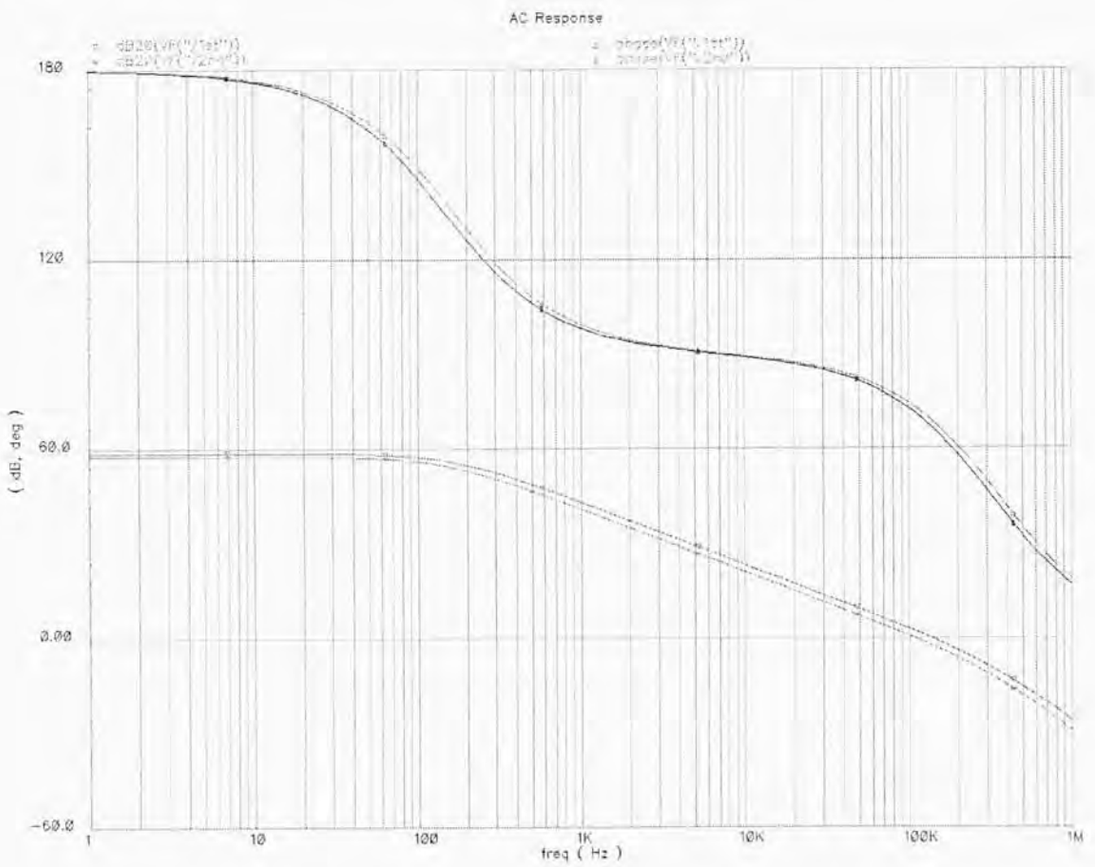


Figure 5.10: The AC response of the amplifier.

	1st stage amplifier	2nd stage amplifier
Open loop gain (dB)	58.7	57.6
Unity gain bandwidth (kHz)	134	106
Phase margin (degree)	69.1	71.5
Loading (fF)	500	500
Total current (nA)	249	188

Table 5.1: The summary of two amplifiers' specifications

5.3.2 Quantizer

The quantizer used in this modulator is the same as the one in Section 4.3.2.

5.3.3 Large delay generation

In this feed-forward delta sigma structure, after the second stage, it needs to sum the feed-forward signal and second stage output; the settling time required for this process is about 5μs, (CV=It, C is several hundreds fF, maximum V is 1.2V, I is about 100nA), then we can give some margin times and compare the final sum with 7.6μs delay, which is 1/8 of the sampling period. The relationship between the delay clock and the sampling clock is shown in Figure 5.11.

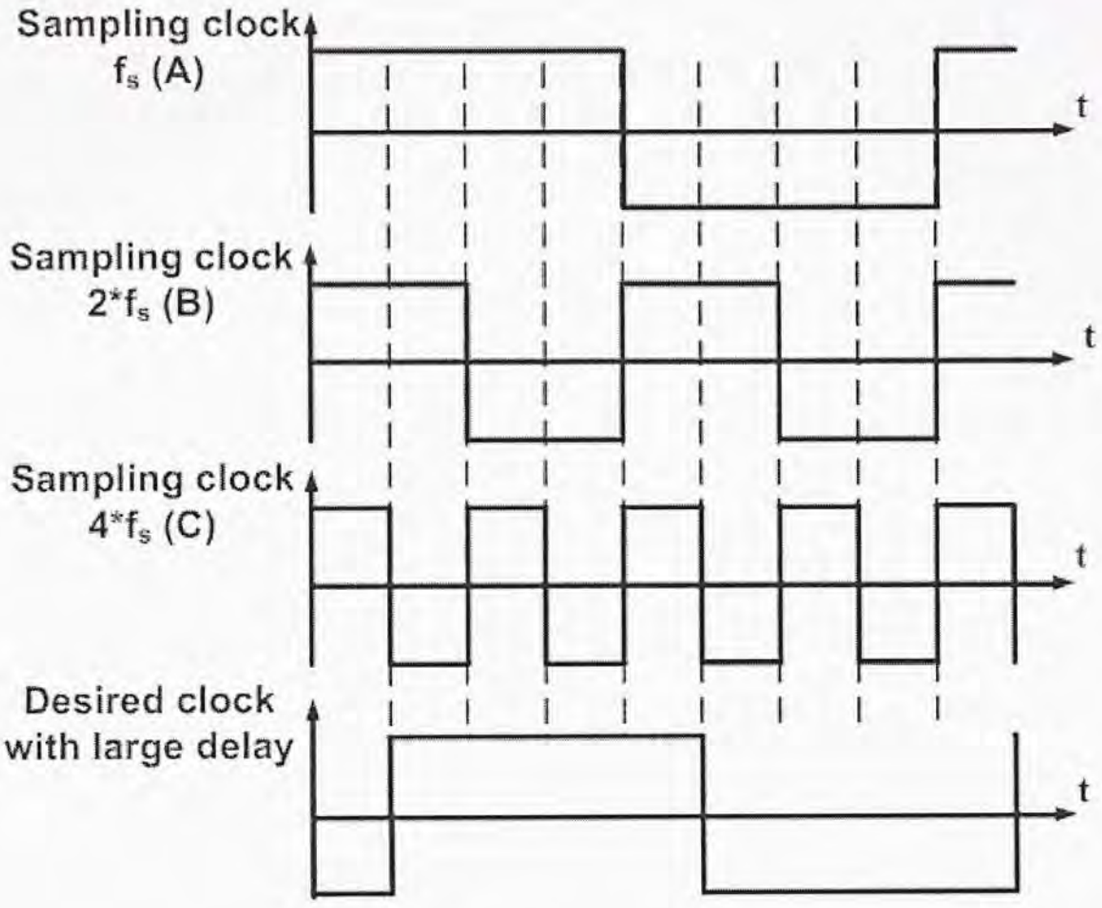


Figure 5.11: The delay clock waveform.

The circuit to generate the large delay clock is shown in Figure 5.12. As we can see that the circuit uses some frequency divider and digital logic circuits to realize the function, the representation of the delay clock (D) with parameter clock A, B, C shown in Figure 5.11 is:

$$D = A\bar{B} + AB\bar{C} + \bar{A}BC \qquad \text{Eq(5.4)}$$

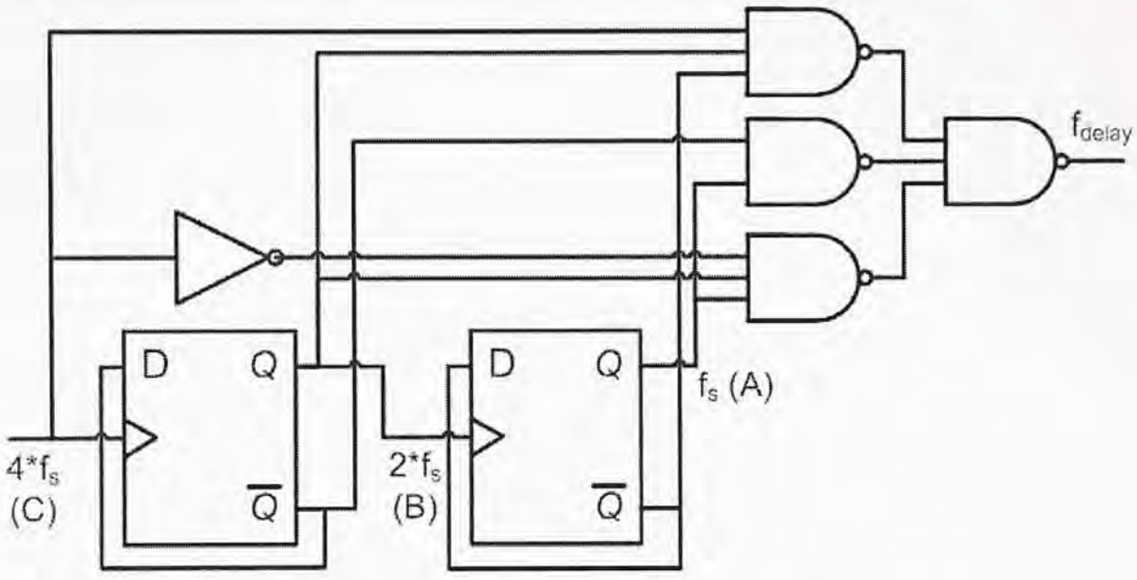


Figure 5.12: The delay clock generation circuit.

5.3.4 Overall circuit

Figure 5.13 shows the switched-capacitor implementation of the proposed feed-forward DSM (Figure 5.6). The values of the capacitors are: C_1 = 600fF, C_2 = 100fF, C_3 = 100fF, C_4 = 200fF, C_5 = 600fF, C_6 = 300fF, C_{f1} = 600fF, and C_{f2} = 300fF. So in this modulator, we control the minimum capacitor to be 100fF for the thermal noise consideration, the thermal noise limited SNR (including the amplifier's thermal noise) is designed to meet 64dB requirement, this 64dB value is the SNR of an ideal 2nd order 1-bit modulator with an oversampling ratio of 32. We also control the maximum capacitor ratio to within 6, for the matching and area consideration.

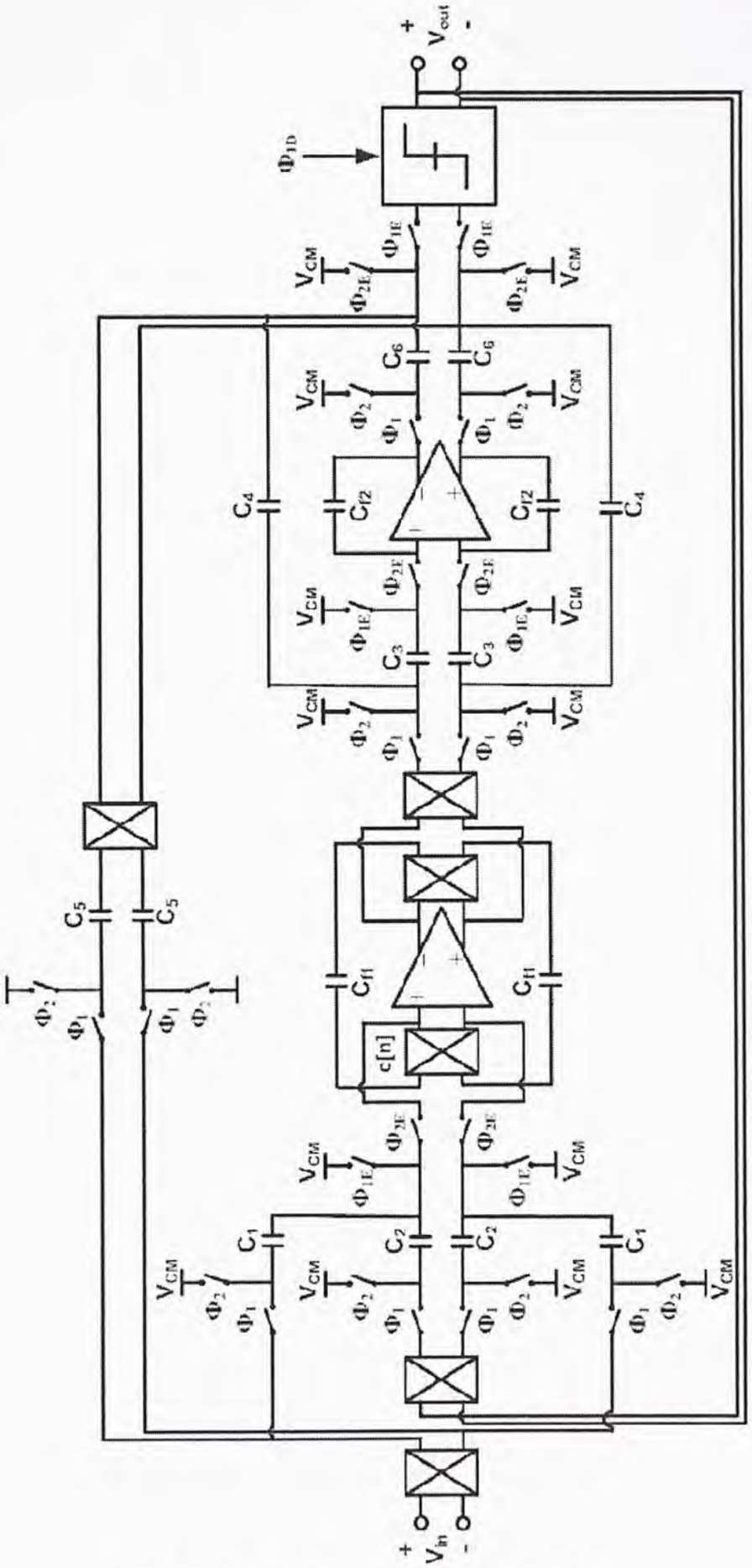


Figure 5.13: The feedforward DSM circuit

5.4 Simulation results

Figure 5.14 shows the simulation output spectrum of the feed-forward DSM for a 1.3 $V_{pp,diff}$ (or -5.4dBV_{FS} with V_{FS} =2.4$V_{pp,diff}$) input at 62Hz. We used 2^{13} data points in the FFT calculation with a Hanning window, resulting in a frequency resolution of 2Hz. From Figure 5.14, we can observe that there exists third harmonic around -70dB; this third harmonic can be accepted because our desired SNR is only 50-56dB. This modulator draws 682nA from a 1.2V supply.

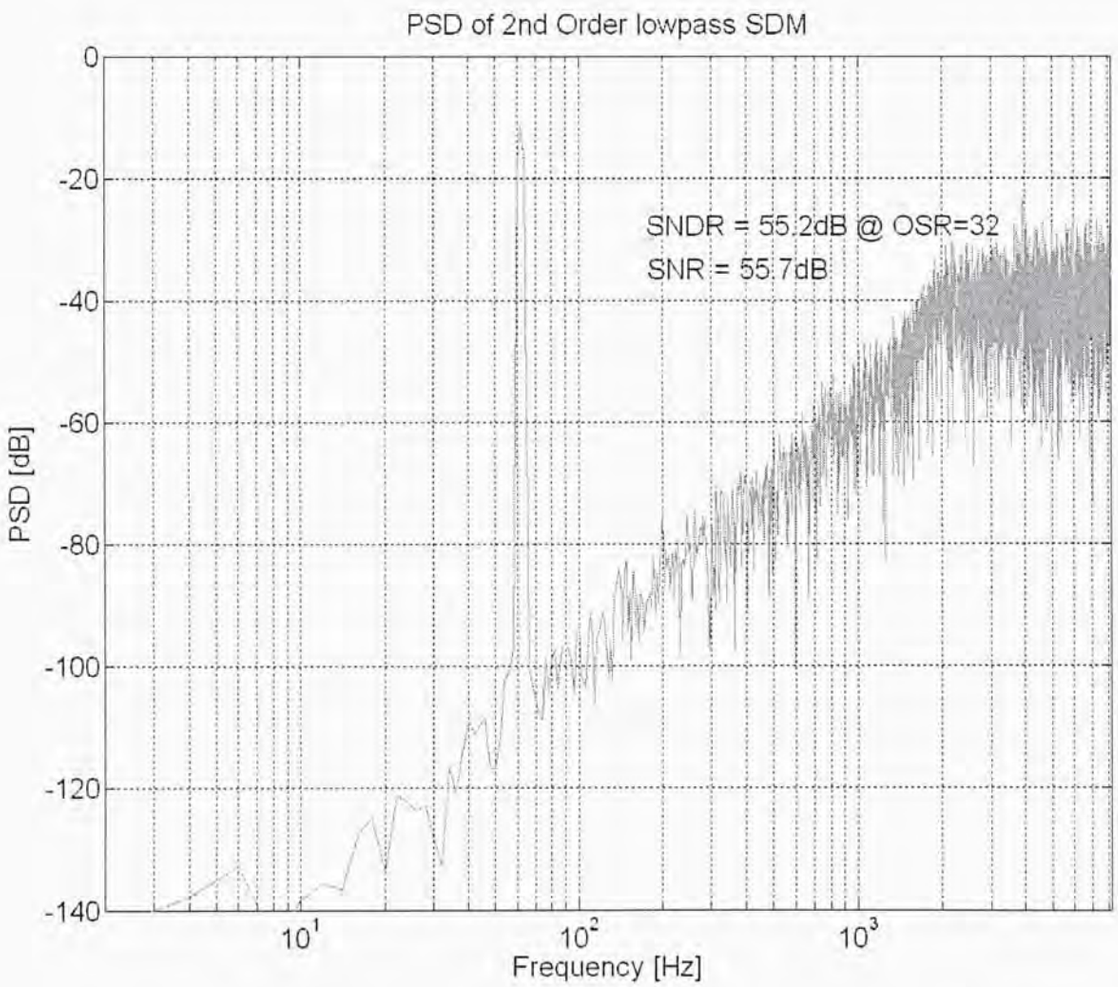


Figure 5.14: The simulation output spectrum of the proposed DSM

The measured results are summarized in Table 5.2, in the last column. The Figure-of-Merit (FoM) in the table is defined as [14]:

$$FoM = \frac{P}{2^{ENOB} * f_n} \qquad \text{Eq(5.5)}$$

where ENOB is effective number of bits and is defined in Eq(2.15), P is the power consumption in Watts and f_n is the Nyquist frequency in Hz. The FoM of this feed-forward DSM is 2.7pJ/conversion-step. Table 5.2 also compares this work with earlier works and my first DSM results.

Specification \ Paper	[15]	[18]	[19]	1st DSM	**This work**
DSM type	HP	LP	LP	HP	**HP**
Process (μm CMOS)	0.35	0.8	0.5	0.18	**0.18**
Supply Voltage (V)	3.3	1.8	1.2	1.8	**1.2**
Bandwidth (*k*Hz)	156	256	0.025	1	**0.256**
Sampling freq. (*k*Hz)	10000	8.192	3.2	256	**16.384**
SNDR (dB)	53	50	62.6	76	**55.2**
SNR (dB)	59	--	66.5	79	**55.7**
Power (μW)	42000	1.8	0.14	144	**0.818**
FoM (pJ/conv.)	371	13.5	2	14	**2.8**

Table 5.2: The comparison between this work and previous works

Chapter 6 Decimation Filter Design

6.1. The whole view of decimation filter

Normally, decimation filters are implemented as two stages. The first stage is a finite impulse response (FIR filter), which removes much of the quantization noise such that its output can be down-sampled to 4 times the Nyquist frequency (8 times of bandwidth). Then the second stage defines the baseband and produces the final converter resolution. The process is shown in Figure 6.1.

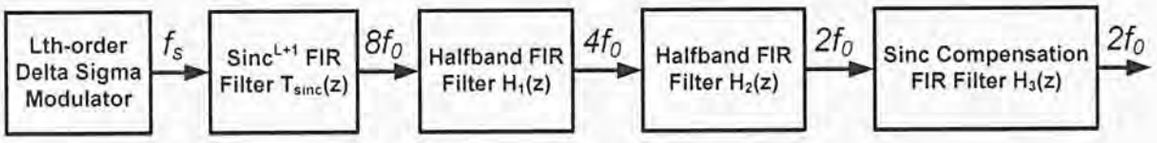


Figure 6.1: The architecture of decimation filter

There are totally 4 filters, one Sinc FIR filter, two half-band FIR filters and one compensation filter. In this project, we neglect the last filter -- compensation filter; and only consider the Sinc FIR filter and half-band FIR filter, because the function of the compensation filter is compensating the effect of sample-and-hold and giving better SNR performance, but it will not influence the main frame of the system response.

6.2. The decimation filter in Simulink

6.2.1 Sinc filter design

The cascaded integrator-comb (CIC) filter architecture is based on a type of FIR filter techniques for multi-rate applications [20], it can achieve sampling rate decrease (decimation) and sampling rate increase (interpolation) without using multipliers. $Sinc^{L+1}$ FIR filter can be represented by a cascade of L+1 filters, $T_{sinc}(z)$, where L is the loop order of the modulator:

$$T_{sinc}(z) = \left[\frac{1}{M}\left(1 + z^{-1} + z^{-2} + \cdots + z^{-(M-1)}\right)\right]^{L+1} \qquad \text{Eq(6.1)}$$

In the previous equation, M is the integer ratio and is defined as:

$$M = f_s/8f_o \qquad \text{Eq(6.2)}$$

where f_s is the sampling frequency and f_o is the bandwidth frequency.

And Eq(6.1) can be transformed to the recursive form as:

$$T_{sinc}(z) = \frac{1}{M^{L+1}}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^{L+1} \qquad \text{Eq(6.3)}$$

From Eq(6.3), we can see that this CIC decimation filter consists of two main sections; first section is the integrator section, with the cascade of L integrators with the transfer function:

$$H_I(z) = \left(\frac{1}{1-z^{-1}}\right)^{L+1} \qquad \text{Eq(6.4)}$$

The second section is the comb section, with the cascade of L combs with the transfer function:

$$H_C(z) = (1 - z^{-M})^{L+1} \qquad \text{Eq(6.5)}$$

The basic block diagram of a CIC decimation filter is shown in Figure 6.2.

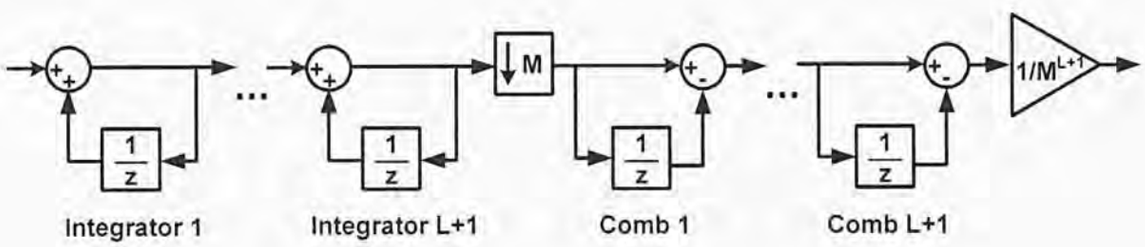


Figure 6.2: The block diagram of Sinc CIC filter.

Figure 6.3 is the corresponding Sinc filter output spectrum with the input signal spectrum the same as in Figure 5.14. Here, our sampling frequency f_s is 16384, bandwidth f_0 is 256, so after this Sinc filter, we will reduce the sampling frequency to $f_{s1} = 8 * f_0 = 2048$Hz. So M=8, filter order is equal to L+1, which is 2+1=3.

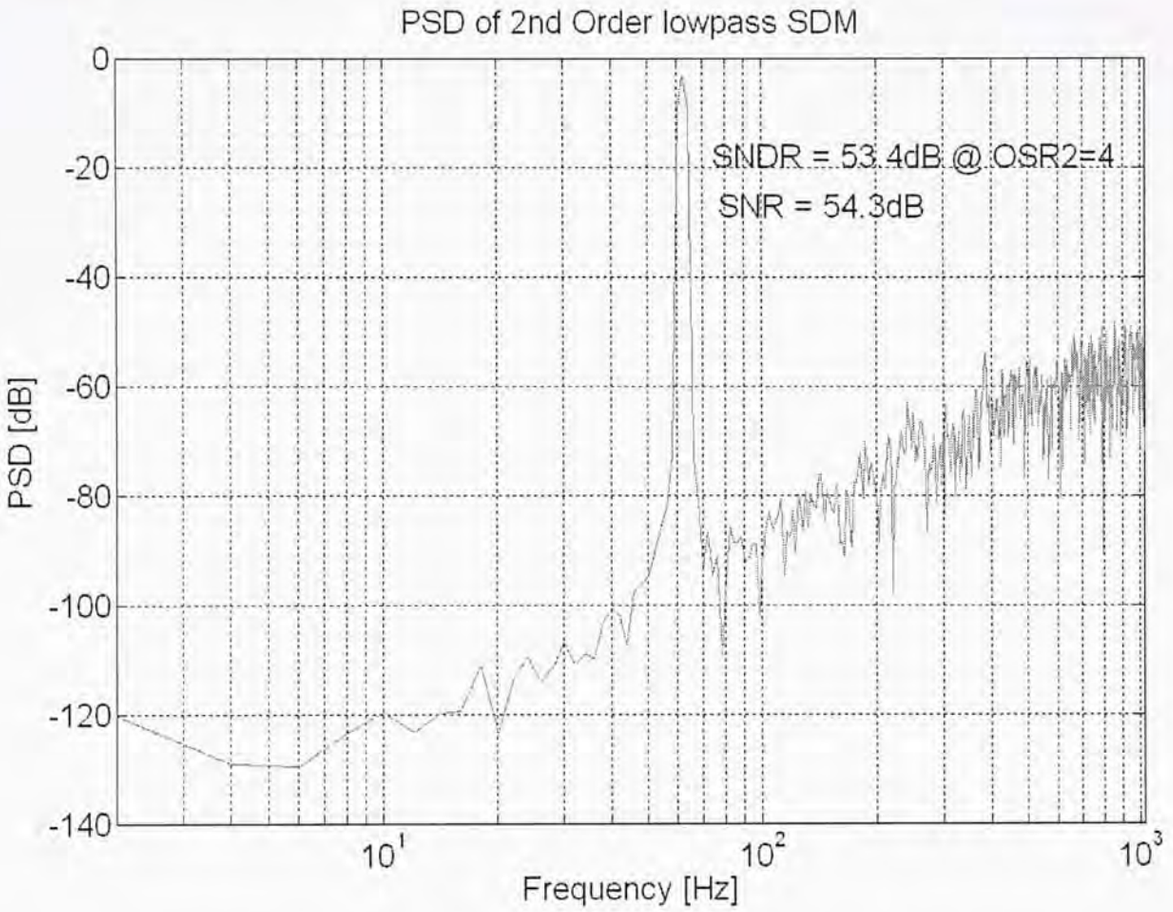


Figure 6.3: The spectrum of the Sinc filter output

6.2.2 Half-band filter design

Half-band filters are normally used when decimating by a factor of 2, which means splitting a full band signal into two equal sub-bands, since the bandwidth now is half of the initial one, the sampling rate can also be reduced by a factor of 2, as shown in Figure 6.4.

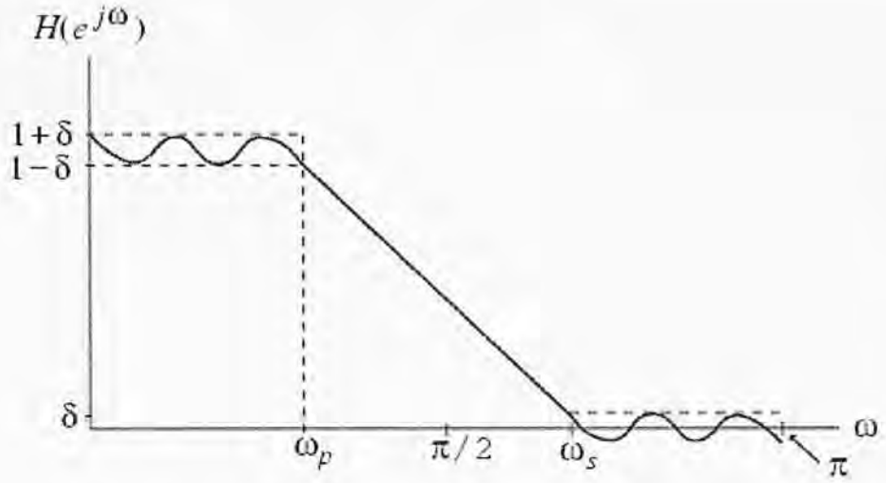


Figure 6.4: The response of typical half-band filter

From Figure 6.4, we can see that the half-band filter has some symmetry characteristics, firstly the pass-band ripple and the stop-band ripple are equal to each other, and secondly the pass-band frequency and the stop-band frequency are symmetric with respect to π/2.

These characteristics induce the most attractive property of the half-band filter, about half of the coefficients of response h[n] are zero, which reduce the complexity of the circuit.

In this project, we design two half-band filters with different bandwidth. For the 1st one, the input signal is the output of the Sinc filter, so the input sampling frequency is 2048Hz. And the 2nd one's input is just the 1st one's output, so the input sampling frequency is 1024Hz.

The Matlab codes to define the transfer function of two half-band filters are shown in Figure 6.5 [21], in this design we use the equal ripple structure of half-band filter as the response shown in Figure 6.4.

```
% ------------------------------------------------------------------
% 1st halfband filter (3) 8BW-->4BW
b1 = firhalfband('minorder', fp1, equiripple1);
[H1,F1]=freqz(b1, 1, nfft2, fs1); % freqz: frequency response of digital filter, continuous time use freqs
H1dB=20*log10(abs(H1)); % dB amplitude
figure(1)
subplot(2,1,1);
semilogx(F1, H1dB);
grid on;
axis([10 fs1 -100 0]);
xlabel('frequency (Hz)')
ylabel('gain (dB)')
Transfer1=tf(b1,1,fs2,'variable','z^-1')
numa1=Transfer1.num{1};
dena1=Transfer1.den{1};
% ------------------------------------------------------------------

% ------------------------------------------------------------------
% 2nd halfband filter (4) 4BW-->2BW
b2 = firhalfband('minorder', fp2, equiripple2);
[H2,F2]=freqz(b2, 1, nfft3, fs2); % freqz: frequency response of digital filter, continuous time use freqs
H2dB=20*log10(abs(H2)); % dB amplitude
subplot(2,1,2);
semilogx(F2, H2dB);
grid on;
axis([10 fs2 -100 0]);
xlabel('frequency (Hz)')
ylabel('gain (dB)')
Transfer2=tf(b2,1,fs3,'variable','z^-1')
numa2=Transfer2.num{1};
dena2=Transfer2.den{1};
% ------------------------------------------------------------------
```

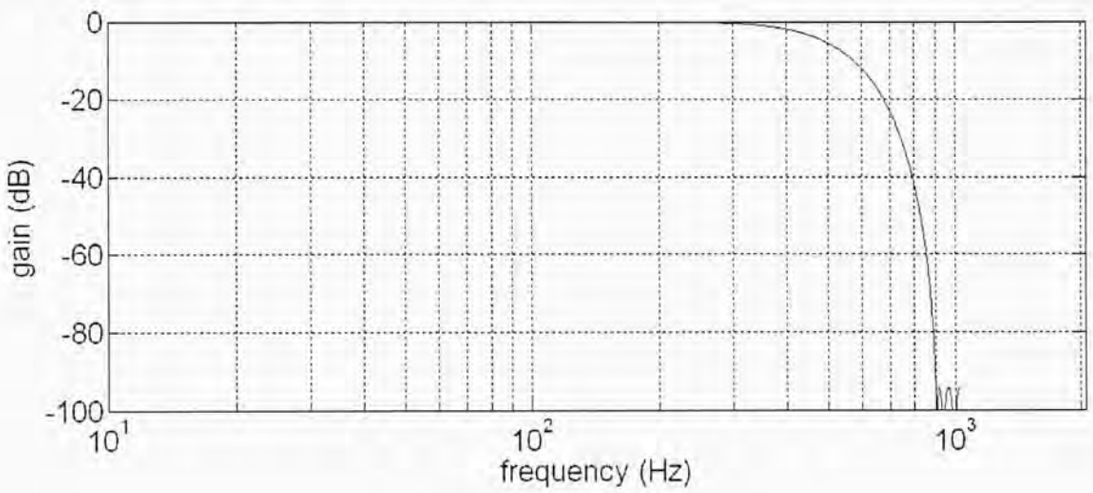
Figure 6.5: The Matlab codes to generate the transfer function of half-band filter

Then the generated transfer functions in Matlab are shown in Figure 6.6, the first half-band filter has only 10 orders, but the second half-band filter has 18 orders, from where we can see that the smaller (f_0/f_s) ratio, the higher filter order needed.

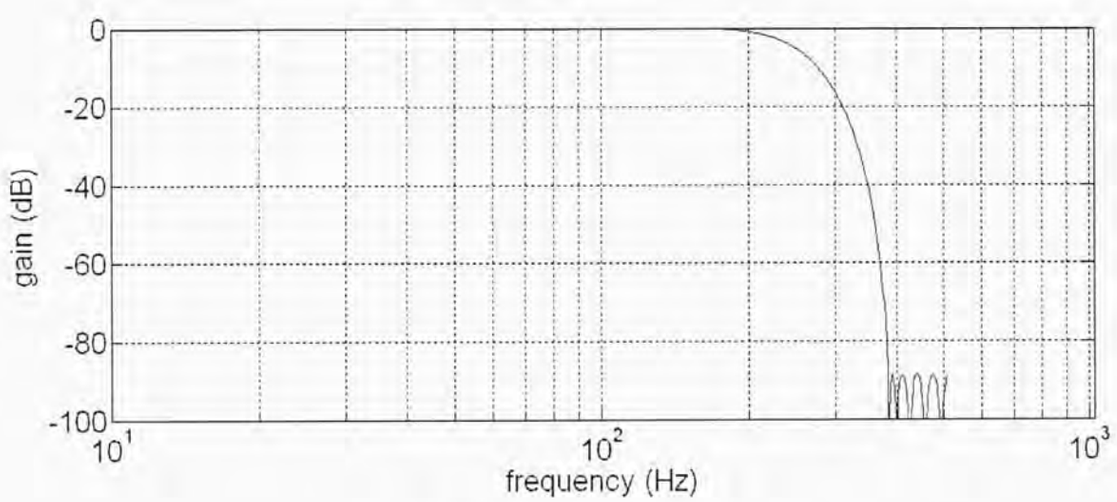
```
Transfer function:
0.007117 - 0.05231 z^-2 + 0.2952 z^-4 + 0.5 z^-5 + 0.2952 z^-6 - 0.05231 z^-8 + 0.007117 z^-10

Sampling time: 1024

Transfer function:
0.001122 - 0.007114 z^-2 + 0.0262 z^-4 - 0.07795 z^-6 + 0.3078 z^-8 + 0.5 z^-9 + 0.3078 z^-10
- 0.07795 z^-12 + 0.0262 z^-14 - 0.007114 z^-16 + 0.001122 z^-18

Sampling time: 512
```

Figure 6.6: The transfer functions of two half-band filters.

The ac responses of the corresponding two half-band filters are shown in Figure 6.7. For the 1st one, the -6dB point is 512Hz ($2*f_0$), where $f_{s1}/2 = 1024 = 4*f_0$. For the 2nd one, the -6dB point is 256Hz (f_0), where $f_{s2}/2 = 512 = 2*f_0$.



(a) 1st half-band filter



(b) 2nd half-band filter

Figure 6.7: The ac response of two half-band filters.

Then the coefficients of two transfer functions are inserted into the Simulink model shown in Figure 6.8, this model is the typical FIR structure, and we can see that there is no feedback in the model.

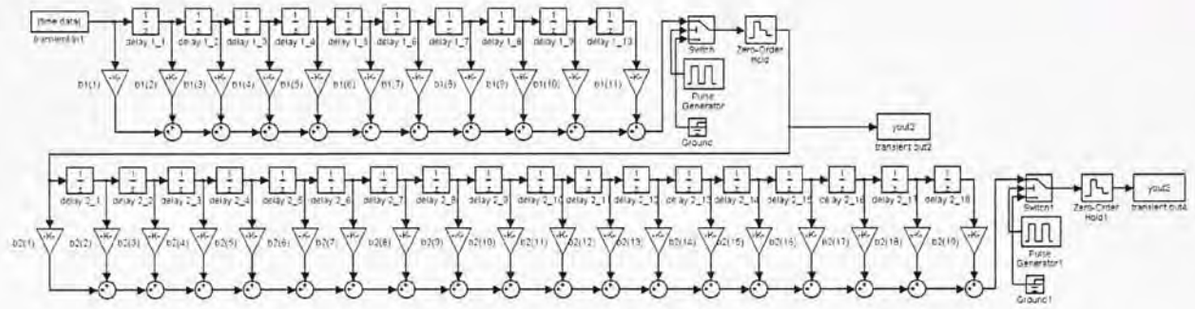


Figure 6.8: The Simulink model of two half-band filters.

Finally after input the Sinc filter's output into this model, we can simulate the 1st half-band filter's output spectrum as in Figure 6.9 and the 2nd half-band filter's output spectrum as in Figure 6.10.

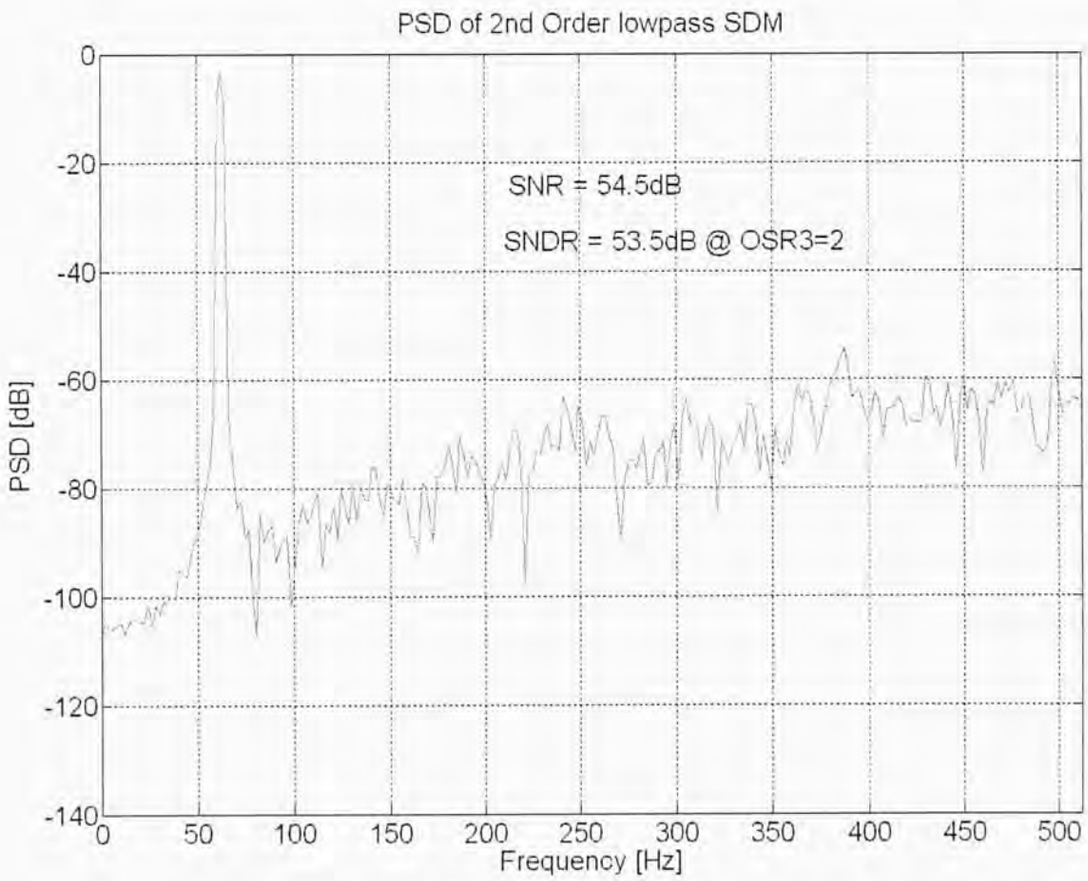


Figure 6.9: The 1st half-band filter's output spectrum.

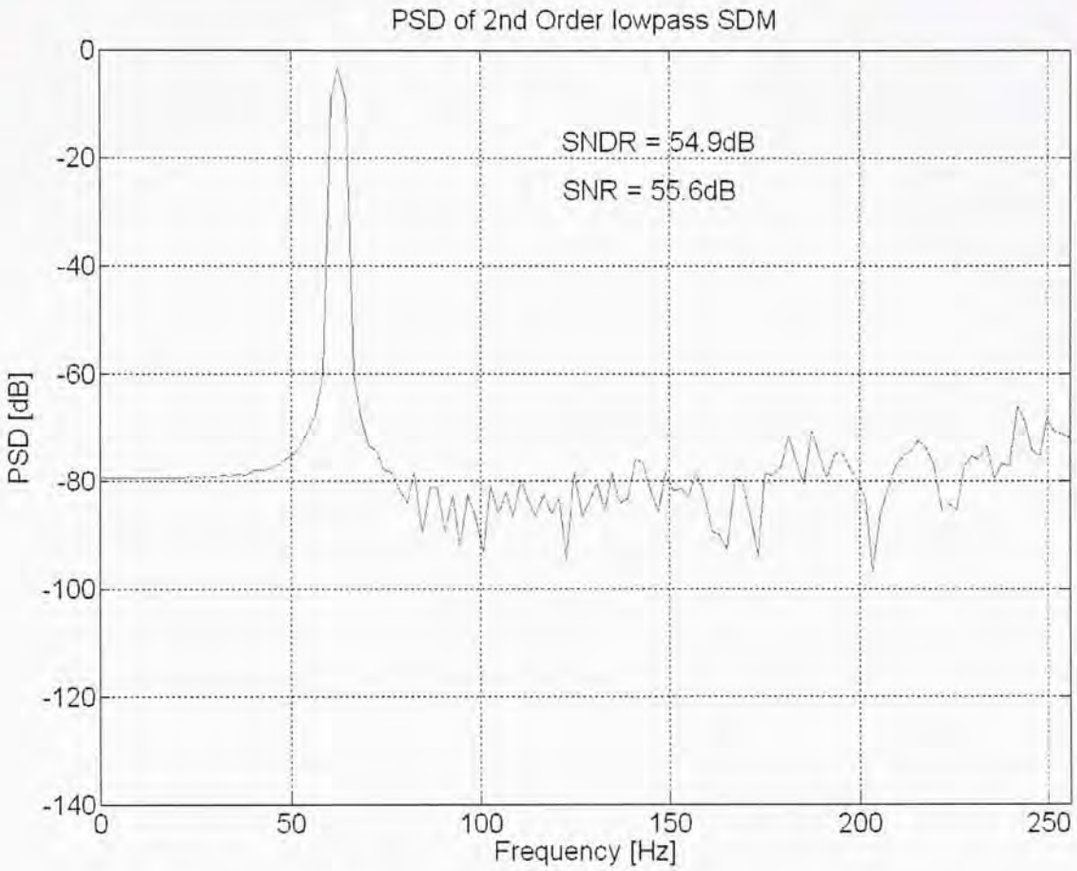


Figure 6.10: The 2nd half-band filter's output spectrum.

Chapter 7 Conclusions and Future Works

7.1. Conclusions

In this thesis, the first chopper-stabilized high-pass DSM with experimental results has been reported for reducing the offset and flicker noise of the modulator. A new circuit technique to suppress the residual offset caused by the chopper switch charge injection has been proposed. Enabled by an amplifier sharing architecture, the technique diverts the error charge from the critical chopper to the second stage of the modulator such that the error becomes first-order high-pass shaped. Fabricated in a 0.18μm CMOS technology, the 2nd order modulator achieves a DR of 82dB over a signal bandwidth of 1 kHz, and has a very low offset of 403μV and invisible 1/f noise. It consumes 144μW from a 1.8V supply.

Then in order to reduce the power consumption and improve the stability, a second chopper-stabilized DSM is proposed with simulation results. The feed-forward structure is used. This DMS also uses the high-pass structure but only involving the 1st stage of DSM in order to reduce the circuit complexity and improve the stability. Designed and simulated in a 0.18μm CMOS technology, this modulator achieves a SNDR of 55dB over a signal bandwidth of 256Hz, and has a very low power consumption of 800nW from a 1.2V supply. In theory it has no offset and 1/f noise.

Last, the design of a decimation filter in Matlab is also reported.

7.2. Future Works

In the future, some further research can be done along the direction of this work. The suggested further works are listed below.

- Further power reduction of the DSM

The portable biomedical devices need long duration and small area, and in most case, they do not need very high resolution. In our second DSM, the power consumption can be further reduced by lowering the oversampling frequency by adding the modulator loop order. Because for a second order DSM, doubling the oversampling frequency means doubling the operational amplifier's bandwidth, as a result doubling the power consumption; but adding the loop order from two to three only means to add third stage amplifier, and it will increase the power consumption by about 50%. So in the future work, we can consider reducing the oversampling frequency and increasing the loop order to realize modulator with less power.

- Fabricate and measure the 2^{nd} DSM

Although simulation results of the 2^{nd} DSM showed good performance, measurement results are the final proof of the circuit.

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