Advanced Design of Microwave Power Divider with Enhanced Harmonic Suppression

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Abstract

Currently, miniaturized and high-performance microwave circuits are in great demand for many wireless or RF applications in order to reduce the system cost. Moreover, microwave devices based on planar microstrip structure can offer many benefits over the other types of transmission line such as strip-line and waveguide, as they can easily be integrated with other planar circuits and provide a low-cost, large volume production with increased reliability.

Wilkinson power divider is one of the major passive devices used in radio frequency (RF) and microwave front-end design due to its simplicity and high degree of isolation between the two output ports. It has a wide range of applications such as the feeding network for an antenna array and the power splitting/combining networks for amplifier modules. The major drawback of the conventional Wilkinson power divider is the presence of spurious response, due to the adoption of simple quarter-wavelength transmission lines. This affects the performance of the system drastically, especially in wireless applications. In the past, the suppression of harmonic bands is usually attained by adding separate filter modules.

In the last decade, this problem has been partially overcome by using defected ground structure (DGS) or electromagnetic bandgap (EBG) cells for the suppression of one or two harmonic frequency bands. Unfortunately, these circuits usually require either backside etching or additional lumped reactive element, which is undesirable for low-cost and mass production environment. Moreover, explicit design formulas are often not available and the desired responses are mainly obtained by computer optimization.

In this research, new designs of two-way and three-way power dividers with enhanced spurious suppression have been developed and demonstrated. The proposed structures require no DGS or reactive elements, and feature low loss, readily available closed form solutions, flexible layout, enlarged suppression bandwidth, and compact size. For the purpose of verification, all designs have been fabricated using microstrip, characterized and compared with simulation results. These devices offer both power dividing capability and multi-harmonic rejection in a single design. As a result, low cost, miniaturized RF front-end may easily be implemented by the adoption of these multi-functional devices, rather than the cascaded connection of multiple modules.

摘要

目前，小型化、高性能微波電路的需求量很大，以減低無線應用中系統成本。此外，在微波器件基礎上，平面微帶結構比其他類型的傳輸線，如帶狀線和波導，有很多好處。因為他們可以很容易地與其他平面電路集成，可作低成本，具有高度可靠性的大批量生產。

由於其簡單性及兩輸出端口之間的高度隔離，在無線電頻率和微波的前端設計之中，威爾金森功率分配器是一個的關鍵設備。該分頻器具有廣泛的應用，如應用於網絡天線陣列和功率分配/結合網絡的放大器模塊。常規威爾金森功率分配器的主要缺點是雜散響應的存在，由於採用簡單的四分之一波長傳輸線。這會影響電路的性能，尤其是對無線系統。單獨的過濾器通常被用作抑制諧波頻帶。

過去的十年，這個問題已經部分克服，通過使用缺陷地面結構（分散型發電）或電磁能隙（EBG 結構）細胞，以抑制諧波的一個或兩個頻段。但是，這些電路通常需要額外的集總反應元件或背面蝕刻，這些方法不適用於低成本和大規模的生產環境。此外，缺乏明確的設計公式，所需的響應主要來自計算機優化。

在本研究中，新設計的雙向及三路功率分配器具有雜散抑制的功能，表現出理想的特性而不使用任何反應的元件，具有損耗低、明確的設計公式，靈活的設計、擴大抑制帶寬和體積小等優點。所有設計的製作，均採用了微帶，並與其仿真結果作對比，以驗證其真僞。新的設計電路同時具備功率劃分及多諧波抑制的功能。因此，低成本、小型化的射頻前端可以很容易的實施通過利用這些多功能設備，而不是串聯多個模塊。

Acknowledgement

The author would like to thank his supervisor, Dr. K.K. Michael Cheng, for his effort, guidance and inspiration throughout the process of this work. Michael is particularly tolerant with his students when making mistakes and helps them to solve problems. The author has learnt a great deal during his guidance that research is not only to focus, but also to wisely diversify his attention in work, to rest, to relax, to innovate and integrate ideas from different fields. To a practical aspect, the author would like to conclude his note of acknowledgement to Mr Li Pak Wing, who has been tremendously generous in helping out to familiarize with the ADS simulation environment, EM and layout issues, and points to note during fabrication in the dark room. Besides, the author would like to appreciate his friends who fully support his research and work.

This work is dedicated to my family.

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Chapter 1: Introduction

1.1 Research Motivation and Objective

This is a High Technology Era. Electronic devices are widely used in the community. Mobile communication devices such as portable computers and mobile phones are closely related to our daily life. The quality of electronic products increases with advances in technology. For instant, the mobile phone, from the first to the third generation, has a general decrease in its size and weight. Faster, lighter and cheaper will be the trends of electronic products. Devices with multiple functions are expected to gain even more attention in research and development. This highlights the motivation behind this work.

Power dividers and combiners are frequently adopted in various microwave applications such as the feeding network for an antenna array, the signal splitting/combining networks for power amplifying stage, mixers and frequency multipliers. It is made available both in the form of lumped-element and distributed structures. However, the major drawback of the conventional Wilkinson power divider is the presence of spurious response due to the adoption of quarter-wavelength transmission lines. If the power divider or combiner structure is able to suppress the unwanted harmonics, a separate harmonic rejection filter will then be eliminated from the microwave circuit and a compact RF-system could be implemented.

In the past, this problem has been partially overcome [1-8] by using Defected Ground Structure (DGS) or Electromagnetic Band-Gap (EBG) cells, for the suppression of one or two harmonic frequency bands. Unfortunately, these circuits usually require either backside etching or additional lumped reactive element, which is undesirable for low-cost and mass production environment. Moreover, explicit design formulas are often not available and the desired responses are mainly obtained by computer optimization [4-8]. In [1-3], modified Wilkinson divider structures based upon either shunt stub or extended line were demonstrated for third-harmonic suppression.

Moreover, these topologies only offer harmonic suppression with equal output power and no more than two output ports. The main objective of this work is to propose new types of power divider with multi-functions including unequal power division, multi-outputs, impedance transformation and enhanced spurious suppression, using standard microstrip technology.

1.2 Original Contribution

This thesis presents four new and original power divider topologies with distinctive features. These include:

1) 2-way Power Divider Design with Spurious Suppression and Impedance Transformation

- Compact size, simple structure and flexible layout
- Low insertion loss
- Enhanced stop-band attenuation (> 30 dB)
- Impedance transformation

2) 2-way Power Divider Design with Extended Spurious Suppression

- Simple structure, flexible layout and compact size
- Moderate line impedance (30 Ω - 90 Ω)
- Large fundamental bandwidth (almost 25%)
- Wide spurious suppression bandwidth (over an octave)
- Low insertion loss

3) 2-way Unequal Power Divider Design with Dual-harmonic Rejection

- Simple structure, compact size and flexible layout
- Power dividing ratio up to 4:1
- Stop-band attenuation (15 dB)
- Low insertion loss

4) 3-way Power Divider Design with Multi-harmonic Rejection

- Simple, compact structure and flexible layout
- Multiple outputs with equal power ratio
- Large fundamental bandwidth (almost 30%)
- Enhanced spurious attenuation (> 20 dB) over an octave frequency range
- Low insertion loss

1.3 Overview of the Thesis Organization

This thesis focuses on the work of advanced microwave power divider designs with harmonic suppression. It is divided into eight chapters.

The first chapter begins with a brief introduction of the research motivation and objective, followed by a list of original designs, an overview of this thesis, and concludes with a statement of the necessary assumptions and limitations for later study.

Chapter 2 briefly describes the fundamentals of power dividers such as operating principles, method of analyses, and practical limitations.

Chapter 3 reviews and compares different design approaches of conventional power dividers.

Chapter 4 describes a new 2-way power divider design with spurious suppression and impedance transformation. Design equations are derived. Electromagnetic (EM) simulations were carried out to tackle the effects of junction discontinuities. Two prototypes of power divider were fabricated and measured.

Chapter 5 presents another 2-way power divider design with extended spurious suppression. This design offers enhanced spurious attenuation (> 25 dB) over an octave frequency range with the presence of three controllable transmission zeros. Design equations are derived and verified by circuit simulation, and experimental results.

Chapter 6 discusses the design of 2-way unequal power divider with dual-harmonic rejection. Closed-form design expressions are given for the evaluation of circuit parameters. Trade-off between the line impedances and spurious response is studied. Both simulation and measurement results are presented.

Chapter 7 gives the design of 3-way power divider with multi-harmonic rejection. The number of circuit parameters to be optimized is largely reduced by analytical formulation. This design offers wide fundamental bandwidth, low insertion loss and broad upper stop-band.

Chapter 8 outlines the pros and cons of the proposed power divider designs. It leads to suggestions for future work and a conclusion of the whole thesis.

1.4 Research Approach, Assumptions and Limitations

This project focuses on the design and implementation of microwave power divider with spurious suppression. It aims at the rigorous formulation and analysis based on transmission line theory, which is carefully verified with ADS circuit models and Electromagnetic (EM) Simulation. Each design is prototyped, characterised and compared with EM simulations.

Designs are implemented on microstrip lines for low-cost, ease of fabrication and compatibility. Duroid substrate with dielectric constant of 3.38 and thickness of 0.813 mm is employed for prototyping. Two to three samples are fabricated for each design with line impedances lying between 20 Ω to 100 Ω. All the designs are realized by distributed elements, except isolation resistors in power dividers. No reactive components or backside etching are needed.

All design equations are formulated based on the assumption of lossless transmission line theory. Even-odd mode analysis is applied for the purpose of circuit analysis. The non-ideal effect of the resistors has been probed through simulations in Advanced Design Systems (ADS) with manufacturer models. Capacitive and inductive effects associated with junction discontinuities are thoroughly studied by commercially available EM tools. Demonstrations illustrate that the assumptions have been reasonably precise for the technology used.

Chapter 2: Power Divider Design Fundamentals

This chapter describes the fundamental theories of power divider that are necessary for the analysis, design and understanding of the later chapters. Topics such as Wilkinson power divider, N-way power divider and divider with unequal power split will be covered in this chapter.

2.1 Power Divider Basics

Power dividers are passive microwave components used for power division or power combining, as illustrated in Figure 2.1. In power division application, an input signal is divided by the coupler into two (or more) signals. Power dividers are often of the equal-division (3 dB) type, but unequal power division ratios are also possible. It is also required that all ports are well matched and the output ports are highly isolated.

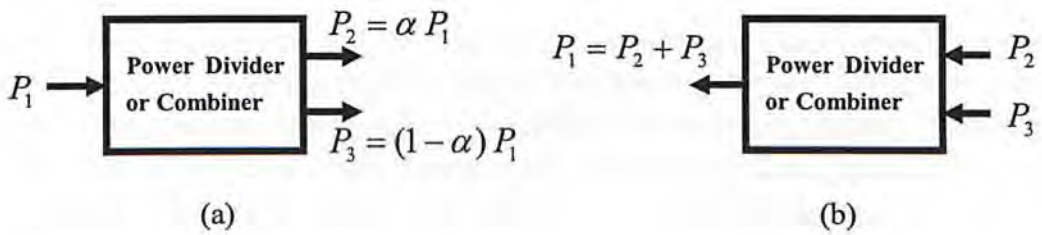


Figure 2.1 Power division and combination: (a) Power division. (b) Power combination

Two-way Power divider is either a three-port or a four-port component. Three-port networks take the form of T-junctions like Wilkinson power dividers, while four-port networks take the form of directional couplers and hybrids.

Different types of couplers and power dividers were invented and developed at the MIT Radiation Laboratory in the 1940s, mainly for the non-planar designs like E- and H-plane waveguide tee junctions, the waveguide magic-T, and various types of couplers and dividers using coaxial probes. In the mid-1950s to the 1960s, many of these couplers and dividers were redesigned using planar structure including stripline and microstrip technologies.

The earliest three port power divider known was developed by Wilkinson [9] in 1960. He presented a circularly symmetric power divider which splits a signal into N signals with equal magnitude and phase. When N = 2, this is known as the most conventional

single-band 3-dB power divider. In 1965, Parad and Moynihan [10] described a power divider that provides two in-phase isolated outputs with arbitrary signal division. Further studies were conducted to improve its bandwidth in the following years [11, 12].

A few years later, Cohn [13] introduced a type of broad-band three-port power dividers which provide perfect isolation between the two output ports and good matching in all ports. It consists of multi-section of transmission line pairs and interconnecting resistors. This paper, published in 1968, suggested that infinite bandwidth can be obtained when the number of sections and resistors is increased without limit. Ekinge [14] improved Cohn's design from the aspects of electrical length and arbitrary power split in 1971.

Multi-way power divider with equi-amplitude equi-phase was first designed by Wilkinson [9] in 1960. In subsequent years, [15-18] radial, fork, multi-section or multi-layer topologies were developed for enhanced bandwidth and reduced circuit complexity.

2.2 Wilkinson Power Divider

Before 1960, T-junctions and circular symmetric dividers were commonly used to provide multiple outputs with equal signal magnitude and phase. However, perfect isolation and port matching were not attainable by those configurations. Wilkinson is the first one to introduce a design (any number of outputs) with ideal return loss and port isolation. For simplicity, a 2-way power divider (3dB) is illustrated.

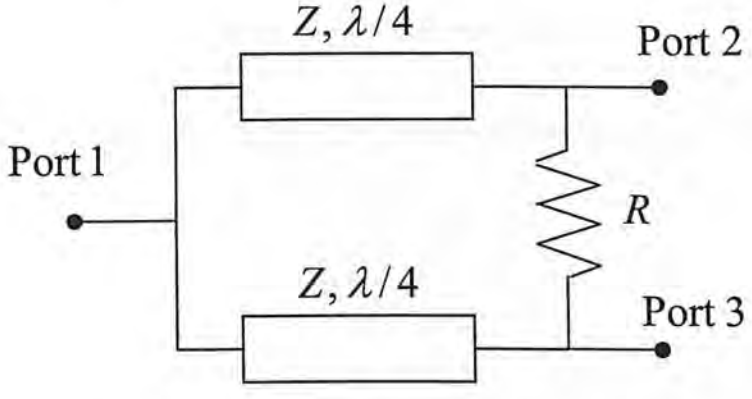


Figure 2.2 Schematic of Wilkinson power divider

Figure 2.2 shows the schematic of a Wilkinson power divider with equal output power. The even-odd mode formulation was introduced by Reed and Wheeler [19] in 1956, which is helpful in analysing symmetrical network. For analysis purposes, in phase

signals with equal amplitude are applied to port 2 and 3. The voltage difference between the upper and lower transmission lines is zero. No power is dissipated in the resistors. The circuit is split into two identical halves (Figure 2.3). The load at the input port is replaced by 2Zo as a result of bisection.

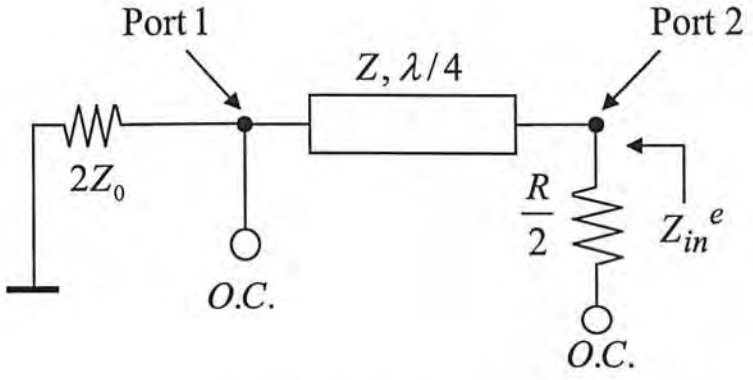


Figure 2.3 Even-mode excitation

For the odd-mode case, a pair of anti-phase signals with equal amplitude is inserted at port 2 and 3. Due to symmetry, the divider is again bisected. However, the midpoints of the resistor and the input junction are now replaced by a virtual ground (Figure 2.4).

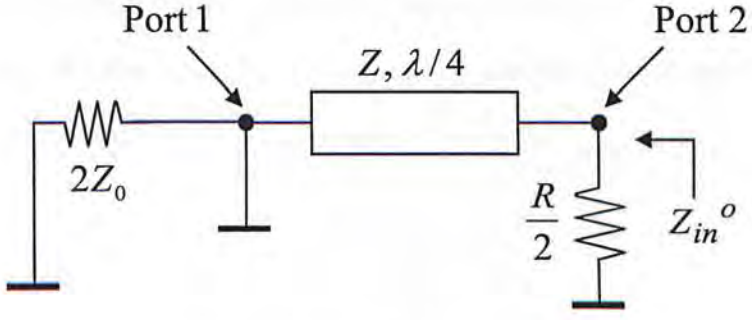


Figure 2.4 Odd-mode excitation

For perfect port matched ($S_{11} = S_{22} = S_{33} = 0$) and isolation ($S_{23} = 0$), we have

$$Z_{in}^{e} = Z_0 \tag{2.1}$$

$$Z_{in}^{o} = Z_0 \tag{2.2}$$

$$Z = \sqrt{2}Z_0 \tag{2.3}$$

$$R = 2Z_0 \tag{2.4}$$

The idealized frequency response of Wilkinson power divider is shown in Figure 2.5 for easy reference.

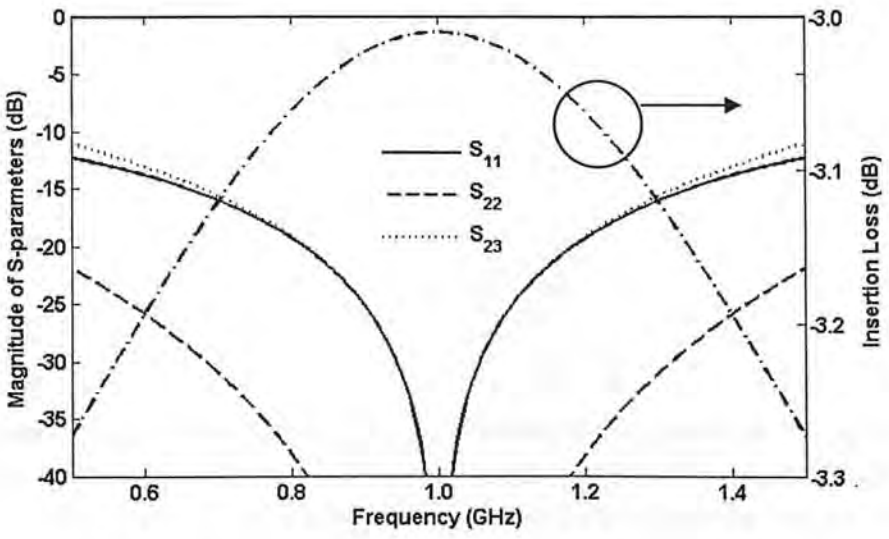


Figure 2.5 Frequency response of a typical 3dB Wilkinson power divider

2.3 Power Divider with Unequal Power Division

Wilkinson power dividers can also be made with unequal power splits (Figure 2.6). With the assumption that $K^2 = \frac{P_3}{P_2}$, we have

$$\frac{R_2}{R_3} = \frac{Z_{02}}{Z_{03}} = K^2 \tag{2.5}$$

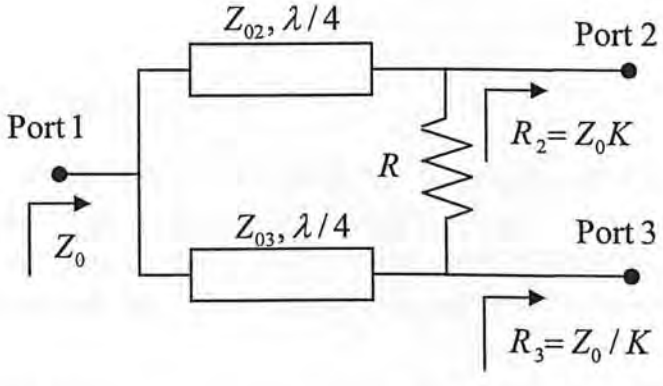


Figure 2.6 Wilkinson power divider with unequal power division

Using the even-odd mode analysis, the design equations are simply given by:

$$R = \frac{1+K^2}{K} Z_o \tag{2.6}$$

$$Z_{02} = Z_0 \sqrt{K\left(1+K^2\right)} \tag{2.7}$$

$$Z_{03} = Z_0 \sqrt{\frac{1+K^2}{K^3}} \tag{2.8}$$

Quarter-wavelength transformers may be introduced to transform the unequal load impedances (R_2, R_3) to Z_0. A quarter-wavelength transformer may be placed [10] at the input port (Figure 2.7) to further improve the bandwidth of the divider. The major drawback of these topologies are the extreme branch-line impedances involved when $K^2 > 2$.

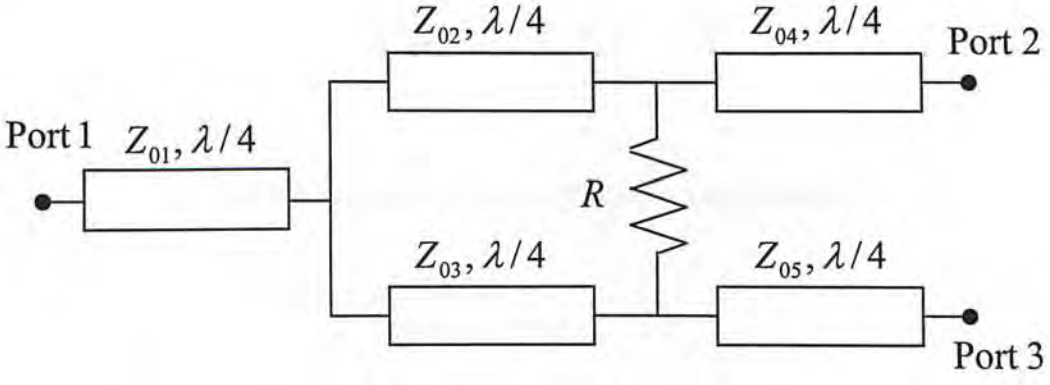


Figure 2.7 Broadband unequal power divider

2.4 Multi-way Power Divider

Multi-way power dividers and combiners are frequently used in the design of microwave and mm-wave systems. In the following section, several multi-way power divider designs like radial, fork, multi-section and multi-layer will be briefly discussed. Some planar design of 3-way power divider will also be covered.

2.4.1 *Wilkinson N-way Hybrid*

The *N*-way power divider was first introduced by Wilkinson [9] in 1960. The design maintains phase and amplitude equality between any numbers of outputs (independent of frequency) and provides good input/output matching as well as output port isolation. Figure 2.8 shows the schematic diagram of the power divider and Figure 2.9 presents its 3D structure.

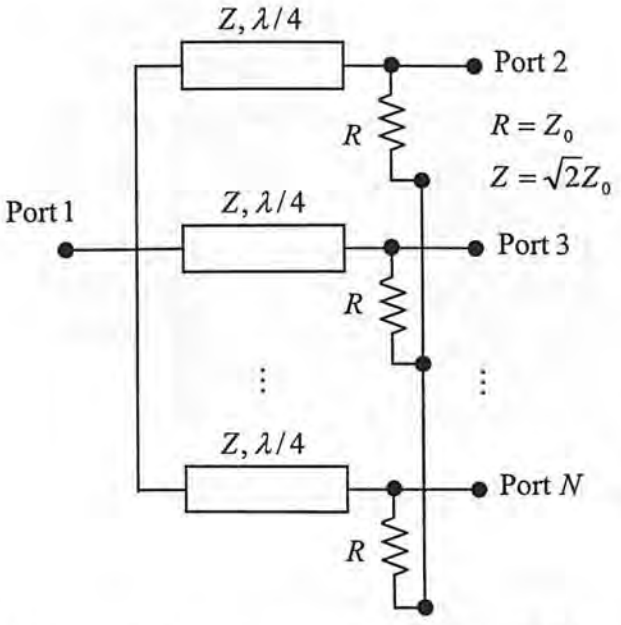


Figure 2.8 Equivalent circuit of Wilkinson N-way Hybrid

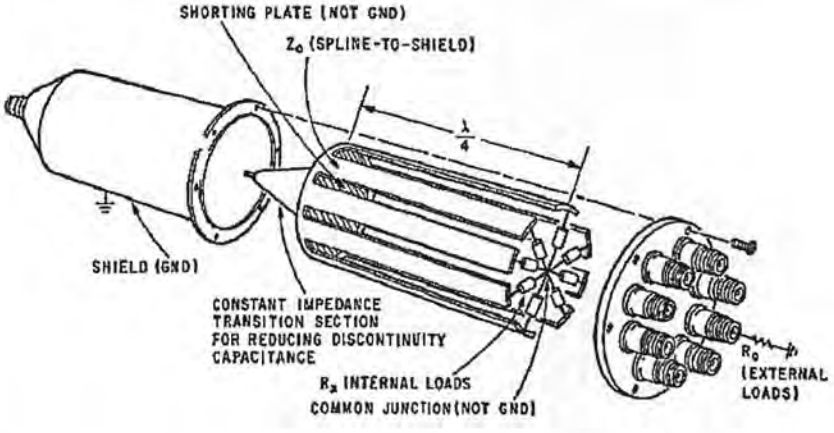


Figure 2.9 3D shape of Wilkinson N-way Hybrid

The power divider consists of *N* quarter-wavelength transmission lines and isolation resistors. Those resistors are connected from the end of the *N* transmission lines to a common junction (floating), which lead to a non-planar design. Yee [20] combined the ideas of Wilkinson [9] and Cohn [13] to obtain a broadband *N*-way hybrid power divider. However, the design is still non-planar in structure.

2.4.2 *Radial Hybrid*

The radial *N*-way hybrid was introduced in the last 1970s [21-23]. It is semi-planar in structure, low-loss and electrically symmetric. Figure 2.10 and 2.11 show the structure of the radial hybrid and its schematic diagram. The input port is assumed to terminate in Z_C and the output ports are each terminated in Z_d.

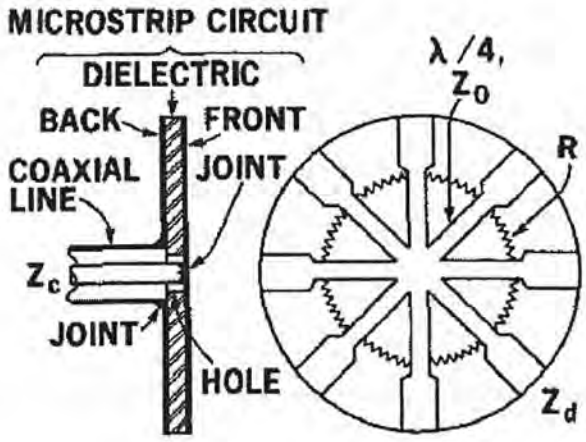


Figure 2.10 The radial *N*-way hybrid power divider/ combiner

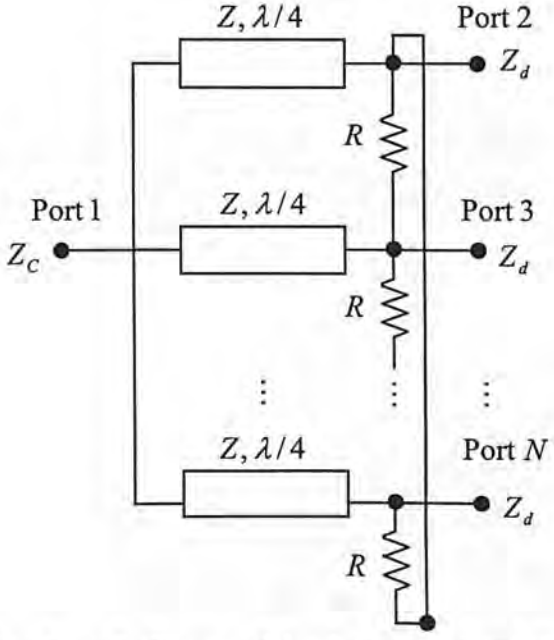


Figure 2.11 The schematic diagram of the single-stage radial *N*-way hybrid

Unlike the Wilkinson hybrid, the match and isolation of the radial cannot be made perfect, even at the centre frequency. No closed-form solutions are available for the evaluation of characteristic impedances and the isolation resistances. Saleh [16] developed the design formulas and tables for optimum match and isolation at the centre frequency for radial hybrids employing one or two stages of quarter-wave lines and isolation resistors (i.e. M = 1 or 2).

2.4.3 *Fork Hybrid*

The fork hybrid was first invented by Galani and Temple [17]. Figure 2.12 and 2.13 shows the structure of fork hybrid and its schematic diagram, respectively. The input and output ports are assumed to be terminated by Z_C and Z_d, respectively.

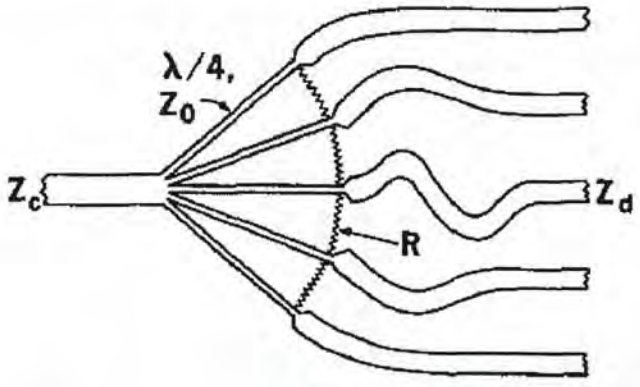


Figure 2.12 The fork *N*-way hybrid power divider/ combiner

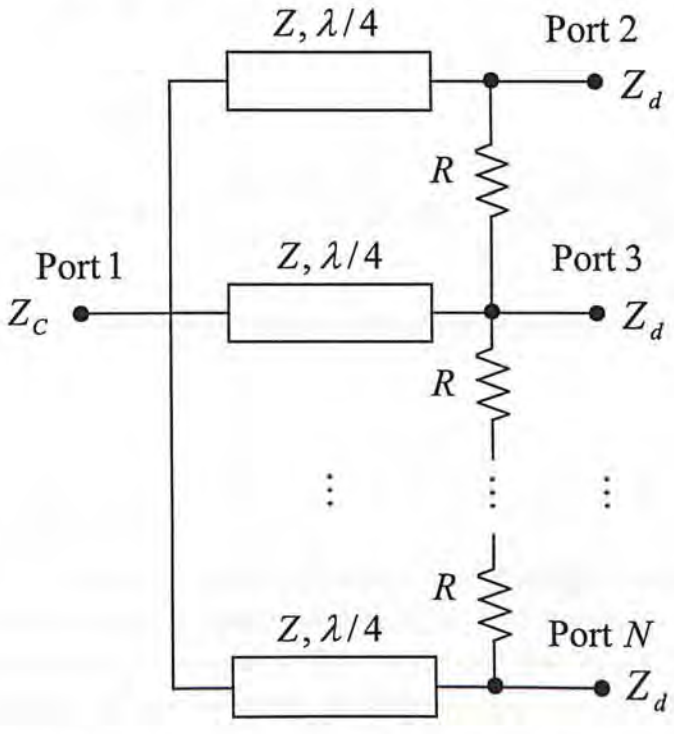


Figure 2.13 The schematic diagram of the single-stage fork *N*-way hybrid

Unlike the radial hybrid, this design is completely planar in structure, but the matching and isolation at the output ports are degraded accordingly. Acceptable performance is often obtained by computer optimization.

N-section Hybrid

The fork hybrid power divider can be further developed into multi-section structure. The schematic diagram of an M-stage fork hybrid power divider is shown in Figure 2.14. It was stated in [15] that *N*-1 stages are needed to obtain perfect match and isolation for a divider circuit with *N* output ports. Saleh [16] derived the design equations and tables for optimum match and isolation at the centre frequency for M = 1 or 2. The general design for broadband operation can be obtained by optimization.

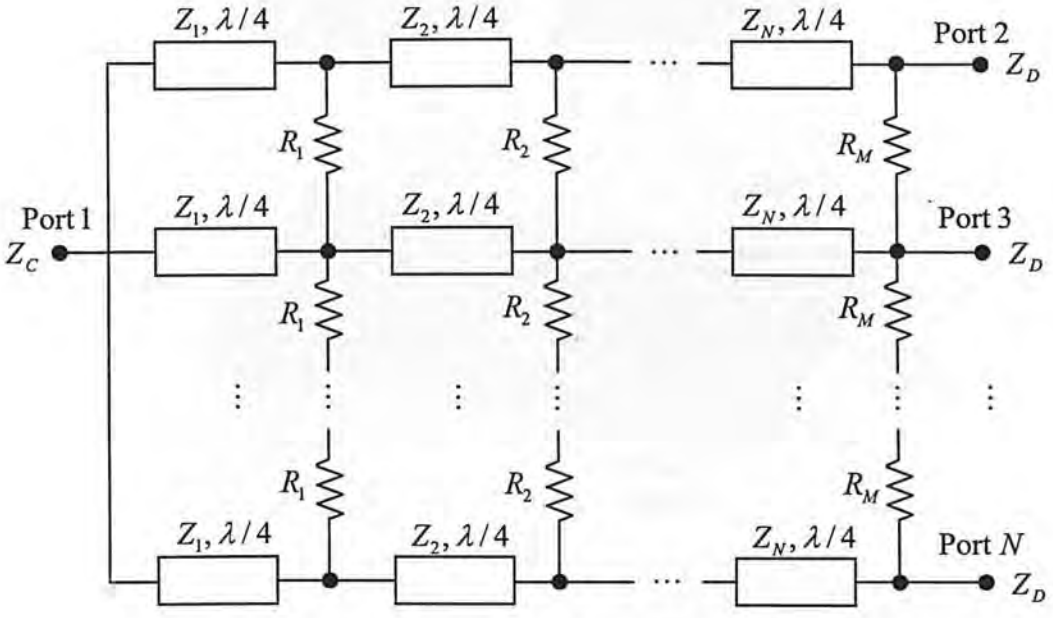


Figure 2.14 The schematic diagram of the M-stage fork *N*-way hybrid

2.4.4 Multi-layer Approach

A compact UWB three-way power divider was proposed recently [18]. The configuration of the divider is shown in Figure 2.15. It consists of five conductor layers interleaved by three dielectrics. The input and one of the output ports are located at the mid layer of the structure. While the other two output ports are at the top and bottom layers. The second and fourth layers are the ground plane with the coupling slots. The coupling patches and slots are elliptical in shape. The two isolated ports have no output power. They are terminated by a matched load to absorb any reflected power from the output ports.

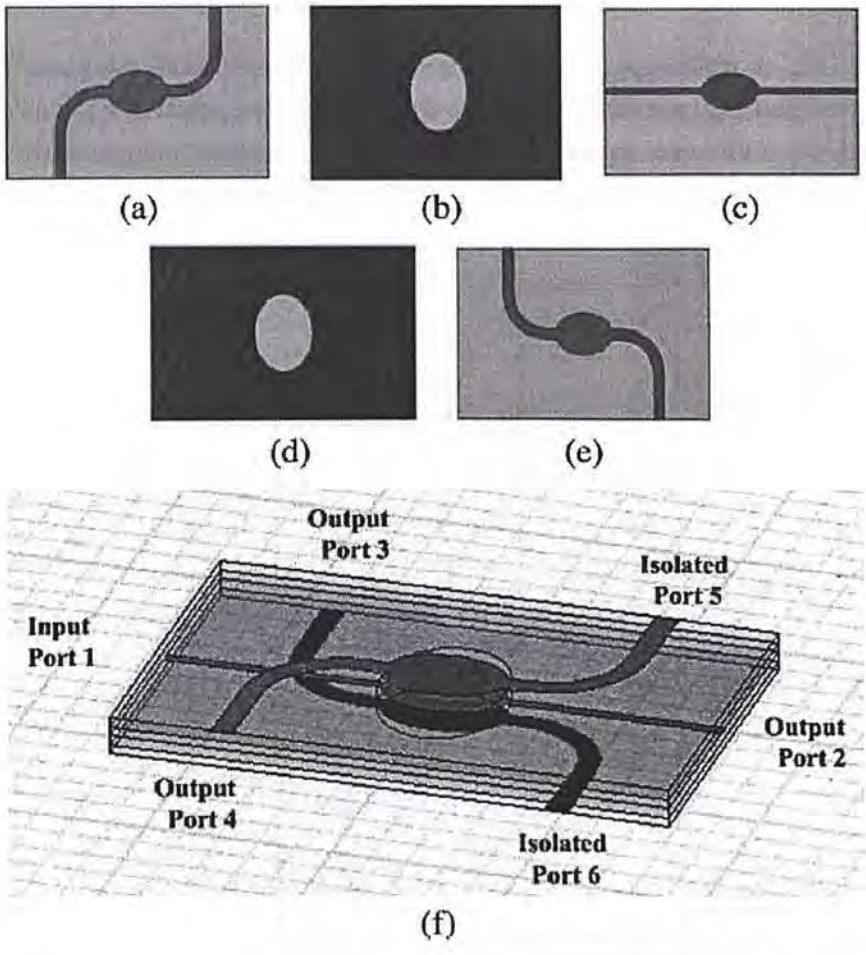


Figure 2.15 Configuration of the three-way power divider: (a) top layer, (b) second layer (ground with coupling slot), (c) mid layer, (d) fourth layer (ground with coupling slot), (e) bottom layer, and (f) the whole configuration.

The even (Z_{oe}) and odd (Z_{oo}) mode characteristic impedances for each of the coupled patches are calculated using the following equations:

$$Z_{oe} = Z_o\sqrt{\frac{1+C}{1-C}}; \quad Z_{oo} = Z_o\sqrt{\frac{1-C}{1+C}} \tag{2.9}$$

where Z_o is the characteristic impedance of the input/output ports of the coupler. Assuming $Z_o = 50\ \Omega$ and $C = \sqrt{1/3}$, then $Z_{oe} = 96.5\Omega$ and $Z_{oo} = 25.9\Omega$.

Dimensions of the elliptical patches and slots calculated from design formulas were derived using conformal mapping technique. Optimization through EM solver is needed to obtain the final dimensions of the coupler. Its main disadvantage is the need of multi-layer substrate, which increases the complexity of the fabrication process and thus the fabrication cost.

2.4.5 *Power Recombination Concept*

The power recombination concept was first introduced by Goldfarb in 1991 [24]. This topology was used to design a planar power divider containing odd number of output ports with either equal or unequal power division. Design equations can be derived through even and odd mode analysis. Figure 2.16 shows the general topology for a recombinant device.

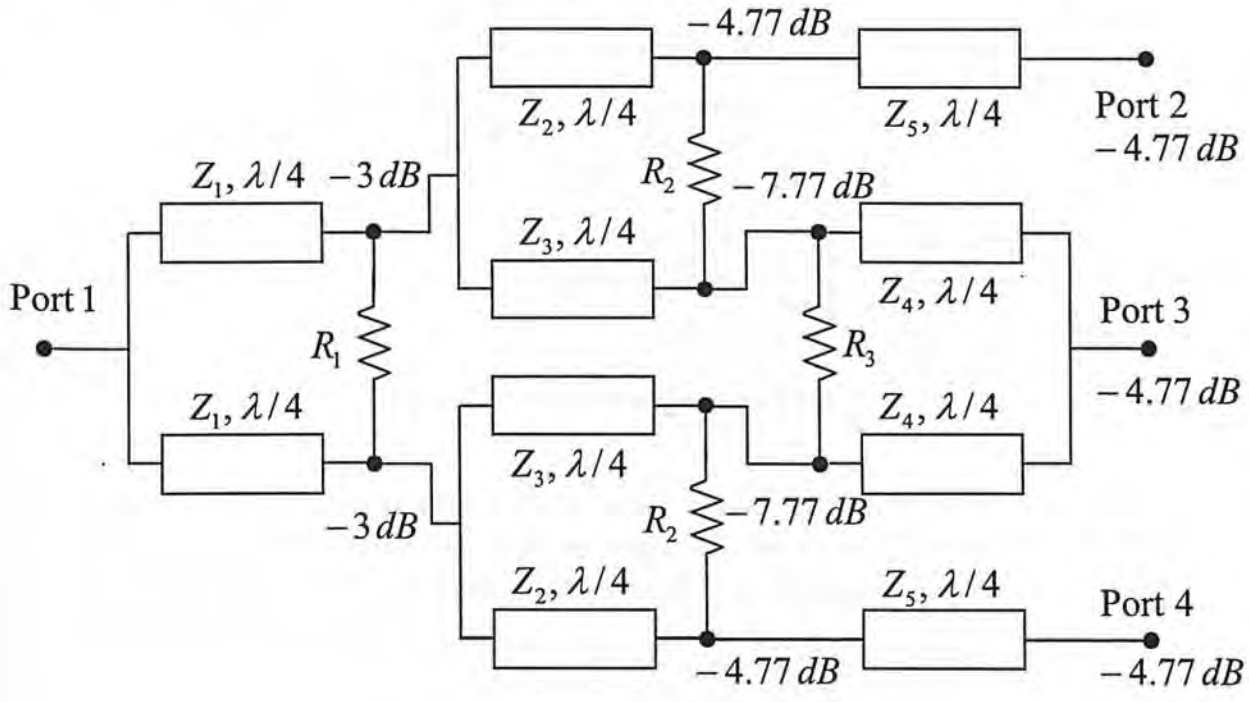


Figure 2.16 Three-way recombinant power divider

A conventional corporate feed power divider design results in 2^n outputs, where n is the number of stages of division. If the second section is designed to provide a 1:2 dividing ratio, as shown in the above figure, the two lower power arms can be recombined into a single centre arm using an equal power combiner. Notice that the resistor (R_3) nearest the centre output arm does nothing to improve the isolation performance under any combination of excitations of the output ports. If the resistor is removed and the two transmission lines (Z_4) at port 3 are combined into a single line, the final result is the topology shown in Figure 2.17.

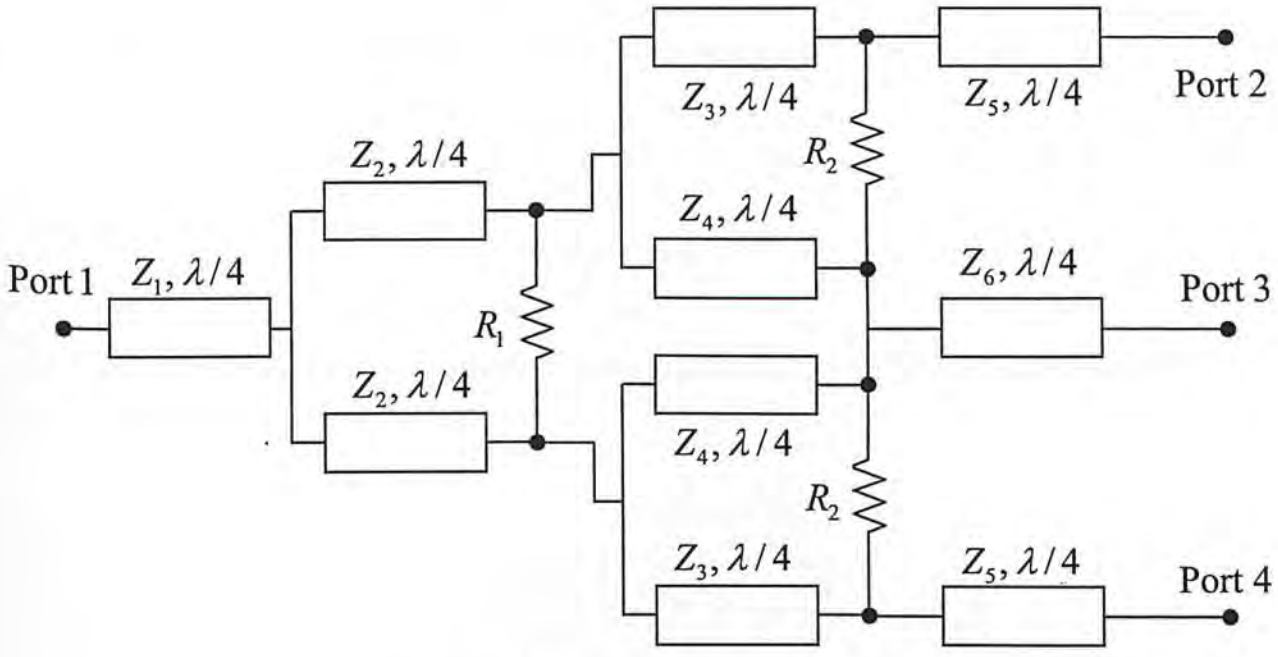


Figure 2.17 Recombinant power divider

To derive the circuit parameters, in-phase / out-of-phase excitation are used to perform the analysis. Under the in-phase excitation, the voltage across each isolation resistor is zero. This allows an equivalent circuit shown in Figure 2.18, to be generated for this divider.

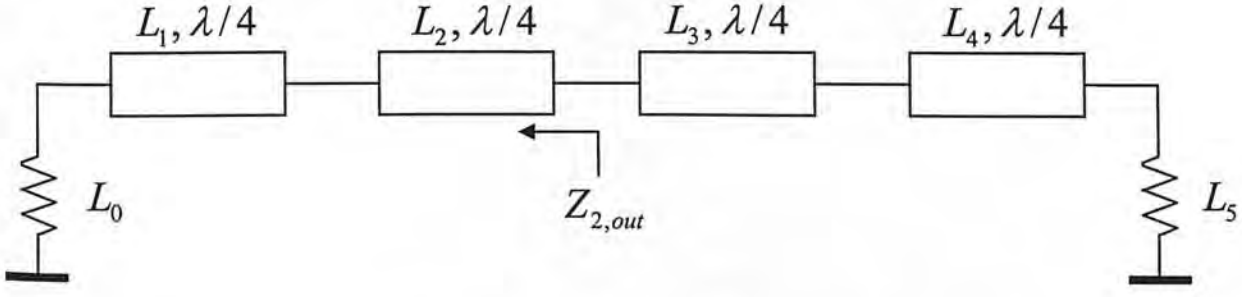


Figure 2.18 Equivalent circuit for synthesis of a three-way divider under in-phase excitation

In this case, a 0.1 dB Chebyshev transformer was selected, resulting in the following impedances:

$$L_0 = Z_0 \qquad L_1 = Z_1 = 0.91Z_0 \qquad L_2 = \frac{Z_2}{2} = 0.70Z_0 \qquad L_5 = \frac{Z_0}{3}$$
$$L_3 = \frac{1}{2}\left(\frac{Z_3 Z_4}{Z_3 + Z_4}\right) = 0.48Z_0 \qquad L_4 = \left(\frac{Z_5 Z_6}{Z_5 + 2Z_6}\right) = 0.36Z_0 \tag{2.10}$$

The power dividing ratio, k^2, places additional requirements on the ratio of Z_3 and Z_4. The constraints are presented in the following relationships:

$$Z_{2,out} = \left(\frac{Z_2}{2Z_1}\right)^2 Z_0 = \frac{k^2}{1+k^2}\left(\frac{Z_3}{Z_5}\right)^2 \frac{Z_0}{2}$$
$$\frac{Z_4}{Z_3} = k\sqrt{2}\frac{Z_6}{Z_5} \tag{2.11}$$

After some algebraic manipulation, these constraints can be written as the following expressions:

$$Z_6 = \frac{L_3 L_4\left(1-k\frac{\sqrt{2}}{2}\right)}{\left(\frac{L_2}{L_1}\right)L_4\sqrt{k^2+1}-k\frac{\sqrt{2}}{2}L_3} \tag{2.12}$$

$$Z_5 = \frac{2L_4 Z_6}{Z_6 - L_4} \tag{2.13}$$

$$Z_4 = 2L_3\left[1+\frac{k\sqrt{2}}{2L_4}(Z_6 - L_4)\right] \tag{2.14}$$

$$Z_3 = \frac{2L_3 Z_4}{Z_4 - 2L_3} \tag{2.15}$$

$$Z_2 = 2L_2 \tag{2.16}$$

$$Z_1 = L_1 \tag{2.17}$$

To determine the value of the isolation resistors, the above technique can be repeated for out-of-phase excitation. By a proper selection of 0°-180°-0° or 0°-0°-180° signals at output ports, the values of R_1 and R_2 can be found. However, the above relationship are singular for the equal dividing ratio where $k^2 = 2$. As a result, it is necessary to begin with the non-singular values of Z_1 and Z_2 and solve for the remainder of the values iteratively.

The recombinant power divider achieves wide isolation bandwidth and requires only three isolation resistors. In addition, this topology allows some freedom to choose the impedance of the transmission lines. The main drawback of this design is that the

number of stages of division increases with the number of output ports, resulting in a large circuit size and high insertion loss.

2.4.6 Multi-coupled-line Approach

Three-way power divider using multi-coupled-line topology was developed in recent years [25-26]. This topology allows a planar structure, reduces isolation resistors and circuit dimension. By using the coupled-line structure, the power divider not only compact but also has dc block characteristics. Figure 2.19 shows the schematic diagram of the three-way power divider using coupled-line which was proposed by Chiu *et al.* [25] in 2006.

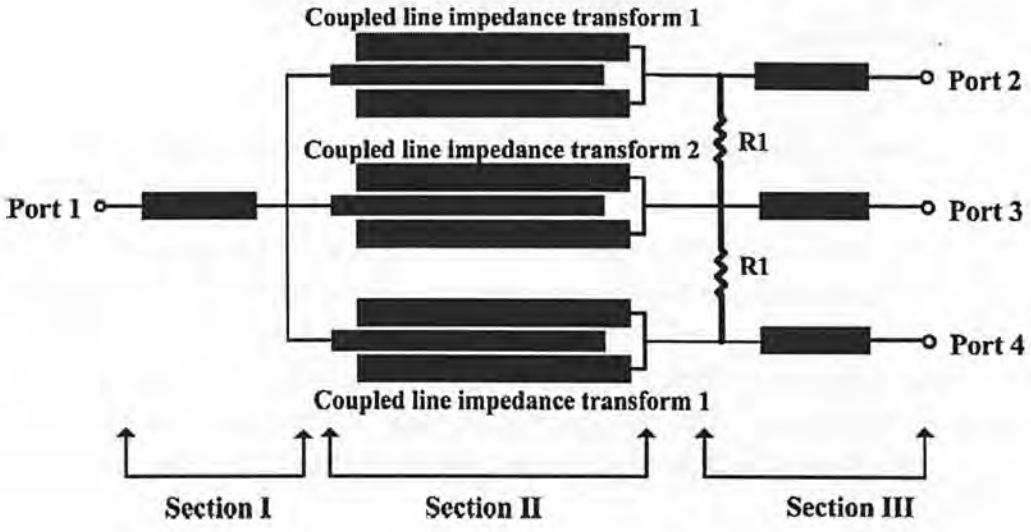


Figure 2.19 Schematic diagram of three-way power divider form Chiu *et al.*

It consists of three λ/4 microstrip coupled lines and 2 isolation resistors, which is easy to design and fabricate. The major drawback of this circuit is that the line impedances and the separation spaces of the coupled lines are estimated by computer optimization. Furthermore, the area utilization rate of this device is still quite low and is not compact enough for monolithic microwave integrated circuits (MMIC) and hybrid microwave integrated circuits (HMIC) applications. Therefore, a new structure of three-way power divider using coupled line approach was presented in 2007 [26]. Figure 2.20 shows the schematic of the new three-way power divider.

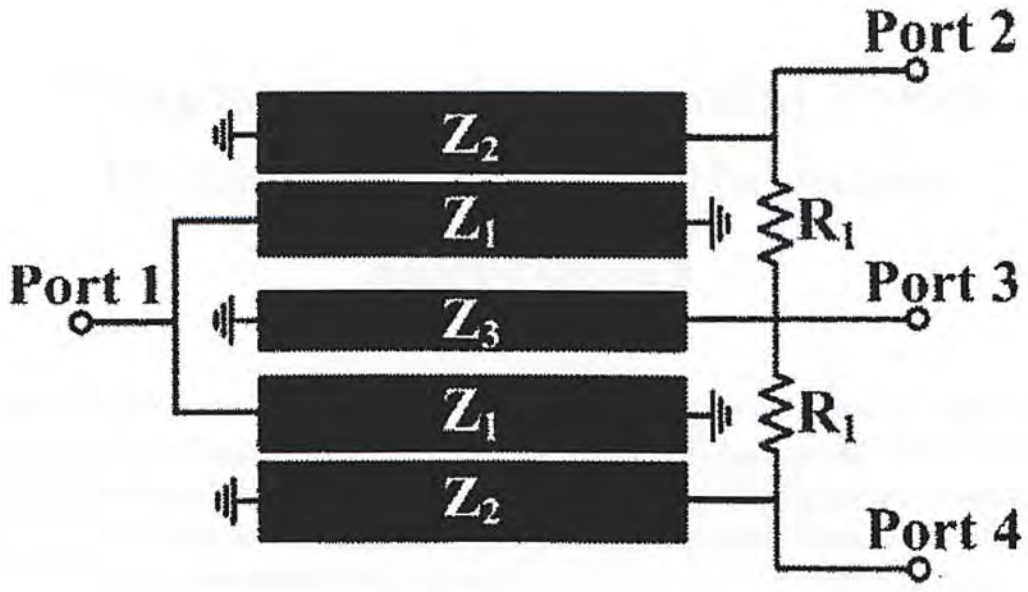


Figure 2.20 Schematic diagram of the new three-way power divider

This new design combined the ideas of Goldfarb [24] and Chiu *et al.* [25]. By utilizing power combination with coupled lines instead of transmission lines, the nine coupled lines can be improved with five λ/4 coupled lines and two isolation resistors. The circuit size is greatly reduced, but still no close-form design formulas can be derived. Thus, the design is time consuming and huge computing resources are needed. The major drawbacks are small gap size and need of ground holes.

Chapter 3: Conventional Power Divider Designs with Harmonic Suppression

In this chapter, some conventional power divider designs with harmonic suppression will be reviewed, which provide the basis and important background information for new designs and topologies to evolve. A summary of the existing divider designs with spurious rejection will be presented in chronological order, from resonating-stubs topology to recent extended line approach.

3.1 Resonating-stubs Topology [27-28]

This is one of the earliest power divider designs with harmonic suppression that have been proposed [27]. As shown in Figure 3.1, the divider is basically modified conventional Wilkinson power divider structure by placing two $\lambda/4n$ open stubs at the centre of each quarter-wave branch of the power divider. An inductor (L) is added in parallel with the isolation resistor (R). Using this topology, the nth harmonic component and its odd multiples are suppressed without surrendering the characteristics of the conventional Wilkinson divider at the operating frequency.

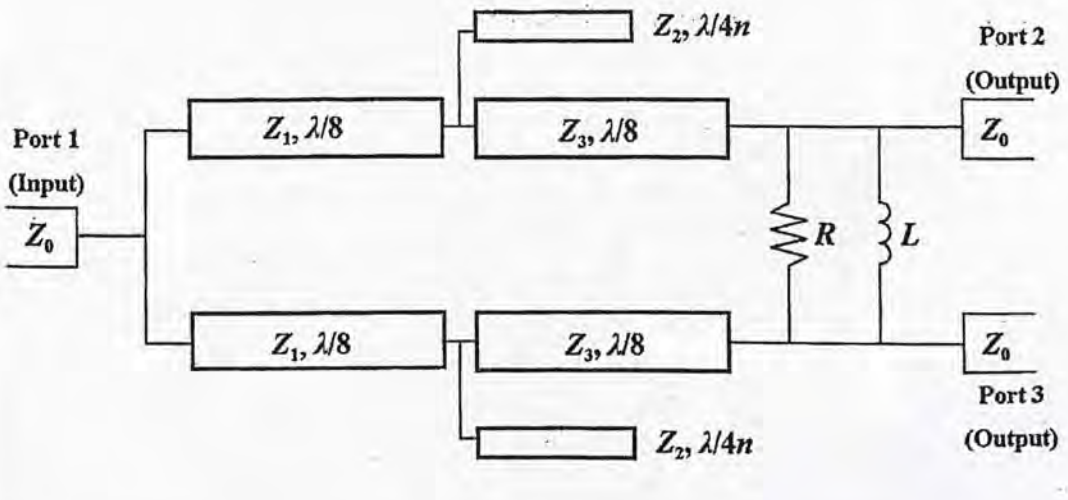


Figure 3.1 Schematic diagram of the Wilkinson power divider for nth harmonic suppression

According to the above diagram, the λ/4 branch of the original Wilkinson divider is divided into two λ/8 sections with different characteristic impedances (Z_1 and Z_3). The nth harmonic component is suppressed using two λ/4n open stubs with impedance Z_2. The power divider is symmetric and hence the even-odd mode analysis can be applied to determine the circuit parameters.

The design equations are shown as follow:

$$Z_1 = 2Z_0 \tag{3.1}$$

$$Z_2 = 2\sqrt{3}\tan\left(\frac{\pi}{2n}\right)Z_0 \tag{3.2}$$

$$Z_3 = \sqrt{3}Z_0 \tag{3.3}$$

$$R = 2Z_0 \tag{3.4}$$

$$L = \frac{2(2+\sqrt{3})}{2\pi f_0}Z_0 \tag{3.5}$$

A modified power divider (f_0 = 2 GHz, n = 3) is illustrated in Figure 3.2 and its frequency responses are plotted in Figure 3.3.

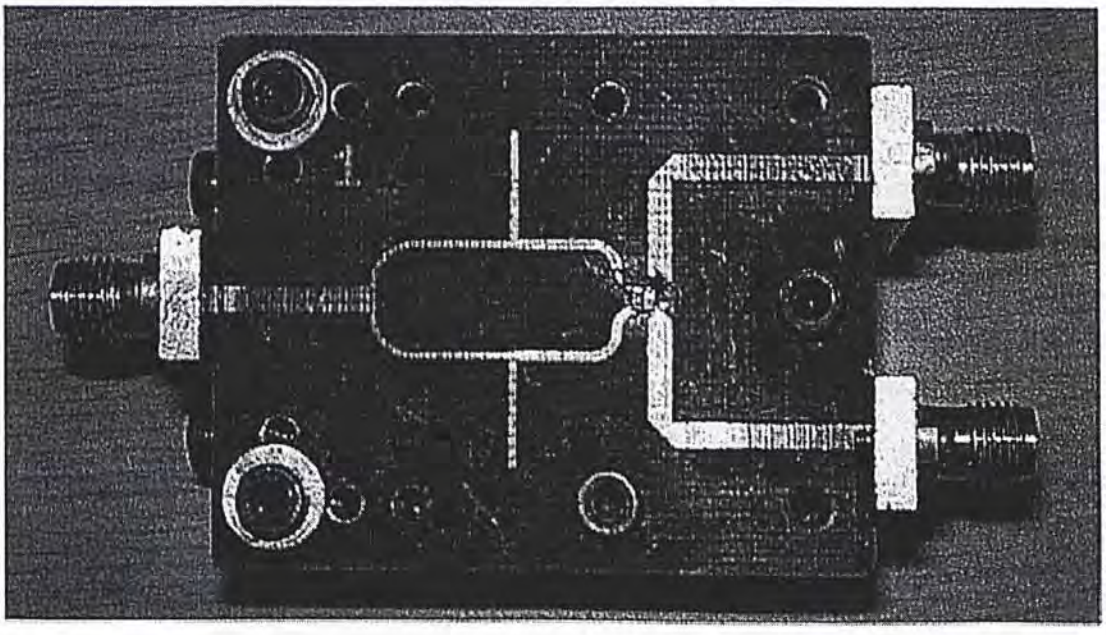


Figure 3.2 Photograph of fabricated 2 GHz Wilkinson power divider for third harmonic suppression

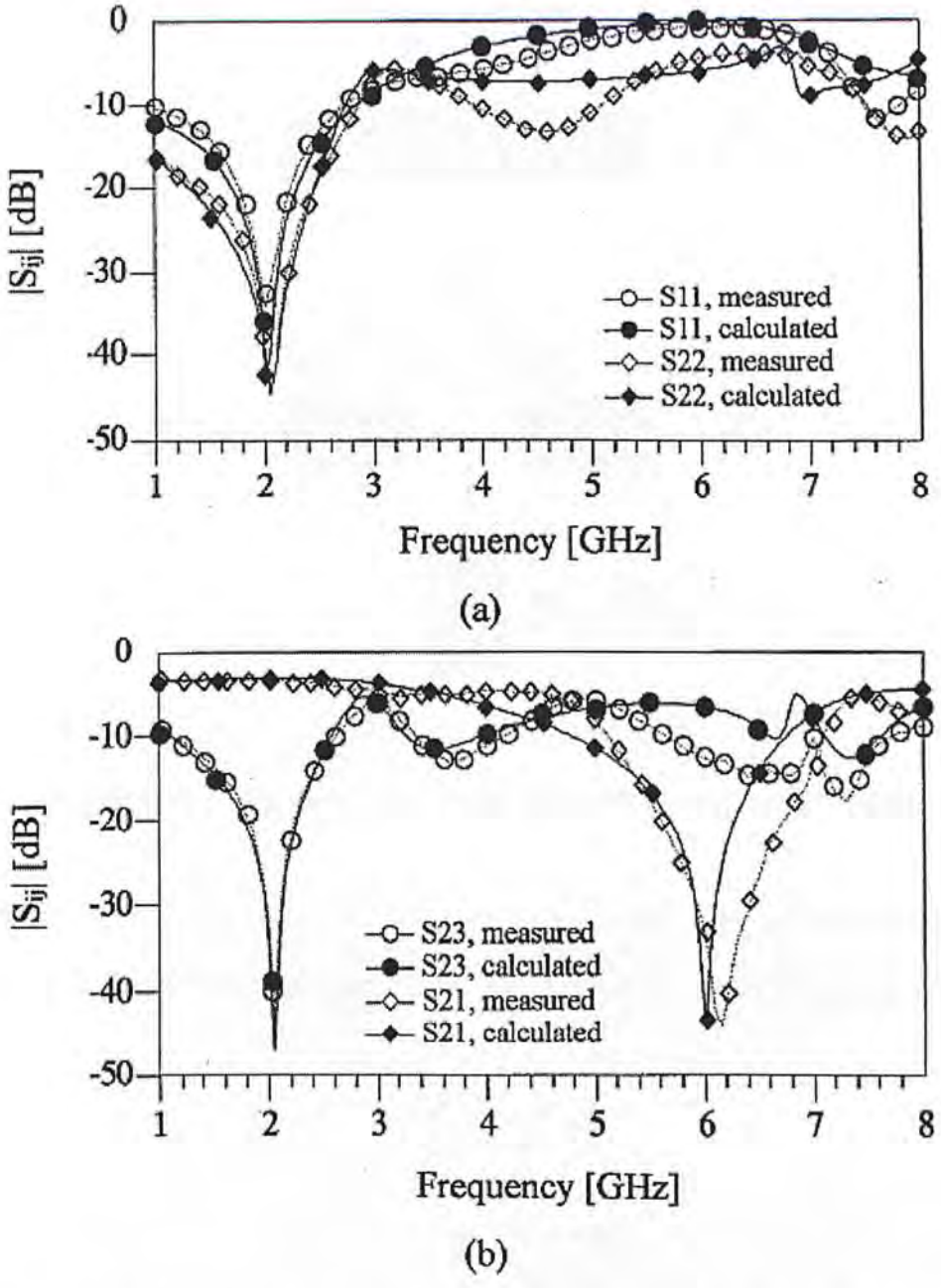


Figure 3.3 Measured and Simulated S-parameters: (a) S_{11} and S_{22}; (b) S_{23} and S_{21}

The drawback of this design is the adoption of additional lumped reactive element (i.e. inductor), as they represent uncertainties in higher frequency operation. In addition, the use of reactive element would increase the manufacturing cost. Therefore, a new design of power divider with harmonic suppression using resonating stubs topology was introduced [28]. Compared to the conversional divider, the λ/4 branch is replaced by a T-network of transmission lines (TL). Figure 3.4 shows the structure of the conventional λ/4 TL and T-network design.

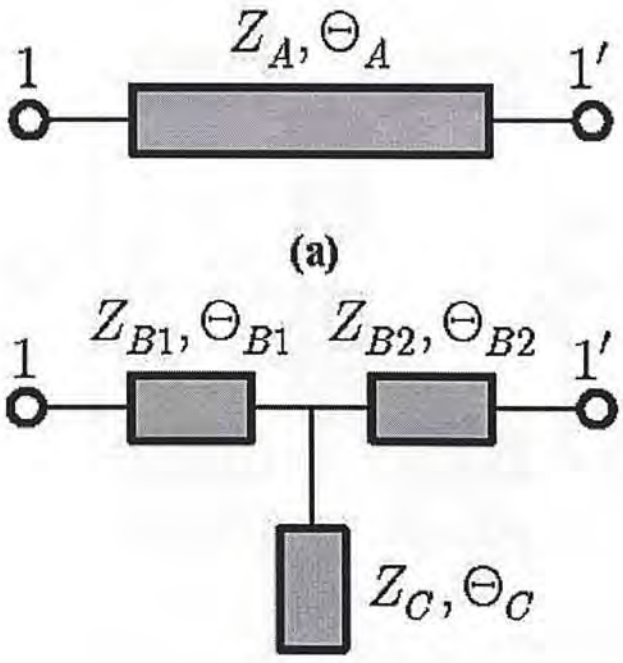


Figure 3.4 Structure of (a) the λ/4 conventional TL and (b) an equivalent T-shaped TL

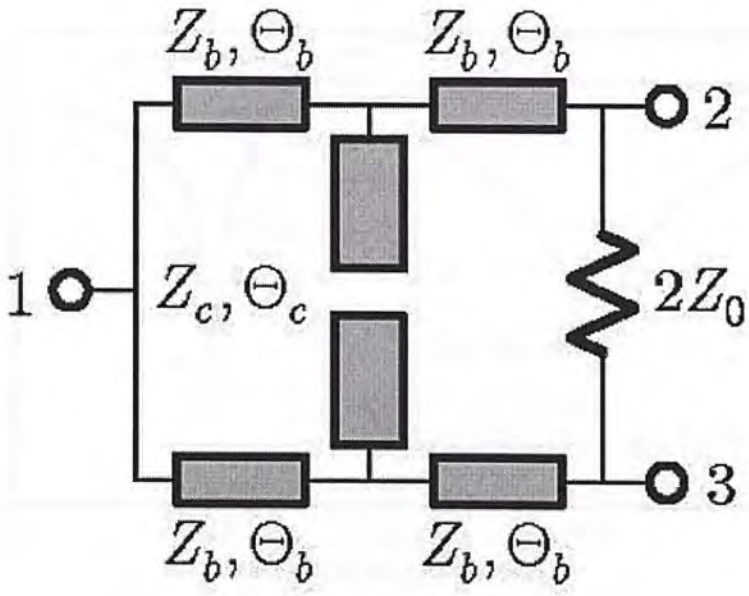
Given that $\Theta_A = \frac{\pi}{2}$, $Z_{B1} = Z_{B2} = Z_B$ and $\Theta_{B1} = \Theta_{B2} = \Theta_B$, the conversion between quarter-wave TL and the T-network TL are summarized by the following equations:

$$\frac{Z_B}{Z_A} = \cot \Theta_B \tag{3.6}$$

$$\frac{Z_C}{Z_A} = \frac{\cos^2 \Theta_B \tan \Theta_C}{1 - 2\sin^2 \Theta_B} \tag{3.7}$$

$$\Theta_C = \left(\frac{\pi}{2}\right)\left(\frac{f_0}{f_1}\right) \tag{3.8}$$

where f_0 is the operating frequency and f_1 is the suppressed frequency ($f_1 > f_0$). Figure 3.5 shows the new power divider configuration ($Z_A = 100\,\Omega$, $\Theta_B = \pi/6$), whereas its frequency response is plotted in Figure 3.6.



(a)

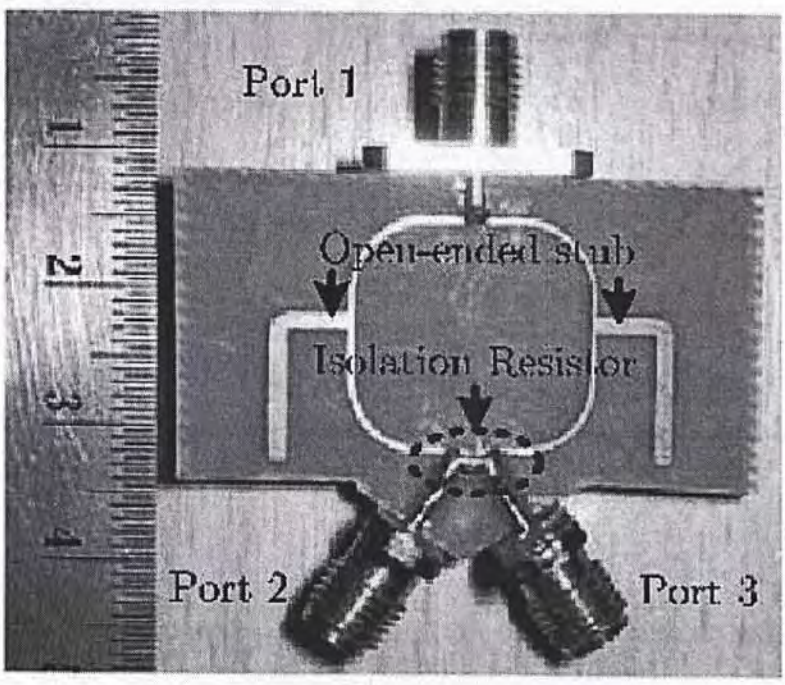
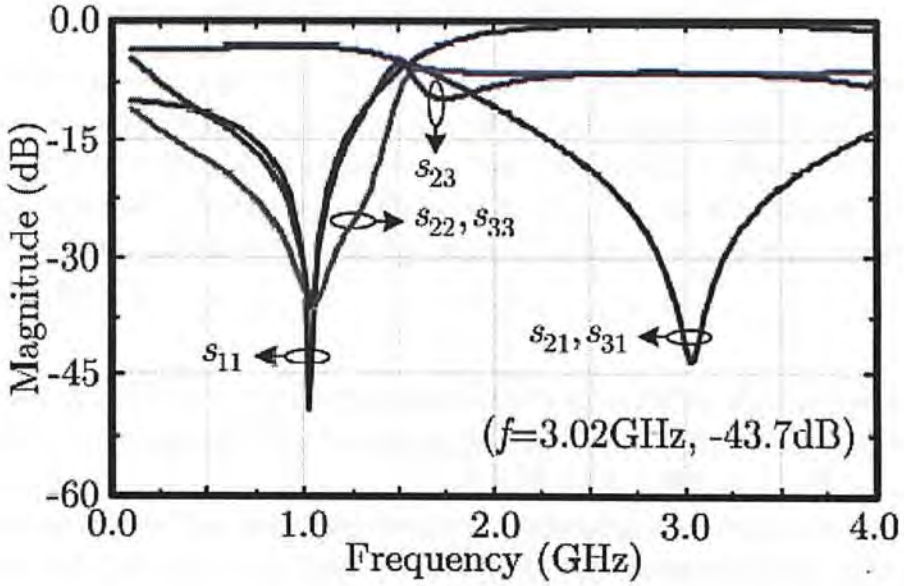
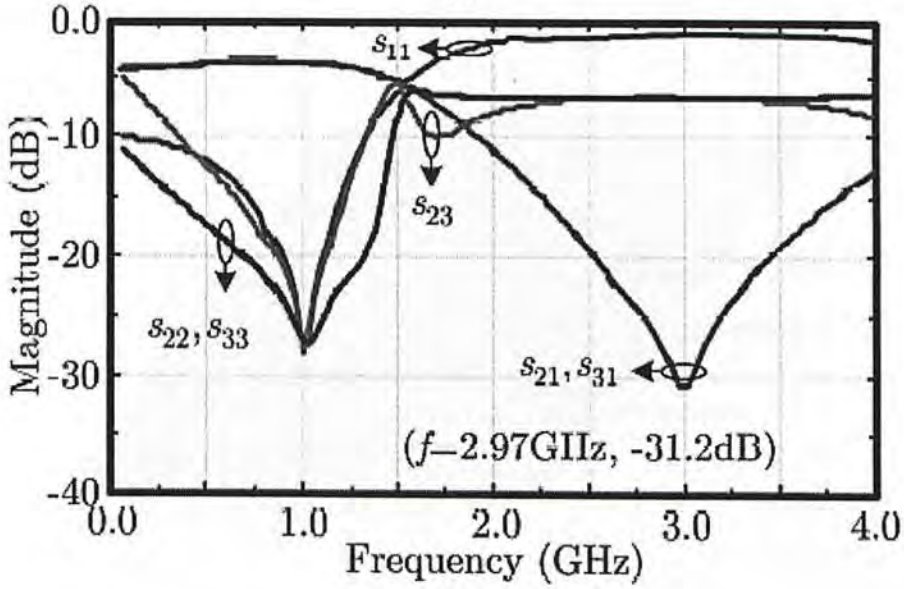


Figure 3.5 The new power divider with harmonic rejection: (a) Schematic; (b) Photograph



(a)



(b)

Figure 3.6 Performances of the new power divider: (a) Simulation results; (b) Meaasured results

The two divider designs are similar to each other in structure and occupy almost the same substrate area. Only one harmonic frequency can be suppressed. The only difference is that no reactive lumped component is used in the new design. The later design, however, involves transmission lines of high impedances for $f_1 = 2f_0$.

3.2 Asymmetric Defected Ground Structure (DGS) [29]

The defected ground structure (DGS) has various applications in microwave and millimetre-wave systems. The DGS of the microstrip line is implemented by making defected pattern on the ground plane. It provides band rejection characteristic at some resonance frequency depending on the design of DGS. In RF circuits, the band-rejection property of the DGS can be utilized in the selective suppression of the harmonics [30-31].

Woo and Lee [29] used asymmetric spiral DGS to suppress the second and third harmonics simultaneously. The Wilkinson power divider with the asymmetric spiral DGS in a quarter-wave line suppresses two harmonics effectively without affecting the performances of the power divider at the operating frequency. The size of the divider is reduced due to the slow-wave effect. The structure of the conventional Wilkinson power divider and the divider using asymmetric DGS are illustrated in Figure 3.7.

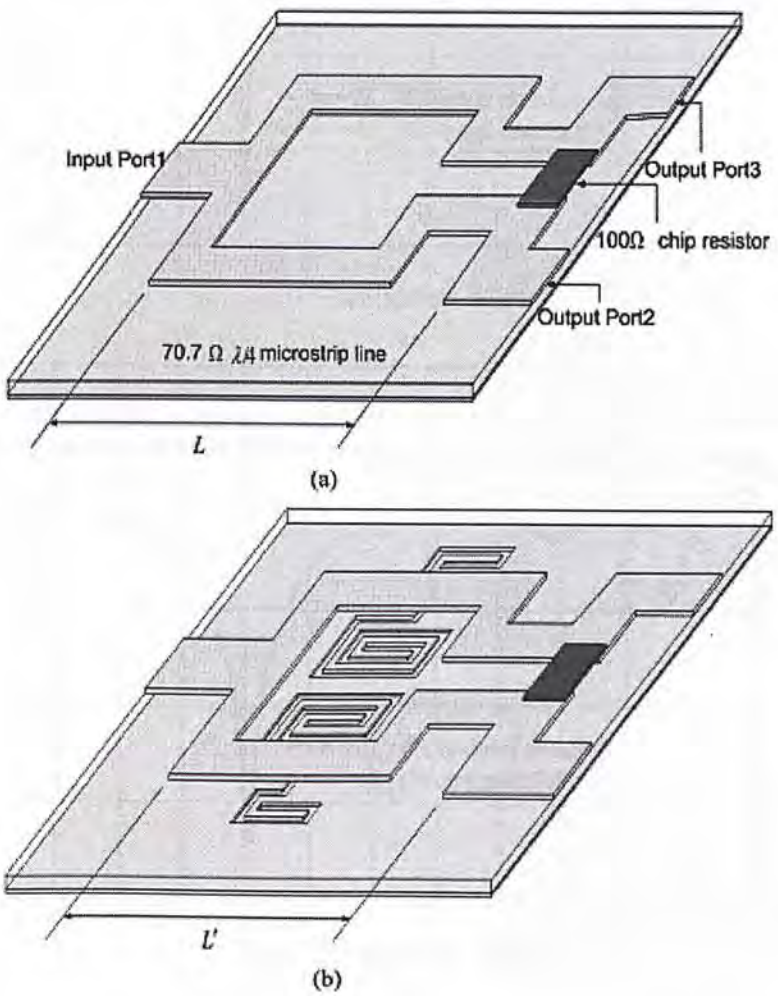


Figure 3.7 Structure of (a) Wilkinson power divider; (b) power divider using asymmetric DGS

The size of the proposed power divider is reduced by 9.1 %. Figure 3.8 shows the simulated frequency responses of the two power dividers. From the simulation results, the second and third harmonic are selected to be suppressed using an asymmetric spiral DGS, while for the conventional one, no suppression is formed. Figure 3.9 and 3.10 shows the photograph of the DGS-based power divider with centre frequency of 1.5 GHz and its frequency response, respectively. However, this design requires backside etching, which is undesirable for low-cost and mass production. Furthermore, this technique can only provide limited rejection (less than 20 dB) at the two harmonic bands with narrow suppression bandwidth.

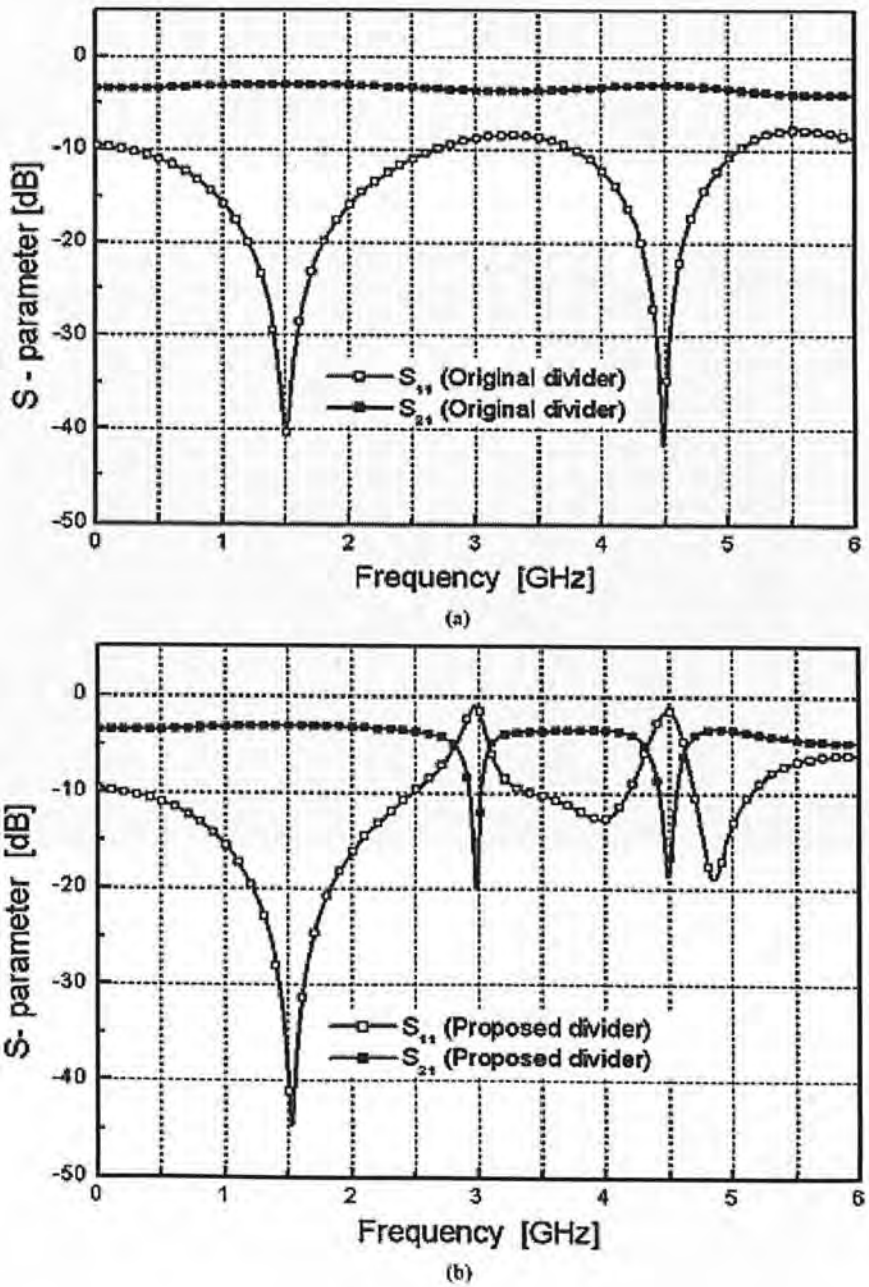
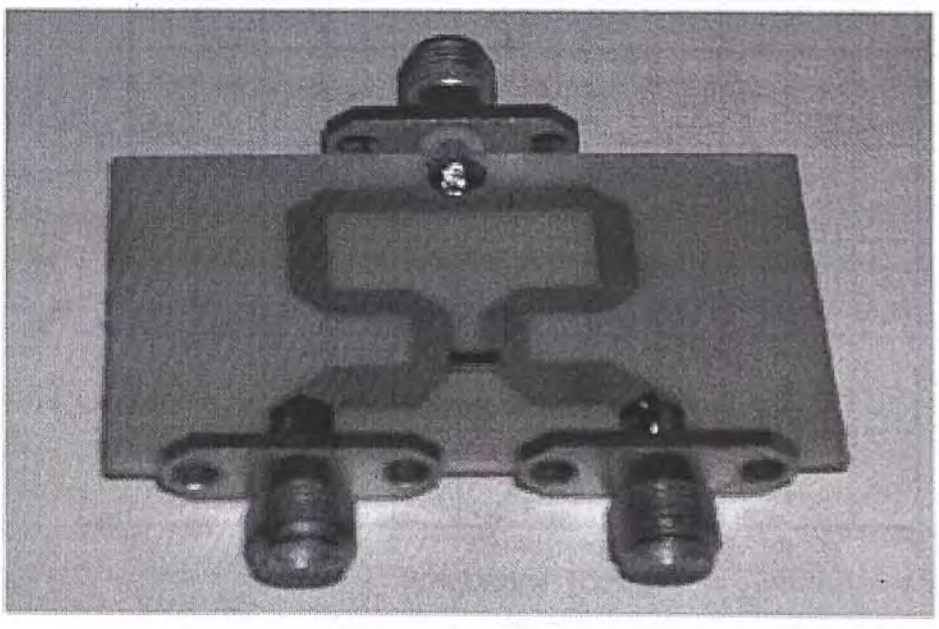
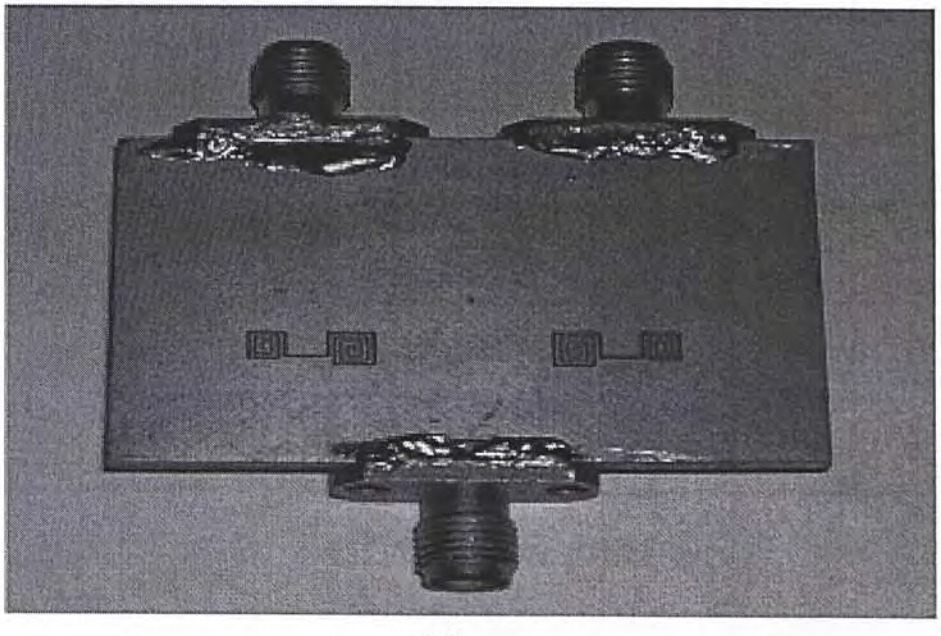


Figure 3.8 Simulated S-parameters of (a) original Wilkinson power divider; (b) power divider using asymmetric DGS



(a)



(b)

Figure 3.9 Fabricated 3-dB Wilkinson power divider with asymmetric spiral DGS. (a) Top view; (b) Bottom view

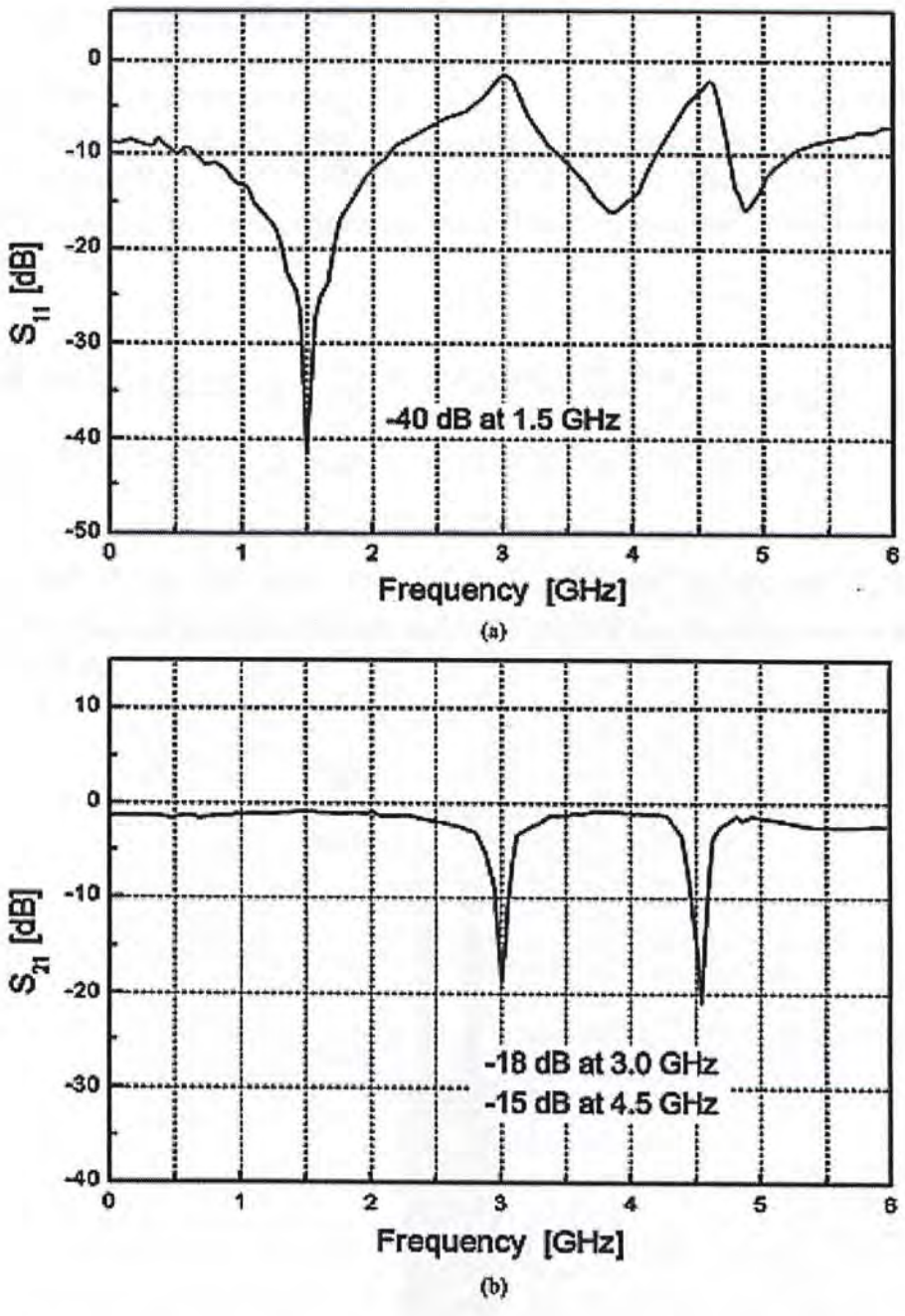


Figure 3.10 Measured S-paramters of the fabricated divider: (a) S_{11}; (b) S_{21}

3.3 Anti-Coupled Line Structure [32]

A short-circuited, anti-coupled line (Figure 3.11) is another technique to enlarge the stop-band bandwidth due to the additional finite attenuation poles, which is useful for harmonic suppression. The circuit consists of a pair of anti-coupled lines short circuited at one end by a low impedance line. The Z –parameter of the structure can be formulated as:

$$Z_T = \begin{bmatrix} j\left(\frac{Z_{oe}\tan\theta_e + Z_{oo}\tan\theta_o}{2} - Z_C\cot\theta_{Lc}\right) & j\left(\frac{Z_{oe}\tan\theta_e - Z_{oo}\tan\theta_o}{2} - Z_C\cot\theta_{Lc}\right) \\ j\left(\frac{Z_{oe}\tan\theta_e - Z_{oo}\tan\theta_o}{2} - Z_C\cot\theta_{Lc}\right) & j\left(\frac{Z_{oe}\tan\theta_e + Z_{oo}\tan\theta_o}{2} - Z_C\cot\theta_{Lc}\right) \end{bmatrix} \quad (3.9)$$

where θ_e and θ_o are the even- and odd-mode electrical length, and Z_C and θ_{Lc} represent the characteristic impedance and the electrical length of the low impedance line respectively.

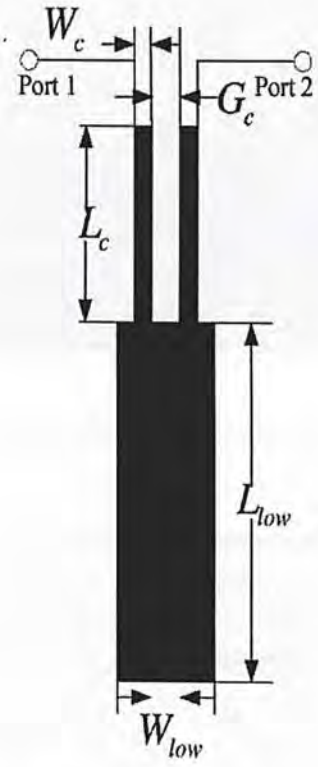


Figure 3.11 Layout of a short circuit anti-coupled line

From (3.9), S_{21} can be obtained as follows:

$$S_{21} = \frac{2Z_{21}}{|Z_T| + Z_{11} + Z_{22} + 1} \quad (3.10)$$

Finite attenuation poles occur when $Z_{21} = 0$, which reduces to:

$$Z_C \cot\theta_{Lc} = \frac{Z_{oe}\tan\theta_e - Z_{oo}\tan\theta_o}{2} \tag{3.11}$$

As $Z_C \cot\theta_{Lc}$ is monotonically decreasing with frequency; while the function of $Z_{oe}\tan\theta_e - Z_{oo}\tan\theta_o$ has maximum and minimum at its discontinuity spot, three controllable attenuation poles will be presented over the stop-band. From the above analysis, it can be concluded that the first and the third finite attenuation poles would shift as the load capacitance changes and the second one would have no shift. Figure 3.12 illustrates the layout of the power divider with anti-coupled lines and a conventional Wilkinson power divider. Both simulated and measured frequency responses are shown in Figure 3.13.

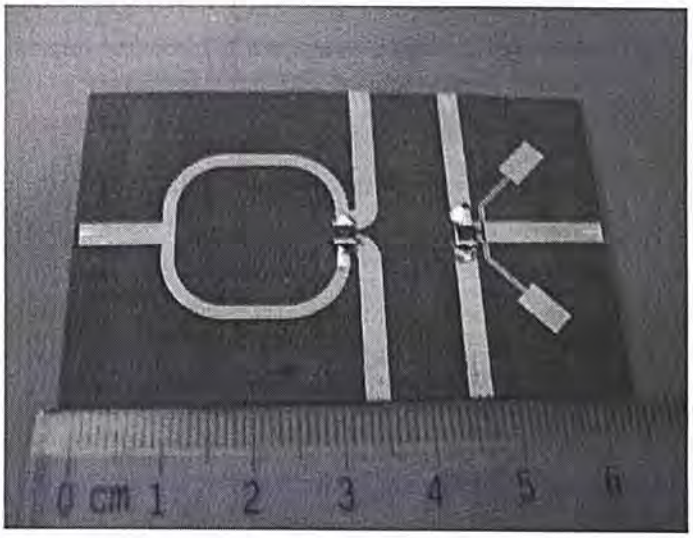
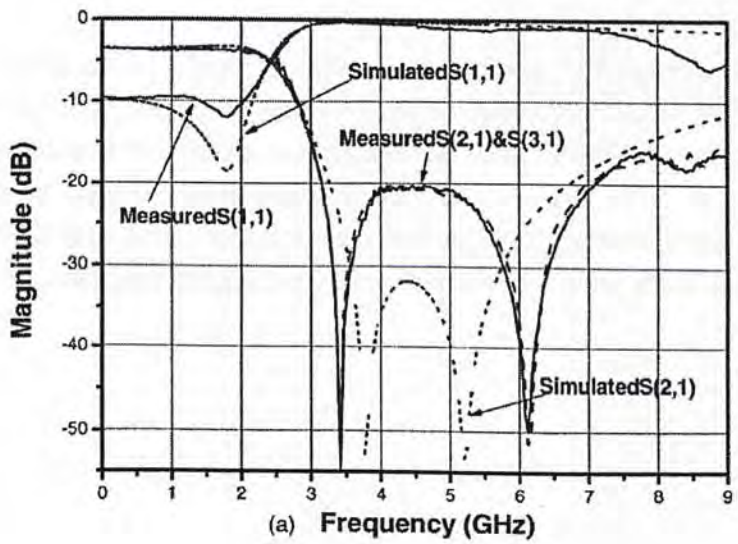


Figure 3.12 Photograph of the divider using anti-cooupled line (right) and conventional power divider



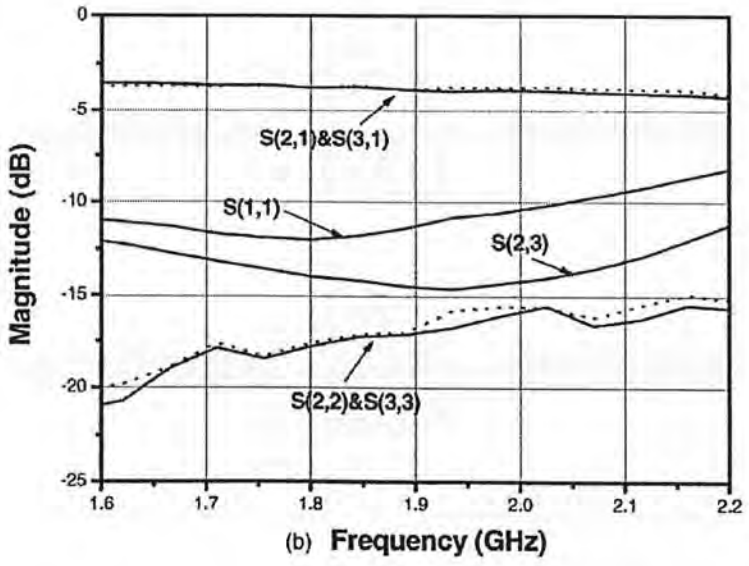


Figure 3.13 Frequency responses of the power divider: (a) at whole frequency band; (b) at frequency band near the operating frequency

According to the above results, the divider can operate with spurious suppression from 3.2 to 7 GHz by more than 20 dB. However, the input return loss (S_{11}) and the output port isolation (S_{23}) are both less than 15 dB, which means that the circuit is not perfectly matched and some power can be coupled between the outputs. Furthermore, as the size of the microstrip lines and gaps (anti-coupled lines) are quite small (W_c = 0.3 mm and G_c = 0.15 mm), precise manufacturing facility is required, which is undesirable for low cost production. In addition, no closed-form design formulas are available and the structural dimensions can only be obtained by computer optimization.

3.4 Microstrip Electromagnetic Bandgap (EBG) Based Topology [33]

Microstrip transmission lines incorporating the electromagnetic bandgap (EBG) structure demonstrate band-stop and slow-wave characteristics, which can be utilized to suppress unwanted harmonics and reduce the sizes of the microstrip branch. Power divider with microstrip EBG cells (Figure 3.14) can offer several advantages including planar structure, compact size and superior harmonic suppression. Figure 3.14 shows the schematic diagram of the power divider using EBD cells.

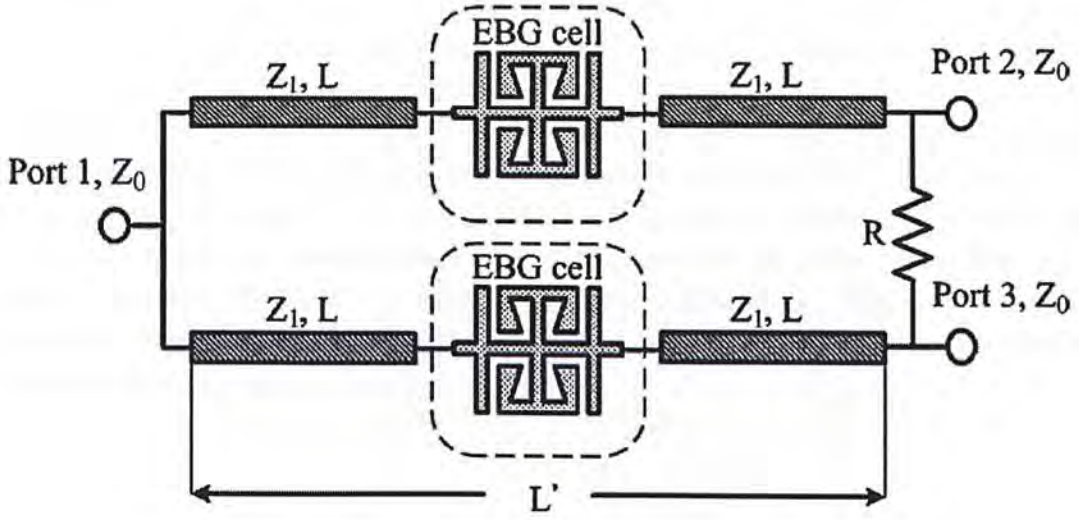


Figure 3.14 Schematic diagram of the power divider using EBG cells

Referring to Figure 3.14, the power divider is consisted of two microstrip EBG cells and four microstrips (length L and characteristic impedance Z_1). The EBG cell can provide two resonances to suppress the unwanted harmonics and reduce the length of a quarter-wave transmission line simultaneously. Figure 3.15 shows the detailed structure of a microstrip EBG cell.

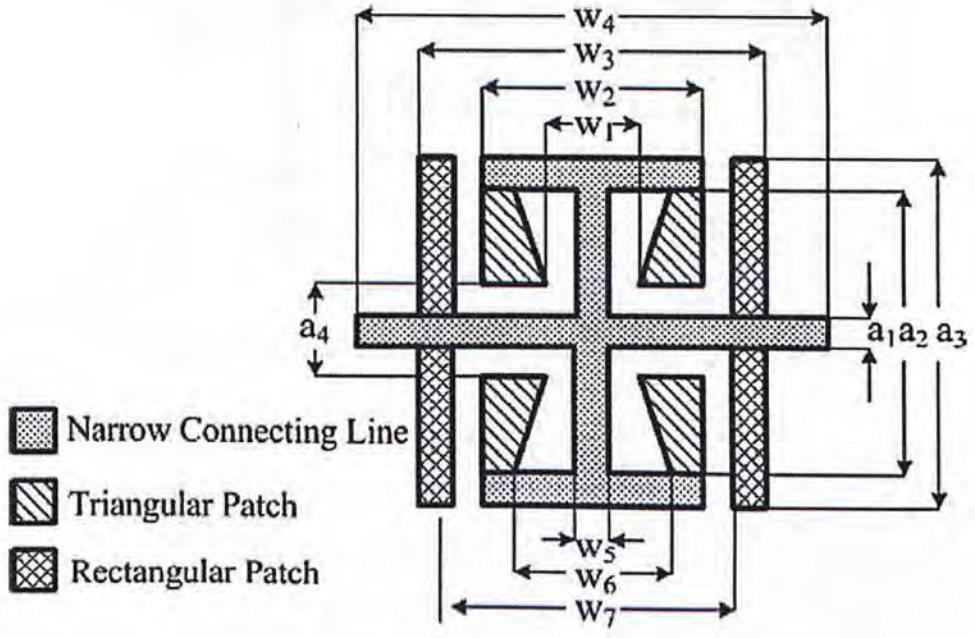


Figure 3.15 Structure of a microstrip EBG cell

By adjusting the narrow connecting lines and the size of the etched pattern, different slow-wave effects can be obtained at different frequencies to suppress the unwanted *n*th harmonics. The dimensions of the EBG cell is first determined by its equivalent circuit model [34] (Figure 3.16) and then finalized by optimization through EM solver. The photograph of the fabricated circuit is shown in Figure 3.17. The frequency responses are illustrated in Figure 3.18. According to the measured results, the prototype operates as a conventional Wilkinson power divider at the centre frequency while suppressing the third and fifth harmonics simultaneously. The size of the λ/4 branch is reduced by more than 30 % compared to the conventional one. Its major disadvantage is the narrow rejection bandwidth.

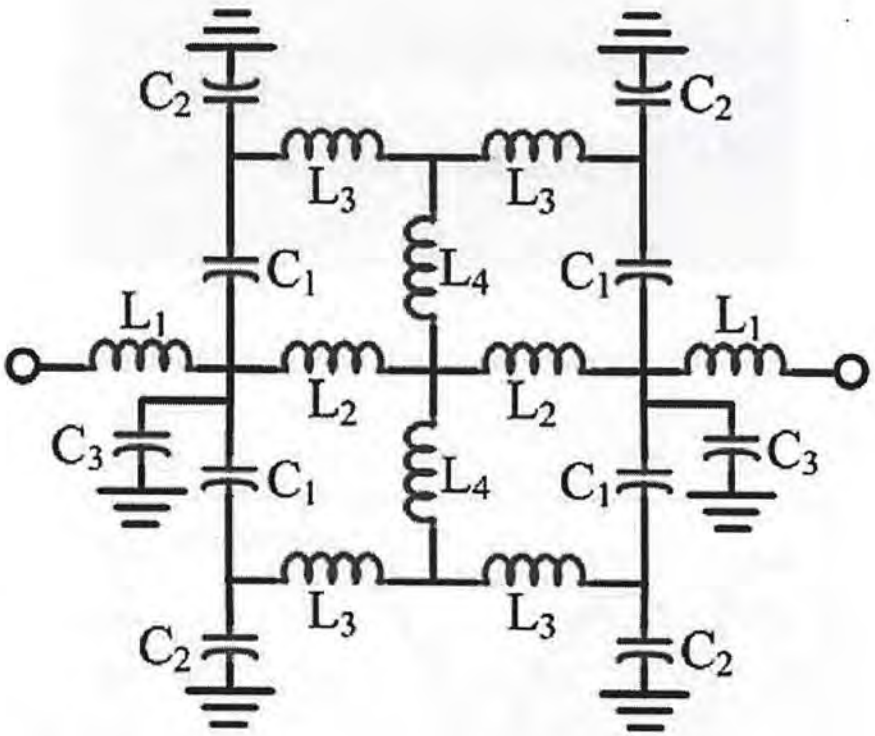


Figure 3.16 Equivalent L-C circuit of a microstrip EBG cell

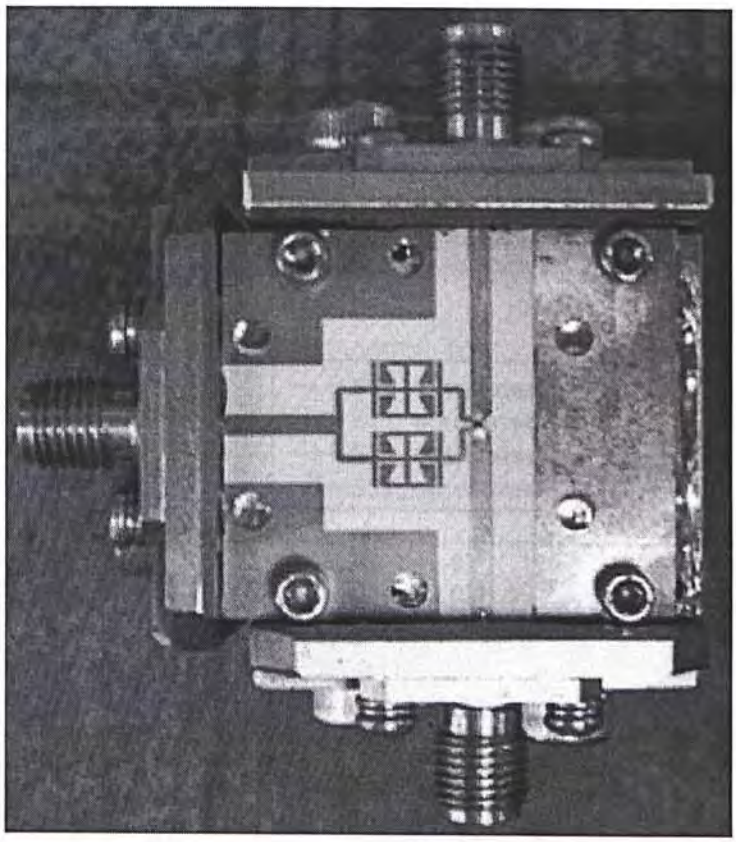
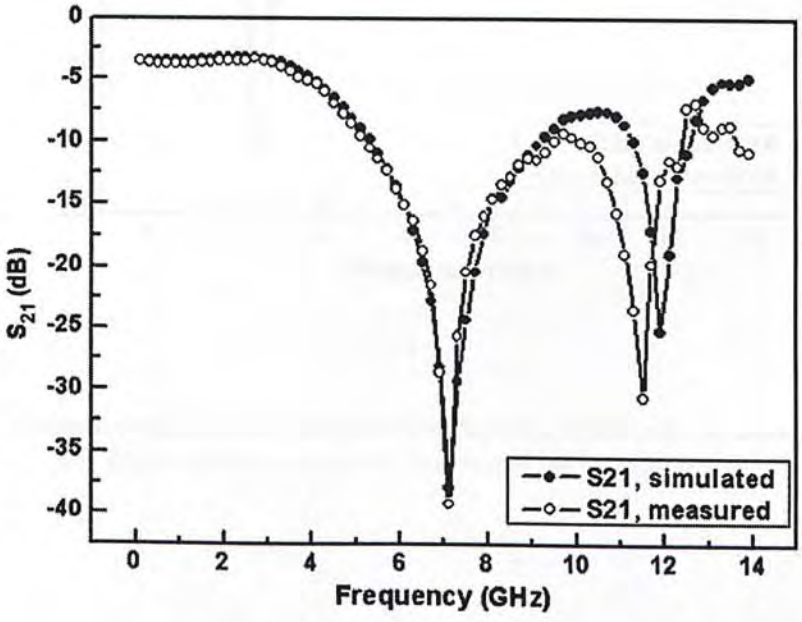
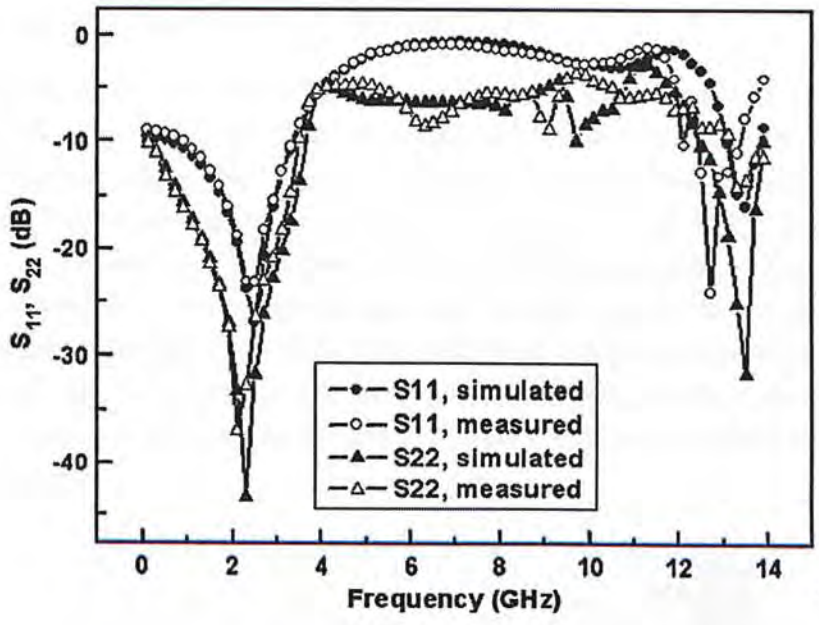


Figure 3.17 Photograph of the power divider with EBG cells



(a)



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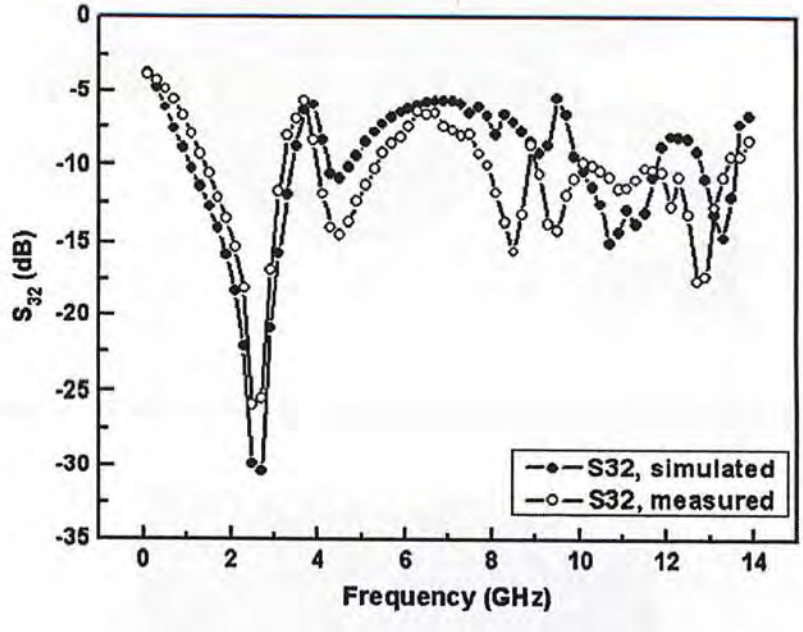


(c)

Figure 3.18 Frequency responses for the power divider using EBG cells: (a) Insertion loss; (b) Input / output return loss; (c) Output port isolation

3.5 Embedded Resonators Topology [35]

A miniaturized microstrip power divider using embedded resonators (Figure 3.19) was proposed recently. It has four microstrip high-low impedance resonator cells uniformly placed inside the Wilkinson power divider. These resonators allow reduction of circuit size and the suppression of harmonic bands (third and fifth). The dimensions of the resonator were obtained by computer optimization. Figure 3.20 and 3.21 give, respectively, the physical layout and frequency response of the prototype. This circuit performs like a low pass filter with high frequency rejection of about 30 dB. However, the drawback is the slow roll-off. Good isolation and return loss performances were achieved. The divider is compact and easy to fabricate by standard etching process.

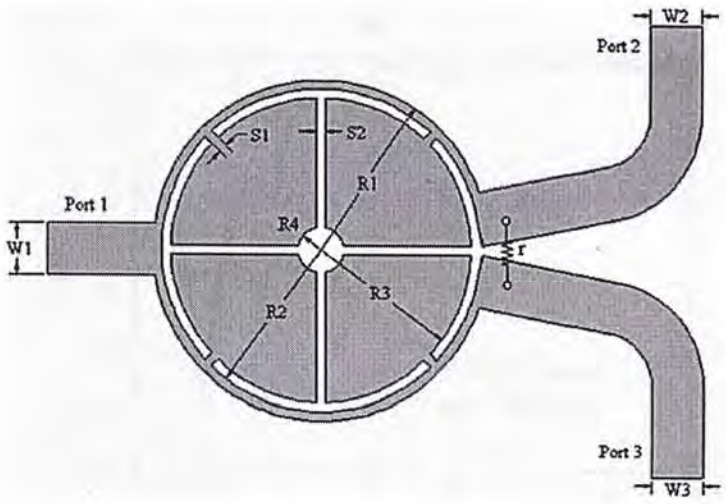


Figure 3.19 Configuration of the power divider using embedded resonators

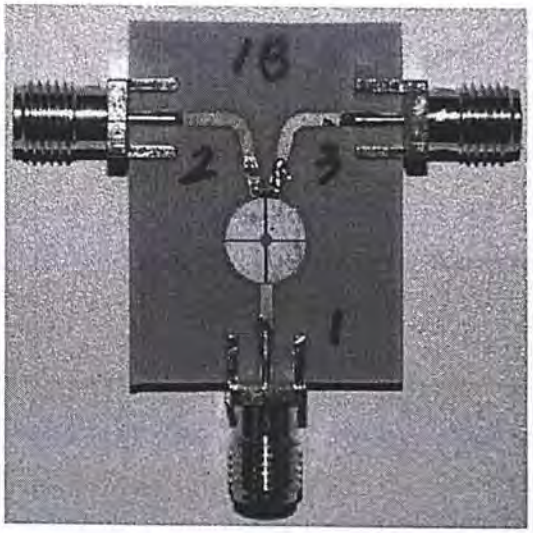
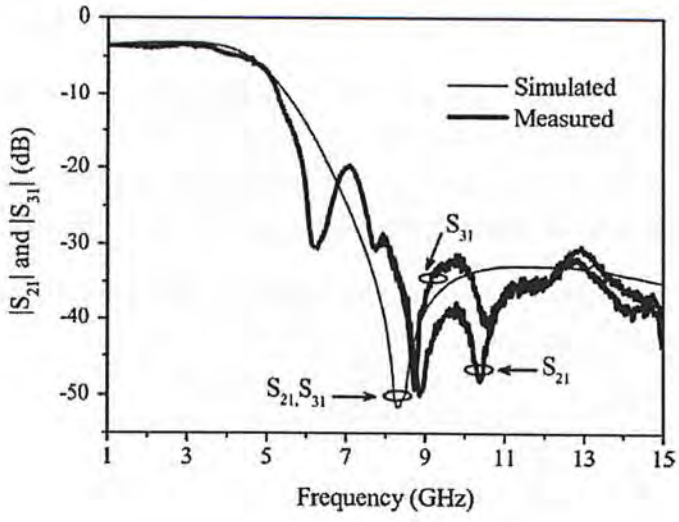
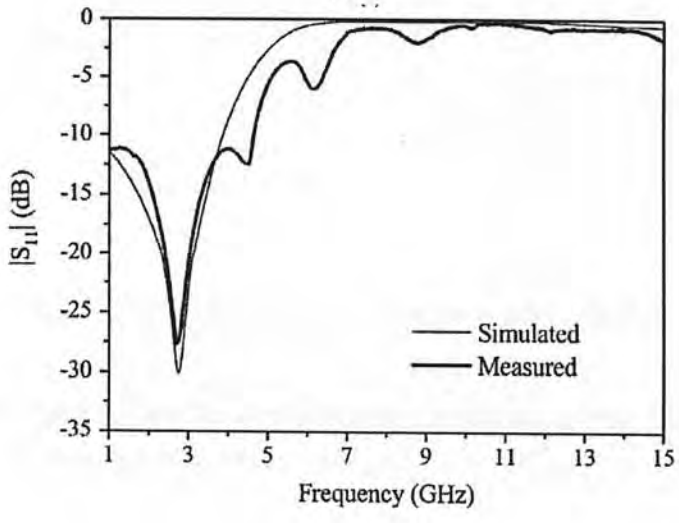


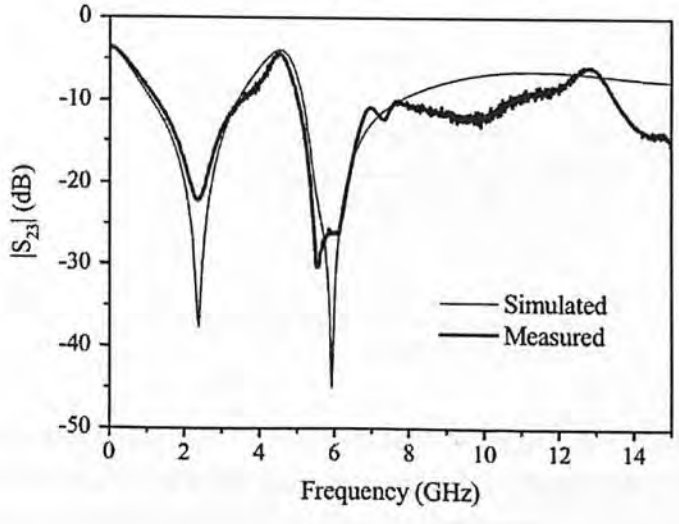
Figure 3.20 Photograph of the divider using embedded resonators



(a)



(b)



(c)

Figure 3.21 Frequency responses for the power divider using embedded resonators: (a) Insertion loss; (b) Input return loss; (c) Output port isolation

3.6 Extended Line Approach [36]

Figure 3.22 shows the configuration of the modified two-way power divider with single harmonic rejection. It basically consists of four branch-line sections and a resistor. Two extended lines with impedance Z_2 are inserted between the output ports. The extended lines are used for harmonic suppression by the proper selection of $\theta_2\left(=\frac{\pi}{2n}\right)$, where n is the number of harmonic band to be rejected.

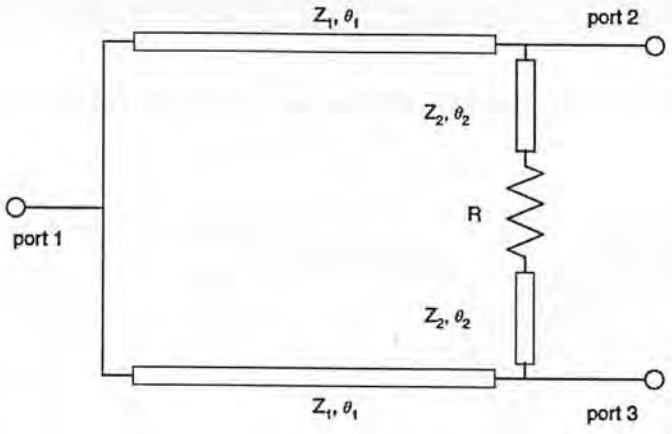


Figure 3.22 Modified two-way Wilkinson power divider

By applying even- and odd-mode formulations, the design parameters can be derived and expressed as follows $(z_1 = Z_1/Z_0, z_2 = Z_2/Z_0, r = R/Z_0)$:

$$r = 2\,(1-\tan^2\theta_2) \tag{3.12}$$

$$z_2 = \sqrt{r} \tag{3.13}$$

$$z_1 = z_2\sqrt{\frac{2}{z_2^2 + 2\tan^2\theta_2}} \tag{3.14}$$

$$\theta_1 = \pi - \tan^{-1}\left(\frac{1}{\tan\theta_2}\frac{z_2}{z_1}\right) \tag{3.15}$$

Figure 3.23 shows the fabricated circuit designed to reject the third harmonic band. Both measured and simulated frequency responses are illustrated in Figure 3.24. The power divider was found to exhibit excellent performance at both the fundamental as well as the third harmonic bands. However, only single harmonic rejection and narrow stop band bandwidth were realizable by the proposed topology.

Figure 3.23 Photograph of the modified Wilkinson power divider

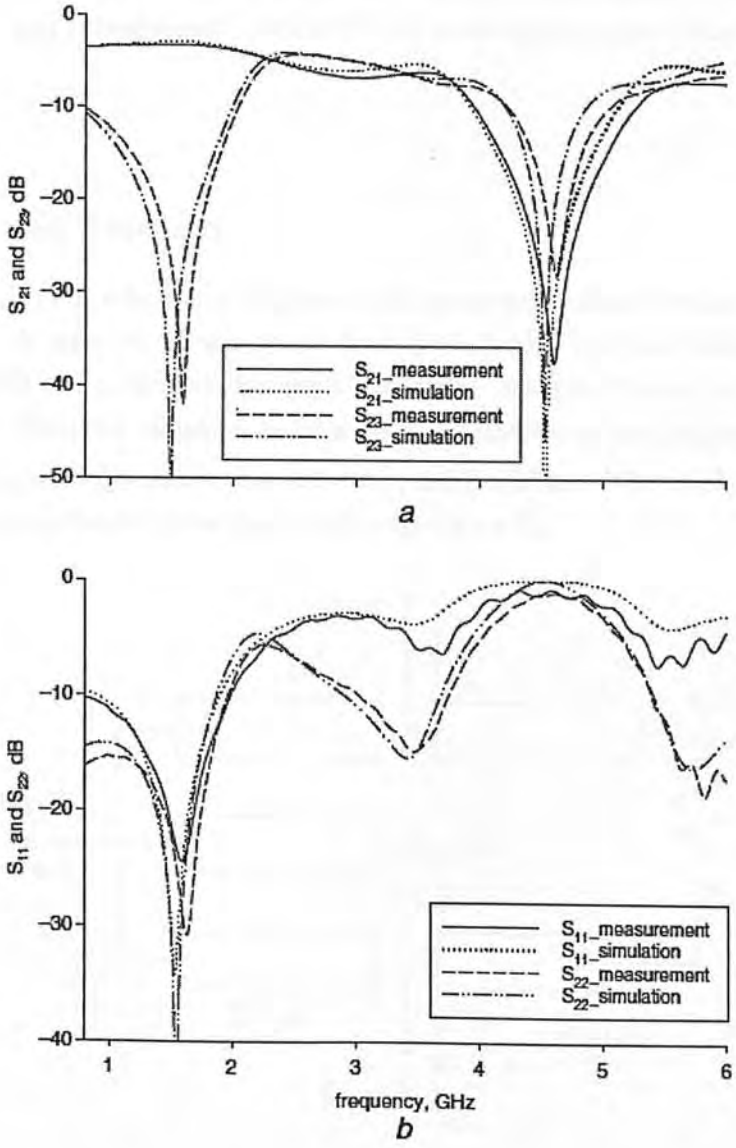


Figure 3.24 Frequency responses of the power divider with extended lines: (a) S_{21} and S_{23}; (b) S_{11} and S_{22}

Chapter 4: New 2-way Power Divider Design with Spurious Suppression and Impedance Transformation

This chapter presents a novel design of microwave power divider with spurious suppression and impedance transformation. Explicit closed-form design equations are derived based upon even- and odd- mode analysis. The proposed circuit also features simple structure, compact size and enhanced stop-band attenuation. For demonstration, the simulated and experimental results of two prototypes implemented on microstrip are given.

4.1 Proposed Topology

Figure 4.1 shows the schematic diagram of the proposed power divider with harmonic suppression. It basically consists of four branch-line sections, single shunt stub (open-circuited) and a resistor. Unlike all previous designs, the output ports are kept distance away from the isolation resistor by the insertion of two extended lines (Z_B) for increased layout flexibility and reduced parasitic effect. The load impedance, R_L, is assumed to be different from the source impedance R_S.

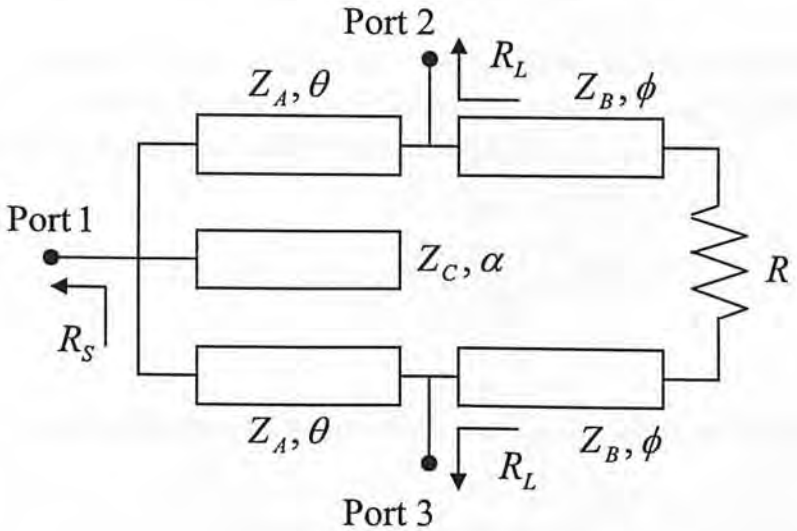


Figure 4.1 Circuit configuration of proposed power divider

It is further assumed that R_S, R_L, R, ϕ and α are free variables while Z_A, Z_B, Z_C and θ are unknowns to be determined. By applying the even- and odd-mode formulation, these unknown parameters can simply be derived from the electrical properties of an ideal power divider (perfect return loss and port isolation) evaluated at the fundamental frequency (f_0).

4.2 Design and Analysis

Even-mode Analysis

Figure 4.2 depicts the equivalent circuit of the proposed divider under even-mode excitation. It can be seen that the extended line (Z_B) and the open circuit stub ($2Z_C$) are responsible for the creation of two transmission zeros. For instant, an electrical length of 45°, 30° or 22.5° corresponds to the suppression of the second, third or fourth harmonic frequencies, respectively. According to (4.1) and (4.2), the frequencies of the transmission zeros (f_{Z1} and f_{Z2}) can be adjusted by the selection of ϕ and α. Meanwhile, the low-pass characteristics of the resulting network can help to further increase the attenuation level of spurious suppression.

$$f_{Z1} = \frac{\pi}{2\alpha} f_0 \tag{4.1}$$

$$f_{Z2} = \frac{\pi}{2\phi} f_0 \tag{4.2}$$

Under the condition of ideal input return loss, it can be proved that the output admittance Y_{even} of the even-mode circuit is simply equal to Y_L at f_0. Mathematically, this relation can be formulated and expressed by (4.3).

$$Y_{even} = Y_L = Y_B \frac{2 + jRY_B \tan\phi}{RY_B + j2\tan\phi} - jY_A \cot\theta \tag{4.3}$$

By equating the real and imaginary parts of the above expression, one obtains:

$$RY_B Y_L - 2Y_A \tan\phi \cot\theta = 2Y_B \tag{4.4}$$

$$2Y_L \tan\phi + RY_A Y_B \cot\theta = RY_B{}^2 \tan\phi \tag{4.5}$$

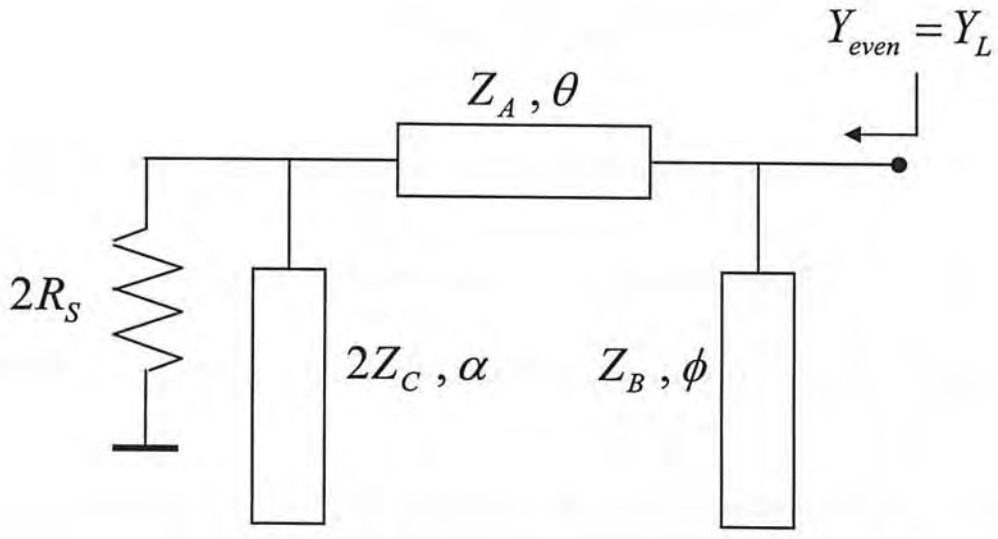


Figure 4.2 Equivalent circuit: even-mode

Odd-mode Analysis

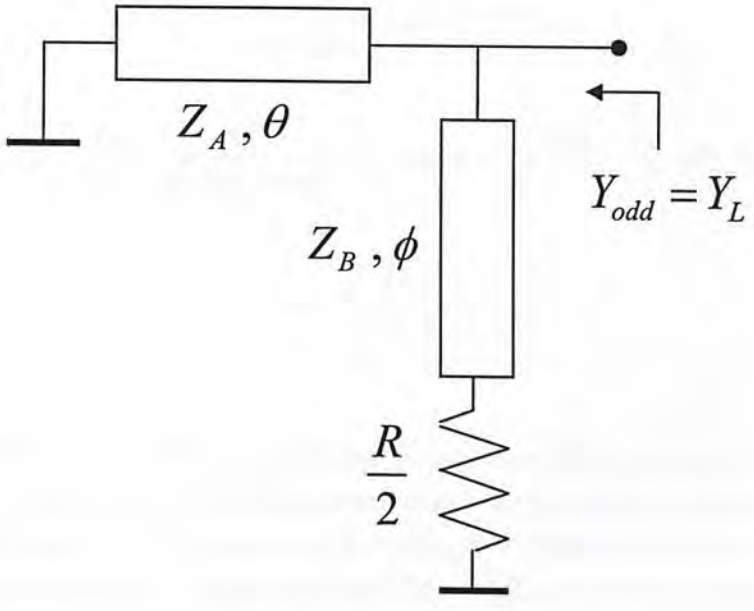


Figure 4.3 Equivalent circuit: odd-mode

Under odd-mode excitation, the equivalent circuit of the proposed divider is given in Figure 4.3. With the assumption that the two output ports are perfectly matched and isolated (evaluated at the center frequency), a second condition may thus be stated as follows:

$$Y_{even} = Y_L = Y_B \frac{2 + jRY_B \tan\phi}{RY_B + j2\tan\phi} - jY_A \cot\theta \tag{4.6}$$

Similarly, the real and imaginary parts of (4.6) may be equated to give:

$$2Y_A Y_L - Y_C Y_L \tan\alpha \tan\theta + Y_B Y_S \tan\theta \tan\phi = Y_A Y_S \tag{4.7}$$

$$Y_S Y_L \tan\theta - 2Y_A Y_B \tan\phi + Y_B Y_C \tan\phi \tan\alpha \tan\theta = Y_A Y_C \tan\alpha + 2Y_A^{\,2} \tan\theta \tag{4.8}$$

Finally, by solving (4.4), (4.5), (4.7) and (4.8), the circuit parameters of the proposed configuration can thus be obtained via the following expressions.

$$Y_A = \frac{1}{Z_A} = \sqrt{\frac{Y_S Y_L}{2} - \frac{Y_B^{\,2}}{2}(RY_L - 2) + \frac{Y_B Y_C \tan\alpha}{4\tan\phi}(2\sec^2\phi - RY_L)} \tag{4.9}$$

$$Z_B = \frac{1}{2\tan\phi}\sqrt{\frac{R}{Y_L}(2\sec^2\phi - RY_L)} \tag{4.10}$$

$$Y_C = \frac{1}{Z_C} = \frac{Y_B}{2Y_L \tan\phi \tan\alpha}[2Y_S \sec^2\phi + Y_L(2RY_L - 4 - RY_S)] \tag{4.11}$$

$$\theta = \frac{\pi}{2} - \tan^{-1}\left[\frac{(RY_L - 2)}{2Y_A Z_B \tan\phi}\right] \tag{4.12}$$

The main objective of the above formulation is to reduce the number of free variables to be adjusted without heavily relying on computer optimization. And for a given set of circuit parameters (R_S, R_L, ϕ and α), the unknown values of Z_A, Z_B, Z_C and θ are simply a function of R only. Additional flexibility is offered by the selection of ϕ and α, which determine the locations of the transmission zeros. In practice, the rejection of the 2nd and 3rd harmonic frequencies ($\phi, \alpha \in 45°, 30°$) are highly desirable.

Two design examples will be discussed next. In Example 1, both input and output loads (R_S and R_L) are assumed to be 50 Ω, with ϕ = 45° and α = 30°. Impedance transformation will be demonstrated in Example 2, with R_S = 50 Ω, R_L = 75 Ω, ϕ = 30° and α = 45°.

4.3 Simulation Study

Design 1

The circuit parameters of this design (same input and output port impedance) are tabulated in Table 4.1. Subsequently, equations (4.9) – (4.12) can further be simplified as follows:

$$Z_A = Z_0 \sqrt{\beta \frac{2-\beta}{1+\beta-\beta^2}} \tag{4.13}$$

$$Z_B = Z_0 \sqrt{\beta(2-\beta)} \tag{4.14}$$

$$Z_C = Z_0 \sqrt{\frac{2-\beta}{3\beta}} \tag{4.15}$$

$$\theta = \frac{\pi}{2} - \tan^{-1}\left[\frac{\beta-1}{\sqrt{1+\beta-\beta^2}}\right] \tag{4.16}$$

$$\beta = \frac{R}{2Z_0} < \frac{1+\sqrt{5}}{2} \tag{4.17}$$

R_S	R_L	ϕ	α
50 Ω	50 Ω	45°	30°

Table 4.1 Circuit parameters of the proposed power divider (Example 1)

Based on the above formulas, the variation of the line impedances and θ as a function of β was calculated and plotted in Figure 4.4.

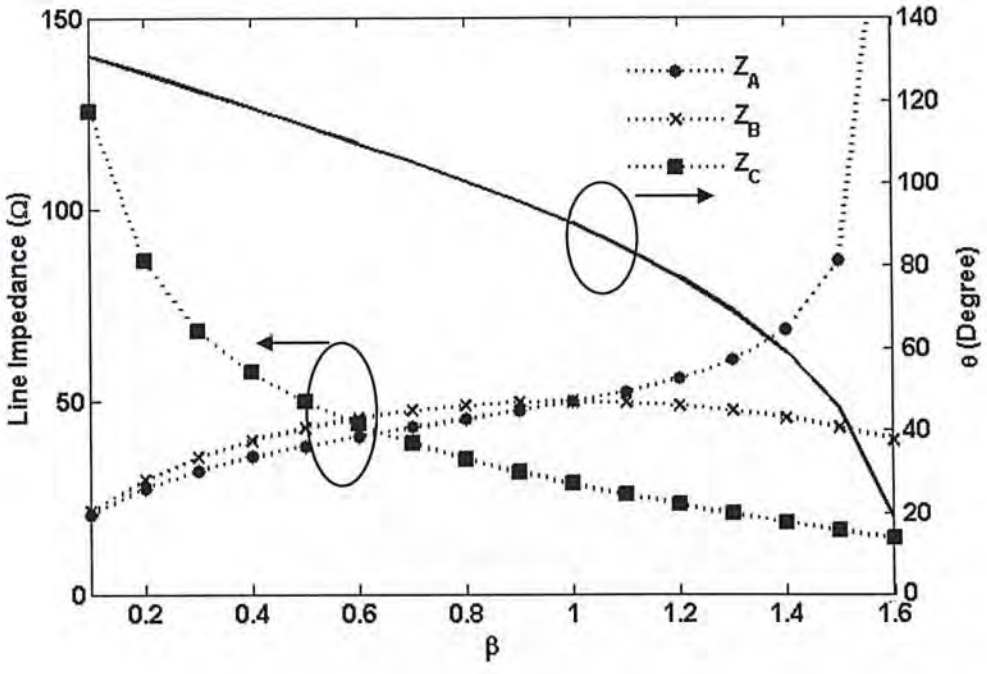
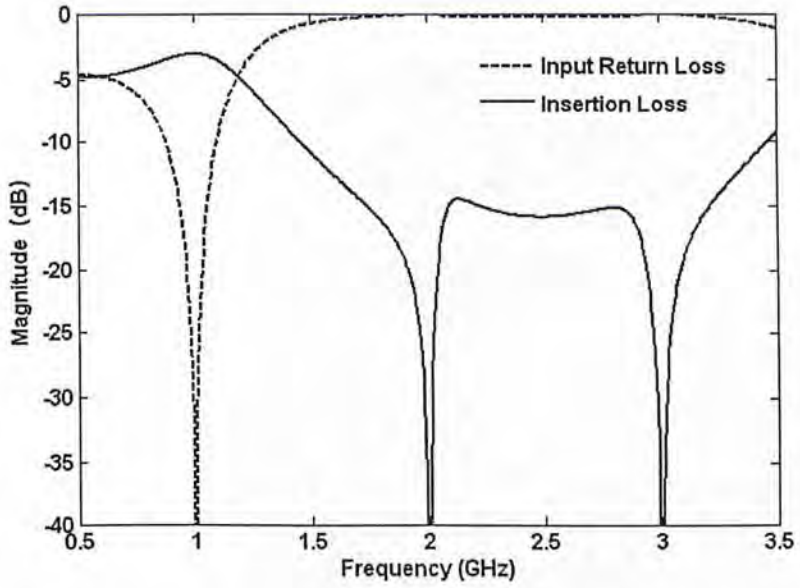
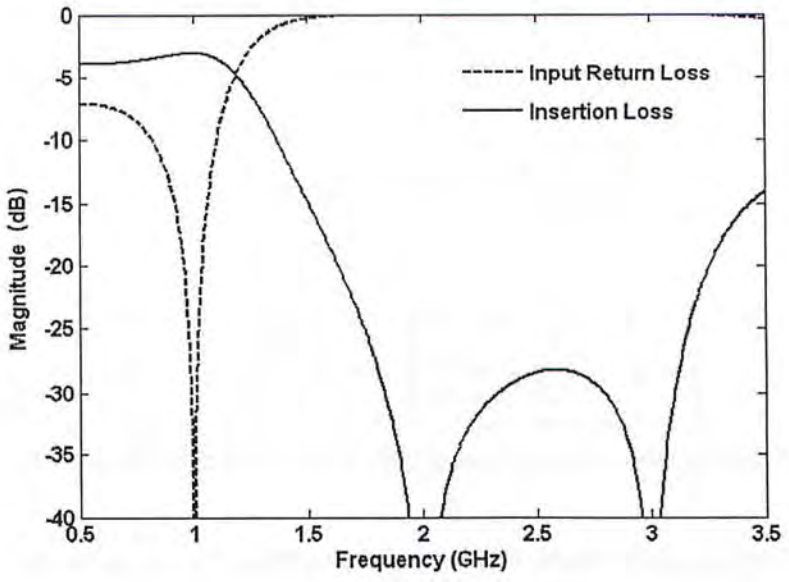


Figure 4.4 Line impedance and length versus β

Note that the value of θ decreases with increasing β. As a result, more compact circuit can be obtained by choosing a larger value of β (= $R/2Z_0$). Figure 4.5 shows the frequency responses (performed by circuit simulator) of the power divider with different values of β (only β = 0.6 and β = 1.5 were given here). It can be seen that there exists tradeoff between impedance values and the level of spurious suppression. And for β = 1.5 (0.6), the corresponding circuit parameters were found to be R = 150 Ω (60 Ω), Z_A = 86.6 Ω (41.2 Ω), θ = 45° (110°), Z_B = 43.3 Ω (45.8 Ω) and Z_C = 16.7 Ω (44.1 Ω).



(a) β = 0.6



(b) $\beta = 1.5$

Figure 4.5 Simulated responses of the proposed divider

Design 2

Table 4.2 lists the circuit parameters of the second design with different source and load impedances. Accordingly, the design equations can be rewritten as:

$$r_S = \frac{R_S}{R_L} \tag{4.18}$$

$$r = \frac{R}{2R_L} \tag{4.19}$$

$$z_B = \sqrt{r(4-3r)} \tag{4.20}$$

$$Z_B = z_B \cdot R_L \tag{4.21}$$

$$y_C = \frac{3(r-1)(2r_S-1)+1}{\sqrt{3}\, r_S\, z_B} \tag{4.22}$$

$$Z_C = \frac{R_L}{y_C} \tag{4.23}$$

$$y_A = \sqrt{\frac{1}{2r_S} + \frac{4-3r}{2\sqrt{3}\, z_B} y_C + \frac{1-r}{z_B^{\,2}}} \tag{4.24}$$

$$Z_A = \frac{R_L}{y_A} \tag{4.25}$$

$$\theta = \frac{\pi}{2} - \tan^{-1}\left[\sqrt{3}\frac{r-1}{y_A z_B}\right] \tag{4.26}$$

R_S	R_L	ϕ	α
50 Ω	75 Ω	30°	45°

Table 4.2 Circuit parameters of the proposed power divider (Example 2)

As a result, the circuit parameters (i.e. line impedances and θ) are simply a function of R only (Figure 4.6). It is observed that large value of R is performed for compact size (small θ). Figure 4.6 shows the corresponding simulated frequency responses of the power divider with r = 1.21. For illustration, simulations were perferred in the presence of a fixed R_L (= 75 Ω) and a frequency-dependent R_L (converted from a 50 Ω load using a quarter-wavelength impedance transformer). According to Figure 4.7, only slight influence is introduced by the output impedance transformer. It was observed that a reasonable choice of R is approximately 182 Ω for tradeoffs between size, spurious suppression and line impedance range.

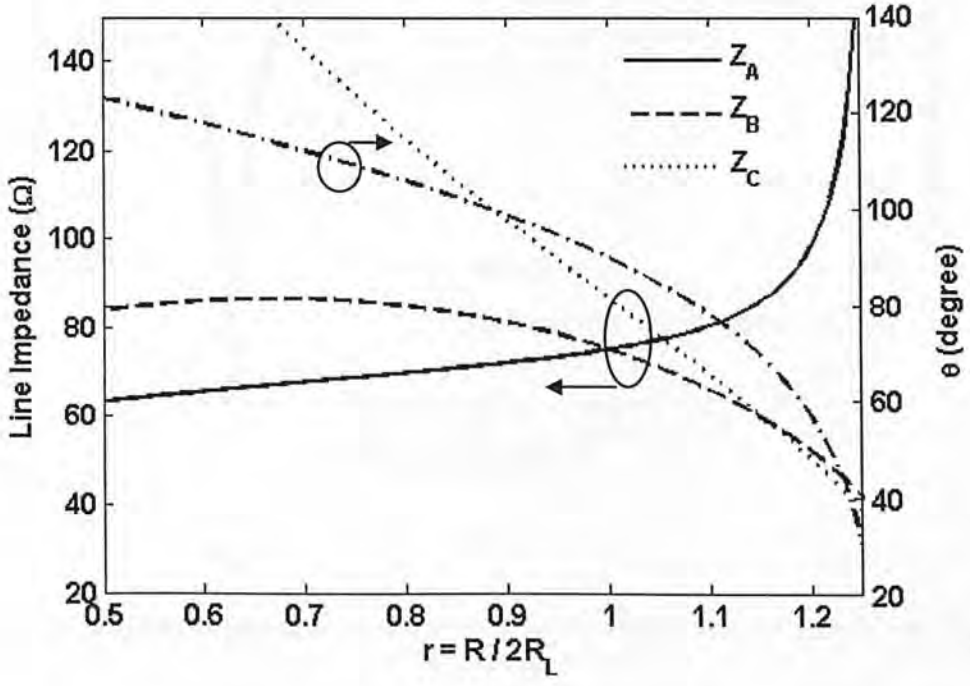
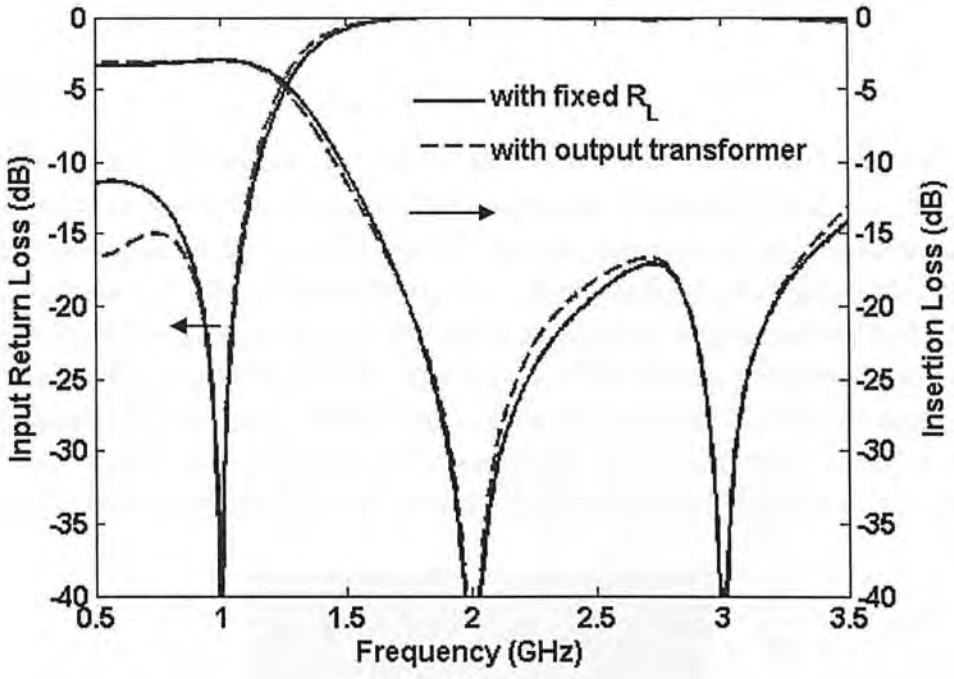
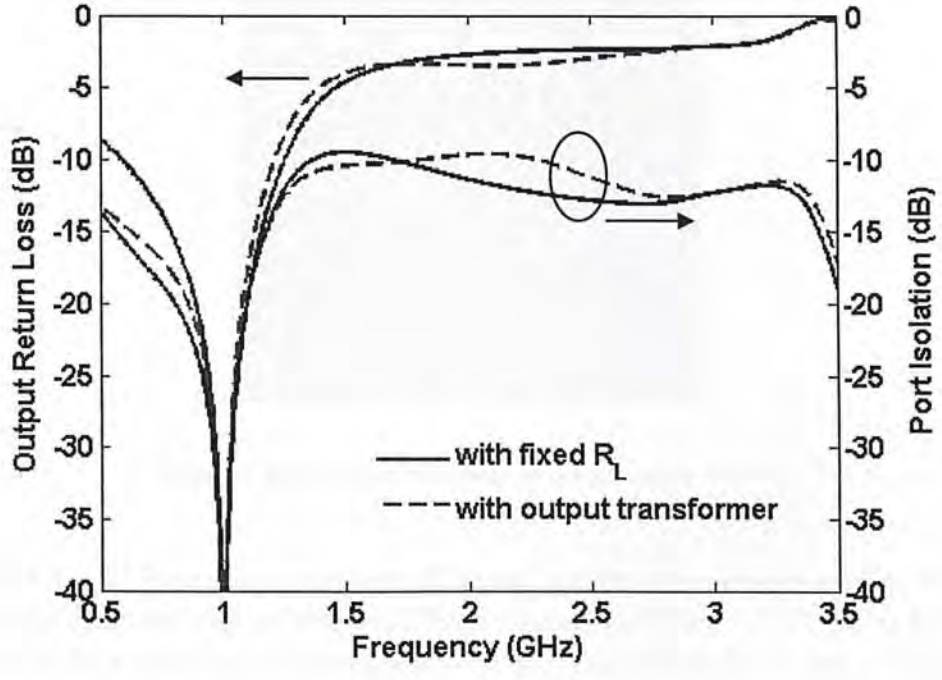


Figure 4.6 Calculated circuit parameters versus *r*



(a)



(b)

Figure 4.7 Simulated frequency responses of the proposed divider with $r = 1.21$, $R_S = 50\ \Omega$, and $R_L = 75\ \Omega$

4.4 Experimental Verification

Design 1

For experimental verification, a power divider designed to operate at 1 GHz ($\beta = 1.5$) was prototyped and characterized. For increased simulation accuracy, the ideal resistor was replaced by a more realistic model provided by the manufacturer to reflect the parasitic effect of packaging. An electromagnetic simulator (Momentum) was employed to take into account the effect of junction discontinuities at the layout level. Figure 4.8 illustrates the physical layout of the circuit prototype. This circuit was fabricated on Duroid substrate with a dielectric constant of 3.38 and thickness of 0.813 mm. Scattering parameter measurements were performed using a 4-port network analyzer (Agilent E5071A) over the frequency range from 0.5 to 3.5 GHz.

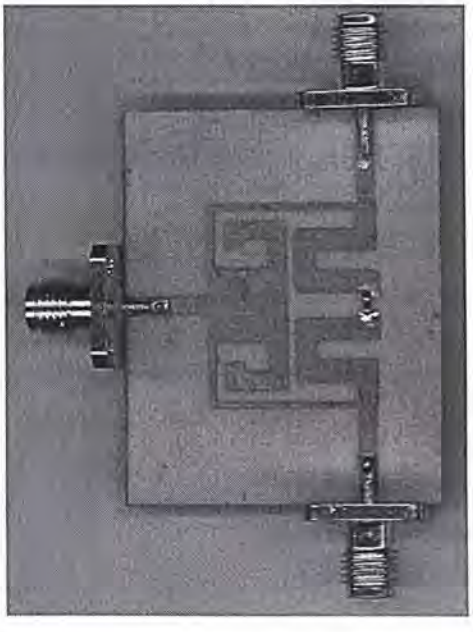


Figure 4.8 Simulated responses of the proposed divider

Figures 4.9 – 4.13 give the simulated (EM) and measured performance of the divider. Figure 4.9 indicates that a wide stop-band bandwidth (1.89 – 3.13 GHz) has been achieved with a minimum attenuation of –30 dB. The suppression levels, evaluated at the second- and third- harmonic frequencies (2.08 and 3.015 GHz), were both below – 40 dB. Within the fundamental pass-band, the divider was found to exhibit an insertion loss of 3.15 ± 0.07 dB, minimum output return loss/port isolation of – 20dB and minimum input return loss of – 15 dB over a fractional bandwidth of about 15 %. It is believed that the small discrepancies between the simulated and measured results were mainly caused by the fabrication tolerances as well as the parasitic effect of the surface-mounted resistor.

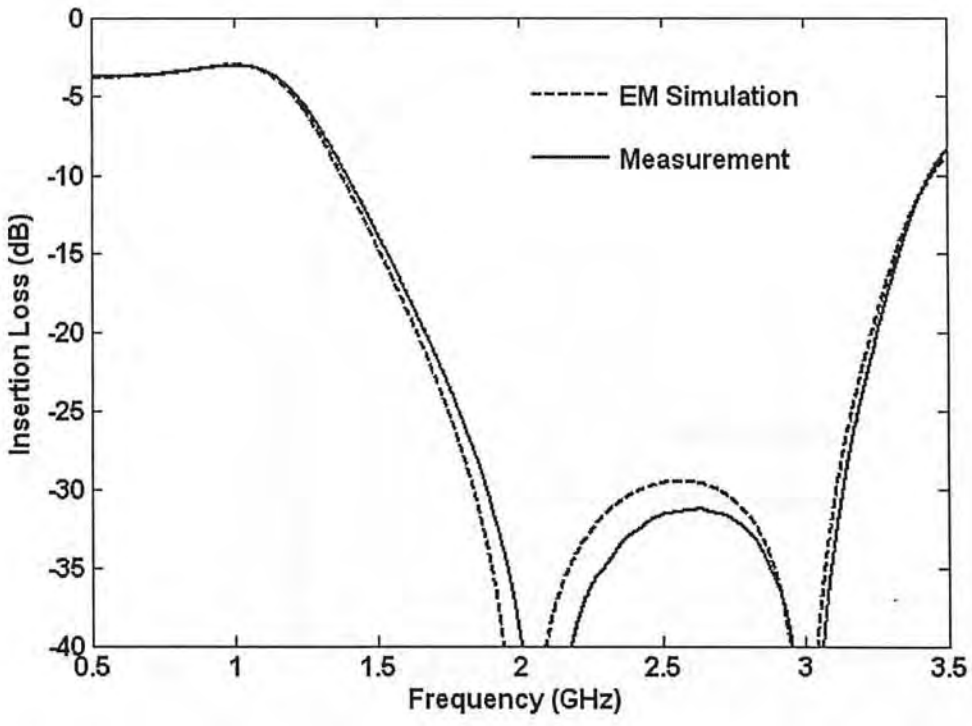


Figure 4.9 Simulated and measured insertion loss

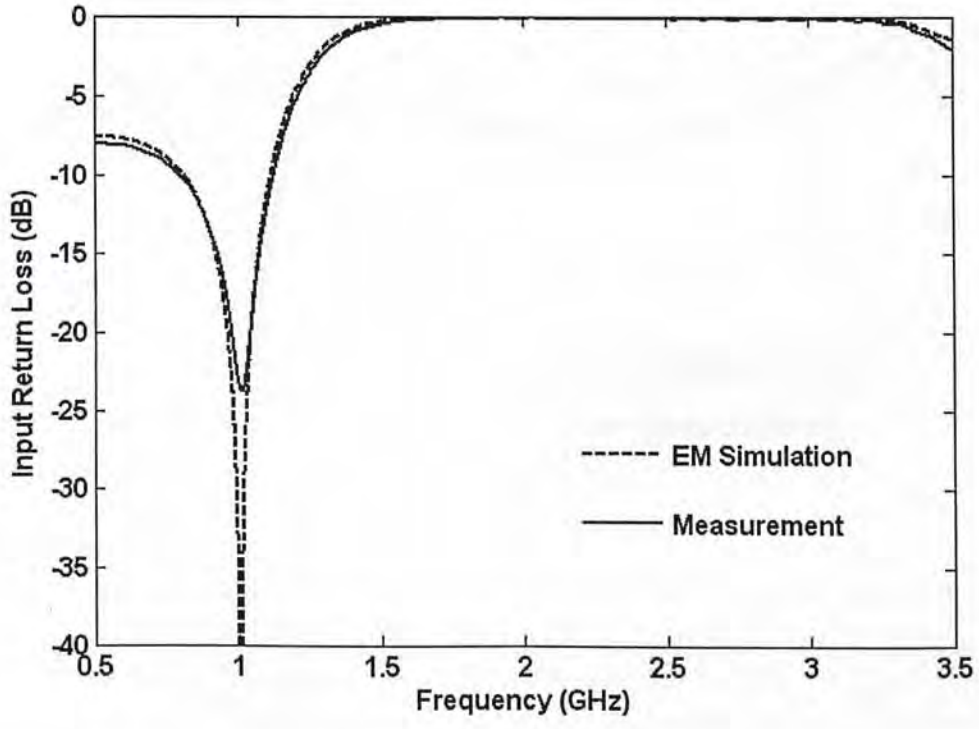


Figure 4.10 Simulated and measured input return loss

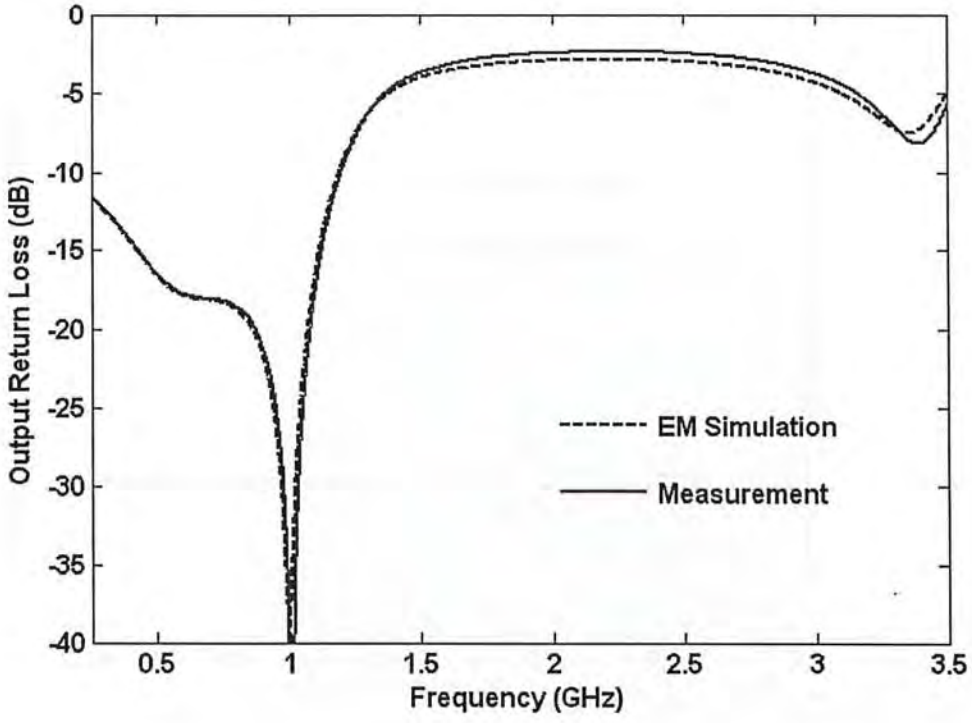


Figure 4.11 Simulated and measured output return loss

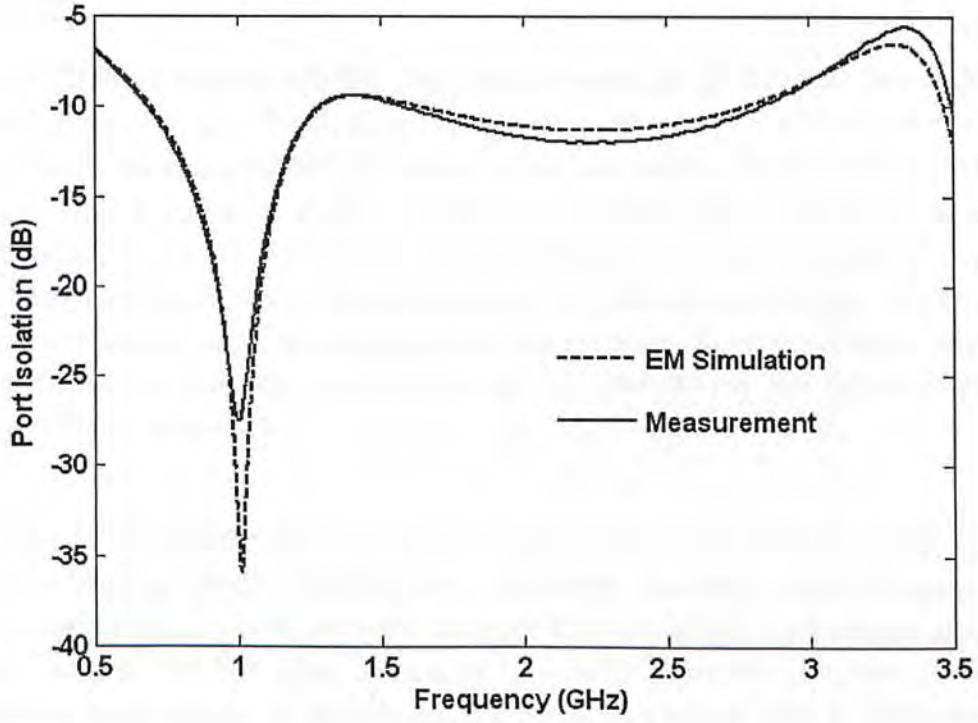


Figure 4.12 Simulated and measured port isolation

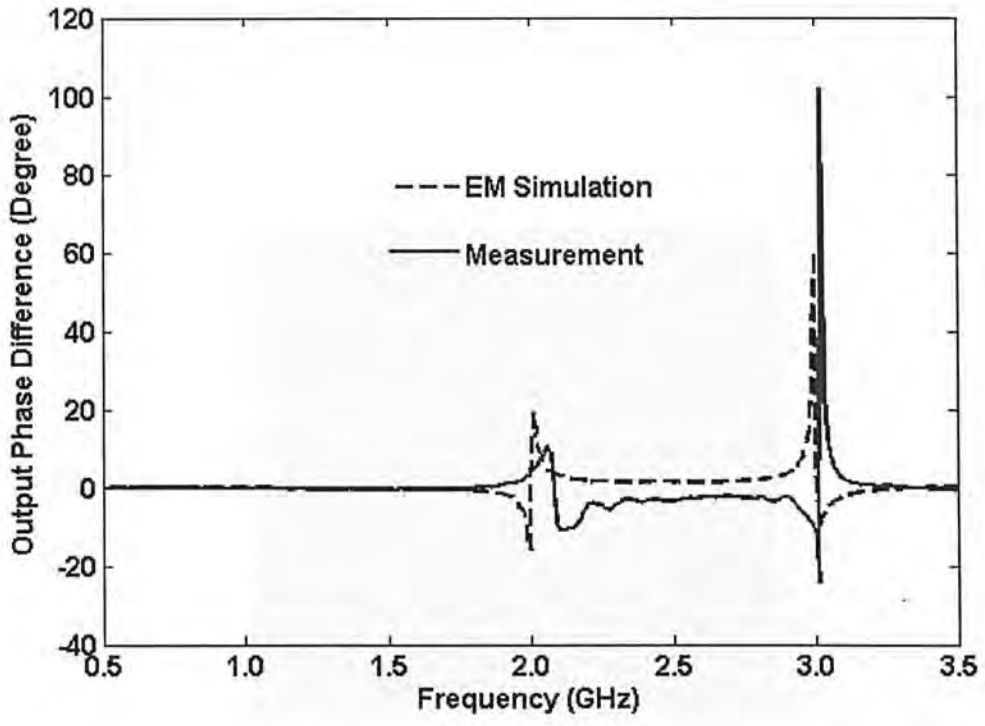


Figure 4.13 Simulated and measured output phase difference

Design 2

For verification, a power divider designed to operate at 1 GHz was prototyped and characterized with $R = 182\ \Omega$, $Z_A = 104.9\ \Omega$, $Z_B = 49.6\ \Omega$, $Z_C = 47.2\ \Omega$ and $\theta = 52.0°$. As a result, the characteristic impedance of the output transformer was chosen to be 61.2 Ω. This circuit was fabricated on Duroid substrate with a dielectric constant of 3.38 and thickness of 0.813 mm. In order to take into account the parasitic effects of junction discontinuities and lumped resistor, co-simulation based upon full-wave EM solver and device model was incorporated. Fine adjustment of the physical lengths of the branch-lines was then applied to tune the fundamental and transmission zero frequencies of the divider.

Figure 4.14 shows the top view of the prototype with a core area of roughly $\lambda_g/12$ by $\lambda_g/6$ (excluding output transformers). Scattering parameter measurements were performed using a 4-port network analyzer (Agilent E5071A) over the frequency range from 0.5 to 3.5 GHz. Figures 4.15 – 4.19 show the simulated (EM) and measured performance of the divider. Figure 4.15 indicates that a wide stop-band bandwidth (1.77 – 3.16 GHz) has been achieved with a minimum attenuation of –23 dB. The suppression levels, evaluated at 1.99 and 3.01 GHz, were well below –40 dB. Inside the fundamental band, the divider was found to exhibit an insertion loss of 3.28 ± 0.1 dB, minimum output return loss/port isolation of –20dB and minimum input

return loss of –15dB, over a fractional bandwidth of about 20%. It is believed that the small discrepancies between the simulated and measured results were mainly caused by the fabrication tolerances as well as the parasitic effect of the junction discontinuities and surface-mounted resistor.

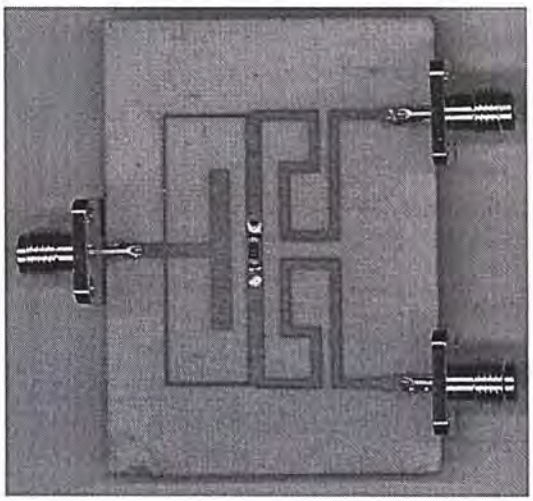


Figure 4.14 Photograph of the prototype (Example 2)

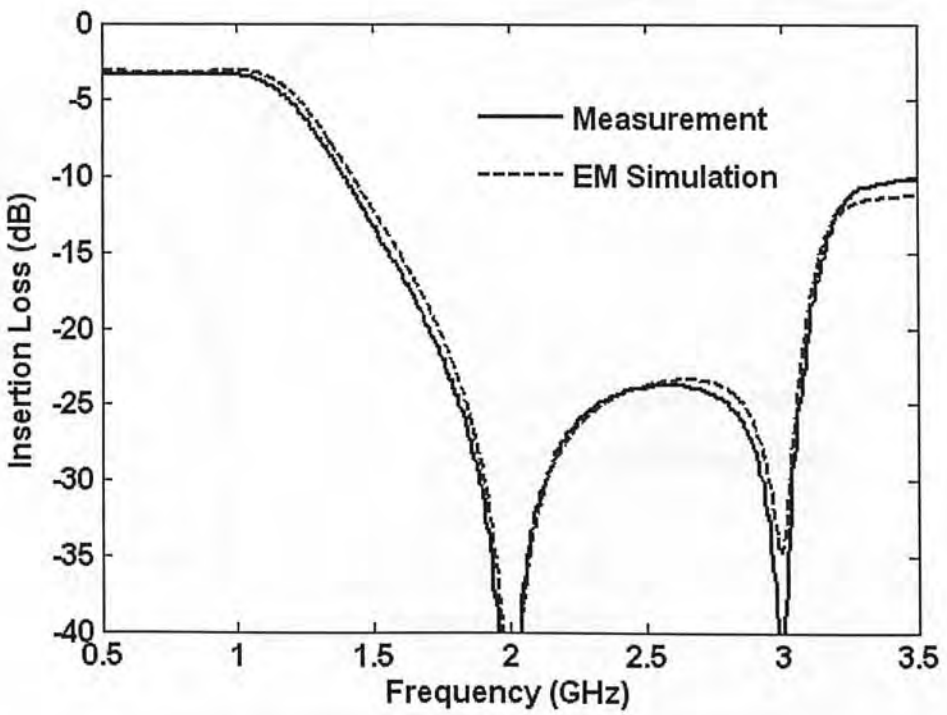


Figure 4.15 Simulated and measured insertion loss

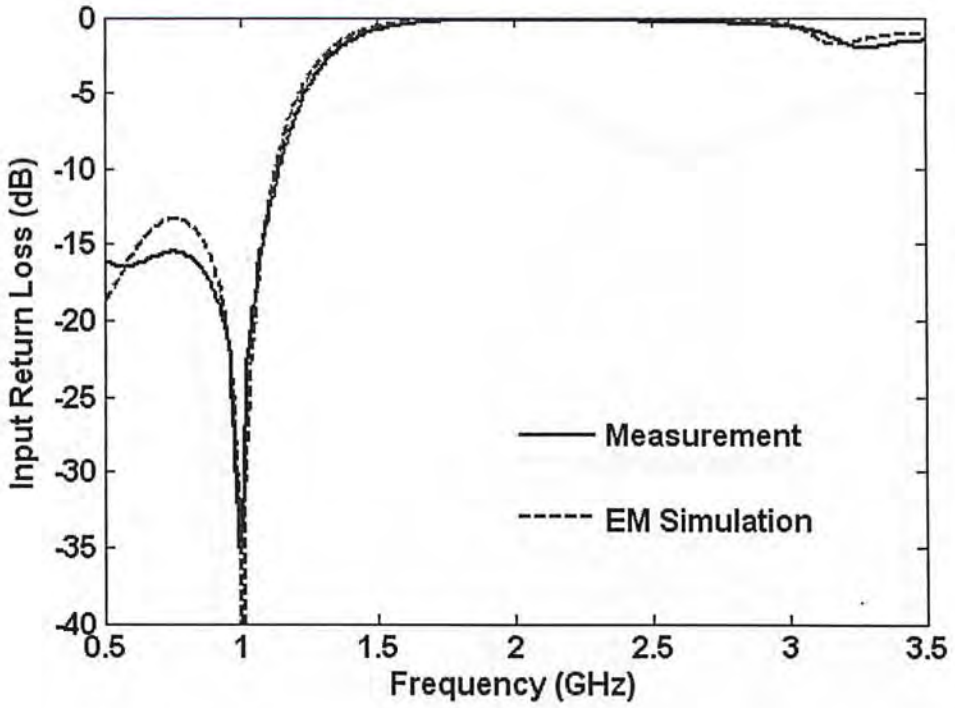


Figure 4.16 Simulated and measured input return loss

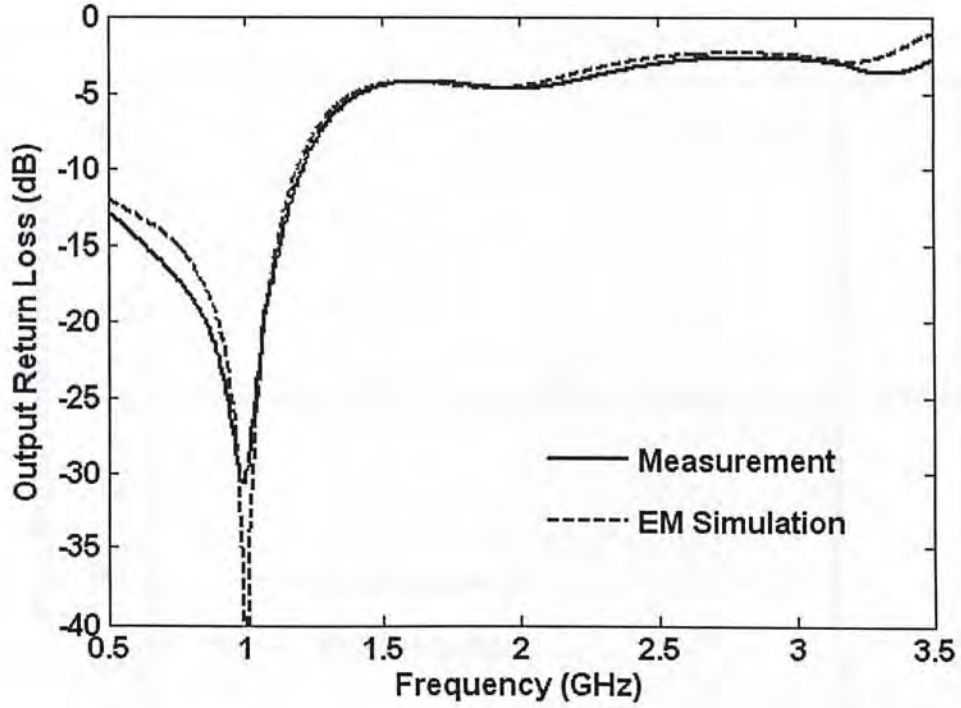


Figure 4.17 Simulated and measured output return loss

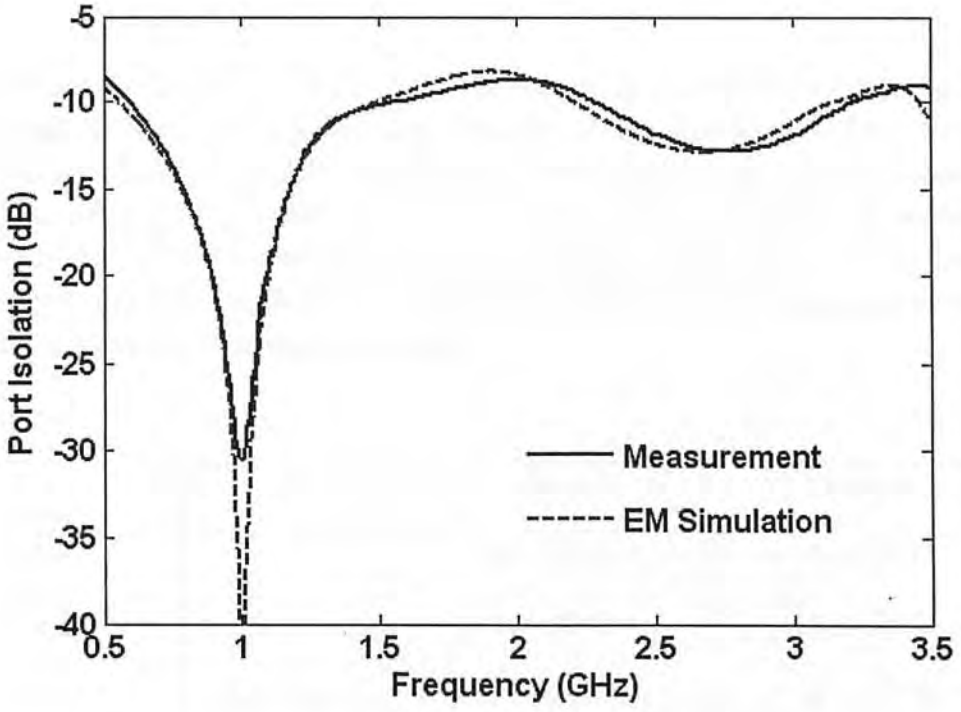


Figure 4.18 Simulated and measured port isolation

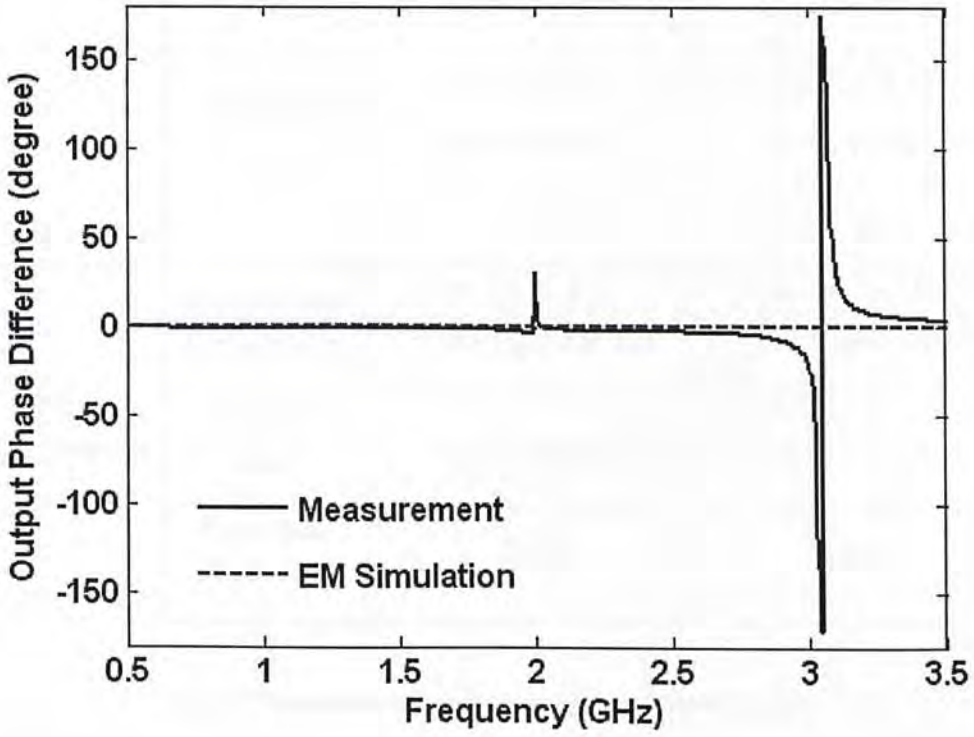


Figure 4.19 Simulated and measured output phase difference

4.5 Summary

The design principle of a novel power divider with impedance transformation and enhanced spurious rejection has been presented in this chapter. This circuit does not require any lumped reactive component, allows simple and flexible layout to be constructed and is compact in size. Excellent results have been experimentally demonstrated, which includes high level of harmonic suppression, low insertion loss, and small output phase difference. Table 4.3 summarizes the circuit parameters and performances of the two design examples.

		Example 1	Example 2
Circuit Parameters	Selected	$R_S = 50\ \Omega$ $R_L = 50\ \Omega$ $R = 150\ \Omega$ $\phi = 45°$ $\alpha = 30°$	$R_S = 50\ \Omega$ $R_L = 75\ \Omega$ $R = 182\ \Omega$ $\phi = 30°$ $\alpha = 45°$
	Calculated	$Z_A = 86.6\ \Omega$ $Z_B = 43.3\ \Omega$ $Z_C = 16.7\ \Omega$ $\theta = 45.0°$	$Z_A = 104.9\ \Omega$ $Z_B = 49.6\ \Omega$ $Z_C = 47.2\ \Omega$ $\theta = 52.0°$
Circuit Performances	Suppression Performance	*from* $2f_0$ *to* $3f_0$ $-30\,dB$ @ minimal	*from* $2f_0$ *to* $3f_0$ $-23\,dB$ @ minimal
	Insertion Loss	$3.15 \pm 0.07dB$	$3.28 \pm 0.1dB$
	Fractional Bandwidth	15 %	20 %

Table 4.3 Summary of the proposed power divider design

Chapter 5: New 2-way Power Divider Design with Extended Spurious Suppression

In the previous chapter, a new power divider was proposed with the introduction of transmission zeros located at the second and third harmonic frequencies. This design offers broadband spurious suppression without the need of backside etching or lumped reactive components. However, its major drawbacks are limited fundamental bandwidth (about 12 %) and the requirement of low impedance line (~ 17 Ω). In this chapter, a novel power divider with improved design and electrical performance is presented.

5.1 Proposed Topology

Figure 5.1 illustrates the schematic diagram of the proposed power divider, which consists of a resistor, several branch-line sections and open stubs. Unlike traditional designs, the two output ports are physically separated from each other by using two extended lines (Z_B), which helps to increase layout design flexibility and to reduce proximity effect. It is further assumed that Z_A, Z_B, ϕ, δ, ξ and ψ are free variables while Z_C, Z_D, θ and R are unknowns to be determined. By applying the even- and odd-mode formulation, these unknown parameters can simply be derived from the electrical properties of an ideal power divider (perfect return loss and port isolation) evaluated at the fundamental frequency (f_0).

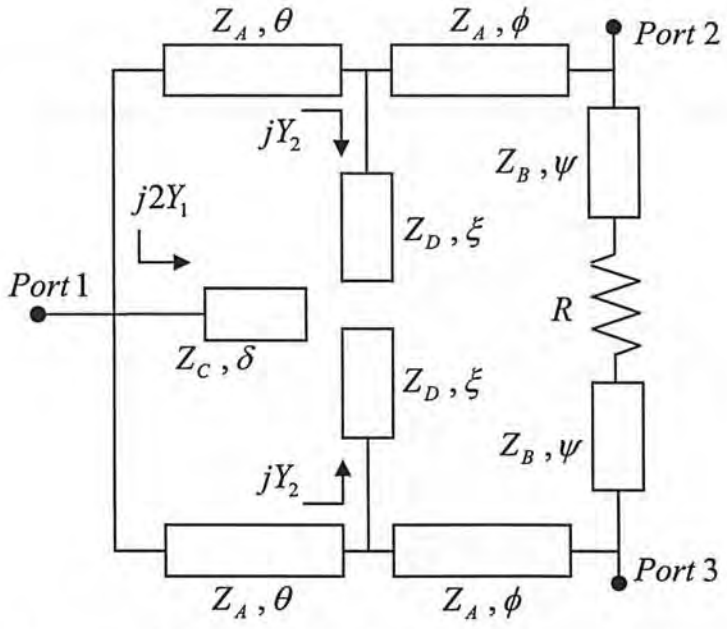


Figure 5.1 Circuit configuration of proposed power divider

5.2 Design and Analysis

Even-mode analysis

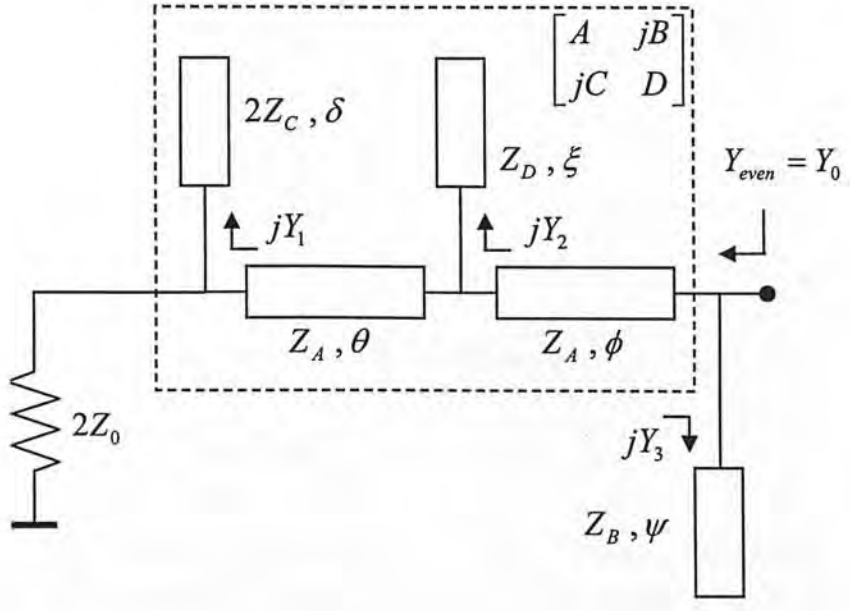


Figure 5.2 Equivalent circuit: even-mode

Figure 5.2 depicts the equivalent circuit of the proposed divider under even-mode excitation. The extended line (Y_B) and the two shunt stubs (Y_1 & Y_2) are responsible for the creation of three transmission zeros. For example, an electrical length of 45°,

30° or 22.5° (at f_0) corresponds to the suppression of the second, third or fourth harmonic frequencies, respectively. According to (5.1) – (5.3), these frequencies (f_{z1}, f_{z2} & f_{z3}) may be arbitrarily assigned by the proper selection of δ, ξ and ψ.

$$f_{Z1} = \frac{\pi}{2\delta} f_0 \tag{5.1}$$

$$f_{Z2} = \frac{\pi}{2\xi} f_0 \tag{5.2}$$

$$f_{Z2} = \frac{\pi}{2\psi} f_0 \tag{5.3}$$

For analysis purposes, the even-mode circuit may be regarded as the cascaded connection of a two-port network (boxed), a resistive load ($2Z_0$) and a shunt stub (Y_3). It is also known that, the output admittance of the even-mode circuit (Y_{even}) is equal to Y_0 at f_0. Mathematically, this admittance can be derived and expressed as follows:

$$Y_{even} = Y_0 = \frac{A\,Y_0 + j\,2\,C}{2\,D + j\,B\,Y_0} + j\,Y_3 \tag{5.4}$$

where

$$Y_1 = \frac{Y_C}{2} \tan\delta \tag{5.5}$$

$$Y_2 = Y_D \tan\xi \tag{5.6}$$

$$Y_3 = Y_B \tan\psi \tag{5.7}$$

$$\begin{bmatrix} A & jB \\ jC & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jY_1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\theta & jZ_A \sin\theta \\ jY_A \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ jY_2 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\phi & jZ_A \sin\phi \\ jY_A \sin\phi & \cos\phi \end{bmatrix} \tag{5.8}$$

By equating the real and imaginary, (5.4) can be rewritten as:

$$A = 2D + B\,Y_3 \tag{5.9}$$

$$Y_3 = Y_B \tan\psi \tag{5.10}$$

Odd-mode analysis

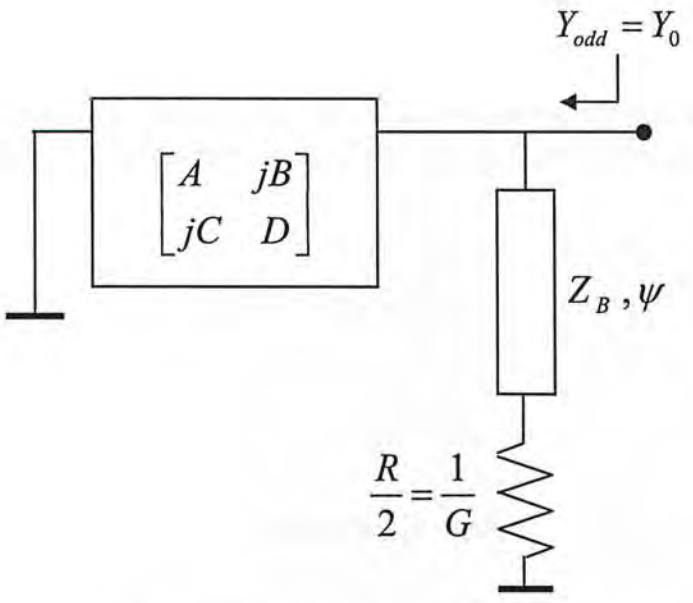


Figure 5.3 Equivalent circuit: odd-mode

Under odd-mode excitation, the equivalent circuit of the proposed divider is redrawn in Figure 5.3. With the assumption that the two output ports are perfectly matched and isolated, a second expression can thus be formulated as:

$$Y_{odd} = Y_0 = Y_B \frac{G + jY_B \tan\psi}{Y_B + jG \tan\psi} + \frac{A}{jB} \tag{5.11}$$

Similarly, the real and imaginary parts of (5.11) may be equated to give:

$$Y_0 = G\,Y_B{}^2 \frac{1 + \tan^2\psi}{Y_B{}^2 + G^2 \tan^2\psi} \tag{5.12}$$

$$\frac{A}{B} = Y_B \tan\psi \cdot \frac{Y_B{}^2 - G^2}{Y_B{}^2 + G^2 \tan^2\psi} \tag{5.13}$$

After some algebraic manipulations, equation (4.12) is reduced to (4.14) and (4.15).

$$\alpha = \frac{Z_0}{Z_B \sin 2\psi} \pm \sqrt{\left(\frac{Z_0}{Z_B \sin 2\psi}\right)^2 - 1} \tag{5.14}$$

$$R = \frac{2Z_B \tan\psi}{\alpha} \tag{5.15}$$

Subsequently, by solving (4.9), (4.10) and (4.13) in conjunction with the reciprocal property, the unknown coefficients (A, B, C and D) can thus be obtained as:

$$B = \pm Z_0 \sqrt{\frac{2}{1 + \alpha^2}} \tag{5.16}$$

$$D = -\frac{\alpha}{2} B Y_0 \tag{5.17}$$

$$A = B\,(Y_B \tan\psi - \alpha Y_0) \tag{5.18}$$

$$C = \frac{1 - AD}{B} \tag{5.19}$$

On the other hand, equation (4.8) may be re-arranged to give:

$$\begin{bmatrix} 1 & 0 \\ jY_1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\theta & jZ_A \sin\theta \\ jY_A \sin\theta & \cos\theta \end{bmatrix} = \begin{bmatrix} a & jb \\ jc & d \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ -jY_2 & 1 \end{bmatrix} \tag{5.20}$$

where

$$a = A\cos\phi + B\,Y_A \sin\phi \tag{5.21}$$

$$b = B\cos\phi - A\,Z_A \sin\phi \tag{5.22}$$

$$c = C\cos\phi - D\,Y_A \sin\phi \tag{5.23}$$

$$d = D\cos\phi + C\,Z_A \sin\phi \tag{5.24}$$

Finally, the expressions for the remaining parameters, as depicted in (5.25) – (5.27), are found by the expansion of equation (5.20) and comparing coefficients.

$$\theta = \sin^{-1}\left(\frac{b}{Z_A}\right) \tag{5.25}$$

$$Z_C = \frac{\tan\delta}{2Y_1} = \frac{\tan\delta}{2} \cdot \frac{b}{\cos\theta - d} \tag{5.26}$$

$$Z_D = \frac{\tan\xi}{Y_2} = \tan\xi \cdot \frac{b}{\cos\theta - a} \tag{5.27}$$

The main objective of the above formulation is to reduce the number of free variables to be adjusted without heavily relying on computer optimization. For a given set of circuit parameters (Z_A, Z_B, ϕ, δ, ξ and ψ), the unknown values of R, θ, Z_C and Z_D of the proposed structure can be calculated by using (5.14) – (5.19) and (5.21) – (5.27). The next step is to identify the optimal choice of circuit parameters with acceptable bandwidth and stop-band attenuation. The search also needs to take into account the physical constraints such as line impedance (e.g. 30 – 90 Ω) as well as small circuit size.

As mentioned before, additional flexibility is offered by the selection of δ, ξ and ψ, which determine the locations of the three transmission zeros. By permutation, there are a total of six possible arrangements. Note that the rejection of the 2nd, 3rd and 4th harmonic frequencies (δ, ξ, $\psi \in 22.5°$, 30°, 45°) are highly desirable in practice. Through circuit simulation, it is observed that when the distinct root (i.e. $\alpha = 1$) of equation (5.14) is employed, the operating bandwidth of the fundamental band can be substantially widened. As a result, we have

$$Z_B = \frac{Z_0}{\sin 2\psi} \tag{5.28}$$

It can also be proven that the selection of the positive sign in (5.16) will eventually lead to a compact solution with a smaller value of θ. And according to (5.27), for positive value of Z_D ($\cos\theta > a$), the lower bound of Z_A is given by (5.29).

$$Z_A > \frac{Z_0}{\sin 2\psi} \tag{5.29}$$

Figure 5.4 shows the transmission response (S_{21}) of the proposed circuit with different values of Z_A (other variables are kept constant). It is found that a higher Z_A is desirable for increased spurious suppression. Hence, Z_A should be given the highest achievable impedance for a selected fabrication process.

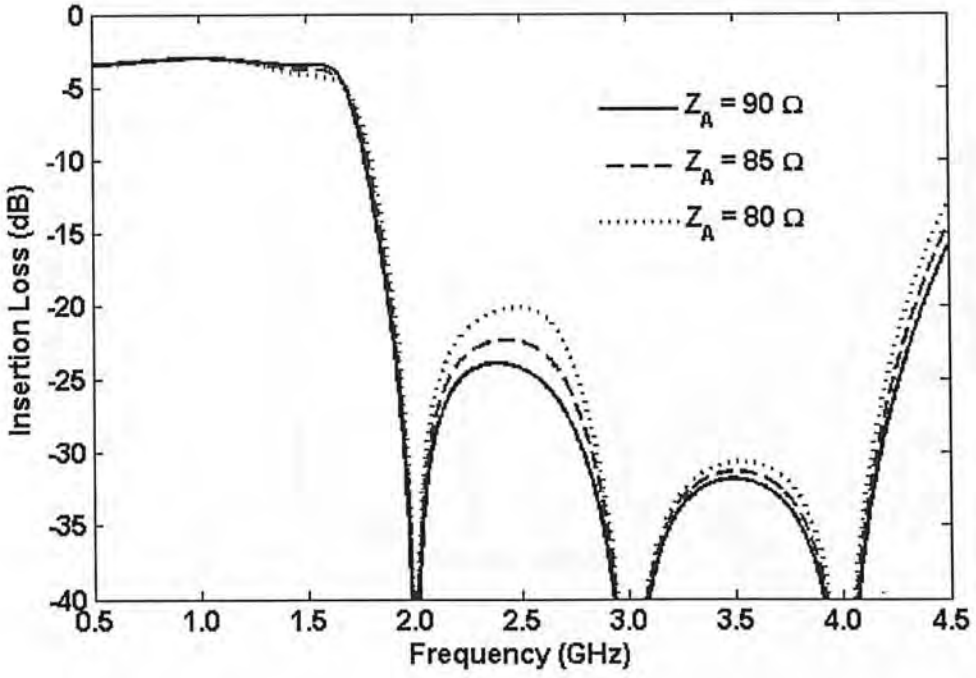


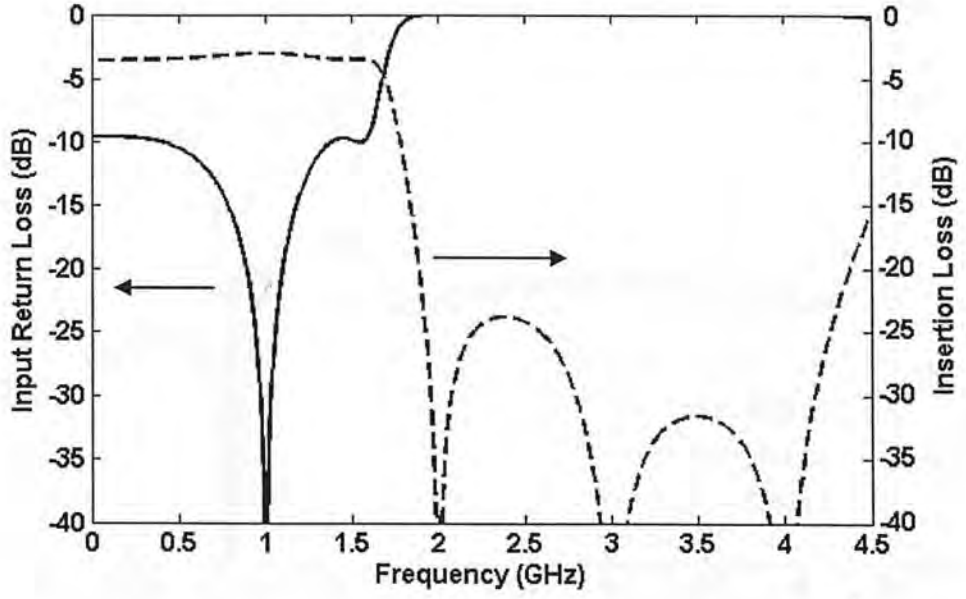
Figure 5.4 Insertion loss of the proposed structure with different choices of Z_A

5.3 Simulation Study

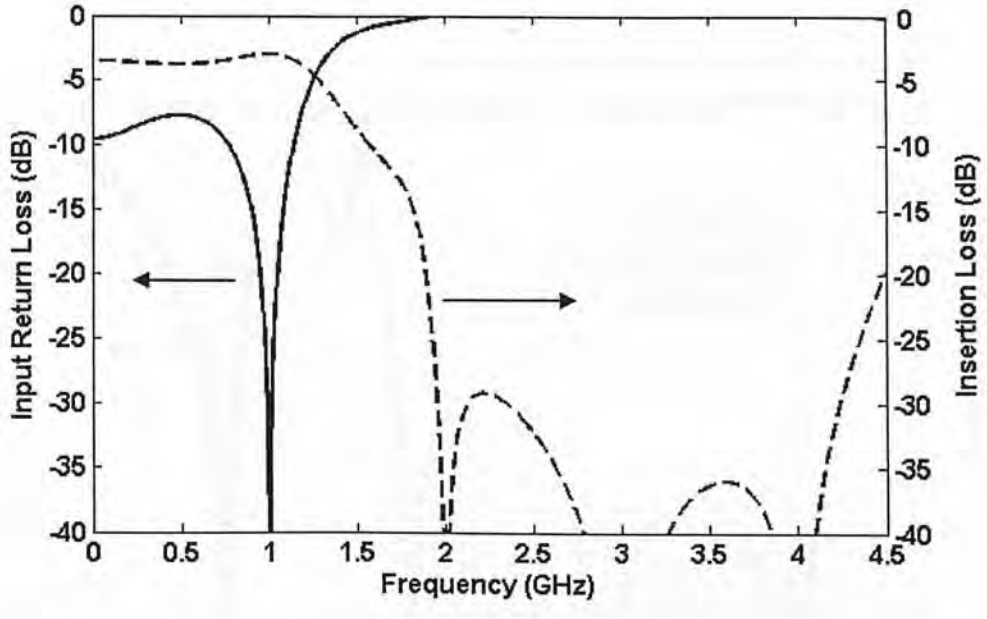
A simulation study has been carried out based upon different circuit permutations (δ, ξ, ψ) and ϕ value. For reference, the corresponding circuit parameters were calculated and tabulated in Table 5.1. For illustration, Figure 5.5 shows the simulated frequency responses of the designs. It is seen that the two designs exhibit some trade-off between available bandwidth and level of spurious suppression.

Circuit variables	Preferred value	Example 1	Example 2
δ, ξ, ψ	Defined by f_{Z1}, f_{Z2} and f_{Z3} with permutations	$\delta = 45°$ $\xi = 22.5°$ $\psi = 30°$	$\delta = 30°$ $\xi = 22.5°$ $\psi = 45°$
ϕ	$\phi < 90°$	32°	32°
Z_A	Maximum (fabrication)	90 Ω	90 Ω
θ, Z_B, Z_C, Z_D, R	Calculated from (14) – (19), (21)–(27) & (28)	$\theta = 47°$ $Z_B = 57$ Ω $Z_C = 86$ Ω $Z_D = 34$ Ω $R = 66.7$ Ω	$\theta = 28°$ $Z_B = 50$ Ω $Z_C = 37$ Ω $Z_D = 30$ Ω $R = 100$ Ω

Table 5.1 Circuit parameters of illustrative designs



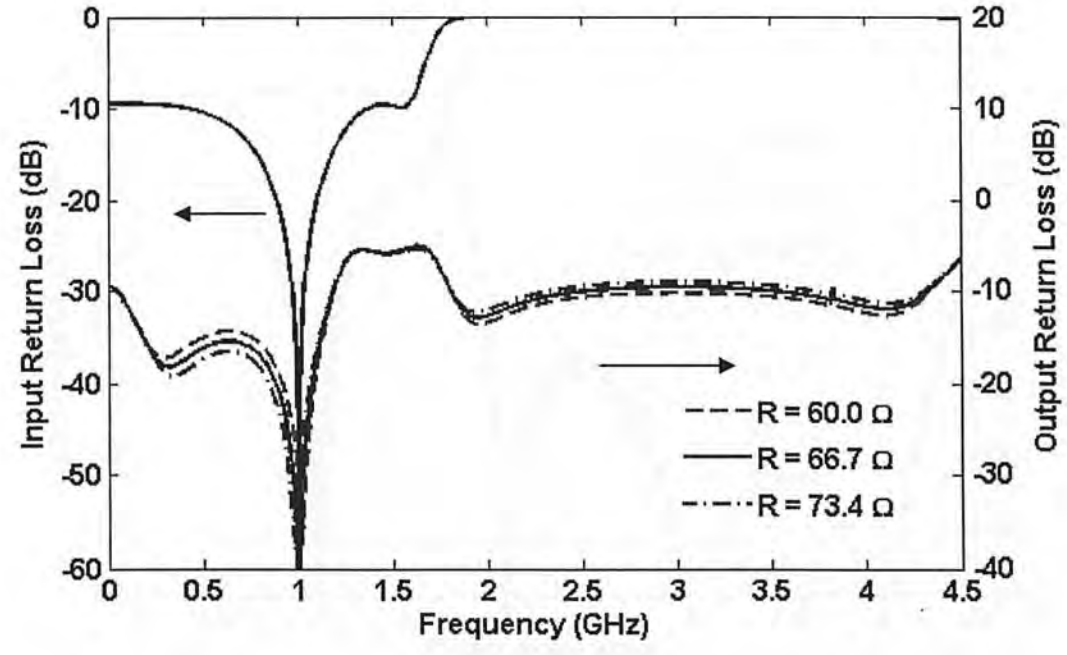
(a)



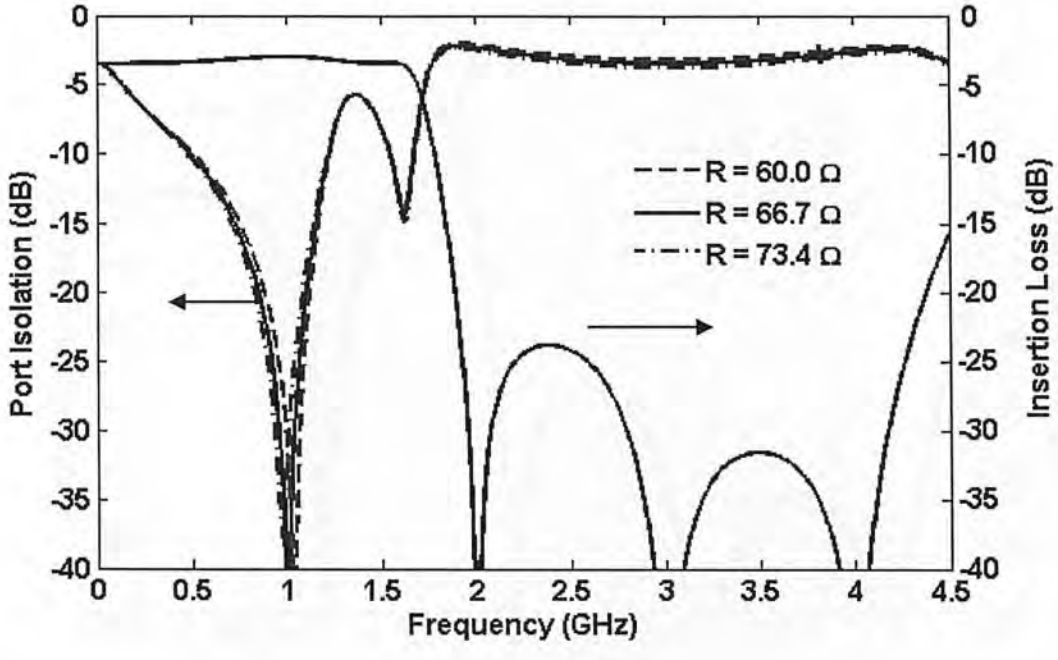
(b)

Figure 5.5 Simulated responses: (a) Example 1, (b) Example 2

In order to study the effect of fabrication tolerances on the RF performance of the proposed divider, further investigation was performed using circuit simulator. Figures 5.6 and 5.7 show the frequency plots of Example 1 versus variation in R ($\pm 10\%$) and Z_A ($\pm$ 5%). These graphs indicate that the performance of the proposed design is not severely affected by the uncertainties in circuit construction such as the precise values of line width and resistance.

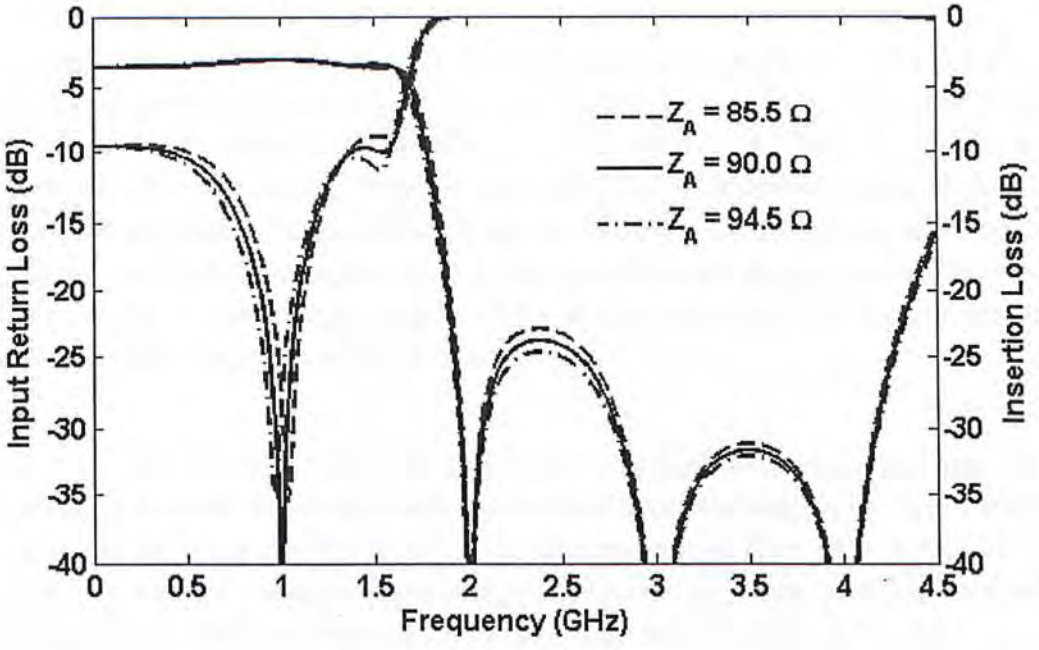


(a)

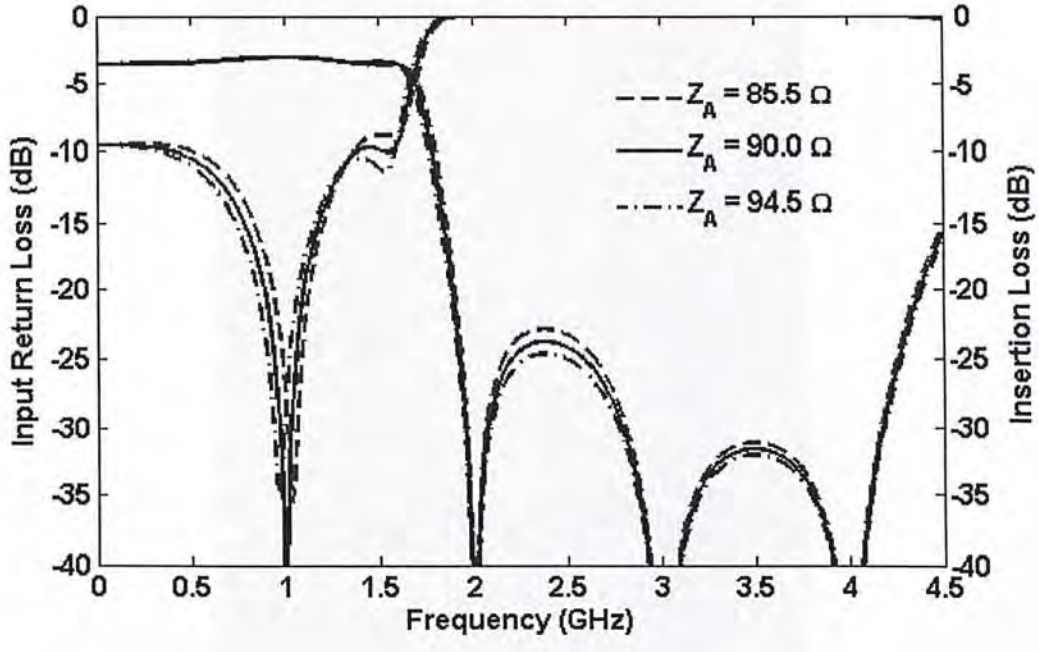


(b)

Figure 5.6 Simulated circuit performances versus *R*: (a) input and output return loss, (b) insertion loss and port isolation



(a)



(b)

Figure 5.7 Simulated circuit performances versus Z_A: (a) input and output return loss, (b) insertion loss and port isolation

5.3 Experimental Verification

For experimental verification, a power divider designed to operate at 1 GHz (Example 1) was prototyped and characterized. This circuit was fabricated on Duroid substrate with a dielectric constant of 3.38 and thickness of 0.813 mm. At first, an initial design was obtained from the derived formulas and confirmed with circuit simulator. And in order to accommodate the parasitic effects of junction discontinuities and lumped component, co-simulation based upon EM solver and device model was incorporated. Fine adjustment of the physical lengths of the branch lines was then applied, mainly to tune the centre frequency of the divider.

Figure 5.8 shows the top view of the physical layout with dimensions included. The core design was found to occupy a substrate area of approximately $\lambda_g/8 \times \lambda_g/6$. Further size miniaturization is possible through the meandering of lines (See Appendix 2). Scattering parameter measurements were performed by using a 4-port network analyzer (Agilent E5071A) over the frequency range from 10 MHz to 4.5 GHz.

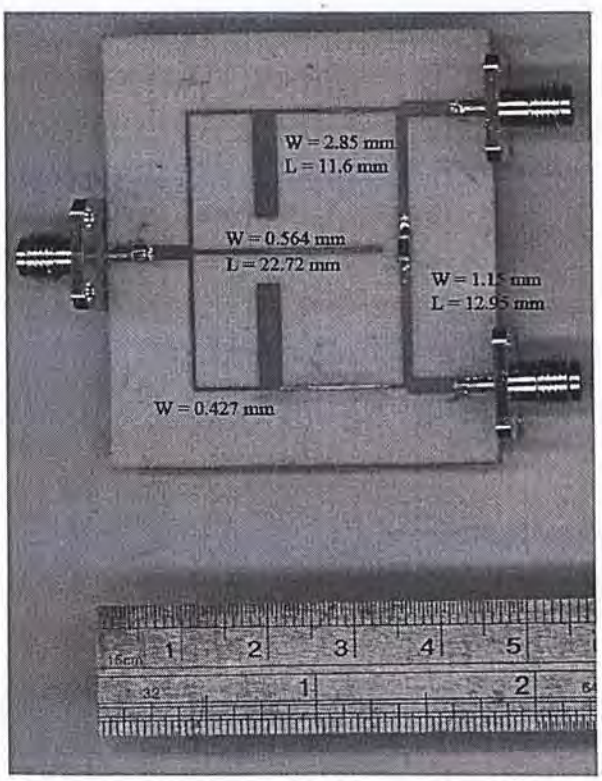


Figure 5.8 Photograph of the prototype (Example 1)

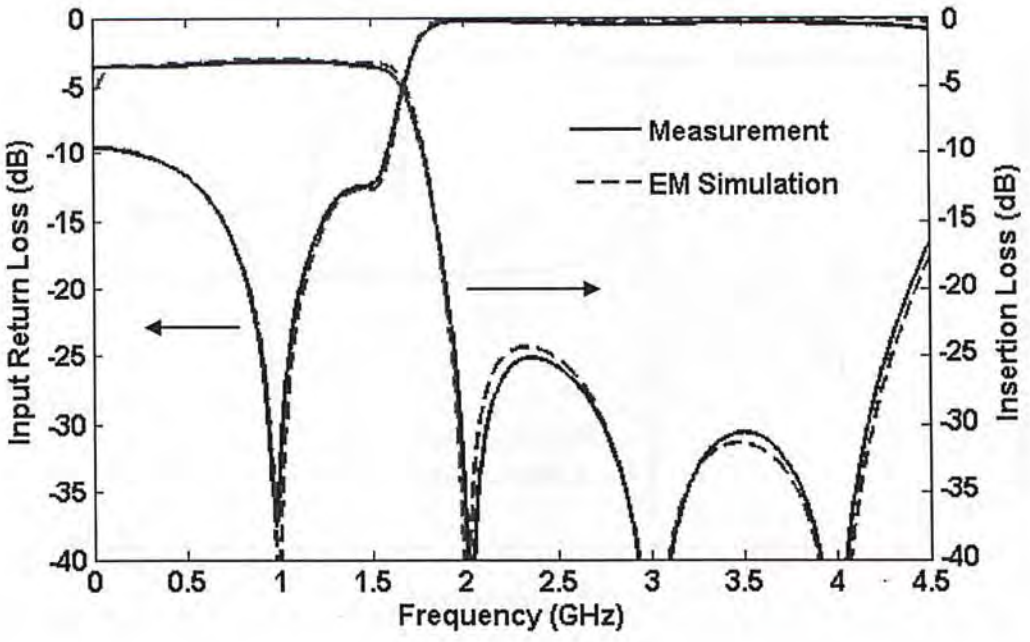


Figure 5.9 Simulated and measured insertion loss and input return loss

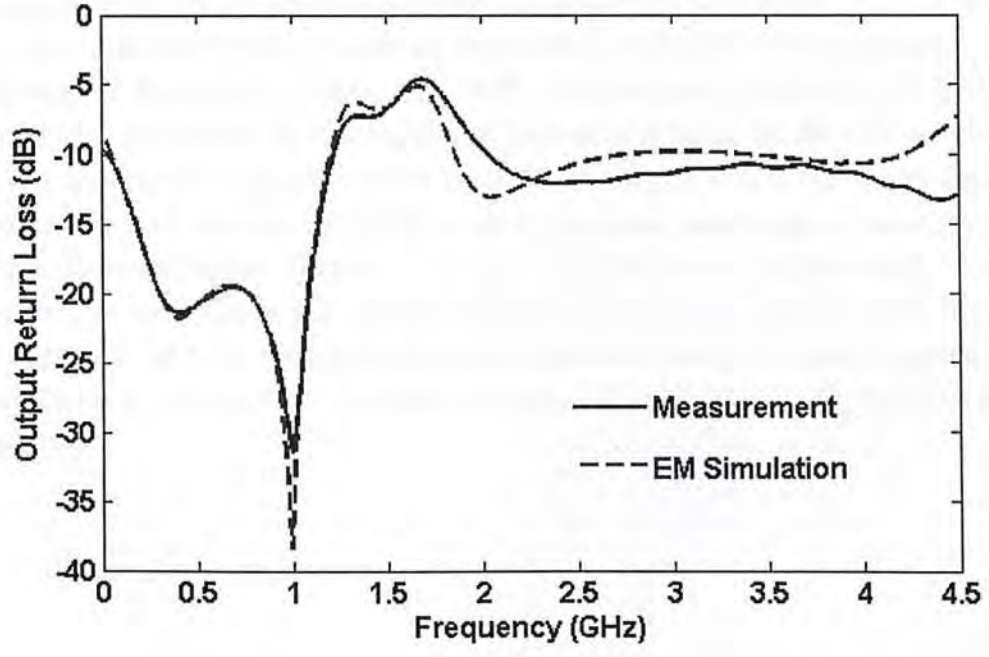


Figure 5.10 Simulated and measured output return loss

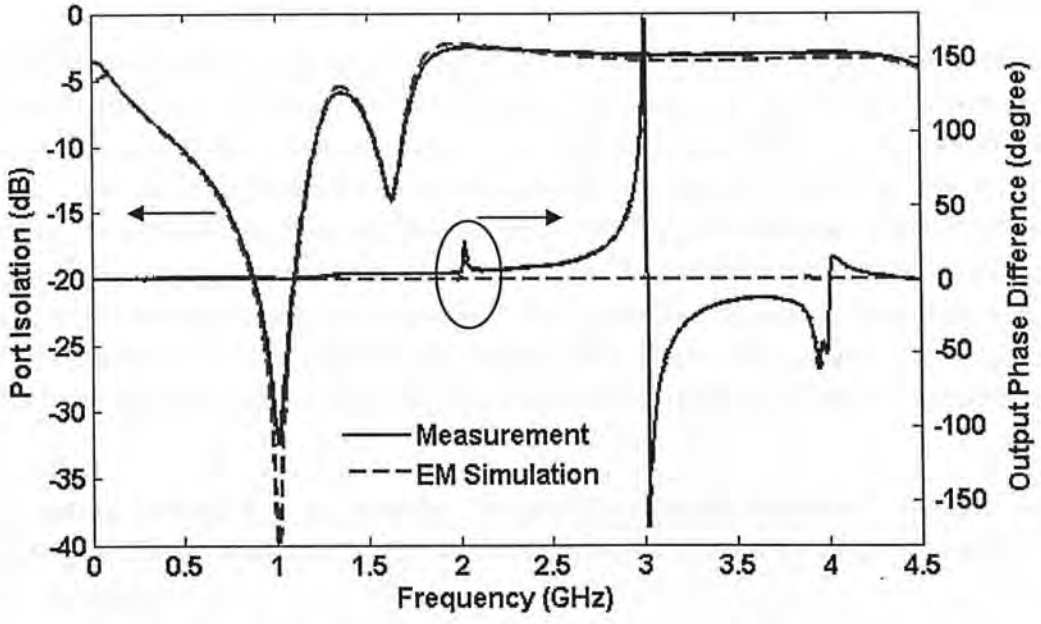


Figure 5.11 Simulated and measured port isolation and output phase difference

Figures 5.9 – 5.11 show the simulated (EM) and measured performance of the prototype. Figure 5.9 indicates that an octave stop-band bandwidth (1.94 – 4.26 GHz) has been achieved with a minimum attenuation of 25 dB. The suppression levels, evaluated at the second-, third- and fourth- harmonic frequencies (2.02, 3.01, 3.99 GHz), were well above 40 dB. Inside the fundamental band, the divider was found to exhibit an insertion loss of 3.25 $\pm$ 0.02 dB, minimum return loss (both input and output) and port isolation of 20 dB, over a fractional bandwidth of about 25%. The output phase difference (Figure 5.11) was found to be negligibly small, except at frequencies well above the second-harmonic band. It is believed that the small discrepancies between the simulated and measured results were mainly caused by the fabrication tolerances and the high frequency behaviour of the surface-mounted resistor.

5.4 Summary

The design and implementation of a novel power divider with enhanced suppression bandwidth has been described in this chapter. The proposed configuration does not require backside etching or lumped reactive component, and allows compact and low cost solution to be constructed. It offers several advantages including: (a) simple structure with moderate line impedance (30 – 90 Ω), (b) flexible layout with an occupied area of approximately $\lambda_g/8 \times \lambda_g/6$, (c) a fundamental bandwidth of almost 25%, and (d) enhanced spurious attenuation (> 25 dB) over an octave frequency range with the presence of three controllable transmission zeros. This design can easily be scaled up in frequency due to the adoption of microstrip lines of moderate impedance.

More design examples (e.g. meander structure; enhanced stop-band response) are illustrated in Appendix 2, and a brief summary of some previously reported designs is given in Appendix 3.

Chapter 6: New 2-way Unequal Power Divider Design with Dual-harmonic Rejection

This chapter presents a novel design of unequal power divider with dual-harmonic rejection. Closed-form design formulas are made available for circuit parameter extraction. The proposed circuit features simple construction and wide spurious suppression bandwidth. Simulated and experimental results of a fabricated prototype implemented on microstrip are given for validation.

6.1 Proposed Topology

Figure 6.1 shows the schematic diagram of the proposed power divider, which consists of four branch-line sections, an open stub and a resistor. All electrical lengths are specified at the fundamental frequency (f_0). Structurally speaking, it is similar to the one described in Chapter 4 but it is asymmetric in structure for unequal power division. By the proper selection of the line impedances and electrical lengths, the proposed circuit is made to offer both unequal dividing ratio and dual-harmonic rejection capabilities. For analysis purposes, it is further assumed that the two output ports are terminated by R_L and k^2R_L. Moreover, the input stub is designed to exhibit a low impedance value at $3f_0$ for third-harmonic suppression. Under the conditions that the input power is divided unequally between the two output loads, with a power dividing ratio of k^2 ($k > 1$) and zero power dissipation in R, the following relation can thus be established.

$$\frac{Z_B}{Z_A} = \frac{Z_2}{Z_1} = k^2 \tag{6.1}$$

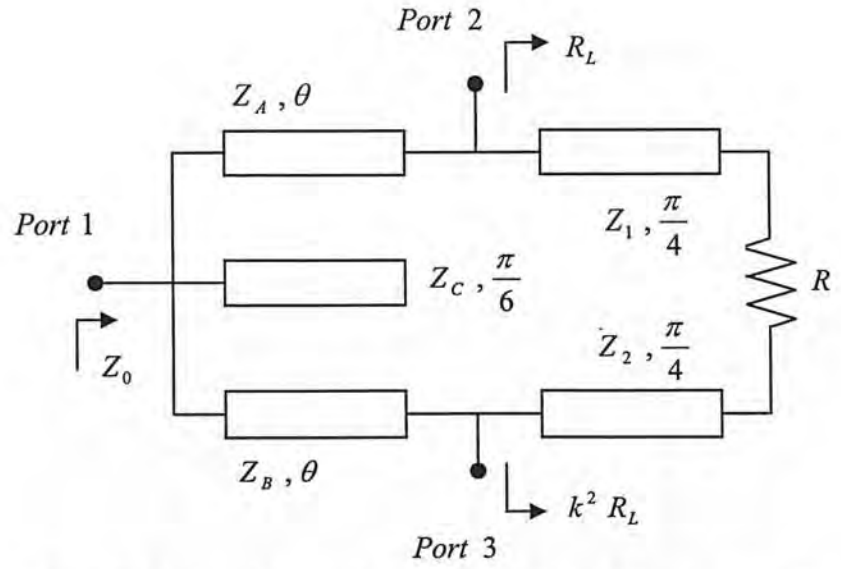


Figure 6.1 Proposed unequal power divider with harmonic rejection

6.2 Design and Analysis

The circuit representation of the proposed power divider evaluated at $2f_0$ is illustrated in Figure 6.2. It can also be shown that the two output ports appear as virtual grounds ($V_2 = V_3 = 0$) due to the presence of the two open stubs, which lead to rejection of second harmonic band.

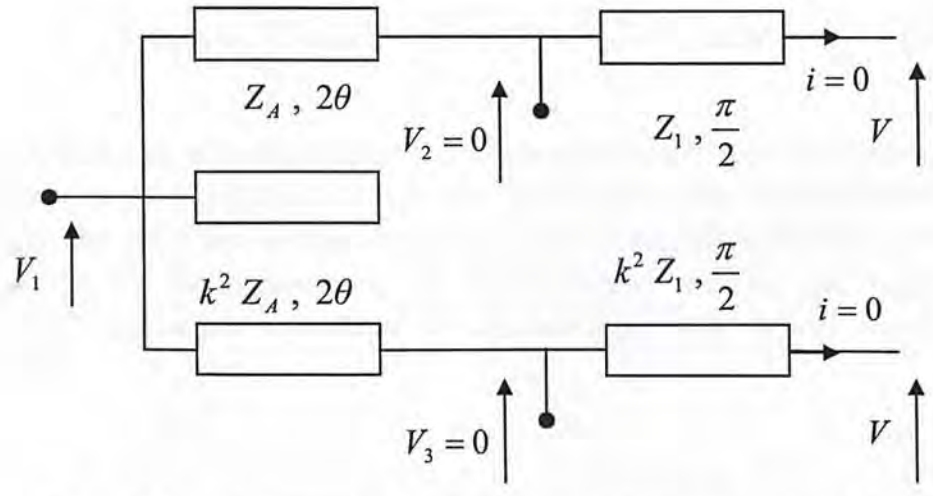


Figure 6.2 Circuit representation of the proposed divider evaluated at $2f_0$

If the two output ports (Figure 6.1) are excited by a pair of in-phase signals (voltage ratio of 1), the proposed divider circuit may be reduced to the one shown in Figure 6.3. Under the ideal return loss and port isolation conditions, we have:

$$\frac{1}{R_L} = jY_1 + Y_A \frac{\frac{k^2}{1+k^2}\left(Y_0 + \frac{jY_C}{\sqrt{3}}\right) + jY_A \tan\theta}{Y_A + \frac{jk^2}{1+k^2}\left(Y_0 + \frac{jY_C}{\sqrt{3}}\right)\tan\theta} \tag{6.2}$$

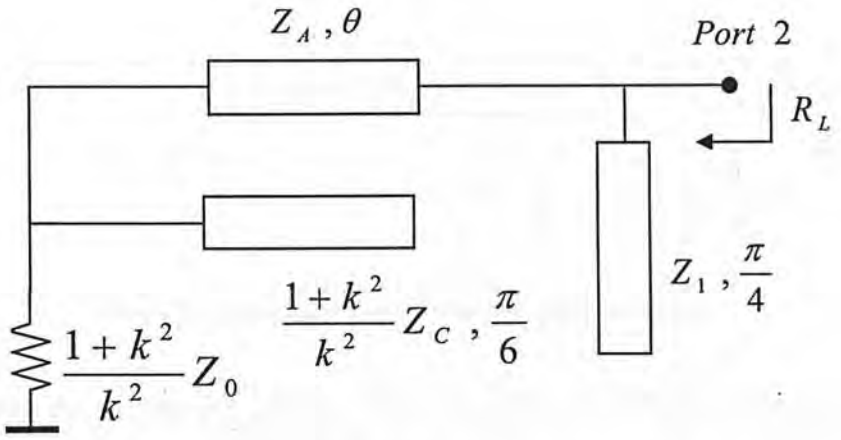


Figure 6.3 Equivalent circuit with in-phase excitation

By equating the real part and imaginary parts of (6.2), one obtains

$$\frac{1+k^2}{k^2}\left(\frac{Y_A}{R_L}\right) - \frac{Y_C}{\sqrt{3}R_L}\tan\theta + Y_0 Y_1 \tan\theta = Y_0 Y_A \tag{6.3}$$

$$\frac{Y_0}{R_L}\tan\theta + \frac{Y_1 Y_C}{\sqrt{3}}\tan\theta - \frac{1+k^2}{k^2} Y_1 Y_A = \frac{1+k^2}{k^2} Y_A^2 \tan\theta + \frac{Y_A Y_C}{\sqrt{3}} \tag{6.4}$$

Figure 6.4 shows the equivalent circuit of the power divider (Figure 6.1) with a pair of anti-phase excitation (voltage ratio of $-k^2$). By the principles of superposition and reciprocity, the combined voltage appearing at the input port is virtually zero (V_1). Subsequently, by the enforcement of the ideal port isolation and return loss requirements, the output admittance of the resulting network can therefore be expressed as:

$$\frac{1}{R_L} = -jY_A \cot\theta + Y_1 \frac{1+k^2 + jY_1 R}{Y_1 R + j(1+k^2)} \tag{6.5}$$

Similarly, the real and imaginary parts of (6.5) may be equated to give:

$$\frac{RY_1}{R_L(1+k^2)} - Y_A \cot\theta = Y_1 \tag{6.6}$$

$$RY_1Y_A \cot\theta + \frac{1+k^2}{R_L} = R_1Y_1^2 \tag{6.7}$$

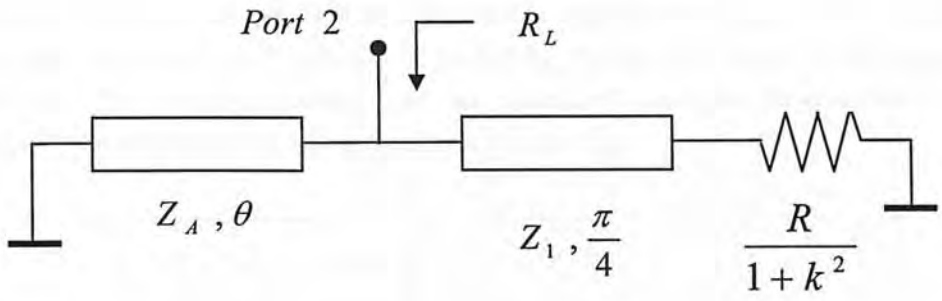


Figure 6.4 Equivalent circuit with anti-phase excitation

Consequently, by solving (6.1), (6.3) – (6.4) and (6.6) – (6.7), the circuit parameters of the proposed design can thus be derived as:

$$\alpha = \frac{1-\frac{1+k^2}{r}}{\sqrt{2\frac{1+k^2}{r}-1}} \tag{6.8}$$

$$Z_1 = \frac{R_L}{\alpha}\left(\frac{r}{1+k^2} - 1\right) \tag{6.9}$$

$$\frac{1}{\sqrt{3}Z_C} = \alpha\frac{1+k^2}{k^2R_L} + Y_0 \cdot \sqrt{2\frac{1+k^2}{r}-1} \tag{6.10}$$

$$\theta = \cos^{-1}\left(\frac{\alpha}{k}\sqrt{r\frac{Z_0}{2R_L}}\right) \tag{6.11}$$

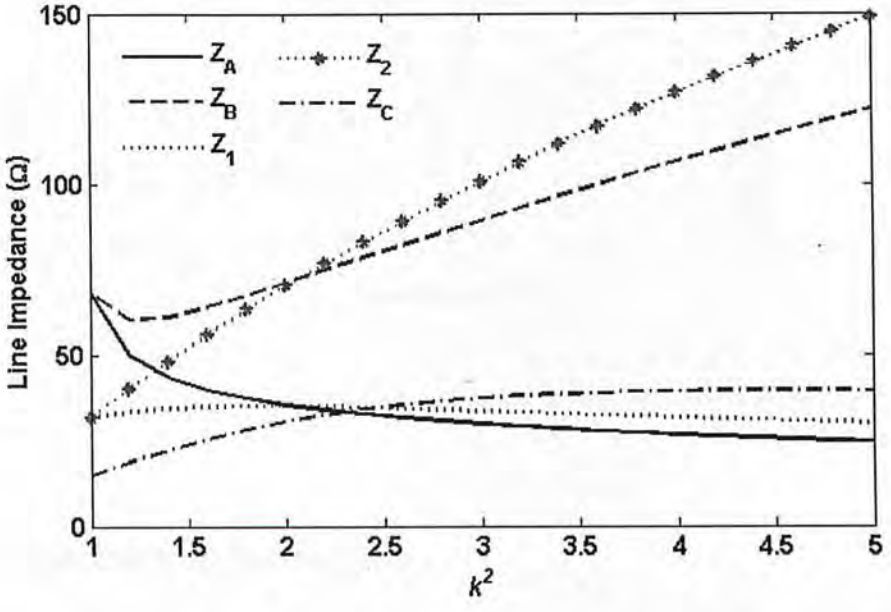
$$Z_A = \frac{\cot\theta}{\alpha}R_L \tag{6.12}$$

$$r = \frac{R}{R_L} < 1+k^2 \tag{6.13}$$

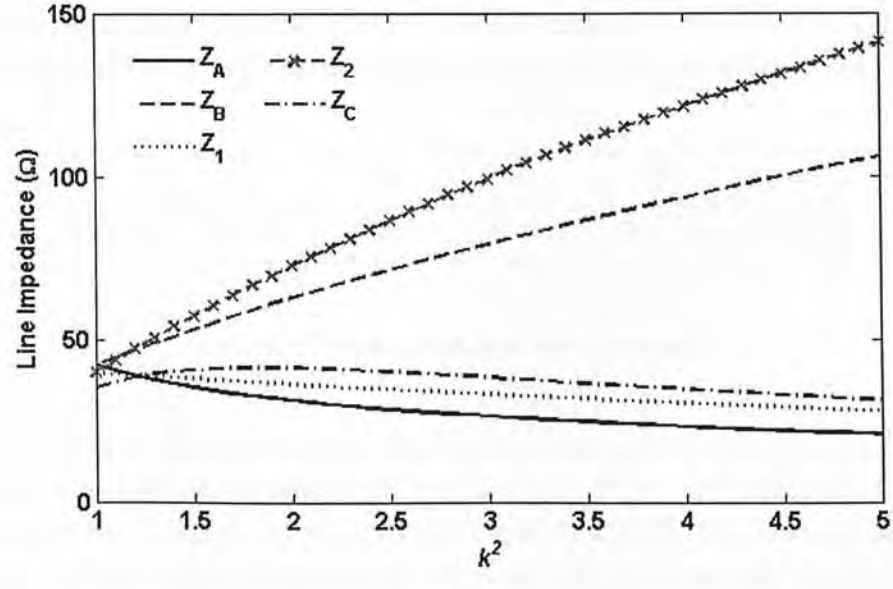
It can be seen that the circuit variables (Z_1, Z_2, Z_A, Z_B, Z_C, θ) are function of k^2, R and R_L only.

6.3 Simulation Study

Figure 6.5 shows the variation of computed line impedance versus k^2 with fixed R_L and R. The maximum dividing ratio is mainly limited by the available impedance range (20 – 130 Ω) to around 4. The simulated frequency responses of two illustrative circuits ($k^2 = 2$) with $R_L = 50$ Ω, $R = 82$ Ω and $R_L = 40$ Ω, $R = 180$ Ω were depicted in Figure 6.6. The results indicate that an enhanced spurious suppression can be achieved by the adoption of a larger value of Z_2 (or Z_B).



(a)



(b)

Figure 6.5 Computed line impedances versus power dividing ratio: (a) $R_L = 35$ Ω, $R = 100$ Ω; (b) $R_L = 40$ Ω, $R = 70$ Ω

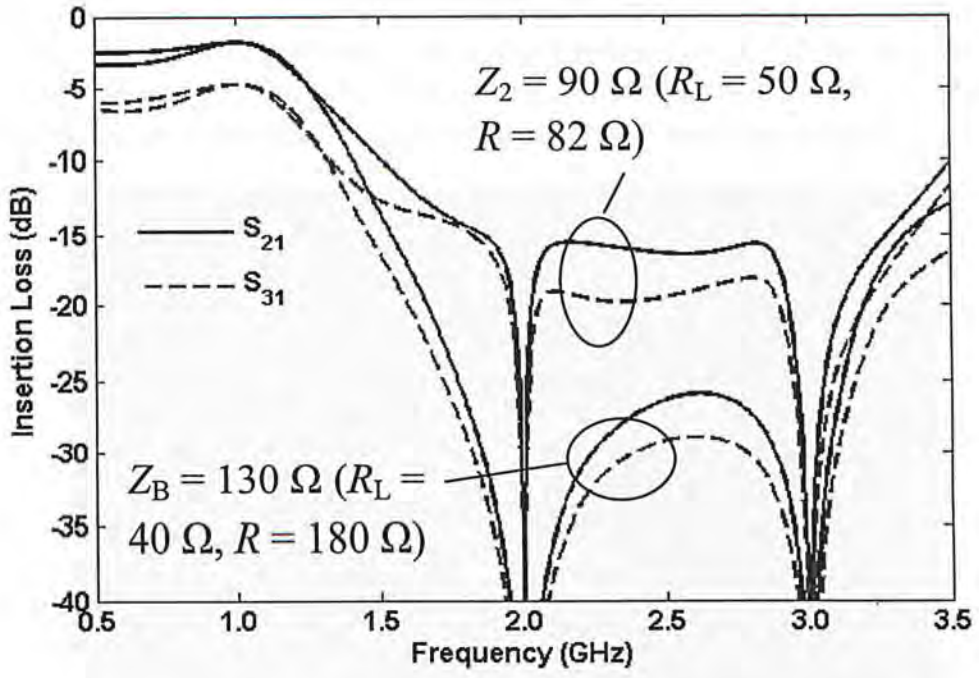


Figure 6.6 Simulated frequency responses (power dividing ratio of 2)

6.4 Experimental Verification

For verification, a 2:1 power divider designed to operate at 1 GHz was prototyped and characterized. Based on the impedance limit (< 90 Ω) of the processing facility, the two circuit parameters (R_L and R) were carefully chosen with an aim to enhance the spurious suppression. The resulting design parameters were shown in Table 6.1.

R_L	R	Z_A	Z_B	Z_1	Z_2	Z_C	θ
50 Ω	82 Ω	34 Ω	68 Ω	44.6 Ω	89.2 Ω	33.3 Ω	109°

Table 6.1 Circuit parameters of the prototype

Figure 6.7 shows the top view of the layout with a core area (excluding output impedance transformer) of approximately $\lambda_g/6 \times \lambda_g/4$. It was fabricated on Duroid substrate with a dielectric constant of 3.38 and thickness of 0.813 mm. Scattering parameter measurements were performed using a 4-port network analyzer (Agilent E5071A) over the frequency range from 0.5 to 3.5 GHz. Figure 6.8 shows the simulated (EM) and measured performance of the divider. These results indicate that a wide spurious suppression bandwidth (1.75 – 3.32 GHz) has been achieved with a minimum attenuation of – 14 dB. The attenuation levels, evaluated at 2.0 and 3.0 GHz, were both greater than 30 dB. Within the fundamental band, the divider was found to

exhibit a S_{21} of – 1.98 ± 0.1 dB (– 1.76 dB in ideal case); a S_{31} of – 5.10 ± 0.1 dB (– 4.77 dB in ideal case); minimum input/output return loss of –15 dB and minimum port isolation of – 25 dB over a fractional bandwidth of about 15 %. Excellent agreement between the simulated and measured results was also observed.

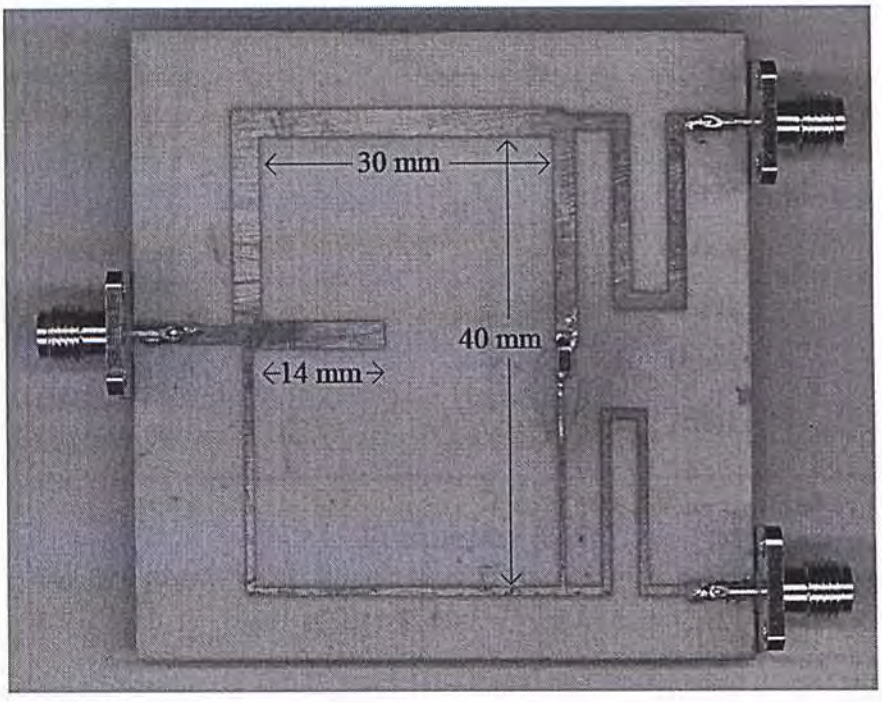
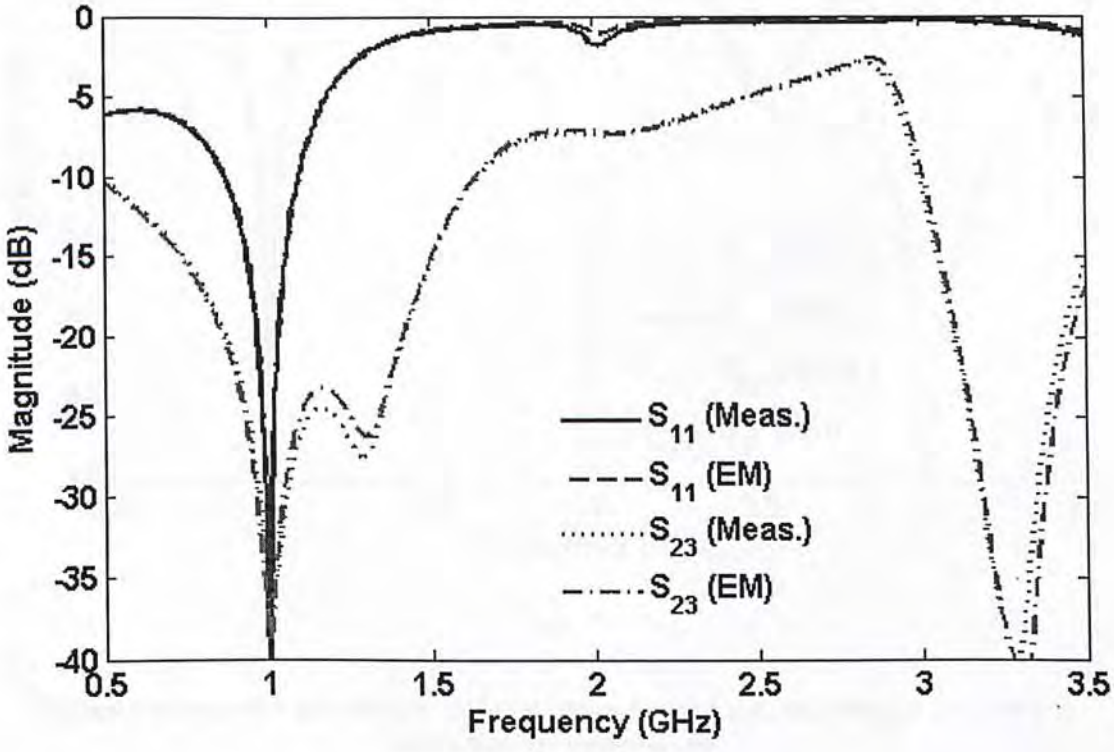
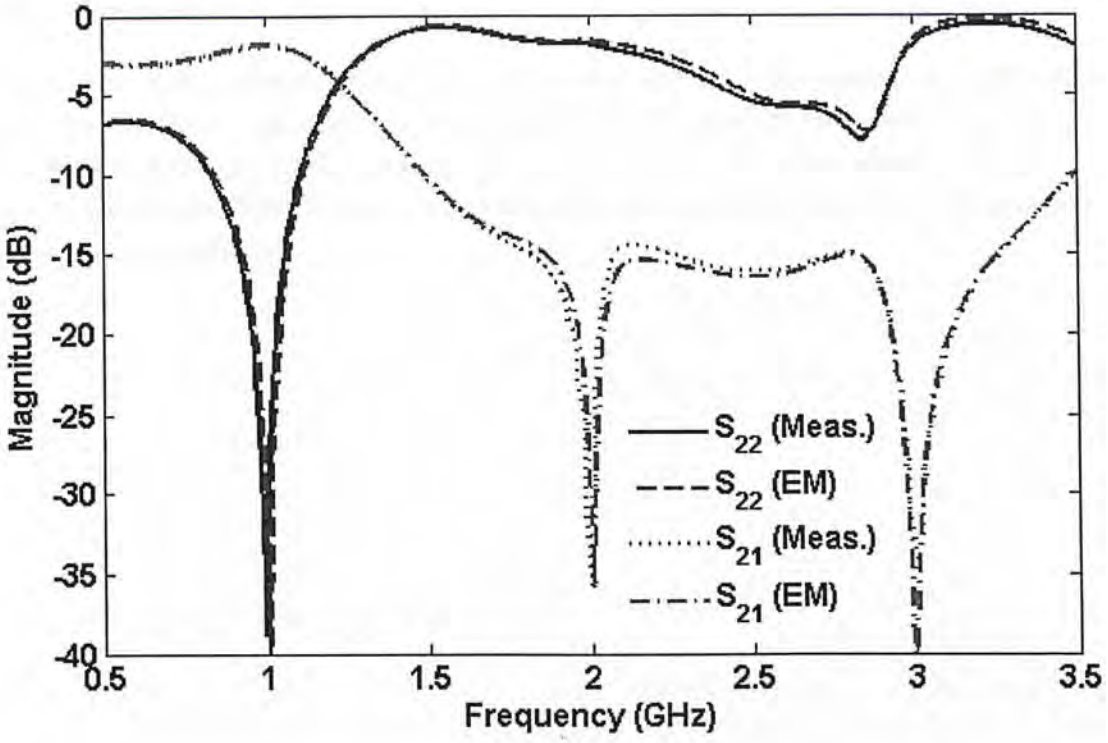


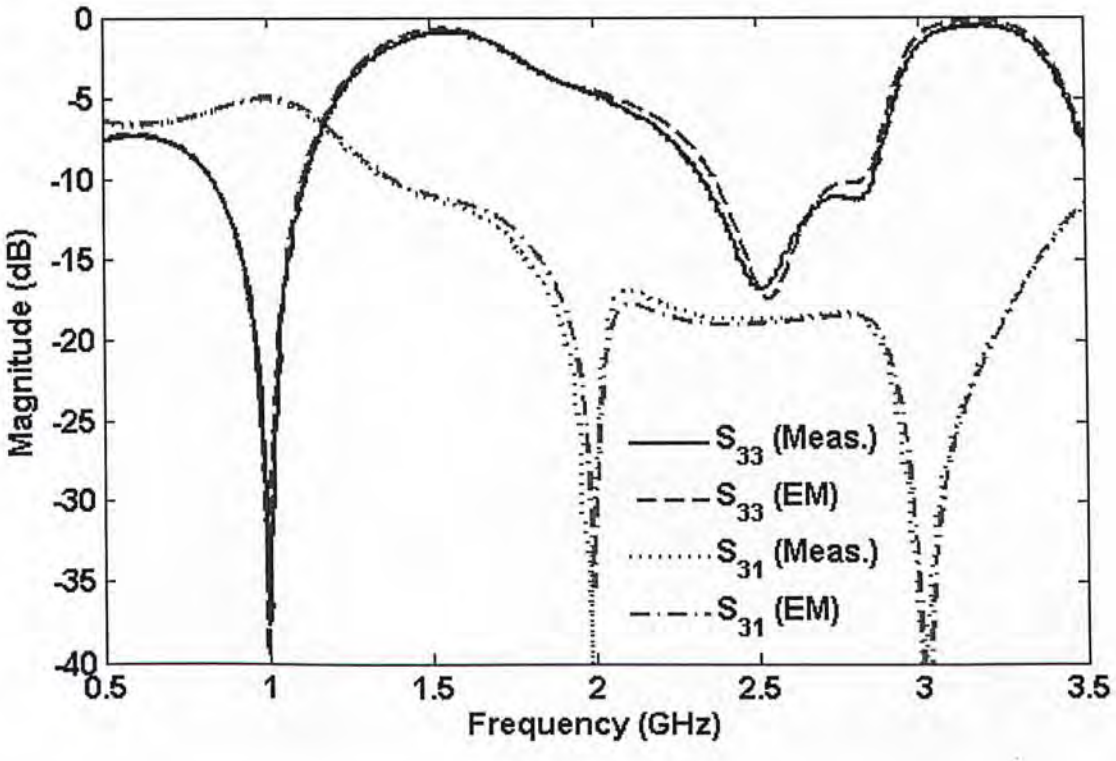
Figure 6.7 Photograph of the prototype



(a)



(b)



(c)

Figure 6.8 Measured S-parameters: (a) input return loss and port isolation, (b) & (c) output return loss and insertion loss

6.4 Summary

The design and implementation of a novel power divider with unequal dividing ratio and dual-harmonic rejection has been presented. This circuit is simple to construct and requires no complex structures such as DGS and multi-layer substrate. Excellent results have been demonstrated, which includes low insertion loss and wide spurious suppression bandwidth.

Chapter 7: New 3-way Power Divider Design with Multi-harmonic Rejection

This chapter introduces a novel 3-way microwave power divider design with harmonic suppression. Details of design concepts and mathematical analyses are discussed. A 1 GHz divider circuit is designed, fabricated and measured for verification.

7.1 Proposed Topology

Figure 7.1 shows the schematic diagram of the proposed power divider. It is based on the power recombination method (Chapter 3) which basically consists of a 1:1 power divider and two 2:1 power dividers. Each power divider is composed of four branch-line sections and an isolation resistor. An open stub is connected to the input port of the 2:1 power divider. Unlike the conventional designs, the output ports are shifted away from the isolation resistor by the insertion of the extended arms (Z_B, Z_1, $2Z_1$) for increased layout flexibility and reduced proximity effect. These extended arms are also responsible for the rejection of 2nd and 4th harmonic bands. The open stub is introduced for 3rd harmonic band suppression. For increased design freedom, transmission lines (Z_C) are inserted between divider stages for impedance transformation. As a result, the transformed load admittance (= $X + jY$) of the first divider is related to the input admittance (= $G + jB$) of the second stage via the transmission line equation:

$$X + jY = Y_C \frac{G + jB + jY_C \tan\alpha}{Y_C + j(G + jB)\tan\alpha} \tag{7.1}$$

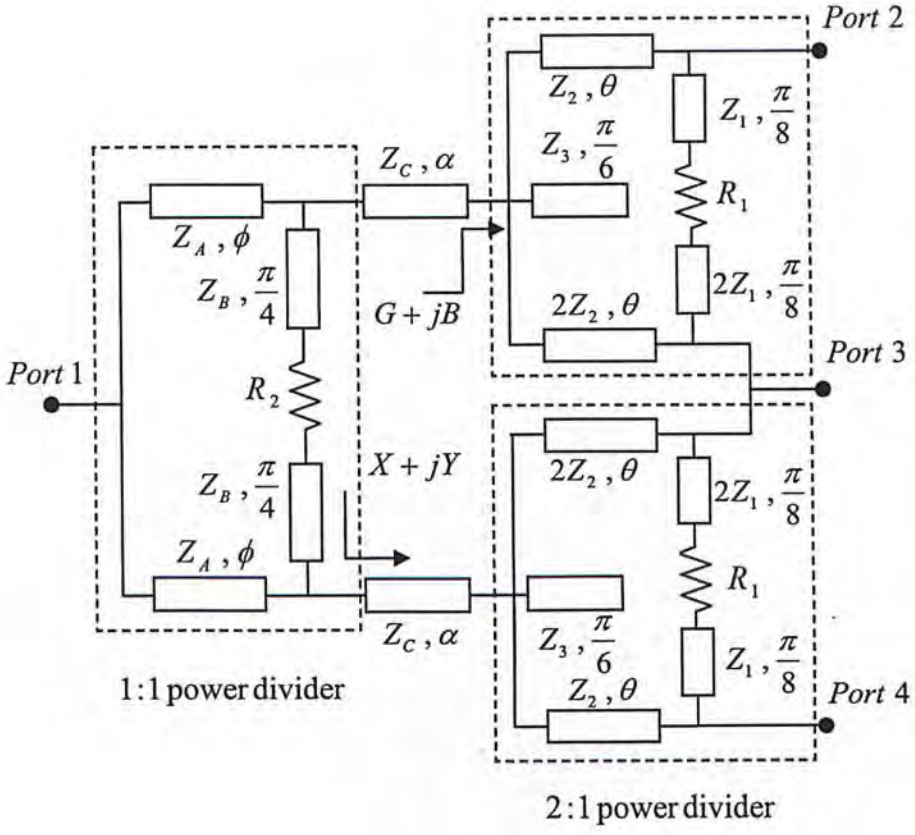


Figure 7.1 Circuit configuration of proposed 3-way power divider

7.2 Design and Analysis

For analysis purposes, Figures 7.2 and 7.3 show the odd- and even-mode circuits of the two divider stages (1:1 and 2:1). By the enforcement of the ideal return loss and port isolation conditions, the various admittances of the even- and odd-mode circuits (2:1 power divider) are derived and expressed by the following equations:

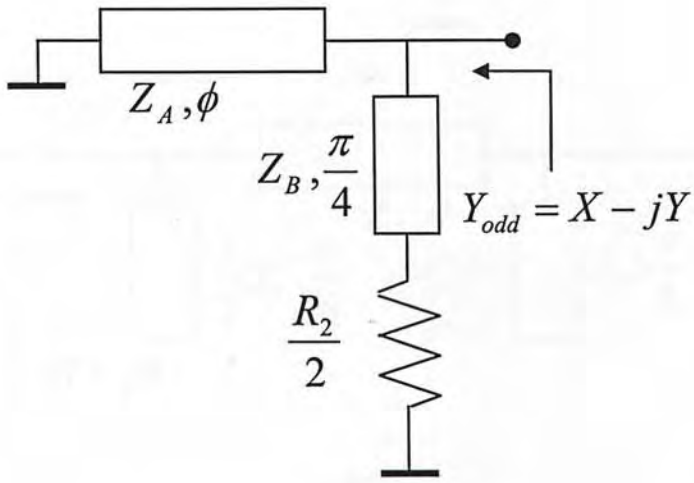
$$Y_0 = Y_1 \frac{3 + j(\sqrt{2}-1)Y_1 R_1}{Y_1 R_1 + j3(\sqrt{2}-1)} - jY_2 \cot\theta \tag{7.2}$$

$$G + jB = \frac{3}{2} Y_2 \frac{Y_0 + j(\sqrt{2}-1)Y_1 + jY_2 \tan\theta}{Y_2 - (\sqrt{2}-1)Y_1 \tan\theta + jY_0 \tan\theta} + j\frac{Y_3}{\sqrt{3}} \tag{7.3}$$

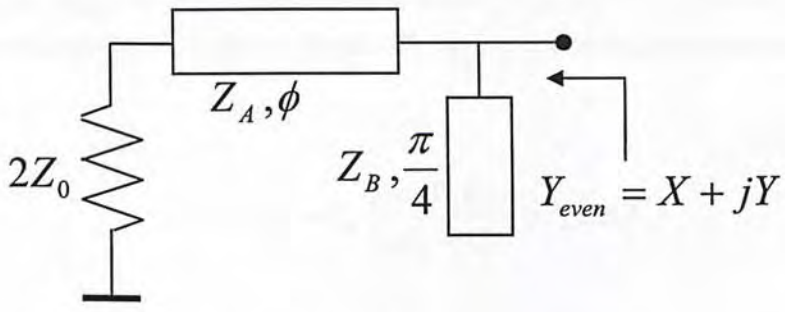
By equating the real and imaginary parts of (7.2), the circuit parameters of the second divider stage can now be obtained as a function of Z_1 and Z_2, as indicated by (7.4) – (7.5).

$$R_1 = 3(\sqrt{2}-1)Z_0\left\{\sqrt{2} \pm \sqrt{2-\left(\frac{Z_1}{Z_0}\right)^2}\right\} \tag{7.4}$$

$$\theta = \frac{\pi}{2} - \tan^{-1}\left[\frac{Z_2(R_1 Y_0 - 3)}{3Z_1(\sqrt{2}-1)}\right] \tag{7.5}$$

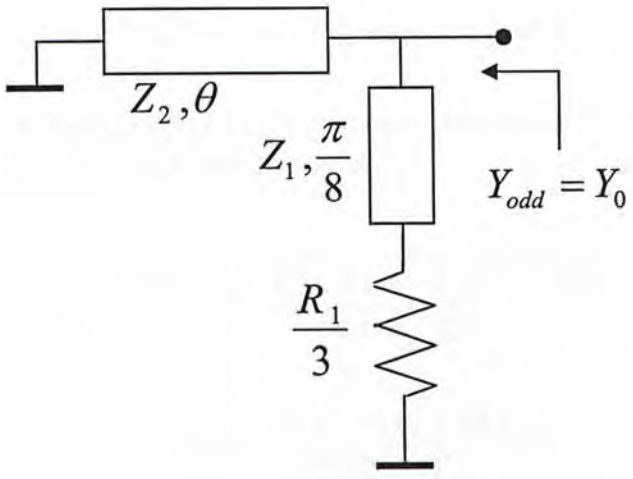


(a)

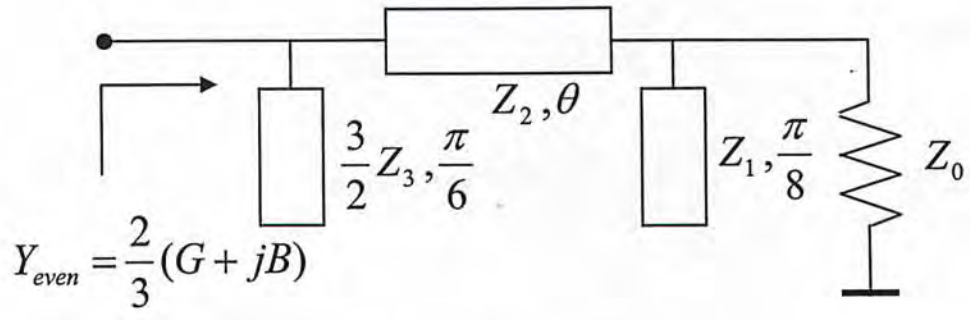


(b)

Figure 7.2 1:1 power divider: (a) odd- and (b) even-mode



(a)



(b)

Figure 7.3 2:1 power divider: (a) odd- and (b) even-mode

Meanwhile, the value of $X + jY$ are obtained from (7.3) and (7.1). By applying even-/odd-formulation to the first power divider (1:1), the following relationship can be established:

$$X - jY = Y_B \frac{2 + jY_B R_2}{Y_B R_2 + j2} - jY_A \cot\phi \tag{7.6}$$

$$X - jY = Y_A \frac{Y_0 + j2Y_A \tan\phi}{2Y_A + jY_0 \tan\phi} + jY_B \tag{7.7}$$

The real and imaginary parts of (7.6) & (7.7) are equated to give:

$$XR_2Y_B - 2(Y + Y_A \cot\phi) = 2Y_B \tag{7.8}$$

$$2X + R_2Y_B(Y + Y_A \cot\phi) = R_2Y_B^2 \tag{7.9}$$

$$2XY_A - (Y - Y_B)Y_0 \tan\phi = Y_AY_0 \tag{7.10}$$

$$2Y_A(Y-Y_B)+XY_0\tan\phi=2Y_A^2\tan\phi \tag{7.11}$$

Consequently, by solving (7.8)-(7.11), the circuit parameters of the 1:1 divider can simply be obtained in terms of X and Y as follows:

$$Y_B=\frac{1}{Z_B}=\frac{-YY_0\pm\sqrt{Y^2Y_0^2+X(X-Y_0)[4Y^2+(2X-Y_0)^2]}}{2(X-Y_0)} \tag{7.12}$$

$$R_2=\frac{4(Y_BX-Y_0Y_B+XY)}{XY_B(2X-Y_0)} \tag{7.13}$$

$$\frac{1}{Z_A}=\sqrt{\frac{XY_0}{2}+\frac{Y_0(Y-Y_B)^2}{2X-Y_0}} \tag{7.14}$$

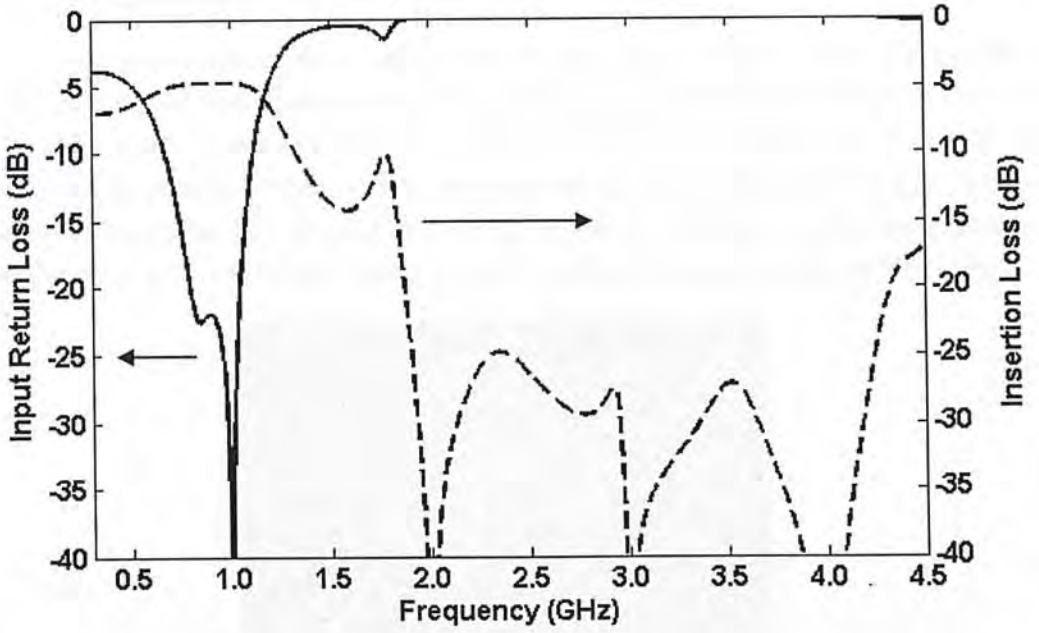
$$\phi=\frac{\pi}{2}-\tan^{-1}\left[\frac{Y_0Z_A(Y-Y_B)}{2X-Y_0}\right] \tag{7.15}$$

7.3 Simulation Study

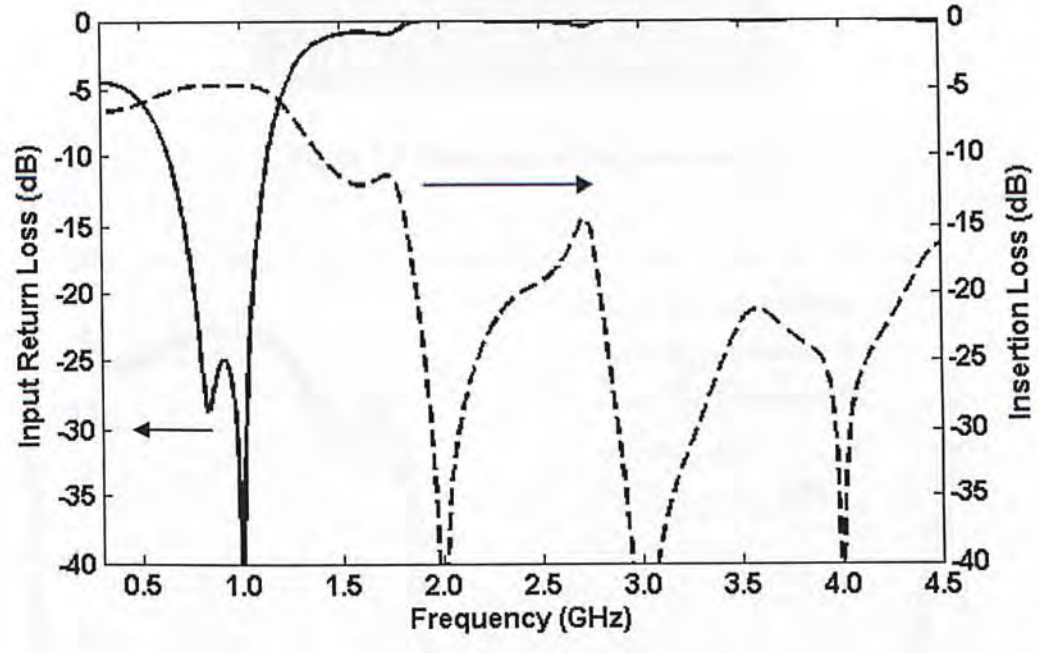
For the study of the optimal selection of the free variables, a series of simulations have been performed based upon ideal circuit elements. For illustration, Figure 7.4 shows the simulated frequency responses of power dividers designed with two sets of circuit parameters (Table 7.1). These results reveal that there exists some trade-off between line impedance value (30 ↔ 90 Ω) and spurious suppression performance.

		Design A	Design B
Selected variables	Z_1	30 Ω	40 Ω
	Z_2	46 Ω	42 Ω
	Z_3	30 Ω	50 Ω
	Z_C	40 Ω	50 Ω
	α	20°	20°
Computed parameters	Z_A	45.3 Ω	55.4 Ω
	Z_B	31.8 Ω	37.5 Ω
	ϕ	112.3°	111.3°
	θ	66.7°	80.1°
	R_1	167.4 Ω	160.3 Ω
	R_2	70.3 Ω	106.5 Ω

Table 7.1 Circuit parameters of design examples



(a)



(b)

Figure 7.4 Simulated responses of the proposed divider: (a) Design A; (b) Design B

7.4 Experimental Verification

For experimental verification, a power divider designed to operate at 1 GHz (Design A) was prototyped and characterized. The circuit was fabricated on Duriod substrate with a dielectric constant of 3.38 and thickness of 0.813 mm. Figure 7.5 shows the top view of the fabricated circuit with a core area of approximately $\lambda_g/4$ by $\lambda_g/4$. Surface mounted resistors of 160 Ω (R_1) and 68 Ω (R_2) were selected. Scattering parameter measurements were performed using a 4-port network analyzer (Agilent E5071A).

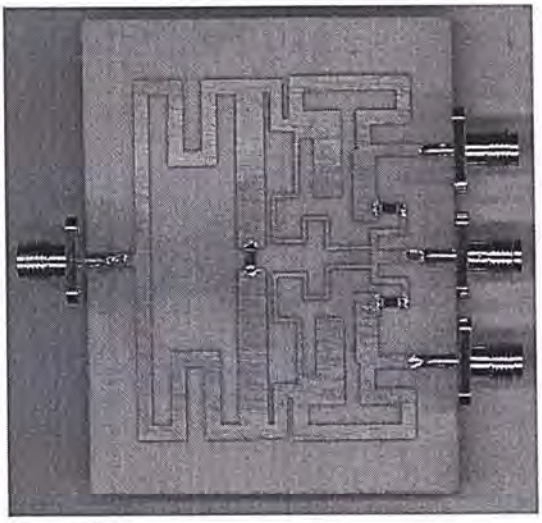


Figure 7.5 Photograph of the prototype

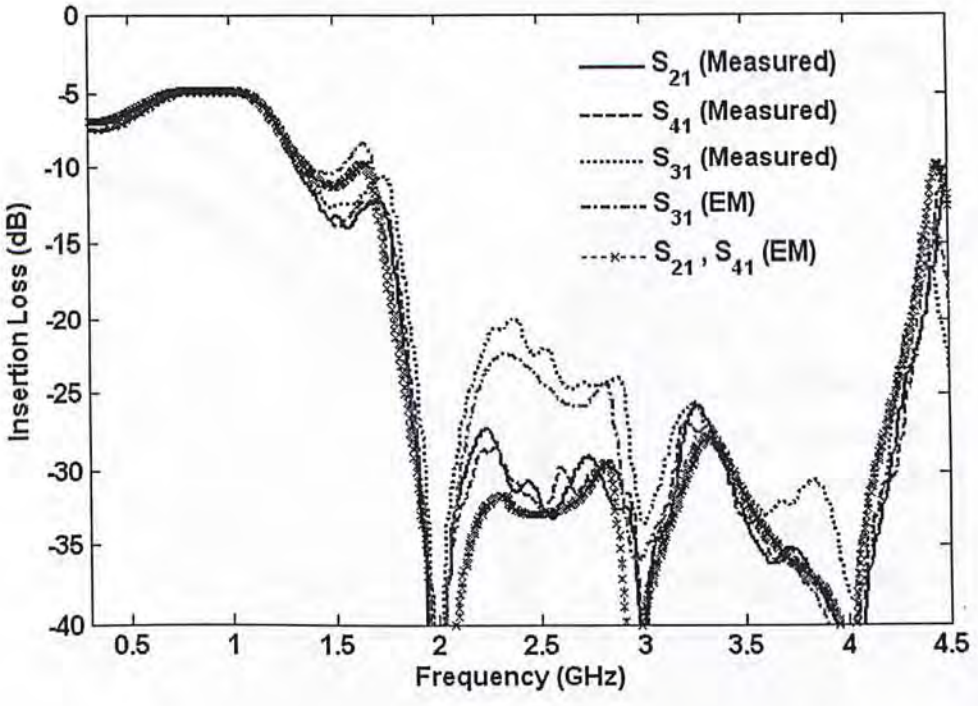


Figure 7.6 Simulated and measured insertion loss

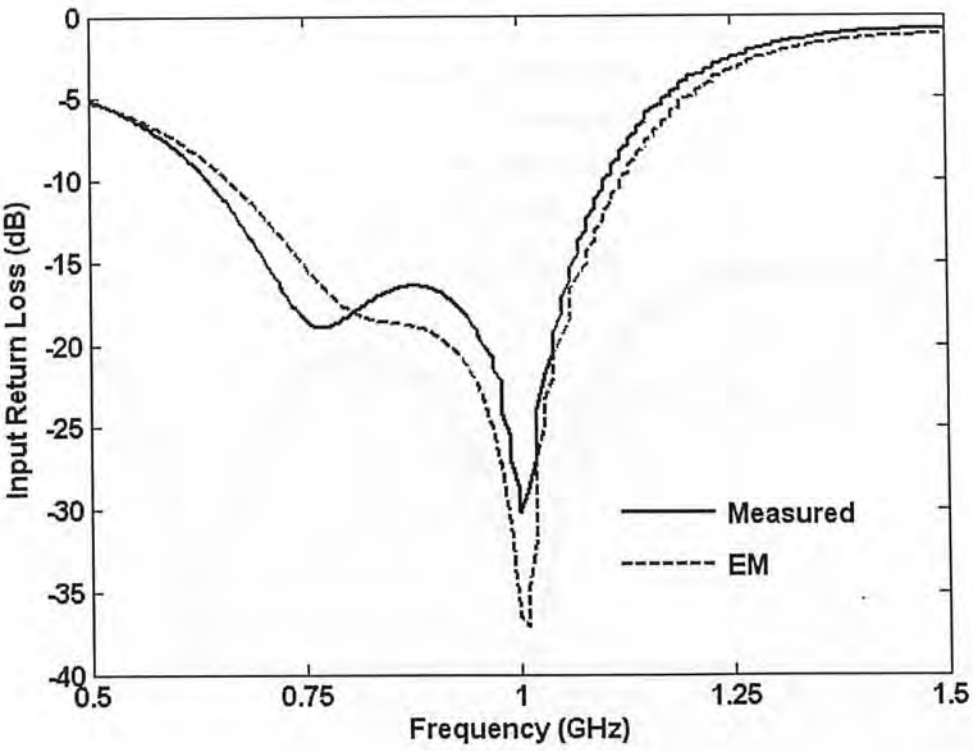


Figure 7.7 Simulated and measured input return loss

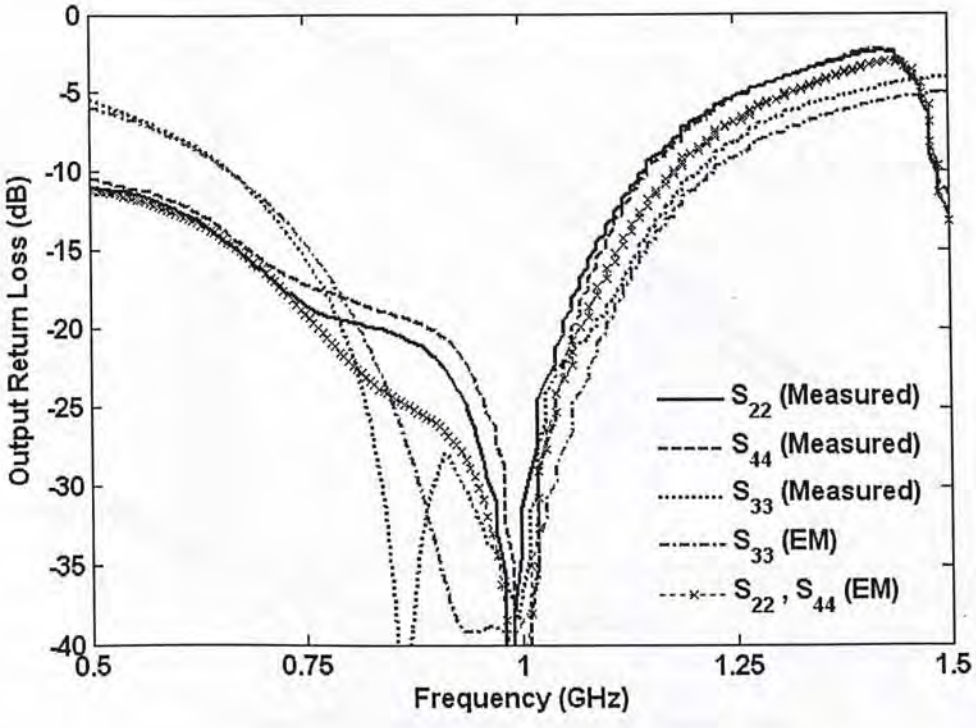


Figure 7.8 Simulated and measured output return loss

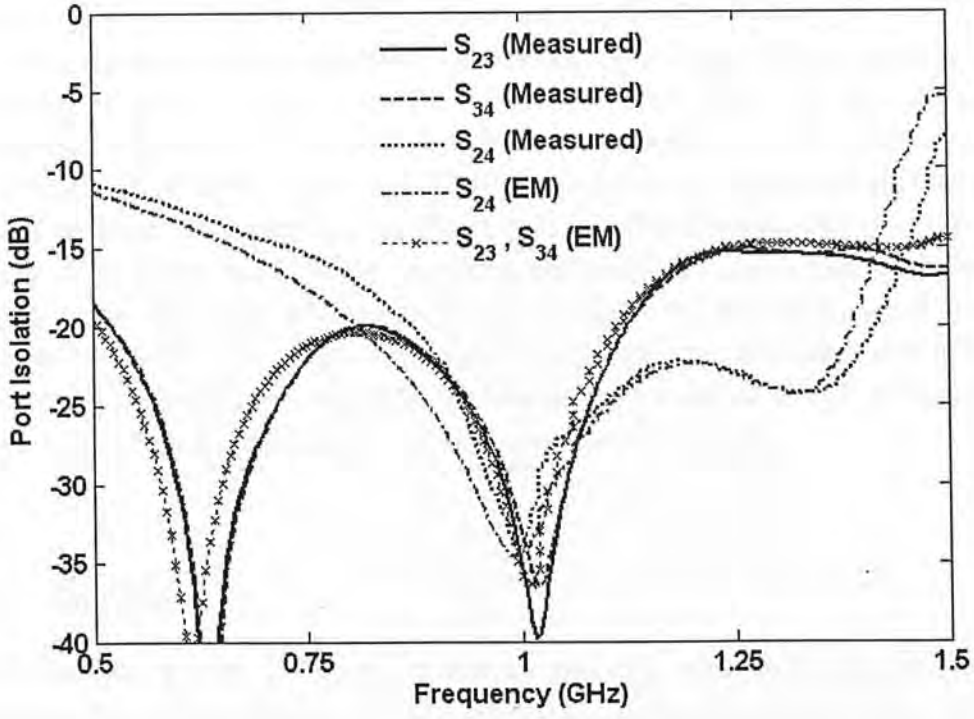


Figure 7.9 Simulated and measured port isolation

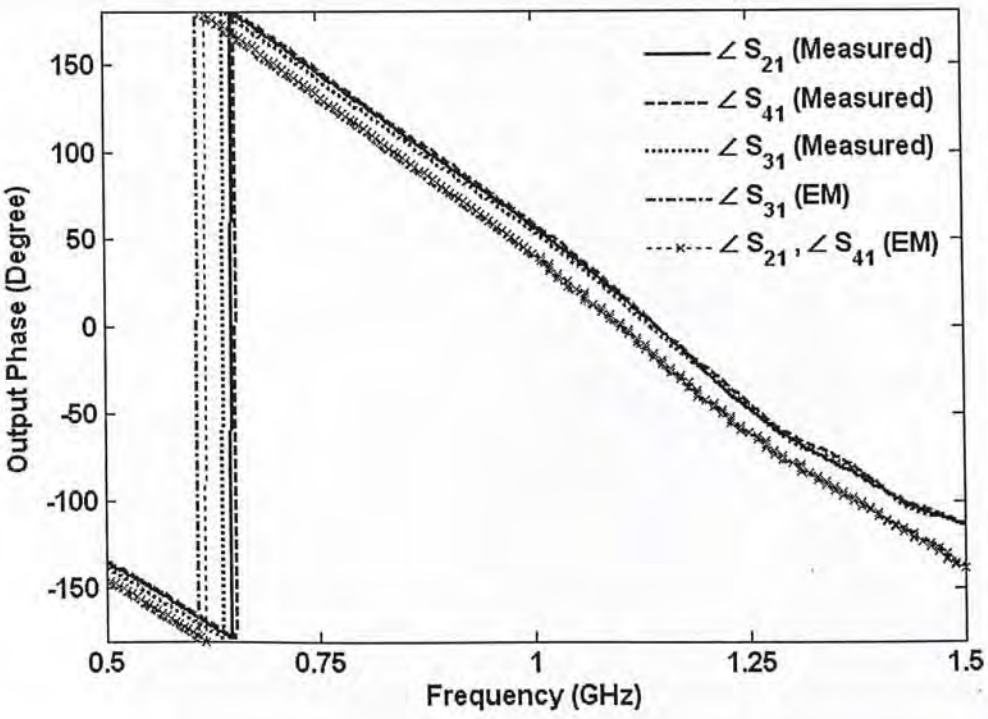


Figure 7.10 Simulated and measured output phase

Figures 7.6 – 7.10 give the simulated (EM) and measured performance of the divider. These results indicate that a wide spurious suppression bandwidth (1.8 ↔ 4.3 GHz) has been achieved with a minimum attenuation of –20 dB. The attenuation levels, evaluated at 2.0, 3.0 and 4.0 GHz, were all better than –30 dB. Within the fundamental band (0.8 ↔ 1.1 GHz), the divider was found to exhibit an insertion loss of –5.00 ± 0.15 dB (ideal value = –4.77 dB), minimum input/output return loss of –15 dB and minimum port isolation of –20 dB over a fractional bandwidth of about 30 %. Excellent agreement between the simulated and measured results was also observed. Output phase difference (Figure 7.10) was found to be negligibly small over the fundamental band. The slight discrepancies between the simulated and measured results were believed to be caused by the fabrication tolerances as well as the parasitic effects of junction discontinuities and surface-mounted resistors.

7.4 Summary

In this chapter, a novel 3-way power divider topology with multi-harmonic rejection capability has been presented. It offers several advantages including simple structure, flexible layout design, and requires minimum number of isolation resistors. The proposed circuit does not require backside etching, bond-wire or multi-layer substrate. Excellent performances have been demonstrated including low insertion loss (less than 0.3 dB), high port isolation and wide spurious suppression bandwidth.

Chapter 8: Conclusion

Due to the rapid development of wireless communication technology in the past decade, mobile devices such as mobile phones, notebooks and tablet PCs become indispensable in modern society. In order to satisfy the increasing demand for lower system cost, the realization of multi-functional and compact RF devices has become an attractive solution for industry and research topic for academics.

Power dividers, as a basic component, are widely used in microwave and millimetre-wave systems including antenna arrays, power amplifiers, mixers, etc. Due to the presence of spurious and harmonic responses, these dividers are normally employed in conjunction with separate low-pass or harmonic reject filters. Recently, different configurations have been proposed to combine harmonic filter and power divider into a single device. Unfortunately, these solutions are either complex in structure (DGS, multi-layer) or require reactive lumped component. Furthermore, none of these circuits can operate with unequal power split or multiple outputs.

In this research, several new power divider designs with enhanced spurious rejection have been introduced and rigorously analysed. In addition, these dividers are simple in structure, compatible with conventional PCB fabrication technology, compact size and multi-functional. The major innovations of this work include:

1. The development of a two-way power divider with equal power division, low spurious response and source/ load impedance transformation.
2. The development of a compact power divider with wide stop-band bandwidth.
3. The first power divider with unequal power dividing ratio and dual-harmonic rejection capabilities.
4. The first 3-way power divider with three transmission zeros over the upper stop-band. It is a compact and planar design with excellent port isolation and minimal number of resistors.

Possible areas for future investigation include power divider with variable dividing ratio or reconfigurable capabilities; further reduction in size; and multi-band operation. Explicit closed-form design formulas are developed for the realization of the proposed configurations and to reduce the effort in circuit tuning.

References

[1] K. H. Yi, and B. Kang, "Modified Wilkinson power divider for nth harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 5, pp. 178–180, May 2003.

[2] J. S. Kim, M. J. Park, and K. B. Kong, "Modified design of Wilkinson power divider for harmonic suppression," *Electronics Letters*, vol. 45, no. 23, pp. 1174-1175, 5th Nov. 2009.

[3] K. Srisathit, P. Jadpum, and W. Surakampontorn, "Miniature Wilkinson divider and hybrid coupler with harmonic suppression using T-shaped transmission line," *2007 Asia-Pacific Microwave Conference Digest*, pp. 1–4, Dec. 2007.

[4] D. J. Woo, and T. K. Lee, "Suppression of harmonics in Wilkinson power divider using dual-band rejection by asymmetric DGS," *IEEE Trans. Microwave Theory & Tech.*, vol. 53, no. 6, pp. 2139-2144, June 2005.

[5] C. M. Lin, H. H. Su, J. C. Chiu, and Y. H. Wang, "Wilkinson power divider using microstrip EBG cells for the suppression of harmonics," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 10, pp. 700–702, Oct. 2007.

[6] J. Zhang, L. Li, J. Gu, and X. Sun, "Compact and harmonic suppression Wilkinson power divider with short circuit anti-coupled line," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 9, pp. 661–663, Sept. 2007.

[7] J. Yang, C. Gu, and W. Wu, "Design of novel compact coupled microstrip power divider with harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 9, pp. 572–574, Sept. 2008.

[8] J. Wang, J. Ni, Y. X. Guo, and D. Fang, "Miniaturized microstrip Wilkinson power divider with harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 7, pp. 440–442, July 2009.

[9] E. J. Wilkinson, "An N-Way Hybrid Power Divider," *IEEE Trans. Microwave Theory Tech.*, vol. 8, no. 1, pp. 116-118, Jan 1960

[10] L. I. Parad and R. L. Moynihan, "Split-tee power divider," *IEEE Trans. Microwave. Theory Tech.*, vol. MTT-13, pp. 91-95, Jan. 1965

[11] S. David, "A wideband coaxial-line power divider," *IEEE Trans. Microwave Theory Tech. (Correspondence)*, vol. MTT-15, pp. 270-271, Apr. 1967.

[12] P. C. Goodman, "A Wideband Stripline Matched Power Divider," in *1986 International Microwave Symposium Digest Tech. Papers* (IEEE Cat. No. 68C38), pp. 16-20, May 1968.

[13] S. B. Cohn, "A class of broadband three-port TEM-mode hybrids," *IEEE Trans. Microwave Theory Tech.*, vol. 19, no. 2, pp. 110-116, Feb. 1968.

[14] R. B. Ekinge, "A new method of synthesizing matched broad-band TEM-mode three-ports," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 81-88, Jan. 1971.

[15] N. Nagai, E. Maekawa, and K. Ono, "New N-way hybrid power dividers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 1008-1012, Dec. 1977.

[16] A. Saleh, "Planar electrically symmetric n-way power dividers/combiners," *IEEE Trans. Microwave Theory Tech.*, vol. MTT- 28, pp. 555-563, June 1980.

[17] Z. Galani and S. J. Temple, "A broadband planar *N*-way combiner/divider," in *1977 International Microwave Symposium Digest* (IEEE Cat. No. 77CH1219-5MTT), pp. 503-504, June 1977.

[18] A. M. Abbosh, "A compact UWB three-way power divider," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 8, pp. 598–600, Aug. 2007.

[19] J. Reed and G. J. Wheeler, "A method of analysis of symmetrical four-port networks," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-4, pp. 246-252, Oct. 1956.

[20] H. Y. Yee, F. C. Chang and N. F. Audeh, "N-way TEM-mode broad-band power dividers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 682-688, Oct. 1970.

[21] S. V. Bearse, Ed., "Compact radical power combiner terms up a dozen power GaAs FETs," *Microwaves*, vol. 16, no.10, pp. 9, Oct. 1977.

[22] J. M. Schellenberg and M. Cohn, "A wideband radial power combiner for FET amplifiers," in *1978 IEEE International Solid-State Circuit Conf. Digest* (IEEE Cat. No. 78CH1298-9SSC), pp. 164-165, 273, Feb. 1978.

[23] M. Cohn, B. D. Geller, and J. M. Schellenberg, "A 10-watt broadband FET combiner/ amplifier," in *1979 IEEE International Microwave Symposium Digest* (IEEE Cat. No. 79CH1439-9MTT), pp. 292-297, Apr. 1979.

[24] M. E. Goldfarb, "A recombinant, in-phase power divider," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 8, pp. 1438-1440, Aug. 1991.

[25] J. C. Chiu, J. M. Lin, and Y. H. Wang, "A novel planar three-way power divider," *IEEE Microwave and Wireless Component Letters*, vol. 16, no. 8, pp. 449-451, Aug. 2006.

[26] Y. A. Lai, C. M. Lin, J. C. Chiu, C. H. Lin and Y. H. Wang, "A compact Ka-band planar three-way power divider," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 12, pp. 840–842, Dec. 2007.

[27] K. H. Yi, and B. Kang, "Modified Wilkinson power divider for nth harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 5, pp. 178–180, May 2003.

[28] K. Srisathit, P. Jadpum, and W. Surakampontorn, "Miniature Wilkinson divider and hybrid coupler with harmonic suppression using T-shaped transmission line," in *Asia–Pacific Microwave Conference Digest*, Dec. 2007, pp. 1–4.

[29] D. J. Woo, and T. K. Lee, "Suppression of harmonics in Wilkinson power divider using dual-band rejection by asymmetric DGS," *IEEE Trans. Microwave Theory & Tech.*, vol. 53, no. 6, pp. 2139-2144, June 2005.

[30] J. S. Lim, Y. C. Jeong, D. Ahn, and S. Nam, "A technique reducing the size of microwave amplifiers using spiral-shaped defected ground structure," *J. Korea Electromagn. Eng.*, vol. 14, no. 9, pp. 904-911, Sep. 2003.

[31] I. S. Lim and B. S. Lee, "Design of defected ground structures for harmonics control for active microstrip antenna," in *Proceeding of IEEE Antennas and Propagation Society International Symposium*, vol. 2, pp. 852-855, June 2002.

[32] J. Zhang, L. Li, J. Gu, and X. Sun, "Compact and harmonic suppression Wilkinson power divider with short circuit anti-coupled line," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 9, pp. 661–663, Sept. 2007.

[33] C. M. Lin, H. H. Su, J. C. Chiu, and Y. H. Wang, "Wilkinson power divider using microstrip EBG cells for the suppression of harmonics" *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 10, pp. 700–702, Oct. 2007.

[34] B.-L. Ooi, "Compact EBG in-phase hybrid-ring equal power divider," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 7, pp. 2329–2334, Jul. 2005.

[35] J. Wang, J. Ni, Y. X. Guo, and D. Fang, "Miniaturized microstrip Wilkinson power divider with harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 7, pp. 440–442, July 2009.

[36] J. S. Kim, M. J. Park and K. B. Kong, "Modified design of Wilkinson power divider for harmonic suppression," *IEEE Electronics Letters*, vol. 45, no. 23, pp. 1174–1175, Nov. 2009.

[37] F. Zhang and C. F. Li, "Power divider with microstrip electromagnetic bandgap element for miniaturisation and harmonic rejection," *Electronics Letters*, vol. 44, no. 6, pp. 422–423, Mar. 2008.

[38] J. Yang, C. Gu, and W. Wu, "Design of novel compact coupled microstrip power divider with harmonic suppression," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 9, pp. 572–574, Sept. 2008.

[39] W. C. Ip, and K. K. M. Cheng, "A novel power divider design with enhanced harmonic suppression and simple layout," *IEEE MTT-S, International Microwave Symposium Digest*, pp. 125–128, May 2010.

[40] W. C. Ip, and K. K. M. Cheng, "A novel microstrip power divider design with harmonic suppression and impedance transformation," *IEEE Asia-Pacific Microwave Conference Proceedings*, pp. 1256–1259, Dec 2010.

[41] K. K. M. Cheng, and W. C. Ip, "A Novel Power Divider Design with Enhanced Spurious Suppression and Simple Structure," *IEEE Trans. Microwave Theory Tech.*, vol. 58, no. 12, part 2, pp. 3903-3908, Dec 2010.

[42] W. C. Ip, and K. K. M. Cheng, "A Novel Unequal Power Divider Design With Dual-Harmonic Rejection and Simple Structure," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 4, pp. 182-184, Apr 2011.

[43] W. C. Ip, and K. K. M. Cheng, "A Novel 3-Way Power Divider Design with Multi-Harmonic Suppression," Accepted by *IEEE MTT-S, International Microwave Symposium 2011*.

Author's Publications and Awards

Publication:

1. W. C. Ip, and K. K. M. Cheng, "A novel power divider design with enhanced harmonic suppression and simple layout," *IEEE MTT-S, International Microwave Symposium Digest*, pp. 125–128, May 2010, Anaheim.

2. K. K. M. Cheng, and W. C. Ip, "A Novel Power Divider Design With Enhanced Spurious Suppression and Simple Structure," *IEEE Trans. Microwave Theory Tech.*, vol. 58, no. 12, part 2, pp. 3903-3908, Dec 2010.

3. W. C. Ip, and K. K. M. Cheng, "A novel microstrip power divider design with harmonic suppression and impedance transformation," *IEEE Asia-Pacific Microwave Conference Proceedings*, pp. 1256–1259, Dec 2010, Yokohama.

4. W. C. Ip, and K. K. M. Cheng, "A Novel Unequal Power Divider Design With Dual-Harmonic Rejection and Simple Structure," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 4, pp. 182-184, Apr 2011.

5. W. C. Ip, and K. K. M. Cheng, "A Novel 3-Way Power Divider Design with Multi-Harmonic Suppression," Accepted by *IEEE MTT-S, International Microwave Symposium 2011*, Baltimore.

6. W. C. Ip, S. Yeung, and K. K. M. Cheng, "A Novel Dual-band Crossover Design with Enhanced Frequency Band Ratio and Operating Bandwidth," submitted to *Asia-Pacific Microwave Conference*, 2011, Melbourne.

Awards:

1. Champion of the IET (HK) YMEC 2010 (Postgraduate Section)

2. IEEE Hong Kong Section AP/MTT Joint Chapter The Eleventh Postgraduate Conference Best Student Paper Award (1st Prize)

Appendix 1: ABCD Parameters of Some Useful Two-port Circuits

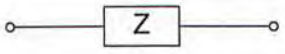
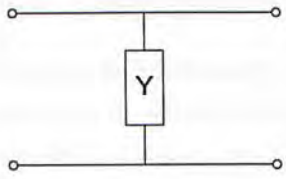
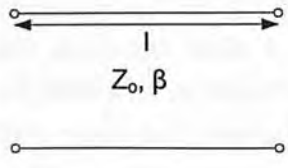
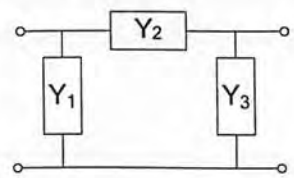
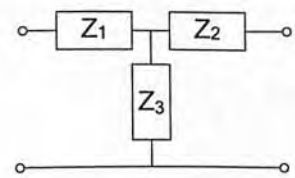
Circuit	ABCD Parameters	
	$A = 1$	$C = 0$
	$B = Z$	$D = 1$
	$A = 1$	$B = 0$
	$C = Y$	$D = 1$
	$A = \cos\beta l$	$B = jZ_o \sin\beta l$
	$C = jY_o \sin\beta l$	$D = \cos\beta l$
	$A = 1 + \frac{Y_1}{Y_3}$	$B = \frac{1}{Y_3}$
	$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}$	$D = 1 + \frac{Y_1}{Y_3}$
	$A = 1 + \frac{Z_1}{Z_3}$	$B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3}$
	$C = \frac{1}{Z_3}$	$D = 1 + \frac{Z_1}{Z_3}$

Table A1.1 ABCD Parameters of Some Useful Two-port Circuits

Appendix 2: More Designs of Proposed Configuration in Chapter 5

In this Appendix, more designs using the configuration in Chapter 5 (Example 1) will be discussed. These designs include the miniaturized version using meandered lines; design with improved attenuation in stop-band, and prototype with operating frequency of 2 GHz. Both simulated and measured results will be shown.

A2.1 Miniaturized version of Example 1

The circuit parameters are summarized in Table A2.1, and the photograph of the prototype is shown in Figure A2.1. The circuit size is reduced by about 30 % in compared to the one described in Chapter 5, with only a slight degradation in performance. Figures A2.2 – A2.6 show the simulated (EM) and measured performance of the prototype. An octave stop-band bandwidth (1.89 – 4.18 GHz) has been achieved with a minimum attenuation of 24 dB. The suppression levels, evaluated at the second-, third- and fourth- harmonic frequencies (1.97, 2.96, 4.03 GHz), were well above 35 dB. Inside the fundamental band, the divider was found to exhibit an insertion loss of 3.22 $\pm$ 0.1 dB, minimum return loss (both input and output) and port isolation of 20 dB, over a fractional bandwidth of about 25%. The output phase difference (Figure A2.6) was found to be negligibly small.

δ	ξ	ψ	ϕ	Z_A	Z_B	Z_C	Z_D	R	θ
45°	22.5°	30°	32°	90 Ω	57 Ω	86 Ω	34 Ω	66.7	47°

Table A2.1 Circuit parameters of the prototype

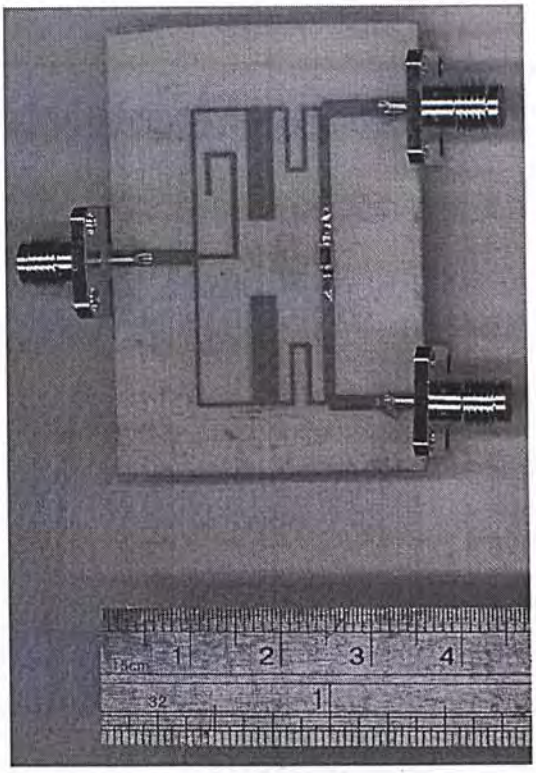


Figure A2.1 Photograph of the prototype

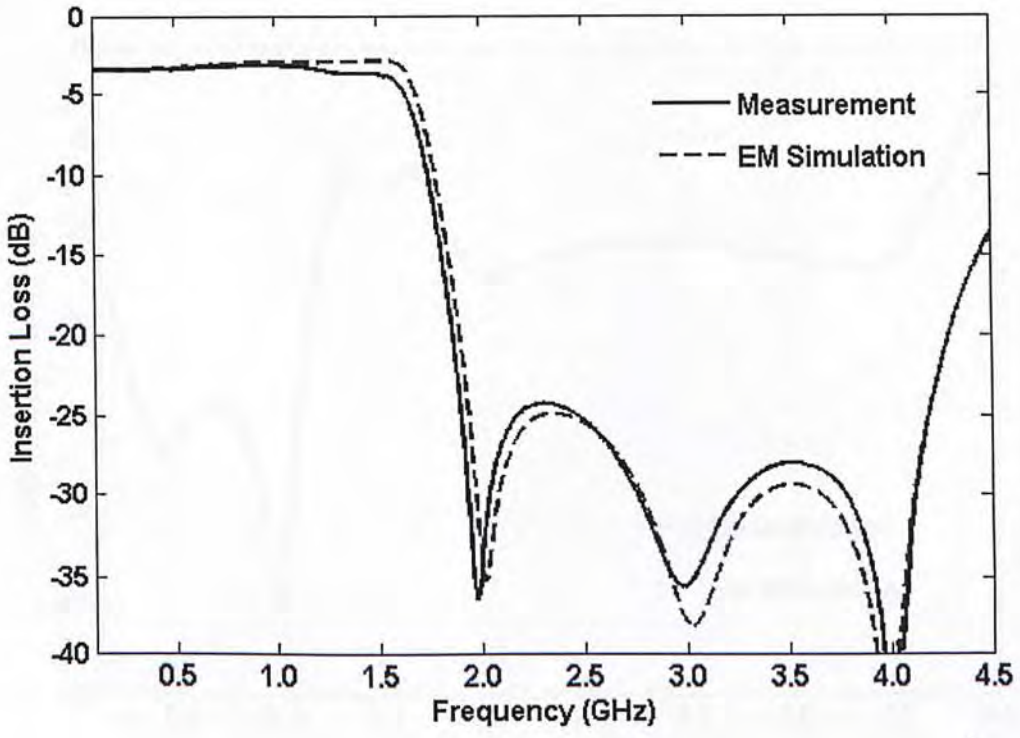


Figure A2.2 Simulated and measured insertion loss

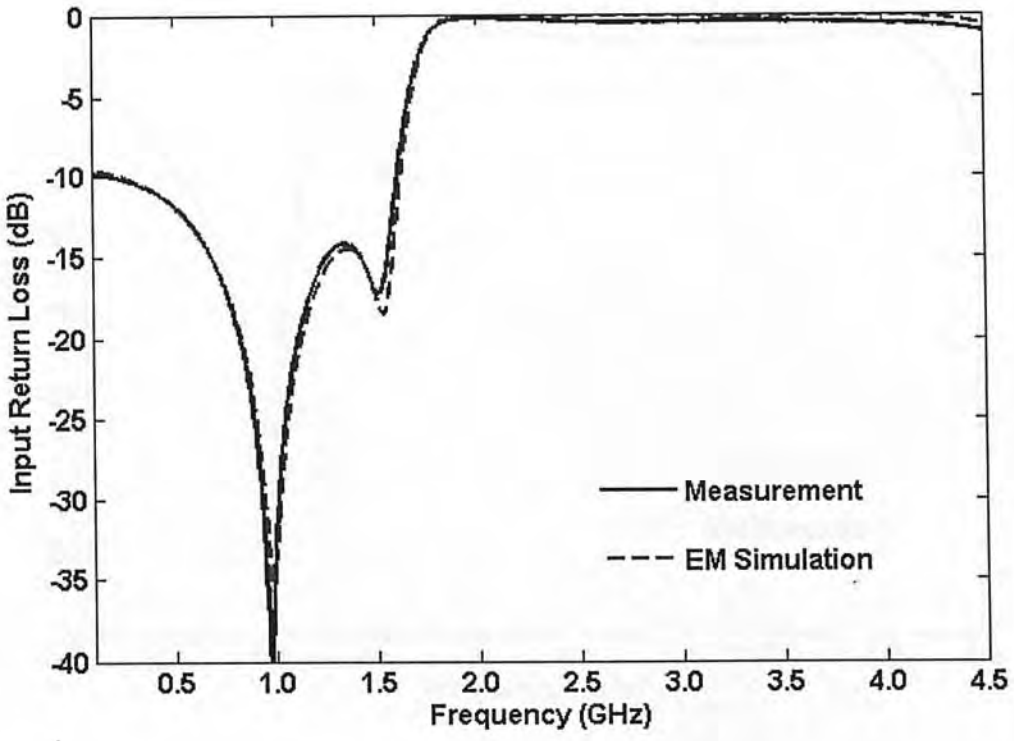


Figure A2.3 Simulated and measured input return loss

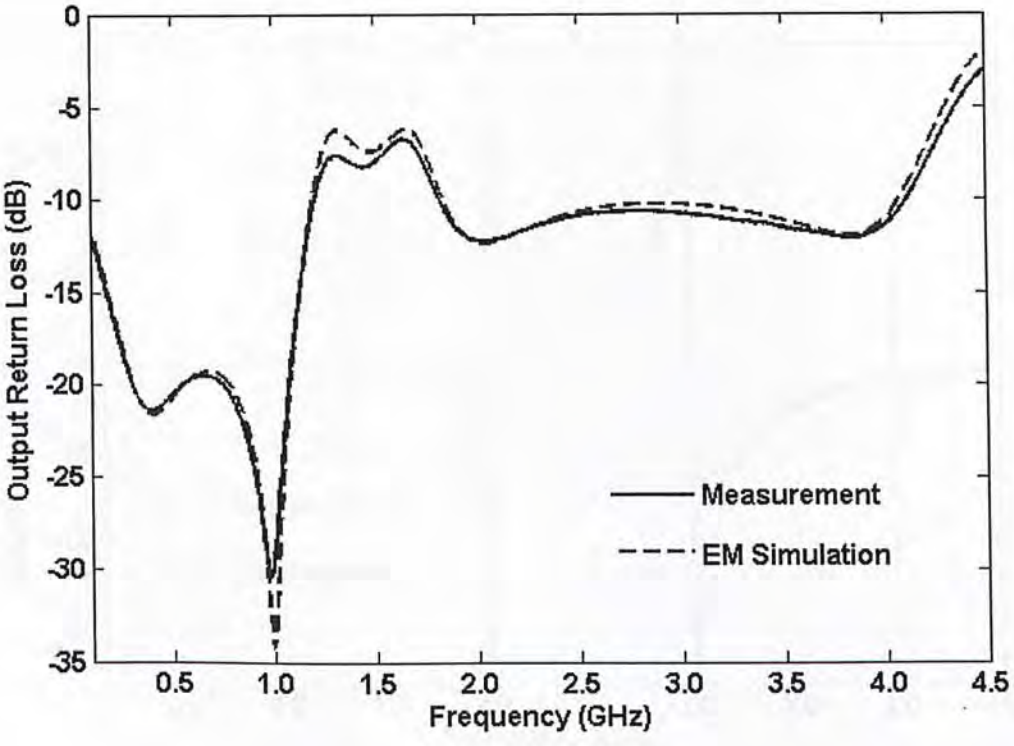


Figure A2.4 Simulated and measured output return loss

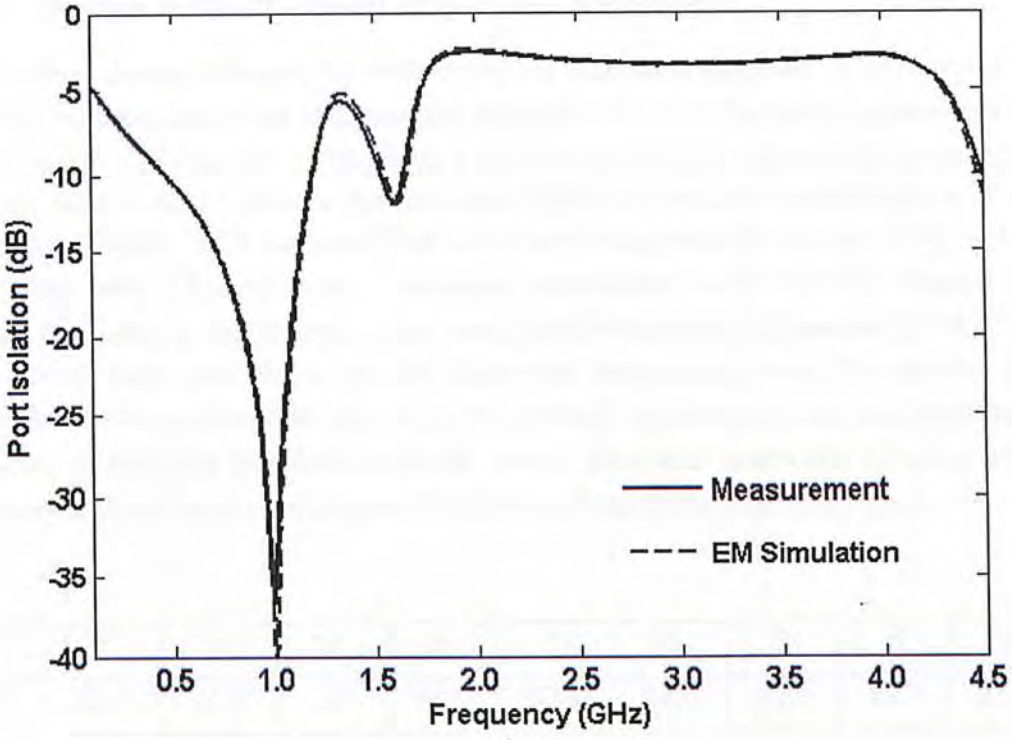


Figure A2.5 Simulated and measured port isolation

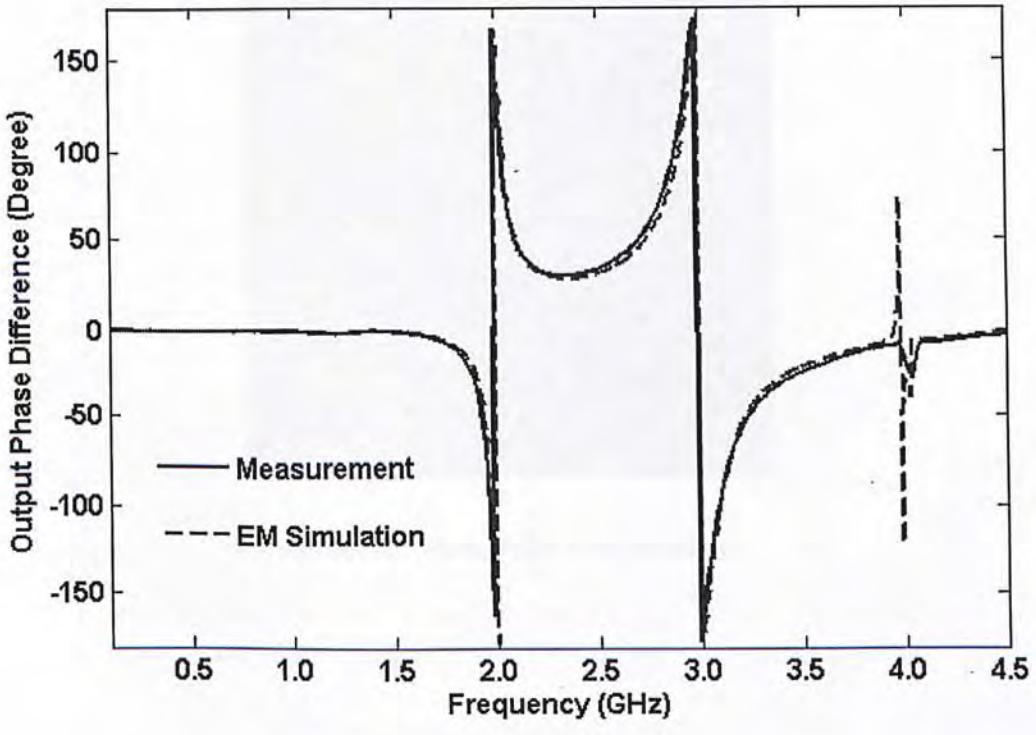


Figure A2.6 Simulated and measured output phase difference

A2.2 Design with improved stop-band response

A modified design (Chapter 5) with enhanced stop-band response is prototyped by shifting the locations of the transmission zeros ($\psi = 32.1$ °). The circuit parameters are summarized in Table A2.2. The layout of the prototype is shown in Figure A2.7. Figures A2.8 – A2.12 present the simulated (EM) and measured performance of the prototype. Figure A2.8 indicates that an octave stop-band bandwidth (1.92 – 4.23 GHz) has been achieved with a minimum attenuation of 28 dB. The suppression levels, evaluated at the second-, third- and fourth- harmonic frequencies (1.98, 2.79, 3.98 GHz), were well above 40 dB. Inside the fundamental band, the divider was found to exhibit an insertion loss of 3.2 $\pm$ 0.04 dB, minimum return loss (both input and output) and port isolation of 20 dB, over a fractional bandwidth of about 20%. The output phase difference (Figure A2.12) was found to be negligibly small.

δ	ξ	ψ	ϕ	Z_A	Z_B	Z_C	Z_D	R	θ
45°	22.5°	32.1°	32°	90 Ω	57.7	84.4	32.8	69.7	45.9°

Table A2.2 Circuit parameters of the prototype

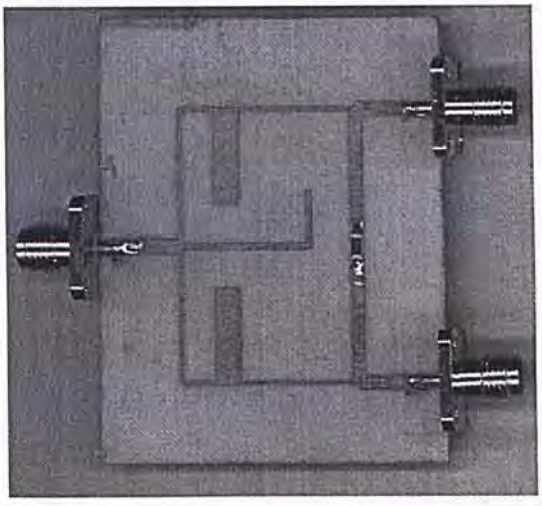


Figure A2.7 Photograph of the prototype

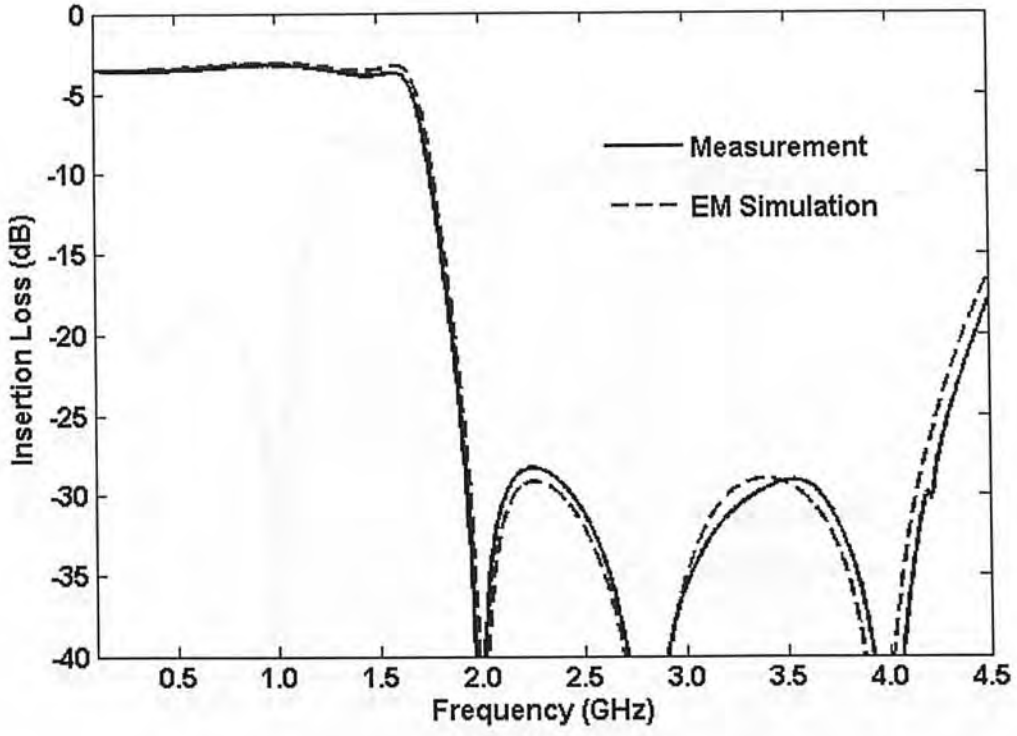


Figure A2.8 Simulated and measured insertion loss

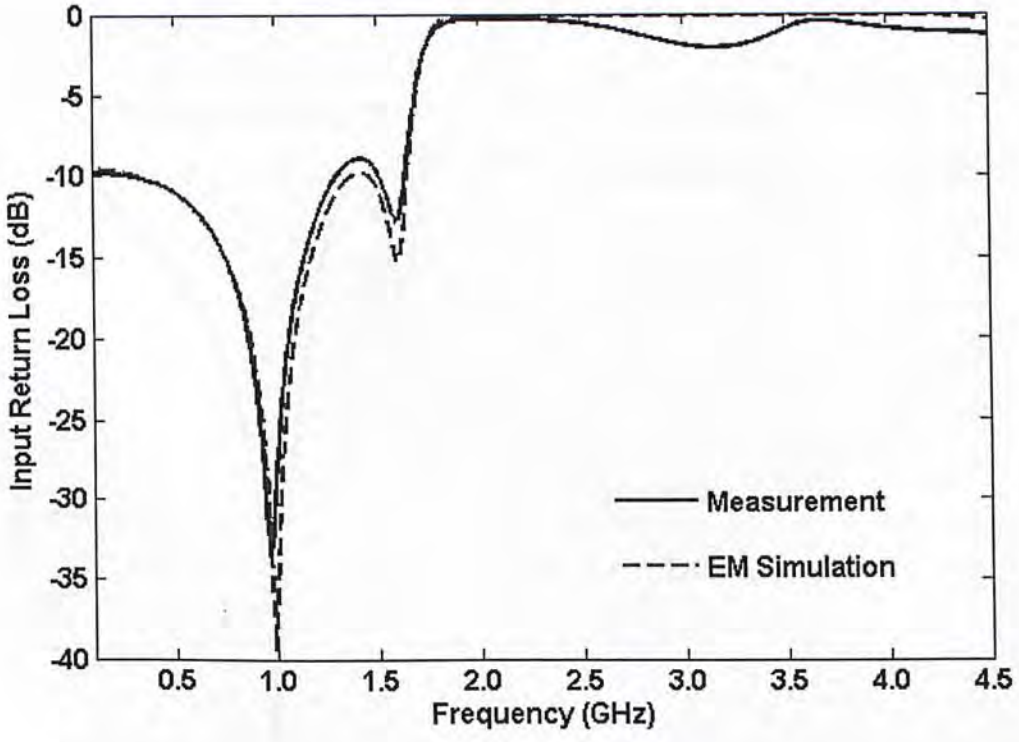


Figure A2.9 Simulated and measured input return loss

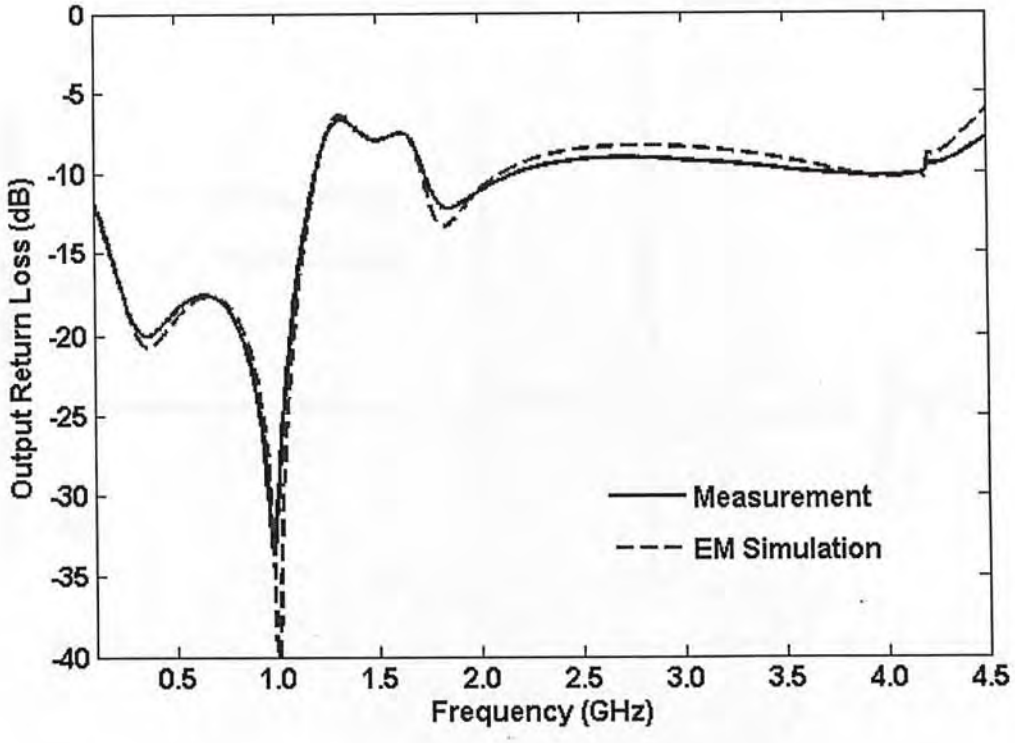


Figure A2.10 Simulated and measured output return loss

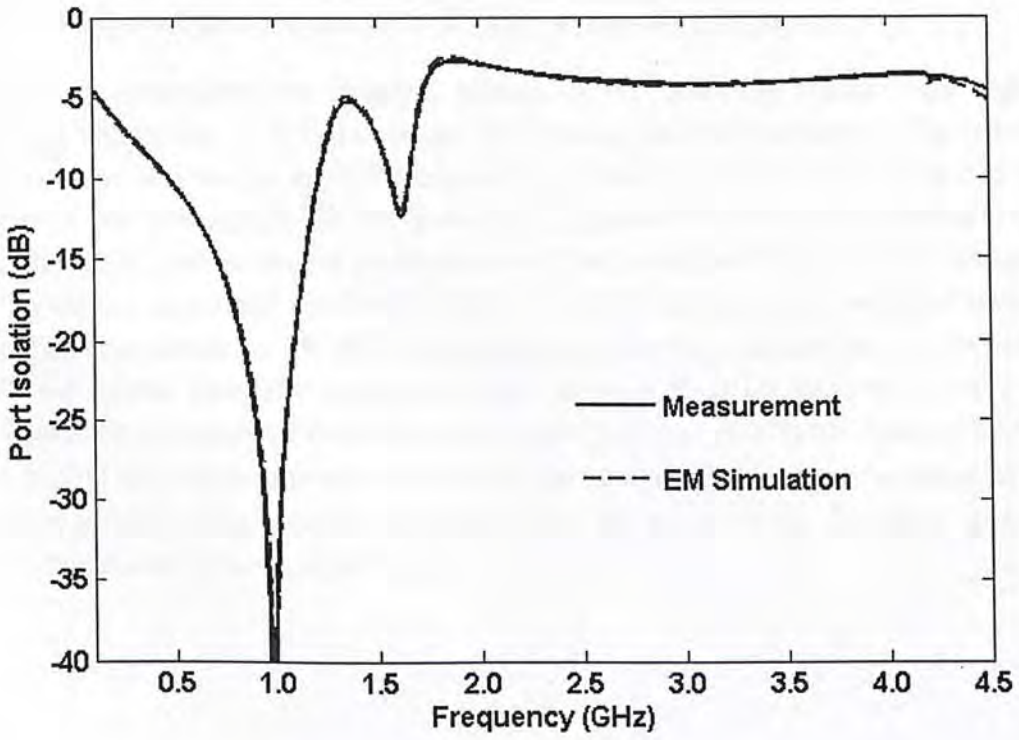


Figure A2.11 Simulated and measured port isolation

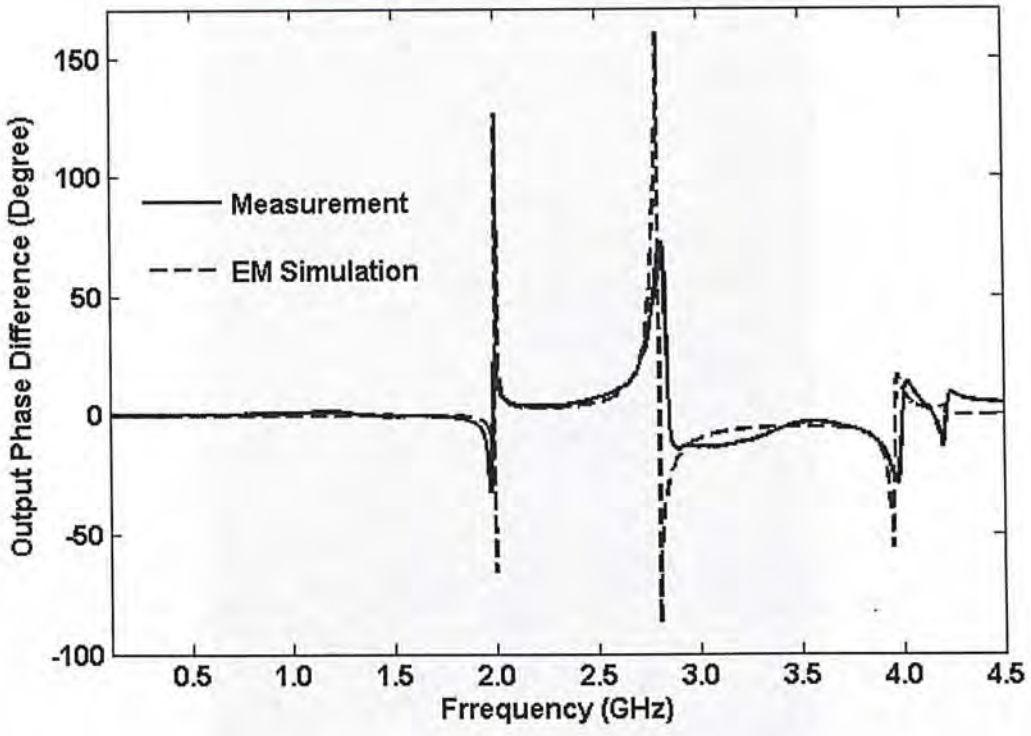


Figure A2.12 Simulated and measured output phase difference

A2.3 Design of prototype with 2 GHz operating frequency

In order to investigate the parasitic effects of the proposed circuit with higher operating frequency, a 2 GHz design was fabricated and measured. The circuit parameters of this design are the same as those listed in Table A2.1. Figure A2.13 illustrated the photograph of the prototype. Figures A2.14 – A2.18 present the simulated (EM) and measured performance of the prototype. Figure A2.14 indicates that an octave stop-band bandwidth (3.85 – 8.45 GHz) has been achieved with a minimum attenuation of 24 dB. The suppression levels, evaluated at the second-, third- and fourth- harmonic frequencies (4.00, 6.04, 8.05 GHz), were well above 40 dB. Inside the fundamental band, the divider was found to exhibit an insertion loss of 3.19 $\pm$ 0.04 dB, minimum return loss (both input and output) and port isolation of 20 dB, over a fractional bandwidth of about 25%. The output phase difference (Figure A2.12) was found to be negligibly small.

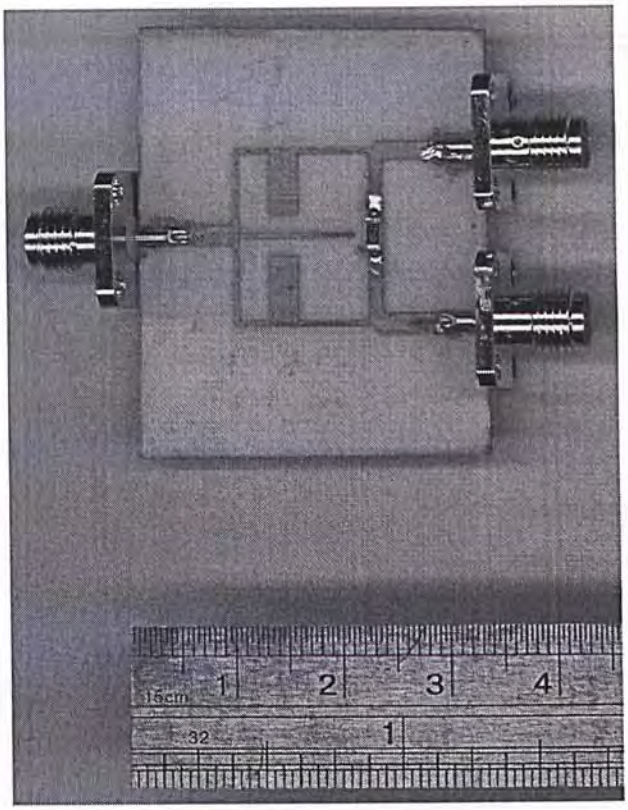


Figure A2.13 Photograph of the prototype with centre frequency at 2 GHz

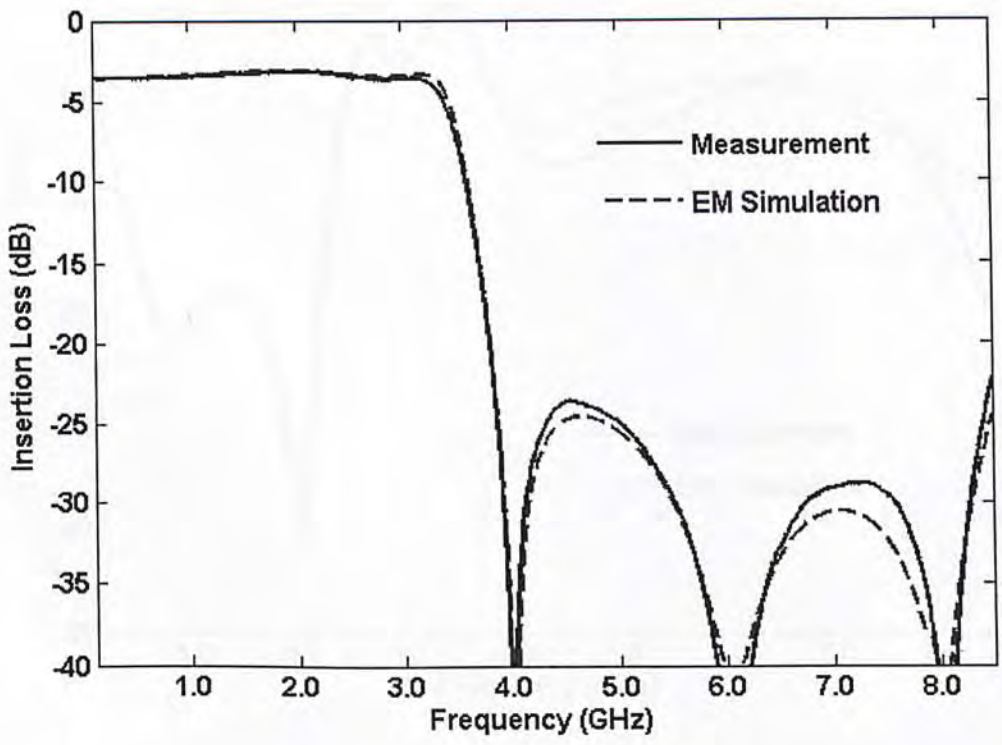


Figure A2.14 Simulated and measured insertion loss

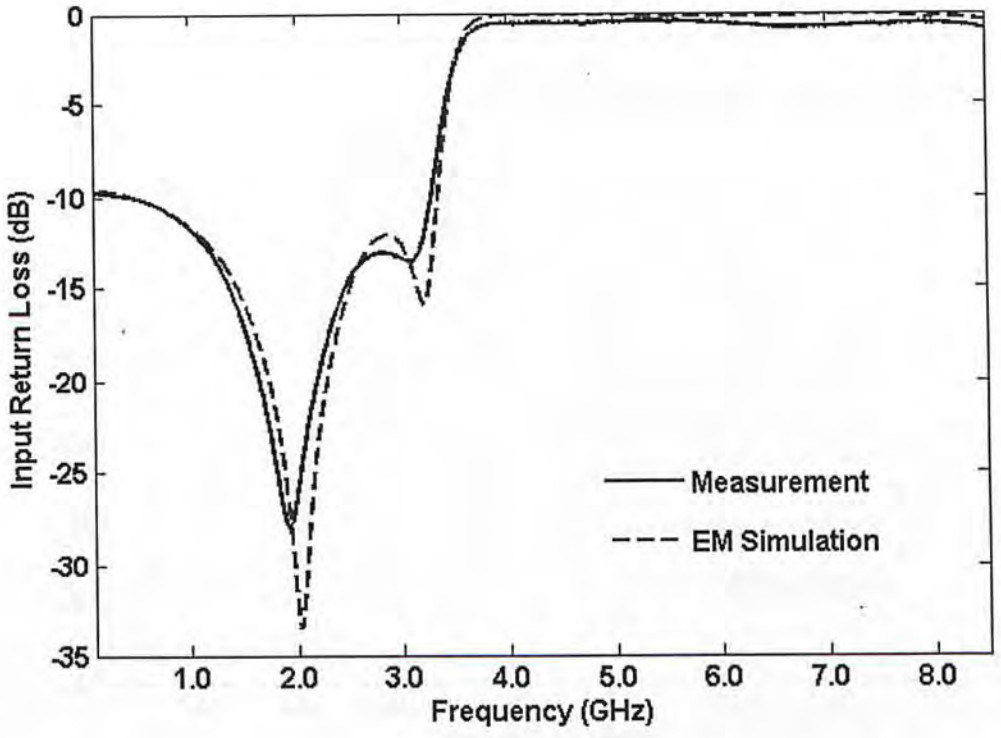


Figure A2.15 Simulated and measured input return loss

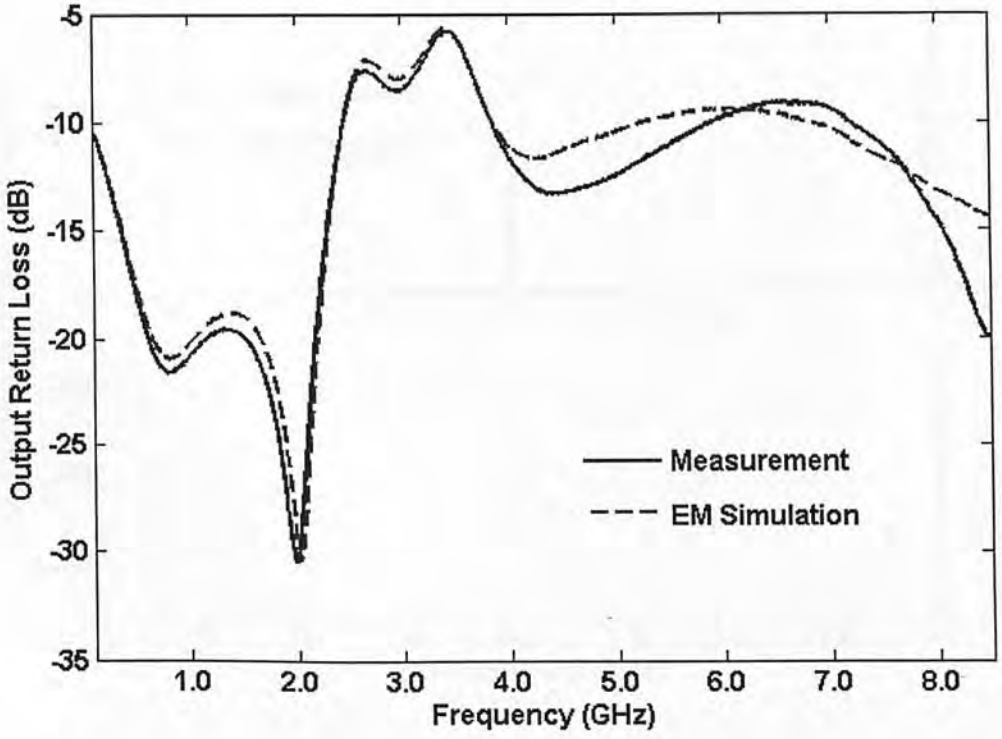


Figure A2.16 Simulated and measured output return loss

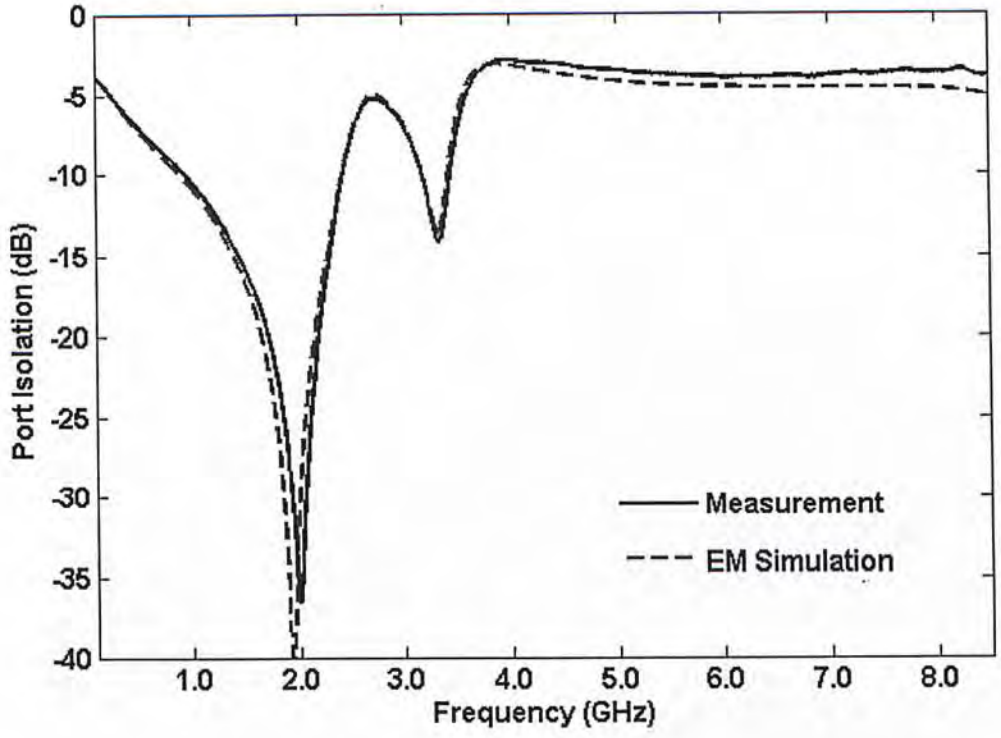


Figure A2.17 Simulated and measured port isolation

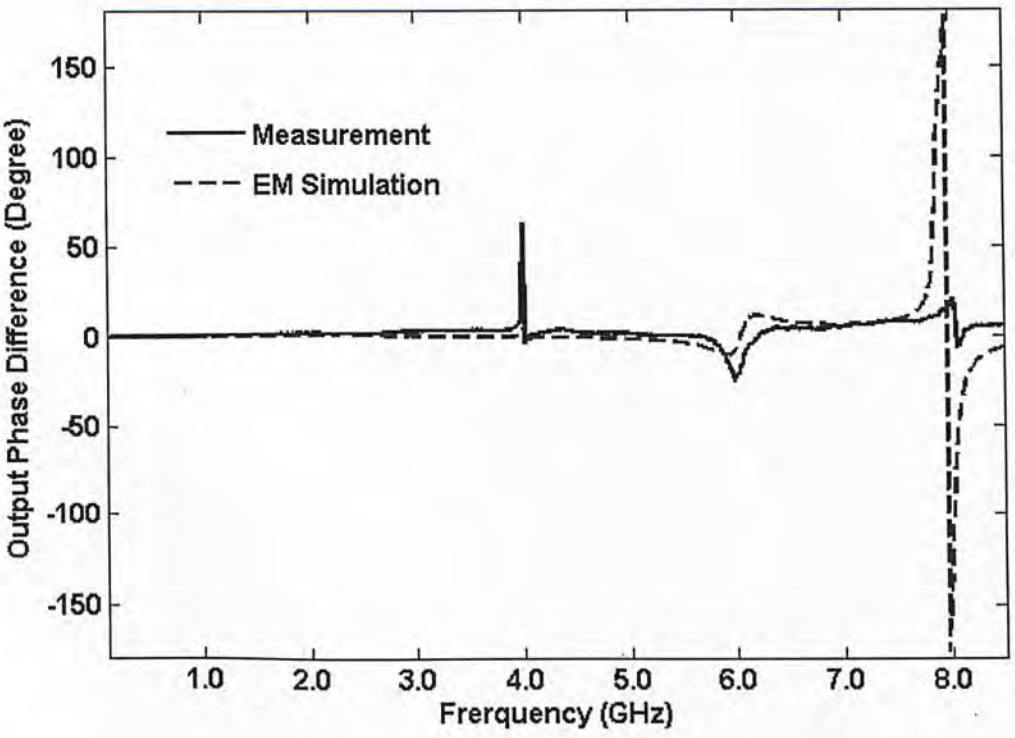


Figure A2.18 Simulated and measured output phase difference