Adiabatic Smart Card / RFID

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Abstract

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Smart card and Radio Frequency Identification (RFID) becomes popular research topic in recent years because of the wide range of applications. Different kinds of smart card and RFID systems, such as Philips Mifare card, microwave tag [Ryo2004] and organic tag [Can.2006], have been developed and applied to commercial applications. The smart card / RFID operating at 13.56MHz is one of the de-facto standard. Compact and low-cost transponder chips enable various secure authentication applications, such as Supply Chain Management and access control. The major issues of smart card / RFID design are low cost and low power consumption. The transponder chip presented here can meet these criterions.

Adiabatic logic is an approach to low power digital circuits that differs fundamentally from other practical low power techniques. The logic makes use of adiabatic switching technique to reduce power dissipation when charging or discharging the load capacitance. Adiabatic circuits are usually energized by an AC or clocked power supply, so that signal energy is recovered rather than dissipated as heat, by recycling signal charges back to the supply. The use of AC supply has two

drawbacks: latency introduced by the evaluate-hold phase scheme, and extra noise generated from the AC supply. Therefore, adiabatic logic is only suitable for low power applications, operating at low speed. We employ the Adiabatic-Quasi-Static CMOS (AQS-CMOS) logic in our design, which requires a two-phase AC power supply. With the newly developed flip-flops, both combinational and sequential logic circuits can be implemented with the AQS-CMOS logic.

A novel RFID tag, which stores an unique ID code for use in secure authentication applications, is developed with the AQS-CMOS logic,. The tag operates at 13.56MHz carrier frequency with a data rate of 200Kbps. The AC-powered AQS-CMOS logic allows the tag directly powered by the RF carrier without needing the full wave rectifier and regulator circuits for AC-to-DC conversion. This new architecture reduces chip size and power consumption of the RFID tag. A 64-bits RFID tag test chip is being fabricated with a 0.35 micron standard CMOS process. The test chip size is only 0.23mm-sq. and the logic core only consumes 20uW.

Moreover, an adiabatic smart card supporting half-duplex communication is developed, based on the same system architecture. The additional receiver front-end circuits, including the ASK demodulator and the clock recovery circuit, are designed and verified with a test chip in the same CMOS process.

摘要

因智能卡及射頻識別技術得到廣泛應用，近年來相關技術成爲熱門研究課題。不同的智能卡及射頻識別技術已經開發出來及發展至商業應用，如飛利浦的 Mifare 卡、微波識別卡[Ryo2004]及有機電子材料識別卡[Can.2006]。其中一個業界標準的智能卡或識別卡是在 13.56MHz 頻段運作。小型而低成本的卡上晶片提供具保密認證功能的應用，如供應鏈管理及考勤系統。智能卡或識別卡晶片設計特別講求低成本及低功耗。我們所設計的卡上晶片正符合上述要求。

絕熱式邏輯(Adiabatic logic)是一種低功耗邏輯電路技術，有別於其他普遍應用的低功耗技術。該邏輯利用到絕熱式交遞原理，減少負載電容充電及放電時的功耗。絕熱式邏輯電路需要由一個交流或帶有時鐘的電源驅動，因此訊號所帶有之電荷及能量得以回收到交流電源，避免功耗。交流電源會導致兩個問題：一是訊號延遲；二是噪訊增加。因此，絕熱式邏輯只適用於低速度、低功耗的應用。我們的設計會使用到絕熱式近似穩態互補式金氧半導體晶體管邏輯(Adiabatic-Quasi-Static CMOS logic, 簡稱 AQS-CMOS 邏輯) ，需要由二相交流電源驅動。加上新研發的觸發器，組合及時序式邏輯電路將可通過此絕熱式邏輯實現。

基於 AQS-CMOS 邏輯，研發出一個帶有獨立識別碼的射頻識別卡，可以用作一些需要保密認證功能的應用。此卡上晶片運作於 13.56MHz 頻段，能夠提供 200Kbps 數據傳送。在天線上耦合產生的射頻載波直接驅動晶片內含的邏輯電路，從而省卻用作交直流轉換的整流器及穩壓器。這嶄新的系統結構能縮減晶片尺寸及功耗。一個帶有 64 位元(64-bits)射頻識別卡測試晶片利用到 0.35 微米互補式金氧半導體晶體管工藝製造出來。該卡上晶片的面積爲 0.23 平方毫米，內核功耗爲 20 微瓦特。

此外，一個基於同樣系統結構，兼具雙向通訊功能的絕熱式智能卡亦被發展出來。額外的前端接收電路已研發出來及在晶片上通過測試，如 ASK 解調器及時鐘復原電路。

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1. Introduction

1.1. Low Power Design

Due to the rapid growth of portable electronics, reducing power consumption becomes a key design issue in the field of integrated circuit. Complementary metal-oxide-semiconductor (CMOS) has prevailed as the technology of choice for implement low power digital circuits. With the increasing complexity of digital integrated circuits, the power consumption is a major design challenge for current and future technologies. Switching power is the main power consumption in CMOS digital circuits and proportional to the square of supply voltage. Thus, reducing supply voltage is one of main strategies to low power design.

Adiabatic logic was proposed to be a novel approach for low power digital circuits. The adiabatic switching principle utilizes a clocked AC power supply to slowly charge the node capacitances, and then recover the energy associated with that charge, instead of dissipated as heat. Adiabatic Quasi-Static CMOS (AQS-CMOS) logic is one of the proposed adiabatic logic.

Our investigations found that AQS-CMOS logic can be applied to 13.56MHz smart card / RFID applications. The main advantage of applying adiabatic logic to smart card / RFID is the elimination of the full wave rectifier and regulator circuits.

In the following subsections, a review of power consumption in convention CMOS logic is given. Then the operating principle and architecture of conventional smart card / RFID are introduced.

1.2. Power Consumption in Conventional CMOS Logic

The average power consumption of conventional CMOS digital circuits can be expressed as the sum of three main components, the dynamic (switching) power consumption, the short-circuit power consumption and the leakage power consumption.

1.2.1. Dynamic Power

In CMOS digital circuits, power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. A precise measure of this energy consumption can be derived. Assuming that the input waveform has zero rise and fall times, the PMOS and NMOS devices are never on simultaneously. During the charge-up phase, the output node voltage typically makes a full transition from 0 to V_{DD}. The amount of energy E_{VDD}, taken from the supply during the transition, as well as the energy E_C, stored on the load capacitor at the end of the transition, can be derived by integrated the instantaneous power over the period of interest:

$$E_{VDD} = \int_0^\infty i_{VDD}(t)V_{DD}dt = V_{DD}\int_0^\infty C_L\frac{dV_{out}}{dt}dt = C_L V_{DD}\int_0^{VDD} dV_{out} = C_L V_{DD}^{\ 2} \qquad (1.1)$$

and

$$E_C = \int_0^\infty i_{VDD}(t)V_{out}dt = \int_0^\infty C_L\frac{dV_{out}}{dt}V_{out}dt = C_L\int_0^{VDD} V_{out}dV_{out} = \frac{C_L V_{DD}^{\ 2}}{2} \qquad (1.2)$$

This means that only half of the energy from the power supply is stored on C_L. The other half has been dissipated as heat in the conducting PMOS transistors. Notice that this energy dissipation is independent of the size (and hence the resistance) of the PMOS transistors. There is no energy drawn from the power supply during the discharge phase, yet the energy stored in the output capacitance during charge-up is dissipated as heat in the conducting NMOS transistors, as the output voltage drops

from V_{DD} to 0.

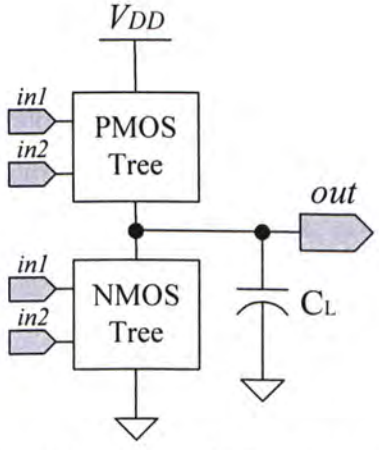


Fig. 1.1 A generic CMOS logic gate

To illustrate the dynamic power dissipation during switching, consider a generic CMOS logic gate in Fig. 1.1. A CMOS logic gate comprises of a NMOS tree and a PMOS tree and a load capacitance connected at the output node. The average power dissipation of a CMOS logic gate, driven by an input signal with a period of T, can be calculated from the energy required to charge up the output capacitance to V_{DD} and discharge the output to ground level.

$$P_{avg\_dynamic} = \frac{1}{T}\left[\int_0^{T/2} V_{out}(-C_L \frac{dV_{out}}{dt})dt + \int_{T/2}^{T}(V_{DD} - V_{out})(C_L \frac{dV_{out}}{dt})dt\right] \quad (1.3)$$

Solving Eq. (1.3) yields the well-known expression for the average dynamic power consumption in CMOS logic circuits.

$$P_{avg\_ynamic} = \frac{1}{T} C_L \cdot {V_{DD}}^2 = C_L \cdot {V_{DD}}^2 \cdot f_{clk} \quad (1.4)$$

The analysis presented is based on the assumption that the output node of gate undergoes one logic transition in each clock cycle. However, the node transition rate can be slower than the clock rate, depending on the circuit topology, logic style, and the input signal statistics. To better present this behavior, the average dynamic power consumption includes α_T (node transition factor), which is the effective number of logic transitions experienced per clock cycle.

$$P_{avg\_dynamic} = \alpha_T \cdot C_L \cdot {V_{DD}}^2 \cdot f_{CLK} \tag{1.5}$$

The dynamic power expressions of Eq. (1.4) and (1.5) are derived by taking into account of the voltage transitions at the output load capacitance C_L. In complex CMOS logic gates, however, most of the internal circuit nodes also make voltage transitions during switching. Since there is a parasitic capacitance associated with each internal node, these internal transitions contribute to the overall power dissipation of the circuits. In fact, the internal nodes may undergo several transitions while the output voltage remains unchanged. Thus, the overall dynamic power consumption may be underestimated if the internal node voltage transitions are not considered.

1.2.2. Short-Circuit Power

The dynamic power dissipation examined above is purely due to the energy required to charge up the load capacitance. Actually, a CMOS logic gate is driven with input voltage waveforms with finite rise and fall times, both PMOS and NMOS transistors may conduct simultaneously for a short time during switching, forming a direct current path between the power supply and the ground. This current component is called short-circuit current, which passes through both PMOS and NMOS transistors to the ground, but does not contribute to the charging of the load capacitances, as illustrated with a CMOS inverter in Fig. 1.2. The NMOS transistor of the inverter starts conducting when the rising input voltage exceeds the threshold voltage $V_{T,n}$. The PMOS transistor remains on until the input reaches the voltage level $(V_{DD} - |V_{T,P}|)$. As the output capacitance is discharged through the NMOS transistor, the output voltage starts to drop and this result in a non-zero

drain-to-source voltage on the PMOS transistor allowing it to conduct current. Thus, there is a short period during which both transistors are on and conduct current. The short-circuit current is terminated when the input voltage transition is completed and the PMOS transistor is turned off. A similar event happens during the falling input transition. The short-circuit current can be reduced by making the output voltage transition time larger or by making the input voltage rise and fall times smaller. When dealing with the short-circuit current, other performance parameters such as propagation delay and noise margin should also be considered.

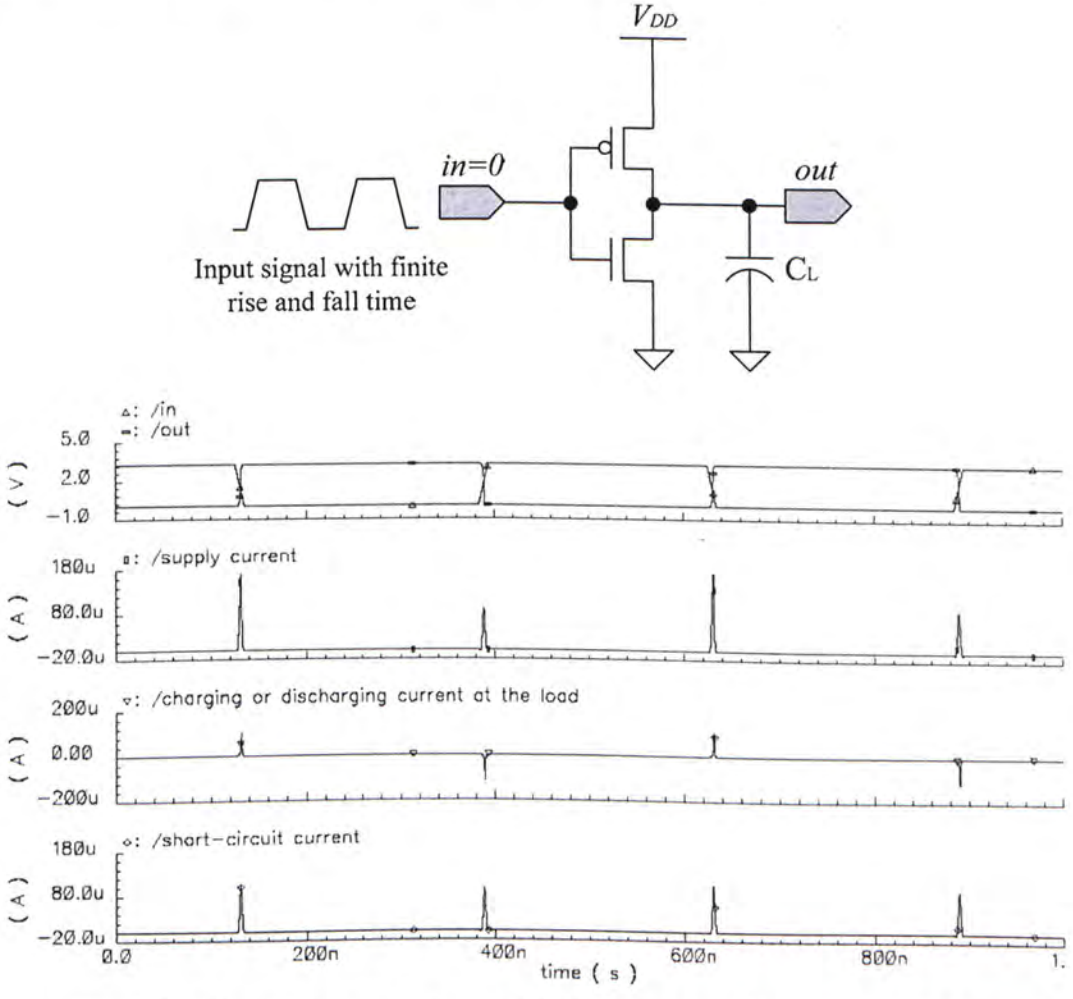


Fig. 1.2 Short-circuit current in a CMOS inverter with finite rise and fall time

1.2.3. Leakage Power

Ideally, static CMOS logic does not have static current, as the PMOS and NMOS devices are never on simultaneously in steady-state operation. There is, unfortunately, a leakage current flowing through the reverse biased diode junctions of the transistors. Fig. 1.3 illustrates the reverse diode leakage current in a CMOS inverter with a high input voltage, where the NMOS transistor is turned on and the output node is discharged to the ground. Although the PMOS transistor is off, there is a reverse potential difference of V_{DD} between its drain and the n-well (bulk), causing a reverse leakage current through the drain junction. Meanwhile, the n-well region of the PMOS transistor is also reverse biased with respect to the p-substrate. Therefore, another reverse leakage current exists at the n-well junction.

A similar situation can be observed when the input voltage is zero, as shown in Fig. 1.4, the PMOS transistor turns on and the output voltage is charged to V_{DD}. The reverse potential between the NMOS drain region and the p-substrate causes a reverse leakage current drawn from the power supply, through the PMOS transistor.

An emerging source of leakage current is the subthreshold current of the transistors. A transistor can experience a drain-source current, even when V_{GS} is smaller than the threshold voltage. The closer the threshold voltage is to zero volt, the larger the leakage current at $V_{GS} = 0V$ and the larger the leakage power consumption. The subthreshold leakage current in a CMOS inverter with a logic high input is depicted in Fig. 1.5. To offset this effect, the threshold voltage of the device has generally been kept high enough. But this approach is being challenged by the reduction in supply voltages that typically goes with deep submicron technology scaling.

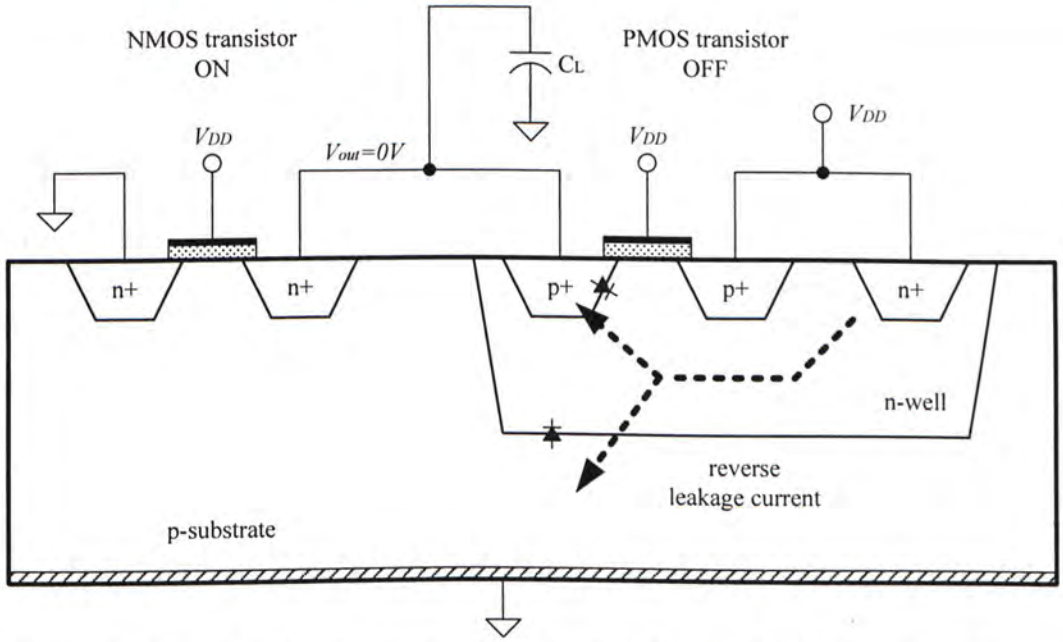


Fig. 1.3 Reverse leakage current paths in a CMOS inverter with a logic high input

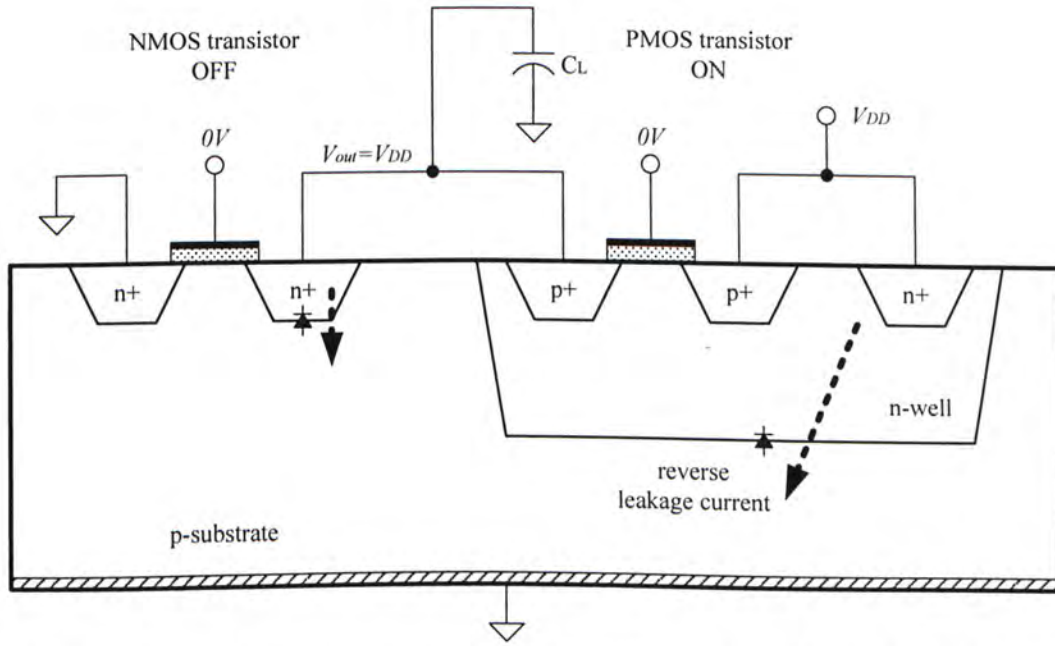


Fig. 1.4 Reverse leakage current paths in a CMOS inverter with a logic low input

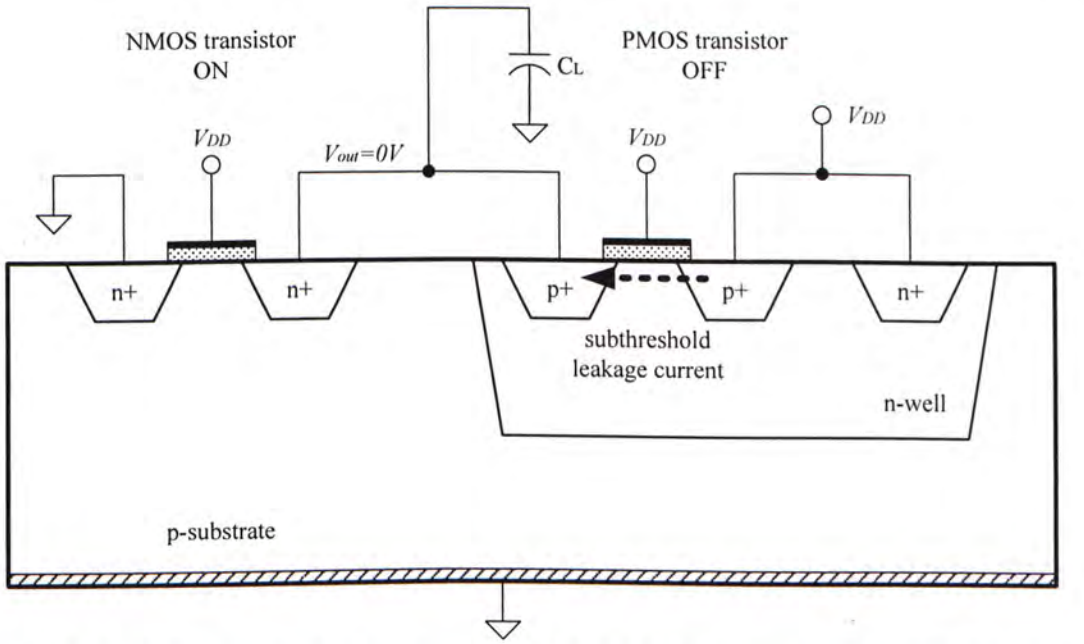


Fig. 1.5 Subthreshold leakage current path in a CMOS inverter with a logic high input

1.2.4. Static Power

In addition to the three major source of power consumption already discussed, some circuits may also consume static power. One example is pseudo-NMOS logic circuit, which utilizes a PMOS transistor as the pull-up device. Fig. 1.6 shows a pseudo-NMOS NAND gate with logic high inputs. The circuit exhibits a direct current path between V_{DD} and ground, which will contribute the static power consumption.

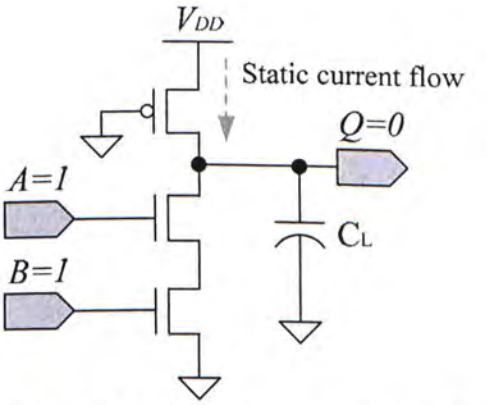


Fig. 1.6 A pseudo-NMOS inverter with logic high inputs

In summary, the total power dissipation in CMOS digital circuits can be expressed as the sum of four components,

$$P_{total} = \alpha_T \cdot C_{load} \cdot V_{DD}{}^2 \cdot f_{CLK} + V_{DD}(I_{short-circuit} + I_{leakage} + I_{static}) \qquad (1.6)$$

where $I_{short-circuit}$ denotes the average short-circuit current, $I_{leakage}$ denotes the reverse leakage current, and I_{static} denotes the DC current component drawn from the power supply. The dynamic power consumption, i.e. the first term in Eq. (1.6), is the dominating component in most cases.

1.3. Smart Card / RFID

A broad range of smart card / RFID applications are being used in our daily life. Starting from the traditional ticketing and supply chain management, the application will further extend in the coming years to allow identification of each item of goods in retail shops. To facilitate this trend, we need to build smart card/ RFID tags with low-cost and small form size. There are different kinds of smart card / RFID technologies, in terms of powering (active or passive), communication media (contact or contactless), operating frequency and fabrication material (silicon based or organic based). Our development focuses on the 13.56MHz contactless, passive, silicon based smart card / RFID tag design.

1.3.1. Applications

The smart card and RFID tags are quite similar, in term of working principle and system architecture. Sometimes, there is no clear boundary to differentiate them. In general, smart card has more processing power and complexity than the RFID. To give an example, an ISO 14443 standard compliant smart card [ISO14443] supports both Read and Write operations, and usually contains a microcontroller, an encryption engine and a programmable EEPROM. Such high functionality smart card enables secure tolling systems and access control applications, protecting the private information inside the tag from theft or counterfeit. Smart card is taking up the role of conventional magnetic-strip cards in financial and tolling applications, where fast and secure transactions are required.

The simple and small size RFID tags are suitable for cost-sensitive applications, such as animal identification, logistics, medical inspection and supply chain

management applications. A major application of RFID is for item-level identification in supply chain management [Ryo2004]. Attaching the RFID tag on each product and detecting the individual product unique ID code number which is linked to a computer database, an automatic identification and product tracking such as "when", "where" and "what" can be realized from product fabrication phase to market environments. Thus it really introduces an innovation of the product lifecycle management.

Some ultra low-cost RFID tags usually have Read-only operation [Ryo2004], which send a unique ID code stored in an internal ROM when activated by a field. Besides open systems requiring RFID chips which are ISO compatible, there are some users require proprietary RFID solutions for closed system applications.

1.3.2. Operating Principle

The smart card and RFID tags discussed in this work make use of the same operating principle. For an example of ISO 14443 standard compliant smart card, the contactless smart card operating at 13.56MHz is powered by and communicates with the reader via inductive coupling of the reader antenna to the card antenna. The two antenna coils effectively form a transformer. An alternating magnetic field is produced by sinusoidal current flowing through the reader antenna coil. When the card enters the alternating magnetic field, an AC voltage is induced in the card antenna coil. The rectifier and power regulator circuits inside the card convert the AC to a regulated DC voltage to power the internal circuits.

The reader amplitude modulates the RF field to send information to the card. The card contains a demodulator which converts the amplitude modulated signal to digital signal. The card also contains a clock extraction circuit that produces a

13.56MHz digital clock for use in the internal circuits.

The card communicates with the reader by modulating the load (either resistive or capacitive) of the card antenna, which in turn modulates the load of the reader antenna. ISO 14443 smart card uses a 847.5kHz subcarrier for load modulation, which allows the reader to filter the subcarrier frequency off the reader antenna and decode the data.

1.3.3. Conventional Architecture

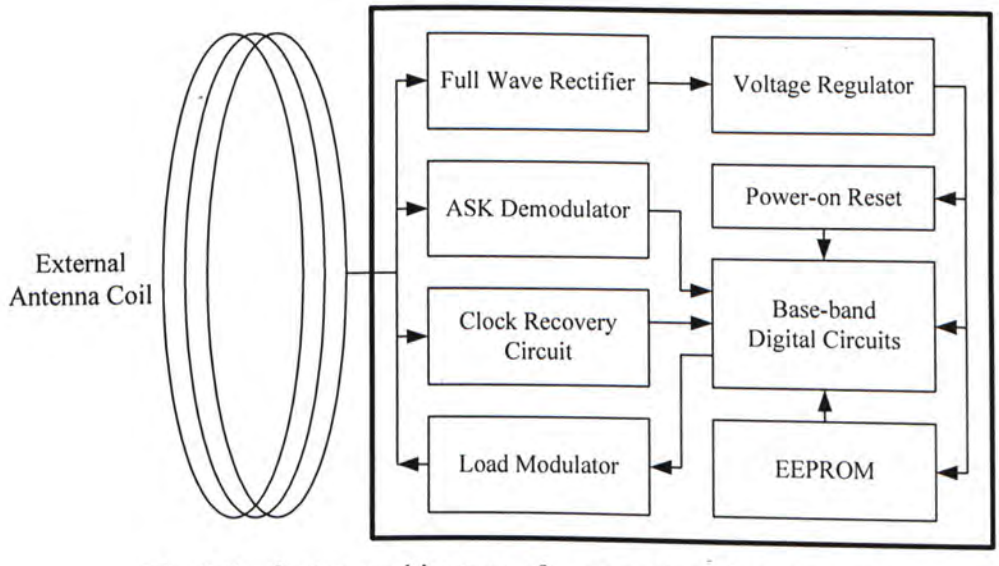


Fig. 1.7 System architecture of a conventional smart card

Fig. 1.7 shows the architecture of a conventional contactless smart card. The full wave rectifier and voltage regulator circuits convert the induced AC voltage to a DC supply voltage for the internal circuits. The demodulator demodulates the amplitude-shift-keying (ASK) signal from the reader. A clock recovery circuit generates a system clock from the RF carrier for the digital circuits. The base-band digital circuits include a microcontroller, an encryption engine and data storage elements, such as ROM and EEPROM. The data from reader is demodulated to digital signal and fetched in the base-band digital circuits for processing. The tag sends back the processed data to the reader through the load modulator.

RFID tag has a similar architecture of the smart card, the only difference is in the smaller base-band digital circuits for relatively simple protocol implementation compared to a smart card. Considering the Read-only RFID tag shown in Fig. 1.8, it further eliminates the demodulator circuit to achieve ultra low-cost and smaller form size. When the tag is powered up, the ring oscillator generates a system clock, which is used to clock the internal logic circuits. The ROM stores a unique ID code which is sent back to the reader by load modulation technique.

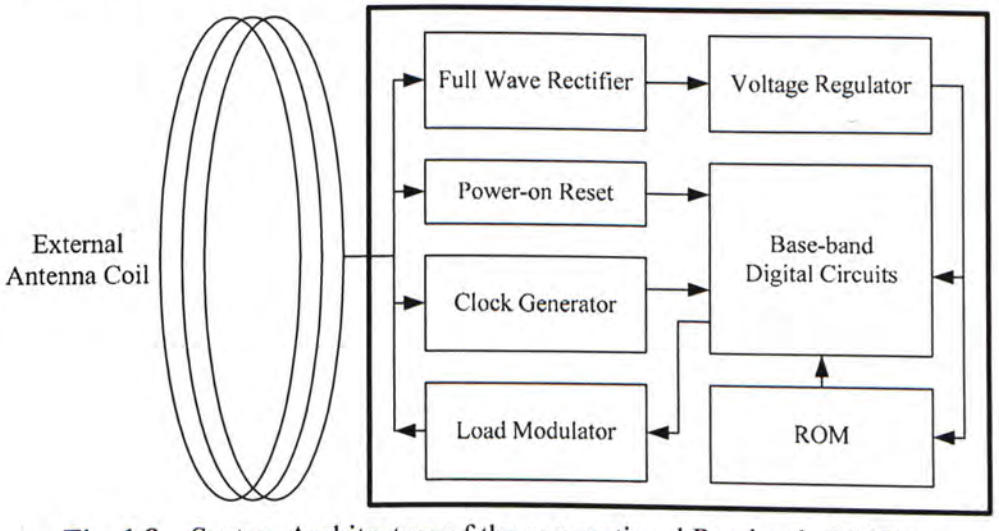


Fig. 1.8 System Architecture of the conventional Read-only RFID tag

2. Adiabatic Logic

Adiabatic logic is a new low power digital circuit design technique that differs fundamentally from other commonly used low power techniques. "Adiabatic" is a term used to describe thermodynamics processes that exchange no heat with the environment. Main concept of this methodology is to make an adiabatic operation in charging and discharging the load capacitance, usually with an AC or a clocked power supply (power-clock) with significant long rise and fall times.

2.1. Adiabatic Switching

For CMOS logic, the transistor act as a switch and the gate voltage is used to control the current flowing through the channel. Recall from Section 1.2, a CMOS logic gate consumes $\frac{1}{2}C_L \cdot {V_{DD}}^2$ of energy (i.e. switching energy) to charge or discharge a load capacitance. Energy dissipation is caused by the non-zero channel resistance of the transistors.

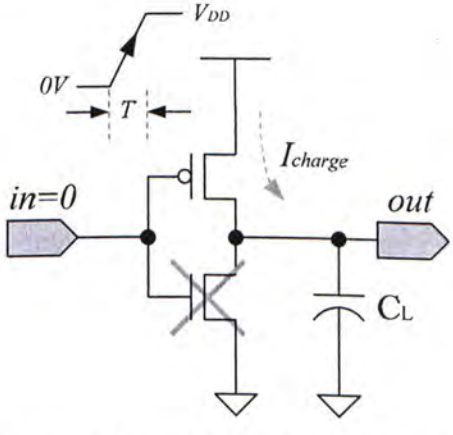


Fig. 2.1 Equivalent circuit of charging a load capacitance a CMOS gate by using a ramp voltage

It is interesting to note that slowing down the charge flowing through the channel or lowering the voltage across the channel, energy that would otherwise be

dissipated in the channel resistance can be conserved for later reuse. This advantage can be readily understood by using a ramp voltage as power supply to charge a load capacitance that delivers the charge $C_L \cdot V_{DD}$ over a time period T, as one can see in Fig. 2.1. The dissipation through the channel resistance R_{eq} is then:

$$E_{diss} = P \cdot T = I^2 \cdot R_{eq} \cdot T = \left(\frac{C_L \cdot V_{DD}}{T} \right)^2 \cdot R_{eq} \cdot T = \left(\frac{R_{eq} \cdot C_L}{T} \right) \cdot C_L \cdot V_{DD}{}^2 \qquad (2.1)$$

Eq. (2.1) shows that it is possible to charge or discharge a capacitance through a resistance while dissipating less than $\frac{1}{2} C_L \cdot V_{DD}{}^2$ of energy when the rise and fall times are set much longer than the natural time constant of the node. We refer to this as the principle of adiabatic charging [Wil.1994], which means that all charge transfer is to occur without generating heat. Fully adiabatic operation is an ideal condition that the energy dissipation approaches zero as the process is slowed down.

Switching circuits that charge and discharge their load capacitances adiabatically are said to use adiabatic switching. This type of circuits relies on special power supplies that provide accurate clocked power delivery. It is important to note that adiabatic logic can be regarded as a low power design approach only if the supply can generate and deliver the clocked power efficiently.

Refer to Fig. 2.1 again, assuming the PMOS transistor conducts in linear region when a relatively slow ramp voltage is used to charge up the output capacitance. Hence, the resulting equivalent resistance is:

$$R_{eq} = \frac{1}{u_p \cdot C_{ox} \cdot \left(\frac{W}{L} \right)_p \cdot (V_{DD} - V_T)} \qquad (2.2)$$

and the energy dissipation described in Eq. (2.1) becomes

$$E_{diss} = \frac{C^2 \cdot {V_{DD}}^2}{T \cdot u_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_p \cdot (V_{DD} - V_T)} \tag{2.3}$$

Minimizing Eq. (2.3) with respect to V_{DD}, we find that the minimum energy dissipation can be achieved when $V_{DD} = 2V_T$. Note that low power dissipation can be determined only if the signal voltage is significantly greater than the threshold voltage of the CMOS devices. On the other hand, when signal voltage is scaled down, close to the threshold voltage, the low power advantage of adiabatic logic will diminish rapidly.

Adiabatic logic circuits consume low power with a tradeoff in the operation speed. Generally adiabatic logic circuits can operate with power-clock frequency up to 150MHz and the adiabatic logic circuits still outperform the conventional CMOS circuits in term of power consumption [Voj.1997, Wil.2000]. Therefore, adiabatic logic circuits are most likely suitable for applications where speed is not a critical problem.

2.2. Energy Recovery

For CMOS logic, the charge at the load capacitance is discharged to the ground and the signal energy associated with the charge is dissipated as heat. Instead, adiabatic logic can conserve this energy by recycling the charge back to the AC or clocked power supply during the discharge phase [Wil.1994]. In adiabatic logic circuits, the power supply is usually implemented with a resonant circuit that can recycle the charge stored in the load capacitance and reuse it in the next cycle. Fig. 2.2 shows the energy (charge) recovery process occurring in an AQS-CMOS inverter during the discharge phase. The accumulative energy loss, as shown in the bottom curve, is calculated by integrating the product of voltage and current delivered from

the power-clock. The energy loss has an oscillating behavior, because part of the energy supplied to the circuit is given back to the power-clock during the recovery phase.

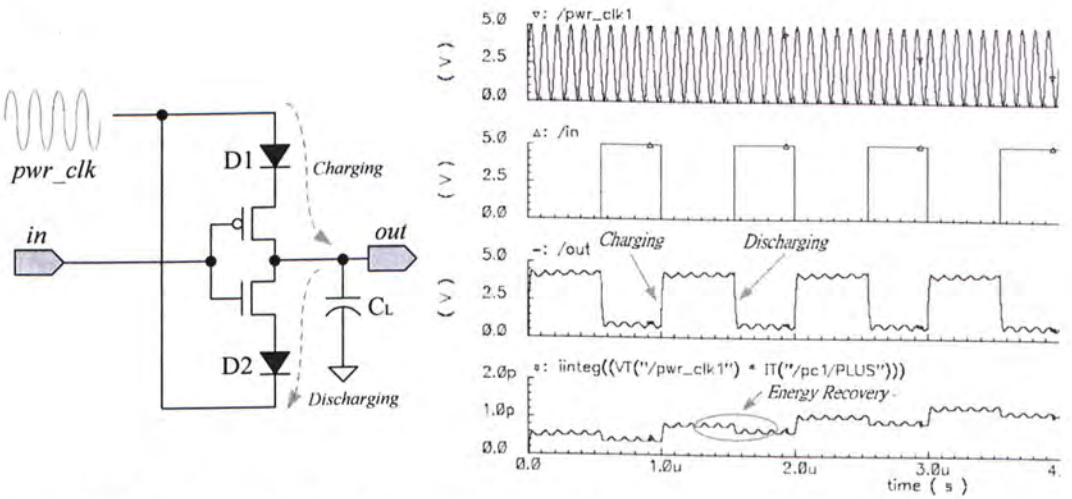


Fig. 2.2 Energy (charge) recovery process occurring in an AQS-CMOS inverter

Note that the AC power supply in our smart card / RFID applications is generated from the center-tapped antenna coil, from which the power is obtained from the reader coil by magnetic coupling. Energy (charge) recovery technique works as well in such transformer-like supply.

2.3. Adiabatic Quasi-Static CMOS Logic

Many adiabatic logic families, such as PAL [Voj.1997], 2N2P [Alioto2000] and ECRL [Yong1996], have been proposed in the past decade. Most of them require multi-phase clocking schemes with complex timing criteria and the output is dynamic in nature which makes it not compatible with conventional CMOS logic. Additional interface circuits are required to convert static input into adiabatic signals and vice versa.

Adiabatic Quasi-Static CMOS logic has several advantages over other adiabatic logic families:

1. It has a less complex clocking scheme with a two-phase power-clock, while some other adiabatic logic needs a more complex clocking scheme, such as four-phase clock.
2. The circuit topology is very similar to conventional CMOS logic. Many circuit techniques developed in CMOS logic can be applied to AQS-CMOS logic.
3. The logic output is quasi-static and compatible with conventional CMOS logic, no extra interface circuit is required.

2.3.1. Logic Structure

Consider the generic AQS-CMOS logic gate shown in Fig. 2.3. A load capacitance C_L, representing the input capacitance of next logic stage and parasitic capacitances, is connected to the power-clock through a charging path and a discharging path. The charging path is composed of a diode and a PMOS tree, while the discharging path is formed by a diode and a NMOS tree. The diodes act as current direction barriers and are implemented by n-well diode in standard CMOS

process. The PMOS and NMOS logic functions are the same as conventional CMOS logic.

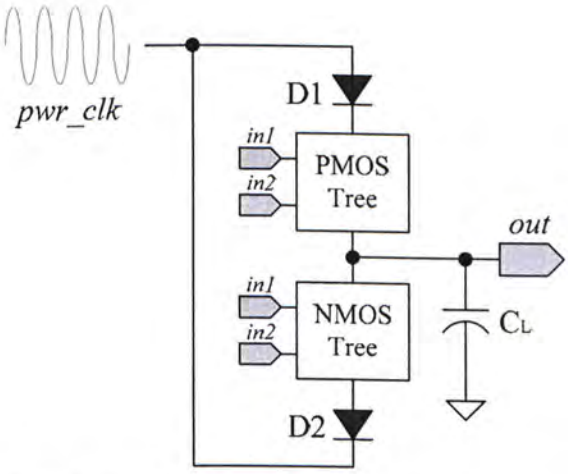


Fig. 2.3 A generic AQS-CMOS logic gate

Being a complementary logic, while the PMOS tree conducts, the NMOS tree cut off. In this case, along the rising edge of the power-clock, once the power-clock reaches the threshold voltage of the diode ($D1$) in the charging path, the diode conducts and the load capacitance is adiabatically charged. Note that the output is charged to the peak voltage of the power-clock minus the forward voltage of the diode and this is not a fully adiabatic process because the diode actually consumes power when conducting current. The charge at the load is kept from discharge, being quasi-static, because of reverse biased diode ($D1$) in the charging path at the falling edge of the power-clock and the non-conducting NMOS tree as long as the input holds its state.

While the input is switched, the PMOS tree is off and the NMOS tree conducts. As the diode ($D2$) in the discharging path is forward biased at the falling edge of the power-clock, the charge at the load is discharged and recovered back to the supply, along the discharging path. However, when the output voltage falls below the forward bias voltage of the diode ($D2$), the diode becomes off and the residual

energy stored on the output capacitance cannot be recovered. Hence, this causes additional energy dissipation of the adiabatic circuits.

For a clear illustration with an AQS-CMOS inverter, Fig. 2.4 shows the simulated timing of both power clock and I/O signals. Note that there are ripples at the output because of non-ideal property (reverse leakage) of the n-well diode and any parasitic capacitance between the output node and power-clock. Although the ripples add extra noise to the logic, it will not cause any problem as long as the peak noise voltage is lower than the threshold voltage of the logic gate.

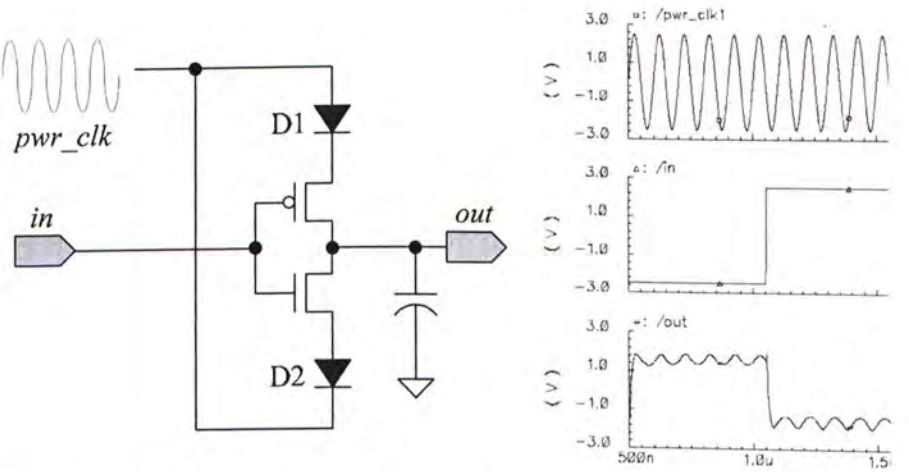


Fig. 2.4 An AQS-CMOS inverter and simulated timing of both power clock and I/O signals

2.3.2. Clocking Scheme

AQS-CMOS requires a two-phase clocking scheme. The two power-clocks are 180 degree out of phase of each other. Normally cascaded gates use alternative phase of the power-clock to prevent signal racing. Fig. 2.5 illustrates this case by two cascaded NOT gates energized by the two power-clocks respectively. The first gate evaluates with a logic low input to give a logic high output, by charging up its output capacitance at the rising edge of the power-clock (pwr_clk1). Meanwhile the second gate senses the logic high output evaluated by the first gate as its input, and

its associated power-clock (pwr_clk2) is in falling edge, so it discharges its output and gives a logic low output. The two gates have simultaneous logic transitions with respect to the rising or falling edges of the power-clock. And all logic transitions are synchronized to the rising or falling edges of the power-clock supply.

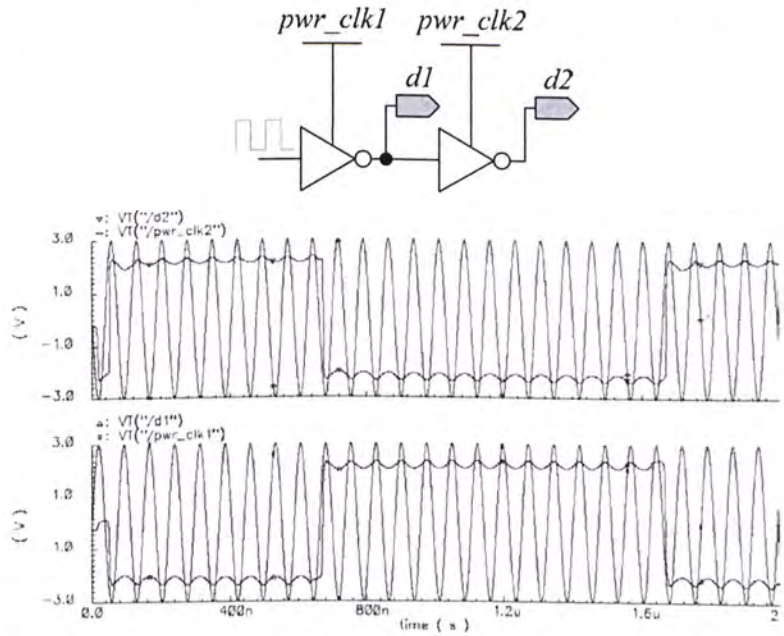


Fig. 2.5 Two cascaded AQS-CMOS NOT gates energized by alternative power-clocks and simulated timing of the I/O signals

If cascaded gates are powered by the same power-clock, this will introduce a latency of half power-clock cycle to each cascaded stage. Fig. 2.6 illustrates this phenomenon by looking at the outputs of three cascaded AQS-CMOS NOT gates energized with the same power-clock. Opposite logic transitions cannot happen simultaneously at the rising or falling edges of the power-clock. When the first gate has a low-to-high logic transition at rising edge of the power-clock, then the second gate starts the consequent high-to-low logic transition only at the succeeding falling edge of the power-clock. Therefore, the output of the second inverter has half power-clock cycle delay, while the third has one cycle delay at output. This technique provides a method to generate accurate time delay, which is referenced to the power-clock and independent of process variations. We will utilize this unique

property for the precise system clock generation by a specially designed ring oscillator, which will be discussed in later section.

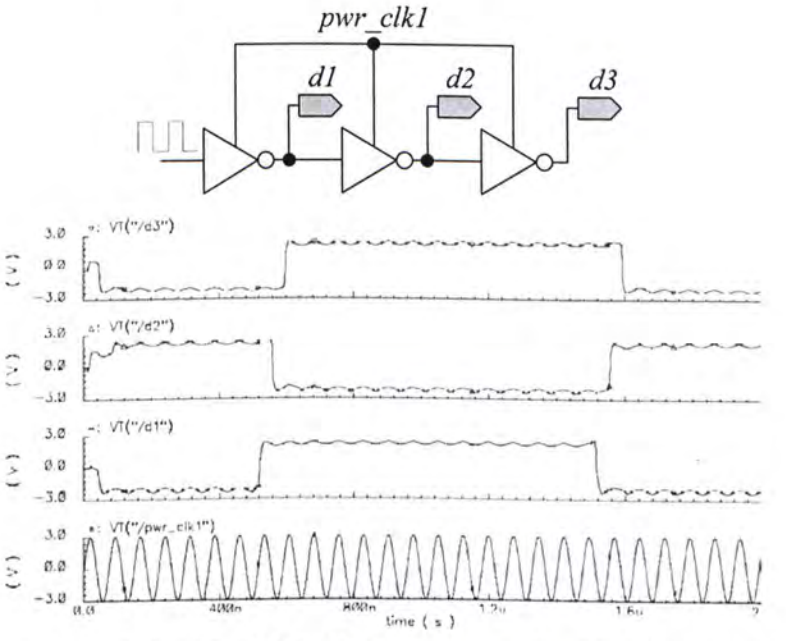


Fig. 2.6 Two cascaded AQS-CMOS NOT gates energized by the same power-clocks and simulated timing of the I/O signals

2.3.3. Flip-flop

Flip-flop, with its ability of storing state, plays a key role in sequential logic circuits. For example, the control logic for a ROM is sequential logic, so flip-flop based on AQS-CMOS logic technique has to be developed. The AQS-CMOS logic with quasi-static output, which can hold the logic state of an internal node, is more easier to implement flip-flop operation than other dynamic adiabatic logics. Two types of flip-flop based on AQS-CMOS logic are developed. The flip-flops inherit the characteristics of two-phase power-clock supply and energy recovery. Thus, AQS-CMOS logic proposed here enables a simple and straightforward implementation of both combinational and sequential logics, which is unavailable in other adiabatic logics.

2.3.3.1. Tri-state Inverter Type Flip-flop

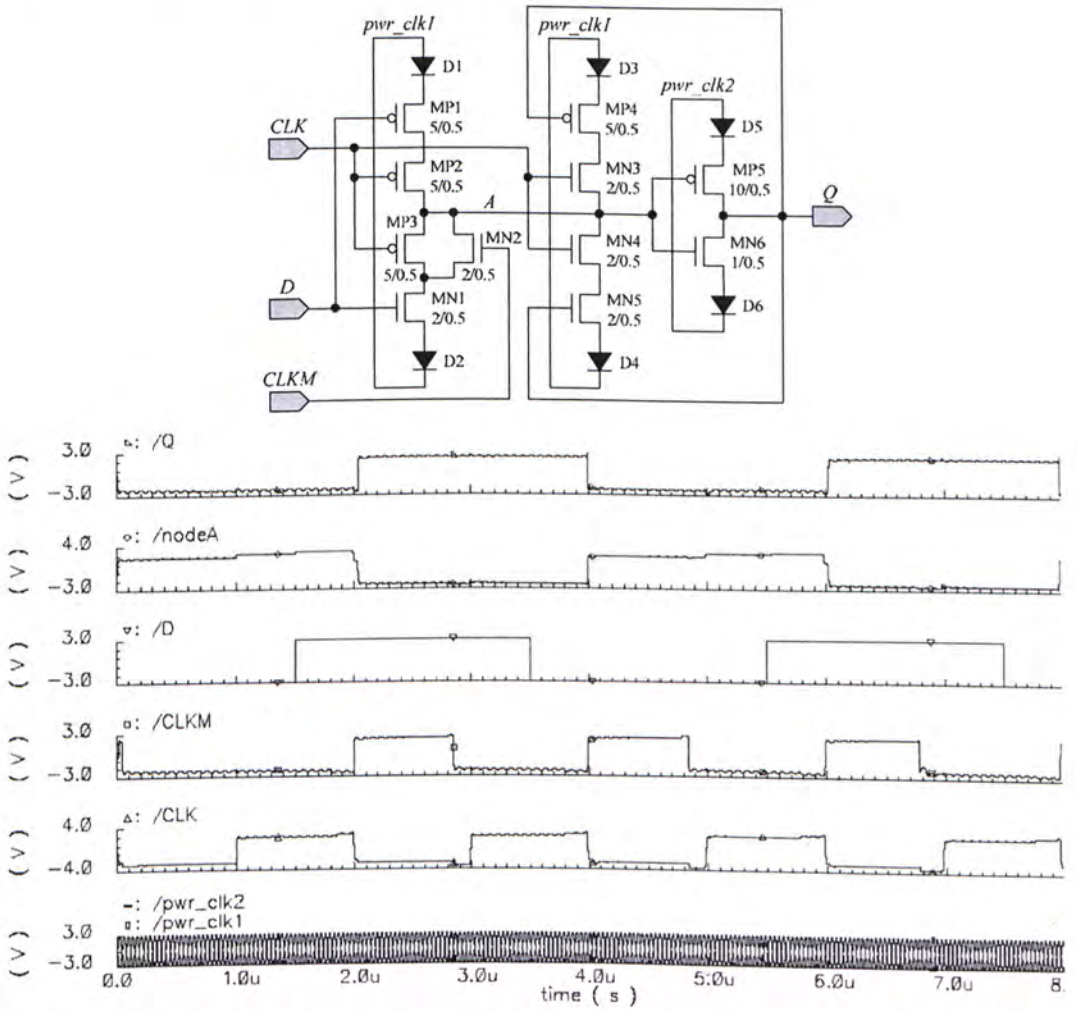


Fig. 2.7 Schematic diagram of an active-low evaluation latch based on AQS-CMOS logic and simulated timing of the I/O signals

The first flip-flop is derived from a conventional tri-state inverter based latch in master-slave configuration. Fig. 2.7 shows a basic active-low evaluation latch implemented in AQS-CMOS logic and its simulated I/O timings. As AQS-CMOS logic synchronizes logic transitions with the rising or falling edges of the power clock, a truly complemented clock signal is not available in this case. A single phase clock is used instead and the tri-state inverter is modified to have all the clocking transistors in PMOS or NMOS. This generates a problem for an active-low

evaluation latch, when latching an logic high input, node A is at the output logic low level plus one threshold voltage because the transistor $MP3$ cuts off when the voltage at node A drops below its threshold voltage. The solution is to add a discharge transistor $MN2$ at node A, clocked by a complemented clock ($CLKM$) with specially designed duty cycle. It provides an alternative discharge path during the latching phase. A similar case happens in the active-high evaluation latch, which requires an additional $CLKS$ clocked pull-up transistor, as shown in Fig 2.8. The clocking signals ($CLKM$ and $CLKS$) for the flip-flop can be easily generated from a ring oscillator. A D flip-flop is built by cascading an active-low evaluation latch with an active-high evaluation latch, as shown in Fig. 2.8. The simulated timing diagram indicates the signal takes a few power-clock cycles to propagate throughout the gates inside the flip-flop, so that the flip-flop should be clocked at least ten times lower than the power clock for correct operation. With a 13.56MHz power clock, the system clock is limited to around 1MHz, which provides enough throughputs for smart card / RFID applications.

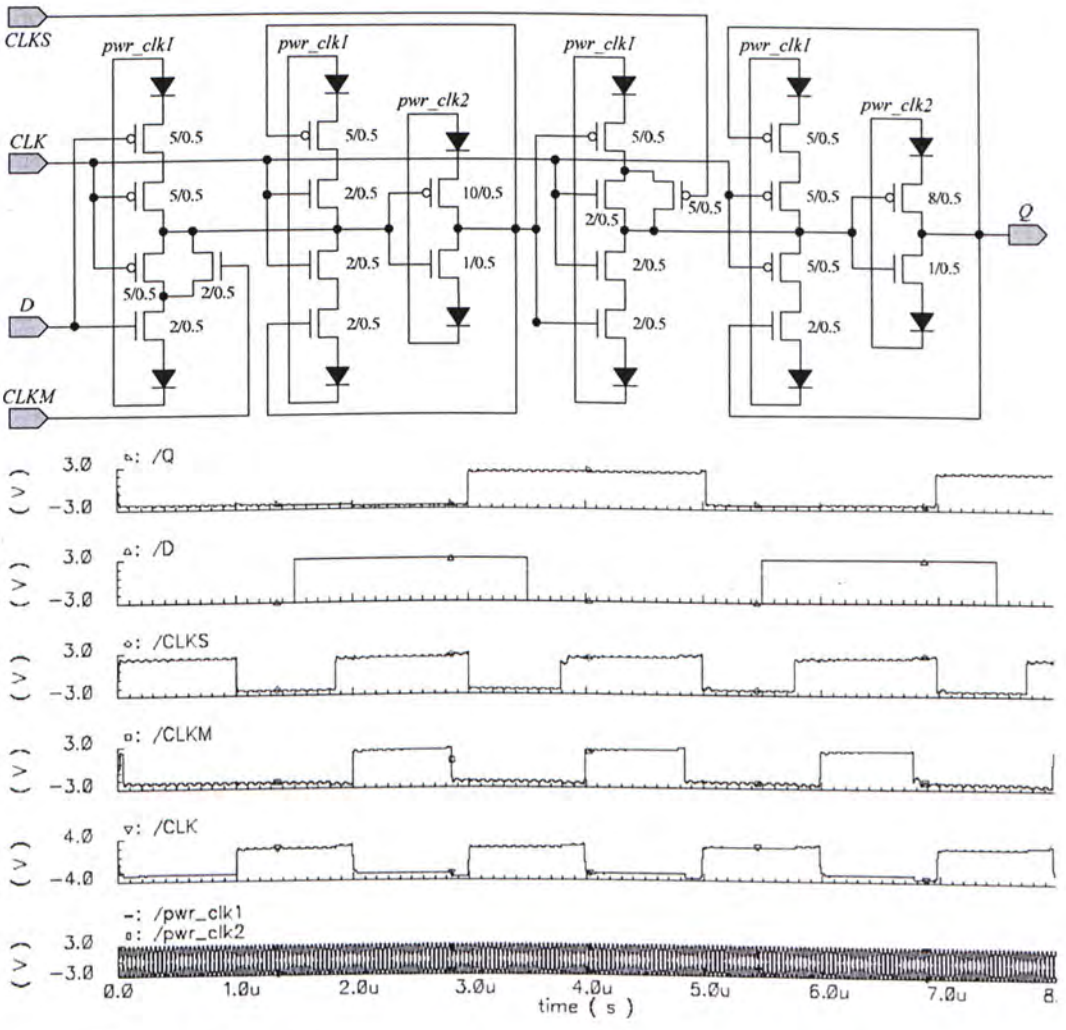


Fig. 2.8 Schematic diagram of a tri-state inverter type D flip-flop based on AQS-CMOS logic and simulated timing of the I/O signals

2.3.3.2. True-Single-Phase-Clock (TSPC) Flip-flop

A True-Single-Phase-Clock (TSPC) flip-flop based on AQS-CMOS logic has been developed as well. It has a similar structure of the static CMOS TSPC flip-flop [Mor.1990] and makes use of the same working principle. Fig. 2.9 depicts a basic positive edge triggered TSPC flip-flop and the simulated timing behavior. The flip-flop consists of only 9 transistors and is controlled by a single phase clock, allowing relatively compact and simple sequential logic implementation. Note that TSPC flip-flop is a dynamic flip-flop, it holds the state in hold phase by internal

nodal capacitances, in spite of feedback network. Therefore, the internal states have to be refreshed during each clock cycle and dedicated MOS capacitor is added to the internal nodes to increase the hold time of the flip-flop.

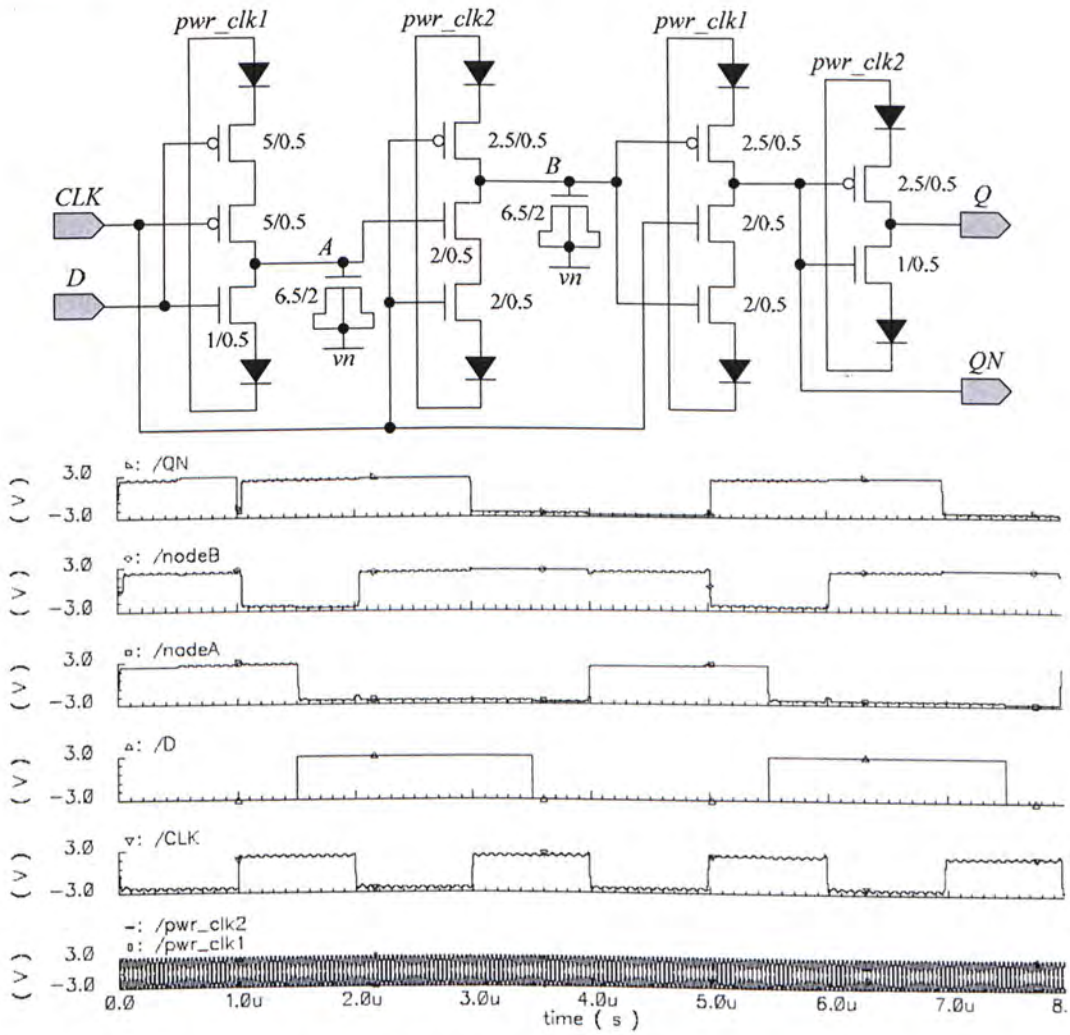


Fig. 2.9 Schematic diagram of a TSPC positive edge triggered D flip-flop based on AQS-CMOS logic and simulated timing of the I/O signals

Sometimes, there are glitches at the output of the TSPC flip-flop, one can see the simulated output (QN) has a glitch at 1us in Fig. 2.9. It is because node B cannot reach its final stage instantaneously at the rising edge of the clock (Remind that AQS-CMOS logic has logic transitions synchronous to the rising or falling edges of the power-clock.), these uncertain, intermediate stages appear at output (QN and Q) as glitches before reaching the final state. Therefore, designing sequential logic

circuits with such flip-flop needs special caution in the timing constraint, making it insensitive to those glitches.

2.3.4. Layout Techniques

For more systematic approach to architecture and floorplan design, an AQS-CMOS logic standard cell library is built. This allows fast and area efficient design of large circuit blocks, using auto-place-and-route function. The library is developed on a 0.35 micron, 4-metal, 2-ploy standard CMOS process. The logic cells developed in this work is for a 5-6 V(pk-pk) power-clock supply, thus they need to use thick-gate transistors with minimum channel length of 0.5 micron. Fig. 2.10 shows the schematic and layout of an active-low reset clear TSPC D flip-flop cell. According to the design rule, thick-gate transistors and n-well diodes require wider clearance, so the cell seems less compact compared to a conventional layout. The two power-clocks (pwr_clk1 and pwr_clk2) are distributed with the M3 metal lines at top and bottom of the cell, respectively. A narrow M1 metal line at the top of the cell is to provide a DC biases (vp) for the n-well with very little current flow, while a similar metal line at the bottom is for the p-substrate bias ($vp\_$ or vn). All logic cells are in the same height. For a more compact layout and further reducing the coupling between the two power-clocks, the logic cells are placed in such a way that inside the power ring, the two power-clock lines are distributed alternatively, with a row of logic cells in between. The cell placement structure is shown in Fig. 2.11. This structure allows the implementation of large scale AQS-CMOS logic circuits in an area-efficient way.

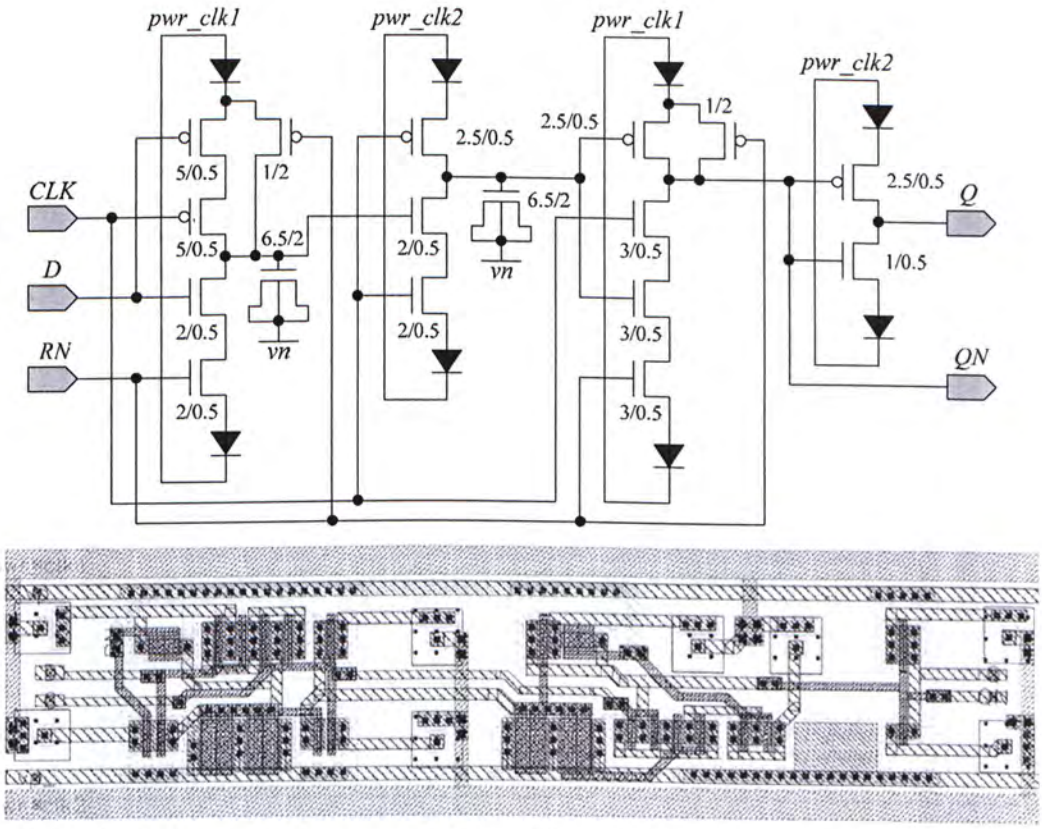


Fig. 2.10 Schematic diagram and layout of an AQS-CMOS active-low reset clear TSPC D flip-flop cell

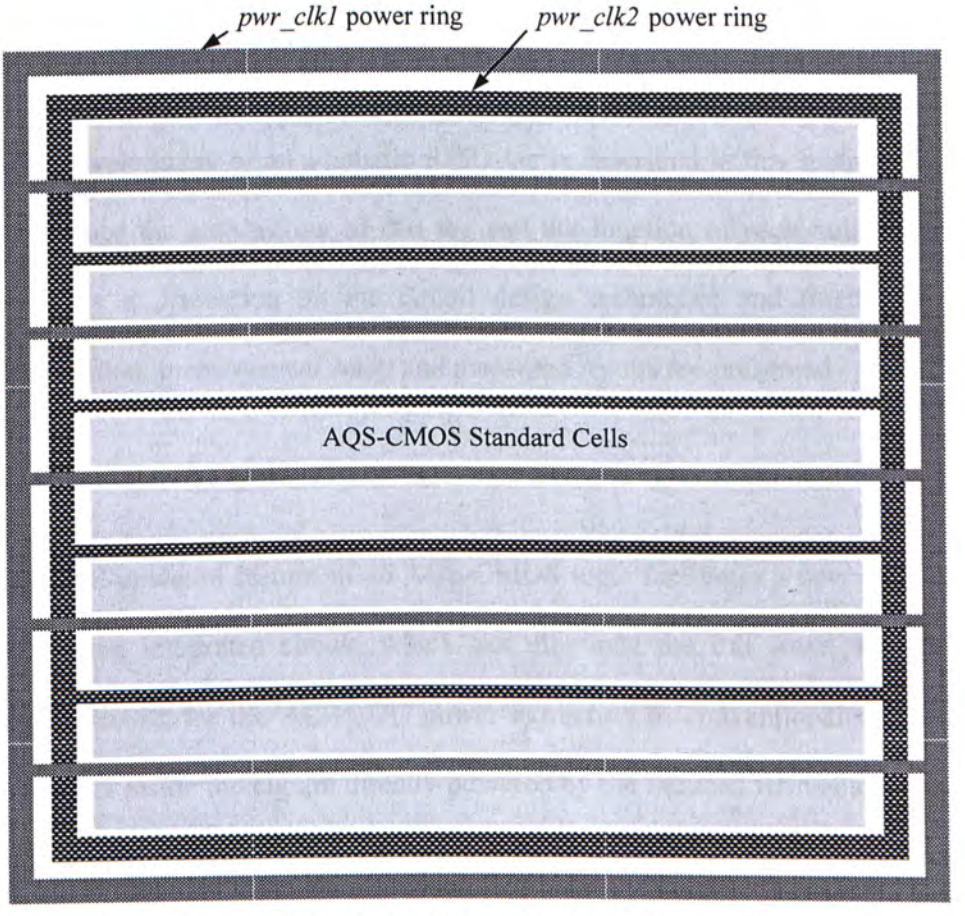


Fig. 2.11 AQS-CMOS logic standard cell placement structure

3. Adiabatic RFID

The development of an adiabatic RFID tag is described in this section. We will first introduce the architecture of this tag and the function of each building block, followed by a discussion on the circuit design techniques and finally the chip implementation, measurement setup and measured results are presented.

3.1. System Architecture

The AC-powered feature of an AQS-CMOS logic facilitates a new architecture for RFID tag integrated circuit, which can eliminate the full wave rectifier and regulator circuits for the AC-to-DC power extraction in conventional design. The logic circuits inside the tag are directly powered by the induced RF voltage from the antenna coil through a voltage limiter circuit. This architecture offers a direct and simple power delivery method, which does not require any complex analog circuits such as bandgap reference, high-current full wave rectifier and regulator circuits. Therefore, an adiabatic RFID tag consumes less power and uses smaller die area than conventional design.

Fig. 3.1 shows the system architecture of an adiabatic RFID tag, which comprises of a voltage limiter, a substrate bias generation circuit, a Power-On-Reset circuit, a ring oscillator, an ROM core with control logic and a load modulator. The induced AC voltage at the antenna coil directly powers the tag through a voltage limiter. The magnitude of the induced AC voltage is a function of the distance between the RFID tag and the reader. A voltage limiter is employed to clamp the varying induced voltage to a fixed amplitude, which is used to power the adiabatic circuits. At power-up, the Power-On-Reset circuit generates a reset signal to wake up

the internal circuits and sets an initial state for the sequential logic. The ring oscillator, ROM and control logic circuit are implemented in AQS-CMOS logic. Basic AQS-CMOS logic design techniques have been developed and reported in [Chan1997, Mak2000]. The ring oscillator provides a system clock for the sequential control logic. A dynamic ROM stores a unique ID code, which is mask programmed during fabrication. When the tag gets activated, the ROM content is read out serially, synchronized to the system clock, and passed to the load modulator. By changing the input impedance of the antenna and hence modulating the RF carrier, the modulator transmits the ID code to reader as an Amplitude Shift Keying (ASK) signal. By the effect of magnetic coupling, this ASK single can be sensed at the reader side.

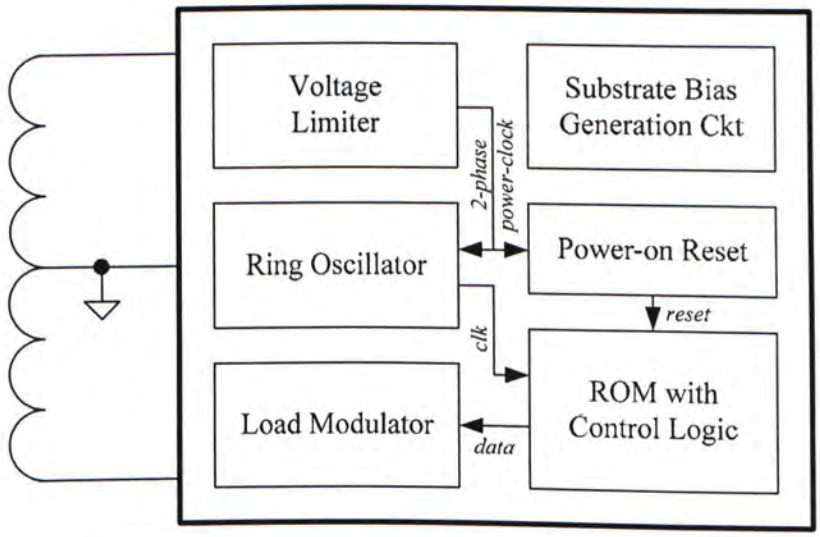


Fig. 3.1 System architecture of the adiabatic RFID tag

3.2. Circuit Design

The circuit design techniques of each building block are discussed one by one in the following subsections. In some cases, simulated results are provided for more detailed elaboration.

3.2.1. Voltage Limiter

The AC voltage induced at the tag antenna coil is varying in magnitude as a function of the distance between the tag and the reader antenna. The closer distance between the tag and the reader antenna, the stronger the induced RF voltage at the tag antenna coil. The voltage limiter aims to clamp the varying RF carrier voltage induced at the antenna coil to a fixed amplitude. The voltage limiter is simply a double-clamping diode circuit at each coil terminal, as shown in Fig. 3.2. Considering the upper side, the two diode chains ($D1-D4$ and $D5-D8$) connected in opposite direction form a clamping network. The n-well diodes are used here and have a forward voltage of around 0.7V. During the positive cycle, the output voltage is limited to approximately +3V which is equal to the voltage drop of 4 forward biased diodes. The diode chain ($D1-D4$) conducts and the other diode chain ($D5-D8$) cuts off. Thus the maximum output voltage is clamped at +3V. For the negative cycle of the induced voltage, the minimum output voltage is clamped at -3V, at which the diode chain ($D1-D4$) cuts off and the other diode chain ($D5-D8$) conducts. Therefore, the output voltage (pwr_clk1) has a fixed amplitude of around ±3V, as depicted in Fig 3.3. The bottom half of the circuit generates pwr_clk2 which is exactly 180 degrees out of phase compared to the pwr_clk1. These two signals are used to power the adiabatic circuits.

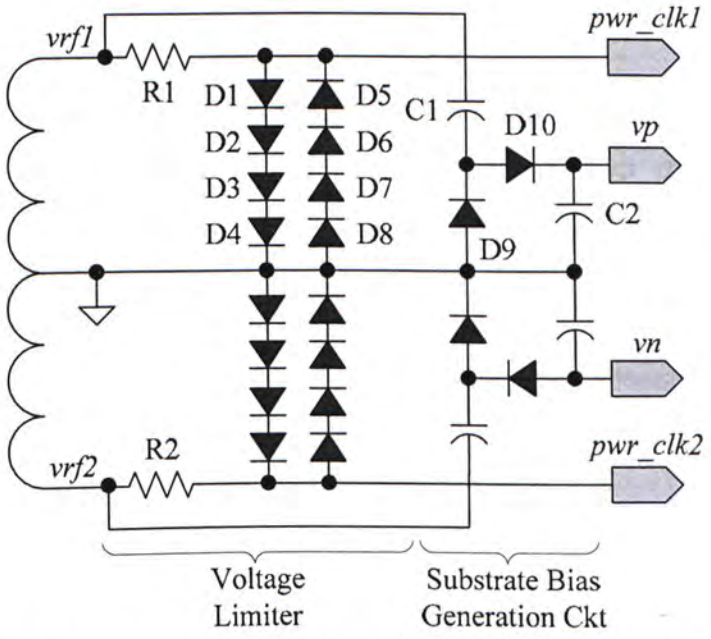


Fig. 3.2 Schematic diagram of the voltage limiter and the substrate bias generation circuit

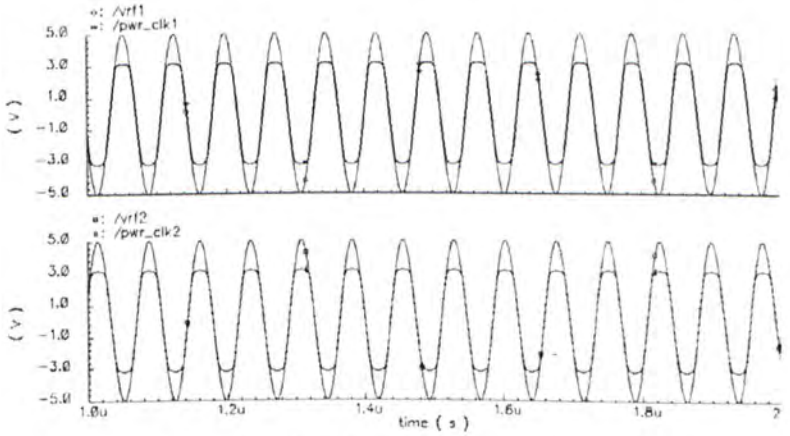


Fig. 3.3 Simulated results of the voltage limiter

The resistors $R1$ and $R2$ limit the current flowing from the antenna coil, which depends on the current consumption of the internal circuits. Assuming that the tag can operate at a minimum induced voltage of 7V(pk-pk), delivering a 274uA(rms) current at each antenna coil, the resistors ($R1$ and $R2$) are set to 1250 ohm. The calculation is shown in Eq. (3.1).

$$\frac{(7-6)V_{pk-pk}}{2\cdot\sqrt{2}} / 274uA_{rms} = 1250\,ohm \tag{3.1}$$

When the induced voltage gets so large that the induced current saturates the

conducting diodes (exceeds the saturation current of the diode), the clamping effect no longer exists and the output just follows the input. Experimental results reveal that the clamping network implemented in 0.35 micron CMOS process allows a maximum induced voltage input of 10V(pk-pk). Note that, for the 64-bits RFID tag currently developed, the current consumption of the internal adiabatic logic circuits is only around 10uA(rms), thus we have a very large design margin. Besides, it is important to balance the loading on the in-phase and anti-phase power-clocks, otherwise the induced voltage and current at the two antenna coils would be different.

3.2.2. Substrate Bias Generation Circuit

In CMOS technology, PMOS and NMOS transistors require a DC positive and a negative substrate (bulk) bias voltage, respectively. For AQS-CMOS logic energized with an AC power-clock, the substrate bias of PMOS transistors should be at or above the positive peak voltage of the power-clock (+3V in our design), while the substrate bias of NMOS transistors should be at or below the negative peak voltage of the power-clock (-3V). As shown in Fig. 3.2, voltage doubler circuit technique is used to generate these two substrate bias voltages (vp and vn) from the induced voltage at the antenna. Assuming that the tag operates with an induced voltage of 7-10V(pk-pk), the generated substrate bias voltages vary with the magnitude of the induced voltage. The generated vp and vn are at +5.8V and -5.8V respectively for a 7V(pk-pk) induced voltage, while vp and vn are at +8.3V and -8.3V for a 10V(pk-pk) induced voltage. Fig 3.4 gives the simulated results of a 7V(pk-pk) induced voltage. There is almost no current flow in the substrate, thus, we can use very small capacitor for the voltage doubler circuits. The capacitors $C1$ and $C2$

are in 3pF and 8pF respectively. In simulation, the substrate bias voltages have a ripple of less than 10mV with a leakage current for 10pA. Although the non-zero source-bulk voltage (V_{SB}) raises the threshold voltage of transistor by body effect, it will not affect the circuit performance because of the high supply voltage swing and low operating speed.

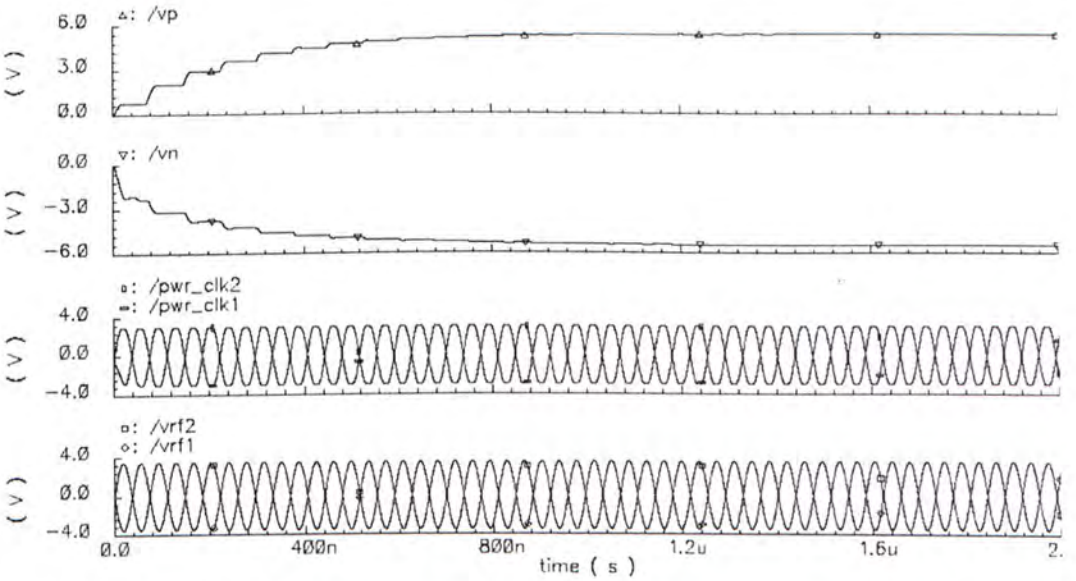


Fig. 3.4 Simulated results of the substrate bias generation circuit

3.2.3. Ring Oscillator

By making use of the delay characteristic of cascaded gates powered by the same power-clock, a ring oscillator based on AQS-CMOS logic is developed. Note that when AQS-CMOS cascaded gates are powered by the same power-clock, there is a latency of half power-clock cycle to each cascaded stage. The gate looks like to have an exact propagation delay of half power-clock cycle and constitutes a delay cell in the ring oscillator. Compared to the RC delay based ring oscillator, this technique can provide a method of clock generation, which is referenced to the power-clock and independent of process variations if the total delay is smaller than one cycle of the power-clock. A ring oscillator, consisting of 87 AQS-CMOS

inverters is used to generate a system clock of 200kHz. To balance the loadings on the two power-clocks, every five successive gates is tied to the in-phase and anti-phase power-clocks alternatively, as depicted in Fig. 3.5, Multi-phase clock signals are available at different nodes within the ring and used to generate the control signals for ROM data access. The simulated multi-phase clock signals are also included in Fig. 3.5.

At the beginning of every data transmission (packet), a synchronization bit pattern, 8 bits of alterative 1 and 0 as an example, is sent at first. The Phase-Locked Loop (PLL) of the reader makes use of this bit pattern to synchronize the clock, which is used for retiming of the data from the tag. This synchronization technique is commonly used for RFID systems.

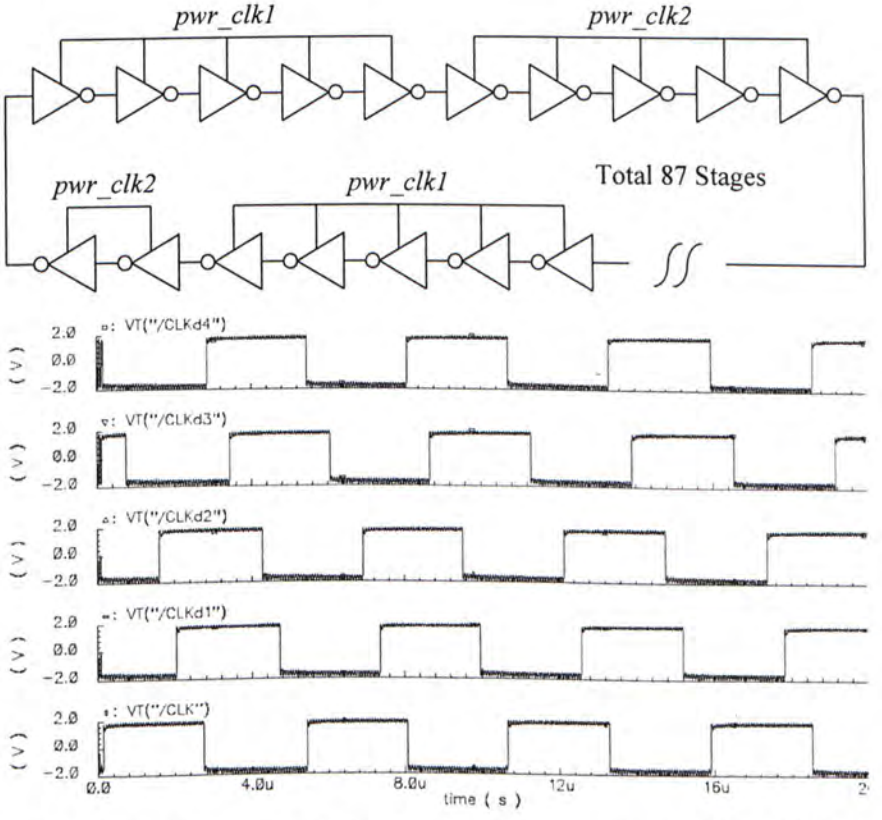


Fig. 3.5 Schematic diagram of the ring oscillator based on AQS-CMOS logic and simulated results of the multi-phase clock signals generated

3.2.4. ROM and Control Logic

A dynamic NOR-based ROM core is developed with AQS-CMOS logic. A read cycle consists of a precharge phase and an evaluation phase. This makes the ROM core only have dynamic power consumption at a cost of more complex control signals. The availability of multi-phase clocks from the ring oscillator facilitate the generation of such complex control signals. The ROM requires a two-phase read cycle. This dynamic ROM is only suitable for low speed applications, such as RFID. The ROM is designed for serial data read out. The block diagram of a 8x8 bits ROM core with control logic is shown in Fig. 3.6. Two barrel shifters are used to provide the column and row control signals for serial data read out. All shifters and control logic are designed with AQS-CMOS logic and flip-flops. The schematic diagram of the ROM core is depicted in Fig. 3.7. The ROM core is hardwired with a bit pattern in hexadecimal notation 'AA-8B-94-55-77-74-98-CC'. Each cell transistor stores a bit value of 0 or 1 either, by connecting the drain to the output node or not. A bit '0' is represented by a short, while a bit '1' corresponds to an open.

Consider a read cycle of the dynamic ROM core. The output node is precharged first. With appropriate signaling of the column and row shifters, a memory cell in the ROM core is accessed, by enabling the corresponding NMOS cell transistor. In case of a bit '0' stored in the memory cell, since the enabled cell transistor is connected to the output node, the charges at output node are discharged and hence a bit '0' is read. For a bit '1' stored in the cell, the unconnected cell transistor would not discharge the output node, thus a bit '1' is read.

At power-up, upon the reset signal from Power-On Reset circuit, the first bit of the row and column shifters are set, so that the first row and column are enabled. The

first data is read out and passed to the load modulator. Subsequent clock acts on the row shifter and the content of next row within the current column is read out. When a whole column is read, by clocking the column shift register, the following column is enabled and read out. Therefore, the content of the memory matrix is read out sequentially in the following order $CS0RS0$, $CS0RS1$, ... $CS7RS6$ and $CS7RS7$. Fig. 3.8 shows the timing of the control signals and read-out data for the dynamic ROM. Just for an illustration, only the first 16 bits read-out signals are showed in Fig. 3.8.

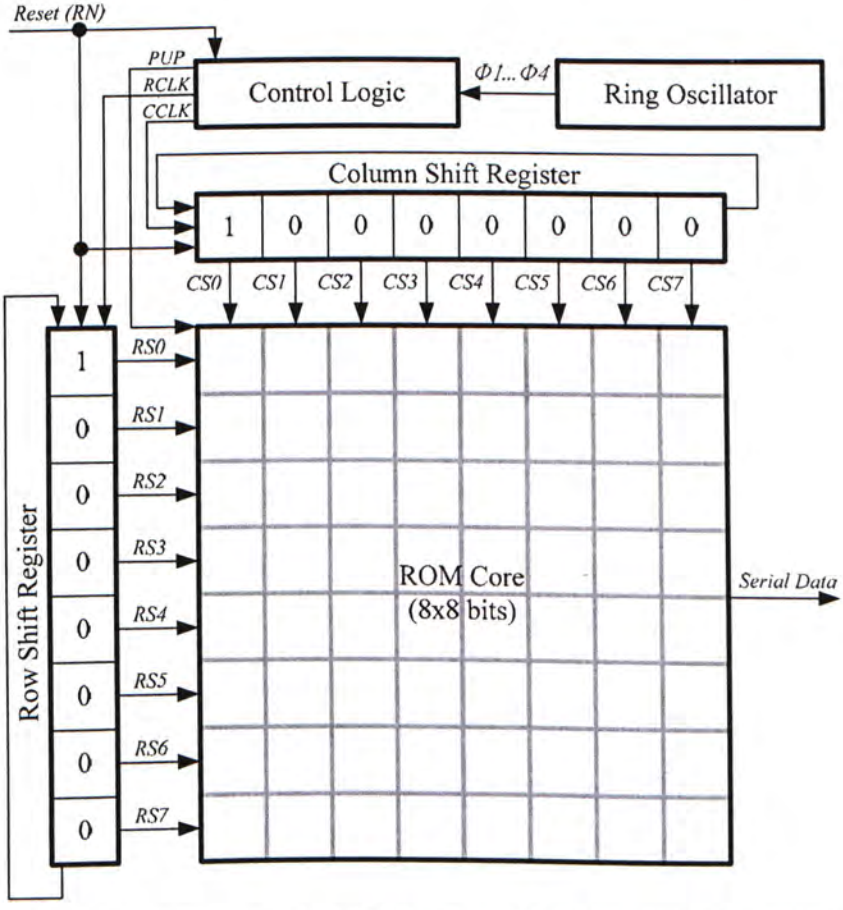


Fig. 3.6 Block diagram of a 8x8 bits dynamic ROM core with control logic

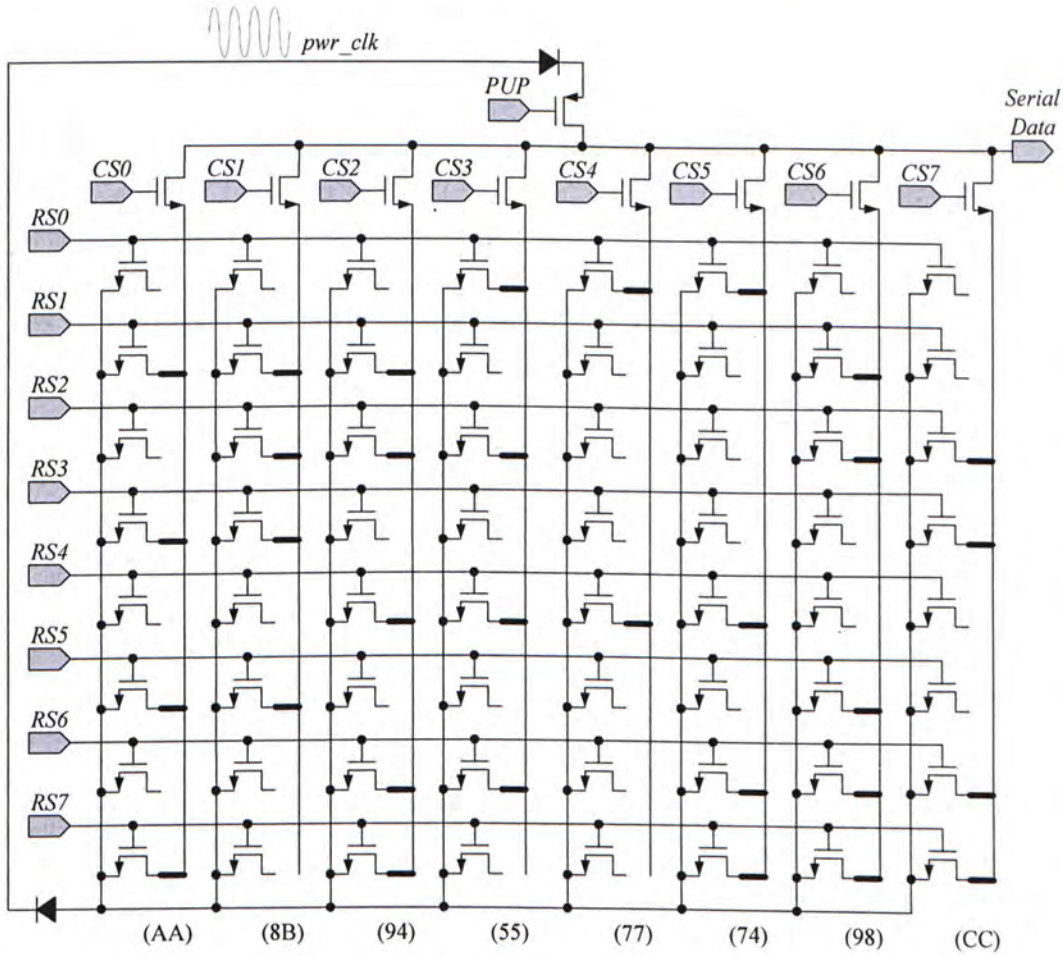


Fig. 3.7 Schematic diagram of a 8x8 bits dynamic ROM core based on AQS-CMOS logic

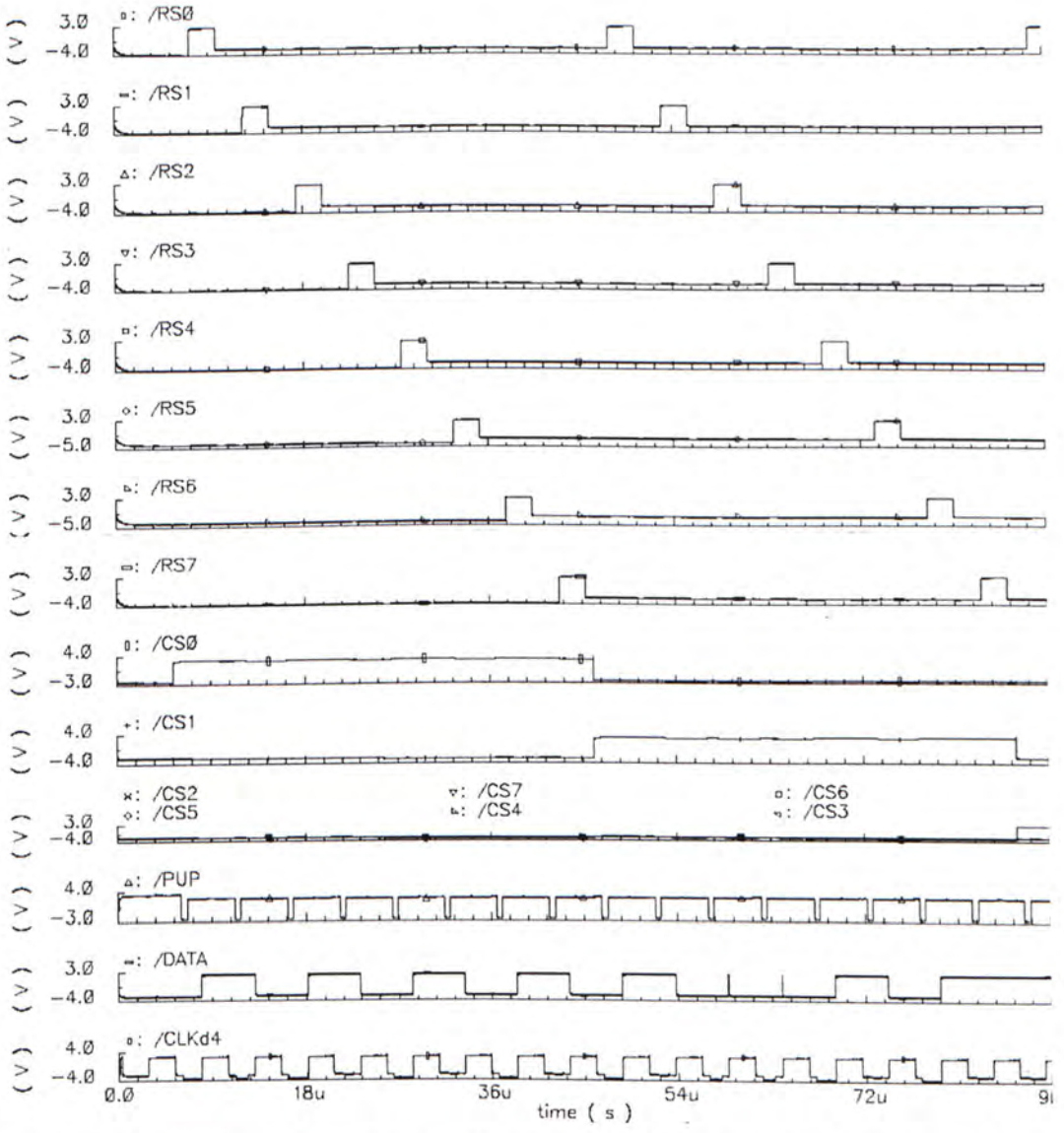


Fig. 3.8 Simulation results of the dynamic ROM core. From top to bottom: Row Select signals (RS0-RS7), Column Select signals (CS0-CS7), Precharge signal (PUP), Read-out data (DATA) and a clock signal (CLKd4).

3.2.5. Load Modulator

As shown in Fig. 3.9, a simple resistive load modulation technique is adopted in this design. The circuit consists of two diodes ($D1$ and $D2$) and a resistor ($R1$) and a switching transistor ($MN1$). Upon a logic high data, the switching transistor is on and the circuit effectively acts as a full wave rectifier. The top diode conducts current and the bottom diode is reversed biased in the positive cycle of the RF carrier, and vice versa in the negative cycle of RF carrier. While a logic low data is present, the switching transistor is off and no current flows in the load modulator. In this way, the modulator effectively changes input impedance of the antenna according to the ID code and transmits the code to reader by ASK modulation on the RF carrier. The ASK modulation depth can be scaled by the resistor $R1$.

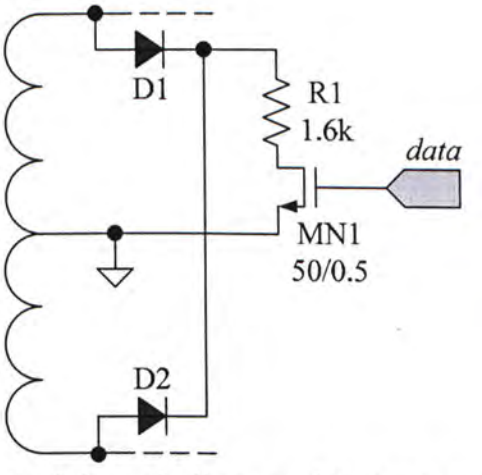


Fig. 3.9 Schematic diagram of the load modulator

3.2.6. Experimental Results

A 64-bits RFID tag test chip is designed and fabricated with *Austriamicrosystems* 0.35 micron standard CMOS process. The AQS-CMOS logic circuits operate with a power-clock of 6V(pk-pk), thus, thick gate transistors are employed in this design, which has a minimum channel length of 0.5 micron. Fig. 3.10 is a micrograph of the 64-bits RFID tag integrated circuit (IC). Each functional block is illustrated on the micrograph. The tag IC including three pads has a chip area of 0.23 mm-square (380 um x 600um in dimension). The IC is housed in a DIP-48 package, assembled with a double-side printed center-tapped antenna coil, to form a complete RFID tag. Fig. 3.11 shows a tag with a credit card size antenna and the following measurements are conducted with this tag.

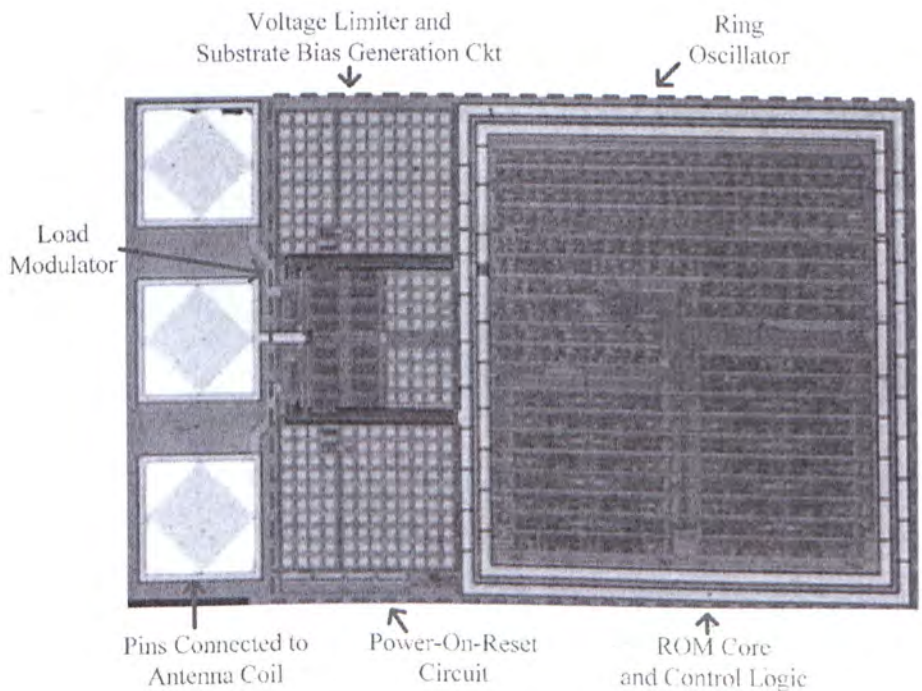


Fig. 3.10 Micrograph of the 64-bits adiabatic RFID tag IC

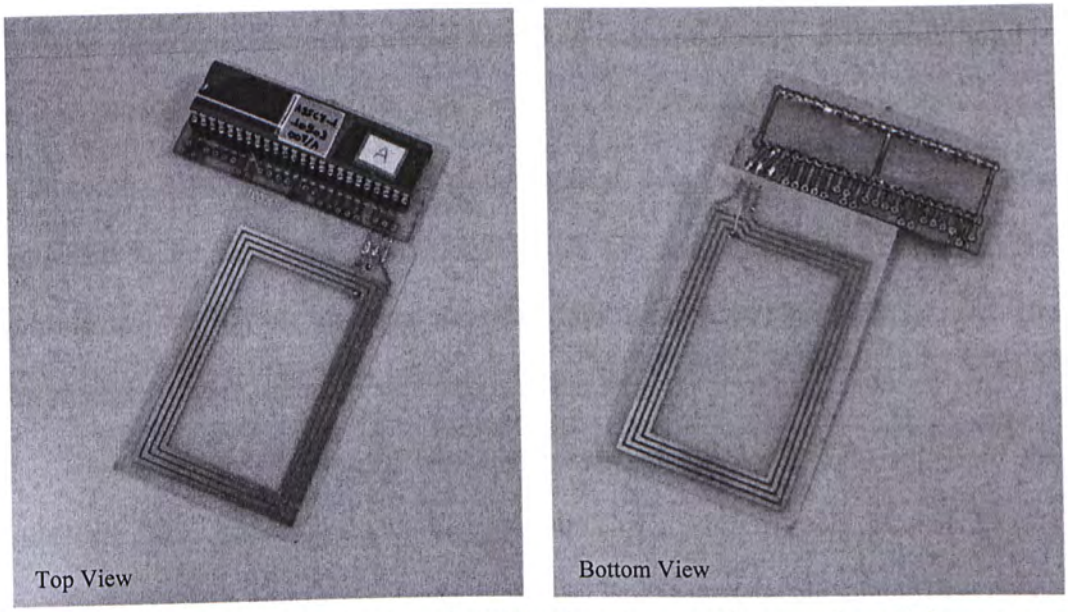


Fig. 3.11 An adiabatic RFID tag in DIP-48 package, with a credit card size antenna

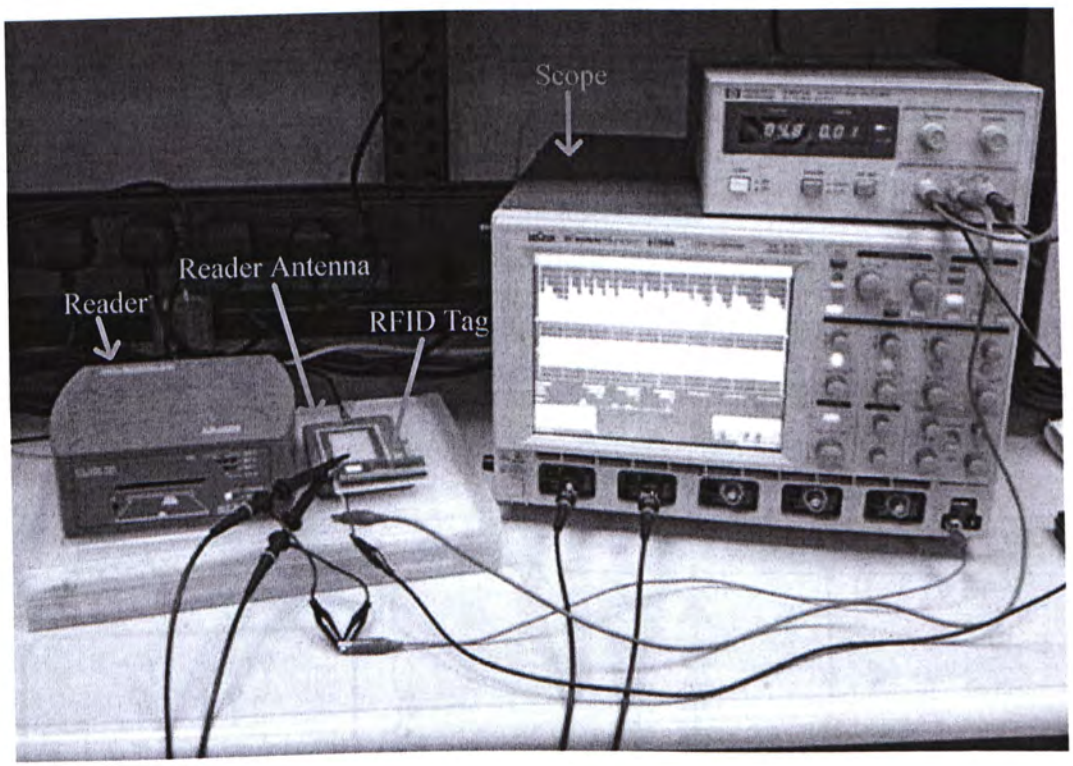


Fig. 3.12 Measurement setup for readout the RFID tag

The functional test setup of the RFID tag is shown in Fig. 3.12. A 13.56MHz smart card reader is used to generate an un-modulated magnetic field at its antenna, with controllable field strength. By placing the tag over the reader antenna, the tag is activated in the field and sends the ID code by modulating the RF carrier. The waveforms at the tag antenna terminals are probed by an oscilloscope. The instruments used in the setup are listed in Table 3.1.

During measurements, we found a mistake in the layout. The inputs of the substrate bias generation circuit (*vp* and *vn*) are wrongly routed to the power-clocks, instead of the antenna terminals. This makes the tag unable to generate the p-substrate bias. Initially the p-substrate bias is at 0V. As shown in Fig. 3.13, n-well junction of D1 is forward biased in the negative cycle of *pwr_clk2* and shorts the node to ground. Thus, the *pwr_clk2* signal becomes a half-rectified signal without the negative cycle, and the voltage doubler cannot generate a negative p-substrate bias voltage (*vn*) from this signal. In this case, the tag will never start up. To cope with this problem, we have to apply an external p-substrate bias to the test chip. This fault will not affect the performance of the test chip. The correct schematic diagram is shown in Fig. 3.2.

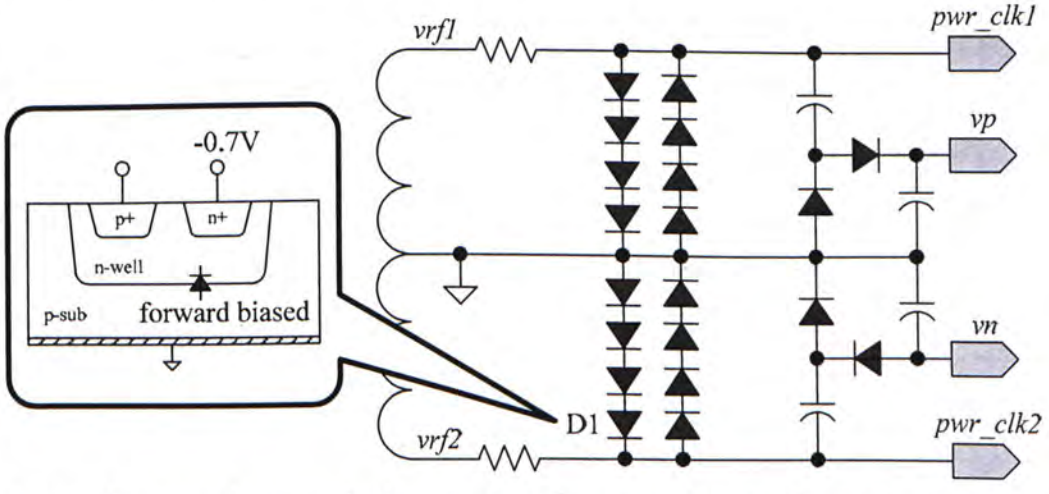


Fig. 3.13 A routing error in the substrate bias generation circuit causes startup fault of the RFID tag

Instrument	Model
13.56MHz Smart Card Reader	Mcropross Class 185
Oscilloscope	LeCroy WaveRunner 6100
DC Power Supply	HP E3611A

Table. 3.1 Instruments used in the measurement setup of the 64-bits adiabatic RFID tag

Fig. 3.14 gives the measured waveforms of the induced voltage at the tag antenna coil and the ASK signal presenting the ID code, notated in hexadecimal, from the tag. The code is exactly the one stored in the ROM core inside the tag. Moreover, the 64-bits ID code takes a time period of 325.4us to read, which means that the data rate and the system clock of the tag IC are equal to 197kHz. It is close to the simulation value of 200kHz. This shows that the ring oscillator functions properly. The ASK signal has a 200mV modulation depth for a 9V(pk-pk) RF carrier. The operating range of the tag is up to 3cm upon a magnetic field strength of 2.4A/m generated at reader antenna. Note that the operating range highly depends on the geometry and resonance frequency of both the tag and reader antennas.

Table 3.2 gives the power consumption of the tag at different induced RF carrier voltage at the antenna coil. In fact the power extracted from the antenna coil is partially dissipated in the current limiting resistors of the voltage limiter (i.e. $R1$ and $R2$ in Fig. 3.2) and the internal adiabatic logic circuits. Simulation tells that the adiabatic logic core inside the 64-bits RFID tag only consumes 20uW of power, the rest is dissipated in the diode chains of the voltage limiter. There is substantial headroom to facilitate more processing power, such as encryption engine or encoder, in the tag.

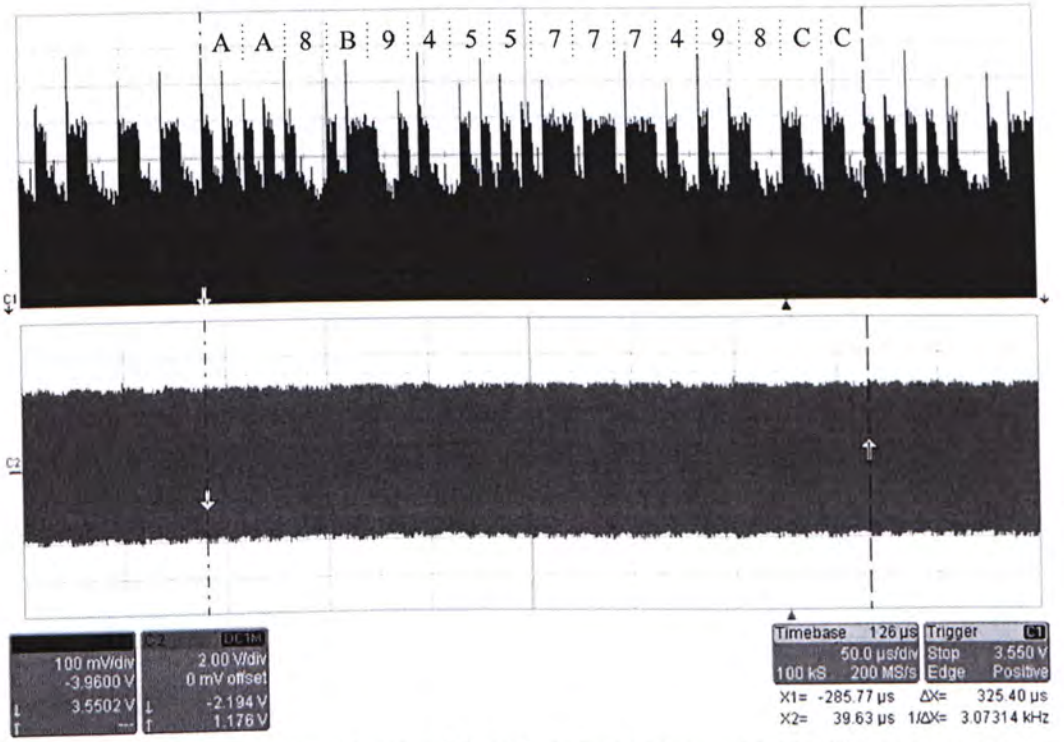


Fig. 3.14 Measured waveforms of the ASK signal presenting the ID code, notated in hexadecimal, and the induced voltage at the tag antenna coil

Induced Voltage[1]	**Induced Current[2]**	**Power Extracted from the Antenna**	**Power Available for the Adiabatic Logic**
7V(pk-pk)	548uA(rms)	1.36mW	1.16mW
10V(pk-pk)	2.06mA(rms)	7.28mW	4.37mW

1. The voltage is measured at one antenna terminal, reference to the center-tapped ground.
2. The currents in both in-phase and anti-phase antenna terminals are taken account.

Table. 3.2 Power consumption of the tag at different induced RF carrier voltage at the antenna coil

Fig. 3.15 further shows the measured waveforms of the in-phase and anti-phase RF voltages induced at each antenna terminal. The equal amplitudes imply that both in-phase and anti-phase power-clocks have equal loadings.

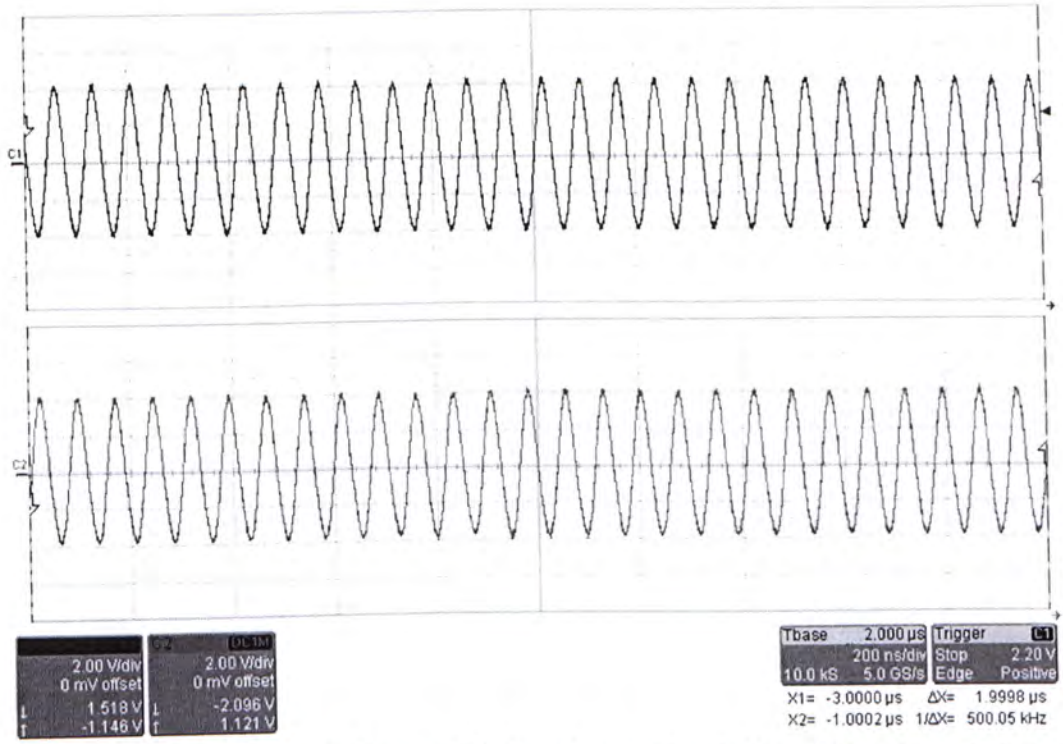


Fig. 3.15 Measured waveforms of the in-phase and anti-phase RF voltages induced at each antenna terminal

4. Adiabatic Smart Card

We have presented an adiabatic RFID tag in previous section, which only supports one-way tag-to-reader communication. Based on that design, an adiabatic smart card supporting half-duplex operations can be developed, by adding a receiver front-end circuit. The two-way communication allows handshaking communication protocol implementation for more secure data transfer. In the following subsections, the additional receiver front-end circuit is discussed and experimental results are provided as well.

4.1. System Architecture

Fig. 4.1 shows the system architecture of an adiabatic smart card. It makes use of the same circuits for power-clock extraction, substrate bias and load modulation, adopted from the adiabatic RFID tag. Additional circuits, including the ASK demodulator and clock recovery circuit, provide the function of receiving data from the reader. Throughout the two-way communication, the passive smart card is powered by and communicates with the reader via magnetic coupling between the two antennas. In the reader-to-card link, the reader transmits data by ASK modulation on the RF carrier. The ASK demodulator inside the smart card demodulates the data from the RF carrier. A clock recovery circuit is employed to recover the clock from the RF carrier, synchronous to the data being transmitted. The clock is used for retiming the data from the reader and clocking all the internal digital circuits. Then the base-band digital circuits process the received data and send back the response (data) to the reader by load modulation.

The front-end circuits of the adiabatic smart card are built compliant with the

ISO/IEC 14443 Type B standard. ISO/IEC 14443 Type B [ISO14443] is an international contactless smart card standard, which operates at a carrier frequency of 13.56MHz and supports half-duplex communication at a data rate of 106kbps. The reader-to-card link is by Amplitude Shift Keying (ASK) modulation with a 10% modulation index on the carrier, and the card-to-reader link is by Binary Phase Shift Keying (BPSK) modulation on a sub-carrier frequency of 847.5kHz.

As EEPROM cannot be powered by the AC power-clock and there is a lack of the AC-to-DC power conversion circuits, EEPROM cannot be integrated in the adiabatic smart card. A hardwired ROM becomes the only choice of storage elements for the adiabatic smart card.

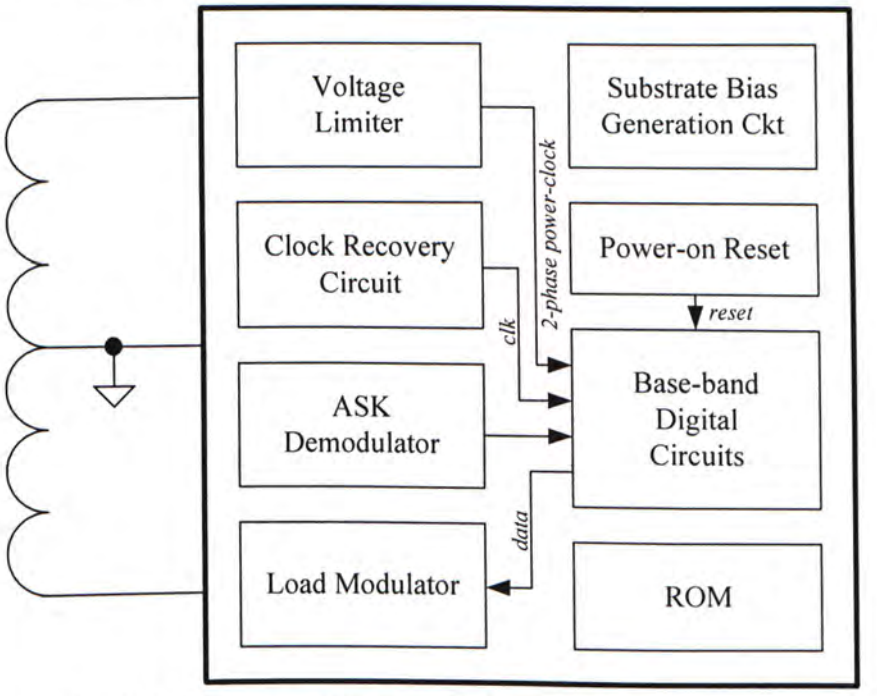


Fig. 4.1 System architecture of the adiabatic smart card

4.2. Circuit Design

The ASK demodulator and clock recovery circuit is discussed briefly in this subsection. The other circuit blocks have been addressed in previous section.

4.2.1. ASK Demodulator

Fig. 4.2 depicts an ASK demodulator circuit that comprises of a full wave rectifier (FWR) envelope detector, a low pass filter, a high pass filter, and a Schmitt trigger. As the FWR is only used for data detection, the transistor size is quite small. The main advantage of using a FWR envelope detector is that the frequency of the RF carrier is doubled, which reduces the value of the capacitor of the low pass filter by half. Conventional design uses a simple RC low pass filter to remove the RF carrier, and the typical size of the capacitor is very large at around 100pF. In this design, we use a peak detector that comprises $MP5$, $MP6$, $R1$, and $C1$ to serve as a low pass filter. This approach can reduce the capacitor value from 100pF to 3pF. The peak detector diode consists of two series connected diodes ($MP5$ and $MP6$), with the extra diode used to reduce the output DC voltage of the detector and reduce the current flow in the resistor $R1$. The peak detector charges the capacitor $C1$ to the peak voltage when the data is high. When the data is low, the diodes turn off and the capacitor $C1$ discharges through the resistor $R1$ in approximately 130 ns, which is approximately equal to two RF cycles. A simulated peak detector output is shown on the second graph in Fig. 4.3. Note that the RF carrier has been removed from the envelope detector circuit. The first graph of Fig. 4.3 is a 7V(pk-pk) ASK signal. A high pass filter comprising $C2$ and $MN2$ is used to level shift the DC output of the peak detector to zero, as shown in the third graph of Fig. 4.3. Note that

the output of the high pass filter requires about 30us to become stable, which is the time required to charge the capacitor $C1$. This time delay has no significant effect on the operation of the smart card. A conventional smart card requires more than 30us to charge up the capacitor of the international regulator. The final stage of the data extraction circuit is a conventional Schmitt trigger with a threshold level of ± 0.3V, which is powered at vp and vn. The simulated output of the Schmitt trigger is shown in the fourth graph of Fig. 4.3. The output signal level is restored to ±2.8V, which is needed to drive the adiabatic circuits. The time constant of the high pass filter and the threshold level of the Schmitt trigger guarantee correct operation from 7V(pk-pk) to 14V(pk-pk) input ASK signal.

Moreover, this circuit provides an alternative solution for the load modulator. In the card-to-reader link, the output data (*data_mod*) drives the transistor $MN1$, which shorts the resistor $R2$ to ground to change the load capacitance and the resonant frequency. The changed resonant frequency is coupled back to the card reader and demodulated to recover the output data.

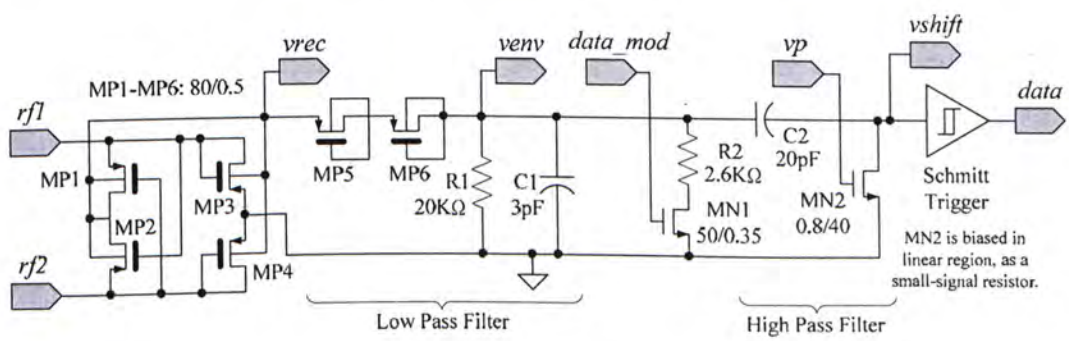


Fig. 4.2 Schematic diagram of the ASK demodulator

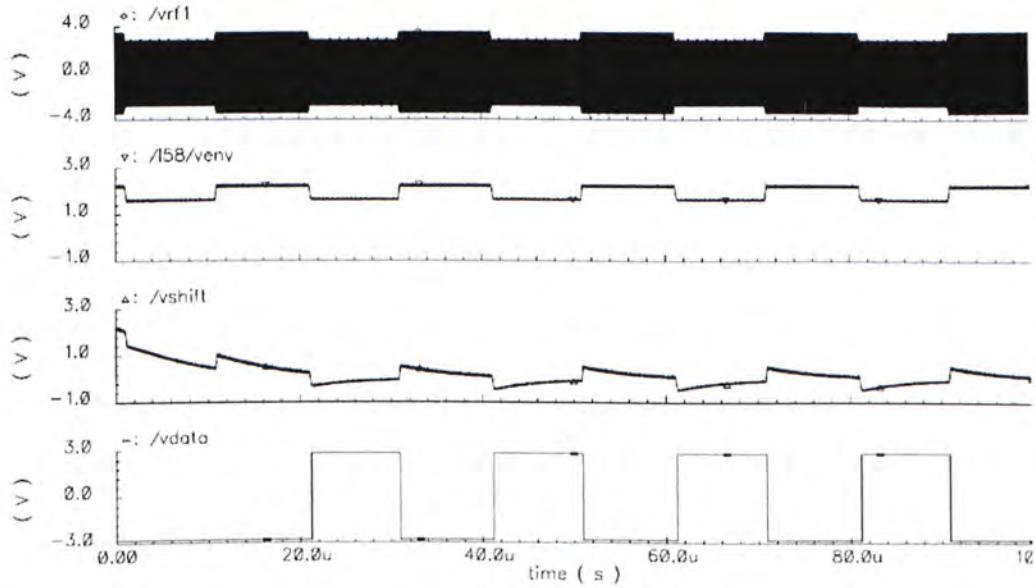


Fig. 4.3 Simulation results of the ASK demodulator with 7V(pk-pk) induced voltage. From top to bottom: the 7Vpk-pk 13.56MHz ASK signal, the peak detector output signal, the DC-shifted envelope signal and the output of Schmitt trigger.

4.2.2. Clock Recovery Circuit

The clock recovery circuit is the most difficult part to design. Conventional architecture uses a very simple clock recovery circuit. The 13.56MHz RF carrier is divided by 128 to recover the 106kHz clock signal. However, we can not use this simple approach for the adiabatic architecture because we use the 13.56MHz carrier as the supply voltage. There is no internal DC supply in the new design, thus, we cannot adopt conventional techniques, such as divider and Phase-Locked Loop (PLL).

A block diagram of the clock recovery circuit is shown in Fig. 4.4. An ASK demodulator retains the 106kbps data from the ASK signal. The 106kbps data is fed into an adiabatic pulse generator that comprises of an adiabatic inverter delay line and an adiabatic exclusive-or gate as illustrated in Fig. 4.5. The pulse generator produces a 106kHz pulse train, synchronous to the input data. The pulse signal is

injected into an adiabatic ring oscillator, which has a free running frequency around 100kHz. The injected signal forces the ring oscillator to oscillate and lock to the frequency and phase of the injected signal [Beg.2003]. So the 106kHz clock for data retiming can be recovered by this injection-locking approach.

A schematic of the ring oscillator used in the clock recovery circuit is shown in Fig. 4.6. We use 81 stages ring oscillator which has a free running frequency of approximately 100kHz. The simulated results of the clock recovery circuit are shown in Fig. 4.7. The top waveform is the 13.56MHz carrier used as the AC supply voltage. The second waveform is the 100kHz free running frequency of the ring oscillator. The third waveform is the 106kHz injected signal and the last waveform is the injection-locked output of the ring oscillator. The injection-locked output is changed from 100kHz to 106kHz.

The injection-locked oscillator operates like a PLL. The oscillator remains in-lock even if the injected signal is missing. The simulation results in Fig. 5.8 illustrate this point. The injected signal is turn off for 8 cycles and the oscillator remains lock. A Type B standard data format is eight bits long with start and stop bit at each end. Fig. 4.8 simulates the worst case condition where the data is either all 0s or 1s.

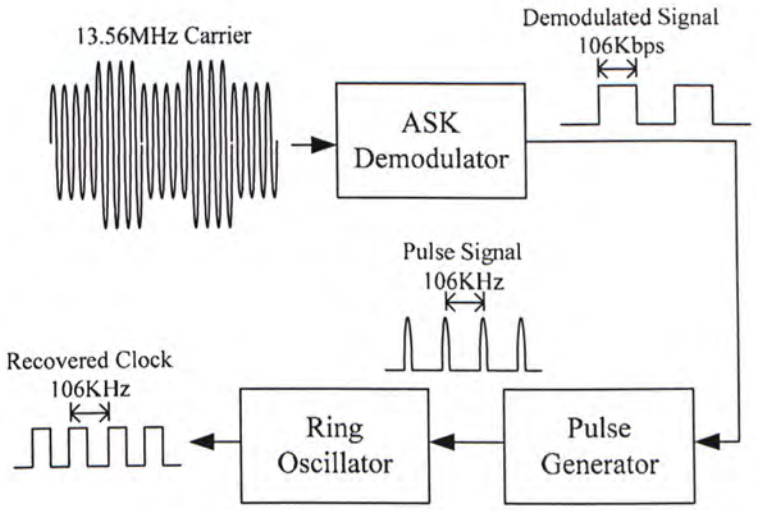


Fig. 4.4 Block diagram of the clock recovery circuit

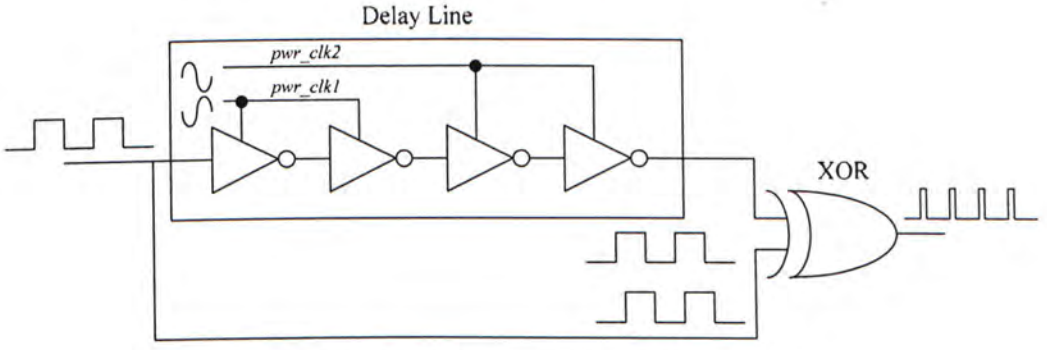


Fig. 4.5 Block diagram of the pulse generator

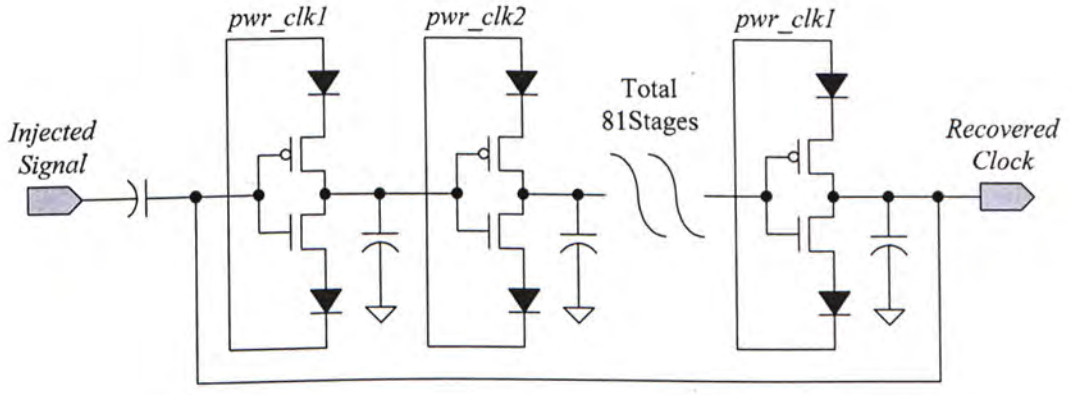


Fig. 4.6 Schematic diagram of the adiabatic ring oscillator used in the clock recovery circuit

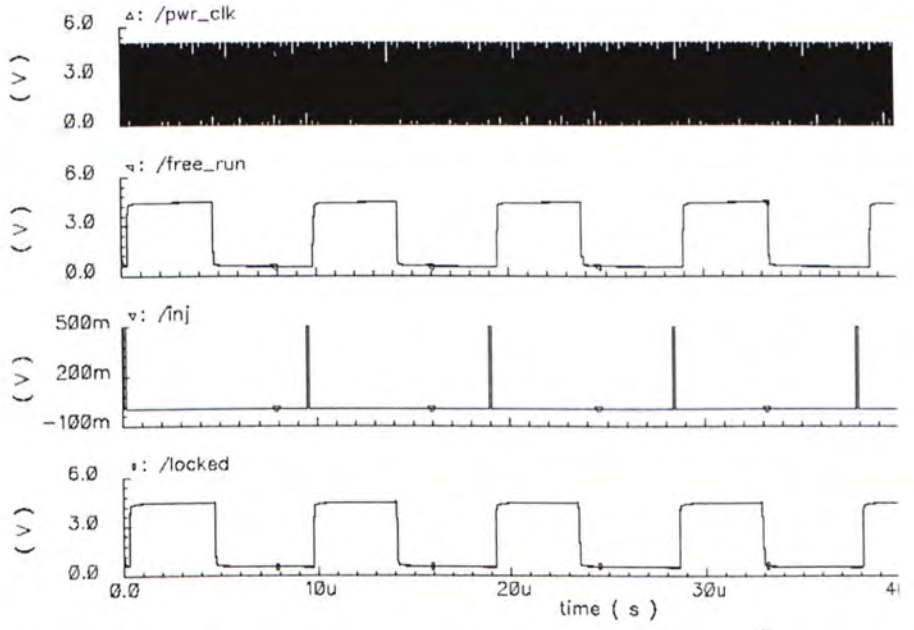


Fig. 4.7 Simulated results of the adiabatic injection-locked oscillator. From top to bottom: the 13.56MHz RF carrier supply, the free-running oscillator output signal, the 106kHz injected pulse signal and the 106kHz recovered clock signal.

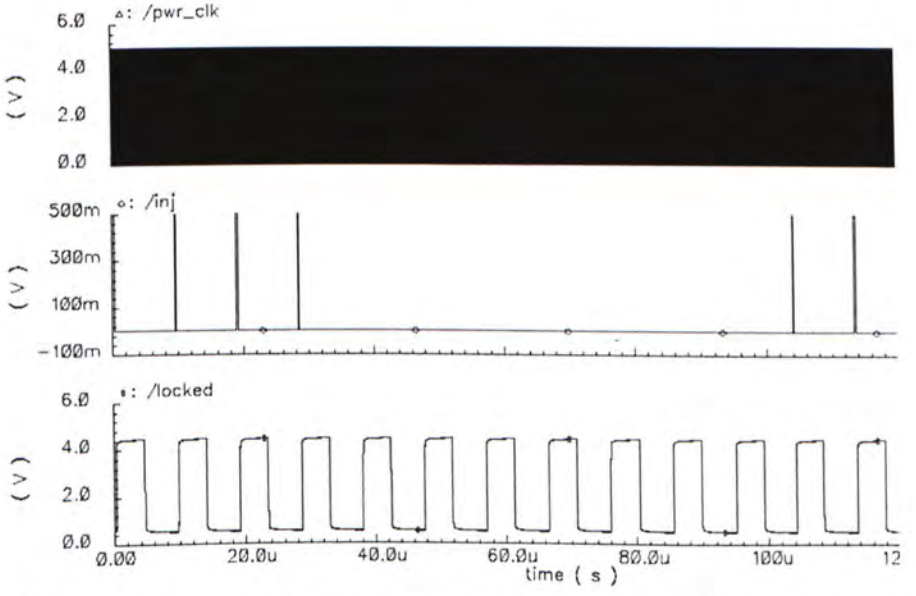


Fig. 4.8 Simulated results of the adiabatic injection-locked oscillator, where the 8-bit packet contains all 0s. Top: the injected pulse signal, Bottom: the recovered clock signal

4.3. Experimental Results

A test chip of an adiabatic smart card receiver front-end circuit is designed and fabricated with *Austriamicrosystems* 0.35 micron standard CMOS process. Similar to the adiabatic RFID tag, thick gate transistors are employed in this design. Fig. 4.9 is a micrograph of the test chip. Each circuit block is illustrated on the micrograph. The other unspecified circuits are the test structures of diodes, voltage limiter, etc. The test chip is housed in a PGA64 package and a PCB test board is developed for measurements. Fig. 4.10 shows the PCB test board.

The functionalities of the receiver front-end circuit is verified in a conductive test setup. An arbitrary signal generator is employed to generate the required ASK-encoded 13.56MHz RF signal with controllable voltage amplitude as the input to the test circuit. An oscilloscope is used to measure the outputs. Furthermore, DC power supplies are required for the DC substrate biases of the test chip and the DC-powered output buffers. Because the outputs of the internal circuit cannot drive the high capacitive loading of the probe, we have placed additional output buffers at the tests nodes. The instruments used in the setup are listed in Table 4.1.

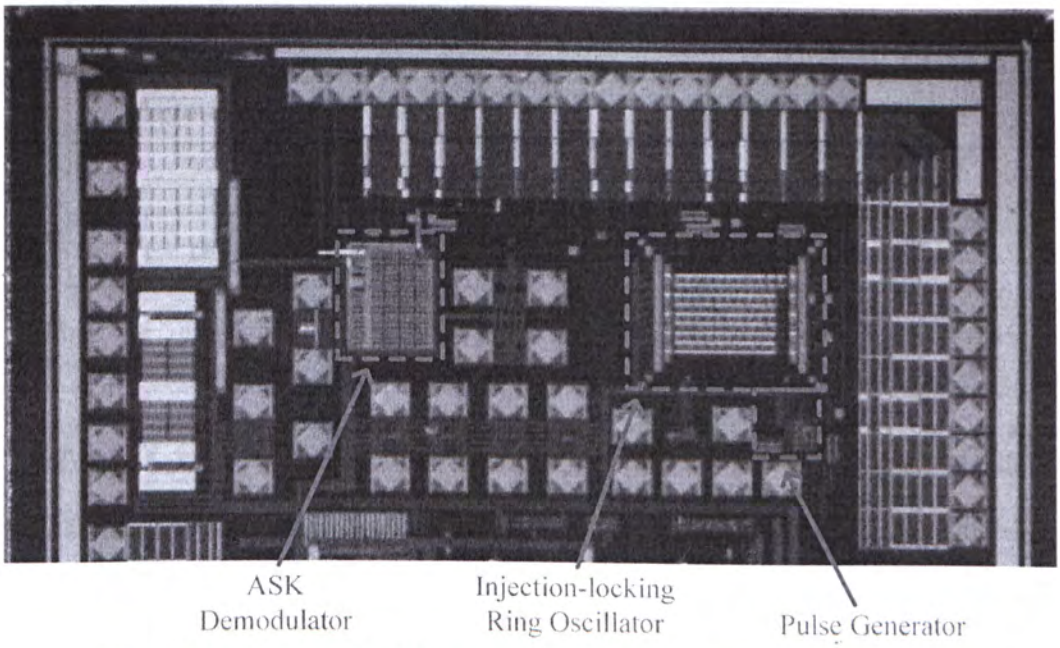


Fig. 4.9 Micrograph of the test chip of the adiabatic smart card receiver front-end circuits

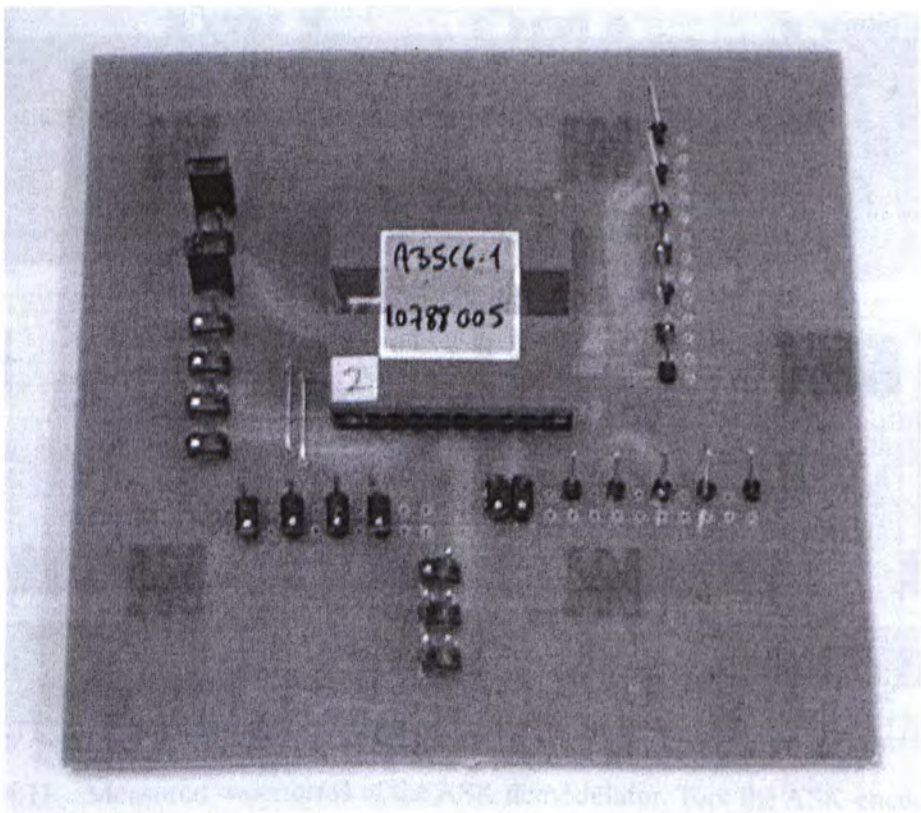


Fig. 4.10 PCB test board of the adiabatic smart card receiver front-end circuits

Instrument	Model
Arbitrary Signal Generator	LeCroy LW420A
Oscilloscope	LeCroy WaveRunner 6100
DC Power Supply	HP E3611A

Table. 4.1 Instruments used in the measurement setup of the adiabatic smart card receiver front-end circuits

An ASK-encoded RF signal is fed to the test circuit and the demodulated data is available at the output, as shown in Fig. 4.11. The encoded data is a bit pattern of '1011-1101-0000-0000'. The result shows that the demodulator is able to treat with common dataset and even the null packet containing all bits of '0'.

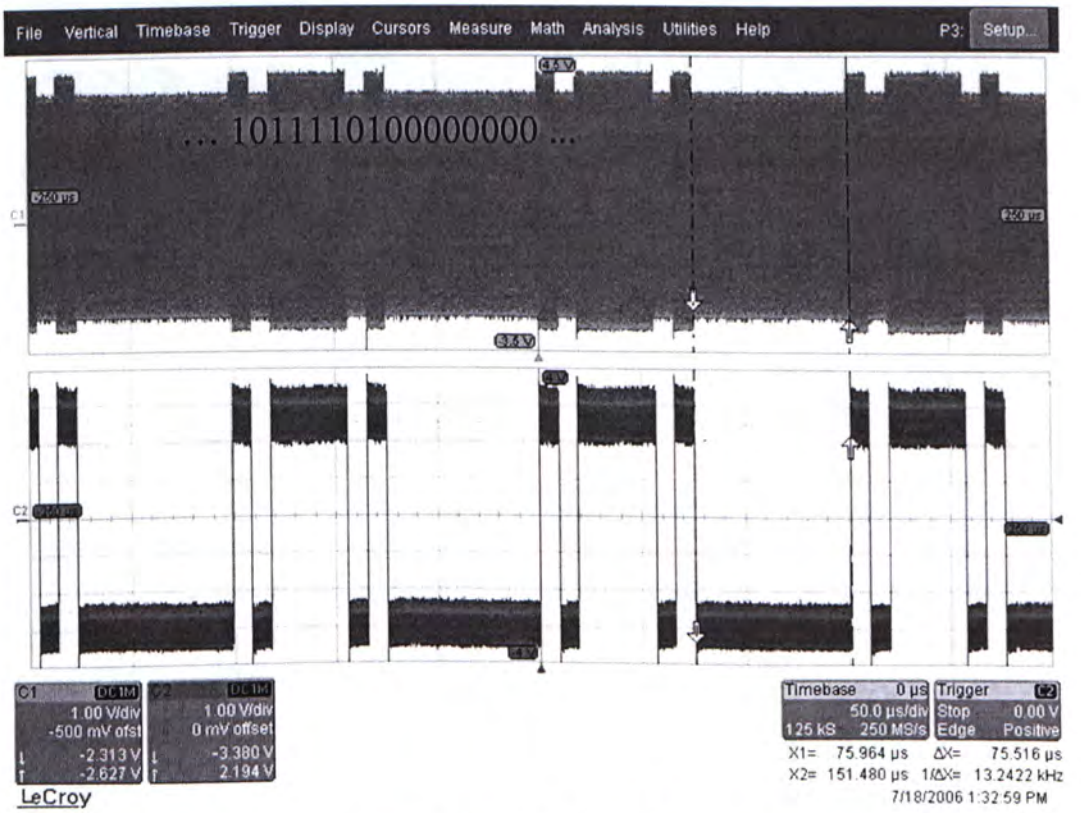


Fig. 4.11 Measured waveforms of the ASK demodulator. Top: the ASK-encoded RF signal, Bottom: the demodulated output

The integrated load modulator mentioned in Section 4.2.1 is verified with the same coupling measurement method for the adiabatic RFID tag. By probing the RF voltage induced at a test antenna coil in proximity, the encoded data from the load modulator can be seen in the form of an ASK modulated signal. Fig 4.12 shows the measured waveforms of the ASK modulated RF carrier coupled at a test antenna coil. The overlay capture shows the zoom-in of the ASK signal on the RF carrier, which the underlay shows a full amplitude RF carrier. There is a modulation depth of 50mV in a 9V(pk-pk) RF signal. The modulation depth can be scaled by the value of the resistor $R2$ in Fig. 4.2.

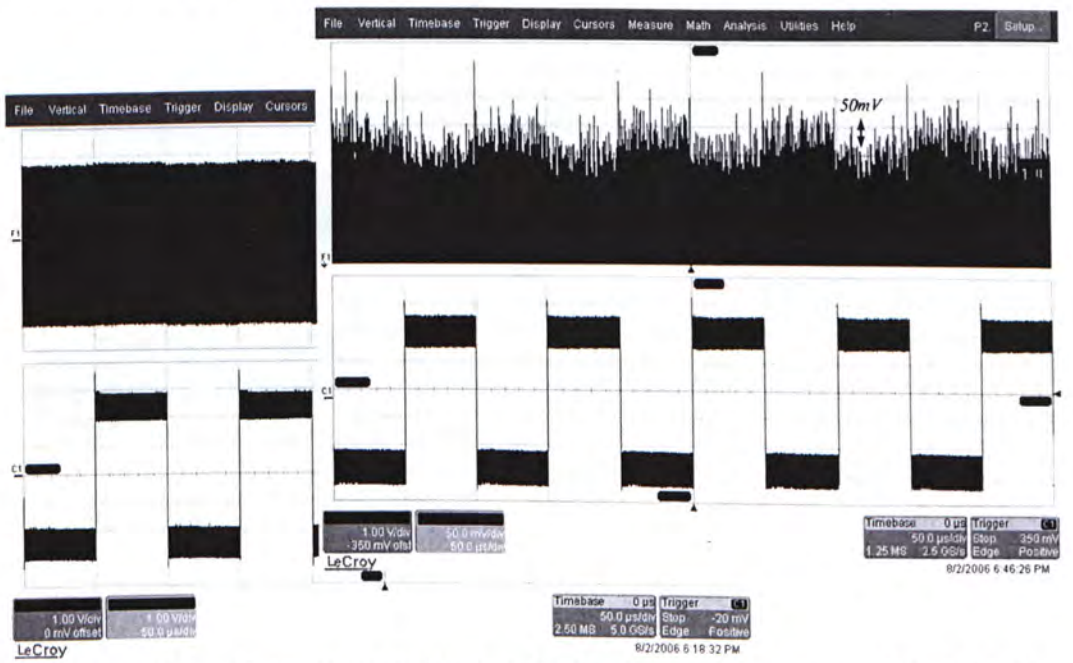


Fig. 4.12 Measured waveforms of the load modulator integrated in the ASK demodulator. Top: the RF carrier and Bottom: the input data of the load modulator, in both captures. The overlay capture shows the zoom-in view of the ASK signal on the RF carrier.

For the injection-locked clock recovery circuit, the pulse generator is examined first. Fig 4.13 shows the measured waveforms of the pulse generator. The demodulated data from the ASK demodulator is fed into the generator. The generator produces an output of pulses at each logic transitions of the input data. The generated output is for injection-locked to the demodulated ASK signal. Fig 4.14 shows the measured waveforms of the injection-locked ring oscillator. In case of a null packet containing 8 successive bits of '0', the ring oscillator still can produce a synchronous clock in the interval of missing pulses and keep in-lock again once the pulse signal reappears. This proves that the clock recovery circuit is able to generate a synchronous clock signal for data retiming.

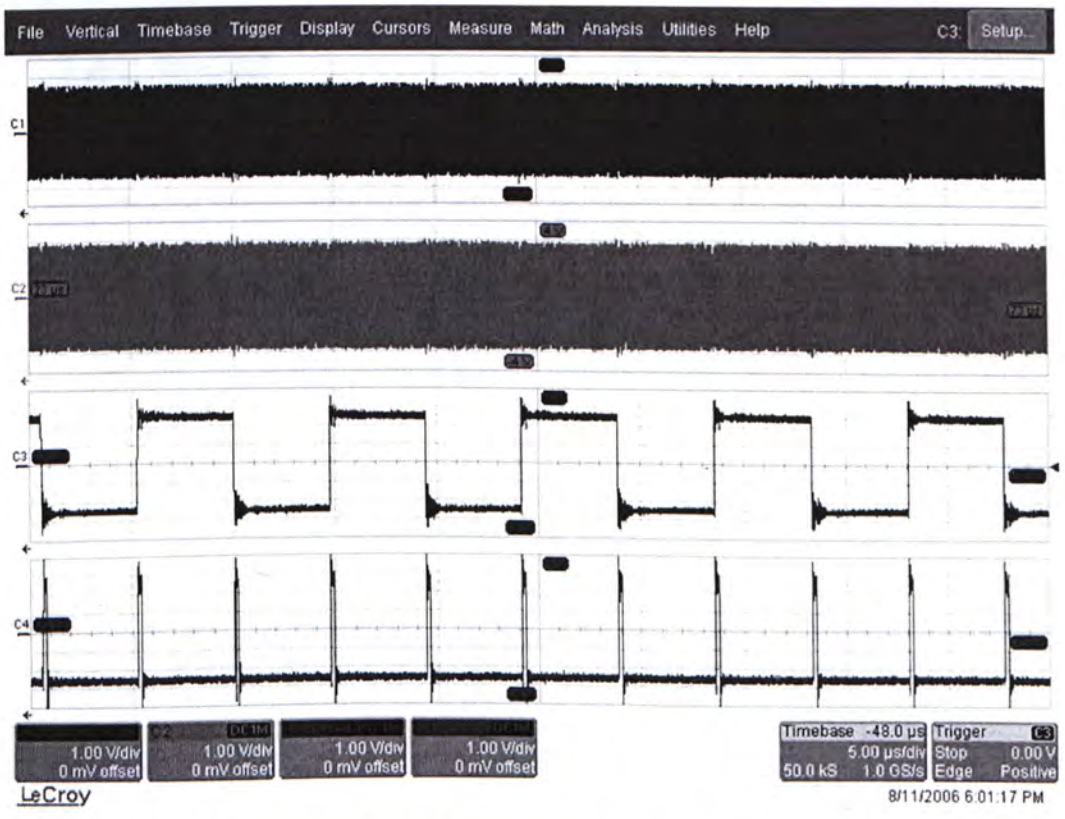


Fig. 4.13 Measured waveforms of the pulse generator used in the clock recovery circuit. From top to bottom: the in-phase power-clock, the out-phase power-clock, the input data and the pulse signal generated.

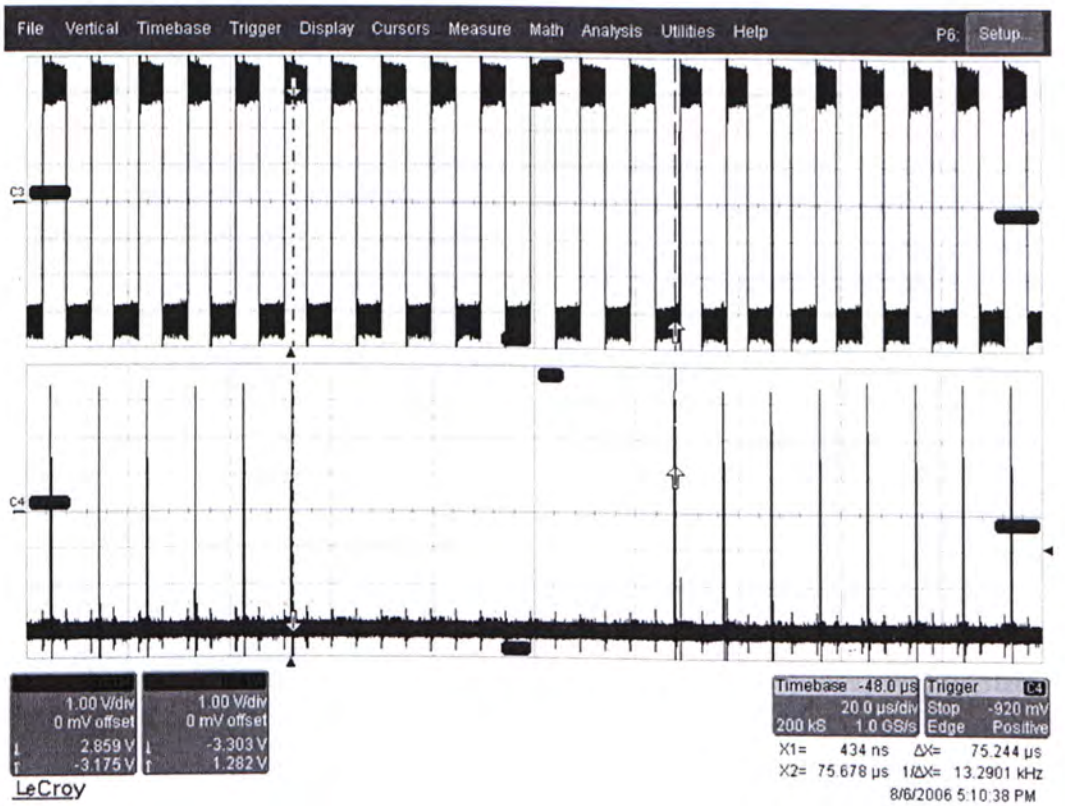


Fig. 4.14 Measured waveforms of the injection-locked ring oscillator, in case of a null packet containing all 0s. From top to bottom: the output clock signal of the oscillator, the injected pulse signal.

The internal adiabatic circuits consume very little power which cannot be measured by our instrument because of limited resolution. We can only present the simulated power consumption. Table 4.2 lists the chip area and the simulated power consumption of the major circuit blocks.

Circuit Block	**Chip Area**	**Simulated Power Consumption**
ASK Demodulator	230um x 280um	370uW
Ring Oscillator	480um x 390um	24.1uW
Pulse Generator	65um x 90um	0.62uW

Table. 4.2 Chip are and power consumption of the adiabatic smart card receiver front-end circuits

5. Conclusion

In this work, the following circuit design techniques are newly developed for the adiabatic smart card / RFID applications.

1. Tri-state inverter type flip-flop based on AQS-CMOS logic, with a specific clocking scheme
2. True Single Phase Clock (TSPC) flip-flop based on AQS-CMOS logic
3. A fixed-frequency ring oscillator that makes use of the delay characteristic of cascaded AQS-CMOS gates powered by the same power-clock
4. A dynamic NOR-based ROM based on AQS-CMOS logic

A Read-only RFID tag based on AQS-CMOS logic is developed. The AC-powering feature of adiabatic logic leads to a unique smart card /RFID architecture, resulting in small chip size and low power consumption. A 64-bits RFID tag test chip has been fabricated in a 0.35 micron CMOS process and a functional measurement is conducted. It demonstrates the technical feasibility of such RFID tag design based on adiabatic logic. Our developed RFID tag is only 0.23 mm-square in size, just equal to the size of the analog circuits in existing commercial products. For example, Philips I-CODE 512-bits RFID tag [ICODE] has a chip size of 0.45 mm-square (740 um x 620um in dimension) and the analog circuits including the full wave rectifier, regulator and bandgap reference already occupy half of the chip area.

Based on the same architecture, an adiabatic smart card supporting half-duplex communication is introduced. A test chip of the receiver front-end circuits, including the ASK demodulator and the clock recovery circuit, is designed and fabricated in the same CMOS process. The results show that an adiabatic smart card can be realized with the additional receiver front-end circuits.

Two international conference papers on the developed adiabatic smart card / RFID have been published, listed below.

1. "Adiabatic Smart Card" in the 2006 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2006)
2. "A 13.56 MHz Adiabatic Smart Card / RFID" in the 7-th International Conference on ASIC (ASICON 2007)

6. Future Works

Another interesting perspective is to investigate the development of adiabatic RFID tag using organic transistor technology [Paul2003, Ryo2004]. As the electrical characteristics of organic transistor are poor compared with conventional silicon devices, high performance analog circuits cannot be implemented. As a result, only simple digital circuits can be implemented with organic transistors. The adiabatic RFID presented here, possessing simpler architecture and circuitry, seems to be a good approach to develop the RFID tag using organic transistors.

Reference

[Alioto2000] Massimo Alioto, Gaetano Palumbo, "Performance Evaluation of Adiabatic Gates", IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, Vol. 47, No. 9, September 2000

[Beg.2003] J-B. Begueret, Y. Deval, C. Scarabello, J-Y. Le Gall, M. Pignol, "An innovative open-loop CDR based on injection-locked oscillator for high-speed data link applications", 2003 IEEE Radio Frequency Integrated Circuits Symposium, Page(s):313 – 316, 8-10 June 2003

[Can.2006] E. Cantatore, T. C. T. Geuns, A. F. A Gruijthuijsen, G. H. Gelinck, "A 13.56MHz RFID System based on Organic Transponders", 2006 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Page(s):1042 - 1051, Feb. 6-9 2006.

[Chan1997] C. F. Chan, K. W. Cheng, and C. S. Choy, "An Adiabatic Quasi-static CMOS Circuit", 5th International Conference on VLSI & CAD, pp.334-337, Korea, October 1997.

[ICODE] NXP I-CODE Label IC, http://www.nxp.com/acrobat_download/other/identification/SL064230.pdf

[ISO14443] ISO/IEC 14443-2 (Final Committee Draft), Identification cards – Contactless integrated circuit(s) cards – Proximity cards, Part 2: Radio frequency power and signal interface

[Kang2003] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", McGraw Hill, 2003, Chapter 11.2.

[Mak2000] W.S. Mak, C.F. Chan, K.W. Cheung and C.S. Choy, "An 8x8 Adiabatic Quasi-Static CMOS Multiplier", IEEE International Symposium on Circuits and Systems, Volume 5, Page(s):553 - 556, May 28-31 2000.

[Mok2006] King-Keung Mok, Ka-Hung Tsang, Cheong-Fat Chan, Chiu-Sing Choy, Kong-Pang Pun, "Adiabatic Smart Card", IEEE Asia Pacific Conference on Circuits and Systems, Page(s):287 – 290, Dec 4-7, 2006.

[Mor.1990] Morteza Afghahi, Christer Svensson, "A Unified Single-phase Clocking Scheme for VLSI Systems", IEEE Journal of Solid-State Circuits, Volume 25, Page(s):225 – 233, 1 February 1990.

[Paul2003] Paul F. Baude, David A. Ender, Tommie W. Kelley, Michael A. Haase, Dawn V. Muyres, and Steven D. Theiss, "Organic semiconductor RFID transponders", IEEE International Electron Devices Meeting 2003, Technical Digest, Page(s):8.1.1 - 8.1.4, 8-10 Dec. 2003.

[Ryo2004] Ryo IMURA, "The World's Smallest RFID u-Chip, bringing about new business and lifestyles", Symposium on VLSI Circuits 2004, Digest of Technical Papers, Page(s):120 - 123, 17-19 June 2004.

[Voj.1997] Vojin G. Oklobdzija, Dragan Maksimovic, Fengcheng Lin, "Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply", IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 44, No. 10, October 1997.

[Wil.1994] William C. Athas, Lars "J." Svensson, Jeffrey G. Koller, Nestoras Tzartzanis, Eric Ying-Chin Chou, "Low-Power Digital Systems Based on Adiabatic-Switching Principles", IEEE Transactions on Very Large

Scale Integration (VLSI) Systems, Volume 2, Issue 4, Page(s):398 – 407, Dec. 1994.

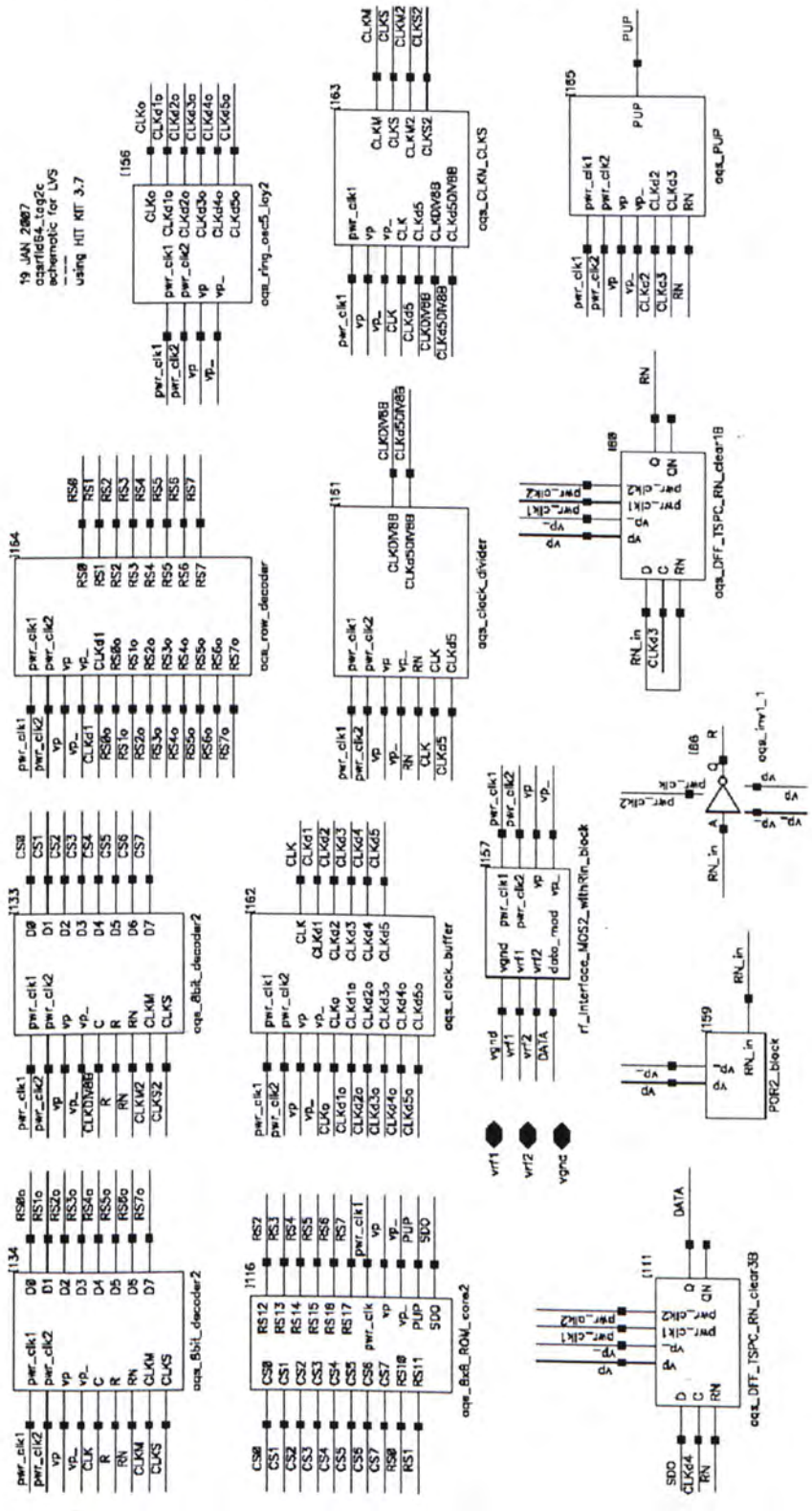
[Wil.2000] William Athas, Nestoras Tzartzanis, Weihua Mao, Lena Peterson, Rajat Lal, Kisup Chong, Joong-Seok Moon, Lars Svensson, Michael Bolotski, "The Design and Implementation of a Low-Power Clock-Powered Microprocessor", IEEE Journal of Solid-State Circuits, Vol. 35, No.11, November 2000.

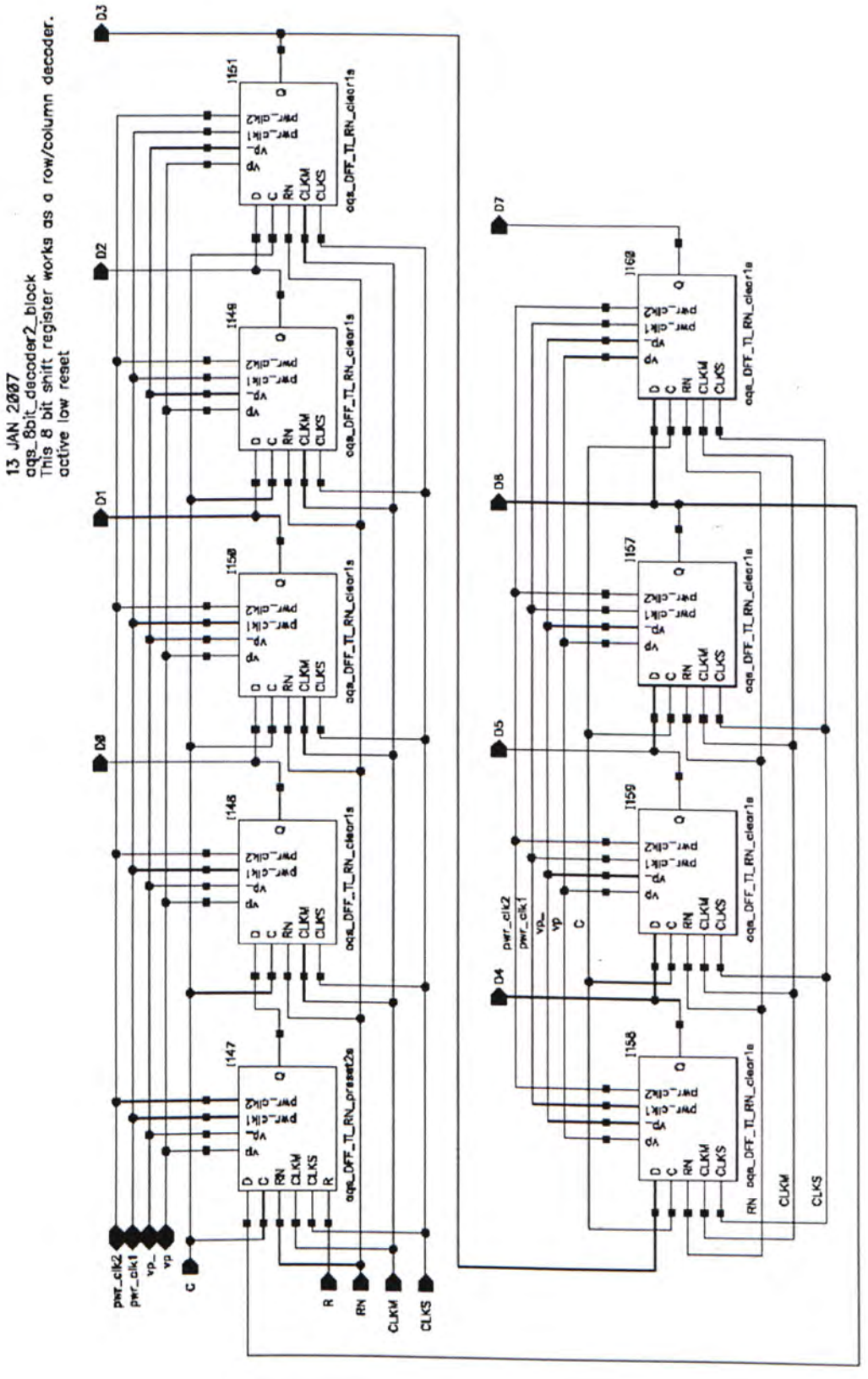
[WKY2003] W.K. Yeung, Cheong-Fat Chan, Chiu-Sing Choy, Kong-Pang Pun, "Clock Recovery Circuit with Adiabatic Technology (Quasi-Static CMOS Logic)", IEEE International Symposium on Circuits and Systems, Volume 2, Page(s):185 - 187, 25-28 May 2003.

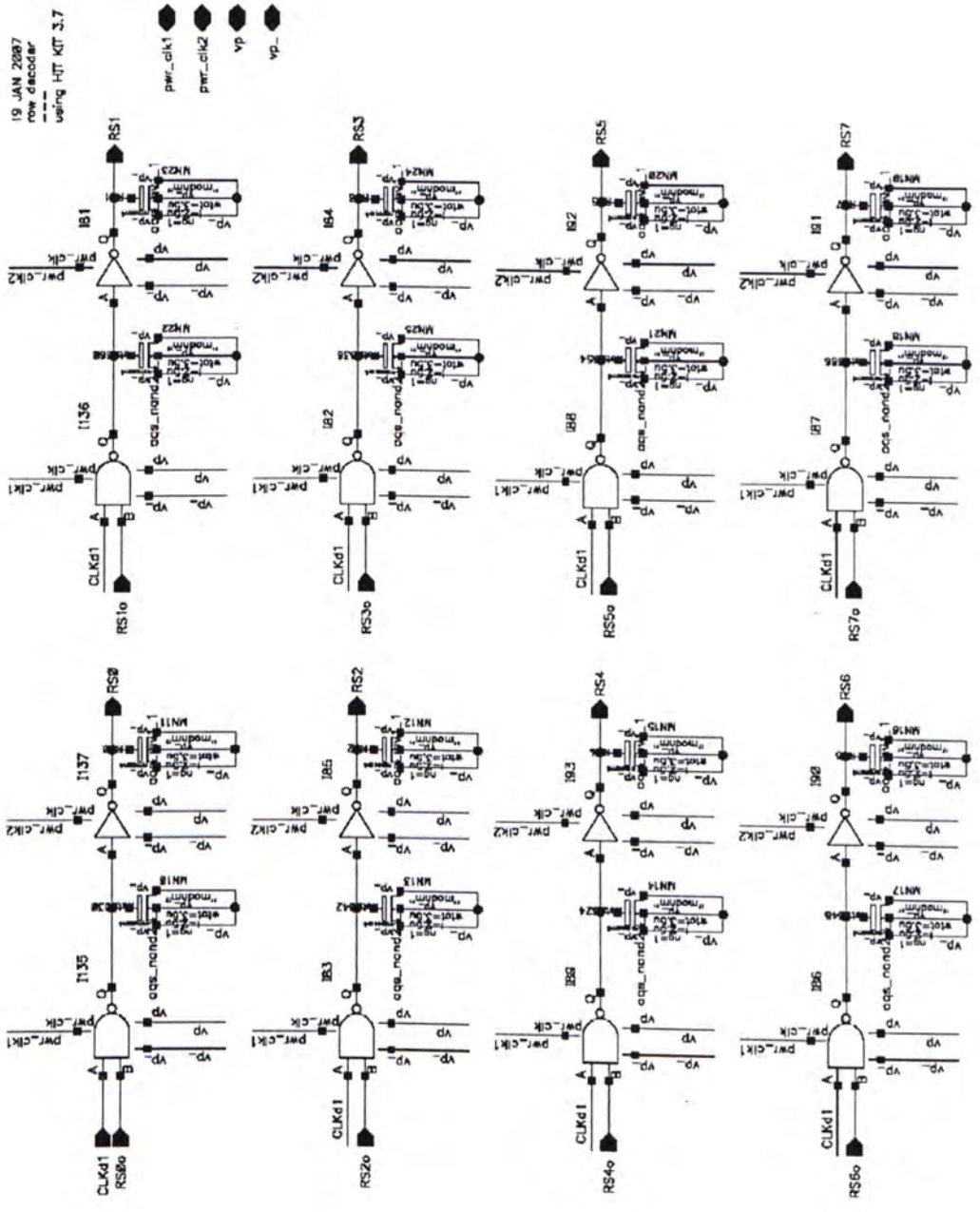
[Yong1996] Yong Moon, Deog-Kyoon Jeong, "An efficient charge recovery logic circuit", IEEE Journal of Solid-State Circuits, Vol. 31, No.4, April 1996.

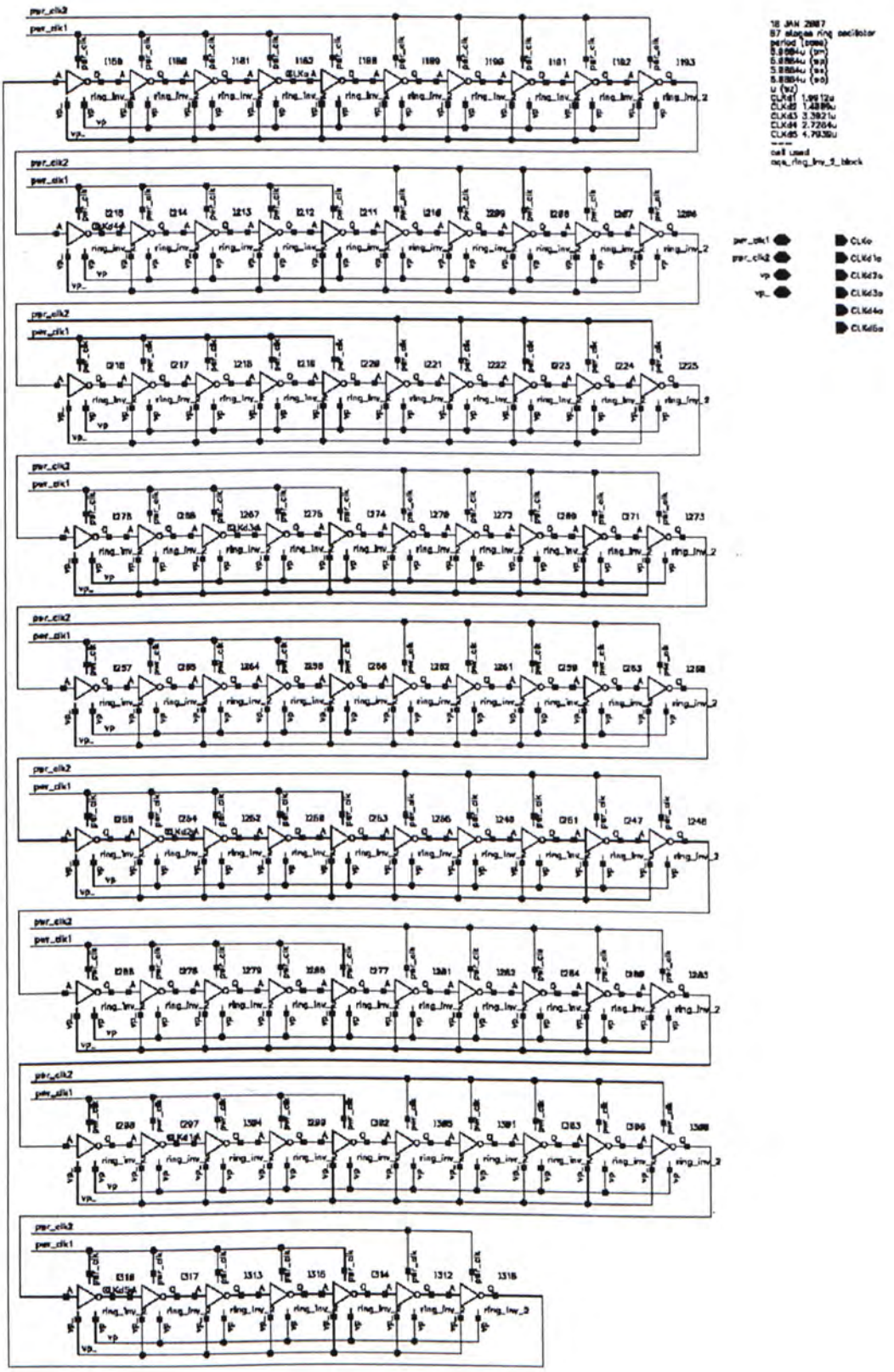
Appendix

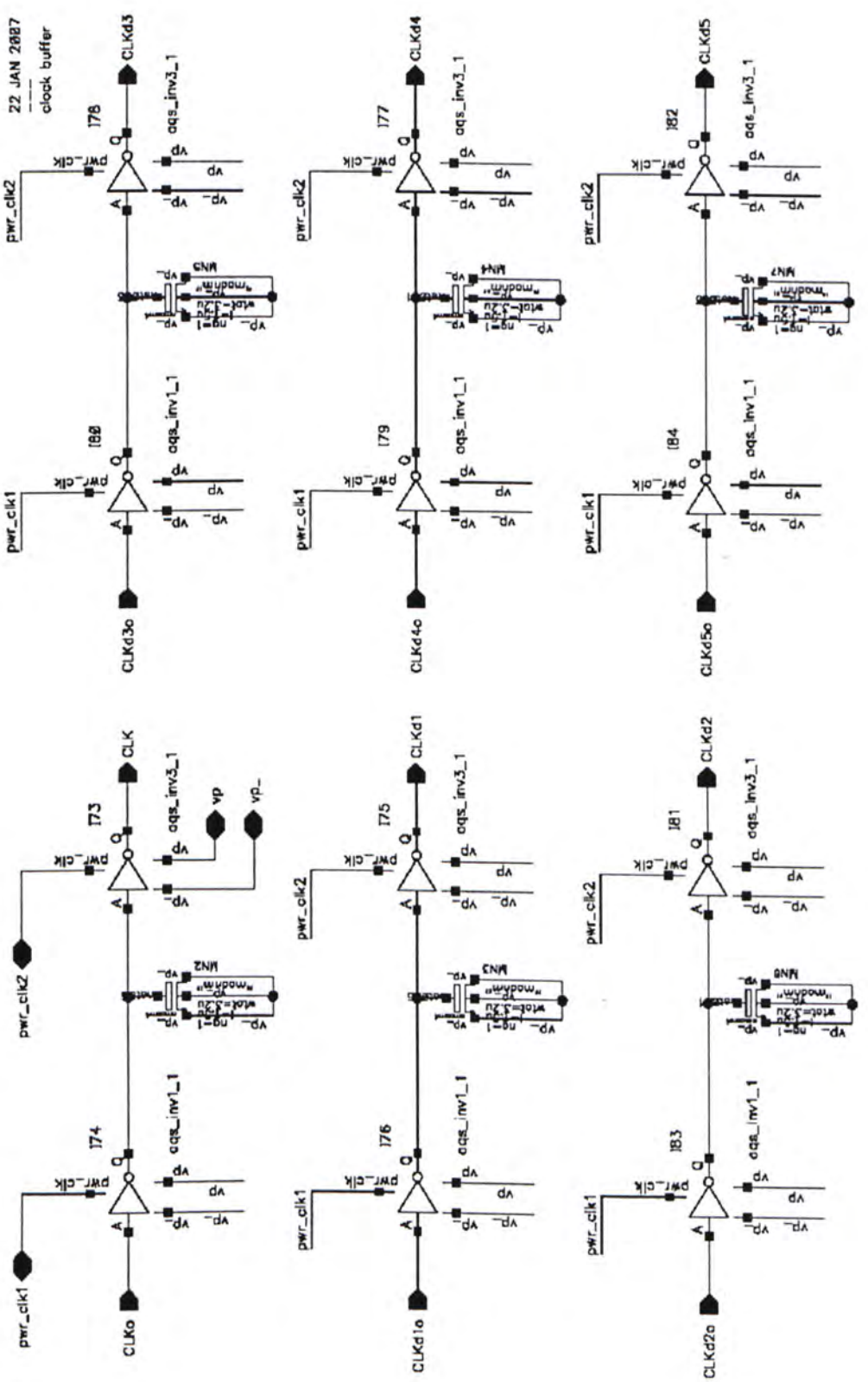
Schematic diagrams of the 64-bits adiabatic RFID tag.

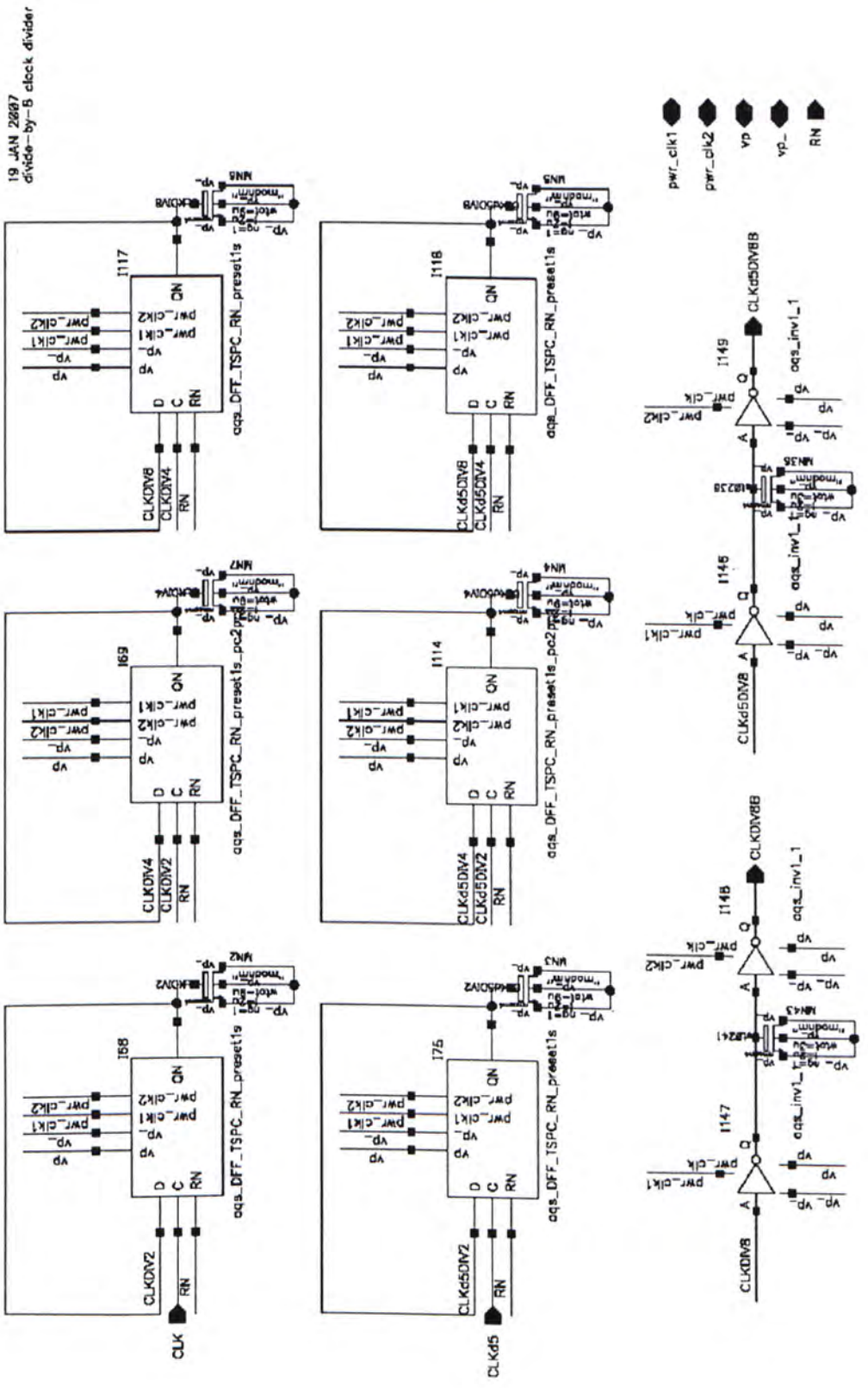


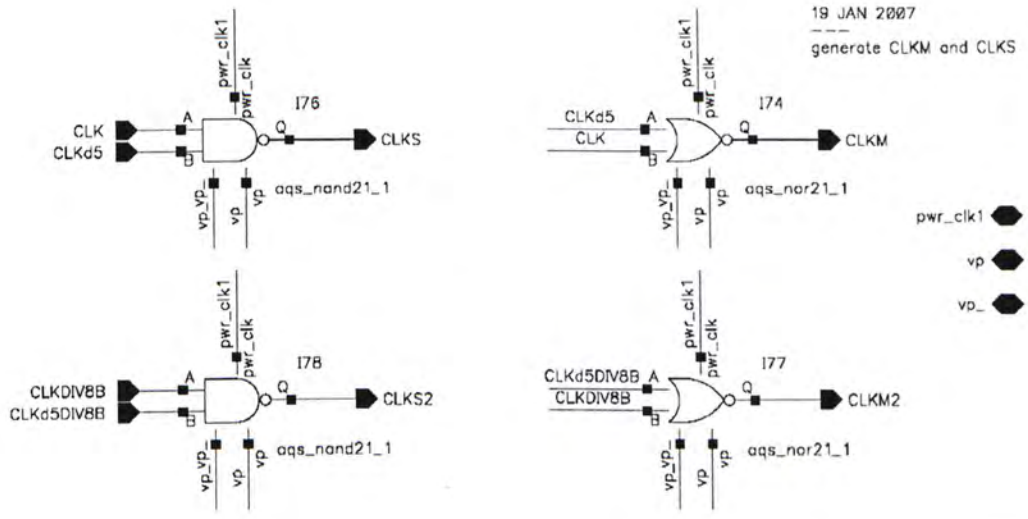

13 JAN 2007
aqs_8bit_decoder2_block
This 8 bit shift register works as a row/column decoder.
active low reset
D3
D2
D1
D0
D7
D6
D5
D4
I151
I149
I150
I148
I147
I152
I157
I159
I158
aqa_DFF_TI_RN_clear1a
aqa_DFF_TI_RN_preset2a
pwr_clk2
pwr_clk1
vp_
vp
C
R
RN
CLKM
CLKS

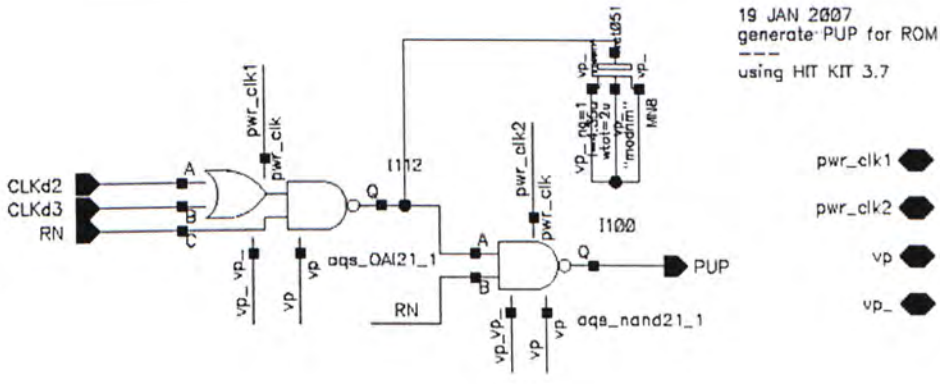

19 JAN 2007
row decoder
using HIT KIT 3.7
pwr_clk1
pwr_clk2
vp
vp_
RS1
RS3
RS5
RS7
RS8
RS2
RS4
RS6
CLKd1
RS1o
RS3o
RS5o
RS7o
RS8o
RS2o
RS4o
RS6o

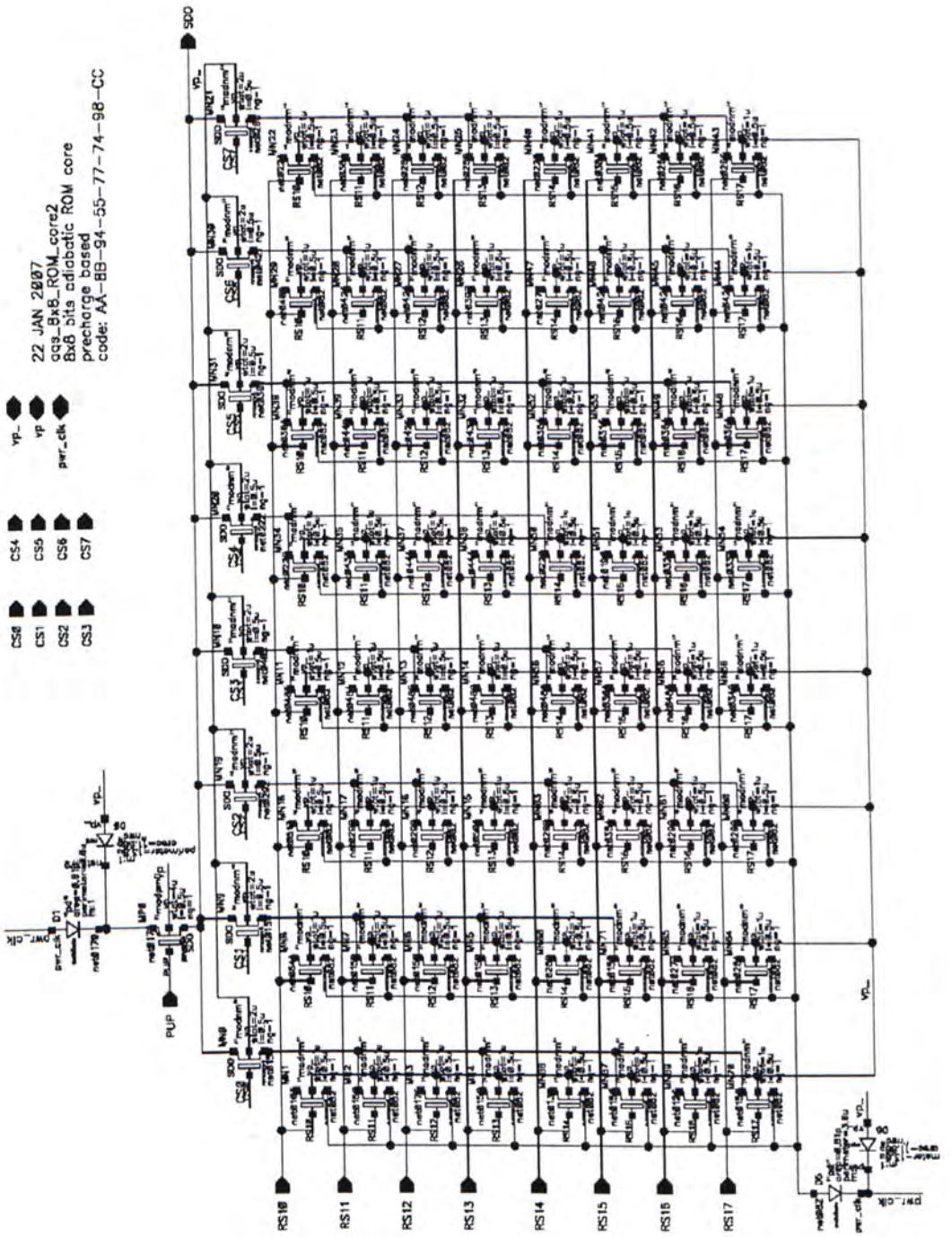


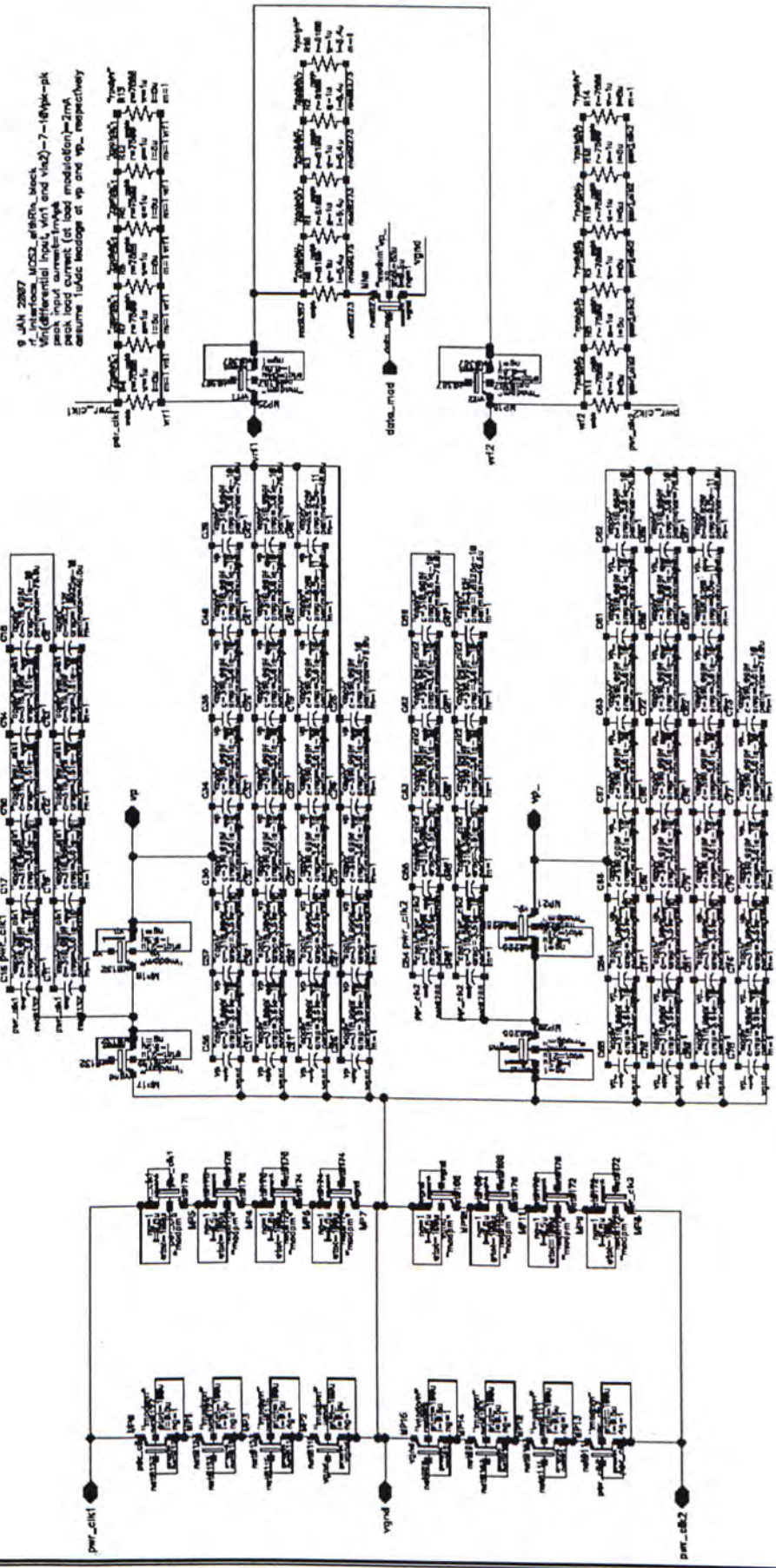

22 JAN 2007
clock buffer
pwr_clk2
pwr_clk1
I78
I88
I77
I79
I82
I84
I73
I74
I75
I76
I81
I83
aqs_inv3_1
aqs_inv1_1
CLKd3
CLKd3o
CLKd4
CLKd4o
CLKd5
CLKd5o
CLK
CLKo
CLKd1
CLKd1o
CLKd2
CLKd2o
vp
vp_

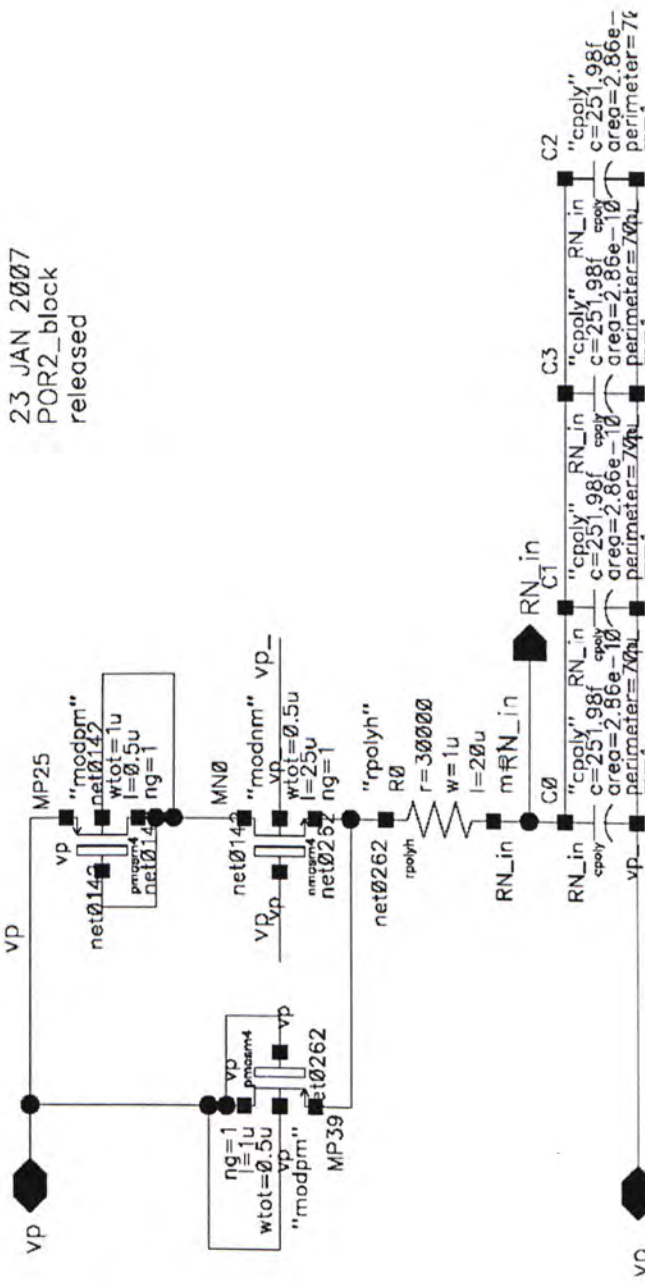

19 JAN 2007
divide-by-5 clock divider
pwr_clk1
pwr_clk2
vp
vp_
RN
aqs_DFF_TSPC_RN_preset1s
aqs_DFF_TSPC_RN_preset1s_pc2
aqs_inv1_1
CLKDIV8
CLKDIV4
CLKDIV2
CLK
CLKd5DIV8
CLKd5DIV4
CLKd5DIV2
CLKd5
I117
I118
I69
I114
I68
I75
I149
I146
I148
I147
MN8
MN5
MN7
MN4
MN2
MN3
MN38
MN43

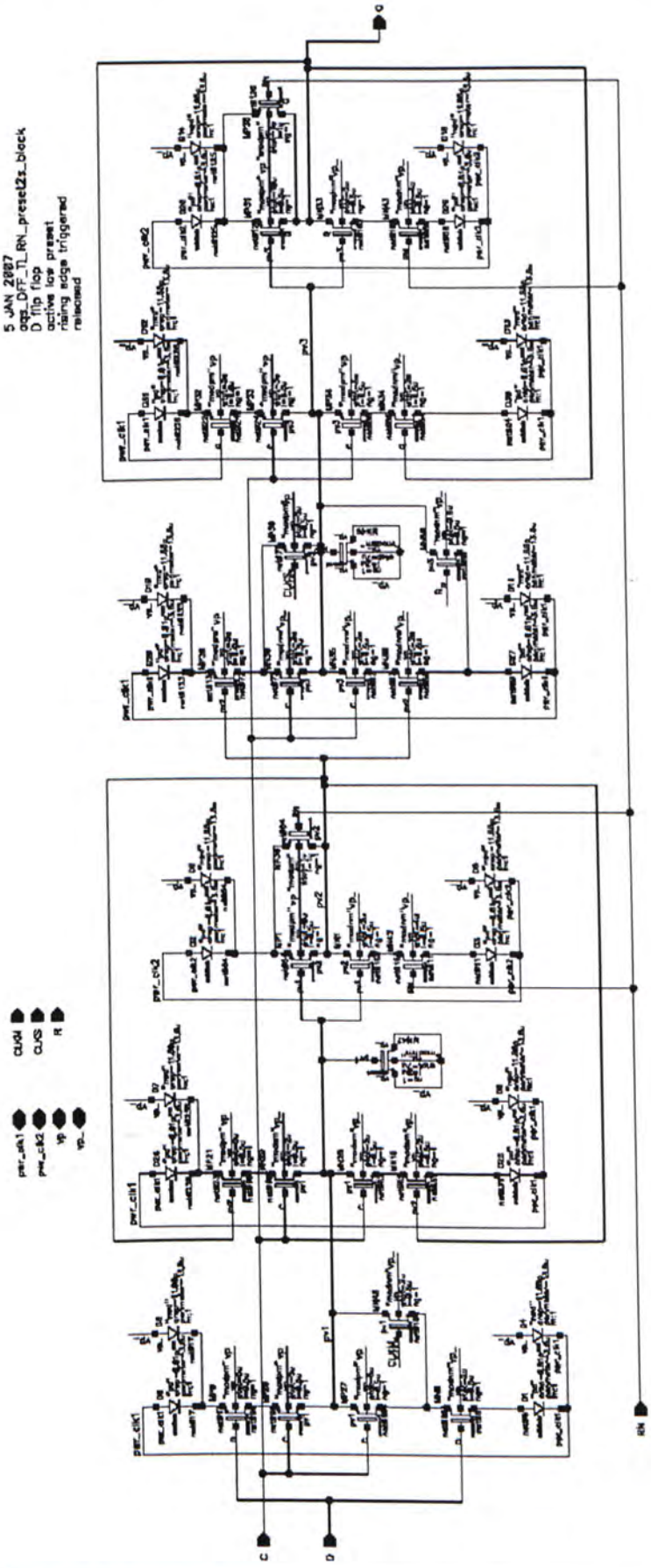

19 JAN 2007
generate CLKM and CLKS
I76
CLK
CLKd5
CLKS
aqs_nand21_1
I74
CLKd5
CLK
CLKM
aqs_nor21_1
I78
CLKDIV8B
CLKd5DIV8B
CLKS2
aqs_nand21_1
I77
CLKd5DIV8B
CLKDIV8B
CLKM2
aqs_nor21_1
pwr_clk1
vp
vp_

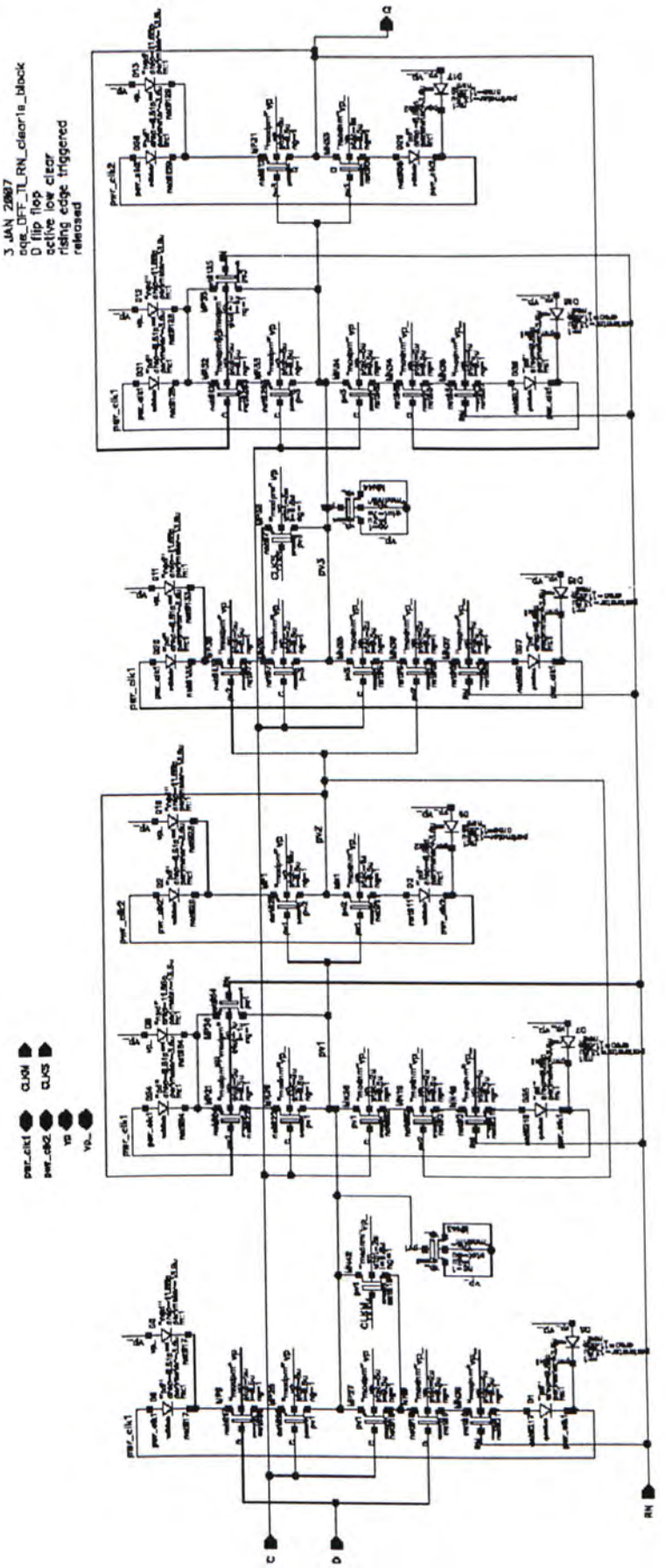

19 JAN 2007
generate PUP for ROM
using HIT KIT 3.7
I112
I100
CLKd2
CLKd3
RN
aqs_OAI21_1
aqs_nand21_1
PUP
pwr_clk1
pwr_clk2
vp
vp_

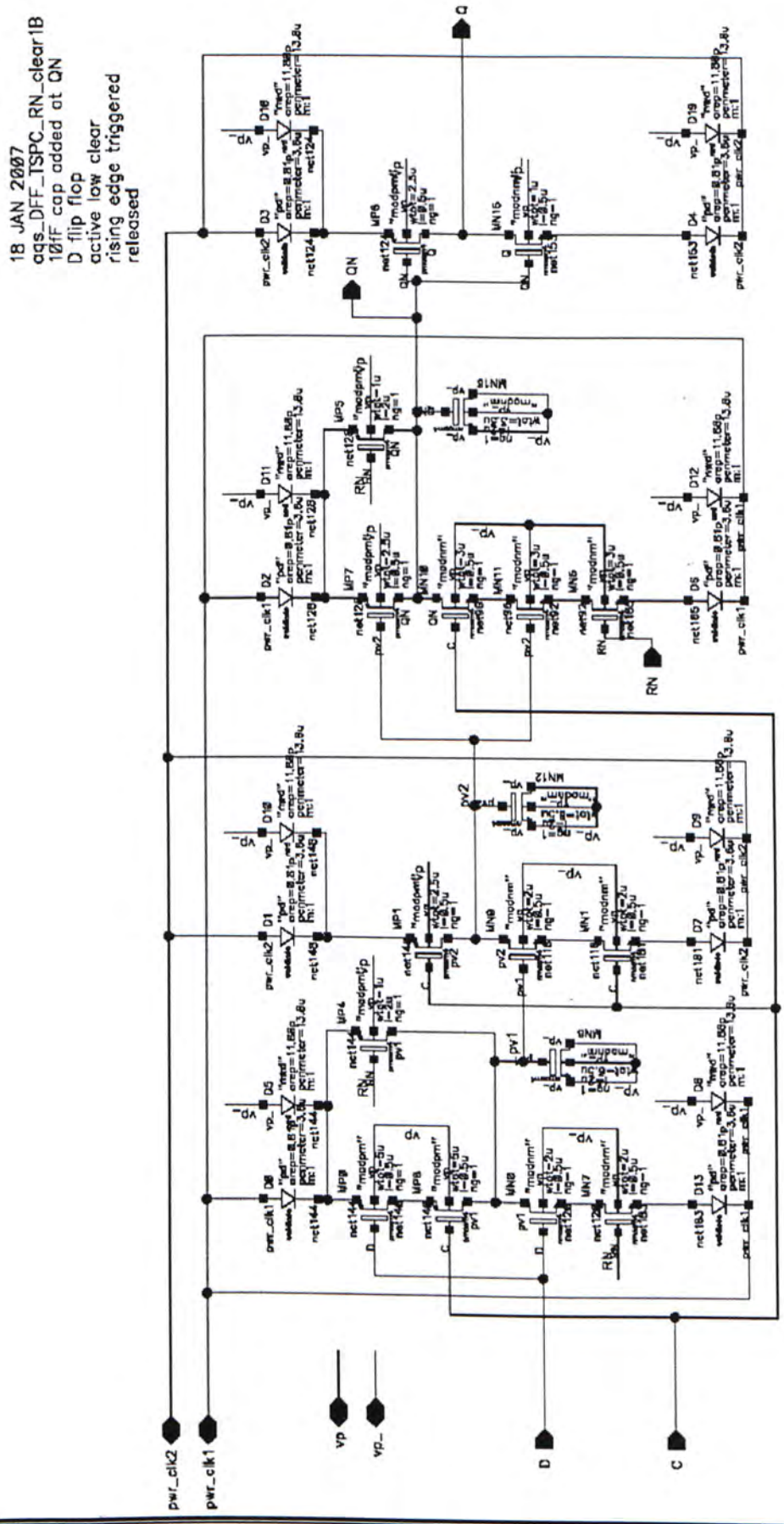

22 JAN 2007
aqs_8x8_ROM_core2
8x8 bits adiabatic ROM core
precharge based
code: AA-BB-94-55-77-74-98-CC
VP_
VP
pwr_clk
CS4
CS5
CS6
CS7
CS0
CS1
CS2
CS3
SDD
PUP
RS10
RS11
RS12
RS13
RS14
RS15
RS16
RS17

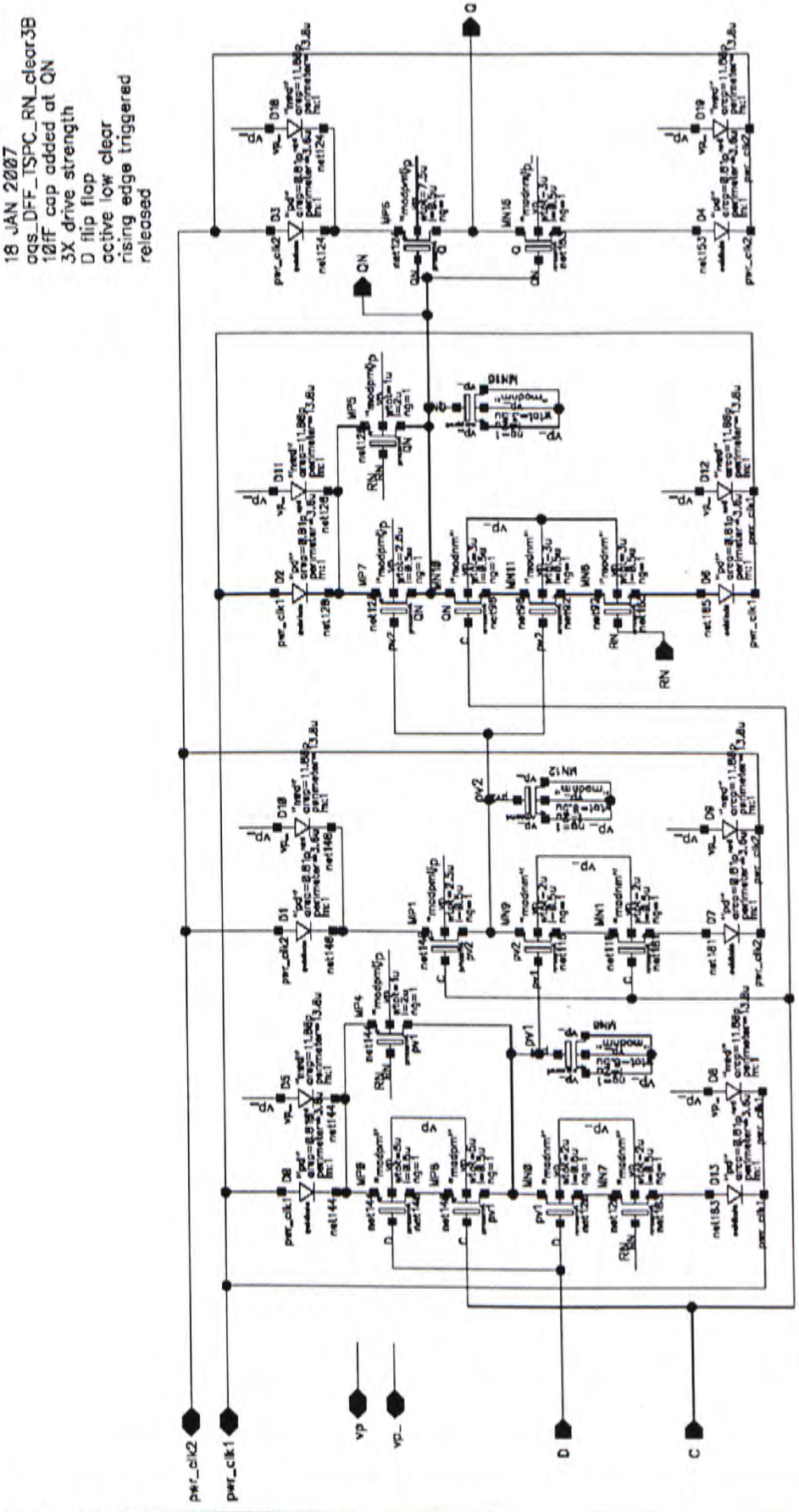


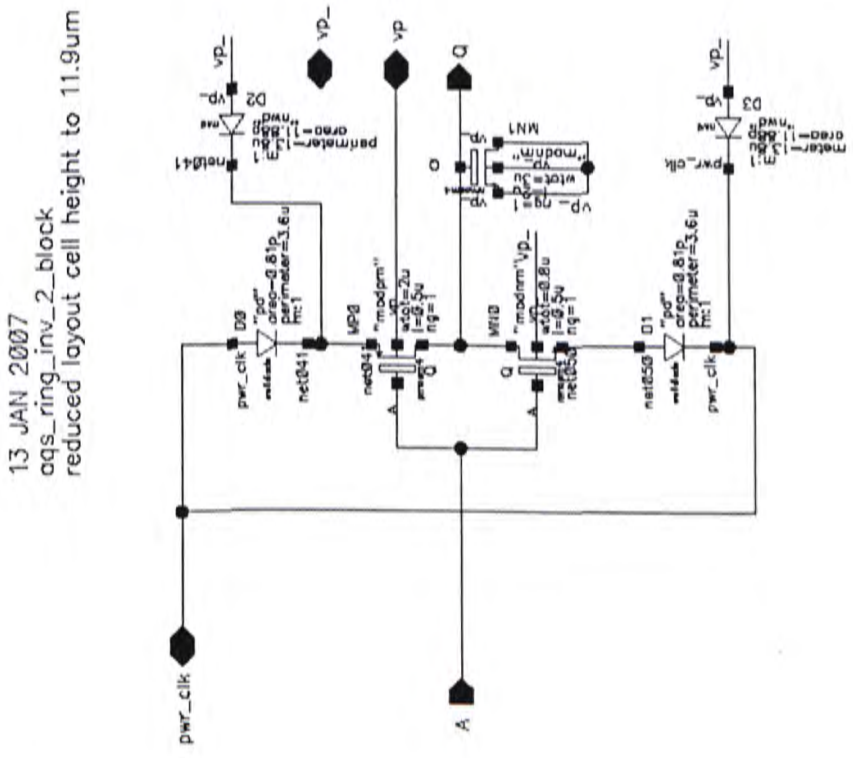

23 JAN 2007
POR2_block
released
vp
MP25
"modpm"
net0142
wtot=1u
l=0.5u
ng=1
MN0
"modnm"
wtot=0.5u
l=25u
ng=1
"rpolyh"
R0
r=30000
w=1u
l=20u
m
RN_in
C0
C1
C2
C3
"cpoly"
c=251.98f
area=2.86e-10
perimeter=7
m=1
net0262
MP39
vp_

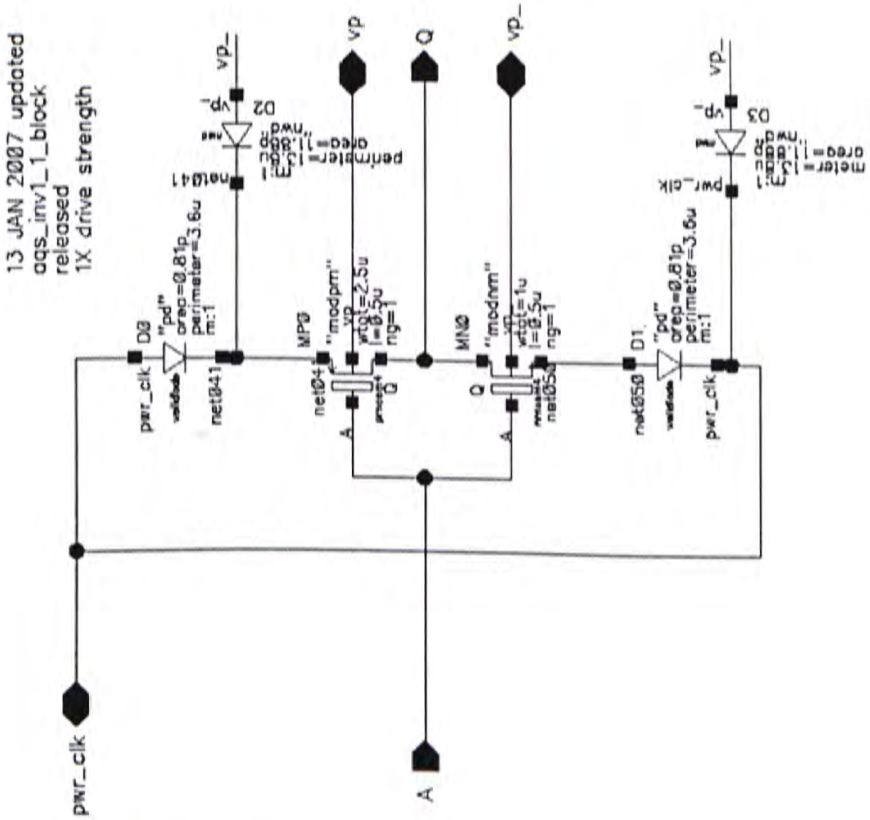

5 JAN 2007
opp_DFF_TL_RN_preset2s_block
D flip flop
active low preset
rising edge triggered
released
Q
CLKI
CLKS
R
pwr_clk1
pwr_clk2
Vp
Vn_
RN
C
D

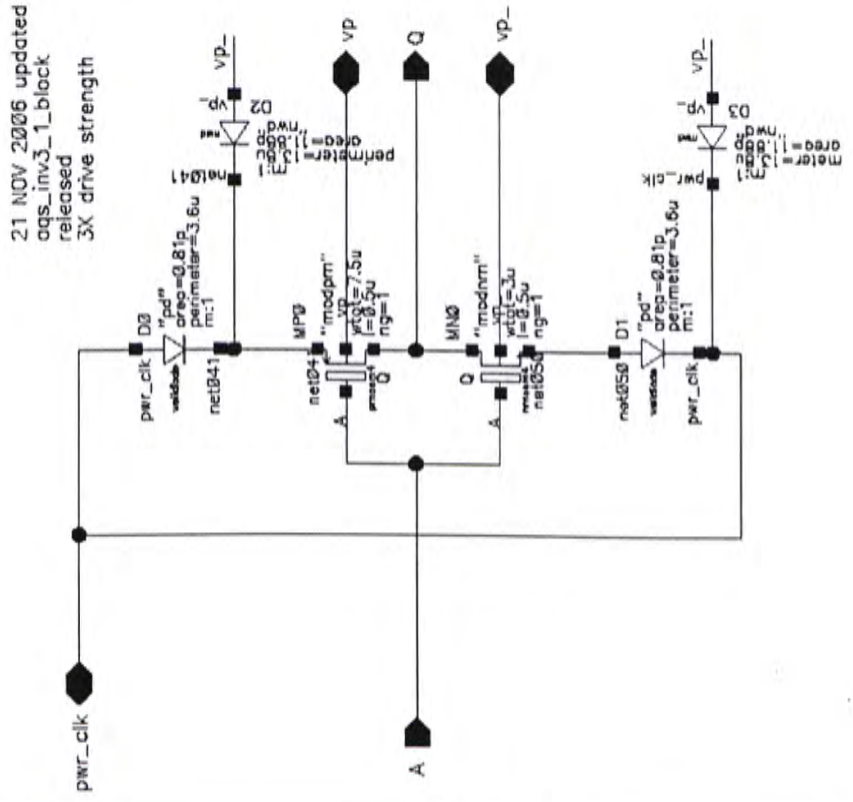

3 JAN 2007
ege_DFF_TL_RN_clear1a_block
D flip flop
active low clear
rising edge triggered
released
CLKN
CLKS
pwr_clk1
pwr_clk2
Q
D
RN

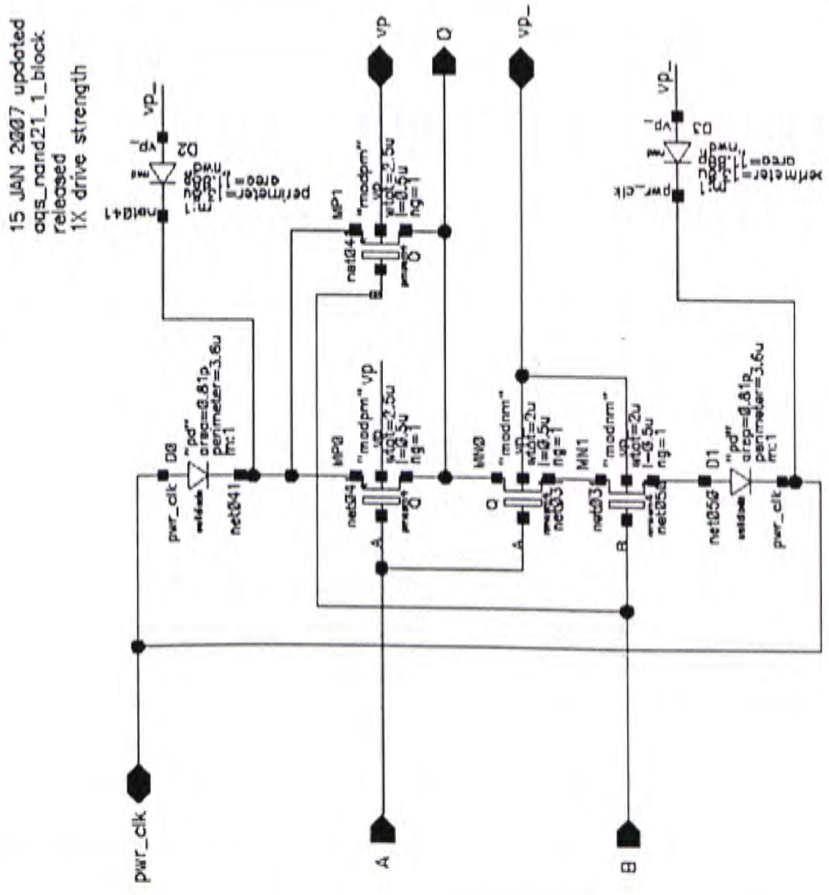

18 JAN 2007
aqs_DFF_TSPC_RN_clear1B
10fF cap added at QN
D flip flop
active low clear
rising edge triggered
released
Q
QN
RN
pwr_clk2
pwr_clk1
vp
vp_
D
C

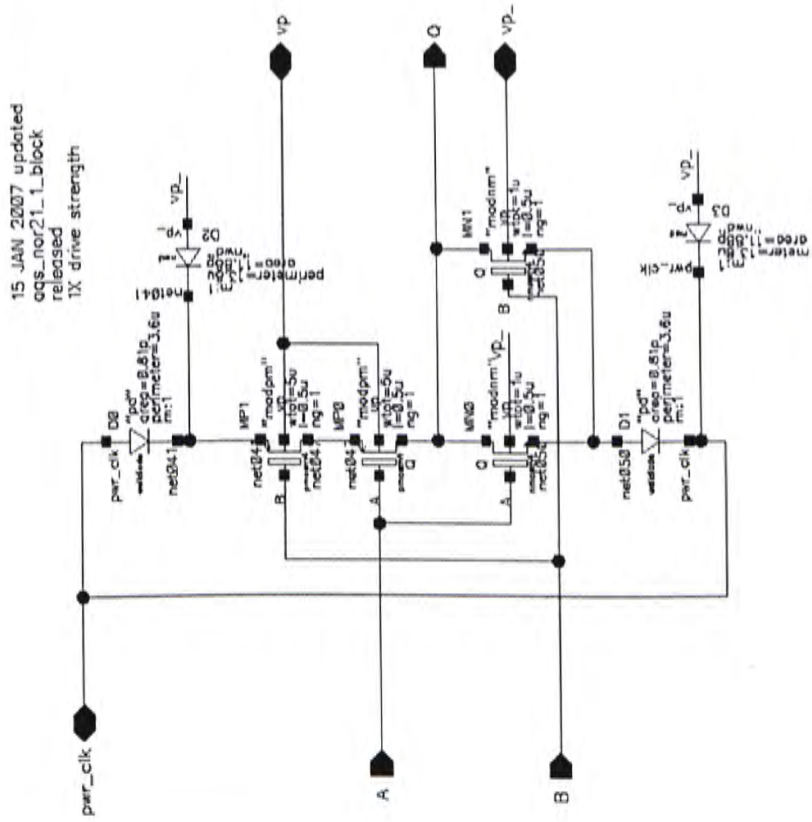

18 JAN 2007
qas_DFF_TSPC_RN_clear3B
10fF cap added at QN
3X drive strength
D flip flop
active low clear
rising edge triggered
released
Q
QN
RN
pwr_clk2
pwr_clk1
vp
vp_
D
C

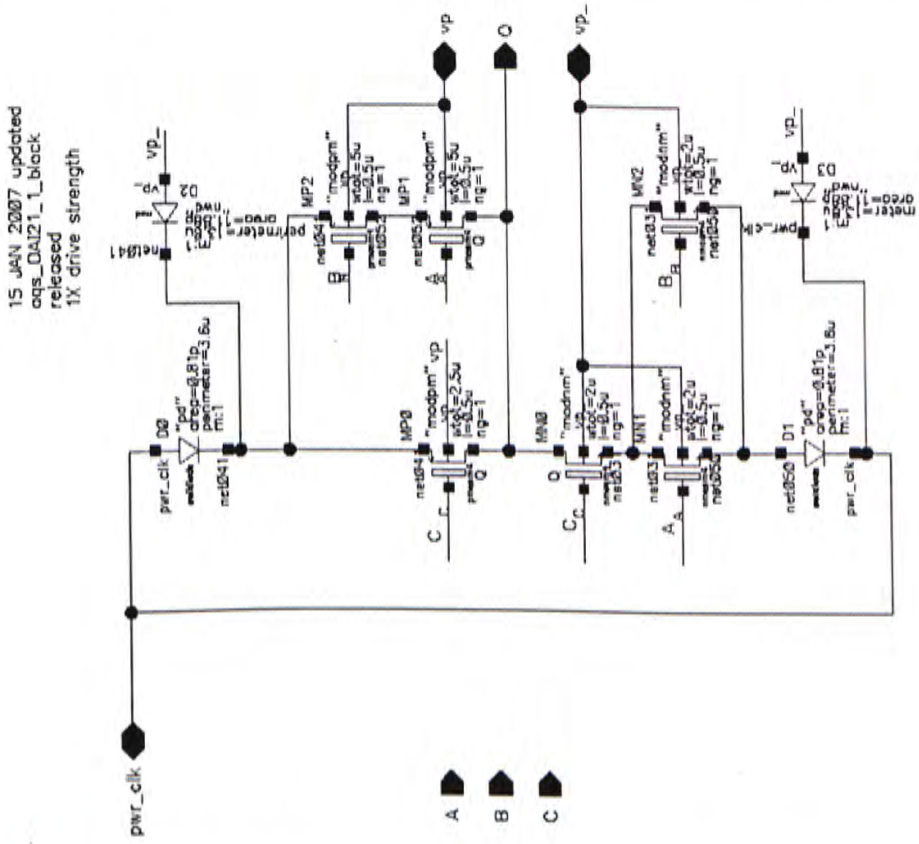

13 JAN 2007
aqs_ring_inv_2_block
reduced layout cell height to 11.9um
pwr_clk
A
Q
vp
vp_
D0
D1
D2
D3
MP0
MN0
MN1
net041
net058
"pd"
"modpm"
"modnm"
pwr_clk


13 JAN 2007 updated
aqs_inv1_1_block
released
1X drive strength
pwr_clk
A
Q
vp
vp_
D0
D1
D2
D3
MP0
MN0
net041
net058
"pd"
"modpm"
"modnm"
pwr_clk


21 NOV 2006 updated
aqs_inv3_1_block
released
3X drive strength
pwr_clk
A
Q
vp
vp_
D0
D1
D2
D3
MP0
MN0
"pd"
"modpm"
"modnm"
net041
net034
net033
net058
net056
pwr_clk


15 JAN 2007 updated
aqs_nand21_1_block
released
1X drive strength
pwr_clk
A
B
Q
vp
vp_
D0
D1
D2
D3
MP0
MP1
MN0
MN1
"pd"
"modpm"
"modnm"
net041
net034
net033
net035
net058
net056
pwr_clk


15 JAN 2007 updated
aqs_nor21_1_block
released
1X drive strength
vp
Q
vp_
pwr_clk
A
B
MP1
MP0
MN1
MN0
D0
D1
D2
D3


15 JAN 2007 updated
aqs_DAU21_1_block
released
1X drive strength
vp
Q
vp_
pwr_clk
A
B
C
MP2
MP1
MP0
MN2
MN1
MN0
D0
D1
D2
D3